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	MODEL 3Ø INTERFACE SPECIFICATION	M3ØIS/S-19

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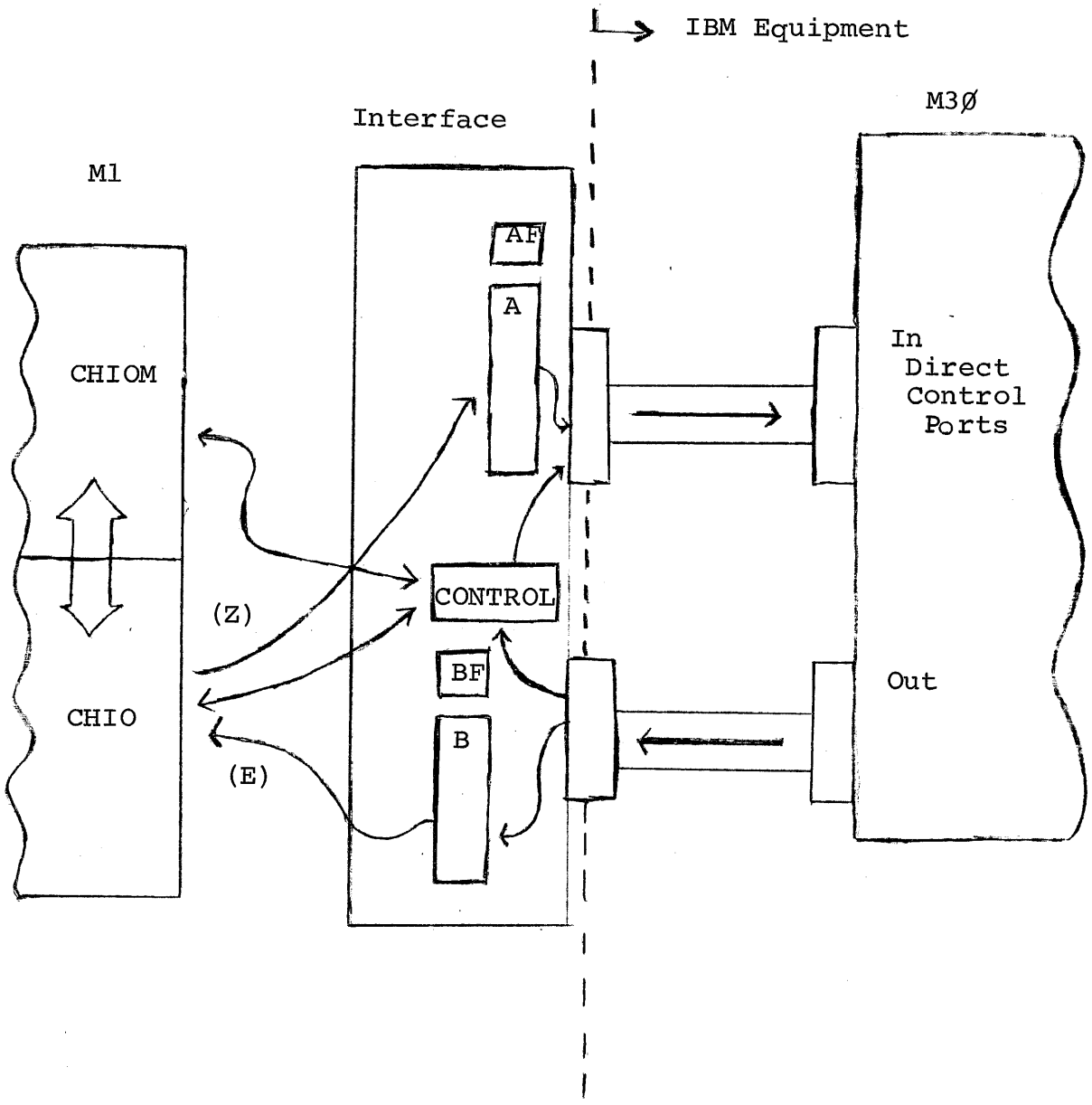
ABSTRACT and CONTENTS

This document describes the signals involved in the interface of the IBM System 360 Model 30 (M3Ø) with the Model 1 (M1).

I. Introduction

The M1/M3Ø interface will handle 8-bit parallel transfers via the direct control feature on the M3Ø and a high speed line on the Phase I CHIO Multiplexer. The Interface will be comprised of a receiver buffer (B), transmitter buffer (A), buffer full/empty flags (BF, AF), and all logic required to process the M1 and M3Ø signals. Communication between the M3Ø and the Interface will be accomplished via standard IBM cables (No. 535392Ø, 92±10Ωcoax, 50' length) with IBM connectors (No. 5353867 and 5353868, and No. 5362302 Serpent contacts) at each end. Figure 1 presents the Interface in block diagram form.



Interface Block Diagram

Figure 1

II. Interfacing to M3Ø signals

The essential M3Ø direct control signals associated with the Interface are described in IBM Manual A22-6845-2. Briefly, they are understood to be the following:

1. Direct Control Bus-Out--A set of 8 parallel output lines onto which high true data is placed during the execution of a M3Ø Write Direct instruction.
2. Write-Out--A single high true output pulse which indicates that data on the Direct Control Bus-Out is not yet valid for the Write Direct being executed.
3. Read-Out--A single high true output pulse which indicates that a Read Direct is being executed and that valid data must be provided on the Direct Control Bus-In, as indicated by the Hold-In signal.
4. Direct Control Bus-In--A set of 8 parallel input lines which carry high true data into the M3Ø during the course of a Read Direct instruction.
5. Hold-In--A single low true input pulse which enables the reading of data on Direct Control Bus-In and thus the completion of a

Read Direct instruction. (The M3Ø will hang-up waiting for this signal in the course of the Read Direct.)

6. Timing Signal Bus-out--A set of 8 parallel output lines which provide high true timing pulses during a Read or Write Direct as determined by bits 8-15 of the instruction. Two such signals are planned for use as follows:

    A. Timing Signal 1 (TS1) is sent by the M3Ø along with Read-Out to indicate that the Read Direct being executed is for the purpose of data transfer.

    B. Timing Signal 3 (TS3) is sent by the M3Ø along with Read-out to indicate the Read Direct being executed is for the purpose of synchronizing a following Write Direct.

7. External Signal Bus-In--A set of 8 input lines, six of which are used, providing access to the M3Ø external interrupt mechanism via high true pulses which may occur at any time. Ext Bus-In 2 and 3

are used as follows:

A. Ext Bus-In 2 (INT 2) is to be used to signal the M3Ø that a control character (and not data) is being sent. These characters serve to signal the beginning and end of M1 to M3Ø transfers.

B. Ext Bus-In 3 (INT 3) is to be used to signal the M3Ø that ZM (either Master ZM or CHIO Local ZM) has been energized and that this fact may be the cause of any interruption in communication.

The sequence of events for transfer of bytes from the M3Ø to the Interface will be:

1. The M3Ø will execute a Sync Read Direct prior to the execution of the Write Direct which will transfer data out. This Sync instruction is sensed at the Interface by the latching of Read-Out /\TS3.

2. The Interface determines whether a new byte may be received from the

M3Ø by checking its receiver buffer flag (BF) for an empty condition. If BF is true, the CHIOM has not taken the previous byte so the new character cannot be allowed to be sent. The interface will then inhibit the transfer by keeping Hold-In high until BF falls. When BF indicates empty (whether initially or after a wait) the Hold-In line will be dropped and the Sync Read Direct will then be completed. (The M3Ø will ignore data read-in on such Sync operations).

3. After completion of the Sync instruction, the M3Ø will execute a Write Direct instruction and will indicate that data out is valid by the Write-out pulse. The byte will be strobed into the Interface at the fall of Write-out and BF will be set. Note that data stored in B will be low true.
4. The process may be repeated from Step 1. Note that bits Ø and 1 from

the M3Ø are complemented by Interface hardware to save software time in the M3Ø.

The sequence of events for transfers from the Interface to the M3Ø will be:

1. Transmitter buffer (A) is loaded with high true data; if the EOR of bits Ø and 1 is true, a control character is awaiting transmission and Interrupt 2 will be sent to the M3Ø.
2. The M3Ø will then initiate an actual Read Direct (as opposed to the Sync) by sending TS1 concurrently with Read-Out. The Interface will drop Hold-In and the byte will be read into the M3Ø; the process may then be repeated. Note that Hold-In is dropped only after AF has been set for 100ns and Read Direct signals have been received from the M3Ø.

III. Interfacing to CHIOM Signals

The essential CHIO and CHIOM Signals associated with the high speed lines are described in the CHIO

Multiplexer Specification NCHIO/S-17. They are briefly described below:

A. Signals entering the Interface from CHIO or CHIOM

1. 8-bit character from the Z bus (XZ(16)-XZ(23), high true)
2. Transmitter On XZ(13) (TON normally high)
3. Receiver On XZ(14) (RON normally high)
4. Send character XZ(12) (POT is for output, not control)
5. Two Device Address Register (DAR) hot shot lines
6. Two Scanner hot shot lines
7. INPUT and OUTPUT (100ns pulses during a PIN or POT)
8. K2'
9. Device Address bit 17 (DA17 high for Modem)

B. Signals leaving the Interface to CHIO or CHIOM

1. 8-bit character to the E bus (E(16)-E(23), low true)
2. Transmitter flag (low true AF output means A buffer empty)
3. Receiver flag (low true BF' output means B buffer full)
4. Receiver request (RREQ' low true)
5. Transmitter request (TREQ' low true)
6. Unused output lines tied high:
   a. clear to send

b. carrier detector

c. data set ready

7. Unused output lines tied low:

a. transmit rate error

b. receiver rate error

c. error

The sequence of events for transfer of bytes from the M1 to the Interface will be briefly as follows:

1. The Interface will be checked periodically by the CHIOM Scanner for transmitter or receiver requests. When scanned, a transmitter request is sent if A is not full and TON is high (similarly for receiver requests with B full and RON high). RON and TON are latched from XZ(13) and XZ(14) respectively when a POT is done to the Interface.
2. Upon encountering a request, the Scanner will halt and set the CHIO attention Latch 2.
3. The CHIO will obtain the request information from the Scanner, allowing the latter to resume normal functioning.
4. The CHIO sends ALERT to the Device Address Register and the requesting

address is loaded causing two of 16 hot shot lines to energize. Depending upon the nature of the request, INPUT or OUTPUT is generated at Alert/K2.

5. If the request being serviced is from the transmitter, then at OUTPUT/K2 register A is loaded from Z and shortly thereafter AF is set. Interrupt 2 is sent to the M3Ø if the byte loaded is found to be a control character. Data transfer then proceeds as outlined in Section II with AF being reset when Hold-In returns high upon completion of the Read Direct. Note that TON and RON are sampled from Z also.
6. Regardless of the request type, the receipt of the DAR hot shot lines and DA17 enables the outputs of the receiver buffer to the E bus. If the request were for input, then the data would be strobed and BF would be reset at INPUT/K2.