bcc	title	prefix/class-number.revision
	SYSTEM CONTROL, CLOCKS AND POWER	SCCP/S-3.1

checked	authors	approval date / revision date
checked	S. Dinsmore	9-11-69 / 9/2/69
approved		classification: Specification
		distribution: company private / pages: 21

ABSTRACT and CONTENTS

This document describes the functional specifications of the Model 1 System Clock pulses and the System Control over the power and clock turn-on and turn-off cycles. It also specifices the manner in which a local unit interfaces with the system controller and the manner in which a unit may be locally turned on and off. System design criteria are given for all power supplies.

1.0 SCOPE

This document describes the functional specifications of the Model 1 System Clock pulses and the System Control over the power and clock turn-on and turn-off cycles. It also specifies the manner in which a local unit interfaces with the system controller and the manner in which a unit may be locally turned on and off. System design criteria are given for all power supplies.

2.0 SYSTEM CLOCKS

2.1 General Description

The System Clock Generator creates a master clock pulse, called K1, which is destributed to all units in the system. It also creates a series of precisely timed pulses for the Fast Memory. A system reference time, called t_0, is defined.

2.2 Reference Time and Phasing of Clocks

2.2.1 Reference Time

The system reference time, t_0, is a fictitious point in time which occurs cyclicly at the repetition rate of the clock. t_0 is said to occur simultaneously throughout the machine. The occurance of all clock pulses is measured in time with respect to t_0. These times may be - or +, i.e., before or after t_0.

2.2.2 Phasing of Clocks

Since all clock pulses are relative to t_0, any convenient point may be chosen. This point in time is normally chosen to be at the fall of K2 in any one unit, then all other pulses are relative to this one point. A K1 clock pulse for each unit in the system is derived from a common Master Clock pulse in the clock generator. Each K1 line has an individual delay adjustment to compensate for varying cable lengths. The total delay in each K1 clock line must be the same plus or minus any small adjustments at an individual unit. In particular it cannot be assumed that the delays may be related by a non-identical integral number of clock periods, because under this condition any variation of clock period would disturb the relationship of the clocks to t_0 and therefore to each other.

K1 occurs in the clock generator prior to t_0 by an amount at least equal to the total delay in the K1 clock lines.

2.3 The Master Clock (K1)

2.3.1 Period

a) Mode 1, fixed - the principal clock period shall be nominally 100 nsec, crystal controlled. Crystals producing a period of 90 to 110 nsec shall be acceptable.

b) Mode 2, fixed - a secondary clock period shall be twice that of mode 1, crystal controlled.

c) Mode 3, variable - the clock period shall be capable of being varied from 90 nsec to 220 nsec.

2.3.2 Pulse Polarity

The master clock pulse shall be a negative pulse as distributed to the units from the Clock Generator.

2.3.3 Pulse Width

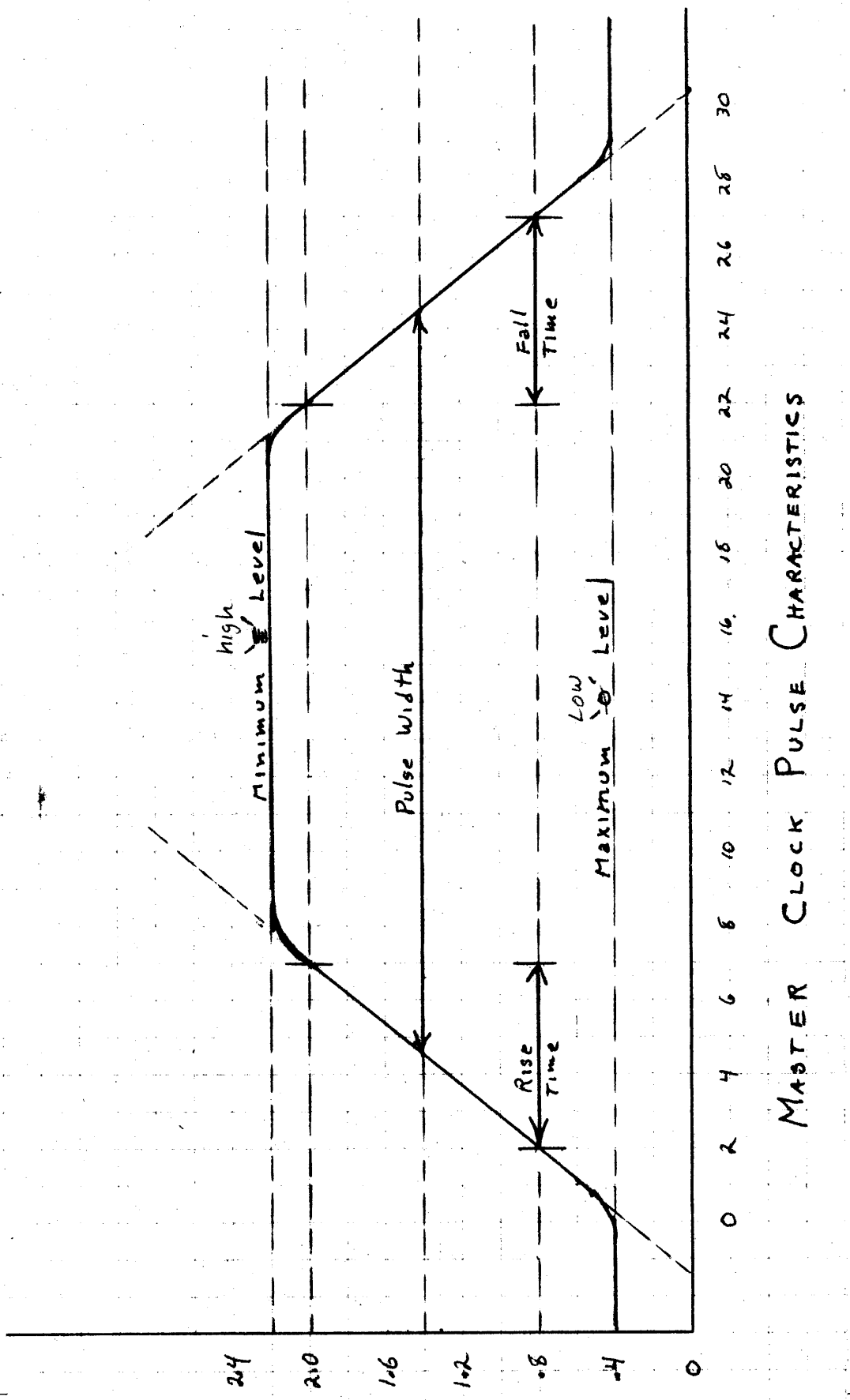
The master clock pulse shall be 20 nsec $\pm$ 2 nsec as measured at the 1.4 volt points. The pulse width shall also be capable of being varied from 15 nsec to 35 nsec.

2.3.4 Pulse Rise and Fall Times

The master clock pulse shall have a rise time and a fall time $\leq$ 5 nsec as measured at the +.8 and the +2.0 volt points at the output of the unit cable receiver (see Figure 1).

2.3.5 Pulse Levels

The master clock pulse low level shall be $\leq$ +.4 volts and the hi level shall be $\geq$ +2.2 volts, both values being measured at the unit cable terminating resistor.



MASTER CLOCK PULSE CHARACTERISTICS

Figure 1

2.3.6 Impedance

The cables between the Master Clock Generator and the receiving units in the system shall be Microdot 260-3919, or equivalent, which has a characteristic impedance, Z_0, of 100 ohms. Each cable shall be terminated at the receiving end with 200 ohm to 5 and 200 ohm to ground and a paralleling load no greater than that presented by a 74H40N integrated circuit.

2.4 Fast Memory Clock Pulses

2.4.1 General Description

The Fast Memory Clock pulses are a series of pulses displaced from the reference time, t_0, and from each other. They are of various pulse widths and polarities. The delay of the entire group of pulses is adjustable as a group. The delay and pulse width of each individual pulse is also adjustable. All delays of the fast memory clock pulses are with respect to t_0. A reference Clock Pulse is also transmitted to the Fast Memory to facilitate the adjustment of the phasing.

2.4.2 Group Delay

The group delay of the Fast Memory Clock pulses shall be defined to be the delay, with respect to t_0, of a common pulse used to generate the various Fast Memory Clock Pulses minus the common delay

of the K1 clock lines. The group delay is normally the values shown in Table 1.

2.4.3 Pulse Delay

The delay of each pulse of the Fast Memory Clock pulse group shall be individually adjustable to the values shown in Table 1. The tolerance on the nominal values shall be $\pm$2 nsec.

2.4.4 Pulse Width

The pulse width of each pulse of the Fast Memory Clock pulse group shall be individually adjustable to the values shown in Table 1. The tolerance on the nominal values shall be $\pm$ 2 nsec.

2.4.5 Other Characterisitcs

The rise time, fall time, and levels of each of the Fast Memory Clock pulses shall be as specified for the Master Clock Pulse. See paragraphs 2.3.4 and 2.3.5. The polarity of each pulse on the cables is indicated in Table 1. Pulse widths shall be measured as specified for the Master Clock Pulse. See paragraph 2.3.3.

2.4.6 Other Outputs

a) A logic level shall be made available which indicates MODE 1 mode of operation.

TABLE 1

Pulse Name	Pulse Width nominal value	Pulse Width minimum nominal range	Mode 1** delay from t_0 nominal value	Mode 1** delay from t_0 minimum nominal range	Mode 2** delay from t_0 nominal value	Mode 2** delay from t_0 minimum nominal range	Mode 3** delay # from t_0 minimum nominal range	Pulse Polarity
TOS	78	65-90	11	5-25	111	105-125	5-125	–
TS	20	15-35	18	13-20	118	113-130	13-130	–
TQ	20	15-35	25	15-35	125	115-135	20-135	+
TJ	70	60-70	30	20-40	130	120-140	20-140	–
SG	20	15-35	35	25-45	135	125-145	25-145	+
TRD	20	15-35	38	25-50	138	125-150	25-150	–
TG	35	25-50	39	25-50	139	125-150	25-150	–
TM	70	60-80	62	50-75	162	150-175	50-175	–
TO	20	15-35	73	60-85	173	160-185	60-185	+,–
TI	20	15-35	73	60-85	173	160-185	60-185	–
FM Group*	N/A	N/A	-10	-20 to +55	90	55-145	-20 to +145	

* The group delay is from t_0 to a common pulse from which the individual clock pulses are generated. Δt_0 must be added to the delay values above when t_0' is used as a reference.

** With group delay set at -5.

\# This is a summation of modes 1 and 2 but with the Master Clock Period variable.

b) A pair of logic levels at +5 volts and -5 volts respectively shall be made available which selects one half Core Memory operation or full Core Memory operation.

c) Four logic lines shall be provided which select the Quadrant of Core Memory, J,K,L, or M, to be enabled.

2.5 Electrical Reactions to Operator Controls

The Master Clock Generator shall react cleanly to all operator controls. There shall be no pulse splitting or pulse doubling upon the changing of period or delays. It shall not be required to stop the clock prior to changing period modes; however, it is permissible to allow the clock period to be longer than normal during the transition between modes.

2.6 Master Clock Regeneration at Each Unit

The K1 Master Clock received by each Unit shall be synchronously gated by the local clock ON/OFF signal. The K1 clock shall be regenerated from the gated input K1 clock and the delay and pulse width shall be variable from 0 to 50 ns.

3.0 TURN-ON AND TURN-OFF OF THE MASTER CLOCK GENERATOR

3.1 General Description

The Master Clock Generator generates a series of Fast Memory pulse groups prior to and after the Master Clock pulse is turned on or off, respectively, in order to complete all Central Memory cycles. This sequence occurs any time the clock generator is turned on or off, whether manually or automatically.

3.2 Turn-on

The Master Clock Generator shall transmit a minimum of 64 (32 in Mode 2) Fast Memory Clock Pulse Groups to the Fast Memory before the Master Clock Pulse Train is turned on.

3.3 Turn-off

The Master Clock Generator shall transmit a minimum of 64 (32 in Mode 2) Fast Memory Clock Pulse Groups to the Fast Memory after the Master Clock Pulse Train is turned off prior to turning off the Fast Memory Clock Pulse Group Train.

3.4 Cleanliness of Turn-on and Turn-off

The Master Clock Generator shall be turned on and off cleanly. There shall be no pulse splitting of any of the pulses transmitted.

4.0 SYSTEM TURN-ON and TURN OFF CYCLES

4.1 General Description

The System turn-on and turn-off cycles consist of specific sequences of conditions and events. For turn-on these are:

a) Initial conditions - The main AC Circuit Breaker is off, the +5 volt Battery supply is operating, the Real Time Frequency Source is operating on its internal Battery, the $\overline{ZM}$ line is grounded.

b) The three phase main AC circuit breaker is closed. The three indicator lights on the control panel turn on, one for each phase.

c) The Pilot Power switch on the control Panel is turned on. This turns on the +5 volt pilot, the -5 volt pilot, the +12 volt pilot and apples AC power to the Core Memory Pilot supplies.

d) The Master Power ON push button is pressed. AC power is applied to all +5 volt and +10 volt power supplies. When the +5 volt reaches a preset threshold, AC power is applied to the -5 volt power supplies. The time delays are also started when the push button is pushed.

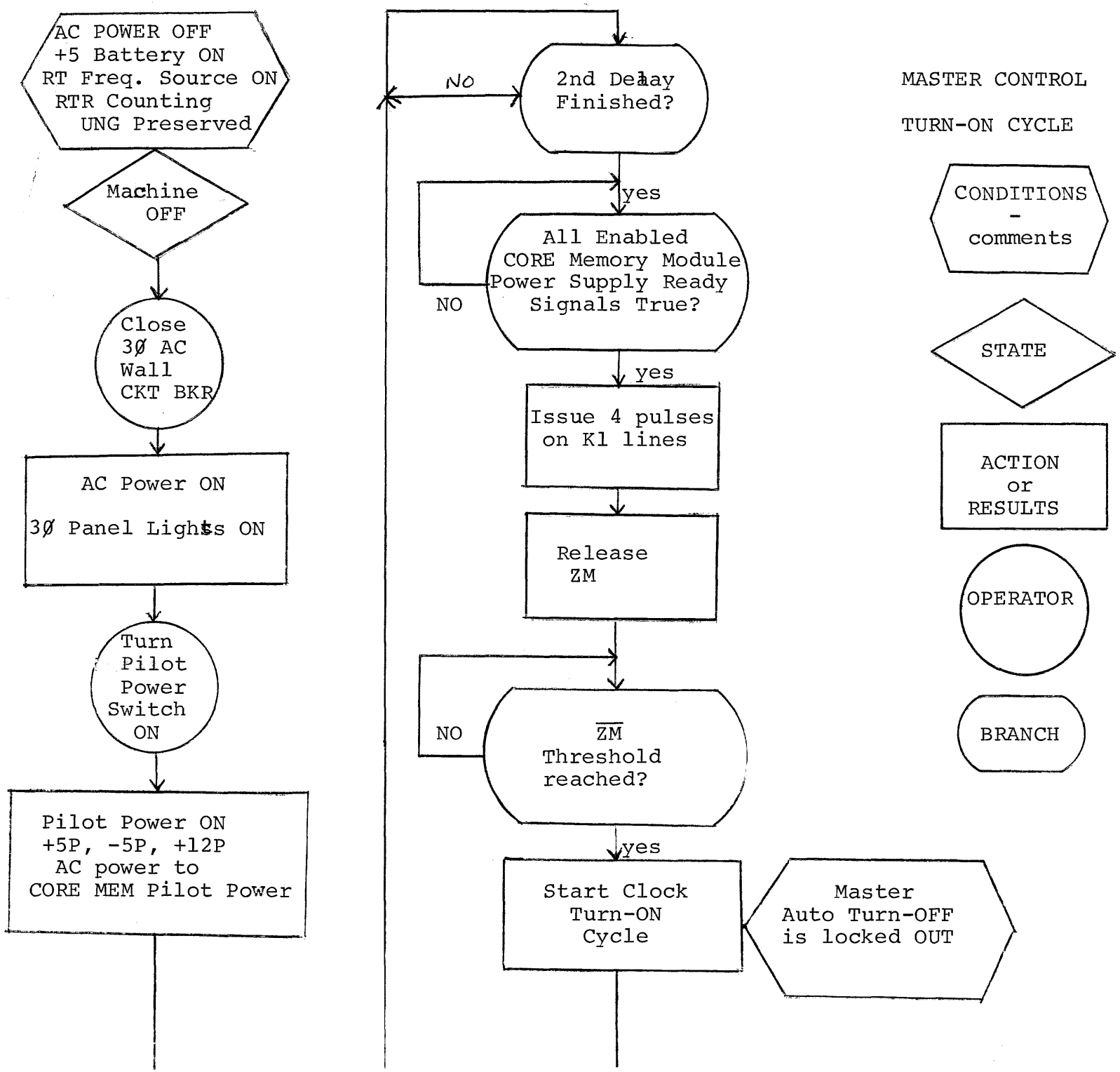
e) All of the supply voltages in each unit are monitered and a logic level is supplied to the Master Controller indicating that all power in the unit is within preset tolerances. In addition there is an AC power fault detector which also supplies a signal to the Master Controller.

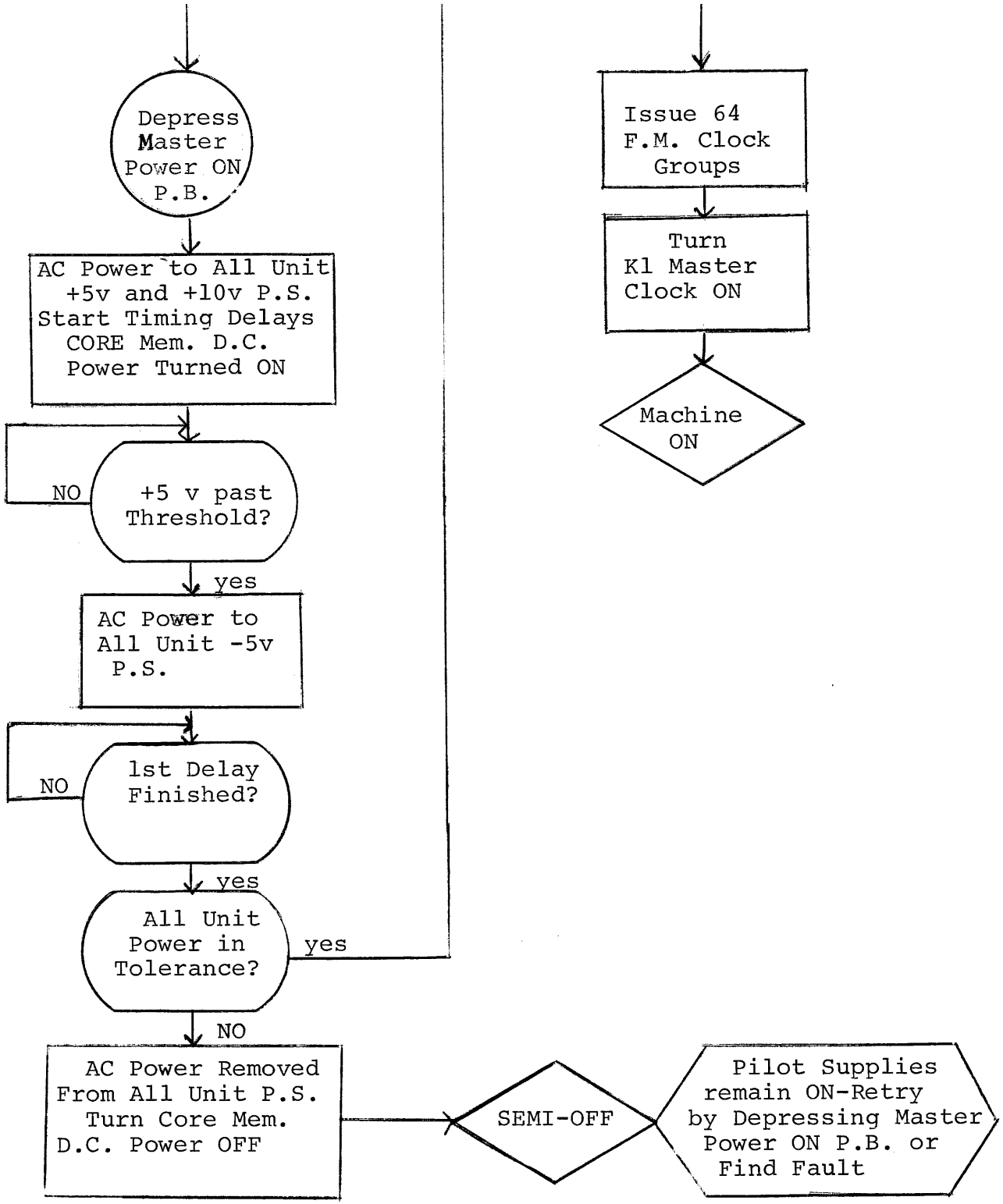
f) At the end of the first delay (approximately .2 sec) the AC power is removed from all power supplies, except the pilot supplies, if any of the Unit power supplies are not in tolerance.

g) At the end of the second delay (approximately 2 sec, required because of the characteristics of the Core Memories) the system waits until all of the Core Memory Power Supply Ready (PSR) signals become true before proceeding.

h) When all Core Memory PSR's become true four pulses are issued on the K1 clock lines. These serve to "copy ZM" into all microprocessors, initializing their starting points. These pulses are 2.56 ms apart. $\overline{ZM}$ is then released from ground.

i) When $\overline{ZM}$ has reached a threshold which assures that all logic attached to the ZM line has


AC POWER OFF
+5 Battery ON
RT Freq. Source ON
RTR Counting
UNG Preserved
Machine OFF
Close 3Ø AC Wall CKT BKR
AC Power ON
3Ø Panel Lights ON
Turn Pilot Power Switch ON
Pilot Power ON
+5P, -5P, +12P
AC power to
CORE MEM Pilot Power
NO
2nd Delay Finished?
yes
All Enabled
CORE Memory Module
Power Supply Ready
Signals True?
NO
yes
Issue 4 pulses on K1 lines
Release ZM
NO
$\overline{ZM}$ Threshold reached?
yes
Start Clock Turn-ON Cycle
Master Auto Turn-OFF is locked OUT
MASTER CONTROL
TURN-ON CYCLE
CONDITIONS - comments
STATE
ACTION or RESULTS
OPERATOR
BRANCH


Depress Master Power ON P.B.
AC Power to All Unit +5v and +10v P.S. Start Timing Delays CORE Mem. D.C. Power Turned ON
NO
+5 v past Threshold?
yes
AC Power to All Unit -5v P.S.
NO
1st Delay Finished?
yes
All Unit Power in Tolerance?
yes
NO
AC Power Removed From All Unit P.S. Turn Core Mem. D.C. Power OFF
SEMI-OFF
Pilot Supplies remain ON-Retry by Depressing Master Power ON P.B. or Find Fault
Issue 64 F.M. Clock Groups
Turn K1 Master Clock ON
Machine ON

received the high logic level correctly the Master Clock is started in its turn on cycle. At the completion of this cycle the machine is ON.

For turn-off the sequence conditions and events are:

a) The machine is ON.

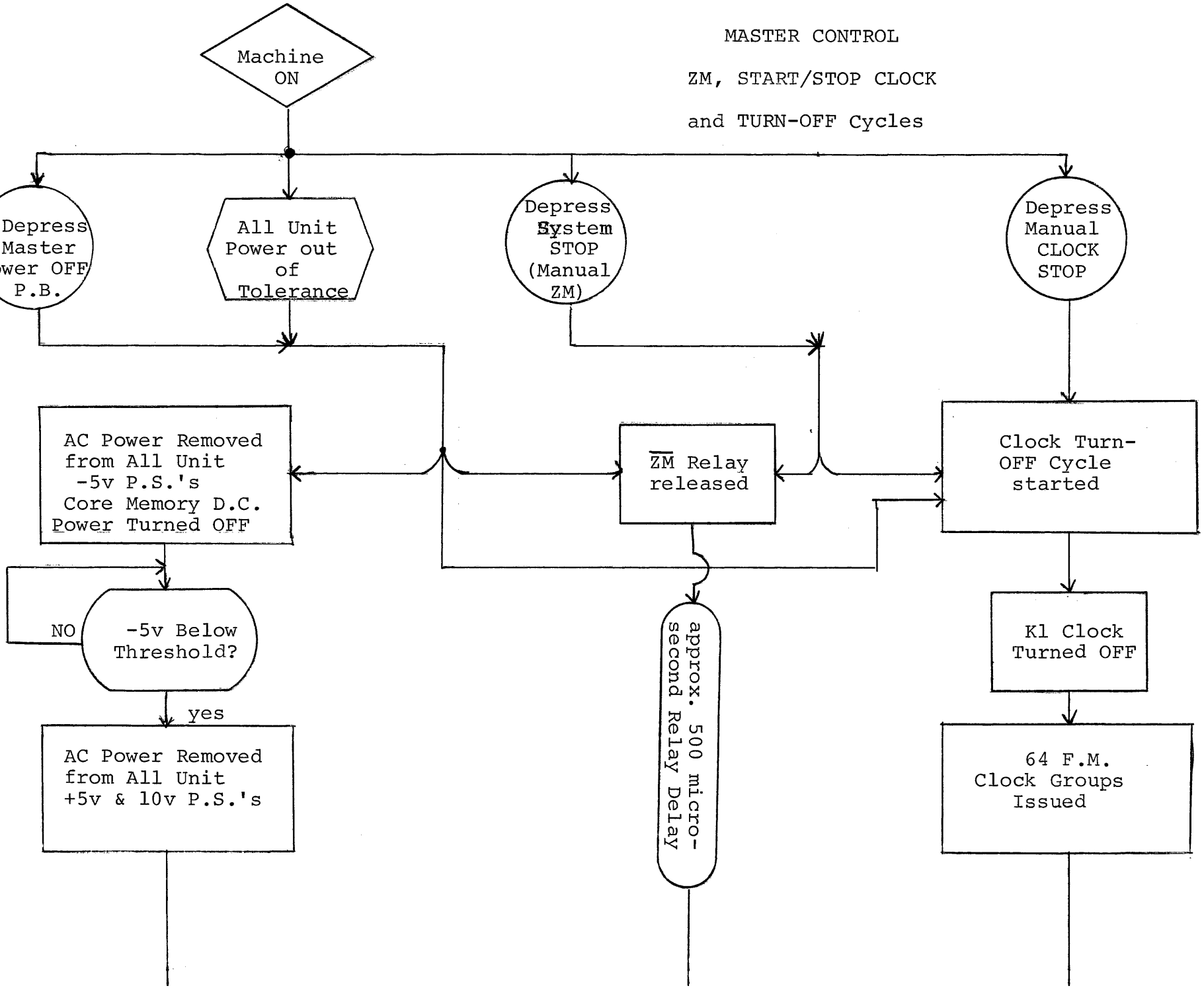
b) The Master Power OFF push button is pressed. This immediately starts the Master Clock turn off cycle and starts to apply ground to the ZM line. Ground is actually applied 500 to 1000 microseconds later due to the relay delay.

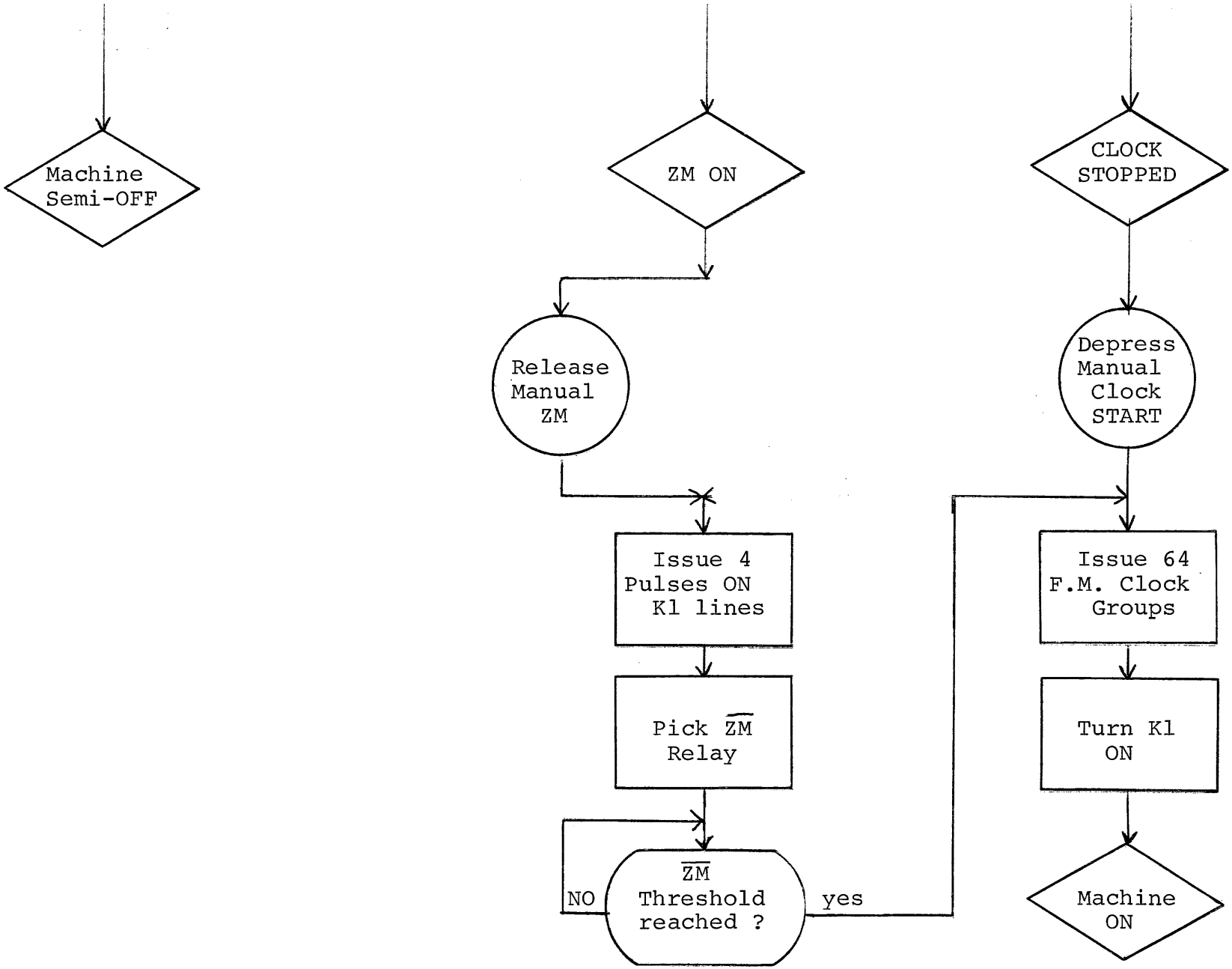
c) The AC power is removed from all unit -5 volt power supplies about 2 ms after the OFF push button is pressed. When the -5 volt supply has reached a low threshold the AC power is removed from all other unit power supplies. The pilot supplies remain on.

d) The Pilot Supplies may be turned off. If the Main AC Power Breaker is opened the system reverts to the initial conditions noted for the turn on cycle.

MASTER CONTROL

ZM, START/STOP CLOCK and TURN-OFF Cycles




Machine Semi-OFF
ZM ON
Release Manual ZM
Issue 4 Pulses ON Kl lines
Pick $\overline{ZM}$ Relay
$\overline{ZM}$ Threshold reached ?
NO
yes
CLOCK STOPPED
Depress Manual Clock START
Issue 64 F.M. Clock Groups
Turn Kl ON
Machine ON

When the System is ON the Master Clock may be cycled on and off manually. ZM may be manually activated. This is also called System STOP (see specification SR/S-8). The turn off cycle of the Master Clock is started and ground is applied to the ZM'line about 1 ms later. Upon the release of the manual activation of $\overline{ZM}$ the turn on cycle is entered at step h as if the PSR's had just become true.

After the ZM'has been released from ground during the Power turn ON, the Unit Power in tolerance Signal (UPO) and the Power Failure signal (PF) are prevented from turning the System Power off. Rather, if only one unit has a power failure, that unit's local turn-off cycle is initiated and the UPO'is send to the System Warning Register.

If the AC input power fails, PF is sent to the System Warning Register. The System turn off cycle is not initiated unless all UPO's go false.

All microprocessors, the fast memory, the MPMBM the TUIM and the CPU's may be put in a local control state at any time. If the Unit is already ON no change in operation takes place, but local initiation of the turn-on, turn-off, clock -on/clock-off (except

Fast Memory), ZM on/off may be made. In general the local turn-on/turn-off cycle is identical to the Master turn-on/turn-off cycle. One difference is that just prior to the release of ZM (LZM) four K1 pulses are gated onto the K1 clock line rather than four 2.56 ms period pulses.

4.2 Requirements -

Master and Local Control of Power-ON, Power-OFF, Zero-Machine, and Start/Stop Clock.

4.2.1 Sequencing

a) Power Supplies:

In any one Unit the -5 volt power supply if present shall be the last to be energized and the first to be deenergized, such that a wide margin of safety exists on all back biased transistors.

b) Inhibition:

During the Power Turn-on Cycle a failure of the AC input power on any one of the phases or the failure of any of the Unit Power Supplies to arrive at in-tolerance conditions within 250 msec shall cause the power control to revert to the OFF state. After the successful completion of the cycle these inhibitors shall themselves be inhibited.

c) Turn-OFF:

After successfully turning on the Master Power Control shall initiate a Turn-OFF cycle only if the Manual Master Power OFF push button is pressed or all Unit Power Supplies have gone out of tolerance.

If a Unit Power Supply goes out of tolerance, the Unit's Clock shall be gated off, the local ZM' initiated and the AC power removed from the Unit's Power Supplies in the order given above after a delay of 1 msec from the detection of the power supply fault.

d) Zero Machine (System STOP):

The ZM'line, which is common throughout the System, shall be grounded through a mercury wetted relay contact during the time of Zero Machine (or System STOP). Just prior to the ungrounding of the ZM' line the ZM Control shall cause a minimum of three pulses to be emitted by the Master Clock generator on the K1 clock lines. When a unit is in local Control the three pulses shall be gated input K1 pulses. When a unit is in remote control the local Manual ZM shall be inhibited. And when in local control or an automatically

induced unit power-down, the ZM' line shall be grounded in such a way so as not to interfere with the rest of the system. The Master Clock or local clock gates shall not be activated until the ZM' line reaches a minumum of 2.2 volts.

4.2.2 Local/Remote

When any unit, which has a Local/Remote Control, is in the Remote State, the local manual Power-on/Power off push button, the local manual ZM push button reset and the local manual start/stop clock switch shall be inactive. When a Unit is ON and running, swtiching from local to remote or from remote to local shall have no effect on the interaction of the Unit with the rest of the system during the switch-over.

4.2.3 Power Supply Tolerances

The tolerances for the various power supplies shall be:

a) $+5 \pm .25$ volts

b) $-5 \pm .5$ volts

c) $+10 \pm 1$ volt

4.2.4 Overvoltage Protection

In the event that a unit power supply has a crowbar (SCR) overvoltage protection circuit the

following settings shall be effected when measured at the bus within a unit:

a) on the +5 volt supply: +5.5 volts ± .1 volt

b) on the -5 volt supply: -5.5 volts ± .1 volt

c) on the +10 volt supply: +12 volts ± .2 volt

4.2.5 Operation Time in the Event of Power Failure

In the event of PF signal or any UPO level going false the power supplies shall have sufficient capacity to give reliable operation for 1 msec after the detection of the fault.

A +5 volt supply powered by a floating storage battery shall be provided to operate the Unique Name Generator and the Real Time Register for a minimum of eight hours.

4.2.6 Output Signals

All of the following logic signals shall be transmitted to the System Warning Register.

a) PF. This signal shall go true if any phase of the three phase input AC power fails. Detection shall occur within 4 msec of any power fault. Since the AC input is normally taken from the reserve power system the activation of this signal indicates a catastrophic power failure. In the abnormal circumstance of AC input power being

taken directly from the power utility the presence of this signal could also indicate a short duration power fault. Normally if this signal becomes true only a short time remains before the system automatically initiates a turn-off cycle because of power bus voltages falling out of tolerance.

b) UPO's. Each autonomous Unit except the Core Memories shall generate a UNIT POWER ON signal which shall indicate that all power busses are within tolerance. UPO' is used to set a corresponding bit in the System Warning Register if it occurs after ZM is released.

c) PSR's. Each Core Memory Module Power Supply generates a POWER SUPPLY READY signal. PSR' is used in the same manner as UPO'.

d) BD. This signal shall go true if the Storage battery powering the +5 Battery Supply is discharging.

e) RTBD. This signal shall go true if the storage battery powering the Real Time Frequency Source is discharging.

4.2.7 Indicators

a) Master Control Panel

Indicators shall be provided for the following conditions:

1) BD
2) ZM ON
3) Master Clock ON
4) FM Clock ON
5) Pilot Power ON
6) Master Power ON
7) The 3 phases of input AC power
8) RT Clock ON
9) Battery Power ON
10) Bits 0-23 of the ILR

b) Local Control Panel

1) ZM ON
2) Clocks gated ON
3) Pilot Power ON
4) Unit Power ON
5) Unit in Local Control