RECOMP II

COMPUTER SERVICE MANUAL

Autonetics Industrial Products
A DIVISION OF NORTH AMERICAN AVIATION, INC 3584 WILSHIRE BOULEVARD, LOS ANGELES 5, CALIFORNIA

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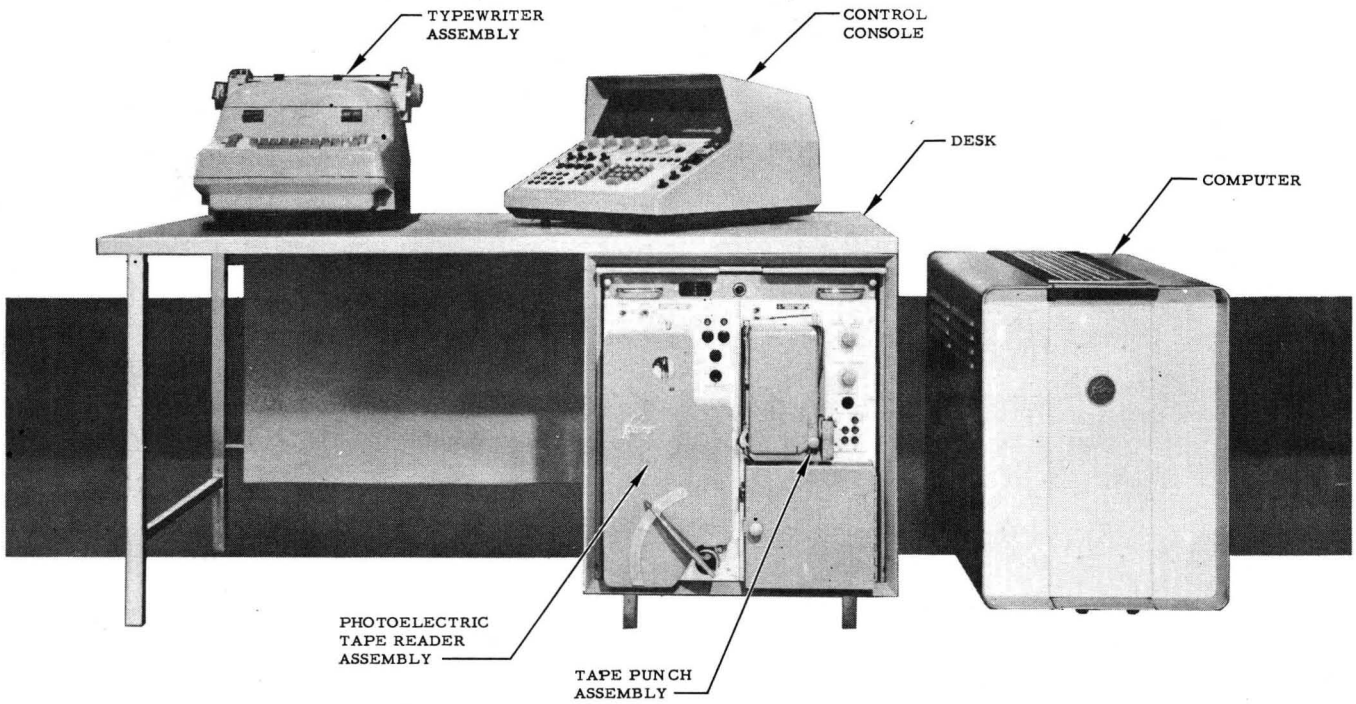

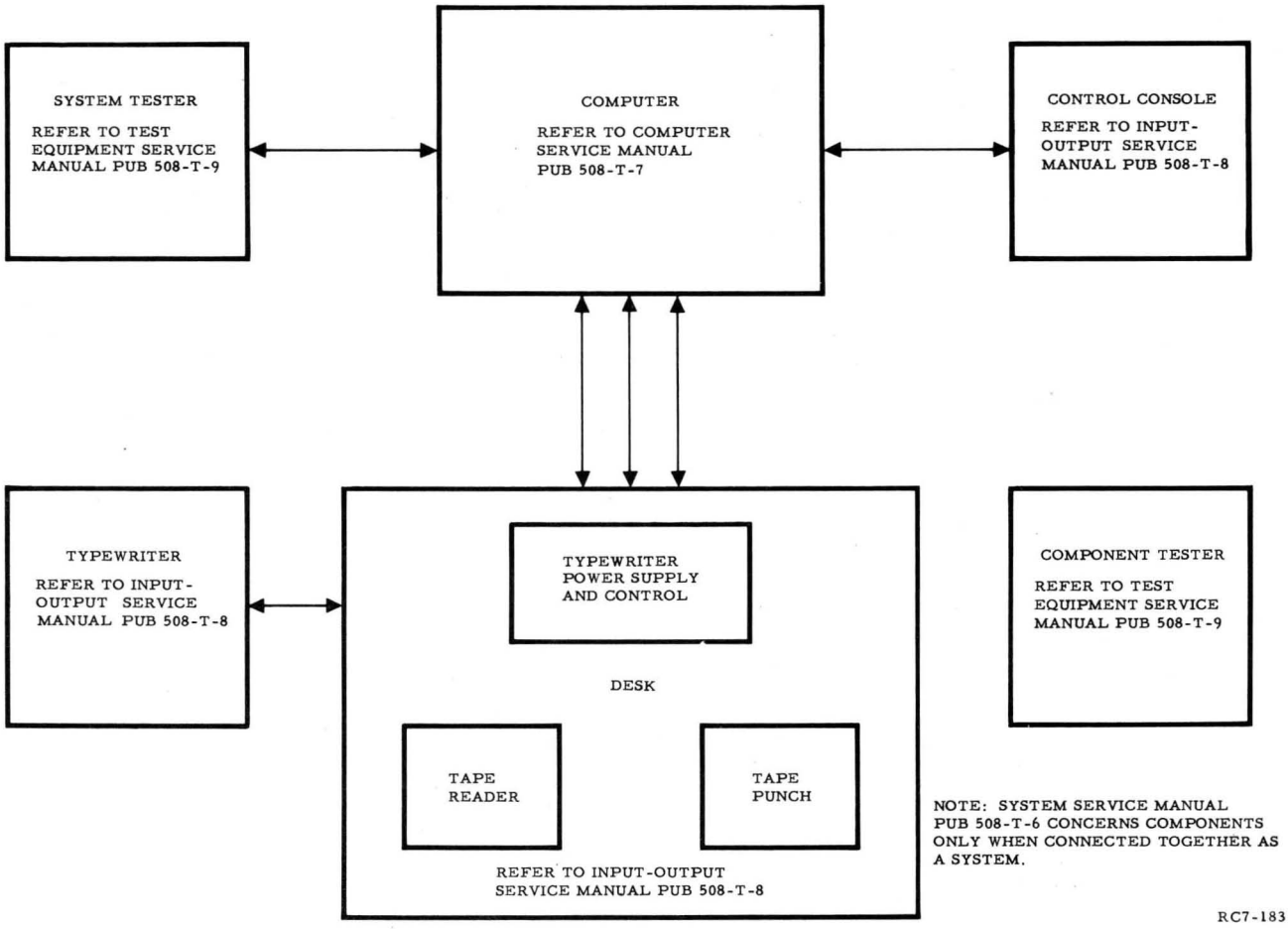

RECOMP II System Block Diagram

PREFACE

This manual is 1 of a set of 5 published by Autonetics to provide maintenance information on the RECOMP II computer system.

System Service Manual: Publication No. 508-T-6
Computer Service Manual: Publication No. 508-T-7
Input-Output Service Manual: Publication No. 508-T-8
Test Equipment Service Manual: Publication No. 508-T-9
System Reference Schematics: Publication No. 508-T-11

The block diagram of figure 1 illustrates each system component and shows its applicable service manual. In brief, the scope of each RECOMP II service manual is as follows:

System Service Manual: This manual describes the general concept of RECOMP II maintenance and provides operating instructions for checkout of the computer system using the system tester and both manual and automatic test routines. The goal of these system test procedures is to isolate malfunctions to a specific operational area or system component.

Computer Service Manual: This manual describes the operational components located in the computer assembly, including memory unit, power circuits, and signal circuits. It also provides maintenance instructions and adjustments for computer components, and gives a detailed set of test procedures for computer circuit boards using the component tester.

Input-Output Service Manual: This manual describes the operational characteristics of RECOMP II input-output equipment (control console, typewriter, tape reader, and tape punch). It also provides maintenance and test instructions for these input-output devices and the associated desk assembly.

Test Equipment Service Manual: This manual describes the functional characteristics of the system tester and component tester. It also provides maintenance and test instructions for these two RECOMP II test equipments.

System Reference Schematics: This publication provides a set of schematics, assembly drawings, wiring charts, and signal charts for each system component; i.e., computer, desk, control console, tape reader, typewriter, and tape punch.

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ILLUSTRATIONS

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INTRODUCTION

GENERAL

This manual provides a description of the operational components located in the computer assembly, including memory, power circuits, and signal circuits. It also provides maintenance and repair instructions for these components, including detailed test procedures for the etched circuit boards using the component tester. In most cases, the functional tests described in the RECOMP II System Service Manual must be performed before the instructions contained in this manual are used.

OPERATIONAL CHARACTERISTICS

The RECOMP II computer (figures 2 and 3) is a general purpose digital computer that utilizes the binary number system for all internal operations. The input equipment used to address the computer consists of: photoelectric paper-tape reader, electric typewriter, and control panel keyboard. Output equipment includes visual readout via the control panel, typewriter, and teletype-coded paper-tape punch.

The computer memory is a rotating magnetic disk. It has a capacity of 4080 nonvolatile words plus two 8-word, rapid access loops. Nonvolatile refers to the fact that even during power interruptions the disk retains the recorded information. Also on the disk memory unit are the permanently recorded timing tracks (clock and origin), and five 1-word arithmetic registers.

A RECOMP word consists of 41 binary digits. One digit is used for a synchronizing bit and is not available for programming. A word can either be a number (sign plus 39 significant digits) or a command. (In actual operation, there will be 2 commands to 1 word.)

There are five basic types of commands in RECOMP II: arithmetic, transfer (conditional or unconditional), store, interchange, and input or output.

ACCESS TIME

Access time for main information channels is 0.52 millisecond minimum and 16.9 milliseconds maximum. Access time for the high-speed loops is 0.95 millisecond maximum for reading and 2.34 milliseconds maximum for writing.

OPERATION TIME

Operation time (excluding access time) for addition or subtraction is 0.52 millisecond. Multiplication and division require 10.4 milliseconds (excluding access time.) Transfer control requires 0.78 millisecond.

POWER REQUIREMENTS

The power requirements for the computer are 115 volts, 60 cps, single-phase at 400 watts (excluding input/output equipment.)

PHYSICAL CHARACTERISTICS

Size: 23 inches wide, 21 inches long, and 16.5 inches high (excludes input/output equipment)

Weight: 196 pounds (excludes input/output equipment)

Structure: Welded aluminum (steel in later models)

Finish: White, cocoa brown, madrone, and pale straw gold enamel (or anodize)

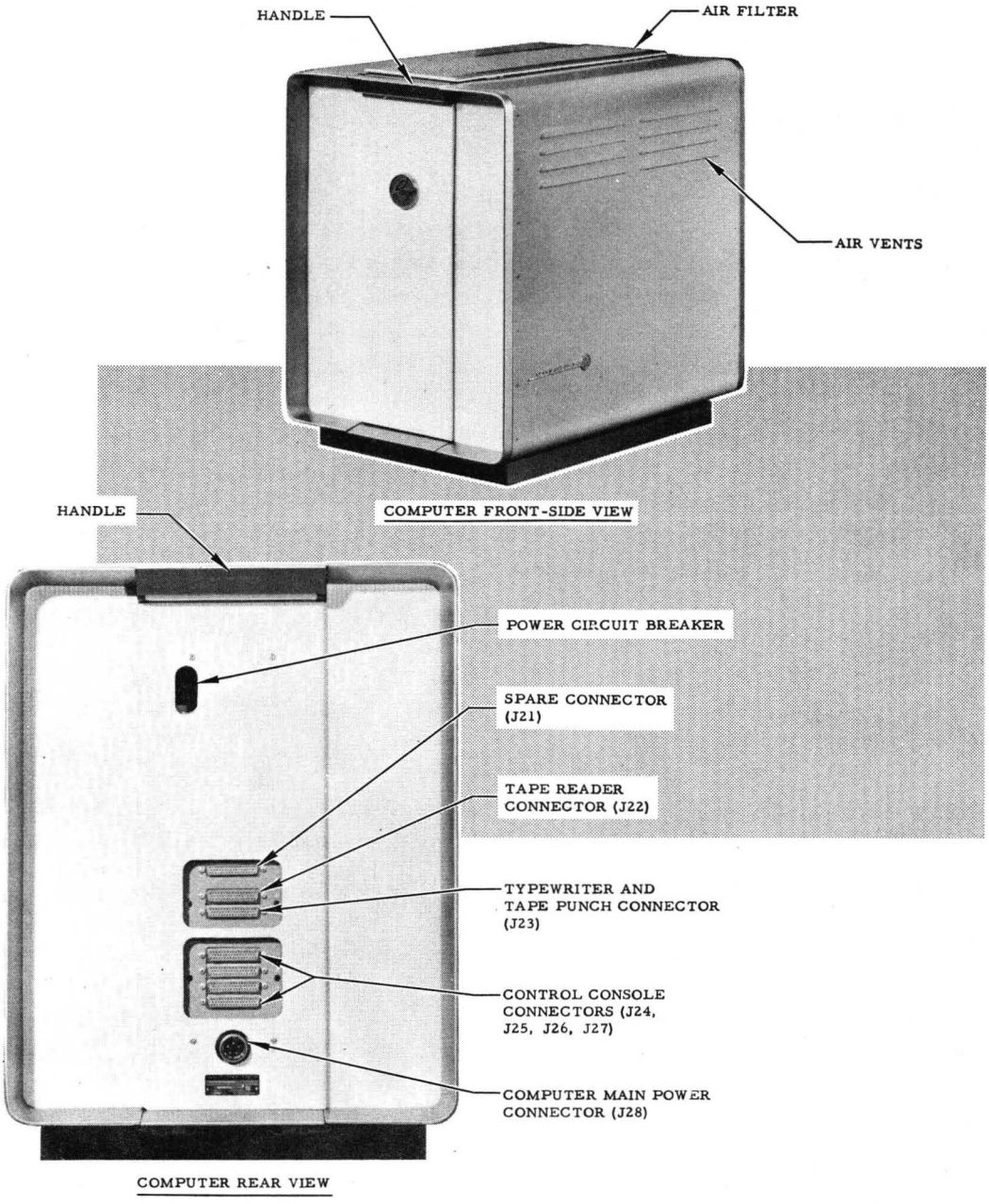


Figure 2. Computer Assembly - Exterior Views

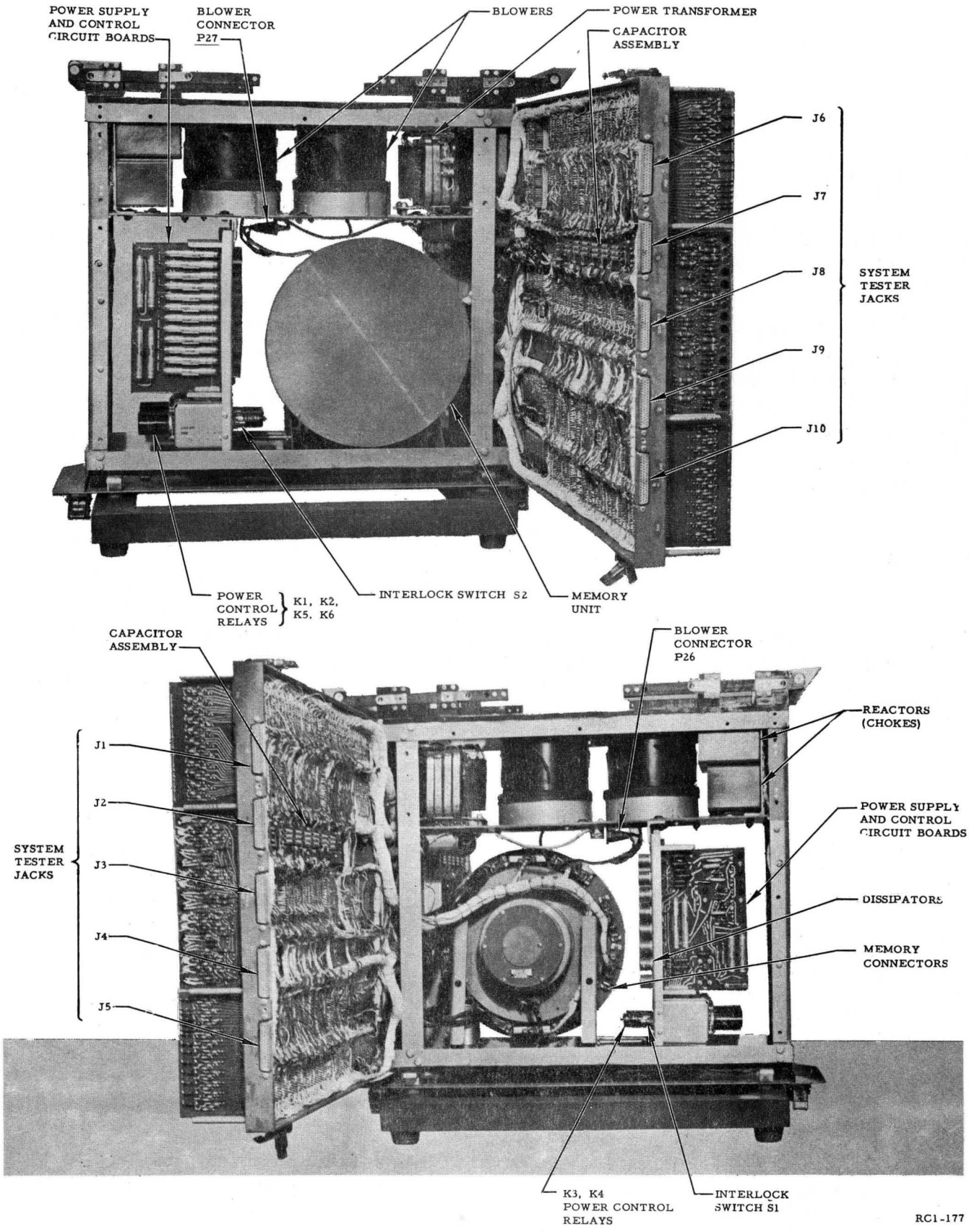


Figure 3. Computer Assembly - Interior Views

FUNCTIONAL DESCRIPTION

GENERAL

This section describes mechanical and electrical functional characteristics of operational components located in the computer assembly.

The computer central framework houses a magnetic disk memory, secondary power supplies, and two blowers. Hinged to both sides of the central framework are castings that form the sides of the computer, and mounted on the outside of these castings are all etched circuit boards except power supply circuit boards. The inside of each casting supports the interconnecting wiring for the circuit boards. Receptacles for the system tester connectors mounted on the unhinged ends of each casting.

MEMORY

The RECOMP II memory consists basically of a magnetic disk rotating past fixed read and write heads. Information is stored on the disk in the form of flux patterns representing binary digits. When the disk is rotating, an air bearing provides an air gap of approximately 50 microinches between the recording surface of the disk and the read and write heads.

MECHANICAL OPERATION

Principal parts of the memory assembly are illustrated in figure 4. A flexible diaphragm attaches the disk to the rotor. The rotor is mounted to a nonrotating shaft with ball bearings held in place by snap rings. The shaft is supported by 2 parallel diaphragms, 1 located in the inner edge of the headplate and 1 in the lower part of the frame. The solenoid coil is contained in a housing fixed to the frame. The solenoid plate (armature) is mounted to the lower end of the shaft. The shaft is spring-loaded between the solenoid plate and solenoid housing collar. Until power is applied to the solenoid, the shaft is held at its lowest extremity by the spring. Information can neither be written on nor read from the disk because of the separation between disk and headplate when the shaft is in this position. The shaft is held at its lowest extremity while the disk motor is run up to speed. The motor is a split-phase induction-type incorporating a capacitance start with an operating speed of 3450 revolutions per minute. When the motor and disk reach operating speed, the solenoid is energized and forces the shaft toward the headplate against the preloaded spring.

Because the shaft, rotor, and disk move as a single body, the disk is forced near the headplate (approximately 50 microinches). Information can now be stored and extracted.

In operating position, an air thrust bearing maintains the spacing between the rotating disk and the headplate. The air bearing consists of eight grooved radial sections, the configurations of which are 45 degrees each (8 x 45 = 360 degrees) in width around the circular surface of the headplate (figure 5). As the disk rotates, air moves in the direction from A to B, expanding in the grooved sections and compressing in the flat sections. Any tendency of the disk to touch the headplate is offset by the pressure of the air at compression points.

READ AND WRITE HEADS

Magnetic read and write heads are used for recording information on and reproducing information from the magnetic disk. They are mounted in slots in

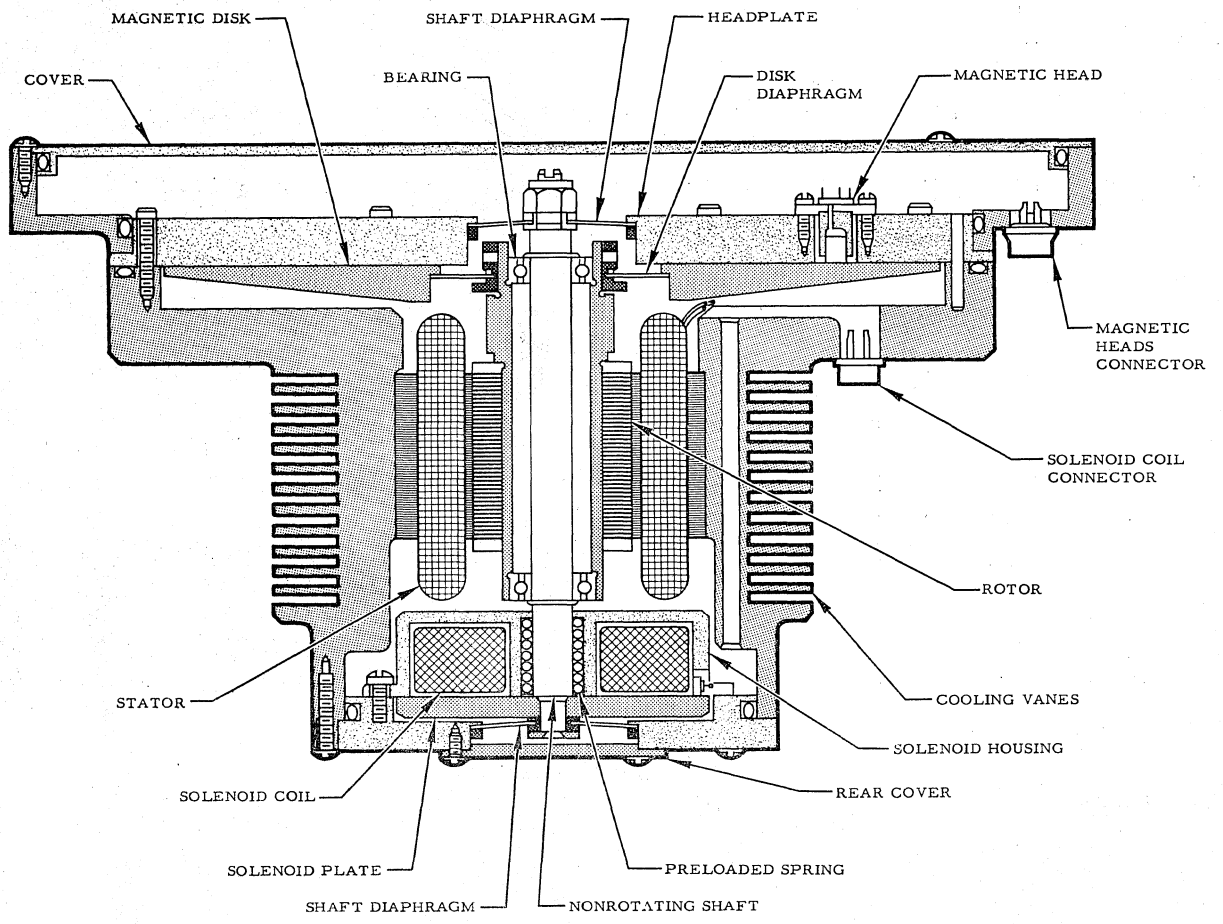
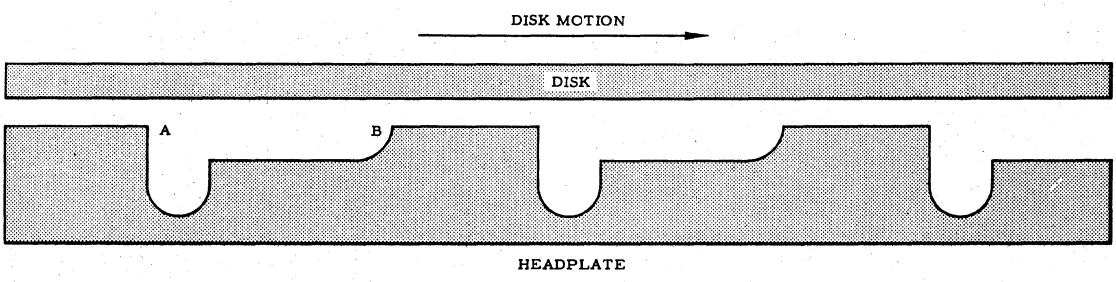


Figure 4. Cross-Sectional Diagram of Magnetic Memory



RCL-153

Figure 5. Air Thrust Bearing Diagram

the headplate. The write head (figure 6) consists of (1) a centertapped coil of copper wire, (2) a metal core formed of thin, high-permeability T-laminations, (3) two fairly high permeability, low-loss magnetic blocks, and (4) ceramic inserts. The pole tip which consists of the edges of the laminations provides the writing area.

Information is written on the disk "perpendicularly," as diagrammed in figure 7. When the coil is energized, flux concentrates at the end of the pole tip and enters the iron oxide recording material. Because this material is of

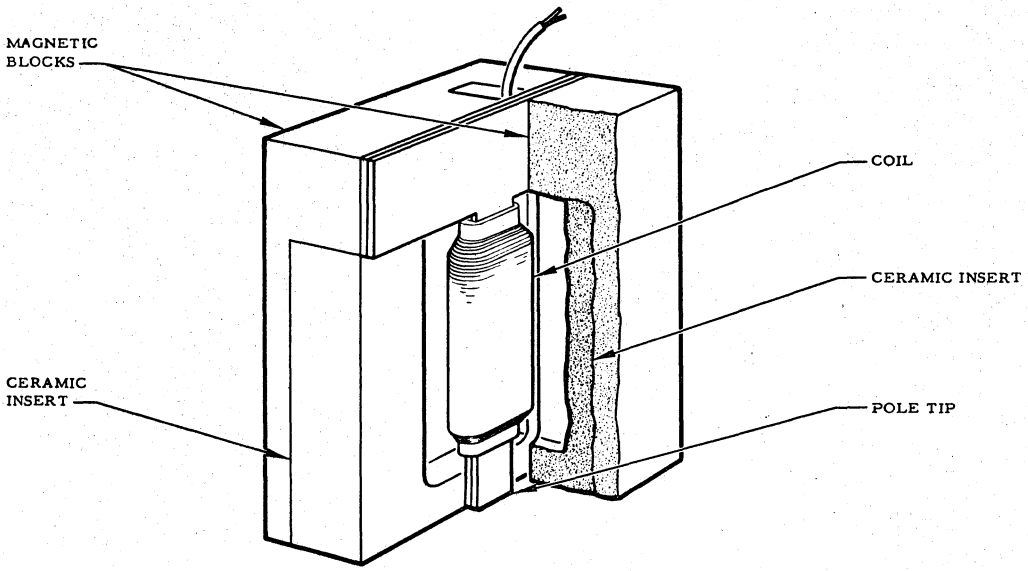


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Figure 6. Write Head Construction

low permeability as compared to that of the backing material, the flux does not spread out. It flows downward, setting up vertical magnets in the iron oxide, and then enters the high-permeability backing material. Here it spreads out, then reenters the recording medium. Completion of the flux path takes place through the magnetic blocks and back to the center leg of the T-laminations. The demagnetizing effect of the return flux on the magnets already produced is very slight because the return flux is highly diffused.

Current through the write head is in the form of square wave pulses flowing through one-half of the coil toward the center tap for a binary-1 signal and through the other half toward the center tap for a binary-0 signal. This type of recording is termed "nonreturn to zero" because the recording current is either at a negative or positive level but never at zero level. The flux pattern induced in the recording medium is shown in figure 10. Positive square wave inducing pulses are magnetized as square waves with rounded corners, that is, lesser intensity at the leading and trailing edges.

The read head (figure 8) consists of (1) a single-ended coil, (2) a metal core formed of T-laminations, and (3) two fairly high-permeability, low-loss magnetic blocks shaped to form a shielding extension near the pole tip. In reading, the read head senses only the changes in the magnetized state of the recording material. Essentially triangular voltage pulses result

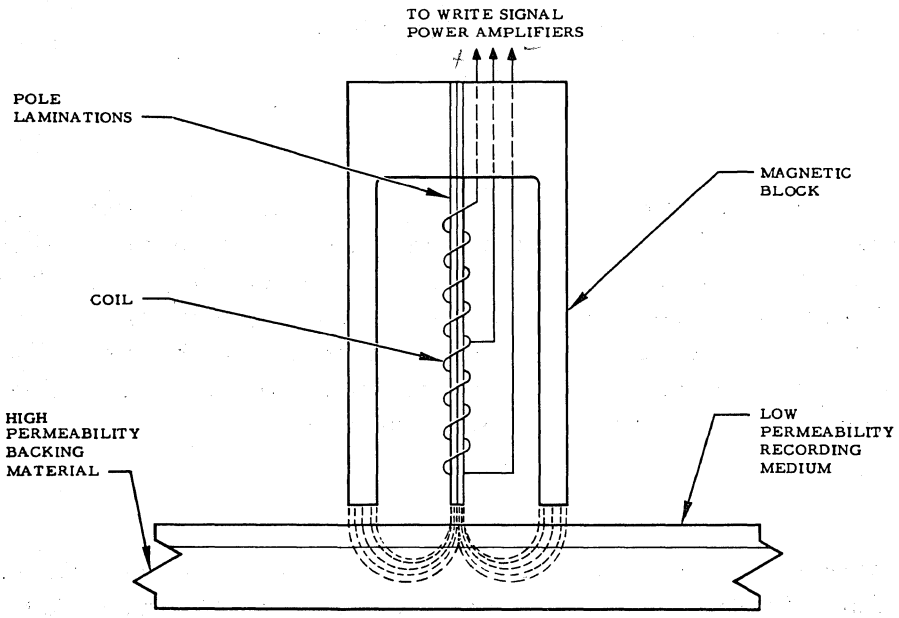

Figure 7. Flux Diagram of Perpendicular Recording

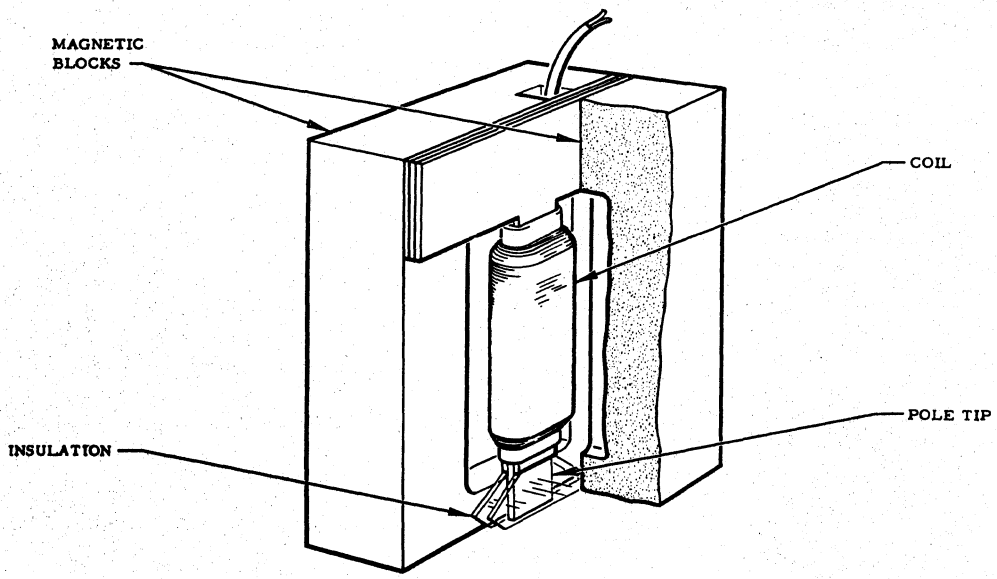

Figure 8. Read Head Construction Diagram

from the reading, a positive pulse representing a change from binary 0 to binary 1 and a negative pulse representing a change from binary 1 to binary 0. For a succession of similar binary digits, the first digit is reproduced as a pulse and succeeding digits have a 0-volt level. The magnetic block extensions at the base shield the coil from adjacent recorded digits, thereby permitting only one digit pattern at a time to be read. (See figures 9 and 10.)

ERASE HEADS

The erase heads are similar to the read and write heads in physical dimensions and appearance. The difference is that the erase heads have a permanent-magnet wire along the center instead of a T-type pole piece with coil. The magnet wire is now the central pole piece. Magnetic lines issuing from this pole piece return through the magnetic blocks, as for the read and write heads. The strength and polarity of this magnetic field is such that all changes of flux are removed from the disk as it passes under the erase heads.

CHANNELS

The memory disk is divided into channels which consist of concentric tracks 0.025 inch wide and separated from each other by 0.015 inch. The channels are utilized as follows:

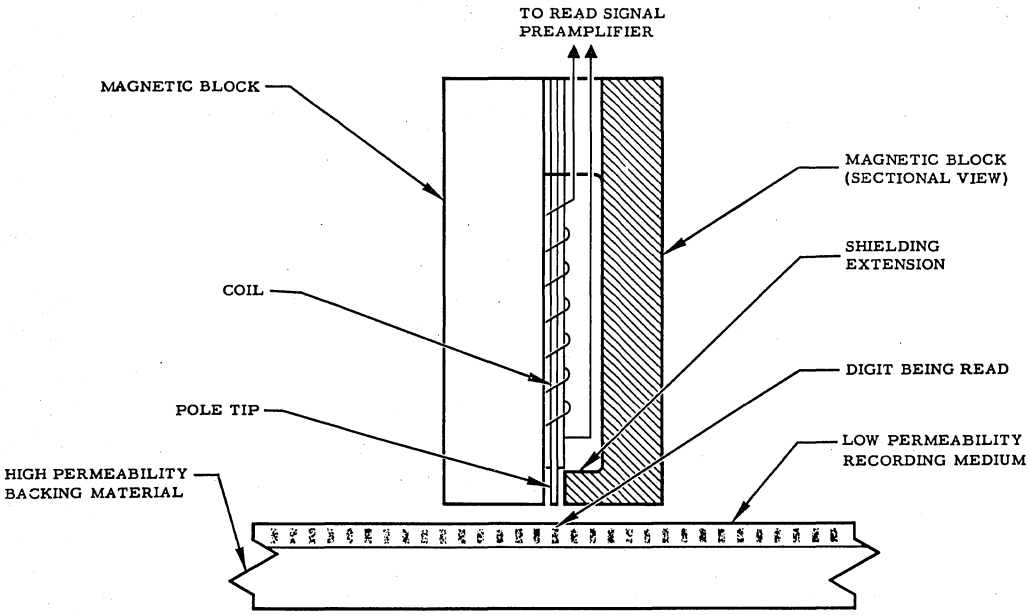

Figure 9. Reading of Perpendicularly Recorded Digits

1. Sixty-four permanent-storage information channels, which store 64 words per channel. (The channels are identified by read heads numbered octally M_0 through M_{77} and corresponding write heads numbered octally W_0 through W_{77}. Channel 77 contains only 48 addressable word spaces because the last 16 addresses are assigned to the rapid-access loops L and V, loop L having the addresses 7760 to 7767, and loop V having the addresses 7770 to 7777.

2. One clock channel (C) which contains permanently recorded sine waves (figure 11) for synchronization of computer circuits.

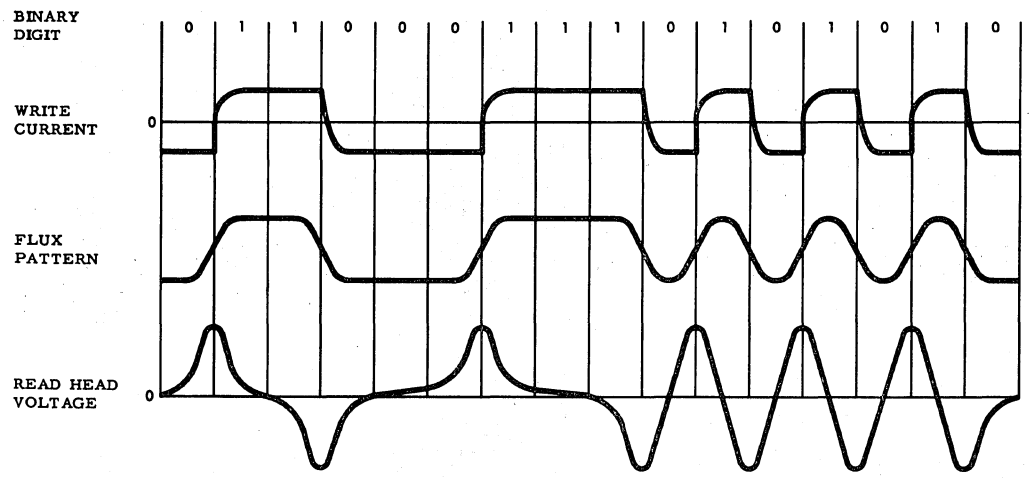

Figure 10. Waveforms in Writing and Reading

3. One origin channel X_{or} which contains a permanently recorded pulse for initial synchronization of computer circuits and for resetting the digit counter.

In addition, one channel provides storage space for the following loops and registers:

1. Four recirculating 1-word arithmetic registers (accumulator A, number register B, remainder register R, and auxiliary register X).
2. One recirculating 1-word control register (command register Z).
3. Two high-speed 8-word recirculating loops (L and V), which can copy and store any 8 consecutive words from any of the 64 information storage channels. An additional read head is located four words from the write head on channels L and V. This head provides access to information stored between the read and write heads on the 8-word loops, thereby reducing the access time for readout.

Each channel, register, and loop has a read head and write head. (See figure 12.) The read heads are separated from the write heads by 180 degrees for the information channels, clock channel, and origin channel. On the outermost channel, the read and write heads are spaced approximately 1-word length for the 1-word A, B, R, X, and Z registers. The read and write heads are spaced at 8-word lengths for the L and V loops with an additional read head spaced at 4-word lengths. A permanent magnet erase head on the outermost channel, which contains the recirculating registers and loops, separates the end of each register or loop from the start of the next. By this location of the erase head, information read from one register is erased before the same area of the disk passes under the write head of the next register.

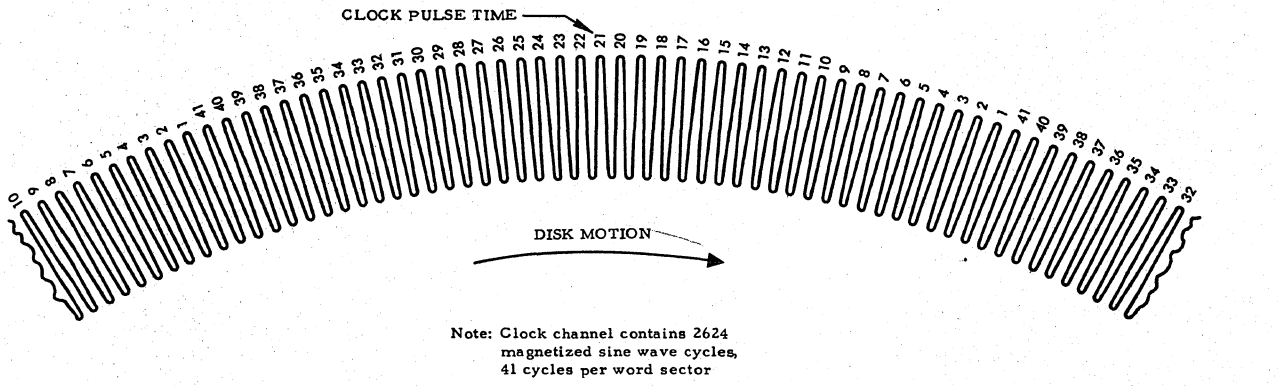

Figure 11. Permanently Recorded Clock Track Waveform

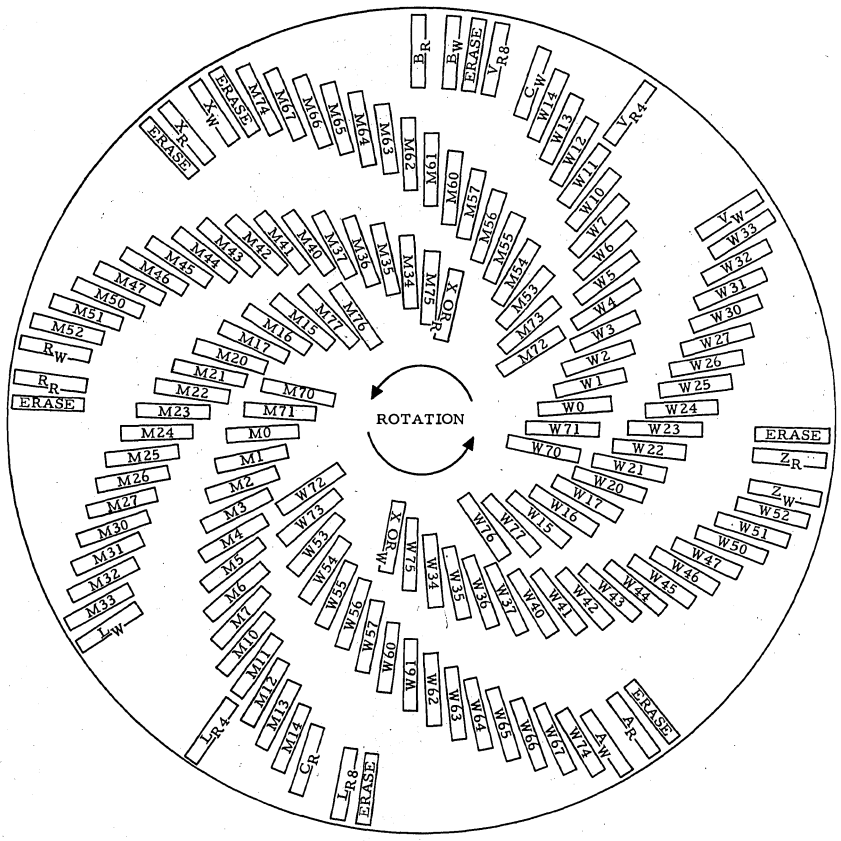

Figure 12. Head Positions on Magnetic Disk (Systems 501 through 520)

The placement of the heads illustrated in figure 12 is applicable only to the memories originally installed in systems 501 through 520. Figure 13 shows the headplate design for systems subsequent to 520, wherein the channels are "pushed out" to provide for a greater diameter, and thus a greater circumference, for the inner tracks.

This greater circumference reduces the possibility of the origin pulse being too wide in terms of duration and also reduces the possibility of amplitude modulation occuring on information stored in the inner channels. Principles of operation, however, are the same as previously described in this section, and all connection details and logic details are the same for both headplate configurations.

Memories with this "push out" design may eventually replace those now installed if replacement is warranted under normal operating conditions.

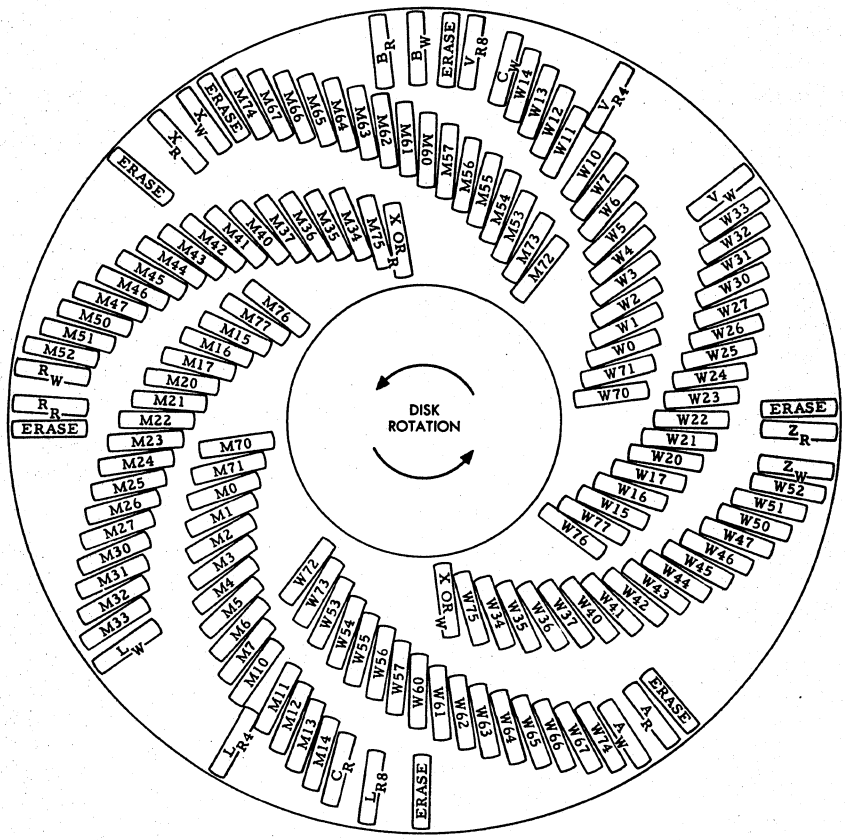

Figure 13. Head Positions on Magnetic Disk (Systems 521 and Subsequent)

POWER CIRCUITS

Primary power for the computer is supplied from a single-phase, 60-cycle, 115-volt, 2-wire system. Connector J28 is the primary power connector to the computer assembly. Within the computer, power control circuitry of the power supply assembly distributes power to the memory, blowers, and secondary power supplies. Initial timing of the computer power distribution is very important to the initial synchronization of logic circuits and to the starting of the memory.

SUMMARY OF POWER CONTROL OPERATIONS

When power is turned on by an operator at the computer control console, the following actions take place:

Power is applied through circuit breaker CB1 and CB2 to the control console and to the memory.

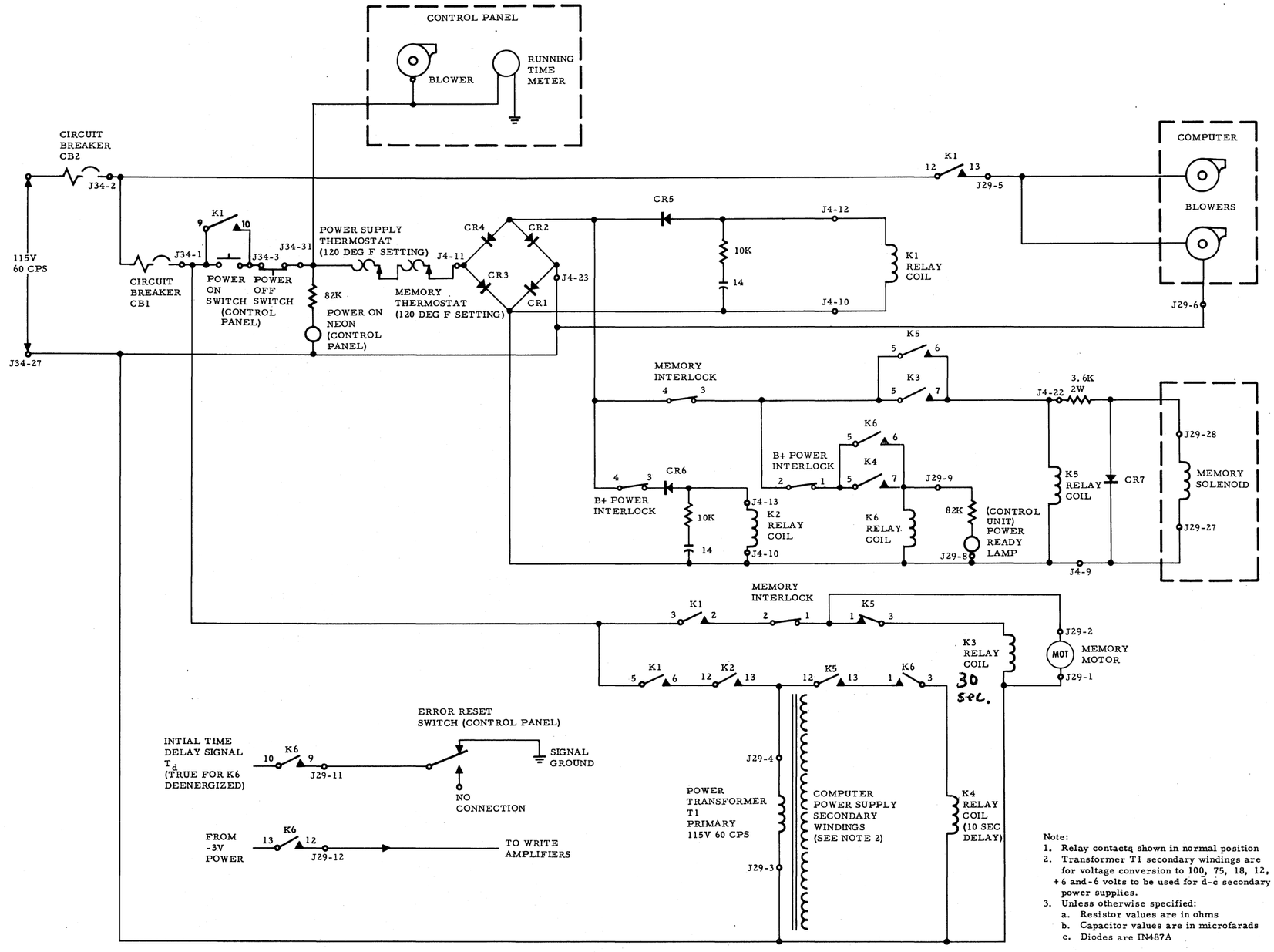

Figure 14. Simplified Power Control Schematic

Power is applied through circuit breaker CB2 to the blowers. If an overload occurs on either circuit breaker, the entire computer is deenergized.

As the memory motor starts to rotate, the memory solenoid remains deenergized for a time delay of approximately 30 seconds.

When the solenoid is energized, the disk is positioned so that the computer can start receiving clock signals. The clock signals, in conjunction with a signal (T_d) generated in the power control circuitry, zero and initialize all computer signal circuitry. T_d is on for approximately 10 seconds; the computer is then initialized and ready for operation.

DETAILED DESCRIPTION OF POWER CONTROL OPERATIONS

In reading the following description, refer to the simplified schematic of figure 14 and the block diagram of figure 15.

With circuit breakers CB1 and CB2 closed and the POWER ON switch depressed, a-c power is applied to the POWER ON indicator, blower, and running-time meter in the control console, and to the full-wave bridge rectifier. The bridge supplies d-c power which energizes relays K1 and K2. Closing of relays K1 and K2 contacts applies a-c power (1) to the computer blowers, (2) to the power transformer, (3) to the memory motor, and (4) to delay relay K3. Relay K3 has a 30-second energizing time. The power supplies and all circuits deriving power from them are energized, with the exception of the main memory write switches. These switches are inhibited by relay K6 contacts 13 and 12 in open position. In addition, the computer cannot be operated because of an initial synchronization delay signal T_d generated as a result of relay K6 contacts 10 and 9 in open position.

Thirty seconds after power application to relay K3, it is fully energized. Closing of relay K3 contacts allows the memory solenoid and relay K5 to be energized. Solenoid action positions the memory disk, thereby permitting clock signals to be generated for zeroing of computer circuits. Solenoid and relay K5 current is distributed through a memory thermostat and a power supply thermostat, both of which are set to open at 120°F and to reclose at 105°F. The memory thermostat is mounted to the memory housing, and the power supply thermostat is mounted on the etched circuit board of the -18-volt power supply.

Closing of relay K5 contacts 5 and 6 provides a holding circuit for the memory solenoid when the normally closed relay K5 contacts 1 and 3 open.

Closing of relay K5 contacts 12 and 13 permits power to be applied to relay K4. This relay has an energizing time of 10 seconds. Zeroing of computer circuitry continues for 10 seconds, at the end of which time relay K4 is energized. Closing of relay K4 contacts energizes relay K6 and causes the POWER READY indicator to glow. This signifies that the computer is ready for operation,

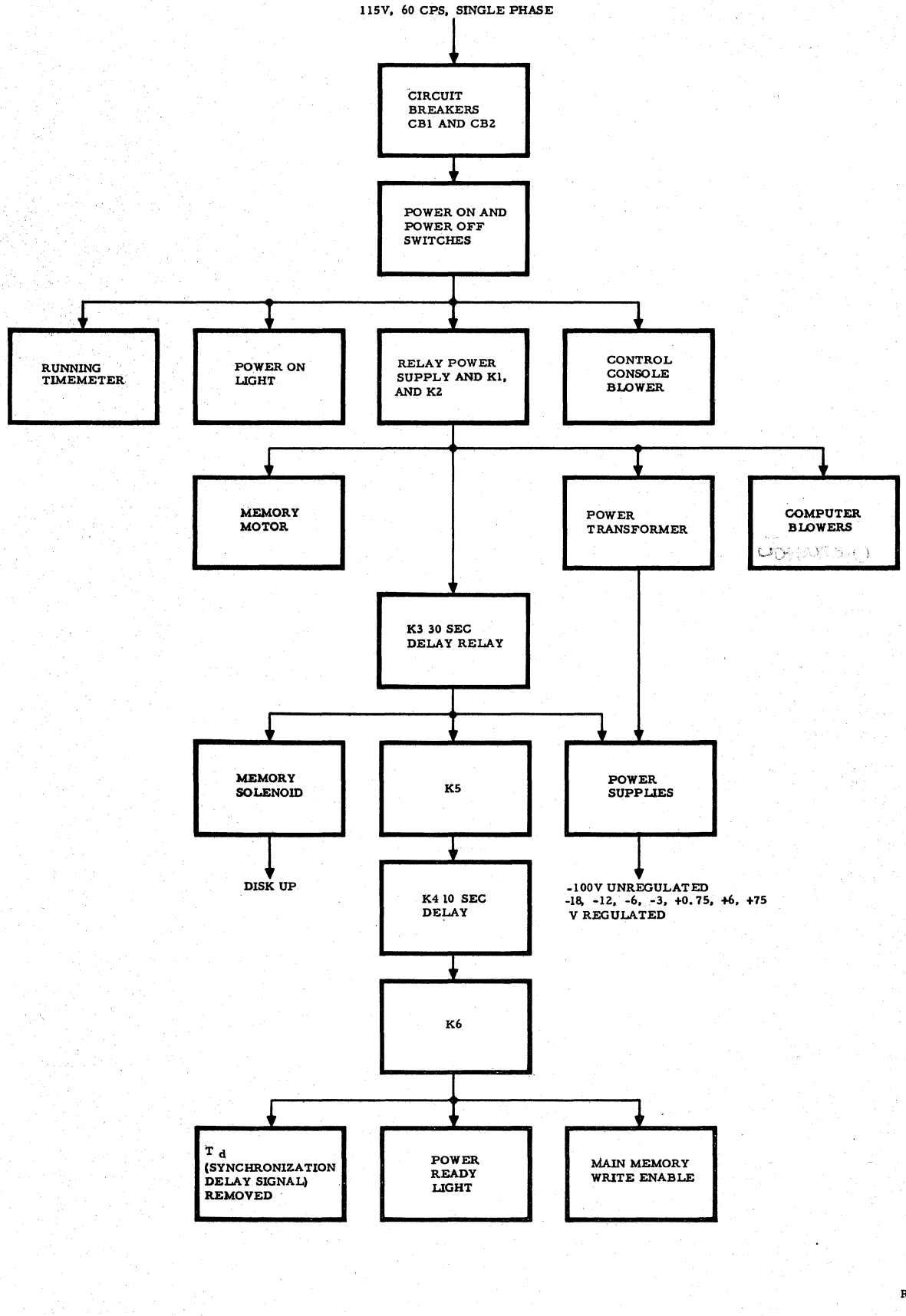

Figure 15. Power Control Circuits Block Diagram

because (1) closing of relay K6 contacts 13 and 12 has applied power to the main memory write selection circuits and (2) closing of relay K6 contacts 10 and 9 has removed the initial synchronization delay signal.

Power is removed from the computer by depressing the POWER OFF button. The memory solenoid is first deactivated, thereby moving the memory disk away from the headplate. To prevent transients from being written on the disk at this time, power is maintained to the computer secondary power supplies for approximately 0.5 second by the r-c networks across relays K1 and K2.

SECONDARY POWER SUPPLIES

D-c voltages required for operation of the computer and control console are supplied by secondary power supplies mounted on six etched circuit boards which plug into receptacles on the power supply chassis: the +6-, -6-, and +0.75-volt board in J1; the -12- and +75-volt board in J2; the -18-, -100-, and -3-volt board in J3; the relay control network board in J4; the network board in J5; and the filter board in J6. A retaining screw at the top of each board and through the power chassis provides additional support.

The power supply assembly further consists of a power transformer, filter chokes, power control relays, and other control elements.

-100-Volt Power Supply

Unregulated -100-volt power is supplied to the decade driver and neon driver circuits of the control console. In addition, the -100-volt supply provides a reference voltage for the other power supplies. The -100-volt power supply (figure 16) consists of a conventional single-phase, full-wave, bridge-type, diode rectifier with r-c filters. A fuse in series with the load protects the power supply on overloads.

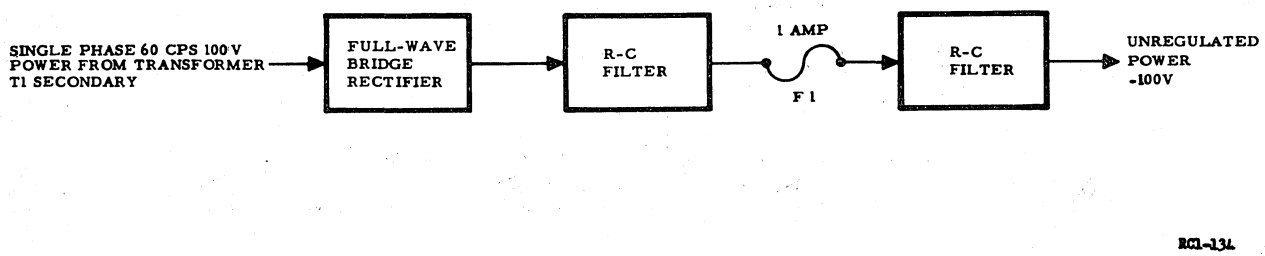

Figure 16. -100-Volt Power Supply Block Diagram

-18-Volt Power Supply

Power at -18 volts with regulation of 3 percent is supplied to all logic gates in the computer. (See Figure 17.)

The power supply comprises a single-phase, full-wave, bridge-type diode rectifier with filter, and a series regulating circuit. The regulator consists of (1) power amplifier stage, (2) driver amplifier, (3) differential amplifier, (4) current limiter, and (5) undervoltage kickout stage.

The differential amplifier senses the difference between a reference voltage and the -18-volt output voltage and applies this difference to the driver amplifier. The driver controls the current to the power amplifier and, therefore, the output or load current. If the -18-volt output tends to increase (negative change), power amplifier current is reduced which causes a reduction in output voltage. A positive-going output change is accompanied by an increase in power amplifier current which, in turn, causes an increase of output voltage.

The current limiter operates when the load exceeds about 30 percent of full load. Normally cut off, the current limiter conducts when the overload occurs and shorts out some of the power amplifier base current drive. The undervoltage kickout circuit then comes into play. This circuit operates when the -18-volt output falls to -15 volts or lower. Normally cut off, the voltage limiter conducts when the undervoltage point is reached and shorts out the power amplifier drive. Load current is completely eliminated and the computer circuits remain inoperative until the overload is removed, and the computer is turned off, then on.

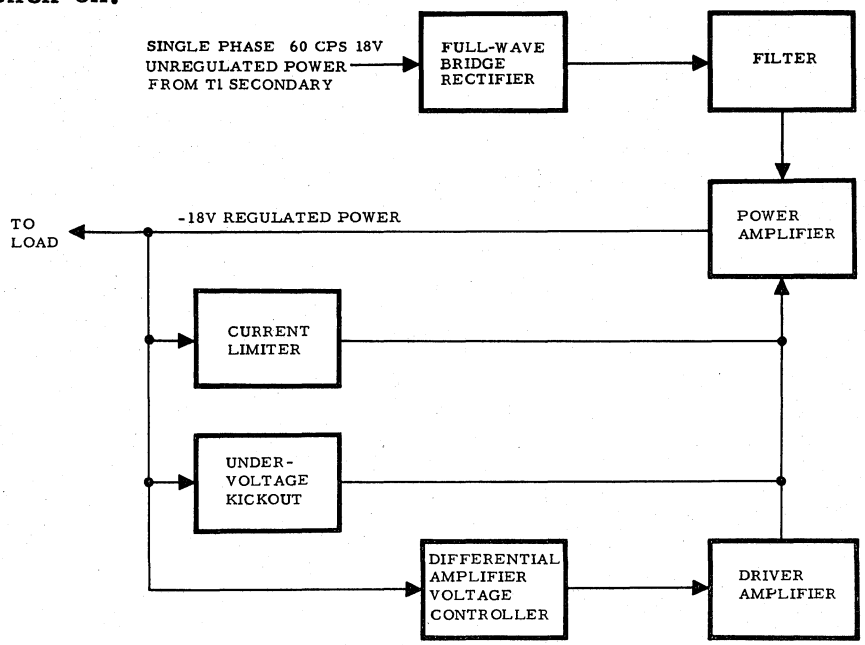

Figure 17. -18-Volt Power Supply Block Diagram

-12-Volt Power Supply

Power at -12 volts with regulation of 3 percent is supplied to the logic flip-flops, read amplifier, and clock circuits. (See figure 18.) The power supply comprises a single-phase, full-wave, bridge-type diode rectifier with filter, and a series regulating circuit. The regulator consists of (1) series power amplifier stage which carries the load current, (2) driver amplifier which amplifies a control signal to control power amplifier current, (3) differential amplifier which senses the differences between a reference voltage and the -12-volt output, (4) current limiter, and (5) undervoltage kickout. Circuit operation is identical to that of the -18-volt power supply.

-6-Volt Power Supply

Power at -6 volts with regulation of 3 percent is supplied to the logic flip-flops and the read amplifiers. The -6-volt power supply comprises a single-phase, full-wave, bridge-type diode rectifier with filter, and a series regulating circuit. (See figure 19.) The regulator consists of (1) power amplifier stage which carries the load current, (2) driver amplifier which amplifies a control signal to control power amplifier current, (3) differential amplifier which senses the difference between a reference voltage and the -6-volt output, (4) current limiter, and (5) undervoltage kickout. Operation of this circuit is identical to that of the -18-volt power supply with the exception that one less power amplifier transistor is used.

-3-Volt Power Supply

Power at -3 volts is supplied to the emitters of the 64 information channel write switches. Current flows only when a load exists; that is, when one of the

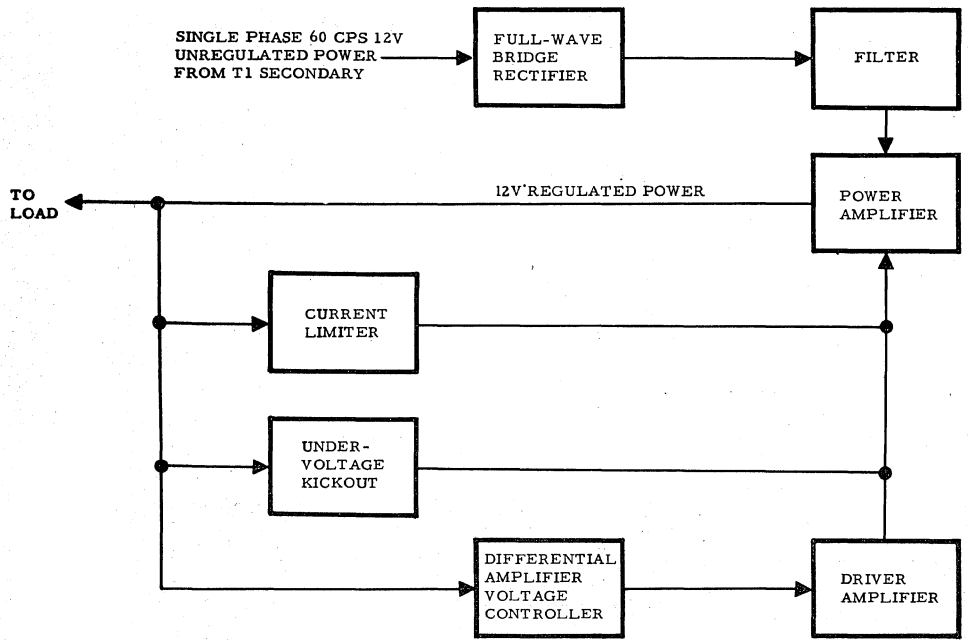

Figure 18. -12-Volt Power Supply Block Diagram

write switches closes the write head circuits. The -3-volt supply consists of 3 identical diodes, series-connected from power ground to the emitters of the write switch transistors. (See figure A-34.) Each diode has a nominal 1-volt drop under load.

+75-Volt Power Supply

Power at +75 volts with regulation of 3 percent is supplied to the neon driver and decimal display tube circuits. The power supply comprises a single-phase, full-wave, bridge-type diode rectifier with filter, and a series regulating circuit. (See figure 20.) The regulator consists of (1) power amplifier stage which carries the load current, (2) driver amplifier which amplifies a control signal to control power amplifier current, (3) differential amplifier which senses the difference between a reference voltage and the +75-volt output, and (4) current limiter. This circuit operates identically to that of the -18-volt power supply with the following exceptions: (1) only one power amplifier transistor is used and (2) the voltage kickout stage is eliminated.

+6-Volt Power Supply

Power at +6 volts with regulation of 3 percent is used mainly in the logic flip-flops. The power supply comprises a single-phase, full-wave, bridge-type diode rectifier with filter, and a series regulating circuit. (See figure 21.) The regulator consists of (1) power amplifier stage which carries the load current, (2) driver amplifier which amplifies a control signal to control power amplifier current, (3) differential amplifier which senses the difference between a reference voltage and the -12-volt output, and (4) current limiter.

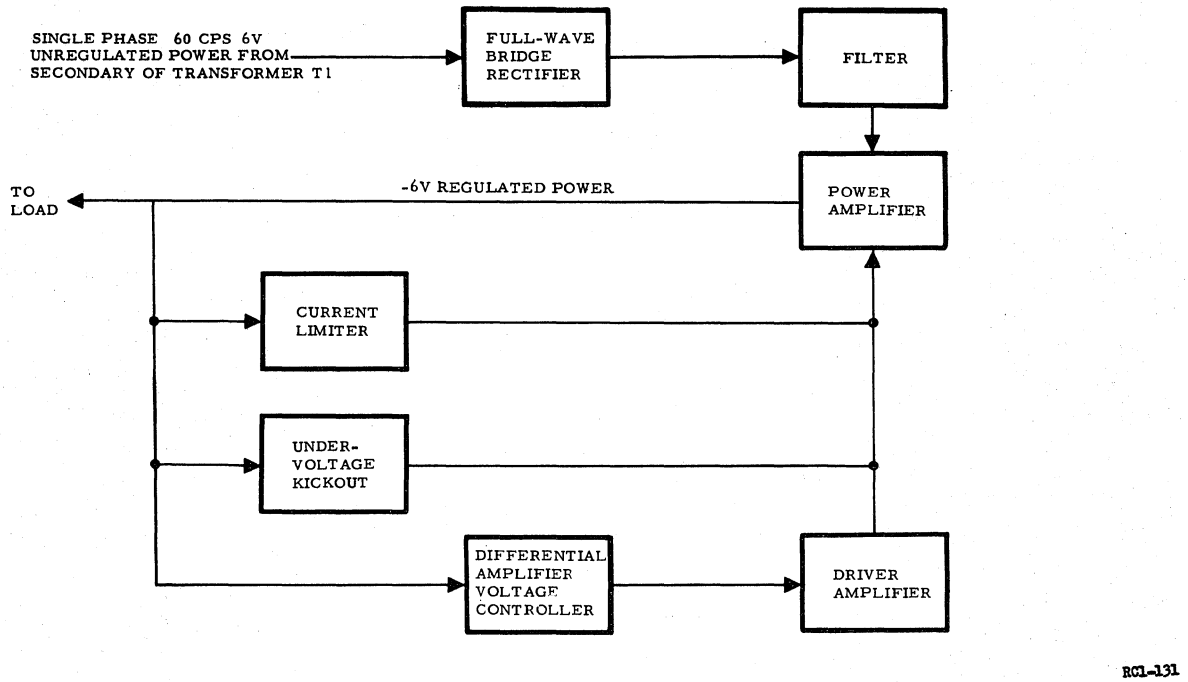

Figure 19. -6-Volt Power Supply Block Diagram

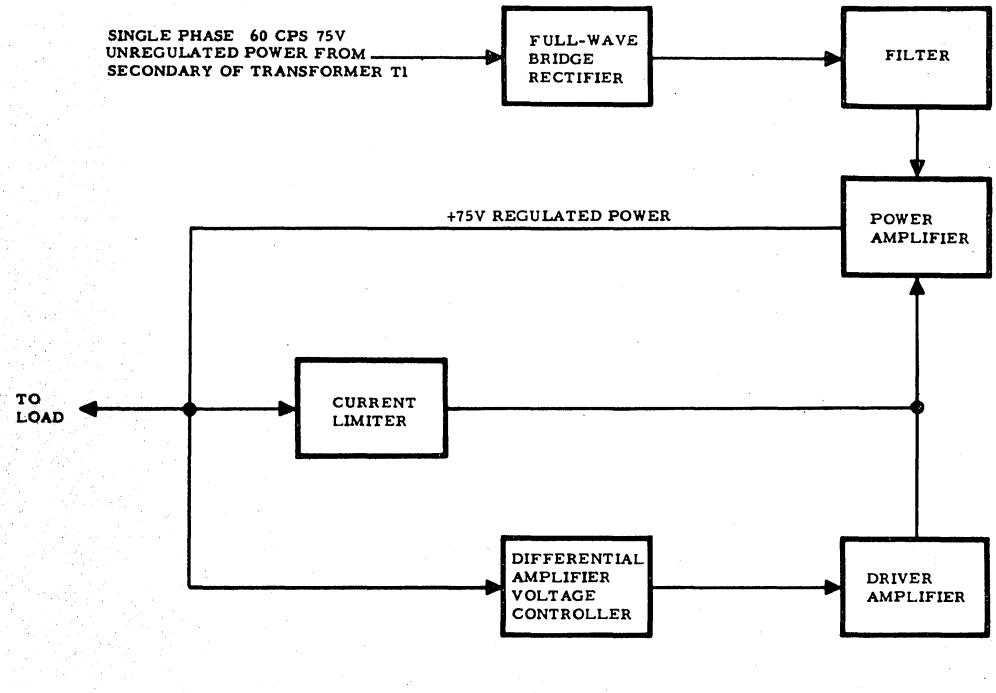

Figure 20. 75-Volt Power Supply Block Diagram

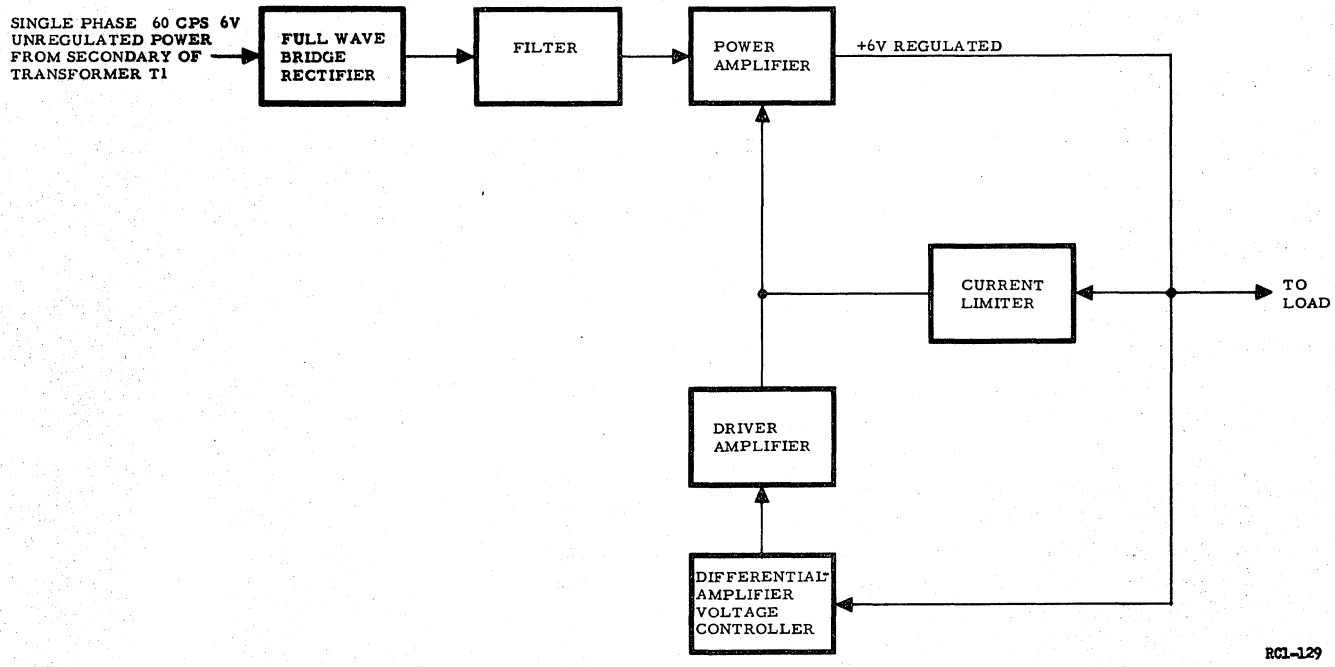

Figure 21. 6-Volt Power Supply Block Diagram

Circuit operation is identical to that of the -18-volt supply with the following exceptions: (1) only three power amplifier transistors are used and (2) the voltage kickout stage is eliminated.

+0.75-Volt Power Supply

Power at 0.75 volt with regulation of 5 percent is derived from 6-volt regulated power and supplied as bias cutoff to the driver stage of the read switching network. The circuit consists essentially of a power amplifier and a voltage control amplifier. (See figure 22.) The power amplifier carries the majority of load current. The voltage amplifier amplifies any change of output voltage appearing across the output resistance. Any voltage increase as sensed by the voltage amplifier effects a decrease in the voltage output of the power amplifier.

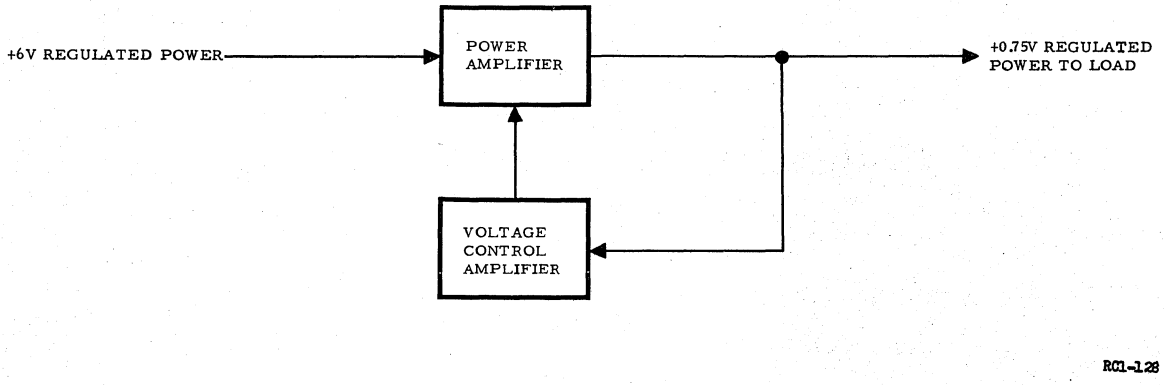

Figure 22. 0.75-Volt Power Supply Block Diagram

SIGNAL CIRCUITS

All operational electronic circuitry is mounted on plug-in circuit boards. Each circuit board is of a particular "building-block" type to allow interchangeability among boards of a single type and to allow a modular-replacement form of maintenance when a particular circuit fails to function.

The plug-in circuit boards are supported in their connectors by color-coded mounting posts as illustrated in figures 23 and 24. The types and numbers of plug-in signal circuit boards mounted in the computer assembly are as follows:

Clock power amplifier No. 1	1
Clock power amplifier No. 2	1
Logic (gates)	108
Flip-flop (four per board)	42
Write amplifier	3
Write switch	8
Read amplifier	19
Read switch	8
Network	6

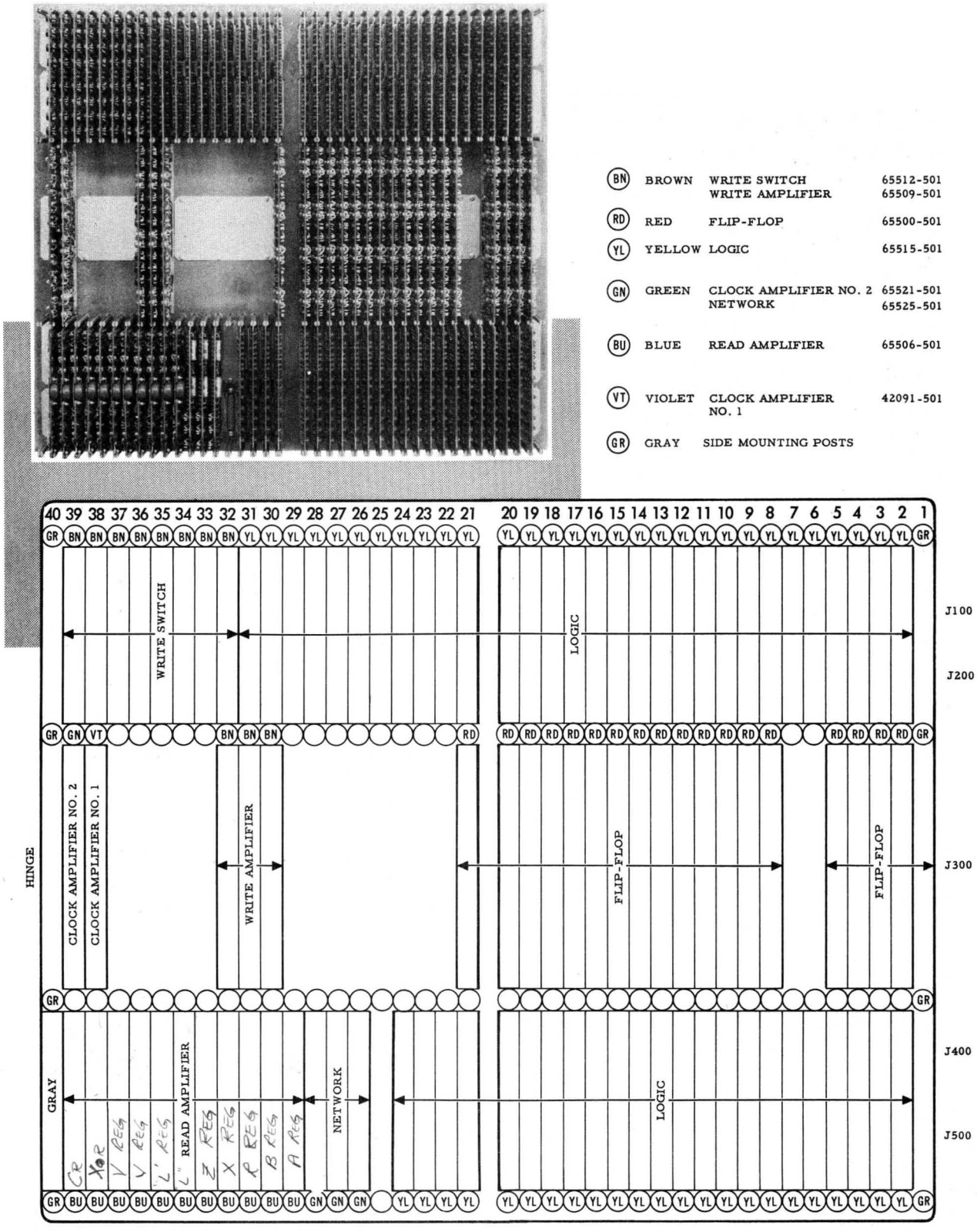

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Figure 23. Location and Color Coding of Computer Etched Boards, Panel Assembly No. 1

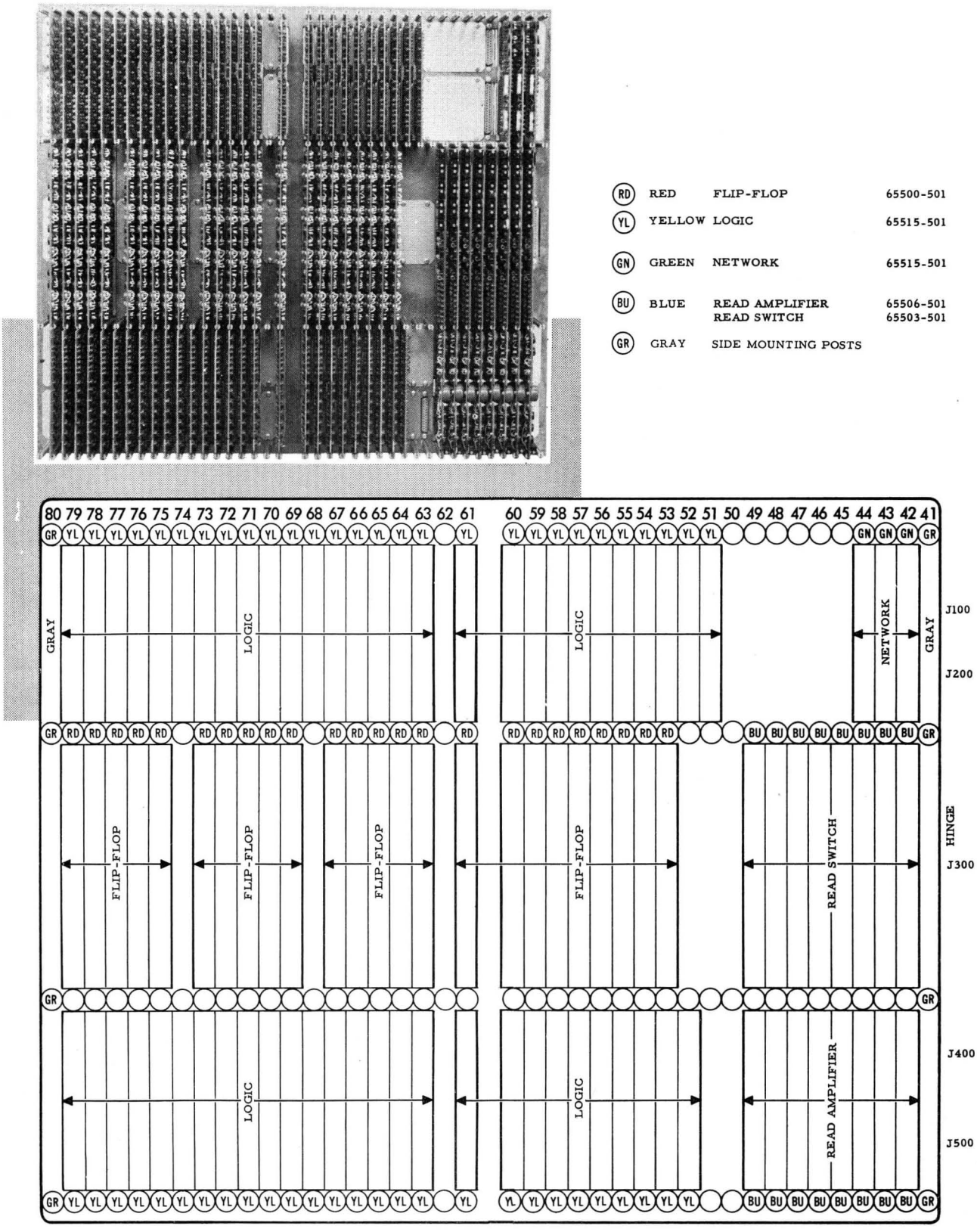

Figure 24. Location and Color Coding of Etched Boards Panel Assembly No. 2

The following circuit descriptions are written in terms of general functional stages that make up each circuit board and do not require reference to the detailed schematics. However, the descriptions are complete enough that the reader can gain a relatively complete knowledge of each circuit by tracing signals on the appropriate schematic (See Pub. 508-T-11) as he reads the the general descriptions of this section.

CLOCK POWER AMPLIFIERS

In RECOMP II, a clock signal synchronizes all computer operations by triggering the logic circuitry at a constant frequency, 153 kilocycles per second (nominal). Because the source of the clock signal is a permanently recorded sine wave on the memory disk, it is assured that all logic operations are synchronized with information transfers to and from memory as well as with each other. The clock signal consists of a squared voltage wave that is "false" (approximately ground level) for 1.75 microseconds and "true" (approximately -6 volts) for 4.62 microseconds. The triggering action always occurs on the true-to-false transition of the waveform.

Two circuit boards are required to amplify and shape the clock signal. Clock power amplifier No. 1 performs the shaping of the signal and partially amplifies it. This board has two outputs. One, the strobe signal, is transmitted directly to all read amplifiers in the computer to gate memory reading; and the other, an inverted clock, is transmitted to clock power amplifier No. 2 for inversion and further power amplification. Figure 24 summarizes the various waveforms the clock signal takes as it goes through the shaping and amplification of clock boards No. 1 and No. 2.

Clock Power Amplifier No. 1

Refer to the block diagram of figure 26 during the following description.

The input to clock board No. 1 is a 4.5-volt peak-to-peak sine wave from the preamplifier of the clock read amplifier. Two clipper stages shape the signal into square wave form. In the one-shot trigger, the square wave is differentiated, resulting in positive-going and negative-going spikes. The positive spikes trigger the one-shot multivibrator where the clock pulse (false state) is developed. The clock pulse width is set to 1.75 microseconds in the multivibrator which permits the remainder of the clock cycle (true state) to have a duration of 4.62 microseconds, and the pulse frequency remains the same as the sine wave frequency. The output pulse of board No. 1 undergoes one stage of power amplification and then travels two paths. One path is through the strobe amplifier which amplifies the pulse for use in all read amplifiers. The other path is the input to board No. 2. There the pulse is inverted, the proper true and false levels are set, and the pulse is further amplified to drive the computer gate load.

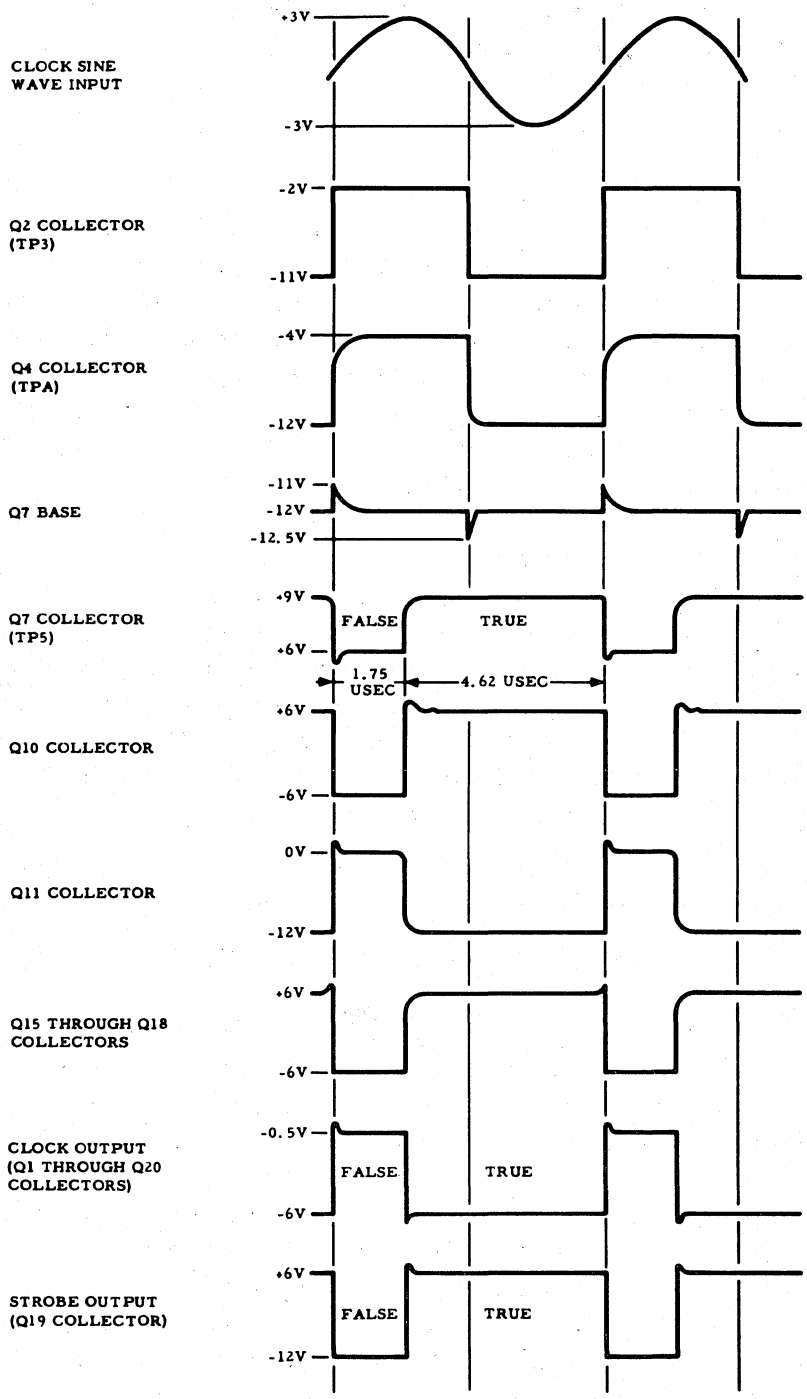

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Figure 25. Clock Circuit Waveforms and Approximate Voltages

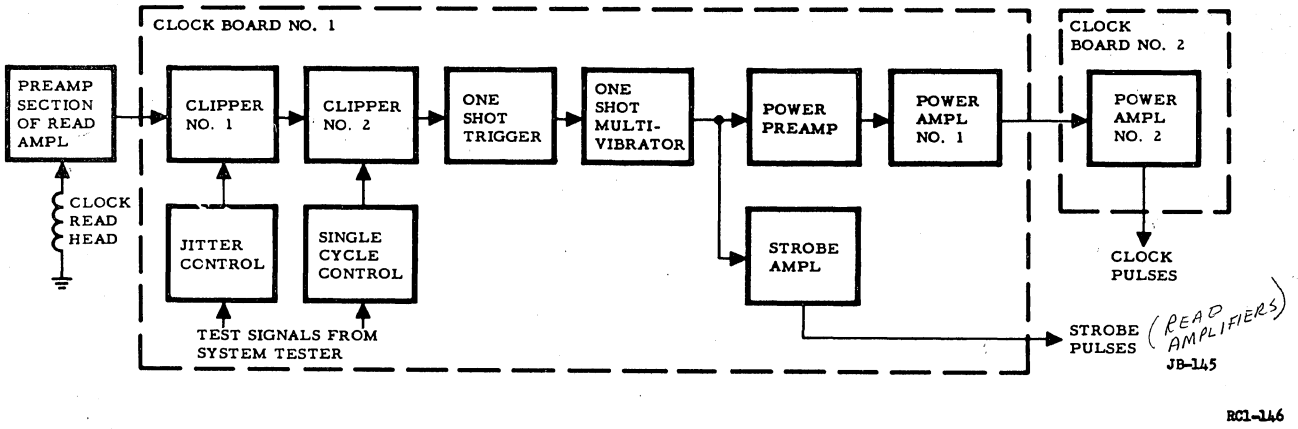

Figure 26. Clock Boards No. 1 and No. 2 Block Diagram

The jitter circuit is used only for marginal testing. Pulses (0 to -12 volts) from the system tester are applied to the first clipper stage. At the same time a control voltage of -25 volts originating in the system tester is applied to the jitter circuit. The simulated clock pulses developed in the first clipper stage establish bunched pairs of pulses in the clock power amplifiers, the spacing (jitter) of which may be varied by the potentiometer in the first clipper stage.

The single-cycle circuit is used only to test computer logic equations one term at a time. A voltage of -25 volts is applied to the second clipper stage from the component tester, which at the same time causes one or more clock pulses to be transmitted to the computer gates.

Clock Power Amplifier No. 2

After the inverted clock pulses have been shaped and partially amplified in board No. 1, they are applied to board No. 2, where they are inverted and provided the final current amplification required to drive the computer logic gates. Clock power amplifier No. 2 consists of 20 power amplifier switches (transistors) in parallel and 3 capacity dischargers. When the 12-volt negative-going clock pulses from board No. 1 are applied to the transistor switches, they conduct and their collector (output) potential swings from -6 volts to approximately -0.5 volt. The final clock voltage thus consists of a true level at -6 volts which lasts for 4.62 microseconds and a false level at -0.5 volt which lasts for 1.75 microseconds. The capacity dischargers switch the output rapidly to the true level (-6 volts) when the amplifier switches are being cut off.

LOGIC NETWORK

Computer operation is specified by the logic "equations" of the machine. These equations are mechanized by means of "and" and "and-or" diode logic gates standardized and mounted on the logic circuit boards.

The "and" gate has the characteristic of giving a true output signal only if all its input signals are true. For the typical "and" gate shown in figure 27, false input signals have a level of -0.5 volt and true signals have a level of -12 volts. The negative terminals of the diodes are connected through a common load resistor to a potential (-18 volts) that is more negative than either of the applied signals. The diodes are therefore forward-biased and current flows through the 16-kilohm resistor, the diodes, and the input circuit. With all input signals true, the output is at a nominal true level of approximately -12 volts; the actual level (approximately -8 volts) depends on flip-flop loading. However, if one of the input signals is false, the true signal is shorted out and the output remains at the false level.

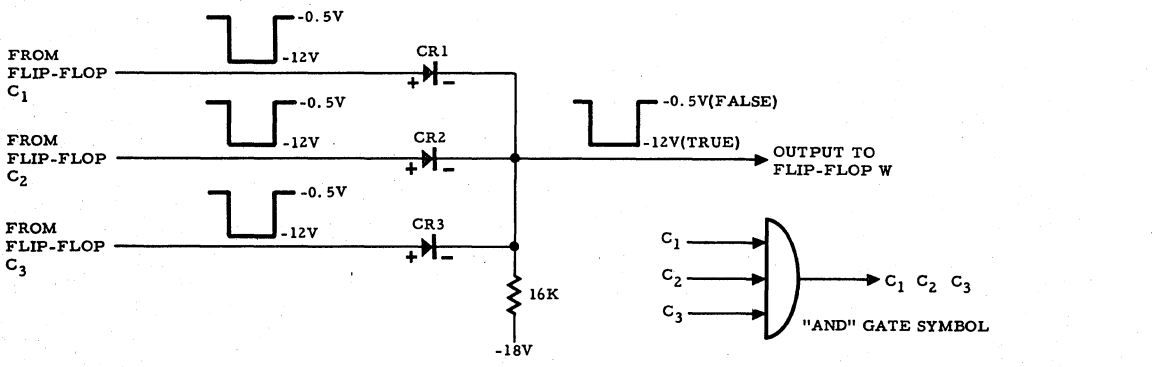

Figure 27. Typical Diode "And" Gate Schematic

"And-and" logic gates are used to mechanize terms of the logic equations that have common members; for example, $M_0'M_1'M_2'M_3'M_4'I_3$ in the following equations

$$0^a41 = A_1'(M_0'M_1'M_2'M_3'M_4'I_3)\ M_{10}'C$$
$$1^a41 = A_1\ (M_0'M_1'M_2'M_3'M_4'I_3)\ M_{10}'C$$
$$1^r41 = R_1\ (M_0'M_1'M_2'M_3'M_4'I_3)\ M_9'C$$
$$0^r41 = R'_1(M_0'M_1'M_2'M_3'M_4'I_3)\ M_9'C$$

The "and-and" gate representing this series of equations is simply a cascading of a common (primary) "and" gate with each "and" gate of the unlike members. (See figure 28.) The output of the common gate becomes one member of the secondary gate.

"And-or" gates are used to complete the mechanization of the computer logic equations. They are often connected between logic flip-flop stages shown in figure 29. The register shown in the diagram stores 37 digits on the

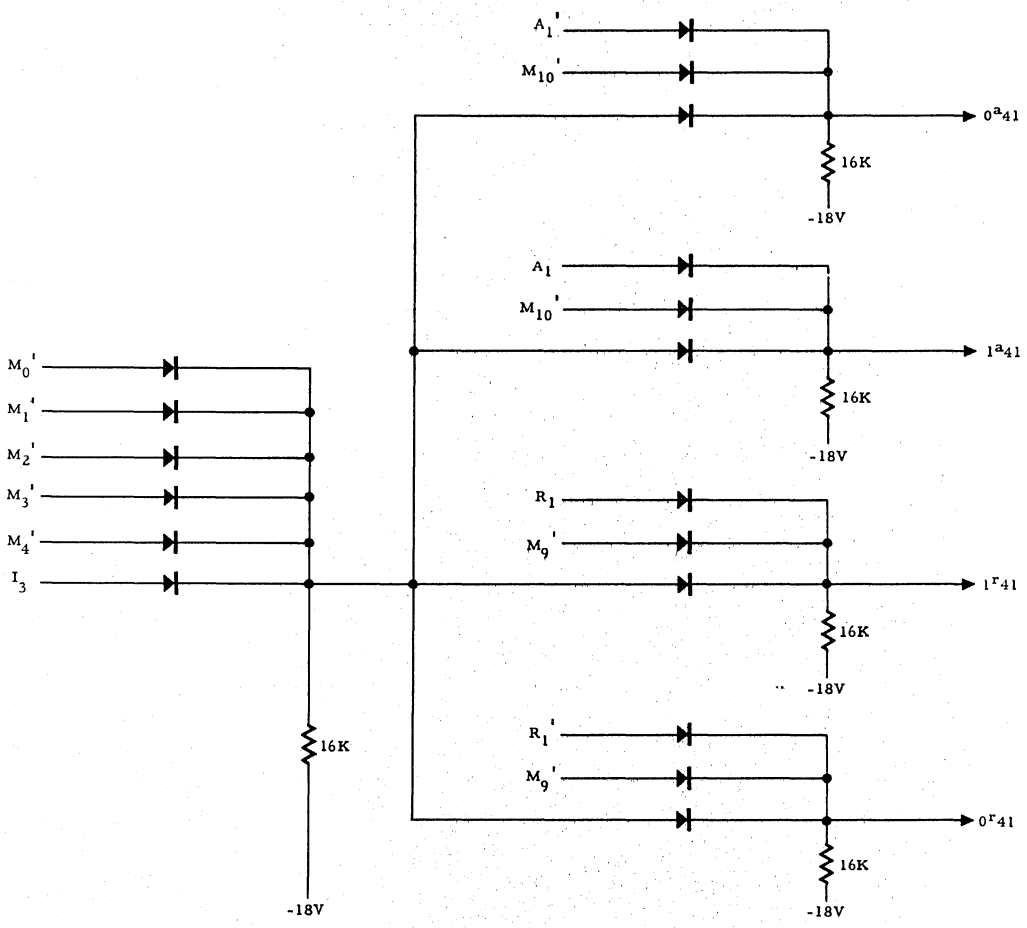

Figure 28. Typical Diode "And-And" Gate Schematic

memory disk and the remaining 4 digits in the 4 flip-flops. A delay built into each gate makes the input of the flip-flop independent of its own output for an interval of time. A typical logic equation mechanized by an "and-or" gate is

$$1x = A_1A_2A_3C + B_1B_2B_3C$$

The equation states that flip-flop X is 1-set if A_1 and A_2 and A_3 and C (clock signal) are true or if B_1 and B_2 and B_3 and C are true.

The logic as expressed in the equation above is mechanized by the "and-or" gate (figure 30) which consists of the following elements:

1. An "and" gate for each term of the logic equation
2. An "or" diode for each group of "and" terms of the logic equation
3. Clock diode for introduction of the clock signal (C)
4. Storage capacitor and associated resistor to provide logic delay
5. Series "or" diode and associated bleeder resistor for noise clipping
6. Flip-flop disconnect diode

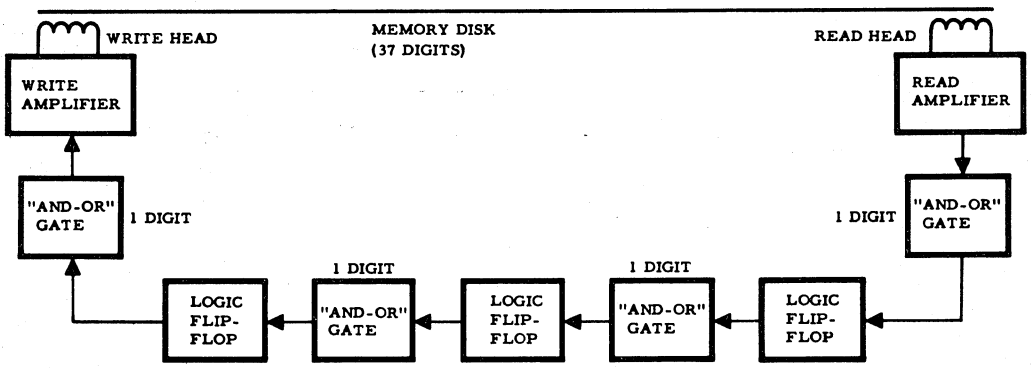

Figure 29. Use of "And-Or" Gates in a 1-Word Register Arithmetic

The "and" and "or" elements are mounted on standard logic boards, and the remaining elements of the gate are mounted on the flip-flop boards.

The flip-flop output signals A_1 through A_3 and B_1 through B_3 can be either false (-0.5 volt) or true (-12 volts). The clock signal (C) has a false level of -0.5 volt and a true level of -6 volts.

The following letters refer to point designations on figure 29.

1. Any false input signal to "and" gate $A_1A_2A_3$ establishes a false potential at point a. All inputs to this gate must be true to establish a true potential at point a. Thus the term $A_1A_2A_3$ in the equation is mechanized.

2. Likewise, for "and" gate $B_1B_2B_3$, false potential is established at point b if any input in false and true potential is established if all inputs are true. Thus the term $B_1B_2B_3$ is mechanized.

3. "Or" diodes CR7 and CR8 establish a true potential at this point if the outputs of either or both "and" gates are true. Thus the logic $A_1 A_2 A_3 + B_1B_2B_3$ is mechanized.

4. A true clock signal establishes a true potential at point e if either "and" gate output is true. If both gate outputs are false, a false potential exists at point e regardless of the clock state. Thus the logic $(A_1A_2A_3 + B_1B_2B_3)$ C is mechanized.

5. Storage capacitor C1 in association with resistor R4 and the -6-volt supply (-12 volts used in some gates) delays true information that arrives from the "and-or" part of the circuit during the true clock interval. At the start of the clock false interval, a trigger pulse is applied to the 1-set input of flip-flop X. Thus the logic equation $_1x = (A_1A_2A_3 + B_1B_2B_3)$ C is mechanized.

LOGIC FLIP-FLOP

Each flip-flop board includes four identical flip-flop circuits together with their associated input gates. A total of 42 identical boards is used.

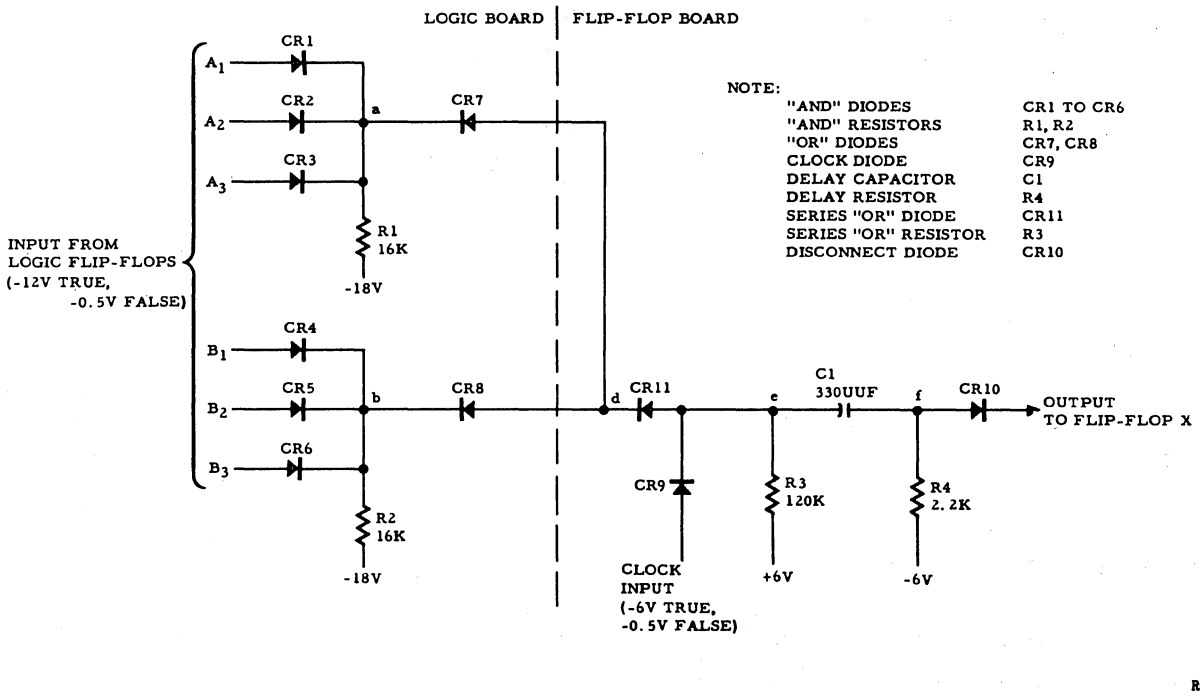

Figure 30. Typical "And-Or" Gate Schematic

The computer flip-flop is a bistable circuit used for counting, storing, or performing logic processes. The two stable states of the flip-flop can be designated as the digits 0 and 1 for counting or true and false for performing logic processes. All operations in the computer are based on the states of these flip-flops, which are controlled in accordance with the logic equations. One such logic equation is

$$o^{S}1 = S_2'N_1C + X_oC$$

which indicates that flip-flop S_1 is 0-set (1) if flip-flop S_2 is 0-set, flip-flop N_1 is 1-set, and the clock pulse is true; or (2) if flip-flop X_o is 1-set, and the clock pulse is true.

The term "logic" is used to distinguish these from the flip-flop circuits in the read amplifier and those in the write amplifiers. Logic flip-flop input and output signals are as follows:

Input from logic circuits:

0-set or 1-set signals	-0.5 volt (false level)
	-12 volts (true level)

Output to logic gates:

0-set	-0.5 volt (false level) -12 volts (true level)
1-set	-0.5 volt (false level) -12 volts (true level)

Set-reset signals from system tester:

Set (1-set)	+65 volts
Reset (0-set)	-200 volts

Operation of a logic flip-flop circuit may be summarized as follows (figure 31):

Logic gates can apply either 1-set or 0-set signals to the corresponding input gates of the flip-flop circuit.

If one input signal and the clock signal are both true, the input gate affected delays the signal during the clock true interval.

When the clock goes false, the input gate delivers a trigger pulse to the flip-flop.

Should the flip-flop be in the 1-state (1-set output true, 0-set output false), then a 0-set input signal is required in order to change the flip-flop to the opposite state (1-set output false, 0-set output true). When this action occurs, the 0-set output of the flip-flop turns off the corresponding power amplifier switch, which, in cutting off, provides a -12-volt (true) potential at the 0 output of the flip-flop board.

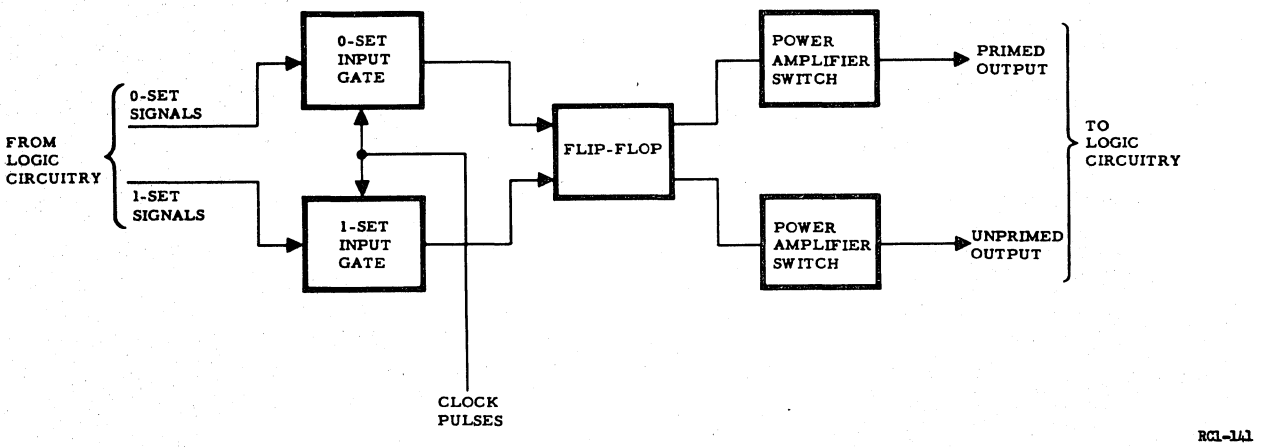

Figure 31. Flip-Flop Block Diagram

Similarly, should the flip-flop be in the 0-state, then a 1-set input signal is required in order to change the flip-flop to the opposite state. In this case, the 1-set output of the flip-flop turns off its associated power amplifier switch and a -12-volt (true) potential is provided at the 1-set output of the flip-flop board.

READ SWITCHING NETWORK

The read switching network selects the output of one information channel read head from eight read head outputs. Each of eight identical switching networks are mounted on a separate board. Figure 32 shows the application of a switching network in the selection of one read head signal from information channels 0 through 7. This is accomplished by a double-selection process. First, 64 read head signals are divided among 8 read switch networks. Each network, during any clock interval, gates only 1 of the 8 read head signals under the control of signals from 3 channel selector flip-flops (C_1 through C_3). Each of the eight selected read head signals is passed through a corresponding read amplifier as one input to an "and" gate. The second selection is accomplished at these 8 "and" gates by signals from the other 3 channel selector flip-flops C_4 through C_6.

During any clock interval, only one combination of signals from channel selector flip-flops C_1 through C_6 is possible, the number of possibilities being $2^6 = 64$; therefore, only 1 read head of the 64 can transfer information to the main memory read flip-flop (M_r) during any clock interval.

Each of the read switching networks contains eight transistor switches, connected in parallel with corresponding read heads. A switch driver is used as a logic inverter and power amplifier for gating one switch on each switching network. A summing amplifier amplifies the read head signal current and an emitter-follower applies the output signal to the associated read amplifier. Input and output signals of the read switching network are:

Input signals	Read head output pulses Maximum frequency: 160 kilocycles Waveform: approximate half sine waves Amplitude: 75 to 450 millivolts peak-to-peak
Gating signals	Channel selector flip-flop pulses Amplitude: -0.5 volt (false) -12 volts (true)
Output load	Read amplifier
Output signals	Maximum frequency: 80 kilocycles Waveform: approximate half sine waves, postive for "1" bits, negative for "0" bits Amplitude: 40 millivolts peak-to-peak

Operation of the read switching networks is summarized as follows: When the gating signals to one of the 8 drivers are true, the driver conducts and opens 1 read switch in each of the 8 read switching networks. As a result, one read head signal from each network enters its summing amplifier. At the same time, the drivers of the seven other networks receive false gating signals. Cutoff of these drivers causes the seven other switches of each network to conduct heavily and thus short out the corresponding read heads.

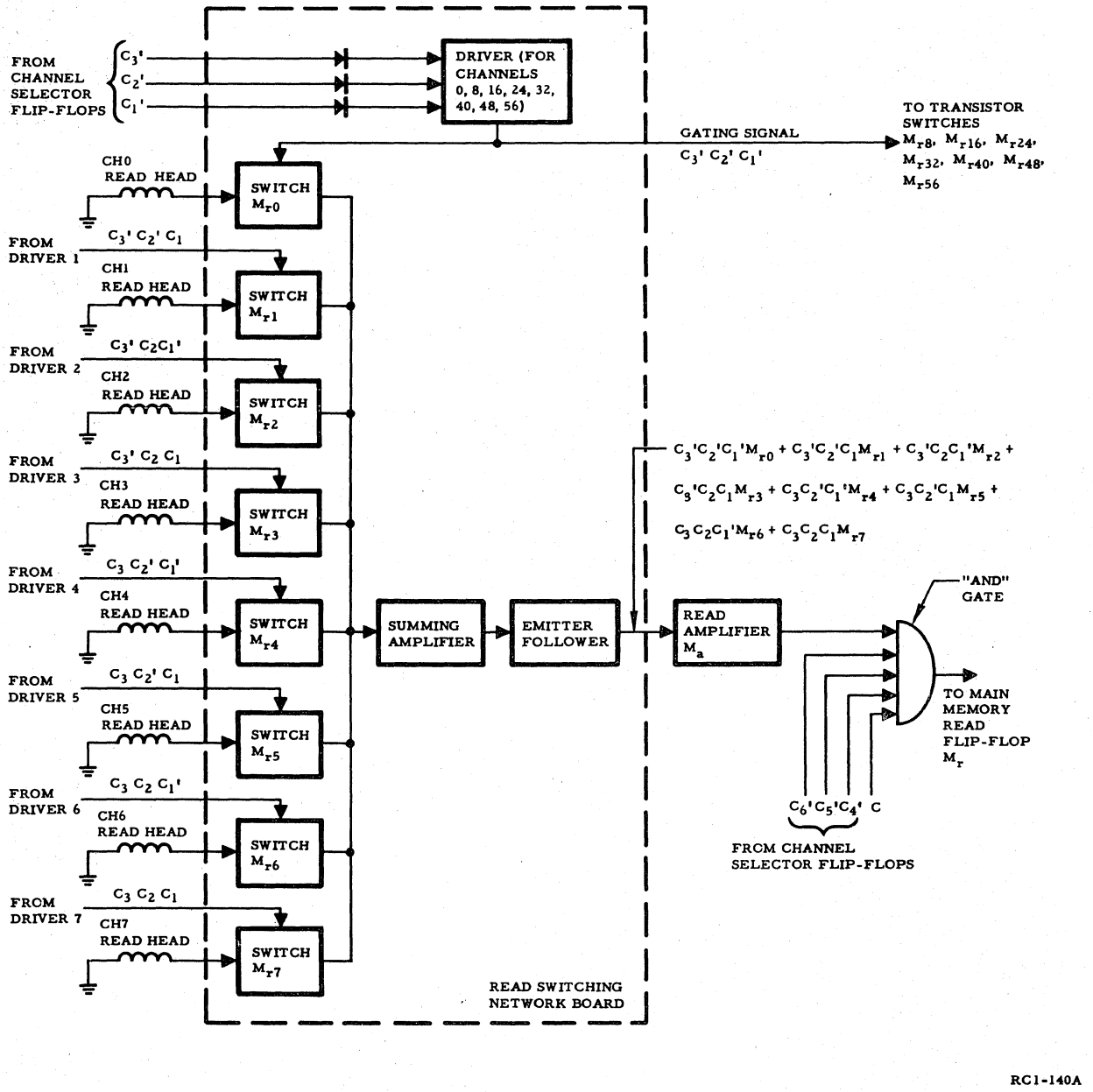

Figure 32. Read Switching Network Block Diagram

READ AMPLIFIER

The read amplifier is used to amplify and shape signals from the memory read heads. (See figure 33.) RECOMP II uses 19 read amplifiers: 8 for the 64 information channels, 2 each for the two 8-word loops (L and V), 5 for the five 1-word registers, 1 for the clock channel, and 1 for the origin channel. For the information channels, read amplifier input signals come from the read switching networks. For the other channels, input signals come directly from the read heads. Input and output signals of the read amplifier are:

Input signal	Pulses from read head or from read switching networks Amplitude: 75 to 450 millivolts peak-to-peak Waveform: approximate half sine waves Frequency: 160 kilocycles maximum
Reset signal	From memory synchronization flip-flop -0.5 volt (false) -12 volts (true)
Inverted clock signal (strobe)	+6 volts (true) -12 volts (false)
Output load	Maximum of 10 logic gates (1.2 milli-amperes per gate at 0-volt level)
Output signal	-9 volts (true) 0 volts (false)

The read amplifier is reset by a positive-going pulse from the memory synchronization flip-flop (M_S). At reset, the primed output is true (-9 volts) and the unprimed output is false (0 volts).

A 1-digit (+) memory read signal applied during a strobe false interval 1-sets the flip-flop power amplifier (false primed output and a true unprimed output).

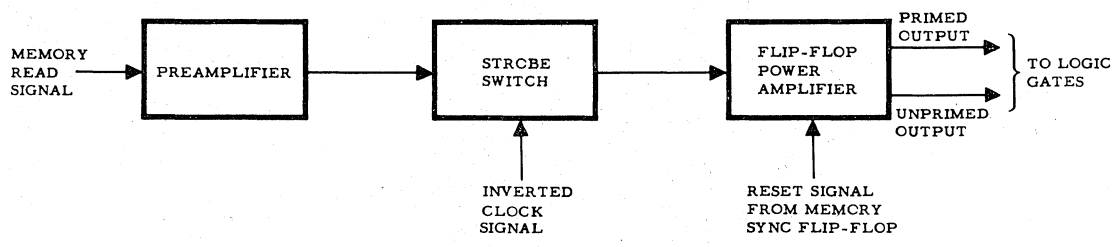

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Figure 33. Read Amplifier Block Diagram

A 0-digit memory read signal applied during a strobe false interval 0-sets the flip-flop power amplifier (true primed output and a false unprimed output).

WRITE SWITCHING NETWORK

Each word on the memory disk consists of 41 bits (binary digits) represented by positive changes of flux (1-bit) or negative changes of flux (0-bit). The bits are written on the disk by magnetic write heads, a total of 64 write heads being required for the 64 information channels. Circuitry for selecting a particular information channel write head consists of (1) a selection matrix gated by signals from the channel selector flip-flops and (2) the write switches gated by the matrix output. (See figure 34.) Eight identical write switching network boards provide the selection circuitry, each board containing eight transistor switches and associated "and" gates. Switching networks are not required for the write heads of the 8-word loops (L and V), and of the arithmetic registers. Signals from the write amplifiers are applied directly to the heads. Input and output signals of the write switching network are:

Gating signals	Channel selector flip-flop output signals True level: -12 volts nominal False level: -0.5 volt
Switch input and output	Write head current: 30 milliamperes

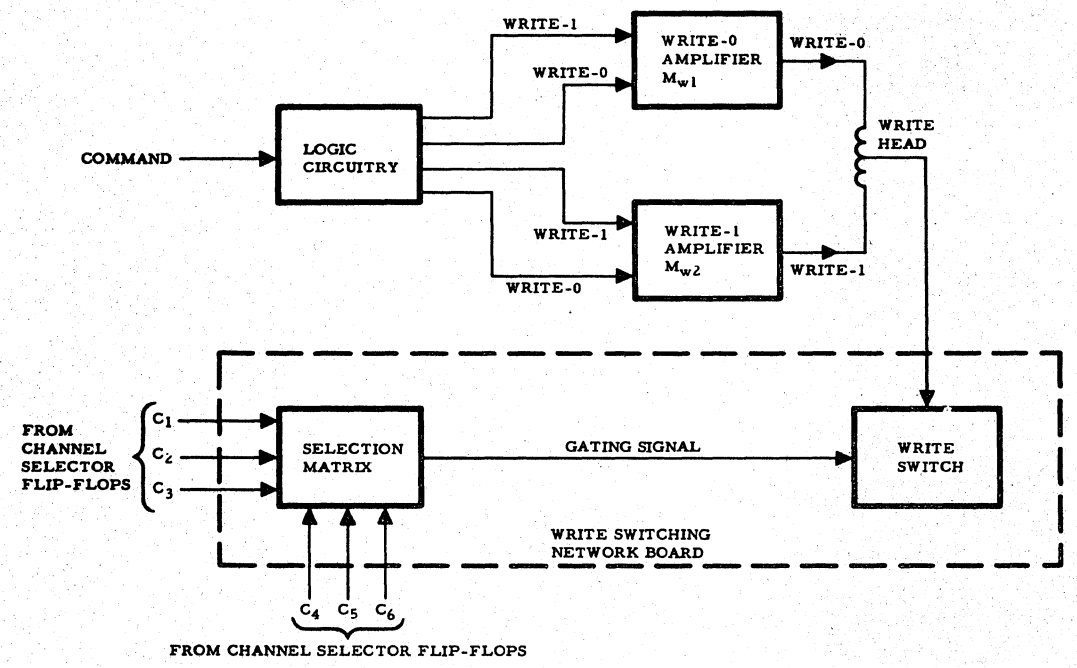

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Figure 34. Write Circuit Block Diagram

The write head selection matrix provides gating signals which select the proper write head for information channel recording. (See figure 35.) Only one write head is recording at any one time. This is accomplished by six channel selector flip-flops C_1 through C_6 which, by their bistable operation, produce $2^6 = 64$ possible gating combinations. In figure 34 these gating signals are shown numbered octally. The channel selector signals are divided into 2 groups of 3 each: C_1 through C_3 flip-flop outputs connected to the "and" gate of the matrix horizontal bus; and C_4 through C_6 connected to the "and" gate of the vertical bus. The outputs of the two gates are combined through "and" diodes, the junction being the gating point for the transistor switch. Because the "and" gate is true only if its input signals are true, only the proper combination of flip-flop signals will produce an output at the junction.

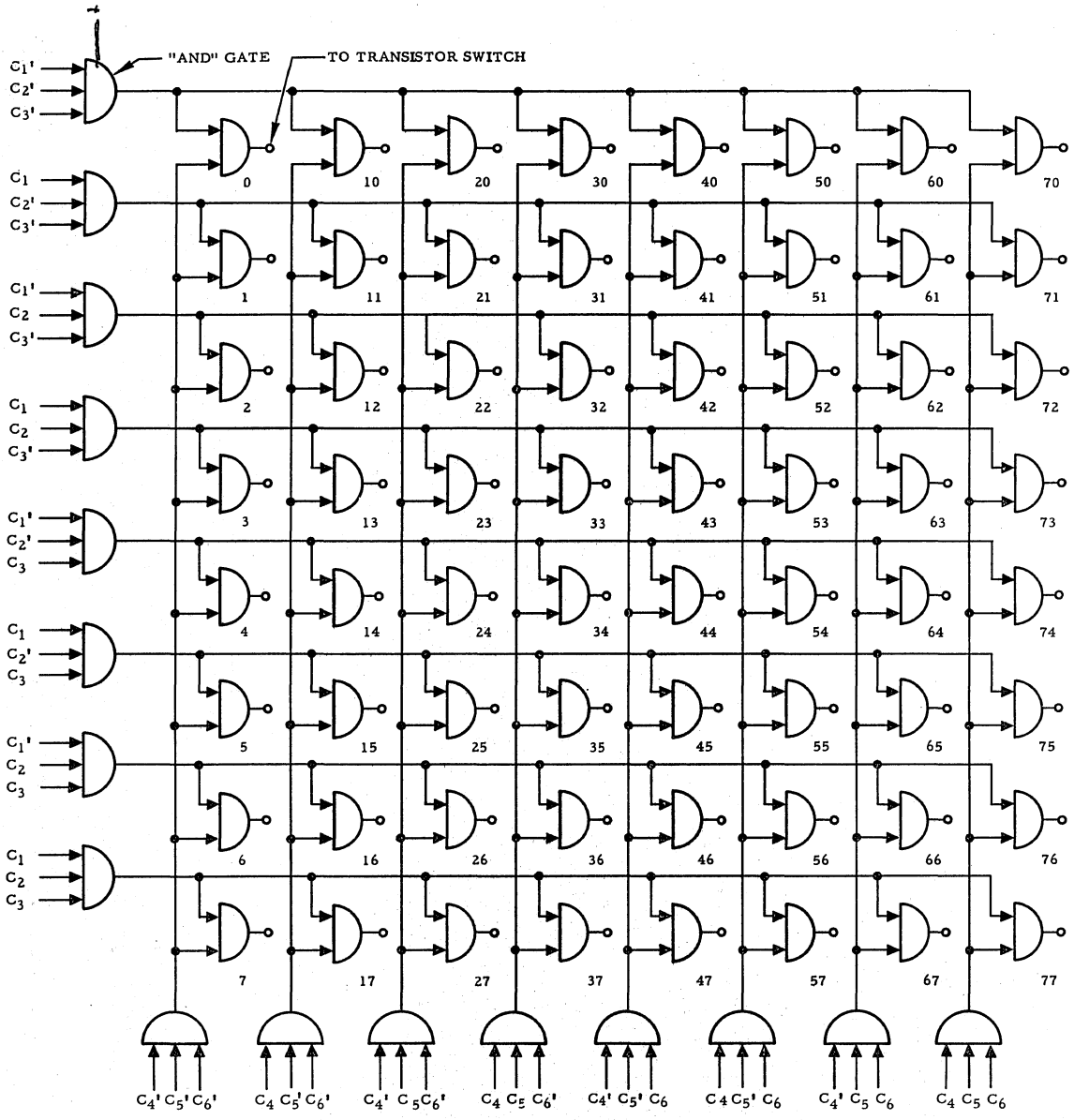

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Figure 35. Write Head Selection Matrix

At junction 43 (figure 35) for example, the combination $C_1C_2C_3'C_4'C_5'C_6$ must be true in order to write in channel 43 (octal). When 1 of 64 possible combinations of channel selector signals C_1 through C_6 is true, the selection matrix applies a gating pulse to the transistor switch. The switch, in turn, completes the circuit of the write -0 or write -1 current to the write head.

WRITE AMPLIFIER

The write amplifier supplies write head current for recording information on the memory disk. The computer uses a total of 3 write amplifier circuit boards, each containing 3 write amplifier flip-flops; 2 are common to each of the 64 information channels; the remaining are used for the high-speed loops and the 1-word registers.

Loop and Register Write Amplifiers

For the recirculating loops and registers, only two commands to the write head are possible: "write 1" or "write 0." (See figure 36.) Because a flip-flop has two stable states, only one flip-flop is required to supply the 0-bit and 1-bit signals to the write head. Input and output signals of the loop and register write amplifiers are:

Input signal	Pulses from logic flip-flops
	"Write 0" input: -0.5 volt (false)
	-12 volts (true)
	"Write 1" input: -0.5 volt (false)
	-12 volts (true)
Clock signals	-0.5 volt (false)
	-6 volts (true)
Set-reset signals	+65 volts (set)
(from system tester)	-200 volts (reset)
Output signals	"Write 0" or "write 1" current to write head
	30 milliamperes

Loop and register write amplifier signal functions are as follows:

1. A "write 1" or a "write 0" positive-going pulse is applied to the amplifier flip-flop during the false clock interval.
2. A "write 0" pulse causes the 0-bit (or prime) side of the flip-flop to conduct and apply a forward bias to the 0-bit power amplifier. Conduction of the power amplifier occurs through one side of the write head, permitting a 0-bit to be recorded.
3. A "write 1" pulse causes the 1-bit (or unprimed) side of the flip-flop to conduct and apply a forward bias to the 1-bit power amplifier. Conduction of the power amplifier occurs through the other side of the write head, recording a 1-bit.

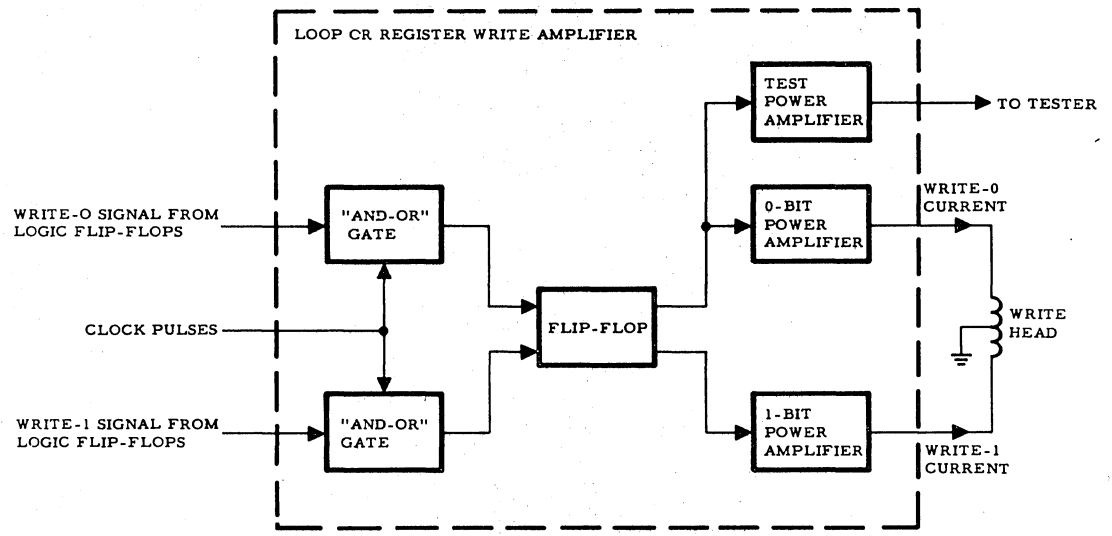

Figure 36. Loop and Register Write Amplifier Block Diagram

Information Channel Write Amplifier

The information channel write commands include not only "write 1" and "write 0" as for the loop write amplifiers but also "not write," a total of three commands. (See figure 37.) Two flip-flops can provide 2^2 or 4 possible outputs, one more than is required. These outputs are

Flip-Flop M_{W1}	Flip-Flop M_{W2}
0	0
1	0
0	1
1	1

Condition 11 is used for "not write." Condition 10 is used for "write 1," where the primed output of M_{W2} provides the writing current. Condition 01 is used for "write 0," where the primed output of M_{W1} provides the writing current. Condition 00 is never commanded by the logic and, consequently, is meaningless.

The operation of the information channel write amplifier circuitry is identical to that of the recirculating loop and the register write amplifiers with the following exceptions:

1. The 1-bit power amplifiers are disconnected from the output. Consequently, there is no output for a 1-bit input.

2. A 0-bit pulse causes the 0-bit side of the flip-flop to conduct and apply a forward bias to its power amplifier. Conduction of the power amplifier occurs when any switch in the write switching network is in the true state.

3. A 0-bit current from the M_{W1} write amplifier flows through one-half of the write head, magnetizing a 0-bit on the memory disk.

4. A 0-bit current from the M_{W2} write amplifier flows in the opposite direction through the other half of the write head, magnetizing a 1-bit on the memory.

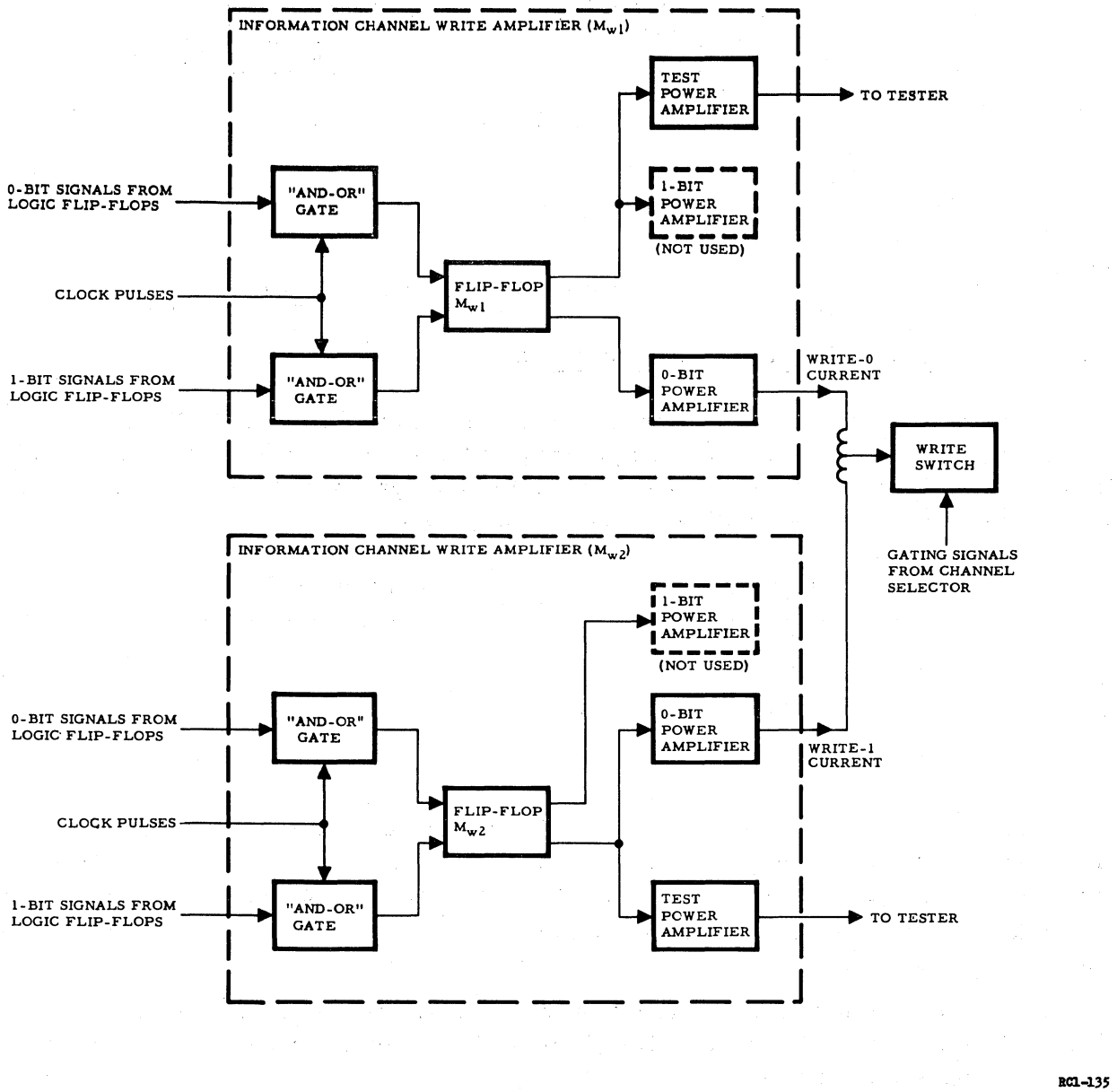

Figure 37. Information Channel Write Amplifier Block Diagram

NETWORK CIRCUIT BOARDS

Included as part of the signal circuitry already described, six network circuit boards provide miscellaneous circuitry for computer operations: clamping circuitry for transistor switches, additional padding resistors for the flip-flop outputs, attenuator networks for the scope readout jacks in the control console, networks for driving neon indicator lamps located in the control console and the photoelectric reader, and miscellaneous gates not provided on the logic boards.

TROUBLE ANALYSIS AND ADJUSTMENTS

GENERAL

Trouble analysis for the computer assembly is presented in the following paragraphs on the basis that the more general and more inclusive checkout procedures of the system service manual have first been performed in an attempt to locate the malfunction. Thus, the only detailed trouble analysis procedures presented in this manual are those for testing etched circuit boards using the component tester.

Adjustments, on the other hand, are described in detail in this section. For normal maintenance of RECOMP II, only electrical adjustments need be made. Adjustments should not be attempted on the memory unit.

COMPONENT TESTER

The component tester is a self-contained portable console used to functionally check out the following circuit boards:

Logic network
Read switching
Read amplifier
Write switching
Write amplifier
Flip-flop
Network
Clock power amplifier No. 1
Clock power amplifier No. 2
Power supply (3 boards)
Relay control network
Network, power supply
Filter network

The necessary controls to accomplish these checks are grouped into individual test sections and labeled to indicate the board tested. The external and internal test points referred to in test procedures are located on the right- and left-hand side of the component tester, respectively. Component tester voltage and signal levels (simulated computer signals) are monitored at the component tester INTERNAL TEST POINTS. Table 1 lists INTERNAL TEST POINTS for monitoring component tester voltage and signal levels. The internal test points contain the information as shown in the table and are adjusted (if applicable) according to information under the "remarks" column.

Table 1. Internal Test Points

TP No.	Signal or Voltage Level	Tolerance (volts dc)	Remarks
1	F - F 1: 1-input gating signal	Tolerances for test points 1 through 16 are as follows: upper limit: 0 to -1 lower limit: more negative than -6	Remarks apply for test points 1 through 16. Rise time: 2 micro-seconds
2	F - F 1: 0-input gating signal		
3	F - F 1: unprimed output square wave		
4	F - F 1: primed output square wave		
5	F - F 2: 1-input gating signal		
6	F - F 2: 0-input gating signal		
7	F - F 2: unprimed output square wave		
8	F - F 2: primed output square wave		
9	F - F 3: 1-input gating signal		
10	F - F 3: 0-input gating signal		
11	F - F 3: unprimed output square wave		
12	F - F 3: primed output square wave		
13	F - F 4: 1-input gating signal		
14	F - F 4: 0-input gating signal		
15	F - F 4: unprimed output square wave		
16	F - F 4: primed output square wave		
17	Clock pulse output pulse train	Between -1 and -6.0	Amplitude variable by CLOCK AMPLITUDE control on front panel
18	Clock pulse output pulse train	-6±0.5	Nonvariable amplitude

Table 1. (Continued)

TP No.	Signal or Voltage Level	Tolerance (volts dc)	Remarks
19	78.7-kilocycle sine wave	2 volts peak-to-peak	Amplitude variable by R7 (also stability control provided by R6)
20	157.7-kilocycle sine wave	6 volts peak-to-peak	Amplitude variable by R5
21	600.0-cps sine wave	4 volts peak-to-peak	Amplitude variable by R3
22	10.0-kilocycle sine wave	4 volts peak-to-peak	Amplitude variable by R2
23	120.0-kilocycle sine wave	4 volts peak-to-peak	Amplitude variable by R4
24	Clock strobe output		Clock strobe output not clamped
25	-0.7-volt dc	±0.1	Fixed
26	-3.0-volt dc	-0.25 +1.50	Fixed
27	-6.0-volt dc	±0.5	Adjustable by R32 on +6, -6, +0.75 power supply board
28	-12.0-volt dc	±1.0	Adjustable by R27 on -12, +75 power supply board
29	-18.0-volt dc	±1.5	Adjustable by R15 on -18, -100, -3 v power supply board
30	-100-volt dc	±15	Unregulated
31	-200-volt dc	±40	Fixed, unregulated
32	+0.75-volt dc	±0.15	Fixed
33	+6-volt dc	±0.5	Adjustable by R24 on +6, -6, +0.75 v power supply board
34	+50.0-volt dc	±3.0	Adjustable by R12 on -200, +50, -1, -0.7 power supply board
35	+75.0-volt dc	±5.0	Adjustable by R23 on -12, +75 v power supply board
36	+75.0-volt dc	±10	High impedance
37	-1.0-volt dc		Adjustable by R3 on -200, +50, -1, 0.7 power supply board
38	GRD	0	Tester ground level

TEST EQUIPMENT REQUIRED

In addition to the component tester, some checkout and adjustment procedures often require the use of standard test equipment. The following items are recommended:

Oscilloscope
Multimeter (20 kilohms per volt)
Variac (115 volts, single phase)

SPECIAL TOOLS SUPPLIED

Two etched-circuit board extractors (figure 38) are supplied for removing computer circuit boards during maintenance.

MEMORY

It is convenient to consider the read and write circuitry of the computer in conjunction with the memory. Therefore, this section contains instructions primarily for adjusting the circuitry associated with the memory. If a computer malfunction is traced to the memory units, it may be necessary to replace it with a spare because adjustments to the memory mechanism or to the magnetic heads are very critical, and except in very rare instances these adjustments must be performed at Autonetics.

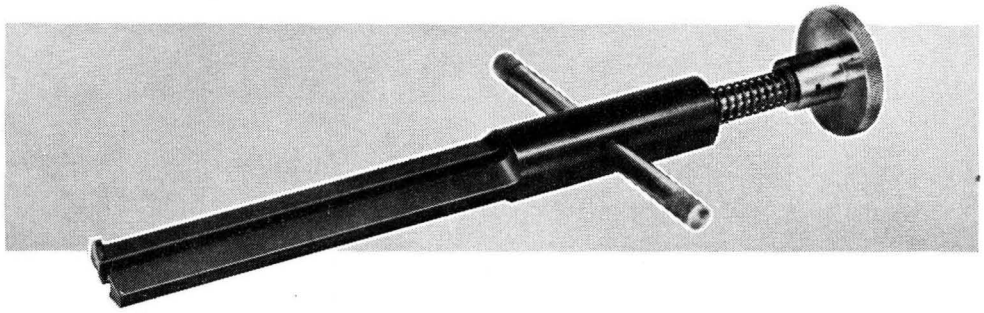

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Figure 38. Etched Circuit Board Extractor

Memory gain readjustments are usually necessary for channels or loops whenever any board replacements are made in the write-read circuitry of the computer. The 11 read amplifiers used in the loops and registers read signals directly from the read heads. The remaining 8 read amplifiers receive signals through a read switch selection arrangement from the 64 main memory channel read heads. Thus, main memory gain adjustments involve setting trimpots on both the read switches and the read amplifiers.

Strobe pulse timing may be checked at the same time that memory gain adjustments are made.

CLOCK CHANNEL GAIN ADJUSTMENT

The output of the clock read head is amplified first by the read amplifier board which plugs into the circuit board mounting panel at connector 439 - 539. The preamplifier output of the amplifier is monitored at the memory test receptacle 525 located on the circuit board mounting panel next to the read amplifier boards in side No. 1. To adjust the clock read signal gain at the preamplifier output, proceed as follows:

1. Using an oscilloscope, monitor the preamplifier output of the clock read amplifier at pin 11 of plug 525 (memory test receptacle).
2. Adjust the trimpot on the clock read amplifier until the output shows 4.5± 0.5 volts peak-to-peak on the oscilloscope.
3. When the gain has been adjusted, the final output should be checked on the oscilloscope at pins 36 and 37 of connector 339 (check both).
4. Final output of the clock should be as shown in figure 39.

ORIGIN CHANNEL GAIN ADJUSTMENT

The origin pulse occurs once for every disk revolution or once every 17 milliseconds. The output of the origin read head is amplified by the read amplifier board that plugs into the circuit board mounting panel at connectors 438 and 538. The preamplifier output of the read amplifier is monitored at the memory test receptacle 525, pin 10. To adjust the signal gain for the preamplifier output, proceed as follows:

1. Using an oscilloscope, monitor the preamplifier output of the origin read amplifier at pin 10 of connector 525 (memory test receptacle).
2. Adjust the trimpot on the origin read amplifier until the output shows 4.5± 0.5 volts peak-to-peak on the oscilloscope.
3. When the gain has been adjusted, the origin signal is further amplified and shaped by the read amplifier, and should be checked by means of the oscilloscope at pins 12 and 13 of connector 438 (check both). The origin wave shapes and timing should be as shown in figure 40.
4. If the preamplified origin signal does not meet the tolerances shown in figure 40, the magnetic memory may need to be sent back to the factory for rewriting of the origin track.

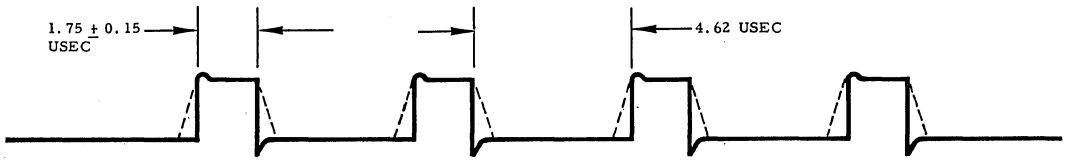

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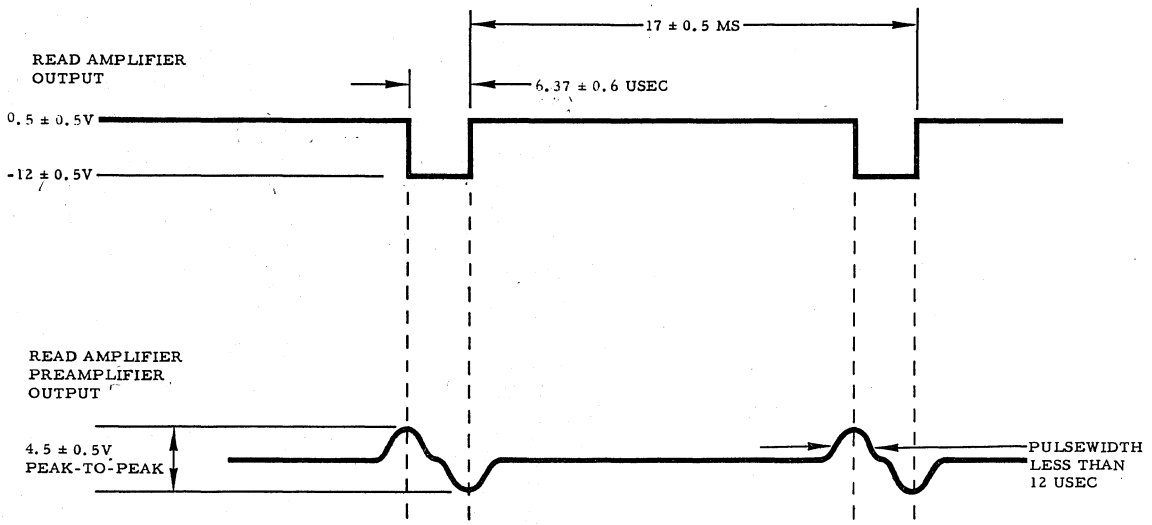
Figure 39. Clock Wave Shape



RC1-193

Figure 40. Origin Wave Shapes

MAIN MEMORY CHANNEL GAIN ADJUSTMENT

The read head signals from the 64 main memory channels (numbered octally from 00 to 77) provide inputs to 8 read switch boards. The gain adjustments involve 4 major steps:

1. Filling the appropriate channels with information.
2. Selecting each of the eight channel read heads that provide inputs to the particular read switch board and read amplifier board to be adjusted.

3. Monitoring the read amplifier preamplifier output for deviation from 4.5-volt peak-to-peak signals from each of the eight channels. The read amplifier board receives signals from the 8 read switches of 1 read switch board.

4. Making appropriate trimpot adjustments on the read switch board and on the read amplifier board so that each of the eight channel outputs causes a 4.5-volt peak-to-peak signal at the output of the preamplifier stage of the read amplifier board.

Normally, there will be programmed information in at least one location of each channel to be tested, and this information will cause the particular read heads to transmit a signal. However, the procedures presented here required the use of a test pattern. Once the channels have been filled with this pattern, each of the 8 read switch boards which control 8 read head signals to 1 read amplifier may be adjusted for the proper gain as described in steps 2 through 4.

In making the read head selection, only 3 channel selector flip-flops, C_3 through C_1, need be set on the system tester. Table 2 shows the settings necessary to select each of the 8 channels for input into each of the 8 read switch boards. The order is such that 1 0 1 means "1-set C_3, 0-set C_2, 1-set C_1".

Table 2. Channel Selector Flip-Flop Settings
For Main Memory Gain Adjustment

C_3	C_2	C_1	Read switch number and selected channel*							
			349	348	347	346	345	344	343	342
0	0	0	70	60	50	40	30	20	10	00
0	0	1	71	61	51	41	31	21	11	01
0	1	0	72	62	52	42	32	22	12	02
0	1	1	73	63	53	43	33	23	13	03
1	0	0	74	64	54	44	34	24	14	04
1	0	1	75	65	55	45	35	25	15	05
1	1	0	76	66	56	46	36	26	16	06
1	1	1	77	67	57	47	37	27	17	07

*Signal groups from right to left are: M_{ra}, M_{rb}, M_{rc}, M_{rd}, M_{re}, M_{rf}, M_{rg}, M_{rh}

Note from table 2 that plug 342 of the circuit board mounting panel provides eight consecutive memory channel read signals starting with channel 00 (octal). This group of read head signals is given the designation M_{ra}. Referring to the signal chart (figure A-8) note also that the read amplifier board which receives this group of signals is the one found in connector 442-542. In the following procedures the preamplifier output of each read amplifier is monitored by means of the oscilloscope at test plug 550 located on the circuit board mounting panel next to the read amplifier boards in side No. 2.

To adjust the read signals at the preamplifier outputs, proceed as follows:

1. Using the control console, fill the following pattern in command format in the last sector (77) of channels 00 through 07, i.e., 0077, 0177, 0277, 0377, 0477, 0577, 0677, 0777:

+ 2525250 + 2525250

2. Using an oscilloscope, monitor the preamplifier output of M_{ra} at pin 1 of plug 550 (memory test receptacle). Trigger the oscilloscope at flip-flop T_{41} at the system tester.

3. Ground flip-flop D_0 at system tester.

4. Adjust the trimpot on read amplifier (M_{ra}) for minimum gain.

5. By setting C_3, C_2, and C_1 at the system tester as shown in table 2, display channels 00 through 07 on the oscilloscope. For each setting, adjust the read switch trimpots of each channel (read switch in plug 342) for maximum signal and then reduce each setting by two turns.

6. Note which of the eight channels gives the lowest output. (It may be necessary to adjust the oscilloscope gain.)

7. Adjust the read amplifier (M_{ra}) trimpot until the output from the lowest channel (read switch) shows 4.5± 0.5 volts peak-to-peak.

8. Reduce each read switch trimpot setting for the seven other channels until they also show 4.5± 0.5 volts peak-to-peak at the preamplifier output.

Note

Strobe pulse pickup and feed-through as observed on the oscilloscope are not to be considered noise.

9. Repeat procedures 1 through 8 for signal groups M_{rb}, M_{rc}, M_{rd}, M_{re}, M_{rf}, M_{rg}, and M_{rh}. Each group should be monitored at the following pin numbers of memory test receptacle 550:

Signal Group	550 Pin Number
M_{rb}	2
M_{rc}	3
M_{rd}	4
M_{re}	5
M_{rf}	6
M_{rg}	7
M_{rh}	8

LOOP GAIN ADJUSTMENT

The long loops (L and V) and the short loops (1-word registers) transmit signals directly from the read heads to their respective read amplifiers. Procedures for checking the gain of a loop involves connecting the outputs of flip-flop T_1, available at the system tester, to the 1-set and 0-set inputs of the write amplifiers of each loop. Flip-flop T_1 is 1-set at bit time 1 of each word (bit time 2 through 41 T_1 is 0-set).

Loading each loop with a 1-pulse pattern per word serves a double purpose in that the signal can be used for monitoring the gain and also for checking loop length (each word location contains 41 bits) through pulse coincidence.

To adjust the gain of the read head signal for each loop, the preamplifier output of each read amplifier is monitored at memory test receptacle 525. The 1-set and 0-set inputs to each loop write amplifier are connected to flip-flop T_1 and T_1' respectively as shown in table 3. To adjust the gain of a loop, proceed as follows:

1. Using an oscilloscope, monitor the preamplifier output of the read amplifier of the loop to be adjusted at the pin indicated in table 3 (oscilloscope is triggered from flip-flop T_{41}, available at the system tester).
2. Connect T_1 and T_1' to the 1-set and 0-set inputs of the write amplifier of the loop to be adjusted as shown in table 3.

Table 3. Flip-Flop T_1 and Preamplifier Connections

Loop	T_1 Connected To 1-Set Input of Write Amplifier	T_1' Connected To 0-Set Input of Write Amplifier	Oscilloscope Connected to Preamplifier Output Pin Number of Memory Test Receptacle 525
Z	330-5	330-1	Pin 5
B	330-31	330-27	Pin 15
L	330-19	330-13	Pin 7* Pin 6*
X	331-5	331-1	Pin 4
R	331-31	331-27	Pin 3
A	331-19	331-13	Pin 1
V	332-31	332-27	Pin 9* Pin 8*

*L and V loops each contain two read heads which transmit signals to separate read amplifiers.

3. The trimpot on the read amplifier of each loop should be adjusted until the output on the oscilloscope shows 4.5± 0.5 volts peak-to-peak.

CHECK OF MEMORY CHANNEL LENGTH

Improper readout of a particular channel may occur because the magnetic read head has been incorrectly positioned or has worked loose and shifted. This special procedure is presented for checking the loop length of any channel from 00 through 77.

1. Using the control console, fill the following pattern in command format in sector 1 of the channel. For example, in channel 07, first location = 07010, fill:

-0000000 -0000040

2. Read out the location entered. If the pattern does not read out as entered, the read head may be improperly positioned. Table 4 indicates, for various possible readouts, the probable incorrect channel lengths. If meaningless readouts occur, the malfunction is probably due to circuit difficulties rather than memory misadjustment.

Table 4. Channel Length Indications

Pattern of Readout	Channel Length is:
-00 00000 0 00 00020	1 bit too short
-00 00000 0 00 00010	2 bits too short
-00 00000 0 00 00100	1 bit too long
-00 00000 0 00 00200	2 bits too long

CHECK OF LOOP LENGTHS

To check for correct length of either a long or short loop, proceed as follows:

1. Connect T_1 to the 1-set input and T_1' to the 0-set input of the write amplifier of the register or loop to be adjusted as shown in table 3.

2. If a dual trace oscilloscope is available, connect the A and B inputs of the oscilloscope to the flip-flops designated for the loop under test as shown in table 5. (All flip-flops shown in the table are available at the system tester.

Table 5. Pulse Coincidence

Loop	A Input of Scope	B Input of Scope	Read Head
Z	Z_1	T_1	Z_R
B	B_{41}	T_1	B_R
L	L_1 L_{2a}	T_1 T_{41}	L_{R8} L_{R4}
X	X_{41}	T_1	X_R
R	R_{41}	T_1	R_r
A	A_{40}	T_1	A_R
V	V_1 V_{2a}	T_1 T_{41}	V_{r8} V_{r4}

3. Observe for pulse coincidence between the two flip-flops on the oscilloscope. If the pulse on input A is lagging the pulse on B, the loop is too long. If the pulse on input A is leading the pulse on input B, the loop is short. When coincidence between pulses is observed on the oscilloscope, the loop length is correct.

MEMORY CHANNEL TIMING CHECK

If strobe timing is off, read head signals may not be gated at the right time and intermittent errors in readout may result.

The strobe timing may be checked whenever read signal gain is adjusted because the waveform is then available at the preamplifier output. The strobe pulse should set directly on the peak of the preamplifier gain signal as illustrated in figure 41 or figure 42.

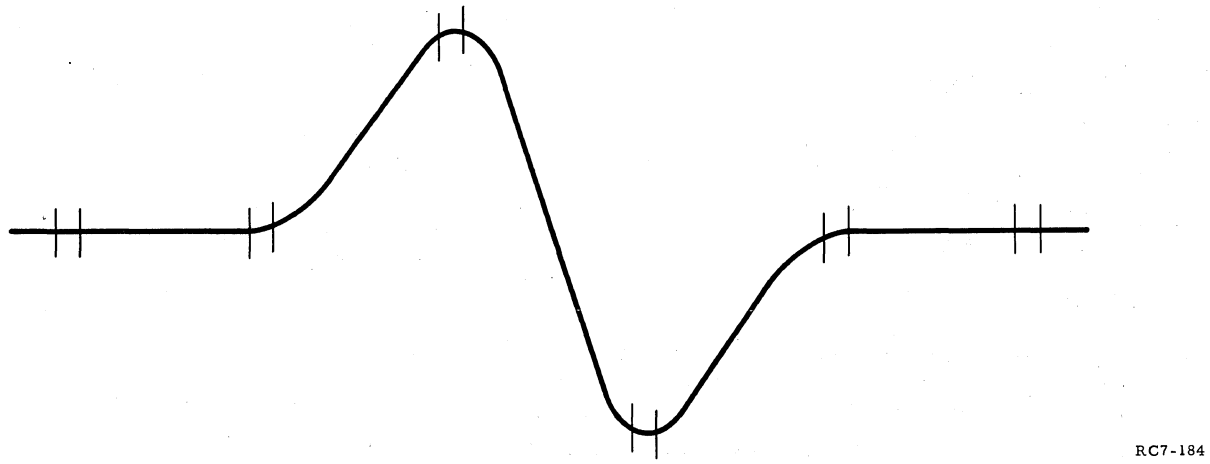


Figure 41. Strobe for Normal Pulse

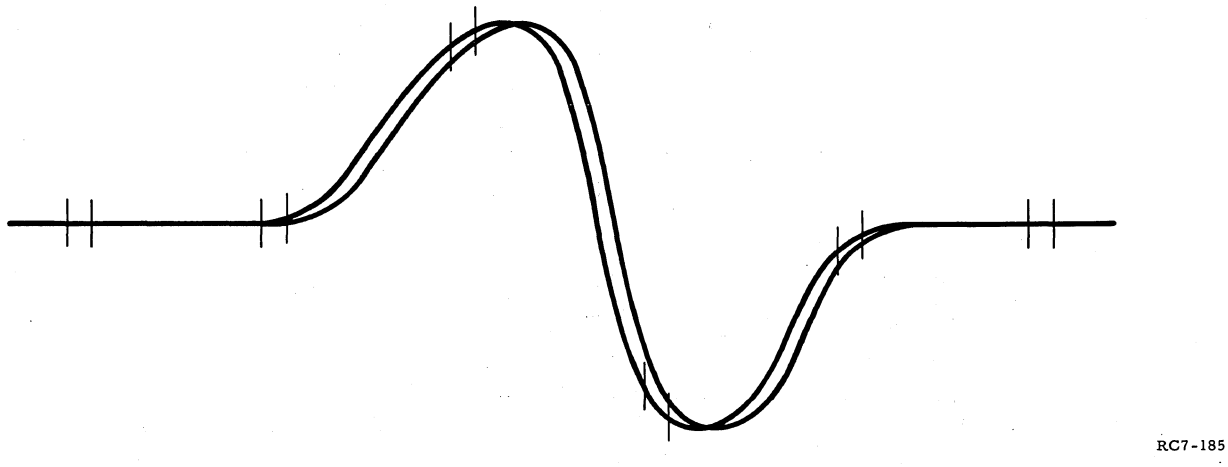


Figure 42. Strobe Setting for Wide Pulse With Some Jitter

LOOP STROBE TIMING CHECK

To check for proper strobing of a loop (L or V) or a 1-word register, proceed as follows:

1. Repeat procedures 1 through 3 of Loop Gain Adjustment, page 50, using the preamplifier output and flip-flop connections shown in table 3.
2. Looking at the preamplifer signal on the oscilloscope, the strobe should reset directly on the peak of the signal as shown in figure 41 or figure 42.

POWER CIRCUITS

PRELIMINARY TESTS AND ADJUSTMENTS

The computer control console may be connected to the computer for application of power through the POWER ON switch. If the control console is disconnected, power may be applied to the computer by shorting pins 35 and 36 of J27.

Application of computer power is dependent on certain temperature conditions existing in the memory assembly and power supply environments:

1. The power supply thermostat (located on -18-, -100-, and -3-volt power supply board 65536-501) will open at 120°F or higher, thereby removing power from the computer.
2. The memory thermostat located on the memory assembly housing will also open at 120°F thereby removing power from the memory.

To provide the proper environmental conditions in these areas, the blowers must be operating and the air filters must be clean. Awareness of these conditions will help to check out specific environmental parts.

Because of the many relays and other control elements involved in properly sequencing power to the various electrical parts of the computer, the functional description of power control sequencing, page 12, with corresponding references in figure 14 should be followed. Knowledge of the computer power control circuitry and timing in conjunction with continuity test, will pinpoint trouble with control circuitry. Use of S1 and S2 interlock switches will narrow the search, as is shown in the following tabulation.

Interlock Switch Positions	Parts Energized	Parts Deenergized
S1 closed and S2 open	All d-c secondary power supplies	Memory solenoid Power ready lamp (control console) Memory motor
S1 open, or S1 and S2 both	Power ON lamp (Control console) Blowers (computer and control console) Running time meter Power supply thermostat	Secondary power supplies Memory motor Memory solenoid Power Ready lamp (control console)

Table 6. Power Supply Voltages

Level	Normal Load (amperes)	Normal Load Resistance (ohms)	Adjustment Trimpot
-18	1.8	10	R15
-12	1.8	6.7	R27
-6	2.5	2.4	R32
+6	1.3	4.6	R24
+75	0.06	1250	R23
-100	0.46	217	Not adjustable

Note

Load resistance is measured with computer de-energized. Trimpots are on individual boards.

Power control circuits may be operating properly, but secondary power supply levels may be improper. Thus, before going to detailed tests of power circuits, first check the secondary levels by means of the power supply voltmeter at the rear of the control console. Table 6 shows the d-c voltage levels that should be observed and indicates the trimpots by which the levels can be adjusted. (Meter reads 100 percent ±5 percent when levels are correct.)

If the voltages cannot be adjusted properly, next check the power transformer secondary voltages as shown in table 7.

Table 7. Power Transformer Voltages

Voltages Supply (volts)	Power Transformer Connect or P21 Terminals	Voltage Measurement (volts rms)
Primary	1	115
	2	
-6	7	19.7±0.4
	8	
+6	9	16.5±0.4
	10	
-12	5	27.1±0.6
	6	
-18	3	33±0.7
	4	
+75	13	118±2
	14	
-100	11	114±2
	12	

If the transformer voltages measure within the specified tolerances, and the power control circuits are operating normally, but the correct d-c voltages still cannot be obtained, the power supply circuit boards should be tested on the component tester as described in the following procedures.

POWER SUPPLY CIRCUIT BOARD TESTS

All computer power supply etched boards are tested with the controls on the 4-POWER SUPPLY section of the component tester. The tests for regulated voltage levels are performed by adjusting the voltage centerpoint at half-load conditions, then checking the voltage drop when full-load is applied.

Operation of bridge and filter circuits is checked by monitoring the voltage outputs at test points by using the panel meters or by additional test equipment.

Before performing any test, the following preparation should be completed:

1. Set MASTER SELECTOR switch to 4.
2. Set POWER switch to OFF.
3. Set LOAD switch to HALF.
4. Set RELAY CONTROL switch to 1.
5. Set bridge switch to OFF.

CAUTION

Always place POWER switch to OFF before inserting or removing a circuit board.

+6-, -6-, +0.75-Volt Power Supply Board

This etched board contains the +6-volt bridge rectifier and the +6-, -6-, and +0.75-volt power supplies. To check for correct circuit continuity for each voltage level, proceed as follows:

1. Perform preparation procedure for Power Supply Circuit Board Tests, page 55.
2. Plug etched board into +6 , -6 , +0.75 VOLT POWER SUPPLY test jack at top of tester.
3. Set LEVEL SELECTOR switch to 1. This sets up the correct circuit for the +6-volt level.
4. Connect a multimeter between EXTERNAL TEST POINT 4-26 and ground. The reading should be no less than 40 ohms.
5. Reverse multimeter connections. The reading should be no less than 40 ohms.

6. Set LEVEL SELECTOR switch to 2. This sets up the correct circuit for the -6-volt level.

7. Repeat procedures 4 and 5. The readings should be no less than 40 ohms.

8. Set LEVEL SELECTOR switch to 3. This sets up the correct circuit for the 0.75-volt level.

9. Repeat procedures 4 and 5. The readings should be no less than 40 ohms.

The requirements for the power supply load tests are that the level be adjusted to the voltage centerpoint at half load and drop less than the specified amount when full load is applied for those levels that are adjustable. To test each load level of the power supply circuit board, proceed as follows:

1. Set POWER switch to ON.
2. Set LEVEL SELECTOR switch to 1.
3. Connect a voltmeter between EXTERNAL TEST POINT 4-26 and ground and monitor the +6-volt d-c level.
4. Adjust the voltage level to +6.0-volt dc using trimpot R24 located on the etched board being tested.
5. Set the LOAD switch to FULL and monitor voltage change. The voltage should not drop more than 0.10-volt dc.
6. Return LOAD switch to HALF.
7. Set LEVEL SELECTOR switch to 2 and monitor -6-volt d-c level.
8. Adjust the voltage level to -6-volt dc using the trimpot R32 located on the etched board being tested.
9. Set LOAD switch to FULL and monitor voltage change. The voltage should not drop more than 0.25-volt dc.
10. Return LOAD switch to HALF.
11. Set LEVEL SELECTOR switch to 3, to monitor +0.75-volt d-c level. (This level is not adjustable.) The reading should be +0.75±0.15-volt dc.
12. Set LOAD switch to FULL and monitor the voltage change. The voltage should not drop more than -0.25-volt dc from original value.
13. Return LOAD switch to HALF.

To test the +6-volt bridge, proceed as follows:

1. Connect a voltmeter between EXTERNAL TEST POINT 4-26 and ground so as to obtain a negative reading.
2. Set BRIDGE switch to ON.
3. Set LEVEL SELECTOR switch to 6 (+6-volt bridge) and monitor voltage level. The voltage should be -22±2-volt dc.

-12-, +75-Volt Power Supply Board

The -12-, +75-volt power supply board also contains the +75-volt bridge rectifier. Perform all tests in the order listed.

To check for correct circuit continuity for each voltage level, proceed as follows:

1. Perform preparation procedure for Power Supply Circuit Board Tests, page 55.
2. Plug etched board into -12, +75 VOLT POWER SUPPLY test jack at top of tester.
3. Set LEVEL SELECTOR switch to 4. This sets up the correct circuit for the -12-volt level.
4. Connect a multimeter between EXTERNAL TEST POINT 4-26 and ground. The reading should be no less than 40 ohms.
5. Reverse multimeter connections. The reading should be no less than 40 ohms.
6. Set LEVEL SELECTOR switch to 5. This sets up the correct circuit for the +75-volt level.
7. Repeat procedures 4 and 5. The reading should be no less than 1000 ohms.

To test each voltage level, proceed as follows:

1. Set POWER switch to ON.
2. Set LEVEL SELECTOR switch to 4.
3. Connect a voltmeter between EXTERNAL TEST POINT 4-26 and ground to obtain a negative reading; monitor the -12-volt d-c voltage level.
4. Adjust the voltage level to -12-volt dc using the trimpot R27 located on the etched board being tested.
5. Place the LOAD switch at FULL and monitor the voltage level change. The voltage should drop no more than 0.20-volt dc.
6. Return LOAD switch to HALF.
7. Set LEVEL SELECTOR switch to 5 to monitor +75-volt d-c level.
8. Connect a voltmeter between EXTERNAL TEST POINT 4-26, and ground, so as to obtain a positive reading and monitor the +75-volt d-c voltage level.
9. Adjust the voltage level to +75 volts using trimpot R23 located on panel assembly being tested.
10. Set the LOAD switch to FULL and monitor the voltage level change. The voltage should drop no more than +1.25-volt dc.
11. Return LOAD switch to HALF.

To test the +75-volt bridge, proceed as follows:

1. Connect a voltmeter to EXTERNAL TEST POINT 4-26 and ground so as to obtain a negative reading.
2. Set BRIDGE switch to ON.
3. Set LEVEL SELECTOR switch to 5 and monitor voltage level. The voltage level should be -81±5-volt dc.

-18, -100, -3 Volt Power Supply Board

The requirements for this etched board are the same as those specified for other circuit boards except that continuity checks of the -3- and -100-volt levels are not performed.

To check the circuit continuity of the -18-volt level, proceed as follows:

1. Perform preparation procedure for Power Supply Circuit Board Tests, page 55.
2. Plug etched board into -18, -100, -3 VOLT POWER SUPPLY test jack at top of tester.
3. Set LEVEL SELECTOR switch to 6. This sets up the correct circuit for the -18-volt level.
4. Connect a multimeter between EXTERNAL TEST POINT 4-26 and ground. The reading should be no less than 100 ohms.
5. Reverse multimeter connections. The readings should be no less than 100 ohms.

To test each voltage level, proceed as follows:

1. Set POWER switch to ON.
2. Set LEVEL SELECTOR switch to 6.
3. Connect a voltmeter between EXTERNAL TEST POINT 4-26 and ground and monitor the -18-volt level.
4. Adjust the voltage level to -18-volt dc using trimpot R15 on the panel assembly being tested.
5. Set LOAD switch to FULL and monitor the voltage level change. The voltage should not drop more than 0.25-volt dc.
6. Return LOAD switch to HALF.
7. Set LEVEL SELECTOR switch to 7.
8. Monitor voltage level at EXTERNAL TEST POINT 4-26 and ground. The voltage should be -3±0.5-volt dc.
9. Set LEVEL SELECTOR switch to 8.
10. Monitor voltage at EXTERNAL TEST POINT 4-26. This level is not adjustable and should read -100±15-volt dc. No voltage stability test is performed on this panel.

Relay Network Control Board

The power supply relay control network etched board contains the relay control bridge network and the -12- and -6-volt d-c power supply bridge rectifiers. The tests performed on the panel consist of monitoring the voltage levels of the relay control networks and the two bridge rectifiers.

To perform the relay control bridge test, proceed as follows:

1. Perform preparation procedure for Power Supply Circuit Board Tests, page 55.
2. Plug etched board into RELAY CONTROL NETWORK P.S. test jack.
3. Set POWER switch to ON.
4. Set LEVEL SELECTOR switch to 6.
5. Connect the positive terminal of a voltmeter to EXTERNAL TEST POINT 4-26 and the negative terminal to EXTERNAL TEST POINT 4-28. The voltage should read +107±10-volt dc.
6. Set RELAY CONTROL switch to 2. The voltage should read 112±10-volt dc.
7. Set RELAY CONTROL switch to 3. The voltage should read 112±10-volt dc.
8. Set the RELAY CONTROL switch to 4. The voltage should read 160± 15-volt dc.
9. Set the RELAY CONTROL switch to 5. The voltage should read 107± 10-volt dc.

To test the -12- and -6-volt bridge rectifiers, proceed as follows:

1. Set LEVEL SELECTOR switch to 1 (-12-volt bridge).
2. Set BRIDGE switch to ON.
3. Connect a voltmeter between EXTERNAL TEST POINT 4-26 and ground so as to obtain a negative reading. The voltage should read -33± 2-volt dc.
4. Set LEVEL SELECTOR switch to 2 (-6-volt bridge).
5. Repeat procedures 2 and 3. The voltage should read -22± 2-volt dc.

Network, Power Supply Board

The power supply network board contains the -18-volt bridge rectifier for the -18-volt power supply and the filters for the -12-, -6-, and +75-volt power supplies. Tests performed on the circuit board consist of bridge and filter output voltage tests.

To check forward and reverse resistance of each diode in the bridge rectifier, proceed as follows:

1. Perform preparation procedure for Power Supply Circuit Board Tests, page 55.
2. Plug etched board into NETWORK, POWER SUPPLY test jack at top of tester.
3. Connect the positive terminal of a multimeter to the anode and the negative terminal to the cathode (stud) of each diode individually.

4. Each reading of the forward resistance should be less than 50 ohms on the "X10" scale.

5. Reverse the multimeter connections. Each reading of the reverse resistance should be more than 500,000 ohms on the "X100,000" scale.

To test the voltage of the -18-volt bridge, proceed as follows:

1. Set POWER switch to ON.
2. Connect a voltmeter between EXTERNAL TEST POINT 4-26 and ground so as to obtain a negative reading.
3. Set BRIDGE switch to ON.
4. Set LEVEL SELECTOR switch to 3 (-18-volt bridge) and monitor voltage level. The voltage should be -33± 2-volt dc.

To test the voltage output and the ripple of the -12-, -6-, and +75-volt filters, proceed as follows:

1. Set LEVEL SELECTOR switch to 1.
2. Set BRIDGE switch to OFF.
3. Set RELAY CONTROL switch to 2. This determines the voltage input to the -12-volt filter.
4. Connect a voltmeter between EXTERNAL TEST POINT 4-27 and ground and monitor the voltage level.
5. The voltage should be -22± 2-volt dc.
6. Connect an oscilloscope between EXTERNAL TEST POINT 4-26 and ground to monitor the voltage ripple.
7. The voltage ripple should be no greater than 750 millivolts peak-to-peak.
8. Set RELAY CONTROL switch to 3. This determines the voltage input to the -6-volt filter.
9. Repeat procedure 4. The voltage should be -22± 2-volt dc.
10. Repeat procedure 6. The voltage ripple should be no more than 500 millivolts peak-to-peak.
11. Set RELAY CONTROL switch to 4. This determines the voltage input to the +75-volt filter.
12. Repeat procedure 4. The voltage should be -33± 2-volt dc.
13. Repeat procedure 6. The voltage ripple should be no more than 7 volts peak-to-peak.

Filter Network, Power Supply Board

The filter network board contains the filters for the -100-, +6-, and -18-volt power supplies. The requirements for checking the board are that the voltage output and ripple for each filter meet the values specified when monitored with the voltmeter and oscilloscope at the designated test points.

To test the voltage output and ripple of the -100-, +6-, and -18-volt filters, proceed as follows:

1. Perform preparation procedure for Power Supply Circuit Board Tests, page 55.
2. Plug etched board into NETWORK FILTER TEST jack at top of tester. Place POWER SWITCH at ON.
3. Set LEVEL SELECTOR switch to 1.
4. Set RELAY CONTROL switch to 2. This determines the voltage input to the -100-volt filter.
5. Connect a voltmeter between EXTERNAL TEST POINT 4-27 and ground to monitor the output voltage.
6. The voltage should be -22± 4-volt dc.
7. Connect an oscilloscope between EXTERNAL TEST POINT 4-26 and ground to monitor the voltage ripple.
8. The voltage ripple should be no more than 4 volts peak-to-peak.
9. Set RELAY CONTROL switch to 3. This determines voltage input to +6-volt filter.
10. Repeat procedure 5. The voltage should be -24± 4-volt dc.
11. Repeat procedure 7. The voltage ripple should be no more than 1.5 volts peak-to-peak.
12. Set RELAY CONTROL switch to 4. This determines the voltage input to the -18-volt filter.
13. Repeat procedure 5. The voltage should be -35± 5-volt dc.
14. Repeat procedure 7. The voltage ripple should be no more than 1.5 volts peak-to-peak.

POWER SUPPLY ELEMENTS NOT ON CIRCUIT BOARDS

Power supply elements not on circuit boards include the power transformer T1, the secondaries which deliver a-c voltages for conversion to the various d-c power levels, control relays which provide the proper sequencing of computer control voltages, and filter chokes which form a part of the filter circuits in the d-c power supplies. In addition, the power control circuits contain two manually operated interlock switches which are located on the power supply chassis. The memory interlock switch (S2) controls the power to the memory solenoid and motor and the power interlock switch (S1) controls power to transformer T1. For control relay checkout purposes, portions of the control circuits, in which the relays to be checked are located, may be isolated by opening first one and then the other interlock switch. (See figure 13.) Continuity checks of the isolated circuit will then pinpoint the malfunction. Checkout procedures for the power transformer require that secondary voltages be monitored at test points and meet the voltage values specified. The chokes are checked for continuity only.

Filter Choke Checkout Procedures

The +6-, -6-, -100-, -18-, and -12-volt filter chokes are checked for continuity at computer power input jack, J34. To perform the continuity check, remove the power supply chassis from the frame of the computer. With computer power off, connect the ohmmeter between the following pins of jack J34 and measure the resistance. The resistance readings for each choke should be as follows:

Measure Between Pin No. (J34)	Read Maximum Resistance
10 and 11 (-100-volt choke)	12 ohms
12 and 13 (+6-volt choke)	2 ohms
4 and 5 (-6-volt choke)	3 ohms
8 and 9 (-12-volt choke)	3 ohms
6 and 7 (-18-volt choke)	3 ohms

Transformer T1 Secondary Level Checkout Procedures

To check the required a-c voltage outputs of the transformer secondaries for conversion to +6-, -6-, +75-, -12-, -100-, and -18-volt dc, proceed as follows:

Note

A variation of 115-volt input to the primary will cause a corresponding variation in the secondaries. If possible the input should be adjusted to 115 volts to meet the voltages and tolerances of the secondaries as specified in the following steps.

1. Plug assembled power supply chassis into computer power jacks J29 and J34.
2. Place power interlock switch in the closed position.
3. Apply 115-volt source voltage to power supply.
4. Connect the voltmeter between transformer pins 9 and 10 (secondary ac for conversion to +6-volt dc).
5. The voltage should be 16.5±0.4-volt rms.
6. Connect the voltmeter between transformer pins 7 and 8 (secondary ac for conversion to -6-volt dc).
7. The voltage should be 19.7±0.4-volt rms.
8. Connect the voltmeter between pins 13 and 14 (secondary ac for conversion to +75-volt dc).

9. The voltage should be 118± 2-volt rms.

10. Connect the voltmeter between pins 5 and 6 (secondary ac for conversion to -12-volt dc).

11. The voltage should be 27. 1± 0. 6-volt rms.

12. Connect the voltmeter between pins 11 and 12 (secondary ac for conversion to -100-volt dc).

13. The voltage should be 114± 2-volt rms.

14. Connect the voltmeter between pins 3 and 4 (secondary ac for conversion to -18-volt dc).

15. The voltage should be 33± 0. 7-volt rms.

SIGNAL CIRCUITS

The following paragraphs provide instructions for testing the individual computer circuit boards using the component tester. Each type of circuit board requires a unique preparation procedure which must be performed before individual tests are performed on the circuit board. Remember that the POWER switch must always be set to OFF before a circuit board is inserted or removed from the test receptacle.

LOGIC CIRCUIT BOARD

The 1-LOGIC section of the component tester contains the necessary controls for checking the operation of the computer logic network circuits. All switches associated with logic network tests, other than the MASTER SELECTOR and POWER switches, are located together on the component tester panel. The position of other switches on the panel does not affect this test procedure.

Preparation

The following preparation should be completed before beginning the test procedure:

1. Set MASTER SELECTOR switch to 1.
2. Set POWER switch to ON.
3. Monitor the -12-volt d-c voltage level at INTERNAL TEST POINT 28 with a voltmeter. Tolerances are shown in table 1, page 43.
4. Set POWER switch to OFF.
5. Plug etched board into LOGIC test jack at top of tester.
6. Set POWER switch to ON.

Forward Current Check

The forward current check measures the forward resistance of the logic diodes by applying -12-volt dc across the diode and associated 16-kilohm resistor. To perform the forward current test, proceed as follows:

Table 8. Gate Selector Positions

DIODE BUTTONS		1	2	3	4	5	6	7	8	9	10	11	12	13	14
	D1	P1 14 CR1	P1 6 CR10	P1 22 CR17	P1 12 CR24	P2 22 CR29	P2 25 CR34	P2 7 CR42	P2 8 CR44	P2 30 CR48	P2 32 CR53	P2 33 CR56	P2 16 CR60	P2 35 CR62	P2 37 CR65
	D2	P1 2 CR2	P1 19 CR11	P1 10 CR18	P2 20 CR25	P2 2 CR30	P2 5 CR35	P2 28 CR43	P2 29 CR45	P2 31 CR49	P2 13 CR54	P2 15 CR57	P2 17 CR61	P2 36 CR63	P2 19 CR66
	D3	P1 15 CR3	P1 7 CR12	P1 23 CR19	P1 13 CR26	P2 23 CR31	P2 26 CR36		P2 9 CR46	P2 11 CR50	P2 14 CR55	P2 34 CR58 CR59*		P2 18 CR64	
	D4	P1 3 CR4	P1 20 CR13	P1 11 CR20	P2 21 CR27	P2 3 CR32	P2 27 CR37 CR39*		P2 10 CR47	P2 12 CR51 CR52*					
	D5	P1 16 CR5	P1 8 CR14	P1 24 CR21	P2 1 CR28	P2 24 CR33	P2 6 CR38 CR41*								
	D6	P1 4 CR6	P1 21 CR15	P1 25 CR22 CR23*											
	D7	P1 17 CR7	P1 9 CR16												
	D8	P1 5 CR8													
	D9	P1 18 CR9													

Note

Numbers within table squares are plug, pin, and diode numbers.
Vertical column of numbers is grouped to form complete diode gates.
*Where 2 diode numbers are listed, only 1 connection is brought to the connector, requiring that they be tested in parallel.

1. Set TEST SELECTOR switch to 1. This sets up the correct anode bias and metering circuit.

2. Set left GATE SELECTOR switch to desired logic gate position. (Refer to table 8 for logic gate locations.)

Note

The left-hand GATE SELECTOR switch must be at position 8 before the right-hand GATE SELECTOR switch will electrically function for gate positions 8 through 14.

3. Depress each of the DIODE buttons 1 through 9. The anode of the diode is grounded when the proper switch is actuated and a reading is indicated on the panel milliammeter. Forward current for single diodes should be between 0.6 and 1.0 milliamperes. Forward current for diodes in parallel (table 8 should be between 1.3 and 1.7 milliamperes.

4. Repeat procedure 3 with GATE SELECTOR switches at positions 2 through 14. Readings will be obtained only where a listing is found in table 8. For example, with GATE SELECTOR switch at 2, readings will be obtained when DIODE buttons 1 through 7 are actuated. Buttons 8 and 9 will indicate as open circuits.

Reverse Current Check

In the reverse current check, the back resistance of each diode is measured by placing -12-volt dc on the anodes and switching in a microammeter at the 16-kilohm cathode resistor. To perform the reverse current check, proceed as follows:

1. Set TEST SELECTOR switch to 2.
2. Set GATE SELECTOR to desired gate position.
3. Depress DIODE buttons 1 through 9 individually and read reverse current on the panel microammeter. Reverse current of single diodes should be no more than 10 microamperes. Reverse current of diodes in parallel should be no more than 18 microamperes. Readings will be obtained only where a listing is found in table 8 and open circuits should appear only at positions without diodes.

Series "Or" Diode Forward Current Check

The series "or" diode forward current checks a series diode without an internal cathode resistor for forward resistance. The method of checking is

similar to that of other diodes except that the 16-kilohm resistor is supplied within the test circuitry. To perform the test, proceed as follows:

1. Set TEST SELECTOR switch to 3. This sets up the necessary circuits for the single "or" diode.
2. Depress the "or" button and observe reading on panel milliammeter. Reading should be between 0.6 and 1.0 milliamperes.

Series "Or" Diode Reverse Current Check

The series "or" diode reverse current check is similar to the forward current check except that the current is measured in an opposite direction through the diode. To perform the test, proceed as follows:

1. Set TEST SELECTOR switch to 4. This sets up the necessary circuits for the single "or" diode.
2. Depress "or" diode button and observe reading on panel microammeter. Reading should be no more than 10 microamperes.

COMPUTER NETWORK CIRCUIT BOARD

The 3-NETWORK section of the component tester provides the controls necessary to check the various circuits of the computer network etched board. In addition, the power ON-OFF, MASTER SELECTOR and BRIDGE switches, panel connectors, and test points are utilized during these tests. Diodes are checked for forward and reverse current characteristics and the neon amplifier circuit is checked along with the seven input diodes. The necessary voltage required to give an approximate 1-volt level output is applied to each of the padder resistors and monitored on the panel meter.

Preparation

Before performing the various tests, the following preparation should be made:

1. Set MASTER SELECTOR switch to 3.
2. Set POWER switch to ON.
3. Set BRIDGE switch to ON (located in 4-POWER SUPPLY section)
4. Monitor +6-, -12-, and -18-volt d-c voltage levels at INTERNAL TEST POINTS shown in table 1. Tolerances should agree with those shown in table 1.
5. Set POWER switch to OFF.
6. Plug etched board into COMPUTER NETWORK test jack at top of tester.
7. Set POWER switch to ON.

Neon Amplifier Test

The neon amplifier circuit is tested along with the seven input diodes which drives the amplifier circuit and causes the neon indicator to light. NETWORK SEL II switch positions 1 through 7 apply voltage to diodes CR1 through CR7, respectively. To perform the check, proceed as follows:

1. Set TEST SEL switch to 1.
2. Set NETWORK SEL II switch to 1.
3. Depress NEON test button. The neon indicator should light while button is depressed.

Note

If the neon indicator does not light, the following voltage measurement procedure may be used to determine the condition of the circuit:

1. Connect a voltmeter between EXTERNAL TEST POINT 3-1 and ground so as to obtain a negative reading.
2. Depress the neon test button and monitor the voltage. The voltage should read more negative than -50-volt dc if the light is at fault and not the circuit.

4. Repeat procedure 2 for positions 2 through 7 of NETWORK SEL II switch. The neon indicator should light while button is depressed for each of the switch positions.
5. Upon completion of the test, return NETWORK SEL II to position 1.

Clamp Diode Forward Voltage Test

Each of the clamp diodes on the etched board is selected and voltage is applied to the cathodes. The forward voltage is monitored on the test set voltmeter. To perform the check, proceed as follows:

1. Set TEST SEL switch to 2.
2. Set NETWORK SEL I switch to 1.
3. Depress DIODE CLAMP test button and monitor voltage on test voltmeter. Voltage should be within the range of +0.7- to 0-volt dc.
4. Repeat procedure 3 for NETWORK SEL I switch positions 2 through 8. (Refer to table 9 for symbol of diodes checked at each position.)

Clamp Diode Reverse Voltage Test

In the reverse voltage check, the back resistance of each clamp diode is measured by applying a reverse voltage through the clamp resistor to the anodes. The voltage is monitored on the test set voltmeter. To perform the test, proceed as follows:

1. Set TEST SEL switch to 3.
2. Set NETWORK SEL I switch to 1.
3. Depress DIODE CLAMP test button and monitor voltage on test set voltmeter. Voltage should be within the range of +0.8- to +1.2-volt dc.
4. Repeat procedure 3 for NETWORK SEL I switch positions 2 through 8.

Table 9. Clamp Diodes Test

NETWORK SEL I Positions							
1	2	3	4	5	6	7	8
CR14	CR15	CR16	CR17	CR18	CR19	CR20	CR21 CR22 CR23

Input Diode Forward Current Test

Each of the input diodes on the etched board is selected and -12-volt dc is applied across the diode and a 16-kilohm resistor. The forward current is monitored on the test set milliammeter. To perform the test, proceed as follows:

1. Set TEST SEL switch to 4.
2. Set NETWORK SEL II switch to 1.
3. Depress DIODE 1 test button and monitor the current on test set milliammeter. The current should read within the range of 0.6 to 1.0 milliamperes.
4. Repeat procedure 3 for NETWORK SEL II switch positions 2 through 5. (Refer to table 10 for symbol of diodes checked at each position when DIODE 1 button is depressed.)
5. Set TEST SEL switch to 6.
6. Return NETWORK SEL II switch to position 1.
7. Depress DIODE 2 test button and monitor the current on the test set milliammeter. The current should read within the range of 0.6 to 1.0 milliamperes.
8. Repeat procedure 7 for NETWORK SEL II switch positions 2 through 6. (Refer to table 10 for symbol of diodes checked at each position when DIODE 2 button is depressed.)

Input Diode Reverse Current Test

In the reverse current check, the back resistance of each diode is measured by applying -12-volt dc on the anodes of each diode and switching in the test set microammeter at the 16-kilohm cathode resistor. To perform the check, proceed as follows:

1. Set TEST SEL switch to 5.
2. Set NETWORK SEL II switch to 1
3. Depress DIODE 1 test button and monitor the current on test set microammeter. The current should be less than 10 microamperes.
4. Repeat procedure 3 for NETWORK SEL II switch positions 2 through 5.
5. Set TEST SEL switch to 7.
6. Return NETWORK SEL II switch to position 1.
7. Depress DIODE 2 test button and monitor the current on test set microammeter. The current should be less than 10 microamperes.
8. Repeat procedure 7 for NETWORK SEL II switch positions 2 through 7.

Table 10. Individual Diodes Test

	NETWORK SEL II Positions					
DIODE Button	1	2	3	4	5	6
1	CR24	CR25	CR26	CR31	CR32	
2	CR27	CR28	CR29	CR30	CR13	CR12

Padder Resistor Test

The padder resistors are checked by adding sufficient resistance in series or parallel between the output and ground, or other test voltages. When PAD 1 or PAD 2 switch is depressed, a reading of 0.7- to 1.2-volt dc should register on the test set voltmeter. To check the padder resistor, proceed as follows:

1. Set TEST SEL switch to 8.
2. Set NETWORK SEL I switch to 1.
3. Set NETWORK SEL II switch to 1.
4. Depress PAD 1 test button and monitor the voltage on test set voltmeter.
5. Repeat procedure 4 for NETWORK SEL I switch positions 2 through 6. (Refer to table 11 for resistor symbols checked at each position when PAD 1 is depressed.)
6. Return NETWORK SEL I switch to position 1.
7. Depress PAD 2 test button and monitor the voltage on test set voltmeter.

8. Repeat procedure 7 for NETWORK SEL I switch positions 2 through 6. (Refer to table 11 for resistor symbols checked at each position when PAD 2 is depressed.

Table 11. Individual Resistors Test

	NETWORK SEL I Positions					
PAD Button	1	2	3	4	5	6
1	R19	R20	R21	R22	R23	R24
2	R26	R29	R27	R28	R2	R1 R31

READ SWITCHING NETWORK CIRCUIT BOARD

The 5-READ SWITCH section of the component tester provides the controls for completely checking the computer read switching network etched boards. The following tests may be performed: input diode forward and reverse current check, static testing, and dynamic testing.

Preparation

The following preparation should be completed before beginning the test procedure:

1. Set MASTER SELECTOR switch to 5.
2. Set POWER switch to ON.
3. Monitor +6-, -12-, -18-, and +0.75-volt d-c levels at test points indicated in table 1. Tolerances should agree with those presented in the table.
4. Set POWER switch to OFF.
5. Plug read switching network etched board into READ SWITCH test jack at top of tester.
6. Set BRIDGE switch to ON. (The bridge switch is located on the 4-POWER SUPPLY section of the component tester and controls the positive internal voltage levels.)

Input Diode Forward Current Test

To test the forward current of the input diodes, proceed as follows:

1. Set TEST SEL switch to 1.
2. Set SWITCH SELECTOR switch to desired diode position. (Position 1 for CR1, position 2 for CR2, and position 3 for CR3.)

3. Depress FOR-DIODE button and read the forward current on test set milliammeter. Forward current should be between 0.6 and 1.0 milliamperes (ignore residual reading).

4. Repeat procedures 1 through 3 for the remainder of the diodes on the board. If diodes do not come within specified tolerances, replace etched board.

Input Diode Reverse Current Test

To test the reverse current of the input diodes, proceed as follows:

1. Set TEST SEL switch to 2.
2. Set SWITCH SELECTOR switch to desired diode (position 1, 2, or 3).
3. Depress REV-DIODE button and read the reverse current on test set microammeter. Reverse current should be less than 10.0 microamperes.
4. Repeat procedures 1 through 3 for the remainder of diodes on the computer board. If readings fail to come within specified tolerances, replace etched board.

Driver Test (Static)

When making a static test, set the STAT-DYN switch to STAT to apply +0.75-volt dc and ground on each switch. Rotating the SWITCH SELECTOR from positions 1 through 8 and monitoring EXTERNAL TEST POINT 5-3 will give the drop across psuedo read head which is simulated with a 100-ohm resistor. To perform the test, proceed as follows:

1. Set TEST SEL switch to 3.
2. Monitor voltage between EXTERNAL TEST POINT 5-4 and ground with a vacuum-tube voltmeter, or equivalent.
3. Set SWITCH SELECTOR switch to 1 and monitor the voltage. Voltage should be between -2.2- and -3.8-volt dc.
4. Connect d-c voltmeter between EXTERNAL TEST POINT 5-3 and ground and monitor the voltage. Voltage should be less than 20.0 millivolts.
5. Repeat procedures 1 through 4 for each of the 8 positions of the SWITCH SELECTOR. If readings do not meet specified tolerances, the panel assembly should be replaced.

Dynamic Driver Test No. 1

The driver dynamic test is performed by placing an internal flip-flop input on each switch individually. Rotating the SWITCH SELECTOR from positions 1 through 8 and monitoring the test point with an oscilloscope will indicate the switch output waveform. To perform the test, proceed as follows:

1. Set TEST SELECTOR switch to 3.
2. Monitor EXTERNAL TEST POINT 5-4 with an oscilloscope.

5. Measure rise and fall times of the flip-flop circuits. The rise time should be less than 2 microseconds and the fall time should be less than 3 microseconds. (The pulsewidth is determined by the internal flip-flop.) The upper voltage level should be between ground potential and +0.75-volt dc, and the lower voltage level should be between 2.2- to 3.8-volt dc.

Dynamic Driver Test No. 2

This dynamic test is made by applying a 10-kilocycles, 100-millivolt a-c rms sine wave across each read head. One gate line is returned individually to +6 volts and monitored. The read head output is monitored at EXTERNAL TEST POINT 5-3, and the read switch output is monitored at EXTERNAL TEST POINT 5-2. To perform the test, proceed as follows:

1. Set TEST SEL switch to 4.
2. Place STAT-DYN switch to STAT.
3. Connect vacuum-tube voltmeter at EXTERNAL TEST POINT 5-3 and ground.
4. Adjust trimpot R2 located on the top tester panel until a reading of 100-millivolt a-c rms is read on the voltmeter.
5. Connect the vacuum-tube voltmeter at EXTERNAL TEST POINT 5-2 and ground and read voltage. Voltage should be 100±20-millivolt a-c rms. If the tolerance is not met, this level may be adjusted using the following trimpots associated with each switch.

Adjust Resistor (See figure 43.)	Switch Selector Position
R1	1
R5	2
R9	3
R13	4
R17	5
R21	6
R25	7
R29	8

6. Set SWITCH SELECTOR switch to position 2 through 8, and monitor voltage at each position. Voltage should be 100± 20-millivolt a-c rms at each position. If correct reading is not obtained by adjusting the resistor on the board, check to see that input voltage has not dropped. If input voltage is different than 100± 5-millivolt a-c rms, readjust using trimpot R2 on component tester panel.

READ AMPLIFIER CIRCUIT BOARD

The read amplifier etched boards are tested by the controls located on the 8-READ AMPL section of the computer component tester. Four tests are accomplished through the proper combination of controls located on the panel. The tests performed are: preamplifier bandwidth, static test, dynamic test, and load test.

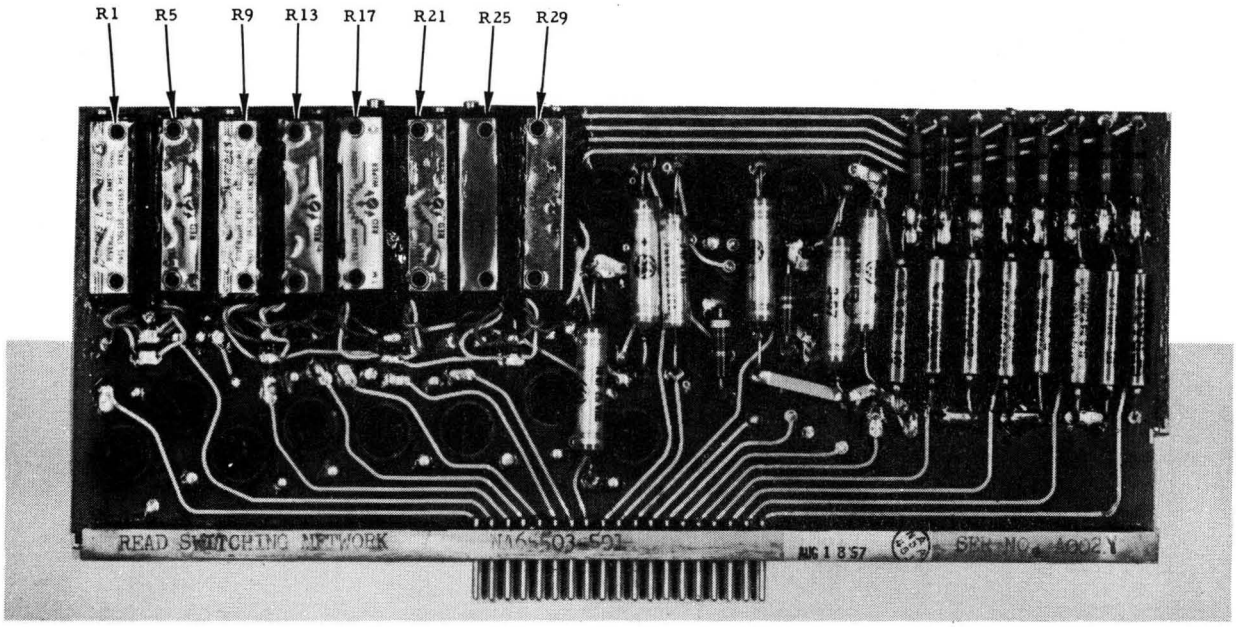


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Figure 43. Read Switching Network Adjustment Points

Preparation

The following preparation should be completed before beginning the test procedures:

1. Set MASTER SELECTOR switch to 8.
2. Set BRIDGE switch to ON (located in 4-POWER SUPPLY section of tester).
3. Set POWER switch to ON.
4. Monitor -6-, -18-, 6-, 75-, -200-, and -12-volt d-c voltage levels at INTERNAL TEST POINTS shown in table 1. Tolerances should agree with those shown in the table.
5. Set POWER switch to OFF.
6. Set LOAD switch to OUT.
7. Set OSC GAIN control fully counterclockwise.

8. Plug etched board into READ AMPLIFIER test jack at top of tester.
9. Set POWER switch to ON.

Preamplifier Bandwidth Test

The preamplifier bandwidth is tested by inserting the following frequencies into the read amplifier input: 600 cps, 10 kilocycles, and 200 kilocycles. The 2-volt peak-to-peak amplitudes are attentuated through a 10-kilohm resistor and a 500-ohm potentiometer to give a variable input of between 0 and 60 millivolts peak-to-peak. The oscillator outputs can be checked for input amplitude at EXTERNAL TEST POINT 8-4 (read amplifier oscillator input.) The preamplifier output is metered while each of these three bandwidth tests are made. The flip-flop output is monitored at EXTERNAL TEST POINT 8-6. To perform the bandwidth test, proceed as follows:

1. Set TEST SELECTOR switch to 1.
2. Connect an a-c voltmeter between EXTERNAL TEST POINT 8-5 and ground and adjust the OSC GAIN control until a reading of 3.0±0.1-millivolt a-c rms is achieved.
3. Connect the voltmeter leads between EXTERNAL TEST POINT 8-6 and ground and adjust the variable resistor (R5) on computer etched board until a reading of 300±5-millivolt a-c rms is achieved.
4. Set TEST SELECTOR switch to 2.
5. Reconnect the a-c voltmeter between EXTERNAL TEST POINT 8-5 and ground, and adjust the OSC GAIN control until a reading of 3.0±0.1-millivolt a-c rms is achieved.
6. Change voltmeter back to EXTERNAL TEST POINT 8-6 and read voltage. Voltage should be more than 211-millivolt a-c rms.
7. Set TEST SELECTOR switch to 3.
8. Reconnect the a-c voltmeter between EXTERNAL TEST POINT 8-5 and ground and adjust the OSC GAIN control until a reading of 3.0±0.1-millivolt a-c rms is achieved.
9. Change voltmeter lead back to EXTERNAL TEST POINT 8-6 and read voltage. Voltage should be more than 211-millivolt a-c rms.

Static Flip-Flop Test

With the TEST SELECTOR at 4, the computer panel flip-flop circuits may be statically set and reset by depressing either the 1 SET or 0 SET buttons. Either the 1 SET or 0 SET neon indicator should come on when the associated switch is depressed. To perform the static test, proceed as follows:

1. Set TEST SELECTOR switch to 4.
2. Depress the 1 SET and 0 SET buttons alternately. The neon lamps associated with each switch should light when the switch is depressed and remain on until the other button is depressed.

Dynamic Flip-Flop Test

To dynamically check the flip-flop circuit on the computer read amplifier panel assembly, a 157.0-kilocycle, 60-millivolt peak-to-peak signal is supplied to the read amplifier input. The flip-flop is triggered from the clock circuitry, which is directly connected to the read strobe line. The flip-flop may be tested with or without a load by placing the LOAD switch at IN with a load, or OUT without a load. To perform the dynamic flip-flop test, proceed as follows:

1. Set TEST SELECTOR switch to 5.
2. Connect an a-c voltmeter between EXTERNAL TEST POINT 8-5 and ground, and adjust OSC GAIN until 42.4± 1.0-millivolt a-c rms is achieved.
3. Connect an oscilloscope between EXTERNAL TEST POINT 8-7 and ground.
4. Measure the rise and fall times of the flip-flop circuit. The rise time should be less than 2 microseconds, and the fall time should be less than 3 microseconds.
5. Connect an oscilloscope to EXTERNAL TEST POINT 8-7 and ground, and monitor the output of the flip-flop for the true and false voltage levels. The output voltage should be -9±1 volts for the true state and 0± 1 volt for the false state when the LOAD switch is at OUT. When LOAD switch is at IN, the waveform will drop -12± 1-volt dc.

Completion of Tests

To complete the test, perform the following steps:

1. Set LOAD switch to OUT
2. Set OSC GAIN control to full counterclockwise.
3. Return TEST SELECTOR switch to 1.
4. Set POWER switch to OFF.
5. Remove etched board from tester.

WRITE SWITCHING CIRCUIT BOARD

The computer write switching etched boards are checked by the controls located on the 9-WRITE SWITCH section of the component tester. The various tests are selected by the TEST SELECTOR switch. The three selector switches located across the top of the 9-WRITE SWITCH section are used conjunctively for selecting individual write head diodes. The switches are connected to provide 22 individual selections. The middle selector switch does not become activated until the first switch is set to position 8. The third switch does not become activated until the middle switch is set to position 15. Therefore, the switch on the left, and the switch in the middle must be set to positions 8 and 15 respectively before positions 16 through 22 are activated. The SWITCH SELECTOR is used in conjunction with positions 3 through 6 on the TEST SELECTOR switch. Each input diode is individually selected according to the corresponding switch positions.

Preparation

Before beginning the test procedure, the following preparation should be performed:

1. Set MASTER SELECTOR switch to 9.
2. Set POWER switch to ON.
3. Monitor -18-, -3-, and -12-volt d-c voltage levels at INTERNAL TEST POINTS shown in table 1. Tolerances should agree with those shown in the table.
4. Set POWER switch to OFF.
5. Set all selector switches fully counterclockwise.
6. Plug etched board into WRITE SWITCH test jack at top of tester.
7. Set POWER switch to ON.

Write Diode Forward and Reverse Current Test

When performing a forward and reverse current check on the write head diodes, a 16-kilohm resistor is connected to all cathodes to keep the reading consistent. In the forward test, the anodes are grounded by depressing the DIODE-FOR button. The cathode resistor is connected to the panel milliammeter through the DIODE SELECTOR switch. As the DIODE SELECTOR switch is rotated, the FOR button is depressed and a forward current reading is obtained for the selected diode. In the reverse current check, the opposite effect is attained. The anode is connected to -12-volt dc by depressing the REV button; the cathode is connected to the test panel microammeter; and by depressing the REV button and rotating the DIODE SELECTOR through all its positions, the individual reverse current readings are obtained. To perform the forward and reverse current test, proceed as follows:

1. Set TEST SELECTOR switch to 1.
2. Depress FOR button and read forward diode current on test set milliammeter for each position of the DIODE SELECTOR switch. Forward diode current should be between 0.6 and 1.0 milliamperes.
3. Set TEST SELECTOR switch to 2.
4. Depress REV button and read reverse diode current on test set microammeter for each position of the DIODE SELECTOR switch except positions 8 through 10 where no reading will be obtained. Reverse diode current should be less than 10 microamperes.

Common Diode Forward, and Switch Diode Reverse Current Test

When the TEST SELECTOR is at 3, the eight common diodes are checked for forward current and the individual switch diode is checked in the reverse direction. As the SWITCH SELECTOR is rotated, -12 volts is placed through

a 3.9-kilohm resistor to the anodes of each switch diode. At the same time, a ground is connected to pin 14, the common point of the eight input diodes. As the SWITCH SELECTOR is rotated, EXTERNAL TEST POINTS 9-12 (forward current) and 9-11 (reverse current) are monitored. To perform the test, proceed as follows:

1. Set TEST SELECTOR switch to 3.
2. Connect a voltmeter between EXTERNAL TEST POINT 9-12 ground, and for the forward current and between EXTERNAL TEST POINT 9-11 and ground for reverse current.
3. Rotate SWITCH SELECTOR to each position and read voltages for the forward and reverse current. Voltmeter at test point 9-12 should read -18-volt dc, and the voltmeter at test point 9-11 should read -12-volt dc.

Switch Diode Forward, and Common Diode Reverse Current Test

When the TEST SELECTOR switch is at position 4, -12-volt dc is applied through a 3.9-kilohm resistor in series with the commonly connected diodes. The individual switch diode anodes are grounded individually when the SWITCH SELECTOR is rotated. The various voltages are monitored at EXTERNAL TEST POINTS 9-12 and 9-10. To perform the test, proceed as follows:

1. Set TEST SELECTOR switch to 4.
2. Connect a voltmeter either between EXTERNAL TEST POINT 9-12 and ground for the forward current readings, or between EXTERNAL TEST POINT 9-10 and ground for the common diode reverse current reading.
3. Rotate SWITCH SELECTOR to each position and read voltage on monitoring meter. The voltage at test point 9-12 should be -18-volt dc, and the voltage at test point 9-10 should be -12-volt dc.

Static Test

The static test checks the write switch transistors for saturation voltage. All inputs to the switches are open and as the SWITCH SELECTOR is rotated, the outputs are read on a monitoring meter. To perform the test, proceed as follows:

1. Set TEST SELECTOR switch to 5.
2. Connect voltmeter between EXTERNAL TEST POINT 9-12 and INTERNAL TEST POINT 26.
3. Rotate SWITCH SELECTOR to each position and monitor the voltage. The voltage should be no more than 0.75-volt dc.

Dynamic Test

When the TEST SELECTOR switch is at 6, a flip-flop is switched to the write switch input diodes. All the remaining diodes are grounded except the common input which goes to 0.3 volt through a 3.9-kilohm resistor. When the SWITCH SELECTOR is rotated through positions 1 to 8, the output is monitored on an oscilloscope for rise and fall time. To perform the test, proceed as follows:

1. Set TEST SELECTOR switch to 6.
2. Using an oscilloscope, monitor EXTERNAL TEST POINT 9-12.
3. Adjust the test oscilloscope as follows:

   Set SQUARE WAVE CALIBRATOR switch to 100V.
   Set vertical sensitivity for full deflection.
   Set TIME/DIV. switch to 1 USEC.
   Adjust ground level on screen until centered.

4. Place an acetate template (conforming to dimensions of figure 44) over the oscilloscope screen and adjust it as indicated in figure 44. The rise time should be less than 1 microsecond from point A to approximately 65 percent of the pulse magnitude. The fall time should be less than 0.5 microsecond from point B to ground level.

Completion of Tests

To complete the tests, perform the following:

1. Return TEST SELECTOR switch to 1.
2. Return SWITCH SELECTOR switch to 1.
3. Set POWER switch to OFF.
4. Remove write switching network panel assembly from tester.

WRITE AMPLIFIER CIRCUIT BOARD

The 10-WRITE AMPL section of the component tester provides the necessary controls for monitoring the inputs and switching the outputs of the three flip-flops on each computer write amplifier panel to a load and a neon indicator for test purposes. The flip-flops are tested either statically or dynamically by the proper selection of the test switch.

Preparation

The following preparation should be completed before beginning the test procedures:

1. Set MASTER SELECTOR switch to 10.
2. Set POWER switch to ON.

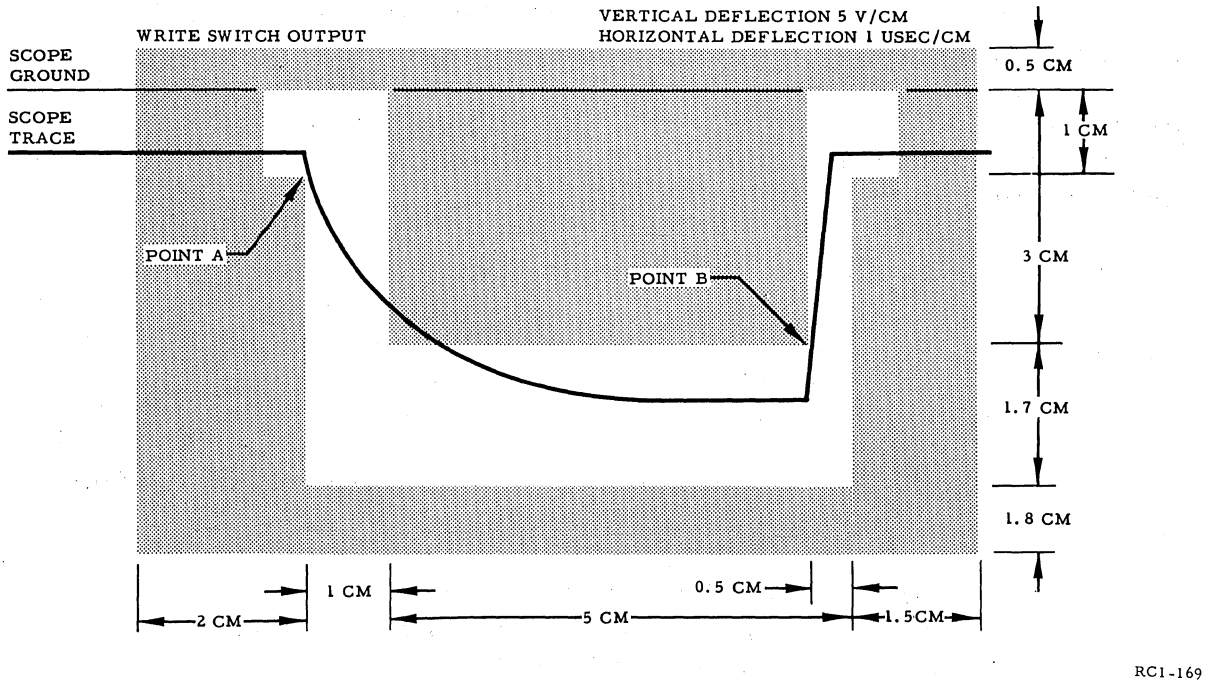

Figure 44. Oscilloscope Template for Write Switch Checkout

3. Set BRIDGE switch to ON.
4. Monitor +6-, -12-, -18-, -200-, and +75-volt d-c voltage levels at INTERNAL TEST POINTS shown in table 1. Tolerances should agree with those shown in the table.
5. Set POWER switch to OFF.
6. Plug etched board into WRITE AMPLIFIER test jack at top of tester.
7. Set POWER switch to ON.

Static Test

To perform the static test of a computer write amplifier board, proceed as follows:

1. Set STAT-DYN switch to STAT.
2. Set FF OUTPUT SELECTOR switch to 1.
3. Connect a voltmeter between EXTERNAL TEST POINT 10-25 and ground.
4. Depress the 1-SET switch. The neon indicator should light and the voltmeter should indicate between -3.3- and -4.1-volt dc.
5. Depress the 0-SET switch. The neon indicator should go out and the voltmeter should indicate +0.4-volt dc.

6. Reconnect voltmeter between EXTERNAL TEST POINT 10-24 and ground.

7. Depress 1-SET switch. The neon indicator should light and the voltmeter should indicate 0.4-volt dc.

8. Depress 0-SET switch. The neon indicator should go out and the voltmeter should indicate between -3.3- and -4.1-volt dc.

9. Repeat procedures 3 through 8 for positions 2 and 3 of FF OUTPUT SELECTOR switch.

Dynamic Test

Because the voltage levels have been checked statically, only the rise and fall times are checked dynamically. Before performing this test, the oscilloscope used must be calibrated. To perform the tests, proceed as follows:

1. Connect oscilloscope signal input to EXTERNAL TEST POINT 10-25.
2. Adjust the test oscilloscope as follows:

   Set vertical sensitivity for full deflection.
   Set SQUARE WAVE CALIBRATOR switch to 2V.
   Set TIME/DIV. switch to 1 USEC.
   Set MULTIPLIER to 2.

3. Set STAT-DYN switch to DYN.
4. Measure rise and fall times of the flip-flop waveforms. The rise and fall time shall be no more than 1.0 centimeter. (Two microseconds measured from the 10-percent point to the 90-percent point of the wave.)
5. Repeat procedure 4 for all three positions of FF OUTPUT SELECTOR switch. If tolerances are not met, check the flip-flop inputs to write amplifier circuits. These inputs, along with associated tolerances, are listed in table 1. Tolerances should agree with those shown in the table.

FLIP-FLOP CIRCUIT BOARD

The 11-FLIP-FLOP section of the component tester contains the controls for performing the following tests on the computer flip-flop circuit boards: static test, dynamic test, and padder resistor tests.

Preparation

The following preparation should be completed before the test procedure:

1. Set MASTER SELECTOR switch to 11.
2. Set POWER switch to ON.

3. Monitor +75-, -200-, -6-, +6-, -12-, -18-, -100-, and -3-volt d-c levels at INTERNAL TEST POINTS shown in table 1. Tolerances should agree with those shown in the table.

4. Set POWER switch to OFF.

5. Plug panel assembly into FLIP-FLOP test jack at top of tester.

6. Set POWER switch to ON.

Static Test

To make a static test of the computer flip-flop circuits, the clock cutoff bias is supplied -18-volt dc. Individual flip-flops are selected by the FF & PAD SELECTOR switch. When the 1-SET microswitch is depressed, +7-volt dc is placed on the selected flip-flop set-reset line, and the flip-flop is set. The opposite effect is accomplished when the 0-SET microswitch is depressed; a voltage of -200-volt dc is applied to the set-reset line and the selected flip-flop is reset. To perform the static test, proceed as follows:

1. Set STA-DYN switch to STA.

2. Set FF & PAD SELECTOR switch to desired flip-flop on computer panel assembly. (Position numbers coincide with flip-flops on panel assemblies.)

3. Connect voltmeter between EXTERNAL TEST POINT 11-37 and ground.

4. Set LOAD switch to OUT.

5. Depress 1-SET switch. The 1-SET indicator should light, the 0-SET indicator should not light, and the voltmeter should indicate between -11.95- and -12.0-volt dc. (No load test is performed.)

6. Depress 0-SET switch. The 0-SET indicator should light, the 1-SET indicator should go out, and the voltmeter should indicate a minimum of 0.4-volt dc (no load condition.)

7. Set LOAD switch to IN.

8. Depress 0-SET switch. The 0-SET indicator should light, the 1-SET indicator should go out, and the voltmeter should indicate a maximum of 0.8-volt dc.

9. Connect voltmeter between EXTERNAL TEST POINT 11-38 and ground.

10. Set LOAD switch to OUT.

11. Depress 1-SET switch. The 1-SET indicator should light, the 0-SET indicator should not light, and the voltmeter should indicate a minimum of 0.4-volt dc.

12. Depress 0-SET switch. The 0-SET indicator should light, the 1-SET indicator should go out, and the voltmeter should indicate between -11.95- and -12.0-volt dc. No load test is performed on the -11.95-volt level.

13. Set LOAD switch to IN.

14. Depress 1-SET switch. The 1-SET indicator should light, the 0-SET indicator should not light, and the voltmeter should indicate a maximum of 0.8-volt dc.

15. Return LOAD switch to OUT

Dynamic Test

The dynamic test consists of monitoring each flip-flop with an oscilloscope and measuring the rise and fall times. When the STAT-DYN switch is at DYN, a 175-kilocycle sine wave is placed at the clock input which causes all four panel assembly flip-flops to operate, but only the set of outputs coinciding with the position selected will appear at EXTERNAL TEST POINTS 11-37 and 11-38. These outputs are checked individually with an oscilloscope by the proper selection of the FF & PAD SELECTOR switch and output jacks. The outputs may be monitored with or without a 150-ohm load by setting the LOAD switch to IN or OUT When the switch is at IN a 150-ohm resistor is placed between each flip-flop output and -12 volts to produce an 80-milliampere load on each side of the test flip-flops. The following test points are provided for monitoring the flip-flop inputs:

EXTERNAL TEST POINT	Input Observed
11-29	1-in of FF-1
11-30	0-in of FF-1
11-31	1-in of FF-2
11-32	0-in of FF-2
11-33	1-in of FF-3
11-34	0-in of FF-3
11-35	1-in of FF-4
11-36	0-in of FF-4

To perform the dynamic test, proceed as follows:

1. Set STAT-DYN switch to DYN.
2. Set FF & PAD SELECTOR switch to 1.
3. Connect an oscilloscope to either EXTERNAL TEST POINT 11-37 and ground to monitor the unprimed output or between EXTERNAL TEST POINT 11-38 and ground to monitor the primed output.
4. Adjust oscilloscope as follows:

Set vertical sensitivity for full deflection.
Set SQUARE WAVE CALIBRATOR switch to 50V.
Set TIME/DIV. switch to 2 USEC.

5. Measure rise and fall time of both the primed and unprimed outputs. Voltage rise time should be 2 microseconds maximum, voltage fall time should be 3 microseconds maximum as read between the 10- to 90-percent levels. If the waveform is not present, adjust CLOCK AMPLITUDE until the flip-flop triggers. If the waveform is present, adjust CLOCK AMPLITUDE for minimum signal to trigger the flip-flop.

6. Connect oscilloscope to INTERNAL TEST POINT 17 and monitor amplitude of the clock pulse. Amplitude should be between -3- and -5-volt dc.

7. Repeat procedures 3 through 6 for positions 2 through 4 on the FF & PAD SELECTOR switch.

Padder Resistor Test

Positions 5 and 6 on the FF & PAD SELECTOR switch are used for checking the two padder resistors on the computer flip-flop panel assembly. This is accomplished by adding sufficient resistance in series with the output to ground. When the PAD switch is depressed, a reading of 1 volt will register on the panel voltmeter. Because the pads are connected to -12-volt dc, a 91-ohm resistor and a 240-ohm resistor are used for pads 1 kilohm and 2.7 kilohms, respectively. To check the padder resistors, proceed as follows:

1. Set FF & PAD SELECTOR switch to either 5 for the 1-kilohm pad, or 6 for the 2.7-kilohm pad.

2. Depress PAD switch and read voltage on panel test meter. Voltage should be 0.8- to 1.1-volt dc.

CLOCK POWER AMPLIFIER NO. 1 CIRCUIT BOARD

Static and dynamic tests are performed on clock power amplifier No. 1. Static operation of the transistors on board No. 1 is checked prior to the dynamic test by applying simulated voltages of the proper value from the tester or an external source to the bases and by monitoring the voltage to determine collector stability at the output.

Note

For pin number and test point locations on clock board No. 1, refer to the amplifier clock No. 1 schematic in the appendixes.

A dynamic test is performed on the clock amplifier No. 1, by monitoring the signal and voltage levels at the test jacks provided. No particular section of the test panel is provided for the controls to test clock amplifier No. 1. Only the POWER ON-OFF switch, BRIDGE ON-OFF switch, MASTER

SELECTOR switch, panel connectors, and test points are utilized during this test. The positions of other controls on the component tester will not affect this test.

Static Test Preparation

The following preparation should be completed before beginning the static tests:

1. Set MASTER SELECTOR switch to 13.
2. Set POWER switch to ON.
3. Set BRIDGE switch to ON (located on 4-POWER SUPPLY SECTION).
4. Monitor -6-, -18-, +6-, -12-, and +75-volt d-c levels at the INTERNAL TEST POINTS shown in table 1. Tolerances should agree with those shown in the table.
5. Set POWER switch to OFF.
6. Plug extender panel No. 1 into CLOCK AMPLIFIER NO. 1 test jack at top of tester.
7. Connect input terminal pin 20 (on extended panel) to ground.
8. Plug clock amplifier No. 1 into extender panel.
9. Set POWER switch to ON.

Static Test on Q1

To test Q1, proceed as follows:

1. Turn potentiometer R4(clock amplifier No. 1)counterclockwise until green is observed.
2. Connect INTERNAL TEST POINT 27 (-6 volts) to TP2 on clock board No. 1.
3. Connect the leads of the VTVM between TP1 (clock board No. 1) and ground to monitor the output. Voltage should be within the range of -0.33- to 0-volt dc.
4. Remove connection between INTERNAL TEST POINT 27 and TP2 on board.

Static Test on Q2

To test Q2, proceed as follows:

1. Connect INTERNAL TEST POINT 27 (-6 volt) to TP1 on clock board No. 1.
2. Connect the leads of the VTVM between TP2 and ground. The voltage should be within the range of -0.2- to 0-volt dc.
3. Remove connection between INTERNAL TEST POINT 27 and TP1 on board.

Static Test on Q6

To test Q6, proceed as follows:

1. Connect the leads of the VTVM between TP9 on the board (+6 volts is applied through pin 6 from tester) and pin 22 on extender panel No. 1.
2. This voltage should be within the range from 0- to 4.2-volt dc.

Static Test on Q3

If Q6 meets the requirements as specified, test Q3 as follows:

1. Apply -25-volt dc to pin 3 on extended panel No. 1 from an external power supply.
2. Connect the VTVM between TP3 on board and ground. The voltage should be within the range of -0.33- to 0-volt dc.

Static Test on Q4

To test Q4, proceed as follows:

1. Connect the VTVM between pin 23 on extender panel No. 1 and TP 20 on clock board No. 1. The voltage should be no more than 0.22-volt dc.
2. Remove the external -25-volt dc from pin 3 on extender panel No. 1.

Static Test on Q5

To test Q5, proceed as follows:

1. Connect pin 1 on extender panel No. 1 to ground.
2. Apply external -25-volt dc to pin 2 on extender panel No. 1.
3. Connect the VTVM between TP4 on clock board No. 1 and ground. The voltage should be within the range of -0.16- to 0-volt dc.
4. Remove the external -25-volt dc from pin 2 and disconnect pin 1 from ground.

Static Test on Q8

To test Q8, proceed as follows:

1. Connect INTERNAL TEST POINT 35 (+75 volt) to TP5 on clock board No. 1.
2. Connect the VTVM between TP6 and TP14 on clock board No. 1. The voltage should be within the range from 0- to 0.18-volt dc.
3. Remove the connection between INTERNAL TEST POINT 35 and TP5.

Static Test on Q7

To test Q7, proceed as follows:

1. Connect the VTVM between TP5 on clock board No. 1 and ground.
2. The voltage should be within the range from +7.5- to +10.5-volt dc.

Static Tests on Q11 and Q12

To test Q11 and Q12, proceed as follows:

1. Connect the VTVM between pin 37 on extender panel No. 1 and ground.
2. The voltage should be within the range from -15- to -10-volt dc.

Static Tests on Q13 and Q14

To test Q13 and Q14, proceed as follows:

1. Connect pin 17 (circuit output) on extender panel No. 1 to ground.
2. Connect the VTVM between TP10 on clock board No. 1 and ground. The voltage should be within the range from 0- to 0.004-volt dc.
3. Connect the VTVM between TP12 and ground. The voltage should be within the range from 0- to 0.004-volt dc.
4. Disconnect pin 17 from ground.

Static Tests on Q15 through Q18

To test these transistors, proceed as follows:

1. Connect the VTVM between TP15, TP16, TP17, and TP18 individually and TP11 on clock board No. 1. Each voltage measured should be no more than 0.0005-volt dc.
2. Connect the VTVM between TP9 (board 1) and pin 17 on the extender panel. The voltage should be within the range from 0- to 0.9-volt dc.

Static Test on Q20

To test Q20, proceed as follows:

1. Connect pin 19 (output of strobe circuit) on extender panel to ground.
2. Connect the VTVM between TP19 (clock No. 1) and pin 19 on the extender panel. The voltage should be within the range from 0- to 0.004-volt dc.
3. Disconnect pin 19 from ground.

Static Test on Q19

To test Q19, proceed as follows:

1. Connect the VTVM between pin 19 on extender panel and TP9. The voltage should be within the range from -0.2- to 0-volt dc.
2. Set POWER switch to OFF before removing circuit board on extender panel.

Dynamic Test Preparation

The following preparation should be completed before beginning the dynamic tests:

1. Perform preparation procedures 1 through 5 of Static Test Preparation, page 84.
2. Plug clock amplifier No. 1 into test jack at top of tester.
3. Set POWER switch to ON.

Note

Pulsewidth during the following tests is determined by the internal high frequency oscillator which should be 157 kilocycles ±10 percent; therefore only pulse amplitude and rise and fall time are critical. The input frequency may be monitored at EXTERNAL TEST POINT 13-43, or INTERNAL TEST POINT 20.

Dynamic Test - Output 1

Calibrate the oscilloscope input as follows:

Set vertical sensitivity for full vertical deflection.
Set SQUARE WAVE CALIBRATOR switch to 50V.
Set TIME/DIV. switch to 2 USEC.

1. Connect the input to ground, and adjust VERTICAL POSITION switch until ground level is approximately 3.5 centimeters below the top of the oscilloscope screen.
2. Connect the input to EXTERNAL TEST POINT 13-39.
3. Place an acetate template corresponding to the dimensions shown in figure 45, part A, over the oscilloscope screen and adjust it until the ground level lies just above point A. Point A should also just touch the vertical trace

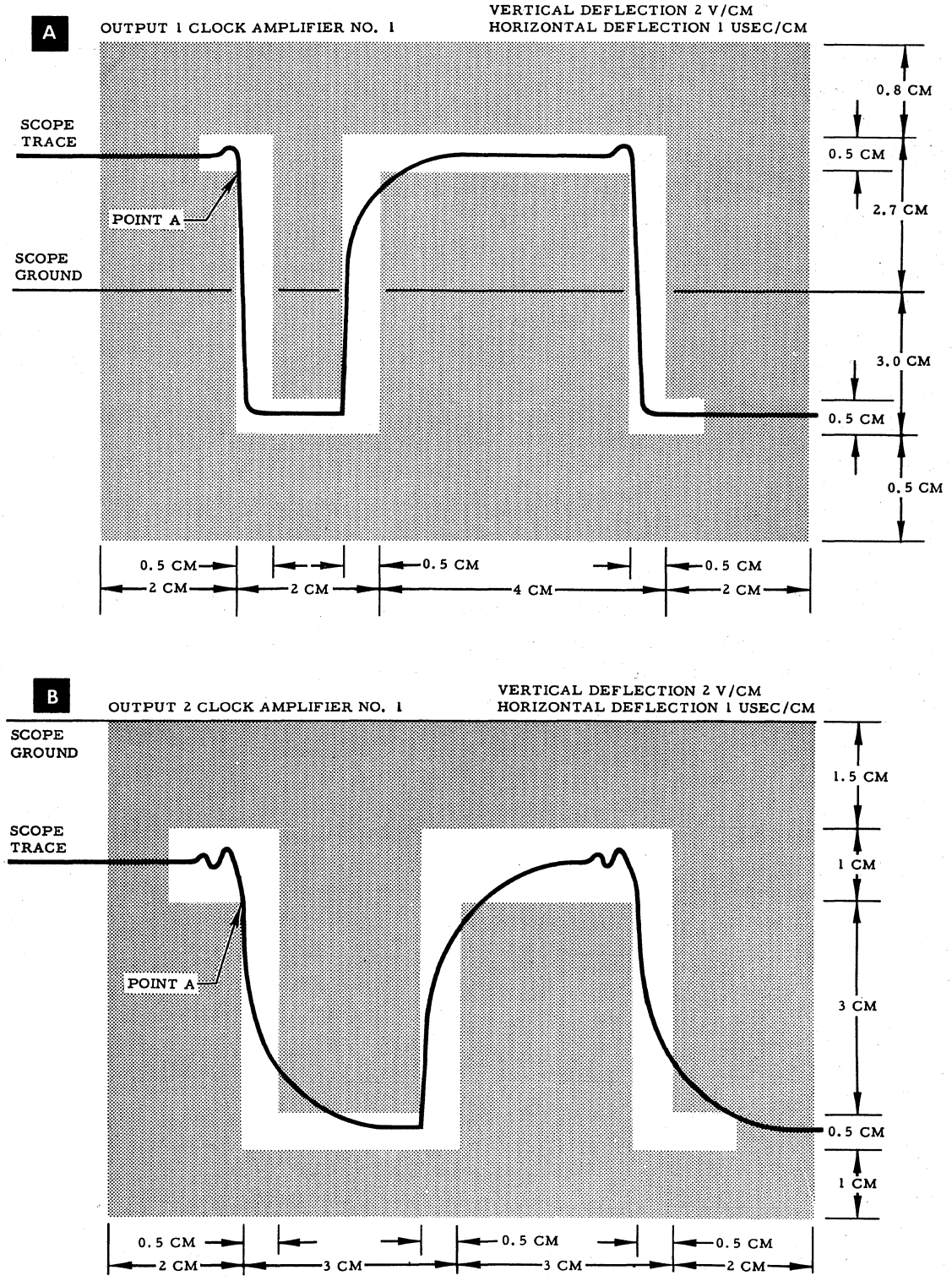

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Figure 45. Calibration Template, Clock Board No. 1, Outputs 1 and 2

of the clock waveform. Small irregularities of overshoot as shown in the figure do not need to fall within the tolerance area, but all straight lines should fall within the cut out area. If waveform does not conform to the template tolerances, resistor R17 on the clock etched board being tested should be adjusted. If the waveform cannot be adjusted to come within the template specifications, the board should be replaced.

Dynamic Test - Output 2

Calibrate the input on the oscilloscope as follows:

Set vertical sensitivity for full deflection
Set SQUARE WAVE CALIBRATOR switch to 50V.
Set TIME/DIV. switch to 2 USEC.

1. Connect the input to ground, and adjust VERTICAL POSITION switch until the zero or ground level is located at the top line on the oscilloscope screen.
2. Connect the input to EXTERNAL TEST POINT 13-40.
3. Place an acetate cutout corresponding to the dimensions of figure 45, part B, over the oscilloscope screen and adjust it until the ground level lies just above point A. Point A should also just touch the vertical trace line. Small overshoot irregularities need not fall inside the tolerance area. If the waveform fails to come within template tolerances, the board should be replaced.

Note

Rise and fall times are not critical due to rounded edges of waveform. This waveform is not an output signal.

Dynamic Test - Output 3

Calibrate the oscilloscope input as follows:

Set vertical sensitivity for full deflection.
Set SQUARE WAVE CALIBRATOR switch to 50V.
Set TIME/DIV. switch to 1.

1. Connect the input to ground and adjust the VERTICAL POSITION switch until the ground level is 1 centimeter below the top of the oscilloscope screen.
2. Connect the input to EXTERNAL TEST POINT 13-41.

3. Place an acetate template corresponding to the dimensions of figure 46, part A, over the oscilloscope screen and adjust it until the ground level lies just above point A. Point A should also just touch the vertical trace line. Small overshoot irregularities need not fall inside the tolerance area. If the waveform fails to come within the template tolerances, the board should be replaced.

Dynamic Test - Output 4

Calibrate the oscilloscope input as follows:

Set vertical sensitivity for full deflection.
Set SQUARE WAVE CALIBRATOR switch to 100V.
Set TIME/DIV. switch to 1 USEC.

1. Connect the input to ground and adjust the VERTICAL POSITION switch until the ground level is 4.0 centimeters below the top line on the oscilloscope screen.
2. Connect the input to EXTERNAL TEST POINT 13-42.
3. Place an acetate template corresponding to the dimensions of figure 46, part B, over the oscilloscope screen and adjust it until the ground level lies just above point A. Point A should also just touch the vertical trace line. The extremely round portion of the waveform may not fit into the tolerance area of the template, however, this is acceptable. If the waveform fails to come within other template tolerances, the board should be replaced.

Dynamic Test - Output 5

Calibrate the oscilloscope input as follows:

Set vertical sensitivity for full deflection.
Set SQUARE WAVE CALIBRATOR switch to 5V.
Set TIME/DIV. switch to 1 USEC.

1. Connect the input to ground and adjust the VERTICAL POSITION switch until the ground is located 2.0 centimeters below the top line of the oscilloscope screen.
2. Connect the input to EXTERNAL TEST POINT 13-44.
3. Place an acetate template corresponding to the dimensions of figure 47 over the oscilloscope screen and adjust it until the ground level lies just above point A. Point A should also just touch the vertical trace line. Small overshoot irregularities need not fall inside the tolerance area of the template. If the waveform fails to come within the template tolerances, the board should be replaced.

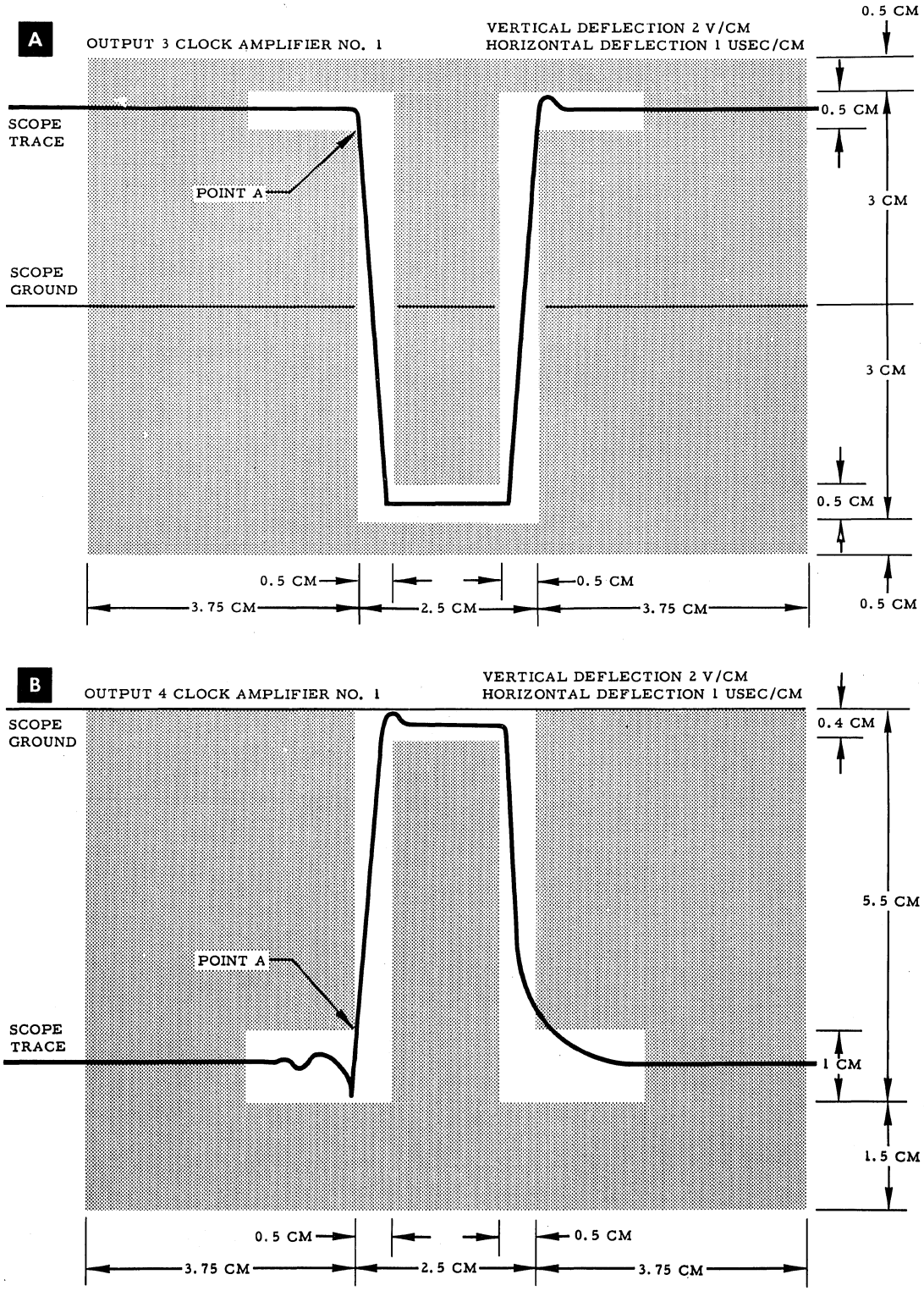


Figure 46. Calibration Template, Clock Board No. 1, Outputs 3 and 4

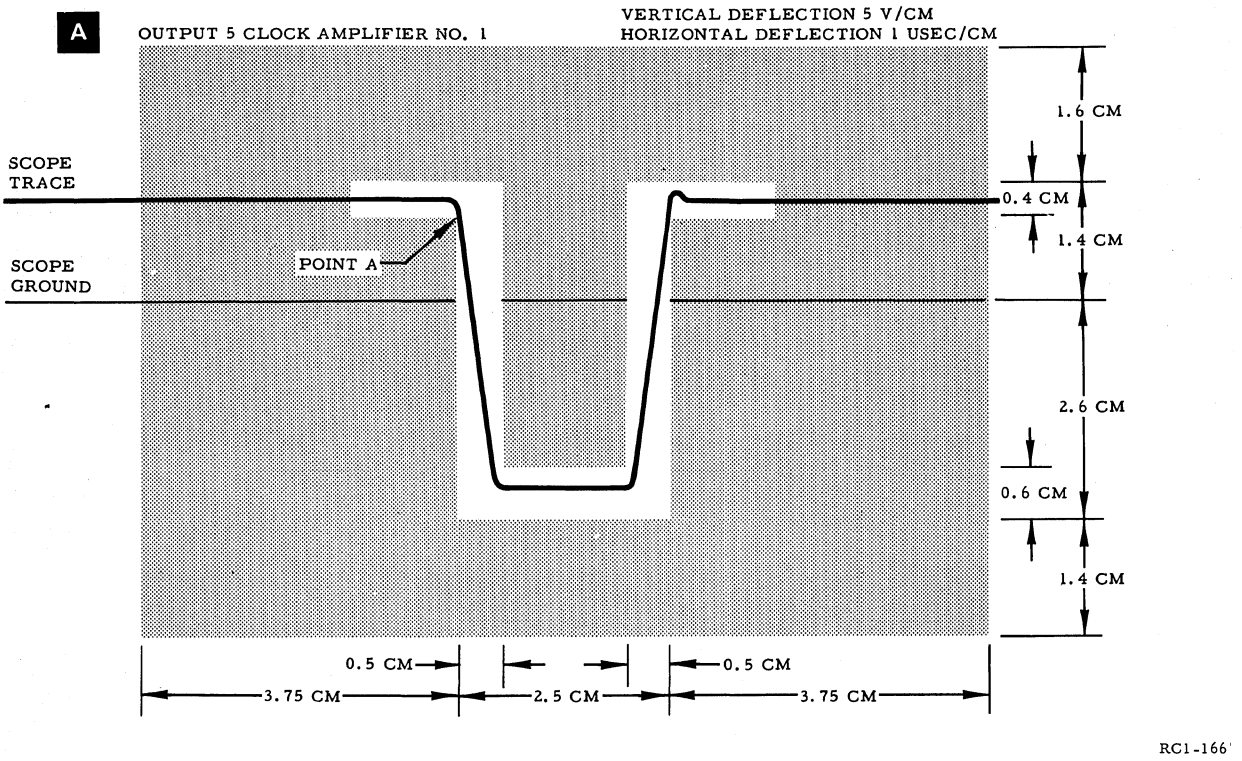


Figure 47. Calibration Template, Clock Board No. 1, Output 5

CLOCK POWER AMPLIFIER NO. 2 CIRCUIT BOARD

Static and dynamic tests are performed on clock amplifier No. 2.

Static operation of the transistors on board No. 2 is checked prior to the dynamic tests by applying voltages of the proper value from the tester to the bases and by monitoring the voltages to determine collector stability at the output. For pin numbers and test point locations refer to amplifier clock No. 2 schematic in the appendixes.

For the dynamic test, only the power ON-OFF switch, BRIDGE ON-OFF switch, MASTER SELECTOR switch, panel connectors, and test points are utilized. The positions of other controls on the component tester do not affect this test.

Static Test Preparation

The following preparation should be completed before beginning the static tests:

1. Set MASTER SELECTOR switch to 14.
2. Set POWER switch to ON.
3. Set BRIDGE switch to ON (controls internal positive d-c voltage levels, and is located in the 4-POWER SUPPLY controls section).

4. Monitor -6-, -18-, +6-, -12-, and +75-volt d-c levels at the INTERNAL TEST points shown in table 1. Tolerances should agree with those shown in the table.

5. Set POWER switch to OFF.

6. Plug extender panel No. 1 into CLOCK AMPLIFIER NO. 2 test jack at top of tester.

7. Plug clock amplifier No. 2 into extender panel No. 1.

Note

Terminals on extender panel are merely extensions of the terminals on clock power amplifier No. 2.

8. Place POWER switch at ON.

Static Tests on Q1 through Q20

To test transistors Q1 through Q20, proceed as follows:

1. Connect INTERNAL TEST POINT 33 (+6 volts from tester) to terminal input pin 5 on extender panel No. 1.

2. Connect the VTVM between TP1 through TP20 on board No. 2 individually and ground and monitor the voltage level.

3. Each voltage should be within the range from -0.0005- to 0-volt dc.

4. Disconnect INTERNAL TEST POINT 33 from pin 5 and open the switch to pin 1 on extender panel No. 1 (removes +6 volts from board).

5. Connect the VTVM between TP1 through TP20 individually and TP21 (ground) on board No. 2 and monitor the voltage levels.

6. Each voltage should be within the range from -0.025- to 0-volt dc.

Static Tests on Q21 through Q23

To test transistors Q21 through Q23, proceed as follows:

1. Connect the VTVM between TP21 through TP23 on board No. 2 individually and pin 37 (output terminal) on extender panel No. 1 and monitor the voltage levels.

2. Each voltage should be within the range from -0.004- to 0-volt dc.

3. Set POWER switch to OFF before removing clock amplifier No. 2 and extender panel No. 1 from tester.

Dynamic Test Preparation

The following preparation should be completed before performing the dynamic test:

1. Perform preparation procedures 1 through 5 of Static Test Preparation, page 84.
2. Plug panel assembly into test jack at top of tester.
3. Set POWER switch to ON.
4. Calibrate output 1 of tester clock amplifier No. 1. (Panel is located inside the component tester.) Use test procedures for Dynamic Test - Output 1, page 87.

Dynamic Test

To perform the dynamic test calibrate the oscilloscope input as follows:

Set vertical sensitivity for full deflection of 25 volts
Set SQUARE WAVE CALIBRATOR switch to 20V.
Set TIME/DIV. switch to 1 USEC.

1. Place an acetate template corresponding to the dimensions of figure 48 over the oscilloscope screen and adjust it until the ground trace coincides with the top of the cutout area.
2. Connect the input to EXTERNAL TEST POINT 14-13.
3. Adjust the horizontal position of the trace until point A of the template is just touching the vertical trace line. The waveform should come within the tolerances listed on the template. Small irregularities of overshoot, as shown in the figure do not need to fall within the tolerance area, but all straight lines should fall within the indicated area. If waveform does not comform to the template tolerances, the board should be replaced.

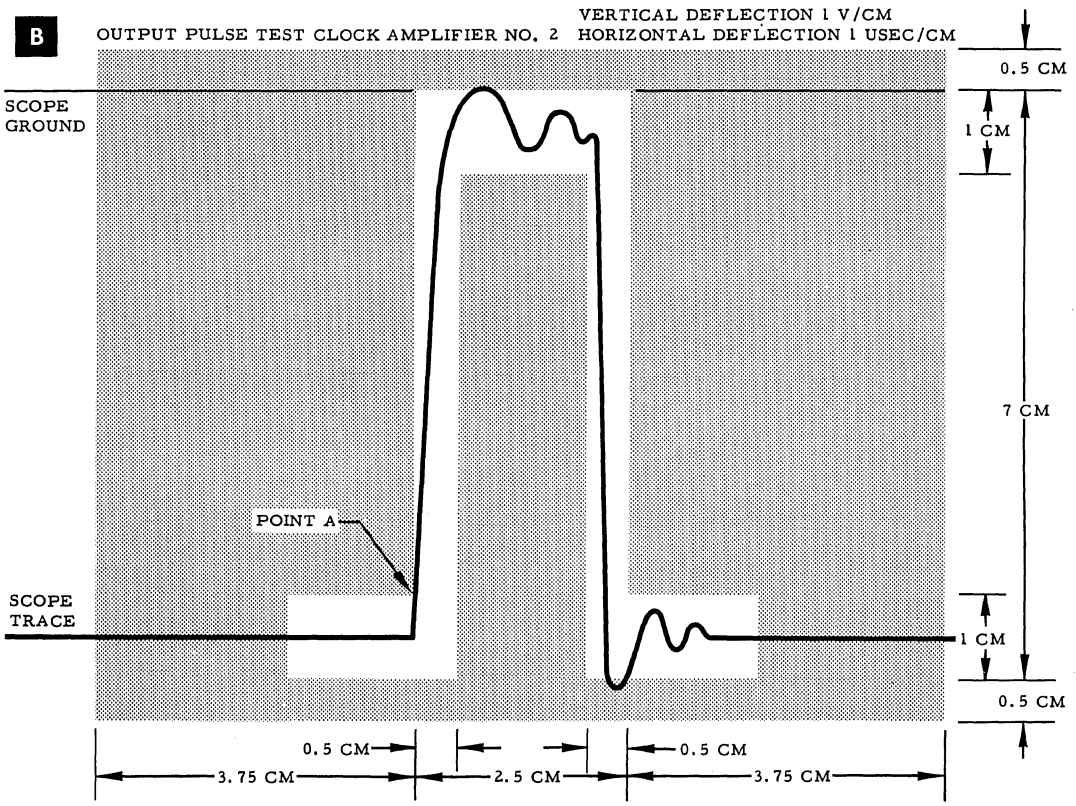


Figure 48. Calibration Template, Clock Board No. 2, Pulse Output

GENERAL MAINTENANCE INFORMATION

REMOVAL AND REPLACEMENT OF COMPONENTS

CAUTION

The computer assembly must never be moved immediately after power shutdown. The rotating memory disk continues to rotate for approximately 12 minutes after power removal and if moved suddenly when it is coasting the gyroscopic effect of the rotating disk may cause it to scrape against the headplate.

OUTSIDE COVERS

Of the 6 computer framework covers, only the 2 side covers need to be removed for normal maintenance of the computer assembly. To remove the side covers, proceed as follows:

1. Release the snap fasteners at the bottom left and bottom right of each side cover.
2. Grasping bottom left-hand side and bottom right-hand side of the cover, lift up straight. Curved hooks at the top of each cover should slide out of their slots as the cover is lifted.
3. To gain access to internal components, release the snap fasteners at the bottom of the hinged castings and carefully open the castings toward the rear of the computer assembly.

MEMORY

To remove the memory unit, proceed as follows:

1. Be positive that the memory motor has been off for at least 12 minutes.
2. Disconnect the following plugs from the memory unit:

Plug No.	Type of Connector
12, 14, 16, 17, and 19	Write head connectors
11, 13, 15, 18, and 20	Read head connectors
30	Memory unit power connector

3. Remove four screws from memory mounting bracket.

CAUTION

Hold memory while removing screws to prevent dropping.

4. Remove memory unit through left-hand side of frame.

To replace the memory, use the removal steps in reverse order as a guide.

POWER SUPPLY CHASSIS

To remove the power supply chassis, proceed as follows:

1. Remove the two screws and locknuts at top of assembly which hold unit to frame of computer.
2. Remove complete power supply assembly by pulling upward until unit is free of jacks (J29 and J34).

Power Supply Circuit Boards

To remove the power supply etched boards from the power supply unit, proceed as follows:

1. Remove power supply unit from computer.
2. Remove the associated retaining screws at top of each panel assembly which hold panel to power supply assembly.
3. Disconnect etched board from associated power supply jack. In many cases the use of a slot screwdriver is helpful when prying boards loose from jacks. The screwdriver should be placed between the metal case and chassis and pried slightly upward until panel assembly is released from jack. The following power supply etched boards are connected to the power supply unit:

Etched Board	Jack No.
+6, -6, and +0.75 volts	J1
-12 and +75 volts	J2
-18, -100, and -3 volts	J3
Relay control network	J4
Network	J5
Filter network	J6

Power Control Relays

To remove the power control relays, proceed as follows:

1. Remove the two retaining screws at base of relays K1 through K6.
2. Remove relays from respective sockets.

SIGNAL CIRCUITS

The etched boards are removed from the computer chassis with the aid of etched circuit board extractors. To remove an etched board proceed as follows (figure 49):

1. Insert the extractor over the mounting post with the extracting flange pointing toward the opposite mounting post.

CAUTION

Do not force extractor over the mounting post. Forcing the extractor could result in serious damage to parts located near the post.

2. Carefully rotate extractor clockwise and counterclockwise until it is seated against the bottom of the chassis.
3. Apply a slight counterclockwise motion to each of the extractors while depressing the extractor knobs within the palm of hand. The etched board should release from chassis jack.
4. Remove etched board extractors from mounting post taking same precautions when inserting extractor over post.
5. Remove board from mounting post by holding at edges.

CAUTION

Avoid touching electronic components with hands.

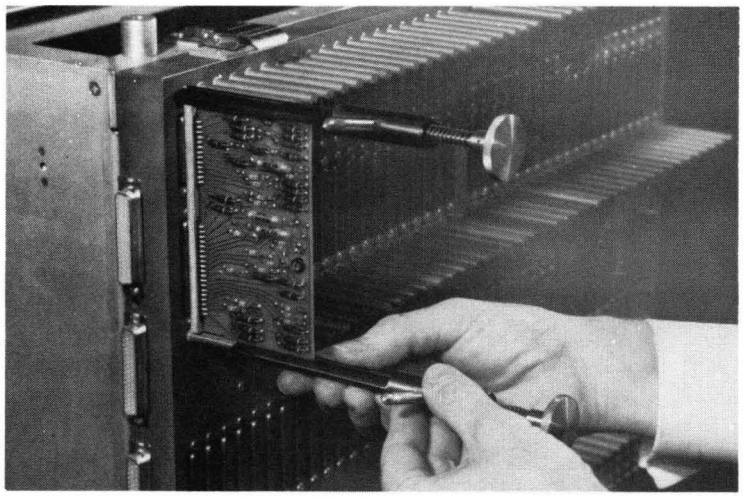
Extractor tools are not used to replace circuit boards. Merely hold mounting frame steady and insert circuit boards into their receptacles slowly but firmly.

BLOWER ASSEMBLY

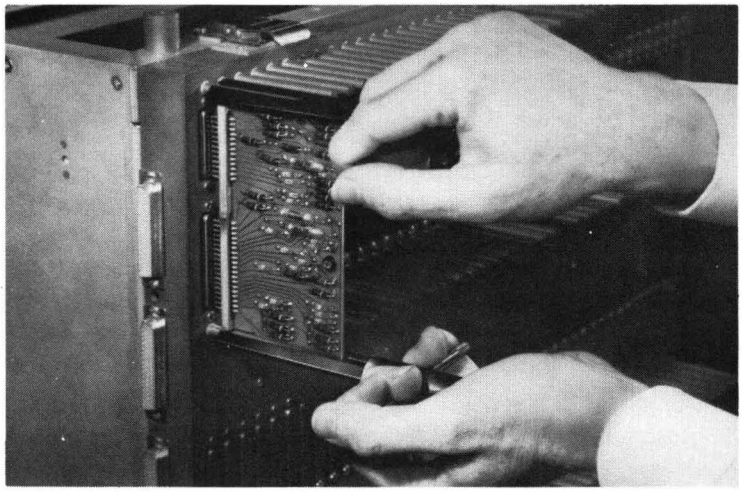
Filter

To remove the filter, proceed as follows:

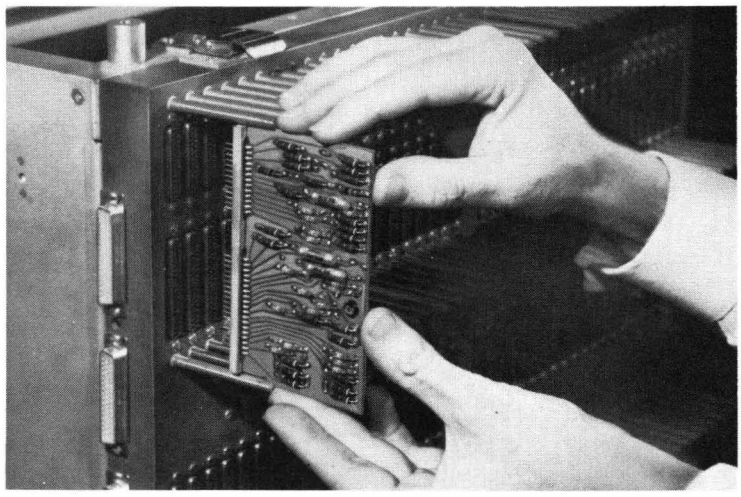
1. Remove six screws from filter retaining frame.
2. Remove filter retaining frame and electrostatic filter from top-center cover.
3. Remove electrostatic filter from retaining frame by removing the six flathead screws and locknuts.



A PLACEMENT OF SPECIAL TOOLS



B TOOLS IN USE



C REMOVAL OF PANEL

RC1-176

Figure 49. Use of Etched Circuit Board Extractors

Note

Filter may be cleaned without removing retaining frame.

To replace filters, use removal procedures in reverse order as a guide.

Blowers

To remove the blowers, proceed as follows:

1. Remove two screws near top of front and rear end covers.
2. Remove four hex-head bolts on top center cover.
3. Remove top center cover assembly (including filter and filter retaining frame).
4. Disconnect power plugs P31 and P32 from associated chassis jacks.
5. Remove four mounting screws attaching blower units to frame.
6. Remove blowers through top of chassis.

To replace the blowers, use removal procedures in reverse order as a guide.

COMPUTER CONNECTOR SIGNAL CHART

The computer connector signal chart represents each cable receptacle, plug receptacle, and terminal board located in the computer assembly, excluding the signal circuit board receptacles and the power circuit board receptacles in the power supply assembly. The chart further identifies each signal found at each pin of these receptacles. See figure 50.

Each individual square represents a pin or a jack on the receptacle, and the letter designation or the combination letter and number designation within individual squares represents the signal or voltage found at that pin or jack. These designations are in general those used for the computer logic equations, or, if not used in the logic equations, are defined in the computer wire list.

CIRCUIT BOARD CONNECTOR SIGNAL CHARTS

Six circuit board connector signal charts are required to represent each plug-in circuit board receptacle mounted on the two side castings of the computer assembly. Again, the signal charts also identify each signal found at each pin or jack of these receptacles, with individual squares representing individual pins or jacks. Each connector signal chart illustrates one complete row of 40 connectors. There are 6 such rows of connectors, 3 on each side casting, thus, there are 6 charts. See figures 51 through 56.

Two of the rows of connectors on each side casting are made up of double-receptacle connectors and one is made up of single-receptacle connectors. Therefore, there are actually five rows of receptacles on each side: number designations 101-140 through 501-540 (side No. 1) and 141-180 through 541-580 (side No. 2). Thus, a 3-digit number specifies exactly 1 receptacle. For example, receptacle 129 specifies the top receptacle in the 29th position of side No. 1.

The following paragraphs briefly discuss the layout of each signal chart.

100-200 SERIES—SIDE NO. 1

This chart is arranged to facilitate signal checking of the logic network boards plugged into receptacles 102 and 202 through 131 and 231. All the pins on the particular board are represented by one horizontal row of squares. The pin numbers for each logic network board are printed at the top of the chart and grouped into individual gates on the boards. The output pin numbers are raised above the input pin numbers for each gate. The number at the top of each gate grouping indicates the number of diodes used in that gate.

The second part of this chart illustrates the signals found at each pin of the eight write switches plugged into side No. 1.

300 SERIES—SIDE NO. 1

This chart is arranged to facilitate signal checking of the flip-flop boards plugged into side No. 1. As for all other signal charts, one horizontal row of squares represents all the pins on a particular circuit board. The pin numbers along the top of the chart are grouped into 4 sets of input-output signals (four flip-flops on a board) and 1 set of voltages.

This chart also illustrates the signal found at each pin of the write amplifier circuit boards and the clock power amplifier boards.

400-500 SERIES—SIDE NO. 1

This chart is arranged according to the same rules as the 100-200 series chart for side No. 1 in order to facilitate signal checking of the logic network boards plugged into 402 and 502 through 424 and 524. It also illustrates the signals found at each pin of 3 computer network boards and the 11 nonmain memory read amplifier boards.

100-200 SERIES—SIDE NO. 2

This chart is arranged according to the same rules as the 100-200 series chart for side No. 1 in order to facilitate signal checking of the logic network boards plugged into 151 and 251 through 179 and 279. It also illustrates the signals found at each pin of the other three computer network boards.

300 SERIES—SIDE NO. 2

This chart is arranged according to the same rules as the 300 series chart for side No. 1 in order to facilitate signal checking of the flip-flop boards plugged into side No. 2. It also illustrates the signals found at each pin of the eight read switching circuit boards.

400-500 SERIES—SIDE NO. 2

This chart is arranged according to the same rules as the 100-200 series chart for side No. 1 in order to facilitate signal checking of the logic network boards plugged into 452 and 552 through 479 and 579 (except that receptacles 462 and 562 comprise a spare connector).

P11
P13
P15
P18
P12
P14
P16
P17
P19
P20
B3
B1
B2
SB1
SB2
INT 1
INT 2
THA
J35
J28
J31
J30
J32
TB04
IDLE LINE IN
MEMORY POWER

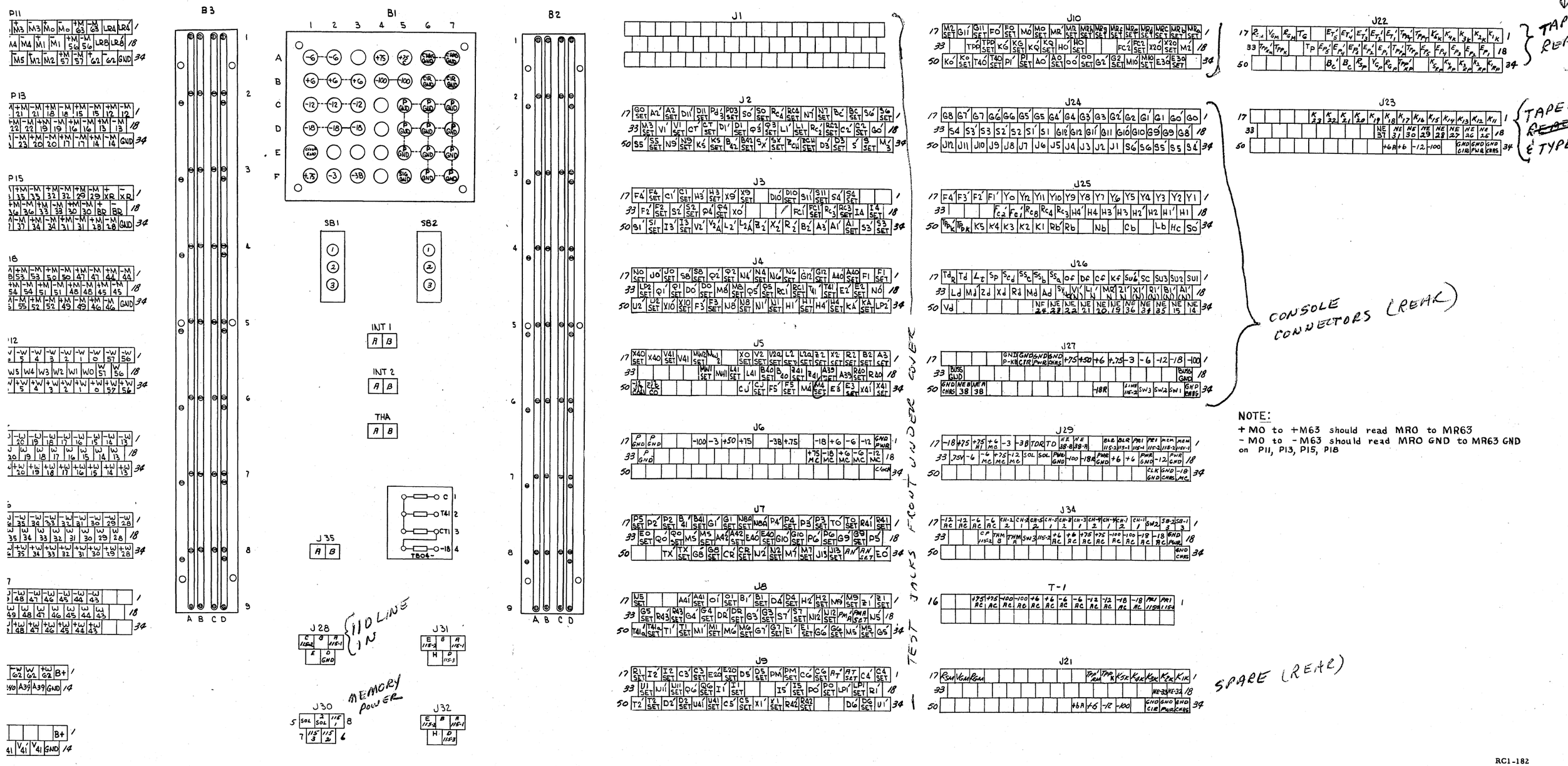


Figure 50. Computer Connector Signal Chart

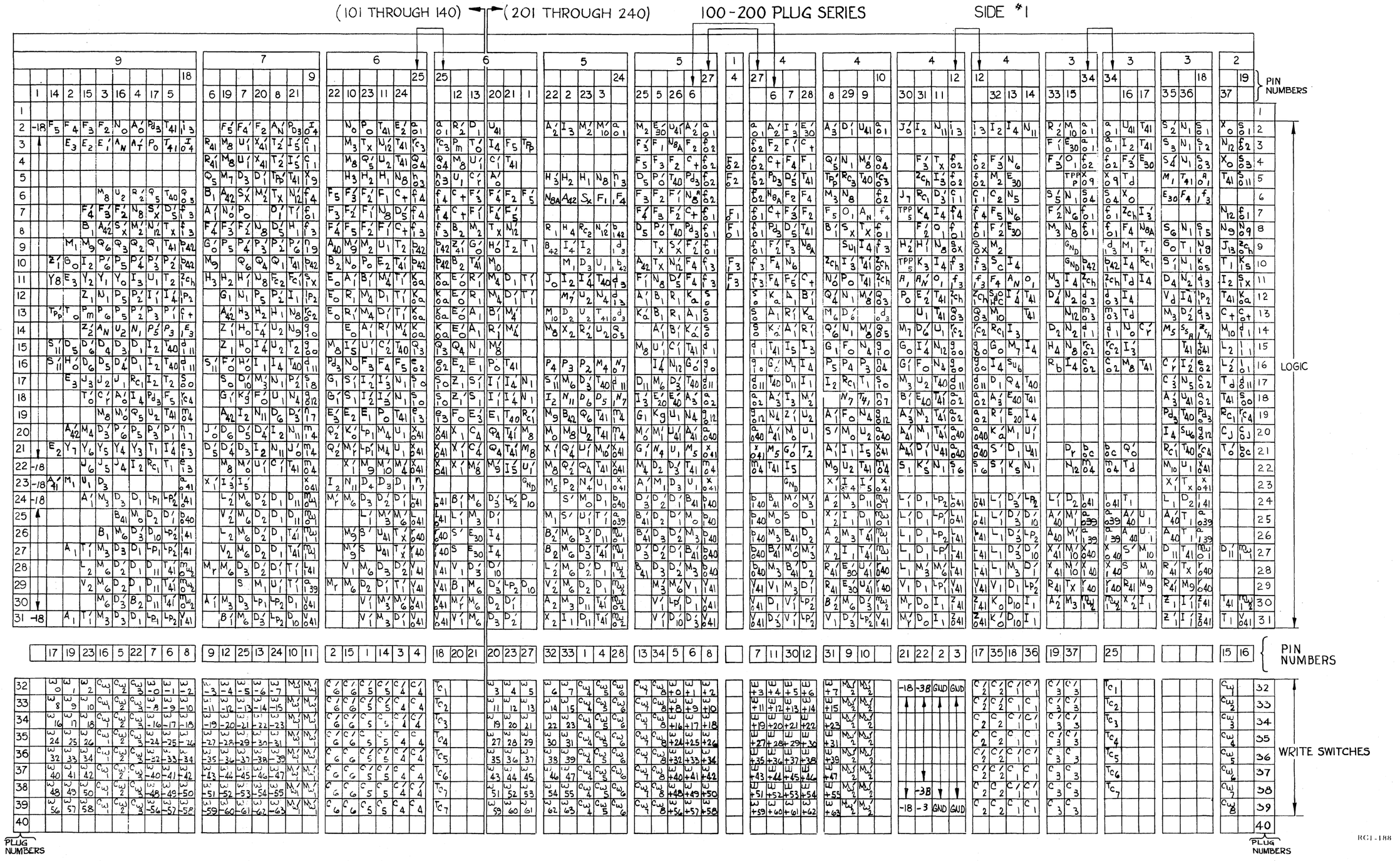


Figure 51. Circuit Board Connector Signal Chart No. 1

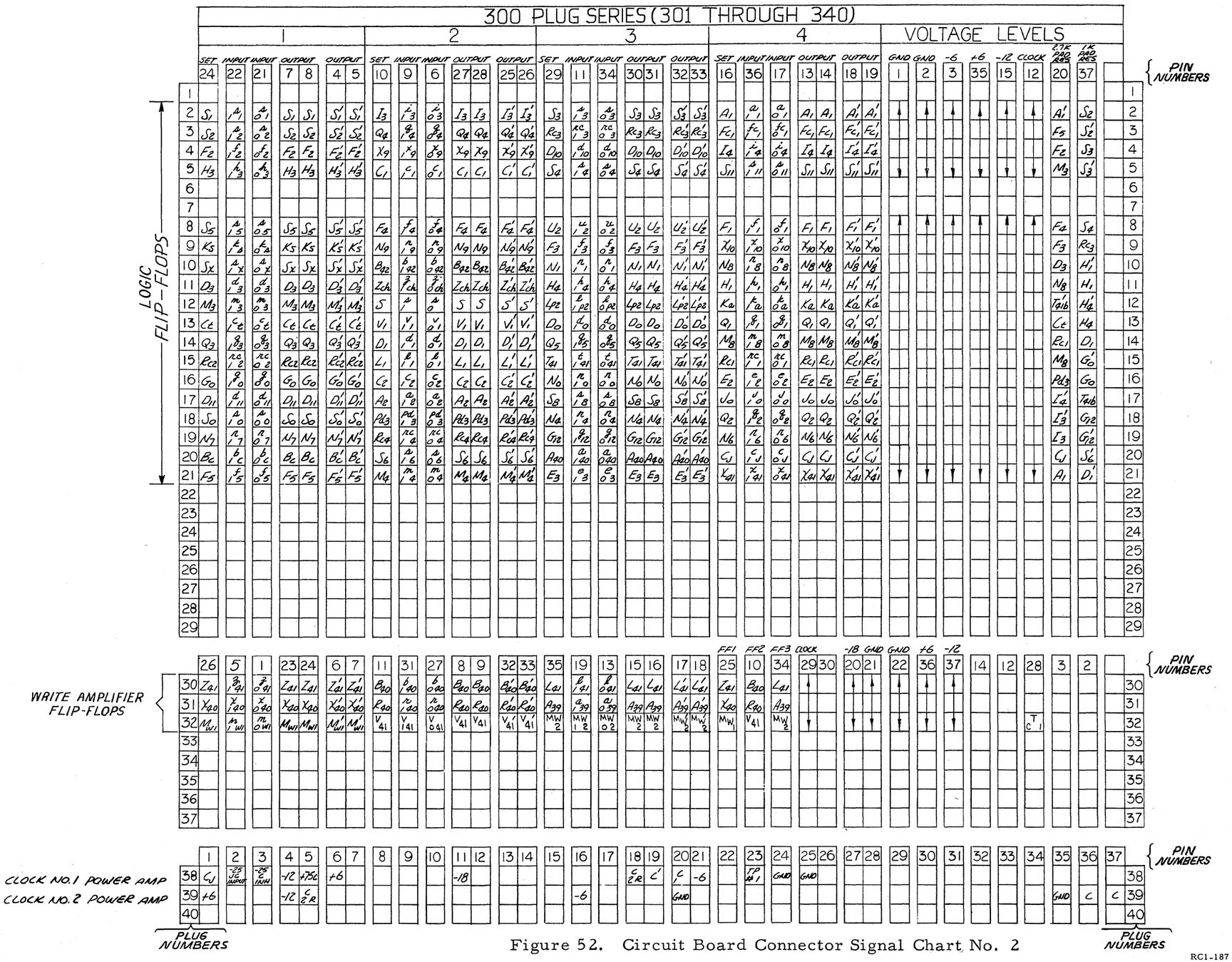


Figure 52. Circuit Board Connector Signal Chart No. 2

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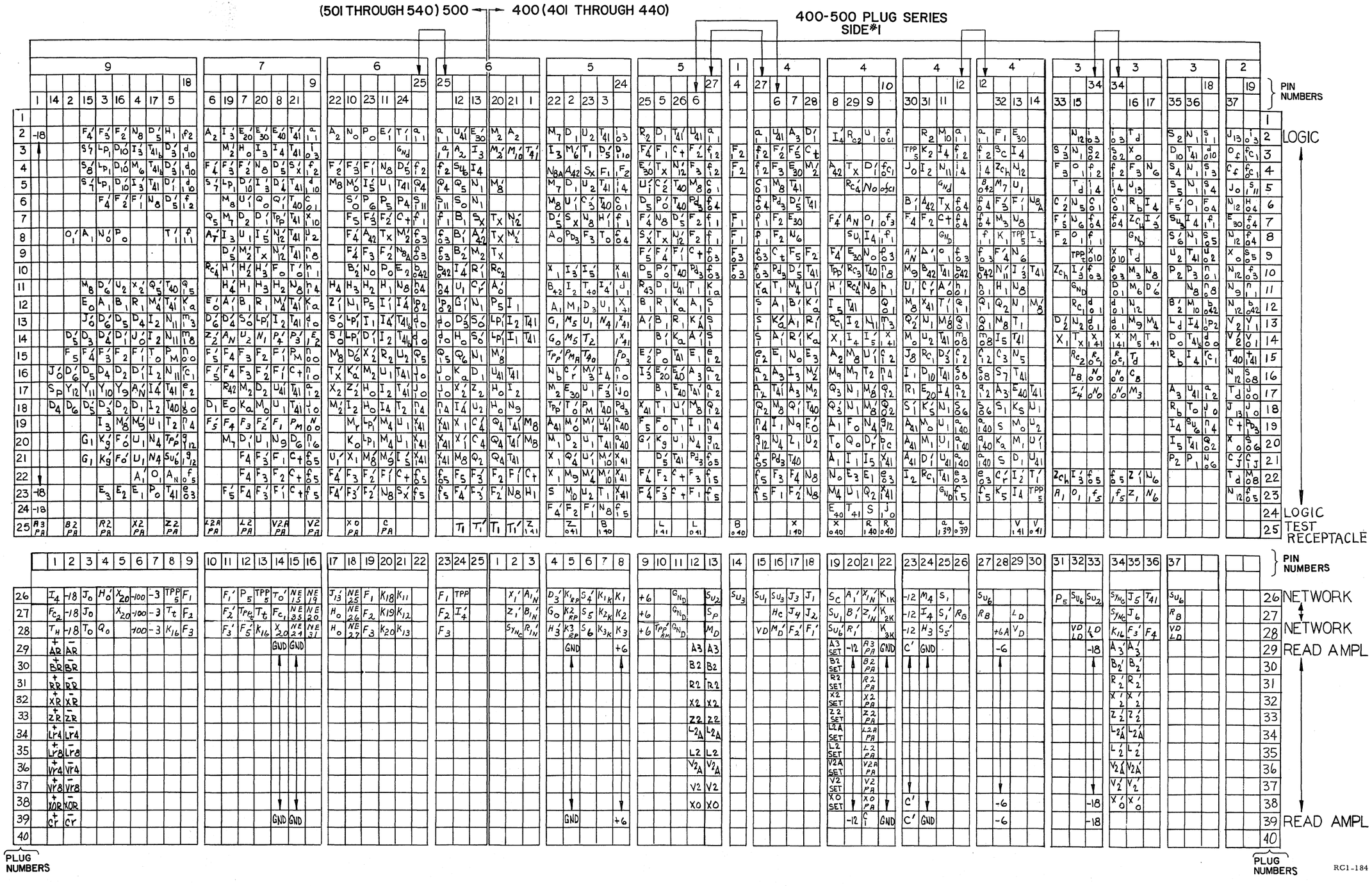

Figure 53. Circuit Board Connector Signal Chart No. 3

100-200 PLUG SERIES-SIDE #2

(141 THROUGH 180) 100 ← → 200 (241 THROUGH 280)

PIN NUMBERS

LOGIC

PIN NUMBERS 46 THROUGH 49, SPARES

NETWORK

PLUG NUMBERS

PLUG NUMBERS

RC1-185

Figure 54. Circuit Board Connector Signal Chart No. 4

300 SERIES SIDE # 2
(341 THROUGH 380)

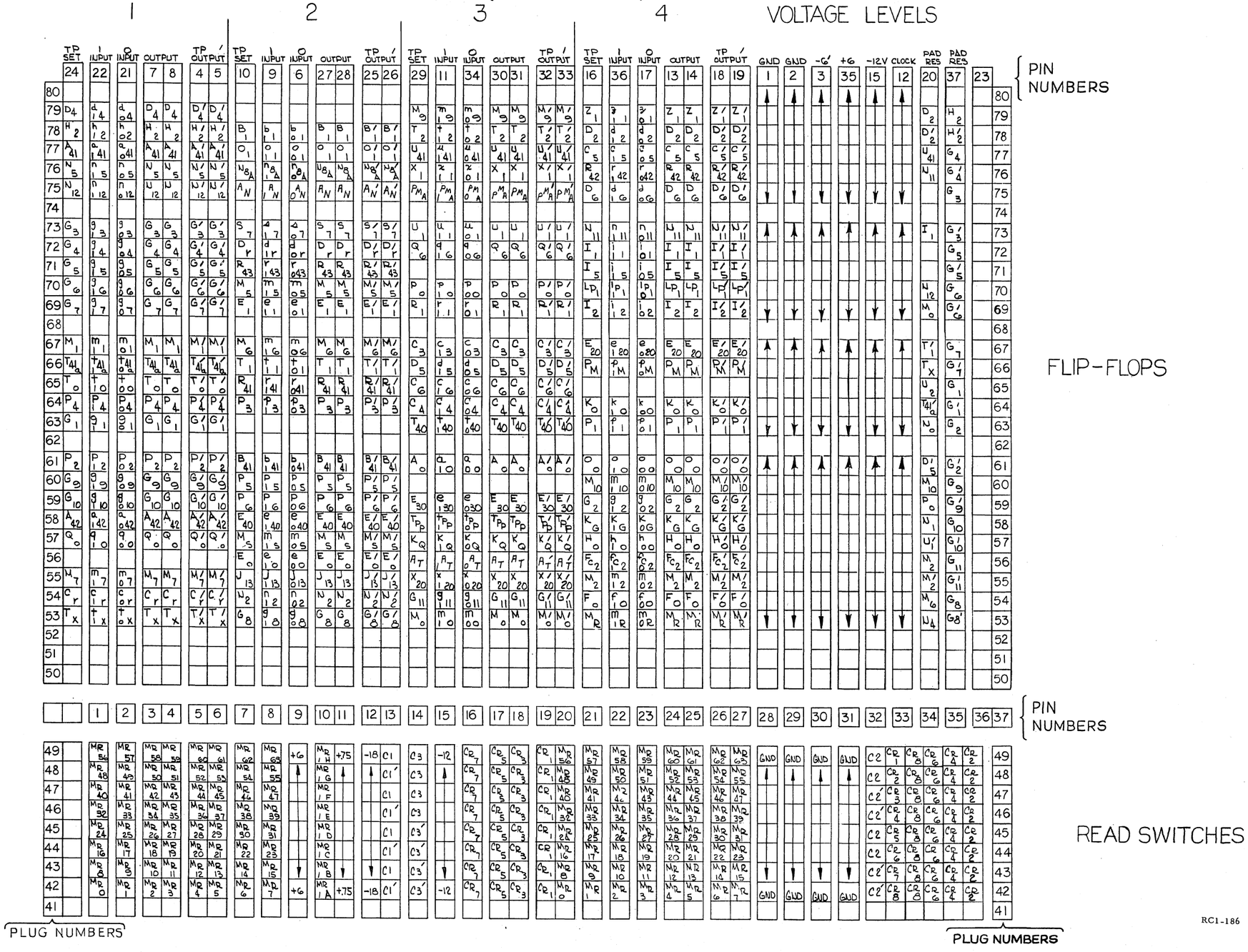

Figure 55. Circuit Board Connector Signal Chart No. 5

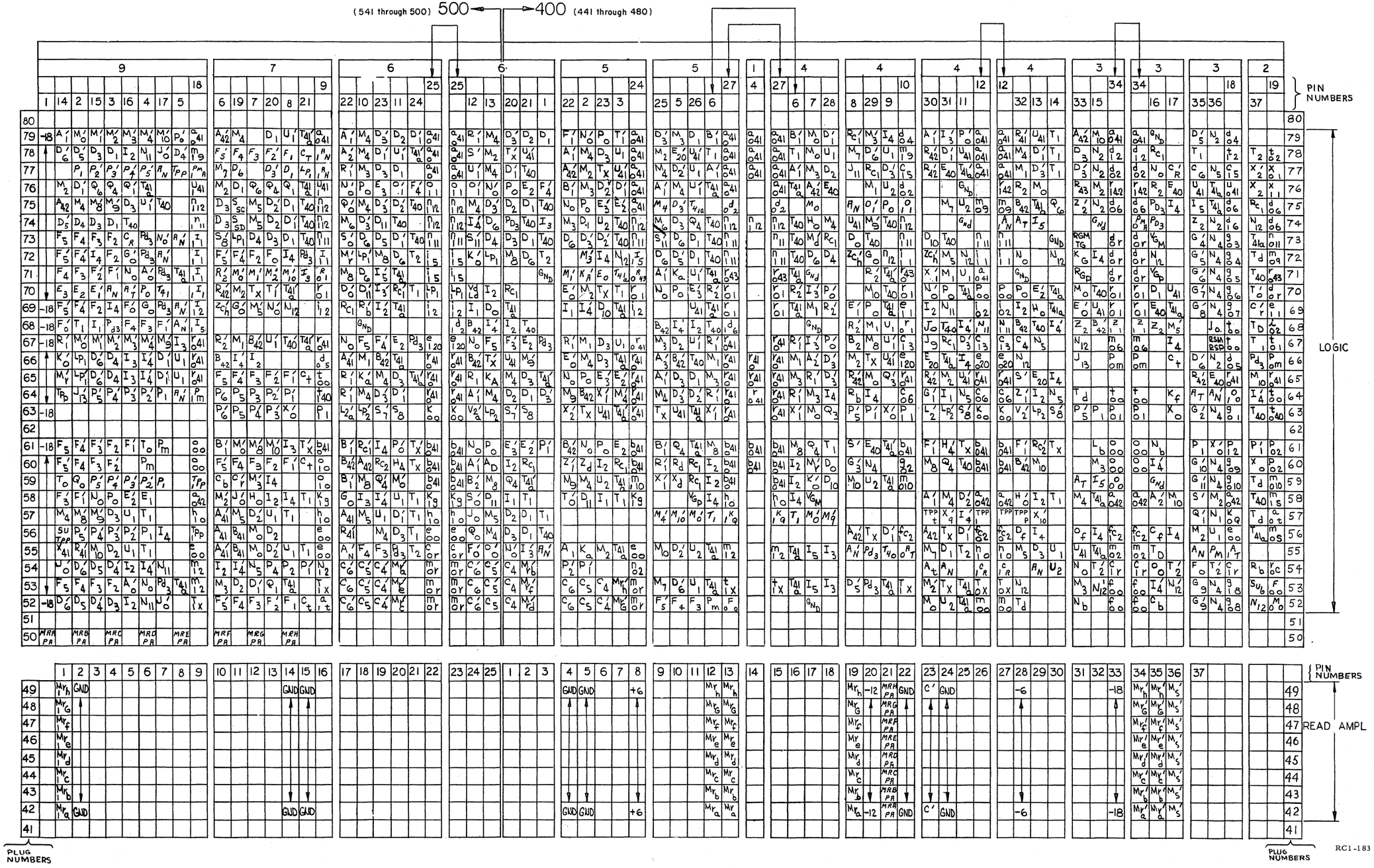

Figure 56. Circuit Board Connector Signal Chart No. 6