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MEM-BRAIN FILE

FOUR VERSIONS FOR DCA

Autonetics A DIVISION OF NORTH AMERICAN AVIATION, INC., ANAHEIM, CALIFORNIA

T5-1435/33
COPY 68

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FOUR VERSIONS FOR DCA

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Approved By:

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ABSTRACT

A large capacity, completely self-contained rotating disk file is currently being developed by Autonetics as a result of a direct continuation of thirteen years of experience in the design, development, and manufacture of disk memory systems for military markets. This new file, known as MEM-BRAIN, embodies a new disk form, a new head positioning principle, a different data buffering concept, and a larger data storage in a smaller package than any presently announced file. This unit, or one of three alternate lower capacity units based on the same principles, is proposed as a solution to the auxiliary storage problems recently discussed with DCA.

GLOSSARY

Access Time:

Read: The time between the instant at which information is called for and the instant at which it is delivered from storage.

Write: The time between the instant at which information is ready for storage and the instant at which it is stored.

Activity Ratio: The fraction of records with file activity in a given time period.

Address: A name or number which designates a register or a memory location. That part of an instruction which specifies the location of an operand.

Alpha-Numerics: Characters representing letters, numbers, or special symbols.

Auxiliary Storage: A storage, other than main memory, usually capable of holding larger amounts of information than the main memory, although with slower access.

Bit: One element of a binary code.

Block: A group of bytes, characters or words considered or transported as a unit.

Block Sort: A sort in which the file is "broken down" according to the characters of the key, and the separated parts are then sorted one at a time.

Block Transfer: The movement a data block from one area of storage to another.

Branch:

(noun): A point in a program at which one of two or more alternatives is chosen under control of the routine.

(verb): Jump.

Break Point: A point in a program at which special action is taken, such as a stop or a jump, often as the result of the setting of a switch.

Buffer Storage: Any device which stores information temporarily.

Byte: A group of bits taken together.

Cell: = Memory cell - Space allocated in memory for storage of one bit.

Channel: A circuit or route in a computer system through which data travels.

Characters: Elementry symbols (groups of bits) which in ordered groups express information.

Clear: To replace information in a storage device by zero or blank.

Clock: Equally spaced pulses used for master synchronization.

Code: A grouping of bits with a specific meaning.

Collate: To merge items from two or more similarly sequenced files into one.

Compare: Determining identity or relative magnitude.

Control Unit: Hardware which directs a sequence of automatic operations.

Core Storage: Storage with information held in the magnitization of magnetic cores.

Counter: A device in which numbers are altered by a unit increment or decrement.

Data: Information handled by a computer, as distinguished from instructions.

Data Processing: A generic term for the operations carried out on data.

Debugging: Determining, locating, and correcting errors of operation.

Decision: The operation of determining if certain relationships exist between words in memory or registers, and taking alternative courses of action.

Digit: One of the symbols 0, 1....9, or others used to designate each of the n quantities of the base n of the number.

Echo Check: Information is sent out, returned, and compared to ensure accuracy.

Erase: In magnetic recording, the removal of all information content.

Execution: Producing the result specified by the operation code of an instruction.

Extract: To read parts of a word as determined by a control pattern.

Field: A set of characters which is treated as a whole.

File: An organized collection of information directed toward some purpose.

File Activity: Any action upon the information in a file.

File Maintenance: The processing of a file required to handle the changes in it.

Format: The arrangement of lines, columns, fields, punctuation marks, etc.

Gas Bearing: A bearing in which gas is used as the lubricant.

Autolubricated: (Hydrodynamic) The support is derived from the relative motion.

Hydrostatic: The lubricant is supplied under pressure from an external source.

Hardware: Machine or mechanism, including electronics. Contrasted with software.

Housekeeping: Parts of a program which are not directly in the solution of the problem but are made necessary by the method of operation of the machine.

Index Register: A device which holds data addresses offset from their callout.

Information: A collection of facts, data, records, characters, bits, etc.

Instruction: A set of characters which, as a unit, causes a machine to perform one of its operations. (Preferred to "command" and "order".)

Interrecord Gap: An interval in a sequential store which contains no data. Separates records.

Item Advance: A technique for operating successively on records in memory.

Iteration: The techniques of repeating a group of instructions; one repetition.

Jump: (noun): A jump instruction.

(verb): To break out of the one-after-the-other sequence of instructions.

Key: The field(s) by which a record is identified and/or controlled.

Label: A part of a record used to identify the record's contents.

Linkage: A technique for providing a re-entry to a storage location.

Location: A place in which information may be stored; identified by an address.

Logical Operations: Operations which are Boolean in nature, such as "and", "or", extract, and decision. Contrasted to arithmetic operations.

Magnetic Disk: A storage device or system in which information is recorded on the magnetizable surface of a rotating disk.

Mask: The coding used for extract.

MCP: (Master Control Program) (Executive Routine): A routine which "directs" the operation of other routines.

Memory: Storage associated with a computation center.

Memory Dump: A listing of the contents of storage.

Merge: To combine items from two or more similarly sequenced files into one sequenced file, including all items from the original files.

Multiplex: To carry out two or more functions time shared.

Nonvolatile Memory: Storage which retains information when power is removed.

Off-Line: Operation of I/O and other devices not under direct computer control.

On-Line: Operation of peripherals under computer control.

Origin: The absolute memory address to which addresses in a region are referenced.

Parallel Transfer: Simultaneous data transfer of elements of information.

Parity Digit, Parity Bit: A bit (0 or 1) added to a group of data bits to produce a chosen "evenness" or "oddness" of the number of one's in the total group.

Peripheral: Refers to parts used with but not in the "main frame" of a computer.

Program: A complete plan of attack on a problem (may include flow charts and routines).

Random Access Storage: A store with access time independent of the address.

Rapid Access Loop: (recirculating loop, revolver). A small section of a sequential access memory in which data is reviewed often.

Read: To transcribe from storage.

Read Head: An electromagnetic device which produces a voltage output in response to a change in the state of magnetization of the record passing under it.

Recirculating Loop: See "Rapid Access Loop."

Record: (noun): Item; a collection of fields.

(verb): To transcribe into storage.

Register: The hardware for temporarily storing information.

Reset: (Clear). To return a location or device to an initial condition.

Revolver: See "Rapid Access Loop."

Search: To locate a desired word or record in a set of words or records.

Sequential Access Storage: A storage in a one-after-the-other sequence.

Serial Storage: See "Sequential Access Storage."

Signal: The output of a circuit, used for control and/or timing.

Software: A term applied to programs and logic (contrasted to hardware).

Storage (Memory): A device which holds information and returns it unaltered.

Store: (noun) A storage device.

(verb) To transfer information to storage.

String: A set of records which is in ascending (or descending) sequence.

Synchronous: All operations are controlled by a clock.

Systems Approach: Looking at the overall situation rather than the narrow implications of the task at hand; looking for interrelationships between the task at hand and the other functions.

Track: The region reviewed by a stationary head in a disk memory.

Volatile Memory: A storage in which information is lost when power is removed.

Word: A set of characters or bits which is treated by the machine as a unit.

Word Length: The number of bits in a word.

Write: To transfer into storage.

Write Head: An electromagnetic device which produces a change in the state of magnetization of the medium passing under it in response to an input current.

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I. INTRODUCTION

A. PURPOSE

This document describes how Autonetics proposes to adapt the company-funded (in-house) 2 gigabit MEM-BRAIN File development to the mass storage problems which have been discussed informally with DCA. Units of four different sizes have been considered. The two smaller units (200 million and 400 million bits) are basic storage for use under detail control of the system computation center(s). The two larger units (one and two billion bits) have the complete internal operational capability of the basic MEM-BRAIN design. They can do much of the internal file organization and management under their own internal stored program control. Therefore, the system computation center(s) will be freed from detail file control. Simple "generic" commands from the computer will serve to control storage or retrieval, after initially loading the unit with the desired program.

A hypothetical civilian problem is described, which Autonetics understands from the referenced discussions to approximate the actual DCA problem. The proposed units are well adapted in speed, capacity, and data organization to the auxiliary storage requirements associated with processing such problems.

B. MEM-BRAIN FILE CONCEPTS

1. Mechanical

The mechanical design of MEM-BRAIN depends on the high stiffness to mass ratio of a pretensioned membrane. This property is employed both in the disk form and in the principal support structure for the rotating mass (the disk stack). This leads to an inside-out structure relative to conventional disk files. Each disk is a thin annular sheet of magnetically plated foil stretched over a tensioning hoop to provide a rigid surface of uniform flatness. A unique feature of this structure is its tolerance to extreme thermal variations without distortion. The principal support structure of the rotating disk stack is formed of pretensioned pairs of conical sheets. This provides extremely high rigidity in both axial and radial directions. The opposite end of the disk stack is located by a flat membrane-type support to complete the kinematic mounting.

The main memory is accessed by internally mounted arms which provide simultaneous radial motion of groups of 8 magnetic read-write heads across the two facing surfaces of adjacent disks. At one end of the disk stack a group of fixed heads is provided to handle internal control and bookkeeping.

The entire disk stack and head assembly is enclosed in the hermetically sealed portion of the frame.

2. Electrical

The basic (two gigabit) MEM-BRAIN unit has sixty-four I/O data channels, each capable of transmitting data to or from storage. Associated with these are four I/O control registers to direct these data. Sufficient electronics, logic, and control is included to permit simultaneous motion of four arms. The arm servos are capable of transferring heads from one set of tracks to any other in less time than one disk revolution. Data organization requirements are very flexible (fixed or variable word, parallel by byte, serial by byte, parallel by bit, serial by bit, etc.). The only fundamental restriction is associated with the relationship between sector length in main memory and short loop length in the fixed head section of the unit.

The electronic elements of the file are located at one end of the main frame accessible for service, in an enclosure which is dust- and drip-proof but not hermetically sealed.

3. Adaptations to Smaller Units

The only mechanical changes required to adapt the MEM-BRAIN principle to smaller capacity requirements are the reduction in the number of memory disks and the corresponding shortening of the overall structure. Electrical changes are more numerous. For all smaller sizes, the number of I/O control registers is reduced to two. For the smallest units, the internal electronics, logic, and control are minimized.

4. Capacities

Table 1 tabulates the capacity of each of the four proposed units, not only in total but in various groupings which indicate data accessible without servo action.

Table 1. Data Capacities

Total File Capacity		$3x2^{26}$ bits (201, 326, 592)	$3x2^{27}$ bits (402, 653, 184)	$15x2^{26}$ bits (1, 006, 632, 960)	$15x2^{27}$ bits (2, 013, 265, 920)
bit/track		2^{14} (16, 384)	---	---	---
128-bit records/track		2^{7} (128)	---	---	---
32-bit words/track		2^{9} (512)	---	---	---
bits/arm	with all heads in fixed positions (all head transports at rest)	2^{17} (131, 072)	---	---	---
128-bit records/arm		2^{10} (1024)	---	---	---
32-bit words/arm		2^{12} (4096)	---	---	---
bits/file		$3x2^{18}$ (786, 432)	$3x2^{19}$ (1, 572, 864)	$15x2^{18}$ (3, 932, 216)	$15x2^{19}$ (7, 864, 432)
128-bit records/file		$3x2^{11}$ (6, 144)	$3x2^{12}$ (12, 288)	$15x2^{11}$ (30, 720)	$15x2^{12}$ (61, 440)
32-bit words/file		$3x2^{13}$ (24, 576)	$3x2^{14}$ (49, 152)	$15x2^{13}$ (122, 880)	$15x2^{14}$ (245, 760)

NOTE: Data on the first six lines are common to all four units.

5. Reliability

The basic MEM-BRAIN concept was aimed at military applications. Therefore, both it and the adaptations proposed herein have used as criteria for design decisions the extensive background in military computer memory work accumulated by Autonetics. These criteria include methods of design for high reliability, for ease of service of elements requiring preventive maintenance, and techniques necessary to insure high tolerance to adverse environmental conditions. Designs are based on MIL E 5400G; FED STD 222 and MIL Q 9858A.

C. QUANTITATIVE EXAMPLES

A few specific numbers may clarify the foregoing qualitative discussion:

1. Assuming 8 bits are used for each alpha-numeric, the smallest unit can store the equivalent of some 1300 pages of standard telephone directory. This is approximately the size of the Los Angeles Central Section directory. The largest unit has ten times this capacity, sufficient to store the telephone directory for a city requiring 7,000,000 entries.

2. All units can store or deliver data at a rate in excess of 10,000,000 bits/sec. Any bit in the file is accessible in less than 0.1 sec. A total memory readout of the 2×10^9 bit unit can be completed in 100 sec.

3. A useful content search of the entire 2×10^9 bit file can be accomplished in 16 seconds, if the data has been properly structured for such a search (records of approximately 1000 characters each, search based on 32-bit fields in these records, for example). This is based on the adjacent track access time of .004 seconds.

4. Mechanical stiffness of the end bell is least in the axial direction, where the spring rate may be expressed as .025 in/ton. Torsional stiffness of the longest disk pack will limit relative deflection from end to end to less than 10% of a data cell.

5. Reliability of the complete units as proposed is conservatively predicted* to range from 3200 hours MTBF for the largest unit to 6800 hours for the smallest. If a full reliability program (of MINUTEMAN class) were undertaken, these figures would rise to 6700 hours and 10,300 hours, respectively.

6. Maintenance is expected to require an average of approximately 1 hr. per month, total of scheduled and unscheduled.

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*Corresponding predictions on the MINUTEMAN program underestimated MTBF relative to subsequent experience by a factor of at least 3 for the memory unit.

II. PROGRAM DESCRIPTION

A. AUTONETICS MEM-BRAIN FILE PROGRAM

In 1960 Autonetics became aware of an almost total lack of militarily fieldable peripheral equipment for data processing systems. A highly successful background in militarized disk memories utilizing air bearings for stability and magnetic surface recording for information storage and retrieval led to the decision to concentrate on a rotating disk auxiliary storage unit for military applications. Exhaustive studies were made to determine the requirements of such a mass storage element for military electronic data processing systems. Concurrent studies showed the poor chance of meeting these requirements by upgrading equipment presently available or about to be offered by the industry, and led to the conclusion that a very drastic change in characteristics was essential if this problem was to be reasonably solved. A completely new attack on such characteristics as form, shape, logical flow, and maintenance philosophy appeared necessary. Based on these studies, the MEM-BRAIN file concept was evolved. The concept included a capacity of two gigabits and considerable internal operational capability to allow for foreseeable military growth within reasonable (state-of-the-art) size and weight.

Based on this concept, as embodied in a preliminary design, a company-funded development program began late in 1963. The initial phase of this program included computer simulations, model tests and material investigations, and demonstrated the feasibility of the concept and of a reduction in disk size from 42" to 23". Subsequent work has been directed toward development and construction of a design proofing model with 33 million bits capacity. Concurrent studies of the software aspects of the MEM-BRAIN concept have elucidated the simplifications and increased flexibility of use resulting from provision of some fixed head operational capacity. Many alternate internal capabilities are possible without upsetting the primary advantage of the electromechanical design of this unit.

Emphasis in the Autonetics MEM-BRAIN File program has been placed on the following factors, deemed necessary or desirable in an auxiliary store for military data processing systems:

1. Tolerance to military environments:

    a. Extremes of shock and vibration

b. High and low temperatures and temperature changes
c. Humidity and other weather factors

2. High MTBF

3. Internal data manipulation to unload the system computation center(s).

4. Reduction in size, weight and power required

5. Large capacity (number of bits)

6. Maintainability

B. OUTLINE OF ADAPTATIONS

This document describes design adaptations of the MEM-BRAIN File to the data storage requirements of DCA as Autonetics understands them. Two smaller units, being as simple as possible, are direct fetch-put stores. They can be viewed at the interface as equivalent to a number of drum files. These smaller units provide only the controls necessary for directly accessing any portion of the file with reasonable rapidity and high veracity. Two larger units include electronics and logic for stored program control to improve efficiency (from a maintenance, MTBF, and data throughout standpoint).

This choice of unit capabilities results from Autonetics' estimate that storage capacities less than one gigabit probably would not justify the cost of internal program control which would be reasonable for larger units. As can be seen from Table 2, capacity in bits per unit of size, weight and power increases with the size of the unit. The magnitude of these changes would be much more drastic if the same internal control capability had been included in all units.

C. AIRBORNE APPLICATION

The shake, rattle and roll environment to which equipment is subjected in military aircraft, dictates a design which has a stiffness to mass ratio that is as high as possible and extreme damping (high logarithmic decrement or low Q). The design must give the recording heads sufficient mechanical fidelity to follow the recording surface without undue signal modulation. Phase (jitter) modulation is more critical than amplitude modulation. This has been a major consideration in the selection of MEM-BRAIN parameters.

Table 2. MEM-BRAIN Characteristics

Description	Total Data Bit Capacity	Number of Disks	Size (Inches)	weight (Pounds)	Power (Watts)	Bits/cu ft ($\times 10^6$)	Bits/lb ($\times 10^6$)	Bits/watt ($\times 10^6$)
6-arm Unit	3×2^{26} bits (201, 326, 592)	7	23x23x11	90	700	66	2.2	.3
12-arm Unit	3×2^{27} bits (402, 653, 184)	13	23x23x14	150	800	110	2.7	.5
30-arm Unit	15×2^{26} bits (1, 006, 632, 960)	31	23x23x23	250	1200	170	4	.8
60-arm Unit	15×2^{27} bits (2, 013, 265, 920)	61	23x23x38	400	1500	210	5	1.3

The external shaft design gives the disks of the file an unexcelled torsional stiffness to mass ratio for a given volume. The relatively great shrinkage-expansion spring stiffness of the external shaft, combined with lightweight preloaded disks, gives a resultant recording surface stiffness far higher than that of any thick disk, center shaft design. The mass of the thin foil disk structure is orders of magnitude less than that of any thick disk design. The integral motor minimizes injection of vibration modes from drive power by eliminating flutter and wow due to such drive train elements as gears and belts. Mounting the rotating element on a preloaded double disk diaphragm at one end and a single diaphragm at the other gives a minimum mass kinematic support which is tolerant of construction, assembly and installation misalinements and low frequency elastic deflections. The small physical size and low total weight of the complete unit allow it to be mounted and demounted, through normal access hatches without special equipment, in many different vehicles.

D. MULTIPLE COMPUTERS

The multiplicity of I/O control registers and I/O data channels permits direct connection to two computation centers (four in the largest unit). These centers can operate as independent controls over and upon the data in the storage units. Neither of the computation center's control programs need be aware of the other's existence in most normal problem handling. Two conditions do exist, however, in which one of the computation centers can get in another's way. The first of these occurs when the machines command an individual head positioner to two separate locations. Under this condition one or the other must wait its turn, and so a basis of priority must be established, tested, and operated upon. The other condition exists when, in a large program, the two computation centers are both working on the same data. If one is altering the data and the other is using the data, it is possible that the data being used will not correlate because some of it will come from old (not updated) storage and some will come from new (just updated) storage. A special security interlock is used to flag this problem. Tags are placed on data blocks indicating the signature of the last writer in that file. If a computation center wishes to be certain that its data are not being modified, it writes its signature in this block before using the data, and each time it uses the data, it inspects this block to ascertain if its signature is still there. If so, no write entries have been made.

E. UTILITY EXAMPLE

To avoid need for classified information, a civilian problem is cited as an example of MEM-BRAIN File utility in this proposal to DCA. This problem is the maintenance of a comprehensive directory for a medium-sized city. The entries in this directory are more complex than name, address, and telephone number. Each consists of about 1,000 characters of data, reasonably well structured and organized. The data include such items as number of members in the family, profession and interest of these members, facilities in the house, and activity numbers on the phone. Further, it is assumed that at irregular but frequent intervals, unchanged family units move to another house which has different facility characteristics with a different address and a different phone number, that entire groups of families such as the occupants of a "company town" covering an area of two or three blocks move out and other families move into the same quarters, sometimes picking up the old telephone numbers and sometimes not. Furthermore, at irregular but frequent intervals whole street names may be changed or the addressing scheme of the entire city or a portion thereof is altered by executive fiat. Besides the file maintenance to keep these data correct, assume that queries will be made rather frequently, and in fact, the main purpose of the file is to answer these queries which are analogous to, "If baseball became extremely popular, what would be the utilization of baseball fields located at various places if they were to have Little League players come from five blocks away, high school intramural players come from three miles away, and collegiate teams come from half the city?" Or, if the emergency demanded it, what distribution would be possible for the doctors in the city so that a minimum distance would exist between the location of any probable injury and the nearest doctor?

All proposed MEM-BRAIN File units have the speed and capacity needed for auxiliary storage in data systems required to handle this class of problem. The two larger units, by virtue of increased capacity and internal data organizational capability, could handle materially larger "cities" than the smaller units. Specifically, the capacities of the four units at 1000 characters per entry will handle maximum populations of about 25,000, 50,000, 125,000 and 250,000 respectively.

F. CORRELATION OF MEM-BRAIN AND DCA NEEDS

As Autonetics understands the mass storage problem with which DCA is concerned, it appears to correlate closely with the reasoning which led to development of the MEM-BRAIN concept. Militarization has been a fundamental criterion in the establishment of MEM-BRAIN principles. So also have minimum size and weight to permit airborne

use. The basic MEM-BRAIN capacity target is at the upper end of the range of values in which DCA has expressed an interest.

The MEM-BRAIN file concept has electromechanical advantages for military use in the three areas of cost, reliability and ruggedness. Cost per bit is expressed in terms of size, weight and power as well as in cents per bit. The design emphasizes fundamental simplicity for the required task in order to provide the maximum potential for overall reliability. In combination with the requirements for compactness and light weight, the design contemplates optimum use of material properties to provide a rugged unit capable of withstanding the military shock and vibration environment. Fundamental knowledge which led to the development of a disk memory which survived a missile crash* with data still readable, has been applied to the task of developing a rugged and reliable large-scale storage unit.

The basic two gigabit concept is particularly adaptable to the use of internal stored program control and data manipulation. This enhances its capability for working with numerous data channels associated with multiple computers or other peripheral equipment. It also reduces the time demands on the associated computer for detailed control of the data store. It obviously is adapted to handling problems which require the use of a very large data base.

The chief features of the MEM-BRAIN concept are readily adaptable to smaller units such as have been discussed with DCA. Problems appropriate to such smaller units can probably afford the use of more computer time for detailed control so that less internal control capacity is required. Since internal control capability is a relatively expensive portion of the entire device, such a reduction can keep the cost per bit to a reasonable value. However, the main storage techniques used for the large unit are directly adaptable to the smaller units by a mere reduction in number of disks.

From Autonetics' point of view, development of units explicitly directed at DCA's problem provides a definite target for the design stage of the program and would, therefore, be a natural effort to undertake in the overall MEM-BRAIN development.

G. PLAN OF ATTACK

The development and construction of these units will be as engineering models. The design of the units will conform to all applicable portions of Military specifications, but there is neither time nor money provided in the proposed development, manufacture, assembly

*See Appendix I

and test effort to run a complete environmental assurance program. All of the units defined are electromechanically as similar as possible to the present two gigabit unit (under development). This commonality makes all but the electrical-information interface a direct result of the present development. One reason for this choice of program is to gain experience of maximum utility to the basic Autonetics two gigabit program without jeopardizing the specific DCA objectives.

III. DESCRIPTION OF MEM-BRAIN

A. FUNDAMENTAL CONSIDERATIONS

Selection of the storage medium for a large-scale auxiliary file is extremely important because the whole electronic data processing system organization can depend upon its characteristics.

In selecting the storage medium, many types were considered. A prime requirement of a high reliability memory is nondestructive readout (NDRO) to eliminate possibility of system malfunction due to improper rewriting of information. Lumped element storage media such as cores, spots, biaxes, bouncers, etc., are undesirable in mass storage systems because their individuality leads to an ensemble of characteristics (probability of failure, unit cost, unit volume, assembly manpower, etc.) which is detrimental to the overall design. Magnetic recording on a surface which rotates under a magnetic head provides NDRO and time-cyclic review. A cyclic (rotating) memory usually is considered to have a disadvantage in access time due to the sequential nature of its access along a track. In a large storage system properly organized, this can be more of an attribute than a deficit. The control for data location along a given track or series of tracks can be greatly simplified and completely hardware implemented. Track-to-track transfer is random, with an access time which is a function of the relative addresses of the old and new tracks. There are three forms of magnetic recording currently in use---magnetic tape loops, magnetic drums and magnetic disks. Of these, the magnetic disk can be smaller, lighter, and more tolerant of high packing densities under the extremes of vibration, shock, and humidity than tapes or drums. Head-per-track systems, head-per-zone systems, head-per-disk-surface systems, and head-per-disk-stack systems with various controls on the head-track selection scheme exist.

Autonetics chose head-per-zone synchronous recording with four zones at the same angular cell density (same bit rate) as a compromise between cost, reliability, access time, latency time, and master control program time. Eight tracks (one head per track) on two facing disk surfaces are accessed simultaneously by a single arm. The number of arms is equal to the number of facing disk surface pairs for each unit, and each can be positioned to access the various tracks independently. The MEM-BRAIN file includes a modest amount of I/O scheduling, formatting, and controlling capability to enhance the average throughput data rate possible, with minimum

attention from the master control program of the data processing system. This random sequential data storage form costs less and has higher reliability than a true random access file, because the addressing and bookkeeping equipment is much simpler.

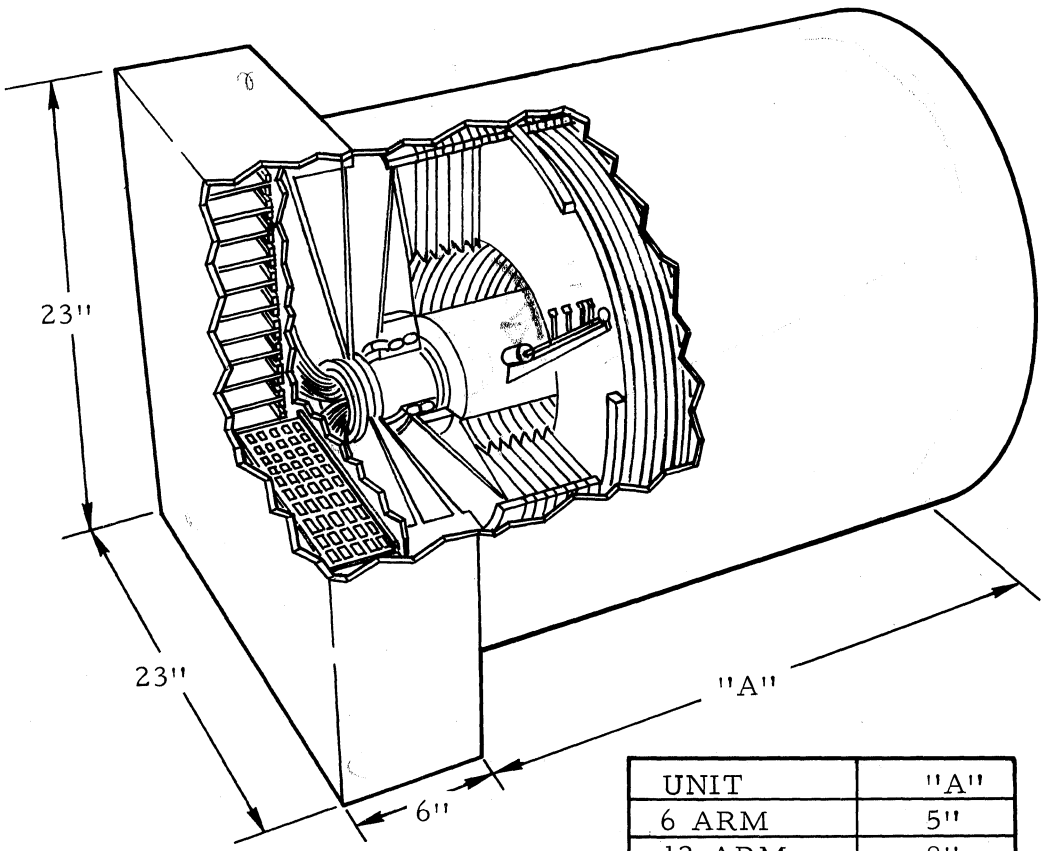
B. MECHANICAL FEATURES

The mechanical design of MEM-BRAIN depends on the high stiffness to mass ratio of a pretensioned membrane both for the disks and for the principle support structure for the rotating mass (the disk stack). This principle leads to an inside-out form for the disk. The disk is mounted and rotated from the periphery and accessed from the center, as shown in Figure 3. The disks are thin annular sheets of magnetically plated foil, each stretched taut over a tensioning hoop. The tensile preload established by this process causes the plated membrane to act as a rigid surface of uniform flatness. This eliminates surface finishing operations. Such a membrane has tolerance to extreme thermal variations without distortion out of plane. This property and the minimum mass of the disk (approximately two orders of magnitude less than a standard disk) lead to the militarized qualities of the MEM-BRAIN File.

The disk stack forms a cylinder which is closed around the periphery. Radial air flow is thus minimized and the usual siren effect of a standard disk stack is virtually eliminated. This disk stack is driven by a synchronous motor which combines with the high moment of inertia to mass ratio of the disk stack to provide a highly uniform rate of rotation.

One end of the disk stack is constructed of a pretensioned pair of shallow coned metal sheets. This forms a light end bell which provides extremely high rigidity in both axial and radial planes. This end bell is carried by a bearing supported by a similar conical pair. The two units are oppositely configured, one having maximum separation at the periphery, the other at the hub. Three degrees of freedom are thus constrained. The other end of the disk stack is supported by a bearing attached to a flat membrane, to complete a five degree of freedom kinematic mount. The sixth degree of freedom is the desired rotation.

The low mass and high stiffness of the dynamic element just described provides a mechanism having high natural frequency and low vibration amplitude. By judicious application of viscoelastic coatings, the mechanical Q of the structure is kept well below the critical



UNIT	"A"
6 ARM	5"
12 ARM	8"
30 ARM	17"
60 ARM	32"

Figure 1. MEM-BRAIN File - Physical Configuration

damping value. The four units proposed all use the same electro-mechanical and magnetic elements. All are similarly packaged with the electronic elements in a rectangular box 23" x 23" x 6" and the electromechanical portion contained in a 23" diameter cylindrical extension whose length varies from 5" to 32" in accordance with the required disk stack length. All use the same head positioning servo, using track-seeking and track-centering for servo control. All are provided with fixed heads associated with one rotating disk surface. Clock, sector, origin and the short loops utilized in the head servos are included in all four units. The two larger units also have a number of fixed head rapid access loops which are used for formatting, editing, bookkeeping, and other I/O control functions.

Each of the movable head arms comprises a light tubular member supported on an internal gas bearing and driven by a "voice coil" servo motor. Each of these tubular arms carries eight read-write heads

on flexible support drag links with suitable means for forcing them toward the facing surfaces of two adjacent disks (four heads per disk surface). The heads are attached to pads which furnish an air bearing support to maintain accurate head spacing from the rotating disk surfaces. The entire assemblage is supported by a rigid structural member attached to the central structural frame of the disk pack unit. The four heads facing one disk surface are equally spaced at a separation corresponding to the zone width of the record pattern. Therefore, the distance through which the servo motor must drive the heads is one zone width.

A unique NRZ phase recording technique was developed for this unit to permit the servo positioning signals to be derived from the output of the heads. This involves effectively displacing the bit pattern of some tracks by 90 electrical degrees relative to other tracks. Suitable processing and rectification of the signals from a plurality of heads serve to give both error signal and sense for the final track-seeking operation of the servo. For gross movements a track-counting technique is used and the servo motor is driven at maximum input to accelerate the arm for approximately one-half the total number of tracks following which it is reversed to decelerate the arm to essentially zero velocity as the desired track is approached. At this point the track-seeking function takes over.

Each arm is equipped with a brake which serves to hold it in position once the servo has attained the proper location. By this means the electronic elements of the servo can be released and switched under I/O register control to position a different arm.

At one end of the disk stack a group of fixed heads are located. These are gas bearing supported on flexible drag links against the exterior surface of the end disk. These head units are supported by a plurality of rigid structural members attached to the central structure and are located and spaced to provide rapid access and buffer loop capability as required for the respective units. In function the support for these fixed heads is equivalent to a solid headplate such as has been used in Autonetics computer memories, but it is structurally segmented to permit removal and replacement for service from the center of the undisturbed disk stack.

C. ELECTRONIC DESIGN

The basic storage function of all units is accomplished on the disks accessed by movable heads. All built-in control functions are

provided by the fixed head elements and associated electronics. Clock, sector and origin are provided by (permanent) records on fixed head tracks (read only).

In the basic 60-arm unit the combination of the fixed head elements with other electronics provides capability for bookkeeping, formatting, and other functions and for storage of an internal program to control these operations. Additional electronics includes the necessary read and write amplifiers, together with a small amount of core buffer and logic and switching networks. These provide the I/O control registers as well as the necessary means for transfer and handling of data between fixed head storage elements and between fixed head and moveable head storage. The electronic package also includes the elements of the arm servos which are switched from arm to arm. A program stored in the fixed head area may be inserted and changed at will by the central processor(s) with which the unit is associated. These facilities are capable of performing automatic and continuous on-line file maintenance, record manipulation, data formatting and editing, sorting, merging, collating and other list processing operations and permit direct interfacing with other peripheral units without need for detail action on the part of the central processor. All circuitry uses advanced state-of-the-art techniques in microminiaturization and replaceable circuit board assemblies to maximize MTBF and minimize service time.

The electronics of each head transport servo automatically inspects the I/O control registers for further instructions as soon as it completes positioning one arm. The maximum time required for movement of an arm from one position to any other is less than required for one disk revolution. Thus the maximum rate of execution of discrete position changes is greater than 40 per second. By the nature of these units all of the data from all of the I/O channels and all of the read-write stations is in synchronism. This allows for the parallel transport of data to and from the files if desired and properly called for.

D. SIZE ADAPTATION FEATURES

In adapting the two gigabit file to smaller sizes, nearly all of the electromechanical, data recording, servo manipulation, integrated circuit, code conversion, environmental integrity, and other design features remain unchanged. The various units utilize the same recording scheme, the same recording density, the same recording code, the same data layout, the same disks, the same heads, the same arms, and essentially the same mounting, stacking, and

holding provisions. In this manner the units, which vary in size from $3x2^{26}$ bits to $15x2^{27}$ bits, vary mainly in the number of independent head arms and magnetic recording disks in the stack.

The 6-arm and 12-arm units are proposed as put-fetch stores only. The 30-arm and 60-arm units will have a considerable capability for data manipulation, data format, and data scheduling included as an integral part of the system. These storage units all operate as synchronous, sequential access units for any given channel, and the synchronous, sequential nature of the data permits its manipulation and control without undue hardware complications when the control and temporary storage is handled and manipulated in like manner. The kinematics of arms and disks is such as to include two disk surfaces in each file which are inaccessible to the roving arm heads of the basic storage unit. A small portion of one of these disks is used for timing and storage and manipulation of servoing data. This surface has a total capacity of 17 million bits which permits its economic use for temporary recirculating and manipulating storage in addition. This capability, which is included in the two larger units, comes at comparatively low equipment cost due to the extreme simplicity of data manipulation in sequential strings when the data is synchronized.

All units are capable of storing or delivering data at a rate in excess of 10,000,000 bits/sec. Any bit in the entire data store is accessible in less than 0.1 second.

IV. LOGICAL ORGANIZATION

A. BASIC CAPABILITIES

The internal organization of these four proposed units is identical in its basic memory area and different in its I/O interface and bookkeeping area. The number of head arms varies from 6 to 60, but the method of directing and controlling the head positioners is identical inside the machine. The form, fit and function of data and format in the basic storage is the same in all models. Signal levels involved are identical in all models and all I/O channels. However, the I/O interface for each of these units is distinctly different. The I/O interface consists of I/O control registers and I/O data channels.

The I/O control registers serve as buffers for address information, to assure that the proper head(s) is positioned on the proper track(s) and connected to the proper I/O channel(s). In the two larger units they also alternatively control the routing of data to and from the internal manipulative elements.

Each I/O data channel consists of two input lines and one output line. The read signal on the output line is either at 0 volts to signify a "0" or at -6 volts to signify a "1." A signal of -6 volts on either input line calls for writing a bit of information, while a 0 volt level is a non-write condition. When activated, one line causes the unit to write a "0"; the other line causes a "1." Associated with each I/O channel (or, in some cases, groups of channels) is a signal line which is activated whenever some internal action is taking place which would render data from that channel invalid. Such conditions include head transport in motion or channel being used by another control element. External connections are provided to supply clock, sector counter and sector strobe signals for use of the central processor (or other peripherals).

In the two larger units a core buffer proposed as having a capacity of 256 16-bit words is provided for use with each I/O control register and its data I/O circuits to permit direct connection between the synchronous internal organization of the MEM-BRAIN unit and external elements of the system, which may be asynchronous or synchronized to a different clock.

In the basic storage region each arm has access to 256 groups of 8 tracks on the facing surfaces of two disks. Each track is currently

thought of as divided into 128 sectors, each sector containing space for 128 bits of information with four-bit gaps between sectors. The number of sectors and bits per sector is controlled by the sector track pre-recorded on the fixed head disk and, therefore, this sector and record length organization can be modified by different recording in the initial fabrication of the machine or by a subsequent "factory type" service operation. As this organization must be compatible with the short loop structure and sector counter capacity of the "fixed head" elements, such later modification is more restricted than in the initial design. Any change in the sector number and length may modify the total number of useful bits of information available to each arm. In the current plan, this number is $2^{25} = 33,554,432$.

B. ADDITIONAL CAPABILITIES OF THE 30- AND 60-ARM UNITS

The provision of additional fixed heads and short loop segments on the two larger units provides capabilities for internal data manipulation. Rapid review of the data in a portion of the basic storage is simply accomplished by copying the data in question into the fixed head storage element where it can be reread by additional heads circumferentially distributed along the corresponding tracks. Data may be reordered in sequence or position by appropriate recirculation of the data from one of these additional read heads to another write head with appropriate recirculation control By proper control of this type of operation, any desired record intermix can be obtained. As a specific example, segments of two records of suitable format may be combined in alternating order in the time required for two disk revolutions. A short recirculation loop can be used to make a given record (of length no greater than the length of the loop) available for serial manipulation once during each recirculation interval. The fixed head equipment can also be used as a temporary storage or buffer for information, pending transfer to or from movable arm storage. A more detailed description of some of these operations is given in Appendix III. The use of fixed head equipment for operations of these types is more economical by any measure than any other known method. The primary additional cost is involved in equipment for reading, writing, and controlling the data flow. The controls can effect a great deal of information with comparatively little hardware because of the sequential nature of the operations. In the MEM-BRAIN design the basic recording medium is essentially free because in fabrication of the recording disks, both sides are plated simultaneously and the outside face of an end disk is not otherwise accessed.

C. EXAMPLE

In terms of the "civilian problem" previously described, these operations of the larger units may be more explicitly exemplified. It is assumed that the directory data is located in the file in order of the social security number of the head of the household. Solution of many facets of the problem therefore requires the limited content search capability which is included in the internally stored program. Suppose that the "baseball field problem" were to arise. Instructions to the MEM-BRAIN file could call for a tally of the number of boys in each of three specified age groups that are located in each of a group of areas defined by street names and address ranges. Such an instruction could be automatically executed within the MEM-BRAIN unit by a search of the entire file. If this particular problem had been anticipated at the time of setting up the stored program, a reduction in search time could be achieved by having the appropriate data located in a subset of the entire file. For example, in the baseball field case, the city might have initially been subdivided into districts and the question might be asked with respect to only one of these districts. The current estimate of the equipment required to perform the content search corresponding to this problem, in addition to the minimal buffering requirements, is five recirculating loops and some logic. The same equipment could be used with only a minor variation in the logic (provided by stored program instruction) to solve other related problems on a time-share basis. Consequently, provision of such capability need not be charged to a single facet of the overall problem. For example, the rearrangement of the file required to handle the movement of groups of families, as mentioned in the problem description, can be covered by essentially the same equipment. In this case, change or alteration of a record can be performed in a systematic search manner without direct supervision by the system's master control program (external to the MEM-BRAIN file). Evidently, any request for data directly correlated with a specific list of social security numbers requires only a simple address access for response.

In the largest unit, a complete serial content search of the file (2 gigabits) can be accomplished in 16 seconds, if the data has been properly structured for optimal access. For the simplest (identity) search criterion on a small field, two tracks of fixed head storage and associated logic will be needed. More complex criteria can be handled by the use of additional fixed head equipment, without affecting search time.

V. INTERFACE WITH OTHER UNITS

A. HARDWARE

The general internal organization of the MEM-BRAIN File units is indicated in the functional schematics, Figures 2 and 3. These are respectively for the smallest and largest of the four units under consideration. In these figures the blocks which appear closest to the viewer symbolize the interface connectors. The basic data channels are shown at the extreme right of each figure, while the control and external signal blocks are shown at the extreme left and intermediate left, respectively. In the simplest unit there is a one-to-one correspondence between heads and data channels as symbolized by the six lines (one per arm) entering the I/O data channel block. Two I/O control registers are provided for the receipt and interpretation of instructions from the outside source. The arm motion indicator provides a signal to warn the user if invalid data may be appearing, on an output data channel, as a result of action of an arm servo. The signal alternatively will indicate that the unit is not yet ready to receive input data if a write instruction has been called for. In the simplest unit, there is one such indicator per arm. The remaining three boxes indicate connections, which provide the internal clock, sector counter, and sector strobe signals for the information of the external equipment. The sector counter is arranged to change its indication, approximately midway through the sector currently being read, to the designation of the next sector to appear. The sector strobe signals indicate the actual beginning of the sector whose number appears in the sector counter at the time they are produced. Separate strobes are provided for read and write operations. To avoid complication of the figures, the internal connections for use of the clock and sector channels are not shown.

In all except the smallest unit internal switching occurs between heads and external data channels. This is symbolized in the functional schematic of the 60-arm unit by showing four separate I/O data channel blocks. Each block corresponds to 16 I/O channels. In parallel with the data channels, four I/O control registers are provided. Each I/O control register has access to only its corresponding group of 16 I/O data channels but has access to all other internal functions. These registers are capable of controlling not only the positioning of the arms but also the switching of head-to-data-channel connections. They also accept and transmit the necessary instructions to control the internal data manipulation on the fixed head equipment. The external signal blocks (clock, etc.) are the same in all four units.

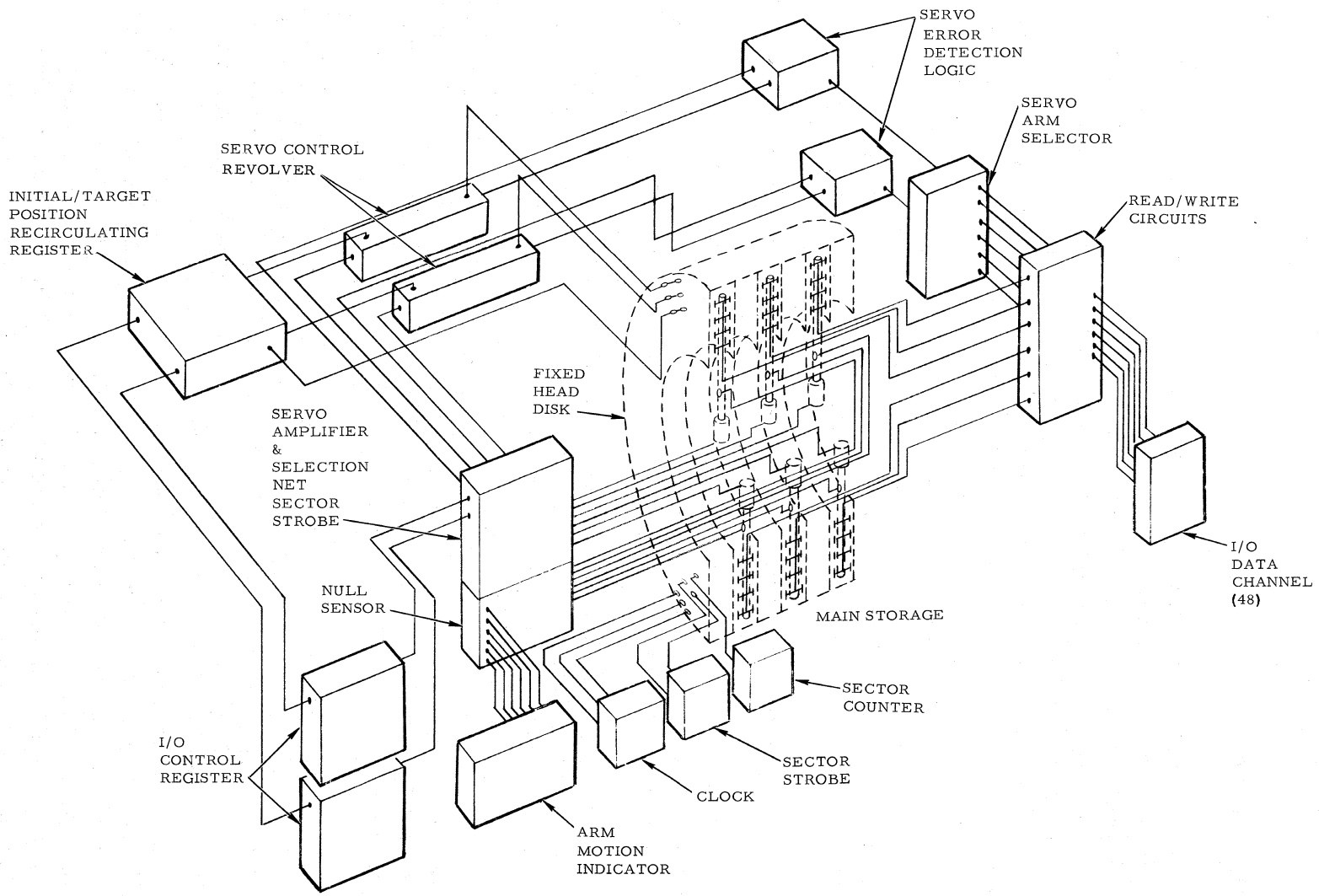


Figure 2. Functional Schematic of 6 Arm Storage Unit

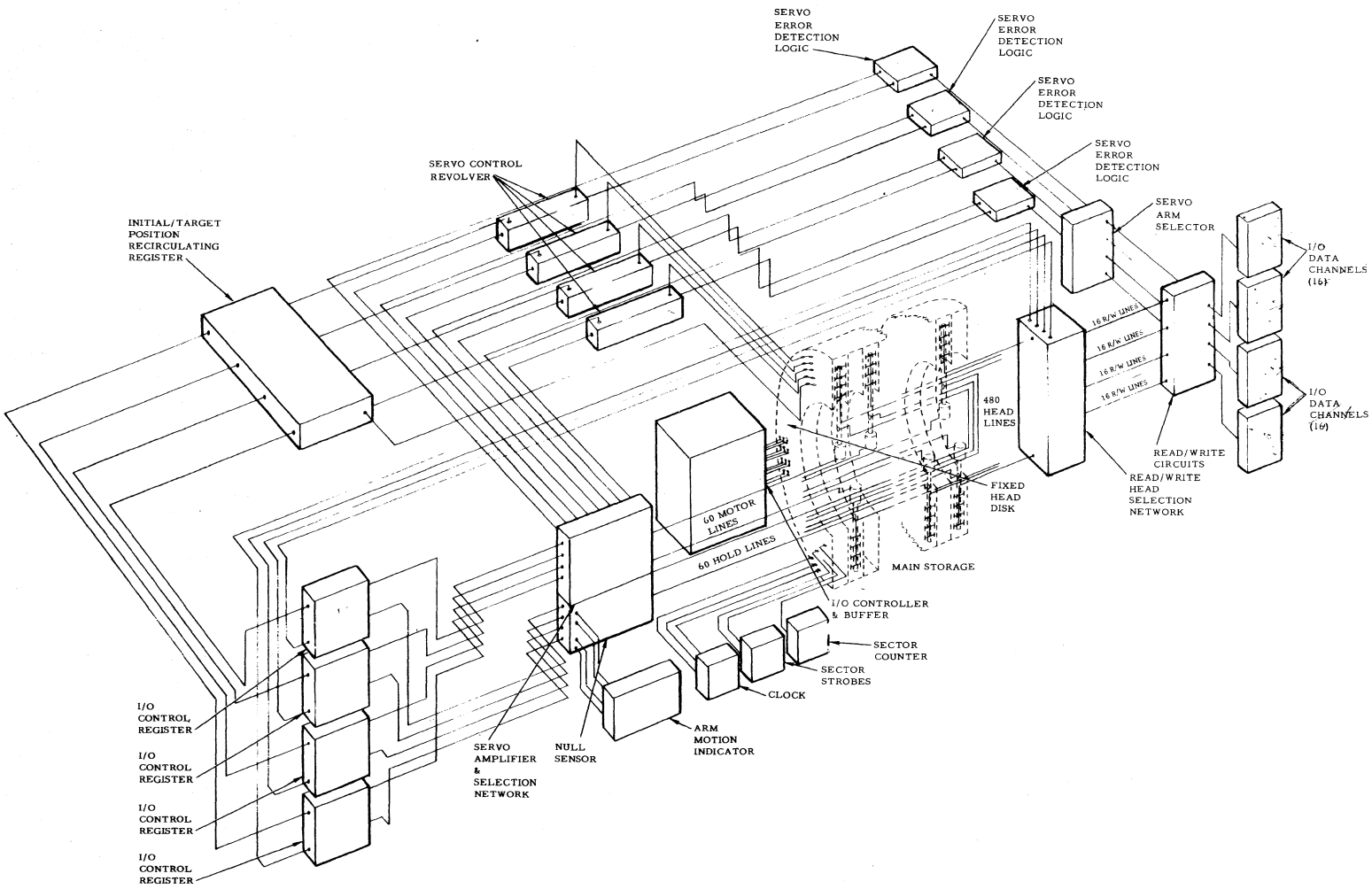


Figure 3. Functional Schematic of 60 Arm Storage Unit

The 30-arm unit is identical in all respects to the 60-arm unit except in length of disk pack and in having only half as many (two each) I/O control registers and corresponding groups of I/O data channels. In both the large units, core buffers are provided (equivalent to one each per I/O control register) to provide synchronous/asynchronous conversion between the MEM-BRAIN file and other equipment.

The 12-arm unit is similar to the 30-arm unit in number of data channels and control registers, but does not have the fixed head data manipulation capabilities or core buffers. In addition, there is a restriction on the data switching capabilities in that a control register can only define which half of a group of 16 I/O lines corresponds to which arm. The ordering of the interconnection from head to line within a block of eight is fixed in the hardware.

For emphasis it is reiterated that in the two larger units, any head in the main store or any head in the data manipulation section of the fixed head unit can be connected under control of the I/O register to any data line associated with that register. It is also emphasized that the two smallest units are designed only as storage for use under direct process control at synchronous rate by the central processor. By contrast the two larger units can work either under such direct control or under independent control of an internal stored program with only generic instructions from outside---either synchronous or asynchronous.

B. SOFTWARE

All four units may be operated in a variety of ways at the option of the user. While the basic operation of any one channel of such a unit is serial by nature, the organization of the complete unit permits some non-serial operation. Because of the multiplicity of heads, characters or words may be recorded and read in parallel from appropriately chosen groups of heads. A natural subdivision for all units is an 8-bit byte parallel mode which can be handled by a single arm. Multiples of this number may be used up to the capacity of the I/O channels provided in each unit. Thus the 6-arm unit can handle 48-bit words in parallel; the 12- and 30-arm units can handle 32-bit words in parallel; and the 60-arm unit can process 64-bit words in parallel. These are maximum capabilities for parallel operation. The two smaller units are designed to be optimal when used with an 8-bit byte parallel or direct serial mode of operation. Because of the internal processing capability, the two larger units may be optimized in other fashions by appropriate program control.

An instruction code is fed into an I/O control register in the form of a binary number which includes segments designating arm number, track number, head number, and (except in the 6-arm unit) an I/O line number. In the two largest units the instruction also contains a sector number and a mode code. Except for the latter item, the functions of these various portions of the instruction code are essentially self-explanatory. They define the necessary arm servo operation, if any, and the internal interconnections required to write or read the data in the proper portion of movable head storage. In the two largest units, when used with non-synchronous external equipment, the core buffers are normally connected in the I/O channels to provide translation services. If the external system is normally synchronized with the MEM-BRAIN unit, these buffers are available for use under control of the mode code in the instruction. This mode code, in general, is provided to control the operation of internal data manipulation or direct the execution of appropriate portions of the internally stored program. If it appears necessary for a particular machine application, the core buffer may be addressed under direction of the mode code (usually by the operation of the internal program) for use in connection with the data manipulation operations in the "fixed head" section. If such operation is called for in a system in which the external elements are not synchronous with MEM-BRAIN, such use of the core buffer will temporarily interrupt the corresponding communication channel between the MEM-BRAIN file and the external system, during the time required to process the portion of the instruction which requires this use of the core buffer. When used with internal stored program control, such interruption is not likely to be of serious consequence because the central processor does not require continuous detailed control of the MEM-BRAIN operations. This function of the core buffer is in addition to that described under "Hardware" above.

In response to an instruction code, an I/O control register addresses the particular head transport called for and designates the target position (track). An available transport servo is included in this operation and compares the target position with the present arm position from the fixed head record to determine control necessary for gross arm motion. When this motion has been completed, the servo switches to target-seek mode and completes the location of the arm to the new track. Simultaneously the necessary logical switching is carried out to connect the heads of this arm to the designated I/O data lines or other elements. A number of independent arm servos equal to the number of I/O control registers may be in operation at any given instant. Any servo may be under control of any I/O

register. The register provides an interface signal when it has accepted the target commands. When this signal is present, an arm may be addressed and a target position may be assigned to it. If less than all servos are operating at that instant, that I/O request will be acted upon by the file. If all servos are active, the I/O register will store the information until a servo is free, and will provide another interface signal showing that it is unavailable for new commands.

Reading or writing on heads associated with any arm while it is in fixed position may occur simultaneously with servoing of another arm to a new location. This capability has advantages in permitting continuous reading of records longer than provided in a single disk revolution by placing successive portions of the record on tracks accessed by different arms and moving the arms, which are not being used for reading or writing, to a position corresponding to a subsequent portion of the continuous record. The file magnetics and electronics uses an inter-record gap of four-bits (the slop-over on stop write is one-bit). Therefore, any change in the word length must be carefully planned to avoid waste of space when grouped into records for storage. A sector counter is included in each storage unit to allow the location of addresses along the track to be fixed with respect to origin. The exact number of sectors is fixed when the hardware is manufactured but is variable in principle (may be changed by a special service operation within the restrictions imposed by hardware, including sector counter capacity). Therefore, in the two smaller units, the simple rewriting of the sector tracks will change the minimum directly alterable record size. In the two larger units, short loops are utilized to manipulate data, and these must be modulo "sector count." Therefore, any change in sector organization after the file is constructed must be taken with the short loop structure in mind.

Because of the flexibility provided in the two larger units, it is possible to optimize the operation of the MEM-BRAIN file on the basis of a variety of criteria in accordance with the needs of the user. Such optimization may be based on the use of content or location address for data or an intermixture of the two. The file may be organized for optimal data access under a variety of contemplated major data manipulation requirements as, for example, to permit the equivalent of alphabetic insertion of new data at the appropriate point in an existing file, etc.

In all cases, it is possible to connect more than one control source to a MEM-BRAIN file unit. However, this capability is primarily an advantage in the two larger units because of the internal techniques available to minimize interference. Specifically, these

units can be connected to a multiplicity of computers and also to direct inquiry stations for appropriate system requirements. Likewise, the outputs of the larger MEM-BRAIN files may be transmitted through the central processing equipment(s) or may be sent direct to display or printer units or other peripheral devices.

Where one of the larger units is used with multiple processing systems, it can either be operated as a unit so that all data storage is available to all processors, or it may be operated with entirely different organization in different parts of machine so that to the external data systems, it looks like a multiplicity of completely independent auxiliary stores.

VI. RELIABILITY

A. STANDARD DOCUMENTS

The proposed storage units will be designed in accordance with the following Military documents: MIL E5400G; FED STD 222; MIL Q 9858A.

B. DESIGN FOR RELIABILITY

Design principles embodied in the MEM-BRAIN File have been selected with the ultimate reliability of the device as a paramount consideration. Simplicity is always of extreme value in eliminating failure modes and enhancing reliability of any system. Consequently, at every point where a choice between simple and complex solutions was available, the simpler technique was chosen.

For any unit intended for military application, it is desirable to assume the need for operation in a hostile environment. Consequently, ruggedness is a necessary feature in such a design. In the MEM-BRAIN development such ruggedness has been sought at every decision point, but not by the brute force method of increasing structural dimensions. Rather, the technique has been one of reducing mass wherever possible and increasing effective stiffness and structural damping to minimize response to shock and vibration.

Furthermore, the electromechanical elements of such a device are known to be sensitive to adverse environments related to humidity, pressure, and temperature. In the MEM-BRAIN file, therefore, the electromechanical package has been designed as a hermetically sealed unit, and care has been taken in the choice of materials and their structural interconnection to minimize disturbance of critical locations due to temperature change or temperature gradient.

The electronic elements of such a system, on the other hand, may be more subject to deterioration in performance by parameter drift or catastrophic failure. Therefore, the electronic package has been designed for ready access to permit maintenance by module replacement. Its enclosure will be dustproof and drip-proof but will not be hermetically sealed.

To minimize the failure potential in the electronic system, the background developed on the MINUTEMAN standard parts will be used wherever applicable but parts will not be subjected to the full "burn-in program" used in the MINUTEMAN itself.

C. PREVENTIVE MAINTENANCE

In addition to the care taken in selecting design features to improve the inherent reliability of the MEM-BRAIN file, it is contemplated that a preventive maintenance program will be developed to enhance the overall (as used) reliability of the file. Such a program will be based on a philosophy of replace and test which assumes that the serviceman has available a stock of spare modules and a check-list giving an optimum routine for such procedure. It is anticipated that the preventive maintenance program will call for carrying through this operation at scheduled intervals (about once per month). However, if an unscheduled failure were to occur, the replace and test routine would remain the same. It is expected that the entire end of which time the electronic elements of the file will have been brought up to essentially "factory-fresh" performance. It is not anticipated that the hermetically sealed electromechanical package will require maintenance except at extremely long intervals. Such maintenance should not be attempted except under clean-room conditions such as exist at the factory or at major military repair centers.

D. RELIABILITY PREDICTION

It was found that MINUTEMAN components without full MINUTEMAN tests were, in general, less expensive than commercial components. Assuming the use of such parts and the methods of predicting reliability which have been so completely successful for MINUTEMAN, the following MTBF and failure rates have been predicted:

Failure Rate* and MTBF

	6-arm Unit	12-arm Unit	30-arm Unit	60-arm Unit
Failure Rate	8.0449	14.7616	19.2972	22.7667
MTBF, hours	12,430	6,774	5,182	4,348

*%failures per 1000 hours operation.

This is the choice of component quality level used in pricing the present proposal (hereafter denoted as category A).

Electronic failure rate and MTBF are rather sensitive to certain parameters. If full MINUTEMAN specifications and tests were applied to all components (whether on the MINUTEMAN parts list or not), the price of the components would be higher and greater effort would be required to define appropriate specifications and tests. However, this choice (hereafter denoted as category B) would yield failure rates and MTBF's for the electronics of:

	6-arm Unit	12-arm Unit	30-arm Unit	60-arm Unit
Failure Rate	2.9959	4.8616	6.4410	6.9543
MTBF (approx.)	33,400	20,570	15,520	14,380

Wearout and aging failure modes are essentially eliminated in all electromechanical elements except the main rotor bearing. Proper design on this bearing essentially eliminates fatigue failure and leaves the lubricant the only remaining contributor to failure. MINUTEMAN experience shows very little difficulty with bearing lubricant. Therefore, the prediction for MINUTEMAN, which is 10,000 hours lubricant life, leads to planning lubricant removal and replacement once a year. The extremely simple design and the care that will be taken in manufacturing and assembly of this file indicates that over 15,000 hours MTBF is readily attainable in the electromechanical package. The overall unit should be expected to show failure rates no greater than:

	6-arm Unit	12-arm Unit	30-arm Unit	60-arm Unit
Failure Rate				
Category A	14.70	21.75	26.3	31.3
Category B	9.65	11.55	13.1	14.95
MTBF (approx.)				
Category A	6,800	4,600	3,800	3,200
Category B	10,300	8,600	7,600	6,700

The conservative realism of these predictions may be judged by the MINUTEMAN experience. The reliability goal allotted to the D17 MINUTEMAN memory under continuous silo operation was very high. To date the operating experience from the active military installations has shown an actual MTBF exceeding the goals by over 3X. Furthermore, there have been no failures traceable to the memory on any of the MINUTEMAN test and training flights to date.

VII. RESISTANCE TO MILITARY ENVIRONMENT

A. VIBRATION AND SHOCK

In the design of an electromechanical storage unit for operation in a high vibration or shock environment, it is essential to maintain a maximum stiffness to mass ratio in all parts to minimize deflections and, whenever possible, to raise the resonant frequencies above the range to be encountered. It is particularly important to maintain a fixed radial relationship between the true center of rotation of the disk or drum and the read/write heads. Variations in this relationship result in phase modulation or timing errors between information and clock track signals, the major mode of functional failure in the electromechanical portion of a storage system. High stiffness to mass ratio minimizes this problem. Minimum weight also reduces loading and stress on parts, thereby reducing physical failures.

The MEM-BRAIN disk configuration reduces weight to the practical minimum while maintaining a very high degree of stiffness due to the radial prestressing. The prestressed conical end bells also provide high stiffness with low mass. Axial spring rate of a single end bell is approximately .025 in./ton. Radial stiffness is much higher. The moving mass in the head support arms is kept to a minimum to minimize radial disturbances. Care is taken in the selection, method preloading, and mounting of the bearings to assure a constant true center of rotation for the disk stack.

Careful attention to similar design considerations, coupled with the most stringent criteria of acceptance in vibration and shock testing, has resulted in Autonetics' production disk memories which function properly under severe missile shock and vibration. These results are attained not only with a new optimum system but also with a theoretical degraded "worst case" system such as might occur at the end of design life.

In the selection of materials for MEM-BRAIN, compatibility of coefficients of thermal expansion has been emphasized. This minimizes stress and distortion in parts and change in spacial relationship of parts within a wide range of operating and storage temperatures. The major sources of heat are separated from the critical mechanical elements to minimize temperature differentials.

The compartment containing the major mechanical components is sealed to prevent the entry of moisture. This is primarily because condensation or high gas viscosity, due to high humidity, would be

detrimental to proper operation of the head pad gas bearings. The cover on the electronics compartment is dust- and drip-proof but provides ready access for maintenance. The electronic modules themselves are resistant to humidity short of condensation.

B. RADIATION AND EXTERNAL FIELDS

Design of the MEM-BRAIN File is based on applicable military specifications. It is, therefore, expected that normal requirements for electromagnetic radiation and RFI will be met. However, as engineering models, the units will not be subject to formal test and correction of deficiencies. Experience has shown that DC magnetic fields of low magnitude can cause detectable reduction in output signal levels. Prediction of an acceptable tolerance for such fields is impracticable at the present stage of development. However, it is expected that only close proximity to strong magnets, such as used with magetrons, is likely to cause a serious degradation.

VIII. MANAGEMENT

A. ORGANIZATION AND MANAGEMENT

Autonetics is one of seven divisions of North American Aviation. Our organization includes product divisions, a systems management division, a research division, and central management activities (Figure 4). Each product division is semi-autonomous and under the direction of a general manager who is also a vice president of Autonetics. The product divisions have their own manufacturing, engineering, sales, quality control, logistics, contracts and pricing, material, financial, plant engineering and administrative organizations. Accordingly, each vice president and general manager, while having corporation vested authority, is held individually responsible for the performance of his organization on a contract such as DCA Disk File.

1. Data Systems Division

The Data Systems Division of Autonetics will fabricate and test the DCA Disk File. We feel that our background qualifies us to engineer and produce the Disk File.

In 1952, as part of the NAVAHO missile guidance system, we developed the NATDAN computer for use with an inertial platform. Our second major guidance computer was the VERDAN (Versatile Differential Analyzer). More than 1700 VERDAN's have been produced for use with the A-5C (A-3J), AGM-28 (GAM-77) HOUND DOG Missile, and several classified airborne programs under ASD management. They are also used with Ship's Inertial Navigations Systems (SINS) on Polaris submarines and aircraft carriers. Production rate on the VERDAN reached a high of 50 per month.

Most recently, we developed the first production model micromin computer---the Autonetics D37 Minuteman II Computer. We also build the AGE for the Minuteman Missile system. This equipment is currently in production. D37 succeeds the Autonetics D17 (Minuteman I) computer which we also designed, developed and produced. More than 1200 of these computers have been delivered. No primary failure has been assessed against the D17 during more than 65 firings of the Minuteman. In the silo, D17 has exceeded 10,000 hours MTBF.

2. Autonetics Computer Memories

Over 3000 production computers built by Autonetics, since 1948, have included a disk memory. Autonetics' Data Systems Division is responsible for basic development of air bearings and open heads for use in disk memories. We initiated the first special rugged disk memory designs for militarized computers.

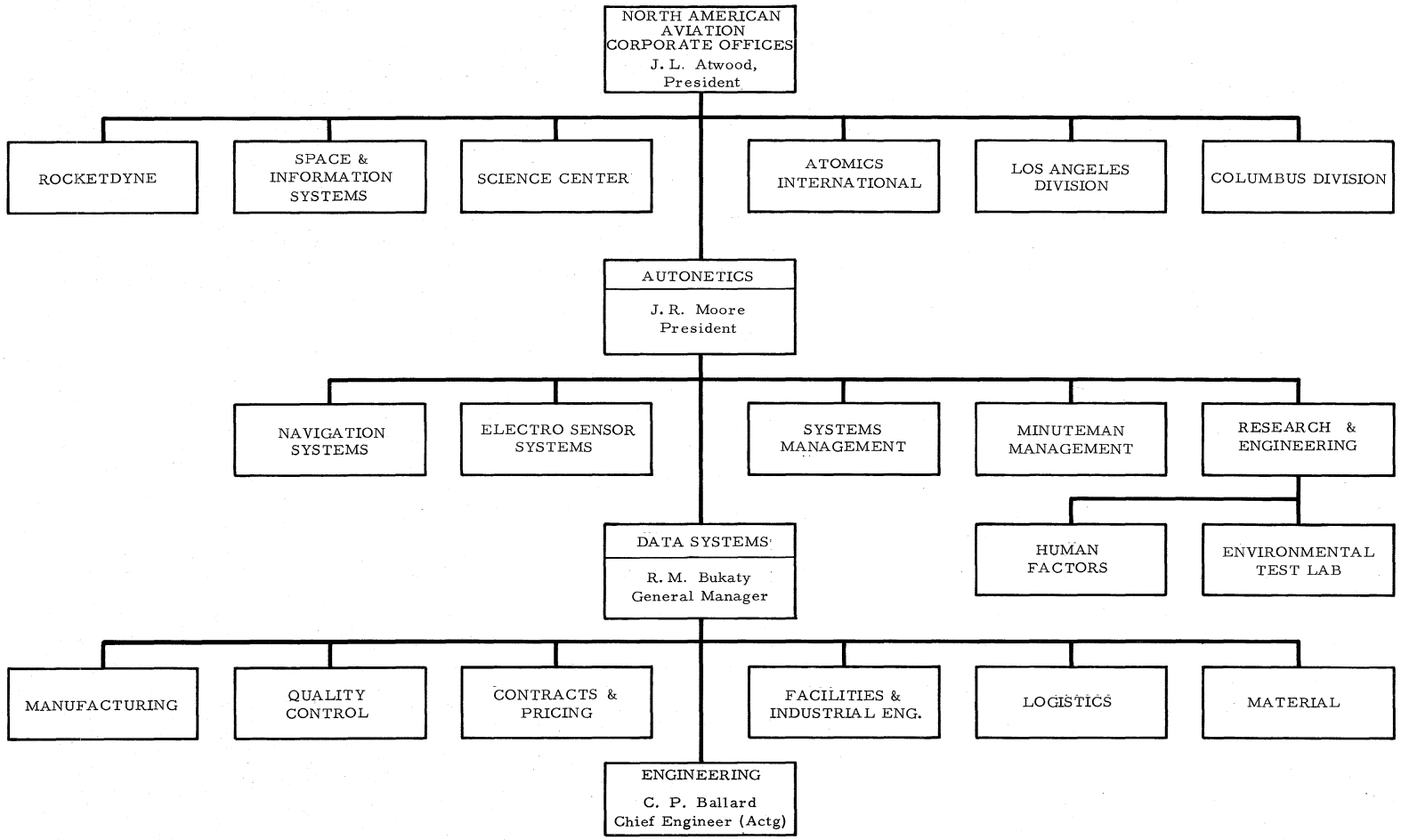


Figure 4. Corporate Structure

We designed and built:

1. The first disk memory used in a military computer.

2. The first disk memory used in a transistorized computer.

3. The first disk memory computer used for submarine navigation.

4. The first disk memory computer to guide a missile.

5. The first disk memory designed to meet Minuteman required MTBF. (In actual performance, these units have surpassed the reliability requirements by more than a factor of 3).

A more detailed history of Autonetics disk memories is provided in Appendix I.

B. CURRENT RELATED RESEARCH

The areas of research described below are being studied on company funds. Only those that have a relation to the DCA Disk File are presented.

1. Advanced System Requirements

Studies are directed toward the analysis of future military and industrial system requirements which affect the design of new computers. Current efforts include the formulation of a means for defining computer capability, development of a mathematical computer model, and formulation of a worth/cost technique for system evaluation.

2. Advanced Logical Design Techniques

Early investigation of new logic design concepts included preliminary design of a new computer, development of a high-speed, scaling integrator, and mechanization requirements for a static-memory digital analyzer. Current research is directed toward development of a theory on threshold logic, automation of the logic layout for interconnecting integrated circuit packages, and establishment of iterative scanning and computation techniques that permit recognition of characters.

3. Microminiaturization

Early investigation and development of microminiaturized concepts and techniques include micromin packaging and mounting techniques, integrated circuit joining techniques, and integrated circuit design. Results of these studies have been applied in the MINUTEMAN II Program. Current efforts are directed toward multiple integrated circuit modules and substrate deposition problems.

4. Thin-Film Device Development

Investigation of thin films applied to logic circuitry includes investigation of thin film hot-electron triodes, space charge triodes, and field effect triodes as well as thin film element fabrication techniques.

5. New Circuits and Components

Early efforts in the investigation of new components and circuit design concepts were directed toward evaluation of new components and circuit designs which offered weight, size, and power reductions. Current investigations include study of nuclear and space radiation effects, evaluation of high speed logic circuits, analysis of the charge control concept applied to high speed logic, and study of threshold logic devices.

6. Advanced Checkout and Maintenance Concepts

Early investigation of techniques for the measurement of dynamic system performance and location of equipment faults includes development of a mathematical technique for piece-part fault isolation and the formulation of a computer-controlled checkout system. Current objectives include studies on transfer function evaluation, development of in-flight testing techniques, and formulation of digital system checkout schemes.

C. FACILITIES

The following facilities are expected to be available to support the DCA Disk File Program.

1. MEM-BRAIN File Development Laboratory

The following equipments support the current development of the MEM-BRAIN file.

1. MEM-BRAIN Foil Preparation

   a. Coil Storage and Handling Equipment
   b. Foil Inspection Equipment
   c. Foil Cutting
   d. Foil-Hoop Thermal "Bonding"
   e. Hoop Trimming
   f. Packaging and Shipping Station

2. MEM-BRAIN Disc Preparation

   a. Receiving Inspection
   b. Foil Pretrimming Equipment
   c. Stretch form Die Foil Holder
   d. Stretch Form Die System
   e. Concentricity-Flatness-Tension Inspection Equipment
   f. I. D. Truing and Reference Diameter Forming Equipment

3. Servo Motor Dynamic Response Test

   a. Power Supplies (2)
   b. Oscillators (2)
   c. Oscilloscope
   d. Drive Motor Jigs & Fixtures
   e. Dynamic Position Measuring System
   f. Power Drive Controller

4. MEM-BRAIN Disc Magnetic Characteristics

   a. Hysterisigraph
   b. Head Tester
   c. 12" Plated Foil Tester
   d. Clock and Sector Writer
   e. Sig. Mod and Demod Exp det'n Setup
   f. Precision Head Assem Area

2. Disk Memory Assembly Shop

The disk memory assembly shop is a 7, 530 sq ft. environmentally-controlled area accomplished at a NAA capital expenditure of $170, 000. Equipment such as sterishields, microscopes, ultrasonic clearing devices, curing ovens, precision gauges, special work stations, etc., was provided at a NAA capital expenditure which

exceeded $200,000. The dust is controlled within the area to below 500 particles per cu ft. (over 5.0 microns in size). Over 3,000 disc memories have been fabricated in this facility at a peak rate of 82 per month. A portion of the pre-production engineering prototype disk memory facilities will be used in the fabrication of the DCA Disk File.

3. Precision Assembly and Engineering Machine Shop

The precision assembly area, which is adjacent to the disk memory assembly shop, diamond laps plus an optical flat measuring device with integral monochromatic light source. Several precision jeweller's lathes are available for the fabrication of air bearings to a tolerance of ±.0001". A rotary table on which is mounted a microscope will be used for lining up the memory heads both in angular and radial orientation.

The Engineering Machine Shop is fully equipped with mills, lathes, boring machines, etc., required to fabricate the detailed parts which comprise the disk file. This facility has been used in the engineering development of Autonetics computer disk memories.

4. Advanced Component Technology Laboratory

The Advanced Component Technology Laboratory (ACTLAB), constructed in 1963, provides the photographic and processing techniques for fabrication for multi-layer boards (MLB's) and for joining integrated circuits (IC's) to the MLB's. The area (22,000 sq ft) is both temperature and dist-controlled. The dust is held below 500 particles per cu ft in the 5 to 65 micron range with no more than 10 particles exceeding 65 microns in size. This degree of control is essential for building micromin equipment.

An $85,000 tutomatic X-Y plotter is available for the generation of accurate, aligned artwork used to produce MLB's. The plotter is capable of holding a location tolerance of ±.001" across a 60" x 48" table. This accuracy is required to assure alignment between the various layers of the MLB's.

Approximately 5,500 sq ft of the ACTLAB contains the precision photographic equipment (i.e. a $22,000 Robertson Overhead Camera, a $13,000 Step and Repeat Camera, an $8,000 Second Reduction Camera and an $8,000 Coordinatograph) necessary to produce the negatives which are used to etch the circuits on the copper-clad module boards.

a. Multilayer Board (MLB) Fabrication

The development of the MLB's which provide the intricate interconnecting network between the integrated circuits (IC's) has been accomplished in a 3,200 sq ft portion of the ACTLAB. It contains the ultrasonic cleaning equipment, etching, photo resist, laminating and plating facilities required to accomplish this effort.

The technology gained in this laboratory has been transferred to the 10,000 sq ft MLB production facility which, has the capability of providing 1,000 (8)-layer MLB's per month.

The 512 word core memories, if designed by Autonetics, will be fabricated in the Core Memory Production Facility. (Qualified vendors can also produce these memories.) The entire 2,000 sq ft area is enclosed with ceiling-high walls. The temperature is controlled to 70° ±5° F with the relative humidity controlled below 50 percent. The light intensity is held to a minimum of 125 ft-candles.

5. Environmental Test Facilities

The Environmental Test Laboratory, part of the Research, Engineering, and Reliability Division, is housed in a 72,000 sq ft single story building. This laboratory contains all of the facilities required to test the systems in the environments specified. These capabilities are:

Shock	Max 75 g's; 64-in drop Duration 6.5 to 32 ms Max load 400 lb
Explosion	Simulates sea level to 80,000 ft Combustible mixture of butane and air 4 ft dia x 5 ft long chamber
RFI	Shielded enclosures 32 x 16 x 10 ft; 56 x 12 x 8 ft; 15 x 8 x 8 ft
Temp Altitude	-100 to +400 F; to 250,000 ft
Vibration	Sine and Random Vibration systems 1500, 3000, 5000, 7500, and 30,000 force lb

Humidity	Temp 32 to 200 F Rel humidity 20 to 100 percent
Salt Spray	Temp 95 F; salt solution 3-20 percent ph 6.5 to 7.2
Sand and Dust	Temp 77 to 160 F; air velocity 200 to 2300 fpm; humidity less than 30 percent
Fungus	Temp 86 F; humidity 100 percent

D. KEY PERSONNEL

Resumes for key personnel on this program follow.

W. A. FARRAND, Assistant to the Chief Engineer, Data Systems Division, (Co-inventor of MEM-BRAIN File) Program Manager, MEM-BRAIN File Project

Mr. Farrand has been with Autonetics for 15 years. He is responsible for new computer and peripheral equipment business. Previously Mr. Farrand was Supervisor in charge of computers for the first inertial navigation systems (X-2, X-2A, 2-B, 2-C, X-4, X-5, and N-5A). As a Design Specialist, he developed the rotating magnetic disk memory. He was the initial Project Engineer on the MINUTEMAN and VERDAN computers. He has performed extensive research, been granted numerous patents and presented many technical papers on air bearings, analog-to-digital converters, displays, plotters, and printers. He wrote the chapter on input/output equipment for the McGraw-Hill Computer Handbook. He served in the Navy during World War II, working with electronics, radio, radar, and encrypting equipment.

Mr. Farrand received a BA degree in chemistry and an MS degree in electrical engineering from UCLA. He was an original member of the staff of the UCLA School of Engineering where he formulated and taught many undergraduate engineering courses. He is a member of the Association of Computing Machinery, AAAS and Instrument Society of America, Chairman of the Digital-Differential Analyzer Council, and a member of the Board of Directors for Simulation Councils, Inc.

T. M. HERTZ, Senior Technical Specialist, Preliminary Engineering Group, In charge of operating systems software and logic for the MEM-BRAIN File Project

During his 13 years at Autonetics Mr. Hertz has been engaged in operations relating to programming and logical design of digital computers. He had the sole responsibility for the logical design of the RECOMP I, II, and III as well as the JUKEBOX and REPAC computers. In addition, he has conducted investigations in the applicability of modular arithmetic and advanced logic techniques to Autonetics digital computers.

Mr. Hertz was a programmer for Remington-Rand, working with UNIVAC I. He taught physics at New York College of Engineering. As an instructor with the Air Force Technical Schools during World War II, he taught a variety of mathematics and electronics courses. He also worked as a technical writer.

Mr. Hertz received his BS degree from the College of the City of New York and his MS degree from New York University. He is a member of the Association for Computing Machinery and the Professional Group of Electronic Computers of the IEEE.

DR. R. B. HORSFALL, Senior Scientist, Command and Control Programs, Chief Scientist, MEM-BRAIN File Project

During his 18 years at Autonetics he has been primarily concerned with advanced research and development programs as a Research Specialist, a Staff Engineer, a Group Leader, and a Senior Scientist. For two years Dr. Horsfall served as a special coordinator for the MINUTEMAN program. In 1961 he served for one year at the Pentagon on a special project with the Weapon System Evaluation Group. His prior experience includes one year each with the Army Ground Forces Board at Fort Knox, Kentucky as an optical physicist and as an optical engineer at Eastman Kodak; ten years at Bausch and Lomb; and, prior to graduate work, one year as a member of the technical staff at Bell Telephone Laboratory.

Dr. Horsfall received a BS degree from Reed College, and MA and PhD degrees from the University of Illinois. He holds several patents in the fields of optics and automatic navigation, including a basic patent on stellar inertial navigation systems, and has written a

number of scientific and technical papers. Dr. Horsfall is a member of the Optical Society of America and Sigma Xi.

G. L. KREGLOW, Senior Research Engineer, Lead Programmer, MEM-BRAIN File Project

Mr. Kreglow has been with Autonetics for over four years. He is presently engaged in the design of a real-time FORTRAN IV compiler for the Autonetics D26C microminiature computer as well as software and programs for MEM-BRAIN File. He has done extensive work in machine learning, man-machine interfacing, computer time-sharing, file-management systems and, in particular, associative memories and distributed logic techniques. He has patents pending in these fields. During five years with Bendix Corporation, he worked on logic and equipment design for machine tool control and telemetering equipment.

Mr. Kreglow received his BS and MS degrees at Michigan State University. He is a member of the IEEE Professional Society, and Tau Beta Pi, Pi Mu Epsilon, and Eta Kappa Nu.

N. E. MARCUM, Supervisor, Mechanical Memories Unit, (Co-inventor of MEM-BRAIN File), In charge of the mechanical design on MEM-BRAIN File Project

Mr. Marcum is responsible for all Autonetics design and development work on rotating magnetic memories. He has been responsible for the design of these memories since 1954. During seven years with Remington Rand Univac, he developed memories and designed many portions of digital computers, peripheral equipment and other complex electro-mechanical devices. His earlier experience consisted of eight years of design of automatic and semi-automatic machinery for several companies.

Mr. Marcum received his BS degree in mechanical engineering from the University of Minnesota in 1939. He holds, and has pending, many basic patents fundamental in disk memory technology.

APPENDIX I. AUTONETICS COMPUTER MEMORY EXPERIENCE

A. INTRODUCTION

Autonetics computer development began in 1949 when it became evident that digital computation offered a greater accuracy potential than analog methods for the trend of the NAVAHO program. Since that time a series of computers has been developed of which the majority were for military applications involving extreme environmental and reliability requirements. Many models were primarily on-line, serial control computers. Some versions include extensive whole number (general purpose) capability for a wide variety of applications.

For these computers, Autonetics has developed a corresponding sequence of rotating magnetic memories, including those for the MINUTEMAN missile and the POLARIS submarines, which have demonstrated MTBF performance well in excess of the design goals. This sequence started with an experimental drum unit, but all later versions have been of disk form. The sequence represents a successful program to increase the ratio of information capacity to weight and bulk, and to reduce the power requirements, while improving resistance to adverse environments.

Many factors have contributed to the success of this program. Autonetics pioneered the application of hydrodynamic, gas lubricated bearings for control of the recording gap. Such bearings contribute greatly to the durability of the memory and to its insensitivity to shock and vibration under operating conditions. An extensive program of magnetic head development has provided high output signals from low writing power, and has permitted denser information packing, both radially and along the track. Materials study led to the use of beryllium for critical elements of the memories, including the recording disk itself, because of its unusually high stiffness to weight ratio and its outstanding dimensional stability. These are but examples of the meticulous attention to detail involved in the memory program.

This appendix summarizes the technical developments and the production programs at Autonetics which have supplied over one-half of all military computers in the free world today.

B. DESIGN CONSIDERATIONS

For memory systems of the type developed at Autonetics, the major factors that must be considered include access time, simplicity, reliability, volatility, power, size, weight, and operating environment. A study of the significance of these factors led Autonetics to develop the rotating magnetic disk memory for the serial real-time computation problems involved in its various military programs.

1. Access Time

Detail consideration of the modes of operation of serial memories and of random access memories shows that for real-time control computations, the serial memory may frequently provide lower access time than can a random access memory which used destructive readout and, as a result, requires a comparatively long reconstruct time. In particular, by proper programming and the use of short loops where necessary, the access time of a serial memory can be reduced to very nearly zero. Where the program does not require such rapid access, a longer time up to a major cycle of the memory can be allowed.

2. Simplicity

The serial memory also permits a material gain in simplicity. For example, a random access (core type) memory capable of storing 512 24-bit words requires 75 drive lines and 24 sensing amplifiers. A serial memory using a 128-word major cycle can store the same amount of information with only 4 drive lines and 4 sensing amplifiers. It is thus evident that where the problem permits use of serial memory, it provides a much simpler solution and, as a result, improves reliability and decreases cost.

3. Reliability

In addition to the simplification inherent in the use of serial memory techniques, other factors which contribute to reliability of the Autonetics rotating disk memory include simple and stable mechanical elements, whose response to environmental conditions can be readily tested and whose design can be adjusted to meet requirements. For example, the dynamic element of such a memory is a simple disk supported by radial ball bearings, whose design parameters are well known; and an axial gas bearing which is extremely stiff, whose normal

operating life is essentially infinite. The response of such an element to shock, vibration and other environmental conditions is much easier to determine than that of a complex collection of magnetic cores, wires, and electronic elements, which is theoretically static but is subject to indeterminate motion under the influence of shock and vibration.

4. Volatility

Many forms of serial memory and some types of random access memory are volatile in the sense that the loss of power or an accidental turn-off of the machine destroys the information stored in the memory. Memories which depend on the state of magnetization of a permanent magnet material are not subject to this type of volatility. This was an additional feature which contributed to the choice of a rotating magnetic disk for Autonetics memory applications. Such a memory is not completely free from destruction of information on turn-off, but intelligence which is not actively being operated on will normally remain undisturbed so that only reasonable care is necessary in shutting down such a machine to permit it to be restarted without reloading.

5. Power Requirements

It is axiomatic that for a given capability, the computer of the lower power requirement is the proper choice in any application. Relative to other types of memories that might be considered, the writing power required for the magnetic disk memory is quite small. Consequently, the Autonetics computers have been designed to make maximum use of the disk memory and to use other devices such as static shift registers only where essential for arithmetic operations. The power required for the drive motor can be very small compared to the difference in writing power.

6. Size and Weight

Size and weight are important design criteria in the development of military computers. In the memory section, this implies a high information density. It also emphasizes the desirability of providing short loops which are capable of supplanting much of the equipment otherwise required in arithmetic and logical operations.

7. Operating Environment

In contrast to fixed base computers, such as are used extensively in the business community, computers required for military applications

must be able to withstand environmental extremes. These include shock, vibration, wide temperature ranges and humidity extremes. For airborne application they also include wide changes in ambient pressure.

C. MAGNETIC MEMORY DEVELOPMENT

Most of the memory units herein described were used in complete computers---some in R&D models and some in production versions.

A small computer was breadboarded in 1949, using an Autonetics designed drum. The first complete Autonetics memory was the 15-channel drum unit shown in Figure AI-1. This memory, built in 1951, used standard ERA magnetic heads. It was used only briefly because it had inadequate capacity, no short loop capability, and because of mechanical tolerance problems. Experience with this unit led to the idea that disk recording promised an easier solution to these problems, and subsequent work followed this path.

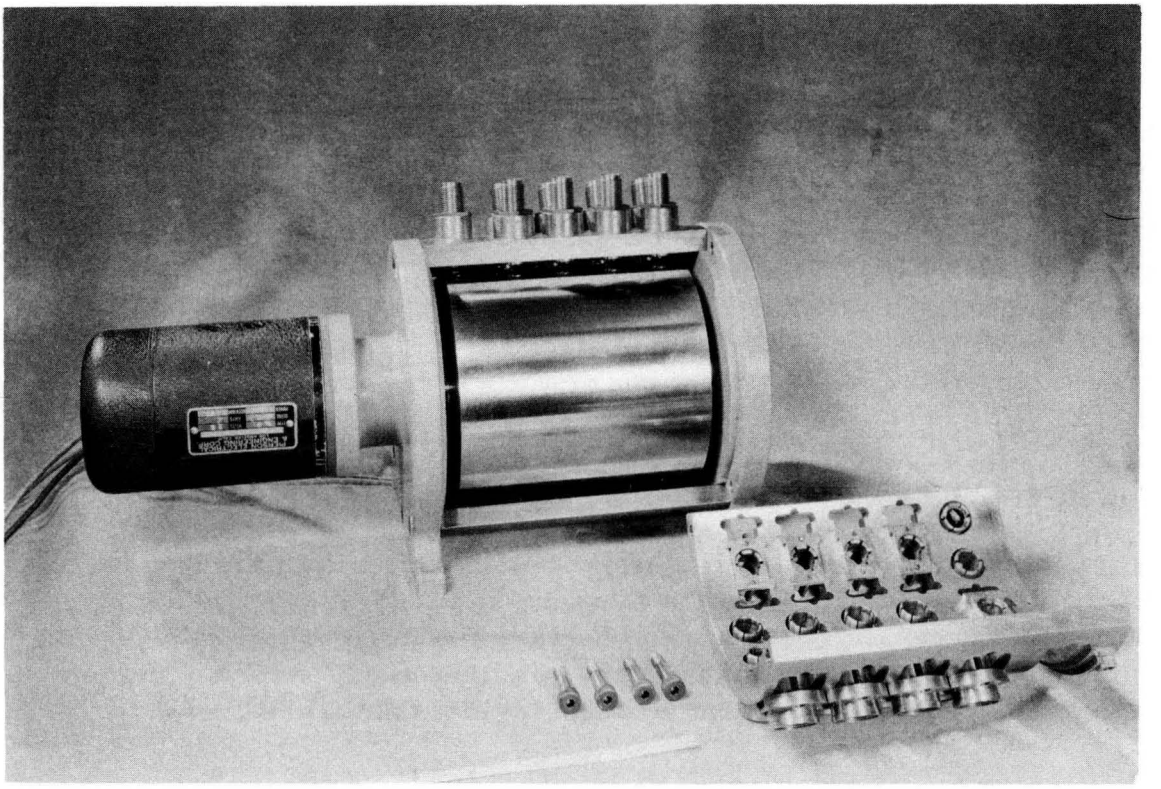


Figure AI-1. Experimental Magnetic Drum Memory

Figures AI-2 and AI-3 shown exploded and assembled views of the first magnetic disk unit. In this model, also completed in 1951, the disk was rigidly attached to the motor shaft and a ball thrust bearing was used to control the headplate to disk gap. Later versions of this unit used the first type of head employed by Autonetics for recording perpendicular to the disk surface. While these heads were still quite inefficient and the mechanical design caused great difficulty in disk alinement and spacing control, it confirmed many of the anticipated advantages of disk recording.

Toward the end of 1951 the first breadboard model utilizing an air bearing to control disk to headplate gap and a flexible diaphragm attachment of the disk to the motor shaft was constructed. This unit, illustrated in Figure AI-4, used the early versions of vertical recording heads. It also pointed up the necessity for finding and using materials which were dimensionally very stable, with respect to time and temperature, for the disk and headplate elements.

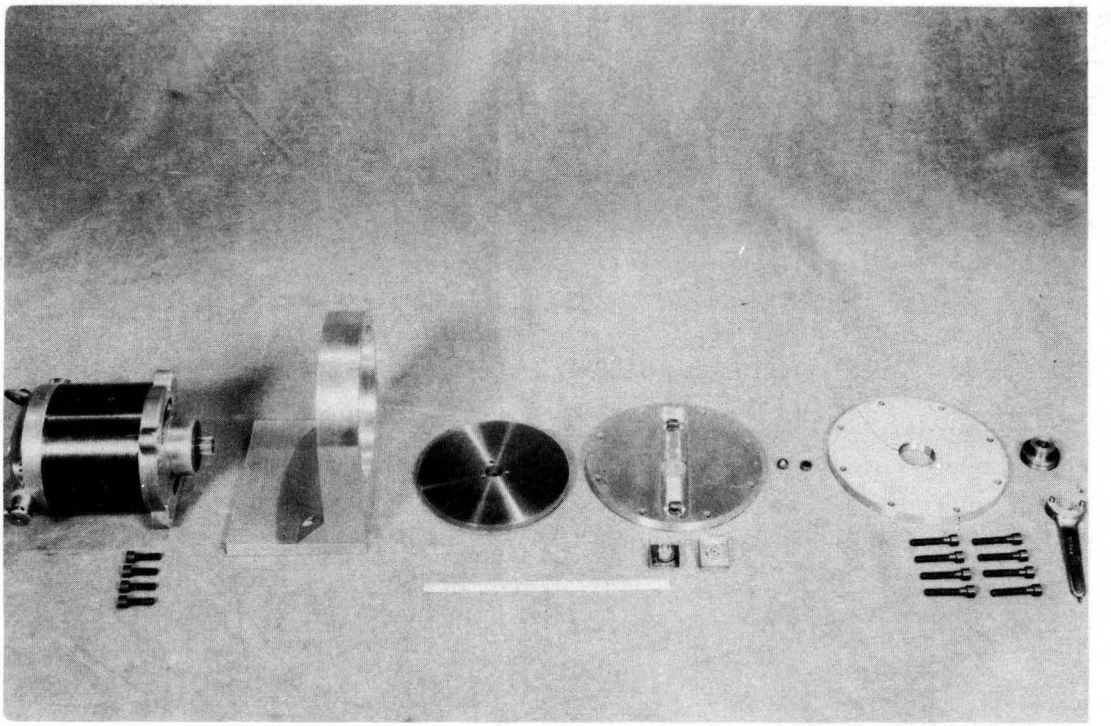


Figure AI-2. Experimental Magnetic Disk Memory, Exploded View

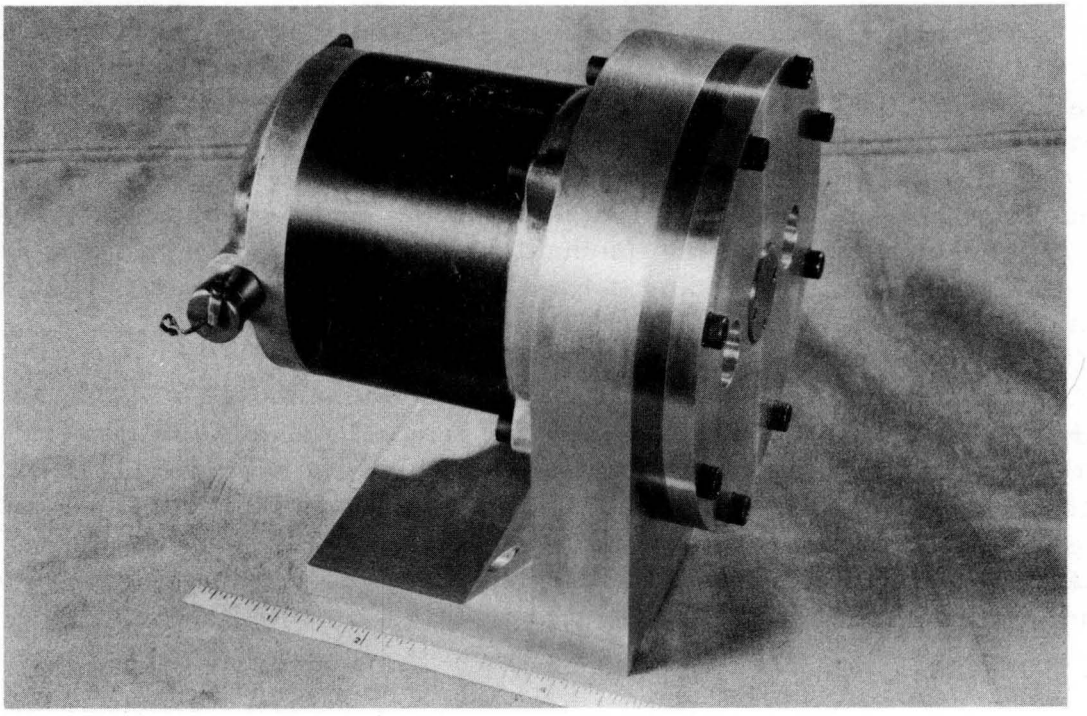
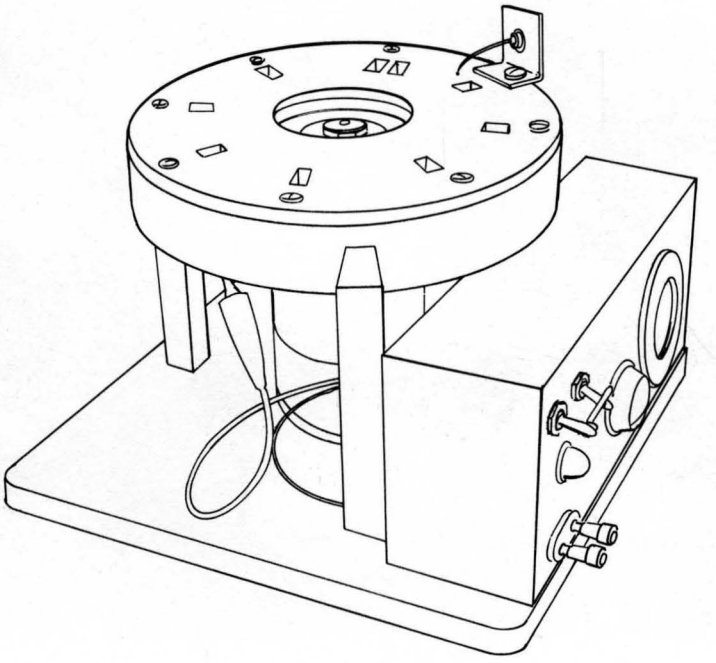


Figure AI-3. Experimental Magnetic Disk Memory, Assembled View



ES-87

Figure AI-4. Experimental Air-Bearing Disk Memory

By 1954 the first memory for a complete computer, which was actually used in test flights, was constructed. It had a storage capacity of some 13,500 bits of information and included provision for short loop operation for use with a digital differential analyzer type computer having 93 integrators in its format. The computer itself used vacuum tubes and, because this used liquid cooling, the memory was also equipped with a liquid cooling jacket. Beginning in 1954, a transistorized version of this computer was developed and a new and smaller air-cooled memory of the same capacity was included. A third stage in this development began in 1955 and resulted in a still smaller memory with capacity increased to over 16,000 bits. Figure AI-5 shows a comparison of these three memories, identified by the names given to the successive computers. An indication of the improvement accomplished is shown by the weights of the three memories which are, respectively, NADAN - 54 pounds, NATDAN A - 19 pounds, and NATDAN B - 5 pounds.

In 1952 a concurrent vacuum tube computer development (NATPAC) began for use with an experimental stellar-inertial navigation system. While the memory for this (Figure AI-6) was similar to the first one described above (NADAN), it used two headplates and provided nearly seven times the storage capacity of the NADAN memory.

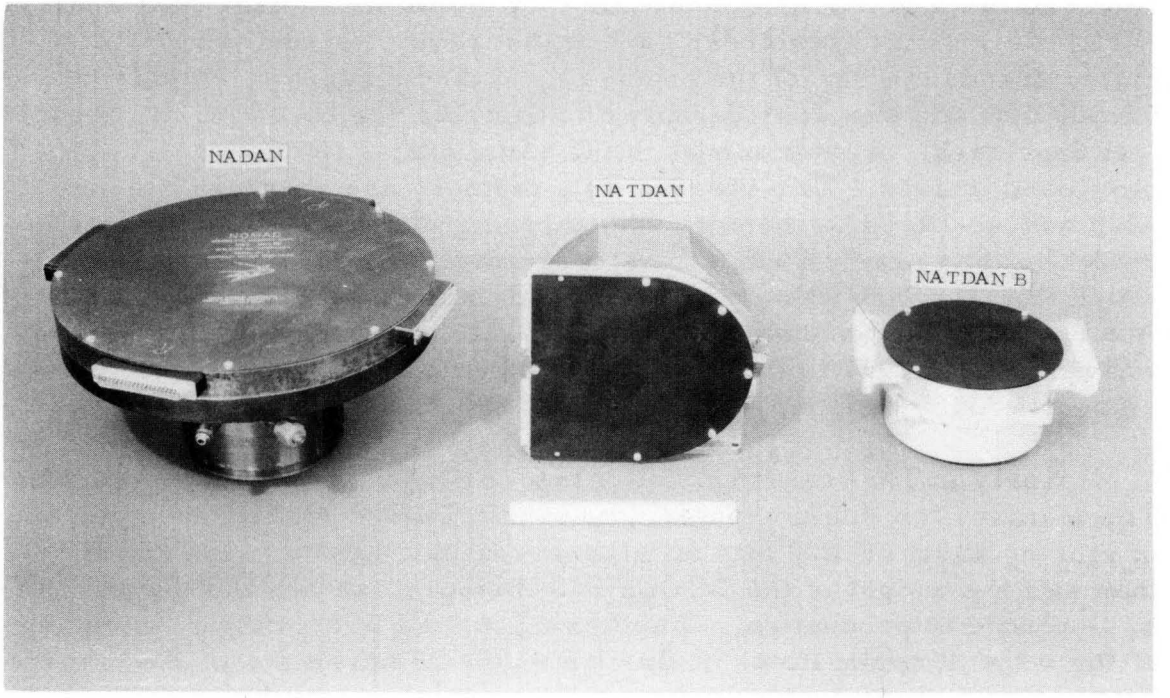


Figure AI-5. Comparison of NADAN, NATDAN A and NATDAN B

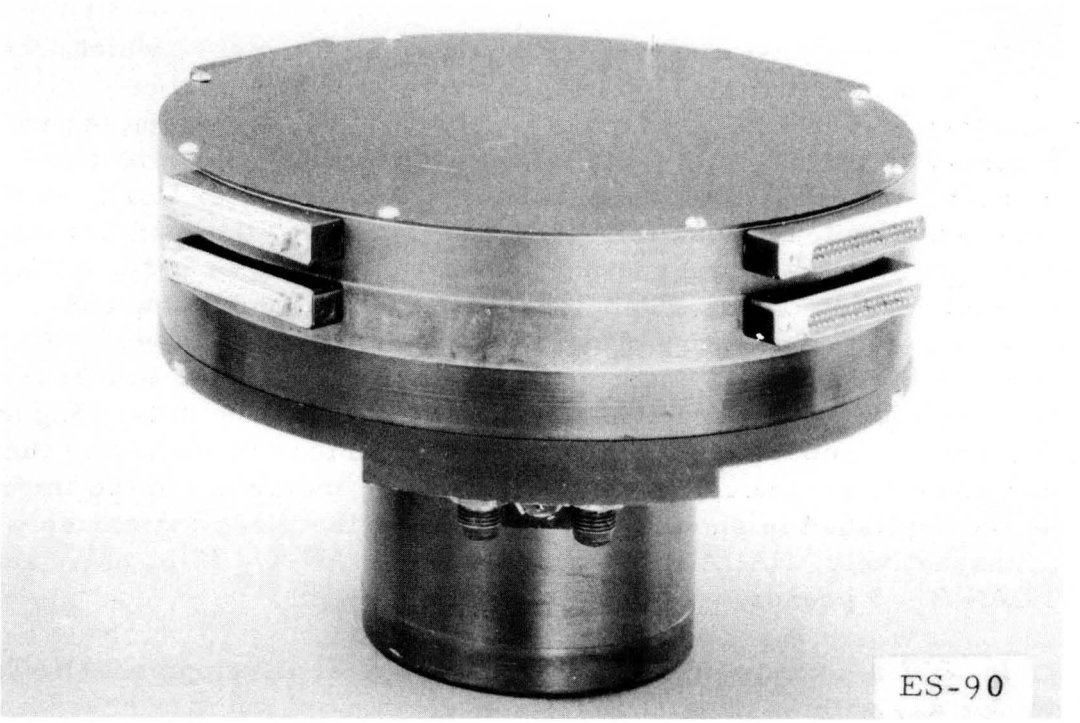


Figure AI-6. NATPAC Memory

Another computer program (RECOMP) began in mid 1955 which required the development of the memory shown in Figures AI-7 and AI-8. This memory included part of the transistorized memory circuitry around the rim of the headplate. It had a capacity of about 92,000 bits and was considerably smaller than the NATPAC memory just described. A later model in the same series (RECOMP II) was developed in 1958. Two views of this memory are shown in Figures AI-9 and AI-10. The memory was only slightly larger than the first model but had nearly double the storage capacity. The computer of which this memory was a part was put into commercial production by Autonetics. The technology of the RECOMP and NATDAN B memories was adapted in 1957 to the JUKEBOX computer which was supplied for a special Army problem.

Early in 1957 development of the VERDAN computer was initiated. The memory for this computer is shown in Figure AI-11. It is capable of storing about 65,000 bits of information in a smaller size and at less than half the weight of the RECOMP II memory. It was the second unit to be placed in production. Quantities involved in meeting requirements of the several applications of this computer required one of the larger programs in Autonetics experience. Later models of this computer used a modified memory similar to that developed on the MINUTEMAN program.

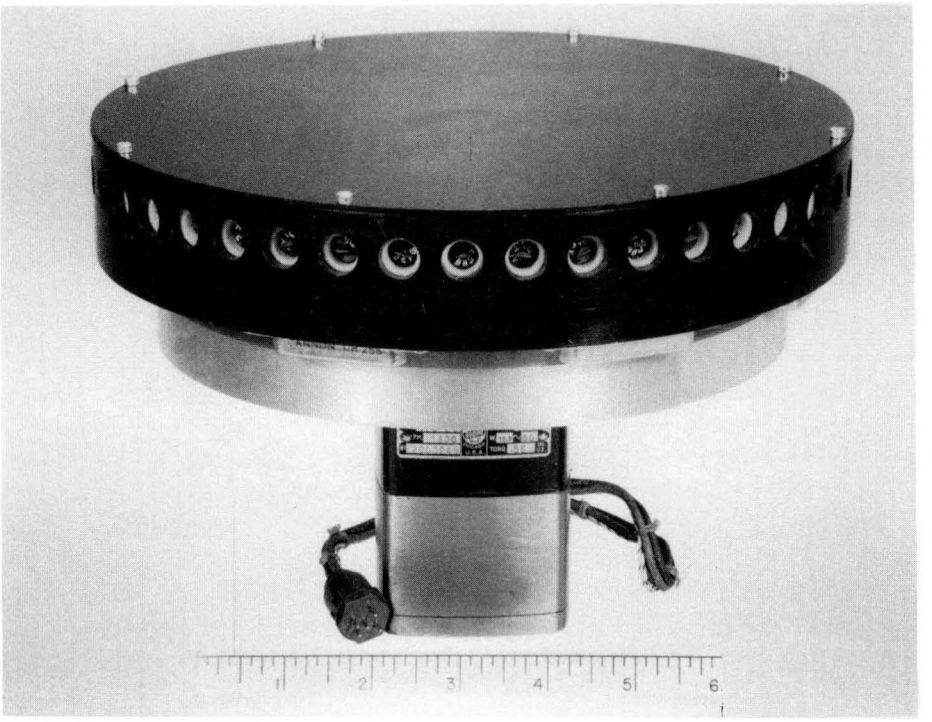


Figure AI-7. RECOMP I Memory, Assembled View

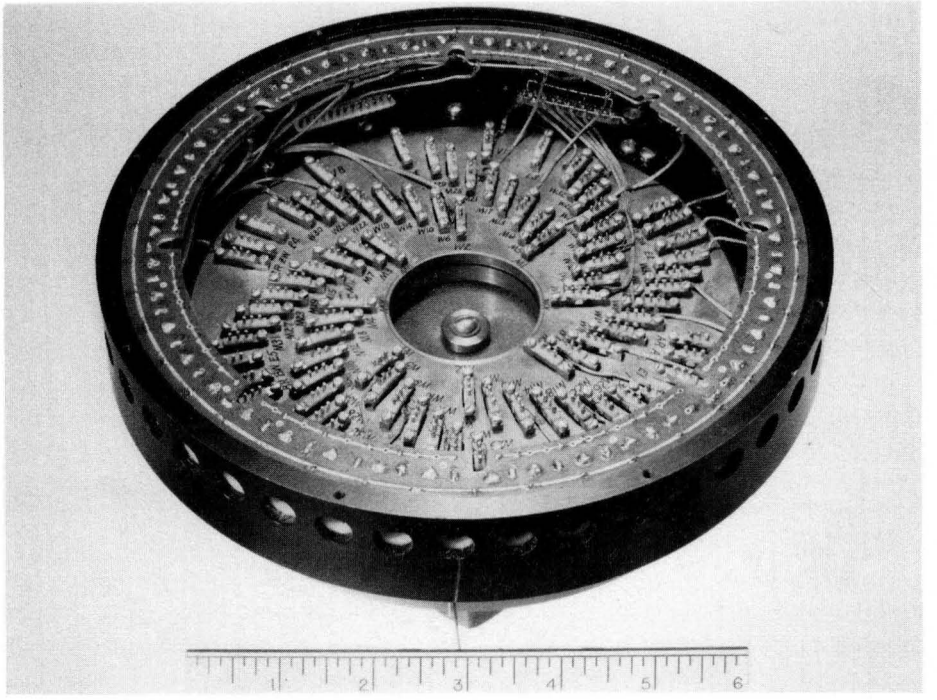


Figure AI-8. RECOMP I Memory, Cover Removed

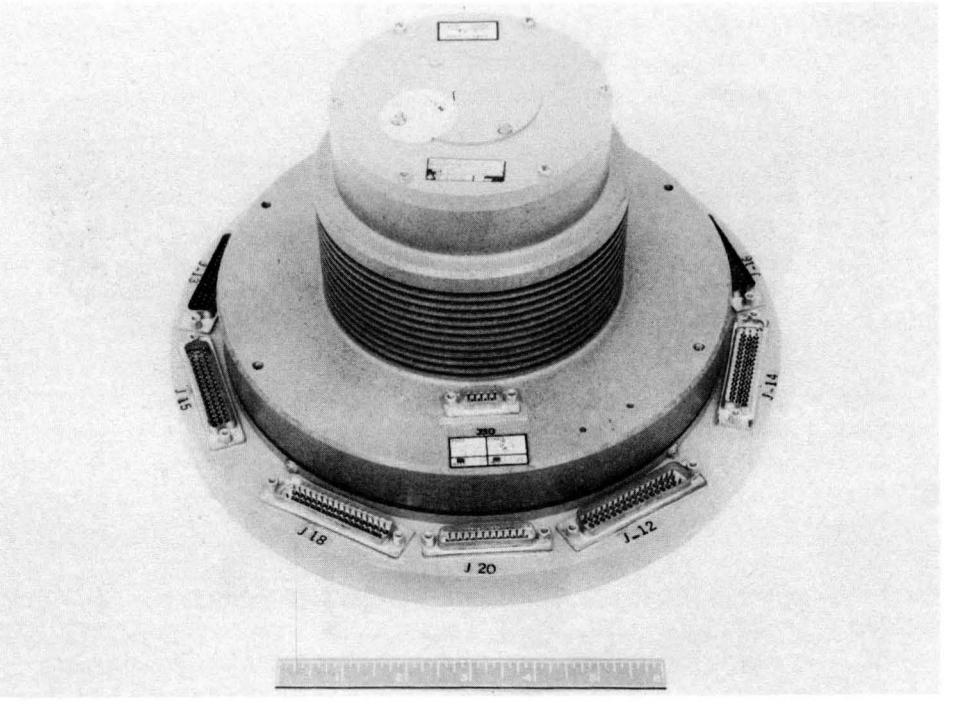


Figure AI-9. RECOMP II Memory, Assembled View

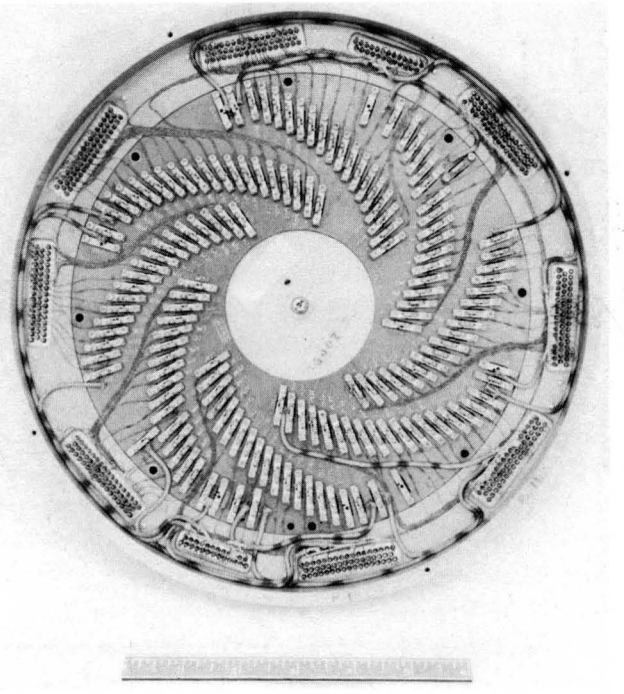


Figure AI-10. RECOMP II Memory, Cover Removed

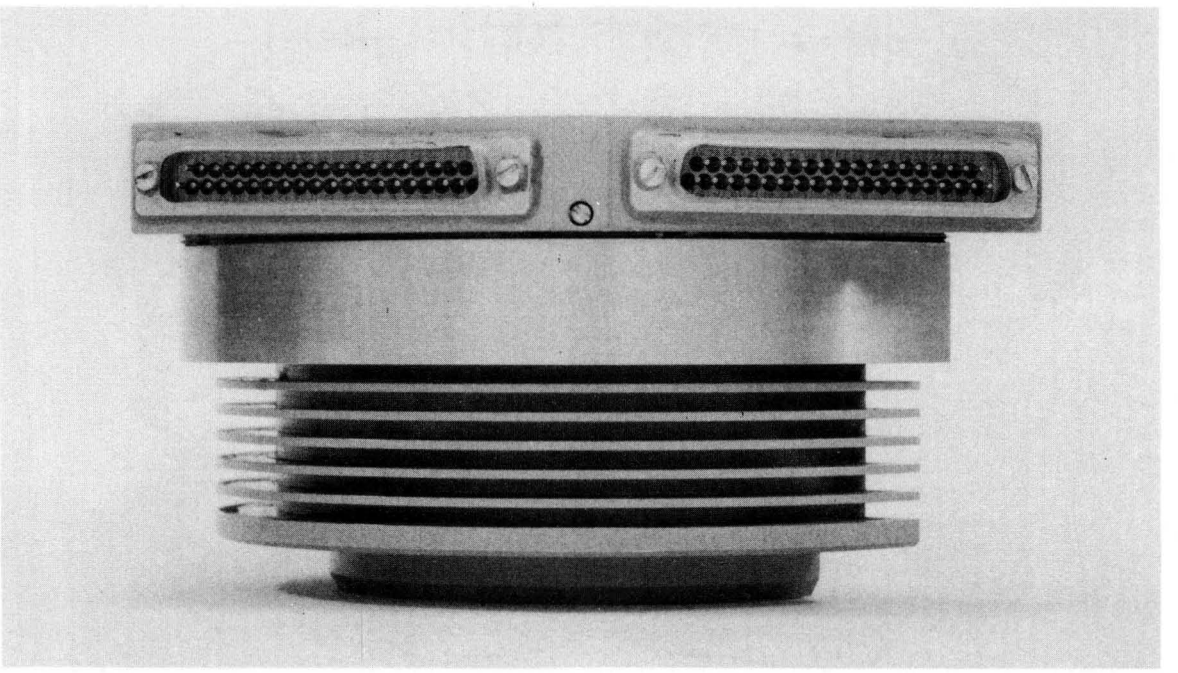


Figure AI-11. VERDAN Memory

The memory for the initial MINUTEMAN series was developed in 1960 and was the first free disk design in production. This change was dictated in part by the extremely high reliability requirements and the shock and vibration environment for which this memory was designed. It has a capacity of about 80,000 bits of information and is comparable with the VERDAN memory in size and weight. A cutaway of this memory is shown in Figure AI-12.

For a second version of MINUTEMAN a still smaller memory having approximately two-and-a-half times the storage capacity was needed to match the new integrated circuit electronic elements and meet the additional targeting requirements for the advanced version. Figure AI-13 shows this memory. Production of this computer began in 1963. A still later version of similar appearance with even more capacity was placed in production in 1964.

Also in 1960 a program was undertaken to develop the FADAC computer for field artillery use. The first model used a memory quite similar to the VERDAN memory in general appearance, but larger, to give it a storage capacity of nearly 150,000 bits. A later version of free disk design, and double the capacity, was also developed. Figure AI-14 shows these two memories.

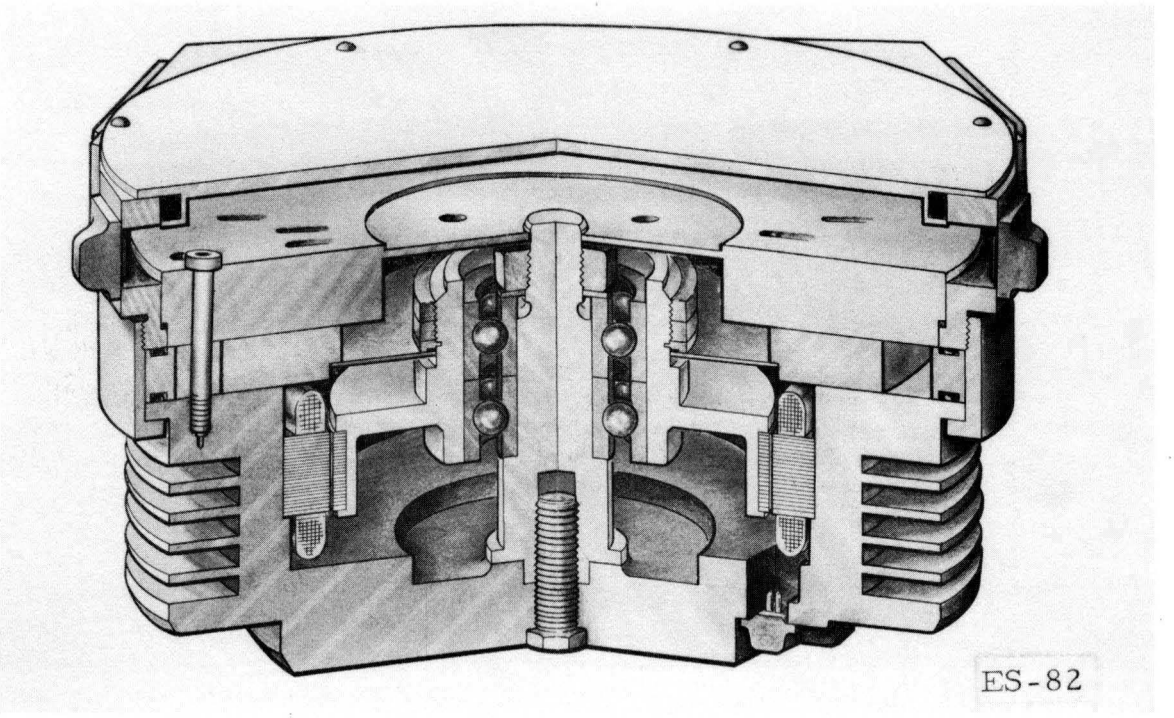


Figure AI-12. MINUTEMAN (D-17) Memory, Cutaway

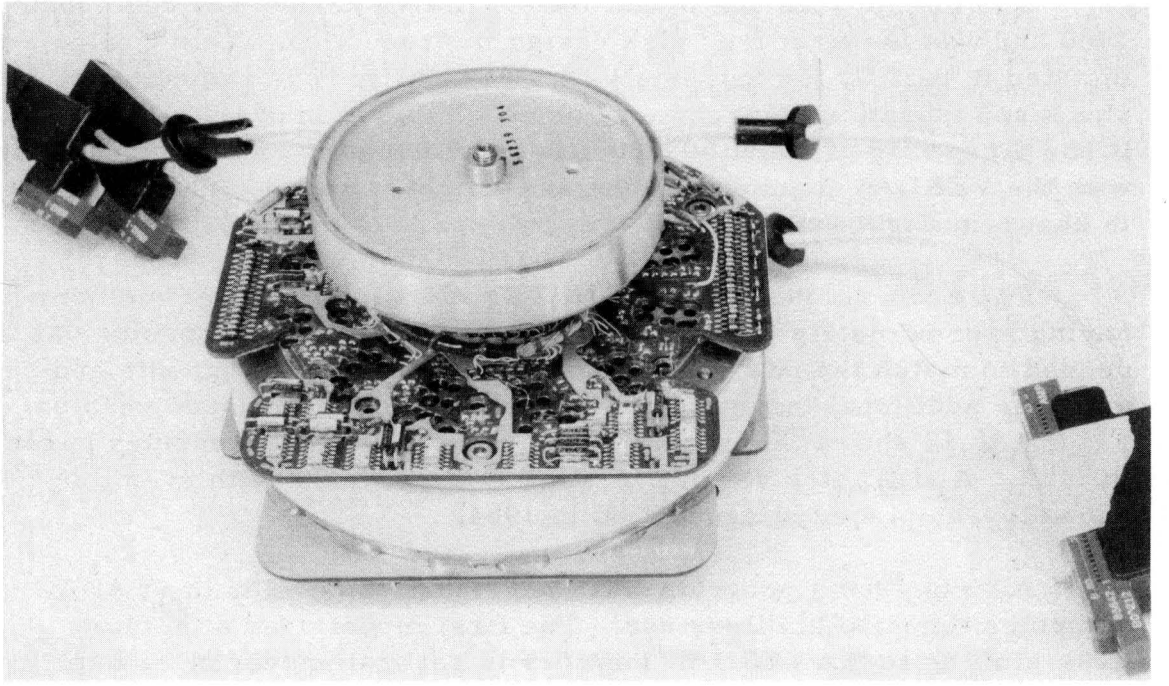


Figure AI-13. MINUTEMAN (D-37) Memory

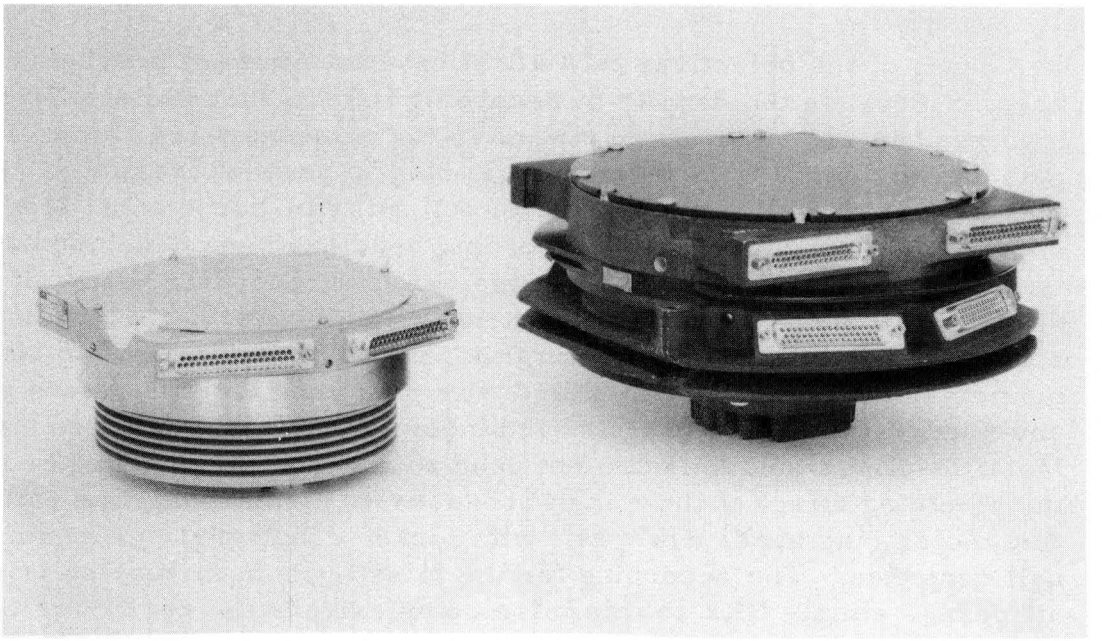


Figure AI-14. FADAC Memories

An advanced version of the VERDAN computer was developed specifically for submarine use and christened MARDAN. This computer involved a modified memory. Its capacity is about 180,000 bits. Production began in 1961.

Figure AI-15 gives a tabular summary of the characteristics of the Autonetics memories described above.

D. MEMORY TECHNOLOGY DEVELOPMENT

The success of the Autonetics military disk memory program is the result of an integrated approach to the solution of many detail problems in such devices. This includes such diverse factors as basic magnetic recording technology, bearing technology---both gas bearing and ball bearing, methods of locating the magnetic heads and adjusting them to precise electronic synchronism, details of design for thermal stability, logical design for optimization of the memory-computer team, and hermetic sealing* to avoid contamination.

*Note: As used herein, hermetic sealing implies complete enclosure by solid or elastomeric materials, rather than "vacuum tightness."

1. Magnetic Recording

One of the objectives in Autonetics' past memory programs has been to increase the density of recording information while providing high readout signal levels to minimize the necessary read amplifier gain and to do this with adequate shielding to prevent crosstalk. For the extreme shielding necessary for full missile-borne short loop operation, a special vertical recording head has been developed and is in production. In order to use the vertical recording heads, it is necessary to back the magnetic retentive medium with a magnetically soft material to provide a return flux path. Present missile main memories utilize beryllium plated with pure iron for this return path and a cubic iron oxide in a plastic binder for the retentive medium. Metallic-plated mediums are not used with vertical recording because the shielding effect of their high conductivity distorts the flux pattern. Autonetics ring heads work well with nickel-cobalt platings at similar cell densities. The recording for the missile main memories is, in all cases, simple NRZ to minimize complexity in the recirculation of very short loops. The recording heads and recording mediums work well with other coding techniques.

2. Bearing Developments

Since the beginning of use of gas bearings for controlling the recording gap, many refinements in gas bearing design and fabrication technology have occurred. The use of the flexible diaphragm constraint for axial control of the disk has simplified the control of gas bearing surfaces to one of shape rather than absolute dimension control, with one exception. That exception is the parallelism control on the free disk design and its concomitant requirement for control of separation of the two gas bearing stator elements relative to the thickness of the disk. Because gas bearing gaps are measured in microinches, it is necessary to control the surface shape to essentially optical precision and this, of course, demands extreme stability in the materials of construction, so that the initial quality of the gas bearing can be maintained under operationg environmental conditions over an extended lifetime. A series of material investigations has developed information on several materials having adequate stability. Most recently it has been found that beryllium provides the necessary stability together with added advantages in stiffness to mass ratio which is of particular value in disk construction.

	MEMORY	SIZE		WT. LBS	VOL FT^3	ELECTRICAL POWER		TYPE OF MOTOR	DISK				DISK STORAGE FORMAT				WORDS PER TRACK	TOTAL WORDS	BITS PER LINEAR IN.	BITS PER WORD	TOTAL BITS	BITS PER FT^3	MAX. ACCESS TIME (MS)	REPETITION RATE KC	HEADS			NO. OF HEAD PLATES	OPERATING ENVIRONMENT		
		DIA. IN.	HGT. IN.			MOTOR	SOLENOID		NO.	SPEED (RPM)	WT. (LBS)	DIA. (IN.)	TRACK WIDTH (IN.)	TRACKS PER RADICAL IN.	NO. OF TRACKS	NO. OF INFORMATION TRACKS									READ	WRITE	ERASE		TEMP ($^{\circ}$F)	ACC G's	VIBRATION G's
1	NADAN	9 1/2	6	54	.246			INDUCTION	1	1740		9	.050	10	7	5	93	465	160	29	13,500	$.055 \times 10^6$	34.6	78.2	11	8	0	1			
2	NATPAC	8 1/2						INDUCTION	2	3540		9	.050	10	37	35	64			41			17.6	151.				2			
3	NATDAN-A	6 1/2	3 1/2	19	.006			HYSTERESIS SYNCHRONOUS	1	1000		5 1/2	.050	10	7	5	93	465	250	29	13.500	$.2 \times 10^6$	60.	45	11	8	0	1			
4	RECOMP I	8 7/8	6 3/8		.207	115 V, 60~	70V DC 20 MA	INDUCTION SPLIT PHASE	1	1740		7	.025	20	37	35	64	2240	300	41	92,000	$.44 \times 10^6$	34.6	76.2	75	73	7	1	50 TO 150		
5	NATDAN-B	5	3	5	.035			HYSTERESIS SYNCHRONOUS	1	2000		4	.025	20	8	6	93	558	340	29	16,200	$.46 \times 10^6$	30	90	12	9	0	1			
6	RECOMP II	11	6 1/8	17	.123	115V, 60~	70V DC 20 MA	INDUCTION SPLIT PHASE	1	1740	1.3	8	.025	33.3	67	65	64	4160	220	41	170,000	1.38×10^6	34.6	76.2	75	73	7	1	32 TO 112	40 G SHOCK 11 MS	
7	JUKE BOX	11	3 3/8	13	.068	115V 400~ 3ϕ	70V DC 20 MA	HYSTERESIS SYCHRONOUS	1	2000	2.6	8	.025	25	67	65	64	4160	220	41	170,000	2.5×10^6	30	87.5	75	73	7	1	50 TO 120		
8	JUKE BOX	7 1/4	4		.057	115V 400~ 3ϕ	NONE	HYSTERESIS SYNCHRONOUS	1	2000		5	.025	28.6	68	66	64	4160	340	41	170,000	2.98×10^6	30	87.5	75	73	7	2			
9	VERDAN (SOLENOID)	6 3/4	3 1/4	6 1/2	.0398	115V 400~ 3ϕ	22V DC 100 MA	HYSTERESIS SYNCHRONOUS	1	6000	.25	5	.025	25	22	20	128	2560	310	26	66,560	$1,67 \times 10^6$	10.	330	28	26	10	1	0 TO 120	3	10
10	VERDAN (FREE DISK)	6 3/4	3 1/4	6 1/2	.0398	115V 400~ 3ϕ	NONE	HYSTERESIS SYNCHRONOUS	1	6000	.25	5	.025	25	30	28	128	2560	310	26	66,560	1.67×10^6	10.	330	28	26	10	1	0 TO 120		
11	MINUTEMAN (SOLENOID)	6 3/4	3 3/8	6 1/2	.0413	22V 400 ~ 3ϕ	22V DC 100 MA	HYSTERESIS SYNCHRONOUS	1	6000	.25	5	.015	40	25	23	128	2944	305	27	79,500	1.92×10^6	10.	345.6	35	33	10	1	65 TO 75	15	15
12	MINUTEMAN (FREE DISK)	6 3/4	3 3/8	6 1/2	.0413	22V 400 ~ 3ϕ	NONE	HYSTERESIS SYNCHRONOUS	1	6000	.25	5	.015	40	25	23	128	2944	305	27	79,500	1.92×10^6	10.	345.6	35	33	10	1	65 TO 75	15	15
13	FADAC	8 1/2	4 1/16	11 1/2	.0628	208V 400~ 3ϕ	22V DC 100 MA	INDUCTION	1	5800	.36	6 3/8	.015	40	35	33	128	4224	321	35	148,000	2.36×10^6	10.3	444	44	42	8	1	-25 TO 135		
14	FADAC	8 X 10	5	15 1/2	.10	208B 400~ 3ϕ	NONE	INDUCTION	1	5800	.73	6 3/8	.015	40	67	65	128	8320	321	35	291,000	2.91×10^6	10.3	444	76	74	8	2	-40 TO + 135		
15	D26A	5	3	2.3	.034	22V 400 ~ 3ϕ	NONE	HYSTERESIS SYNCHRONOUS	1	6000	.33	4	.015	50	38	36	128	4608	495	34	157,000	4.62×10^6	10.	435.2	65	53	17	2	-40 TO +65°C	14	10
16	MARDAN	6 3/8	4 1/8	7 1/2	.075	115V 400~ 3ϕ	NONE	HYSTERESIS SYNCHRONOUS	1	6000	.25	5	.015	40	54	52	128	6656	330	27	179,000	2.4×10^6	10.	345.6	77	67	18	2	50 TO 120	50	2
17	D37C	4 3/4	2 3/4	2.6	.027	22V 400 ~ 3ϕ	NONE	HYSTERESIS SYNCHRONOUS	1	6000	.1	4	.012	55	62	60	128	7680	408	27	207,000	7.66×10^6	10.	345.6	79	77	0	2	65 TO 75	15	15

Figure AI-15. Summary of Autonetics Memory Characteristics

To avoid damage to the recording surface by scraping during start and stop operations, early memory designs made use of a solenoid to apply an elastic preload to the flexible diaphragm after the memory came up to speed. Thus, the gas bearing was not brought into operation during slow speed running. The more recent free disk memory design confines the disk between parallel gas bearing surfaces and is constructed so that the diaphragm applies no appreciable load on either bearing. It has been found that this construction permits many thousands of start-stop cycles with negligible wear on the disk surfaces.

Deviations from perfection in radial location of the disk during operation could produce frequency modulation or timing jitter in the recorded signals. Therefore, as much attention has been given to the radial control bearings and their supports as to the gas bearings. Much cooperative work has been carried out with ball bearing manufacturers to develop bearing pairs which will provide dependably true running in preload configurations and will also provide satisfactory durability. This has involved not only the configuration of the bearing races and ball complements but also considerable investigation of optimum lubrication methods. In parallel, Autonetics has developed methods for mounting these bearings and controlling the working preload to a high order. It has been found necessary to use specialized techniques of cementing the races to the other memory elements to prevent mechanical distortion or uncontrolled relative motion.

3. Head Location and Tuning

In the earlier memories it was necessary to provide mechanical adjustment to permit accurate relative location of the heads along the tracks to control the length of short loops and assure satisfactory synchronism. Recently a technique for electronic tuning has been developed which permits the heads to be located to mechanical tolerances only and to provide the fine adjustment in the external circuitry.

4. Thermal Design

Because military computers are likely to require operation under relatively wide temperature extremes, a number of design factors have been included to assure stability of operating parameters under such temperature changes. Specifically, this has required careful consideration of compatibility in thermal expansion of the various elements of the memory unit to avoid disturbance of critical dimensions or preloads

under temperature changes and temperature gradients. Among the more critical of these problems has been the design of the ball bearing mounting to minimize changes in bearing preload and the control of the gas bearing gaps in the free disk design. The latter of these two has been solved by the use of spacers between the two bearing stators, made of the same material as the disk itself. Furthermore, designs of the various memories have been considered from the point of view of compatibility with the corresponding computer. The most obvious example of this is the use of liquid cooling in the early NATPAC and the use of suitable fin structures for gas cooling in later models.

5. Recording Patterns and Logical Design

Autonetics has standardized on the NRZ system of recording because it is compatible with high density recording and high readout signals and provides less chance of misinterpretation than other systems.

Provision of short loops by using more than one head on a given memory track can provide computer capabilities which would otherwise require special registers (flip-flops, magnetic cores, etc.) contributing to bulk and unreliability of the computer. The optimum selection of the short loop complement of the memory for a given class of computer has been extensively studied by Autonetics, and the success of this program can be judged by the combination of simplicity and capability of the existing systems.

6. Hermetic Sealing

Even for computers used in essentially sea-level applications, it has been found desirable to provide complete hermetic sealing, either of the memory itself or of the entire computer. Under adverse conditions of humidity, the natural breathing due to barometric changes may combine with diurnal temperature variations to produce adverse effects on an unsealed unit. Therefore, the later memory designs have all considered this factor, and, for those in which the memory required separate sealing, design development has led to considerable simplification in the methods of sealing (0-rings, etc.) to provide hermetic closure in combination with accessibility for fabrication.

While memories are tested and adjusted using air (ambient in a dust-free area) as the lubricant, the completed units are purged and filled with clean dry nitrogen before final sealing.

E. USE OF AUTONETICS MEMORIES IN COMPUTERS

By the middle of 1965, Autonetics had produced over 3000 computers. Each of these used one of the rotating disk memories herein described. To allow for spares, logistic supplies, special tests, etc., additional memories were required for each program. A few of the especially noteworthy accomplishments of Autonetics memories in these computers deserve some additional words.

The VERDAN computer program is an example of one whose applications were numerous and whose results were outstanding. This computer was used in such varied applications as the SINS system for the early POLARIS submarines, for the HOUND DOG air-launched missile, and for the North American VIGILANTE aircraft. The computer and, in particular, the computer memory exceeded the design goals set for these programs. The memories have turned in outstanding records of failure-free operation with MTBF's ranging upward from 3,000 hours, depending on the rigors of the environment to which they have been subjected. As an illustration of the ruggedness of the VERDAN memory and of the non-volatility of disk recording, Figures AI-16 through AI-18 show photographs of a VERDAN memory recovered after the crash of a malfunctioning HOUND DOG. In this case, it was possible to use the basic memory elements to read the information in normal fashion to assist in determining the cause of malfunction. In addition, the memory disk itself was treated with carbonyl iron which made the magnetic pattern visible and permitted optical reading of the stored information, as can be seen in Figures AI-16 and AI-18.

The MARDAN computer being used in the later POLARIS submarines is an advanced version of the basic VERDAN computer.

The original MINUTEMAN computer (D17) was aimed at extremely high design goals for reliability. A major reliability improvement program involving extensive work with component suppliers as well as in-house activity, was undertaken and has served as a guide for all electronic reliability efforts in the country since that time. As a result, this computer materially exceeded its reliability design goals, and the results of several years' service use in this missile continue to establish new records for MTBF on such equipment. A recent summary of operating experience shows a demonstrated MTBF of over three times the predicted good.

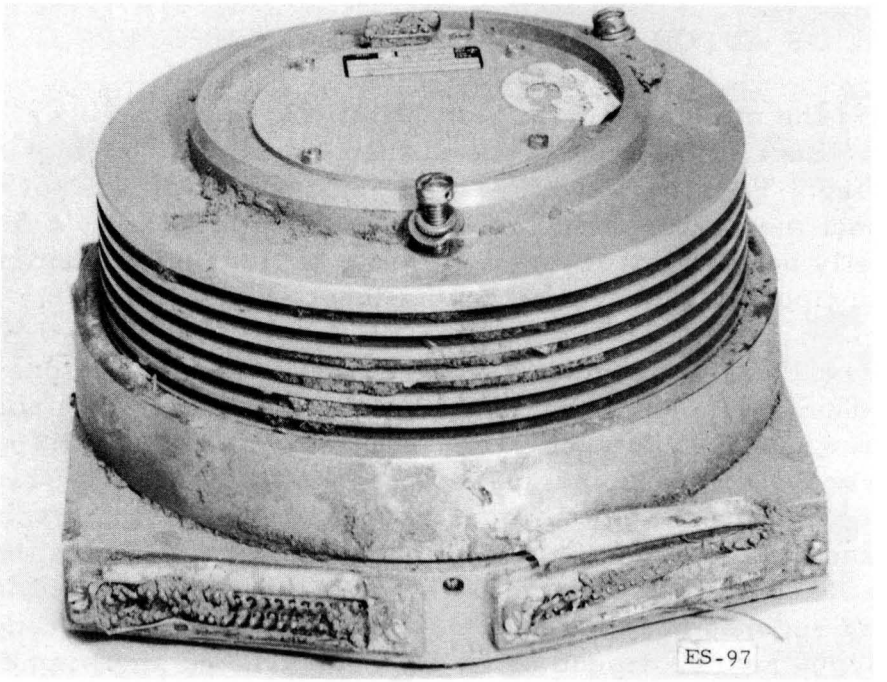


Figure AI-16. VERDAN Memory Recovered from Missile Wreck

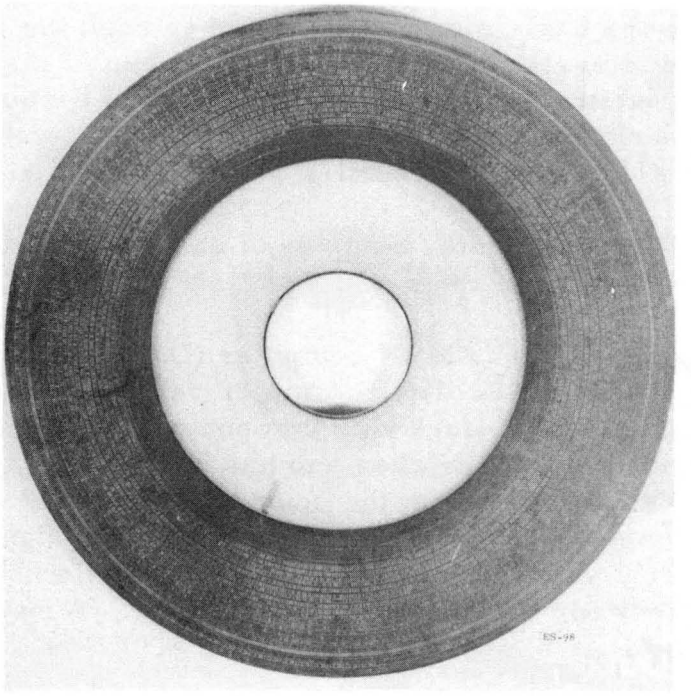


Figure AI-17. VERDAN Recording Disk With Data Made Visible With Carbonyl Iron

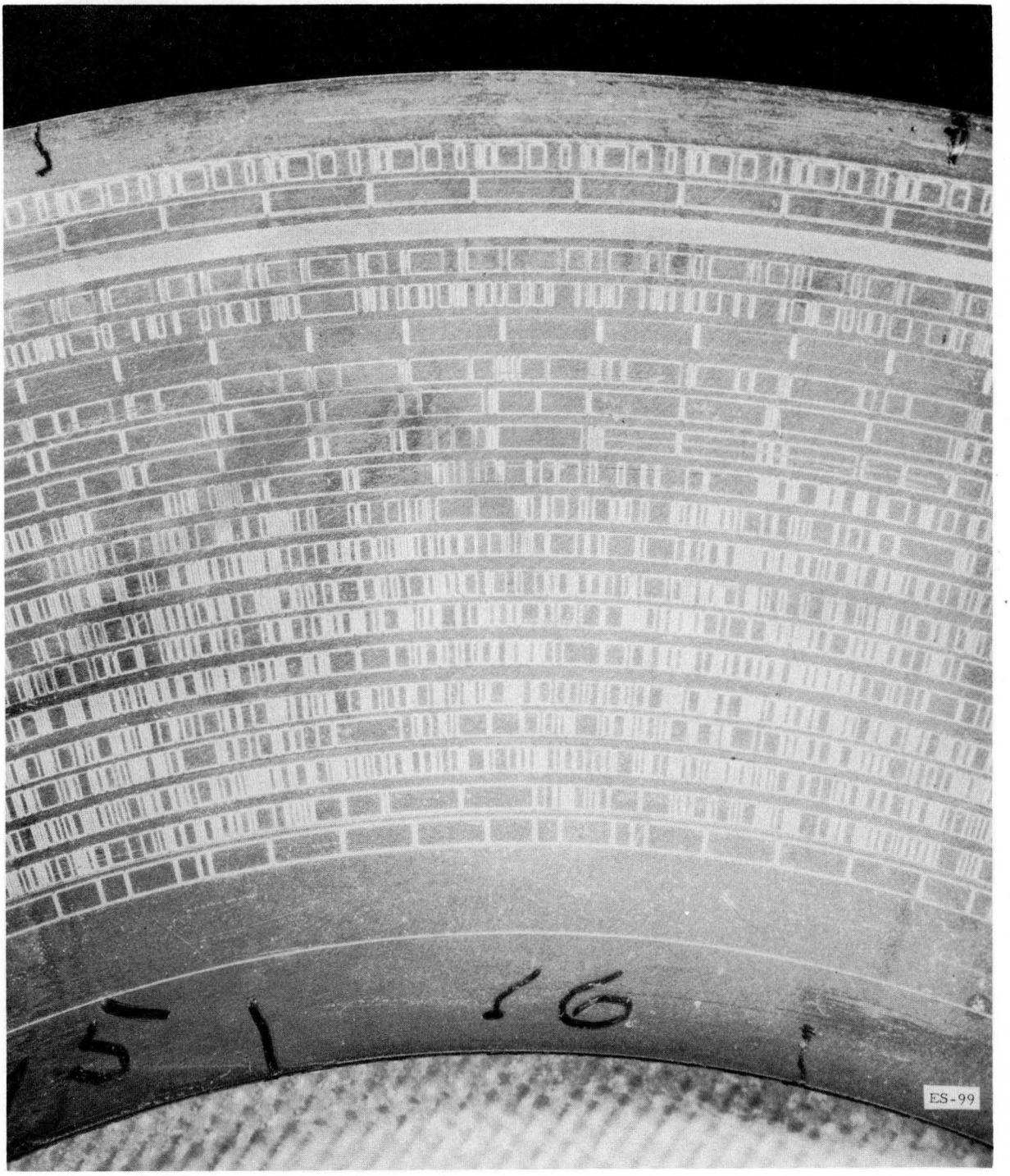


Figure AI-18. Enlarged View of Carbonyl Iron Pattern on VERDAN Disk

The more recent MINUTEMAN computer (D37) has provided increased computation capability in a considerably smaller package by extensive use of integrated circuits together with a memory modified on the basis of improvements in the state of the art. It is anticipated that this unit will eventually turn in even better results than its predecessor when service experience is accumulated.

APPENDIX II. PRESENT STATUS OF IN-HOUSE PROGRAM

A. INTRODUCTION

The immediate objective of the MEM-BRAIN File development is the fabrication of a 33 million bit design proofing model, Figure AII-1. This unit will incorporate for integrated test the principal unique features of the 2 gigabit MEM-BRAIN File, both in hardware and in electronics. Prior to undertaking this objective, concept proofing studies were made of the design philosophy. These concept proofing studies included analytical investigations, computer simulation runs and, in some areas, fabrication of models for testing particular concepts. These studies provided the basic design information needed for the design proofing model now in fabrication and the proposed 2 gigabit MEM-BRAIN File.

Two major results from these concept proofing studies were the demonstration of the properties of a taut membrane---the disk form used in the file---and the verification by computer simulation runs of the feasibility of the head positioning servo technique. From these and other results of these concept proofing studies, the present program for developing a design proofing model was defined. The present status of this program is described in terms of the major development areas. These areas are:

1. Disk stack structure and support
2. Taut membrane disk
3. Magnetic recording
4. Head positioner servo
5. Gas bearings
6. Logic and interface

B. DISK STACK STRUCTURE AND SUPPORT

The rotating support structure (end bell) for the design proofing model has been fabricated and subjected to design proofing tests. This

structure comprises a pair of pretensioned shallow cones base to base, fabricated from formed thin plates, which form a light, high stiffness support from a central bearing housing to the disk mounting surface. Viscoelastic surface coatings have been found desirable to further reduce the mechanical Q of the end bell. The disassembled unit is shown in Figure AII-2. This end bell is identical in design principle to the structure planned for the final 2 gigabit MEM-BRAIN File. It is presently being used in a testing machine for various experiments on the taut membrane disks.

Two end bells have been fabricated, one using aluminum as the structural material and the other using stainless steel. Tests conducted on these units led to the selection of the stainless steel end bell as offering superior stiffness and stability properties which offset the weight difference. As an example of the high stiffness, the aluminum end bell, subjected to an axial load applied at its periphery, exhibits a deflection of 40 microinch per pound of applied force. The stainless steel end bell of similar design exhibits an axial deflection of only 12 microinch under the same test conditions.

The drive member comprising the end bell, its bearing and the rim for support of the taut disks, is mounted on the top of a steel cabinet, Figure AII-3. The cabinet forms a simple base for the mounting of the unit and will house the electronics. The motor for driving the disk assembly is mounted in the underside of the top of the cabinet. The disk rotational speed of the design proofing model is 1200 RPM as proposed for the 2 gigabit MEM-BRAIN File.

C. TAUT MEMBRANE DISK

The development of the MEM-BRAIN File recording disk has required building a prototype production facility. Numerous test disks of unplated brass foil have been produced and several final model plated disks have been fabricated. This has included techniques and equipment for batch handling of the foil from coil strip to the completion of the taut plated disk.

This handling technique is as follows: The foil sheet cut from the coil stock is thermally bonded to a hoop made of channel section material. The foil remains attached to this hoop through all handling and plating processes prior to final press stretching of the disks. This hoop forms both a shipping support and handling frame to ensure that the foil remains free of any surface deformations. A mounted foil-to-hoop assembly, supported in the internal portion of the shipping container is shown in Figure AII-4.

The plated foil is cut from the handling hoop in the form of an annular disk. This annular disk is press formed into a finished taut disk in a single operation. A precision press has been designed and fabricated to perform this operation for engineering model quantities, and is shown in Figure AII-5. It is to be emphasized that a finished disk on its mounting hoop results from a single press forming operation. The surface uniformity of the basic foil stock, coupled with the pre-tension established by stretching the foil, yields a recording surface of extremely high uniformity and freedom from localized asperities.

The stretch-formed membrane disk has been subjected to extensive tests to ensure that highly uniform and reproducible properties can be established. These tests have proven the membrane disk concept and fabrication techniques to a level of production confidence.

D. MAGNETIC RECORDING

Studies initiated during the concept proofing phase are continuing to determine magnetic recording factors appropriate for MEM-BRAIN, such as properties and means for production of the magnetic plating of the disks, design of the read/write heads, the record format and techniques for its production.

The principal hardware effort has been testing the relative merits of various formulations and plating techniques for the nickel-cobalt recording surface. These tests were carried out on 12-inch diameter foil blanks in the apparatus shown in Figure AII-6. This preliminary phase has been completed, and several full-size MEM-BRAIN plated disks are undergoing quality and reproducibility tests.

Optimization tests for selection of a combination magnetic read/write head are underway. Several head designs are being tested for write current versus readout voltage. Factors under investigation are the head material (grade of ferrite), the recording gap, and the turns ratio. These tests use the 12 in. apparatus of Figure AII-6 with a disk plating of the type selected for use. A recording track of 10 mils width is planned for initial use in the design proofing model. The head tests are being made using NRZ write techniques.

The NRZ phase recording technique proposed for MEM-BRAIN has been under study. These studies have resulted in circuit designs

and design ground rules for clock coding-decoding of the data. This recording technique is based on phasing the bit pattern of recorded data in a specific order according to track number.

Two clocks are provided at 180° phase difference, each in combination with a 90° delay element. These are used to produce an ordered pattern of information storage with 90° phase intervals. The combination of this technique with moderate cell spacing assures uncrowded bit patterns. On read-back of the recorded information, two signals are derived in parallel. One is the recorded data and the other is servo position control data. During servo positioning action, a direction sense indication and odd or even track signal are derived by comparing the demodulated signals from a pair of heads. The track signals are used to update the contents of an arm position register (recirculating loop). The sense indication provides the information needed for final track-seeking (centering) servo action.

E. HEAD TRANSPORT SERVO

A preliminary head transport servo motor has been designed and prototype models have been tested. These tests have been conducted with the linear motion motor driving a shaft guided by ball bushings, Figure AII-7. Results of these tests have shown that the predicted maximum access times are achieved even under the high friction conditions presented by the ball bushings. A later version of the servo motor for use in the design proofing model file has been designed and several units are in fabrication. This arm motor will drive a tubular shaft supported by an internal hydrostatic gas bearing. This tubular shaft carries both the drive winding and the roving read/record heads. A preliminary test model of this head transport assembly is shown partially disassembled in Figure AII-8.

Control circuits for driving the servo in response to the previously described positioning and direction sense information are being designed.

F. GAS BEARINGS

During the concept proofing phase, consideration was given to development of a hybrid hydrostatic-hydrodynamic gas bearing support for the rotating disk stack. Fabrication of a test model was initiated, and carried far enough to provide reasonable assurance that material stability would be adequate for the purpose. This effort was then

suspended because it was not considered essential to the design proofing model development, and because existing gas bearing technology at Autonetics was deemed adequate to assure successful completion at a later date.

Work has continued on gas bearing support for the head arms, and on the slider pads for head-to-disk spacing control.

A series of configuration test models has been fabricated for support of a "rod" arm in external journals. Successful gas bearing action has been demonstrated. Models of the preferred configuration with a tubular arm supported by internal gas bearings are well along in fabrication, but have not yet been tested to determine the necessary parameters (restrictor configuration and radial clearance requirements) for proper operation.

Various forms of slider pads for head support have been subjected to preliminary tests. These led to the discovery that the slight local flexibility of the disk surface aids in maintaining a constant gas bearing gap. Specifically, it was found that a simple pad with a spherical surface of 14 in. radius provided excellent flotation on a full-size foil disk at 1200 RPM. Conversely, experiments with a particular configuration of small pad carefully lapped to a flat surface gave a jump transition from "Kingsbury type" flotation of large gap at small load to direct contact (no flotation) when the load was increased. Investigations are continuing in the areas of a) pad aspect ratio, b) pad surface shape, and c) drag link configuration for connection of the pad to the arm.

G. LOGIC AND INTERFACE

The design proofing model of the MEM-BRAIN File is planned to work both with a RECOMP III computer and with manual keyboard entry and oscilloscope display. Logic and interface electronics are being designed to use RECOMP III spare boards. To demonstrate the final goal of using integrated circuits as the principal electronic elements, the fixed heads for the clock, sector and recirculating loops will employ such circuits. Circuit requirements for performing the internal logic and interface control have been determined. Studies are currently underway to determine the number and size of recirculating loops to be included for demonstration of the high versatility of this technique of data manipulation.

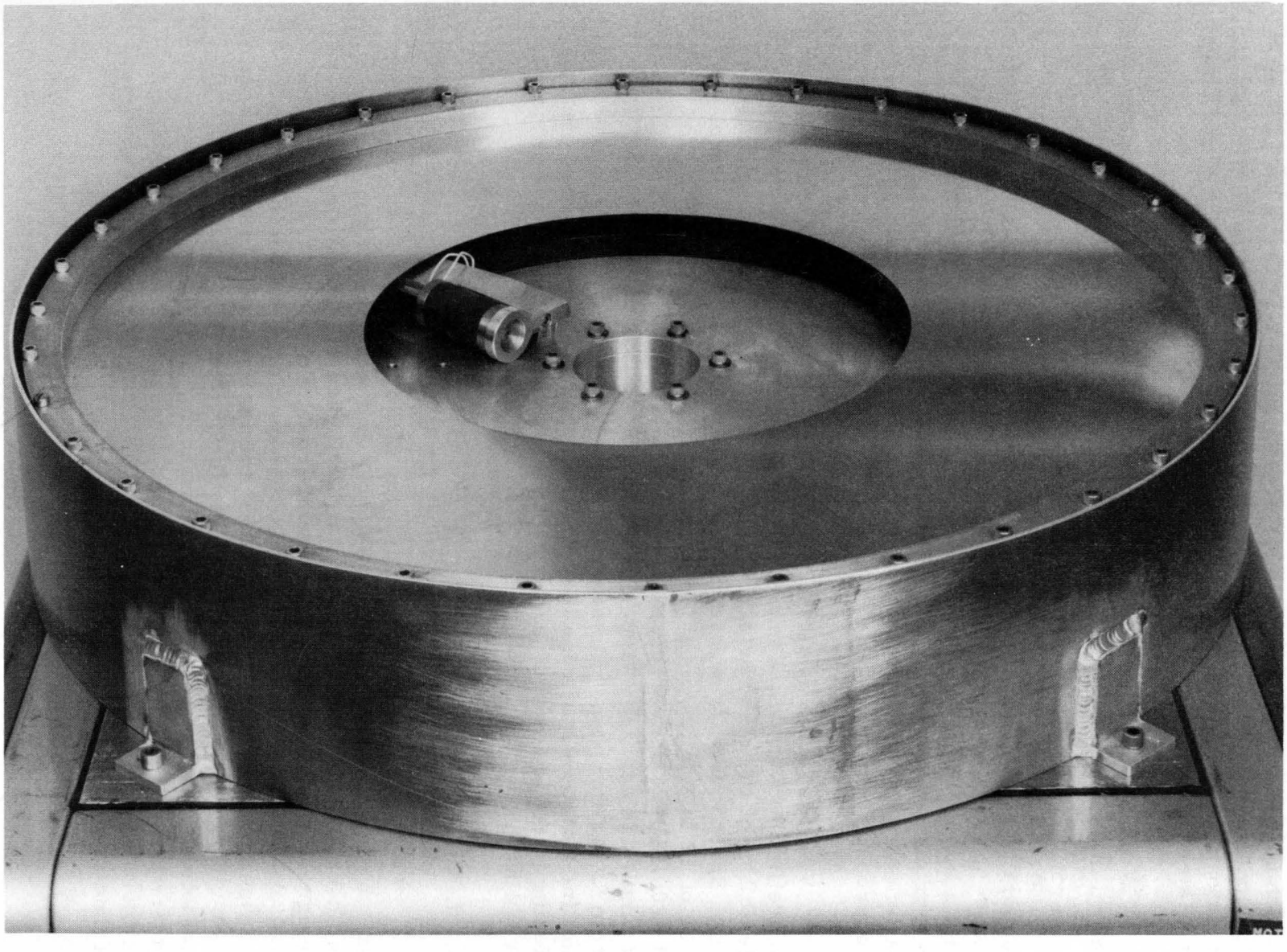


Figure AII-1. MEM-BRAIN Design Proofing Model

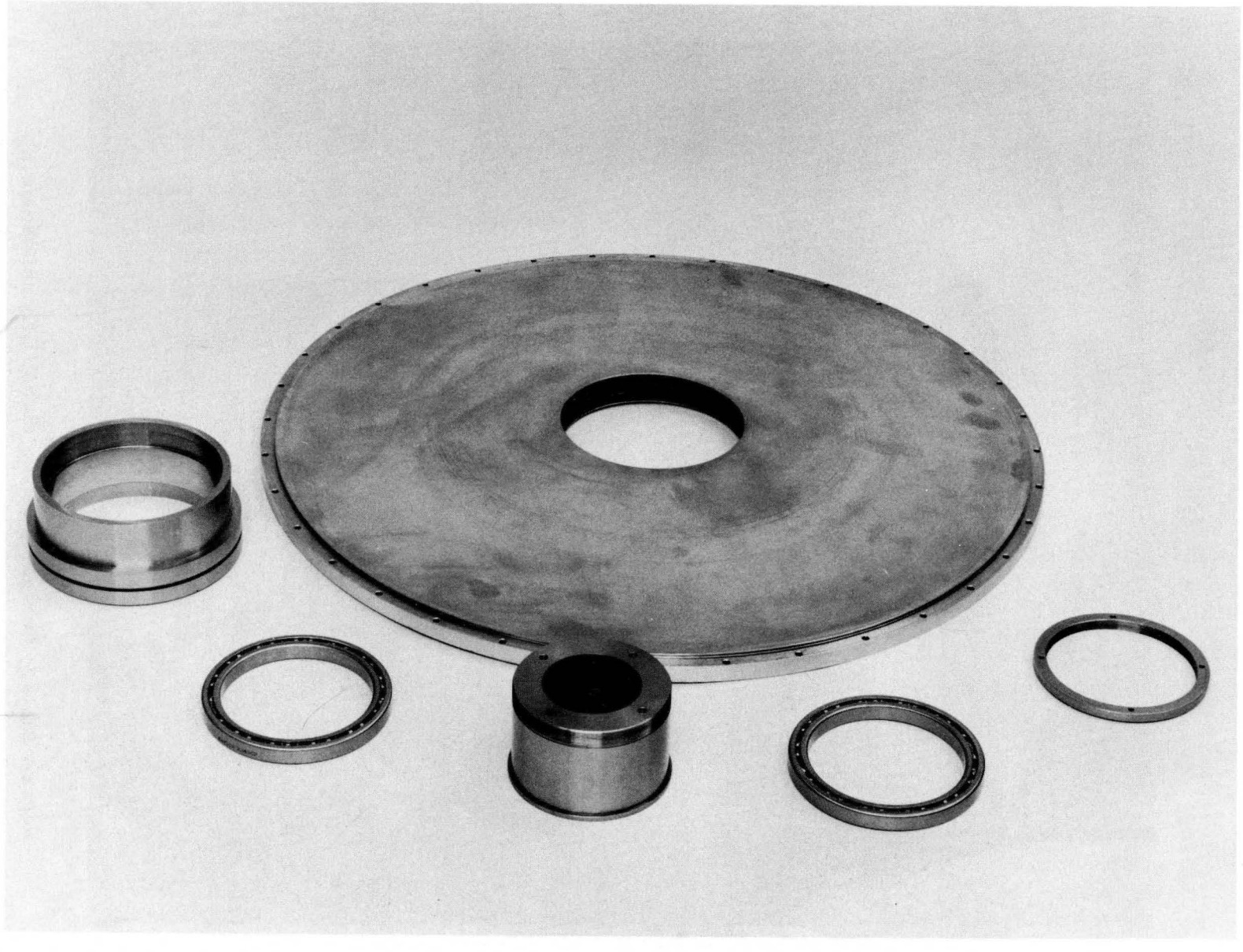


Figure AII-2. End Bell Drive Member, Exploded

Figure AII-3. Design Proofing Model Cabinet Mounting

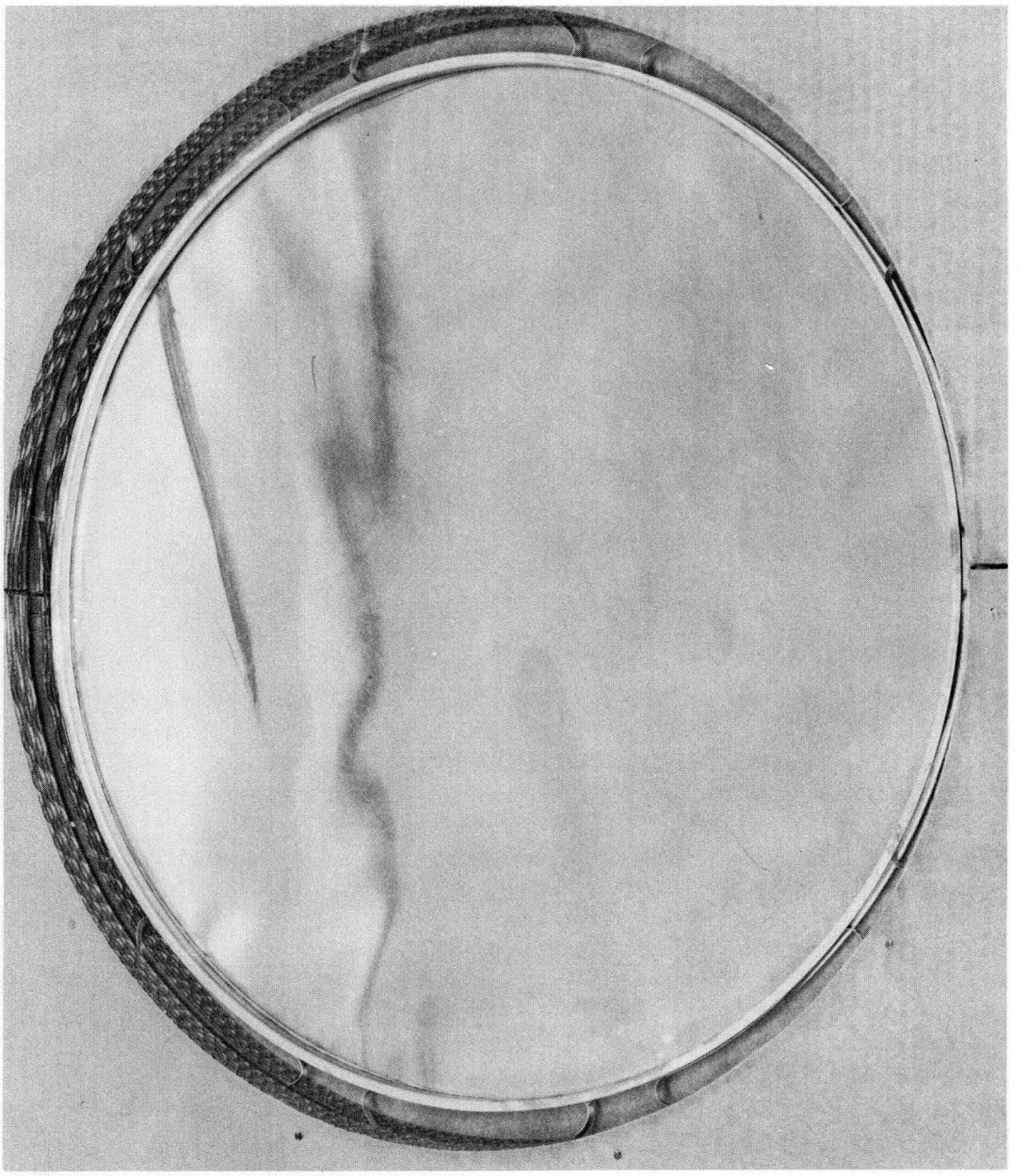


Figure AII-4. Hoop Mounted Plated Foil

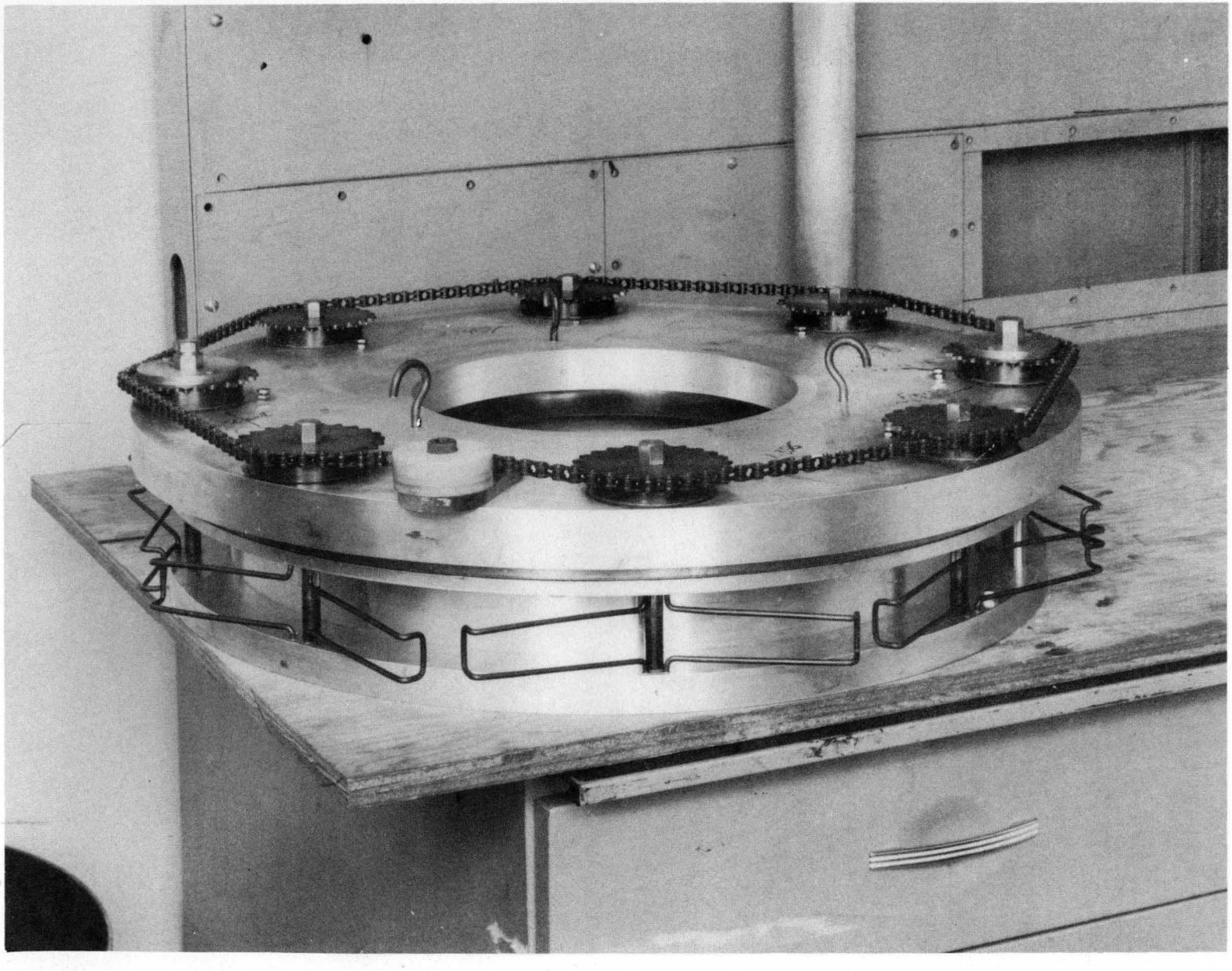


Figure AII-5. Precision Taut Disk Forming Press

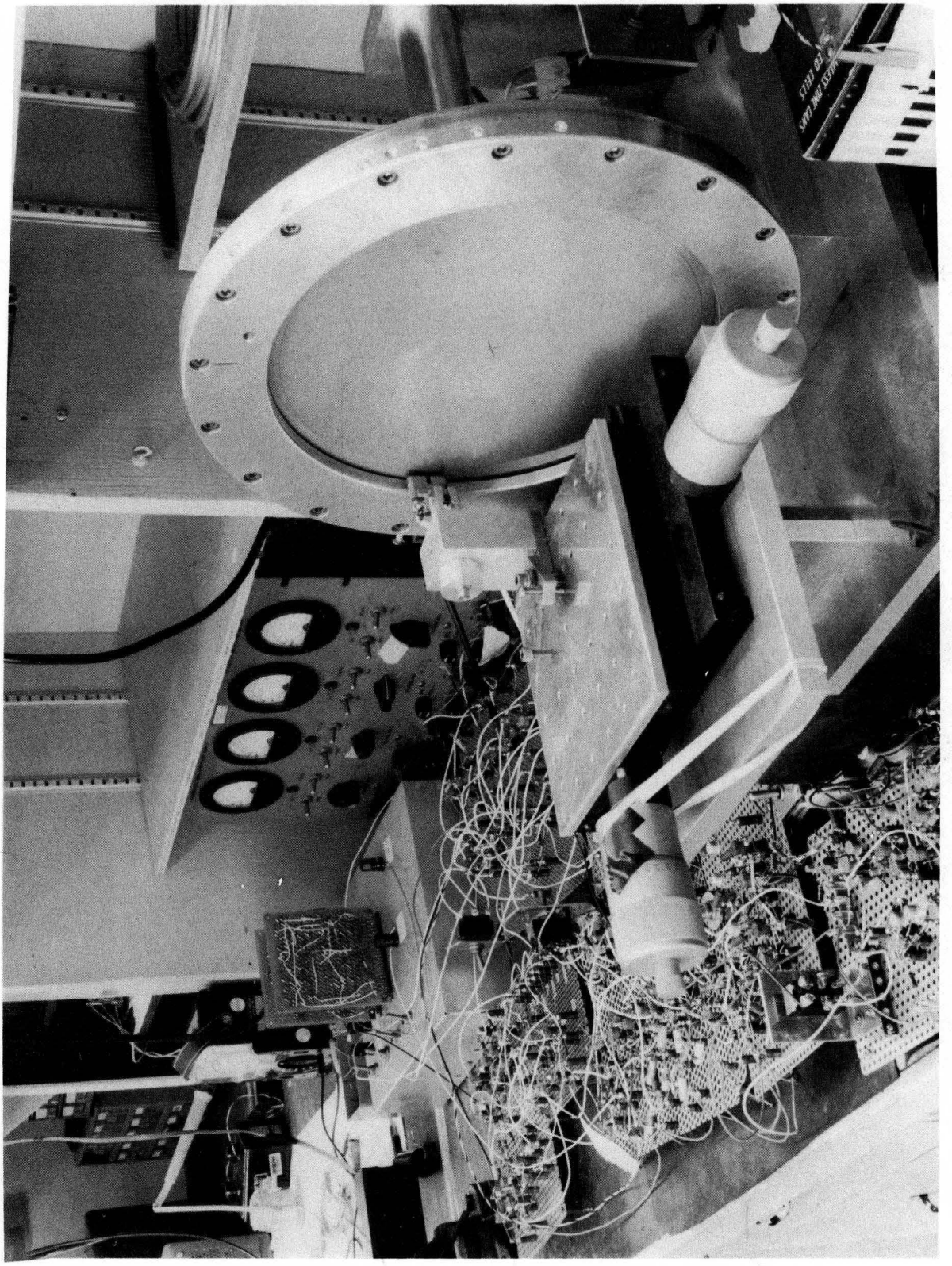


Figure AII-6. Twelve Inch Disk Test Apparatus

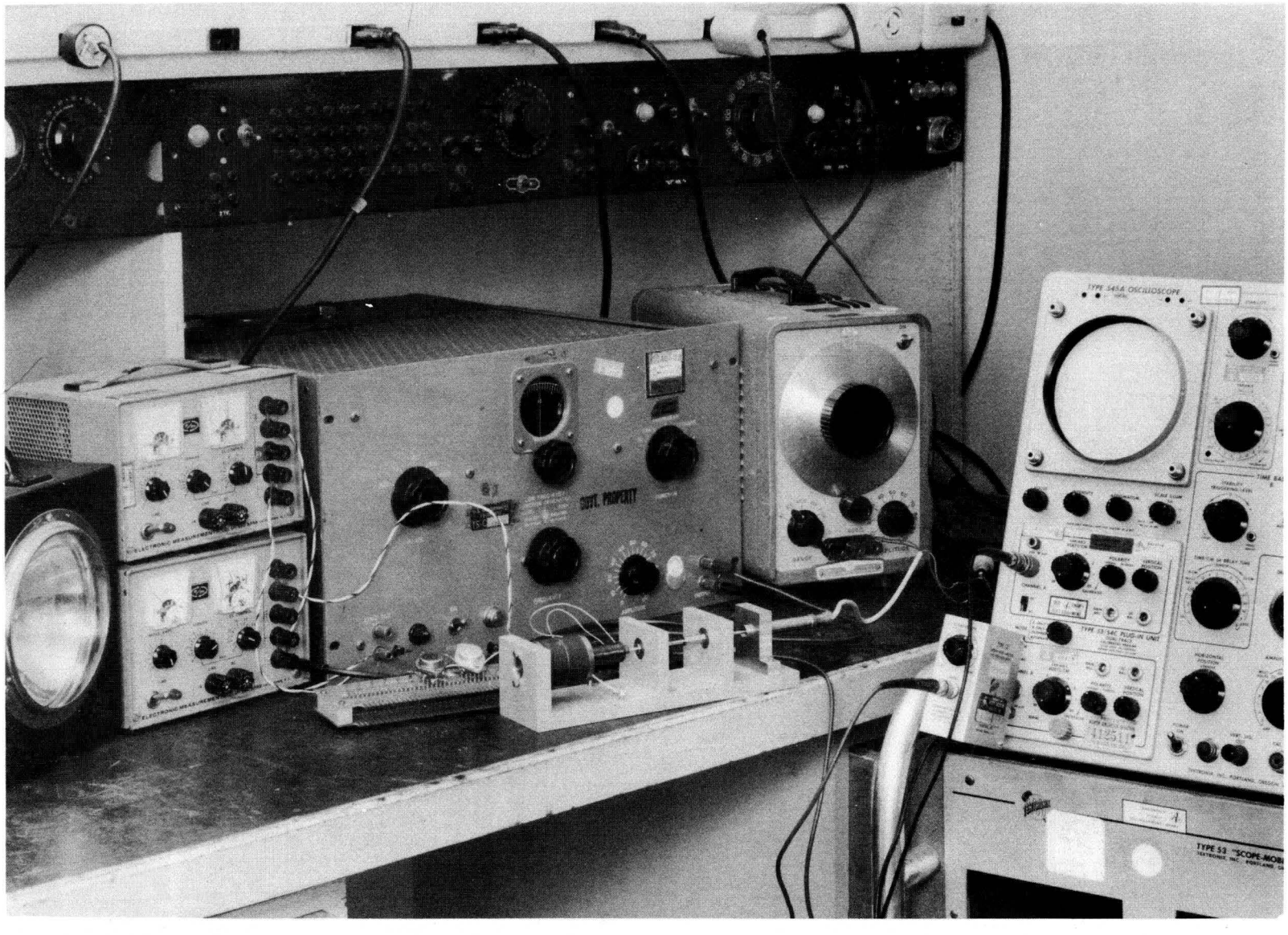


Figure AII-7. Arm Drive Motor Test Equipment

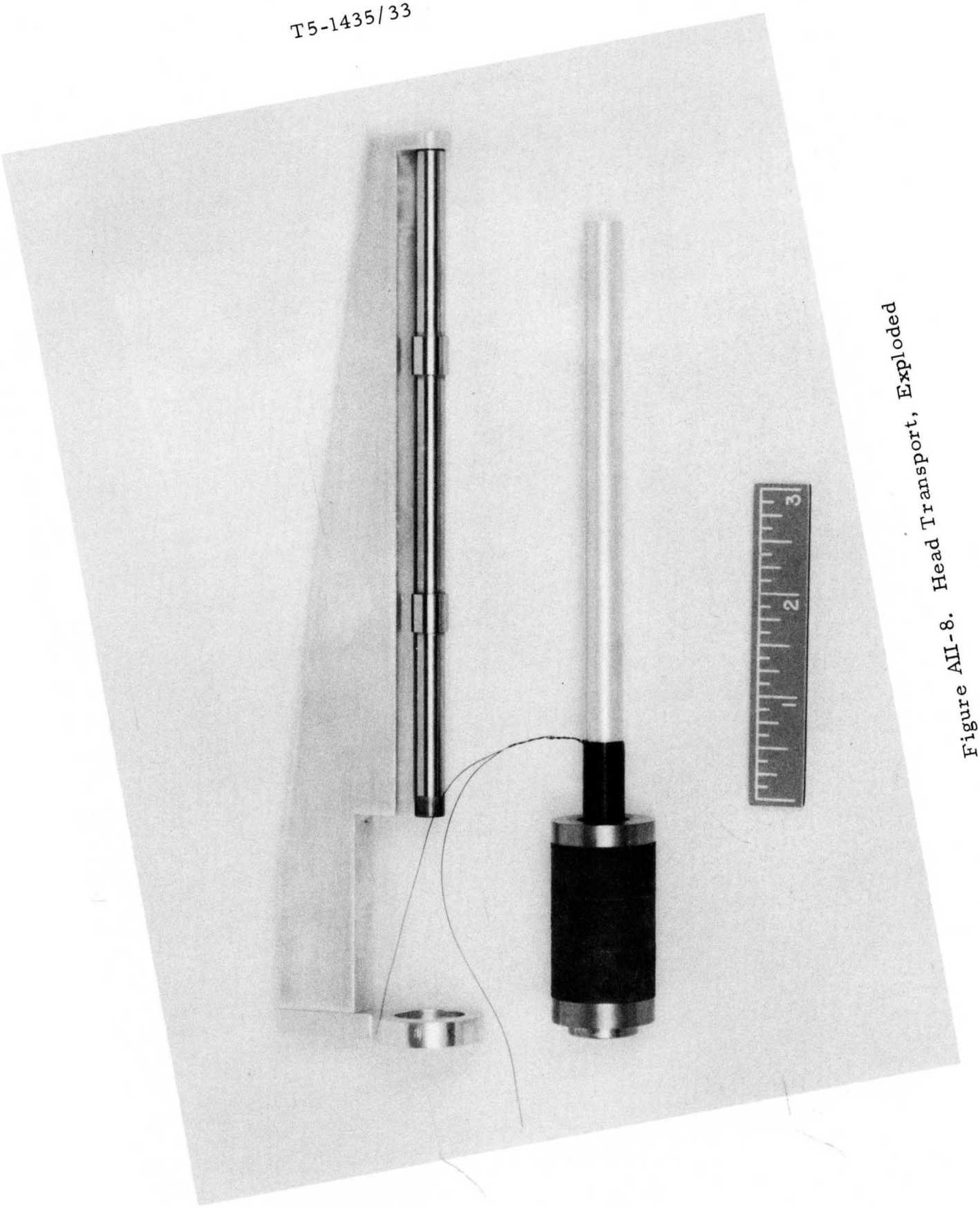


Figure AII-8. Head Transport, Exploded

APPENDIX III. FIXED HEAD AND SHORT LOOP OPERATION AND UTILITY

A. INTRODUCTION

It is possible to construct certain registers, buffers, and logical elements with the aid of recirculating loops in a rotating magnetic memory. Medium speed digital computers have long found the cost of storing information on magnetic surfaces is much less than for storing in other memories suitable for electronic manipulation of data. These computers often make optimum use of such loops and registers to minimize their total cost. In fact, several machines have been built with less than seven logical flip-flops contained in their entire arithmetic and control structure. Placing two heads on the same track, some number of sector lengths apart, provides a lower-capacity memory than that of a full channel but with a proportionally lower access time. More than one such loop may be placed on a given track. If there are normally 100 sectors around the disk, then two heads spaced 10 sector lengths apart may be used to provide a 10-word capacity loop with an access time of one-tenth the access time of a track containing but one head. Logic can be placed between the read and the write circuitry to alter the data being written. By the serial nature of the operation, only one bit can be altered at a given clock time. This yields an accumulator at a cost of one carry flip-flop and four gates if two such loops are used---a very low price indeed. If an extra delay flip-flop is inserted with or without placing the heads one bit closer together, the recirculation loop can be used as a shift register. Shift occurs when the loop length is altered from normal by gating the flip-flop into or out of the loop. A combination of the add and shift by such methods produces a multiply or divide operation. As can be seen, the material costs are not very great.

An objection frequently raised is that the multiply time or divide operation is a number of bit times equal to the square of the loop length in bits. Relatively long manipulation times do indeed accrue when utilizing such controls and registers in data handling. However, the simplicity of equipment for control is such as to yield an extremely high total data flow rate when logically sequential operations are manipulated in a like manner. Some specific examples of applications of short loop utility are described in the following sections.

B. BUFFER TRACK FOR SERIAL DATA TRANSFER

The problem of moving data within a disk file generally requires transfer between different channels and sectors. Transfer of data between channels merely involves reading from one channel and writing on another channel. Transfer of data between sectors presents a timing problem that requires a delay between the reading and writing stations. For maximum flexibility, a variable delay from one word to just under a full disk channel is needed.

Assume that a block of information starting with a sector address F_s is to be transferred to a portion of disk storage starting with sector address T_s. It will be necessary to introduce a space delay between the reading and writing stations equal to the difference

$$D_s = T_s - F_s$$

To obtain the desired delay, consider a single disk track having combination read/write heads spaced at intervals increasing in length by successive powers of two. Figure AIII-1 shows such a head spacing arrangement for a track containing sixteen words of storage. If we place a head arbitrarily at the starting position on the track, the next head is positioned one word along in the direction of rotation, another head is placed two words further along, another head is placed four words further along and the last head is placed eight words further along, occupying a position one word before the first head as shown. In our example, address registers T_s and F_s and a difference register D_s will be provided, each containing four bits. Decoding of the difference bits determines the interconnections between the heads on the delay track. Using the example of Figure AIII-1, suppose that we wish to transfer a block of data that starts at sector two (F_s) of a given disk channel to a region of a different channel beginning at sector thirteen (T_s). Since the sector position of all heads in the main disk store is fixed, information read from sector two of a given channel cannot be written into sector thirteen of another channel until exactly eleven word times (D_s) later. Hence the four bits of the difference register D_s are as indicated in Figure AIII-2. Clearly, the existence of a binary one or zero in the D_1 position indicates whether an odd or even number of words of delay is required and hence whether the one word portion of the buffer track, between head positions 0 and 1, is to be used. Similarly, the D_2 bit position indicates whether or not the two-word portion of the buffer track, between head positions 1 and 3, is to be used, etc.

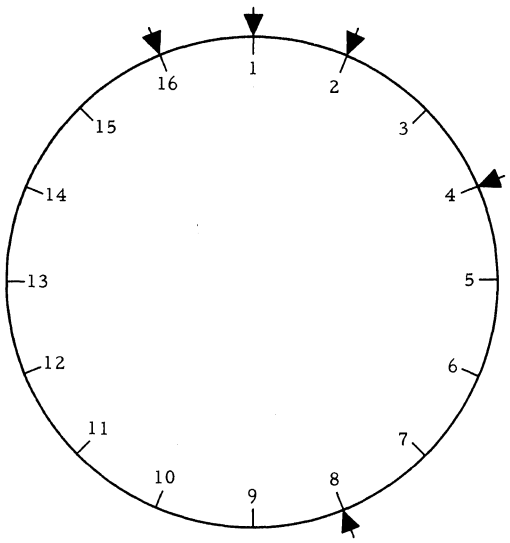


Figure AIII-1. Buffer Track Head Arrangement

D_4	D_3	D_2	D_1
1	0	1	1

Figure AIII-2. Difference Register D_s

In the specific case shown, data read from the source track is written at position 0, read out at position 4, and rewritten at position 8, then finally read out at position 16 for writing on the target location, thus experiencing the required eleven word delay. Detailed logical equations for definition of these operations may readily be written.

If common read/write heads are used on the main disk, transfer of data between sectors served by the same head requires an additional full channel buffer. Since continuous data transfer is desired, separate read and write heads must be used which cannot have a full channel displacement. We can obtain a full channel buffer by placing heads one-half word apart to provide a delay of a full channel minus one-half word. The extra half-word can be obtained by the inclusion of an additional head in the original buffer track of Figure AIII-1, placed one-half word beyond the head at position 16. The arrangement is shown in Figure AIII-3.

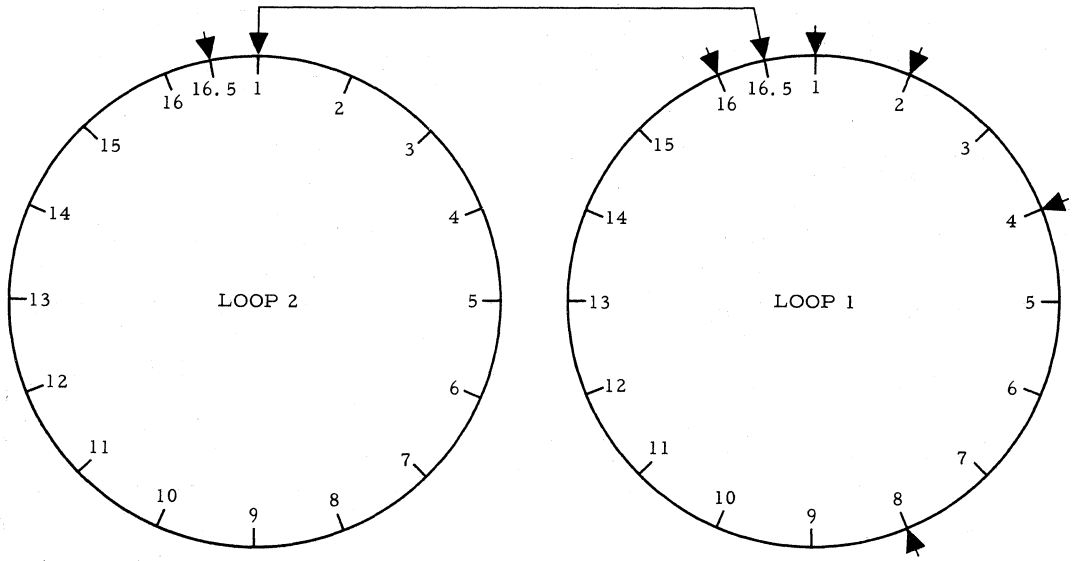


Figure AIII-3. Extended Buffer Arrangement

Suppose a signal is available that indicates a transfer is to be made between sectors served by the same read/write head. Additional logic will provide for reading from the head at position 16 1/2 on the first loop into position 1 of the second loop, and reading out the final signal for re-recording from position 16 1/2 of the second loop, to provide a full channel delay in addition to the sector change.

The necessity to provide a buffer delay in excess of two channels in the MEM-BRAIN File can be avoided by arranging the data in sequence from surface to surface rather than channel to channel on the same surface. For example, we can designate the outside track of the topmost disk as channel 1, the outside track of the next lower disk as channel 2, and so on until the outside track of the lowest disk is channel N, the next to the outside track of the topmost disk then becomes channel N+1, etc. In this case, the extra buffer channel of Figure AIII-3 would be needed only when transfer is to occur within a particular track or between tracks whose channel addresses differ by a multiple of N. Discrepancies in timing that result from the placement of the read/write heads on the buffer track can be compensated for by the introduction of external electronic delays either prior to writing or after reading.

While the above description has used a 16-word loop for example, the principles involved may obviously be applied to loops of different length. Logical extensions of this principle have been developed to handle 8-bit byte parallel operation, variable word length requirements, etc., for inclusion as desired in MEM-BRAIN.

C. CONTENT SEARCH

By the use of suitable fixed head storage, automatic content searching may be accomplished as indicated by the following example. Assume a fixed head mask track and two fixed head descriptor limit tracks. The mask serves to limit the portion of the file to be searched; the descriptors define the particular content sought. Consider a file track consisting of 1024 16-bit fields (2 8-bit characters per field). A 64-bit instruction will specify a 10-bit field address, an operation code and tag bits followed by a pair of 16-bit descriptors. Execution of such an instruction generates the mask as a multiplicity of fields, each of 16 binary ones in the mask track corresponding to the specified search limits. It will also store the descriptor limits in their respective tracks. Logic then determines whether the contents of a record field corresponding to the mask fall within the limits prescribed by the descriptor tracks. Possible tests for descriptor match include equality (same limits), upper bound (lower limit zeros), lower bound (upper limit ones) and interval test. Short loops store and accumulate record fields, identified by instruction tag bits, and also tally and store addresses of those records satisfying the search conditions. The tag bits are stored on the descriptor tracks just before the mask is read. These tag bits determine whether the corresponding record field is to be copied into a temporary storage loop or added into an accumulation loop. If copied into temporary storage, it awaits the result of the full record test to determine subsequent action. If later retrieval of the entire record is required, only the record address in the file is copied into a loop to await trnsfer to a push-down register. Automatic tallying of the content-identified records occurs in another loop if called for by the operation code.

The example chosen corresponds to the track length planned for the MEM-BRAIN File. The use of this track as 1024 16-bit fields, rather than 128 128-bit sectors, has no effect on the interrecord gap requirements, so is entirely compatible.

D. RECORD UPDATING

Partial alteration of a record or group of records may be accomplished by using a mask track to specify the fields to be altered. A fixed head modifier track is then used to hold the new data to be stored.

Data from the original record is transferred directly to a new (updated) record track when the mask reads "0." When "1" occurs in the mask track, the new data is read from the modifier track into the updated track.

E. DATA MERGE

The problem of merging (inserting) additional words at appropriate points (alphabetic order, for example) into an existing record occurs frequently in data processing. Fixed head storage may be used to accomplish this function as herein exemplified.

The words to be inserted are initially stored in one-word recirculation loops. The existing record, or the first portion of it whose length is less than a full track by the number of words to be inserted, is transferred to a multi-head track, with heads spaced by powers of two word lengths, but in inverse order to those used for serial data transfer. This track is connected to form a precession loop whose length is maintained equal to the (instantaneous) number of words in the record by appropriate head switching. The words from the short loops are taken in order, and compared with the word being read from the end of the precession loop. When this comparison shows that the new word belongs in front of the word being read, it is written into the record in the precession loop in place of the existing word. Meanwhile, the existing word is transferred temporarily to a one-word delay loop and logic is set up to increase the length of the precession loop by one word. It is again compared with the next new word. If this word is also to be inserted, the existing word is recirculated in the delay loop and the logic is further modified while the new word is recorded. The delayed word is written in its proper place by the head which has been the beginning of the precession loop. Then the switch in loop length is activated and the operation continues.

If merging of a group of words longer than the difference between the existing record and a full track length is required, the operation described above is carried to completion on the first part of the

existing record. (All new words have been compared and inserted if required.) Then this portion of the merged record is returned to permanent storage, and the next portion of the existing record is brought to the precession loop and processed in turn. This process is repeated as often as necessary to complete the merge operation. Alternatively, multiple precession loops may be used for simultaneous processing of long records. Similarly, if more new words are to be inserted than the available one-word loops, batches may be withdrawn from temporary storage to load the one-word loops. The final operation in any case is the transfer of the merged record to permanent storage.

APPENDIX IV. MEM-BRAIN FILES PRELIMINARY SPECIFICATIONS

1.0 SCOPE

1.1 Scope - This specification covers the operation and performance requirements of four configurations of the MEM-BRAIN File digital storage system.

1.2 Classification - The equipment covered by this specification shall consist of the following four sizes of MEM-BRAIN Files:

1.2.1

Size Designation	Data Capacity-Bits	Size	Weight
6 arm	201,326,592	23 in. x 23 in. x 11 in.	90 lbs
12 arm	402,653,184	23 in. x 23 in. x 14 in.	150 lbs
30 arm	1,006,632,960	23 in. x 23 in. x 23 in.	250 lbs
60 arm	2,013,265,920	23 in. x 23 in. x 38 in.	400 lbs

2.0 APPLICABLE DOCUMENTS

2.1 General - The following documents of the issue indicated form a part of this specification to the extent specified herein.

Specifications

Military

MIL-E-5400G	Electronic Equipment, Aircraft, General Specification for, dated 15 May 1964.
FED-STD-222	Radiation Standard for Communications and Other Information Processing Equipment.
MIL-Q-9858A	Quality Program Requirements.

Military Standards

MIL-STD-275A	Printed Wiring for Electronic Equipment, dated 7 September 1960.
MIL-STD-701	Preferred and Guidance List for Transistors, dated 15 April 1961.
MIL-STD-704	Electric Power, Aircraft, Characteristics and Utilization of

NAA Documents

NA5-15836	Output Driver
NA5-15833	Input Network

2.2 Document Precedence - This specification shall have precedence over all applicable subsidiary specifications. Where the requirements of this specification and those documents listed herein are in conflict, the requirements of this specification shall govern.

3.0 REQUIREMENTS

3.1 General Requirements

3.1.1 General Specification - Unless otherwise specified herein, the general requirements of MIL-E-5400G shall apply as requirements of this specification. Where the general specification MIL-E-5400G and this specification conflict, this specification shall govern.

3.1.2 Design - The equipment shall be designed for maximum functional reliability and minimum complexity consistent with the requirements of this specification.

3.1.3 Parts and Processes - In the selection of parts and material, fulfillment of major design objectives shall be of prime consideration. In so doing, the following shall govern.

3.1.3.1 Materials - When the characteristics of standard MIL parts and materials are such that their use will not fulfill the requirements because of size, weight, performance or other reasons, material and parts which exceed the

3.1.3.1 (Cont) requirements of the respective standard parts shall be used wherever they are suitable, and shall be identified by their applicable part numbers.

3.1.3.2 Standard Parts - Military standard parts or Autonetics standard parts shall be used wherever they are suitable, and shall be identified by their applicable part numbers.

3.1.3.3 Non-Standard Parts - When a non-standard part is used, the meeting of general material requirements such as non-flammable, fungus resistant, non-toxic, etc., and the meeting of environmental conditions as required by specification MIL-E-5400G shall be of prime consideration.

3.1.3.4 Microminiature Parts - Where microminiature electronics are used, the performance requirements shall exceed the requirements of the equivalent conventional design; although, the microminiature design may not conform to all of the detail requirements.

3.1.3.5 Non-Standard Parts and Material Approval - Non-standard parts will be procured to Autonetics standard procedures. Successful completion of the Acceptance Tests will constitute the acceptance of the parts, procedures, and methods used in the fabrication and testing of the equipment.

3.1.3.6 Metals - Metals of the corrosion resistant type shall be used wherever possible. Those metals that are not corrosion resistant and are required in the system design shall be suitably protected to resist corrosion during service.

3.1.3.7 Dissimilar Metals - Dissimilar metals shall not be used in intimate contact unless suitably protected against electrolytic corrosion.

3.1.4 Functional Modules - The units shall contain easily replaceable modules. Wherever possible, each module shall provide a complete function and shall contain all components necessary for performing that function.

3.1.5 Interchangeability - Serialized assemblies having the same manufacturer's part number shall be functionally, electrically, and dimensionally interchangeable.

3.1.6 Nomenclature and Nameplates - Nomenclature assignment and nameplates for equipment identification shall be in accordance with Autonetics procedures.

3.2 Design and Construction - The equipment shall conform with all of the applicable requirements of MIL-E-5400G for design, construction, and workmanship, except as otherwise specified herein.

3.2.1 Integrated Semiconductor Circuits - Integrated circuits (I. C. 's) shall be used wherever practical and shall be restricted to the smallest practical number of different types.

3.2.2 Semiconductor Parts - Every effort shall be made to restrict the use of transistors and diodes to the smallest practical number of different types. MIL-STD-701 will be used as an objective.

3.2.3 Multilayer Printed - Circuit Boards - Multilayer printed-circuit boards shall be utilized to mount and interconnect integrated circuits, semiconductors, and other discrete miniature and microminiature electronic components.

3.2.4 Mounting of Electrical Parts - Electrical components may be mounted on each side of the multilayer printed-circuit board.

3.2.5 Functional Test Points - Functional test points shall be provided on the multilayer printed-circuit boards to facilitate board test and malfunction isolation.

3.2.6 Hardware - Stainless steel fasteners (bolts, screws, nuts, cotter pins, washers, etc.) shall be utilized in the construction of the MEM-BRAIN File.

3.2.7 Weight - The total weight of the units shall not exceed that specified in 1.2.1. This weight does not include mounting supports or cables.

3.2.8 Size - The units size shall be not greater than that specified in 1.2.1.

3.2.9 Accessibility - The electronic modules shall be accessible and removable when the environmental covers are removed.

3.2.10 Cooling - The cooling of the modules shall be accomplished by the use of thermal conducting strips on each module containing IC's. The thermal conductive strips shall conduct the heat from the IC's to the case.

3.2.11 Cooling Air Requirements - The air required to cool the electronics unit shall be externally supplied to achieve the conditions of 3.2.14.2.

3.2.12 Reliability - General reliability design and reporting requirements shall be in accordance with established Autonetics procedures.

3.2.13 Functional Reliability - The design objective reliability of the units shall be a mean time between failure (MTBF) of the following when operated under the conditions specified herein.

6 arm = 6,800 hrs.
12 arm = 4,600 hrs.
30 arm = 3,800 hrs.
60 arm = 3,200 hrs.

3.2.14 Environmental Requirements - The units shall have design objectives to meet the environmental requirements of MIL-E-5400G except as separately specified herein. Salt-spray and sand and dust are excluded.

3.2.14.1 Non-Operating Temperature - The non-operating temperature range shall be -55°C to +75°C.

3.2.14.2 Operating Temperature - The operating temperature range of the MEM-BRAIN File shall be -40°C to +55°C.

3.2.14.3 Vibration - The units shall be designed to meet the vibration requirements of MIL-E-5400G, Curve I, with continuous sweep and excluding resonant dwells, except maximum input shall not exceed ±5g's.

3.2.14.4 Shock, Humidity, Altitude, Pressure - The MEM-BRAIN File shall be designed to withstand the environments of MIL-E-5400G Class IA for altitude.

3.2.14.5 Inclination - The MEM-BRAIN File shall be designed to operate in any position.

3.2.15 Radio Frequency Interference - The generation of Electro Interference by the units shall be controlled to specification FED-STD-222 requirements when all environmental covers are in place.

3.3 Electrical Requirements

3.3.1 Power Requirements - The units shall be supplied with the nominal power listed below. The general requirements are to MIL-STD-704 Category B.

	28 VDC	115 VAC 400 C 3 ph
6 arm	80 watts	650 watts
12 arm	160 watts	650 watts
30 arm	250 watts	825 watts
60 arm	400 watts	825 watts

3.3.2 Grounding - The units shall have four grounds: chassis (CASE) ground, power ground, shield ground, and signal (DC level) ground.

3.3.3 Over Temperature Protection - The units shall provide a set of contacts which open when an over temperature condition exists within the unit. The power specified in 3.3.1 shall be removed whenever the over temperature condition exists.

3.3.4 Functional Requirements - The functional operating requirements are:

All units:

Data bits per track	2^{14} = 16,384
Heads per arm	2^{3} = 8
Tracks per head	2^{8} = 256
Disk diameter	23"
Rotation rate	1200 RPM (Synchronous)

High flexibility of organization for compatibility with any mainframe design, subject only to synchronism requirement in 6 arm and 12 arm units.

Access time, direct: 100 ms (maximum)
Format: Serial or parallel by bit, byte or character
Rate: 500,000 items (bit, byte, character) per second maximum

3.3.4 (Cont) In/Out Synch: Ready strobe
Multiple in/out connections (computers, etc) possible with appropriate controls.

6 Arm Unit
Fetch-put store only
Synchronous interface required
Capacity, bits $3x2^{26}$ = 201, 326, 592

12 Arm Unit
Fetch-put store only
Synchronous interface required
Capacity, bits $3x2^{27}$ = 402, 653, 184

30 Arm Unit
Stored program processing capability
Synchronous or asynchronous interface
Capacity, bits $15x2^{26}$ = 1, 006, 632, 960

60 ARM Unit
Stored program processing capability
Synchronous or asynchronous interface
Capacity, bits 15×2^{27} = 2, 013, 265, 920

3.3.5 Input-Output Characteristics - The following chart specifies the number of data input and output lines for each configuration.

	Inputs	Outputs
6 arm	96	48
12 arm	64	32
30 arm	64	32
60 arm	128	64

The input circuit is specified by NA5-15833. The output circuit is specified by NA5-15836.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 General - The quality assurance program shall be governed by MIL-Q-9858A.

4.2 Acceptance Tests - Acceptance tests will be performed on each unit to Autonetics prepared functional test specification. The following table specifies the manner in which the items of section 3 will be verified.

4.3 Qualification Tests - No qualification test will be performed.

	Tested	Inspected	Not Applicable	Drawings and Analytical Data
3.1.1			X	
3.1.2				X
3.1.3			X	
3.1.3.1				X
3.1.3.2				X
3.1.3.3				X
3.1.3.4				X
3.1.3.5			X	
3.1.3.6				X
3.1.3.7				X
3.1.4				X
3.1.5		X		
3.1.6		X		
3.2				X
3.2.1			X	
3.2.2				X
3.2.3				X
3.2.4				X
3.2.5				X
3.2.6				X

	Tested	Inspected	Not Applicable	Drawings and Analytical Data
3.2.7	X			
3.2.8	X			
3.2.9				X
3.2.10				X
3.2.11			X	
3.2.12			X	
3.2.13				X
3.2.14				X
3.2.14.1				X
3.2.14.2				X
3.2.14.3				X
3.2.14.4				X
3.2.14.5				X
3.2.15				X
3.3.1	X*			
3.3.2				X
3.3.3				X
3.3.4	X			
3.3.5	X			

*Excluding transient conditions.

5.0 PREPARATION FOR DELIVERY

5.1 Preservation and Packaging - Preservation and packaging of the units shall be adequate to prevent damage in delivery by commercial carriers.

6.0 NOTES

6.1 Definitions

6.1.1 Reliability - Reliability is the probability of an item performing its purpose adequately for the time required under the environment specified. For the purposes of this specification, reliability will be considered to be defined as the mean-time-between-failure requirements of this specification.

6.1.2 Mean-Time-Between-Failures - The total measured operating time of a population of equipment items divided by the total number of failures within the population during the measured time period is the MTBF for that population of equipment between the early life and wear-out failures. In the case of exponentially distributed time between failures, the MTBF is the reciprocal of failure rate.