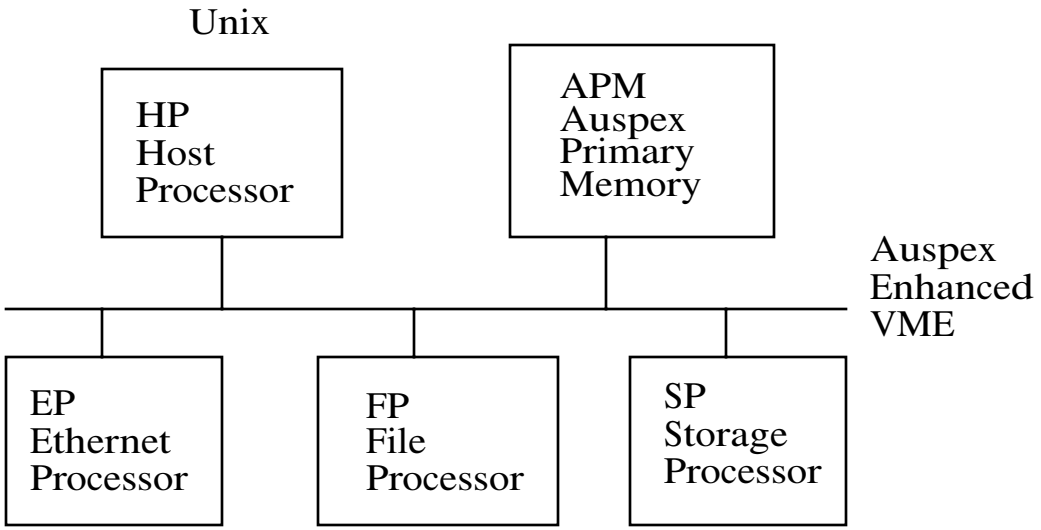
Auspex Architecture

AUSPEX

System Architecture



Functional multi-processing

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Software Architecture

Functional multi-processors running mostly in one VME address space (some boards have their own local space not shared on VME)

Lightweight kernel variously called M16, FMK

128 byte messages (256 bytes in next release for NFS V3)

Unsolicited messages sent by writing pointer to HW FIFO

Host has FMK driver so that it can talk to the other boards

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VME Bus Backplanes

NS5000, 6000, 7000	14 slot backplane, .8” spacing
NS3000	7 slot backplane, .8” spacing
NS7000/200	4 slot backplane, 1.6” spacing
NS7000/700	12 slots, 6 slots 1.6”, 6 .8”
	enhanced cooling

High density connectors, adding grounds for reliability

Physical slot IDs

Somewhat larger than VME 9U form factor

Injectors, ejectors

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VME Bus protocols

Auspex Enhanced VME 32 protocol -

32 lines address, 32 lines data.

Extra protocol to get true 60MB/sec burst VME32

(uses reserved address modifier decode)

Auspex Enhanced VME 64 bus (IOP3, SP5)

Same physical backplane

Multiplexes 64 lines, 1 address cycle followed by multiple data cycles (typically 32 cycles for 256 bytes)

64 bit address used, MBus like - 36 bits physical

(today's software limited to 32 bits - 4GB)

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Host Processor Evolution

HP1	OEM Sun 3E 68020 + memory card (2 boards)
HP2	OEM Sun 3E 68020 + Auspex memory (1 board)
HP3	Auspex 68020 board
HP4	OEM Sun 1E Sparc 1 + Auspex memory (1 board)
HP5	Auspex Sparc 2 40Mhz CPU, MBus, MVIC
HP6	Auspex Sparc 55Mhz HyperSparc
HP7	Auspex Sparc 90Mhz HyperSparc
HP8	Auspex Sparc 125Mhz HyperSparc
HP10	Auspex Sparc Axil chipset, 100% Sun Compatible, MVIC64 *Dual MBus modules, local boot*

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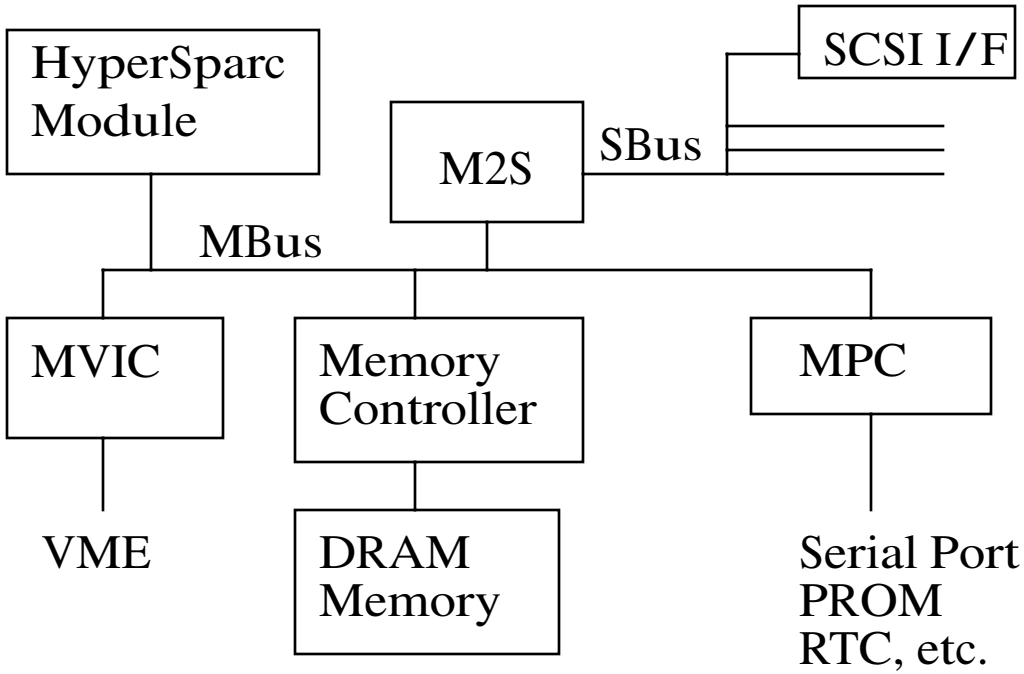
Host Processor Architecture



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Auspex Primary Memory Evolution

1. Clearpoint VME memory board
2. APM1 Enhanced VME32 support
3. APM2 Different connectors for memory modules
4. Became part of memory of IOP

   (IOP1,2 Auspex memory modules

   IOP3,4 Industry standard SIMMs)

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Ethernet Processor Evolution

(originally called the ANC, the Auspex Network Controller)

EP1 Auspex design, 2 x 10Mb Ethernets,
20Mhz 68020 CPU, 256KB memory

EP2 EP1 with 512KB memory

EP3 40Mhz 68EC030 CPU,
Ethernet fuses on front panel

then became part of IOP

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File Processor Evolution

FP1 Auspex design derived from EP1

20Mhz 68020 CPU, 256KB SRAM, 4MB DRAM

FP2 40Mhz 68EC030 CPU, 512KB SRAM, 16MB DRAM

then became part of IOP

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Storage Processor Evolution

(originally called the PSA, the Parallel SCSI Adaptor)

SP1 Auspex design, 10 SCSI channels,
20Mhz 68020 CPU

SP2 SP1 with only 5 SCSI channels for NS3000

SP3 Add support for 1 MB Write Cache
(10 SCSI channels, 20Mhz 68020 CPU)

(SP3E SP3 with more SRAM for optional products)

SP4 Support for 3.5" disk drives, 6 SCSI channels,
40Mhz 68EC030

SP5 SP4 with VME64 support
50Mhz 68030, 2 MB write cache (optional 8 MB)

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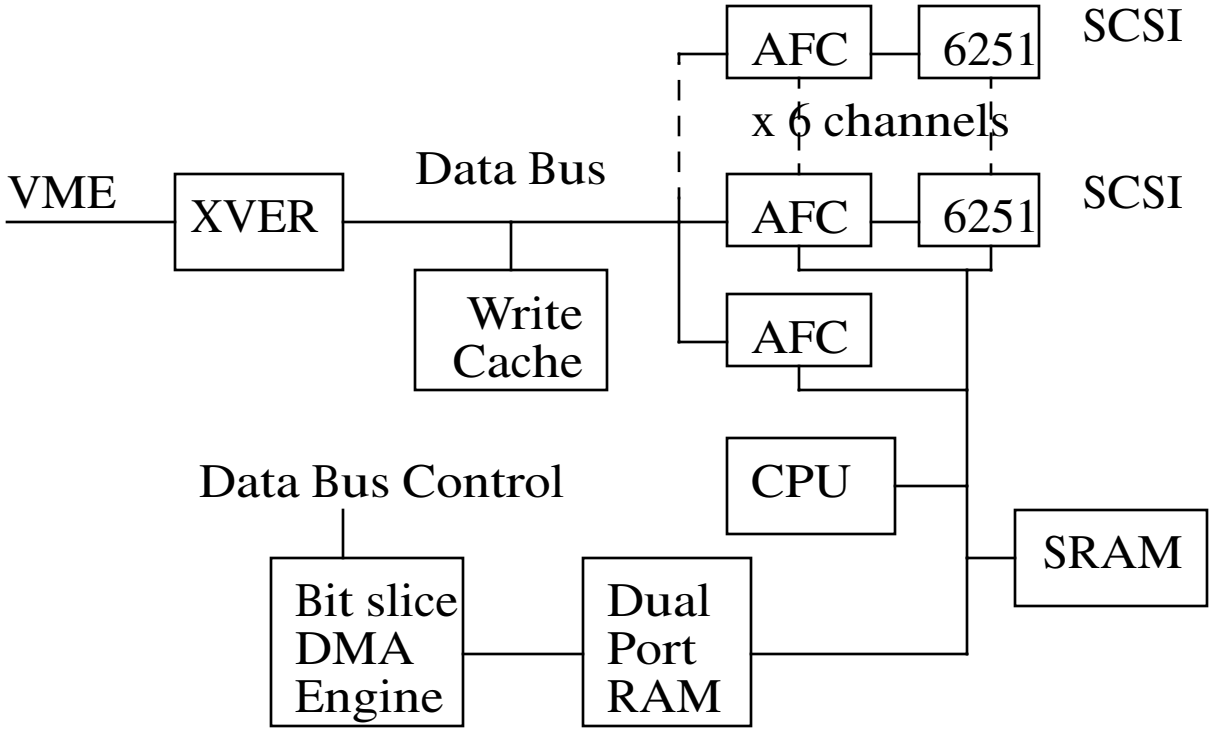
Storage Processor Architecture



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I/O Processor Evolution

IOP1 Combined Network Processor, File Processor, & APM

40Mhz Sparc CPU, MBus, MVIC

IOP2 55Mhz HyperSparc

IOP3 60Mhz HyperSparc, MVIC64

Axil chip set, SRAM execution memory

IOP4 100Mhz HyperSparc, RMC3

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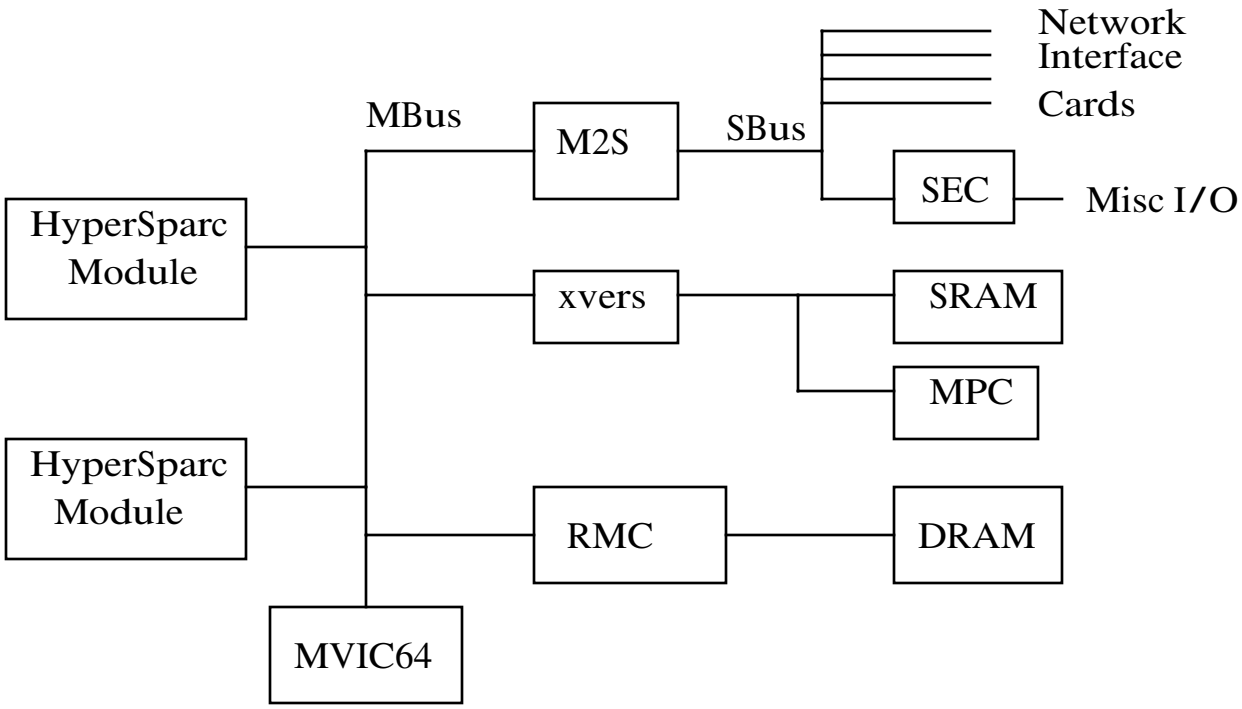
IOP3,4 Architecture



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System Cabinet Evolution

1.	2.	3.	4.	5.	6.	7.
	1.5	1.6	1.7	1.8	1.8.1	1.9
NS5000 /NS5500	NS6000	NS7000 /500	NS7000 /600	NS7000 /650	NS7000 /700	
Big cabinet (NS5500 was improved performance)	HP5	Mack Truck 1 Big Cabinet 5.25” disks SP3, IOP1	Mack Truck 2 Big Cabinet 3.5” disks	Mack Truck 2 Big Cabinet SP5, IOP3	12 slot Backplane IOP4	Env. Monitor
NS3000		/200		/250	Harness for Environmental Monitor	
Ninja Small cabinet 10 disk drives		Roadrunner Small cabinet 3.5” disks		Roadrunner Small cabinet SP5, IOP3		
				/150 Roadrunner SP4, IOP1		

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Futures

System Interconnect

Local busses

Processors

Drive interfaces

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