AMERICAN TELEPHONE & TELEGRAPH INFORMATION SYSTEMS

S4BUS - AT&T *UNIX*™ PC EXPANSION BUS

SPECIFICATIONS

ISSUE 1.3

CONTENTS

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SPECIFICATIONS

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1. GENERAL

This section contains a general description of the S4BUS, the conventions used within this specification, and definitions of the terms applicable to the S4BUS.

1.1 General Description

The S4BUS is a custom, multimaster, synchronous expansion bus that contains data, address, and timing signals present internally to the AT&T UNIX™ Personal Computer. It is tied to the AT&T UNIX PC internal bus structure to such an extent that the bus timing is totally predetermined by the AT&T UNIX PC. There are no data transfer handshaking signals even for bus masters. This synchronous bus architecture provides a fixed and controlled bus bandwidth; and permits the use of simple control logic in each bus master. The S4BUS provides the means for connection expansion memory, expansion I/O, and expansion bus master cards. It supports one two Megabyte expansion memory address space and eight one-quarter Megabyte expansion I/O address spaces.

The AT&T UNIX PC is configured to accommodate three expansion cards in the main unit; or two in the main unit and six in a proposed expansion box. When the expansion box is used one of the three slots in the AT&T UNIX PC will contain a bus repeater card. Each expansion slot is identified by a three-bit code that is permanently wired into each slot connector. These slot ID bits determine the physical address space for memory and I/O expansion cards plugged into expansion slots. Expansion memory cards are supported only in the main unit.

The S4BUS also provides a multi-level bus-cycle by bus-cycle arbitration protocol, and a two-level interrupt protocol. Bus arbitration logic is centralized and based on synchronous system timing. Arbitration is pipelined and occurs at the end of the previous bus cycle. This allows the transfer from one bus master to another without switching delay. Bus masters may retain bus mastership until preempted by another bus master of higher priority. Ordinarily each master controls the bus just long enough for one bus cycle. Bus priority is determined by slot position. Slot three in the main unit has the highest priority and slot one the lowest. Priority in the expansion slots will vary, in reference to the other main unit slots, according to which slot is used for the expansion box bus repeater card.

1.2 Standards

Expansion boards should be compatible with safety and agency standards met or exceeded by the AT&T UNIX PC. These include:

American: UL 478 (EDP) and 114 (Office Equipment)
FCC Part 15, Subpart J, Class B
FCC Part 68
AT&T PUB 61100
EIA Standards RS-470, RS-478, and RS-487
EIA Project PN-1361

Canadian: CSA (EDP) and 143 (Office Equipment)
DOC

1.3 Conventions

Table 1 is a list of conventions that are either unique to the S4BUS or stated to prevent any misunderstandings.

TABLE 1. S4BUS CONVENTIONS

CONVENTION	DEFINITION
Active Low	Level significant active low control signals are identified by asterisks (*) after the mnemonic name (eg. RST*) and are active (asserted) when at the logic low level. They are inactive (de-asserted) at the logic high level.
Active High	Level significant active high control signals are identified by plus signs (+) after the mnemonic (eg. RST+) and are active (asserted) when at the logic high level. They are inactive (de-asserted) when at the logic low level.
Valid Signals	Address and Data signals are not characterized as either active high or active low. They are valid when all of the signals on the bus stablize after a transition period

between bus cycles. They are invalid during periods of transition between bus cycles.

Leading Edge	The leading edge of an active low signal is at the signal's high-to-low transition point. The leading edge of an active high signal is at the signal's low-to-high transition point.
Trailing Edge	The trailing edge of an active low signal is at the signal's low-to-high transition point. The trailing edge of an active high signal is at the signal's high-to-low transition point.
Falling Edge	The falling edge of a clock signal is the clock's high-to-low transition.
Rising Edge	The rising edge" of a clock signal is the clock's low-to-high transition.
Bus Notation	The notation <n:m> represents all signals from n and m inclusive. For example: XD<15:00> represents the 16 data bus signals from XD15 through XD00.

1.4 Definitions

Table 2 is a list of definitions for the S4BUS.

TABLE 2. S4BUS DEFINITIONS

TERM	DEFINITION
Bus Cycle	A bus cycle is a number of clock cycles that define the basic unit of time for accessing data via the S4BUS. The number of clock cycles ranges from four to ten depending upon the type of bus cycle. All S4BUS bus cycles begin at the falling edge of XPCK+.
Bus Interface	The AT&T UNIX PC bus interface circuit is the AT&T UNIX PC's driver/receiver interface to the S4BUS, or its equivalent in the expansion box.
Bus Master	An expansion bus master is an expansion card with a bus requester circuit and the capability of driving address, data strobe, and read/write S4BUS signals. Bus masters depend upon the AT&T UNIX PC's memory management unit to provide logical page to physical page translation and other memory management functions. A bus master can be either the AT&T UNIX PC processor, Disk DMA Controller, or Memory Refresh Controller, or an expansion card.

Master Mode	The S4BUS is in the expansion bus master mode during bus cycles that the expansion bus is granted to the expansion bus master. Bus masters on the S4BUS are slaved to bus cycle timing provided by the AT&T UNIX PC.
Bus Requester	Expansion bus masters are referred to as bus requesters during bus arbitration.
Bus Slave	There are two types of bus slaves, memory and I/O. Slaves are accessed by bus masters. The S4BUS signals driven by bus slaves are the XD<15:00> data bus during read cycles, the parity error interrupt signal (XPERR*), and two general purpose interrupts signals (INT01* and INT05*).
Slave Mode	The S4BUS is in the bus slave mode during bus cycles controlled by the AT&T UNIX PC processor, Disk DMA, or Refresh Controller.
Disk DMA	The AT&T UNIX PC includes a Direct Memory Access (DMA) Controller specifically to handle data transfers between the disk subsystem and memory.
Expansion Box	A Proposed six slot chassis that provides the means of increasing the I/O capability of the AT&T UNIX PC.
Expansion Slot	An expansion slot is a position provided in the AT&T UNIX PC or the expansion box to accommodate expansion cards.
Expansion Cards	An expansion card is a circuit card designed to interface with the S4BUS and provide I/O or Memory expansion for the AT&T UNIX PC.
Frame Ground	Frame ground is the same as the "green wire" safety ground of the three wire power cord. Frame ground is connected to signal ground at the power supply and is common throughout the system.
Interrupter	An interrupter is an expansion card circuit capable of driving any of the three S4BUS interrupt signals.

2. SPECIFICATIONS

This section contains the Electrical and Mechanical specifications for the S4BUS. The electrical specifications include bus pin assignments, signal definitions, power, signal levels, and driver and receiver specifications.

2.1 Electrical Specifications

The following electrical specifications apply to all S4BUS signals except for the analog signals which are specified in Section 3.6. The AT&T UNIX PC backplane is relatively short and as such presents negligible IR drop and transmission line propagation delays. The backplane in the expansion box will be relatively long and will present approximately 100 pf loading to bus signals.

2.1.1 *S4BUS Pin Assignments* Table 3 details the S4BUS signals and their associated pin assignments for the AT&T UNIX PC expansion connector.

TABLE 3. EXPANSION CONNECTOR PIN ASSIGNMENTS

ROW 1			ROW 2			ROW 3		
#	I/O	NAME	#	I/O	NAME	#	I/O	NAME
01	P	-12	34	P	+12	67	P	+12
02	I	INT05*	35	O	XI/OEN*	68	I/O	XR/W*
03	P	+5	%36	O	XENRAS*	69	I	INT01*
04	P	GND	%37	I	XPERR*	70	I/O	XUDS*
05	P	GND	38	I/O	XLDS*	71	NC	SPARE 1
06	P	+5	39	O	XRST*	%72	O	XMEM+
07	P	GND	40	O	XPCK+	73	NC	SPARE 0
08	P	GND	%41	O	X20MCK+	%74	O	RFBG*
09	P	+5	42	P	AG	75	I/O	XD15
10	P	GND	43	I	AFT	76	I/O	XD14
11	P	GND	44	O	AFPL	77	I/O	XD13
12	P	+5	45	I	ATPL	78	I/O	XD12
13	P	GND	46	I/O	XD07	79	I/O	XD11
14	P	GND	47	I/O	XD06	80	I/O	XD10
15	P	+5	48	I/O	XD05	81	I/O	XD09
16	O	EXPBG*	49	I/O	XD04	82	I/O	XD08
17	I	EXPRQ*	50	I/O	XD03	%83	O	XMA20
18	P	GND	51	I/O	XD02	%84	O	XMA19
19	P	GND	52	I/O	XD01	%85	O	XMA18
20	P	+5	53	I/O	XD00	%86	O	XMA17
21	P	GND	54	I/O	XA21	%87	O	XMA16
22	P	GND	55	I/O	XA20	%88	O	XMA15
23	P	+5	56	I/O	XA19	%89	O	XMA14
24	P	GND	57	I/O	XA18	%90	O	XMA13
25	P	GND	58	I/O	XA17	%91	O	XMA12
26	P	+5	59	I/O	XA16	92	I/O	XA08
27	P	GND	60	I/O	XA15	93	I/O	XA07
28	O	XID2	61	I/O	XA14	94	I/O	XA06
29	O	XID1	62	I/O	XA13	95	I/O	XA05
30	O	XID0	63	I/O	XA12	96	I/O	XA04
%31	O	XBP+	64	I/O	XA11	97	I/O	XA03
32	P	GND	65	I/O	XA10	98	I/O	XA02
33	P	GND	66	I/O	XA09	99	I/O	XA01

%: These signals are unique to expansion memory and will not be supported in the expansion box.

2.1.2 *Power* The total short term peak power and long term continuous power dissipated by an expansion card shall not exceed 15 watts and 12 watts respectively. The maximum available current per expansion slot is given in table 4.

TABLE 4. SUPPLY VOLTAGE SPECIFICATIONS

MNEMONIC	VARIATION	RIPPLE VOLTAGE	MAXIMUM CURRENT PER EXPANSION SLOT
+5	+/- .25 V	100 mv	2500 ma
+12	+/- .6 V	500 mv	100 ma
-12	+/- .6 V	500 mv	100 ma

2.1.3 *Connector Specifications*

1. Contact Resistance < 50 milliohms
2. Insulation Resistance > 100 megohms pin to pin

2.1.4 *Logic Signal Levels*
Logic signals are specified as logic high and logic low and are defined in Tables 5 and 6 respectively.

TABLE 5. LOGIC LOW VOLTAGE LEVELS

DRIVER OUTPUT VOLTAGE:	0 ≤ VOL ≤ 0.5 Volts
RECEIVER INPUT VOLTAGE:	0 ≤ VIL ≤ 0.8 Volts
S4BUS NOISE MARGIN:	0.3 Volts Minimum

TABLE 6. LOGIC HIGH VOLTAGE LEVELS

DRIVER OUTPUT VOLTAGE:	2.4 ≤ VOH ≤ VCC* Volts
RECEIVER INPUT VOLTAGE:	2.0 ≤ VIH ≤ VCC* Volts
S4BUS NOISE MARGIN:	0.4 Volts Minimum

Note: VCC means the value of the voltage on the +5 S4BUS power leads.

2.1.5 *Signal Receiver Specifications*
Signal receivers are devices for receiving logic signals via the S4BUS driven by the AT&T UNIX PC bus interface circuit or by expansion cards. All receivers should provide diode clamping at -1.5 volts and it is recommended that receivers on the XPCK+, X20MCK+, XENRAS*, and XI/OEN* leads have a minimum hysteresis of 200 mv.

2.1.6 *Input Current Limitations*
Receivers on all signal leads shall conform to the limitations given in Table 7.

TABLE 7. SIGNAL RECEIVER SPECIFICATIONS

Logic Low Level Input Current	IIL ≤	4 ma at VIL = 0.5 Volts
Logic High Level Input Current	IIH ≤	100 ua at VIH = 2.4 Volts
Input Capacitance	CIN ≤	15 pF

2.1.7 *Suggested Layout Rules*

1. The number of receivers on any signal lead should be limited to two.

2. Receivers on the XPCK+, X20MCK+, XENRAS*, and XI/OEN* signals should be placed within 7.5 centimeters (printed wiring path length) of the connector and all other receivers should be placed within 15 centimeters (printed wiring path length) of the connector.

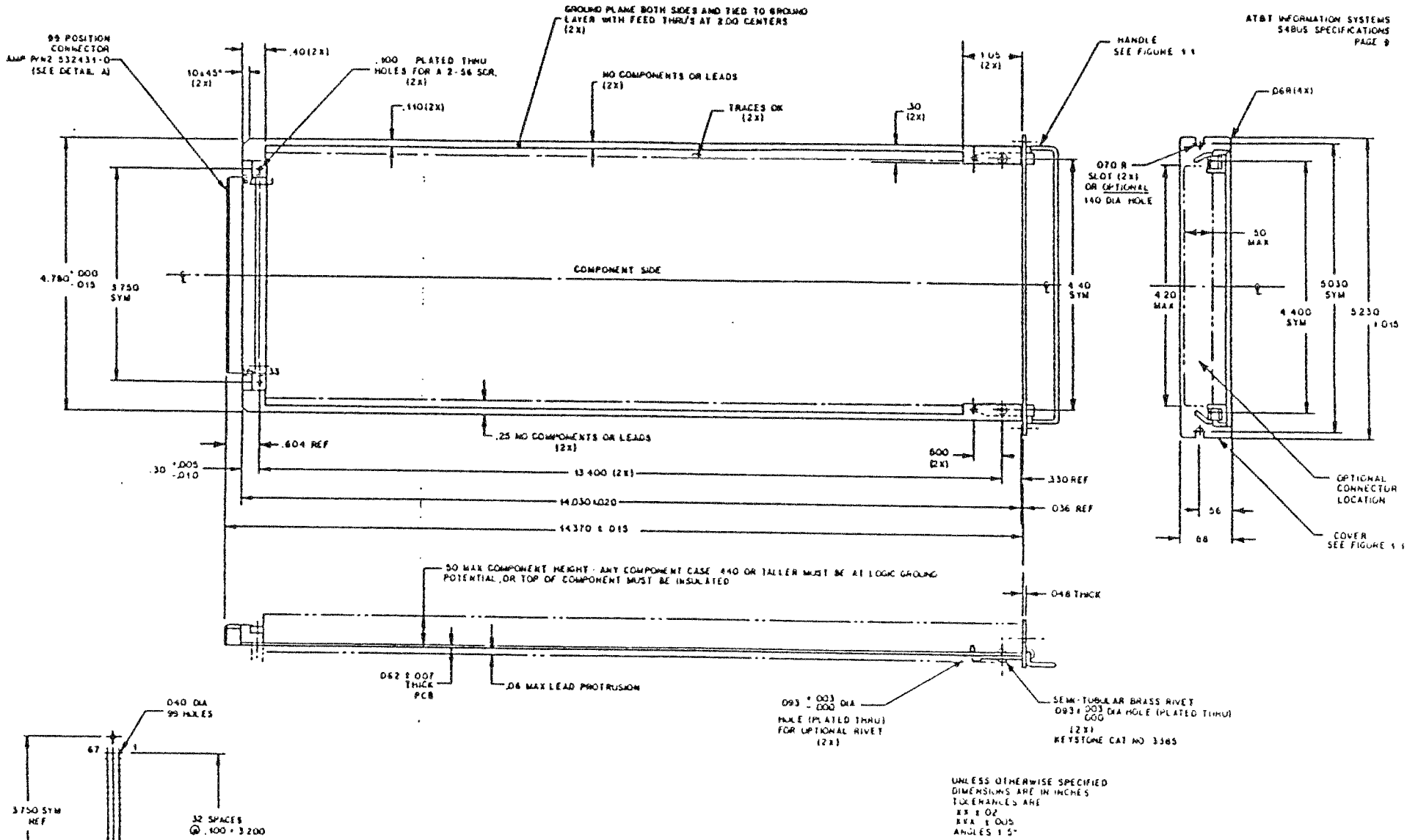
2.1.8 *Signal Driver Specifications*
Signals that are driven by expansion cards fall into two categories: Totem Pole, and Open Collector.

2.1.8.1 *Totem Pole Drivers*
Totem pole drivers are required by bus request signal EXPRQ*, data bus signals XD<15:00>, and (for bus masters only) signals XUDS*, XLDS*, XR/W*, and XA<21:01>. Totem pole drivers shall provide, as a minimum, the electrical DC characteristics given in Table 8.

TABLE 8. TOTEM POLE DRIVER SPECIFICATIONS

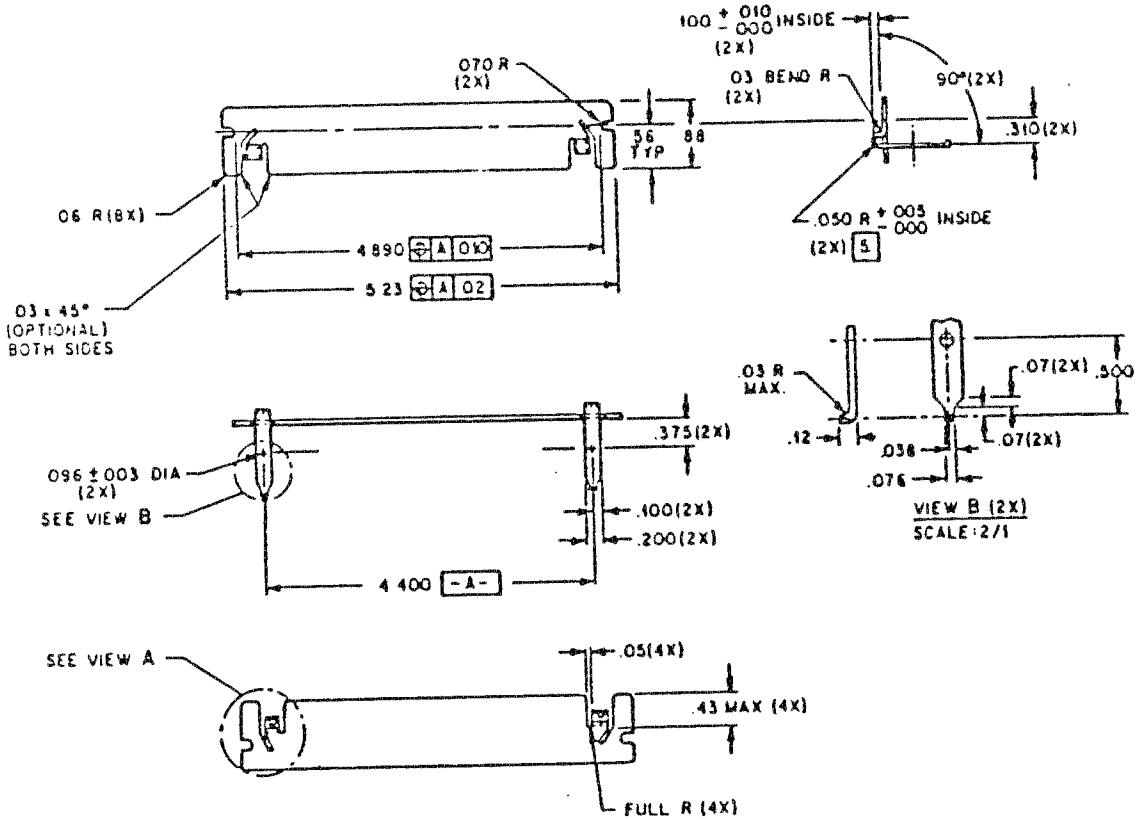
Low Logic Level Output Current:	IOL ≥ 24 ma.
Low Logic Level Output Voltage:	VOL ≤ 0.5 Volts at IOL = 20 ma.
High Logic Level Output Current:	IOH ≥ -3 ma.
High Logic Level Output Voltage:	VOH ≥ 2.4 Volts at IOH = -1 ma.
Output Capacitance:	COUT ≤ 10 pF.

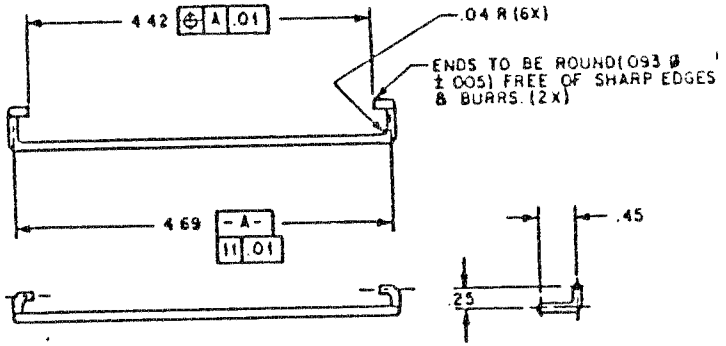
2.1.8.2 *Open Collector Drivers*
Open collector drivers are required for parity error signal XPERR* and interrupt signals INT01*, and INT05*. These signals are designed to be driven by one or more expansion cards and received by the AT&T UNIX PC bus interface circuit. The AT&T UNIX PC bus interface unit provides pull up resistors to establish the inactive high state. These drivers shall provide, as a minimum, the electrical DC characteristics given in Table 9.

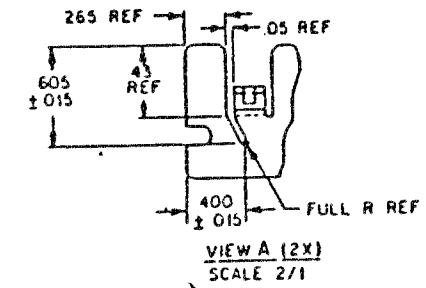


UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE
XX ± .02
XXX ± .005
ANGLES ± 5°

EXPANSION BOARD OUTLINE DRAWING
FIGURE 1







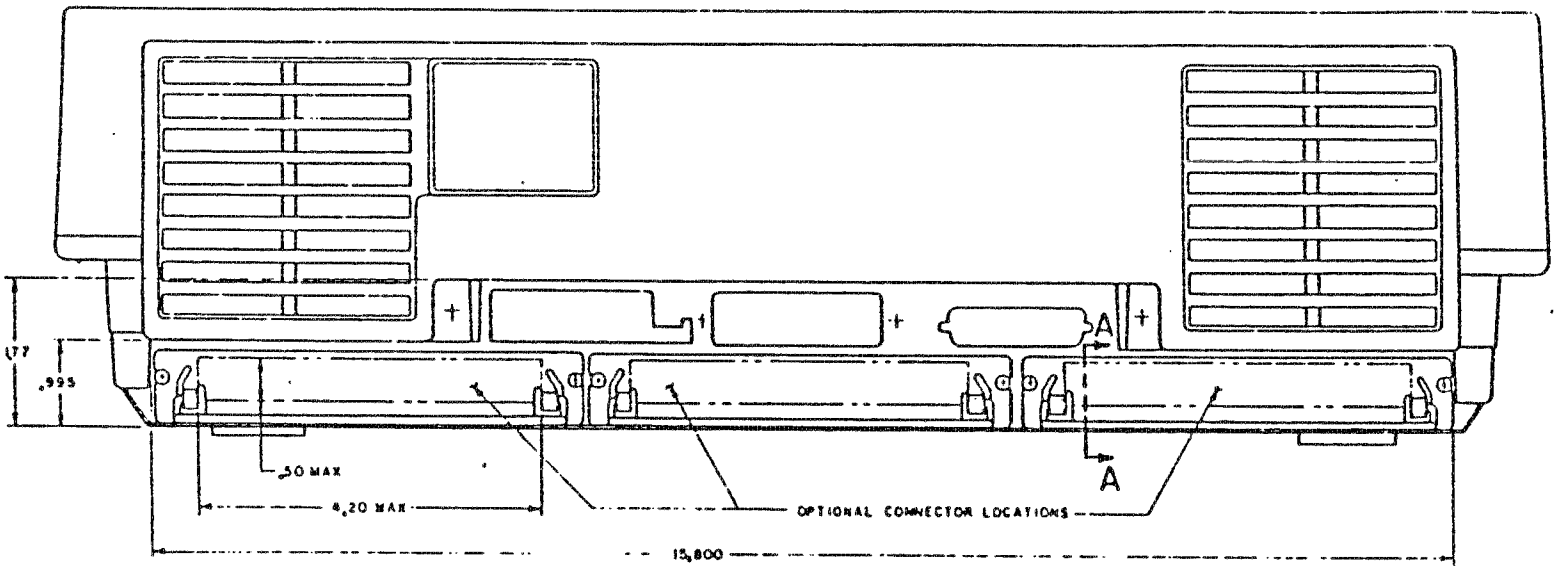
NOTES: UNLESS OTHERWISE SPECIFIED

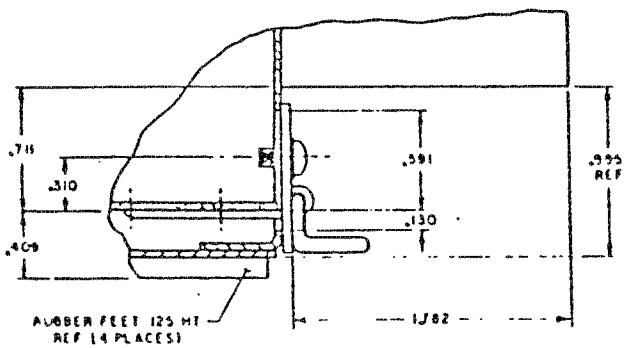
1. MATERIAL: 18 GA. (.0478) CRS
2. FINISH: POST-PLATE ZINC TYPE II, CLASS 2 PER QQ-Z-325 BRIGHT SILVER
3. BREAK & DEBURR ALL SHARP EDGES & CORNERS
4. THIS PART MUST BE MANUFACTURED TO ACHIEVE ZERO DEFECTS
5. THIS FEATURE TO HOLD A .093 DIA WIRE WITHOUT INTERFERENCE (2 PLCS REF)

NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: .093 DIA STAINLESS ROD, TYPE 304
2. FINISH: PART IS TO BE BRIGHT & SHINY; FREE OF SCRATCHES AND OTHER BLEMISHES
3. PART MUST BE MANUFACTERED TO ACHIEVE ZERO DEFECTS

EXPANSION BOARD/ EPLATE AND HANDLE





SECTION A-A

REAR VIEW OF AT&T UNIX PC

FIGURE 1.2

NOTE:
REFER TO THE EXPANSION BOARD OUTLINE DRAWING (FIG 1)

3. BUS SIGNALS DESCRIPTION

S4BUS signals are grouped into seven categories: Data Transfer, Slot Identification, Bus Arbitration, Interrupt, Utilities, Audio, and Power. See Table 3 for pin assignments.

3.1 Data Transfer Signals

This group of signals is used to transfer data between the AT&T UNIX PC and expansion cards. These signals are divided into bidirectional and unidirectional signals.

3.1.1 *Bidirectional Data Transfer Bus Signals*

In the slave mode, bidirectional data transfer bus signals, including the data bus during write bus cycles, are driven by the AT&T UNIX PC expansion bus interface and may be received by all expansion cards. During read bus cycles the data bus is driven by the addressed bus slave.

In the expansion bus master mode, bidirectional data transfer bus signals, including the data bus during write bus cycles, are driven by the bus master and are received by the AT&T UNIX PC bus interface circuit and by all other expansion cards. During read bus cycles the data bus is driven by the addressed bus slave which could include the AT&T UNIX PC main memory.

1. XD<15:00>: Bidirectional Data Bus.

   During read bus cycles the data bus is driven by the addressed slave device, and received by the bus master. During write bus cycles the data bus is driven by the bus master and received by the addressed slave device.

2. XUDS*: Upper Data Strobe (active low).
   XLDS*: Lower Data Strobe (active low).

   These signals are used to access individual bytes within an addressed word (there is no XA0 address signal). The most significant 8-bits (XD<15:08>) of a word is the even byte. They are accessed by the assertion of signal XUDS* (implied XA0 = 0). The least significant 8-bits (XD<07:00>) of a word is the odd byte. They are accessed by the assertion of signal XLDS* (implied XA0 = 1). Both bytes (word access) may be accessed by the simultaneous assertion of signals XUDS* and XLDS*. Table 10 list all possible combinations of the two data strobes during read and write bus cycles and in both the master and slave modes.

TABLE 10. DATA STROBES AND BYTE ACCESS CONTROL

XUDS*	XLDS*	XR/W*	XD<15:08>	XD<07:00>	COMMENTS
1	1	X	-	-	No Access
1	0	1	X	VALID	ODD BYTE READ
0	1	1	VALID	X	EVEN BYTE READ
0	0	1	VALID	VALID	WORD READ
1	0	0	X	VALID	ODD BYTE WRITE
0	1	0	VALID	X	EVEN BYTE WRITE
0	0	0	VALID	VALID	WORD WRITE

3. XA<11:01>: Lower Unmapped Address Bus (11 leads).

I/O Bus Cycles — The Lower Unmapped Address Bus, in conjunction with the two data strobes and the Upper Unmapped Address Bus, is used to address words and bytes of expansion I/O.

Memory Bus Cycles — The Lower Unmapped Address Bus is used in conjunction with the data strobes and the Mapped Address Bus, to address words and bytes within 4K-byte pages of memory.

Refresh Bus Cycles — Eight bits XA<10:03> of the Lower Unmapped Address Bus are used for refresh addresses.

4. XA<21:12>: Upper Unmapped Address Bus (10 leads)

I/O Bus Cycles — The Upper Unmapped Address Bus, in conjunction with the Slot ID bits, the two data strobes and the Lower Unmapped Address Bus, is used to select I/O expansion cards and to address words and bytes within the selected expansion I/O card's address space.

Memory Bus Cycles — The Upper Unmapped Address Bus is used by bus masters as a logical page address input to the AT&T UNIX PC memory management unit. The Upper Unmapped Address Bus (although valid) is not intended to be used by expansion memory cards.

Refresh Bus Cycles — The Upper Unmapped Address Bus is not used during refresh bus cycles.

5. XR/W*: Read/Write

Write Bus Cycles	Asserted Low.
Read Bus Cycles	Asserted High.

3.1.2 *Unidirectional Data Transfer Bus Signals*
The following address and control signals, for all types of bus cycles including bus master bus cycles are driven by the AT&T UNIX PC expansion bus interface and received by slave type expansion cards.

1. XMA<20:12>: Mapped Address Bus (9 leads).
This address bus is unique to expansion memory and will not be supported in the expansion box.

I/O Bus Cycles	The Mapped Address Bus is not intended to be used by slave I/O expansion cards.
Memory Bus Cycles	The Mapped Address bus is the buffered output of the AT&T UNIX PC memory management unit and is used in conjunction with the Slot ID bits for card selection and to address physical pages of expansion memory.
Refresh Bus Cycles	The Mapped Address Bus is not used during refresh bus cycles.

2. XENRAS*: Enable RAS (active low).
This control signal is unique to expansion memory and will not be supported in the expansion box.

I/O Bus Cycles	Control signal XENRAS* is not asserted during I/O bus cycles.
Memory Bus Cycles	Control signal XENRAS* is asserted by the AT&T UNIX PC expansion bus interface to mark the beginning of memory bus cycles.
Refresh Bus Cycles	Control signal XENRAS* is asserted by the AT&T UNIX PC expansion bus interface to mark the beginning of refresh bus cycles.

3. XMEM+: Expansion Memory Select (active high).
This signals is unique to expansion memory and will not be supported in the expansion box.

I/O Bus Cycles	Not asserted.
Memory Bus Cycles	Control signal XMEM+ is asserted by the AT&T UNIX PC expansion bus interface to select expansion memory. XMEM+ is invalid, that is, it may be in any state including changing state several times during the first part of a read bus cycle. Signal XMEM+ is not

asserted if memory access is from a bus master to AT&T UNIX PC on-board memory.

Refresh Bus Cycles — Not asserted.

4. XI/OEN*: Expansion I/O Enable (active low).

I/O Bus Cycles — Control signal XI/OEN* is asserted by the AT&T UNIX PC expansion bus interface to select expansion I/O.

Memory Bus Cycles — Not asserted.

Refresh Bus Cycles — Not asserted.

3.2 Expansion Slot Identification

Expansion slots are identified by signals XID<2:0> that are permanently wired into each expansion slot connector. These signals are intended to be used to automatically select address spaces for I/O and memory cards: Table 11 is a list of the expansion slot identification signals.

TABLE 11. EXPANSION SLOT IDENTIFICATION SIGNALS

XID2	XID1	XID0	SLOT NUMBER	LOCATION
0	0	0	1	AT&T UNIX PC
0	0	1	2	AT&T UNIX PC
0	1	0	3	AT&T UNIX PC
			3	SEE NOTE
0	1	1	4	EXP. BOX
1	0	0	5	EXP. BOX
1	0	1	6	EXP. BOX
1	1	0	7	EXP. BOX
1	1	1	8	EXP. BOX

Note: 0 —> Ground 1 —> Vcc
Expansion box slot 3 duplicates the ID bits of the AT&T UNIX PC expansion slot used for the bus repeater card.

3.3 Bus Arbitration Signals

1. EXPRQ*: Expansion Bus Request (active low).

Signal EXPRQ* is used by bus masters to request bus mastership.

2. EXPBG*: Expansion Bus Grant (active low).

Signal EXPBG* is asserted by the AT&T UNIX PC expansion bus interface to grant bus mastership.

3. RFBG*: Refresh Bus Grant (active low).

   Assertion of signal RFBG* by the AT&T UNIX PC bus interface unit identifies refresh bus cycles. This signal is unique to expansion memory and will not be supported in the expansion box.

3.4 Interrupt Signals

1. INT01*: Interrupt Level 1 (active low).
   INT05*: Interrupt level 5 (active low).

   Signals INT01* and INT05* are general purpose interrupt signals at absolute processor interrupt levels 1 (lowest priority) and 5 respectively. They may each be driven by multiple expansion cards.

2. XPERR*: Parity Error (active low).

   Assertion of interrupt signal XPERR* causes a non-maskable interrupt to the AT&T UNIX PC processor in the next processor bus cycle. Assertion of XPERR* triggers a parity error interrupt on the AT&T UNIX PC processor board and this event causes bus information, including the address at which the parity error occurred, to be latched into a status register. XPERR* need only be asserted during the memory cycle in which the parity error occurs. Signal XPERR* is intended primarily for expansion memory and although it may be driven by I/O and bus master expansion cards it will not be supported in the expansion box.

3.5 Utility Signals

1. XPCK+: Processor Clock Signal.

   Signal XPCK+ is a buffered version of the AT&T UNIX PC 10 MHz clock signal, and is used to define events during bus cycles. It is recommended that this signal be terminated by a series 33 ohm resistor. Signal XPCK+ has a nominal 50 % duty cycle, a maximum frequency tolerance of ±500 parts per million, and is synchronous to the rising edge of clock signal X20MCK+. Note, signal XPCK+ is synchronous to the falling edge of clock signal X20MCK+ on D-60-00216 CPU boards which are associated with AT&T UNIX PC's with serial numbers from 010-00101 to approximately 010-001894.

2. X20MCK+: Clock Signal.

   Signal X20MCK+ is a 20 MHz clock signal from which signal XPCK+ is derived. The maximum skew between XPCK+ and X20MCK+ is ±5 ns. It is recommended that this signal be terminated by a series 33 ohm resistor. Clock signal X20MCK+ will not be supported in the expansion box.

3. XRST*: Reset Signal (active low).

   Signal XRST* is a buffered version of the AT&T UNIX PC system wide reset signal and is asserted at power up and in response

to pushing the reset button. XRST* remains asserted for at least 175 milliseconds. See Section 10 for reset requirements.

4. XBP+: Bad Parity (active high).

   Signal XBP+ is asserted by the AT&T UNIX PC bus interface during memory diagnostics to force bad parity on memory writes. This is intended to be used to cause parity errors on subsequent memory reads at the bad parity location and provides a means of testing the parity detection circuitry. This signal is unique to expansion memory and will not be supported in the expansion box.

3.6 Audio Signals

1. AFPL: Audio From Phone Line.

   Analog signal AFPL is a buffered version of the telephone line audio signal. It is driven by an operational amplifier, DC coupled, and single ended. Signal receivers on AFPL shall be AC coupled and shall have an input impedance greater one kilohm. The gain from tip and ring to AFPL is approximately unity.

2. ATPL: Audio To Phone Line.

   This analog type bus lead is intended for audio signals which are to be transmitted over the telephone line. ATPL is terminated in 50 kilohms and AC coupled by the AT&T UNIX PC telephone circuit. Signals on this lead shall not exceed 1.42 volts peak to peak. The gain from ATPL to the telephone line is approximately unity.

3. AFT: Audio From Tape.

   This analog type bus lead is intended for audio signals which are to be coupled to the AT&T UNIX PC loud speaker. AFT is terminated in 50 kilohms by the AT&T UNIX PC telephone circuit. Signals on this lead shall be AC coupled and shall not exceed 1.42 volts peak to peak. The gain from AFT to the speaker terminals is approximately unity.

4. AG: Analog Ground.

   This analog ground is the return path for the above audio signals.

3.7 Power Signals

1. +5: Plus 5 Volts (8 leads)

   Power at plus five volts is available on these leads for expansion cards. See Table 4 for the 5 volt tolerance and total available power. It is suggested that all +5 leads be connected to reduce contact resistance.

2. GND: Digital Ground (17 leads)

   GND is the digital ground return path for all S4BUS signals and power. It is suggested that all ground leads be connected to reduce contact resistance and ground noise.

3. +12: Plus 12 Volts Power (2 leads)

   Power at plus twelve volts is available on these leads for expansion cards. See Table 4 for the +12 volt tolerance and total available power.

4. -12: Minus 12 Volts Power (1 lead)

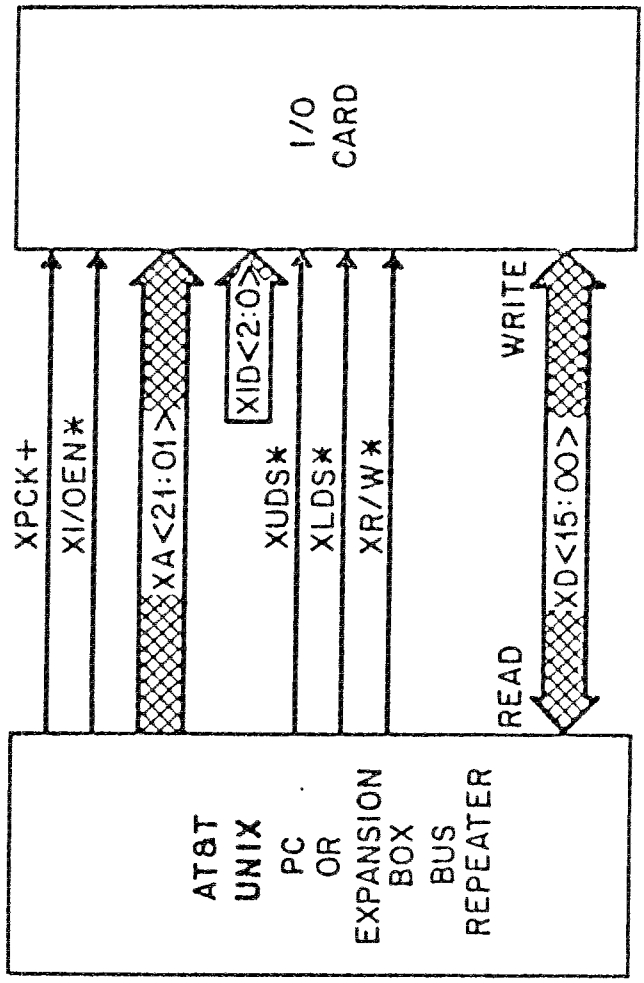
   Power at minus twelve volts is available on this lead for expansion cards. See Table 4 for the -12 volt tolerance and total available power.

4. BUS CYCLE TYPES

There are three basic types of expansion bus cycles supported by the S4BUS: I/O Access, Memory Access, and Memory Refresh.

Expansion boards may contain any combination of memory, I/O, or bus master capabilities. For purposes of this description, I/O, Memory, and Bus Master expansion circuits will be treated separately. Each of the basic bus cycle types, as well as, bus arbitration and bus master timing are discussed in separate sections below. These sections are written from the point of view of the expansion card being discussed. For example, system clock XPCK+ will encounter considerable delay in its path to an expansion card located in the expansion box and it is the delayed version of XPCK+ that is shown on all timing diagrams.

Bus cycles are identified by the state of certain control signals as shown in Table 12.



SIGNAL FLOW DIAGRAM FOR I/O CARDS

FIGURE 2

TABLE 12. CONTROL SIGNAL BUS CYCLE DETERMINATION

TYPE	I/O	MEMORY ACCESS			REFRESH
CONTROL SIGNAL	* TO I/O	EXPANSION BUS MASTER TO: *	XMEM	* TO XMEM	* TO XMEM
XI/OEN*	A	I	I	I	I
XENRAS*	I	A	A	A	A
XMEM+	X	I	A	A	X
RFBG*	I	I	I	I	A
EXPBG*	I	A	A	I	I

Note: * —> AT&T UNIX PC
A —> ACTIVE CONTROL SIGNAL
I —> INACTIVE CONTROL SIGNAL
X --> UNDEFINED

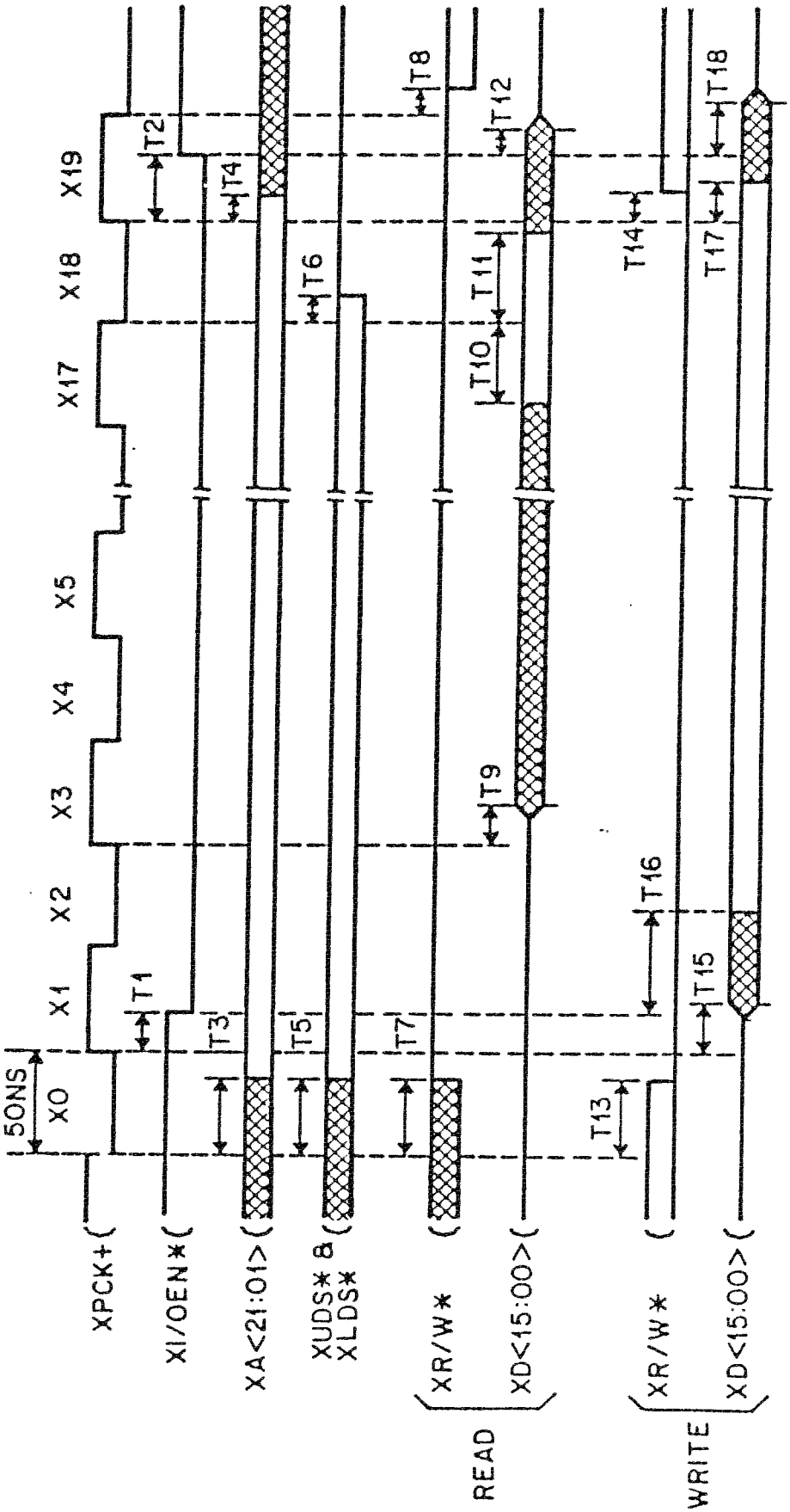
Each half clock cycle of bus clock signal XPCK+ is individually identified with a sequence of X-numbers beginning with X0. This makes it easier to identify particular time intervals within bus cycles. The next bus cycle is marked with a sequence of Y-numbers beginning with Y0.

5. I/O EXPANSION CARD SPECIFICATIONS

Figure 2 is a signal flow diagram for I/O expansion cards. I/O bus cycles are distinguished from all other bus cycles by the assertion of I/O select signal XI/OEN* (see Table 12). Expansion I/O cards are accessible exclusively by the AT&T UNIX PC processor while operating in the Supervisory mode. A "Bus Fault Exception" will occur if the processor attempts to access I/O in the User Mode. I/O is not accessible by expansion bus masters.

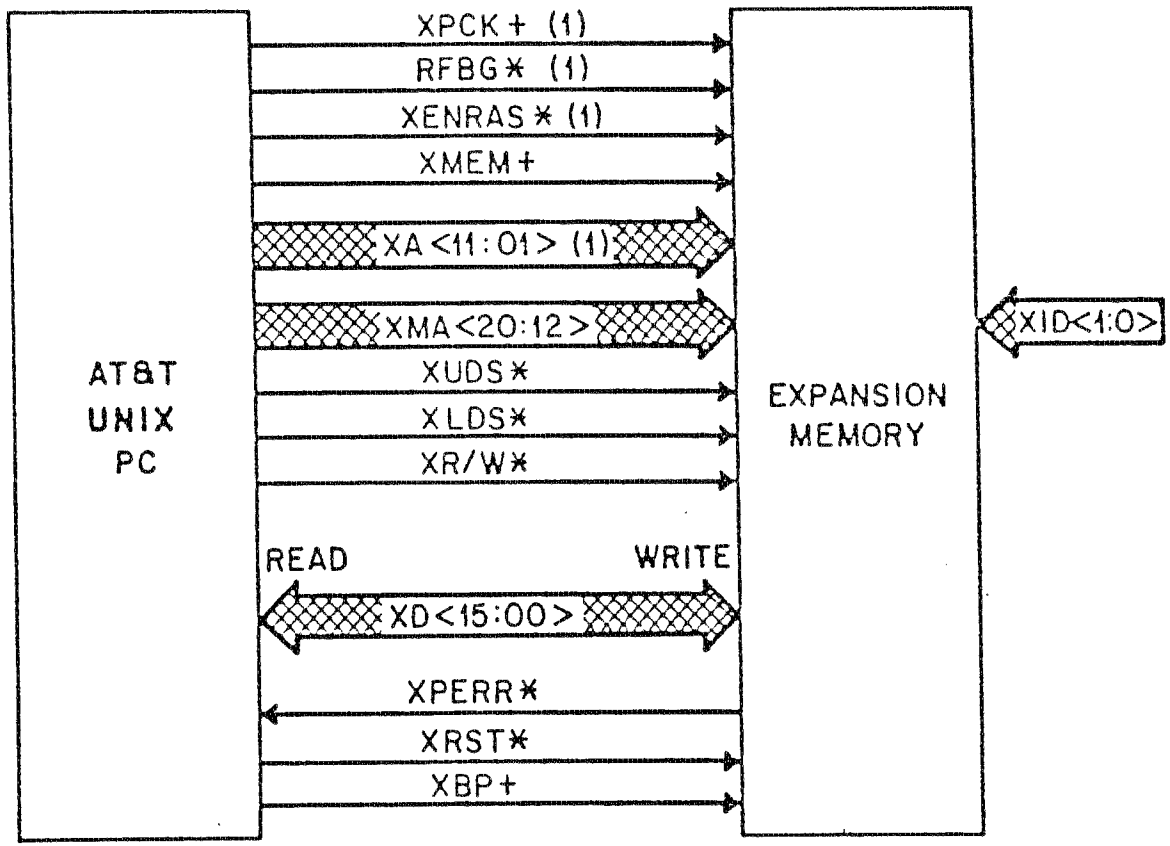
5.1 Expansion I/O Card Selection and Addressing

Expansion I/O cards shall be selected if Unmapped Address bit XA21 equals zero and Unmapped Address bits XA<20:18> match slot identification bits XID<2:0> (See Table 11). The remaining Unmapped Address bits XA<17:01> together with the two data strobes XUDS* and XLDS*, address words and/or bytes within the 256 K-byte address space allowed for each I/O card. Slot-by-slot physical address space for I/O cards is shown in Table 13.



I/O BUS CYCLE TIMING DIAGRAM
(SEE TABLE 14)

FIGURE 3

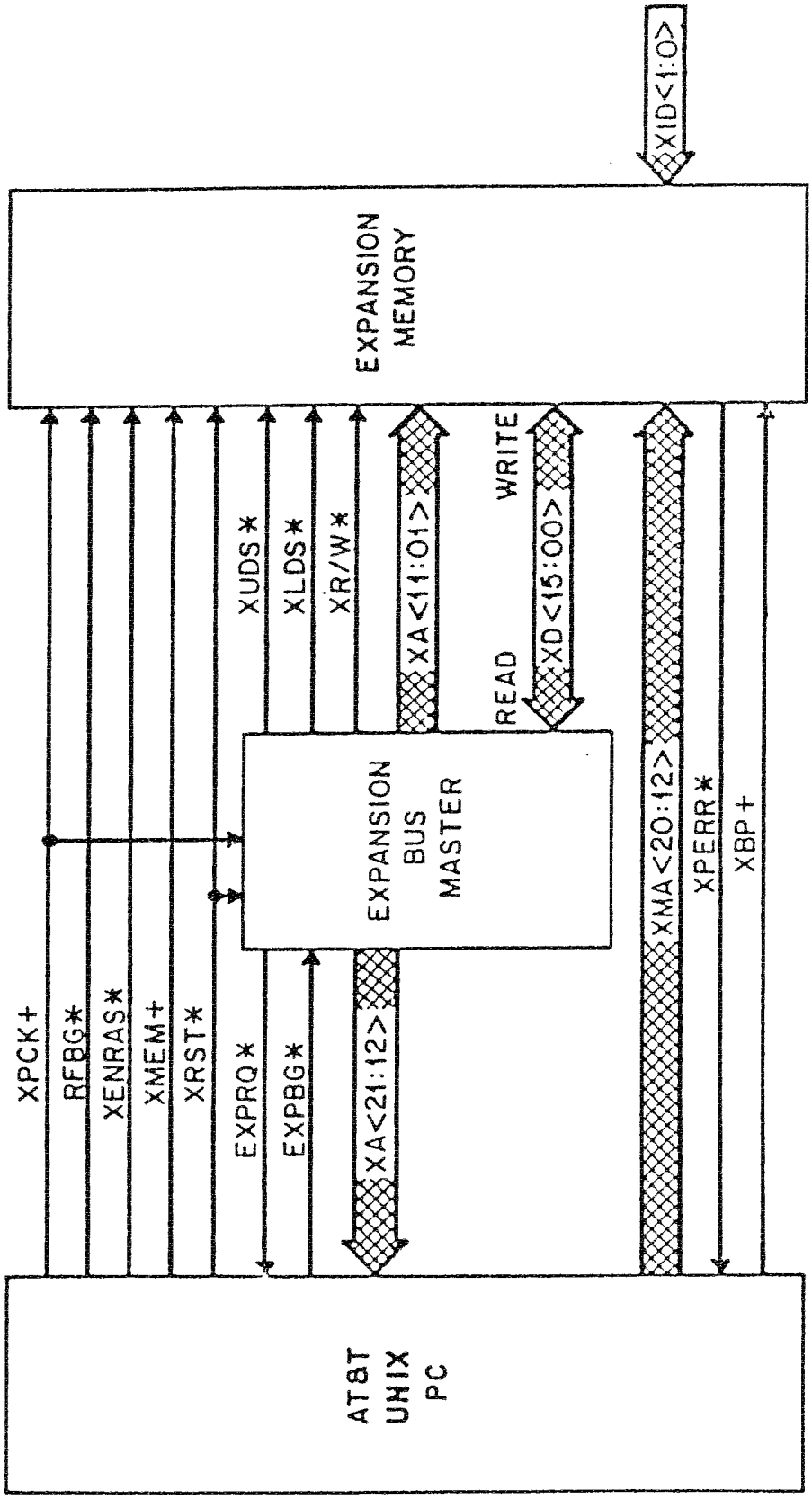


NOTE: (1) SIGNALS ACTIVE DURING REFRESH BUS CYCLES

SIGNAL FLOW DIAGRAM FOR:

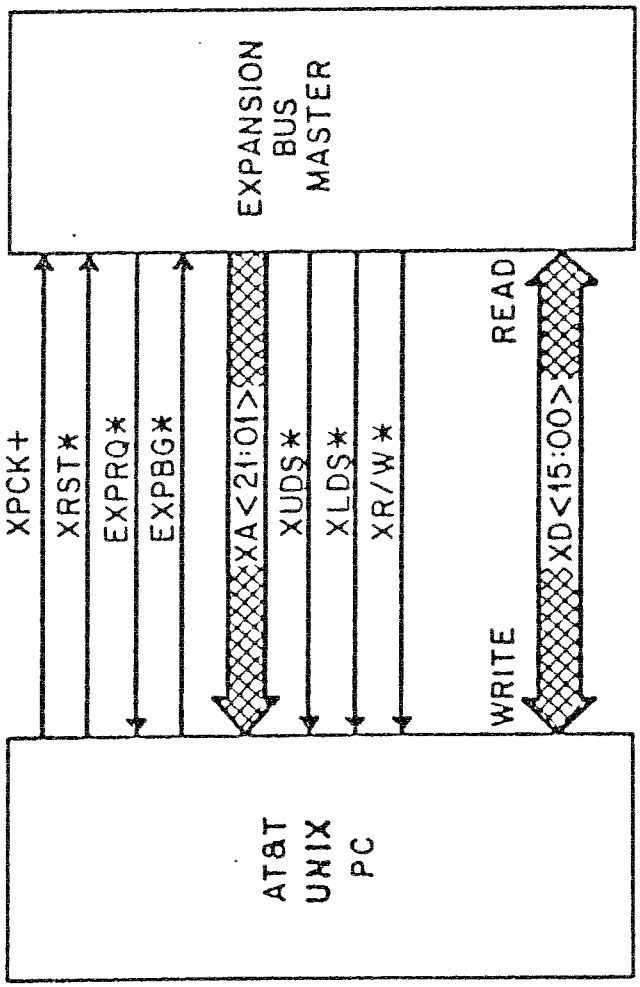
- AT&T UNIX PC PROCESSOR ⟶ EXPANSION MEMORY
- AT&T UNIX PC DISK DMA ⟶ EXPANSION MEMORY
- AT&T UNIX PC REFRESH ⟶ EXPANSION MEMORY

FIGU / 4



SIGNAL FLOW DIAGRAM FOR BUS MASTER TO EXPANSION MEMORY

FIGURE 5



SIGNAL FLOW DIAGRAM FOR BUS MASTER TO AT&T UNIX PC ON BOARD MEMORY

FIGURE 6

TABLE 13. EXPANSION SLOT IDENTIFICATION

SLOT NUMBER	LOCATION	256K-BYTE I/O PHYSICAL ADDRESS SPACE
1	AT&T UNIX PC	0XC00000 - 0XC3FFFF
2	AT&T UNIX PC	0XC40000 - 0XC7FFFF
3	AT&T UNIX PC	0XC80000 - 0XCBFFFF
3	EXP. BOX	SEE NOTE
4	EXP. BOX	0XCC0000 - 0XCFFFFF
5	EXP. BOX	0XD00000 - 0XD3FFFF
6	EXP. BOX	0XD40000 - 0XD7FFFF
7	EXP. BOX	0XD80000 - 0XDBFFFF
8	EXP. BOX	0XDC0000 - 0XDFFFFF

Note: The address space assigned to expansion box slot 3 is the same as the address space assigned to the AT&T UNIX PC expansion slot used for the bus repeater card.

5.2 I/O Bus Cycle Timing

Bus timing for 1000 ns I/O bus cycles is shown in Figure 3 and the corresponding timing specifications are given in separate columns in Table 14 for I/O cards located in the AT&T UNIX PC main unit and in the expansion box. I/O cards are expected to provide an access time (from the assertion of XI/OEN* to valid data from the I/O card) of 690 ns.

It should be noted that it is possible for signal XI/OEN* to be asserted prior to when the address bus XA<21:01> becomes valid. If it is important to the I/O design for the address bus to be stable prior to when XI/OEN* is asserted it is recommended that signal XI/OEN* be sampled on the rising edge of the XPCK+ clock. The S4BUS and I/O timing specifications are designed to ensure that signal XI/OEN* will be asserted and the XA<21:01> addresses will be valid prior to the next rising edge of the XPCK+ clock signal even if the I/O card is located in the expansion box.

6. EXPANSION MEMORY CARD SPECIFICATIONS

Expansion memory bus cycles are distinguished from all other bus cycles by the assertion of signal XENRAS* and the subsequent assertion of signal XMEM+ (see Table 12).

Expansion memory cards must be located in the AT&T UNIX PC main unit and may be accessed by either the AT&T UNIX PC processor or its Disk DMA controller (see Figure 4) or by an expansion Bus Master (see Figure 5). Bus Masters may also access AT&T UNIX PC on-board memory (see Figure 6) in which case the bus cycle is exactly the same except that signal XMEM+ will not be asserted.

TABLE 14. TIMING SPECIFICATIONS FOR I/O BUS CYCLES

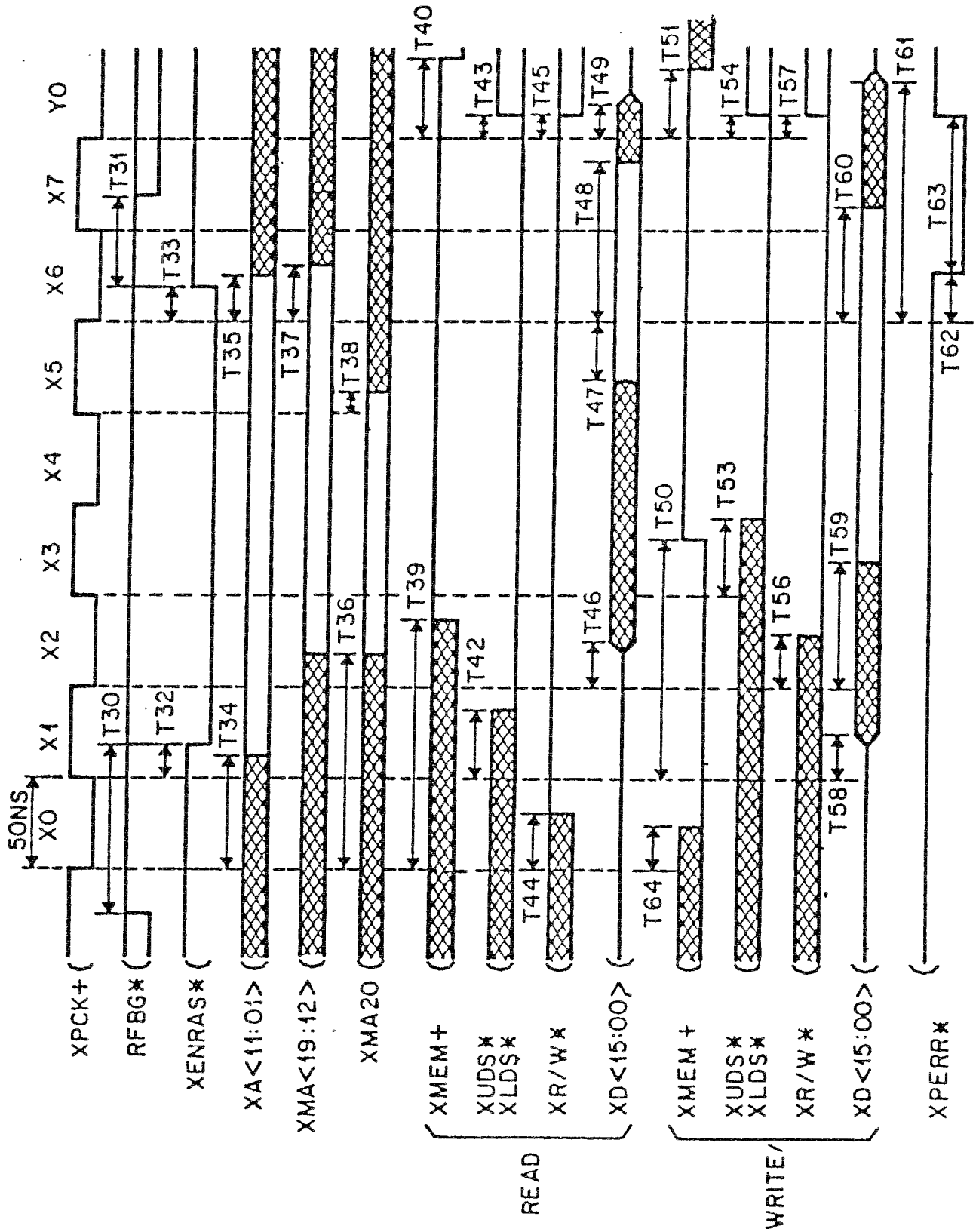
		AT&T UNIX PC		EXP. BOX	
		MIN	MAX	MIN	MAX
T1	CLOCK HIGH (X1) TO XI/OEN* LOW	5	55	5	80
T2	CLOCK HIGH (X19) TO XI/OEN* HIGH	5	55	5	80
T3	CLOCK LOW (X0) TO XA<21:01> VALID	-	40	-	90
T4	CLOCK HIGH (X19) TO XA<21:01> INVALID	5	-	5	-
T5	CLOCK LOW (X0) TO X<U:L>DS* VALID	-	40	-	90
T6	CLOCK LOW (X18) TO X<U:L>DS* INVALID	5	80	5	120
	READ BUS CYCLES				
T7	CLOCK LOW (X0) TO XR/W* HIGH	-	40	-	90
T8	CLOCK LOW (Y0) TO XR/W* MAY CHANGE	5	-	5	-
T9	CLOCK HIGH (X3) TO XD<15:00> LOW Z	0	-	0	-
T10	SET UP TIME: XD<15:00> MUST BE VALID PRIOR TO CLOCK LOW (X18)	25	-	70	
T11	HOLD TIME: CLOCK LOW (X18) TO XD<15:00> MUST REMAIN VALID	50	-	50	-
T12	XI/OEN* HIGH TO XD<15:00> HIGH Z	-	40	-	40
	WRITE BUS CYCLES				
T13	CLOCK LOW (X0) TO XR/W* LOW	-	40	-	90
T14	CLOCK HIGH (X19) TO XR/W* MAY CHANGE	5	-	5	-
T15	CLOCK HIGH (X1) TO XD<15:00> LOW Z	5	-	5	-
T16	XI/OEN* LOW TO XD<15:00> VALID	-	60	-	60
T17	CLOCK HIGH (X19) TO XD<15:00> INVALID	5	-	5	-
T18	XI/OEN* HIGH TO XD<15:00> HIGH Z	-	25	-	25

NOTE: ALL TIME INTERVALS ARE IN NANOSECONDS.

6.1 Expansion Memory Card Selection and Addressing

The address ranges over which expansion memory cards operate must be on half-megabyte boundaries and must lie within the 0X200000 to 0X3FFFFF address range allocated to expansion memory.

To facilitate the use of two or three half-megabyte or one-megabyte memory cards in the same AT&T UNIX PC, some form of variable address range card selection must be used. Automatic address range selection may be achieved by using Slot Identification bits XID<2:0> as specified in Table 15. Half-megabyte memories should be selected when Mapped Address bits XMA20 and XMA19 equal Slot ID bits XID1 and XID0 respectively. Similarly, one-megabyte memories should be selected when Mapped Address bit XMA20 equals Slot ID bit XID1. Note that Table 15 specifies the same address range for slots 1 and 2 and thus only one of these slots may be occupied by a one-megabyte memory card.



MEMORY BUS CYCLE TIMING DIAGRAM
(SEE TABLE 16)

Because of address space limitations, only one-1.5 megabyte memory card may be used in a AT&T UNIX PC and thus slot dependent card selection is not necessary. Of the two address ranges possible (namely, 0X200000 - 0X37FFFF and 0X280000 - 0X3FFFFF) the higher range allows a 1.5-megabyte memory card to be used along with a half-megabyte memory card plugged into slot 1.

TABLE 15. EXPANSION MEMORY PHYSICAL ADDRESS SPACE

SLOT NUMBER	XID<2:0> 2 1 0	0.5M-BYTE PHYSICAL ADDRESS SPACE	1M-BYTE PHYSICAL ADDRESS SPACE
1	0 0 0	0X200000 - 0X27FFFF	0X200000 - 0X2FFFFF
2	0 0 1	0X280000 - 0X2FFFFF	0X200000 - 0X2FFFFF
3	0 1 0	0X300000 - 0X37FFFF	0X300000 - 0X3FFFFF

Mapped Address bits XMA<20:12> for two-megabyte memory cards, XMA<19:12> for one-megabyte memory cards, and XMA<18:12> for half-megabyte memory cards address 4 K-byte physical pages. Words and bytes within physical pages are addressed by the Lower Unmapped Address Bus XA<11:01> together with the two data strobes XLDS* and XUDS*. The Upper Unmapped Address bus XA<21:12>, although valid, is not intended to be used by expansion memory.

6.2 Expansion Memory Access Bus Cycle Timing

Bus timing for access to expansion memory shown in Figure 7 and the corresponding timing specifications are shown in Table 16.

To obtain the maximum access time within a expansion memory bus cycle, an expansion memory circuit should begin an access (namely, assert its RAS signal) on the assertion of signal XENRAS* rather than waiting for signal XMEM+ to become valid. The CAS cycle should follow the assertion of XMEM+ and XMA<20:12>. It should be noted that it is possible for signal XENRAS* to be asserted before the Unmapped Address Bus becomes valid. Also note that signal XMEM+ will have an arbitrary value during time intervals T39 (Read) and thus must not be used as a strobe. In a read cycle, CAS should be strobed by some delay after XENRAS* to achieve maximum access time. In a write cycle CAS should be strobed by XMEM+ to achieve sufficient data set up time. Expansion memory cards are expected to provide a maximum access time to valid data from the assertion of XENRAS* of 193 ns and from the assertion of XMEM+ of 145 ns.

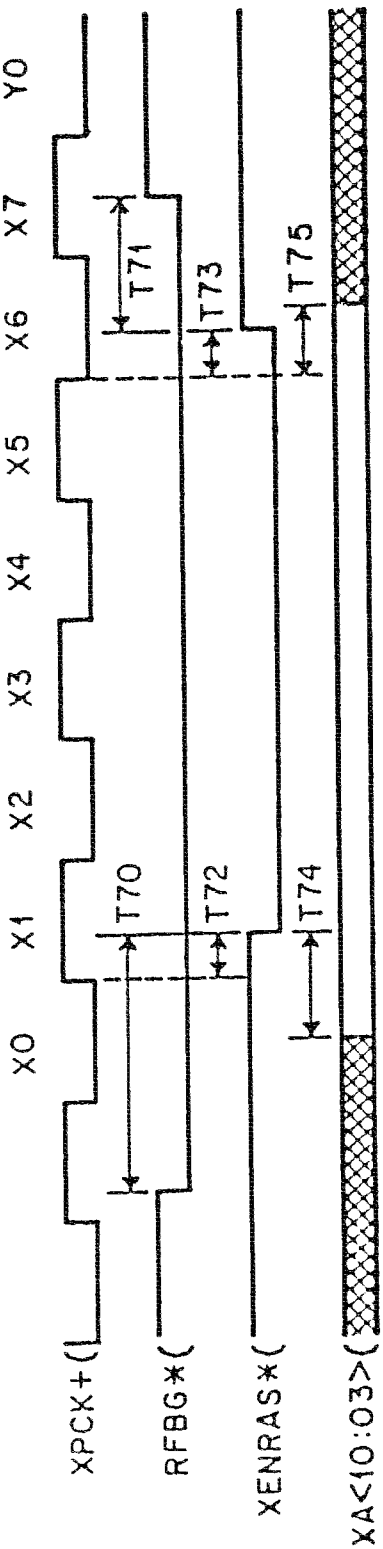
6.3 Refresh Bus Cycles

Figure 8 shows the Timing Diagram for the AT&T UNIX PC refresh controller to expansion memory type bus cycle and the corresponding Timing Specifications are given in Table 17. This type of bus cycle is distinguishable from all other bus cycles by the assertions of bus grant signal RFBG* and memory start control signal XENRAS* (see Table 12). The eight refresh address bits used by the AT&T UNIX PC on-board memory refresh controller appear on S4BUS address leads XA<10:03>. Refresh bus cycles occur once each 14.6 microseconds and may be used to refresh expansion memory.

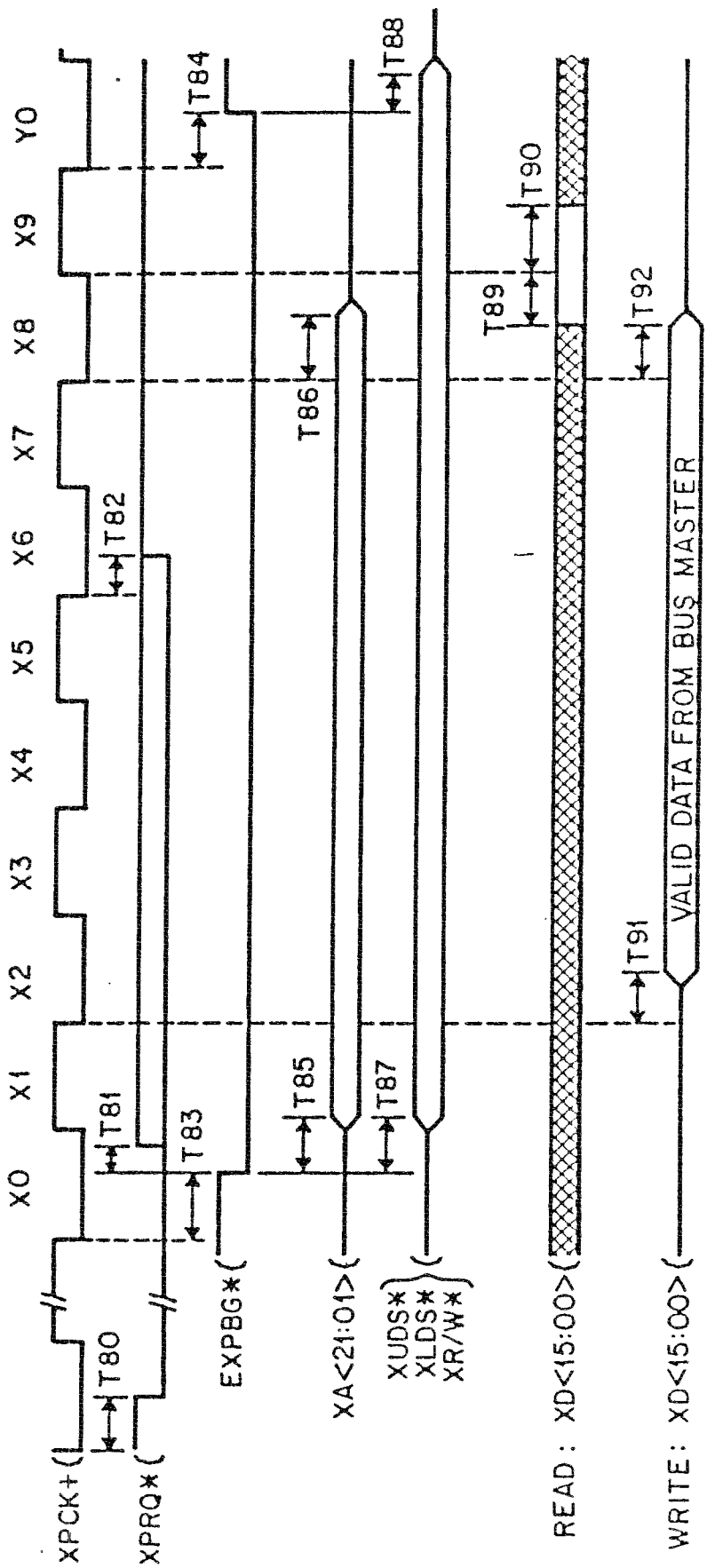
TABLE 16. TIMING SPECIFICATIONS FOR MEMORY BUS CYCLES

		MIN	MAX
T30	RFBG* HIGH TO XENRAS* LOW	40	-
T31	XENRAS* HIGH TO REBG* MAY CHANGE	50	-
T32	CLOCK HIGH (X1) TO XENRAS* LOW	-	32
T33	CLOCK LOW (X6) TO XENRAS* HIGH	-	25
T34	CLOCK LOW (X0) TO XA<11:01> VALID	-	70
T35	CLOCK LOW (X6) TO XA<11:01> INVALID	5	-
T36	CLOCK LOW (X0) TO XMA<20:12> VALID	-	125
T37	CLOCK LOW (X6) TO XMA<19:12> INVALID	15	-
T38	CLOCK HIGH (X5) TO XMA20 INVALID	5	-
	READ MEMORY BUS CYCLES		
T39	CLOCK LOW (X0) TO XMEM+ VALID AND HIGH	-	130
T40	CLOCK LOW (Y0) TO XMEM+ LOW	-	120
T42	CLOCK HIGH (X1) TO X<U:L>DS* VALID AND LOW	-	70
T43	CLOCK LOW (Y0) TO X<U:L>DS* MAY CHANGE	5	-
T44	CLOCK LOW (X0) TO XR/W* VALID AND HIGH	-	70
T45	CLOCK LOW (Y0) TO XR/W* MAY CHANGE	5	-
T46	CLOCK LOW (X2) TO XD<15:00> LOW Z	25	-
T47	SET UP TIME: XD<15:00> MUST BE VALID TO CLOCK LOW (X6)	25	-
T48	HOLD TIME: CLOCK LOW (X6) TO XD<15:00> MUST REMAIN VALID	75	-
T49	CLOCK LOW (Y0) TO XD<15:00> LOW Z	-	20
	WRITE MEMORY BUS CYCLES		
T64	CLOCK LOW (X0) TO XMEM+ VALID AND LOW	-	50
T50	CLOCK HIGH (X1) TO XMEM+ VALID AND HIGH	150	200
T51	CLOCK LOW (Y0) TO XMEM+ INVALID	5	-
T53	CLOCK HIGH (X3) TO X<U:L>DS* VALID AND LOW	-	70
T54	CLOCK LOW (Y0) TO X<U:L>DS* MAY CHANGE	5	-
T56	CLOCK LOW (X2) TO XR/W* VALID AND LOW	-	75
T57	CLOCK LOW (Y0) TO XR/W* MAY CHANGE	5	-
T58	CLOCK HIGH (X1) TO XD<15:00> LOW Z	10	-
T59	CLOCK LOW (X2) TO XD<15:00> VALID	-	70
T60	CLOCK LOW (X6) TO XD<15:00> INVALID	5	-
T61	CLOCK LOW (X6) TO XD<15:00> HIGH Z	-	190
T62	CLOCK LOW (X6) TO XPERR*	-	100
T63	XPERR* PULSE WIDTH	50	250

NOTE: ALL TIME INTERVALS ARE IN NANOSECONDS.



REFRESH BUS CYCLE TIMING DIAGRAM
(SEE TABLE 17)
FIGURE 8



EXPANSION BUS MASTER TIMING DIAGRAM
(SEE TABLE 18)

FIGURE 9

TABLE 17. TIMING SPECIFICATIONS FOR REFRESH BUS CYCLE

		MIN	MAX
T70	RFBG* LOW TO XENRAS* LOW	100	-
T71	XENRAS* HIGH TO RFBG* HIGH	50	-
T72	CLOCK HIGH (X1) TO XENRAS* LOW	-	32
T73	CLOCK LOW (X6) TO XENRAS* HIGH	-	25
T74	XA<10:03> VALID TO XENRAS* LOW	34	-
T75	CLOCK LOW (X6) TO XA<10:03> INVALID	15	-

NOTE: ALL TIME INTERVALS ARE IN NANOSECONDS.

7. EXPANSION BUS MASTER SPECIFICATIONS

7.1 Expansion Bus Master Bus Cycle Timing

Expansion Bus Master bus cycles are distinguished from all other types by the assertion of bus grant signal EXPBG*. If the bus master is accessing expansion memory, signals XENRAS* and XMEM+ will be asserted for the bus master by the AT&T UNIX PC and if the access is to AT&T UNIX PC on-board memory, only signal XENRAS* will be asserted (See Table 12). Figure 9 is the timing diagram for expansion bus master bus arbitration and for memory access (both expansion and AT&T UNIX PC on-board memory) and Table 18 contains the corresponding Timing Specifications.

7.2 Bus Master Address Space

Bus Masters may be plugged into any expansion slot and are allowed access to the two megabyte AT&T UNIX PC on-board memory address. space (0X000000 - 0X1FFFFF) and to the two megabyte expansion memory address space (0X200000 - 0X3FFFFF). Bus masters, however, are not allowed I/O a access.

7.3 Bus Arbitration Protocol

Bus mastership requests are arbitrated for and granted at the end of every bus cycle according to a slot dependent fixed priority scheme and bus masters are allowed to retain bus mastership until preempted by a bus master of higher priority. During master mode bus cycles, the AT&T UNIX PC processor is idled by wait states, and interrupts are ignored.

A potential bus master may request use of the S4BUS, at any time, by asserting bus request signal EXPRQ* synchronized to the falling edge of bus clock signal XPCK+ and holding it asserted until acknowledged by the assertion of bus grant signal EXPBG* as shown in Figure 9.

There are six bus priority levels defined for the AT&T UNIX PC system including three levels for AT&T UNIX PC on-board requests plus one spare and three for expansion bus masters as shown in Table 19.

TABLE 18. TIMING SPECIFICATIONS FOR BUS MASTER BUS CYCLES

	BUS ARBITRATION SIGNALS	MIN	MAX
T80	CLOCK LOW (ANY TIME) EXPRQ* LOW	-	20
T81	EXPBG* LOW TO EXPRQ* MAY GO HIGH	0	-
T82	CLOCK LOW TO EXPRQ* MUST GO HIGH	-	30
T83	CLOCK LOW (X0) TO EXPBG* LOW	-	45
T84	CLOCK LOW (Y0) TO EXPBG* HIGH	-	45
	ADDRESS AND READ/WRITE SIGNALS		
T85	EXPBG* LOW TO XA<21:01> MUST BE LOW Z AND VALID	-	30
T86	CLOCK LOW (X8) TO XA<21:01> MUST HIGH Z	-	75
T87	EXPBG* LOW TO XUDS*, XLDS*, & XR/W* | MUST BE LOW Z AND VALID	-	30
T88	EXPBG* HIGH TO XUDS*, XLDS*, & XR/W* MUST HIGH Z	-	30
	DATA BUS DURING READ BUS CYCLES		
T89	READ XD<15:00> VALID TO CLOCK HIGH (X9)	15	-
T90	READ XD<15:00> VALID AFTER CLOCK HIGH (X9)	15	-
	DATA BUS DURING WRITE BUS CYCLES		
T91	CLOCK LOW (X2) TO WRITE XD<15:00> MUST BE VALID	0	35
T92	CLOCK LOW (X8) TO WRITE XD<15:00> MUST REMAIN VALID	0	75

NOTE: ALL TIME INTERVALS ARE IN NANOSECONDS.

TABLE 19. BUS MASTER PRIORITY LEVELS

SIGNAL	DESCRIPTION
DKRQ*	On-board Disk DMA, highest priority
RFRQ*	On-board Refresh Controller
EXP2RQ*	Expansion bus request 2 highest priority
EXP1RQ*	Expansion bus request 1
EXP0RQ*	Expansion bus request 0 lowest priority
CPU	AT&T UNIX PC processor, lowest priority

AT&T UNIX PC expansion bus request signal EXP2RQ* is connected to the EXPRQ* connector pin of expansion slot 3 making slot 3 the highest priority bus expansion slot. Likewise, bus request signals EXP1RQ* and EXP0RQ* are respectively connected to the slots 2 and 1 EXPRQ* connector pins. The AT&T UNIX PC also defines three bus grant signals EXP<2:0>BG* which correspond to the three bus request signals and they are also individually connected to EXPBG* pins on the three expansion connectors. Thus the bus priority for an expansion bus master is determined by its slot location.

If an expansion box is used, the expansion box bus repeater card may be plugged into any AT&T UNIX PC expansion slot and it will pass along the pre-defined slot priority bus request/grant signals to the expansion box. Common circuitry in the expansion box will prioritize each of the six expansion slots in a way similar to that done in the AT&T UNIX PC. Thus bus master cards plugged into the expansion box also have their bus priorities set by their slot location.

7.4 Expansion Bus Master Transfer Procedure

The actual Bus Master transfer procedure is as follows (See Figure 9):

1. The bus master asserts EXPRQ* at some falling edge of XPCK+ to request bus mastership.

2. Signal EXPBG* will be asserted at some falling edge of XPCK+ after the assertion of EXPRQ* depending on bus traffic and the priority of the expansion slot. EXPBG* will remain asserted for exactly 5 XPCK+ clock periods.

3. Signal EXPRQ* must be de-asserted shortly after the assertion of EXPBG* if bus mastership for exactly one bus cycle is desired. Note that if EXPRQ* is asserted continuously, EXPBG* may be continuously asserted to give mastership of the bus for more than one bus cycle. In this case, cycle-to-cycle synchronization must be done by the bus master.

4. Following the assertion of EXPBG*, the bus master must drive signals given in Table 20 according to the timing diagrams in Figure 9.

7.5 Bus Grant Latency

Bus request to bus grant latency depends upon the following:

1. The type of bus cycle in progress when the request is made.

2. Where in the bus cycle the request is made.

3. The request level relative to other pending bus request levels.

The minimum bus grant latency is 100 ns and will occur if a bus request is made at the end of a bus cycle for which there are no other pending bus requests.

The maximum bus latency could approach infinity for a low priority bus master and no attempt will be made in this specification to quantify such a delay. The maximum bus latency for the highest priority expansion bus master can be determined, however. This will occur if the request is made at the beginning of a processor access to video memory and if during this processor bus cycle both a disk bus request and a refresh bus request is made. The resulting maximum bus latency is 2.4 microseconds.

7.6 Maximum Bus Request Rate

During Disk DMA activity, disk bus requests occur once every 3.2 microseconds and each Disk DMA access requires a bus time of 500 nanoseconds or 15.6% of the available bus time. Refresh bus cycles occur once every 14.6 microseconds and each requires 500 nanoseconds or 3.4% of the available bus time. The remaining bus time (81%) is available for use by the AT&T UNIX PC processor and all other expansion bus masters. To ensure that the processor has adequate bus time and to ensure that the disk DMA and the refresh controller may obtain the bus on demand, the average bus request rate for all expansion bus masters should not exceed a rate of one request every 0.8 microseconds. Assuming 500 nanoseconds per bus activity for bus masters and assuming one request every 0.8 microseconds, the bus availability for the processor will be 18.5% during peak bus activity. It is expected, although not specified, that the long term average bus occupancy by the disk DMA and all other bus masters will be much lower than 81.5%.

7.7 Bus Master Bus Addressing and Control Signals

Bus requesters must be prepared to drive the bus signals given in Table 20 (see Signal Flow diagram Figures 5 and 6) upon receiving bus mastership.

TABLE 20. SIGNALS TO BE DRIVEN BY BUS MASTERS

DESCRIPTION	SIGNAL
Upper Unmapped Address Bus	XA<21:12>
Lower Unmapped Address Bus	XA<11:01>
Upper Data Strobe	XUDS*
Lower Data Strobe	XLDS*
Read/Write	XR/W*
Data Bus (write mode)	XD<15:00>

The Upper Unmapped Address Bus is used as an input to the AT&T UNIX PC memory management unit which, in turn, generates the Mapped Address Bus. It should be noted that a certain amount of cooperation must exist between the AT&T UNIX PC operating system and the bus requester so that the bus requester will use an assigned logical address space for conversion to the proper physical address space by the memory management unit.

Address bit XMA21 selects either AT&T UNIX PC on-board memory (XMA21 = 0) or expansion memory (XMA21 = 1). The Lower Unmapped Address Bus XA<11:01> together with the Upper and Lower Data Strobes (XUDS* and XLWD*) are used to select words and bytes within pages selected by the Mapped Address Bus. The AT&T UNIX PC bus interface unit will supply the Mapped Address Bus XMA<20:12>, the bus cycle initiation signal XENRAS*, and if appropriate the expansion memory select signal XMEM+. Expansion I/O select signal XI/OEN* will not be asserted during the entire bus master bus cycle.

8. INTERRUPT PROTOCOL

Internally, the AT&T UNIX PC supports seven interrupt levels. Two of these (INT05* and INT01*) are reserved for general purpose expansion bus interrupts. The highest level AT&T UNIX PC interrupt is nonmaskable and is shared by the AT&T UNIX PC and the S4BUS parity error interrupt signal XPERR*. The AT&T UNIX PC has two interrupt levels higher in priority than INT05* and three levels between INT05* and INT01*.

Expansion cards may interrupt the AT&T UNIX PC processor using either of the general purpose interrupt signals and should assert their interrupt signals using open collector (or equivalent) drivers. There is no special purpose interrupt acknowledge bus cycle supported by the S4BUS; however, the AT&T UNIX PC processor will determine the identification of the interrupter or interrupters by a I/O polling sequence. Interrupters should hold their general purpose interrupt signals asserted until polled and should be prepared to respond to the poll with an interrupt status word. The address of the interrupt status word is not specified although of course, it must be located within the slot's assigned I/O address space.

Non maskable interrupts may be caused by asserting the parity error interrupt signal XPERR*. .This interrupt is intended primarily for expansion memory cards and will not be supported in the expansion box.

9. EXPANSION BOARD IDENTIFICATION

Each I/O and Bus Master expansion board shall contain four read only registers located in the last four odd byte addresses of an expansion slot's I/O address range as determined by the slot ID bits. See Tables 11, 13, and 21. These registers shall contain respectively (from lower address to high address) Byte-1 of the boards unique two byte board identification number, Byte-2 of this same number, the 2's-complement of Byte-1 and the 2's-complement of Byte-2. The actual addresses for the four board identification bytes is equal to a slot's base address (first address column in Table 13) plus the offset address shown in Table 21.

Unique two byte board identification numbers will be assigned by AT&T-IS and may be obtained by contacting: AT&T UNIX PC Product Management, 1776 On-The-Green, Morristown, New Jersey, 07960.

TABLE 21. EXPANSION BOARD IDENTIFICATION REGISTER ASSIGNMENTS

OFFSET ADDRESS	REGISTER CONTENTS
0X03FFF8	NOT USED
0X03FFF9	BOARD ID BYTE-1
0X03FFFA	NOT USED
0X03FFFB	BOARD ID BYTE-2
0X03FFFC	NOT USED
0X03FFFD	TWO'S COMPLEMENT OF BYTE-1
0X03FFFE	NOT USED
0X03FFFF	TWO'S COMPLEMENT OF BYTE-2

10. EXPANSION BOARD RESET

Each I/O and bus master expansion card shall contain circuitry that will cause the expansion card to enter and maintain a reset quiescent state (all bus drivers turned off) in response to either the assertion of bus reset signal XRST* or a write to any of the board's identification register addresses (software reset). The expansion board shall maintain the quiescent state until activated under software control. Board activation is not specified in this specification.

11. SOFTWARE MODEL FOR HARDWARE EXPANSION

To be supplied.