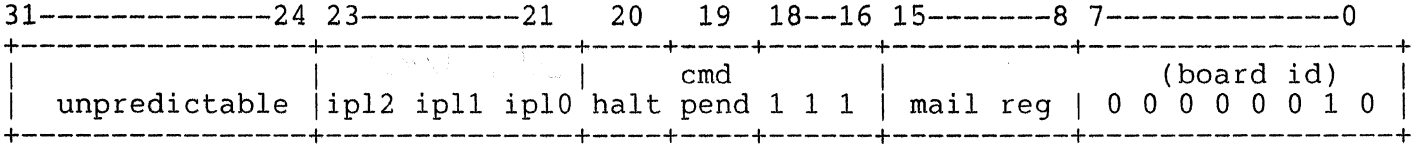
This describes the appearance of the processor module
as seen by other modules on the CSS bus.

Read Status Register:

An automatic register may be read (byte or long) at physical address

<slot>offset:0xfffffffc.

The register is "automatic" because it responds without assistance
from the processor.



ipl2,1,0 reflect the (low true) value at the processor input

halt=0 indicates the processor has a double bus error

cmd-pend=1 indicates the command buffer is full

mail reg is loaded by the processor at BUS_MAIL_BYTE.

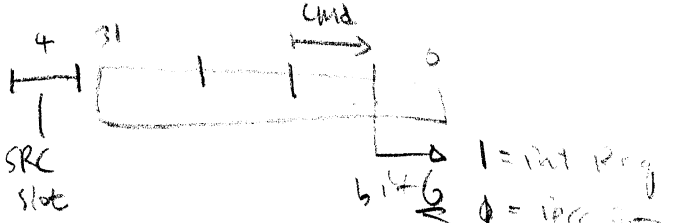
Command register:
Commands to read or write are accepted at

<slot>offset:0x??????00
(where ? represents 4 don't care bits),

as required by the CSS Bus Specification.
The register captures four bytes of address and four bytes of data.
The data captured from a read command is not predictable.

Receiving a command,
except the automatic read,
causes a Non-Maskable Interrupt to be asserted
at the processor, and the cmd-pend bit to be set.
The processor's firmware is expected to respond to the command.
Further commands cannot be received until the processor
increments its ready-count on the arbiter.

HARDWARE LIMITATIONS: Since the equipment for sending DATA RESPONSEs
is not usable while the processor is
executing from main memory or testing cache or mmu,
read commands are not recommended as part of the normal protocol.
Also, the type value is not captured, so the module has no easy way to tell
an arriving read from a write command.



The cmd-pend bit goes to 0 when the processor resets it by writing
at CLR_NMI.
Separately, a write to INC_READY is required to allow more commands.

Interrupt Requests:
The interrupt request register contains seven individual request bits.
An aligned long write command to

<slot>0xfffffffc

can change the state of any one request bit.
The command values are:

```
0x?0??????: clear level 0        This command is a NOP
0x?1??????: clear level 1
0x?2??????: clear level 2
0x?3??????: clear level 3
0x?4??????: clear level 4
0x?5??????: clear level 5
0x?6??????: clear level 6
0x?7??????: clear level 7
0x?8??????: set level 0          This command is a NOP
0x?9??????: set level 1
0x?a??????: set level 2
0x?b??????: set level 3
0x?c??????: set level 4
0x?d??????: set level 5
0x?e??????: set level 6
0x?f??????: set level 7
```

Question marks represent ignored data.

The seven request bits are priority-encoded into the three-bit IPL
value which appears at the cpu chip, the automatic register,
and an onboard register.

Interrupt acknowledge by the cpu chip is auto-vectored,
and has no effect on any request bits.

The interrupt request register is not directly readable anywhere.
If there is a command pending or an interrupt from the diagnostic console,
(that is, either NMI)
then IPL will read low no matter what requests are pending.

CONTROL WRITE
is a function defined by the A3000 bus spec.
The module responds to the four CONTROL WRITE values defined:

module enable	releases on-card RESET
module disable	asserts RESET
interface enable	lets the bus-driver work
interface disable	forces the module to shut up.