Maintenance Manual

ARCHIVE

MODELS 3020-9020-9045

ARCHIVE
CORPORATION

SIDEWINDER

¼" Streaming Cartridge Tape Drive
MAINTENANCE MANUAL

PART NUMBER 20109—001B

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CHAPTER 1

INTRODUCTION

1.1 SCOPE

This manual contains maintenance information for the SIDEWINDER Intelligent and Basic Streaming Cartridge Tape Drive and applies to Models 3020B, 3020I, 9020B, 9020I, 9045B, and 9045I units. Included are physical and functional descriptions, specifications, specifics of operation, preventive maintenance, field maintenance, and depot maintenance.

1.2 PHYSICAL DESCRIPTION

The Intelligent Cartridge Tape Drive is available in three models: the MODEL 9020I, the MODEL 3020I, and the MODEL 9045I. These models include an Intelligent Controller and the MODEL 9020B or the MODEL 3020B or the MODEL 9045B Basic Drive, respectively.

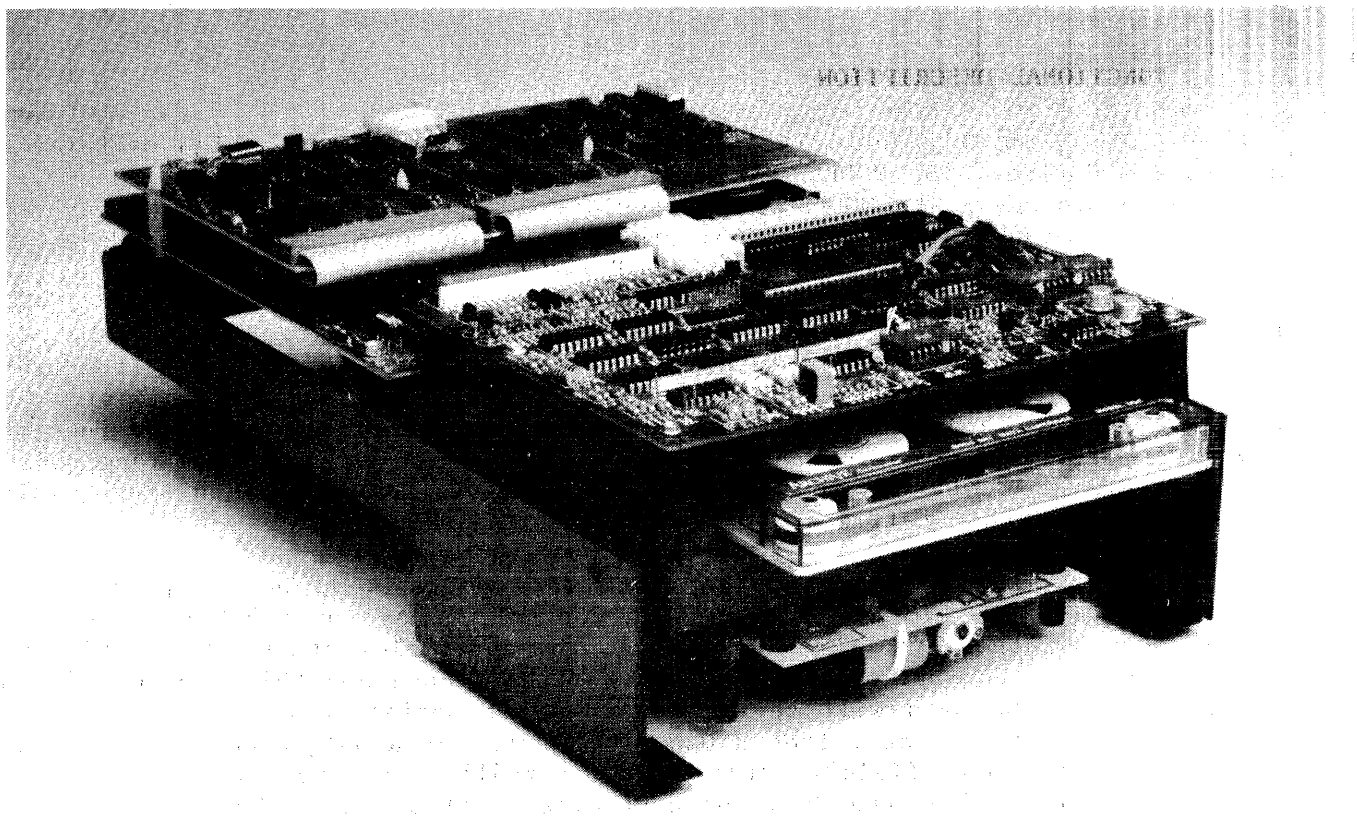


Figure 1-1. The ARCHIVE Intelligent Cartridge Tape Drive

1.2.1 Basic Drive

The MODEL 9020B, MODEL 3020B, and MODEL 9045B drive contains a basic main frame on which is mounted the magnetic recording head, capstan drive motor, tape hole sensors, "cartridge in place" and "safe" sensing switches. The drive electronics is packaged on two printed wiring boards (PWBs), one mounted above and one mounted below the installed tape cartridge. The drive may be equipped with an optional front panel. The drive employs as storage media a 450 foot long, 1/4 inch wide tape contained in a cartridge that is described mechanically by ANSI Standard X3.55-1977.

1.2.2 Controller

The controller contains independent read and write channels, three 512 byte buffer memories, a host interface, a drive interface and a micro-computer. The incorporation of the micro-computer into the controller makes tape formatting, tape error processing, tape positioning and tape motion controls invisible to the host system. Additionally, the micro-computer provides statistical error data to prevent progressive deterioration of the tape system due to bad tapes and marginal components.

1.3 FUNCTIONAL DESCRIPTION

The Archive Intelligent Cartridge Tape Drive is a low cost, high performance mass storage device. The MODEL 9020I provides 90 ips tape speed and 20 Megabytes of user data storage. The MODEL 3020I provides 30 ips tape speed and 20 Megabytes of user data storage. The MODEL 9045I provides 90 ips tape speed and 45 Megabytes of user data storage. The Intelligent Drive consists of two components, the Archive Streaming Cartridge Tape Controller and up to four Archive Streaming Basic Cartridge Tape Drives. The Basic Tape Drive recording density is 8000 bits per inch. The tape controller relieves the host CPU of the overhead functions associated with tape formatting, tape error processing, file mark processing and tape positioning. This high degree of intelligence minimizes the engineering hardware and software efforts required to interface Archive Cartridge Tape Drives to a host CPU. Archive Basic Cartridge Tape Drives equipped with the Archive Controller are called Intelligent Drives.

When the host system is ready to write data on tape, it begins transferring that data in 512 byte blocks. The Archive Controller has three 512 byte buffers. When the first of the three buffers is full, the controller starts tape motion and begins writing to the tape, accepting data for the second and third buffers during this operation. The data will be written in a bit serial format, one track at a time. The controller first writes a Gap of 13 bytes of a unique code (a code that cannot appear in a data field). This Gap is actually 104 bits long, written in a bit serial format. After the Gap, the controller writes a Sync Mark which is four bits long. Following the Sync Mark, the controller writes the user data stored in the first buffer to the tape. This 512 byte data field is referred to as a block of data and is 4096 bits long. When the entire data block is written, the

controller writes a block address. The block address is eight bits long. The first block is block number one and the address is incremented by one for each consecutive block of data. The block address resets to zero after 255. After the block address, the controller writes the CRC character. This character is two bytes or 16 bits long. The complete block is 528.5 bytes (4228 serial bits) and is written to track 0. When the second buffer is full, the controller begins the process over again. There are no "dead" spots between blocks. As long as the host system can keep data coming to the controller fast enough to keep the buffers full, tape motion will not stop. This method of writing a continuous stream of data is referred to as streaming tape mode.

The Archive Streaming Tape Drive uses a 4-to-5 run-length limited code. Every four bits of data are translated to a corresponding five bit code. There are 32 possible combinations of bits in each five bit block. Only 16 of these possible combinations are needed to represent four bit nibbles of data. Using only 16 combinations permits choosing those groups of five bits which do not have more than two consecutive zeroes. Also, no matter how the five bit groups are strung together, there will never be more than two consecutive zeroes in the data stream. Because there are never more than two consecutive zeroes in this 4-to-5 code, the NRZI recording method can be used reliably. The 4-to-5 code also permits choosing unique bit patterns for Gap, Sync, and File Mark that will never appear as encoded user data in data field.

1.4 SPECIFICATIONS

The performance, environmental, and physical specifications are listed in tables 1-1 through 1-4. The mean time between failures for intelligent models is greater than 3500 hours of actual use and the mean time to repair is less than 0.5 hour. There will be fewer than one soft read error in 100 million bits and fewer than one hard read error in 10 billion bits.

Table 1-1. SIDEWINDER Performance Specifications

Model	3020B	3020I	9020B 9045B	9020I	9045I
No. of Tracks	*	4	*	4	9
No. of Heads	2	2	2	2	2
Formatted Capacity	*	20 MB	*	20 MB	45 MB
Unformatted Capacity	*	21.6 MB	*	21.6 MB	48.6 MB
Dump Time	*	12 Min.	*	4 Min.	9 Min.
Recording Mode	*	NRZI	*	NRZI	NRZI
Recording Density	*	8K BPI	*	8K BPI	8K BPI
Flux Density	*	10K FCI	*	10K FCI	10K BPI
Track Capacity	*	5.2 MB	*	5.2 MB	5.2 MB
Tape Speed	30 IPS	30 IPS	90 IPS	90 IPS	90 IPS
Start/Stop Time	100 MS Max.	100 MS Max.	300 MS Max.	300 MS Max.	300 MS Max.

* Customer Selectable

Table 1-2. Environmental Specifications

Parameter	Operational	Non-Operational
Temperature	+5 to +45°C	-30 to +60°C
Relative Humidity (non-condensing)	20 to 80%	0 to 99%
Altitude	-200 to 15,000 Ft.	-200 to 50,000 Ft.
Shock	2.5 g max., 1/2 sine wave, 11 msec duration on any axis.	Cartridge and front panel installed: 25g max., 1/2 sine wave, 11 msec duration on any axis. Cartridge and front panel not installed: 50 g max., 1/2 sine wave, 11 msec duration on any axis.
Vibration	0.005 inch max peak-to-peak displacement 0 to 63 Hz, 1 g max acceleration 63 to 500 Hz.	0.1 inch max peak-to-peak displacement 0 to 17 Hz, 1.5 g max acceleration 17 to 500 Hz.

Table 1-3. Power Specifications

Parameter	Basic Drive	Intelligent Drive
Voltage	+24 ± 10% vdc +5 ± 5% vdc	+24 ± 10% vdc +5 ± 5% vdc
Peak-to-Peak Ripple	+24 vdc; 500 mv, max. +5 vdc; 100 mv, max.	+24 vdc; 500 mv, max. +5 vdc; 100 mv, max.
Voltage Rise Time	+24 vdc; 100 msec, max. +5 vdc; 50 msec, max.	+24 vdc; 100 msec, max. +5 vdc; 50 msec, max.
Power-On Sequence	+24 vdc before +5 vdc or else use RESET.	+24 vdc before +5 vdc or else use RESET.
Current +24 VDC	Standby; 0.1 amp Operating; 0.8 amp - max., 1.6 amps - surge, 2.5 amps	Standby; 0.2 amp Operating; 0.8 amp - max., 1.7 amps - surge, 2.5 amps

Table 1-3. Power Specifications (Continued)

Parameter	Basic Drive	Intelligent Drive
+5 VDC	Standby; 1.0 amps Operating; 1.0 amps	Standby; 3.5 amps Operating; 3.5 amps
Power Dissipation	30 Watts, typical 50 Watts, maximum	35 Watts, typical 60 Watts, maximum

Table 1-4. Physical Specifications

Characteristic	English System	Metric System
Intelligent Drive		
Depth	14 ± 0.01 inches	355.6 ± 0.25 mm
Width	8.55 ± 0.01 inches	217.2 ± 0.25 mm
Height	4.5 + 0, -0.2 inches	114.3 + 0, -5.1 mm
Weight	4 ± 0.2 pounds	1.81 ± 0.09 kg
Basic Drive		
Depth	6.0 ± 0.02 inches	152.4 ± 0.51 mm
Width	7.75 ± 0.02 inches	196.9 ± 0.51 mm
Height	4.5 + 0, -0.2 inches	114.3 + 0, -5.1 mm
Weight	2.1 ± 0.1 pounds	0.95 ± 0.05 kg

1.5 SUGGESTED MAINTENANCE TOOLS

The following tools are suggested for field maintenance personnel.

1. One tape cartridge known to be in good condition with good data recorded on it is to be used for reading.

2. One tape cartridge known to be in good condition is to be used as test tape for writing.

3. One digital multimeter.

4. One shop quality oscilloscope.

5. Standard shop tools.

CHAPTER 2

OPERATION

2.1 GENERAL INFORMATION

The SIDEWINDER PRODUCT MANUAL contains general operating information. It is not intended that this manual be used as a source for operating instructions. The information provided in this chapter is intended for maintenance use only.

2.2 HOST GENERATED SIGNALS

Table 2-1 lists the host generated signals, their input pin number, mnemonic, and description. All signals from the host are standard TTL logic levels, i.e., FALSE, logic 0 (high) is +2.0 to +5.25 vdc and TRUE, logic 1 (low) is 0 to +0.8 vdc. Odd numbered pins are signal returns.

Table 2-1. Input Signal Pin Assignments and Signal Description

Pin	Name	Description
12	HB7-	BUS BIT 7 - most significant bit, bi-directional data bus
14	HB6-	BUS BIT 6
16	HB5-	BUS BIT 5
18	HB4-	BUS BIT 4
20	HB3-	BUS BIT 3
22	HB2-	BUS BIT 2
24	HB1-	BUS BIT 1
26	HB0-	BUS BIT 0 - least significant bit, bi-directional data bus
28	ONL-	ONLINE - must be activated prior to tranferring a Read or Write command and may be deactivated to terminate a Read or Write operation.
30	REQ-	REQUEST - indicates that a command has been placed on the data bus in Command mode or that status has been taken from the data bus in Status Input mode. Can be asserted by host only when RDY- or EXC- is asserted by controller.
32	RST-	RESET - causes controller to perform same sequence as a POWER-ON sequence.
34	XFR-	TRANSFER - indicates that data has been placed on the data bus in Write mode or that data has been taken from the data bus in Read mode.

2.3 DRIVE GENERATED SIGNALS

Table 2-2 lists the drive generated signals, their output pin number, their mnemonic, and description. All output signals are standard TTL logic levels, i.e., FALSE, logic 0 (high) is +2.4 to +5.25 vdc and TRUE, logic 1 (low) is 0 to +0.55 vdc.

Table 2-2. Output Signal Pin Assignments and Signal Description

Pin	Name	Description
12	HB7-	BUS BIT 7 - most significant bit, bi-directional data bus
14	HB6-	BUS BIT 6
16	HB5-	BUS BIT 5
18	HB4-	BUS BIT 4
20	HB3-	BUS BIT 3
22	HB2-	BUS BIT 2
24	HB1-	BUS BIT 1
26	HB0-	BUS BIT 0 - least significant bit, bi-directional data bus
36	ACK-	ACKNOWLEDGE - indicates that data has been taken from the data bus in Write mode or that data has been placed on the data bus in Read mode.
38	RDY-	READY - indicates the following: 1. command has been taken from the data bus in Command Transfer mode. 2. data has been placed on the data bus in Status Input mode. 3. a BOT, Retension or Erase command is completed following issuance. 4. a buffer is ready to be filled by the host, or a WFM command can be issued in Write mode. 5. a WFM command is completed in Write File Mark mode. 6. a buffer is ready to be emptied by the host or a READ FILE MARK can be issued in Read mode. 7. otherwise, controller is ready to receive a new command.
40	EXC-	EXCEPTION - indicates that an exception condition exists in the controller and host must issue Status command and perform a Status Input to determine cause.

Table 2-2. Output Signal Pin Assignments and Signal Description (Continued)

Pin	Name	Description
42	DIR-	DIRECTION - controller generated signal which when false causes host data bus drivers to assert their data bus levels and controller data bus drivers to assume high impedance states, when true causes host data bus drivers to assume high impedance states and controller data bus drivers to assert their data bus levels.

2.4 TAPE FORMAT

Table 2-3 lists the operational characteristics resulting from the tape format as well as the technical description of the format. Figures 2-1 through 2-3 illustrate the details of tape formatting.

"Serpentine" refers to recording logically adjacent tracks in opposite directions, even numbered tracks in a forward direction, and odd tracks in a reverse direction. Tracks are recorded serially one at a time. This eliminates the need of rewinding the tape to read or write the next track of data and allows the tape to logically appear as one long track.

Table 2-3. Tape Format Description

Parameter	Description
Capacity, Streaming	
MODELS 9020I and 3020I	20 Mbytes
MODEL 9045I	45 Mbytes
Number of Recording Tracks	
MODELS 9020I and 3020I	4
MODEL 9045I	9
Average Streaming Write	
Transfer Rate MODEL 9020I	86.7 $\pm$ 0.87 Kbytes/sec
Transfer Rate MODEL 3020I	28.9 $\pm$ 0.29 Kbytes/sec
Transfer Rate MODEL 9045I	86.7 $\pm$ 0.87 Kbytes/sec
Burst Data Transfer Rate	200 Kbytes/sec max
Average Streaming Read	
Transfer Rate MODEL 9020I	86.7 $\pm$ 3.47 Kbytes/sec
Transfer Rate MODEL 3020I	28.9 $\pm$ 1.16 Kbytes/sec
Transfer Rate MODEL 9045I	86.7 $\pm$ 3.47 Kbytes/sec
Recording Form	
MODELS 9020I and 3020I	4 track "serpentine"
MODEL 9045I	9 track "serpentine"

Table 2-3. Tape Format Description (Continued)

Parameter	Description
Recording Code	4-to-5 run-length limited
Head Type	Read-after-write with separate full width erase bar

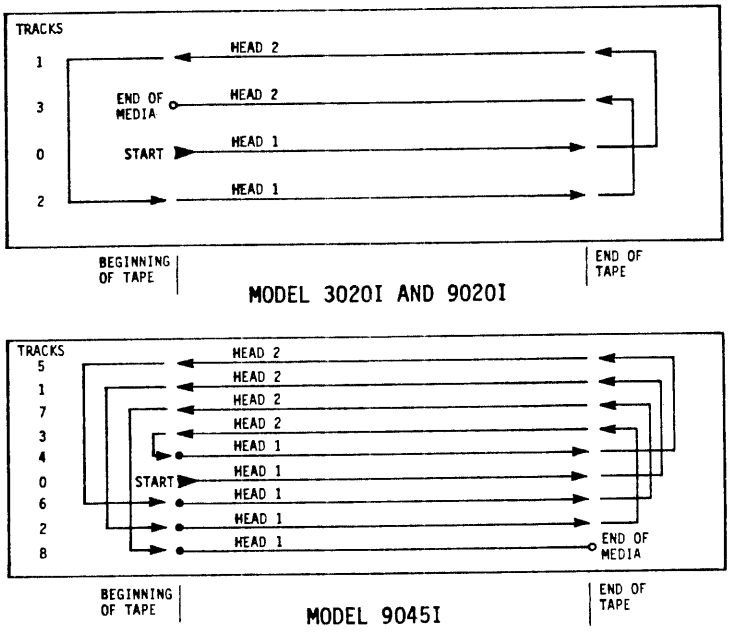


Figure 2-1. Tape Tracks, Serpentine

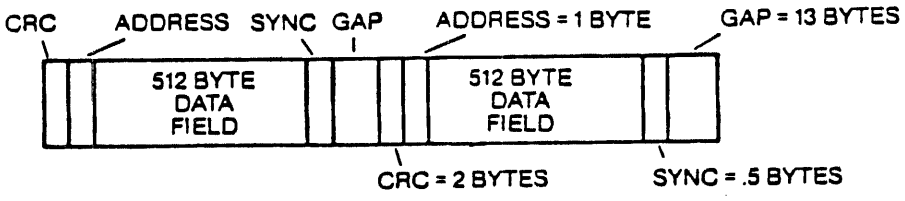


Figure 2-2. Tape Format

2.5 DATA BUS COMMANDS

Table 2-4 lists a statement of the result of each command transferred from the host on the data bus.

Table 2-4. Host Data Bus Commands

Command	Result
Select	Selects Basic Drive to be used.
Position	Causes tape to be moved to BOT, erased, or retensioned.
Write Data	Write host data onto tape.
Write File Mark	Write File Mark at the end of last data block.
Read Data	Read data from tape and transfer it to the host.
Read File Mark	Move the tape to the next File Mark without transferring data to the host.
Read Status	Transfer six bytes of status and statistics to the host.

2.6 POWER CONNECTOR

The power connector for both the Basic and Intelligent units are identical and are shown in figure 2-3. The mating connector is a 3M type 3415-0001 or equivalent.

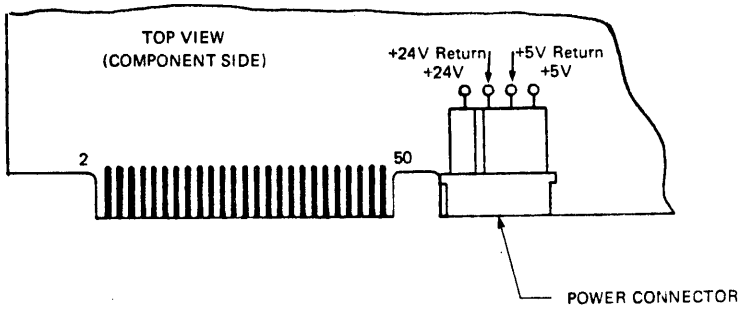


Figure 2-3. Power Connector Input Voltages

CHAPTER 3

PREVENTIVE MAINTENANCE

3.1 CLEANING

Clean the read/write/erase head assembly and the tape hole detector openings with a clean, lintless cotton swab dampened with IBM head cleaning solution or 95% isopropyl alcohol using the following schedule:

1. After an intial pass with a new tape cartridge or, if using all new tape cartridges, after every 2 hours of actual use.

2. After every 8 hours of normal use.

3.2 SOFT ERROR STATISTICS

Read and write error statistics are available to the host through the Read Status command. Typically, the Read Status command should be requested after completion of each cartridge used and the statistics reported at least on an exception basis. An increase in the soft write error rate normally indicates a deterioration of the recording media. If retensioning the cartridge does not reduce the soft errors dramatically, a known good tape should be used. If the soft error rate is high on a known good tape, the drive is ready for servicing. If the soft write error rate is low on a known good tape, the cartridge with the high soft write error rate should be replaced with a new cartridge.

CHAPTER 4

FIELD TROUBLESHOOTING

4.1 GENERAL INFORMATION

The Archive Intelligent Cartridge Tape Drive is a reliable device that should operate trouble-free most of the time. In fact, the most frequent causes of failure are the quality of the tape cartridges being used, failure to keep the read/write heads clean, and failure to remove oxide dust from inside the drive. Therefore, when trouble is reported, inspect the condition of the tapes being used and clean the interior of the drive using the procedures in Chapter 3. When the reported failure does not sound like a catastrophic failure, i.e., nothing works or tape has ran off the supply reel in the cartridge, try to read a tape that is known to be a good tape with known data. If the read operation is successful, then try to write some known data on a test cartridge that is known to be of good quality. When the read and write operations can be checked, enough information may be available to correct the trouble without additional checks.

The balance of this chapter consists of suggested checks to isolate the malfunction to the Basic Drive or the Intelligent Controller. If a major subassembly is replaced, perform the checks in Chapter 5. When severe misalignment is detected after repair, the procedures in Appendix III should be run.

It is essential that the procedures in Appendix III be performed only in a shop environment. The special tapes required to perform the procedures in Appendix III should not be used regularly on drives in the field. For the most part, mechanical troubles such as errors in tape movement and head recalibration are in the Basic Drive and, when the heads are clean and the tape is good, other troubles are in the Intelligent Controller. Table 4-1 lists some common symptoms with suggested probable causes. The main board and motor driver board are in the Basic Drive.

Table 4-1. Troubleshooting

Symptom	Check	Probable Cause
Drive will not respond.	+5 vdc and +24 vdc on Intelligent Controller board near J2.	1. No power from host. 2. Power cable to J2 disconnected. 3. Open line. 4. Short in the drive. If voltages are present at cable connector, disconnect internal cable to J2 on the main board. If this restores

Table 4-1. Troubleshooting (Continued)

Symptom	Checks	Probable Cause
		voltage to controller, then short is in Basic Drive.
Does not read or write.	+12 vdc	1. +12 vdc regulator on main board. 2. Read amplifiers on main board.
	Read pulses at J1-26 of main board.	1. If no pulses are present, problem is on main board. 2. If pulses are present, problem is on Intelligent Controller.
Head does not calibrate on power-up.	Check exposed pins at 5C on main board.	1. Missing shunt clip (two shunt clips are required). 2. Shorted pins at location 5C.
	Check signals on pins with shunt clips during power-up.	If a signal is missing, trouble is on the main board (location 5C).
	Check signals on pins 3 and 5 of 5Ba and 5Bb on main board.	1. If a signal is missing, trouble is on the main board. 2. If all signals present, trouble is in the stepper motor.
Stepper motor "chatters", does not calibrate.		Zero phase collar needs adjustment.
Tape does not move.	Disconnect existing motor and externally connect a good motor. Short CF0 pads on main board. Close the Cartridge In switch.	1. If substitute motor drives, replace existing motor. 2. If substitute motor does not work, check for pulses at 7C, pin 6. If pulses present, trouble is on motor

Table 4-1. Troubleshooting (Continued)

Symptom	Check	Probable Cause
		driver board. If no pulses, trouble is on main board.
Tape does not reverse.	Check for pulses at 7C, pin 3 on main board.	If no pulses, trouble is on main board. If pulses present, trouble is on motor driver board.
Capstan motor drives without tape cartridge in place.	Connect 3B, pin 4 to ground on main board.	Trouble is probably in motor driver board. If grounding 3B, pin 4 stops motor, trouble is probably on main board.
Tape unloads, tape shears or tape unwinds.	Check for pulses at 7C, pin 3 on main board.	If no pulses, trouble is on main board. If pulses present, trouble is on motor driver board or sensor assembly.
Unselectable, Select LED will not light.	Ground 2B, pin 14 on main board.	If symptom remains, trouble is on main board.
Hangs on Read Status command.		Trouble is in Intelligent Controller.
Excessive rewrites.	Check for pulses at 7E, pin 12 on main board.	If no pulses, trouble is on main board, else trouble is in Intelligent Controller.
Does not write or has unrecoverable write errors. Reads OK.	Check for pulses at 7E, pin 12 on main board.	If no pulses, trouble is on main board, else trouble is in Intelligent Controller.
Does not write or read.	Check for low signal at 3A, pin 12 on main board. If OK, rewind tape and check for low pulses at 3A, pins 10 and 11.	If all pulses OK, trouble is in the Intelligent Controller. If not, trouble is on main board.

CHAPTER 5

FIELD CHECKS AND ADJUSTMENTS

5.1 GENERAL INFORMATION

There are no field adjustments for the Archive Intelligent Tape Cartridge Drive. The adjustments listed in Chapter 6 are shop adjustments requiring special equipment. There are two field checks that are overall performance tests. These are the read test and the write test.

5.2 EQUIPMENT REQUIRED

1. A known good tape with known data written on the Master Drive. Number of read errors when tape is read on Master Drive should be known. This tape is used only for read testing.

2. A known good tape to be used for write testing.

5.3 READ TEST

1. Using the known good tape, read a file from the tape.

2. Check soft error count. If tape was read with a comparable number of errors as were found on the Master Drive, the read channel is acceptable.

5.4 WRITE TEST

1. Using the good test tape, write a file of known data to the tape.

2. Check soft error count. If the data was written with a comparable number of rewrites as occurred with the Master Drive, then the write channel is acceptable.

CHAPTER 6

MASTER DRIVE

6.1 PURPOSE

A Master Drive is frequently maintained by users and distributors as a secondary standard. This Master Drive is used to check the quality of tapes written by drives which are in daily use in the field. Specifically, this drive may be used to create software distribution tapes or to create test tapes used for product verification. This chapter contains information to be used by a trained maintenance person and is intended to ensure the viability of the Master Drive as a standard.

6.2 MASTER DRIVE CLEANING

Perform the following cleaning procedures on the Master Drive after each 10 hours of use. Clean the drive after each new tape is used or, if all new tapes are being used, clean after every two hours.

1. Clean the read/write head using a clean Q-tip saturated with alcohol. Be sure to remove all visible oxide.

2. Using alcohol dampened Q-tips, clean the tape hole detector opening.

3. Using alcohol dampened Q-tips wipe all dust and debris out of the tape cartridge cavity.

6.3 MASTER DRIVE VERIFICATION

On a scheduled basis, perform the procedures in Appendix III using the special tools listed to verify the quality of the Master Drive. ARCHIVE CORP. will train personnel to effectively use these procedures.

CAUTION

Extreme caution should be exercised when performing the procedures in Appendix III on the Master Drive. Insure all personnel are properly trained and that adequate controls are in place prior to using the procedure in Appendix III.

CHAPTER 7

FIELD REMOVAL AND REPLACEMENT

7.1 GENERAL INFORMATION

Field shop replacement is limited to replacement of printed wiring boards, the drive motor, and the two microswitches. Replacement of these parts require the capability to perform the adjustment checks specified in Appendix III.

7.2 BASIC DRIVE REMOVAL AND REPLACEMENT

7.2.1 Main Board (Figure 7-1)

1. Disconnect all cables.
2. Remove four screws securing board to frame.
3. Carefully remove board and place it in a protective bag or box.
4. Gently lay main board on frame.
5. Ensure that cables are routed for easy reconnection.
6. Attach board with four screws.
7. Reconnect cables to board.
8. Place stepper motor phase shunts at location 5C on replacement board in locations similar to the phase shunts on the removed board.

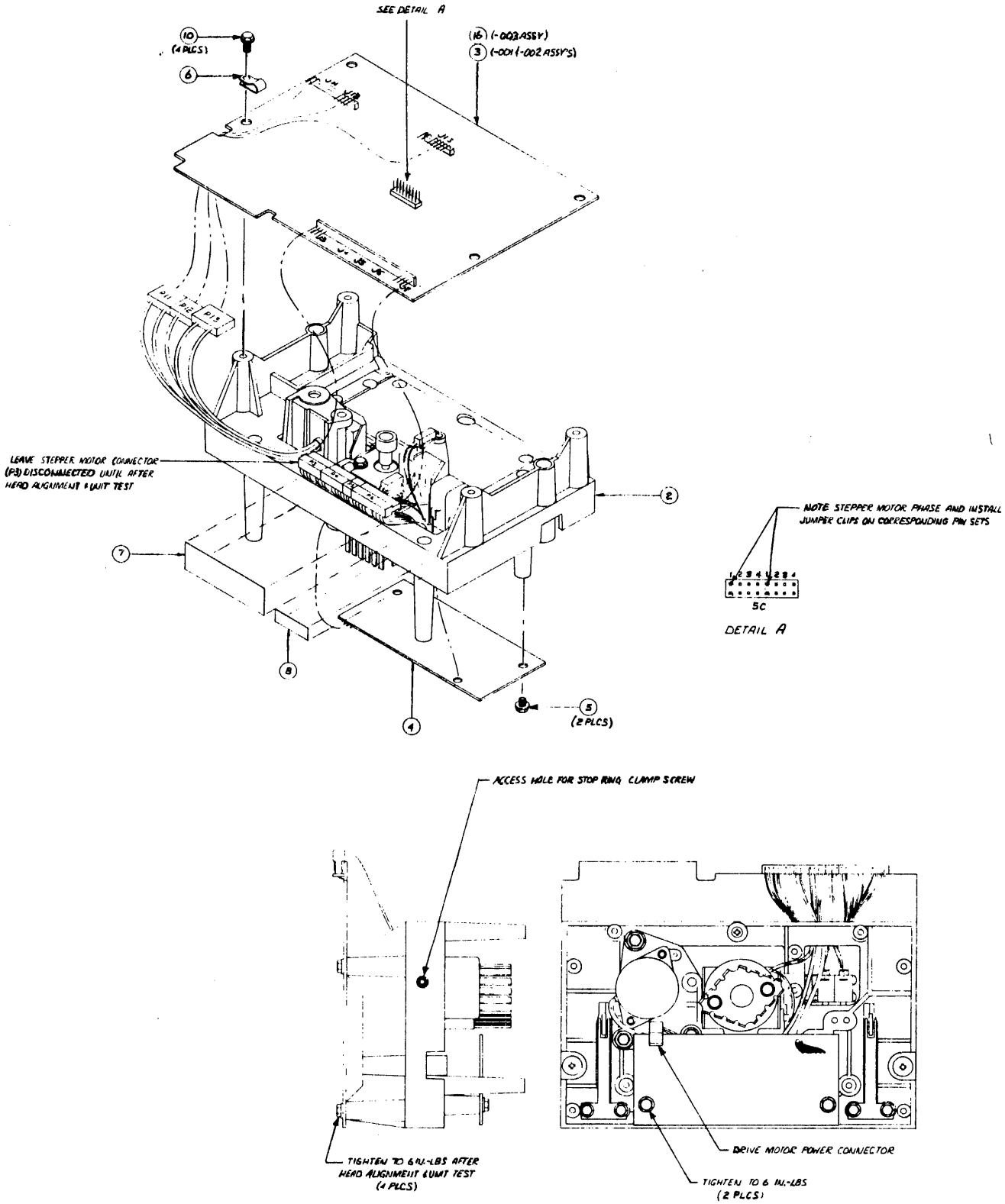


Figure 7-1. Main Board Removal Diagram

7.2.2 Motor Driver Board (Figure 7-1)

1. Disconnect cables to board.
2. Remove two screws securing board.
3. Carefully remove board and place it in a protective bag or box.
4. Attach board with two screws.
5. Reconnect cables to board.

7.2.3 Drive Motor Without Fan Assembly (Figure 7-2)

1. Disconnect cables to drive motor.
2. Remove four screws securing main board and lift it out of the way.
3. Remove two screws securing motor.
4. Carefully remove motor.
5. Carefully insert motor and position to match holes.
6. Attach with two screws.
7. Secure main board with four screws.
8. Reconnect cables to motor.

7.2.4 Drive Motor With Fan Assembly (Figure 7-3)

1. Disconnect cables to drive motor.
2. Remove four screws securing main board and lift it out of the way.
3. Remove four screws securing two motor brackets () to frame.
4. Carefully remove motor and brackets.
5. Remove two screws securing motor to brackets.
6. Attach replacement motor to brackets with two screws.
7. Carefully insert motor and brackets.
8. Secure brackets with four screws.

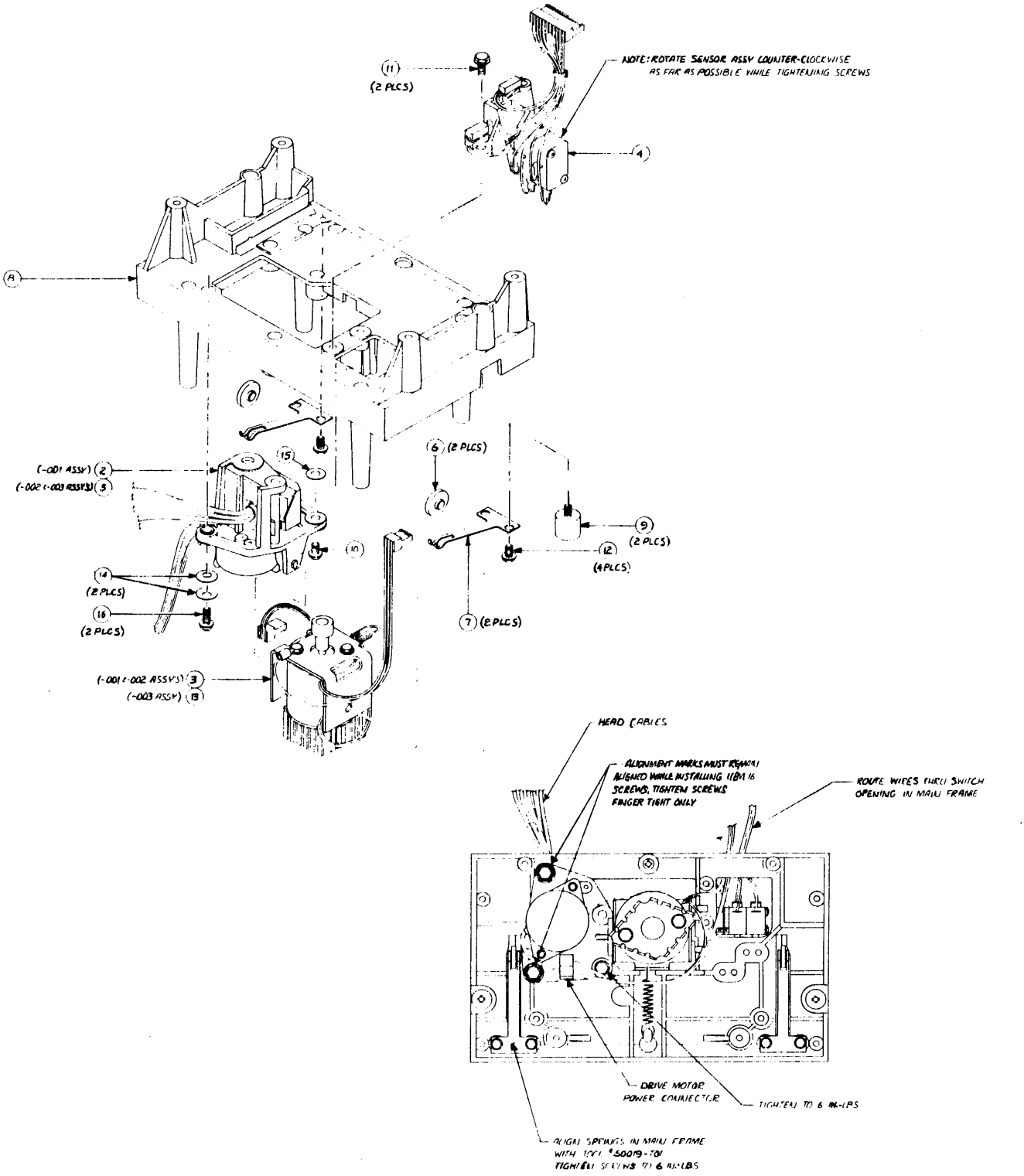


Figure 7-2. Motor (Without Fan) Removal Diagram

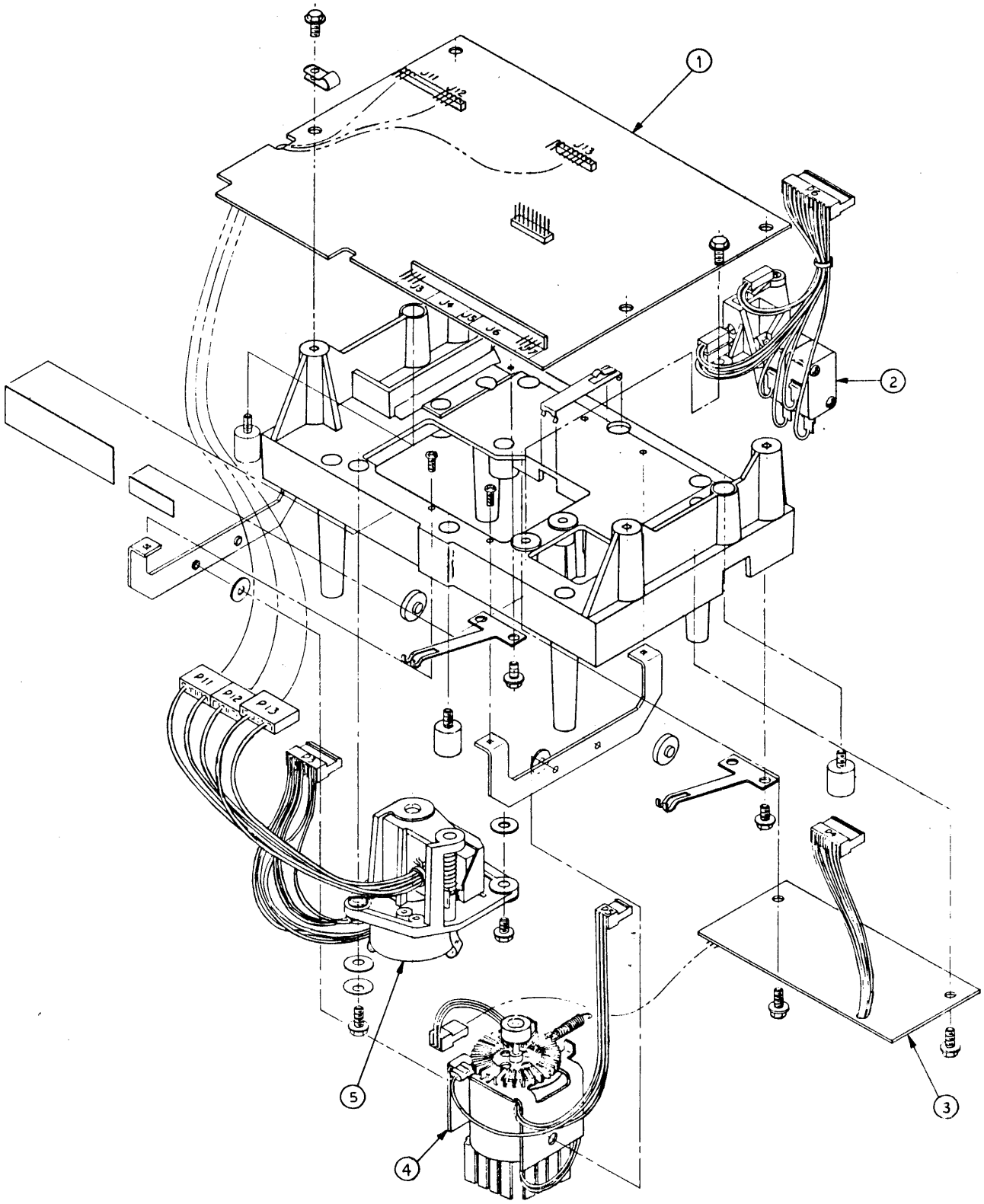


Figure 7-3. Motor (With Fan) Removal Diagram

9. Secure main board with four screws.

10. Reconnect cables to motor.

7.2.5 Sensor Block And Switch Replacement (Figure 7-2)

1. Remove main board.

2. Remove push-ons securing wires to photo diodes and LED. Note placement and orientation of push-ons for proper replacement.

3. Remove two screws securing tape hole sensor and switches.

4. Remove assembly carefully.

5. Remove two screws securing switches.

6. Remove push-ons securing wire to switches.

7. Replace by reconnecting push-ons to secure wires to switch.

8. Attach switches with two screws.

9. Carefully seat assembly in drive.

10. Attach assembly with two screws but do not tighten them.

11. Insert a tape cartridge.

12. Position assembly so the sensor does not touch the cartridge but clearance is 0.025-in. or less and tighten screws.

13. Replace main board.

7.3 INTELLIGENT CONTROLLER REMOVAL AND REPLACEMENT (Figure 7-4)

1. Disconnect cables to controller.

2. Remove four screws securing controller to frame.

3. Place controller in protective bag or box.

4. Place controller on frame and match holes.

5. Attach controller to frame with four screws.

6. Reconnect cables to controller.

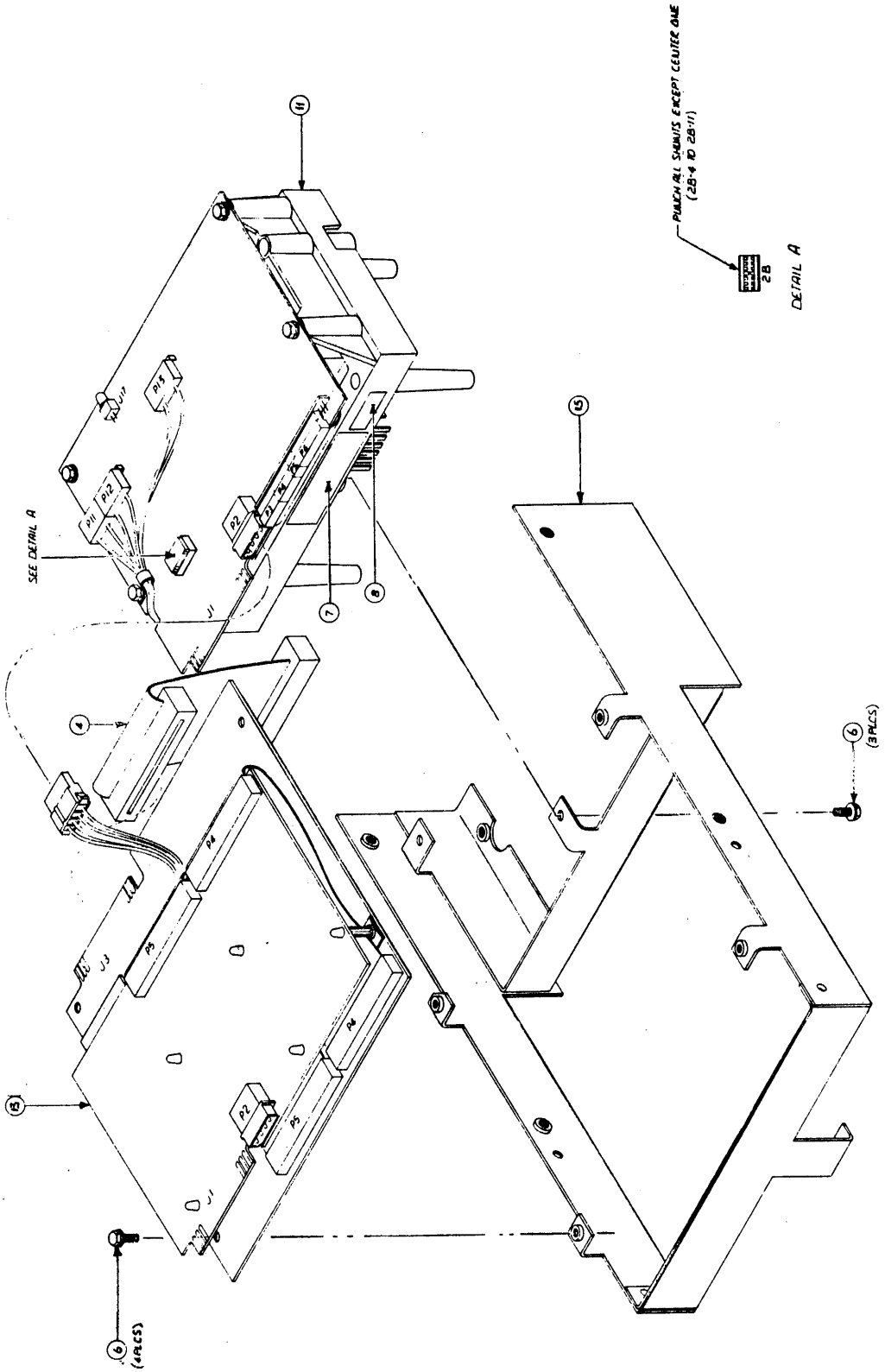


Figure 7-4. Intelligent Controller Removal Diagram

CHAPTER 8

BASIC DRIVE DEPOT MAINTENANCE

Section I.

THEORY OF OPERATION

8.1 OVERVIEW

Although the Basic Drive may be controlled directly by a customer controller, it is usually controlled by the Archive Intelligent Controller (Chapter 9). In either case, the Basic Drive must be supplied with +24 vdc and +5 vdc. When power is applied, and in response to RESET-, the head positioning stepper motor is driven to its calibration point and then back to track 0 position. When using a customer controller, the host must provide write data on dual complementary lines as serial data at the appropriate bit rate for the drive and also receive both read level and read pulse signals on single lines as serial data. Obviously, without an Intelligent Controller, the host must send the appropriate control signals to the Basic Drive. The logic diagrams (schematics) for the Basic Drive are in Appendix II, figures A2-1, A2-2, and A2-3. The parts lists and parts location diagrams are in Appendix I.

8.2 SIMPLIFIED BASIC DRIVE DATA FLOW (Figure 8-1)

The Basic Drive may be one of four drives so the select signal may be on any of the four input lines (J1-16, 18, 20, or 22). Whether a Basic Drive is selected by a given select signal depends on the address shunt in 2B. There are five address shunts available; always selected, drive 0, drive 1, drive 2, and drive 3. The appropriate select signal enables the microprocessor, the write drivers, and the read line drivers.

Since the Basic Drive writes to or reads from one of four tracks at a time (nine tracks for 9045 unit), input track selector signals are required. The track selector signals select the appropriate read and write heads, controls head positioning, and controls the erase head. The erase head functions only when track 0 is selected and the erase enable input signal is present.

Anytime the Basic Drive is separated from the controller or when more than one Basic Drive is serviced by one controller, line terminators must be inserted in the controller and in the last drive. The line terminator network is in a 14-pin, 180/390-ohm, resistor network DIP package. When required, one package is inserted at location 6B of the Intelligent Controller (figure A2-8) and two packages in the Basic Drive at locations 1A and 3A (figure A2-1).

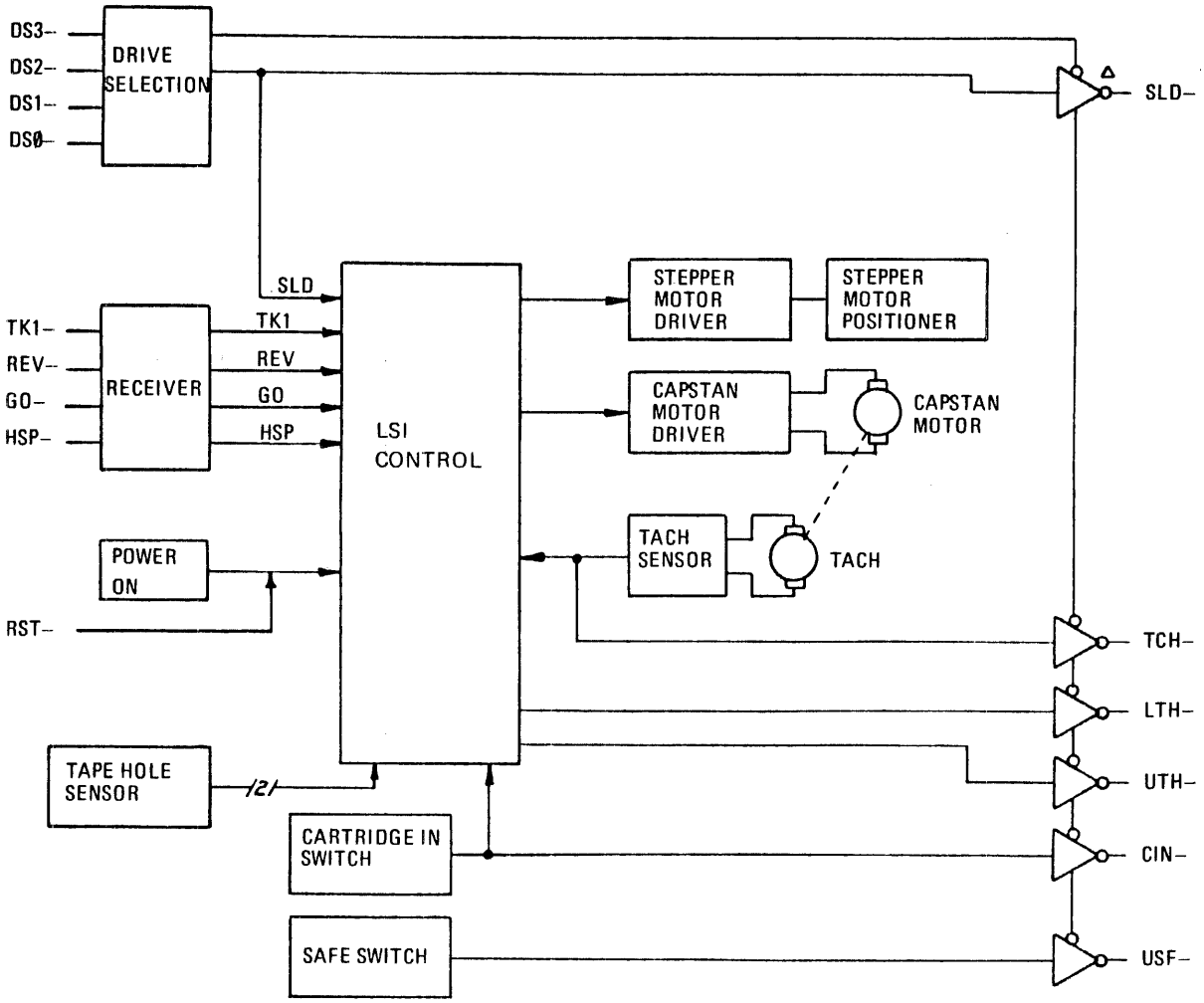


Figure 8-1. Basic Drive Control and Motor Circuits Block Diagram

The Basic Drive has a 3.5795 megahertz clock circuit. The two clock signals generated by the clock circuit trigger operations by the microprocessor and control the switching of the erase signal. All other operations in the Basic Drive are asynchronous.

Once a Basic Drive has been selected and track commanded (always track 0 initially), a move tape forward (GO-) signal is required to cause the capstan motor to move the tape. The GO- signal, a processed tachometer signal from the capstan, and the speed control signal (HSPD-) are used by the microprocessor to

maintain a constant capstan motor rotation at the selected speed. As the capstan motor rotates, the tape is moved past the read/write head, the capstan, and the tape hole sensors (figure 8-2).

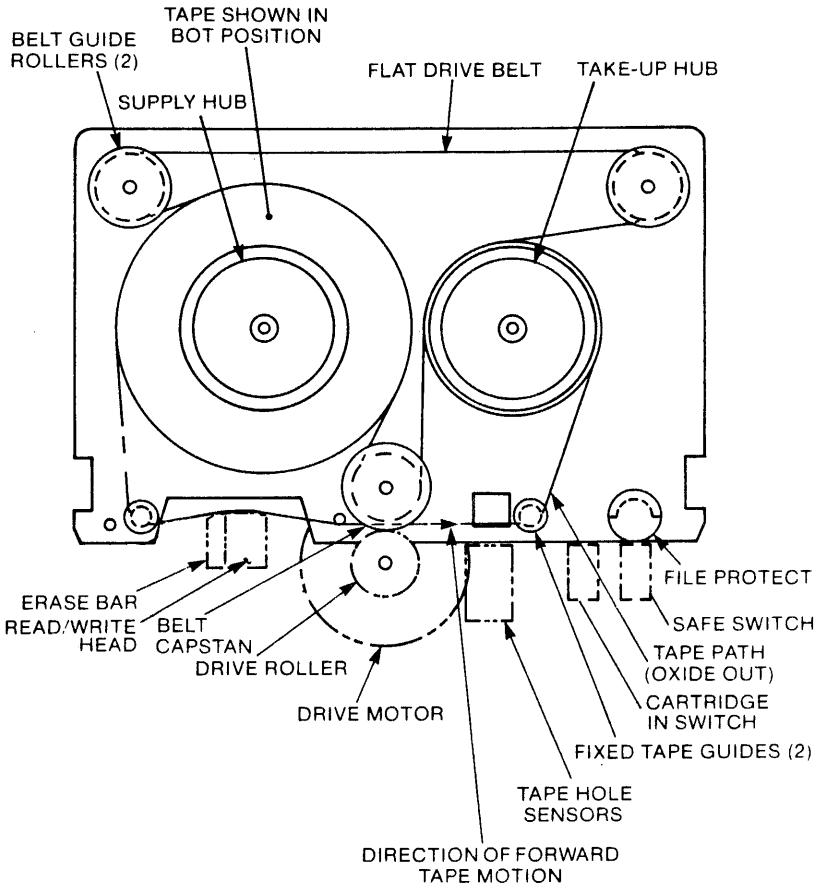


Figure 8-2. Tape Cartridge Relationship to Basic Drive.

The tape in the tape cartridge is normally opaque because of the oxide coating. However, there are a number of precisely located holes near each end of the tape (figure 8-3). These holes permit light from a LED (light emitting diode) to strike one or both of the light-activated transistors which generate a hole detected signal. These hole detected signals are used by circuits in the Basic Drive to control tape motion, writing on the tape, and reading from the tape. Near the beginning of the tape are three pairs of holes located at 18-inch intervals. The Basic Drive circuits recognize this hole configuration as beginning of tape (BOT). A single hole between track 0 and track 1 placed 36

inches beyond BOT marks the tape load point. Writing starts at this point. Near the other end of the tape are four holes. As the tape moves in the forward direction the first hole (between track 0 and 1) is the early warning hole. Writing and reading may continue beyond this hole but will stop before the tape reaches the three end of tape (EOT) holes that are 48 inches beyond the early warning hole (figure 8-3).

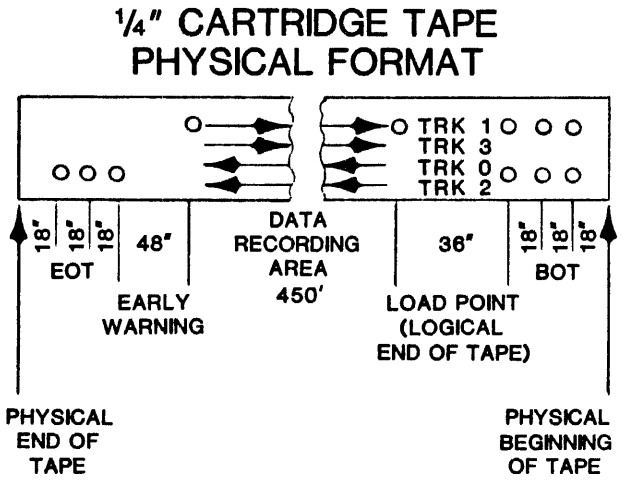


Figure 8-3. Hole Placement On Tape.

When track 0 is selected and the erase enable signal (EEN-) is true, the erase head is activated and the tape is erased. When the Basic Drive is slaved to an Intelligent Controller, the tape is erased as track 0 is written. Therefore, normal operation is to erase the tape each time track 0 is written. This ensures that data will not be written over old data. In order for the write circuits to be activated, the cartridge must not have the file protect cam in the safe position and the write enable signal (WEN-) must be true (figure 8-4).

The read circuits are always operating. The tape is read after being written and during read operations. The difference in the use of the read data is left to the Intelligent Controller or the host. Within the Basic Drive, the difference between read-after-write and read data is caused by requiring read-after-write data to exceed a 25 percent threshold (figure 8-5).

8.3 POWER CIRCUITS

The power circuits are shown in the lower left corner of figure A2-1. The capacitors connected between +5 vdc and ground are distributed on the PWB as transient suppressors. Capacitor C32 and diode CR15 are connected between +24 vdc and ground for spike suppression. The +24 vdc supplies regulator, 4B, which provide regulated +12 vdc.

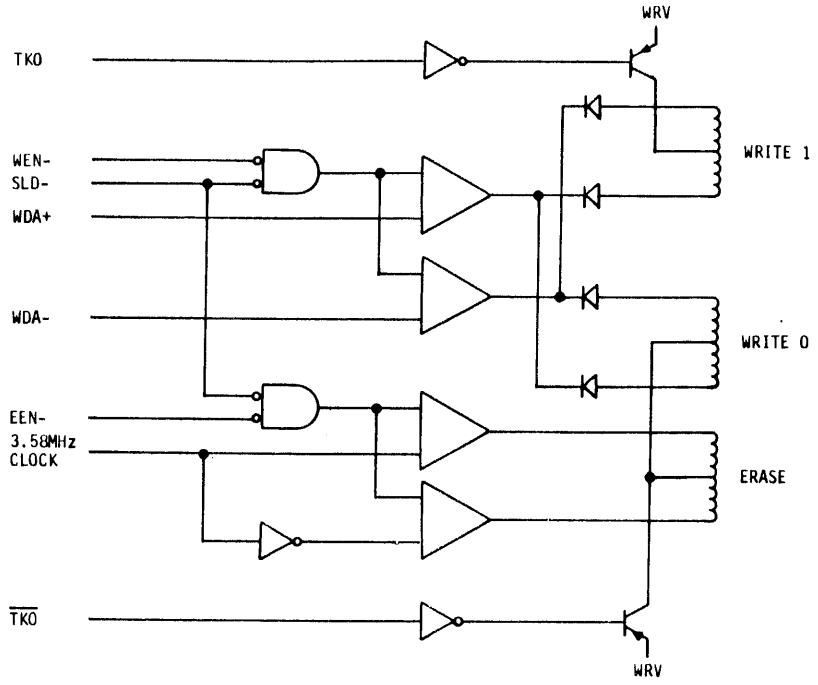


Figure 8-4. Write Circuits Block Diagram

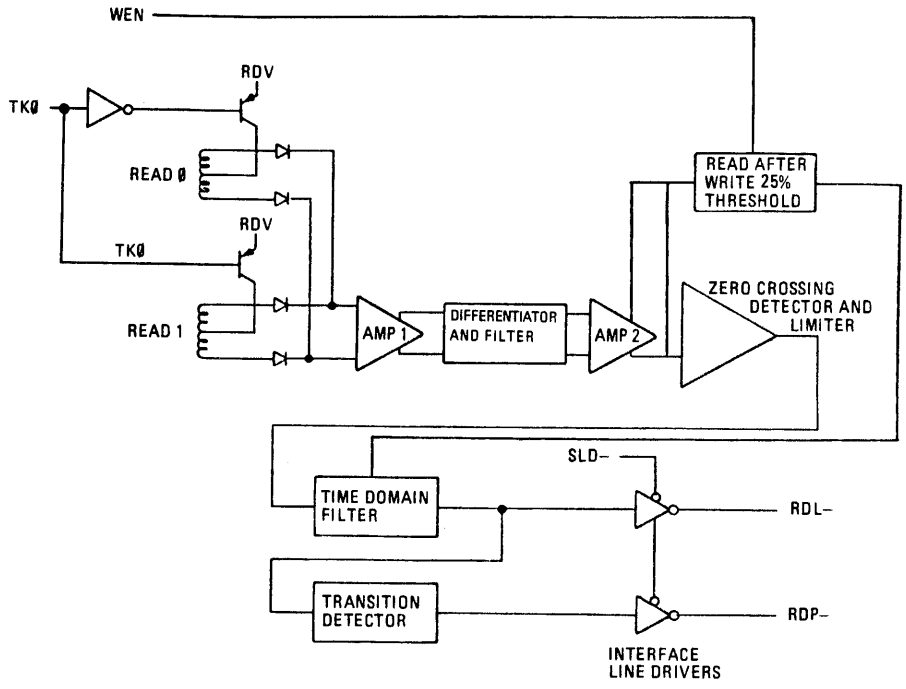


Figure 8-5. Read Circuits Block Diagram

8.4 CLOCK CIRCUITS

The 3.5795 megahertz clock generator (shown top, center, figure A2-1) consists of crystal, Y1, and four of the inverters in the 74LS04 in 1D. The outputs, CLK and CLK are isolated by two AND gates in the 74LS09 in 2D for use by the microprocessor. This isolation is required since the microprocessor will create its own clock with a crystal connected between its XTAL1 and XTAL2 inputs. The feedback for this capability, if it were not isolated, would degrade the clock signals. The clock signals generate the erase signal when gated to the erase drivers by erase enable.

8.5 POWER-UP AND RESET

The reset circuits are shown in the upper right corner, figure A2-1. The RESET- signal from the host or the Intelligent Controller is ORed with the PSEN, WR, and PROG signals from the microprocessor to create the reset signal for the microprocessor. To the left of the reset input to the microprocessor is the power-up reset pulse generator. In response to the reset pulse, the microprocessor generates the stepper controls to drive the stepper motor to its calibration point.

8.6 STEPPER CIRCUITS

The stepper circuits are shown in the upper right, figure A2-1. The stepper phase signals, P15 and P16, are inverted twice to provide four phase signals. In order for these signals to actually agree with the calibration point, they are routed through 5C. Two shunt clips are inserted onto the pins of 5C to select the proper phase signals. The two selected signals are again inverted to generate the four signals required by the stepper motor. The four signals are gated to the stepper motor by STPEN from the microprocessor.

8.7 SELECT CIRCUITS

The select circuits are shown in the upper left corner, figure A2-1. When a drive is selected, the select signal is inverted to enable the microprocessor and inverted again to become SELD. The select signal also causes an inverter to drive LED, CR16. SELD enables the write drivers, the erase drivers, and the output line drivers. Accurate drive selection requires a jumper in 2B, figure A2-1, a jumper from pin 7 to pin 8 always selects the drive. The other positions of the jumper determine the drive number: a jumper between pins 4 and 11 defines drive 0, between pins 3 and 12 defines drive 1, between pins 2 and 13 defines drive 2, and between pins 1 and 14 defines drive 3.

8.8 TRACK SELECTION CIRCUITS

The track selection circuits are shown in the upper left, figure A2-1. Although there are four track selection input circuits, only track 0 and track 1 get through 1C on 20 Mbyte units. On 45 Mbyte units all four track select bits are passed through 1C. Both TR0- and TR1- are inverted on 1B. TR0 is then inverted to become TR0-. The track signals, TR0 and TR1, are used by the microprocessor. TR0 and TR0- are used to select the appropriate read and write heads by switching the current source to the correct write head and by bias from the +12 vdc to the correct read head. TR0 high enables write head 1 and read head 1. TR0- high selects write head 2 and read head 2.

8.9 CAPSTAN MOTOR CONTROL

The capstan motor control circuits are shown across the center, figure A2-1 on the left of the microprocessor. These circuits include the inverter/buffers for the REV- and GO- signals, the tachometer circuits, the hole detector circuits, and the circuits associated with the write protect switch, and cartridge-in-place switch. On the right of the microprocessor, these circuits include the exclusive OR gates, 7C and a divide-by three counter, 3D. REV- (reverse) and GO- (move tape) are inverted on 1B and routed to the microprocessor. When REV- is high at J1, the tape moves forward; when GO- is high, tape stops. REV- determines which output, P21 (forward) or P20 (reverse), of the microprocessor will be a pulse train. The pulse width in the pulse train determines the energy delivered to the capstan motor. As the positive portion of the pulse train becomes wider, more energy is applied to the motor and it accelerates. As the motor approaches the correct speed, the width of the positive portion of the pulse becomes narrower until both the motor speed and pulse width stabilize at the correct speed. As the capstan motor turns, a tachometer signal is generated by the motor. This tachometer signal waveform is cleaned up by the twin T filter and then is processed by dual operational amplifier, 6C. The first operational amplifier converts the tachometer signal to square waves. Coupling capacitor, C37, and the second operational amplifier generate a 50 microsecond negative pulse (tach pulse) for each square wave. The square wave tachometer signal from the first operational amplifier is transmitted to the host or the Intelligent Controller by line driver, 2A, shown on right, center, figure A2-2.

The output of a counter which is in the microprocessor is divided by three by the flip-flops at 3D shown to the right of the microprocessor. The output of the divide-by-three circuit is compared with the tach pulse to control the width of the negative pulses (P20 or P21) generated by the microprocessor to drive the capstan motor.

The upper hole and lower hole transistors shown left, center, figure A2-1, generate signals that are used by the microprocessor to identify which portion of the tape is passing the read/write heads. The signals from these photo-transistors are shaped by the operational amplifiers, 6C, to set the flip-flops, 6D. After the presence of the hole is recognized by the

microprocessor, it generates a signal to reset the flip-flops. When either hole signal is still present from the NOR gate, 4D, after the flip-flops are reset, the microprocessor presumes that the tape has run off the supply reel and so, stops the capstan motor. The CIN switch is closed when the cartridge is correctly seated. Inverter, 3B, shown at the bottom, right, figure A2-1, has a low output when the CIN switch is open which inhibits the microprocessor from energizing the capstan motor. This signal is also transmitted to the host or Intelligent Controller by line driver, 2A.

8.10 MOTOR DRIVER BOARD

Figure A2-3 shows the motor driver board and its connection to the capstan motor. The motor driver board translates a low-frequency positive pulse train into a higher frequency pulse-modulated motor drive signal. The duty cycle of the high frequency drive signal is proportional to the input pulse width. Control signals and power for the circuits and the motor are present at P4, pins 1 through 7. The signals SREV and SFWD control the direction and speed of the capstan motor. Only one of these two signals is active at a time. Since the logic is the same for both directions, only forward tape motion is described.

The signal SFWD is output by the microprocessor on the main board. The signal is a constant period square ware of varying positive pulse width. The power applied to the capstan motor is proportional to the positive pulse width. A wider pulse applies more power to the motor and it turns faster. The signal SFWD is received at pin 9 of 2E. The output on pin 8 goes to a cross-coupled flip-flop. This flip-flop senses which of the two control signals is active (SFWD or SREV) and enables the voltage control circuitry to possess the pulse-width-modulated signal. When SFWD is active, pin 8 of 2E causes 2E, pin 6 to go high, which causes 1B, pin 8, to go low. This turns on Q8, which turns on Q4. 1B, pin 8, also disables 1B, pin 5, disabling the reverse direction transistors. It is the inactive state of SREV through 1B, pin 11, that enables 1B, pin 2. The other input to 1B (pin 1) receives the modulated, translated logic signal which will control the application of power to the capstan motor.

The signal SFWD also goes to 1E, pin 1. The output, on pin 3, is fed through a filter (R24, C7) which converts SFWD to a DC voltage that is proportional to the positive width of SFWD. This voltage is monitored by the comparator at 1C, in on pin 5, out on pin 7. The output from pin 7 is applied to the control input of the timer 2G, pin 11. This timer performs a frequency translation function. A 5000-Hz square wave is applied to the trigger input of 2G on pin 8. The output of the timer (pin 9) is a 5K-Hz signal whose duty cycle is proportional to the control voltage applied to pin 11. The result of this circuit (R24, C7, 1C and 2G) is a digital signal with a duty cycle that is directly proportional to the width of SFWD (or SERV) but which has a frequency that is about eight times greater (at 90 i.p.s.). The output of 2G, pin 9, is fed through 1E, in on pin 5, out on pin 6. This digital signal of varying duty cycle is used to switch Q7, thus switching Q1, applying +24V to the capstan motor. The output of pin 6 is also filtered as SFWD was. The resulting DC voltage is placed on the other input of the comparator, 1C, pin 6. This voltage is directly proportional to the duty

cycle of the signal on 1E, pin 6. This allows the higher frequency modulated cotrol signal to be compared to the original modulated control signal, SFWD. When the voltage on 1C, pin 7, is not high enough, then the voltage on 1C, pin 6, does not equal to the voltage on 1C, pin 5, and the voltage at 1C, pin 7 is increased. This circuit is a closed loop servo that ensures that the duty cycle of the translated modulated control signal equals the width of SFWD. This circuit is frequency sensitive (tape speed of 30 or 90 i.p.s.). To allow for either speed, the proper component value is jumper selectable, choosing either R34 or R41 for the filter of the frequency translated signal.

The two remaining circuits on this board are overcurrent circuits. Current is monitored by sensing the voltage across R1. The first comparator, 2C, in on pins 2 and 3, is a fast reacting circuit. It reacts quickly at a higher current value than the other overcurrent circuit. It is primarily used to prevent too-rapid accelertion of the tape. If this circuit is triggered, its output 2C, pin 1 disables SFWD (or SREV) at 1E, pin 3, until current drops to an acceptable limit.

The other overcurrent circuit reacts more slowly and triggers at a lower current value. Its input are pins 2 and 3 of 1C. Its output is on 2C, pin 7. When triggered, this circuit produces the signal OL-, which goes to the microprocessor on the main board. The microprocessor responds by stopping tape motion.

8.11 WRITE CIRCUITS

The write circuits are shown on the lower left one-fourth of figure A2-2. Before anything can be written to the tape, a number of conditions must be satisfied. The Basic Drive must be selected, the stepper motor must not be enabled, the cartridge write protect cam must be positioned to close the USF switch (lower, left, figure A2-1), and the appropriate write head must be selected by one of the TRO signals. Transistor Q3 and 2E form a write current switch. Q3 functions as an AND gate since the USF switch must be closed to provide a ground for its emitter and STPEN must be false to drive the base of Q3 to control base drive to 2E. The inverted TRO or TRO- signals (7D, pins 11 and 13) will saturate one of the two transistors (2E) connected to a write head. When TRO is high, current flows through the write 1 head, pins 8 and 10 of 2E, and pin 14 of 2E. When the erase circuits are enabled, this is also the path for erase current. When TRO is high, current flows through the write 2 head, pins 7 and 5 of 2E, and pin 14 of 2E.

Write enable (WEN-) from the host or the Intelligent Controller and SELD from the select circuits are ANDed in 4D to provide a high at pin 13 of 4D. This signal enables the complementary write (WDA- and WDA+) signals, when high, to drive transistors Q5 or Q4 through the AND gates at 2D. This signal also enables the NAND gates (6E, upper, right, figure A2-2) used for read-after-write verify. Q9 and its associated circuitry provide current limiting. Diodes, CR3 through CR6, provide head isolation and protect Q4 and Q5 from switching transients. The erase circuits are identical to the write circuits except for input signals.

Erase enable (EEN-) replaces write enable, and the complementary clock signals replace the complementary write signals.

8.12 READ CIRCUITS

The read circuits are shown on figure A2-2. The flow is from the read heads in the upper left corner to amplifiers, 7E, on the right and through the one-shot multivibrators, 4E, flip-flops, 5E, and the line drivers, 2A, in the center right. The read heads are selected, as were the write heads, by TR0 and TR0-. In this case the inverted signal at 7D applies a bias voltage to the center-tap of the selected head which forward biases CR9 and CR10 for the read 1 head or CR7 and CR8 for the read 2 head. This action gates the signal read from the selected head to read amplifier 5F. The outputs of 5F, observed at TP1 and TP2 as a 200 to 600 millivolt pulse, represents a flux reversal which indicates a logical one. The pulses from 5F saturate amplifier, 7F, in such a manner that it switches with each logical one. The lower comparator, 7E, is a zero threshold comparator that switches on any transition of the input signal. The upper comparator is a 25 percent comparator and so requires a quality signal to switch. During a read operation the output of the lower comparator creates the read signals. During a write operation the 25 percent comparator must detect the signal for the read level signal to be generated.

The read signal from the zero threshold comparator triggers the top one-shot multivibrator, 4E. At the time out of one-shot 4E, the state of the read signal at 6E, pin 8 is latched by flip-flop 5E. The output of this flip-flop is the read level signal and is transmitted to the host or the Intelligent Controller as RDL- from line driver 2A. Lower one-shot, 4E, is triggered by the RDL flip-flop and generates the read pulse. Lower flip-flop, 5E, conditions the exclusive OR gate to trigger the one-shot on the next opposite going transition.

Section II.

PERFORMANCE TESTING

8.13 SCOPE

Performance testing is of two types; performance testing of suspected Basic Drives and performance testing of repaired Basic Drives. In either type of performance testing, the Basic Drive should be mated with a known good Intelligent Controller and known good tapes should be used.

8.14 TESTING SUSPECTED DRIVES

Always clean the read/write heads and verify that the sensor block is secure before testing the Basic Drive.

8.14.1 Read Check

Using a known good tape with known data recorded on it and with the Basic Drive mated with a known good Intelligent Controller, attempt to read the tape.

NOTE

Do not use the Track Zero Alignment Tape or the Azimuth Alignment Tape for this check.

If the tape can be read but has an unacceptable number of retries, then perform the alignment procedures in Appendix III. If the tape cannot be read, refer to the trouble list in Chapter 4.

8.14.2 Write Check

NOTE

Due to imperfections in the tape oxide coating, it is not uncommon to encounter numerous soft errors during writing of data to tape. With a known good qualified cartridge this soft error rate could approach 200 rewrites for a 20 Mbyte transfer.

Using a tape that is known to be physically a good tape and with the Basic Drive mated with a known good Intelligent Controller, attempt to write to the tape.

NOTE

Ensure that the write protect cam on the cartridge is in the write position before inserting the cartridge in the Basic Drive.

If the tape is written on but has an unacceptable number of retries, then perform the alignment procedures in Appendix III. If the Basic Drive cannot write on the tape, recheck the position of the write protect cam and the condition of the tape. If the problem is not with the tape cartridge, refer to the trouble list in Chapter 4.

8.15 TESTING REPAIRED DRIVES

Before testing a repaired Basic Drive, perform the alignment procedure in Appendix III.

8.15.1 Read Check For Serviceability

Using a tape with zero read errors when read by the master drive and with the Basic Drive mated with a known good Intelligent Controller, attempt to read the tape. If there are a comparable number of read errors, then the Basic Drive may be returned to service.

8.15.2 Write Check For Serviceability

Using a known good tape, preferrably an Archive qualified tape, and with the Basic Drive mated with a known good Intelligent Controller, attempt to write to the tape.

NOTE

Ensure that the write protect cam on the cartridge is in the write position before inserting the cartridge in the Basic Drive.

If there are zero write errors, then the Basic Drive may be returned to service. Otherwise, write to the test tape with the master drive. If the number of errors is the same as with the repaired Basic Drive, then it may be returned to service. Policy may permit the Basic Drive to be returned to service with a small number of errors.

Section III.

REPAIR PROCEDURES

8.16 SCOPE

The repair procedures in this section includes removal and replacement procedures, troubleshooting tips, and general precautions.

8.17 GENERAL PRECAUTIONS

Within the drive mechanism, dirt, particularly oxide dust from the tape, degrades the operation of the Basic Drive. In all cases, when a Basic Drive has been removed from service for repair, the read/write head should be thoroughly cleaned using a swab saturated with alcohol. The holes in the hole sensor block should be carefully cleaned. All foreign material in the Basic Drive should be removed using a vacuum and a soft bristle brush. When unsoldering and resoldering connections, be sure to use the appropriate size soldering tips. The tips should be large enough to melt the solder quickly and small enough not to damage insulation or semiconductor devices or loosen the circuit from the board. When possible, place a heat sink, such as long nose plier tips, between the semiconductor and the solder joint. When unsoldering, use a device to remove the melted solder. Always place piece parts that have been removed to gain access for repair in a plastic box or plastic bag for use during reassembly.

8.18 TROUBLESHOOTING TIPS

Obvious damage caused by overheating or breakage should always be repaired first. The information given in the trouble lists in Chapter 4 should be used to isolate the source of trouble to a specific circuit. Substitution of known good motors within the circuit by disconnecting the motor in the Basic Drive and connecting the good motor without physically replacing the suspected motor can often save time. When the trouble has been isolated to one of the printed wiring boards (PWBs), it may be necessary to use an oscilloscope to isolate the trouble. There are, however, some facts that tend to suggest the failing part. The following is a list of electronic components presented in the order of their failure frequency:

Motors (including misalignment and overloading)
Light Emitting Diodes
Power Transistors
Photo Transistors
Complex Integrated Circuits
Capacitors (fail short)
Signal Transistors
Diodes (fail open)
Mechanical Switches
Resistors

This list is useful only as a clue after the faulty circuit has been isolated. All of the components can be expected to operate acceptably for thousands of hours.

Whenever there is evidence of physical mistreatment of the Basic Drive, it is reasonable to check all solder connections.

8.19 REMOVAL AND REPLACEMENT

It is presumed in these procedures the Basic Drive is not connected to the Intelligent Controller. When the Intelligent Controller is still with the Basic Drive, exercise care not to damage the Intelligent Controller while disassembling the Basic Drive. It is recommended that the Intelligent Controller be removed prior to removing any mechanical assembly from the Basic Drive.

8.19.1 Field Replaceable Parts

The removal and replacement procedures for the main board, the motor driver board, the drive motor, the sensor block, and the micro-switches are in Chapter 7.

8.19.2 Stepper Motor And Read/Write Head

1. Remove the main board (Chapter 7).
2. Remove three screws securing stepper motor assembly to frame.
3. Carefully remove stepper motor assembly from drive.
4. Carefully place stepper motor assembly in drive and align mounting holes.
5. Replace three screws and secure stepper motor assembly to frame.
6. Replace main board.
7. Alignment of unit is required.

CHAPTER 9

INTELLIGENT CONTROLLER DEPOT MAINTENANCE

Section I.

THEORY OF OPERATION

9.1 OVERVIEW (Figure 9-1)

The Intelligent Controller (controller) is microprocessor based which relieves the host of the overhead functions of tape positioning, tape formatting, and error processing. The controller also permits eight-bit parallel byte transfer of write data from and read data to the host. The controller may process data to as many as four Basic Drive units. In addition to the bi-directional eight-bit data bus, there are four control signals sent to the host and four control signals required from the host. The host supplies ONLINE, XFER, REQUEST, and RESET to the controller. The controller supplies READY, ACK, DIRC, and EXCEPTION to the host. The logic diagrams for the Intelligent Controller are A2-4 through A2-8.

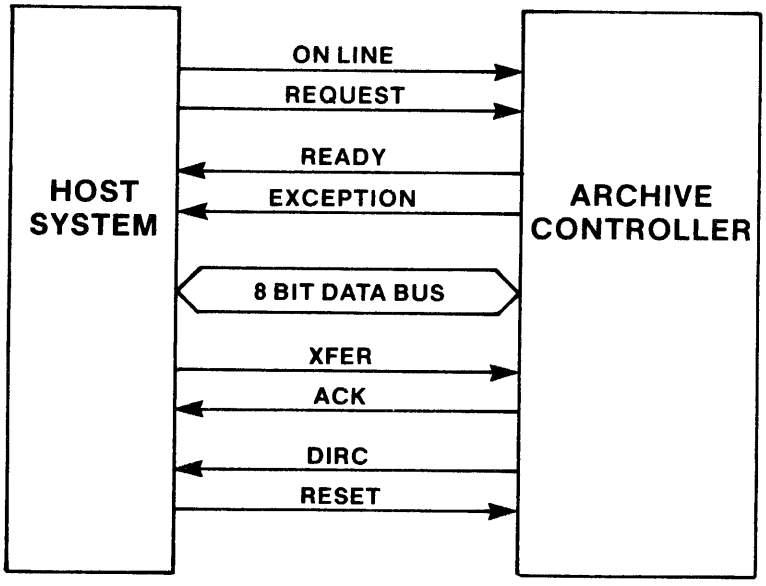


Figure 9-1. Controller/Host Interface

9.2 ONLINE

ONLINE must be true for any read or write operation and remain true throughout the operation. If ONLINE goes false during a write operation, the controller writes the content of its buffers to tape followed by a File Mark and then commands the Basic Drive to rewind the tape to BOT. If ONLINE goes false during a read operation, the controller stops transferring data to the host at the next block boundary and commands the Basic Drive to rewind the tape to BOT.

9.3 XFER (TRANSFER)

XFER- is set true during a write operation by the host to indicate that it has put data on the data bus and, during a read operation, to indicate that it has read the data bus. In either case, XFER- goes true once for each byte transferred.

9.4 REQUEST

REQUEST is set true by the host to indicate that it has a command to transfer to the controller or indicates host has read a status byte during a Read Status sequence.

9.5 RESET

RESET from the host causes the same action as the POWER-ON reset. That is, the controller is reset and the Basic Drive stepper motor is driven to its calibration point and then back to the track 0 position. Figure 9-2 shows reset timing.

9.6 READY

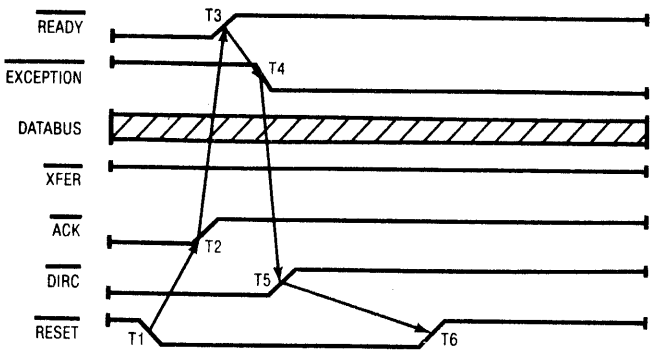
Controller generated signal which indicates one of the following:

1. If no operation is currently in process, READY means that the controller is ready to act on a command from the host.

2. During a command transfer (from the host) operation, READY means that the controller has read the command byte from the data bus.

3. During a status transfer (to the host) operation, READY means that the controller has placed the next status byte on the data bus.

4. During a positioning operation, READY means that positioning has been completed.



RESET TIMING

ACTIVITY	CRITICAL TIMING
T1-HOST ASSERTS $\overline{\text{RESET}}$	NA
T2-CONTROLLER DISABLES $\overline{\text{ACK}}$	T1→T2<0.25 U sec.
T3-CONTROLLER DISABLES $\overline{\text{READY}}$	T1→T3<0.25 U sec.
T4-CONTROLLER ASSERTS $\overline{\text{EXCEPTION}}$	T1→T4<3 U sec
T5-CONTROLLER DISABLES $\overline{\text{DIRC}}$	T1→T5<3 U sec
T6-HOST DISABLES $\overline{\text{RESET}}$	T1→T6>13 U sec.

Figure 9-2. Reset Timing Diagram

5. During a write operation, READY indicates that the controller has a buffer ready to be filled, that a Write-File-Mark (WFM) command may be issued or that ONLINE may be taken false.

6. During a WFM operation, READY indicates that the command has been completed, i.e., the File Mark has been written.

7. During a read operation, READY indicates that a buffer is full and ready to be transferred to the host, a Read File Mark command may be issued, or that ONLINE may be taken false.

9.7 ACK (ACKNOWLEDGE)

ACK indicates, during a write operation, that the byte on the data bus has been read and, during a read operation, that a byte has been put on the data bus for transfer to the host.

9.8 DIRC (DIRECTION)

DIRC indicates the direction of data transfers between the controller and the host. DIRC is true for transfers from the controller and the host (status and read operation). DIRC is false for transfers from the host to the controller (command and write operations). DIRC is a hardware convenience only.

9.9 EXCEPTION

EXCEPTION goes true for an error condition, when a File Mark is read, and after RESET whether it is a POWER-UP reset or a host originated RESET. The first command from the host to the controller after an EXCEPTION must be a Read Status command since the controller will not accept any other command.

9.10 CONTROLLER DATA FLOW (Figure 9-3)

The controller is programmed by the host commands transmitted on the data bus. Each command results in a sequential set of subfunctions in the controller that result in commands to the Basic Drive. When the command is either read or write, data is stored in three 512 byte buffers. Write data from the host is loaded into one buffer at a time. During write operations, one buffer is being loaded, one has been loaded and is being written to tape, and the third has been loaded, its content written to tape, and it is awaiting completion of the read-after-write check. Read data from the Basic Drive is also temporarily stored in the three buffers. During a read operation, one buffer is being loaded from tape, another is being transferred to the host, and the third is reserved for use if the host gets behind.

9.11 HOST COMMANDS

All commands from the host to the controller are transferred on the data bus. They are single-byte two-field commands. The most significant three bits (7,6,5) indicate the command type and the least significant five bits contain the command data if required. Only Select and Position require command data. There are seven command types as defined below.

Command	Command Type	Bits 7 6 5
Select	0	0 0 0
Position	1	0 0 1
Write Data	2	0 1 0
Write File Mark	3	0 1 1
Read Data	4	1 0 0
Read File Mark	5	1 0 1
Read Status	6	1 1 0

Generally, the controller will accept any command when READY is true except that only Read Status is accepted when EXCEPTION is true. READY need not be true for the controller to respond to the Read Status command. All unused modifier bits in the command byte must be zero.

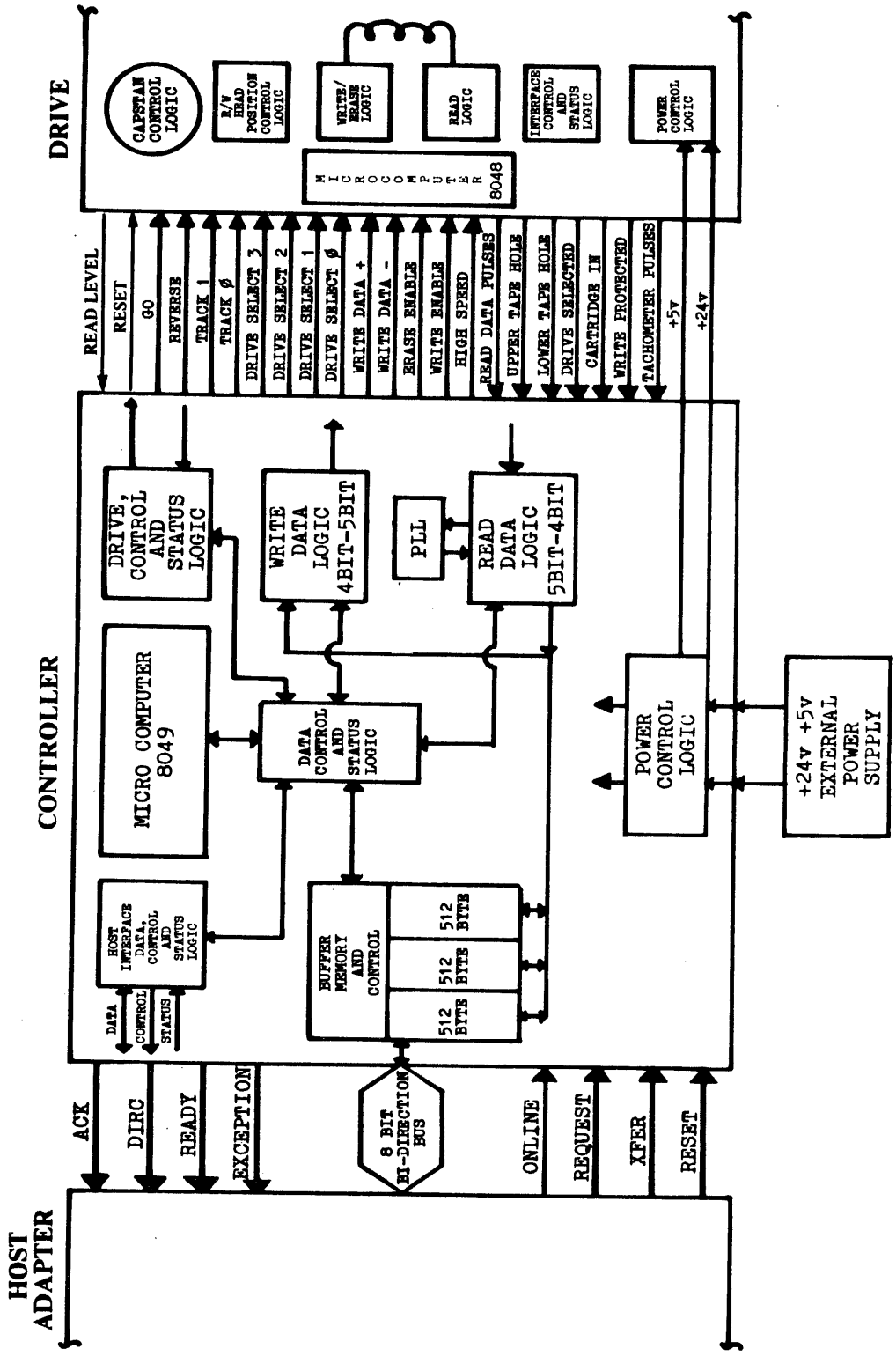


Figure 9-3. Intelligent Controller Block Diagram

9.11.1 Select Command Data

The bits in the data field of the Select command are defined as shown below.

Select Data	Bits 4 3 2 1 0
Drive 0	0 0 0 0 1
Drive 1	0 0 0 1 0
Drive 2	0 0 1 0 0
Drive 3	0 1 0 0 0
Select Light	1 0 0 0 0

The Select Light command (bit 4 true) causes the select light to stay on until the next Select command is issued with bit 4 false. This permits a number of operations to be performed sequentially without the select light going off. There are several situations that are related to the Select command that will result in the EXCEPTION signal going true.

1. The select light option was included in the last Select command and the cartridge was removed.

2. The Select command is issued with no drive specified.

3. The Select command is issued with more than one drive specified.

9.11.2 Position Command Data

The bits in the Position command data field are defined as shown below.

Position Data	Bits 4 3 2 1 0
Rewind to BOT	0 0 0 0 1
Erase Tape	0 0 0 1 0
Retension Tape	0 0 1 0 0

During execution of any Position command, the tape is moved at 90 ips. EXCEPTION will go true if the Position command is issued when a cartridge is not present in the drive. When the Position command is issued and there was no prior Select command, the command will be executed on drive 0.

9.12 5-VOLT DETECT

The 5-volt detect circuit is shown on lower, center, figure A2-4. This is a fail-safe circuit that monitors the +5 vdc to the controller. As long as the +5 vdc is greater than approximately +4.5 vdc, the collector of Q2 is low thus enabling line drivers 2B and 3B. These line drivers transfer commands to the Basic Drives. Should the +5 vdc drop enough to potentially cause erratic operation in the controller, the line drivers are disabled so that the Basic Drive will not be sent erroneous commands.

9.13 DATA BUS CIRCUITS

Since all commands from the host, write data from the host, and read data to the host are transferred by the data bus circuits, they will be described first. The data bus circuits are shown in figure A2-5. The eight data bits for each byte pass through the even numbered pins 12 through 26 of J1. Incoming data is inverted by line receivers in 2K to become HIN0 through HIN7. Outgoing data is put on the bus by tri-state line drivers in 3K. XFER- is the host transfer control signal and ACK- is the controller transfer control signal. When DIRC is low, line drivers, 3K, are enabled and a controller byte is placed on the data bus; when it is high, the line drivers are disconnected from the bus. The line receivers always respond to the data bus signals but their output is ignored when not addressed to the controller. When the incoming byte is a command, the bits are sent to multiplexers in 3E, 3F, 4E, and 4F shown in figure A2-4. When the incoming byte is data, it is changed to serial data by shift register 2H and routed to the selected buffer memory shown in figure A2-6. XFER- is received by a line receiver in 4K where it becomes XFR. XFR is inverted to XFR- and routed to OR gate, 5C, upper right corner, figure A2-4, then OR gate, 10F, to reset the READY flip-flop.

9.14 RESET CONTROL

RESET- from the host is received by the controller by line receiver, 4K, shown in the lower left corner, figure A2-4. RESET is routed through 4B to the reset input of the control microprocessor. A power-up reset is generated by 2G. Either reset will reset the controller and the Basic Drives. Within the controller this reset signal is RST and clears the READY flip-flop (6D), the interface sequencer latches (4H, figure A2-5), the write sequence latch (5K, figure A2-7), and the read latches (5H, figure A2-8).

9.15 ONLINE CONTROL

ONL- is received by a line receiver in 4K where it is inverted to set on-line latch, 4B, (2 cross-coupled NOR gates) when strobed by the microprocessor. See lower left, figure A2-4. The on-line latch will remain set until ONL- goes high which resets the on-line latch. This terminates the operation and the on-line latch may not be set again, even if ONL- goes low,

until the current operation has been completed and the Basic Drive has positioned the tape to BOT. The output of the on-line latch is connected to the T1 input to the microprocessor. The microprocessor samples this input periodically. If the latch resets during an operation, the P27 output from the microprocessor inhibits the latch from becoming set until the tape is at BOT.

9.16 REQUEST CONTROL

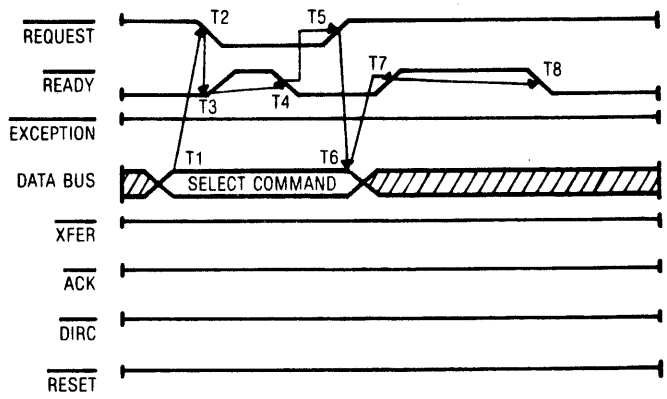
REQ- is received by line receiver, 4K, (figure A2-4) and supplied to the T0 input of the microprocessor and through gate, 7B, to reset the READY flip-flop. NAND gate 7B functions as an edge detector which generates a negative pulse of the leading edge of REQ-. REQ- is true for all command transfers and status transfers to/from the host.

9.17 COMMAND COMMON DATA FLOW (Figure A2-4)

All commands are preceded by REQ- which causes the microprocessor to issue the P20 and P21 code to select the HIN signals to the command multiplexers, 3E, 3F, 4E, and 4F. When READY- to the host goes true, the host puts the command byte on the data bus and sets REQ- true. The line receivers in 2K change the data bus bits 0 through 7 to HIN0 through HIN7. These signals are routed through the command multiplexers (this bus is selected by P20 and P21) to the microprocessor inputs P10 through P17. Bits 5, 6, and 7 contain the command type.

9.18 SELECT COMMAND DATA FLOW (Figure A2-4)

The microprocessor decodes the Select command at input signals P10 through P17. If the Select command is valid the microprocessor selects the appropriate drive by loading drive select register 3C. Figure 9-4 shows the Select command timing.



SELECT COMMAND

ACTIVITY	CRITICAL TIMING
T1-HOST COMMAND TO BUS	N/A
T2-HOST SETS REQUEST	T1→T2>Ø U sec.
T3-CONTROLLER RESETS READY	T2→T3<0.25 U sec.
T4-CONTROLLER SETS READY	50<T3→T4<500 U sec.*
T5-HOST RESETS REQUEST	T4→T5>Ø U sec.
T6-BUS DATA INVALID	T4→T6>Ø U sec.
T7-CONTROLLER RESETS READY	20<T5→T7<100 U sec.
T8-CONTROLLER SETS READY	T7→T8>20 U sec.

*NOTE: THIS TIME MAYBE >500 M SEC IF THE FOLLOWING OCCURS:
a. THE ONLINE SIGNAL IS DEASSERTED
b. RETRY SEQUENCE AND NO DATA DETECTED
c. AT END OF THE TRACK AND TURN AROUND OR START UP.

Figure 9-4. Select Command Timing Diagram

9.19 POSITION COMMAND DATA FLOW (Figure A2-4)

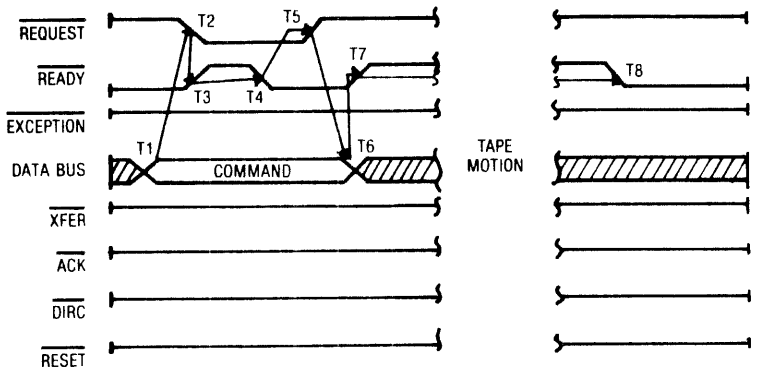
The Position commands perform the following functions:

1. BOT moves tape back to physical beginning of the tape at 90 ips (rewind).

2. Retension moves tape from BOT to EOT and rewinds back to BOT. This function is suggested by tape manufacturers when excessive read/write errors are encountered.

3. Erase turns on the erase head and erases the full tape beginning at BOT and continuing on to EOT. Upon encountering the EOT holes, the erase head is turned off and the tape is rewound to BOT.

The microprocessor decodes the Position command at input signals P10 through P17. If the command is valid the microprocessor performs the indicated function by setting the appropriate control signals in Drive Control register 2C. Figure 9-5 shows the Position command timing.



BOT, RETENSION OR ERASE COMMAND

ACTIVITY

T1-HOST BUS DATA VALID
T2-HOST SETS REQUEST
T3-CONTROLLER RESETS READY
T4-CONTROLLER SETS READY
T5-HOST RESETS REQUEST
T6-BUS DATA INVALID
T7-CONTROLLER RESETS READY
T8-CONTROLLER SETS READY

CRITICAL TIMING

N/A
T1→T2 = >Ø U sec.
T2→T3 = <0.25 U sec
20<T3→T4<500 U sec. *
T4→T5 = >Ø U sec
T4→T6>Ø U sec.
20<T5→T7<100 U sec
T7→T8 = >20 U sec

*NOTE: THIS TIME MAYBE>500 M SEC IF THE FOLLOWING OCCURS:
a. THE ONLINE SIGNAL IS DEASSERTED
b. RETRY SEQUENCE AND NO DATA DETECTED
c. AT END OF THE TRACK AND TURN AROUND OR START UP.

Figure 9-5. Position Command Timing Diagram

9.20 WRITE DATA COMMAND DATA FLOW

Writing data to tape is accomplished by:

1. Select Drive, if no Select command is issued, the unit select defaults to drive 0, track 0, BOT upon issuance of a Write command.

2. Issue Write Command with ONLINE active; if initial command, rewind tape to BOT; if the previous command was a Write File Mark, start appending the data at File Mark boundary.

3. After filling the first buffer, tape motion is started to get to recording area (past load point).

4. Start writing data to tape when the load point is encountered, meanwhile allowing data transfers from host to the remaining buffer memories.

During a Write command, one buffer memory is allocated for each of the following:

1. Data for the block of data currently being written.

2. Data for the block being read checked so that the data is available for rewriting.

3. Receiving the next block of data from the host.

Should the hosts transfer of data be inadequate to keep the buffer memories full to allow streaming, the following sequence will occur:

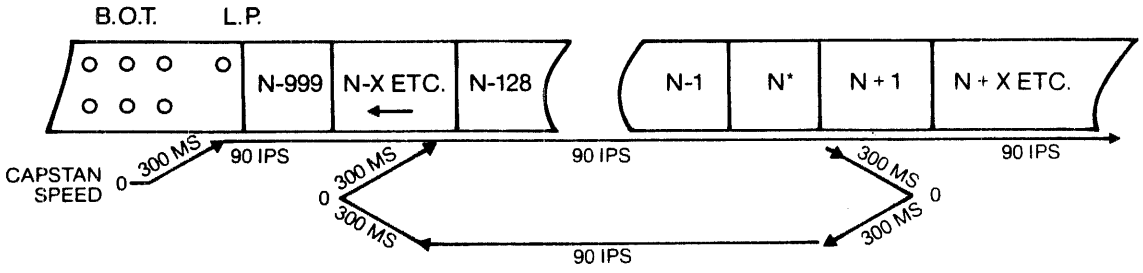
1. When the controller detects that there is no more data being transferred from the host, it will write out to tape the remaining buffers and automatically rewrite the last available block of data. This rewrite is to give the host additional time to transfer the next block to keep the tape unit streaming, and to prevent a reposition sequence. If at the end of rewriting the last block the next block transfer has not been completed, the tape unit will write an extended gap (0.3 inch plus two milliseconds) and ramp down. Once the tape unit has initiated writing an extended gap, it is committed to ramping down.

2. Upon completion of ramp down, tape motion stops ahead of the last block.

3. When the buffer is filled by the host, the drive repositions 10 blocks behind the last block. The drive reverses direction and ramps to speed. When the last block written is passed, the new data is appended to tape. Figure 9-6 defines details for the repositioning routine.

A statistical count is incremented each time the tape encounters an underrun condition. These statistics can be retrieved by executing a Read Status command.

Should the host terminate the Write command by de-activating ONLINE, or issuing a Write File Mark command, a File Mark will be written after all buffers have been written to tape. A File Mark is a unique code generated by the Intelligent Controller.



EXAMPLE: 1. RECORD N IS THE 1000TH RECORD ON TAPE
2. CAPSTAN STOPS AFTER N BECAUSE:
A. HOST TOO SLOW ON WRITE OPERATION TO KEEP TAPE STREAMING
B. HOST TOO SLOW ON READ OPERATION TO KEEP TAPE STREAMING

Figure 9-6. Write Repositioning Diagram

To ensure that the data is being written correctly, a read check is performed on each block of data immediately following the write operation. If an error is found during a read check, that block is rewritten.

Due to the gap between the read/write heads, the controller must begin writing the next block prior to the previous block being completely verified by the read-after-write check.

The sequence for read-after-write checking is as follows:

1. Begin writing block N.
2. When block N reaches the read head, begin read checking.
3. The write channel completes writing block N.
4. A short resynchronization gap is written.
5. The write channel begins writing block N + 1.
6. The read channel finishes reading block N.
7. Block N has an error.

An error encountered during a read-after-write check will initiate the following sequence:

1. The controller finishes writing block N + 1.

2. Block N is rewritten.

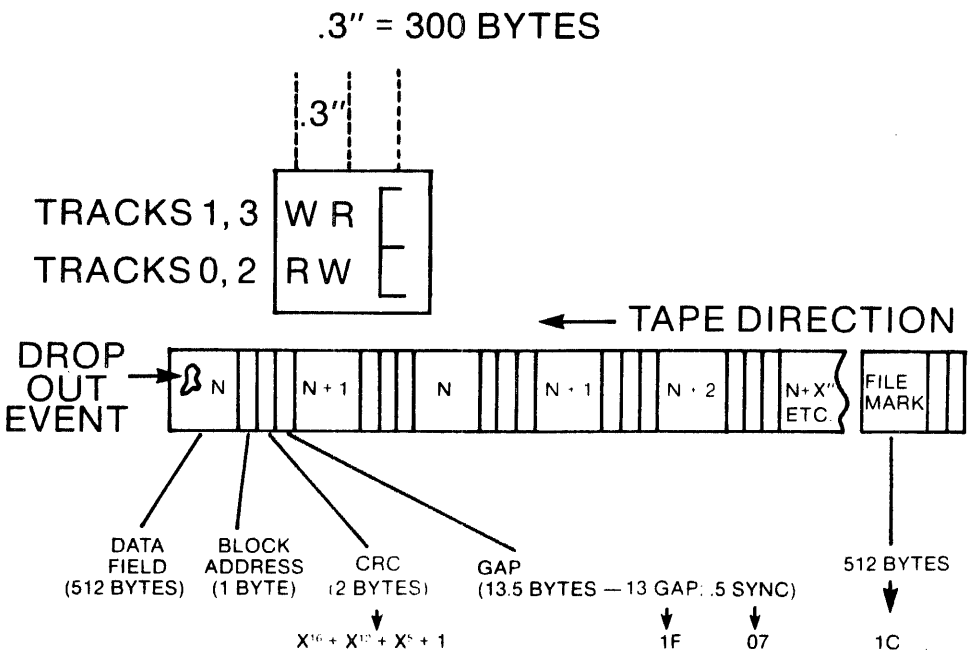
3. When block N reaches the read head, begin read checking.

4. Block N + 1 is rewritten.

5. The read channel finishes reading block N.

If block N contains an error after it is rewritten, the controller will continue to rewrite the block-in-error until no error is detected or until the limit of 16 same block rewrites occur. Figure 9-7 details this procedure.

The microprocessor decodes the Write command at input signals P10 through P17. If the command is valid the microprocessor initiates the write sequence. Buffers are assigned to the host channel and write channel as data is written to tape. Figure 9-8 shows the Write command timing.



1. Read head detects error on block N →write head at byte 287 of N + 1.
2. Hold buffer N until N + 1 written →hold buffer N + 1 and rewrite N and N + 1.
3. If new record N is good, continue on →or if still bad repeat sequence 16 times before terminating write command with unrecoverable data error status.

Figure 9-7. Read-After-Write Error Sequence Diagram

9.21 WRITE FILE MARK COMMAND DATA FLOW

The microprocessor decodes the Write File Mark command at input signals P10 through P17. If the command is valid, tape motion is initiated by setting appropriate control signals in Drive Control register, 2C. A file mark block is written on the tape and tape motion stopped. The Write File Mark timing is shown in figure 9-9.

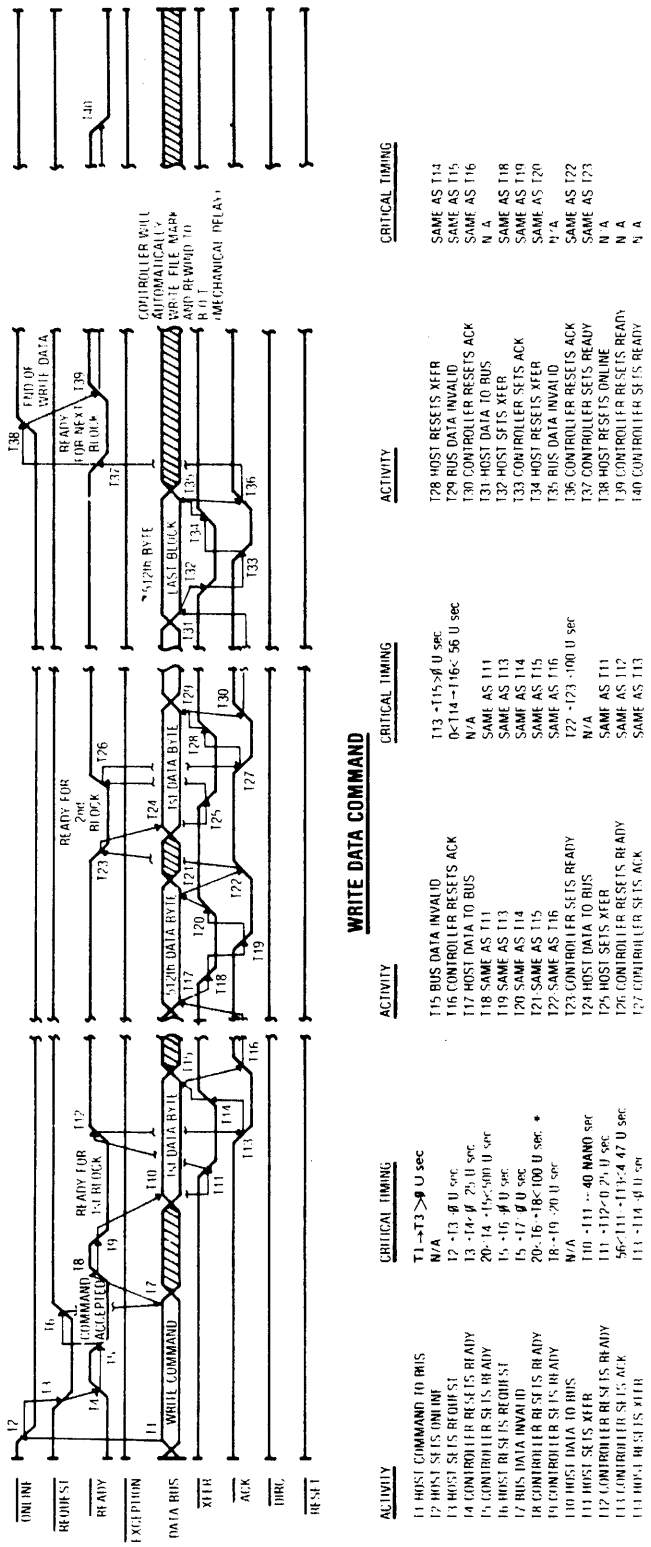
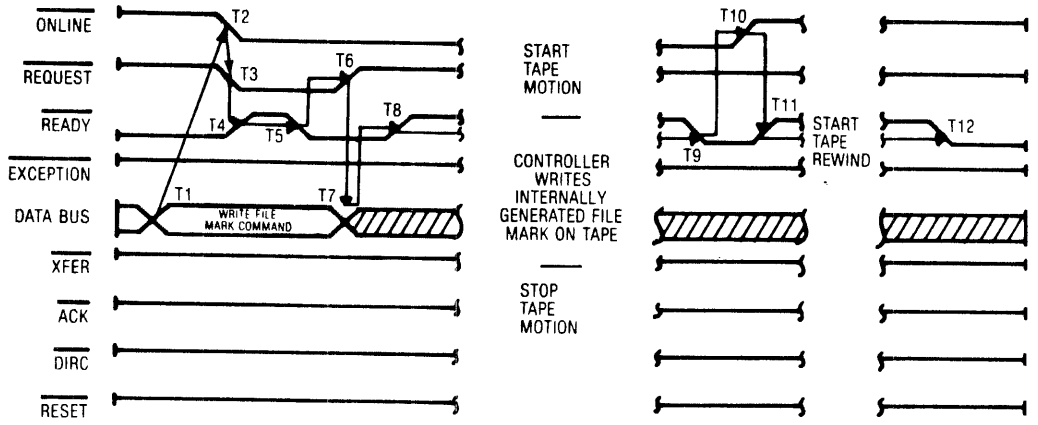


Figure 9-8. Write Data Command Timing Diagram



WRITE FILE MARK COMMAND

ACTIVITY	CRITICAL TIMING
T1-HOST COMMAND TO BUS	N/A
T2-HOST SETS ONLINE	T1→T2>Ø U sec.
T3-HOST SETS REQUEST	T2→T3>Ø U sec.
T4-CONTROLLER RESETS READY	T3→T4<0.25 U sec
T5-CONTROLLER SETS READY	20<T4→T5<500 U sec. *
T6-HOST RESETS REQUEST	T5→T6>Ø U sec
T7-BUS DATA INVALID	T5→T7>Ø U sec
T8-CONTROLLER RESETS READY	20<T6→T8<100 U sec
T9-CONTROLLER SETS READY	N/A
T10-HOST RESETS ONLINE	T9→T10>Ø U sec.
T11-CONTROLLER RESETS READY	N/A
T12-CONTROLLER SETS READY (AT B O T.)	N/A

*NOTE: THIS TIME MAYBE>500 M SEC IF THE FOLLOWING OCCURS:
a. THE ONLINE SIGNAL IS DEASSERTED
b. RETRY SEQUENCE AND NO DATA DETECTED
c. AT END OF THE TRACK AND TURN AROUND OR START UP.

Figure 9-9. Write File Mark Command Timing Diagram

9.22 READ DATA COMMAND DATA FLOW

1. Select drive, if no select command is issued, unit select defaults to drive 0, track 0, BOT upon issuance of a Read command.

2. Issued Read command with ONLINE active, the drive rewinds to BOT (if initial command) and continues after encountering File Mark (if ONLINE was active).

3. Start tape motion to get recorded data.

4. Start reading data and start filling controller buffers.

5. Start transferring data to the host when the first buffer is full (512 bytes of data).

6. Fill the remaining buffers as data is being transferred to the host.

Data read from the tape will be transferred to the host at the rate the host can accept the data.

In the read mode the three buffer memories are allocated as follows:

1. One allocated to the read channel.

2. One allocated to the host channel.

3. One is held in reserve if the host temporarily gets behind the transfer rate of the read channel.

Should the tape unit transfers overrun the host in the transfer of data being read, the tape unit will:

1. Ramp down the capstan.

2. Wait for the host to complete a block transfer.

3. Increment the internal underrun counter (which is accessible via the Read Status command).

4. Back up the tape approximately 10 blocks and reposition to the next block after the last block stored in a buffer memory.

5. Continue reading and transferring data as usual.

This sequence will continue until the host terminates the Read command by removing ONLINE, or until the controller terminates the command (at File Mark, EOM [end of media] etc.) by asserting Exception. Figure 9-6 shows detail on repositioning routine

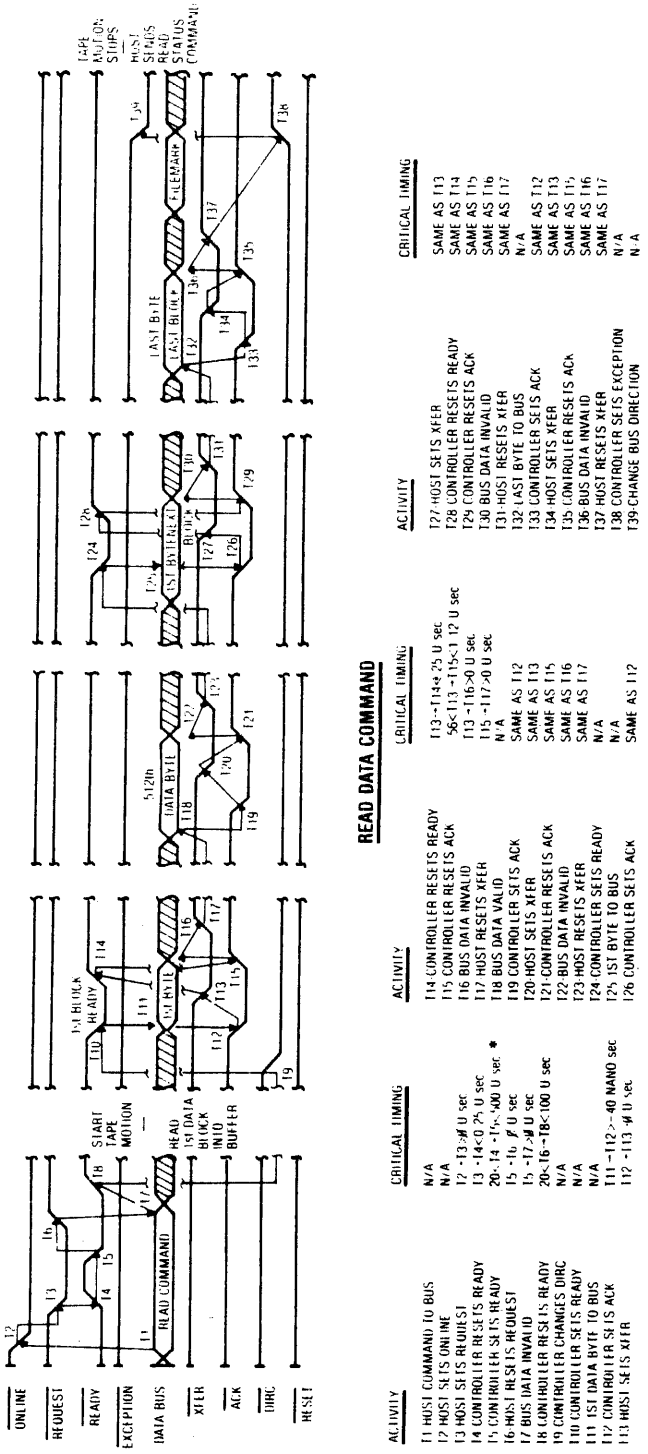
A statistical counter is incremented each time the host underruns the tape. These statistics can be retrieved by executing a Read Status command.

The microprocessor recognizes input signals P10 through P17 as the Read Data command. The sequence of events thereafter is controlled by the read logic circuits. The timing for the Read command is shown in figure 9-10.

9.23 READ FILE MARK DATA FLOW

A Read File Mark command is executed the same as a Read command, except that no data is transferred to the host. When a File Mark is detected, the Exception line will be activated which requires a Read Status command be issued prior to issuance of a subsequent command.

A Read File Mark command may be given during a read operation. This stops the flow of data to the host and the tape is advanced to the next File Mark.



ACTIVITY	CRITICAL TIMING
I1 HOST COMMAND TO BUS	N/A
I2 HOST SETS ONLINE	N/A
I3 HOST SETS REQUEST	I2 -I3>.4 U sec
I4 CONTROLLER RESETS READY	I3 -I4<0.25 U sec
I5 CONTROLLER SETS READY	20.14 -I5>.400 U sec *
I6 HOST RESETS REQUEST	I5 -I6>.4 U sec
I7 BUS DATA INVALID	I5 -I7>.4 U sec
I8 CONTROLLER RESETS READY	20.16 -I8<.100 U sec
I9 CONTROLLER CHANGES DIRC	N/A
I10 CONTROLLER SETS READY	N/A
I11 1ST DATA BYTE TO BUS	N/A
I12 CONTROLLER SETS ACK	I11 -I12>-.40 NANO sec
I13 HOST SETS XFER	I12 -I13 .4 U sec

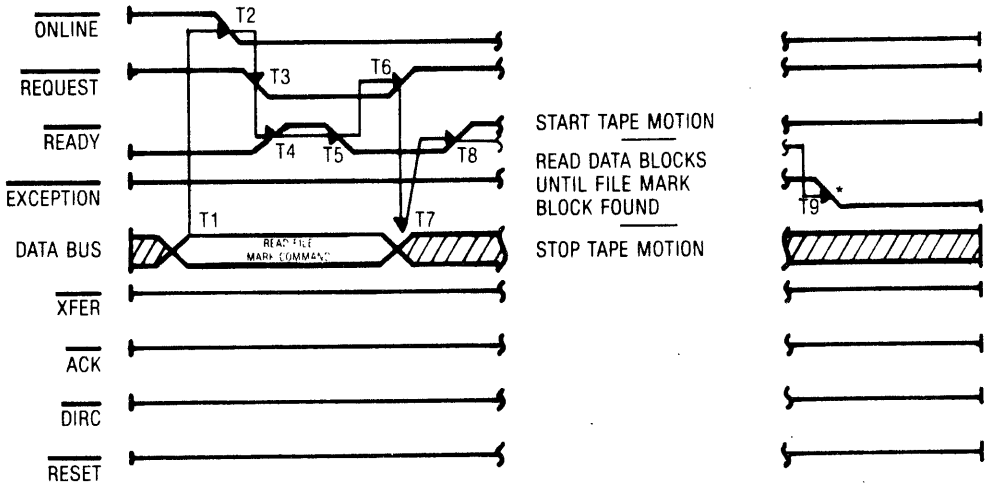
ACTIVITY	CRITICAL TIMING
I14 CONTROLLER RESETS READY	I13 -I14<.25 U sec
I15 CONTROLLER RESETS ACK	56<I13 -I15<1.12 U sec
I16 BUS DATA INVALID	I13 -I16>0 U sec
I17 HOST RESETS XFER	I15 -I17>0 U sec
I18 BUS DATA VALID	N/A
I19 CONTROLLER SETS ACK	SAME AS I12
I20 HOST SETS XFER	SAME AS I13
I21 CONTROLLER RESETS ACK	SAME AS I15
I22 BUS DATA INVALID	SAME AS I16
I23 HOST RESETS XFER	SAME AS I17
I24 CONTROLLER SETS READY	N/A
I25 1ST BYTE TO BUS	N/A
I26 CONTROLLER SETS ACK	SAME AS I12

ACTIVITY	CRITICAL TIMING
I27 HOST SETS XFER	SAME AS I13
I28 CONTROLLER RESETS READY	SAME AS I14
I29 CONTROLLER RESETS ACK	SAME AS I15
I30 BUS DATA INVALID	SAME AS I16
I31 HOST RESETS XFER	SAME AS I17
I32 LAST BYTE TO BUS	N/A
I33 CONTROLLER SETS ACK	SAME AS I12
I34 HOST SETS XFER	SAME AS I13
I35 CONTROLLER RESETS ACK	SAME AS I15
I36 BUS DATA INVALID	SAME AS I16
I37 HOST RESETS XFER	SAME AS I17
I38 CONTROLLER SETS EXCEPTION	N/A
I39 CHANGE BUS DIRECTION	N/A

Figure 9-10. Read Data Command Timing Diagram

In order to write past existing data on a tape, a Read File Mark command should be issued to get to the end of the written data. To ensure that the head is in fact over an area that has no data recorded on it, a subsequent Read command should be issued. This will cause a retry of two times and the assertion of Exception indicating "No Data Detected" and "Unrecoverable Data Error". At this point a Read Status command must be issued to clear the Exception and a subsequent Write command can be issued and data will be recorded on the tape starting at the boundary of the File Mark.

The microprocessor recognizes the Read File Mark command at P10 through P17. This command causes the drive to continue the selected drive in the current direction of travel looking for the next File Mark. When the end of a track is reached, the next track is selected and the direction of tape motion is reversed. If there is no File Mark on tape the read head will eventually find erased tape and set EXCEPTION. The timing for the Read File Mark command is shown in figure 9-11.



READ FILE MARK COMMAND

ACTIVITY	CRITICAL TIMING
T1-HOST COMMAND TO BUS	T1→T3>Ø U sec
T2-HOST SETS ONLINE	T2→T3>Ø U sec
T3-HOST SETS REQUEST	N/A
T4-CONTROLLER RESETS READY	T3→T4<0.25 U sec
T5-CONTROLLER SETS READY	20<T4→T5<500 U sec *
T6-HOST RESETS REQUEST	T5→T6> Ø U sec
T7-BUS DATA INVALID	T5→T7> Ø U sec
T8-CONTROLLER RESETS READY	20<T6→T8<100 U sec
T9-CONTROLLER SETS EXCEPTION	N/A

SYSTEM MUST ISSUE READ STATUS COMMAND

*NOTE: THIS TIME MAYBE>500 M SEC IF THE FOLLOWING OCCURS:
a. THE ONLINE SIGNAL IS DEASSERTED
b. RETRY SEQUENCE AND NO DATA DETECTED
c. AT END OF THE TRACK AND TURN AROUND OR START UP.

Figure 9-11. Read File Mark Timing Diagram

9.24 READ STATUS COMMAND DATA FLOW

A condition may occur which prevents or terminates the performance of a command. If this should happen, the controller has the ability to report to the host the cause of the condition. This is done by transmitting six status bytes to the host. Refer to figure 9-12 for Read Status command.

The controller will alert the host to a special condition by setting the EXCEPTION line to its true state. When EXCEPTION goes true, the host must respond with a Read Status command. The Read Status will cause the bytes to be transmitted to the host. The status bytes will contain the following information.

The first two bytes will define one or more conditions that caused the EXCEPTION to go true. The MSB, bit 7, will be set true if any other bit in that byte is also true. If bit 7 of either bytes 0 or 1 is not set, then no other bit in that byte will be set.

The byte 0 bits are defined at follows:

Bit 7 - Another bit in this byte is set.

Bit 6 - A tape cartridge is not in place or the cartridge was removed while the drive select light was on.

Bit 5 - The selected drive was not present when SELECT, BOT, RETENSION, ERASE, WFM, WRITE, READ or RFM was issued.

Bit 4 - A WRITE ERASE, or WFM command was given to a drive containing a write- protected cartridge. This bit stays on as long as the cartridge is write-protected.

Bit 3 - During a read or write operation, the end of the last track has been reached.

Bit 2 - An unrecoverable data error has occurred.

Bit 1 - The data transmitted to the host was not the block in error, i.e., filler data.

Bit 0 - A File Mark was detected.

The byte 1 bits are defined as follows:

Bit 7 - Another byte in this bit is set.

Bit 6 - An illegal command was sent to the controller.

Bit 5 - The controller was unable to find data on the tape. (Note: The last block that may have been sent to the host was good.)

Bit 4 - Eight or more read retries were required to recover a data block (indicative of data nearing end of life).

Bit 3 - The tape is at the beginning of media, track 0.

Bit 2 - Reserved

Bit 1 - Reserved

Bit 0 - A Power-On or reset has occurred since the last operation.

Bytes 2 and 3 contain a 16 bit binary number that is the count of the number of rewrites that occurred during a write operation or the number of blocks requiring retries that occurred during a read operation. Byte 2 contains the MSB and byte 3 contains the LSB.

Bytes 4 and 5 contain a 16 bit binary number that is the count of the number of underruns that occured during a read or write operation. Byte 4 contains the MSB and byte 5 contains the LSB.

A Read Status command will reset a status bit in bytes 0 and 1 and clear the count in bytes 2 through 5. Bits 6, 5, and 4 of byte 0 also will not change until the condition is corrected.

The microprocessor recognizes the 11Q on inputs P15, P16, P17 as the Read Status command. This command causes the controller to load six status bytes on the data bus. These bytes contain all status data collected since the beginning of the previous operation (read or write). Figure 9-12 shows the timing for the Read Status command.

9.25 HOST SEQUENCER (Figure A2-5)

The host sequencer (a PROM at 11K and latch at 11H) controls the flow of data to and from the host. The direction of data flow is dictated by the state of DIRC from 10H, pin 8 (figure A2-4). DIRC is true (high) for a read operation (data going to host) and false for a write operation (data coming from host). The outputs of the sequencer in the idle state is 1111 (all outputs false). The host sequencer output from the most to least significant are: DONE-, ST3 (STMEM-), ST2 (LDAT-), and ST1 (SACK-). DONE- means just that; the operation is done. STMEM- means start memory. LDAT- means load data and SACK- means set acknowledge. The sequencer is started by a control word on the internal bus that came from the 8049. This control word is clocked into the latch at 4H by LDHOST- on pin 9. During a read transfer the host sequencer cycles through states 1001, 1101, and 1100 for 512 times then after the transfer of the 512th byte, sequences to 0111 and then 1111 (idle again). During a write operation the host sequencer cycles through states 1101, 1010, 1110 and to 1111 if the next byte is not available from the host or to 1101 if it is. After receipt of the 512th byte, the host sequencer goes to 0111 and then 1111.

9.25.1 Read Sequencing

The control word from the internal bus sets HCMP (4H, pin 3) false and selects one of the read buffers (figure A2-6) by setting one of the buffer latches in 4H. As HCMP goes false the sequencer goes to 1001. STMEM- enables the host clock, HCLK-, at 5F, pin 13 to increment the buffer address with HINCAD-. HINCAD- also goes to clock input at 3G, pin 10 and 3H, pin 10. Data is clocked into shift registers, 3G and 3H on pins 3. The sequencer goes to state 1101 when this counter indicates a byte has been transferred. Each time STMEM- goes true, the 4040 counter, 6F, is incremented. The next state of the sequencer is determined by XFER-. XFER- false indicates that the byte is on the bus. When XFER- goes false, the sequencer advances to state 1100. The resulting true SACK- becomes the ACK- signal at J1-36 and informs the host that a byte is ready. This cycle is repeated 512 times and on the 512th byte (as indicated by the byte counter at 6F), the sequencer advances to state 0111. DONE- clears the latch at 4H on pin 1 (figure A2-5) causing HCMP to go true and the sequencer resets to the idle state (1111).

9.25.2 Write Sequencing

The control word from the internal bus sets HCMP false as in read sequencing, but this time the host sequencer stays in the 1111 state until XFER- goes true at J1-34. XFER- true means the host byte is on the bus and the sequencer advances to state 1101 (LDAT- is true). A true LDAT- to the shift register at 2H, pin 15 (figure A2-5) loads the byte from the bus and removes the clock inhibit from pin 6 so HCLK- on 2H, pin 7 may clock data in. After one HCLK- cycle the sequencer advances to state 1010. In this state STMEM- enables the gate at 5F, pin 13 so HINCAD- increments the buffer address and remove the clock inhibit at 2H, pin 6 so the byte is shifted out. The shift register output (2H, pin 13) is host data in (HDIN) and goes to the buffers shown on figure A2-5. STMEM- becomes HWTMEM- at 5F, pin 8. HWTMEM- strobes data into the buffer. STMEM also clocks the byte counter (6F). SACK- becomes ACK- to the host signifying that the byte has been read. If XFER- remains true, the sequencer stays in state 1010 until BYTERDY from 10G, pin 8 (bit counter) goes true and then advances to state 1110. When XFER- finally false the sequencer advances to idle (1111). If XFER- goes false before the byte is stored in the buffer, the sequencer advances to state 1101 until BYTERDY goes true. In this case, the next state of the host sequencer will be determined by one of the following conditions:

1. This was the 512th byte so the next state is 0111, DONE-.

2. This was not the 512th byte and XFER- is still false so the next state is 1111, idle.

3. This was not the 512th byte but XFER- has gone true again so the next state is 1101; start processing the next byte.

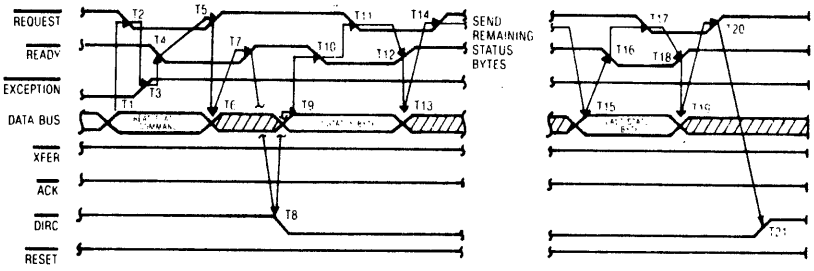
After the 512th byte, DONE- clears the latch at 4H on pin 1 and HCMP is true.

9.26 BUFFER MEMORIES DATA FLOW

The three buffer memories are used in both read and write operations. During the write opeation data is converted from parallel eight-bit bytes to serial bit streams, stored in the memory buffers, one buffer at a time, and transferred out to the write circuits in blocks by buffer. Addressing of the RAM buffer memories is controlled by a buffer address counter for each of the three buffers.

9.26.1 Buffer Address Counters

Each buffer stores 512 bytes (4096 bits) of data which becomes a block of data on the tape. At the beginning of each block transfer, either into or out of a buffer, RSTAD is gated to reset the appropriate buffer address counter to zero. The counters (9G and 10G, 9H and 10K, 9K and 10K, figure A2-6) are incremented by HINCAD during loading of data from the host, by WINDCAD during a write operation, and by RINC during a read operation.



READ STATUS COMMAND

ACTIVITY	CRITICAL TIMING
T1-HOST COMMAND TO BUS	N/A
T2-HOST SETS REQUEST	T1→T2>0 U sec
T3-CONTROLLER RESETS EXCEPTION	T3→T4>10 U sec
T4-CONTROLLER SETS READY	20<T2→T4<500 U sec *
T5-HOST RESETS REQUEST	T4→T5>0 U sec
T6-BUS DATA INVALID	T4→T6>0 U sec
T7-CONTROLLER RESETS READY	20<T5→T7<100 U sec
T8-CONTROLLER CHANGES BUS DIRECTION	N/A
T9-1ST STATUS BYTE TO BUS	T9→T10>0 U sec.
T10-CONTROLLER SETS READY	T7→T10>20 U sec.
T11-HOST SETS REQUEST	T10→T11>0 U sec.
T12-CONTROLLER RESETS READY	T11→T12<0.25 U sec.
T13-BUS DATA INVALID	T11→T13>0 U sec.
T14-HOST RESETS REQUEST	T11→T14>20 U sec.
T15-LAST STATUS BYTE TO BUS	N/A
T16-SAME AS T10	SAME AS T10
T17-SAME AS T11	SAME AS T11
T18-SAME AS T12	SAME AS T12
T19-SAME AS T13	SAME AS T13
T20-SAME AS T14	SAME AS T14
T21-CONTROLLER CHANGES BUS DIRECTION	N/A

*NOTE: THIS TIME MAYBE>500 M SEC IF THE FOLLOWING OCCURS:
a. THE ONLINE SIGNAL IS DEASSERTED
b. RETRY SEQUENCE AND NO DATA DETECTED
c. AT END OF THE TRACK AND TURN AROUND OR START UP.

Figure 9-12. Read Status Command Timing Diagram

9.26.2 Write Operation Data Flow

The eight-bit parallel transmission from the host passes through the line receivers, 2K, to the shift register, 2H (figure A2-5). The serial write data, HDIN, is shifted out by LDAT from the interface sequencer, 11H and 11K, and inverted twice in 12K. HDIN is routed to RAM drivers, 6G, 6H, 6K, (figure A2-6). The RAM driver for the memory being loaded is enabled by 1HST or 2HST or 3HST from the microprocessor. HWTMEM strobes the input to the selected RAM, HINCAD advances the address counter, and each bit is loaded sequentially. When one buffer is full, the next is enabled and loaded. After a buffer memory is filled, it is ready to be written to tape. The buffer is unloaded by resetting its address counter and enabling the appropriate RAM driver with 1WT or 2WT or 3WT. As the counter counts up from zero, the output bit from each memory location is transferred out as WDATA.

9.26.3 Read Operation Data Flow

During the read operation, the serial read data, RDATA, is routed to the appropriate buffer by 1RD or 2RD or 3RD (figure A2-6). The buffer memory address counters are advanced by RINC which also strobes the input to the RAM. Each block on the tape should fill a buffer. After a buffer is filled, the CRC check is made and the filling of the next buffer is started. A successful CRC check permits tranferring the buffer content to the host. Again the appropriate buffer is enabled by 1HST or 2HST or 3HST and the buffer address counter is reset. The output of the selected buffer is HOUT. HOUT is routed to the serial-to-parallel shift register, 3G, and 3H (figure A2-5). When eight bits have been shifted into the register, they are transferred to the output data drivers, 3K.

9.27 THE WRITE LOGIC DATA FLOW (Figure A2-7)

The write logic consists of two groups of circuits: a) In the lower right hand corner is the circuit which generates the write clock and host clock. b) The remainder of the page is a write sequencer.

The clock circuit consists of a crystal and three dividers. The first is a latch at 12H (74LS74) which divides the frequency by two to produce the Host Clock, HCKL-. Immediately above the first latch is a divide-by-three circuit. This circuit consists of the NAND gate at 13F and the two latches at 12F (74LS74). The output of this circuit on pin 8 of 12F is one-third the frequency of the crystal. This circuit is present only on controllers designed for 30 ips drives and the component at 12F is not present on a 90 ips drive. There is a jumper to by-pass this circuit below and to the right of 12F. The final circuit is the divide-by-four at location 12G. On a 30 ips drive, the final frequency out is one-twelfth the frequency of the crystal. On a 90 ips drive, the final frequency out is one-fourth the crystal. The output of 12G pin 8 is Write Clock, WCLK-. Write Clock is used to generate two other clocks, the Nibble Clock, NIBCLK, and the Data Shift Register Clock Pulse, DSRCP-. Data is handled in a bit serial stream and it must travel in two forms: a) The user data as it comes across the

interface in eight bit bytes or four bit nibbles. b) As encoded data to be written to tape. ARCHIVE uses a 4-to-5 code to limit the number of consecutive zeros in the data stream. In the encoded form, bytes are 10 bits long and nibbles are 5 bits long. Both forms of data must be handled in synchronization with each other. Because of this, two clocks are needed; one with five bits per nibble and one with four bits per nibble. The first clock is WCLK- which has five positive transitions per nibble time. WCLK is used to create NIBCLK by using the synchronous counter at 13D. This is a four bit counter. The output of the third bit, pin 12, is tied back to the clear of the counter, pin 1. On the next positive transition of WCLK- the counter clears itself. The result is NIBCLK, which has one positive going transition for every five WCLK-. NIBCLK is used to define nibble boundaries. The last clock to be created is DSCRP-. This is done by NANDing NIBCLK with WCLK- at 5F to cancel one positive transition per nibble item. DSCRP- now has four positive transitions per nibble boundary and can be used to clock unencoded data. The remainder of the page is the write sequencer which will step through one of two possible sequences of states. They are state 0, 1, 2, 4, 5 and 7 or 0, 1, 3, 4, 5, and 7.

State 0: Gap Write - write 13 bytes of gap.

State 1: Synce Write - write 0.5 bytes of gap

State 2: Data Write - write 512 bytes of user data.
or
State 3: File Mark Write - write File Mark pattern.

State 4: Block Address Write - write 1 byte of block address.

State 5: CRC Write - write 2 bytes of CRC character.

State 6: Not used.

State 7: Write Done - clear the sequencer and return to state 0.

The sequencer consists of the PROM at 9F, the latch at 9E (74LS174) and the decoder at 10E (74LS138). The inputs to the PROM are four bits of a twelve bit counter at 8F (4040) and a signal called Write File Mark, WFM. The latch at 9E is held clear by WCMP in its true state and is clocked by NIBCLK-. This sequencer has three store bits and seven possible states. When the sequencer is not in use, it is held in state 0 by the WCMP signal. To start the sequencer, the 8049 places a control word on the internal bus. This word uses bits 2, 3, 4 and 5 to do two things: a) One bit of 2, 3 or 4 is set. At the output of the latch at 5K, this will become 1WT-, 2WT-, or 3WT-, and connect the write sequencer to an appropriate buffer. b) Bus bit 5 will take WCMP false, allowing the sequencer to cycle. These bits will be loaded into 5K by the signal LDWRT- which was generated by bits 6 and 7 of the control word going into the demultiplexer at 11G (figure A2-4). Before the sequencer was started, Write Enable (WEN) went true removing the pre-set condition from the J-K flip-flop at 13E (74LS109) which was holding the counter at 8F reset. Pin 11 of 8F is high active. The next WCLK at the clear input at 13E (pin 15) will cause pin 10 of

13E to go low, allowing the counter 8F to cycle. The counter will be clocked by NIBCLK, so it will count in nibble increments.

As the tape comes up to speed, the 8049 begins looking for the load point hole, the write circuit is held in state 0, writing a long continuous gap signal to tape (state 0). Gap is written when the sequencer is in state 0 and WEN is true. In state 0 or Gap Write, GAPW-, pin 15 of 10E (74LS138) is true. The GAPW- signal goes through the OR gate 13F to the output disable of the tri-state PROM at 13H, pin 15. The pull-up resistors R37 through R41 cause all ones to be loaded by NIBCLK- into the shift register at 13G (74LS166). The all ones pattern is clocked by WCLK- out of the register to the J-K flip-flop at 13E which is clocked to the Basic Drive as NRZ data. When load point is detected, the write sequencer is released by WCMP going false. On the next 32 nibble count from 8F, pin 2, the sequencer goes to state 1, Sync Write (SYNCW-). Pin 14 of 10E goes true for state 1. The SYNCW- signal has three functions:

1. Clears the CRC generator at pin 2, 11E and holds it clear until state 2 (DATAW-).

2. As did GAPW-, it disables the output of the tri-state PROM at pin 15, 13H and enables the two NAND gates at 13F. This causes a 07 hex pattern (Sync Mark) to be loaded into 13G.

3. Reset the counter at 8F by clocking the J-K flip-flop at 13F, pin 12. The sequencer will stay in SYNCW- for one nibble clock and move on to the next state upon completion.

In state 2, pin 13, 10E, goes low, enabling the negative input NAND gate at 11F, pin 2. This allows data to flow out on pin 3 of 11F through the NOR gate 10F, at pin 3. Data is clocked out of the buffers by WINCAD-. WINCAD- is DATAW- and DSRCP-. DSRCP- is also clocking the CRC as it samples the data. The data is clocked into the shift register at 13K. The outputs of this register are always enabled. The four bit nibble goes to four of the five address lines of the PROM. The fifth line is high. These four bit data nibbles address locations which contain their corresponding five bit code. The outputs of the PROM are enabled and loaded into the shift register at 13G on nibble boundaries by NIBCLK-. The five bit code is then clocked out to the write circuits while another four bits are clocked into 13K. In state 3, File Mark Write (FMW-), the sequencer will write a File Mark because WCMP will go false, but no buffer will be assigned on bus bits 2, 3 or 4. The AND gate at 10F, is enabled. Pin 12, 10F, is WFM. In state 3, WFM goes low. FMW- goes directly to pin 14 of the PROM at 13H. Regardless of what signals appear on the other address inputs of 13H, only the lower 16 locations are addressed. All 16 locations contain the pattern for a File Mark. During a File Mark Write, the controller will generate 512 bytes of Hex 1C for the data field. The write sequencer will stay in either Data Write state or File Mark Write state for 1024 nibbles (512 bytes). When pin 15 of the counter at 8F goes true, the sequencer will move to state 4.

In state 4, pin 11, 10E, goes true. WADR- goes to pin 4 of 11F, enabling the contents of the shift register at 4C to be shifted into the data stream through the OR gate at 10F. WADR- also takes the clock enable true for the shift register at 4C, pin 6. The block address was loaded into the shift register before it is needed by 8049. The 8049 assigns the block number to each data block and places it on the 8 bit internal bus. It is loaded into the shift register by LDBADR-. The two latches, 6C, (figure A2-4) ensure that LDBADR- is present on a clock edge of DSRCP- to load the register at 4C. The sequencer remains in state 4 for two nibbles, appending a block address to the data field.

In state 5, pin 10, 10E, goes true. CRCW- enables the NAND gate at pin 10, 11F, allowing the CRC character to join the data stream. CRCW- also goes to pin 10, 11E, the CRC generator. Until now, the 9401 had been sampling the data stream and maintaining a check character. The CRC character includes both data and the block address. When pin 10, 11E, goes low, the 9401 stops sampling the data and begins shifting the 16 bit check character out on pin 12. The clock used here is DSCRP- with four bits per nibble. The sequencer will stay in CRCW- for four nibbles and then move to state 7.

State 6 is not used.

In state 7, pin 7, 10E, goes true, the signal goes to the clear input of the latch at 5K, pin 1. When this latch is cleared, the buffer assignment on its output goes false and the buffer is disconnected from the sequencer. WCMP goes true, clearing the latch at pin 1, 9E. When 9E is cleared, the sequencer is forced to state 0 and will remain there until it is started again by the 8049. A reset pulse at pin 9, 5G, will disconnect the sequencer from its buffer and force the sequencer back to state 0. The last circuit is the AND gate at 4B for TP9. Write Pulse is available at TP9 for viewing on a scope.

9.28 READ LOGIC DATA FLOW (Figure A2-8)

The read logic contains three groups of logic:

1. The gap and no-data detect circuits.

2. The read sequencer.

3. The Phase Locked Loop.

The gap and no-data detect circuits consist of one-shots and a latch across the top of figure A2-8. The data enters the controller at J3-26 as Read Data Pulses, RDP-. The pin shown above RDP- is Read Level, RDL-; it is not used by the controller. RDP- goes from J3-26 to pin 4 of the one-shot at 12B (9602). The one-shot at 12B is set to generate a square wave that will be 0.7 of a bit cell wide. The output of the first one-shot is fed to the input of the second one-shot at pin 12, 13B. The output of the second one-shot is timed to 1.33 bit cells. Its output is tied to the negative edge triggered input to the last one-shot in the chain. Any zero, or absence of a data pulse, entering this chain

will cause the third one-shot to retrigger. The third one-shot is set for 12 bit cell times. The only stream of bits that will allow the last one-shot to time out and stay timed out, is a gap signal. The output at pin 9, 12B, is fed to the input of a latch at pin 12, 12H, that is triggered every bit cell time. If pin 9, 12B, goes high, the signal GAP detected is generated and fed to the read sequencer. It is also available to the 8049 on its Port 1 inputs. The no-data detect circuit is the one-shot in 13B. It is set for 4 bit cell times. Since no more than two zeroes can ever appear in our 4-to-5 run-length limited code, this one-shot should always remain retriggered. Its output is called No Data Detected, NDTADET and goes to an input in the read sequencer.

9.28.1 The Phase Locked Loop And Data Separator

When data is read from magnetic tape moving across a read head, even a signal which was written at constant frequency will vary in frequency as it is read. This is due primarily to mechanical properties of the tape. When NRZ data is read from tape, it is necessary to identify where data bits should be. To do this, a bit cell window is needed. This window must be able to shift to some degree to follow the variation in tape speed and data frequency. The circuit which will produce a clock to define a bit cell window is the phase locked loop. The phase locked loop will track the frequency of data as it is read from the tape and identify where the next bit should be. Data enters the PLL from pin 6, 7A. At first, this signal is fed to the 4044 at pin 1, 8E. The 4044 will compare the phase and frequency of the data coming in to the phase and frequency of the clock that the PLL is producing. If the PLL signal is faster than the input signal, the 4044 will output a signal on pin 2. This signal will go into a filter. The output of the filter will cause the control voltage going to pin 15 of the voltage controlled oscillator (VCO) at 12A to be lowered. It produces a signal on pin 10 whose frequency can be increased or decreased by increasing or decreasing the voltage on pin 15. The VCO signal is divided by 32 and becomes the clock produced by the PLL. The clock is constantly compared on pin 3, 8E to the data stream and is adjusted to match it. If the PLL is slower than the input, the 4044 will output a signal on pin 13, causing the VCO to speed up. In this phase locked loop, two different comparison circuits are used:

1. The 4044 is used only when reading gap because it compares both phase and frequency. Gap is a constant-frequency signal of all ones.

2. For data fields, a circuit is used to track where the ones are in relation to where they should be. Data field frequency will vary depending on the number of ones and zeroes.

   a. If they are early, the VCO speeds up.

   b. If they are late, the VCO slows down.

The read sequencer controls which comparison circuit is used by placing a signal on pin 12 of the gates at 9B (figure A2-4): a) If a high is present, the 4044 is used. b) If a low is present, the sample and hold circuit is used. Both

comparison circuits apply voltage to the VCO through a filter which determines how quickly the VCO will respond to: a) variations in frequency; b) range of frequencies it can track. After the 4044 has adjusted the VCO at 12A to the correct frequency during gap, the read sequencer disables its output and enables the second comparison circuit. The second comparison circuit generates a digital signal which is converted to a voltage and applied to the filter. The Read Data Pulse (RDP-) goes to a latch at 7F. A "one" will clock the latch and pin 5, 7F will go high. The output of pin 5, 7F goes to the input of pin 12, 7F. When the next positive going edge of the VCO output occurs, the output of pin 9, 7F goes high. The output is tied back to the clear of pin 1, 7F. For every "one" in the data stream, this circuit produces a short pulse synchronized with the VCO. The pulse goes to 8C. The other input to this gate is the VCO output. The output of pin 11, 8C goes to the clock of five latches at pin 9, 8B. When a data pulse occurs, some five-bit digital value is clocked in 8B on pins 14, 13, 11, 6 and 4. The digital value is created by the five bit counter above it. The counter consists of the latch, 7D (74LS74) and the synchronous counter (74LS163) at 8D. The counter is clocked by the output of the VCO. The counter will count from 0 to 31 in 1 bit-cell time. If a data pulse occurs early, the count will be low. If the data pulse occurs late, the count will be high. When the pulse does occur, that count is latched into 8B and appears on its outputs of pins 15, 12, 10, 7 and 5. The digital value is converted to voltage by the resistor network below the gates at 9B (CD4502). This voltage is fed back to the VCO and is kept until another data pulse appears. Because 4-to-5 code is used to write data, the sample and hold circuit will never see more than two zeroes between data pulses. A sample is guaranteed at least every 3 bits. Until now, the data has been in the form of read data pulse. It needs to be translated to properly synchronize data levels. This is done by the latch at 6D (74LS74). The data pulse from the output of pin 9, 7F goes through 8C to the pre-set at pin 10, 6D. Each data pulse will set the latch for 1 bit-cell time. The bit-cell time is defined by the read clock pulse (the output of the PLL from pin 11 of the counter at 8D). This same clock will be the read clock of the read sequencer and will be in sync with the data coming from pin 9, 6D. If a data pulse does not occur during a bit cell, the low input on pin 12, 6D will be clocked through. To the left of 6D is another latch, 7D (74LS74). During a read-only operation, this latch is held pre-set by Write Enable. The output of pin 5, 7D enables pin 5, 8C allowing the data pulses to pass through. During a read-after-write operation, WEN is true, no longer holding the latch pre-set. The outputs of pins 11 and 12 of 8D are fed through the NAND gate at 8C, pins 1 and 2. The output of 8C, pin 3 goes to the input of the latch at pin 2, 7D. This input is clocked by the output of pin 13, 8D. The result is that pin 5, 7D is only high for the center 75 percent of each bit-cell window. 8C is only enabled during this time. This reduced bit-cell window is used during the read-after-write operation to ensure that any data bit is properly written on the tape and will be well within the full bit-cell window during a read-only operation. The final products of the phase locked loop and data separator are a read clock pulse from pin 11, 8D and a data stream from pin 9, 6D.

9.28.2 Read Sequencer

The sources of clock signals for the read sequencer differ from the write sequencer. The sequencer must follow the actual frequency of data as it is read from the tape. The source of the clock which will follow a varying frequency is the phase locked loop. The signal which will be the read clock for the read sequencer is output on pin 11 of the synchronous counter 8D (figure A2-8). It will function in this sequencer as WCLK- did in the write sequencer, clocking 5 bits per nibble data. The other two clocks of the write logic also have counterparts in the read logic. To define nibble boundaries Read Nibble Clock, RNIB-, is generated by the synchronous counter (74LS163) pin 12, 9D as NIBCLK- was in the write sequencer. The third clock which will handle the 4 bit per nibble data is Read Shift Register clock, RDSR-. As in the write logic, this clock is created by NANDing RNIB- with the read clock signal at 11D, pins 4 and 5.

The read sequencer consists of the PROM at 10B, the latch at 10C and the decoder at 11C. The inputs to the PROM are five input signals and four state bits. Only the three most significant bits are input to the decoder. This sequencer will begin to cycle any time gap is detected. It is not held by any control signal from the microprocessor. It is clocked by Read Nibble, RNIB-. The states of the read sequencer are:

0	Idle (IDLE-)
2	Read Lock (RLOCK-)
4	Lock - no signal
6	Expect Read Sync (ERSYNC-)
5	Stall one nibble - no signal
9	Data (DATA-)
A+B	Block Address Read (ADDR-)
C+D	Read CRC 1 - no signal
E+F	Read CRC 2 (RCRC2-)

The read sequencer remains in state 0 (IDLE) until the output of the gap detect circuit goes true. Pin 15, 11C is low when the sequencer is in state 0. IDLE- goes to AND gates 7A, pins 4 and 3. While the sequencer is in state 0, the phase locked loop will be synchronizing for phase and frequency to the Write Clock, WCLK-, through the lower AND gate of 7A, pin 2. The write clock is the nominal frequency at which the read logic expects to see the data. By synchronizing to this frequency, the phase locked loop will be close to the correct frequency when the actual data enters the circuit. Note that the least significant state bit (LST0) going to pin 3, 10B does not go to the decoder at 11C (74LS138). This sequencer has 16 states, but only six become signals on the outputs of 11C and not all states are used.

When GAP goes true, the sequencer will move to state 2 Read Lock (RLOCK-). In state 2, pin 14, 11C goes low and pin 15 goes high. When IDLE- goes high, it enables the upper AND gate at 7A, causing the phase locked loop to synchronize on gap signal for frequency and phase. RLOCK- goes to two gates at 11D and 5C. The output of pin 11, 11D resets the counter at pin 11, 13C. The output of pin 11, 5C clears the latch at pin 1, 11B. RLOCK- will only stay true for one nibble. On

the next RNIB- clock, the sequencer moves either to state 4, if GAP is true and NDTADET is false, or back to state 0, if GAP is false or NDTADET is true.

In state 4, pin 13, 11C is low. This pin is not used. During state 4, the phase locked loop circuit is synchronizing to the gap signal on the tape for both phase and frequency. This state will last for eight bytes. When pin 3 of the counter at 13C goes high, it will clock the latch at pin 3, 11B, so the output on pin 5, 11B will go high. The output is the signal LOCK, which is an input to the sequencer. The Q- output of the latch at pin 6, 11B will go to the tri-state drivers at pin 12, 9B. This will cause the phase locked loop to begin tracking on phase only. After 8 bytes or 16 nibbles if GAP is true and NDTADET is false, the sequencer will move to state 6, EXPECT READ SYNC (ERSYNC). If Gap is false or NDTADET is true, the sequencer will return to state 0.

In state 6, ERSYNC-, pin 12 of the decoder 11C is low. This signal goes to 11D, pin 2. The other input to 11D on pin 1 is from pin 7 of the PROM at 6E. This pin will go high only when its input on pins 10, 11, 12, 13 and 14 is a Sync Mark. As data is shifted into the register at 5E (LS164), its outputs are constantly changing. The NAND gate at 11D will only be enabled immediately following gap, therefore, the circuit cannot mistakenly read a Sync Mark from a shifting data field. After seeing a Sync Mark, the gate will be disabled. The output of pin 3, 11D will only be true for 1 bit-cell time. This signal is Sync Read (SYNCR-). SYNCR- will reset the RNIB- counter at 9D and also clock the sequencer latch at 10C. This synchronizes the nibble clock, RNIB- and the state sequencer to the nibble boundaries of data on the tape. Pin 7 of the PROM at 6E is also an input to the read sequencer on pin 6 of the PROM 10B. When this input goes high the sequencer moves to state 5.

When the sequencer is in state 5 (stall one nibble), pin 13, 11C is low. This pin is not used. The sequencer will stay in state 5 for 1 nibble time while the first nibble of data is being shifted into the register at 5E, pins 1 and 2. If Gap goes false or NDTADET goes true during state 5, the sequencer will return to state 0. If Gap remains true and NDTADET remains false, the sequencer will go to state 9.

In state 9 (DATA), pin 11, 11C goes low. This is DATA- state. If GAP goes false or NDTADET goes true after the sequencer enters state 9, the sequencer will jump forward to state F, causing a CRC error. The signal from pin 11, 11C (DATA-) goes to pin 12, 12C (74LS32). Its other input is RDSR-. RDSR- and DATA- form Read Increment Memory (RINC-) which goes to the buffer memories. RINC- will increment the buffer address of the buffer being used to process this block of data. The data enters the sequencer from the output of the latch at pin 9, 6D. The data is shifted into the register at 5E (74LS164), pins 1 and 2. The outputs of the register are always enabled. These outputs go to the address lines of the PROM at pins 10 through 14, 6E. At each nibble boundary, the five bit code will be present to address a location which contains the corresponding 4 bits of decoded data. This circuit decodes the run-length-limited code that the similar circuit in the write sequencer created. The decoded data will be loaded into the shift register (74LS166) at 7E, on pins 10, 11, 12 and 14, on nibble boundaries by RNIB-. The data will then be shifted out by the read clock pulse. The read

clock pulse has five transitions per nibble. Four transitions will clock the data out of pin 13, 7E to one of three gates (7G pin 6, 7H pin 6, or 6K pin 12) feeding the buffers (figure A2-6). The sequencer will remain in state 9 until pin 15 of the counter, 13C, goes high indicating 1024 nibbles have been read.

From state 9, the sequencer goes to state A (block address read). In state A, pin 10, 11C goes low, enabling the gate at pin 1, 12C. This will allow RDSR- (four transitions per nibble) to clock the block address into the read block address register (74LS164) at pin 8, 4D. Pin 10, 11C, is address state (ADDR-) and will remain true for both states A and B in two nibble times or 1 byte, just long enough to clock block address into 4D. The outputs of 4D are the read block address bus (RB), which can be read by the 8049. RB enters 8D, figure A2-4.

The sequencer will step into state C (read CRC on) the RNIB- clock. In states C and D, pin 9, 11C is low, but pin 9 is not connected to anything. The sequencer will take two nibble times to step through to states C and D to state E. In state E, pin 7, 11C goes low.

The signal on pin 7 goes to latch at 12D (figure A2-8) and through NOR gate pin 12, 5G to the clear of the latches (74LS175) at pin 1, 5H (figure A2-4). 5H will go clear, disconnecting the buffer and setting RCMP false. In the read sequencer, RCMP going false does not stop the sequencer. The latch at 12D will not clock until pin 7, 11C goes high. It will take two nibble times to step through states E and F. The sequencer will leave state F four nibble times after it entered state C. This is the length of the CRC character. When the sequencer entered state 9, the most significant state bit (LST3) went high. This enabled the 9401 at pin 11, 13A to be sampling the data, the block address, and the CRC character for this block. When it has sampled the last bit of the CRC character, its output on pin 13 should be low. As the read sequencer leaves state F, pin 7, 11C goes high. In the transition to high, it clocks the state of the 9401 at pin 13, 13A into the latch at pin 12, 12D. The output of the latch goes to Port 1 of the 8048 via pin 3, 4E. By sampling Port 1, the 8049 can detect CRC errors.

There are three remaining circuits in the read sequencer.

1. The first is the File Mark detect circuit. If the unique code for a File Mark is placed on the address lines of the PROM at 6E, pins 10 through 14, pin 6 will go high as pin 7 did for a Sync Mark.

2. The state of pin 6, 6E, goes to the input of the latch at pin 2, 12D. This latch is clocked on every nibble boundary for the second half of each block by the output of the NAND gate at pin 8, 11D.

3. If the File Mark pattern is detected by the PROM at 6E, the output of pin 5, 12D will go high. This output can be sampled by the 8048 on Port 1 via pin 13, 4E to see if a File Mark was read.

The next circuit is the Overrun flag.

1. When a Sync Mark is detected, the latch at pin 11, 11B is clocked by the SYNCR- signal. The input to the latch on pin 12, 11B is RCMP. RCMP is high when a buffer is not connected to the sequencer.

2. If a buffer has not been connected to read sequencer by the time a Sync Mark has been read, then data will be lost. When pin 9, 11B is high, an overrun has occurred. The 8049 can sample the output of this latch via pin 13, 3D.

The last circuit in the sequencer is the latch 5H.

1. This latch performs the same function as its counterpart in the write logic. The read sequencer is self-cycling and triggers on gap signal.

2. During the read-after-write the data does not go to a buffer.

3. Only the CRC and block address need to be verified.

4. During a read-only operation, data must go to a buffer to be transmitted to the host. To connect the sequencer to a buffer, the 8049 places a control word on the internal bus and clocks it into the latch at 5H. The clock is LDRD- which comes from pin 6, 11G. The control word assigns a buffer and takes RCMP false. When the buffer is full, the sequencer disconnects the buffer and sets RCMP true.

5. A reset from the host will also disconnect a buffer and set RCMP true.

Section II.

PERFORMANCE TESTING

9.29 SCOPE

Performance testing is of two types; performance testing of suspected Intelligent Controller and performance testing of repaired Intelligent Controller. In either type of performance testing, the Intelligent Controller should be mated with a known good Basic Drive and known good tapes should be used.

9.30 TESTING SUSPECTED INTELLIGENT CONTROLLERS

When testing a suspected controller, always use a known good Basic Drive.

9.31 READ CHECK

Using a known good tape with known data recorded on it and with a known good Basic Drive mated with the Intelligent Controller, attempt to read the tape.

NOTE

Do not use the Track Zero Alignment Tape or the Azimuth Alignment Tape for this check.

If the tape can be read, but has an unacceptable number of retries, then perform the alignment procedures in Appendix III. If the tape cannot be read, refer to the trouble list in Chapter 4.

9.32 WRITE CHECK

NOTE

Due to imperfections in the tape oxide coating, it is not uncommon to encounter numerous soft errors during writing of data to tape. With a known good qualified cartridge this soft error rate could approach 200 rewrites for a 20 Mbyte transfer.

Using a tape that is known to be physically a good tape and with the Intelligent Controller mated with a known good Basic Drive, attempt to write to the tape.

NOTE

Ensure that the write protect cam on the cartridge is in the write position before inserting the cartridge in the Basic Drive.

If the tape is written on, but has an unacceptable number of retries, the Controller is malfunctioning.

9.33 TESTING REPAIRED INTELLIGENT CONTROLLERS

Before testing a repaired Intelligent Controller, verify controller adjustments by using the procedures in Appendix III.

9.33.1 Read Check For Serviceability

Using a tape with zero read errors when read by the master drive and with the Intelligent Controller mated with a known good Basic Drive, attempt to read the tape. If there are a comparable number of read errors, then the Intelligent Controller may be returned to service.

9.33.2 Write Check For Serviceability

Using a known good tape, such as an Archive qualified tape, and with the Intelligent Controller mated with a known good Basic Drive, attempt to write to the tape.

NOTE

Ensure that the write protect cam on the cartridge is in the write position before inserting the cartridge in the Basic Drive.

If there are an acceptable number of errors, then the Intelligent Controller may be returned to service. Otherwise, write to the test tape with the master drive. If the number of errors is comparable to that of the repaired Intelligent Controller, then it may be returned to service.

Section III.

REPAIR PROCEDURES

9.34 SCOPE

The repair procedures in this section includes removal and replacement procedures, troubleshooting tips, and general precautions.

9.35 GENERAL PRECAUTIONS

When unsoldering and resoldering connections, be sure to use the appropriate size soldering tips. The tips should be large enough to melt the solder quickly and small enough not to damage insulation or semiconductor devices or loosen the circuit from the board. When possible, place a heat sink, such as long nose plier tips, between the semiconductor and the solder joint. When unsoldering, use a device to remove the melted solder. Always place piece parts that have been removed to gain access for repair in a plastic box or plastic bag for use during reassembly.

9.36 TROUBLESHOOTING TIPS

Obvious damage caused by overheating or breakage should always be repaired first. The information given in the trouble lists in Chapter 4 should be used to isolate the source of trouble to a specific circuit. It may be necessary to use an oscilloscope to isolate the trouble. There are, however, some facts that tend to suggest the failing part. The following is a list of electronic components presented in the order of their failure frequency:

Complex Integrated Circuits
Capacitors (fail short)
Signal Transistors
Diodes (fail open)
Resistors

This list is useful only as a clue after the faulty circuit has been isolated. All of the components can be expected to operate acceptably for thousands of hours.

Whenever there is evidence of physical mistreatment of the Intelligent Controller, it is reasonable to check all solder connections and verify that etching on the board is not broken.

9.37 REMOVAL AND REPLACEMENT

Normal removal of electronic components constitutes the only removal required. Observe precautions listed in paragraph 9.34.

APPENDIX I

PARTS LISTS

A1-1 SCOPE

This Appendix contains the parts lists and parts location diagrams for the basic Drive and the Intelligent Controller.

Table A1-1. Basic Drive Parts List

Item	Part Number	Description	Quantity
1	20068-901	Assembly, Main PWB	1*
1	20068-301	Assembly, Main PWB	1**
2	20026-001	Assembly, Sensor	1
3	20142-001	Assembly, Motor PWB	1
4	20023-001	Assembly, Drive Motor	1
4	20137-001	Assembly, Drive Motor (with fan)	1
5	20017-006	Assembly, Carriage	1

* Models 9020B and 9020I only.
** Models 3020B and 3020I only.

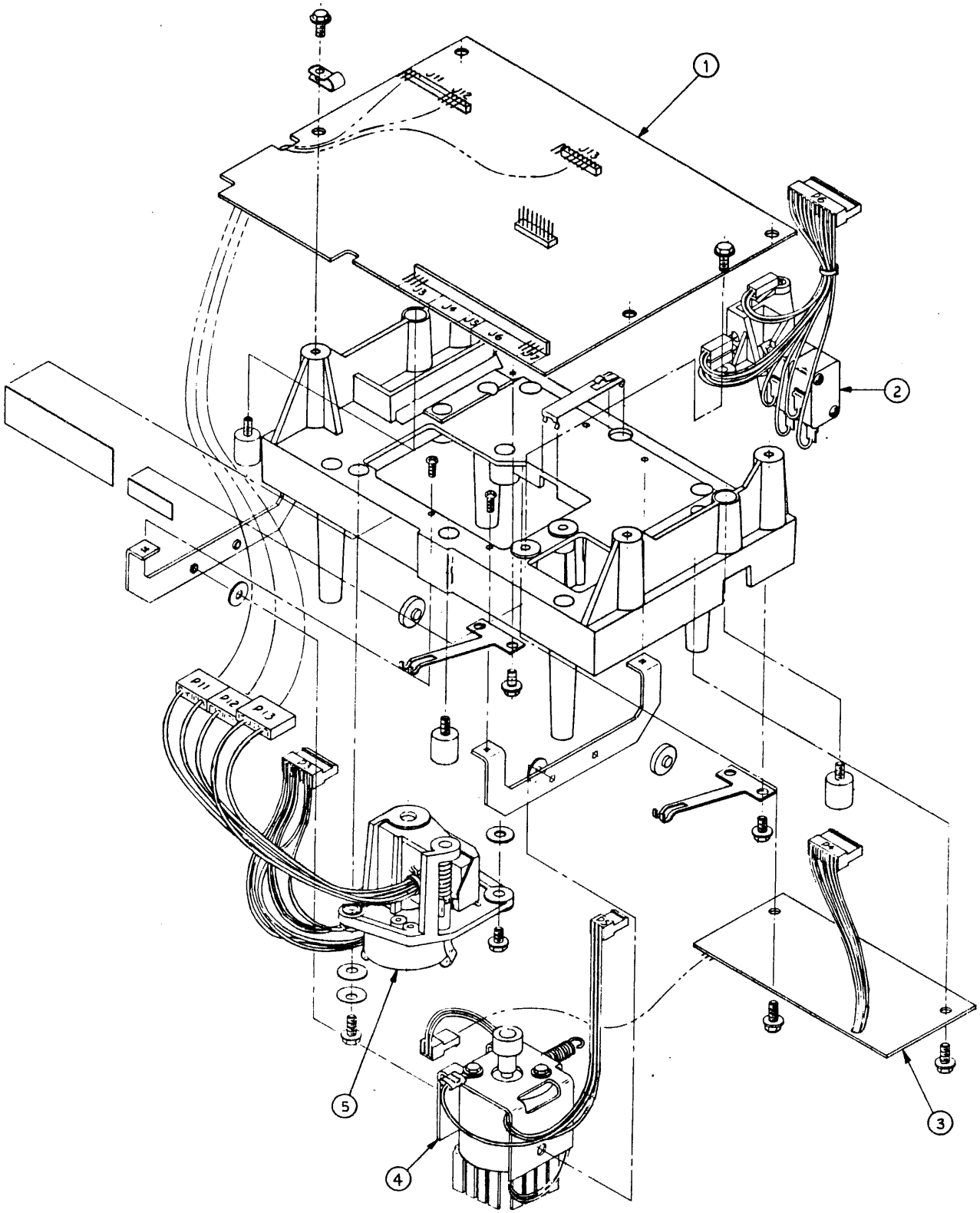


Figure A1-1. Basic Drive Parts Location Diagram

Table A1-2. Assembly, Main PWB Parts List

Reference Desig.	Part Number	Description	Quantity
	50029-001	PWB, Main	1*#
	50029-003	PWB, Main	1&@
1A	18204-001	Term., 220/330, 14 PIN DIP	1*#
1A	18209-001	Term., 180/290, 14 Pin DIP	1&@
1A, 2B	15815-014	Socket, I.C., Soldertail, DIP (14 PIN)	
1B, 1D, 3B, 5D	16502-001	I.C., 74LS04	4
2A	16500-001	I.C., 74S240	1
3A	18205-001	Term., 220/330, 16 PIN DIP	1*#
3A	18210-001	Term., 180/390, 16 Pin DIP	1&@
2B	18700-001	Shunt, I.C., 14 PIN	1
2D	16507-001	I.C., 74LS09	1
2E	19102-001	Trans., Array, PNP (QT2905)	1
2G	16512-001	I.C., 75451B	1
3A	15815-016	Socket, I.C., Soldertail, DIP (16 PIN)	1
3-4C	15815-040	Socket, I.C., Soldertail, DIP (40 PIN)	1
3-4C	17303-012	Micro Computer (8748-8)	1*
3D, 5E, 6D	16509-001	I.C., 74LS74	3
4B	16511-001	I.C., uA78L12AWC	1
4D	16508-001	I.C., 74LS02	1
4E	16513-001	I.C., 9602	1
5Ba, 5Bb	16504-001	I.C., 75452B	2
5C	15818-016	Header, Double Row	1
5C	15816-001	Clip, Jumper	2
5F, 7F	16516-001	I.C., NE592A	2
6C	16510-001	I.C., LM339	1
6E	16517-001	I.C., 74LS00	1
7C	16506-001	I.C., 74LS86	1
7D	16503-001	I.C., 7406	1
7E	16515-001	I.C., LM319	1
C1, 5, 7-10, 12 14, 15, 23-27, 29-31, 33, 29-42	15505-104	Cap., Ceramic, Z5U, +80% - 20%, 50V, 0.1uf	23
C2	15500-200	Cap., Ceramic, NPO, 5%, 50V, 20pf	1
C11, 13	15502-685	Cap., Tantalum, 20%, 4V, 6.8uf	2
C16, 21, 22	15500-330	Cap., Ceramic, NPO, 5%, 50V, 33pf	3*
C16	15500-330	Cap., Ceramic, NPO, 5%, 50V, 33pf	1#&@
C17	15500-301	Cap., Ceramic, NPO, 5%, 50V, 300pf	1&
C17	15500-302	Cap., Ceramic, NPO, 5%, 50V, 3000pf	1#@
C17	15500-331	Cap., Ceramic, NPO, 5%, 50V, 330pf	1*
C18, 19	15500-391	Cap., Ceramic, NPO, 5%, 50V, 390pf	2&
C18, 19	15500-122	Cap., Ceramic, NPO, 5%, 50V, 1200pf	2@
C18, 19	15500-301	Cap., Ceramic, NPO, 5%, 50V, 300pf	2*
C18, 19	15500-911	Cap., Ceramic, NPO, 5%, 50V, 910pf	2#
C20	15500-101	Cap., Ceramic, NPO, 5%, 50V, 100pf	1&

Table A1-2. Assembly, Main PWB Parts List (Continued)

Reference Desig.	Part Number	Description	Quantity
C20	15500-301	Cap., Ceramic, NPO, 5%, 50V, 300pf	1@
C20	15500-750	Cap., Ceramic, NPO, 5%, 50V, 75pf	1*
C20	15500-221	Cap., Ceramic, NPO, 5%, 50V, 220pf	1#
C21	15500-131	Cap., Ceramic, NPO, 5%, 50V, 130pf	1#
C21, 22	15500-221	Cap., Ceramic, NPO, 5%, 50V, 220pf	2&@
C22	15500-101	Cap., Ceramic, NPO, 5%, 50V, 100pf	1#
C28, 38	15501-225	Cap., Tantalum, 20%, 10V, 2.2uf	2
C32	15503-475	Cap., Tantalum, 20%, 35V, 4.7uf	1
C34	15504-225	Cap., Tantalum, 20%, 20V, 2.2uf	1
C35, 51, 52	15501-226	Cap., Tantalum, 20%, 10V, 22uf	3
C37	15506-472	Cap., Ceramic, X7R, 10%, 50V, 0.0047uf	1
C43, 46-49	15506-102	Cap., Ceramic, X7R, 10%, 50V, 0.001uf	5
C44, 45	15506-104	Cap., Ceramic, X7R, 10%, 50V 0.1uf	2
C50	15500-047	Cap., Ceramic, NPO, 5%, 50V, 4.7uf	1
C53	15500-620	Cap., Ceramic, NPO, 5%, 50V, 62pf	1@
C53	15500-200	Cap., Ceramic, NPO, 5%, 50V, 20pf	1&
CF2	19402-001	Wire, 26 AWG Solid	A/R#@
CR1-14, 18-25	16100-001	Diode, (1N4150)	22
CR15	16103-001	Diode, (1N4001)	1&@
CR16	17201-001	Led, Visible, Red	1
J2	15804-004	Housing, Connector	1
J2	15806-001	Contact, Connetor	1
J2	14500-004	Tie, Cable	1
J3	15809-007	Header, Right Angle	1
J4-7	15809-024	Header, Right Angle	1
J11, 12	15817-014	Wafer, Right Angle	1
J13	15817-008	Wafer, Right Angle	1
L1, 2	16401-127	Inductor, Molded, 5%, 120uh	2*#
L3, 4	16401-247	Inductor, Molded, 5%, 240uh	2*
L3, 4	16401-757	Inductor, Molded, 5%, 750uh	2#
L3, 4	16401-277	Inductor, Molded, 5%, 270uh	2&
L3, 4	16401-827	Inductor, Molded, 5%, 820uh	2@
L5, 6	16401-566	Inductor, Molded, 5%, 56uh	2*
L5, 6	16401-167	Inductor, Molded, 5%, 160uh	2#
L5, 6	16401-127	Inductor, Molded, 5%, 120uh	2&
L5, 6	16401-367	Inductor, Molded, 5%, 360uh	2@
L7, 8	16401-106	Inductor, Molded, 10%, 10uh	2
Q1, 2	14300-001	Pad, Transistor	2
Q1, 2	19105-001	Transistor, (MM3007)	2
Q3, 4, 5, 6, 7	19107-001	Transistor, (2N3904)	5
R1	18203-181	Resistor, Metal Film, 1/4w, 1%, 75	1
R2, 3	18200-121	Resistor, Carbon, 1/4w, 5%, 120	2
R4	18200-470	Resistor, Carbon, 1/4w, 5%, 47	1

Table A1-2. Assembly, Main PWB Parts List (Continued)

Reference Desig.	Part Number	Description	Quantity
R5	18203-232	Resistor, Metal Film, 1/4w, 1%, 255	1
R7, 10, 58, 61	18200-681	Resistor, Carbon, 1/4w, 5%, 680	4
R8	18203-254	Resistor, Metal Film, 1/4w, 1%, 432	1
R13, 16, 18, 47, 87, 89, 73, 74, 41, 42, 55	18200-102	Resistor, Carbon, 1/4w, 5% 1K	11#&
R13, 16, 18, 47, 55, 87, 89, 41, 42, 38	18200-102	Resistor, Carbon, 1/4w, 5%, 1K	10#@
R14, 15, 17, 19, 20	18200-682	Resistor, Carbon, 1/4w, 5%, 6.8K	5
R22, 62	19402-001	Wire, 26 AWG Solid	A/R*#
R23, 24	18200-100	Resistor, Carbon, 1/4w, 5%, 10	2
R25, 26, 36, 37, 52	18203-385	Resistor, Metal Film, 1/4w, 1%, 10.0K	5
R27	17800-104	Pot., Ceramic, 10%, 100K	1
R28, 30	18200-333	Resistor, Carbon, 1/4w, 5%, 33K	2
R29, 39	18203-289	Resistor, Metal Film, 1/4w, 1%, 1.0K	2
R31	18203-302	Resistor, Metal Film, 1/4w, 1%, 1.37K	1*
R31	18203-254	Resistor, Metal Film, 1/4w, 1%, 432	1#
R31	17800-202	Pot., Ceramic, 10%, 2K	1@
R31	17800-502	Pot., Ceramic, 10%, 5K	1&
R32, 33	18203-351	Resistor, Metal Film, 1/4w, 1%, 4.42K	2
R34, 35, 49, 50, 51	18200-511	Resistor, Carbon, 1/4w, 5%, 510	5
R38	18200-302	Resistor, Carbon, 1/4w, 5%, 3K	1*@
R40, 44	18203-347	Resistor, Metal Film, 1/4w, 1%, 4.02K	2
R43	18200-203	Resistor, Carbon, 1/4w, 5%, 20K	1
R45	18203-365	Resistor, Metal Film, 1/4w, 1%, 6.19K	1&
R45	18203-413	Resistor, Metal Film, 1/4w, 1% 19.6K1	1@
R45, 46	18200-303	Resistor, Carbon, 1/4w, 5%, 30K	2*#
R46	18200-622	Resistor, Carbon, 1/4w, 5%, 6.2K	1&
R46	18200-203	Resistor, Carbon, 1/4w, 5%, 20K	1@
R48	18200-330	Resistor, Carbon, 1/4w, 5%, 33	1
R53, 95	18203-415	Resistor, Metal Film, 1/4w, 1%, 20.5K	2
R54	18200-221	Resistor, Carbon, 1/4w, 5%, 220	1

Table A1-2. Assembly, Main PWB Parts List (Continued)

Reference Desig.	Part Number	Description	Quantity
R56	18200-471	Resistor, Carbon, 1/4w, 5%, 470	1
R57, 59, 60, 79, 81	18200-472	Resistor, Carbon, 1/4w, 5%, 4.7K	5
R63, 66, 72, 77	18200-104	Resistor, Carbon, 1/4w, 5%, 100K	4
R64, 65, 67, 71, 75, 76, 78, 86, 88, 92, 93, 96	18200-103	Resistor, Carbon, 1/4w, 5%, 10K	12
R69	18200-152	Resistor, Carbon, 1/4w, 5%, 1.5K	1
R70	18201-121	Resistor, Carbon, 1/2w, 5%, 120	1
R73, 74	18200-332	Resistor, Carbon, 1/4w, 5%, 3.3K	2#@
R80	18200-122	Resistor, Carbon, 1/4w, 5%, 1.2K	1
R82-85	18200-101	Resistor, Carbon, 1/4w, 5%, 100	4*#
R90	18200-161	Resistor, Carbon, 1/4w, 5%, 160	1
R91, 94	18200-473	Resistor, Carbon, 1/4w, 5%, 47K	2
R97	18200-272	Resistor, Carbon, 1/4w, 5%, 2.7K	1
R98	18200-392	Resistor, Carbon, 1/4w, 5%, 3.9K	1
TP1-9	15810-004	Pin, Wire Wrap	9
Y1	16000-001	Crystal, 3.579545 MHZ	1
Y1	14400-001	Tape, Double Coated Polyurethane	A/R

Note: Unless indicated by a symbol, all quantities are per assembly for all models. The symbol references are as follows:

* = PN 20144-901
\# = PN 20144-301
& = PN 20144-903
@ = PN 20144-303

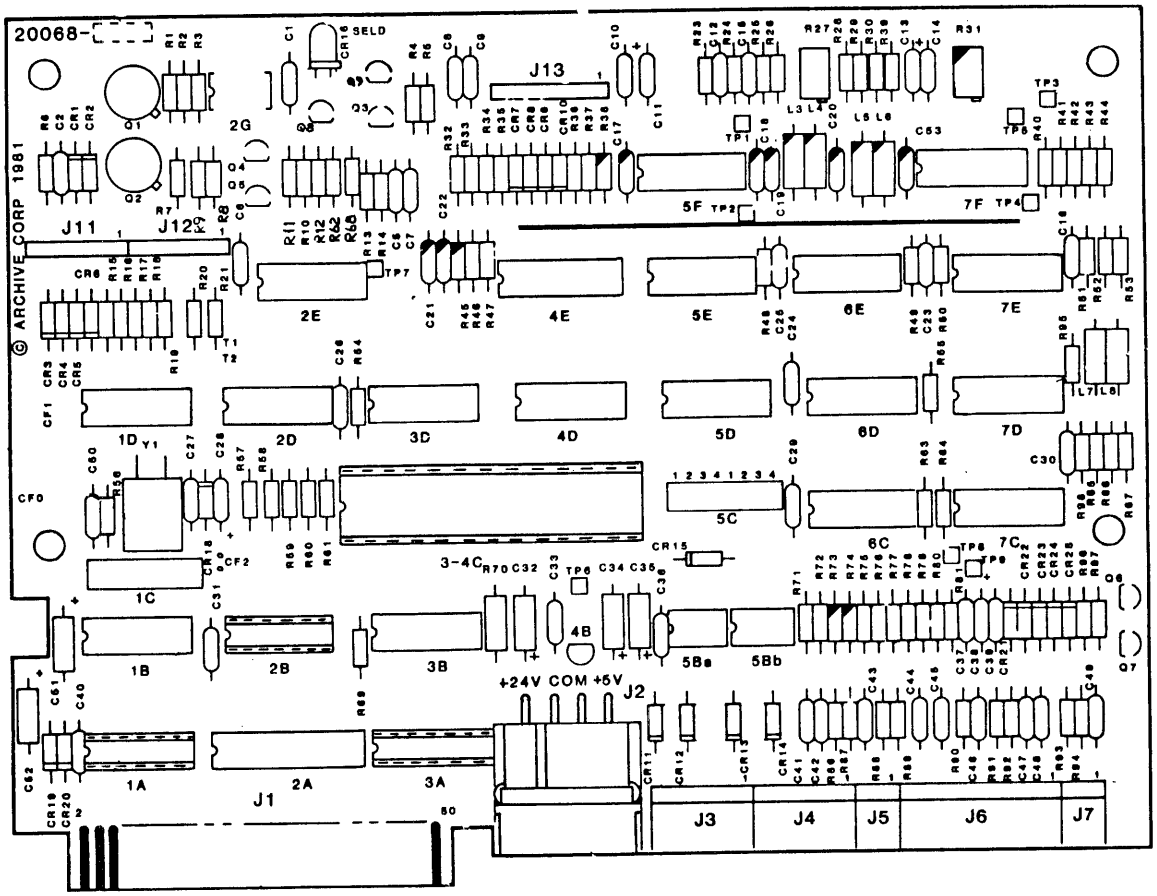


Figure A1-2. Assembly, Main PWB Parts Location Diagram

Table A1-3. Assembly Motor PWB

Reference Desig.	Part Number	Description	Quantity
	40079-001	PWB, Motor Driver	1
	20143-001	Assembly, Cable	1
1B, 2E	16517-001	I.C., 74LS00	2
1C, 2C	16564-001	I.C., LM2904	2
1E	16565-001	I.C., 74LS136	1
2G	16569-001	I.C., NE556	1
C1	15507-107	Cap., Miniature Electrolytic, +50-10%, 35V, 100uf	1
C2, C3	15501-106	Cap., Tantalum, 20%, 10V, 10wf	2
C4, C5, C10, C12	15505-104	Cap., Ceramic, Z5U, 50V, .1wf	4
C6	15506-473	Cap., Ceramic, X7R, 5%, 50V, .047wf	1
C7	15506-183	Cap., Ceramic, X7R, 10%, 50V, .018wf	1
C8	15506-104	Cap., Ceramic, X7R, 10%, 50V, .1wf	1
C9, C11	15500-473	Cap., Ceramic, NPO, 5%, 50V, 4700pf	2
CR1, CR4	16100-001	Diode (1N4150)	2
J8	15808-003	Header, 0.100 CTR, Straight (3 positions)	1
Q1, 3	19101-001	Transistor, Power, Darlington, NPN (TIP 125)	2
Q2, 4	19100-001	Transistor, Power, Darlington, NPN (TIP 120)	2
Q5, Q6, Q7, Q8	19107-001	Transistor, NPN (2N3904)	4
(Q1-Q4)	13602-404	Screw, Pan hd, Phillips	2
(Q1-Q4)	12900-004	Nut, hex	2
(30-90)	15816-001	Clip, jumper	1
(30-90)	15810-004	Pin, wire wrap	3
R1	18208-001	Res., Wirewound, 1W, 1%, 0.1 ohm	1
R2, R3, R10, R15	18200-103	Res., Carbon, 1/4W, 5%, 10K	4
R4, R5	18200-682	Res., Carbon, 1/4w, 5%, 6.8K ohms	2
R6, R12, R13	18200-202	Res., Carbon, 1/4W, 5%, 2K	3
R7	18200-752	Res., Carbon, 1/4W, 5%, 7.5K	1
R8, R9	18200-152	Res., Carbon, 1/4W, 5%, 1.5K	2
R11, R14	18200-302	Res., Carbon, 1/4W, 5%, 3K	2
R16, R17, R20, R23	18203-481	Res., Metal film, 1/4W, 1% 100K	4
R18	18203-334	Res., Metal film, 1/4W, 1%, 2.94K	1
R19, R21	18203-385	Res., Metal film, 1/4W, 1%, 10.0K	2
R22, R30	18200-203	Res., Carbon, 1/4W, 5%, 20K	2
R24	18203-477	Res., Metal Film, 1/4W, 1%, 90.0K	1
R25, R32	18203-452	Res., Metal Film, 1/4W, 1%, 49.9K	2
R26, R29, R33	18203-289	Res., Metal Film, 1/4W, 1%, 1.00K	2
R27, R28	18203-347	Res., Metal Film, 1/4W, 1%, 499K	2
R31, R36	18203-548	Res., Metal Film, 1/4W, 1%, 1.82K	1
R34	18203-314	Res., Metal Film, 1/4W, 1%, 2.00K	1
R35	18203-318	Res., Metal Film, 1/9W, 1%, 1.2K	1
R37	18200-122	Res., Carbon, 1/4W, 5%, 1.2K	1
R38	18203-460	Res., Metal Film, 1/4W, 1%, 60.5K	1
R39	18200-102	Res., Carbon, 1/4W, 5%, 1K	1
R40	18203-444	Res., Metal film, 1/4W, 1%, 41.2K	1
R41	18203-270	Res., Metal film, 1/4W, 1%, 634 ohm	1

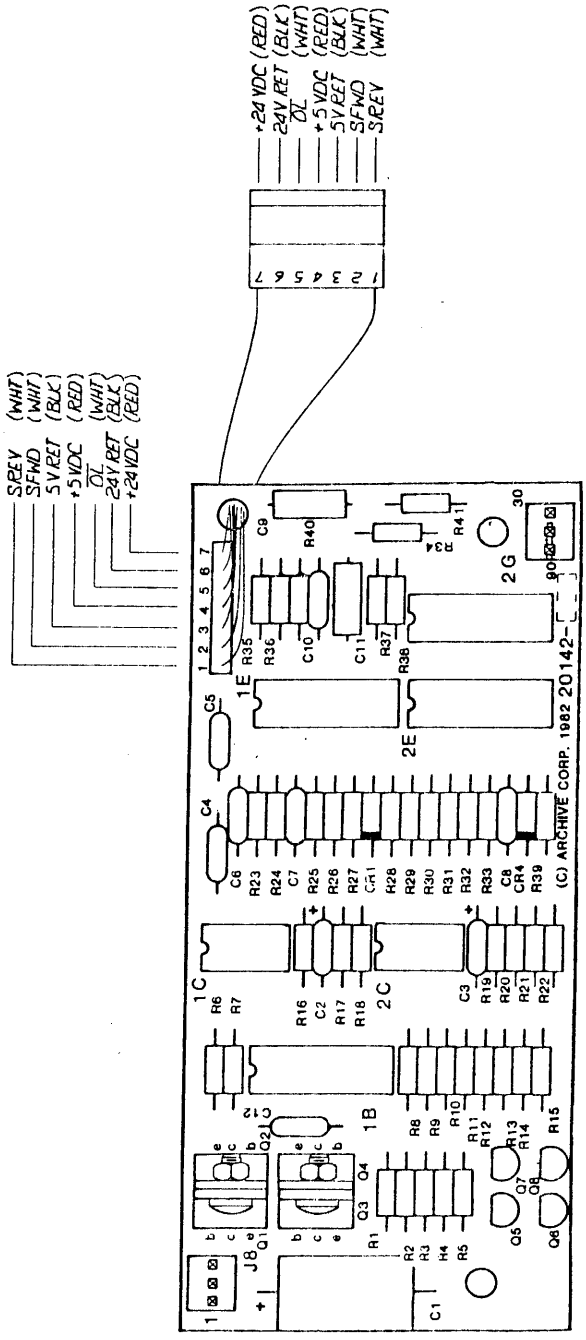


Figure A1-3. Assembly Motor PWB Parts Location Diagram

Table A1-4. Intelligent Controller Board Parts List

Reference Desig.	Part Number	Description	Quantity
	50039-001	PWB Controller	1*#&¢
	50039-003	PWB, Controller	1&@
	20048-002	Power Cable Assy.	1
1K, 6B	15815-016	Socket, I.C., Soldertail, DIP (16 PIN)	2
1K	18210-001	Terminator, 180/390, 16 Pin DIP	1&@
1K	18205-001	Terminator, 220/330, 16 PIN DIP	1*#$¢
2B, 3B, 3K, 4K	16500-001	I.C., 74S240	4&@$¢
2B, 2K, 3B, 3K, 4K	16500-001	I.C., 74S240	5*#
2C	16563-001	I.C., 74LS273	1
2EF	15815-040	Socket, I.C., Soldertail, DIP (40 PIN)	1
2G	16514-001	I.C., LM311	1
2K	16548-001	I.C., 74LS240	1&@$¢
3C	16536-001	I.C., 74LS374	1
3D	16551-001	I.C., 74LS373	1
3E, 3F, 4E, 4F	16527-001	I.C., 74LS153	4
3G, 3H	16534-001	I.C., 74LS195	2
4B	16501-001	I.C., 7438	1
4D, 5E, 13K	16530-001	I.C., 74LS164	3
4G, 5C, 5G	16519-001	I.C., 74LS08	3
4H, 5H, 5K	16533-001	I.C., 74LS175	3
5B	16521-001	I.C., 74LS14	1
5D, 10E, 11C	16525-001	I.C., 74LS138	3
5F, 11F, 12C	16522-001	I.C., 74LS32	3
6A	16504-001	I.C., 75452B	1
6C, 11B, 12D, 12G, 12H	16509-001	I.C., 74LS74	5*&$
6C, 11B, 12D, 12F, 12G, 12H	16509-001	I.C., 74LS74	6#@¢
6D, 7D, 7F	16555-001	I.C., 74SL74	3
6E	16544-001	I.C., 74S288 (32 x 8 PROM) (RD DEC)	1
6F, 8F, 13C	16541-001	I.C., 4040	3
6G, 6H, 6K, 7G, 7H	16535-001	I.C., 74LS367	5
7A	16523-001	I.C., 74LS51	1
7B, 11D	16517-001	I.C., 74LS00	2
7C	16557-001	I.C., 74S04	1
8B	16559-001	I.C., 74S174	1
8C	16556-001	I.C., 74S00	1
8D	16558-001	I.C., 74S163	1
8E	16539-001	I.C., 4044	1
8G, 8H, 8K	16545-001	I.C., 2141-5 (4096 x 1 RAM)	3
9B, 9C	16562-001	I.C., CD4502	2

Table A1-4. Intelligent Controller Board Parts List (Continued)

Reference Desig.	Part Number	Description	Quantity
9D, 13D	16529-001	I.C., 74SL163	2
9E, 10C, 11H	16532-001	I.C., 74SL174	3
9F	16543-001	I.C., 74S287 (256 x 4 PROM) (W SEQ)	1
9G, 9H, 9K, 10G, 10K	16537-001	I.C., 74LS393	5
10B	16542-001	I.C., 93446 (512 x 4 PROM) (RD SEQ)	1
10D, 10H, 12E, 12K	16502-001	I.C., 74LS04	4
10F	16520-001	I.C., 74LS11	1
11A	16561-001	I.C., LF353	1
11E, 13A	16538-001	I.C., 9401	2
11G	16526-001	I.C., 74LS139	1
11K	16543-004	I.C., 74S287 (256 x 4 PROM) (HOST SEQ)	1
12A	16560-001	I.C., 74S124	1
12B, 13B	16513-001	I.C., 9602	2
13E	16524-001	I.C., 74LS109	1
13F	16518-001	I.C., 74LS01	1
13H	16544-002	I.C., 74S288 (32 x 8 PROM) (W ENC)	1
14G	16552-005	I.C., 7805 (5V POS VOLTAGE REG.)	1
90 IPS	19402-001	Wire, 26 Awg Solid	A/R*&$
C1	15500-100	Cap., Ceramic, NPO, 5%, 50V, 10pf	1*&$
C1	15500-330	Cap., Ceramic, NPO, 5%, 50V, 33pf	1#@ç
C2, 3, C6, C7, C8, 24-50	15505-104	Cap., Ceramic, Z5U, +80% - 20%, 50V, 0.1uf	32
C4	15500-472	Cap., Ceramic, NPO, 5%, 50V, 4700pf1	1
C5	15500-472	Cap., Ceramic, NPO, 5%, 50V, 4700pf	1*&$
C5	15506-563	Cap., Ceramic, X7R, 10%, 50V, 0.056uf	1#@ç
C9, 10	15500-301	Cap., Ceramic, NPO, 5%, 50V, 300pf	2&@
C10	15500-301	Cap., Ceramic, NPO, 5%, 50V, 300pf	1*#$ç
C11	15500-911	Cap., Ceramic, NPO, 5%, 50V, 910pf	1*&$
C11	15500-272	Cap., Ceramic, NPO, 5%, 50V, 0.0027uf	1#@ç
C12	15500-272	Cap., Ceramic, NPO, 5%, 50V, 0.0027uf	1*&$
C12	15500-822	Cap., Ceramic, NPO, 5%, 50V, 0.0082uf	1#@ç
C13	15500-301	Cap., Ceramic, NPO, 5%, 50V, 300pf	1*&$
C13	15500-911	Cap., Ceramic, NPO, 5%, 50V, 910pf	1#@ç

Table A1-4. Intelligent Controller Board Parts List (Continued)

Reference Desig.	Part Number	Description	Quantity
C14	15500-150	Cap., Ceramic, NPO, 5%, 50V, 15pf	1
C15	15501-225	Cap., Tantalum, 20%, 10V, 2.2uf	1
C16	15501-226	Cap., Tantalum, 20%, 10V, 22uf	1
C17, 21	15503-475	Cap., Tantalum, 20%, 34V, 4.7uf	2
C18, 22, 23	15506-102	Cap., Ceramic, X7R, 10%, 50V, 0.001uf	3
C19	15500-391	Cap., Ceramic, NPO, 5%, 50V, 390pf	1*&$
C19	15500-122	Cap., Ceramic, NPO, 5%, 50V, 1200pf	1#@¢
C20	15501-475	Cap., Tantalum, 20%, 10V, 4.7uf	1
C51	15500-047	Cap., Ceramic, NPO, 5%, 50V, 4.7pf	1
C52	15500-151	Cap., Ceramic, NPO, 5%, 50V, 150pf	1*#
C52	15506-102	Cap., Ceramic, X7R, 10%, 50V, 1000pf	1&@$¢
C54	15500-221	Cap., Ceramic, NPO, 5%, 50V, 220pf	1&@$¢
CR1, 3-6	16100-001	Diode, Switching (1N4150)	5&@$¢
CR1, 3-5	16100-001	Diode, Swtiching (IN4150)	4*#
CR2	16101-001	Diode, Zener, 12V (IN759)	1
J2	15804-004	Housing, Connector	1
J2	15806-001	Contact, Connector	4
J2	14500-004	Tie, Cable	1
P4, 5	20081-001	Cable Assy	2
Q1	19110-001	Transistor, PNP, 2N3906	1
Q2	19107-001	Transistor, NPN, 2N3904	1
R1, 29, 28, 31-34, 37-41, 47, 51, 52, 55, 60-66, 73-77, 79	18200-102	Resistor, Carbon, 1/4w, 5%, 1K	29*#
R1	18203-318	Resistor, Metal Film, 1/4w, 1%, 2.0K	1&@
R2	18200-302	Resistor, Carbon, 1/4w, 5%, 3K	1*#
R2	18203-335	Resistor, Metal Film, 1/4w, 1%, 3.01K	1&@
R3, 19, 35, R5	18200-511	Resistor, Carbon, 1/4w, 5%, 510	4*#$¢
R3, 19, 35	18200-511	Resistor, Carbon, 1/4w, 5%, 510	3&@
R4	18200-562	Resistor, Carbon, 1/4w, 5%, 5.6K	1*#$¢
R4	18203-361	Resistor, Metal Film, 1/4w, 1%, 5.62K	1&@
R5	18203-261	Resistor, Metal Film, 1/4w, 1%, 511	1&@
R6	18200-362	Resistor, Carbon, 1/4w, 5%, 3.6K	1
R7	17800-502	Pot., Cermet, 10%, 5K	1
R8	18200-562	Resistor, Carbon, 1/4w, 5%, 5.6K	1*$
R8	18200-302	Resistor, Carbon, 1/4w, 5%, 3K	1#¢
R8	18203-361	Resistor, Metal Film, 1/4w, 1%, 5.62K	1&

Table A1-4. Intelligent Controller Board Parts List (Continued)

Reference Desig.	Part Number	Description	Quantity
R8	18203-335	Resistor, Metal Film, 1/4w, 1%, 3.01K	1@
R9, 10, 15, 16, 21, 50, 68, 70	18203-414	Resistor, Metal Film, 1/4w, 1%, 20.0K	8
R11	17800-503	Pot., Cermet, 10%, 50K	1
R12	18200-823	Resistor, Carbon, 1/4w, 5%, 82K	1*&$
R12	18200-154	Resistor, Carbon, 1/4w, 5%, 150K	1#@¢
R13, 14	18200-333	Resistor, Carbon, 1/4w, 5%, 33K	2
R17, 67	18203-443	Resistor, Metal Film, 1/4w, 1%, 40.2K	2
R18, 49, 69, 71	18203-385	Resistor, Metal Film, 1/4w, 1%, 10.0K	4
R20, 42	18200-750	Resistor, Carbon, 1/4w, 5%, 75	2
R22, 58	18200-473	Resistor, Carbon, 1/4w, 5%, 47K	2
R23, 44	18200-512	Resistor, Carbon, 1/4w, 5%, 5.1K	2
R24, 78	18200-103	Resistor, Carbon, 1/4w, 5%, 10K	2
R25	17800-103	Pot., Cermet, 10%, 10K	1
R26, 27, 43, 45, 46, 56, 57	18200-472	Resistor, Carbon, 1/4w, 5%, 4.7K	7
R29, 28, 31-34, 51, 52, 55, 60-62, 64-66, 73-77, 79, 47	18200-102	Resistor, Carbon, 1/4w, 5%, 1K	27&@$¢
R30	18200-244	Resistor, Carbon, 1/4w, 5%, 240K	1
R36	18200-471	Resistor, Carbon, 1/4w, 5%, 470	1
R53	18200-470	Resistor, Carbon, 1/4w, 5%, 47	1
R59	18200-105	Resistor, Carbon, 1/4w, 5%, 1 MEG	1
R63, 80-83	18200-221	Resistor, Carbon, 1/4w, 5%, 220	5&@
R63, 80-82	18200-221	Resistor, Carbon, 1/4w, 5%, 220	4$¢
R72	18200-203	Resistor, Carbon, 1/4w, 5%, 20K	1
R80-82	18200-221	Resistor, Carbon, 1/4w, 5%, 220	3*#
R84	18200-331	Resistor, Carbon, 1/4w, 5%, 330	1&@
TP1-16	15810-004	Pin, Wire Wrap	16&@
TP1-13	15810-004	Pin, Wire Wrap	13*#$¢
Y1	16000-002	Crystal, 6.000 MHZ	1
Y2	16000-001	Crystal, 3.579545 MHZ	1
Y1, 2, 14G	14400-001	Tape, Double Coated Polyurethane	A/R

Note: Unless indicated by a symbol, all quantities are per assembly for all Models. The symbol references are as follows:

* = PN 20146 - 901
\# = PN 20146 - 301
& = PN 20146 - 903
@ = PN 20146 - 303
$ = PN 20146 - 904
¢ = PN 20146 - 304

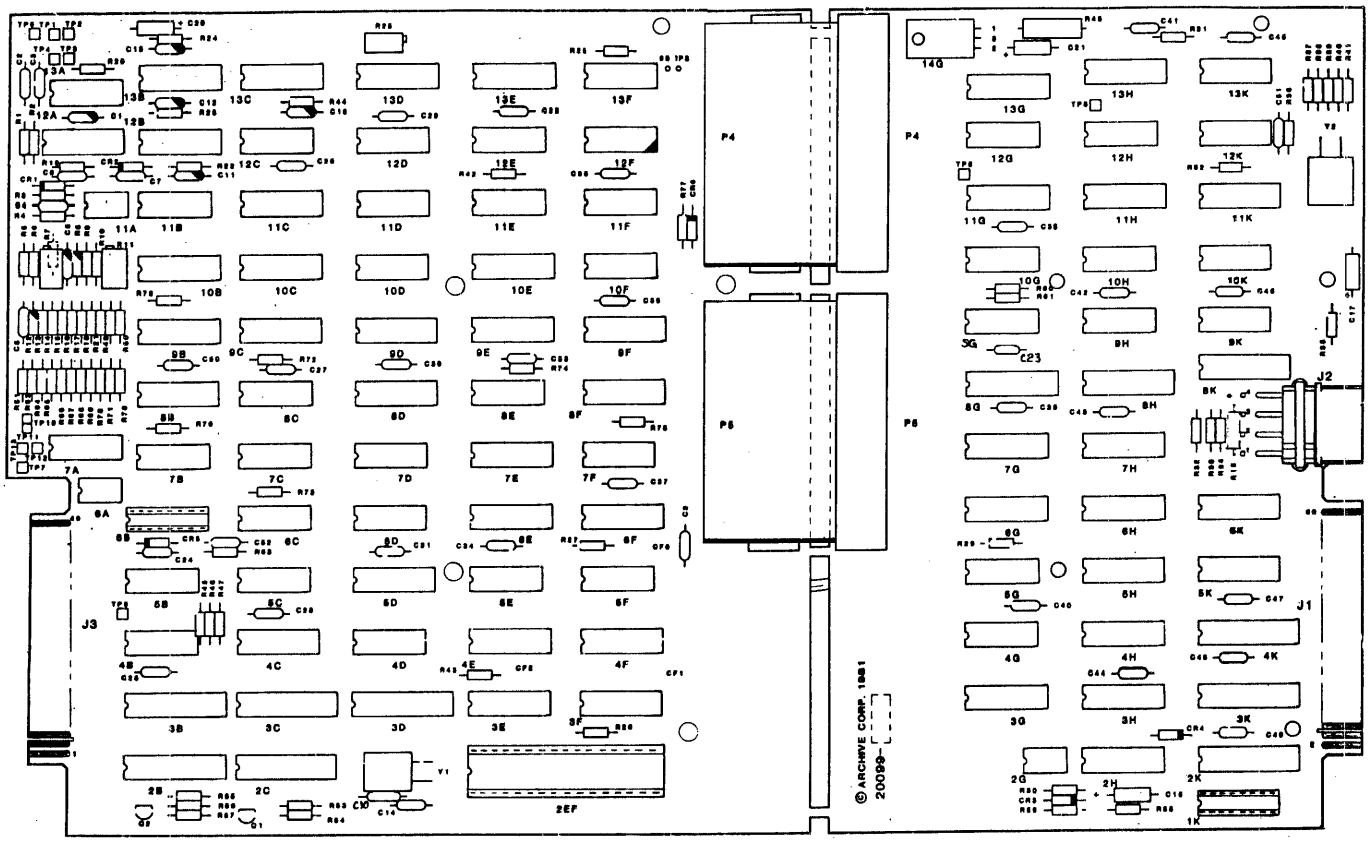


Figure A1-4. Intelligent Controller Board Parts Location

Table A1-5. Microcomputer Expander Board Parts List

Reference Desig.	Part Number	Description	Quantity
	40050-001	PWB, Expander	1
1B	17302-001	Microcomputer (8035)	1
2A	16533-001	IC, Quad D-Type Flip-Flop (74LS175)	1
2B	15815-024	Socket, IC, Soldertail, DIP (24-Pin)	1
3A	16551-001	IC, Octal Transparent Latch (74LS373)	1
C1	15505-104	Cap., Ceramic, Z5U, +80% - 20%, 50V, 0.1uf	1
P10	15823-040	Connector, DIP Plug (CA# CA-40PF-12)	1
	14901-001	Tape	4"

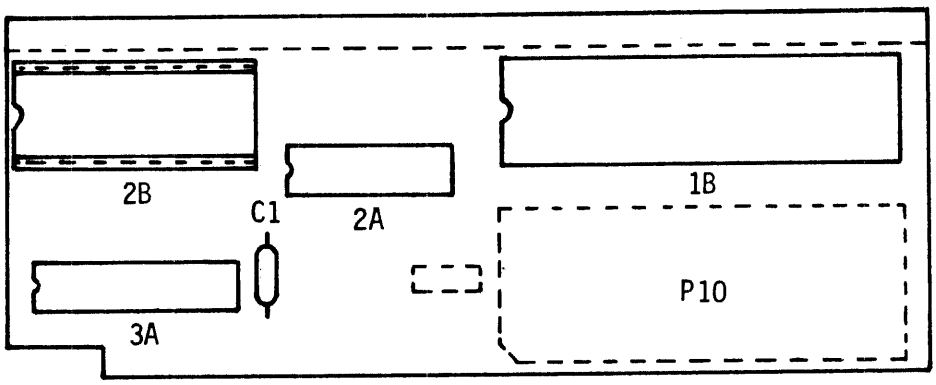


Figure A1-5. Microcomputer Expander Board Parts Location

APPENDIX II

LOGIC DIAGRAMS

A2.1 SCOPE

This appendix contains the logic diagrams and schematics and a glossary of mnemonics for the ARCHIVE Intelligent Cartridge Tape Drive.

Table A2-1. Mnemonic Glossary

Mnemonic	Meaning
ADDR	Address Read
BYTERDY	BYTE READY
CFO-CF2	Configuration Jumpers
CIN	Cartridge In
CRCER	CRC Error
CLROVR	Clear Overrun
CRCW	CRC Character Write
DONE	Done
DIRC	Direction
DSCRP	Data Shift Register Clock Pulse
DATAW	Data Write
DATA	Data
EXCEPT	Exception
ERSYNC	Expect Read Sync
EEN	Erase Enable
FMDET	File Mark Detect
FMW	File Mark Write
GAPW	Gap Write
GO	Go
GAP	Gap
HCMP	Host Complete
HDIN	Host Data In
HSPD	High Speed
HIN 0-7	Host Bus In
HINCAD	Host Increment Address
HWTMEM	Host Write Memory
HCLK	Host Clock
IDLE	Idle
LDSEL	Load Drive Select
LHOST	Load Host-Status
LDHOST	Load Host-Data
LDBADR	Load Block Address
LDBUF	Load Buffer Assignment
LDDRV	Load Drive
LDRD	Load Read

Table A2-1. Mnemonic Glossary (Continued)

Mnemonic	Meaning
LDWRT	Load Write
LTH	Lower Tape Hole
LDAT	Load Data
LST 0-3	Read Sequencer state bits
NIBLCK	Nibble Clock - write sequencer
NDTADET	No Data Detected
OVRUN	Overrun
ONLINE	Online
RST	Reset
RSTAD	Reset Address
REQUEST	Request
READY	Ready
REV	Reverse
RB	Read Block Address, bits 0-7
RINC	Read Increment Address
RDATA	Read Data
RDP	Read Data Pulse
RDL	Read Data Level
RNIB	Nibble clock-read sequencer
RDSR	Read Data Shift Register pulse
RLOCK	Read Lock
RCRC2	Read CRC byte two
RCMP	Read Complete
SYNCR	Sync Read
SEL 0-3	Select Drive 0-3
SELD	Selected
SYNCW	Sync Write
STPEN	Step Enable
STMEM	Start Memory
SACK	Set Acknowledge
ST 1-3	State bits, host sequencer
THD	Not used
TACH	Tach
WDONE	Write Done
WEN	Write Enable
WR	Write Strobe
WCMP	Write Complete
WINCAD	Write Increment Address
WFM	Write File Mark
WADR	Write Block Address
WRP	Write Data Pulse
WST	State bits, write sequencer
WDATA	Write Data
UTH	Upper Tape Hole
USF	Unsafe
XFR	Transfer

Table A2-1. Mnemonic Glossary (Continued)

Mnemonic	Meaning
1-3HST	One-Three Host
1-3WRT	One-Three Write
1-3RD	One-Three Read

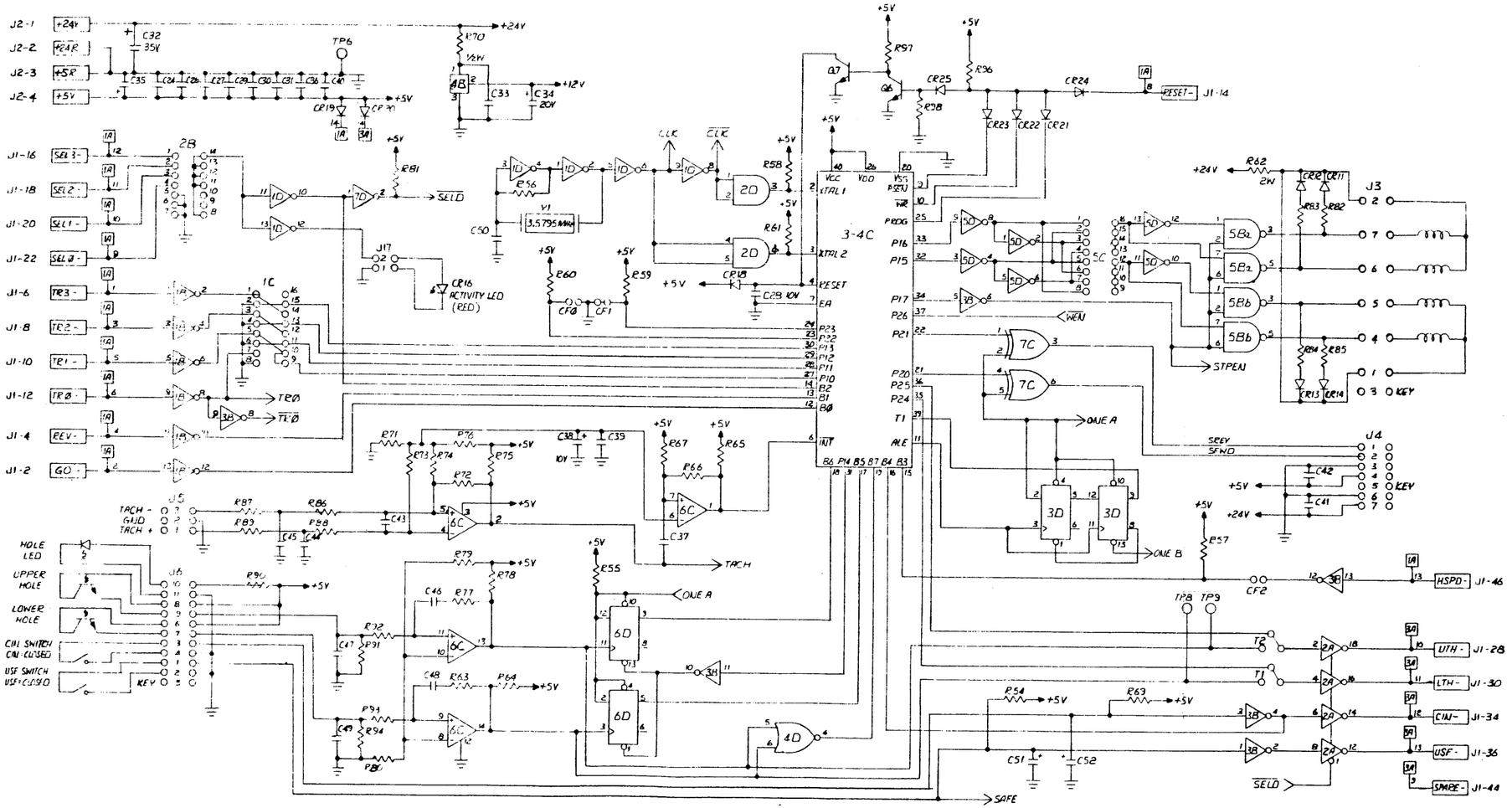


Figure A2-1. Main PWB Control Circuits Logic Diagram

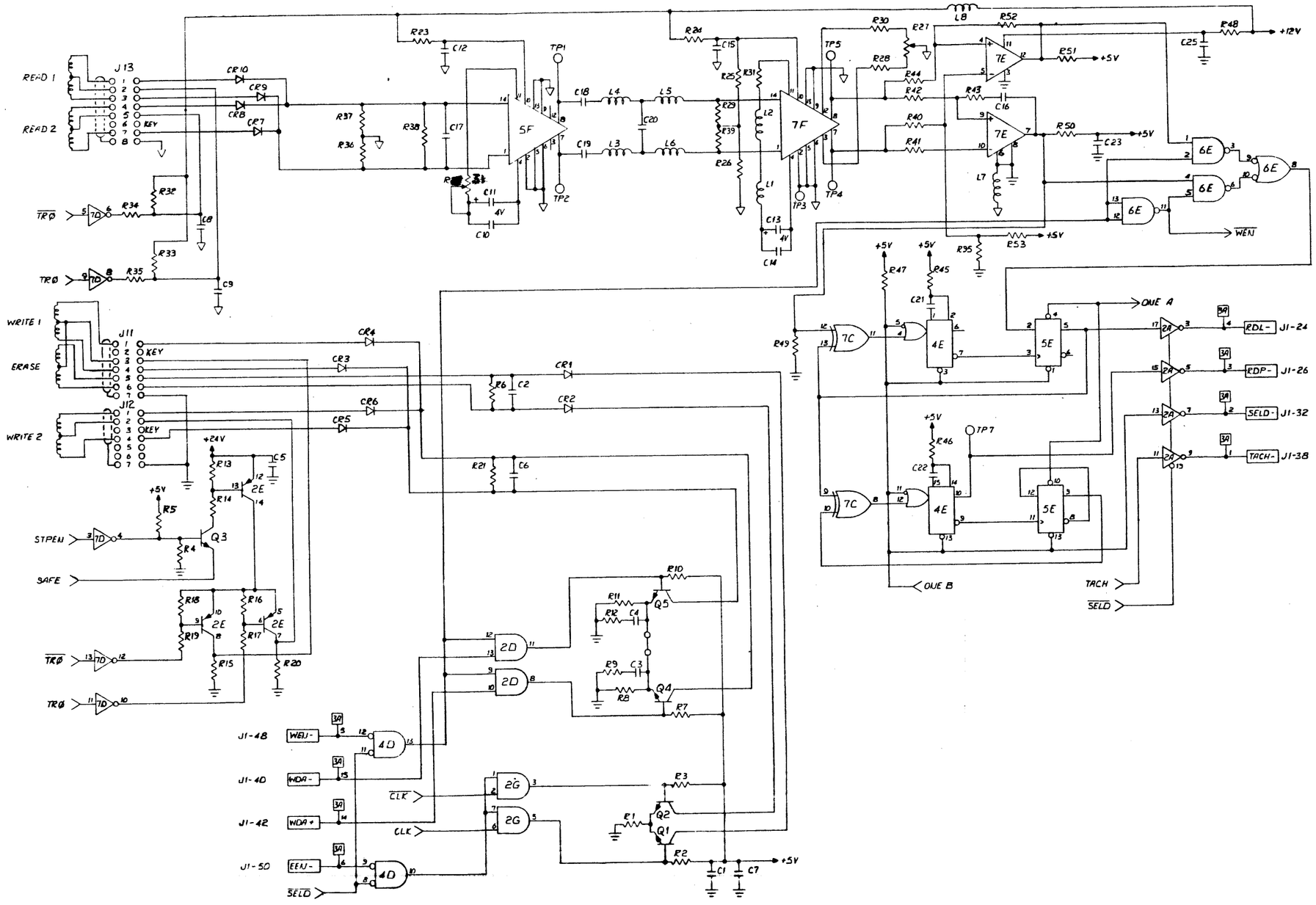


Figure A2-2. Main PWB Read/Write Circuits Logic Diagram

IC DESIGNATORS			
LOCATION	TYPE	PWR	GND
1E	74LS136	+5V	5R
1C	LM2904	+24V	24R
2G	NE556	+5V	5R
2E, 1B	74LS00	+5V	5R
2C	LM2904	+5V	5R

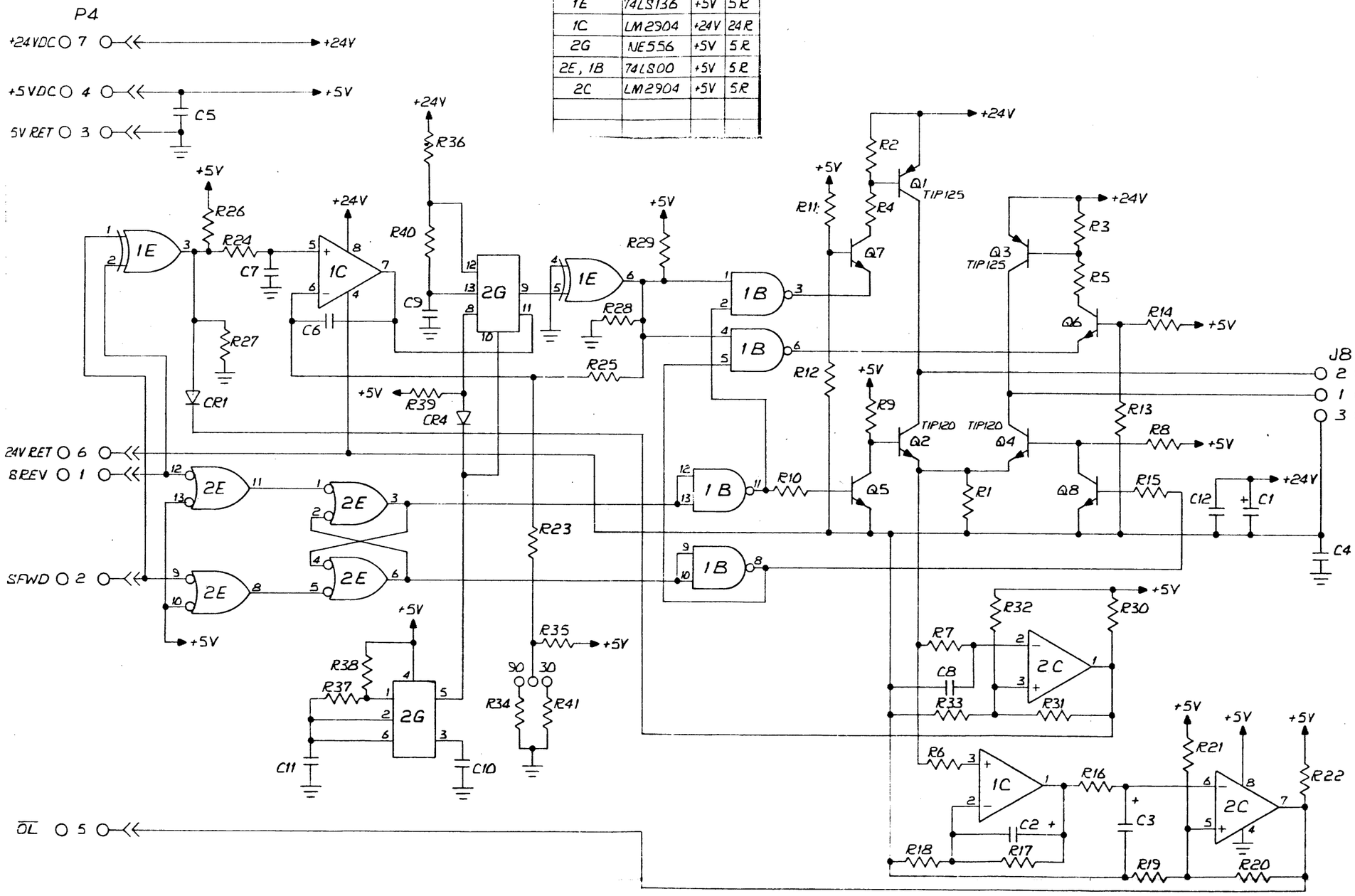


Figure A2-3. Motor Driver Board Logic Diagram

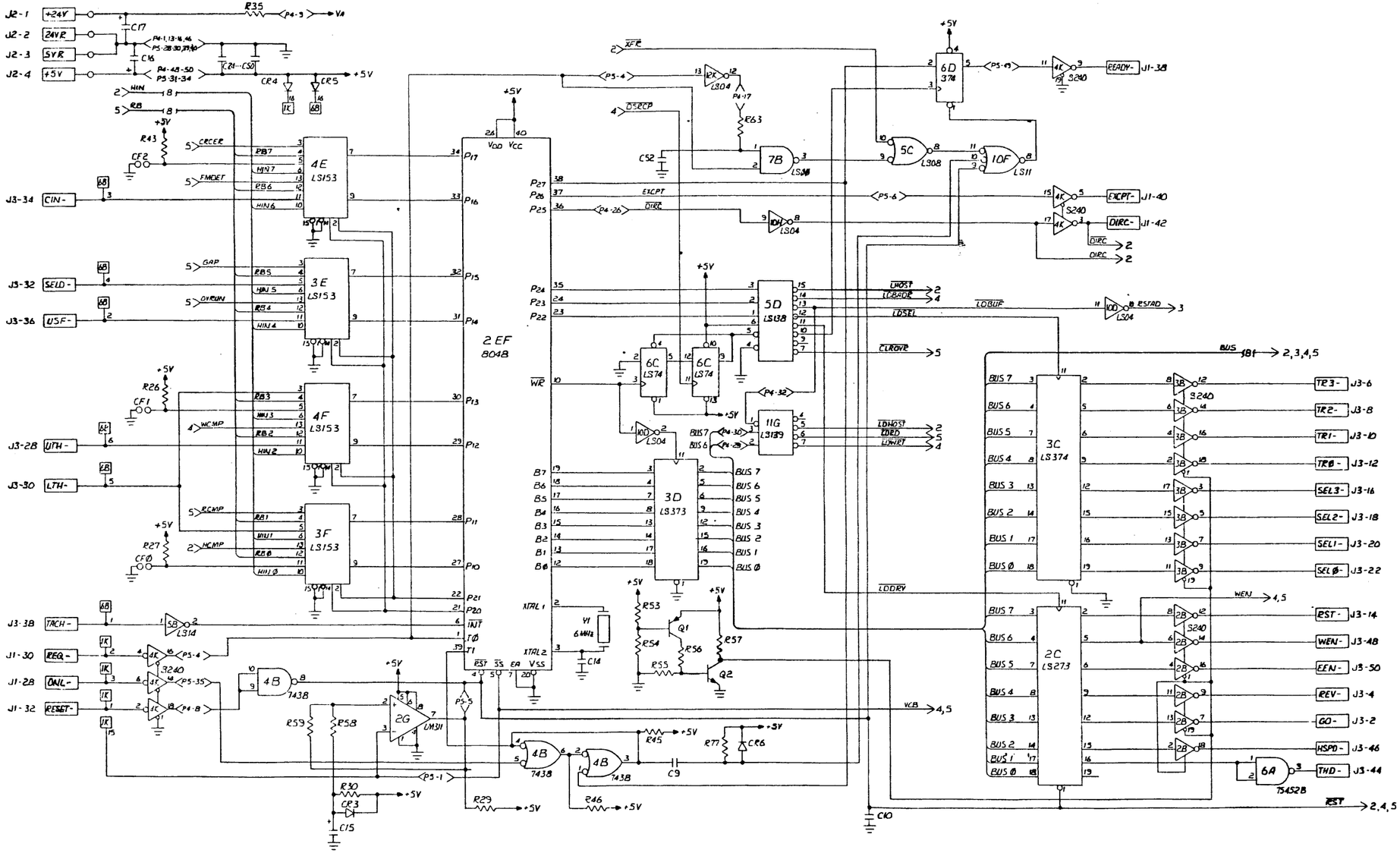


Figure A2-4. Intelligent Controller Control and Drive Interface Circuits Logic Diagram

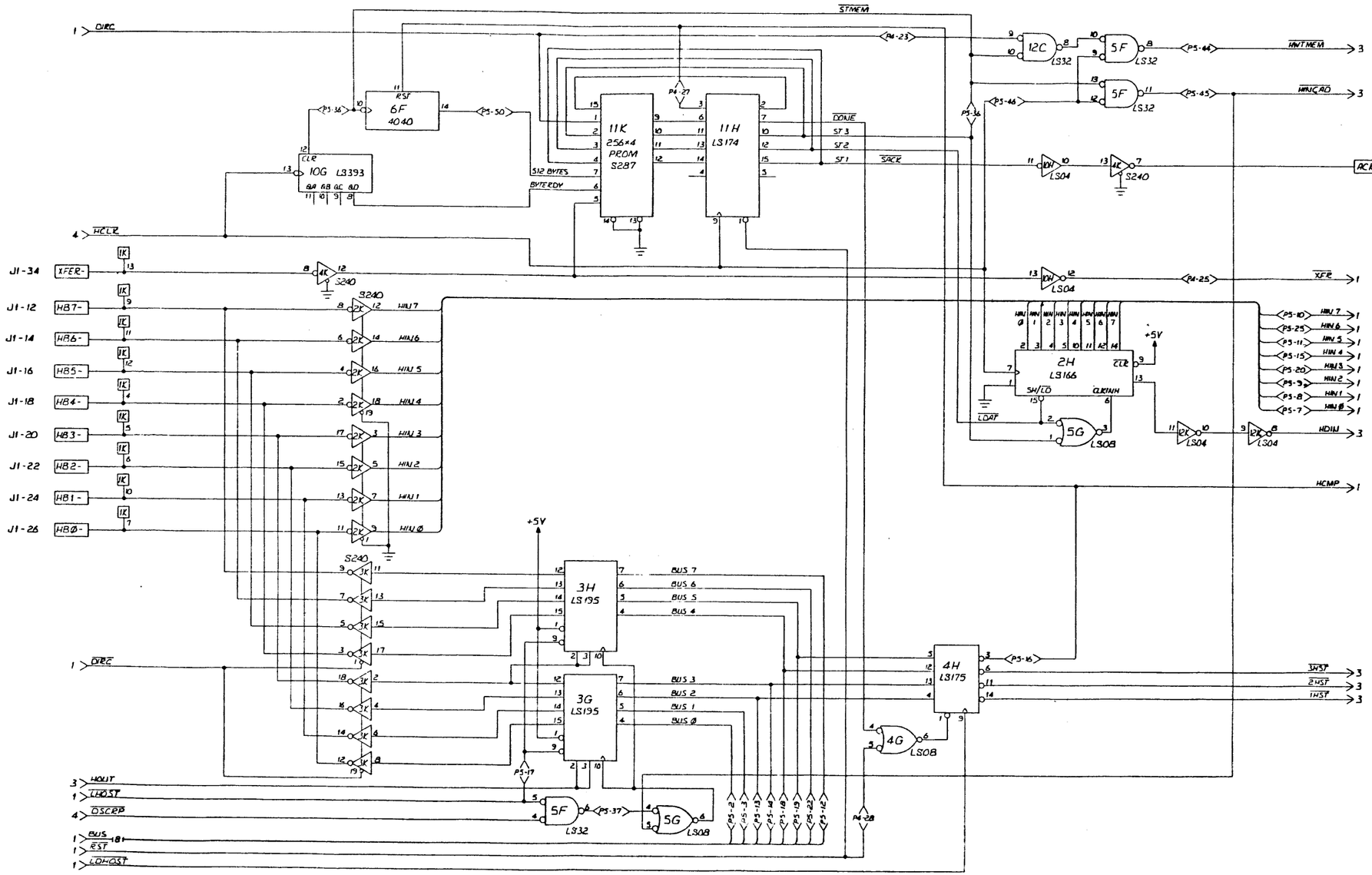


Figure A2-5. Intelligent Controller Host Interface Logic Diagram

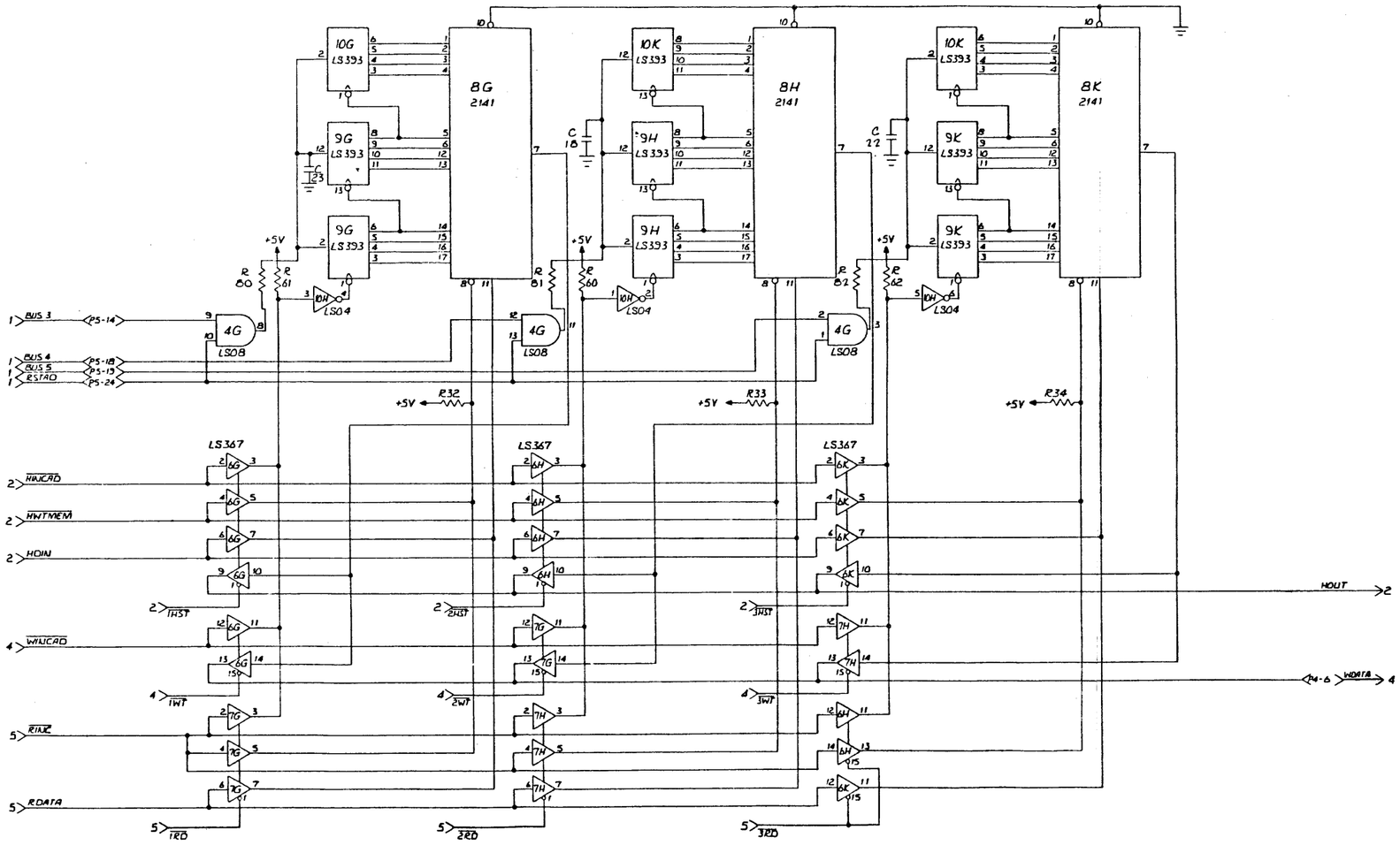


Figure A2-6. Intelligent Controller Buffer Memories Logic Diagram

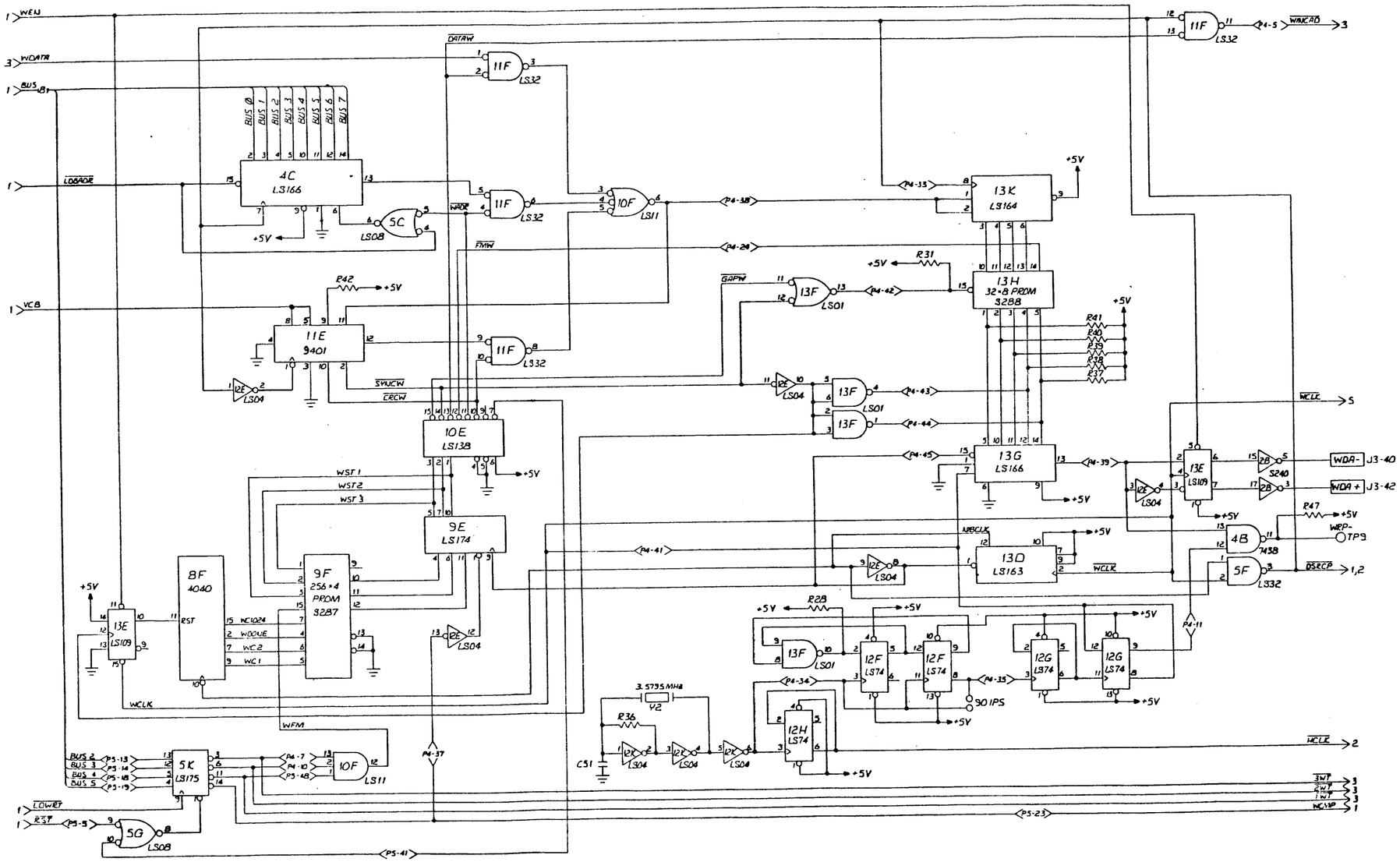


Figure A2-7. Intelligent Controller Write Logic Diagram

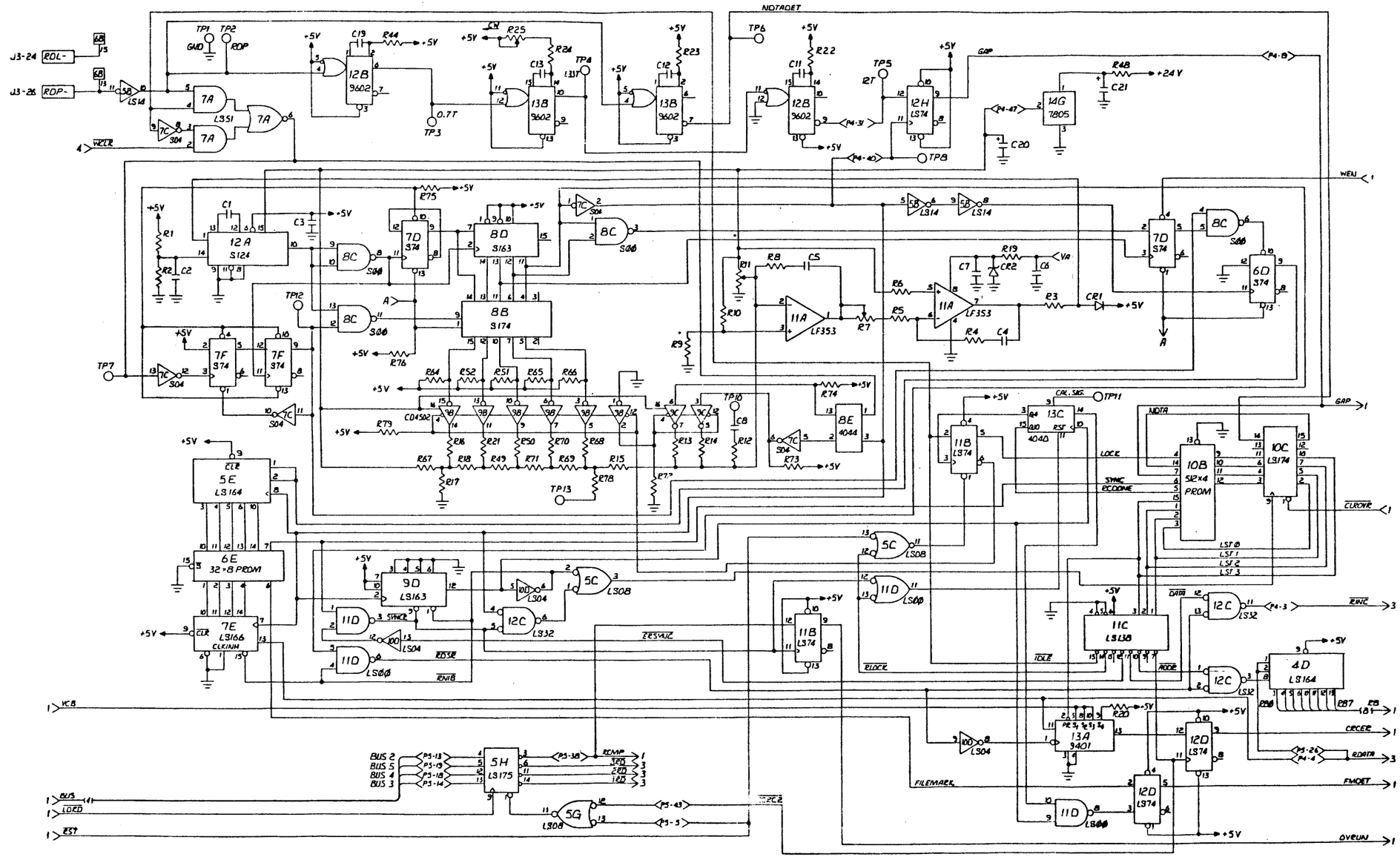


Figure A2-8. Intelligent Controller Read Logic Diagram

APPENDIX III

ADJUSTMENT AND ALIGNMENT CHECK PROCEDURE

A3.1 SCOPE

The procedures that follow consist of electrical and mechanical checks which will verfiy the proper alignment and adjustment of an Intelligent Drive. In the event that the drive fails to pass these mechanical checks, the adjustments that must be made are provided to those personnel who have been trained at Archive. Do not attempt to make mechanical adjustments unless you have been trained and have the appropriate procedures. The procedures in this appendix are used only to VERIFY the quality of the master drive and of a repaired Intelligent Drive.

A3.2 USE OF PROCEDURES

ARCHIVE CORPORATION recommends that these procedures be performed on the Master Drive as specified in Chapter 6. These procedures are also to be used to verify a repaired Intelligent Tape Drive. ARCHIVE CORPORATION will train customer personnel to effectively use the procedures to ensure the quality of an Intelligent Drive. Throughout these procedures, requirements for the MODEL 3020I are enclosed in parentheses ().

A3.3 SPECIAL TOOLS

The following special tools are required to implement the procedures in this chapter.

1. A computer system providing both power (+24 vdc and +5 vdc) and interface cabling to the tape drive.
2. Diagnostic software that includes RESET, ERASE, TENSION, WRITE, and READ capabilities.
3. Oscilloscope, Tektronix Model 465, or equivalent, with its attendant probes.
4. Potentiometer Adjustment Tool.
5. Alligator Clip for jumpering adjacent test points.
6. Jumpers for grounding test points.
7. Resistor, 100 ohm, 1/4 watt.
8. Long Nose Pliers for removing the upper Controller board, if required.
9. 14 or 16 pin I.C. Test Clip.

10. Archive Model 09C Tape Cartridge, (P/N 20121-001).

11. Track Zero Alignment Tape, ARCHIVE part number 20071-001.

12. Azimuth Alignment Tape, ARCHIVE part number 20071-002.

13. Zenith Alignment Check Tool, ARCHIVE part number 90003-001.

NOTE

Alignment tapes are precision tools and must be handled carefully. Insure proper personnel training and control procedures prior to use.

A3.4 ALIGNMENT TAPE CARE

Observe the following precautions to ensure the viability of the alignment tapes. Alignment tapes are issued by ARCHIVE CORPORATION in sets (a minimum of two). Upon receipt of alignment tape sets mark one tape in each set as a reference tape. Mark the other tapes as working tapes.

1. Store reference tape in a secure area.

2. Use the working tape to verify the Master Control Drive. Do not use the working tape as a test tool on all units.

3. Always keep the working tape in a clean container in an area free from magnetic fields (electric motors, transformers, tools, etc.) when not in the Master Control Drive.

4. Always cycle alignment tapes from BOT to EOT without stops.

5. Periodically verify working tapes by using them to verify the Master Control Drive and then reverifying the Master Control Drive with the reference tape. Contact ARCHIVE CORPORATION immediately when this procedure results in discrepancies.

6. Use alignment tapes under controlled temperature conditions (25±3 °C).

A3.5 ELECTRICAL ADJUSTMENTS

These adjustment procedures verify three of the four potentiometer settings. It also checks the timing of some additional signals. These adjustments are performed with input power applied. They do not require the installation of a tape cartridge.

The Basic Drive need not be selected for the measurements performed on the drive, but will require SELECT- to enable the drive signals to the controller while measuring the controller. Selection of the Basic Drive is either established and maintained by the computer or may be performed by jumpering any of the following points to ground.

J1-22
01A09
01D11
01D13
02B05
02B08

A3.5.1 Differentiator Symmetry/Balance (R27) (Figure A3-1)

This check is a verification of the symmetrical balance of the differentiator. The check is performed by monitoring the Read Data Pulse (RDP) at TP7 on the Basic Drive main board, (P/N 20068-X01). This check requires that the R27 potentiometer be turned in both directions to verify the adjustment.

1. Oscilloscope Settings:

   SYNC: INT POS 200NS(500NS) CH 1
   CHAN 1: AC 1V
   MODE: Channel One Only
   CHAN 1 PROBE: TP7 (on Basic Drive). Signal is RDP.
   NOTE: Set ground on the center horizontal graticule

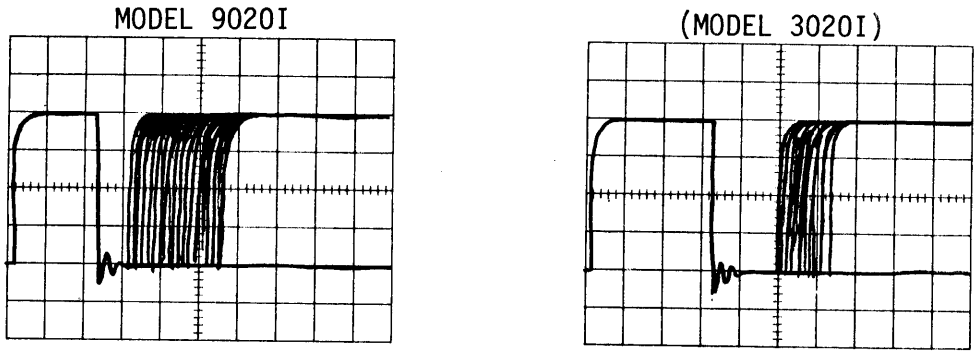


Figure A3-1. Differentiator Symmetry/Balance

2. Adjust the R27 potentiometer, in both directions, and verify that the signal waveform is at its maximum negative position/level.

A3.5.2 Read Data Pulse (RDP) Timing (Figure A3-2)

This check is a verification of the RDP One-Shot Timing. The requirement is that the timing be one-half of a cell time, ±30%.

1. Oscilloscope Settings:

   SYNC: INT POS 100NS(200NS) CH 1
   CHAN 1: AC 1V
   MODE: Channel One Only
   CHAN 1 PROBE: TP7 (on Basic Drive). Signal is RDP.

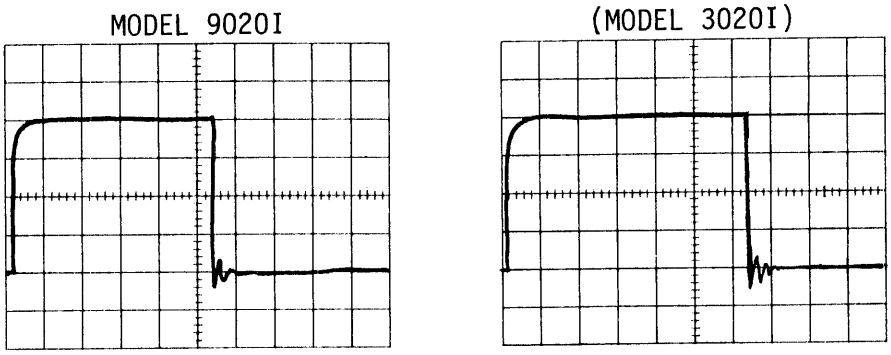


Figure A3-2. Read Data Pulse Timing

2. Verify that the timing of the pulse is within the following tolerances:

   MODEL 9020I - 550±55 nanoseconds (495 - 605 ns)
   MODEL 3020I - 1300±130 nanoseconds (1170 - 1430 ns)

A3.5.3 Read Data Level (RDL) Timing (Figure A3-3)

This check is a verification of the RDL One-Shot Timing. This requirement is that the timing be one-half of a cell time, ±10%.

1. Oscilloscope Settings:

   SYNC: INT POS 100NS(200NS) CH 1
   CHAN 1: AC 1V
   MODE: Channel One Only
   CHAN 1 PROBE: 4E7 (on Basic Drive). Signal is RDL.

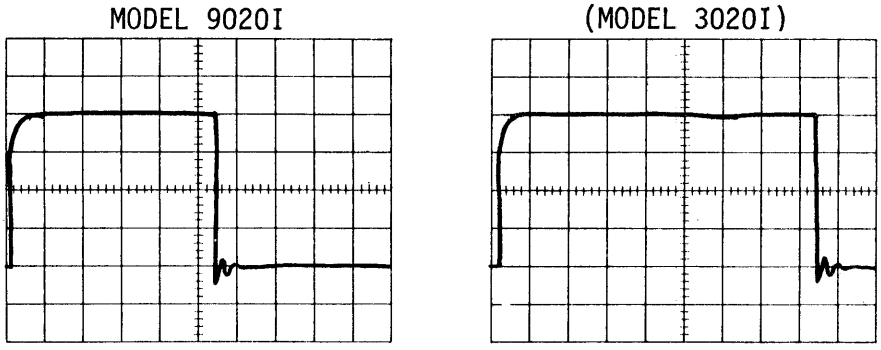


Figure A3-3. Read Data Level Timing

2. Verify that the timing of the pulse is within the following tolerances:

   MODEL 9020I - 550±55 nanoseconds (495 - 605 ns)
   MODEL 3020I - 1600±166 nanoseconds (1495 - 1825 ns)

A3.5.4 Gap One-Shot (R25) Timing (Figure A3-4)

This check is a verification of the Gap One-Shot Timing. The timing check is performed by monitoring TP4 on the controller board (P/N 20099-X01). The adjustment is performed via the R25 potentiometer which is located on the side of the controller, underneath the upper portion.

1. Select the Basic Drive.

2. Oscilloscope Settings:

   SYNC: INT POS 200NS(500NS) CH 1
   CHAN 1: DC 1V
   MODE: Channel One Only
   CHAN 1 PROBE: TP4 (on Intelligent Controller). Signal is GAP O/S.

3. Verify that this timing of the pulse is within the following tolerances:

   MODEL 9020I - 1480±40 nanoseconds (1440 - 1520 ns)
   MODEL 3020I - 4440±120 nanoseconds (4320 - 4560 ns)

4. Adjust R25 as required. The trailing edge may have some minute "jitter". Center the "jitter" on the required minor division mark.

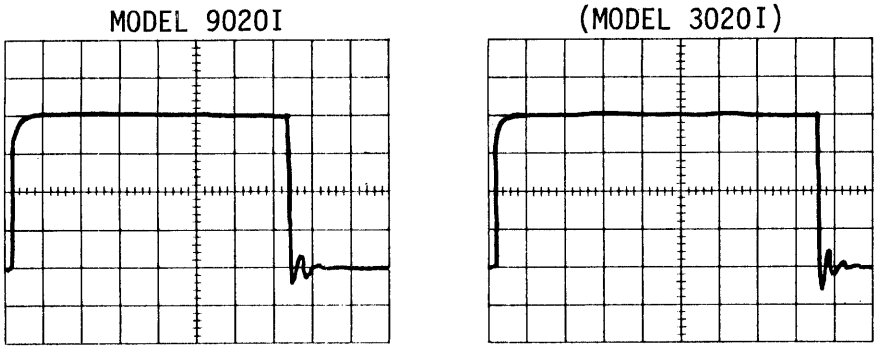


Figure A3-4. Gap One-Shot Timing

A3.5.5 Phase Locked Loop Gain (R7)

This check verifies the gain setting of the Phase Locked Loop (PLL). The check is performed by monitoring the Read Clock at TP8 and injecting a calibration signal into the PLL. The adjustment is made via the R7 potentiometer located on the front of the controller, behind the Basic Drive main board.

1. Select the Basic Drive.

2. Jumper TP10 to TP11. The test points are located underneath the Basic Drive input power connector. An alligator clip may be used for more convenience.

3. Jumper the negative side of resistor R79 to ground. Resistor R79 is located between the integrated circuits at 09B and 10B (figure A3-5).

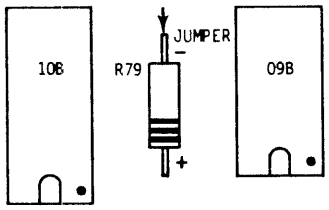


Figure A3-5. Jumper Connection to R79

4. Oscilloscope Settings:

   SYNC: INT POS 100NS(200NS) CH 1
   CHAN 1: DC 1V
   MODE: Channel One Only
   CHAN 1 PROBE: TP8 (on Intelligent Controller). Signal is RDCLK.
   NOTE: Uncalibrate the time base. Vary the time base to display the entire signal, including all the "jitter", on the screen (figure A3-6).

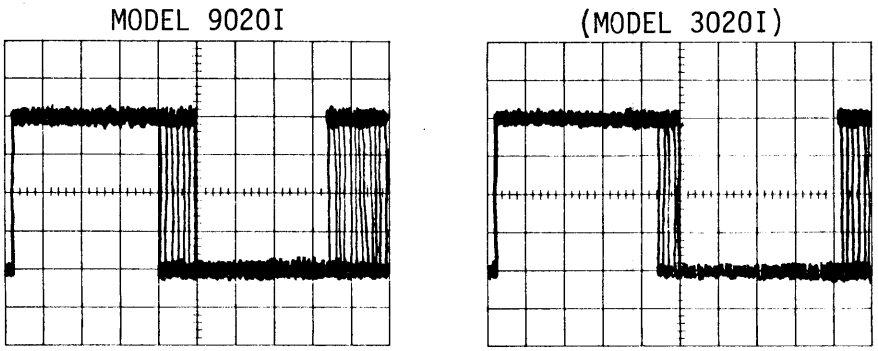


Figure A3-6. Phase Lock Loop Gain

5. Horizontally position the leading edge on the first left hand graticule and verify that the entire signal with all of its "jitter" is displayed (figure A3-6).

6. Verify that the leading edge of the second pulse is within the following tolerances:

   MODEL 9020I - 8.4±0.1 Division (8.3 - 8.5 Divs)
   MODEL 3020I - 9.2±0.1 Division (9.1 - 9.3 Divs)

7. Adjust R7 as required. Adjust by turning the potentiometer one turn at a time. Verify that the entire signal is displayed by manipulating the horizontal position to locate the leading edge and the time base for the last of the second set of leading (raising) edges.

8. Remove the jumpers from TP10, TP11, and R79 after the check/adjustment is completed.

A3.6 BASIC OPERATIONS

These tests address the basic operations criteria of the drive. They require that the drive responds to and executes computer issued commands.

1. Execute a Read Status command without a tape cartridge installed. The unit should respond with No Cartridge and Write Protected.

2. Install an Archive Model 09C Tape Cartridge with Safe indicator positioned to inhibit writing (Safe).

3. Execute a Read Status command. The unit should respond with Cartridge In and Write Protected.

4. Remove the Archive Model 09C. Tape Cartridge and rotate the Safe indicator to enable writing.

5. Execute a Read Status command. The unit should respond with Cartridge In and Write Enabled.

6. Execute a Rewind command to position the tape at BOT (Beginning of Tape).

7. Execute an Erase command. The unit will respond by performing an Erase from BOT to EOT (End of Tape) and a Rewind from EOT to BOT (approximately two minutes).

A3.6.1 Capstan Motor Noise Check (Figure A3-7)

This check verifies that the capstan motor does not create excessive noise. The check is performed by reading an erased tape and monitoring the output of the differentiator for excessive noise spikes.

1. Oscilloscope Settings:

```
SYNC:  INT   NEG    1MS(500uS)   CH 1
CHAN 1:       DC    2V
CHAN 2:       AC  200MV
MODE:  Alternate
CHAN 1 PROBE:  6C1 (on Basic Drive).  Signal is TACH.
CHAN 2 PROBE:  TP4 (on Basic Drive).  Signal is DIFFOUT.
NOTE:  The MODEL 9020I will display 7 pulses @ 1 ms
       The MODEL 3020I will display 5 pulses @ 500 us
```

2. Execute a Tension command. The unit will move tape from BOT to EOT and back to BOT (approximately two minutes).

3. Uncalibrate the time base. Vary the time base to display eight pulses across screen, i.e., one revolution of the capstan motor.

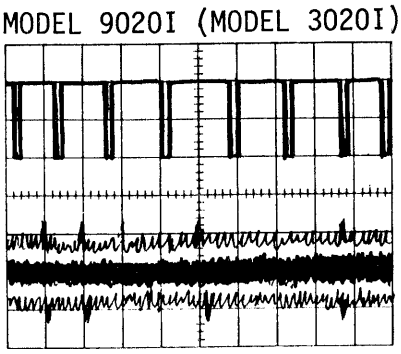


Figure A3-7. Capstan Motor Noise Check

4. Verify that the noise spikes do not exceed ±250 millivolts peak (500 mv peak-to-peak). The noise spikes will be asynchronous with the tachometer pulses.

NOTE

The next step is to check the Capstan Motor Speed Variation while executing a Write command. The check can be performed during any Motion command, ERASE, TENSION, WRITE, READ, or REWIND on the MODEL 9020I. It can only be performed on a MODEL 3020I during a WRITE or READ as that is the only time the micro-computer regulates the capstan motor at 30 ips. All other Motion commands are performed in an unregulated mode at 90 ips. It is useful to establish a write data pattern that can be used for the remainder of this test. The following data patterns result in a specific number of flux reversals per inch (FRPI), A5, 29, and CF. The optimum write data buffer would be 170 bytes of A5, 170 bytes of 29, and 172 bytes of CF (512 bytes total). If possible, establish the optimum pattern. If not, establish the write buffer with 512 bytes of A5. A5 represents a one-half frequency (5000 FRPI) whose amplitude when divided into the full-frequency amplitude of the all ones (at 10000 FRPI) written by the drive during GAP time, provides a resolution ratio. Twenty-nine represents a one-third frequency (3300 FRPI) whose

amplitude divided in the full-frequency amplitude of all the ones (at 10000 FRPI) also provides a resolution ratio. CF is a worst case data pattern that combined with a 29 pattern exercises the units ability to accommodate peak shift.

A3.6.2 Capstan Motor Speed Variation (Figure A3-8)

This check verifies that the capstan motor is under the control of the micro-computer and does not exhibit excessive speed variation. This check is performed by monitoring the tachometer pulses to the micro-computer during the execution of a Motion command.

1. Oscilloscope Settings:

   SYNC: INT NEG 200uS CH 1
   CHAN 1: DC 2V
   MODE: Channel One Only
   CHAN 1 PROBE: 6C1 (on Basic Drive). Signal is TACH.

2. Execute a Write command. Write from Beginning of Media (BOM) to End of Media (EOM). At the conclusion of the Write, ensure that a File Mark is written.

3. Horizontally position the second negative pulse on the center vertical graticule and magnify the display times ten (10X).

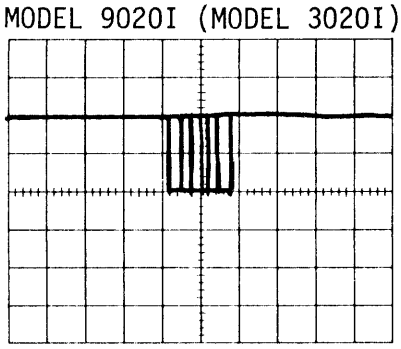


Figure A3-8. Capstan Motor Speed Variation

4. Verify the total "jitter" does not exceed six vertical graticules (±3 Divisions) for the entire length of the tape in both directions.

5. At the conclusion of the Write sequence, note and record the following:

   Total number of Blocks/Bytes Written
   Total number of Blocks/Bytes Rewritten

NOTE

The number of blocks rewritten is provided via the read status data. The number of blocks rewritten divided by two equals the actual number of rewrites that occurred. Verify that the number of rewrites do not exceed 100.

A3.6.3 Resolution Check (Figure A3-9)

This check verifies the resolution of the read/write heads and is provided as a troubleshooting aid, not a specification check.

The objective is to measure the playback amplitudes of three basic frequencies, i.e., 10000 FRPI, 5000 FRPI, and 3300 FRPI.

The 10000 FRPI is always available under GAP. The 5000 FRPI is created by writing a data pattern of A5. The 3300 FRPI is created by writing a data pattern of 29.

1. Oscilloscope Settings:

   SYNC: INT POS 50uS CH 1
   CHAN 1: DC 5V
   CHAN 2: AC 200MV
   MODE: Alternate
   CHAN 1 PROBE: TP5 (on Intelligent Controller). Signal is GAP.
   CHAN 2 PROBE: TP1 (on Basic Drive). Signal is RDAMP.

2. If required, execute a Write command writing blocks of data consisting of A5.

3. Execute a Read command. Read and record the amplitude of the data on both sides of the trailing (falling) edge of GAP.

MODEL 9020I (MODEL 3020I)

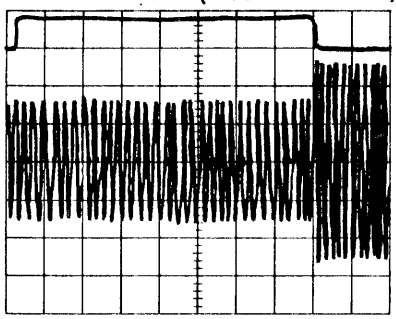


Figure A3-9. Resolution Check

4. Perform the measurement in both directions.

5. Repeat the last three steps with a data pattern of 29.

6. Develop the resolution by taking the ratio of each of the lower frequency, higher amplitude signals and dividing them into the high frequency, low amplitude signal. Then multiply by a 100 to convert to percentages.

7. Verify that the difference between the heads is less than 20 percent. A typical example is shown as follows.

Amplitudes	GAP	A5	29	GAP/A5	GAP/29
Forward	800MV	1300MV	1400MV	61%	57%
Reverse	750MV	1200MV	1300MV	63%	58%
Delta	50/750 = 7%	100/1200 = 8%	100/1300 = 8%		

8. Verify that the amplitude measured and resolutions developed are within the following tolerances.

		MODEL 9020I	(MODEL 3020I)
Amplitudes:	GAP	400-1100MV	160-440MV
	A5	725-1570MV	290-625MV
	29	850-1690MV	340-675MV
Resolutions:	GAP/A5	55 to 70%	
	GAP/29	47 to 65%	

A3.6.4 Phase Lock Loop (PLL) Balance (R11) (Figure A3-10)

This check is a verification of the Phase Lock Loop (PLL) Balance. The check is performed by monitoring the output of the digital to analog converter (DAC) at TP13 while the drive is either reading or writing. TP13 is located on the controller.

The adjustment is made via the R11 potentiometer. R11 is the second potentiometer mounted inboard from R7 which is located at the front of the controller.

1. Oscilloscope Settings:

   SYNC: INT POS 50uS CH 1
   CHAN 1: DC 5V
   CHAN 2: AC 100MV
   MODE: Alternate
   CHAN 1 PROBE: TP5 (on Intelligent Controller). Signal is GAP.
   CHAN 2 PROBE: TP13 (on Intelligent Controller). Signal is DAC.

2. Execute a Read command. Read an adequate number of blocks to ensure readings/measurements in both directions, i.e., read from both the forward head and reverse head.

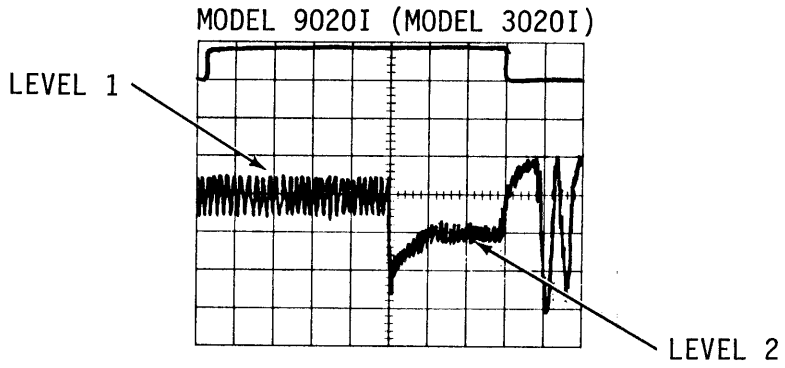


Figure A3-10. Phase Lock Loop Balance

3. Verify that the second level is negative in respect to the first level and that the difference between them is 100 millivolts (0.1V) as measured through the center of the "fuzz".

4. Adjust R11 as required to set the difference between the two levels at 100 millivolts (0.1V).

5. Switch the oscilloscope coupling to dc and verify that the second level is at 2.4 vdc.

A3.6.5 Peak Shift Check (Figure A3-11)

This check verifies that the PLL accommodates peak shift. The check is performed by monitoring the output of the PLLs DAC. The objective is to verify that the error signals from the DAC do not exceed the requirements while reading a worst case peak shift pattern.

1. Oscilloscope Settings:

   SYNC: INT POS 500uS CH 1
   CHAN 1: DC 5V
   CHAN 2: AC 100MV
   MODE: Alternate
   CHAN 1 PROBE: TP5 (on Intelligent Controller). Signal is GAP.
   CHAN 2 PROBE: TP13 (on Intelligent Controller). Signal is DAC.
   NOTE: Uncalibrate the time base. Vary the time base to display a GAP pulse at each end of the screen. The Channel 2 display will then depict one entire 528.5 byte block.

2. If required, execute a Write command with the write buffer set to the combination of 29 and CF, i.e., 50 bytes of 29, 50 bytes of CF, etc., throughout the buffer. Figure A3-11 is based on A5, 29, CF buffer of approximately 170 bytes each.

3. Execute a Read command of adequate block/byte length to facilitate a reading in both directions.

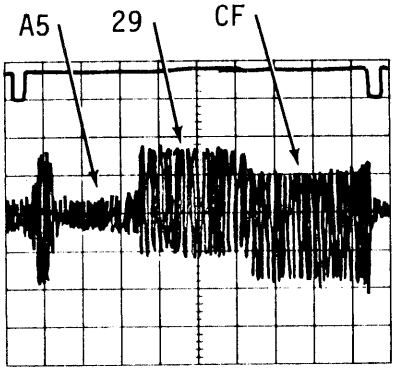


Figure A3-11. Peak Shift Check

4. Verify that the maximum peak-to-peak amplitudes achieved by the combination of 29 and CF does not exceed 1700 millivolts (1.7V) in both directions. The measurement is taken from the top of the 29 pattern to the bottom of the CF pattern and excludes or discounts the minute spikes exceeding the body of the waveform.

A3.6.6 Read Playback Verification Check (Figure A3-12)

This check is a verification of the read playback. This check is performed while monitoring the playback amplitude of the all one's frequency that occurs during the GAP time between the actual blocks of user data. The frequency of this all one's area is 10000 FRPI. Its amplitude is therefore the lowest peak-to-peak value of all the possible data patterns/frequencies.

1. Oscilloscope Settings:

   SYNC: INT POS 50uS CH 1
   CHAN 1: DC 5V
   CHAN 2: AC 200MV
   MODE: Alternate
   CHAN 1 PROBE: TP5 (on Intelligent Controller). Signal is GAP.
   CHAN 2 PROBE: TP1 (on Intelligent Controller). Signal is DAC.

2. Execute a Read command. Read an adequate number of blocks/bytes to take readings/measurements of the playback amplitude in both directions, i.e., read from both the forward head and the reverse head.

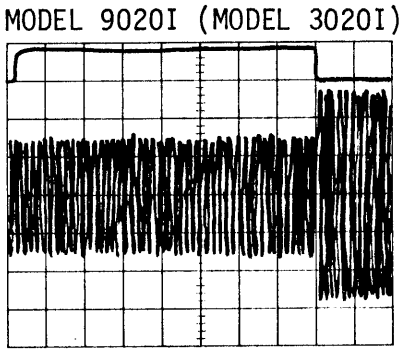


Figure A3-12. Read Playback Verification

3. Verify that the read playback during GAP is within the following tolerances:

   MODEL 9020I - 400 to 1100 millivolts in both directions
   MODEL 3020I - 160 to 440 millivolts in both directions

4. Note and record the values of the playback amplitudes in both directions.

5. Verify that the amplitudes of each head are within 20 percent of each other, i.e., divide the differences between them by the lesser of the two values and multiply by a 100.

A3.7 ALIGNMENTS

There are three mechanical checks; zenith, vertical track position, and azimuthal. Zenith is checked with a tool. Vertical track position and azimuthal alignment checks require a special reference tape cartridge.

A3.7.1 Zenith

The zenith alignment check verifies that the forward (front) face of the read/write head is parallel to the vertical tape path. In other words, zenith is the slope or lean of the read/write head as it addresses the tape. Positive zenith would indicate that the head is sloped backwards from the vertical tape while negative zenith would indicate that the head is leaning forward into the vertical tape.

1. Insert the Cartridge Base.
2. Insert the Zenith Tool.
3. Place the face of the tool between the two read/write heads.
4. Apply a light pressure to maintain the face of the tool on the face of the head.
5. Verify that the zenith of the read/write head is within ±15 minutes (±1 division on the zenith check tool).

CAUTION

Both of the reference tape cartridges required for the following procedures are manufactured by Archive under stringently controlled conditions and are intended for use by Archive trained and qualified personnel under the auspices of a constant calibration and correlation program. The program assures that the integrity of the reference tapes are maintained since indiscriminate use of these tapes may result in erroneous conclusions regarding the integrity of the alignment checks.

A3.7.2 Vertical Track Position (Figure A3-13)

The objective of the vertical track position check is to verify that the read/write head is properly positioned during the read/write operations.

A Vertical Track Position Reference Tape Cartridge is required. This tape has been written full width with an erase head at 5000 FRPI. The Track Zero position on the tape, with the exception of the first 75 feet, has been erased with a read head. The result is a Track Zero null.

1. Oscilloscope Settings:

   SYNC: INT POS 5uS CH 1
   CHAN 1: AC 500MV
   MODE: Channel One Only
   CHAN 1 PROBE: TP4 (on Basic Drive). Signal is DIFFOUT.
   NOTE: Set ground on center graticule. The voltage base is selectable as it will be necessary to adjust the playback observed to full scale.

2. Execute a Tension command.

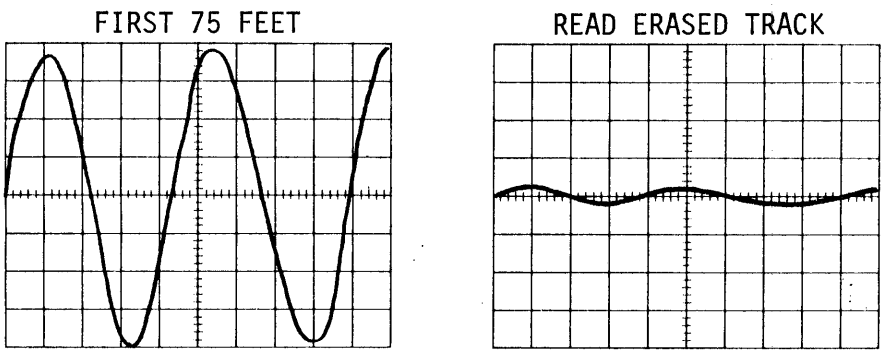


Figure A3-13. Vertical Track Position

3. Set amplitude of playback observed for the first 75 feet (10 seconds for 90 ips, 30 seconds for 30 ips) to eight divisions (maximum vertical deflection).

4. Verify that the output for reading the erased Track Zero is less than 0.6 division for both the forward and reverse directions in both horizontal and vertical mounting positions.

A3.7.3 Azimuthal Alignment Check (Figure A3-14)

The azimuth check verifies that the read/write head is perpendicular to the tape path.

An Azimuth Reference Tape is required. This tape has a 15000 FRPI signal recorded on Track Zero only. The rest of the tape has been erased.

The objective of this check is to verify that the read/write head does not have excessive azimuthal arc. This is done by verifying that the read head playback amplitude is at, or near, its peak (maximum) and that any movement of the head will result in a decrease in amplitude while reading the azimuth reference tape.

1. Oscilloscope Settings:

   SYNC: INT POS 5uS
   CHAN 1: AC 100-200MV
   MODE: Channel One Only
   CHAN 1 PROBE: TP4 (on Basic Drive). Signal is DIFFOUT.
   NOTE: Set ground on control graticule. The voltage base is selectable as it will be required to adjust the observed playback for six divisions.

2. Execute a Tension command.

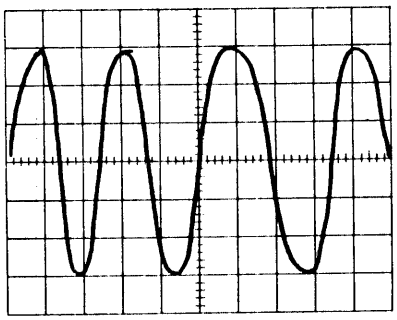


Figure A3-14. Azimuth Alignment Check

3. Apply finger point pressure to the base of the stepper motor at two points, on each side.

4. Verify that the playback amplitude decreases in all cases.

5. Should the amplitude increase, note and record the point at which pressure on the stepper motor base resulted in the increase, i.e., inside or outside and how much the signal increased.

6. Verify that the increase in amplitude was less than one-half minor division, zero to peak (not peak-to-peak).

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