# American National Standard

for information systems –

# storage module interfaces

ANSI X3.91M-1987

american national standards institute, inc.
1430 broadway, new york, new york 10018

ANSI®
X3.91M-1987
Revision of
ANSI X3.91M-1982

# American National Standard for Information Systems –

# Storage Module Interfaces

Secretariat

**Computer and Business Equipment Manufacturers Association**

Approved November 21, 1986

**American National Standards Institute, Inc**

## Abstract

This standard defines stringent mechanical, electrical, and functional requirements for attaching disk drives to their control unit. A subset configuration is compatible with that defined by the original standard, ANSI X3.91M-1982. This revised version allows extensions from 10 to 24 Mbits per second and revises the definitions of optional extensions. The resulting interface facilitates the interconnection of high-performance disk drives and the control unit and thus provides a common device interface specification for both controller and drive suppliers.

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# Foreword (This Foreword is not part of American National Standard X3.91M-1987.)

The Storage Module Drive (SMD) interface was first proposed as a standards project in 1977. As a result of that proposal, task group X3T9.3 was formed to develop device-level interface standards. The SMD interface standard was completed by X3T9.3 and published by ANSI in 1982 as American National Standard for Information Systems — Storage Module Interfaces, ANSI X3.91M-1982.

The SMD interface has proved to be one of the most important and longest lasting interfaces in the Original Equipment Manufacturer (OEM) market. The mandatory portions of the standard have been widely used on a broad range of disk drives.

However, the optional portions of the original standard were not employed by many implementors. The 1982 version of the standard had a maximum transfer rate requirement of 10 megabits per second (Mbits/s). Newer systems have application requirements for higher transfer rates than the original standard provided for. More recent designs are able to accomodate the needs for higher-performance magnetic disk drives. These factors led to a project to update ANSI X3.91M-1982.

For the revised SMD standard, it was not necessary to form a committee since X3T9.3 was still operating with experts familiar with the SMD interface. In fact, several members of the group that developed the original American National Standard on SMD interface were still active within X3T9.3.

This revised standard provides for the higher transfer rate capability, replaces several of the optional features with more generic, capability-matching, preferred techniques, and corrects inadvertant errors in the phase relationship of the clock signals and in the dimensions for the round cable connectors. At the same time, the revised standard allows for the original lower transfer rate implementations as well as known implementations of the original optional features.

Several interface standards, which describe the requirements for attractive alternate interfaces, have been developed since the publication of ANSI X3.91M-1982. However, the very large, installed base of software customized for the American National Standard on SMD interface, as well as a large body of technical know-how, was ample justification for publication of the revised standard.

Suggestions for improvement of this standard will be welcome. They should be sent to the Computer and Business Equipment Manufacturers Association, 311 First Street, NW, Suite 500, Washington, D.C. 20001.

This standard was processed and approved for submittal to ANSI by Accredited Standards Committee on Information Processing Systems, X3. Committee approval of the standard does not imply that all committee members voted for approval. At the time it approved this standard, the X3 Committee had the following members:

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# American National Standard for Information Systems –

# Storage Module Interfaces

## 1. Scope

This American National Standard is a revision of American National Standard for Information Systems - Storage Module Interfaces, ANSI X3.91M-1982. This standard provides mechanical, electrical, and functional requirements for the storage module class of interface between disk drives and their respective control units. To obtain total interchangeability of such disk drives, an operational manual should be developed. Neither the operational nor ac-power requirements are part of this standard. The design of the interface provides the following important features:

(1) Addressability of up to 16 disk drives
(2) Capability for both variable and fixed sector sizes
(3) Capability for daisy-chain or radial configuration of control signals with radial configuration of data signals
(4) Data transfer rates across the interface of up to 24 megabits/second (Mbits/s)
(5) Extended cylinder addressing capabilities
(6) Extended disk drive status and diagnostic capabilities

The first four features were documented in ANSI X3.91M-1982 for transfer rates up to 10 Mbits/s. This newer version of the standard has extended the maximum transfer rate and added features (5) and (6). These optional enhancements are intended to facilitate downward compatibility. This standard provides a functional description of the interface lines together with electrical and mechanical requirements.

The mechanical and electrical requirements for the interface are defined in Section 3. Section 4 specifies the logical definition of each signal line. Section 5 develops the timing characteristics of each operation at the drive. Section 6 specifies the definition of optional features (5) and (6) and provides information for downward compatibility between the extended and earlier versions of this standard.

This standard is distinct from a specification in that it delineates a minimum, rather than a specific, set of requirements consistent with compatibility and interchangeability of drives.

In this standard, the terms "disk drive," "device," and "drive" are equivalent.

## 2. Definitions

The terms used in this standard shall be defined as shown in the American National Dictionary for Information Processing, ANSI X3/TR-1-77. Terms not covered in ANSI X3/TR-1-77 are defined as follows:

**asserted.** A signal is asserted when it is driven to a "true" or "one" value. Tables 1 and 2 show the signal polarities for the asserted condition for each signal. A signal may be either asserted, negated (the "false" or "zero" value), or in a high impedance state.

**enabled.** A signal is enabled when it is permitted to actively assert or unassert a signal line. Three-state drivers that are not enabled enter the high impedance state.

**original equipment manufacturer (OEM).** This term, when applied to disk drives, means a drive that is first built by a disk drive manufacturer, then sold to a system vendor who typically integrates the drive with a computer or control unit, and then resold to an end user. This is distinct from a drive that is built, integrated into a computer system, and sold to an end user all by the same manufacturer.

**PLO synchronization.** This term means "Phase-Lock-Oscillator synchronization."

**rotational position sensing.** This is a mechanism for detecting the angular position of a reference point on the media with respect to the recording heads.

**stranded conductor.** A stranded conductor is a conductor composed of a group of small wires usually twisted or braided together.

**three-state.** When applied to signal drivers, three-state indicates a device that can be in one of the following three states:

(1) Driving the signal to the asserted value
(2) Driving the signal to the unasserted or "negated" value
(3) A high impedance state that effectively removes the driver from the signal line

**twinax.** Twinax is a twisted pair in coaxial configuration.

**write splice.** This is the point on the media in which the head current is turned on or off during a WRITE sequence.

## 3. Physical Characteristics

Unless otherwise indicated, all values include a ±5% tolerance. Signals are assumed to propagate at 70% the speed of light in all cables.

**3.1 Cabling Configuration.** The disk drives are connected to a control unit by means of a READ/WRITE cable, a CONTROL cable, and a dc ground cable. Delivery of primary ac power cannot be accomplished on any of these cables and is not described in this standard. A READ/WRITE cable connects each drive directly to the control unit. The maximum length of any READ/WRITE cable shall be 15 meters. A CONTROL cable can connect each drive directly to the control unit (as in Figures 1a and 1b) or via other drives in a daisy-chain configuration (as in Figures 2a and 2b). The cumulative length of the CONTROL cables on a given string shall not exceed 30 meters. For data transfer rates up to 10 Mbits/s, a separate dc ground may be provided. For data rates greater than 10 Mbits/s, a dc ground should be provided. Detailed implementation of this grounding requirement is not a subject of this standard. Refer to the manufacturer's recommendations for specific power/ground information.

**3.2 Connector Characteristics**

**3.2.1 CONTROL Cable**. Control and status information is exchanged between the drive and a control unit via the CONTROL cable. Pin assignments and signal polarities shall be as defined in Table 1. The signal polarities correspond to the asserted state. All pins are enumerated in Table 1. Essential signals shall be as defined in Section 4. Optional signals (those referenced to footnote 6 in Table 1), if implemented, shall be as defined in Section 6.

Either of the following two cable-connector configurations is acceptable for the CONTROL cable. The first connector type is the 75-pin rectangular connector illustrated in Figure 3. It is used with round, multiple-twisted-pair cable. The second connector type is the 60-pin, two-row, inline connector illustrated in Figures 4 and 5. It is used with flat-ribbon, multiple-twisted-pair cable. Characteristics of these cables shall be as described in 3.3.1 and 3.3.2.

To allow for the daisy-chain configuration, each drive shall provide two CONTROL cable connectors, one toward and one away from the control unit. With the exception of PICK, all signals shall be carried through from one connector to the other, as well as connected to internal electronics, as appropriate. If implemented, the unidirectional nature of PICK shall be as defined in 6.3. The transmission-line "stub" in each drive shall not exceed 1 meter in length.

**3.2.2 READ/WRITE Cable**. READ/WRITE DATA, bit synchronization information, and certain dedicated status lines shall be exchanged between the drive and a control unit via the READ/WRITE cable. These status lines shall be enabled, regardless of whether the drive is selected. Pin assignments and signal polarities shall be as defined in Table 2. The signal polarities correspond to the asserted state. All pins not defined in Table 2 are reserved for options (see Section 6).

Either of the two cable-connector combinations described previously is acceptable for the READ/WRITE cable, although the type shall correspond with the type chosen for the CONTROL cable. The first connector type is the 34-pin rectangular connector illustrated in Figure 6. It is used with round, multiple-twisted-pair cable. The second connector type is the 26-pin, two-row, inline connector illustrated in Figures 7 and 8. It is used with a flat-ribbon cable containing a ground plane. Characteristics of these cables shall be as described in 3.3.1 and 3.3.2.

Termination of the READ/WRITE cable shall be internal to each control unit and drive according to the electrical requirements of 3.4.3.

**3.3 Cable Characteristics**. Cables shall be either round, jacketed (twisted-pair or twinax and twisted-pair) or flat-ribbon configurations, depending on the input/output connectors selected. Both will be described under their appropriate sections. Round, jacketed (twisted-pair or twinax and twisted-pair) cable shall be used with rectangular cable-to-panel connectors and flat-ribbon cable shall be used with ribbon inline connectors.

**3.3.1 Round, Jacketed Cable**

**3.3.1.1 CONTROL Cable**. The round twisted-pair cable, when used, shall consist of 36 twisted pairs, a ground wire, and a shield. Each conductor of the twisted-pairs shall be 24 AWG stranded and shall exhibit a characteristic impedance of 100 ohms ± 10 ohms.

**3.3.1.2 READ/WRITE Cable.** The round twinax and twisted-pair cable, when used, shall consist of five twinax conductor pairs, four twisted pairs, and three discrete wires. The twinax conductor pairs shall have a characteristic impedance of 160 ohms ±16 ohms. The conductor shall be 28 AWG. The four twisted-pairs shall have a characteristic impedance of 100 ohms ±10 ohms. The conductor for the twisted pairs and the discrete wires shall be 26 AWG.

Table 1
CONTROL Cable ("A" Cable) Signal Locations

| Signal Name | 60-Pin Connector Asserted-State Pin Polarity | | Source | Alternate 75-Pin Connector Asserted-State Pin Polarity | |
|---|---|---|---|---|---|
| | - LO, | + HI | | - LO, | + HI |
| TAG 0 (DEVICE SELECT ENABLE) | 22, | 52 | CU | 22, | 25 |
| DEVICE SELECT 1 | 23, | 53 | CU | 1, | 4 |
| DEVICE SELECT 2 | 24, | 54 | CU | 2, | 5 |
| DEVICE SELECT 4 | 26, | 56 | CU | 3, | 7 |
| DEVICE SELECT 8/TAG 5[5] | 27, | 57 | CU | 8, | 12 |
| TAG 1[2] | 1, | 31 | CU | 46, | 49 |
| TAG 2[2] | 2, | 32 | CU | 48, | 51 |
| TAG 3[2] | 3, | 33 | CU | 52, | 55 |
| TAG 4[6] | 30, | 60 | CU | 54, | 57 |
| BUS OUT BIT 0[2,3] | 4, | 34 | CU | 23, | 26 |
| BUS OUT BIT 1[2,3] | 5, | 35 | CU | 24, | 27 |
| BUS OUT BIT 2[2,3] | 6, | 36 | CU | 28, | 31 |
| BUS OUT BIT 3[2,3] | 7, | 37 | CU | 29, | 32 |
| BUS OUT BIT 4[2,3] | 8, | 38 | CU | 30, | 33 |
| BUS OUT BIT 5[2,3] | 9, | 39 | CU | 34, | 37 |
| BUS OUT BIT 6[2,3] | 10, | 40 | CU | 35, | 38 |
| BUS OUT BIT 7[2,3] | 11, | 41 | CU | 36, | 39 |
| BUS OUT BIT 8[2,3] | 12, | 42 | CU | 40, | 43 |
| BUS OUT BIT 9[2,3] | 13, | 43 | CU | 41, | 44 |
| INTERFACE ENABLE | 14, | 44 | CU | 16, | 20 |
| BUS IN BIT 0[2,4] | 19, | 49 | Drive | 17, | 21 |
| BUS IN BIT 1[2,4] | 17, | 47 | Drive | 15, | 18 |
| BUS IN BIT 2[2,4] | 16, | 46 | Drive | 75, | 78 |
| BUS IN BIT 3[2,4] | 15, | 45 | Drive | 11, | 14 |
| BUS IN BIT 4[2,4] | 28, | 58 | Drive | 53, | 56 |
| BUS IN BIT 5[2,4] | 20, | 50 | Drive | 42, | 45 |
| BUS IN BIT 6[2,4] | 18, | 48 | Drive | 10, | 13 |
| BUS IN BIT 7[2,4] | 25, | 55 | Drive | 74, | 77 |
| PICK[6] | | 29 | CU/Drive[8] | 73, | |
| SEQUENCE DISABLE[6] | | 59 | Drive | 76, | |
| BUSY[1,2,6] | 21, | 51 | Drive | 47, | 50 |
| TERMINATOR GROUND | -- | -- | -- | 80, | |
| CABLE SHIELD | -- | -- | -- | 82, | |

[1] DUAL PORT UNITS ONLY
[2] GATED BY DEVICE SELECTED
[3] BUS OUT INFORMATION
[4] BUS IN INFORMATION
[5] TAG 5 GATED BY UNIT SELECTED
[6] OPTIONAL LINES DEFINED IN SECTION 6
[7] SPARE PINS ON THE 75 PIN CONNECTOR ARE:47,50,54,57-60,62-65,67, 70-73,76 & 79. OPTIONALLY 47,50,54,57,73 & 76 MAY BE USED.
[8] See 6.3

Table 2
READ/WRITE Cable Signal Locations

| Signal Name | Pin Polarity (Active) - | + | Shield | Source |
|---|---|---|---|---|
| WRITE DATA | A | B | D | CU [3] |
| WRITE CLOCK | H | J | E | CU |
| SERVO CLOCK | M | N | K | DRIVE |
| READ DATA | U | V | T | DRIVE |
| READ CLOCK | W | X | Y | DRIVE |
| SELECTED | DD | BB | - | DRIVE |
| SEEK END | AA | CC | - | DRIVE |
| INDEX MARK [1] | EE | HH | - | DRIVE |
| SECTOR MARK [1] | FF | JJ | - | DRIVE |
| dc Ground | NN | LL [2] | - | CU,DRIVE |
| -5 Volts [1] | MM | - | - | DRIVE |
| Cable Shield | - | - | Z | CU,DRIVE |

Round-Cable (34-Pin Connector) Pin Assignments

| | | | | |
|---|---|---|---|---|
| WRITE DATA | 8 | 20 | 7 | CU |
| WRITE CLOCK | 6 | 19 | 18 | CU |
| SERVO CLOCK | 2 | 14 | 1 | DRIVE |
| READ DATA | 3 | 16 | 15 | DRIVE |
| READ CLOCK | 5 | 17 | 4 | DRIVE |
| SELECTED | 22 | 9 | 21 | DRIVE |
| SEEK END | 10 | 23 | - | DRIVE |
| INDEX MARK [1] | 12 | 24 | 11 | DRIVE |
| SECTOR MARK [1] | 13 | 26 | 25 | DRIVE |
| DRAIN WIRE/SHIELD | | | 1 [2] | CU,DRIVE |

Flat-Cable (26-Pin Connector) Pin Assignments

NOTES:

These signals are not gated with UNIT SELECT.

[1] These are optional signals defined in Section 6.
[2] These ground or shield connections were not indicated in the original issue of this standard and consequently may be omitted in some implementations.
[3] CU = Control Units.

**3.3.2 Flat-Ribbon Cable**

**3.3.2.1 CONTROL Cable.** The flat-ribbon cable, when used, shall consist of 30 twisted-pairs. The conductor of each twisted-pair cable shall be 28 AWG. The characteristic impedance of each pair shall be 100 ohms ± 10 ohms.

**3.3.2.2. READ/WRITE Cable.** The flat-ribbon cable shall consist of 26 conductor ribbon cables with a ground plane and drain wire. The conductor spacing shall be 0.050 inch center-to-center to provide for mass termination. The conductors shall be 28 AWG. The characteristic impedance of any single wire driven against the ground plane shall be 65 ohms.

**3.4 Electrical Characteristics**

**3.4.1 Transmitter.** Transmitters are differential, three-state devices; each transmitter circuit consists of a negatively connected NPN current switch. Each side of the differential transmitters shall be capable of sinking 12 milliamperes ±3 milliamperes in the "ON" state, and shall leak no more than 100 microamperes in the high impedance state. When a drive is selected, its transmitters shall switch differentially according to the polarities shown in Figures 3 and 4. When a drive is not selected, its CONTROL cable transmitters shall have both outputs in the high impedance state.

**3.4.2 Receiver.** Each receiver circuit is a differential receiver. Its sensitivity shall be ±25 millivolts and it shall reject common-mode noise of at least ±3 volts on its inputs. Differential voltages of at least ±6 volts and common-mode voltages of at least ±5 volts shall be withstood without damage. Series protection resistors of 470 ohms may be used.

**3.4.3 Termination**

**3.4.3.1 CONTROL Cable.** All signal pairs except INTERFACE ENABLE, PICK, and SEQUENCE DISABLE shall be electrically terminated within any control unit or disk drive that does not pass on the CONTROL cable in daisy-chain fashion. Thus, both ends of these signals shall be terminated. At each end, both sides of each signal pair shall be connected to ground through a 56-ohm resistor.

Instead of cable termination, the INTERFACE ENABLE signal shall be biased to the negated condition in each drive. This may be accomplished near the receiver with a resistor to +5 volts from the negative side of the pair and a resistor to -5 volts from the positive side. The resistor values shall be selected for the receiver type and may be an appropriate value greater than 10K ohms. The termination of PICK and SEQUENCE DISABLE, if implemented, shall be as described in 6.3.

**3.4.3.2 READ/WRITE Cable.** The READ DATA, WRITE DATA, SERVO CLOCK, READ CLOCK, and WRITE CLOCK signals shall be terminated with appropriate resistors from each side of the differential line to ground at the receiving end only. The resistor values for up to 10 Mbits/s with the flat cable are typically 68 ohms. For transfer rates up to 24 Mbits/s, the resistor values for the flat cable are typically 56 ohms from each side of the twisted pair to a common 22-ohm resistor to ground, per pair. The round cable resistor values are typically 82 ohms from each side of the twisted pair to ground. READ DATA, READ CLOCK, and SERVO CLOCK shall be terminated in the controller and WRITE DATA and WRITE CLOCK shall be terminated in the drive.

All other signals remaining in the READ/WRITE cable shall be terminated with 68-ohm (flat-cable) or 56-ohm (round-cable) resistors from each side of the differential line to ground at the receiver end.

**3.4.4 Cable Lengths.** The transmitting and receiving circuitry shall function properly with READ/WRITE cable lengths of up to 15 meters and with cumulative CONTROL cable chain lengths of up to 30 meters.

## 4. Signal Definitions

This section defines essential signals and the intended operation and states of the signals. Relative signal timings and tolerances shall be as defined in Section 5.

**4.1 CONTROL Cable Interface.** Control and status information shall be exchanged between a drive and a control unit via the CONTROL cable. Pin assignments and signal polarities shall be as defined in Table 1.

**4.1.1 Output Lines (Control Unit to Drive).** The output line functions are:

4 DEVICE SELECT
1 INTERFACE ENABLE
6 TAG SIGNALS (7 LOGICAL FUNCTION TAGS)
10 BUS-OUT LINES (optionally 11)
2 PICK and HOLD LINES

**4.1.1.1 Device Selection Lines.** These lines shall be used for the logical connection of a disk drive to the control unit.

**4.1.1.1.1 DEVICE SELECT 3, 2, 1, 0.** These four lines shall be decoded to select one of up to sixteen drives on the CONTROL cable. DEVICE SELECT 3, 2, 1, and 0 correspond to binary weights 8, 4, 2, and 1, respectively, when specifying the select number. The select number is determined by the drive. Each drive on a given CONTROL cable chain shall have a unique select number.

**4.1.1.1.2 TAG 0 (DEVICE SELECT ENABLE).** Selection of the drive shall occur at the leading edge of DEVICE SELECT ENABLE, provided that the select number on the DEVICE SELECT lines is equal to that designated within the drive. Selection of the drive shall be acknowl-

edged by the assertion of SELECTED on the READ/WRITE cable. The drive shall remain selected until DEVICE SELECT ENABLE is negated. The drive shall acknowledge deselection by negating SELECTED. If either the drive's select number or the DEVICE SELECT lines are changed while the drive is selected, the drive shall remain selected and responsive to the control unit until SELECT ENABLE is dropped by the control unit.

**4.1.1.2 INTERFACE ENABLE (or OPEN CABLE DETECT).** This signal, when asserted, enables the drive's receivers and drivers and allows selection and operation of the drive from the control unit. Negation of this signal shall disable the drive's receivers and drivers. During the entire control unit's internal power sequencing (up or down), this signal shall be negated to prevent spurious information transfer. The INTERFACE ENABLE signal is terminated in such a way that removal of the cable shall disable line receivers.

**4.1.1.3 Function Tags.** These tags, asserted singly, perform the following operations on a selected disk drive (see Tables 1 and 2).

**4.1.1.3.1 TAG 1 (SET CYLINDER).** This tag transfers the cylinder address bits to the drive via BUS out lines. BUS out 9,8,...,0 correspond to binary weights 512,256,....,1, respectively, when determining the cylinder address. Optional extended cylinder addressing capability, if implemented, shall be as described in 4.1.1.3.2 and 6.9.

If the cylinder address is invalid, SEEK ERROR shall be asserted in response to the leading edge of SET CYLINDER. ON CYLINDER and SEEK END shall always be negated on the trailing edge of SET CYLINDER.

**4.1.1.3.2 TAG 2 (HEAD SET).** This tag transfers the head address bits to the drive via the BUS OUT lines. BUS OUT lines 6,5,...,0 correspond to binary weights 64, 32,....,1, respectively, when determining the head address. The head address specifies one of the tracks on a given cylinder on which READ or WRITE operations may be performed. Note that the number of heads is drive dependent.

Optionally, BUS OUT lines 9, 8 and 7 correspond to cylinder address bits with binary weights 4,096, 2,048, and 1,024, respectively. If this extended cylinder addressing function is used, TAG 2 shall precede TAG 1 and all BUS OUT bits shall be controlled (see 6.9).

**4.1.1.3.3 TAG 3 (CONTROL SELECT).** This tag, when active, allows the BUS OUT lines to control operations in a selected drive. The significance of the BUS OUT lines with the CONTROL SELECT asserted is as follows:

(1) *BUS OUT 0 — WRITE GATE.* With ADDRESS MARK ENABLE negated, WRITE GATE command enables the write circuitry to transfer the serialized information on the WRITE DATA line to the recording medium. If ADDRESS MARK ENABLE is asserted during WRITE GATE, the drive shall record an address mark. While the WRITE GATE is asserted, the drive faults related to WRITE operations may be detected and signaled via the FAULT line on the CONTROL cable.

Other than ADDRESS MARK ENABLE, all other combinations of control functions asserted with WRITE GATE result in undefined action.

(2) *BUS OUT 1 — READ GATE.* With ADDRESS MARK ENABLE negated, READ GATE command enables the read circuitry to transfer the serialized information on the READ DATA line from the recording medium. If ADDRESS MARK ENABLE is asserted during READ GATE, the drive shall search for a previously recorded address mark.

NOTE: The READ GATE shall be asserted while the read head is positioned over a zero data field area of the track for proper synchronization. See the manufacturer's specification for exact timing.

Any combination of the following conditions may also be asserted:

(a) ADDRESS MARK ENABLE

(b) OFFSET FORWARD or OFFSET REVERSE, but not both

(c) DATA STROBE EARLY or DATA STROBE LATE, but not both

All other combinations of control functions asserted with READ GATE result in undefined action.

(3) *BUS OUT 2 — OFFSET FORWARD.* Assertion of the OFFSET FORWARD command displaces the head positioner a fixed amount, from its normal position towards the spindle center. The leading edge of this command causes the negation of ON CYLINDER during the offset positioning in conjunction with SEEK END. The trailing edge of OFFSET FORWARD initiates the removal of the offset condition.

Any combination of the following signals may also be asserted:

(a) READ GATE

(b) ADDRESS MARK ENABLE

(c) DATA STROBE EARLY or DATA STROBE LATE, but not both

(d) FAULT RESET

All other combinations of control functions asserted with OFFSET FORWARD result in undefined action.

NOTE: This command, if asserted during WRITE GATE, causes the assertion of FAULT.

(4) *BUS OUT 3 — OFFSET REVERSE.* Identical to the OFFSET FORWARD command, but displaces the head positioner in the opposite direction.

(5) *BUS OUT 4 — FAULT RESET.* This signal clears the FAULT status, provided no condition remains that activates FAULT. REZERO, RELEASE,

or both may also be asserted. All other combinations of control functions asserted with FAULT RESET result in undefined action.

(6) *BUS OUT 5 — ADDRESS MARK ENABLE.* This command, used only for variable sector formats, allows the control unit to record and identify record boundaries. When asserted in conjunction with WRITE GATE, the drive records an address mark. This command, when used in conjunction with READ GATE, causes the drive to assert ADDRESS MARK when a previously recorded address mark is detected.

The following conditions may also be asserted:

(a) WRITE GATE

(b) READ GATE; READ GATE may be asserted with OFFSET FORWARD or OFFSET REVERSE and DATA STROBE EARLY or DATA STROBE LATE. Both OFFSET signals and both DATA STROBE signals shall not be used simultaneously. READ GATE may be asserted by itself. All other combinations of control functions asserted with ADDRESS MARK ENABLE result in undefined action.

(7) *BUS OUT 6 — REZERO.* This command causes the head positioner to reposition to cylinder 0 and resets the head address register to zero. The leading edge of REZERO negates ON CYLINDER, SEEK END, and SEEK ERROR. FAULT RESET, UNIT RELEASE (6.2.2.3), or both may also be asserted. All other combinations of control functions asserted with REZERO result in undefined action.

(8) *BUS OUT 7 — DATA STROBE EARLY.* During assertion of the DATA STROBE EARLY command, the drive's internal data recovery logic shall strobe the READ data at a time earlier than normal. The normal strobe timing and the timing change covered by this signal are drive dependent.

Any combination of the following commands may also be asserted:

(a) READ GATE

(b) ADDRESS MARK ENABLE

(c) OFFSET FORWARD or OFFSET REVERSE, but not both

All other combinations of control functions asserted with DATA STROBE EARLY result in undefined action.

(9) *BUS OUT 8 — DATA STROBE LATE.* During assertion of the DATA STROBE LATE command, the drive's internal data recovery logic shall strobe the READ data at a time later than normal. In all other respects, this command is identical to DATA STROBE EARLY.

(10) *BUS OUT 9 — Not Used (in mandatory subset).* This signal is not used when CONTROL SELECT is asserted. (See 6.2.2.3 for optional usage.)

**4.1.1.3.4 TAG 4 (CURRENT PHYSICAL SECTOR).** The use of this signal is optional. It is defined in 6.4.

**4.1.2 Input Lines (Drive to Control Unit).** There are eight primary status lines between the drive and control unit that serve as input lines. They are as follows:

(1) INDEX MARK
(2) SECTOR MARK
(3) FAULT
(4) SEEK ERROR
(5) ON CYLINDER
(6) UNIT READY
(7) WRITE PROTECTED
(8) ADDRESS MARK

NOTE: If the drive has a maintenance mode, and the mode is activated, all output lines will be ignored and all input lines will be held inactive.

The drive shall be selected to enable the status lines described in 4.1.2.1 — 4.1.2.8 onto the BUS IN line.

**4.1.2.1 INDEX MARK.** This status line, when asserted, indicates that the reference point or index area is passing under the heads. This pulse occurs once per revolution of the recording surface.

**4.1.2.2 SECTOR MARK.** This status line establishes rotational reference points on the recording surface. Each track may be divided into sectors with the initial sector starting coincident with the INDEX MARK. SECTOR MARK is omitted at the initial sector. SECTOR MARK indicates the beginning of each subsequent sector. The number of sectors into which each track is divided shall be determined within the drive.

**4.1.2.3 FAULT.** When asserted, this line indicates that a fault condition (for example, READ/WRITE unsafe) has occurred within the drive. The FAULT condition disables the READ and WRITE operations within the drive. This condition also causes negation of UNIT READY (ON CYLINDER and SEEK END remain unaffected). The FAULT signal shall be reset either by a FAULT RESET command, or optionally by operator intervention at the drive, provided no condition remains that activates FAULT.

**4.1.2.4 SEEK ERROR.** When asserted, this status line indicates that the drive failed to complete an initial head load, SET CYLINDER, or REZERO command. SEEK ERROR also results when an invalid cylinder address is received by the drive. The SEEK ERROR status may be negated either by a REZERO command from the control unit or optionally by operator intervention at the drive.

**4.1.2.5 ON CYLINDER.** This status line indicates that the heads are stabilized at a usable cylinder. However, ON CYLINDER is not negated when OFFSET FORWARD or OFFSET REVERSE is removed. ON CYLINDER is negated on the trailing edge of the SET CYLINDER command or on the leading edge of REZERO, OFFSET FORWARD, or OFFSET REVERSE.

**4.1.2.6 UNIT READY.** This status line indicates that the drive is ready to accept commands and that no FAULT condition exists within the drive.

**4.1.2.7 WRITE PROTECTED.** This line indicates that recording of information on the recording surface is inhibited at the drive. Asserting WRITE GATE after WRITE PROTECTED has been asserted causes FAULT to be asserted.

**4.1.2.8 ADDRESS MARK.** This line indicates drive detection of a previously recorded address mark, when READ GATE and ADDRESS MARK ENABLE are both asserted.

**4.2 READ/WRITE Cable Interface.** The READ/WRITE cable signals shall be as listed in Table 2. Signals on this cable shall be continuously available when the drive is powered on.

**4.2.1 WRITE CLOCK.** The WRITE CLOCK is used by the drive to strobe the WRITE DATA line while recording. WRITE CLOCK is generated in the control unit by regenerating the drive's SERVO CLOCK signal. The WRITE CLOCK signal shall precede and be transmitted continuously during the assertion of WRITE GATE.

**4.2.2 WRITE DATA.** The WRITE DATA line carries the serial data to the drive during WRITE GATE assertion. The serial write data is strobed with the WRITE CLOCK.

**4.2.3 SERVO CLOCK.** The SERVO CLOCK is developed within the drive and provides a reference clock for the control unit that synchronizes WRITE DATA to the rotational position of the recording surface during a WRITE operation. The SERVO CLOCK is valid only when UNIT READY is asserted.

**4.2.4 READ CLOCK.** The READ CLOCK signal is developed within the drive. The leading edge of the READ CLOCK signal is used by the control unit to strobe READ DATA.

**4.2.5 READ DATA.** The READ DATA line carries serial data synchronized with READ CLOCK during the assertion of READ GATE.

**4.2.6 SELECTED.** This signal is transmitted from the drive to the control unit to indicate successful selection of a device. SELECTED shall remain asserted until DEVICE SELECT ENABLE is negated.

**4.2.7 SEEK END.** This signal is asserted in response to the assertion of either ON CYLINDER or SEEK ERROR. SEEK END is negated as a result of the assertion of TAG 1 (SET CYLINDER) or the negation of UNIT READY.

## 5. Timing Characteristics

The timing characteristics described in the following subsections refer to the signals (Section 4) at the drive interface connector. The control unit timing should be designed to accommodate cable delays and signal skew within the cables.

**5.1 Device Selection Sequence.** The timing for the initial selection of a drive shall be as shown in Figure 9. The control unit should wait at least 1 microsecond following the assertion of DEVICE SELECT ENABLE before sampling the status and selected lines. Since the SELECTED signal is in a separate cable from the status lines, it should not be used to strobe the status lines. The timing for device deselection shall be as shown in Figure 10.

**5.2 SEEK Command Sequence.** The timing for a SEEK command with a valid moving head cylinder number shall be as shown in Figure 11a. If the BUS OUT lines contain an invalid moving head cylinder address, the timing shall be as shown in Figure 11b.

**5.3 REZERO Command Sequence.** The timing for a REZERO command shall be as shown in Figure 12.

**5.4 OFFSET Command Sequence.** The OFFSET command timing shall be as shown in Figure 13. When an OFFSET command is negated, a delay of at least 10 milliseconds shall be guaranteed by the control unit prior to assertion of SEEK, REZERO, READ, or WRITE commands.

**5.5 HEAD SET Command Sequence.** The timing for a HEAD SET command shall be as shown in Figure 14.

**5.6 FAULT CLEAR Command Sequence.** The timing for a FAULT CLEAR command shall be as shown in Figure 15. If the fault is permanent, the fault status shall not reset as a result of the FAULT CLEAR command.

**5.7 INDEX MARK and SECTOR MARK Timing.** The INDEX MARK and SECTOR MARK are pulses with a minimum duration of 1 byte. The maximum duration of either pulse shall be 5.0 microseconds. The drive inhibits the SECTOR pulse during the INDEX pulse so that a SECTOR pulse is not transmitted at INDEX. The INDEX and SECTOR status lines are enabled by DEVICE SELECT, thus the control unit shall ignore the INDEX MARK and SECTOR MARK lines for at least 5.0 microseconds from the time that the status lines are valid to ensure a valid INDEX or SECTOR pulse.

NOTE: In ANSI X3.91M-1982, the minimum INDEX mark pulse was 2 microseconds and the minimum SECTOR mark was 1 microsecond. Consult the specifications of the manufacturer of the controller to determine if the original values are required.

**5.8 READ Command Sequence.** The timing for the READ command sequence shall be as shown in Figure 16. Data shall be recovered correctly if the READ GATE command is asserted in a field of zeros that lasts after READ GATE for the PLO synchronization interval. To ensure the recovery of previously recorded data, the timing requirements in 5.8.1 — 5.8.4 shall be satisfied by the control unit and the track format.

**5.8.1 SEEK END (ON CYLINDER) to READ GATE.** The assertion of READ GATE shall occur a minimum of 500 nanoseconds following the assertion of SEEK END or ON CYLINDER.

**5.8.2 OFFSET to READ GATE.** The assertion of the READ GATE command shall occur a minimum of 10 milliseconds following the negation of an OFFSET FORWARD or OFFSET REVERSE command.

**5.8.3 TAG 2 (HEAD SET) to READ GATE.** The assertion of READ GATE command shall occur a minimum of 15 microseconds following the assertion of TAG 2. If TAG 2 included a cylinder change, 5.8.1 shall also apply.

**5.8.4 WRITE GATE to READ GATE.** The assertion of READ GATE shall occur a minimum of 10 microseconds following the negation of the WRITE GATE command.

**5.9 WRITE Command Sequence.** The timing for the WRITE command sequence shall be as shown in Figure 17. A WRITE command sequence shall be initiated immediately following a WRITE ADDRESS MARK or READ ADDRESS MARK command sequence.

To ensure storage of data for subsequent recovery, a WRITE sequence shall begin with a synchronization field of zeros. The timing requirements described in 5.9.1 — 5.9.4 shall be satisfied by the control unit and track format.

**5.9.1 SEEK END or ON CYLINDER to WRITE GATE.** The assertion of the WRITE GATE command shall occur a minimum of 500 nanoseconds following the assertion of an ON CYLINDER or SEEK END status.

**5.9.2 OFFSET to WRITE GATE.** The assertion of the WRITE GATE command shall occur a minimum of 10 milliseconds following the negation of either an OFFSET FORWARD or an OFFSET REVERSE command.

**5.9.3 TAG 2 (HEAD SET) to WRITE GATE.** The assertion of the WRITE GATE command shall occur a minimum of 5 microseconds following the negation of TAG 2. If TAG 2 included a cylinder change, 5.9.1 shall also apply.

**5.9.4 READ GATE to WRITE GATE.** The assertion of WRITE GATE shall occur a minimum of 500 nanoseconds following the negation of the READ GATE command.

**5.10 READ ADDRESS MARK Command Sequence.** The timing for the READ ADDRESS MARK command sequence and the pulse duration for the ADDRESS MARK FOUND command shall be as described in Figure 18. The pulse duration is not affected by the negation of the READ ADDRESS MARK command.

To ensure recovery of an ADDRESS MARK, the timing requirements described in 5.10.1 — 5.10.5 shall be satisfied by the control unit and the track format.

**5.10.1 SEEK END to READ ADDRESS MARK.** The assertion of the READ ADDRESS MARK command shall occur a minimum of 500 nanoseconds following the assertion of ON CYLINDER or SEEK END status.

**5.10.2 OFFSET to READ ADDRESS MARK.** The assertion of the READ ADDRESS MARK command shall occur a minimum of 10 milliseconds following the negation of either an OFFSET FORWARD or an OFFSET REVERSE command.

**5.10.3 TAG 2 (HEAD SET) to READ ADDRESS MARK.** The assertion of the READ ADDRESS MARK command shall occur a minimum of 15 microseconds following the assertion of TAG 2. If the TAG 2 included a cylinder change, 5.8.1 shall also apply.

**5.10.4 WRITE GATE to READ ADDRESS MARK.** The assertion of the READ ADDRESS MARK command shall occur a minimum of 25 microseconds following the negation of the WRITE GATE command.

**5.10.5 READ GATE to READ ADDRESS MARK.** The assertion of the READ ADDRESS MARK command shall occur a minimum of 500 nanoseconds following the assertion of the READ GATE command.

**5.11 WRITE ADDRESS MARK Command Sequence.** The timing for the WRITE ADDRESS MARK command shall be as described in Figure 19. WRITE GATE precedes ADDRESS MARK ENABLE and shall meet all requirements of 5.9.

To ensure generation of an ADDRESS MARK for subsequent recovery, the timing requirements in 5.11.1 — 5.11.3 shall be satisfied by the control unit and the track format.

**5.11.1 SEEK END or ON CYLINDER to WRITE ADDRESS MARK.** The assertion of the WRITE ADDRESS MARK command shall occur a minimum of 500 nanoseconds following the assertion of the SEEK END or ON CYLINDER status.

**5.11.2 OFFSET to WRITE ADDRESS MARK.** The assertion of the WRITE ADDRESS MARK command shall occur a minimum of 10 milliseconds following the negation of either an OFFSET FORWARD or an OFFSET REVERSE command.

**5.11.3 TAG 2 (HEAD SET) to WRITE ADDRESS MARK.** The WRITE ADDRESS MARK command shall occur a minimum of 5 microseconds following the negation of TAG 2. If TAG 2 included a cylinder change, 5.9.1 shall also apply.

**5.12 SERVO CLOCK.** This clock has a duty cycle of 50 percent ± 3 percent.

**5.13 READ CLOCK and READ DATA.** The READ CLOCK and READ DATA signals shall be synchronized as shown in Figure 20.

NOTE: In ANSI X3.91M-1982, the read clock was erroneously shown 180 degrees out of phase.

**5.14 WRITE CLOCK and WRITE DATA.** The WRITE CLOCK and WRITE DATA signals shall be synchronized as shown in Figure 21.

NOTE: In ANSI X3.91M-1982, the write clock was erroneously shown 180 degrees out of phase.

## 6. Interface Extensions

The storage module interface defined by Sections 3, 4, and 5 forms the basic equipment covered by this standard. Compliance with this standard requires that all of the nonoptional features described in Sections 3, 4, and 5 be implemented in the manner specified. This section describes extensions to the basic equipment that may be optionally added in any control-unit/drive design. Whenever any of these extensions are included, conformance to this standard requires that they be implemented in the manner specified.

All signals returned by the drive to a control unit shall function as described in Section 4, unless indicated otherwise in this section.

**6.1 Extended Functions** (See Figure 22). The signals TAG 1, TAG 2, and TAG 3 in the mandatory subset take on the specific functions or signal names SET CYLINDER, HEAD SET, and CONTROL SELECT, respectively. The interface provides extended capabilities beyond that described in Sections 4 and 5. The optional extended functions may include:

(1) Current physical sector address
(2) Expanded status
  (a) Fault status
  (b) Operating status
  (c) Diagnostic status
  (d) Device identification

These extended capabilities may be invoked by the use of TAG 4, TAG 5, or TAG 6 (which is the logical "and" of TAG 4 and TAG 5) (see Figure 23). If the functions of TAG 4 and TAG 6 are not implemented and if the extended cylinder capability of TAG 2 is not implemented, the TAG 4 line may optionally be used as a cylinder address bit of weight 1024.

**6.2 Dual Port.** The dual port extension allows interleaved access to one drive by two control units. The dual port operates as a switch that routes control, data, and status signals between the drive and the control unit to which the drive may be reserved. Once selection is accomplished, the dual port is not apparent to normal operation of the interface.

The dual port interface communicates with the two control units through two identical interfaces designated Port A and Port B. The physical interface between each port and its attached control unit consists of a radial READ/WRITE cable and a CONTROL cable with provisions for daisy chaining or terminating the CONTROL cable (see Figure 2b).

**6.2.1 Signal Descriptions** (See Figure 24)

**6.2.1.1 BUSY.** This signal is enabled by the drive onto the CONTROL cable when that drive is selected. It shall be asserted if the drive is reserved to the other control unit, and negated otherwise.

**6.2.1.2 SEEK END.** While a drive is reserved to one control unit, SEEK END shall be asserted to the nonreserving control unit. If the drive is reserved by one control unit and selection is attempted by the other control unit during the period of reservation, SEEK END shall be negated to the nonreserving control unit for a period of 30 microseconds after the reserving control unit releases the drive.

**6.2.2 Device Reservation and Release**

**6.2.2.1 Reservation.** The drive shall become reserved to a control unit when it is selected by that control unit and not already reserved by the other control unit. It shall remain reserved until released, or until a PRIORITY SELECT command sequence occurs on the other port. On power-up, the drive shall not be reserved to either control unit.

If the drive was reserved by the first control unit and selection was attempted by the second control unit during the period of reservation, the drive shall become reserved to the second control unit after the first control unit releases the drive.

**6.2.2.2 PRIORITY SELECT Command Sequence.** Drive reservation shall be forced from one control unit to another if the control unit demanding reservation performs a PRIORITY SELECT command sequence consisting of a unit selection sequence with BUS OUT 9 asserted. Drive reservation shall be switched at the leading edge of TAG 0 (DEVICE SELECT ENABLE). Continued assertion of BUS OUT 9 and TAG 0 by that control unit shall not prevent the other control unit from reserving the drive by issuing a PRIORITY SELECT command sequence.

**6.2.2.3 UNIT RELEASE.** The drive shall be released by the control unit if the control unit asserts TAG 3 and BUS OUT 9 while the drive is selected. The drive shall remain reserved until TAG 0 is negated. FAULT RESET, REZERO, or both can also be asserted. All other combinations of control functions asserted with UNIT RELEASE result in undefined action.

**6.2.2.4 Release Timer.** The drive may be released by a timer 500 milliseconds after it was last reserved, or after its reservation is changed from one port to the other. A means should be provided to inhibit the release timer. The states shall be as follows:

(1) *Inhibit.* The drive stays reserved to a control unit until that control unit issues a UNIT RELEASE command sequence, the other control unit issues a PRIORITY SELECT command sequence,. or the drive is powered down.

(2) *Enable.* The reserve timer releases the drive 500 milliseconds after the last reservation.

**6.2.2.5 Simultaneity.** In the event of simultaneous occurrence, the order of precedence shall be PRIORITY SELECT B over PRIORITY SELECT A over UNIT RELEASE B over UNIT RELEASE A over the timer.

**6.3 Spinup Sequencing.** Drive spinup sequencing shall be controlled by the lines PICK and SEQUENCE DISABLE (see Figure 25). These are single-ended lines as defined in a string; PICK IN is defined as PICK from the control unit direction. Likewise, PICK OUT is defined as PICK away from the control unit. PICK shall be passed on in such a manner that PICK OUT of one drive connects to PICK IN of the next drive in the string. PICK IN to the first drive in the string shall be controlled by the control unit. SEQUENCE DISABLE is controlled by any drive in the process of spinning up.

A drive shall begin its spinup sequence only if its power is on, its start switch is enabled, PICK IN is asserted (grounded) on either port, and SEQUENCE DISABLE is negated (high) on the same port. The control unit and each drive shall be capable of sinking 60 milliamperes when PICK is asserted. The drive shall not pull up PICK more than +20 volts. SEQUENCE DISABLE is biased at the control unit by a 2200-ohm resistor to +5 volts. While spinning up, a drive asserts SEQUENCE DISABLE on both ports, and negates PICK OUT on both ports. When it has spun up, it releases SEQUENCE DISABLE on both ports and asserts PICK OUT on any port that has PICK IN asserted. The maximum level of SEQUENCE DISABLE is 5.5 volts.

Each unit shall propagate PICK IN to PICK OUT if its start switch is disabled, if it is not powered up, or if its spinup sequence is complete. A drive shall receive a PICK-IN-asserted signal for a minimum of 10 milliseconds before beginning a spinup sequence. A drive shall spin up and propagate PICK IN a maximum of 1 minute. The control unit shall maintain PICK for the sum of the spinup propagation times of the drives attached to it.

Negation of INTERFACE ENABLE for a minimum of 50 milliseconds shall constitute a spindown command.

**6.4 TAG 4.** The TAG 4 signal asserted with TAG 5 negated shall allow the current physical sector address to be transmitted to the control unit on BUS IN Bits 0 through 7 inclusive. The physical sector address is a dynamic count. The current physical sector count shall be valid until at least 200 nanoseconds before the leading edge of SECTOR or INDEX pulses and the next count shall be valid within 300 nanoseconds of the trailing edge of the SECTOR or INDEX pulse. TAG 5 and TAG 6 may be used to define optional extended status information as indicated in Table 3. Table 4 provides a summary of the various conditions defined by the TAGs.

**6.5 TAG 5.** TAG 5 shall allow Status. Optionally, BUS OUT bits may be used to permit multiple status bytes to be presented.

**6.6 TAG 6.** TAG 6 is the logical "and" of TAG 4 and TAG 5. A typical use of TAG 6 is to provide device identification. TAG 6 may optionally be used for other vendor-unique purposes.

**6.7 INDEX MARK and SECTOR MARK** (See Figure 26). These lines are available on the READ/WRITE cable and are not gated by UNIT SELECT. See 4.1.2.1 and 4.1.2.2 for definitions of these status lines.

**6.8 Fixed-Head Addressing.** The fixed heads in a drive shall be addressed as a unit number that may, at the user's option, be distinct from the unit number that addresses the moving-head address space in a drive. The fixed heads shall be organized within that unit as a contiguous set of cylinders with the same number of tracks per cylinder as the moving-head address space. ON CYLINDER and SEEK END refer only to the status of the movinghead positioner, even if the fixed heads are addressed.

**6.9 Service Voltages on Round Radial Cable.** Some service equipment requires -5 volts on pin MM of the round cable.

**6.10 Extended Cylinder Addressing.** This function provides for the HIGH-ORDER CYLINDER Bits 2 to the 10th through 2 to the 12th for drives with more than 1024 cylinders. BUS OUT Bits 7 through 9 with TAG 2 (the Head Set Tag) shall be utilized to provide the most significant bits of the cylinder address. If the HIGH-ORDER CYLINDER ADDRESS bits are to be utilized (or changed), TAG 2 (Head Set/High Cylinder Address) shall precede TAG 1 (Set (Low) Cylinder Address). Seek execution begins with the trailing edge of TAG 1. BUS OUT Bits 7 and 9 shall be controlled under all TAG 2 functions addressed to drives with the extended function capability.

NOTE: An alternate extended cylinder addressing method, with limited extended function capability, appears in 6.1.

Table 3
TAG BUS Decode

| BUS OUT BIT | TAG 0 DEVICE SELECT ENABLE | TAG 1 SET (LOW) CYLINDER | TAG 2 HEAD SET & OPTIONAL HIGH CYL | TAG 3 CONTROL SELECT |
|---|---|---|---|---|
| 0 | | C001 | H001 | WRITE GATE |
| 1 | | C002 | H002 | READ GATE |
| 2 | | C004 | H004 | OFFSET FORWARD |
| 3 | | C008 | H008 | OFFSET REVERSE |
| 4 | | C016 | H016 | FAULT RESET |
| 5 | | C032 | H032 | ADDRESS MARK ENABLE |
| 6 | | C064 | H064 | REZERO |
| 7 | | C128 | C1024* | DATA STROBE EARLY |
| 8 | | C256 | C2048* | DATA STROBE LATE |
| 9 | PRIORITY SELECT* | C512 | C4096* | UNIT RELEASE* |
| TAG 4 | | C1024** | ----- | ------ |

| BUS IN BIT | TAG 0 DEVICE STATUS | TAG 4* CURRENT SECTOR | TAG 5* EXTENDED STATUS | TAG 6* DEVICE TYPE OR OTHER VENDOR UNIQUE |
|---|---|---|---|---|
| 0 | UNIT READY | S001 | VU | VU |
| 1 | ON CYLINDER | S002 | VU | VU |
| 2 | SEEK ERROR | S004 | VU | VU |
| 3 | FAULT | S008 | VU | VU |
| 4 | WRITE PROTECTED | S016 | VU | VU |
| 5 | ADDRESS MARK | S032 | VU | VU |
| 6 | INDEX MARK | S064 | VU | VU |
| 7 | SECTOR MARK | S128 | VU | VU |

Notes:

* Optional.
** Optional method that precludes the use of TAG 4 and 6.
VU Vendor and/or device unique. Consult manufacturer's specification.

Table 4
TAG Truth Table

| TAG 0 | TAG 1 | TAG 2 | TAG 3 | TAG 4 | TAG 5 | COUNT |
|---|---|---|---|---|---|---|
| NO DEVICE SELECTED | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BETWEEN CONTROL TRANSFERS | | | | | | |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| DEVICE SELECTION "TAG 0" | | | | | | |
| 1 | 0 | 0 | 0 | 0 | N/A | 1 |
| SET (LOW) CYLINDER "TAG 1" | | | | | | |
| 1 | 1 | 0 | 0 | 0 | 0 | 3 |
| SET HEAD AND OPTIONALLY HIGH CYLINDER "TAG 2" | | | | | | |
| 1 | 0 | 1 | 0 | 0 | 0 | 5 |
| CONTROL SELECT "TAG 3" | | | | | | |
| 1 | 0 | 0 | 1 | 0 | 0 | 9 |
| Mandatory Functions | | | | | | |
| OPTIONAL CURRENT PHYSICAL SECTOR "TAG 4" | | | | | | |
| 1 | 0 | 0 | 0 | 1 | 0 | 17 |
| OPTIONAL STATUS "TAG 5" | | | | | | |
| 1 | 0 | 0 | 0 | 0 | 1 | 33 |
| OPTIONAL DEVICE TYPE OR OTHER VENDOR UNIQUE "TAG 6" | | | | | | |
| 1 | 0 | 0 | 0 | 1 | 1 | 49 |
| Optional Functions | | | | | | |

Table 4
TAG TRUTH TABLE (continued)

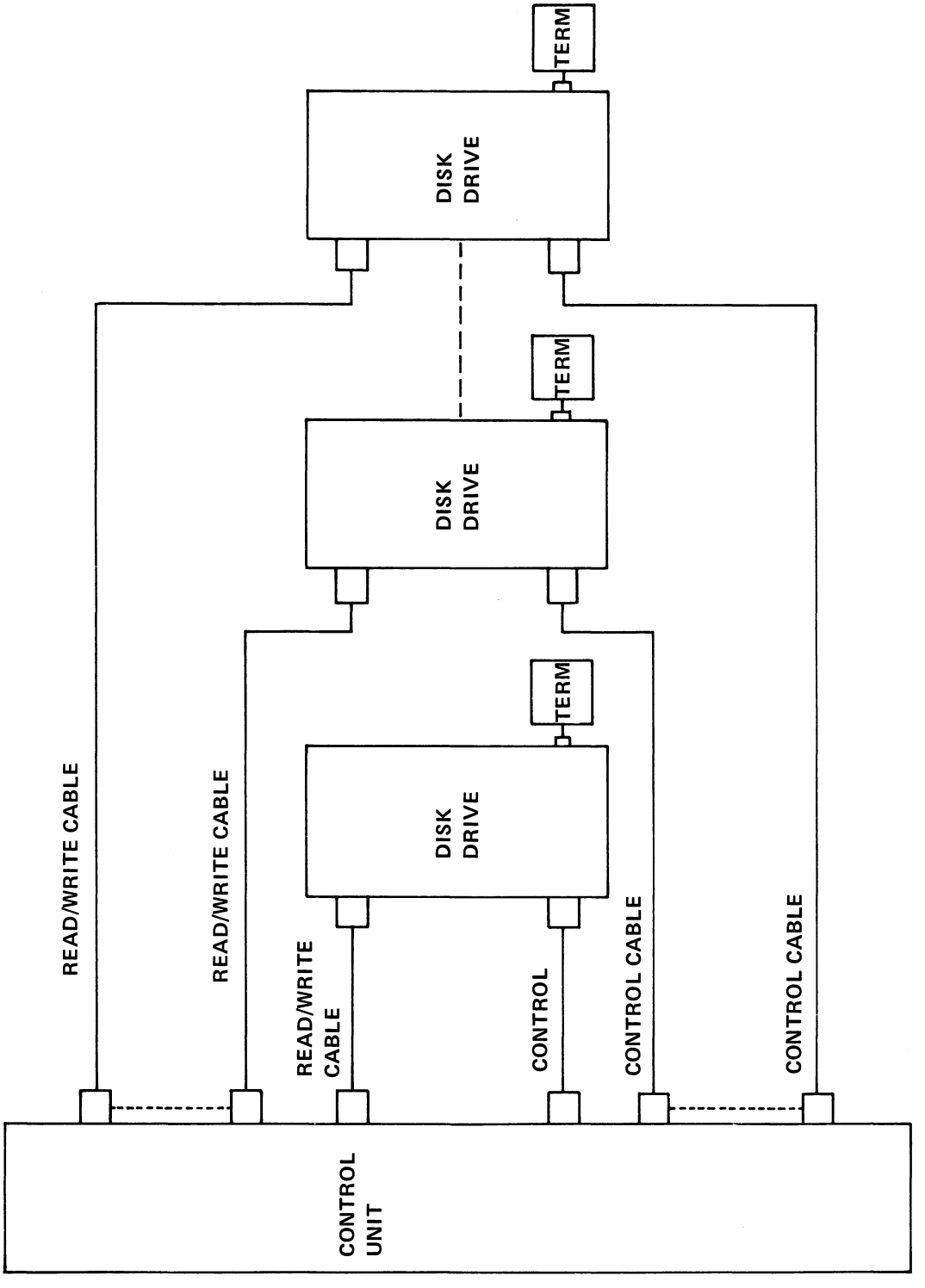
| TAG 0 | TAG 1 | TAG 2 | TAG 3 | TAG 4 | TAG 5 | COUNT |
|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 0 | 3 |
| 1 | 0 | 1 | 0 | 0 | 0 | 5 |
| 1 | 1 | 1 | 0 | 0 | 0 | 7 |
| 1 | 0 | 0 | 1 | 0 | 0 | 9 |
| 1 | 1 | 0 | 1 | 0 | 0 | 11 |
| 1 | 0 | 1 | 1 | 0 | 0 | 13 |
| 1 | 1 | 1 | 1 | 0 | 0 | 15 |
| 1 | 0 | 0 | 0 | 1 | 0 | 17 |
| 1 | 1 | 0 | 0 | 1 | 0 | 19 |
| 1 | 0 | 1 | 0 | 1 | 0 | 21 |
| 1 | 1 | 1 | 0 | 1 | 0 | 23 |
| 1 | 0 | 0 | 1 | 1 | 0 | 25 |
| 1 | 1 | 0 | 1 | 1 | 0 | 27 |
| 1 | 0 | 1 | 1 | 1 | 0 | 29 |
| 1 | 1 | 1 | 1 | 1 | 0 | 31 |
| 1 | 0 | 0 | 0 | 0 | 1 | 33 |
| 1 | 1 | 0 | 0 | 0 | 1 | 35 |
| 1 | 0 | 1 | 0 | 0 | 1 | 37 |
| 1 | 1 | 1 | 0 | 0 | 1 | 39 |
| 1 | 0 | 0 | 1 | 0 | 1 | 41 |
| 1 | 1 | 0 | 1 | 0 | 1 | 43 |
| 1 | 0 | 1 | 1 | 0 | 1 | 45 |
| 1 | 1 | 1 | 1 | 0 | 1 | 47 |
| 1 | 0 | 0 | 0 | 1 | 1 | 49 |
| 1 | 1 | 0 | 0 | 1 | 1 | 51 |
| 1 | 0 | 1 | 0 | 1 | 1 | 53 |
| 1 | 1 | 1 | 0 | 1 | 1 | 55 |
| 1 | 0 | 0 | 1 | 1 | 1 | 57 |
| 1 | 1 | 0 | 1 | 1 | 1 | 59 |
| 1 | 0 | 1 | 1 | 1 | 1 | 61 |
| 1 | 1 | 1 | 1 | 1 | 1 | 63 |

Reserved Functions

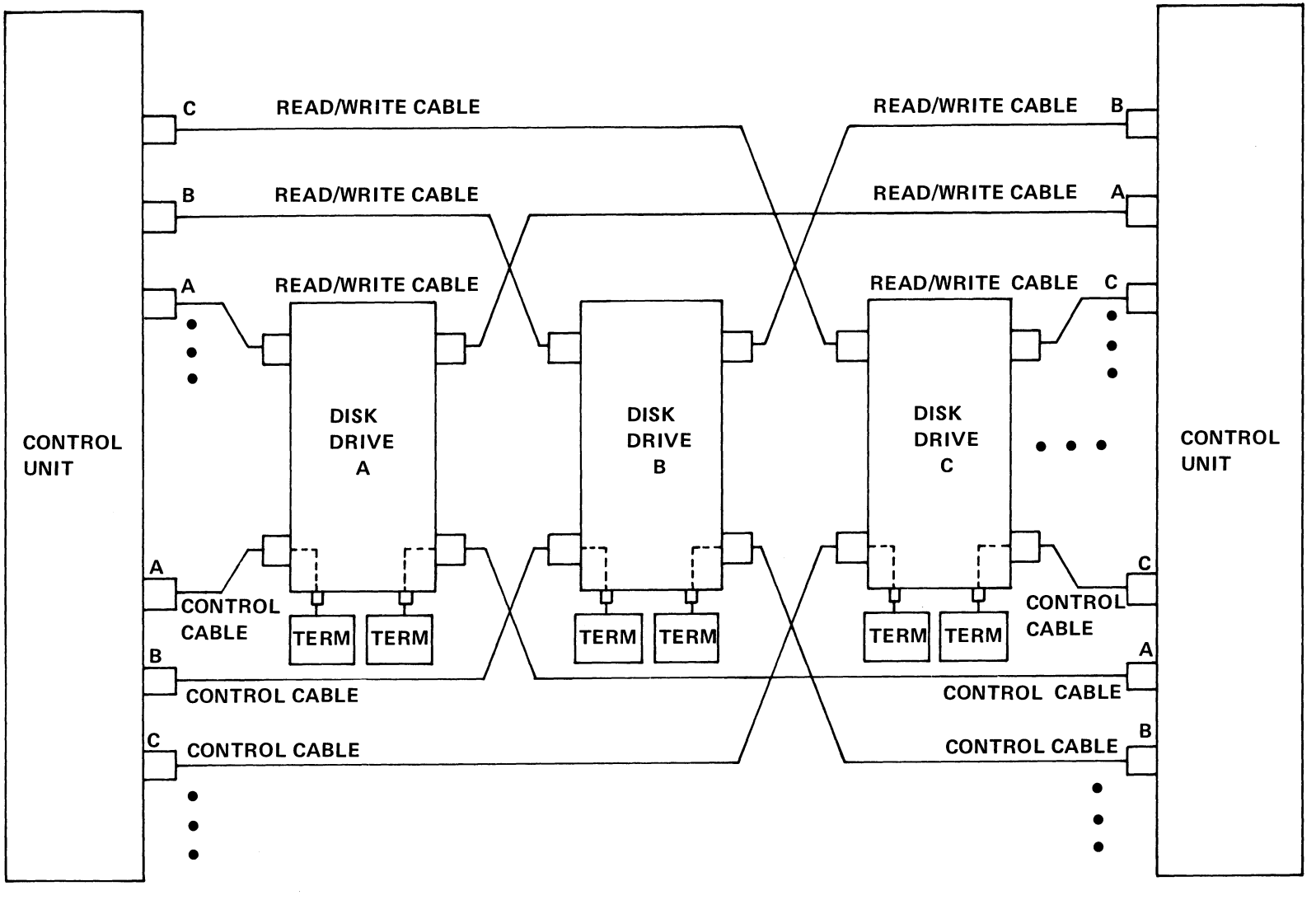
Notes:

(1) Reserved Functions have not been considered. They should not be used in "standard" implementations. If utilization is required, a request for consideration as a standard or vendor-unique function should be submitted to ASC X3 following approved procedures. There is no requirement that any design be capable of interpreting in any way the reserved functions.

(2) All even counts except 0 are not applicable since no device is selected if TAG 0 is false.



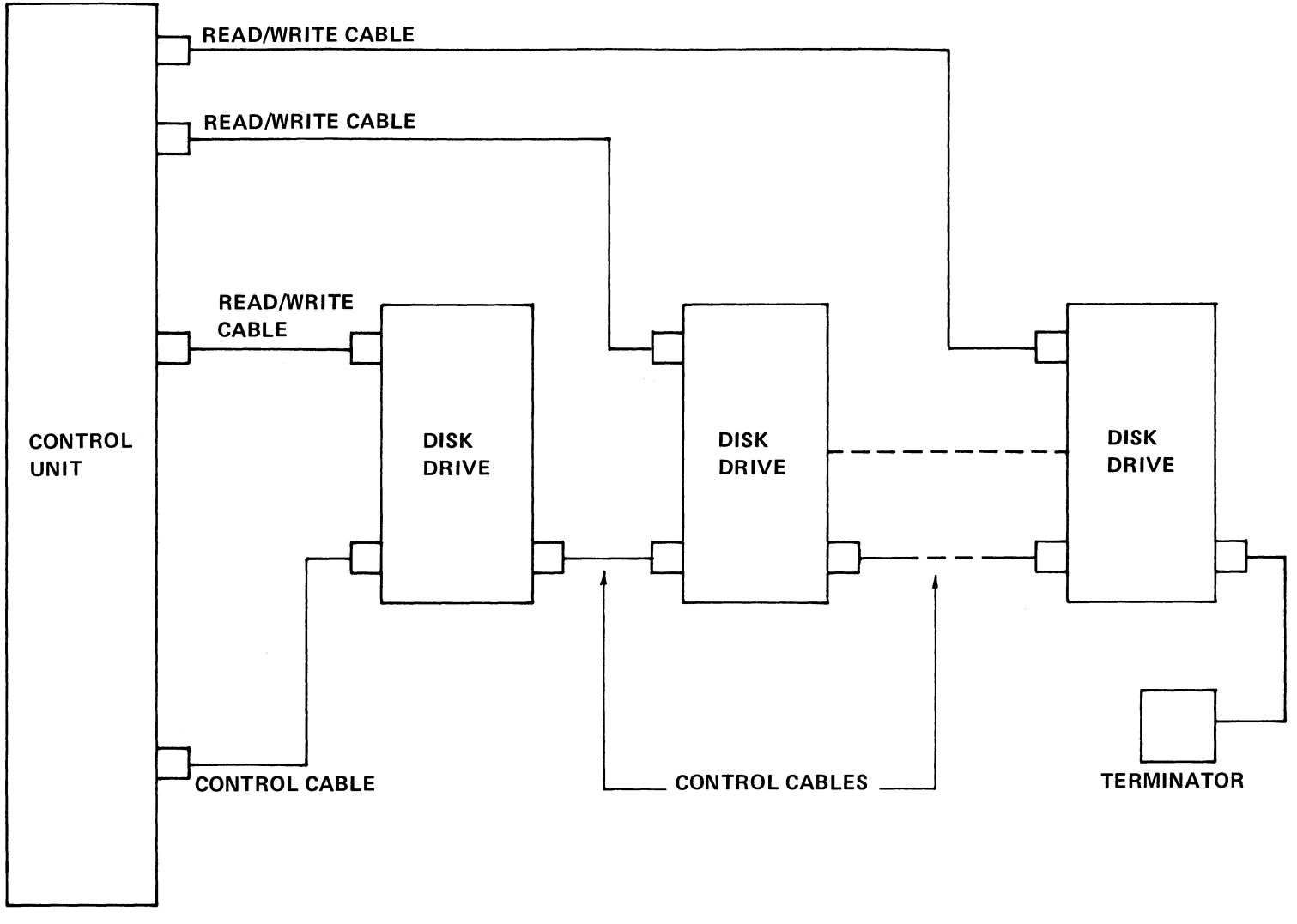

*(a) Single Port*



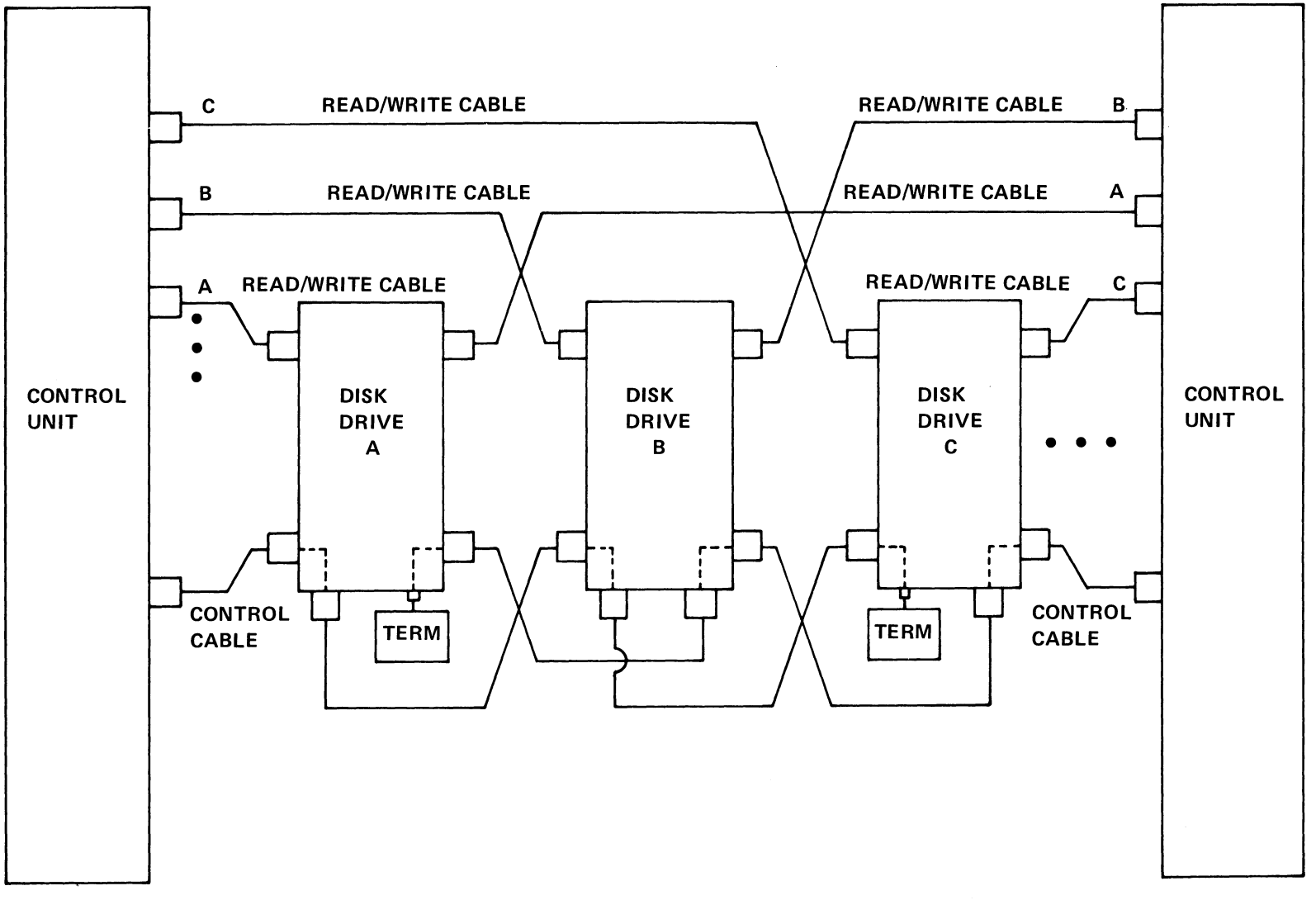

NOTE: Optional configuration defined in Section 6.

(*b*) *Dual Port*

**Figure 1**
**Radial Cabling Configuration**




*(a) Single Port*




NOTE: Optional configuration defined in Section 6.

(*b*) *Dual Port*

**Figure 2**
**Daisy-Chain Cabling Configuration**

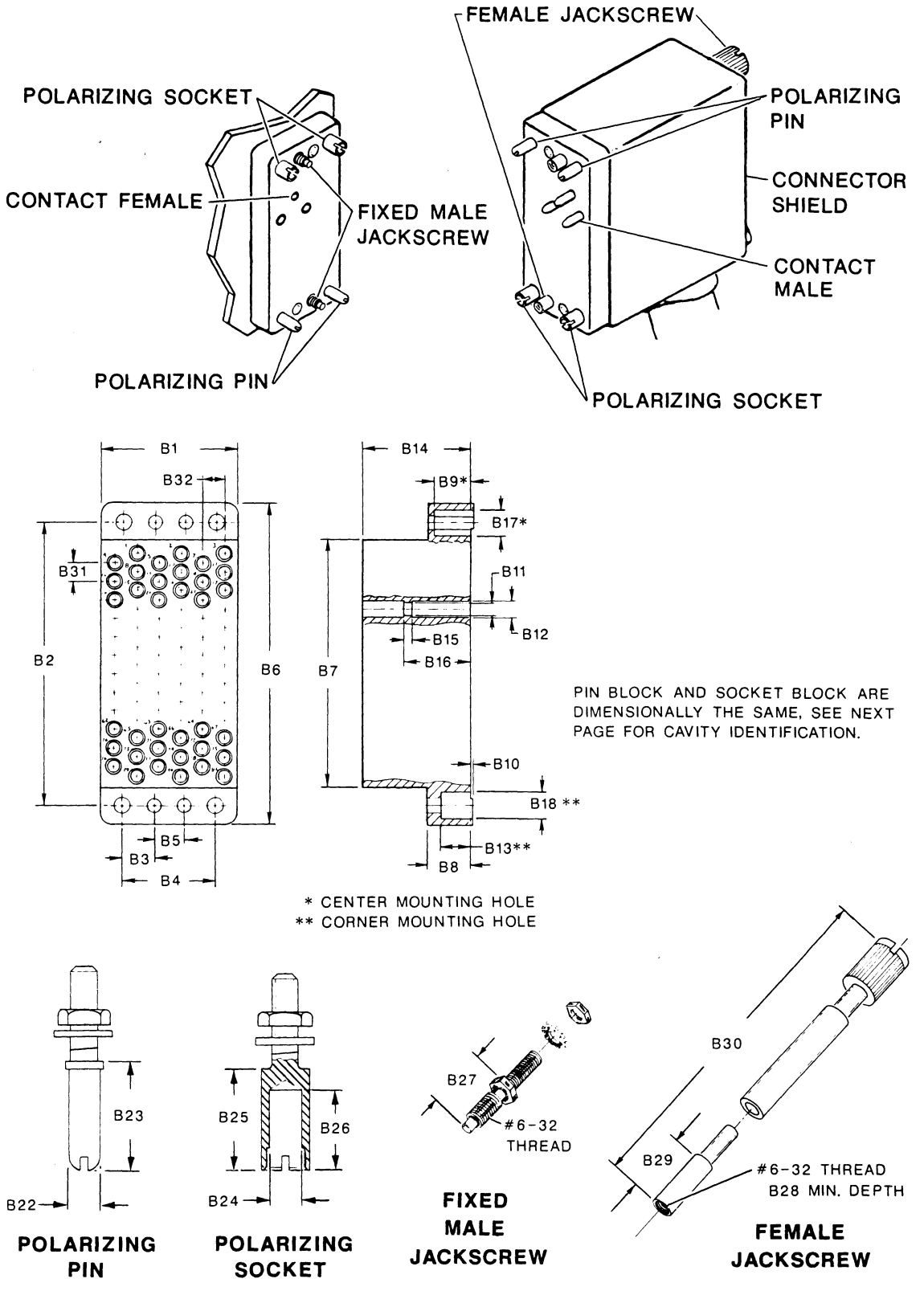
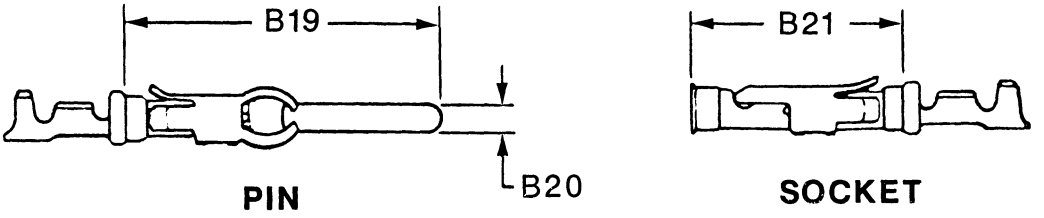
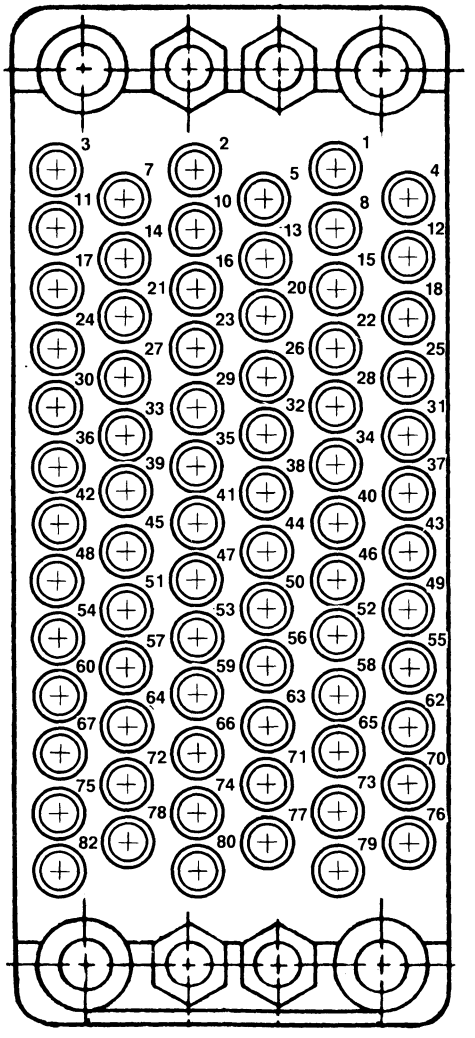



Figure 3
CONTROL Round Cable Connectors



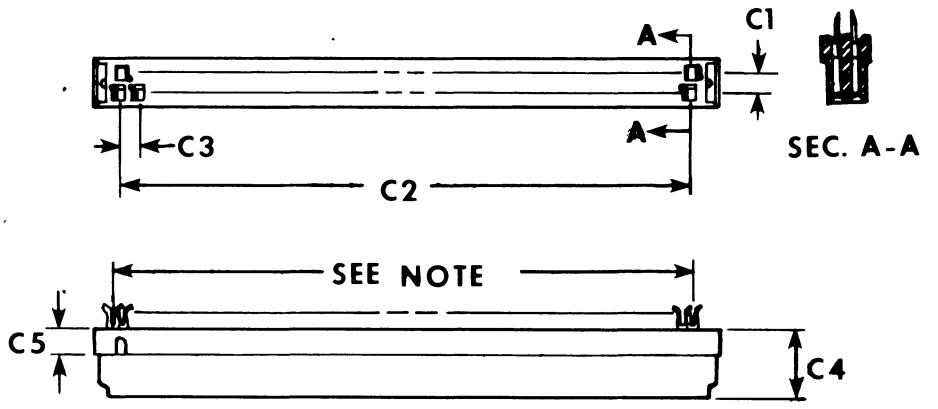



| Dimensions | Inches | Millimeters |
|---|---|---|
| B1 | 1.110 | 28.19 |
| B2 | 2.281 | 57.94 |
| B3 | 0.266 | 6.75 |
| B4 | 0.766 | 19.45 |
| B5 | 0.234 | 5.94 |
| B6 | 2.595 | 65.91 |
| B7 | 1.983 | 50.37 |
| B8 | 0.365 | 9.27 |
| B9 | 0.300 | 7.62 |
| B10 | 0.011* | 0.28* |
| B11 | 0.115 | 2.92 |
| B12 | 0.131 | 3.33 |
| B13 | 0.250 | 6.35 |
| B14 | 0.915 | 23.24 |
| B15 | 0.054 | 1.37 |
| B16 | 0.554 | 14.07 |
| B17 | 0.195 | 4.95 |
| B18 | 0.234† | 5.94† |
| B19 | 0.797 | 20.24 |
| B20 | 0.062† | 1.57† |
| B21 | 0.529 | 13.44 |
| B22 | 0.130 Max† | 3.30 Max* |
| B23 | 0.440 | 11.17 |
| B24 | 0.133† | 3.38† |
| B25 | 0.405 | 10.29 |
| B26 | 0.330 | 8.38 |
| B27 | 0.465 | 11.81 |
| B28 | 0.312 | 7.92 |
| B29 | 0.485 | 12.32 |
| B30 | 2.305 | 58.55 |
| B31 | 0.150* | 3.81* |
| B32 | 0.180* | 4.57* |

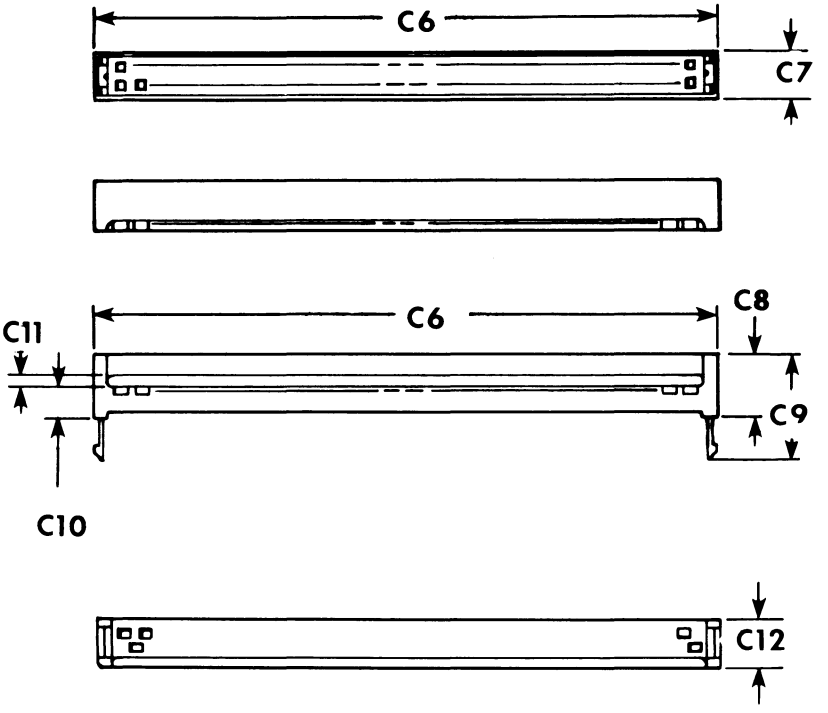
*Typical
†Diameter

NOTE: Circuit identification for pin block.
Socket block identification is mirror image.

**Figure 3 (*Continued*)**




NOTE: 60 contacts on 0.050 inch (1.27 mm) staggered spacing = 2.950 inches (74.93 mm)

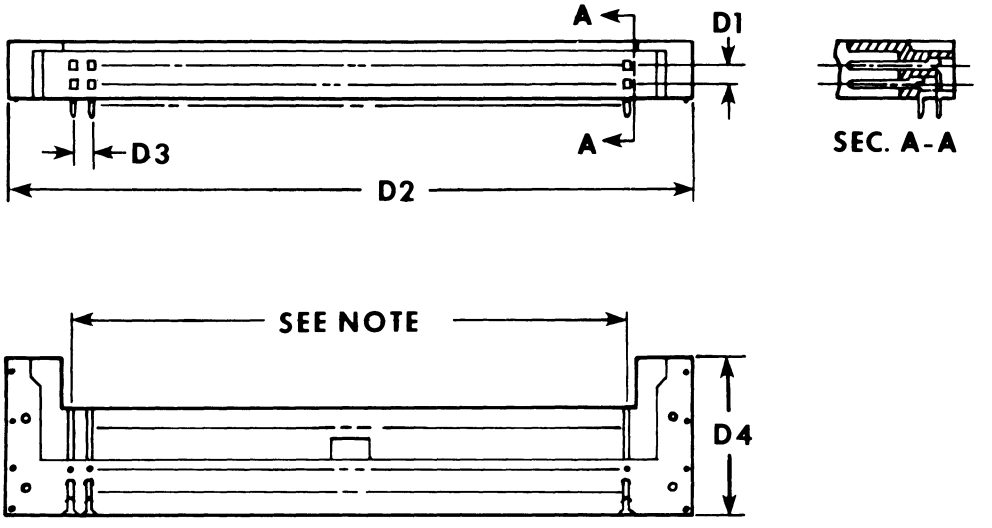




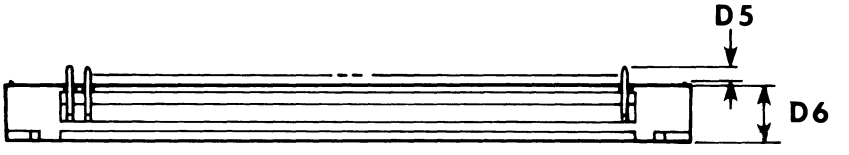


| Dimensions | Inches | Millimeters |
|---|---|---|
| C1 | 0.100 | 2.54 |
| C2 | 2.900 | 73.66 |
| C3 | 0.100 | 2.54 |
| C4 | 0.392 | 9.96 |
| C5 | 0.130 | 3.30 |
| C6 | 3.180 | 80.77 |
| C7 | 0.240 | 6.10 |
| C8 | 0.312 | 7.92 |
| C9 | 0.531 | 13.49 |
| C10 | 0.150 | 3.81 |
| C11 | 0.050 | 1.27 |
| C12 | 0.240 | 6.10 |

**Figure 4**
**CONTROL Flat Cable Plug**




NOTE: 60 contacts on 0.100 inch (2.54 mm) spacing = 2.90 inches (73.66 mm)




| Dimensions | Inches | Millimeters |
|---|---|---|
| D1 | 0.100 | 2.54 |
| D2 | 3.580 | 90.93 |
| D3 | 0.100 | 2.54 |
| D4 | 0.810 | 20.57 |
| D5 | 0.092 | 2.34 |
| D6 | 0.295 | 7.49 |

**Figure 5**
**CONTROL Flat Cable Receptacle**

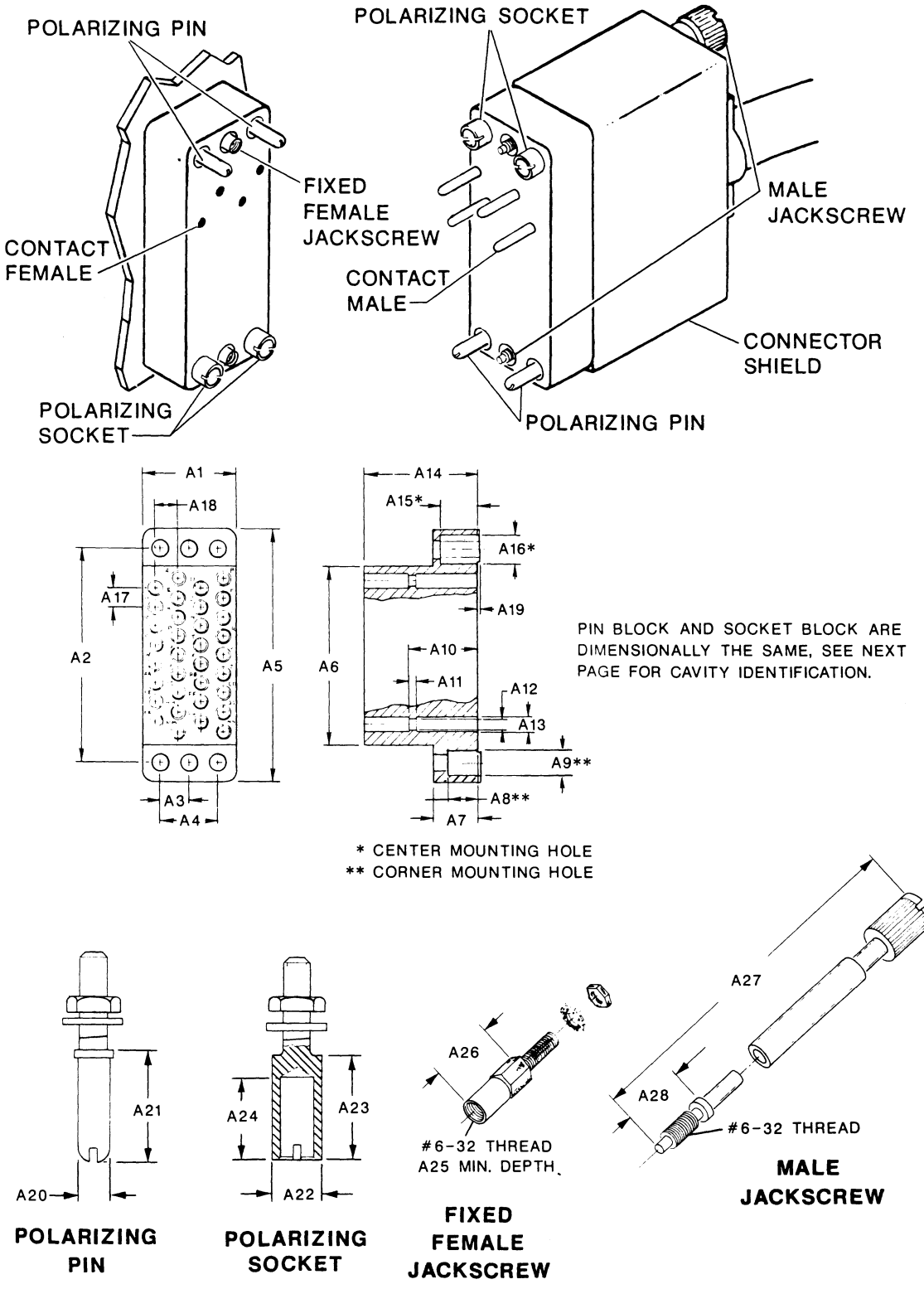
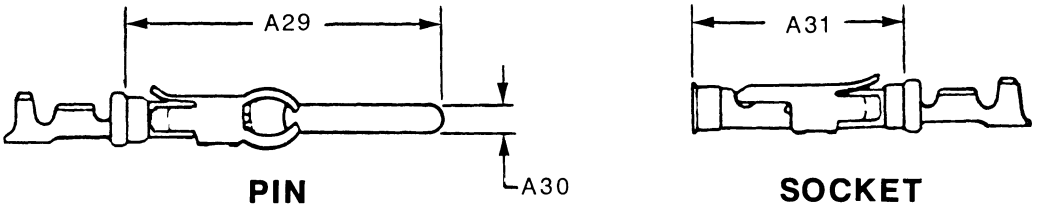
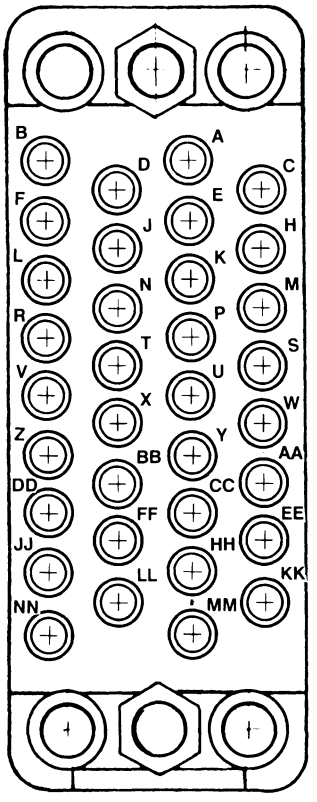



Figure 6
READ/WRITE Round Cable Connectors



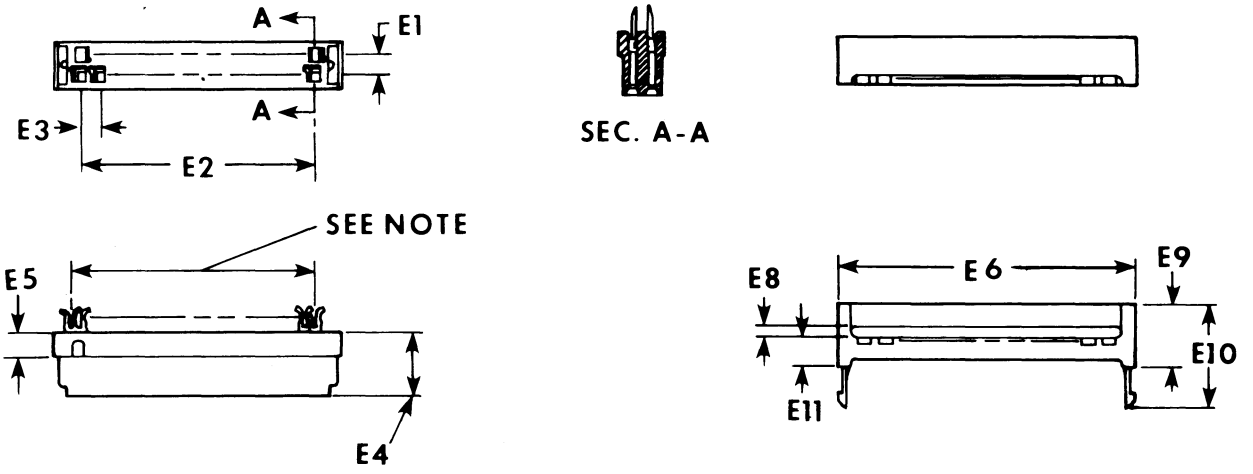




| Dimensions | Inches | Millimeters |
|---|---|---|
| A1 | 0.750 | 19.05 |
| A2 | 1.686 | 42.85 |
| A3 | 0.234 | 5.94 |
| A4 | 0.468 | 11.89 |
| A5 | 2.000 | 50.80 |
| A6 | 1.411 | 35.84 |
| A7 | 0.365 | 9.27 |
| A8 | 0.250 | 6.35 |
| A9 | 0.218* | 5.54* |
| A10 | 0.554 | 14.07 |
| A11 | 0.054 | 1.37 |
| A12 | 0.115 | 2.92 |
| A13 | 0.131 | 3.33 |
| A14 | 0.915 | 23.24 |
| A15 | 0.300 | 7.62 |
| A16 | 0.195 | 4.95 |
| A17 | 0.150† | 3.81† |
| A18 | 0.180† | 4.57† |
| A19 | 0.011† | 0.28† |
| A20 | 0.130 Max* | 3.30 Max* |
| A21 | 0.440 | 11.17 |
| A22 | 0.141* | 3.58* |
| A23 | 0.405 | 10.29 |
| A24 | 0.330 | 8.38 |
| A25 | 0.312 | 7.92 |
| A26 | 0.485 | 12.32 |
| A27 | 2.285 | 58.04 |
| A28 | 0.465 | 11.81 |
| A29 | 0.797 | 20.24 |
| A30 | 0.062* | 1.57* |
| A31 | 0.529 | 13.44 |

*Diameter
†Typical

NOTE: Circuit identification for pin block. Socket block identification is mirror image.

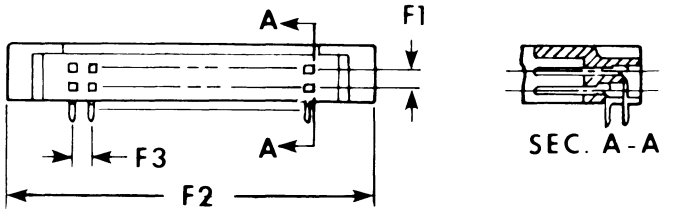
**Figure 6 (*Continued*)**

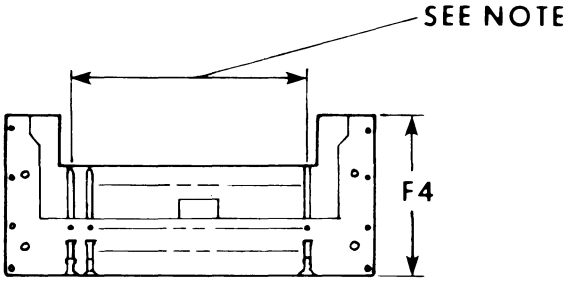



NOTE: 26 contacts on 0.050 inch (1.27 mm)
staggered spacing = 1.250 inches (31.75 mm)

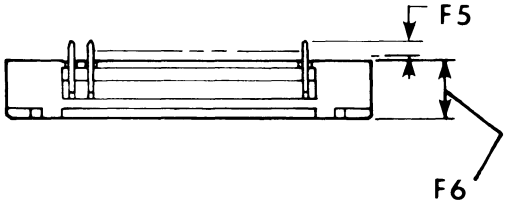

| Dimensions | Inches | Millimeters |
|---|---|---|
| E1 | 0.100 | 2.54 |
| E2 | 1.200 | 30.48 |
| E3 | 0.100 | 2.54 |
| E4 | 0.329 | 8.36 |
| E5 | 0.130 | 3.30 |
| E6 | 1.480 | 37.59 |
| E7 | 0.240 | 6.10 |
| E8 | 0.050 | 1.27 |
| E9 | 0.321 | 8.15 |
| E10 | 0.531 | 13.49 |
| E11 | 0.150 | 3.81 |
| E12 | 0.240 | 6.10 |

**Figure 7**
**READ/WRITE Flat Cable Plug**



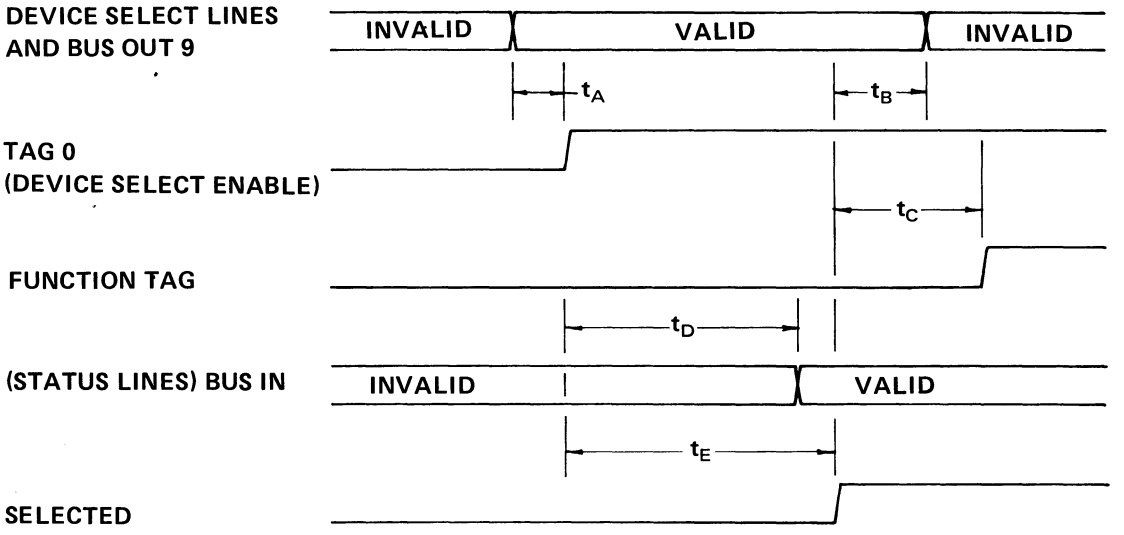




NOTE: 26 contacts on 0.100 inch (2.54 mm) spacing = 1.200 inches (30.48 mm)



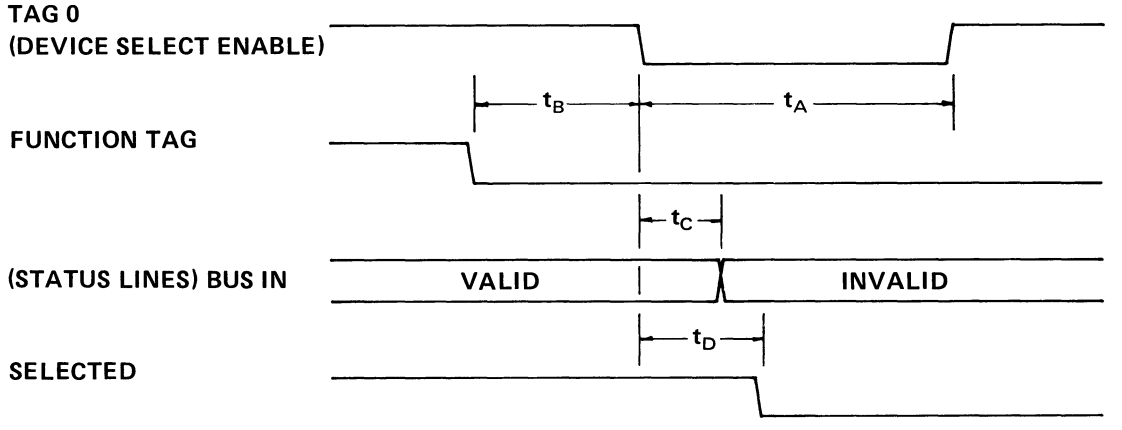

| Dimensions | Inches | Millimeters |
|---|---|---|
| F1 | 0.100 | 2.54 |
| F2 | 1.880 | 47.75 |
| F3 | 0.100 | 2.54 |
| F4 | 0.810 | 20.57 |
| F5 | 0.092 | 2.34 |
| F6 | 0.295 | 7.49 |

**Figure 8**
**READ/WRITE Flat Cable Receptacle**



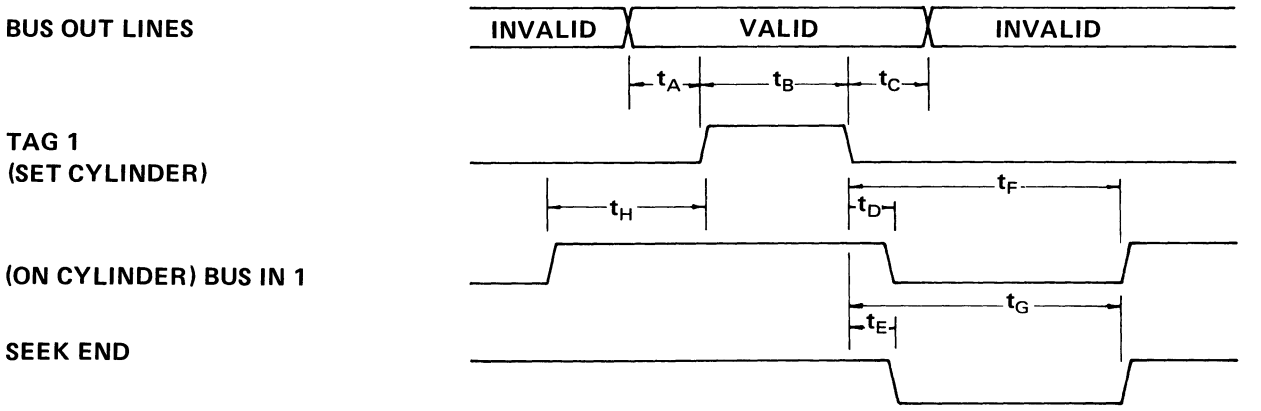

| Reference | Comments | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $t_A$ | – | 0.5 | – | – | Microseconds |
| $t_B$ | – | 0.5 | – | – | Microseconds |
| $t_C$ | – | 1.0 | – | – | Microseconds |
| $t_D$ | – | – | – | 1.0 | Microseconds |
| $t_E$ | – | – | – | 1.0 | Microseconds |

**Figure 9**
**Device Selection Sequence**



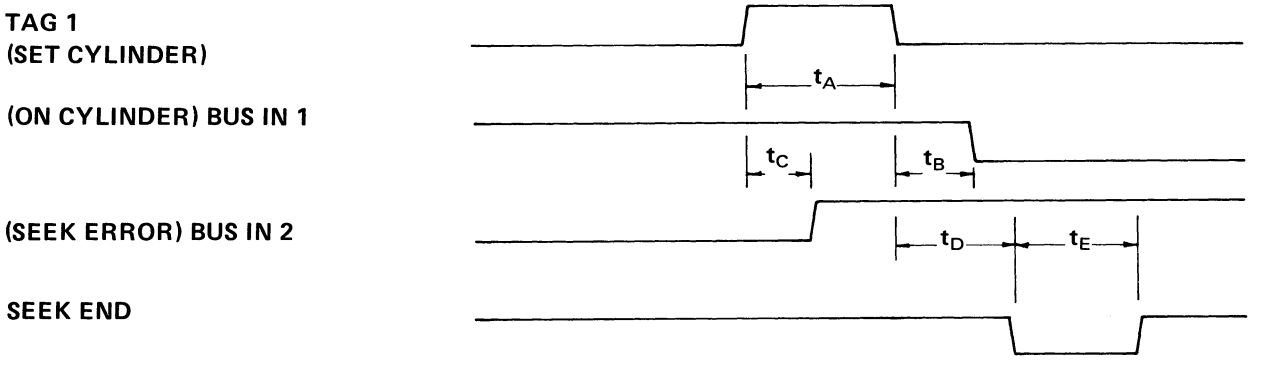

| Reference | Comments | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $t_A$ | – | 1.0 | – | – | Microseconds |
| $t_B$ | – | 0.5 | – | – | Microseconds |
| $t_C$ | – | 0 | – | 1.0 | Microseconds |
| $t_D$ | – | – | – | 1.0 | Microseconds |

**Figure 10**
**Device Deselection Sequence**




| Reference | Comments | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $t_A$ | – | 0.5 | – | – | Microseconds |
| $t_B$ | – | 1.0 | – | 500 | Microseconds |
| $t_C$ | – | 0.5 | – | – | Microseconds |
| $t_D$ | – | – | – | 0.5 | Microseconds |
| $t_E$ | – | – | – | 0.5 | Microseconds |
| $t_F$ | – | 4.0 | – | – | Microseconds |
| $t_G$ | – | 4.0 | – | – | Microseconds |
| $t_H$ | – | 0.5 | – | – | Microseconds |

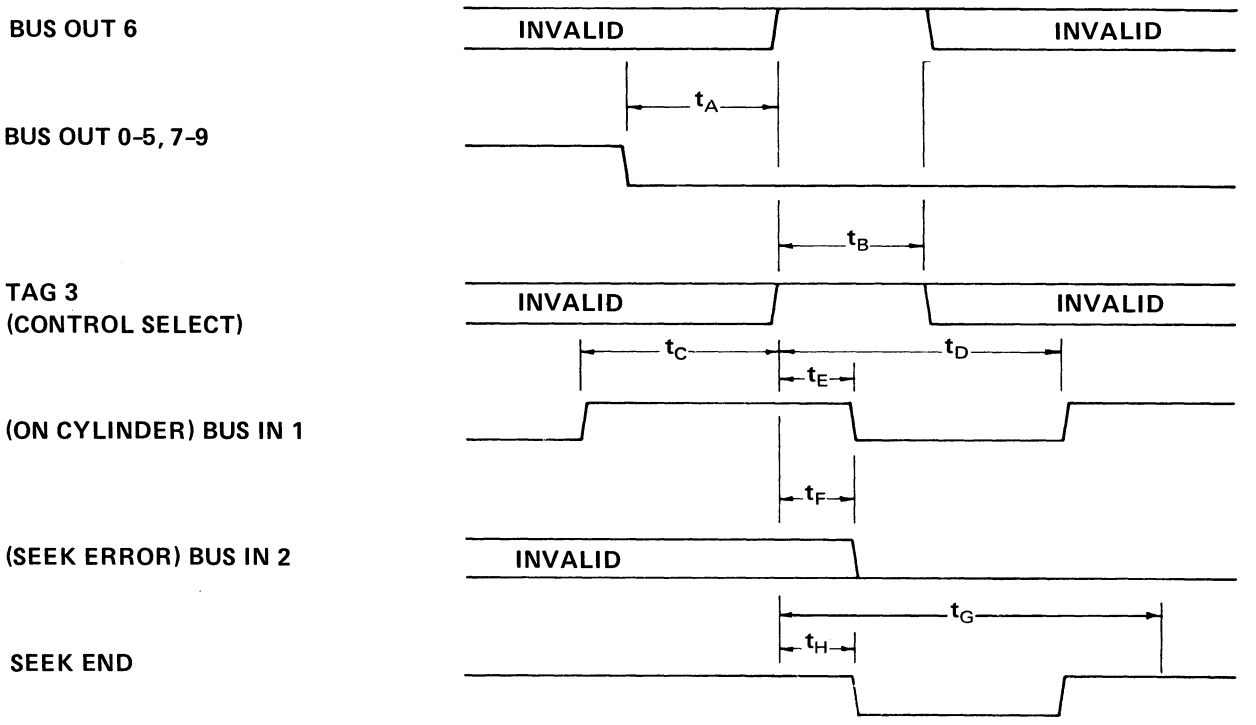
*(a) Valid Cylinder Address*




| Reference | Comments | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $t_A$ | – | 1.0 | – | 500 | Microseconds |
| $t_B$ | – | – | – | 0.5 | Microseconds |
| $t_C$ | – | – | – | 450 | Microseconds |
| $t_D$ | – | – | – | 0.5 | Microseconds |
| $t_E$ | – | 4.0 | – | – | Microseconds |

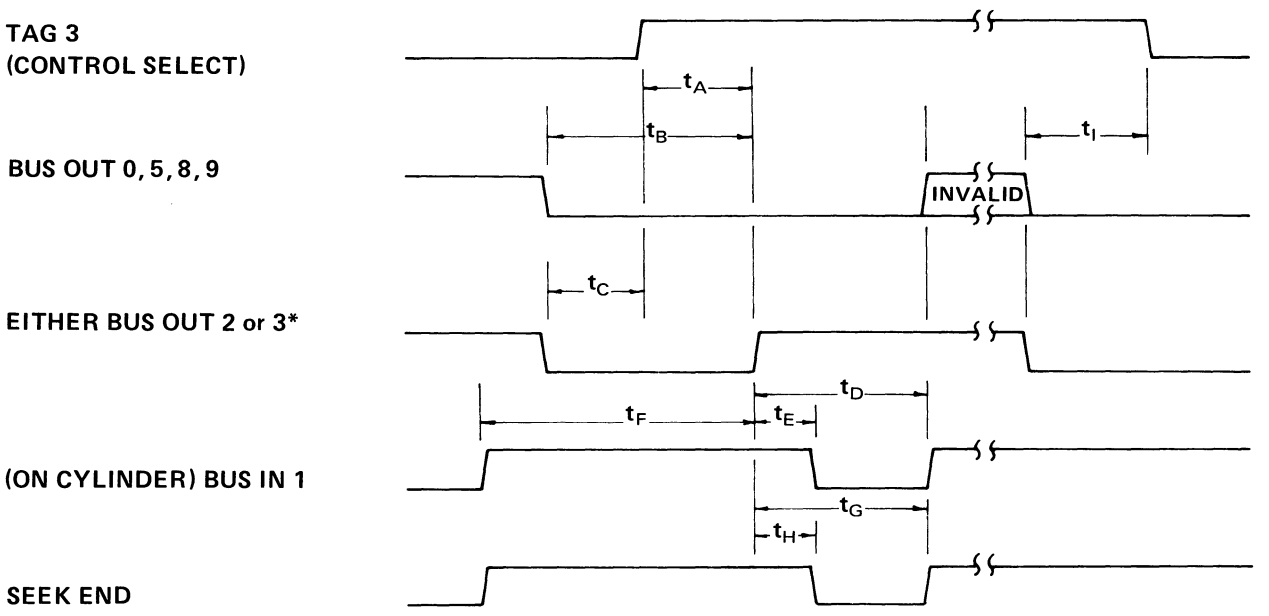
*(b) Invalid Cylinder Address*

**Figure 11**
**SEEK Command Sequence**




| Reference | Comments | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $t_A$ | – | 0.5 | – | – | Microseconds |
| $t_B$ | "LOGICAL AND" of CONTROL SELECT and BUS 6 | 1.0 | – | 500 | Microseconds |
| $t_C$ | – | 0.5 | – | – | Microseconds |
| $t_D$ | – | 1.0 | – | – | Microseconds |
| $t_E$ | – | – | – | 0.5 | Microseconds |
| $t_F$ | – | – | – | 0.5 | Microseconds |
| $t_G$ | – | 10.0 | – | – | Microseconds |
| $t_H$ | – | – | – | 0.5 | Microseconds |

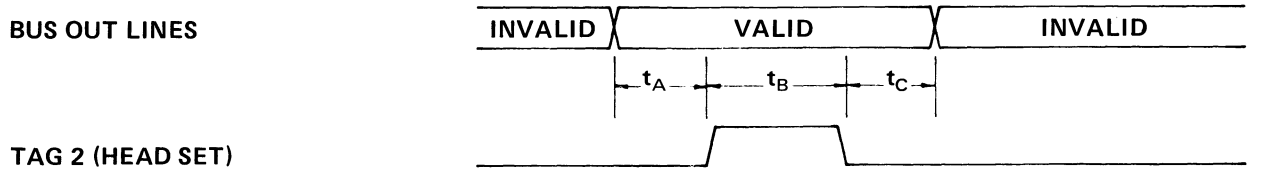
**Figure 12**
**REZERO Command Sequence**




*See 4.1.1.3.3(3) and 4.1.1.3.3(4).

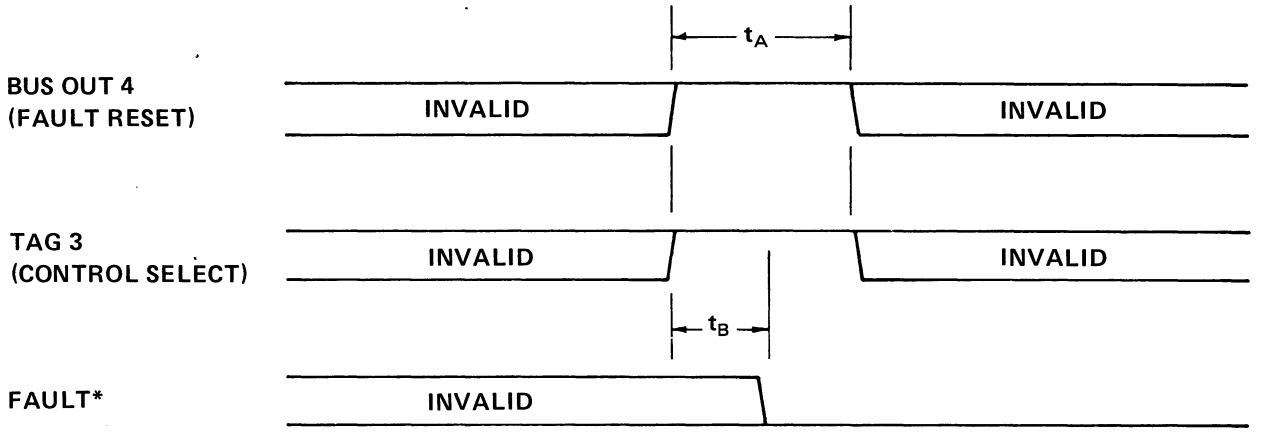
| Reference | Comments | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $t_A$ | – | 0 | – | – | Microseconds |
| $t_B$ | – | 0.5 | – | – | Microseconds |
| $t_C$ | – | 0.5 | – | – | Microseconds |
| $t_D$ | – | – | – | 10K | Microseconds |
| $t_E$ | – | – | – | 0.5 | Microseconds |
| $t_F$ | – | 0.5 | – | – | Microseconds |
| $t_G$ | – | – | $t_D$ | – | Microseconds |
| $t_H$ | – | – | – | 0.5 | Microseconds |
| $t_I$ | – | 0 | – | – | Microseconds |

**Figure 13**
**OFFSET Command Sequence**




| Reference | Comments | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $t_A$ | – | 0.5 | – | – | Microseconds |
| $t_B$ | – | 1.0 | – | – | Microseconds |
| $t_C$ | – | 0.5 | – | – | Microseconds |

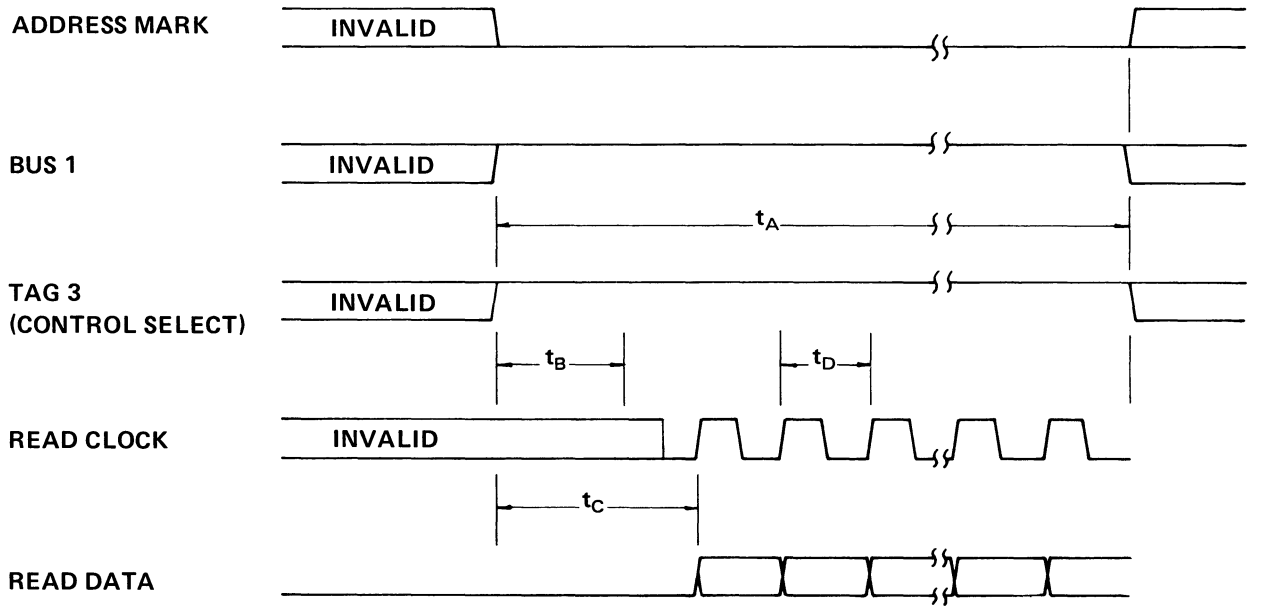
**Figure 14**
**HEAD SET Command Sequence**




| Reference | Comments | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $t_A$ | "LOGICAL AND" of CONTROL SELECT and BUS 4 | 0.5 | – | – | Microseconds |
| $t_B$ | – | – | – | 0.5 | Microseconds |

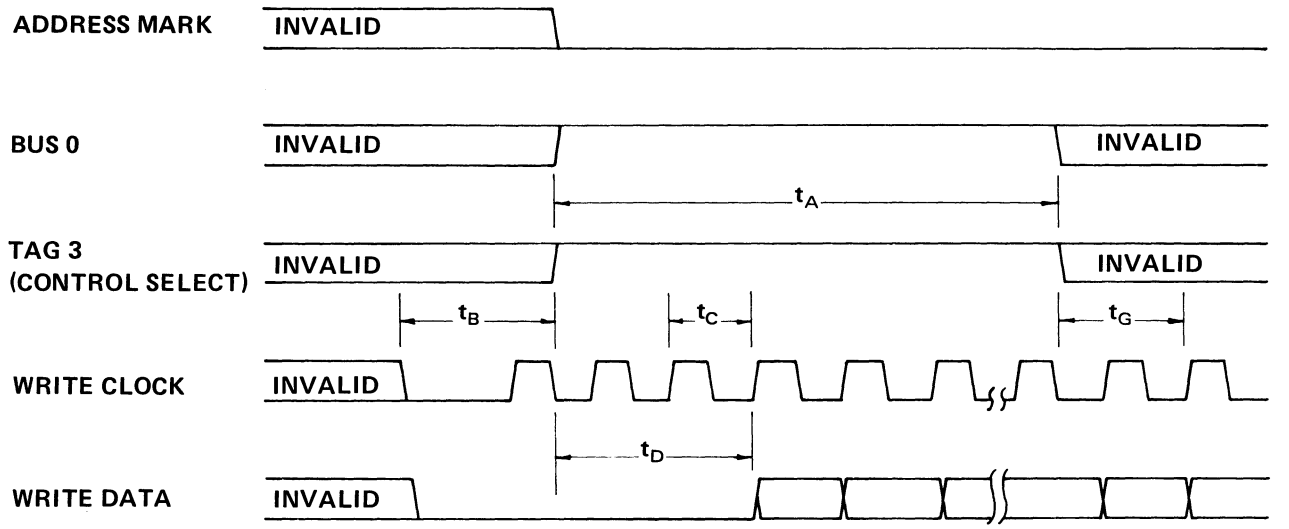
*Fault might not be cleared if a fault setting condition persists.

**Figure 15 – FAULT CLEAR Command Sequence**



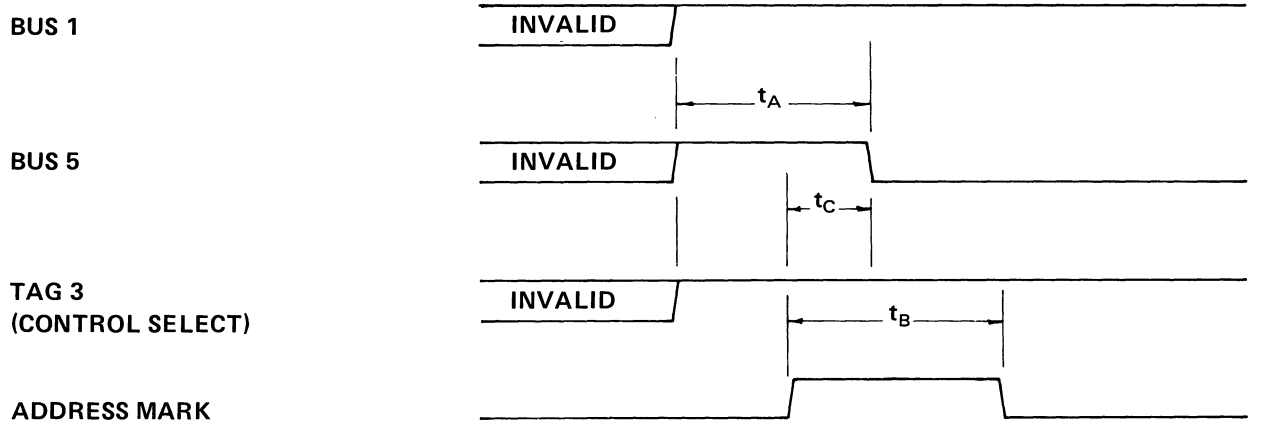

| Reference | Comments | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $t_A$ | "LOGICAL AND" of CONTROL SELECT BUS 1 | 0 | – | – | Microseconds |
| $t_B$ | Synchronization interval | – | – | 9 | Microseconds |
| $t_C$ | Zeroes field | $>t_B$ | – | – | Microseconds |
| $t_D$ | $T_P$ = Nominal bit period | – | $T_P$ | – | Microseconds |

**Figure 16 – READ Command Sequence**



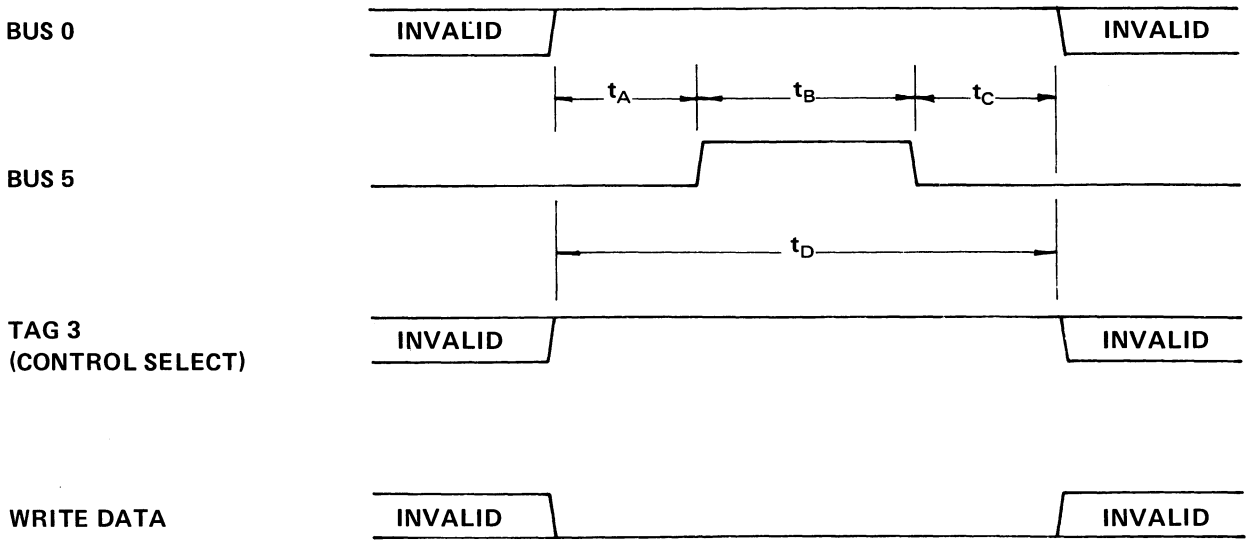

| Reference | Comments | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $t_A$ | "LOGICAL AND" of CONTROL SELECT and BUS 0 | 0 | – | – | Nanoseconds |
| $t_B$ | – | $2T_P$ | – | – | Nanoseconds |
| $t_C$ | $T_P$ = Nominal bit period | – | $T_P$ | – | Nanoseconds |
| $t_D$ | Synchronization interval | 9 | – | – | Microseconds |
| $t_G$ | – | $3T_P$ | – | – | Nanoseconds |

**Figure 17**
**WRITE Command Sequence**



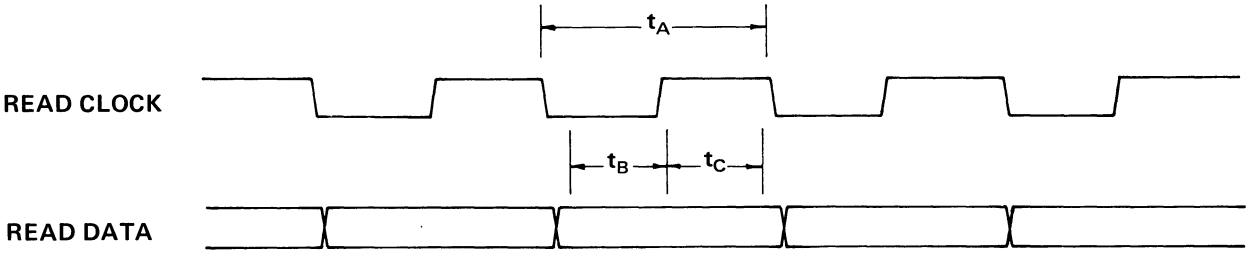

| Reference | Comments | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $t_A$ | "LOGICAL AND" of CONTROL SELECT, BUS 1, BUS 5 | 0 | – | – | Microseconds |
| $t_B$ | – | 1.0 | – | – | Microseconds |
| $t_C$ | – | 0 | – | 1.1 | Microseconds |

**Figure 18**
**READ ADDRESS MARK Command Sequence**



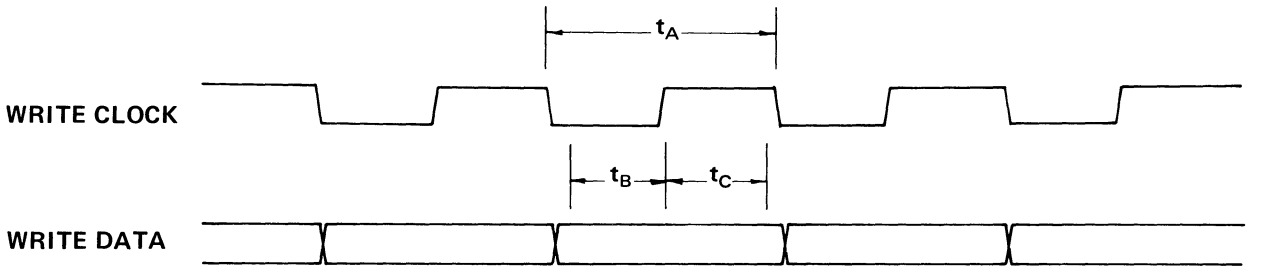

| Reference | Comments | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $t_A$ | – | 5.0 | – | – | Microseconds |
| $t_B$ | $T_P$ = Nominal bit period | $24T_P$ | – | $28T_P$ | Microseconds |
| $t_C$ | – | $8T_P$ | – | – | Microseconds |
| $t_D$ | "LOGICAL AND" of CONTROL SELECT, BUS 0 | – | – | – | Microseconds |

**Figure 19**
**WRITE ADDRESS MARK Command Sequence**



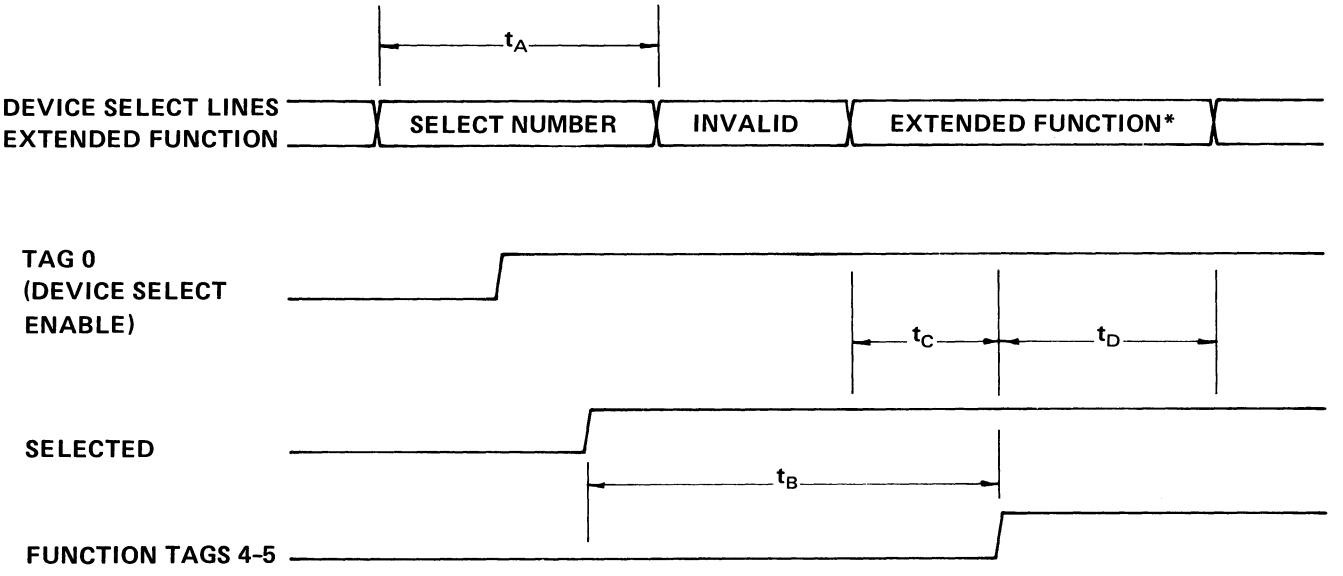

| Reference | Comments | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $t_A$ | T = Nominal bit period | 0.95Tp | $T_P$ | $1.05T_P$ | – |
| $t_B$ | Set-up time | 16 | – | – | Nanoseconds |
| $t_C$ | Hold time | 16 | – | – | Nanoseconds |

**Figure 20**
**READ CLOCK and READ DATA**




| Reference | Comments | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $t_A$ | T = Nominal bit period | 0.95Tp | $T_P$ | $1.05T_p$ | – |
| $t_B$ | Set-up time | 16 | – | – | Nanoseconds |
| $t_C$ | Hold time | 16 | – | – | Nanoseconds |

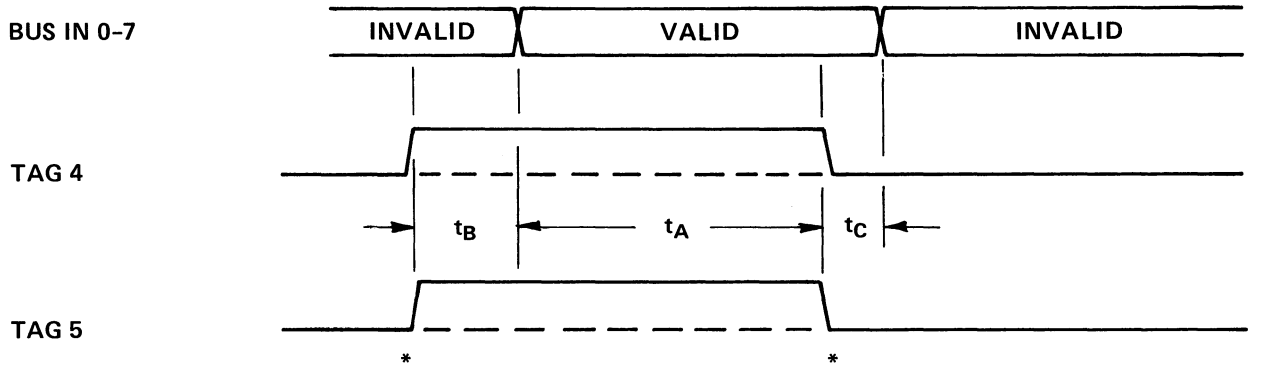
**Figure 21**
**WRITE CLOCK and WRITE DATA**




| Reference | Comments | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $t_A$ | See 5.1 | – | – | – | Microseconds |
| $t_B$ | Selected to any function tag | 1.0 | – | – | Microseconds |
| $t_C$ | Set-up time | 0.5 | – | – | Microseconds |
| $t_D$ | Hold time | 0.5 | – | – | Microseconds |

*DEVICE SELECT 8 = TAG 5; DEVICE SELECT 1, 2, 4 = INVALID.

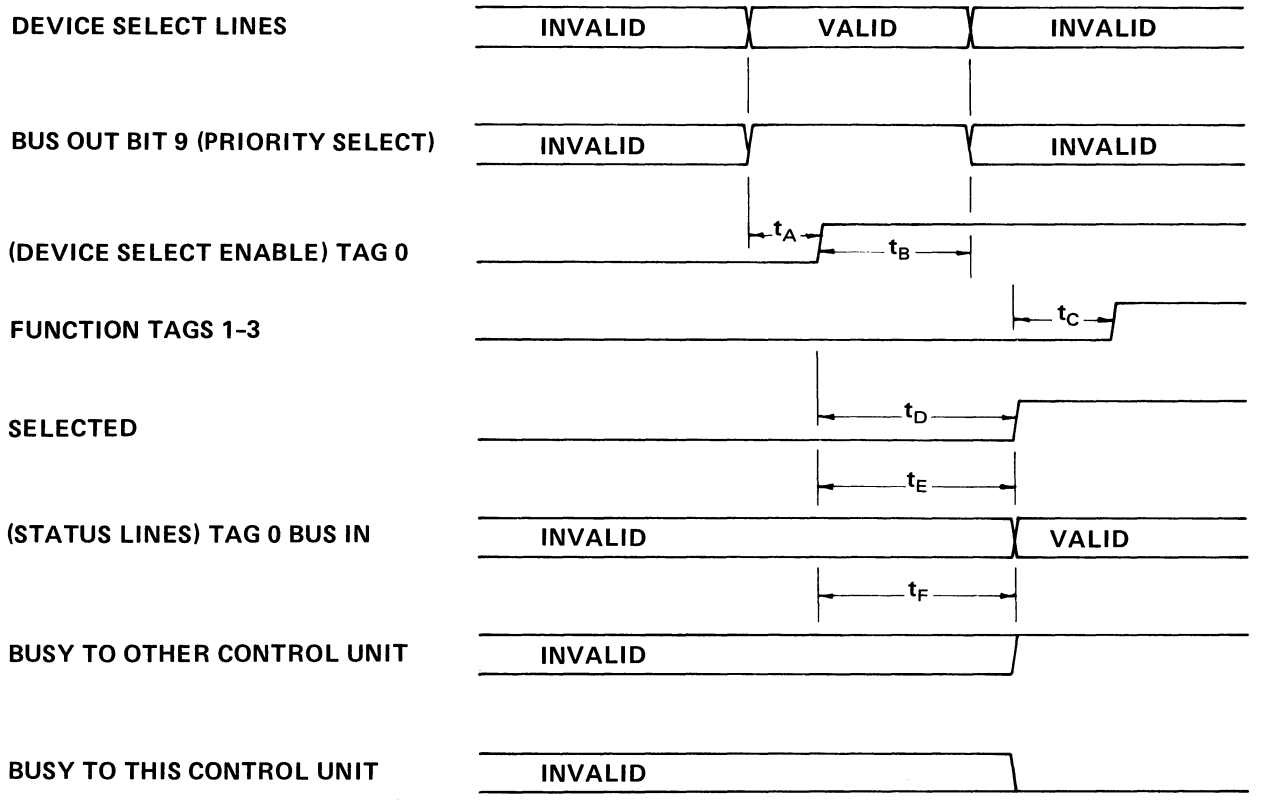
**Figure 22**
**Extended Functions**




| Reference | Comments | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $t_A$ | – | 0.5 | – | – | Microseconds |
| $t_B$ | – | – | – | 1.0 | Microseconds |
| $t_C$ | – | 0.5 | – | – | Microseconds |

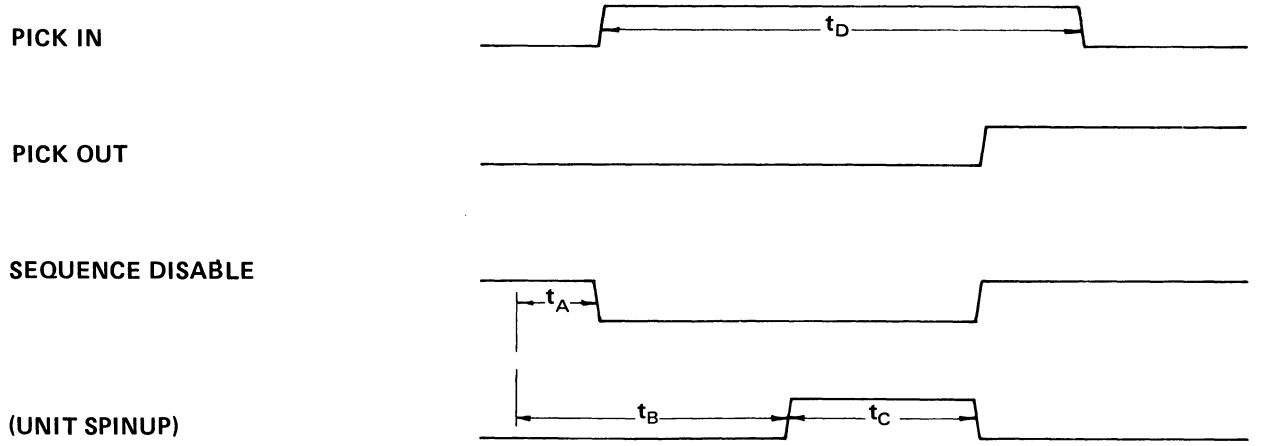
*Maximum skew of TAG 4 and TAG 5 edges = 0.1 microsecond.

**Figure 23**
**Extended Function Sequence**




| Reference | Comments | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $t_A$ | – | 0.5 | – | – | Microseconds |
| $t_B$ | – | 0.5 | – | – | Microseconds |
| $t_C$ | – | 0.5 | – | – | Microseconds |
| $t_D$ | – | – | – | 1.0 | Microseconds |
| $t_E$ | – | – | – | 1.0 | Microseconds |
| $t_F$ | – | – | – | 1.0 | Microseconds |

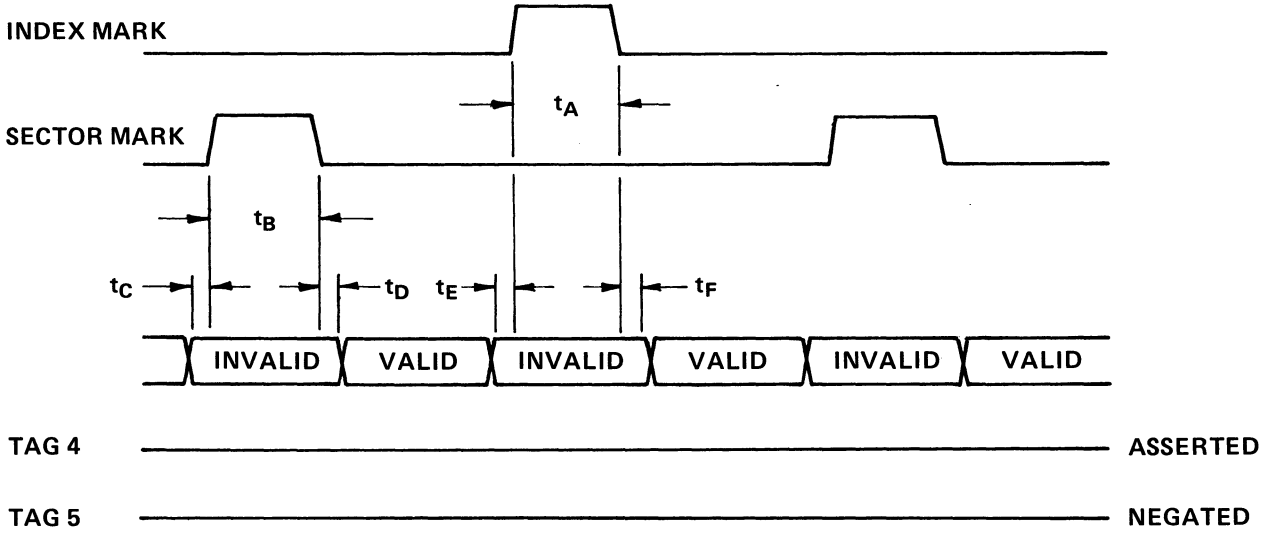
**Figure 24**
**Dual Port PRIORITY SELECT Command Sequence**




| Reference | Comments | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $t_A$ | – | 1.0 | – | – | Microseconds |
| $t_B$ | – | 10.0 | – | – | Microseconds |
| $t_C$ | – | – | 1.0 | – | Minutes |
| $t_D$ | – | Sum | – | – | See note |

NOTE: The sum of $t_B$ and $t_C$ for all units on a string.

**Figure 25 – Spinup Sequencing**




| Reference | Comments | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $t_A$ | – | 1.0 | – | – | Bytes |
| | | – | * | 5.0 | Microseconds |
| $t_B$ | – | 1.0 | – | – | Bytes |
| | | – | * | 5.0 | Microseconds |
| $t_C$ | – | 0.2 | – | – | Microseconds |
| $t_D$ | – | – | – | 0.3 | Microseconds |
| $t_E$ | – | 0.2 | – | – | Microseconds |
| $t_F$ | – | – | 0.3 | 0.3 | Microseconds |

*See vendor specifications for typical value.

**Figure 26 – INDEX and SECTOR Timing**

**X3.115-1984** Unformatted 80 Megabyte Trident Pack for Use at 370 tpi and 6000 bpi (General, Physical, and Magnetic Characteristics)
**X3.116-1986** Recorded Magnetic Tape Cartridge, 4-Track, Serial 0.250 Inch (6.30 mm) 6400 bpi (252 bpmm), Inverted Modified Frequency Modulation Encoded
**X3.117-1984** Printable/Image Areas for Text and Facsimile Communication Equipment
**X3.118-1984** Financial Services – Personal Identification Number – PIN Pad
**X3.119-1984** Contact Start/Stop Storage Disk, 158361 Flux Transitions per Track, 8.268 Inch (210 mm) Outer Diameter and 3.937 inch (100 mm) Inner Diameter
**X3.120-1984** Contact Start/Stop Storage Disk
**X3.121-1984** Two-Sided, Unformatted, 8-Inch (200-mm), 48-tpi, Double-Density, Flexible Disk Cartridge for 13 262 ftpr Two-Headed Application
**X3.122-1986** Computer Graphics Metafile for the Storage and Transfer of Picture Description Information
**X3.124-1985** Graphical Kernel System (GKS) Functional Description
**X3.124.1-1985** Graphical Kernel System (GKS) FORTRAN Binding
**X3.125-1985** Two-Sided, Do
(130-mm), 48-tpi (1,9-tpmm)
bpr Use
**X3.126-1986** One- or Two-S
5.25-inch (130-mm), 96 Trac
**X3.127-1987** Unrecorded M
Interchange
**X3.128-1986** Contact Start-
Transitions per Track, 130-m
40-mm (1.575-in) Inner Diam
**X3.129-1986** Intelligent Peri
**X3.130-1986** Intelligent Peri
Specific Command Sets for M

**X3.131-1986** Small Computer Systems Interface
**X3.132-1987** Intelligent Peripheral Interface – Logical Device Generic Command Set for Optical and Magnetic Disks
**X3.133-1986** Database Language –NDL
**X3.135-1986** Database Language – SQL
**X3.136-1986** Serial Recorded Magnetic Tape Cartridge for Information Interchange, Four and Nine Track
**X3.139-1987** Fiber Distributed Data Interface (FDDI) Token Ring Media Access Control (MAC)
**X3.140-1986** Open Systems Interconnection – Connection Oriented Transport Layer Protocol Specification
**X3.141-1987** Data Communication Systems and Services – Measurement Methods for User-Oriented Performance Evaluation
**X3.146-1987** Device Level Interface for Streaming Cartridge and Cassette Tape Drives
**X3.147-1987** Intelligent Peripheral Interface – Logical Device Generic Command Set for Magnetic Tapes
**X3.153-1987** Open Systems Interconnection – Basic Connection Oriented Session Protocol Specification
**X11.1-1977** Programming Language MUMPS
**IEEE 416-1978** Abbreviated Test Language for All Systems (ATLAS)
**IEEE 716-1982** Standard C/ATLAS Language
tandard C/ATLAS Syntax
**983** Programming Language PASCAL
uide to the Use of ATLAS
ecifications for a Data Descriptive File for
hange
**983** Reference Manual for the Ada Programming

Fingerprint Identification – Data Format for
hange

nary for Information Processing Systems
)

# American National Standards for Information

**X3.1-1976** Synchronous Signaling Rates for Data Transmission
**X3.2-1970** Print Specifications for Magnetic Ink Character Recognition
**X3.4-1986** Coded Character Sets – 7-Bit ASCII
**X3.5-1970** Flowchart Symbols and Their Usage
**X3.6-1965** Perforated Tape Code
**X3.9-1978** Programming Language FORTRAN
**X3.11-1969** General Purpose Paper Cards
**X3.14-1983** Recorded Magnetic Tape (200 CPI, NRZI)
**X3.15-1976** Bit Sequencing of the American National Standard Code for Information Interchange in Serial-by-Bit Data Transmission
**X3.16-1976** Character Structure and Character Parity Sense for Serial-by-Bit Data Communication in the American National Standard Code for Information Interchange
**X3.17-1981** Character Set for Optical Character Recognition (OCR-A)
**X3.18-1974** One-Inch Perforated Paper Tape
**X3.19-1974** Eleven-Sixteenths-Inch Perforated Paper Tape
**X3.20-1967** Take-Up Reels for One-Inch Perforated Tape
**X3.21-1967** Rectangular Holes in Twelve-Row Punched Cards
**X3.22-1983** Recorded Magnetic Tape (800 CPI, NRZI)
**X3.23-1985** Programming Language COBOL
**X3.25-1976** Character Structure and Character Parity Sense for Parallel-by-Bit Data Communication in the American National Standard Code for Information Interchange
**X3.26-1980** Hollerith Punched Card Code
**X3.27-1978** Magnetic Tape Labels and File Structure
**X3.28-1976** Procedures for the Use of the Communication Control Characters of American National Standard Code for Information Interchange in Specified Data Communication Links
**X3.29-1971** Specifications for Properties of Unpunched Oiled Paper Perforator Tape
**X3.30-1986** Representation for Calendar Date and Ordinal Date
**X3.31-1973** Structure for the Identification of the Counties of the United States
**X3.32-1973** Graphic Representation of the Control Characters of American National Standard Code for Information Interchange
**X3.34-1972** Interchange Rolls of Perforated Tape
**X3.37-1980** Programming Language APT
**X3.38-1972** Identification of States of the United States (Including the District of Columbia)
**X3.39-1986** Recorded Magnetic Tape (1600 CPI, PE)
**X3.40-1983** Unrecorded Magnetic Tape (9-Track 800 CPI, NRZI; 1600 CPI, PE; and 6250 CPI, GCR)
**X3.41-1974** Code Extension Techniques for Use with the 7-Bit Coded Character Set of American National Standard Code for Information Interchange
**X3.42-1975** Representation of Numeric Values in Character Strings
**X3.43-1986** Representations of Local Time of Day
**X3.44-1974** Determination of the Performance of Data Communication Systems
**X3.45-1982** Character Set for Handprinting
**X3.46-1974** Unrecorded Magnetic Six-Disk Pack (General, Physical, and Magnetic Characteristics)
**X3.47-1977** Structure for the Identification of Named Populated Places and Related Entities of the States of the United States for Information Interchange
**X3.48-1986** Magnetic Tape Cassettes (3.81-mm [0.150-Inch] Tape at 32 bpmm [800 bpi], PE)
**X3.49-1975** Character Set for Optical Character Recognition (OCR-B)
**X3.50-1986** Representations for U.S. Customary, SI, and Other Units to Be Used in Systems with Limited Character Sets
**X3.51-1986** Representations of Universal Time, Local Time Differentials, and United States Time Zone References
**X3.52-1976** Unrecorded Single-Disk Cartridge (Front Loading, 2200 BPI) (General, Physical, and Magnetic Requirements)
**X3.53-1976** Programming Language PL/I
**X3.54-1986** Recorded Magnetic Tape (6250 CPI, Group Coded Recording)
**X3.55-1982** Unrecorded Magnetic Tape Cartridge, 0.250 Inch (6.30 mm), 1600 bpi (63 bpmm), Phase encoded
**X3.56-1986** Recorded Magnetic Tape Cartridge, 4 Track, 0.250 Inch (6.30 mm), 1600 bpi (63 bpmm), Phase Encoded
**X3.57-1977** Structure for Formatting Message Headings Using the American National Standard Code for Information Interchange for Data Communication Systems Control
**X3.58-1977** Unrecorded Eleven-Disk Pack (General, Physical, and Magnetic Requirements)
**X3.60-1978** Programming Language Minimal BASIC
**X3.61-1986** Representation of Geographic Point Locations
**X3.62-1987** Paper Used in Optical Character Recognition (OCR) Systems
**X3.63-1981** Unrecorded Twelve-Disk Pack (100 Megabytes) (General, Physical, and Magnetic Requirements)
**X3.64-1979** Additional Controls for Use with American National Standard Code for Information Interchange
**X3.66-1979** Advanced Data Communication Control Procedures (ADCCP)
**X3.72-1981** Parallel Recorded Magnetic Tape Cartridge, 4 Track, 0.250 Inch (6.30 mm), 1600 bpi (63 bpmm), Phase Encoded
**X3.73-1980** Single-Sided Unformatted Flexible Disk Cartridge (for 6631-BPR Use)
**X3.74-1981** Programming Language PL/I, General-Purpose Subset
**X3.76-1981** Unformatted Single-Disk Cartridge (Top Loading, 200 tpi 4400 bpi) (General, Physical, and Magnetic Requirements)
**X3.77-1980** Representation of Pocket Select Characters
**X3.78-1981** Representation of Vertical Carriage Positioning Characters in Information Interchange
**X3.79-1981** Determination of Performance of Data Communications Systems That Use Bit-Oriented Communication Procedures
**X3.80-1981** Interfaces between Flexible Disk Cartridge Drives and Their Host Controllers
**X3.82-1980** One-Sided Single-Density Unformatted 5.25-Inch Flexible Disk Cartridge (for 3979-BPR Use)
**X3.83-1980** ANSI Sponsorship Procedures for ISO Registration According to ISO 2375
**X3.84-1981** Unformatted Twelve-Disk Pack (200 Megabytes)(General, Physical, and Magnetic Requirements
**X3.85-1981** 1/2-Inch Magnetic Tape Interchange Using a Self Loading Cartridge
**X3.86-1980** Optical Character Recognition (OCR) Inks
**X3.88-1981** Computer Program Abstracts
**X3.89-1981** Unrecorded Single-Disk, Double-Density Cartridge (Front Loading, 2200 bpi, 200 tpi) (General, Physical, and Magnetic Requirements)
**X3.91M-1987** Storage Module Interfaces
**X3.92-1981** Data Encryption Algorithm
**X3.93M-1981** OCR Character Positioning
**X3.94-1985** Programming Language PANCM
**X3.95-1982** Microprocessors – Hexadecimal Input/Output, Using 5-Bit and 7-Bit Teleprinters
**X3.96-1983** Continuous Business Forms (Single-Part)
**X3.98-1983** Text Information Interchange in Page Image Format (PIF)
**X3.99-1983** Print Quality Guideline for Optical Character Recognition (OCR)
**X3.100-1983** Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment for Packet Mode Operation with Packet Switched Data Communications Network
**X3.101-1984** Interfaces Between Rigid Disk Drive(s) and Host(s)
**X3.102-1983** Data Communication Systems and Services – User-Oriented Performance Parameters
**X3.103-1983** Unrecorded Magnetic Tape Minicassette for Information Interchange, Coplanar 3.81 mm (0.150 in)
**X3.104-1983** Recorded Magnetic Tape Minicassette for Information Interchange, Coplanar 3.81 mm (0.150 in), Phase Encoded
**X3.105-1983** Data Link Encryption
**X3.106-1983** Modes of Operation for the Data Encryption Algorithm
**X3.110-1983** Videotex/Teletext Presentation Level Protocol Syntax
**X3.111-1986** Optical Character Recognition (OCR) Matrix Character Sets for OCR-M
**X3.112-1984** 14-in (356-mm) Diameter Low-Surface-Friction Magnetic Storage Disk
**X3.113-1987** Programming Language FULL BASIC
**X3.114-1984** Alphanumeric Machines; Coded Character Sets for Keyboard Arrangements in ANSI X4.23-1982 and X4.22-1983

*(Continued on reverse)*