MULTIBUS OEM Products and Microprogrammable Development Tools

1984 Data Book

ADVANCED MICRO DEVICES

1

Advanced Micro Devices

Microcomputer Systems Data Book

901 Thompson Place, P.O. Box 3453, Sunnyvale, California 94088
(408) 732-2400 TWX: 910-339-9280 TELEX: 34-6306

Printed in U.S.A.

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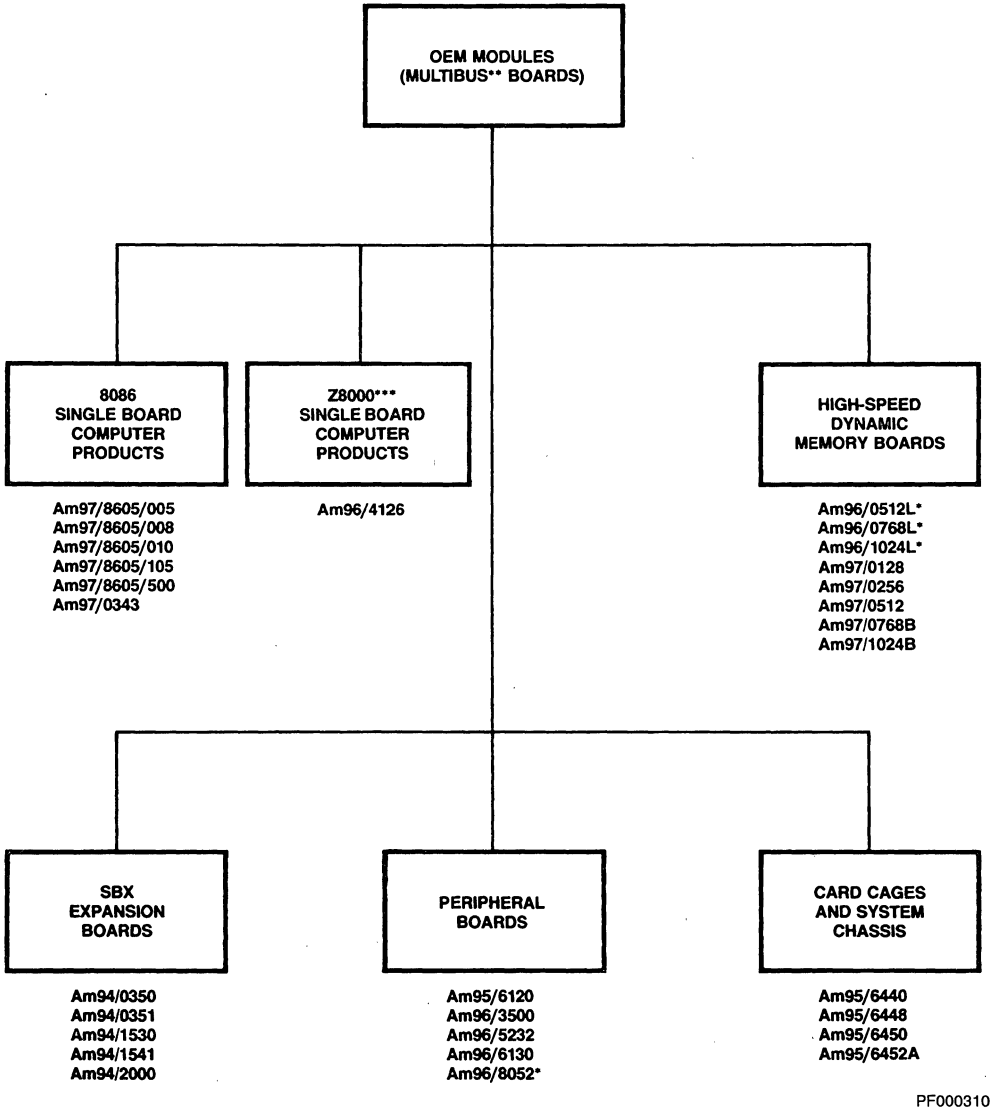

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*In development.

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Am97/8605

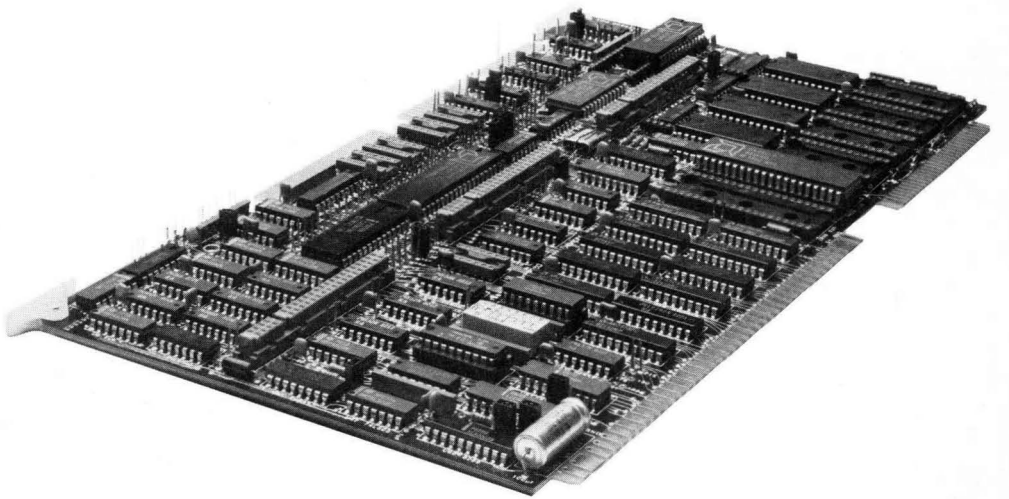
8086 16-Bit Single Board Computer

DISTINCTIVE CHARACTERISTICS

- 8086 microprocessor with 5,8, or 10MHz operation
- Fully software transparent with Intel iSBC*86/05 and iSBC 86/12
- On-board socket for 8087 Numeric Data Coprocessor
- Two 16-bit timers/event counters
- Two serial ports with optional Z80B-SIO/0
- Sockets for up to 64K bytes EPROM. Expandable on-board to 128K with memory module
- 24 programmable parallel I/O lines
- Nine levels of vectored interrupt control

GENERAL DESCRIPTION

The Am97/8605 is a complete 16-bit computer system on a single MULTIBUS* board. It includes CPU, 8K static RAM, EPROM sockets, counter/timers, 3 SBX connectors, and both serial and parallel I/O ports. The large EPROM capacity, extensive I/O, and modular expansion capabilities make the Am97/8605 ideally suited for industrial control and intelligent I/O applications. It is designed to work in both standalone and multiple CPU systems.



*iSBC and MULTIBUS are registered trademarks of Intel Corporation.

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PRODUCT OVERVIEW

The Am97/8605 is a powerful 16-bit single board computer that is based on the 8086 microprocessor and 8087 coprocessor. The Am97/8605 is a complete computer system on a single MULTIBUS board (see Figure 1). It includes CPU, static RAM, EPROM sockets, counter/timers, 3 SBX connectors, and both serial and parallel I/O ports. In addition, it has full MULTIBUS multimaster capability, interrupt logic, and is fully software compatible with the Intel iSBC 86/05 and iSBC 86/12 boards.

The large EPROM capacity, extensive I/O, and modular expansion capabilities make the Am97/8605 ideally suited for ROM-intensive control and I/O applications. It is designed to work as both a standalone CPU and as a slave CPU in a multiple master system.

The Am97/8605 is a very versatile CPU board. Custom I/O and special functions can be added with the addition of up to three SBX modules. Memory capacity can be doubled by adding an Am97/0343 Memory Expansion Module, and an additional serial port can be added by using the Z80B-SIO/0 Serial I/O chip. The Am97/8605 board comes in three CPU speeds (5,8, or 10MHz) and the 5MHz version can be ordered with or without an 8087 coprocessor.

Central Processing Unit

The Am97/8605 contains the high-performance, 16-bit 8086 microprocessor. The pipelined architecture of the 8086 incorporates both a bus interface unit and an execution unit. This enables the microprocessor to execute one instruction while at the same time fetching the next, thus greatly improving throughput.

The advanced architecture of the 8086 supports high-level languages and complex application programs. The microprocessor contains four 16-bit data registers, two 16-bit index registers and two 16-bit base pointer registers. It can directly access up to one megabyte of memory. The 8086 has 24 operand addressing modes for comprehensive memory addressing and for support of various data structures. The instruction set includes variable length instruction format, 8 and 16-bit signed and unsigned arithmetic operators for binary, BCD and ASCII data, and iterative word and byte string manipulation functions.

Basic Am97/8605 Components

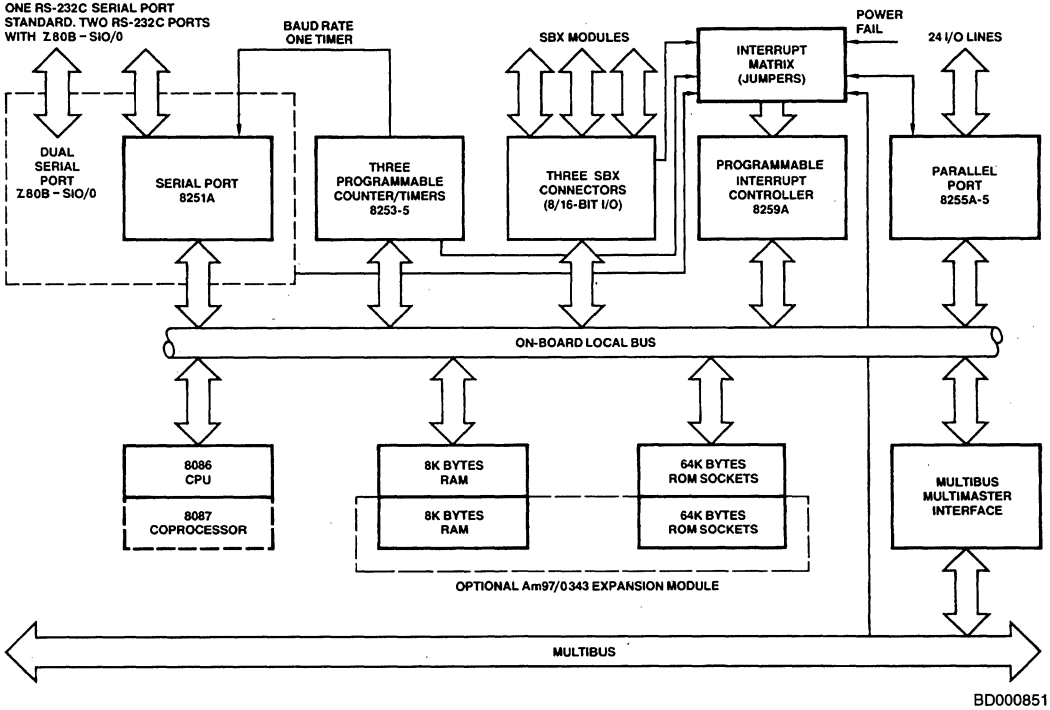
CPU	8086
Coprocessor	8087
Static RAM	9128 or 6116
Counter/Timers	8253-5
Serial I/O	8251A
Parallel I/O	8255A-5
Interrupt Controller	8259A

Numeric Data Coprocessor

The 8087 is a numeric coprocessor that can provide up to 100 times the performance of an 8086 alone for numeric processing. It performs arithmetic, transcendental, and comparison operations on a variety of numeric data types. It supports 32 and 64-bit floating point and 16, 32, and 64-bit integer numbers.

The 8087 works in parallel with the 8086. Both processors share the same data and address lines and communicate with each other through status lines. When the 8087 recognizes an instruction that it must execute, it gains control of the local

Figure 1. Am97/8605 Functional Block Diagram



bus. In this manner both the 8086 and 8087 can execute their own particular instructions.

The 8087 coprocessor is ideally suited for numerical-based application programs. A socket is provided on-board so that you may add the 8087 when ordering the board, or at a later date.

On-Board Memory

The Am97/8605 comes with 8K bytes of high-speed static RAM and four 28-pin memory sockets. The four sockets will accept any JEDEC standard 24/28-pin memory device for up to 64K bytes of EPROM memory. If more RAM and less EPROM is desired, two of the sockets may be used for static RAMs.

If additional memory is required, the Am97/0343 Memory Expansion Module can be added to double both RAM and EPROM capacity for a total of 16K bytes of RAM, and 128K bytes of EPROM (see Figure 2).

Full 20-bit addressing is utilized on the Am97/8605, allowing it to control up to one megabyte of memory over the MULTIBUS. Memory accesses are performed either a word (16 bits) at a time, or a byte (8 bits) at a time, for maximum flexibility.

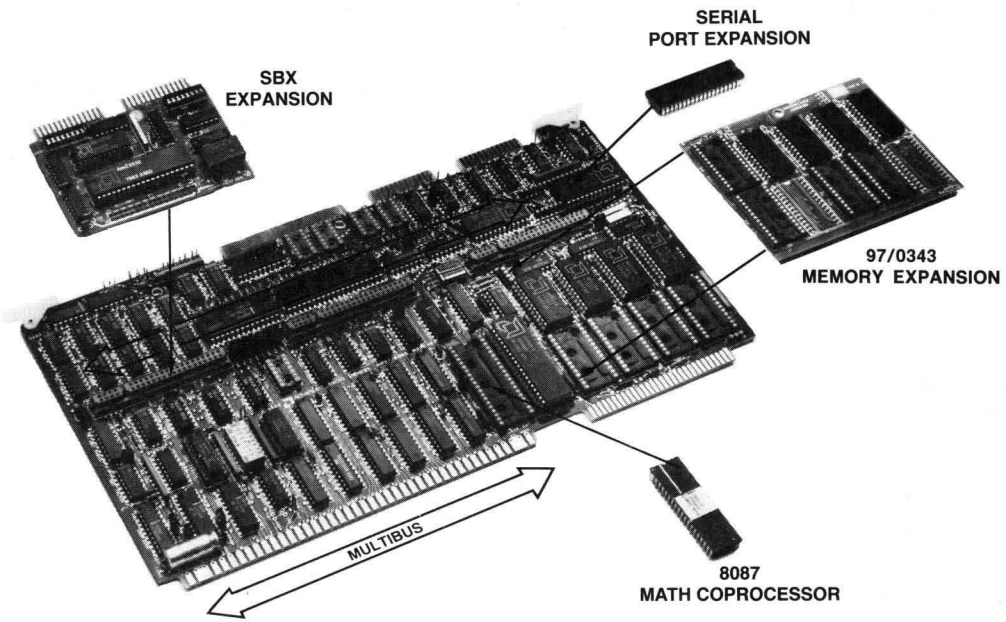
Serial I/O

The Am97/8605 will accommodate either an 8251A or Z80B-SIO/0 Serial I/O device. The 8251A comes with the board and provides a single RS-232C serial port. The 8251A can be replaced by an Z80B-SIO/0 which will provide two serial ports. Both devices feature software-selectable baud rates, synchronous and asynchronous operation, parity, data format and control character format. The serial lines are routed to two 26-pin edge connectors on top of the Am97/8605 board.

Parallel I/O

An 8255A-5 Programmable Peripheral Interface (PPI) device supplies 24 lines of parallel input/output capability to the Am97/8605. These lines can be programmed and hardware configured as three sets of 8-bit ports with either status-driven, polled, or interrupt-driven protocol. One of the ports is supplied with a bidirectional bus transceiver, while sockets are provided for drivers or terminators for the other two ports. A 50-pin edge connector is provided on top of the board to access the ports.

Figure 2. Am97/8605 Board Expansion



Programmable Timers

To handle timing, sequencing, and counting functions, the Am97/8605 board utilizes an 8253-5 Programmable Interval Timer. The 8253-5 has three independent, 16-bit interval timer/event counters. Each counter is capable of operating in either BCD or binary mode. Two counters are available to the systems' designer, while the third is dedicated for generating the baud rate for the serial port.

Interrupt Capability

Nine interrupt levels are supported on the Am97/8605. The non-maskable interrupt line is routed directly to the 8086, while an 8259A Programmable Interrupt Controller (PIC) handles eight vectored interrupt levels. The 8259A PIC efficiently oversees and controls the interface between I/O devices and the CPU. The 8259A features four priority processing modes including auto rotating, fully nested, polled and specific priority. In addition, the interrupt mask register can be programmed to mask a variety of interrupt levels. The number of interrupt levels is expandable to 64 by the addition of slave 8259A PICs on the MULTIBUS.

Multimaster Capability

Full MULTIBUS arbitration is provided on the Am97/8605 board through the use of an 8289 Bus Arbiter. The control logic allows up to three masters using serial priority resolution, and sixteen masters using parallel priority resolution. This capability makes the Am97/8605 particularly suited for devel-

opment and OEM applications requiring multiple master processors.

SBX Expansion

The Am97/8605 contains three 8/16-bit SBX type connectors for plug-in I/O expansion. These SBX connectors meet the Intel iSBX* specifications and can be used to add on-board I/O functions. By mounting modules directly on the Am97/8605 CPU board, less interface logic, less power, higher performance, and lower costs result when compared to alternative expansion methods.

*iSBX is a registered trademark of Intel Corp.

SPECIFICATIONS

CPU

8086 CPU with optional 8087 coprocessor

Word Size

Instruction	8, 16, 24, or 32 bits
Data	8 or 16 bits

System Clock

The Am97/8605 can be ordered with either a 5, 8, or 10MHz system clock.

System Clock (MHz)	5	8	10
CPU	8086	8086-2	8086-1
Coprocessor	8087		

CPU Cycle Time

At 10MHz	600ns
	200ns (with instruction in queue)
At 8MHz	750ns
	250ns (with instruction in queue)
At 5MHz	1200ns
	400ns (with instruction in queue)

Memory Cycle Time

RAM	150ns (no-wait-states)
EPROM	Jumper selectable from 200ns to 450ns

Memory Capacity and Addressing

On-Board RAM:
8K Bytes 0-1FFF H

On-Board EPROM:

Device	Total Capacity	Address Range
2716	8K Bytes	FE000 – FFFFF H
2732	16K Bytes	FC000 – FFFFF H
2764	32K Bytes	F8000 – FFFFF H
27128	64K Bytes	F0000 – FFFFF H

On-Board RAM with Am97/0343 Expansion Module:
16K Bytes 0-3FFF H

On-Board EPROM with Am97/0343 Expansion Module:

Device	Total Capacity	Address Range
2716	16K Bytes	FC000 – FFFFF H
2732	32K Bytes	F8000 – FFFFF H
2764	64K Bytes	F0000 – FFFFF H
27128	128K Bytes	E0000 – FFFFF H

Serial I/O

Configured for either one or two ports. The 8251A provides one serial port, while the Z80B-SIO/0 provides two.

Synchronous Baud Rates: 4,800 to 38,400
Asynchronous Baud Rates: 75 to 19,200

Synchronous Modes: 5/8-bit characters with internal or external character synchronization and automatic sync insertion.

Asynchronous Modes: 5/8-bit characters; break character generation; 1, 1-1/2, or 2 stop bits; and false start bit detection.

Parallel I/O

24 programmable lines are provided utilizing the 8255A-5 Programmable Peripheral Interface device.

Timers

Three independent, fully programmable, 16-bit timers/event counters are provided utilizing the 8253-5. Two of these are user-available, while the third is dedicated for baud rate generation.

Interfaces

MULTIBUS:	All signals three-state TTL, 32mA sink
Serial I/O:	RS-232C to J2A, J2B
Parallel I/O:	User-selectable
Interrupt:	TTL active-LOW, 9 levels
SBX:	Per Intel iSBX specifications

Connectors

Interface	Pins	Centers	Mating Connectors
MULTIBUS	86	0.156 in.	Viking 3KH43/9AMK12
Serial I/O	26	0.1 in.	3M 3462-0001 Flat or AMP 88106-1 Flat
Parallel I/O	50	0.1 in.	3M 3415-000 Flat or TI H312125 Pins

Physical Characteristics

Width:	12.00 in	(30.48 cm.)
Height:	6.50 in	(17.15 cm.)
Thickness:	0.50 in	(1.27 cm.)
Weight:	15 oz	(425 gr.)
Shipping Weight:	2.00 lbs	(907 gr.)

Electrical Characteristics

DC Power Requirements

+5 Volts	2.8Amps (Typical)
+12 Volts	40mA
-12 Volts	40mA

Reference Manual

0059920036-001-Am97/8605 16-Bit SingleBoard Computer

ORDERING INFORMATION

Part Number	Description
97/8605/005	5MHz 8086 CPU Board without an 8087
97/8605/008	8MHz 8086 CPU Board without an 8087
97/8605/010	10MHz 8086 CPU Board without an 8087
97/8605/105	5MHz 8086 CPU Board with an 8087
Options	
97/8605/500	EPROM Monitor for the Am97/8605
97/0343	Memory Expansion Module

RMX On The Am97/8605

Application Note by Bruce Pettner
AMD Microcomputer Systems Directorate

INTRODUCTION

Are customers asking you how to configure the Am97/8605 Single Board Computers to run RMX 86? If so, the following information should help get them started:

The fully configured RMX 86 system is a unique environment that utilizes the special capabilities of its associated hardware and software. Due to this flexibility, there are many possible jumper configurations for the CPU board (designated by the user, based on his application requirements). Keeping this in mind, however, it is possible to provide the customer with a "basic" jumper configuration that allows the iRMX* 86 Nucleus Demo, version 3.0, to be loaded and run on the Am97/8605 board.

The hardware configuration used in our test lab was:

1. Am97/8605/005 – 5MHz Single Board Computer
2. Am97/1024B – 1 Megabyte Dynamic RAM Board
3. Am95/6448 – Standard 6-Slot Card Cage w/power supply

The software used was iRMX 86, version 3.0, and the development tool used for down-loading the software was ICE* 86A (5MHz pod). Information on version 5.0 of iRMX 86 will be provided as it becomes available.

The following table shows the basic jumper configuration used.

Am97/8605 – iRMX Nucleus Demo Jumper List

	ADD	DESCRIPTION
	E1 – E2	1 wait states – I/O
	E6 – E7	2 wait states – PROMs
	E10 – E11	3 wait states – acknowledge
	E14 – E15	Bus timeout timer enable
8253–5 Timer	E25 – E27	Timer 0 gate input
	E32 – E33	Timer 1 gate input
	E56 – E57	Timer 2 clock input
	E58 – E59	Timer 0 clock input
	E60 – E61	Timer 1 clock input
	E69 – E70	Serial port B RX, TX clk (timer 2)
	E79 – E80	Serial port A RX clock (timer 2)
	E83 – E84	Serial port A TX clock (timer 2)
Serial Port	E87 – E88	Connects CTS to RTS of port A
	E89 – E90	Connects CTS to RTS of port B
	E91 – E92	External DTR port A
Memory	E107 – E108	Enable RAM at 00000H – 1FFFFH
	E115 – E116	Enable PROM at E0000H – FFFFFH
8259 Interrupt Controller	E120 – E121	NON-MASKABLE INTERRUPT
	E123 – E124	Clock 1 out to IR2
	E143 – E131	INT3/ to IR3
	E147 – E130	INT4/ to IR4
	E146 – E145	INT5/ to IR5
	E125 – E128	RXRDY to IR6
	E134 – E127	TXRDY to IR7
	E170 – E171	8086 clock (always installed)
	E177 – E178	Disable battery backup
	E179 – E180	Allows 97/8605 to be BCLK/ source
	E186 – E187	Bus priority out (BPRO/)

*iRMX and ICE are registered trademarks of Intel Cororation.

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Am97/9605 – iRMX Nucleus Demo Jumper List (cont.)

	ADD		DESCRIPTION
	E188 – E189	Bus arbitor, resident bus mode	
	E191 – E192	Allows 97/8605 to be CCLK/ source	
Jumper Block X1	1 – 14	PROM Select	2732 EPROMs
	3 – 12	PROM select	
	6 – 9	PROM select	
Switch 1	1 ON	SBX J4	ON = disabled
	2 ON	SBX J3	OFF = enabled
	3 ON	SBX J5	
	4 OFF	Don't care	
	5 OFF	PROM select	2732 EPROMs
	6 ON	PROM select	
	7 ON	PROM select	
	8 ON	PROM Select	

Note: Intel's iRMX 86 Nucleus Demo, version 3.0 (Part number 143705-001) comes on a single-density diskette as part of the iRMX 86 Software Package.

The Am97/8605 is a complete 16-bit computer system on a single MULTIBUS* board. It includes CPU, static RAM, EPROM sockets, counter/timers, 3 SBX connectors, and both serial and parallel I/O ports. The large EPROM capacity, extensive I/O, and modular expansion capabilities make the Am97/8605 ideally suited for industrial control and intelligent I/O applications. It is designed to work in both standalone and multiple CPU systems.

FEATURES

- 8086 microprocessor with 5,8, or 10MHz operation
- Fully software transparent with Intel iSBC* 86/05 and iSBC 86/12
- Three SBX bus expansion connectors
- On-board socket for 8087 Numeric Data Coprocessor
- Two 16-bit timers/event counters
- Two serial ports with optional Z8OB-SIO/0
- 8K bytes of static RAM. Expandable on-board to 16K with Am97/0343 Memory Expansion Module
- Sockets for up to 64K bytes EPROM. Expandable on-board to 128K with memory module
- 24 programmable parallel I/O lines
- Nine levels of vectored interrupt control
- MULTIBUS multimaster interface
- One year warranty and Rapid Exchange Service (RES)
- Extensive burn-in and testing for enhanced reliability

*MULTIBUS and iSBC are registered trademarks of Intel Corporation.

iSBC 86/05 and Am97/8605 Jumper Comparison

Application Note by Bruce Pettner
Microcomputer Systems Directorate

INTRODUCTION

The following pages are a "pin-for-pin comparison" of Intel's iSBC* 86/05 board and our Am97/8605 8086-Based, 16-Bit Single Board Computers (SBC). The intent is to show their functional similarities and to provide a quick reference list for reconfiguring to user requirements.

The following table starts on the left with a consecutive list of numbers from 1 to 219, which represent jumper pin numbers. The next column to the right is a list of jumpers that appear on Intel's iSBC 86/05 board. When a jumper does not exist on-board, the word "none" is written in its place. The next column to the right contains the pin number on the Am97/8605 SBC with the signal that corresponds to that provided by the Intel board jumper. The last column contains the signal description, as specified by the Intel schematic. All discrepancies are noted in the Legend and Tables following the jumper pin list.

Table 1.0 iSBC 86/05 and Am97/8605 Jumper Comparison

PIN #	Intel iSBC 86/05	AMD Am97/8605	SIGNAL
1	1	1	1 WAIT/
2	2	2	I/O sync ready
3	3	3	2 WAIT/
4	4	4	1 WAIT/
5	5	5	0 WAIT/
6	6	6	PROM sync ready
7	7	7 !	2 WAIT/
8	8	8 !	3 WAIT/
9	9	9	2 WAIT/
10	10	10	
11	11	11	3 WAIT/
12	none	12	OPT1 J5-28
13	13	13	
14	14	14	
15	15	15	
16	none	16	
17	17	17	
18	18	18	
19	19	19	PROM ASYNC
20	20	20	BUSY/ (J6)
21	21	21	READY/ (J6)
22	22	22	STXD
23	23	23	EXT CLK/
24	24	24 !	OVERRIDE/
25	25	33 *	GATE 1 CNTRL
26	26	26	NMI MASK/
27	27	27	+5 VOLTS
28	28	28 .	8287 pin 11 ($T/\overline{R}$)
29	29	29	GROUND
30	30	30	PB INTR
31	31	31	BUS INTR OUT
32	32	32	+5 VOLTS
33	33	25 *	GATE 0 CNTRL
34	34	34	PA INTR
35	35	35	TEST/
36	36	36 !	PFSN/
37	none	37	SBX3 INTR 1 (J5-12)
38	38	38	J1-28
39	39	39	J1-30
40	40	40	J1-32
41	41	41	J1-26
42	42	42	8255A-5 PC-5
43	43	43	8255A-5 PC-6

*iSBC and iSBX are registered trademarks of Intel Corporation.

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Table 1.0 (cont.)

PIN #	Intel iSBC 86/05	AMD Am97/8605	SIGNAL
44	44	44	8255A-5 PC-7
45	45	45	8255A-5 PC-4
46	46	46	J1-24
47	47	47	J1-22
48	48	48	J1-20
49	49	49	J1-18
50	50	50	8255A-5 PC-0
51	51	51	8255A-5 PC-1
52	52	52 !	8255A-5 PC-2
53	53	53	8255A-5 PC-3
54	54	–	8255A-5 PC-3 (light)
	–	54 +	OVERRIDE/ second serial port
55	55	–	light
	–	55 +	Z80-SIO/0 RXTXCB second serial port
56	56	56 !	8253-5 CLK 2
57	57	57	
58	58	58	
59	59	59	8253-5 CLK 0
60	60	60	
61	61	61	8253-5 CLK 1
62	62	62	EXT CLK/
63	63	63	8253-5 OUT 0 (TIMER 0 INTR)
64	64	64	8251A CLK
65	65	65	8253-5 OUT 1 (TIMER 1 INTR)
66	66	66	PLC
67	67	67	8253-5 OUT 2
68	68	–	+5 VOLTS (P1-83,84)
	–	68 +	2XCB J2B-8
69	69	–	J2-23
	–	69 +	
70	70	–	J2-19
	–	70 +	Z80-SIO/0 RXTXCB
71	71	–	–12 VOLTS (P1-79,80)
	–	71 +	
72	72	72	8251 TXC
73	73	73	STXD
74	74	74	
75	75	75	J2-26
76	76	76	
77	77	77	J2-5
78	78	78	J2-21
79	79	79	8251A RXC
80	80	80	8253-5 OUT 2
81	81	81	SEC. TRANSMIT CLOCK J2-7
82	82	82	SEC. TRANSMIT CLOCK J2-7
83	83	83	8251A TXC
84	84	84	8253-5 OUT 2
85	85	–	J2-22
	–	85 +	
86	86	–	+12 VOLTS (P1-7,8)
	–	86 +	
87	87	87	CLEAR TO SEND J2-10
88	88	88	REQUEST TO SEND J2-8
89	89	89 !	
90	90	90 !	
91	91	91	8251A DSR
92	92	92	DATA TERMINAL READY J2-13
93	none	none	
94	none	none	
95	none	none	
96	none	none	
97	none	none	
98	none	none	

Table 1.0 (cont.)

PIN #	Intel iSBC 86/05	AMD Am97/8605	SIGNAL
99	none	none	
100	none	none	
101	none	none	
102	none	none	
103	none	none	
104	104	SWITCH1	select SBX 302 RAM expansion
105	105	SWITCH1	Ground
106	106	SWITCH1	select SBX 341 PROM expansion
107	107	107	Page select RAM
108	108	108	RAM @ 00000 – 1FFFF
109	109	109	RAM @ 40000 – 5FFFF
110	110	110	PROM @ 20000 – 3FFFF
111	111	111	RAM @ 80000 – 9FFFF
112	112	112	PROM @ 60000 – 7FFFF
113	113	113	RAM @ C0000 – DFFFF
114	114	114	PROM @ A0000 – BFFFF
115	115	115	Page select PROM
116	116	116	PROM @ E0000 – FFFFF
117	117	117	SBX2 INTR 0
118	118	118	PFI/
119	119	119	EXT INTR0/ (J1-50)
120	120	120	NMI MASK/
121	121	121	GROUND
122	122	122	TIMER 1 INTR
123	123	123	TIMER 2 INTR
124	124	124	8259A IR2
125	125	125	SIRX INTR
126	126	126	SBX2 INTR 1
127	127	127	8259A IR7
128	128	128	8259A IR6
129	129	129	EDGE INTR
130	130	130	8259A IR4
131	131	131	8259A IR3
132	132	132	8259A IR0
133	133	133	8259A IR1
134	134	134	SITX INTR
135	none	none	
136	136	136	
137	137	137	SBX1 INTR 0
138	138	138	SBX1 INTR 1
139	139	24 *!	MINT
140	140	140	PB INTR
141	141	141	PA INTR
142	142	142	
143	143	143	
144	144	144	
145	145	145	8259A IR5
146	146	146	
147	147	147	
148	148	148	
149	149	149	
150	150	150	PLC
151	none	none	
152	152	152	8288 AMWTC/ (J6-2)
153	153	153	U33 (U73) & U66 (U74) PGM
154	none	none	
155	none	none	
156	none	none	
157	none	none	
158	none	none	
159	none	none	
160	none	none	
161	none	none	

Table 1.0 (cont.)

PIN #	Intel iSBC 86/05	AMD Am97/8605	SIGNAL
162	none	none	
163	none	none	
164	none	none	
165	none	none	
166	166	166	OPT 0 (J3-30)
167	167	167	OPT 1 (J3-28)
168	168	168	ON BD ADR/
169	169	169	
170	170	170	8284A CLK
171	171	171	8086 CLK
172	172	172	OPT 0 (J4-30)
173	173	173	OPT 1 (J4-28)
174	none	none	
175	none	none	
176	none	none	
177	177	177	
178	178	178	
179	179	179	BCLK/ (P1-13)
180	180	180	
181	181	none	} Installed = 8 MHz
182	182	none	} Removed = 5 MHz
183	183	183	CBR0/ (P1-29)
184	184	184	8289 CBRQ
185	185	185	GROUND
186	186	186	8289 BPR0
187	187	187	BPR0/ (P1-16)
188	188	188	8289 CRQCK, RESB, IOB, +5V
189	189	189	8289 ANYREST
190	190	190	GROUND
191	191	191	
192	192	192	CCLK/ (P1-31)
193	193	193	Bus interrupt output
194	194	none	INT4/ P1-37
195	195	none	INT2/ P1-39
196	196	none	INT5/ P1-38
197	197	none	INT3/ P1-40
198	198	none	INT7/ P1-36
199	199	none	INT0/ P1-41
200	200	none	INT6/ P1-35
201	201	none	INT1/ P1-42
202	none	none	
203	none	none	
204	none	none	
205	none	none	
206	206	none	Jumper in for 16-bit mode J4
207	207	none	Jumper in for 16-bit mode J4
208	208	none	Jumper in for 16-bit mode J3
209	209	none	Jumper in for 16-bit mode J3
210	210	SWITCH1	PROM select } See Table 2.1
211	211	SWITCH1	PROM select } See Table 2.1
212	212	SWITCH1	PROM select } See Table 2.1
213	213	SWITCH1	PROM select } See Table 2.1
214	214	214	
215	215	215	LOCK/ (P1-25)
216	none	216	
217	none	217	4.72MHZ CLOCK
218	none	218	Z80B-SIO/0 CLK J2B
219	none	219	8251 CLK J2A

LEGEND:
! = Jumper number duplicated on this board (see Table 1.1)
* = Indicates "pin number different" for this signal
+ = Indicates "jumper exists, but has different signal"
none = Indicates "jumper number does not exist on this board" (see Table 4.0)
SWITCH1 = Indicates "jumper function performed by switch" (see Table 2.0)

Table 1.1 Am97/8605 Duplicate Pins

PIN #	AMD Am97/8605	SIGNAL
7	7	DTRB on J2B-24
8	8	To DSR pin on MK3884
24	24	See Intel jumper 139
36	36	J5-14 SBX INT0
52	52	RTS To J2B-9 (CTSB)
56	56	
89	89	To J2B-22
90	90	To J2B-25

Table 2.0 SWITCH1 Jumper Function

SWITCH1-1 SBX J4 select
-2 SBX J3 select
-3 SBX J5 select
-4 not used
-5 PROM select
-6 PROM select
-7 PROM expansion select
-8 RAM expansion select

Table 2.1 PROM Selection

PROM	Intel iSBC 86/05	AMD Am97/8605
2716	no jumper	SW1-5,6 on
2732	210-211	SW1-5 off
2764	212-213	SW1-6 off
27128	210-211 212-213	SW1-5,6 off

Note: Switch 1 uses off active logic.

Table 3.0 PROM/IC Sockets Cross Reference

Intel iSBC 86/05	AMD Am97/8605	FUNCTION
U8	U11	Parallel Port C (4-7)
U9	U12	Parallel Port C (0-3)
U10	U13	Parallel Port B (0-3)
U11	U14	Parallel Port B (4-7)
U33	U72	Bank 0 High (odd) bytes (0H)
U34	U73	Bank 1 High (odd) bytes (1H)
U66	U74	Bank 0 Low (even) bytes (0L)
U67	U75	Bank 1 Low (even) bytes (1L)
U35	X1	Jumper block

Table 4.0 Unused Jumper Pin Numbers

Intel iSBC 86/05	AMD Am97/8605
12	93 thru 106
16	135
37	151
93 thru 103	154 thru 165
135	174 thru 176
151	181
154 thru 165	182
174 thru 176	193 thru 213
202 thru 205	
216 thru 219	

Am97/0343

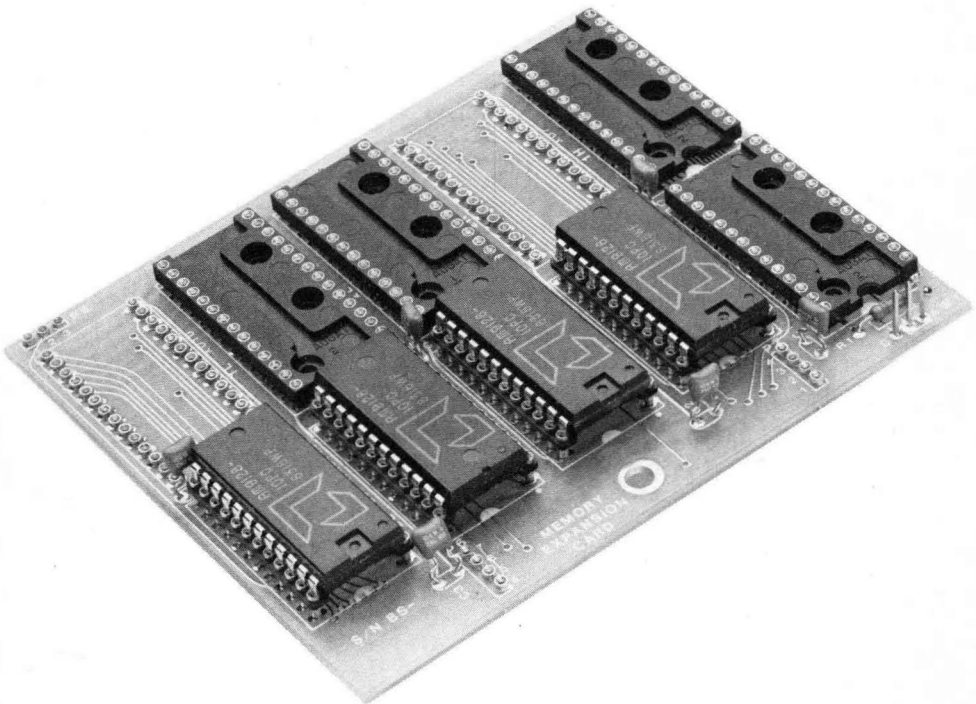
Memory Expansion Module for the Am97/8605
Single Board Computer

DISTINCTIVE CHARACTERISTICS

- Doubles Am97/8605 on-board memory capacity
- 8K bytes of 150ns static RAM
- Four additional 28-pin JEDEC sockets accommodate up to 64K bytes of EPROM/ROM
- Same access times as memory provided on the Am97/8605

GENERAL DESCRIPTION

The Am97/0343 Memory Expansion Module doubles the memory capacity of the Am97/8605 Single Board Computer (SBC) by providing an additional 8K bytes of static RAM and four 28-pin JEDEC EPROM sockets. It is designed to plug directly on-board the Am97/8605 SBC and has the same access time as the memory provided on the host board.



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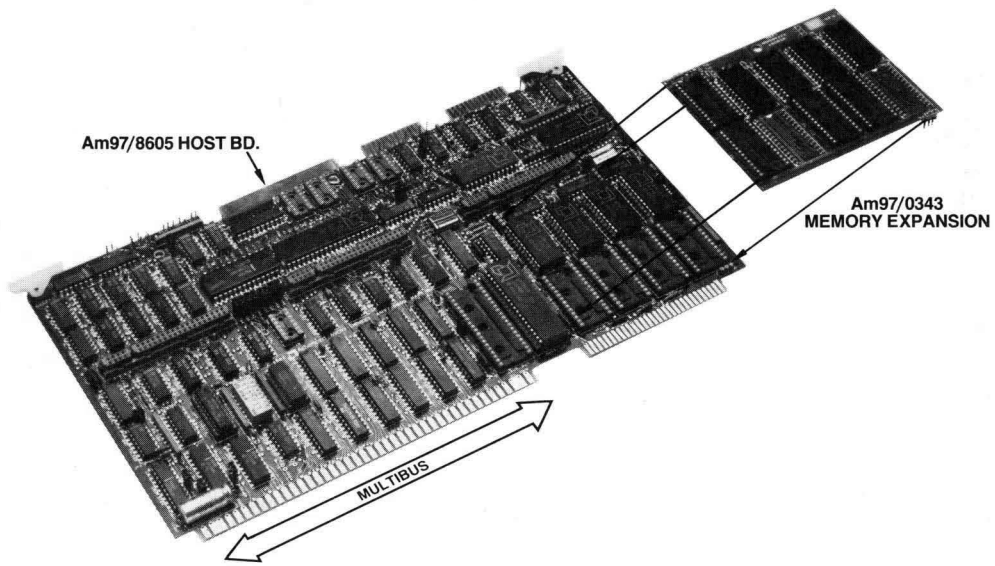
FUNCTIONAL DESCRIPTION

The Am97/0343 Memory Expansion Module doubles the on-board memory capacity of the Am97/8605 SBC. The module mounts directly over the memory section on the host board and is installed by plugging the module into two of the EPROM sockets on the Am97/8605 and connecting three additional plugs (see Figure 1). Switches on the Am97/8605 are set to enable access to the static RAM and EPROM portions of the Am97/0343.

Four 16K static RAMs on the Am97/0343 provide 8K bytes of incremental memory. In addition, there are six 28-pin JEDEC sockets. Two of the sockets are used to replace those on the Am97/8605 which are required for mounting the expansion module, and four are used for expanding the EPROM capacity an additional 64K bytes. EPROMs used on the Am97/0343 must be the same size as those on the Am97/8605; ranging from 16K devices, such as the 2716-1, up to 128K devices, such as the 27128. The type of EPROM is determined by the jumpering on the Am97/8605.

The signals required to access the Am97/0343 memory are carried through the connectors attaching the expansion module to the Am97/8605. Since the signals do not have to pass through the MULTIBUS* interface or any additional logic, access time is the same for the Am97/0343 as it is on the Am97/8605.

Figure 1. Am97/0343 Memory Expansion and Am97/8605 Installation



*MULTIBUS is a registered trademark of Intel Corp.

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SPECIFICATIONS

Board Capacity

Am97/0343: 8K bytes of static RAM provided Sockets for up to 64K bytes of PROM/EPROM

Memory Cycle Times

RAM:	150ns (no-wait states)
EPROM:	350ns using 2716
	200ns using 2732A
	200ns using 2764
	200ns using 27128

Physical Characteristics

Width:	4.30 in.	(10.92 cm.)
Height:	3.48 in.	(8.84 cm.)
Thickness:	0.18 in.	(.46 cm.) – Module only
	1.08 in.	(2.74 cm.) – Module and Host Board
Weight:	2.4 oz.	(70 gr.)
Shipping Weight:	1 lb.	(454 gr.)

Environmental Characteristics

Operating Temperature:	0°C to 55°C (32°C to 130°F) with free moving air across the base board and the module
Relative Humidity:	Up to 90% without condensation
Storage Temperature:	–40°C to 75°C

Electrical Characteristics

DC Power Requirements

RAM:		+5 Volts at 230mA max
EPROM:	2716:	+5 Volts at 300mA max
	2732A:	+5 Volts at 390mA max
	2764:	+5 Volts at 360mA max
	27128:	+5 Volts at 480mA max

Reference Manual

059920059-001 – Am97/0343 Memory Expansion Module

ORDERING INFORMATION

Part Number	Description
Am97/0343	Memory Expansion Module for Am97/8605 Series
Companion Products	
Am97/8605 Series	8086-Based, 16-Bit Single Board Computers

Am97/8605A

8086-Based 16-Bit Single Board Computer
ADVANCED INFORMATION

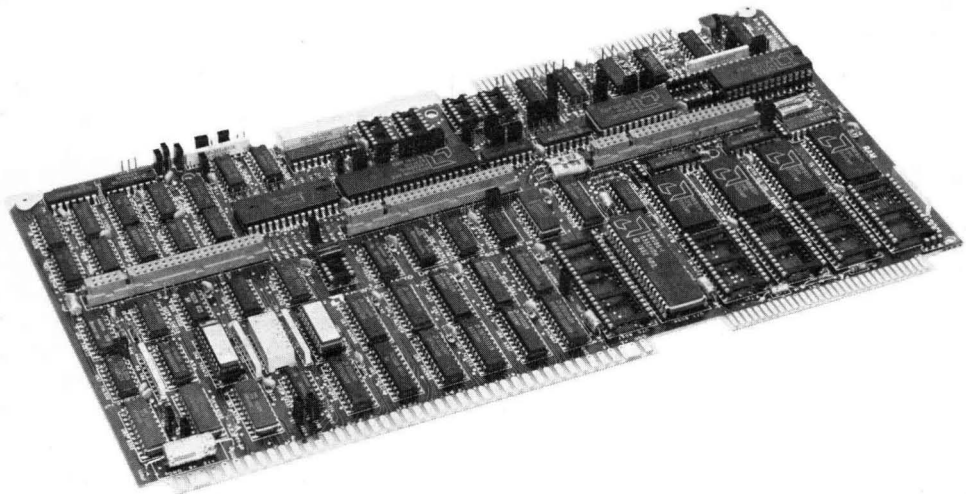
DISTINCTIVE CHARACTERISTICS

- 8086 microprocessor with 5,8, or 10MHz operation
- Fully software transparent with Intel iSBC* 86/05 and iSBC 86/12
- On-board socket for 8087 Numeric Data Coprocessor
- Flexible memory section
  - 8K bytes of static RAM supplied; optional on-board expansion to 32K bytes
  - Sockets can support up to 512K bytes of EPROM
- Flexible I/O
  - Three SBX expansion connectors
  - One serial port supplied, second serial port supported
  - 24 programmable parallel I/O lines
- Two 16-bit timers/event counters
- Nine levels of vectored interrupt control

GENERAL DESCRIPTION

The Am97/8605A is an enhanced version of the Am97/8605 16-bit Single Board Computer (SBC) based on the 8086 microprocessor. It includes a very flexible memory section making memory expansion modules unnecessary.

The large EPROM capacity of up to 512K bytes along with extensive I/O capabilities make the Am97/8605A ideally suited for controller applications. It is designed to work in both standalone and multiple CPU systems.



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PRODUCT OVERVIEW

The Am97/8605A is a powerful 16-bit Single Board Computer based on the 8086 microprocessor and 8087 coprocessor. The Am97/8605A SBC is a complete computer system on a single board. It includes CPU, static RAM, EPROM sockets, counter/timers, 3 SBX connectors, and both serial and parallel I/O ports. In addition, it has full MULTIBUS* multimaster capability, interrupt logic, and is fully software compatible with the Intel iSBC 86/05 and iSBC 86/12 boards.

The large EPROM capacity, extensive I/O, and modular expansion capabilities make the Am97/8605A ideally suited for ROM-intensive control and I/O applications. It is designed to work as both a standalone CPU and as a slave CPU in a multimaster system.

The Am97/8605A is a very versatile CPU board. Custom I/O and special functions can be added with the addition of up to three SBX modules. An additional serial port can be obtained by using the Z80B SIO/0 (MK3884) Serial I/O chip. The on-board memory section is configurable for up to 32K bytes of RAM or 512K bytes of EPROM or a combination of static RAM and EPROM.

There are three versions of the board. One version runs at 5 or 8MHz jumper-selectable; one runs at 5MHz with an on-board 8087 coprocessor; and the third runs at 5 or 10MHz jumper-selectable.

Central Processing Unit

The Am97/8605A SBC contains the high-performance, 16-bit 8086 microprocessor. The pipelined architecture of the 8086 incorporates both a bus interface unit and an execution unit. This enables the microprocessor to execute one instruction while at the same time fetching the next, thus greatly improving throughput.

The advanced architecture of the 8086 supports high-level languages and complex application programs. The microprocessor contains four 16-bit data registers, two 16-bit index registers, and two 16-bit base pointer registers. It can directly access up to one megabyte of memory. The 8086 has 24 operand addressing modes for comprehensive memory addressing and for support of various data structures. The instruction set includes variable length instruction format, 8 and 16-bit signed and unsigned arithmetic operators for binary, BCD and ASCII data, and iterative word and byte string manipulation functions.

BASIC Am97/8605A COMPONENTS

CPU	8086
Coprocessor	8087
Static RAM	9128
Counter/Timers	8253-5
Serial I/O	8251A
Parallel I/O	8255A-5
Interrupt Controller	8259A

Programmable Timers

To handle timing, sequencing, and counting functions, the Am97/8605A SBC utilizes an 8253-5 Programmable Interval Timer (PIT). The 8253-5 has three independent, 16-bit interval timer/event counters. Each counter is capable of operating in either BCD or binary mode. Two counters are available to the systems designer, while the third is dedicated for generating the baud rate for the serial port.

Interrupt Capability

Nine interrupt levels are supported on the Am97/8605A SBC. The non-maskable interrupt line is routed directly to the 8086, while an 8259A Programmable Interrupt Controller (PIC) handles eight vectored interrupt levels. The 8259A PIC efficiently oversees and controls the interface between I/O devices and the CPU. The 8259A features four priority processing modes including auto rotating, fully nested, polled and specific priority. In addition, the interrupt mask register can be programmed to mask a variety of interrupt levels. The number of interrupt levels is expandable to 64 by the addition of slave 8259As on the MULTIBUS.

Multimaster Capability

Full MULTIBUS arbitration is provided on the Am97/8605A SBC through the use of an 8289 Bus Arbiter. The control logic allows up to three masters using serial priority resolution. This capability makes the Am97/8605A particularly suited for development and OEM applications requiring multiple master processors.

SBX Expansion

The Am97/8605A contains three 8/16-bit SBX-type connectors for plug-in I/O expansion. These SBX connectors meet the Intel iSBX* specifications and can be used to add on-board I/O functions. By mounting modules directly on the Am97/8605A SBC, less interface logic, less power consumption, higher performance, and lower costs result when compared to alternative methods.

Numeric Data Coprocessor

The 8087 is a numeric coprocessor that can provide up to 100 times the performance of an 8086 alone for numeric processing. It performs arithmetic, transcendental, and comparison operations on a variety of numeric data types. It supports 32 and 64-bit floating point and 16, 32, and 64-bit integer numbers.

The 8087 works in parallel with the 8086. Both processors share the same data and address lines and communicate with each other through status lines. When the 8087 recognizes an instruction that it must execute, it gains control of the local bus. In this manner both the 8086 and 8087 can execute their own particular instructions.

The 8087 coprocessor is ideally suited for numerical-based application programs. A socket is provided on-board so that you may add the 8087 when ordering the board, or at a later date.

On-Board Memory

The Am97/8605A has a very flexible memory section which replaces the need for memory expansion modules required by other 8086-based boards. It consists of eight 28-pin JEDEC sockets capable of supporting from 16K EPROMs (2716s) to 512K EPROMs (27512s) for a maximum of 512K bytes. Four of the sockets can be used instead for static RAMS to provide 32K bytes using 64K devices. In addition, two more static RAMs could occupy PROM space if needed.

The standard configuration for shipping is with four 16K static RAMs for 8K bytes of memory and the ability to use up to six EPROMs in sizes ranging from 2764s to 27512s. The ability to use smaller EPROMs or all eight sockets for EPROMs are optional configurations.

Serial I/O

The Am97/8605A will accommodate either an 8251A Programmable Communications Interface (PCI) or Z80B-SIO/

*iSBX is a registered trademark of Intel Corporation.

0 (MK3884) device. The 8251A comes with the board and provides a single RS-232C serial port. The 8251A can be replaced by a Z80B SIO/0, which will provide two serial ports. Both devices feature software-selectable baud rates, synchronous and asynchronous operation, parity, data format and control character format. The serial lines are routed to two 26-pin edge connectors on top of the Am97/8605A board.

Parallel I/O

An 8255A-5 Programmable Peripheral Interface (PPI) device supplies 24 lines of parallel input/output capability to the Am97/8605A. These lines can be programmed and hardware-configured as three sets of 8-bit ports with either status-driven, polled, or interrupt-driven protocol. One of the ports is supplied with a bidirectional bus transceiver, while sockets are provided for drivers or terminators for the other two ports. A 50-pin edge connector is provided on top of the board to access the ports.

Am97/0000 Series

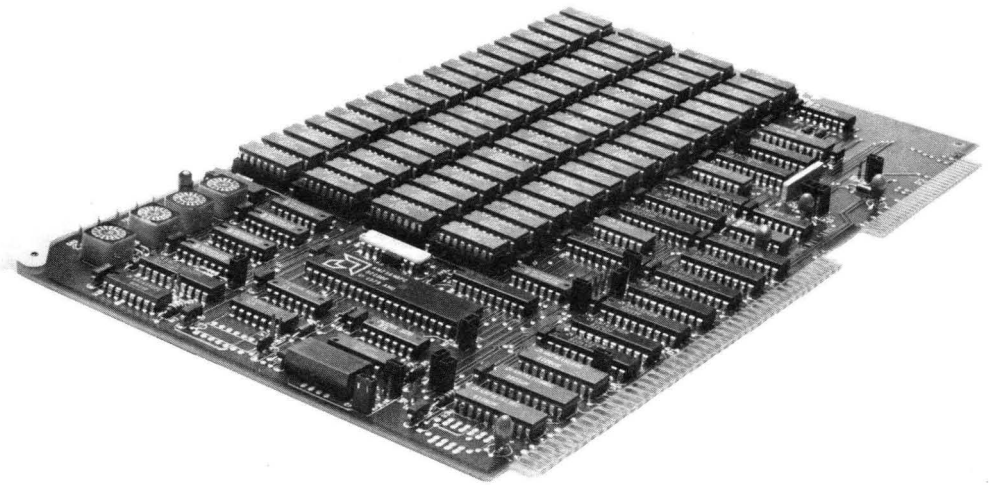
Random-Access Memory Boards

DISTINCTIVE CHARACTERISTICS

- Plug compatible with Intel's iSBC* 032A, 064A, 028A, 056A, and 012B RAM boards
- Compatible with 8 or 16-bit processors
- Supports 16/20/24-bit addressing
- On-board refresh circuitry with jumper for optional external refresh control
- Board memory starts on any 4K byte boundary within the 16 Megabyte addressing range
- User-selectable and adjustable advanced acknowledge
- Incorporates the Am2964B Dynamic Memory Controller
- Undergoes extensive burn-in and testing for enhanced reliability

GENERAL DESCRIPTION

The Am97/0000 Series is a family of five high performance, MULTIBUS*-compatible, Random-Access Memory (RAM) boards. They feature fast access and cycle times, low-power consumption, parity-type error detection with latching error registers, and power back-up capability.



*iSBC and MULTIBUS are registered trademarks of Intel Corporation.

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PRODUCT OVERVIEW

The Am97/0000 Series is a family of five high performance, MULTIBUS compatible, Random-Access Memory (RAM) boards. Their fast access and cycle times, low-power consumption, and enhanced reliability, make the Am97/0000 memory boards ideal for today's fast 8 and 16-bit computer systems. (See Figure 1.)

The latest in memory technology is incorporated in the Am97/0000 Series to provide a reliable, fast memory board with low power consumption. An Am2964B Dynamic Memory Controller and four PALs* are utilized to handle all logic functions. In addition, a four layer printed circuit board design is used to increase noise immunity. Three hexadecimal encoder switches are used to simplify the setting of memory starting addresses. The advanced design and extensive burn-in and testing that each board goes through makes the Am97/0000 Series of memory boards the right choice for your system.

FUNCTIONAL DESCRIPTION

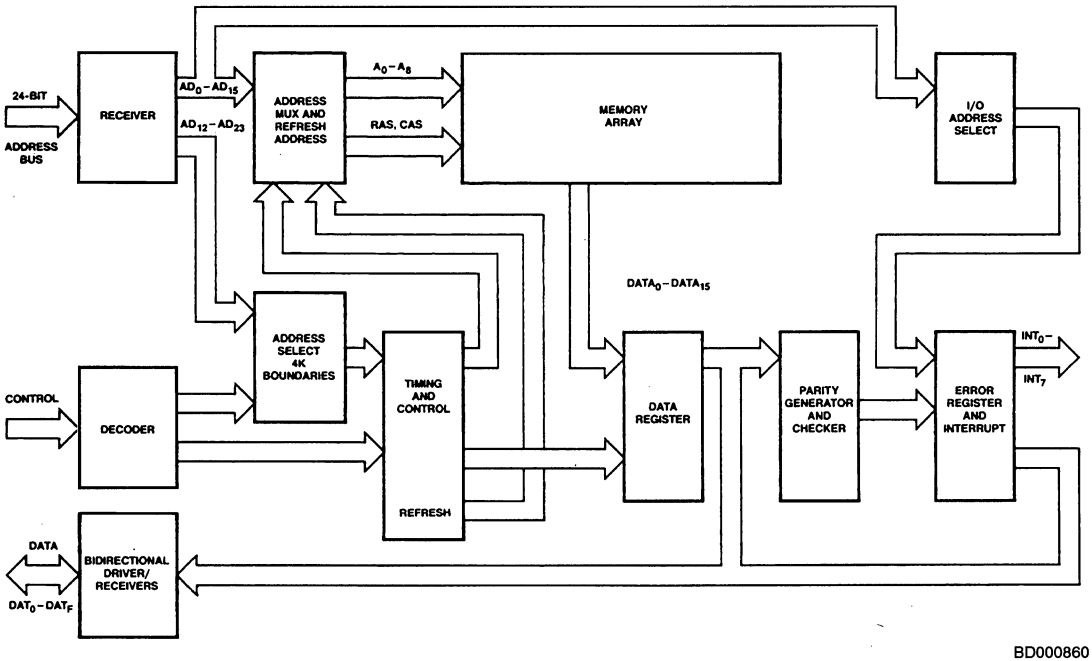
The Am97/0000 Series boards are single board MULTIBUS memory systems that include a memory array, refresh logic, parity generator and checker, two latching error registers, data register, address decoding and selection hardware, LED error indicator, and the MULTIBUS interface logic. (See Figure 2.)

The memory board can be configured to use one or two parity error registers with selectable interrupt levels, internal or external refresh, internal or external parity generation, and advanced acknowledge with selectable advance times. If advanced delayed write is needed, a socket is provided to insert a delay line.

Figure 1. Am97/0000 Series Memory Board Lineup

AMD Part No.	Memory Size	RAM Device	Access Time	Cycle Time	Power Required
Am97/0032	32K bytes	16K x 1	200ns	350ns	12W
Am97/0064	64K bytes	16K x 1	200ns	350ns	12W
Am97/0128	128K bytes	64K x 1	200ns	350ns	10W
Am97/0256	256K bytes	64K x 1	200ns	350ns	11W
Am97/0512	512K bytes	64K x 1	200ns	350ns	11W

Figure 2. Am97/0000 Series RAM Memory Board Block Diagram



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Plug-Compatible with Intel Memory Boards

The Am97/0000 Series boards are plug-compatible with Intel's iSBC 032A, 064A, 028A, 056A, and 012B RAM boards. Both one-for-one and one-for-two swaps can be made. For example, an Am97/0256 can plug into a slot designed for an iSBC 056A, or an Am97/0512 can replace two iSBC 056A boards as shown in Figure 3. Since the AMD boards have two parity error registers on each board, they can be software transparent to either one or two Intel boards.

Addressing Memory

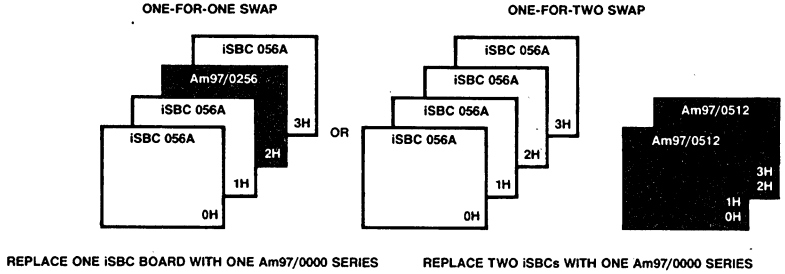
Three hexadecimal encoder switches determine the memory starting address. They allow the user to set the starting address directly in Hex with a 4K byte resolution. The memory starting address can be set anywhere within the 16 Megabyte address space without any boundary restrictions.

To select the board's starting address, the user sets three 16-position rotary switches. Appending three zeros to the 3-digit Hex equivalent of the switch settings equals the starting address. Figure 4 shows how to set these switches.

Parity Error Detection

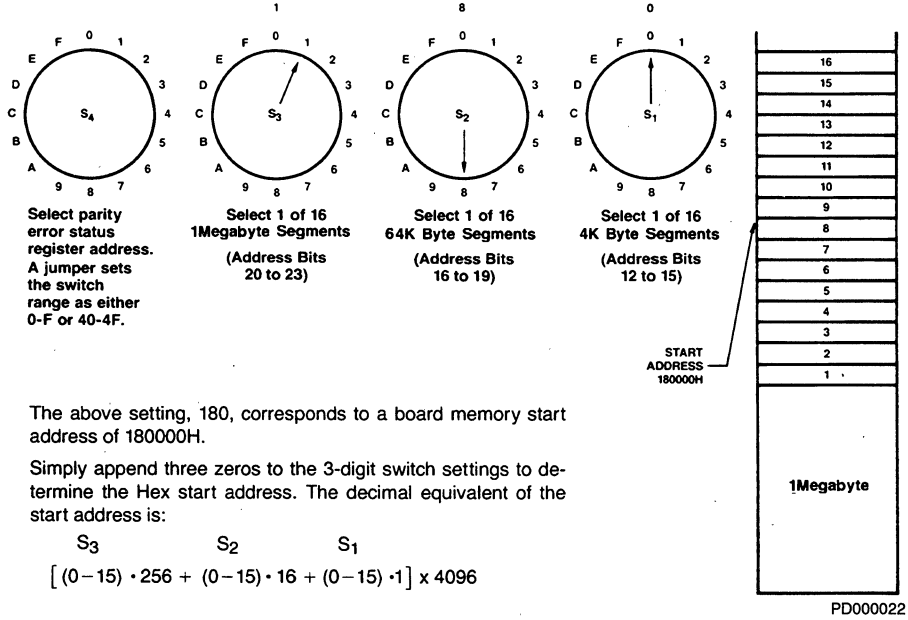
Parity logic is used on the Am97/0000 Series boards to detect single bit errors. With each memory write, the parity is calculated and stored, and with every memory read, the parity is calculated and checked. On a parity error, one of two error registers latches the row and bank location of the RAMs with the parity error, an interrupt is generated over the MULTIBUS, and the on-board LED is turned on. Each error register can generate its own interrupt on any of the MULTIBUS interrupt lines, or the interrupts can be disabled.

Figure 3. Plug Compatibility with Intel's iSBC Boards



PD000010

Figure 4. Rotary Switch Selection of Board Memory Start Address



The above setting, 180, corresponds to a board memory start address of 180000H.

Simply append three zeros to the 3-digit switch settings to determine the Hex start address. The decimal equivalent of the start address is:

$$S_3 \qquad S_2 \qquad S_1$$
$$[(0-15) \cdot 256 + (0-15) \cdot 16 + (0-15) \cdot 1] \times 4096$$

PD000022

SPECIFICATIONS

Word Size

8 or 16 bits

Memory Size

Am97/0032:	32,768 bytes
Am97/0064:	65,536 bytes
Am97/0128:	131,072 bytes
Am97/0256:	262,144 bytes
Am97/0512:	524,288 bytes

MULTIBUS Interface

Compatible with IEEE P796

Physical Characteristics

Width:	30.48 in. (12.00 cm.)
Height:	17.15 in. (6.75 cm.)
Thickness:	1.27 in. (.50 cm.)

Environmental Characteristics

Operating Temperature

0°C to 55°C (32 to 130°F)

Operating Humidity

To 90% without condensation

Parity

Interrupt on selectable level with status register on selectable I/O port address

Reference Manual

059920016-001 – Am97/0000 series RAM Memory Boards

Product	T_{ACC} max	R/W T_{Cycle} max	Refresh T_{Cycle} max
Am97/0032	200ns	350ns	400ns
Am97/0064	200ns	350ns	400ns
Am97/0128	200ns	350ns	400ns
Am97/0256	200ns	350ns	400ns
Am97/0512	200ns	350ns	400ns

Power Requirements

	P_1 Supplies			Auxiliary Connector P_2 Backup Supplies*		
Product	+5V	+12V	−12 or−5V	+5V	+12V	−12V or−5V
Am97/0032	1.7A	.2A	.05A	.6A	.075A	.05A
Am97/0064	1.7A	.2A	.05A	.6A	.075A	.05A
Am97/0128	2.0A			.8A		
Am97/0256	2.1A			.8A		
Am97/0512	2.2A			.8A		

*Optional

ORDERING INFORMATION

Part Number	Description
97/0032	32K Byte Dynamic RAM Board with Parity (16K RAMs)
97/0064	64K Byte Dynamic RAM Board with Parity (16K RAMs)
97/0128	128K Byte Dynamic RAM Board with Parity (64K RAMs)
97/0256	256K Byte Dynamic RAM Board with Parity (64K RAMs)
97/0512	512K Byte Dynamic RAM Board with Parity (64K RAMs)

Am97/0000B Series

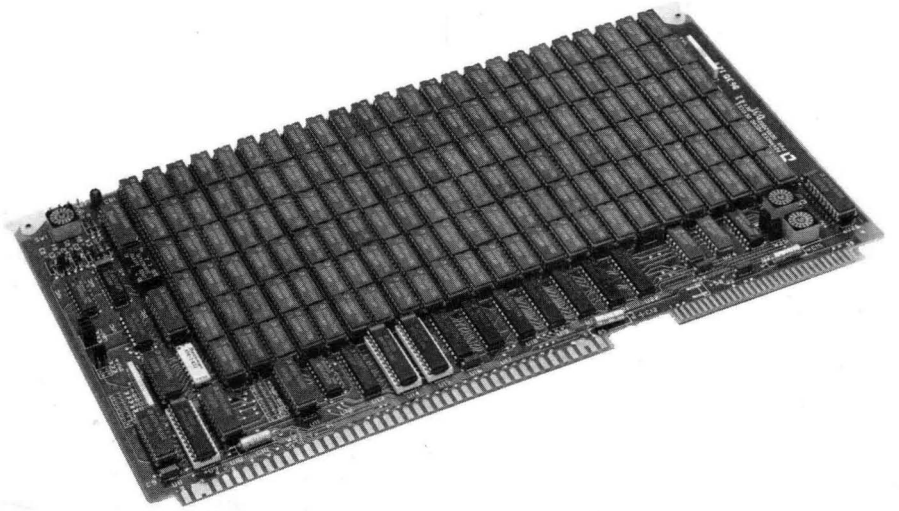
1 Megabyte RAM Boards
768K Bytes, 512K Bytes RAM Boards

DISTINCTIVE CHARACTERISTICS

- Meets IEEE P796 specifications for MULTIBUS* compatibility
- Supports up to 24-bit addressing for a maximum address range of 16 megabytes
- Board memory starts on any 64K byte boundary, selectable by rotary Hex switches. On-board memory can be set to cross any megabyte boundary or optionally stop on a megabyte boundary
- Optional lock-out feature for flexibility:
  - Lower 32K and/or upper 64K addresses of first megabyte can be disabled on-board
- 8 or 16-bit word size with byte swapping capability
- High speed:
  - 200ns max. access time
  - 300ns max. cycle time
- Parity with latching error register and interrupt generation
- On-board refresh circuitry
  - 350ns max. refresh cycle every 14μs
- Power back-up facilities
- Extensive use of PALs** provides high density and enhances reliability

GENERAL DESCRIPTION

The Am97/0000B Series is a family of high density, MULTIBUS compatible, Random-Access Memory (RAM) boards. They make use of the latest in LSI technology to provide 512K, 768K, or 1024K bytes of dynamic RAM memory on a single MULTIBUS board. Extensive testing and 100% dynamic burn-in ensure high quality and performance.



*MULTIBUS is a registered trademark of Intel Corporation.
**PAL is a registered trademark of and used under license from Monolithic Memories, Inc.

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PRODUCT OVERVIEW

The Am97/0000B Series of dynamic Random-Access Memory boards is the perfect choice for system designers needing large memory space in their MULTIBUS systems. These boards make use of the latest in memory technology to provide up to one megabyte of high-speed, low-power memory on a MULTIBUS board using 64K dynamic RAMs. The boards come populated in the following sizes: 512K, 768K and 1024K bytes.

The addressing capabilities of the Am97/0000B boards provide great flexibility. These boards support up to 24-bit addresses for a range of 16 megabytes. They have 64K byte starting address resolution with the ability to cross any boundary. In addition, the lower 32K and upper 64K addresses of the first megabyte of memory can be locked-out.

Parity error detection logic is provided on board with interrupt generation capability and a latching register to store the physical row and byte of the occurrence. Other features include an auxiliary connector for back-up power with memory protect control line and automatic refresh.

The advanced design, incorporating several PALs and sockets with integral capacitors to minimize chip count and maximize space utilization, increases performance and ensures high quality. AMD puts the boards through 100% dynamic burn-in and extensive testing to further ensure a highly reliable product.

FUNCTIONAL DESCRIPTION

The Am97/0000B boards are single board, MULTIBUS memory systems that include a memory array, refresh logic, parity generator and checker, latching error register, address decoding and selection hardware, LED error indicator and the MULTIBUS interface logic (see Figure 1).

Configurations include various addressing options, memory timing schemes, parity error interrupts and battery back-up.

Addressing Scheme

These memory boards support up to 24-bit addressing to provide an addressing range of 16 Megabytes. One jumper enables the memory to stop on any arbitrary megabyte boundary. Other jumpers enable the memory to cross megabyte boundaries to allow full use of the memory's capacity.

The board can start on any 64K boundary within the 16 Megabytes address space available. Two rotary hexadecimal switches establish the exact starting address with one switch defining the megabyte boundary and the other, the 64K boundary (see Figure 2). If only 20 address bits are used, switch 3 is set to 0.

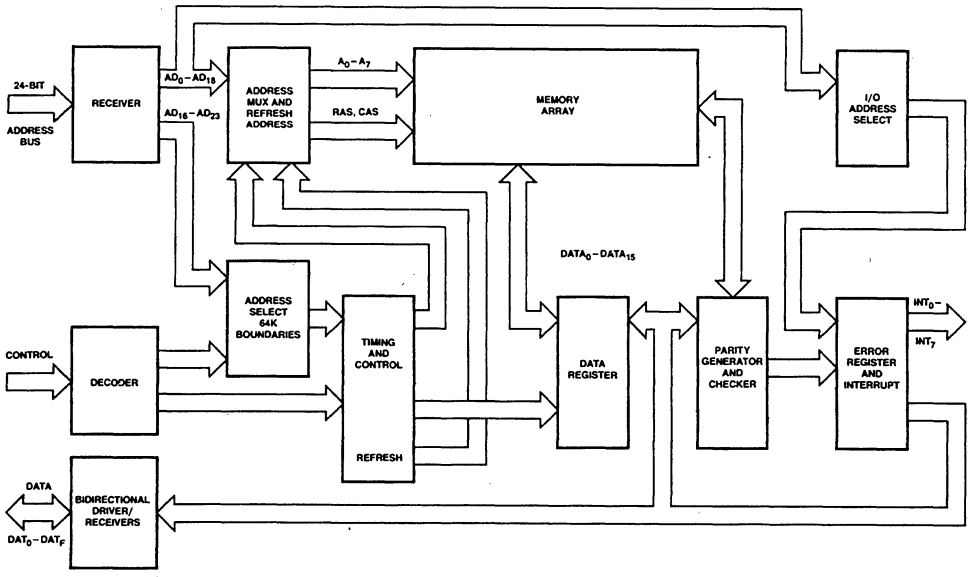
The boards have the ability to lock-out portions of memory in the first megabyte (starting address 0H). The low order 32K bytes and the upper 64K bytes can be disabled by jumpers. The low order 32K byte lock-out is useful in many systems with memory on the host CPU board by enhancing the starting address resolution of the memory board to be 32K (i.e., the board would respond to addresses between 32K and 1 Megabyte). Lock-out of the upper 64K bytes can be useful in systems, for example, that make use of those locations for I/O addresses.

Parity Error Detection

Parity logic is used on the Am97/0000B Series to detect the occurrence of single bit errors. Parity is calculated and stored with each memory write and is calculated and checked with each memory read. On an error condition, the error register stores the physical row and byte locations of the error and the LED turns on. If a parity interrupt was enabled, then the error causes the generation of that interrupt over the MULTIBUS. The register can then be polled at its I/O address to find out the location of the parity error and take corrective action.

The error register I/O address can be chosen as one of 32 possible locations and is set by jumpers and a Hex switch. One jumper selects between an 8-bit and 16-bit I/O address scheme, another jumper selects the low order 8 bits as 00-

Figure 1. Am97/0000B Series RAM Memory Board



0FH or 40-4FH; and the switch chooses the exact location within the low order 4 bits (see Figure 2).

Timing Consideration

Access times of 200ns maximum and cycle times of 300ns maximum mean high-performance dynamic RAM memory for a MULTIBUS system. To optimize system performance, user-adjustable Acknowledge signals are provided. Traditionally, AACK/ was used to improve system timing. However, the pin used to transmit the AACK/ signal is defined by IEEE P796 to be the LOCK/ signal. Therefore, Am97/0000B boards provide an adjustable Transmit Acknowledge signal (XACK/) which can be user-adjustable with respect to memory read (MRDC/) at 50, 105, and 200ns ± 15ns after the signal. XACK/ is transmitted 50ns ± 15ns after the memory write signal. If AACK/ is needed, it can be optionally asserted via a jumper and would be equivalent to XACK/.

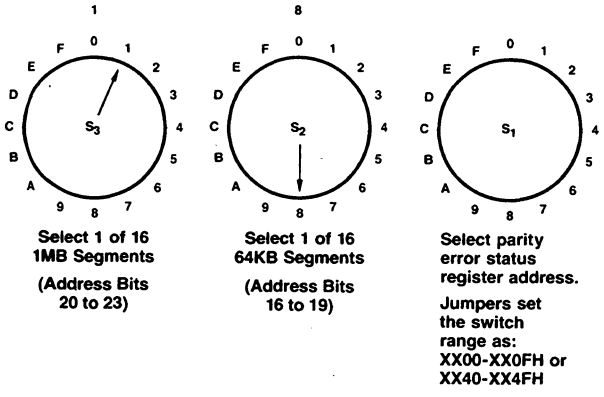
Auxiliary Power Back-Up

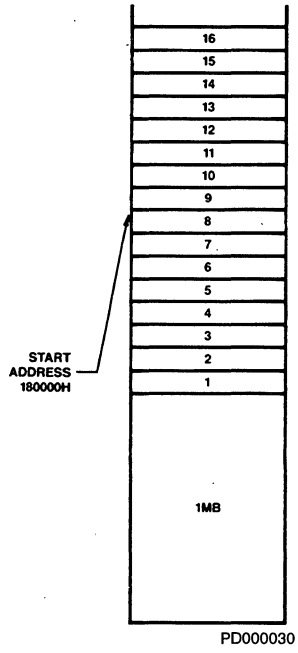
The boards come configured to run without auxiliary power back-up unless otherwise specified. A simple cut and jump can be used to provide for a back-up power supply to be switched in via the Memory Protect Control line and the auxiliary P_2 connector.

Transparent Refresh

On-board control circuitry automatically refreshes the dynamic RAM every 14μs. The maximum cycle time for refresh takes 350ns.

Figure 2. Rotary Switch Selection of Board Memory Start Address





PD000030

The above setting (18) on switches SW2 and SW3 correspond to board memory starting address of 180000 H.

SPECIFICATIONS

Word Size

8 or 16 bits

Memory Size

Am97/0521B:	524,288 bytes
Am97/0768B:	786,432 bytes
Am97/1024B:	1,048,576 bytes

MULTIBUS Interface

Compatible with IEEE P796

Maximum Timing

Access T_{ACC}	200ns
R/W Cycle T_{cycle}	300ns
Refresh T_{cycle}	350ns

Electrical Characteristics

DC Power Requirements

	Auxiliary Connector P_2
P_1 Supplies	Back-Up Supplies
+5V	+5VB
2.5A	0.8A

Physical Characteristics

Width:	30.48 in.	(12.00 cm)
Height:	17.15 in.	(6.75 cm)
Thickness:	1.27 in.	(.50 cm)
Weight:	1.25 lbs.	(568 gr.)

Environmental characteristics

Operating Temperature

0°C to 55°C (32°F to 130°F)

Operating Humidity

To 90% without condensation

Parity

Interrupt on selectable level with status register on selectable I/O port address

Address Selection

Switch selectable to one of 64K starting address boundaries

Reference Manual

059920049-001 – Am97/0000B Series 1 Megabyte RAM Boards

ORDERING INFORMATION

Part Number	Description
97/0512B	¼ Megabyte Dynamic RAM Board
97/0768B	¾ Megabyte Dynamic RAM Board
97/1024B	1 Megabyte Dynamic RAM Board

Am97/0000C Series

512K – 4 Megabyte RAM Boards
ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Supports up to 24-bit addressing for a maximum address range of 16 megabytes
- Board memory starts on any 64K byte boundary, selectable by rotary Hex switches. On-board memory can be set to cross any megabyte boundary or optionally stop on a megabyte boundary
- Optional look-out feature for flexibility:
  - Lower 32K and/or upper 64K addresses of first megabyte can be disabled on-board
- 8 or 16-bit word size with byte swapping capability
- High speed:
  - 200ns max. access time
  - 300ns max. cycle time
- Parity with latching error register and interrupt generation
- On-board refresh circuitry with jumper for optional external refresh control
- Power back-up facilities

GENERAL DESCRIPTION

The Am97/0000C Series is a family of high-density, MULTIBUS*-compatible, Random-Access Memory (RAM) boards. They make use of the latest in LSI technology to provide 512K to 4 megabytes of dynamic RAM memory on a single MULTIBUS* board. Extensive testing and 100% dynamic burn-in ensure high quality and performance.

*MULTIBUS is a registered trademark of Intel Corporation.

05199A

PRODUCT OVERVIEW

The Am97/0000C Series of dynamic Random-Access Memory boards is the perfect choice for system designers needing large memory space in their MULTIBUS systems. These boards make use of the latest in memory technology to provide up to four megabytes of high-speed, low-power memory on a MULTIBUS board. The boards come populated in the following sizes: 512K, 768K, 1, 2, 3, and 4 megabytes.

The addressing capabilities of the Am97/0000C boards provide great flexibility. These boards support up to 24-bit addresses for a range of 16 megabytes. They have 64K byte starting address resolution with the ability to cross any boundary. In addition, the lower 32K and upper 64K addresses of the first megabyte of memory can be locked-out.

Parity error detection logic is provided on board with interrupt generation capability and a latching register to store the physical row and byte of the occurrence. Other features include an auxiliary connector for back-up power with memory protect control line and automatic refresh.

The advanced design, incorporating several PALs** to minimize chip count and maximize space utilization, increases performance and ensures high quality. AMD puts the boards through 100% dynamic burn-in and extensive testing to further ensure a highly reliable product.

FUNCTIONAL DESCRIPTION

The Am97/0000C boards are single board, MULTIBUS memory systems that include a memory array, refresh logic, parity generator and checker, latching error register, address decoding and selection hardware, LED error indicator and the MULTIBUS interface logic (see Figure 1).

Configurations include various addressing options, memory timing schemes, parity error interrupts and battery back-up.

Addressing Scheme

These memory boards support up to 24-bit addressing to provide an addressing range of 16 megabytes. One jumper enables the memory to stop on any arbitrary megabyte boundary. Other jumpers enable the memory to cross megabyte boundaries to allow full use of the memory's capacity.

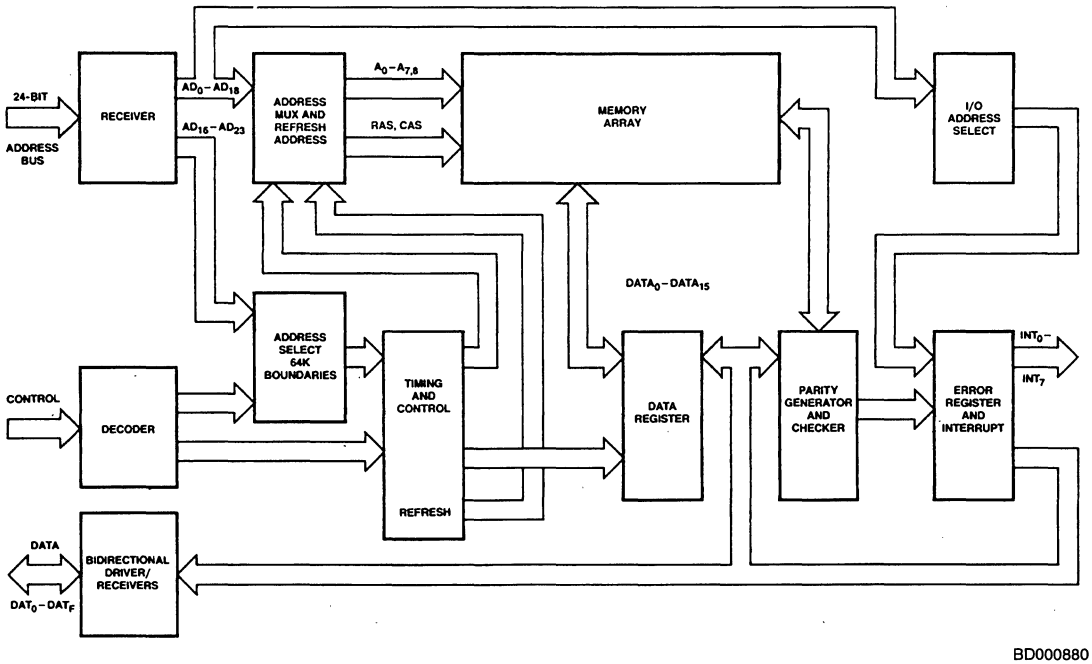
The board can start on any 64K boundary within the 16 megabyte address space available. Two rotary hexadecimal switches establish the exact starting address with one switch defining the megabyte boundary and the other, the 64K boundary (see Figure 2). If only 20 address bits are used, switch 3 is set to 0.

The boards have the ability to lock out portions of memory in the first megabyte (starting address 0H). The low order 32K bytes and the upper 64K bytes can be disabled by jumpers. The low order 32K byte lock-out is useful in many systems with memory on the host CPU board by enhancing the starting address resolution of the memory board to be 32K (i.e., the board would respond to addresses above 32K). Lock-out of the upper 64K bytes can be useful in systems, for example, that make use of those locations for I/O addresses.

Parity Error Detection

Parity logic is used on the Am97/0000C Series of boards to detect the occurrence of single bit errors. Parity is calculated and stored with each memory write and is calculated and checked with each memory read. On an error condition, the error register stores the physical row and byte locations of the error and the LED turns on. If a parity interrupt was enabled, then the error causes the generation of that interrupt over the MULTIBUS. The register can then be polled at its I/O address to find out the location of the parity error and take corrective action.

Figure 1. Am97/0000C Series Block Diagram



**PAL is a registered trademark of and is used under license from Monolithic Memories, Inc.

The error register I/O address can be chosen as one of 32 possible locations and is set by jumpers and a Hex switch. One jumper selects between an 8-bit and 16-bit I/O address scheme, another jumper selects the low order 8 bits as 00-0FH or 40-4FH, and the switch chooses the exact location within the low order 4 bits (see Figure 2).

Timing Consideration

Access times of 200ns maximum and cycle times of 300ns maximum mean high-performance dynamic RAM memory for a MULTIBUS system. To optimize system performance, user-adjustable Acknowledge signals are provided. Traditionally, AACK/ was used to improve system timing. However, the pin used to transmit the AACK/ signal is defined by IEEE P796 to be the LOCK/ signal. Therefore, the Am97/0000C boards provide an adjustable Transmit Acknowledge signal (XACK/) which can be user-adjustable with respect to memory read (MRDC/) at 50, 105, and 200ns ±15ns after the signal. XACK/ is transmitted 50ns ±15ns after the memory write signal. If AACK/ is needed, it can be optionally asserted via a jumper and would be equivalent to XACK/.

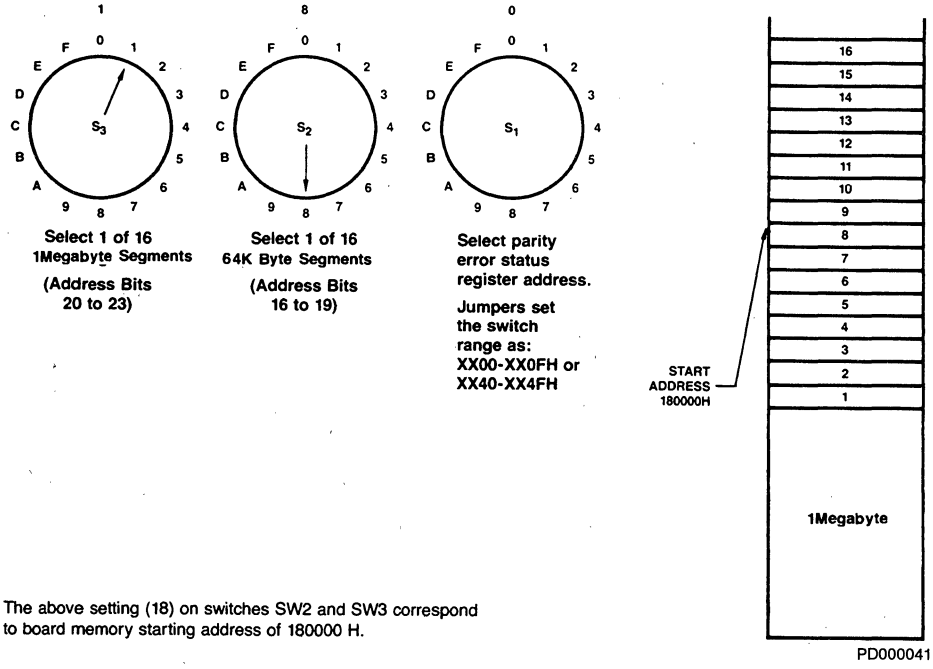
Auxiliary Power Back Up

The boards come configured to run without auxiliary power back-up unless otherwise specified. A simple cut and jump can be used to provide for a back-up power supply to be switched in via the Memory Protect Control line and the auxiliary P_2 connector.

Transparent Refresh

On-board control circuitry automatically refreshes the dynamic RAM every 14μs. The maximum cycle time for refresh takes 350ns. The board may be configured for external refresh.

Figure 2. Rotary Switch Selection of Board Memory Start Address



The above setting (18) on switches SW2 and SW3 correspond to board memory starting address of 180000 H.

PD000041

SPECIFICATIONS

Word Size

8 or 16 bits

Memory Size

Am97/0512C: 524,288 bytes
Am97/0768C: 786,432 bytes
Am97/1024C: 1,048,576 bytes
Am97/2048C: 2,097,152 bytes
Am97/3072C: 3,145,728 bytes
Am97/4096C: 4,194,304 bytes

MULTIBUS Interface

Compatible with IEEE P796

Maximum Timing

Access T_{ACC}	200ns
R/W Cycle T_{cycle}	300ns
Refresh T_{cycle}	350ns

Electrical Characteristics

DC Power Requirements

	Auxiliary Connector P_2
P_1 Supplies	Back-up Supplies
+5V	+5VB
2.5A	0.8A

Physical Characteristics

Width:	12.00 in.	(30.48 cm.)
Height:	6.75 in.	(17.15 cm.)
Thickness:	.50 in.	(1.27 cm.)
Weight:	1.25 lbs.	(568 gr.)

Environment characteristics

Operating Temperature

0°C to 55°C (32 to 130°F)

Operating Humidity

To 90% without condensation

Parity

Interrupt on selectable level with status register on selectable I/O port address

Address Selection

Switch selectable to one of 64K starting address boundaries

ORDERING INFORMATION

Part Number	Description
97/0512C	½ Megabyte Dynamic RAM Board
97/0768C	¾ Megabyte Dynamic RAM Board
97/1024C	1 Megabyte Dynamic RAM Board
97/2048C	2 Megabyte Dynamic RAM Board
97/3072C	3 Megabyte Dynamic RAM Board
97/4096C	4 Megabyte Dynamic RAM Board

Am96/0000L Series

512K – 4 Megabyte RAM Boards with LBX
ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Dual-port architecture:
  - MULTIBUS*
  - LBX bus
- Superior memory access performance over LBX:
  - Zero wait states at 5 and 6MHz CPU operation
  - One wait state at 8 and 10MHz CPU operation
- High speed
  - 225ns maximum access time
  - 300ns maximum cycle time
- Board may reside anywhere in 16 megabyte address range starting on a 64K byte boundary
- Optional lock-out feature for flexibility:
  - Upper 64K addresses of first megabyte can be disabled on-board
- 8 or 16-bit word size with byte swapping capability
- Parity with latching error register and interrupt generation
- On-board refresh circuitry with jumper for optional external refresh control

GENERAL DESCRIPTION

The Am96/0000L Series is a family of high-performance, dual-ported MULTIBUS Random-Access Memory (RAM) boards. Available in sizes ranging from 512K bytes to 4 megabytes with parity, they feature high-speed access via either of two ports, the MULTIBUS or the LBX bus. Making use of the LBX bus can greatly improve a system's performance by providing CPU-memory access over a private bus, thus reducing the saturation of the MULTIBUS. The Am96/0000L Series meets IEEE P796 specifications (with proposed LBX addition).

*MULTIBUS is a registered trademark of Intel Corporation.

05195A

PRODUCT OVERVIEW

The Am96/0000L Series of dynamic RAM boards provides superior performance and density required of memory in leading-edge MULTIBUS systems. These boards come in sizes up to 4 megabytes with 225ns access time using only 16 watts maximum. They also have dual-ported architecture with the LBX bus interface which establishes a private bus between memory and CPU. This reduces bus saturation on the MULTIBUS and improves system throughput.

The memory can occupy any location in a 16 megabyte range with 64K byte starting address resolution. Four of these boards in the 4 megabyte size provides for complete address space as specified by IEEE P796. The high density available means the complete 16 megabyte memory can reside on the LBX bus which allows a maximum of five boards.

Parity error detection logic is provided on-board with interrupt generation capability and a latching register to store the physical row and byte of the error. The board also offers automatic on-board refresh and optional external refresh.

The advanced design uses PALs* to minimize chip count, maximize space utilization and power consumption, and increase performance. AMD puts the boards through 100% dynamic burn-in and extensive testing to further ensure a highly reliable product.

FUNCTIONAL DESCRIPTION

The Am96/0000L boards include a memory array, refresh logic, parity generator and checker, latching error register, data register, address decoding and selection hardware, and MULTIBUS and LBX interface logic.

Configurations include various addressing options, memory timings, and parity-error interrupts.

Addressing Scheme

These memory boards support up to 24-bit addressing to provide an addressing range of 16 megabytes. They can start on any 64K boundary within the available address space. Memory locations on the board have the same addresses on the MULTIBUS and LBX bus.

The last 64K of the first megabyte of memory can be disabled by jumper. This lock-out feature can be useful in systems, for example, that make use of those locations for I/O addresses.

LBX Bus

The Local Bus Extension (LBX) bus expands the capability of MULTIBUS systems by providing a private CPU-to-memory bus. High-speed memory accesses can take place over the LBX bus, and thus free up the MULTIBUS for other communications.

The bus specification calls for a maximum of five boards utilizing the LBX bus. Therefore, the high density of the Am96/0000L Series provides for the capability to make use of the complete 16 megabyte address space addressable over the LBX bus.

Parity Error Detection

Parity logic is used on the Am96/0000L Series of boards to detect the occurrence of errors. Parity is calculated and stored with each memory write and is calculated and checked with each memory read. On an error condition, the error register stores the physical row and byte locations of the error. If a parity interrupt was enabled, then the error causes the generation of that interrupt over the MULTIBUS. The register can then be polled at its I/O address to find out the location of the parity error and take corrective action.

The error register I/O address can be configured for 8-bit or 16-bit I/O address schemes and can occupy one of 32 possible locations, 00-0FH or 40-4FH.

Parity checking can be optionally disabled.

Timing Considerations

Access times of 225ns maximum and cycle times of 300ns maximum mean high-performance dynamic RAM memory for a MULTIBUS system. To optimize system performance, a user-adjustable Acknowledge signal is provided (XACK/) which can be adjusted with respect to memory read (MRDC/) at 105 or 225ns ±15ns after the signal. XACK/ is transmitted 50ns ±15ns after the memory write signal (MWTC/).

Memory Refresh

On-board control circuitry automatically refreshes the dynamic RAM every 14μs. The maximum cycle time for refresh takes 350ns. External refresh is optional and can be asserted by jumper.

*PAL is a registered trademark of and is used under license from Monolithic Memories, Inc.

Am94/0350

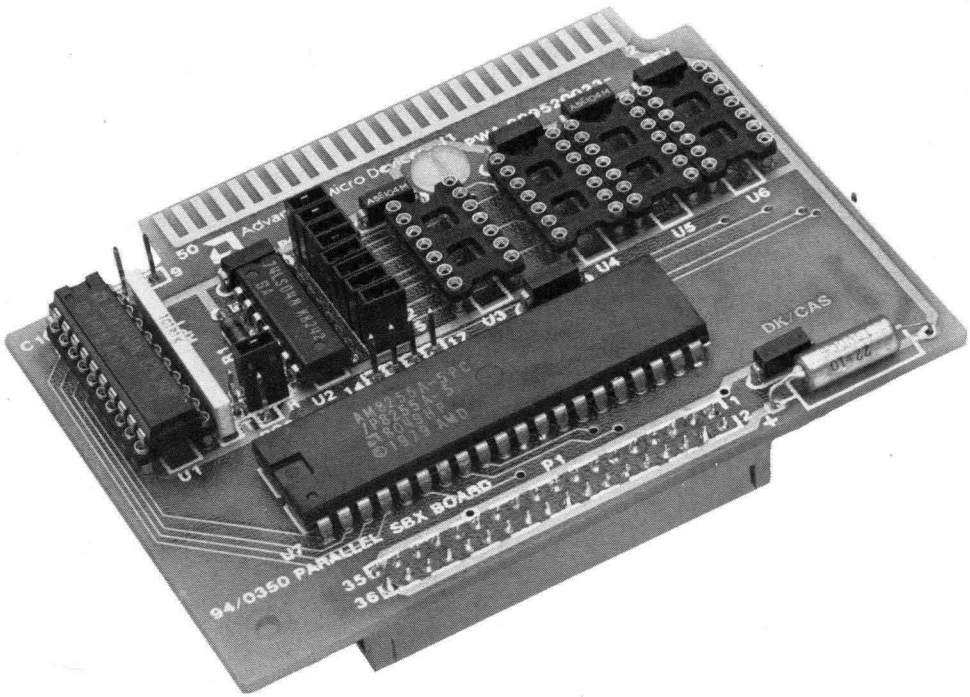
Parallel I/O SBX Module

DISTINCTIVE CHARACTERISTICS

- SBX bus interface provides incremental expansion
- Fully compatible with the Intel iSBX 350 Multimodule* board
- Utilizes an 8255A-5 Programmable Peripheral Interface for 24 programmable I/O lines
- Sockets provided for line drivers and terminators to configure I/O
- Four jumper-selectable interrupts
- 8-hit single-width SBX module

GENERAL DESCRIPTION

The Am94/0350 Parallel I/O SBX Module is a single-width module providing 24 programmable I/O lines. Sockets for line drivers and terminators are provided for custom configuration. This module attaches to any host board which supports the Intel iSBX* bus.



*Multimodule and iSBX are registered trademarks of Intel Corporation.

04281A

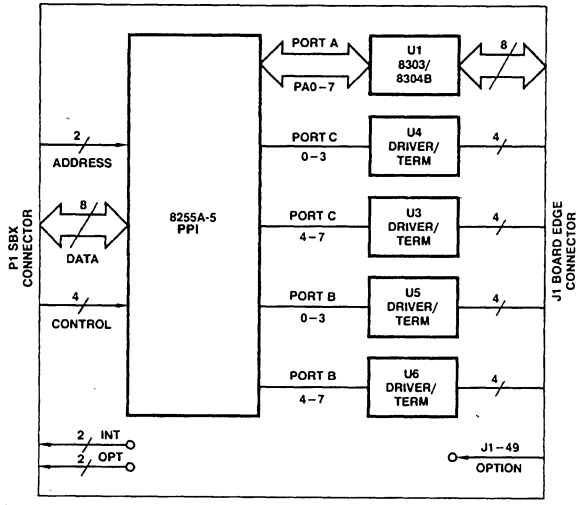
PRODUCT OVERVIEW

The Am94/0350 Parallel I/O (PIO) Module is an 8-bit single-width SBX module which provides the designer a low-cost, high-performance method for adding incremental I/O capability. The module consists of an 8255A-5 Programmable Peripheral Interface (PPI) and sockets for line drivers and terminators which provide for 24 lines of configurable parallel I/O.

FUNCTIONAL DESCRIPTION

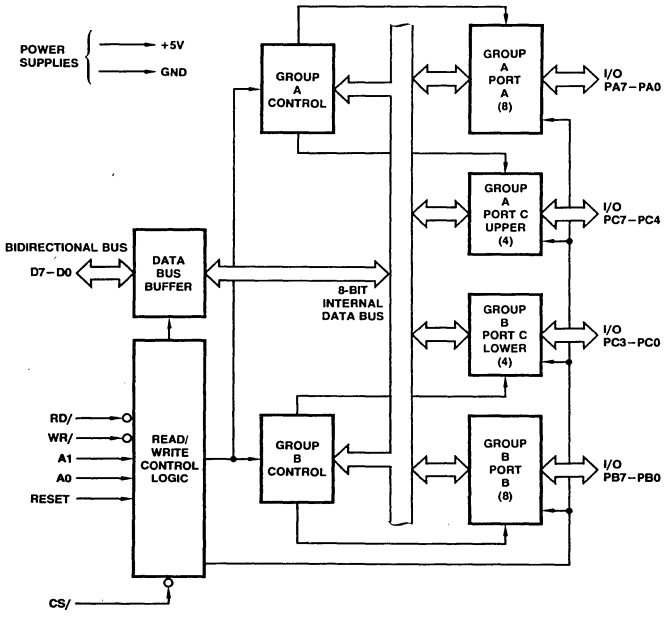
The Am94/0350 PIO Module contains an 8255A-5 PPI and sockets for interchangeable line drivers and terminators (see Figures 1 and 2 for Block Diagrams). The 24 programmable I/O lines are divided into three 8-bit ports (Ports A, B and C). The board provides up to four interrupts.

Figure 1. Am94/0350 Parallel I/O SBX Module Block Diagram



BD000891

Figure 2. 8255A Programmable Peripheral Interface Block Diagram



BD000900

TABLE 1. Mode Definition Summary

Port		Mode 0		Mode 1		Mode 2	
		In	Out	In	Out	Group A Only	
A	PA0	In	Out	In	Out	Bidirectional	
	PA1	In	Out	In	Out	Bidirectional	
	PA2	In	Out	In	Out	Bidirectional	
	PA3	In	Out	In	Out	Bidirectional	
	PA4	In	Out	In	Out	Bidirectional	
	PA5	In	Out	In	Out	Bidirectional	
	PA6	In	Out	In	Out	Bidirectional	
	PA7	In	Out	In	Out	Bidirectional	
B	PB0	In	Out	In	Out	–	Mode 0 or Mode 1 Only
	PB1	In	Out	In	Out	–	
	PB2	In	Out	In	Out	–	
	PB3	In	Out	In	Out	–	
	PB4	In	Out	In	Out	–	
	PB5	In	Out	In	Out	–	
	PB6	In	Out	In	Out	–	
	PB7	In	Out	In	Out	–	
C	PC0	In	Out	Interrupt B	Interrupt B	I/O	
	PC1	In	Out	Buffer Full B	Buffer Full B	I/O	
	PC2	In	Out	Strobe B	Acknowledge B	I/O	
	PC3	In	Out	Interrupt A	Interrupt A	Interrupt A	
	PC4	In	Out	Strobe A	I/O	Strobe A	
	PC5	In	Out	Buffer Full A	I/O	Input Buffer Full	
	PC6	In	Out	I/O	Acknowledge A	Acknowledge A	
	PC7	In	Out	I/O	Buffer Full A	Output Buffer Full	

Port A can be input, output or bidirectional, according to the mode set. An 8304B bidirectional bus transceiver is supplied for users requiring non-inverted applications. The user can also replace the 8304B with an inverting 8303, as required. Data direction of the 8304B/8303 buffer is optional and is selected by jumper. The options are transmit (T), receive (R), or software control through Port C, pin 6 (PC6).

Ports B and C have 14-pin sockets to allow the installation of user-provided line drivers or terminator devices in U3–U6, as required by the application. Port B can be an input or output port and Port C can be an input, output or control port.

Programming Considerations

The 8255A-5 PPI allows the user to program the Am94/0350 PIO Module in three software-selected modes of operation (see Table 1 for Mode Definition Summary).

Mode 0, Basic I/O, allows simple input or output operation to each port without handshaking.

Mode 1, Strobed I/O, allows Ports A and B to transfer data using Port C as the handshaking line.

Mode 2, Strobed Bidirectional Bus I/O, provides a bidirectional 8-bit data bus (Port A) with handshaking.

I/O Addressing

The three signals used to select the 8255A-5 PPI on the Am94/0350 PIO Module are Address 0 (MA0), Address 1 (MA1) and Chip Select (MCS0/). As shown in Table 2 the addresses are used to select among the three ports and the control register. Note that the control register is Write Only. Trying to read the control register is an illegal operation.

Interrupt Requests

There are four jumper-selectable interrupt requests. One can be generated from the I/O device over the user option I/O interface line J1–49. Two others can be generated by the 8255A-5 PPI. The fourth is provided as a user-defined interrupt.

Installation

The Am94/0350 PIO Module plugs directly into the female SBX connector on the host board. The module is then secured with a nylon post to firmly attach it to the host.

TABLE 2. I/O Port Addressing

MCSO/	MA1	MA0	Result
H	X	X	Chip Disabled
L	L	L	Port A
L	L	H	Port B
L	H	L	Port C
L	H	H	Control (Write Only)

H=HIGH
L=LOW
X=Don't care

SPECIFICATIONS

Word Size

Data – bits

Access Times

Read – 50ns max.
Write – 300ns max.

Note: The above times are taken from the iSBX Bus Specification, number 142686-002. Actual transfer speed is dependent upon the cycle time of the host microcomputer.

I/O Capacity

24 programmable lines

Interface Connectors

P1 SBX
- 36-pin, dual row, 0.1 in. centers

J1 Parallel I/O
- 50-pin board edge, 0.1 in. centers (Mates with 3M 3415-0001 or equivalent)

Interfaces

SBX Bus
- Meets the Intel iSBX bus specification

Parallel
- All signals TTL compatible

Interrupts

Interrupt requests may originate from the 8255A-5 PPI or the user-supplied I/O.

Line Drivers

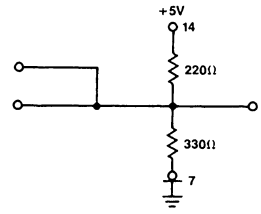
The following line drivers are all compatible with I/O driver sockets on the Am94/0350 PIO Module.

Driver	Characteristics	Sink Current (mA)
7438	Inverting Open Collector	48
7437	Inverting	48
7432	Non-Inverting	16
7426	Inverting Open Collector	16
7409	Non-Inverting Open Collector	16
7408	Non-Inverting	16
7403	Inverting Open Collector	16
7400	Inverting	16

Terminators

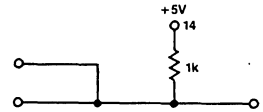
The sockets also allow the use of special terminator resistor packs SBC 901 and SBC 902.

SBC 901
220/330 14-PIN DIP
(DUAL IN-LINE PACKAGES)
TERMINATOR



TC000280

SBC 902
1K 14-PIN DIP PULL UP



TC000270

Physical Characteristics

Width:	3.70 in.	(9.40 cm.)	
Height:	2.85 in.	(7.24 cm.)	
Thickness:	0.40 in.	(1.02 cm.)	– Module only
	1.00 in.	(2.50 cm.)	– Module and Host Board
Weight:	1.62 oz.	(46 gr.)	
Shipping Weight:	1.00 lb.	(454 gr.)	

Electrical Characteristics

DC Power Requirements

+5V ±5% at:
- 385mA max. when sockets U3–U6 are empty
- 575mA max. when sockets U3–U6 have 7438 buffers
- 685mA max. when sockets U3–U6 have 220/330 terminators

Environmental Characteristics

Operating Temperature
- 0°C to 55°C (32°F to 130°F) with free moving air across the base board and the module

Operating Humidity
- 0 to 90% without condensation

Storage Temperature
- –55°C to +85°C (–67°F to +185°F)

Storage Humidity
- 0 to 99% without condensation

Reference Manual

059920052-001 – Am94/0350 Parallel I/O SBX Module

ORDERING INFORMATION

Part Number	Description
94/0350	Parallel I/O SBX Module
Companion Products	
94/2000	SBX Motherboard
96/5232	Programmable RAM/EPROM and I/O Board
97/8605 Series	8086-Based 16-Bit Single Board Computers

iSBX 350 and Am94/0350 Jumper Comparison

Application Note by Doug Kern
Microcomputer Systems Directorate

INTRODUCTION

The following pages are a "pin-for-pin comparison" of Intel's iSBX* 350 board and our Am94/0350 Parallel I/O (PIO) SBX Module. The intent is to show their functional similarities and to provide a quick reference list for reconfiguring to user requirements.

The following table starts on the left with a consecutive list of numbers from 1 to 26, which represent jumper pin numbers. The next column to the right is a list of jumpers that appear on Intel's iSBX 350 board. When a jumper does not exist on-board, the word N/C is written in its place. The next column to the right contains the pin number on the Am94/0350 PIO with the signal that corresponds to that provided by the Intel board jumper. The last column contains the signal description, as specified by the Intel schematic.

iSBX 350 and 94/0350 Jumper Comparison

	Intel	AMD	
PIN #	iSBX 350	Am94/0350	SIGNAL
1	1	10	Transmit
2	2	11	Port A Direction
3	3	12	Receive
4	4	13	Software Control
5	5	8	+5V
6	6	9	I/O Device
7	7	0R	8255 PC0
8	8	0L	I/O Device PC0
9	9	1R	8255 PC1
10	10	1L	I/O Device PC1
11	11	2R	8255 PC2
12	12	2L	I/O Device PC2
13	13	3R	8255 PC3
14	14	3L	I/O Device PC3
15	15	15	OPT0
16	16	16	MINTR0
17	17	14	OPT1
18	18	17	MINTR1
19	19	4R	8255 PC4
20	20	4L	I/O Device PC4
21	21	5R	8255 PC5
22	22	5L	I/O Device PC5
23	23	6R	8255 PC6
24	24	6L	I/O Device PC6
25	25	7R	8255 PC7
26	26	7L	I/O Device PC7
Driver Terminator Sockets			
	U3	U3	PC4-7
	U4	U4	PC0-3
	U5	U5	PB0-3
	U6	U6	PB4-7

*iSBX is a registered trademark of Intel Corporation.

05288A

Am94/0351

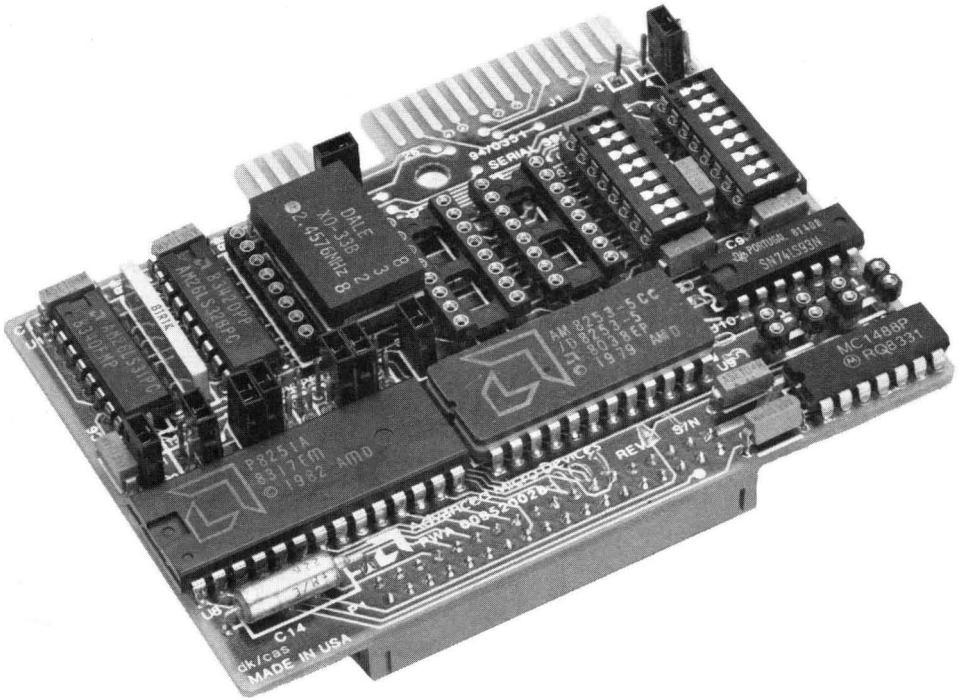
Serial I/O SBX Module

DISTINCTIVE CHARACTERISTICS

- SBX bus interface
- One programmable synchronous/asynchronous channel of serial I/O with support for RS-232C or RS-449/422 interface
- Fully compatible with the Intel iSBX* 351 Multimodule* board
- Three software-programmable counter/timers
  - One for use as baud rate generator
  - Two as optional interval timers
- Four jumper-selectable interrupts

GENERAL DESCRIPTION

The Am94/0351 Serial I/O SBX Module provides one channel of programmable synchronous/asynchronous serial I/O for RS-232C or RS-449/422 interfaces. Three programmable, 16-bit counter/timers are provided, with one available to generate baud rate for the serial channel and the other two available to the host. This module attaches to any host board which supports the Intel iSBX bus.



*iSBX and Multimodule are registered trademarks of Intel Corporation.

05072A

PRODUCT OVERVIEW

The Am94/0351 Serial I/O (SIO) Module is an 8-bit, single-width SBX module which provides a low-cost, high-performance method for adding incremental I/O capability. The module uses an 8251A Programmable Communications Interface (PCI) and an 8253-5 Programmable Interval Timer (PIT) to provide a programmable serial communications channel. Sockets and configuration blocks are supplied to customize the module for the specific RS-232C or RS-449/422 application.

FUNCTIONAL DESCRIPTION

The 8251A PCI can be programmed to operate under several serial data transmission methods in synchronous and asynchronous modes. Some of the key features include full duplex, double-buffered transmitter and receiver, and error detection for parity, overrun, and framing.

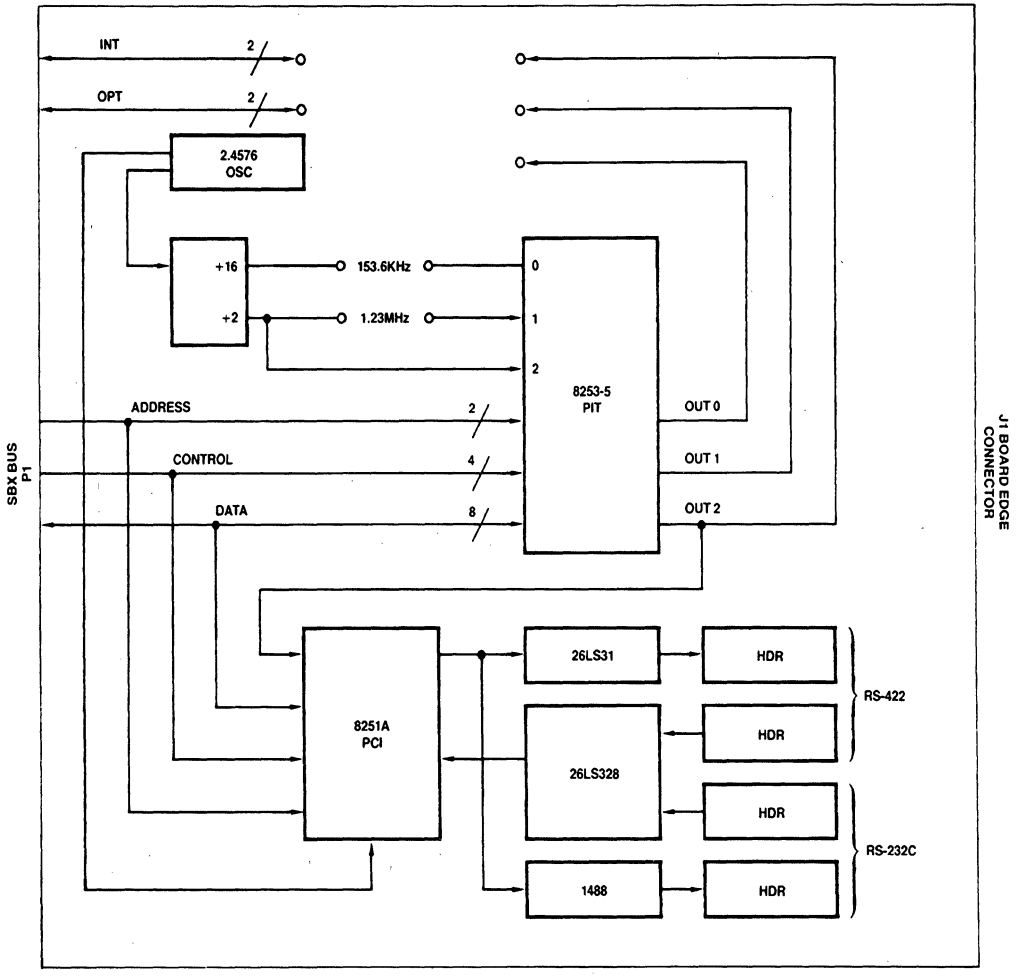
The 8253-5 PIT is organized as three independent, software-programmable, 16-bit counters. Both BCD and binary counting are possible. One counter may be used to generate the baud rate required by the 8251A, leaving the other two available for use by the host board.

RS-232C and RS-449/422 interfaces are supported. High reliability sockets are provided so the user can add termination resistor packs for RS-422 or slew rate capacitors for RS-232C operation. Configuration blocks are also provided to customize the board by supplying the correct signals to the board-edge connector (see Figure 1 for the Block Diagram).

Interrupts

The Am94/0351 has four possible sources. Two of the interrupt requests are originated by the 8251A PCI. These are generated when a character is ready to be transferred to the host and when a character has been transmitted. The other two interrupts can be generated by the 8253-5 PIT and are jumper-selectable by the user.

Figure 1. Am94/0351 Serial I/O SBX Module Block Diagram



BD000910

SPECIFICATIONS

Clock Frequency

2.4576MHz crystal oscillator

Word Size

Data – 8 bits

Access Times

Read – 250ns max
Write – 300ns max
Note: The above times are taken from the iSBX Bus Specification, number 142686-002. Actual transfer speed is dependent upon the cycle time of the host microcomputer.

Interface Connectors

P1 SBX:
– 36-pin dual row, 0.1 in. centers

J1 Serial I/O

RS-232C:
– 26-pin board edge, 0.1 in. centers
(Mates with 3M 3462-0001 or equivalent)

RS-422:
– 40-pin board edge, 0.1 in. centers
(Mates with 3M 3464-0001 or equivalent)

Interfaces

SBX Bus
– Meets the Intel iSBX bus specification

Serial I/O
– EIA standard RS-232C signals supported:

Clear-To-Send	(CTS)
Data-Set-Ready	(DSR)
Data-Terminal-Ready	(DTR)
Request-To-Send	(RTS)
Receive Clock	(RCLK)
Transmit Clock	(TCLK)
Receive Data	(RXD)
Transmit Data	(TXD)
Frame Ground	(FG)
Signal Ground	(SG)

– EIA standard RS-422 signals supported:

Clear-To-Send	(CS)
Data Mode	(DM)
Terminal Ready	(TR)
Request-To-Send	(RS)
Receive Timing	(RT)
Receive Data	(RD)
Terminal Timing	(TT)
Send Data	(SD)
Shield	(SHIELD)
Receive Common	(RC)
Send Common	(SC)
Signal Ground	(SG)

Serial I/O Port Addressing

MCS1/	MCS0/	MA1	MA0	Result
L	L	X	X	Illegal Condition
H	H	X	X	Module Not Selected
H	L	X	L	8251A Data
H	L	X	H	8251A Command
L	H	L	L	8253-5 Counter 0
L	H	L	H	8253-5 Counter 1
L	H	H	L	8253-5 Counter 2
L	H	H	H	8253-5 Mode Word
Note: The 8253-5 Mode Word is a write only register.				

H = HIGH
L = LOW
X = Don't care.

Serial Communications

One Synchronous/Asynchronous Serial Channel

Synchronous:
– 5 – 8 bit characters
– Internal character synchronization
– Automatic sync insertion
– Even/odd/no parity generation/detection
– Baud rate – DC to 64K

Asynchronous:
– 5 – 8 bit characters
– False start bit detection
– 1, 1.5, 2 stop bits
– Break character generation/detection
– Even/odd/no parity generation/detection
– Baud rate – DC to 19.2K

8253-5 Rate Generator Frequencies and Timer Intervals

	Single Timer (1) Counter 0		Single Timer (2) Counter 1		Dual Timer 0 and 1 Series	
	Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**
Rate Generator Frequency	18.76Hz	614.4KHz	2.34Hz	76.8KHz	286.0μHz	307.2KHz
Time Interval	1.63μs	53.3ms	13.0μs	426.7ms	3.26μs	58.25 min

Notes: 1. Assumes the 1.23MHz Clock Input.
2. Assumes the 153.6KHz Clock Input.

Physical Characteristics

Width: 3.70 in. (9.40 cm.)
Height: 2.85 in. (7.24 cm.)
Thickness: 0.40 in. (1.02 cm.) – Module only
1.00 in. (2.50 cm.) – Module and Host Board
Weight: 1.90 oz. (55 gr.)
Shipping Weight: 1.00 lb. (454 gr.)

Electrical Characteristics

DC Power Requirements

Mode	Voltage	Amps (Max)
RS-232C	+5V ± 5%	450mA
	+12V ± 5%	30mA
	−12V ± 5%	30mA
RS-422	+5V ± 5%	520mA

Environmental Characteristics

Operating Temperature
– 0°C to 55°C (32°F to 130°F) with free moving air across the base board and the module

Operating Humidity
– 0 to 90% without condensation

Storage Temperature
– −55°C to +85°C

Storage Humidity
– 0 to 99% without condensation

Reference Manual

059920061-001 – Am94/0351 Serial I/O SBX Module

ORDERING INFORMATION

Part Number	Description
94/0351	Serial I/O SBX Module
Companion Products	
94/2000	SBX Motherboard
96/5232	Programmable RAM/EPROM and I/O Board
97/8605 Series	8086-Based 16-Bit Single Board Computers

iSBX 351 and Am94/0351 Jumper Comparison

Application Note by Doug Kern
Microcomputer Systems Directorate

INTRODUCTION

The following pages are a "pin-for-pin comparison" of Intel's iSBX*351 board and our Am94/0351 Serial I/O (SIO) SBX Module. The intent is to show their functional similarities and to provide a quick reference list for reconfiguring to user requirements.

The following table starts on the left with a consecutive list of numbers from 1 to 38 which represent jumper pin numbers. The next column to the right is a list of jumpers that appear on Intel's iSBX 351 board. When a jumper does not exist on-board, the word "none" is written in its place. The next column to the right contains the pin number on the Am94/0351 SIO with the signal that corresponds to that provided by the Intel board jumper. The last column contains the signal description, as specified by the Intel schematic.

iSBX 351 and 94/0351 Jumper Comparison

PIN #	Intel iSBX0351	AMD Am94/0351	SIGNAL	
1	1	4	Power	
2	2	3	+5V	
3	3	2	SC	
4	4	1	GND	
5	5	none	RS-232C GND	(See Note 1)
6	6	none	GND	(See Note 1)
7	7	7	FG or Shield	
8	8	8	GND	
9	9	5	RC	
10	10	6	GND	
11	11	11	DTR*	
12	12	12	DTR to Driver	
13	13	9	RS-422 Driver EN	
14	14	none	Soft 5	(See Note 2)
15	15	10	GND	
16	16	none	GND	
17	17	15	150KHz Clk	
18	18	16	8253 Clk 0	
19	19	27	1.23MHz Clk	
20	20	28	8253 Clk 1	
21	21	24	8253 Gate 0	
22	22	23	8253 Gate 1	
23	23	22	OPT1	
24	24	21	8253 Out0	
25	25	25	OPT0	
26	26	26	8253 Out1	
27	27	20	TxCLK	
28	28	19	8253 Out2	
29	29	18	RxCLK 8251	
30	30	17	8253 Out2	
31	31	14	RxCLK 8251	
32	32	13	RxCLK Out	
33	33	31	MINTR1	
34	34	32	TxRDY	
35	35	29	MINTR0	
36	36	30	RxRDY	
37	37	34	LS161 CLK Input	
38	38	33	2.26MHz CLK Input	
Shunts				
	U4	U4	RS-422-	
	U5	U5	RS-422+	
	U6	U7	RS-232C	
	U7	U6	RS-232C Power	

Note: 1. Jumper is not required, removal of the RS-232C shunt will remove ground.
2. Jumper is not required to a pull-up resistor.

*iSBX is a registered trademark of Intel Corporation.

05289A

Am94/1530

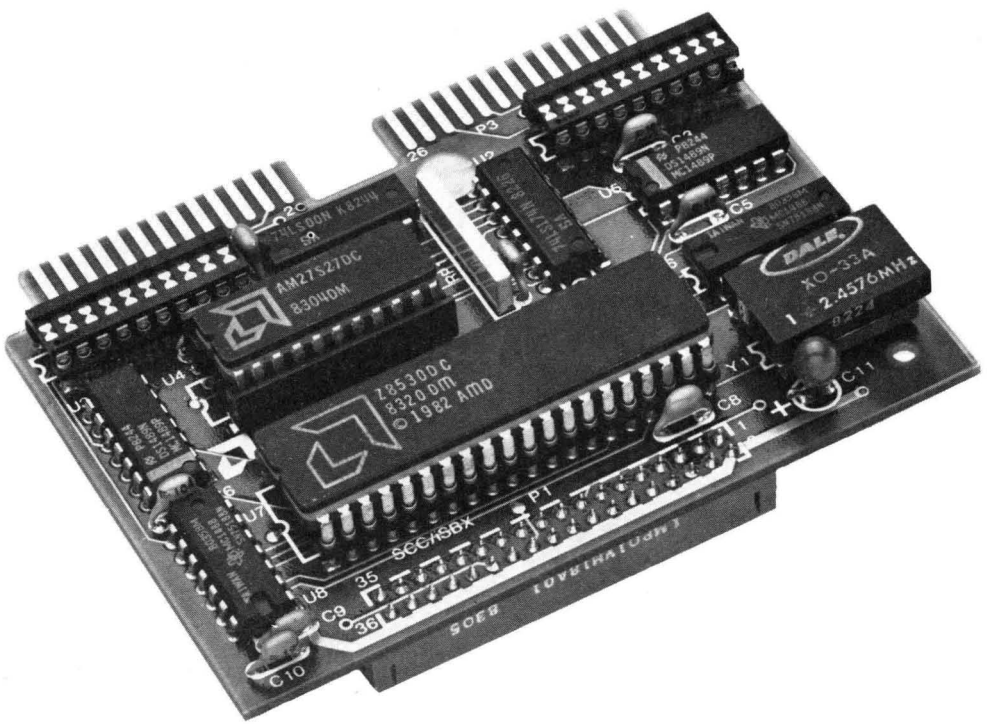
Dual-Channel Serial Communications
Controller SBX Module

DISTINCTIVE CHARACTERISTICS

- Incorporates the Z8530* Serial Communications Controller
- Programmable baud rate generator per channel
- Synchronous or asynchronous operation
- Communications rates of up to 38,400 baud asynchronous and 614,400 BPS synchronous
- Extensive interrupt capabilities
- Crystal oscillator
- Programmable for NRZ, NRZI, or FM coding
- SDLC/HDLC and bisynchronous modes

GENERAL DESCRIPTION

The Am94/1530 is an SBX module that provides two independent, full duplex RS-232C serial communications channels with multiple protocol operation. The module attaches to any host board which supports the Intel iSBX** bus and offers incremental on-board I/O expansion.



*Z8530 is a trademark of Zilog, Inc.
**iSBX is a registered trademark of Intel Corporation.

04248B

PRODUCT OVERVIEW

The Am94/1530 is a programmable, dual channel serial communications module for the SBX bus. The module adds two RS-232C serial channels to any host board which includes an SBX bus compatible connector. This enables the designer to add incremental I/O capability at lower cost and higher performance than alternative methods.

FUNCTIONAL DESCRIPTION

The Am94/1530 is an 8-bit SBX module which incorporates the Z8530 Serial Communications Controller (see Block Diagram in Figure 1). This high-performance module provides dual-channel RS-232C multiprotocol data communication. It is software configured to satisfy a wide variety of serial communication needs. The Am94/1530 handles asynchronous formats, synchronous byte-oriented protocols such as IBM Bisync and synchronous bit-oriented protocols such as HDLC and IBM SDLC.

The on-board Z8530 SCC can be programmed to handle all common asynchronous formats regardless of data size, number of stop bits, or parity requirements. Within each operating mode the SCC allows for protocol variations by checking odd or even parity, CRC generation and checking, break generation and detection, and many other protocol-dependent features.

Figure 1. Am94/1530 Block Diagram

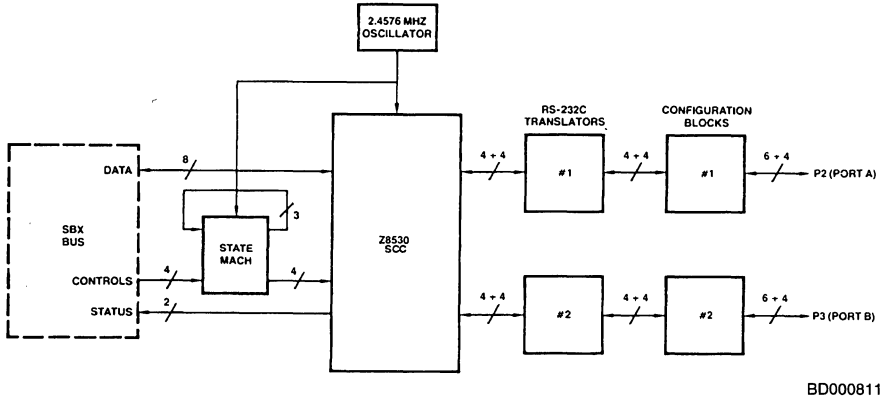
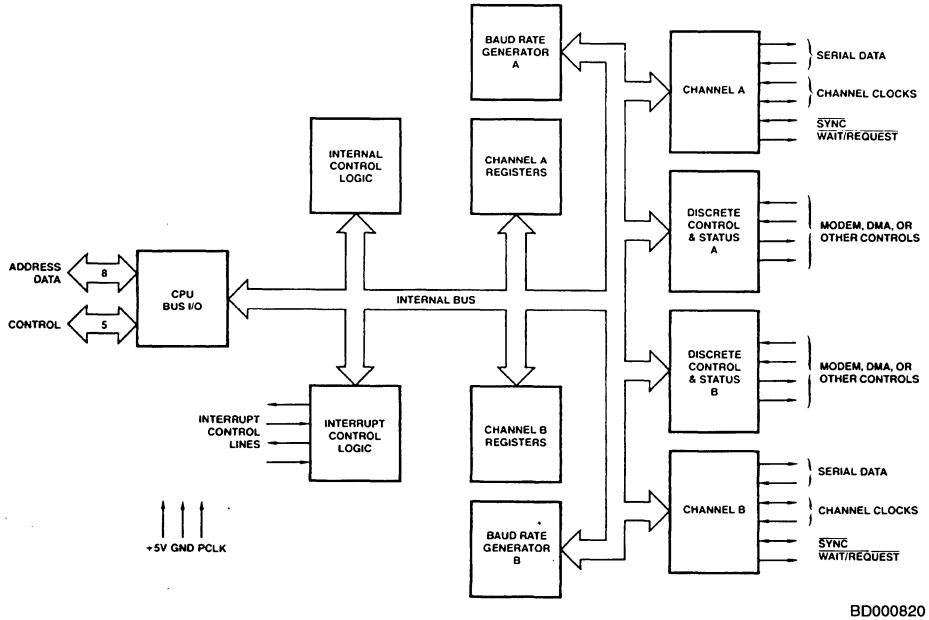


Figure 2. Z8530 SCC Block Diagram



Programming Considerations

The Z8530 SCC contains several registers which must be programmed to initialize and control each of the two channels. The SCC Technical Manual (#AIZ-2135) contains detailed descriptions of these registers. In addition, the Am94/1530 SCC/SBX Module User's Manual (#059920037-001) contains detailed instructions for initializing the Z8530, as well as examples of interrupt handlers.

Configuration Blocks

Two jumper blocks are provided on the Am94/1530 Module, one for each serial channel. These enable the module to be easily modified to handle a variety of RS-232C modes (see Figure 3).

Installation

The Am94/1530 Module plugs directly into the female SBX connector on the host board. The module is then secured with a nylon post to firmly attach it to the host.

Figure 3. Configuration Block

RTxC	1	20	Transmit Timing (DTE)
TRxC	2	19	Transmit Timing (DCE)
CTS	3	18	Request to Send
RTS	4	17	Clear to Send
n/c	5	16	Carrier Detect*
n/c	6	15	Ring Indicator*
DCD	7	14	Data Terminal Ready*
DTR	8	13	Data Set Ready
RxD	9	12	Transmit Data
TxD	10	11	Receive Data

*Mutually Exclusive

SPECIFICATIONS

Clock Frequency

2.4576MHz

Word Size

Data – 8 bits

Access Times

Interrupt Acknowledge – 2 μsec max.
Read or Write – 1.5 μsec max.

Serial Communications

Two independent full-duplex channels

Synchronous/Isosynchronous Data Rates

- Up to 614.4K bits/second
- Up to 153.6K bits/second (FM encoding)
- Up to 76.8K bits/second (NRZI encoding)

Receive data registers quad buffered
Transmit data registers double buffered

Asynchronous Capabilities

- 5, 6, 7, or 8 bits per character
- 1, 1½, or 2 stop bits
- Odd or even parity
- Times, 1, 16, 32 or 64 clock modes
- Break generation and detection
- Parity, overrun and framing error detection

Byte-Oriented Synchronous Capabilities

- Internal character synchronization
- 1 or 2 sync character
- Automatic sync character insertion and deletion
- 6 or 8-bit sync character

SDLC/HDLC Capabilities

- Abort sequence generation and checking
- Automatic zero insertion and deletion
- Automatic flag insertion between messages
- Address field recognition
- I-field residue handling
- CRC generation/detection
- SDLC loop mode with EOP recognition/loop entry and exit

NRZ, NRZI or FM Encoding/Decoding
Baud rate generator per channel
Digital Phase-Locked Loop for clock recovery

Sample Baud Rate Dividers

Divider	Baud Rate (x16)	Bit Rate (x1)
696	100	
254	300	4800
126	600	9600
62	1200	19200
30	2400	38400
14	4800	76800
6	9600	153600
2	19200	307200
0	38400	614400

Interfaces

SBX Bus:

- Meets the Intel iSBX bus specification

Serial:

- Meets the EIA RS-232C standard

Signals Provided

- Transmit Timing (DTC)
- Transmit Timing (DCE)
- Request to Send
- Clear to Send
- Carrier Detect*
- Ring Indicator*
- Data Terminal Ready*
- Data Set Ready
- Transmit Data
- Receive Data
- Signal Ground
- Protective Ground

*mutually exclusive

Interface Connectors

Board Edge Connector

- 26 pins, 100 mil centers
- Mates with 3M 3462-0001 or equivalent

Physical Characteristics

Width:	3.70 in.	(9.40 cm.)
Height:	2.85 in.	(7.24 cm.)
Thickness:	0.40 in.	(2.79 cm.)
Weight:	2 oz.	(57 gr.)
Shipping Weight:	1 lb.	(454 gr.)

I/O Addressing

MCS0	MCS1	MA1	MA0	Function
H	H	X	X	Am94/1530 Not Selected
L	H	L	L	Port B Control
L	H	L	H	Port B Data
L	H	H	L	Port A Control
L	H	H	H	Port A Data
H	L	X	X	Interrupt Acknowledge
L	L	X	X	Illegal

H = HIGH
L = LOW
X = Don't care.

Electrical Characteristics

DC Power Requirements

+5 Volts at 560 mA max.
+12 Volts at 50 mA max.
−12 Volts at 50 mA max.

Environmental Characteristics

Operating Temperature: 0°C to 55°C with free moving air across the base board and the module

Operating Humidity: To 90% without condensation

Reference Manual

059920037-001 – Am94/1530 SCC/SBX Module

ORDERING INFORMATION

Part Number	Description
94/1530	Dual Channel Serial Communications Controller SBX Module (2.4576MHz)
Companion Products	
94/2000	SBX Motherboard
96/5232	Programmable RAM/EPROM and I/O Board
97/8605 Series	8086 Based 16-Bit Single Board Computers

Am94/1541

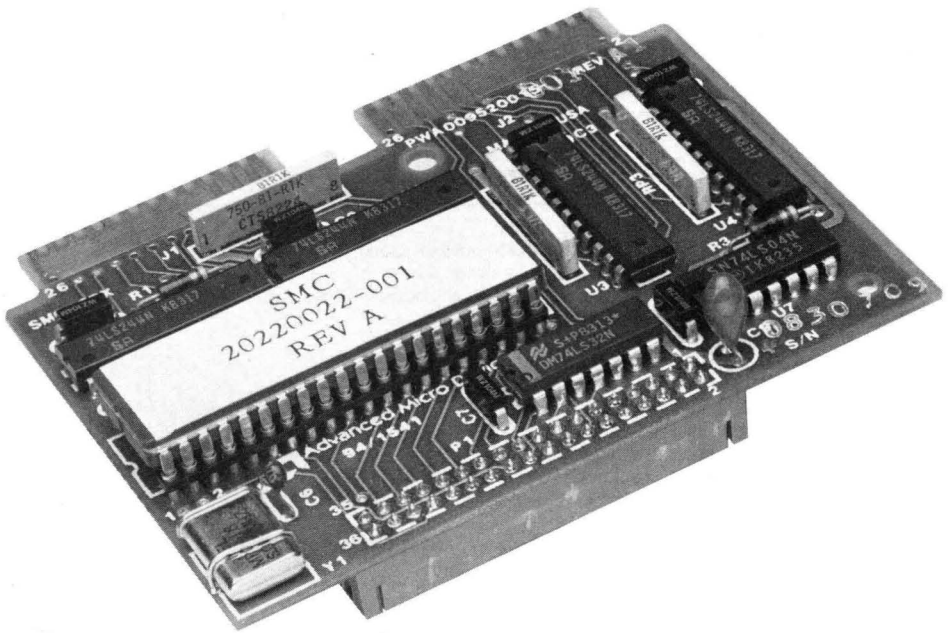
Stepper Motor Controller SBX Module

DISTINCTIVE CHARACTERISTICS

- Full control for one four-phase stepper motor
- 8-bit single-width SBX module
- Incorporates a powerful 8-bit microcontroller
- Simple user interface
- 15 lines of feedback from external sensor
- Line provided for external clock synchronization of multiple Am94/1541s
- 8 or 16 bits of precision
- Command or stored-program modes

GENERAL DESCRIPTION

The Am94/1541 is an SBX module providing complete control and feedback for one four-phase stepper motor. It incorporates a powerful microcontroller with a concise instruction set which offloads the host processor and simplifies programming. The Am94/1541 attaches to any host board which supports the Intel iSBX* bus, and offers a cost-effective means for adding motor control to a system.



*iSBX is a registered trademarks of Intel Corporation.

PRODUCT OVERVIEW

The Am94/1541 Stepper Motor Controller (SMC) is a powerful, programmable, single-width SBX module with capabilities heretofore existent only on full-size boards. Taking advantage of an 8-bit microcontroller chip, it has the ability to send out the appropriate signals to drive one four-phase stepper motor via either a stored program in the microcontroller or commands sent from the CPU board. A line is provided for an external clock to synchronize several Am94/1541s so that multiple stepper motors can be controlled synchronously. Also included on the module are buffered lines for external feedback from the device controlled by the Am94/1541.

The Am94/1541 provides a cost-effective approach to control one or more stepper motors. For example, up to six Am94/1541s can be mounted on the Am94/2000 SBX Motherboard (which provides six connectors to expand the SBX capability of a MULTIBUS* system) to provide control for up to six stepper motors in a two-slot space in the card cage.

FUNCTIONAL DESCRIPTION

The Am94/1541 Module contains a slave microcontroller programmed to fully control a four-phase stepper motor. It is designed to interact with a CPU board using an interrupt-based protocol which frees up the CPU for other activities. Table 1 shows the primary control capabilities of the module.

There are 15 external data feedback lines which are buffered and sent to the CPU board for processing. This creates a closed loop system ideal for high-performance applications.

The stepper motor drivers are off-board and are connected via a cable to the SBX module so that the motor can be remote from the system and control panels. This is a flexible configuration allowing a wide variety of motors and drivers to be used.

The problem of synchronizing multiple stepper motors driven by Am94/1541s is handled by providing an external clock signal which would be sent to each SBX module, thus providing smooth operation. Figure 1 shows the functional block diagram.

I/O Addressing

There are four I/O-addressable ports on the module:
- low order 8 bits of external feedback
- high order 7 bits of external feedback
- microcontroller data port
- microcontroller command port

These I/O ports are selectable by three SBX signals – MA0, MCS0/ and MCS1/. Port addresses are shown in Table 2.

Slave Microcontroller

The slave microcontroller is an 8-bit processor that responds to a set of 18 commands and 4 flow control instructions used to control a stepper motor. It contains six registers and two buffers. The registers are used to hold the data specifying the control and status information and the buffers are used to hold a stored program (if the stored-program mode is chosen) and the ramping pattern.

There are two modes of operation: stored-program mode and command mode. In stored-program mode, commands and data can be stored in the on-chip 11-byte buffer. This mode provides a method for executing a limited number of instructions repetitively without any CPU intervention. The primary use of this mode is for simple tasks requiring little feedback.

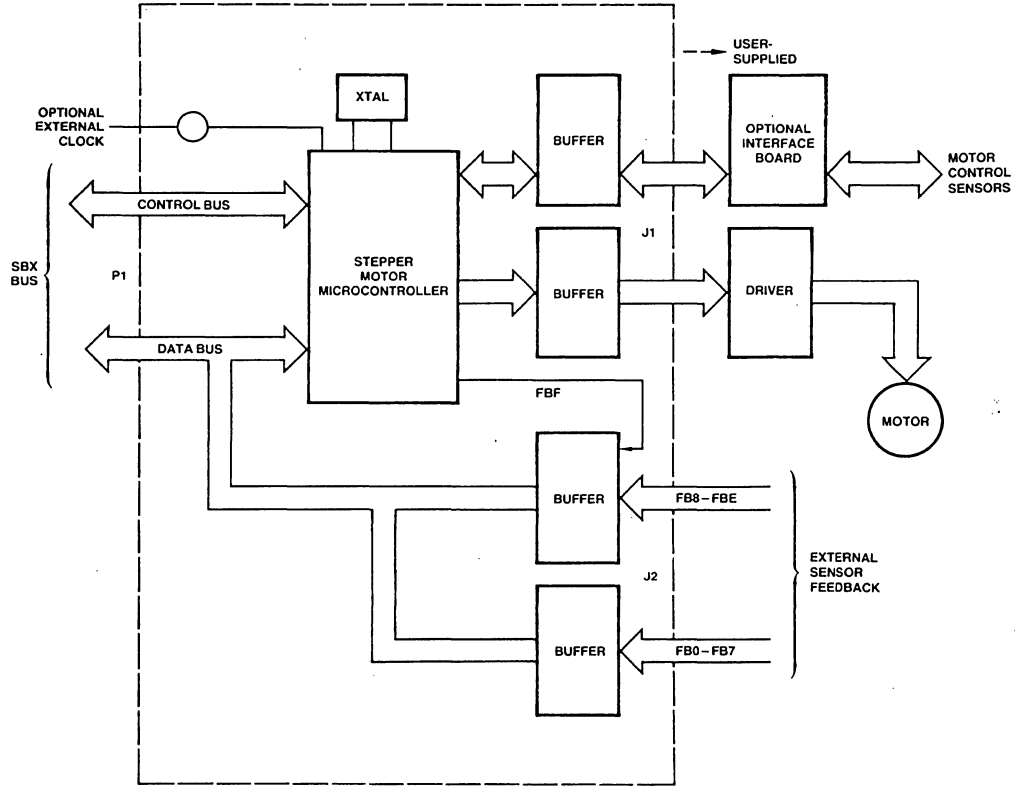
In command mode, each instruction sent to the Am94/1541 from the CPU is executed when received. This mode is primarily used for closed-loop systems, large programs and changeable environments where the CPU needs to intervene.

TABLE 1. Primary Control Capabilities

- Handles one four-phase stepper motor
- Supports acceleration/deceleration with variable speed ramp (user-definable)
- Ramping achieved by programming a set of buffers
- Decelerates automatically when it reaches the vicinity of the target position
- Operates in absolute or relative distance mode
- 8 or 16 bits of precision
- Maximum Speed: 4166 steps/sec with on-board clock
  8333 steps/sec with external clock
- Binary/BCD data processed
- Half step/full step capability
- Command mode or stored program mode
- Eighteen command and four flow-control instructions which make a powerful and complete set for programming the controller
- Two interrupt request outputs
- External clock for synchronized driving of several controllers simultaneously
- 15 bits of external feedback

*MULTIBUS is a registered trademarks of Intel Corporation.

Figure 1. Am94/1541 Stepper Motor Controller Block Diagram



Interrupt-Based Protocol

Two interrupts are available to enhance the speed of operation. One interrupt, MINTR0, notifies the host processor that the module needs information or wants to send information. The other interrupt, MINTR1, is used when an error has occurred. The use of interrupts allows the Am94/1541 to operate standalone, until further action is required by the host processor.

Installation

The Am94/1541 Module plugs directly into the female SBX connector on the host board. The module is then secured with a nylon post to firmly attach it to the host.

TABLE 2. I/O Port Addressing

MCS0/	MCS1/	MA0	Function
L	H	L	Microcontroller data
L	H	H	Microcontroller command
H	L	L	Feedback LOW (FB0–FB7)
H	L	H	Feedback HIGH (FB8–FBE)
L	L	X	Not allowed
H	H	X	Module not selected

H = HIGH
L = LOW
X = Don't Care

SPECIFICATIONS

Clock Frequency

6.0MHz

Word size

Data – 8 Bits

Access Times

Read – 250ns max.
Write – 300ns max.
Note: The above times are taken from the iSBX Bus Specifications, number 142686-002. Actual transfer speed is dependent upon the cycle time of the host microcomputer.

Interface Connectors

P1 SBX
- 36-pin, dual row, 0.1 in. centers

J1 Motor Interface
- 26-pin board edge, 0.1 in. centers (Mates with 3M 3462-0001 or equivalent)

J2 Feedback
- 26-pin board edge, 0.1 in. centers (Mates with 3M 3462-0001 or equivalent)

Interfaces

SBX Bus
- Meets the Intel iSBX bus specification

Motor Interface
- All signals TTL compatible

Signals Provided

Feedback (FB8–FBE)
Stop Motor (STOP/)
Home Position (XHOME/)
Motion Limits (NEGLIM and POSLIM)
Motion Direction (XDIR/)
Motor Power (POWER/)
Controller Direction (DIR/)
New Pattern (PHASECLK/)
Stop Acknowledge (STOPACK/)
Motor Phases (A/, B/, C/, and D/)

System Placement

Am94/1541 may be up to 100 feet away from driver

Drivers

The user must provide the driver circuitry to interface the Am94/1541 to the stepper motor. This circuitry, usually available from the motor manufacturer, must convert the Am94/1541 TTL signals to the drive signals required by the particular stepper motor being used. AMD recommends that the circuitry incorporate optical isolation for noise immunity.

Physical Characteristics

Width:	3.70 in. (9.40 cm.)	
Height:	2.85 in. (7.24 cm.)	
Thickness:	0.45 in. (1.15 cm.)	– Module only
	1.05 in. (2.65 cm.)	– Module and Host Board
Weight:	2.10 oz. (59 gr.)	
Shipping Weight:	1.00 lb. (454 gr.)	

Electrical Characteristics

DC Power Requirements
+5V ±5% at 485mA max.

Environmental Characteristics

Operating Temperature
- 0°C to 55°C (32°F to 130°F) with free moving air across the base board and the module

Operating Humidity
- To 90% without condensation

Reference Manual

059920048-001 – Am94/1541 SMC/SBX Module

ORDERING INFORMATION

Part Number	Description
94/1541	Stepper Motor Controller SBX Module
Companion Products	
94/2000	SBX Motherboard
96/5232	Programmable RAM/EPROM and I/O Board
97/8605 Series	8086-Based 16-Bit Single Board Computers

Am94/2000

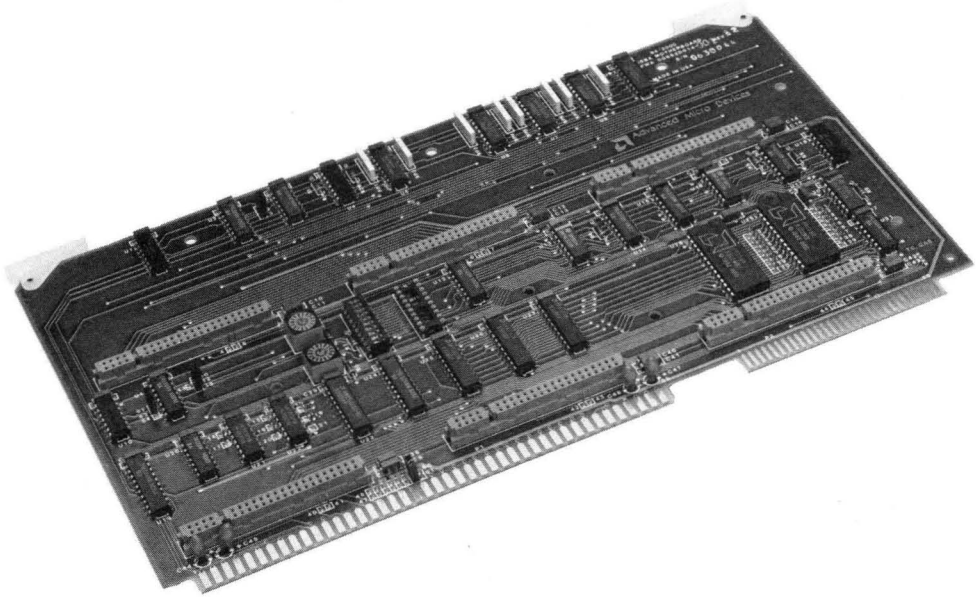
SBX Motherboard

DISTINCTIVE CHARACTERISTICS

- Six SBX connectors handle any 8 or 16-bit SBX module available; DMA is not supported
  - provides for up to six single-width modules, or
  - one double-width and four single-width modules, or
  - two double-width and two single-width modules
- Cost-effective – buy SBX modules to get the exact functions needed
- IEEE P796 compatible
- 8 or 16-bit I/O addressing
- MULTIBUS*-SBX bus timing reconciliation
- Two 8259A Programmable Interrupt Controllers

GENERAL DESCRIPTION

The Am94/2000 SBX Motherboard adds SBX capability to any MULTIBUS* system by providing support circuitry and connectors for the growing family of SBX modules. The Motherboard improves upon the concept of SBX modules by providing a cost-effective method for adding up to six specialized functions in a space otherwise occupied by two full size MULTIBUS boards.



*MULTIBUS is a registered trademark of Intel Corporation.

04279B

PRIDUCT OVERVIEW

The Am94/2000 SBX Motherboard is a MULTIBUS-compatible board which can add SBX capability to any MULTIBUS system. Six SBX connectors are provided to support single-width and double-width modules not requiring DMA. Am94/2000 features include MULTIBUS address decoding and data buffering, MULTIBUS-SBX timing reconciliation, and two interrupt controllers.

SBX modules can be a cost-effective approach to adding specialized functions to a MULTIBUS system. They tend to be lower cost than equivalent full-size MULTIBUS boards which may include functions not required in the system. However, SBX connectors generally exist only on some CPU and intelligent peripheral boards. Therefore, a system may have very few connectors, if any at all. The Am94/2000 solves that problem by providing a low-cost method for adding SBX capability. The Motherboard, plus SBX modules, can provide up to six functions in a two-slot space.

FUNCTIONAL DESCRIPTION

The Am94/2000 SBX Motherboard is a MULTIBUS slave board which has support circuitry to permit attached SBX modules to communicate with a bus master. The Motherboard processes the I/O addresses and has two 8259As Programmable Interrupt Controllers (PIC) for interrupt handling. The block diagram is shown in Figure 1.

Several I/O addresses are provided for each SBX module connected to the Am94/2000. These addresses not only select a module, but also provide the required SBX function and chip select signals—MA_0, MA_1, MA_2, CS_0, and CS_1. I/O addresses are also used to access the status registers and interrupt controllers on-board. The reserved I/O addresses are shown in Table 1.

The Motherboard can be configured for 8 or 16-bit I/O addresses. Eight-bit mode should be used only when the bus masters cannot generate 16-bit addresses. In 8-bit mode, the Am94/2000 can only accept 8-bit SBX modules, whereas in 16-bit mode, both 8 and 16-bit modules are accepted. In addition, 16-bit mode affords a much larger I/O address space.

Figure 1. Am94/2000 Block Diagram

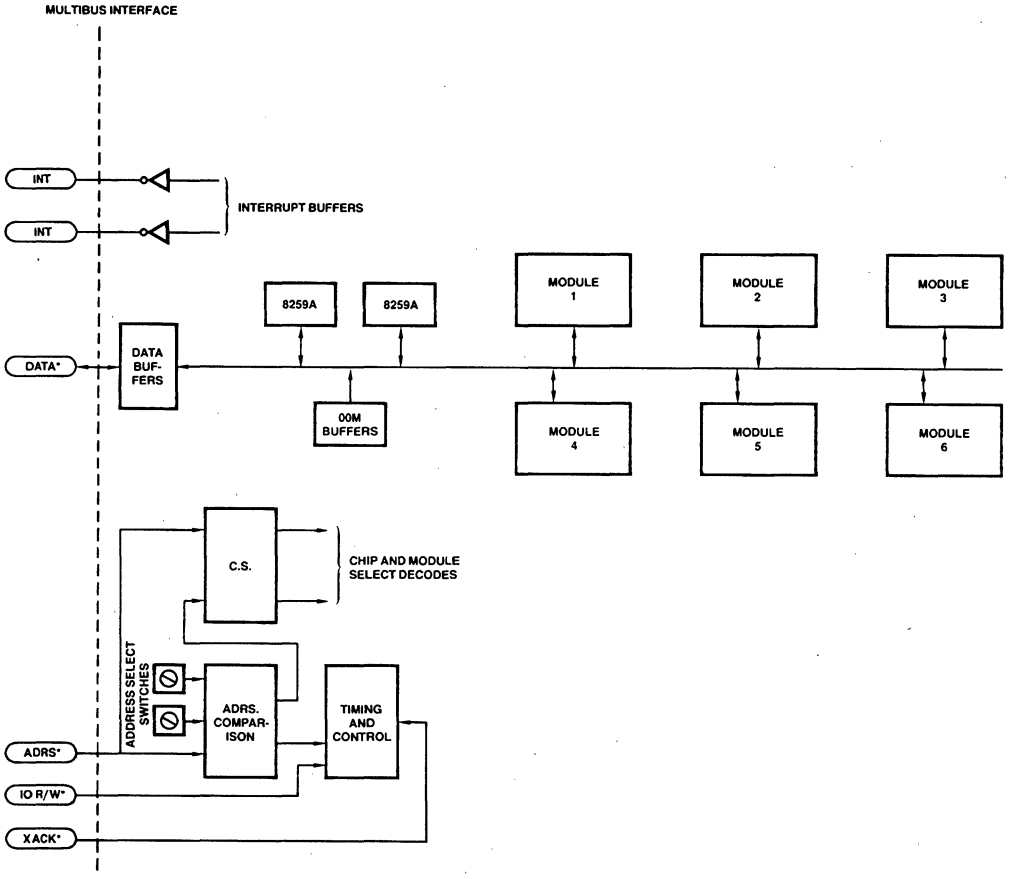


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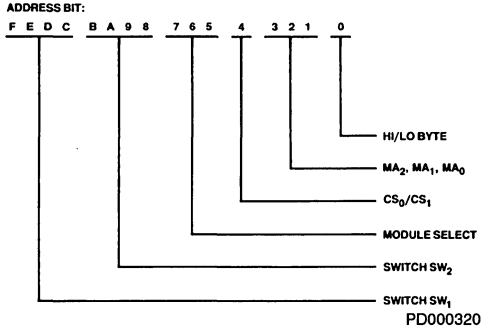
TABLE 1. Reserved I/O Addresses

16-Bit I/O		8-Bit I/O	
Addresses	**Selected**	**Addresses**	**Selected**
XX00-XX0F*	MODULE 1, CS_0	00-07	MODULE 1, CS_0
XX10-XX1F	MODULE 1, CS_1	08-0F	MODULE 1, CS_1
XX20-XX2F	MODULE 2, CS_0	10-17	MODULE 2, CS_0
XX30-XX3F	MODULE 2, CS_1	18-1F	MODULE 2, CS_1
XX40-XX4F	MODULE 3, CS_0	20-27	MODULE 3, CS_0
XX50-XX5F	MODULE 3, CS_1	28-2F	MODULE 3, CS_1
XX60-XX6F	MODULE 4, CS_0	30-37	MODULE 4, CS_0
XX70-XX7F	MODULE 4, CS_1	38-3F	MODULE 4, CS_1
XX80-XX8F	MODULE 5, CS_0	40-47	MODULE 5, CS_0
XX90-XX9F	MODULE 5, CS_1	48-4F	MODULE 5, CS_1
XXA0-XXAF	MODULE 6, CS_0	50-57	MODULE 6, CS_0
XXB0-XXBF	MODULE 6, CS_1	58-5F	MODULE 6, CS_1
XXC0-XXCF	FIRST 8259A	60-67	FIRST 8259A
XXD0-XXDF	SECOND 8259A	68-6F	SECOND 8259A
XXE0-XXEF	00M REGISTER	70-77	00M REGISTER
XXF0-XXFF	RESERVED	78-7F	RESERVED

*XX – Dialed into SW_1, SW_2 on Am94/2000

16-Bit Addressing

Two hexadecimal rotary switches are used to set the upper byte of all I/O addresses on the board for 16-bit address mode. (See the following diagram.)



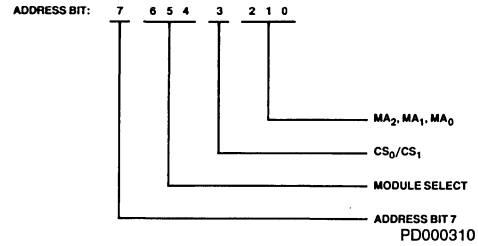
Address bit 0 is used to choose between the high and low byte of a 16-bit module. A jumper is provided to invert bit zero to provide for the requirements of the microprocessor.

CS_0/CS_1, MA_0, MA_1, MA_2 are sent to the SBX module and used as needed.

The Module Select bits are used to select the module, interrupt controller, or read-only status register assigned to each module.

8-Bit Addressing

In 8-bit mode, which should only be used when 16-bit addressing is not supported, the address bits are assigned as follows:



CS_0/CS_1, MA_0, MA_1, MA_2 are sent to the SBX module and used as needed.

The Module Select bits are used to select the module, interrupt controller, or read-only status register assigned to each module.

Address bit 7 is used to select the Motherboard, i.e., the Motherboard I/O space can be in the range 00-7FH or 80-FFH, which allows two Am94/2000s to exist in an 8-bit system. In 8-bit mode, the Motherboard does not respond to I/O addresses which would access unoccupied connectors. This allows these addresses to be used by otherI/O functions.

Read-Only Status Registers (00M Registers)

One register is available for each module on-board as a read-only status register. The register contains the MPST/bit ("one" indicates module present) and the two option bits of a module – OPT_0 and OPT_1. These registers are accessed by an I/O read.

Interrupts

Interrupts can be assigned to specific modules as required for maximum flexibility. Each SBX connector has two interrupt lines which can either be brought out directly to the MULTIBUS interrupt lines via buffers, or can be routed to one of the two 8259A PICs on the Motherboard for interrupt handling, including bus-vectored interrupts.

SPECIFICATIONS

I/O Addressing

The Am94/2000 Motherboard may be configured to occupy any 256-I/O port space in a 16-bit system or any 128-I/O port space in an 8-bit system. These spaces can be selected on 256 or 128 byte boundaries, respectively.

Interface Connectors

86-pin IEEE Standard P796 P1
Six each 44-pin SBX connectors

Environmental Characteristics

Operating Temperature
– 0 to 55°C (32 to 130°F) with free moving air across base board and module

Operating Humidity
– To 90% without condensation

Physical Characteristics

Width:	12.00 in.	(30.48 cm.)	
Height:	6.75 in.	(17.15 cm.)	
Thickness:	0.50 in.	(1.27 cm.)	Motherboard only
	1.10 in.	(2.79 cm.)	Motherboard and module
Weight:	10.20 oz.	(288 gr.)	

Electrical Characteristics

DC Power Requirements
+ 5V at 1A maximum plus module requirements
+ 12V as required by modules
– 12V as required by modules

Reference Manual

059920045-001 – Am94/2000 SBX Motherboard

ORDERING INFORMATION

Part Number	Description
94/2000	SBX Motherboard
Companion Products	
94/0350	Parallel I/O SBX Module
94/0351	Serial I/O SBX Module
94/1530	Dual Channel Serial Communications Controller SBX Module
94/1541	Stepper Motor Controller SBX Module

Am95/6120

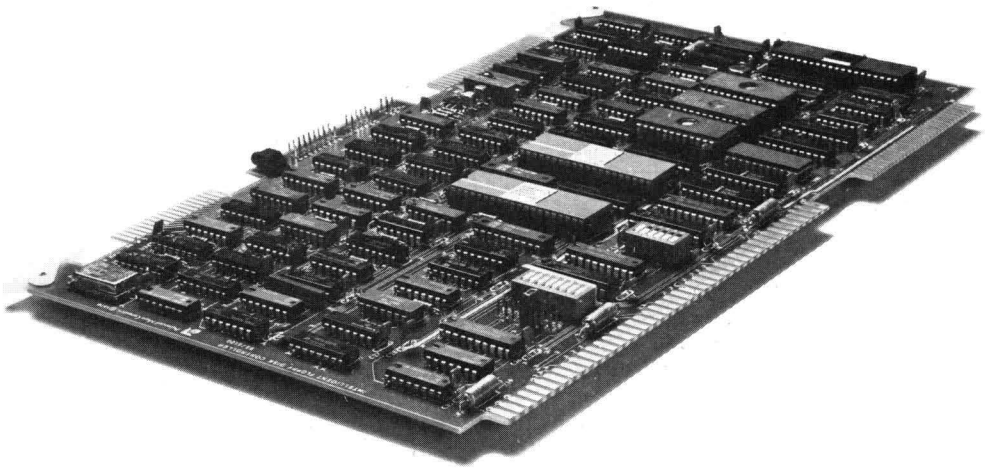
Intelligent Floppy Disk Controller Board

DISTINCTIVE CHARACTERISTICS

- Supports up to four 5¼ or 8-inch drives
- Intermixed single and dual-density plus single and double-sided drives managed by one controller
- Distributed I/O processor architecture
  - Performs all disk I/O without host CPU intervention
- Control firmware provides program code for read, write, execute and initialize, plus commands for error checks, status words and operation verification
- High throughput supports maximum disk read/write data rates. Provides high-speed DMA transfers (up to 1.8M bits/sec) in programmable block, burst, or byte mode
- 20-bit addressing handles transfers in a 1 megabyte address space
- Confidence check automatically provides a diagnostic check on start-up of RAM, ROM, FDC and DMA. Provides status word response to CPU. Visual LED fault indicator
- Automatic system boot capability on-disk

GENERAL DESCRIPTION

The Am95/6120 Intelligent Floppy Disk Controller is a high-speed system component interfacing and controlling up to four 8-in. or four 5¼-in. floppy disk drives. It supports both single and dual-density as well as single and double-sided drives intermixed in MULTIBUS-compatible systems.



*MULTIBUS and iSBC are registered trademarks of Intel Corporation.

05207A

PRODUCT OVERVIEW

The Am95/6120 Intelligent Floppy Disk Controller (IFDC) includes an 8085A Microprocessor, an FD1793 Floppy Disk Controller, 1K bytes of high-speed static RAM, a 9517A DMA Controller, 3K bytes of EPROM firmware and five interfacing mailbox registers. The functional diagram in Figure 1 shows the architecture of the board.

The 8085A CPU provides local processing power and, together with the intelligence of the on-board firmware, frees the host CPU while it concurrently processes all disk I/O transfers.

Under control of the MPU and on-board firmware, the FD1793 controller chip selects a particular disk drive, accesses a specific location on the disk, formats data and writes onto, or reads from the disk. Up to 64 disk sectors can be transferred with a single host command.

The Am95/6120 also offers such features as automatic head unloading (for longer diskette life), automatic track-seek-verify, automatic CRC generation and check, and write protection with verification. Phase-lock loop and write precompensation circuitry help ensure data reliability.

The 9517A DMA controller allows high-speed transfers at up to 1.8M bits/sec in block or programmable burst mode in combination with the 1K byte RAM buffer or in byte mode directly from the FD1793 controller. In byte mode, data is transferred directly between a disk drive and the host system, with a bus request necessary for each byte transfer.

Transfer rates of up to 225,000 bytes/sec are contingent upon system memory speed and interim bus requests and contention.

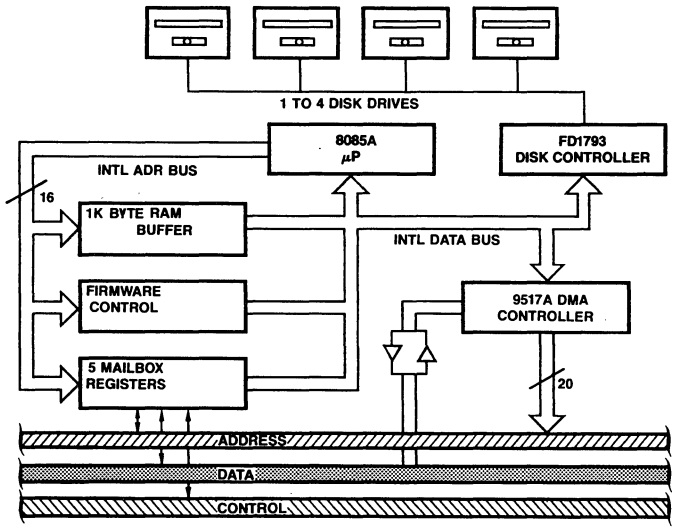
Command-level communications between the host CPU and the Am95/6120 take place through five mailbox registers (see Figures 1 and 2).

Block mode transfers a sector of information as a continuous data stream. A software-selectable burst mode can be employed with the amount of information in the burst transfer programmed in 16 or 64 byte increments. A rich set of status and verification commands and responses built into the firmware intelligently monitors system operations and allows recovery routines to be implemented. Operating errors such as mounting a disk that does not match the program code density designation are detected and reported.

The Am95/6120 can drive up to four 8-in. or four 5¼-in. floppy disk drives (single or dual-density as well as single or double-sided) from most manufacturers.

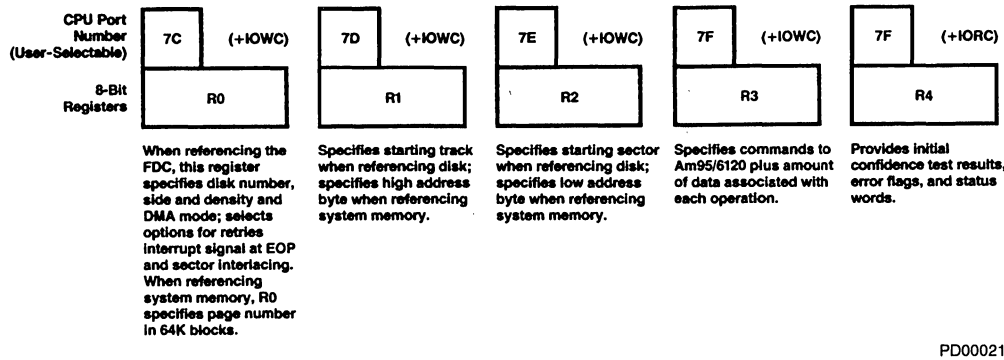
The Am95/6120 is compatible with the Intel iSBC/MULTIBUS bus standard. It can operate in a single master or Multimaster environment. It can generate one of eight jumper-selectable interrupts at the end of each operation.

Figure 1. Am95/6120 Functional Diagram



BD000961

Figure 2. Am95/6120-to-CPU Interface



PD000210

Firmware

The 3K EPROM-based firmware programs all the major disk operations. Once a command is initiated by the host CPU, the Am95/6120 IFDC operates under its control.

Factory-supplied firmware is present in EPROMs. The firmware receives host CPU commands through four ports and registers referred to as R0 through R3. Each operation is terminated by a return-of-status byte through a fifth register, R4, which indicates completion of the requested command. In the case of operational errors, R4 also stores appropriate error flags. The firmware initially performs a confidence test on the board ROM, RAM DMA and FD1793 when the reset signal is asserted on the system bus. An on-board LED fault indicator lights at the start of the confidence test and turns off if all four tests pass.

Following every command, a routine return-of-status is supplied by the Am95/6120 to the host CPU to verify operation. Additional detailed error checking is provided by commands Sense 1 and 2.

The factory-supplied firmware includes the command set shown in Table 1.

Automatic Boot From Disk

A jumperable option exists on the Am95/6120 to boot a system from code stored on-disk. When this option is exercised, code residing on track 0, sector 1, is read from disk and written into system RAM at location 00000H. The CPU must be in a "Not Ready" state (e.g., HOLD signal asserted). This can be accomplished by means of an on-board system-reset jumper. After the boot transfer to RAM memory, Am95/6120 firmware releases the HOLD to allow the CPU to begin fetching instructions at location 0.

Table 1. Am95/6120 Command Structure

Command	Description
Initialize disk	Diskette is automatically initialized to the specified soft-sector format without use of main memory.
Set parameters	Sets up the controller with unit code, track number, and sector number information. Unit code includes disk drive number, side number, type of density, number of retries, DMA transfer, interrupt, and interlace modes.
Read/Write	Read from, or write to, 1-64 consecutive or interlaced sectors, either directly or through the 1K byte on-board RAM buffer. Command is normally preceded by the Set Parameter command to designate the drive number and head position.
Execute	As an alternative to the Read/Write command, Execute transfers program code from system memory to the on-board 1K byte RAM and begins execution. This allows the user to write special programs (such as diagnostics) not implemented in firmware and store appropriate blocks of data on disk without mailbox interfacing. (With an appropriate DMA command routine, the Execute command can allow the board to function as a system DMA controller.)
Status	Returns miscellaneous status information on R4 such as operation completion, unit readiness, write protect.
Home	Positions the specified drive head over track zero.
Clear interrupt	Clears the interrupt latch set at the completion of a previous operation.
Sense 1 & 2	Provide status and verification information to the system CPU for error detection and correction. Data furnished provide system designers with the ability to implement intelligent error recovery routines.
Board reset	Reinitializes Am95/6120 hardware and firmware and invokes a confidence test of on-board RAM, ROM DMA and FDC.

Status Information

Sense 1 and Sense 2 commands provide status and verification information as feedback to the system CPU to monitor controller and drive operations. These commands allow intelligent recovery routines to be written.

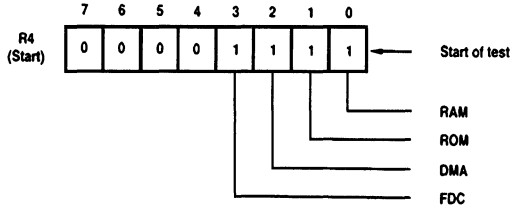
Sense 1 provides data on unit code (echo), drive number, density, side selected, and head loading, based on information in the drive select register. Track and sector number are also reported.

The Sense 2 command provides 12 bytes of information including the same information as Sense 1. The additional eight bytes provide information to the system CPU about the status of commands, utilities and primitives based on the operation of the FD1793 floppy disk controller chip.

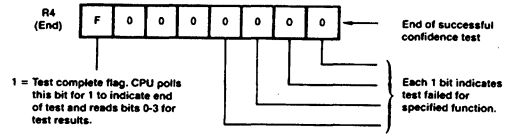
Data requested by the sense commands are placed in four (Sense 1) and twelve (Sense 2) contiguous bytes of system memory via the Am95/6120 DMA controller starting at the address specified in mailbox registers R0, R1 and R2.

Confidence Test

(On Init/Reset and Board Reset)

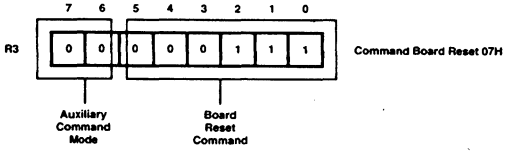


PD000170



PD000180

Board Reset

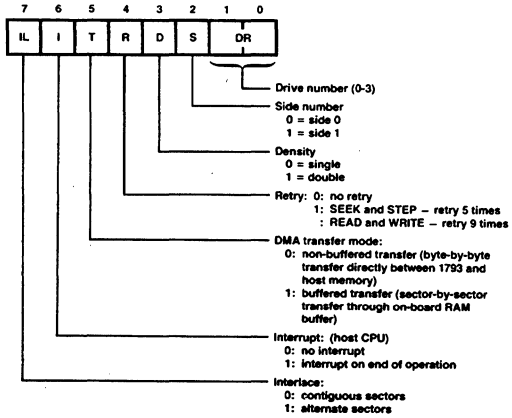


R4 Return of status: Complete confidence test is performed via R4 with format identical to the two-step operation as shown under CONFIDENCE TEST.

PD000190

Unit Code

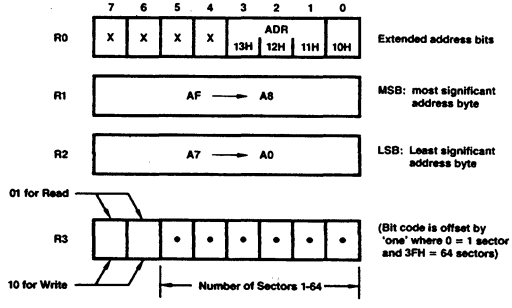
Register R0



PD000200

Read/Write Operations

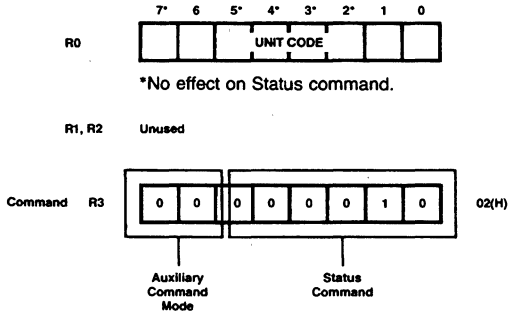
(Following a Set Parameters command)



R4 Return of status. See format under Set Parameters command.

PD000290

Status



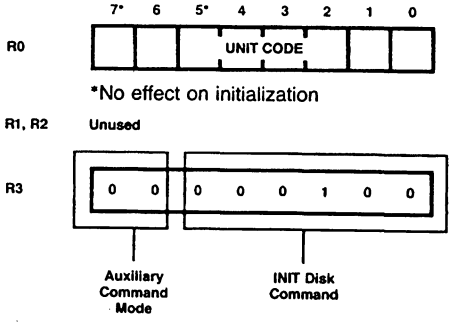
R4 Return of status. See format under Set Parameter command.

PD000270

Initialize Disk

(Under Auxiliary Command Mode)

Initializes diskette per IBM 3740, IBM System/34 8 inch format, or Shugart-type 5 ¼ inch format, soft sector, 128 bytes per sector, single-density or 256 bytes per sector, double-density, single- or double-sided, prior to system operation.

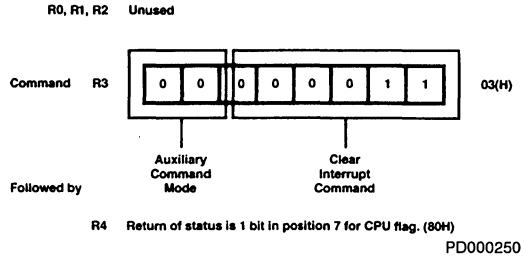


PD000300

Clear Interrupt

(Under Auxiliary Command Mode)

Clears interrupt set at the completion of a previous operation.

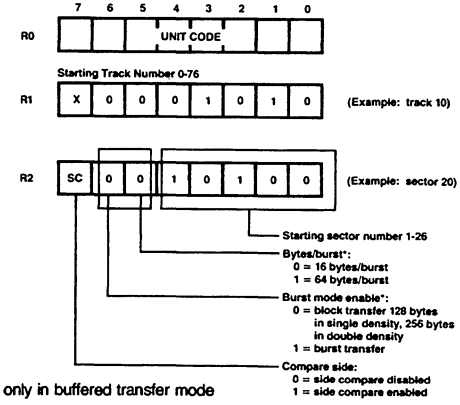


PD000250

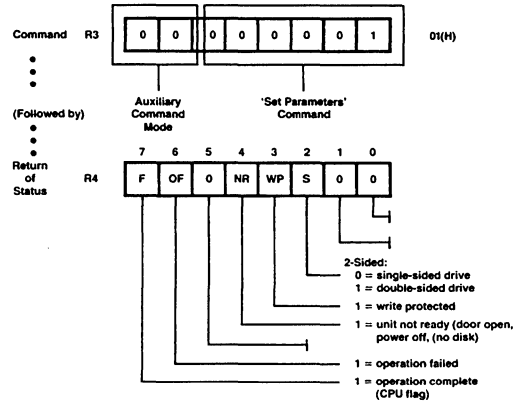
Set Parameters

(Under Auxiliary Command Mode)

Sets device address information for a subsequent read or write operation.



PD000240

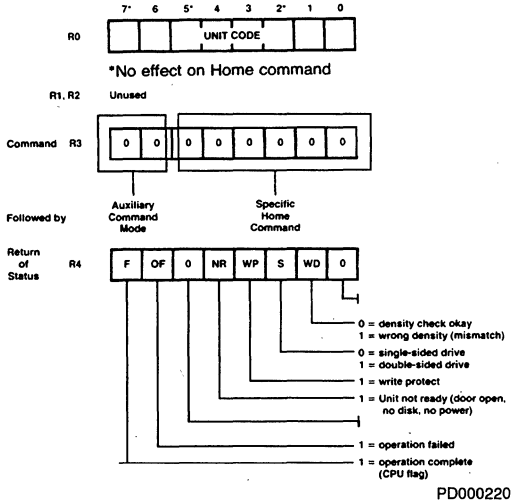


PD000260

Home

(Under Auxiliary Command Mode)

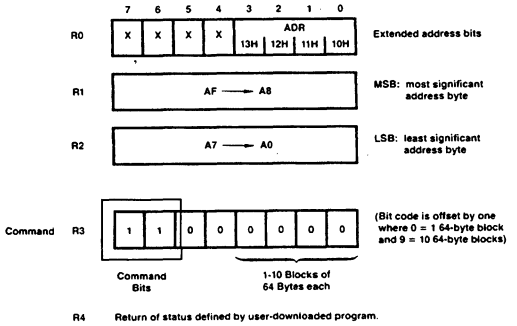
Positions specified disk read/write head over track 0. Automatically provides up to three retries when required.



PD000220

Special Execute

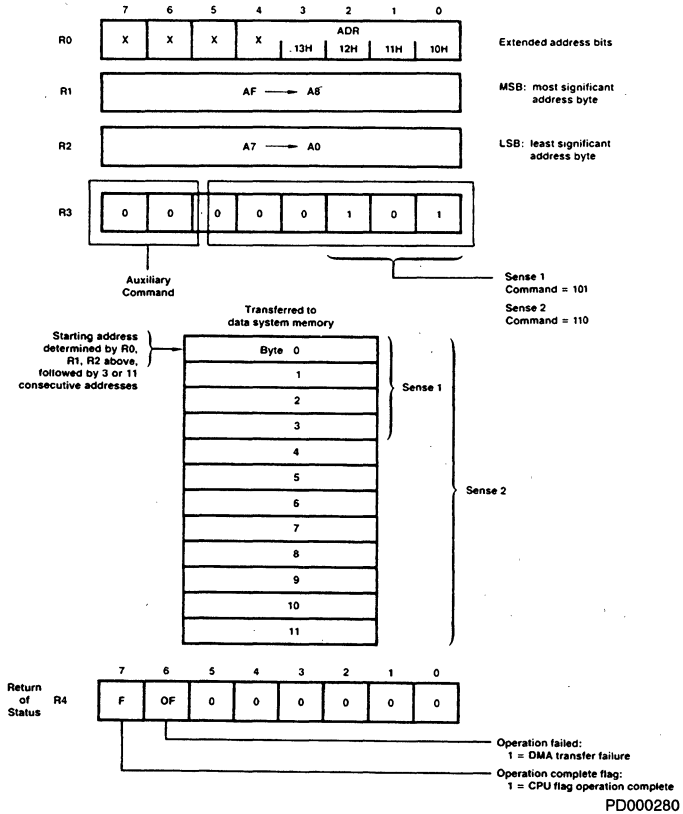
Downloads (via the Am95/6120 DMA controller) up to ten 64-byte blocks of program code from system memory, beginning at the address shown in R0-R2 to the on-board RAM and begins execution of the transferred code.



PD000230

Sense 1 and Sense 2

Status and verification command



PD000280

SPECIFICATIONS

Connectors

Interface	Number of Pins	Centers (in.)	Mating Connectors
MULTIBUS	86	0.156	CDC VPB01E43A00A1
8-in.	50	0.100	3M3415-0001 or TIH312125
5¼-in.	34	0.100	3M3463-0001

Media

Standard 8-in. floppy disks or 5¼-in. mini floppies.
One or two recording surfaces per floppy disk.

Characteristics	Single Density 8-in.	Double Density 8-in.
Media format	IBM 3740	IBM System/34
Tracks/surface	77	77
Sectors/track	26	26
Bytes/sector	128	256
Data/format	FM	MFM

Characteristics	Single Density 5¼-in.	Double Density 5¼-in.
Media format	Shugart-type	Shugart-type
Tracks/surface	35	35
Sectors/track	18	18
Bytes/sector	128	256
Data/format	FM	MFM

Computer Compatibility

iSBC-80, 8-bit or 16-bit with byte-mode operation

Direct Memory Access

Addresses up to 1 megabyte
1.8M bits/sec transfer rate

Physical Characteristics

Width:	12.00 in.	(17.15 cm.)
Height:	6.75 in.	(30.48 cm.)
Thickness:	0.62 in.	(1.57 cm.)
Weight:	2 lb.	

Electrical Characteristics

DC Power Requirements
+ 5V @ 1.65A typical 2.8A max.
+12V @ .11A typical 10.14A max.

Environmental Characteristics

Operating Temperature: 0°C to 55°C (operating); −55°C to +85°C (nonoperating)
Operating Humidity: up to 90% without condensation

Reference Manual

059901341-001 – Am95/6120 Intelligent Floppy Disk Controller Board

ORDERING INFORMATION

Part Number	Description
95/6120	Intelligent Floppy Disk Controller Board

Am95/6110 to Am95/6120 Upgrade

Application Note by Bruce Pettner
Microcomputer Systems Directorate

INTRODUCTION

The Am95/6120 Intelligent Floppy Disk Controller (IFDC) board can be used as a replacement for the Am95/6110 FDC design-ins with only minor modifications to the user software driver. The major differences are in the configuration of the STATUS BYTE and error processing.

On the Am95/6120 IFDC, the STATUS BYTE has been reconfigured to provide only status information. The error reporting function of the STATUS BYTE of the 6110 was redesigned to provide a less complicated decode. In addition, the 6120 provides a more detailed error reporting capability with the new SENSE commands. Below is a comparison of the STATUS BYTE configurations:

Am95/6110 STATUS BYTE		Am95/6120 STATUS BYTE	
BIT	STATUS	BIT	STATUS
0	Seek CDC Error	0	Unused (always 0)
1	Seek Error	1	Wrong Density
2	Lost Data / Write Fault	2	2 Sided Diskette
3	Read / Write CRC Error	3	Write Protect
4	Sector Not Found / 2 Sided	4	Unit Not Ready
5	Write Protect	5	Command Reject
6	Unit Not Ready	6	Operation Failed
7	Operation Complete	7	Operation Complete

As you can see by the above table, error reporting on the 6110 is handled right in the STATUS BYTE, whereas the 6120 gives you only failure status in bit 6. Notice also that the 6120 STATUS BYTE bits have one meaning and do not combine for a second decode meaning, as in the case of the 6110 bits 2 thru 4.

All but three of the original eleven 6110 commands have remained the same in the 6120 design. The three redefined commands are listed below:

05 SENSE1 – The functions performed by 05 (INTUNT), 06 (INTTRK) and 07 (INTSEC) commands on the 6110 are combined, on the 6120, into one command (SENSE1).

06 SENSE2 – Provides 12 bytes of status, the first four bytes of which are identical to that provided by SENSE1 and eight additional bytes of error reporting.

07 BDRESET – Performs a hardware reset on the 6120 board from the user's software driver.

The 6120 has the same eleven commands but with expanded capabilities.

Below is a table comparing the 6110 and 6120 commands:

	FDC COMMANDS		
		FUNCTION	
	Hex	6110	6120
	00	HOME	HOME
	01	SETPAR	SETPAR
	02	STATUS	STATUS
	03	CLRINT	CLRINT
	04	INIDSK	INIDSK
*	05	INTUNT	SENSE1
*	06	INTTRK	SENSE2
*	07	INTSEC	BDRESET
	08	UNUSED	UNUSED
	.	.	.
	.	.	.
	.	.	.
	3F	UNUSED	UNUSED
	4X	READ	READ
	8X	WRITE	WRITE
	CX	EXECUTE	EXECUTE

* Commands that have changed

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In most 6120 operations, if STATUS BYTE bit 6 is set then an error has occurred and the reason for the failure is found by performing an 06 (SENSE2) command and decoding the data bytes passed to the host memory. See the Am95/6120 Users Manual for details on commands and syntax.

Other minor changes, but worthy of noting, are found in UNIT CODE and SECTOR SELECT CODE formats.

UNIT CODE			
6110		6120	
BIT	**FUNCTION**	**BIT**	**FUNCTION**
0	Drive Select	0	Drive Select
1	Drive Select	1	Drive Select
2	Side Select	2	Side Select
3	Unused (always 0)	3	Density Select
4	Retries	4	Retries
5	Transfer MODE	5	Transfer MODE
6	Interrupt	6	Interrupt
7	Interlace	7	Interlace

Bit 3 of the 6120 UNIT CODE specifies single or double density disk format. This bit should always be set to zero for 6110 drivers and will not present a problem unless the driver does not set it to zero or the user plans to use double density.

SECTOR CODE			
6110		6120	
BIT	**FUNCTION**	**BIT**	**FUNCTION**
0	Sector address	0	Sector address
1	" "	1	" "
2	" "	2	" "
3	" "	3	" "
4	" "	4	" "
5	Unused	5	Bytes per burst
6	Unused	6	Burst mode enable
7	Unused	7	Side compare

The 6120 will not support multi-sector, buffered reads or writes on disks with contiguous sector formats. The 6110 was capable of supporting this type of operation.

The above capsulizes the areas of change when converting from the 6110 IFDC to the 6120 IFDC. There are other functions are which you may choose to consider as part of converting, such as supporting double density. Therefore, it is recommended that the user read the Am95/6120 IFDC User's Manual before attempting the conversion.

Users who have designed-in the Am95/6110 IFDC can modify their existing driver code and upgrade to the Am95/6120 IFDC and avoid obsolescence. The extent of the software changes would be limited to the routine or routines that handle STATUS BYTE processing, the removal of routines that use the INTUNT, INTTRK and INTSEC functions and the addition of routines to take advantage of the new functions SENSE1, SENSE2 and BDRESET. It is left to the user to decide how best to use the functionality of the 6120 command set.

Am96/6130

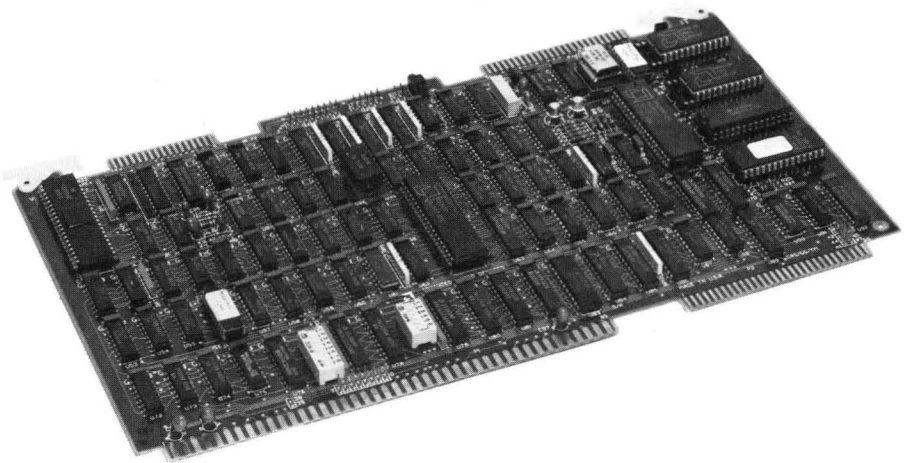
Intelligent Floppy Disk Controller Board
ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Supports up to four 5¼ and four 8 inch drives concurrently
  - 3 ½ inch drives that support the 5¼ inch interface are also supported
- Distributed I/O processor architecture
  - Performs all disk I/O without host CPU intervention
- Simple user interface
  - High-level commands sent through mailbox registers
- Meets IEEE P796 specifications for MULTIBUS*
- High throughput
  - Supports maximum disk read/write data rates. Provides high-speed DMA transfers (up to 1.8M bits/sec) in programmable block, burst, or byte mode
  - Full track buffering capability
- 24-bit addressing for a 16 megabyte address space
- Automatic system boot capability on disk
- Am95/6120 emulation mode

GENERAL DESCRIPTION

The Am96/6130 is an Intelligent Floppy Disk Controller that is an upgrade of our popular Am95/6120 FDC. It can handle up to four 5¼ inch and four 8 inch drives concurrently, supporting both single and dual-density, as well as, single and double-sided drives in intermixed systems. Optional full-track buffering means the highest performance floppy disk controller in the industry.



*MULTIBUS is a registered trademark of Intel Corporation.

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- **Formats supported**

Characteristics	Single Density 8-in.	Double Density 8-in.
Media format	IBM 3740	IBM System/34
Tracks/surface	77	77
Track density (TPI)	48	48
Sectors/track	26	26
Bytes/sector	128	256
Data/format	FM	MFM

Characteristics	Single Density 5¼-in.	Double Density 5¼-in.
Media format	Shugart-Type	Shugart-Type
Tracks/surface	35 – 80	35 – 80
Track density (TPI)	48 – 96	48 – 96
Sectors/track	16/18 – 16/18	16/18 – 16/18
Bytes/sector	128 – 128	256 – 256
Data/format	FM – FM	MFM – MFM

Am96/5232

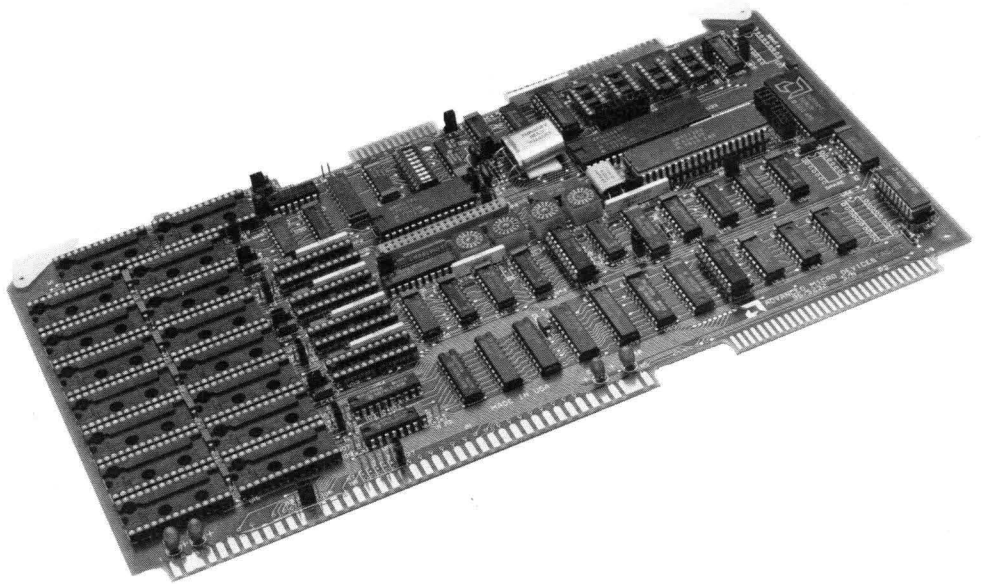
Programmable RAM/EPROM and I/O Board

DISTINCTIVE CHARACTERISTICS

- Sixteen 28-pin sockets support all 24/28-pin JEDEC standard memory devices up to 16K x 8
  - Provides for 256K bytes of ROM/EPROM, or
  - 128K bytes of static RAM, or
  - 32K bytes of EEPROM (2816A-compatible), or
  - A combination of supported devices
- Support for 8 and 16-bit CPUs
- 20 or 24-bit memory addressing for a 16 Megabyte addressing range
- Memory mapping via PALs* provides for easy custom configuration
- 8 or 16-bit I/O addressing
- Counter/timer with five programmable timers for interrupt and baud rate generation
- Programmable interrupt controller
- SBX connector supports 8-bit SBX modules

GENERAL DESCRIPTION

The Am96/5232 is a versatile MULTIBUS**-compatible board which performs two distinct functions: memory and I/O expansion. The memory section provides sockets for up to 256K bytes of EPROM, or 128K bytes of static RAM, or some combination of supported devices. The I/O portion includes one serial port, a parallel interface with 24 lines, counter/timers, programmable interrupt controller, and an SBX connector permitting customized I/O.



*PAL is a registered trademark of and used under license from Monolithic Memories, Inc.
**MULTIBUS is a registered trademark of Intel Corporation.

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PRODUCT OVERVIEW

The Am96/5232 board is a versatile, multi-function MULTIBUS-compatible board that extends the memory and I/O capabilities of a system. The primary use of the Am96/5232 is as a companion board in ROM-based applications where complete systems can be created by coupling the Am96/5232 with a CPU board. The extensive memory space is capable of holding large dedicated applications and systems' software in EPROM, as well as providing RAM working storage to run the applications. The board can support 8 and 16-bit microprocessors by providing 20 and 24-bit addressing, 8 and 16-bit memory data, and 8 and 16-bit I/O addresses. Figure 1 shows the Functional Block Diagram.

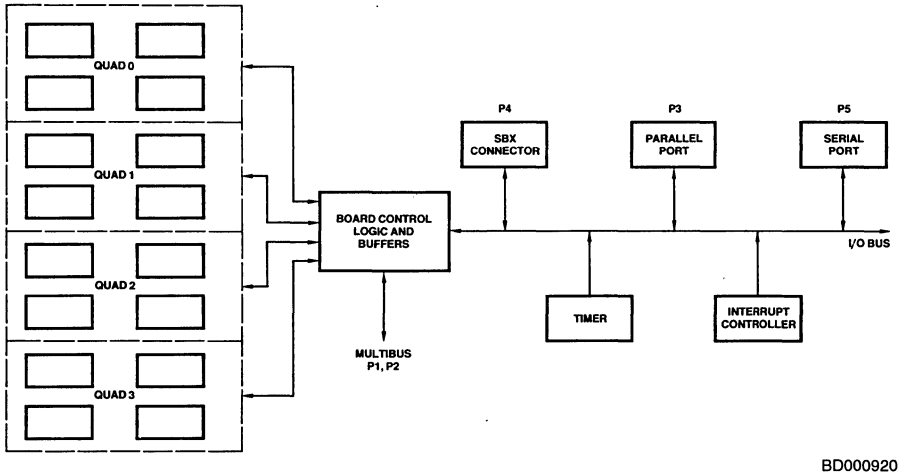
The memory section consists of sixteen 28-pin sockets configured in four quads. These sockets can support any 24/28-pin JEDEC standard memory device to provide a maximum capacity of 256K bytes using 16K x 8 EPROMs, or 128K bytes using 8K x 8 static RAMs. All sockets in a quad must contain devices of the same memory size, although they may be different devices (see Table 1 for examples of memory devices supported). Each quad is independent and can reside anywhere in a 16 Megabyte address range with the only restrictions being that all memory on-board must reside within the same megabyte space and quad addresses cannot overlap. A memory mapping PAL is associated with each quad and is easily programmed to configure that quad's memory addressing. The board can take advantage of high-speed memories by providing jumpers to make the acknowledgment signal (XACK/) adjustable.

The I/O section has several capabilities: one serial port, twenty-four lines of programmable parallel I/O, and an SBX connector which will support any 8-bit SBX module that does not require DMA. A counter/timer can be used to generate interrupts for the system and a programmable baud rate for the serial port. A programmable interrupt controller is provided for interrupt servicing flexibility.

TABLE 1. Example OF Am96/5232 Memory Devices Supported

Device Type	AMD Part #	Generic Part #	Per Quad Capacity	Total Board Capacity
2K x 8 EPROM	2716	2716	8K Bytes	32K Bytes
2K x 8 EEPROM	N/A	2816A	8K Bytes	32K Bytes
2K x 8 Static RAM	9128	6116	8K Bytes	32K Bytes
4K x 8 EPROM	2732	2732	16K Bytes	64K Bytes
8K x 8 EPROM	2764	2764	32K Bytes	128K Bytes
8K x 8 Static RAM	N/A	6264	32K Bytes	128K Bytes
16K x 8 EPROM	27128	27128	64K Bytes	256K Bytes

Figure 1. Am96/5232 Functional Block Diagram



Memory Functional Description

Memory Quad Configuration

Memory is divided into four quads, each consisting of four 28-pin sockets and a memory decoder PAL. The quads can be considered separate entities for memory layout flexibility, except that board address restrictions require all memory on-board occupy the same megabyte, and that quad addresses cannot overlap. Each quad can be enabled or disabled by writing to a 4-bit register. Quad addresses must begin on a boundary that is a multiple of the quad capacity for a given device. Figure 2 shows the layout of a quad.

The sixteen sockets have 28 pins and will support any 24 or 28-pin JEDEC standard memory device type. Jumpers are provided to connect the appropriate signals for a given device and the decoder PALs are programmed for the size of the devices placed in the quad. Table 1 lists example devices and corresponding capacity.

Quad addressing information is programmed into the memory decoding PAL and has been made very simple for the board. AMD provides a source listing of the BASIC program used in generating the PALs. Device size and beginning address are the only items necessary to enter into the program which then generates a file suitable as input to PAL24. The decoder PALs monitor the appropriate signals and generate Chip Select(s) to the four memory devices in each quad. The PALs also generate a Quad Enable which tells the board control logic that the quad recognizes the current address.

Power-On Quad Enable

A jumper-selectable option allows the board to be configured so that the first memory quad (Quad 0) is enabled upon board reset. By selecting this option, memory stored on the Am96/5232 can be read without executing instructions to enable the quad. In this way, system initialization code and data can be stored on the Am96/5232.

Memory Addressing

The Am96/5232 supports 20 and 24-bit addressing selectable by jumper, thus providing a maximum range of 16 Megabytes. If the 24-bit option is chosen, all of the board memory must occupy the same megabyte which is set by a 16-position rotary switch corresponding to the high order four address bits.

The board can be configured for 8/16-bit memory data or 8-bit only memory data modes. In the 8/16-bit mode, word and byte operations are permitted. Consecutive addresses are stored side-by-side in chip pairs with a quad, thus address bit 0 is stripped off so both the even and odd byte can be accessed for a word operation. Address bit 0 is decoded for byte operations to access the correct device.

In the 8-bit-only mode, all of the low order address bits go to the memory chips, thus allowing consecutive addresses to be located in the same device.

Memory Device Speed Configuration

The Am96/5232 supports adjustable memory timing by providing an adjustable XACK/, as measured from the memory read or write signal, to take advantage of higher speed memory devices. Three choices for response time are available: 350ns, 450ns, and 550ns (all ± 50ns). All quads use the same XACK/ configuration, so the response time must be based on the slowest device on the board. Table 2 shows the device speeds supported by the different response times.

Figure 2. Block Diagram of One Quad

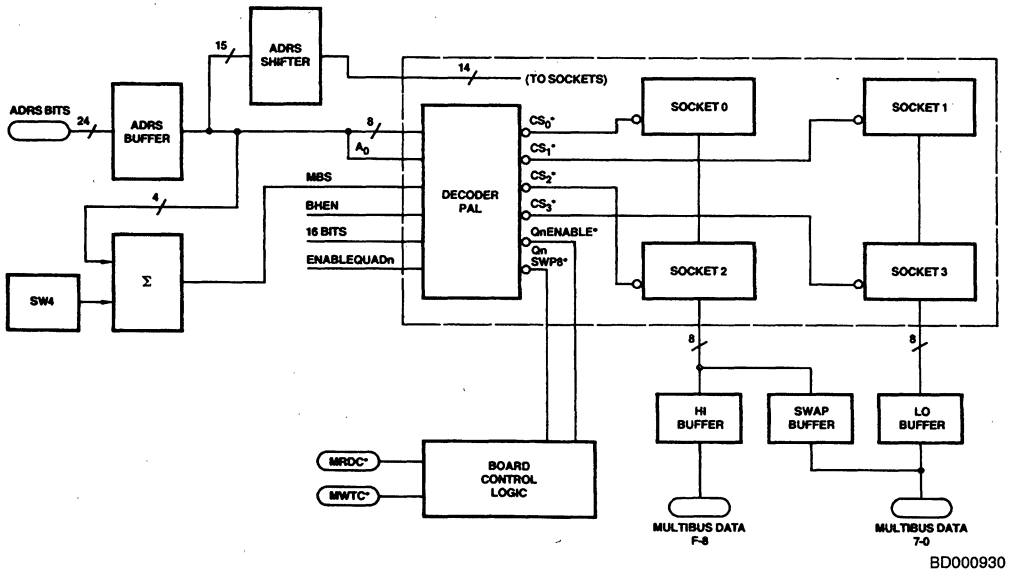


Figure 3. Block Diagram of I/O Section

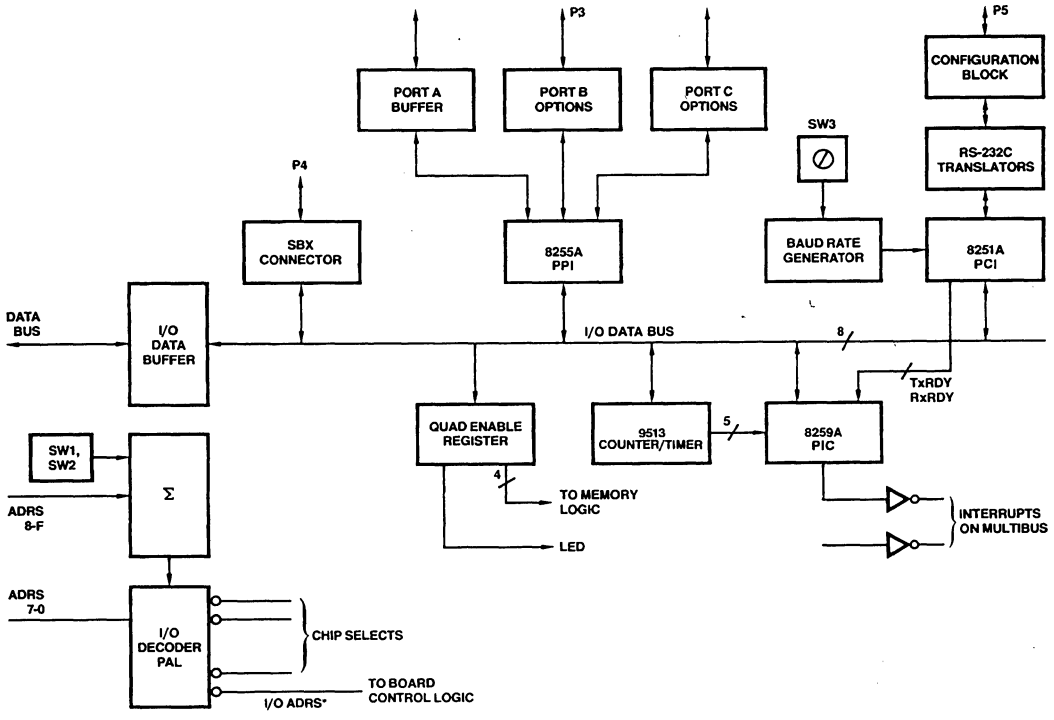


TABLE 2. Adjustable XACK/Timing

Slowest Device Speed*	Command ↓ to XACK ↓ (± 50ns)
⩽300ns	350ns
⩽400ns	450ns
⩽500ns	550ns

*Note – Device speed measured as:

EPROMs/ROMs: slower of T_{ACC} or T_{CE}

RAMs: slower of read cycle or write cycle where:

- read is slower of T_{ACC} and T_{CE}
- write is T_{WP} + 100ns

Inhibit Signals

The Am96/5232 can be configured to generate the INH1/ or INH2/ inhibit MULTIBUS signals to prevent other boards from responding to the memory address on the system address bus. Similarly, the INH1/ and the INH2/ signals from the system bus can prevent the Am96/5232 from responding to the memory address on the system address bus.

I/O Functional Description

The following subsections describe the I/O functions of the board (see Figure 3 for Block Diagram).

Serial I/O

The 8251A Programmable Communications Interface (PCI) on the Am96/5232 provides the system with an additional RS-232C interface. Transmit and Receive baud rates can be individually selected from any of three sources: hardware baud rate, generated on-board and switch selectable up to 9600 baud; programmable baud rate, generated on-board by the 9513 counter/timer and software-programmable up to 19200 baud; and external baud (or bit) clock, sent over the serial interface from the other end of the link. A configuration block makes it easy for the user to connect the on-board 8251A signals to the appropriate RS-232C signals to set up the proper mode, such as "data terminal" or "data set."

Parallel I/O

The Am96/5232 provides twenty-four lines of buffered or unbuffered parallel I/O controlled by a programmable 8255A Programmable Peripheral Interface (PPI). The twenty-four lines are divided into three 8-bit ports: one port that can be

input, output or bidirectional; one port that can be input or output; and the third port, which can be further subdivided into two 4-bit ports, each of which can be input or output. A set of buffers and sockets are provided for interchangeable I/O line drivers and terminators to take advantage of a large number of possible configurations.

Counter/Timer Controller

The 9513 System Timing Controller chip is a high-speed programmable device intended for generating signals. Five timers are provided to generate interrupts. One timer can be used to provide the programmable baud rate signal for the serial I/O.

Interrupt Handling

Interrupts can be configured by directly buffering the interrupt requests onto the backplane or they can be routed through the 8259A Programmable Interrupt Controller (PIC). The programmable interrupt controller is preferred since it uses fewer MULTIBUS interrupt lines and allows programmable interrupt schemes such as bus-vectored interrupts.

SBX Connector

An SBX connector provides additional flexibility to the Am96/5232. All 8-bit SBX modules that do not require DMA are supported. Many different I/O functions are available on modules permitting customization of the system.

I/O Addressing

The Am96/5232 supports both 8 and 16-bit I/O addressing. In 16-bit mode, all addresses on board are within the same 256-bit page which is established by two rotary hexadecimal switches. Table 3 shows the I/O addresses as the board is configured. The low order address byte can be changed by rewriting the appropriate equations and making a new I/O decoder PAL.

TABLE 3. I/O Addresses

I/O Function	Address
Memory Quad Enable/LED Register	XXD0
Miscellaneous Read Register	XXD0
Parallel Port A	XXD4
Parallel Port B	XXD5
Parallel Port C	XXD6
Parallel Port Control	XXD7
Timer Data	XXD8
Timer Control	XXDA
Serial Data	XXDC
Serial Control	XXDD
Interrupt Controller Low	XXDE
Interrupt Controller High	XXDF
SBX Connector CS0	XXE0-XXE7
SBX Connector CS1	XXE8-XXEF

(Note: For 16-bit addressing, 'XX' means the value dialed into the two switches; for 8-bit addressing, 'XX' means "don't care")

SPECIFICATIONS

Memory Capacity

Up to 256K bytes of ROM/EPROM using 16K x 8 devices, or up to 128K bytes of static RAM using 8K x 8 devices, or up to 32K bytes of EEPROM using 2K x 8 devices

Note: Memory sizes and types can be mixed in groups of four

Memory Addressing

20-bit memory addressing, or
24-bit memory addressing where all the memory must occupy the same megabyte area (i.e., high order 4 bits must be the same)

I/O Addressing

16-bit I/O addresses or 8-bit I/O addresses

Serial Interface

EIA Standard RS-232C signals provided and supported:

Transmit Timing	(DTE)
Transmit Timing	(DCE)
Request to Send	
Clear to Send	
Carrier Detect*	
Ring Indicator*	
Data Terminal Ready*	
Data Set Ready	
Transmit Data	
Receive Data	
Signal Ground	
Protective Ground	

Serial Baud Rates

Switch-selectable up to 9600 baud, Programmable up to 19200 baud, or External

Parallel Interface

One 8-bit input, output, or bidirectional port
Two 8-bit input or output ports
– one of which can be subdivided into two 4-bit ports

Counter/Timer Function

Five programmable timers, each of which can be jumpered to generate interrupts; one of those being able to be jumpered for use as baud rate generator

Interrupt Function

8259A Programmable Interrupt Controller supports bus-vectored interrupts; functions can be jumpered to MULTIBUS interrupts (up to six), if desired

SBX Connector

8-bit data only; DMA controls are not supported
Single and Double-width modules supported

Interface Connectors

P1 MULTIBUS CONNECTOR
P2 MULTIBUS Extension Connector
P3 Parallel Port Connector
P4 SBX Connector
P5 Serial Port Connector

Physical Characteristics

Width:	12.00 in.	(30.48 cm.)	
Height:	6.75 in.	(17.15 cm.)	
Thickness:	0.50 in.	(1.27 cm.)	without module
	1.10 in.	(2.79 cm.)	with module
Weight:	0.780 lbs.	(0.35 kg.)	

Electrical Characteristics

DC Power Requirements
+5V at 1A max.
+12V at 25mA max.
−12V at 25mA max.

Note: For Basic board, as delivered. To calculate overall maximum power requirements, include all memory chips on-board and SBX module (if used).

Environmental Characteristics

Operating Temperature: 0°C to 55°C
Operating Humidity: To 90% without condensation

Reference Manual

059920039-001 – Am96/5232 Programmable RAM/EPROM and I/O Board

*mutually exclusive

ORDERING INFORMATION

Part Number	Description
96/5232	Programmable RAM/EPROM and I/O Board
Companion Products	
94/0350	Parallel I/O SBX Module
94/0351	Serial I/O SBX Module
94/1530	Dual-Channel Serial Communications Controller SBX Module
94/1541	Stepper Motor Controller SBX Module

USING EEPROMS ON Am96/5232

Application Note by Tom Crawford
Microcomputer Systems Directorate

INTRODUCTION

This profile discusses the installation and programming of X2816A Electrically Erasable PROMS (EEPROMS) on the Am96/5232 Programmable RAM/EPROM and I/O Board.

X2816A EEPROMs, from XICOR Inc., have been successfully installed and programmed on the Am96/5232. The X2816A (not to be confused with the Intel 2816) is a 5 Volt only 2K x 8 device with pinouts identical to 2K x 8 static RAMs (e.g., Am9128).

For read access, the X2816A will behave similarly to the 9128. When CE is LOW (with WE HIGH and OE LOW), the device will access the data at the specified address and place it on the I/O pins.

Writing data is similar to writing data into a static RAM. A LOW on WE (with OE HIGH and CE LOW) initiates a write cycle. The address is latched on the falling edge of CE or WE (WE in the case of the 5232) and data is latched on the rising edge of CE or WE (WE in the case of the 5232). Once the write cycle is initiated, it will automatically continue to completion inside the EEPROM within 10 msec. During this period the EEPROM is busy, but the buses are available for other uses.

Am96/5232 Jumpering and X2816A Installation

The Am96/5232 is jumpered as described in the User's Manual (Publication Document Number 059920039-001) in the Memory Quad Device Type Configuration section. Pin 26 of the X2816A socket is jumpered to VCC and pin 23 of the socket is jumpered to MEMWT. This is the same jumpering as specified for 2K x 8 static RAMs and the parts can be mixed in a quad, if desired.

Use a C2KxxPAL* decoder where xx are the high order two hex digits of the base address in a 1 megabyte address space.

The X2816A comes in three read access speed versions, as indicated below. If the X2816A is the slowest memory device on the board, jumper the memory access time of the 96/5232 as indicated in the table.

XICOR PART	$t_{CE} = t_{AA}$	t_{WP}	LONGEST TIME	5232 JUMPER
X2816A	300	150	300	86-to-87
X2816A-35	350	150	350	89-to-87
X2816A-45	450	150	450	88-to-87

The X2816As are installed by plugging them into the appropriate sockets; 24-pin devices are installed in the RIGHT-HAND twenty-four pins of 28-pin sockets on the Am96/5232.

Timing the Write Recovery

The X2816A has a nominal write recovery time of 10 μsec. During this time another write cycle must not be initiated. The easiest way of timing this is to simply enter a program loop which will last 10 msec.

The following code segment illustrates this technique for a 6MHz Z8002,** assuming no wait states for instruction fetches. This is a subroutine which writes one byte, delays 10 msec. and recovers the byte which was written. The data to write is in RL3 and the address is in R2. The data recovered is returned in RH3. If the Zero flag is set on return, the byte was successfully written. No register other than RH3 is changed.

```
WEEPROM:
   PUSHL     R15@,RR4          ;%SAVE A COUPLE OF REGISTERS
   PUSHL     R15@,RR6          ;%AND A COUPLE MORE
   LD        R6,741            ;%ITERATION COUNT
   LDB       R2@,RL2           ;%INITIATE THE WRITE CYCLE
WEEPROML:
   MULT      RR4,R6            ;%70 CYCLES
   DJNZ      R6,WEEPROML       ;%11 CYCLES
%
%741 TIME 81 CYCLES AT 6 CYCLES/MSEC = 10,004 MSEC
%
   POPL      RR6,R15@          ;%RESTORE EVERYTHING
   POPL      RR4,R15@          ;
   LDB       RH3,R2@           ;%READ THE DATA BACK
   CPB       RH3,RL3           ;%SET ZERO FLAG IF OK
   RET                         ;%AND EXIT
```

*PAL is a registered trademark of andis used under license from Monolithic Memories, Inc.
**Z8002 is a trademark of Zilog Corporation.

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An alternate method is to start one of the timers on the Am96/5232 (at say, 1KHz) which generates an interrupt, which in turn increments a counter. Then the wait loop can wait for the counter to increment the appropriate number of times.

Power On/Off Problems

There is a potential problem with non-volatile memories, in that the control terms have to be carefully controlled when power is being cycled in the system. If CE and WE both go LOW before VCC goes LOW (during power off), or if VCC goes HIGH before both CE and WE (during power on), an undesired write cycle could be initiated.

The best method for protecting X2816As on the Am96/5232 against undesired write cycles during power on/off sequences is to insure that no CE is generated.

CE is made in the memory decoder PAL devices and includes addresses and the QUAD enable term (which is active HIGH and comes from a programmable register on the board). So long as the enable term is LOW, the decoder PAL cannot generate CE (what happens is: CE follows VCC up and down very closely).

During power-on, INIT/ on the backplane resets the register containing the QUAD enable terms so that the board comes up with all four QUAD enable terms LOW. If the X2816As are in the first QUAD, it is necessary to remove the jumper at 12-13 to insure that the QUAD enable term is suppressed.

During power-off, the program must insure that the Quad containing the X2816As is not enabled. This could be done during a power-fail interrupt routine.

X2864A

The X2864A is an 8K x 8 EEPROM (analogous to the 5564, etc.). To use this part, the board is jumpered as for an 8K x 8 RAM and the PAL decoder is C8Kxx. The X2864A has not been physically tried on the Am96/5232 as of yet, but parts are on order.

The X2864A has a feature called DATA Polling. During a write cycle, an attempted read of the last byte written results in the data complement of that byte. After completion of the write cycle, true data is available. This is intended to be used to determine when a write cycle has completed, thus eliminating the full 10 msec. wait. One could start the write cycle and merely wait for the data to become correct.

BIBLIOGRAPHY:

Am96/5232 Programmable RAM/EPROM and I/O Board User's Manual, Pub. Document Number 059920039-001

X2816A 2K x 8-Bit Electrically Erasable PROM Data Sheet, Xicor Stock Number 200-012

X2864A 8K x 8-Bit Electrically Erasable PROM Data Sheet, Xicor Stock Number 200-021

5-Volt-Only EE-PROM Mimics Static RAM Timing, *Electronics* - June 10, 1982

Am96/3500

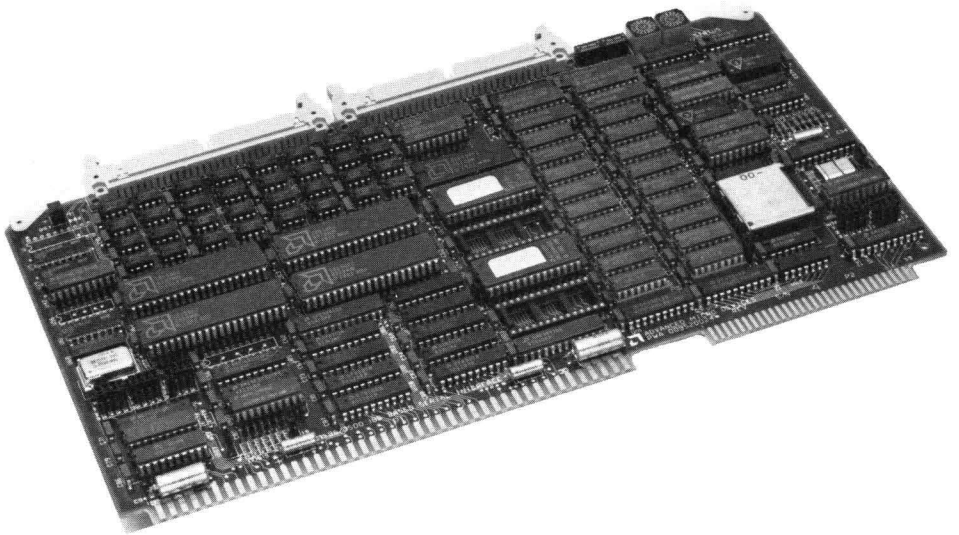
Intelligent Serial Interface Board
ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Eight independently programmable channels based on the Z8530* with multifunction support for serial communications protocols including:
  - Asynchronous
  - Bit-oriented synchronous (SDLC/HDLC)
  - Byte-oriented synchronous (Bisync)
- RS-232C and RS-423 supported on-board
- Software-selectable data rates to 38.4K baud async and 612.5K bits/second sync
  - Independent for each channel
- On-board 16-bit 80186 CPU provides high-performance operation
- Two-channel DMA controller provides:
  - One high-speed, full-duplex DMA channel using one of the serial ports
  - High-speed DMA transfer between system memory and on-board memory
- Three uncommitted versatile timers
- Full multimaster capability
- 128K zero-wait-state RAM with parity
  - Upper 64K can optionally be dual-ported

GENERAL DESCRIPTION

The Am96/3500 Intelligent Serial Interface (ISI) board is an intelligent, eight channel, multiprotocol serial communications controller. It provides high performance, flexible and diverse serial I/O for MULTIBUS**-compatible systems. Capable of operation as a slave controller or bus master, it relieves the system CPU and software of the overhead normally associated with serial I/O service and allows operations at much higher data rates than otherwise possible.



*Z8530 is a registered trademark of Zilog, Inc.
**MULTIBUS is a registered trademark of Intel Corporation.

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PRODUCT OVERVIEW

The Am96/3500 ISI board is a powerful eight-channel serial communications controller board with complete MULTIBUS/ Multimaster capability. Making use of the latest VLSI components, the board is capable of handling a tremendous amount of serial I/O without host CPU intervention. This provides for extremely high throughput and improves performance of a MULTIBUS system.

The Am96/3500 contains an 80186 16-bit microprocessor, four Z8530 Serial Communications Controllers (SCC), an 8259A Programmable Interrupt Controller (PIC), sockets for 128K of EPROM, 128K of parity RAM (of which 64K is dual ported), and provisions for on-board diagnostics.

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The heart of the Am96/3500 ISI is a 16-bit 80186 microprocessor. The 80186 is a highly integrated microprocessor incorporating an enhanced 8086 CPU and many support circuits. These include clock generator, two independent DMA channels, programmable interrupt controller, three timers, and chip-select logic. With 80186 controlling operations, the Am96/3500 is able to operate eight serial channels at extremely high data rates and with minimal intervention from the host CPU board.

Serial Communications Controllers

There are four Z8530 SCCs on the Intelligent Serial Interface board. Each SCC contains two independent communications channels complete with Baud Rate Generator, Digital Phase-Locked Loop, CRC insertion and checking.

The SCCs can be programmed to handle all asynchronous formats regardless of data size, number of stop bits, or parity requirements. They can also be configured to support synchronous byte-oriented protocols such as Bisync and synchronous bit-oriented protocols such as HDLC and SDLC.

Within each operating mode, the SCC allows for protocol variations by checking odd or even parity, CRC generation and checking, break generation and detections, and many other protocol-dependent features.

On-Board Memory

The Am96/3500 ISI contains 128K bytes of parity RAM accessible with zero wait states by the 80186 microprocessor. The upper 64K may be optionally jumpered to be accessible by the MULTIBUS. If dual-ported, the 64K may be mapped into any portion of the 16 megabyte address space of the MULTIBUS on any 64K boundary.

Direct Memory Access

The 80186 DMA controller provides two high-speed DMA channels which may be used to transfer data between on-board memory and system memory. The DMA also supports data transfers between memory and I/O, and I/O-to-I/O anywhere in the system. Either bytes or words can be transferred with a maximum data rate of 2 megabytes/second.

One of the serial channels can make use of the two DMA channels for receive and transmit, respectively, to transfer data at a high rate of speed at full duplex.

Printer Port

One Centronics-compatible parallel printer port is provided.

Versatile Timers

Three uncommitted versatile timers are provided by the 80186. The hardware hooks are present to use one of them as a MULTIBUS-timeout timer. A second timer could be used to generate 60Hz interrupts for character-delay timing.

Firmware

Four EPROM sockets on-board provide for a maximum capacity of 128K bytes of firmware. AMD offers optional firmware to handle various communications configurations.

Serial Interface Configuration

The Am96/3500 ISI uses two 60-pin locking-right-angle headers for increased reliability. Ribbon cables are used to connect the board directly to the customer's equipment, or the cables can run to a breakout panel.

Interrupt Capability

All SCCs support vectored interrupts which eliminates the need for software polling and increases the speed of the interrupt service routine (one of the most time-critical portions of the system).

MULTIBUS communications can be done with interrupts. An interrupt is provided for both directions so that the MULTIBUS can signal the Am96/3500 ISI with a CHANNEL ATTENTION interrupt and in turn, the Am96/3500 can generate a STATUS interrupt on the MULTIBUS.

All interrupts are vectored. These include PRINTER DATA READY and PRINTER STATUS NOT READY.

Am96/8052

Intelligent Color Video Controller Board
ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Am8052 CRT Controller chip provides:
  - Displays up to 4500 characters (each with its foreground/background color)
  - Flicker-free soft scrolling
  - Split screens
  - Multiple window display
- Character attributes include:
  - Eight foreground colors
  - Eight background colors
  - Blink
  - Superscript
  - Subscript
- Up to 32K bytes of EPROM
- Meets IEEE P796 specifications
- 128K bytes of zero wait state dynamic RAM
  - Storage for up to seven screens of character and attribute data
  - Storage for downloaded procedures
- Z8002* CPU provides on-board intelligence
  - Execute terminal emulator
  - Execute procedures downloaded from host or on-board firmware
  - Controls on-board serial port for a keyboard
  - Extensive self-test and error reporting capability
- Options include:
  - ANSI-standard terminal emulator firmware
  - Bit-map overlay of 384 scan lines by 1024 pixels
  - 2K bytes of EEPROM for setup information

GENERAL DESCRIPTION

The Am96/8052 is a high-performance, intelligent, color CRT controller board which adds a flexible and powerful means of adding video to a MULTIBUS** system. Up to 4500 characters, each with its own attributes, can be displayed. In addition, the color of each character, as well as its background, can be programmed. Other features of the board include flicker-free soft scrolling, split screens, and multiple windows. On-board intelligence provides the means to make the board a terminal emulator and to relieve the host of the burden of controlling the peripheral device. Several options are available to tailor the board for specific requirements including ANSI terminal emulator firmware and bit-mapped graphics overlay.

*Z8002 is a registered trademark of Zilog, Inc.
**MULTIBUS is a registered trademark of Intel Corporation.

05197A

Am95/6440, 6448, 6450, 6452A

Card Cages and System Chassis

DISTINCTIVE CHARACTERISTICS

Am95/6440 and Am95/6448 Card Cages

- All metal construction
- Available with (Am95/6448) and without (Am95/6440) integrated switching power supply

Am95/6450 and Am95/6452A System Chassis

- 19-in. rack mounted
- Six-board (Am95/6450) or 14-board (Am95/6452A) capacity
- Front access panel for easy board installation, removal and inspection
- Power, reset and interrupt switches
- Cooling fans
- Rear connector panel and cable routing channel

GENERAL DESCRIPTION

Advanced Micro Devices offers high-quality, all metal construction Card Cages and System Chassis. The card cages come with six slots with or without cooling fans and power supplies. The chassis are 19″ rack-mountable with six and fourteen board capacities.

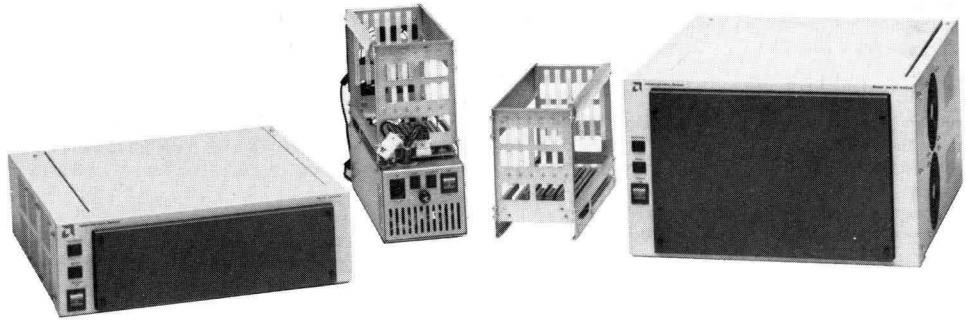

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Figure 1. Am95/6440 Standard Card Cage

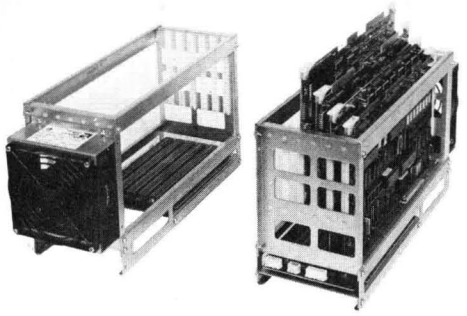
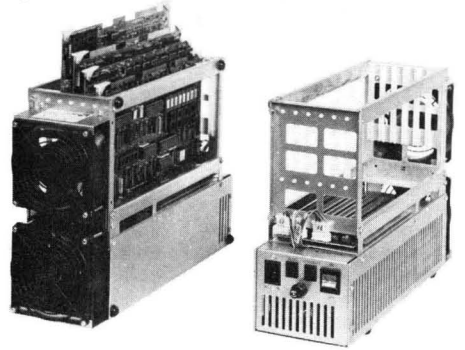


Figure 2. Am95/6448 Card Cage with Power Supply



Am95/6440 STANDARD CARD CAGE PRODUCT OVERVIEW

The Am95/6440 Standard Card Cage consists of a six-slot MULTIBUS*-compatible backplane mounted in a rigid metal enclosure. Also included are three power supply connectors, guides to accommodate six MULTIBUS-compatible printed circuit boards and MULTIBUS-compatible signal terminators.

Figure 1 shows the card cage with optional fan installed. The cooling fan, mounted to blow air into the card cage, can be reinstalled to function as an exhaust fan.

Optional expansion interconnectors are available for cascading up to three cages together.

Expansion Capability

The connectors along the edges of the backplane are used in conjunction with the expansion interconnection option (Am95/6445) to extend Am95/6440 card cages for additional PC board capacity. The expansion option includes a double-sided edge connector and hardware for fastening the extended card cages together to form a single rigid unit. When standard card cages are extended, terminators should be removed from all cages but one. Up to three Am95/6440 cages (18 slots total) can be joined without exceeding bus specifications.

Power Connection

Power is connected to the Am95/6440 card cage via the three backplane connectors shown in Table 1. When card cages are expanded, power is supplied to each via the three power connectors. Heavy-duty power connectors on the backplane permit currents as high as 25A to be applied. Plated connections at the edge of the backplane can handle up to 5A per individual circuit.

Auxiliary Connectors (P2 Bus Area)

The Am95/6440 allows users to mount (bolt) wire-wrap connectors at location J2 to extend the bus or to interface external signals to printed circuit boards (refer to Table 1).

Am95/6448 CARD CAGE WITH POWER SUPPLY

PRODUCT OVERVIEW

The Am95/6448 Card Cage is similar to the Am95/6440 except that it contains a high-efficiency switching-type power supply. It furnishes ±5 and ±12VDC (regulated) MULTIBUS voltage requirements. The power supply module, MULTIBUS backplane, input panel, cooling fans, and metal frame are integrated into a compact trim design for use in industrial chassis and for benchtop use (see Figure 2).

The regulated outputs from the power supply are wired to the corresponding backplane lines through connectors at the edge of the backplane (see Table 1). The power supply module contains secondary regulators to improve load regulation.

The input panel contains an IEC recessed AC receptacle with EMI filter, power switch with indicator light, fuse holder, reset switch and interrupt control switch. The reset switch outputs an active 'Initialize' signal (pin 14) to provide a system reset to memory location zero. The interrupt switch is wired to INT7 (restrappable) to generate a programmable interrupt with capability to alter the course of program execution by software control.

AC input to the unit is internally strappable for either 110VAC or 220VAC operation. For 110VAC operation, specify Am95/6448; for 220VAC, Am95/6448/100. The assembly is designed to meet Underwriter's Laboratories specification UL478.

TABLE 1. Am95/6440 AND Am95/6448 Power Connectors

Power/Gnd. Backplane Connector	Pin Voltage	Max. Current	Mating Connector Housing†
3-circuit	1–12V 2+ 12V Ret. 3+ 12V	9A 9A	AMP-1-480303-0
2-circuit	1–5V 2–5V Ret.	9A	AMP-1-480318-0
4-circuit	1+ 5V 2+ 5V Ret. 3+ 5V Ret. 4+ 5V	 	 25A 25A

†Contacts for specified socket housings are AMP-60617-5.

*MULTIBUS is a registered trademark of Intel Corporation.

Figure 3. Am95/6450 System Chassis

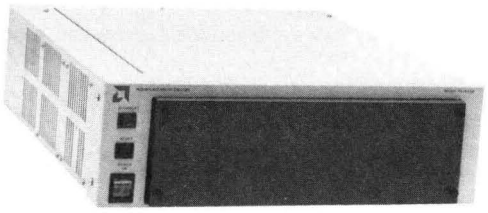
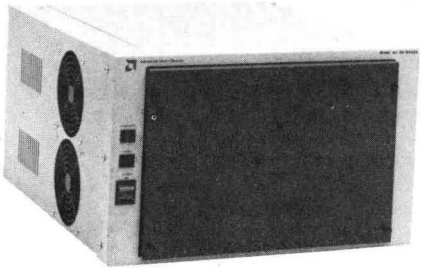


Figure 4. Am95/6452A System Chassis



Am95/6450 AND Am95/6452A SYSTEM CHASSIS

PRODUCT OVERVIEW

Both the Am95/6450 and the Am95/6452A System Chassis incorporate a MULTIBUS-based card cage and switching power supply into an EIA rack-mountable metal enclosure. Most features of these units are identical except for board capacity: the larger size of the Am95/6452A accommodates up to 14 horizontally mounted printed circuit boards, while the Am95/6450 accommodates six boards. A detailed comparison is included in Table 2.

Front Panel

Each system chassis has a large front panel access plate held in place with four self-retained quick release fasteners. Removal of the front plate provides access to the printed circuit boards for installation, removal, and inspection.

The rocker-type power switch has an indicator light for on-off status. Pushing the reset switch reinitializes the system and begins programmed operation at address 0000. Pushing the interrupt switch asserts a signal on one of the bus interrupt lines (INT0-INT7) to invoke a software routine that can jump the operating program to a preselected memory address. As delivered, the interrupt switch is connected to INT7, but the signal line can be strapped to any interrupt line on the backplane to suit specific applications.

Board Edge Cables

Signals from the input/output edge connectors on the printed circuit boards are sent via ribbon cables to connectors mounted on the rear panel of the enclosure. A cable channel is provided between the top board and the chassis housing. Two quick-lock fasteners remove the 14-in. wide top panel for easy cable routing.

Rear Panel

The rear panel includes vertical brackets to mount interfacing connectors. The bracket spacings accommodate 25-pin, 50-pin, and D-type connectors to provide a flexible and convenient means to connect external equipment to the system within the enclosure.

The rear panel houses a combination AC power receptacle, voltage selector, and fuse holder. A heavy-duty line cord plugs into the 3-prong receptacle to provide AC power. The user determines the primary AC operating voltage by inserting a small printed circuit board into a slot under the fuse holder. Depending on the orientation of the board in the slot, it selects one of four voltages: 100, 110, 220, or 240VAC. The main power line fuse, safety-interlocked with the line cord, can be reached from the rear of the unit.

Two 2-circuit connectors are also located on the rear panel. One provides +5VDC from the internal power supply to power auxiliary devices such as LED displays or test instruments. The other connector accepts a TTL-compatible input signal to turn the enclosure's power supply on and off via a relay mounted inside the unit. With this arrangement, power for the entire system within the enclosure can be controlled remotely.

Power

Both units contain switching-type power supplies that accept AC power and provide regulated DC outputs to conform to MULTIBUS voltage requirements. See Table 2. The Am95/6450 contains one power supply and the Am95/6452A contains two supplies. Refer to the specification section for detailed power supply information.

TABLE 2. Comparison of Features

Part Number	Slots	Slot Spacing	Input Voltage	Fans	Height	Width	Depth	Weight	Rack Mounting Hardware
Am95/6440	6	0.7-in.	–	–	8.0-in.	5.1-in.	13.2-in.	4lb	–
Am95/6440/100	6	0.7-in.	–	1	8.0-in.	5.1-in.	14.7-in.	4lb	–
Am95/6448	6	0.7-in.	110/220	2	11.8-in.	5.2-in.	16.1-in.	11lb	–
Am95/6450	6	0.625-in.	100/110 220/240	2	5.25-in.	17.0-in.	19.25-in.	22lb	slide mounts
Am95/6452A	14	0.625-in.	100/110 220/240	4	10.5-in.	17.0-in.	19.25-on.	31lb	slide mounts

SPECIFICATIONS

Power Supply

AC Input

Nominal – 115/230VAC, field selectable, 47 to 440Hz
Operating range – 90–132 to 180–264VAC

DC Output

+5V @ 25 Amps max.

±12V@ 4 Amps max.
–5V @ 4 Amps max.
The total output available is 150 watts. Thus, 5V @ 25 Amps will only leave a total of 25 watts divided among the other 3 outputs

Adjustments
– All fully regulated output voltages are adjustable ±5%

Line Regulation
– ±0.2% over an input range of 90–132/180–264VAC when operating with 100% of rated load

Load Regulation
– Measured while the load on a given output is varied from 20% to 100% of maximum output current. Auxiliaries need 10% load on main output

Ripple and Noise
– Any output; 0.5% max.; RMS ripple; typically 1.0% p-p

Over Voltage Protection

Main output – Both crowbar OVP and inverter shutdown OVP
Auxiliary output – OVP on all outputs

Reverse Voltage Protection

Semi regulated – Protected to rated current
Fully regulated – Main output protected to rated current. All other is protected to 1 Amp continuously or full rated current momentarily

Power Fail

A TTL-compatible logic signal is available

Logic Inhibit

A logic inhibit input can be used to turn off DC outputs

Reference Manuals

059901281-001 – Am95/6440 Standard Card Cage
00680135 – Am95/6448 Card Cage with Power Supply
00680144 – Am95/6450 System Chassis
059910706-001 – Am95/6452A System Chassis

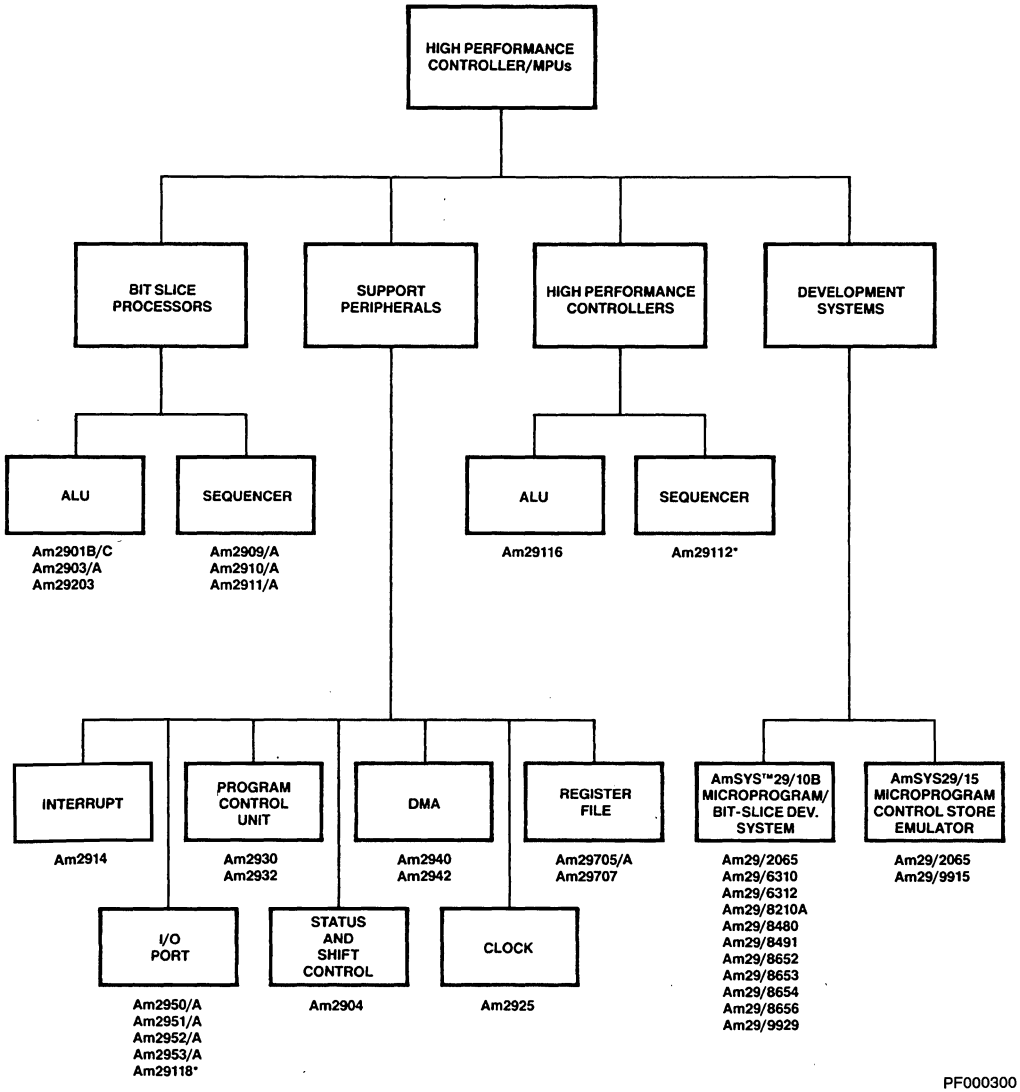
ORDERING INFORMATION

Part Number	Description
95/6440	Standard 6-slot Card Cage
95/6440/100	Standard 6-slot Card Cage with Cooling Fan, 110VAC
95/6440/200	Standard 6-slot Card Cage with Cooling Fan, 220VAC
95/6445	Expansion Interconnector
95/6448	Powered 6-slot Card Cage, 110VAC, 50/60 cycle
95/6448/100	Powered 6-slot Card Cage, 220VAC, 50 cycle
95/6450	Rack-mounted 6-slot System Chassis
95/6450/200	Mounting slide rails, flanges, and hardware
95/6452A	Rack-mounted 14-slot System Chassis (50A power supply)
95/6452/200	Mounting slide rails, flanges, and hardware

Engineering Systems

High Performance Controllers/MPUs

Line Card



*In Development

AmSYS is a trademark of Advanced Micro Devices, Inc.

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AmSYS™29/10B

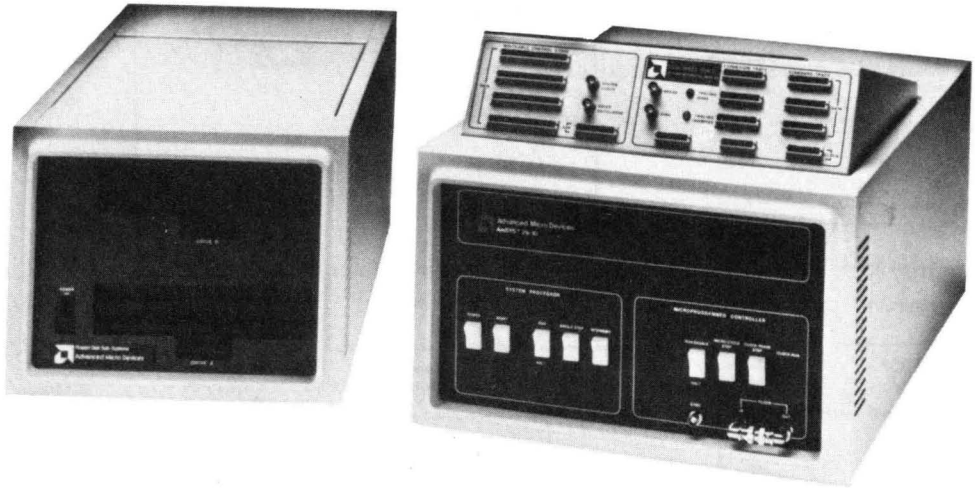
Microprogram/Bit-Slice Development System

DISTINCTIVE CHARACTERISTICS

- Complete floppy disk-based Microprogram/Bit-Slice Development system
- AMDASM® 2.0, fast meta-assembler for microcode language definition and source file assembly
- Full-speed Microprogram Controller for microcode and hardware integration
- Optional High-Speed Trace provides integrated 10MHz logic state analyzer with 48-bit input
- AMDOS® 29 Disk Operating System (CP/M*2.2 compatible)
- Dual single/double-density floppy disk subsystem provides 1 megabyte storage
- Supports Registered PROMs. Output buffer (std) replaceable with output registers
  - Am27S25, 27
  - Am27S35, 37
  - Am27S45, 47

GENERAL DESCRIPTION

The AmSYS29/10B Microprogram/Bit-Slice Development System is the most efficient development system for writing microcode and debugging high-speed microprogrammed or bit-slice microprocessor designs. With the super fast AMDASM 2.0 Meta-Assembler and High-Speed Trace option, project engineering efficiency is maximized and project design-time is cut to a minimum.



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AMDASM and AMDOS are registered trademarks of Advanced Micro Devices, Inc.
*CP/M is a trademark of Digital Research, Inc.

PRODUCT OVERVIEW

AmSYS29/10B is an engineering tool designed to aid development of microprogrammed Target Systems. Designers of high-speed computers use bit-slice architecture, like the 2900 Family, and microprogramming to optimize processor performance. The microprogrammed processor is more versatile and offers higher performance than the "fixed-instruction set" microprocessor. However, the versatility demands development tools specific to microprogrammed machines.

AmSYS29/10B provides the bit-slice designer with similar software development and hardware debug tools as those available to the MOS microprocessor developers. AmSYS29/10B is a Microprogram Development System offering symbolic language development of microcode, high-speed control store emulation, target-system clock control and logic state monitoring.

During the development cycle of a microprogrammed system, the greatest challenges are writing a microprogram for a user-defined microinstruction format and debugging the prototype hardware and microprogram in the target environment. AmSYS29/10B supplies the designer with the AMDASM meta-assembler to support microprogram development. The meta-assembler allows definition of a mnemonic instruction set for any microinstruction format. AMDASM, with the language definition table, then assembles the microprogram source file of symbolic code into a binary object file.

During hardware and software integration, AmSYS29/10B greatly reduces debug time by emulating critical parts of the Target System. AmSYS29/10B provides a Writable Control Store (WCS), replacing control store PROM with high-speed RAM. Target system clock control by the Clock Control Logic (CCL) allows single-step, multiple-step and full-speed execution with multiple breakpoints. Software is provided to set the RUN address to any location, monitor up to 128 bits and 32 logic points of microinstructions, and edit WCS contents.

A Microprogram Sequencer board is provided as an evaluation vehicle for microprogram familiarization and software module testing. The Microprogram Sequencer, when combined with CCL and WCS, forms a complete Microprogram Controller for testing and debugging prototype hardware.

AmSYS29/10B provides support for an optional High-Speed Trace unit with logic-state analyzing. The Trace unit is designed to track microinstructions and numerous bus paths found within complex bit-slice architectures.

The AmSYS29/10B provides complete hardware and software tools for the development of microprogrammed Target Systems.

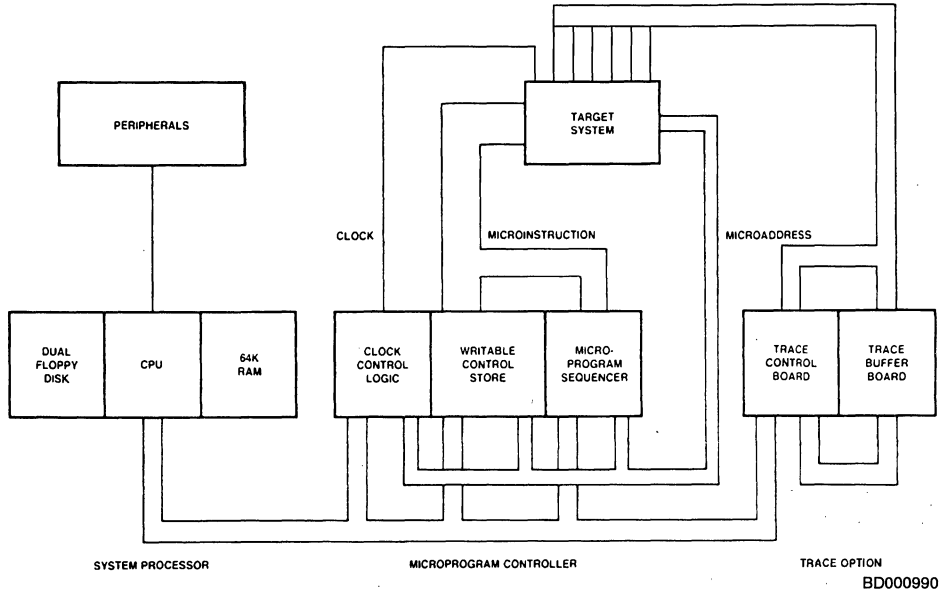
FUNCTIONAL DESCRIPTION

AmSYS29/10B is comprised of a System Processor, Microprogram Controller and support for an optional High-Speed Trace (Am29/6310) unit. A Block Diagram of the AmSYS29/10B is shown in Figure 1. The System Processor provides an interface to a CRT console, supports microprogram development software and directs the Microprogram Controller and High-Speed Trace option. The Microprogram Controller replaces target system PROM with high-speed, dual-ported RAM and replaceable output buffers. It also gates the target clock for single-step and breakpoint control and monitors up to 160 logic points in the target system. A Microprogram Sequencer is included to generate conditional 12-bit microaddresses (under microprogram control) forming a closed-loop controller for hardware testing. It also handles interrupts and maps opcodes to microroutine addresses. The optional High-Speed Trace provides 48 bits (expandable to 96 bits) of logic state analyzer capability at a 10MHz clock speed.

System Processor Processor Hardware

The System Processor is comprised of a CPU board, 64K bytes of RAM and a dual single/double-density floppy disk subsystem. The CPU board is configured around an 8080A microprocessor, along with four RS-232C serial ports, parallel printer interface and floppy disk interface. The serial ports support the Am29/8210A CRT console and a line printer at

Figure 1. AmSYS29/10B Block Diagram



9600 baud, a PROM programmer at 600 baud and any TTY-compatible device at 110 baud. The parallel port is configured to support a Centronics 702/703 dot matrix printer.

The memory support is a single RAM board with 64K bytes of dynamic RAM and self-refresh.

A separate chassis contains two 8-inch floppy disk drives. The floppy disk controller in the mainframe automatically detects and matches to the density (single or double) of the IBM format-compatible diskette in each drive.

Processor Software

AmSYS29/10B software supports microprogram development and controls the Microprogram Controller and Trace hardware. The Microprogram Support Software package runs under the disk operating system, AMDOS29, along with an editor, 8080/8085/Z80 relocatable macroassembler and file handling utilities.

Operating System

AMDOS29 provides rapid access to programs through a comprehensive file-management structure. The file subsystem supports a named-file structure allowing dynamic allocation of file space, as well as sequential and random-file access. AMDOS29 is compatible with a widely used and well documented operating system, CP/M, Version 2.2.

Communications with Host Computer

Source programs (written in C and Fortran languages) for communicating with the host computer are provided on diskette. One or the other must be installed to provide the correct protocol required by AmSYS29/10B.

MAP or WCS files created on a host computer may be downloaded to AmSYS29/10B over the RS-232C serial link at 110, 600, or 9600 baud using the host communications utility.

Perfect Writer

A powerful screen-oriented, word-processor/text editor configured for AmSYS29/10B may be used to write and edit microcode. Popular features are the on-screen menus to assist while learning; cursor movement by character, word, line, sentence, paragraph, screen, document; simple deletion commands; and commands to copy and move both within as well as between documents. Perfect Writer uses virtual memory architecture for editing documents larger than the computer's memory. It allows up to seven files to be "on-line" at the same time for ease in moving and copying text among documents or programs.

To take full advantage of the combined features of virtual memory architecture and multiple file buffers, Perfect Writer uses Dual Display Windows. With this feature you can view and edit files on-screen at the same time, plus scroll through one window while simultaneously editing the other.

Microprogram Generation Software

Development support of microprogram software is provided by the AMDASM, AMMAP, AMSCRM and AMPROM programs.

AMDASM is a meta-assembler designed to support microprogram formats with assembly-level mnemonics. The definition phase of the meta-assembler builds a lookup table of user-specified microinstruction word formats and format labels. Mnemonics are then assigned to constants, variables and format-field-default bit patterns. The resulting table is used by the assembly phase of AMDASM to assemble the source code into object code.

The AMMAP program assembles non-microinstruction PROM data such as constant tables and opcode-to-microaddress maps. This one-pass assembler accepts constant values for input or the AMDASM symbol table file "MAP," as an input along with an assembly source file provided by the user.

AMSCRM rearranges columns of code in an assembled object file. This feature allows hardware rearrangement without forcing definition file update and reassembly.

The final microprogram object file is generally entered into PROMs. AMPROM fragments the AMDASM object file in PROM-size blocks. These blocks are compatible with operating system utility that prepares files for the driver of the selected PROM programmer.

Microprogram Controller

The Microprogram Controller replaces target system PROM with high-speed, dual-ported RAM. It is comprised of a Writable Control Store board, Clock Control Logic board and Microprogram Sequencer board which provides microcode editing and target system control during hardware and software integration. It gates the target system clock and monitors up to 20 logic points and 12 addresses within the target system.

Writable Control Store (WCS)

Target system control PROM is replaced by high-speed WCS. AmSYS29/10B provides a single WCS board with 1K x 64 bits of buffered, dual-ported RAM (with replaceable output buffers), having a guaranteed access time of 35ns. Output registers are used to replace these buffers when Registered PROMs are to be simulated. Up to four WCS boards are supported by AmSYS29/10B in configurations of up to 128 bits wide or 4K words deep. User-modification of the basic board provides an 8K x 32-bit configuration. This memory may be mapped in 1K blocks to any address space in the Target System. The dual-port feature lets the user load, edit and save WCS contents through the System Processor while the other port can be connected to the Target System microinstruction bus.

Clock Control Logic (CCL)

The CCL board interfaces the System Processor, external interrupts and front panel controls to the Target System.

Under System-Processor control, the console operator can step one clock cycle, step one microinstruction, or run at full speed until a breakpoint is reached. The CCL monitors the microaddress and 20 target system logic points allowing them to be displayed on the CRT console. The microaddress from the Target Sequencer can be replaced by any new value from the System Processor through the CCL.

Up to seven full-speed interrupts may be enabled. These interrupts allow the target system clock to be halted due to a console input, front panel switch, address compare on the CCL board, or an interrupt on any one of four external inputs. One bit of the WCS applied to one of these external inputs may be used as an additional source of breakpoints, giving a breakpoint-per-address capability. The breakpoints may be SET or CLEARed either individually or within an address range. Two more external inputs are typically connected to the optional High-Speed Trace providing eight additional breakpoints that can be based on event comparisons up to 96 bits wide.

Microprogram Sequencer

The Microprogram Sequencer board allows testing of microprogram modules prior to hardware bread-board stage. This

sequencer provides conditional control of the microaddress bus and executes instructions provided by the WCS. Included are a 12-bit wide microsequencer with 16 instructions, a 12-bit loop counter, pipeline register, 16-way branch unit and 16 input condition code multiplexer. In addition, an 8-bit opcode can be mapped into a 12-bit microinstruction through the 256 x 12 mapping RAM.

Microprogram Debug Software

Microprogram Debug Software is a set of utilities used to move and edit microcode. They move microcode between disk and WCS RAM or disk and Microprogram Sequencer mapping RAM. These RAMs are commonly referred to as Bipolar Memory (BPM). DDT29 (Dynamic Debug Tool) edits Bipolar Memory contents and interfaces the console to the CCL.

LBPM and VBPM load and verify contents of Bipolar Memory while SBPM and RBPM save and restore contents.

DDT29 displays and allows the operator to edit the contents of Bipolar Memory. It transmits operator clock, microaddress and breakpoint commands to the CCL. In addition, DDT29 will access and display the current microaddress, microinstruction and monitor bits for a total display of 160 state bits. Any of these commands can be combined into a sequence that repeats automatically with the macro facility of DDT29.

High-Speed Trace Option

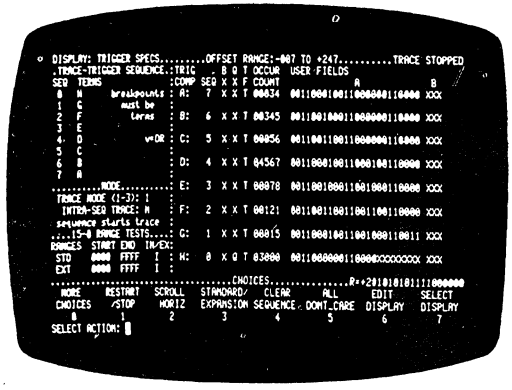
An optional High-Speed Trace (Am29/6310) unit provides additional hardware debug. The trace unit selectively records 48-bit wide data in a 256 word memory at a 10MHz rate. It is comprised of a Trace Control board, a 48-bit x 256 word Trace Buffer board, and a new system top cover, providing an extended front panel with microaddress and microinstruction connectors. An additional Trace Expansion (Am29/6312) option is available to extend trace buffer width to 96-bits, and a Trace Time-Tag board, providing 32 bits of event time storage.

Eight general-purpose triggers (with 16-bit programmable delays) are generated by eight comparators (48 or 96 bits wide). These triggers start or stop trace activity, qualify data for storage in the Trace Buffer and append up to eight additional breakpoints to the CCL.

Trace Time-Tag records the time between qualified events stored in Trace Buffer memory. With time based on target system clock pulses, it is easy to time complex operations and count loop iterations. The Time-Tag reduces the available trace data width unless the optional 32-bit wide Trace Time-Tag is used.

Innovative software reduces control of the complex structure to a few key strokes. The complete state of the Trace hardware is represented by five unique CRT screens. A representative display in Figure 2 is used to update the eight general-purpose triggers. All information controlling that state of each trigger, and relationship between triggers, is shown in this single display. Changes are inserted by entering the EDIT DISPLAY mode (soft key 6) and moving the cursor to the appropriate parameter. New values are typed in to change the state of the trigger hardware. Once all hardware has been set, the entire state can be saved as a disk file. A subsequent load of the saved state file will reset all hardware to the desired state.

Figure 2. Trigger Spec Screen Display



PD000330

SPECIFICATIONS

Physical Characteristics

System Chassis

Width:	17.1 in.	(43.4 cm.)
Height:	10.5 in.	(26.7 cm.)
Depth:	24.0 in.	(60.0 cm.)

Floppy Disk Subsystem

Width:	13.0 in.	(33.0 cm.)
Height:	10.5 in.	(26.7 cm.)
Depth:	24.3 in.	(61.6 cm.)

Electrical Characteristics

Voltage	Frequency	Current
100VAC ± 10%	50Hz ± 5%	7.5A
115VAC ± 10%	60Hz ± 5%	7.5A
220VAC ± 10%	50Hz ± 5%	4A
240VAC ± 10%	50Hz ± 5%	4A

Environmental Characteristics

Operating Temperature: 10°C to 40°C (50°F to 104°F) max.

Operating Humidity: 10 to 90% RH max. (noncondensing)

Equipment Supplied

AmSYS29/2910B Chassis including:

8080A-Based CPU Board
64K Bytes Dynamic RAM
Single/Double-Density Controller
Microprogram Controller comprised of:
- 1K x 64 High-Speed Writable Control Store Board with Registered PROM option (35ns)
- Clock Control Logic (100ns) Board
- Microprogram Sequencer Board

5V DC Power Supply at 75 Amps

Equipment Supplied (Cont.)

Floppy Disk Subsystem including:

Two 8-Inch Floppy Disk Drives
Software including:

AMDOS29 Disk Operating System
Communications Utilities Pkg.
Microprogram Support Software
Perfect Writer Software Pkg.
AMDASM 2.0 Fast Meta-Assembler
AMDASM 3.0 Fast Macro Meta-Assembler (option)
Trace29 (option)

Blank Floppy Diskettes (2)

Reference Manuals

680123
050510294-001 – ED Editor Manual
050510295-001 – DDT29 User's Manual
059910496-001 – AMDOS29 Interface Guide
059910500-001 – AMDOS29 D.O.S. User's Manual
059920003-002 – AmSYS29/10/15 High-Speed Writable Control Store User's Manual
059920026-002 – AmSYS29/10/15 Clock Control Logic/Instr. Board User's Manual
059920027-003 – AmSYS29/10B User's Manual
050520029-002 – Communications Utilities User's Manual

ORDERING INFORMATION

Part Number	Description
29/2910B*	AmSYS29/10B Microprogram/Bit-Slice Development System (115V/60Hz power supply)
29/2920B*	Same as 29/2910B except with 220V/50Hz power supply
29/2930B*	Same as 29/2910B except with 100V/50Hz power supply
29/2940B*	Same as 29/2910B except with 240V/50Hz power supply
Companion Products	
29/2065	1K x 64 High-Speed Writable Control Store Board with Registered PROM option (35ns)
29/6310	10MHz High-Speed Trace (48 x 256) Unit. (Requires a 29/8210A, 29/8220A, 29/8230A, or 29/8240A CRT Console)
29/6312	Trace Buffer Expansion (48 x 256) Board and Trace Time-Tag (32 x 256) Board
29/8210A	CRT Console (115V/60Hz)
29/8220A	CRT Console (220V/50Hz)
29/8230A	CRT Console (100V/50Hz)
29/8240A	CRT Console (240V/50Hz)
29/8652	PROM Programmer Cable, Data I/O
29/8653	PROM Programmer Cable, Prolog
29/8654	Serial I/O Cable
29/8656	Parallel Printer Cable

*Requires Software License Agreement.

AmSYS™29/15

Microprogram Control Store Emulator

DISTINCTIVE CHARACTERISTICS

- Low cost emulator for AMD's 2900 Family
- Attaches to any 'Host' computer
- Full-speed Microprogram Controller for microcode and hardware integration
- Supports Am29116, Am29501, and Am29540
- Components shared with the AmSYS29/10B
- Upgrade path to the AmSYS29/10B
- Supports Registered PROMs. Output buffer (std) replaceable with output registers.
  - Am27S25, 27
  - Am27S35, 37
  - Am27S45, 47
- Extended breakpoint-per-address

GENERAL DESCRIPTION

A member of the AmSYS29/10B Family of Microprogram/Bit-Slice Development System products, the AmSYS29/15 provides the large mainframe or minicomputer user with high-speed, real-time emulation and debug features for microprogram/bit-slice designs.

04366A

PRODUCT OVERVIEW

AmSYS29/15 is an engineering tool specifically designed to aid development of microprogrammed systems. Designers of high-speed computers use bit-slice architecture, like the 2900 Family, and microprogramming to optimize processor performance. The microprogrammed processor is more versatile and offers higher performance than the fixed-instruction set microprocessor. However, this versatility demands development tools specific to microprogrammed machines.

AmSYS29/15 provides the bit-slice designer with similar software development and hardware debug tools as those available to the MOS microprocessor developers. AmSYS29/15 is a Microprogram Development System offering the latest in high-speed control store emulation, target-system clock control and comprehensive debug capabilities.

During the development cycle of a microprogrammed system, the greatest challenges are writing a microprogram for a user-defined microinstruction format, and debugging the prototype hardware and microprogram in the target environment. After writing and assembling a microprogram using an editor and the Meta-assembler program (on the host computer), the resulting object code files may be downloaded using the AmSYS29 Host Communication Utility and run in real-time on the AmSYS29/15.

During hardware and software integration, AmSYS29/15 greatly reduces debug time by emulating critical parts of the target system. AmSYS29/15 provides a Writable Control Store (WCS) replacing control store PROM with high-speed RAM. Target system clock control by the Clock Control Logic (CCL) allows single-step, multiple-step and full-speed execution with multiple breakpoints. Software is provided to set the RUN address to any location, monitor up to 128 bits and 32 logic points of microinstructions, and edit WCS contents.

A Microprogram Sequencer board is provided as an evaluation vehicle for microprogram familiarization and software module testing. The Microprogram Sequencer, when combined with the CCL and WCS, form a complete Microprogram Controller that is useful for testing and debugging prototype hardware.

FUNCTIONAL DESCRIPTION

AmSYS29/15 Microprogram Control Store Emulator (MCSE) is comprised of a System Processor, a Microprogram Controller, and the fast host communication software. Figure 1 shows the AmSYS29/15 Block Diagram. The System Processor provides an interface to a CRT console, supports microprogram development software and directs the Microprogram Controller. The Microprogram Controller replaces target system PROM with high-speed, dual-ported RAM. It also gates the target clock for single step and breakpoint control and monitors up to 160 logic points in the target system. A Microprogram Sequencer is included to generate conditional 12-bit microaddresses (under microprogram control) forming a closed-loop controller for hardware testing. It also handles interrupts and maps opcodes to microroutine addresses.

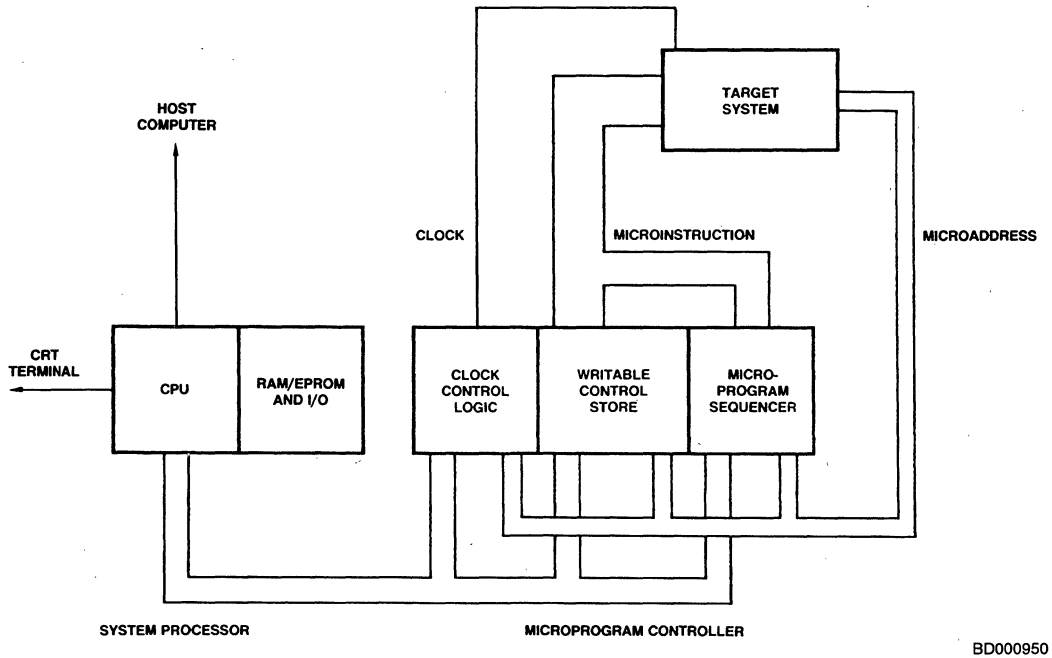
System Processor

Processor Hardware

The System Processor is comprised of a CPU board and a Programmable RAM/EPROM and I/O board. The CPU board is configured around an 8080A microprocessor, along with four RS-232C serial ports and a parallel printer interface port. One of the serial ports supports the Am29/8210A CRT console and one connects to the host computer, both at 9600 baud. The other two serial ports are not used in the AmSYS29/15 and are designated as spare ports.

The memory support is a single RAM/EPROM and I/O board with 16K bytes of RAM and 40K bytes of EPROM.

Figure 1. AmSYS29/15 Block Diagram



Processor Software

Diagnostics

A diagnostic utility is included in the system to test system RAM on power-up or RESET. Errors are displayed on the CRT console.

A second diagnostic is available in EPROM to test the WCS and mapping RAM when called up via the keyboard.

Communications with Host Computer

Source programs (written in C and Fortran languages) for communicating with the host computer are provided on diskette. One or the other must be installed to provide the corrected protocol required by AmSYS29/15.

MAP or WCS files created on a host computer may be downloaded to AmSYS29/15 over the RS-232C serial link at 110, 600, or 9600 baud using the host communication utility.

Microprogram Controller

The Microprogram Controller replaces the target system PROM with high-speed, dual-ported RAM. It is comprised of a Writable Control Store board, Clock Control Logic board and Microprogram Sequencer board which provide microcode editing and target system control during hardware and software integration. It gates the target system clock and monitors up to 20 logic points and 12 addresses within the target system.

Writable Control Store (WCS)

Target system control PROM is replaced by high-speed WCS. AmSYS29/15 provides a single WCS board with 1K x 64 bits of buffered, dual-ported RAM (with replaceable output buffers), having a guaranteed access time of 35ns. Output registers are used to replace these buffers when Registered PROMS are to be simulated. Up to four WCS boards are supported by AmSYS29/15 in configurations of up to 128 bits wide or 4K words deep. User modification of the basic board provides an 8K x 32-bit configuration. This memory may be mapped in 1K blocks to any address space in the Target System. The dual-port feature lets the user load, edit and save WCS contents through the System Processor while the other port can be connected to the Target System microinstruction bus.

Clock Control Logic (CCL)

The CCL board interfaces the System Processor, external interrupts and front panel controls to the Target System.

Under System-Processor control, the console operator can step one clock cycle, step one microinstruction, or run at full speed until a breakpoint is reached. The CCL monitors the microaddress and 20 target system logic points allowing them to be displayed on the CRT console. The microaddress from the Target Sequencer can be replaced by any new value from the System Processor through the CCL.

Up to seven full-speed interrupts may be enabled. These interrupts allow the target system clock to be halted due to a console input, front panel switch, address compare on the CCL board, or an interrupt on any one of four external inputs. One bit of the WCS may be dedicated for use as additional source of breakpoints, thus giving a break-per-address capability. The breakpoints may be SET or CLEARed either individually or within an address range.

Microprogram Sequencer

The Microprogram Sequencer board allows testing of microprogram modules prior to hardware bread-board stage. This sequencer provides conditional control of the microaddress bus and executes instructions provided by the WCS. Included are a 12-bit wide microsequencer with 16 instructions, a 12-bit loop counter, pipeline register, 16-way branch unit and 16 input condition code multiplexer. In addition, an 8-bit opcode can be mapped into a 12-bit microinstruction through the 256 x 12 mapping RAM.

Microprogram Debug Software

Microprogram Debug Software is a set of utilities used to move and edit microcode. They move microcode between disk and WCS RAM or disk and Microprogram Sequencer mapping RAM. These RAMs are commonly referred to as Bipolar Memory (BPM). DDT29 (Dynamic Debug Tool) edits Bipolar Memory contents and interfaces the console to the CCL.

LBPM and VBPM load and verify contents of Bipolar Memory while SBPM and RBPM save and restore contents.

DDT29 displays and allows the operator to edit the contents of Bipolar Memory. It transmits operator clock, microaddress and breakpoint commands to the CCL. In addition, DDT29 will access and display the current microaddress microinstruction and monitor bits for a total display of 160 state bits. Any of these commands can be combined into a sequence that repeats automatically with the macro facility of DDT29.

Upgrade Path to the AmSYS29/10B

If local editing and assembly are necessary, the AmSYS29/15 can be upgraded to the full-featured AmSYS29/10B Microprogram/Bit-Slice Development System. The AmSYS29/10B contains all the tools necessary to develop a microprogrammed project. An efficient word processor and meta-assembler are part of the comprehensive software provided. The High-Speed Trace (Am29/6310) option is available to provide logic state analyzing which is invaluable during hardware and software integration.

SPECIFICATIONS

Physical Characteristics

System Chassis

Width:	17.1 in.	(43.4 cm.)
Height:	10.5 in.	(26.7 cm.)
Depth:	24.0 in.	(60.0 cm.)

Electrical Characteristics

Voltage	Frequency	Current
100VAC ±10%	50Hz ± 5%	7.5A
115VAC ±10%	60Hz ± 5%	7.5A
220VAC ±10%	50Hz ± 5%	4A
240VAC ±10%	50Hz ± 5%	4A

Environmental Characteristics

Operating Temperature: 10°C to 40°C (50°F to 104°F) max

Operating Humidity: 10 to 90% RH max (noncondensing)

Equipment Supplied

AmSYS29/2915 Chassis including:
8080A-based CPU Board
64K Bytes Dynamic RAM

Equipment Supplied (Cont.)

Microprogram Controller comprised of:
1K x 64 High-Speed Writable Control Store Board (35ns) with Registered PROM Option
Clock Control Logic (100ns) Board
Microprogram Sequencer Board

5V DC power supply @ 75 Amps

Reference Manuals

059920078-001 – AmSYS29/15 Microprogram Control Store Emulator User's Manual
059920079-001 – AmSYS29/15 Microprogram Support Software User's Manual
059920080-001 – DM9MCSE Diagnostic Monitor User's Manual
059920003-002 – AmSYS29/10/15 High-Speed Writable Control Store User's Manual
059920026-002 – AmSYS29/10/15 Clock Control Logic/ Instr. User's Manual
050520029-002 – Communications Utilities User's Manual
059920039-001 – Am96/5232 Programmable RAM/EPROM and I/O Board User's Manual

ORDERING INFORMATION

Part Number	Description
29/2915*	AmSYS29/15 Microprogram Control Store Emulator (115V/60Hz power supply)
29/2925*	Same as 29/2915 except with 220V/50Hz power supply
29/2935*	Same as 29/2915 except with 100V/50Hz power supply
29/2945*	Same as 29/2915 except with 240V/50Hz power supply
Companion Products	
29/2065	1K x 64 High-Speed Writable Control Store Board (35ns) with Registered PROM Option
29/8210A	CRT Console (115V/60Hz)
29/8220A	CRT Console (220V/50Hz)
29/8230A	CRT Console (100V/50Hz)
29/8240A	CRT Console (240V/50Hz)
Upgrade to AmSYS29/10B Kits	
29/9915	Includes 64K RAM Board, Floppy Disk Controller, 110V/60Hz Dual Floppy Disk Subsystem, AmSYS29/10B Software and Manuals
29/9925	Same as 29/9915 except with 220V/50Hz Subsystem
29/9935	Same as 29/9915 except with 100V/50Hz Subsystem
29/9945	Same as 29/9915 except with 240V/50Hz Subsystem

*Requires Software License Agreement.

Am29/2065

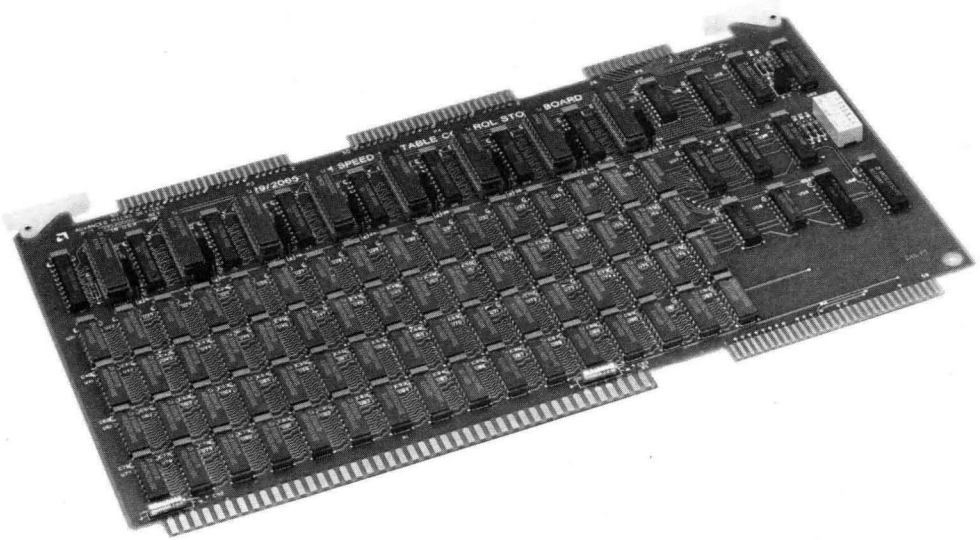
High-Speed Writable Control Store

DISTINCTIVE CHARACTERISTICS

- Fast, dual-ported RAM replaces target control store (Access: 35ns)
- Supports Registered PROMs (option). Output buffer (std) replaceable with output registers
  - Am27S25, 27
  - Am27S35, 37
  - Am27S45, 47
- WCS in the AmSYS™29/10B and AmSYS29/15 Development Systems
- 1K words x 64 bits standard
- Configurable as 2K x 32 bits
- May be mapped in 1K blocks to any address in the target system

GENERAL DESCRIPTION

The Am29/2065 High-Speed Writable Control Store with Registered PROM Option is a fast, dual-ported static RAM board for use in the System 29 Family of Microprogram/Bit-Slice Development Systems.



AmSYS is a trademark of Advanced Micro Devices, Inc.

04708A

PRODUCT OVERVIEW

In a microprogrammed or bit-slice microprocessor design, the microprogram that controls operation of the prototype system is generally kept in a Writable Control Store (WCS). This WCS is a special memory in which the microprogram can be easily modified and updated during the development process. In most cases it will be replaced by Read-Only Memory (ROM) when the prototype goes into production.

FUNCTIONAL DESCRIPTION

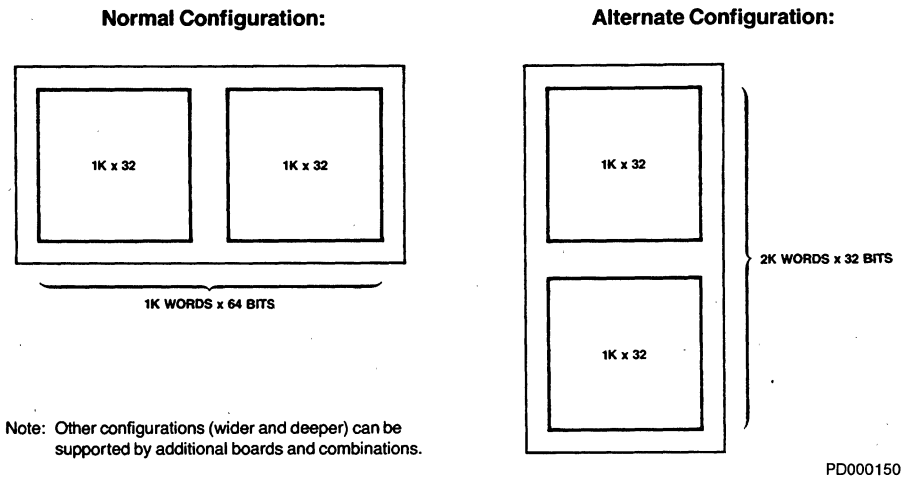
The High-Speed Writable Control Store has a basic word width of 64 bits, which by changing jumpers can be altered to a 32-bit width (see Figure 1 for configurations). In any case, a maximum of four boards can be installed in the AmSYS29/10B or AmSYS29/15. The System Processor can write to or read from the fast Random-Access Memory (RAM) contained on-board to load or save the microprogram. The prototype system can gain access to the RAM in a read-only mode to execute information stored there.

User Interface

Connectors P3, P4 and P5, along the top edge of the WCS board, are used to interface the WCS to the prototype system (see Figure 2). The prototype system must supply a 12-bit address to connector P5. The WCS supplies the data bits (associated with that address) to the prototype system via connectors P3 and P4. Being a dual-ported RAM, the System Processor is not allowed to access the WCS board when the prototype system is operating. The on-board bus buffers select the appropriate operation of the board depending upon the operation of the target system clock.

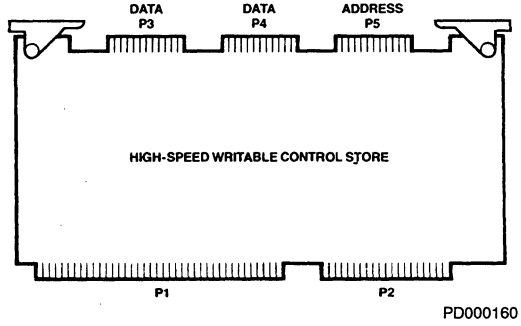
To support a design using AMD's Registered PROMs (Am27S25, Am27S35 and Am27S45), the AMD 29800 Bus Interface Family in 24-pin 300-mil wide packages, are used as output buffers or registers in the sockets provided on-board. The output buffers serving the prototype system (Am29828s) can be replaced with an output register (Am29824s).

Figure 1. Am29/2065 Configurations



Note: Other configurations (wider and deeper) can be supported by additional boards and combinations.

Figure 2. High-Speed Writable Control Store



SPECIFICATIONS

The Am29/2065 is a block of 1K x 64 bits of fast RAM on MULTIBUS*-form circuit boards using P1 and P2 edge connectors for backplane interface to data and address buses.

Access Time

35ns

Interface Characteristics

P1 and P2
- Backplane Connector

P3 and P4
- High-Speed Data Bus Connector

P5
- High-Speed Address Bus Connector

Physical Characteristics

Width:	12.00 in. (30.48 cm.)
Height:	6.75 in. (17.15 cm.)
Thickness:	.50 in. (1.27 cm.)

Electrical Characteristics

DC Power Requirement
+5V at 12.0 Amps max.

Environmental Characteristics

Operating Temperature:	10°C to 40°C (50 to 104°F) max.
Operating Humidity:	10 to 90% RH max. (noncondensing)

Reference Manual

059920003-002 – AmSYS29/10/15 High - Speed Writable Control Store

ORDERING INFORMATION

Part Number	Description
29/2065	1K x 64 High-Speed Writable Control Store Board (35ns) with Registered PROM Option
Companion Products	
29/2910B*	AmSYS29/10B Microprogram/Bit-Slice Development System (115V/60Hz power supply)
29/2915*	AmSYS29/15 Microprogram Control Store Emulator (115V/60Hz power supply)

*Requires Software License Agreement.

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*Multibus is a registered trademark of Intel Corporation.

Am29/6310 • Am29/6312

High-Speed Trace/Trace Expansion

DISTINCTIVE CHARACTERISTICS

- Provides logic analyzer capability for 2900 Family bipolar designs
- Plugs into AmSYS™29/10B Microprogram Development System
- 10MHz (100nsec) event storage capability
- Event storage unit of 48 x 256 words, expandable to 96 bits
- 32-bit Trace Time Tag records event occurrence time
- Eight general purpose 48-bit triggers, expandable to 96 bits
- Adds eight hardware breakpoints to AmSYS29/10B clock control logic
- Software integrated with microprogram debug software (DDT29) on AmSYS29/10B

GENERAL DESCRIPTION

The Am29/6310 is a 48-bit wide, 10MHz logic state analyzer that plugs directly into the AmSYS29/10B Development System. It can be expanded to 96 bits wide (with 32 bits of event counting) by adding the Am29/6312 Trace Expansion. Rapid software and hardware integration result from use of these comprehensive development tools.

AmSYS is a trademark of Advanced Micro Devices, Inc.

05200A

PRODUCT OVERVIEW

The Am29/6310 High-Speed Trace unit is an option available on AmSYS29/10B that takes general purpose measurements of simultaneous logic events. These events typically occur in microprocessor-based computers and in microprogrammed machines. The Trace unit performs real-time event and count measurement at speeds up to 10MHz on a 48-bit-wide sample. In addition, multiple triggers provide event-based controls that allow you to capture the data of interest.

Event measurements are displayed on the CRT in a user-defined format. Each field of the format can be displayed in binary, octal, decimal, hexadecimal or ASCII, as specified by the user. Field formatting and number-base specification are set up on a single CRT page using a movable cursor and a command menu. Events are captured on each specified clock transition and are retained in buffer memory.

Completion of a trigger sequence enables trace activity. The trigger sequence may be from one to eight levels deep. The sophisticated trigger sequence capability allows trace activity to be controlled by a complex sequence of events. For example, program execution of different flow paths and loops is easily analyzed.

Once trace activity has been initiated, up to 255 events that satisfy the trace qualifiers will be recorded in the trace buffer. The user may specify any number of events to be traced before, during, or after the trigger sequence is complete.

Upon completion of the trigger sequence, a SYNC pulse will be generated as an output signal to synchronize any user supplied equipment to the trace sub-system.

In addition, any trigger term may generate a breakpoint to the AmSYS29/10B Clock Control Logic. This adds eight complex hardware breakpoints to the system capabilities.

A count measurement capability accumulates a time tag that can be stored with each event. Each clock pulse increments the counter until an event occurs. The event data is recorded along with the count.

FUNCTIONAL DESCRIPTION

The High-Speed Trace unit consists of two boards that plug into the AmSYS29/10B, together with a set of trace software programs. The Trace Control Board communicates with the System Processor, synchronizes timing with a master clock, and controls the mode of operation. The Trace Buffer Board consists of 255 words (48 bits wide) and eight comparators. The 48-bit input can be split into a data register segment and a time count segment which records clock edges. Communication between the Trace Control Board and the Trace Buffer Board takes place over the High-Speed Trace bus on the P2 connector.

The optional Trace Buffer Expansion (Am29/6312) consists of two boards, the Trace Buffer Expansion Board and Time-Tag Board. The buffer expansion adds 48 bits of event memory and the Time-Tag adds 32 bits of clock counter and stores up to 255 event occurrence times.

The complete four-board High-Speed Trace unit is shown in Figure 1.

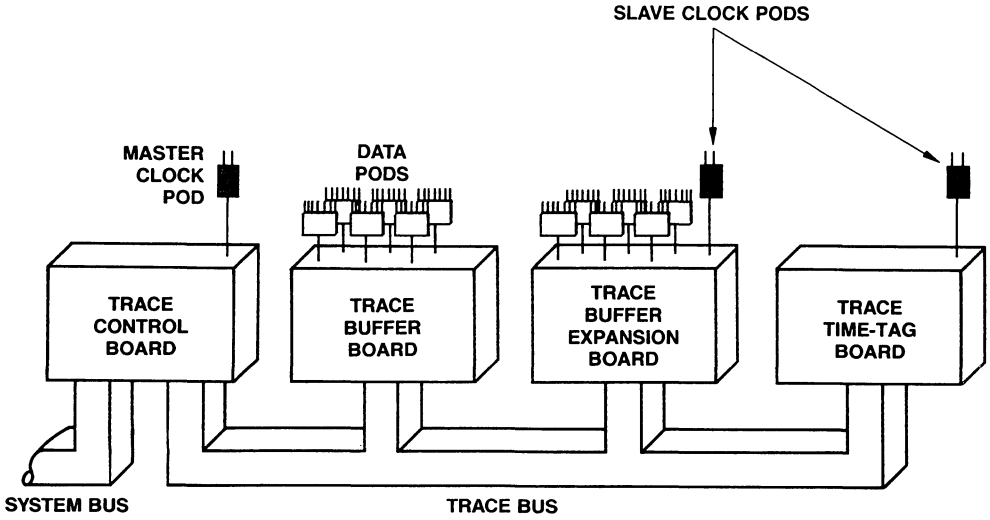
Operation of the High-Speed Trace is directed from the AmSYS29/10B system console. On AmSYS29/10B, the microcode debug program has been expanded to handle control of the Trace unit. The new display shows the state of the Trace unit in six CRT pages which can be called up by a single keystroke. Each page can then be updated with cursor-directed editing.

Screen Display Formats

A common format, shown in Figure 2, is used for each page. The display name shows which page is on the CRT; the hardware status indicates the present hardware activity. At the bottom of every page is a query/response section used by the operator to enter such additional information as the name of a Load/Save file.

Above this section are the soft key labels. These allow up to eight actions, including an EXIT key and a MORE ACTIONS key. The ACTION/ERROR segment indicates the operator interface state, and the CALCULATOR segment allows the

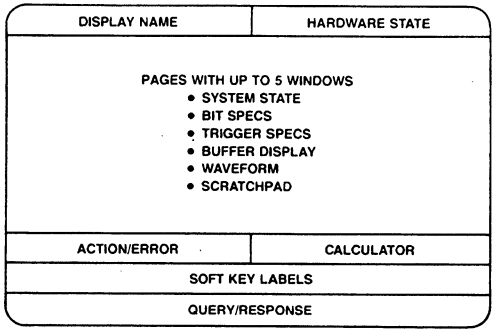
Figure 1. Four-Board High-Speed Trace Unit



operator to compute address offsets and change number bases.

The central portion of the screen is page dependent and can be broken down into as many as five windows. The window contents are explained for each of the six pages.

Figure 2. Trace Display Page Format



PD000080

System State Display

The system state page (Figure 3) allows the operator to describe the Trace hardware configuration to the software.

The Trace Buffer Board and optional Trace Buffer Expansion Board each have a 48-bit input register/counter that is segmented into 16/8/8/16 bits. The first three segments can be selected to capture data or act as a single 16, 24, or 32-bit counter as selected by the USE (D/T) field.

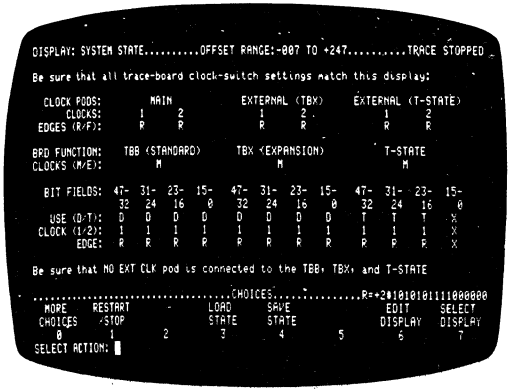
Each board has two clock inputs, clock (1/2), that can be connected to the counter and each register segment. Data is captured on the rising or falling edge of the clock as specified by the EDGE field.

The optional Trace Time-Tag Board can act only as a counter of clock edges and is 32 bits wide. Use of the Trace Time-Tag Board allows 96 bits of data to be captured by the buffer boards.

Bit Spec Display

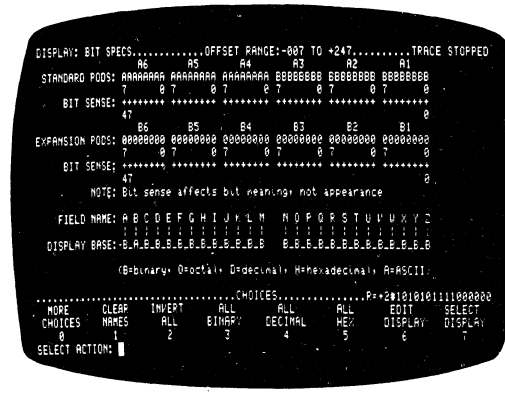
Display of the input data can be formatted by the operator. Up to 96 bits are represented on the BIT SPECS page (see Figure 4), providing the operator with bit-wide format control.

Figure 3. System State Screen Display



PD000100

Figure 4. Bit Spec Screen Display



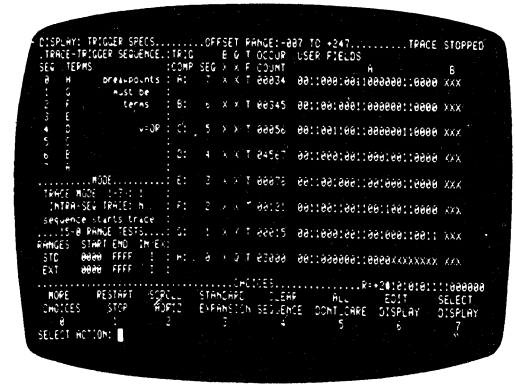
PD000110

The Bit Sense allows the corresponding data bit to be specified in a high or low true sense. The data displayed is as captured. This is particularly useful when displaying a negative-logic bus signal. Each bit can have a one-letter label assigned to it, along with other selected bits. The field of bits under a common label can then be displayed in a user-specified base selected from the five number bases listed.

Trigger Spec Display

Utilization of the trace memory buffer can be optimized by activating data storage only when events of interest have occurred. The High-Speed Trace unit provides eight general purpose comparators that generate a pulse when incoming data matches one of the eight specifications. The specifications are user-defined in the right-hand window of the trigger spec page, shown in Figure 5.

Figure 5. Trigger Spec Screen Display



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A Hex display base allows all 96 data bits to be displayed while a BINARY display base with horizontal scrolling allows individual specification bits to be set to 1, 0, or X ("don't care"). The T/F column allows the entire mask specification to be complemented, forcing triggers on all events not meeting the specification.

The control window includes a 16-bit pass count for each trigger which delays the trigger output for up to 65,535 comparison events. The delayed trigger can be used as a breakpoint to stop the clock, or as an event recognizer to delay the start of trace activity.

Triggers may be ORed into levels, and the levels time sequenced to provide a complex trigger sequence which controls the start of trace activity. Each trigger may be assigned to a different level as shown at the upper left window of the display. Triggers sharing a level are ORed such that the first trigger to occur satisfies the level.

The sequence activates trace activity in one of three modes: sequence start; sequence end, or pre-sequence start. Sequence start mode enables recording of the next 255 qualified events following sequence completion. In sequence end mode, the last 255 events, including at least the final trigger, are recorded. In pre-sequence count mode, the operator may specify how many events before the sequence completion are stored in the buffer. The remainder of the buffer is filled with the events that follow the sequence.

The lower window of the trigger spec display allows specification of a range of valid input data. The range applies to the lower 16 bits of the input register for each 48-bit memory buffer used. The two values entered specify the limits of an acceptable range of data values. Data may fall within or outside the defined values as specified by the I/E toggle. Examples of acceptable ranges are shown in Figure 6.

Figure 6. Event Data Range Comparisons

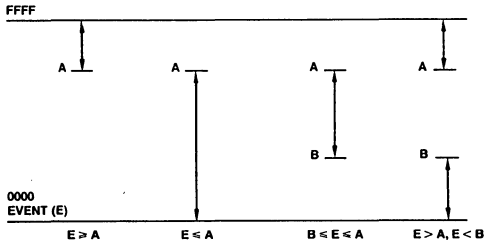

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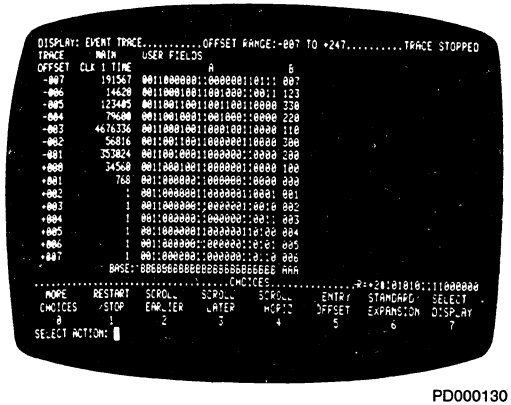
Figure 7. Event Buffer Screen Display



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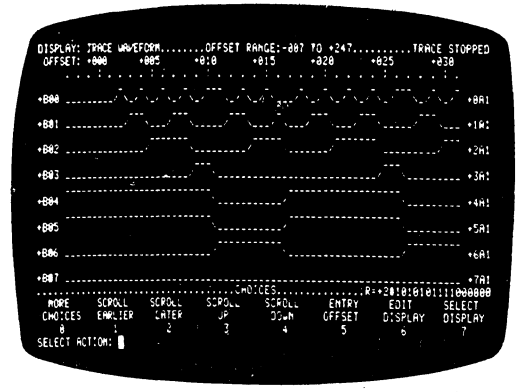
Event Buffer Display

The event buffer page (Figure 7) displays the contents of the memory buffer when the trace is stopped. The display format can be modified to a user-selected format or to one of the standard data bases. The clock display shows the time-tag value for each data point. Time tags may be shown incrementally or cumulatively and a time base scale factor may be specified. This is useful if an oscilloscope has been triggered by the SYNC pulse. The time-tag values are then scaled to correspond to the time base used on the oscilloscope.

Figure 8. Trace Waveform Screen Display



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Trace Waveform Display

As an additional aid in tracking logic activity with an oscilloscope, any data recorded with the High-Speed Trace unit can be displayed in waveform format (Figure 8). Scrolling allows monitoring of all 255 words horizontally and all 96 inputs vertically. Resolution of this display is a function of the clock used to sample the data.

Scratchpad Display

A blank half-page area, together with a line editor, allow user-comments to be stored with the save file for future reference The scratchpad display also shows a history of recent calculations and of files loaded and saved.

SPECIFICATIONS

Clock Frequency

Master clock: 10MHz maximum
Slave clock: 10MHz maximum
Minimum clock pulse width: 40ns

Interface

Interface	Clock Probe	Data Probe
I_{IL}	−0.8mA	−0.2mA
I_{IH}	0.1mA	0.02mA
Note: All signals on connectors are TTL compatible		

Power Requirements

Part Number	Voltage	Typical Current	Maximum Current
Am29/6310	+5VDC±5%	10.1A	14.8A
Am29/6312	+5VDC±5%	6.9AA	10.0A

Physical Characteristics

Width: 12.00 in. (30.4 cm.)
Height: 6.75 in. (17.15 cm.)
Thickness: 0.50 in. (1.27 cm.)

Environmental Characteristics

Operating Temperature: 0°C to 40°C
Operating Humidity: Up to 90° RH max. (non-condensing)

Reference Manual

059910329-002 – Am29/6310 High-Speed Trace Unit

ORDERING INFORMATION

Part Number	Description
29/6310	High-Speed Trace unit, includes Trace Control Board with clock pod, Trace Buffer Board with 255 x 48 bits of 10MHz memory buffer, six 8-bit-wide data pods, 1 clock pod, connector panel, cables, software, documentation. Plugs into AmSYS29/10B.
29/6312	Trace Buffer Expansion Board expands High-Speed Trace to 96 bits of data input. Trace Time-tag Expansion Board adds 256 x 32 bits of time-tag storage to 96-bit configuration of High-Speed Trace. Includes 6 data pods and 2 clock pods.
Companion Products	
29/2910B*	AmSYS29/10B Microprogram/Bit-Slice Development System (115V/60Hz power supply).

*Requires Software License Agreement.

MULTIBUS Data Book

MULTIBUS® SYSTEM ARCHITECTURE: Its Origin and Evolution

The Beginning

MULTIBUS® system architecture is a relatively new phenomenon, but its roots can be traced back to the formative years of the microcomputer industry. Its history is one of humble beginnings and gradual, controlled evolution. An understanding of this history is useful in understanding the architecture.

In the early 1970's, the advent of VLSI component technology offered revolutionary benefits to the awaiting public. The emergence of these new "super chips" created opportunities and chaos in the marketplace, while competitive pressures forced companies to invest in the new concept. Everyone had to participate to be competitive, but not everyone had the design expertise.

Intel Corporation, being aware of the situation, introduced their Intellec™ series of development systems to provide design engineers with the software development tools needed to implement system designs. This software assist was welcomed, however customers also wanted to reduce the hardware design effort. Consequently, they purchased development system units, removed the boards for incorporation into their own boxes, and used the development system bus as the interface. They wanted the capability of designing their own custom boards, so a copy of the system bus specifications was requested. Intel then began distribution of the system bus specifications to the world.

Intel recognized the need for board level solutions, and pursued it. In 1976, they introduced their first board-level computer, the iSBC® 80/10, integrating a CPU, memory and I/O onto the first OEM single board computer. Soon after, the development system bus was given its own name, the MULTIBUS system bus, and the MULTIBUS architecture was born.

The new single board computers became an instant success, and an array of compatible products emerged from Intel and other vendors as well. Then in 1977-78, the microcomputer industry witnessed the introduction of new VLSI microcomputers. These new 16-bit machines had a new set of requirements. With a downward compatible evolution, the MULTIBUS structure supported these new processors, and reaffirmed the viability of the MULTIBUS system bus as a long-lived industry standard.

Standards Assure Success

Some of the characteristics which are required of a standard should be known before examining its advantages. The three most important requirements are:

- A standard must have industry acceptance and support.
- A standard must evolve to meet the needs of the future.
- A standard must have a single point of control.

In the case of the MULTIBUS system bus standard, it was introduced in 1976 and, in two years, had achieved wide spread industry acceptance. The bus had evolved to accommodate both 8- and 16-bit machines and their requirements. At first, Intel maintained control of the bus specifications, but now this task has been assumed by the IEEE. This single point of control ensures product compatibility between different board sources. MULTIBUS specifications were freely available to the industry and in the public domain. It was for these reasons that MULTIBUS architecture became the de facto industry standard, and also the IEEE bus standard, IEEE 796.

Advantages of Standards

The advantages that the MULTIBUS architecture standard offers to the user are based on growing support by multiple sources and continued evolution. The MULTIBUS market has shown phenomenal growth in the number of MULTIBUS vendors. Another area of tremendous growth in the MULTIBUS market is in the number of MULTIBUS products made available to the industry by the growing MULTIBUS vendor base. Together, the MULTIBUS vendor and product growth trends reveal a healthy market.

A healthy open market offers tremendous benefits to potential users of MULTIBUS products. For instance, 120 MULTIBUS vendors means competition; and competition encourages competitive, low prices. The user pays less per MULTIBUS product which reduces overall system unit cost. Multiple sources of MULTIBUS products also means reduced risk to the user by eliminating the threat of sole source supply of important parts. Also, an open market which offers over 1000 MULTIBUS products provides a user with a wider range of choices. This selection of system solutions offers system designers almost unlimited flexibility and freedom. These pre-tested, off-the-shelf units mean a user can get to market quicker, with lower costs, and yet have the latest in VLSI technology. Additionally, a MULTIBUS user can optimize his own resources and expertise, by concentrating on what he does best, and designing his own proprietary boards to the MULTIBUS standard. This allows the user to inject as much added-value into the system as he can in order to maximize his profit and be competitive. Only adherence to the MULTIBUS standard allows this flexible, added value concept to work.

In order to maintain adherence to a standard, the standard must continue to evolve to meet the need of the future. Since the MULTIBUS market needs are dynamic, the standard cannot remain static. It must be adaptable and upgradeable; continuing to evolve in a controlled deliberate manner.

Evolving Architecture: MULTIBUS®, iLBX™,iSBX™, MULTICHANNEL™

The MULTIBUS standard actually evolved in two different aspects: structure and architecture. The structure evolved from 8-bit to 16-bit capability, and direct addressing expanded from 64 KB to 16 MB. The architecture was expanded via the iLBX™ bus, iSBX™ bus, and MULTICHANNEL™ bus. These evolutionary expansions were necessary because a single system bus structure was no longer capable of supporting the demands of today's high-speed, high-performance VLSI microprocessor technology, and its increasingly complex configurations. A single bus structure also tended to limit the available products to one dimensional "solutions".

The MULTIBUS architectural extensions occurred in the evolutionary process, because of the potential advantages in improved performance and flexibility.

The iLBX bus was created to provide users an architectural solution that extends the high performance benefits of a processor's on-board local bus to off-board memory resources. By supporting large amounts of high performance memory, the iLBX structure maximizes the performance potential for today's high-speed microprocessors by eliminating their need to access memory resources solely over the system bus. Powerful iLBX system modules can be created using the iLBX bus to connect a single board computer and a maximum of four memory cards. Acting as "virtual" iSBCs, these modules can directly access up to 16 megabytes of processor addressable memory over the iLBX bus and appear as though it were resident on the processor board. The iLBX bus preserves the advantages in performance and architecture of on-board memory, while allowing a wide range of memory capabilities to match application requirements.

The iSBX bus was created to provide users with a low cost, on-board expansion solution for MULTIBUS single board computers. Currently, the iSBX boards allow users to add capability to a single board computer in the areas of parallel I/O, serial I/O, peripheral controllers, and high-speed math, without going to the expense of adding another full MULTIBUS board. The iSBX bus compatible boards enable users to buy exactly the capabilities they require for their MULTIBUS based systems, which keeps both system size and system cost at a minimum.

The MULTICHANNEL bus was created to provide users with a separate path for DMA I/O block transfers. The ability of new VLSI microprocessors to process data at very high rates necessitates the connection of numerous high-speed I/O devices to the system bus. The major problem with this approach is that the attachment of these burst-type peripherals can saturate a general purpose bus and reduce the computing performance of the system. The MULTICHANNEL bus was designed to eliminate this problem by providing for high speed (8 MB/sec) block transfers of data over an 8-/16-bit wide data path between peripherals and single board computer resources.

Development Support

Technical support has developed over time, and now offers a wide variety of development/debug tools, documentation, and training for users of MULTIBUS-based systems. These technical tools provide the means to design, debug and implement microcomputer software and hardware systems with minimal effort.

The Result

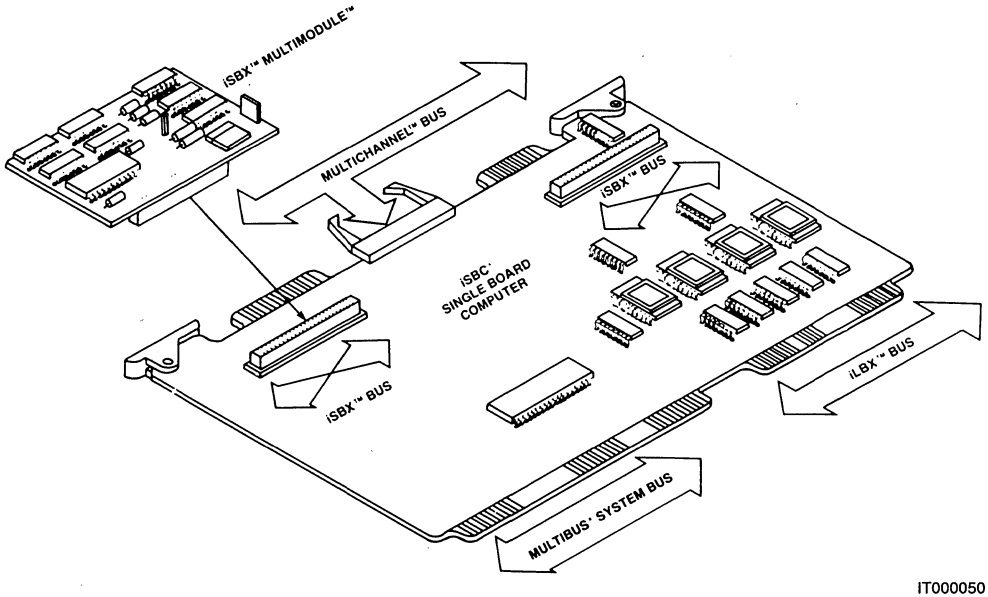
The continued evolution of the MULTIBUS standard, along with continued support and adherence by the market has made the MULTIBUS solution the fastest growing microcomputer system architecture in the board level marketplace. Its dominance of the 8-bit market and its growing influence in the 16-bit market is an example of its success as a true industry standard.

iLBX™ EXECUTION BUS

PRELIMINARY

- High bus bandwidth
  - 9.5 Mbytes/sec. for 8-bit transfers
  - 19 Mbytes/sec. for 16-bit transfers
- 16 Mbyte addressing range
- 8 and 16-bit data transfers
- Supports up to 5 iLBX™ compatible devices per bus
- Primary and secondary master bus exchange capabilities
- Standard 60-pin MULTIBUS® P2 connector

The iLBX™ Execution Bus is one of a family of standard bus structures resident within Intel's total system architecture. The Local Bus Extension (iLBX) Bus is a dedicated execution bus capable of significantly increasing system performance by extending the processor board's on-board local bus to off-board resources. This extension provides for arbitration-free, direct access to high-performance memory. Acting as a "virtual" iSBC®, up to 16 megabytes of processor addressable memory can be accessed over the iLBX bus and appear as though it were resident on the processor board. The iLBX Bus preserves advantages in performance and architecture of on-board memory, while allowing memory configurations larger than possible on a single board computer. High throughput and independence from MULTIBUS® activities make the iLBX bus an ideal solution for "working store" type program memory and data processing applications requiring large amounts of high performance memory. Such applications include graphics systems, robotics, process control, office systems, and CAD/CAM.



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FUNCTIONAL DESCRIPTION

Architectural Overview

The iLBX is an architectural solution for supporting large amounts of high performance memory. It is the first structure that allows the CPU board selection to be decoupled from the on-board memory requirement, and still maximizes the processor's performance potential. It eliminates the processor's need to access its off-board memory resources solely over the MULTIBUS system bus. Architectural consistency with the single board computer approach including iLBX memory can be maintained by dual port access of memory resources between the iLBX bus and the MULTIBUS system bus. This allows for global access by other processors and I/O devices while still providing high speed local CPU operations. This subsystem created by the iLBX bus of a single board computer and a maximum of 4 memory cards can be perceived architecturally as a "virtual single board computer". The implementation of iLBX bus "virtual modules" makes it possible to create functional modules with a new level of flexibility and performance in implementing a wide range of memory capabilities. With future needs in mind, the iLBX bus has the capability of accessing a full 16 megabytes of memory.

Structural Features

The iLBX bus uses a non-multiplexed 16-bit configuration capable of 8 and 16-bit transfers. Used in conjunction with the MULTIBUS interface, the iLBX bus resides on the MULTIBUS form factor P2 connector and supercedes the MULTIBUS interface definitions for the P2 signals. The iLBX bus uses the standard 60-pin MULTIBUS P2 connector and occupies 56 of the P2 connector pins with 16 data lines, 24 address lines plus control, command access, and parity signals. The four MULTIBUS address extension lines on the MULTIBUS/iLBX P2 connector retain the standard MULTIBUS interface definition.

Bus Elements

The iLBX bus supports three distinct device categories: 1) Primary Master, 2) Secondary Master, 3) Slave. These three device types may be combined to create several iLBX local busses ranging (in size) from a minimum of two to a maximum of five devices per iLBX bus. There is only one Primary Master in any given implementation of iLBX bus, and its presence is required along with the attachment of at least one Slave device. To provide alternate access over an iLBX bus, one optional Secondary Master may be incorporated to create a "two-master" local bus subsystem. By limiting the iLBX bus to two masters (a Primary and a Secondary), bus arbitration is reduced to a simple request and acknowledge process, with privileged use of the bus maintained by the Primary Master, and limited access granted to the Secondary Master when needed.

The Primary Master executes the role of iLBX bus "supervisor" by controlling the general operation of the bus and managing Secondary Master accesses to the Slave memory resources.

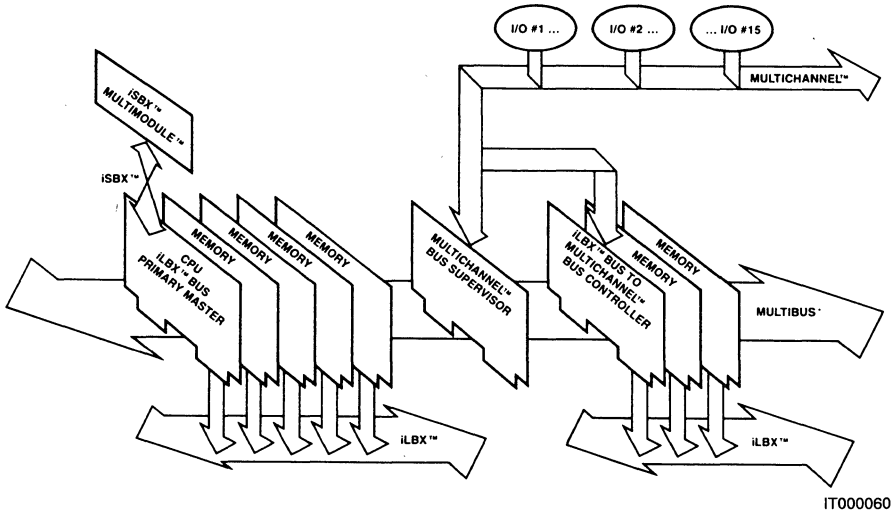
The Secondary Master Device is an option providing alternate access to the Slave resources on the iLBX bus. Secondary master devices are typically DMA driven. This feature is provided for implementation flexibility when occasional DMA transfers in and out of iLBX memory resources can optimize the overall system performance. The Secondary Master essentially duplicates the Primary Master's data transfer capability, but must rely on the Primary Master to grant access. Once access is granted, the Secondary Master controls the bus, and drives all signal lines until the operation is complete and control is passed back to the Primary Master.

The Slave devices contain the memory resources used by the Primary Master and the optional Secondary Master. Each iLBX implementation can contain a maximum of four Slave devices. Using 64K RAM technology on four slave devices with ECC can provide for over 2 megabytes of "on-board" high performance memory. With 256K RAM chips, each iLBX bus could contain slave devices with memory totalling 8 megabytes. As memory technology increases, the iLBX bus is designed to incorporate it in rapid fashion because it is capable of directly accessing a full 16 megabytes of memory on its high-performance Slave devices.

Bus Interface/Signal Line Descriptions

The iLBX bus interface is divided into four functional classes of signal lines: address and data lines, control lines, command lines, and bus access lines. The 40 address and data lines

Figure 1. MULTIBUS® System Architecture



defined by the iLBX Bus Specification consist of 16 data lines and 24 address lines.

There are 16 bi-directional data lines exclusively used to handle 8-bit and 16-bit data transfers between the active bus master and the selected slave device. The iLBX bus uses these data lines for all data transfers, and are driven by tri-state drivers.

The 24 address lines on the iLBX bus provide the ability to directly address 16 megabytes of memory. These single-direction address lines are exclusively driven by the active bus master. The iLBX bus master uses them to select a specific slave device. Three control lines specify the type of data transfer between master and slave devices, while the three command lines initiate, control, and terminate the transfer. There are also three bus access lines used to transfer bus control between master devices.

Bus Pin Assignments

The iLBX bus uses the standard 60-pin MULTIBUS P2 connector. The physical location of each pin assignment and its corresponding function is listed in Table 1. The four MULTIBUS address extension lines (pins 55-58 on the P2 connector) retain the standard MULTIBUS interface functions.

Bus Operation Protocol

The operation protocol for the iLBX bus is a straight-forward set of procedures consisting of three basic operations: bus control access, write data to memory, read data from memory. These operations use asynchronous protocol with positive acknowledgement.

Bus Access

The iLBX bus is shared by at most two masters; one Primary Master and one optional Secondary Master, each providing an alternate access path to iLBX bus memory resources. The mechanism for obtaining bus access is a simple request and acknowledge process communicated between masters. Each master is a bus controller of similar capabilities, responsible for data transfer operations between devices, but the Primary Master has the added responsibility of controlling iLBX bus accesses.

The Primary Master has default control of the iLBX bus. If the Secondary Master needs access to the bus, it must initiate a request and wait for acknowledgement from the Primary Master. The choice of when to surrender control of the bus rests with the Primary Master, but if no data transfer is in progress, the Primary Master normally relinquishes control immediately to the Secondary Master.

Data Transfer Operation

The iLBX bus supports two types of data transfer operations: write data to memory and read data from memory. These data transfer operations facilitate the passing of information between the active bus master and the selected slave device.

TABLE 1. iLBX™ Bus Pin Assignments, P2 Edge Connector

Component Side			Solder Side		
16-Bit Pin	**Mnemonic**	**Signal Name**	**16-Bit Pin**	**Mnemonic**	**Signal Name**
1	DB0	DATA LINE 0	2	DB1	DATA LINE 1
3	DB2	DATA LINE 2	4	DB3	DATA LINE 3
5	DB4	DATA LINE 4	6	DB5	DATA LINE 5
7	DB6	DATA LINE 6	8	DB7	DATA LINE 7
9	GND	GROUND	10	DB8	DATA LINE 8
11	DB9	DATA LINE 9	12	DB10	DATA LINE 10
13	DB11	DATA LINE 11	14	DB12	DATA LINE 12
15	DB13	DATA LINE 13	16	DB14	DATA LINE 14
17	DB15	DATA LINE 15	18	GND	GROUND
19	AB0	ADDRESS LINE 0	20	AB1	ADDRESS LINE 1
21	AB2	ADDRESS LINE 2	22	AB3	ADDRESS LINE 3
23	AB4	ADDRESS LINE 4	24	AB5	ADDRESS LINE 5
25	AB6	ADDRESS LINE 6	26	AB7	ADDRESS LINE 7
27	GND	GROUND	28	AB8	ADDRESS LINE 8
29	AB9	ADDRESS LINE 9	30	AB10	ADDRESS LINE 10
31	AB11	ADDRESS LINE 11	32	AB12	ADDRESS LINE 12
33	AB13	ADDRESS LINE 13	34	AB14	ADDRESS LINE 14
35	AB15	ADDRESS LINE 15	36	GND	GROUND
37	AB16	ADDRESS LINE 16	38	AB17	ADDRESS LINE 17
39	AB18	ADDRESS LINE 18	40	AB19	ADDRESS LINE 19
41	AB20	ADDRESS LINE 20	42	AB21	ADDRESS LINE 21
43	AB22	ADDRESS LINE 22	44	AB23	ADDRESS LINE 23
45	GND	GROUND	46	ACK*	SLAVE ACKNOWLEDGE
47	BHEN	BYTE HIGH ENABLE	48	R/W	READ NOT WRITE
49	ASTB*	ADDRESS STROBE	50	DSTB*	DATA STROBE
51	SMRQ*	SECONDARY MASTER REQUEST	52	SMACK*	SECONDARY MASTER ACKNOWLEDGE
53	LOCK*	ACCESS LOCK	54	GND	GROUND
55	ADR22*	MULTIBUS® ADDRESS EXTENSION LINE 22	56	ADR23*	MULTIBUS® ADDRESS EXTENSION LINE 23
57	ADR20*	MULTIBUS® ADDRESS EXTENSION LINE 20	58	ADR21*	MULTIBUS® ADDRESS EXTENSION LINE 21
59	RES	RESERVED	60	TPAR*	TRANSFER PARITY

The operation of these two transfer types is very similar; the only differences being the direction of the data transfer and the device driving the data lines.

For either type of data transfer, the active bus master first initiates the transfer operation by placing the memory address on the address lines (AB23-AB0) and a control configuration on the control lines to select the slave device. Once the slave device is selected, the type of data transfer becomes the key factor. With the write operation, the active master maintains control of the data lines and provides valid data within the specified time. Upon accepting a data element, the slave sends a receipt acknowledgment signal to the master which completes the data transfer operation.

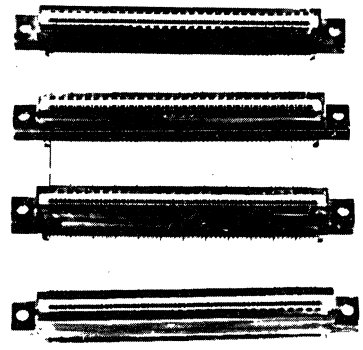
With the read operation, the slave device drives the data lines and places valid data on the data lines before sampling by the active master. The slave acknowledges the master to signal the end of the data transfer, and the master completes the operation.

The iLBX Bus Specification includes provisions for both optimized and non-optimized data transfers. Optimized operation uses pipelining and signal overlapping techniques to manage the data transfer timing relationships between the active bus master and the selected slave. The use of signal overlapping requires that every device attached to the iLBX bus provide a means for varying the timing of the slave request and acknowledge signals. The non-optimized operation uses fixed signal sequences, instead of signal overlapping, to assure a valid data transfer, and a device does not need a variable request or acknowledge to read data-valid timing on the iLBX bus. Please refer to the iLBX Bus Specification for detailed descriptions of these transfer operations.

Mechanical Implementation

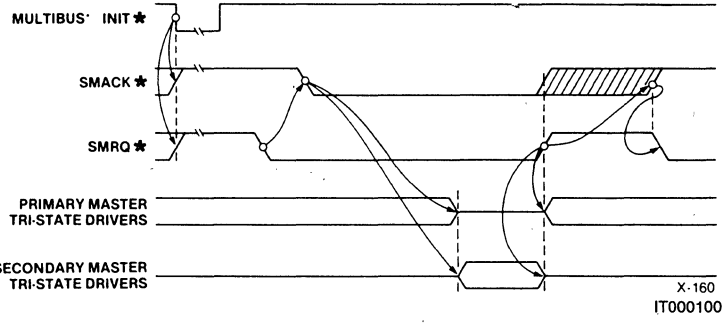
Because the iLBX bus uses the P2 connector of the MULTIBUS form factor, the iLBX bus "shares" a MULTIBUS chassis with the MULTIBUS backplane system bus in the system design. The iLBX mechanical specifications are synonymous with the MULTIBUS specifications for board-to-board spacing, board thickness, component lead length, and component height above the board. The iLBX bus interconnection can use either flexible ribbon cable or a rigid backplane. The iLBX bus interconnect maximum length is limited to 10 cm (approximately 4 inches); that is sufficient to span 5 card slots across two connected chassis. Figure 2 shows an iLBX bus cable assembly.

Figure 2. Typical iLBX™ Bus Interface Cable Assembly



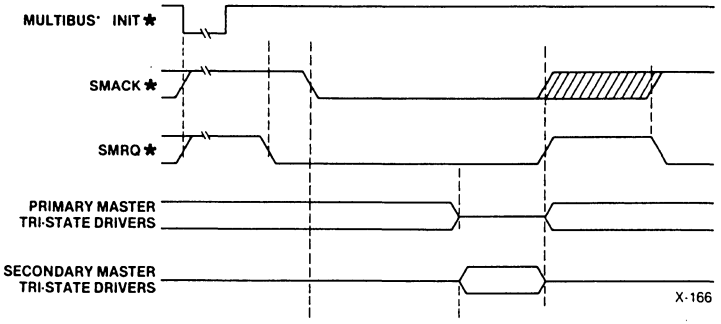
BUS TIMING

Figure 3. iLBX™ Bus Granting Time Chart



BUS TIMING

Figure 4. iLBX™ Bus Control Transfer Timing Chart



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16-Bit Transfer Timing —

Figure 5. Write Data-To-Memory (1 = 1)

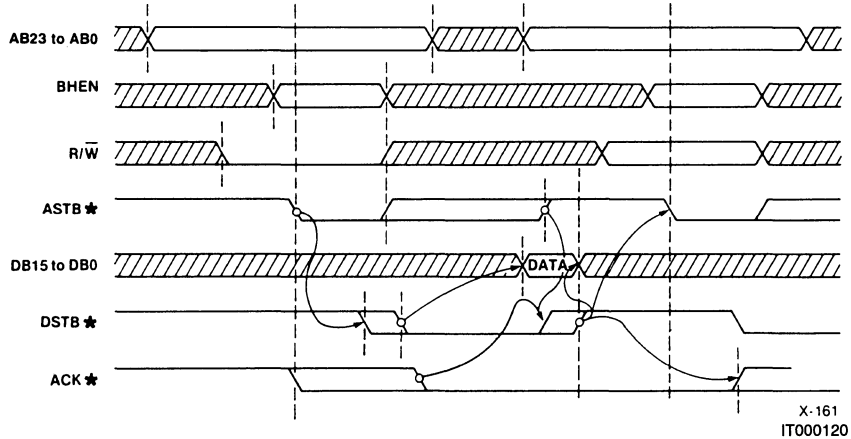

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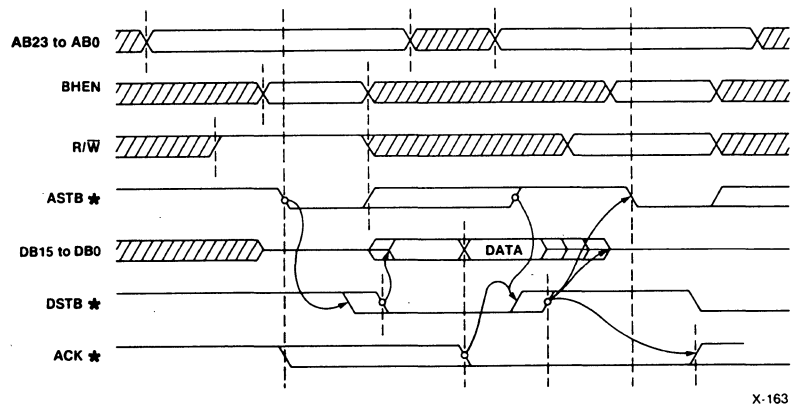
Figure 6. Read Data-From-Memory



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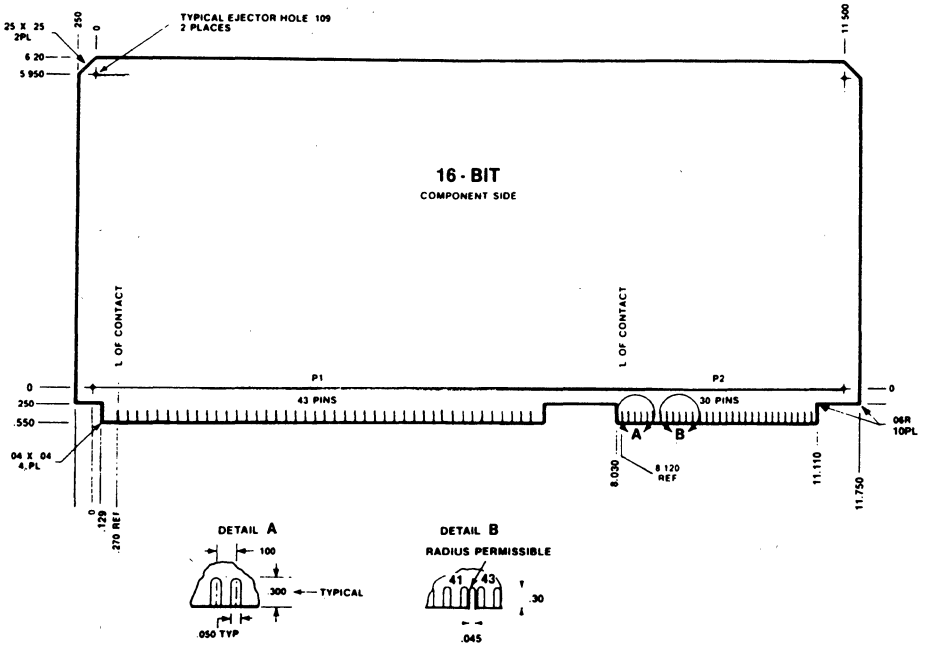
Physical Characteristics

Figure 7. iLBX™ Bus Standard Printed Circuit Board Outline



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SPECIFICATIONS

Word Size

Data – 8 and 16-bit

Memory Addressing

24-bits – 16 megabyte – direct access

Electrical Characteristics

DC Specifications

Bus Bandwidth

9.5 megabytes/sec—8-bit
19 megabytes/sec—16-bit

Table 2. DC Specifications

Signal Name	Driver Type	Termination (to +5 Vdc) At Master	Min. Driver Requirements			Max. Receiver Requirements		
			High	Low	Load Cap.	High	Low	Load Cap.
DB15-0	TRI-STATE	10K Ohms	0.4 ma	9 ma	75 pf	0.15 ma	2 ma	18 pf
TPAR*	TRI-STATE	10K Ohms	0.4 ma	9 ma	75 pf	0.15 ma	2 ma	18 pf
AB23-0	TRI-STATE	None	0.4 ma	20 ma	120 pf	0.10 ma	5 ma	30 pf
R/W	TRI-STATE	None	0.2 ma	8 ma	75 pf	0.05 ma	2 ma	18 pf
BHEN	TRI-STATE	None	0.2 ma	8 ma	75 pf	0.05 ma	2 ma	18 pf
LOCK*	TRI-STATE	None	0.2 ma	8 ma	75 pf	0.05 ma	2 ma	18 pf
SMRQ*	TTL	10K Ohms	0.05 ma	8 ma	20 pf	0.05 ma	2 ma	18 pf
SMACK*	TTL	None	0.05 ma	2 ma	20 pf	0.05 ma	2 ma	18 pf
†ASTB*	TRI-STATE	10K Ohms	0.2 ma	9 ma	75 pf	0.05 ma	2 ma	18 pf
†DSTB*	TRI-STATE	10K Ohms	0.2 ma	9 ma	75 pf	0.05 ma	2 ma	18 pf
ACK*	OPEN COLL.	330 Ohms	N.A.	20 ma	45 pf	0.05 ma	2 ma	18 pf

†At slave, series RC termination to GND (100 ohm, 10 pf)

Cables and Connectors

Table 3. Cable and Receptacle Vendors

iLBX™ Bus Compatible Cable		
Vendor	**Vendor Part No.**	**Conductors**
T&B Ansley	171-60	60
T&B Ansley	173-60	60
3M	3365/60	60
3M	3306/60	60
Berg	76164-060	60
Belden	9L28060	60
Spectrastrip	455-240-60	60
iLBX™ Bus Compatible Receptacles		
Vendor	**Vendor Part No.**	**Pins**
Kelam	RF30-2803-5	60
T&B Ansley	A3020 (609-6025 modified)	60

Environmental Characteristics

Operating

Temperature – 0°C to 55°C
Relative Humidity – 0 to 85 percent; non-condensing

Reference Manuals

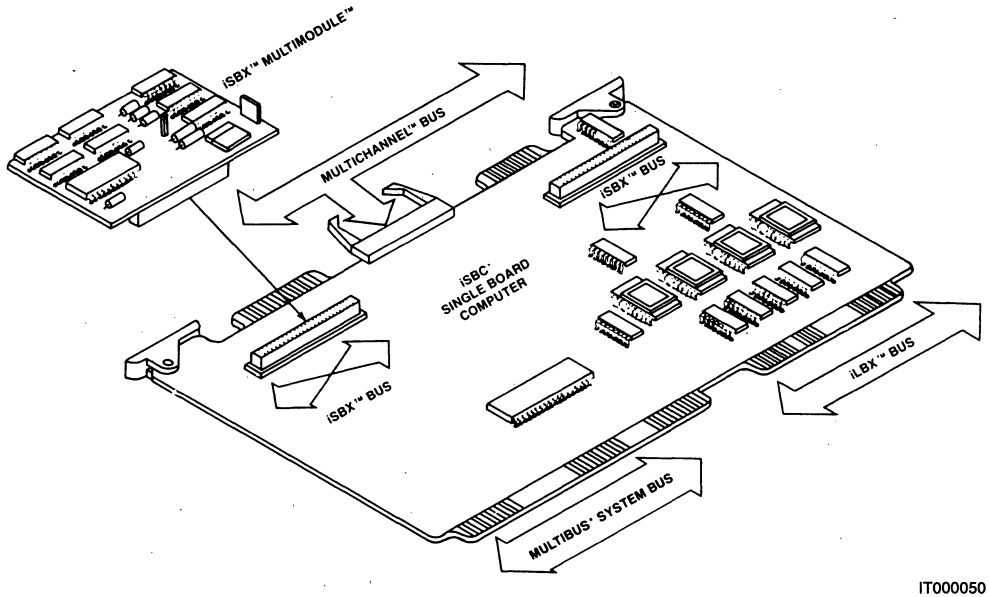
210883 – MULTIBUS Handbook

MULTICHANNEL™ I/O BUS

PRELIMINARY

- High speed 8- or 16-bit block transfers between memory and/or I/O
- Transfer rates up to 8 megabytes/sec.
- Full speed operation at distances of up to 15 meters.
- Supports Supervisor, Controller, or basic Talker/Listener capabilities
- Off-loads burst mode I/O activities from host CPU and MULTIBUS® system bus
- Up to 16 devices may be interfaced to the bus.
- 16 megabytes of memory and 16 megabytes of I/O are addressable on each device.

The MULTICHANNEL™ I/O Bus is one of a family of standard bus structures resident within Intel's total system architecture. The MULTICHANNEL bus is a general purpose, high-speed I/O bus capable of significantly increasing system performance by providing a separate data path for DMA I/O activities. By isolating I/O transfers from the system bus, the MULTICHANNEL bus off-loads I/O activity from the host CPU, reduces the probability of bus saturation on the system bus, and reduces contention between I/O and data processing activities on the system bus. The MULTICHANNEL bus can support up to 16 devices at distances up to 15 meters with a maximum burst throughput of 8 megabytes per second. These 16 devices are classified in a manner similar to the IEEE 488 bus concept: Supervisors, Controllers, or Talker and Listeners. As a non-proprietary, standardized I/O bus, the MULTICHANNEL bus is a cost-effective DMA interface ideal for applications such as computer graphics, specialized peripheral control, automatic test equipment, video camera image processing, data acquisition, and high-speed MULTIBUS® system-to-system communication.



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MULTICHANNEL is a trademark of Intel Corporation.

FUNCTIONAL DESCRIPTION

Architectural Overview

The MULTICHANNEL bus is the standard high speed I/O interface to MULTIBUS-based systems. Its general purpose design and high performance (8 MB/sec) augment the overall system design by improving I/O interface flexibility and system throughput. The flexibility is realized by using an easy-to-use public standard interface that can support up to sixteen 8-bit or 16-bit devices at up to 15 meters. This structure allows the MULTICHANNEL bus to provide easy I/O system expansion, effective box-to-box communication, and a growth path capable of supporting new generations of high-performance I/O devices. The MULTICHANNEL bus increases system throughput by providing a high-performance data path for efficient movement of large amounts of data.

Structural Features

MULTICHANNEL™ BUS CONFIGURATION

The MULTICHANNEL bus is a multiplexed, asynchronous block transfer, 16-bit I/O bus designed to handle 8-bit and 16-bit transfers between peripherals and single board computers. Its structure (pictured in Figure 2) consists of 16 address/data lines, 6 control lines, 2 interrupt lines, plus parity and reset. These signal lines are implemented as either a 60 conductor flat ribbon cable or a twisted-pair cable spanning a distance of up to 15 meters. A 30/60-pin 3M® connector is recommended for device connection to the MULTICHANNEL bus. The male connectors are installed on each MULTICHANNEL device and the female connectors are mounted on the cable. To insure system integrity, the MULTICHANNEL cable is terminated at both ends.

BUS ELEMENTS

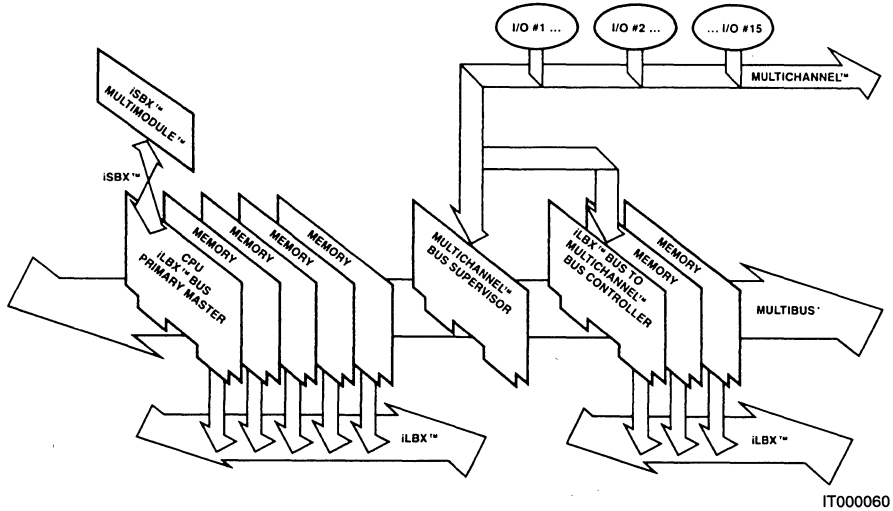
Three device types—The Basic device, the bus Controller device, and the bus Supervisor device—each provide a different level of capability. The Basic Talker/Listener device has lowest capability, responding only to data transfer requests issued by a Supervisor or Controller. The bus Controller device has higher capability than a Basic Talker/Listener on the bus. It can respond to data transfer requests, control data transfers, and can program other MULTICHANNEL devices under direction from a bus Supervisor. Operating at the highest capability is the bus Supervisor device. It provides major control and management of the MULTICHANNEL bus. The bus Supervisor resolves and grants MULTICHANNEL bus priority, monitors bus status, handles interrupts, and controls the reset line, in addition to performing all bus Controller functions.

MULTICHANNEL bus devices are functionally flexible, creating overlaps between types of bus functions and types of bus devices performing those functions. These devices perform functions in various states of operation: master, slave, talker, listener. When a device is controlling the command/action lines, it is in the master state, and both the bus Supervisor and the bus Controller can operate in this state, although not simultaneously. The slave state indicates a device that can monitor the command/action lines. Only Controllers and Basic Talker/Listeners operate as slaves. All three device types can operate in the talker state or the listener state, but not all at the same time. A Talker is any device selected by the bus master which is writing data to the bus. A Listener is any selected device which is reading data from the bus.

BUS INTERFACE/SIGNAL LINE DESCRIPTIONS

The MULTICHANNEL bus signal lines are grouped into five classes based on the functions they perform: address/data, control, interrupt, parity, and reset. The 16 address/data lines are multiplexed by a control line to act either as 16 unidirectional address lines or 16 bidirectional data lines. When used as address lines, they transmit the device address to all devices attached to the MULTICHANNEL bus. When used as bidirectional data lines, they transmit and receive data to or from MULTICHANNEL devices. The six control lines determine the overall operation of the bus from specifying the type of data transfer to providing the handshake for data transfers between MULTICHANNEL devices. Two interrupt lines are supplied to initiate and terminate data transfers, and to indicate device failures, memory failures, or parity errors. A parity line and a reset line provide support for a parity option and system reset capability whenever required.

Figure 1. MULTIBUS® System Architecture



3M is a registered trademark of 3M Corporation.

BUS PIN ASSIGNMENTS

For proper MULTICHANNEL implementation, a 60 conductor (twisted pair or flat) cable using a 30/60 pin 3M connector, is used for device connection to the bus. Figure 3 is an outline drawing of the iSBC® MULTICHANNEL connector which also shows the pin numbering. The MULTICHANNEL bus connector signal pin assignments are listed in Table 1. Cable termination is implemented at both cable ends to insure proper system integrity over a 15-meter cable. Figure 4 is a schematic of the cable termination circuits. A cable termination module could be created that would then be connected to the cable end via a 30/60 pin connector.

Figure 2. Block Diagram of MULTICHANNEL™ Bus Structure

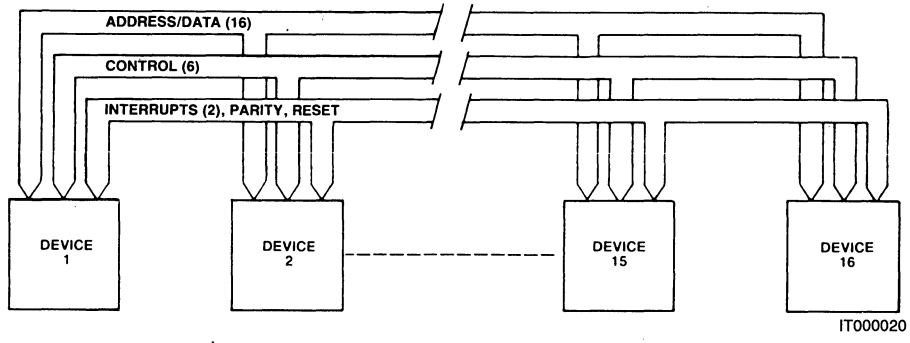


Figure 3. Connector Example

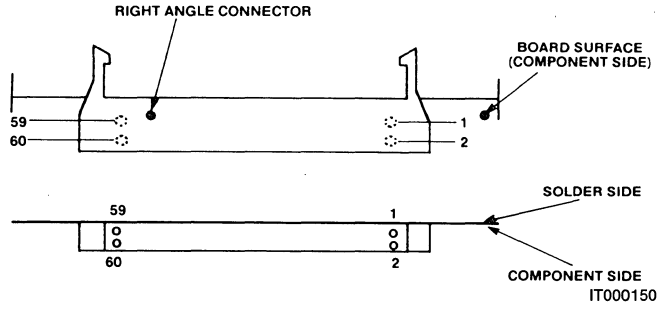
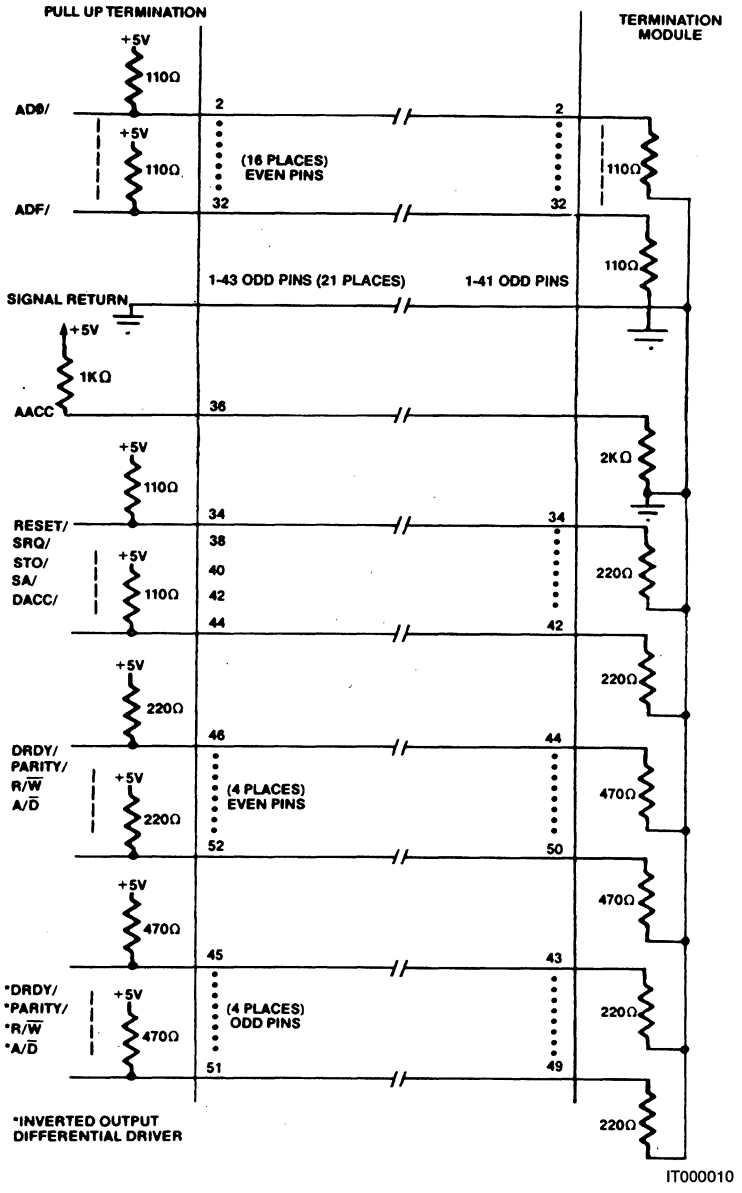


TABLE 1. MULTICHANNEL™ Bus Pin Assignments

Lower Row			Upper Row		
Pin	**Mnemonic**	**Signal Name**	**Pin**	**Mnemonic**	**Signal Name**
1	GND	GROUND	2	AD0/	ADDRESS DATA LINE 0
3	GND	GROUND	4	AD1/	ADDRESS DATA LINE 1
5	GND	GROUND	6	AD2/	ADDRESS DATA LINE 2
7	GND	GROUND	8	AD3/	ADDRESS DATA LINE 3
9	GND	GROUND	10	AD4/	ADDRESS DATA LINE 4
11	GND	GROUND	12	AD5/	ADDRESS DATA LINE 5
13	GND	GROUND	14	AD6/	ADDRESS DATA LINE 6
15	GND	GROUND	16	AD7/	ADDRESS DATA LINE 7
17	GND	GROUND	18	AD8/	ADDRESS DATA LINE 8
19	GND	GROUND	20	AD9/	ADDRESS DATA LINE 9
21	GND	GROUND	22	ADA/	ADDRESS DATA LINE 10
23	GND	GROUND	24	ADB/	ADDRESS DATA LINE 11
25	GND	GROUND	26	ADC/	ADDRESS DATA LINE 12
27	GND	GROUND	28	ADD/	ADDRESS DATA LINE 13
29	GND	GROUND	30	ADE/	ADDRESS DATA LINE 14
31	GND	GROUND	32	ADF/	ADDRESS DATA LINE 15
33	GND	GROUND	34	RESET/	RESET
35	GND	GROUND	36	AACC	ADDRESS MODE ACCEPT
37	GND	GROUND	38	SRQ/	SERVICE REQUEST
39	GND	GROUND	40	STO/	SUPERVISOR TAKE OVER
41	GND	GROUND	42	DACC/	DATA MODE ACCEPT
43	GND	GROUND	44	SA/	SUPERVISOR ACTIVE
45	PB*/	PARITY BIT (INV.)	46	PB/	PARITY BIT
47	R/W/	READ NOT WRITE (INV.)	48	R/W	READ NOT WRITE
49	A/D/	ADDRESS NOT DATA (INV.)	50	A/D	ADDRESS NOT DATA
51	DRDY*/	DATA READY (INV.)	52	DRDY/	DATA READY
53	RES	RESERVED	54	RES	RESERVED
55	RES	RESERVED	56	RES	RESERVED
57	RES	RESERVED	58	RES	RESERVED
59	RES	RESERVED	60	RES	RESERVED

Figure 4. Bus Termination Schematic



Bus Operation Protocol

DATA TRANSFER OPERATION

There are three modes of communication in the operation protocol: address mode, data mode, and control transfer mode. Using these transfer modes, each MULTICHANNEL device provides handshaking capability for totally asynchronous block data transfers. Address mode is the time when the address/data control line is high. Information placed on the address/data lines of the MULTICHANNEL bus as two successive 16-bit words is interpreted to select or deselect a device on the bus and address the specific resource on the device. Typically, these address mode transfers are only 2 word sequences. Figure 5 is a timing diagram of the handshake routine in address mode. The data mode is the time when the address/data control line is low. Valid data is placed on the address/data lines of the bus and can occur only after an address mode has been performed. Transfers during data mode are usually large quantities of either 8-or 16-bit data, and are passed to or from the addressed device until it is deselected. Figure 6 is a timing diagram of a data transfer sequence.

Control transfer mode is the time when the bus Supervisor selects the bus Controller and programs its registers with required information. Once programmed, a bus Controller may select a device and originate a data transfer operation.

The operational sequences of these transfer modes are similar in handling read and write operations to and from the 16 megabytes of memory and the 16 megabytes of registers addressable on each MULTICHANNEL device.

A typical transfer sequence begins when the master sends a two-word address sequence to select a MULTICHANNEL device and specify address, direction and resource (memory vs. I/O) of the data transfer. Following device selection, the Talker proceeds to send the data as a continuous 8 or 16-bit data word stream until the block data move is complete. The master terminates the transfer by issuing another two-word address sequence for device deselection.

The transfer sequence described is identical for both memory and register type transfers. The master controls similar read

Figure 5. MULTICHANNEL™ Bus Address Cycle

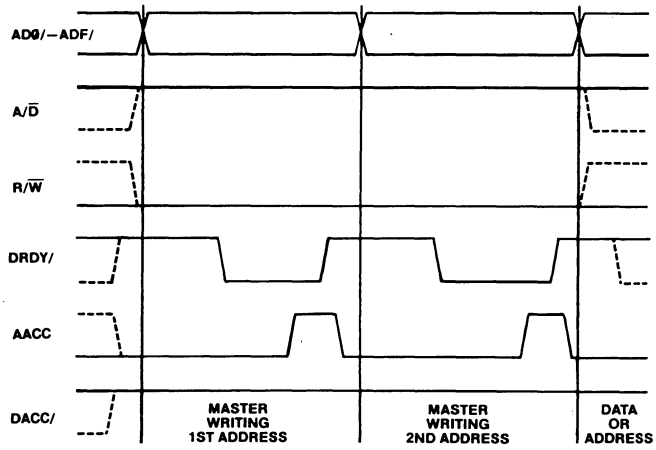
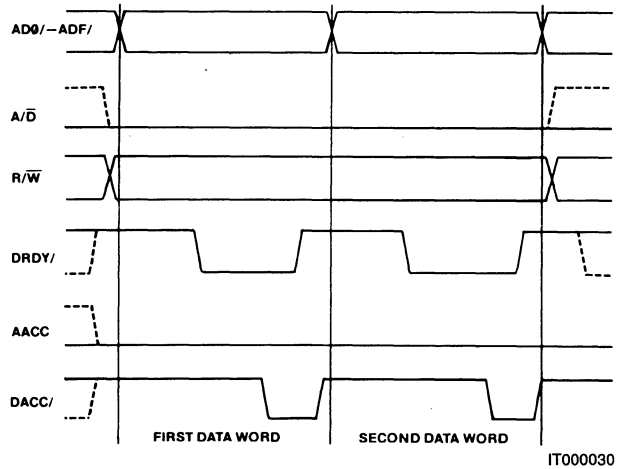


Figure 6. MULTICHANNEL™ Bus Data Transfer Sequence



and write operations between devices, and the address select and deselect sequences use the same address format. Figure 7 contains the MULTICHANNEL bus address format.

DEVICE REGISTER DEFINITION

Of the 16 megabytes of register space per device, the first 16 registers are pre-defined to provide a standard register area common to all devices. The remaining registers are user definable. Table 2 lists the 16 defined registers along with their function. The use of this register concept allows for standard interface between all MULTICHANNEL devices. Please refer to the MULTICHANNEL Bus Specification for more detailed information.

TABLE 2. MULTICHANNEL™ Device Register Definitions

Register Number	Definition	Mode
0	STO/Flag/Status	Read Only
1	SRQ/Flag/Status	Read Only
2	SRQ/Mask	Write Only
3	Device Command	Write Only
4	Device Parameter	Write Only
5	Data Address 1	Read or Write
6	Data Address 2	Read or Write
7	Block Length 1	Read or Write
8	Block Length 2	Read or Write
9	Error Address 1	Read Only
10	Error Address 2	Read Only
11	Address Extension	Write Only
12-15	Reserved	
16-16 Mbyte	User Defined	Read or Write

BUS INTERRUPT HANDLING

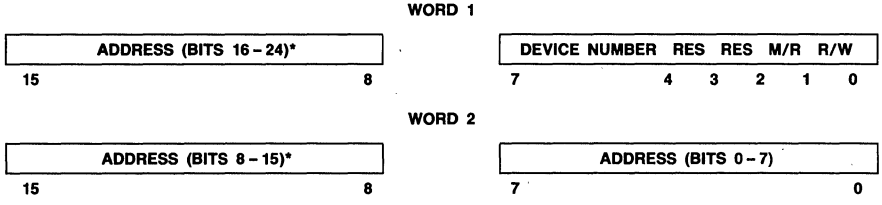
The MULTICHANNEL bus Supervisor, being responsible for bus access and control, monitors the two bus interrupt lines. The Supervisor Take-Over interrupt (STO) is used to inform the bus Supervisor that a device wants to return control of the bus to the Supervisor or that an error has occurred. The Service Request Interrupt (SRQ) is used by devices which do not have control of the bus, but require service from the bus Supervisor. To locate a device transmitting a bus interrupt, the bus Supervisor polls each device attached to the bus by reading the appropriate register of each device and testing for a nonzero value. In current implementations, the Supervisor polls each device only once. If the interrupt is not removed an error occurs.

Parity and Reset

Parity operation on the MULTICHANNEL bus is provided, but is not required. The bus Supervisor selects between parity mode and non-parity mode depending upon system requirements. If parity mode is selected all Talkers must generate odd parity. All active Listeners monitor the parity line and generate an STO interrupt signal if there is a parity error.

A reset function is also supported by the MULTICHANNEL bus, and is controlled by the bus Supervisor to bring the bus to a known state. It is used to reset all devices after power-up, and when required to gain control of the bus.

Figure 7. MULTICHANNEL™ Bus Address Format



WHERE:

ADDRESS (BITS 16 – 24) = MOST SIGNIFICANT BYTE OF 24 BIT MEMORY OR REGISTER ADDRESS
DEVICE NUMBER = A DEVICE NUMBER FROM 0 TO 15
RES = RESERVED BIT
M/R = MEMORY/REGISTER ADDRESS
R/W = READ/WRITE BIT
ADDRESS (BITS 8 – 15) = MIDDLE BYTE OF 24 BIT MEMORY OR REGISTER ADDRESS
ADDRESS (BITS 0 – 7) = LEAST SIGNIFICANT BYTE OF 24 BIT MEMORY OR REGISTER ADDRESS
*** = THESE BITS ARE UNDEFINED WHEN 8-BIT ADDRESSING IS USED**

SPECIFICATIONS

Word Size

Data — 8, 16-bit

Memory Addressing

24-bits — 16 megabyte – direct access – automatic incrementing

Register Addressing

24-bits — 16 megabyte – direct access

Electrical Characteristics

DC SPECIFICATIONS

Maximum Bus Length

15 meters (50 feet)

Bus Devices Supported

16 total devices — (Supervisor, Controller, and Talker/Listener)

Bus Bandwidth

8 megabytes/sec. — 16-bit
4 megabytes/sec. — 8-bit

Table 3. DC Specifications

Signal Name	Driver Type	Termination (see Note)	Min. Driver Requirements			Max. Receiver Requirements		
			High	Low	Load Cap	High	Low	Load Cap
AD15-0/	TRI-STATE	110 Ohms	– 5 ma	48 ma	300 pf	0.2 ma	0.8 ma	15 pf
SA/	OPEN COLL	110/220 Ohms	N.A.	48 ma	300 pf	0.4 ma	0.6 ma	15 pf
RESET/	OPEN COLL	110/220 Ohms	N.A.	48 ma	300 pf	0.4 ma	0.6 ma	15 pf
AACC	OPEN COLL	1K/2K Ohms	N.A.	48 ma	300 pf	0.4 ma	0.6 ma	15 pf
DACC/	OPEN COLL	110/220 Ohms	N.A.	48 ma	300 pf	0.4 ma	0.6 ma	15 pf
SRQ/	OPEN COLL	110/220 Ohms	N.A.	48 ma	300 pf	0.4 ma	0.6 ma	15 pf
STO/	OPEN COLL	110/220 Ohms	N.A.	48 ma	300 pf	0.4 ma	0.6 ma	15 pf
R/W	DIF, NON-INV	220/470 Ohms	–20 ma	40 ma	300 pf	0.5 ma	0.5 ma	15 pf
R/W/	DIF, INV	470/220 Ohms	–20 ma	40 ma	300 pf	0.5 ma	0.5 ma	15 pf
A/D	DIF, NON-INV	220/470 Ohms	–20 ma	40 ma	300 pf	0.5 ma	0.5 ma	15 pf
A/D/	DIF, INV	470/220 Ohms	–20 ma	40 ma	300 pf	0.5 ma	0.5 ma	15 pf
PB/	DIF, NON-INV	220/470 Ohms	–20 ma	40 ma	N.A.	0.5 ma	0.5 ma	N.A.
PB*/	DIF, INV	470/220 Ohms	–20 ma	40 ma	N.A.	0.5 ma	0.5 ma	N.A.
DRDY/	DIF, NON-INV	220/470 Ohms	–20 ma	40 ma	N.A.	0.5 ma	0.5 ma	N.A.
DRDY*/	DIF, INV	470/220 Ohms	–20 ma	40 ma	N.A.	0.5 ma	0.5 ma	N.A.

NOTE: Termination provided only at the physically ends of the interconnect cable. Where the positive termination (pull-up) resistance is different from the negative termination (pull-down) resistance, the positive termination resistance is listed first.

BUS TIMING

Figure 8. Address-Read-Address-Write Cycles

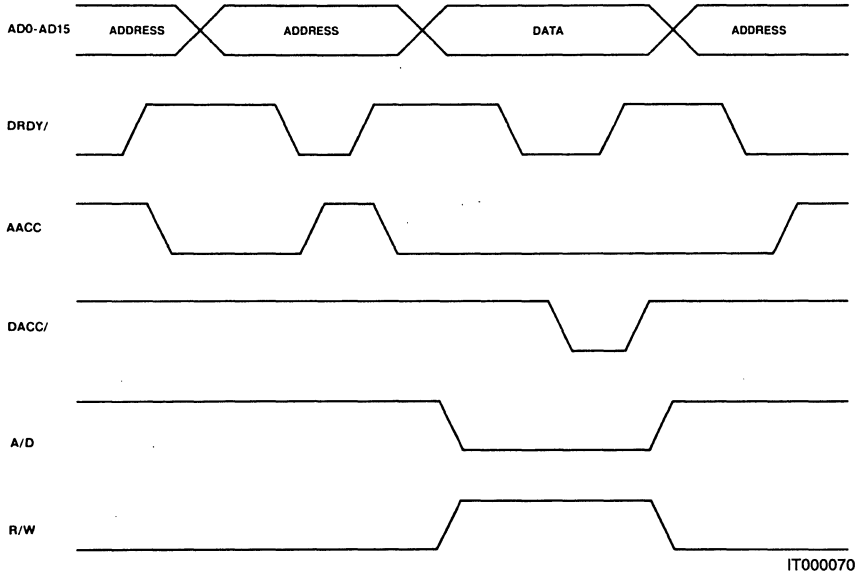
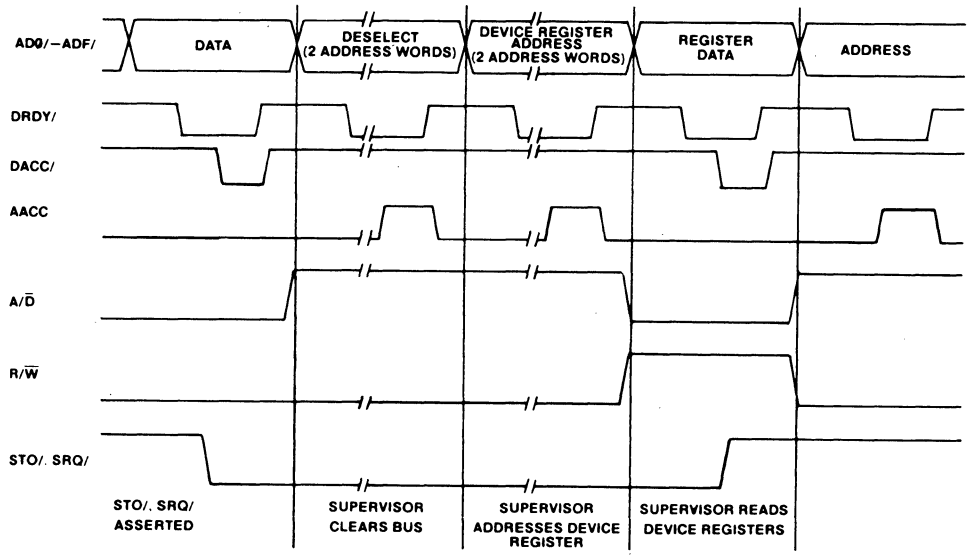


Figure 9. Supervisor Interrupt Timing



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Cables and Connectors

Table 4. Cable and Receptacle Vendors

MULTICHANNEL™ Bus Compatible Cable			
Vendor	**Ribbon Type**	**Vendor No.**	**Conductor**
Belden	Plain Flat	9L28060	60
Belden	Twisted-Pair	9V28060	60
Belden	Insulated Flat	9L28260	60
Spectrastrip	Plain Flat	455-240-60	60
Spectrastrip	Twisted-Pair	455-248-60	60
Spectrastrip	Insulated Flat	151-2830-060	60
MULTICHANNEL™ Bus Compatible Receptacles			
Vendor	**Type**	**Vendor No.**	**Pins**
Berg	Male	65823-103	60
Berg	Female	65949-960	60
3M	Male	3372-1302	60
3M	Female	3334-6000	60

PHYSICAL PROPERTIES

Conductors — 28 AWG, 7/36 strand, tinned copper
Conductor Insulation — 0.010 inch wall, nominal
Conductor Spacing — Twisted pair – 0.10 inch, nominal; Flat – 0.050 inch, ±10%
Cable Thickness — Flat – 0.042 inch, nominal
Temperature Rating — 80°C

ELECTRICAL PROPERTIES

Impedance (nominal) — 105 ohms ±10%
Propagation Velocity (nominal) — 1.7 ns/ft
Capacitance (nominal) — 22 pf/ft

INSULATION REQUIREMENTS

Voltage Rating(minimum) — 100 Vdc
Insulation Resistance (minimum) — 1×10^{10} ohms

Environmental Characteristics

Temperature — 0°C – 55°C
Humidity — 90% max. relative (no condensation)

Reference Manuals

210883 — MULTIBUS Architecture Handbook

General Information Index

ONE YEAR WARRANTY and RAPID EXCHANGE SERVICE (RES[SM])

Advanced Micro Devices now offers a One Year Warranty * and a new Field Service called Rapid Exchange Service (RES)** on all Microcomputer System products listed below.

RES ensures that any Customer with a field service problem on the products listed will be able to contact AMD's MCS Field Service Department directly to determine which module is failing and is then guaranteed that a replacement module will be shipped within 24 hours via Federal Express. The Customer must return the defective module, at his own expense, to AMD Field Service within one week. If not received within this period, the Customer will be billed, at list price, for the module shipped to him.

The following numbers may be used to contact the Field Service Department: (408) 749-5394, (408) 732-2400, ext. 5394, or toll free (outside of California – within Continental U.S.): (800) 538-8450, ext. 5394

All products listed are covered by a One Year Warranty. If the module exchange occurs within this one year warranty period, the RES is free of charge. At the end of the one year period, each faulty module can be sent to the factory for repair on a "fixed-cost basis." A Before Return Replacement (BRR) Service is also available after the warranty period expires (consult Field Service regarding BRR Service).

Products covered are as follows:

MULTIBUS BOARDS — CARD CAGES AND SYSTEM CHASSIS

94/0350	95/6448	96/6130	97/1024B
94/0351	95/6450	97/0032	97/8605/005
94/1530	95/6450/200	97/0064	97/8605/008
94/1541	95/6452A	97/0128	97/8605/010
94/2000	95/6452/200	97/0256	97/8605/105
95/6120	96/0000L	97/0343	97/8605/500
95/6440	96/3500/100	97/0512	
95/6440/100	96/4126	97/0512B	
95/6445	96/5232	97/0768B	

MICROPROGRAM/BIT-SLICE SUPPORT DEVELOPMENT SYSTEMS

29/2065	29/6312	29/8491	29/8656
29/2910B	29/8210A	29/8652	29/9915
29/2915	29/8250	29/8653	29/9929
29/6310	29/8480	29/8654	

*Other Microcomputer Systems' products not listed have a 90 day warranty. AMD's Warranty covers the original purchase of the product and is not transferrable. Customers may be required to provide Date of Purchase proof to determine warranty coverage.

**RES is available *only* to Customers within the Continental United States. For Customers outside of the U.S., the Return for Replacement Service (with a two week turnaround) will continue to be in effect. RES covers the original purchase of the product and is not transferrable.

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Phoenix, Arizona 85021
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Suite 5000
Newport Beach, California 92660
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Advanced Micro Devices
21600 Oxnard Street, Suite 675
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Tel: (213) 992-4155

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9619 Chesapeake Drive #210
San Diego, California 92123
Tel: (619) 560-7030

NORTHWEST AREA

Advanced Micro Devices
1245 Oakmead Parkway
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Tel: (408) 720-8811

Advanced Micro Devices
1873 South Bellaire Street
Suite 920
Denver, Colorado 80222
Tel: (303) 691-5100

NORTHWEST AREA (Con't.)

Advanced Micro Devices
One Lincoln Center, Suite 230
10300 Southwest Greenburg Road
Portland, Oregon 97223
Tel: (503) 245-0080

Advanced Micro Devices
Honeywell Ctr., Suite 1002
600 108th Avenue N.E.
Bellevue, Washington 98004
Tel: (206) 455-3600

MID-AMERICA AREA

Advanced Micro Devices
500 Park Boulevard, Suite 940
Itasca, Illinois 60143
Tel: (312) 773-4422

Advanced Micro Devices
9900 Bren Road East, Suite 601
Minnetonka, Minnesota 55343
Tel: (612) 938-0001

Advanced Micro Devices
3592 Corporate Drive, Suite 108
Columbus, Ohio 43229
Tel: (614) 891-6455

Advanced Micro Devices
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Two Park North, Suite 385
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Tel: (512) 346-7830

Advanced Micro Devices
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Dallas, Texas 75240
Tel: (214) 934-9099

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290 Elwood Davis Road
Suite 316
Liverpool, New York 13088
Tel: (315) 457-5400

Advanced Micro Devices
Waterview Plaza Suite 303
2001 U.S. Route #46
Parsippany, New Jersey 07054
Tel: (201) 299-0002

Advanced Micro Devices
110 Gibralter Road #110
Horsham, Pennsylvania 19044
Tel: (215) 441-8210
TWX: 510-665-7572

Advanced Micro Devices
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5100 Tilghmant Street, Suite 320
Allentown, Pennsylvania 18104
Tel: (215) 398-8006
FAX: 215-398-8090

Advanced Micro Devices
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Tel: (914) 471-8180
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