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AmZ8000 16-Bit
MonoBoard™ Computer

User's Manual

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PREFACE

This manual provides general information, an installation and interface guide, programming information, principles of operation, and service information for the Advanced Micro Computers Am96/4116A MonoBoard Computer. Additional information concerning components of the Am96/4116A is available in the following documents:

- AmZ8001/2 Processor Instruction Set
- Zilog, Z8001 CPU/Z8002 CPU Product Spec.
- AMD Shottky and Low Power Shottky Data Book
- Am8251-Am9551 Data Sheet
- Am8255A/Am8255A-5 Data Sheet
- Am9513 Data Sheet
- Am9513 Application Brief
- 8259A Data Sheet (Intel)
- Multibus† Interfacing (Intel Application Note AP-28A)

In this manual, both active-high (positive true) and active-low (negative true) signals appear in the text. To eliminate confusion and simplify presentation, the following convention is used throughout this manual. The mnemonic for a signal that is active-low is followed by an asterisk (i.e. MEMR*). The mnemonic for an active-high signal is denoted without the asterisk suffix.

Common mnemonics and acronyms are used without additional explanation. The first time a non-standard or uncommon acronym is used, its full name will be spelled out and the acronym enclosed in parenthesis. Following references will use the acronym without further explanation.

The information in this manual is believed to be accurate and complete at the time it was printed. AMC reserves the right to change specifications without notice. No responsibility is assumed for errors that might appear in this manual.

†Multibus a registered trademark of Intel Corporation

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CHAPTER 1
GENERAL INFORMATION

INTRODUCTION

The Am96/4116A MonoBoard Computer (MBC) is a complete, AmZ8002 based, 16-bit, microcomputer on a single board. It is plug compatible with the Intel Multibus board product interface. The Am96/4116A offers the following features:

- High performance, AmZ8002, 16-bit microprocessor.
- Supports up to eight kilobytes of on-board ROM. Two sockets are provided with jumper selectable addressing for 2K, 4K, or 8K bytes.
- Under software control, addresses for on-board shadow ROM are mapped to off-board RAM.
- Supports up to 32 kilobytes of on-board dynamic RAM.
- Two-port configuration of RAM. RAM can be simultaneously accessed by the AmZ8000 and the Multibus. If both are attempting continuous access, 50% interleave results.
- Eight fully-programmable, vectored, priority interrupt channels with provisions for software generated interrupts. 24 sources.
- Two Serial Communications Interfaces, one with full RS232C support and the other with modified RS232C support.
- A parallel I/O interface with two 8-bit ports and two 4-bit ports socketed for drivers or receivers.
- Programmable Timer for on-board time-of-day clock and delayed interrupts.

PHYSICAL DESCRIPTION

The Am96/4116A MonoBoard Computer (MBC) is a four-layer printed circuit board with MSI TTL and LSI MOS circuits. Five edge connectors provide bus and peripheral interface capabilities. Physical characteristics of the Am96/4116A are:

Board Dimensions:

Width	30.48 cm (12.00 inches)
Depth	17.15 cm (6.75 inches)
Thickness	1.50 cm (0.60 inches)

Environmental Requirements:

Operating Temperature	0°C to 55°C
Relative Humidity	Up to 90% without condensation
Storage Temperature	-40°C to +75°C

FUNCTIONAL DESCRIPTION

The Am96/4116A MonoBoard Computer contains an AmZ8002 CPU, two Am9551 serial ports, one Am8255A parallel I/O port, an Am9513 timer, an 8259A interrupt controller, 32 kilobytes of RAM, two sockets for 2K, 4K, or 8K of ROM, and various TTL circuits. The board is compatible with the Multibus interface requirements. The AmZ8002 CPU is an advanced architecture, 16-bit microprocessor with an instruction set more powerful than many minicomputers. There are sufficient resources, such as sixteen 16-bit general purpose registers, seven data types, eight addressing modes, and 110 distinct instruction types. The 110 distinct instructions can be combined with the various data types and addressing modes to expand the instruction set to 414 instructions. Most instructions can use any of the five addressing modes and can operate on byte (8-bit), word (16-bit), and long-word (32-bit) data types. Figure 1-1 is a block diagram of the Am96/4116A.

Selection of ROM is optional. Two sockets are provided to accommodate ROM. The ROM type can be Am2708 or Am2758 (2 kilobytes), Am2716 or Am9218 (4 kilobytes), or Am2732 or Am9233 (8 kilobytes). Jumpers are provided to select the correct ROM addressing scheme to accommodate the various ROMs. Addresses for the Am2708 range from 0 through 07FFH; the Am2716 addresses range from 0 through 0FFFH; and the Am2732 addresses range from 0 through 1FFFH.

The ROM addressing range is 8,192 bytes. If 2 kilobyte or 4 kilobyte ROM is implemented, the unused address space, from 0800 to 1FFFH or 1000 to 1FFFH, for 2 kilobyte or 4 kilobyte ROM, respectively, will be mapped to off-board RAM.

All ROM on the Am96/4116A MonoBoard Computer is Shadow ROM. A Write instruction addressed to port FFF0H disables on-board ROM and causes memory access to addresses 0 through 1FFFH to be mapped to off-board. Either ROM or RAM can be used as off-board memory; both read and write operations at the off-board memory are allowed, even though a write operation when ROM is used is meaningless. A Write instruction addressed to port FFF1H enables the on-board ROM. When first powered-up, ROM is enabled. Shadow ROM and RAM can occupy the same

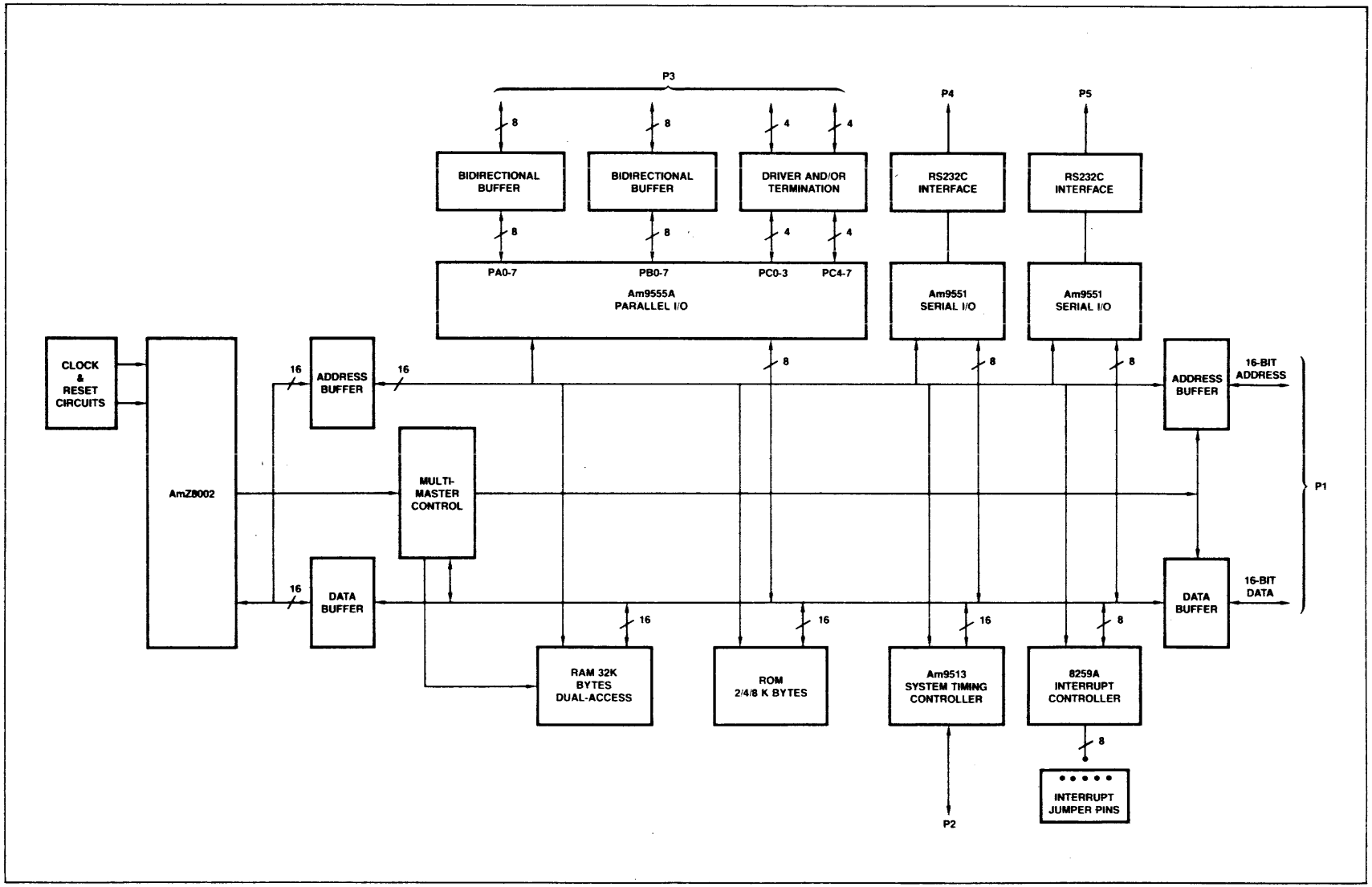


Figure 1-1. Am96/4116A MonoBoard Computer, Block Diagram

physical address space. It is possible to write to RAM, but RAM can only be accessed for read when the shadow ROM is disabled. This permits all or portions of ROM to be copied to RAM and then the ROM turned off.

There are 32K bytes of dynamic RAM included on the Am96/4116 board, configured as two-port (dual access) memory. Sixteen 16,384 by 1, N-channel dynamic R/W RAMs are used. With 200 nanosecond RAMs, no wait state is needed.

RAM can be simultaneously accessed from the Multibus interface and the AmZ8002 CPU. Access arbitration for two-port operation provides 50 percent interleave of AmZ8002 and Multibus access. Control defaults to the AmZ8002 if no Multibus requests are active.

An 8259A provides an eight channel vectored priority interrupt system. The eight channels can be programmed to perform priority resolution on either a fixed or rotating basis in either an interrupt or polled mode, allowing the user flexibility to establish interrupt service priorities based upon individual requirements.

The eight inputs to the 8259A are jumper selectable from an interrupt matrix. Selection can be from eight gated Multibus interrupts, four serial port (Am9551) interrupts, one parallel port (Am8255A) interrupt, and interrupts from the timer chip (Am9513).

Non-maskable interrupts are also produced and are, Multibus power fail, timeout for AmZ8002 access to Multibus, selected interrupt from interrupt matrix, and odd word trap.

The system contains one Am8255A Programmable Peripheral Interface containing three parallel I/O ports. Two 8-bit ports are buffered with bidirectional buffers. The buffer direction for each port is selected by jumper to provide either input, output or dynamic direction control using a bit from one of the two 4-bit ports. The remaining port on the Am8255A is configured as two 4-bit ports socketed for drivers or receivers (optional). Signals from each 4-bit port are used as interrupt signals at the interrupt matrix. The I/O lines are brought out at the 50 pin connector P3 at the top of the board.

Two Am9551 Programmable Communications Interfaces provide two serial I/O ports. One of these ports supports a full RS232C interface. The other supports a modified RS232C interface where, Data Set Ready, and Clear to Send signals are omitted. The Am9551 provides full duplex, buffered transmit and receive capabilities. A programmable baud rate generator provides baud rates between 50 and 9,600 baud for asynchronous data transmission, and up to 38,400 baud for synchronous operation. Each communications interface can be programmed to implement the desired synchronous or asynchronous serial data protocol. Data format, control character format, and parity are under program control. Parity, overrun, and framing error detection are all incorporated on the programmable communications interface. Command and control lines, serial data lines, and signal ground lines are brought out to P4 and P5 at the top the board.

The system includes an Am9513 System Timing Controller to enhance system capability with respect to counting and timing operations. It provides the capability for programmable frequency synthesis, complex waveform generation including programmable duty cycles, digital one-shots, time-of-day clocking including alarms, pulse generation, baud rate generation, frequency shift keying, stop watch timing, event count accumulation, and many more applications. The Am9513 can be dynamically reconfigured under program control. Source, gate, and output lines are brought out to connector P2 at the bottom of the board.

SPECIFICATIONS

Specifications for the Am96/4116 MonoBoard Computer are listed in table 1-1.

TABLE 1-1. SPECIFICATIONS

Word Size	Instruction:	1 word (16 bits) to 4 words (64 bits)
	Data:	byte (8 bits), word (16 bits), or long word (32 bits)
Memory Addressing	On-board ROM/EPROM:	0-7FFH (2708 chips) 0-0FFFH (2716 chips) 0-1FFFH (2732 chips)
	On-board RAM:	8000-FFFFH or 0000-7FFFH
	Off-board Memory:	0000-7FFFH or 8000-FFFFH Any 32K space not occupied by on-board RAM.
Memory Capacity	On-board ROM/EPROM:	2 sockets for up to 8K bytes 2708 E-PROM or 2758 ROM 2K bytes 2716 E-PROM or 9218 Mask ROM 4K bytes 2732 E-PROM or 9233 Mask ROM 8K bytes
	On-board RAM:	Dynamic, 32K bytes

TABLE 1-1. SPECIFICATIONS (continued)

Shadow ROM		A Write command to I/O port FFFOH disables addressing on-board ROM and causes ROM addresses o to 8K to be mapped to off-board RAM. A Write to I/O port FFF1 enables on-board ROM.
RAM Access	Type of Access:	2-port (Dual Access)
	Wait States:	No wait states for access from AmZ8002
	Access Time from Multibus, Command to XACK Time:	1350-3275 nanoseconds
	w/2 port RAM lock:	First Access: 1350-3275 ns Subsequent Access: 737-1087 ns
Multibus Interface	Clocks:	BCLK and CCLK jumperable
	Exchange Capability:	Serial priority on-board Parallel priority off-board
	Bus Lock:	Write to I/O port FFF9H locks the bus to exclude other access. Write to I/O port FFF8H unlocks the bus.
	Multibus Interrupts:	Non-bus vectored interrupts are supported and may be implemented with the following options: Interrupts are always recognized when jumpered. Bus vectored interrupts are not supported.
I/O Port Functions	Single Step Enable:	FFCOH
	Interrupt Controller (Am8259A):	Data: FFC8H Control: FFCAH
	Timer (Am9513):	Data: FFDOH Control: FFD2H
	Serial I/O Port #1 (Am9551):	Data: FFD8H Control: FFDAH
	Serial I/O Port #2 (Am9551):	Data: FFEOH Control: FFE2H

TABLE 1-1. SPECIFICATIONS (continued)

I/O Port Functions	Parallel I/O Port (Am8255A):	Chan A:	FFE8H	Chan C:	FFECH
		Chan B:	FFEAH	Control:	FFEEH
	ROM Enable:	Shadow On:	FFF1H		
	ROM Disable:	Shadow Off:	FFF0H		
	Multibus Lock:		FFF9H		
	Multibus Unlock:		FFF8H		
Serial I/O Capacity	Synchronous:	5 to 8 bit characters Internal or external synchronization Automatic sync insertion			
	Asynchronous:	5 to 8 bit characters Break character generation 1, 1 1/2, or 2 stop bits False start bit detector			
	Baud Rate:	Programmable			
	Parallel I/O Capacity:	Two 8 bit ports (A and B) Two 4 bit ports (C even and C odd) socketed for drivers or receivers			
Power Requirements		Typical (With E-PROM devices installed)			
	+ 5V DC	3.80A			
	+12V DC	0.10A			
	-12V DC	0.03A			
Environmental Characteristics		0° to 55°C up to 90% without condensation			
Physical Characteristics	Length:	304.80 mm (12.00 inches)			
	Heigth:	171.50 mm (6.57 inches)			
	Thickness:	12.70 mm (0.50 inches)			
	Weight:	0.45 Kg (1.00 pounds)			
	Shipping Weight:	1.36 Kg (3.00 pounds)			

CHAPTER 2
INSTALLATION AND INTERFACE

INTRODUCTION

This chapter provides information to install an Am96/4116A MonoBoard Computer (MBC) in a user's system. The information includes unpacking and inspection, and user design information such as interface data, power requirements, cooling requirements, bus interface characteristics, and connector pin assignments.

UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severly damaged or water stained, request the carrier's agent to be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection. Shipping damages should be immediately reported to the carrier.

NOTE

Do not attempt to service the board yourself as this will void the warranty.

It is suggested that salvageable shipping cartons and packing materials be saved for use in case the product must be shipped in the future.

POWER REQUIREMENTS

The Am96/4116A requires +5 Vdc and ±12 Vdc power inputs. The power supply must be capable of supplying at least 3.8A to accommodate the Am96/4116A requirements.

COOLING REQUIREMENTS

The Am96/4116 dissipates approximately 30 W (typical). Adequate air circulation must be provided to prevent a temperature rise above 55°C (131°F).

USER SELECTABLE OPTIONS

The Am96/4116A is designed as a general purpose 16 bit micro computer; optional jumpering facility is provided to tailor board operation to specific use. Jumpers must be in the correct positions prior to board operation. The following paragraphs provide instructions for optional jumper configurations.

MEMORY EXPANSION

The Am96/4116A has the capability of bank selecting up to sixteen 32k byte blocks of off-board memory, for a maximum of 152k bytes of external RAM and/or ROM. Parallel I/O port C bits 0 to 3, are used to select the off-board memory. However, off-board memory must not occupy the same logical address space as the on-board RAM. If on-board RAM is in the upper 32k (8000 to FFFF hex), then off-board memory must occupy the space from 0000 to 7FFF hex. Table 2-1 lists the jumpers available.

TABLE 2-1. MEMORY EXPANSION JUMPERS

SIGNAL	JUMPER PIN (s)
PC0*	10
PC1*	12
PC2*	14
PC4*	16
ADRF*	62-63
AD10*	65, 36-37
AD11*	68, 38-39
AD12*	58, 40-41
AD13*	59, 42-43
N/S*	66
I-FETCH*	69

For example, to connect PC0* to the Multibus AD10* pin, connect a jumper from pin 10 to 65, and a jumper from 36 to 37. To connect PC1* to AD11*, connect a jumper from 12 to 68 and another from 38 to 39.

Two additional lines, defined by the CPU, are available at jumper pins to expand the memory to a maximum of 160K bytes. The signals are I-FETCH* (code) and N/S* (Normal/System). The I-FETCH* signal provides the capability of having two separate areas of memory one for code and one for data. The N/S* signal provides for two additional areas of memory, one for system use and one for normal (user) functions. The functions of I-FETCH* and N/S* can be combined as shown in figure 2-1. The blocks shown in figure 2-1 can occupy the same logical area of memory, though the physical locations will be different.

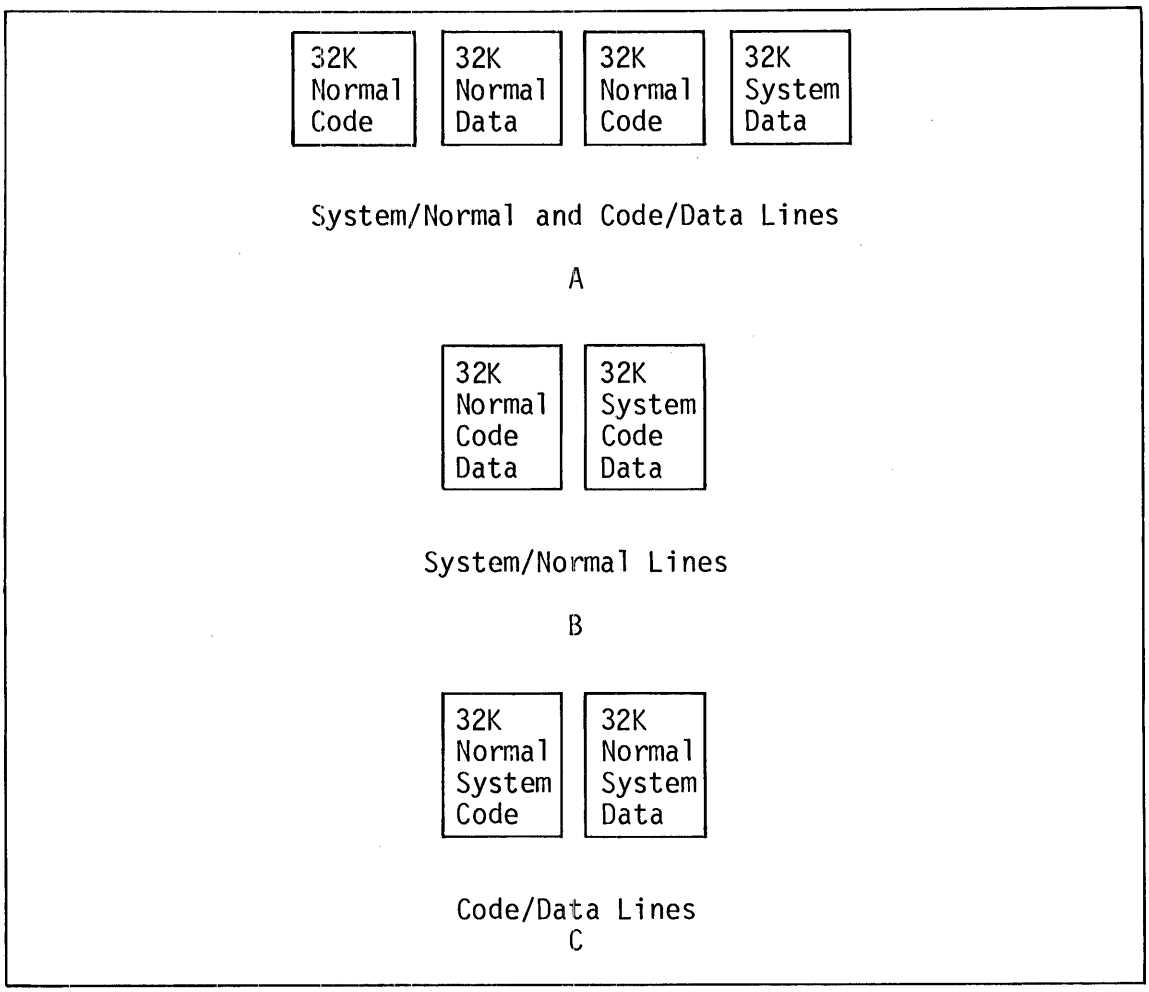


Figure 2-1. Off-Board Memory Expansion Using Normal/System and Code/Data Signals

STARTING ADDRESS OF ON-BOARD RAM

On-board RAM can be located in either the upper or lower 32K of the Am96/4116 memory space. For the upper 32K byte space, connect a jumper between pin 192 and 193. To locate RAM in the lower 32K byte area reconnect the jumper between pin 192 and 193. To locate RAM in the lower 32K byte area reconnect the jumper between pins 193 and 194.

WAIT STATE FOR SLOW ROMS

One wait state is required for ROMs with cycle time slower than 400 nanoseconds. Installation of jumper 186 to 187 introduces the wait state.

SERIAL I/O PERIPHERAL INTERFACE CLOCK SELECT

The Receive Clock (RxC) and Transmit Clock (TxC) for the two Am9551 serial I/O devices are jumper selectable. The clock inputs for serial port 1 can be jumpered together to the on-board clock source, or separately connected to external RxC and TxC. The clock source for serial port 2 is on-board only. Table 2-2 lists the jumper locations.

TABLE 2-2. SERIAL I/O JUMPERS

SIGNAL	FUNCTION	JUMPER	I/O CONNECTIONS
RxC-1	Ext. Rcv Clk #1	147-161	P4-22
TxC-1	Ext. Xmit Clk #1	146-160	P4-14
RTS-1	Request to Send #1	132-134 (Active) 130A-134 (Ground)	P4-9 None
CTS-1	Clear to Send #1	133-135 (Active) 131-133 (Ground)	P4-7 None
CTS-2	Clear to Send #2	180-181 (Active) 181-179 (Ground)	P5-7 None
CLK-1	Baud Rate Clk #1	141-143 (9600 Baud) 142-143 (Prog.)	None None
CLK-2	Baud Rate Clk #2	39-140 (9600 Baud) 138-139 (Prog.)	None None
P4 is Serial Port #1. P5 is Serial Port #2, (Modified RS232C)			

BAUD RATE SELECT

The Am96/4116A baud rate is programmable using two of the counters in the Am9513 System Timing Controller. As shipped from the factory, the baud rate is set at 9600. Table 2-2 lists the clock source jumpers. Table 3-5 lists the values for programming other baud rates, using asynchronous communications mode.

CUSTOMIZING DATA SET OPERATION

The Clear to Send and Request to Send signals, between a data set or data terminal can be jumpered to external signals or can be jumpered to ground (to be continuously active). Table 2-2 lists these jumpers. Table 2-3 lists pin assignments for the serial I/O connectors, P4 (port 1) and P5 (port 2), serial port 2 is the modified RS232C port.

TABLE 2-3. CONNECTOR P4 AND P5 TO TERMINAL CONNECTOR PIN ASSIGNMENTS

PIN	SIGNAL	DB-25 PIN NO.	PIN	SIGNAL	DB-25 PIN NO.
1	CHASSIS GND	1	14	DATA TERM READY/ TX CLK	20
2	Not Used	14	15	DATA CARRIER RET	8
3	TRANSMITTED DATA	2	16	Not Used	21
4	Not Used	15	17	Not Used	9
5	RECEIVED DATA	3	18	Not Used	22
6	Not Used	16	19	Not Used	10
7	REQUEST TO SEND	4	20	Not Used	23
8	Not Used	17	21	Not Used	11
9	CLEAR TO SEND	5	22	RX RET/RX CLK	24
10	Not Used	18	23	Not Used	12
11	DATA SET READY	6	24	Not Used	25
12	Not Used	19	25	Not Used	13
13	SIGNAL GND	7	26	SIGNAL GND	--

AUXILIARY CONNECTOR P2

Connector P2 is a 60 pin double-sided edge connector that provides interface to the Am9513 System Timing Controller. Table 2-4 lists the signals and pin numbers for P2.

TABLE 2-4. P2 CONNECTIONS

PIN	SIGNAL	PIN	SIGNAL
27	FOUT	43	GATE3
29	OUT1	45	GATE4
31	OUT2	47	GATE5
33	OUT3	49	SOURCE1
35	OUT4	51	SOURCE2
37	OUT5	53	SOURCE3
39	GATE1	55	SOURCE4
41	GATE2	57	SOURCE5
		23	POWER FAIL*

INTERRUPT JUMPERS

A priority interrupt jumper matrix provides for eight out of 24 possible interrupts sources to be jumpered to eight interrupt controller inputs. Table 2-5 lists the possible jumper configurations. In addition, four sources of non-maskable interrupts are shown below in table 2-6.

TABLE 2-5. PRIORITY INTERRUPT JUMPERS

SIGNAL	PIN NO.	COLUMN 1 JUMPER PINS	COLUMN 2 JUMPER PINS	INT INPUT
TxRDY1*	On-Board	98		
RxRDY1*	On-Board	101		
TxRDY2*	On-Board	99		
RxRDY2*	On-Board	100		
PPC0*	On-Board	102		
PPC3*	On-Board	103		
OUT1	On-Board	118		
OUT2	On-Board	114		
OUT3	On-Board	120		
OUT4	On-Board	116		
OUT5	On-Board	112		
TIMEOUT*	On-Board	122	78,113	IRQ7*
POWERFAIL*	On-Board	126	81,115	IRQ6*
ODD WORD TRAP*	On-Board	124	84,117	IRQ5*
SS TRAP*	On-Board	130	87,119	IRQ4*
Z8002 NVI*	On-Board	75,129	90,121	IRQ3*
INT0* Buf.	On-Board	73	93,123	IRQ2*
INT1* Buf.	On-Board	79	96,125	IRQ1*
INT2* Buf.	On-Board	85	97,127	IRQ0*
INT3* Buf.	On-Board	91		
INT4* Buf.	On-Board	94		
INT5* Buf.	On-Board	88		
INT6* Buf.	On-Board	82		
INT7* Buf.	On-Board	76		
Jumper any column 1 pin to any column 2 pin.				

TABLE 2-6. NON-MASKABLE INTERRUPTS

SIGNAL	JUMPER PINS
Time Out*	157-171
Power Fail*	159-173
Odd Word Trap*	158-172
User Selected	xxx-128
Note: The user selected interrupt can be one of the ones listed in table 2-5.	

PARALLEL I/O INTERFACE

The parallel I/O section is configured for Am8304 bidirectional bus transceivers at Port A (FFE8) and Port B (FFEA). As shipped from the factory, jumpers are installed between jumper pins 105 and 110 for Port A and between 104 and 109 for Port B. Table 2-7 lists the jumpers for Port A and B functions. Port C is two 4 bit ports. Sockets are provided for each port for TTL line drivers as listed in table 2-8. The Port C interface lines may be terminated by either a 220Ω/330Ω divider or a 1KΩ pull-up as shown in figure 2-2.

The 220Ω/330Ω Pull-Up/Pull-Down Pack is stocked by distributor under Intel part number SBC-901 and National Semiconductor part number BLC-901. The 1KΩ Pull-Up Pack is stocked under Intel part number SBC-902 and National Semiconductor part number BLC-902.

Table 2-9 lists the pin connections for parallel I/O connector P3.

TABLE 2-7. PARALLEL I/O PORT A AND B JUMPERS

PORT	INPUT	OUTPUT	BI-DIRECTIONAL
A	105-108	105-110	105-111
B	104-109	104-107	104-106

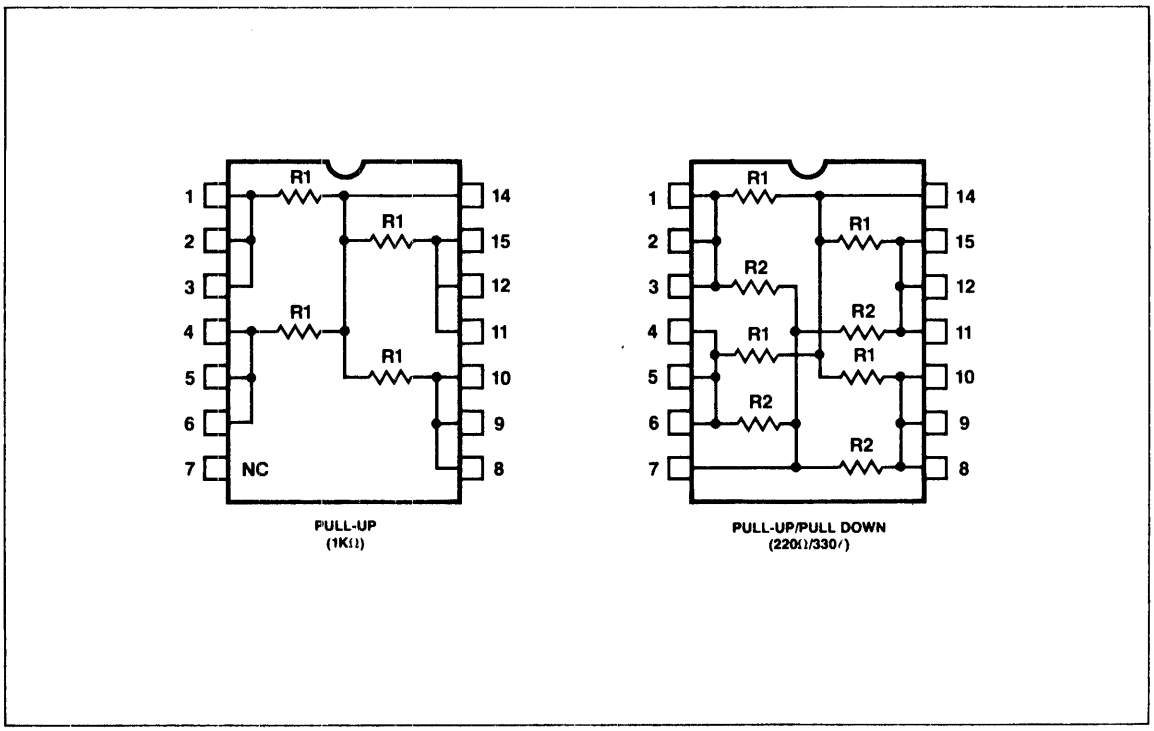


Figure 2-2. Parallel I/O Line Terminator

TABLE 2-8. PARALLEL I/O SOCKET COMPATIBLE LINE DRIVERS

DRIVER	CHARACTERISTIC	SINK CURRENT	DRIVER	CHARACTERISTIC	SINK CURRENT
7438	I, OC	48mA	7409	NI, OC	16mA
7437	I	48mA	7408	NI	16mA
7432	NI	16mA	7403	I, OC	16mA
7426	I, OC	16mA	7400	I	16mA

NOTE: I = Inverting
NI = non-inverting
OC = open collector

TABLE 2-9. PARALLEL I/O CONNECTOR P3

PIN		SIGNAL	PIN	SIGNAL
1		PB7	2	Ground
3		PB6	4	Ground
5		PB5	6	Ground
7	Port B	PB4	8	Ground
9		PB3	10	Ground
11		PB2	12	Ground
13		PB1	14	Ground
15		PB0	16	Ground
17		PC3	18	Ground
19		PC2	20	Ground
21		PC1	22	Ground
23	Port C	PC0	24	Ground
25		PC4	26	Ground
27		PC5	28	Ground
29		PC6	30	Ground
31		PC7	32	Ground
33		PA7	34	Ground
35		PA6	36	Ground
37		PA5	38	Ground
39		PA4	40	Ground
41	Port A	PA3	42	Ground
43		PA2	44	Ground
45		PA1	46	Ground
47		PA0	48	Ground
49		None	50	Ground

ENABLE REAL-TIME CLOCK

When the jumper from 188 to 189 is installed, the real-time clock in the Am9513 System Timing Controller is enabled.

ON-BOARD ROM TYPE SELECTION

Two ROM sockets are provided on the Am96/4116A board. The user can select 2708, 2716, 2732 E-PROMS or 2758 ROM. The jumpers are listed in table 2-10.

TABLE 2-10. ROM TYPE JUMPER SELECTION

FUNCTION	MEMORY DEVICES			
	Am9708	Am9716	Am9732	2758
+12 V to pin 19	24- 25	-------	-------	-------
GND to pin 19	-------	-------	-------	25- 26
AA (bit 10)	-------	25- 27	25- 27	-------
AB (bit 11)	-------	-------	29- 30	-------
-5 V to pin 21	30- 31	-------	-------	-------
+5 V to pin 21	-------	28- 30	-------	28- 30
ROM select	177-178 175-176	177-178	174-176	174-176
Note: For 2708 types connect 70 to 71. All others 71 to 72.				

SYSTEM BUS PRIORITY

If the Am96/4116A is not the highest priority master, jumper pins 22 to 23. Jumper pins 21 to 22 for highest priority. Jumper pins 184 and 185 to drive BPRO* (Bus Priority OUT). Jumpers installed at the factory are: 22-23 and 184-185 (sets up the daisy chain priority scheme).

INITIALIZE/POWER UP RESET

The power-up-reset function can be jumpered to the bus INIT line. This jumper is located between pins 190 and 191.

BUS CLOCK (BCLK) AND CONSTANT CLOCK (CCLK) JUMPERS

The Am96/4116A can be used as the source of the 9.83 MHz BCLK and/or CCLK Multibus clock signals. The jumpers are 19 to 20 and 17 to 18.

DUAL PORT RAM ACCESS

The on-board RAM can be accessed either by the CPU or an off-board source through the Multibus. Jumpering pins 167 and 168 permits normal dual-port access. Jumpering pins 166 and 167, permits shorter RAM access times through the Multibus. The first bus access is 1350 to 3275 subsequent accesses, providing the BUSY* line is kept active, are 737 to 1087 ns.

NOTE

CPU operation is suspended while BUSY* is true.

INTERFACE REQUIREMENTS

The Am96/4116A MonoBoard Computer connects into a system bus through P1, to an auxiliary bus through P2, to a parallel peripheral interface through P3, and to two serial peripheral interfaces through P4 and P5. Table 2-11 lists the mating connectors.

TABLE 2-11. Am96/4116A CONNECTORS

CONNECTOR NUMBER	NUMBER OF PINS	CONNECTOR CHARACTERISTICS	EQUIVALENT TYPE
P1	86	0.156 inch spacing	CDC VPB01E43A-00A1
P2	60	0.100 inch spacing	
P3	50	0.100 inch spacing	3M #3415-0001
P4	26	0.100 inch spacing	3M #3462-0001
P5	26	0.100 inch spacing	3M #3462-0001

BUS INTERFACE

Connector P1 provides the bus interface for the Am96/4116A. Connector P1 is a double-sided edge connector. Table 2-12 lists pin designations.

DC BUS CHARACTERISTICS

Table 2-13 lists the DC characteristics of the Multibus. For more information on the Multibus, refer to the Intel Application Note, AP-28A, Multibus Interfacing.

TABLE 2-12. SYSTEM BUS CONNECTOR P1 PIN ASSIGNMENTS

	(Component Side)			(Circuit Side)		
	Pin	Mnemonic	Description	Pin	Mnemonic	Description
	1	GND	Signal GND	2	GND	Signal GND
	3	+5	+5 VDC	4	+5	+5 VDC
Power	5	+5	+5 VDC	6	+5	+5 VDC
Supplies	7	+12	+12 VDC	8	+12	+12 VDC
	9	-5	Not Used	10	-5	Not Used
	11	GND	Signal GND	12	GND	Signal GND
	13	BCLK*	Bus Clock	14	INIT*	Initialize
	15	BPRN*	Bus Priority In	16	BPRO*	Bus Priority Out
	17	BUSY*	Bus Busy	18	BREQ*	Bus Request
	19	MRDC*	Mem Read Command	20	MWTC*	Mem Write Command
Bus	21	IORC*	I/O Read Command	22	IOWC*	I/O Write Command
Controls	23	XACK*	XFER Acknowledge	24	INH1*	Inhibit 1 (RAM)
	25	AACK*	Advanced Acknowledge	26	INH2*	Not Used (ROM)
	27	BHEN*	Byte High Enable	28	ADR10*	See table 2-1
	29	CBRQ*	Common Bus Request	30	ADR11*	see table 2-1
	31	CCLK*	Constant Clock	32	ADR12*	see table 2-1
	33	INTA*	Interrupt Acknowledge	34	ADR13*	see table 2-1
	35	INT6*		36	INT7*	
Interrupts	37	INT4*	Interrupt Requests	38	INT5*	Interrupt Requests
	39	INT2*		40	INT3*	
	41	INT0*		42	INT1*	
	43	ADRE*		44	ADRF*	
	45	ADRC*		46	ADRD*	
	47	ADRA*		48	ADRB*	
Addresses	49	ADR8*	Address Bus	50	ADR9*	Address Bus
	51	ADR6*		52	ADR7*	
	53	ADR4*		54	ADR5*	
	55	ADR2*		56	ADR3*	
	57	ADR0*		58	ADR1*	
	59	DATE*		60	DATF*	
	61	DATC*		62	DATD*	
	63	DATA*		64	DATB*	
Data	65	DAT8*		66	DAT9*	
	67	DAT6*		68	DAT7*	
	69	DAT4*		70	DAT5*	Data Bus
	71	DAT2*	Data Bus	72	DAT3*	
	73	DAT0*		74	DAT1*	
	75	GND	Signal GND	76	GND	Signal GND
	77	---	Reserved	78	---	Reserved
Power	79	-12	-12 VDC	80	-12	-12 VDC
Supplies	81	+5	+5 VDC	82	+5	+5 VDC
	83	+5	+5 VDC	84	+5	+5 VDC
	85	GND	Signal GND	86	GND	Signal GND

TABLE 2-13. Am96/4116A BUS DC CHARACTERISTICS

SIGNALS	SYMBOL	PARAMETER DESCRIPTION	CONDITION	MIN	MAX	UNITS
ADRO*-ADRF* ADDRESS	V_{OL}	Output Low Voltage	I_{OL} = 48.0mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} =-10.0mA	2.4		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4mA		-200	µA
	I_{IH}	Input Current at High V	V_{IN} = 2.7mA		80	µA
	C_L	Capacitive Load			18	pF
MRDCI*, MWTC*, IORC*, IOWC*	V_{OL}	Output Low Voltage	I_{OL} = 32.0mA		0.4	V
	V_{OH}	Output High Voltage	I_{OH} = -5.2mA	2.4		V
	I_{LH}	Output Leakage High	V_O = 2.4 V		40	µA
	I_{LL}	Output Leakage Low	V_O = 0.4 V		-40	µA
	C_L	Capacitive Load			15	pF
DATA0-DATA7	V_{OL}	Output Low Voltage	I_{OL} = 48.0mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} =-10.0mA	2.4		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4 V		-200	µA
	I_{IH}	Input Current at High V	I_{OL} = 48.0 V		80	µA
	C_L	Capacitive Load			18	pF
INTI*	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4 V		-2.2	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.5 V		1	mA
	C_L	Capacitive Load			18	pF
BPRN*, XACK*, AACK*	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.5		-2.6	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.7 V		0.3	mA
	C_L	Capacitive Load			18	pF
BUSY* OPEN COLLECTOR	V_{OL}	Output Low Voltage	I_{OL} = 25.0mA		0.4	V
	C_L	Capacitive Load		2.0	20	pF
INIT* (SYSTEM RESET)	V_{OL}	Output Low Voltage	I_{OL} = 32.0mA		0.6	V
	V_{OH}	Output High Voltage	OPEN COLLECTOR			
	V_{IL}	Input Low Voltage			0.7	V
	V_{IH}	Input High Voltage	V_{IN} = 5.5			V
	I_{IL}	Input Current at Low V	V_{IN} = 0.3	2.7	0.1	mA
	I_{IH}	Input Current at High V			-0.7	mA
	C_L	Capacitive Load			38	pF
BCLK*	V_{OL}	Output Low Voltage	I_{OL} = 48.0mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} = -1.0mA	2.7		V
	C_L	Capacitive Load			18	pF
EXT INTR*	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4 V	6.8		mA
	I_{IH}	Input Current at High V	V_{IN} = 5.5 V		2.0	mA
	C_L	Capacitive Load			18.0	pF

CHAPTER 3
OPERATION AND PROGRAMMING

INTRODUCTION

This section provides operating and programming information for the Am96/4116A MonoBoard Computer (MBC) and the programmable devices. The MCB includes five programmable devices as follows:

- Two Am9551 Programmable Communications Interfaces that provide two RS232C serial I/O ports.
- An Am8255A Programmable Peripheral Interface that controls the 24 parallel I/O lines.
- An 8259A Programmable Interrupt Controller that responds to eight interrupt lines.
- An Am9513 System Timing Controller

I/O ADDRESS ASSIGNMENT

The CPU communicates with the programmable devices through a sequence of I/O read and I/O write commands. A summary of I/O addresses is listed in table 3-1.

NOTE

I/O addresses from C000H to FFFFH are reserved for the Am96/4116 board.

SHARED MEMORY AND THE MULTIBUS

Sometimes it is useful for two processors to share the same memory locations in order to communicate and pass data. With the Am96/4116A, only byte (8-bit) operations should be used when passing data between processors and shared memory. The Multibus considers data bits 0 to 7 as even bytes and data bits 8 to 15 as odd bytes. However, the AmZ8002 considers data bits 0 to 7 as odd bytes and data bits 8 to 15 as even bytes. Figure 3-1 illustrates the Am96/4116A and external RAM attached to the Multibus. The same example applies to the on-board RAM if shared by an external device. In figure 3-1, memory locations are given as 8000H and 8001H. Note that 8000H in RAM uses bits 0 to 7 while the AmZ8002 uses bits 8 to 15.

TABLE 3-1. I/O PORT ADDRESS

I/O ADDRESS BITS	I/O PORT ADDRESS	I/O DEVICE	INPUT (READ) FUNCTION	OUTPUT (WRITE) FUNCTION
F E D C B A 9 8 7 6 5 4 3 2 1 0				
1 1 - - - - - - - - 0 0 0 0 0 0	FFC0	Single Step		Write FFC0
1 1 - - - - - - - - 0 0 1 0 0 0	FFC8	8259A Interrupt	Read ISR, IRR, or Polled Status	Write ICW1 and OCW2,3
1 1 - - - - - - - - 0 0 1 0 1 0	FFCA	Controller	Read IMR	Write ICW2, 4, and OCW1
1 1 - - - - - - - - 0 1 0 0 0 0	FFD0	Am9513 System	Read Data Register	Write Data Register
1 1 - - - - - - - - 0 1 0 0 1 0	FFD2	Timing Controller	Read Status Register	Write Command Register
1 1 - - - - - - - - 0 1 1 0 0 0	FFD8	Am9551 Serial	Receive Data Buffer	Transmit Data Buffer
1 1 - - - - - - - - 0 1 1 0 1 0	FFDA	I/O Port #1 (P4)	Status Register	Command Register
1 1 - - - - - - - - 1 0 0 0 0 0	FFE0	Am9551 Serial	Receive Data Buffer	Transmit Data Buffer
1 1 - - - - - - - - 1 0 0 0 1 0	FFE2	I/O Port #2 (P5)	Status Register	Command Register
1 1 - - - - - - - - 1 0 1 0 0 0	FFE8	Am8255A	Read Port A	Write Port A
1 1 - - - - - - - - 1 0 1 0 1 0	FFEA	Parallel I/O Port	Read Port B	Write Port B
1 1 - - - - - - - - 1 0 0 1 0 0	FFEC		Read Port C	Write Port C
1 1 - - - - - - - - 1 0 0 1 1 0	FFEE		Status Register	Command Register
1 1 - - - - - - - - 1 1 1 0 0 0	FFF0	Shadow ROM ON		Write FFF0
1 1 - - - - - - - - 1 1 1 0 0 1	FFF1	Shadow ROM OFF		Write FFF1

BLOCK-SELECT MEMORY EXPANSION

Normally, CPU address bits 0 to F (ADR0* to ADRF*) are used to address up to 64K bytes of memory. Parallel I/O port C, bits 0 to 3, can be used as additional address lines to expand memory addressing. Address line ADF* is jumperable to either the CPU address output or one of the port C bits. Figure 3-2 illustrates one method of external memory addressing. Note that the Multibus address line ADF* is connected to port C bit 0. Since the Am96/4116 has only 32K bytes on-board, the ADF* line can be used to bank switch external memory. The scheme shown in figure 3-2 permits up to eight external 64K byte RAM boards to be used for a total of 512K bytes. Actually, external memory can be either RAM or ROM, and is addressable in 32K-byte blocks. Blocks are selected by programming bits 0 to 3 of port C.

ROM ADDRESSING

The Am96/4116 includes sockets for up to 8K bytes of ROM or EPROM. The maximum storage for 2708 type devices is 2K bytes, for 2716 type devices, 4K bytes, and for 2732 type devices 8K bytes. A Shadow ROM design permits ROM to be interchanged with RAM under program control.

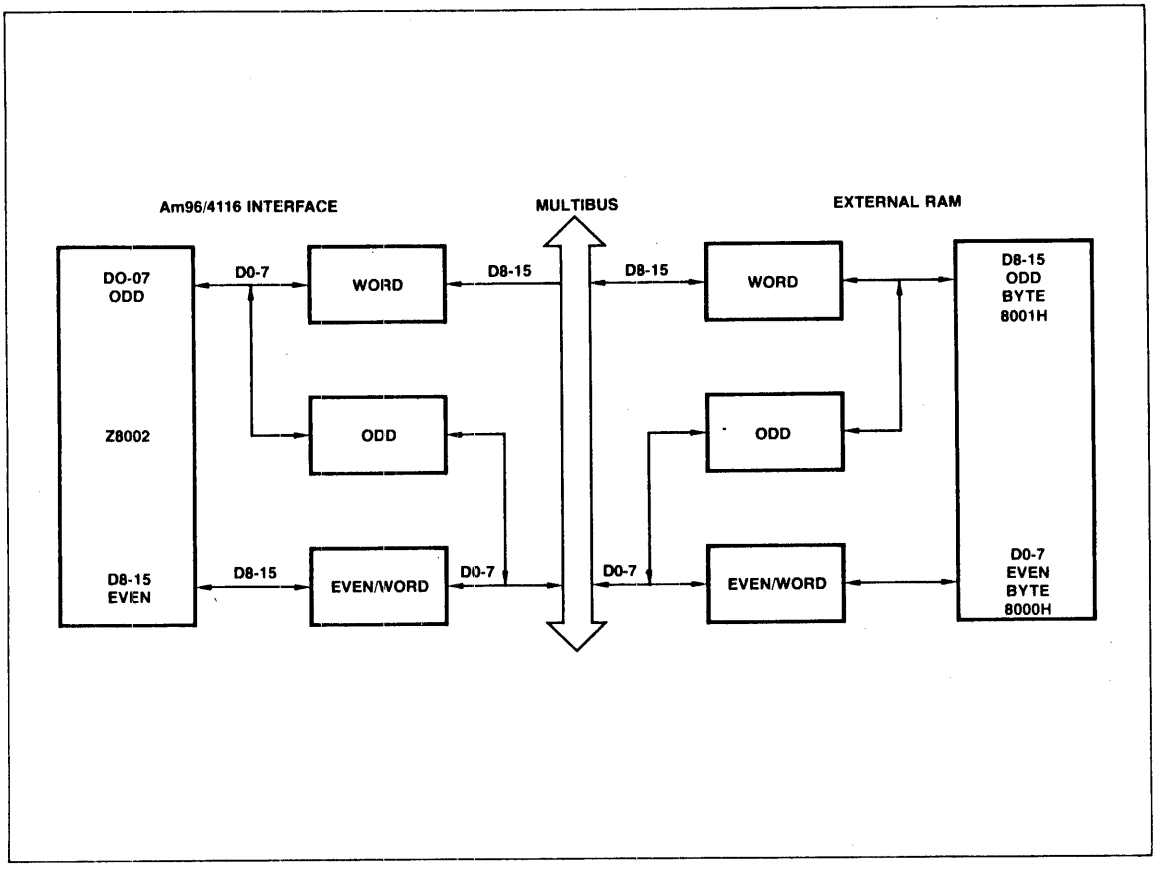


Figure 3-1. Am96/4116A to Multibus Interface

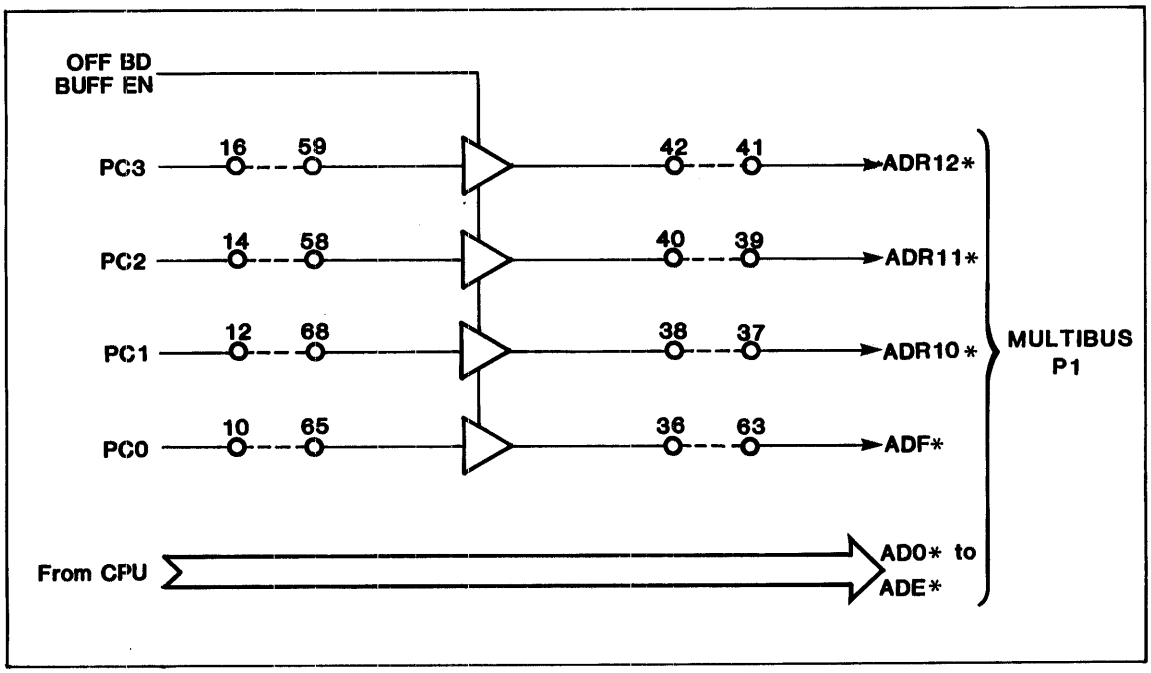


Figure 3-2. Memory Expansion

The shadow technique essentially adds the PROM/ROM space to the direct address size of the CPU, effectively increasing the usable address space by up to 8K bytes. An I/O write to address FFF0H will disable the shadow ROM. An I/O write to address FFF1H enables the shadow ROM. When enabled, ROM space goes from 0000 to 1FFFH, if 8K of ROM is being used. Jumpers configure PROM/ROM space for 1FFFH maximum. If the shadow ROM occupies the same physical memory space as RAM, the RAM can be written to, but not read until shadow ROM is disabled. This feature permits copying all or part of ROM into RAM, and then using only RAM.

SERIAL I/O INTERFACE PROGRAMMING

Two Am9551 Programmable Communications Interface chips are used to interface between the CPU data bus and two RS232C I/O ports. One Am9551 provides a full RS232C serial interface to P4. The other Am9551 provides a modified RS232C serial interface at P5. The modified serial I/O port does not use the Data Set Ready and Clear To Send lines. Programmable operating modes and format options allow the Am9551 to service a wide range of communications, disciplines, and applications. Operating modes are determined by a mode instruction word and a command instruction word.

Am9551 INITIALIZATION

The Am9551 chip is initialized as follows:

- Reset the chip by writing a command word (with bit 6 set) to hex address FFDAH or FFE2H.
- Write a MODE instruction word to command register.

NOTE

If the Am9551 is looking for a MODE when the reset command word is written, multiple reset commands must be issued.

- If synchronous mode is selected, write one or two sync characters as required.
- Write a command instruction word to command register.

NOTE

After initialization, always check the status of the TxRDY bit prior to writing data or a new command word to the Am9551. The TxRDY bit must be true to prevent overwriting and subsequent loss of commands or data. The TxRDY is inactive until initialization has been completed.

Once initialized, it is not necessary for a command instruction to precede all data transactions, only those transmissions that require a change in the command instruction.

Am9551 MODE INSTRUCTION WORD FORMAT

The mode instruction word defines the general characteristic of the Am9551. Once the mode instruction has been written, sync characters or command instructions can be inserted. The mode instruction word defines the following:

- For synchronous mode:

  Character length
  Parity enable/disable
  Even/odd parity
  Character synchronization
  Single or double character
  Sync

- For asynchronous mode:

  Baud rate multiplier
  Character length
  Parity enable/disable
  Even/odd parity
  Number of stop bits

The mode instruction word formats for synchronous and asynchronous modes are shown in figures 3-3 and 3-4 respectively.

Am9551 SYNC CHARACTERS

In the synchronous mode, one or two sync characters must be written to the command register. The format of the sync characters is at the option of the programmer.

COMMAND INSTRUCTION WORD FORMAT

The command instruction word must follow the mode and/or sync words. Once the command word is written, data can be transmitted or received by the Am9551. The format of the command word is shown in figure 3-5.

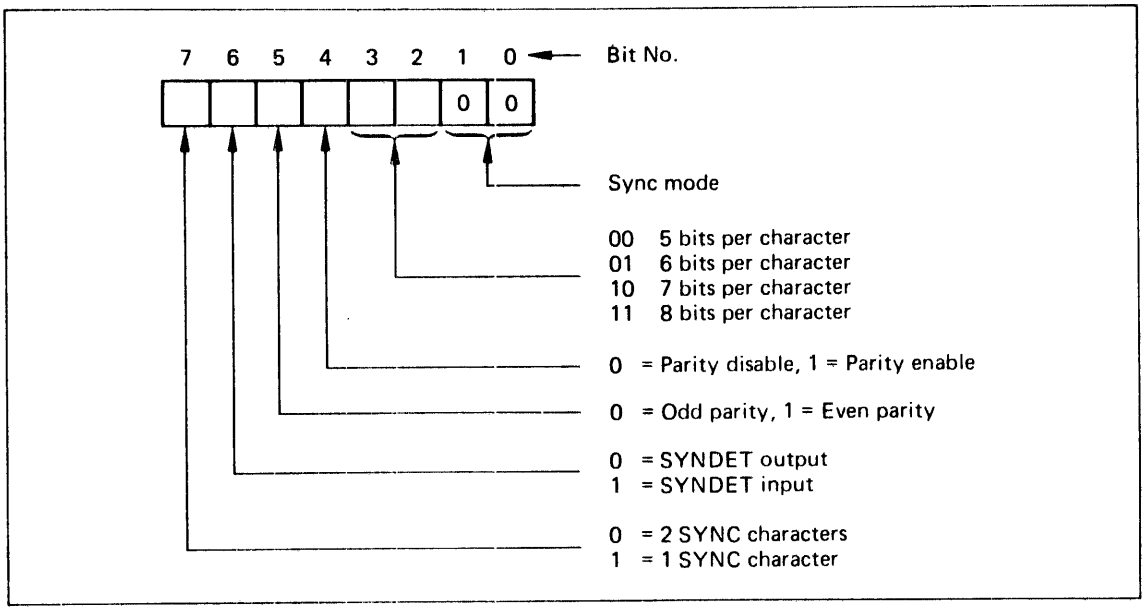


Figure 3-3. Am9551 Synchronous Mode Control Code

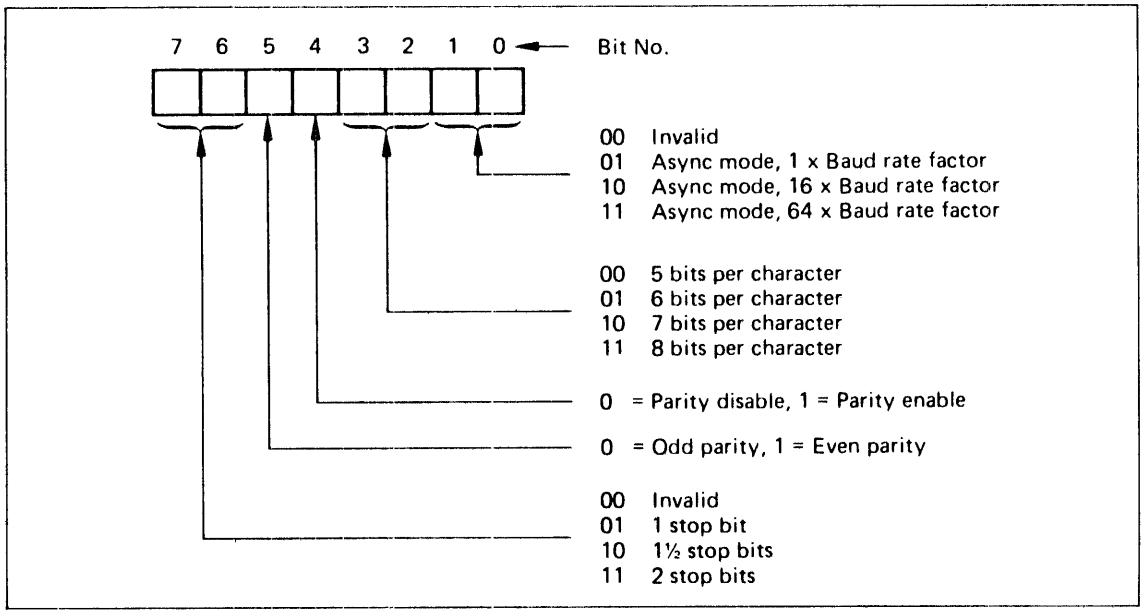


Figure 3-4. Am9551 Asynchronous Mode Control Code

Am9551 STATUS READ

The CPU can determine the status of the Am9551 any time by issuing an I/O input to addresses FFDAH and FFE2H. The format of the status byte is shown in figure 3-6.

The definition of the status bits is as follows:

TxRDY Transmitter Ready indicates the Am9551 is ready to accept a data character or command.

RxRDY — Receiver Ready indicates the Am9551 has received a character on its serial input and is ready to transfer it to the CPU.

TxE — Transmitter Empty signals the processor that the transmit register is empty.

PE — Parity Error indicates the character stored in the received character buffer was received with an incorrect number of binary 1 bits.

OE — Overrun flag is set when a byte stored in the receiver character register is overwritten with a new byte before being transferred to the processor.

FE — Framing Error indicates the asynchronous mode byte stored in the receiver character buffer was received with incorrect character bit format.

SYNDET — When Sync Detect is set for internal sync detect, this bit indicates character sync has been acheived and the Am9551 is ready for data.

DSR — Data Set Ready is set by the external Data Set Ready Signal to indicate the communications data set is ready.

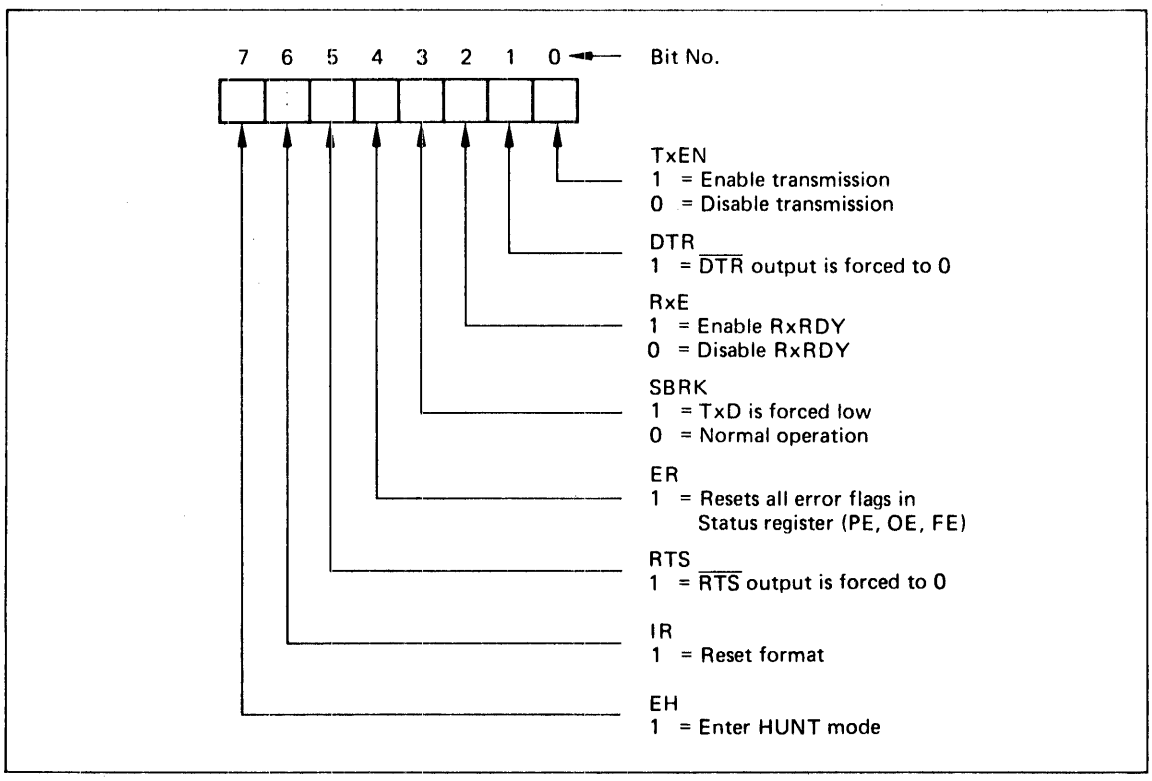


Figure 3-5. Am9551 Command Instruction Word Format

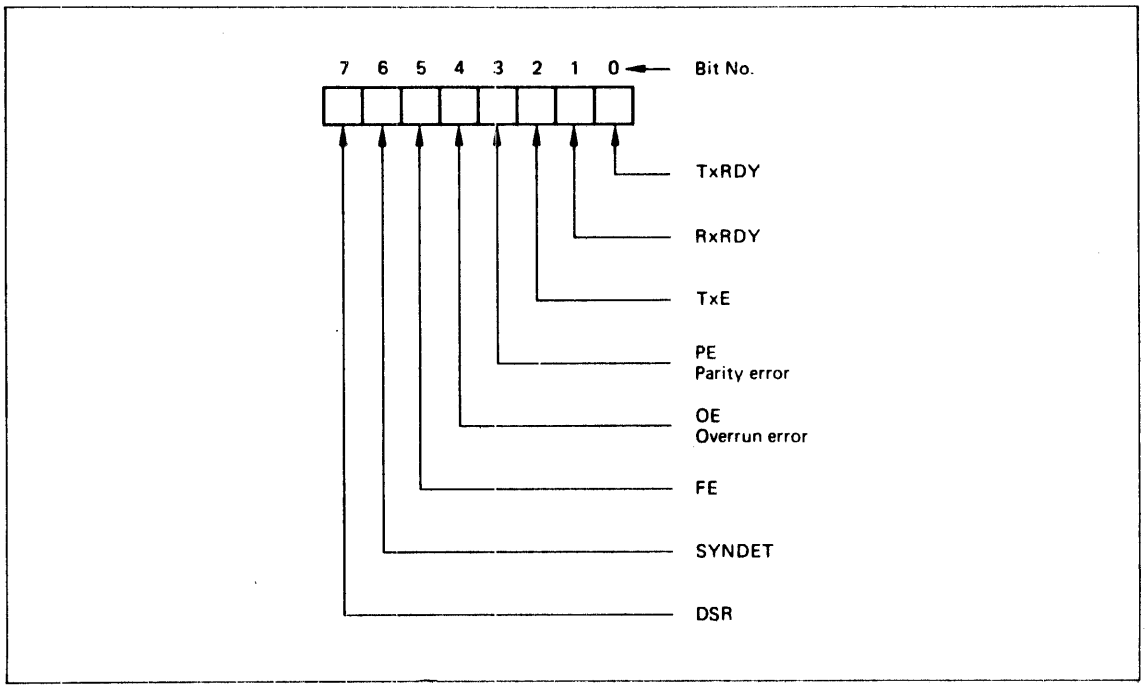


Figure 3-6. Am9551 Status Word Format

PARALLEL I/O INTERFACE PROGRAMMING

An Am8255A Programmable Peripheral Interface chips provide 24 parallel signal lines for the transfer and control of data to and from peripheral devices.

The chip provides three 8 bit ports (A, B, and C). Each port can be configured as either input or output, and port C on each chip is used as control lines for ports A and B in some modes. The operating modes of the ports are controlled by outputting either an operation control word or a bit set/reset control word. Table 3-2 is a configuration guide for the Am8255A.

Am8255A ADDRESSING

There are four consecutive word addresses (FFE8H through FFEEH) for control, data transfer, and status read. See table 3-1 for the port addresses and their functions.

Am8255A INITIALIZATION

The Am8255A is initialized by writing an operation control word to address to define the mode and by writing a bit set/reset control word for Port C control if required.

TABLE 3-2. PARALLEL I/O PORT CONFIGURATION SUMMARY

PORT AND MODE	CONTROL WORD	CONNECTOR POLARITY	DRIVER/TERMINATOR NETWORK	JUMPER ACTION			PORT RESTRICTIONS
				DELETE	ADD	EFFECT	
A Mode 0 Input FFE8	1001XXXX	Positive True	8304 at U3	None	105-108 As shipped	Enable input at U3	Port B: None Port C: None unless port B is in mode 1. B=FFEA and C=FFEC
A Mode 0 Output (Latched)	1000XXXX	Positive True	8304 at U3	105-108	105-110	Enable input at U3	Port B: None Port C: None unless port B is in mode 1.
A Mode 1 Inputs (Strobed)	1011XXXX	Positive True	8304 at U3	None	105-108 As shipped	Enable input at U3	Port B: None Port C: Perform the following dedicated functions: Bit 0, 1, 2: None unless port B is in mode 1. Bit 3: INTR (interrupt Request) output for port A. Bit 4: STB* (Strobe) input for port A. Bit 5: IBF (Input Buffer Full) output for port. Bit 6 and 7: Can be used for input or output. Both have same direction.
A Mode 1 Output (Latched)	1010XXXX	Positive True	8304 at U3	105-108	105-110	Enable output at 8304	Port B: None Port C: Performs the following dedicated functions: Bit 0, 1, 2: None unless port B is in mode 1. Bit 3: INTR (Interrupt Request) output for port Bits 4 and 5: Can be used for input or output; both have same direction. Bit 6: ACK* (Acknowledge) input for port A. Bit 7: OBF* (Output Buffer Full) Output for port A.
A Mode 2 Bidirectional	11XXXXXX	Positive True	8304 at U3	105-108	105-111	Allows PPC6 Output of Port C to Control Direc-tion of Data Flow	Port B: None Port C: Performs the following dedicated functions: Bit 0: Cannot be used. Bit 1 and 2: Can be used as input or output if port B is in mode 0. Bit 3: INTR (Interrupt Request) output for port. Bit 4: STR* (Strobe) input for port A. Bit 5: IBF (Input Buffer Full) output for port A. Bit 6: ACK* (Acknowledge) input for port A. Data flow direction control for 8304 via jumper 105-111 Bit 7: OBF* (Output Buffer Full) output for port A.
B Mode 0 Input FFEA	1XXXX01X	Positive True	8304 at U5	None	104-109 As shipped	Enable Input at U5	Port A: None Port C: None unless port A is in mode 1 or 2

TABLE 3-2. PARALLEL I/O PORT CONFIGURATION SUMMARY (continued)

PORT AND MODE	CONTROL WORD	CONNECTOR POLARITY	DRIVER/TERMINATOR NETWORK	JUMPER ACTION DELETE	JUMPER ACTION ADD	EFFECT	PORT RESTRICTIONS
B Mode 0 Output (Latched)	1XXXX00X	Positive True	8304 at U5	104-109	104-107	Enable Output at U5	Port A: None Port C: None unless port A is in mode 1 or 2
B Mode 1 Input (Strobed)	1XXXX11X	Positive True	8304 at U5	None	104-109 As shipped	Enable Input at U5	Port A: None Port C: Performs the following dedicated functions: Bit 0: INTR (Interrupt Request) output for port B. Bit 1: IBF (Input Buffer Full) output for port E5H. Bit 2: STB* (Strobe) input for port B. Bit 3: Can be used as input or output if port A is in mode 0. Bits 4 to 7: Can be used as input or output if port A is in mode 0 or in some combinations where port A is in mode 1. These bits are always dedicated when port is in mode 2.
B Mode 1 Output (Latched)	1XXXX10X	Positive True	8304 at U5	104-109	104-107	Enable Output at U5	Port A: None Port C: Performs the following dedicated functions: Bit 0: INTR (Interrupt Request) output for port B. Bit 1: OBF* (Output Buffer Full) output for port B. Bit 2: ACK* (Acknowledge) input for port. Bit 3: Can be used as input or output if port A is in mode 0 Bit 4 to 7: Can be used as input or output if port A is in mode 0 in some combinations where port 1 is in mode 1. These bits are always dedicated when port is in mode 2.
C Mode 0 High Order Bits Input FFEC	100X10XX	Positive True	Termination Network at U4				Port A: Must be in mode 0 for all four bits to be available. Port B: Must be in mode 0 for all four bits to be available.
C Mode 0 Low Order Bits Input	100XX0X1	Positive True	Termination Network at U13				Port A: Must be in mode 0 for all four bits to be available. Port B: Must be in mode 0 for all four bits to be available.
C Mode 0 High Order Bits Output (Latched)	100X00XX	Positive True	Driver Network at U4				Port A: Must be in mode 0 for all four bits to be available. Port B: Must be in mode 0 for all four bits to be available.
C Mode 0 Low Order Bits Output (Latched)	100XX0X0	Positive True	Driver Network at U13				Port A: Must be in mode 0 for all four bits to be available. Port B: Must be in mode 0 for all four bits to be available.

Am8255A OPERATION CONTROL WORD FORMAT

The operation control word (bit 7=1) defines three basic modes of operation.

- Mode 0 = Basic Input/Output
- Mode 1 = Strobed Input/Output
- Mode 2 = Bidirectional Bus

The modes for port A and B can be separately defined, while port C is divided into two 4 bit ports as required by the port A and port B definitions. Table 3-2 provides a summary of mode definitions and port restrictions. The mode control word format is shown in figure 3-7.

Am8255A BIT SET/RESET CONTROL WORD

When operating in mode 1 or 2, the bits of the port C can be set or reset using the bit set/reset control word. The functions of some port C bits are defined by port A and B operations in modes 1 and 2. Refer to table 3-2 for port C bit definitions in modes 1 and 2. Figure 3-8 shows the bit set/reset control word format.

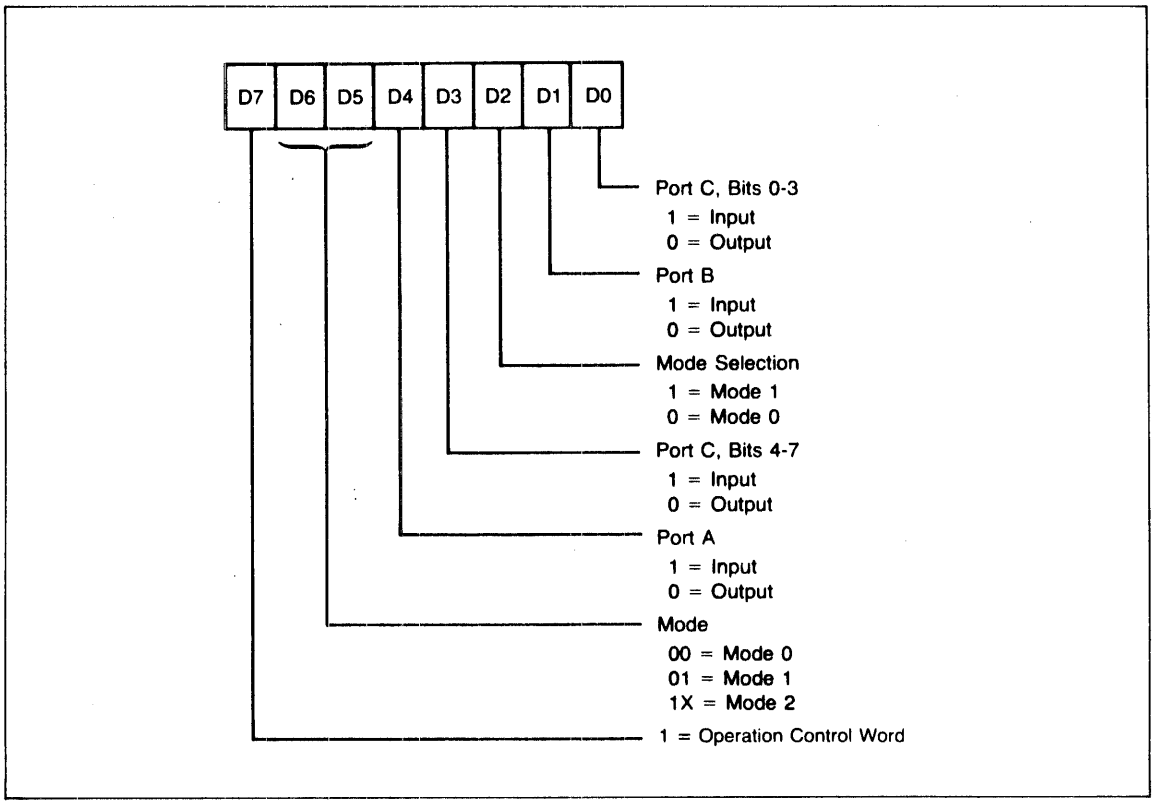


Figure 3-7. Am8255A Operation Control Word Format

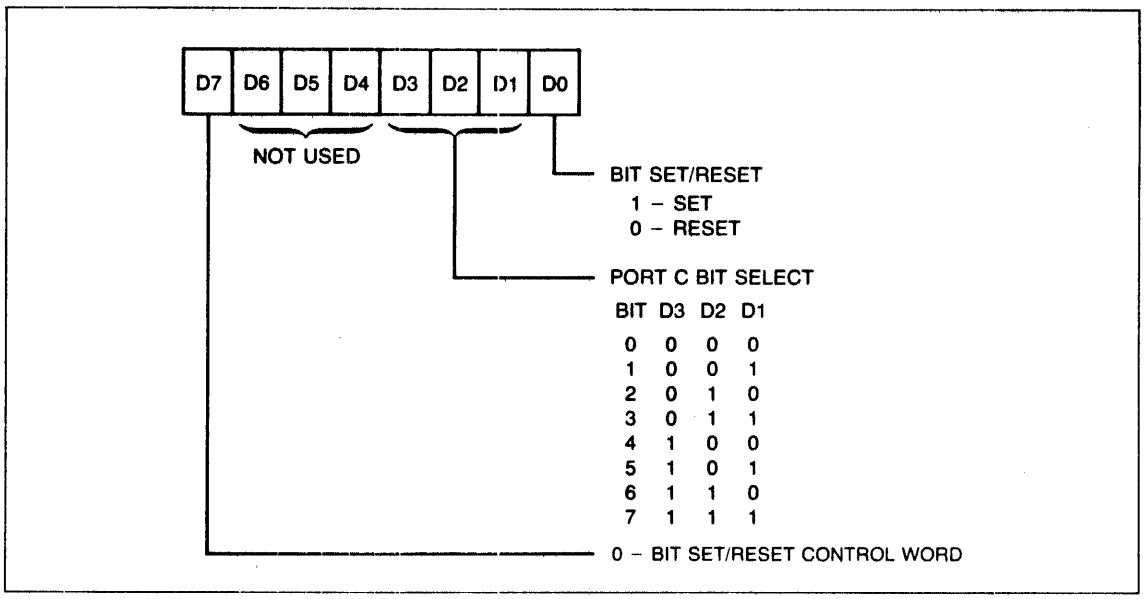


Figure 3-8. Bit Set/Reset Control Word Format

INTERRUPT CONTROL PROGRAMMING

An 8259A Programmable Interrupt Controller device provides priority resolution for eight interrupt levels. An interrupt matrix on the Am96/4116 provides for connecting the eight interrupt inputs to 24 possible interrupt sources. The 8259A has the capability to determine which unmasked input has the highest priority. A higher priority input will interrupt any lower priority input being serviced. A lower priority interrupt will be held for later service.

NOTE

When using Multibus interrupts, the 8259A must be used in the edge trigger mode.

INITIALIZATION

The 8259A accepts two types of command words, Initialization Command Words (ICWs) and Operation Command Words (OCWs). Before normal operation can occur, the 8259A must be initialized. Initialization consists of three ICWs, ICW1, ICW2, and ICW4. The ICWs are shown in figure 3-9.

The ICW1 format for use with the Am96/4116 should be 13 hex for edge triggering or 1B hex for level triggering, written to address FFC8. Bit 0 should always be a 1, because ICW4 is required for a 16-bit microprocessor. Since only one 8259A is used, bit 1 should always be set. Bit 2 is a don't care and bit 3 determines the type of triggering at the interrupt inputs. The Initialization Control Word is defined as ICW1 when address bit 1 is zero and ICW bit 4 is set.

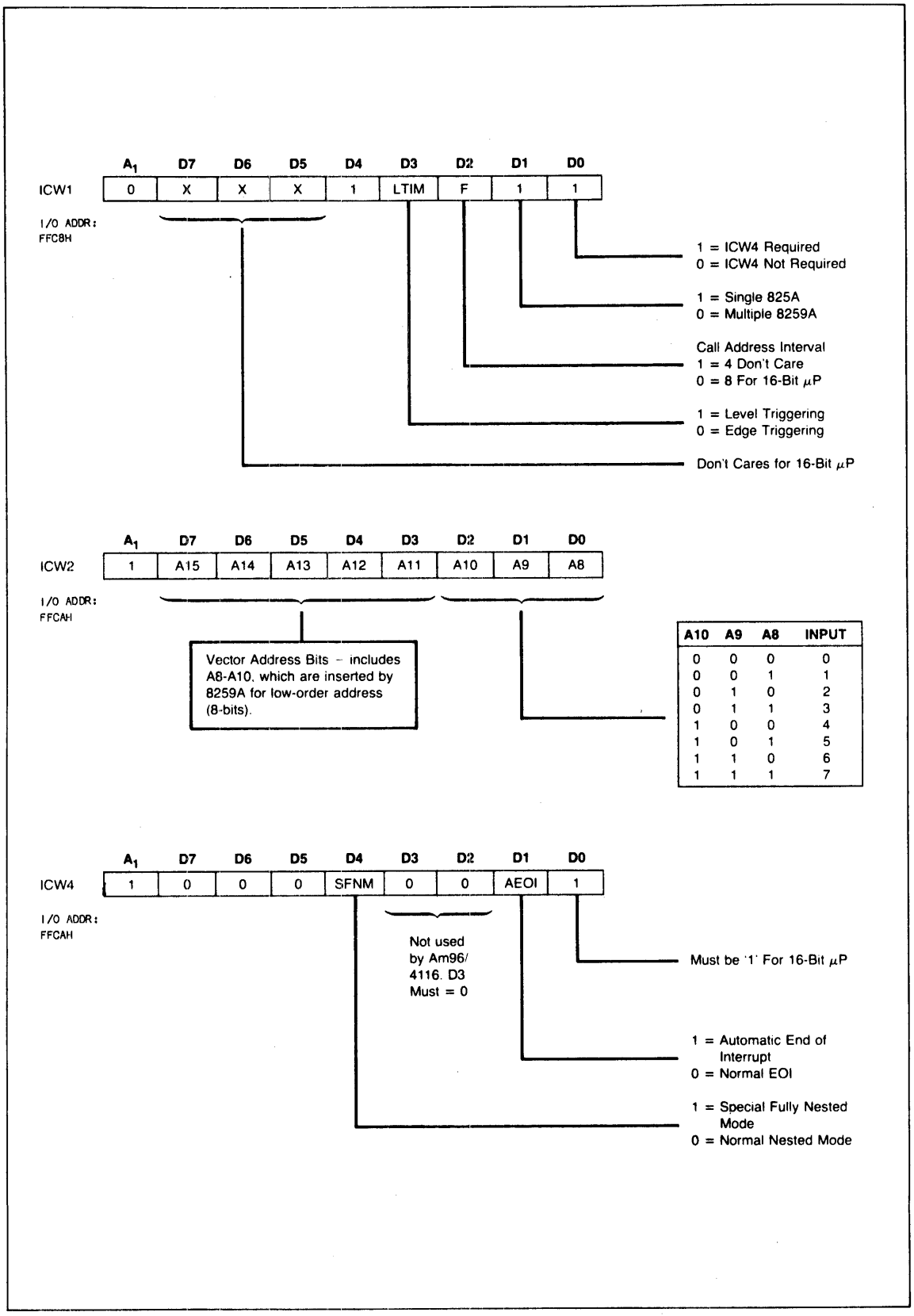


Figure 3-9. Initialization Control Word (ICW) Formats

The next ICW expected by the 8259A is ICW2. The ICW2 format uses bits 3 to 7 (A11 to A15) to determine part of the interrupt vector. The three lower bits, 0 to 2, of ICW2 become address bits 8 to 10 and are inserted by the 8259A to form the complete interrupt vector. ICW2 bits 3 to 7 are determined by the programmer.

Initialization Control Word ICW4 is the next to be programmed into the 8259A. Bit 0 of ICW4 must be set for use with the Am96/4116. When an interrupt is acknowledged, two bytes are output to the bus. The first byte is ignored and the second byte contains the interrupt vector.

If ICW4 bit 1 is zero, the CPU must output an End of Interrupt (EOI) command to the 8259A. If bit 1 is set, then an Automatic EOI (AEOI) will be generated at the trailing edge of the second (last) IACK pulse. ICW4 bits 2 and 3 should be zeros.

OPERATION CONTROL

The 8259A uses Operation Control Words (OCWs) to set interrupt mask bits, command various operations, and allow the CPU to read the Interrupt Request Register (IRR) and Interrupt Service Register (ISR) to determine status. Figure 3-10 illustrates the three OCWs. OCW1 is the interrupt mask register. When a particular bit is set, the corresponding interrupt input is masked (inhibited). Any bits cleared will enable the corresponding interrupts. Reading the IRR allows the programmer to look at which bits are masked or unmasked. Bit 0 of OCW1 is input 0 and bit 7 represents input 7.

The OCW2 format uses bits 5 through 7 for control of the Rotate and EOI modes. Figure 3-10 illustrates the various modes. Bits 0 to 2 are used to indicate a particular interrupt level to be controlled. The following are descriptions of the OCW2 commands:

Non-Specific EOI - Automatically resets the highest ISR bit of the ones that are set.

Specific EOI - Resets only the ISR bit specified by bits L0-L2 of OCW2.

Rotate at EOI Automatically (Mode A) - Rotates priorities after receiving an EOI or AEOI command. Figure 3-9 illustrates the rotate after level 2 interrupt was serviced and an EOI received.

Rotate at EOI (Mode B) - Allows the programmer to fix the bottom priority (bits L0-L2) in order to fix all other priorities. if level 3 is fixed as the lowest priority device, then level 4 will be the highest.

Set Rotate A F/F - Allows for automatic rotation of priorities when the AEOI mode is programmed.

Clear Rotate A F/F - Disables automatic rotation on AEOI.

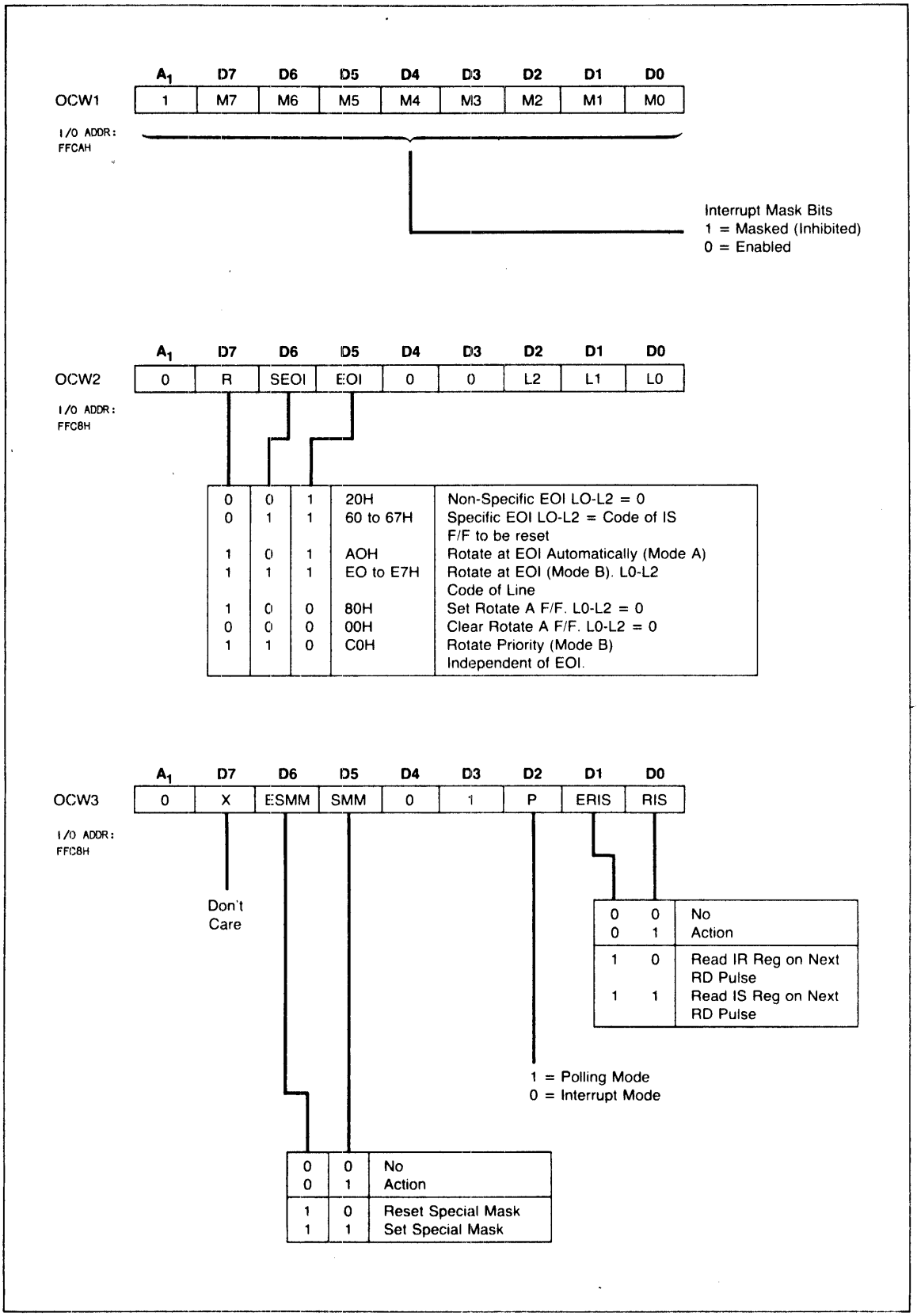


Figure 3-10. Operation Control Word (OCW) Formats

Rotate Priority (Mode B) Independent of EOI - Same as Rotate at EOI (Mode B), except that EOI is not required. Fixing of priorities may be done at any time.

The third Operation Control Word (OCW3) has two basic functions. Bits 0 and 1 are used to read either the Interrupt Service Register (ISR) or the Interrupt Request Register (IRR) to determine the interrupt status. The second function is to set or reset the Special Mask Mode. When a mask bit is set in OCW1, the Special Mask Mode inhibits further interrupts at that level and enables interrupts from other levels, lower as well as higher, that are not masked. This permits inhibiting only the masked bits set in OCW1, even if an EOI command was not received to reset the corresponding ISR bit.

Bit 2 of OCW3 selects either the polling mode (bit 2 = 1) or interrupt mode (bit 2 = 0). When the polling mode is active, a CPU read at address FFC8H is treated as an interrupt acknowledge. The corresponding ISR bit is set to indicate which interrupt input needs service. The byte read at FFC8H contains two pieces of information; bit 7 is set if an interrupt request exists, and the three least significant bits (0 to 2) are coded (000 to 111) to indicate the interrupt level. The software has the task of determining how to handle requests.

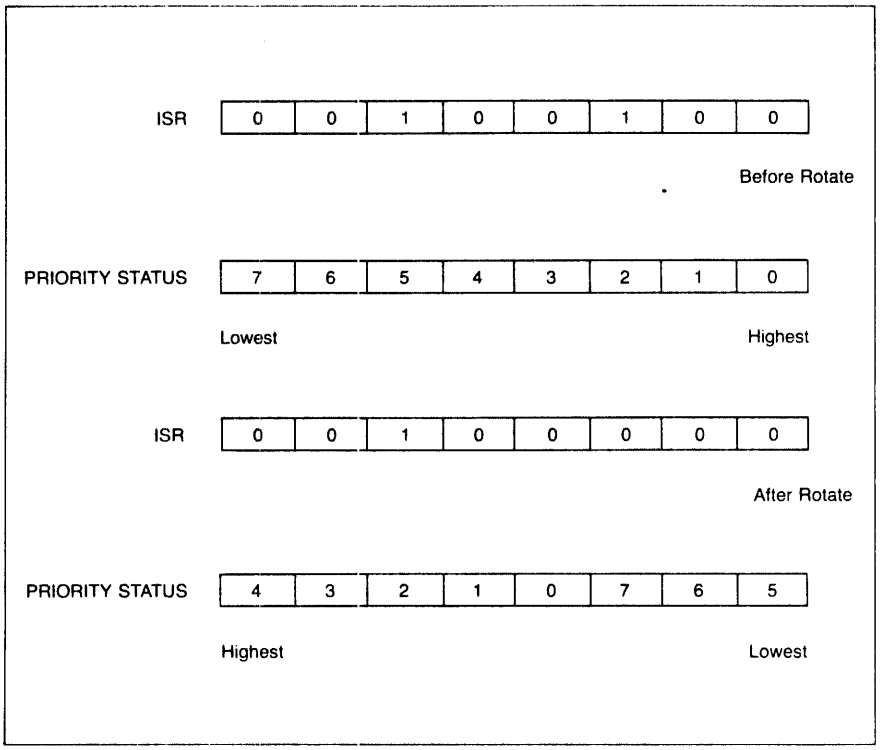


Figure 3-11. Rotating Priority Mode A (Automatic Rotation)

SYSTEM TIMING CONTROLLER PROGRAMMING

An Am9513 system timing controller is used to provide the timing and counting functions performed by the Am96/4116. The System Timing Controller contains many control elements that allow it to be customized for particular applications as well as dynamically reconfigured under program control. These control elements, which include comparators, registers, and counters, are summarized in table 3-3. Most of the registers can be both written to and read from under host processor control. Control elements within the system timing controller are accessed by hexadecimal address FFD2.

TABLE 3-3. CONTROL ELEMENT SUMMARY

CONTROL ELEMENT	BIT SIZE	QUANTITY
Output Control Bit	1	5
FOUT Divider Counter	4	1
Data Pointer Counter	5	1
Status Register	6	1
Command Register	8	1
Frequency Scaling Counter	16	1
Master Mode Register	16	1
Alarm Register	16	2
Comparator	16	2
Counter Mode Register	16	5
Counter Load Register	16	5
Counter Hold Register	16	5
General Counter	16	5

COMMAND REGISTER

Direct host processor software control over many general counter functions is provided by the 8-bit command register. The host CPU accesses the command register by performing an I/O write to hex address FFD2. Command register codes and a brief description of each function is presented in table 3-4. Six of the command types are used for direct software control of the counting process and they each contain a

five-bit S field. In a linear-select fashion, each bit in the S field corresponds to one of the five general counters (S1 = Counter 1, S2 = Counter 2, etc.). When an S bit is a one, the specified operation is performed on the counter so designated; when an S bit is a zero, no operation occurs for the corresponding counter. This type of command format has three basic advantages:

- Host software is conserved by allowing any combination of counters to be acted on by a single command.
- Facilitates simultaneous action of multiple counters where synchronization of commands is important.
- Allows counter specific service routine to control individual counters regardless of the operating context of other counters.

STATUS REGISTER

The 8-bit read-only status register indicates the state of the Byte Pointer bit in the Data Pointer register and the state of the OUT signal for each of the general counters shown in figure 3-12. The OUT signals reported are those internal to the chip just before the three state interface buffer circuitry. Thus, the status register reflects the results of polarity control over the OUT signals, and continues to indicate the counter condition even when the output is off.

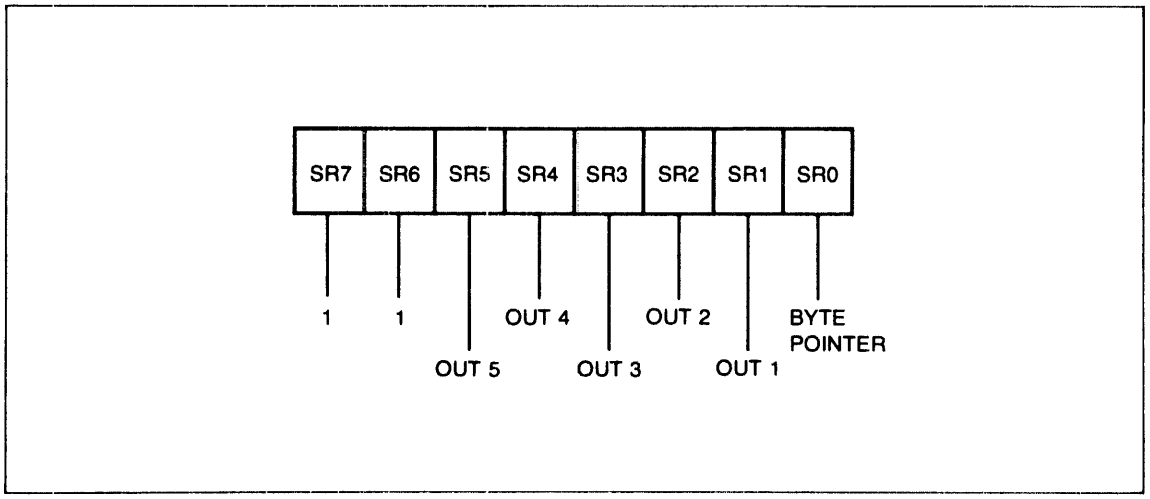


Figure 3-12. Status Register Bits

TABLE 3-4. COMMAND SUMMARY

Command Code								Command Description
C7	C6	C5	C4	C3	C2	C1	C0	
0	0	0	E2	E1	G4	G2	G1	Load Data Pointer register with contents of E and G fields. (G ≠ 000, G ≠ 110)
0	0	1	S5	S4	S3	S2	S1	Arm counting for all selected counters
0	1	0	S5	S4	S3	S2	S1	Load contents of specified source into all selected counters
0	1	1	S5	S4	S3	S2	S1	Load and Arm all selected counters
1	0	0	S5	S4	S3	S2	S1	Disarm and Save all selected counters
1	0	1	S5	S4	S3	S2	S1	Save all selected counters in hold register
1	1	0	S5	S4	S3	S2	S1	Disarm all selected counters
1	1	1	0	1	N4	N2	N1	Set output bit N (001 ≤ N ≤ 101)
1	1	1	0	0	N4	N2	N1	Clear output bit N (001 ≤ N ≤ 101)
1	1	1	1	0	N4	N2	N1	Step counter N (001 ≤ N ≤ 101)
1	1	1	0	1	0	0	0	Set MM14 (Disable Data Pointer Sequencing)
1	1	1	0	1	1	1	0	Set MM12 (Gate off FOUT)
1	1	1	0	1	1	1	1	Set MM13 (Enter 16-bit bus mode)
1	1	1	0	0	0	0	0	Clear MM14 (Enable Data Pointer Sequencing)
1	1	1	0	0	1	1	0	Clear MM12 (Gate on FOUT)
1	1	1	0	0	1	1	1	Clear MM13 (Enter 8-bit bus mode)
1	1	1	1	1	1	1	1	Master reset

MASTER MODE REGISTER

The 16-bit Master Mode (MM) register is used to control those internal activities that are not controlled by the individual Counter Mode registers. This includes frequency control, time-of-day operation, comparator controls, data bus width and data pointer sequencing. Figure 3-13 shows the bit assignments for the Master Mode register. Each control field is described in the following paragraphs.

After power-on reset or a Master Reset command, the Master Mode register is cleared to an all zero condition. This results in the following configuration:

Time-of-day disabled
Both Comparators disabled
FOUT Source is frequency F1
FOUT Divider set for divide-by-16
FOUT gated on
Data Bus 8 bits wide
Data Pointer Sequencing enabled
Frequency Scaler divides in binary

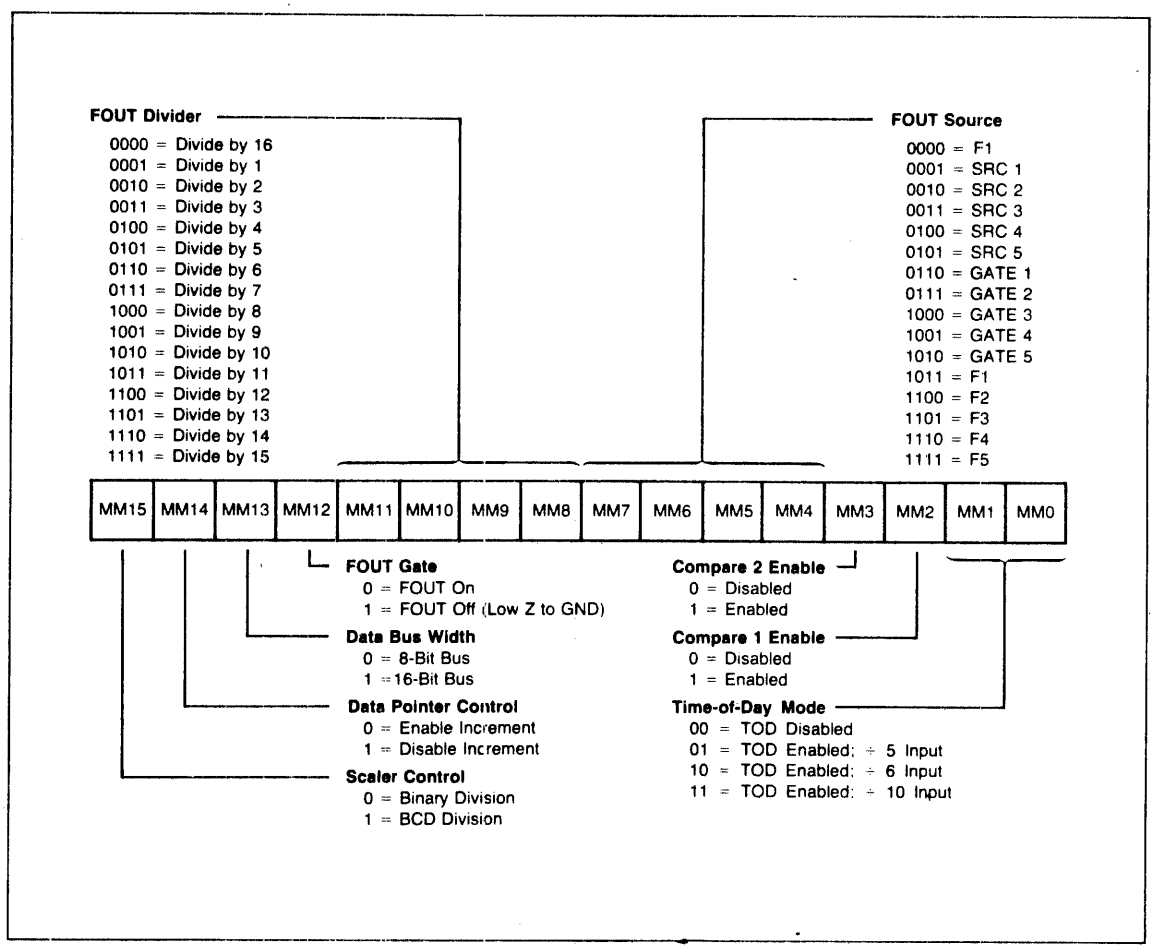


Figure 3-13. Master Mode Register Bits

TIME OF DAY

Bits MM0 and MM1 of the Master Mode register specify the time-of-day (TOD) options. When MM0 = 0 and MM1 = 0, the special logic used to implement TOD is disabled and counters 1 and 2 will operate in exactly the same ways as counters 3, 4, and 5. When MM0 = 1 or MM1 = 1, additional counter decoding and control logic is enabled for counters 1 and 2 which causes them to turn-over at the counts that generate appropriate 24-hour TOD accumulations.

Figure 3-14 shows the counter configurations for TOD operation. The two most significant decades of Counter 2 contain the hours digits and they can hold a maximum count of 23 hours. The two least significant decades of Counter 2 indicate minutes and will hold values up to 59. The three most significant decades of Counter 1 indicate seconds and will contain values up to 59.9. The least significant decade of Counter 1 is used to scale the input frequency in order to output

tenth-of-second periods into the next decade. It can be set up to divide by five (MM0 = 1, MM1 = 0), divide by six (MM0 = 0, MM1 = 1), or divide by ten (MM0 = 1, MM1 = 1). The input frequency, therefore, for real-time clocking can be, respectively, 50Hz, 60Hz or 100Hz. For the Am96/4116, an input frequency of 2.4576 MHz must be divided by 40,960 and the TOD input divider set 60 Hz input. This is accomplished by selecting FOUT Source for F4, scaler control to binary and FOUT Divider to divide-by-10. The Master Mode Register bits provide the proper configuration. A jumper (188 to 189) must be connected also.

NOTE

When TOD is used, the serial Baud Rates cannot be taken from FOUT (see paragraph 3-46).

COMPARATOR ENABLE

Bits MM2 and MM3 control the Comparators associated with Counters 1 and 2. When a Comparator is enabled, its output is substituted for the normal counter output on the associated OUT1 or OUT2 pin. Once the compare output is true, it remains true until the count changes and the comparison therefore goes false. The two Comparators can always be used individually in any operating mode. One special case occurs when the time-of-day option is selected and both Comparators are enabled. The operation of Comparator 2 is then conditioned by Comparator 1 so that a full 32-bit compare must be true in order to generate a true signal on OUT2. OUT1 continues, as usual, to reflect the state of the 16-bit comparison between Alarm 1 and Counter 1.

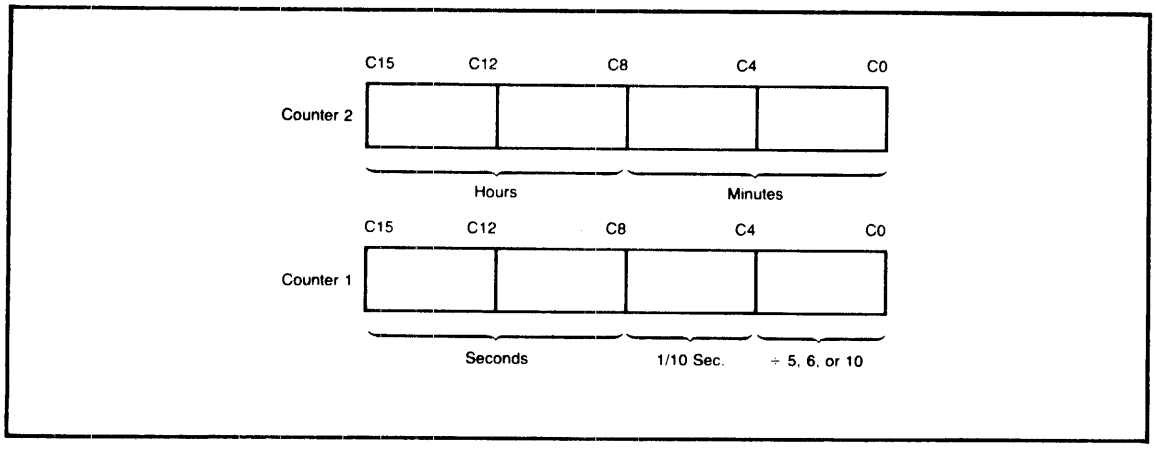


Figure 3-14. Time-of-Day Configuration

FOUT SOURCE

Master Mode bits MM4 through MM7 specify the source input for the FOUT Divider. Fifteen inputs are available for selection and they include the five Source pins, the five Gate pins and the five internal frequencies derived from the oscillator. The 16th combination of the four control bits (all zeros) is used to assure that an active frequency is available on FOUT following a reset.

FOUT DIVIDER

Bits MM8 through MM11 specify the dividing ratio for the FOUT Divider. The FOUT source selected by bits MM4 through MM7 is divided by an integer value between 1 and 16, inclusive, and is then passed to the FOUT output buffer. The undivided oscillator frequency is available at FOUT simply by selecting the F1 source and a dividing ratio of one. After power-on or reset, the FOUT Divider is set to divide by sixteen.

FOUT GATE

Master Mode bit MM12 provides a software gating capability for the FOUT signal. When MM12 = 1, FOUT is off and in a low impedance state to ground. MM12 can be set or cleared in conjunction with the loading of the other bits in the Master Mode register; alternatively, there are commands that allow MM12 to be individually set or cleared directly without changing any other Master Mode bits. After power-up or reset, FOUT is gated on.

BUS WIDTH

Bit MM13 controls the multiplexer at the data bus interface in order to configure the part for an 8-bit or 16-bit external bus. Only the 16-bit configuration is used on the Am96/4116. The internal bus is always 16-bits wide. When MM13 = 0, 16-bit internal data is transferred a byte at a time to and from the eight low-order external data bus lines.

DATA POINTER SEQUENCE

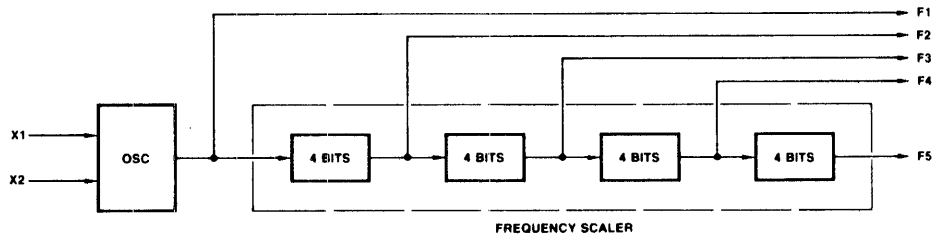
Bit MM14 controls the Data Pointer logic to enable or disable the automatic sequencing functions. When MM14 = 1, the contents of the Data Pointer can be changed only directly by entering a command. When MM14 = 0, several types of automatic Data Pointer sequencing are available. Thus the host processor, by controlling MM14, can repetitively read/write a single internal location, or can sequentially read/write groups of locations.

SCALER RATIOS

Master Mode bit MM15 controls the counting configuration of the Frequency Scaler counter. When MM15 = 0, the Scaler divides the oscillator frequency in binary steps so that each subfrequency is 1/16 of the preceding frequency. When MM15 = 1, the Scaler divides in BCD steps so that adjacent frequencies are related by ratios of 10 instead of 16.

FREQUENCY SCALING COUNTER

A 16-bit scaling counter divides the output of the on-chip oscillator into four additional sub-frequencies. This provides a total of five internal frequencies that can be routed to any of the general counters and to the FOUT divider. The scaler is tapped every four bits and can be programmed to divide in binary or in BCD. The combinations of frequencies thus available are shown in figure 3-15. For example, if the base oscillator frequency is 8MHz, the F4 frequency will be 8KHz when BCD scaling is selected. If the base oscillator frequency is 8MHz, the F3 frequency will be 31.25KHz when binary scaling is selected. The control bit that selects BCD or binary scaling is located in the Master Mode register.



Frequency	BCD Scaling MM15 = 1	Binary Scaling MM15 = 0
F1	OSC	OSC
F2	F1 ÷ 10	F1 ÷ 16
F3	F1 ÷ 100	F1 ÷ 256
F4	F1 ÷ 1,000	F1 ÷ 4,096
F5	F1 ÷ 10,000	F1 ÷ 65,536

Figure 3-15. Frequency Scaler Ratios

FOUT DIVIDER COUNTER

The 4-bit FOUT Divider is used to subdivide the source selected for the Frequency Out pin. It provides for division by an integer from 1 to 16, inclusive. The dividing ratio is selected by a 4-bit field in the Master Mode register. The FOUT Divider is intended to allow a relatively low FOUT frequency for use as a system clock while still permitting higher resolution internal frequencies from the crystal oscillator. With a crystal frequency of 8MHz, for example, a divider ratio of four with F1 selected would provide an FOUT rate of 2MHz. In applications that do not use FOUT as a frequency source or as a clock, the Divider forms a simple general-purpose programmable 4-bit divider that can use any of the general input pins.

DATA POINTER COUNTER

The 6-bit Data Pointer is used to control internal addressing for data bus transfers via the data port. The Data Pointer is directly loaded by command and can be automatically incremented following data transfers. Figure 3-16 shows the pointer configuration.

The Byte Pointer bit is only active when the data bus is operating with its 8-bit width option. Whenever the Data Pointer is loaded, the Byte Pointer bit cleared to zero. The Byte Pointer toggles following each 8-bit data transfer with an 8-bit data bus (MM13 = 0), or it always remains reset with the 16-bit data bus option (MM13 = 1).

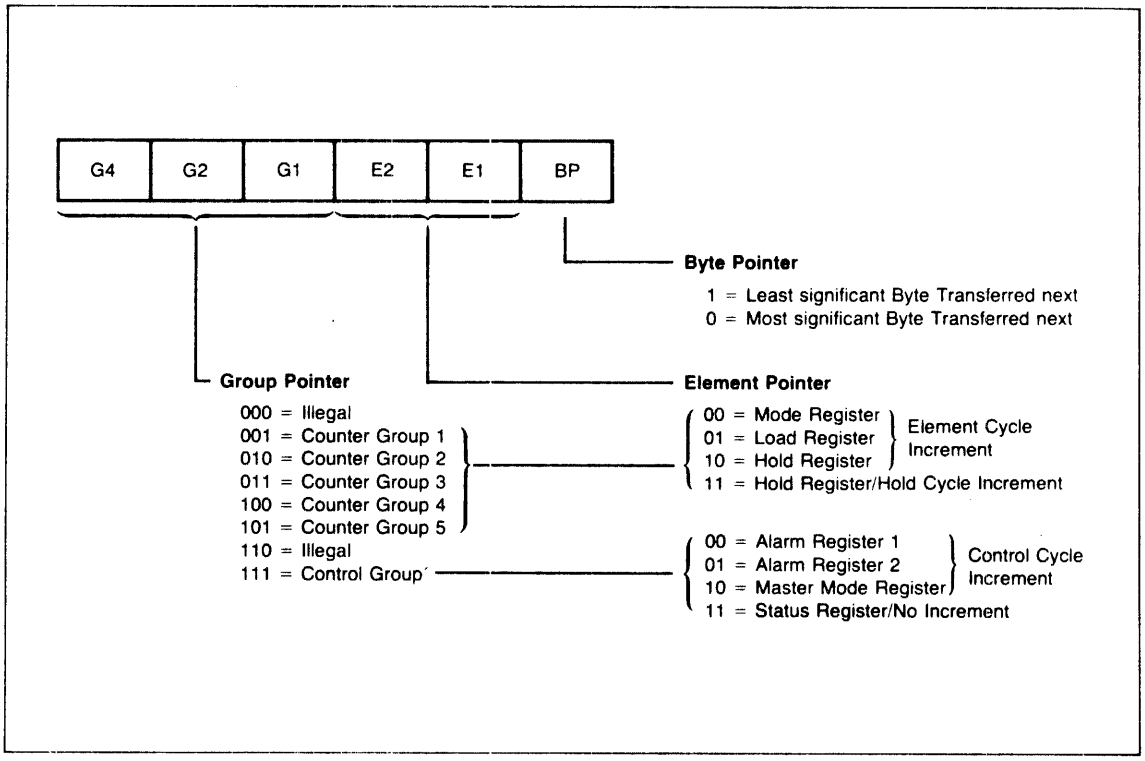


Figure 3-16. Data Pointer Counter

The Element Pointer field definitions vary depending on the state of the Group Pointer. When one of the Counter Groups is specified, the Element field selects one of the three 16-bit registers within the group for access. The element Pointer also selects a type of sequencing that may be used.

When control bit MM14 = 1, automatic sequencing of the Data Pointer register is disabled and the contents of the Group and Element fields will change only when the Data Pointer is loaded by command. This allows the host processor to repetitively access any given internal data register without intervening commands.

When control bit MM14 = 0, the Data Pointer automatically sequences through new pointer values as information is transferred into or out of the data port. Several types of sequencing operations are available depending on the data bus width being used and the initial Data Pointer value entered by command. When E1 = 0 or E2 = 0, and MM14 = 0, the Element field is automatically sequenced through three values: 00, 01 and 10. When the transition from 10 to 00 occurs, the Group Field is also incremented by one. Note that the Element field in this case does not sequence to a value of 11. When E1 = 1 and E2 = 1, only the Group field is sequenced. This allows the Hold registers to be sequentially accessed while bypassing the Mode and Load registers.

Once the Am9513 is operating, the two illegal codes shown in figure 3-16 for the Group Pointer field will not occur because:

- no commands will load the illegal values into the Group Pointer, and
- no automatic sequencing will change the Group Pointer to an illegal value.

The illegal codes can occur following power-up and the Data Pointer should always be loaded with some appropriate value during initialization.

When the Control Group is specified (G4, G2, G1 = 111), automatic increment of the Group field is disabled and the Element field will circulate through the first three values (assuming MM14 = 0). When one of the Counter Groups is specified, the G field can increment through the five Counter Group values; it will not sequence into the illegal codes or into the Control Group.

PREFETCH LATCH

A Prefetch Latch is used for all read operations through the data port to reduce the read access time to internal Am9513 registers. Following each read or write operation through the Data Port, the Data Pointer register is updated to point to the next register to be accessed. Immediately following this update the new register data is transferred to a special Prefetch Latch at the interface pad logic. When the user

performs a subsequent read of the Data Port, the data bus drivers are enabled, outputting the pre-feteched data on the bus. Since the internal data register is accessed prior to the start of the read operation, its access time is transparent to the user. In order to keep the Prefetched data consistent with the Data Pointer, Prefetches are also performed after each write to the Data Pointer and after execution at the Load Data Pointer command. The following rules should be kept in mind regarding Data Port transfers:

- The data pointer register should always be reloaded before reading from the Data Port if a command other than Load Data Pointer was issued to the Am9513 following the last Data Port read or write. The Data Pointer does not have to be loaded again if the first Data Port transaction after a command entry is a write, since the Data Port write will automatically causes a new prefetch to occur.

- Operating modes, N, O, Q, and R allow the user to save the counter contents in the Hold register by applying an active-going gate edge. If the Data Pointer register had been pointing to the Hold register in question, the prefetched value will not correspond to the new value saved in the Hold register. To avoid reading an incorrect value, a new Load Data Pointer command should be issued before attempting to read the saved data. A Data Port write (to another register) will also initiate a prefetch; subsequent reads will access the recently saved Hold register data. Many systems will use the saving gate edge to interrupt the host CPU. In systems such as this the interrupt service routine should issue a Load Data Pointer command prior to reading the saved data.

COUNTER LOGIC GROUPS

Each of the five Counter Logic Groups consists of a 16-bit general counter with associated control and output logic, a 16-bit Load register, a 16-bit Hold register and a 16-bit Mode register. In addition, Counter Groups 1 and 2 also include 16-bit comparators and 16-bit Alarm registers. The comparator/alarm functions are controlled by the Master Mode register. The operation of the Counter Mode registers is the same for all five counters. The host CPU has both read and write access to all registers in the Counter Logic Groups. The counter itself is never directly accessed.

COUNTER LOAD REGISTER

The read/write Load register is used to control the effective length of the general counter. Any 16-bit value can be written into the Load register. That value can then be transferred into the counter each time the Terminal Count (TC) occurs. Terminal Count is defined as that period of time when the counter contents would have been zero if an external value had not been transferred into the counter. Thus, the terminal count frequency can be the input frequency divided by the

value in the Load register. In all operating modes, either Load or Hold will be transferred into the counter when TC occurs. In cases where values are being accumulated in the counter, the Load register action can become transparent by filling the Load register with all zeros.

COUNTER HOLD REGISTER

The 16-bit read/write Hold register is dual-purpose. It can be used in the same way as the Load register, thus offering an alternate source for modulo definition for the counter. The Hold register can also be used to store accumulated counter values for later transfer to the host processor. This allows the count to be sampled while the counting process proceeds without interruption. Transfer of the counter contents into the Hold register is accomplished by the hardware interface in some operating modes or by software commands at any time.

COUNTER MODE REGISTER

Each Counter Logic Group includes a Counter Mode (CM) register used to control all of the individual options available with its associated general counter. These options include output configuration, count control, count source and gating control. Figure 3-17 shows the bit assignments for the Counter Mode registers. The following paragraphs describe the control options in detail. Note that generally each counter is independently configured and does not depend on information outside its Counter Logic Group. The counter mode register should be loaded only when the counter is disarmed.

After power-on reset or a Master Reset command, the Counter Mode registers are initialized to a preset condition. The value entered is 0B00 hex and results in the following control configuration:

Output low impedance to ground

Count down

Count binary

Count once

Load register selected

No retriggering

F1 input source selected

Positive-true input polarity

No gating

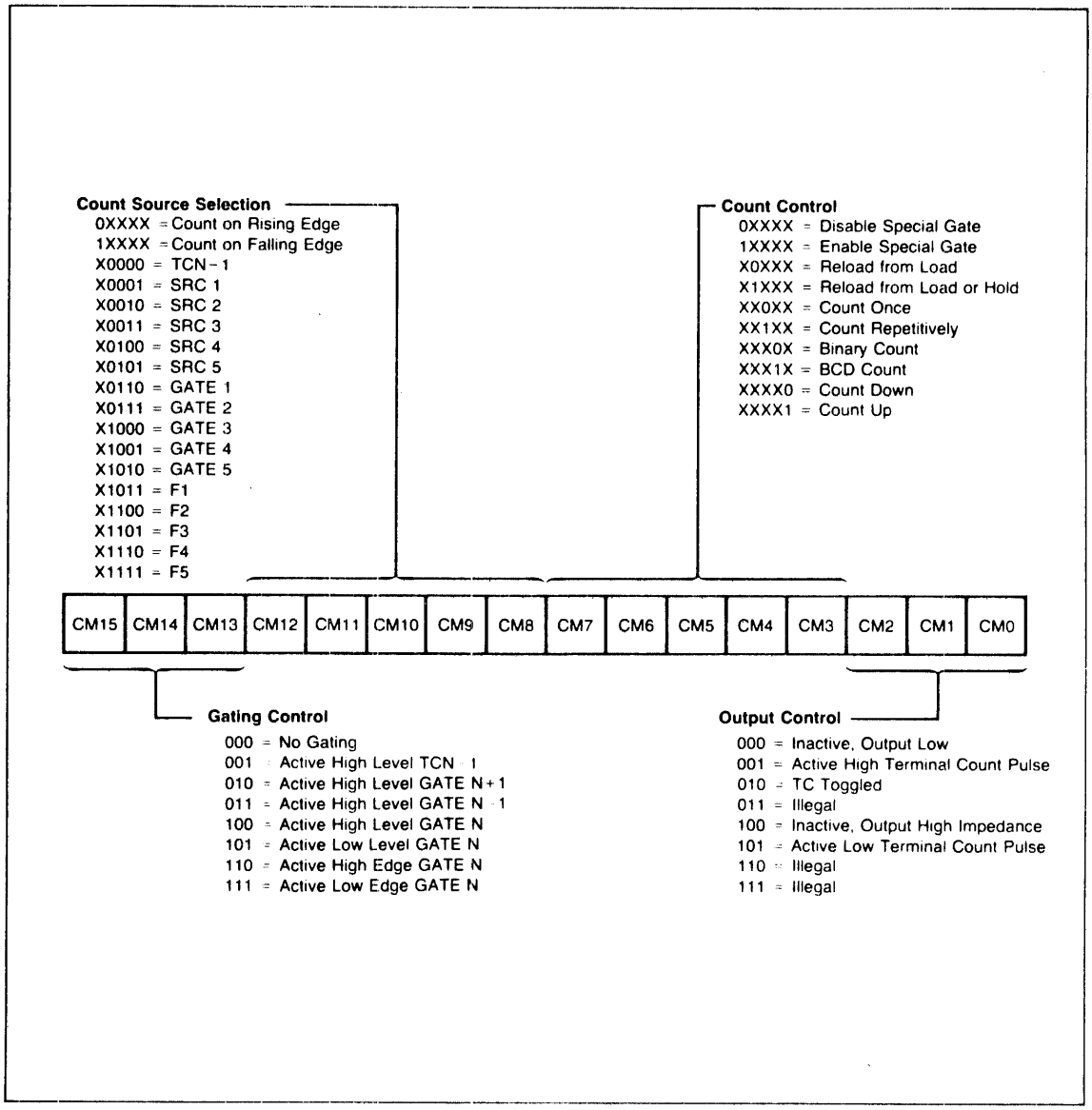


Figure 3-17. Counter Mode Register Bit Assignments

OUTPUT CONTROL

Counter Mode bits CM0 through CM2 specify the output control configuration. The OUT pin can be off and in a high impedance state or it can be off with a low impedance to ground. The six remaining combinations are split into active-high and active-low versions of the three basic output waveforms.

One output form available is called Terminal Count (TC) and represents the period of time that the counter reaches an equivalent value of zero. Figure 3-18 shows a Terminal Count pulse and an example context that generated it. Notice that the TC width is determined by the period of the counting source. Figure 3-18 assumes active-high source polarity, counter armed, gate active, counter decrementing and a reload value of K.

The counter will always be updated when TC occurs; the user can choose the source location and the value. If a non-zero value is picked, the counter will never really attain a zero state and TC will indicate the counter state that would have been zero had no parallel transfer occurred.

COUNT CONTROL

Counter Mode bits CM3 through CM7 specify the various options available for direct control of the counting process. Most of the control bits operate relatively independently of the others so that they can be combined freely to form many types of counting configurations.

Bit CM3 specifies incrementing or decrementing of the counter. For many timing and frequency division purposes, down-counting is preferred since the key value is identified when the counter reaches zero. Alternatively, for even counting or elapsed time applications, up-counting will be preferred so that accumulated values can be conveniently handled.

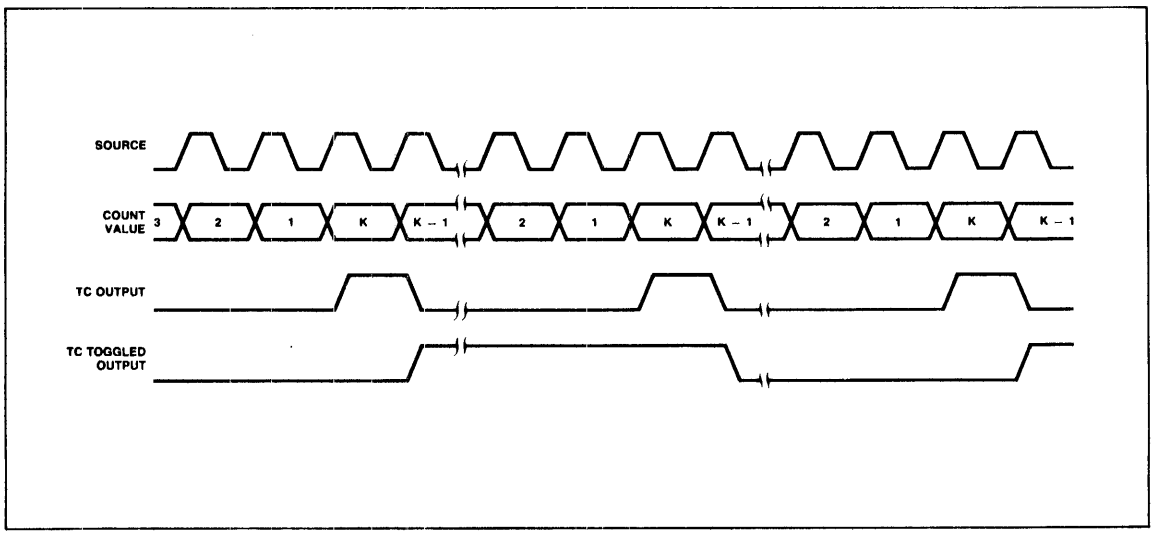


Figure 3-18. TC Waveform Format

Bit CM4 selects binary or BCD counting. This option greatly simplifies the interface with the host system by helping to minimize format conversions. Indeed, this capability can be used in some cases to make conversions.

Bit CM5 controls the repetition of the count process. When CM5 = 1, counting will proceed in the specified mode until the counter is disarmed or the mode is changed. When CM5 = 0, the count process will proceed only until one or two TC events occur. The counter is then disarmed automatically. The single or double TC requirement depends on the state of other control bits.

When TC occurs, the counter is always reloaded with a value from either the Load register or the Hold register. Bit CM6 specifies the source options for reloading the counter. When CM6 = 0, the contents of the Load register will be transferred into the counter at every occurrence of TC, and when CM6 = 1, the counter reload location will be either the Load or Hold Register. These locations can alternate or can be controlled by a GATE pin. With alternating sources and with the toggle output selected, the duty cycle of the output waveform is controlled by the relative Load and Hold values and very fine resolution of duty cycle ratios will then be available in many circumstances.

Bit CM7 controls the special gating functions that allow retriggering and the selection of Load or Hold sources for counter reloading. The use and definition of CM7 depends on the status of the Gating Control field and bits CM5 and CM6.

When some form of Gating is specified, CM7 controls hardware retriggering. In this case, when CM7 = 0, hardware retriggering does not occur; when CM7 = 1, the counter is reloaded any time an active Gate input occurs. Any time that retriggering occurs, the Counter contents are transferred into the Hold register. When No Gating is specified, the definition of CM7 changes. In this case, when CM7 = 0, the Gate input has no effect on the counting; when CM7 = 1, the Gate input specifies the source used to reload the counter when TC occurs.

COUNT SOURCE SELECTION

Counter Mode bits CM8 through CM12 specify the source used as input to the counter and the active edge that is counted. Bit CM12 controls the polarity for all the sources with logic zero indicating active high and logic one indicating active low. Bits CM8 through CM11 select one of sixteen counting sources to route to the counter input. Five of the available inputs are internal frequencies derived from the internal oscillator. Ten of the available inputs are interface pins; five are labeled SRC and five are labeled GATE.

The sixteenth available input is the TC output from the adjacent lower numbered counter. (The Counter 5 TC wraps around to the Counter 1 input.) This option allows internal concatenating that permits very long counts to be accumulated. Since all five counters can be

concatenated, it is possible to configure a counter that is 80 bits long on one Am9513 chip. When TCN-1 is the source, the count ripples between the connected counters. External connections can also be made, and can use the toggle bit for even longer counts. This is easily accomplished by selecting a TOG output mode and wiring OUTN to one of the SRC inputs.

GATING CONTROL

Counter Mode bits CM13 through CM15 specify the hardware gating options. When no gating is selected (000), the counter will proceed unconditionally as long as it is armed. For any other gating mode, the count process is conditioned by the specified gating configuration.

For a code of 100 in this field, counting can proceed only when the pin labeled GATEN associated with Counter N is at a logic high level. When it goes low, counting is simply suspended until Gate goes high again. A code of 101 performs the same function with an opposite active polarity. Codes 010 and 011 offer the same functions as 100, but specify alternate input pins as Gating Sources. This allows any of three interface pins to be used as gates for a given counter. On Counter 4, for example, pin 34, pin 35 or pin 36 can be used to perform the gating function. This also allows a single Gate pin to simultaneously control up to three counters.

For codes of 110 or 111 in this field, counting proceeds after the specified active Gate edge until one or two TC events occur. Within this interval the Gate input is ignored, except for the retriggering option. When repetition is selected, a cycle is repeated as soon as another Gate edge occurs. This mode is useful when implementing a digital single-shot since the gate can serve as a convenient firing trigger.

A 001 code in this field selects the TC output from the adjacent lower-numbered counter as the gate. Thus, one counter can be configured to generate a counting window for another counter.

ALARM REGISTERS AND COMPARATORS

Added functions are available in the Counter Logic Groups for counters 1 and 2. Each contains a 16-bit Alarm register and a 16-bit Comparator. When the value in the counter reaches the value in the Alarm register, the Comparator output will go true. The Master Mode register contains control bits to individually enable/disable the comparators. When enabled, the comparator output appears on the OUT pin of the associated counter in place of the normal counter output. The output will remain true as long as the comparison is true, that is, until the next input causes the count to change.

In some applications, values are being accumulated and recognition of a particular count event is desired. This might be accomplished by preloading the counter with the desired value and then counting it down toward zero. Alternatively, the counter can be initialized with zero and the desired value entered into the Alarm register. With the Comparator enabled, an OUT transition will then occur when the value is reached, plus counts will continue to accumulate.

OUTPUT CONTROL BIT

The output control circuitry for each of the five counter groups includes a toggle flip-flop that can be used to generate various output waveforms. TC from the counter is the toggling signal and the output frequency can thus be half the TC frequency. The toggle can be initialized to either high or low state by command. More details of the toggle activity are included in the Counter Mode Register description.

BAUD RATE PROGRAMMING

The Am96/4116A uses the Am9513 System Timing Controller as the on-board clock source for the two serial ports. As shipped, both ports are set to function at 9600 baud. (FOUT from the Am9513). The Am9551 clock sources may jumpered to Am9513 OUT3 (U6) and OUT4 (U22). OUT3 and OUT4 are the outputs of counters 3 and 4 respectively. The jumpers should be located between pins 138 and 139 (U22) and pins 142 and 143 (U6). Table 3-5 lists the Load Register values to be programmed for the desired baud rate. The table assumes a frequency source of F1 and FOUT divide-by-one, which are selected by the programmer, and a synchronous communications. The counter output frequencies are 16X the baud rate. The maximum baud rate is 9600 for asynchronous and 38,400 for synchronous mode.

TABLE 3-5. BAUD RATE SELECTION

BAUD RATE	DECIMAL	HEX
9,600.0	16	0010
4,800.0	32	0020
2,400.0	64	0040
1,800.0	85	0055
1,200.0	128	0080
600.0	256	0100
300.0	512	0200
200.0	768	0300
150.0	1024	0400
134.5	1142	0476
110.0	1396	0574
75.0	2048	0800
50.0	3072	0C00

CHAPTER 4
THEORY OF OPERATION

INTRODUCTION

This chapter provides a functional description of the Am96/4116A MonoBoard Computer. Figure 4-1 is a block diagram of the Am96/4116A.

Both active high and active low signals appear on the schematics. To eliminate confusion and simplify presentation, the following convention is adhered to in this manual: whenever a signal is low-true, its mnemonic is followed by an asterisk (*). For example, MEMR* denotes a low-true signal. There is no asterisk for high-true signals.

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of an AmZ8002 16-bit microprocessor, clock circuitry, and associated buffer and control circuitry.

The AmZ8002 is a general purpose 16-bit CPU with a 16-bit multiplexed address and data bus, which can directly address 64K bytes (32K words) of memory. There are four status output lines (ST0 to ST3) to indicate the type of bus access; a Normal/System output for selecting Normal (user) or System (privileged) memory space; a Byte/Word output to permit addressing of either bytes (8-bit) or 16-bit words. Decoding of the status outputs is provided for I/O functions, code or data functions, and memory operations. One decoded signal is I-FETCH*, which can be jumpered and used externally to select either code or data areas of off-board memory. The Normal/System (N/S*) output can also be jumpered and used externally to select Normal or System areas of memory.

The clock circuit is made up of an 8 MHz oscillator, flip-flop (U83) and a clock driver circuit. The driver circuit is required to drive the AmZ8002. As shipped from the factory, jumpers are installed at pins 150-151, 153-154, and 163-164. Flip-flop U83 divides the oscillator output to provide a 4 MHz clock for the CPU.

A failsafe timer is available to generate a timeout (TIME OUT*) signal to interrupt the processor to prevent hanging up the CPU if memory or a device does not respond within approximately 10μs.

NOTE

It is recommended that the TIME OUT* signal be used as an interrupt source.

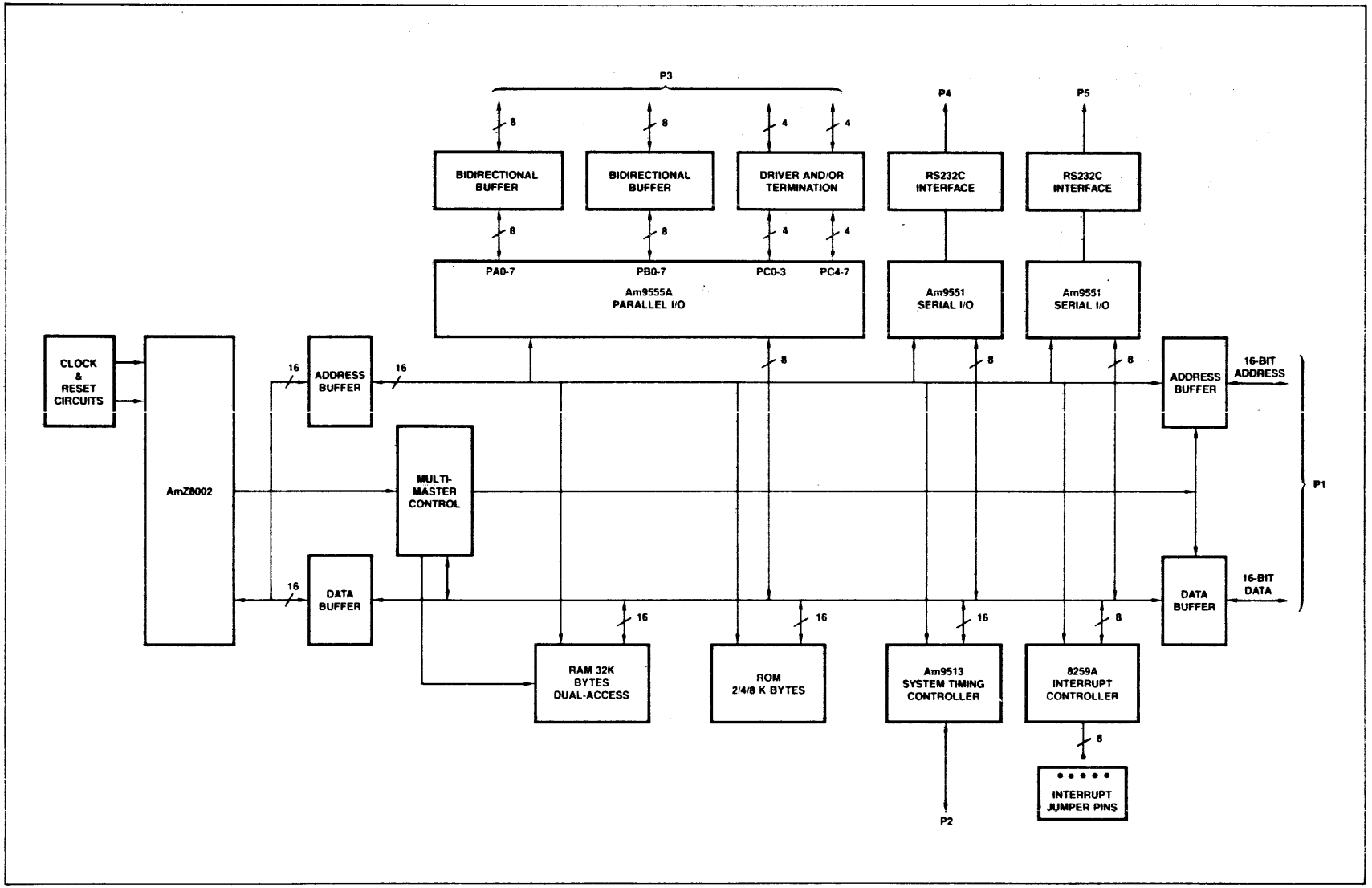


Figure 4-1. Am96/4116A MonoBoard Computer, Block Diagram

A circuit consisting of U37, U45, U26 and U84 provides power-on initialization for the Am96/4116. In addition, the INIT* pin (P1-14) may be used as an external reset input to the Am96/4116. A jumper position is available to permit initialization of other boards in the system as well. The jumper should be installed between pins 190 and 191.

The AmZ8002 shares a 16-bit data bus with the address bus. Two signals, address strobe (AS*) and data strobe (DS*) are used to multiplex the 16-bit bus. Bus transceivers U69 and U79 provide data bus buffering. The address lines are latched by U68 and U78 by an inverted AS* signal. Bus transceiver U94 and U86 provide buffered addresses to external locations and access to the on-board dual-port RAM. When BUSAK* goes low, access to on-board RAM is available. At the same time, the latches U68 and U78 are in a high-impedance mode.

The dual port RAM logic consists of a state machine U62, U63, and U73. The state machine controls arbitration between the Multibus, CPU, and refresh cycles.

Dual port RAM control logic consists of digital comparator U85. Jumpers are available to determine the address an external processor uses to access the Am96/4116 RAM. The output of U85 drives a synchronizing flip-flop U81 to produce ZBUSRQ* to request the bus from the AmZ8002. The CPU will respond with ZBUSAK*.

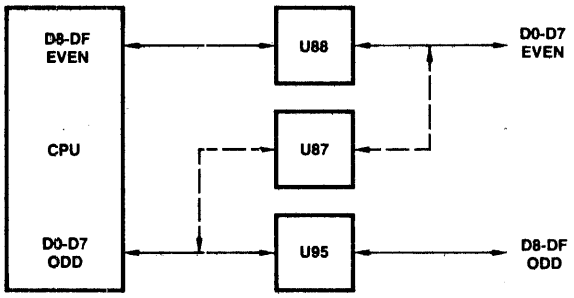
Bus transceivers U87, U88, and U95 provide data bus buffering between the AmZ8002 and the off-board devices and memory. Figure 4-2 illustrates word (16-bit) and (8-bit) byte operations.

NOTE

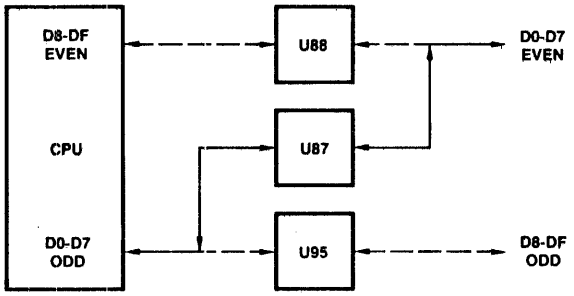
Even lines for the CPU are D8 to DF (bit 15), while even on the Multibus pins are D0 to D7.

Byte operations look only at data bits 0 to 7 (DAT0-DAT7) of the Multibus pins. Odd-byte operations enable U87 and Even-byte operations enable U88 (figure 4-2b and 4-2c). Word operations enable both U88 and U95 (figure 4-2a). If the CPU shares an area of memory with an external processor, only byte operations should be used. The AmZ8002 and the Multibus have odd and even bytes reversed.

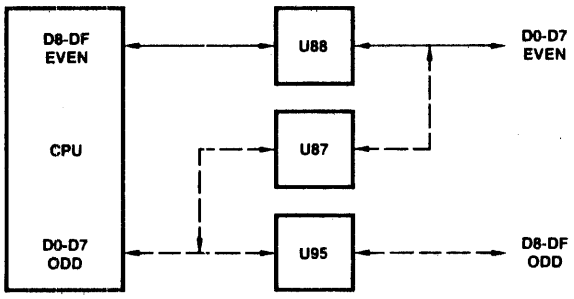
The I/O port decoding is performed by 3 to 8 line decoder U80. Address bits 3, 4, and 5 perform the I/O port selection. Bits 14 and 15 (E and F) determine the base address of C000 hex for the I/O area, which is C000 to FFFF. Status line decoding is performed by a fusible-link PROM U51.



A. Word Data Transfer



B. Odd-Byte Data Transfer



C. Even-Byte Data Transfer

Figure 4-2. CPU Memory Operations

RANDOM ACCESS MEMORY

The Am96/4116A has 32K bytes of dynamic RAM locatable in either upper or lower 32K byte of the 64K address space. The RAM consists of sixteen 16,384 x 1 dynamic devices with 200 nano-second access times. Addressing of the devices consists of 7 bits of row address and 7 bits of column address. Buffer U76 is enabled for the row address, and U66 is enabled for the column address. Accessing the RAMs requires first latching the row address, then the column address. The Am96/4116A RAM has all of the row address strobes (RAS*) in common. However, the column address strobes (CAS*) are separate for each device such that the low and high bytes can be enabled separately or for byte-writes together for word operations.

Since the RAM devices are dynamic, periodic refreshing is required. Normal read/write operation refreshes the devices. However, when the RAM is not being accessed by the CPU, another refresh scheme must be used. The method used on the Am96/4116A is a separate row address counter which cycles through the seven row addresses at a 77KHz rate or one address every 13μS. Dual binary counter U57 is the refresh address counter. During refresh cycles, the counter output drives row address 0 to 6 to refresh the RAM chips. An algorithmic state machine consisting of U62, U63, and U73 provides synchronization of refresh and memory availability with both a delayed CPU clock and the 77 KHz refresh clock.

ROM/EPROM

The on-board ROM consists of two devices of 1K, 2K, or 4K byte capacity each, for a maximum of 4K words or 8K bytes. One ROM, U91 is for odd-byte addresses (bits 0 to 7), and U75 is for even-byte addresses (bits 8 to F). Jumpers are provided for selection of ROM type. Both ROMs must be the same type. Jumpers at the inputs to U71 are required to select ROM size. The output of U71 is used to generate the EPROM CE* signal. Flip-flop U81 is used to enable or disable the shadow ROM feature. An I/O write to address FFF0 disables the shadow ROM. An I/O write to address FFF1 enables the shadow ROM address bit 0 (AB0) functions as the shadow ROM select line.

MEMORY EXPANSION

The memory expansion feature of the Am96/4116A uses the bit set/reset capability of the parallel I/O Port C bits. Connecting the required jumpers (see figure 3-2), and outputting the desired bits can select up to 512K bytes of external ROM or RAM. Buffer U92 is enabled only when the on-board RAM space is not addressed. If the on-board RAM is located at 8000 to FFFF hex, the off-board bank select address lines are only valid in the address range from 0000 to 7FFF hex. Using port C bit 0 to drive the ADF* (address bit F hex), permits addressing 32K-byte blocks. However, the 32K-byte blocks are contiguous. An extra programming step of setting the port C bits is required, but up to eight 64K RAM boards, for example, can be addressed.

SERIAL I/O INTERFACE

The Am96/4116A has two RS232C serial ports. Both channels can be programmed to operate with either synchronous or asynchronous protocols. Character length, number of stop bits, and even/odd parity are program selectable. The Serial I/O Interface consists primarily of two 9551 Programmable Communications Interface devices, part of an Am9513 System Timing Controller used as a baud rate generator, and driver/ receiver circuits. The following description will be on one Am9551. Any exceptions will be noted. Address bit 1 (AB1) is applied to the C/D input of the Am9551. An output instruction (serial 2 CE*, IO WRITE1*, and C/D high) causes the Am9551 to accept a control byte through its data bus pins. The control byte can be either a mode instruction or a command instruction, depending on the sequence in which it is sent. The mode instruction specifies the baud rate multiplier, character length, parity, and the number of stop bits. The actual baud rate selection is determined by the baud rate input from the Am9513. The command word instructs the Am9551 to enable/disable the receiver and transmitter, to reset errors, to return to Idle mode, and to set/clear the Data Terminal Ready Signal output. An output instruction also causes the Am9551 to accept a data byte through its data bus pins. Bit 0 is the least significant bit and bit 7 is the most significant bit. The Am9551 will subsequently transmit serial data to an external device if the transmitter is enabled.

An input instruction (Serial 2 CE*, IO READ*, and C/D high) causes the Am9551 to place a status byte on the data bus. The status bits are the result of status and error checking functions performed within the Am9551. An input instruction also causes the Am9551 to output a data byte onto the data bus. Bit 0 is the least significant bit and bit 7 is the most significant bit.

Timing for the Am9551 internal functions is provided by a 2.4576 MHz output from counter U40, which is derived from a 19.6608 MHz oscillator. The Am9513 also uses the 2.4576 MHz signal. Jumpers at the Am9513 determine the baud rate source. The baud rate can be jumpered for 9600 baud, which is from the Am9513 FOUT pin or for programmable baud rates from counters 3 and 4 in the Am9513. The clock source for Serial Port 1 can also be from external sources. The clock source for Serial Port 2 is the on-board source only.

A high on the Am9551 RESET line forces the device into an idle mode. After a high RESET input, the Am9551 remains idle until a new set of control words are written into the Am9551 to define its function.

In addition to the above control lines, the Am9551 also has a set of control inputs and outputs that can be used to simplify the interface to almost any serial data device. These control signals are general purpose in nature. The following paragraphs describe the interface controls.

Receiver Data (RxD) Serial data is received from the communication line of the RxD input.

Receiver Clock (RxC) The serial data on input RxD is clocked into the Am9551 by the RxC clock signal. In the synchronous mode, RxC is determined by the baud rate and suplied by the modem. In the asynchronous mode, RxC is 1, 16, or 64 times the baud rate selected by the mode control instruction. Data is sampled by the Am9551 on the rising edge of RxC.

Receiver Ready (RxRDY) The RxRDY output signal indicates to the processor that data has been shifted from the receiver section into the receiver buffer and can be read. The active high RxRDY signal is reset when the buffer is read by the processor. RxRDY can be activated only if the receiver enable (RxE) has been set in the command register, even though the receiver might be running. If the processor does not read the receiver buffer the next character is shifted from the receiver section, an overrun error is indicated in the status buffer.

Sync Detect (SYNDET) This signal is used only in the synchronous mode. It can be either an output or input depending on whether the program is set for internal or external synchronization. As an output, a high level indicates when the sync character has been detected in the received data stream after the internal synchronization mode has been programmed. If the Am9551 is programmed to utilize two sync characters, SYNDET will go to a high level when the last bit of the second sync character is received. SYNDET is reset when the status buffer is read or when a reset signal is activated. SYNDET will perform as an input when the external synchronization mode is programmed. External logic can supply a positive-going signal to indicate to the Am9551 that synchronization has been achieved. This will cause it to initiate the assembly of characters on the next falling edge of RxC. To successfully achieve synchronization, the SYNDET signal should be maintained in a high condition for at least one full RxC period.

Transmit Data (TxD) Serial data is transmitted to the communication line on the TxD output.

Transmitter Clock (TxC) The serial data on TxD is clocked out with the TxC* signal. The relationship between clock rate and baud rate is similar to that for RxC*. Data is shifted out of the Am9551 on the falling edge of TxC*.

Transmitter Ready (TxRDY) The TxRDY output signal goes high when data in the transmit data buffer has been shifted into the transmitter section allowing the transmit data buffer to accept the next byte from the processor. TxRDY is reset when information is written into the transmit data buffer. Loading the command register also resets TxRDY. TxRDY is available only when the Am9551 is enabled to transmit (CTS* = 0, TxEN = 1). However, the TxRDY bit in the status buffer will always be set when the transmit data buffer is empty regardless of the state of TxEN and CTS*.

Transmitter Empty (TxE) The TxE output signal goes high when the transmitter section has transmitted its data and is empty. The signal remains high until a new data byte is shifted from the transmit data

buffer to the transmitter section. In the synchronous mode, when the processor does not load a new byte into the buffer in time, TxE will momentarily go to high level as SYNC characters are loaded into the transmitter section. TxE going high is independent of the status of the TxEN bit in the command register.

Data Terminal Ready (DTR*) This signal is a general purpose output which reflects the state of bit 1 in the command instruction. It is commonly connected to an associated modem to indicate that the Am9551 is ready.

Data Set Ready (DSR*) This is a general purpose input signal and forms part of the status byte that can be read by the processor. The DSR* signal is generally generated by the modem as a response to the DTR* signal; it indicates that the modem is ready. The signal acts only as a flag and does not control any internal logic.

Request to Send (RTS*) This is a general purpose output, similar to DTR*; it reflects the state of bit 5 in a command instruction. RTS* is normally used to initiate a data transmission by requesting the modem to prepare to send.

Clear to Send (CTS*) This is a general purpose input signal used to enable the Am9551 to transmit data if the TxEN bit in the command byte is a one. CTS* is generally used as a response to RTS* by a modem to indicate that transmission can begin. Designers not using CTS* in their systems should remember to tie it low so that Am9551 data transmission will not be disabled.

PARALLEL I/O INTERFACE

The Parallel I/O Interface on the Am96/4116A provides 24 lines for the transfer and control of data to and from peripheral devices using one Am8255A Programmable Peripheral Interface.

The Am8255A is organized as three 8-bit ports (A, B, and C). Two of the ports A and B have Am8304 bus transceivers installed, providing 16 bidirectional I/O lines. As shipped from AMC, port A is configured as an output port, and port B is configured as an input port. Port C is organized as two four-bit I/O ports, with sockets provided for either line drivers or terminations (see figure 2-2 and table 2-8). The Am96/4116A has the capability of using port C bits 0 to 3 for block selection of external memory.

Communication between the CPU and the Am8255A is via the data bus and six control lines. Control and data bytes are transmitted to a Am8255A; status and data bytes are transmitted from a 8255A on the data bus 0 to 7. The six control lines provide the necessary control for all Am8255A data bus operations. The following is a description of the control lines:

CS* PARALLEL CE* is used to enable the Am8255A during parallel I/O operations.

RESET RESET is used during POWER ON cycle and at any time the system is initialized.

RD* IO READ* is used when either parallel data or status bytes are read by the CPU.

WR* IO WRITE* is used when either data or control bytes are written by the CPU.

A0,A1 AB1 and AB2 allow selection by the CPU, of a specific port or control word register.

A1	A0	SELECTION
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Control Register

All internal registers are cleared and the ports are set to the high impedance input mode when a high level is presented to the Reset input.

INTERRUPT CONTROLLER

The interrupt controller logic consists of an 8259A Interrupt Controller and a jumper pad that allows the user to connect any of 32 possible interrupt requests to the 8259A eight interrupt priority inputs.

The Interrupt Controller resolves priorities among the eight levels. The priority resolution algorithm can be changed dynamically at any time. This means that the complete interrupt structure can be modified as required.

The operation of the Interrupt Controller is controlled via five control lines and the data bus. The five control lines are decoded to provide controls for programming and reading status. Control words and status information are transferred through the data bus. The functions of the control lines are as follows:

CS* RUPT CE* enables the 8259A control and status operations.

C/D AB1 is address bit 1. Provides access to control register when high and data when low.

RD* IO READ* permits reading of status information by the CPU.

WR* IO WRITE* permits the CPU to write control data to 8259A control register.

IACK* Is supplied by the CPU and other logic elements. Transfers one byte for each of two IACK* pulses. Only the second byte is used to provide an 8-bit interrupt vector.

The INT output from the 8259A goes to the AmZ8002 VI* input via inverter U58.

SYSTEM TIMING CONTROLLER

The Am9513 System Timing Controller provides five 16-bit general purpose counters, each with a load register and a hold register. Counters 1 and 2 each have a 16-bit comparator and an alarm register and can function in a 24-hour clock mode. In addition, the Am9513 contains a 16-bit counter/frequency scaler and a 4-bit counter/FOUT divider. All counters except the FOUT divider can operate either in a binary or BCD mode. Each of the five 16-bit counters has an output pin, gate pin, and a source pin associated with it.

Control of the Am9513 is by means of four control lines. Data and control programming between the Am9513 and CPU is over a 16-bit data bus. The following is a description of the four control lines:

CS* TIMER CE* enables the Am9513 whenever timer/CPU operations take place.

C/D AB1 is address bit 1. When AB1 is high, the control and status registers are available to the CPU. When AB1 is low, data registers are accessible to the CPU.

RD* IO READ* permits reading of status registers or data from the Am9513, depending on the state of AB1.

WR* IO WRITE* permits writing of control words or data to the Am9513, depending on the state of AB1.

The FOUT pin of the Am9513 is used to provide the baud rate clock for the two Am9551 serial I/O devices. The clock source for the Am9513 is a 2.4576 MHz signal derived from a 19.6608 MHz oscillator. The 2.4576 MHz signal is divided by 16 whenever the Am9513 is reset or power is applied, and available at FOUT. The 2.4576 MHz signal divided by 16 to produce 16 x 9600 baud. Also, counters 3 and 4 can be used to provide programmable baud rates by connecting the proper jumpers and programming the appropriate load register. Programming information is available in chapter 3. All of the inputs, outputs, and gate inputs for the five general purpose counters are available at connector P2. Jumpers 188 and 189 are available when the 24 hour clock function is desired.

CHAPTER 5
SERVICE INFORMATION

INTRODUCTION

This chapter provides information on service and repair assistance, user replaceable parts and service diagrams for the Am96/4116A AmZ8000 16-Bit MonoBoard Computer.

SERVICE AND REPAIR ASSISTANCE

Service and repair assistance can be obtained from Advanced Micro Computers by contacting the AMC Field Service Department in Santa Clara, California at one of the following numbers:

Telephone: (408) 988-7777

Toll Free: (800) 672-3548 California

(800) 538-9791 U.S.A. (except California)

If it is necessary to return a product to Advanced Micro Computers for service or repair, contact the Field Service Department at the previously listed telephone number. A Return Material Authorization number will be provided along with shipping instructions and other important information that will help AMC provide you with fast, efficient service. When reshipment is due to the product being damaged during shipment from AMC, or when the product is out of warranty, a purchase order is required for the AMC Field Service Department to initiate the repair.

Prepare the product for shipment by repackaging it in the original factory packaging material, if available. When the original packaging is not available, wrap the product in a cushioning material (such as Air Cap TH-240, manufactured by the Sealed Air Corporation, Hawthorne, New Jersey) and enclose in a heavy-duty corrugated shipping carton. Seal the shipping carton securely, mark it FRAGILE, and ship it to the address specified by the AMC Field Service Department.

Customers outside of the United States can contact an AMC Sales Office or Authorized AMC Distributor for directions on obtaining service or repair assistance.

SERVICE DIAGRAMS

Figure 5-1 is a component location diagram. Schematic diagrams for the Am96/4116A are provided in figures 5-2 through 5-13.

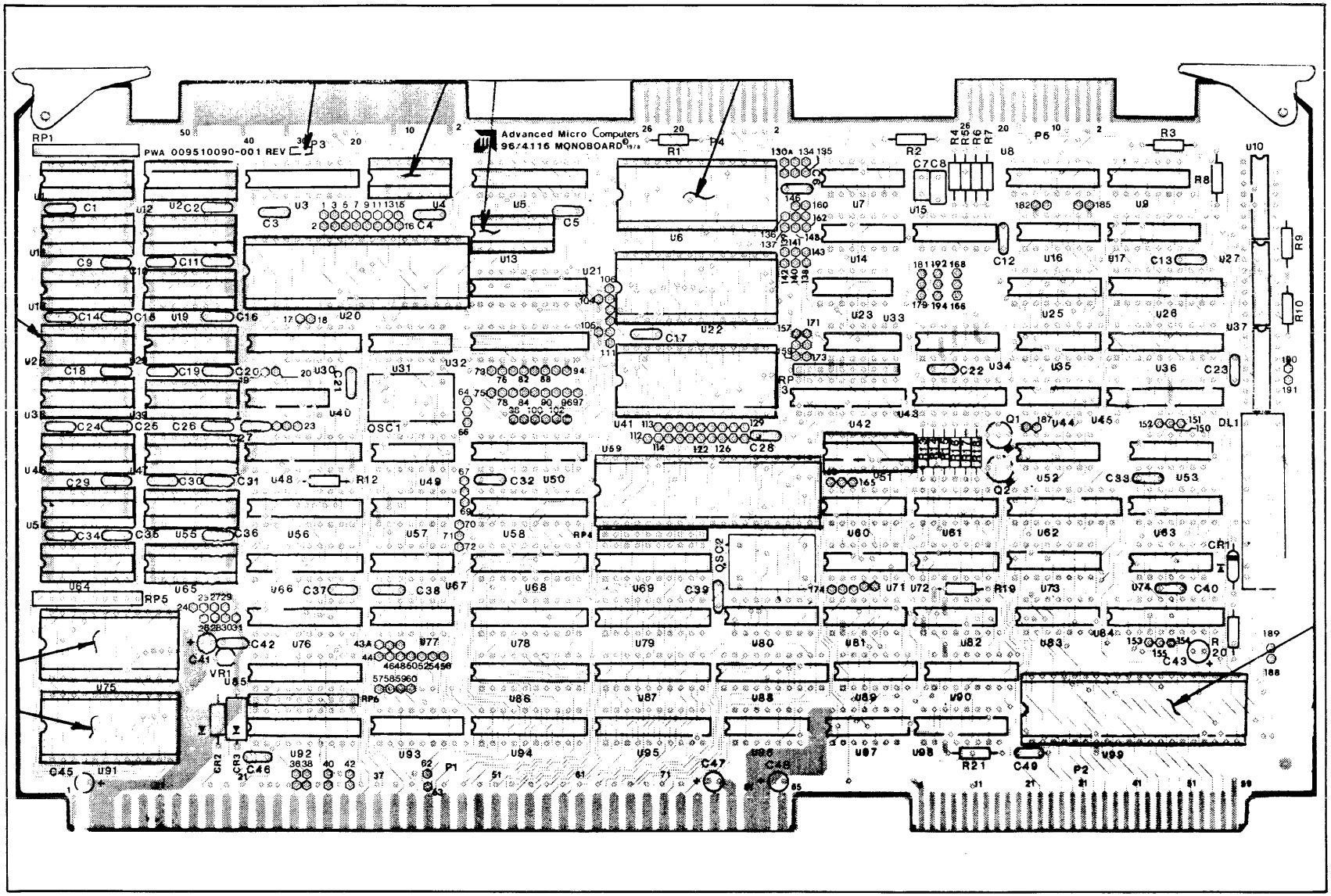


Figure 5-1. Am96/4116A MonoBoard Computer, Component Locations

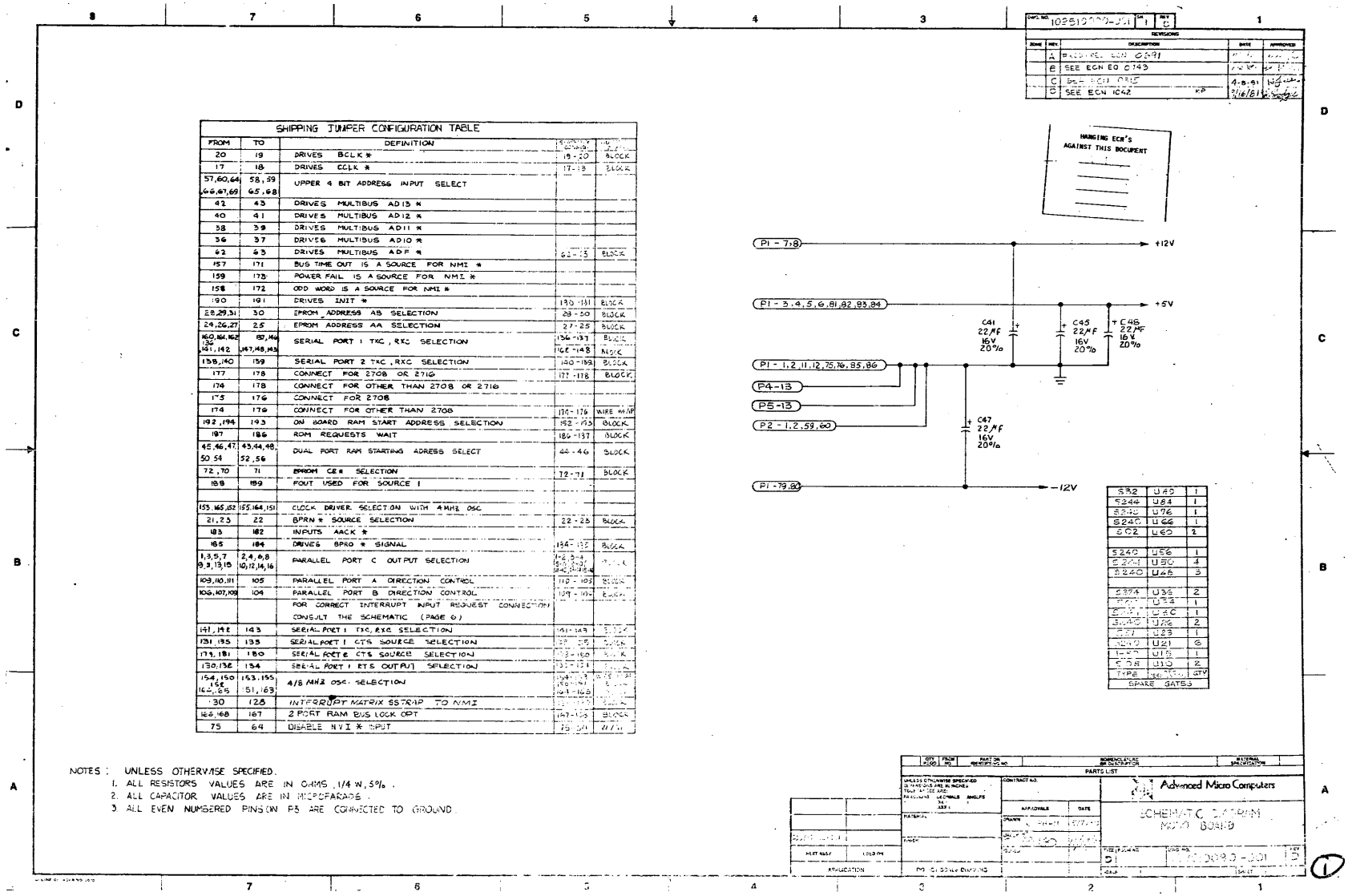


Figure 5-2. Am96/4116A MonoBoard Computer, Schematic Diagram

CPU

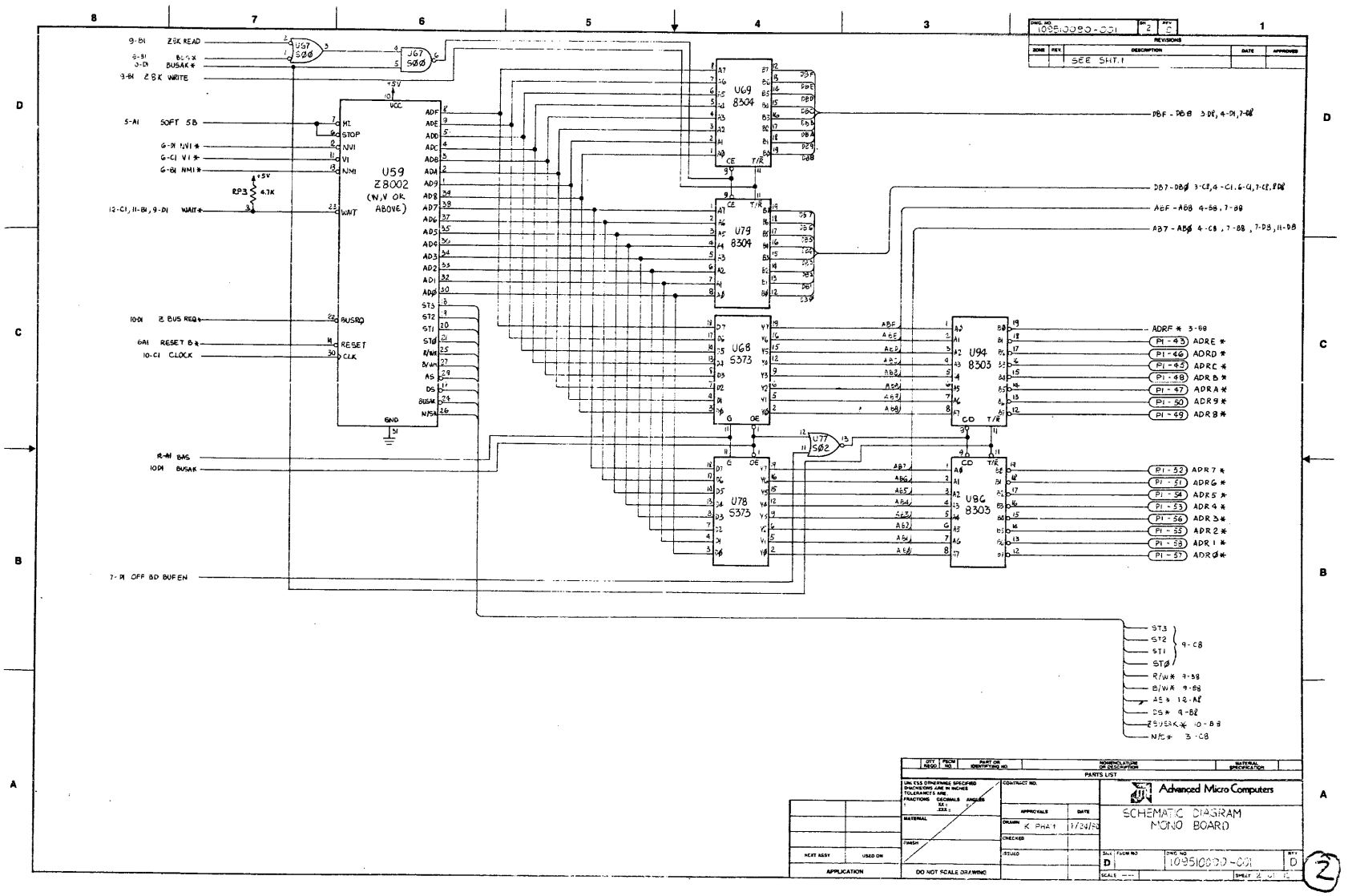


Figure 5-3. Am96/4116A MonoBoard Computer, Schematic Diagram

timing & OFF board Memory

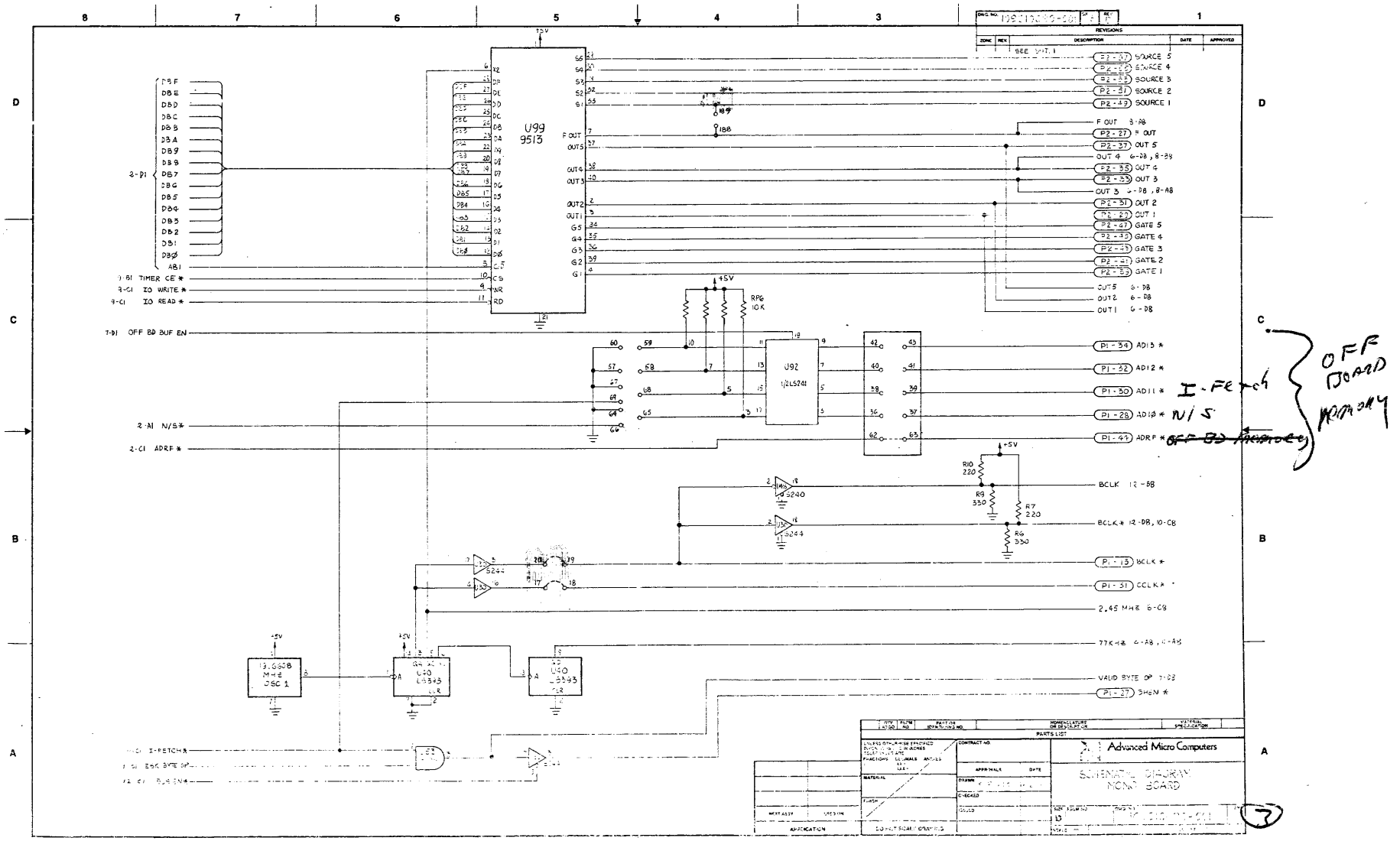


Figure 5-4. Am96/4116A MonoBoard Computer, Schematic Diagram

Ram

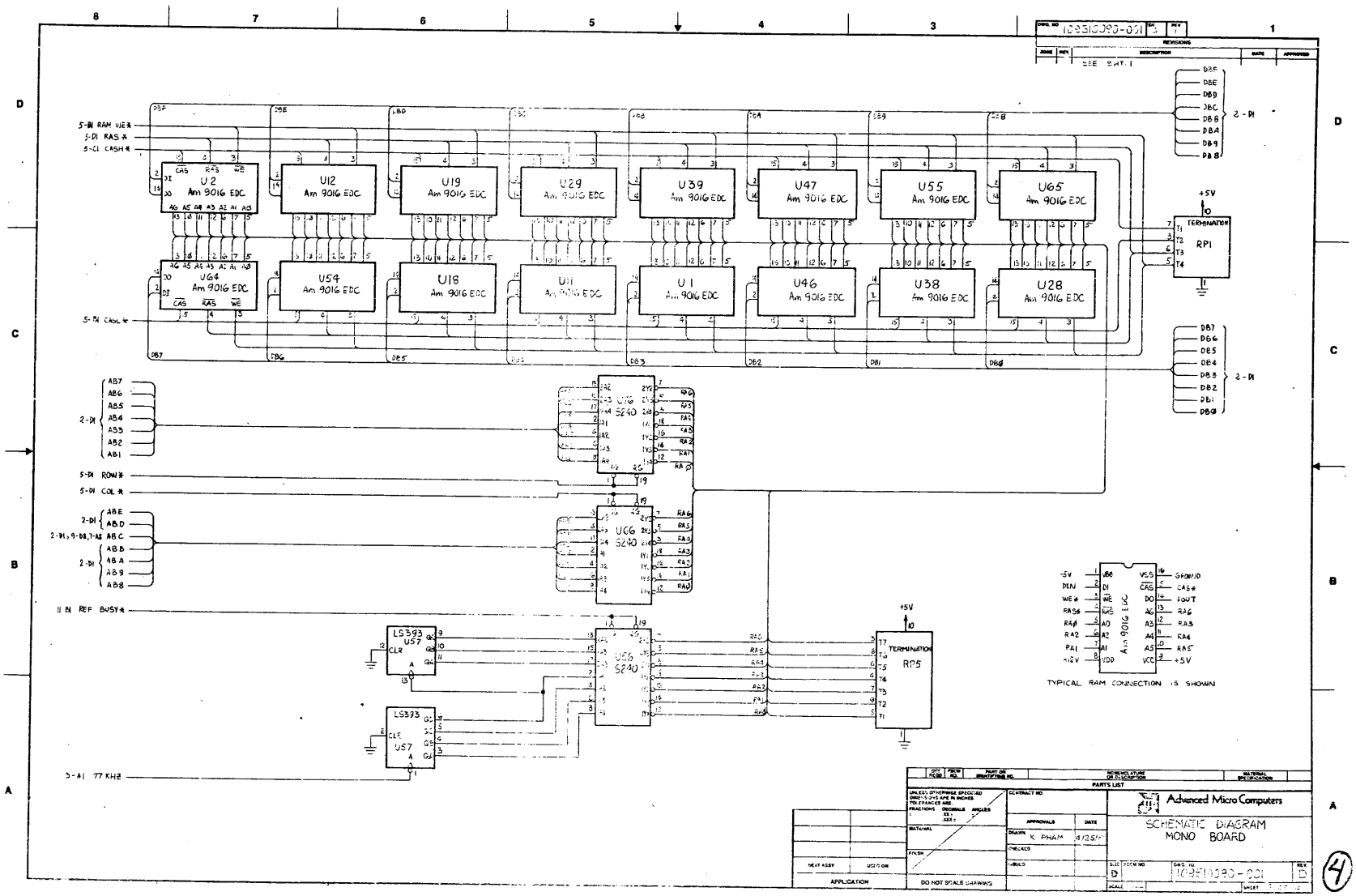


Figure 5-5. Am96/4116A MonoBoard Computer, Schematic Diagram

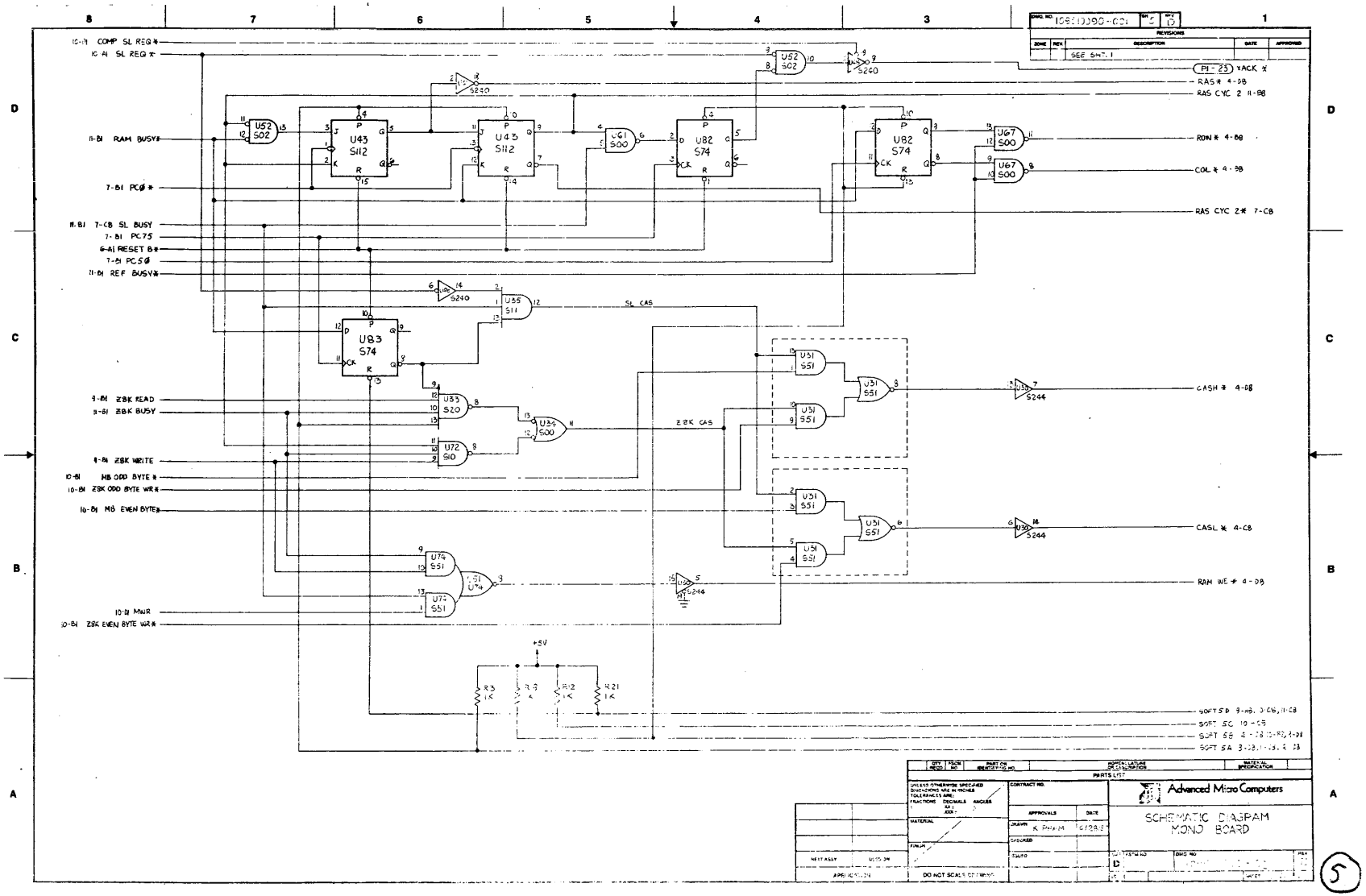


Figure 5-6. Am96/4116A MonoBoard Computer, Schematic Diagram

Interrupt Controller

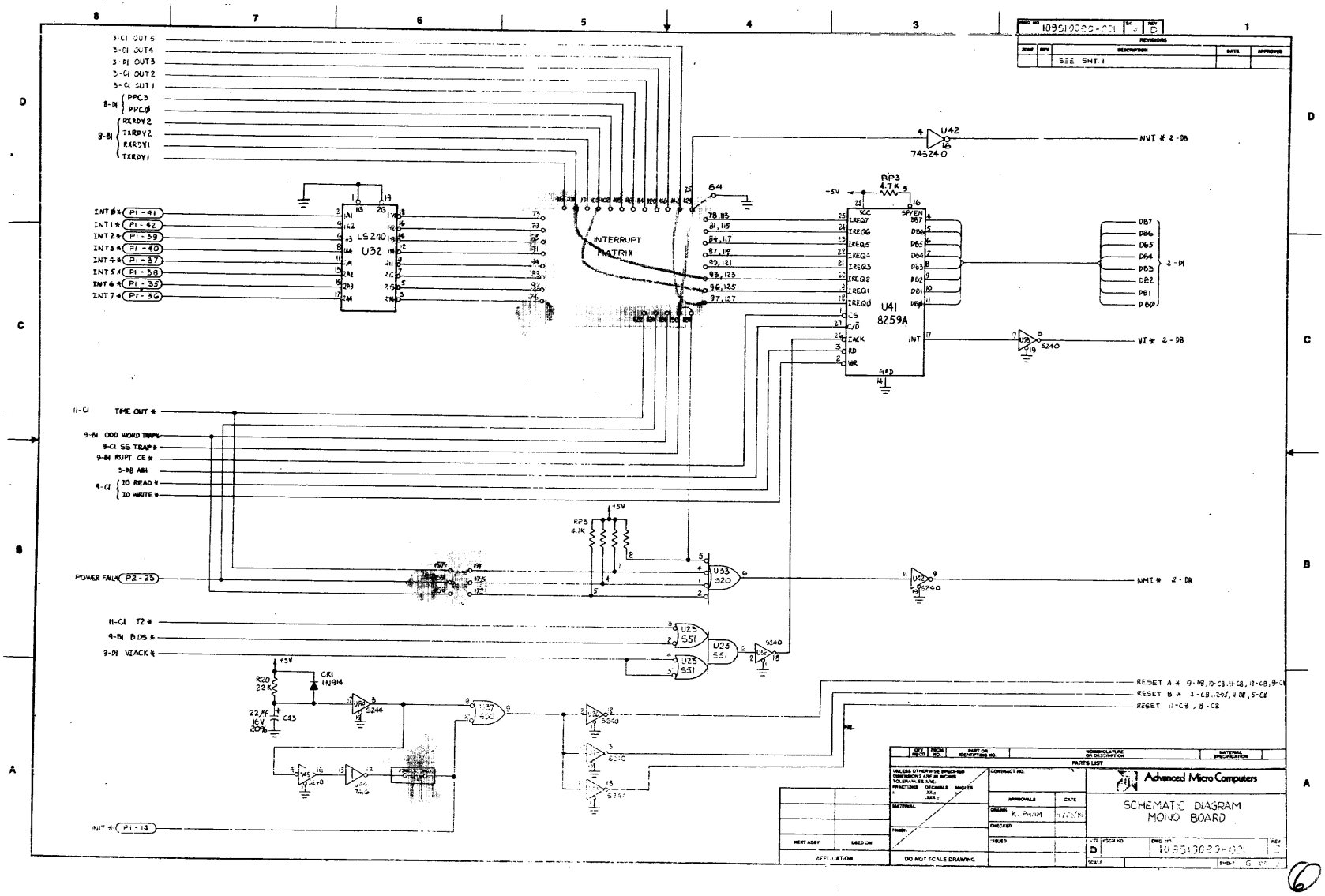


Figure 5-7. Am96/4116A MonoBoard Computer, Schematic Diagram

Monitor

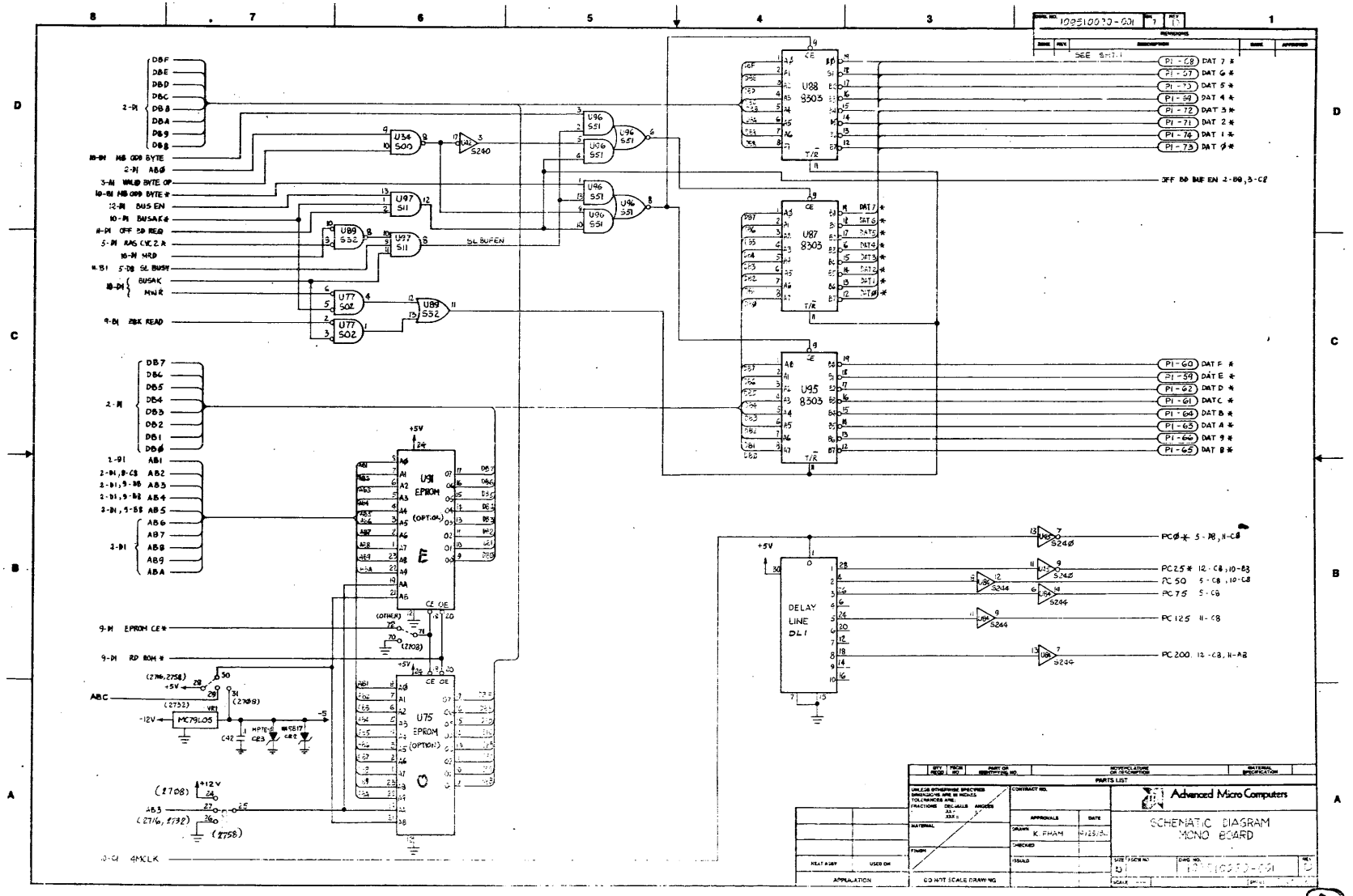


Figure 5-8. Am96/4116A MonoBoard Computer, Schematic Diagram

I/O PORTS

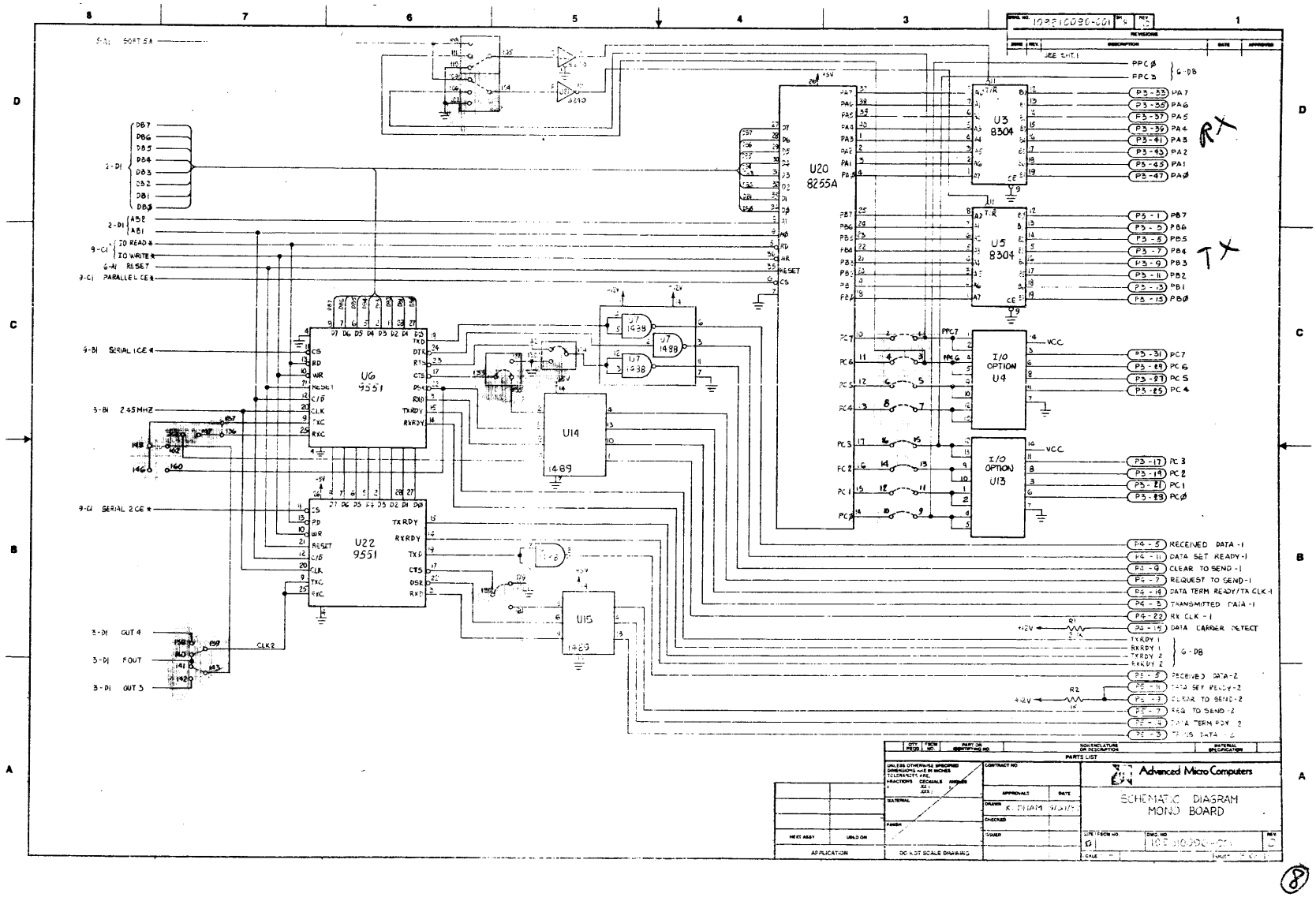


Figure 5-9. Am96/4116A MonoBoard Computer, Schematic Diagram

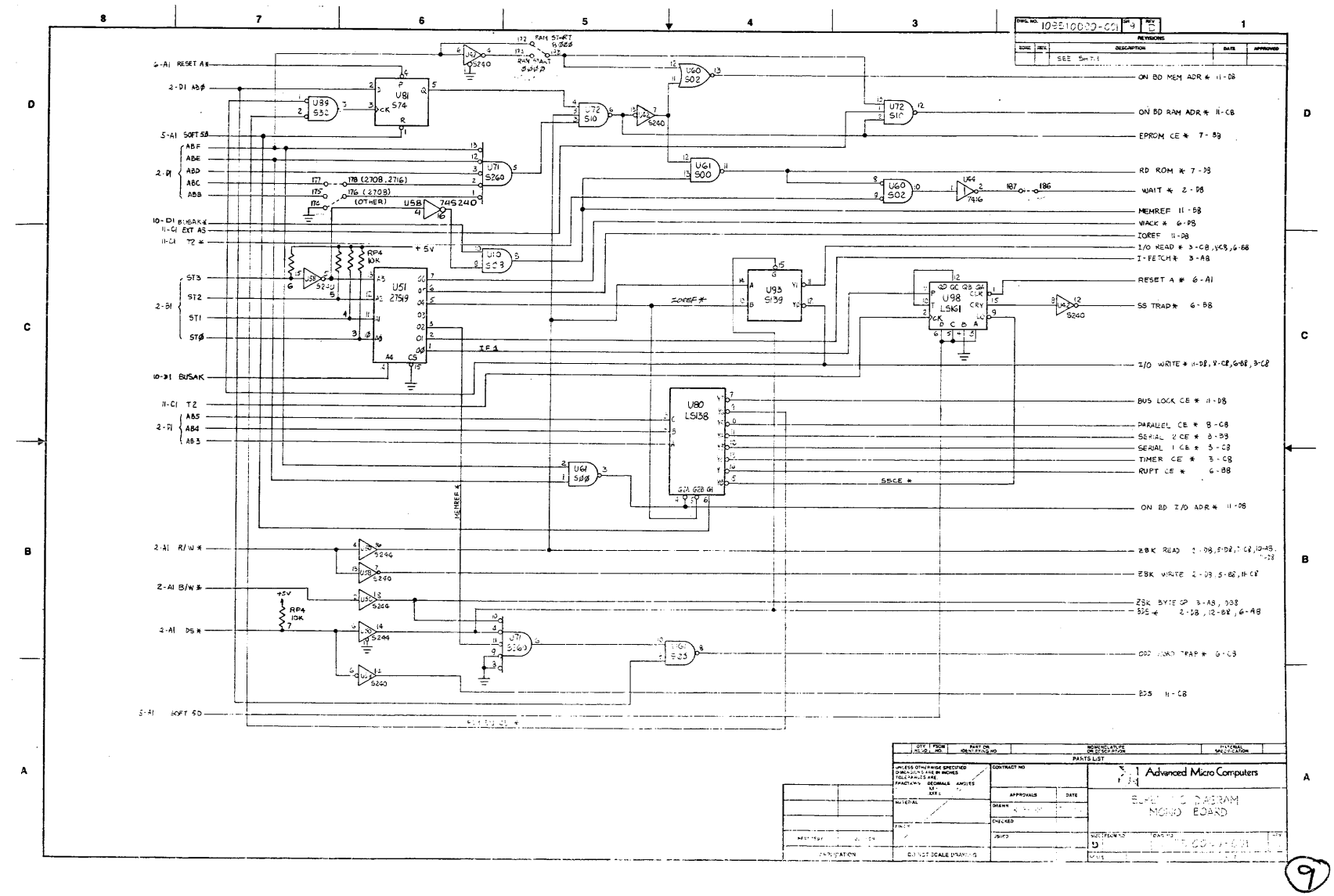


Figure 5-10. Am96/4116A MonoBoard Computer, Schematic Diagram

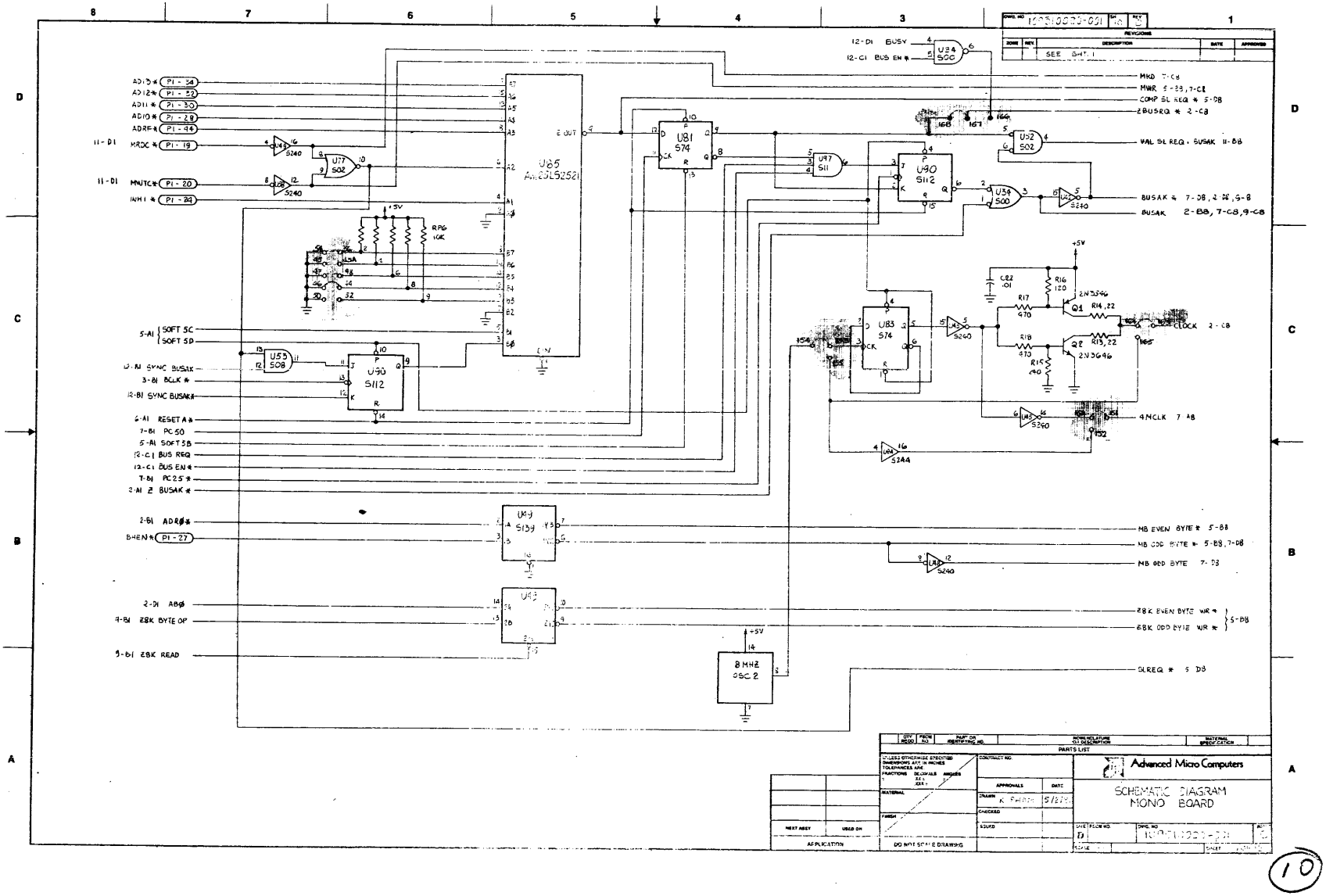


Figure 5-11. Am96/4116A MonoBoard Computer, Schematic Diagram

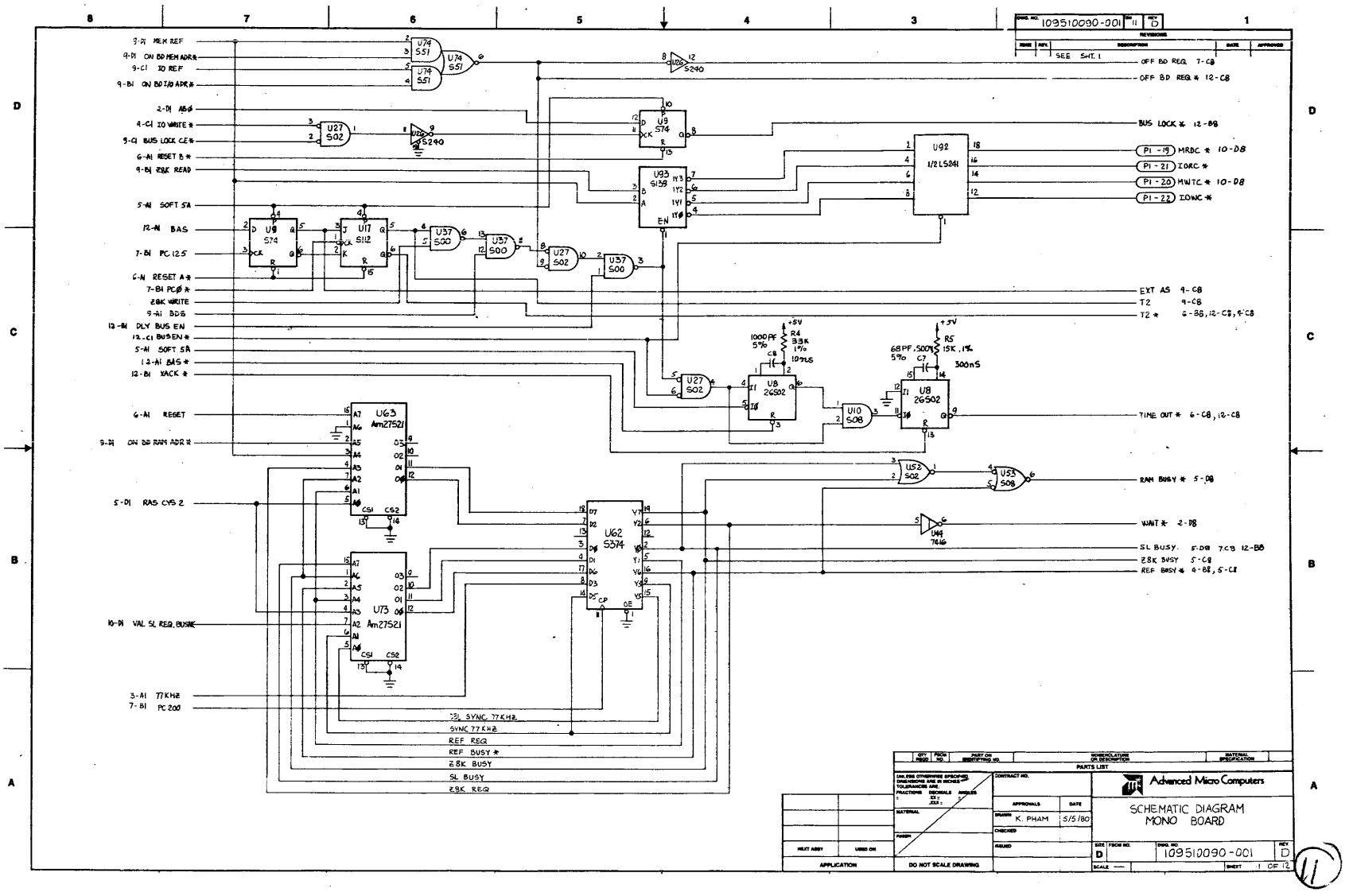


Figure 5-12. Am96/4116A MonoBoard Computer, Schematic Diagram

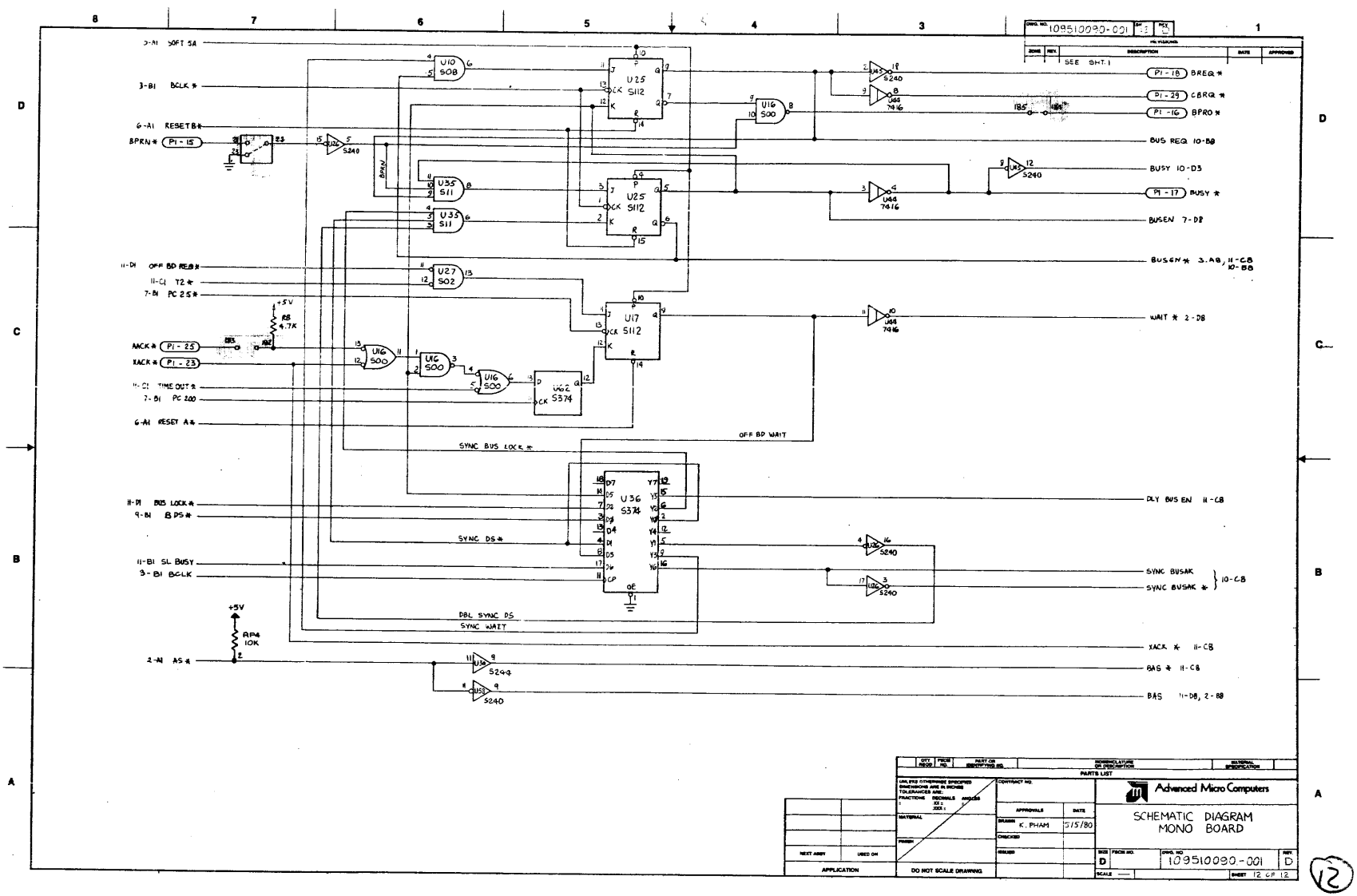


Figure 5-13. Am96/4116A MonoBoard Computer, Schematic Diagram

COMMENT SHEET

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