D A T A S H E E T

Document Revision 5
December 1995

AIC-8375B

Fast IDE Disk Controller IC

adaptec®

AIC-8375 Features

ATA Interface Block

- ATA Multiword DMA modes 0-2
- Fast IDE PIO modes 0-4
- IORDY for PIO flow control
- Automatic AT R/W command execution
- Automatic AT Task File updates
- 32-byte host FIFO
- LBA or CHS TASK File Modes
- Programmable IRQ automation to comply with different BIOS implementations
- Provides logic for daisy chaining two embedded disk drive controllers
- Hardware selectable PCMCIA 2.0
- Full BIOS compatibility
- On-Chip12 mA Host Drivers
- PCMCIA Attribute Memory stored in buffer memory

Buffer Controller Block

- 8 bit wide or 16 bit wide buffer data bus with parity
- DRAM support with up to 4 Mbyte addressing capability; up to 36 Mbyte/s (18 Mbyte/s PCMCIA) buffer bandwidth using page mode DRAM access
- SRAM support for up to 256 Kbyte direct addressing; up to 50 Mbyte/s (25 Mbyte/s PCMCIA) buffer bandwidth
- Automated Data Flow Management (ADFM) automates disk/host transfers.
- 2K page direct microprocessor access
- Variable Segmentation
- Write Cache Support
- Servo Split count out of buffer

Other Features

- 128-pin QFP and TQFP packages
- Automatic power-down modes
- High-speed, low-power CMOS

EDAC Block

- Optimized 168 bit ECC with Triple Burst on-the-fly (OTF) correction
- 65 bit single burst OTF correction in <1 sector time or 17 bit Double or Triple Burst OTF correction in <1 sector time
- SW correction up to three 17-bit bursts
- Error detection of one 89-bit error, two 41-bit errors, or three 17-bit errors
- ECC seeding validating servo and head track position
- Fault tolerant sync mark detection with 2 byte sync

Disk Controller Block

- Enhanced Headerless Architecture (EDSA)
- 50 Mbits/sec, 100 Mbits/sec and 120 Mbits/sec disk rate in single, dual, and byte-wide NRZ modes respectively
- 31 x 3 byte flexible high-speed RAM-based sequencer
- Defect skipping and/or embedded servo capabilities with Constant Density Recording (CDR)
- 32-byte disk FIFO for speed matching with the buffer manager
- Two-index timer
- Supports (1,7) and (2,7) RLL interfaces
- MR and PRML channel support

Microcontroller Interface Block

- Direct support for Intel or Motorola multiplexed or non-multiplexed interfaces
- Ready line for interfacing to faster microprocessors and for direct microprocessor access to the Buffer
- Programmable open drain interrupt output for host, disk, and buffer
- Address latch outputs for multiplexed microprocessor interface
- Direct buffer addressing in programmable 2K windows with 1K resolution on base address

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REVISION NOTES
for AIC-8375B Data Sheet (PN 700191-011 Rev 5) - December 1995

In this document, **all** changes to **technical information** incorporated by document ***Rev 4*** (interim release) and ***Rev 5*** are indicated by a change bar in the left-hand margin. The sections and pages affected are listed in the table below. Included are all final AC characterization timing data for the rev B chip. (Superficial or non-technical edits are not indicated.)

Changes incoporated by ***Rev 5*** only are noted with ***bold section and page numbers*** in the table below.

Changes incorporated into document *Rev 4* and *Rev 5*:

Section Updated	Pages Affected	Change Description
Overall	---	Miscellaneous changes/corrections, and all AC characterization timing data have been incorporated as indicated.
3.3	**28**	Reg. 9Fh (ECC Indirect Data (moto)) has been deleted. Register 9Eh is always used for ECC Indirect Data regardless of Swapmode bit for Motorola mode.
4.3	**41**	Reg. 9Fh has been deleted. See description for page 28 above.
5.2	55	Correction made to register 60h (Disk Control 0 Reg.) bit 5 (ENNRZFALL).
	66	Changes made to register 7Bh (Disk Modulo 64 Counter).
7.3	**152 &153**	DC char data: Changes made to Sleep Mode and Power-Down mode data.
8.2	156 &157	AC char timing data: Changes made to microprocessor timing parameter data.
8.3	164 & 166	AC char timing data: Changes made to buffer timing parameter data.
8.4	181	AC char timing data: Changes made to disk timing parameter data.
8.4	182	Changes made to notes 6 and 7 clarifying Disk Write timing parameter data.
8.5	183	Changes made to clarify Disk Write timing diagrams, Figures 8-29 and 8-30.
8.5	188	AC char timing data: Changes made to AT host timing parameter data.
9 new	197 - 200	New package dimensioning information corrections and additions.
Addendum	201 - 204	There are new buffer, disk, ECC, and microprocessor operational characteristics described in the Addendum.

SECTION 1
Introduction

1.1 Introduction

The Adaptec AIC-8375 is an automated single-chip disk controller designed for high performance, headerless ATA and PCMCIA drive applications. The AIC-8375 is a feature enhancement of the AIC-8371 which includes EDSA Headerless support, a fixed 168 bit ECC that supports triple burst on-the-fly hardware correction, PCMCIA interface support, and a 2K direct address range for the microprocessor. The AIC-8375 is pin compatible with the AIC-8371 in ATA mode.

The AIC-8375 is capable of executing full track read/write operations, at a maximum disk rate of up to 50 Mbits/sec in single NRZ mode, 100 Mbits/sec in dual NRZ mode, and 120 Mbits/sec in byte wide NRZ mode, with complete automation including full automation of the various sub functions such as error detection and correction, buffer data flow management, embedded servo or defect algorithms, and AT or PCMCIA interface management. The various functional blocks within the device work together automatically to ensure proper data flow management and data integrity. This automation provides the local microprocessor with more bandwidth to apply to other tasks such as servo control functions and cache management. Alternately, the improved bandwidth may be applied towards the use of a lower performance microprocessor to further increase the performance/price ratio.

Designed using high speed CMOS technology, the AIC-8375 provides a hierarchy of power down and automatic wake up modes for power sensitive applications.

1.2 General Description and Features

The AIC-8375 works in conjunction with a local microprocessor to perform the AT or PCMCIA interface control, buffer data flow management, disk format/read/write control, and error correction functions of an embedded disk drive controller. The microprocessor communicates with the AIC-8375 by reading from and writing to its various internal registers.

To the microprocessor, the registers of the AIC-8375 appear as unique memory or I/O locations that are randomly accessed and operated upon. By reading from and writing to the registers, the local microprocessor initiates operations and examines the status of the different functional blocks. Once an operation is started, successful completion or an error condition may cause the AIC-8375 to interrupt the local microprocessor, which then examines the status registers of the AIC-8375 and determines an appropriate course of action. The local microprocessor may also poll the device to ascertain successful completion or error conditions.

Figure 1-1 reveals the various blocks within the AIC-8375 along with their generalized interconnection. The blocks described in this figure will be referred to throughout this document.

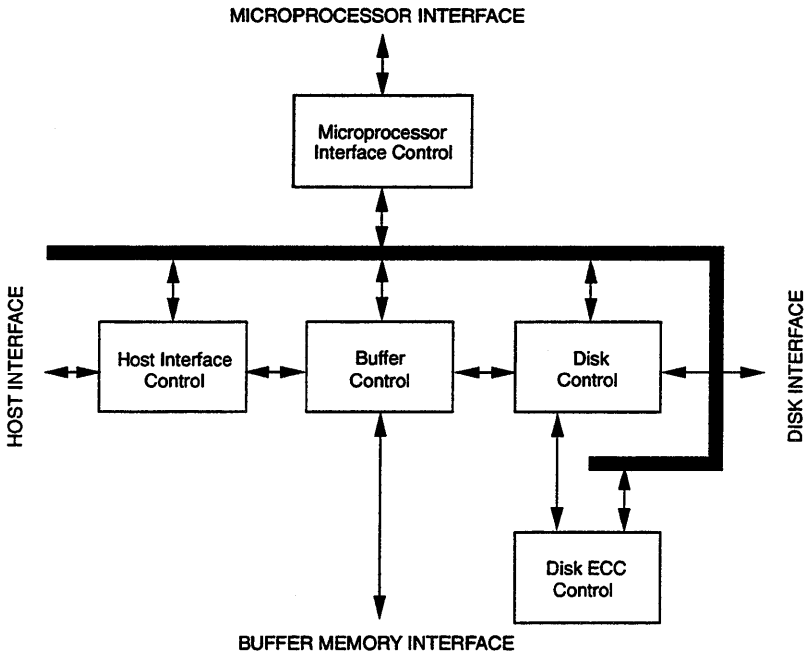

Figure 1-1 AIC-8375 Block Diagram

1.2.1 The Local Microprocessor Interface Block

It is through the Local Microprocessor Interface Block that the local microprocessor communicates to the other control blocks within the device or to the buffer. The AIC-8375 supports Intel and Motorola type 8-bit multiplexed and non-multiplexed address/data busses. The AIC-8375 requires two chip selects, one for the internal register space and the other for directly addressing the buffer memory. Each chip select covers a 2K addressing range. The microprocessor interface block also supports a READY/DSACK line for interfacing to very fast microprocessors.

1.2.2 The Host Interface Block

The AIC-8375 provides both an ATA and a PCMCIA interface to the host computer. Both provide a means for the host to access the Task File Registers used to control the transfer of data between host memory and the disk. The PCMCIA communication modes available are:

1. Primary/Secondary I/O Addressing Mode: This mode is compatible with existing IDE drives and ATA BIOSes. The primary addresses are 1F0h-1F7h and 3F6h-3F7h.

2. Block I/O Mode: This mode allows the host to locate the Task File Registers on a 16-Byte boundary in the host's I/O memory space. This allows multiple cards to coexist without I/O conflicts.

3. Attribute Memory: This is read by the host to determine information about the PCMCIA card and to change the card's configuration. It is not available in ATA mode. The Attribute Memory can be read by the host at any time the AIC-8375 is not in a busy state.

   The AIC-8375 Attribute Memory consists of two parts:

   Card Information Structure: This data structure contains readable tuple configuration data. This is a user-defined interface that supports up to 256 Bytes of information. The CIS is not writable by the host.

   Configuration Registers: These registers return information about the current configuration. The host can write to these registers to change the current configuration (e.g., change from Memory to a Block I/O Addressing Mode).

4. Memory Mode: The Task File Registers are mapped into memory along with a 1KByte block of memory for data transfers. The PCMCIA specification refers to this memory as Common Memory.

The Host Interface Block can be programmed to execute various host read/write commands either completely automatically without any microprocessor intervention, semi-automatically with minimal microprocessor intervention, or manually with the aid of the microprocessor.

1.2.3 The Buffer Control Block

The Buffer Control block manages the flow of data into and out of the buffer. Significant automation is incorporated which allows buffer activity to take place automatically during read/write operations between the host and the disk. This automation works together with automation within the Host Control and Disk Control blocks to provide more bandwidth for the local microprocessor to perform non-data flow functions.

The buffer control circuitry keeps track of buffer full and empty conditions and automatically works with the Disk Control block to stop transfers to or from the disk when necessary. In addition, transfers to or from the host are automatically stopped or started based on buffer full or empty status.

1.2.4 The Disk Control Block

The AIC-8375 Disk Control block manages the flow of data between the disk and the buffer. It is capable of performing completely automated track read and write operations at a maximum data rate of 50 Mbits/sec in single NRZ mode, 100 Mbits/sec in dual NRZ mode, or 120 Mbits/sec in byte-wide NRZ mode. Many flexible features and elements of automation have been incorporated to complement the automation contributed by the Host and Buffer blocks.

The Disk Control block consists of the programmable 31 by 3 byte sequencer, CDR/data split logic, disk FIFO, fault tolerant sync detect logic, and other support logic.

1.2.5 The Disk ECC Block

The AIC-8375 supports a fixed 168 bit 3-way interleaved Reed-Solomon ECC. The code is capable of correcting up to three 17-bit bursts or one 65-bit burst in hardware. The Disk ECC block also supports up to 48 bits of seed data to the ECC generator to allow for greater data integrity in a headerless environment. The ECC will also detect up to three 17-bit bursts or one 89-bit burst errors. Software provides correction with burst limiting.

1.2.6 Power Management

Power management features are incorporated into each block of the AIC-8375. This allows the designer to tailor the amount of power management to the specific design as required. Other power management features include:

- Independent power management control for each block.
- ECC logic automatically powered down when not in use and powered up when needed.
- Disk sequencer and associated disk logic powered up when the sequencer is started.
- Weak pull-up structure on input pins to prevent undesirable power consumption due to floating CMOS inputs.

1.2.7 Headerless Architecture

The AIC-8375 supports an Enhanced Data Sector headerless architecture. This is an enhancement of the headerless architecture currently in production with the AIC-8371.

This architecture is based on the sequencer flushing then loading the CDR FIFO every data sector pulse. The chip does not require the servo microprocessor to suppress sector pulses. The microprocessor determines alignment with the media using EOS counts. Once on track and using the EOS count the microprocessor can set the servo CDR pointer to the CDR word for the sector following the EOS pulse. The microprocessor also invalidates the first CDR word of every sector that the microprocessor would like to skip (i.e. defective sectors, spare sectors and unrequested sectors). This architecture can support ZLR. The microprocessor loads the Sector Address register with the data sector number of the first sector to be read. The sequencer increments the sector address after successful transfer with the buffer of a sector. This allows the microprocessor the ability to know which sector had an error if an error occurs.

Figures 2-1 and 2-2 show the pinouts of the AIC-8375. Many signal pins have pullup resistors (refer to Section 7 for pull-up, hysteresis, and other values). Most pullups can be enabled/disabled via the Device Control registers (reg. 50h, R/W, bit 7 and reg. 51h, R/W, bits 7, 6, & 4) as described in Section 5 of this document.

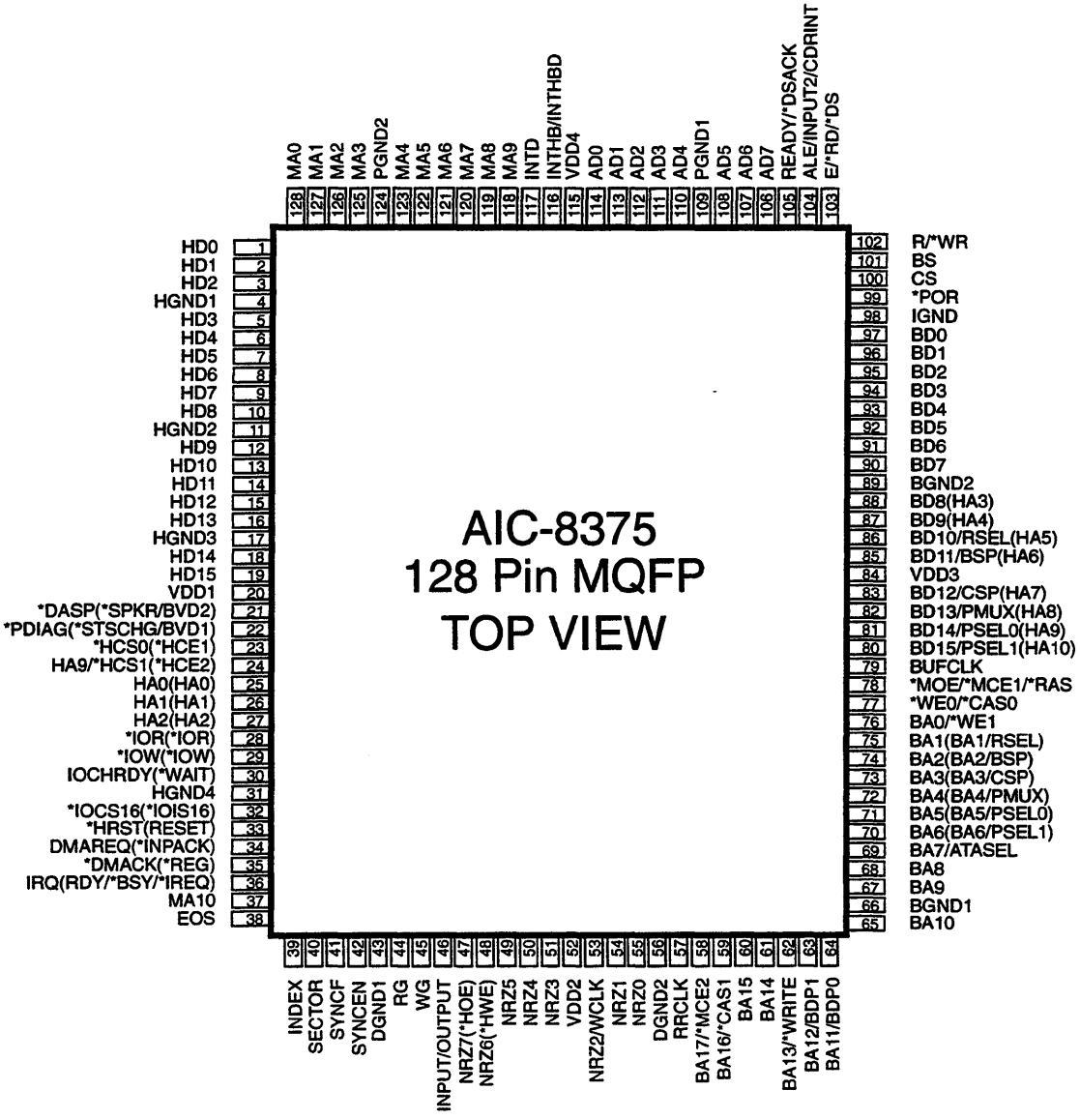

Figure 2-1 AIC-8375 MQFP Pin Assignments

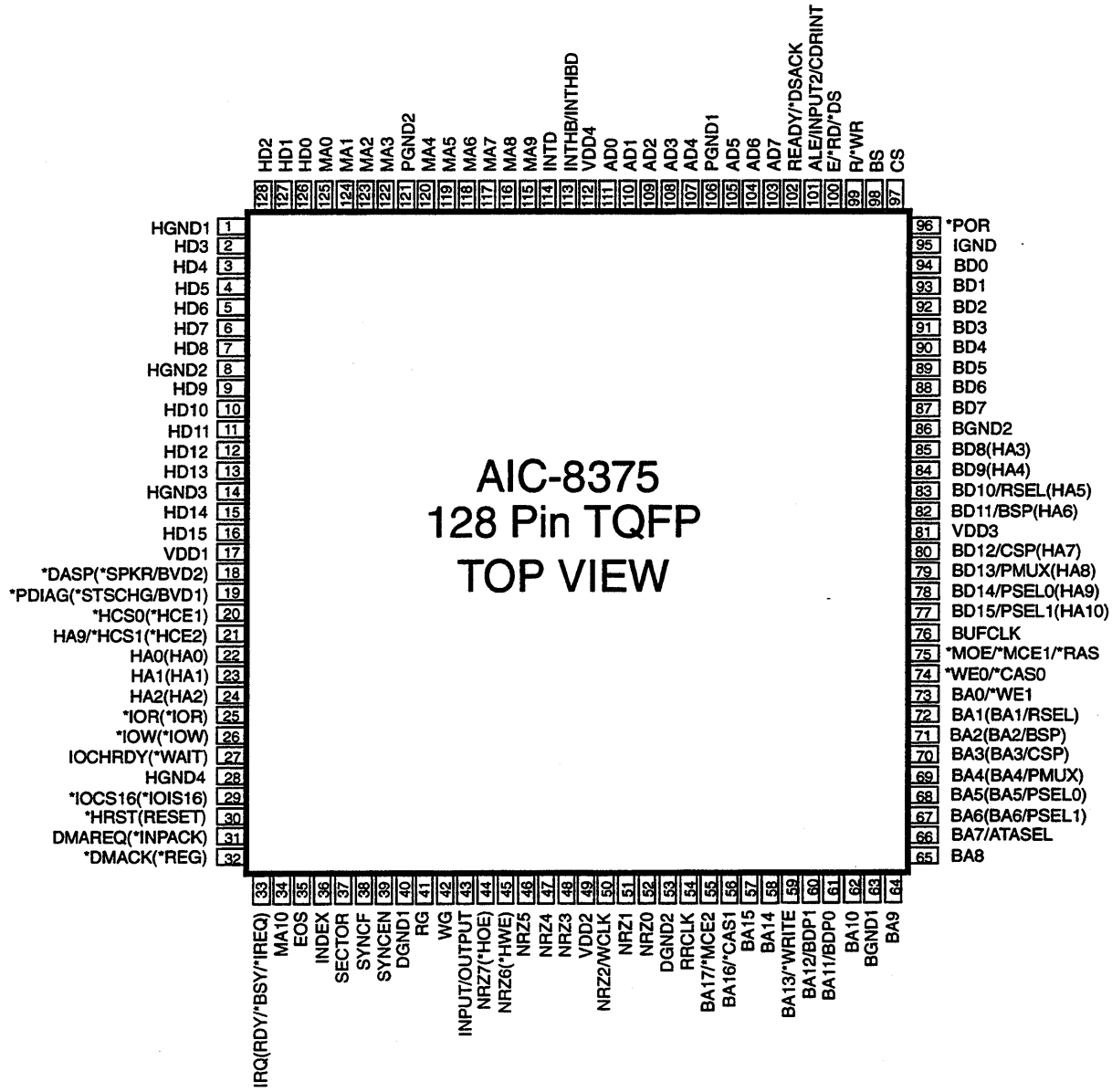

Figure 2-2 AIC-8375 TQFP Pin Assignments

2.1 AIC-8375 Disk Interface Pins

Refer to Section 7 of this document for hysteresis and pull-up values.

Table 2-1 Disk Interface Pin Descriptions

SYMBOL (* = active low)	PIN # (MQFP)	TYPE	DESCRIPTION
EOS	38	I (hysteresis)	END OF SERVO: This is a programmable input pin used to signal the end of a servo burst field. This input is edge sensitive with the polarity programmable via the ACTHIEOS bit (reg. 63h, R/W, bit 4).
INDEX	39	I (hysteresis)	INDEX: This is a programmable level edge sensitive input pin used to signal the Index point on the track of a Disk Drive HDA. The polarity is programmable via the ACTHIIDX bit (reg. 63h, R/W, bit 5). The leading (asserting) edge of the Index signal will set the INDEXPASS bit (reg. 65h, R/W, bit 5). This signal pin can be tested in the Sequencer Map.
SECTOR	40	I (hysteresis)	SECTOR: This is a programmable level edge sensitive input used to signal hard sector marks (SECTOR). The Disk Sequencer uses this as a branch condition, and it must be at least 2 BUFCLK periods in duration. The polarity is programmed with the ACTHISEC bit (reg. 63h, R/W, bit 6). The Disk Sequencer can be programmed to branch on this signal.
SYNCFND	41	I (hysteresis)	EXTERNAL SYNC FOUND: This is an active high input used to indicate when the external Sync Detect logic has found the sync byte. The polarity of this bit is programmable via the ACTHISFND bit (reg. 63h, R/W, bit 7).
SYNCEN	42	O (4 mA)	EXTERNAL SYNC DETECT ENABLE: This pin is an active high output used to enable an external sync detector. This pin is asserted via the "Wait For Sync Instruction" decode in the Sequencer Map.
RG	44	O (4 mA)	READ GATE: This is an active high output signal controlled by the Disk Sequencer, and it is used to enable the external Disk Drive Read circuitry.
WG	45	I/O (4 mA)	WRITE GATE: This is an active high output signal controlled by the Disk Sequencer, and it is used to enable the external Disk Drive Write circuitry. When it is high the appropriate NRZ pins for the NRZ mode are driven. This pin is an input during Host Standalone Test Mode only.

Table 2-1 Disk Interface Pin Descriptions (Continued)

SYMBOL (* = active low)	PIN # (MQFP)	TYPE	DESCRIPTION
INPUT/OUTPUT	46	I/O (4 mA w/ pull-up & hysteresis)	INPUT BRANCH / OUTPUT CONTROL: This pin can be programmed to be either an input or output of the disk sequencer. It can be used by the disk sequencer for branching on external events or for external control and status. If the ENOUPUT bit (reg. 62h, R/W, bit 4) is set, this pin is configured as an output. As an output, it is directly controlled via the Set and Reset OUTPUT control instructions in the disk sequencer. If ENOUTPUT is cleared, this pin is used as a level sensitive input branch condition in the disk sequencer.
NRZ7 (*HOE)	47	I/O (8 mA w/ pull-up & hysteresis)	DISK SERIAL NRZ I/O BIT 7/HOST OUTPUT ENABLE: ATA MODE - NRZ7: When WG is set this pin is bit 7 of the active high serial NRZ output, but it is only valid when in 8-bit NRZ Mode. When RG is set this pin is an input. PCMCIA MODE - *HOE: Refer to (*HOE) description in Table 2-3.
NRZ6 (*HWE)	48	I/O (8 mA w/ pull-up & hysteresis)	DISK SERIAL NRZ I/O BIT 6/HOST OUTPUT ENABLE: ATA MODE - NRZ6: When WG is set this pin is bit 6 of the active high serial NRZ output, but it is only valid when in 8-bit NRZ Mode. When RG is set this pin is an input. PCMCIA MODE - *HWE: Refer to (*HWE) description in Table 2-3.
NRZ[5:3]	49-51	I/O (4 mA w/ pull-up)	DISK NON RETURN TO ZERO [5:3]: These bits are used to send or receive bits 5:3 of the NRZ data to or from the drive. These bits are used only when the NRZSEL[1:0] bits (reg. 60h, R/W, bits 3:2) are set to '10', selecting 8-bit NRZ mode. These bits are driven while WG is asserted and receive data while RG is asserted.
NRZ2/WCLK	53	I/O (8 mA w/ pull-up)	DISK NON RETURN TO ZERO [2] / WRITE CLOCK: When 8-bit NRZ mode is selected (NRZSEL[1:0] = '10'), this pin is configured as NRZ2 and is driven while WG is asserted and receives data while RG is asserted. If 8-bit NRZ mode is not selected, this pin is configured as the disk write clock output which provides better setup and hold times for disk write operations than RRCLK. In this mode, a clock will always be present on the pin regardless of the state of WG or RG.

Table 2-1 Disk Interface Pin Descriptions (Continued)

SYMBOL (* = active low)	PIN # (MQFP)	TYPE	DESCRIPTION
NRZ[1:0]	54, 55	I/O (8 mA w/ pull-up)	DISK NON RETURN TO ZERO [1:0]: These signal pins function as the two least significant bits of 8-bit NRZ data if 8-bit NRZ mode is selected. If Dual bit NRZ mode is selected, these two bits are used to send and receive data in bit-pairs to and from the drive. If Single bit NRZ mode is selected, only NRZ0 is used to input or output a serial NRZ bit stream (refer to reg. 60h, R/W, bits 3:2).
RRCLK	57	I	READ / REFERENCE CLOCK: This pin is the input reference clock for the Disk controller logic. NRZ data is synchronized to it during reads and writes.

2.2 AIC-8375 Buffer Interface Pins

Refer to Section 7 of this document for hysteresis and pull-up values.

Table 2-2 Buffer Interface Pin Descriptions

SYMBOL (* = active low)	PIN # (MQFP)	TYPE	DESCRIPTION
BA17/*MCE2	58	O (4 mA)	BUFFER ADDRESS [17] / *MEMORY CHIP SELECT 2: This is an active high output pin used as address bit 17 in SRAM mode (256K) or an active low Chip Select in a two SRAM configuration. Dual SRAM mode is selected when the RAMSEL [2:0] bits (reg. 100h, R/W, bits 5:3) are set to '100', '101', or '110'.
BA16/*CAS1	59	O (8 mA)	BUFFER ADDRESS [16] / *COLUMN ADDRESS STROBE 1: This is an active high output pin used as address bit 16 in SRAM mode or an active low High Byte (bits 15:8) Column Address Strobe in DRAM mode.
BA[15:14]	60, 61	O (4 mA)	BUFFER ADDRESS [15:14]: These are active high output pins for address bits [15:14] in SRAM mode. They are not used in DRAM mode.
BA13/*WRITE	62	O (4 mA)	BUFFER ADDRESS [13] / *DRAM WRITE: This is the active high SRAM address bit 13 in SRAM mode or the active low write control for DRAM using early write mode access when in DRAM Mode.
BA12/BDP1	63	I/O (4 mA w/ pull-up)	BUFFER ADDRESS [12] / BUFFER DATA PARITY 1: This is the active high SRAM address bit 12 in SRAM mode or the active high Buffer Data parity for BD[15:8] in DRAM mode.
BA11/BDP0	64	I/O (4 mA w/ pull-up)	BUFFER ADDRESS [11] / BUFFER DATA PARITY 0: This is the active high SRAM address bit 11 in SRAM mode or the active high Buffer Data parity for BD[7:0] in DRAM mode.
BA[10:8]	65, 67, 68	O (4 mA)	BUFFER ADDRESS [10:8]: In SRAM mode, these pins are buffer addresses [10:8]. In DRAM mode, they are used as the row and column address lines.
BA7/ATASEL	69	I/O (4 mA w/ pull-up)	BUFFER ADDRESS[7] / ATA/*PCMCIA CONFIG PIN: At power on time (negation of *POR) this pin is automatically checked. If it is a 1, ATA Mode is selected; if it is a 0, PCMCIA Mode is selected (an external 6.8K pull-down resistor is used to bias this pin low). During this reset time the output driver is disabled; at all other times this pin is bit 7 of the Buffer Address. In ATA Mode, the MPU Configuration pins are on BD[15:10]; in PCMCIA Mode, they are on BA[6:1].

Table 2-2 Buffer Interface Pin Descriptions (Continued)

SYMBOL (* = active low)	PIN # (MQFP)	TYPE	DESCRIPTION
BA[6:1] (BA[6:1]/ PSEL[1:0], PMUX, CSP BSP, RSEL)	70-75	I/O (4 mA w/ pull-up)	ATA MODE - BUFFER ADDRESS[6:1]: These are active high output pins used to address the Buffer Memory. PCMCIA MODE - BUFFER ADDRESS[6:1] / ATA/*PCMCIA CONFIG PIN: At power on time these pins are the MPU Configuration pins which are checked when *POR is negated. The output drivers are disabled at this time. At all other times they are bits 6:1 of the Buffer Address. Refer to the ATA pin definitions for BD[15:10] to determine the MPU Configuration operation. An external 6.8K pull-down resistor is used to bias each pin low at power on time.
BA0/*WE1	76	O (8 mA)	BUFFER ADDRESS [0] / *WRITE ENABLE 1: This is a multifunction output pin based on the type and width of RAM used. In DRAM mode and in 8-bit SRAM mode, this pin is configured as BA0. In 16-bit SRAM mode, it is configured as *WE1 and is used as the SRAM Write Enable signal for BD[15:8] only.
*WE0/*CAS0	77	O (8 mA)	*MEMORY WRITE ENABLE 0 / *COLUMN ADDRESS STROBE 0: In DRAM mode, this pin is an active low output used for the CAS function. In SRAM mode, it is configured as the Write Enable signal to the SRAM bits 7:0. RAM SELECT [2:0], (reg. 100h, R/W, bits 5:3) establishes the function of this pin.
*MOE/*MCE1/ *RAS	78	O (8 mA)	*MEMORY OUTPUT ENABLE / *MEMORY CHIP ENABLE 1 / *ROW ADDRESS STROBE: In DRAM mode, this pin is an active low output used for the RAS function. In SRAM mode it is an active low output function of Output Enable (*MOE) or Chip Enable (*MCE1). RAM SELECT [2:0], (reg. 100h, R/W, bits 5:3) establishes the function of this pin.
BUFCLK	79	I	BUFFER CLOCK: This input is the clock source for the Buffer Controller and Host Interface logic.

Table 2-2 Buffer Interface Pin Descriptions (Continued)

SYMBOL (* = active low)	PIN # (MQFP)	TYPE	DESCRIPTION
BD[15:14] / PSEL[1:0] (HA[10:9])	80, 81	I/O (4 mA w/ pull-up & hysteresis)	ATA MODE - BUFFER DATA [15:14] / PROCESSOR SELECT: These pins are dual function pins. On the rising (negating) edge of Power On Reset (*POR), these pins are internally sampled. Based upon the value of PSEL[1:0] (see AIC-8375 User's Guide) at this sample time, the device will be configured to interface with a specific microprocessor. At all other times, these pins function as bits [15:14] of the Buffer Data bus. These pins incorporate internal pullup resistors to bias the pins high. A 6.8K Ohm external resistor tied to ground can be used to pull down these pins. Without any external pulldown resistors, the default value of PSEL[1:0] after *POR is '11'. PCMCIA MODE - HOST ADDRESS[10:9]: These pins are active high inputs used as bits 10:9 of the Host Address.
BD13/PMUX (HA8)	82	I/O (4 mA w/ pull-up & hysteresis)	ATA MODE - BUFFER DATA [13] / PROCESSOR BUS MODE: This is a dual function pin. On the rising (negating) edge of Power On Reset (*POR) this pin is internally sampled. If it is found to be high, the device is configured for multiplexed microprocessor bus mode. If found to be low, the device is configured for non-multiplexed microprocessor bus mode. At all other times, this pin functions as bit 13 of the Buffer Data bus. This pin has an internal pullup resistor to bias the pin high. A 6.8K Ohm pull-down resistor is externally used to pull it down. Without an external pulldown resistor, the default value of PMUX after *POR is '1' (multiplexed mode). PCMCIA MODE - HOST ADDRESS[7]: This pin is an active high input used as bit 8 of the Host Address.

Table 2-2 Buffer Interface Pin Descriptions (Continued)

SYMBOL (* = active low)	PIN # (MQFP)	TYPE	DESCRIPTION
BD12/CSP (HA7)	83	I/O (4 mA w/ pull-up & hysteresis)	ATA MODE - BUFFER DATA [12] / CHIP SELECT POLARITY: This is a dual function pin. On the rising (negating) edge of Power On Reset (*POR) this pin is internally sampled. If found to be low, the polarity of the Chip Select (CS) pin is inverted. If found to be high, the polarity is not inverted. At all other times, this pin functions as bit 12 of the Buffer Data bus. This pin has an internal pullup resistor to bias the pin high. A 6.8K Ohm pulldown resistor is externally used to pull it down. PCMCIA MODE - HOST ADDRESS[7]: This pin is an active high input used as bit 7 of the Host Address.
BD11/BSP (HA6)	85	I/O (4 mA w/ pull-up & hysteresis)	ATA MODE - BUFFER DATA [11] / BUFFER SELECT POLARITY: This is a dual function pin. On the rising (negating) edge of Power On Reset (*POR) this pin is internally sampled. If found to be low, the polarity of the Buffer Select (BS) pin is inverted. If found to be high, the polarity is not inverted. At all other times, this pin functions as bit 11 the Buffer Data bus. This pin has an internal pullup resistor to bias the pin high. A 6.8K Ohm pulldown resistor is externally used to pull it down. PCMCIA MODE - HOST ADDRESS[6]: This pin is an active high input used as bit 6 of the Host Address.
BD10/RSEL (HA5)	86	I/O (4 mA w/ pull-up & hysteresis)	ATA MODE - BUFFER DATA [10] / READY SELECT: This is a dual function pin. On the rising (negating) edge of Power On Reset (*POR) this pin is internally sampled. If found to be low, the READY pin is active low, otherwise it is active high. At all other times it is bit 10 of the Buffer RAM data bus. This pin has an internal pullup resistor to bias the pin high. A 6.8K Ohm pulldown resistor is externally used to pull it down. Without any external pulldown resistor, the default value of RSEL will be high configuring the READY line for active high (see AIC-8375 User's Guide for the use of this function). PCMCIA MODE - HOST ADDRESS[5]: This pin is an active high input used as bit 5 of the Host Address.

Table 2-2 Buffer Interface Pin Descriptions (Continued)

SYMBOL (* = active low)	PIN # (MQFP)	TYPE	DESCRIPTION
BD[9:8] (HA[4:3])	87, 88	I/O (4 mA w/ pull-up & hysteresis)	ATA MODE - BUFFER DATA [9:8]: These are active high input/output pins. They are bits [9:8] of the Buffer RAM data. These pins have internal pullup resistors to bias the pins high. External 6.8K Ohm pulldown resistors can be used on these pins to create '0' values when this bus is read to retrieve the User Configuration Bits. PCMCIA MODE - HOST ADDRESS[4:3]: These pins are active high inputs used as bits 4:3 of the Host Address.
BD[7:0]	90-97	I/O (4 mA w/ pull-up & hysteresis)	BUFFER DATA [7:0]: These are active high input/output pins. They are bits [7:0] of the Buffer RAM data. These pins have internal pullup resistors to bias the pins high. External 6.8K Ohm pulldown resistors can be used on these pins to create '0' values when this bus is read to retrieve the User Configuration Bits. (See AIC-8375 User's Guide.)

2.3 AIC-8375 Host Interface Pins

Refer to Section 7 of this document for hysteresis and pull-up values.

Table 2-3 Host Interface Pin Descriptions

SYMBOL (* = active low)	PIN # (MQFP)	TYPE	DESCRIPTION
*DASP (*SPKR/BVD2)	21	I/O (24 mA w/ pull-up)	ATA MODE - *DRIVE ACTIVE / SLAVE PRESENT: This is an active low input/output signal used for communication between Master and Slave drives (Slave Present), and typically is also used to drive an activity LED to indicate that the drive is active (Drive Active). This pin is driven/read by the *DASP/*SPKR bit (reg. BFh, R/W, bit 5). When inactive this pin can be programmed with HHIZ (reg. 55h, R/W, bit 5) to be in a high impedance driven state. PCMCIA MODE - *SPEAKER/BATTERY VOLTAGE DEAD 2: When in I/O Configuration this is an active low output signal used as a Binary Audio Waveform to the speaker. When in Memory Card Configuration this is an active high output signal Battery Voltage Detect used to signal battery condition.
DMAREQ (*INPACK)	34	O (24 mA)	ATA MODE - DMA REQUEST: This is an active high tri-state output used to request a DMA transfer on the ATA interface. When inactive this pin can be programmed with HHIZ (reg. 55h, R/W, bit 5) to be in a high impedance driven state. PCMCIA MODE - ATTRIBUTE MEMORY OR I/O SELECT: This is an active high output used in Primary/Secondary I/O Addressing Mode to indicate that a valid address has been decoded by the AIC-8375 and data is available on the HDB[15:0] pins for reading by the Host. This signal can be used by the host to enable its input data buffers.
*DMACK (*REG)	35	I (pull-up & hysteresis)	ATA MODE - *DMA ACKNOWLEDGE: This is an active low input used with DMAREQ to complete a DMA handshake for data transfer on the ATA interface. This pin has an internal pullup resistor to bias the pin high. PCMCIA MODE - ATTRIBUTE MEMORY OR I/O SELECT: This is an active low input that specifies that an access to the Attribute Memory or the Task File Registers is occurring in one of the I/O Addressing Modes.

Table 2-3 Host Interface Pin Descriptions (Continued)

SYMBOL (* = active low)	PIN # (MQFP)	TYPE	DESCRIPTION
(HA[10:3]) BD[15:8]	80-83, 85-88	I/O (4 mA w/ pull-up & hysteresis)	ATA MODE - BUFFER DATA [15:8]: See BD[15:8] pin definitions in Buffer Interface Section 2.2. PCMCIA MODE - HOST ADDRESS [10:3]: These are active high inputs used to address the required AT Task File Registers. The active addressing mode (Primary/Secondary I/O, Block I/O, or Memory) determines which lines are used. These pins have internal pullup resistors to bias the pins high.
HA[2:0]	27-25	I (pull-up & hysteresis)	ATA MODE - HOST ADDRESS [2:0]: These are active high inputs used to address the required AT Task File Registers. PCMCIA MODE - HOST ADDRESS [2:0]: These are active high inputs used to address the required AT Task File Registers. The active addressing mode (Primary/Secondary I/O, Block I/O, or Memory) determines which lines are used. These pins have internal pullup resistors to bias the pins high.
HA9/*HCS1 (*HCE2)	24	I (pull-up & hysteresis)	ATA MODE - HOST ADDRESS [9] / *HOST CHIP SELECT 1: This pin can be programmed to function either as Host Address 9 or as Host Chip Select 1 and is selected via the HCS1SEL bit (reg. C0h, R/W, bit 3). When HCS1SEL is cleared, this signal is the active high Host Address bit 9. When HCS1SEL is set, this signal is the active low Host Chip Select 1. This bit distinguishes between 1Fx and 3Fx register ports. *HCS1 is chosen in those systems in which address lines are decoded on the ATA paddle board and produce an *HCS1 signal. HA9 is chosen in those systems that can directly use this address line to eliminate the *HCS1 decode logic. After power up this pin defaults to the HA9 state. This pin has an internal pullup resistor to bias the pin high. PCMCIA MODE - HOST CARD ENABLE 2: This is an active low input which enables the data byte on Host Data pins HD[15:8]. Internally HA0 is forced to 0 for addressing the Task File Register block. Sixteen bit transfers are performed when both *HCE1 and *HCE2 are asserted.

Table 2-3 Host Interface Pin Descriptions (Continued)

SYMBOL (* = active low)	PIN # (MQFP)	TYPE	DESCRIPTION
*HCS0 (*HCE1)	23	I (pull-up & hysteresis)	ATA MODE - *HOST CHIP SELECT 0: This is an active low input used to select PIO access to the chip. This pin has an internal pullup resistor to bias the pin high. PCMCIA MODE - HOST CARD ENABLE 1: This is an active low input that enables data bytes on Host Data bits HD[7:0]. Sixteen bits are transferred if both *HCE1 and *HCE2 are asserted, and the transfer is eight bits if only *HCE1 is asserted. During 8-bit accesses A0 selects odd or even bytes. During 16-bit accesses A0 is assumed to be 0.
HD[15:0]	19, 18, 16-12, 10-5, 3-1	I/O (12 mA w/ pull-up & hysteresis)	ATA MODE - HOST DATA BUS [15:0]: This 16-bit bus is used to transfer Data, Commands, and Status between the Host and Drive Controller. During 16-bit DMA and PIO data transfer all bits are used. During 8-bit DMA and PIO data transfers and Command and Status transfers (always 8 bits) only bits 7:0 are used. These pins have internal pullup resistors to bias them high. PCMCIA MODE - HOST DATA BUS [15:0]: This 16-bit bus is used to transfer Data, Commands, and Status between the Host and Drive Controller. During 16-bit PIO data transfer all bits are used. During 8-bit PIO data transfers and Command and Status transfers (always 8 bits) inputs *HCE1 and *HCE2 determine high byte HD[15:8] or low byte HD[7:0] usage.
(*HOE) NRZ7	47	I/O (8 mA w/ pull-up & hysteresis)	ATA MODE - NRZ DATA BIT 7: Refer to NRZ7 pin definition in the Disk Interface Section 2.1. PCMCIA MODE - HOST OUTPUT ENABLE: This is an active low input pin that is used to read the Attribute Memory or Task File Registers (if in Memory Addressing Mode). The *REG input pin distinguishes between Attribute Memory or Task File Registers.

Table 2-3 Host Interface Pin Descriptions (Continued)

SYMBOL (* = active low)	PIN # (MQFP)	TYPE	DESCRIPTION
(*HWE) NRZ6	48	I/O (8 mA w/ pull-up & hysteresis)	ATA MODE - NRZ DATA BIT 6: Refer to NRZ6 pin definition in the Disk Interface Section 2.1. PCMCIA MODE - HOST WRITE ENABLE: This is an active low input pin that is used to write to the Card Configuration Registers, or if in Memory Addressing Mode into the Task File Registers. The *REG input pin distinguishes between Card Configuration Registers or Task File Registers.
*HRST (RESET)	33	I (pull-up & hysteresis)	ATA MODE - *HOST RESET: This active low input is used by the Host to reset the Host Interface Logic. This pin has an internal pullup resistor to bias the pin high. PCMCIA MODE - RESET: This is an active high level input used by the Host to reset the Host Interface Logic.
*IOCS16 (*IOCS16)	32	O (24 mA)	ATA MODE - *16 BIT HOST DATA ENABLE: This is an active low tri-state output used to signal to the host the number of bits used during PIO transfers. It is negated during DMA transfers and 8-bit PIO transfers. This pin can be programmed as open drain (default) with the ENIOCS16OD control bit (reg. C5h, R/W, bit 7). PCMCIA MODE - *16 BIT HOST DATA ENABLE: This is an active low tri-state output used to signal to the host the number of bits used during PIO transfers. In Block and Primary/Secondary I/O Addressing Modes this output indicates that the addressed register is capable of 16-bit I/O transfers. The host then has the option to perform an 8- or 16-bit transfer. While in Memory Addressing Mode this output represents the write protected status of the PCMCIA interface.
IOCHRDY (*WAIT)	30	O (24 mA)	ATA MODE - I/O CHANNEL READY: This is an active high tri-state output used for flow control on the Host data transfers. This signal is driven low to insert wait states into Host I/O cycles. When inactive this pin can be programmed with HHIZ (reg. 55h, R/W, bit 5) to be in a high impedance driven state. PCMCIA MODE - *WAIT: This active low tri-state output is used during Task File Register access or data transfers to extend the Host I/O cycle.

Table 2-3 Host Interface Pin Descriptions (Continued)

SYMBOL (* = active low)	PIN # (MQFP)	TYPE	DESCRIPTION
*IOR (*IOR)	28	I/O (4 mA w/ pull-up & hysteresis)	ATA MODE - *I/O READ: This is an active low input pin used to enable read data from the Controller to the Host onto the HD[15:0] data bus when asserted with the proper combination of *HCS0, HA9/ *HCS1, and HA[2:0]. This pin has an internal pullup resistor to bias the pin high. PCMCIA MODE: - *I/O READ: This is an active low input pin used to enable read data from the Controller to the Host onto the HD[15:0] data bus when asserted with the proper combination of the *REG, *HCE1, *HCE2, and HA[9:0] pins. This pin is an output during EDAC Standalone Test Mode only.
*IOW (*IOW)	29	I/O (4 mA w/ pull-up & hysteresis)	ATA MODE - *I/O WRITE: This is an active low input pin used to write data to the Controller from the Host via the HD[15:0] data bus when asserted with the proper combination of *HCS0, HA9/*HCS1, and HA[2:0]. This pin has an internal pullup resistor to bias the pin high. PCMCIA MODE - *I/O WRITE: This is an active low input pin used to write data to the Task File Registers from the Host onto the HD[15:0] data bus when asserted with the proper combination of *REG, *HCE1, *HCE2, and HA[9:0]. This pin is an output during EDAC Standalone Test Mode only.
IRQ (RDY/*BSY/ *IREQ)	36	O (24 mA)	ATA MODE - INTERRUPT REQUEST: This is an active high tri-state output used to alert the Host to start a Data I/O transfer. This is an output signal during normal operation. When inactive this pin can be programmed with HHIZ (reg. 55h, R/W, bit 5) to be in a high impedance driven state. PCMCIA MODE - READY/*BUSY or INTERRUPT REQUEST: This is an output pin that is defined per the current addressing mode. In Memory Addressing Mode (default after power-up or RESET) it is the Ready/Busy Status. In the I/O addressing modes it is the active low Interrupt Request

Table 2-3 Host Interface Pin Descriptions (Continued)

SYMBOL (* = active low)	PIN # (MQFP)	TYPE	DESCRIPTION
*PDIAG (*STSCHG/BVD1)	22	I/O (24 mA w/ pull-up)	ATA MODE - *PASSED DIAGNOSTICS: This pin functions as an active low input/output control signal and is used for communication from the Slave drive to the Master drive. It is negated whenever the *POR and *HRST pins are active or when the Host Programmed Reset bit is set (Host reg. 3F6h, bit 2). It is driven/read via the *PDIAG bit (reg. BFh, R/W, bit 6). When inactive this pin can be programmed with HHIZ (reg. 55h, R/W, bit 5) to be in a high impedance driven state. PCMCIA MODE - STATUS CHANGED: In I/O Addressing Mode this is and active low output that is asserted when any of the Pin Replacement Register bits (CBVD1, CBVD2, CRDY/*BSY, or CWPROT) is set to one. In Memory Addressing Mode this is the BVD1 pin. It is driven/read via the *PDIAG bit (reg. BFh, R/W, bit 6).

2.4 AIC-8375 Microprocessor Interface Pins

Refer to Section 7 of this document for hysteresis and pull-up values.

Table 2-4 Microprocessor Interface Pin Definitions

SYMBOL (* = active low)	PIN # (MQFP)	TYPE	DESCRIPTION
CS	100	I	CHIP SELECT: This is a programmable level input used to select registers in the chip. When it is active the input controls are enabled to access the internal registers. The BD12/CS pin initializes the polarity of this signal when *POR is negated.
BS	101	I	BUFFER SELECT: This is a programmable level input used to select access to the Buffer Memory RAM through the chip. When it is active the input controls are enabled to access the RAM. The BD11/BS pin initializes the polarity of this signal when *POR is negated.
R/*WR	102	I	READ-WRITE DIRECTION / *WRITE STROBE: This is a dual function input pin whose function is programmed via the BD[15:14] / PSEL[1:0] pins when *POR is negated. When Motorola type is selected this pin is the READ-WRITE DIRECTION (R) function (high for read, low for write). When Intel type is selected it functions as the active low Write Strobe (*WR).
E/*RD/*DS	103	I	ECLK / *READ STROBE / *DATA STROBE: This is a multi-function input pin used to enable the transfer of data on the AD[7:0] pin to/from the chip internal registers. It is configured when *POR is negated at reset time by the BD[15:14]/PSEL[1:0] pins. For Intel type processors, it is configured as an active low READ STROBE (*RD) and is used to enable register data out of the chip. For Motorola 68HC11 type processors, it becomes the active high ECLK (E) and is used to write/read data to/from the chip registers via AD[7:0]. For Motorola 68HC16 type processors, this pin is configured as the active low DATA STROBE (*DS) and is used to write/read data to/from the chip registers via AD[7:0].
ALE/IN2/CDRINT	104	I	ADDRESS LATCH ENABLE / DISK SEQUENCER INPUT 2 / EXTERNAL CDR INTERRUPT: This is an active high input used to latch the address on the AD[7:0] pins when configured for multiplexed processor mode. An internal transparent latch is used to latch the address from the AD[7:0] lines on the falling edge of ALE. When configured for non-multiplexed processor mode this can be used as a level sensitive input branch to the disk sequencer (alternate branch 011b) or as an external CDR Interrupt. CDRINT is selected via the ENEXTCDR bit (reg. 61h, R/W, bit 5).

Table 2-4 Microprocessor Interface Pin Definitions (Continued)

SYMBOL (* = active low)	PIN # (MQFP)	TYPE	DESCRIPTION
READY / *DSACK	105	O (8 mA w/ pull-up)	READY / *DATA SIZE ACKNOWLEDGE: This is an output pin whose function is selected via the BD[15:14] / PSEL[1:0] pins at reset time. When Motorola 68HC11 and Intel type is selected, this pin functions as the the READY line (high for ready, low for not ready). When Motorola 68HC16 type is selected, it becomes the active low DATA SIZE ACKNOWLEDGE signal (*DSACK, connect to *DSACK0 of 68HC16). The READY line is configured for push-pull operation when the ENPPRDY bit (reg. 51h, R/W, bit 3) is set and operates in open-drain mode when this bit is cleared. See also Table 2-1 in the AIC-8375 User's Guide.
AD[7:0]	106-108, 110-114	I/O (4 mA w/ pull-up)	µP ADDRESS/DATA [7:0]: This is an active high I/O bus used to interface to the local microprocessor. In multiplexed microprocessor mode, these pins are connected to the microprocessor address/data bus. In non-multiplexed mode, these pins are connected to the microprocessor data bus only.
INTHB / INTHBD	116	O (4 mA w/ pull-up)	HOST-BUFFER INTERRUPT / HOST-BUFFER-DISK INTERRUPT: This is a programmable level (reg. 51h, R/W, bit 0) output pin which can also be programmed (reg. 51h, R/W, bit 1) as push/pull or open drain. It goes active when the EN_BUFINT[1:0] and/or EN_HOSTINT[2:0] bits (reg. 53h, R/W, bits 4:3 and 2:0 respectively) are set and one or more bits in the corresponding interrupt registors are set. It can also be programmed to include Disk Interrupts which are enabled by the EN_DISKINT[1:0] bits (reg. 53h, R/W, bits 6:5). Combining the Disk Interrupt is enabled by setting the COMBINT bit (reg. 51h, R/W, bit 2). Polarity is determined by ACTHIINT (reg. 51h, R/W, bit 0). This pin defaults to active low/open drain at power-up (refer to reg. 51h, R/W, bit 1).
INTD	117	O (4 mA w/ pull-up)	DISK INTERRUPT: This is a programmable level (reg. 51h, R/W, bit 0) output pin which can be programmed (reg. 51h, R/W, bit 1) as push/pull or open drain. It goes active when the EN_DISKINT[1:0] bits (reg. 53h, R/W, bits 6:5) are set and one or more bits in the corresponding interrupt register (reg. 52h, R, bits 6:5) are set. Polarity is determined by the ACTHIINT bit (reg. 51h, R/W, bit 0). This pin defaults to active low/open drain mode at power-up (refer to reg. 51h, R/W, bit 1).
MA[10:8]	37, 118, 119	I	MICROPROCESSOR ADDRESS [10:8]: These are active high input pins used with MA[7:0] to address the internal registers and Buffer Memory.

Table 2-4 Microprocessor Interface Pin Definitions (Continued)

SYMBOL (* = active low)	PIN # (MQFP)	TYPE	DESCRIPTION
MA[7:0]	120-123, 125-128	I/O (4 mA w/ pull-up)	MICROPROCESSOR ADDRESS [7:0]: These are active high input/output pins used with MA[10:8] to address the internal registers and Buffer Memory. When in a Multiplexed bus mode these pins are outputs and reflect the value internally latched by ALE on the AD[7:0] data lines.
*POR	99	I (hysteresis)	*POWER ON RESET: An active low signal on this input pin will reset logic within the device.

2.5 AIC-8375 Power/Ground Pins

Table 2-5 Power/Ground Pin Descriptions

SYMBOL (* = active low)	PIN # (MQFP)	TYPE	DESCRIPTION
BGND1	66	GND	BUFFER GROUND 1: I/O ring ground for Buffer Interface pins BA17/*MCE2, BA16/CAS1, BA[15:14], BA13/*WRITE, BA12/BDP1, BA11/BDP0, and BA[10:1].
BGND2	89	GND	BUFFER GROUND 2: I/O ring ground for Buffer Interface pins BD[15:0], BUFCLK, *MOE/*RAS, *WE0/*CAS0, and *WE1/*CAS1.
DGND1	43	GND	DISK GROUND 1: I/O ring ground for Disk Interface pins RG, WG, SYNCF, INDEX, SECTOR, INPUT/OUTPUT, EOS.
DGND2	56	GND	DISK GROUND 2: I/O ring ground for all Disk Interface pins NRZ[7:0], RRCLK.
HGND1	4	GND	HOST GROUND 1: I/O ground for Host Data Bus pins HD[5:0].
HGND2	11	GND	HOST GROUND 2: I/O ground for Host Data Bus pins HD[10:6].
HGND3	17	GND	HOST GROUND 3: I/O ground for Host Data Bus pins HD[15:11].
HGND4	31	GND	HOST GROUND 4: I/O ring ground for Host Interface pins *DASP, *DMACK, DMARQ, HA[2:0], HA9/*HCS1, *HCS0, *HRST, *IOCS16, IOCHRDY, *IOR, *IOW, IRQ, and *PDIAG.
IGND	98	GND	INTERNAL GROUND: Substrate Ground, not tied to any I/O ring ground.
PGND1	109	GND	PROCESSOR GROUND 1: I/O ring ground for Processor Interface pins READY, *POR, CS, BS, ALE/INPUT2/CDRINT, E/*RD/*DS, R/*WR, and AD[7:0].
PGND2	124	GND	PROCESSOR GROUND 2: I/O ring ground for Processor Interface pins MA[9:0], INTHB, and INTD.
VDD1-4	20, 52, 84, 115	GND	CHIP POWER 1-4: I/O ring power and internal power pins.

3.1 Device Control Registers

Addresses in parentheses indicate register mapping in Motorola Mode.

50h (R/W) RST/PWR DOWN CNTRL	51h (R/W) CHIP MODE	52h (R) CHIP STATUS	53h (R/W) CHIP INTERRUPT ENABLE
7 Disable All Pull-Ups	7 Disable Host Addr. Pull-Ups	7 Microproc. Access Busy	7 Scan Test Mode Enable
6 Reserved	6 Disable Host Ctrl. Pull-Ups	6 Disk Interrupt Active[1]	6 Disk Interrupt Enable[1]
5 En. Disk Block Power Dn	5 Swap Register Addresses	5 Disk Interrupt Active[0]	5 Disk Interrupt Enable[0]
4 En. Buffer Block Power Dn	4 Disable Buf. Data Pull-Ups	4 Buffer Interrupt Active[1]	4 Buffer Interrupt Enable[1]
3 En. Host Block Power Dn	3 Enable Push-Pull Ready	3 Buffer Interrupt Active[0]	3 Buffer Interrupt Enable[0]
2 Disk Block Reset	2 Combine All Interrupts	2 Host Interrupt Active[2]	2 Host Interrupt Enable[2]
1 Buffer Block Reset	1 En. Push-Pull Int. Outputs	1 Host Interrupt Active[1]	1 Host Interrupt Enable[1]
0 Host Block Reset	0 En. Active High Int. Outputs	0 Host Interrupt Active[0]	0 Host Interrupt Enable[0]

54h (R) CHIP REVISION	55h (R/W) CHIP TEST
7 Revnum[7]	7 Disk Interface Hi Z Mode
6 Revnum[6]	6 Buffer Interface Hi Z Mode
5 Revnum[5]	5 Host Interface Hi Z Mode
4 Revnum[4]	4 Input Thresh. Volt. Test
3 Revnum[3]	3 Output Voltage Test
2 Revnum[2]	2 Test Mode[2]
1 Revnum[1]	1 Test Mode[1]
0 Revnum[0]	0 Test Mode[0]

3.2 Disk Control Registers

Addresses in parentheses indicate register mapping in Motorola Mode.

58h (R/W) EOS COUNTER	59h (R/W) EOS MAXIMUM	5Ah (5Bh) (R/W) CURRENT SECTOR 0	5Bh (5Ah) (R/W) CURRENT SECTOR 1
7 EOSCTR[7]	7 EOSMAX[7]	7 CURRSEC[7]	7 CURRSECEQ (R)
6 EOSCTR[6]	6 EOSMAX[6]	6 CURRSEC[6]	6 EOSCMPEQ (R)
5 EOSCTR[5]	5 EOSMAX[5]	5 CURRSEC[5]	5 EOSMAXEQ (R)
4 EOSCTR[4]	4 EOSMAX[4]	4 CURRSEC[4]	4 WRAPSECEQ (R)
3 EOSCTR[3]	3 EOSMAX[3]	3 CURRSEC[3]	3 Reserved
2 EOSCTR[2]	2 EOSMAX[2]	2 CURRSEC[2]	2 Reserved
1 EOSCTR[1]	1 EOSMAX[1]	1 CURRSEC[1]	1 CURRSEC[9]
0 EOSCTR[0]	0 EOSMAX[0]	0 CURRSEC[0]	0 CURRSEC[8]

5Ch (R/W) EOS COMPARE	5Dh (R/W) DISK CONTROL 4	5Eh (R/W) DISK INTERRUPT STATUS 0	5Fh (R/W) DISK INTERRUPT EN. 0
7 EOSCMP[7]	7 Reserved	7 Servo Overrun Int.	7 En. Servo Overrun Int.
6 EOSCMP[6]	6 Stop On Seed Overrun	6 Reserved	6 Reserved
5 EOSCMP[5]	5 Stop On Auto Write	5 Reserved	5 Reserved
4 EOSCMP[4]	4 Enable Seed	4 Soft. Corr. ECC Error Int.	4 En. Soft. Corr. ECC Error
3 EOSCMP[3]	3 Stop On CDR Parity Error	3 Sector Hit	3 En. Sector Hit Int.
2 EOSCMP[2]	2 Stop On Seed Error	2 Reserved	2 Reserved
1 EOSCMP[1]	1 En. Clr EOS Ctr On Index	1 Data Comp. Not Equal Int.	1 En. Data Comp. Not Equal
0 EOSCMP[0]	0 Enable EDSA Mode	0 Write Fault Interrupt	0 En. Write Fault Int.

60h (R/W) DISK CONTROL 0	61h (R/W) DISK CONTROL 1	62h (R/W) DISK CONTROL 2	63h (R/W) DISK CONTROL 3
7 Disk Write	7 En. 2-Byte Fault Tol. Sync	7 Disk Verify	7 Sel. Active High Sync Fnd
6 Reset Disk FIFO (W)	6 Disable FIFO Flush	6 Supress Transfer	6 Sel. Active High SEC
5 En. NRZ to RRCLK ↓	5 En. External CDR Int.	5 Reserved	5 Sel. Active High Index
4 Reserved	4 En. Index to Sect. Branch	4 Enable Output	4 Sel. Active High EOS
3 NRZ Select[1]	3 Stop On Input Write Fault	3 Enable CDR	3 Reserved
2 NRZ Select[0]	2 Ext. Sync Found Offset[2]	2 Enable CURRSECEQ	2 En. CDR FIFO Read POP
1 Delay Write Gate	1 Ext. Sync Found Offset[1]	1 Enable BUFNRDY	1 En. CDR Bytes From Buffer
0 En. SYNCFND to RRCLK ↓	0 Ext. Sync Found Offset[0]	0 Enable DEFSEC	0 En. External Sync Found

64h (R/W) DISK STATUS 0	65h (R/W) DISK STATUS 1	66h (R) DISK INTERRUPT STATUS 1	66h (W) DISK INTERRUPT CLEAR 1
7 ECC Seed FIFO Overrun	7 EOS Passed	7 Two Index Time-out Int.	7 Clr. Two Index Time-out Int.
6 CDR Parity Error	6 EOS Compare Passed	6 Sequencer Time-out Int.	6 Clr. Seq. Time-out Int.
5 Missing RRCLK Detected	5 Index Passed	5 Uncorr. ECC Int.	5 Clr. Uncorr. ECC Int.
4 Reserved	4 Sector Passed	4 Reserved	4 Reserved
3 Reserved	3 Output Pin State (R)	3 Corrected ECC Int.	3 Clr. Corrected ECC Int.
2 Buffer Not Ready (R)	2 Input Pin State (R)	2 Sec. Num. Wrapped Int.	2 Clr. Sec. Num. Wrapped Int.
1 Seq. Timeout On SECVLD	1 Seq. Timeout On EOSCMP	1 Sector OK Int.	1 Clr. Sector OK Int.
0 Stop Sector Reached (R)	0 Index Counter=0 (R)	0 Sequencer Stopped Int.	0 Clr. Seq. Stopped Int.

67h (R/W) DISK INTERRUPT ENABLE 1	68h (69h) (R/W) WRAP SECTOR NUMBER 0	69h (68h) (R/W) WRAP SECTOR NUMBER 1	6Ah (6Bh) (R/W) WRAP TO SECTOR 0
7 En. Two Index Time-out Int.	7 WRAPSEC[7]	7 Reserved	7 WRAP TO SECTOR[7]
6 En. Seq. Time-out Int.	6 WRAPSEC[6]	6 Reserved	6 WRAP TO SECTOR[6]
5 En. Uncorr. ECC Int.	5 WRAPSEC[5]	5 Reserved	5 WRAP TO SECTOR[5]
4 Reserved	4 WRAPSEC[4]	4 Reserved	4 WRAP TO SECTOR[4]
3 En. Corrected ECC Int.	3 WRAPSEC[3]	3 Reserved	3 WRAP TO SECTOR[3]
2 En. Sec. Num. Wrapped Int.	2 WRAPSEC[2]	2 Reserved	2 WRAP TO SECTOR[2]
1 En. Sector OK Int.	1 WRAPSEC[1]	1 WRAPSEC[9]	1 WRAP TO SECTOR[1]
0 En. Seq. Stopped Int.	0 WRAPSEC[0]	0 WRAPSEC[8]	0 WRAP TO SECTOR[0]

6Bh (6Ah) (R/W) WRAP TO SECTOR 1	6Ch (6Dh) (R/W) REQUEST SECTOR 0	6Dh (6Ch) (R/W) REQUEST SECTOR 1	6Eh (6Fh) (R/W) STOP SECTOR 0
7 Reserved	7 REQSEC[7]	7 Reserved	7 STOPSEC[7]
6 Reserved	6 REQSEC[6]	6 Reserved	6 STOPSEC[6]
5 Reserved	5 REQSEC[5]	5 Reserved	5 STOPSEC[5]
4 Reserved	4 REQSEC[4]	4 Reserved	4 STOPSEC[4]
3 Reserved	3 REQSEC[3]	3 Reserved	3 STOPSEC[3]
2 Reserved	2 REQSEC[2]	2 Reserved	2 STOPSEC[2]
1 WRAP TO SECTOR[9]	1 REQSEC[1]	1 REQSEC[9]	1 STOPSEC[1]
0 WRAP TO SECTOR[8]	0 REQSEC[0]	0 REQSEC[8]	0 STOPSEC[0]

6Fh (6Eh) (R/W) STOP SECTOR 1	70h (R/W)	71h (R/W)	72h (R/W) R/W VECTOR ADDRESS
7 Reserved	7 Reserved	7 Reserved	7 Reserved
6 Reserved	6 Reserved	6 Reserved	6 Reserved
5 Reserved	5 Reserved	5 Reserved	5 Reserved
4 Reserved	4 Reserved	4 Reserved	4 R/W. Vector Address[4]
3 Reserved	3 Reserved	3 Reserved	3 R/W. Vector Address[3]
2 Reserved	2 Reserved	2 Reserved	2 R/W. Vector Address[2]
1 STOPSEC[9]	1 Reserved	1 Reserved	1 R/W. Vector Address[1]
0 STOPSEC[8]	0 Reserved	0 Reserved	0 R/W. Vector Address[0]

73h (R/W) SEQ. ADDRESS	74h (R/W) FRAME COUNTER 0	75h (R/W) COUNTER TEST	76h (77h) (R/W) INDEX COUNTER 0
7 Seq. Run Control/Status	7 FRAMECTR[7]	7 Test Disk Block Enable	7 INDEXCTR[7]
6 Reserved	6 FRAMECTR[6]	6 Test High Byte Of Cntrs	6 INDEXCTR[6]
5 Reserved	5 FRAMECTR[5]	5 Frame Counter = 0	5 INDEXCTR[5]
4 Seq. Address[4]	4 FRAMECTR[4]	4 Reserved	4 INDEXCTR[4]
3 Seq. Address[3]	3 FRAMECTR[3]	3 CDR Counter = 0	3 INDEXCTR[3]
2 Seq. Address[2]	2 FRAMECTR[2]	2 CDR FIFO Full	2 INDEXCTR[2]
1 Seq. Address[1]	1 FRAMECTR[1]	1 Sync Detect Match Even	1 INDEXCTR[1]
0 Seq. Address[0]	0 FRAMECTR[0]	0 Sync Detect Match Odd	0 INDEXCTR[0]

77h (76h) (R/W) INDEX COUNTER 1	78h (79h) (R/W) CDR FIFO DATA 0	79h (78h) (R/W) CDR FIFO DATA 1	7Ah (7Bh) (R) DISK SEQUENCER COUNTER
7 INDEXCTR[15]	7 CDRDATA[7]	7 CDRDATA[15]	7 Reserved
6 INDEXCTR[14]	6 CDRDATA[6]	6 CDRDATA[14]	6 SEQCTR[6]
5 INDEXCTR[13]	5 CDRDATA[5]	5 CDRDATA[13]	5 SEQCTR[5]
4 INDEXCTR[12]	4 CDRDATA[4]	4 CDRDATA[12]	4 SEQCTR[4]
3 INDEXCTR[11]	3 CDRDATA[3]	3 CDRDATA[11]	3 SEQCTR[3]
2 INDEXCTR[10]	2 CDRDATA[2]	2 CDRDATA[10]	2 SEQCTR[2]
1 INDEXCTR[9]	1 CDRDATA[1]	1 CDRDATA[9]	1 SEQCTR[1]
0 INDEXCTR[8]	0 CDRDATA[0]	0 CDRDATA[8]	0 SEQCTR[0]

7Bh (7Ah) (R) DISK MODULO 64 COUNTER	7Dh (R) DISK FIFO STATUS	7Eh (R/W) DISK AUTO STOP CNTRL	80h (81h) (W) ECC SEED 2
7 Reserved	7 Disk FIFO Error	7 Stop On Unc. ECC Error	7 SEED[23]
6 Reserved	6 Reserved	6 Stop On INPUT	6 SEED[22]
5 MOD64CTR[5]	5 DFCNT[5]	5 Stop On Disk/Buffer Error	5 SEED[21]
4 MOD64CTR[4]	4 DFCNT[4]	4 Stop On Index	4 SEED[20]
3 MOD64CTR[3]	3 DFCNT[3]	3 Stop On Corrected ECC	3 SEED[19]
2 MOD64CTR[2]	2 DFCNT[2]	2 Stop On Sector Boundary	2 SEED[18]
1 MOD64CTR[1]	1 DFCNT[1]	1 Stop On Buffer Not Ready	1 SEED[17]
0 MOD64CTR[0]	0 DFCNT[0]	0 Stop On 2-Index Timeout	0 SEED[16]

81h (80h) (W) ECC SEED 3	83h (82h) (W) ECC SEED 1	84h (85h) (R) CORRECTED SEED FIFO 0	85h (84h) (R) CORRECTED SEED FIFO 1
7 SEED[31]	7 SEED[15]	7 CSEED[7]	7 Corrected Seed Valid
6 SEED[30]	6 SEED[14]	6 CSEED[6]	6 Reserved
5 SEED[29]	5 SEED[13]	5 CSEED[5]	5 Reserved
4 SEED[28]	4 SEED[12]	4 CSEED[4]	4 Reserved
3 SEED[27]	3 SEED[11]	3 CSEED[3]	3 Reserved
2 SEED[26]	2 SEED[10]	2 CSEED[2]	2 Reserved
1 SEED[25]	1 Reserved	1 CSEED[1]	1 CSEED[9]
0 SEED[24]	0 Reserved	0 CSEED[0]	0 CSEED[8]

3.3 ECC Control Registers

Addresses in parentheses indicate register mapping in Motorola Mode.

94h (R/W)	95h (R/W)	96h (R/W) ECC ERROR LOG THRESHOLD	97h (R) ECC ERROR LOG COUNTER
7 Reserved	7 Reserved	7 Reserved	7 Reserved
6 Reserved	6 Reserved	6 Reserved	6 Reserved
5 Reserved	5 Reserved	5 Reserved	5 Reserved
4 Reserved	4 Reserved	4 Reserved	4 Reserved
3 Reserved	3 Reserved	3 ELTH[3]	3 ELOGCTR[3]
2 Reserved	2 Reserved	2 ELTH[2]	2 ELOGCTR[2]
1 Reserved	1 Reserved	1 ELTH[1]	1 ELOGCTR[1]
0 Reserved	0 Reserved	0 ELTH[0]	0 ELOGCTR[0]

98h (R/W) ECC CONFIGURATION 0	99h (R) ECC CONFIGURATION 1	9Ah (R/W) ECC INTERNAL ADR. CNTR	9Bh (R/W) ECC CONTROL
7 Disable Addr. Cntr. Incr.	7 Reserved	7 Reserved	7 Reserved
6 Early Warning Thresh.[1]	6 Reserved	6 Reserved	6 Reserved
5 Early Warning Thresh.[0]	5 Reserved	5 Reserved	5 Error Threshold Exceeded
4 Correction Threshold[1]	4 Reserved	4 Reserved	4 Seed Error
3 Correction Threshold[0]	3 Reserved	3 ECCADDCTR[3]	3 Reset ECC Block
2 Reserved	2 Reserved	2 ECCADDCTR[2]	2 Rotate Current Interleave
1 Reserved	1 Reserved	1 ECCADDCTR[1]	1 Reset Corr. State Machine
0 Reserved	0 Reserved	0 ECCADDCTR[0]	0 Initialize LFSR

9Ch (R) ECC STATUS 0	9Dh (R) ECC STATUS 1	9Eh (9Fh) (R) ECC INDIRECT DATA
7 Current Sector In Error	7 Current Interleave No.[1]	7 ECCIDATA[7]
6 Correction Overrun	6 Current Interleave No.[0]	6 ECCIDATA[6]
5 ECC Busy	5 Reserved	5 ECCIDATA[5]
4 Uncorrectable ECC Error	4 Early Inter. Warning Error	4 ECCIDATA[4]
3 Data Compare Not Equal	3 No. Errors In Interleave[1]	3 ECCIDATA[3]
2 Interleave Byte Diff[2]	2 No. Errors In Interleave[0]	2 ECCIDATA[2]
1 Interleave Byte Diff[1]	1 Software Correction Req.	1 ECCIDATA[1]
0 Interleave Byte Diff[0]	0 HW Correctable Error	0 ECCIDATA[0]

3.3.1 ECC Indirect Data Registers

The following registers are the locations that are available to the microprocessor to read in order to perform software ECC correction.

ECCADDCTR[3:0] (reg. 9Ah, R/W)				Indirect Data Registers - ECCIDATA[7:0]
[3]	[2]	[1]	[0]	(regs. 9Eh/9Fh, R)
0	0	0	0	Syndrome SN3[7:0]
0	0	0	1	Syndrome SN2[7:0]
0	0	1	0	Syndrome SN1[7:0]
0	0	1	1	Syndrome S0[7:0]
0	1	0	0	Syndrome S1[7:0]
0	1	0	1	Syndrome S2[7:0]
0	1	1	0	Syndrome S3[7:0]
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Error Pattern_0[7:0]
1	0	1	1	Error Location_0[7:0]
1	1	0	0	Error Pattern_1[7:0]
1	1	0	1	Error Location_1[7:0]
1	1	1	0	Error Pattern_2[7:0]
1	1	1	1	Error Location_2[7:0]

3.4 Host Control Registers

Addresses in parentheses indicate register mapping in Motorola Mode.

A0h (R/W) MICRO. AT ERROR	A1h (R/W) MICRO. AT FEATURES	A2h (R/W) MICRO. AT SECTOR COUNT	A3h (R/W) MICRO. AT SECTOR NUM.
7 Bad Block Detected	7 M_FEATRS[7]	7 M_SECCNT[7]	7 M_SECNUM[7]
6 Uncorr. Data Error	6 M_FEATRS[6]	6 M_SECCNT[6]	6 M_SECNUM[6]
5 Media Changed	5 M_FEATRS[5]	5 M_SECCNT[5]	5 M_SECNUM[5]
4 ID Not Found	4 M_FEATRS[4]	4 M_SECCNT[4]	4 M_SECNUM[4]
3 Media Change Requested	3 M_FEATRS[3]	3 M_SECCNT[3]	3 M_SECNUM[3]
2 Abort	2 M_FEATRS[2]	2 M_SECCNT[2]	2 M_SECNUM[2]
1 Track 0 Not Found	1 M_FEATRS[1]	1 M_SECCNT[1]	1 M_SECNUM[1]
0 Address Mark Not Found	0 M_FEATRS[0]	0 M_SECCNT[0]	0 M_SECNUM[0]

A4h (A5h) (R/W) MICRO. AT CYL. LOW	A5h (A4h) (R/W) MICRO. AT CYL. HIGH	A6h (R/W) MICRO. AT DRIVE/HEAD	A7h (R/W) MICRO. AT COMMAND
7 M_CYL[7]	7 M_CYL[15]	7 M_Pass Thru[2]/1	7 M_CMD[7]
6 M_CYL[6]	6 M_CYL[14]	6 M_Pass Thru[1]/LBA	6 M_CMD[6]
5 M_CYL[5]	5 M_CYL[13]	5 M_Pass Thru[0]/1	5 M_CMD[5]
4 M_CYL[4]	4 M_CYL[12]	4 M_Drive Number Select	4 M_CMD[4]
3 M_CYL[3]	3 M_CYL[11]	3 M_Head Select[3]	3 M_CMD[3]
2 M_CYL[2]	2 M_CYL[10]	2 M_Head Select[2]	2 M_CMD[2]
1 M_CYL[1]	1 M_CYL[9]	1 M_Head Select[1]	1 M_CMD[1]
0 M_CYL[0]	0 M_CYL[8]	0 M_Head Select[0]	0 M_CMD[0]

A8h (R) SECTOR COUNT IMAGE	A9h (R) SECTOR NUMBER IMAGE	AAh (ABh) (R) CYLINDER LOW IMAGE	ABh (AAh) (R) CYLINDER HIGH IMAGE
7 I_SECCNT[7]	7 I_SECNUM[7]	7 I_CYL[7]	7 I_CYL[15]
6 I_SECCNT[6]	6 I_SECNUM[6]	6 I_CYL[6]	6 I_CYL[14]
5 I_SECCNT[5]	5 I_SECNUM[5]	5 I_CYL[5]	5 I_CYL[13]
4 I_SECCNT[4]	4 I_SECNUM[4]	4 I_CYL[4]	4 I_CYL[12]
3 I_SECCNT[3]	3 I_SECNUM[3]	3 I_CYL[3]	3 I_CYL[11]
2 I_SECCNT[2]	2 I_SECNUM[2]	2 I_CYL[2]	2 I_CYL[10]
1 I_SECCNT[1]	1 I_SECNUM[1]	1 I_CYL[1]	1 I_CYL[9]
0 I_SECCNT[0]	0 I_SECNUM[0]	0 I_CYL[0]	0 I_CYL[8]

ACh (R) DRIVE/HEAD IMAGE	ADh (R/W) START SECTOR NUMBER	AEh (AFh) (R/W) START CYLINDER LOW	AFh (AEh) (R/W) START CYLINDER HIGH
7 I_Pass Thru[2]/1	7 ST_SECNUM[7]	7 ST_CYL[7]	7 ST_CYL[15]
6 I_Pass Thru[1]/LBA MODE	6 ST_SECNUM[6]	6 ST_CYL[6]	6 ST_CYL[14]
5 I_Pass Thru[0]/1	5 ST_SECNUM[5]	5 ST_CYL[5]	5 ST_CYL[13]
4 I_Drive Number Select	4 ST_SECNUM[4]	4 ST_CYL[4]	4 ST_CYL[12]
3 I_Head Select[3]	3 ST_SECNUM[3]	3 ST_CYL[3]	3 ST_CYL[11]
2 I_Head Select[2]	2 ST_SECNUM[2]	2 ST_CYL[2]	2 ST_CYL[10]
1 I_Head Select[1]	1 ST_SECNUM[1]	1 ST_CYL[1]	1 ST_CYL[9]
0 I_Head Select[0]	0 ST_SECNUM[0]	0 ST_CYL[0]	0 ST_CYL[8]

B0h (R/W) START DRIVE/HEAD	B1h (R/W) MAX SECTOR NUMBER 0	B2h (R/W) MAX SECTOR NUMBER 1	B3h (R/W) MAX HEAD NUMBER
7 ST_Pass Thru[2]/1	7 MAXSEC_0[7]	7 MAXSEC_1[7]	7 MAXHEAD_1[3]
6 ST_Pass Thru[1]/LBA	6 MAXSEC_0[6]	6 MAXSEC_1[6]	6 MAXHEAD_1[2]
5 ST_Pass Thru[0]/1	5 MAXSEC_0[5]	5 MAXSEC_1[5]	5 MAXHEAD_1[1]
4 ST_Drive Number Select	4 MAXSEC_0[4]	4 MAXSEC_1[4]	4 MAXHEAD_1[0]
3 ST_Head Select[3]	3 MAXSEC_0[3]	3 MAXSEC_1[3]	3 MAXHEAD_0[3]
2 ST_Head Select[2]	2 MAXSEC_0[2]	2 MAXSEC_1[2]	2 MAXHEAD_0[2]
1 ST_Head Select[1]	1 MAXSEC_0[1]	1 MAXSEC_1[1]	1 MAXHEAD_0[1]
0 ST_Head Select[0]	0 MAXSEC_0[0]	0 MAXSEC_1[0]	0 MAXHEAD_0[0]

B4h (R/W) DRIVE 0 STATUS	B5h (R/W) DRIVE 1 STATUS	B6h (R/W) HOST BLOCK SIZE	B7h (R) HOST BLOCK COUNTER
7 Reserved	7 Reserved	7 HBLKSIZE[7]	7 HBLKCTR[7]
6 Reserved	6 Reserved	6 HBLKSIZE[6]	6 HBLKCTR[6]
5 Reserved	5 Reserved	5 HBLKSIZE[5]	5 HBLKCTR[5]
4 Reserved	4 Reserved	4 HBLKSIZE[4]	4 HBLKCTR[4]
3 Reserved	3 Reserved	3 HBLKSIZE[3]	3 HBLKCTR[3]
2 Drive 0 Ready	2 Drive 1 Ready	2 HBLKSIZE[2]	2 HBLKCTR[2]
1 Drive 0 Write Fault	1 Drive 1 Write Fault	1 HBLKSIZE[1]	1 HBLKCTR[1]
0 Drive 0 Seek Complete	0 Drive 1 Seek Complete	0 HBLKSIZE[0]	0 HBLKCTR[0]

B8h (R/W)	B9h (R) HOST TIMER	BAh (R/W) HOST BUSY TIME	BBh (R/W) HOST INTERRUPT TIME
7 Reserved	7 HTIMER[7]	7 BSYTIME[7]	7 IRQTIME[7]
6 Reserved	6 HTIMER[6]	6 BSYTIME[6]	6 IRQTIME[6]
5 Reserved	5 HTIMER[5]	5 BSYTIME[5]	5 IRQTIME[5]
4 Reserved	4 HTIMER[4]	4 BSYTIME[4]	4 IRQTIME[4]
3 Reserved	3 HTIMER[3]	3 BSYTIME[3]	3 IRQTIME[3]
2 Reserved	2 HTIMER[2]	2 BSYTIME[2]	2 IRQTIME[2]
1 Reserved	1 HTIMER[1]	1 BSYTIME[1]	1 IRQTIME[1]
0 Reserved	0 HTIMER[0]	0 BSYTIME[0]	0 IRQTIME[0]

BCh (R/W)	BDh (R/W)	BEh (R/W)	BFh (R/W) HOST CONTROL PIN 1
7 Reserved	7 Reserved	7 Reserved	7 Reserved
6 Reserved	6 Reserved	6 Reserved	6 *PDIAG
5 Reserved	5 Reserved	5 Reserved	5 *DASP/*SPKR
4 Reserved	4 Reserved	4 Reserved	4 Reserved
3 Reserved	3 Reserved	3 Reserved	3 Reserved
2 Reserved	2 Reserved	2 Reserved	2 Reserved
1 Reserved	1 Reserved	1 Reserved	1 Reserved
0 Reserved	0 Reserved	0 Reserved	0 Reserved

C0h (R/W) HOST CONTROL 0	C1h (R/W) HOST CONTROL 1	C2h (R/W) HOST CONTROL 2	C3h (R/W) HOST CONTROL 3
7 En. Auto- Local Micro Cmds	7 Set Busy/Internal Busy	7 En. Auto. Multi-Sector XFR	7 Host Write Operation
6 Dis. Auto Cmd Blk Update	6 Reset Busy/BTRANS	6 Enable Auto Write	6 Reserved
5 En. Rd Vrfy Task File Updt	5 Corrected Data	5 Enable Auto Read	5 Enable Auto Error Set
4 Dis. Start Register Update	4 Host Interrupt Request	4 Enable Auto Write DMA	4 En. Auto Pause On Error
3 HCS1 Select	3 Reset IRQ	3 Enable Auto Read DMA	3 Enable LBA Mode
2 Slave Mode	2 One Block Auto Cmd.	2 En. Auto WR Mult.CMDs	2 Start AT Transfer
1 Master/Slave Enable	1 Interrupt Enable Status	1 En. Auto RD Mult. CMDs	1 Restart AT Transfer
0 Reserved	0 Error	0 En. Auto WR Verify/Same	0 Pause Host Transfer

C4h (R/W) HOST CONTROL 4	C5h (R/W) HOST CONTROL 5	C6h (R/W) HOST CONTROL 6	C7h (R/W)
7 Test Cylinder Counter	7 En. IOCS16 Open Drain	7 En. Read Interlock Pause	7 Reserved
6 Select Alternate Timer	6 En. 16-bit Host Data XFER	6 En. Auto Read Interlock	6 Reserved
5 Reserved	5 Reserved	5 Update Host Count	5 Reserved
4 Reserved	4 Enable Auto IRQ	4 En. Ext. DMA HDB Drive	4 Reserved
3 Reserved	3 En. PIO Transfer Mode	3 Host FIFO Reset	3 Reserved
2 Reserved	2 En. Auto. AT Wait States	2 Auto Read Interlock Status	2 Reserved
1 IRQ Mode[1]	1 Reserved	1 En. Demand Mode DMA	1 Reserved
0 IRQ Mode[0]	0 Early IOCHRDY	0 En. Ext. PIO HDB Drive	0 Reserved

C8h (R) HOST INTERRUPT STATUS 0	C8h (W) HOST INTERRUPT CLEAR 0	C9h (R/W) HOST INTERRUPT ENABLE 0	CAh (R) HOST INTERRUPT STATUS 1
7 Host IRQ Time-Out Int.	7 Clr. Host IRQ Time-Out Int.	7 En. Host IRQ Time-Out Int.	7 Reserved
6 Auto Wr Cmd Started Int.	6 Clr. Auto Wr Cmd Start. Int.	6 En. Auto Wr Cmd Start. Int.	6 Reserved
5 Auto Rd Cmd Started Int.	5 Clr. Auto Rd Cmd Start. Int.	5 En. Auto Rd Cmd Start. Int.	5 Reserved
4 Host Reset Detected Int.	4 Clr. Host Reset Det. Int.	4 En. Host Reset Det. Int.	4 Host Cmd. Aborted Int.
3 Host Soft. Reset Det. Int.	3 Clr. Host Soft. Res. Det. Int.	3 En. Host Soft. Res. Det. Int.	3 Auto Write Overrun Int.
2 Sel. Phase Detected Int.	2 Clr. Sel. Phase Det. Int.	2 En. Sel. Phase Det. Int.	2 Host Stat. Rd. Det. Int.
1 Host FIFO Error Int.	1 Clr. Host FIFO Error Int.	1 En. Host FIFO Error Int.	1 Stat. Rd. Det. After XFER
0 Transfer Done Int.	0 Clr. Transfer Done Int.	0 En. Transfer Done Int.	0 Host Transfer Started Int.

CAh (W) HOST INTERRUPT CLEAR 1	CBh (R/W) HOST INTERRUPT ENABLE 1	CCh (R) HOST STATUS 1	CDh (R) HOST STATUS 2
7 Reserved	7 Reserved	7 Rd. Verify Cmd. Rcvd.	7 Reserved
6 Reserved	6 Reserved	6 DRV. Diag. Cmd. Received	6 DMA Cmd. Rcvd.
5 Reserved	5 Reserved	5 Fmt/Buf/Long/Same Cmd	5 Start Head=MAXHEAD
4 Clr. Host Cmd. Aborted Int.	4 En. Host Cmd. Aborted Int.	4 RD/WR Long Cmd. Rcvd.	4 Start Sector=MAXSEC
3 Clr. Auto Write Overrun Int.	3 En. Auto Write Overrun Int.	3 RD/WR Mult. Cmd. Rcvd.	3 Reserved
2 Clr. Host Stat. Rd. Det. Int.	2 En. Host Stat. Rd. Det. Int.	2 Auto DMA Cmd. In Prog.	2 Start DRV/HD=AT DRV/HD
1 Clr. Rd. Det. After XFER Int.	1 En. Rd. Det. After XFER	1 Auto Read Cmd. In Prog.	1 Start Cyl=AT Cyl
0 Clr. Host XFER Started Int.	0 En. Host XFER Started Int.	0 Auto Write Cmd. In. Prog.	0 Start Sector=AT Sector

CEh (R/W) HOST STATUS 3	CFh (R) HOST FIFO STATUS	D0h (D1h) (R) HOST TRANSFER CNT 0	D1h (D0h) (R) HOST TRANSFER COUNT 1
7 AT DRQ (R)	7 Reserved	7 HTC[7]	7 Host ECC Time
6 AT BUSY (R)	6 Reserved	6 HTC[6]	6 Host Transfer Done
5 Host Timer=00h (R)	5 Host FIFO Byte Count[5]	5 HTC[5]	5 Buffer Transfer Done
4 Reserved	4 Host FIFO Byte Count[4]	4 HTC[4]	4 Host ECC Transfer Done
3 SECCNT Loaded With 00h	3 Host FIFO Byte Count[3]	3 HTC[3]	3 Buffer ECC Transfer Done
2 SECCNT=00h (R)	2 Host FIFO Byte Count[2]	2 HTC[2]	2 Transfer Done Status
1 Host Block Ctr.=00h (R)	1 Host FIFO Byte Count[1]	1 HTC[1]	1 HTC[9]
0 "En. AT DRQ" status (R)	0 Host FIFO Byte Count[0]	0 HTC[0]	0 HTC[8]

D2h (R/W) HOST ECC SIZE	D3h (R) HOST ECC COUNT	E0h (R) CONFIGURATION OPTION	E1h (R) CONFIGURATION STATUS
7 Reserved	7 Host/Buffer ECC Time	7 PCMCIA Soft Reset	7 Changed Status
6 Reserved	6 Reserved	6 PCMCIA Level Interrupt	6 En. Changed Status
5 Host ECC Size[5]	5 Host ECC Count[5]	5 Reserved	5 Host Is Only 8 Bit
4 Host ECC Size[4]	4 Host ECC Count[4]	4 Configuration Option Bit 4	4 Configuration Status[4]
3 Host ECC Size[3]	3 Host ECC Count[3]	3 Configuration Index[3]	3 Configuration Status[3]
2 Host ECC Size[2]	2 Host ECC Count[2]	2 Configuration Index[2]	2 Power Down
1 Host ECC Size[1]	1 Host ECC Count[1]	1 Configuration Index[1]	1 ATA Interrupt
0 Host ECC Size[0]	0 Host ECC Count[0]	0 Configuration Index[0]	0 Configuration Status[0]

E2h (R) PINREPLACE	E3h (R) SOCKETCOPY	E4h (R) HOST INTERRUPT STATUS 2	E4h (W) HOST INTERRUPT CLEAR 2
7 BVD1 Change State	7 Reserved	7 Reserved	7 Reserved
6 BVD2 Change State	6 Copy Number[2]	6 Reserved	6 Reserved
5 RDY/*BSY Change State	5 Copy Number[1]	5 CIS Read By Host	5 Clr. CIS Read By Host
4 WPROT Change State]	4 Copy Number[0]	4 Socket & Copy Written	4 Clr. Socket & Copy Written
3 BVD1 Status	3 Socket Number[3]	3 Power Down Bit Changed	3 Clr. Pwr Down Bit Changed
2 BVD2 Status]	2 Socket Number[2]	2 Pin Replacement Written	2 Clr. Pin Replacement Written
1 RDY/*BSY Status	1 Socket Number[1]	1 Config. Status Written	1 Clr. Config. Status Written
0 WPROT Status	0 Socket Number[0]	0 Config. Option Written	0 Clr. Config. Option Written

E5h (R/W) HOST INTERRUPT ENABLE 2	E6h (R/W) PCMCIA MISCELLANEOUS		
7 Reserved	7 Host Reset Signal Status (R)		
6 Reserved	6 Host Interface Mode (R)		
5 En. CISRD Interrupt	5 Reserved		
4 En. SOCKETWR Interrupt	4 Reserved		
3 En. PWRDWNCHG Int.	3 Reserved		
2 En. PINREPWR Interrupt	2 Reserved		
1 En. CONFIGSTWR Int.	1 Host Interface Select[1]		
0 En. CONFIGOPTWR Int.	0 Host Interface Select[0]		

3.5 Buffer Control Registers

Addresses in parentheses indicate register mapping in Motorola Mode.

100h (R/W) BUFFER MODE	101h (W) REFRESH PERIOD	101h (R) REFRESH TIMER	102h (R/W) BUFFER CONTROL 0
7 Buffer Cycle Time Sel.[1]	7 RPERIOD[7]	7 RTIMER[7]	7 Enable Disk Up Counter
6 Buffer Cycle Time Sel.[0]	6 RPERIOD[6]	6 RTIMER[6]	6 Reserved
5 Buffer RAM Select[2]	5 RPERIOD[5]	5 RTIMER[5]	5 Enable Disk No Room Occ.
4 Buffer RAM Select[1]	4 RPERIOD[4]	4 RTIMER[4]	4 Enable Host No Room Occ.
3 Buffer RAM Select[0]	3 RPERIOD[3]	3 RTIMER[3]	3 En. Dsk Rm Logic On Wrap
2 Enable 16-Bit Wide Buffer	2 RPERIOD[2]	2 RTIMER[2]	2 En. 16-Bit Micro/Buf. Acc.
1 Enable High Host Priority	1 RPERIOD[1]	1 RTIMER[1]	1 Disable *MOE/*MCE/*RAS
0 Enable Buffer Pseudo-Read	0 RPERIOD[0]	0 RTIMER[0]	0 Reserved

103h (R) BUFFER INTERRUPT 0	103h (W) BUFF. INTERRUPT CLEAR 0	104h (R/W) BUFF. INTERRUPT ENABLE 0	105h (R/W) BUFFER CONTROL 1
7 Disk Sec. Cntr. Done Int.	7 Clr. Disk Sec. Cntr. Done	7 En. Disk Sec. Cntr. Done	7 Reserved
6 Reserved	6 Reserved	6 Reserved	6 Reserved
5 Disk No Room Occur. Int.	5 Clr. Disk No Room Occur.	5 En. Disk No Room Occur.	5 Reserved
4 Host No Room Occur. Int.	4 Clr. Host No Room Occur.	4 En. Host No Room Occur.	4 Reserved
3 Reserved	3 Reserved	3 Reserved	3 Disable Disk Error Stop
2 Cor. Port Overrun Error Int.	2 Clr. Cor. Port Overrun Error	2 En. Cor. Port Overrun Error	2 Disable Host Error Stop
1 Reserved	1 Reserved	1 Reserved	1 Force Buffer Parity Error
0 Reserved	0 Reserved	0 Reserved	0 En. Buffer Parity Checking

106h (R) BUFFER INTERRUPT 1	106h (W) BUFF. INTERRUPT CLEAR 1	107h (R/W) BUFF. INTERRUPT ENABLE 1	108h (R/W) BUFF. COUNTER CONTROL
7 Reserved	7 Reserved	7 Reserved	7 En. Delayed Block Release
6 Reserved	6 Reserved	6 Reserved	6 Host Byte Counter Clear
5 Host CIS Port Check Error	5 Clr. Host CIS Port Chk Err	5 En. Host CIS Port Chk Err	5 Disk Byte Counter Clear
4 Servo Port Check Error	4 Clr. Servo Port Chk Error	4 En. Servo Port Chk Error	4 Disk Block Counter Clear
3 Micro. Port Check Error	3 Clr. Micro. Port Chk Error	3 En. Micro. Port Chk Error	3 Release Blocks To Host
2 Corr. Port Check Error	2 Clr. Corr. Port Chk Error	2 En. Corr. Port Chk Error	2 Reserved
1 Disk Port Check Error	1 Clr. Disk Port Chk Error	1 En Disk Port Chk Error	1 Reserved
0 Host Port Check Error	0 Clr. Host Port Chk Error	0 En. Host Port Chk Error	0 Buffer Counter Select

109h (R/W) BUFFER PORT ENABLE	10Ah (W) BUFF. COUNTER ADD/SUB	10Bh (R/W) BUFFER STATUS 1	10Ch (R/W)
7 Reserved	7 BCTRAS[7]	7 Disk No Room (R)	7 Reserved
6 Reserved	6 BCTRAS[6]	6 Host No Room (R)	6 Reserved
5 Host CIS Port Enable	5 BCTRAS[5]	5 Reserved	5 Reserved
4 Servo Port Enable	4 BCTRAS[4]	4 Reserved	4 Reserved
3 Micro. Port Enable	3 BCTRAS[3]	3 Reserved	3 Reserved
2 Corr. Port Enable	2 BCTRAS[2]	2 Reserved	2 Reserved
1 Disk Port Enable	1 BCTRAS[1]	1 Reserved	1 Reserved
0 Host Port Enable	0 BCTRAS[0]	0 Auto Write Select	0 Reserved

10Dh (R/W) DISK SEC. COUNTER	10Eh (R) DISK BLOCK COUNTER	10Fh (R/W)	110h (111h) (R/W) MICRO. PAGE 0
7 DISKCTR[7]	7 Reserved	7 Reserved	7 MPAGE[15]
6 DISKCTR[6]	6 DBCTR[6]	6 Reserved	6 MPAGE[14]
5 DISKCTR[5]	5 DBCTR[5]	5 Reserved	5 MPAGE[13]
4 DISKCTR[4]	4 DBCTR[4]	4 Reserved	4 MPAGE[12]
3 DISKCTR[3]	3 DBCTR[3]	3 Reserved	3 MPAGE[11]
2 DISKCTR[2]	2 DBCTR[2]	2 Reserved	2 MPAGE[10]
1 DISKCTR[1]	1 DBCTR[1]	1 Reserved	1 Reserved
0 DISKCTR[0]	0 DBCTR[0]	0 Reserved	0 Reserved

111h (110h) (R/W) MICRO. PAGE 1	112h (113h) (R/W) SERVO PAGE 0	113h (112h) (R/W) SERVO PAGE 1	114h (115h) (R/W) BUFFER CNTR. A BYTE 0
7 Reserved	7 VPAGE[15]	7 Reserved	7 BCTRA[7]
6 Reserved	6 VPAGE[14]	6 Reserved	6 BCTRA[6]
5 MPAGE[21]	5 VPAGE[13]	5 VPAGE[21]	5 BCTRA[5]
4 MPAGE[20]	4 Reserved	4 VPAGE[20]	4 BCTRA[4]
3 MPAGE[19]	3 Reserved	3 VPAGE[19]	3 BCTRA[3]
2 MPAGE[18]	2 Reserved	2 VPAGE[18]	2 BCTRA[2]
1 MPAGE[17]	1 Reserved	1 VPAGE[17]	1 BCTRA[1]
0 MPAGE[16]	0 Reserved	0 VPAGE[16]	0 BCTRA[0]

115h (114h) (R/W) BUFFER CNTR. A BYTE 1	116h (117h) (R/W) MAX BUFF COUNT A BYTE 0	117h (116h) (R/W) MAX BUFF COUNT A BYTE 1	118h (119h) (R/W) BUFFER CNTR. B BYTE 0
7 BCTRA[15]	7 BKMAXA[7]	7 BKMAXA[15]	7 BCTRB[7]
6 BCTRA[14]	6 BKMAXA[6]	6 BKMAXA[14]	6 BCTRB[6]
5 BCTRA[13]	5 BKMAXA[5]	5 BKMAXA[13]	5 BCTRB[5]
4 BCTRA[12]	4 BKMAXA[4]	4 BKMAXA[12]	4 BCTRB[4]
3 BCTRA[11]	3 BKMAXA[3]	3 BKMAXA[11]	3 BCTRB[3]
2 BCTRA[10]	2 BKMAXA[2]	2 BKMAXA[10]	2 BCTRB[2]
1 BCTRA[9]	1 BKMAXA[1]	1 BKMAXA[9]	1 BCTRB[1]
0 BCTRA[8]	0 BKMAXA[0]	0 BKMAXA[8]	0 BCTRB[0]

119h (118h) (R/W) BUFFER CNTR. B BYTE 1	11Ah (11Bh) (R/W) MAX BUFF COUNT B BYTE 0	11Bh (11Ah) (R/W) MAX BUFF COUNT B BYTE 1	11Ch (11Dh) (R/W) SERVO BEGIN OF SEG BYTE 0
7 BCTRB[15]	7 BKMAXB[7]	7 BKMAXB[15]	7 VBOS[7]
6 BCTRB[14]	6 BKMAXB[6]	6 BKMAXB[14]	6 VBOS[6]
5 BCTRB[13]	5 BKMAXB[5]	5 BKMAXB[13]	5 VBOS[5]
4 BCTRB[12]	4 BKMAXB[4]	4 BKMAXB[12]	4 VBOS[4]
3 BCTRB[11]	3 BKMAXB[3]	3 BKMAXB[11]	3 VBOS[3]
2 BCTRB[10]	2 BKMAXB[2]	2 BKMAXB[10]	2 VBOS[2]
1 BCTRB[9]	1 BKMAXB[1]	1 BKMAXB[9]	1 VBOS[1]
0 BCTRB[8]	0 BKMAXB[0]	0 BKMAXB[8]	0 VBOS[0]

11Dh (11Ch) (R/W) SERVO BEGIN OF SEG BYTE 1	11Eh (11Fh) (R/W) SERVO END OF SEG BYTE 0	11Fh (11Eh) (R/W) SERVO END OF SEG BYTE 1	120h (121h) (R/W) SECTOR SIZE BYTE 0
7 Reserved	7 VEOS[7]	7 Reserved	7 SECSIZE[7]
6 Reserved	6 VEOS[6]	6 Reserved	6 SECSIZE[6]
5 Reserved	5 VEOS[5]	5 Reserved	5 SECSIZE[5]
4 VBOS[12]	4 VEOS[4]	4 VEOS[12]	4 SECSIZE[4]
3 VBOS[11]	3 VEOS[3]	3 VEOS[11]	3 SECSIZE[3]
2 VBOS[10]	2 VEOS[2]	2 VEOS[10]	2 SECSIZE[2]
1 VBOS[9]	1 VEOS[1]	1 VEOS[9]	1 SECSIZE[1]
0 VBOS[8]	0 VEOS[0]	0 VEOS[8]	0 SECSIZE[0]

121h (120h) (R/W) SECTOR SIZE BYTE 1	122h (123h) (R/W)	123h (122h) (R/W)	124h (125h) (R) HOST BYTE COUNT BYTE 0
7 Reserved	7 Reserved	7 Reserved	7 HBC[7]
6 Reserved	6 Reserved	6 Reserved	6 HBC[6]
5 Reserved	5 Reserved	5 Reserved	5 HBC[5]
4 Reserved	4 Reserved	4 Reserved	4 HBC[4]
3 Reserved	3 Reserved	3 Reserved	3 HBC[3]
2 SECSIZE[10]	2 Reserved	2 Reserved	2 HBC[2]
1 SECSIZE[9]	1 Reserved	1 Reserved	1 HBC[1]
0 SECSIZE[8]	0 Reserved	0 Reserved	0 HBC[0]

125h (124h) (R) HOST BYTE COUNT BYTE 1	126h (127h) (R) DISK BYTE COUNT BYTE 0	127h (126h) (R) DISK BYTE COUNT BYTE 1	128h (129h) (R/W)
7 Reserved	7 DBC[7]	7 Reserved	7 Reserved
6 Reserved	6 DBC[6]	6 Reserved	6 Reserved
5 Reserved	5 DBC[5]	5 Reserved	5 Reserved
4 Reserved	4 DBC[4]	4 Reserved	4 Reserved
3 Reserved	3 DBC[3]	3 Reserved	3 Reserved
2 HBC[10]	2 DBC[2]	2 DBC[10]	2 Reserved
1 HBC[9]	1 DBC[1]	1 DBC[9]	1 Reserved
0 HBC[8]	0 DBC[0]	0 DBC[8]	0 Reserved

129h (128h) (R/W)	12Ah (12Bh) (R/W)	12Bh (12Ah) (R/W)	12Ch (12Dh) (R/W) SERVO POINTER BYTE 0
7 Reserved	7 Reserved	7 Reserved	7 VP[7]
6 Reserved	6 Reserved	6 Reserved	6 VP[6]
5 Reserved	5 Reserved	5 Reserved	5 VP[5]
4 Reserved	4 Reserved	4 Reserved	4 VP[4]
3 Reserved	3 Reserved	3 Reserved	3 VP[3]
2 Reserved	2 Reserved	2 Reserved	2 VP[2]
1 Reserved	1 Reserved	1 Reserved	1 VP[1]
0 Reserved	0 Reserved	0 Reserved	0 VP[0]

12Dh (12Ch) (R/W) SERVO POINTER BYTE 1	12Eh (12Fh) (R/W) DISK UP COUNTER BYTE 0	12Fh (12Eh) (R/W) DISK UP COUNTER BYTE 1	130h (133h) (R/W) HOST POINTER BYTE 0
7 Reserved	7 DUCTR[7]	7 Reserved	7 HP[7]
6 Reserved	6 DUCTR[6]	6 Reserved	6 HP[6]
5 Reserved	5 DUCTR[5]	5 Reserved	5 HP[5]
4 VP[12]	4 DUCTR[4]	4 Reserved	4 HP[4]
3 VP[11]	3 DUCTR[3]	3 Reserved	3 HP[3]
2 VP[10]	2 DUCTR[2]	2 Reserved	2 HP[2]
1 VP[9]	1 DUCTR[1]	1 DUCTR[9]	1 HP[1]
0 VP[8]	0 DUCTR[0]	0 DUCTR[8]	0 HP[0]

131h (132h) (R/W) HOST POINTER BYTE 1	132h (131h) (R/W) HOST POINTER BYTE 2	133h (130h) (R/W) HOST SEGMENT CONTROL	134h (137h) (R/W) DISK POINTER BYTE 0
7 HP[15]	7 Reserved	7 Auto Write Mode[1]	7 DP[7]
6 HP[14]	6 Reserved	6 Auto Write Mode[0]	6 DP[6]
5 HP[13]	5 HP[21]	5 Auto Write Segment Select	5 DP[5]
4 HP[12]	4 HP[20]	4 Auto Write BCTR Select	4 DP[4]
3 HP[11]	3 HP[19]	3 En. Auto Write Room Logic	3 DP[3]
2 HP[10]	2 HP[18]	2 Host Segment Select	2 DP[2]
1 HP[9]	1 HP[17]	1 Host BCTR Select	1 DP[1]
0 HP[8]	0 HP[16]	0 En. Host Room Logic	0 DP[0]

135h (136h) (R/W) DISK POINTER BYTE 1	136h (135h) (R/W) DISK POINTER BYTE 2	137h (134h) (R/W) DISK SEGMENT CONTROL	138h (13Bh) (R/W) BEGIN OF SEGMENT A BYTE 0
7 DP[15]	7 Reserved	7 Reserved	7 ABOS[7]
6 DP[14]	6 Reserved	6 Reserved	6 ABOS[6]
5 DP[13]	5 DP[21]	5 Reserved	5 ABOS[5]
4 DP[12]	4 DP[20]	4 Reserved	4 ABOS[4]
3 DP[11]	3 DP[19]	3 Reserved	3 ABOS[3]
2 DP[10]	2 DP[18]	2 Disk Segment Select	2 ABOS[2]
1 DP[9]	1 DP[17]	1 Disk BCTR Select	1 ABOS[1]
0 DP[8]	0 DP[16]	0 Enable Disk Room Logic	0 ABOS[0]

139h (13Ah) (R/W) BEGIN OF SEGMENT A BYTE 1	13Ah (139h) (R/W) BEGIN OF SEGMENT A BYTE 2	13Bh (138h) (R/W)	13Ch (13Fh) (R/W) END OF SEGMENT A BYTE 0
7 ABOS[15]	7 Reserved	7 Reserved	7 AEOS[7]
6 ABOS[14]	6 Reserved	6 Reserved	6 AEOS[6]
5 ABOS[13]	5 ABOS[21]	5 Reserved	5 AEOS[5]
4 ABOS[12]	4 ABOS[20]	4 Reserved	4 AEOS[4]
3 ABOS[11]	3 ABOS[19]	3 Reserved	3 AEOS[3]
2 ABOS[10]	2 ABOS[18]	2 Reserved	2 AEOS[2]
1 ABOS[9]	1 ABOS[17]	1 Reserved	1 AEOS[1]
0 ABOS[8]	0 ABOS[16]	0 Reserved	0 AEOS[0]

13Dh (13Eh) (R/W) END OF SEGMENT A BYTE 1	13Eh (13Dh) (R/W) END OF SEGMENT A BYTE 2	13Fh (13Ch) (R/W)	140h (143h) (R/W) BEGIN OF SEGMENT B BYTE 0
7 AEOS[15]	7 Reserved	7 Reserved	7 BBOS[7]
6 AEOS[14]	6 Reserved	6 Reserved	6 BBOS[6]
5 AEOS[13]	5 AEOS[21]	5 Reserved	5 BBOS[5]
4 AEOS[12]	4 AEOS[20]	4 Reserved	4 BBOS[4]
3 AEOS[11]	3 AEOS[19]	3 Reserved	3 BBOS[3]
2 AEOS[10]	2 AEOS[18]	2 Reserved	2 BBOS[2]
1 AEOS[9]	1 AEOS[17]	1 Reserved	1 BBOS[1]
0 AEOS[8]	0 AEOS[16]	0 Reserved	0 BBOS[0]

141h (142h) (R/W) BEGIN OF SEGMENT B BYTE 1	142h (141h) (R/W) BEGIN OF SEGMENT B BYTE 2	143h (140h) (R/W)	144h (147h) (R/W) END OF SEGMENT B BYTE 0
7 BBOS[15]	7 Reserved	7 Reserved	7 BEOS[7]
6 BBOS[14]	6 Reserved	6 Reserved	6 BEOS[6]
5 BBOS[13]	5 BBOS[21]	5 Reserved	5 BEOS[5]
4 BBOS[12]	4 BBOS[20]	4 Reserved	4 BEOS[4]
3 BBOS[11]	3 BBOS[19]	3 Reserved	3 BEOS[3]
2 BBOS[10]	2 BBOS[18]	2 Reserved	2 BEOS[2]
1 BBOS[9]	1 BBOS[17]	1 Reserved	1 BEOS[1]
0 BBOS[8]	0 BBOS[16]	0 Reserved	0 BEOS[0]

145h (146h) (R/W) END OF SEGMENT B BYTE 1	146h (145h) (R/W) END OF SEGMENT B BYTE 2	147h (144h) (R/W)	148h (14Bh) (R/W) WRITE CACHE PTR BYTE 0
7 BEOS[15]	7 Reserved	7 Reserved	7 WCP[7]
6 BEOS[14]	6 Reserved	6 Reserved	6 WCP[6]
5 BEOS[13]	5 BEOS[21]	5 Reserved	5 WCP[5]
4 BEOS[12]	4 BEOS[20]	4 Reserved	4 WCP[4]
3 BEOS[11]	3 BEOS[19]	3 Reserved	3 WCP[3]
2 BEOS[10]	2 BEOS[18]	2 Reserved	2 WCP[2]
1 BEOS[9]	1 BEOS[17]	1 Reserved	1 WCP[1]
0 BEOS[8]	0 BEOS[16]	0 Reserved	0 WCP[0]

149h (14Ah) (R/W) WRITE CACHE PTR BYTE 1	14Ah (149h) (R/W) WRITE CACHE PTR BYTE 2	14Bh (148h) (R/W)	14Ch (14Fh) (R) AUTO WRITE SAVE BYTE 0
7 WCP[15]	7 Reserved	7 Reserved	7 AWSAVE[7]
6 WCP[14]	6 Reserved	6 Reserved	6 AWSAVE[6]
5 WCP[13]	5 WCP[21]	5 Reserved	5 AWSAVE[5]
4 WCP[12]	4 WCP[20]	4 Reserved	4 AWSAVE[4]
3 WCP[11]	3 WCP[19]	3 Reserved	3 AWSAVE[3]
2 WCP[10]	2 WCP[18]	2 Reserved	2 AWSAVE[2]
1 WCP[9]	1 WCP[17]	1 Reserved	1 AWSAVE[1]
0 WCP[8]	0 WCP[16]	0 Reserved	0 AWSAVE[0]

14Dh (14Eh) (R) AUTO WRITE SAVE BYTE 1	14Eh (14Dh) (R) AUTO WRITE SAVE BYTE 2	14Fh (14Ch) (R/W)	150h (153Fh) (R/W)
7 AWSAVE[15]	7 Reserved	7 Reserved	7 Reserved
6 AWSAVE[14]	6 Reserved	6 Reserved	6 Reserved
5 AWSAVE[13]	5 AWSAVE[21]	5 Reserved	5 Reserved
4 AWSAVE[12]	4 AWSAVE[20]	4 Reserved	4 Reserved
3 AWSAVE[11]	3 AWSAVE[19]	3 Reserved	3 Reserved
2 AWSAVE[10]	2 AWSAVE[18]	2 Reserved	2 Reserved
1 AWSAVE[9]	1 AWSAVE[17]	1 Reserved	1 Reserved
0 AWSAVE[8]	0 AWSAVE[16]	0 Reserved	0 Reserved

3.6 Disk Sequencer RAM Registers

200h-21Fh (R/W) SEQ. NEXT ADDR/DATA	240h-25Fh (R/W) SEQUENCER CONTROL	280h-29Fh (R/W) SEQUENCER COUNT	2C0h-2FFh (R/W)
7 BRSEL[2] / SEQDATA[7]	7 NEXTADREN	7 MODCNTEN	7 Reserved
6 BRSEL[1] / SEQDATA[6]	6 SEQCTLA[1]	6 SEQCNT[6]	6 Reserved
5 BRSEL[0] / SEQDATA[5]	5 SEQCTLA[0]	5 SEQCNT[5]	5 Reserved
4 SEQNAD[4] / SEQDATA[4]	4 SEQCTLB[1]	4 SEQCNT[4]	4 Reserved
3 SEQNAD[3] / SEQDATA[3]	3 SEQCTLB[0]	3 SEQCNT[3]	3 Reserved
2 SEQNAD[2] / SEQDATA[2]	2 SEQCTLC[2]	2 SEQCNT[2]	2 Reserved
1 SEQNAD[1] / SEQDATA[1]	1 SEQCTLC[1]	1 SEQCNT[1]	1 Reserved
0 SEQNAD[0] / SEQDATA[0]	0 SEQCTLC[0]	0 SEQCNT[0]	0 Reserved

3.7 PCMCIA Interface Registers

200h (R/W) PCMCIA CONFIG OPTION	202h (R/W) PCMCIA CONFIG STATUS	204h (R/W) PCMCIA PIN REPLACEMENT	206h (R/W) PCMCIA SOCKET COPY
7 PCMCIA Soft Reset	7 Changed Status (R)	7 BVD1 Change State	7 Reserved
6 PCMCIA Level Interrupt	6 En. Changed Status	6 BVD2 Change State	6 Copy Number[2]
5 Reserved	5 Host Is Only 8 Bit	5 RDY/*BSY Change State	5 Copy Number[1]
4 Configuration Option Bit 4	4 Configuration Status[4]	4 WPROT Change State	4 Copy Number[0]
3 Configuration Index[3]	3 Configuration Status[3]	3 BVD1 Status	3 Socket Number[3]
2 Configuration Index[2]	2 Power Down	2 BVD2 Status	2 Socket Number[2]
1 Configuration Index[1]	1 ATA Interrupt (R)	1 RDY/*BSY Status	1 Socket Number[1]
0 Configuration Index[0]	0 Configuration Status[0]	0 WPROT Status	0 Socket Number[0]

3.8 Host Task File Registers (AT Host)

1F0/170h (R/W) AT HOST DATA	1F1/171h (R) AT HOST ERROR	1F1/171h (W) AT HOST FEATURES	1F2/172h (R/W) AT HOST SECTOR COUNT
7 H_DATA[7]	7 Bad Block Detected	7 H_FEATRS[7]	7 H_SECCNT[7]
6 H_DATA[6]	6 Uncorr. Data Error	6 H_FEATRS[6]	6 H_SECCNT[6]
5 H_DATA[5]	5 Media Changed	5 H_FEATRS[5]	5 H_SECCNT[5]
4 H_DATA[4]	4 ID Not Found	4 H_FEATRS[4]	4 H_SECCNT[4]
3 H_DATA[3]	3 Media Change Requested	3 H_FEATRS[3]	3 H_SECCNT[3]
2 H_DATA[2]	2 Abort	2 H_FEATRS[2]	2 H_SECCNT[2]
1 H_DATA[1]	1 Track 0 Not Found	1 H_FEATRS[1]	1 H_SECCNT[1]
0 H_DATA[0]	0 Address Mark Not Found	0 H_FEATRS[0]	0 H_SECCNT[0]

1F3/173h (R/W) AT HOST SECTOR NUMBER	1F4/174h (R/W) AT HOST CYLINDER LOW	1F5/175h (R/W) AT HOST CYLINDER HIGH	1F6/176h (R/W) AT HOST DRIVE/HEAD
7 H_SECNUM[7]	7 H_CYL[7]	7 H_CYL[15]	7 H_Pass Thru[2]/1
6 H_SECNUM[6]	6 H_CYL[6]	6 H_CYL[14]	6 H_Pass Thru[1]/LBA
5 H_SECNUM[5]	5 H_CYL[5]	5 H_CYL[13]	5 H_Pass Thru[0]/1
4 H_SECNUM[4]	4 H_CYL[4]	4 H_CYL[12]	4 H_Drive Number Select
3 H_SECNUM[3]	3 H_CYL[3]	3 H_CYL[11]	3 H_Head Select[3]
2 H_SECNUM[2]	2 H_CYL[2]	2 H_CYL[10]	2 H_Head Select[2]
1 H_SECNUM[1]	1 H_CYL[1]	1 H_CYL[9]	1 H_Head Select[1]
0 H_SECNUM[0]	0 H_CYL[0]	0 H_CYL[8]	0 H_Head Select[0]

1F7/177h (R) AT HOST STATUS	1F7/177h (W) AT HOST COMMAND	3F6/376h (R) AT HOST ALTERNATE STATUS	3F6/376h (W) AT HOST DEVICE CONTROL
7 Busy	7 H_CMD[7]	7 Busy	7 Reserved
6 Drive Ready	6 H_CMD[6]	6 Drive Ready	6 Reserved
5 Drive Write Fault	5 H_CMD[5]	5 Drive Write Fault	5 Reserved
4 Drive Seek Complete	4 H_CMD[4]	4 Drive Seek Complete	4 Reserved
3 Data Request	3 H_CMD[3]	3 Data Request	3 Reserved
2 Corrected Data	2 H_CMD[2]	2 Corrected Data	2 Host Software Reset
1 Index	1 H_CMD[1]	1 Index	1 *Interrupt Enable
0 Error	0 H_CMD[0]	0 Error	0 Reserved

3F7/377h (R) AT HOST DRIVE ADDRESS
7 Reserved
6 Inverted Write Gate
5 *Head Sel[3]
4 *Head Sel[2]
3 *Head Sel[1]
2 *Head Sel[0]
1 *Drive Select 1
0 *Drive Select 0

4.1 Device Control Registers

REGISTER NUMBER	HRST pin 33 (mqfp)	SRST 3F6h bit 2	*POR pin 99 (mqfp)	BUF BLK RESET 50h, bit 1	DISK BLK RESET 50h, bit 2	HOST BLK RESET 50h, bit 0	REGISTER VALUE 7	6	5	4	3	2	1	0
50h			•				0	0	0	0	0	1	1	1
51h			•				0	0	0	0	0	0	0	0
52h, R							X	X	X	X	X	X	X	X
53h			•				0	0	0	0	0	0	0	0
54h, R							X	X	X	X	X	X	X	X
55h			•				0	0	0	0	0	0	0	0

• = register is affected; blank = register not affected.

1 = Bit value set to 1 by reset

0 = Bit value set to 0 by reset

X = Bit is not affected by reset

4.2 Disk Control Registers

REGISTER NUMBER	HRST pin 33 (mqfp)	SRST 3F6h bit 2	*POR pin 99 (mqfp)	BUF BLK RESET 50h, bit 1	DISK BLK RESET 50h, bit 2	HOST BLK RESET 50h, bit 0	REGISTER VALUE 7	6	5	4	3	2	1	0
58h							X	X	X	X	X	X	X	X
59h							X	X	X	X	X	X	X	X
5Ah							X	X	X	X	X	X	X	X
5Bh							X	X	X	X	X	X	X	X
5Ch							X	X	X	X	X	X	X	X
5Dh			•		•		0	X	0	0	0	0	0	0
5Eh			•		•		0	X	X	0	0	X	0	0
5Fh			•		•		0	X	X	0	0	X	0	0
60h			•		•		0	0	0	X	0	0	0	0
61h			•		•		0	0	0	0	0	0	0	0
62h			•		•		0	0	X	0	0	0	0	0
63h			•		•		0	0	0	0	X	0	0	0
64h			•		•		X	0	0	X	X	1	0	X
65h			•		•		X	X	X	X	0	0	0	X
66h			•		•		0	0	0	X	0	0	0	0
67h			•		•		0	0	0	X	0	0	0	0
68h							X	X	X	X	X	X	X	X
69h							X	X	X	X	X	X	X	X
6Ah							X	X	X	X	X	X	X	X
6Bh							X	X	X	X	X	X	X	X
6Ch							X	X	X	X	X	X	X	X
6Dh							X	X	X	X	X	X	X	X
6Eh							X	X	X	X	X	X	X	X
6Fh							X	X	X	X	X	X	X	X
70h							X	X	X	X	X	X	X	X
71h							X	X	X	X	X	X	X	X
72h							X	X	X	X	X	X	X	X
73h, W			•		•		0	X	X	X	X	X	X	X
73h, R			•		•		0	X	X	X	X	X	X	X
74h							X	X	X	X	X	X	X	X
75h			•		•		0	0	X	X	X	X	X	X
76h							X	X	X	X	X	X	X	X
77h							X	X	X	X	X	X	X	X
78h							X	X	X	X	X	X	X	X
79h							X	X	X	X	X	X	X	X
7Ah							X	X	X	X	X	X	X	X
7Bh							X	X	X	X	X	X	X	X
7Ch							X	X	X	X	X	X	X	X
7Dh			•		•		0	X	0	0	0	0	0	0
7Eh			•		•		0	0	0	0	0	0	0	0
7Fh							X	X	X	X	X	X	X	X

NOTE: This table is continued on the following page.

4.2 Disk Control Registers (cont.)

REGISTER NUMBER	HRST pin 33 (mqfp)	SRST 3F6h bit 2	*POR pin 99 (mqfp)	BUF BLK RESET 50h, bit 1	DISK BLK RESET 50h, bit 2	HOST BLK RESET 50h, bit 0	REGISTER VALUE 7	6	5	4	3	2	1	0
80h							X	X	X	X	X	X	X	X
81h							X	X	X	X	X	X	X	X
82h							X	X	X	X	X	X	X	X
83h							X	X	X	X	X	X	X	X
84h							X	X	X	X	X	X	X	X
85h			•		•		0	X	X	X	X	X	X	X
86h-8Fh							X	X	X	X	X	X	X	X

• = register is affected; blank = register not affected.

1 = Bit value set to 1 by reset

0 = Bit value set to 0 by reset

X = Bit is not affected by reset

4.3 ECC Control Registers

REGISTER NUMBER	HRST pin 33 (mqfp)	SRST 3F6h bit 2	*POR pin 99 (mqfp)	BUF BLK RESET 50h, bit 1	DISK BLK RESET 50h, bit 2	HOST BLK RESET 50h, bit 0	REGISTER VALUE 7	6	5	4	3	2	1	0
94h							X	X	X	X	X	X	X	X
95h							X	X	X	X	X	X	X	X
96h			•				0	0	0	0	1	1	1	1
97h			•		•		0	0	0	0	0	0	0	0
98h			•				0	0	0	1	1	0	0	0
99h			•				0	0	0	1	0	1	0	1
9Ah			•				0	0	0	0	0	0	0	0
9Bh			•				0	0	0	0	0	0	0	0
9Ch			•		•		0	0	0	0	0	0	0	0
9Dh			•		•		1	1	0	0	0	0	0	0
9Eh							X	X	X	X	X	X	X	X

• = register is affected; blank = register not affected.

1 = Bit value set to 1 by reset

0 = Bit value set to 0 by reset

X = Bit is not affected by reset

4.4 Host Control Registers

REGISTER NUMBER	HRST pin 33 (mqfp)	SRST 3F6h bit 2	*POR pin 99 (mqfp)	HOST WRITE TO 1F7h	HOST ISSUES DIAG 90	HOST BLK RESET 50h, bit 0	REGISTER VALUE 7	6	5	4	3	2	1	0
A0h	•		•	•		•	0	0	0	0	0	0	0	0
A1h							X	X	X	X	X	X	X	X
A2h							X	X	X	X	X	X	X	X
A3h							X	X	X	X	X	X	X	X
A4h							X	X	X	X	X	X	X	X
A5h							X	X	X	X	X	X	X	X
A6h	•	•	•		•	•	0	0	0	0	0	0	0	0
A7h							X	X	X	X	X	X	X	X
A8h, R							X	X	X	X	X	X	X	X
A9h							X	X	X	X	X	X	X	X
AAh							X	X	X	X	X	X	X	X
ABh							X	X	X	X	X	X	X	X
ACh	•				•		0	0	0	0	0	0	0	0
ADh							X	X	X	X	X	X	X	X
AEh							X	X	X	X	X	X	X	X
AFh							X	X	X	X	X	X	X	X
B0h			•			•	0	0	0	0	0	0	0	0
B1h							X	X	X	X	X	X	X	X
B2h							X	X	X	X	X	X	X	X
B3h							X	X	X	X	X	X	X	X
B4h	•		•			•	X	X	X	0	0	0	0	0
B5h	•		•			•	X	X	X	0	0	0	0	0
B6h							X	X	X	X	X	X	X	X
B7h							X	X	X	X	X	X	X	X
B8h							X	X	X	X	X	X	X	X
B9h							X	X	X	X	X	X	X	X
BAh							X	X	X	X	X	X	X	X
BBh							X	X	X	X	X	X	X	X
BCh							X	X	X	X	X	X	X	X
BDh							X	X	X	X	X	X	X	X
BEh							X	X	X	X	X	X	X	X
BFh, W	•	•	•			•	X	1	1	X	X	X	X	1
BFh, W					•		X	1	X	X	X	X	X	X
BFh, R	•	•	•	•		•	X	X	X	X	X	X	X	X
C0h, R			•			•	0	0	0	0	0	0	0	0
C1h	•	•	•			•	1	0	0	0	X	1	0	0
C1h		•			•		1	0	0	0	X	X	X	0
C1h				•			0	0	0	X	X	X	X	0

NOTE: This table is continued on the following page.

4.4 Host Control Registers (cont.)

REGISTER NUMBER	HRST pin 33 (mqfp)	SRST 3F6h bit 2	*POR pin 99 (mqfp)	HOST WRITE TO 1F7h	HOST ISSUES DIAG 90	HOST BLK RESET 50h, bit 0	REGISTER VALUE 7	6	5	4	3	2	1	0
C2h			•			•	0	0	0	0	0	0	0	0
C3h			•			•	0	0	0	0	0	0	0	0
C4h			•			•	0	0	X	0	0	0	0	0
C5h			•			•	1	0	0	1	1	0	0	0
C6h			•			•	0	0	0	0	0	0	0	0
C7h			•			•	X	X	X	X	X	X	X	X
C8h, R	•	•	•			•	0	0	0	0	0	0	0	0
C8h, R				•			X	X	X	X	X	X	X	0
C9h			•			•	0	0	0	0	0	0	0	0
CAh	•	•	•			•	X	X	X	X	0	0	0	0
CAh				•			X	X	X	X	X	0	0	0
CBh			•			•	0	0	0	0	0	0	0	0
CCh	•	•	•			•	0	0	0	0	0	0	0	0
CDh	•	•	•			•	X	0	X	X	X	X	X	X
CEh	•	•	•		•	•	0	1	0	0	X	X	X	0
CEh				•			0	1	0	0	X	X	X	0
CFh	•	•	•	•		•	0	0	0	0	0	0	0	0
D0h							X	X	X	X	X	X	X	X
D1h							X	X	X	X	X	X	X	X
D2h			•			•	0	0	0	0	0	1	0	0
D3h							X	X	X	X	X	X	X	X
E0h	•	•	•				0	1	0	0	0	0	0	0
E1h	•	•	•				0	0	0	0	0	0	X	0
E2h	•	•	•				0	0	0	0	0	0	X	0
E3h	•	•	•				0	0	0	0	0	0	0	0
E4h			•			•	X	X	0	0	0	0	0	0
E5h			•			•	X	X	0	0	0	0	0	0
E6h			•			•	X	X	X	X	X	X	0	0

• = register is affected; blank = register not affected.

1 = Bit value set to 1 by reset

0 = Bit value set to 0 by reset

X = Bit is not affected by reset

4.4.1 Host Task File Registers (AT Host)

REGISTER NUMBER	HRST pin 33 (mqfp)	SRST 3F6h bit 2	*POR pin 99 (mqfp)	HOST WRITE TO 1F7h	HOST ISSUES DIAG 90	HOST BLK RESET 50h, bit 0	REGISTER VALUE 7	6	5	4	3	2	1	0
1F0/170h							X	X	X	X	X	X	X	X
1F1/171h, W							X	X	X	X	X	X	X	X
1F1/171h, R				•			0	0	0	0	0	0	0	0
1F2/172h							X	X	X	X	X	X	X	X
1F3/173h							X	X	X	X	X	X	X	X
1F4/174h							X	X	X	X	X	X	X	X
1F5/175h							X	X	X	X	X	X	X	X
1F6/176h	•				•		0	0	0	0	0	0	0	0
1F7/177h, W							X	X	X	X	X	X	X	X
1F7/177h, R	•		•			•	1	0	0	0	0	0	X	0
1F7/177h, R		•					1	X	X	X	0	0	X	0
1F7/177h, R				•			0	X	X	X	0	0	X	0
3F6/376h, W	•		•			•	X	X	X	X	1	0	0	0
3F6/376h, R	•		•			•	1	0	0	0	0	0	X	0
3F6/376h, R		•					1	X	X	X	0	0	X	0
3F6/376h, R				•			0	X	X	X	0	0	X	0
3F7/377h, R							Z	1	1	1	1	1	1	0

• = register is affected; blank = register not affected.

1 = Bit value set to 1 by reset

0 = Bit value set to 0 by reset

X = Bit is not affected by reset

4.4.2 PCMCIA Interface Registers

REGISTER NUMBER	HRST pin 33 (mqfp)	SRST 3F6h bit 2	*POR pin 99 (mqfp)	HOST WRITE TO 1F7h	HOST ISSUES DIAG 90	HOST BLK RESET 50h, bit 0	REGISTER VALUE 7	6	5	4	3	2	1	0
200h							0	1	0	0	0	0	0	0
202h	•	•	•				0	0	0	0	0	0	X	0
204h	•	•	•				0	0	0	0	0	0	X	0
206h	•	•	•			•	0	0	0	0	0	0	0	0

• = register is affected; blank = register not affected.

1 = Bit value set to 1 by reset

0 = Bit value set to 0 by reset

X = Bit is not affected by reset

4.5 Buffer Control Registers

REGISTER NUMBER	HRST pin 33 (mqfp)	SRST 3F6h bit 2	*POR pin 99 (mqfp)	BUF BLK RESET 50h, bit 1	DISK BLK RESET 50h, bit 2	HOST BLK RESET 50h, bit 0	REGISTER VALUE 7	6	5	4	3	2	1	0
100h			•				0	0	0	0	0	0	0	0
100h							X	X	X	X	X	X	X	X
101h							X	X	X	X	X	X	X	X
102h			•	•			0	0	0	0	0	0	0	0
103h			•	•			0	0	0	0	0	0	0	0
104h			•	•			0	0	0	0	0	0	0	0
105h			•	•			0	0	0	0	0	0	0	0
106h			•	•			0	0	0	0	0	0	0	0
107h			•	•			0	0	0	0	0	0	0	0
108h			•	•			0	0	0	0	0	0	0	0
109h			•	•			0	0	0	0	0	0	0	0
10Ah							X	X	X	X	X	X	X	X
10Bh			•	•			0	0	0	0	0	0	0	0
10Ch			•	•			0	0	0	0	0	0	0	0
10Dh			•	•			0	0	0	0	0	0	0	0
10Eh			•	•			0	0	0	0	0	0	0	0
10Fh			•	•			0	0	0	0	0	0	0	0
110h							X	X	X	X	X	X	X	X
111h							X	X	X	X	X	X	X	X
112h							X	X	X	X	X	X	X	X
113h							X	X	X	X	X	X	X	X
114h			•	•			0	0	0	0	0	0	0	0
115h			•	•			0	0	0	0	0	0	0	0
116h							X	X	X	X	X	X	X	X
117h							X	X	X	X	X	X	X	X
118h			•	•			0	0	0	0	0	0	0	0
119h			•	•			0	0	0	0	0	0	0	0
11Ah							X	X	X	X	X	X	X	X
11Bh							X	X	X	X	X	X	X	X
11Ch							X	X	X	X	X	X	X	X
11Dh							X	X	X	X	X	X	X	X
11Eh							X	X	X	X	X	X	X	X
11Fh							X	X	X	X	X	X	X	X
120h							X	X	X	X	X	X	X	X
121h							X	X	X	X	X	X	X	X
122h			•	•			0	0	0	0	0	0	0	0
123h			•	•			0	0	0	0	0	0	0	0
124h			•	•			0	0	0	0	0	0	0	0
125h			•	•			0	0	0	0	0	0	0	0
126h			•	•			0	0	0	0	0	0	0	0
127h			•	•			0	0	0	0	0	0	0	0
128h			•	•			0	0	0	0	0	0	0	0
129h			•	•			0	0	0	0	0	0	0	0

NOTE: This table is continued on the following page.

4.5 Buffer Control Registers (cont.)

REGISTER NUMBER	HRST pin 33 (mqfp)	SRST 3F6h bit 2	*POR pin 99 (mqfp)	BUF BLK RESET 50h, bit 1	DISK BLK RESET 50h, bit 2	HOST BLK RESET 50h, bit 0	REGISTER VALUE 7	6	5	4	3	2	1	0
12Ah			•	•			0	0	0	0	0	0	0	0
12Bh			•	•			0	0	0	0	0	0	0	0
12Ch							X	X	X	X	X	X	X	X
12Dh							X	X	X	X	X	X	X	X
12Eh			•	•			0	0	0	0	0	0	0	0
12Fh			•	•			0	0	0	0	0	0	0	0
130h							X	X	X	X	X	X	X	X
131h							X	X	X	X	X	X	X	X
132h							X	X	X	X	X	X	X	X
133h			•	•			0	0	0	0	0	0	0	0
134h							X	X	X	X	X	X	X	X
135h							X	X	X	X	X	X	X	X
136h							X	X	X	X	X	X	X	X
137h			•	•			0	0	0	0	0	0	0	0
138h							X	X	X	X	X	X	X	X
139h							X	X	X	X	X	X	X	X
13Ah							X	X	X	X	X	X	X	X
13Bh			•	•			0	0	0	0	0	0	0	0
13Ch							X	X	X	X	X	X	X	X
13Dh							X	X	X	X	X	X	X	X
13Eh							X	X	X	X	X	X	X	X
13Fh			•	•			0	0	0	0	0	0	0	0
140h							X	X	X	X	X	X	X	X
141h							X	X	X	X	X	X	X	X
142h							X	X	X	X	X	X	X	X
143h			•	•			0	0	0	0	0	0	0	0
144h							X	X	X	X	X	X	X	X
145h							X	X	X	X	X	X	X	X
146h							X	X	X	X	X	X	X	X
147h			•	•			0	0	0	0	0	0	0	0
148h							X	X	X	X	X	X	X	X
149h							X	X	X	X	X	X	X	X
14Ah							X	X	X	X	X	X	X	X
14Bh			•	•			0	0	0	0	0	0	0	0
14Ch							X	X	X	X	X	X	X	X
14Dh							X	X	X	X	X	X	X	X
14Eh							X	X	X	X	X	X	X	X
14Fh			•	•			0	0	0	0	0	0	0	0

• = register is affected; blank = register not affected.

1 = Bit value set to 1 by reset

0 = Bit value set to 0 by reset

X = Bit is not affected by reset

5.1 Device Control Register Descriptions

50 CHIP RESET/POWER-DOWN CONTROL REGISTER (50h, R/W, CRPCTL)

7 (R/W) (IDDQTST) - DISABLE ALL PULL-UPS: When set, this bit disables the internal pull-up resistors for all signal pins that use pull-up resistors.

6 (R/W) Reserved

5 (R/W) (DBLKPDN_EN) - DISK BLOCK POWER-DOWN ENABLE: When set, this bit allows the Disk block to turn off clocks to circuits that do not require them at the current time. The clocks are automatically enabled as needed. When this bit is reset, the Disk Control block is powered up and various internal disk related circuits are clocking as required. This bit is internally synchronized so that the internal clock does not glitch when being powered up or down.

4 (R/W) (BBLKPDN_EN) - BUFFER BLOCK POWER-DOWN ENABLE: When set, this bit allows the Buffer block to turn off clocks to circuits that do not require them at the current time (except for the DRAM refresh logic, which is powered down via the RAM Select bits RAMSEL[2:0], reg. 100h, R/W, bits 5-3). The clocks are automatically enabled as needed. When this bit is reset, the Buffer Control block is powered up and various internal buffer related circuits are clocking as required. This bit is internally synchronized so that the internal clock does not glitch when being powered up or down.

3 (R/W) (HBLKPDN_EN) - HOST BLOCK POWER-DOWN ENABLE: When set, this bit allows the Host block to turn off clocks to circuits that do not require them at the current time. The clocks are automatically enabled as needed. When this bit is reset, the Host block is powered up and various internal host related circuits are clocking as required.

2 (R/W) (DBLKRST) - DISK BLOCK RESET: When this bit is set, the Disk Control block and the ECC block are initialized to their reset state. This bit is latched to a 1 by the occurrence of Power-On Reset (*POR), and it remains latched until a 0 is written to it.

1 (R/W) (BBLKRST) - BUFFER BLOCK RESET: When this bit is set, the Buffer Control block is initialized to its reset state. This bit is latched to a 1 by the occurrence of Power-On Reset (*POR), and it remains latched until a 0 is written to it.

0 (R/W) (HBLKRST) - HOST BLOCK RESET: When this bit is set, the Host block is initialized to its reset state. This bit is latched to a 1 by the occurrence of Power-On Reset (*POR), and it remains latched until a 0 is written to it.

51 CHIP MODE REGISTER (51h, R/W, CMODE)

7 (R/W) (HADSBLPU) - DISABLE HOST ADDRESS PULL-UPS: When set, this bit disables the internal pull-up resistors for the HA[2:0] input pins.

6 (R/W) (HCDSBLPU) - DISABLE HOST CONTROL PULL-UPS: When set, this bit disables the internal pull-up resistors for the Host control (*PDIAG and *DASP) I/O pins.

5 (R/W) (SWAPREG) - SWAP REGISTER ADDRESSES: When this bit is set, certain two and three byte registers that are accessible by the microprocessor will have their addresses swapped so that the MSB will have a lower address than the LSB. This is useful for word access using Motorola type microprocessors. When this bit is reset, the LSB will have a lower address than the MSB, which is useful for word access using Intel type microprocessors.

4 (R/W) (BDDSBLPU) - DISABLE BUFFER DATA BUS PULL-UPS: When set, this bit disables the internal pull-up resistors for the BD[15:0] signal pins.

3 (R/W) (ENPPRDY) - ENABLE PUSH-PULL READY: When set, this bit configures the READY pin for push-pull operation. When cleared, the READY pin operates in open drain mode.

2 (R/W) (COMBINT) - COMBINE ALL INTERRUPTS: When set allows the disk interrupts to be OR'd into the INTHBD pin. When cleared, the disk interrupts create an interrupt only on the INTD pin.

1 (R/W) (ENPPINT) - ENABLE PUSH-PULL INTERRUPT OUTPUTS: When set, this bit configures the INTHBD and INTD signal pins as push-pull signals. When cleared, INTHBD and INTD are configured in the open drain mode.

0 (R/W) (ACTHIINT) - ENABLE ACTIVE HIGH INTERRUPT OUTPUTS: When this bit is set, the INTHBD and INTD interrupt signals to the microprocessor will be active high. When this bit is reset, INTHBD and INTD will be active low.

52 CHIP STATUS (52h, R, CSTAT)

7 (R) (BUSYMA) - BUSY FOR MICROPROCESSOR ACCESS: This bit is set whenever the AIC-8375 is busy completing a previous microprocessor access to the buffer RAM or a synchronous write or read register. When the READY signal to the microprocessor is not being used, the microprocessor should check this bit after it accesses the buffer RAM or certain synchronous registers to make sure that the access has internally been completed before next access is started. On buffer read accesses, this bit is cleared after data has been latched into the 'register to data bus' latch, i.e., at the negation of *MOE or *RAS.

6:5 (R) (DISKINT[1:0]) - DISK INTERRUPT ACTIVE[1:0]: These two bits reflect the OR'd status of the two Disk Interrupt Status registers. DISKINT[1] will be set as the OR'd condition of any enabled interrupt status bit currently set in the Disk Interrupt 1 Status register (reg. 66h, R). DISKINT[0] will be set as the OR'd condition of any enabled interrupt status bit currently set in the Disk Interrupt 0 Status register (reg. 5Eh, R).

4:3 (R) (BUFINT[1:0]) - BUFFER INTERRUPT ACTIVE[1:0]: These two bits reflect the OR'd status of the two Buffer Interrupt Status registers. BUFINT[1] will be set as the OR'd condition of any enabled interrupt status bit currently set in the Buffer Interrupt 1 Status register (reg. 106h, R). BUFINT[0] will be set as the OR'd condition of any enabled interrupt status bit currently set in the Buffer Interrupt 0 Status register (reg. 103h, R).

2:0 (R) (HOSTINT[2:0]) - HOST INTERRUPT ACTIVE[2:0]: These three bits reflect the OR'd status of the three Host Interrupt Status registers. HOSTINT[2] will be set as the OR'd condition of any enabled interrupt status bit currently set in the Host Interrupt 2 Status register (reg. E4h, R). HOSTINT[1] and HOSTINT[0] apply in an identical fashion to the Host Interrupt 1 Status (reg. CAh, R) and the Host Interrupt 0 Status registers (reg. C8h, R) respectively.

53 CHIP INTERRUPT ENABLE (53h, R/W, CINTEN)

7 (R/W) Reserved

6:5 (R/W) (EN_DISKINT[1:0]) - ENABLE DISK INTERRUPT[1:0]: These two bits enable either one or both of the Disk Interrupt Active bits (reg. 52h, R, bits 6:5) to generate an interrupt to the local microprocesor via the INTD pin (and possibly the INTHB pin - see reg. 51h, R/W, bit 2). EN_DISKINT[1] will enable DISKINT[1] (reg. 52h, R, bit 6) to generate an interrupt. EN_DISKINT[0] will enable DISKINT[0] (reg. 52h, R, bit 5) to generate an interrupt.

4:3 (R/W) (EN_BUFINT[1:0]) - ENABLE BUFFER INTERRUPT[1:0]: These two bits enable either one or both of the Buffer Interrupt Active bits (reg. 52h, R, bits 4:3) to generate an interrupt to the local microprocesor via the INTHBD pin. EN_BUFINT[1] will enable BUFINT[1] (reg. 52h, R, bit 4) to generate an interrupt. EN_BUFINT[0] will enable BUFINT[0] (reg. 52h, R, bit 3) to generate an interrupt.

2:0 (R/W) (EN_HOSTINT[2:0]) - ENABLE HOST INTERRUPT[2:0]: These three bits enable the corresponding Host Interrupt Active bits (reg. 52h, R, bits 2:0) to generate an interrupt to the local microprocesor via the INTHBD pin. EN_HOSTINT[2] will enable HOSTINT[2] (reg. 52h, R, bit 2) to generate an interrupt. EN_HOSTINT[1] and ENHOSTINT[0] enable HOSTINT[1] and HOSTINT[0] to generate interrupts in a similar fashion.

54 CHIP REVISION REGISTER (54h, R, CREV)

7:0 (R) (REVNUM) - PART REVISION NUMBER: The value in this register reflects the revision status of the AIC-8375. The revision number for the AIC-8375 is '00h'. The number will be incremented by '1h' for any subsequent revisions of the device.

55 CHIP TEST REGISTER (55h, R/W, CTEST)

The bits in this register are intended only for manufacturing test of the AIC-8375 device.

7 (R/W) (DHIZ) - DISK INTERFACE HIGH IMPEDANCE MODE: When this bit is set, all of the Disk Interface output signals will be forced to the high-impedance state.

6 (R/W) (BHIZ) - BUFFER INTERFACE HIGH IMPEDANCE MODE: When this bit is set, all of the Buffer Interface output signals will be forced to the high-impedance state.

5 (R/W) (HHIZ) - HOST INTERFACE HIGH IMPEDANCE MODE: When this bit is set, all of the Host Interface output signals will be forced to the high-impedance state.

4 (R/W) (VTHTEST) - INPUT THRESHOLD VOLTAGE TEST: When this bit is set, all of the bi-directional pins of the AIC-8375 will be forced into a high impedance state. The INTD pin will become the output from the VTH test NAND chain whose inputs are driven by all the input and bi-directional pins (except *POR).

3 (R/W) (VOTEST) - OUTPUT VOLTAGE TEST: When this bit is set, all of the output and bi-directional pins will be configured as outputs. The output level is determined by one or more user selected input pins.

2:0 (R/W) (TESTMODE[2:0]) - STANDALONE TEST MODE SELECT[2:0]: For manufacturing use only. These bits should be left at '0' for normal operation.

5.2 Disk Block Register Descriptions

58 EOS COUNTER (58h, R/W, EOSCTR)

7:0 (R/W) (EOSCTR[7:0]) - END OF SERVO COUNTER: This 8-bit counter is loaded with the current Frame Number. This counter increments every EOS pulse and wraps to 00h on the EOS pulse when its value equals the contents of the EOS Maximum register (reg. 59h, R/W). When ENIDXEOS=1 (reg. 5Dh, R/W, bit 1) this counter is reset to 00h if the INDEX pin is asserted. This counter cannot be loaded at the same time as EOS or the INDEX pulse. The CURRSEC registers (regs. 5Ah, 5Bh, R/W) wrap to 000h whenever the EOSCTR wraps/ resets to 00h, but only if the EOSCTR passed the EOS Compare (EOSCMP, reg. 5Ch, R/W) value while the Disk Sequencer was running.

59 EOS MAXIMUM REGISTER (59h, R/W, EOSMAX)

7:0 (R/W) (EOSMAX[7:0]) - END OF SERVO MAXIMUM VALUE: This 8-bit register is loaded with the Maximum Frame Number during ESDA Mode. This register is compared to the contents of the EOS Counter (EOSCTR, reg. 58h, R/W) and when it is equal the EOSCTR wraps to 00h if the EOS pin is asserted. The CURRSEC registers (regs. 5Ah, 5Bh, R/W) wrap to 000h on the EOS pulse while the EOSCTR=EOSMAX if the EOSCTR passed the EOS Compare (EOSCMP, reg. 5Ch, R/W) value while the Disk Sequencer was running.

5A CURRENT SECTOR REGISTER 0 (5Ah (5Bh), R/W, CURRSEC0)

7:0 (R/W) (CURRSEC[7:0]) - CURRENT SECTOR NUMBER[7:0]: This register is the low byte of the Current Sector Number Register. This register address is swapped with CURRSEC1 if SWAPREG=1 (reg. 51h, R/W, bit 5).

The CURRSEC Register is used to define the actual position of the Head during Enhanced Data Sector Headerless (EDSA) Mode. This register is compared to the Request Sector Number register (REQSEC, reg. 6Ch/6Dh, R/W), and when they are equal the CURRSECEQ status bit (reg. 5Bh, R/W, bit 7) is asserted for use by the Sequencer branch instructions. This register resets to 000h when the EOS Counter (EOSCTR, reg. 58h, R/W) equals the contents EOS Maximum register (EOSMAX, reg. 59h, R/W) and the EOS pulse is asserted, but only if the EOSCTR has passed the EOSCMP while the Disk Sequencer is running. If ENIDXEOS=1 (reg. 5Dh, R/W, bit 1) the CURRSEC resets to 000h when the INDEX pin asserted if the EOSCTR has passed the EOSCMP while the Disk Sequencer is running.

5B CURRENT SECTOR REGISTER 1 (5Bh (5Ah), R/W, CURRSEC1)

7 (R) (CURRSECEQ) - CURRENT SECTOR EQUALS REQUEST SECTOR: This ***read only*** bit is asserted when the CURRSEC (reg. 5Ah/5Bh, R/W) equals the contents of the Request Sector Number registers (REQSEC, reg. 6Ch/6Dh, R/W).

6 (R) (EOSCMPEQ) - EOS COUNTER EQUALS EOS COMPARE: This ***read only*** bit is asserted when the EOS Counter (reg. 58h, R/W) equals the contents of the EOS Compare register (reg. 5Ch, R/W).

5 (R) (EOSMAXEQ) - EOS COUNTER EQUALS EOS MAXIMUM: This ***read only*** bit is asserted when the EOS Counter (reg. 58h, R/W) equals the contents of the EOS Maximum Value register (reg. 59h, R/W).

4 (R) (WRAPSECEQ) - REQUEST SECTOR EQUALS WRAP SECTOR: This ***read only*** bit is set when the Wrap Sector Number registers (WRAPSEC, regs. 68h/69h, R/W) equal the contents of the Request Sector Number registers (REQSEC, regs. 6Ch/6Dh, R/W).

3:2 (R/W) Reserved

1:0 (R/W) (CURRSEC[9:8]) - CURRENT SECTOR NUMBER[9:8]: These bits are the two most significant bits of the Current Sector Number Register. (See CURRSEC0 register definition.) This register address is swapped with CURRSEC0 if SWAPREG=1 (reg. 51h, R/W, bit 5).

5C EOS COMPARE REGISTER (5Ch, R/W, EOSCMP)

7:0 (R/W) (EOSCMP[7:0]) - END OF SERVO COMPARE: This 8-bit register is loaded with the Target Frame Number minus 1 during EDSA Mode. It is compared to the contents of the EOS Counter Register (reg. 58h, R/W) and when it is equal and the EOS pin is asserted the EOSCMPEQ status bit (reg. 5Bh, R/W, bit 6) is asserted for use by the Sequencer branch instructions.

5D DISK CONTROL 4 REGISTER (5Dh, R/W, DCTL4)

7 (R/W) Reserved

6 (R/W) (STPSEEDOVR) - STOP ON SEED OVERRUN: When this bit is set the Disk Sequencer will stop when the Corrected Seed FIFO overruns, i.e. more than two hardware corrected Sectors have passed without the Local MPU reading Corrected Seed FIFO (CSEED1/0, regs. 85h, 84h, R).

5 (R/W) (STPAUTOWR) - STOP ON AUTO WRITE: When this bit is set the Disk Sequencer will stop when the Host receives an Auto Write Command.

4 (R/W) (ENSEED) - ENABLE SEED: When this bit is set the SEED function is enabled. When ENSEED=1 the INITECC decode (SEQCTLC=100b) is selected to initiate the Seed transfer to the EDAC and initialize the EDAC. The INITDATA decode (SEQCTLC=011b) is used to signal when to write the Sync Byte(s). When ENSEED=0 INITECC is disabled and INIDATA initializes the EDAC. The CSEED FIFO (CSEED0/1, regs. 84h/85h, R) is reset when ENSEED=0.

3 (R/W) (STPCDRPERR) - STOP ON CDR PARITY ERROR: When this bit is set the Disk Sequencer will stop when the CDRPARERR status (reg. 64h, R/W, bit 6) is set.

2 (R/W) (STPSEEDERR) - STOP ON SEED ERROR: When this bit is set the Disk Sequencer will stop when the SEEDERR (reg. 9Bh, R/W, bit 4) is detected by the EDAC. Regardless of the state of this bit when an ECC Seed Error is detected, the Sector just read is not released in the Buffer Memory even if there is no ECC Error or there is a Correctable ECC Error.

1 (R/W) (ENIDXEOS) - ENABLE CLEAR EOS COUNTER ON INDEX: When this bit is set the EOS Counter (EOSCTR, reg. 58h, R/W) is reset to 00h when the INDEX pin is asserted, otherwise EOSCTR only resets to 00h when it wraps at EOS Maximum (EOSMAX, reg. 59h, R/W). The CURRSEC Register (regs. 5Ah/5Bh, R/W) will reset to 000h when INDEX is asserted, but only if the EOSCTR has previously passed the EOSCMP value (reg. 5Ch, R/W) while the Disk Sequencer was running.

0 (R/W) (ENHANCEDSA) - ENABLE ENHANCED DATA SECTOR HEADERLESS: This bit changes how the CDR Split counts are fetched from the Buffer when ENBUFCDR=1 (reg. 63h, R/W, bit 1), how the CDR FIFO is flushed, and how the CDR Split Counts are loaded from the CDR FIFO to the CDR Counter.

If ENBUFCDR=0 the Local MPU loads the CDR FIFO the same regardless of the setting of this bit. When this bit is set while ENBUFCDR=1 the CDR Split Counts are fetched whenever the CDR FIFO is not full. When this bit is reset while ENBUFCDR=1 a finite number of CDR Split Counts specified by the Disk Sequencer SEQCNT Field are fetched when the Disk Sequencer issues LOADCDR (SEQCTLC=001b).

When this bit is set LOADCDR will flush all CDR Split Counts up to and including the first one with the LASTSPLIT bit set. When this bit is reset LOADCDR resets or flushes the entire CDR FIFO, and then initiates a fetch of a specific number of bytes into the CDR FIFO.

When this bit is reset the CDR Split Counts are transferred from the CDR FIFO to the CDR Counter whenever the Counter is empty and the FIFO is not empty. The counter is empty after reset (Power-On, LOADCDR, or RSTCDR) or when it counts down to 0000h. When this bit is set the CDR Split Counts are transferred the same except it is stopped when a CDR Split Count with LASTSPLIT=1 counts down to 0000h.

5E DISK INTERRUPT STATUS 0 REGISTER (5Eh, R, DISKINT0)

The status bits in this register get set and remain set when the corresponding status condition occurs. Each bit can be cleared by writing a 1 to the corresponding bit in the Disk Interrupt Clear 0 register (reg. 5Eh, W). Writing a 0 has no affect. Also, each status bit can be enabled to generate an interrupt via the corresponding interrupt mask bit in the Disk Interrupt Enable 0 register (DISKINTEN0, reg. 5Fh, R/W) and by setting EN_DISKINT0 (reg. 53h, R/W, bit 5).

7 (R) (SRVOVRN) - SERVO OVERRUN: This bit is set whenever the Servo fetch logic did not transfer the Servo information from Buffer to CDR FIFO before the next Data Field Sync (except the last one if all requested CDR splits have been fetched from the Buffer). It is also set if the Disk Sequencer times out in the "Wait for Defect Flag" instruction. When this bit is set the Sequencer will immediately halt.

6 (R) Reserved

5 (R) Reserved

4 (R) (SWCORR) - SOFTWARE CORRECTABLE ERROR DETECTED: This bit is set when the Data ECC is not hardware correctable, but is software correctable.

3 (R) (SECHIT) - SECTOR HIT: This bit is set when the Disk Sequencer transfers a Data Sector, i.e. when INITDATA is asserted.

2 (R) Reserved

1 (R) (DCMPNEQ) - DATA COMPARE NOT EQUAL: This bit is set when the Data Compare in the Data ECC Block failed.

0 (R) (WRFLTDET) - WRITE FAULT DETECTED: This bit is set if the Disk Sequencer is ever stopped due to the Stop On Input Write Fault (STPWRFAULT, reg. 61h, R/W, bit 3).

5E DISK INTERRUPT CLEAR 0 REGISTER (5Eh, W, DISKINTCLR0)

These bits are used to clear the corresponding bits in the Disk Interrupt 0 Status register (reg. 5Eh, R).

7 (W) (CLR_SRVOVRN) - CLEAR SERVO OVERRUN: When set, this bit clears the Servo Overrun bit (reg. 5Eh, R, bit 7).

6 (W) Reserved

5 (W) Reserved

4 (W) (CLR_SWCORR) - CLEAR SOFTWARE CORRECTABLE ERROR DETECTED: When set, this bit clears the Software Correctable Error Detected bit (reg. 5Eh, R, bit 4).

3 (W) (CLR_SECHIT) - CLEAR SECTOR HIT: When set, this bit clears the Sector Hit bit (reg. 5Eh, R, bit 3).

2 (W) Reserved

1 (W) (CLR_DCMPNEQ) - CLEAR DATA COMPARE NOT EQUAL: When set, this bit clears the Data Compare Not Equal bit (reg. 5Eh, R, bit 1).

0 (W) (CLR_WRFLTDET) - CLEAR WRITE FAULT DETECTED: When set, this bit clears the Write Fault Detected bit (reg. 5Eh, R, bit 0).

5F DISK INTERRUPT ENABLE 0 REGISTER (5Fh, R/W, DISKINTEN0)

The bits in this register enable the corresponding bits in the Disk Interrupt Status 0 Register (DISKINT0, reg. 5Eh, R) to generate an interrupt to the local microprocessor if the EN_DISKINT0 bit (reg. 53h, R/W, bit 5) is also set. Writing a 1 to a bit in this register will enable the corresponding status bit as an interrupt to the microprocessor. Writing a 0 to a bit in this register will inhibit the interrupt for the corresponding status bit, but will have no effect on the state of that status bit.

7 (R/W) (EN_SRVOVRN) - ENABLE SERVO FETCH OVERRUN INTERRUPT: Setting this bit will enable the Servo Fetch Overrun bit (SRVOVRN, reg. 5Eh, R/W, bit 7) to set the Disk Interrupt Active bit (reg. 52h, R, bit 5).

6 (R/W) Reserved

5 (R/W) Reserved

4 (R/W) (EN_SWCORR) - ENABLE SOFTWARE CORRECTABLE DATA INTERRUPT: Setting this bit will enable the Software Correctable Data bit (SWCORR, reg. 5Eh, R/W, bit 4) to set the Disk Interrupt Active bit (reg. 52h, R, bit 5).

3 (R/W) (EN_SECHIT) - ENABLE SECTOR HIT INTERRUPT: Setting this bit will enable the Sector Hit bit (SECHIT, reg. 5Eh, R/W, bit 3) to set the Disk Interrupt Active bit (reg. 52h, R, bit 5).

2 (R/W) Reserved

1 (R/W) (EN_DCMPNEQ) - ENABLE DATA COMPARE NOT EQUAL INTERRUPT: Setting this bit will enable the Data Compare Not Equal bit (DCMPNEQ, reg. 5Eh, R/W, bit 1) to set the Disk Interrupt Active bit (reg. 52h, R, bit 5).

0 (R/W) (EN_WRFLTDET) - ENABLE WRITE FAULT DETECT INTERRUPT: Setting this bit will enable the Write Fault Detected bit (WRFLTDET, reg. 5Eh, R/W, bit 0) to set the Disk Interrupt Active bit (reg. 52h, R, bit 5).

60 DISK CONTROL 0 REGISTER (60h, R/W, DCTL_0)

7 (R/W) (DWRITE) - DISK WRITE: When set, this bit establishes the direction of the data transfer to be from the Buffer to the Disk. While set, and with the Disk Sequencer running, the Disk FIFO will pre-fetch data from the Buffer if data is available in the buffer (Buffer Ready condition is present). During a Verify operation the Disk Verify bit (DVERIFY, reg. 62h, R/W, bit 7) is set and the DWRITE bit must be cleared.

6 (W) (RSTDFIFO) - RESET DISK FIFO: When set, Disk FIFO and associated logic is reset. The Disk FIFO pointers are reset to the beginning of the FIFO. This bit does not have to be reset before being set. This bit reads back as '0' always. RRCLK must be present for the actual Disk FIFO reset to occur.

5 (R/W) (ENNRZFALL) - ENABLE NRZ REFERENCED TO FALLING EDGE OF RCLK: WCLK is generated from RCLK (with a slight propogation delay). NRZ Write Data can be referenced from rising or falling edge of RCLK, or from rising edge of WCLK. When this bit is set, WCLK is inverted with respect to RCLK, and NRZ Write Data is referenced from falling edge of RCLK or rising edge of WCLK. When this bit is reset, WCLK is in phase with RCLK, and NRZ Write Data is referenced from rising edge of RCLK or rising edge of WCLK. See Figure 8-29 on page 183.

4 (R/W) Reserved

3:2 (R/W) (NRZSEL[1:0]) - NRZ SELECT[1:0]: This two bit field selects how many NRZ data pins are used for the Disk interface.

NRZSEL[1:0]	DISK INTERFACE
0 0	Single NRZ NRZ[0]
0 1	Dual NRZ NRZ[1:0]
1 0	8-Bit NRZ NRZ[7:0]
1 1	Reserved

1 (R/W) (DLYWG) - DELAY WRITE GATE: When this bit is set to 1 the WG pin is delayed by one Byte Clock, and the relationship to the NRZ data out is changed. When DLYWG=0 the first byte of data on NRZ when WG is asserted is 00h followed by the selected data source, and when WG is negated the number of bytes written (e.g. the pad bytes) is one less than the Sequencer Count field specifies. When DLYWG=1 the first byte of NRZ data when WG is asserted is the selected data source, and when WG is negated the number of bytes written is

the same as the Sequencer Count field specifies.

0 (R/W) (ENSYNCFALL) - ENABLE SYNC FOUND REFERENCED TO FALLING EDGE OF RCLK: When this bit is set the SYNCF input is sampled on the falling edge of RCLK. When this bit is reset SYNCF input is sampled on the rising edge of RCLK.

61 DISK CONTROL 1 REGISTER (61h, R/W, DCTL_1)

7 (R/W) (EN2BSYNC) - ENABLE 2-BYTE FAULT TOLERANT SYNC: When set, this bit configures the disk logic to utilize a 2-byte fault tolerant sync byte with a tolerance of a 6-bit burst error. The expected 2-byte sync pattern is defined in the Disk Sequencer Map. The most significant byte is defined when LOADSYNC=1 (Alternate Instruction SEQCTLB=11b) and the least significant byte whenever NEXTADREN=0 (SEQCTL bit 7). While this bit is cleared, the sync byte is a single byte with no fault tolerance, and the expected sync byte is programmed in the Sequencer Map.

6 (R/W) (DSBLFLUSH) - DISABLE FIFO FLUSH: When this bit is reset the Disk FIFO is flushed each time the Buffer/Disk transfer is terminated, i.e. the ENBUFFER decode in the Sequencer is negated. If the Disk data size is an odd number of bytes and the buffer is 16 bits wide the flush also pads the extra byte with indeterminate data. During a Write operation the extra pad byte is thrown away. The FIFO is flushed during a read to get the full sector into the buffer.

When this bit is set the Disk FIFO is never flushed. When this bit is reset from a 1 to a 0 by writing to this register the Disk FIFO is flushed.

5 (R/W) (ENEXTCDR) - ENABLE EXTERNAL CDR INTERRUPT: When this bit is set the External CDR Interrupt signal is used to interrupt the Disk Sequencer. The ENCDR bit (reg. 62h, R/W, bit 3) must be reset. When this bit is reset the internal CDR circuitry is used (ENCDR=1).

4 (R/W) (ENINDEX) - ENABLE INDEX TO SECTOR BRANCH: When this bit is set, the INDEX pin is OR'd into the Sector branches W_SECTOR (Primary Branch 001b) and W_SECVALID (Alternate Branch 111b).

3 (R/W) (STPWRFAULT) - STOP ON INPUT WRITE FAULT: While this bit is set, an assertion of the INPUT pin signal will cause the Disk Sequencer to immediately stop. In this case, the INPUT signal will be recognized by its leading edge and must be asserted for more than two BUFCLK periods to guarantee detection.

2:0 (R/W) (SYNCOFS[2:0]) - EXTERNAL SYNC BYTE FOUND OFFSET[2:0]: This three bit field is used only when the Enable External Sync bit (reg. 63h, R/W, bit 0) is set. This field is used to align the sequencer to the SYNCFND mark produced by an external sync detect circuit. The offset is specified in RRCLK periods. The following table shows the offset values and the associated valid NRZ modes.

SYNCOFS[2:0]	OFFSET	VALID NRZ MODES
1 1 1	+7 RRCLKs	Single
1 1 0	+6 RRCLKs	Single
1 0 1	+5 RRCLKs	Single
1 0 0	+4 RRCLKs	Single

0 1 1	+3 RRCLKs	Single, Dual
0 1 0	+2 RRCLKs	Single, Dual
0 0 1	+1 RRCLKs	Single, Dual, Byte
0 0 0	0 RRCLKs	Single, Dual, Byte

A zero offset means that SYNCFND occurs on the first byte following the Sync byte. All offsets are early and no "late" offset is supported. In all cases, the SYNCFND mark must meet the RRCLK setup time to be valid.

62 DISK CONTROL 2 REGISTER (62h, R/W, DCTL_2)

7 (R/W) (DVERIFY) - DISK VERIFY: This bit compares data read off the Disk with data in the Buffer. While this bit is set, the ECC logic will perform a user selectable ECC check of the data being read from the disk. The selection is done via the CORR_TH bits (reg. 98h, R/W, bits 4:3). When this bit is set ECC correction in the Buffer is disabled.

6 (R/W) (SUPXFR) - SUPRESS TRANSFER: When set, this bit overrides the ENBUFFER decode (SEQCTLB[1:0] = '10', with ALTINSTSEL=0) in the Sequencer Map and prevents transfers to or from the Buffer memory. During a disk write operation, the Sequencer Data Field will be the source of the write data. ECC check bytes will not be generated in this case. During a disk read operation, the incoming data will have the ECC verified but no data will be transferred to the Buffer memory; hardware correction must be disabled in this case. When this bit is set ECCcorrection in the Buffer is disabled.

5 (R/W) Reserved

4 (R/W) (ENOUTPUT) - ENABLE OUTPUT: When set, this bit configures the INPUT/OUTPUT pin as an output. In this case, the OUTPUT pin signal can be set via the SETOUTPUT decode (SEQCTLB = '01', Alternate) in the Sequencer Map and reset via the RSTOUTPUT decode (SEQCTLB = '10', Alternate). When cleared, the INPUT/OUTPUT pin is an input. In this case, the Sequencer can execute a branch instruction based upon the presence of the INPUT signal in the Sequencer Map (Primary BRSEL = '011').

3 (R/W) (ENCDR) - ENABLE CDR: While this bit is set, the CDR Counter is enabled to generate CDR interrupts to the Disk Sequencer whenever it has counted down to zero. The Disk Sequencer in turn, will be interrupted and begin execution at the Sequencer Map location specified by the Read/Write Vector Address register (reg. 72h, R/W). It also enables the CDR Counter to be loaded from the CDR FIFO during a CDR FIFO write by the microprocessor or from the buffer. When this bit is cleared, the CDR FIFO and associated control circuitry is cleared and the CDR FIFO pointer is reset to point to the top of the FIFO. This bit must be cleared when using External CDR.

2 (R/W) (SECEQ) - ENABLE CURRSECEQ IN W_SECVALID BRANCH: When this bit is set the W_SECVALID Branch in the Disk Sequencer (Alternate Branch 111b) goes to PC+1 if CURRSEC=REQSEC (and other conditions - see bits 1:0 of this register), else it goes to Next Address.

1 (R/W) (SECRDY) - ENABLE BUFNRDY IN W_SECVALID BRANCH: When this bit is set the W_SECVALID Branch in the Disk Sequencer (Alternate Branch 111b) goes to PC+1 if

BUFNRDY=0 (and other conditions - see bits 2 and 0 of this register), else it goes to Next Address.

0 (R/W) (SECDEF) - ENABLE DEFSEC IN W_SECVALID BRANCH: When this bit is set the W_SECVALID Branch in the Disk Sequencer (Alternate Branch 111b) goes to PC+1 if CDRVALID=1 and DEFSEC=0 (and other conditions - see bits 2:1of this register), else it goes to Next Address. If the Sequencer Timeout occurs and CDRVALID=0 the Sequencer stops.

63 DISK CONTROL 3 REGISTER (63h, R/W, DCTL_3)

7 (R/W) (ACTHISNCF) - SELECT ACTIVE HIGH SYNC FOUND: This bit establishes the polarity of the SYNCF input pin. While this bit is set, SYNCF is active high. While this bit is cleared, SYNCF is active low.

6 (R/W) (ACTHISEC) - SELECT ACTIVE HIGH SECTOR: This bit establishes the polarity of the SECTOR input pin. While this bit is set, SECTOR is active high. While this bit is cleared, SECTOR is active low. This has the effect of changing the edge/polarity at which SECTOR is detected.

5 (R/W) (ACTHIIDX) - SELECT ACTIVE HIGH INDEX: This bit establishes the polarity of the INDEX input pin. While this bit is set, INDEX is active high. While this bit is cleared, INDEX is active low. This has the effect of changing the edge/polarity at which INDEX is detected.

4 (R/W) (ACTHIEOS) - SELECT ACTIVE HIGH END OF SERVO: This bit establishes the polarity of the EOS input pin. While this bit is set, EOS is active high. While this bit is cleared, EOS is active low. This has the effect of changing the edge/polarity at which EOS is detected.

3 (R/W) Reserved

2 (R/W) (ENCDRPOP) - ENABLE CDR FIFO READ POP: This bit is normally set for diagnostic reading of the CDR FIFO only. While this bit is set, a read of the CDR FIFO by the local microprocesor will result in the CDR FIFO "pop" operation allowing the next sequential CDR FIFO bytes to be read. For normal CDR FIFO operation during Disk read and write operations, this bit must be cleared. A CDR FIFO pointer 'pop' operation will take place when a read of the CDR FIFO 1 register (reg. 79h, R/W) is performed.

1 (R/W) (ENBUFCDR) - ENABLE READING SERVO COUNTS FROM BUFFER: This bit determines the source for the CDR split data bytes to be loaded into the CDR FIFO. When this bit is set, the CDR FIFO is loaded with CDR split values from the buffer. When this bit is cleared, the data is loaded into the CDR FIFO by the Local MPU.

0 (R/W) (ENEXTSYNC) - ENABLE EXTERNAL SYNC FOUND: When this bit is set, the SYNCFND input signal is enabled as the sync source for the Disk Sequencer. When this bit is cleared, the internal sync detect circuitry is used. The internal Sync Detect can be a single byte or the two byte fault tolerant Sync per EN2BSYNC (reg. 61h, R/W, bit 7). The ACTHISYNCF bit (reg. 63h, R/W, bit 7) determines the polarity of the SYNCFND signal while enabled by this bit. This bit is used in conjunction with the SYNCOFS[2:0] bits (reg. 61h, R/W, bits 2:0).

64 DISK STATUS 0 REGISTER (64h, R/W, DSTAT_0)

7 (R/W) (SEEDOVRN) - ECC SEED FIFO OVERRUN: This bit is set when the Corrected Seed FIFO is loaded with three or more values before the Local MPU reads it to Log the Sector in error. If STPSEEDOVR=1 (reg. 5Dh, R, bit 6) the Disk Sequencer will stop when this bit is set. The overflowing Seed value will not be saved. This bit is cleared when a 1 is written to it.

6 (R/W) (CDRPARERR) - CDR PARITY ERROR: This bit is set when a parity error is detected on the CDR Split count as it is transfered from the CDR FIFO into the CDR Counter. When it is set the Disk Sequencer will immediately stop if STPCDRPERR (reg. 5Dh, R/W, bit 3) is set. This bit is cleared by writing a 1 back to it.

5 (R/W) (MISSRCLK) - MISSING READ CLOCK DETECTED: This bit is set whenever the RRCLK input has not made a low to high transition within 16 BUFCLK cycles. This bit is cleared by a Disk Block reset or by writing a '1' to it. This bit requires an active BUFCLK in order to be set or cleared.

4:3 (R/W) Reserved

2 (R) (BUFNRDY) - BUFFER NOT READY: This ***read only*** bit is set when the buffer is not ready for disk transfer either to or from the buffer. The Disk FIFO must contain at least 8 bytes (8-bit buffer) or words (16-bit buffer).

1 (R/W) (SECTIMEOUT) - SEQUENCER TIMEOUT ON WAIT FOR SECVALID: This bit is set if the Disk Sequencer times out while executing the W_SECVALID branch. This bit is cleared when a 1 is written to it.

0 (R) (STOPSECEQ) - STOP SECTOR REACHED: This ***read only*** bit is set when the Request Sector Number registers (REQSEC, regs. 6Ch/6Dh, R/W) equal the Stop Sector Number registers (STOPSEC, regs. 6Eh/6Fh R/W).

65 DISK STATUS 1 REGISTER (65h, R/W, DSTAT_1)

7 (R/W) (EOSPASS) - END OF SERVO PASSED: This bit is asynchronously set on the asserting edge of the EOS input signal; it is cleared when written with a 1. Note that the EOS signal has programmable polarity. This bit requires an active BUFCLK in order to be set or cleared.

6 (R/W) (EOSCMPASS) - END OF SERVO COMPARE PASSED: This bit is asynchronously set on the asserting edge of the EOS input signal when EOSCTR equals EOSCMP Register (reg. 5Ch, R/W); it is cleared when written with a 1. Note that the EOS signal has programmable polarity. This bit requires an active BUFCLK in order to be set or cleared.

5 (R/W) (INDEXPASS) - INDEX PASSED: This bit is asynchronously set by the asserting edge of the INDEX pin signal; it is cleared when a 1 is written to this bit. Note that the polarity of the INDEX signal pin is programmable. This bit requires an active BUFCLK in order to be set or cleared.

4 (R/W) (SECTORPASS) - SECTOR PASSED: This bit is asynchronously set by the asserting edge of the SECTOR pin signal. It is cleared when a 1 is written to this bit. The polarity of the SECTOR signal pin is programmable. This bit requires an active BUFCLK in order to be set or cleared.

3 (R) (SEQOUTPUT) - SEQUENCER OUTPUT STATUS: This ***read only*** bit indicates the state of the OUTPUT pin while the Enable Output bit (ENOUTPUT, reg. 62h, R/W, bit 4) is set. However, while the ENOUTPUT bit is cleared, this bit will reflect the state of the OUTPUT function in the Disk Sequencer.

2 (R) (SEQINPUT) - SEQUENCER INPUT STATUS: This ***read only*** bit indicates the state of the INPUT pin while the Enable Output bit (ENOUTPUT, reg. 62h, R/W, bit 4) is cleared. However, while the ENOUTPUT bit is set, this bit will always be 0.

1 (R/W) (EOSTIMEOUT) - SEQUENCER TIMEOUT ON WAIT FOR EOSCMP: This bit is set if the Disk Sequencer times out while executing the W_EOSCMP branch. This bit is cleared when a 1 is written to it.

0 (R) (IDXCTREQ0) - INDEX COUNTER EQUALS ZERO: This ***read only*** bit is set to 1 when the Index Counter (INDEXCTR, regs. 76h/77h, R/W) decrements to 00h. It is cleared when the microprocessor writes to the INDEXCTR1 Register (reg. 77h, R/W) or the INDEXCTR0 Register (reg. 76h, R/W) if addresses are swapped for Motorola mode (SWAPADD=1, reg. 51h, R/W, bit 5). The Index Counter registers can be used by the microprocessor as a general purpose register timer.

66 DISK INTERRUPT 1 STATUS REGISTER (66h, R, DISKINT 1)

The status bits in this register get set and remain set when the corresponding status condition occurs. Each bit can be cleared by writing a 1 to the corresponding bit in the Disk Interrupt Clear 1 register (reg. 66h, W). Also, each status bit can be enabled to generate an interrupt via the corresponding interrupt mask bit in the Disk Interrupt Enable 1 register (reg. 67h, R/W) and by setting the EN_DISKINT1 bit (reg. 53h, R/W, bit 6).

7 (R) (TWOINDEXTO) - TWO INDEX TIME-OUT: When set, this bit indicates that two Index pulses have been detected since the last RST2IDXTO instruction decode (SEQCTLB = '11', Primary) operation by the sequencer. The sequencer is automatically stopped while this bit is set if the Stop On Index Time-Out bit (STP2IDXTO, reg. 7Eh, R/W, bit 0) is set.

6 (R) (SEQWAITTO) - SEQUENCER WAIT TIME-OUT: This bit indicates that a "Wait For ..." instruction in the Disk Sequencer has timed out before the test condition became true. The one exception to the above is the "Wait For Defect Flag" instruction in which case the 'SRVOVRN' interrupt is set (reg. 5Eh, R, bit 7).

5 (R) (UNCORR) - UNCORRECTABLE ECC ERROR: When set, this bit indicates that an uncorrectable ECC error has been found in the previous read sector that cannot be corrected via hardware. This bit will also be set if the ECC correction threshold is exceeded even if the error can be corrected via full hardware correction. The Sequencer will automatically stop if the Stop On Uncorrectable ECC bit (STPUNCORR, reg. 7Eh, R/W, bit 7) bit is set.

4 (R) Reserved

3 (R) (CORRECC) - CORRECTED ECC ERROR: This bit is set after a hardware correctable ECC error is found and has been corrected in the buffer.

2 (R) (SECWRAP) - SECTOR NUMBER WRAPPED: This bit is set when the Request Sector Number Registers (REQSEC, regs. 6Ch/6Dh, R/W) have wrapped to the value specified in the Wrap To Sector Registers (WRAPTOSEC, regs. 6Ah/6Bh, R/W) as a result of having reached the value in the Wrap Sector Number Registers (regs. 68h/69h, R/W). REQSEC is incremented by the "Increment Requested Sector Number" Disk Sequencer instruction.

1 (R) (SECOKDET) - SECTOR OK DETECTED: When set, this bit indicates that one of the following events has occurred:

a. On a Write operation, the ECC redundancy for a sector Data field has been written.

b. On a Read operation, a sector without errors has been written to the buffer, or sector data has been corrected in the buffer.

0 (R) (STOPPED) - SEQUENCER STOPPED: When set, this bit indicates that the Sequencer has changed from a running to a stopped state.

66 DISK INTERRUPT CLEAR 1 REGISTER (66h, W, DISKINTCLR 1)

These bits are used to clear the corresponding bits in the Disk Interrupt 1 Status register (reg. 66h, R).

7 (W) (CLR_TWOINDEXTO) - CLEAR TWO INDEX TIME-OUT: When set, this bit clears the Two Index Time-Out bit (reg. 66h, R, bit 7).

6 (W) (CLR_SEQWAITTO) - CLEAR SEQUENCER WAIT TIME-OUT: When set, this bit clears the Sequencer Time-out bit (reg. 66h, R, bit 6).

5 (W) (CLR_UNCORR) - CLEAR UNCORRECTABLE ECC ERROR: When set, this bit clears the Uncorrectable ECC Error bit (reg. 66h, R, bit 5).

4 (W) Reserved

3 (W) (CLR_CORRECC) - CLEAR CORRECTED ECC ERROR: When set, this bit clears the Corrected ECC Error bit (reg. 66h, R, bit 3).

2 (W) (CLR_SECWRAP) - CLEAR SECTOR NUMBER WRAPPED: When set, this bit clears the Sector Number Wrapped bit (reg. 66h, R, bit 2).

1 (W) (CLR_SECOKDET) - CLEAR SECTOR OK DETECTED: When set, this bit clears the Sector OK Detected bit (reg. 66h, R, bit 1).

0 (W) (CLR_STOPPED) - CLEAR SEQUENCER STOPPED: When set, this bit clears the Sequencer Stopped bit (reg. 66h, R, bit 0).

67 DISK INTERRUPT ENABLE 1 REGISTER (67h, R/W, DISKINTEN 1)

The bits in this register enable the corresponding bits in the Disk Interrupt 1 Status register (reg. 66h, R) to generate an interrupt to the local microprocessor if the EN_DISKINT1 bit (reg. 53h, R/W, bit 6) is also set. Writing a 1 to a bit in this register will enable the corresponding status bit as an interrupt to the microprocessor. Writing a 0 to a bit in this register will inhibit the interrupt for the corresponding status bit, but will have

no effect on the state of that status bit.

7 (R/W) (EN_TWOINDEXTO) - ENABLE TWO INDEX TIME-OUT INTERRUPT: Setting this bit will enable the Two Index Time-Out bit (reg. 66h, R, bit 7) to set the Disk Interrupt Active 1 bit (reg. 52h, R, bit 6).

6 (R/W) (EN_SEQWAITTO) - ENABLE SEQUENCER WAIT TIME-OUT INTERRUPT: Setting this bit will enable the Sequencer Wait Time-Out bit (reg. 66h, R, bit 6) to generate an interrupt.

5 (R/W) (EN_UNCORR) - ENABLE UNCORRECTABLE ECC INTERRUPT: Setting this bit will enable the Uncorrectable ECC Error bit (reg. 66h, R, bit 5) to set the Disk Interrupt Active 1 bit (reg. 52h, R, bit 6).

4 (R/W) Reserved

3 (R/W) (EN_CORRECC) - ENABLE CORRECTABLE ECC INTERRUPT: Setting this bit will enable the Corrected ECC Error bit (reg. 66h, R, bit 3) to set the Disk Interrupt Active 1 bit (reg. 52h, R, bit 6).

2 (R/W) (EN_SECWRAP) - ENABLE SECTOR NUMBER WRAP INTERRUPT: Setting this bit will enable the Sector Number Wrapped bit (reg. 66h, R, bit 2) to set the Disk Interrupt Active 1 bit (reg. 52h, R, bit 6).

1 (R/W) (EN_SECTOKDET) - ENABLE SECTOR OK DETECTED INTERRUPT: Setting this bit will enable the Sector OK Detected bit (reg. 66h, R, bit 1) to set the Disk Interrupt Active 1 bit (reg. 52h, R, bit 6).

0 (R/W) (EN_STOPPED) - ENABLE SEQUENCER STOPPED INTERRUPT: Setting this bit will enable the Sequencer Stopped bit (reg. 66h, R, bit 0) to set the Disk Interrupt Active 1 bit (reg. 52h, R, bit 6).

68 WRAP SECTOR NUMBER 0 REGISTER (68h (69h), R/W, WRAPSEC_0)

7:0 (R/W) (WRAPSEC[7:0]) -WRAP SECTOR NUMBER 0[7:0]: These bits form the low order byte of the Wrap Sector register.

69 WRAP SECTOR NUMBER 1 REGISTER (69h (68h), R/W, WRAPSEC_1)

7:2 (R/W) Reserved

1:0 (R/W) (WRAPSEC[9:8]) -WRAP SECTOR NUMBER 1[9:8]: These two bits are the most significant bits of the Wrap Sector register.

The WRAPSEC register establishes the wrap value at which the Request Sector Number Register (regs. 6Ch/6Dh) will be loaded with the contents of the WRAPTOSEC Register (regs. 6Ah/6Bh). This will occur when the Disk Sequencer attempts to increment the Request Sector Number Register (regs. 6Ch/6Dh) when it equals WRAPSEC.

6A WRAP TO SECTOR NUMBER 0 REGISTER (6Ah (6Bh), R/W, WRAPTOSEC_0)

7:0 (R/W) (WRAPTOSEC[7:0]) -WRAP TO SECTOR NUMBER 0[7:0]: These bits form the low order byte of the Wrap To Sector register.

6B WRAP TO SECTOR NUMBER 1 REGISTER (6Bh (6Ah), R/W, WRAPTOSEC_1)

7:2 (R/W) Reserved

1:0 (R/W) (WRAPTOSEC[9:8]) -WRAP TO SECTOR NUMBER 1[9:8]: These two bits are the most significant bits of the Wrap To Sector register.

The WRAPTOSEC register specifies the value that the Request Sector Number Register (regs. 6Ch/6Dh) will wrap to when it is incremented by the Disk Sequencer past the value in the Wrap Sector Number Register (regs. 68h/69h).

6C REQUEST SECTOR 0 REGISTER (6Ch (6Dh), R/W, REQSEC_0)

7:0 (R/W) (REQSEC[7:0]) - REQUEST SECTOR NUMBER [7:0]: This is the low order byte of the Request Sector Number register. This register will only be written correctly when the SEQRUN bit (reg. 73h, R/W, bit 7) is not set.

6D REQUEST SECTOR 1 REGISTER (6Dh (6Ch), R/W, REQSEC_1)

7:2 (R/W) Reserved

1:0 (R/W) (REQSEC[9:8]) - REQUEST SECTOR NUMBER [9:8]: These are the high order bits of the Request Sector Number register.

This register is used to define the physical sector number of the next Requested Sector. It is compared to the CURRSEC Register (regs. 5Ah/5Bh, R/W) and generates the CURRSECEQ status bit (reg. 5Bh, R/W, bit 7) which is used by the Sequencer 'Wait For Sector Valid Branch' instruction. It is incremented when the "Increment Requested Sector Number" decode is set in the Sequencer.

6E STOP SECTOR NUMBER 0 REGISTER (6Eh (6Fh), R/W, STOPSEC_0)

7:0 (R/W) (STOPSEC[7:0]) - STOP SECTOR NUMBER 0[7:0]: This is the low order byte of the Stop Sector Number register.

6F STOP SECTOR NUMBER 1 REGISTER (6Fh (6Eh), R/W, STOPSEC_1)

7:2 (R/W) Reserved

1:0 (R/W) (STOPSEC[9:8]) - STOP SECTOR NUMBER 1[9:8]: These are the high order bits of the Stop Sector Number register.

The contents of the Stop Sector Number Register are compared to the Request Sector Number register (regs. 6Ch/6Dh, R/W) whenever the Disk Sequencer executes a "Next Address If End of Transfer" instruction decode. The Sequencer will branch to the Next Address (typically the Sequencer Stop Address, 1Fh) if they are equal. This register can be updated on-the-fly. The update always occurs on a write to address 6Fh, thus keeping word writes available for both Intel and Motorola Modes.

72 READ/WRITE VECTOR REGISTER (72h, R/W, RDWRVEC)

7:5 (R/W) Reserved

4:0 (R/W) (RDWRVEC[4:0]) - READ/WRITE VECTOR ADDRESS[4:0]: This register contains the vector address used by the Disk Sequencer during read or write operations of the data field or ECC field. When the CDR counter reaches zero the Sequencer will branch to the address in this register.

73 SEQUENCER ADDRESS REGISTER (73h, R/W, SEQADR)

7 (R/W) (SEQRUN) - SEQUENCER RUN CONTROL/STATUS: Setting this bit starts the Disk Sequencer at the Start Address specified in this register. Resetting this bit causes the asynchronous stopping of the Sequencer. Reading this bit will return the current run/stop state of the Disk Sequencer.

When this bit is set the Sequencer will start executing 3 to 4 Disk Byte Clocks after this bit is set. The SEQRUN read status is immediately set. When this bit is reset it takes 2 to 3 Byte Clocks to stop the Sequencer, and the read of this status reflects that.

6:5 (R/W) Reserved

4:0 (R/W) (SEQADR[4:0]) - SEQUENCER START/CURRENT ADDRESS[4:0]: When writing to this register with the SEQRUN bit is set in this register, these bits specify the address at which the Disk Sequencer is started. If these bits are read while the Sequencer is stopped, the value returned will indicate the last Sequencer address executed before going to the stop address (1Fh).

74 FRAME COUNTER REGISTER (74h, R/W, FRAMECTR)

7:0 (R/W) (FRAMECTR[7:0]) - FRAME COUNTER[7:0]: A write to this register actually loads the Frame Count register (reg. 74h, W). In turn, the contents of the Frame Count register is loaded into the Frame Counter. Thus, the value in the Frame Count register is never changed by the Counter since it must be reloaded into the Frame Counter again at some point in time. A read of this register actually retrieves the current value in the Frame Counter (reg. 74h, R).

The Frame Counter is a general purpose counter which can be used in the sequencer map to implement "do-loop" structures. The Frame counter is tested and decremented by execution of every Sequencer instruction which contains the Primary '110' branch instruction (Next Address If FRAMECTR = 0). The Frame counter is tested for zero in this instruction. If it is zero, a branch to the address in the Next Address field is executed and then it is reloaded with the pre-load value in the Frame Count register. If the Frame counter is non-zero, it is decremented and the sequencer program counter is incremented.

75 COUNTER TEST REGISTER 1 (75h, R/W, CTRTEST)

7 (R/W) (TESTCTRS) - TEST DISK BLOCK COUNTERS: When this bit is set every byte clock will cause the FRAME, CDR, INDEX, EOS, REQSEC, and CURRSEC counters to increment/decrement.

6 (R/W) (TESTHBYTE) - TEST HIGH BYTE OF THE COUNTER: When this bit is set every byte clock will cause the high byte of the INDEX counter to increment/decrement.

5 (R) (FRMZERO) - FRAME COUNTER ZERO: This ***read only*** bit is active only while the TESTCTRS bit (reg. 75h, R/W, bit 7) is set. It is set when FRAMECTR is zero. This bit is used for manufacturing test purposes only.

4 (R/W) Reserved

3 (R) (CDRZERO) - CDR COUNTER ZERO: This ***read only*** bit is active only while the TESTCTRS bit (reg. 75h, R/W, bit 7) is set. It is set when the CDR Counter is zero. This bit is used for manufacturing test purposes only.

2 (R) (CDRFIFOFULL) - CDR FIFO FULL: This ***read only*** bit is set when the CDR FIFO is full. This bit is used for manufacturing test purposes only.

1 (R) (SYNCMATCHE) - SYNC DETECT MATCH EVEN: This ***read only*** bit is set when a Sync Byte is found. This is only valid for Dual NRZ and is set when the Sync Byte is aligned Bit 7 to NRZ1. This bit is used for manufacturing test purposes only.

0 (R) (SYNCMATCHO) - SYNC DETECT MATCH ODD: This ***read only*** bit is set when a Sync Byte is found. This bit is set for Dual NRZ when the Sync Byte is aligned Bit 7 to NRZ0. It is also valid for Single NRZ. This bit is used for manufacturing test purposes only.

76 INDEX COUNTER 0 REGISTER (76h (77h), R/W, INDEXCTR_0)

7:0 (R/W) (INDEXCTR[7:0]) - INDEX COUNTER[7:0]: This is the least significant byte of the Index Counter.

77 INDEX COUNTER 1 REGISTER (77h (76h), R/W, INDEXCTR_1)

7:0 (R/W) (INDEXCTR[15:8]) - INDEX COUNTER[15:8]: This is the most significant byte of the Index Counter.

The Index Counter (INDEXCTR) can be used as a timer for relatively long time periods (up to 18 minutes for a 3600 RPM drive). The counter is enabled to decrement on each occurrence of the INDEX signal only after the microprocessor has written to INDEXCTR_1 (or INDEXCTR_0 if addresses are swapped for Motorola microprocessors). When the Index counter decrements to 0000h, further decrementing is inhibited and the IDXCTREQ0 bit (reg. 65h, R/W, bit 0) is set. This counter is loaded with the desired value, e.g. 0001h will count 1 index pulse minimum.

78 CDR FIFO 0 REGISTER (78h (79h), R/W, CDRDATA_0)

7:0 (R/W) (CDRDATA[7:0]) - CDR FIFO DATA[7:0]: This register is used to access the low order byte of the CDR FIFO, which feeds the CDR Counter. The CDR FIFO is four words deep and is used to hold up to four 16-bit CDR count values. For each count value, this byte is loaded first followed by the byte in CDRDATA_1 (reg. 79h, R/W) which will trigger the internal CDR FIFO pointer address increment. When the TESTCTRS bit (reg. 75h, R/W, bit 7) is set, a read of this register returns the CDR Counter bits [7:0].

79 CDR FIFO 1 REGISTER (79h (78h), R/W, CDRDATA_1)

7:0 (R/W) (CDRDATA[15:8]) - CDR FIFO DATA[15:8]: This register is used to access the high order byte of the CDR FIFO, which feeds the CDR Counter. For each count value, the low byte in CDRDATA_0 (reg. 78h, R/W) is loaded first followed by this register which triggers the internal CDR FIFO pointer address increment. If the ENCDRPOP bit (reg. 63h, R/W, bit 2) is set, a read of this register will cause a CDR entry to "pop" from the FIFO and the CDR FIFO pointer to point to the next CDR count value. A write of this register will cause a "push" of data onto the CDR FIFO every other write. If the ENCDRPOP bit is cleared, a read of this register will not cause a CDR FIFO pop but every other write of this register will cause a push to occur. When the TESTCTRS bit (reg. 75h, R/W, bit 7) is set, a read of this register returns the CDR Counter bits [12:8] (in this case, bits 15:13 are reserved). The CDR Counter is read mainly for manufacturing test purposes.

7A DISK SEQUENCER COUNTER (7Ah (7Bh), R, SEQCTR)

7 (R) Reserved

6:0 (R) (SEQCTR[6:0]) - SEQUENCER COUNTER[7:0]: This register reflects the current value of the Disk Sequencer Counter and is used for manufacturing test purposes.

7B DISK MODULO 64 COUNTER (7Bh (7Ah), R, MOD64CTR)

7 (R) Reserved

6:0 (R) (MOD64CTR[6:0]) - MODULO 64 COUNTER[6:0]: This register reflects the current value of the Disk Sequencer Modulo 64 Counter and is used for manuafacturing test put-poses.

7D DISK FIFO STATUS REGISTER (7Dh, R, DFSTAT)

7 (R) (DFERR) - DISK FIFO ERROR: When set, this bit indicates that either a write of a byte into the Disk FIFO while it was full was attempted or that a read of the Disk FIFO while it was empty had occurred. This bit is reset whenever the microprocessor writes a '1' to the DBCCLR bit (reg. 108h, R/W, bit 5).

6 (R) Reserved

5:0 (R) (DFCNT[5:0]) - DISK FIFO BYTE COUNT[5:0]: These bits reflect the number of bytes currently in the Disk FIFO. A value of 00h indicates that the Disk FIFO is empty and a value of 20h indicates that it is full.

7E DISK AUTO STOP CONTROL REGISTER (7Eh, R/W, DISKSTOP)

7 (R/W) (STPUNCORR) - STOP ON UNCORRECTABLE ECC: When this bit is set, the Disk Sequencer will stop if the correction logic encounters an uncorrectable ECC error in the data field. Note that if the error is in the data field, this bit may get set during the sector following the one that had the ECC error. The BCTR register associated with the disk transfer is not incremented and the corrupted sector is not released to the host.

6 (R/W) (STPINPUT) - STOP ON INPUT: When this bit is set, the Disk Sequencer will stop when the INPUT signal is asserted while Write Gate is off. If Write Gate is on when the INPUT signal is asserted, the sequencer will keep running until Write Gate is turned off, at which time the sequencer will stop.

5 (R/W) (STPDBDPERR) - STOP ON DISK/BUFFER DATA PATH ERROR: When this bit is set, the Disk Sequencer will stop whenever the Disk FIFO Error bit (reg. 7Dh, R, bit 7) or the Disk Check Error bit (reg. 106h, R, bit 1) is set.

4 (R/W) (STPINDEX) - STOP ON INDEX: When this bit is set, the Disk sequencer will stop when the INDEX input pin is asserted.

3 (R/W) (STPCORR) - STOP ON CORRECTED ECC ERROR: When this bit is set, the Disk Sequencer will stop after an ECC error is hardware corrected in the buffer. Note that "SECTOR_OK" is not generated to the buffer controller for the corrected sector that stops the Sequencer. The BCTR register associated with the disk transfer is not incremented and the corrected sector is not released to the host. The Disk Sequencer will stop immediately when this condition occurrs.

2 (R/W) (STPENDSEC) - STOP ON SECTOR BOUNDARY: When this bit is set, the Disk Sequencer will stop at the sector boundary (WG and RG both = 0), and the Sequencer is not processing a CDR event.

1 (R/W) (STPBNRM) - STOP ON BUFFER NO ROOM: When this bit is set, the disk Sequencer will stop when the Buffer Memory is not available for transfer of data.

0 (R/W) (STPTWOIDXTO) - STOP ON TWO INDEX TIME-OUT: When this bit is set, the Disk Sequencer will stop when the Two Index Time-out status bit (reg. 66h, R, bit 7) is set.

NOTE: If an automatic stop condition occurs while Write Gate is on, the Sequencer will not be stopped until Write Gate turns off. Therefore, a write terminates either in a servo area or at the end of a sector. However, during a read operation the Sequencer is stopped immediately (except STPENDSEC) when a stop condition is detected. All of the bits in this register (except STPENDSEC), STPSEEDOVR (reg. 5Dh, R, bit 6), *STP-SEEDERR* (reg. 5Dh, R, bit 2), *and STPWRFAULT* (reg. 61h, R/W, bit 3) *can only be set when the Disk Sequencer is not running to avoid WG glitches. STPENDSEC can be written at any time.*

80 ECC SEED 2 (80h (81h), W, SEED2)

7:0 (R) (SEED2[7:0]) - SEED2[23:16]: These are bits 23:16 of the ECC Seed.

The SEED Registers are loaded with the 3 most significant bytes of the ECC Seed sent to the EDAC. The least significant 10 bits are sourced from the REQSEC1/0 Registers (regs. 6Ch/6Dh, R/W). These registers are used when ENSEED=1 (reg. 5Dh, R, bit 4) and the INITECC Decode (SEQCTLC=100b) is issued. When this occurs the four Seed Bytes are sent to the EDAC (SEED3-1, REQSEC1/0).

81 ECC SEED 3 (81h (80h), W, SEED3)

7:0 (R) SEED3[7:0]) - SEED3[31:24]: These are bits 31:24 of the ECC Seed.

83 ECC SEED 1 (83h (82h), W, SEED1)

7:2 (R) SEED1[7:2]) - SEED3[15:10]: These are bits 15:10 of the ECC Seed.

84 CORRECTED SEED FIFO 0 (84h (85h), R, CSEED0)

7:0 (R) (CSEED[7:0]) - CORRECTED SEED[7:0]: These are bits 7:0 of the first Corrected Seed entered into the CSEED FIFO since the last read of the CSEED1/0 Registers.

The Corrected Seed FIFO is loaded with the current ECC Seed Value when the REQSEC Register (regs. 6Ch/6Dh, R/W) is incremented and there is a current ECC Error. However, this entry is not valid until the EDAC has determined it is correctable and has corrected it in the Buffer Memory and it does exceed the Error Logging Threshold defined in the EDAC. After two values have been pushed into the FIFO it is full, and any further pushes sets the SEEDOVRN status bit (reg. 64h, R/W, bit 7). The overflow Seed value is not stored to preserve the last value pushed. The Disk Sequencer will stop when SEEDOVRN is set if STP-SEEDOVR=1 (reg. 5Dh, R, bit 6). When the Local MPU reads these registers the first available value is popped when Reg. 85h is read. These registers can be read while the Disk Sequencer is running without corrupting the CSEED FIFO. The CSEED FIFO is reset when ENSEED=0 (reg. 5Dh, R, bit 4).

85 CORRECTED SEED FIFO 1 (85h (84h), R, CSEED1)

7 (R) (CSEEDVALID) - CORRECTED SEED VALID: This bit is set when the value in CSEED1/0 is valid. When the microprocessor reads the CSEED1/0 value this bit is reset if the CSEED FIFO is empty.

6:2 (R) Reserved

1:0 (R) (CSEED[9:8]) - CORRECTED SEED[9:8]: These are bits 9:8 of the first Corrected Seed entered into the CSEED FIFO since the last read of the CSEED1/0 Registers.

5.3 ECC Block Register Descriptions

96 ECC ERROR LOG THRESHOLD REGISTER (96h, R/W, ECCELTH)

7:4 (R/W) Reserved

3:0 (R/W) (ELTH[3:0]) - ECC ERROR LOG THRESHOLD[3:0]: These bits are the ECC Error Log Threshold value. If the Error Log Counter value (reg. 97h, R) is greater than the value in this register, the error log threshold will be exceeded and the CDTH status bit (reg. 9Bh, R/W, bit 5) will be set. To disable the XCDTH status bit, ELTH[3:0] must be set to 15 (decimal).

97 ECC ERROR LOG COUNTER (97h, R, ECCELOG)

7:4 (R/W) Reserved

3:0 (R) (ELOG[3:0]) - ECC ERROR LOG COUNTER [3:0]: This counter accumulates the number of error bytes encountered in the current sector. It is reset to 0 at the start of correction or upon a correction state machine reset. This counter is valid only if the sector is not uncorrectable.

98 ECC CONFIGURATION 0 REGISTER (98h, R/W, ECCCFG_0)

Writing to this register while the ECC Busy bit (reg. 9Ch, R, bit 5) is set will result in an unknown state.

7 (R/W) (AUTOINCDSBL) - DISABLE AUTO E_ADR INCREMENT: While this bit is set, the ECC Internal Address Counter (reg. 9Ah, R/W) will not automatically increment.

6:5 (R/W) (EWARN_TH[1:0]) - EARLY WARNING THRESHOLD[1:0]: This field determines the number of errors per interleave which will cause the EWARN bit (reg. 9Dh, R, bit 4) to be set indicating an early warning of the impending ECC error. The possible threshold levels are summarized in the table below.

EWARN_TH[1:0]	Description
0 0	Disable Early Warning
0 1	Early Warning on one or more error in any interleave
1 0	Early Warning on two or more errors in any interleave
1 1	Early Warning on three or more errors in any interleave

4:3 (R/W) (CORR_TH[1:0]) - ECC CORRECTION THRESHOLD[1:0]: The bits in this field select the desired ECC correction threshold. This field can be used in conjunction with the DVERIFY bit (reg. 62h, R/W, bit 7) to perform read verify operation on the disk with a user selectable level of error tolerance. If the number of errors exceed this threshold but is less than four, SWCORR (reg. 9Dh, R, bit 1) is asserted.

CORR_TH[1:0]	Description
0 0	Disable automatic correction in the buffer (Error location and pattern calculations will still take place)
0 1	Automatic correction of one error in any interleave
1 0	Automatic correction of up to two errors in any interleave
1 1	Automatic correction of up to three errors in any interleave.

2:0 (R/W) Reserved

99 ECC CONFIGURATION 1 REGISTER (99h, R, ECCCFG_1)

7:0 (R) Reserved

9A ECC INTERNAL ADDRESS COUNTER REGISTER (9Ah, R/W, ECCACNTR)

7:4 (R) Reserved

3:0 (R/W) (ECCADDCTR[3:0]) - ECC INTERNAL ADDRESS COUNTER [3:0]: These bits are used to address the desired registers which are indirectly accessed through the ECC Indirect Data register (reg. 9Eh, R). This address counter is incremented after every read operation to the above mentioned register. While the AUTOINCDSBL bit (reg. 98h, R/W, bit 7) is set, this address counter will not increment.

9B ECC CONTROL REGISTER (9Bh, R/W, ECCCNTRL)

7:6 (R/W) Reserved

5 (R) (XCDTH) - ERROR THRESHOLD EXCEEDED: When set, this bit indicates that the number of accumulated errors exceeds threshold. It is negated by the microprocessor writing a 1 to this bit or upon a correction state machine reset. This bit is not setable by the microprocessor and is valid only if the sector is not uncorrectable.

4 (R/W) (SEEDEER) - SEED ERROR: When set, this bit indicates a Seed error. It is negated by the microprocessor writing a 1 to this bit or upon a correction state machine reset. This bit is not setable by the microprocessor.

3 (R/W) (RST_ECC) - RESET ECC LOGIC: Setting this bit resets the ECC block logic. All logic and state machines are held in the reset state while this bit is set. To terminate the reset state, this bit must be cleared by the local microprocesor. The RST_CORRSM and INIT_LFSR bits in this register are a subset of the function of this bit.

2 (R/W) (ROTATE) - ROTATE CURRENT INTERLEAVE: This bit is used to acknowledge a software correction request. At the end of a software correction service, writing a 1 to this bit will rotate the current interleave and allow hardware correction to continue. The current interleave number is available from the ECC Status Register 1 (reg. 9Dh, R, bits 7:6). The order of interleave rotation is: ...→ 2 → 1 → 0 → 2 → 1 → 0 →.... It is a pulsed bit - it is automatically cleared after the rotation is done.

1 (R/W) (RST_CORRSM) - RESET CORRECTION STATE MACHINE: Setting this bit will reset the correction state machine. To terminate the reset of the correction state machine the local microprocessor must clear this bit. The Disk Block can also force a correction state machine reset.

0 (R/W) (INIT_LFSR) - INITIALIZE LFSR: Setting this bit initializes the Linear Feedback Shift register (LFSR) to an all zeros state. To terminate the forced initialization this bit must be cleared by the local microprocessor. This bit is set automatically whenever the INITDATA decode (SEQCTLC='011') is asserted.

9C ECC STATUS 0 REGISTER (9Ch, R, ECCSTAT_0)

7 (R) (CURRERR) - CURRENT READ SECTOR IN ERROR: When set, this bit indicates that the current sector just read from the disk has an ECC error. This bit is set somewhere within the last four bytes of the ECC field for that sector. This bit is cleared when the Disk Sequencer executes an INITDATA decode (SEQCTLC = '011').

6 (R) (CORROVRN) - CORRECTION OVERRUN ERROR: Used for manufacturing test only.

5 (R) (ECCBUSY) - ECC BUSY: When set, this bit indicates that an ECC read, write, or correction operation is in progress.

4 (R) (UNCORR) - UNCORRECTABLE ECC ERROR: When set, this bit indicates that an uncorrectable ECC error has been encountered even if software algorithms are used. At its earliest, this bit will be set a few RRCLK cycles after the end of the current ECC field. This bit is cleared by setting the Reset ECC Logic bit (reg. 9Bh, W, bit 3) or the Reset Correction State Machine bit (reg. 9Bh, W, bit 1).

3 (R) (CMPNE) - DATA VERIFICATION COMPARE NOT EQUAL: This bit is set when the number of defective data per interleave, as indicated by the Correction Threshold bits (reg. 98h, R/W, bits 4:3), has been exceeded. This bit is valid only when doing a disk verify operation. It is cleared when the DVERIFY bit is cleared or by a LFSR INIT. This status bit does not generate an interrupt.

2:0 (R) (CMPDIFF[2:0]) - COMPARISON BYTE DIFFERENCE: These bits are internal signals that reflect the byte difference number in the current interleave during a verification. If no verification occurs, these bits are irrelevant. (For manufacturing use only.)

9D ECC STATUS 1 REGISTER (9Dh, R, ECCSTAT_1)

7:6 (R) (CURRINTL[1:0]) - CURRENT INTERLEAVE[1:0]: This field indicates the current interleave being operated upon by the ECC circuitry. During the correction operation, the value of these bits will be changing dynamically as per the interleave being operated on at the time they are read. During the first sector read operation, while no correction is taking place, the value of these bits will be '11'. For example, these bits are used during software ECC correction. After the Rotate Current Interleave bit (ROTATE, reg. 9Bh, W, bit 2) is used during firmware correction to point to a new interleave, these bits will reflect the new interleave to be corrected.

CURRINTL[1:0]	Description
0 0	Interleave 0
0 1	Interleave 1
1 0	Interleave 2
1 1	No current Interleave

5 (R) Reserved

4 (R) (EWARNSTAT) - EARLY WARNING STATUS: When set, this bit indicates that the desired early warning threshold, set up via the EWARN_TH[1:0] field (reg. 98h, R/W, bits 6:5), has been detected. This bit is cleared by setting the Reset ECC Logic bit (reg. 9Bh, W, bit 3) or the Reset Correction State Machine bit (reg. 9Bh, W, bit 1).

3:2 (R) (NUMERR[1:0]) - NUMBER OF ERROR IN CURRENT INTERLEAVE[1:0]]: These bits are used to indicate the number of ECC errors encountered in the current interleave. The value present on these bits will vary dynamically depending upon the interleave currently being operated upon and if there are any errors in that interleave. For example, these bits are used during software ECC correction. After the Rotate Current Interleave bit (ROTATE, reg. 9Bh, W, bit 2) is used during firmware correction to point to a new interleave, these bits will reflect the number of bad symbols in the new current interleave.

NUMERR[1:0]	Description
0 0	No errors in the current interleave
0 1	One error in the current interleave
1 0	Two errors in the current interleave
1 1	Three or more errors in the current interleave

1 (R) (SWCORR) - SOFTWARE CORRECTION REQUIRED: This signal is asserted when the number of errors in an interleave is greater than the correction threshold, but the errors are not determined to be uncorrectable. No further correction can occur when this signal is set. Correction can again resume when this signal is acknowledged by a micro forced rotate (ROTATE, reg. 9Bh, W, bit 2). This signal can also be negated by a correction state machine reset. The BCTR associated with the disk to buffer transfer will not get incremented if this bit is set. This bit may get set as early as several RRCLK cycles after the end of the current ECC field.

0 (R) (HWCORR) - HARDWARE CORRECTABLE ERROR: This bit indicates that an error has been encountered that is correctable via hardware. At the earliest, this bit can be set several RRCLK cycles after the end of the ECC field of the current sector. It is cleared by setting the Reset ECC Logic bit (reg. 9Bh, W, bit 3) or the Reset Correction State Machine bit (reg. 9Bh, W, bit 1). In addition, this bit is cleared if the Software Correction Required bit (reg. 9Dh, R, bit 1) or the Uncorrectable ECC Error bit (reg. 9Ch, R, bit 4) is set, or when status of the next sector is available.

9E ECC INDIRECT DATA REGISTER (9Eh, R, ECCIDATA)

The ECC Indirect Data register is used for software correction and test purposes only to access sixteen other registers indirectly. ECCIDATA_0 is used to access the lower order byte of the desired register. The register to be accessed is determined by the ECC Internal Address Counter (reg. 9Ah, R/W, bits 3:0). These registers are summarized in the following table:

ECCACNTR[3:0]	Register Name	Description	R/W
0	SN3	Syndrome SN3	R
1	SN2	Syndrome SN2	R
2	SN1	Syndrome SN1	R
3	S0	Syndrome S0	R
4	S1	Syndrome S1	R
5	S2	Syndrome S2	R
6	S3	Syndrome S3	R
7	Reserved	-	-
8	Reserved	-	-
9	Reserved	-	-
A	ERRPAT0	Error Pattern 0	R
B	ERRL0	Error Location 0	R
C	ERRPAT1	Error Pattern 1 (Double or triple error only)	R
D	ERRL1	Error Location 1 (Double or triple error only)	R
E	ERRPAT2	Error Pattern 2 (Triple error only)	R
F	ERRL2	Error Location 2 (Triple error only)	R

Error location and error patterns are valid only when SWCORR (reg. 9Dh, R, bit 1) is asserted.

5.4 Host Block Register Descriptions

Note: The microprocessor can only write to registers A1h through A7h (M_FEATRS, M_SECCNT, M_SECNUM, M_CYLLO, M_CYLHI, M_DRVHD, and M_CMD) when the Internal Busy bit (reg. C1h, R/W, bit 7) is set while the Buffer Transfer bit (reg. C1h, R, bit 6) is cleared. The microprocessor always has read access to these registers.

A0 MICROPROCESSOR AT ERROR REGISTER (A0h, R/W, M_ERROR)

This register provides error information to the Host about the last failed command. During diagnostics or power-up, this register is used for passing controller diagnostic error information to the Host. When an error condition occurs, the microprocessor can load this register and then set the Error bit (reg. C1h, R/W, bit 0). This register is the local microprocessors window into the AT Host Error register (reg. 1F1h, R). There are no restrictions as to when this register can be written or read.

7 (R/W) (BBK) - BAD BLOCK DETECTED: This bit indicates that a bad block mark was detected in the ID of the requested sector.

6 (R/W) (UNC) - UNCORRECTABLE DATA ERROR: This bit is set when the selected hardware error correction cannot correct the indicated sector.

5 (R/W) (MC) - MEDIA CHANGED: When set, this bit indicates that the removable media has been changed.

4 (R/W) (IDNF) - ID NOT FOUND: This bit is set whenever a sector to be read or written cannot be found.

3 (R/W) (MCR) - MEDIA CHANGE REQUESTED: When set, this bit indicates that the release latch on a removable media drive has been pressed. Removal of media has been requested by the user.

2 (R/W) (ABORT) - ABORT: This bit indicates that the requested command has been aborted due to a drive status error or because the command code is not valid. It is automatically set along with the HERROR bit in (reg. C1h, R/W, bit 0) if the Enable Auto Error Set bit (reg. C3h, R/W, bit 5) is set and the Host Port Check Error bit (HCHKERR, reg. 106h, R, bit 0) is set or the Host FIFO Error bit (HFIFOERR, reg. C8h, R, bit 1) is set. This bit will remain set as long as HCHKERR or HFIFOERR is set, so that HCHKERR and HFIFOERR must be cleared before the microprocessor attempts to clear this bit.

1 (R/W) (TRKONF) - TRACK 0 NOT FOUND: When set, this bit indicates that the selected drive could not successfully find Track 0.

0 (R/W) (AMNF) - ADDRESS MARK NOT FOUND: When set, this bit indicates that the sector in error could not be located due to a problem in reading the associated address mark in the header.

A1 MICROPROCESSOR AT FEATURES REGISTER (A1, R/W, M_FEATRS)

7:0 (R/W) (M_FEATRS[7:0]) - MICROPROCESSOR AT FEATURES [7:0]: This register is command specific and may be used to enable and disable features of the interface. This register may be ignored by some drives. Some hosts, based on definitions prior to the ATA specification, used this register to designate a recommended Write Pre-compensation Cylinder value. This register is the local microprocessors window into the AT Host Features register (reg. 1F1h, W). This register can only be written while AT BUSY (reg. CEh, R, bit 6) is set. There are no restrictions as to when this register can be read.

A2 MICRO. AT SECTOR COUNT REGISTER (A2h, R/W, M_SECCNT)

7:0 (R/W) (M_SECCNT[7:0]) - MICRO. AT SECTOR COUNT [7:0]: This register contains the number of sectors to be transferred during a PIO or DMA operation. During a non-automated PIO or DMA operation, the sector count in this register is decremented by the microprocessor as each sector is transferred. During an automated multi-sector PIO or DMA operation, this count is automatically decremented by the hardware with every sector transferred, and the operation is complete when the count decrements to zero. This also occurs on a Read Verify Command in which data is transferred only between the disk and the buffer. If a 256-sector transfer is desired, this register should be loaded with 00h. This register is the local microprocessors window into the AT Host Sector Count register (reg. 1F2h, R/W). This register can only be written while AT BUSY (reg. CEh, R, bit 6) is set. There are no restrictions as to when this register can be read.

A3 MICRO. AT SECTOR NUMBER REGISTER (A3h, R/W, M_SECNUM)

7:0 (R/W) (M_SECNUM[7:0]) - MICRO. AT SECTOR NUMBER [7:0]: The usage of this register is dependent upon the Enable LBA Mode bit (reg. C3h, R/W, bit 3) and the LBA bit (reg. 1F6h, bit 6). CHS (Cylinder/Head/Sector) mode of operation is used when the Enable LBA Mode bit is cleared. LBA (Logical Block Mode) mode of operation is used when the Enable LBA mode bit is set and the LBA bit is set. This register is the local microprocessors window into the AT Host Sector Number register (reg. 1F3h, R/W). This register can only be written while AT BUSY (reg. CEh, R, bit 6) is set. There are no restrictions as to when this register can be read.

The following paragraphs describe the operation of this register in both modes.

<u>CHS Mode:</u>

In CHS mode, this register contains the 8-bit sector number for the current PIO or DMA operation. During a non-automated PIO or DMA operation, this register is incremented by the microprocessor as each sector is transferred. During an automated multi-sector PIO or DMA operation, this register is automatically incremented by the hardware, so that when the transfer is completed, it is left pointing to the last sector transferred. When incremented from the Maximum Sector Number (regs. B1h/B2h, R/W), the Sector Number wraps to 1 and the Head Number is auto-incremented.

LBA Mode:

In LBA mode, this register contains the least significant logical block address (A7:A0) of the specified logical block. It is not compared to the Max. Sector Number registers (regs. B1h/ B2h, R/W) and will always wrap to 00h after counting to FFh. At the end of the command, this register is updated to reflect the current LBA bits A7:A0.

A4 MICRO. AT CYLINDER LOW REGISTER (A4h (A5h), R/W, M_CYLLO)

7:0 (R/W) (M_CYLLO[7:0]) - MICRO. AT CYLINDER LOW [7:0]: The usage of this register is dependent upon the Enable LBA Mode bit (reg. C3h, R/W, bit 3) and the LBA bit (reg. 1F6h, bit 6). CHS (Cylinder/Head/Sector) mode of operation is used when the Enable LBA Mode bit is cleared. LBA (Logical Block Mode) mode of operation is used when the Enable LBA mode bit is set and the LBA bit is set. This register is the local microprocessor's window into the AT Host Cylinder Low register (reg. 1F4h, R/W). This register can only be written while AT BUSY (reg. CEh, R, bit 6) is set. There are no restrictions as to when this register can be read.

The following paragraphs describe the operation of this register in both modes.

CHS Mode:

In CHS mode, this register contains the low byte of the 16-bit Cylinder Number for the current PIO or DMA operation. During a non-automated PIO or DMA operation, the Cylinder Low and Cylinder High registers are updated by the microprocessor when appropriate. During an automated multi-sector PIO or DMA operation, the Cylinder Number is automatically incremented by the hardware every time the Head Number wraps to 0, so that when the transfer is completed, the Cylinder Low and Cylinder High registers will reflect the Cylinder Number for the last sector transferred.

LBA Mode:

In LBA mode, this register contains logical block address bits A15:A8. At the end of the command, this register is updated to reflect the current LBA bits A15:A8. It will increment as required.

A5 MICRO. AT CYLINDER HIGH REGISTER (A5h (A4h), R/W, M_CYLHI)

7:0 (R/W) (M_CYLHI[7:0]) - MICRO. AT CYLINDER HIGH REGISTER: The usage of this register is dependent upon the Enable LBA Mode bit (ENLBAMODE, reg. C3h, R/W, bit 3) and the LBA bit (reg. 1F6h, bit 6). CHS (Cylinder/Head/Sector) mode of operation is used when the ENLBAMODE bit is cleared. LBA (Logical Block Mode) mode of operation is used when the ENLBAMODE bit is set and the LBA bit (reg. 1F6h, bit 6) is set. This register is the local microprocessor's window into the AT Host Cylinder High register (reg. 1F5h, R/W). This register can only be written while AT BUSY (reg. CEh, R, bit 6) is set. There are no restrictions as to when this register can be read.

The following paragraphs describe the operation of this register in both modes.

CHS Mode:

In CHS mode, this register contains the high byte of the 16-bit Cylinder Number for the current PIO or DMA operation. During a non-automated PIO or DMA operation, the Cylinder Low and Cylinder High registers are updated by the microprocessor when appropriate. During an automated multi-sector PIO or DMA operation, the Cylinder Number is automatically incremented by the hardware every time the Head Number wraps to 0, so that when the transfer is completed, the Cylinder Low and Cylinder High registers will reflect the Cylinder Number for the last sector transferred.

LBA Mode:

In LBA mode, this register contains logical block address bits A23:A16. At the end of the command, this register is updated to reflect the current LBA bits A23:A16. It will increment as required.

A6 MICRO. AT DRIVE/HEAD REGISTER (A6h, R/W, M_DRVHD)

The usage of this register is dependent upon the Enable LBA Mode bit (ENLBAMODE, reg. C3h, R/W, bit 3) and the LBA bit (reg. 1F6h, bit 6). CHS (Cylinder/Head/Sector) mode of operation is used when the Enable LBA Mode bit is cleared. LBA (Logical Block Mode) mode of operation is used when the Enable LBA mode bit is set and the LBA bit (reg. 1F6h, bit 6) is set. This register is the local microprocessor's window into the AT Host Drive/Head register (reg. 1F6h, R/W). The bits in this register are automatically reset when an Execute Drive Diagnostics command (90h) is received from the Host. This register can only be written while AT BUSY (reg. CEh, R, bit 6) is set. There are no restrictions as to when this register can be read.

The following paragraphs describe the operation of this register as a function of the Enable LBA Mode bit.

Enable LBA Mode bit (reg. C3h, R/W, bit 3) cleared:

7:5 (R/W) (PASS[2:0]) - PASS-THRU BITS [2:0]: These are pass through bits used between the Host and microprocessor.

4 (R/W) (DRV) - DRIVE NUMBER SELECT: When this bit is set to 1, Drive 1 is selected. When this bit is reset to 0, Drive 0 is selected. This bit is reset to 0 when the Host Software Reset bit (reg. 3F6h, W, bit 2) is asserted by the Host.

3:0 (R/W) (HEAD_SEL[3:0]) - HEAD NUMBER SELECT: These bits contain the head number for the current PIO or DMA operation. During a non-automated PIO or DMA operation, these bits are updated by the microprocessor when appropriate. During an automated multi-sector PIO or DMA operation, these bits are automatically incremented by the hardware every time the Sector Number wraps to 1, so that when the transfer is completed, these bits will reflect the Head Number for the last sector transferred. When auto-incremented from the Maximum Head Number (MAXHEAD, reg. B3h, R/W), the Head Number wraps to 0 and the Cylinder Number is auto-incremented.

Enable LBA Mode bit (reg. C3h, R/W, bit 3) set:

7 (R/W) Reserved. This bit must be set to 1 per the ATA specification.

6 (R/W) (LBA) - LBA MODE: When set, this bit indicates that the Task File registers will be utilized in the LBA mode. When cleared, the Task File registers will be used in the CHS mode.

5 (R/W) Reserved. This bit must be set to 1 per the ATA specification.

4 (R/W) (DRV) - DRIVE NUMBER SELECT: When this bit is set to 1, Drive 1 is selected. When this bit is reset to 0, Drive 0 is selected. This bit is reset to 0 when the Host Software Reset bit (reg. 3F6h, W, bit 2) is asserted by the Host.

3:0 (R/W) (HEAD_SEL[3:0]) - HEAD NUMBER SELECT[3:0]: These bits contain the high order bits of the logical block address (A27:A24). At the end of the command, this register is updated to reflect the current LBA bits A27:A24.

A7 MICROPROCESSOR AT COMMAND REGISTER (A7h, R/W, M_CMD)

7:0 (R/W) (M_CMD[7:0]) - MICRO. AT COMMAND [7:0]: This register holds the latest command issued to the disk controller by the Host. Refer to the ATA specification for a definition of the command codes. When the microprocessor writes to this register, the modes internally decoded from the command are updated. However, unlike Host writes to this register, the Selection Phase Detected status/interrupt (reg. C8h, R, bit 2) bit is not set, and the Busy status to the host (reg. 1F7h, R, bit 7) is not set nor are any Auto Read/ Write commands initiated unless the ENAUTOMPU control bit (reg. C0h, R/W, bit 7) is set. This register is the local microprocessors window into the AT Host Command register (reg. 1F7h, W). This register can only be written while AT BUSY (reg. CEh, R, bit 6) is set. There are no restrictions as to when this register can be read.

A8 SECTOR COUNT IMAGE REGISTER (A8h, R, I_SECCNT)

7:0 (R) (I_SECCNT[7:0]) - SECTOR COUNT IMAGE [7:0]: This register reflects the contents loaded by the host or local microprocessor into the AT Host Sector Count register (reg. 1F2h, R/W), and is not affected by automatic hardware updates of that register or local microprocessor updates utilizing the Update Host Count bit (reg. C6h, R/W, bit 5). This register is loaded when the AT Command Register (reg. 1F7h/177h, W) is loaded with a valid command. The valid command is qualified with drive number in master/slave environment.

A9 SECTOR NUMBER IMAGE REGISTER (A9h, R, I_SECNUM)

7:0 (R) (I_SECNUM[7:0]) - SECTOR NUMBER IMAGE [7:0]: This register reflects the contents loaded into the AT Host Sector Number register (reg. 1F3h, R/W) by either the host or the local microprocessor, and is not affected by automatic hardware updates of that register or local microprocessor updates utilizing the Update Host Count bit (reg. C6h, R/W, bit 5). This register is loaded when the AT Command Register (reg. 1F7h/177h, W) is loaded with a valid command. The valid command is qualified with drive number in master/slave environment

AA CYLINDER LOW IMAGE REGISTER (AAh (ABh), R, I_CYLLO)

7:0 (R) (I_CYLLO[7:0]) - CYLINDER LOW IMAGE [7:0]: This register reflects the contents loaded into the AT Host Cylinder Low register (reg. 1F4h, R/W) by either the host or the local microprocessor, and is not affected by automatic hardware updates of that register or local microprocessor updates utilizing the Update Host Count bit (reg. C6h, R/W, bit 5). This register is loaded when the AT Command Register (reg. 1F7h/177h, W) is loaded with a valid command. The valid command is qualified with drive number in master/slave environment.

AB CYLINDER HIGH IMAGE REGISTER (ABh (AAh), R, I_CYLHI)

7:0 (R) (I_CYLHI[7:0]) - CYLINDER HIGH IMAGE [7:0]: This register reflects the contents loaded into the AT Host Cylinder High register (reg. 1F5h, R/W) by either the host or the local microprocessor, and is not affected by automatic hardware updates of that register or local microprocessor updates utilizing the Update Host Count bit (reg. C6h, R/W, bit 5). This register is loaded when the AT Command Register (reg. 1F7h/177h, W) is loaded with a valid command. The valid command is qualified with drive number in master/slave environment.

AC DRIVE/HEAD IMAGE REGISTER (ACh, R, I_DRVHD)

7:0 (R) (I_DRVHD[7:0]) - DRIVE/HEAD IMAGE [7:0]: This register reflects the contents loaded into the AT Host Drive/Head register (reg. 1F6h, R/W) by either the host or the local microprocessor, and is not affected by automatic hardware updates of that register or local microprocessor updates utilizing the Update Host Count bit (reg. C6h, R/W, bit 5). These bits are reset by the HRST (pin 33) and by the DIAG 90 command. This register is loaded when the AT Command Register (reg. 1F7h/177h, W) is loaded with a valid command. The valid command is qualified with drive number in master/slave environment.

AD START SECTOR NUMBER REGISTER (ADh, R/W, ST_SECNUM)

7:0 (R/W) (ST_SECNUM[7:0]) - START SECTOR NUMBER [7:0]: The contents of this register and the Host Sector Number register (reg. 1F3h, R/W) are compared when a read command is received while Auto Read is enabled via the various Enable Auto Read bits (reg. C2h, R/W, bits 5, 3 ,1) being set. If the two registers don't match, Auto Read execution is disabled. This register is automatically loaded with the contents of the Sector Number register (regs. A3h, 1F3h) when a valid Read command (Read Sectors, Read Multiple, Read DMA) is loaded into the AT Command Register (reg. 177h/1F7h, W). This is done to automatically load the new start in the event of a compare mismatch; this can be disabled using the "Disable Start Register Update" bit (reg. C0h, R/W, bit 4). This register is automatically updated along with the Sector Number registers (regs. A3h, 1F3h) for every sector or block transferred when Auto updates are enabled. This register is also updated for the last sector transferred, so that it holds the sector number corresponding to the sector following the last one transferred when the command is done. BUSY (reg. C1h, R/W, bit 7) must be set in order to write to this register.

The above described process takes place in either CHS mode or LBA mode.

AE START CYLINDER LOW REGISTER (AEh (AFh), R/W, ST_CYLLO)

7:0 (R/W) (ST_CYLLO[7:0]) - START CYLINDER LOW [7:0]: The contents of this register and the AT Host Cylinder Low register (reg. 1F4h, R/W) are compared when a read command is received while Auto Read is enabled via the various Enable Auto Read bits (reg. C2h, R/W, bit 5, 3, 1) being set. This register is automatically loaded with the contents of the AT Cylinder Low register (regs. A4h, 1F4h) when a valid Read command (Read Sectors, Read Multiple, Read DMA) is loaded into the AT Command Register (reg. 177h/1F7h, W). This is done to automatically load the new start in the event of a mismatch; this can be disabled using the "Disable Start Register Update" bit (reg. C0h, R/W, bit 4). If the two registers don't match, Auto read execution is disabled. This register is automatically updated along with the AT Host Cylinder Low register (reg. 1F4h, R/W) for every sector or block transferred while auto updates are enabled. This register is also updated on the last sector transferred, so that it holds the cylinder low number corresponding to the sector following the last one transferred when the command is done. BUSY (reg. C1h, R/W, bit 7) must be set in order to write to this register.

The above described process takes place in either CHS mode or LBA mode.

AF START CYLINDER HIGH REGISTER (AFh (AEh), R/W, ST_CYLHI)

7:0 (R/W) (ST_CYLHI[15:8]) - START CYLINDER HIGH [15:8]: The contents of this register and the AT Host Cylinder High register (reg. 1F5h, R/W) are compared when a read command is received while Auto Read is enabled via the Enable Auto Read bits (reg. C2h, R/W, bits 5, 3, and 1) being set. If the two registers don't match, Auto read execution is disabled. This register is automatically loaded with the contents of the AT Cylinder High register (regs. A5h, 1F5h) when a valid Read command (Read Sectors, Read Multiple, Read DMA) is loaded into the AT Command Register (reg. 177h/1F7h, W). This is done to automatically load the new start in the event of a mismatch; this can be disabled using the "Disable Start Register Update" bit (reg. C0h, R/W, bit 4). This register is automatically updated along with the AT Host Cylinder High register (reg. 1F5h, R/W) for every sector or block transferred while automatic updates are enabled. This register is also updated on the last sector transferred, so that it holds the cylinder high number corresponding to the sector following the last one transferred when the command is done. BUSY (reg. C1h, R/W, bit 7) must be set in order to write to this register.

The above described process takes place in either CHS mode or LBA mode.

B0 START DRIVE/HEAD REGISTER (B0h, R/W, ST_DRVHD)

The algorithm used to compare this register to the AT Host Drive/Head register (reg. 1F6h, R/W) differs when using CHS mode or LBA mode. The following paragraphs explain the differences.

CHS Mode:

When the Enable LBA Mode bit (reg. C3h, R/W, bit 3) is cleared, the bits in this register and bits 4:0 in the AT Host Drive/Head register (reg. 1F6h, R/W) are compared when a read command is received while Auto Read is enabled via the various Enable Auto Read bits (reg. C2h, R/W, bit 5, 3, 1). This register is automatically loaded with the contents of the AT Drive/Head register (regs. A6h, 1F6h) when a valid Read command (Read Sectors, Read Multiple, Read DMA) is loaded into the AT Command Register (reg. 177h/1F7h, W).

This is done to automatically load the new start in the event of a mismatch; this can be disabled using the "Disable Start Register Update" bit (reg. C0h, R/W, bit 4). If the two registers don't match, Auto Read execution is disabled. This register is automatically updated along with the AT Host Drive/Head register (reg. 1F6h, R/W) for every sector or block transferred while auto updates are enabled. This register is also updated on the last sector transferred, so that it holds the drive and head numbers corresponding to the sector following the last one transferred when the command is done. BUSY (reg. C1h, R/W, bit 7) does not have to be set in order to write to this register.

7:5 (R/W) (PASS[2:0]) - PASS-THRU BITS [2:0]: These are pass through bits used between the Host and microprocessor.

4 (R/W) (STDRV) - START DRIVE NUMBER SELECT: When set, this bit specifies Drive 1 as the drive to be used as the comparison for an Auto Read operation.

3:0 (R/W) (STHS[3:0]) - START HEAD NUMBER SELECT[3:0]: These bits specify the starting head number to be used as the comparison for an Auto Read operation.

LBA Mode:

When the Enable LBA Mode bit (reg. C3h, R/W, bit 3) is set and the LBA bit (reg. 1F6h, bit 6) is set, the bits in this register and bits 7:0 in the AT Host Drive/Head register (reg. 1F6h, R/W) are compared when a read command is received while Auto Read is enabled via the various Enable Auto Read bits (reg. C2h, R/W, bit 5, 3, 1). This register is automatically loaded with the contents of the AT Drive/Head register (reg. A6h, 1F6h) when a valid Read command (Read Sectors, Read Multiple, Read DMA) is loaded into the AT Command Register (reg. 177h/1F7h, W). This is done to automatically load the new start in the event of a mismatch; this can be disabled using the "Disable Start Register Update" bit (reg. C0h, R/W, bit 4). If the two registers don't match, Auto Read execution is disabled. The LBA A27:A24 bits in this register are automatically updated along with the AT Host Drive/Head register (reg. 1F6h, R/W) for every sector or block transferred while auto updates are enabled. The LBA A27:A24 bits in this register are also updated on the last sector transferred, so that it holds the LBA corresponding to the sector following the last one transferred when the command is done. BUSY (reg. C1h, R/W, bit 7) does not have to be set in order to write to this register.

7 (R/W) Reserved. Must be set to 1 to comply with the ATA specification.

6 (R/W) (LBA MODE) - Must be set to 1 for LBA mode, or 0 for non-LBA mode, to comply with the ATA specification.

5 (R/W) Reserved. Must be set to 1 to comply with the ATA specification.

4 (R/W) (STDRV) - START DRIVE NUMBER SELECT: When set, this bit specifies Drive 1 as the drive to be used as the comparison for an Auto Read operation.

3:0 (R/W) (LBA A27:A24) - LOGICAL BLOCK ADDRESS A27:A24: These bits specify the starting head number to be used as the comparison for an Auto Read operation.

B1 MAXIMUM SECTOR NUMBER DRIVE 0 REGISTER (B1h, R/W, MAXSEC_0)

7:0 (R/W) (MAXSEC_0[7:0]) - MAXIMUM SECTOR NUMBER DRIVE 0[7:0]: While operating in the CHS mode, these bits specify the maximum value to which the Sector Number (reg. A3h, R/W) will auto-increment when the Drive Number (reg. A6h, bit 4) is 0. If the Sector Number is auto-incremented when it equals MAXSEC_0, it will wrap back to 1 and the Head Number (reg. A6h, R/W, bits 3:0) will be auto-incremented. If LBA mode is in use, this register is not used in any compares for incrementing.

B2 MAXIMUM SECTOR NUMBER DRIVE 1 REGISTER (B2h, R/W, MAXSEC_1)

7:0 (R/W) (MAXSEC_1[7:0]) - MAXIMUM SECTOR NUMBER DRIVE 1[7:0]: While operating in the CHS mode, these bits specify the maximum value to which the Sector Number (reg. A3h, R/W) will auto-increment when the Drive Number (reg. A6h, bit 4) is 1. If the Sector Number is auto-incremented when it equals MAXSEC_1, it will wrap back to 1 and the Head Number (reg. A6h, R/W, bits 3:0) will be auto-incremented. If LBA mode is in use, this register is not used in any compares for incrementing.

B3 MAXIMUM HEAD NUMBER REGISTER (B3h, R/W, MAXHEAD)

7:4 (R/W) (MAXHEAD_1[3:0] - MAXIMUM HEAD NUMBER DRIVE 1[3:0]: While operating in the CHS mode, these bits specify the maximum value to which the Head Number (reg. A6h, R/W, bits 3:0) will auto-increment if the Drive Number (reg. A6h, bit 4) is 1. If the Head Number is auto-incremented when it equals MAXHEAD_1, it will wrap back to 0 and the Cylinder Number registers (regs. A4h/A5h, R/W) will be appropriately auto-incremented. If LBA mode is in use, this register is not used in any compares for incrementing.

3:0 (R/W) (MAXHEAD_0[3:0]) - MAXIMUM HEAD NUMBER DRIVE 0 [3:0]: While operating in the CHS mode, these bits specify the maximum value to which the Head Number (reg. A6h, R/W, bits 3:0) will auto-increment if the Drive Number (reg. A6h, bit 4) is 0. If the Head Number is auto-incremented when it equals MAXHEAD_0, it will wrap back to 0 and the Cylinder Number registers (regs. A4h/A5h, R/W) will be appropriately auto-incremented. If LBA mode is in use, this register is not used in any compares for incrementing.

B4 DRIVE 0 STATUS REGISTER (B4h, R/W, DRV0STAT)

This register contains drive-related control and status information that is part of the H_STAT (reg. 1F7h, R), H_DVCTL (reg. 3F6h, W), and H_DRVADD (reg. 3F7h, R) registers when Disk Drive 0 is selected (i.e. Drive Number Select (reg. A6h, R/W, bit 4) is cleared). If master/slave mode is physically implemented with two drives, this register is used for accessing drive 0 and drive 1 status. In this mode, the Master/Slave Enable bit (reg. C0h, R/W, bit 1) is set. If master/slave mode is logically implemented on one drive, this register is used for accessing drive 0 status only. These bits are reset by the HRST (pin 33), and *POR.

7:3 (R/W) Reserved

2 (R/W) (DRDY0) - DRIVE 0 READY: This bit determines the state of the Drive Ready bit (reg. 1F7h, R, bit 6) while Drive 0 is selected.

1 (R/W) (DWF0) - DRIVE 0 WRITE FAULT: This bit determines the state of the Drive Write Fault bit (reg. 1F7h, R, bit 5) while Drive 0 is selected.

0 (R/W) (DSC0) - DRIVE 0 SEEK COMPLETE: This bit determines the state of the Drive Seek Complete bit (reg. 1F7h, R, bit 4) while Drive 0 is selected.

B5 DRIVE 1 STATUS REGISTER (B5h, R/W, DRV1STAT)

This register contains drive-related control and status information that is part of the H_STAT (reg. 1F7h, R), H_DVCTL (reg. 3F6h, W), and H_DRVADD (reg. 3F7h, R) registers when Disk Drive 1 is selected (i.e. Drive Number Select (reg. A6h, R/W, bit 4) is set. If master/slave mode is logically implemented on one drive, this register is used for accessing drive 1 status. This register is not used for Drive 1 status if master/slave mode is physically implemented with two drives. These bits are reset by the HRST (pin 33), and *POR.

7:3 (R/W) Reserved

2 (R/W) (DRDY1) - DRIVE 1 READY: This bit determines the state of the Drive Ready bit (reg. 1F7h, R, bit 6) while Drive 1 is selected.

1 (R/W) (DWF1) - DRIVE 1 WRITE FAULT: This bit determines the state of the Drive Write Fault bit (reg. 1F7h, R, bit 5) while Drive 1 is selected.

0 (R/W) (DSC1) - DRIVE 1 SEEK COMPLETE: This bit determines the state of the Drive Seek Complete bit (reg. 1F7h, R, bit 4) while Drive 1 is selected.

B6 HOST BLOCK SIZE REGISTER (B6h, R/W, HBLKSIZE)

7:0 (R/W) (HBLKSIZE[7:0]) - HOST BLOCK SIZE [7:0]: This register is loaded with the number of sectors per block corresponding to the required amount to support Write Multiple or Read Multiple commands. A value of 00h in this register is undefined and will result in incorrect operation of Read Multiple and Write Multiple commands.

B7 HOST BLOCK COUNTER REGISTER (B7h, R, HBLKCTR)

7:0 (R) (HBLKCTR[7:0]) - HOST BLOCK COUNTER [7:0]: The Host Block Counter is an eight-bit counter that counts sectors within a block during execution of a Write Multiple or Read Multiple command. This counter gets loaded with the contents of the Host Block Size register (reg. B6h, R/W) prior to the beginning of a block transfer for Write Multiple or Read Multiple commands and then decrements.

B9 HOST TIMER REGISTER (B9h, R, HTIMER)

7:0 (R) (HTIMER[7:0]) - HOST TIMER [7:0]: The Host Timer is a down counter which is used during an automatic multi-sector PIO operation and at the start of an Auto read operation. Refer to the definitions for the HBSYTIME (reg. BAh, W) and HIRQTIME (reg. BBh, W) registers for more detail.

BA BUSY TIME REGISTER (BAh, W, BSYTIME)

7:0 (W) (HBSYTIME[7:0]) - HOST BUSY TIME [7:0]: The contents of this register is loaded into the Host Timer (HTIMER, reg. B9h, R) during an automatic multi-sector PIO operation or at the start of an Auto read PIO operation when the Busy bit (reg. 1F7h, R, bit 7) is set after a host command is received or after a sector has been transferred, except for the last sector. The contents of this register determines the time that the AIC-8375 waits before resetting the Busy bit and asserting the DRQ bit and IRQ pin in preparation for transfering the next sector. The use of the Busy Timer is also governed by the IRQMODE[1:0] bits (reg. C4h, R/W, bits 1:0).

The timer period is determined by the equation:

$$\text{Timer Period} = 16 \bullet \text{BSYTIME} \bullet T_{BUFCLK}$$

A value of 0 in this register implies no waiting before resetting the Busy bit (reg. 1F7h, R, bit 7). The following table shows the HBSYTIME resolution and maximum values for different BUFCLK frequencies:

fBUFCLK	HBSYTIME Resolution	Maximum HBSYTIME
16MHz	1000 ns	255 us
24MHz	667 ns	170 us
32MHz	500 ns	127 us
40MHz	400 ns	102 us

BB HOST INTERRUPT TIME REGISTER (BBh, W, HIRQTIME)

7:0 (W) (HIRQTIME[7:0]) - HOST INTERRUPT TIME [7:0]: The contents of this register is loaded into the Host Timer register (reg. B9h, R) during an automatic multi-sector PIO read operation when the Host Interrupt signal (IRQ) is asserted. This is used for generating a missed IRQ time-out. The IRQ time-out bit (IRQTIM, reg. C8h, R, bit 7) will not be set if the host responds with a Data IOR cycle before the timeout occurs. The use of the Interrupt Timer is also governed by the IRQMODE[1:0] bits (reg. C4h, R/W, bits 1:0).

The time-out period is determined by the equation:

$$\text{Time Out Period} = 2048 \bullet \text{IRQTIME} \bullet T_{BUFCLK}$$

A value of 0 in this register corresponds to 0 length time-out period. The following table shows the IRQTIME resolution and maximum values corresponding to different BUFCLK frequencies:

fBUFCLK	IRQTIME Resolution	Maximum IRQTIME
16MHz	128 us	32.6 ms
24MHz	85.3 us	21.7 ms
32MHz	64 us	16.3 ms
40MHz	51.2 us	13.1 ms

BF HOST CONTROL PIN 1 REGISTER (BFh, R/W, HCP_1)

7 (R/W) Reserved

6 (R/W) (*PDIAGO) - *PDIAG PIN: This bit determines the output state of the *PDIAG signal pin at all times. When set, the *PDIAG signal pin will be in a high impedance state. When this bit is cleared, the *PDIAG pin will be driven low. This bit is set by a Host Programmed Reset, the HRST pin asserted by the host, or receipt of an Execute Drive Diagnostics command from the Host. When read, this bit reflects the state of the *PDIAG pin.

5 (R/W) (*DASPO/*SPKR) - *DASP PIN (ATA Mode) / *SPKR or BVD2 PIN (PCMCIA Mode): This bit determines the output state of the *DASP signal pin at all times. When set, the *DASP signal pin will be in a high impedance state. When cleared, the *DASP signal pin will be driven low. This bit is also set by a Host Programmed Reset (Soft Reset) or when the HRST pin is asserted by the host. When read, this bit reflects the state of the *DASP pin. In PCMCIA mode, this bit controls the state of the *SPKR or BVD2 pin. When in I/O mode (reg. 200h, R/W, Configuration Index is ***not*** zero), this signal is *SPKR. When in memory mode (reg. 200h, R/W, Configuration Index ***is*** zero), this signal is BVD2 and should be set high.

4:0 (R/W) Reserved

C0 HOST CONTROL 0 REGISTER (C0h, R/W, HCTL_0)

7 (R/W) (ENAUTOMPU) - ENABLE AUTOMATIC LOCAL MPU COMMANDS: If this bit is cleared, the local microprocessor can't start an Auto Command (defined by the bits in the Host Control 2 register (reg. C2h, R/W)) by loading the Micro. AT Command register (reg. A7h, R/W). While this bit is set, any load of the Micro. AT Command register with a command which has been enabled for Auto execution, will result in the Auto execution of that command.

6 (R/W) (DISAUTOUPD) - DISABLE AUTOMATIC COMMAND BLOCK UPDATE: When this bit is set, the Host Transfer State Machine will not automatically update the task file registers during command execution. This bit should only be set when complete manual transfer mode is required.

5 (R/W) (ENRDVERUPD) - ENABLE READ VERIFY COMMAND AUTOMATIC TASK FILE UPDATE: When this bit is set, task file registers are updated on every good sector transferred from disk to buffer for Read Verify command. When reset, automatic update function is disabled.

4 (R/W) (DSBLSTUPD) - DISABLE START REGISTER UPDATE: When this bit is set the Start Registers are not updated during the load or execution of a Read Command. This bit is set when the Read Cache is static.

3 (R/W) (HCS1SEL) - HCS1 SELECT: When this bit is set, the HA9/*HCS1 pin is configured as the active low Host Chip Select 1 input from the AT bus. When this bit is cleared, the HA9/*HCS1 pin is configured as the input for bit 9 of the Host address. This bit must be cleared for a PCMCIA interface.

2 (R/W) (SLAVEMODE) - SLAVE MODE: When this bit is set, the chip is configured for Slave mode. When this bit is reset, the chip is configured for Master mode. This bit is only valid if the MSEN bit (reg. C0h, R/W, bit 1) is set.

1 (R/W) (MSEN) - MASTER/SLAVE ENABLE: When this bit is set, Master/Slave mode is enabled. In this case, the drive will respond as Master or Slave depending upon the state of the SLAVEMODE bit described above. If cleared, the drive will respond as both drive 0 and drive 1.

0 (R/W) Reserved

C1 HOST CONTROL 1 REGISTER (C1h, R/W, HCTL_1)

7 (R/W) (SETBSY/IBSY) - SET BUSY/INTERNAL BUSY LATCH: If this bit is set by the local microprocessor, the internal BUSY latch is set. Writing a '0' to this bit has no affect on the BUSY latch. Writing a '1' to this bit sets the BUSY latch regardless of whether RSTBSY (reg. C1h, R/W, bit 6) is set or not.

This bit is set if the HRST pin is asserted or if the Host Programmed Reset bit (reg. 3F6h, W, bit 2) is set.

This bit is also set when the host writes to the Host Command register (reg. 1F7h, W) while one of the following conditions is true:

- Master/Slave mode is disabled when the Master/Slave Enable bit (reg. C0h, R/W, bit 1) is cleared.
- Master/Slave mode is enabled when the Master/Slave Enable bit (reg. C0h, R/W, bit 1) is set and the corresponding drive is selected (i.e. SLAVEMODE=0 in HCTL_0 (reg. C0h, R/W, bit 2) and DRV=0 in M_DRVHD (reg. A6h, R/W, bit 4), or SLAVEMODE=1 and DRV=1).
- The command written by the host is the Execute Drive Diagnostics (90h) command.

This bit is cleared either automatically or by the microprocessor (via writing to bit 6 below) after a command is done. It is cleared on the first data word of the block transferred except during a Read Long Command where it is cleared on the first ECC byte transferred.

6 (R/W) (RSTBSY/BTRANS) - RESET BUSY/BUFFER TRANSFER: This bit is set during transfers between buffer memory and the host. It is set whenever a transfer between the Host and the buffer can occur. It is essentially coincident with DRQ on AT write operations. During Auto Write command execution with Automatic Multi Sector Transfer enabled, this bit will be negated for a short time between the first and second sectors. It is reset when the last byte is transferred to the host during a read operation or to the buffer memory during a write operation.

NOTE: When writing to this register, the states of bits 7:6 will have the following effects:

Bit 7	Bit 6	Function
0	0	NOP
0	1	Reset bit 7
1	0	Set Bit 7
1	1	Set bit 7 (unreliable - illegal action)

Writing a one to this bit, while SBSY is not set, will reset the internal Busy latch. Writing a zero to this bit has no affect.

5 (R/W) (CDATA) - CORRECTED DATA: This bit is the same as the Corrected Data bit (reg. 1F7h, R, bit 2). It is set by the microprocessor when, on the previous read sector transfer, an ECC error was detected and corrected. This bit is automatically reset when the host writes to the H_CMD register (reg. 1F7h, W). This bit is also cleared when the host has read the sector worth of data and read the Host Status register (reg. 1F7h, R) with its CDATA bit set.

4 (R/W) (IRQ) - HOST INTERRUPT REQUEST: This bit controls the IRQ output pin to the host. The microprocessor can only set this bit. This bit is cleared when the host reads the Host Status register (reg. 1F7h, R). This bit is read back as a 1 when the IRQ pin is asserted - either active low or active high.

3 (W) (RSTIRQ) - RESET HOST INTERRUPT REQUEST: When this bit is set, the IRQ signal will be reset. This bit does not have to be loaded with a '0' before using again.

2 (R/W) (ONEBLK) - STOP AFTER ONE BLOCK: When this bit is set, all sector based write commands which have been enabled for Auto Command execution, will be stopped after one sector has been transferred. Likewise, a Write Multiple command which has been enabled for Auto Command execution will stop after one block of sectors have been transferred. This bit applies only to PIO or DMA Auto Write commands and does not apply to the Start or Restart of automatic multiple sector transfers.

1 (R) (IEN_ST) - INTERRUPT ENABLE STATUS (active low): This ***read only*** bit reflects the state of the *IEN bit (reg. 3F6h, W, bit 1).

0 (R/W) (HERROR) - HOST ERROR: This is the same as the Error bit (reg. 1F7h, R, bit 0). It is set by the microprocessor when a command error occurs. It is also automatically set along with the Abort bit (reg. A0h, R/W, bit 2) if the Enable Auto Error bit (reg. C3h, R/W, bit 5) is set and the Host Port Check Error bit (reg. 106h, R, bit 0) or the Host FIFO Error bit (reg. C8h, R, bit 1) is set.

This bit will remain set as long as ENAUTOERR=1 and HCHKERR or HFIFOERR is set, so that HCHKERR and HFIFOERR must be cleared before the microprocessor attempts to clear this bit. This bit is automatically cleared when the host writes to the Command register (H_CMD, reg. 1F7h, W).

C2 HOST CONTROL 2 REGISTER (C2h, R/W, HCTL_2)

7 (R/W) (ENMULXFR) - ENABLE AUTOMATIC MULTI SECTOR TRANSFER: When this bit is set, multi-sector ATA PIO or ATA DMA transfers will be performed automatically by the hardware, and no microprocessor intervention will be required between sectors or blocks. Transfer will continue until the AT Host Sector Count register (reg. 1F2h, R/W) decrements to 0. The HIRQTIME (reg. BBh, R/W) and HBSYTIME (reg. BAh, R/W) registers should be initialized to the desired values before this bit is set. The IRQ timing algorithm used while this mode is enabled is also governed by the IRQMODE[1:0] bits (reg. C4h, R/W, bits 1:0).

If the current command in the AT Host Command register (reg. 1F7h, W) is a Write Long, Write Buffer, Write Same, Read Verify, Read Long, Read Buffer, or Format command, the hardware defaults to single sector operation regardless of the state of this bit.

6 (R/W) (ENAUTOWR) - ENABLE AUTO WRITE: Setting this bit enables the automatic start of execution of Write commands. When this bit is set to 1, command execution will start automatically for the Write Sector, Write Long, Write Buffer, and Format commands. Automatic execution for more than one sector requires the Enable Automatic Multi Sector Transfer bit (reg. C2h, R/W, bit 7) to be set. When one of the above Auto Commands are received, the HWRITE bit (reg. C3h, R/W, bit 7) is set.

5 (R/W) (ENAUTORD) - ENABLE AUTO READ: Setting this bit enables the automatic start of execution of a Read Sector command. Auto Read execution will start only if the Sector, Head, Cylinder and Drive numbers specified by the host match the contents of the ST_SECNUM (reg. ADh, R/W), ST_DRVHD (reg. B0h, R/W), ST_CYLLO (reg. AEh, R/W) and ST_CYLHI (reg. AFh, R/W) registers. If there is a match, then the Host data path will be automatically enabled and the HWRITE bit (reg. C3h, R/W, bit 7) will be automatically cleared. Following the above actions, the sending of data to the host will take place when the Buffer is ready. Upon successful completion of the read operation, the ST_SECNUM, ST_DRVHD, ST_CYLLO and ST_CYLHI registers will be updated to point to the sector following the last one transferred.

This bit is cleared if a read data transfer is aborted, ie. if a new command is received between the start of a transfer (or restart) and the Host Transfer Done condition with SECCNT (reg. 1F2h, R) equal to zero, or if an enabled Auto Write Command is received.

4 (R/W) (ENAUTOWDMA) - ENABLE AUTO WRITE DMA: When this bit is set, Auto Write execution of a Write DMA command is enabled as per the description for the ENAUTOWR bit in this register. When this bit is reset, Auto execution of Write DMA commands is disabled.

3 (R/W) (ENAUTORDMA) - ENABLE AUTO READ DMA: When this bit is set, Auto Read execution of a Read DMA command is enabled. When this bit is reset, Auto execution of Read DMA commands is disabled. Auto execution of a Read DMA command is subject to the same conditions as those for a Read Sector command, as described for the ENAUTORD bit in this register. This bit is cleared if a read data transfer is aborted, i.e. if a new command is received between the start of a transfer (or restart) and the Host Transfer Done condition while SECCNT (reg. 1F2h, R) is equal to zero, or if an enabled Auto Write Command is received.

2 (R/W) (ENAUTOWM) - ENABLE AUTO WRITE MULTIPLE COMMAND EXECUTION: When this bit is set, Auto Write execution is enabled for Write Multiple host commands. When this bit is reset, Auto Write execution is disabled for Write Multiple host commands.

1 (R/W) (ENAUTORM) - ENABLE AUTO READ MULTIPLE COMMAND EXECUTION: When this bit is set, Auto Read execution is enabled for Read Multiple host commands. When this bit is reset, Auto Read execution is disabled for Read Multiple host commands. Auto execution of a Read Multiple command is subject to the same conditions as those for a Read Sector command, as described for the ENAUTORD bit in this register. This bit is cleared if a read data transfer is aborted, i.e. if a new command is received between the start of a transfer (or restart) and the Host Transfer Done condition while SECCNT (reg. 1F2h, R) is equal to zero, or if an enabled Auto Write Command is received.

0 (R/W) (ENAUTOWVS) - ENABLE AUTO WRITE VERIFY AND SAME: When this bit is set, Auto Write execution is enabled for the Write Verify and Write Same commands.

C3 HOST CONTROL 3 REGISTER (C3h, R/W, HCTL_3)

7 (R/W) (HWRITE) - HOST WRITE OPERATION: This bit determines the direction the data transfer for host data transfer commands. It is automatically set when any ATA defined write type commands (Write Sectors, Write DMA, Write Multiple, Write Long, Write Same, Write Verify, Write Buffer, or Format) is loaded into the H_CMD or M_CMD registers (reg. 1F7h, reg. A7h). It is automatically reset when any defined ATA read command (Read Sectors, Read DMA, Read Multiple, Read Long, Read Verify, Identify Drive, or Read Buffer) is loaded into the H_CMD or M_CMD registers.

The automatic setting and resetting of this bit can be overridden by writing any command code not identified above into the M_CMD registers and then writing to this bit. For any other "vendor unique" read or write command, this bit must be manually configured.

A new command will not set/reset HWRITE if CMDABORT (reg. CAh, R/W, bit 4) is set, but HWRITE will be set/reset when the current host-buffer access is finished.

6 (R/W) Reserved

5 (R/W) (ENAUTOERR) - ENABLE AUTO ERROR SET: While this bit is set, a Host Port Check Error (reg. 106h, R, bit 0), Host FIFO error (reg. C8h, R, bit 1), or an Auto Write Overrun error (reg. CAh, R, bit 3) will automatically set the AT Error bit (reg. 1F7h, R, bit 0) and the Abort bit (reg. 1F1h, R, bit 1). If the current operation is a read, the internal Busy latch is cleared on the next data transfer strobe. At the end of the sector or block currently being transferred, the overall transfer will be stopped and the XFRDONE Interrupt bit (reg. C8h, R/W, bit 0) is set if the ENAUTOPAUSE bit in this register is also set.

4 (R/W) (ENAUTOPAUSE) - ENABLE AUTO PAUSE ON ERROR: When this bit is set, the automated host data transfer is paused when any of the following four bits are set; the Error bit (reg. C1h, R/W, bit 0), the Host FIFO error bit (reg. C8h, R, bit 1), the AUTOWROVRN bit (reg. CAh, R, bit 3), and the HCHKERR bit (reg. 106h, R, bit 0). When the HERROR bit (reg. C0h, R/W, bit 0) is set, data transfer is always paused.

3 (R/W) (ENLBAMODE) - ENABLE LBA MODE: When set, this bit configures the Task File registers and Start registers (regs. A3h -A6h, and ACh-AFh) for operation in LBA mode or CHS mode determined by the LBA bit (reg. 1F6h, R, bit 6). While this bit is cleared, the Task File registers and the Start registers function only in CHS mode.

2 (R/W) (STARTXFR) - START AT TRANSFER: Setting this bit while the SECCNT register (reg. 1F2h, R) is not equal to 00h and there is no Buffer No Room condition, will start a host data transfer. The transfer will not start if the SECCNT register is equal to 00h. When a write transfer is started, the IRQ signal pin and bit (reg. BFh, R, bit 3) is not automatically set. To automatically set the IRQ signal pin for a write transfer start, use the RESTARTXFR bit (bit 1 of this register). When a read transfer is started, the Busy Timer is used to establish when the IRQ pin and bit and the DRQ bit (reg. 1F7h, R, bit 3) will be asserted. When a write transfer is started, the Busy Timer is not used. This bit is always read back as 0 and it does not have to be cleared after writing a 1 to it. This STARTXFR bit and the RESTARTXFR bit must not be set at the same time.

This bit can also be used to start a host sector transfer when a command has been received and it is desired to execute it without automation. In the case of a one sector read command, the Task File registers will have been manually decremented to zero prior to the transfer start time. Even though the SECCNT register is zero, setting this bit will start the transfer in this specific case. This bit can be used to start PIO or DMA commands.

1 (R/W) (RESTARTXFR) - RESTART AT TRANSFER: Setting this bit while the SECCNT register (reg. 1F2h, R) is not equal to 00h and there is no Buffer No Room condition, will start a host data transfer. The transfer will not start if the SECCNT register is equal to 00h. When a write transfer is restarted, the IRQ signal pin and bit (reg. BFh, R, bit 3) are automatically set. To start the write transfer without the IRQ signal pin and bit being set, use the STARTXFR bit (bit 2 of this register) to start the write transfer. When a read or write transfer is restarted, the Busy Timer will be used to establish when the IRQ pin and bit and the DRQ bit (reg. 1F7h, R, bit 3) will be asserted. This bit is always read back as 0, and it does not have to be cleared after writing a 1 to it. This RESTARTXFR bit and the STARTXFR bit must not be set at the same time. This bit can be used to restart PIO or DMA commands.

0 (R/W) (PAUSEHXFR) - PAUSE HOST TRANSFER: Setting this bit will cause the currently automated host read or write transfer to pause. If the current command is a Read or Write sector based command, the transfer will stop at the next sector boundary (after a sector has been transferred but before the next sector is started) and the XFRDONE Interrupt bit (reg. C8h, R/W, bit 0) will be set. If the current command is a Read Multiple or Write Multiple command, the transfer will stop at the next block boundary (after a block of sectors have been transferred but before the next block is started) and the XFRDONE Interrupt bit will be set. DMA or PIO commands can be paused using this bit. This bit must be cleared after the XFRDONE Interrupt bit is set.

If this bit is set when a transfer is started no transfer will occur and XFRDONE is set.

C4 HOST CONTROL 4 REGISTER (C4h, R/W, HCTL_4)

7 (R/W) (TEST_CYL) - TEST CYLINDER COUNTER: This bit is used to set the carry between the eight bit AT Cylinder Register/Counters. This enables the counter to be tested in an easier method. This bit is used only for manufacturing test of the device.

6 (R/W) (SEL_ATIMER) - SELECT ALTERNATE TIMER: When set, this bit selects BUFCLK as the clock to run the IRQ and BUSY timers. The timers will function as otherwise specified in this specification. This bit is intended only for manufacturing test purposes.

5:2 (R/W) Reserved

1:0 (R/W) (IRQMODE[1:0]) - IRQ MODE [1:0]: These bits provide the user several AT automation alternatives with respect to the IRQ timer, the BUSY timer, and host status read variations. These bits will assist the user to successfully interface to different BIOS and Device Driver implementations.

IRQMODE[1:0]	Mode Name / Description
0 0	(BUSY TIMER/IRQ TIMER ONLY): The BUSY timer is used to determine when IRQ will be asserted. The IRQ timer generates IRQTIM (IRQ time-out) in the event the IRQ generated by the BUSY timer was asserted too early and was clobbered by the host read status.
0 1	(BUSY TIMER AND HOST RD STATUS/IRQ TIMER): Both the BUSY timer and the host reading status is used to determine when IRQ will be asserted. The intention of this mode is to force the host inter-block gap to a minimum time per the Busy Timer, however, it does penalize ATA complient hosts. Certain test programs require a larger host inter-block gap to be able to see ATBUSY = 1, or they may not have the interrupt controller configured properly. After a sector is transferred, the BUSY timer is started and the device waits for the Host to read Status and also for the BUSY timer to expire at which time the next IRQ will be set. If the Host reads the Status multiple times and incorrectly clears IRQ, and fails to read the next data word before the IRQ Timer times out, IRQTIM will be generated.
1 0	(HOST READ STATUS ONLY): In this mode, IRQ will be generated based upon when the host reads the status register. This mode is the highest performance mode with the smallest host inter-block gap, but it may hang on hosts which are not ATA complient and blindly read the AT Status register (reg. 1F7h, R) when the device is attempting to set IRQ.
1 1	Reserved

C5 HOST MODE CONTROL 5 REGISTER (C5h, R/W, HCTL_5)

7 (R/W) (EN16BITOD) - ENABLE IOCS16 OPEN DRAIN: In AT mode, when set this bit configures the IOCS16 bit in the open drain mode and when cleared IOCS16 is in push/pull mode. When this bit is cleared, the IOCS16 pull-up is turned on only if the drive number is matched when in a master/slave environment. This bit is set at power-on-reset time but is always cleared when in PCMCIA mode.

6 (R/W) (HEN16BIT) - ENABLE 16-BIT HOST DATA TRANSFER: When this bit is set, data transferred to or from the host is 16 bits wide. When this bit is reset, data transferred to or from host is 8 bits wide. Note that control, status, and ECC bytes are always transferred in 8-bit mode, irrespective of the state of this bit.

5 (R/W) Reserved

4 (R/W) (ENAUTOIRQ) - ENABLE AUTO INTERRUPT: When this bit is set, the Host Interrupt signal (IRQ) is asserted while in PIO transfer mode at the initiation of a host data transfer by the microprocessor. In DMA transfer mode, auto interrupt generation is disabled regardless of the state of this bit.

3 (R/W) (PIOMODE) - PIO TRANSFER MODE ENABLE: This bit is used to select between PIO and DMA transfer modes. When this bit is set, PIO mode is selected. When this bit is a cleared, DMA mode is selected. This bit is ignored if any DMA command is loaded into the H_CMD register (regs. 1F7h, A7h) and the command will be performed in DMA mode.

2 (R/W) (AUTOWAIT) - AUTOMATIC WAIT STATE ENABLE: When this bit is set, the IOCHRDY output signal to the host will be automatically negated to generate wait states during PIO transfers when the device is not ready to send data between the host and buffer memory.

1 (R/W) Reserved

0 (R/W) (EARLYIORDY) - EARLY IOCHRDY: When this bit is set IOCHRDY is driven from address alone without decoding *IOR or *IOW asserted.

C6 HOST MODE CONTROL 6 REGISTER (C6h, R/W, HCTL_6)

7 (R/W) (RDINTLK) - READ INTERLOCK: Writing a 1 to this bit will cause an AT Read command to stop at the last host inter-block gap. For a Read Sectors command this is the last sector and for a Read Multiple command it is the last block. This bit is used to force a firmware interlock during an automatic muli-sector transfer because there is no ending status on a read command. If an Auto-Read command of 1 sector is received while this bit is set, the sector will not be transferred, and XFRDONE is asserted.

6 (R/W) (AUTORDINTLK) - ENABLE AUTO READ INTERLOCK: When this bit is set, automatic multi-sector transfer will stop at the last Inter Sector Gap only if Auto Read Command Received Interrupt (reg. C8h, R, bit 5) is generated. It does not stop if data transfers were initiated by firmware for normal read commands. But if the microprocessor clears AUTORDINTLKSTAT (bit 2 of this register) before the last Inter Sector Gap, data transfers of last sector or block continues without pause. When Read Interlock (reg. C6h, R/W, bit 7) is set, this bit is ignored.

5 (R/W) (UPDATECNT) - UPDATE HOST COUNT: The task file registers are affected in different ways depending on whether the Enable LBA Mode bit (reg. C3h, R/W, bit 3) is set or cleared.

CHS Mode:

When the Enable LBA Mode bit (reg. C3h, R/W, bit 3) is cleared or the LBA bit (reg. 1F6h, R/W, bit 6) is cleared, the Update Host Count bit will operate as follows:

Writing a 1 to this bit will cause the AT Sector Count register (reg. A2h, R/W) to be decremented. Also, if the Sector Count is not decremented to 0 (i.e. last sector has not been transferred yet), the AT Sector Number register (reg. A3h, R/W), Head Number Select bits (reg. A6h, R/W, bits 3:0) and the Cylinder Number registers (regs. A4h, A5h, R/W) will be automatically updated to point to the next sector.

LBA Mode:

When the Enable LBA Mode bit (reg. C3h, R/W, bit 3) is set and the LBA bit (reg. 1F6h, R/W, bit 6) is set, the Update Host Count bit will operate as follows:

Writing a 1 to this bit will cause the AT Sector Count register (reg. A2h, R/W) to be decremented. The Logical Block address (residing in registers A3h-A6h) will be incremented.

This bit does not have to be reset to 0, and writing a 0 to it has no effect. A read of this bit will return a zero.

4 (R/W) (HDBDRVDMA) - HOST DATA BUS DRIVE ENABLE FOR DMA TRANSFER: Writing a 1 to this bit will allow the controller to drive the HDB[15:0] pins continuously during a DMA read data transfer. This includes single and multiple word (demand mode) transfers. When this bit is reset HDB[15:0] is only driven when *IOR pin is active to the data port. When this bit is set while a read transfer is enabled (HWRITE=0, BTRANS=1) the HDB[15:0] data lines are continuously driven as long as the Data Port is addressed (*DMACK is active). Data lines are not driven when the *IOW pin is active to avoid bus contention problems.

3 (R/W) (HFIFORST) - HOST FIFO RESET: Writing a 1 to this bit resets the Host FIFO circuitry. The Host FIFO Status register (reg. CFh, R) will be cleared to zero. This bit does not have to be reset to 0, and writing a 0 to this bit has no effect. A read of this bit will return a 0.

2 (R/W) (AUTORDINTLKSTAT) - AUTO READ INTERLOCK STATUS: This bit is used along with the AUTORDINTLK bit (bit 6 of this register). This bit is automatically set when Auto Read commands are received. The microprocessor clears this bit by writing a 1 to it. If firmware clears it after being set, automatic multiple sector transfers does not stop at the last Inter Sector Gap for Auto Read commands.

1 (R/W) (ENDEMAND) - ENABLE MULTI-WORD DMA: When this bit is set, DMA transfers, when enabled, will use the Multi-Word DMA handshake. When this bit is reset, DMA transfers will use the ATA Single-Word DMA handshake protocol.

0 (R/W) (HDBDRVPIO) - HOST DATA BUS DRIVE ENABLE FOR PIO TRANSFER: Writing a 1 to this bit will allow the device to drive the HD[15:0] pins continuously during a PIO read data transfer. When this bit is cleared, the HD[15:0] pins are only driven when the *IOR pin is active with respect to the device data port. When this bit is set while a read transfer is enabled (HWRITE = 0 and BTRANS = 1), the HD[15:0] pins are continuously driven as long as the device data port is addressed (*HCS0, HA9/*HCS1, and HA[2:0] properly driven). Data lines are not driven when the *IOW pin is active to avoid bus contention problems.

C8 HOST INTERRUPT 0 STATUS REGISTER (C8h, R, HINT_0)

The status bits in this register get set and remain set when the corresponding status condition occurs. Each bit can be cleared by writing to the corresponding bit in the Host Interrupt Clear 0 register (reg. C8h, W). Also, each status bit can be enabled as an interrupt via the corresponding interrupt mask bit in the Host Interrupt Enable 0 register (reg. C9h, R/W), and by setting the EN_HOSTINT0 bit (reg. 53h, R/W, bit 0).

7 (R) (IRQTIM) - HOST INTERRUPT REQUEST TIME-OUT: This bit is set whenever a host IRQ time-out occurs during an automatic multi-sector PIO Read operation. A host IRQ time-out occurs when the host has not started to take data from the drive before the Host Interrupt Time register (reg. B9h, W) has counted down to zero (timed out).

6 (R) (AWRCMD) - AUTO WRITE COMMAND STARTED: This bit is set when automatic execution of a received ATA write command, which was enabled for Auto execution, is started.

5 (R) (ARDCMD) - AUTO READ COMMAND STARTED: This bit is set when automatic execution of a received ATA read command, which was enabled for Auto execution, is started.

4 (R) (HRSTDET) - HOST RESET DETECTED: This bit is set when the Host Reset pin (HRST) is asserted. This bit will remain set, and cannot be cleared, for the duration of the reset condition.

3 (R) (SRSTDET) - HOST SOFTWARE RESET DETECTED: This bit is set when the host has asserted the Host Soft Reset bit (reg. 3F6h, R, bit 2). This bit will remain set, and cannot be cleared, for the duration of the reset condition.

2 (R) (SELPHDET) - SELECTION PHASE DETECTED: This bit is set when the host writes to the Host Command register (H_CMD, reg. 1F7h, W) indicating that a new command has been received.

1 (R) (HFIFOERR) - HOST FIFO ERROR: This bit is set when a host FIFO overrun or underrun condition is detected during data transfers between the host and buffer.

0 (R) (XFRDN) - TRANSFER DONE: This bit is set when either a DMA or PIO transfer has completed. During automated multi-sector PIO or DMA transfers, this bit will be set after the last sector is transferred to or from the host and the Host FIFO is empty. During non-automated PIO or DMA transfers (i.e. where microprocessor intervention is required between sectors), this bit will be set after any sector is transferred to or from the host and the Host FIFO is empty. This bit will also be set after the first sector or block is transferred to the buffer during an Auto-Write Sectors command or Auto-Write Multiple command or after a transfer has been stopped by action of the Read Interlock bit (reg. C6h, R/W, bit 7). This bit is reset when the host writes to the H_CMD register (reg. 1F7h) and the command is qualified with the drive number when in a master/slave environment, or when a new sector (or block) transfer is started with the Start Transfer bit (reg. C3h, R/W, bit 2) or the Restart Transfer bit (reg. C3h, R/W, bit 1).

C8 HOST INTERRUPT CLEAR 0 REGISTER (C8h, W, HINTCLR_0)

The bits in this register are used to clear the corresponding bits in the Host Interrupt 0 Status register (reg. C8h, R).

7 (W) (CLR_IRQTIM) - CLEAR HOST INTERRUPT REQUEST TIME-OUT: When set, this bit clears the Host Interrupt Request Time-Out bit in the Host Interrupt 0 Status register (reg. C8h, R, bit 7).

6 (W) (CLR_AWRCMD) - CLEAR AUTO WRITE COMMAND STARTED: When set, this bit clears the Auto Write Command Started bit in the Host Interrupt 0 Status register (reg. C8h, R, bit 6).

5 (W) (CLR_ARDCMD) - CLEAR AUTO READ COMMAND STARTED: When set, this bit clears the Auto Read Command Started bit in the Host Interrupt 0 Status register (reg. C8h, R, bit 5)

4 (W) (CLR_HRSTDET) - CLEAR HOST RESET DETECTED: When set, this bit clears the Host Reset Detected bit in the Host Interrupt 0 Status register (reg. C8h, R, bit 4). However, the Host Reset Detected bit will remain set and not be cleared by this bit as long as the host reset condition is asserted by the host.

3 (W) (CLR_SRSTDET) - CLEAR HOST SOFTWARE RESET DETECTED: When set, this bit clears the Host Software Reset Detected bit in the Host Interrupt 0 Status register (reg. C8h, R, bit 3). However, the Host Software Reset Detected bit will remain set and not be cleared by this bit as long as the host reset condition is asserted by the host.

2 (W) (CLR_SELPHDET) - CLEAR SELECTION PHASE DETECTED: When set, this bit clears the Selection Phase Detected bit in the Host Interrupt 0 Status register (reg. C8h, R, bit 2).

1 (W) (CLR_HFIFOERR) - CLEAR HOST FIFO ERROR: When set, this bit clears the Host FIFO Error bit in the Host Interrupt 0 Status register (reg. C8h, R, bit 1).

0 (W) (CLR_XFRDN) - CLEAR TRANSFER DONE: When set, this bit clears the Transfer Done bit in the Host Interrupt 0 Status register (reg. C8h, R, bit 0).

C9 HOST INTERRUPT ENABLE 0 REGISTER (C9h, R/W, HINTEN_0)

The bits in this register have a one-to-one correspondence to the those in the Host Interrupt 0 Status register (reg. C8h, R). Setting a bit in this register will enable the corresponding status bit as an interrupt to the microprocessor if the EN_HOSTINT0 bit (reg. 53h, R/W, bit 0) is also set. Clearing a bit in this register will inhibit the interrupt for the corresponding status bit, but will have no effect on the state of that status bit.

7 (R/W) (EN_IRQTIM) - ENABLE IRQTIM INTERRUPT: When set, this bit enables the Host Interrupt Request Time-Out bit (reg. C8h, R, bit 7) to set the Interrupt Active 0 bit (reg. 52h, R, bit 0).

6 (R/W) (EN_AWRCMD) - ENABLE AWRCMD INTERRUPT: When set, this bit enables the Auto Write Command Started bit (reg. C8h, R, bit 6) to set the Interrupt Active 0 bit (reg. 52h, R, bit 0).

5 (R/W) (EN_ARDCMD) - ENABLE ARDCMD INTERRUPT: When set, this bit enables the Auto Read Command Started Interrupt bit (reg. C8h, R, bit 5) to set the Interrupt Active 0 bit (reg. 52h, R, bit 0).

4 (R/W) (EN_HRSTDET) - ENABLE HRSTDET INTERRUPT: When set, this bit enables the Host Reset Detected bit (reg. C8h, R, bit 4) to set the Interrupt Active 0 bit (reg. 52h, R, bit 0).

3 (R/W) (EN_SRSTDET) - ENABLE HOST SOFTWARE RESET DETECT INTERRUPT: When set, this bit enables the Host Software Reset Detected bit (reg. C8h, R, bit 3) to set the Interrupt Active 0 bit (reg. 52h, R, bit 0).

2 (R/W) (EN_SELPHDET) - ENABLE SELPHDET INTERRUPT: When set, this bit enables the Selection Phase Detected bit (reg. C8h, R, bit 2) to set the Interrupt Active 0 bit (reg. 52h, R, bit 0).

1 (R/W) (EN_HFIFOERR) - ENABLE HFIFOERR INTERRUPT: When set, this bit enables the Host FIFO Error bit (reg. C8h, R, bit 1) to set the Interrupt Active 0 bit (reg. 52h, R, bit 0).

0 (R/W) (EN_XFRDN) - ENABLE XFRDN INTERRUPT: When set, this bit enables the Transfer Done bit (reg. C8h, R, bit 0) to set the Interrupt Active 0 bit (reg. 52h, R, bit 0).

CA HOST INTERRUPT 1 STATUS REGISTER (CAh, R, HINT_1)

The status bits in this register get set and remain set when the corresponding status condition occurs. Each bit can be cleared by writing to the corresponding bit in the Host Interrupt Clear 1 register (reg. CAh, W). Also, each status bit can be enabled as an interrupt via the corresponding interrupt mask bit in the Host Interrupt Enable 1 register (reg. CBh, R/W) and by setting EN_HOSTINT1 (reg. 53h, R/W, bit 1).

7:5 (R) Reserved

4 (R) (CMDABORT) - HOST COMMAND ABORTED: This bit is set when the host issues another command before a current read or write data transfer is completed. A transfer is considered completed when the Busy latch (reg. C1h, R, bit 7) is cleared and BTRANS=0 (reg. C1h, R, bit 6).

3 (R) (AUTOWROVRN) - AUTO WRITE OVERRUN ERROR: This bit is set whenever the host starts writing to the Data Port (reg. 1F0h) after an Auto Write command has been issued, and is automatically starting execution, before the buffer controller is in the ready state.

2 (R) (HSTATRD) - HOST STATUS READ DETECTED: This bit is set when the host reads the Host Status register (reg. 1F7h, R). This bit is reset when the host writes to the H_CMD register (reg. 1F7h, W).

1 (R) (HSTATAFT) - HOST STATUS READ DETECTED AFTER DATA TRANSFER DONE: This bit is set the first time that the host reads the Host Status register (reg. 1F7h, R) after the Transfer Done bit (reg. C8h, R, bit 0) is set indicating that the transfer is done. This bit is reset when the host writes to the H_CMD register (reg. 1F7h, W).

0 (R) (HXFRSTART) - HOST TRANSFER STARTED: This bit is set when either a DMA or PIO transfer has started. This bit is reset when the host writes to the H_CMD register (reg. 1F7h, W).

CA HOST INTERRUPT CLEAR 1 REGISTER (CAh, W, HINTCLR_1)

The bits in this register are used to clear the corresponding bits in the Host Interrupt 1 Status register (reg. CAh, R).

7:3 (W) Reserved

4 (W) (CLR_CMDABORT) - CLEAR HOST COMMAND ABORTED: When set, this bit clears the Host Command Aborted bit in the Host Interrupt 1 Status register (reg. CAh, R, bit 4).

3 (W) (CLR_AUTOWROVRN) - CLEAR AUTOWROVRN INTERRUPT: When set, this bit clears the Auto Write Overrun bit in the Host Interrupt 1 Status register (reg. CAh, R, bit 3).

2 (W) (CLR_HSTATRD) - CLEAR HSTATRD INTERRUPT: When set, this bit clears the Host Status Read Detected bit in the Host Interrupt 1 Status register (reg. CAh, R, bit 2).

1 (W) (CLR_HSTATAFT) - CLEAR HSTATAFT INTERRUPT: When set, this bit clears the Host Status Read Detected After Data Transfer Done bit in the Host Interrupt 1 Status register (reg. CAh, R, bit 1).

0 (R) (CLR_HXFRSTART) - CLEAR HXFRSTART INTERRUPT: When set, this bit clears the Host Transfer Started bit in the Host Interrupt 1 Status register (reg. CAh, R, bit 0).

CB HOST INTERRUPT ENABLE 1 REGISTER (CBh, R/W, HINTEN_1)

The bits in this register have a one-to-one correspondence to the those in the Host Interrupt 1 Status register (reg. CAh, R). Setting a bit in this register will enable the corresponding status bit as an interrupt to the microprocessor if the EN_HOSTINT1 bit (reg. 53h, R/W, bit 3) is also set. Clearing a bit in this register will inhibit the interrupt for the corresponding status bit, but will have no effect on the state of that status bit.

7:5 (R/W) Reserved

4 (R/W) (EN_CMDABORT) - ENABLE CMDABORT INTERRUPT: When set, this bit enable the Host Command Aborted bit in the Host Interrupt 1 Status register (reg. CAh, R, bit 4) to generate the Interrupt Active 1 Bit (reg. 52h, R, bit 1).

3 (R/W) (EN_AUTOWROVRN) - ENABLE AUTOWROVRN INTERRUPT: When set, this bit enables the Auto Write Overrun bit in the Host Interrupt 1 Status register (reg. CAh, R, bit 3) to generate the Interrupt Active 1 Bit (reg. 52h, R, bit 1).

2 (R/W) (EN_HSTATRD) - ENABLE HSTATRD INTERRUPT: When set, this bit enables the Host Status Read Detected bit in the Host Interrupt 1 Status register (reg. CAh, R, bit 2) to generate the Interrupt Active 1 Bit (reg. 52h, R, bit 1).

1 (R/W) (EN_HSTATAFT) - ENABLE HSTATAFT INTERRUPT: When set, this bit enables the Host Status Read Detected After Data Transfer Done bit in the Host Interrupt 1 Status register (reg. CAh, R, bit 1) to generate the Interrupt Active 1 Bit (reg. 52h, R, bit 1).

0 (R/W) (EN_HXFRSTART) - ENABLE HXFRSTART INTERRUPT: When set, this bit enables the Host Transfer Started bit in the Host Interrupt 1 Status register (reg. CAh, R, bit 0) to generate the Interrupt Active 1 Bit (reg. 52h, R, bit 1).

CC HOST STATUS 0 REGISTER (CCh, R, HSTAT_0)

This register is the status of the Host Command register (reg. 1F7h, W) decode. All status bits change only if valid command is received. The valid command is qualified with drive number in master/slave environment.

7 (R) (RDVERIFY) - READ VERIFY COMMAND: This bit is set when the H_CMD register (reg. 1F7h, W) has been loaded with a Read Verify (40h, 41h) Command.

6 (R) (DIAGCMD90) - DIAGNOSTIC COMMAND 90: This bit is set when the Command register has been loaded with an Execute Drive Diagnostics command (90h). In addition, *PDIAG (reg. BFh, W, bit 6) will be cleared.

5 (R) (FBLSCMD) - FORMAT/BUFFER/LONG/SAME COMMAND: This bit is set when the Command register (reg. 1F7h, W) has been written with one of the following commands: Format (50h), Write Buffer (E8h), Write Long (32h, 33h), or Write Same (E9h). When this bit is set, the Enable Automatic Multi Sector Transfer bit (reg. C2h, R/W, bit 7) is disabled.

4 (R) (LONG) - READ/WRITE LONG COMMAND: This bit is set when the Command register (reg. 1F7h, W) has been loaded with a Read Long (22h, 23h) or Write Long (32h, 33h) command.

3 (R) (RWMULTICMD) - READ/WRITE MULTIPLE COMMAND: This bit is set when the Command register (reg. 1F7h, W) has been loaded with a Read Multiple (C4h) or Write Multiple (C5h) command. When this bit is set, the buffer control logic operates on block boundaries defined by the Host Blocksize register (reg. B6h, R/W), and when reset it operates on sector boundaries.

2 (R) (AUTODMA) - AUTO DMA COMMAND: This bit is set when the Command register (reg. 1F7h, W) has been loaded with a Read DMA (C8h, C9h), or Write DMA (CAh, CBh) command and those commands have previously been enabled for Auto execution. In the case of the Read DMA command, the desired read data must be present in the buffer and the Task File registers must match the Start registers (address match) before this bit is set.

1 (R) (AUTORD) - AUTO READ COMMAND: This bit is set when the Command register (reg. 1F7h, W) has been loaded with a read command that is enabled for Auto Read via the various Enable Auto Read bits (reg. C2h, R/W, bits 5, 3, 1), and the Start registers (regs. ADh, AEh, AFh, and B0h), match the corresponding AT Task File registers.

0 (R) (AUTOWR) - AUTO WRITE COMMAND: This bit is set to indicate that the Command register (reg. 1F7h, W) has been loaded with any write command that is enabled for Auto Write mode via the various Enable Auto Write bits (reg. C2h, R/W, bits 6, 4, 2, 0).

CD HOST STATUS 1 REGISTER (CDh, R, HSTAT_1)

7 (R) Reserved

6 (R) (DMACMD) - DMA COMMAND: This ***read only*** bit is set whenever a valid DMA command has been loaded and decoded in the AT Host Command register (reg. 1F7h, W). The valid command is qualified with drive number in master/slave environment.

5 (R) (HEADEQMAX) - HEAD EQUALS MAX: This ***read only*** bit is set when Head Number in the Starting register equals the Maximum Head Number, STHS[3:0] (reg. B0h, R/W, bits 3:0) = MAXHEAD[3:0] (reg. B3h, R/W, bits 3:0). This bit is not valid when the Enable LBA Mode bit (reg. C3, R/W, bit 3) is set and an LBA command is in progress.

4 (R) (SECEQMAX) - SECTOR EQUALS MAX: This ***read only*** bit is set when STSECNUM (reg. ADh, R/W) = MAXSEC (reg. B1h, R/W or reg. B2h as determined by the DRV bit in reg. 1F6h). This bit is not valid when the Enable LBA Mode bit (reg. C3, R/W, bit 3) is set and an LBA command is in progress.

3 (R) Reserved

2 (R) (STDRVHDEQ) - START DRIVE/HEAD EQUAL: This ***read only*** bit is set when STDRVHD (reg. B0h, R/W) = H_DRVHD (reg. 1F6h, R/W).

1 (R) (STCYLEQ) - START CYLINDER EQUAL: This ***read only***bit is set when STCYLLO (reg. AEh, R/W) = H_CYLLO (reg. 1F4h, R/W) and STCYLHI (reg. AFh, R/W) = H_CYLHI (reg. 1F5h, R/W).

0 (R) (STSECEQ) - START SECTOR EQUAL: This ***read only*** bit is set when STSECNUM (reg. ADh, R/W) = H_SECNUM (reg. 1F3h, R/W).

CE HOST STATUS 2 REGISTER (CEh, R/W, HSTAT_2)

7 (R) (ATDREQ) - AT DRQ: This ***read only*** bit reflects the state of the DRQ bit in the H_STAT register (reg. 1F7h, R, bit 3).

6 (R) (ATBUSY) - AT BUSY: This ***read only*** bit reflects the state of the BUSY bit in the H_STAT register (reg. 1F7h, R, bit 7).

5 (R) (HTIMEREQ0) - HOST TIMER EQUALS ZERO: This ***read only*** bit is set when the Host Timer register (reg. B9h, R) equals zero.

4 (R/W) Reserved

3 (R/W) (SECCNT8) - SECCNT REGISTER A2H BIT 8: This bit is set when the H_SECCNT register (reg. 1F2h, R/W) or the M_SECCNT register (reg. A2h, R/W) is loaded with 00h. It is cleared when the Sector Counter is decremented or when this bit is written with a 0. This bit can only be written with a 0 to clear SECCNT8 if ATBUSY is set (bit 7 of this register).

2 (R) (SECCNTEQ0) - SECTOR COUNT EQUALS ZERO: This ***read only*** bit is set when the AT Host Sector Count register (reg. 1F2h, R/W) equals zero. This bit is set when the Sector Count Register (reg. 1F2h) decrements from 1 to 0 and it is reset when a new count is loaded.

1 (R) (HBLKCTREQ0) - HOST BLOCK COUNTER EQUALS ZERO: This ***read only*** bit is set when the Host Block Counter register (reg. B7h, R) equals zero.

0 (R) (ENATDREQ) - ENABLE AT DRQ: This ***read only*** bit provides visibility to an internal device signal which is used to enable the generation of the DRQ bit in the AT Host Status register (reg. 1F7h). This bit is used only for manufacturing test of the device.

CF HOST FIFO STATUS REGISTER (CFh, R, HFSTAT)

7:6 (R) Reserved

5:0 (R) (HFCNT[5:0]) - HOST FIFO BYTE COUNT [5:0]: These ***read only*** bits indicate the number of bytes remaining in the Host FIFO. A value of 0 indicates that the FIFO is empty, and a value of 20h indicates that the FIFO is full. This register is reset to 00h whenever the Host FIFO Reset bit (reg. C6h, R/W, bit 3) is set.

D0 HOST TRANSFER COUNT 0 REGISTER (D0h, R, HTCNT_0)

7:0 (R) (HTCNT[7:0]) - HOST TRANSFER COUNT[7:0]: This ***read only*** counter shows the lower eight bits of the HTCNT[9:0] register which indicates the number of bytes remaining to be transferred to or from the host for the current sector data transfer. This count is valid during PIO or DMA command execution.

This counter is loaded with the contents of the Sector Size Register (reg. 120h/121h, R) when a data transfer is started. After the data portion of the sector is transferred during a Read Long or Write Long command, this counter holds the number of ECC bytes remaining to be transferred to or from the host and is loaded with the ECC Size register (reg. D2h, R/W) at the data/ECC boundary point in the transfer. The HECCTIME bit (reg. D1h, R, bit 7) is set when this counter shows the value "ECC Transfer Count".

D1 HOST TRANSFER COUNT 1 REGISTER (D1h, R, HTCNT_1)

7 (R) (HECCTIME) - HOST ECC TIME: This ***read only*** bit is set during a Read Long or Write Long command when the ECC bytes are being transferred to or from the host. When this bit is set, HTCNT[9:0] will reflect the number of remaining ECC bytes to transfer at the time immediately following the data portion of the sector transfer. When this bit is cleared, HTCNT[9:0] will reflect the remaining data bytes to transfer.

6 (R) (DONEH) - HOST TRANSFER DONE: This ***read only*** bit is set when a host data transfer is done. This may not be the end of the command, but the current sector or block data transfer to the the host has completed. This bit is cleared at the start of the next sector or block transfer or by receipt of a new command from the Host.

5 (R) (DONEB) - BUFFER TRANSFER DONE: This ***read only*** bit is set when a transfer between the buffer and the host FIFO is done. This may not be the end of the command, but the current sector or block data transfer between the buffer and the host FIFO has completed. This bit is cleared at the start of the next sector or block transfer or by receipt of a new command from the Host.

4 (R) (ECCDONEH) - HOST ECC TRANSFER DONE: This ***read only*** bit is set when the appropriate number of ECC bytes to be transferred to or from the host is done. This may not be the end of the Read Long or Write Long command, but the transfer of ECC bytes to or from the the host has completed. This bit is reset by the receipt of a new command from the Host or another transfer started.

3 (R) (ECCDONEB) - BUFFER ECC TRANSFER DONE: This ***read only*** bit is set when a transfer of the appropriate number of ECC bytes between the buffer and the host FIFO, for the current Read Long or Write Long command, is done. This may not be the end of the Read Long or Write Long command, but the transfer of the ECC bytes between the buffer and the host FIFO has completed. This bit is cleared by receipt of a new command from the Host.

2 (R) (XFRDNSTAT) - TRANSFER DONE STATUS: This ***read only*** bit is set when a Host data transfer for the current sector is complete. This status bit sets the XFRDONE Interrupt bit (reg. C8h, R, bit 0). This bit is cleared at the start of the next sector or block transfer or by receipt of a new command from the Host.

1:0 (R) (HTCNT[9:8]) - HOST TRANSFER COUNT[9:8]: These are the two most significant ***read only*** bits of the Host Transfer Counter (HTCNT[9:0]) which shows the number of bytes remaining to be transferred to or from the host for the current data transfer. It is utilized as described in the description of HTCNT_0 (reg. D0h, R).

D2 HOST ECC SIZE REGISTER (D2h, R/W, ECCSIZE)

7:6 (R/W) Reserved_

5:0 (R/W) (ECCSIZE[5:0]) - HOST ECC SIZE[5:0]: This field is used to specify the number of bytes that are transferred to or from the host during a Read Long or a Write Long command.

D3 HOST ECC COUNT REGISTER (D3h, R, ECCCOUNT)

7 (R) (HBECCTIME) - HOST/BUFFER ECC TIME: This ***read only*** bit is set when the host or buffer ECC transfer is active for the current Read Long or Write Long command.

6 (R) Reserved

5:0 (R) (ECCCOUNT[5:0]) - HOST ECC COUNT[5:0]: This ***read only*** field reflects the number of ECC bytes tranferred between the Host FIFO and the buffer controller during the ECC transfer phase of a Read Long or Write Long command. It is loaded with the contents of the ECCSIZE register (reg. D2h, R/W) when the data transfer is started.

E0 CONFIGURATION OPTION REGISTER (E0h, R, CONFIGOPT)

This register is an image of PCMCIA Host Register 200h, R/W.

7 (R) (SRESET) - PCMCIA SOFT RESET: This ***read only*** bit reflects the status of the SRESET bit in the PCMCIA Configuration Option Register (PCMCONFIGOPT, reg. 200h, R/W, bit 7). The host will write a one to generate a PCMCIA soft reset, and a zero to clear the reset.

6 (R) (LEVLREQ) - PCMCIA LEVEL INTERRUPT: This ***read only*** bit reflects the status of LEVLREQ bit in the PCMCIA Configuration Option Register (PCMCONFIGOPT, reg. 200h, R/W, bit 6). A one written by the host signifies level mode interrupt and a zero indicates pulsed mode interrupt.

5 (R) Reserved

4 (R) (CONFIGOPT4) - CONFIG OPTION BIT 4: This ***read only*** bit reflects the status of bit 4 in the PCMCIA Configuration Register (PCMCONFIGOPT, reg. 200h. R/W, bit 4). It can be used to transfer data from host to local microprocessor..

3:0 (R) (CONFIGIDX[3:0]) - CONFIGURATION INDEX: These ***read only*** bits reflect the status of the CONFIGIDX bits in the PCMCIA Configuration Register (PCMCONFIGOPT, reg. 200h. R/W, bits 3:0). They select the access mode as described below:

CONFIGIDX[3:0]	Access Mode
0	Memory Mode (power-on reset default)
1	Block I/O Mode
2	Primary I/O Mode (I/O Address 1F0-1F7h and 3F6-3F7h)
3	Secondary I/O Mode (I/O Address 170-177h and 376-377h)
4	Primary I/O Mode with Floppy Support
5	Secondary I/O Mode with Floppy Support
6-16	Reserved

E1 CONFIGURATION STATUS REGISTER (E1h, R, CONFIGSTAT)

This register is an image of PCMCIA Host Register 202h, R/W.

7 (R) (CHANGED) - PIN REPLACEMENT REGISTER BIT CHANGED: This ***read only*** bit indicates that one or more bits (CBVD1, CBVD2, CRDY/*BSY, or CWPROT) in the PCMCIA Pin Replacement Register (PCMPINREPLACE, reg. 204h, R/W, bits 7-4, respectively) is set to one. This signal drives the *STSCHG pin I/O mode if SIGCHG is set (reg. 202h. R/W, bit 6).

6 (R) (SIGCHG) - ENABLE CHANGED STATUS ON *STSCHG SIGNAL: This ***read only*** bit reflects the status of SIGCHG bit in the PCMCIA Configuration Status Register (reg. 202h, R/W, bit 6). When this bit is set by host and card is configured for I/O interface, the CHANGED bit (reg. 202h, R/W, bit 7) drives *STSCHG pin. If no state change signal is desired, this bit should be cleared to 0 and *STSCHG will be held high.

5 (R) (IOIS8) - HOST IS ONLY 8 BIT: This ***read only*** bit reflects the status of the IOIS8 bit in the PCMCIA Configuration Status Register (reg. 202h, R/W, bit 5). It is set by the host when it only supports 8-bit data transfers.

4:3 (R) (CONFIGSTAT[4:3]) - CONFIG STATUS BIT 4-3: These ***read only*** bits reflect the status of CONFIGSTAT4-3 bits in the PCMCIA Configuration Option Register (reg. 202h, R/W, bits 4:3). These bits can be used to transfer data from the host to local microprocessor.

2 (R) (PWRDWN) - POWER DOWN: This ***read only*** bit reflects the status of the PWRDWN bit in the PCMCIA Configuration Status Register (reg. 202h, R/W, bit 2). This bit is set by the host to place the card in a low power mode.

1 (R) (INTR) - ATA INTERRUPT: This ***read only*** bit shows the internal state of the ATA IRQ signal. In Primary/Secondary I/O Mode, if the *INTEN bit in the AT Host Fixed Disk Register (ATA reg. 3F6h, W, bit 1) is set, then this bit reflects the state of the ATA interrupt request signal. This bit is inactive if the *ITNEN bit is cleared.

0 (R) (CONFIGSTAT[0]) - CONFIG STATUS BIT 0: This ***read only*** bit reflects the status of the CONFIGSTAT0 bit in the PCMCIA Configuration Status Register (reg. 202h, R/W, bit 0). These bits can be used to transfer data from host to local microprocessor.

E2 PIN REPLACEMENT REGISTER (E2h, R, PINREPLACE)

This register is an image of PCMCIA Host Register 204h, R/W.

7 (R) (CBVD1) - BVD1 CHANGE STATE: This ***read only*** bit is not used and always returns a status 0. This bit may be written by the host.

6 (R) (CBVD2) - BVD2 CHANGE STATE: This ***read only*** bit is not used and always returns a status 0. This bit may be written by the host.

5 (R) (CRDY/*BSY1) - RDY/*BSY CHANGE STATE: This ***read only*** bit is set when internal Ready/*Busy signal changes state. This bit may be written by the host.

4 (R) (CWPROT) - WPROT CHANGE STATE: This ***read only*** bit is not used and always returns a status 0. This bit may be written by the host.

3 (R) (RBVD1) - BVD1 STATUS: This ***read only*** bit is not used and always returns a status 1 for good battery level. This bit may be written by the host.

2 (R) (RBVD2) - BVD2 STATUS: This ***read only*** bit is not used and always returns a status 1 for good battery level. This bit may be written by the host.

1 (R) (RRDY/*BSY1) - RDY/*BSY STATUS: This ***read only*** bit represents the internal state of the Ready/*Busy signal. When this bit is set by the host, the corresponding CRDY/*BSY bit is also written. When this bit is reset by the host, the CRDY/*BSY bit is unaffected.

0 (R) (RWPROT) - WPROT STATUS: This ***read only*** bit is not used and always returns a status 0 for no write protection. This bit may be written by the host.

E3 SOCKET COPY REGISTER (E3h, R, SOCKETCOPY)

This register is an image of PCMCIA Host Register 206h, R/W.

7 (R) Reserved

6:4 (R) (COPY[2:0]) - COPY NUMBER: These ***read only*** bits reflect the status of the COPY[2:0] bits in the PCMCIA Socket Copy Register (PCMSOCKETCOPY, reg. 206h, R/W, bits 6:4). This permits identical cards to share a common set of I/O addresses while remaining uniquely identifiable, and consecutively ordered. The first copy number is 0.

3:0 (R) (SOCKET[3:0]) - SOCKET NUMBER: These ***read only*** bits reflect the status of the SOCKET[3:0] bits in the PCMCIA Socket Copy Register (reg. 206h, R/W, bits 3:0). These bits indicate to the card the socket it is located in. The first socket number is 0.

E4 HOST INTERRUPT STATUS 2 REGISTER (E4h, R, HINT_2)

The ***read only*** status bits in this register get set and remain set when the corresponding status condition occurs. Each bit can be cleared by writing to the corresponding bit in the Host Interrupt Clear 2 register (reg. E4h, W). Also, each status bit can be enabled as an interrupt via the corresponding interrupt mask bit in the Host Interrupt Enable 2 register (reg. E5h, R/W) and by setting the EN_HOSTINT2 Bit (reg. 53h, R/W, bit 2).

7:6 (R) Reserved

5 (R) (CISRD) - CIS READ BY HOST: This bit is set whenever the host reads the Card Information Structure area of Attribute Memory (000h-1FFh).

4 (R) (SOCKETWR) - SOCKET & COPY WRITTEN: This bit is set when the PCMCIA Socket Copy Register (reg. 206h, R/W) is written by the host.

3 (R) (PWRDWNCHG) - POWERDOWN BIT CHANGED: This bit is set when the Power Down bit (reg. 202h, R/W, bit 2) is changed by the host.

2 (R) (PINREPWR) - PIN REPLACEMENT WRITTEN: This bit is set when the PCMCIA Pin Replacement Register (reg. 204h, R/W) is written by the host.

1 (R) (CONFIGSTWR) - CONFIGURATION STATUS WRITTEN: This bit is set when PCMCIA Configuration Status Register (reg. 202h, R/W) is written by the host.

0 (R) (CONFIGOPTWR) - CONFIGURATION OPTION WRITTEN: This bit is set when PCMCIA Configuration Option Register (reg. 200h, R/W) is written by the host.

E4 HOST INTERRUPT CLEAR 2 REGISTER (E4h, W, HINTCLR_2)

The ***write only*** bits in this register are used to clear the corresponding bits in the Host Interrupt Status 2 register (reg. E4h, R).

7:6 (R/W) Reserved

5 (W) (CLR_CISRD) - CLEAR CIS READ BY HOST: When set, this bit clears the CIS Read By Host bit in the Host Interrupt 2 Status register (reg. E4h, R, bit 5).

4 (W) (CLR_SOCKETWR) - CLEAR SOCKET & COPY WRITTEN: When set, this bit clears the Socket & Copy Written bit in the Host Interrupt 2 Status register (reg. E4h, R, bit 4).

3 (W) (CLR_PWRDWNCHG) - CLEAR POWERDOWN BIT CHANGED: When set, this bit clears the Powerdown Bit Changed bit in the Host Interrupt 2 Status register (reg. E4h, R, bit 3).

2 (W) (CLR_PINREPWR) - CLEAR PIN REPLACEMENT WRITTEN: When set, this bit clears the Pin Replacement Written bit in the Host Interrupt 2 Status register (reg. E4h, R, bit 2).

1 (W) (CLR_CONFIGSTWR) - CLEAR CONFIGURATION STATUS WRITTEN: When set, this bit clears the Configuration Status Written bit in the Host Interrupt 2 Status register (reg. E4h, R, bit 1).

0 (W) (CLR_CONFIGOPTWR) - CLEAR CONFIGURATION OPTION WRITTEN: When set, this bit clears the Configuration Option Written bit in the Host Interrupt 2 Status register (reg. E4h, R, bit 0).

E5 HOST INTERRUPT 2 ENABLE REGISTER (E5h, R/W, HINTEN_2)

The bits in this register have a one-to-one correspondence to the those in the Host Interrupt 2 Status register (reg. E4h, R). Setting a bit in this register will enable the corresponding status bit as an interrupt to the microprocessor if the EN_HOSTINT2 Bit (reg.53h, R/W, bit 2) is also set. Clearing a bit in this register will inhibit the interrupt for the corresponding status bit, but will have no effect on the state of that status bit.

7:6 (R/W) Reserved

5 (R/W) (EN_CISRD) - ENABLE CISRD INTERRUPT: When set, this bit enables the CIS Read by Host bit (reg. E4h, R/W, bit 5) to generate the Interrupt Active 2 Bit (reg. 52h, R, bit 2).

4 (R/W) (EN_SOCKETWR) - ENABLE SOCKETWR INTERRUPT: When set, this bit enables the Socket & Copy Write bit (reg. E4h, R/W, bit 4) to generate the Interrupt Active 2 Bit (reg. 52h, R, bit 2).

3 (R/W) (EN_PWRDWNCHG) - ENABLE PWRDWNCHG INTERRUPT: When set, this bit enables the Power Down Changed bit (reg. E4h, R/W, bit 3) to generate the Interrupt Active 2 Bit (reg. 52h, R, bit 2).

2 (R/W) (EN_PINREWR) - ENABLE PINREPWR INTERRUPT: When set, this bit enables the Pin Replacement Write bit (reg. E4h, R/W, bit 2) to generate the Interrupt Active 2 Bit (reg. 52h, R, bit 2).

1 (R/W) (EN_CONFIGSTWR) - ENABLE CONFIGSTWR INTERRUPT: When set, this bit enables the Configuration Status Write bit (reg. E4h, R/W, bit 1) to generate the Interrupt Active 2 Bit (reg. 52h, R, bit 2).

0 (R/W) (EN_CONFIGOPTWR) - ENABLE CONFIGOPTWR INTERRUPT: When set, this bit enables the Configuration Option Write bit (reg. E4h, R/W, bit 0) to generate the Interrupt Active 2 Bit (reg. 52h, R, bit 2).

E6 PCMCIA MISCELLANEOUS REGISTER (E6h, R/W, PCMCIAMISC)

7 (R) (HRST) - HOST RESET SIGNAL STATUS: This ***read only*** bit reflects the unlatched status of the Host Reset signal. This bit will return a one if reset signal is asserted and a zero if reset is negated.

6 (R) (HOSTMODE) - HOST INTERFACE MODE: This ***read only*** bit reflects the currently selected interface mode (0 = PCMCIA, 1 = ATA). The selected interface can be changed by writing to bit 1:0 of this register.

5:2 (R/W) Reserved

1:0 (R/W) (HOSTSEL[1:0]) - HOST INTERFACE SELECT: These bits select the interface type (ATA or PCMCIA). 0: Automatic Selection (via hardware; power on reset default mode). 1: Select ATA Mode. 2: Select PCMCIA Mode. 3: Reserved. At *POR time, the interface is automatically selected by the hardware (ATA is selected if no pull-down resistor on Buffer Address BA7 pin). The microprocessor can override the automatic selection by writing 10b to select PCMCIA. Writing 01b changes the interface back to ATA mode.

5.5 Buffer Block Register Descriptions

100 BUFFER MODE REGISTER (100h, R/W, BMODE)

7:6 (R/W) (BUFCYC[1:0]) - BUFFER CYCLE TIME SELECT: These bits, in conjunction with the RAMSEL[2:0] bits in this register, select the number of BUFCLK cycles it takes to access data in the buffer memory. The options are summarized in the table below.

RAM Type	BUFCYC[1:0]	Configuration Name	Single Word/Byte Access Period	N-Word Page Mode Access Period
SRAM	0 0	SRAM2T	$2 \bullet T_{BUFCLK}$	$2 \bullet N \bullet T_{BUFCLK}$
SRAM	0 1	SRAM3T	$3 \bullet T_{BUFCLK}$	$3 \bullet N \bullet T_{BUFCLK}$
SRAM	1 0	SRAM4T	$4 \bullet T_{BUFCLK}$	$4 \bullet N \bullet T_{BUFCLK}$
SRAM	1 1	SRAM5T	$5 \bullet T_{BUFCLK}$	$5 \bullet N \bullet T_{BUFCLK}$
DRAM	0 0	DRAM6T	$6 \bullet T_{BUFCLK}$	$(4+2 \bullet N) \bullet T_{BUFCLK}$
DRAM	0 1	DRAM8T	$8 \bullet T_{BUFCLK}$	$(5+3 \bullet N) \bullet T_{BUFCLK}$
DRAM	1 0	not allowed		
DRAM	1 1	not allowed		

5:3 (R/W) (RAMSEL[2:0]) - RAM SELECT[2:0]: This field selects the type of RAM used and the configuration as follows:

RAMSEL[2:0]	RAM Type and Configuration
0 0 0	Single SRAM with *MOE
0 0 1	Single SRAM with *MCE
0 1 0	reserved
0 1 1	reserved
1 0 0	Dual 32K SRAM with *MCE1 and *MCE2
1 0 1	Dual 64K SRAM with *MCE1 and *MCE2
1 1 0	Dual 128K SRAM with *MCE1 and *MCE2
1 1 1	DRAM

2 (R/W) (BEN16BIT) - ENABLE 16-BIT WIDE BUFFER: While this bit is set, 16-bit wide buffer memory is selected. When it is cleared, 8-bit wide buffer memory is selected. When 16-bit wide buffer mode is selected all multisector transfers, to or from the disk, must be even byte sector transfers.

1 (R/W) (ENHIPH) - ENABLE HIGH PRIORITY FOR HOST PORT: This bit is set to enable higher priority access of the buffer by the Host Port. During transfers from the Host to the buffer, a higher priority will be established when the Host FIFO has more than 16 bytes of data. During transfers from the buffer to the Host, a higher priority will be established when the Host FIFO has less than 16 bytes of data. When this bit is cleared, the Host Port will have lower priority.

While this bit is reset, the default priority in descending order is: Servo, Disk, Refresh, Correction, Microprocessor, and Host ports.

While this bit is set, the dynamically modified priority in descending order is: Servo, Disk, Refresh, Host High, Correction, Microprocessor, and Host Low ports.

0 (R/W) (RDPSEUDO) - ENABLE PSEUDO READ FROM BUFFER: This bit enables the buffer to be read via the microprocessor without using the READY line. This bit must be cleared when performing direct reads from the buffer using the READY line.

101 REFRESH PERIOD REGISTER (101h, W, RPERIOD)

7:0 (W) (RPERIOD[7:0]) - REFRESH PERIOD[7:0]: The Refresh Timer is a programmable timer used for generating DRAM refresh cycles while the RAMSEL[2:0] bits (reg. 100h, R/W, bits 5:3) select DRAM mode. The value to be loaded into the Refresh Timer each time it counts down to zero is specified by the value in this register. These bits determine the time period between two consecutive refresh cycles of the DRAM. The refresh timer (RTIMER, reg. 101h, R) is loaded with the contents of this register, and is then decremented once every 32 BUFCLK cycles. When the Refresh Timer register becomes zero, it is reloaded with the contents of this register and a CAS before RAS refresh cycle is generated for the DRAM. After it reaches 0, a request is made to the Prioritizer for a DRAM refresh, and the request is cleared by a refresh acknowledge from the Buffer Access State Machine. Thus, the time between refresh cycles is:

$$T_{REFRESH} = (RPERIOD + 1) \bullet 32 \bullet T_{BUFCLK}$$

Where T_{BUFCLK} is the BUFCLK period. A value of zero loaded into the Refresh Period register will disable refreshes to the DRAM. The following table shows the RPERIOD resolution and maximum values for different BUFCLK frequencies:

fBUFCLK	RPERIOD Resolution	Maximum RPERIOD
16 Mhz	2000 ns	512 us
24 Mhz	1333 ns	341 us
32 Mhz	1000 ns	256 us
40 Mhz	800 ns	204 us
48 Mhz	670 ns	172 us

101 REFRESH TIMER REGISTER (101h, R, RTIMER)

7:0 (R) (RTIMER[7:0]) - REFRESH TIMER [7:0]: These bits show the contents of the Refresh Timer, and are provided for test purposes. The Refresh Timer is continuously running in DRAM mode. The bits may be changing when the local microprocessor reads this register which may result in an erroneous value being read.

102 BUFFER CONTROL 0 REGISTER (102h, R/W, BCTL_0)

7 (R/W) (ENDUCTR) - ENABLE DISK UP COUNTER: Setting this bit allows the Disk Up Counter (regs. 12Eh, 12Fh, R/W) to count up. While this bit is cleared, the Disk Up Counter is forced to the value 000h.

6 (R/W) Reserved (This bit must be set to 0.)

5 (R/W) (ENDNRMOCR) - ENABLE DISK NO ROOM OCCURRED: When this bit is set, the Disk No Room Occurred bit (reg. 103h, R, bit 5) is enabled to be set whenever the buffer becomes full or empty for disk transfers. When this bit is cleared, the DNRMOCR bit (reg. 103h, R, bit 5) will be disabled from getting set to 1. Clearing this bit will not clear DNRMOCR if that bit is already set to 1.

4 (R/W) (ENHNRMOCR) - ENABLE HOST NO ROOM OCCURRED: When this bit is set, the Host No Room Occurred bit (reg. 103h, R, bit 4) is enabled to be set whenever the buffer becomes full or empty for Host transfers. When this bit is cleared, the HNRMOCR bit (reg. 103h, R, bit 4) will be disabled from getting set to 1. Clearing this bit will not clear HNRMOCR if that bit is already set to 1.

3 (R/W) (ENDRMWRAP) - ENABLE DISK ROOM LOGIC ON WRAP: When this bit is set, the ENDROOM bit (reg. 137h, R/W, bit 0) will be automatically set when the disk pointer wraps from end of segment to begin of segment.

2 (R/W) (MP16BIT) - ENABLE 16-BIT MICROPROCESSOR BUFFER ACCESS: When set, this bit speeds up the microprocessor accesses of buffer memory while operating in 16-bit mode. When set, the *WE0 and *WE1 pins are asserted at the same time to decrease the allocated access time in the case where *WE1 and *WE0 are staggered in time. This works only if the microprocessor does sequential low byte and high byte accesses.

1 (R/W) (DISMOE) - DISABLE *MOE/*MCE/*RAS: When this bit is set, the *MOE, *MCE or *RAS signal is disabled when accessing the buffer. This allows external switch settings on the BD[15:0] signals to be read by the local microprocessor by doing a buffer read after setting this bit. DRAM refresh cycles will continue to occur while this bit is set.

0 (R/W) Reserved

103 BUFFER INTERRUPT 0 STATUS REGISTER (103h, R, BINT_0)

The status bits in this register get set and remain set when the corresponding status condition occurs. Each bit can be cleared by writing a 1 to the corresponding bit in the Buffer Interrupt Clear 0 register (reg. 103h, W). Also, each status bit can be enabled as an interrupt via the corresponding interrupt mask bit in the Buffer Interrupt Enable 0 register (reg. 104h, R/W) and by setting EN_BUFINT0 (reg. 53h, R/W, bit 3).

7 (R) (DCDONE) - DISK SECTOR COUNTER DONE: This bit is set when the Disk Sector Counter (reg. 10Dh, R/W) decrements to zero, indicating that the number of sectors loaded into the counter have been transferred between the disk and the buffer.

6 (R) Reserved.

5 (R) (DNRMOCR) - DISK NO ROOM OCCURRED: This bit is set when the Enable Disk No Room Occurred bit (reg. 102h, R/W, bit 5) is set and the Disk No Room bit (reg. 10Bh, R/W, bit 7) makes a transition from 0 to 1.

4 (R) (HNRMOCR) - HOST NO ROOM OCCURRED: This bit is set when the Enable Host No Room Occurred bit (reg. 102h, R/W, bit 4) is set and the Host No Room bit (reg. 10Bh, R/W, bit 6) makes a transition from 0 to 1.

3 (R) Reserved

2 (R) (CPOVR) - CORRECTION PORT OVERRUN ERROR: This bit is set during ECC correction if the last data word (or byte) of a sector is written into the buffer and the ECC correction for the previous sector has not been completed. The ECC correction will be terminated when this bit is set.

1:0 (R) Reserved

103 BUFFER INTERRUPT CLEAR 0 REGISTER (103h, W, BINTCLR_0)

The bits in this register clear the corresponding bits in the Buffer Interrupt 0 Status register (reg. 103h, R).

7 (W) (CLR_DCDONE) - CLEAR DCDONE INTERRUPT: Setting this bit will clear the corresponding bit in the Buffer Interrupt 0 Status register.

6 (W) Reserved.

5 (W) (CLR_DNRMOCR) - CLEAR DNRMOCR INTERRUPT: Setting this bit will clear the corresponding bit in the Buffer Interrupt 0 Status register.

4 (W) (CLR_HNRMOCR) - CLEAR HNRMOCR INTERRUPT: Setting this bit will clear the corresponding bit in the Buffer Interrupt 0 Status register.

3 (W) Reserved

2 (W) (CLR_CPOVR) - CLEAR CPOVR INTERRUPT: Setting this bit will clear the corresponding bit in the Buffer Interrupt 0 Status register.

1:0 (W) Reserved

104 BUFFER INTERRUPT ENABLE 0 REGISTER (104h, R/W, BINTEN_0)

The bits in this register have a one-to-one correspondence to the bits in the Buffer Interrupt 0 Status register (reg. 103h, R). Setting a bit in this register will enable the corresponding status bit as an interrupt to the microprocessor if the EN_BUFINT0 bit (reg. 53h, R/W, bit 3) is also set. Clearing a bit in this register will inhibit the interrupt for the corresponding status bit, but will have no effect on the state of that status bit.

7 (R/W) (EN_DCDONE) - ENABLE DCDONE INTERRUPT: Setting this bit will enable the corresponding bit in the Buffer Interrupt 0 Status register to generate the Interrupt Active 3 bit (reg. 52h, R, bit 3).

6 (R/W) Reserved. This bit must be set to 0.

5 (R/W) (EN_DNRMOCR) - ENABLE DNRMOCR INTERRUPT: Setting this bit will enable the corresponding bit in the Buffer Interrupt 0 Status register to generate the Interrupt Active 3 bit (reg. 52h, R, bit 3).

4 (R/W) (EN_HNRMOCR) - ENABLE HNRMOCR INTERRUPT: Setting this bit will enable the corresponding bit in the Buffer Interrupt 0 Status register to generate the Interrupt Active 3 bit (reg. 52h, R, bit 3).

3 (R/W) Reserved

2 (R/W) (EN_CPOVR) - ENABLE CPOVR INTERRUPT: Setting this bit will enable the corresponding bit in the Buffer Interrupt 0 Status register to generate the Interrupt Active 3 bit (reg. 52h, R, bit 3).

1:0 (R/W) Reserved

105 BUFFER CONTROL 1 REGISTER (105h, R/W, BCTL_1)

7:4 (R/W) Reserved

3 (R/W) (DISDERRSTOP) - DISABLE DISK ERROR STOP: When this bit is cleared, data transfers between the buffer and the Disk FIFO will be stopped when the Disk Check Error bit (reg. 106h, R, bit 1) is set. If that bit is set because of a parity error, the transfer will be stopped within two words of the one that had the parity error.

2 (R/W) (DISHERRSTOP) - DISABLE HOST ERROR STOP: When this bit is cleared, data transfers between the buffer and the Host FIFO will be stopped when the Host Check Error bit (reg. 106h, R, bit 0) is set. If that bit is set because of a parity error, the transfer will be stopped within two words of the one that had the parity error.

1 (R/W) (FRCBPERR) - FORCE BUFFER PARITY ERROR: When this bit is set, the parity bits are inverted when writing to the buffer in order to force wrong parity.

0 (R/W) (ENBPCHK) - ENABLE BUFFER PARITY CHECKING: When this bit is set, parity will be checked on all words or bytes read from the buffer memory. If a parity error is detected, one of six appropriate Check Error bits will be set (reg. 106h, R, bits 5:0).

106 BUFFER INTERRUPT 1 STATUS REGISTER (106h, R, BINT_1)

The status bits in this register get set and remain set when the corresponding status condition occurs. Each bit can be cleared by writing a 1 to the corresponding bit in the Buffer Interrupt Clear 1 register (reg. 106h, W). Also, each status bit can be enabled as an interrupt via the corresponding interrupt mask bit in the Buffer Interrupt Enable 1 register (reg. 107h, R/W) and by setting EN_BUFINT1 (reg. 53h, R/W, bit 4).

7:6 (R) Reserved

5 (R) (HCISCHKERR) - HOST CIS PORT CHECK ERROR: This bit is set if a parity error is detected when the Host CIS Port reads a byte from the buffer while the Enable Buffer Parity Checking bit (reg. 105h, R/W, bit 0) is set.

4 (R) (VCHKERR) - SERVO PORT CHECK ERROR: This bit is set if a parity error is detected when the Servo Port reads a data split byte from the buffer while the Enable Buffer Parity Checking bit (reg. 105h, R/W, bit 0) is set.

3 (R) (MCHKERR) - MICROPROCESSOR PORT CHECK ERROR: This bit is set if a parity error is detected when the local microprocessor reads a byte from the buffer while the Enable Buffer Parity Checking bit (reg. 105h, R/W, bit 0) is set.

2 (R) (CCHKERR) - CORRECTION PORT CHECK ERROR: This bit is set if a parity error is detected when the Correction Port reads a byte from the buffer while the Enable Buffer Parity Checking bit (reg. 105h, R/W, bit 0) is set.

1 (R) (DCHKERR) - DISK PORT CHECK ERROR: This bit is set if, while the Enable Buffer Parity Checking bit (reg. 105h, R/W, bit 0) is set, a parity error is detected when the Disk Port reads a byte from the buffer.

0 (R) (HCHKERR) - HOST PORT CHECK ERROR: This bit is set if, while the Enable Buffer Parity Checking bit (reg. 105h, R/W, bit 0) is set, a parity error is detected when the Host Port reads a byte from the buffer.

106 BUFFER INTERRUPT CLEAR 1 REGISTER (106h, W, BINTCLR_1)

The bits in this register clear the corresponding bits in the Buffer Interrupt 0 Status register (reg. 106h, R).

7:6 (W) Reserved

5 (W) (CLR_HCISCHKERR) - CLEAR HCISCHKERR INTERRUPT: Setting this bit will clear the corresponding bit in the Buffer Interrupt 1 Status register.

4 (W) (CLR_VCHKERR) - CLEAR VCHKERR INTERRUPT: Setting this bit will clear the corresponding bit in the Buffer Interrupt 1 Status register.

3 (W) (CLR_MCHKERR) - CLEAR MCHKERR INTERRUPT: Setting this bit will clear the corresponding bit in the Buffer Interrupt 1 Status register.

2 (W) (CLR_CCHKERR) - CLEAR CCHKERR INTERRUPT: Setting this bit will clear the corresponding bit in the Buffer Interrupt 1 Status register.

1 (W) (CLR_DCHKERR) - CLEAR DCHKERR INTERRUPT: Setting this bit will clear the corresponding bit in the Buffer Interrupt 1 Status register.

0 (W) (CLR_HCHKERR) - CLEAR HCHKERR INTERRUPT: Setting this bit will clear the corresponding bit in the Buffer Interrupt 1 Status register.

107 BUFFER INTERRUPT ENABLE 1 REGISTER (107h, R/W, BINTEN_1)

The bits in this register have a one-to-one correspondence to the bits in the Buffer Interrupt 1 Status register (reg. 106h, R). Setting a bit in this register will enable the corresponding status bit as an interrupt to the microprocessor if the EN_BUFINT1 bit (reg. 53h, R/W, bit 4) is also set. Clearing a bit in this register will inhibit the interrupt for the corresponding status bit, but will have no effect on the state of that status bit.

7:6 (R/W) Reserved

5 (R/W) (EN_HCISCHKERR) - ENABLE HCISCHKERR INTERRUPT: Setting this bit will enable the corresponding bit in the Buffer Interrupt 1 Status register to generate the Interrupt Active 4 bit (reg. 52h, R, bit 4).

4 (R/W) (EN_VCHKERR) - ENABLE VCHKERR INTERRUPT: Setting this bit will enable the corresponding bit in the Buffer Interrupt 1 Status register to generate the Interrupt Active 4 bit (reg. 52h, R, bit 4).

3 (R/W) (EN_MCHKERR) - ENABLE MCHKERR INTERRUPT: Setting this bit will enable the corresponding bit in the Buffer Interrupt 1 Status register to generate the Interrupt Active 4 bit (reg. 52h, R, bit 4).

2 (R/W) (EN_CCHKERR) - ENABLE CCHKERR INTERRUPT: Setting this bit will enable the corresponding bit in the Buffer Interrupt 1 Status register to generate the Interrupt Active 4 bit (reg. 52h, R, bit 4).

1 (R/W) (EN_DCHKERR) - ENABLE DCHKERR INTERRUPT: Setting this bit will enable the corresponding bit in the Buffer Interrupt 1 Status register to generate the Interrupt Active 4 bit (reg. 52h, R, bit 4).

0 (R/W) (EN_HCHKERR) - ENABLE HCHKERR INTERRUPT: Setting this bit will enable the corresponding bit in the Buffer Interrupt 1 Status register to generate the Interrupt Active 4 bit (reg. 52h, R, bit 4).

108 BUFFER COUNTER CONTROL REGISTER (108h, R/W, BCTRCTL)

7 (R/W) (ENDLYRLS) - ENABLE DELAYED BLOCK RELEASE: When this bit is set, the Disk Block Counter (DBCTR, reg. 10Eh, R) will be incremented for every good data block transferred between disk and buffer, instead of incrementing the Buffer Counter that is selected for the disk (DBCTRSEL, reg. 137h, R/W, bit 1).

6 (R/W) (HBCCLR) - HOST BYTE COUNTER CLEAR: When this bit is set, Host Byte Counter 0 and Host Byte Counter 1 registers (regs. 124h, 125h, R) are cleared. This bit does not have to be reset to 0, and writing a 0 to it has no effect. This bit is always read back as 0.

5 (R/W) (DBCCLR) - DISK BYTE COUNTER CLEAR: When set, this bit clears Disk Byte Counter 0, Disk Byte Counter 1 (reg. 126h, R, and reg. 127h, R, bits 2:0), and the Disk FIFO. This bit does not have to be reset to 0, and writing a 0 to it has no effect. This bit is always read back as a 0.

4 (R/W) (DBCTRCLR) - DISK BLOCK COUNTER CLEAR: Setting this bit will clear the Disk Block Counter (reg. 10Eh, R). This bit should only be set when the DBCTR is not active. This bit does not have to be reset back to 0, and writing a 0 to it has no effect. This bit is always read back as 0.

3 (R/W) (RLSBLKS) - RELEASE BLOCKS TO HOST: Writing a 1 to this bit will add the contents of the Disk Block Counter (DBCTR, reg. 10Eh, R) to the BCTR selected for the disk and clear DBCTR. This is used for the delayed block release option. This bit does not have to be reset back to 0, and writing a 0 to it has no effect. This bit is always read back as 0.

2:1 (R/W) Reserved

0 (R/W) (BCTRSEL) - BUFFER COUNTER SELECT: This bit is used to select which Buffer Counter register (BCTRA or BCTRB) will be operated upon when the local microprocessor performs an add or subtract operation by writing to the BCTRAS register (reg. 10Ah, W). BCTR register selection is summarized in the following table:

BCTRSEL	Buffer Counter Selected
0	BCTRA
1	BCTRB

109 BUFFER PORT ENABLE REGISTER (109h, R/W, BPORTEN)

7:6 (R/W) Reserved

5 (R/W) (HCISPEN) - HOST CIS PORT ENABLE: While this bit is set, the transfer of data between the buffer memory and the Host CIS port can occur.

4 (R/W) (VPEN) - SERVO PORT ENABLE: While this bit is set, the transfer of data between the buffer memory and the Servo port can occur.

3 (R/W) (MPEN) - MICROPROCESSOR PORT ENABLE: While this bit is set, the transfer of data between the buffer memory and the Microprocessor port can occur.

2 (R/W) (CPEN) - CORRECTION PORT ENABLE: While this bit is set, the transfer of data between the buffer memory and the Correction port can occur.

1 (R/W) (DPEN) - DISK PORT ENABLE: While this bit is set, the transfer of data between the buffer memory and the Disk port can occur.

0 (R/W) (HPEN) - HOST PORT ENABLE: While this bit is set, the transfer of data between the buffer memory and the Host port can occur.

10A BUFFER COUNTER ADD/SUBTRACT REGISTER (10Ah, W, BCTRAS)

7:0 (W) (BCTRAS[7:0]) - BUFFER COUNTER ADD/SUBTRACT[7:0]: The value loaded into this register by the local microprocessor will be either added to or subtracted from the BCTR which is currently selected via the BCTRSEL bit (reg. 108h, R/W, bit 0). If bit 7 is cleared, an addition is performed. If bit 7 is set, a two's complement subtraction is performed. Thus, the add/subtract range is from -128 (80h) to +127 (7Fh). This function is implemented such that it can take place at any time during disk or Host transfers and will not interfere with correct counting of the selected BCTR.

10B BUFFER STATUS 1 REGISTER (10Bh, R/W, BSTAT1)

7 (R) (DNOROOM) - DISK NO ROOM: This ***read only*** bit is set when the Buffer Counter register that is selected for the Disk Segment indicates that there is no room in that segment during a read operation, or there is no data available in that segment during a write operation. If power management is enabled for the Buffer Manager block (BBLKPDNEN=1, reg. 50h, R/W, bit 4), this bit will not be updated while the Buffer Manager block is powered down.

This bit is set when the Buffer Counter register (BCTRn) becomes ≥ to BKMAXn, and can be used as an indication to the Disk Sequencer for stopping transfers to/from buffer. This is a segment full condition for a read operation and a segment empty condition for a write operation. It is also set during a read operation if BCTRn=BKMAXn-1and the ECC correction circuitry is trying to correct the last sector that was read from disk. This means that the last sector that was read filled up the buffer but BCTRn has not incremented because the sector has not been corrected yet. If the ECC error is determined to be uncorrectable, this bit will remain set but BCTRn will not increment to BKMAXn. Note that this bit is forced to 0 when ENDROOM=0 (reg. 137h, R/W, bit 0).

6 (R) (HNOROOM) - HOST NO ROOM: This ***read only*** bit is set when the Buffer Counter register that is selected for the Host Segment indicates that there is no room in that segment during a read operation, or there is no data available in that segment during a write operation. If power management is enabled for the Buffer Manager block (BBLKPDNEN=1, reg. 50h, R/W, bit 4), this bit will not be updated while the Buffer Manager block is powered down.

This bit is set whenever the Buffer Counter register (BCTRn) becomes ≤ 0, and is used to halt data between host and buffer memory. During an AT Read Multiple or Write Multiple command, this bit is set when BCTRn < HBLKSIZE, indicating that the buffer does not have room or data for a host block. Note that this bit is forced to 0 when ENHROOM=0 (reg. 133h, R/W, bit 0) and AWSEL=0 (bit 0 of this register), or when ENAWROOM=0 (reg. 133h, R/W, bit 3) and AWSEL=1.

5:1 (R) Reserved.

0 (R/W) (AWSEL) - AUTO WRITE SELECT: This bit is automatically set at the start of an auto write host transfer. When set, the AWSEGSEL, AWBCTRSEL, and ENAWROOM bits (reg. 133h, R/W, bits 5-3 respectively) are used to select the buffer segment and buffer counter for host transfer and to enable the host room logic, respectively. When cleared, the HSEGSEL, HBCTRSEL, and ENHROOM bits (reg. 133h, R/W, bits 2-0 respectively) are used to select the buffer segment and buffer counter for host transfer and to enable the host room logic, respectively. This bit also enables the operation of the Write Cache Pointer (WCP).

Additionally, The microprocessor writes to the folowing registers and bits are disabled when this bit is set:

- Host Pointer Registers (regs. 130h-132h, R/W)
- Host Byte Counter Clear Bit (reg. 108h, R/W, bit 6)

10D DISK SECTOR COUNTER REGISTER (10Dh, R, DISKCTR)

7:0 (R) (DISKCTR[7:0]) - DISK SECTOR COUNTER [7:0]: This register reflects the contents of the 8-bit Disk Sector Counter which is used to count the number of sectors transferred between the disk and the buffer. The counter is idle when it contains a value of 00h. Having been loaded with a non-zero value, the Disk Sector Counter will decrement by 1 for every sector that is transferred between the disk and the buffer.

During a disk write operation, the counter decrements when the last byte of a sector is transferred from the buffer. This will occur when the Disk Byte Counter (reg. 126h and reg. 127h, bits 2:0) decrements to zero. During a disk read or verify operation, the counter decrements after an error-free sector is read from the disk or after a sector with an error has been automatically corrected.

When the Disk Sector Counter decrements to zero, the Disk Counter Done bit (DCDONE, reg. 103h, R, bit 7) will be set. The counter will remain at zero until it is reloaded with a non-zero value by the local microprocessor.

10E DISK BLOCK COUNTER REGISTER (10Eh, R, DBCTR)

7 (R/W) Reserved

6:0 (R/W) (DBCTR[6:0]) - DISK BLOCK COUNTER: The Disk Block Counter is an 7-bit up counter that is used for the delayed block release option. DBCTR defaults to 0, and the microprocessor can clear it by writing a 1 to the DBCTRCLR bit (reg. 108h, R/W, bit 4).

If the delayed block release option has been enabled (ENDLYRLS=1, reg. 108h, R/W, bit 7) every good block transferred between disk and buffer will increment the DBCTR instead of incrementing the BCTR that is selected for the disk (DBCTRSEL, reg. 137h, R/W, bit 1). When the blocks are to be released to the host, the microprocessor writes a 1 to the RLSBLKS bit (reg. 108h, R/W, bit 3). This adds the contents of DBCTR to the BCTR selected for the disk and resets DBCTR back to 0.

In this mode the DNOROOM signal is generated based on the sum of DBCTR and the BCTR that is selected for the disk. This allows the disk to stop transferring to or from buffer on buffer full or empty conditions, respectively.

110 MICROPROCESSOR PAGE 0 REGISTER (110h (111h), R/W, MPAGE_0)

7:2 (R/W) (MPAGE[15:10]) - MICROPROCESSOR PAGE 0 [15:10]: This register contains the least significant six bits of the Microprocessor Page address.

1:0 (R/W) Reserved

111 MICROPROCESSOR PAGE 1 REGISTER (111h (110h), R/W, MPAGE_1)

7:6 (R/W) Reserved

5:0 (R/W) (MPAGE[21:16]) - MICROPROCESOR PAGE 1 [21:16]: These bits are the most significant bits of the Microprocessor Page address.

The Microprocessor Page registers provide the base address for a 2048-byte page in the Buffer that can be directly accessed by the microprocessor. The base address can be set with 1024 byte resolution. The microprocessor provides an 11-bit address which selects the byte to be accessed within the 2048-byte window.

112 SERVO PAGE 0 REGISTER (112h (113h), R/W, VPAGE_0)

7:5 (R/W) (VPAGE[15:13]) - SERVO PAGE 0 [15:13]: This register contains the least significant three bits of the Servo Page address.

4:0 (R/W) Reserved

113 SERVO PAGE 1 REGISTER (113h (112h), R/W, VPAGE_1)

7:6 (R/W) Reserved

5:0 (R/W) (VPAGE[21:16]) - SERVO PAGE 1 [21:16]: These bits are the most significant bits of the Servo Page address.

The Servo Page registers provide the base address for a 8Kbyte page in the Buffer that can be directly accessed by the Servo port. The Servo Page registers provide the upper address bits for the Servo port access while the least significant 13 bits of the address are provided by the Servo Pointer (regs. 12Ch/12Dh, R/W).

114 BUFFER COUNTER A 0 REGISTER (114h (115h), R/W, BCTRA_0)

7:0 (R/W) (BCTRA[7:0]) - BUFFER COUNTER A[7:0]: This is the least significant byte of the Buffer Counter A (BCTRA) register.

115 BUFFER COUNTER A 1 REGISTER (115h (114h), R/W, BCTRA_1)

7:0 (R/W) (BCTRA[15:8]) - BUFFER COUNTER A[15:8]: This is the most significant byte of the Buffer Counter A (BCTRA) register.

The Buffer Counter (BCTR) is used for keeping track of the number of sectors in the buffer and controls the starting and stopping of disk and host transfers through the buffer room logic when enabled. It is a two's complement counter, where a negative count is indicated by bit 15 being set. Enabling Buffer Counter operation and the room logic for host and disk transfers is controlled separately through the register bits shown below, so that the user has the flexibility of enabling them for both the Host and Disk, only the Host, only the Disk, or neither one.

for Host transfers: HBCTRSEL and ENHROOM bits (reg. 133h, R/W, bits 1 and 0)
or
AWBCTRSEL and ENAWROOM bits (reg. 133h, R/W, bits 4 and 3)

for Disk transfers: DBCTRSEL and ENDROOM bits (reg. 137h, R/W, bits 1 and 0)

116 MAXIMUM BUFFER COUNT A 0 REGISTER (116h (117h), R/W, BKMAXA_0)

7:0 (R/W) (BKMAXA[7:0]) - MAXIMUM BUFFER COUNT A[7:0]: This is the least significant byte of the Maximum Buffer Count register (BKMAXA).

117 MAXIMUM BUFFER COUNT A 1 REGISTER (117h (116h), R/W, BKMAXA_1)

7:0 (R/W) (BKMAXA[15:8]) - MAXIMUM BUFFER COUNT A[15:8]: This is the most significant byte of the Maximum Buffer Count register (BKMAXA).

BKMAX[15:0] is a value that represents the maximum number of sectors that can fit in a circular buffer (minus one or two sectors to make room for error handling to prevent data corruption), and is used in conjunction with the Buffer Counter (BCTR) whenever buffer room logic is enabled. BKMAXA is used in conjunction with BCTRA while BCTRA is selected by either the HBCTRSEL bit (reg. 133h, R/W, bit 1), the AWBCTRSEL bit (reg. 133h, R/W, bit 4), or the DBCTRSEL bit (reg. 137h, R/W, bit 1).

118 BUFFER COUNTER B 0 REGISTER (118h (119h), R/W, BCTRB_0)

7:0 (R/W) (BCTRB[7:0]) - BUFFER COUNTER B[7:0]: This is the least significant byte of the Buffer Counter B (BCTRB) register.

119 BUFFER COUNTER B 1 REGISTER (119h (118h), R/W, BCTRB_1)

7:0 (R/W) (BCTRB[15:8]) - BUFFER COUNTER B[15:8]: This is the most significant byte of the Buffer Counter B (BCTRB) register.

The Buffer Counter (BCTR) is used for keeping track of the number of sectors in the buffer and controls the starting and stopping of disk and host transfers through the buffer room logic when enabled. It is a two's complement counter, where a negative count is indicated by bit 15 being set. Enabling Buffer Counter operation and the room logic for host and disk transfers is controlled separately through the register bits shown below, so that the user has the flexibility of enabling them for both the Host and Disk, only the Host, only the Disk, or neither one.

for Host transfers: HBCTRSEL and ENHROOM bits (reg. 133h, R/W, bits 1 and 0)
or
AWBCTRSEL and ENAWROOM bits (reg. 133h, R/W, bits 4 and 3)

for Disk transfers: DBCTRSEL and ENDROOM bits (reg. 137h, R/W, bits 1 and 0)

11A MAXIMUM BUFFER COUNT B 0 REGISTER (11Ah (11Bh), R/W, BKMAXB_0)

7:0 (R/W) (BKMAXB[7:0]) - MAXIMUM BUFFER COUNT B[7:0]: This is the least significant byte of the Maximum Buffer Count register (BKMAXB).

11B MAXIMUM BUFFER COUNT B 1 REGISTER (11Bh (11Ah), R/W, BKMAXB_1)

7:0 (R/W) (BKMAXB[15:8]) - MAXIMUM BUFFER COUNT B[15:8]: This is the most significant byte of the Maximum Buffer Count register (BKMAXB).

BKMAX[15:0] is a value that represents the maximum number of sectors that can fit in a circular buffer (minus one or two sectors to make room for error handling to prevent data corruption), and is used in conjunction with the Buffer Counter (BCTR) whenever buffer room logic is enabled. BKMAXB is used in conjunction with BCTRB while BCTRB is selected by either the HBCTRSEL bit (reg. 133h, R/W, bit 1), the AWBCTRSEL bit (reg. 133h, R/W, bit 4), or the DBCTRSEL bit (reg. 137h, R/W, bit 1).

11C SERVO BEGIN OF SEGMENT 0 REGISTER (11Ch (11Dh), R/W, VBOS_0)

7:0 (R/W) (VBOS[7:0]) - SERVO BEGIN OF SEGMENT: This is the least significant byte of the Servo Begin of Segment Pointer (VBOS).

11D SERVO BEGIN OF SEGMENT 1 REGISTER (11Dh (11Ch), R/W, VBOS_1)

7:5 (R/W) Reserved

4:0 (R/W) (VBOS[12:8]) - SERVO BEGIN OF SEGMENT: This is the most significant bits of the Servo Begin of Segment Pointer (VBOS).

11E SERVO END OF SEGMENT 0 REGISTER (11Eh (11Fh), R/W, VEOS_0)

7:0 (R/W) (VEOS[7:0]) - SERVO END OF SEGMENT: This is the least significant byte of the Servo End of Segment Pointer (VEOS).

11F SERVO END OF SEGMENT 1 REGISTER (11Fh (11Eh), R/W, VEOS_1)

7:5 (R/W) Reserved

4:0 (R/W) (VEOS[12:8]) - SERVO END OF SEGMENT: This is the most significant bits of the Servo End of Segment Pointer (VEOS).

VBOS and VEOS (regs. 11Ch-11Fh, R/W) define the begin and end of the Servo Segment which is located within the 8KByte Servo Page defined by the VPAGE Registers (regs. 112h/113h, R/W).

120 SECTOR SIZE 0 REGISTER (120h (121h), R/W, SECSIZE_0)

7:0 (R/W) (SECSIZE[7:0]) - SECTOR SIZE[7:0]: This is the least significant byte of the Sector Size register (SECSIZE) which defines the number of bytes per sector.

121 SECTOR SIZE 1 REGISTER (121h (120h), R/W, SECSIZE_1)

7:3 (R/W) Reserved

2:0 (R/W) (SECSIZE[10:8]) - SECTOR SIZE[10:8]: These are the most significant bits of the Sector Size register (SECSIZE) which defines the number of bytes per sector.

124 HOST BYTE COUNTER 0 REGISTER (124h (125h), R, HBC_0)

7:0 (R) (HBC[7:0]) - HOST BYTE COUNTER 0 [7:0]: These are the least significant eight bits of the Host Byte Counter.

125 HOST BYTE COUNTER 1 REGISTER (125h (124h), R, HBC_1)

7:3 (R) Reserved

2:0 (R) (HBC[10:8]) - HOST BYTE COUNTER 1 [10:8]: These are the most significant bits of the Host Byte Counter.

The Host Byte Counter (HBC) is an 11-bit down counter that counts bytes within a data block that is transferred between buffer memory and the Host FIFO. It is initialized to 0 by the microprocessor when it writes a 1 to the HBCCLR bit in the BCTRCTL register (reg. 108h, R/W, bit 6). It is also automatically cleared at the start of an Auto Write operation.

When the first word of a data block is transferred between the Host FIFO and buffer, the HBC wraps to a value that corresponds to the number of data bytes remaining to be transferred for that data block.

After the HBC wraps, it decrements by 1 (8-bit mode) or 2 (16-bit mode) for every word transferred. It returns to zero when the whole data block has been transferred. In 16-bit mode, if the data block contains an odd number of bytes, then the HBC will decrement from 1 to 0 when the last byte of the data block is transferred. The HBC is used by the Buffer Counters block for auto decrementing the BCTR selected for the host port, if any, for every data block transferred.

The HBC can be cleared by the microprocessor by setting the HBCCLR bit (reg. 108h, R/W, bit 6).

126 DISK BYTE COUNT 0 REGISTER (126h (127h), R, DBC_0)

7:0 (R) (DBC[7:0]) - DISK BYTE COUNT[7:0]: These are the least significant bits of the Disk Byte Count 0 register.

127 DISK BYTE COUNT 1 REGISTER (127h (126h), R, DBC_1)

7:3 (R) Reserved

2:0 (R) (DBC[10:8]) - DISK BYTE COUNT[10:8]: These are the most significant bits of the Disk Byte Count (DBC) register which counts bytes within a sector transferred between buffer and the Disk FIFO. The DBC bits can be cleared by the microprocessor via the DBCCLR bit in the BCTRCTL register (reg. 108h, R/W, bit 5).

The Disk Byte Counter (DBC) is an 11-bit down counter that counts bytes within a sector. It is initialized to 0 by the microprocessor when it writes a 1 to the DBCCLR bit (reg. 108h, R/W, bit 5). Note that writing a 1 to DBCCLR will also reset the Disk FIFO in the Disk controller block.

When the first word of a sector is transferred between disk and buffer, the DBC wraps to a value that corresponds to the number of bytes remaining to be transferred for that sector. That value is a function of the BEN16BIT bit (reg. 100h, R/W, bit 2, a 0 selects 8-bit and a 1 selects 16-bit) as shown in the following table.

BEN16BIT	DBC Wrap Value
0	SECSIZE - 1
1	SECSIZE - 2

After the first word of a sector is transferred, the DBC decrements by 1 (8-bit mode) or 2 (16-bit mode) for every word transferred. It returns to zero when a whole sector has been transferred.

The DBC keeps track of sector boundaries for the Correction Port which performs ECC correction on sector data. It is also used for incrementing the BCTR selected for the disk port, if any, for every good data block transferred between disk and buffer.

The microprocessor can read the contents of the DBC via the DBC_0 and DBC_1 registers (regs. 126h/ 127h, R).

12C SERVO POINTER 0 REGISTER (12Ch (12Dh), R/W, VP_0)

7:0 (R/W) (VP[7:0]) - SERVO POINTER [7:0]: These are the least significant bits of the Servo Pointer register.

12D SERVO POINTER 1 REGISTER (12Dh (12Ch), R/W, VP_1)

7:5 (R/W) Reserved

4:0 (R/W) (VP[12:8]) - SERVO POINTER[12:8]: These are the most significant bits of the Servo Pointer register.

The Servo Pointer is used to access the Servo Segment for data split values to be loaded into the CDR FIFO. The Servo Pointer is used as an offset into the Servo Page determined by the Servo Page registers (reg. 112h, 113h, R/W).

The Servo Segment is located within the Servo Page and is defined by the Servo Begin of Segment (regs. 11Ch, 11Dh, R/W) and Servo End of Segment (regs. 11Eh, 11Fh, R/W) Registers.

12E DISK UP COUNTER 0 REGISTER (12Eh (12Fh), R/W, DUCTR_0)

7:0 (R/W) (DUCTR[7:0]) - DISK UP COUNTER[7:0]: This is the least significant byte of the Disk Up Counter register.

12F DISK UP COUNTER 1 REGISTER (12Fh (12Eh), R/W, DUCTR_1)

7:2 (R/W) Reserved

1:0 (R/W) (DUCTR[9:8]) - DISK UP COUNTER[9:8]: These are the most significant bits of the Disk Up Counter register.

The Disk Up Counter is enabled for use via the ENDUCTR bit (reg. 102h, R/W, bit 7). Whenever the ENDUCTR bit is cleared, the Disk Up Counter will be forced to 00h. While ENDUCTR is set, the Disk Up Counter will increment by one whenever a sector without error is transferred from the disk into the buffer or whenever a sector just transferred into the buffer has been successfully corrected.

130 HOST POINTER 0 REGISTER (130h (133h), R/W, HP_0)

7:0 (R/W) (HP[7:0]) - HOST POINTER 0 [7:0]: This register contains the least significant eight bits of the Host Pointer.

131 HOST POINTER 1 REGISTER (131h (132h), R/W, HP_1)

7:0 (R/W) (HP[15:8]) - HOST POINTER 1 [15:8]: This register contains the middle eight bits of the Host Pointer.

132 HOST POINTER 2 REGISTER (132h (131h), R/W, HP_2)

7:6 (R/W) Reserved

5:0 (R/W) (HP[21:16]) - HOST POINTER 2 [21:16]: These bits are the most significant bits of the Host Pointer.

The Host Pointer (HP) is used to generate the Buffer Address during transfers between the buffer and the Host FIFO. It is a 22-bit up counter which is automatically incremented during transfers, and automatically wraps from the end of segment to the beginning of segment. Writing to these registers while AWSEL=1 (reg. 10Bh, R/W, bit 0) has no affect.

133 HOST SEGMENT CONTROL REGISTER (133H (130H), R/W, HSCTL)

7:6 (R/W) (AWMODE[1:0]) - AUTO WRITE MODE[1:0]: These bits select if and how the Host Pointer (HP_0/1/2, regs 130h-132h, R/W) is loaded at the start of an Auto-Write transfer, as follows:

AWMODE[1:0]	Description
0 0	Do not load HP at start of Auto-Write.
0 1	Load HP from selected Begin of Segment Pointer (xBOS) at start of Auto-Write
1 0	Load HP from Write Cache Pointer (WCP) at start of Auto-Write
1 1	Reserved

5 (R/W) (AWSEGSEL) - AUTO WRITE SEGMENT SELECT: This bit selects the buffer segment to be used for Auto-Write host transfers (when AWSEL, reg. 10Bh, R/W, bit 0, is set). A value of 0 selects Segment A, while a value of 1 selects Segment B.

4 (R/W) (AWBCTRSEL) - AUTO WRITE BCTR SELECT: This bit selects which buffer counter is used for Auto-Write host transfers when the ENAWROOM bit (of this register) is set. A value of 0 selects BCTRA, while a value of 1 selects BCTRB.

3 (R/W) (ENAWROOM) - ENABLE AUTO WRITE ROOM LOGIC: Setting this bit enables the buffer room logic for auto write host transfers.

2 (R/W) (HSEGSEL) - HOST SEGMENT SELECT: This bit selects the buffer segment to be used for non-Auto Write host transfers (when AWSEL, reg. 10Bh, R/W, bit 0, is cleared). A value of 0 selects Segment A, while a value of 1 selects Segment B.

1 (R/W) (HBCTRSEL) - HOST BCTR SELECT: This bit selects which buffer counter is used for non-Auto-Write host transfers when the ENHROOM bit (in this register) is set. A value of 0 selects BCTRA, while a value of 1 selects BCTRB.

0 (R/W) (ENHROOM) - ENABLE HOST ROOM LOGIC: Setting this bit enables the buffer room logic for non-auto write host transfers. The associated BCTR will not decrement while this bit is cleared.

134 DISK POINTER 0 REGISTER (134h (137h), R/W, DP_0)

7:0 (R/W) (DP[7:0]) - DISK POINTER[7:0]: This register contains the least significant byte of the Disk Pointer (DP).

135 DISK POINTER 1 REGISTER (135h (136h), R/W, DP_1)

7:0 (R/W) (DP[15:8]) - DISK POINTER[15:8]: This register contains the middle byte of the Disk Pointer (DP).

136 DISK POINTER 2 REGISTER (136h (135h), R/W, DP_2)

7:6 (R/W) Reserved

5:0 (R/W) (DP[21:16]) - DISK POINTER[21:16]: This register contains the most significant six bits of the Disk Pointer (DP).

The Disk Pointer is used to generate the Buffer Address during transfers between the buffer and the Disk FIFO. It is a 22-bit up counter which is automatically incremented during disk transfers, and automatically wraps from begin of Segment to end of Segment.

137 DISK SEGMENT CONTROL REGISTER (137h (134h), R/W, DSCTL)

7:3 (R/W) Reserved

2 (R/W) (DSEGSEL) - DISK SEGMENT SELECT: This bit selects the buffer segment to be used for disk transfers. A value of 0 selects Segment A, while a value of 1 selects Segment B.

1 (R/W) (DBCTRSEL) - DISK BCTR SELECT: This bit selects the buffer counter to be used for disk transfers when the ENDROOM bit (in this register) is set. A value of 0 selects BCTRA, while a value of 1 selects BCTRB.

0 (R/W) (ENDROOM) - ENABLE DISK ROOM LOGIC: Setting this bit enables the buffer room logic for disk transfers. It is automatically set at the end of a disk segment if ENDRM-WRAP=1 (reg. 102h, R/W, bit 3). The associated BCTR will not increment while this bit is cleared

138 BEGIN OF SEGMENT A PTR 0 REGISTER (138h (13Bh), R/W, ABOS_0)

7:0 (R/W) (ABOS[7:0]) - BEGIN OF SEGMENT A POINTER[7:0]: This register contains the least significant byte of the Begin Of Segment A Pointer.

139 BEGIN OF SEGMENT A PTR 1 REGISTER (139h (13Ah), R/W, ABOS_1)

7:0 (R/W) (ABOS[15:8]) - BEGIN OF SEGMENT A POINTER[15:8]: This register contains the middle byte of the Begin Of Segment A Pointer.

13A BEGIN OF SEGMENT A PTR 2 REGISTER (13Ah (139h), R/W, ABOS_2)

7:6 (R/W) Reserved

5:0 (R/W) (ABOS[21:16]) - BIGIN OF SEGMENT A POINTER[21:16]: This register contains the most significant six bits of the Begin Of Segment A Pointer.

13B RESERVED (13Bh (138h), R/W)

7 (R/W) Reserved

13C END OF SEGMENT A PTR 0 REGISTER (13Ch (13Fh), R/W, AEOS_0)

7:0 (R/W) (AEOS[7:0]) - END OF SEGMENT APOINTER[7:0]: This register contains the least significant byte of the End Of Segment A Pointer.

13D END OF SEGMENT A PTR 1 REGISTER (13Dh (13Eh), R/W, AEOS_1)

7:0 (R/W) (AEOS[15:8]) - END OF SEGMENT A POINTER[15:8]: This register contains the middle byte of the End Of Segment A Pointer.

13E END OF SEGMENT A PTR 2 REGISTER (13Eh (13Dh), R/W, AEOS_2)

7:6 (R/W) Reserved

5:0 (R/W) (AEOS[21:16]) - END OF SEGMENT A POINTER[21:16]: This register contains the most significant six bits of the End Of Segment A Pointer.

13F RESERVED (13Fh (13Ch), R/W)

7 (R/W) Reserved

140 BEGIN OF SEGMENT B PTR 0 REGISTER (140h (143h), R/W, BBOS_0)

7:0 (R/W) (BBOS[7:0]) - BEGIN OF SEGMENT B POINTER[7:0]: This register contains the least significant byte of the Begin Of Segment B Pointer.

141 BEGIN OF SEGMENT B PTR 1 REGISTER (141h (142h), R/W, BBOS_1)

7:0 (R/W) (BBOS[15:8]) - BEGIN OF SEGMENT B POINTER[15:8]: This register contains the middle byte of the Begin Of Segment B Pointer.

142 BEGIN OF SEGMENT B PTR 2 REGISTER (142h (141h), R/W, BBOS_2)

7:6 (R/W) Reserved

5:0 (R/W) (BBOS[21:16]) - BIGIN OF SEGMENT B POINTER[21:16]: This register contains the most significant six bits of the Begin Of Segment B Pointer.

143 RESERVED (143h (140h), R/W)

7 (R/W) Reserved

144 END OF SEGMENT B PTR 0 REGISTER (144h (147h), R/W, BEOS_0)

7:0 (R/W) (BEOS[7:0]) - END OF SEGMENT B POINTER[7:0]: This register contains the least significant byte of the End Of Segment B Pointer.

145 END OF SEGMENT B PTR 1 REGISTER (145h (146h), R/W, BEOS_1)

7:0 (R/W) (BEOS[15:8]) - END OF SEGMENT B POINTER[15:8]: This register contains the middle byte of the End Of Segment B Pointer.

146 END OF SEGMENT B PTR 2 REGISTER (146h (145h), R/W, BEOS_2)

7:6 (R/W) Reserved

5:0 (R/W) (BEOS[21:16]) - END OF SEGMENT B POINTER[21:16]: This register contains the most significant six bits of the End Of Segment B Pointer.

147 RESERVED (147h (144h), R/W)

7 (R/W) Reserved

148 WRITE CACHE POINTER 0 REGISTER (148h (14Bh), R/W, WCP_0)

7:0 (R/W) (WCP[7:0]) - WRITE CACHE POINTER[7:0]: This register contains the least significant eight bits of the Write Cache Pointer (WCP) which points to the start of the next auto write sector in the buffer.

149 WRITE CACHE POINTER 1 REGISTER (149h (14Ah), R/W, WCP_1)

7:0 (R/W) (WCP[15:8]) - WRITE CACHE POINTER[15:8]: This register contains the middle significant eight bits of the Write Cache Pointer (WCP) which points to the start of the next auto write sector in the buffer.

14A WRITE CACHE POINTER 2 REGISTER (14Ah (149h), R/W, WCP_2)

7:6 (R/W) Reserved

5:0 (R/W) (WCP[21:16]) - WRITE CACHE POINTER[21:16]: This register contains the most significant six bits of the Write Cache Pointer (WCP) which points to the start of the next auto write sector in the buffer.

14B RESERVED (14Bh (148h), R/W)

7:0 (R/W) Reserved

14C AUTO WRITE SAVE 0 REGISTER (14Ch (14Fh), R/W, AWSAVE_0)

7:0 (R/W) (AWSAVE[7:0]) - AUTO WRITE SAVE POINTER[7:0]: This register contains the least significant eight bits of the Auto Write Save Pointer (AWSAVE) which stores the value of the Host Pointer (HP) at which the last auto write transfer started.

14D AUTO WRITE SAVE 1 REGISTER (14Dh (14Eh), R/W, AWSAVE_1)

7:0 (R/W) (AWSAVE[15:8]) - AUTO WRITE SAVE POINTER[15:8]: This register contains the middle byte of the Auto Write Save Pointer (AWSAVE) which stores the value of the Host Pointer (HP) at which the last auto write transfer started.

14E AUTO WRITE SAVE 2 REGISTER (14Eh (14Dh), R/W, AWSAVE_2)

7:0 (R/W) (AWSAVE[21:16]) - AUTO WRITE SAVE POINTER[21:16]: This register contains the middle bits of the Auto Write Save Pointer (AWSAVE) which stores the value of the Host Pointer (HP) at which the last auto write transfer started.

5.6 Disk Sequencer RAM Register Descriptions

The register summarized in this section are the registers that are loaded by the user to create an appropriate Sequencer Map to execute disk read and write functions. These registers are discussed in depth in the section on the Disk Sequencer Map.

200-21F SEQ. NEXT ADDRESS/DATA REGISTERS (200h - 21Fh, R/W, SEQNADAT)

7:5 (R/W) (BRSEL[2:0]/SEQDATA[7:5]) - BRANCH SELECT[2:0]/SEQUENCER DATA[7:5]: The function of these three field bits is determined by the NEXTADREN bit (SEQCTL, bit 7). If NEXTADREN is set, these three bits function as the Next Address Condition field. If NEXTADREN is cleared, these three field bits form the three most significant bits of the Data Field.

4:0 (R/W) (SEQNAD[4:0]/SEQDATA[4:0]) - SEQ. NEXT ADDR[4:0]/SEQ. DATA[4:0]:]: The function of these five field bits is determined by the NEXTADREN bit (SEQCTL, bit 7). If NEXTADREN is set, these five bits function as the Next Address field. If NEXTADREN is cleared, these five field bits form the five least significant bits of the Data Field.

240-25F SEQUENCER CONTROL REGISTERS (240h - 25Fh, R/W, SEQCTL)

7 (R/W) (NEXTADREN) - NEXT ADDRESS ENABLE: This bit determines the usage of the SEQNADAT field.

6:5 (R/W) (SEQCTLA[1:0]) - SEQUENCER CONTROL A[1:0]: Miscellaneous control bits used in the operation of the Disk Sequencer.

4:3 (R/W) (SEQCTLB[1:0]) - SEQUENCER CONTROL B[1:0]: Miscellaneous control bits used in the operation of the Disk Sequencer.

2:0 (R/W) (SEQCTLC[2:0]) - SEQUENCER CONTROL C[2:0]: Miscellaneous control bits used in the operation of the Disk Sequencer.

280-29F SEQUENCER COUNT FIELD REGISTERS (280h - 29Fh, R/W, SEQCNT)

7 (R/W) (MODCNTEN) - MODULO 64 COUNT ENABLE: When this bit is set to 1 the Sequencer Count is Modulo 64. For every 64 bytes the SEQCNT[6:0] is decremented by one. When this bit is cleared the counter is a normal 7 bit down counter and is decremented.

6:0 (R/W) (SEQCNT[6:0]) - SEQUENCER COUNT[6:0]: These bits normally define the Sequencer Byte Count minus 1. In certain instructions they can define a bit significant Compare Mask or a Buffer CDR Fetch Count.

NOTE: In either normal mode or Modulo 64 mode the counter must be loaded with the desired count minus 1.

5.7 PCMCIA Interface Register Descriptions

This section describes the registers which are loaded and read by the host to facilitate PCMCIA command execution.

5.7.1 Card Information Structure (000h-1FFh, R, CIS)

These 256 bytes of read-only memory contain the Card Information Structure. This structure defines the characteristics of the card, including: card type, speed, card power requirements, memory and/or I/O addresses used to access, etc.

This structure is written at power-on time by the microprocessor when the PCMCIA RDY/*BSY signal is low. Its content is not affected by any reset other than *POR. Its content is user definable.

5.7.2 PCMCIA Registers

200 PCMCIA CONFIG OPTION REGISTER (200h, R/W, PCMCONFIGOPT)

7 (R/W) (SRESET) - PCMCIA SOFT RESET: The host will write a one to generate a PCMCIA soft reset, and a zero to clear the reset. The functionality of this reset is the same as *HRST signal and it clears the PCMCIA interface block. This forces the card to Memory addressing mode (Configuration Index = 0)

6 (R/W) (LEVLREQ) - PCMCIA LEVEL INTERRUPT: Determines the type of interrupt. A one signifies level mode interrupt and a zero indicates pulsed mode interrupt. In pulsed interrupt mode, an active LOW pulse of > 0.5usec will be generated.

5 () Reserved

4 (R/W) (CONFIGOPT4) - CONFIGURATION OPTION BIT 4: The content of this bit is reflected by the corresponding bit in Register E0h in the address space of the microprocessor. Thus it can be used to transfer data from host to local microprocessor.

3:0 (R/W) (CONFIGIDX[3:0]) - CONFIGURATION INDEX: These bits select the access mode as described in the table below. The configuration index is an entry in the Device Configuration tuple of the Card Information Structure (CIS). The host should read CIS memory before trying to initialize this register.

CONFIGIDX[3:0]	Access Mode
0	Memory Mode (power-on reset default)
1	Block I/O Mode
2	Primary I/O Mode (I/O Address 1F0-1F7h and 3F6-3F7h)
3	Secondary I/O Mode (I/O Address 170-177h and 376-377h)
4	Primary I/O Mode with Floppy Support
5	Secondary I/O Mode with Floppy Support
6-16	Reserved

202 PCMCIA CONFIG STATUS REGISTER (202h, R/W, PCMCONFIGSTAT)

7 (R) (CHANGED) - PIN REPLACEMENT REGISTER BIT CHANGED: This ***read only*** bit indicates that one or more bits CBVD1, CBVD2, CRDY/*BSY, or CWPROT in the PCMCIA Pin Replacement Register (PCMPINREPLACE, reg. 204h, bits 7-4, respectively) is set to one. This signal drives the *STSCHG pin in I/O mode if SIGCHG is set (bit 6 of this register).

6 (R/W) (SIGCHG) - ENABLE CHANGED STATUS ON *STSCHG SIGNAL: When this bit is set and card is configured for I/O interface, the CHANGED bit (bit 7 of this register) drives *STSCHG pin. If no state change signal is desired, this bit should be cleared to 0 and *STSCHG will be held high.

5 (R/W) (IOIS8) - HOST IS ONLY 8 BIT: It is set by host when it only supports 8-bit data transfers.

4:3 (R/W) (CONFIGSTAT[4:3]) - CONFIG STATUS BIT 4-3: The content of these bits is reflected by the corresponding bits in the Configuration Status Register (reg. E1h, R, bits 4:3) in the address space of the microprocessor. Thus these bits can be used to transfer data from host to local microprocessor.

2 (R/W) (PWRDWN) - POWER DOWN: This bit is set by host to place the card in a low power mode.

1 (R) (INTR) - ATA INTERRUPT: This ***read only*** bit shows the internal state of ATA IRQ signal. In Primary/Secondary I/O Mode, if *INTEN bit in AT Host Fixed Disk register (ATA reg. 3F6h, W, bit 1) is set, then this bit reflects the state of ATA interrupt request signal. This bit is inactive if *INTEN bit is cleared.

0 (R/W) (CONFIGSTAT[0]) - CONFIG STATUS BIT 0: The content of this bit is reflected by the corresponding bit in the Configuration Status Register (reg. E1h, R, bit 0) in the address space of the microprocessor. Thus this bit can be used to transfer data from host to local microprocessor.

204 PCMCIA PIN REPLACEMENT REGISTER (204h, R/W, PCMPINREPLACE)

7 (R/W) (CBVD1) - BVD1 CHANGE STATE: This bit may be written by host. Writing to this bit is allowed if bit 3 of this register is set at the same time that this bit is being written.

6 (R/W) (CBVD2) - BVD2 CHANGE STATE: This bit may be written by host. Writing to this bit is allowed if bit 2 of this register is set at the same time that this bit is being written.

5 (R/W) (CRDY/*BSY) - RDY/*BSY CHANGE STATE: This bit is set when internal Ready/*Busy signal changes state. This bit may be written by host. Writing to this bit is allowed if bit 1 of this register is set at the same time that this bit is being written.

4 (R/W) (CWPROT) - WPROT CHANGE STATE: This bit may be written by host. Writing to this bit is allowed if bit 0 of this register is set at the same time that this bit is being written.

3 (R/W) (RBVD1) - BVD1 STATUS: This bit is not used and always returns a status 1 for good battery level. Writing a 1 to this bit enables writes to bit 7 of this register.

2 (R/W) (RBVD2) - BVD2 STATUS: This bit is not used and always returns a status 1 for good battery level. Writing a 1 to this bit enables writes to bit 6 of this register.

1 (R/W) (RRDY/*BSY) - RDY/*BSY STATUS: This bit represents the internal state of Ready/*Busy signal. When this bit is set by host, the corresponding CRDY/*BSY bit is also written. When this bit is reset by host, CRDY/*BSY bit is unaffected.

0 (R/W) (RWPROT) - WPROT STATUS: This bit is not used and always returns a status 0 for no write protection. Writing a 1 to this bit enables writes to bit 4 of this register.

206 PCMCIA SOCKET COPY REGISTER (206h, R/W, PCMSOCKETCOPY)

This register supports PCMCIA-ATA twin card mode. This would allow two cards to operate at the same I/O address (similar to ATA Master/Slave mode). This register is always written by the host before writing to the card's Configuration Index (reg. 200h, R/W, bits 2-0). The drive's microprocessor would use the value written by host (0 or 1) to program HIF to respond to the Master address (0) or Slave address (1).

7 (R/W) Reserved

6:4 (R/W) (COPY[2:0) - COPY NUMBER: These bits indicate to the card the copy number it has been assigned by the host. This permits identical cards to share a common set of I/O addresses while remaining uniquely identifiable, and consecutively ordered. The first copy number is 0.

3:0 (R/W) (SOCKET[3:0]) - SOCKET NUMBER: These bits indicate to the card the socket it is located in. The first socket number is 0.

5.8 AT Interface Register Descriptions

This section describes the registers which are loaded and read by the host to facilitate AT command execution.

5.8.1 AT Task File/Command Block Registers

The AT Task File registers are used in either CHS (Cylinder/Head/Sector) mode or in LBA (Logical Block Address) mode. Its usage is determined by the LBA bit (reg. 1F6h, R/W, bit 6). This mode of operation will only be recognized by the AIC-8375 device when the Enable LBA Mode bit (reg. C3h, R/W, bit 3) is set.

Table 5-1 AT Task File/Command Registers (definition during CHS mode)

I/O Address	Read	Write
1F0/170h	Data register	Data register
1F1/171h	Error register	Features register
1F2/172h	Sector Count	Sector Count
1F3/173h	Sector Number	Sector Number
1F4/174h	Cylinder Low	Cylinder Low
1F5/175h	Cylinder High	Cylinder High
1F6/176h	Drive/Head	Drive/Head
1F7/177h	Controller/Drive Status	Command

Table 5-2 AT Task File/Command Registers (definition during LBA mode)

I/O Address	Read	Write
1F0/170h	Data register	Data register
1F1/171h	Error register	Features register
1F2/172h	Sector Count	Sector Count
1F3/173h	LBA A7:A0	LBA A7:A0
1F4/174h	LBA A15:A8	LBA A15:A8
1F5/175h	LBA A23:A16	LBA A23:A16
1F6/176h	LBA A27:A24/Drive	LBA A27:A24/Drive
1F7/177h	Controller/Drive Status	Command

1F0/170h AT HOST DATA REGISTER (1F0/170h, R/W, H_DATA)

7:0 (R/W) (H_DATA[7:0]) - AT HOST DATA [7:0]: This register is used by the host to access the buffer memory during read and write operations and must not be accessed unless a read or write command is being executed. This register provides a 16-bit path to or from the buffer memory unless it is being used to transfer ECC data when it is 8-bits wide. This register may only be accessed by the host when the Data Request bit (DRQ, reg. 177h/1F7h, bit 3) is set.

1F1/171h AT HOST ERROR REGISTER (1F1/171h, R, H_ERROR)

7:0 (R) (H_ERROR[7:0]) - AT HOST ERROR [7:0]: This register reflects the contents of the Microprocessor AT Error register (reg. A0h, R/W) and contains specific error information about the last failed command. During diagnostics or on power-up, this register contains controller diagnostic errors. If an error occurs, the microprocessor loads the Microprocessor AT Error register and then sets the Error bit (reg. C1h, R/W, bit 0) which in turn sets the AT Error bit (reg. 177h/1F7h, R, bit 0).

1F1/171h AT HOST FEATURES REGISTER (1F1/171h, W, H_FEATRS)

7:0 (W) (H_FEATRS{7:0]) - AT HOST FEATURES [7:0]: This register is command specific and may be used by the host to enable or disable features of the interface or drive. This register may be ignored by some drives. Some hosts, based upon definitions prior to the formalization of the ATA specification, used this register to designate a recommended Write Pre compensation Cylinder value. This register can be accessed by the local microprocessor via the Microprocessor AT Features register (reg. A1h, R/W).

1F2/172h AT HOST SECTOR COUNT REGISTER (1F2/172h, R/W, H_SECCNT)

7:0 (R/W) (H_SECCNT[7:0]) - AT HOST SECTOR COUNT [7:0]: This register contains the number of sectors to be transferred during any Host PIO or DMA transfers. This register can be accessed via the Microprocessor AT Sector Count register (reg. A2h, R/W).

1F3/173h AT HOST SECTOR NUMBER REG. (1F3/173H, R/W, H_SECNUM)

7:0 (R/W) (H_SECNUM[7:0]) - AT HOST SECTOR NUMBER [7:0]: The contents of this register specifies the sector number for the current PIO or DMA command. This register can be accessed via the Microprocessor AT Sector Number register (reg. A3h, R/W).

In LBA mode, this register contains LBA bits A7:A0. At the end of the command, this register is updated to reflect the current LBA bits A7:A0.

1F4/174h AT HOST CYLINDER LOW REGISTER (1F4/174h, R/W, H_CYLLO)

7:0 (R/W) (H_CYLLO[7:0]) - AT HOST CYLINDER LOW [7:0]: This register contains the lower byte of the 16 bit Cylinder Number. It can be accessed by the local microprocessor via the Microprocessor AT Cylinder Low register (reg. A4h, R/W).

In LBA mode, this register contains LBA bits A15:A8. At the end of the command, this register is updated to reflect the current LBA bits A15:A8.

1F5/175h AT HOST CYLINDER HIGH REGISTER (1F5/175h, R/W, H_CYLHI)

7:0 (R/W) (H_CYLHI[7:0]) - AT HOST CYLINDER HIGH [7:0]: This register contains the upper byte of the 16 bit Cylinder Number. It can be accessed by the local microprocessor via the Microprocessor AT Cylinder High register (reg. A5h, R/W).

In LBA mode, this register contains LBA bits A23:A16. At the end of the command, this register is updated to reflect the current LBA bits A23:A16.

1F6/176h AT HOST DRIVE/HEAD REGISTER (1F6/176h, R/W, H_DRVHD)

This register can be accessed via the AT Microprocessor Drive/Head register (reg. A6h, R/W). This register is cleared when the HRST signal, the *POR signal, or RESET (reg. 3F6h/376h, bit 2) is asserted. It is also cleared when a Diagnostic command (90h) is issued by the host.

The AIC-8375 device utilization of this register in LBA mode conforms to the ATA specification as follows:

7 (R/W) Reserved. This bit must be set to 1 to conform to the ATA specification.

6 (R/W) (LBA) - LOGICAL BLOCK ADDRESS MODE: When set, this bit establishes Task File usage in LBA mode. When cleared, CHS mode is used.

5 (R/W) Reserved. This bit must be set to 1 to conform to the ATA specification.

4 (R/W) (DRV) - DRIVE NUMBER SELECT: When set, this bit selects Drive 1. When reset, Drive 0 is selected. Drive Select 1 and 0 (reg. 3F7h, R, bits 1:0) will directly be affected by this bit.

3:0 (R/W) (LBA A27:A24) - LOGICAL BLOCK ADDRESS A27:A24: These bits contain the highest order Logical Block Address bits.

The AIC-8375 device utilization of this register in CHS mode conforms to the ATA specification as follows:

7 (R/W) Reserved. This bit must be set to 1 to conform to the ATA specification.

6 (R/W) (LBA) - LOGICAL BLOCK ADDRESS MODE: When set, this bit establishes Task File usage in LBA mode. When cleared, CHS mode is used.

5 (R/W) Reserved. This bit must be set to 1 to conform to the ATA specification.

4 (R/W) (DRV) - DRIVE NUMBER SELECT: When set, this bit selects Drive 1. When reset, Drive 0 is selected. Drive Select 1 and 0 (reg. 3F7h, R, bits 1:0) will directly be affected by this bit.

3:0 (R/W) (HS[3:0]) - AT HEAD SELECT [3:0]: These bits contain the Head number for the current PIO or DMA location.

To accommodate older BIOS implementations, the following use of this register is allowed. The Enable LBA Mode bit (reg. C3h, R/W, bit 3) must be cleared in this case.

7:5 (R/W) (PASS[2:0]) - PASS THRU [2:0]: These bits are used to pass information between the host and the drive.

4 (R/W) (DRV) - DRIVE NUMBER SELECT: When set, this bit selects Drive 1. When reset, Drive 0 is selected. Drive Select 1 and 0 (reg. 3F7h, R, bits 1:0) will directly be affected by this bit.

3:0 (R/W) (HS[3:0]) - AT HEAD SELECT [3:0]: These bits contain the Head number for the current PIO or DMA location.

1F7/177h AT HOST STATUS REGISTER (1F7/177h, R, H_STAT)

This register can be accessed by the host at any time. However, when the BSY bit is set, the other bits in this register are not valid. A read of this register by the host clears the Host Interrupt (IRQ). When master-slave mode is selected (MSEN, reg. C0h, R/W, bit 1 set), this register always returns the status from Drive 0 which will reflect the status of that physical drive. The following table shows which drive returns status via this register based on the Master/Slave Enable bit (MSEN) and the Drive Number Select bit (DRV, reg. 1F6h, R/W, bit 4).

MSEN Reg. C0h, bit 1	DRV Reg. 1F6h, bit 4	H_STAT Register Used
0	0	Drive 0 Stat. Reg. (reg. B4h, R/W)
0	1	Drive 1 Stat. Reg. (reg. B5h, R/W)
1	0	Drive 0 Stat. Reg. (reg. B4h, R/W)
1	1	Drive 0 Stat. Reg. (reg. B4h, R/W)

7 (R) (BSY) - BUSY: When this bit is set, the local microprocessor has access to the AT Task File registers, and the host cannot access any registers other than H_STAT (this register), H_ALSTAT (reg. 3F6h, R), H_DVCTL (reg. 3F6h, W), or H_DRVADD (reg. 3F7h, R). This bit is set whenever the Internal Busy Latch (IBSY, reg. C1h, R/W, bit 7) is set and the Data Request bit (DRQ) in this register is reset.

6 (R) (DRDY) - DRIVE READY: When set, this bit indicates that the selected drive is capable of responding to a command. This bit is set or reset via the DRDY0 bit (reg. B4h, R/W, bit 2) if Drive 0 is selected, or the DRDY1 bit (reg. B5h, R/W, bit 2) if Drive 1 is selected.

5 (R) (DWF) - DRIVE WRITE FAULT: This bit indicates the current write fault status of the selected drive. It is set or reset via the DWF0 bit (reg. B4h, R/W, bit 1) if Drive 0 is selected, or the DWF1 bit (reg. B5h, R/W, bit 1) if Drive 1 is selected.

4 (R) (DSC) - DRIVE SEEK COMPLETE: When set, this bit indicates that the drive heads are settled over a track at the conclusion of a seek operation. It is set or reset via the DSC0 bit (reg. B4h, R/W, bit 0) if Drive 0 is selected, or the DSC1 bit (reg. B5h, R/W, bit 0) if Drive 1 is selected.

3 (R) (DRQ) - DATA REQUEST: When set, this bit indicates that the selected drive is ready for data transfer to/from the host. During a read operation, this bit indicates that a sectors worth of data is ready to be taken by the host. During a write operation, this bit indicates that the buffer is ready to accept a sectors worth of data from the host.

2 (R) (HCDATA) - CORRECTED DATA: This bit is set to indicate that, on the previous read sector transfer, an ECC error was detected and corrected. It is set or reset via the CDATA bit (reg. C1h, R/W, bit 5). This bit is automatically reset when the host writes to the H_CMD register (reg. 1F7h, W).

1 (R) (INDEX) - INDEX: This bit is the reflection the AIC-8375 INDEX input signal. If the DRDY bit in this register is cleared, this bit will be reset to 0.

0 (R) (HERR) - ERROR: This bit is set to indicate that an error occurred during the execution of the current command. It is set or reset via the Error bit in register HCTL_1 (reg. C1h, R/W, bit 0). In addition, this bit will automatically be set if a Host Port Check error (reg. 106h, R, bit 0) or a Host FIFO error (reg. C8h, R, bit 1) has occurred while the Enable Auto Error Set bit (reg. C3h, R/W, bit 5) is set. This bit is automatically reset when the host writes to the H_CMD register (reg. 1F7h, W).

1F7/177h AT HOST COMMAND REGISTER (1F7h, W, H_CMD)

7:0 (W) (H_CMD[7:0]) - AT HOST COMMAND [7:0]: Commands are executed by first loading all other AT Task File registers and then writing into this register while Busy (reg. 1F7h, bit 7) is cleared. The host may abort the pending data transfer to start a new operation by writing to this register when Data Request (AT Host Status reg. 1F7h, R, bit 3) is set. Refer to the ATA specification for a definition of the various command codes.

5.8.2 AT Task File/Control Block Registers

Table 5-3 AT Task File/Control Block Registers

I/O Address	Read	Write
3F6/376h	AT Host Alternate Status Reg.	AT Drive Control Reg.
3F7/377h	AT Host Drive Address Register	not used

3F6/376h AT HOST ALTERNATE STATUS REGISTER (3F6h, R, H_ASTAT)

7:0 (R) (H_ASTAT[7:0]) - AT HOST ALTERNATE STATUS [7:0]: This register contains the same information as the AT Host Status register (reg. 1F7h, R). Reading this register does not clear any pending host interrupt. This register may be read at any time.

3F6/376h AT HOST DEVICE CONTROL REGISTER (3F6h, W, H_DVCTL)

7:4	(W)	Reserved: These bits should all be programmed to zero.
3	(W)	Reserved: This bit should always be programmed to one.
2	(W)	(SRST) - HOST SOFTWARE RESET: When this bit is set, Drive 0 and Drive 1 are held in a reset state. The Host Software Reset Detected bit (reg. C8h, R, bit 3) will be set as a result of this bit being set.
1	(W)	(*IEN) - INTERRUPT ENABLE: When asserted (LOW), this bit enables the AIC-8375 IRQ signal pin to be driven by the device. When inactive (HIGH), the IRQ signal pin output is tri-stated regardless of the presence or absence of a pending interrupt.
0	(W)	Reserved: This bit should allways be programmed to zero.

3F7/377h AT HOST DRIVE ADDRESS REGISTER (3F7h, R, H_DRVADD)

7	(R)	Reserved. This bit is in the high impedance state at the HD7 data pin when this register is read.
6	(R)	(*WG) - INVERTED WRITE GATE: This bit is the compliment of the Write Gate output signal (WG) from the AIC-8375 device.
5:2	(R)	(*HS[3:0]) - *HEAD SELECT 3-0: These bits are the complements of the HS[3:0] bits (reg. 1F6h, R/W, bits 3:0).
1	(R)	(*DS1) - *DRIVE 1 SELECT: When Drive 1 has been selected as a result of the DRV bit (reg. 1F6h, R/W, bit 4) having been set, this bit will be asserted low.
0	(R)	(*DS0) - *DRIVE 0 SELECT: When Drive 0 has been selected as a result of the DRV bit (reg. 1F6h, R/W, bit 4) having been cleared, this bit will be asserted low.

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6.1 Overview Of The Disk Sequencer Map

The AIC-8375 Disk Sequencer Map (DSM) controls the flow of Data between the external ENDEC and the Buffer Memory. The DSM is a programmable memory which stores user specific instructions to control the data flow. It is organized as an array of 31 x 3 byte instructions with each instruction being 3 bytes wide. The DSM can be programmed to perform the three main disk drive functions of Read, Write, and Format. The DSM does this by providing means for: Index detection, Sector detection, Sync Byte detection and synchronization, external Sync detection and synchronization, Read Gate and Write Gate control, skips of embedded servo fields, and other specific functions as described in this section.

The Disk Sequencer Map must be loaded with the appropriate user instructions after the power on process and before it is started (SEQRUN, reg. 73h, R/W, bit 7 = 1). A DSM instruction is executed once every byte time. The number of Read Reference clocks (RRCLKs) per byte time depends on which NRZ mode (single, double, or byte wide) is enabled. The relationship between the byte time and RRCLK is listed in Table 6-1. After each instruction is executed the DSM will either execute the same instruction again, or the next instruction, or branch to a different instruction, or stop.

The Disk Sequencer should not be restarted until a poll of the Sequencer Run Status bit (SEQRUN, reg. 73h, R/W, bit 7) shows a zero.

Table 6-1 Relationship Between Byte Time and Read Reference Clock (RRCLK)

NRZ Mode	Byte Time in # of RRCLK
Single	8
Double	4
Byte-wide	1

Figure 6-1 is an example of a single instruction in the Disk Sequencer Map.

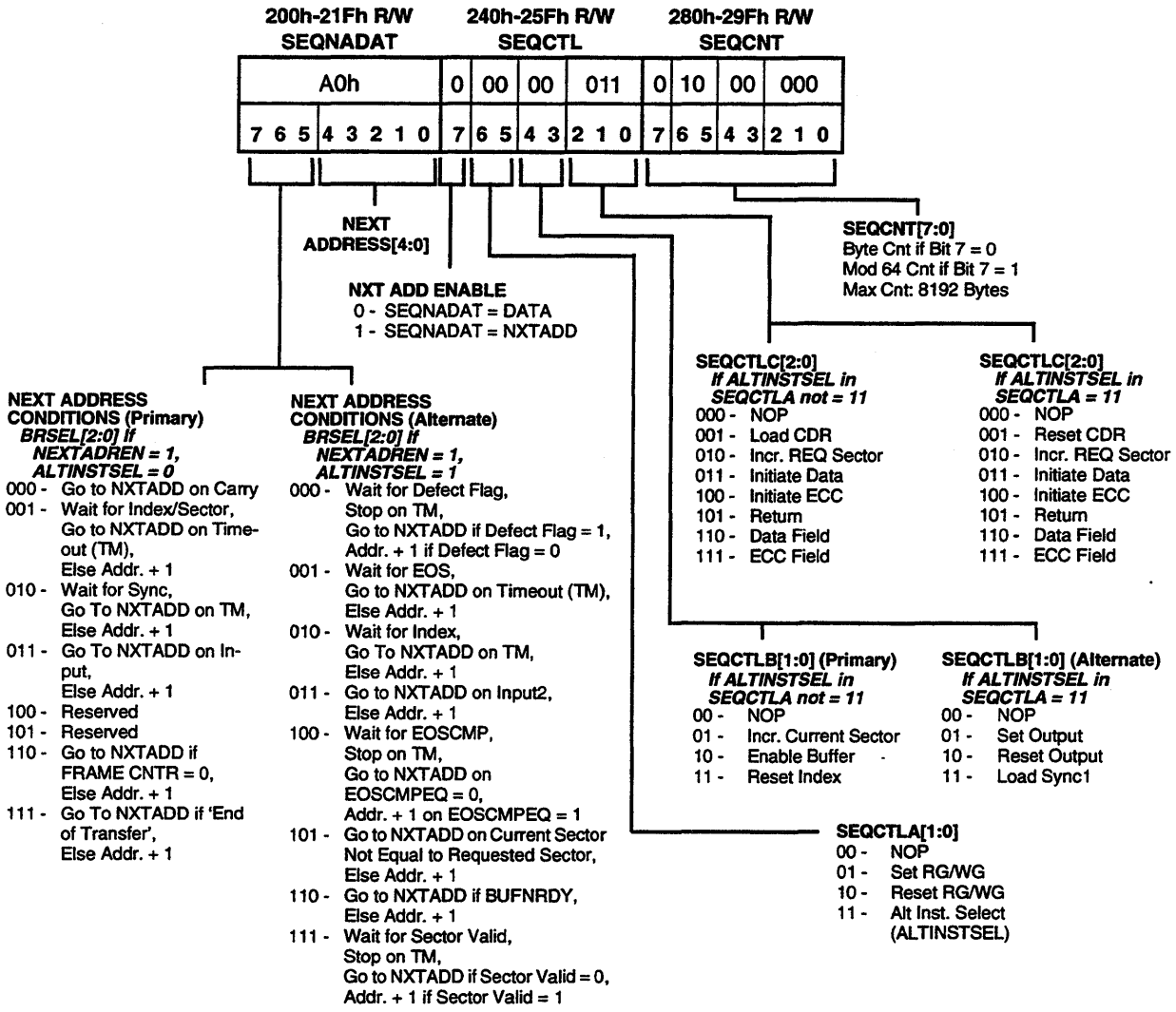

Figure 6-1 Sequencer Map Format

The sections that follow define the usage of each bit within the 3-byte instructions.

6.2 Sequencer Data/Next Address Byte (200h-21Fh, R/W, SEQNADAT)

Each instruction in the Disk Sequencer Map (DSM) may use this first byte as either a Data Field (SEQDATA) or a Next Address Field (SEQNADR) of a branch condition which must also be specified in the same byte. If used as Data Field, bits [7:0] define one byte of Sequencer data. If used as Next Address Field, bits [7:5] define a branch condition and bits [4:0] specify the Next Address to be executed if the branch condition is satisfied. The field type for the current instruction is determined by the state of the NXTADDEN bit of the Sequencer Control Field (second instruction byte, SEQCTL, bit 7). If the NXTADDEN bit is cleared to 0, the 'Data Field' type is selected. If it is set to 1, the 'Next Address field' type will be selected.

6.2.1 Data Field

In total, there are two sources for data which can be written to the disk. These are from:

1. the buffer memory, or
2. the Data field (SEQDATA) which is also referred to as Sequencer Data.

Table 6-2 shows when each of these sources is enabled. Data specified in the 'Data Field' (SEQDATA) can either be written to the disk or compared against the data being read from the disk.

Table 6-2 Disk Sequencer Data Sources

En. Buffer Xfer SEQCTLB (10b)	Suppress Xfer reg. 62h, Bit 6	Data Source
0	X	Sequencer Data Field (SEQDATA)
1	0	Buffer Memory
1	1	Sequencer Data Field (SEQDATA)

The Data field value (SEQDATA) is stored in a holding register during the time the field is being used as the Next Address field. The loading of the holding register occurs on every instruction in which the NXTADDREN decode in the SEQCTL byte is equal to "0". This specifically allows for a Sync-Byte to be loaded into a holding register in preparation for a 'Wait for Sync' branch condition.

When this field is used as a Data field, the default Sequencer operation is to execute the next instruction on Sequencer Count Field Carry (third instruction byte, SEQCNT). The Sequencer will execute the current instruction until the Count Field (SEQCNT) of the current instruction has decremented pass zero (Count Field Carry). On Count Field Carry, the Sequencer will execute the next instruction (PC=PC+1) in the Map.

6.2.2 Next Address Field

The DSM logic uses a program counter (PC) which points to the instruction currently being executed. When the Sequencer is started, the value contained in the Sequencer Address register (reg. 73h, W, bits 4:0) is loaded into the PC. Every byte time thereafter, the PC is loaded with the address of the next instruction to be executed. There are a total of six sequencing operations that determine which Sequencer instruction is to be executed next. These sequencing operations are listed in Table 6-3.

Table 6-3 Sequencer Program Flow Instructions

DSM Operation	Effect on PC	Action
Hold	PC = PC	Execute the same instruction again.
Continue	PC = PC+1	Execute the following instruction.
Jump	PC = Next Addr. Field	Branch to the address contained in the Next Address Field of the current instruction (SEQNADAT[4:0]).
CDR Interrupt	PC = CDR Vector	Vector to the address pointed to by the CDR Vector register (reg. 72h, R/W).
Return	PC = Stored Address	Return to the address stored when a CDR interrupt was taken.
Stop	PC = PC	Sequencer stop condition or when Sequencer jumps to location 1Fh.

The Next Address field is divided into two sub-fields. The three most significant bits [7:5] select one of eight possible primary branch conditions, and when used with SEQCTLA=11b (Alternate Instruction Select) define eight alternate branch conditions. The five least significant bits [4:0] form the address of the instruction to which the sequencer will jump to next. A jump will occur if the specified conditions or condition within the selected branch parameters are satisfied. The following describes the eight primary branch conditions that are implemented for the Sequencer.

NOTE: When using a "Wait For" instruction in the primary or alternate condition fields, always use a non-zero value for the count field value in any instruction pointed to by the "Next Address" instruction following a "Wait For" instruction.

7:5 (R/W) NEXT ADDRESS *Primary* Condition Field

Bit 7 6 5	Description
0 0 0	(NA_CARRY) - NEXT ADDRESS ON CARRY: The Sequencer will execute the current instruction until Count Field Carry occurs. On Count Field Carry, the Sequencer will execute a Jump operation as specified by Next Address (PC=SEQNADR).
0 0 1	(W_SECTOR) - WAIT FOR SECTOR: The Sequencer will execute the current instruction until Count Field Carry occurs or the SECTOR input is asserted. If the Enable Index To Sector Branch bit (ENINDEX, reg. 61h, R/W, bit 4) is set, the INDEX pin is OR'd with SECTOR. If the Sequencer leaves its current state because of a Count Field Carry, then a Branch instruction to Next Address will be executed (PC=SEQNADR) and the Sequencer Wait Time-Out status bit (reg. 66h, R, bit 6) is set. Otherwise, execution will continue with the next instruction (PC=PC+1).
0 1 0	(W_SYNC) - WAIT FOR SYNC: The Sequencer will execute the current instruction until Count Field Carry occurs or the Sync-Byte is detected. If the Sequencer leaves its current state because of a Count Field Carry (Sync Time Out), then a branch instruction to Next Address will be executed (PC=SEQNADR) and the Sequencer Wait Time-Out bit (SEQWAITTO, reg. 66h, R, bit 6) is set. Otherwise, when the Sync-Byte is detected, the Sequencer will execute the next instruction (PC=PC+1). If External Sync is enabled, then the SYNCEN pin will be asserted during this instruction.
0 1 1	(W_INPUT) - WAIT FOR INPUT: The Sequencer will execute the current instruction until Count Field Carry occurs. When the Count Field Carry occurs the status of the INPUT pin is tested. If INPUT=1 the Next Address branch is executed (PC=SEQNADR). If INPUT=0 the Continue is executed (PC=PC+1).
1 0 0	Reserved
1 0 1	Reserved

7:5 (R/W) NEXT ADDRESS *Primary* Condition Field (continued)

Bit 7 6 5	Description
1 1 0	(NA_FRAME) - NEXT ADDRESS IF FRAME COUNTER IS ZERO: The Sequencer will execute the current instruction until Count Field Carry occurs. When Count Field Carry occurs, the Sequencer examines the value in the Frame Counter (reg. 74h, R). If the Frame Counter contains 0, the Sequencer jumps to the Next Address (PC=SEQNADR) and the Frame Counter (reg. 74h, R) is reloaded with the value from the Frame Count register (reg. 74h, W). If the Frame Counter is not 0, then it is decremented and execution continues with next instruction (PC=PC+1).
1 1 1	(NA_ENDXFR) - NEXT ADDRESS IF END OF TRANSFER: The Sequencer will execute the current instruction until Count Field Carry occurs. Upon Count Field Carry, if the contents of the Request Sector Number register (reg. 6Ch-6Dh, R/W) equal the contents of the Stop Sector Number register (reg. 6Eh-6Fh, R/W), the Sequencer will execute a branch instruction to Next Address (PC=SEQNADR). Otherwise, the next instruction in the Map will be executed (PC=PC+1).

The following describes the eight possible alternate branch conditions.

7:5 (R/W) NEXT ADDRESS *Alternate* Condition Field

Bit 7 6 5	Description
0 0 0	(W_DEFECT) - WAIT FOR DEFECT FLAG: The Sequencer will hold on the current instruction until Count Field Carry occurs or the first CDR Split count is loaded into the CDR Counter. On Count Field Carry, the SRVOVRN Status is set and the disk sequencer will halt. If the CDR Counter is loaded before the carry occurs and the Defect Flag (CDR bit 14) is set then a branch to the Next Address Field is executed (PC=SEQNADR). If the Defect Flag is not set a Continue is executed (PC=PC+1). **NOTE:** If the Enhanced DSA bit (reg. 5Dh, R/W, bit 0) is *not* set the Defect Flag signal requires a minimum of 12 byte times following the "Load CDR FIFO" instruction to become effective, i.e., loaded and activated.
0 0 1	(W_EOS) - WAIT FOR EOS: The Sequencer will hold on the current instruction until Count Field Carry occurs or the EOS input (pin 38) signal is asserted. If the Sequencer leaves its current state because of a Count Field Carry then a branch to the Next Address Field is executed (PC=SEQNADR), and the Sequencer Wait Time-Out status bit (reg. 66h, R, bit 6) is set. If the EOS branch is taken a Continue is executed (PC=PC+1).
0 1 0	(W_INDEX) - WAIT FOR INDEX: The Sequencer will hold on the current instruction until the Count Field Carry occurs or the INDEX input is asserted. If the Sequencer leaves its current state because of a Count Field Carry then a branch to the Next Address Field is executed (PC=SEQNADR), and the Sequencer Wait Time-Out status bit (reg. 66h, R, bit 6) is set. If the INDEX branch is taken a Continue is executed (PC=PC+1).

7:5 (R/W) NEXT ADDRESS *Alternate* Condition Field (continued)

Bit 7 6 5	Description
0 1 1	(NA_INPUT2) - NEXT ADDRESS IF INPUT2 ASSERTED: The Sequencer will hold on the current instruction until the Count Field Carry occurs. When the Count Field Carry occurs the INPUT2 (ALE/IN2, pin 104) status is tested. If INPUT2 is false a Continue is executed (PC=PC+1). If INPUT2 is true the Next Address Branch is executed (PC= SEQNADR). INPUT2 is driven by the ALE pin and can only be used as a Sequencer input branch while using a non-multiplexed processor.
1 0 0	(NA_CMPNEQ) - NEXT ADDRESS IF EOS COMPARE NOT EQUAL: The Sequencer will hold on the current instruction until the Count Field Carry occurs or the EOS input is asserted. If the Sequencer leaves its current state because of a Count Field Carry the Disk Sequencer STOPS and EOSTIMEOUT status (reg. 65h, W, bit 1) is set. When EOS is detected the compare of EOSCTR to EOSCMP is tested (EOSCMPEQ status). If EOSC-MPEQ=1 a Continue is executed (PC=PC+1). If EOSCMPEQ=0 the Next Address Branch is executed (PC=SEQNADR).
1 0 1	(NA_CURRSECEQ) - NEXT ADDRESS CURRSEC NOT EQUAL REQSEC: The Sequencer will hold on the current instruction until the Count Field Carry occurs. When the Count Field Carry occurs the CURRSECEQ status is tested (reg. 5Bh, R/W, bit 7). If CURRSECEQ is true a Continue is executed (PC=PC+1). If CURRSECEQ is false the Next Address Branch is executed (PC=SEQNADR).
1 1 0	(NA_BUFNRDY) - NEXT ADDRESS IF BUFFER NOT READY: The Sequencer will hold on the current instruction until the Count Field Carry occurs. When the Count Field Carry occurs the Buffer Not Ready status is tested. If BUFNRDY is false a Continue is executed (PC=PC+1). If BUFNRDY is true the Next Address Branch is executed (PC=SEQNADR).
1 1 1	(W_SECVALID) - WAIT FOR SECTOR VALID: The Sequencer will hold on the current instruction until the Count Field Carry occurs or the SECTOR input is asserted. If the Sequencer leaves its current state because of a Count Field Carry then the Sequencer stops, and the SECTIMEOUT status bit (reg. 65h, R/W, bit 1) is set. If the Sequencer leaves its current state because of SECTOR asserted the BUFNRDY (reg. 62h, R/W, bit 1 if SECRDY=1), the CURRSECEQ (reg. 62h, R/W, bit 2 if SECEQ=1), and/or the CDRVALID/DEFSEC (bit 13 of CDR Split Count) statuses are checked. If CDRVALID=0 the Sequencer STOPS and SRVOVRN status (reg. 5Eh, W, bit 7) is set. If CDRVALID=1 and DEFSEC=1, or BUFNRDY=1, or CURRSECEQ=0 a branch to the Next Address Field is executed (PC=SEQNADR). If CDRVALID=1 and DEFSEC=0 and CURRSECEQ=1 and BUFNRDY=0 a Continue is executed (PC=PC+1). If ENINDEX=1 (reg. 61h, R/W, bit 4), the INDEX pin is OR'd with SECTOR.

4:0 (R/W) NEXT ADDRESS[4:0] Field: These bits form bits 4:0 of the Sequencer Program Counter (PC) when a branch is taken to the Next Address (PC=SEQNADR).

6.3 Sequencer Control Byte (240h-25Fh, R/W, SEQCTL)

This is the second byte of a Sequencer instruction. This byte contains four fields. These are: Next Address Enable (bit 7), SEQCTLA (bits 6:5), SEQCTLB (bits 4:3), and SEQCTLC (bits 2:0). Each of these fields are described in detail below.

7 (R/W) **(NEXTADREN) - NEXT ADDRESS ENABLE:** This bit is used to select whether the SEQNADAT field contains data or Next Address values. If NEXTADREN=0 the Data Field is selected; if NEXTADREN=1 the Next Address Field is selected.

6:5 (R/W) SEQCTLA Field

Bit 6 5	Description
0 0	(NOP) - NO OPERATION: No action is taken. The state of the RG (pin 44) and WG (pin 45) outputs are not affected by this decode. In other words, this decode does not reset any decode in this field (SEQCTLA) that had been previously set.
0 1	(SETRGWG) - SET READ GATE / WRITE GATE: If DWRITE=0 (reg. 60h, R/W, bit 7) this decode asserts the Read Gate output RG at the beginning of the instruction cycle. If DWRITE=1 this decode asserts the Write Gate output WG at the beginning of the instruction cycle. Note that Read Gate and Write Gate are mutually exclusive signals.
1 0	(RSTRGWG) - RESET READ GATE AND WRITE GATE: This decode deasserts both the Write Gate and Read Gate outputs at the beginning of the instruction cycle.
1 1	(ALTINSTSEL) - ALTERNATE INSTRUCTION SELECT: This decode selects between the Alternate Branches and Instructions and the Primary Branches and Instructions. Alternates are selected when this decode is true.

4:3 (R/W) SEQCTLB Field

Bit 4 3	Description
0 0	(NOP) - NO OPERATION: No action is taken by this decode. This decode resets any previously set decode of this field to 'NOP.'
0 1	(INCURSEC/SETOUTPUT) - *If ALTINSTSEL=0* INCREMENT CURRENT SECTOR COUNTER: This decode will increment the CURRSEC Counter. *If ALTINSTSEL=1* SET OUTPUT PIN: This decode will set the OUTPUT Signal, and it stays set until it is reset with the RSTOUTPUT decode.

4:3 (R/W) SEQCTLB Field (continued)

Bit 4 3	Description
1 0	(ENBUFFER/RSTOUTPUT) -

If ALTINSTSEL=0

DATA TRANSFER FROM BUFFER MEMORY: This decode enables the data buffer as the source or destination of the disk data transfers. This bit is overridden by the Suppress Transfer Control bit (SUPXFR, reg. 62h, R/W, bit 6) which when set disables data transfer to/from the Buffer Memory.

If ALTINSTSEL=1

RESET OUTPUT PIN: This decode will reset the OUTPUT Signal. OUTPUT is set with the SETOUTPUT decode.

1 1 (RSTIDX/LOADSYNC1) -

If ALTINSTSEL=0

RESET TWO INDEX TIMER: This decode resets the Two Index Timer.

If ALTINSTSEL=1

LOAD SYNC BYTE 1: This decode will load the SYNCPAT1 Registers from the SEQ-DATA field. NEXTADREN must be 0. This is used to load the most significant byte of the Sync Byte during Internal Fault Tolerant Sync Mode.

2:0 (R/W) SEQCTLC Field

Bit 2 1 0	Description
0 0 0	(NOP) - NO OPERATION: No action is taken by this decode. This decode resets any previously set decode of this field to 'NOP.'
0 0 1	(LOADCDR/RSTCDR) -

If ALTINSTSEL=0

LOAD CDR FIFO: This decode is used to load the Servo Split information into the CDR FIFO or flush old CDR counts from the CDR FIFO and Counter. The CDR FIFO can be loaded with data from either the Buffer Memory or Local MPU.

When ENBUFCER=0 (reg. 63h, R/W, bit 1) and ENHANCEDSA=0 (reg. 5Dh, R, bit 0) this decode must not be used.

When ENBUFCDR=1 and ENHANCEDSA=0 the CDR FIFO will be loaded with data from the Buffer. The number of bytes fetched is specified in the Sequencer Count Field when LOADCDR=1. The Sequencer count is forced to 00h for this instruction. The fetch of information is done in parallel with the succeeding Sequencer instructions. When LOADCDR is executed the CDR FIFO is reset before the load occurs throwing away any split counts in the CDR FIFO and Counter. When specifying the CDR Byte Count, the actual number of bytes required minus 1 must be used.

2:0 (R/W) SEQCTLC Field (continued)

Bit 2 1 0	Description
	When ENHANCEDSA=1 and ENBUFCDR=1 issuing this decode will not cause a fetch of bytes from the Buffer Memory. It will flush all of the CDR Split counts for the current Sector by flushing all counts up to and including the count with the LASTSPLIT bit set (CDR Split Count bit 13). The Sequencer count is forced to 00h for this instruction. This instruction cannot be issued in two consecutive word and expect two flushes. Flushes can be consecutive only after the CDR is valid. After LOADCDR is issued the CDR is not valid until the flush is complete. *If ALTINSTSEL=1* RESET CDR FIFO: When this decode is issued the CDR FIFO and CDR Counter are reset.
0 1 0	(INCREQSEC) - INCREMENT REQUEST SECTOR NUMBER: This decode is used to increment the Request Sector Number Register by one. If the REQSEC Register equals the Wrap Sector Number Register (reg. 68h/69h, R/W) the REQSEC Register will wrap to the value specified in the Wrap To Sector Number Register (reg. 6Ah/6Bh, R/W). If this decode is used in the same instruction as a "Next Address on End of Transfer" the increment will take place after the compare.
0 1 1	(INITDATA) - INITIALIZE DATA FIELD: This decode initializes and starts ECC logic after the data Sync byte is detected or written. The Sync-Byte is not included in the ECC calculation. This decode must be used in a 'Wait for Sync' instruction. This decode should also be set when writing the first data Sync byte and not for the subsequent data Sync bytes used in Servo splits. When writing a 2-byte fault tolerant byte sync, this decode must be executed coincident with the second of the two sync bytes. The INIT_LFSR bit (reg. 9Bh, R/W, bit 0) is set whenever this decode is executed if ENSEED=0.
1 0 0	(INITECC) - INITIALIZE DATA ECC: If ENSEED=1 this decode initializes the Data ECC and triggers a four byte Seed write to the EDAC. If ENSEED=0 this decode is not used. This operation should be executed 4 byte times before the sync byte is written. The INIT_LFSR bit (reg. 9Bh, R/W, bit 0) is set whenever this decode is executed if ENSEED=1.
1 0 1	(RETURN) - RETURN FROM CDR VECTOR: This decode returns the program address counter to the address saved during a CDR Interrupt Vector. The ECC circuitry is automatically enabled when the RETURN is executed.
1 1 0	(DATAFIELD) - DATA FIELD: This decode is set when the Data Field is being transferred.
1 1 1	(ECCFIELD) - ECC FIELD: This decode is set when the Data ECC field is being transferred to/from the disk if the ECC circuitry is to be used.

6.4 Sequencer Count Byte (280h-29Fh, R/W, SEQCNT)

This is the third byte of a DSM instruction. This byte can function as a fetch count, or as a Sequencer Count byte. If used as a fetch count the Sequencer Count is forced to zero in order to execute the instruction in one byte time.

If the 'Load CDR FIFO' decode (SEQCTLC bits 2:0 = '011' with ALTINSTEL not ='11') is enabled, the Enable CDR from Buffer bit (reg. 63h, R/W, bit 1) is set to 1, and the Enable EDSA Mode bit is cleared (reg. 5Dh, R/W, bit 0), this byte represents the number of CDR bytes (minus 1) to be fetched from the buffer memory and loaded into the CDR FIFO. In this mode, the Sequencer Count is forced to zero.

If the 'Load CDR FIFO' decode is not set, this byte represents, in byte times, the number of times plus one that the current instruction is to be executed. Of course, the execution of the current instruction can be interrupted for a number of reasons. Every byte time the Sequencer Count is decremented. The DSM will execute a new instruction upon a Count Field Carry which occurs if the Sequencer Count counts down from zero. The following describes how the bits in this byte are used.

7 (R/W) **(MODCNTEN) - MODULO 64 COUNT ENABLE:** When this bit is set to 1, the Sequencer Count is Modulo 64. For every 64 bytes, the Sequencer Count[6:0] is decremented by one. When this bit is cleared to 0, the Sequence Count[6:0] is a normal 7-bit down counter and is decremented on every byte time.

6:0 (R/W) **(SEQCNT[6:0]) - SEQUENCER COUNT[6:0]:** This field determines the value of the Sequencer counter. These bits are loaded into the Sequencer Counter at the start of the Sequencer instruction. The counter will decrement by one for every 1 or 64 bytes that are transferred, depending on the state of the MODULO 64 COUNT ENABLE bit. When the counter generates a Carry, a new instruction is accessed from the Sequencer Map.

NOTE: In either normal mode or Mod 64 mode, the counter should be loaded with the desired count minus one.

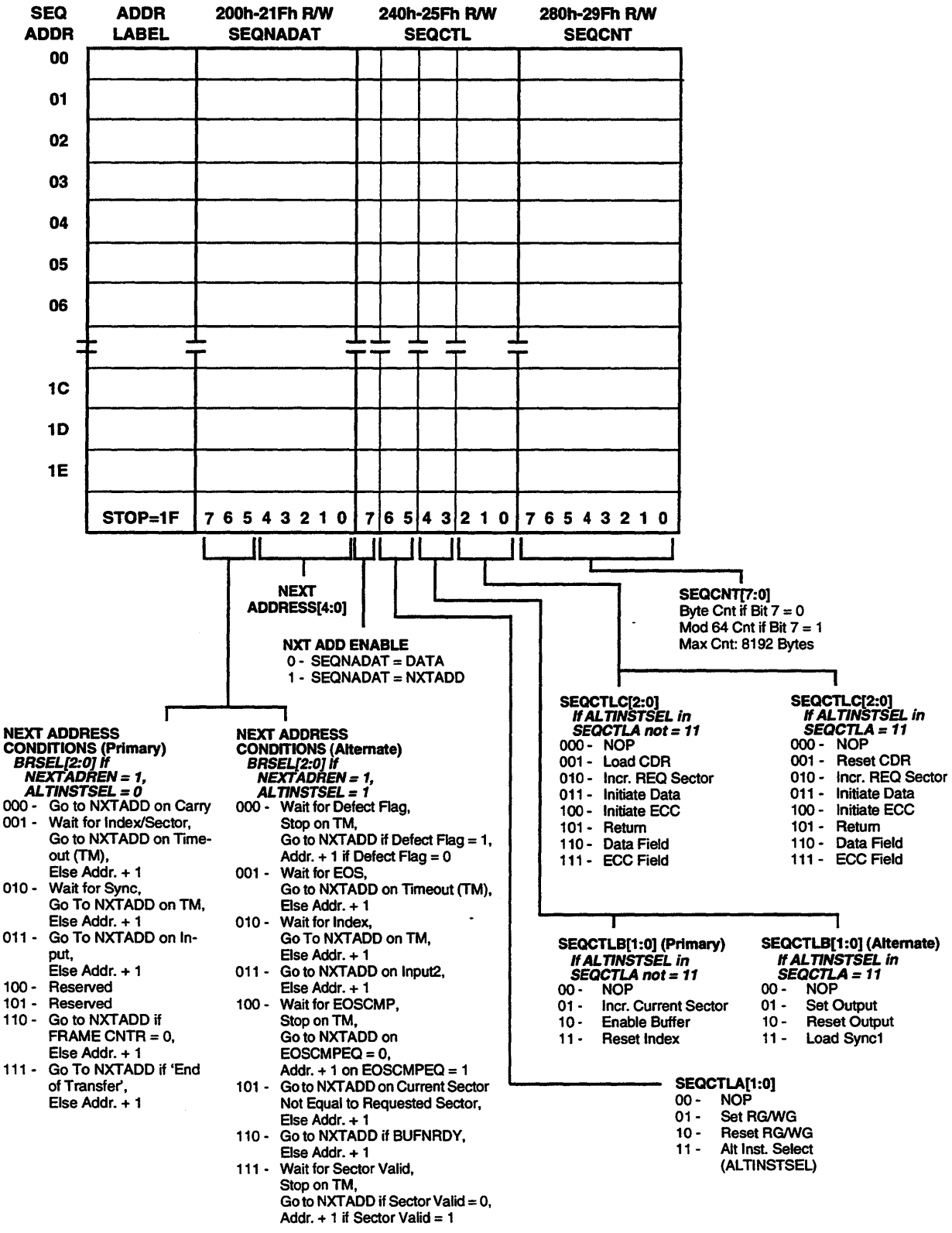

Figure 6-2 Blank Sequencer Map

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7.1 Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Power Supply Voltage	7 Volts
Voltage on any pin	Gnd – 0.5 to Vdd + 0.5 Volts

7.2 Operating Conditions

Ambient Temperature Under Bias	0°C to 70°C
Supply Voltage (Vdd)	4.50 to 5.50 Volts
Power Dissapation	0.5 Watts

7.3 DC Characteristics

(Operating Conditions: V_{dd} = 5.0V ± 10%, 0°C < T <70°C)

SYMBOL	PARAMETER	VALUES MIN	TYP	MAX	UNITS	CONDITIONS/NOTES
I_{DDQ}	Quiescent Current		0.2	3	mA	Vdd = 5.50V All pins @ Vdd or Vss
I_{DD}	Operating Current		80	100	mA	Vdd = 5.50V w/ R/W cmd RRCLK = 15 MHz, byte-wide BUFCLK = 50 MHz
V_{IH}	Input High Voltage	2.0		Vdd+0.5	V	
V_{IL}	Input Low Voltage	–0.5		0.8	V	
V_{TH}	Input Hysteresis	300			mV	(Refered to in Section 2)
V_{OL1}	Output Low Voltage$_1$			0.4	V	IOL = 4 mA
V_{OL2}	Output Low Voltage$_2$			0.4	V	IOL = 8 mA
V_{OL3}	Output Low Voltage$_3$			0.4	V	IOL = 12 mA
V_{OL4}	Output Low Voltage$_4$			0.4	V	IOL = 24 mA
V_{OH}	Output High Voltage	2.4			V	IOH = -1 mA
I_{IL}	Input Leakage Current	–10		10	µA	0 < Vil < Vdd
I_{OZ}	High Z Output Leakage Current	–10		10	µA	0 < ViO < Vdd
C_{IN}	Input Capacitance			10	pF	
C_{OUT}	Output Capacitance			10	pF	
R_{PU}	Internal Pull-up Resistance	50		300	K Ohm	(Refered to in Section 2)
I_{SLP1}	Sleep Mode Current 1		15		mA	BUFCLK = Vdd RRCLK = Vdd All I/O pins pulled to their inactive state by internal or external pullup/-pulldown resistors Host Block powered off Buffer Bolck powered off Disk Block powered off
I_{SLP2}	Sleep Mode Current 2		35		mA	I_{SLP1} conditions with BUFCLK = 50 MHz RRCLK = 15 MHz, byte-wide DRAM refresh off

NOTE: See Section 2 of this manual for output pin current types (4, 8, 12, or 24 mA).

7.3 DC Characteristics (Cont.)

SYMBOL	PARAMETER	VALUES MIN	TYP	MAX	UNITS	CONDITIONS/NOTES
I_{SLP3}	Sleep Mode Current 3		35		mA	I_{SLP2} conditions with Microprocessor interface active.
I_{PDN1}	Power-Down Current 1		35		mA	Host Block powered off Buffer Bolck powered off Disk Block powered off DRAM refresh off BUFCLK = 50 MHz RRCLK = 15 MHz, byte-wide Microprocessor and ATA interfaces active.
I_{PDN2}	Power-Down Current 2		35		mA	I_{PDN1} conditions with DRAM refresh on.
I_{PDN3}	Power-Down Current 3		40		mA	I_{PDN1} conditions with RRCLK = Vdd

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8.1 General Timing

The timing values in this section are derived from timing simulations.

8.1.1 AC Input/Output Timing Parameters

Symbol	Parameter	Values Min	Typ	Max	Units	Notes
TF	Signal Fall Time			5	ns	Cap loading @ 20pF
TR	Signal Rise Time			5	ns	

8.1.2 AC Input/Output Timing

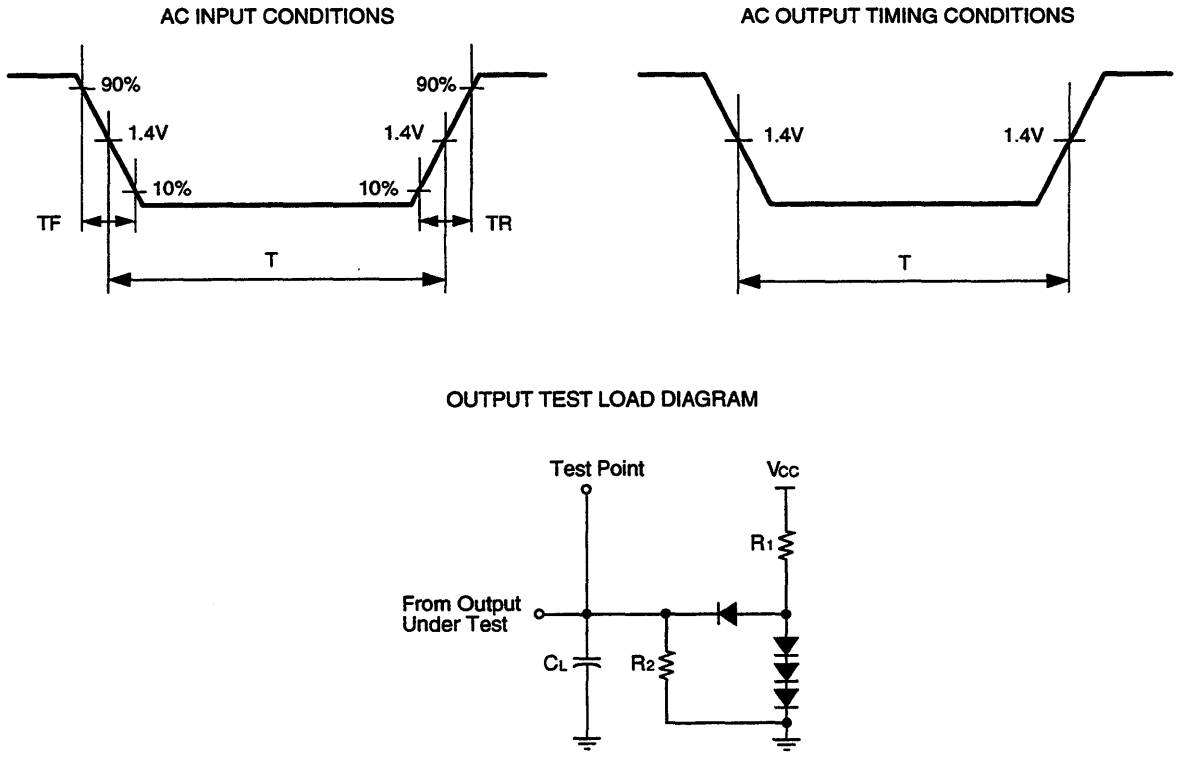


Figure 8-1 AC Input/Output Timing

8.2 Microprocessor Interface Timing

8.2.1 Microprocessor Interface Timing Parameters

Symbol	Parameter	Values Min	Typ	Max	Units	Notes
TWRL	*WR Pulse Width	30			ns	Note 1
TRDL	*RD Pulse Width	35			ns	Note 1
TALE	ALE Pulse Width or AS Pulse Width	15			ns	
TAS	AD[7:0] Address Valid to ALE or AS Negated Setup Time	5			ns	
TAH	AD[7:0] Address Hold Time from ALE or AS Negated	7			ns	
TDWS	AD[7:0] Write Data Setup to *WR Negated	20			ns	
TDES	AD[7:0] Write Data Setup to E Negated	20			ns	
TDEH	AD[7:0] Write Data Hold Time from E Negated	15			ns	
TDWH	AD[7:0] Write Data Hold Time from *WR Negated	15			ns	
TCSH	CS or BS Hold Time from *WR/*RD Negated	5			ns	
TRDV	*RD or E Asserted to AD[7:0] Read Data Valid Time			17	ns	
TRDH	AD[7:0] RD Data Hold Time from *RD Negated	0		25	ns	
TREH	AD[7:0] RD Data Hold Time from E Negated	0		25	ns	
TRTS	*RD or E Asserted to AD[7:0] Active Time	0			ns	Note 2
TRWS	R/*W to E Setup Time	0			ns	
TAOUT	AD[7:0] to MPA[7:0] delay time when ALE=1			15	ns	
TRWH	R/*W Hold Time from E Negated	5			ns	
TCES	CS or BS Asserted to E Asserted Setup Time	5			ns	
TCEH	CS Hold Time from E Negated	5			ns	
TAES	MPA[9:0] Address Valid to E Setup Time	15			ns	
TAAR	AD[7:0] Address Valid and ALE or AS Asserted to AD[7:0] Read Data Valid			45	ns	Note 3
TAVRL	AD[7:0] Address Valid and ALE Asserted to *RD Asserted	15			ns	
TAVWL	AD[7:0] Address Valid and ALE Asserted to *WR Asserted	15			ns	
TCBS	CS or BS Setup to Assertion of *RD or *WR	5			ns	
TWHLH	*WR negated to ALE enabled	35			ns	
TRHLH	*RD negated to ALE enabled	35			ns	

Table continued on next page.

8.2.1 Microprocessor Interface Timing Parameters (Cont.)

Symbol	Parameter	Values Min	Typ	Max	Units	Notes
TMVWL	Non-multiplexed Address Valid to *WR Asserted Setup Time	10			ns	
TMVRL	Non-multiplexed Address Valid to *RD Asserted Setup Time	10			ns	
TWHAX	Non-multiplexed Address to *WR Negated Hold Time.	5			ns	
TRHAX	Non-multiplexed Address to *RD Negated Hold Time	6			ns	
TNAR	Non-multiplexed Address valid to AD[7:0] Read Data Valid			45	ns	Note 3
TRHQZ	*RD Negated to AD[7:0] drivers off.			25	ns	
TAVEH	MPA[9:8], AD[7:0] Address Valid to Assertion of E Setup Time	15			ns	
TELQZ	E Negated to AD[7:0] Drivers Off			25	ns	
TELAX	E Negated to Next MPA[7:0] Address Valid	0			ns	
TRDYV	AD[7:0] Read Data Valid to Ready Asserted Time	0			ns	
TRDYC	BS or CS Asserted to Ready Negated Time			20	ns	
TRDYW	*WR or E Negated to Ready Negated			17	ns	
TRDYN	CS Negated to Ready Asserted	0			ns	

NOTES: Timing responses are measured with 50 pF loading on microprocessor pins.

1. Minimum pulse width determined by components in R/W path and setup and hold times given here.
2. If TAAR time is met, TRDA is when Read Data is valid.
3. For register access only, does not apply to Sequencer Map or Buffer RAM accesses.

8.2.2 Intel Multiplexed Mode

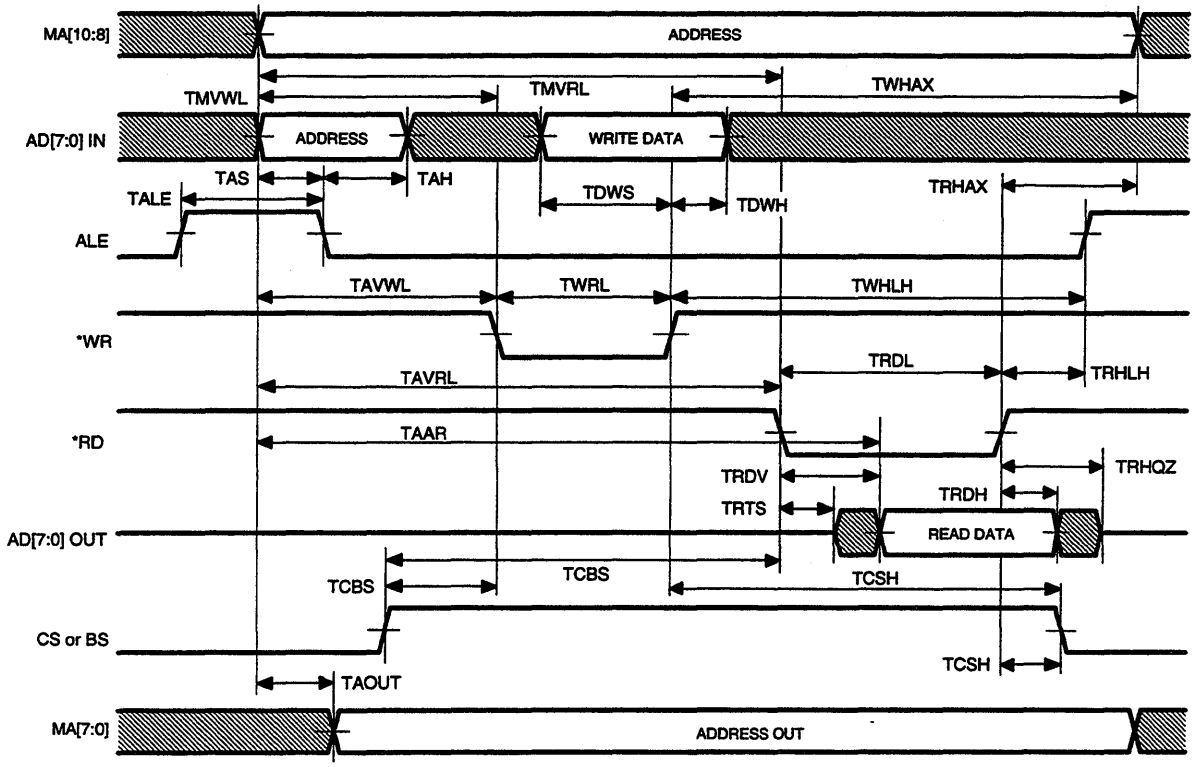


Figure 8-2 Intel Multiplexed Mode

8.2.3 Intel Non-Multiplexed Mode

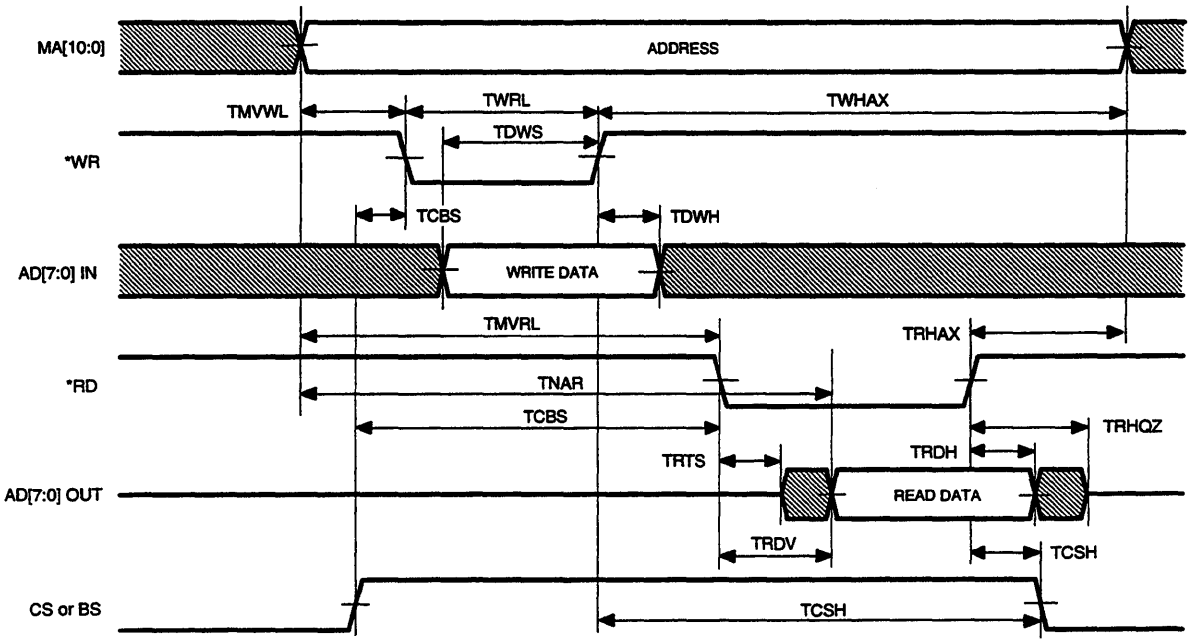


Figure 8-3 Intel Non-Multiplexed Mode

8.2.4 Motorola Multiplexed Mode

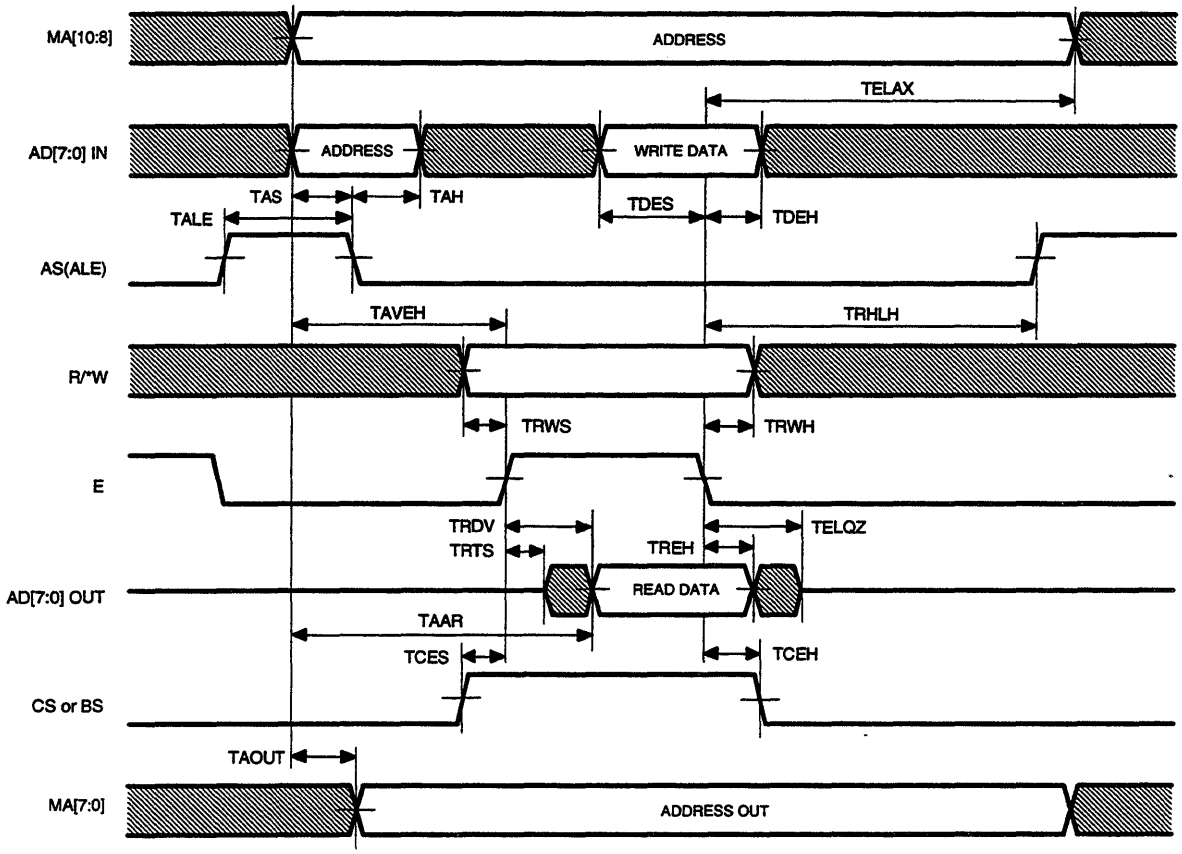


Figure 8-4 Motorola Multiplexed Mode

8.2.5 Motorola Non-Multiplexed Mode

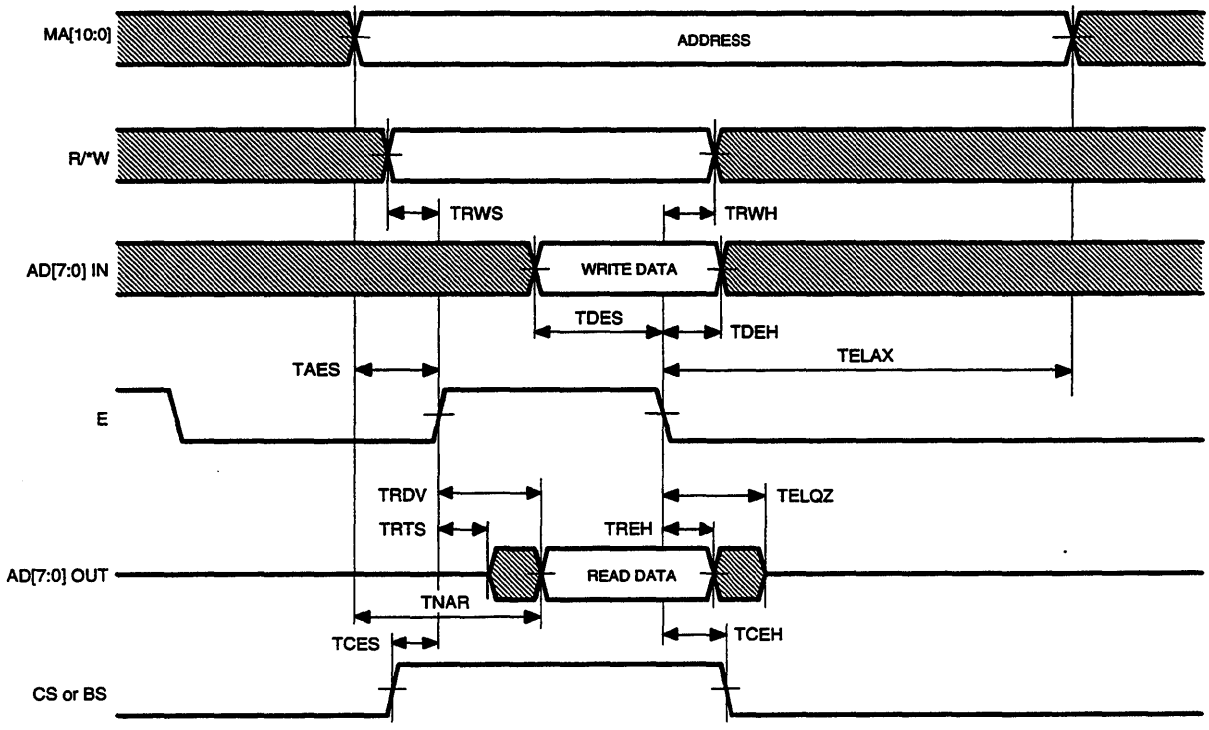


Figure 8-5 Motorola Non-Multiplexed Mode

8.2.6 Microprocessor Ready Line Operation

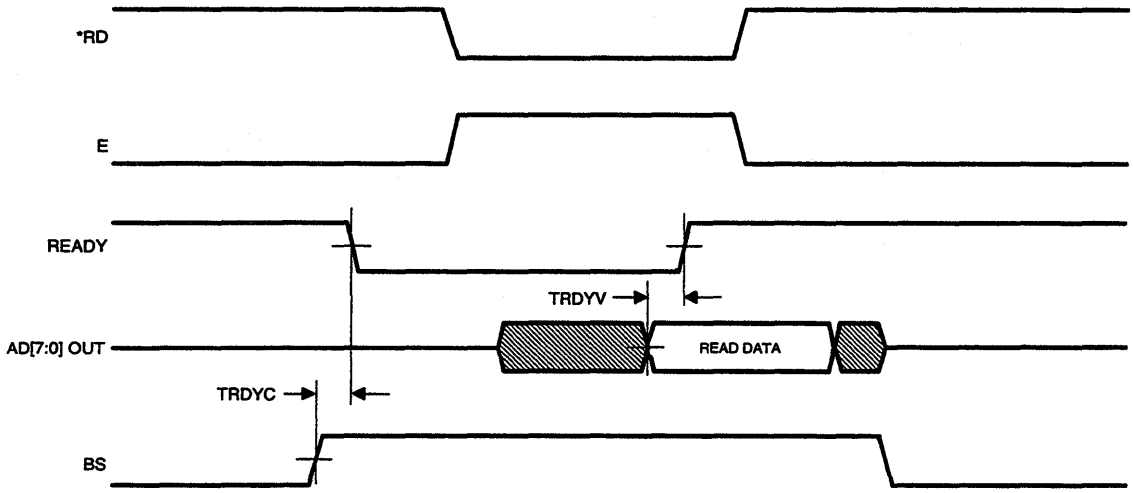


Figure 8-6 Microprocessor Ready Timing (Buffer RAM Read Cycle)

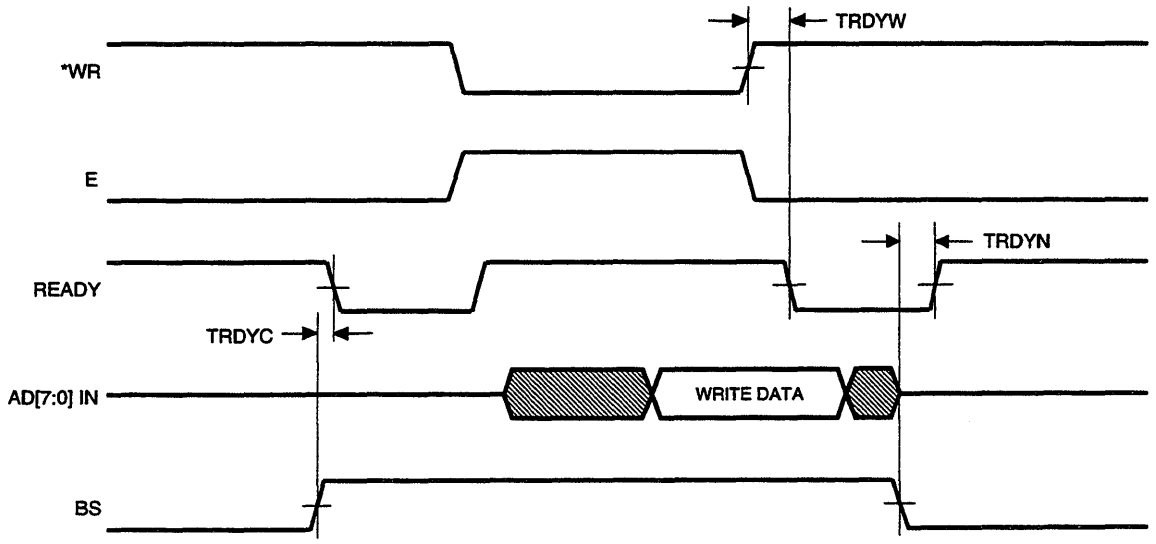
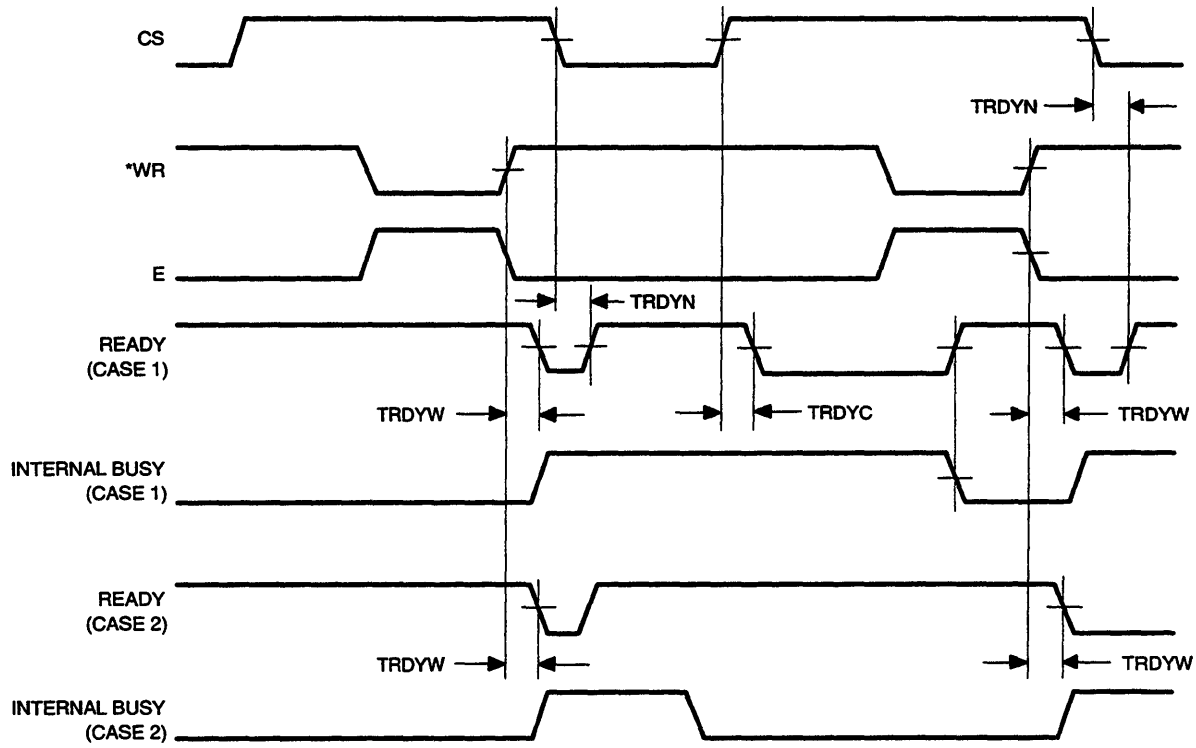


Figure 8-7 Microprocessor Ready Timing (Buffer RAM Write Cycle)



The following cases are shown:

Case 1: Subsequent write of a type 1 register is occurring while the previous write has not internally been completed. (Internal Busy still set at time of second write operation.) Ready is negated at second CS in order to prevent negation of second *WR until data of first write operation has been written into its destination.

Case 2: Subsequent write of a type 1 register occurs after the previous write operation has been completed.

Figure 8-8 Microprocessor Ready Timing

(Synchronous Type 1 Register or Buffer Memory Write Cycle)

8.3 Buffer Interface Timing

8.3.1 SRAM Timing Parameters

Symbol	Parameter	Values Min	Typ	Max	Units	Notes
TCYC	SRAM Cycle Time		2T, 3T, 4T, 5T		ns	Note 1
T	BUFCLK Period	20			ns	
TBH	BUFCLK High Time	8			ns	
TBL	BUFCLK Low Time	8			ns	
Timing Requirements for the SRAM						
TAA	Access Time from Address Valid			TCYC-15	ns	
TDAH	Data Hold from Address Change	0			ns	
TDOEH	Data Hold from *MOE, *MCE1, *MCE2 Negated	3			ns	
TOE	*MOE Asserted to BD[15:0] Read Data Valid			TCYC-TBH-15	ns	
	*MCE1, *MCE2 Asserted to Respective Data Bus (Upper or Lower Byte) Read Data Valid			TCYC-TBH-15	ns	
Timing Responses of the AIC-8375						
TCMOV	BUFCLK to *MOE, *MCE1, *MCE2 Asserted	5		24	ns	Note 2
TCMON	BUFCLK to *MOE, *MCE1, *MCE2 Negated	5		20	ns	Note 2
TAS	Address Setup to *WE0 Asserted	TBH-9			ns	2T,3T,4T,5T
TWP	*WE Asserted Pulse Width	TCYC-T-5			ns	
TAH	Address Hold from *WE Negated	TBL-5			ns	
TAW	Address Valid to *WE Negated	TCYC-TBL-15			ns	
TQS	BD[15:0] Data Setup to *WE Negated (2T)	T-10			ns	2T
	(3T)	T+TBH-10			ns	3T
	(4T)	2T-10			ns	4T
	(5T)	2T+TBH-10			ns	5T
TQH	Data Hold from *WE Negated	TBL-8			ns	3T,4T - Note 2
TDD	Data Delay from *MCE1 or *MCE2 (3T)			TBL+5	ns	3T - Note 2
	(4T)			T+7	ns	4T - Note 2
TCAV	BUFCLK to Address Valid	3		20	ns	
TCAI	BUFCLK to Address Invalid	3		20	ns	
TCWA	BUFCLK to *WE0 Asserted	3		17	ns	Note 2
TCWN	BUFCLK to *WE Negated	3		17	ns	Note 2

NOTES:

1. Programmable via Reg. 100h bits 6 and 7.
2. For both Single and Dual MCE Modes (MCE1 and MCE2). Simulations indicate that the difference between Single and Dual MCE Modes is very small. The values in the table cover both modes.

8.3.2 DRAM Timing Parameters

Symbol	Parameter	Zero-Wait State Values			One-Wait State Values			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
T	BUFCLK Period	20			20			ns	
TBH	BUFCLK High Time	8			8			ns	
TBL	BUFCLK Low Time	8			8			ns	
TCYCD1	One Byte Access Cycle Time		6T			8T		ns	
TCYCD8	Eight Byte Access Cycle Time		20T			29T		ns	
TRC	Random Read/Write Cycle Time		6T			8T		ns	
TPC	Page Mode Read/Write Cycle		2T			3T		ns	
Timing Requirements for the DRAM									
TOFF	BD[7-0] Read Data Hold from *CAS Negated	0			0			ns	
TAA	Access Time From Column Address Valid			2T+TBL-20			3T+TBL-20	ns	
TRAC	Access Time from *RAS Asserted			3T+TBL-10			4T+TBL-10	ns	
TCAC	Access Time from *CAS Asserted			T+TBL-10			2T+TBL-10	ns	
TCPA	Access Time from *CAS Pre-charge			2T-8			3T-8	ns	
Timing Response of the AIC-8375									
TRAS	*RAS Pulse Width (for Single Byte Access)	3T+TBL-10			4T+TBL-10			ns	
TRCD	*RAS to *CAS Delay Time	2T-10			2T-10			ns	
TCAS	*CAS Pulse Width	T+TBL-10			2T+TBL-10			ns	
TASR	Row Address to Assertion of *RAS Setup Time	T+TBH-20			T+TBH-20			ns	
TRAH	Row Address Hold Time from *RAS Asserted	T-5			T-5			ns	
TASC	Column Address to *CAS Asserted Setup Time	T-15			T-15			ns	
TCAH	Column Address Hold Time from *CAS	T			2T			ns	
TCP	Page Mode *CAS Precharge Time	TBH			TBH			ns	
TDSW	BD[7-0] Write Data Setup Time to *CAS Asserted	TBH-7			TBH-7			ns	
TDHW	BD[7-0] Wr Data Hold Time from *CAS Asserted	T+TBL-10			2T+TBL-10			ns	

Table continued on next page.

8.3.2 DRAM Timing Parameters (Cont.)

Symbol	Parameter	Zero-Wait State Values			One-Wait State Values			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
TCSR	*CAS to *RAS Setup Time (Refresh)	T-10			T-10			ns	
TBRAV	BUFCLK↑ to Row Address (BA[10-0]) Valid			25			25	ns	Note 1
TBCAV	BUFCLK↓ to Col. Address (BA[10:0]) Valid			25			25	ns	Note 1
TBCAX	BUFCLK↓ to Col. Address (BA[10:0]) Invalid	5			5			ns	Note 1
TBRA	BUFCLK↓ to *RAS Asserted	3		20	3		20	ns	Note 1
TBRN	BUFCLK↑ to *RAS Negated	3		20	3		20	ns	Note 1
TBCA	BUFCLK↓ to *CAS Asserted	3		20	3		20	ns	Note 1
TBCN	BUFCLK↑ to *CAS Negated	3		20	3		20	ns	Note 1
TBWA	BUFCLK↑ to *WE Asserted	3		20	3		20	ns	Note 1
TBWN	BUFCLK↑ to *WE Negated	3		20	3		20	ns	Note 1
TRP	*RAS Precharge Time	2T+TBH-5			3T+TBH-5			ns	
TCRP	*CAS Negated to Next *RAS Asserted	2T+TBH-10			3T+TBH-10			ns	
TRSH	*CAS Asserted to *RAS Negated Hold Time	T+TBH-10			2T+TBH-10			ns	
TCSH	*RAS Asserted to *CAS Negated Hold Time	3T+TBL-10			4T+TBL-10			ns	
TRPC	*RAS Negated to Next *CAS Asserted	T+TBH-10			2T+TBH-10			ns	
TWCS	*WE Asserted to *CAS Asserted Setup Time	T+TBH-10			T+TBH-10			ns	
TWCH	*WE Hold from *CAS Asserted	2T+TBL-10			3T+TBL-10			ns	
TCHR	*RAS Assertion to *CAS Negation (Refresh)	3T+TBL-10			4T+TBL-10			ns	
TRHCP	*RAS Hold from *CAS Pre-charge	2T-5			3T-5			ns	

NOTE:

1. This parameter is included for reference purposes only. Use other parameters for design calculations.

8.3.3 SRAM Timing (Read, 2T Access)

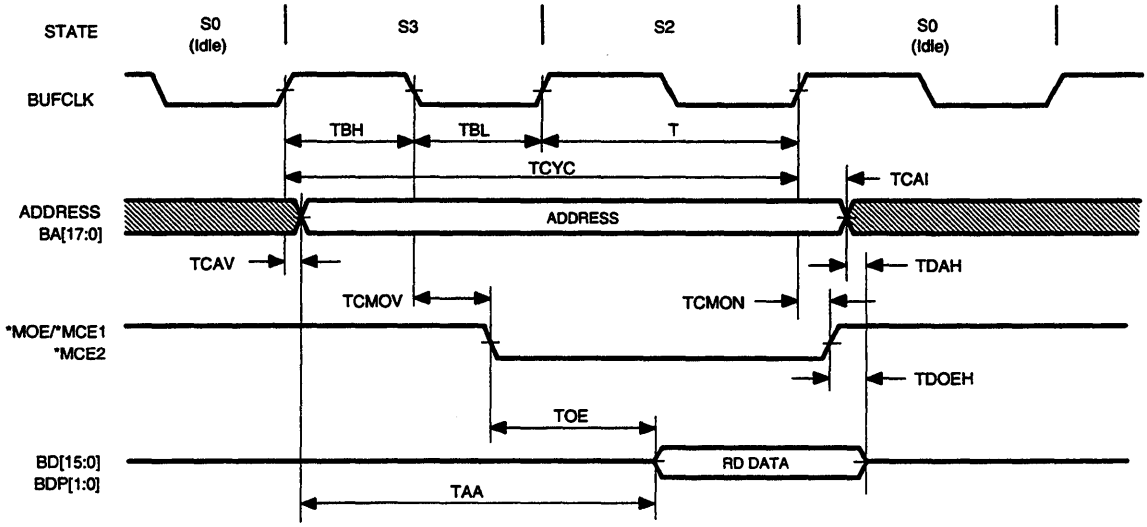


Figure 8-9 SRAM Timing (Read, 2T Access)

8.3.4 SRAM Timing (Read, 3T Access)

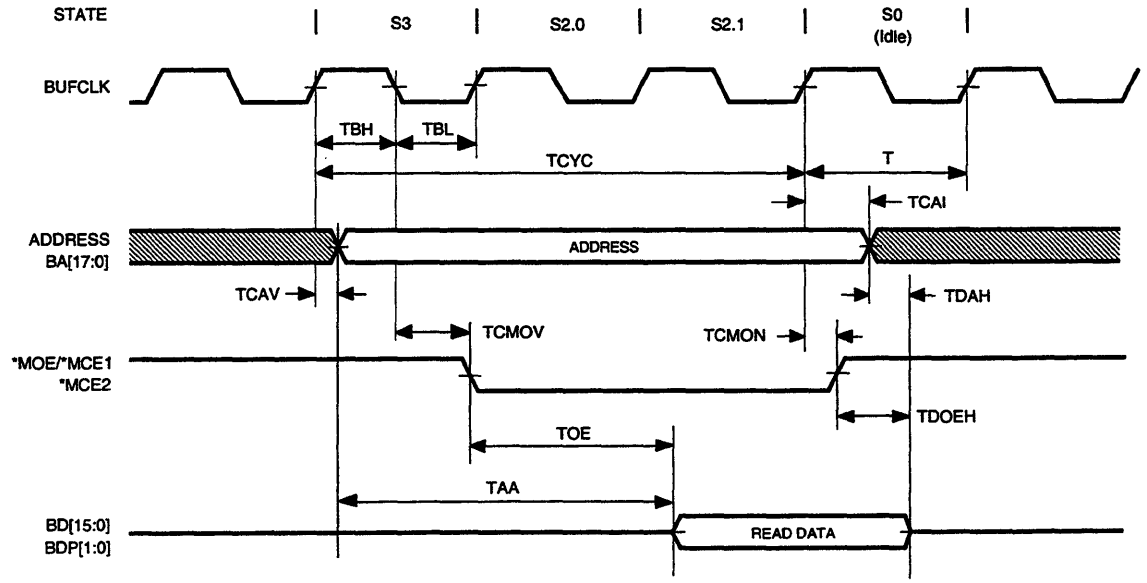


Figure 8-10 SRAM Timing (Read, 3T Access)

8.3.5 SRAM Timing (Read, 4T Access)

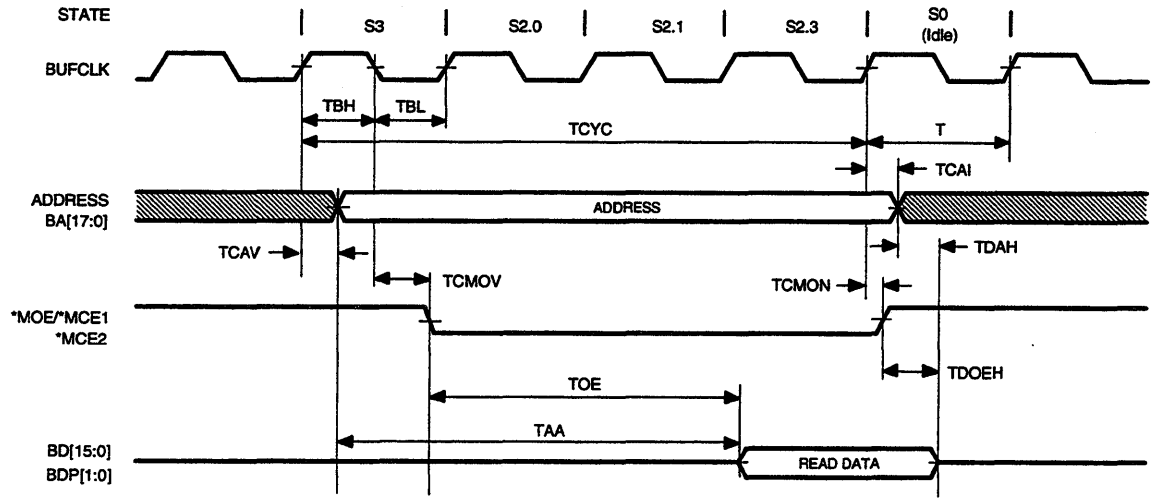


Figure 8-11 SRAM Timing (Read, 4T Access)

8.3.6 SRAM Timing (Read, 5T Access)

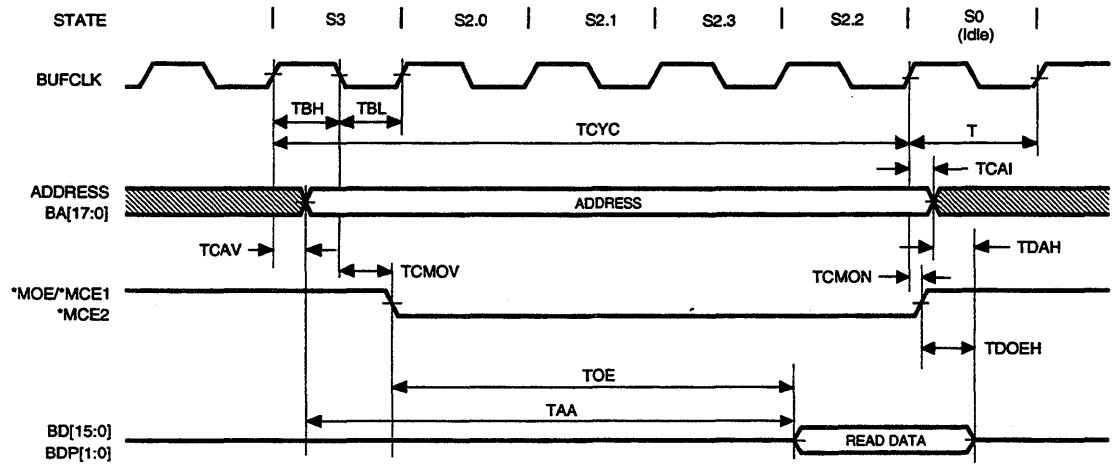


Figure 8-12 SRAM Timing (Read, 5T Access)

8.3.7 SRAM Timing (Write, 2T Access)

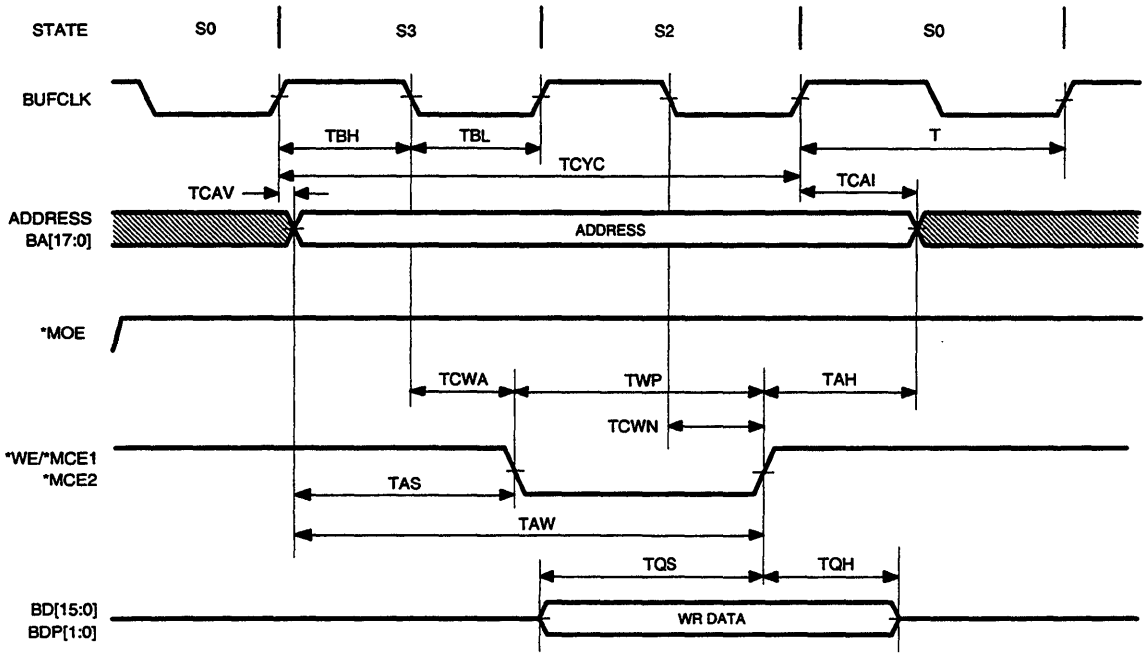


Figure 8-13 SRAM Timing (Write, 2T Access)

8.3.8 SRAM Timing (Write, 3T Access)

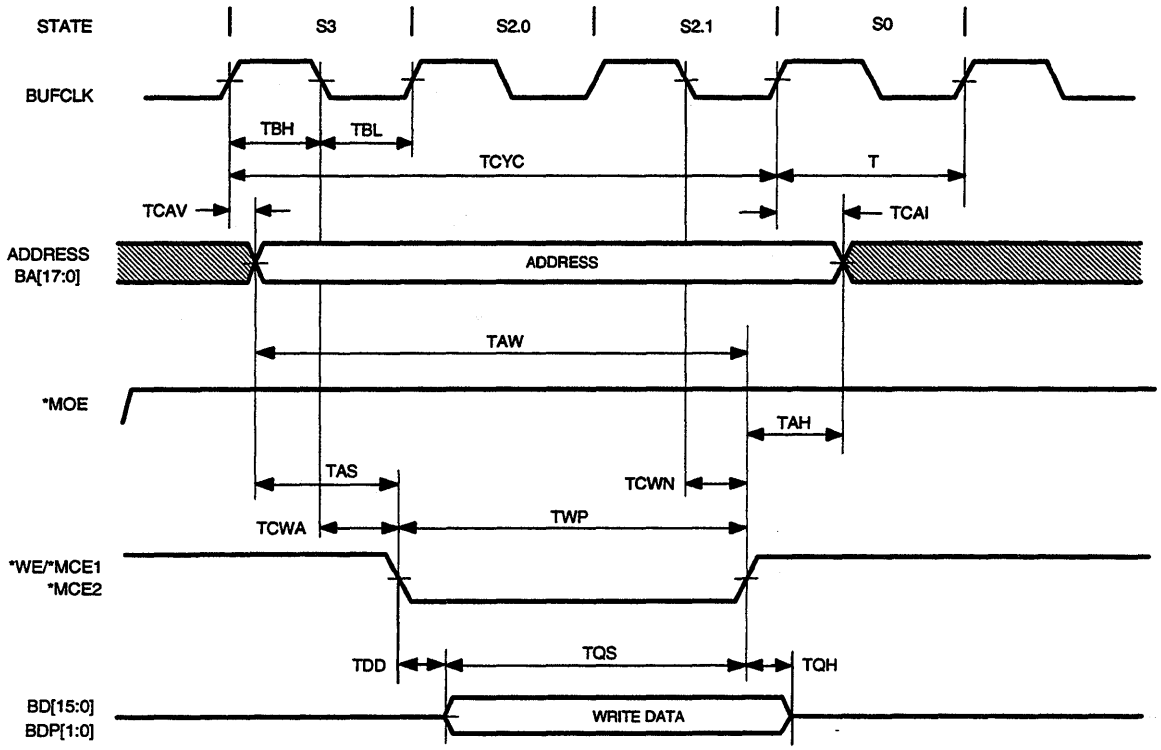


Figure 8-14 SRAM Timing (Write, 3T Access)

8.3.9 SRAM Timing (Write, 4T Access)

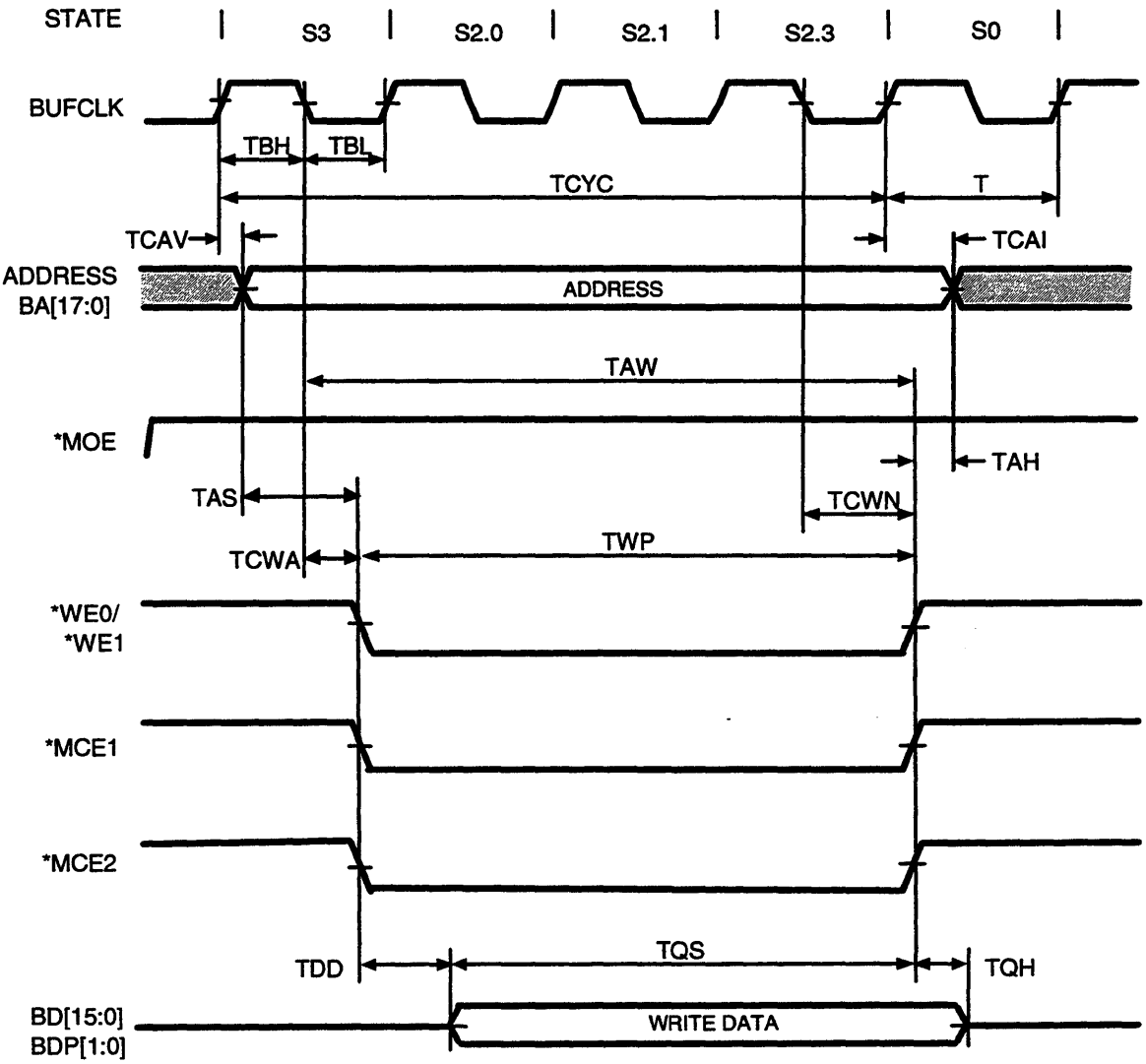


Figure 8-15 SRAM Timing (Write, 4T Access)

8.3.10 SRAM Timing (Write, 5T Access)

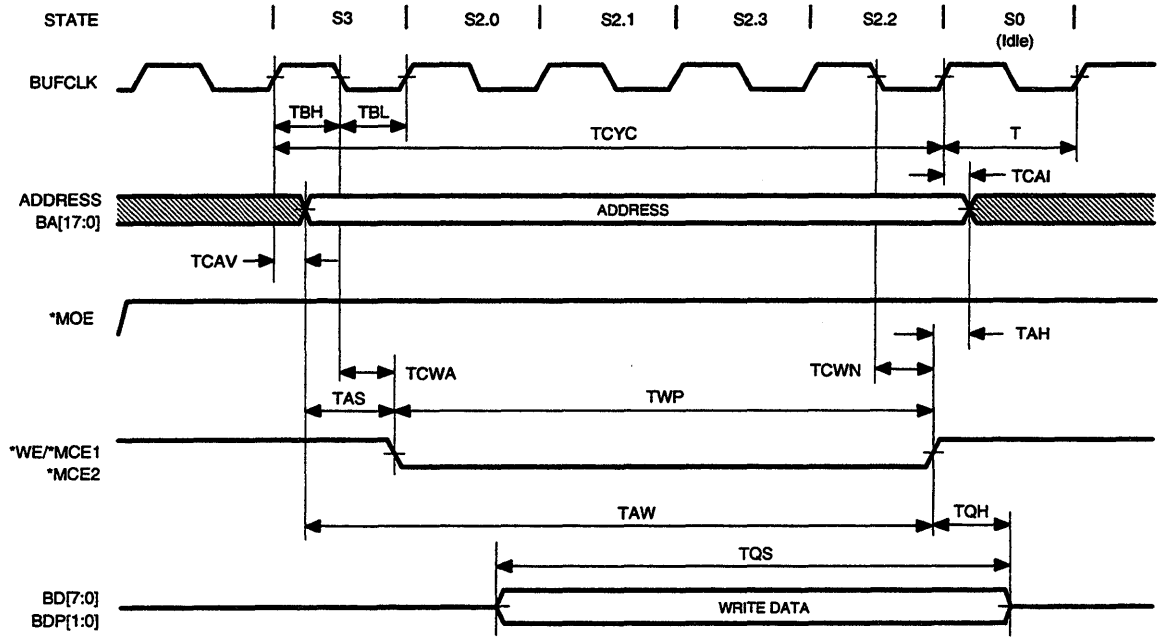


Figure 8-16 SRAM Timing (Write, 5T Access)

8.3.11 DRAM Timing (No Wait State, One Byte Read)

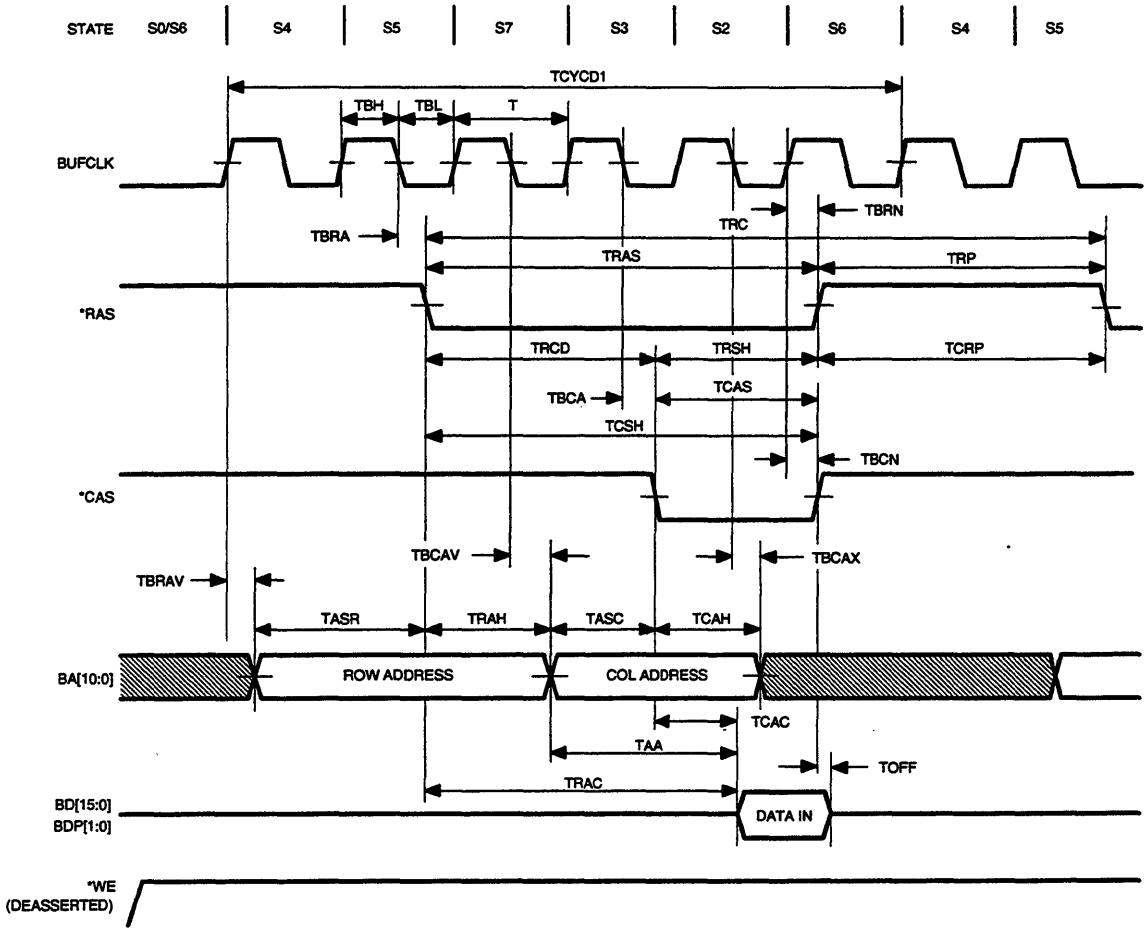


Figure 8-17 DRAM Timing (No Wait State, One Byte Read)

8.3.12 DRAM Timing (Wait State, One Byte Read)

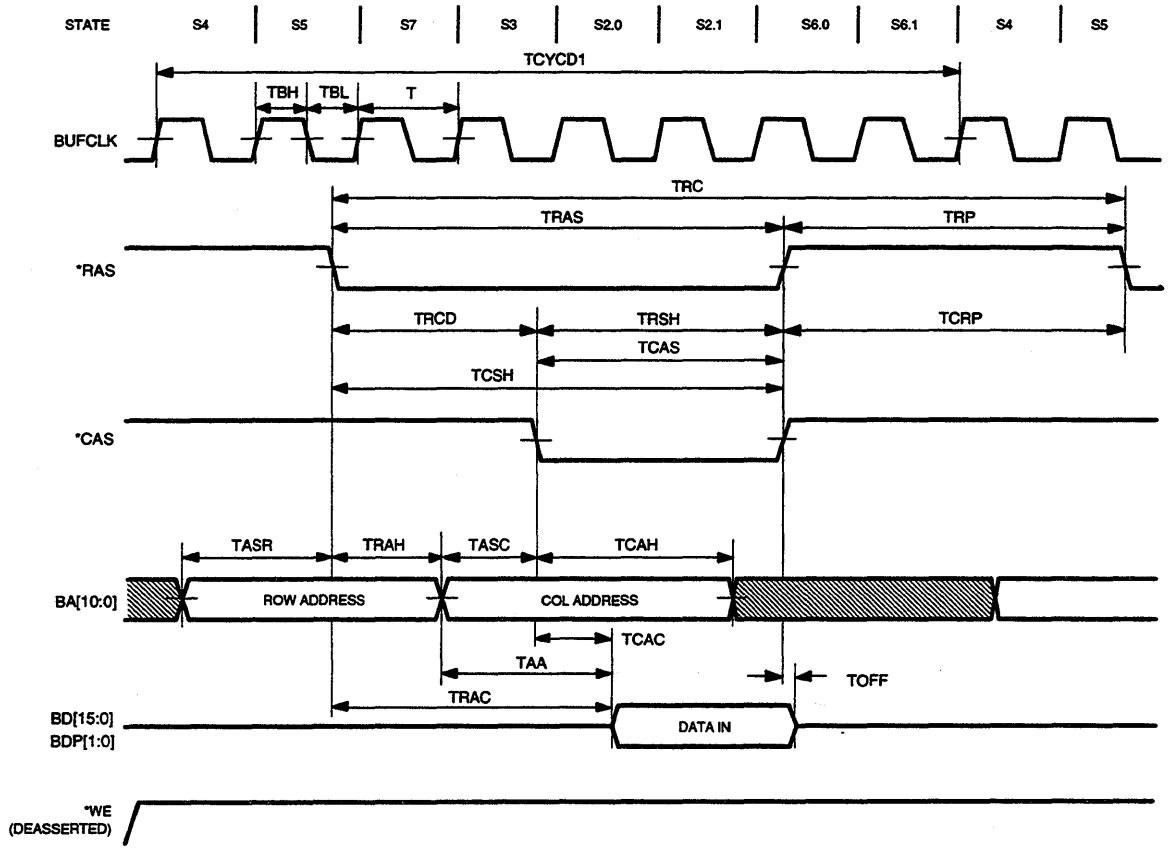


Figure 8-18 DRAM Timing (Wait State, One Byte Read)

8.3.13 DRAM Timing (No Wait State, One Byte Write)

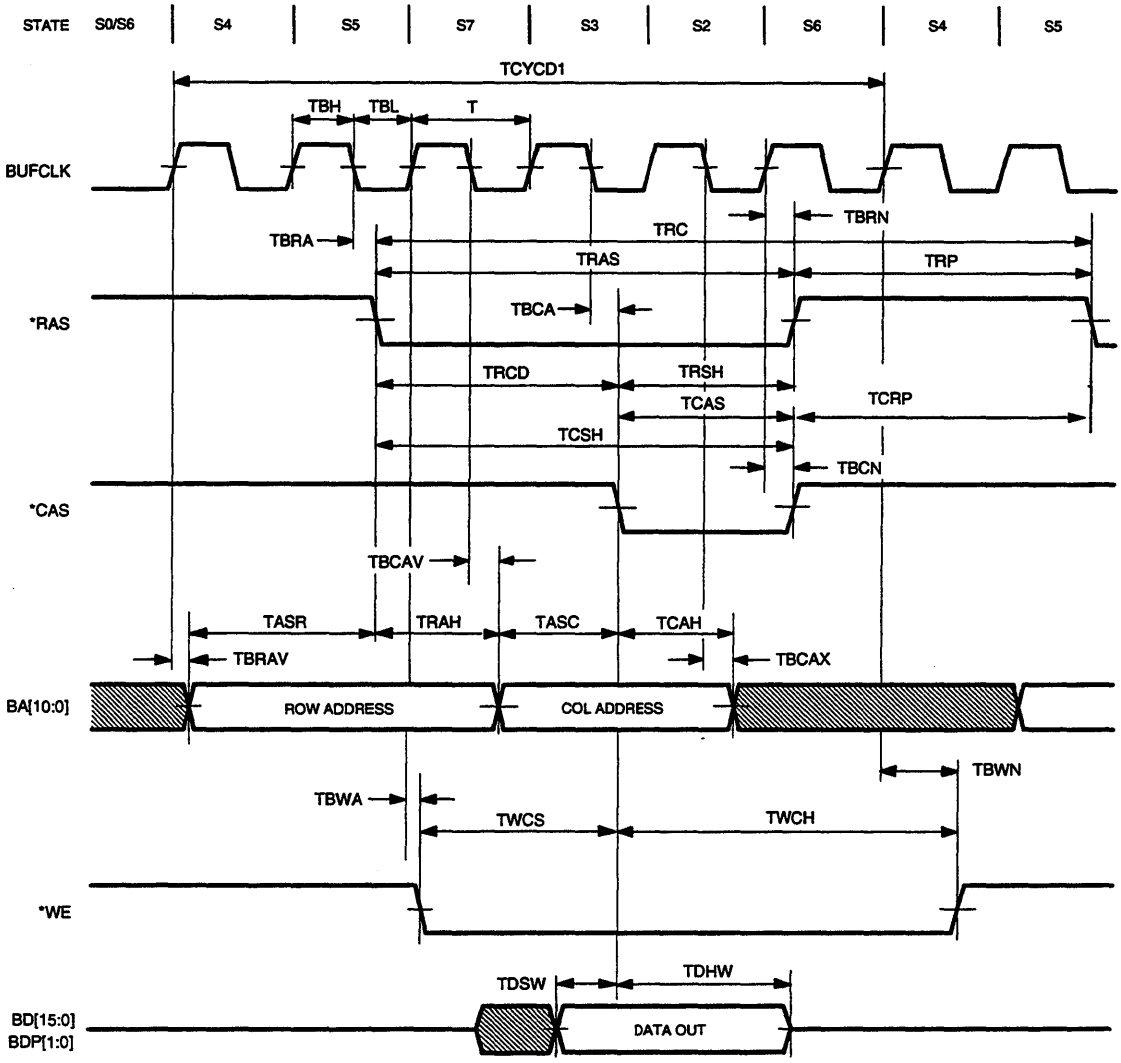


Figure 8-19 DRAM Timing (No Wait State, One Byte Write)

8.3.14 DRAM Timing (Wait State, One Byte Write)

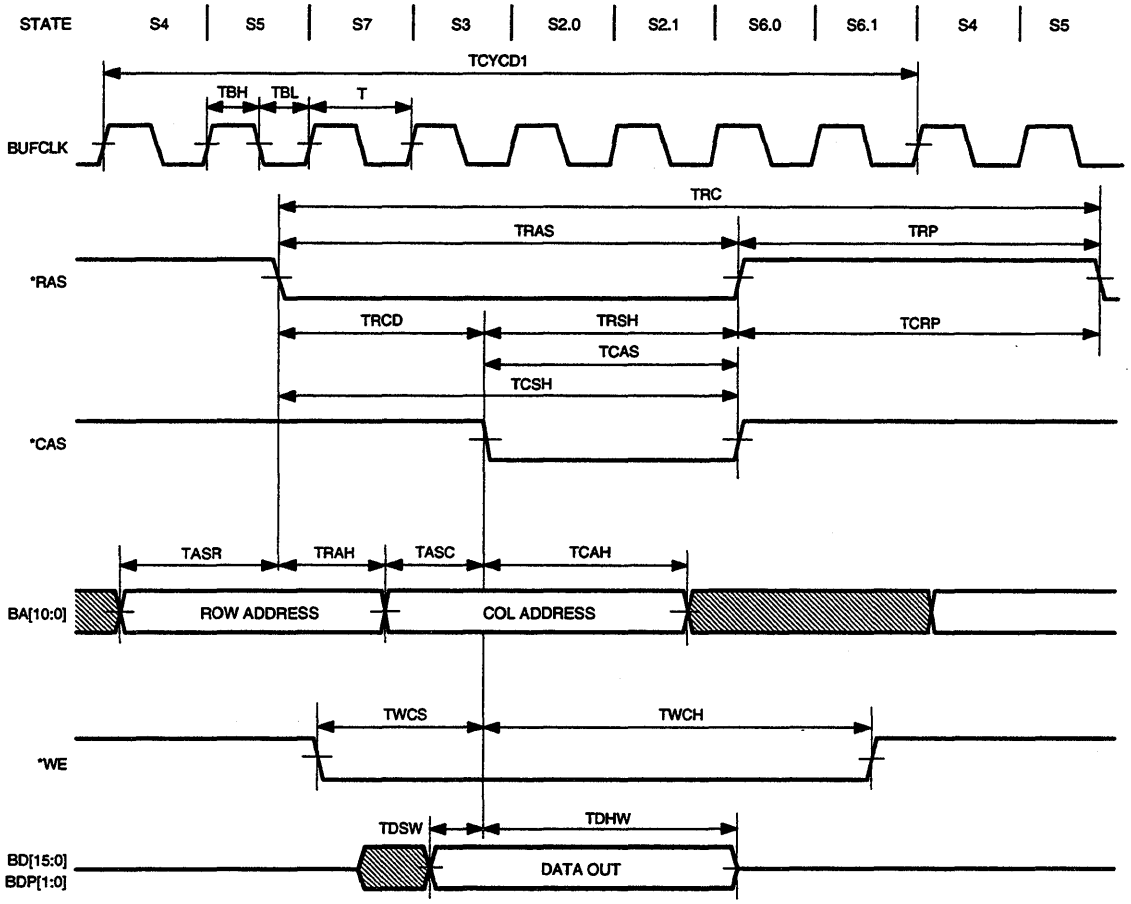


Figure 8-20 DRAM Timing (Wait State, One Byte Write)

8.3.15 DRAM Timing (Page Mode, No Wait State, Read)

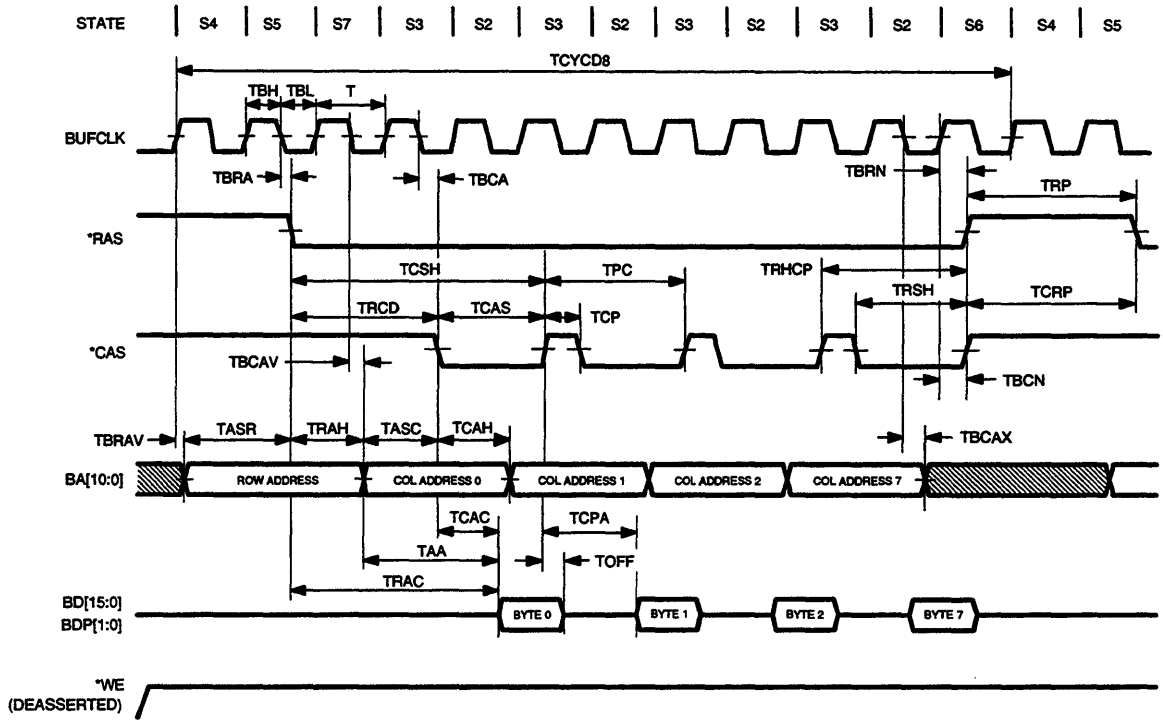


Figure 8-21 DRAM Timing (Page Mode, No Wait State, Read)

8.3.16 DRAM Timing (Page Mode, Wait State, Read)

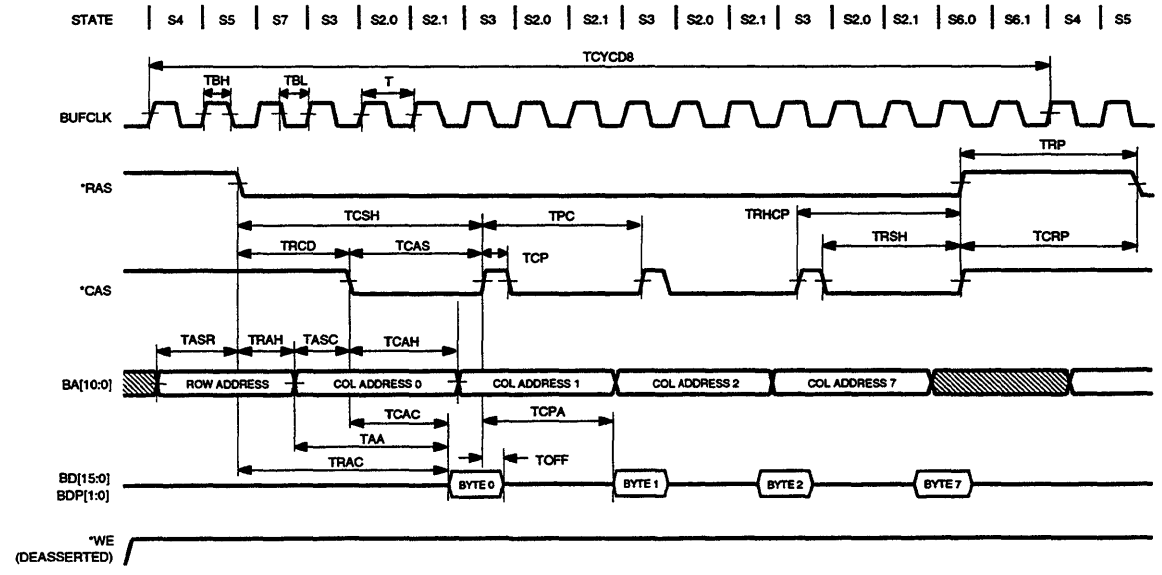


Figure 8-22 DRAM Timing (Page Mode, Wait State, Read)

8.3.17 DRAM Timing (Page Mode, No Wait State, Write)

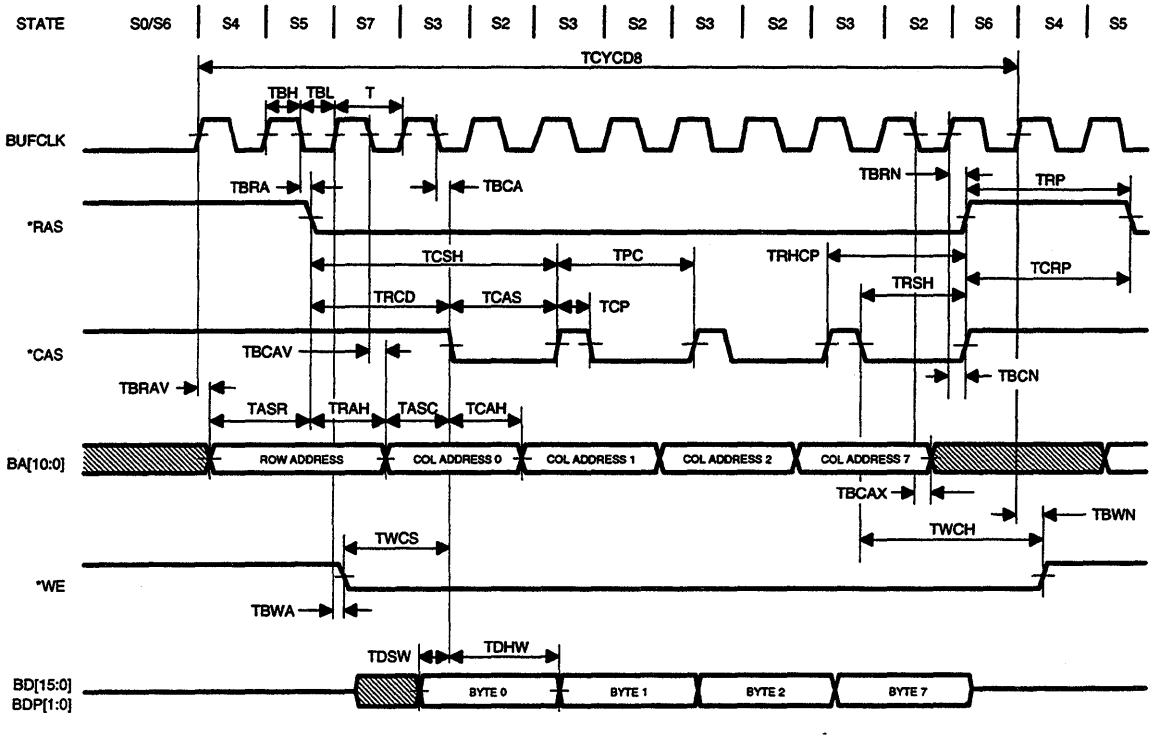


Figure 8-23 DRAM Timing (Page Mode, No Wait State, Write)

8.3.18 DRAM Timing (Page Mode, Wait State, Write)

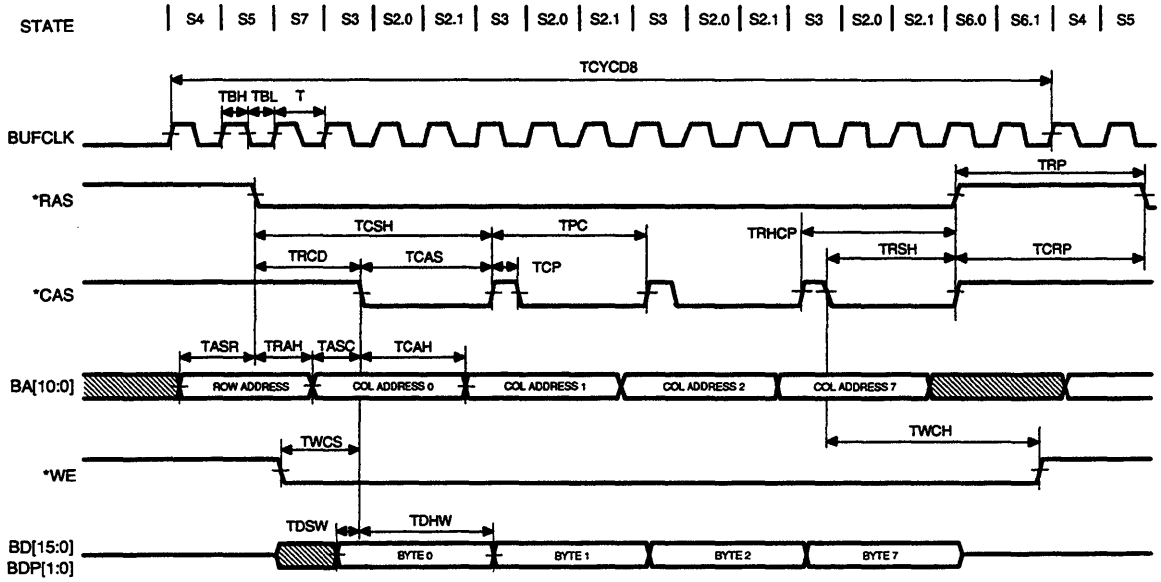


Figure 8-24 DRAM Timing (Page Mode, Wait State, Write)

8.3.19 DRAM Timing (Refresh, No Wait State)

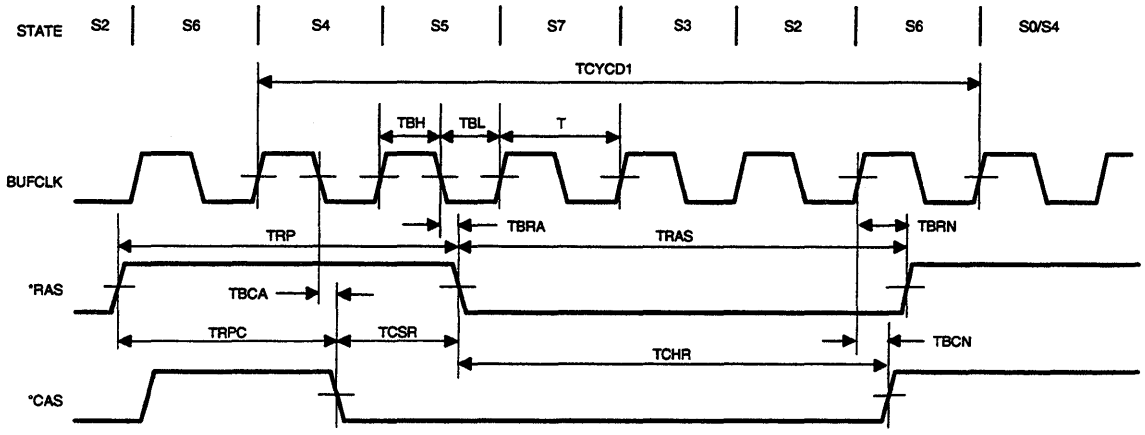


Figure 8-25 DRAM Timing (Refresh, No Wait State)

8.3.20 DRAM Timing (Refresh, Wait State)

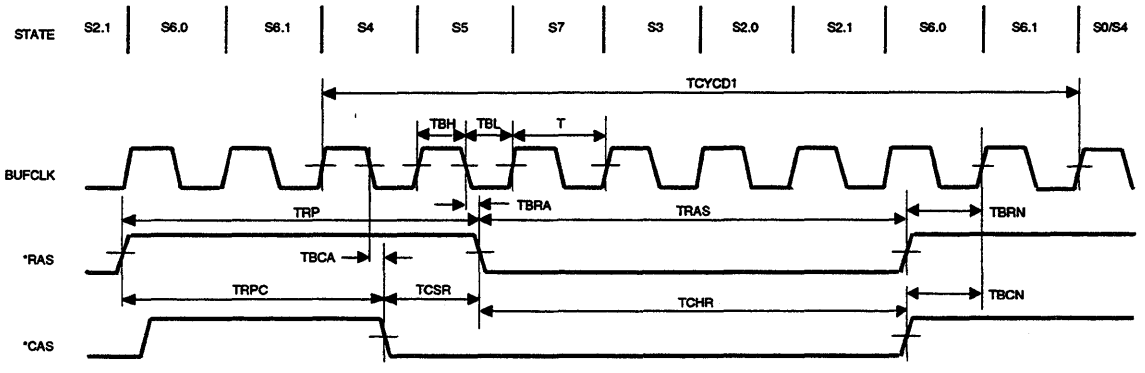


Figure 8-26 DRAM Timing (Refresh, Wait State)

8.4 Disk Interface Timing

8.4.1 Disk Timing Parameters

Symbol	Parameter		Values Min	Typ	Max	Units	Notes
TRRC	Period	(Single NRZ mode)	20			ns	1
		(Dual NRZ mode)	20			ns	2
		(8-bit NRZ mode)	60			ns	3
TRRCH	RRCLK Assert Time	(Single & dual NRZ mode)	8			ns	1 & 2
		(8-bit NRZ mode)	12			ns	3
TRRCL	RRCLK Negated Time	(Single & dual NRZ mode)	8			ns	1 & 2
		(8-bit NRZ mode)	12			ns	3
TNRZIS	NRZ[7:0] (in) Setup	(Single & dual NRZ mode)	5			ns	1 & 2
		(8-bit NRZ mode)	5			ns	3
TNRZIH	NRZ[7:0] (in) Hold	(Single & dual NRZ mode)	5			ns	1 & 2
		(8-bit NRZ mode)	5			ns	3
TDCS	SYNCFND Setup Time	to RRCLK ↑	5			ns	1, 2 & 5
		to RRCLK ↓	5			ns	1, 2 & 5
TDCH	SYNCFND Hold Time	from RRCLK ↑	5			ns	1, 2 & 5
		from RRCLK ↓	5			ns	1, 2 & 5
TDCS	SYNCFND Setup Time	to RRCLK ↓	5			ns	3-5, 10
		to RRCLK ↑	5			ns	3-5, 10
TDCH	SYNCFND Hold Time	from RRCLK ↓	5			ns	3-5, 10
		from RRCLK ↑	5			ns	3-5, 10
TPLHNRZ2	NRZ[1:0] (out) L to H prop. delay	from RRCLK ↓	4		19	ns	1, 2 & 7
		from RRCLK ↑	4		19	ns	1, 2 & 7
TPHLNRZ2	NRZ[1:0] (out) H to L prop. delay	from RRCLK ↓	4		19	ns	1, 2 & 7
		from RRCLK ↑	4		19	ns	1, 2 & 7
TWLHNRZ2	NRZ[1:0] (out) L to H prop. delay	from WCLK ↑	1		10	ns	1, 2 & 7
TWHLNRZ2	NRZ[1:0] (out) H to L prop. delay	from WCLK ↑	1		10	ns	1, 2 & 7
TPLHNRZ8	NRZ[7:0] (out) L to H prop. delay	from RRCLK ↓	4		20	ns	3 & 6
		from RRCLK ↑	4		20	ns	3 & 6
TPHLNRZ8	NRZ[7:0] (out) H to L prop. delay	from RRCLK ↓	4		20	ns	3 & 6
		from RRCLK ↑	4		20	ns	3 & 6
TSCT	Control Input Setup Time		2T+2Tbyte		3T+3Tbyte	BUFCLKs	8 & 9
TCDRS	CDRINT setup to RRCLK ↑		30			ns	
TCDRH	CDRINT hold from RRCLK ↑		10			ns	

See notes on following page.

NOTES: Parameter values assume 20 pF loading on all disk interface pins.

1. For single NRZ mode.
2. For dual NRZ mode.
3. For 8-bit NRZ mode
4. Sync offset specified in RRCLKs (see SYNCOFS[2:0], reg. 61h, R/W, bits 2:0).
5. RRCLK ↑ or ↓ edge programmable (ENSYNCFALL, reg. 60h, R/W, bit 0) with ↑ bit 0=0, ↓ bit 0=1.
6. RRCLK ↑ or ↓ edge programmable (ENNRZFALL, reg. 60h, R/W, bit 5) with ↑ bit 5=0, ↓ bit 5=1, in 8-bit mode.
7. In single- and dual-bit mode, when reg. 60h bit 5=0, WCLK is in phase with RCLK and NRZ Write Data is referenced from RRCLK ↑ (or from WCLK ↑). When reg. 60h bit 5=1, WCLK is inverted with respect to RRCLK and NRZ Write Data is referenced from RRCLK ↓ (or from WCLK ↑).
8. Minimum times required to positively recognize the control signal's leading edge. The active edge can be positive or negative.
9. For single NRZ mode:Tbyte = 8 RRCLK
   For dual NRZ mode:Tbyte = 4 RRCLK
   For 8-bit NRZ mode:Tbyte = 1 RRCLK
10. Offset may be 0 or 1.

8.4.2 Single- and Dual-Bit: Disk Read Timing

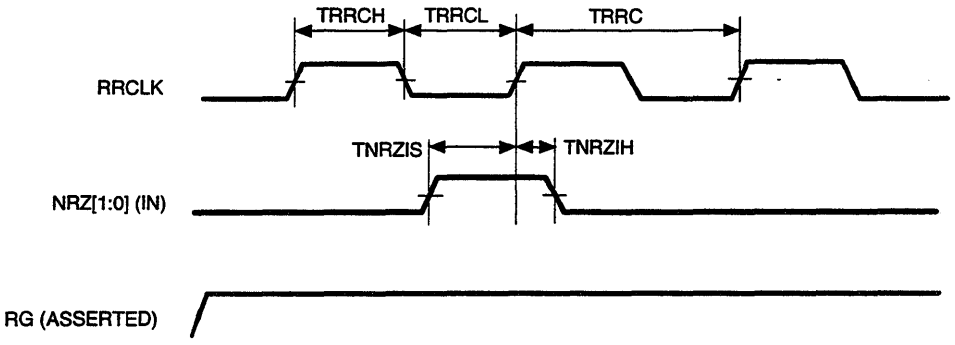


Figure 8-27 Single- and Dual-Bit: Disk Read Timing

8.4.3 Eight-Bit: Disk Read Timing

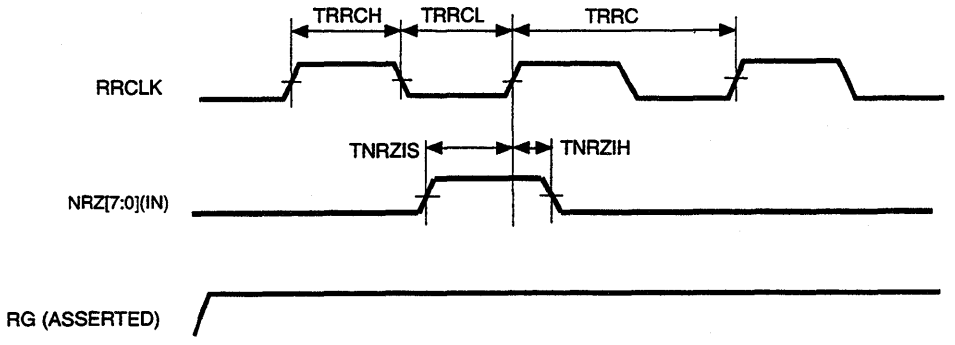
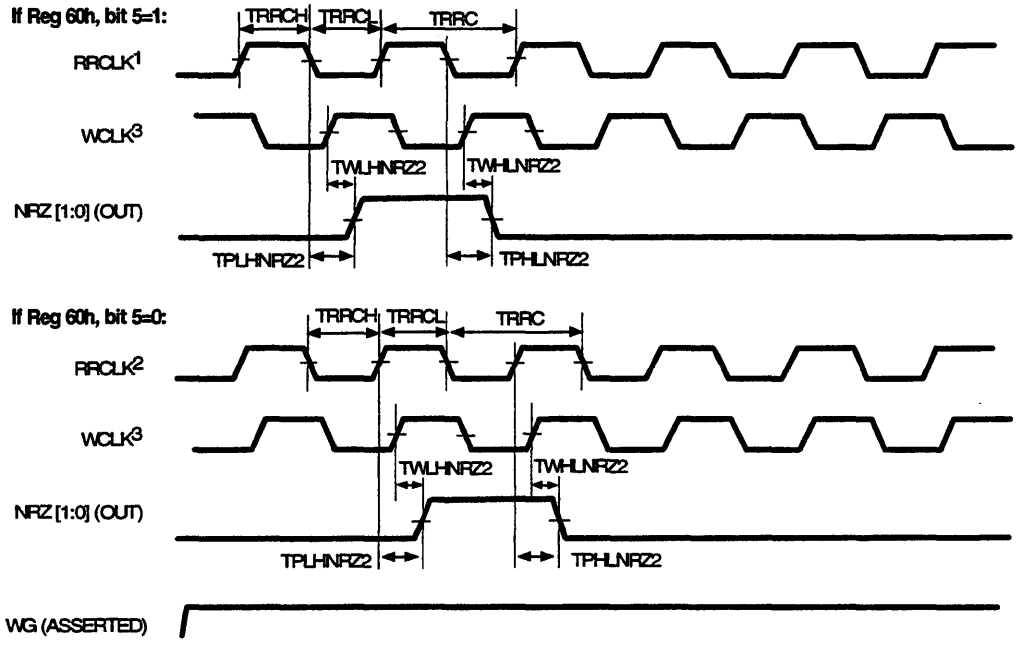


Figure 8-28 Eight-Bit: Disk Read Timing

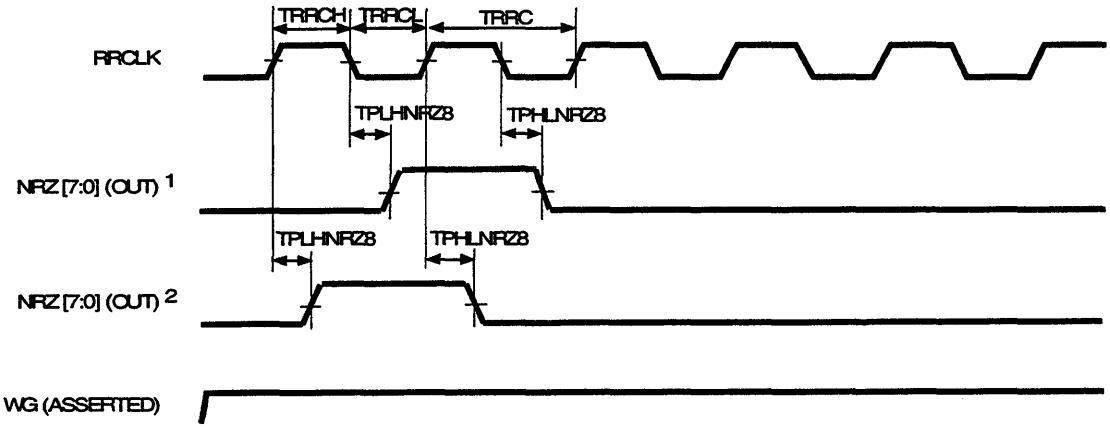
8.4.4 Single- and Dual-Bit: Disk Write Timing



NOTES: 1. If reg. 60h, bit 5=1, NRZ Write Data can be referenced from WCLK↑ or RRCLK↓. If bit 5=1, WCLK is inverted with respect to RRCLK.
2. If reg. 60h, bit 5=0, NRZ Write Data can be referenced from WCLK↑ or RRCLK↑. If bit 5=0, WCLK is in phase with RRCLK.
3. NRZ [1:0] can be referenced from RRCLK↓ or ↑,or from WCLK↑. In single- & dual-bit mode, NRZ Write Data always follows WCLK↑.

Figure 8-29 Single- and Dual-Bit: Disk Write Timing

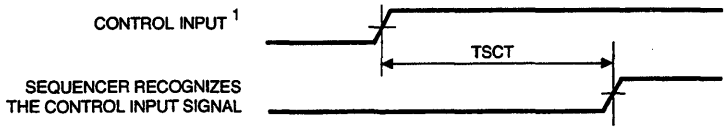
8.4.5 Eight-Bit: Disk Write Timing



NOTES: 1. NRZ [7:0] if Reg. 60h, bit 5 = 1 (referenced from RRCKL↓.)
2. NRZ [7:0] if Reg. 60h, bit 5 = 0 (referenced from RRCKL↑.)

Figure 8-30 Eight-Bit: Disk Write Timing

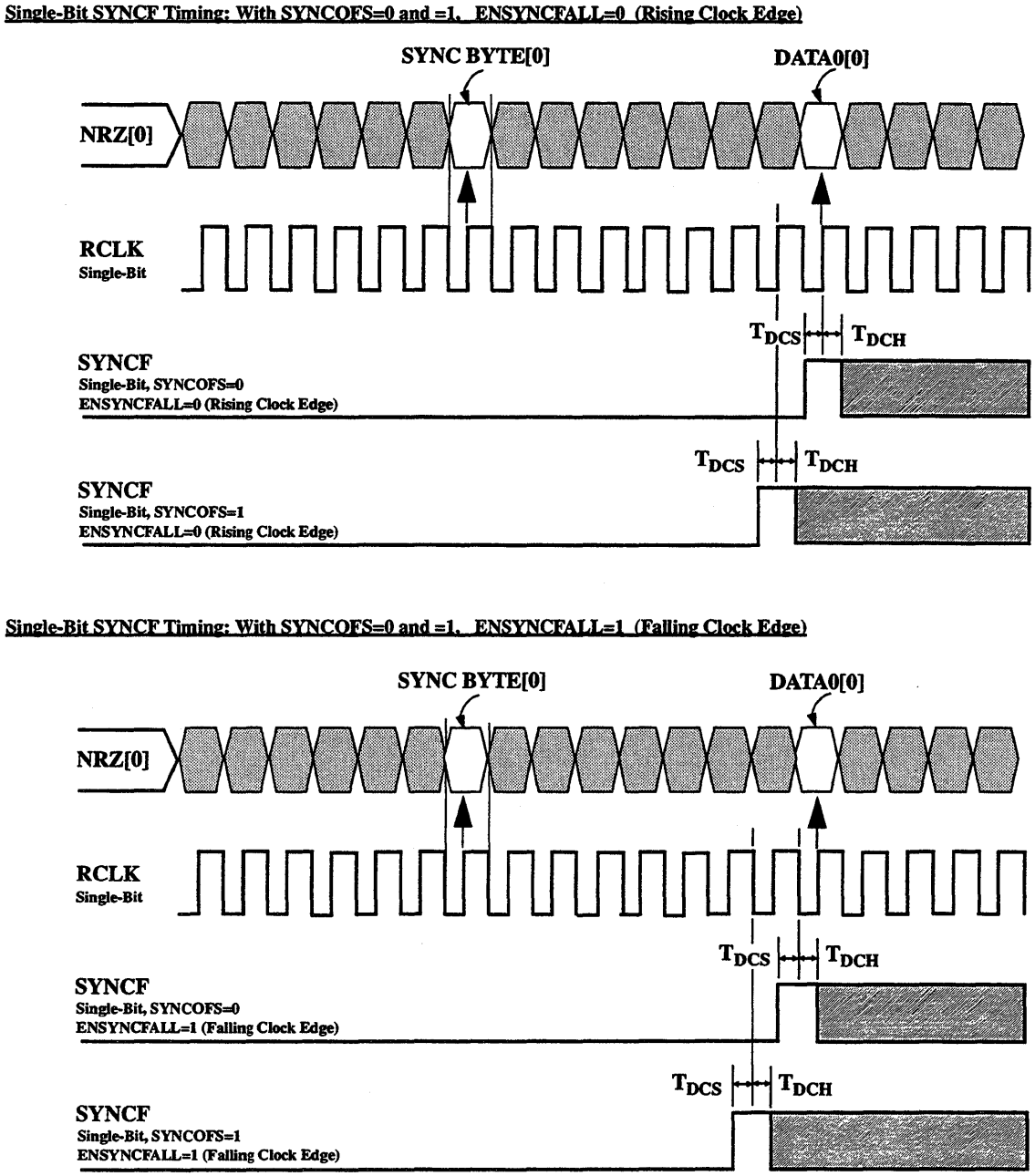
8.4.6 Disk Control Timing



1 SECTOR, INDEX, INPUT, EOS

Figure 8-31 Disk Control Input Timing

8.4.7 External Sync Found Timing

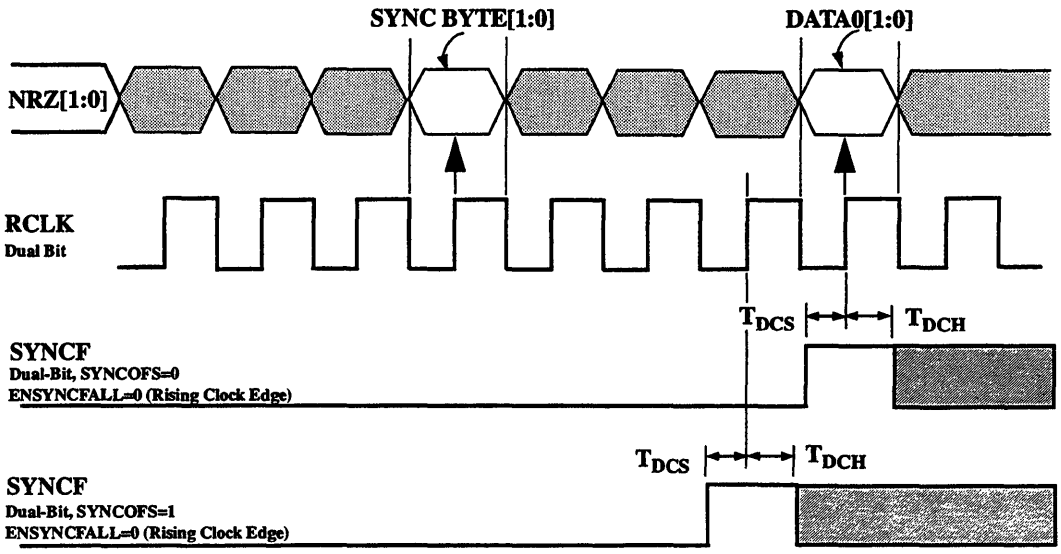


NOTE: SYNCF is shown for Sync Offset = 0 and =1. SYNCF can be internally delayed to get the alignment shown here. See DCTL1 Reg 61h, R/W, bits 2:0.

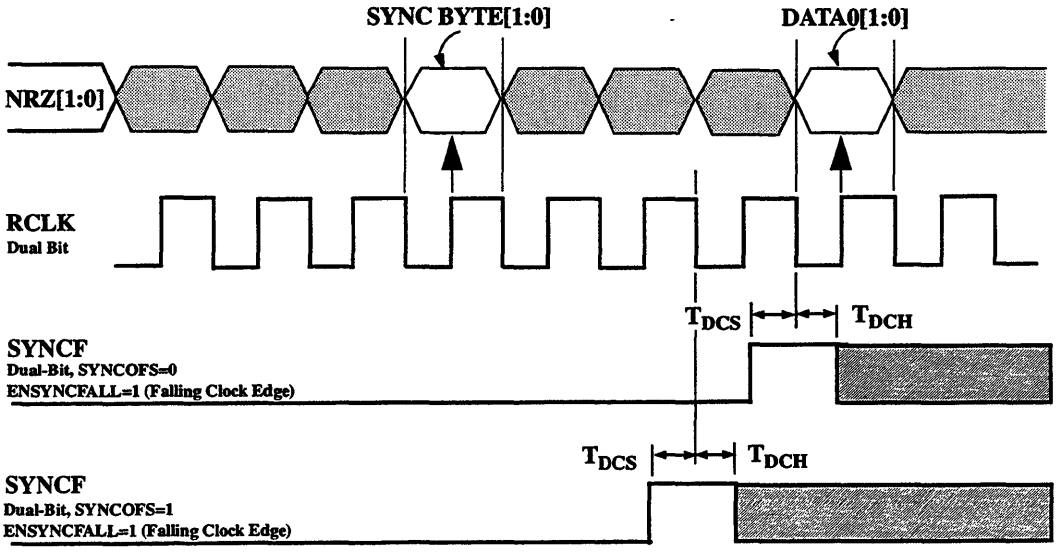
Figure 8-32 External Sync Found Timing

(Single-Bit SYNCF Timing)

Dual-Bit SYNCF Timing: With SYNCOFS=0 and =1, ENSYNCFALL=0 (Rising Clock Edge)



Dual-Bit SYNCF Timing: With SYNCOFS=0 and =1, ENSYNCFALL=1 (Falling Clock Edge)

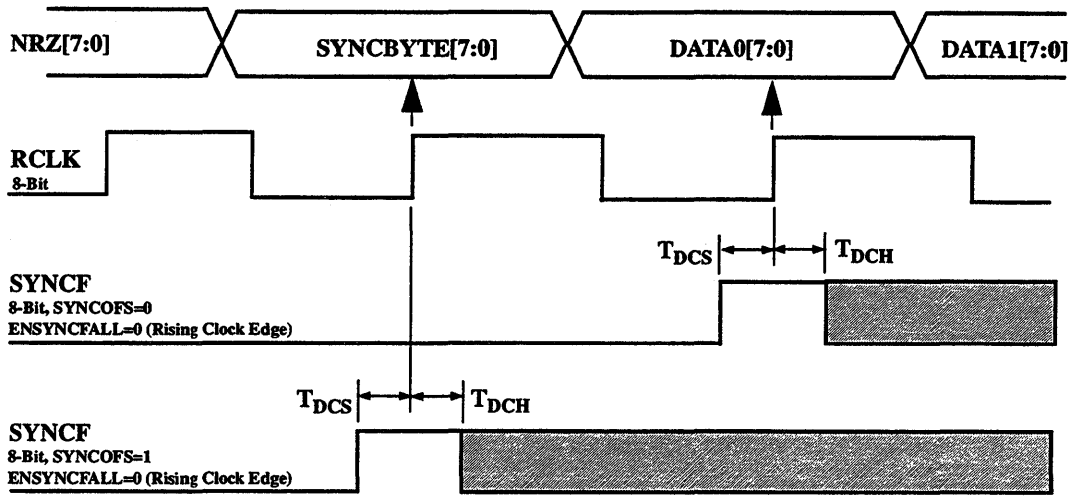


NOTE: SYNCF is shown for Sync Offset = 0 and =1. SYNCF can be internally delayed to get the alignment shown here. See DCTL1 Reg 61h, R/W, bits 2:0.

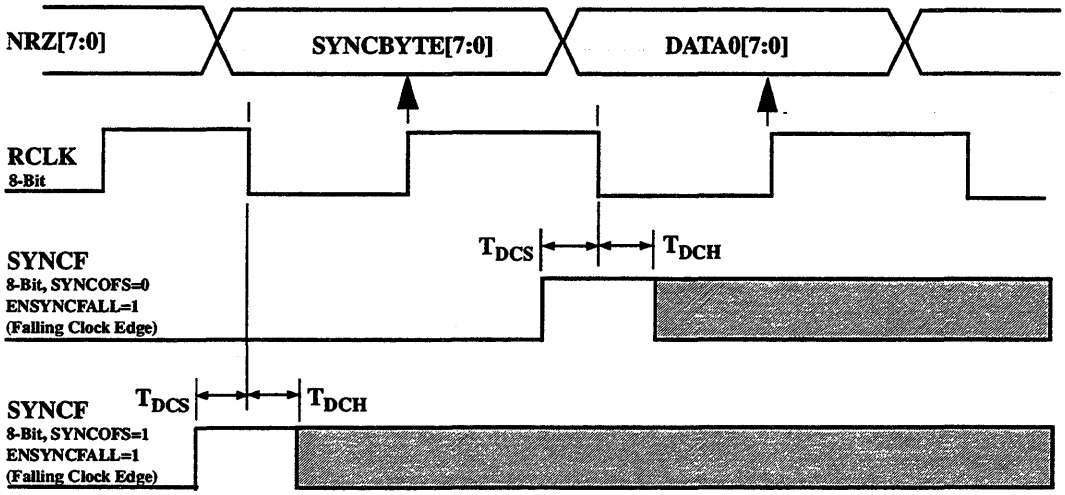
Figure 8-32B External Sync Found Timing (Continued)

(Dual-Bit SYNCF Timing)

8-Bit SYNCF Timing: With SYNCOFS=0 and =1, ENSYNCFALL=0 (Rising Clock Edge)



8-Bit SYNCF Timing: With SYNCOFS=0 and =1, ENSYNCFALL=1 (Falling Clock Edge)



NOTE: SYNCF is shown for Sync Offset = 0 and =1. SYNCF can be internally delayed to get the alignment shown here. See DCTL1 Reg 61h, R/W, bits 2:0.

Figure 8-32C External Sync Found Timing (Continued)

(8-Bit SYNCF Timing)

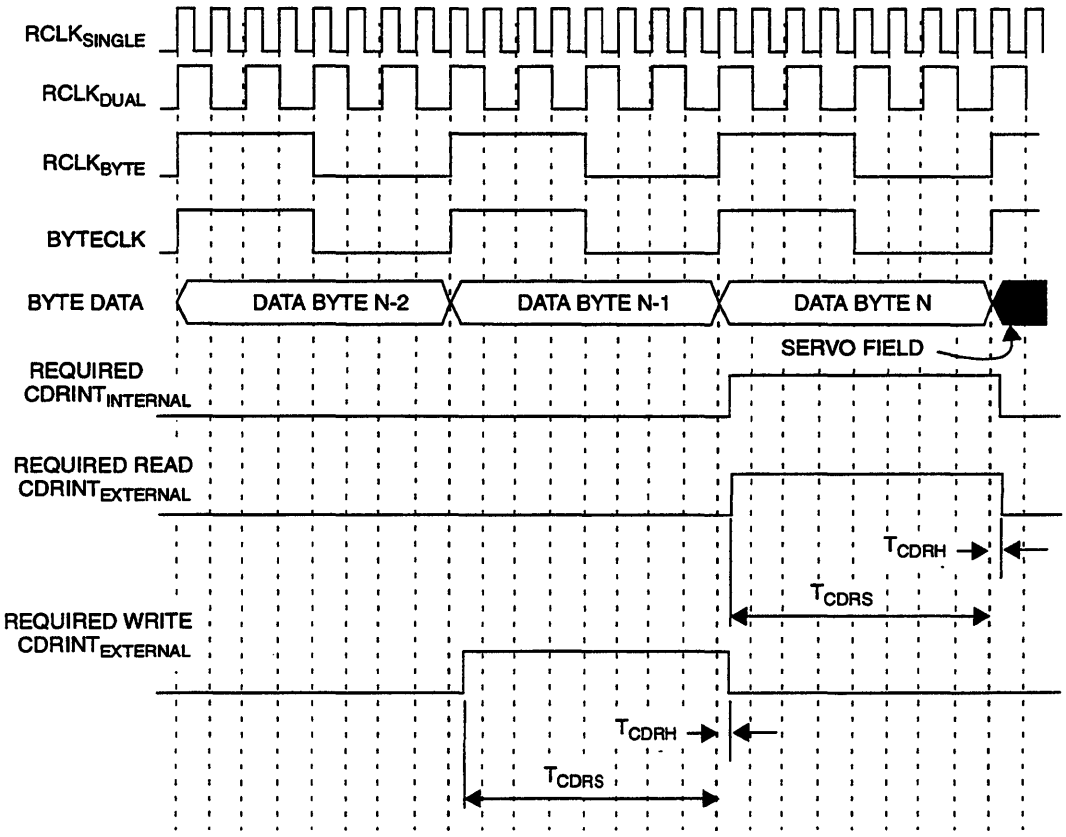


Figure 8-33 External CDR Interrupt Timing

8.5 AT Host Interface Timing

8.5.1 AT Host Timing Parameters

Symbol	Parameter	Values			Units	Notes
		Min	Typ	Max		
TDRQL	DMARQ Negation from *DMACK Asserted Time			20	ns	
TPW	*IOR/*IOW Pulse Width	50			ns	1
TRDA	HD[15:0] driven from *IOW/*IOR Asserted Time	0			ns	2 & 3
TRDA2	*HCS[1:0] and HA[2:0] valid to HD[15:0] Asserted	0			ns	2
TRDV	HD[15:0] Valid from *IOR Asserted			30	ns	
TDKZ	*DMACK Negated to HD[15:0] Tristated			40	ns	4
TRDV2	*HCS[1:0] and HA[2:0] Valid to HD[15:0] Valid			30	ns	
TDKA	HD[15:0] driven from *DMACK Asserted	0			ns	3
TDKV	*DMACK Asserted to HD[15:0] Valid			40	ns	
TRDZ	*IOR/*IOW Negated to HD[15:0] Tristated			30	ns	5
TRDZ2	Address Invalid to HD[15:0] Tristated			30	ns	
TWDS	Write Data to *IOW Negated Setup Time	10			ns	
TWDH	Write Data Hold Time from *IOW Negated	5			ns	
TRDH	*RD Data Hold Time from *IOR Negated	5		•	ns	
TADS	Address and HCS[1:0] Setup Time to Assertion of *IOR and *IOW	20			ns	
TADH	Address and HCS[1:0] Hold Time from Negation of *IOR or *IOW	0			ns	
TIOCSL	Address Valid to *IOCSI6 Setup Time			30	ns	
TIOCHL1	*IOR/*IOW Asserted to IOCHRDY Negated			20	ns	6
TIOCHL2	Reg. 1F0h (read data) selected to IOCHRDY Negated			•	ns	6
TIOCHPW	IOCHRDY Pulse Width				ns	7
TIOCSH	*IOCS16 Negated Hold Time from Address Invalid.			30	ns	
TDDRQL	*IOR or *IOW Assertion to DMARQ Negation			30	ns	
TDACKS	*DMACK Asserted to *IOR or *IOW Asserted Setup Time	0			ns	
TDACKH	*DMACK Negated to *IOR or *IOW Negated Hold Time	0			ns	
TMACH	*IOW/*IOR Negated to *DMACK Negated Hold time	5			ns	
TDHT	*DMACK Negated to HD[15:0] Tristated			25	ns	8
TRDV3	*IOR Negated to HD[15:0] Valid			30	ns	4 & 5
TMWC	Multi-word DMA Cycle Time	120			ns	

See notes on following page.

NOTES:

1. Minimum pulse width determined by components in R/W path, host, and Setup/hold times given here. Pulse widths compliant with PIO mode 4 and DMA mode 2 are valid.
2. TRDA is applicable while the HDBDRVPIO bit (reg, C6h, R/W, bit 0) is cleared; TRDA2 is applicable while this bit is set. *(for PIO mode)*
3. TRDA is applicable while the HDBDRVDMA bit (reg, C6h, R/W, bit 4) is cleared; TDKA is applicable while this bit is set. *(for DMA mode)*
4. TDKZ is applicable while the HDBDRVDMA bit (reg, C6h, R/W, bit 4) is cleared; TRDV3 is applicable while this bit is set. *(for DMA mode)*
5. TRDZ is applicable while the HDBDRVPIO bit (reg, C6h, R/W, bit 0) is cleared; TRDV3 is applicable while this bit is set. *(for PIO mode)*
6. TIOCHL1 is applicable while the DXFRMODE bit (reg, C5h, R/W, bit 0) is cleared; TIOCHL2 is applicable while this bit is set.
7. The length of time that this signal is negated is determined by when data becomes present in the Host FIFO (see reg. C5h, R/W, bit 2). In addition, if data is available at the time of assertion of the *IOR or *IOW signal, IOCHRDY will not be negated.
8. Applies at end of an ATA multi-word DMA cycle, when *DMACK is negated.

8.5.2 AT PIO Timing

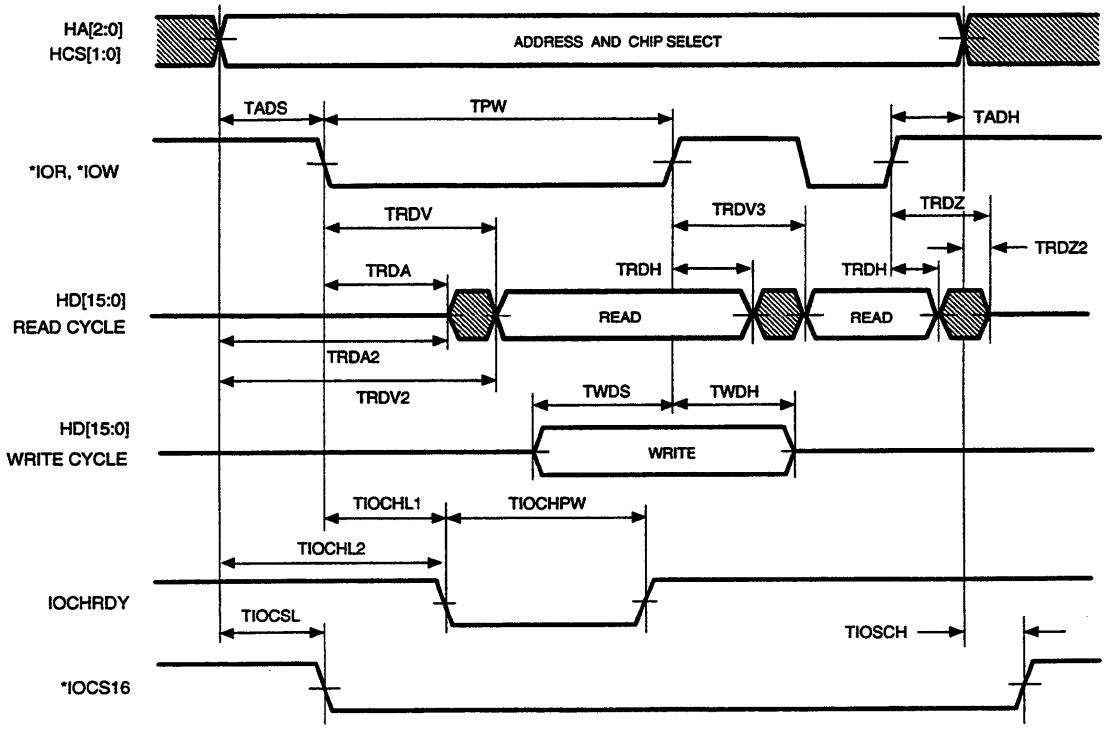


Figure 8-34 AT PIO Timing

8.5.3 ATA Single-Word DMA Timing

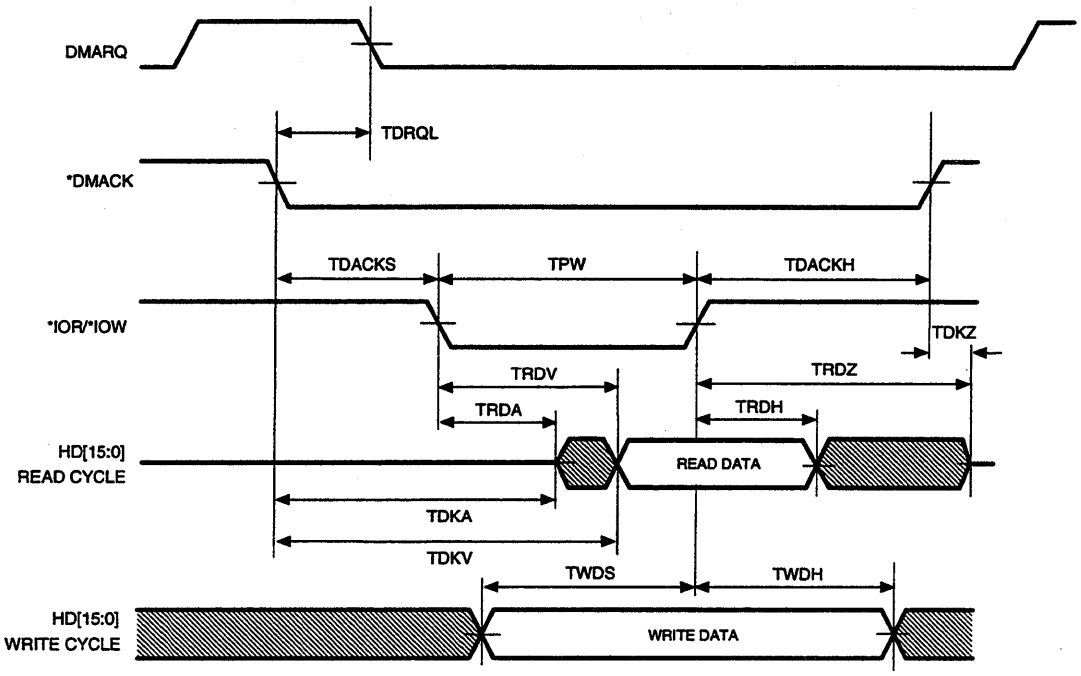


Figure 8-35 AT Single-Word DMA Timing

8.5.4 ATA Multi-Word DMA Timing

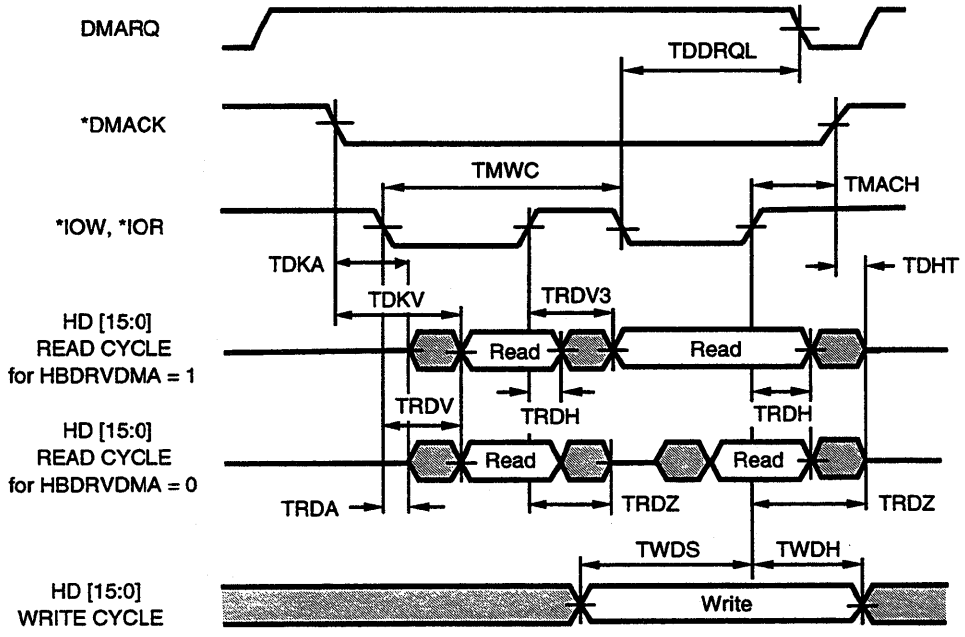


Figure 8-36 AT Multi-Word DMA Timing

8.6 PCMCIA Host Interface Timing

8.6.1 PCMCIA Host Timing Parameters

Symbol	Parameter	Values Min	Typ	Max	Units	Notes
TADS	Address Setup Time	30			ns	
TADH	Address Hold Time	10			ns	
TPWM	*HOE/*HWE Pulse Width	55			ns	
TPWIO	*IOR/*IOW Pulse Width	55			ns	
TRDA	Data Valid from *IORD or *HOE Asserted			45	ns	
TRDH	Read Data Hold Time from *IOR or *HOE Deasserted	0		30	ns	
TWDS	Write Data Setup Time	10			ns	
TWDH	Write Data Hold Time from *IOW or *HWE Deasserted	10			ns	
TREGS	*REG and *HCE1/*HCE2 Setup Time	5			ns	
TREGH	*REG Hold from *IORD/*IOWR or *HOE/*HWE Deasserted	0			ns	
TINPL	*INPACK Low from *IORD Asserted			45	ns	Note 1
TCEH	*HCE1/*HCE2 Hold from *IORD/*IOWR or *HOE/*HWE Deasserted	10			ns	
TCES	*HCE1/*HCE2 Setup to *IORD/*IOWR or *HOE/*HWE	0			ns	
TIO16L	*IOIS16 Asserted from Address Valid			35	ns	Note 2
TIO16H	*IOIS16 Deasserted from Address Invalid			35	ns	Note 2

NOTES:

1. Only valid in I/O read modes.
2. Not used in Attribute or Memory modes.

8.6.2 PCMCIA Attribute Memory Read/Write Timing

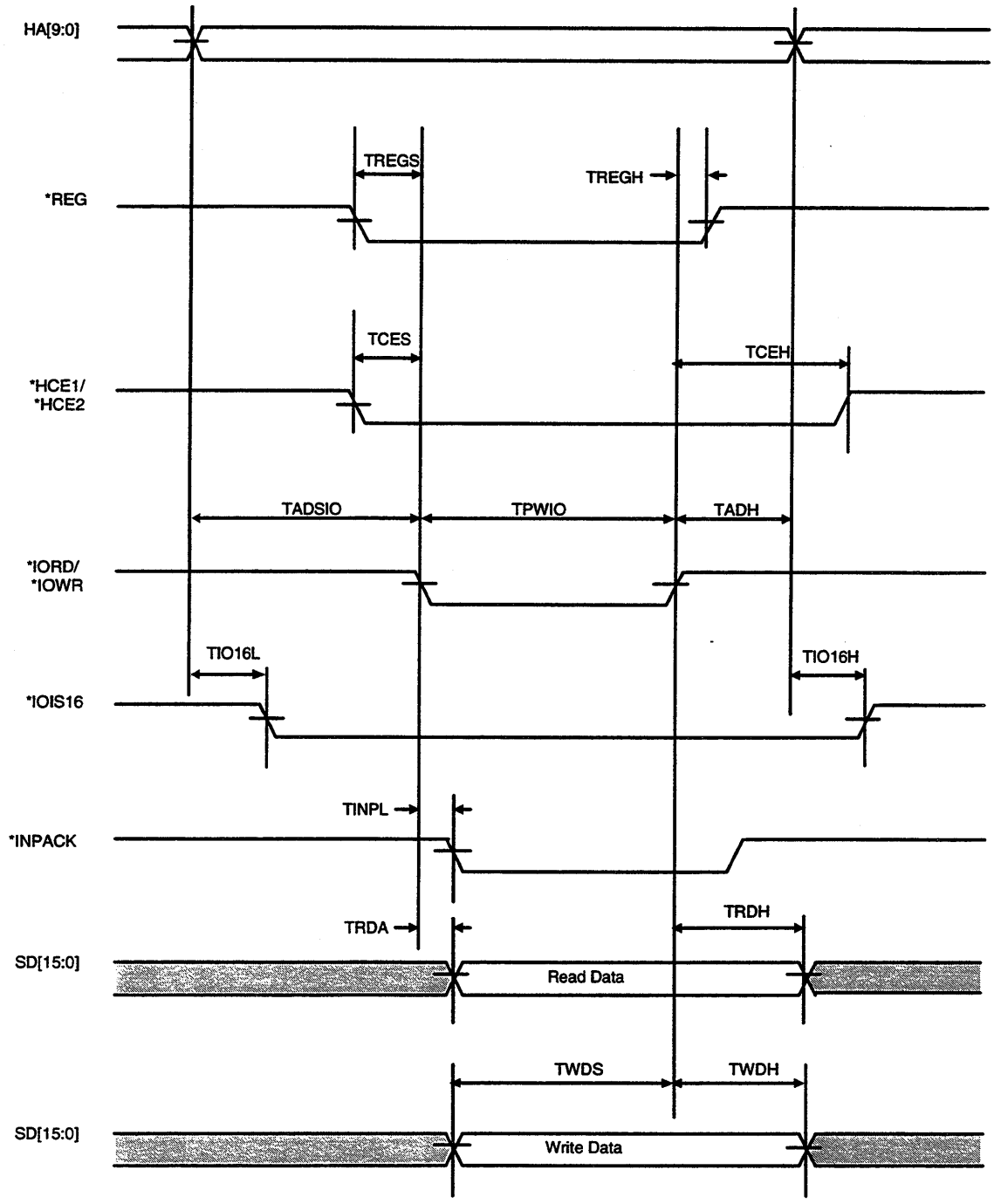


Figure 8-37 PCMCIA Attribute Memory R/W Timing

8.6.3 PCMCIA Primary/Secondary Input/Output Addressing Mode Timing

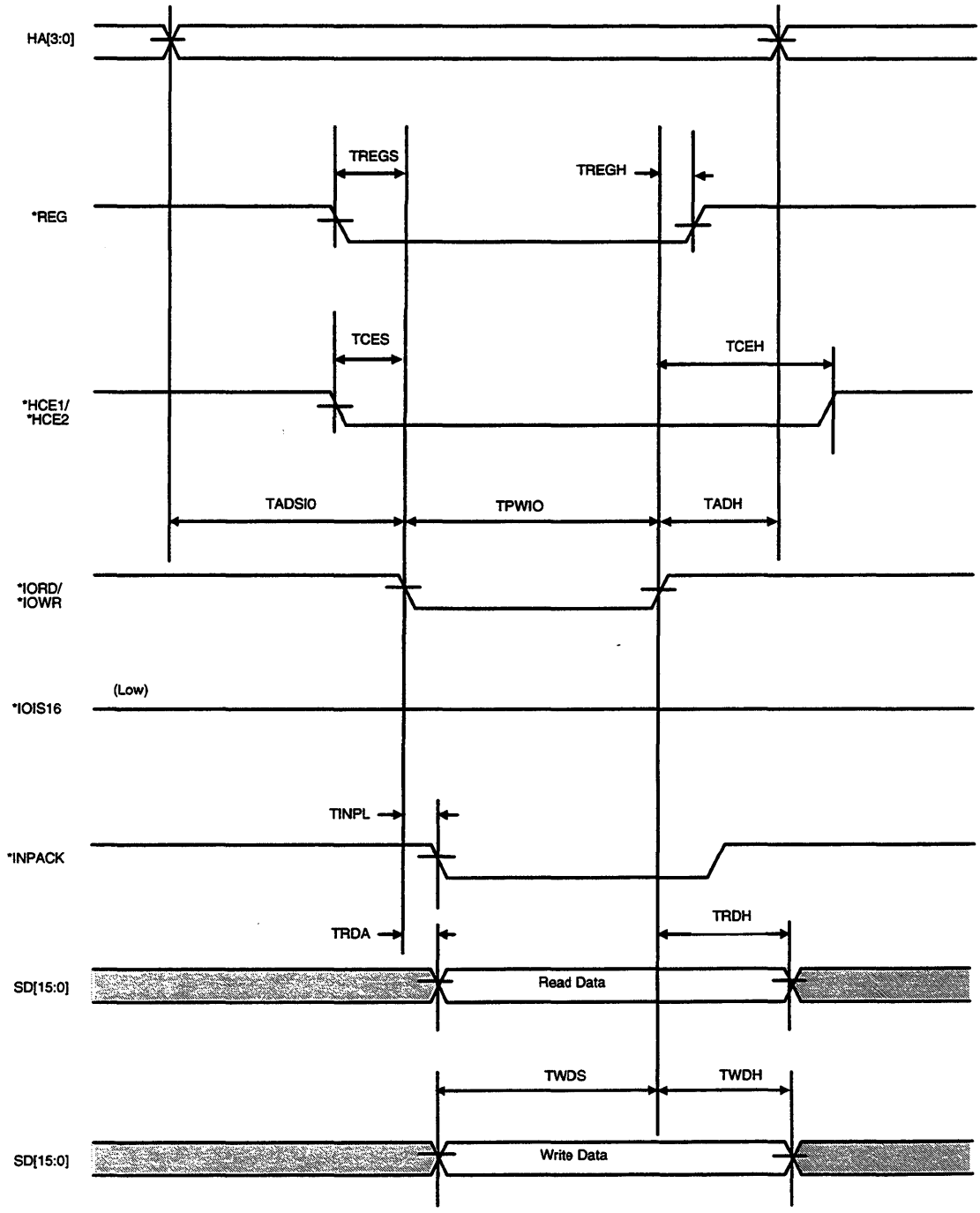


Figure 8-38 PCMCIA Primary/Secondary I/O Mode Timing

8.6.4 PCMCIA Block Mode Input/Output Addressing Mode Timing

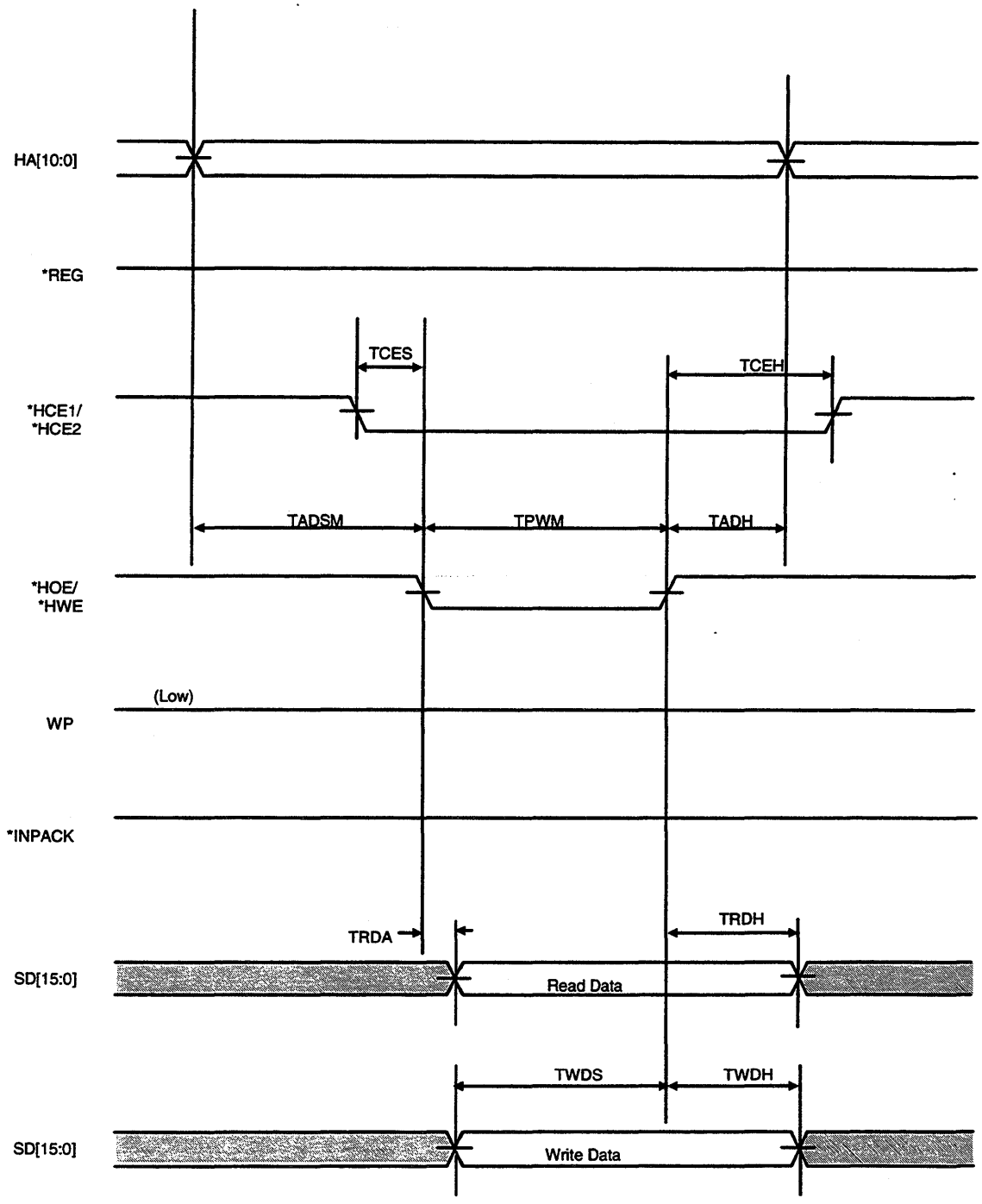


Figure 8-39 PCMCIA Block I/O Mode Timing

8.6.5 PCMCIA Memory Addressing Mode Timing

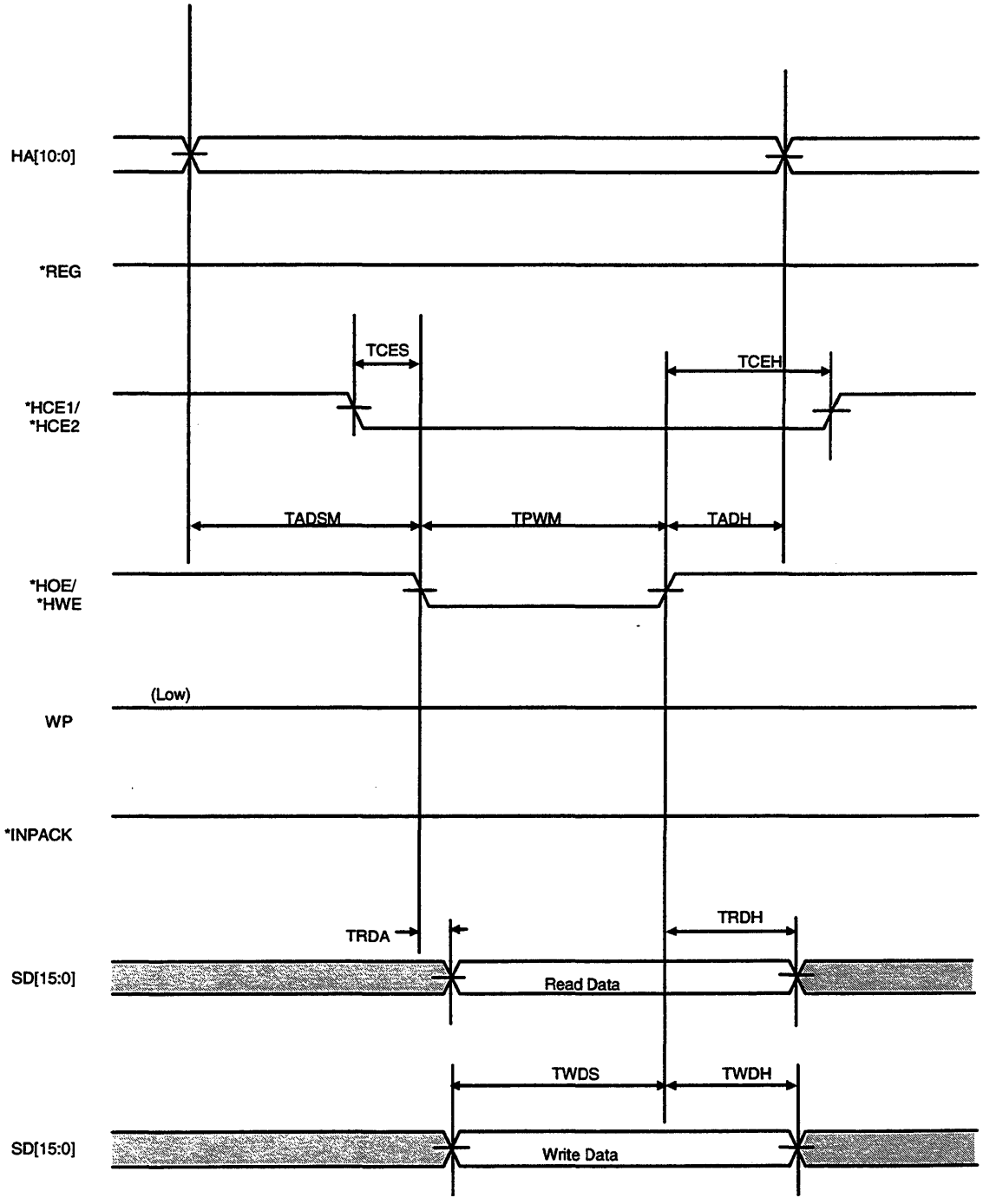


Figure 8-40 PCMCIA Memory Mode R/W Timing

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9.1 AIC-8375 MQFP Packaging Specifications

Figure 9-1 shows the physical dimensions of the AIC-8375's 128-pin MQFP package.

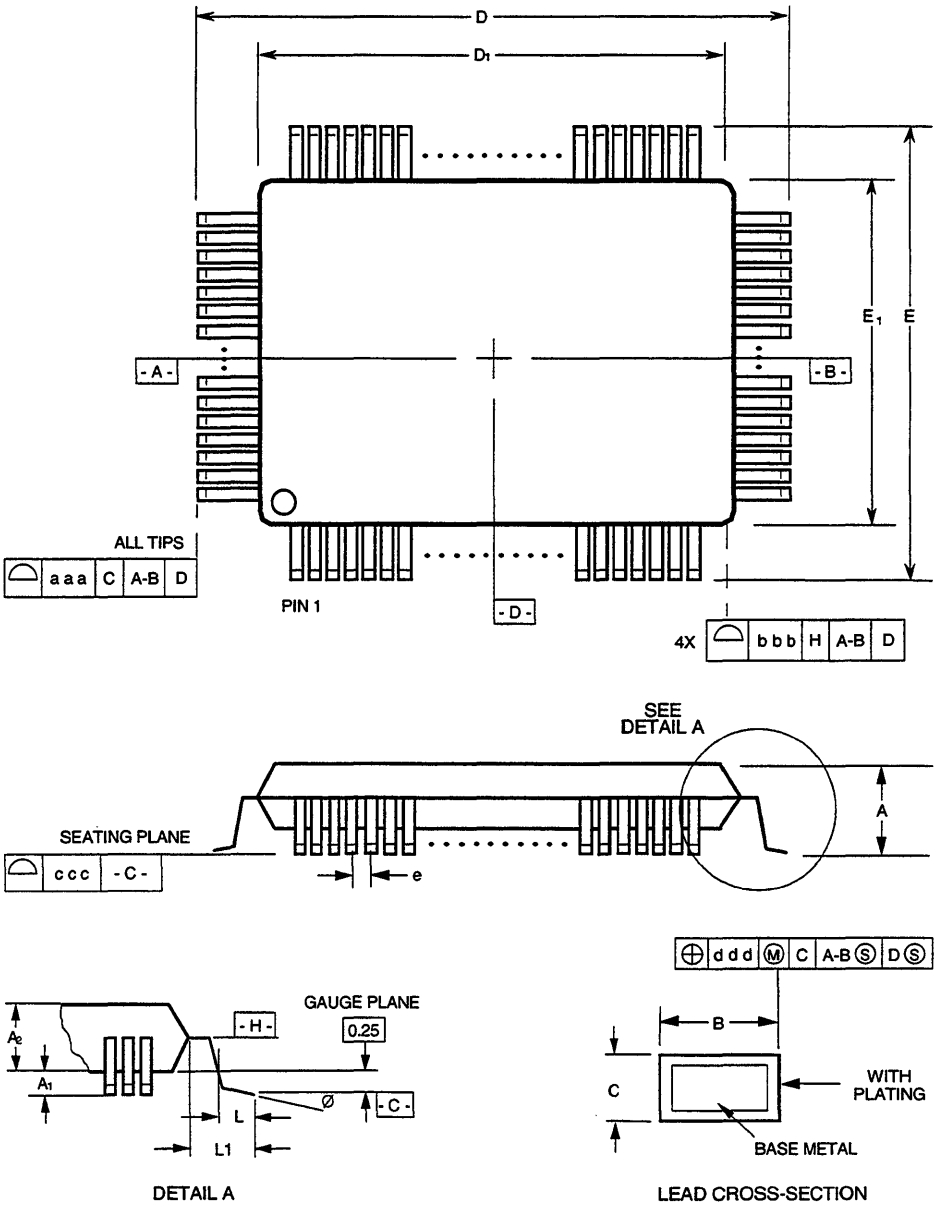

Figure 9-1 128-Pin MQFP Package Outline

Table 9-1 AIC-8375 MQFP Package Dimensions

SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	3.40	-	-	0.134
A1	0.25	-	-	.010	-	-
A2	2.55	2.80	3.05	0.100	0.110	0.120
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.13	-	0.23	0.005	-	0.009
D	22.95	23.20	23.45	0.904	0.913	0.923
D1	19.90	20.00	20.10	0.783	0.787	0.791
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.50 BSC			0.02 BSC		
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 BSC			0.063 BSC		
Ø	0 deg	3.5 deg	7 deg	0 deg	3.5 deg	7 deg
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

**NOTES:*

1. *Controlling dimensions are in millimeters (mm).*
2. *Datums A-B and -D- to be determined at datum plane -H-.*
3. *Reference plane -H- is located at mold parting line and is coincident with bottom of lead where it exits plastic body.*
4. *Dimensions D and E to be determined at seating plane -C-.*
5. *Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.*
6. *Dimension B does not include dambar protrusion. Allowable protrusion shall be .08 mm total in excess of B dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07 mm.*
7. *The dimensions shown in lead cross-section apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.*
8. *A1 is defined as the distance from the seating plane to the lowest point of the package body.*
9. *Solder plate thickness shall be 200 microinches minimum.*

9.2 AIC-8375 TQFP Packaging Specifications

Figure 8-2 shows the physical dimensions of the AIC-8375's 128-pin TQFP package.

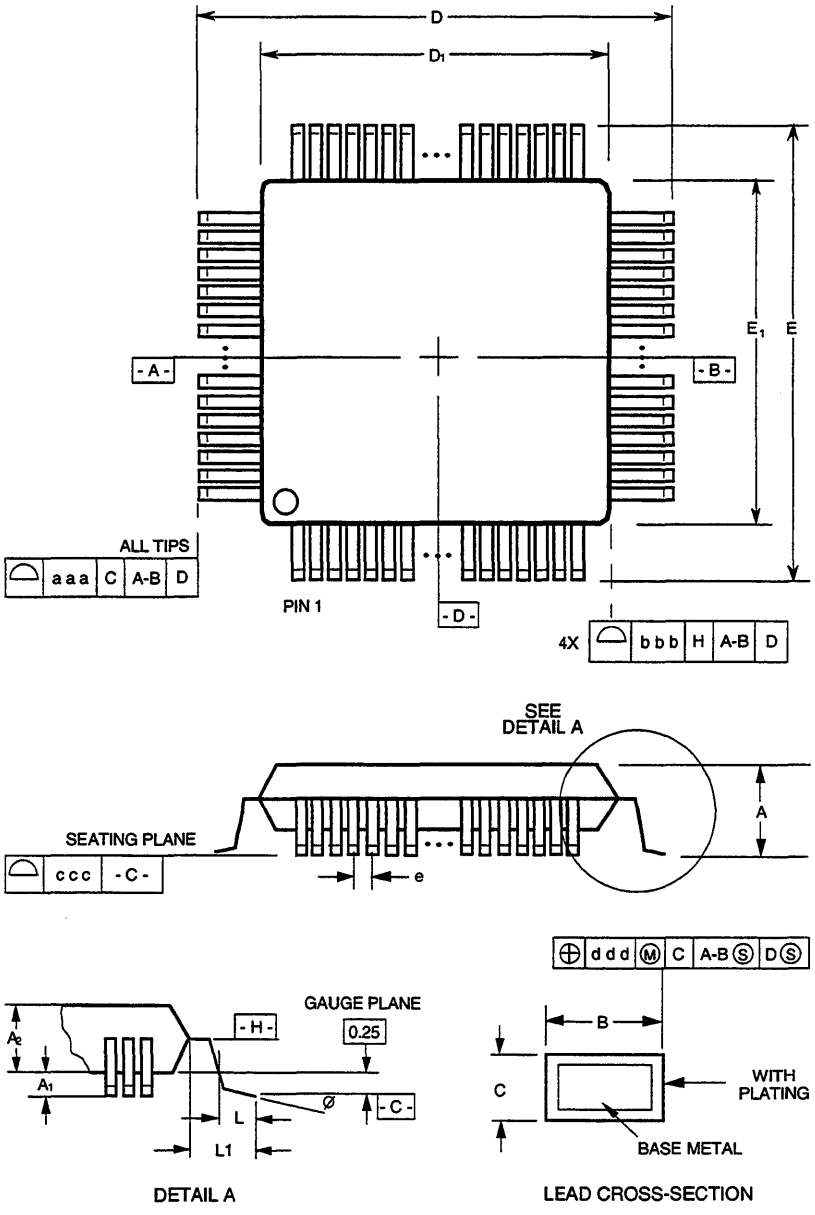

Figure 9-2 128-Pin TQFP Package Outline

Table 9-2 AIC-8375 TQFP Package Dimensions

SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.13	0.18	0.23	0.005	0.007	0.009
C	0.09	-	0.20	0.004	-	0.008
D	16.00 BSC			0.630 BSC		
D1	14.00 BSC			0.551 BSC		
E	16.00 BSC			0.630 BSC		
E1	14.00 BSC			0.551 BSC		
e	0.40 BSC			0.0157 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 BSC			0.039 BSC		
Ø	0 deg	3.5 deg	7 deg	0 deg	3.5 deg	7 deg
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

**NOTES:*

1. *Controlling dimensions are in millimeters (mm).*
2. *Datums A-B and -D- to be determined at datum plane -H-.*
3. *Reference plane -H- is located at mold parting line and is coincident with bottom of lead where it exits plastic body.*
4. *Dimensions D and E to be determined at seating plane -C-.*
5. *Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.*
6. *Dimension B does not include dambar protrusion. Allowable protrusion shall be .08 mm total in excess of B dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07 mm.*
7. *The dimensions shown in lead cross-section apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.*
8. *A1 is defined as the distance from the seating plane to the lowest point of the package body.*
9. *Solder plate thickness shall be 200 microinches minimum.*

ADDENDUM

AIC-8375B Operational Characteristics (10/16/95) Revision B.2

This document details the operational characteristics in the AIC-8375 Rev B device. These items are intended to alert the designer to behaviors of the device that require particular attention.

A.1 Host Block - No discrepancies noted.

A1.1 Buffer Block

A1.1.1 Erroneous Increment Of BCTR After A Write Failure

Condition: During a write operation, if a sector transfer failure occurs within 32 bytes (the depth of the Disk FIFO) of the end of the sector, the BCTR will be erroneously incremented. The BCTR will increment because the entire sector will have been transferred out of the buffer and into the Disk FIFO. Meanwhile, the Disk Sequencer has stopped because of a Write failure.

Workaround: After a sector transfer failure occurs during a write operation, the BCTR may have been erroneously incremented. This needs to be checked by the local microprocessor. This can be done by interrogating the value in the Disk Pointer registers (Reg. 134h-136h) and the Disk FIFO Count (Reg. 7Dh, R, bits 5:0). Using these values the microprocessor can determine if the write error occurred in the window which would cause the BCTR to increment.

A1.1.2 Microprocessor Page Switch Corruption Problem

Condition: If the Microprocessor Page registers (Reg. 110h, 111h) are changed immediately following a microprocessor write to the buffer, the buffer access might use the new updated value in the Microprocessor Page registers as the desired address rather than the original value. If this occurs, the microprocessor will either read from an incorrect location or write to an incorrect location, resulting in data corruption.

Workaround: This situation can be avoided by making sure the Busy For Microprocessor Access bit (Reg. 52h, R, bit 7) is negated before the Microprocessor Page registers (Reg. 110h, 111h) are changed.

A1.1.3 Limitations When Interfacing to DRAMs With Two Write Enables

Condition: If the AIC-8375 is interfaced to a 16-bit DRAM that uses two Write Enable control lines, various restrictions apply.

a. Microprocessor accesses of the buffer must be performed in 16-bit mode only.

b. The external glue logic which is required to interface to this type of DRAM will alter the timing slightly. This can result in slight degradation of timing relationships which may require using either a slower BUFCLK or a higher speed DRAM. An analysis must be performed to determine if the selected operating point is suseptible to this degradation.

Workaround: If attempting to use DRAMs having two Write Enable control lines, an analysis must be performed to determine if the selected operating point is suseptible to degradation. In addition, the microprocessor must only perform word accesses of the buffer.

A1.2 Disk Block

A1.2.1 LD CDR Decode CNT Field Is Forced To 00h While Doing EDSA Headerless

Condition: While the ENHANCEDSA bit (Reg. 5Dh, R/W, bit 0) and the ENBUFCDR bit (Reg. 63h, R/W, bit 1) are both set (performing EDSA using Data Split words from the buffer), the value in the Count Field during the LD CDR decode (SEQCTLC = '001') is ignored and forced to '00h'.

Workaround: The designer must take this into account while creating the Disk Sequencer Map.

A1.2.2 Possible Two Index Time-Out During Normal Disk Operation

Condition: A Two Index Time-Out condition can be encountered in situations where the last EOS pulse of the track is generated before the upcoming Index Mark.

If the Disk Sequencer is started after the last EOS of the track but before the Index Mark, and the target frame is the first frame of the track, the Index Counter will increment but the EOS counter (Reg. 58h, R/W) will not compare equal to the EOS Compare register (Reg. 5Ch, R/W). This prevents the EOSCMPEQ bit (Reg. 5Bh, R, bit 6) from being set. This will cause the Disk Sequencer to wait until it encounters the last EOS pulse again, which will be one revolution later. At this point in time, EOSCMPEQ will be true, allowing the Disk Sequencer to start searching for the requested sector. However, the Index counter will increment to '2' at the next Index Mark and cause a Two Index Time-Out condition.

Workaround: This situation can be avoided by executing a Reset Two Index Timer decode (Primary, SEQCTLB = '11') after the Wait For EOS Compare Equal decode (Alternate, BRSEL = '100') has found the correct frame, but before the Index Mark occurs (typically the next instruction).

A1.3 ECC Block

A1.3.1 Uncorrectable ECC Retry Procedure

Condition: Attempting to perform a read retry operation of a sector which has been found to be uncorrectable could result in an erroneous correction process of that sector if found to be correctable on the read retry operation. This could result in the wrong bytes being modified during the correction process and then passed on to the Host as corrupted data.

Workaround: To ensure proper retry operation, the following procedure should be followed prior to attempting the retry operation.

a. Disable the Correction port and Disk port.

b. Reset the ECC logic by writing 0Bh to register 9Bh.

c. Reset the Disk FIFO and Disk Byte Counter.

d. Re-enable the ECC logic by clearing register 9Bh.

e. Re-enable the Correction port and Disk port.

f. Set the Disk Pointer to the proper boundary.

g. Perform the retry operation.

A1.4 Microprocessor Block

A1.4.1 MA[10] Signal Pin Is Decoded During Register (CS) Accesses

Condition: The addressing range of registers within the AIC-8375 is from 5xh through 2xxh. This address range requires decoding of the MA[9:0] signal pins (for non-multiplexed mode) or the MA[9:8] and the AD[7:0] signal pins (for multiplexed mode). However, the device also decodes MA[10]. The device decoding requires that MA[10] be '0' for all register accesses (using the CS input). If an address range is selected which uses MA[10] = '1', no decode will occur and the intended register will not be written or read.

Workaround: The AIC-8375 register mapping must use MA[10] = '0'.

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