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Microsystems

Volume 4 / Number 11

November 1983

Some Super 16-bit Micros

Bill Wong compares the architectures of the 80286, 68000 and 16032, and highlights their most important features.

Hardware Reviews

Andrew Bender reviews the CompuPro System 8/16, Model 86/87, which gets its speed from the 16-bit 8086 and 8087 math coprocessor.

David Hardy and Kenneth Jackson review a new S-100 board from CompuPro: the CPU-68K processor, supplied with CP/M-68K.

Hardy and Jackson also review a dual-processor desktop computer from Zenith: the Z-100, which uses 8085/8088 CPUs and has S-100 expansion slots.

Super 16-bit micros—architecture and real implementations

Software Reviews

David Dupuy reviews the $29 Nevada Fortran from Ellis Associates.
Robert Minnis contributes some notes on Fortran-80 from Microsoft.

Other Feature Articles

Andrew Bender shows how to break the 64K barrier on a veteran S-100 computer, using a simple extended address memory manager.

Bill Wong concludes his Introduction to Local Area Networks, of which the first part appeared last month.

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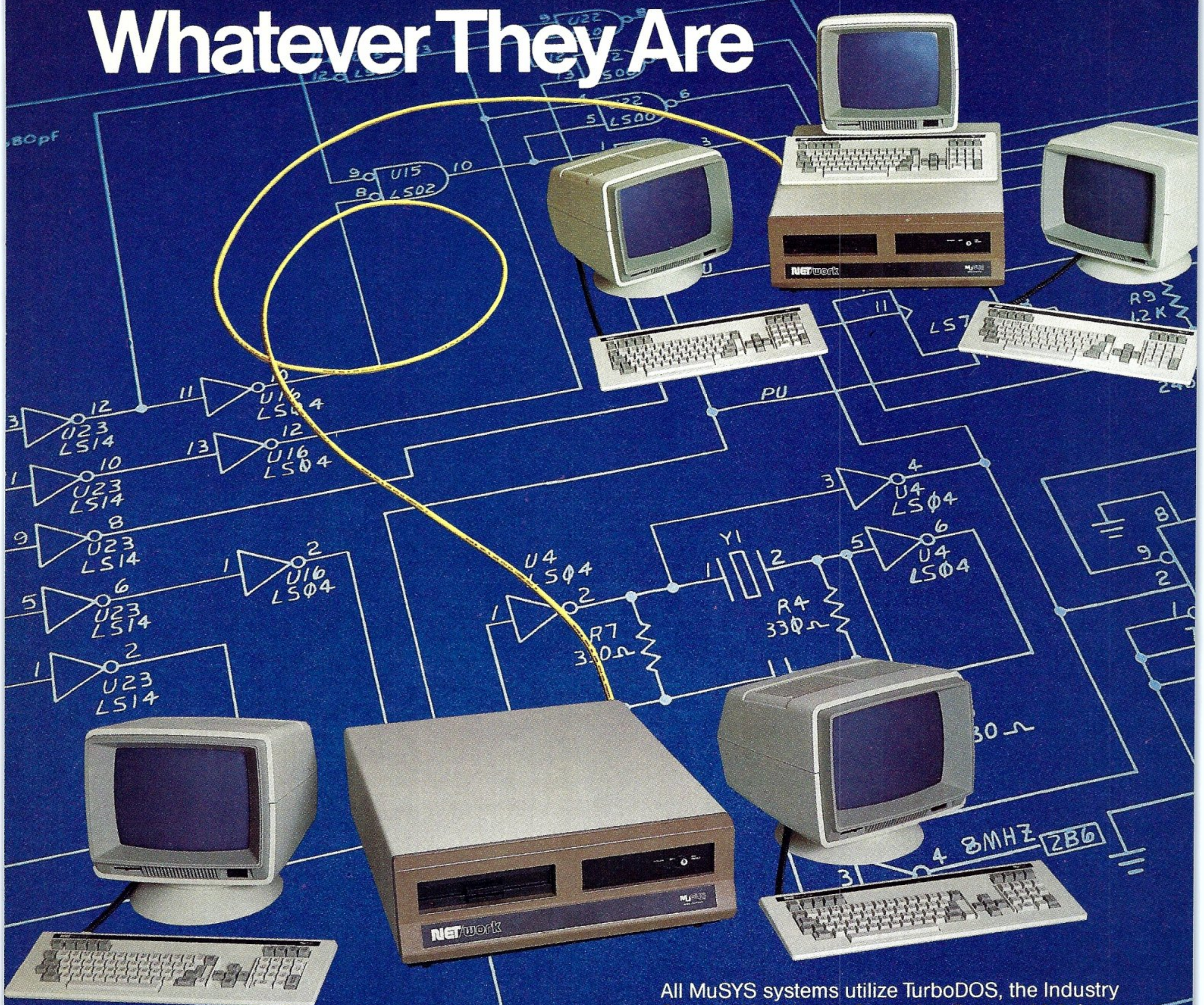

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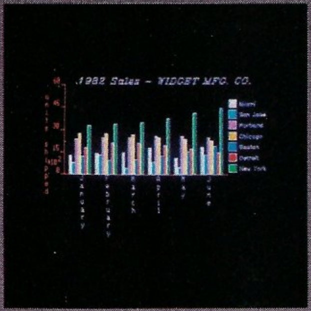

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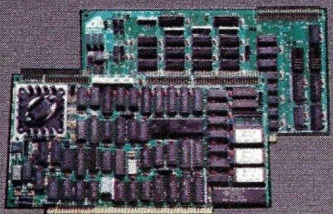

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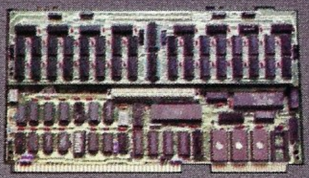

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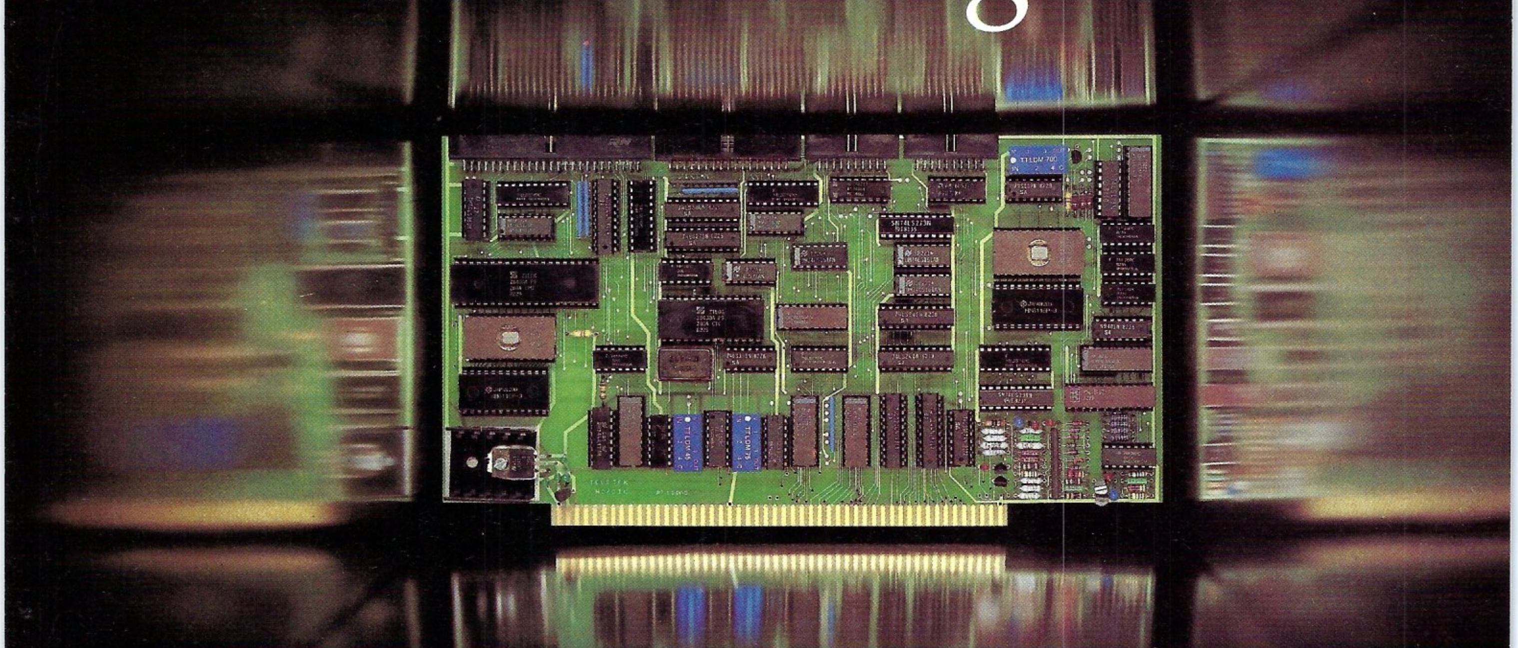

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November 1983

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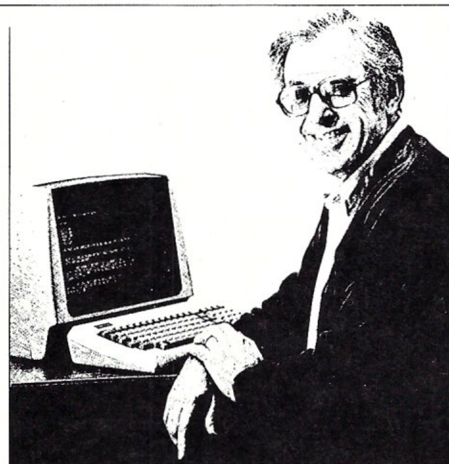
Editor's Page

by Sol Libes

Which is better—an 8-bit or 16-bit microcomputer? That is the current question. I think the answer is still unclear. There is no doubt that the 8-bit systems have some distinct advantages. First of all there is lots of software available for them—particularly the CP/M-80 systems. This will continue to be true in the forseeable future because it takes a substantial period of time to generate a significant software base.

Secondly, the cost of an 8-bit system is always going to be less than that of a 16-bit system. One has only to compare the prices of 16-bit and 8-bit computers running a word processing package such as WordStar. For example, 8-bit machines such as the Morrow Micro Decision and Kaypro currently sell for half the price of 16-bit systems such as the IBM-PC and their look-alikes. This significant price difference appears to be based more on market demand than on the manufacturing cost of the product. A 16-bit system sure doesn't cost twice as much to build as an 8-bit system. Although I expect the price differential between the 8 and 16-bit system to decrease with time, it will always be there.

16-bit systems have two huge advantages over 8-bit systems. First,



they can directly address much more memory, and second, they have larger and more powerful instruction sets. Thus we might expect the 16-bit systems to be more powerful and much faster than the 8-bit systems. However, the 16-bit systems introduced so far have not demonstrated that they are faster than the newer 8-bit systems. In fact, some are slower. The technology to make 16-bit based systems faster than 8-bit systems does not, as yet, appear to be in place. For example, the execution of a program such as WordStar is faster on the current generation of 8-bit processors (e.g., CompuPro 6 MHz Z80-based system) then it is on the IBM-PC, which uses the Intel 8088 16-bit microprocessor. Further, software packages that run very nicely on 64K Z80-based CP/M systems "require" a minimum of 128K to run on a 16-bit system such as the IBM-PC. That is why the new version of IBM-PC now comes with 128K RAM as standard, and the next verson is expected to have 256K RAM as standard.

There is no doubt that the instruction sets of the 16-bit micros are much richer than those of the 8-bit machines. Many are designed to support high-level languages, networking, multiprocessing and multiusers. Thus, as the marketplace moves toward the newer applications, the 16-bit machines will be the preferred systems.

The trend in the current 8-bit market is one of increasing price sensitivity. For example, there are already several CP/M-80 systems with base prices of under $1000. It is already possible to purchase a complete double-drive, 64K-RAM CP/M-80 for well under $1300. I have seen the Osborne 1 system, which now lists for $1295, on sale for under $995. And I expect these prices to drop even further by year-end. CP/M-80 systems for under $500 appear attainable in the very near future.

Editor's Page

continued . . .

The 16-bit area is presently a marketplace with a large variety of chips, which presents a problem for software developers. Software developers in the 8-bit market had it easier . . . . they developed software either for 8080/Z80- or for 6502-based systems that dominated the market. And CP/M-80, which dominated the 8-bit arena, made it easy for software developers to write new software.

The 16-bit market is not clear, and hence we find a company such as Digital Research bringing out versions of CP/M for the 68000, 8086, Z8000 and 16032. And likewise there are versions of Microsoft's Xenix operating system for the 68000, 8086 and Z8000, and there may be an implementation for the 16032.

Thus a portability problem is being created in the 16-bit market, which would tend to limit its growth. DRI and Microsoft are attacking the problem by using the high-level C-language for software development, recognizing that although this leads to less efficient, slower-executing code, it does make transporting software from one system to another easier and faster.

The other problem facing software suppliers in the 16-bit area is the chaos that exists in disk formats, which presents a problem in software distribution. This was not a problem in the early days, because many 8-bit systems used the IBM 8" disk format and adopted it as the standard for software distribution. The 5.25" disk size has not seen a similar trend toward format standardization; however, some vendors have provided programs which allow files to be converted from one format to another.

Errata

CompuPro has notified us that an interrupt-driven I/O is now available for the 8/16C. It was not available to the author at the time the review was written ("Life in the Fast Lane: Three Multiuser Microcomputers," *Microsystems*, September 1983).

In addition, on pages 10 and 133 of the September 1983 issue, CompuPro's address was incorrectly given. The correct address is: CompuPro, 3506 Breakwater Court, Hayward, CA 94545 . We apologize for any inconvenience this may have caused.

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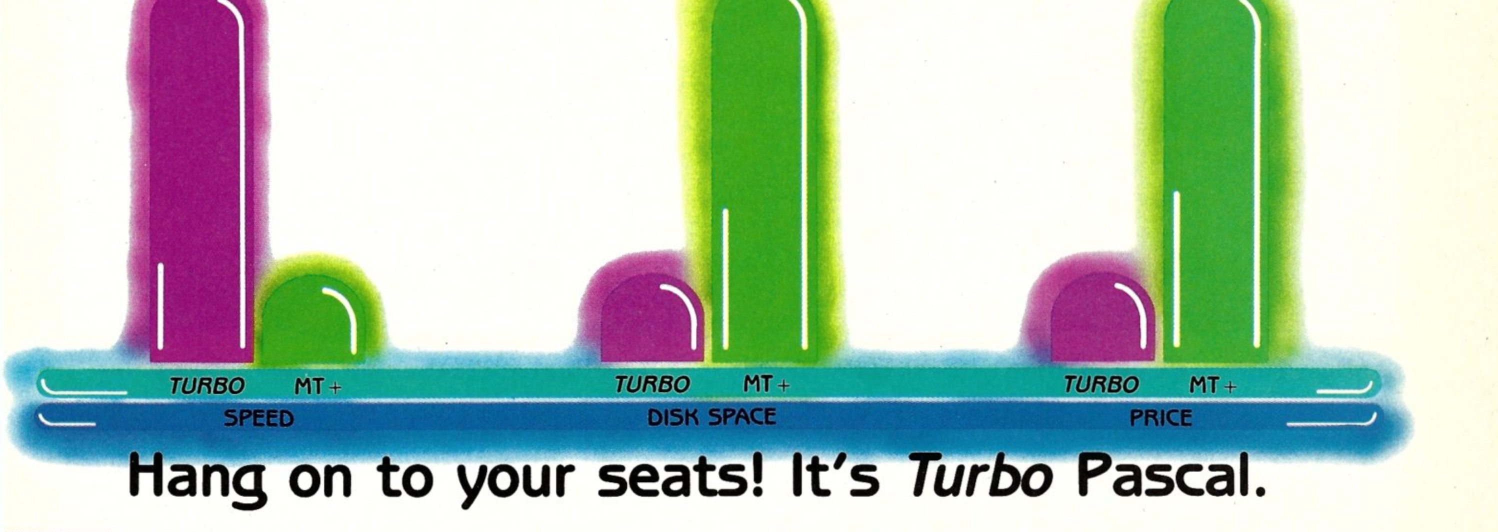

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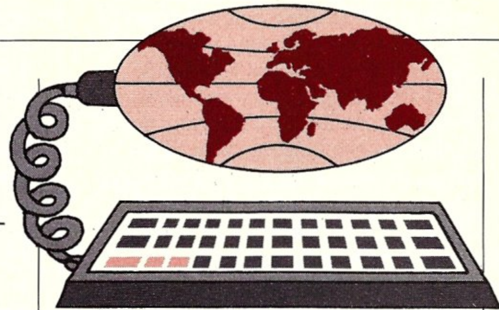
News and Views

by Sol Libes



Random rumors

Western Electric's first desktop microcomputer is expected out before year-end. It is expected to be a UNIX-based system similar to terminals currently available from Teletype and should sell for about $5,000. Look for it to use the Bellmac-32 32-bit microprocessor and contain 256K of RAM. Further down the road from WE is a lower cost desktop unit with videotex capability in the under $2,000 bracket. And there is speculation that a $200 low-end computer will be forthcoming . . . . Digital Equipment Corp. recently reduced the price on their low-end VAX, the 11/730, by 30%, making it the first VAX available for under $20,000. Next DEC is expected to introduce a desktop VAX unit to be designated the 11/610, using a "VAX-on-a-chip-set" and a new high-speed bus.

New SIG/M software

The SIG/M subgroup of the Amateur Computer Group of New Jersey has released 19 new volumes of public domain software. This brings their total to 136 volumes. They have also released a new version of their catalog describing all 136 volumes. The catalog is $2 domestic ($2.50 foreign). Write: SIG/M, Box 97, Iselin NJ 08830. These new volumes will be found on many RCPM systems and can be copied at meetings of many CP/M user groups (see the October *Microsystems* for a directory of these groups).

The contents of the new SIG/M volumes are:

Vol.	Contents
118	XLISP—a Lisp compiler written in C with full source
119	Library Filing/Utility system and BYE program update
120	New version of that old standby MODEM (new version to be known as MODEM9) and Music Composer program for AY38910 sound chip
121	Updates for MODEM7, SMODEM and SD (Super Directory) programs
122	Updates for ZCPR2 for systems with 8080 micros
123	A mixed bag of programs
124	ZCPR2 and SYSLIB updates; ZCPR2 for Osborne-1
125	ZCPR2 and SYSLIB updates including ZCPR2 for Kaypro II and Morrow MD
126	ROFF4 text formatter
127	COMM7 communication program DISK7 file maintenance program and update of SAP
128	Updates of Bulletin board Software
129	dBASE II Order/Inventory program & JRT Pascal routines
130	RCPM Utility subroutines and programs
131	Miscellaneous Pascal/Z programs
132	More Pascal/Z programs
133	Even more Pascal/Z programs
134	Still more Pascal/Z programs
135	Utilities
136	Utilities for Big Board, MODEM for Osborne, Big Board, Datamax, & Sorcerer; YAM for Osborned, Kaypro, & Sanyo

Xenix goes commercial

Until now the Xenix operating system, from Microsoft, was available only to OEMs (original equipment manufacturers). The largest quantity had reportedly been supplied to 25,000 Tandy model 16 owners and about 10,000 Altos system owners. Microsoft has announced that it expects to begin shipping versions of Xenix 3.0 for the IBM-PC to about 100 selected dealers. Microsoft hopes to ship 20,000 copies by year-end and to more than double the number next year.

This version of Xenix reportedly implements UNIX System III and has been upgraded with a menu-based command shell similar to that of the recently updated MS-DOS single-user operating system (we will be doing an in-depth review of MS-DOS in an upcoming issue. Xenix running on the Altos system was reviewed in the September issue). Xenix 3.0 is expected to be able to read and write MS-DOS files. Further, it will have enhanced electronic mail capabilities.

The full package will be 8.5 MB and furnished on 10 160K disks for the PC. The user is expected to transfer the software to his hard disk. Microsoft also plans to offer various books and manuals for users and programmers separately. To make the package more attractive and more compact, Microsoft will also make the system available in separate modules. The text-processing module that includes T-roff, N-roff and the Vi visual shell, will be $395. A software development module is $495. The single-user version will be $395, while the multiuser version will be $695. A plug-in memory management card will be needed as well as I/O cards for the PC.

Apple is expected to sell a similar version of Xenix for the Lisa. IBM decided not to market the product directly, and hence Microsoft is doing their own marketing. Microsoft is also known to be working on porting Xenix to the National Semiconductor 16000 series of micros. Demand for this is seen as low and thus not expected soon. However, Microsoft's European distributor, Logica Ltd., is known to have already ported Xenix to the 16000 and is expected to begin distribution soon.

In the meantime UniPlus+ from UniSoft Systems has been available for the Apple Lisa for several months now. It is being distributed by UniPress Systems, 1164 Raritan Ave., Highland Park, NJ 08904 (201-985-8000). It requires that the Apple Lisa have a second 5 MB hard disk drive since there is not enough room on the drive built into the Lisa, and the Lisa software must be resident. Furthermore, since the Lisa floppy disks are in extremely short supply, UniPress is currently requiring that purchasers send them the drive and they will put UniPlus+ on the drive and check it out. When Lisa floppies become available, they will furnish UniPlus+ on floppies for uploading.

Osborne woes

Rumor is that Osborne stockholders had to give up 50% of their stock last July to obtain $20 million additional financing when the company couldn't meet its bills. The company had rough going when sales of the Osborne 1 dropped severely, and they couldn't ramp up production of the new Executive model fast enough. In the meantime, Osborne has been getting strong competition from Kaypro and Zorba. The latter, made by Telcon, was bought out by Modcomp, a minicomputer builder.

Although Osborne is finally delivering the Executive, one other problem still exists. Osborne promised that the plug-in board to provide IBM-PC compatibility would be available one month after they began delivering the new machine. This is no doubt one of the reasons why people are attracted to the machine. However, they seem to be having trouble delivering this unit.

Osborne closed its New Jersey manufacturing facility and laid off about 100 people, about one 11% of its staff. The company, which pioneered the transportable computer and packaged software concepts, was also the price leader when the original Osborne 1 was introduced. However, their price leadership is now a thing of the past, and many other suppliers are packaging software with their systems today. The transportable versions of the IBM-PC have taken away some business and the soon-to-be-announced transportables from IBM and Apple are expected to make further inroads.

Although Osborne Computer makes good systems, the basic problem appears to be that the marketplace is changing at a very fast clip and OC is just too slow to change. The Executive may prove to be too little too late. After all, the Kaypro can now be had with a 10 MB disk drive, and it had a larger screen and standard ports over a year ago.

Adam Osborne had hoped to make the low-cost Osborne-1 into a standard. However, refusal to make the machine a truly open system made it difficult (but not impossible) for independent vendors to supply software and peripherals for the machine.

Chapter 11 bankruptcy

Since the above was written, Osborne Computer filed for bankruptcy on September 15 under Chapter 11 of the Federal bankruptcy law. If the company is able to obtain emergency financing, it may continue to operate on a reduced scale, but many analysts are doubtful whether the company can survive.

DRI vs. Microsoft

Even though Gary Kildall and Bill Gates say there is no battle, there certainly are all the signs of one. Losing the IBM-PC DOS battle to Microsoft has its pluses for Digital Research. As Gary Kildall said, "If IBM had not given the contract for its operating system, PC DOS, to Microsoft, we would not be as strong as we are today." There is no doubt that DRI is not the complacent outfit that it used to be and that it is learning how to fight.

The decision to release versions of all its software to run directly under MS-DOS was no doubt a very smart move. One no longer has to purchase

News & Views
continued . . .

CP/M to run them on the PC. They learned that if you can't beat 'em, then join 'em! And DRI is now offering an MS-DOS emulator that runs under CP/M-86 so that users can run MS-DOS software.

Now DRI has entered into an agreement with VisiCorp to support the Visi-On system under CP/M-86. Couple Visi-On with the multiprocessing capability of Concurrent CP/M and you have one hell of a powerful system. And in another move, IBM has finally agreed to market concurrent CP/M, packaging it up with a version of WordStar that takes advantage of the concurrency features.

DRI has also disclosed that it will soon release a fully ANSI-77-compatible version of Fortran and will add graphics to its Personal Basic. DRI is also known to be working with Digital Equipment Corp. to develop a smaller version of DEC's VMS operating system, and there is a rumor that DR is planning to enter the ROM-cartridge software market.

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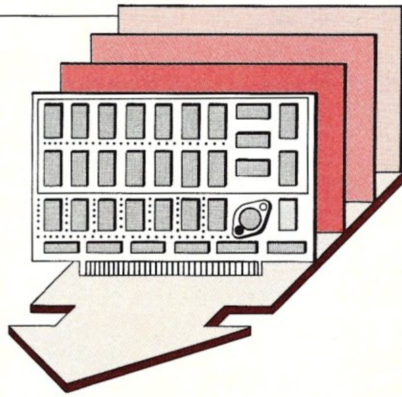
CIRCLE 73 ON READER SERVICE CARD

The S-100 Bus

by Dave Hardy



This column is intended as a forum on S-100 topics. I encourage readers to send in questions about the S-100 bus, which I will attempt to answer. Please write to Dave Hardy, 736 Notre Dame, Grosse Pointe, MI 48203.

In spite of its rather intimidating 100-pin bus, the IEEE-696 (S-100) bus is actually easy to use. Although there are simpler, more straightforward bus structures available (like STD, and those of many manufacturers, like Sanyo, etc.), all are less complete than S-100, and not nearly as versatile.

This month, instead of discussing the IEEE-696 bus definition, I'd like to discuss some simple S-100 I/O interfacing methods. Afterwards, I have some more interesting reader feedback.

Some simple I/O circuits

Most avid S-100 users have two things in common. First, they never have enough memory in their machines (nobody does), and second, they always need just one more serial or parallel I/O port to connect their newest peripheral.

Many S-100 users also have a third thing in common. They don't know how easy it is to add additional I/O to their S-100 machines. The circuits shown in Figures 2 and 3 illustrate some simple "bare-bones" parallel and serial I/O circuits that can be added to any S-100 machine.

Although these circuits perform different interfacing functions (one is a parallel interface, and the other is a serial interface), both demonstrate the basic techniques needed to interface I/O devices to the S-100 bus.

I/O addressing

In order to send data between the peripheral device and the S-100 bus, the interface must monitor several of the S-100 lines to determine when the bus is ready to input or output a piece of data. In addition, the interface must also decide if the data about to be transferred is to be transferred by it, or by some other interface. The interface does this by reading the S-100 bus address lines to see if its own unique I/O port number (or group of port numbers) is being addressed (see Figure 1). This procedure is generally called "address decoding." If the number it reads doesn't match its own address (port) number, then it does nothing. If the number it reads *does* match its own address, then it assumes that the bus might want to talk to it. The address match causes the SELECT* line (shown in Figure 1) to go true (that is, it goes to a logic 0, since SELECT* is a "low true" signal). This enables the rest of the interface, which is shown in Figure 2 (parallel) or Figure 3 (serial).

Notice that address decoder B in Figure 1 does not look at the least significant address line (A0). This is done to allow the decoder to detect more than one address. In this case, decoder B can detect any two consecutive addresses, starting on an even boundary, such as 0 and 1, 4, and 5, 98 and 99, and so on. Decoding only seven of the eight I/O address lines, however, makes it necessary to do further address decoding in other parts of the interface. For example, the 8251 USART shown in Figure 3 decodes address line A0 itself to determine internally whether data transfers are to be to/from its control registers, or its data registers.

Still more decoding

After determining that the I/O address is proper, a few other things still need to be determined by the interface. First, all that the address decoder does is read the address lines and tell the interface when they match. In the S-100 bus, I/O ad-

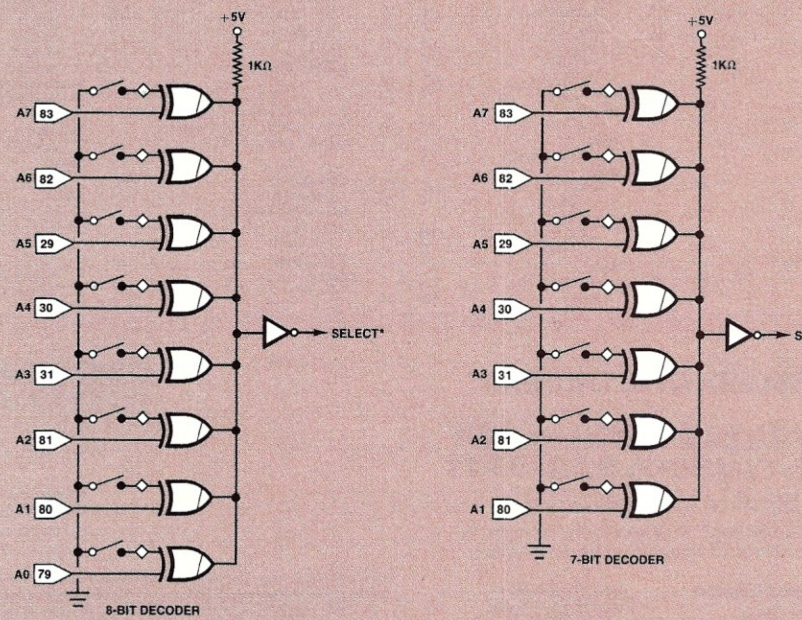


FIGURE 1 - TWO ADDRESS DECODERS.

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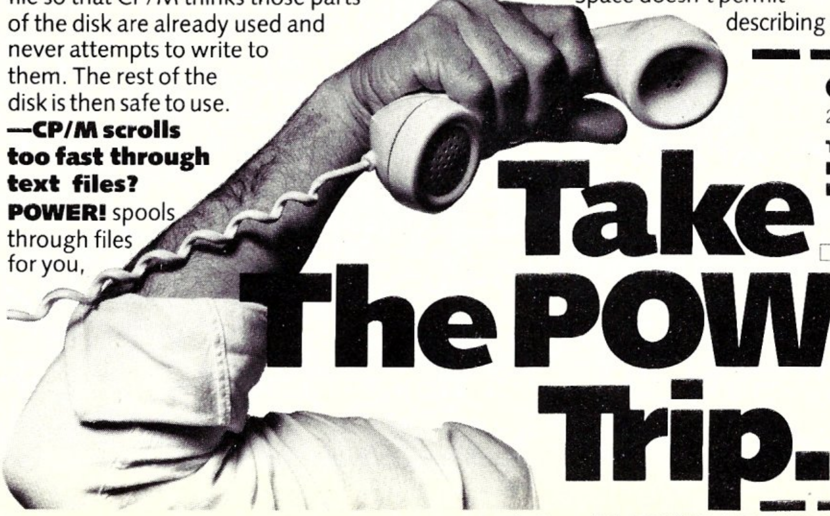

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CIRCLE 14 ON READER SERVICE CARD

dressing *and* memory addressing are *both* done on the same lines, so the next thing that must be determined is whether the address that the decoder is seeing is an I/O address or a memory address. This is done by looking at the sINP and sOUT lines, which indicate if the read or write operation about to take place is an I/O operation or a memory operation.

Once the interface has decided that the bus operation about to take place *is* at its own address, and that it *is* an I/O operation, it then monitors the pWR* (for output) or pDBIN (for input) line to determine exactly when to transfer the data to or from the bus.

The following definitions for the S-100 bus lines that are used here should be of some help in understanding what is happening in the examples given:

pDBIN (processor Data Bus IN) pin 78, active high:

A generalized read strobe, asserted for memory read, I/O read, and interrupt acknowledge cycles. Used to enable a slave's data output bus drivers to gate data onto the S-100 bus.

pWR* (processor WRite) pin 77, active low:

A generalized write strobe, asserted for memory and I/O write cycles. Indicates to slave that the data output bus contains valid data.

sINP (status INPut) pin 46, active high:

Active when S-100 bus is executing an input cycle and reading from an I/O port address.

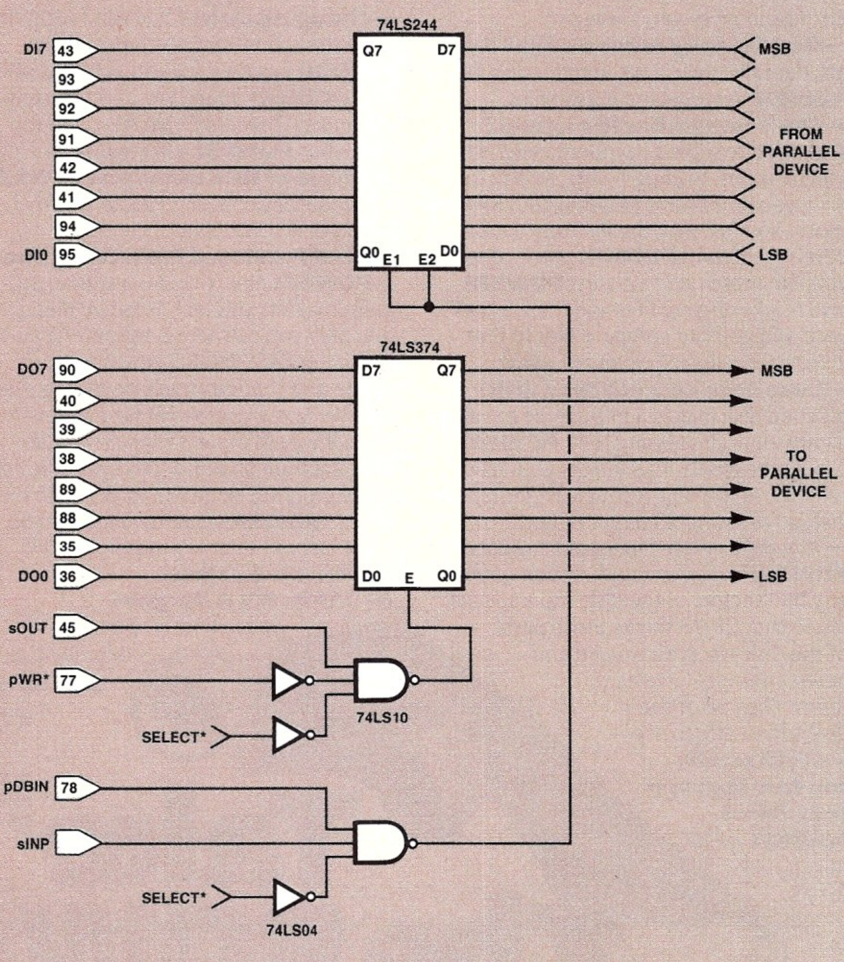


FIGURE 2 - A SIMPLE PARALLEL I/O PORT

sOUT (status OUTput) pin 45, active high:
Active when S-100 bus is executing an output cycle and writing data to an I/O port address.

Although these definitions are not complete, and are not strictly in agreement with the IEEE-696 standard, they should be adequate for most simple S-100 interfacing projects.

Reader feedback

IEEE-696 compliance: I've received a number of letters from readers mentioning that many S-100 boards that are advertised as "IEEE-696 compatible" are actually not, because they lack 24-bit addressing or 16-bit I/O capability. The IEEE-696 standard actually says only that a bus master must assert at least 16 address bits, but *may* assert 24 address bits *if* extended address capability is desired. Furthermore, the IEEE-696-defined data bus consists of 16 lines grouped as two unidirectional 8-bit buses for byte operations, and as a single bidirectional bus for 16-bit word operations. If an S-100 master contains only an 8-bit processor, 24-bit addressing is useless without additional memory management devices, and word operations are just not possible. In other words, an S-100 board doesn't have to include every single feature of the IEEE-696 standard to be considered "IEEE-696 compatible," although I agree that some manufacturers may be stretching the truth a bit when they claim complete compatibility.

Mysterious missing interrupts: Several readers have written mentioning that many interrupt-generating circuits (such as the one presented in the first "S-100 Bus" back in September 1982) don't work reliably. This is particularly true of the 8253-based circuit that I use myself. I had the same problem when I tried to install MP/M on my own S-100

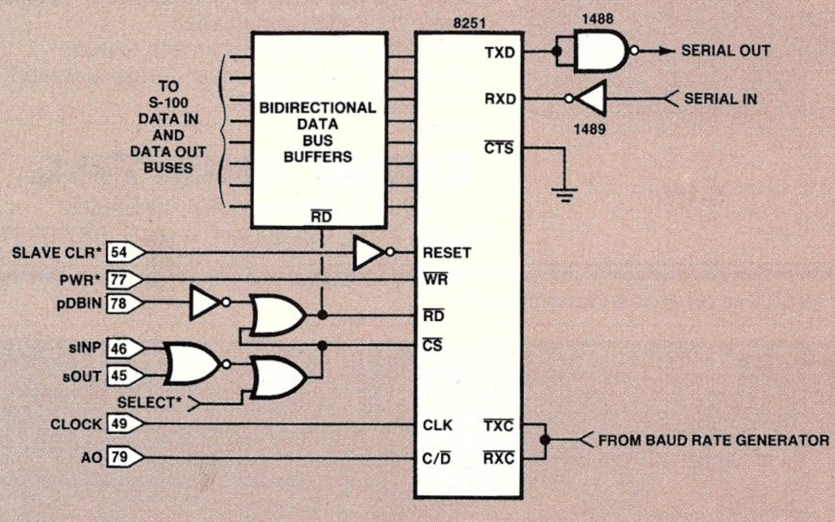


FIGURE 3 - A SIMPLIFIED SERIAL I/O INTERFACE

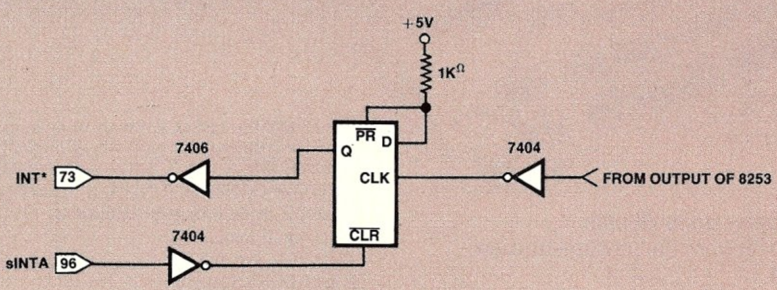


FIGURE 4 - "PULSE STRETCHER" INTERRUPT FIX CIRCUIT

system. Although the 8253 was generating interrupts 60 times each second, the system was only being interrupted about 10 times each second, and not at regular intervals. The problem turned out to be that the pulse generated by the 8253 was just a bit too narrow for the processor to reliably see it. The circuit in Figure 4 is a "pulse stretcher" flip-flop that latches the INT* (interrupt) signal each time an interrupt pulse is generated, until the processor acknowledges the interrupt by returning sINTA (status INTerrupt Acknowledge). I've been using this "fix" in my system for several months now without any problems.

North Star S-100 bus pinout differences: A few months ago, I received a note from Dave Kozinn (one of the SYSOPs of CompuServe's CP/M Interest Group) along with a list of the North Star CPU board's S-100 pin assignments. He mentioned that he would like to see a comparison of the North Star S-100 bus pinout and the IEEE-696 bus pinout. I've made the comparison, and they are quite different. If enough interest is shown, I will list the differences in a future "S-100 Bus"; otherwise, I will make the list available on the RCPM network and CompuServe. Basically, the differences are what would be expected, including the many redefined IEEE-696 lines such as address lines 16-23, the deletion of the old front-panel lines, etc.

Next time, we'll have a discussion of S-100 wait states.

The UNIX File

The UNIX File looks at many aspects of the UNIX operating system. If you have comments or questions about UNIX or this column, feel free to write to me, at the University of Toronto Computing Services (UTCS), 255 Huron Street, Toronto, Ontario, Canada M5S 1A1. If you're on the UNIX network "USENET", you can contact me at "utcsstat!ian".

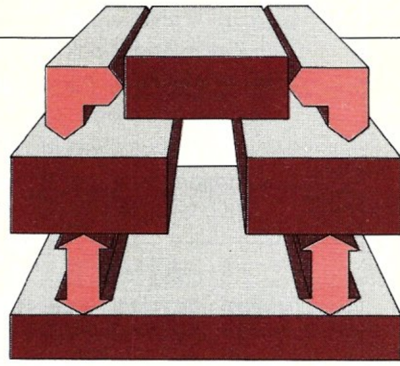
This month's column looks at the USENIX Conference in Toronto, tackles the myth that there is no software for UNIX, and looks at another introductory book on UNIX.

The USENIX Conference—Toronto, July 1983

The conference was great! I came away with about seven pages of typewritten notes, just on the sessions I attended. There's no way I can condense all that to fit this column, and most of the talks will be in the proceedings anyway, so I'll just hit some of the highlights. The next USENIX Conferences will be January 17-20, 1984, in Washington, D.C., and June 12-15 in Salt Lake City. Circle those dates now if you want to be plugged into the mainstream of UNIX activity.

Western Electric started by announcing that the 'S' statistical package was now available for licensing, at a cost of \$8000. This is the commercial user price, per CPU(!). What they did not mention was that the previous, use-only nonlicense price had been \$150, and that they had jumped the price from \$150 to \$8000 with *no change in support* (i.e., none to begin with, and none now) and apparently no change in the software. The educational-only price goes up to \$400 per CPU.

Another package, the Writer's Workbench, was finally announced at a price of \$4000. And a product called the Instructional Workbench was announced at \$2500 in binary-only form. The others, and most all UNIX software products, have come in source form. *Western Electric*



seems to back the trend to binary-only distribution of UNIX software. This trend is resisted by the technical people but encouraged by some of the three-piece-suit crowd. Western as usual gave the figures on UNIX source licenses (currently 5,523 total) but refused to comment on the number of binary sublicenses that have been issued. Perhaps they don't know. The speaker said that the "figures floating around in the press, which range from 3,000 to 300,000, are very good numbers."

Focusing on the philosophy of computer usage and programming, Mike Lesk and Rob Pike gave excellent talks. Lesk discussed an experiment run in the technical library at Bell Labs, Murray Hill, on keyword searching vs. menu searching, and another (using the AP Wire) comparing menu searching against a user-provided keyword profile. Lesk concluded that keyword searching is more effective than menu searching for most applications, and that "novice modes" are not a very good idea. If the effort spent on "novice modes" in software were spent instead on better training for users, the computer would be a more effective tool. Pike spoke out strongly against the current habit of coding a solution without identifying the problem to be solved, and pointed out some examples from current Berkeley and Bell versions of UNIX.

This talk engendered considerable discussion, as did a later panel on "The Future of UNIX." The founders of UNIX were at the conference, and Dennis Ritchie sat on this panel. Ritchie commented that in the past, Bell and Berkeley had seemed to be going in different directions, but that now they were at least talking to one another.

There were many technical talks on compilers, new implementations of UNIX, and a few comparing the newest systems (4.nBSD vs. Bell 3/5), several good papers on user interfaces (including speech input), and many, many other topics.

And then there were the social activities. Most of the major vendors had hospitality suites. Fortune Systems, not to be outdone, booked the Ontario Place Cinesphere theatre for a marathon of IMAX™ movies. The dedicated UNIX fans arrived after the Ontario Place shut down at 10 PM, and most were still gazing at the silver screen when the final flick flew by just before 3 AM. A few actually made it to the first technical session at 8 AM the next morning.

There was a lot of activity in the vendor area. UniSoft, celebrating their fiftieth port of UNIX to an OEM configuration, were demonstrating one of their ports of System 5 to the 68000. Others were exhibiting ports based on System 5, System 3, various Berkeley implementations, and the older but cleaner version 7. Hardware shown included Gould's micro, several 68000 machines, a few 16032 machines, and others. Shown for possibly the first time was the Teletype 5620, based on a Rob Pike design called the BLIT. The 5620 can run a small number of sessions (six) simultaneously through use of windowing à la Smalltalk, Apple LISA, etc. The sessions can be producing either text or graphical images, or both. All outputs are sent to the screen as they arrive from the host.

There's a lot more I could talk about. If you have questions about anything that went on, please feel free to write to me. Or better yet, make plans to attend one or both of next year's USENIX conferences.

Who says there's no software for UNIX?

I frequently hear an argument that goes something like "Well, UNIX may be a good operating system, but there's no commercially available software for it." Here's my attempt to counter this scandalous misrepresentation of fact.

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CIRCLE 87 ON READER SERVICE CARD

Urban Software has a UNIX software survey that contains *several pages of small print* listing software available for UNIX. The software listing comes as a sample database with their "Leverage" list management package, and is also included in hardcopy in the current issue of their *Urban Software Newsletter.* The list includes word processing packages, accounting systems, menu generators, compilers for most languages, databases, spreadsheets, and other goodies. Dozens of suppliers are listed. And the list is not yet complete—they will be updating it periodically. Urban Software, 330 West 42nd Street, New York, NY 10036. Or call (212) 736-4030.

Another source of software is UniPress Software, Inc. This outfit seems to be trying to do for UNIX what Lifeboat did for CP/M, that is, make available a variety of software from a range of software manufacturers in the common distribution formats for the variety of small UNIX systems available. They sell screen editors, word processors, and a (growing) number of other software packages. Write to UniPress at 1164 Raritan Avenue, Highland Park NJ 08904, or call (201) 985-8000.

In addition, there is a large body of public domain software available to UNIX users. Much of it is available through the UNIX network "USENET." I will have more to say about this in a later column.

Low-cost C program source

Although this is not just for UNIX, but for anyone with a C compiler, here's a company that supplies inexpensive C source programs. William Hutchison, Jr., of Algorithmic Technology sent me a catalog of software tools/utilities which range in price from $0.10 (ten cents!) up to $100. A dime (plus $5 for a diskette) will fetch you object code (in CP/M format) for various public domain or copyrighted but freely distributed programs; the source for some of these is 25 or 50 cents. Most of the programs from the *Software Tools* books are here, recoded in the C language. The most expensive is an elaborate Sort program, at $100. The smaller ones such as **grep, include, archive** sell for about a dollar each. The size of each file is given, and you add them up to find out how many diskettes you need to order. It all sounds good. I haven't seen any of the source code, and they only come on various 5" floppy formats. To get a copy of the catalog, write to Algorithmic at P.O. Box 278, Exton, PA 19341-0278. If you're on Compuserve or The Source, mail to [70665,1307] or TCT586 respectively.

A user-friendly book?

I am always sceptical when I see or hear the words "user-friendly." This phrase has been so over-used that it no longer retains an accurate meaning. It seems to be used to refer mostly to programs designed for someone with an IQ of 43 or below, which have rigid user interfaces that you can't speed up when you get tired of them, and which come with documentation that treats you like a moron. Perhaps I exaggerate, but only slightly. A recent article in *Byte* magazine claimed that a hinged keyboard contributes to the 'user-

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Bring the flavor of Unix to your Z80 CP/M system with Unica

"Unicum: a thing unique in its kind, especially an example of writing. Unica: the plural of unicum."

The Unica: a unique collection of programs supporting many features of the Unix operating system never before available under CP/M. The Unica are more than software tools; they are finely crafted instruments of surgical quality. Some of the Unica are:

bc	-	binary file compare, display differences in hex
cat	-	catenate files (vertically)
cp	-	copy one or more files, even between users
dm	-	disk mapper, reports free blocks and directory space
fid	-	file identification by unique numbers (CRC's)
hc	-	horizontal file catenation and column permutation
ln	-	create file links (multiple names for one file)
ls	-	intelligent directory lister, optional multi-columns
mv	-	move (rename) files, even between users
rm	-	remove (delete) files, with optional verification
sc	-	source file compare, with resynchronization
sfa	-	set/reset file attributes, optional verification
sp	-	spelling error corrector, with 80,000 word dictionary
sr	-	search multiple files for a pattern
srt	-	in-memory file sorter, optional duplicate line omission
tee	-	pipe fitting (copy input stream to multiple outputs)
tr	-	transliterate (translate character codes)
wc	-	word counter, counts characters, words, and lines
wx	-	word extractor, copies each word to a separate line

Each Unicum understands several flags ("options" or "switches") which control program alternatives. No special "shell" is needed; Unica commands are typed to the standard CP/M command interpreter. The Unica package supports several Unix-like facilities, such as filename user numbers:

sc data.bas;2 data.bas;3

(compares files belonging to user 2 and user 3);
Wildcard patterns:

rm -v *tmp*

(types each filename containing the letters TMP and asks whether to delete the file);
I/O redirection:

ls -a >proj.dir

(writes a directory listing of all files to file "proj.dir");
Pipes:

dm b: | sr free >lst:

(creates a map of disk B:, extracts those lines in the map which contain the word "free", and prints them on the listing device).

The Unica are written in XM-80, a low level language which combines rigorously checked procedure definition and invocation with the versatility of Z80 assembly language. XM-80 includes a language translator which turns XM-80 programs into source code for MACRO-80, the industry standard assembler from Microsoft. It also includes a MACRO-80 object library with over forty "software components", subroutine packages which are called to perform services such as piping, wildcard matching, output formatting, and device-independent I/O with buffers of any size from 1 to 64k bytes.

The source code for each Unicum main program (but not for the software component library) is provided. With the Unica and XM-80, you can customize each utility to your installation, and write your own applications quickly and efficiently. Programs which you write using XM-80 components are not subject to any licensing fee.

Extensive documentation includes tutorials, reference manuals, individual spec sheets for each component, and thorough descriptions of each Unicum.

Update policy: each Unica owner is informed when new Unica or components become available. At any time, and as often as you like, you can return the distribution disk with a $10 handling fee and get the current versions of the Unica and XM-80, with documentation for all new or changed software.

The Unica and XM-80 (which requires MACRO-80) are priced at $195, or $25 for the documentation. The Unica alone are supplied as *.COM executable files and are priced at $95 for the set, or $15 for the documentation. Software is distributed only on 8" floppy disks for Z80 CP/M version 2 systems. All orders must be paid in advance; no COD's or purchase orders, please. Quantity discounts are available. Shipment outside of the US or Canada costs an additional $20. Bank checks must be in US funds drawn on a US bank.

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friendliness' of the machine.

And now there is a "User Friendly Guide to the UNIX Operating System." I am not exaggerating here. That is exactly how the book *UNIX Primer Plus* by Mitchell Waite, Donald Martin and Stephen Prata bills itself. It says so right on the cover. So I expected the worst when I started reading. Fortunately, I didn't get it. But neither did I find the ultimate introduction to UNIX. I did find a reference card to the UNIX commands, the designer of which thinks that people need a diagram and instructions on how to fold up a simple reference card! If you can't fold a reference card without instructions, then perhaps even this book will be too complex for you.

What you do get with this book is an attempt to introduce the UNIX system to somebody who has never held a keyboard in his life. Now, the book is not written by acknowledged experts on UNIX. But it is not written by nonprogrammers, either. The authors are experts with the CP/M system (and authors of various books on CP/M), and seem to have written this book as an exercise in learning UNIX. "We began learning UNIX through a trial-and-error approach that brought us a lot of surprises, some of them pleasant," they tell us. "Then we tried to pass on the benefit of our labors" by teaching others, and wound up writing a book about the system. So the authors can be forgiven for not including many of the advanced features of UNIX, since these have probably not come to their attention yet.

The book does give a general overview of the kinds of things that UNIX can do and is used for. Coverage of the basic command set is included. Both the **ed** line editor and the **vi** editor from Berkeley are covered. There is (not surprisingly in a book for nonprogrammers) little information on programming UNIX either at the shell script level or at the C language level; a simple interactive "hello" program is given in C, and information is given on invoking some other compilers (Pascal, Fortran) and on some other languages available. A comparison of CP/M and UNIX suffers from the authors' lack of familiarity with the UNIX universe, and includes the typical assumption that there is a dearth of "real" software for UNIX, a point I have already touched upon.

What I really wonder is this: Why write a detailed book on the system without teaching people how to program it? Many people don't want to write computer programs, they want to use them. Nothing wrong with that. I shouldn't have to build a car before I can drive to work. Most of these people will likely be locked into full-screen, menu-driven "user-friendly" software packages; many won't even see the underlying UNIX. Why do these people need to know about **cat**, and **ls**, and **wc**? If they aren't going to use UNIX at the UNIX level, these commands may well have no more interest to them than the throttle or instruments of a train they're riding on. On the other hand, if they're going to use UNIX as UNIX, then why not treat them as consenting adults, and show them the details of programming and the advanced features?

It seems to me that this book falls

UNIX continued . . .

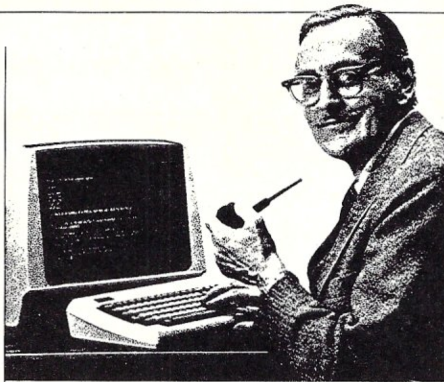
into a middle ground between two different marketplaces. If you want a book that gives nonprogrammers some information about the system, and holds back anything that might confuse them, then this is the book for you. The authors clearly love the system, and their enthusiasm will help carry nontechnical people along despite a few irrelevant cartoons and a few minor errors. For programmers, this book will be found wanting in detail, and I suggest the Bourne book as a more technical introduction to the system. The Lamuto book (*A UNIX Primer*, Ann and Nico Lamuto, Prentice-Hall) is of interest to nonprogrammers. Read what I said about it and the other books in the previous columns (*Microsystems*, July 1983), and decide for yourself. The Waite book is for some, but not for everybody.

The opinions expressed in this column are those of the author, and not necessarily those of the University of Toronto or UTCS.

In the Public Domain

by Chris Terry

This month I'll be talking about hardware diagnostic programs. The public domain libraries contain very few diagnostics of this kind, perhaps because memory is about the only internal component for which one can set up a generalized program. Thus, I have found only one CPU diagnostic, one terminal test, three memory tests, and a program that surveys the current system and describes it.



CPU diagnostic

The CPU diagnostic (CPUDIAG, SIG/M Vol. 5) is a comprehensive hardware test of an 8080 or 8085 chip. It was contributed for noncommercial uses by Kelly Smith. The documentation is brief, but extensive comments in the source code are helpful in understanding what is being done. The program tests branch instructions of all types, register-to-register transfers, arithmetic and logical instructions, and load/store instructions. If an error is detected at any time, the test aborts with the message "CPU HAS FAILED!" and the address of the error exit is displayed. This diagnostic was intended to reside in ROM for system diagnostic purposes; the version supplied here runs as a CPM .COM file with BDOS calls for console I/O.

The ability to run the test at all presupposes that most functions are operating correctly. It can therefore serve as a positive assurance that the CPU chip is working properly, and this itself helps to eliminate some causes of trouble. It has also helped me to find a chip that was failing to set the Z flag after decrementing the B register from 1 to 0. However, diagnosis of a failing branch or I/O instruction would require a more elaborate program that could be loaded and monitored by an external processor rather than by the device under test.

Memory diagnostics

Memory diagnostics seem no longer to be as necessary as they once were. Chip reliability has increased enormously since the days of the old 2102, possibly because lower power consumption means less heat to be removed. Still, memory faults do occasionally happen, and then you need a good memory test.

In deciding what constitutes a good memory test, a number of trade-offs have to be considered. The first of these is speed vs. resolution. A simple test for "sticky" bits in some location can run fast and requires little code. Such a test might consist of filling the area under test with zeros, checking every location, and then filling with OFFH and checking again. This would find only very gross faults. A refinement is to walk a 0 through a field of 1s in each location and then a 1 through a field of 0s; this will detect chips in which data lines are open or tied. A yet further refinement that will generally detect pattern-sensitive chips is to write and read all data combinations possible (i.e., 00 through FF for an 8-bit memory) to every location. This takes considerably longer to do, and modern chips seem to be less pattern-sensitive than the older ones. My experience has been that individual bits either work or they don't, in which case such faults are found by the "walking bit" test, whereas 2102s often had (or developed) marginally operating operational bits.

The real difficulty comes when address lines, either on the bus or within a particular chip, are open or tied. Under these conditions, some locations never get accessed, or get accessed by two different addresses. To find this kind of trouble, the test must fill the test area with a known pattern, write a new pattern to the current location under test, and then check all other locations to see that they were not affected by the new pattern in the location under test. The time required increases as the square of the number of locations being tested, and may amount to as much as 60 minutes for 4K. The basic principle of such tests is simple, but it is not easy to design the coding to pinpoint which chip is defective and the exact nature of the fault.

MEMTEST (CPMUG Vol. 1) is a fairly simple test adapted from the Intel User's Group Library.

MEMDIAG (SIG/M Vol. 5) is an elaborate diagnostic that allows the user to select any block of memory above 1000H; the program itself requires the space below that address. The program tests 4K at a time, using any or all of the following tests:

- Galloping patterns
- Galloping columns
- Walking patterns
- Random patterns
- Write saturation (detects slow sense amplifier recovery)
- Static cycle check (detects data retention errors)

Error reporting is good, and the user has the option to run any or all of the tests continuously, accumulated error counts of various types being sent to the LST: device. This is probably one of the best memory diagnostics available from any source.

WORM8/8 (SIG/M Vol. 17) is a specialized test designed to show up memory failures that occur because the Z80's access window is significantly shorter during an instruction fetch cycle than during a normal memory read cycle.

This program, first published by Henry Melton in *Personal Computing* (July 1979), was adapted to run under CP/M by Jim Eccleston. The Worm consists of a short 12-byte routine that breaks away from the main body and crawls up through the memory space, reporting its location as it goes. This routine also includes an RST 7 instruction as a trap which, if the program counter gets out of sync, attempts to return control to the error-reporting routines. When the Worm reaches ROM or the bottom of the BDOS, the system will be rebooted. This program is useful for the occasions when your memory test reports perfect memory, but you can't run a program.

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Disk Maker I, with S-100 controller board, 1-48 tpi DSDD 5¼" disk drive, dual drive cabinet and power supply, cables and Disk Maker software is $1500.00 (plus shipping). Please notice: There is no per format charge. All formats currently available are provided at no extra charge and future software updates are only $25.00.

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Letters to the Editor

Dear Mr. Libes,

I was glad to see the article by Ian F. Darwin on C programming ("The 50-Line Text Formatter," August 1983). I'm getting Small C now to try to learn the language myself, and the example was a good dry run for me. I will try to use it when I get my C.

However, Mr. Darwin may have been hasty in concluding that he needed to write it. ED certainly has its shortcomings—more of them than even WordStar. Nobody who has WordStar uses ED (except for everybody I know). ED is not a word processor. When I got WordStar I had Smartkey, written by FBN Software. It lets you substitue a string for any character on your keyboard. I used to put these strings in it:

```
sALAZ AZ
m59cs AZALAZ
-8t9t5zOtt5zOt
```

I used to use the first two macros to right-justify as follows:

1. Put myself at the head of a paragraph.
2. Use the T command to see how many lines the paragraph had.
3. Put that number, minus one, before the S macro that I had in Smartkey.
4. Tap zero to put myself at the start of the very long line that I had just created, and to look at it.
5. Put that same number (no, not the zero) at the start of the M macro.

Of course, I did "h n Op" before that, in order to save the text in case of booboos. H saves the text, N brings it back to ED, and Op shows it. That seems like lost of keystrokes, but it's faster than waiting for WordStar. Here is what the commands in the macros mean:

```
s        Substitute
AL       End of line marker
         (line feed, carriage
         return)
AZ       Terminate this part
         of the command
(space)  Put a space here in
         place of the
         end-of-line

m        Do all of this as a
         macro
59c      Go ahead 59 characters
s        Substitute
(space)  Get rid of the first
         space you see
```


```
AZ       Terminate this part
         of the command
AL       Put in an
         end-of-line
```

I used the -8t9t . . . . macro to show where I was on the page. It does it all in one keystroke, and it does it right now. Here's what the -8t9t . . . . macro does:

```
-8t   show 8 lines above
9t    show 9 lines below
5z    pause 5 periods of time
      (about a second)
Ott   show all of the line
      we're on
5z    pause 5 periods of time
Ot    show this line to the
      left of where we are
```

Why do some people still use ED sometimes?

- It doesn't put any loony, non-ASCII characters into your text
- You can print as many lines as you like wherever and whenever you want to—fast. And you do can do it from right where you are in ED.
- Everything about it is fast: getting in, doing simple processing, getting out, etc. I'll bet that ED is the fastest, in execution time, there is.
- You can do as many commands as you like before you tap carriage return to execute them—more speed.

I used ED to type this letter just to show everybody that I can still do it, and it was torture. WordStar has spoiled me. But ED is still the best for nonletter work. And if it were not for characters in which WordStar sets the 8th bit, you could even use it to correct WordStar files.

Dean Dwyer
1103 Cota St.
Torrance, CA 90501

Dear Mr. Libes,

I just finished reading the article by Jim Gilbreath in the August '83 issue on updating WordMaster. The information prompted me to write for some help on getting a useful date out of MP/M and TurboDOS function calls for time and date.

The problem is that the MP/M "standard" for sending and receiving the date is to treat the current date as an integer equal to the number of days since December 31, 1977. I have never seen any simple assembly code that allows a program to change a "human readable" date like July 19, 1983 into a number usable by the MP/M standard. I have no idea why this method of date storage was used, and it would be a real help to programmers everywhere if *Microsystems* could publish some code to perform the date translation. In fact, a standard format to input and output dates is not a bad idea.

As you may know, TurboDOS (a networking CP/M-80 replacement) supports most of the MP/M 2.0 and CP/M 3.0 function calls, including the date functions. There are several utilities provided with Turbo that manipulate the date, so I know it is humanly possible to do so. The problem is that I have never found any easy source code (hopefully in assembly language) that allows a mere mortal to use the date functions as part of other programs. This may be why there is a complete absence of time and date support in all the CP.M languages that operate under MP/M (and Turbo).

I hope you have the answer or have access to someone who can provide the needed code. Computers have reached a level of sophistication that is amazing even to those of us who build them, and it is a shame that the machines cannot easily tell us what the date is.

Arthur M. Zatarain
Principal Engineer
Dataran Corporation
808 N. Causeway Blvd.
Metairie, LA 70001

Dear Mr. Ashdown,

Many, many thanks for your XERA, as listed in the August 1983 *Microsystems*. Since I am a Pascal programmer (but not an assembly language programmer) and am stuck with CP/M (I purchased a Vector 4/30), your program was a godsend. Being naturally finger lazy, I named the program D (for delete) and now find computer housekeeping not

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only anxiety free but enjoyable.

Have you a similar fix for PIP (a Y/N option for, say, PIP A:=B:*.COM)?

For all of us out here, again many thanks for turning a chore fraught with peril into a task laced with pleasure.

George R. Chamberlin
73 Hillside Avenue
Englewood, N.J. 07631

Dear Mr. Terry,

I've been a bit behind on my reading, so it was yesterday that I was scanning through *Microsystems* while eating at my neighborhood Chinese restaurant. I was delighted to see your review of my program, DIMS (May 1983, p. 132).

I'd like to point out that another thing that makes DIMS unique, besides the continuous automatic backup, is the storage method. Fields are of random length within fixed-length records. This is a compromise straddling between the present commercial programs. In dBASE, for example, all fields are fixed-length, and all the unused space is saved. My local address file of 645 records takes 136K in dBASE, 84K in DIMS, and 56K as a comma-delimited sequential file (using quotes only when necessary). This is with 4K blocking on my Morrow hard disk. dBASE searches records at least three times faster than DIMS at its fastest (find).

Two more features not in dBASE: data in any field may be carried from the previous entry by entering ";" and RETURN. Scrolling screen formats may be set up—the industry is stuck on "one record at a time" displays right now, but these are ergonomically inferior to a scrolling entry display that shows context and helps you keep your place.

There are a couple of known bugs. I'm enclosing the notice that upgrades to version 1.02; I don't know whether the SIG/M release includes these fixes or not, or even if it includes all the files in the system. I have also done some minor debugging in the display of nonscrolling forms recently.

There is a bug in the DSORT.BAS program. Do not use descending-order sorts. It is data-dependent; descending-order sorts crash sometimes in line 2730 or 2750 when HI=−1; I don't know how to fix it. A minor bug in the sort program is the way it concatenates fields to make the key; i.e., DUGANDAN. This will sort George Duganasi ahead of Dan Dugan. I think it would be better if the program inserted a high-ASCII character like 126 into the key when concatenating.

You *can* display and enter fields in any order in a designed format; guess my documentation obscured that. See the array SQ ( ) in FORFORM.DWS, which determines what fields to use and their sequence. It is also possible to omit a field in either the screen or printer form independently by entering a negative number in either FL( ) or LFL( ) respectively.

I was pleased to get feedback from the Yankee Osborne Users Group, who have converted DIMS for the Osborne; contact Martin Lewis Jr., 100 Hartford Rd., Simsbury, CT

06070. DIMS isn't very useful on a single-density Osborne because of the size of the program and the storage limitation. I've thought about fixing a version that doesn't use backup for the Osborne, but can't give it a high enough priority to get done here. Hope someone else does.

I am presently (in my spare time, I'm a free-lance sound consultant) writing a structured DBMS for the Radio Shack Model 100.

Dan Dugan

Update to version 1.01

(October 17, 1982)
To: All users of DIMS version 1.0
Bug fix in "select" command. Whenever the question "Do you want to select records to exclude" is answered "y," the first exclusion specification will not be cleared, and will remain in effect in all subsequent selections until the program is restarted from Basic. This results in skipping wanted records in later operations. The fix is just one character in one line in "DEDIT.BAS:"

Old line:

```
7660  IF A$<>"y" THEN
      SKIPWORD$(1)="":RETURN
```

Replace with new line:

```
7660  IF A$<>"y" THEN
      SKIPWORD$(0)="":RETURN
```

Sorry for the trouble. Since the "SETSEARCH" subroutine only happens in DEDIT, fixing this line will fix the whole system. Implementing this fix updates DIMS to version 1.01.

Update to version 1.02

Enhancement to allow selecting records with a blank field. This improvement requires changing code not only in DEDIT but also in all the transient programs that use record selection. The cost of this change is a 3.5% decrease in record selection speed and a very small increase in program size.

When the "select" command asks for an expression, entering the underline character "___" alone will select records that are blank (no data at all) in the specified field.

Add the following two lines to DEDIT.BAS:

```
3165 IF B$(LOOKFIELD(J))="" AND
        SKIPWORD$(J)="_" THEN
        5770 'blank field
3265 IF B$(SEARCHFIELD(J))=""
        AND SEARCHWORD$(J)="_"
        THEN 3290
```

Add two similar lines to the following programs (the number after "then" will change):

DLABELS	1395	1495
DLETTERS	1475	1575
DSTAT	1435	1535
DPUT	5255	5355

While doing this I found that the built-in editor in Basic-80 5.2 goofs up if you use "_" in edit mode. Just type the line as a new line.

Dan Dugan Sound Design
833 14th St.
San Francisco, CA 94114
(415) 621-0781

The New 16-Bit Super Microcomputers

A comparative look at the Intel 80286, Motorola 68000, and National 16032

by William G. Wong

The new collection of super microcomputers provides a major architectural improvement over the existing 8- and 16-bit microcomputer chips such as the 8080, Z80, and 8086. The architectures of three new super microcomputer chips are presented in this article. These include the iAPX 80286 from Intel, the 68000 family from Motorola, and the National Semiconductor 16032. The main features found in these new architectures include:

1. Faster execution
2. Enhanced instruction sets
3. Hardware multitasking support
4. Improved debugging capabilities
5. Large address space (usually 16 MB)
6. Virtual memory support (greater than 16 MB/task)
7. Instruction and data cache
8. Floating-point hardware

More details in areas such as individual instruction operation can be found in the various manuals available from the manufacturers listed at the end of the article. The architectures of the 80286, the 68000, and the 16032 will be considered individually, since they are all quite different. The summary will deal only with a superficial comparison of the three, since any actual implementation using any of these chips depends heavily on the intended use and product line of the company designing a new computer. Newer chips not covered in this article, but within the same class, include the Zilog Z8000 and Z80000, the Intel 432, and the DEC LSI-11 series.

The three microprocessors reviewed cover both the 16- and 32-bit world. The 80286 is a 16-bit processor, while the 68000 and 16032 are 32-bit processors. The following presentation shows why all three are within the same class of super microcomputers.

Intel iAPX 80286

The Intel iAPX 80286 is really a greatly improved version of the very popular Intel 8086 family. In fact, the 80286 actually has two operating modes. One is the 8086 mode, which provides a fully compatible 8086 environment, including the 1 MB memory limit. The advantage over the 8086 is speed: The 80286 native mode is more powerful and increases the memory limit to 16 MB. There are quite a number of additional enhancements, which are addressed in the remaining part of this section.

Figure 1 shows a block diagram of an 80286 system. It includes the optional 80287 numeric processing unit (NPU) which provides IEEE-compatible floating-point support in the same fashion as the 8087 NPU does for the 8086. The 80286 includes two queues for instruction pipelining, which increases execution speed. The prefetch queue simply does a look-ahead from the instruction pointer and retrieves up to 8 bytes of code; the other queue contains decoded instructions that have been converted into internal microcode from the prefetch queue code. The 1 gigabyte logical memory limit is discussed later.

William G. Wong, 902B Merritt Drive, Somerville, NJ 08876

Figure 2 shows the programmer's model of the 80286. Note that the visible register set is identical to that of the 8086. The invisible portion is used in the native mode operation. The key additions to the 8086 architecture are in the invisible portion used in the native mode operation. The key additions to the 8086 architecture are in the invisible portion of the 80286 model. This is also where the virtual memory and multitasking support are provided.

The 80286, like the 8086, is a segmented memory machine where memory is viewed as a number of segments which, in this case, are smaller than the logical address space. The segment size for both the 8086 and 80286 is limited to 64K. Four segment registers (CS, DS, SS, ES) are provided, and all memory accesses use of one of these registers to reference physical memory. The native mode operation also has a program-invisible segment descriptor register paired with each of the segment register.

The segment descriptor register contains the physical base address within the 16 MB physical memory along with the size of the segment, which is up to 64K. Access rights are also contained in the descriptor register, which indicate whether the segment is read only, executable, resident, and so on. These access rights and limit values allow an operating system to restrict the use of segments by programs and provide the virtual memory support required in the super microcomputer environment.

Since the segment descriptor registers are invisible to the program, the 80286 must take care of their contents. In fact, the 80286 does this on a demand basis, using the Global Descriptor Table (GDT) and the Local Descriptor Table (LDT) registers. These registers also contain segment descriptors whose segments contain segment descriptors, whereas the CS, DS, SS, and ES segment descriptors reference program code and data. The value in the visible segment registers is actually an index into either the GDT or the LDT. When a segment register is first used for a memory reference, the 80286 checks the appropriate descriptor table and loads the invisible portion of the segment register with the segment descriptor located in the table. Changing the contents of a segment register will cause the local copy of the memory segment descriptor to be marked invalid, thereby requiring a subsequent descriptor table reference if the segment register is used again.

The Interrupt Descriptor Table (IDT) register is used in the same fashion, except that an interrupt vector is used to index the table. The other difference is that the IDT contains special task segment descriptors that are loaded into the Task State Segment (TSS) register. This process is actually a hardware-supported task switch mechanism, which is the basis for the hardware multitasking support provided by the 80286. This support and its operation are discussed in more detail later.

Figure 3 shows how the 80286 uses the segment descriptor registers to reference main memory. A process can access only four 64K segments at any one time, as in the 8086. However, the segment registers can index 8K segment descriptors in the GDT or the LDT; thus a program can have indirect access to 1 gigabyte of memory, provided that all segments are 64K in size. The number of processes is limited only by the operating system implementation.

Figure 4a shows the selector format for values loaded into the visible segment registers. The use of the index and table fields have been described. The Requested Privilege Level (RPL) field provides an additional protection mechanism that is combined with other privilege level indicators within the 80286 architecture. Each process (also called a task) operates at one of four privilege levels shown in Figure 4b. The Kernel is the most privileged process and has access to all memory segments, invisible segment regis-

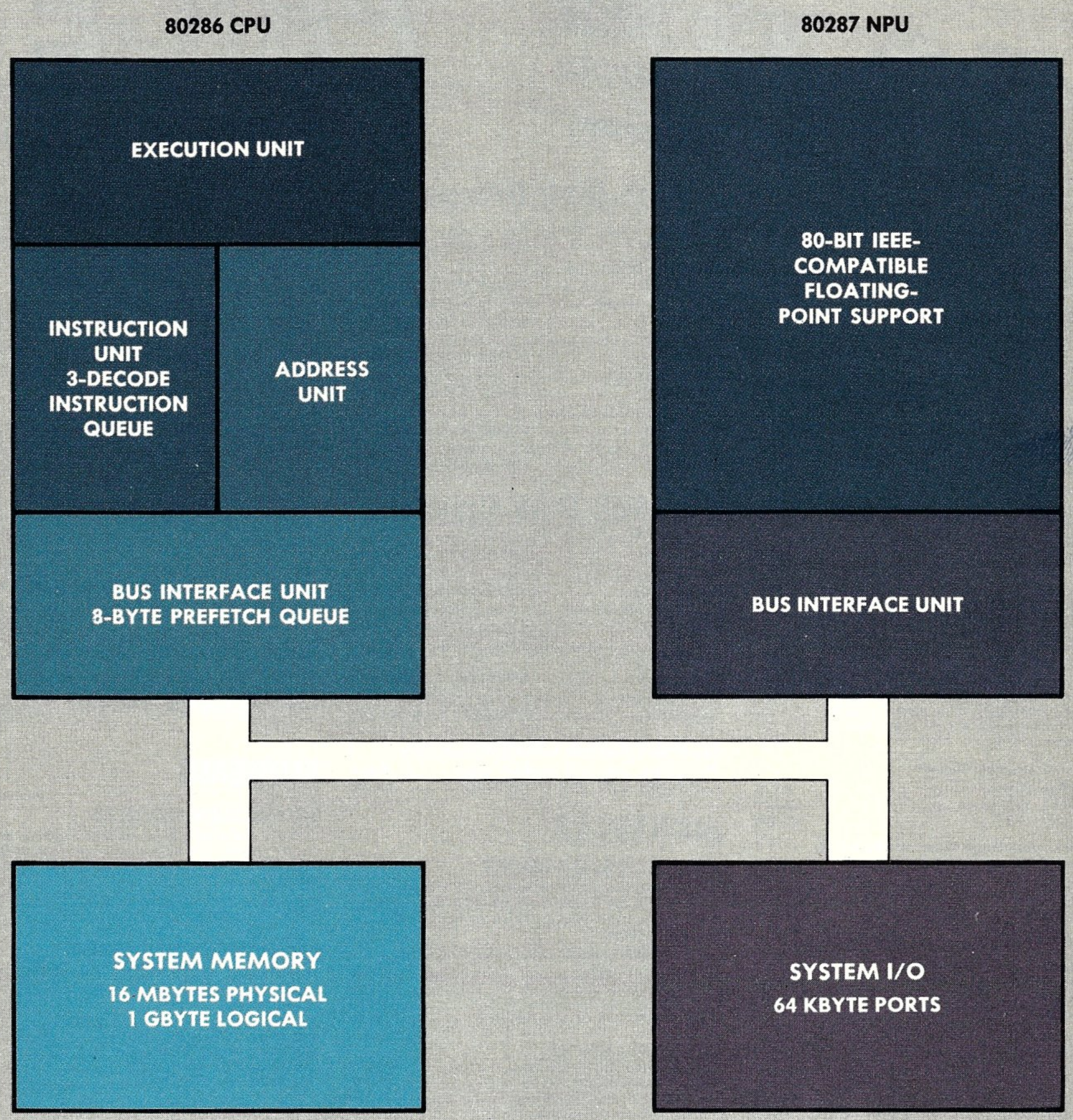
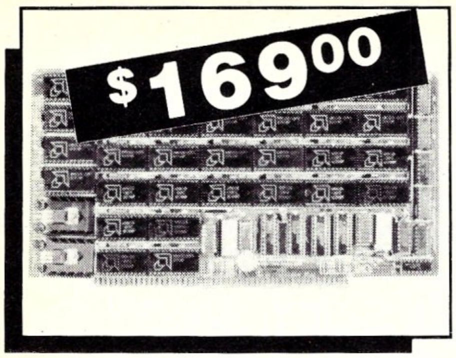
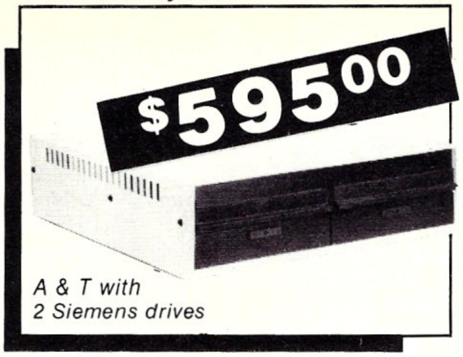


Figure 1. Intel 80286 system diagram.

64K Static Ram



8-inch Sub-system



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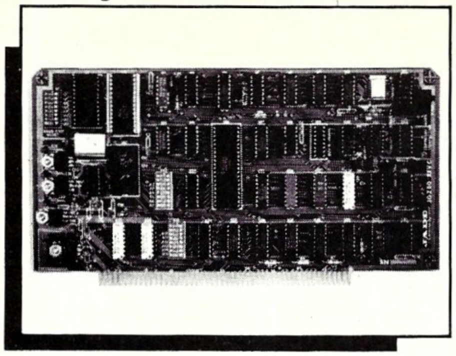

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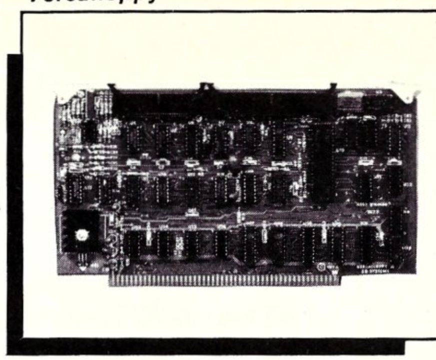

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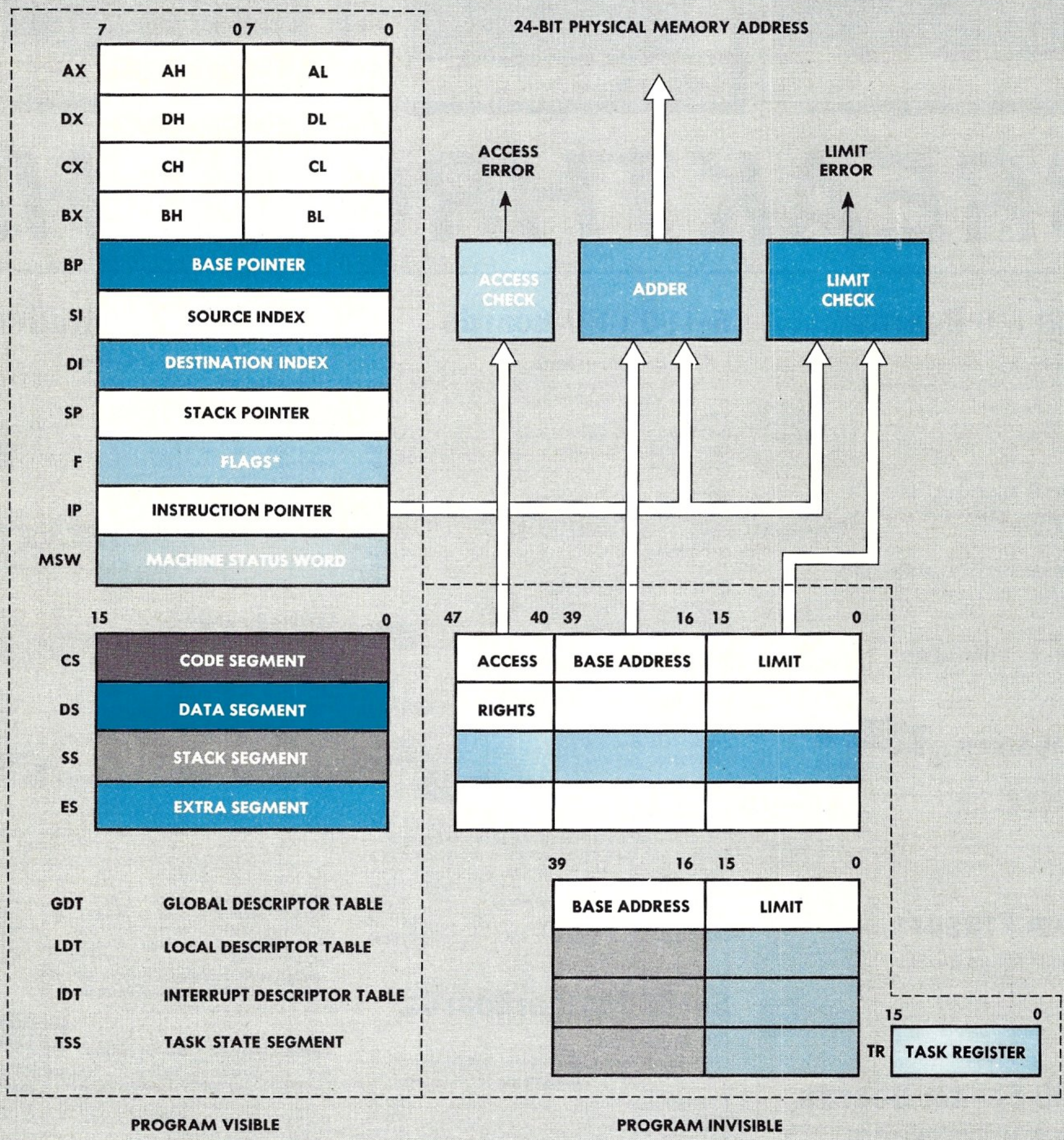


*Flags Bits:

0	CARRY	4	AUXILIARY CARRY	8	TRAP ENABLE	12, 13	I/O PRIVILEGE LEVEL
1	RESERVED	5	RESERVED	9	INTERRUPT ENABLE		
2	PARITY	6	ZERO	10	DIRECTION	14	NESTED TASK
3	RESERVED	7	SIGN	11	OVERFLOW	15	RESERVED

Figure 2. Intel 80286 CPU block diagram.

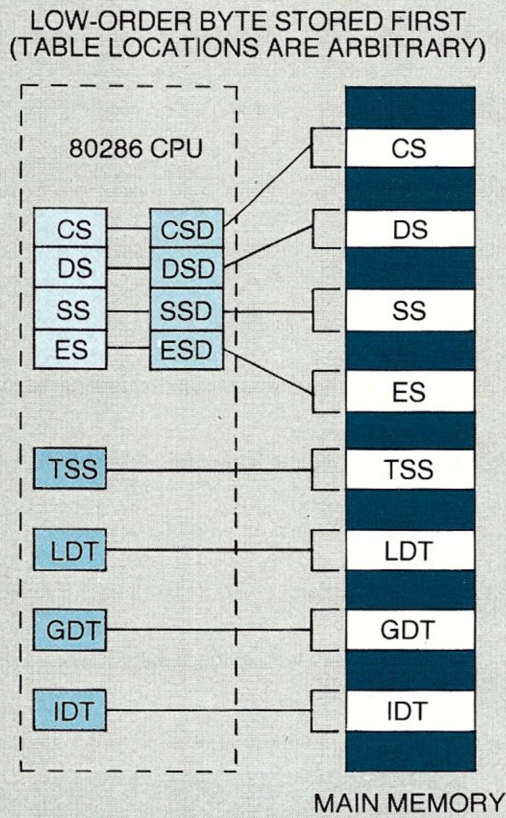


Figure 3. Intel 80286 memory map.

ters, and all I/O. The Kernel is always imbedded in the operating system. Application processes, on the other hand, are the most restricted and must request the operating system to perform control operations such as I/O. This hardware privilege level support is needed to provide security in a multitasking environment.

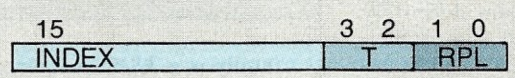
Figure 4c shows the general format for a descriptor contained in a table referenced by the GDT, LDT or IDT. The reserved section must be zero for compatibility with future Intel super microcomputers such as the iAPX 80386. The descriptor information is dependent upon the contents of the type field; however, the field to notice at this time is the Descriptor Privilege Level (DPL). This is also tied in with the privilege level of the current 80286 and each of the selectors. In general, the DPL value is used to control access to segments indexed through the GDT, since this does not usually change when different processes run. System services could thereby access segments when called from different processes, but a normal application could not use this privileged information.

Figure 5 shows the format for different descriptor types which are referenced by the GDT, LDT and IDT. The code and data descriptor format in Figure 5a shows how the contents of the descriptor match those of the invisible segment descriptor registers in the 80286. The base and limit fields describe the segment location and size within the 16 MB of physical memory, while the remaining bits contain the access of rights. The Present and Accessed bits are used for virtual memory support. An interrupt occurs if a referenced segment is not present, and the accessed bit is updated in the appropriate GDT or LDT table entry when a segment is referenced.

Figure 5b shows a gate descriptor whose operation may be new to many people. Gates are accessed by a long call or

Intel 80286 Privilege Control

Selector:



T—TABLE TO BE ACCESSED (0—GDT, 1—LDT)
RPL—REQUESTED PRIVILEGE LEVEL (0-3)

Figure 4A. selector format.

The Intel iAPX 80286 is really a greatly improved version of the very popular Intel 8086 family. The 80286 native mode is more powerful and increases the memory limit to 16 MB, and there are quite a number of enhancements.

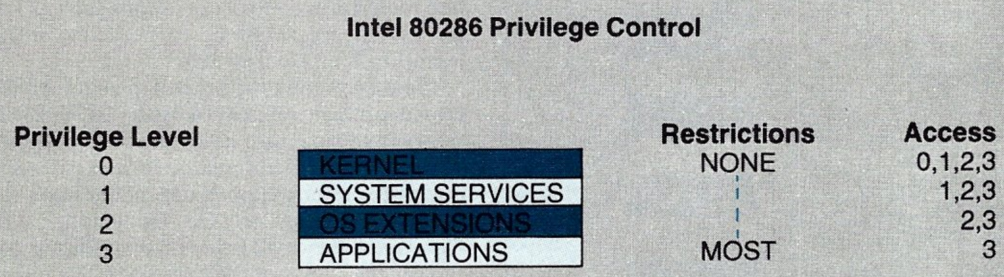


Figure 4B. The four privilege levels.

jump through the GDT or LDT segments or an interrupt through the IDT segment. The difference occurs when the segment accessed contains a gate descriptor instead of a code segment descriptor. A gate allows two things to occur. The first is that the privilege level of a process can change in a controlled fashion and, optionally, a coroutine style task switch can occur. The original privilege level is restored when the referenced routine returns.

Figure 5c describes the system segment descriptor. This can be loaded into the TSS register only in response to a task switch operation via a gate segment descriptor. In this case, the current process state is saved in a segment like that shown in Figure 5d. The new process state is loaded from a similar segment referenced by the new system segment descriptor, which is then loaded in the TSS register.

The 80286 also provides a number of new instructions that are primarily for access to the invisible registers, such as the LDT and GDT, while in the Kernel privilege mode. This, combined with the hardware support for multitasking, virtual memory, and floating point definitely make the 80286 a super microcomputer. A fairly compatible superset of the 8086 instruction set makes it a formidable chip. Programmers using the 8086 should keep in mind that the values placed into the visible segment registers should be used carefully if programs are to be moved to the 80286 without any change. This upgrade path is one of the best features of the 80286.

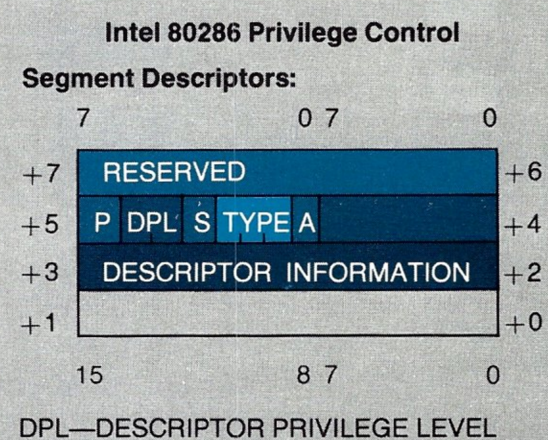
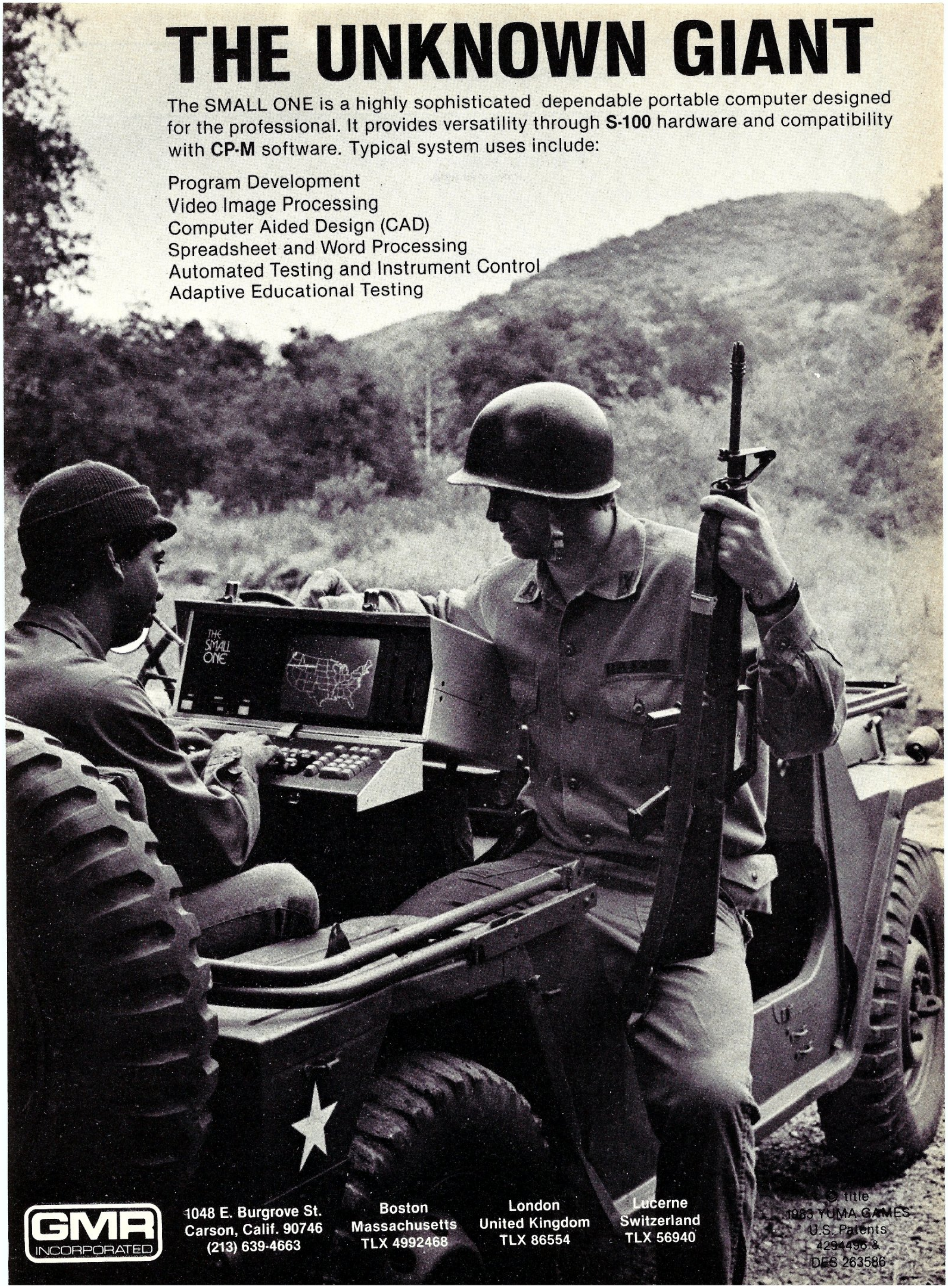


Figure 4C. General format for a descriptor.

Motorola 68000

The M68000 family contains a number of code-compatible processors, some of which (like the 68010) provide virtual memory support. Internally, each member of the 68000 family is a 32-bit microprocessor with an orthogonal instruction set; most of the registers are fully general purpose, so a programmer can use them without having to worry about special instructions that use particular registers. Figure 6 shows a system diagram of a 68000 with virtual memory support provided by one or more separate 68451 Memory Management Units (MMU). This differs from the on-chip support provided by the 80286. The 68000/68451 provides a 16 MB physical address space and a 16 MB logical address space per process. I/O is memory mapped and thus forms part of the physical address space.

Internally, each member of the 68000 family is a 32-bit microprocessor with an orthogonal instruction set. Most of the registers are fully general purpose, so the programmer can use them without worrying about special instructions that use specific registers.



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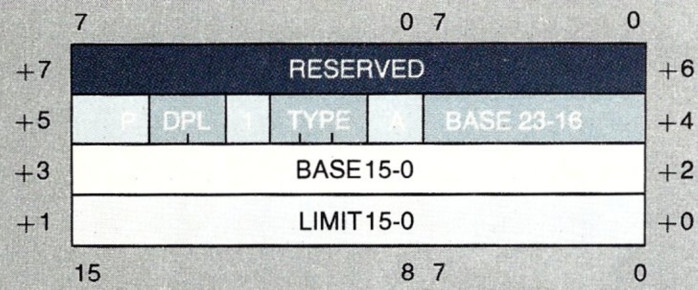
Intel 80286 Segment Descriptors

Code and Data Descriptors:



	Bit	Name	Function (0)	Function (1)
	7	PRESENT	SEGMENT NOT IN MEMORY	SEGMENT IN MEMORY
	6-5	DPL	SEE PRIVILEGE CONTROL	DESCRIPTION
	4	—	—	MUST BE 1
BIT 3 IS 0	3	EXECUTABLE	DATA SEGMENT	CODE SEGMENT
BIT 3 IS 0	2	DIRECTION	SEGMENT GROWS UP	SEGMENT GROWS DOWN
BIT 3 IS 0	1	WRITEABLE	READ-ONLY ACCESS	READ-WRITE ACCESS
BIT 3 IS 1	2	CONFORMING	EXECUTE ANYTIME	CPL CANNOT BE LESS THAN DPL
BIT 3 IS 1	1	READABLE	EXECUTE ONLY	READ AND EXECUTE ACCESS
BIT 3 IS 1	0	ACCESSED	SEGMENT HAS NOT BEEN ACCESSED	SEGMENT HAS BEEN ACCESSED

Figure 5A. Code and data descriptor format.

This reduces the instruction set complexity, since there are no special instructions for supporting peripheral interfaces. The MMU is the exception to the rule because there are special instructions for accessing this device. By design, such operations are normally restricted to the operating system, so application programs would not require their use.

Figure 7 shows the programmer's model of the 68000, which is the same for each chip. It has a very simple and regular architecture, and the 32-bit registers allow a program to have direct access to the entire 16-MB address space. The address is actually 24 bits in length, allowing growth for future chips such as the 68020.

The 68000 provides limited multiprocessing support along the lines of conventional microprocessors. It does have two privilege levels, user and supervisor, along with a separate stack pointer for each level. Unlike the 80286, the 68000 must do a task switch in software. The task switch is complicated due to the interaction with the 68451 MMU shown in Figure 8. The task state number must be changed in each MMU in addition to changing all the 68000 registers when a task switch occurs.

Each process usually operates in a different logical address space controlled by the MMU. The MMU accepts logical memory address and converts them into physical memory addresses, which are then sent to physical memory. The MMU operates in a paged/segment mode where the pages are 256 bytes and the segments are some number of pages. The page index is used to access a form of content-addressable memory in each MMU containing segment descriptors similar to those of the 80286. The selected segment descriptor supplies the physical page index. An interrupt occurs if only one segment descriptor is not selected.

The MMU is a very complex device that is equally complex in its programming. Each process is given a number that is placed into the address state table when the process is active. This table is accessed for each memory reference depending upon the current state of the 68000. The table also contains the supervisor process number, which is compared against address space number in each segment descriptor. A segment descriptor is selected when the address space and logical address match. A mask is provided for each of these to allow segment descriptors to be shared

The 68000 family presents a very simple and regular architecture to the programmer, since MMU control is performed by the operating system. The clean processor model and large linear address space make the 68000 similar to many large mainframes.

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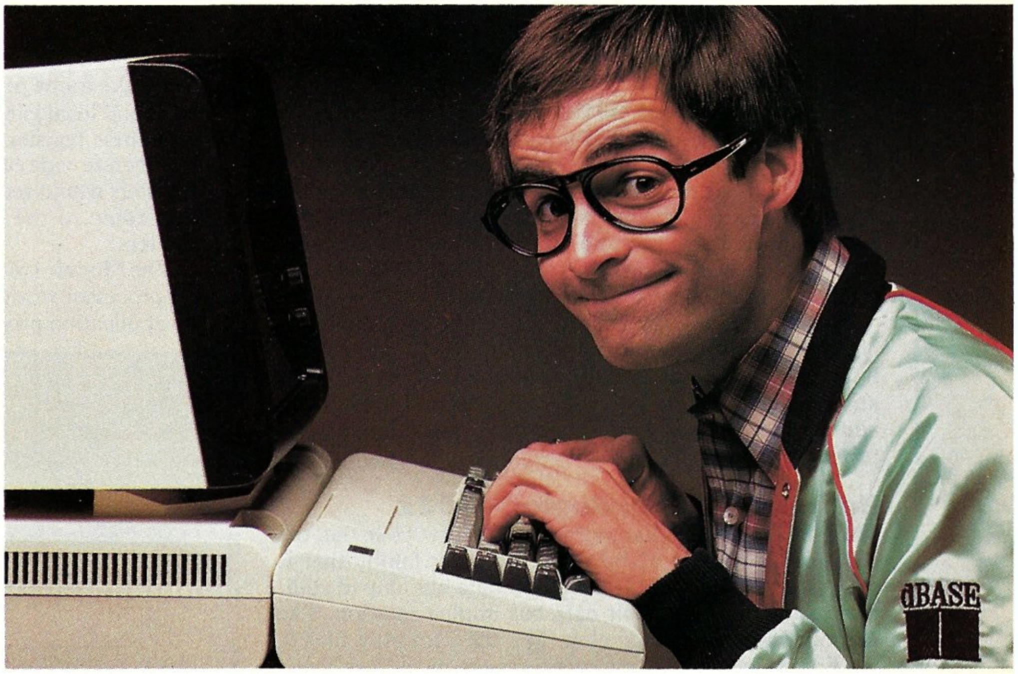

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by a number of different tasks.

Loading the segment descriptors is done under program control, using special instructions to access the accumulator registers in each MMU. A system can have one or more MMUs. Some operations access all MMUs at once; other instructions access one MMU at a time. The control registers in the MMU are used to determine memory access conflicts.

Figure 9 shows that the 68000 memory map is much simpler than that of the 80286; however, the interrupt vectors must be placed at the bottom of the physical memory. Actually, this is not a problem, given the memory mapping scheme, since application programs can have this logical area mapped to some other physical area in memory, thereby allowing only the operating system to update the interrupt vectors in a controlled fashion.

The 68000 family presents a very simple and regular architecture to the programmer, since the MMU control and interrupt control are normally performed only by the operating system. The clean processor model and large linear address space make the 68000 similar to many large mainframe computers.

National Semiconductor 16032

The NSC16032 is similar to the Motorola 68000 in that the NSC16032 is also a 32-bit microcomputer family that is supposed to include an 8- and 32-bit data bus chip in addition to the original 16-bit data bus implementation. The National Semiconductor chip, like the Motorola 68000, provides an orthogonal instruction space and a large linear access space. The 16032 system diagram (Figure 10) is very similar to that of the Motorola chip, but the 16032 contains a number of significant features.

The first is the 8-byte instruction prefetch queue in the main processor, which is the 16032 chip. This helps increase execution speed for many programs. There is also an IEEE-compatible floating-point processor chip called the 16081 Floating Point Unit (FPU) which, amazingly, fits into a standard 24-pin dual inline package (DIP) instead of the 40-pin DIPs normally associated with super microcomputer floating-point units. The 16082 MMU fits into a larger 48-pin DIP and provides the programmer with a large, linear, paged virtual address memory similar to that of the 68000; however, only one 16082 MMU is ever needed, regardless of configuration, which simplifies hardware design. The MMU is discussed later in more detail.

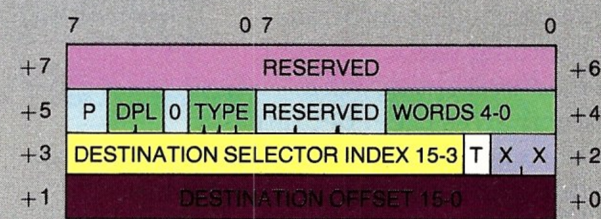
The 16081 FPU contains eight general-purpose floating-point registers, similar to the eight general-purpose registers in the main CPU, as shown in Figure 11. The symmetric register set is combined with an orthogonal instruction set to produce a very complete execution environment. A number of special registers are included to improve this environment.

The first is the Interrupt Base (INTBASE) register, which points to the base of the interrupt vector table. This allows the table to be placed anywhere in memory, as with the 80286, instead of being limited to a fixed location as with the 68000. The Static Base (SB), Frame Pointer (FP), and stack registers (SP0 and SP1) are used to provide a conventional stack architecture that facilitates the implementation of lexical languages such as Algol, C and Pascal. The static base (SB) points to the base of the global variable table; the frame pointer (FP) references procedure parameters and local variables. The instruction set is designed to take these registers into account, thus allowing compilers to generate code easily and efficiently. Elimination of these registers would require two or more general registers to be dedicated to the same purpose, thereby complicating matters.

The Module (MOD) register is a new addition to the microprocessor world. It assists in the use of system modules by application programs. Mathematical subroutine librar-

Intel 80286 Segment Descriptors

Gate Descriptors:



Field Name	Description
PRESENT	0—CONTENTS NOT VALID 1—CONTENTS VALID
TYPE	(SEE SYSTEM SEGMENT DESCRIPTION) 4—CALL GATE 5—TASK GATE 6—INTERRUPT GATE 7—TRAP GATE
WORDS	(FOR CALL GATE ONLY) NUMBER OF WORDS TO COPY FROM CALLER'S STACK TO CALLED PROCEDURE STACK.
TABLE	0 — USE GDT 1 — USE LDT

Figure 5B. Gate descriptor.

The 16032 contains a number of attractive features. Among them are a 8-byte instruction prefetch queue in the main processor, which helps increase execution speed, and an IEEE-compatible floating-point processor chip called the 16081 Floating Point Unit.

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Intel 80286 Segment Descriptors

System Segment Descriptors:

	7				0 7	0	
+7	RESERVED						+6
+5	P	DPL	0	TYPE	BASE 23-16		+4
+3	BASE 15-0						+2
+1	LIMIT 15-0						+0

Bit	Name	Function (0)	Function (1)
7	PRESENT	CONTENTS NOT VALID	CONTENTS VALID
6-5	DPL	SEE PRIVILEGE CONTROL	DESCRIPTION
4	—	MUST BE 0	—
3-4	TYPE	SEE BELOW	—

Type	Description
0	RESERVED
1	AVAILABLE TASK STATE SEGMENT
2	LOCAL DESCRIPTOR TABLE (LDT) DESCRIPTION
3	BUSY TASK STATE SEGMENT
4-7	SEE GATE DESCRIPTOR DEFINITION
8-15	RESERVED

Figure 5C. System segment descriptor.

ies would be a good example of modules that could be used by a number of applications running at the same time in a multitasking environment. The MOD register allows these programs to share the same subroutine module without having it as part of each program that requires it. Instead, each program references the module through the MOD register with special access instructions. This reduces program loading and memory requirements since common modules are shared and only loaded once.

Unfortunately, there was a little skimping on the silicon because the MOD register is only 16 bits wide, which means that the module table *must* reside in the first 64K of memory. Although this is a restriction it is not too limiting, since only references to the modules are stored within this space, not the modules themselves. The module table is shown in Figure 12, along with the interrupt vector table and the memory mapping implementation.

The 16082 MMD (Figure 11) is a very interesting piece of hardware. It provides each process with a large linear address space like that of the Motorola 68000, but it uses memory-resident tables which, like those of the Intel 80286, are automatically referenced and updated by the MMU. This combination leads to a very elegant solution to the problem of handling a large virtual address space, while still allowing a large number of processes to run in a multitasking environment such as a typical multiuser system.

The 16082 MMU takes each address from the 16032 and converts it to a physical address using an internal, associative, address translation cache. It is page oriented, with 512 bytes per page. This allows the nine least significant address bits to be used without any sort of translation. The translation cache contains 32 entries. The operation of the cache is fairly simple and is totally transparent to the program and CPU, unless an error occurs. This will be discussed later.

Logical addresses are presented to the 16082 MMU, which generates a physical memory address. This is done

The 16082 MMD provides a very elegant solution to the problem of handling large vertical address space.

by taking the two indices in the logical address and comparing them with the contents of the address translation cache. The Page Frame Number (PFN) from the matching cache entry is used in the physical memory address. If no matching entry is found, then the Least Recently Used (LRU) entry is discarded and the PFN for the new address is found by indexing the two Index Page Tables. Accessing the tables, updating the cache, and generating the physical address are done automatically by the MMU.

Parity and nonresident memory page errors are serviced by the supervisor process, which uses a different set of index page tables. The 16032 keeps track of the user/supervisor state and gives this information to the 16082 MMU, which has two Page Table Base regulars (PTB0 and PTB1)—one for each state. The 16082 MMU also has a number of other registers, as shown in Figure 12.

These include the page table base registers, the status and error registers, and a number of special registers added just for program debugging. The latter can be extremely useful when building a system and even for debugging application programs. The main difference between the conventional debugging techniques on other systems and the 16032 is that the 16082 MMU keeps track of breakpoint locations and program statistics, whereas conventional debuggers normally replace the code being traced with a special debugging instruction.

In the conventional case, the breakpoint is found by executing the special instruction that calls the debugger, which can then replace the original instruction. There are three disadvantages to this approach. The first is that the program is actually changed when debugging, which may affect its operation. The second disadvantage is that this approach cannot be used to debug ROM-based software or software that may use ROM-based modules. The third disadvantage is more subtle. The 16032 is designed for a multitasking environment; debugging programs in this environment could be a problem if a program using a shared module is being debugged, because setting a breakpoint in this module may cause a trap to occur in a program that is not being debugged.

The additional debugging registers in the 16082 MMU solve these problems by supporting the debugging process without the need for program modification. The breakpoint registers can be set to the address that is to be traced. An interrupt will occur whenever this location is used in the appropriate manner. These breakpoint registers are actually more powerful than the conventional debugging sequence mentioned above because the MMU can trace program execution or variables. A number of other extremely useful options associated with these breakpoint registers make the MMU more powerful than most of the commercially available logic analyzers. The only part that detracts from this debugging feature is that the loading operation is not automatic like the normal virtual memory address translation.

Although the task switch process for the 16032 is not as automatic as in the Intel 80286, it is much better than in the Motorola 68000. This, combined with a powerful instruction set and large address space, make the National

Intel 80286 Segment Descriptors

PHYSICAL MEMORY	
TASK LDT SELECTOR	42
DS SELECTOR	40
SS SELECTOR	38
CS SELECTOR	36
ES SELECTOR	34
DI	32
SI	30
BP	28
SP	26
BX	24
DX	22
CX	20
AX	18
FLAG WORD	16
IP (ENTRY POINT)	14
SS FOR CPL2	12
SP	10
SS FOR CPL1	8
SP	6
SS FOR CPL0	4
SP	2
BACK LINK SELECTOR TO TSS	0

Figure 5D. System segment layout.

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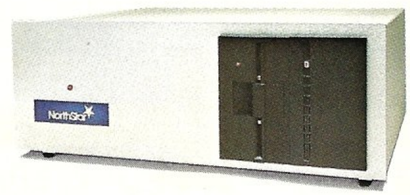

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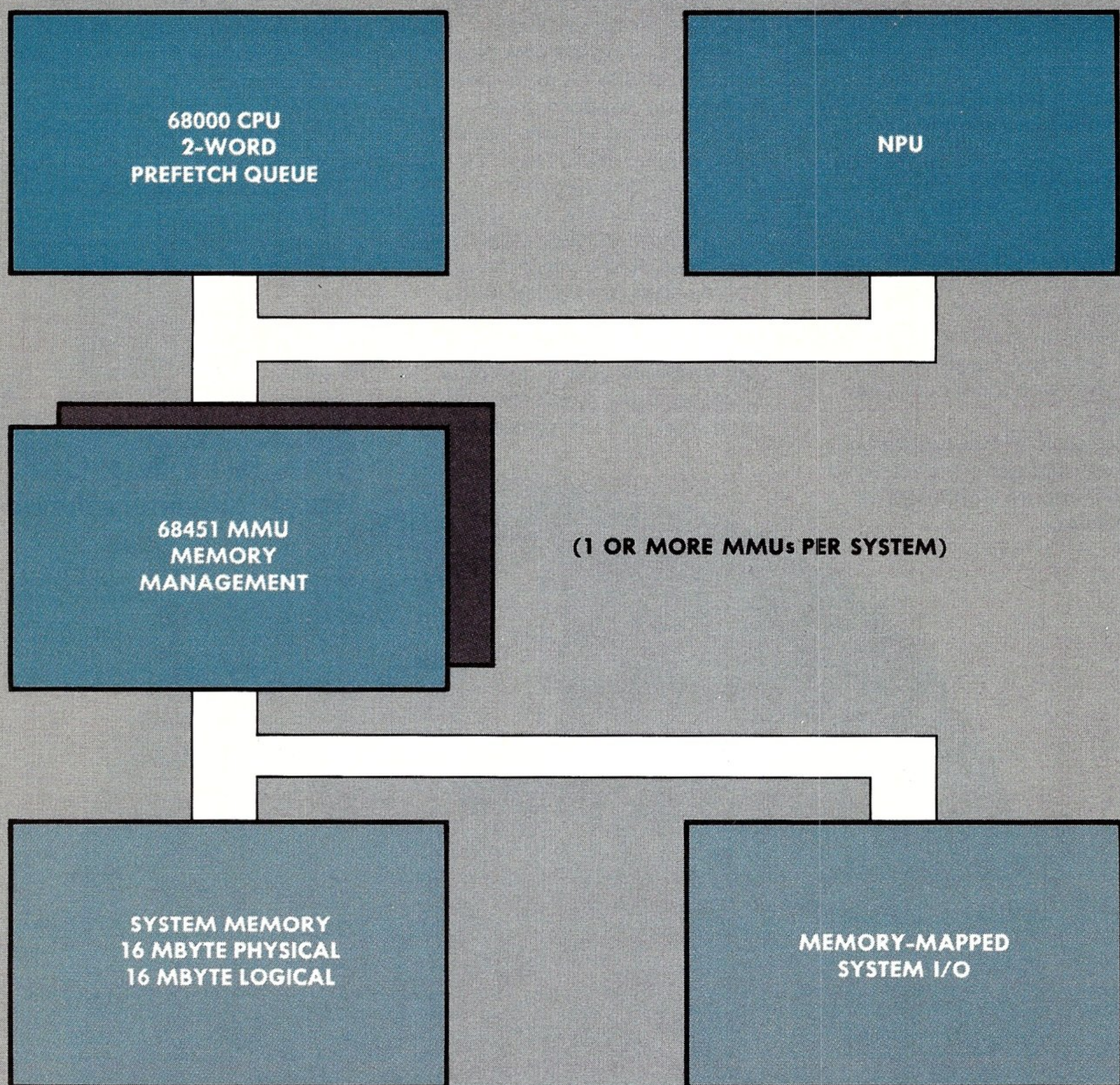
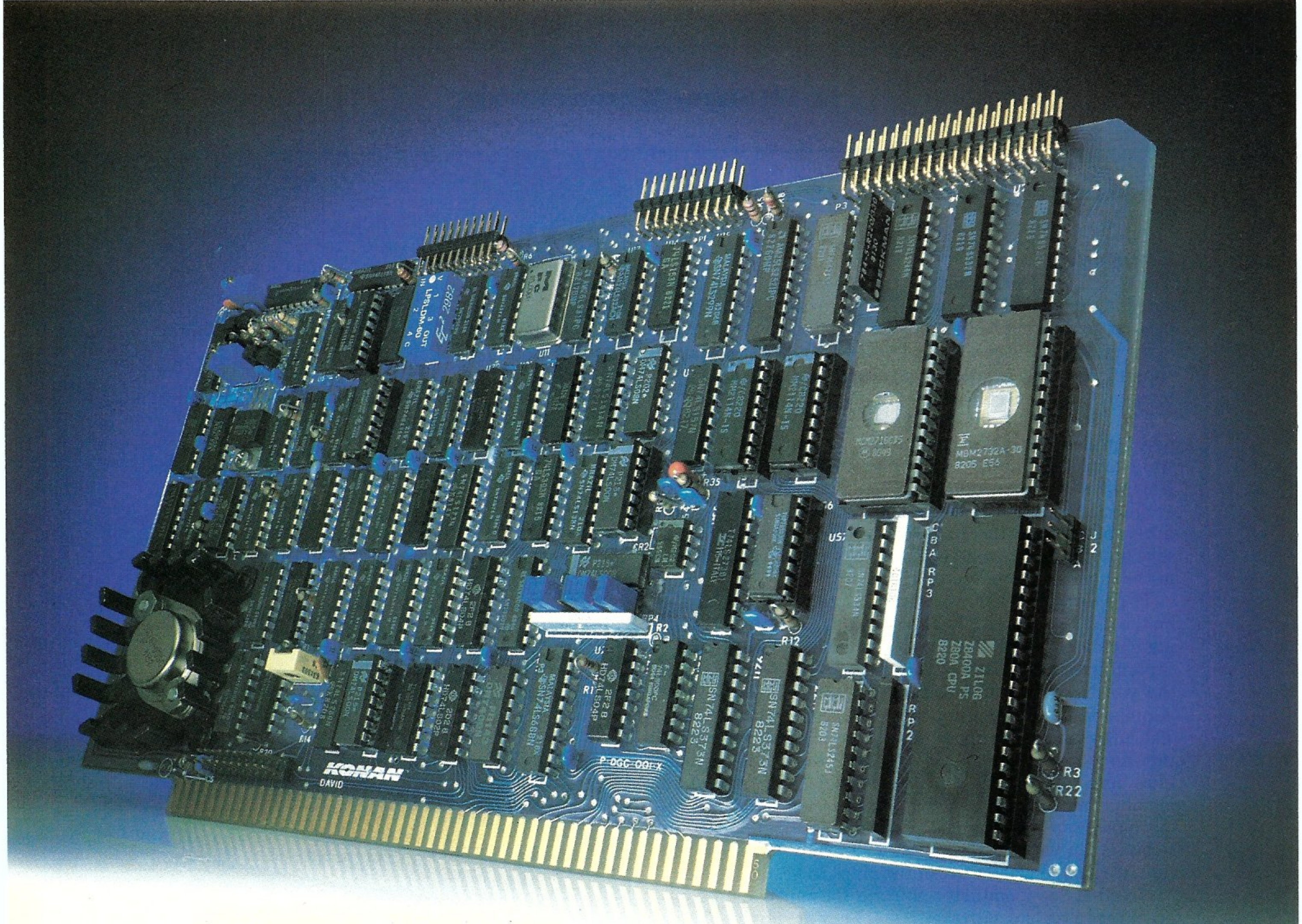


Figure 6. Motorola 68000 system diagram.



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Semiconductor 16032 a very formidable processing system.

Summary

The 80286, the 68000, and the 16032 are all quite sophisticated in design and operation. They provide support for a new range of applications that could not be done using existing microprocessors. Virtual memory and floating-point support will lead to functionally large, sophisticated systems that are physically small and inexpensive.

The Intel 80286's unique design provides a number of new features that make it an interesting candidate for software implementation. The compatibility with the Intel 8086 will add to its popularity. The 80286 has only a 16-bit architecture; however, it provides the largest virtual address space of the three microprocessors discussed. I am sure that the 80286 will become one of the top contenders in the super microcomputer arena.

The Motorola 68000 was the first of the three to arrive on the market; hence, it has an advantage in terms of existing implementations. Although it is the least radical of the three chips covered here, it remains a textbook example of the von Neumann architecture. The 68000 is extremely popular for implementing the UNIX operating system. The interesting thing about the various implementations is that the corresponding MMU is not always used, so that most implementations are incompatible with regard to memory management. In fact, many systems did not require memory management hardware at all, choosing instead to run without the virtual memory support. In any case, the 68000 will be one of the chips to keep an eye on.

National Semiconductor got into the super microcomputer race a bit late with the 16032. They are hoping that is clean design and sophisticated architecture will make it number one in this contest. Inclusion of a single sophisticated MMU within the architecture should lead to common-system architectures in the commercial world, which will benefit application development and ultimately the users, who are really the most important part of the system.

Each super microcomputer examined has its own unique features that make it suitable for particular applications. No one processor appears to be the best in all cases. There are only the first in a line of new super microcomputers, and future versions should prove to be even more interesting.

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NSC16032S-6,-4 High Performance Microprocessor Data Sheet, National Semiconductor Corp., Santa Clara, CA, 1982

Motorola 68000 CPU Block Diagram

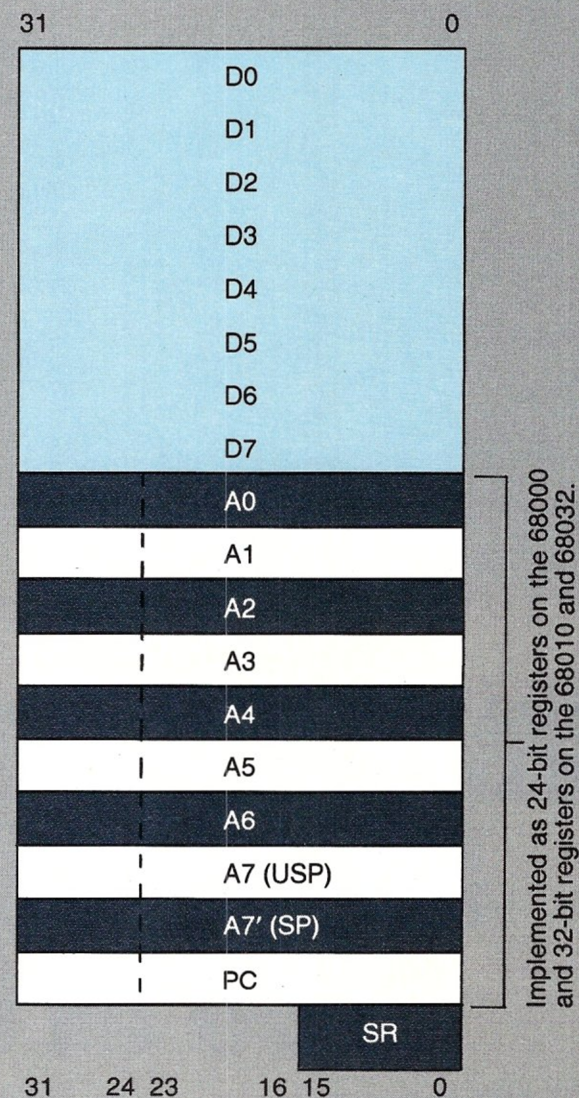

Figure 7. Programmer's model of 68000.

Each super microcomputer reviewed has unique features that make it suitable for particular applications.

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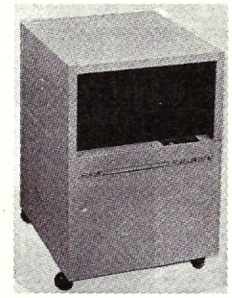

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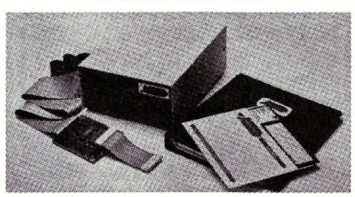

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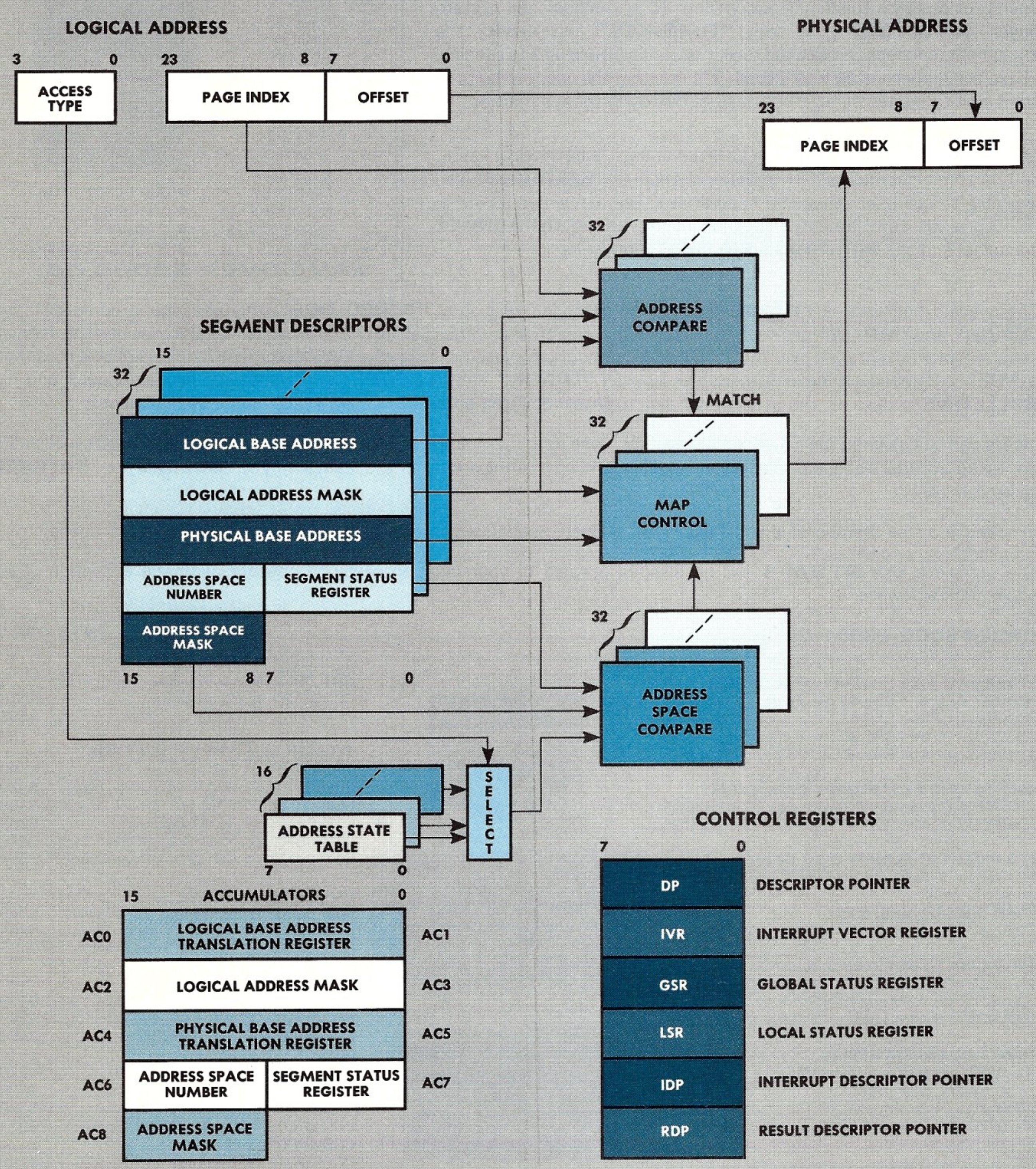

Figure 8. Motorola 68451 MMU block diagram.

Additional information may be obtained from:

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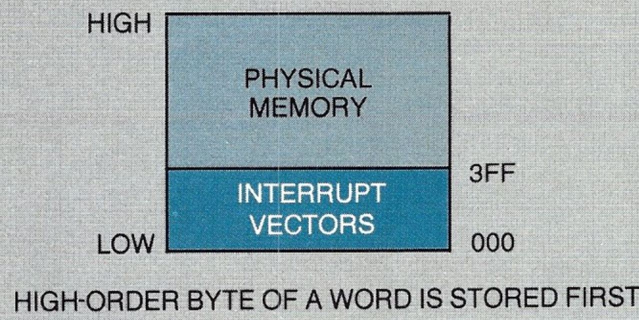

Figure 9. Motorola 68000 memory map.

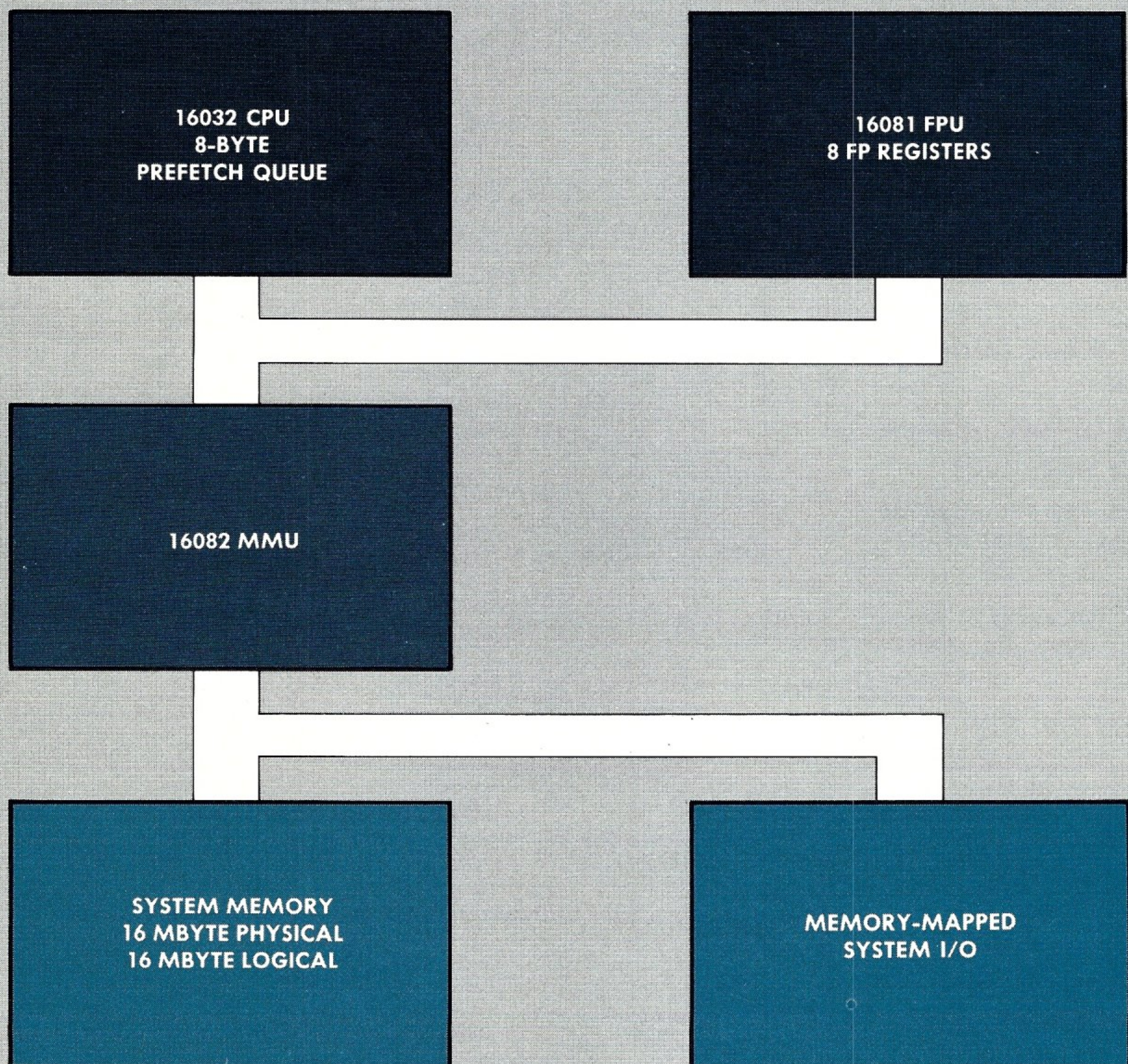

Figure 10. National Semiconductor 16032 system diagram.

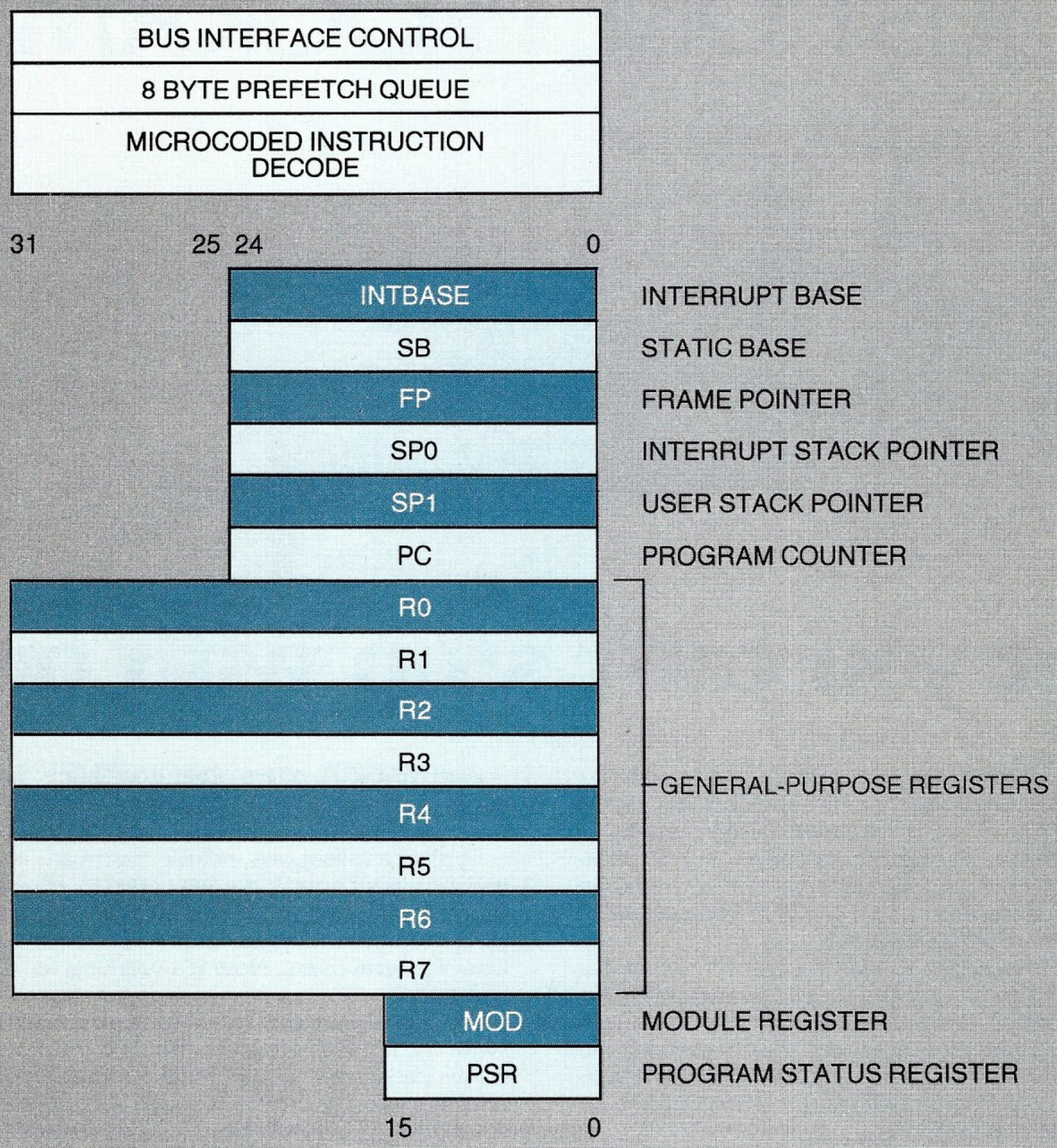

Figure 11. NS 16032 CPU block diagram.

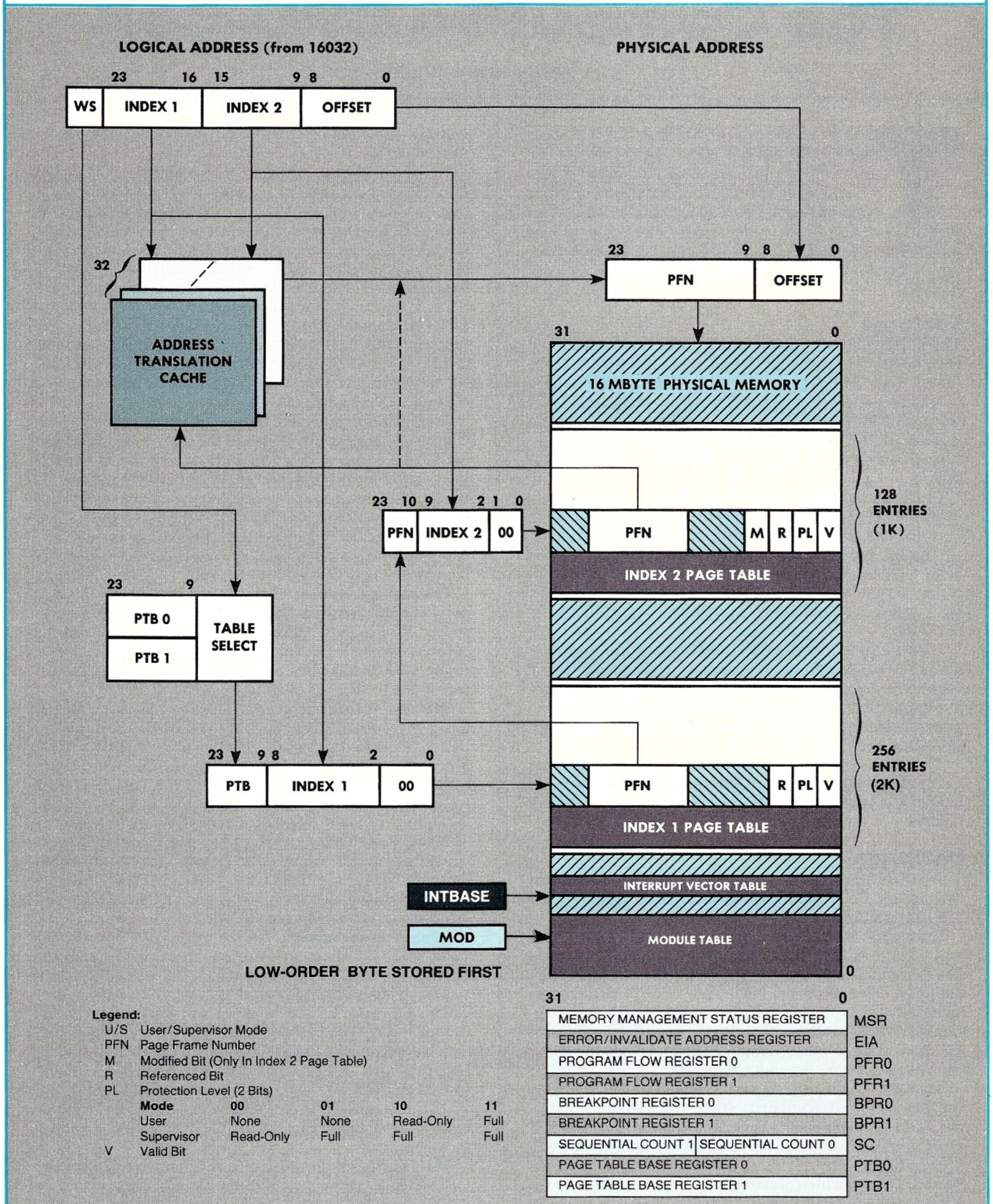

Figure 12. NS16082 MMU block diagram.

MICROSYSTEMS REVIEWS

The CompuPro CPU-68K

by Dave Hardy and Ken Jackson

The CPU-68K 16-bit 68000-based CPU board is one of CompuPro's latest entries into the 16-bit S-100 market. The board is offered ready-to-run with various configurations of other CompuPro boards, and is available with either the CP/M 68K or Forth operating systems. For those who prefer their own O/S, the CPU-68K also has provisions for up to 16K (8K words) of on-board 2716, 2732, or 2764 EPROM.

Features

The CPU-68K is available either A&T (assembled and tested) with an 8 MHz clock and a one-year limited warranty, or in a 10 MHz version under the CompuPro CSC (Certified System Component) program with a two-year warranty. The 8 MHz version costs $695, and the 10 MHz version sells for $850. Both boards also have the ability to run at half-speed (4 MHz or 5 MHz) by just flipping a switch.

Provision has been made on the board for an optional 68451 MMU (Memory Management Unit), although it was not yet available when we tested the CPU-68K. CompuPro recommends that the board be returned to the factory for installation of the MMU so that it can be completely tested before use. At the time of this writing, the 68451 was not able to operate properly at speeds in excess of 4 MHz.

Also included in the CPU-68K board are a unique jump-on-reset feature (that is, unique to the 68000 CPU), vectored interrupt ability, 24-bit addressing, full IEEE-696 compatibility when run at or below 6 MHz, and programmable wait states (which comes in handy with older, slower memory boards).

The quality of the CPU-68K board itself is, like all other CompuPro boards, excellent. It is obvious that CompuPro makes a conscious and effective effort toward quality control.

Hardware

The CPU-68K is literally packed full of features that merit description. Following are brief descriptions of some of the more interesting ones:

Interrupts. Probably the most interesting of the CPU-68K's features is its built-in interrupt system. CompuPro has chosen to use the 68000's built-in prioritized interrupt ability to drive the S-100 NMI* line and six of the seven vectored interrupt lines, VI0 through VI5. A jumper option is also available to allow the CPU-68K to use the S-100 INT* line to signal temporary bus masters to release the bus for master interrupt processing.

The CPU-68K is able to use its own internal ("auto vector") mode for interrupt processing, or it can use an external interrupt controller (CompuPro recommends the System Support I). A jumper is provided to allow the user to select whether a byte-wide or a word-wide response is expected. This is an unexpected but very useful feature of the CPU-68K board that makes it a great deal easier to use in existing systems and, potentially, a lot more versatile in future systems.

Power-on-Jump. Another interesting feature of the CPU-68K is its Power-On-Jump (POJ) ability. This is done in a way similar to the one used in many S-100 boards with POJ features. At system reset, an on-board EPROM is enabled to provide an initial jump address. However, after a reset, the 68000 CPU reads the two double words (8 bytes) starting at address zero and loads them into its stack pointer and program counter, respectively. The on-board EPROM is disabled by any memory write. CompuPro recommends that the first instruction executed after a reset be a JSR (that's a CALL instruction to us Z80 folk) to force the 68000 to push the return address onto the stack and thus disable the EPROM.

I/O. Although the 68000 uses memory-mapped I/O, CompuPro has cleverly designed the CPU-69K to perform S-100 I/O cycles to conform with the IEEE-696 requirements. This means that the system I/O devices will appear to the programmer as memory addresses (from OFF0000H to 0FFFFFFH), but to the S-100 bus as I/O devices! This method allows the CPU-68K to have IEEE-696 16-bit I/O addressing ability, but still allows older 8-bit addressing I/O devices to be used.

Programmable array logic. In order to cram all these goodies onto a single S-100 board, CompuPro used several special ROM chips, called PALs, to perform many of the complicated logic functions required, such as the interface to the S-100 control bus, and the state machine used to decide if one or two bus operations are needed.

Memory management unit. Dynamic memory allocation is provided by the optional 68451 MMU IC. If this option is not installed, the address bus of the 68000 directly drives the address bus drivers. If the 68451 MMU is installed, then it adds the ability to map a virtual address from the 68000 to a physical address that is sent out to the S-100 bus. Using the 68451, it is possible to "re-map" S-100 extended address memory to appear in almost any extended page. Just to make life easy for the programmer, when the MMU is initially reset, it starts up in a "transparent" mode in which no remapping occurs. The MMU itself is located in extended page OFEH.

Miscellaneous signals. Unlike some CPU boards, the CPU-68K will allow an external device to generate the MWRT (Memory WRiTe) signal. This feature allows a system to have a front panel, since most front panels must generate the MWRT signal in order to work properly. Although it is not required by the IEEE-696 standard, provision has been made in the CPU-68K to allow it to tristate (and thus turn OFF) its own master system clock signal Φ (pin 24 on the S-100 bus). Using pin 21 as PHI-DSB*, and NDEF line in the current IEEE-696 standard, slave processors can actually turn off the CPU-68K's clock and insert their own.

Wait states. Wait-state circuitry is provided on the CPU-68K to allow virtually any type of slow device to work properly. From one to five wait states may be independently selected for I/O cycles, ROM cycles, M1 cycles, and/or all cycles.

Dave Hardy, 736 Notre Dame, Grosse Pointe, MI 48230

Software. Software provided with the CPU-68K comes in two basic flavors, mapFORTH and CP/M-68K, both available from CompuPro.

- mapFORTH is a stand-alone operating system with several basic utilities, such as a screen-oriented line editor, a full 68000 assembler, a debugger and miscellaneous utilities.
- CP/M-68K is, of course, Digital Research's 68000 version of the popular CP/M operating system, which is so remarkably like regular old CP/M that is needs no additional explanation, except that it also comes with a C compiler.

Because neither of us speaks fluent FORTH, all or our evaluations were made while running under CP/M-68K. We were provided with several different implementations of CP/M-68K while we were evaluating the CPU-68K, each one less buggy than its predecessor. The final implementation that we received (late in August '83) had no major bugs. Source code for the CompuPro BIOS is included, so we could have easily changed the BIOS to do whatever we wanted.

Two different versions of CP/M-68K are provided on two separate disks. The first disk contains a CP/M system that uses a System Support 1 for the console, requires 256K of RAM, and expects that its floppy drives can step at 3 ms. The second disk contains a system that expects to see an Interfacer 3 (user 7) or an Interfacer 1 addressed at port 10H, and requires only 128K of RAM and floppies with an 8 ms step rate.

The only real problem we had with the software was the relative lack of canned software for CP/M-68K. No doubt, this problem will eventually disappear, as it did for the 8086/8088, when CP/M-68K becomes more widely used. Many of the benchmark tests that we usually perform on a new board couldn't be performed because we didn't have the proper applications software. In our sorting tests, runtime measurements were about the same for the CPU-68K as they were for the IBM-PC. Unfortunately, they can't be considered valid because the 68000 code was generated by translating the programs from 8086 code. Our suspicions are that the 68000 is a great deal better at sorting when its programs are optimized for the 68000.

Documentation

Documentation provided for the CPU-68K is a single concise manual of about 20 pages. It includes a technical overview, a theory of operation, a jumper and switch set-up summary, schematic diagrams, and a board layout drawing. Although brief, the manual provides all of the information necessary to understand the operation of the CPU-68K board, except for the 68000 IC itself. All of the jumper and switch settings are explained in the text, although a knowledge of reading schematic diagrams is necessary to really understand what some of the jumpers do.

Similar manuals are provided for the mapFORTH and CP/M-68K operating systems. These manuals, however, give exact descriptions of exactly what to do to set up a system to run their operating system. Instructions are given for setting up most of the CompuPro I/O boards to work with the particular operating system, right down to the exact switch and jumper settings on each board.

System start-up and use

In any case, no matter which operating system you choose, you'll need to have the following to bring up the CPU-68K:

- An S-100 frame
- A CPU-68K board
- A CompuPro System Support 1 or Interfacer 3 or 4 board
- A CompuPro DISK 1 floppy disk controller
- At least 128K of RAM
- At least one 8″ floppy drive, with cable and power supply
- A serial terminal and cable set up for 9600 baud, 8 bits, no parity, and 1 stop bit.

To start up the system, you'll have to set up each board according to the instructions given in the manual for the operating system that you've chosen. There are *many* jumpers to be set, so this will take a while. Fortunately, the operating system manuals tell you how to set up *all* of the boards, so you don't have to waste a lot of time paging through each of the technical manuals trying to figure out which jumper goes where.

Although the systems are provided on single-sided disks, double-sided floppy drives will also work, and double-sided disks can be read and written once the system is booted up.

Likes/dislikes

We were impressed with the quality and reliability of the hardware provided for our tests. Once the system was running, we really had no problems at all. Our biggest complaint was that if the system didn't start up, we wouldn't know where to start looking. An EPROM monitor or at least some built-in diagnostics would come in very handy for troubleshooting in the event of system trouble. To a certain extent, we could tell if the problem was in the floppy controller or CPU board, but if there had been an I/O problem, we would have been in deep trouble to diagnose it from the system's reactions. This is a problem in any turnkey type of system.

Our only other complaint was that the operating systems provided each required at least 128K of RAM. This isn't really a terrible problem, considering the fact that this is such a high-powered system, but it would be nice to be able to start up with just a single 64K RAM board, even if just for test purposes.

Conclusion

The 68K is truly a generation ahead of most of the 8-bit machines commonly associated with the S-100 bus. Its powerful instruction set and high speed make it a versatile machine easily capable of multiuser, multitasking applications far in advance of those available in the 8-bit world. The CompuPro CPU-68K gives the advantages of the 68000 CPU to the S-100 bus without adding any limitations. It is particularly suited to interrupt-driven multiprocessor applications, and can perform these within the IEEE-696 specifications, which is no small design achievement. The CompuPro people really did their homework on the design of this board.

For more information, contact:
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The CompuPro CPU-68K gives the advantages of the 68000 CPU to the S-100 bus without adding any limitations.

HARDWARE REVIEW

The CompuPro System 8/16 Model 86/87 Computer

by Andrew L. Bender

Bill Godbout has built a solid reputation among the S-100 user community. This reputation has been earned by hard work and a dogged adherence to the IEEE-696 standard. Especially considering the contributions to the IEEE-696 standard made by Mark Garetz of the CompuPro staff, the entire product line is an advertisement for excellence in electronics. I was invited recently to use the CompuPro System 8/16 Model 86/87 as my development system; this report resulted from my experiences with the 8086 computer board, the 128K RAM-21, and a DISK-1 controller board. I also got a 3″ stack of manuals, two 8″ floppy disks containing CP/M-86, some headaches, and a peek at what level of system performance will result from the use of this board set. The Intel Corporation engineered and produced the 8086 microprocessor as one member of a 16-bit microprocessor series known as the iAPX-86/88 series.

Let me say at the outset that my review was impartial. Godbout had no idea that I would be receiving this board set, what I would use it for, and how or in what configuration I would put it together. I have no connection with Godbout Electronics, and I have had no communication with them during the time that I prepared this report. I did speak to Intel Corporation to get some information on the line of coprocessors for the iAPX-86 family, which I incorporated into this report. In order to get the information I did identify myself as a writer of "a feature article on the 8086."

The 8086 processor board

The 8086/87 board is marketed as the "CPU 86/87" in two grades. The normal grade board is assembled and tested and has a one-year warranty. A faster board with direct replacement service and a two-year warranty is available at a slightly higher cost under the CompuPro CSC (Certified System Component) program. If you know little about computers and don't want to be bothered with looking for someone to fix them, I would recommend purchase of CSC boards.

Both boards contain the 8086 processor, a socket for the 8087 math coprocessor, the 80130 "silicon operating system" support chip and the "glue" chips that make it work in the IEEE-696 environment. If you buy the board with the 8087 math coprocessor, the 8087 socket will, of course, contain this chip. I didn't have an 8087 chip on my board. Godbout states that although the board is field-upgradable to contain the 8087 chip, they very strongly recommend that you return it to them to have this chip installed. Because of the arbitration of signals between the 8086 and 8087, you cannot just plug in the 8087—some changes need to be made to the foil lands on the board to accommodate this additional processor. When you add the 8087, the 8086 cannot be operated at its full-rated speed of 8 MHz (10 MHz for CSC boards) because the fastest 8087 in current production runs at 5 MHz. This causes the overall performance of the board on non-8087 tasks to be degraded. If you do a lot of software development work such as text editing, compiling, and assembling, you are probably better off not dragging around the extra burden of a chip you won't often use.

The 8087 is a fantastic partner in cases where the 8086/87 would be employed as a digital filter, in complex signal processing, and in image processing or similar applications with a large computational overhead. This board, together with accurate analog-to-digital and digital-to-analog converters, has many applications in neurophysiological signal processing, and I was tempted to take my computer to the office to hook up to my electooculography equipment.

The 80130 chip, as marketed by Intel, usually contains a ROM with operating system firmware—normally the nucleus routines for Intel's proprietary operating system iRMX-86. In addition to the ROM, the 80130 also contains an interrupt controller similar in many respects to the 8259A and a set of interval timers similar to the 8253/54. Godbout supplies the 80130 chip, without the ROM, on his CPU 86/87 board so that all you get is the interrupt controller and the interval timers. The CPU 86/87 board is arranged so that if you want to use the 80130 chip *with* the iRMX-86 firmware or the 80150 chip *with* the CP/M operating system and BIOS I/O drivers in ROM, you can set the starting address of the firmware in a DIPswitch on the board. While some data on the 80130 was given in the manual, the assumption is that you will know all about this relatively new chip. It would have been better to reprint the technical data on the chip and include it in the manual.

The remaining chips on the board serve to interface the board with the S-100 bus. I used revision B of this board in my tests. Documentation was terse but complete. The usual section for "I can't wait to get it into my mainframe and running" freaks occupied the first page of the manual.

8086 architecture

The 8086, unlike its 8-bit counterpart, the 8088, fetches 8 or 16 bits per fetch from the data bus. There is a 6-byte instruction queue, rather than the 4-byte queue of the 8088. Like the 8088, instructions may be from one to four bytes in length. Unless a jump instruction occurs, the 8086 fully overlaps instruction fetch with instruction execution. These differences result in higher internal speeds for the 8086 and result in higher throughput. The instruction queue also lessens the demands on the memory bus. The 8- or 16-bit data bus fetch requires that the system contain word-wide memory. The 8088 always fetches 8 bits at a time from the data bus, so there is no problem in using your old memory boards. Enter the new CompuPro RAM-21 board. This board uses a programmed logic ar-

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ray to control all of the fetches possible, since it looks like two 64K static boards to an 8-bit system but a single word-wide 64K static board to a 16-bit system.

The 8086 interfaces with the outside world by means of address lines, data lines, and control signals. Intel Corporation has invested a considerable amount of effort in developing a complete line of coprocessors that compliment the iAPX-86 line of microcomputers. The 8087 is the best known of these coprocessor chips, but there are I/O processors, text processors, graphics display processors, even local area network processors—which all work with the iAPX-86 chip set. For the hardware hacker it should be possible to put one of these coprocessors on a little carrier board and plug it right into the 8087 socket.

The RAM-21 memory board

The board runs without wait status at 8 MHz. I didn't test it in a faster environment. The "B" version of the board that was supplied did not have any stated operating speed. Note that the board can be addressed only on a 128K boundary. It cannot be used in an 8-bit 808X system where MP/M II or CP/M-80 Plus is used, because there is no provision for the global memory needed in a banked system. There are no board options; a DIPswitch provides the start address for the memory board. The board is neatly laid out and constructed, with four regulator chips at the top of the board where the heat will go up and out of the enclosure instead of across all of those heat-sensitive chips. Since this board is not the focus of this review, I will not discuss it further.

The Disk-1 controller card

This disk controller card features a full 24-bit DMA transfer. Since there is no commercially available LSI DMA controller chip supporting 24-bit transfers, these are done with "glue." Lots of chips provide fully arbitrated, 24-bit DMA transfers from a floppy disk to the IEEE-696/S-100 bus. In addition to the floppy disk I/O functions, a serial I/O port is included on the Disk-1 card. This port, called the "bitbanger," is intended to be used only to "bring up a system," not as a standard serial I/O channel. The data are sent to the port by serializing them in software and then presenting them, one bit at a time, at a programmed speed so that the software takes the place of a hardware baud rate generator and UART. This technique, it might be remarked, was *the* way of doing serial I/O in the days when UARTs were expensive. The idea is that you can get the system up with the bit banger port on the Disk-1 card; you can then program the other hardware in your system to really get running. There is a major catch. The bit banger doesn't work with CP/M-86. You need a serial I/O port that is either on a CompuPro Serial I/O card or on the System Support Card.

The actual disk interface is through an Intel 8272 floppy disk controller chip. This chip allows a variety of sectoring choices and is an example of the latest in LSI circuitry. A reprint of Intel's 8272 chip data is presented in the Disk-1 manual.

The Disk-1 card requires that the system memory be phantomed out during booting. A 2716 EPROM on the Disk-1 board contains eight boot routines to be used with different hardware and software configurations. There is provision for adding wait states to the EPROM boot routines and to the DMA transfers by means of a DIP-switch and a jumper plug. Each of the boot routines is switch selectable by the user, but the EPROM is divided in two sections. One section is for the 8-bit processors such as the Z80, 8080, and 8085. The other section is for 16-bit processors such as the 8088 or 8086. One half of the eight-position DIPswitch selects the appropriate boot programs for a given processor, and a jumper plug sets the appropriate processor. The other half of the DIPswitch sets the priority of the Disk-1 board as a temporary bus master. Since the EPROM can be changed, you are not bound to the hardware routines in the boot EPROM.

The Disk-1 board layout is dense and neat; locations are clearly identified with silk-screen legends. The board is solder-masked on both sides and appears to have been wave soldered. Because of the density of the components on the board, some jumper plugs are hard to remove and insert, and a surgical "mosquito" clamp is a definite aid to changing these plugs. I used board revision "F" in these tests.

The controller can be used with $5^1/_4''$ or 8″ floppies. When minifloppies are used, it is necessary to make some minor alterations to the PC board. Computer House, 501 "B" Street, San Rafael CA, 94901 offers a version of MS-DOS on 8″ disk for the Disk-1 controller board and the 8086/87 CPU card. I did not have the opportunity to try this system.

Getting it all together

I brought my system up under CP/M-80, then switched it to CP/M-86 after a lot of problems of varying magnitudes. Headaches, which began with the statement that the bit banger port couldn't be used with a 8086/87 system, turned into real pain when I tried to configure my disks to use the Disk-1 card.

Though it would have been easy to plug in my CompuPro disk system and give a glowing report, it would not have been fair to a reader trying to decide whether it was worth going out, spending a fairly substantial sum, and configuring an 8086/87 system. I had two old Memorex 550 drives which are single-sided old beasts that have coexisted with my Micromation Doubler System. That system, second-hand when I bought it, has worked flawlessly for four years. The Memorex drives were not double sided, but since the preconfigured CompuPro CP/M-86 system only uses one side, it could be booted from them without being modified.

The memory-mapped Micromation controller card would not run with the high-speed 8086/87. It contains an EPROM with 8080 instructions that are executed by the CPU in order to perform memory-mapped disk transfers, and it was not designed to run at any speed above 4 MHz.

I had to modify the Memorex drives to allow the stepper motors to be energized forever, and jumpered and unjumpered some options that were not used on the Micromation system. A statement in the Disk-1 manual stuck in my mind ". . . they (the stepper motors) will get warm." Warm was a typical computerese understatement. They were damn near hot enough to fry an egg on! Yes, my drive box was well ventilated! Memorex does not recom-

What to run it in? You don't own an old shoebox? How about an old IMSAI? Well, unplug the front panel, plug in a terminator card, and it does run. But without the terminator, forget it! Too much noise and crosstalk.

mend keeping the stepper motors of the 550 floppy drive energized, but the 8272 disk controller scans the connected drives, requiring the stepper motors to be energized at all times. Finally I did get the thing to work, but only after a lot of tinkering with the software, and I admit that I got the system up with CP/M-80 2.2 running first. It was a big task to get CP/M-86 up after that, but not impossible—I mean, I did know that the Disk-1 board and drives were working properly when I saw the system boot CP/M-80.

Now, ready to try anything, I tried to get my ancient Altair/Pertec FD-400 drives up with the Disk-1 card. No luck. The Intel 8272 chip really needs the drives to look like Shugart floppies. The Altair drives have a Step In line and a Step Out line instead of a Step and Direction line. Having visions of adding little circuits to provide these functions to the Altair Buffer Boards in these drives, I quit this project.

The mainframe

What to run it in? You don't own an old shoebox? How about an old IMSAI? Well, unplug the front panel, plug in a terminator card, and it does run. Without the terminator? Forget it! Too much noise and crosstalk. It does run very well in the CompuPro Enclosure. It will run in an Altair 8800b without a front panel. Just leave the motherboard and power supply and add a terminator card. While writing this report, a power dip occurred. Both the IMSAI and CompuPro systems were powered up. The IMSAI crashed, but the CompuPro kept going. I guess that the constant-voltage transformer really does work.

Serial I/O

Now for the easy part: communications. You really need a device that will run at the speed of 8086/87 CPU. An old IMSAI 2S10/2 card won't work. Even correcting the board—so that it takes its address from the low-order eight address lines and its clock signal from the CLOCK, line 49, instead of $\Phi 2$, line 24—won't help. It's just too slow. The Altair 2SIO/2 was just as bad. It didn't work either. I tried the CPU 86/87 board with my PMMI modem card, and it did work. The CompuPro serial I/O boards, at least the Interfacer-1, work with it.

Summarizing the experience: For a novice it will be frustrating or impossible to get this three-board set working with older S-100 hardware. For an experienced hacker, it will not be a simple task but it can be done. I advise the use of a Godbout Interfacer-1 or System Support Card and a double-sided, double-density disk system to get the system up and running.

The stepper motors *will* burn out in any drives without proper cooling. The disk drive power supply must be adequate to handle the burden of those steppers being turned on at all times. The poorly designed disk power supply, whose +24 volt supply is marginal and designed with the idea that the steppers won't be used continuously, will not run reliably with the Disk-1 board, and that is a fact proven by trying several cheap disk cabinets and drives.

With respect to the software, I advise that if you are bringing up a non-CompuPro system, bring up CP/M-80 *first*. If you have little experience with bringing up CP/M, then just don't bother. Get someone to do it for you or buy the recommended hardware. If you are going to bring up CP/M-80, you will need the voluminous listings in the Disk-1 manual. You will be spending about 80 to 100 hours to get things working perfectly, including getting CP/M-86 up after CP/M-80. You will need a copy of Sorcim's ACT assembler and a good text editor. You will also need a lot of patience and the dogged determination of a real CP/M hacker who could bring up CP/M with GETSYS and PUTSYS. Don't work when tired. Good luck. The experience is worth it, but it can be frustrating.

Documentation

CompuPro manuals are OK but not great. The fact that the information is there is not a consolation. It is sometimes buried, hard to find, or discernable only by rereading material several times. I find myself becoming irritable and annoyed when the material is more disorganized than I remembered it to have been from my last reading. The manual is easy to read, but there isn't much text when you consider that there are the necessary software listings, circuit diagrams, and reprints of chip manufacturer's data sheets. The manuals need to be brought up to the quality of the electronics.

The Digital Research CP/M-86 manuals are as bad as the CP/M-80 manuals. They are just prettier. What can anyone say? It is all there—but try to find it. The same errors in the CP/M-80 manuals have found their way into the CP/M-86 manuals. The manuals, are, however, similarly disorganized, so that if you remember where the information was in the CP/M-80 manual set, you probably won't be disappointed with the CP/M-86 set. Thank God that all of the information (and I especially hope the jumbled presentation) is proprietary to Digital Research, including the errors—certainly no one else would lay claim to these manuals, perhaps the epitomy of poor writing. On the other hand, the Concurrent CP/M-86 manual for the IBM PC is well written, and its slick presentation makes you wish that DR had done the same for CP/M-86. While on that subject, I don't know who wrote the End User License Agreement; perhaps he or she could get a job in the technical writing department. The agreement is clearer than the manuals!

Getting it up and running

Not a task for the neophyte if you are using a mixture of CompuPro and non-CompuPro hardware. I suggest you buy your system from an authorized CompuPro dealer who can configure the system for you if you have little or no experience in this area.

I recommend the CompuPro hardware for several reasons: First, it is designed into the software. This is not a trick to make you buy the hardware. You can configure it yourself. It is rock-solid stuff with a very good warranty. Second, it is all *strictly* IEEE-696/S-100 hardware. There are no catch phrases, such as "complies with IEEE-696 . . . " or "compatible with S-100 systems." Third, Godbout stands behind his line. He has been in business for some time and has earned respect for his work.

Decide what you are going to use this hardware for. If it

The CompuPro hardware is rock-solid stuff with a very good warranty, and it is designed into the software.

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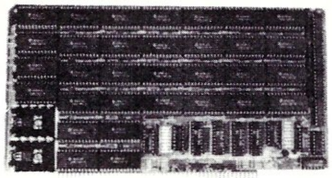

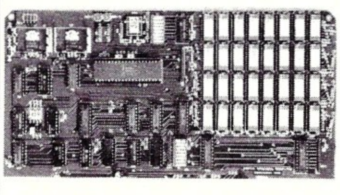

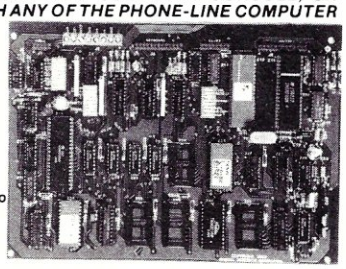

Model 86/87 continued . . .

is a serious and important use, then you don't want the stuff breaking down all the time. You will need to pay a bit more for this.

Testing

I used two configurations for testing. The first had an IMSAI mainframe with the original motherboard but the front panel removed. A terminator card was always used. The Disk-1 board drove two Memorex 550 drives reconfigured to match the proper requirements. A 64-Kword RAM-21 board, Interfacer-1, and CPU 86/87 was used. The second used a CompuPro Enclosure-2, CompuPro Disk Subsystem, and the same boards. There was no difference in performance, but the double-sided double-density Qume drives provided better throughput than the single-sided double-density Memorex 550s.

In closing, there is only one problem with 8086/8088 systems, and that is software. Most 8086/8088 software is reheated, warmed over, or mechanically translated 8080/Z80 code. None of this will show the virtue of the 8086 system to an advantage. Until the software base matures, most users will not gain a real advantage from the use of this excellent hardware.

For additional information, contact:

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An Introduction to Local Area Networks: Part II

by William G. Wong

In Part I of this article (*Microsystems*, October 1983) we examined the generalized model of a computer network provided by the ISO standard. We now consider aspects of implementing the model. This is the final article of a two-part series.

LAN topology, access methods, and protocols

Topology. Local area network topology, access methods, and protocols apply to the Data Link and Physical Layers on the ISO model. The three are related in that certain topologies dictate corresponding access methods and protocols. As mentioned before, the topology of a network may change depending upon the viewpoint. A description of basic network topologies is presented first, and is followed by a general description of the access methods and protocols. These facets will then be combined and described with regard to different viewpoints. The basic topologies are:

1. Bus
2. Fully Interconnected Point-to-Point
3. Irregular Point-to-Point
4. Star
5. Tree
6. Ring
7. Chain
8. Matrix

The Bus topology (Figure 1) is the simplest form. Every node is connected to a common communication link, usually serial in nature. Only one node can send information at one time, and all other nodes can receive the information. A node can check the destination of a particular message and simply ignore the information not destined for that node. The advantages of such a topology are: 1) connection to the bus is usually simple; 2) any node can send information directly to any other node. The disadvantages are: 1) only one node can send information at a time, which makes the bus a potential bottleneck if it has insufficient bandwidth; 2) the bus itself offers a single failure point that could halt the entire system.

The Fully Connected Point-to-Point system (Figure 2) is also a simple configuration. In this case, each node is connected to every other node in the system by a dedicated communications link. The advantage is that the communication between nodes is full duplex; that is, nodes can simultaneously send and receive information. It also offers the best throughput of any design, since there are many communication links within the network. Routing is easy, since information is sent directly to its destination and failure of a single link will not cause the entire network to fail. The disadvantage is that the cost and complexity grow at an amazing rate, making this configuration impractical for systems with more than 20 or so nodes. This is because the number of communication links per node is directly proportional to the number of nodes; thus the total number of links grows as the *square* of the number of nodes.

The Irregular Point-to-Point topology (Figure 3) is designed to reduce the number of physical connections, compared to that in a Fully Interconnected version, while keeping the reliability of the system high because the failure of a single link does not cause the entire system to fail. The disadvantage is that the routing of information becomes a very complex software problem, since information may have to be sent through other nodes to reach its destination. Going through one or more intermediate nodes increases the time required for a message to reach its destination and requires additional buffer space in each node for message forwarding.

The Star topology (Figure 4) is also simple and very similar to the Bus and Fully Interconnected Point-to-Point topologies. The Central Node can operate in one of two modes. In the first mode, the Central Node is analogous to the Bus in that all information will be sent from one node through the Central Node to the destination node. In the second mode, the nodes communicate only with the Central Node, which supplies services to them. The advantages are that the failure of a communications link will not cause the entire system to fail, and that the number of connections at a node is always one; this makes routing very simple. The disadvantage is that failure of the Central Node halts the entire system.

The Tree topology (Figure 5) is actually a hierarchical form of the Star topology. It has a simple routing scheme and is less vulnerable to failure of a communications link. It does have the disadvantage that messages often must go through intermediate nodes to reach their destination.

The Ring topology (Figure 6) is a simple connection method in which each node is attached to two neighbors. Routing is easy, since a message simply moves around the ring until it reaches its destination. Information is usually sent around the ring in only one direction; but this has the disadvantage that a failure of any node or communications link causes the whole ring to fail.

The Chain topology (Figure 7) is really a Tree topology where each node is restricted to having, at most, two communication links or a broken Ring topology. The advantages and disadvantages are the same as for the Tree topology. The Chain topology is often called the "daisy-chain" topology.

The final topology mentioned here is the Matrix topology (Figure 8). It is really a Regular Point-to-Point topology with the same advantages as the Irregular Point-to-Point topology; in addition, the routing procedure is very simple. The disadvantage is that a message usually goes through more than one node before it reaches its destination. Also, failure of a node or link makes the routing process as complex as for the Irregular Point-to-Point topology.

William Wong, 902 B Merritt Drive, Somerville, NJ 08876

Access methods. The network access methods are part fo the low-level physical operation of the network. Some access methods are simple, while others are very complex, with many dependencies. An access method is required when more than one node can request the use of a communications link at one time. There is an obvious need for an access method on a bus topology, but access methods can also apply to other topologies, depending upon their implementation.

The Point-to-Point, Tree, Chain, and Matrix topologies do not require an access method, since the communication links between nodes are dedicated. The Star topology also does not require an access method if the nodes communicate only with the Central Node, and the Ring topology does not need an access method if messages can be passed from one node to another at any time. This leaves the Star topology, where the nodes communicate with each other through the Central Node, some implementations of the Ring topology, and the Bus topology.

The Star is actually a very familiar system which is often supplied by the telephone company. The simplest form of this system is called a Private Branch Exchange (PBX). This is a switching system which allows nodes (telephones in some cases) to be connected together. The access method is the procedure to make or break a connection.

The Bus and Ring topologies are those usually discussed with regard to LANs, and they are also the two which have the largest number of different access methods. It turns out that both can use the same types of access methods. This is because a ring operates essentially like a bus if only one node can send information at a time and data always traverses the entire ring once. The three access methods for these two topologies, illustrated in Figure 9, are:

1. Time division multiplexing
2. Token passing
3. Carrier sensing

Time-division multiplexing operates in a synchronized fashion, where each node is allocated a fixed time slot within a predefined cycle. A node can send a message to another node during its time slot. This method allows for synchronization, total access by any node, and priority messages. It is usually used in GANs, since transmission occurs at a predefined time. The disadvantage is that the bandwidth of a channel may not be fully utilized.

The token-passing access method uses a logical item called a token, which is passed from node to node. The token is usually a short, specially formatted message. The node which has the token can either send a message to another node or send the token to another node. Only the node containing the logical token can send a message.

The token-passing access method can provide priority control by having the token passed to high-priority nodes more often than to low-priority nodes. This method also provides high channel utilization, since token passing requires little overhead and all remaining time can be used to send information. An important advantage in some instances is that the message delay time may vary with system loading, but will usually be less than the upper delay limit. The token-passing method also operates more efficiently if most nodes send large bursts of information at long time intervals.

The disadvantage of the token access method is its complexity. The nodes must be able to distinguish the token from other messages. There must also be a method of generating a new token if the current one disappears. This can happen for a number of reasons, including noise on the communication links. Adding active nodes to the system can also be a problem, since a token is sent only to an active node which is known, and newly activated nodes are ignored.

The carrier sense access methods are also called Carrier Sense, Multiple Access (CSMA) methods. They do away with many characteristics that are disadvantageous for the token-passing access method, but pick up others that are advantageous. The carrier sense access method is very simple. A node wishing to send a message will first listen to the communications link. It will send the message if a message is not currently being sent; otherwise, it will wait until transmission of the other message is complete before sending the message.

Two problems can occur when two nodes wish to send a message at the same time. In the first case, both nodes see an inactive link and immediately start to send their messages. In the second case, they both see the end of a message just sent by a third node and again begin sending simultaneously. In both cases the result is a garbled message. This is called a collision. Notice that a collision will only occur for the two cases mentioned, and not while a message is being sent; so the problem does not occur all the time. The collision problem can be resolved in two ways.

The first is called Carrier Sense, Multiple Access/Collision Avoidance (CSMA/CA). This method simply tries to make the time that a collision can occur as small as possible, has an easy and reliable way to detect garbled messages, and requires that messages be acknowledged by the destination. The first two items can be done in hardware and the latter in either hardware or software. A message is retransmitted if no acknowledgement is received. This is the simplest CSMA method.

The second method is called Carrier Sense, Multiple

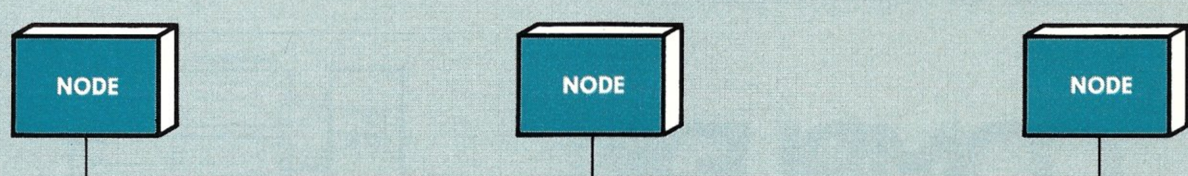

Figure 1. Bus topology.

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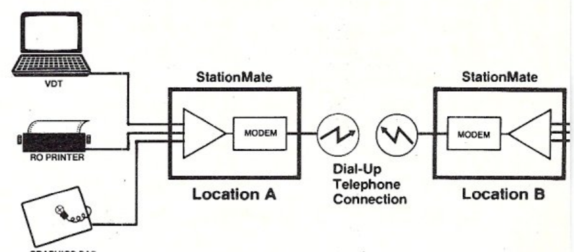

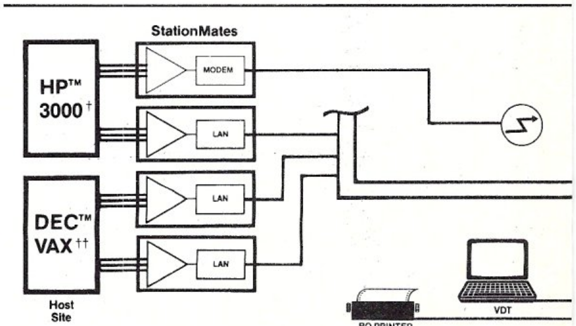

Local Networking

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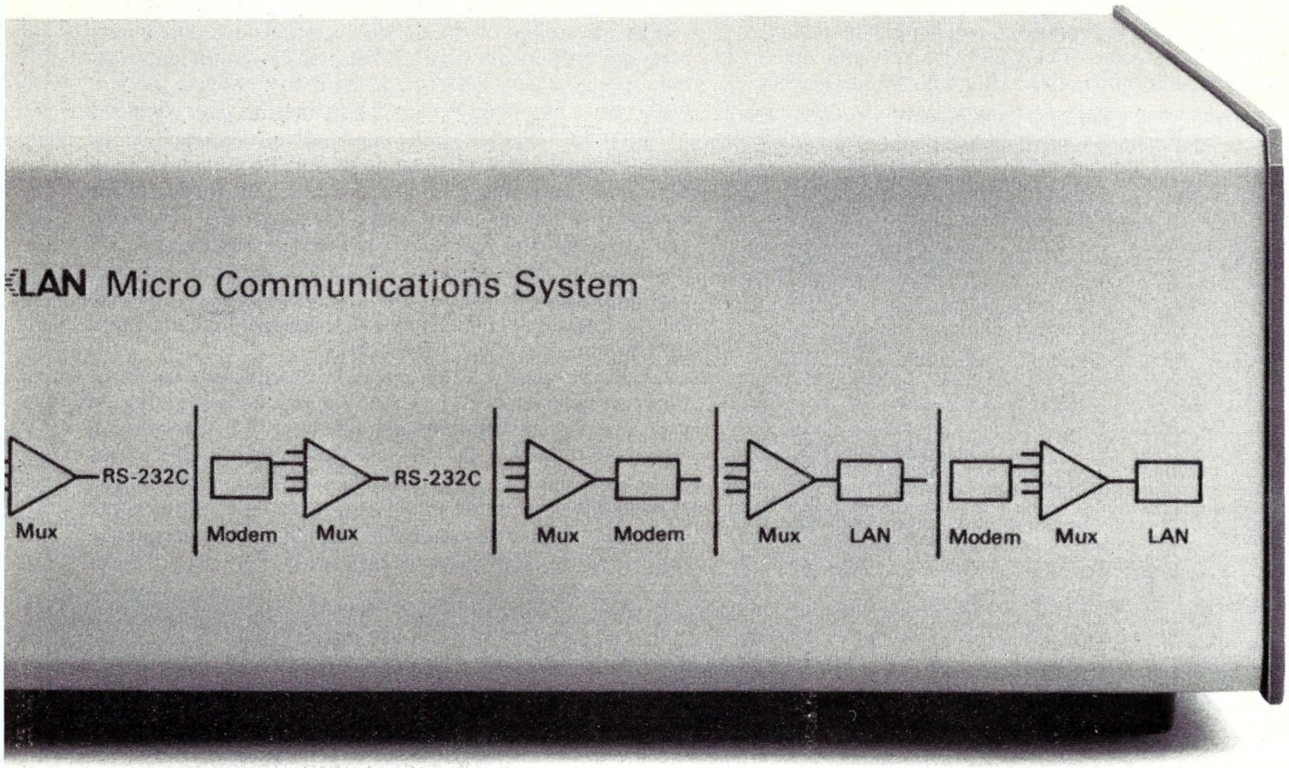

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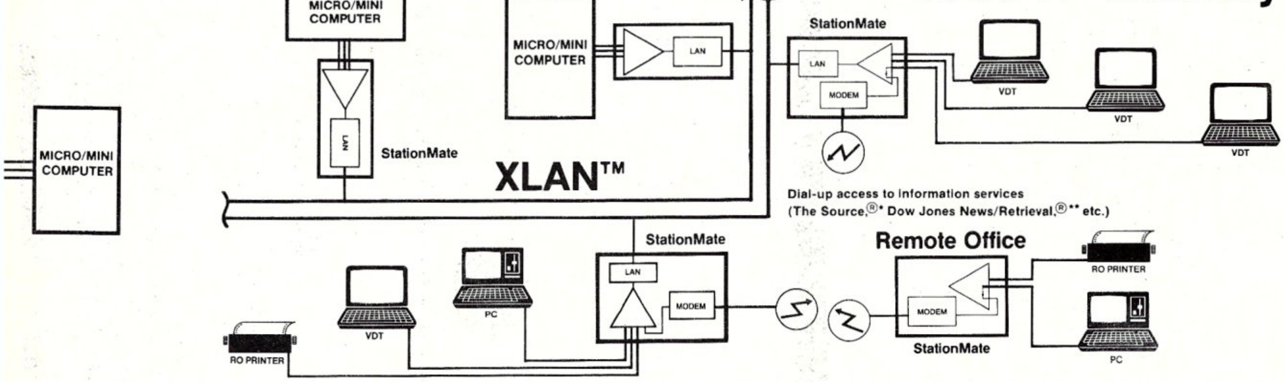
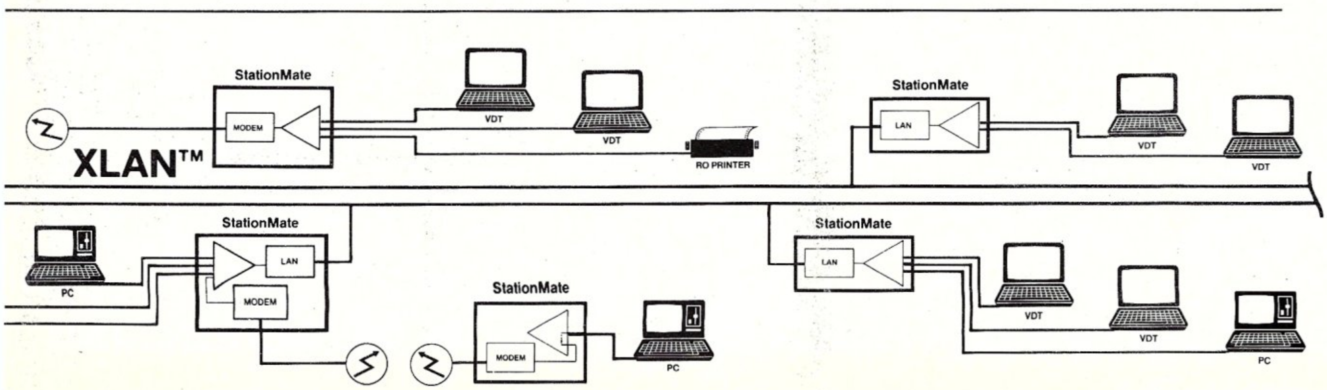




Access/Collision Detection (CSMA/CD). In this case, each node will listen to the link while it sends its message. The message will be aborted (by sending a special abort sequence) if the message heard on the link does not match the one being sent. The advantage of this method over the CSMA/CA is that garbled messages will be terminated as soon a collision is detected. The CSMA/CA wastes time by continuing to send information after a collision has occurred. The additional collision detection hardware usually adds to the cost of the network interface. The CSMA/CD method normally includes a random delay period before retransmission of a message is started, to prevent the same two nodes from repeating the process.

The advantage of the CSMA methods are that bursty message traffic from nodes is handled in an efficient manner. It is also very easy to add an active node to the network, since any node can send information after checking to the communications link. The disadvantages include the lack of priority control, a nondeterministic maximum message delay time, and less than maximum utilization of the communication link bandwidth, although the utilization can approach the optimal. It is theoretically possible for one node to wait forever to send a message, but this does not happen in practice. In fact, the typical maximum message delay time is usually low if the communication link utilization is less than 50 percent.

On a Bus topology, the type of bus technology used further complicates the decision on the best access method to use. The two possibilities are baseband and broadband. Baseband indicates that a single physical communications link can be used for one message at a time. A broadband system allows a single physical link to be used for more than one message at a time. This is achieved by frequency multiplexing. Different messages are sent on different

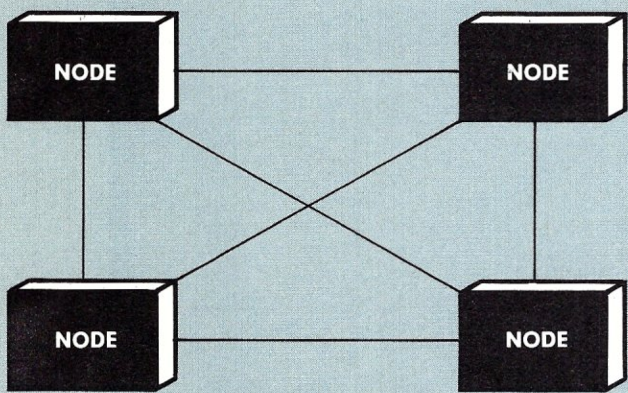


Figure 2. Fully connected point-to-point.

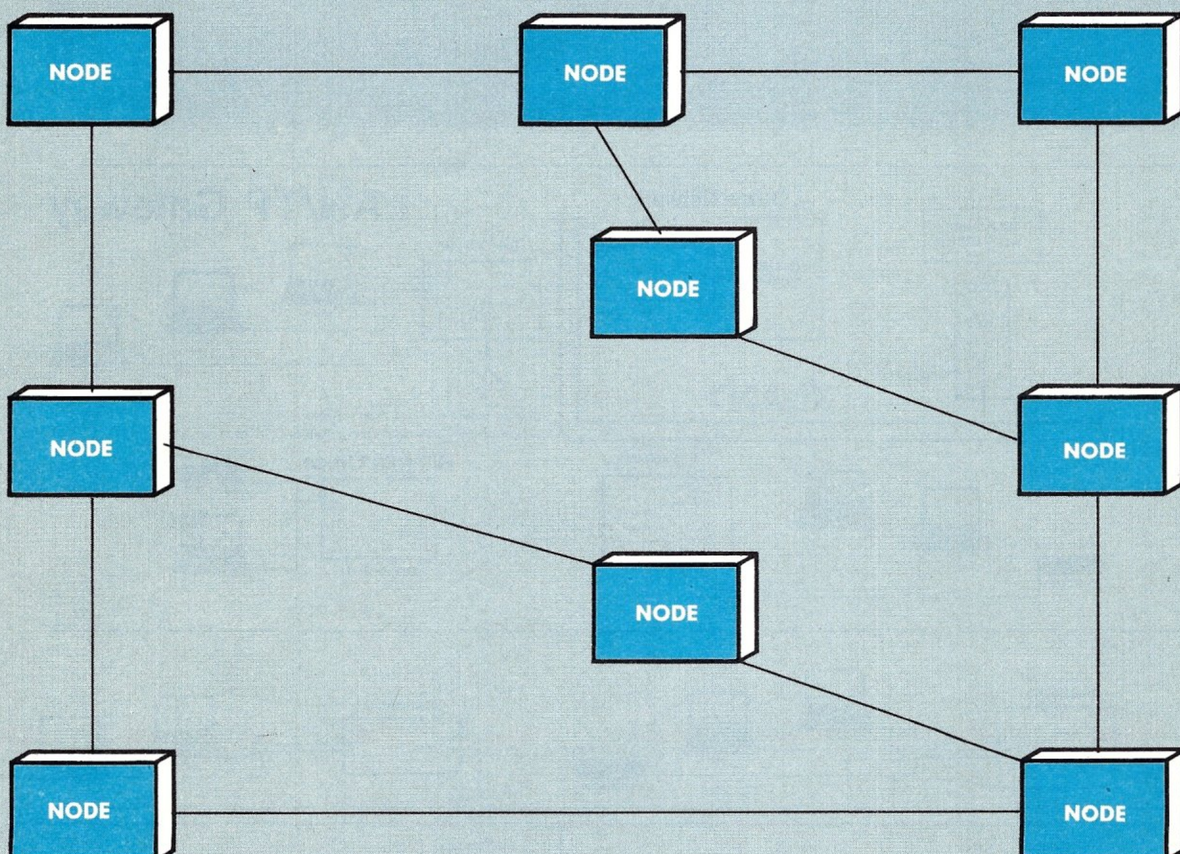
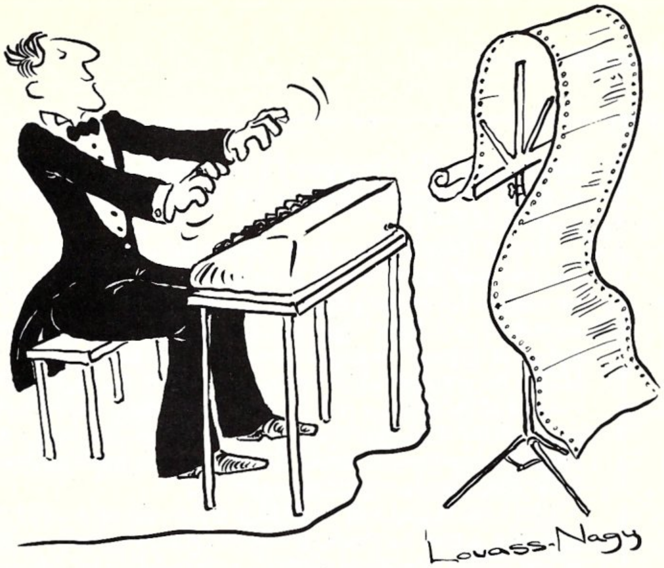


Figure 3. Irregular point-to-point topology.


Lovass-Nagy

channels that do not interfere with each other. A channel is a range of frequencies that does not overlap those of another channel. Television channels are a good example of a broadband channel. In fact, broadband systems use technology from the cable attached television (CATV) systems. The broadband systems have the advantage of higher data-transfer rates, the ability to send voice, video, and data on different channels, and the ability to use different access methods on different channels. The disadvantage is that the system cost and complexity are significantly higher than those of baseband systems.

Protocols. Finally, there are the network protocols that are used on the communication link once the communication link has been accessed. Protocols address the message format and the message exchange procedures. Message format protocols can be divided into byte-oriented and bit-oriented protocols. These differ primarily in the way the data portion of the message is handled.

The bit-oriented protocols are usually based on the High Level Data Link (HDLC) protocol, of which the Synchronous Data Link Control (SDLC) protocol is a subset. SDLC is the bit-oriented protocols for IBM's Systems Network Architecture (SNA). The bit-oriented protocols use a special bit sequence to indicate the idle state (in which no message is being sent), and a special flag sequence indicating the start of a message. A technique known as "bit-stuffing" is used to keep any data from looking like either a flag or an idle sequence. A message usually has the following parts:

1. Flag indicating the start of a message
2. Destination address
3. Control information
4. Data which may include the source address
5. Error detection information such as a cyclic redundancy check (CRC) item
6. Flag indicating the end of a message

The destination address and control information consist of one or more bytes; the CRC is usually two bytes; and the flag is a special bit sequence. The data section can be any number of bits and is usually not restricted to an integral number of bytes.

Byte-oriented protocols do restrict the data section to an integral number of bytes, and there is normally a special procedure for sending arbitrary binary data, since the flag sequence and CRC information are specially encoded bytes. A typical example of a byte-oriented protocol is IBM's Bisynch protocol. Special bytes are used to indicate the end of the data section. Multibyte sequences are used to send binary data that is the same as the special bytes. Alternative systems use either a fixed size or additional bytes indicating the size of the data section.

More confusion will be introduced as the nice set of topologies, access methods, and protocols are mixed together into some sample networks and viewed from different vantage points. The first view is how the nodes are positioned, the second is now the nodes are connected by the communication link, and the third is how the protocol and access methods work.

The simplest case is where the view of the system is always a bus, always a ring, and so on. Unfortunately, the number of other combinations is very large, and many of them are useful and practical implementations. For example, the nodes may be positioned in a daisy-chain mode, while the communications link forms a bus. Finally, the token-passing access method is used, forming a logical ring. Figure 10 shows this structure.

And just to show that this is not a fluke, one of the proposed IBM LAN implementations uses a token-passing access method with a ring communication link and a star topology with respect to the node positions, as shown in Figure 11.

The token-passing view is the ring that matches the connection view of the communication link. The reason for using this architecture is that the central node would have special connectors that would know when a node is not connected (either logically or physically) and close the

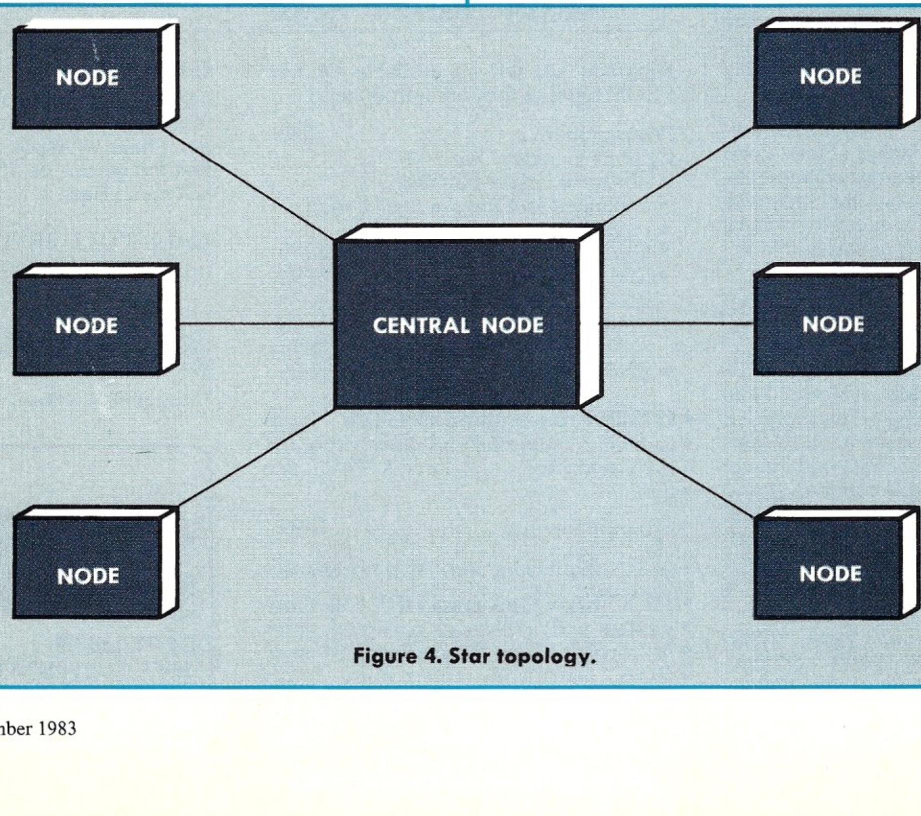


Figure 4. Star topology.

ring. This prevents the failure of the entire system if either a node or a communication link fails; nevertheless, a failure in the central node still causes the entire communications network to become inoperative.

Network standards

The IEEE 802 committee is currently working on standards for the Data Link and Physical Layers of the ISO network model. The standards are based upon the Bus and Ring topologies for the communication link. CSMA/CD and token passing are the two access methods being defined in conjunction with these topologies. Table 1 shows a summary of the committee's recommendations. The channel size on the broadband systems indicates the bandwidth of one channel on the communications link.

Notice that the three basic standards (P802.3, P802.4, and P802.5) define a range of implementations in terms of transmission speed and connection media. The standards follow existing implementations when possible. For example, the CSMA/CD bus implementation by Xerox is called Ethernet, and this essentially matches the P802.3 standard with a baseband, coaxial design running at 10 megabits per second (Mbps). Ethernet is a de facto industry standard baseband LAN that is implemented by a number of vendors other than Xerox.

Standards already exist for the point-to-point communication links. These include the Electronic Institute of America (EIA) standards such as the famous RS-2320 standard, and the RS-422 and RS-423 standards. The current set of standards deal with the lowest levels of the ISO model. The next section deals with some of the services that may be provided at the higher levels, even though standards do not exist in these areas.

Table 1. IEEE 802 Committee Recommendations

1. CSMA/CD (P802.3)
   a. Baseband coaxial cable (1, 5, 10, 20 Mbps)
   b. Broadband (10 Mbps, 6 MHz channel)

2. Token passing
   a. Bus (P802.4)
      1. Baseband
         a. Phase continuous coaxial cable (1 Mbps)
         b. Phase coherent coaxial cable (5, 10 Mbps)

      2. Broadband
         a. 1.544 Mbps (4, 6 MHz channel)
         b. 5 and 10 Mbps (6 MHz channel)
         c. 10 and 20 Mbps (12 MHz channel)

   b. Ring (P802.5)
      1. Baseband shielded twisted pair (1.4 Mbps)
      2. Broadband coaxial cable (4, 20, 40 Mbps)

Node services

The purpose of a LAN is to provide the communications link between the nodes within a LAN so nodes can provide services and resources to other nodes within the LAN. Some of the generic names given to services that can be provided by nodes in a LAN are:

1. User interface
2. Compuational server
3. File server
4. Print server
5. Communication server
6. Gateway server

A node in a LAN may provide one or more of these services to users at the node or other nodes within the LAN, depending upon the implementation. The term "server" is often interchanged with "node" when a node provides only that service: e.g., computational server and computational node. Other terms are used to refer to combinations of services provided at a node.

The use interface is typically a keyboard and display or

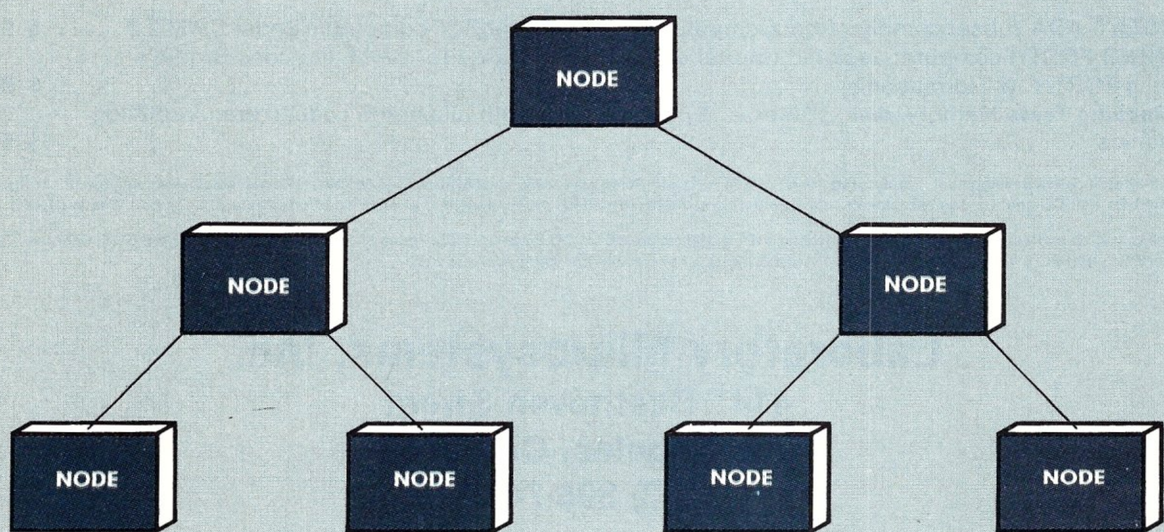


Figure 5. Tree topology.

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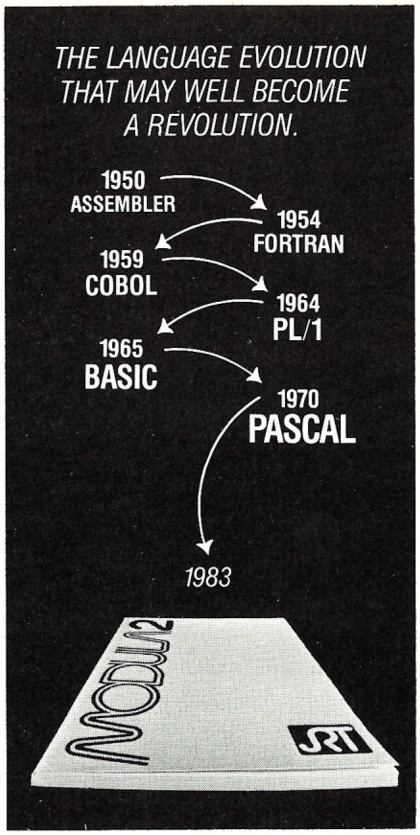

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printer. It is often combined with other services in the form of a personal computer, or it may be a simple computer terminal which must be logically attached to other servers in the LAN. In either case, the purpose is to allow a user to enter information and receive results.

A computational server is the usual computer, less peripheral interfaces. It consists of a processing unit and memory. This is where programs initiated by a user are run. Typical programs include applications such as order entry, program compilation, and word processing. Diskless workstations in a LAN often include a user interface and a computational server. Note that the memory in a computational server is usually small and volatile in comparison to that of a file server, and therefore not suitable for long-term storage.

The file server provides the memory function for large amounts of data over long periods of time. A file server usually manages resources consisting of a hard disk and corresponding backup facility. The way the file server manages these resources can differ significantly, depending upon implementation. Any file server implementation can usually be categorized as one of the following:

1. Paritioned file server
2. Shared file server
3. Data base server

A partitioned file server (Figure 12) divides its resource into one or more partitions. A node can access a partition and the files within the partition; however, another node cannot access the same partition at the same time unless all parties are allowed read-only access. This is the implementation normally used for LANs which have simple but different operating systems running on the computational servers. A partition is usually allocated to only one of the operating systems at a time. The advantage is that the hard disk resource and associated backup can be shared among a number of nodes running different operating systems. The disadvantage is that running a shared data base is difficult, since controlled simultaneous access and update by many nodes is not possible.

A shared file server (Figure 13) may divide the hard disk into a number of partitions, but the files within a partition can be accessed and updated in a controlled fashion by different nodes at the same time. This usually requires that a more sophisticated operating system be run in the computational servers, with additional sophistication in the file server. Typical implementations usually restrict the computational servers to the same operating system. A good example would be the CP/NET system from Digital Research. A mix of different operating system partitions on a shared file server is theoretically possible; however, such implementations do not currently exist.

The data base server (Figure 14) is a more complex animal than the previous file servers mentioned. These presented a file system to the computational servers which could be manipulated by programs; however, any data base operations would have to be done by the computa-

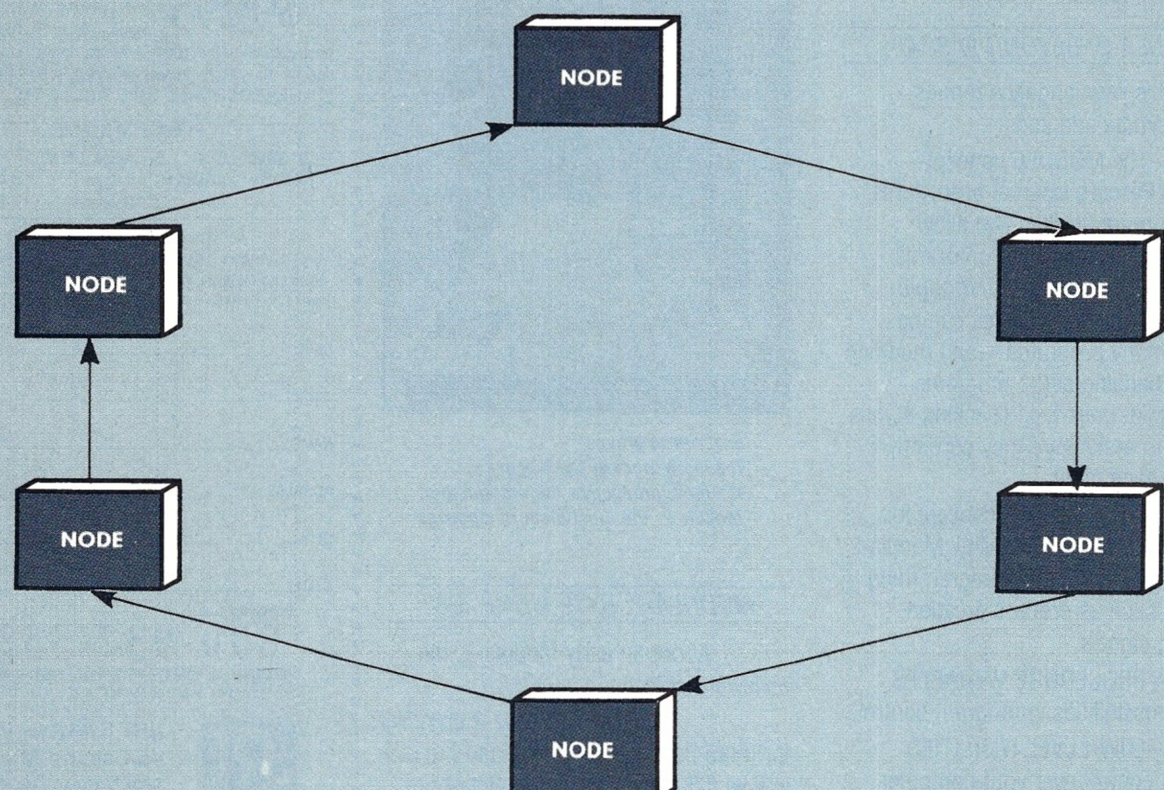

Figure 6. Ring topology.

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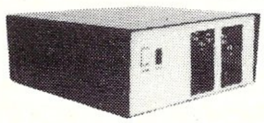

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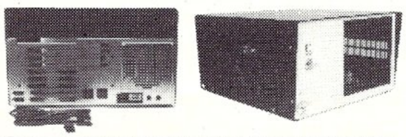

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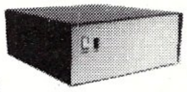

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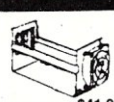

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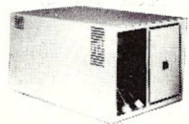

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CIRCLE 39 ON READER SERVICE CARD

tional server which must also control the integrity of the data base through the use of file and record locks. The data base server relieves the computational server of this work by preserving data base integrity itself. This higher level interface allows different operating systems and language access to a common data base. The advantage of such a system is its power and flexibility, but there is a significant increase in complexity and cost—which is why data base servers are currently used only in the more expensive systems.

A print server is an interesting system which provides a printer as a resource. It can be driven by information from a computational server, but a print server configured as a node usually operates in a different fashion. In this case, the print server normally receives requests to print files which reside in a file server. More complex print servers will receive information from other nodes and route it to a file server if the printer is currently in use. The file created will be added to the list of files to be printed. This is called print spooling. A print server allows the resource to be shared efficiently, since the printer will be in constant use if sufficient files exist to be printed.

A communication server and a gateway server are similar animals. They are used to connect a node or LAN to an external node or LAN. A communication server normally implies a connection to the remote system with the node acting as an IBM 3101, IBM 3270 or IBM 3780 terminal. A computational server normally emulates the terminal in conjunction with the communication server and a user interface. A gateway server allows for a more complex connection between nodes in a LAN and the outside world. In this case a logical link can be made between a node in the LAN and a node outside the LAN, over which communication between the two proceeds as if both nodes were in the same LAN. A communication server requires a node to use the protocol of the terminal being emulated, while the gateway server allows a node to use the LAN protocol.

LAN implementations

This section briefly presents some of the existing hardware and software implementations of various portions of the ISO model. Table 2 gives a larger set of existing implementation in less detail. This is not an exhaustive study, however. Four implementations will be described briefly. These are: Ethernet, Ominet, ARCnet, and CP/NET.

The foremost implementation to date is probably the Xerox Ethernet, which matches the IEEE 802.3 standard (10 Mbps, CSMA/CD, coax bus). The Ethernet specification applies to the Physical and Data Link layers of the ISO model. It has a data rate of 10 million bits per second, a maximum node separation of 2.5 kilometers, up to 1024 nodes, and uses a passive shielded coaxial cable operating with baseband signaling. The passive aspect of the system is important in that no particular node need be active to keep the system running. This, along with the high reliability of coaxial cable, leads to a highly fault-resistant system.

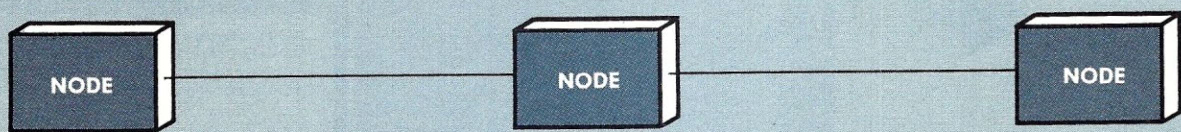

Figure 7. Chain topology.

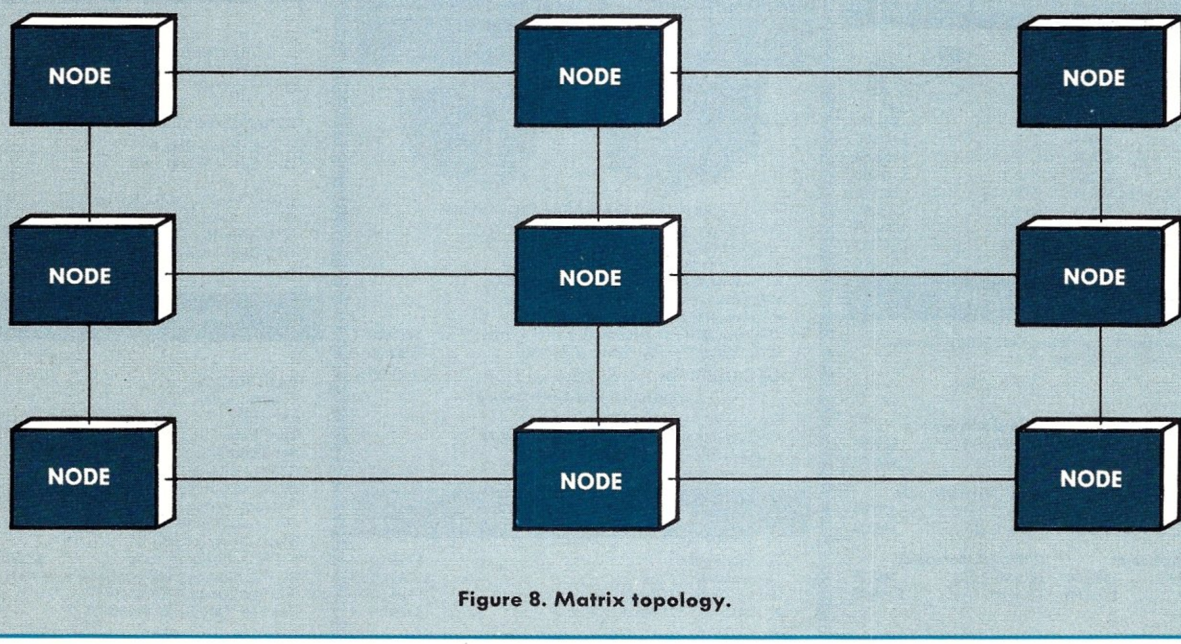

Figure 8. Matrix topology.

Z80 Software

SOFTWARE DESCRIPTIONS

TPM (TPM I) - $80 A Z80 only operating system which is capable of running CP/M programs. Includes many features not found in CP/M such as independent disk directory partitioning for up to 255 user partitions, space, time and version commands, date and time, create FCB, chain program, direct disk I/O, abbreviated commands and more! Available for North Star (either single or double density), TRS—80 Model I (offset 4200H) or II, Versafloppy I, or Tarbell I.

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CONFIGURATOR I

This package provides all the necessary programs for customizing TPM for a floppy controller which we do not support. We suggest ordering this on single density (8SD).
Includes: TPM-II ($125), Sample PIOS (BIOS) SOURCE ($FREE), MACRO II ($100), LINKER ($80), DEBUG I ($80), QED ($150), ZEDIT ($50), TOP I ($80), BASIC I ($50) and BASIC II ($100)
$815 Value NOW $250

CONFIGURATOR II

Includes: TPM-II ($125), Sample PIOS (BIOS) SOURCE ($FREE), MACRO II ($100), MACRO III ($150), LINKER ($80), DEBUG I ($80), DEBUG II ($100), QSAL ($200), QED ($150), ZTEL ($80), TOP II ($100), BUSINESS BASIC ($200) and MODEM SOURCE ($40) and DISASSEMBLER ($80)
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MODEL I PROGRAMMER

This package is only for the TRS-80 Model I. Note: These are the ONLY CDL programs available for the Model I. It includes: TPM I ($80), BUSINESS BASIC ($200), MACRO I ($80), DEBUG I ($80), ZDDT ($40), ZTEL ($80), TOP I ($80) and MODEM ($40)
$680 Value NOW $175

MODEL II PROGRAMMER

This package is only for the TRS-80 Model II. It includes: TPM-II ($125), BUSINESS BASIC ($200), MACRO II ($100), MACRO III ($150), LINKER ($80), DEBUG I ($80), DEBUG II ($100), QED ($150), ZTEL ($80), TOP II ($100), ZDDT ($40), ZAPPLE SOURCE ($80), MODEM ($40), MODEM SOURCE ($40) and DISASSEMBLER ($80)
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BASIC II - $100. A 12 digit precision version of Basic I.

BUSINESS BASIC - $200. A full disk extended basic with random or sequential disk file handling and 12 digit precision (even for TRIG functions). Also includes PRIVACY command to protect source code, fixed and variable record lengths, simultaneous access to multiple disk files, global editing, and more!

ACCOUNTING PACKAGE - $300. Written in Business Basic. Includes General Ledger, Accounts Receivable/Payable, and Payroll. Set up for Hazeltine 1500 terminal. Minor modifications needed for other terminals. Provided in unprotected source form.

MACRO I - $80. A Z80/8080 assembler which uses CDL/TDL mnemonics. Handles MACROs and generates relocateable code. Includes 14 conditionals, 16 listing controls, 54 pseudo-ops, 11 arithmetic/logical ops, local and global symbols, linkable module generation, and more!

MACRO II - $100. An improved version of Macro I with expanded linking capabilities and more listing options. Also internal code has been greatly improved for faster more reliable operation.

MACRO III - $150. An enchanced version of Macro II. Internal buffers have been increased to achieve a significant improvement in speed of assembly. Additional features include line numbers, cross reference, compressed PRN files, form feeds, page parity, additional pseudo-ops, internal setting of time and date, and expanded assembly-time data entry.

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DEVELOPER II

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Includes: QSAL ($200), QED ($150), BUSINESS BASIC ($200), ZTEL ($80) and TOP II ($100)
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COMBO

Includes: DEVELOPER II ($1280), ACCOUNTING PACKAGE ($300), QSAL ($200) and 6502X ($150)
$1930 Value NOW $500

LINKER - $80. A linking loader for handling the linkable modules created by the above assemblers.

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QED - $150. A screen editor which is both FAST and easy to learn. Commands include block delete, copy, and move to a named file or within text, repeat previous command, change, locate, find at start of line, and numerous cursor and window movement functions. Works with any CRT having clear screen, addressable cursor, clear to end of line, clear to end of screen, and 80X24.

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When ordering software specify which disk format you would like.

CODE	DESCRIPTION
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8DD	8" Double Density (256 bytes/26 sectors/77 tracks)
8XD	8" CDL Extended Density (1024 bytes/8 sector/77 traceks 616K)
5SD	5.25" Single Density (TRS80 Model I, Versafloppy I, Tarbell I)
5EP	5.25" Epson Double Density
5PC	5.25" IBM PC Double Density
5XE	5.25" Xerox 820 Single Density
5OS	5.25" Osborne Single Density
5ZA	5.25" Z80 Apple (Softcard compatible)

TPM INFO When ordering TPM I or II, in addition to Disk Format, please specify one of the following codes:

	CODE	DESCRIPTION
TPM I:	NSSD/H	North Star Single Density for Horizon I/O
	NSSD/Z	North Star Single Density for Zapple I/O
	NSDD/H	North Star Double Density for Horizon I/O
	NSDD/Z	North Star Double Density for Zapple I/O
	TRS80-I	TRS-80 Model I (4200H Offset)
	TRS80II	TRS-80 Model II
	VI8	Versafloppy I 8"
	VI5	Versafloppy I 5.25"
TPM-II:	VII8	Versafloppy II 8" (XD)
	VII5	Versafloppy II 5.25"
	TRS80II	TRS-80 Model II (XD)

ZTEL - $80. An extensive text editing language and editor modelled after DEC's TECO.

ZEDIT - $50. A mini text editor. Character/line oriented. Works well with hardcopy terminals and is easy to use. Includes macro command capability.

TOP I - $80. A Text Output Processor for formatting manuals, documents, etc. Interprets commands which are entered into the text by an editor. Commands include justify, page number, heading, subheading, centering, and more.

TOP II - $100. A superset of TOP I. Adds: embedded control characters in the file, page at a time printing, selected portion printing, include/merge files, form feed/CRLF option for paging, instant start up, and final page ejection.

ZDDT - $40. This is the disk version of our famous Zapple monitor. It will also load hex and relocatable files.

ZAPPLE SOURCE - $80. This is the source to the SMB ROM version of our famous Zapple monitor. It can be used to create your own custom version or as an example of the features of our assemblers. Must be assembled using one of our assemblers.

MODEM - A communication program for file transfer between systems or using a system as a terminal. Based on the user group version but modified to work with our SMB board or TRS-80 Models I or II. You must specify which version you want.

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APPLE II — Chairman Z80 $345. Add Z80 capability to your Apple II/II Plus computer. Runs CP/M programs with our more powerful TPM. Includes 64K memory add on (unlike the competition this is also useable by the 6502/DOS as well as the Z80), TPM, QSAL assembler, QED Screen Editor, and Business Basic. Mfr'd by AMT Research.
Apple Special $175. Buy the Apple Z80 Developer at the same time as the "Chairman" and pay only $175 instead of $325.

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CIRCLE 84 ON READER SERVICE CARD

The logical communication topology is a bus, but the physical topology can be a bus or a non-rooted tree, which means there need not be a central connection of any sort.

The Ethernet Data Link Layer has fully distributed control of the bus by using the CSMA/CD access method. Detection of a collision causes a node to send a jamming signal to notify all nodes that a collision has occurred. The Ethernet packets are variable length with the following format:

Field Description	Size
Destination address	6 bytes
Source address	6 bytes
Type	2 bytes
Data	46 bytes to 1500 bytes
Frame check sequence	4 bytes
Total	64 bytes to 1518 bytes

The Ethernet uses self-clocking Manchester bit-encoding on the bus. A special prefix is sent at the beginning of each packet to synchronize the clocks at each node. Synchronization should occur before the destination address field reaches a node.

The most significant bit of the destination address field is the multicast bit. A zero value indicates that the packet is destined for a single node, while a one indicates that the packet may be destined for multiple nodes. The source and destination address fields allow for significantly more node addresses than the maximum number of nodes specified in the standard. This allows for expansion and an easy interface between Ethernet LANs via gateway nodes. Allocation of addresses is even being handled by Xerox to prevent duplication of addresses when using equipment from different vendors. The large address fields should provide for all cases.

The type and data field are available for use by the other levels in the ISO model and their format is not specified by the Ethernet standard. The fields may contain any data.

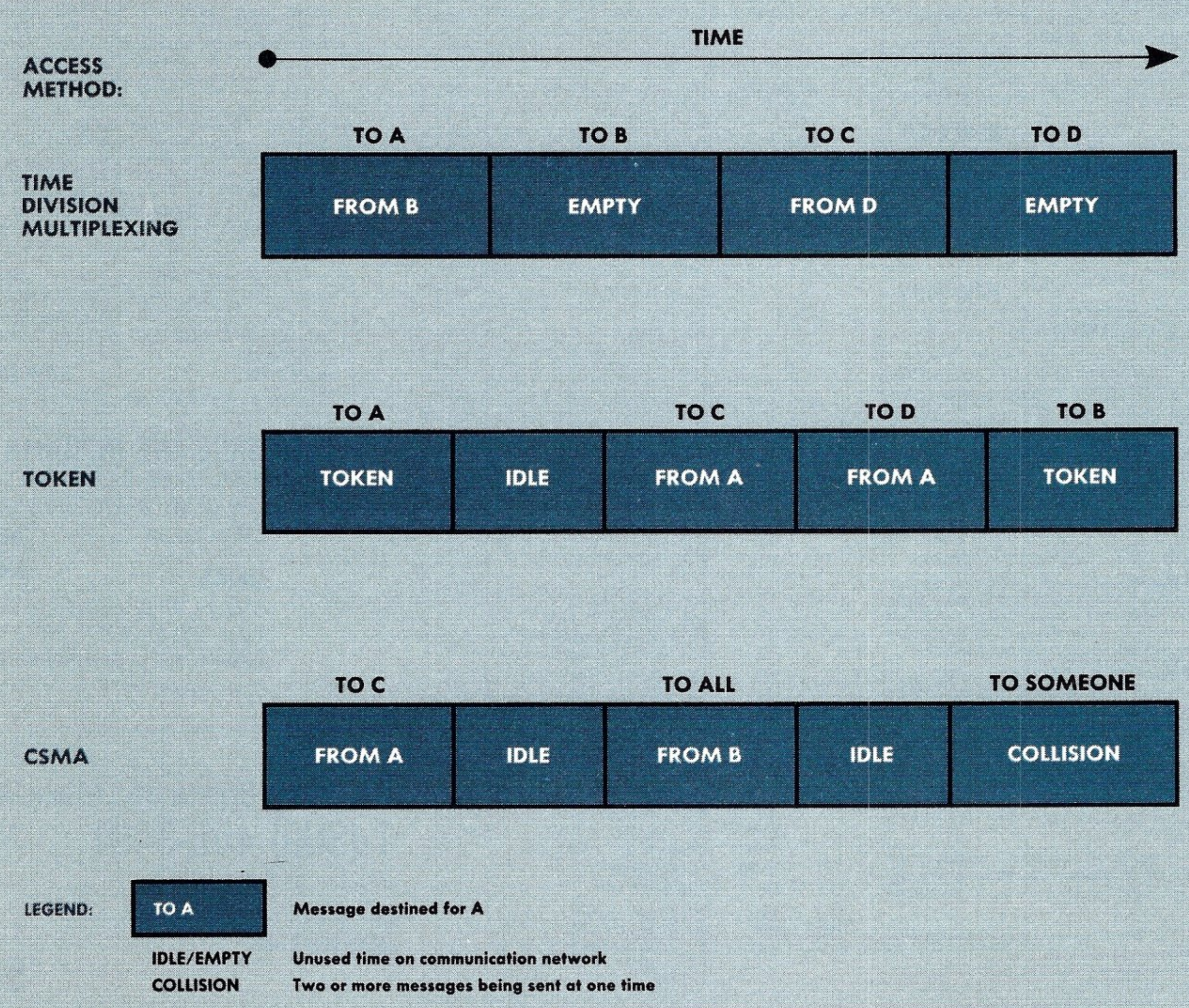

Figure 9. Three access methods.

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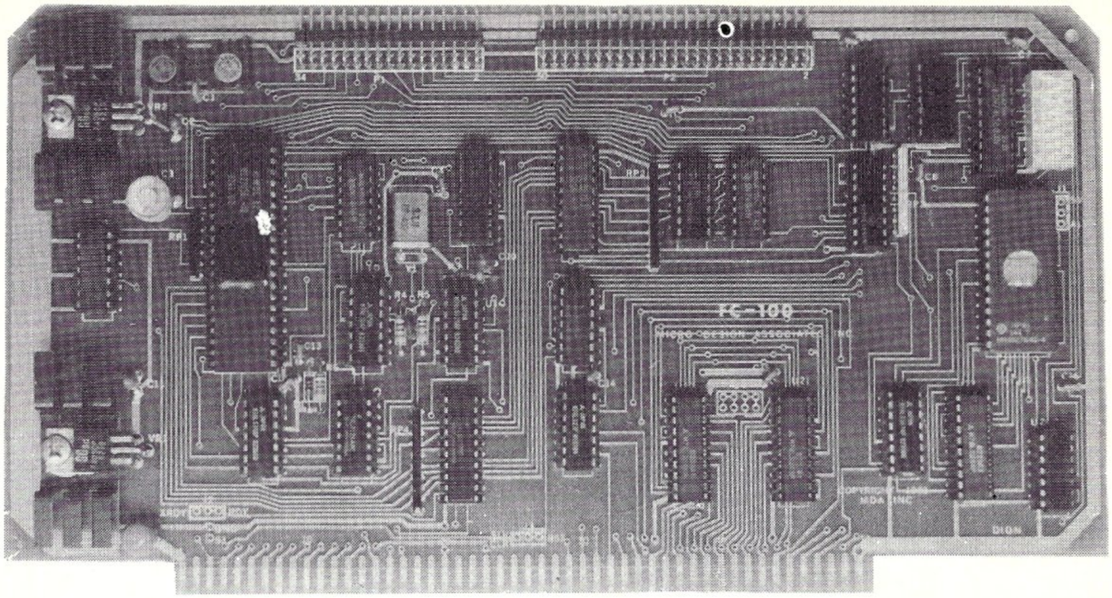

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The reason for the minimum data field size is to keep a minimum packet length. This is required because transmission mode is being used. It takes some small amount of time for a signal to propagate from one end of the coaxial cable to the other and this time is significantly longer than the time for one bit of information to be sent on the Ethernet. This means that a node will be sending a later part of the packet when the first bit of the packet reaches the end of the cable.

This phenomenon becomes important when considering the CSMA/CD access method. If two nodes at opposite ends of the bus send a packet at about the same time, causing a collision, then they should be able to detect the collision and send the jamming signal. They can only do this consistently if both nodes are transmitting when the first bits from the other packet reach them, hence the minimum packet size. The maximum packet size is a matter of overall system efficiency. Longer packets are more susceptible to errors caused by noise; the longer retransmission time reduces overall system throughput. The maximum data field size is larger than 1024, which is a convenient size for a block of computer information, thereby allowing additional information describing the contents of the data field.

The frame check sequence is a 32-bit cyclic redundancy check (CRC) value computed from all the other fields except the frame check sequence itself. It is used to detect errors, other than collision, during transmission.

The technology for the cables and connectors is stan-

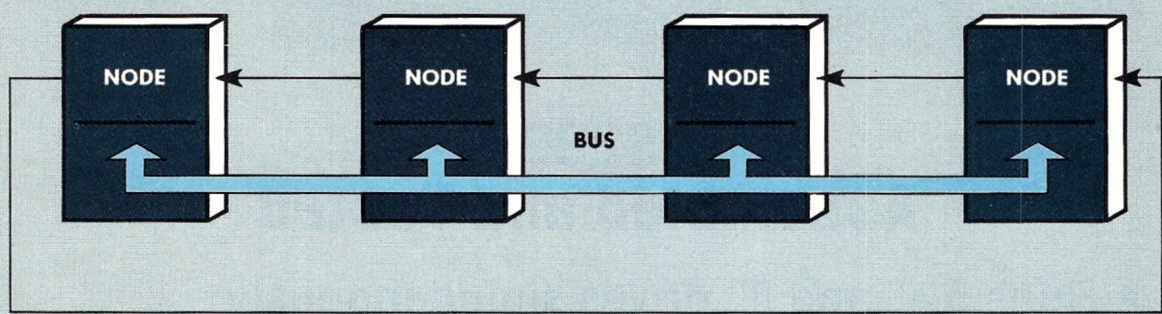

Figure 10. Logical token path (ring).

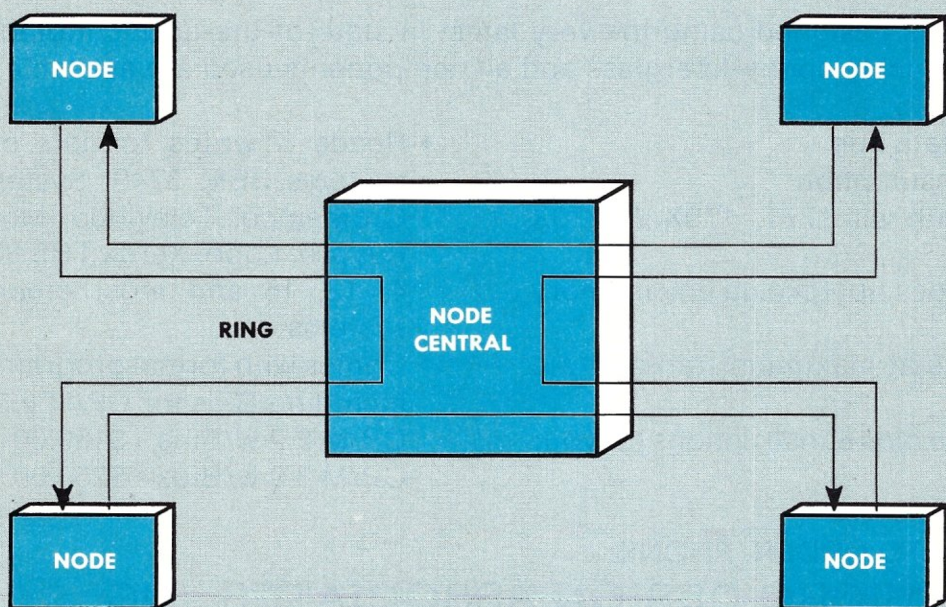

Figure 11. Proposed IBM LAN.

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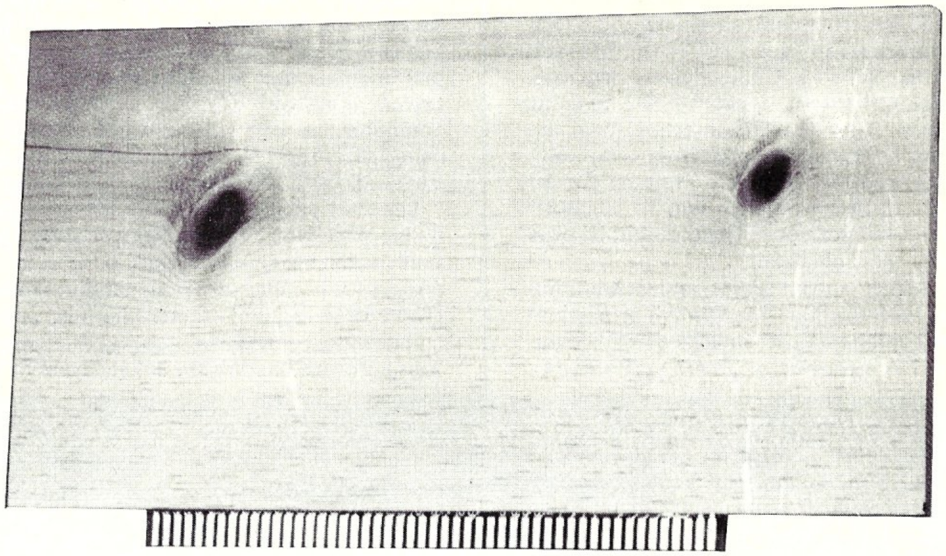

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This S-100 four-serial, two-parallel I/O board provides 4 RS-232 I/O ports, full handshaking, four 8251's and eight consecutive 8080 ports. Another feature: four separate dip-switch controlled baud-rate generators. The 2 parallel 8-bit I/O ports feature separate handshaking, use of four consecutive 8080 ports, and four 8-bit latches. The board was designed to provide maximum I/O expansion for multi-user systems.

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CIRCLE 223 ON READER SERVICE CARD

dard off-the-shelf parts, and the electrical interface is compatible with standard 10,000 series ECL logic. In fact, this was used for initial implementations; current system implementations, however, are being designed around VLSI chips for the Data Link controllers and the physical drivers and receivers. Xerox is working on a single-chip implementation, but it is not alone.

Intel has an 82586 Ethernet controller chip and 82501 interface chip combination. Seeq 8001, the Mostek MK7990 Local Area Network Controller for Ethernet (LANCE), the Rockwell International R68802, and the AMD AM87991 controller/AM7990 interface chips are just a few other implementations currently available. These chips should reduce the per-node cost for an Ethernet interface from over $1000 for non-VLSI implementations to under $400 per node. The cost will be even lower as the prices of these chips fall.

Xerox sells a file server, a print server, and a communications server along with the Star. The Star is a professional workstation that combines a user interface with a computational server. A number of firms sell similar equipment, including 3COM, which has an interface for the IBM PC along with software for such facilities as electronic mail.

The Omninet is a lower-cost, lower-speed LAN implementation from Corvus. It is also a bus-oriented implementation, though it uses the CSMA/CA access method instead of the Ethernet CSMA/CD access method. This is said to reduce the network interface complexity. The serial bus is implemented using a single twisted-pair wire. The bus interface uses standard EIA RS-422 drivers and receivers along with a Motorola M6801 single chip microcomputer and two custom VLSI chips. This interface is called a transporter. The combination is responsible for the Physical, Data Link, Network, and Transport Layers.

Omninet operates at a Mbps transfer rate with up to 64 nodes, which must be significantly closer than in the maximum Ethernet implementation. Corvus supplies transporters for popular personal computers such as the Apple II, the IBM PC, and others. They also sell a hard disk file and print server with the associated software for the nodes. This software handles the other layers of the ISO model.

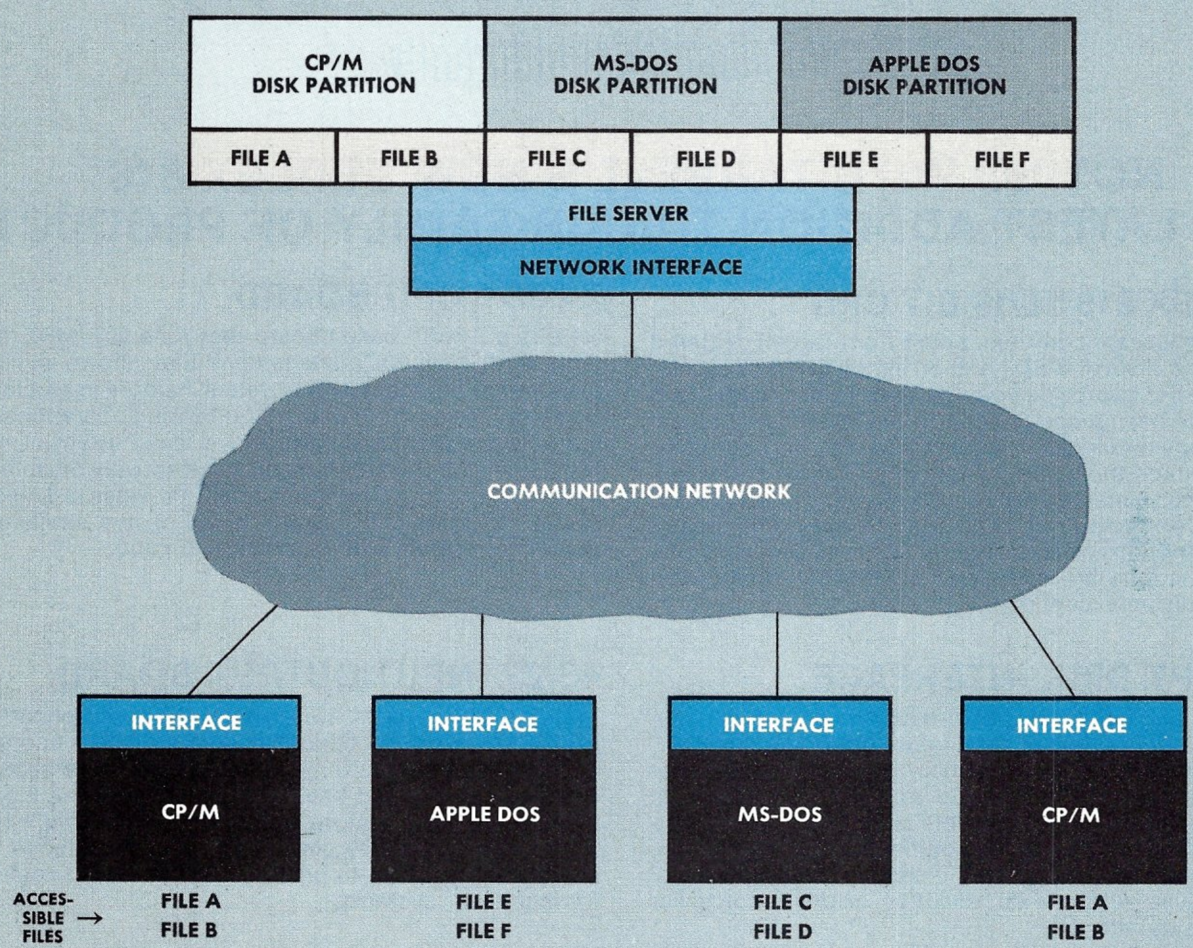
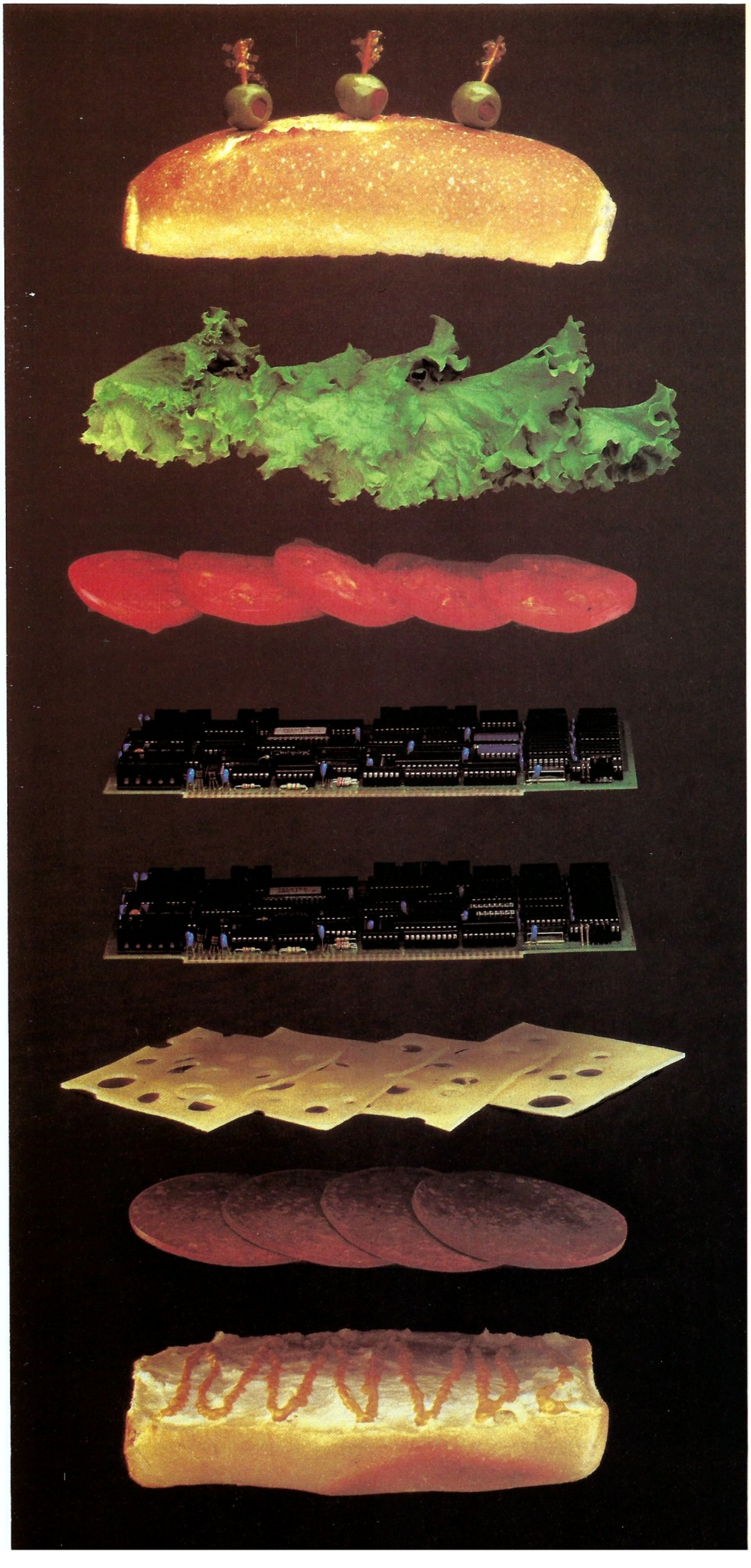


Figure 12. Partitioned file server.



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CIRCLE 174 ON READER SERVICE CARD

The file server is a partitioned system, where a partition can be allocated to a single operating system such as Apple DOS, MS-DOS, or CP/M. It essentially allows the hard disk to be shared by a number of users, but its shared data base facility is limited.

The ARCnet network was originated by Datapoint and is currently supported by Tandy/Radio Shack. It uses a modified token-passing access method with broadcast capability on a bus operating at 2.5 Mbps with a maximum of 255 nodes. The physical connection is typically a star or a tree. The modification to the token-passing access method is that token passes are acknowledged immediately.

The original implementation was done with coaxial cable and discrete logic. This has been expanded to allow for different connection media, including fiber optics and VLSI interface implementations. Standard MicroSystems Corporation currently supplies the COM 9026 Local Area Network Controller (LANC) and COM 9032 interface chips for the ARCnet. It interfaces to the host processor through an external 1K or 2K dual-ported RAM. The system supports a short packet up to 256 bytes and a long packet up to 512 bytes. The first 2 bytes are the source and destination addresses, followed by the size of the packet and the data. A 2-byte CRC is used for error detection.

CP/NET is a software product from Digital Research Incorporated (DRI), which is adaptable to many LAN implementations. CP/NET (Figure 15) consists of two parts: a Network Disk Operating System (NDOS) and a Network Input/Output System (NIOS). The first is supplied by DRI and the second is supplied by the LAN implementor, although DRI does supply numerous examples. The NDOS corresponds to the Transport, Session, and Presentation layers of the ISO model, while the NIOS encompasses the Physical, Data Link, and Network layers. The current implementation also includes some Application Layer software, including a rudimentary electronic mail facility.

The CP/NET system is configured with a host that usually runs MP/M, a multitasking version of CP/M also from DRI. The host has a special set of programs that are logically connected in a star configuration with one to 16 nodes running CP/M. These nodes run standard CP/M

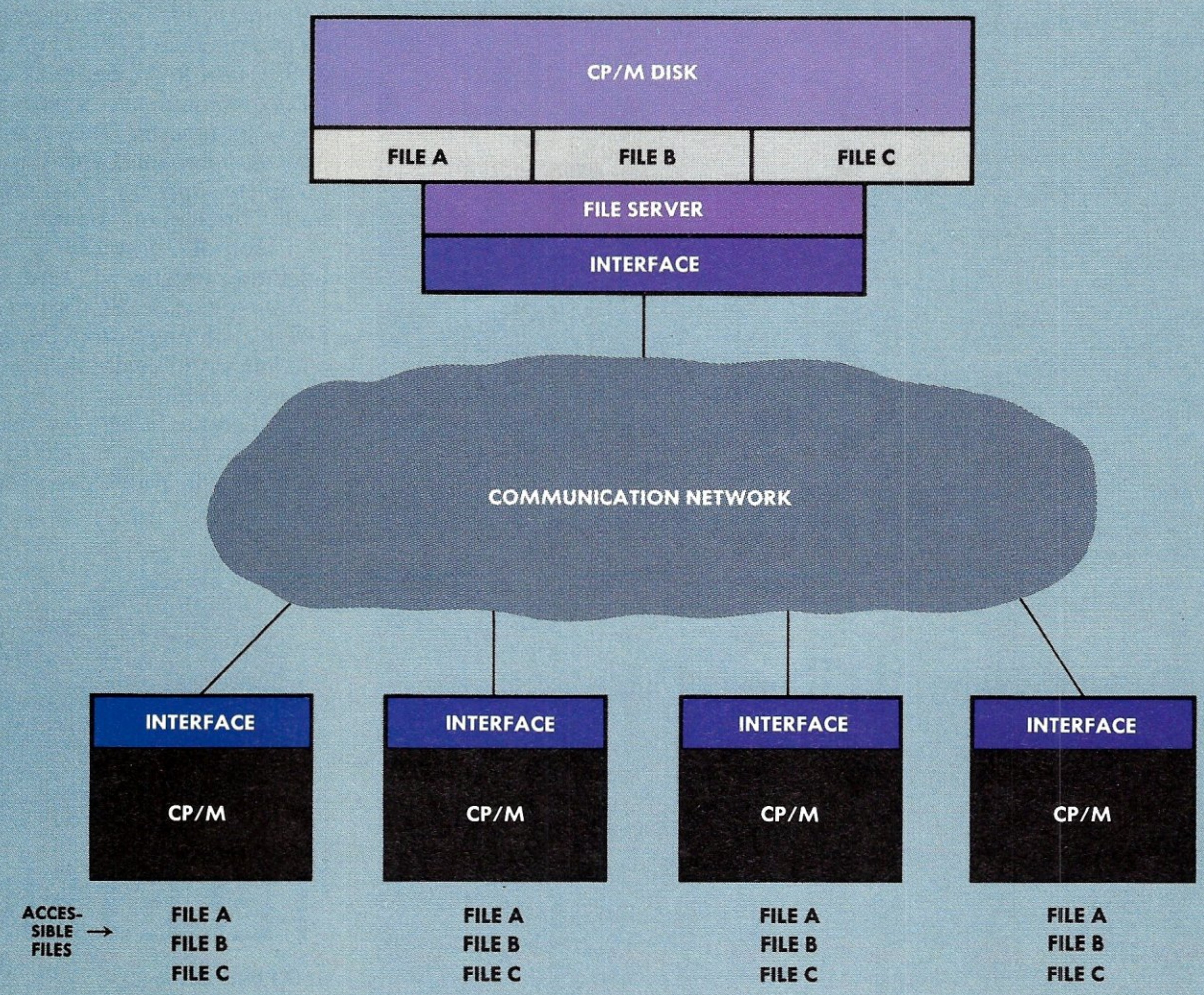


Figure 13. Shared file server.

with additional CP/NET software. Each node has 16 logical disk drives and one logical printer. Operating system commands allow a node to assign these logical devices to local physical devices or physical devices at the host.

Application programs operate by accessing the logical devices and are unaware that a device may not be resident. This means that the typical CP/M copy program, PIP, can be used to move a file from a disk drive located at the host to a local disk drive by simply assigning the appropriate physical devices to the associated logical devices. The CP/NET system implements a shared file server, so more than one node can be linked simultaneously to the same physical host disk.

The CP/NET system is more sophisticated in that it supports the password protection, and record and file locking functions of MP/M. These functions are very important when using a shared data base at the host. This is something which is not usually possible with a partitioned file server. CP/NET has many other features too numerous to mention here; however, one option which may be of particular interest is a version of CP/NET called CP/NOS. This version has no local disk drives, but instead uses only those at the host.

CP/NET is of particular interest because the NIOS can be customized to support just about any Physical and Data Link implementation including Ethernet, Omninet, and ARCnet. In fact, many implementations already exist. CP/NET is just one example of how the various layers in the ISO model can be partitioned in an implementation.

Summary

Local area networks are becoming more prevalent in today's computer industry. The array of existing and future products in this area continues to grow. Hopefully this article has been able to shed some light on the subject.

Bill Wong is currently doing program development for Rising Star. He received his M.S. in Computer Sciences from Rutgers and his B.E.E. from Georgia Tech. Bill is interested in microcomputer systems, parallel processing and artificial intelligence.

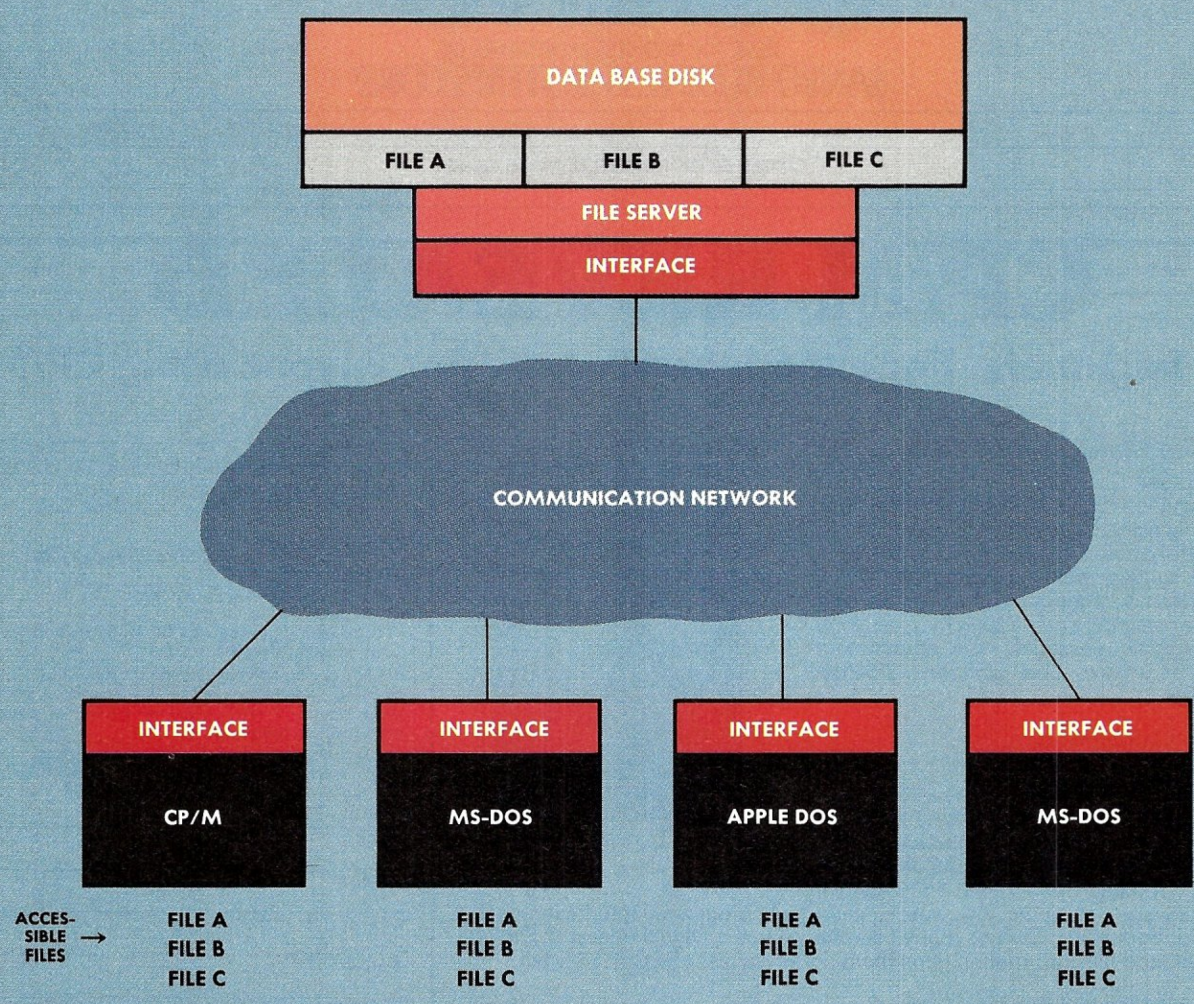
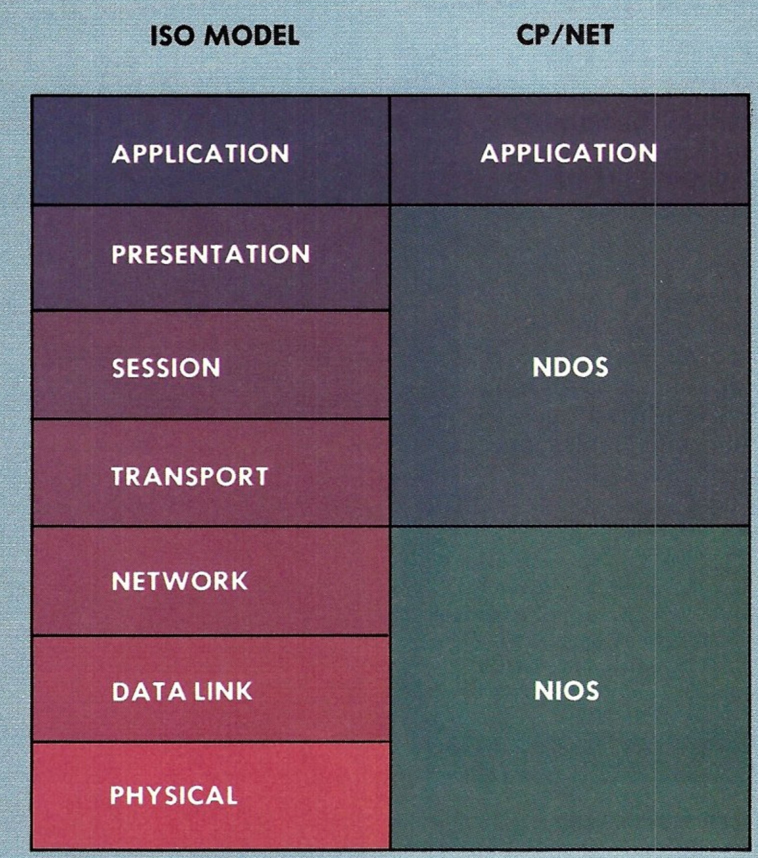


Figure 14. Data base file server.



RELATIONSHIP BETWEEN ISO NETWORK MODEL AND CP/NET

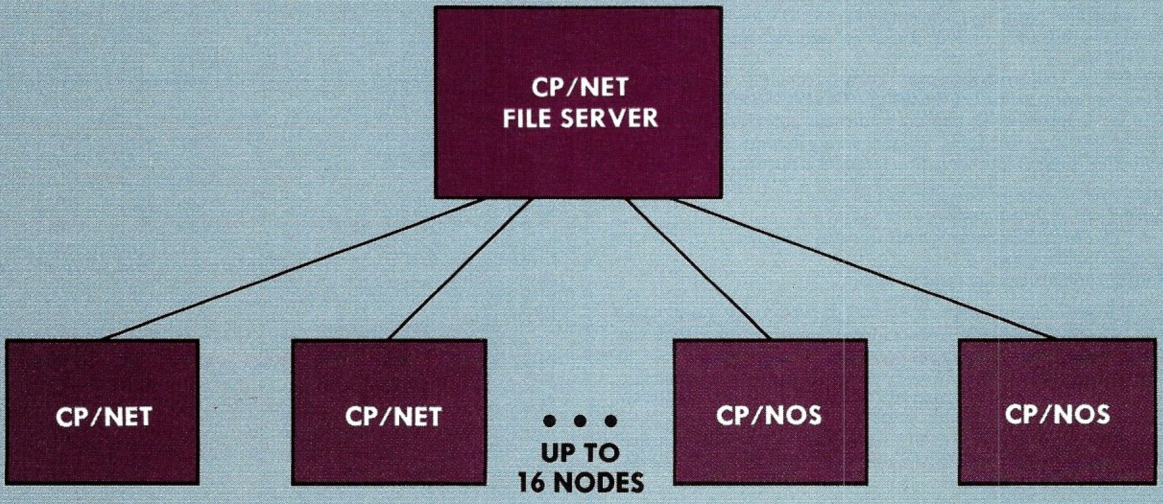


Figure 15. Logical CP/NET configuration.

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Table 2. A Few Existing LAN Implementations

Network	Company	Connection Topology	Access Method	Data Rate (bps)	Maximum Nodes	Distance (meters)	Reader Service #
ARC	Datapoint	Coax Bus Fiber Bus	Token Token	2.5 M 2.5 M	255 255	610 1600	300
Cluster/1	Nestar Systems	Wire Bus	CSMA/CD	250 K	65	300	301
Domain	Apollo Computer	Coax Ring	Token	12 M	–	900	302
Ethernet	Xerox 3COM DEC Intel Ungerman/Bass	Coax Bus	CSMA/CD	10 M	1024	2500	303 304 305 306 307
HYPERbus	Network Systems	Coax Bus	CSMA/CD	10 M	128	730	308
HYPERchannel		Coax Bus	CSMA/CD	50 M	16	1500	309
LINC	Vector Graphics	Wire Ring	Token	750 K	16	3200	310
Modway	Gould	Coax Bus	Token	1.544 M	250	4500	311
Omnilink	Northern Telecom	Coax Ring	Token	40 K	20	1500	312
OmniNet	Corvus	Wire Bus	CSMA/CA	1 M	64	1200	313
PLAN 4000	Nestar Systems	Coax Ring	Token	2.5 M	255	6400	314
Primenet	Prime Computers	Coax Ring	Token	10 M	247	3048	315
proNET	Proteon Assoc.	Coax Ring	Token	10 M	255	2400	316
NorthNet	North Star	Wire Bus	CSMA/CA	1 M	64	1200	317
Wangnet	Wang Labs	Coax Tree	Broadband	64 K	–	1000	318
Z-Net	Zilog	Coax Bus	CSMA/CD	800 K	255	2000	319

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  North Star
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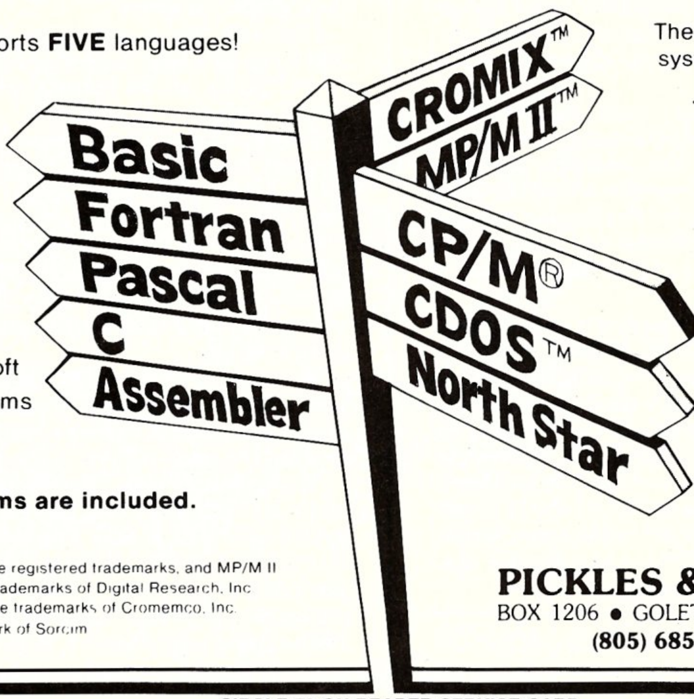
- Fortran: Microsoft
- C: Quality Systems
- Assembler

Sample Programs are included.



The P&T-488 supports **5** operating systems, **2** of which are multiuser!

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MICROSYSTEMS TESTS

The Zenith Low-Profile Z-100 Computer System

by Dave Hardy and Ken Jackson

The Z-100 low-profile desktop computer system from Zenith Data Systems (manufactured by Heath Co.) is another entry into the dual-processor 8085/8088 market. What distinguishes the Z-100 from its competitors is its high quality and its completeness as a whole computing system.

Features

The Z-100 is available in a conventional desktop cabinet with a built-in monochrome monitor and as a low-profile machine without a built-in monitor. Both of these models can also be purchased in kit form and assembled in the usual Heathkit fashion.

The Z-100 cabinet, which contains one or two double-sided 40-track 5¼″ floppy drives, a power supply, keyboard, plus a motherboard with two serial ports and a Centronics port, has something even more interesting than its 8085/8088 hardware: a five-slot S-100 (IEEE-696) bus.

Also built into the Z-100 is a video board that can display eight colors (or eight levels of gray if you don't have a color monitor) in a 640 by 225 pixel array. The dynamically redefinable character set provides an 80-character by 25-line display. Optionally, the board can also include a second page of video display and a light pen. The video board uses VT-52 control functions.

The basic Z-100 comes with 128K of user-addressable RAM, which can be expanded up to ¾ MB.

Hardware

Like all Heath products, the Z-100 is 100% high-quality hardware, well designed and dependable. The cabinet is heavy foam plastic, reinforced by an internal metal chassis. The low-profile unit is particularly rugged and compact.

Inside, all ICs are socketed, and the drives and power supply are fully shielded.

Keyboard. The 95-key keyboard, which includes a separate numeric keypad, has sculpted keycaps and a good "feel" for both touch-typists and hunt-and-peck computer hackers. It is well laid out, and resembles a standard IBM typewriter keyboard in appearance. Besides the numeric keypad, the keyboard has an additional 12 function keys, which may be assigned by the user to do whatever task is desired.

Actually, the keyboard is itself a complete 8-bit computer, with an 8041A processor with 1K of ROM and 8K of RAM, a clock, a counter/timer, and two parallel I/O ports on-board. Whenever a key is pressed, the keyboard generates an interrupt to the motherboard's 8259 interrupt controller. Auto-repeat and audio keyclick can be software selected, and a built-in 17-character FIFO (type-ahead) buffer is also under software control. In all, the keyboard accepts 14 commands to do these things and more, including enabling interrupts to the 8259, changing the scan mode, and turning the keyboard on and off.

Dave Hardy, 736 Notre Dame, Grosse Pointe, MI 48230

Zenith low-profile Z-100, exterior view.

Video. The built-in video board (as mentioned above) can be used as a VT-52 cursor control compatible terminal, or as a high-resolution graphics display of 640 by 225 pixels. Composite monochrome video, composite sync, horizontal sync, vertical sync, and RGB video signals are generated for use with different monitors. We were provided with a Zenith 15″ RGB monitor for our tests, and the display was quite good, with excellent linearity and color.

Characters are displayed in an 8 by 9 matrix, and are well defined. If you don't like the characters, you can make your own character set. Characters sets for several different languages are available, and can be easily loaded into the character generator.

The video board allows an alternate display format, which could be used to provide an interlaced display of 640 by 525 pixels, but no information is provided on specific programming for that purpose.

The color display is produced from three separate banks of video RAM, one for each main color (red, green and blue). Using this scheme, eight colors are available in much the same way that a color television makes different colors. By turning on combinations of the three main colors, eight colors are produced: black, blue, red, magenta, green, cyan, yellow, and white. The monochrome display can use the color selections to produce eight different levels of intensity.

The optional light pen detects the pulse made by the first pixel it "sees" when pressed against the video screen and generates a pulse of its own to cause the video board to remember the exact address of the pixel detected.

Motherboard; I/O. The 8085 and 8088 processors run at 5MHz. The 8085 uses standard 16-bit addressing, extended to 24 (IEEE-696). The 8088 uses 20-bit addressing, extended to 24 bits. Both processors can use interrupts generated by the 8259. In addition, each processor is also interrupted by NMI* (nonmaskable interrupt from the S-100 bus) and power failure. Both processors can also perform DMA to external (S-100 plug-in) devices.

Various configurations of RAM and ROM are available, but the Z-100 can hold up to 196K of RAM, and up to 32K of ROM.

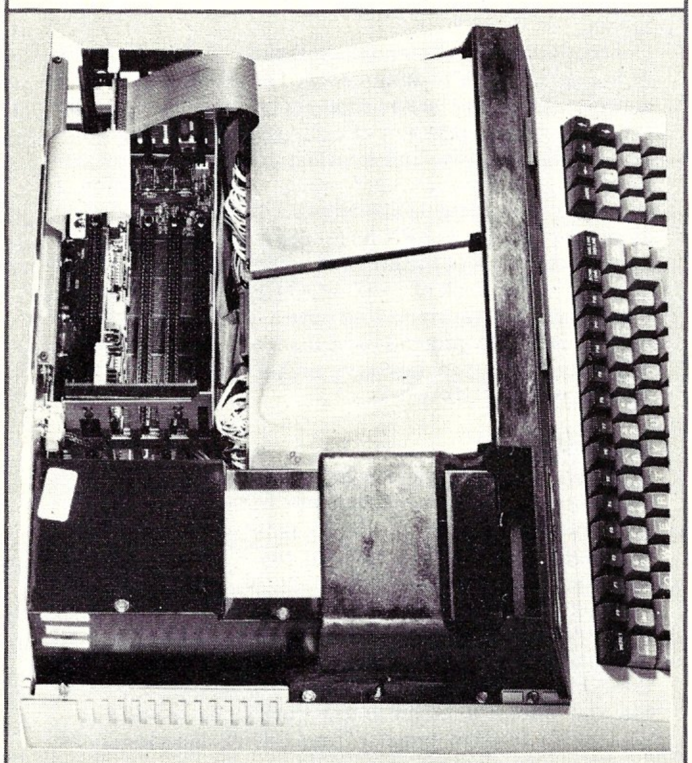
The master 8259 interrupt controller generates eight different interrupts:

Level 0 — Error (Monitors S-100 bus pin 98)
1 — Processor swap
2 — 8253 timer output #0 or #2
3 — Slave 8259
4 — Serial port A
5 — Serial port B
6 — Keyboard/Display
7 — Printer

The most interesting of these interrupts is the Processor Swap interrupt (Level 1), which allows the currently selected processor to be interrupted for a processor "swap," to switch in the *other* processor (8085 or 8088). The Z-100 has a processor "swap" port that allows a program to switch from one processor to another, and cause the newly selected processor to pick up where it left off, or force a restart to occur as the newly selected processor becomes active.

The Z-100 is one of the few machines we've seen that makes use of the ERROR* line of the S-100 bus to monitor external (S-100) boards for an error condition.

The optional slave 8259 interrupt (Level 3) allows access to the eight IEEE-696 interrupts generated on the S-100 bus, VIO*-V17*.



Internal view of Z-100, showing S-100 slots.

The Z-100 contains two integral serial ports (2661s), an 8253 counter/timer, and a 68A21 parallel port mapped at port addresses from 0E0H to 0FFH. Port addresses 0B0H to 0BFH are reserved for floppy disk operations, and ports addresses 0D8H to 0DFH are used for the video, light pen, and CRT controllers. Since the technical manuals mention that ports 0C0H to 0D7H are also "reserved" (lost to the decoding circuits, at least), this leaves port addresses 0 to 0CFH available for use on the S-100 bus.

The two serial ports are brought outside of the machine as RS-232 ports with DB-25 connectors. The parallel port mentioned above is used as a Centronics-type parallel printer port.

Floppy disk controller. The floppy disk controller is a card that plugs into the Z-100's S-100 bus. Why Heath chose to put the disk controller on an S-100 card is a mystery to us. Maybe they didn't have enough room on the motherboard. Whatever the reason, the board is fully IEEE-696 compatible and has several other nice features, too, including: user-selectable port address, programmable step rates, and independent 5¼" and 8" write precompensation adjustments. The board also allows up to four 5¼" drives *and* four 8" drives at the same time, although current software only supports two 5¼" and two 8" maximum. Single- or double-sided drives are allowed, and the 5¼" drives can be either 48 or 96 tpi. The 1797 floppy controller IC's data and interrupt request lines can be connected to S-100 vectored interrupt lines, if desired. (The board comes set up to work in a Z-100, so naturally, the interrupt lines are already hooked up.) The floppy controller board can also be bought separately, and used in any other S-100 system.

As it comes from the factory, the Z-100 is set up to handle two built-in 5¼" floppies, and one or two 8" floppies that plug into a standard 8" drive expansion connector on the back of the machine.

S-100 expansion bus. A complete five-slot fully IEEE-696 compatible S-100 bus is built into the back of each Z-100. Because the floppy disk controller takes up one of the five slots, only four are available for external use. If it is desired to add additional memory (beyond 196K) to the Z-100, S-100 memory boards can just be plugged in. In fact, most any S-100 board can just be plugged in, with minimal hassle. We were able to use several boards, including a PMMI modem, and various IEEE-696 memory boards with no problems. Eleven connector cutouts, in various sizes, are provided in the back panel of the Z-100 for additional I/O connectors from added S-100 bus boards.

Software

Two operating systems are available from Zenith for the Z-100; Z-DOS (which is actually MS-DOS) for the 8088 processor, and CP/M-85 (which is plain vanilla CP/M 2.2) for the 8085 processor.

Z-DOS performed perfectly with all of our generic MS-DOS programs, including several compilers, utilities, and test programs. Z-DOS did not perform well with many IBM-PC programs, particularly those which made calls to specific IBM devices, like the IBM PC version of dBASE II. If you choose software that operates under MS-DOS only, you should have no problems. If you see the error message "Wild interrupt," then you are probably running

The Z-100 has something even more interesting than its 8085/8088 hardware: a five-slot S-100 bus.

a piece of software that does not use generic MS-DOS calls. More than 20 utility programs are provided with Z-DOS, including the standard MS-DOS utilities, and much more. The I/O configuration program is particularly nice, since it allows the user to set up all I/O baud rates and handshaking simply and quickly. It is so complete that it even draws a picture of the back panel of the Z-100 on the screen and *points* to the proper plug for whatever I/O you are using! A utility called RDCPM is provided to copy CP/M files to Z-DOS, but no similar utility is provided to go from Z-DOS to CP/M.

CP/M-85 also worked well in all of our tests. Disk I/O was faster than we expected, possibly because most of the BIOS functions are handled by the 8088, which uses full-track buffering. Because of the 8088's involvement, the BIOS is extraordinarily complicated, but, fortunately, there is very little reason to want to modify it, because of the very versatile configuration programs provided with CP/M-85. The set-up programs are similar to those provided with the Z-DOS O/S, with various differences, including configurable autoload features, I/OBYTE assignment, and default mapping. Interestingly, the CP/M-85 I/O configuration includes an option for a Votrax board. The TPA available is 61K, which should be more than adequate for most CP/M applications. Complete source for the CP/M-85 BIOS is included.

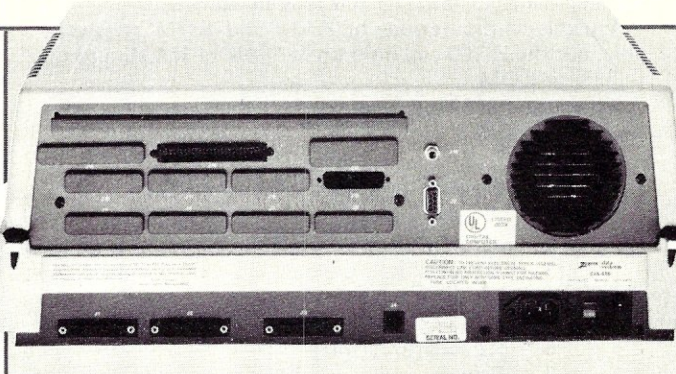
Several exceptionally good utilities are provided with both operating systems, including the various configuration programs mentioned for setting up printer and serial device protocols, selecting physical devices, etc. Quite a few printers are supported in the printer set-up programs, including the Diablo, MX-80 parallel or serial, HZ25 (of course), H14, T1810, DecWriters, and various others.

A "starter" package is available from Heath/Zenith that includes Z-DOS, CP/M-85, MultiPlan, and ZBasic. MultiPlan and ZBasic are both for use under Z-DOS. ZBasic, incidentally, appears to be very similar to IBM PC Basic. One of the local PC gurus tells us that it is IBM PC Advanced Basic, but we can't be sure.

The most frequent question asked about the Z-100 is "Is it IBM PC compatible?" As mentioned previously, as long as only generic MS-DOS programs are used, there should be no problem. Many software manufacturers already mark their products as Z-100 compatible. When in doubt, it is sometimes best to ask the manufacturer, and it is usually best to see the software work before you buy it. With the Z-100, software selection is helped by the fact that there are HeathKit stores all over the place, and they all carry Z-100 software. Zenith also publishes a list of third-party software vendors who support the Z-100.

Documentation

Heath documentation has long been considered a de facto standard in quality comparisons of documentation. The Z-100's documentation is no different. The manuals are clear, concise, well illustrated and voluminous. The Z-DOS documentation is contained in two entire manual sets, and includes a general introduction, a Z-DOS reference manual, a utilities manual, appendices, a glossary, and an index. The CP/M-85 documentation is also a two-manual set, that includes a complete set of the Digital Research manuals, a general introduction to CP/M, and a CP/M Reference Guide. In all, about 500 pages or so.



Rear view of Z-100, showing I/O connectors.

All manuals are high quality, typeset, multicolor, and contained in custom ring-binders. Sections are clearly marked, and important points and facts are boldfaced or printed in different colors and sizes for clarity and easy reference.

A demo disk is included that demonstrates some business graphics and some general graphics techniques, including line and circle drawing, charts, bar graphs, and multicolor pie charts. The graphics programs are written in ZBasic, so you can list them out to figure out what's going on.

An optional set of manuals, called the *Z-100 Technical Manuals,* is highly recommended. These manuals contain complete hardware information, including schematics, detailed theory of operation of each assembly, set-up information, floppy drive information, troubleshooting, programming information, and much more. In addition, a complete copy of the IEEE-696 specifications is included, along with the Intel iAPX 88 (8088) manual and complete data sheets for all of the major ICs inside the Z-100. Finally, a 1½″ thick book of Z-100 BOOT ROM SOURCE listings is included, for those who have a lot of spare time. We would highly recommend these manuals if you are considering doing any programming on the Z-100, or want to know how the Z-100 works.

Complaints

Although we were generally impressed with what we saw, we did have a few small complaints. First, in the early version we received, the 8″ floppy drive capability wasn't working, so we couldn't perform any 8″ drive tests. Second, the Centronics parallel port on the back of the Z-100 is brought out to a DB-25 type of connector, which means that you'll need a special cable to connect a printer to your machine. We think it would have been just as easy to bring the Centronics signals out on a Centronics-style connector, and quite a bit easier to use. Finally, we would like to see a utility to allow transfer from Z-DOS disks to CP/M-

The Z-100 offers the advantages of both the popular 8-bit CP/M (with its incredibly large software base), and those of the new, more powerful, 16-bit world.

Zenith Z-100 continued . . .

85 disks. It seems reasonable, since a utility is provided to transfer from CP/M-85 to ZDOS.

Conclusions

The biggest advantage of the Z-100 is that it is a complete system that is still expandable for a user's needs. It offers the advantages of both the popular 8-bit CP/M operating system with its incredibly large software base, and the new, more powerful, 16-bit world. In addition, it offers the advantage of the expandable S-100 bus system for those who need it, and a complete stand-alone machine for those who don't. Moreover, it is well built, well documented, and dependable.

Z-100 desktop model (13½"h x 19½"w x 19½"d) with built-in monochrome monitor (screen available in amber, green or white): Kit, $2,349; A&T, $3,599. Z-100 low-profile model (7⅛"h x 19½"w x 19½"d) with monochrome graphics: Kit, $2,199; A&T, $2,899. Monochrome monitor recommended: High-resolution ZVM-122, $169.95 (12" display). To upgrade the Z-100 to color capability, two color video RAM chip sets are needed at $145 per set. Configured for high-resolution color graphics, the Z-100 is: Kit, $2,199, A&T, $3,499. Color monitor recommended: High-resolution ZVM-135, $649 (13" display).

For more information, contact:

Heath Co.
Benton Harbor, MI 49022
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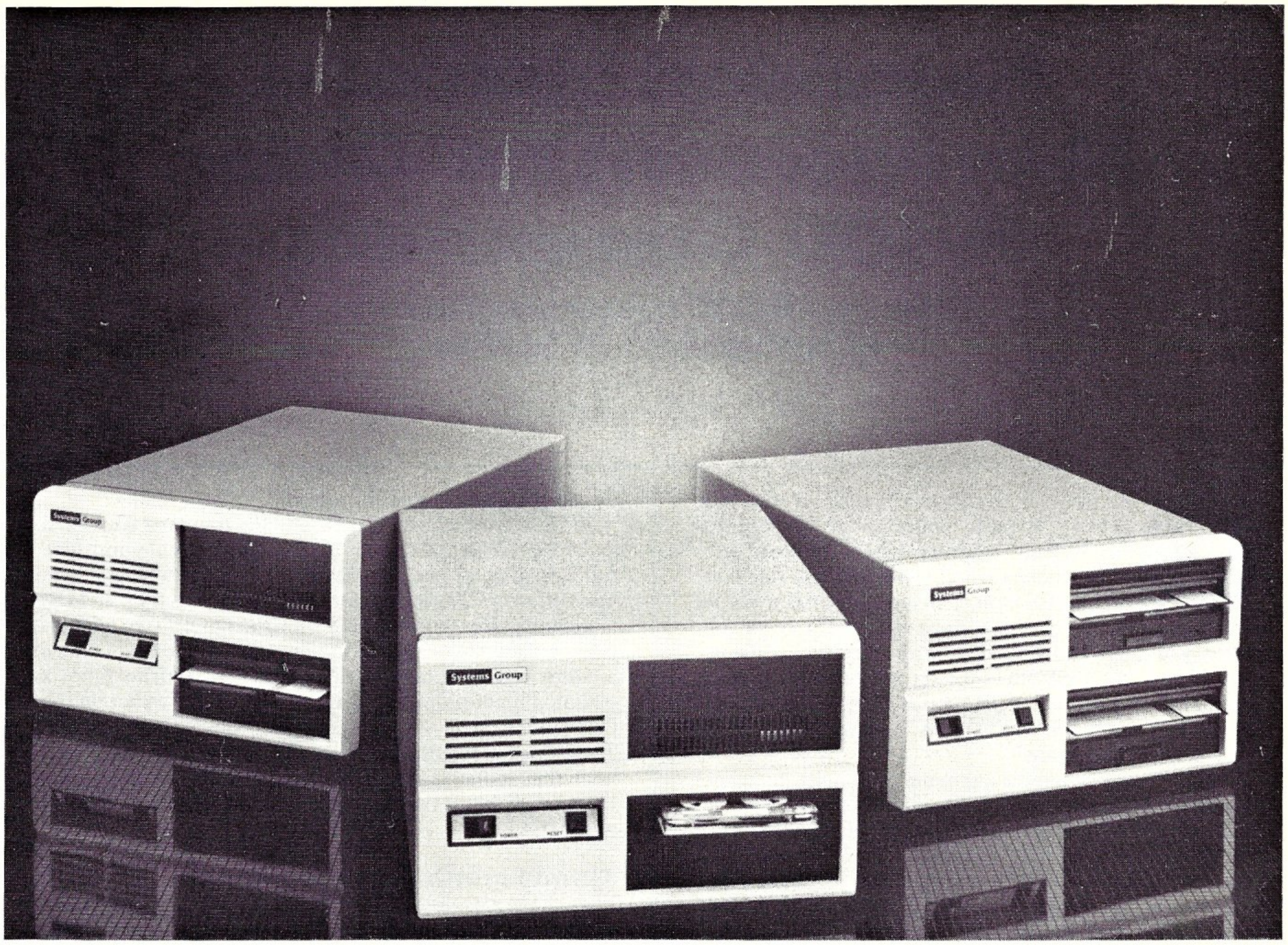
CIRCLE 324 ON READER SERVICE CARD



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Extended Memory Management for Older S-100 Computers

How one S-100 owner went about breaking the 64K barrier

by Andrew L. Bender

Got an older computer? Maybe an Altair or IMSAI? Want to modernize it? Interested in CP/M Plus? Multibanking? Then read on. I have an old IMSAI to which I am much attached (though I haven't given it a name) and which works fairly well as measured by the cover test. In case you don't know what a "cover test" is, let me explain: if you can keep the cover on your computer for a whole week at a time, its operation is "fair"; two weeks is "good"; three weeks is "fairly good"; and more than three weeks is "probably lying!"

I recently went to a local computer club meeting, where I heard all about CP/M Plus. Delighted by the introduction, I wanted to run CP/M Plus on my own machine, but at that time I owned only one bank of memory. While a single-bank CP/M Plus configuraton does give some speed increase over 2.2, it occupies more memory space, and the reduced TPA may not be tolerable in some applications. Deciding to build a 3-bank system was not easy—it would be expensive, even if I used my existing memory boards, which were old and had no provision for extended addressing. However, it turned out that you can use older boards in such a system, provided that they have some means (such as the PHANTOM* line) for disabling the board under program control. I shall first discuss the basic requirements for extended memory management in an 8-bit system and a simple circuit to perform this function. Then I shall describe some additional circuitry needed for the control of older memory boards.

Extended addressing or bank switching?

Until the preliminary IEEE-696/S-100 standard appeared, memory was so expensive that few people even contemplated using more than 64K of memory in an 8-bit system. Thus, the early memory boards sometimes had a phantom circuit to disable them while the CPU was reading PROM bootstrap routines on a disk controller. As memory prices started dropping, some manufacturers began to incorporate provisions for bank switching. Each board contained an output port with a data latch, in which each bank number corresponded to one data bit; eight switches connected the enable line to one or more bits of the data latch. Thus, outputting a data word with, say, bit 2 set would cause a memory bank with switch 2 on to respond to memory read/write instructions. Any other memory bank would be deselected. This scheme allowed up to eight banks to be addressed.

Andrew L. Bender, M.D., Neurological Services, Inc., 336 Center Ave., Westwood, NJ 07675.

With the advent of the IEEE-696 standard (finalized and adopted last December by the Standards Committee), full decoding of the additional 8 extended address lines now allows a CPU to address up to 256 banks (i.e., 16 MB) of memory. But, because an 8-bit CPU has only 16 address lines, a memory manager is still required. However, since modern boards can decode the extended address lines, a common memory manager is usually located either on the CPU board or on a separate memory management board. The manager consists of a port address decoder and a data latch that activates the eight extended address lines. This is the type of circuit that I built for my CP/M Plus system on the IMSAI.

Simple memory management

If you have a prototype card which already has address decoding on it, such as the clock/calendar circuit described by Chris Terry in *Microsystems* Vol. 3, No. 2 (Mar/Apr 1982), the circuit in Figure 1 will provide extended addressing by adding just a few chips. The 8212 latch accepts data from an OUT instruction and transfers it to the extended address lines, where it remains until another OUT instruction is executed to the memory management port. The OS6* signal is an output strobe generated by the circuitry in Figure 4 of Chris Terry's article. This select line goes low whenever sOUT and pWR* are active, the proper 5-bit address is on lines A7 through A3, and the bit pattern "110" is on lines A2 through A0. The DS2 line on the 8212 is tied high so that the chip is always enabled when the DS1* line (driven by OS6*) goes low. The CLR* input is activated whenever pRESET* or POC* goes low, so that bank 0 is always enabled by turn-on or by hitting the RESET button.

There were some errors and omissions in the figures accompanying Chris Terry's article. In Figure 3 (page 62), the bus address line pins are reversed: the correct numbers are A3, pin 31, A4, pin 30; A6, pin 82; A7, pin 83. In Figure 4 (page 64), the connections of two address lines to U2 and U3 (74LS138s) are backwards: A2 should go to pin 3 of both ICs, and A0 should go to pin 1 of both ICs.

A complete memory manager circuit

If you do not already have address decoding and I/O strobe circuitry available, Figure 2 shows how to set up a complete memory manager. Address lines A7 through A2 are compared (in the 8131 6-bit magnitude comparator) to the outputs from a 6-position DIPswitch that sets the high-order bits to the desired base port address. The 8131 strobe input is grounded so that the chip examines all addresses. When the upper 6 address bits match the switch settings,

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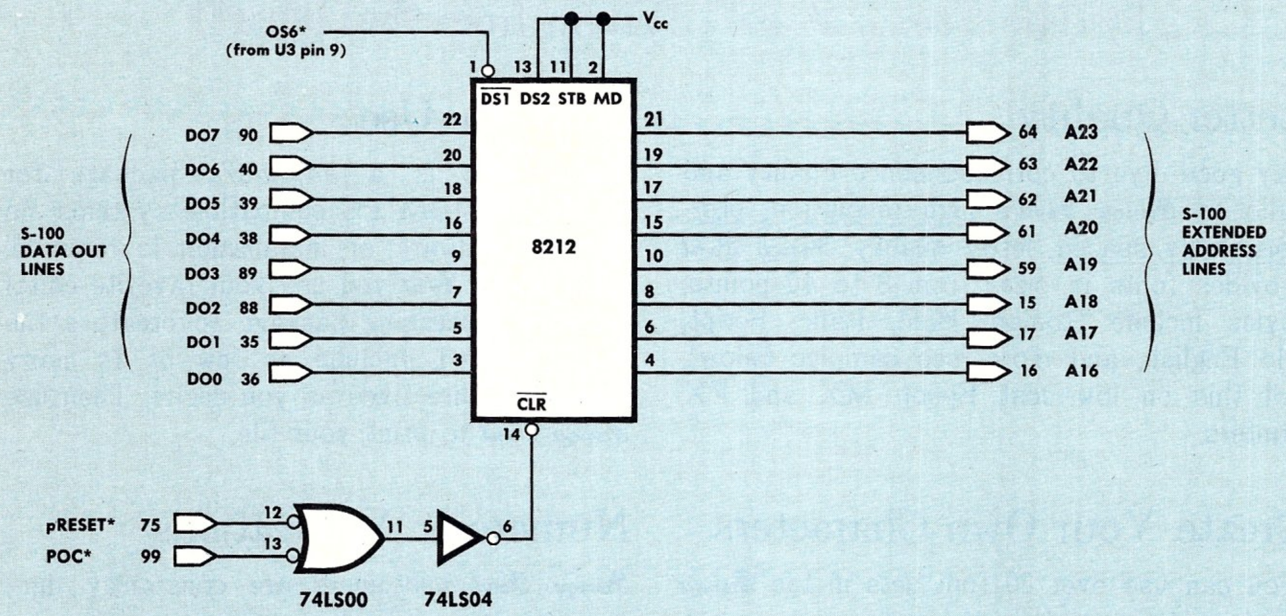

Figure 1. Simple memory manager (for Chris Terry's clock circuit).

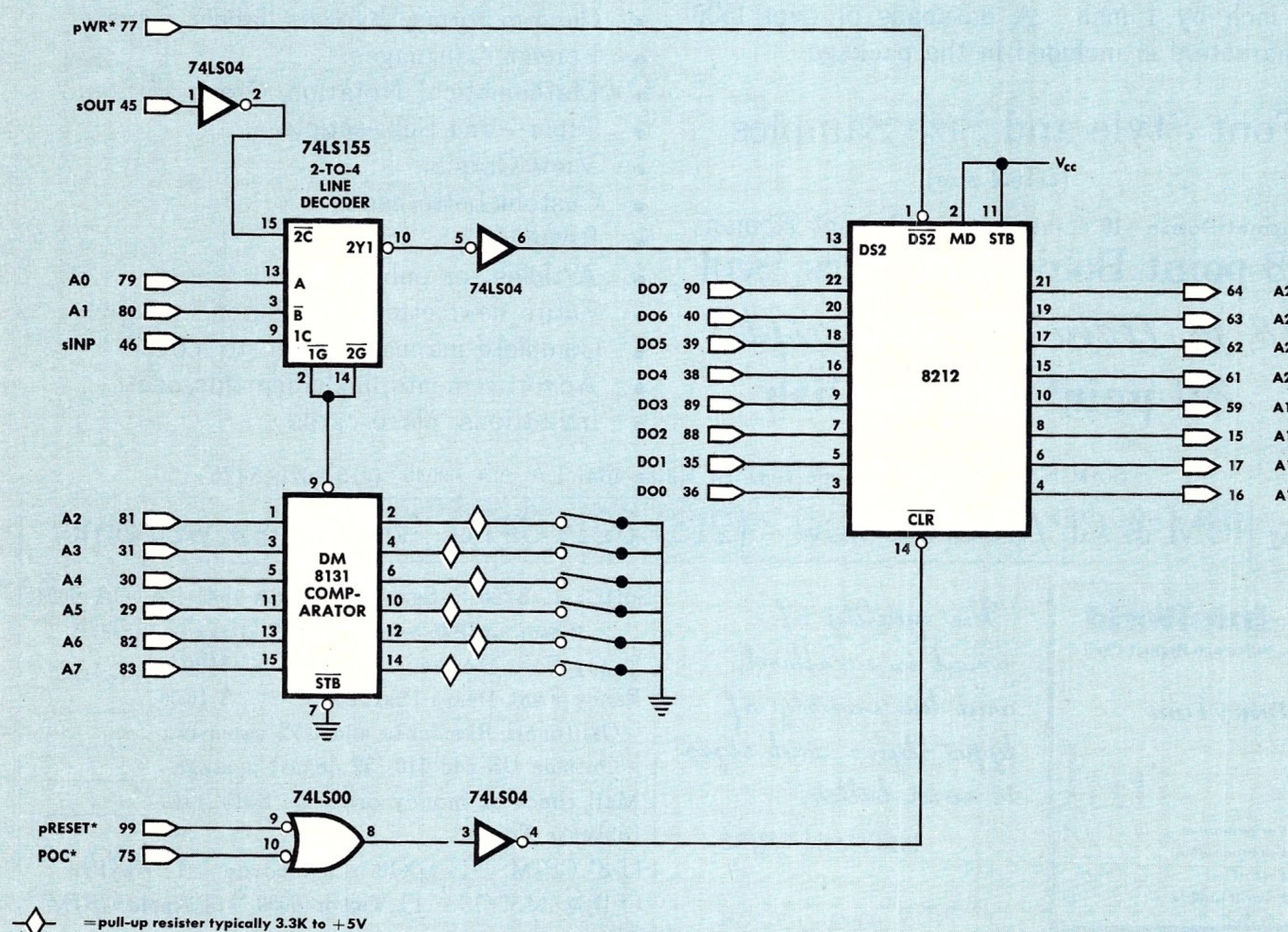

Figure 2. Complete memory manager.

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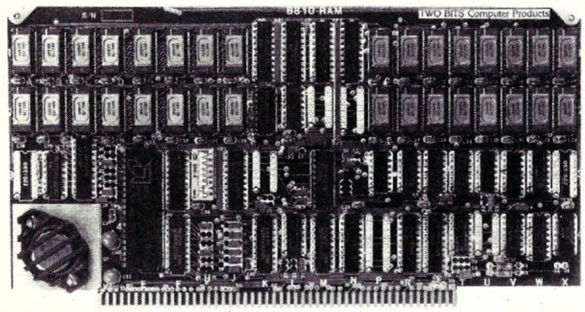

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the MATCH* output goes low and enables the 74LS155 2-to-4-line decoder. This chip decodes the two low-order address lines (A1 and A0). The 74LS155 decoder has two halves, which I used to provide both input and output strobes. Note that the two halves are *not* symmetrical; one half requires an active-high signal, the other an active-low signal. The half that provides input strobes is directly enabled by sINP; the other half, that provides output strobes, is enabled by inverted sOUT. This allows the port address for the memory manager to be OFDH, which is a current de facto standard address for memory manager devices.

Modification for alternate bank-select boards

Memory boards such as the TDL Z-16 do not have any provision for extended addressing; however, they may have an alternate bank select line (ABX*) which, when low, keeps the first bank selected, but deselects the bank when high. Bursky's book gives schematics for many of the older boards of this type, and they can be used in Bank 0 by adding the circuit shown in Figure 3. I used pin 60 in my system because TDL had assigned it to ABX*. Check to see that the pin you use in your system is not assigned to any function that might cause a conflict.

Program to move data between banks

A demonstration program to test the bank select circuit is given in Listing 1. This program moves data between banks and must always reside in the global portion of

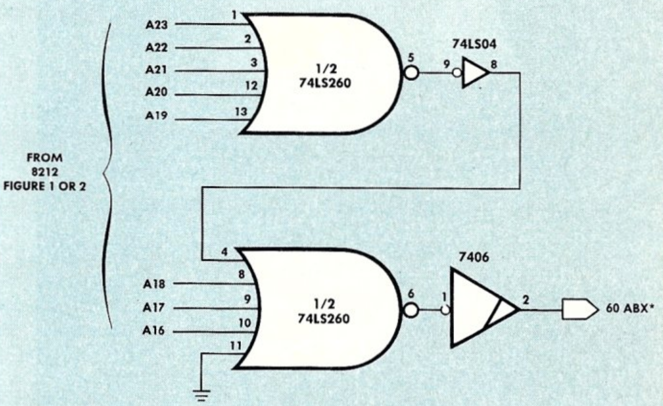

Figure 3. Modification for alternate bank select line.

Extended Memory Management
continued . . .

memory common to all banks. Note that a Z80 machine cannot use a block transfer instruction to move data between banks. I have made the assumption that this program is called from another routine in global memory, so there are no problems as to which bank the stack is in. The banks must be switched for each byte transferred. On entry, register pair HL points to the source address, register pair DE points to the destination address, B contains the number of the source bank, and C contains the number of the destination bank.

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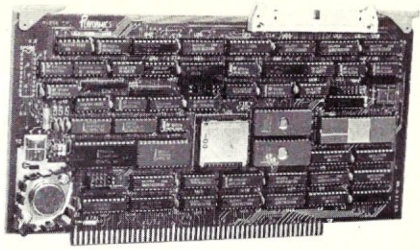

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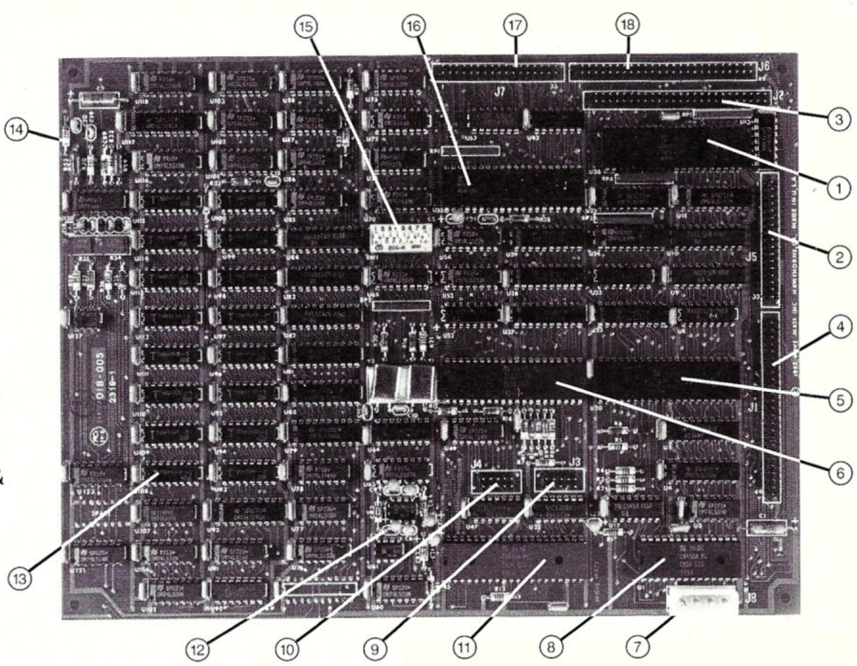

1. Printer/Winch Port
2. Printer Conn.
3. Winch. Conn.
4. Exp. Data Bus
5. CPU Chip
6. DMA Chip
7. Power
8. Clock Timer Cont.
9. First Serial Port
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MICROSYSTEMS REVIEWS

Nevada Fortran from Ellis Computing

For $29, how good is it?

by David L. Dupuy

Some of us grew up with Fortran and still find it very useful, mainly because of its speed, familiarity, and general availability on mainframe computers. All this, despite the purists who look down on Fortran these days! Among CP/M users, Microsoft F80 Fortran is pretty well the standard, but at $350, one is likely to pause carefully before ordering. Hence when I saw Nevada Fortran from Ellis Computing advertised for $29.95, I was intrigued. But at $29, how good is it?

The $29 price tag reminds us of the recent discussions concerning $29 Pascal. Curiously, as someone has already said in these pages, the price of software these days often bears no relation to its quality. I recently purchased the $29 Fortran, and the purpose of this article is to convey my reactions after using it for a couple of months. This review should give you a feeling for the general capabilities of this Fortran—which you may not be able to glean from the ads—and help you decide if you want to purchase it or not.

To quickly summarize my reactions: for $29, this software is remarkably good! Although slower for computations than other Fortrans, overall it is very capable Fortran. I heartily recommend it, especially at 1/12 the Microsoft price. But consider its limitations, discussed below, before you buy.

Documentation

For $29, can the software *and* the documentation be acceptably good? In this case, yes! The manual is not intended as a Fortran primer (correctly so, in my opinion), but it does adequately document the features, structure, and use of Nevada Fortran. The manual has 137 pages, plus an additional 40 pages describing the Nevada Assembler, which is included in the $29 package. The manual was obviously put together with a good word processor, and the top header carries a revision date of January 1982. The printing quality is great, and the manual is punched for a three-ring binder, then *bound* with a soft cover. Nice! There is a detailed table of contents, and the chapters are divided into the usual (useful) categories, e.g., number systems, control statements, arrays, I/O, etc. There are 13 appendices, and most are very useful, such as statement summary, standard and nonstandard functions (e.g., SIN, ABS, AMOD, etc.), system subroutines (e.g., CALL OPEN), and errors.

A number of examples are included for most items, but I personally would have liked at least twice as many, since I find examples the quickest way to learn. However, if one remembers that the manual is not intended as a Fortran primer, then one must concede that the number of examples is adequate. At the end of the manual there are several sample programs, mostly to illustrate features not normally found in Fortran. For instance, there are sample programs for the TRACE ON and TRACE OFF statements, the CHAIN statement for chaining programs, the DUMP statement, the SEEK statement for random access disk I/O, and even sample programs for a simple graph routine and a Shell sort.

I have two negative comments about the manual: First, there is no index. I consider this an almost unforgivable omission, especially since a capable word processor appears to have been used. Surely it would have been only one day's effort to use the FIND command to root out all the references to, say, FORMAT or DIMENSION, etc. My other complaint has to do with the location of the installation procedure and other information for first-time users. All the details needed to configure the software for certain defaults and to compile a program are in Chapter 9 under the section "Getting Started," tucked away on page 84! It took me a while to find that the first night! Why not in the first chapter?

Aside from these two complaints, the manual is fairly complete and not hard to use. It's not organized as well as the DEC Fortran manual, but very few manuals are. There is a complete list of errors, good descriptions of system subroutines and functions, and most of the manual is logically arranged. I consider the manual a very positive factor

David L. Dupuy, Dept. of Physics, Virginia Military Institute, Lexington, VA 24450

Table 1. Comparisons of computation speeds (in seconds)

	Microsoft Fortran	Nevada Fortran	Microsoft Basic
Pournelle benchmark	14	67	108
Eratosthenes prime numbers*	5.8	284	607

*10 iterations, 4K array elements

Table 2. Disk I/O benchmark times (in seconds)

Statement	Nevada	Microsoft
WRITE (8,20) (x(k),k=1,4096)	23	182
WRITE (8) x	10	6

Table 3. Disk space for typical short program

Nevada		Microsoft	
JERRY.FOR	2K	JERRY.FOR	2K
JERRY.OBJ	2K	JERRY.COM	14K
(JERRY.REL	2K)	(JERRY.REL	2K)

in the decision to purchase this software.

Structure and convenience of use

As mentioned above, the procedure to get a Fortran program running is covered in Chapter 9 of the manual (page 84). If you are accustomed to Basic, you have probably heard that Fortran is very clumsy to use, since it must be compiled, linked, and so on. It's certainly true that debugging a Fortran program can take longer because of the extra time in compiling. But the payoff is in compatibility with mainframe programs, runtime and other areas. If you are familiar with a mainframe Fortran compiler and operating system (e.g., the DEC compiler and linker), you will find that the Nevada Fortran is compiled a little differently. Here is an example for compiling a simple Fortran program named PGM.FOR under Nevada Fortran:

```
FORT PGM    compiles source code, produces inter-
            mediate assembly file PGM.HEX
FRUN PGM    runtime package executes program
```

Now you see one of the main structural differences between this and other Fortrans: there's no linker! Even if you have never used a Fortran compiler, you will find the Nevada procedure simple, and it may be quicker than compiling and linking (e.g., Microsoft Fortran). For most situations, the absence of a relocating linker (sometimes called a linking loader) is no real disadvantage. (Read on—I have to justify that statement!)

An important use for linking a subroutine is to interface to an assembly language subroutine, e.g., for tasks that require speed or outputting to a port, or other tasks that are simpler to do in assembly language. That capability *is* available with Nevada Fortran, and in fact, by several different routes. First, assembly language statements can simply be included in your Fortran source program with the inclusion of an asterisk, which means that these statements are assembled directly and not taken to mean Fortran statements. That could sometimes be far simpler than linking to a subroutine. Second, there is a CALL routine (a function of the form **A = CALL (parameters)**) that allows assembly language programs to be CALLed and to be passed an argument. The starting address in memory is specified in this CALL function, and another Fortran statement is used to get your assembly language program into memory, the **CALL LOAD** system subroutine. Finally, FUNCTIONS and SUBROUTINES written in Fortran can be used as usual, but they must be included at the end of your program and compiled with the main program. The **COPY filename** statement is probably useful here: the file specified is inserted and you do not have to retype your favorite subroutine at the bottom of each new program.

There are all the usual compile options to make life easy for you. The general form of the compile command is

```
FORT U:PGM.LAO $OPTIONS
```

where FORT is the Fortran compiler, U: is the drive where the source code (PGM) is found (if not present, the default drive is assumed), L is the drive to receive the list file (PGM.LST), and A is the drive for the final object program. There are the usual useful options for LAO, such as "do not generate a PGM.LST file", etc., and there are useful defaults. For example, "FORT PGM" compiles and assumes the default drive for everything. For OPTIONS, one finds N (no assembly or object files), P (paginate the list file), blank pad the source statements to either 64 or 72 characters, and several others having to do with COMMON blocks.

Incidentally, I found the Nevada Fortran to be as accurate in trigonometric functions as other implementations. For example, the result of $\sin^2 x + \cos^2 x$ (which should equal 1) was 0.99999998 (an error of 2 parts in 100 million). No other checks were made on the number of digits of accuracy.

Computation and I/O speed

I fully realize that benchmarks are a sensitive subject, but I would like to give you an idea of the computing and I/O speeds. The tests with Nevada Fortran were performed on my CompuPro S-100 system, which has a Z80 CPU (CPU-Z) running at 6 MHz and a Shugart 801 8" disk drive with the CompuPro DISK1 controller. I am indebted to Dr. Arne Henden for running the Microsoft Fortran for these comparisons on his S-100 system.

A comparison of computational times first. I ran Jerry Pournelle's benchmark (*BYTE,* October 1982, page 254), which I translated from Basic into Fortran. I also ran the Eratosthenes Sieve prime number benchmark (Gilbreath and Gilbreath, *BYTE,* January 1983, page 286). The results of these tests are shown in Table 1, and execution times in Microsoft Basic are shown for comparison. For the prime number program, I could not use an array with 8K elements with the Nevada Fortran because of the way *all* Nevada Fortran numbers are stored (6 bytes per digit). Therefore all three prime number benchmarks were run with 4K elements, and that should be taken into account if these times are compared with the Gilbreath and Gilbreath results. It is clear that Nevada Fortran is significantly slower in these computations than the Microsoft Fortran, but still faster than interpreter Basic.

Since I write numerous data files to disk, I was very interested to see how quickly Nevada Fortran handled this chore. I wrote a simple I/O intensive program to test this, and this program is given in Listing 1. The line "WRITE STATEMENT GOES HERE" was first replaced with a formatted write statement: WRITE (8,20) (x(k), k=1, 4096) and then with a unformatted write statement: WRITE (8) x. The resulting times are shown in Table 2. Note the PAUSE statement; the timings did not include computation times. The Nevada Fortran is considerably faster than the Microsoft on formatted I/O, and virtually the same on unformatted I/O. (Remember that these timing comparisons were obtained on two different computers, and slightly different times would likely result if these comparisons were run on the same computer. Nonetheless, I feel this rough comparison is useful.)

Incidentally, if you are perpetually short of floppy disk space for user files, the Nevada Fortran will give you an advantage. The disk storage requirements for the Pournelle benchmark are shown in Table 3. The two files in parentheses can be removed after successful compilation, and then, for the same program, the Nevada system requires 4K of disk space, while the Microsoft version requires 16K. This is true because of the Nevada runtime package, which has been excluded in Table 3 (analogous to keeping the Microsoft compiler on your disk). This is also

Even if you have never used a Fortran compiler, you will find the Nevada procedure simple, and it may be quicker than compiling and linking.

the reason the runtimes are longer for the Nevada Fortran, because of the runtime interpretation.

Features and details

In this section I intend to list some of the enhancements, omissions, and details in this Fortran. First of all, at this price, something must have been left out. There was, of course, and on page 118 in the manual is found a clear list of enhancements and omissions with respect to the ANSI 66 standard. Perhaps the most serious omissions are (1) the lack of any double precision computations or functions (that could be important for some types of scientific computations), and (2) the lack of complex numbers, statements, and functions. The other ANSI 66 features not implemented seemed less important to me for most computing. For example, there is no EQUIVALENCE statement, no D or P format specifications, no extended DATA statement of the form DATA A,B,C/1,2/3/, and a couple of other minor items.

There are numerous useful enhancements, i.e., things you cannot do in ANSI 66 Fortran. Some of the enhancements were undoubtably required because no linking loader was available, as discussed above. For example, assembly language routines can be written in directly, with an asterisk to alert the assembler to assemble these statements directly. There is also a COPY statement to insert source files into a Fortran program. Those two features make the Fortran viable without a linking loader. In addition, a CHAIN subroutine is available to load and execute another program. Also, a CALL LOAD subroutine can be used to load a PGM.HEX or PGM.OBJ file into memory under program control, and a CALL function then causes execution of this code, passing an argument if desired.

In addition to the usual formatted and unformatted (binary) I/O, a free-form I/O is available. This is similar to the free-form I/O found in DEC Fortran and on other mainframes these days. For example, the TYPE and ACCEPT statements need no formatting, e.g., TYPE 'The answer is', ANS outputs the string and variable to the console, and ACCEPT 'Input value for XMAX:', XMAX prompts the user on the console and then reads in the value. A more flexible free-form I/O is available with the usual READ and WRITE statements: WRITE (1,*) x writes to logical unit 1 (the console) and needs no format statement. The free-form READ is similar: READ (6,*) (x(k), k=1, npts) would read from a disk file. With these you can avoid the FORMAT statements if you wish. The usual CALL OPEN and CALL CLOSE subroutines are available, with an optional error parameter that can even convey the reason for the I/O error, such as "disk is full" or "end of file encountered". A REWIND statement positions the pointer to the beginning of the file, and the BACKSPACE will backspace the logical unit specified by one record. The CALL OPEN (8,'LST:') sends output directly to the printer. You can even delete and rename disk files *under programs control* (CALL DELETE and CALL RENAME). Very useful and easy-to-use I/O statements!

Finally, there are several powerful features that should appeal greatly to those interested in using Fortran for instrument control and real-time experiments. Here's one you won't find in ordinary Fortran: the CALL DELAY (wait time) implements a delay up to 635 seconds, with a resolution of 0.01 seconds. That's much easier programming than most of the assembly language clock calls that I've seen! The CALL OUT (part, value) outputs an 8-bit number to any port you specify, and there is a corresponding A = INP (port) to input data from a parallel port (these two are not exclusive to Nevada Fortran). One of the most useful system subroutines is the CALL BIT (arg), which allows the setting, resetting, flipping, or testing of individual bits in a variable. If you don't like assembly language and are using a parallel port for instrument I/O, this one feature could save you weeks of programming time! There is also a RAND (arg) function for random numbers (not in Microsoft Fortran). And if you like structured programming, you can use the IF . . . THEN . . . ELSE construct.

Listing 1. Program for I/O timings

```
dimension x(4096)
do 10 k=1, 4096
10 x (k) = k
pause 'Begin?'
call open (8, 'DATA.DAT')
WRITE STATEMENT GOES HERE
endfile 8
write (1,1)
1 format ('All Done.')
end
```

Conclusion

After living with and using the Nevada Fortran for a couple of months, I conclude it is a remarkable bargain at $29. If you feel you would like to learn Fortran but cannot justify the $350 price tag, you no longer have an excuse. For the engineer or scientist, there are several enhancements that make this high-level language easier to use than most for instrument interfacing or real-time control. It is significantly slower than Microsoft Fortran in computations, but faster than interpreter Basic, and as fast or faster in disk I/O operations. The only significant ANSI 66 features not present are the lack of double precision capabilities and complex numbers; if you do not need these, then I think you will find Nevada Fortran completely satisfactory.

Nevada Fortran is available for $29.95 plus a $4 shipping charge from:

Ellis Computing
3917 Noriega St.
San Francisco, CA 94122
(415) 753-0186

CIRCLE 321 ON READER SERVICE CARD

Comments from Ellis Computing

Since this review was written, version 3.0 (released June 1983) has appeared. Many features that the author of this review criticizes have been changed in the new version. Part 1 of the manual has been expanded to 166 pages and contains an index. Three or four examples are now given for every command, and some of the commands have been rewritten to be more meaningful. Ten to 15 more sample programs have been added to the section at the end, and the installation procedure and other information for first-time users has been put in Chapter 1. Part 2 now has 46 pages and includes an index. The new version also has a double precision statement, although it is treated as single precision.

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Some Notes on Microsoft Fortran-80

by Robert S. Minnis

Fortran-80, Microsoft's Fortran for CP/M, is a very good product. In addition to the compiler and built-in subroutine library (F80 and FORLIB), the purchaser receives a linking loader (L80), a library manager (LIB80), a good relocatable macro assembler for Z80 as well as 8080 (M80), and a cross-reference generator (CREF80, which I have never used).

The price is reasonable: the list price is $500, but I have seen it advertised as low as $325 (although it is disconcerting that the cost for versions on Apple, Radio Shack, and some others is less than half the above discounted price for the CP/M version). I have owned version 3.34 of this product for about three and a half years, and have recently gained access to version 3.44 at work. Version 3.44 is the most current release. According to the Microsoft manual, "Updates to Fortran-80 are announced periodically and are available for a minimal charge." This was certainly true at one time, since my original version 3.2 was updated to 3.34 (paid for by the reputable dealer that sold me the package) soon after purchase, including a disk and new manual, through Lifeboat for $30. However, when I recently inquired about the latest update, Lifeboat quoted a price of $105, which seems more than "minimal." Microsoft's price is substantially less than that, but they will not provide updates directly unless the product was originally purchased from them. When I complained to Microsoft about the price difference, they said that their dealers could charge whatever they wished, and I should take any complaints to Lifeboat. In addition, Microsoft does not currently have a method of notifying owners of the availability of updates.

Nevertheless, even at $500, the product is a real value.

The output of the compiler (and the M80 assembler) is a REL file (the file type is REL, for relocatable). The REL file is a compact object file that contains linking and relocation information. L80 is used to combine these files, along with routines in FORLIB and optionally with routines from a user-created subroutine library, into an executible memory image. A COM file or Intel HEX file may be produced, plus a SYM file for use with Digital Research's SID or ZSID symbolic debuggers. A program listing may be produced on the console, on the printer, or in a disk file (or may be omitted). The linker does not use disk work files, so significant memory (apparently about 12K) is unavailiable for object code, though Fortran subsequently uses some of this memory for disk buffers and FCBs during execution, or the memory may be used dynamically by user-written routines.

The package appears to be very clean. However, there are a few problems of which the user should be aware, including at least one fairly serious bug.

First the bug. One of the nicest features of Microsoft's implementation of Fortran, particularly on memory-strained micros and where speed is important, is the ability to define one-byte integer variables (by use of the INTEGER*1, LOGICAL*1, or BYTE statement). Unfortunately, the one real bug that I have found in the package is right in the middle of this nice feature. It seems that in doing one-byte integer comparisons in which one of the variables is negative, such as in

```
IF (I .LT. J) ...
```

the test fails for many combinations of I and J. In particular, for the "less than" comparison, if I is negative, then the test fails when J is greater than or equal to -128+I. For the "greater than" comparison, if I is positive, then the test fails whenever J is less than or equal to -128+I. The range of values of a one-byte integer is -128 to 127.

By calling Microsoft's technical support department, I found that they were well aware of the problem. I was told that the problem probably will be fixed in the next release (date unavailable at this time). Since the problem exists in both versions 3.34 and 3.44, and that the time span on these versions is over three years, I am not going to hold my breath (even if I could afford the cost of the update). Fortunately, most of my use of single-byte integers is restricted to positive values, and this is the reason I only recently encountered the problem (at least as far as I know!). Unfortunately, as with update availability, Microsoft has not implemented a method of notifying owners of their packages about known bugs.

The second problem is actually the result of attempting to fix a problem in earlier releases. In 3.34, formatted output to disk files uses the first character of each output record as carriage control, just as for console or printer output. This first character is used to determine line spacing, and is not placed in the disk record. For single spacing, the most common case, each disk record is terminated in a carriage return (CR), followed by a single linefeed character (LF). If the carriage control character calls for double spacing, then two linefeeds follow the CR; skip to new page results in a formfeed character; a request for overprint results in CR only.

A serious problem with this is that every record, *except the first*, has one or more extra characters at the beginning (the CR is interpreted as the end of the record). Any attempt to read these records in character format, using the format codes A,H,X, or literal (single quotes surrounding the appropriate number of blanks) will misread either the first record or all except the first. The various format codes perform differently. Interestingly, using numeric format codes seems to work properly, as if the leading control characters were not there. Microsoft's solution, apparently beginning with version 3.36, is to stop using carriage control specifications in disk files, simply terminating each record with a CR only.

There are several difficulties with this solution. First, if TYPE is used to list the file, all you get to see is the last record. Similarly, using control-P to produce a printed list, on printers that do not perform an automatic linefeed on return, results in overprinting all lines. If the disk file is created with another program, including most editors, it cannot be processed properly by Fortran programs. Or if the file created with F80 is to be processed by a program

Robert S. Minnis, 1213 Hopkins Dr., Denton, TX 76201

that requires the linefeed, that program will not function properly. Finally, one cannot produced a formatted output to disk for later printing. Of course each Fortran program could explicitly output linefeeds and formfeeds at the appropriate points, but this is really a pain.

After complaining about both the initial problem and the solution, you are probably asking if I have a better answer to propose. I believe that I do. Fortunately, the source for the disk driver is provided as part of the package. My solution, on version 3.34, is simply to ignore the first leading linefeed on each record, if any. Implementing this fix requires about five lines of code added to the formatted read routine in the disk driver, which I was able to add before I really even knew 8080 assembly language. In version 3.44, however, the fix is more complicated, since the code to process carriage control characters must be reinstalled in the formatted write routine, as well as putting in the above-mentioned change.

Another minor annoyance also concerns disk file processing. When a disk file is read or written to, say to unit 9, the default file name used is FORT09.DAT. But F80 also provides an explicit OPEN routine, allowing the user to associate a specific filename with a logical unit number. This is a very imporant capability, but the OPEN routine provided is not very smart. It does not check that a valid filename has been passed, and if invalid, CP/M will obediently create the file, which then cannot be processed by most commands or programs, and cannot even be erased. (If by chance either the filename or file type part is valid, then a wildcard-type erase often can be used.) In addition, it is very easy to enter an invalid name to OPEN because the name must be exactly eleven characters, with the filename and file type parts each padded with blanks if not eight or three characters, respectively. For example, 'DATA________X____' for file DATA.X.

While converting from the external user form of the name to the format required by CP/M is not trivial, it sure would have been nice if this function had been provided. OPEN is actually part of the disk driver routine, and this could be modified by the user, but I chose to implement file name checking and formatting in a separate routine (written in Fortran, again thanks to those one-byte variables).

It should also be noted that when performing sequential output to a file, any existing file of the same name will be erased without notice. Therefore it is not possible to add data to the end of an existing file. This is true for sequential type output only; direct access writes will modify an existing file, or add records to the end.

The final problem I would like to discuss is not really a bug, but more a deficiency in implementation. Sure enough, Fortran's history is that of 80-column cards and fixed-length records. However, recent implementations for use specifically in an interactive environment certainly should be expected to remedy as many shortcomings as possible. A case in point in F80 is the situation in which it is necessary to read character strings that by nature are variable in length. If the maximum record size is 40 characters (a name, say), then each record must be padded with blanks to the full 40 positions. Both disk files and console input must be padded in this manner. I have heard this problem mentioned several times as a near-fatal failing of Fortran when used interactively. It would be highly desirable for the input routines to pad unfilled positions with blanks. This is not done in F80, but there is a simple and relatively painless solution. The I/O routines maintain an external variable named $BL, which contains the number of bytes transferred by the last I/O operation. Listing 1 is a function subroutine, written in assembler, to return this one-byte value. It also is possible, through some trickery, to retrieve $BL with Fortran subroutines.(see Listing 2). In either case, the function is referenced by

```
LEN = IOLEN(0)
```

The (0) is not actually required, but avoids the necessity of declaring the function as EXTERNAL. The function should be called immediately following the READ for which the length is needed, but certainly before a subsequent I/O operation. The value returned is minus the terminating carriage return.

Listing 3 is a subroutine, using IOLEN, which pads a variable to a specified length. Note that the above is not a problem when reading numeric variables, such as with I, F and E format codes; any variables "off the end" of the record are zeroed automatically.

I would like to conclude by discussing a few of the really nice features of this package.

At some point between 3.34 and 3.44, L80 was changed to reset the disk system periodically. This allows changing disks at any prompt, including just before writing out the COM file. Nice improvement! By the way, this is not documented in the manual.

Another feature added at some point is the ability to include statements from another file in the compile (the INCLUDE statement). This can be useful for COMMON statements or other sequences of code that are not appropriate for implementing as subroutines. The same capability is provided in M80, and can be used for including macros from a library, as well as for normal source code.

Free-format input is another highly useful feature. If numeric data values in a record, on disk or from the console, are separated by commas, the values need not be located in the positions called for by the format. For example, consider the following read and format:

```
      READ (1,10) I,J,K
   10 FORMAT (3I5)
```

Normally, this data record would be required:

```
___21__107_____5
```

However, in F80, this record would also be acceptable:

```
21,107,5
```

The only apparent restriction is that the field widths specified in the format are in effect as maximum lengths. For example, (3I2) could not be used, since the second data value is three digits long. The format (3I7) would be acceptable, however. Also, A format codes must be used with caution when mixed with numeric codes, since commas are valid character data and will not serve as separators.

Finally, statements are provided that allow moving data to and from variables (arrays) using formats, just like in reading and writing records (the ENCODE and DECODE statements). This facility has many uses, and is particularly useful for converting to and from internal characters forms, and for effectively reading the same record multiple times and with different formats.

The above are just the best of several important features of this package.

Many people claim that Fortran is a dead language (or should be), but the Microsoft implementation provides a very useful and productive system. The compiler is fast and the resulting program, while slower than assembly

Many people claim that Fortran is a dead language (or should be), but the Microsoft implementation provides a very useful system.

language, is fast indeed. The linking process requires considerable time, but the savings and convenience in being able to use previously written and compiled routines more than makes up for this. With the judicious use of assembly routines, one can program just about any application desired using Microsoft Fortran. In fact, this article was produced using a word processing program I wrote, originally using only Fortran. I later rewrote certain routines in assembly for faster execution.

More information on this product can be obtained from:

Microsoft
10700 Northup Way
Belleville, WA 98004
(206) 828-8080

CIRCLE 349 ON READER SERVICE CARD

```
        FUNCTION IOLEN (I)
        EXTERNAL $BL
        CALL $RECLN ($BL, IOLEN)
        RETURN
        END

        SUBROUTINE $RECLN ($BL, IOLEN)
        INTEGER*1 BL
        IOLEN = BL - 1
        RETURN
        END
```

Listing 2: *Two Fortran routines to perform the same function as the assembly routine in Listing 1.*

```
        TITLE   IOLEN  - GET LENGTH OF LAST FORTRAN I/O
;       SAMPLE CALL:            I=IOLEN(0)
;       'IOLEN' IS AN INTEGER VARIABLE
        ENTRY   IOLEN
        EXT     $BL
IOLEN:
        LXI     H,$BL    ;ADDR OF LEN
        MOV     A,M      ;GET LEN
        DCR     A        ;REDUCE FOR <CR>
        MVI     H,0      ;PUT IN INTEGER REGS
        MOV     L,A      ;<H,L>
        RET
        END
```

Listing 1: *A function to return the length in characters of the last I/O.*

```
        SUBROUTINE PAD (STR, LEN)
        INTEGER*1 STR(1), BLANK
        DATA BLANK /' '/
        IF (LEN.LT.1) RETURN
        IL = IOLEN(0)+1
        IL (IL.GT.LEN) RETURN
        DO 1 I = IL, LEN
1       STR (I) = BLANK
        RETURN
        END
```

Listing 3: *A subroutine, using IOLEN, to pad a string with blanks. STR is assumed to have been read using A format codes. Variable LEN is the length of variable STR, in characters (bytes).*

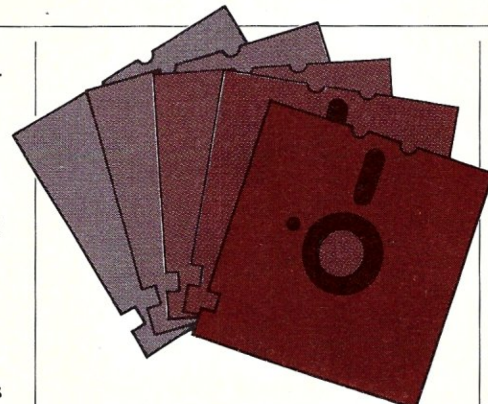
Software Directory

Program name: MBasic-to-Oasis Basic translator (MTRANS)
Hardware system: Any computer that can run under OASIS
Minimum memory: 64K in 8-bit; 320K in 16-bit
Language: OASIS Basic and OASIS Exec
Description: MTRANS is a utility that converts Microsoft Basic programs to executable OASIS Basic with little or no programmer assistance. When translated, all programs automatically support OASIS' multiuser functions, including automatic record locking and optional file locking.

MTRANS converts any MBasic program which has been saved in ASCII format and moved to OASIS via the GETFILE command. It displays each line of program text on the CRT screen as it is being converted, and informs the operator of any difficulty or errors in a brief report which may be written to a sequential file or printed on an attached printer. Errors are also clearly flagged in the code itself.

To accommodate the various versions of MBasic, MTRANS permits the operator to add, change, or delete items in the replacement table. A renumbering feature converts line numbers during the first pass of conversion, automatically splitting long lines as needed for logical execution. In addition, MTRANS enables the operator to enter the dimensions of the screen used by the original program and then reconfigure the size to accommodate virtually any CRT. Files may be opened with LOCK, FORMAT, and QUOTE options. The operator also may choose which output device will be used to store the MTRANS files.

The key element of MTRANS is a subroutine generator which allows the file-handling logic of Microsoft Basic to be used under OASIS. Generated subroutines include FIELD statements, GETs, and PUTs. MTRANS also creates functions to handle CVI, CVS, CVD, MKI$, and MKD$, along with PRINT@, RIGHT$, and VAL.
Price: 8-bit version of MTRANS, $245; 16-bit version (soon to be released), $345.
Included with price: MTRANS on appropriate disk, documentation, full reference guide, and technical support from Phase One.
Available from:
Phase One Systems, Inc.
7700 Edgewater Drive, Suite 830
Oakland, CA 94621
(415) 562-8085
CIRCLE 325 ON READER SERVICE CARD



Program name: 8086 OS converter
Hardware system: PC-DOS (MS-DOS), CP/M-86
Language: Object code
Description: The OS converter, produced by Dynamic Microprocessor Associates, permits PC-DOS (MS-DOS) object code to run on CP/M-86 microcomputers, and enables CP/M-86 object code to run on MS-DOS systems. Use of the OS converter involves no loss of speed, and will permit users to run such programs as Microsoft Basic and Fortran, Digital Research Pascal and other language compilers, as well as utilities like Microsoft ASSEMBLER and LINKER.

The new program operates by loading a target program into memory and creating the environment that the program expects. There is no interpretation of instructions; the program itself remains in control of operations.

The OS converter is 4K in size. When in use, it resides just above the operating system in RAM and enables the program being run to take full advantage in available memory. The OS converter for the IBM PC is supplied with a companion program that enables PC-DOS systems to read CP/M-86 files.
When released: May 1983
Price: $95
Available from:
Dynamic Microprocessor Associates, Inc.
545 Fifth Ave.
New York, NY 10017
(212) 687-7115
CIRCLE 328 ON READER SERVICE CARD

Program name: Database System
Hardware system: CP/M Plus
Minimum memory: 241K
Language: CB-80
Description: Tarbell Electronics has introduced an improved Database System for CP/M Plus. This system's added functions include multiline field type, multilevel sort, nested IF-ELSE, and user-creatable menus. DBQUERY now has features that were previously available only in the DBREPORT module. ATTACH and DETACH commands for MP/M printers are new, and it is now possible for several users to append data to the same file, with all data intact.

Nested IF-ELSE-ENDIF for command files are now part of DBQUERY and DBREPORT. New functions in both are upper case, ASCII character, length and index.

The entire system is more user-friendly. In the new Tarbell Database System CP-80, overlays are now used instead of .COM files for modules. This saves disk space, improves loading time, and allows sharing of common variables between modules.
Price: Complete system in ready-to-run form, $100; source code in CB-80, $200. Updates: $25 for database system only; $50 including source code.
Available from:
Tarbell Electronics
950 Dovlen Place, Suite B
Carson, CA 90746
(213) 538-4251
CIRCLE 329 ON READER SERVICE CARD

Program names: TRAKSPLAYER and TUNINGS
Hardware system: Soundchaser computer music system, Apple II+, Apple IIe, Franklin Ace 1000
Minimum memory: 48K
Description: Passport Designs, Inc. has added two new utility software packages to its software list. TRAKSPLAYER and TUNINGS allow Soundchaser users to greatly expand their musical imagination and enjoyment. TRAKSPLAYER is a "record player" program for four-track composition. It allows the user to produce albums by creating four-track musical selections. They may

then be played back in any order and repeated as many times as desired. Simply by loading the tracks into TRAKSPLAYER and organizing the playback, an album is produced. This utility also takes advantage of improved DOS and compressed file formats.

TUNINGS, the second package, is a collection of different four-track tuning files for the Soundchaser keyboard. This allows the user to experiment with a variety of tunings for exotic instruments such as eastern or ancient instruments. Included in the package are "Mean," "Just," "Tempered" and "Quarter" tone tunings. Several unusual tunings are also included to stimulate the user's creativity.

Price: TRAKSPLAYER: $75; TUNINGS: $50
Included with price: disk and instructions.
Available from:
Passport Designs, Inc.
116 North Cabrillo Hwy.
Half Moon Bay, CA 94019

Software Directory
continued . . .

(415) 726-0280
CIRCLE 330 ON READER SERVICE CARD

Program name: WS-Patch
Hardware system: CP/M 8″ SSSD, 5¼″ Osborne, Kaypro, Morrow, North Star, Epson QX-10, Apple (CP/M) card. MS DOS 5¼″ IBM PC and compatibles.
Language: Machine Code
Minimum memory: 64K
Description: Enhancement program for WordStar enables the user to access all of his dot matrix printer's capabilities through WordStar. WS-Patch also revises WordStar's print menu to include the new printing commands. Depending on the type of printer, WS-Patch may enable wide and condensed type, letter quality printing, continuous underline, sub and superscript, italics font elite, doublestrike, triplestrike, proportional spacing and various combinations. Programs available for Epson and Epson-compatible printers, Okidata microline printers and CITON prowriter printers. WS-Patch documentation comes on the

Software Directory
continued . . .

program disk. The documents print out of the user's printer. The file, which is a standard WordStar file, can be edited to see how the print commands are entered in the file and how they will print out.
When released: February, 1983
Price: $49.95
Included with price: appropriate disk, instructions, document file. IBM version includes WS-KEYS, a utility program that allows the user to redefine the IBM function keys in WordStar.
Available from:
CMB3
P.O. Box 3061
Walnut Creek, CA 94598
(415) 372-7733
CIRCLE 332 ON READER SERVICE CARD

Program name: Model EIS-110
Hardware system: 8086, 68000, Z-8000 class machines; any 16-bit or larger computer; any microcomputer
Minimum memory: 32K with application software
Language: C
Description: This versatile microprocessor-based, real-time operating system incorporates a number of unusual features designed to overcome man-machine interface problems. Among the numerous advantages of EIS-110 are: menu-driven command scanning that eliminates operator uncertainty; structured program commands that speed and simplify program writing and maintenance and minimize bugs; prioritized, responsive queue scanning for real-time capabilities; built-in data-reduction algorithms for conservation of memory while collecting data. The method of dispatching employed by EIS-110 is economical for analyzing a relatively small number of tasks and responding on a priority basis. Commands are prioritized, allowing high-priority commands, such as diagnostics, to be invoked while the machine is operating on a previously issued command. EIS-110, which uses COHERENT, a UNIX-compatible operating system, was used to drive a gas spectroscope in its initial application.
Available from:
Electronic Information Systems
360 Fairfield Ave.
Stamford, CT 06902
(203) 358-0764
CIRCLE 334 ON READER SERVICE CARD

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☐ Master Charge/Visa # ____________________

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☐ Osborne I ☐ Kaypro 4

☐ AppleII/Z-80 ☐ Other ________________

Please add shipping: $6 USA or $28 overseas

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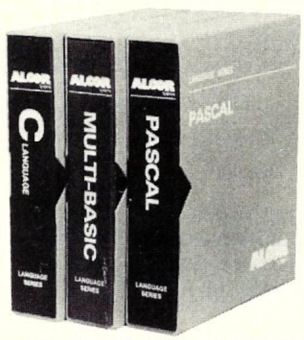
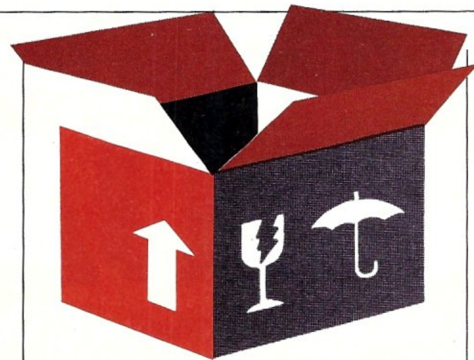
CP/M is a trademark of Digital Research Inc.



ALCOR Systems
800 W. Garland Ave. #204
Garland, TX 75040
214/494-1316

New Products

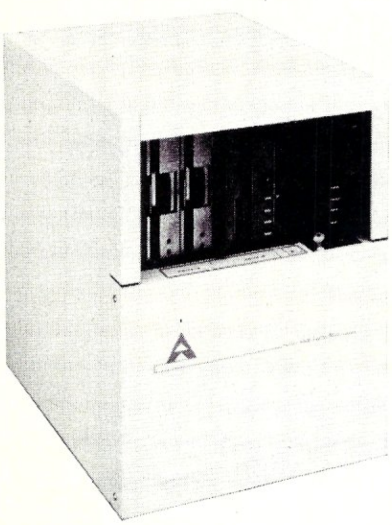


Series 8000 Turbo-Micro

The Series 8000 Turbo-Micro computer has recently been introduced in a stand-alone model. The Turbo-Micro is designed to provide an expandable, easily-serviced multiuser computer system that maintains industry-standard compatibility with thousands of applications written for the CP/M-80 operating system. It runs under the Turbo-DOS operating system with networking, record locking, password protection, and print spooling capabilities.

The Turbo-Micro is based on the S-100 bus, with 20 slots for user expansions, and the Z80 8-bit microprocessor. It runs at 6 MHz with 64 or 128K per processor board. It also offers a 16-bit processor board based on the latest Intel chip, the 186 CPU, with 128 or 256K per board.

The Turbo-Micro can support up to 30 independent users, each having his or her own CPU board and own memory, with 300 MB of disk storage using either 5¼″ or 8″ Winchester hard disk. Storage back-up is provided by either a cartridge tape or



½″ real tape drive. Each Turbo-Micro user controls a dedicated Z80B or 186 processor, 64 or 128K of memory, and four RS-232C I/O ports.

The system master processor board has a Z80B CPU with 128K of memory and two serial, two parallel ports. Its main function is to control the shared resources of floppy and hard-disk storage, floppy controller, DMA interface to hard disk drives, the real-time clock, and the traffic handling of all other processor boards.

The Turbo-Micro also features self-diagnostics and well-written technical manuals with schematics that make possible a mean time to repair of five minutes. Its modular design allows unskilled persons to replace components and disks by using a simple screwdriver.

The Turbo-Micro's 700-watt power supply is designed for system expansion. It has a constant-voltage transformer that eliminates line voltage fluctuation problems, separate line spike suppression, and a power sequencer for start-up and shutdown to protect electronic components. The power supply is protected by a double-pole circuit breaker and has two convenient AC outlets separately fused.

The system can be moved easily from one location to another, as it has caster rollers. Height: 26½″, width: 18½″, depth: 23½″; weight: 135 lbs.

Price: two-user unit, $11,000.

Advanced Computer Technology, Inc., *5575 Magnatron Boulevard, Suite D, San Diego, CA 92111; (619) 571-2746.*

CIRCLE 335 ON READER SERVICE CARD

ShareNet operating system

The core of every ShareNet, produced by Novell, Inc., is the Network Operating System. This proprietary operating system is designed specifically for the high-performance demand of networking personal computers. The ShareNet Operating System takes a universal file server approach that will support multiple types of personal computers with their various operating systems. ShareNet will function transparently to the local personal computer system. The intent of ShareNet is not to change the local operating system, but to be a natural extension to the networking environment.

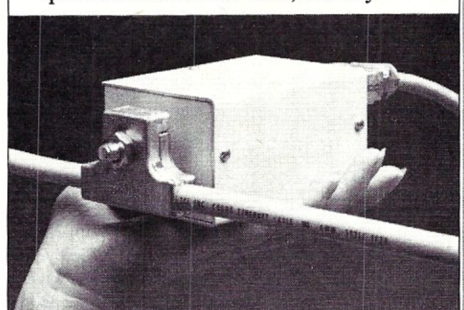
Novell is also offering a Public Bulletin Board and an Electronic Mail Service called HostComm. As new products are added to the Novell product line, they will be available first through this service. The phone number for HostComm is (801) 224-5740; it operates at 300 baud.

Novell, Inc., *1170 N. Industrial Park Drive, Orem, UT 84057.*

CIRCLE 336 ON READER SERVICE CARD

New Ethernet transceiver

TCL Inc. has developed an improved, easier-to-install Ethernet transceiver that features two new functions. The new transceiver, called the Model 2010EB, has both heartbeat and watchdog timer features. With the heartbeat circuitry, the transceiver informs the station connected to it that the collision detection circuitry is operational. The watchdog timer citcuitry limits the amount of data that can be sent out in a particular packet by cutting off the signal after a specified amount of time, usually



about 60 ms. Like other TCL transceivers, the new unit is designed to operate at a data rate of 10 megabaud.

A number of other features have also been added to the transceiver. First, instead of a fixed-pin stinger, the Model 2010EB features a spring-action stinger that is self-adjusting and maintains the right amount of contact with the center conductor of the cable. Second, the footprint of the transceiver's tap block around the cable has been increased to 2.2″. This lessens the chances of losing contact between the stinger and the cable. Third, nonskid ribs have been added on each end of the tap block

where it attaches to the cable to further reduce the chances of disconnection when the cable is twisted. Finally, the number of ground pins has been increased from two to four to ensure a solid connection between the tap block and shield.

Dimensions: 2⅛" x 2¾" x 4".

Price: $232.80, tap block included. Special cable drill, $11; shield remover tool, $21.50; insulation piercing tool, $19.80.

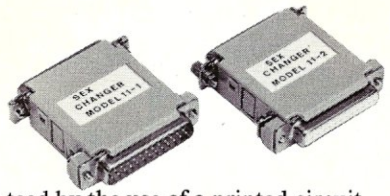
TCL Inc., *2066B Walsh Ave., Santa Clara, CA 95050; (408) 727-3800.*

CIRCLE 337 ON READER SERVICE CARD

Sex changer

The Remark Datacom Div. of Telebyte Technology, Inc., has announced the availability of their Series 11 Sex Changer modules to provide a low-cost method of altering the polarity of an existing data cable, terminal, printer or modem. The Model 11-1 is designated male-to-male, whereas the Model 11-2 is female-to-female.

Integrity of the 25 electrical paths of the RS-232 connector is guaran-



teed by the use of a printed circuit board, allowing the connection of mismatched RS-232 devices.

Price: $24.95 each.

Remark Datacom Div. *of Telebyte Technology, Inc., 148 New York Ave., Halesite, NY 11743; (516) 423-3237.*

CIRCLE 338 ON READER SERVICE CARD

Naked Mini 4 family expanded

The NM 4/12—newest member of Computer Automation's Naked Mini 4 family of computer systems—offers high-performance 16-bit functionality at a cost reduction of as much as $745 per unit over the NM 4/10.

The half-card NM 4/12 processor features 128K of on-board, dynamic RAM memory addressable in byte or word mode, and is fully compatible with all NM 4 hardware and software. State-of-the-art VLSI technology is used in the NM 4/12, giving the processor its 16-bit, high-level functionality. Its architecture includes eight programmable registers, six levels of priority-vectored interrupts, seven processor traps, direct memory access, and auto and programmed I/O data transfers.

The NM 4/12 uses current bipolar and NMOS memory technology to provide 128K of dynamic RAM. By placing the memory on-board, instruction and data retrieval times are reduced. Active DMA execution allows processing to occur in parallel with direct memory transfers when RAM references are not required.

Up to 32K of on-board EPROM is available in optional sockets provided for the user. Under software control, the EPROM can be enabled or disabled, overlaying the top portion of the NM 4/12 address space. A switch-selectable option allows program execution to begin at the first EPROM address upon power-up. Standard option is for cold-start boot

New Products
continued . . .

from the first available I/O device upon power-up or console-initiated autoload.

Additional memory features include a byte parity check to maintain system integrity and the provision of RAM battery backup terminals (requires +5V regulated). For applications requiring regulation of battery power, a low-cost half-card option with DC input range of 6 to 12 V is available.

The NM 4/12 is supported by three of Computer Automation's operating systems: OS4, RTX4, and OPUS-1. The OS4 is a disk-oriented programming system that includes a comprehensive set of software for developing and executing programs. The RTX4 (Real-Time Executive) provides the basic tools necessary for building real-time application environments. The OPUS-1 is a multiuser, multitasking system that automatically allocates memory and disk resources, and accommodates up to 16 I/O devices.

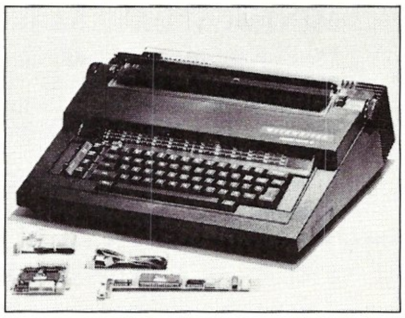
Price: $1,600 in single-unit quantity.

Computer Automation, *Naked Mini Division, 18651 Von Karman, Irvine, CA 92713.*

CIRCLE 339 ON READER SERVICE CARD

Printers and interfaces from Bytewriter

Bytewriter has added two new printer/typewriters to their line and is selling interface kits as well. Until now, the Bytewriter was offered only



as a complete daisywheel printer based on the Olivetti Praxis 30 typewriter. With the increasing availability of the Praxis series typewriters from discount stores, the demand for the interface in kit form has increased. Now, owners of a Praxis typewriter can install the interface themselves and in less than an hour can be outputting letter-quality printing from their computer.

New Products
continued . . .

The interfaces are available for the Praxis 30, 35, and 40 typewriters and are prewired and tested for a retail price of $165.

In a further effort to bring inexpensive letter-quality printing to the computer world, the normal dealer markup has been taken off the retail price. Thus the Praxis 30 Bytewriter has been reduced from $695 to $495. The Praxis 35 and the new Praxis 40 are also available now as completed printer/typewriters priced at $545 and $645, respectively. As with the Praxis 30, the interface fits entirely inside these machines. Only a cable is needed between the computer and the Bytewriter, and these are also stocked by Bytewriter.

Bytewriter, *125 Northview Rd., Ithaca, NY 14850; (607) 272-1132.*
CIRCLE 340 ON READER SERVICE CARD

Speedpro-5

The Speedpro-5, which consists of a Zilog Z80B microprocessor and support circuitry mounted on a PC board that piggybacks onto the main board of the Kaypro, significantly

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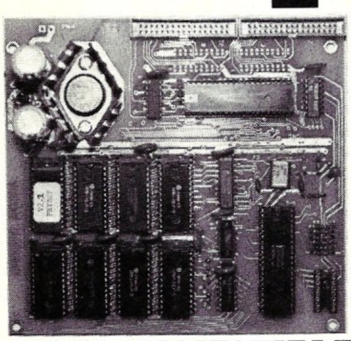

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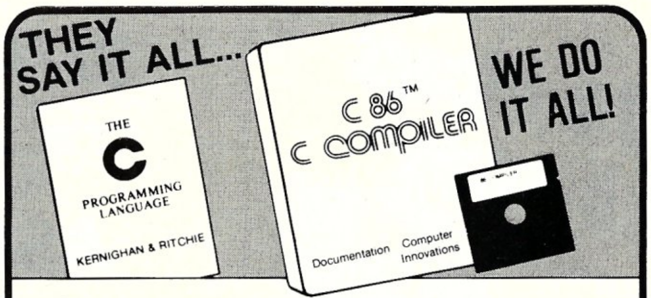
- **ISAM** products and products compatible with C86 and with OPTIMIZING C86 are available from some of our customers. **Graphics** and **screen** manipulation function libraries are available. Ask for a product list.
- **C_to_dBASE™** is in Beta Test by CI. It is a package to interface C86 with dBASE files. Heavily annotated source to the product and a function library are included. Save time and learn C86 quickly.
- A C86 **User's Group** is being formed.



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CIRCLE 209 ON READER SERVICE CARD

improves the utility of the Kaypro II and IV portable computers. It doubles the processing speed from the standard clock speed of 2.5 MHz to 5 MHz, making the Kaypro one of the fastest 8-bit micros on the market. A DIPswitch on the Speedpro-5 board allows the user to select double speed, standard speed, and zero or one of the wait states.

The Speedpro-5 is fully compatible with all CP/M software used on the Kaypros, considerably improving response times, particularly for Perfect Calc and the S-Basic compiler.

Installation of the Speedpro-5 is quite simple and can be done by either the dealer or purchaser. All connections are by ribbon cable with DIP connectors, so no soldering is required. Complete installation and operating instructions are included.

Price: Speedpro-5 is available through most Kaypro dealers for $74.95, customer installed.

Digital Dynamics, *P.O. Box 5653, Tacoma, WA 98405; (206) 627-0797.*

CIRCLE 341 ON READER SERVICE CARD

Static control mat

Protech Data, Inc., has introduced a static control computer mat designed to safely dissipate the static charges that can cause extensive damage to both software and hardware, such as erratic data transmission, loss of program, damage to disks, and even component failure.

Protech's static control mat is placed under the computer, and static discharge is accomplished by

touching the mat with the hand before operating the computer or accessories.

Price: $79.

Protech Data, Inc., *P.O. Box 2472, South Portland, ME 04106; (207) 799-0124.*

CIRCLE 342 ON READER SERVICE CARD

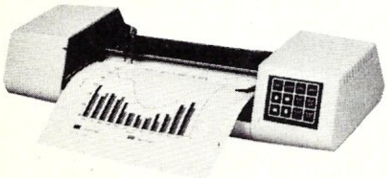
"Dancing Sailors"

A new option is now available for Houston Instrument's DMP-40 plotter. Dubbed the "Dancing Sailors," this dual-pen assembly enables DMP-40 users to generate two-color plots or plots employing different line widths, all without operator intervention.

Taking advantage of the firmware already resident in the plotter, a simple command directs the DMP-40 to place the alternate pen in plotting position. Since both pens are carriage mounted, pen changes are fast and certain.

The DMP-40 can be ordered with the dual-pen option already installed for $995, as the DMP-40-2. Also available as a factory or authorized-dealer conversion, retrofitting provides owners a quick and reliable way of obtaining multicolor plots.

Houston Instrument *(a Division of*



Bausch & Lomb), 8500 Cameron Rd., Austin, TX 78753; (512) 835-0900.

CIRCLE 343 ON READER SERVICE CARD

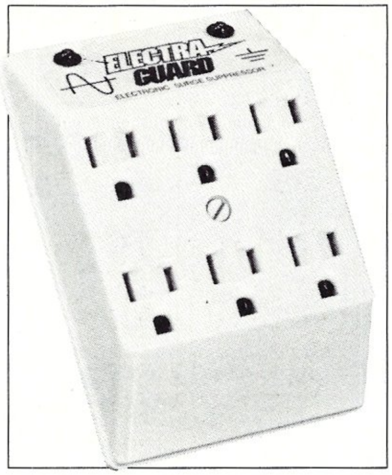
Electronic surge supressor

Computer Power Solutions, Inc., has added a new model to its line of surge supressors for AC power lines. The Electra-Guard System 2 is a solid-state clamping device designed to eliminate undetected submicrosecond overvoltage transients from electrical circuits. Commonly referred to as "spikes" or "glitches," these transients can cause computer hardware and software damage to unprotected circuits. The Electra-Guard System 2 expands a standard two-outlet power receptacle to provide six outlets, and offers a very inexpensive answer to potential equipment damage.

Threats to electronic equipment come from many quarters. On-line disturbances could result from sudden power-line voltage increases when certain kinds of equipment are switched on or off, or from malfunctioning voltage regulation. Off-line disturbances could result from lightning striking nearby.

Noise, voltage spikes, radio hash, spark transients, and other unwanted elements can appear on power lines from any number of everyday devices such as radio transmitters, appliances, power tools, neon lighting, and more. Electronic surge suppressors are designed to eliminate overvoltage transients from circuits, protect mini and micro computers, and sensitive computer-controlled equipment. Without such protection, computer logic can become scrambled, and memory banks can be lost.

The Electra-Guard System 2 (15 amps at 120 volts AC) can handle six devices not exceeding 1875 watts, providing line-to-line and line-to-ground clamping protection with a response time of less than 5 ns to overvoltage spikes and surges, and is compatible with 50 Hz and 60 Hz AC power mains.



Price: $49.95.

Computer Power Solutions, Inc., *8800 49th St. North, Suite 203, Pinellas Park, FL 33656; (813) 544-8801 or (800) 237-6010.*

CIRCLE 344 ON READER SERVICE CARD

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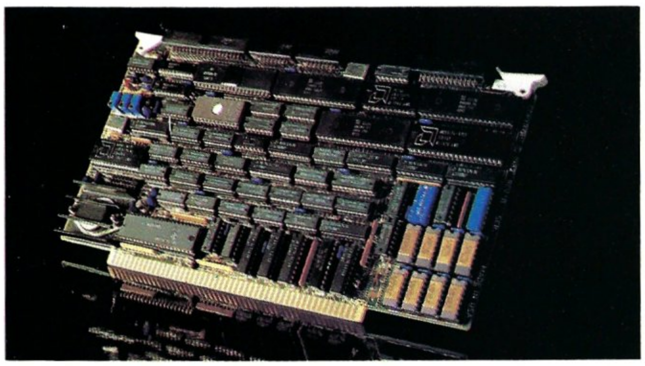
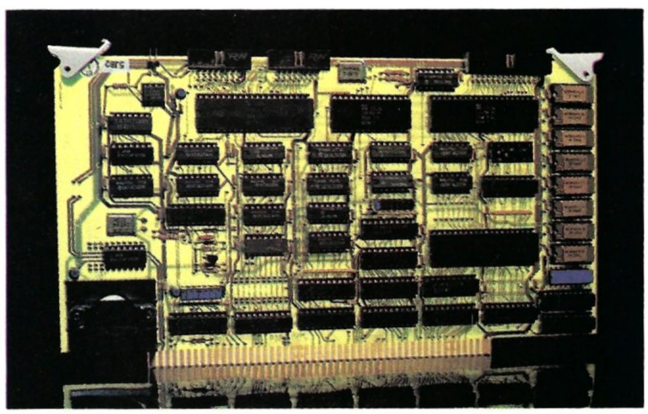


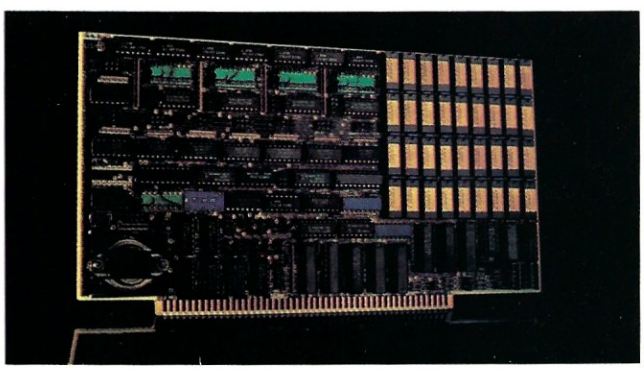
1 CPZ-48000 SINGLE BOARD COMPUTER.

□ IEEE 696.1/D2 S-100 compliance. □ Z80A,™ 4MHz Operation. □ Floppy disk controller (FDC). Single or double sided. Single or double density. 8" or 5¼." □ Two synchronous or asynchronous serial I/O channels (SIO). □ Two parallel I/O channels (PIO). □ Four channel DMA controller. □ 64K on board RAM. □ Memory management unit (MMU). Addresses up to 16 megabytes of system memory. □ Eight Vectored priority interrupts. □ Provisions for 2K or 4K onboard EPROM. □ Software selectable baud rates. □ IBM Bisync, HDLC, SDLC and other protocols. □ CP/M,™ MP/M,™ and TurboDOS™ operating systems available. □ Turbo-Disk® implementation included.

2 CPX-MX SLAVES.

□ IEEE 696.1/D2 S-100 compliance. □ Compatible with CPZ-48000 SBCP, any Z-80A based CPU with extended address capability or 16 bit based CPUs complying with IEEE 696.1/D2 bus specification. □ Z-80B™ 6MHz (CPS-6X) or Z80A 4MHz (CPS-4X) operation. □ Two synchronous (CPS-MS) or asynchronous (CPS-MA) serial I/O ports. □ TurboDOS™ & CP/NET™ compatible. □ Master confiscation of slave memory for diagnostic purposes. □ Two parallel I/O ports; eight data bits + 2 handshake lines per port. □ 64 Kbytes of onboard dynamic RAM. □ Master/slave memory-to-memory transfers under DMA control @ 571 Kbyte/sec transfer rate when used with CPZ-48000 SBCP. □ Software selectable baud rates. □ Usable as an intelligent I/O processor in single user system.



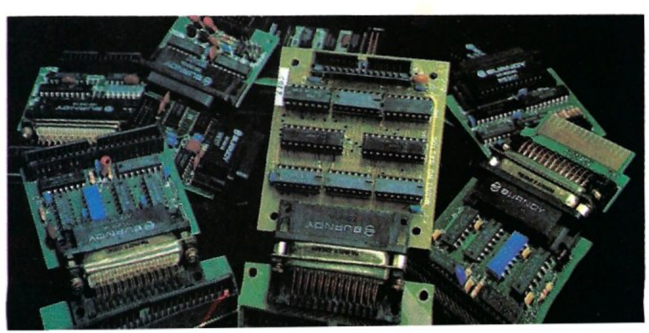


3 256KMB-100 256K MEMORY.

□ IEEE S-100 bus, spec 696.1/D2 compliance. The 256KMB-100 is compatible with most IEEE S-100 board products now on the market. □ Linear addressable to 2 megabytes. □ 225 nanosecond access time, maximum, 160 nano-seconds, typical. □ 295 nano- second read-write time, minimum. □ Bank selectable 16K increments. □ I/O port address bank selection. □ Configures for phantom deselection. □ Parity error detection, visual and/or interrupts. □ Bank selection compatible with CROMIX,™ CP/M2.2,™ MP/M,™ Alpha Micro, and other major systems.

4 PERSONALITY BOARDS.

□ Centronics printer. □ 8 inch floppy disk. □ 5¼ inch floppy disk. □ RS232 serial communications. □ Synchronous/asynchronous modem. □ Priam smart/smart E hard disk. □ Long distance serial communication (2000 ft @ 9600 baud). □ Shugart Associates Systems Interface (SASI). □ Clock/calendar. □ Konan David, Jr.™ hard disk. □ Archive tape drive.



INTERCONTINENTAL MICRO

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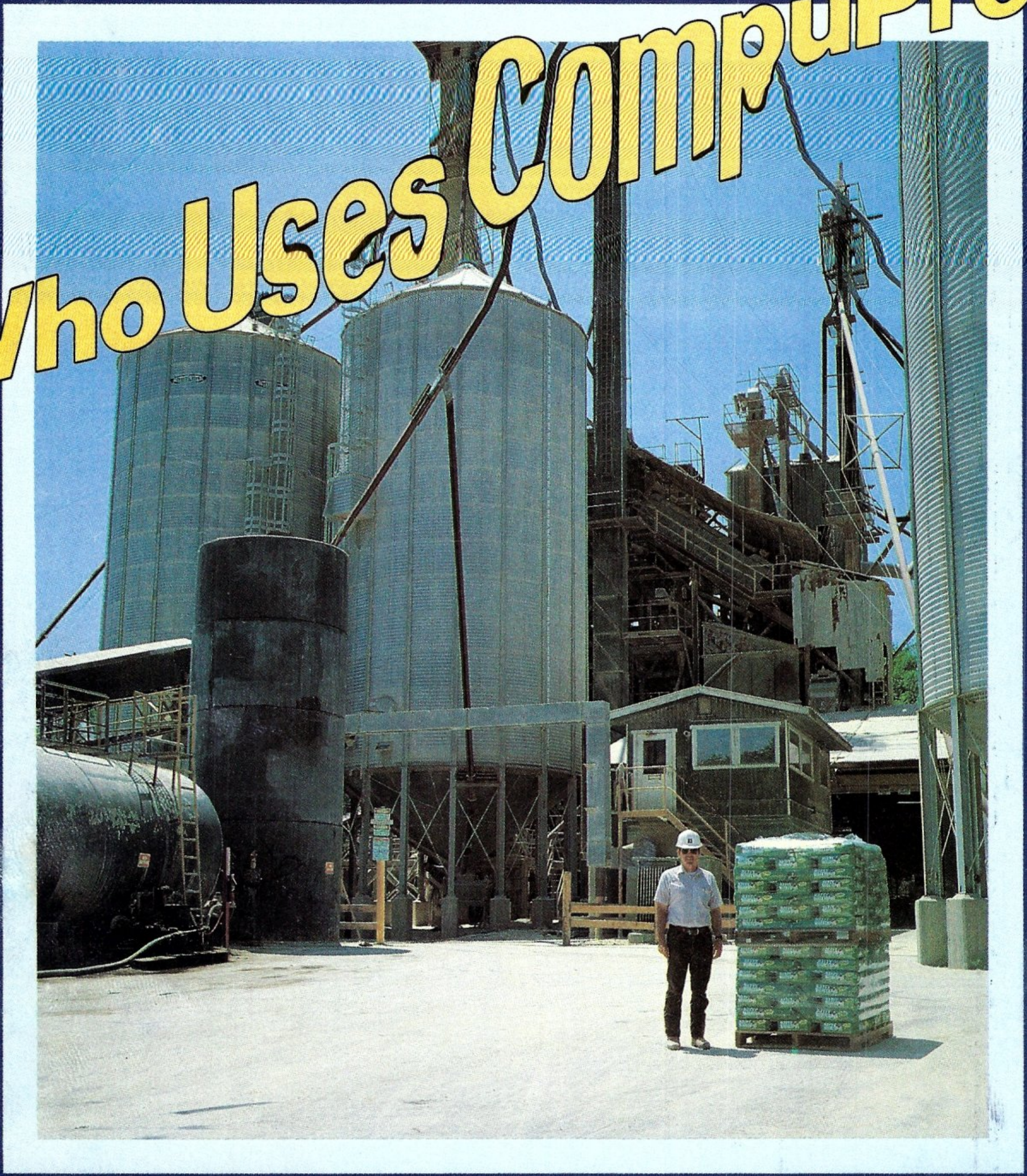
Who Uses CompuPro?



Although it owns a large minicomputer, Mid-Florida Mining Company is turning more and more frequently to its microcomputer—made by **CompuPro**.

"It's more flexible," explains Allen Edgar, president of the tri-state operation that turns a unique absorbent clay into a broad line of products ranging from cat litter to jet fuel filtrate.

The problem with the mini, according to chief financial officer Michael Wilkinson, is that modifying its programs requires expensive and time-consuming outside programming. By contrast, the firm is adding new applications to the **CompuPro** so fast that in one year it has taken on inventory control, production scheduling, sales figures, invoicing, customer lists and even executive flight planning.

In clay mines and board rooms, **CompuPro** delivers performance, quality and reliability. For your business, scientific and industrial computing solutions, contact a **Full Service CompuPro System Center** today; call **(415) 786-0909**, ext. 206 for location.

Mid-Florida Mining Company's **CompuPro** system was integrated by Micro Computer Technology of Brandon, Fla., a **Full Service CompuPro System Center.**

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