THE CP/M USER'S JOURNAL

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Microsystems

Volume 4/Number 2

February 1983

CP/M Plus—4 to 10 times faster, with enhancements that take advantage of large memory and large disk space

CP/M Plus

This month we start coverage of the new, greatly enhanced version of CP/M from two points of view. First is an article by David Hardy and Kenneth Jackson, giving an overview of the features and the differences from version 2.2. We also present the first of Bruce Ratoff's two-part series on the implementation of CP/M Plus for a banked-memory system.

Triple-Density Floppy Disk Storage

Bob Weidemann shows that small sector size results in a large overhead of storage space inaccessible to the user. He presents a scheme for choosing a sector size that increases disk capacity from 480K (standard double-density) to 660K or more.

Microcomputer Troubleshooting

Ron Derynck discusses both external and internal sources of trouble, and methods of neutralizing these gremlins. He also presents systematic methods of isolating malfunctions to a particular part of the system and quick ways of correcting them.

State-of-the-Art Hardware

The new Electrically Erasable PROMs can be reprogrammed byte by byte under software control. Randy Reitz gives us a design for a wire-wrapped EEPROM board—the first such design to appear in any magazine.

David Hardy reviews four of the most modern S-100 SBCs in depth. Each of these boards can be used as either a master or a slave in single or multiuser systems and contains a CPU, timer/counters, 64K of memory, a disk controller, and I/O ports.

Bill Machrone reviews the Morrow Designs Micro Decision—a fast, compact, dual-drive CP/M system in the under-$2200 price range.

Ian Darwin reviews a versatile PROM programmer—the Promblaster, from ADS, which handles many different chip types.

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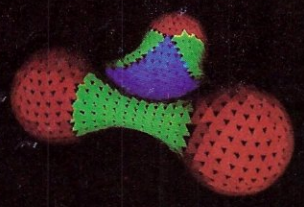

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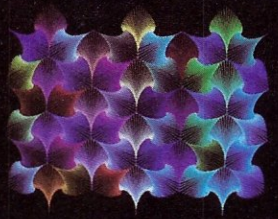

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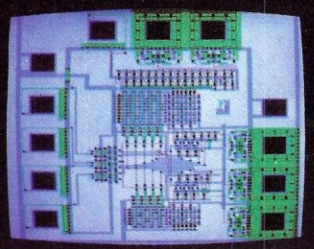

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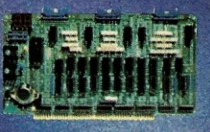

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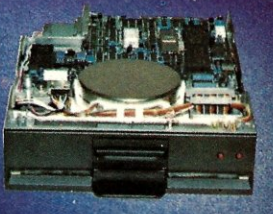

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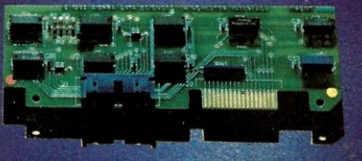

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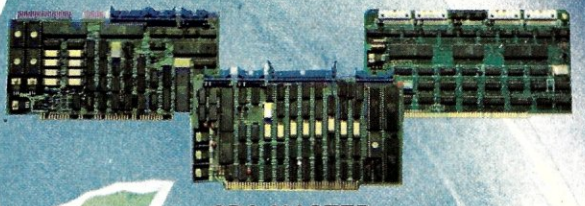

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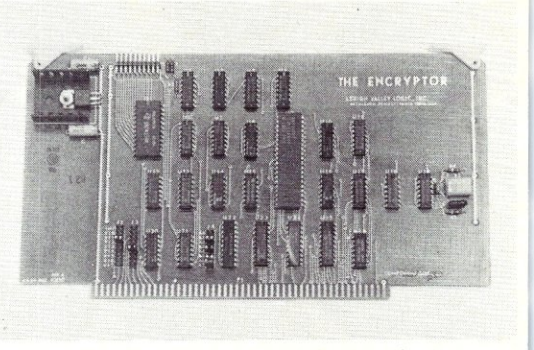

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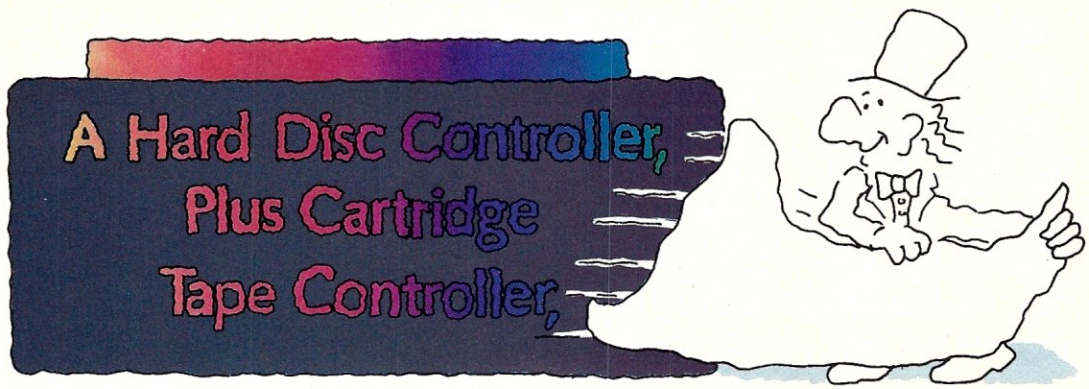

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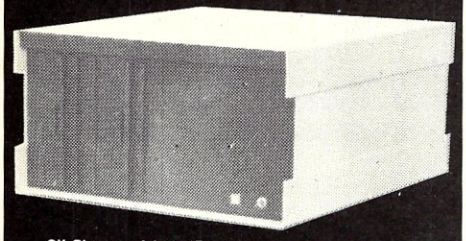

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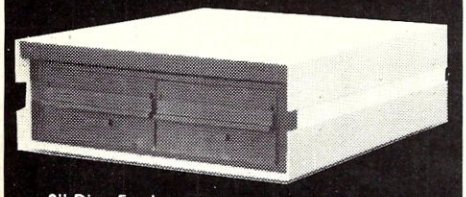

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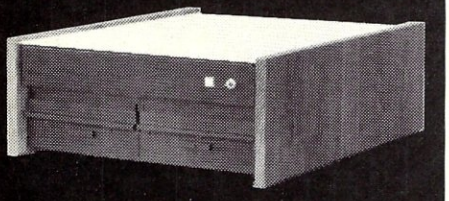

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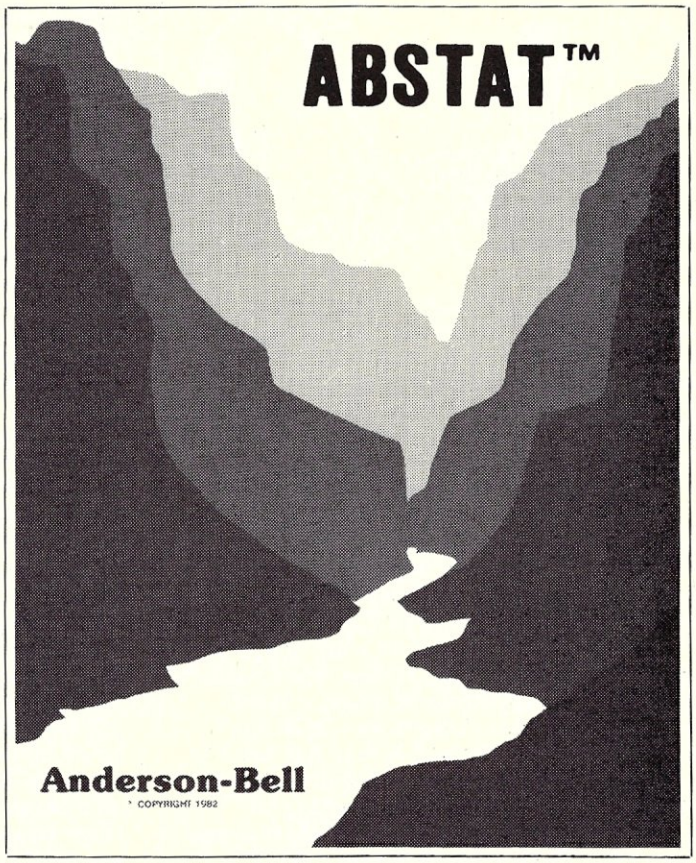

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CIRCLE 86 ON READER SERVICE CARD

Editor's Page

by Sol Libes

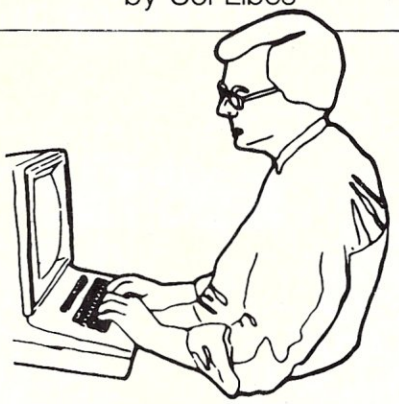
I can still remember way back in 1974 when, together with some of my students*, I got my first microcomputer system up and running. It used an 8008 microprocessor and was built from a set of plans that was published in Radio-Electronics magazine. It had 256 bytes of memory. We entered a few simple programs via a set of switches and watched them control some lights. It was a real learning experience!

A year later we built an Altair 8080 kit system with 1K of memory. We again played with the front panel switches and lights. Then we added a serial interface card and teletype. We had a little monitor program (256 bytes) that we stored on papertape and loaded each time with a simple loader routine that we entered manually each time we got the system up and running.

Early in 1976 we moved up to a 1702, 256-byte ePROM, a Tarbell cassette interface, and expanded our memory to 8K. We now had a system on which we could run the first version of Microsoft Basic and store files on audio cassettes. It was a real hassle to use, but by comparison to what we had previously, we thought that we were really flying along.

In 1977 we built a Tarbell disk controller and plugged it into our Altair. With the kit, Tarbell provided a floppy disk containing a thing called "CP/M". It took a while to work out some hardware bugs and work with manuals that assumed you had extensive knowledge of Disk Operating Systems. Fortunately, we had the assistance of several knowledgeable members of the Amateur Computer Group of New Jersey to help, and we got the system to run.

I cannot describe our feelings when we heard the clicking noise from our disk drive and then saw the "a>" appear on our teletype. Then to type "DIR" and immediately see a



listing of all the files on the disk. Wow, were we in heaven!

It amazes me to realize that when we had discovered CP/M, back in 1977, it was already four years old; that even while we were building our primitive 8008 microcomputer system back in 1974, CP/M was already in existence.

But then again, little did Gary Kildall know the consequences of his efforts to write a little program to control a prototype Shugart disk drive with an Intel microprocessor development system way back in 1973. In fact, it was not until IMSAI, a manufacturer of an Altair look-alike seeking to compete with a Disk Operating System introduced by MITS, heard of CP/M and, in 1976, came to Gary and asked him for a license, that he began to realize that he had something. He then did additional work on it to make it a more complete DOS and added utilities to make it a full development system. This became known as version 1.4. And in 1977 Gary formed Digital Research Inc. (DRI) to license and market CP/M.

MITS seemed to do everything wrong when it came to disk systems. They chose to not use the IBM disk format, would only sell through their franchised dealers (of which there never were more than 50), promoted the system as being a complete business system, and put it out of reach of hobbyists. The truth was that they were having innumerable software and hardware problems, did not have the production capacity to meet the demand, and did not have the applications software they were advertising. Processor Technology Co. also tried to deliver its own disk operating system, but had problems similar to MITS. On the other hand, IMSAI and several other suppliers (e.g., Tarbell) promised nothing more than a disk-based development system within reach of hobbyists, and they delivered on their promises. The result was that by 1978 CP/M was firmly established as the de facto standard for microcomputer systems.

CP/M version 1.4 was written to be a basic programmer's development system that could run on a small system (with as little as 16K of RAM). Applications programmers quickly wrote packages to run under CP/M. Also, hardware cost was dropping and system features were expanding. Thus, in 1979 DRI introduced version 2.2 with expanded facilities tailored to working with larger memory, larger disk storage, and better file handling for more powerful applications programs. In 1981 CP/M-86 and MP/M were introduced. In 1982 Concurrent CP/M-86 and CP/M-68K were brought out.

Recognizing that the 8-bit world is still a growing and expanding world (more new 8-bit systems were introduced in 1982 than all 16-bit micros combined), DRI upgraded CP/M to version 3, or, as DRI now calls it, "CP/M Plus". It is therefore with great pleasure that we place special emphasis on CP/M Plus in this issue. Also, in next month's *Microsystems,* and for several issues afterward, we will present an in-depth series of articles on CP/M Plus, just as we did for CP/M 2.2.

**For those of you who are not already aware of it, I am a Professor of Electronics Technology at Union County College in New Jersey.*

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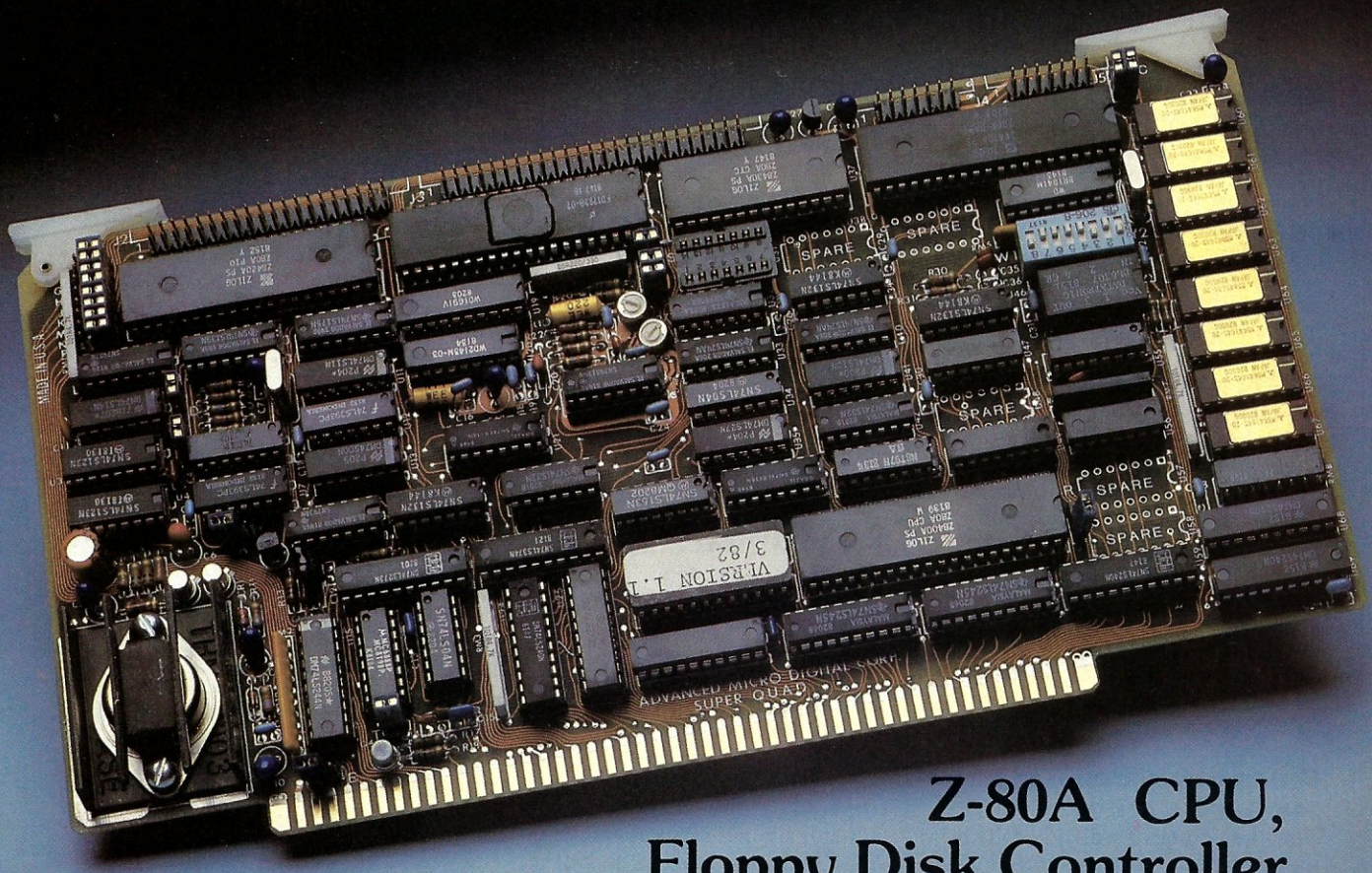

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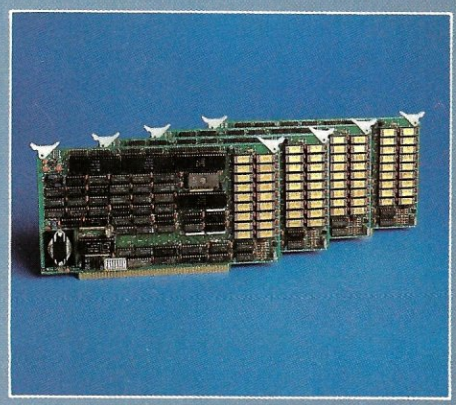

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News & Views

DRI rumor

Digital Research is rumored working on a C-language compiler. If this is indeed true, does this mean that DRI is going the UNIX route? After all, the big advantage that C has over other system development languages is that it is the language used by UNIX programmers.

ZCPR version 2

A new version of ZCPR is due for release into the public domain shortly and will be known as version 2. It will have user-definable paths. The user will be able to search explicitly. Also it will have utilities for named file structure and user area security. ZCPR will be available via many RCPM systems and via the SIG/M user group. ZCPR is an enhanced Z80 version of the CP/M CCP.

Content-addressable memory introduced

The first content-addressable memory for S-100 systems has been introduced by Racom Decision System Division, 5 Neston Way, Handforth, Wilmslow, Cheshire, SK9 3BX, England. Content-addressable memory provides faster file searching, text processing, and pattern recognition.

New CP/M public domain software releases

The CP/M Users Group (CPMUG) has released five new volumes of Software (Volumes 86 through 90). They are a five-volume set containing a package entitled "Businessmaster II," which includes programs for inventory/fixed asset accounts, mail list, payroll, purchase order/payables, order entry/receivables and general ledger. The programs are written in CBasic 2. This package was previously sold commercially and has been superseded by an updated version, allowing the old version to be put into the public domain. The disks are available from: CPMUG, 1651 Third Ave., NY NY 10028.

The SIG/M User Group (a subgroup of the Amateur Computer Group of New Jersey, Inc.) has also released five new volumes, raising their total to 80 volumes. The disks are available from SIG/M, Box 97, Iselin NJ 08830.

Foreign CP/M user groups

The following are three user groups we have learned of outside the U.S. If you know of any others, we would like to hear of them and publicize their existence.

CP/M Users Group (UK), 72 Mill Road, Hawley, Dartford, Kent DA2 7RZ, England; tel: (0322)22669, is a very active CP/M group in England. They publish a quarterly newsletter and distribute both the CPMUG and SIG/M public domain software disks.

CP/M gebruikersgroep Nederland (Hobby Computer Club), Secr.: Trajanusplein 1 - 4041 AK Kesteren, Netherlands; tel: 08886-1667, is a CP/M users group in the Netherlands with approximately 1,000 members. It is a subgroup of the Hobby Computer Club, which has 10,000 members. They hold regular meetings, distribute both the CPMUG (U.S. and U.K.) and SIG/M software disks, and publish a catalog listing the software.

UCSD p-System Users' Group (UK), c/o Mark Woodman, Open University, Mathematics Faculty, Walton Hall, Milton Keynes MK7 6AA, England.

New publications worthy of note

A newsletter for owners of the "Big Board" CP/M system, called *Micro Cornucopia*, is being published (Box 223, Bend OR 97709). Six issues/year are $16. Each issue averages 24 pages and is packed with hardware and software hints for Big Board system owners.

The third edition of the *CP/M Software Index*, listing 1,688 CP/M programs from 507 vendors, has been released by Small Systems Group, Box 5429, Santa Monica CA 90405, (213) 392-1234. Single copies are $10, prepaid ($14 outside North America).

A new publication joins the ranks of magazines directed to CP/M users. Called, appropriately enough, *CP/M Review*, it is published six times a year by the CP/M Review Co., 2711 76th Ave SE, Mercer Island, WA 98040; price is $18/year. It appears to be oriented to the beginning CP/M user.

S-100 Bus Standard adopted

The IEEE S-100/IEEE-696 Bus Standard for microcomputers is now an official standard (having passed the working committee, the Microprocessor Committee, Computer Standards Committee, and the IEEE Standards Board). Credit for development of the Standard goes to George Morrow (Morrow Designs) and Kels Elmquist (Ithaca InterSystems) for drafting the orginial standard, and most particularly to Mark Garetz (CompuPro) who finalized the standard and piloted it through the committees for final adoption. It is expected that the Standard will be published in final form by the IEEE, and we hope to get permission from the IEEE to publish it in its entirety in *Microsystems*. In the meantime, to find out how to receive a copy of the Standard, send a stamped, self-addressed business-size envelope to Mark Garetz, CompuPro, Box 2355, Oakland Airport, CA 94614. Enclose a note requesting information on the availability of the Standard.

Errata

We apologize for the errors that crept into "The UNIX File" in the January 1983 issue. In col. 1, par. 1, "Kernighan and Ritchie" should read "Thompson and Ritchie." In col. 3, line 39 should read "Brian W. Kernighan is one of the early developers."

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CIRCLE 9 ON READER SERVICE CARD

Letters to the Editor

Dear Editor,

After looking over the new "look" of *Microsystems,* I find that I approve, for the present. I do like the contents on the cover and the expanded coverage of other operating systems. Oasis in particular has been ignored for some time. When I can afford it I will be running it.

An increase in the coverage of home-built hardware would be appreciated. It is now dwindling to nothing in nearly all the magazines. I have to believe that when the home hardware articles stop, then the S-100 Bus is dead. While the IEEE standard is now in effect, the designs that one sees are almost never S-100. These are particularly missed because, having no skill in design, I can only mimic others.

I would like to see intelligent board designs: for instance, a version of the clock that Chris Terry did recently (throw in the hardware random-byte generator), or an intelligent speech synthesizer like that of Ciarcia's, or a Z80 controlled noise/music generator.

The CPMUG volumes of public domain software are published as they become available, but other sources are not. A nice addition would be a catalog and abstract of the new SIG/M volumes. The first 60 are well documented, but how about the more recent ones?

Carl Camper
POB 877
Colstrip, MT 59323

Dear Editor,

Thank you for publishing Andrew Bender's "Three Macro Assemblers," (Jul/Aug '82). His candor in describing Macro-80's unusable manual is to be commended. My personal copy serves only as a $151 reminder to "buy the manual first." The documentation states "it defines, explains and gives examples of all the features in terms that should be understandable to any one familar with assembly language programming," and then wastes scarce examples by using 8086 code for unique Macro-80 pseudo ops. The intro ends with "The user should refer to instructional material available from a variety of sources." At least that statement isn't misleading (it isn't anything). In buying Macro-80 for a software tool, I feel I bought a hammer without a handle!

I'm thankful for all the growth in microcomputing in that, when I bought my 8086 assembler, I didn't have to (and didn't) consider Macro-86.

Bob Johnson
565 Mohawk Dr. A-5
Boulder, CO 80303

Dear Editor,

Microsystems's readers may be interested in the following idea for enhancing their standard CP/M-based computers.

When configured for 8-inch single-sided single-density disks, CP/M reserves the first two tracks (track 0 and track 1) for the operating system, and the first 16 logical sectors on track 2 for the disk directory. It allocates the remaining disk space to files. The remaining disk space, ten 128-byte sectors on track 2 plus 26 128-byte sectors on tracks 3 through 76, totals 241.75K. File allocation is done in 1K increments, however. Therefore, on a standard CP/M disk there are 0.75K or six sectors that are never written to or read from by the operating system.

The unused sectors are physical sectors 18, 24, 4, 10, 16, and 22 on track 76 (assuming the standard sector skew factor of 6 is employed), corresponding to the last six logical sectors on the disk. These sectors can be very useful for BIOS expansion, disk ID, data encryptation, or other systems-level functions. If they are used for BIOS expansion, the cold-start loading and sysgen procedures must be appropriately rewritten.

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CIRCLE 75 ON READER SERVICE CARD

The CP/M Bus

By Anthony Skellum

This column is planned as a CP/M forum. Readers are encouraged to send in questions about CP/M, which I will try to answer.

This month's "CP/M Bus" is devoted to the discussion of relocatable object code and its uses under the CP/M environment. The concept of relocatable code is defined, and specific types of relocatable code are discussed.

What is relocatable code?

Relocatable code is specially prepared object code (machine code) that contains additional information to make it suitable for relocation at various addresses within the address space of the 8080 or Z80. Thus, such code is independent, or at least quasi-independent, of an absolute assembly address. The code may also include symbolic information about variables defined at the source code level. Such symbolic information makes it feasible for a linkage editor (also called a linking loader) to create an absolute object code module by combining several relocatable modules prepared independently. The resulting absolute module is often linked in a way that makes it suitable for use as a transient program under CP/M.

Two distinct varieties of relocatable code will be discussed here. The first is page-relocatable code; the second, byte-relocatable object modules as supported by Microsoft-compatible compilers and assemblers. The latter is the standard relocatable format for CP/M and is also supported by Digital Research's compilers and relocatable macro assembler (RMAC). Each will be discussed in turn. However, before beginning these separate discussions, it is useful to introduce the concept of relative and absolute addressing, and how the microprocessor instruction architectures impact the need for relocatable code.

Relative and absolute addressing

The 8080/Z80 family of microprocessors support only absolute addressing for the majority of machine code operations. Absolute addressing is a machine language addressing mode where a specific memory location is referred to by an instruction. Thus, it follows that when only absolute addressing is available for most instructions, nontrivial programs can execute at only one fixed address (the assembly address).

On the other hand, relative addressing is an addressing mode in which the processor forms the ultimate absolute address by adding the relative address specified by the machine code to the value of the program counter (PC or IP). The newer 8086/88, Z8000, and 68000 processors support relative addressing to the degree that position-independent code may be created. Thus there is no need for page relocation techniques under these newer processors. Nevertheless, the concept of relocatable object libraries remains important, as we shall see below.

Page relocation

Page relocation is a code relocation technique that permits the relocation of code to memory page boundaries (XX00 hexadecimal). This is generally sufficient for most relocation applications, and is the simplest to implement. The relocator itself requires about 50 bytes of assembly code to implement and is generally a subroutine of the transient program.

This type of relocation is usually used to place a code segment below the CP/M BDOS. The transient program then consists of two parts: the first part, which executes at the start of the transient program area (generally 0100H); and the second part, a relocatable module that is moved below BDOS (CP/M's basic disk operating system) by the relocator. Once relocation is complete, control is transferred to the relocated code residing in high memory (below BDOS), which subsequently performs its functions.

This technique is used by debuggers (e.g. DDT), print spoolers (e.g. DESPOOL), CRT managers, and other programs that must supplement the operating system environment provided by the BDOS to transient programs. It is important to note that such relocated modules are responsible for adjusting the low-memory CP/M variables (specifically BASE+1 and ENTRY+1) if they are to have a continued presence while a regular transient program executes. Failure to make these adjustments would generally cause the relocated program to be overwritten by the next transient program to execute.

A more novel use for page relocation is to use it to provide code overlays in large programs. With the capability to use overlays, large programs can sometimes be segmented so that only a subset of the code is present in memory at a given time. When a certain section is needed, it is brought in off disk and relocated for a free area of memory. It may then be used as needed in that memory area and subsequently overwritten by another code segment (or data) when necessary. An example system where this concept could be used is in full-function word processors.

Implementing page relocation

The page relocation concept is effected through the use of a bit map. The bit map is a table of data in which a single bit corresponds to each byte of the program to be relocated. Thus, there is a 12.5% memory overhead associated with the use of the algorithm.

A bit in the bit map indicates whether or not the byte it

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corresponds to requires patching when the code is page relocated. The map is created by assembling the code in question at two page boundaries and then using a program to compare the two versions—thereby generating the correct bit map. The offset added by the relocator to bytes requiring relocation is:

(Destination Page #) − (Page # of copy we are relocating.)

If we use a copy assembled at page zero, then all relocation involves is addition of the destination page number to all bytes requiring relocation.

For programs exceeding approximately 512 bytes, the greater part of the memory overhead comes from the bit table and not from the relocation code itself. This attests to the fact that the relocation procedure is quite simple to effect.

This concludes our discussion of page relocation. Although the discussion of the method required is terse, the important parts of the algorithm have been discussed. Furthermore, the important applications of page relocation have been detailed. We now turn to a discussion of relocatable object modules and their benefits.

Relocatable object modules and libraries

In order to minimize the complexity of any given software project, software designers generally create modular software; that is, software consisting of relatively small modules, each given a specific function. Some of these modules will be specific to the project at hand, while others will be reusable in other software projects. Thus, it is useful to have the ability to file such modules into libraries where they may be accessed easily when a program is linked. Such libraries are called object libraries. Linking loaders are used to build executable programs by extracting copies of the appropriate modules from the user-specified libraries. The modules are said to be relocatable, since they ultimately will reside at arbitrary byte addresses within the executable programs that include them.

Thus we see that relocatable object libraries promote modular programming, which helps to save time and work since repetition of effort is reduced.

The general format of object libraries

Relocatable object libraries contain the following type of data about a given module (which is generally a subroutine):

- The other modules to which it refers
- The global variables to which it refers
- The global variables it makes available to other routines.
- The local storage it requires
- Miscellaneous data, includ-

CP/M Bus
continued . . .

• Miscellaneous data, including the size of the module.

Certain algorithms may contain more information about storage types. Also included serially with the code are specific instructions on how to resolve the requirements of the various machine code instructions with respect to addresses when forming the ultimate absolute code at link time.

For specific information on the Microsoft relocatable format, the reader should refer to the *Microsoft Utility Software Manual.*

Conclusion

We have discussed the concepts of page relocation and relocatable object modules. Future "CP/M Bus" colums will address the subject further if reader response suggests genuine interest in the elaboration of this topic.

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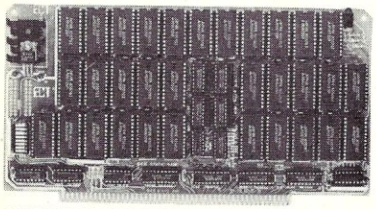

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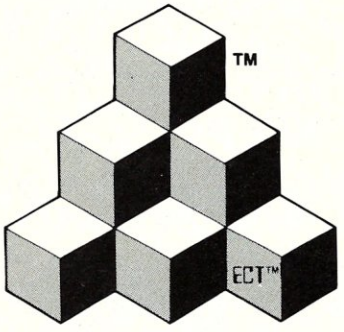

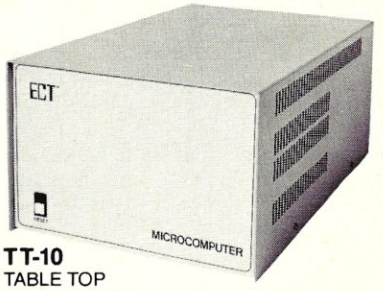

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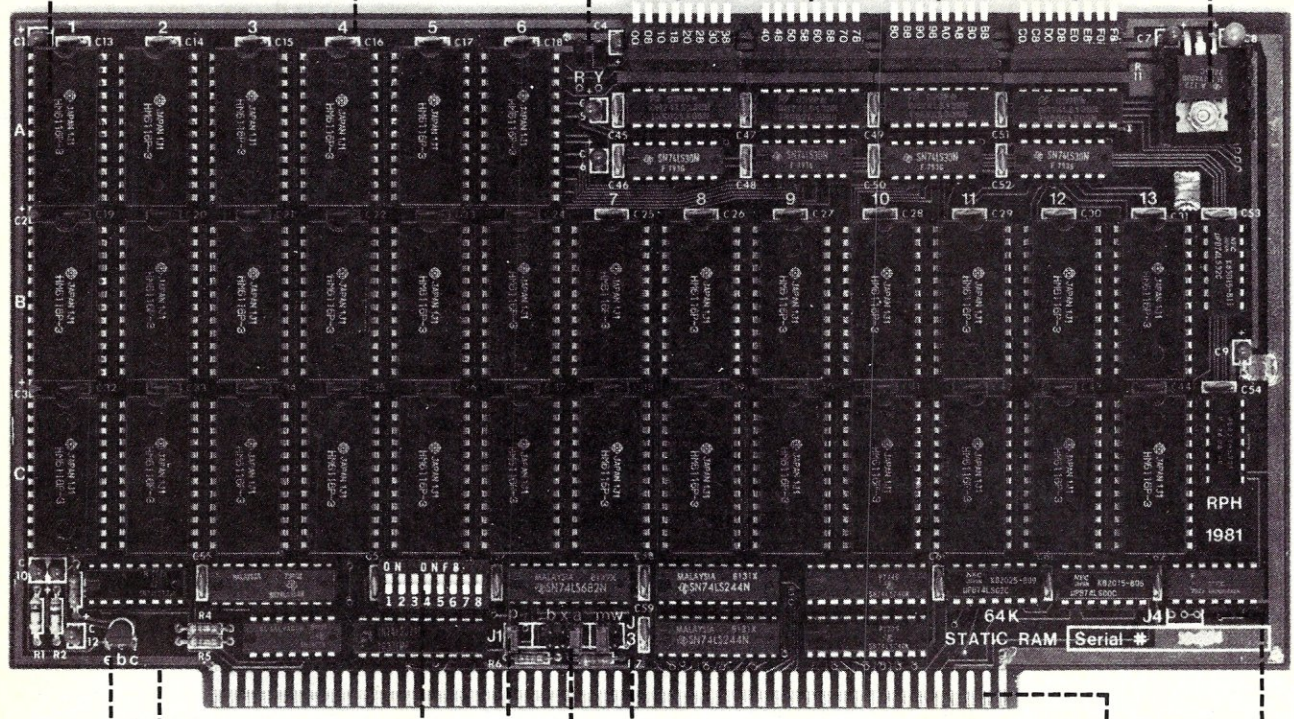

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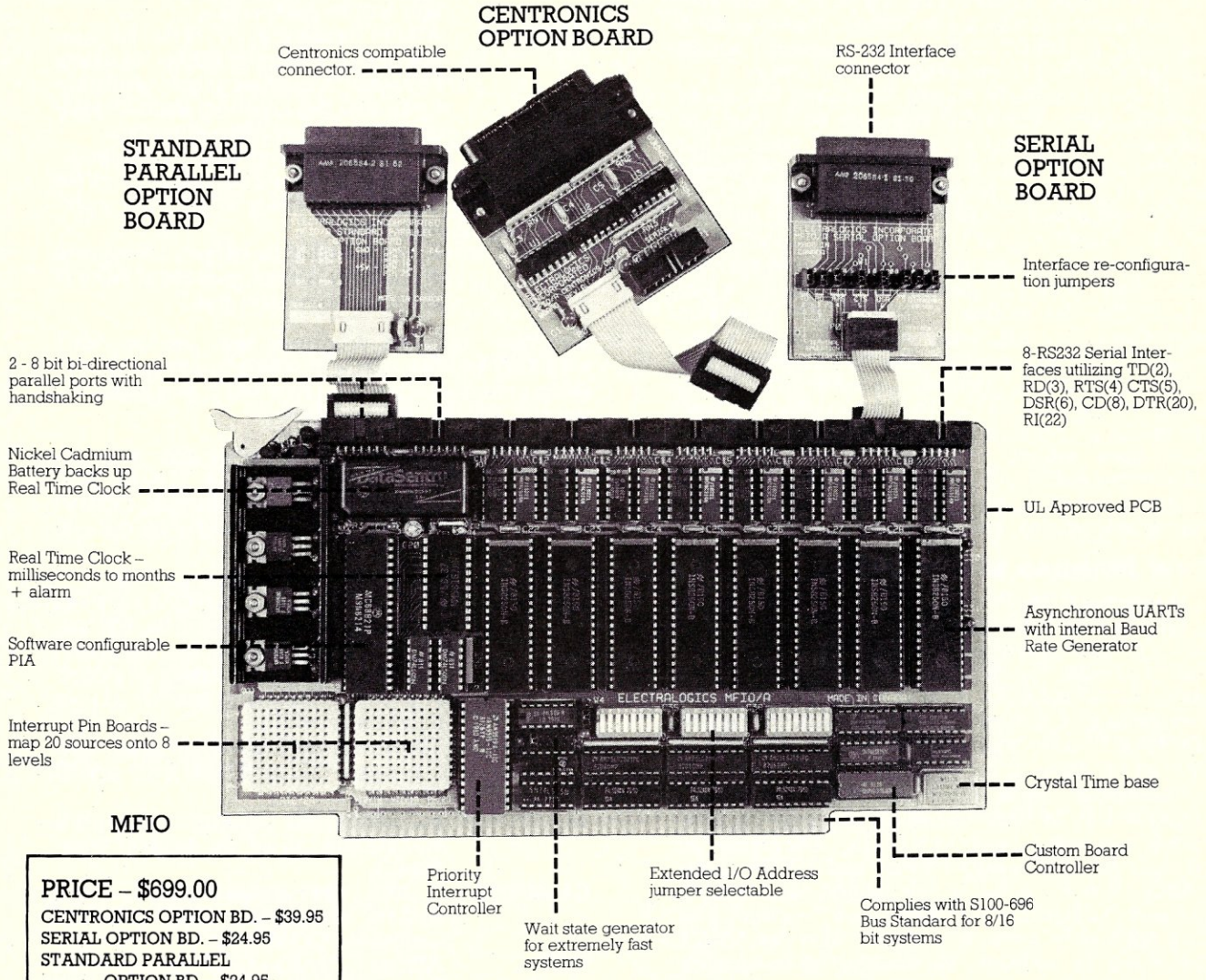

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CP/M Plus: An Overview for CP/M 2.2 Users

by David Hardy and Ken Jackson

Externally, CP/M Plus (alias CP/M version 3.0) is still very much like version 2.2. It still has the familiar "A>" and is still single-user. It still runs .COM files and has the same old commands like DIR, REN, TYPE, etc. It should take an average user about 5 minutes to become familiar with the simple operations at the command level. But that's really where the similarity ends.

CP/M Plus is radically different from its predecessors, and is at least a generation ahead. Directories are now hashed. LRU (Least Recently Used) buffering is now done by the BDOS. Drive capacity has been expanded to 512MB. Maximum file size is now 32MB. The 3.0 can be run with banked memory, which adds even more versatility, including extended line editing, password access similar to MP/M, and extended buffering.

Many things have stayed the same, but many have changed. The CCP can now be a transient program. The operating system now resides in a regular disk file, and is loaded by a simple loader kept in the system tracks of the boot drive. The SAVE command is now a transient program that relocates itself to the top of the TPA. A CP/M Plus system is now generated from a set of relocatable files with a generator program called GENCPM, in a manner similar to MP/M system generation. The BIOS has been broken down into a set of simplified modules that make modification easier and faster, although a modified 2.2 BIOS can also be used. I/O can be redirected with a simple utility program. Several new system programs have been added, including a comprehensive HELP command. All this, plus the BDOS is now finally smart enough to figure out when a disk has been changed and avoid trashing it.

New features of CP/M Plus

Documentation. Probably the nicest new feature of CP/M Plus is the documentation. It is now broken up into three well-designed manuals: the User's Guide, the System Guide, and the Programmer's Guide. All three manuals are complete enough to give the user a thorough understanding of CP/M Plus, including how to implement CP/M Plus on an existing 2.2 system.

Commands. Several new commands have been added to CP/M Plus, including new built-in commands and new transient programs. The DIRectory, ERAse, RENname, TYPE, and USER commands all remain, but a new command DIRSYS has been added to allow display of "system" files that previously were only visible with the STAT command. In addition, all the built-in commands (except USER) have been significantly enhanced to automatically load related transient programs when certain command line options are specified. The built-in commands are:

DIR	A greatly enhanced directory display utility. DIR has more than 16 command line options, including the ability to show file sizes, remaining space and entries, attributes, date, all drives or user areas, and more.
DIRSYS	Displays all "system" files in the current user area.
ERASE	Same as the 2.2 ERA command, except now allows optional confirmation before each erase.
RENAME	Allows renaming of files. Its new features include the ability to delete duplicate filenames (with confirmation), and the ability to include wildcards in the specified filenames.
TYPE	Same functions as before, except allows pagination and will prompt for a filename if none is given on command line.
USER	Same function as before, except will prompt for a user number if none is given on command line.

The new transient programs that are provided with CP/M Plus, many of which are valuable development tools not supplied with previous versions of CP/M, are as follows:

COPYSYS	A loader copy utility that replaces SYSGEN. Since the CP/M Plus system is kept in a disk file, COPYSYS puts only the loader on the system tracks.
DATE	Set or display the date and time.
DEVICE	Used to assign LOGICAL CP/M devices to one or more of the PHYSICAL CP/M devices. It also allows the user to change driver protocols and baud rates, and modify screen height and width.
DUMP	The same old DUMP program that displays a file in HEX and ASCII format.
ED	ED is now line oriented, although it still retains all of its original commands.
GENCOM	A utility that allows RSX (Resident System eXtenison) files to be attached to .COM files.
GET	Allows CP/M to GET console input from a disk file instead of from the keyboard.
HELP	A utility program that (along with a

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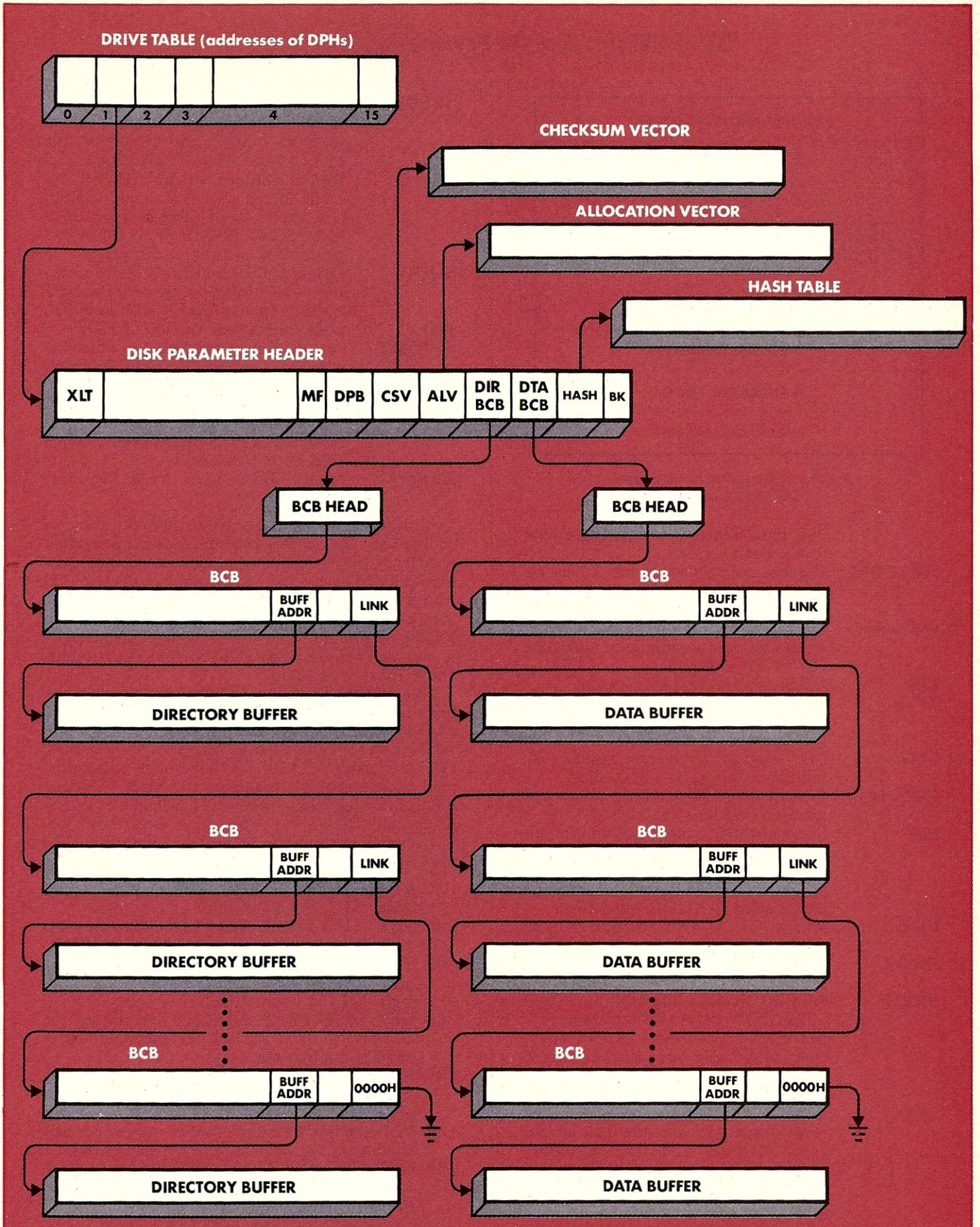

Figure 1. Banked system BIOS data structures from CP/M Plus Preliminary System Guide (by DRI)

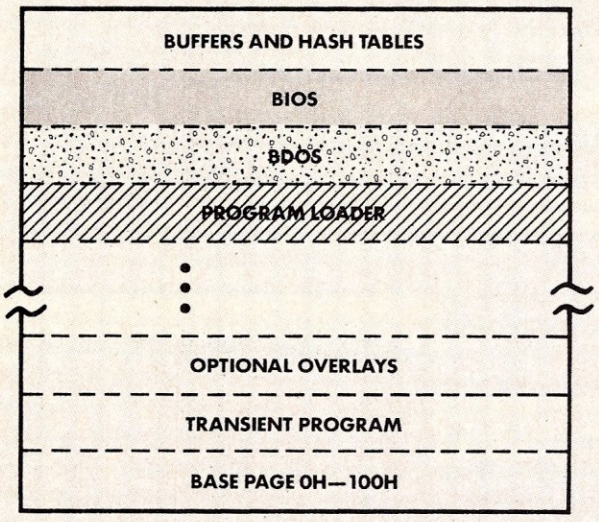

Figure 2. A typical nonbanked CP/M Plus system

76K data file) tells you in depth how to use each command.

HEXCOM Pronounced "LOAD" for 2.2 users, this program is used to convert .HEX files to .COM.

INITDIR Initializes a disk directory to allow time- and date-stamping in a banked CP/M Plus system.

LIB DRI's library utility program.

LINK The standard DRI linker, used to produce program files from .REL files created by RMAC.

MAC The Digital Research macro assembler. Generates .HEX files.

PATCH A system or file-patching utility for installing system "patches."

PIP Same old PIP, except this one can be used to put files in other user areas, and can ask for confirmation of each procedure in wildcard operations; also, has an ARCHIVE feature.

PUT Allows CP/M Plus to PUT printer or console output into a disk file.

RMAC The DRI Relocating Macro assembler. Generates .REL files.

SAVE A utility that installs itself at the top of the TPA, returns, then intercepts the NEXT program's exit to allow the TPA contents to be saved. (There is no SAVE command built into CP/M Plus!)

SET Allows file attributes to be SET or reset. Attributes include disk labels, type of time- and date-stamping, password protection, and the usual system and read-only attributes that STAT used to allow.

SETDEF Allows user to set various system options, including drive search chain, temporary drive, and filetype search order. Also controls DISPLAY and PAGE system modes: DISPLAY mode forces system to display names and locations of programs or .SUB files loaded; PAGE function allows pagination of console display.

SHOW Displays disk and drive characteristics. This utility, along with the SET utility, replaces the STAT command.

SID DRI's advanced version of DDT.

SUBMIT A much improved command file executer that includes NESTED submit ability and can contain program input lines. A special case of a .SUB file is the PROFIL.SUB file that is automatically SUBMITed on each cold-boot, if it exists.

XREF Digital Research's ASM file cross reference utility.

Two things you should have noticed about the preceding lists: CP/M Plus's commands are amazingly MP/M-like—in fact, many are downright identical. CP/M Plus comes with a lot of software that would cost a great deal of money if bought separately, notably: LIB, LINK, MAC, RMAC, SID, XREF. If you don't have these programs already, it may be cheaper to buy CP/M Plus than to purchase them separately!

New BDOS functions. BDOS functions 3 and 4 have been renamed from READER INPUT and PUNCH OUTPUT to AUXILIARY INPUT and AUXILIARY OUTPUT. Functions 7 and 8, GET and SET I/O BYTE, have been eliminated and their numbers assigned to AUX. INPUT STATUS and AUX. OUTPUT STATUS. Many of the old BDOS functions have been modified, but remain compatible, or nearly compatible. The *new* BDOS functions of CP/M Plus are:

37 RESET DRIVE—used to reset a particular drive. MP/M compatible.

44 SET MULTISECTOR COUNT—provides logical record blocking. MP/M compatible.

45 SET BDOS ERROR MODE—determines how physical and extended errors are handled. MP/M compatible.

46 GET DISK FREE SPACE—determines the number of free sectors on specified drive. MP/M compatible.

47 CHAIN TO PROGRAM—allows chaining from one program to another. MP/M compatible.

48 FLUSH BUFFERS—forces write of any write-pending records. MP/M compatible.

49 GET/SET SYSTEM CONTROL BLOCK—allows access to the CP/M Plus System Control Block.

The BDOS is now finally smart enough to figure out when a disk has been changed and avoid trashing it.

50 DIRECT BIOS CALLS—allows direct BIOS calls through the BDOS to the BIOS.
59 LOAD OVERLAY OR RESIDENT SYSTEM EXTENSION—loads an overlay module or RSX module into memory.
60 CALL RESIDENT SYSTEM EXTENSION—used to call RSXs.
98 FREE BLOCKS—returns to free space all temporarily allocated data blocks of all currently logged-in drives. Used by CCP after a warm start.
99 TRUNCATE FILE—sets the last record of a file to a specified random record number.
100 SET DIRECTORY LABEL—creates or updates a directory label. MP/M compatible.
101 RETURN DIRECTORY LABEL DATA—returns the label entry of the directory label for the specified drive. MP/M compatible.
102 READ FILE DATE STAMPS AND PASSWORD MODE—returns date- and time-stamp information and password mode for the specified file. MP/M compatible.
103 WRITE FILE XFCB—creates/updates an XFCB for specified file. MP/M compatible.
104 SET DATE AND TIME—sets the system internal date and time. MP/M compatible.
105 GET DATE AND TIME—gets the system internal date and time. MP/M compatible.
106 SET DEFAULT PASSWORD—allows a program to specify a file's password before that file is accessed, to avoid a password error. MP/M compatible.
107 RETURN SERIAL NUMBER—returns 6-byte CP/M Plus serial number
108 GET/SET PROGRAM RETURN CODE—allows a program to set or get a return code before returning.
109 GET/SET CONSOLE MODE—a 16-bit system parameter that determines the action of certain BDOS console I/O functions, such as Control-C function, scroll/no scroll, etc.
110 GET/SET OUTPUT DELIMITER—gets or sets current output delimiter, normally "$."
111 PRINT BLOCK—sends a character string located by the specified CCB (Character Control Block) to the logical console.
112 LIST BLOCK—sends a character string located by the specified CCB to the logical list device.
152 PARSE FILENAME—parse an ASCII filename and prepare an FCB (File Control Block).

In addition, many MP/M functions (38, 39, 41, 42, 43), although not supported, will return a proper ("successful") code.

New BIOS functions. The CP/M Plus BIOS jump vector was expanded from 17 to 33 jumps.

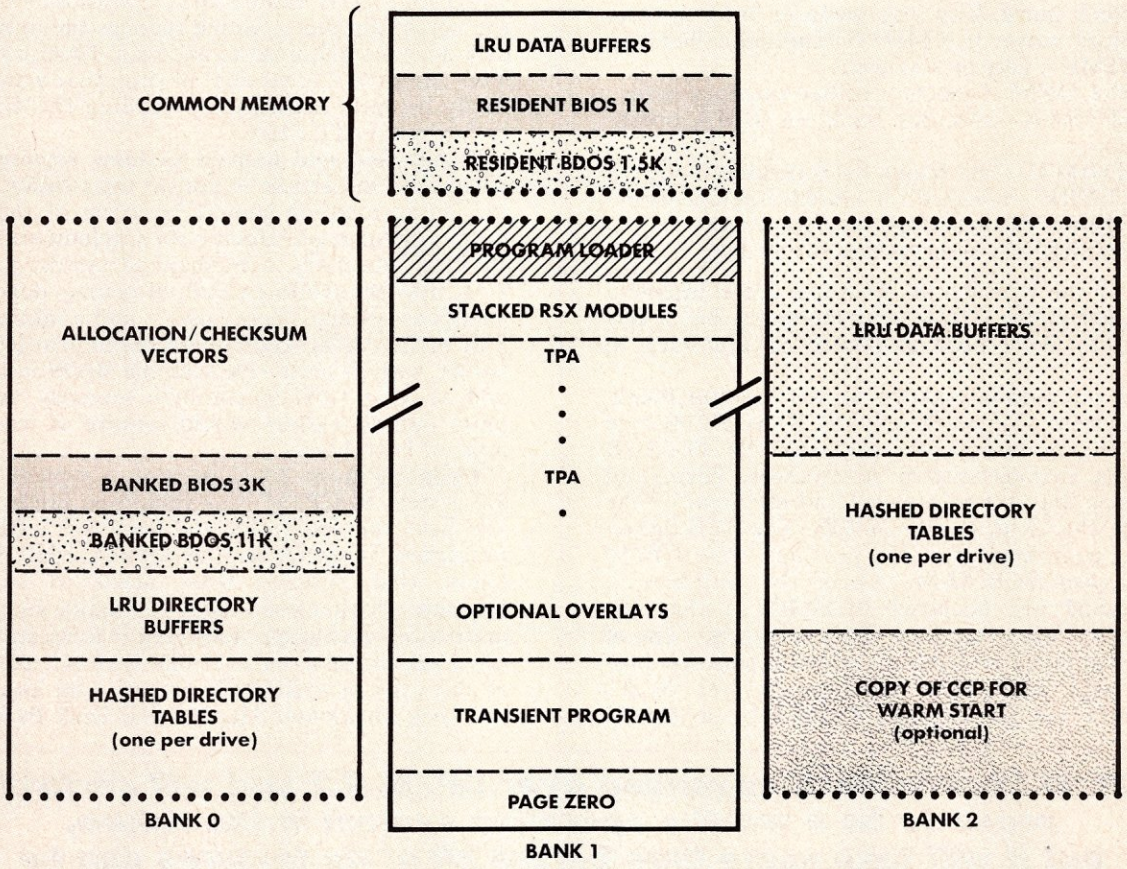

Figure 3. A typical banked CP/M Plus system

Not all of them have to be implemented to bring up a CP/M Plus system, but all 33 jumps must, of course, be included in the jump table. Usually, an unused jump can just point to a RET instruction. One of the jumps is reserved for OEM implementors (#30) and can be accessed via BDOS function 50; the last two jumps are reserved for future use. To operate a basic CP/M Plus system, only jumps 0-4, 8-14, 16, and 26 need be implemented.

BIOS functions 0-16 are basically the same as their 2.2 counterparts, except functions 6 and 7 (PUNCH, READER) have been replaced with AUXOUT and AUXIN, the auxiliary I/O routines. The new CP/M Plus BIOS functions are:

17 CONOST—returns output status of the Console.
18 AUXIST—returns input status of Auxiliary port.
19 AUXOST—returns output status of Auxiliary port.
20 DEVTBL—returns address of the Character I/O Table.
21 DEVINI—initializes Character I/O device.
22 DRVTBL—returns address of Disk Drive Table.
23 MULTIO—sets number of consecutive sectors to read or write.
24 FLUSH—forces physical buffer flushing for user-supported deblocking.
25 MOVE—performs a memory-to-memory block move. Can also perform bank-to-bank block moves if XMOVE function called.
26 TIME—gets or sets time.
27 SELMEM—selects specified memory bank.
28 SETBNK—specifies bank for DMA operation.
29 XMOVE—sets banks for following move.
30 USERF—reserved for system implementor.
31 RESERV1—reserved for future use.
32 RESERV2—reserved for future use.

Most of the new BIOS functions are completely explained in the CP/M Plus manuals, but a few small bits have been neglected or are hard to find.

I/O redirection and the system control block. The System Control Block (SCB) is a 100-byte long block of data located in the BDOS. The SCB contains various system parameters, flags, and variables that are referenced and modified by the BDOS, the CCP, and the BIOS. The SCB definition is contained in a file provided with CP/M Plus called SCB.ASM. All of the variables in SCB.ASM are declared PUBLIC so that the BIOS can reference them. This is certainly one of the advantages of using a system generation program and .REL files. Furthermore, the SCB's variables are all marked Read-Only or Read/Write with regard to whether or not they can be modified by the BIOS. The SCB.ASM file is contained in Listing 1.

Disk data structures. CP/M Plus is very similar to 2.2 in that it still uses Disk Parameter Headers (DPH), Disk Parameter Blocks (DPB), checksum and allocation vectors. However, in Plus, some new things have been added. Buffer Control Blocks (BCB) have been added to locate physical record buffers for the BDOS, and directory buffers have been added, too. As Figure 1 shows, the DPB has been expanded somewhat to accommodate many of these new structures, or their pointers. The new DPHs, although somewhat confusing and certainly more complex than their 2.2 ancestors, are responsible for much of Plus's increased speed. Notice, also, how the BCBs are linked together—the same BCB structure is used to locate both directory buffers and data buffers. If you think this takes up a lot of memory, you're right!

LRU buffering. In a banked system, CP/M Plus uses a Least Recently Used (LRU) buffering scheme to maintain a cache of deblocking buffers and directory records. When a buffer is needed by the BDOS, it will always select the least recently used one. LRU buffering doesn't directly increase execution speed or disk I/O, but can save valuable time reloading frequently used information.

Hash tables. CP/M Plus uses hash tables to increase its directory searching speed. By hashing, directory sectors can be located without searching the actual directory, which reduces the number of disk accesses required to access a directory entry. This can save a great deal of time that would normally be spent sequentially reading the directory to find a specific entry.

Nonbanked and banked systems requirements. Although this article is not an installation "how-to," some mention should be made of the minimum system requirements for implementing CP/M Plus. Basically, a nonbanked system requires 8.5K plus the BIOS (which, of course, depends of whatever system is being used), and a minimum of 32K RAM. A banked system requires at least two banks, with at least 11K plus the BIOS in bank 0, and at least 1.5K in common memory. A minimum banked system would require at least 96K total in both banks.

Updating from 2.2. Updating a typical CP/M 2.2 system to CP/M Plus should be fairly easy if you have the source for the CP/M 2.2 BIOS. A procedure is given in the CP/M Plus System Guide that explains what needs to be done. Chances are that you'll have to modify your BIOS quite a bit, including modifying it to assemble under a relocating assembler like RMAC, adding all of the (16) new BIOS functions, and expanding the Disk Parameter Header and Disk Parameter

CP/M Plus is much advanced over CP/M 2.2 and will certainly prove to be a worthy operating system in the future, but it will take some time before all of its features can be fully used in popular applications software.

CP/M Plus: An Overview continued . . .

Block data structures. Most of the existing BIOS functions (0-16) will have to be changed a bit, some a great deal. You'll also have to make a smaller version of your BIOS to link into the CP/M Plus loader program, but that is simple once you have the BIOS written. Naturally, nothing is ever as easy as it sounds, so count on spending many long hours debugging your CP/M Plus before it is working completely. If it's of any help, it is much easier to implement CP/M Plus than MP/M.

Conclusion

This article was written while evaluating a Beta-test version (1.2), so some of the items covered here may be different in the first release of CP/M Plus. The manuals were also preliminary, lacking both tables of contents and indexes, but were already complete enough to make the program completely understandable.

CP/M Plus is much advanced over CP/M 2.2, perhaps at the limit of 8-bit processor ability, and will certainly prove to be a worthy operating system in the future, but it will take some time before all of its features can be fully used in popular applications software. Most CP/M 2.2 applications software should run under CP/M Plus. Much systems software (like most of the popular debugging and disk utilities) may not. The biggest immediate advantage of CP/M Plus is probably its increased disk speed. In the long run, its biggest advantage will probably be its banked memory, I/O redirection, and extended BDOS functions.

```
        title 'System Control Block Definition for CP/M3 BIOS'

        public @civec, @covec, @aivec, @aovec, @lovec, @bnkbf
        public @crdma, @bflgs
        public @crdsk, @vinfo, @resel, @fx, @usrcd, @ermde
        public @date, @hour, @min, @sec, ?erjmp, @mxtpa


scb$base equ    0FE00H          ; Base of the SCB

@CIVEC  equ     scb$base+22h    ; Console Input Redirection
                                ; Vector (word, r/w)
@COVEC  equ     scb$base+24h    ; Console Output Redirection
                                ; Vector (word, r/w)
@AIVEC  equ     scb$base+26h    ; Auxiliary Input Redirection
                                ; Vector (word, r/w)
@AOVEC  equ     scb$base+28h    ; Auxiliary Output Redirection
                                ; Vector (word, r/w)
@LOVEC  equ     scb$base+2Ah    ; List Output Redirection
                                ; Vector (word, r/w)
@BNKBF  equ     scb$base+35h    ; Address of 128 Byte Buffer
                                ; for Banked BIOS (word, r/o)
@CRDMA  equ     scb$base+3Ch    ; Current DMA Address
                                ; (word, r/o)
@CRDSK  equ     scb$base+3Eh    ; Current Disk (byte, r/o)
@VINFO  equ     scb$base+3Fh    ; BDOS Variable "INFO"
                                ; (word, r/o)
@RESEL  equ     scb$base+41h    ; FCB Flag (byte, r/o)
@FX     equ     scb$base+43h    ; BDOS Function for Error
                                ; Messages (byte, r/o)
@USRCD  equ     scb$base+44h    ; Current User Code (byte, r/o)
@ERMDE  equ     scb$base+4Bh    ; BDOS Error Mode (byte, r/o)
@BFLGS  equ     scb$base+57h    ; BDOS Message Size Flag (byte,r/o)
@DATE   equ     scb$base+58h    ; Date in Days Since 1 Jan 78
                                ; (word, r/w)
@HOUR   equ     scb$base+5Ah    ; Hour in BCD (byte, r/w)
@MIN    equ     scb$base+5Bh    ; Minute in BCD (byte, r/w)
@SEC    equ     scb$base+5Ch    ; Second in BCD (byte, r/w)
?ERJMP  equ     scb$base+5Fh    ; BDOS Error Message Jump
                                ; (word, r/w)
@MXTPA  equ     scb$base+62h    ; Top of User TPA
                                ; (address at 6,7)(word, r/o)
        end
```


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CIRCLE 18 ON READER SERVICE CARD

Implementing the Advanced Features of CP/M Plus

by Bruce R. Ratoff

For the past few months I have had the opportunity to tinker with Digital Research's latest brainchild: CP/M Plus. This most recent step in the evolution of CP/M is expected to be released sometime this month. CP/M Plus offers many new features such as date and time stamping of files, file passwords, and a clever new command line editor. Perhaps even more striking than the visible system enhancements are the internal enhancements that have been made to improve file access speed and increase the memory space available to a running program. The price one must pay for many of these features is a more complex BIOS module. The changes and additions required are nontrivial, but are certainly a manageable task. For this extra effort, one is rewarded with a truly high-performance system. The purpose of this article will be to explain some of the BIOS functions that may be implemented to take advantage of the new features of CP/M Plus.

It is a certainty about computer software that when one adds features to a program, its memory requirements increase. CP/M Plus is no exception, particularly since many of the internal enhancements are accomplished through the use of extra tables and buffers to avoid unnecessary disk accesses. However, before you start moaning about how you've hardly got enough room in your version 2.2 CP/M system, let me tell you that it is possible to have a full-blown CP/M Plus system with a larger Transient Program Area (the place in memory where your programs run) than any prior version of CP/M! How is this apparent contradiction possible? Through a little trick called memory management.

What is memory management?

Memory management is a technique that has been employed on larger computers for years. Its power is based on the fact that the real limitation on the amount of memory most CPUs can handle is the number of unique *memory addresses* the processor can generate. Our 8080, 8085, and Z80 processors all have a 16-bit address bus, which allows for 65,536 possible unique memory addresses. This results in the well-known 64K maximum memory capacity.

But suppose you knew for sure that certain programs or parts of programs do not reference each other, and therefore do not need to be in memory at the same time. It then becomes possible to take several blocks of memory, locate them at the same range of addresses within the 64K address space, and use a few simple output instructions to turn each block of memory on or off as its contents are needed. This of course requires a small amount of additional hardware to perform the switching, but the additional hardware is already present on most popular S-100 memory boards. You may also see it referred to as "bank switching" or "extended addressing."

There are several limitations on the use of memory management in a system. For one thing, it usually is not possible to switch the entire 64K space in and out. The reason is simple: You can't switch out the part of memory where the bank switching routines themselves reside. If you did, the result would be something like trying to pull a rug out from under yourself, and your program would stand just about the same chance of remaining on its feet! You can't allow the memory management routine to disappear while it is being executed. For the sake of convenience, you would probably also like to take some of your input/output routines and other code that needs to access or be accessed by the switchable parts, and place it where it won't disappear when you perform your bank switching.

In CP/M Plus you define a boundary address called the "common base," and all nonswitchable code and data reside at addresses above this point. Note that the value of the common base depends on how the memory management hardware on your machine works. More specifically, it depends on what area of memory can be switched by your hardware. On my test system, I can switch memory at any 16K boundary, so I have chosen to set the common base at C000 hex, with four separate "banks" of memory that can be switched in the 48K region between 0000 and BFFF hex.

Banked memory and CP/M Plus

A full implementation of CP/M Plus requires at least three banks of memory. The first bank (Bank 0) is used to hold the banked portion of the BIOS and BDOS software, the disk allocation vectors, checksum vectors, directory buffers, and hash tables. Bank 1 is used as the Transient Program Area (TPA), where the Console Command Processor (CCP) and all your applications programs execute.

Note from Figure 1 that the leftover nonbanked memory between the common base and the start of the Resident BDOS is also part of the TPA. Since the resident BDOS is only 1.5K long, and only a small part of your BIOS needs to be resident, the TPA can be quite large. On my system, the Resident BIOS is 1.5K bytes long, leaving a TPA of 61K! The remaining banks are used primarily as disk data buffers. A 3K region in one of these banks should be set aside to hold a spare copy of the CCP, which will be copied into Bank 1 by the

Bruce R. Ratoff, 26 Broad St., Cranford, NJ 07016; (201) 272-1973

warm boot routine of your BIOS. By doing this, a warm boot will no longer perform any disk access. You therefore can change disks in drive A at any time, and no longer have to worry about which of your disks contain a valid system in the system tracks. Up to a total of 16 banks are supported, allowing you to have lots of data buffers! The usefulness of these will be clear as you read on.

As was mentioned above, the first bank of memory holds part of the BDOS and BIOS program modules. The BDOS is supplied by Digital Research in "System Program Relocatable" (SPR) form. Three files are provided: BDOS3.SPR is the full BDOS for use in a nonbanked system, while BNKBDOS3.SPR and RESBDOS3.SPR are the banked and nonbanked portions of the BDOS respectively. These modules are read by GENCPM, the CP/M Plus system generation utility, and become part of the generated system.

Banking the BIOS

Making your BIOS bankable is a matter of going through the code and identifying the sections that need access to all banks. Any part of the BIOS that accesses more than one bank should probably remain resident (nonbanked). This usually includes your bank selection routine and the portion of your disk read and write routines that actually perform the data transfer. You also probably should keep your console and printer routines resident, since they can be called from either the TPA (Bank 1) or the BDOS (Bank 0). These sections are marked as resident by preceding them with a CSEG command in the assembler source code. The various other disk-related routines such as Select Disk, Set Track, Set Sector, etc., and the setup and error recovery portions of your disk routines can all be placed in banked memory. This is indicated by preceding them with a DSEG command in the assembler source code. When the modified BIOS is assembled with RMAC (a relocating version of the MAC assembler) and linked with the LINK utility, the resulting BNKBIOS3.SPR file contains the banked and unbanked portions of your code, sorted out into two separate sections. GENCPM will recognize the two sections and divide up the BIOS accordingly.

In addition to specifying which sections of the BIOS must be banked, a few minor changes must be made to your code. The BDOS will always make its disk I/O BIOS calls with Bank 0 switched in. This is convenient, since you will be called with both halves of the BIOS already present. In the resident part of the disk read and write routines, you must add a call to your memory management routine to turn on the correct bank for the data transfer. After reading or writing the specified sector, you must turn Bank 0 back on before returning to the BDOS. The bank number to use for the disk read or write is obtained from a new BIOS routine called Set Bank, which simply passes you a bank number from 0 to 15. This number should be stored away along with the track and sector numbers and the DMA address, to be used when the actual disk read or write takes place. You will need to implement Select Memory, which

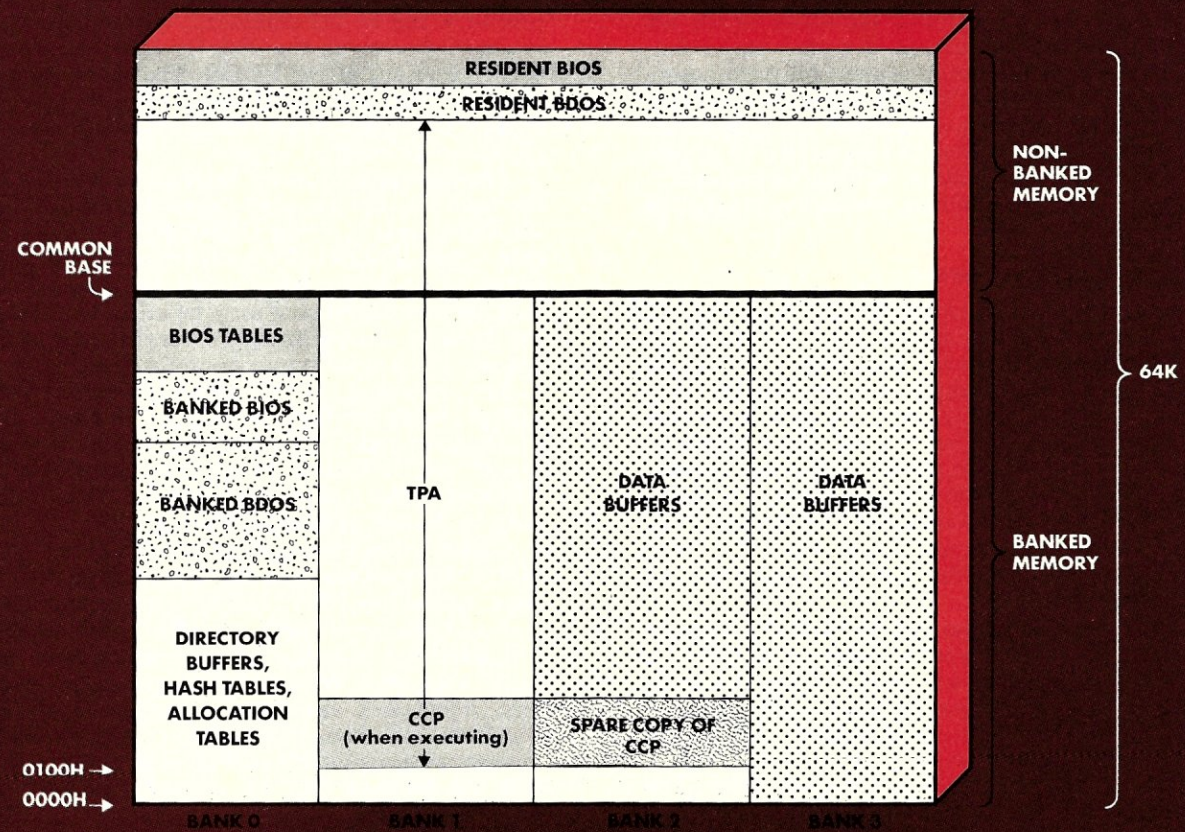


Figure 1. A typical four-bank CP/M Plus system model

is called with a bank number and must perform the hardware-dependent task of switching in the correct bank of memory. Finally, you will need to implement MOVE and XMOVE, which are routines to copy a block of memory within the current bank (MOVE) or between two banks (XMOVE). Z80 users have an edge here, since the Z80 block move instruction is a natural for these routines.

Benefits of the banked system

The first and most noticeable benefit of running a banked CP/M Plus system is that more memory is available for your programs. The bulk of the operating system now lives in a separate bank of memory, leaving you a larger TPA than you could ever have had under CP/M 2.2. The banked BDOS also contains some new features that make the system more convenient to use. There is now a CRT-oriented line editor built into the Read Console Buffer command, which is normally used when entering commands to the CCP, PIP, and other utilities. This editor lets you recall your last line of console input, and move the cursor around making insertions and deletions. By hitting the return key, you send the modified command line back to the system to be processed again. This saves a lot of typing when you have several similar commands to be entered, or when you discover a typing error at the beginning of a long line just before you hit the return key. You also get longer, more explicit error messages from the system, which show you the BDOS function number and the name of the file on which the error occurred. Another major feature of the banked BDOS is the ability to assign passwords to your files. This provides a way to protect the privacy of your work when you must share a system with others. You can set each disk to protect your files from deletion, writing, or both reading and writing by someone who doesn't have the correct password.

Tables and buffers

In addition to the added visible features described above, banked memory allows you take advantage of a number of internal improvements in the BDOS. Each of these improvements contributes to the very noticeable increase in speed of most disk operations. While all but one of these improvements are also available in the nonbanked system, the banked system allows you to make full use of them without eating up valuable TPA space. As an added convenience, you may elect to have GENCPM determine the size and location of all of these tables.

Two of the tables that can be banked should be familiar to anyone who has worked on a CP/M 2.2 BIOS. The checksum vector is a table that contains a 1-byte checksum for each sector of each disk's directory. During directory operations, CP/M uses these checksums to recognize that a different diskette has been put into the drive. The only change in CP/M Plus is that the checksum vectors may now be placed in Bank 0, recovering valuable TPA bytes.

The other familiar table is the allocation vector. This table is used to keep track of which blocks (groups) of disk space are used and which are free. In CP/M 2.2, and optionally in nonbanked CP/M Plus, one bit is used to keep track of each disk block. The bit is updated whenever a new block is written, and the entire table is rebuilt whenever a warm start or drive log-in occurs.

In banked CP/M Plus, two bits are used for each block. One bit indicates that the block has been used for a file which has not yet been closed, while the second bit says that the file associated with this block has been closed, making the allocation permanent. This double-bit scheme makes it possible to free up blocks that were allocated during the current program run if the drive is reset or the program exits without closing its files. The directory scan required in a 2.2 system to rebuild the allocation vector during each warm start is therefore no longer required. This shaves a substantial amount of time off the warm-start operation. In fact, with the CCP pulled in from an alternate bank rather than from the disk, warm starts are now virtually instantaneous.

Directory hashing is a completely new feature in CP/M Plus. You may elect in the GENCPM dialogue to enable hashing on some or all of your drives. This causes an extra table of four bytes for each directory entry to be allocated by GENCPM and built when a drive is logged in. This table is used by the BDOS to directly calculate the location of a file in the directory, without having to sequentially search the disk for it as was done in earlier versions of the BDOS. The speed improvement is dramatic, with most opens, closes, renames, and deletions now requiring that only a single sector be read or written.

The final improvement internal to the BDOS is the use of a sophisticated cache-buffering scheme for disk access. During GENCPM you may allocate a pool of buffers for each drive in your system. Separate pools are maintained for directory and data sectors. Each pool may be allocated to a single drive or shared among several drives at your option. Each pool may contain as many as 255 buffers, meaning that the total number of buffers will probably be limited only by the amount of available memory. Directory buffers go in Bank 0 (as shown in Figure 1) for easy access by the BDOS directory-handling functions. Data buffers may be placed in banks 2 through 15.

Cache buffers are used to avoid making unnecessary repeated reads to the same disk sectors. After a sector has been read or written once, it remains in memory. Another read of the same sector will fetch the in-memory copy rather than going back to the disk. When the system runs out of buffers, it releases the least recently used one. A BDOS call has been provided to release all buffers, so that programs such as PIP with the verify option can be sure they are actually performing a real disk access.

The effect of all this buffering on compilers, word processors, database packages and other pro-

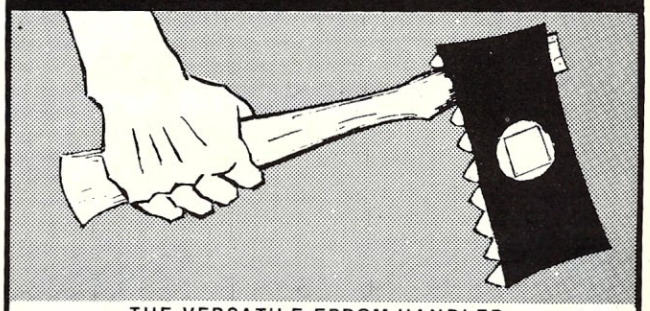
grams that repeatedly access the same data is quite interesting. Once one pass has been made through the file, the disk is no longer accessed unless a record is updated. Programs that use overlays run faster, since the overlay is often still in memory from its last use. Overall, cache buffering gives the impression that your programs are running in a much larger memory space. The degree of improvement, of course, depends on the amount of repetitious disk access the program does.

Conclusions

As you can see, there are a number of significant benefits to CP/M Plus, particularly when memory management can be implemented. One is quickly "spoiled" by the command line editor and the other new conveniences, as well as the impressive speed improvement. The disk speed enhancements are especially notable on a high-density floppy or hard disk system, where large directories have always suffered from sluggish access in prior versions of CP/M. Also, by banking the allocation vector and checksum vector, one no longer pays a TPA space penalty for large directories and small block sizes. This makes it possible to use the large disk drives much more efficiently. These improvements should be greeted enthusiastically by all.

Next month, in Part 2 of this series, I will examine some additional BIOS changes that can substantially improve the speed and usefulness of the CP/M Plus system.

UNIPROM



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Triple-Density Floppy Disks for CP/M

Optimizing sector size increases capacity

by Bob Weidemann

I may be stretching a track to make a point, but if you're still working in single density or have less than 500K on your one-sided double-density disks, then this article may help you stretch your computer budget. Six hundred sixty kilobytes of formatted storage (available to the CP/M user) on a single-sided diskette; 1.3 megabytes on a double-sided diskette; 2.6 megabytes on 2 drives; or 5 megabytes using four Tandon drives in the same size package most of us are using right now: That's what I mean by "triple" density.

Single-density 8-inch diskettes provide 241K of formatted space to a standard CP/M user. (There are actually many more bytes on the diskette, but they are used for "hardware" or system purposes—see later discussion.) So, when a claim regarding the number of bytes of storage is made, be sure the claim refers to end-user available bytes.

Double-density 8-inch diskettes provide 450 to 482K of storage. So a diskette that has 650–660K, by observation, could be called triple density.

Singles and doubles

For the purist, the terms double density and triple density are a misnomer, but for the operator the proof is in the number of bytes he can fill. The purist may want to dig out my article in the Jan/Feb 1981 *Microsystems*. There, I discussed how single-density diskettes store a data bit and a clock bit for every user-entered bit of data, whereas double-density encoding eliminates the clock bit and puts data in the space thereby released. Phase-locked loop data separators help keep data in sync when reading back, but obviously timing is more critical in double-density format, and obviously a good hardware data separator is the key. This means the density of the magnetic flux changes for a single-density encoded diskette is approximately the same as for a double-density diskette.

The basic reason you pay more for double-density diskettes is that the supplier must format them separately from the more common single-density diskettes; and since there are more types of double-density formats to stock, the price is passed on to the user. So, don't feel you have to buy high octane diskettes when regular will do. You can save money if you buy single-density diskettes and format them yourself. I particularly save because I punch a new hole in the single-sided disk to convert it to double-sided; the old hole must be covered, of course. I use Memorex diskettes with total satisfaction.

Bob Weidemann, 5 Bondsburry Lane, Melville, NY 11747

The big triple play

Now, for the "purist" again. "Triple density" still uses the same old diskette. But this time the sector sizes are changed. "Normal" CP/M operation requires the user to store data in logical blocks of 128 bytes. These blocks are stored on tracks on the diskette. When you write a program into your computer, your information is buffered in your main memory. When you direct your editor to save your program to your diskette, your program is moved one byte at a time to an "output-to-disk" buffer. When this buffer contains 128 bytes, it is loaded to a sector on your disk. This buffer must be the same size as a disk sector so that no time will be lost in looking for bytes. Similarly, there is an "input-from-disk" buffer that gets filled when you read from your diskette.

When CP/M was first introduced, memory costs were about $300 for 8K. Most of us had only 16 to 32K of on-board memory. With a 16K computer, 2 buffers of 128 bytes each (1 for reading, 1 for writing) used up a barely noticeable portion of total available memory (which was about 10K after subtracting CP/M's system requirement). This was relatively painless to main memory. However, by saving memory, we had to suffer with the small sector sizes on our diskettes.

The use of such small buffers meant that each track on our diskettes had to be divided into many small parts (26 altogether). Between each of these parts there are many bytes of "formatting" information. This information tells your controller the track number and the sector number of each part and provides for error detection (cyclical redundancy checks). Altogether, there are 56 bytes of formatting information for every 128 bytes of user-available storage. In addition, every track contains a "leader" (think of a tape leader) of 73 bytes and a "trailer" of approximately 247 "wasted" bytes. One track in single density holds 26 * 128 bytes or 3328 user-available bytes plus 1759 bytes inaccessible to the user. Do you see the logical conclusion?

Today memory is eight times cheaper, and most of us are running 56 to 64K. So, if you were willing to sacrifice 10K for the two buffers, you could format your disks with just one sector of 5000 bytes per single-density track. But even today, 10K is too big a sacrifice (note: with bank-select memory, 10K might become reasonable), so let's compromise. Instead of 128-byte sectors, let's use 512-byte sectors (or even 1024). This will require reasonably sized buffers and still reduce most of the overhead between sectors.

Now, all of this discussion was based on single density for illustrative purposes. Of course, we can

use larger single-density sectors. But it makes much more sense to use our larger sectors in the "double-density" format, and it makes much more sense to leave single density simple and compatible. Using 512-byte sectors in double density gives the end user 608K per disk, and using 1024-byte sectors can give 668K per disk (almost three times the single-density amount).

How do you get triple density?

Triple density requires the user to have a more sophisticated BIOS (Basic Input/Output System) for his CP/M. This new BIOS can be thought of like a funnel.

CP/M's BDOS (Basic Disk Operating System) still expects blocks of reads and writes to the disk to be 128 bytes long. If your diskette sectors are 512 bytes long, then you must hold them in a buffer and give them to BDOS in 128-byte chunks. As you feed the chunks to BDOS, you mark off the buffer area until BDOS has taken all four chunks. When BDOS requests another chunk, you read in 512 bytes to your buffer, but give BDOS only 128. Thus you actually read the disk once for every four BDOS requests. All this can be implemented using the blocking and deblocking schemes supplied by Digital Research with CP/M 2.x.

Fortunately, most manufacturers of disk controllers are supplying the implemented blocking and deblocking features in their BIOS, and so the end user can simply turn on and run.

Something for nothing?

As with everything in life, there are advantages and disadvantages to changing to a new system. Fortunately, the advantages of a triple-density system far outweigh any of the disadvantages. Let's look at them:

Advantages

1. Compatibility. IBM never defined a double-density diskette standard using 128-byte sectors. So, every disk controller manufacturer went his own way and, as a result, double-density diskettes are all but incompatible from manufacturer to manufacturer and often from user to user. But IBM did define 512-byte sectors. And, already, many controllers that use triple density record compatibly with others. (But *please*, let's not forget that *all* single-density diskettes are compatible and universal, and so compatibility in triple density is a convenience, not a necessity.)

2. Speed. In the typical microcomputer, processing time is usually reasonably fast (with the possible exception of number-crunching applications). However, I/O time usually causes annoying periods of operator idleness. My own experience is that when I am compiling even a medium-sized Pascal program, I can usually make a long trip to the refrigerator, guzzle down some unneeded calories, and still get back in time to wait while the computer finishes polishing my drive heads on my latest program. Fortunately, I may not be gaining as

Figure 1. Disc areas inaccessible to user (single density)

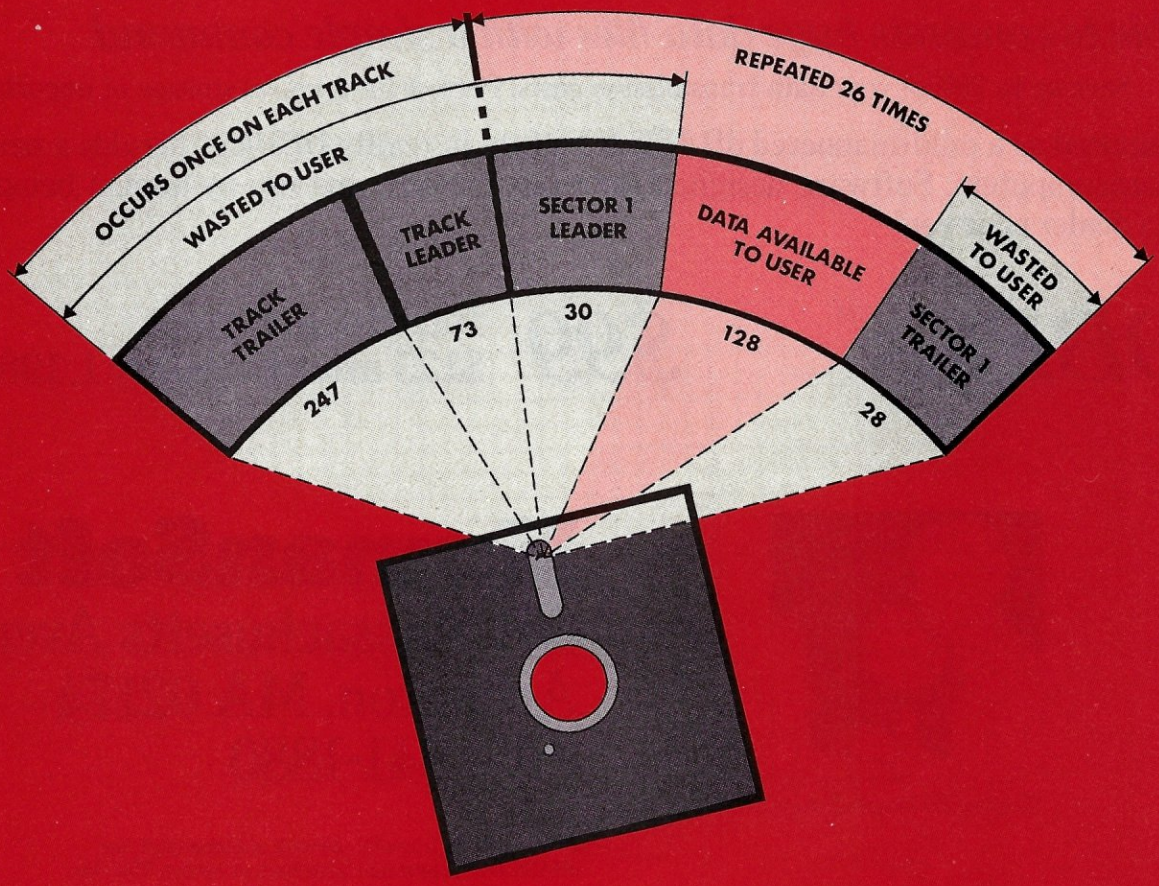

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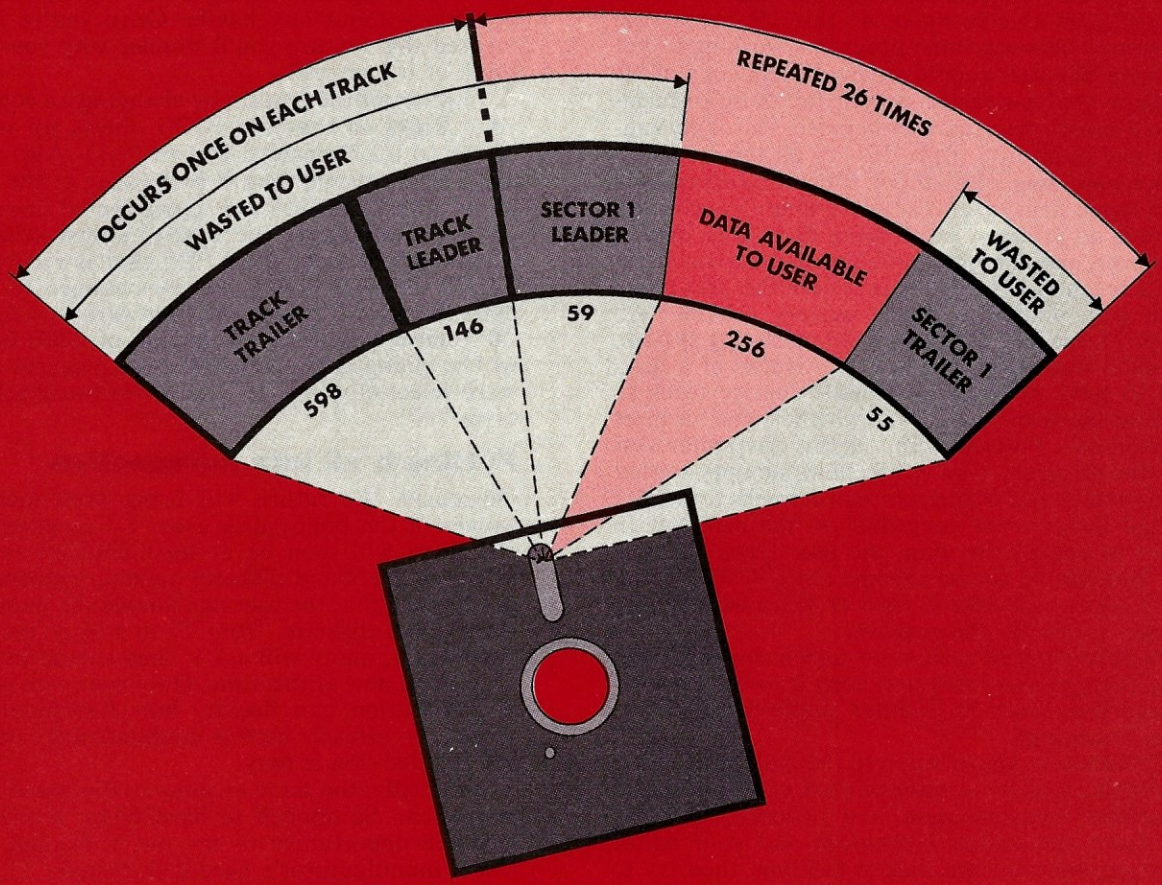
Figure 2. Disc areas inaccessible to user (double density)



much weight or wearing down as many disks now that I have implemented triple density on my system. A benchmark test program compiled in 35 seconds using 128-byte sectors; but the time was reduced to 22 seconds when using 512-byte sectors. These times represent a random program selection and not all programs will speed up this much; but then again, some programs may speed up even more.

The speed-up occurs because reading a small or a large sector takes virtually the same amount of time. Most of the lost time in reading from a disk is spent moving the head, letting it settle, and rotating the disk to the desired sector. Once all that is done, actual reading is relatively fast.

3. Increased storage. Very little discussion is needed here. Who doesn't want to get more available storage? Typically, most applications require certain programs to be on the system disk. Once they're on the disk, that overhead is taken care of. So increasing disk space by a factor of one-third may actually double a user's available data area.

The disadvantages

1. Price. I am including price, almost with tongue-in-cheek, because although most users will be able to implement triple density at no cost, some people will have to pay to get triple density. If your disk controller manufacturer supplies it with your controller, as do California Computer Systems, Morrow Designs, and CompuPro, you get it virtually free. Once you have the system you can format all the disks you want using the same single-density diskettes and drives you've been using. If you didn't get it free, contact your controller's manufacturer and ask if it's available. I had to write my own triple-density system for S&D's Versafloppy II, since S&D does not support CP/M. I am making it available at a very reasonable price to readers of *Microsystems*. Send an SASE to me for information.

2. Loss of memory. As already discussed, bigger sectors require bigger buffers. Allowing for input and output sector buffers of 512 bytes will cost the

You pay more for double-density disks because the supplier must format them separately . . . many formats must be stocked, and the cost is passed on to the user.

user 1K of memory. This usually means that he creates a CP/M system 1K smaller than he would normally be able to make. If this 1K means the difference between some programs working or not working, the user should simply keep a copy of his original double-density system for those once-in-a-blue-moon operations. Otherwise, I strongly suggest you jump into triple density all the way.

3. Conversing with others. Most disk controllers with triple density also support single density. So there is no problem exchanging disks with others. However, one annoying problem came up on a system I recently used. On this system the user could have only double or triple density on the "A" drive. This is because the CP/M operating system, which is located on the first two tracks of a disk, had to have at least one double-density track to contain the oversized BIOS (which is true for most controllers). Furthermore, on this particular system the directory map was kept in memory so that reads and writes would not require seeks to track 2 to find locations of programs on the diskette. In order to update the map, the user types "control C". But this of course reboots the CP/M system. So, it was impossible to read or write with single-density media on the A drive.

With a two-disk system, to copy a single-density disk, the operator must first copy it to triple density and then back to another single-density disk. Very annoying!

Fortunately, the solution to this problem is really simple. And it's a solution that can help others in similar circumstances. For instance, let's say you have just edited a program and your editor tells you your current disk is full; you then try to write the program to your second drive; if that also is full, you will lose all of the work you've done. But suppose you had already fooled the CP/M BDOS and told it you had four drives. Now, you can tell it to write the program to the "C" or "D" drive. Of course, you only have two drives but each of the two drives can be called "A" or "C", and "B" or "D". This scheme can be implemented on any system to enable the user to have ultimate flexibility in disk transfers.

Now you can place a single-density disk in the "A" drive and type "C:". CP/M will think it is operating to a third drive so no "control C" is needed, but your hardware will turn on the "A" drive. Once again, copying from single to single is possible without any hassle. Once you've implemented this feature you'll wonder why you didn't think of it yourself!

Implement the feature by changing an equate in your BIOS so that the BIOS allows up to four drives (0,1,2,3) instead of two (0,1). Also in the disk select routine (find it by looking at the BIOS jump table), "AND" the user-selected drive with 0FDH to eliminate the next-to-lowest order bit. Thus a selection of drive "D" that is recorded in CP/M as 0000 0011b will be changed to 0000-0001, which will cause the hardware to select the "B" drive. Likewise, a selection of 0000 00010b will be changed to 0000 0000, which causes a software select of drive "C" and a hardware select of drive "A".

Putting it all into perspective

Obviously, the future will bring even more advances in the floppy disk area. 1.3 megabytes on one drive will soon be at least doubled as drive manufacturers and diskette makers improve their products so that the user can double the number of tracks on a diskette, from 77 to 154 or more. So once again, many will ask if they should invest in something new at this time. Only your own personal application can decide, but, fortunately, for those who already have a double-density controller, the decision is easy.

Naturally, the same techniques discussed in this article can be applied to hard disks. Recently, I had the opportunity to try out a famous West Coast manufacturer's hard disk system. This system uses a Shugart 14-inch drive that contains 28 megabytes of unformatted storage. It also uses 128-byte sectors.

User-available area is slightly over 20 megabytes. Speed is faster than my 512-byte sectored floppies, but not by that much. Imagine what that system would be like with large sectors.

Well, until I see a hard disk whizzing away at a substantially higher speed than I can get with my two Qume double-sided floppies, at a price in line with what I've spent already, I'm not about to tap my own reservoir again. Triple density, I think you've saved my marriage.

Figure 3

Here is how you can alter your BIOS to allow for four logical drives when you only have two physical drives in your system.

```
seldsk: ; Select disk
        ;
        ; Entry: C = desired drive
        ;
        ld   a,c          ;****** add line to convert c to a, d to b
        and  a,0fdh       ;****** add line so reg c is altered also
        ld   c,a
        ld   hl,0000h     ;****** maxdrives should be equated to 4 earlier
        cp   a,maxdrives  ;if bad (diskno) then exit
        ret  nc           ; save requested disk
        ld   (reqdrv),a   ; A := currently selected drive
        ld   a,(curdrv)
```

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CIRCLE 152 ON READER SERVICE CARD

A CP/M CHAIN Routine

A simple assembly language subroutine useful for menu-type applications

by Robert S. Minnis

One of the real advantages of Basic is the ability to chain from one program to the next. This feature allows one program to cause another to be loaded into memory and to begin execution. Three principal benefits derive from this capability. First, programs larger than available memory may be developed. Second, programs may be broken into smaller, more manageable segments, perhaps each encompassing a logical function. Third, menu-driven applications may be developed more easily.

Few other languages implemented on micro computers provide this capability. Those which do usually provide it in the form of an overlay facility that requires a complex and usually expensive linking loader and overlay supervisor.

The routine provided here is a rather simple subroutine that can be called from a program written in assembly language or most high-level languages. In particular, the parameter-passing conventions conform to that of Microsoft Fortran. These parameters are the name of the program to be executed (NAME) and a string that contains whatever would normally be entered on the command line following the program name (PARM).

Parameter NAME is a string containing a program name in the standard CP/M convention, including the optional disk specification and file type. Normally the type is .COM, but the file must be of this type, regardless of the name. For example, B:NXTPGM.COM. Any leading blanks are ignored. NAME must be terminated with a blank, backslash (?), or a binary zero. If the disk specification is omitted, the program is loaded from the currently selected drive.

Parameter PARM is the command line parameter to be passed to the chained program. This string must be terminated with a backslash. If there is no leading blank on PARM, which would always occur on a command line entry, one is inserted unless PARM is null (consists of a backslash only).

The following is a sample FORTRAN call:

```
CALL CHAIN ('A:ED.COM\',
           'B:NEWFIL.DAT\')
```

Program execution

When CHAIN is called, the routine first attempts to open the file for the program to be executed. If the open fails (or the file name is invalid), the routine returns to the calling program. This is the only circumstance in which a return may occur. Next, the PARM string is moved to the default buffer and the length is placed in the first byte of the buffer. Lower-case characters are converted to upper case. The default FCB is also set up, including the second file name in the disk map part of the FCB, if appropriate. Since the CP/M documentation is unclear as to the results, if the command line does not contain one or two valid file names (for example, when using PIP), there is no assurance of compatibility in this case.

Finally, the routine that actually performs the load is relocated to the top page (256 bytes) of memory just below the BDOS. This page of memory may have been used by the current program (unless of course CHAIN itself happens to be there) but must not be required by the program being loaded. However, once loaded, the program may use this page. If the load routine is about to be overlaid, the routine performs a warm start. (A possible modification would be to display a message at this point first.)

Just before jumping to 100H to execute the loaded program, the warm start address is pushed on the stack so that if the chained program saves the stack and attempts a return, a warm start will occur.

Routine internals

CHAIN is written in Z80 assembly language to take advantage of the relative jump instructions. The only really tricky part of CHAIN is writing the load routine so that it can be easily relocated. Those more familiar with that task might produce a neater method than the one used in this routine, but it does work.

CHAIN is written using two MACROs that may be replaced with inline code if necessary.

Routine FILFCB, which formats an FCB, is an adaptation of a routine by S. J. Singer from the CP/M user's group library.

Following the Microsoft conventions, the address of NAME must be located in the HL registers, and the address of PARM must be in the DE registers.

Notes on usage

It is important to close any output files before calling CHAIN, or the files will not be complete. It should also be noted that there is no way to pass data to the chained program in memory (COMMON in Basic). This feature could probably be incorporated for assembly programs, but this would not be compatible with high-level languages such as Fortran.

Sample usage

There are several possible useful applications that could be developed with the help of CHAIN. One use might be the implementation of a fully menu-driven CP/M system. The main program, say MENU, could read the directory and display the

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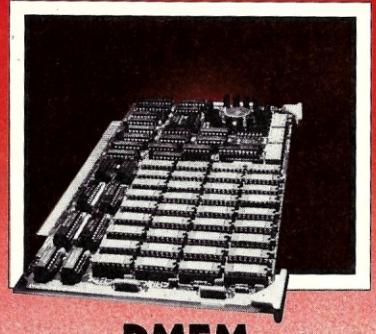

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CIRCLE 51 ON READER SERVICE CARD

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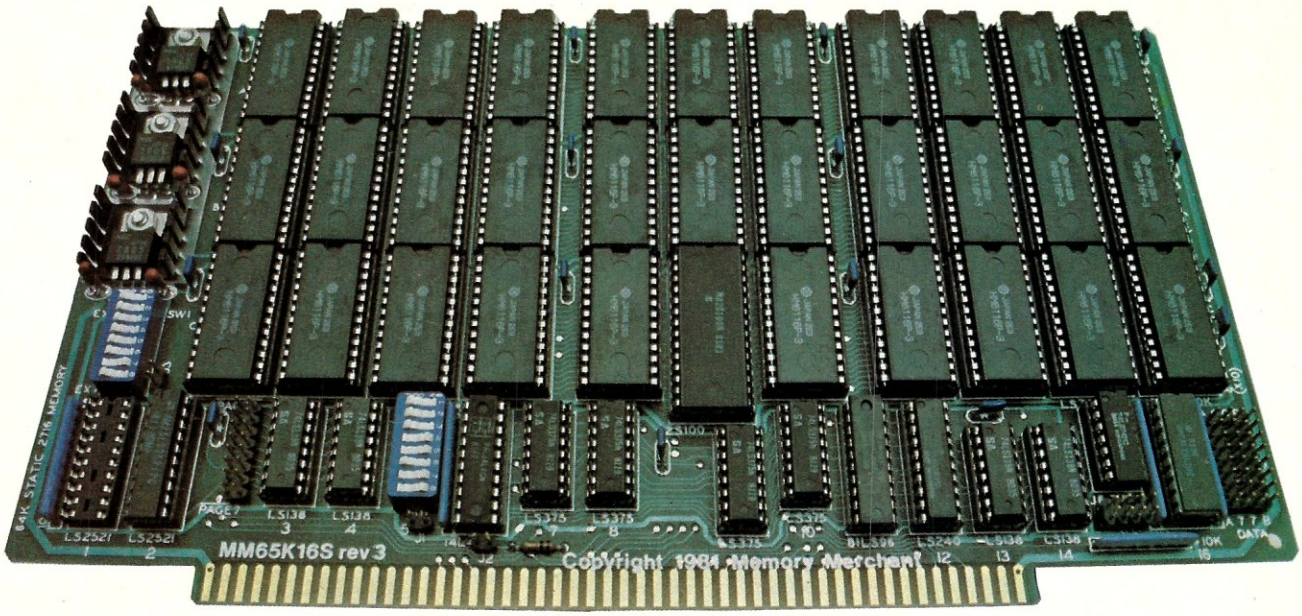

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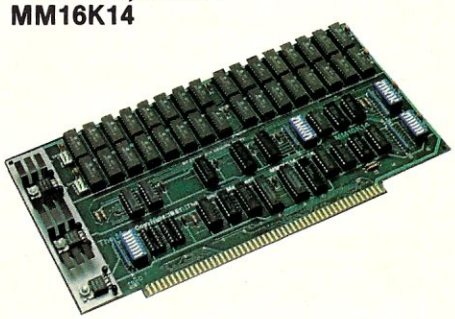

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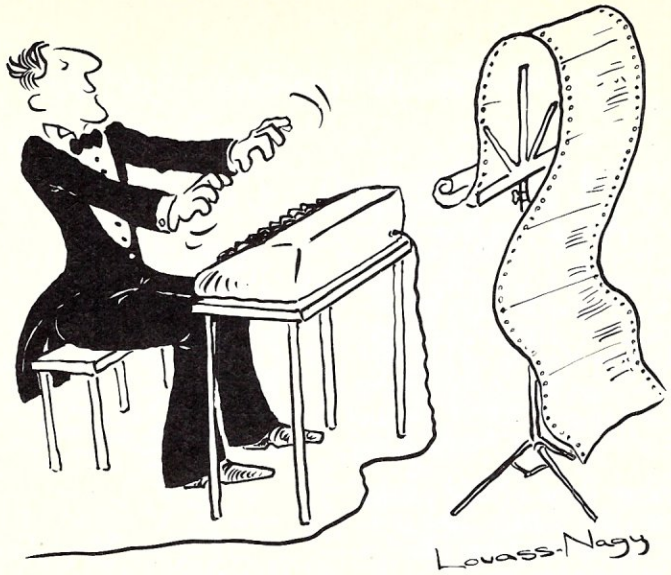
programs available on the disk or disks. Help files could be prepared for each of these programs. The user could then call the desired program from the menu or request help in setting up the parameters or in the use of the program. For any called programs written to also use CHAIN, the MENU program could be recalled at termination. If the CP/M autoload feature (*Microsystems* 1982: Vol. 3, No. 1) is implemented, even programs that do not use CHAIN (such as ED, PIP, STAT) would terminate with a warm start, which would cause MENU to be reloaded.

The reader can probably think of many dedicated applications (statistical package, file maintenance system, accounting package) that could be implemented in a similar manner.

Robert S. Minnis is currently Technical Support Coordinator at North Texas State University in Denton, Texas.

```
;CALL CHAIN('D:NAME.EXT','PARMS')

        TITLE   CHAIN   -   LINK TO NEXT PROGRAM

        ENTRY   CHAIN

        EXT     FILFCB

WBOOT   EQU     0               ;WARM BOOT
CPM     EQU     5               ;CPM ENTRY
ENTRY   EQU     0100H           ;CHAINED PROGRAM ENTRY
TFCB    EQU     05CH            ;FIRST FCB
TFCB2   EQU     TFCB+16         ;DISK MAP PART OF FCB
TBUFF   EQU     080H            ;DEFAULT BUFFER
EOP     EQU     '\'             ;END OF PARMS MARKER

SETDMA  MACRO                   ;SET DMA FOR READ
        POP     HL
        PUSH    HL
        PUSH    HL              ;SAVE AGAIN
        LD      E,(HL)
        INC     HL
        LD      D,(HL)
        LD      HL,128          ;ADD A RECORD
        ADD     HL,DE           ; RECORD
        EX      DE,HL           ;IN <D,E>
        POP     HL
        LD      (HL),E
        INC     HL
        LD      (HL),D          ;RESAVE
        LD      C,26            ;SET DMA
        CALL    CPM

        ENDM                    ;END OF SETDMA

READ    MACRO                   ;READ A SECTOR
        POP     DE
        PUSH    DE
        INC     DE
        INC     DE
        INC     DE              ;TO FCB
        LD      C,20            ;READ
        CALL    CPM

        ENDM                    ;END OF READ

CHAIN:  PUSH    DE              ;SAVE PARM

        EX      DE,HL           ;FILL FCB FOR CHAINED PGM READ
        LD      HL,FCB          ;NAME TO <DE>
                                ;POINT TO FCB
        XOR     A               ;CLEAR FLAG
        LD      (FLAG),A        ; FLAG
        LD      BC,FLAG         ;POINT TO FLAG
        CALL    FILFCB          ;FILL IT IN
        LD      A,(FLAG)        ;GET FLAG
        OR      A               ;GOOD?
        JP      NZ,RAD1         ;NO-EXIT

        LD      C,15            ;OPEN FILE
        LD      DE,FCB          ;OPEN
        CALL    CPM             ; FILE
        INC     A
        JP      Z,RAD1          ;ERROR IF NOT FOUND

        POP     DE              ;COPY PARMS TO TBUFF
        LD      B,0             ;RESTORE PARM ADDR
        LD      HL,TBUFF+1      ;ZERO COUNT
        LD      A,(DE)          ;POINT TO TBUFF DATA
        CP      EOP             ;GET FIRST
        JR      Z,PCOPY4        ;ANY?
        CP      ' '             ;NO-SKIP
        JR      Z,PCOPY1        ;BLANK?
        LD      (HL),' '        ;YES-SKIP
                                ;FORCE A BLANK
```



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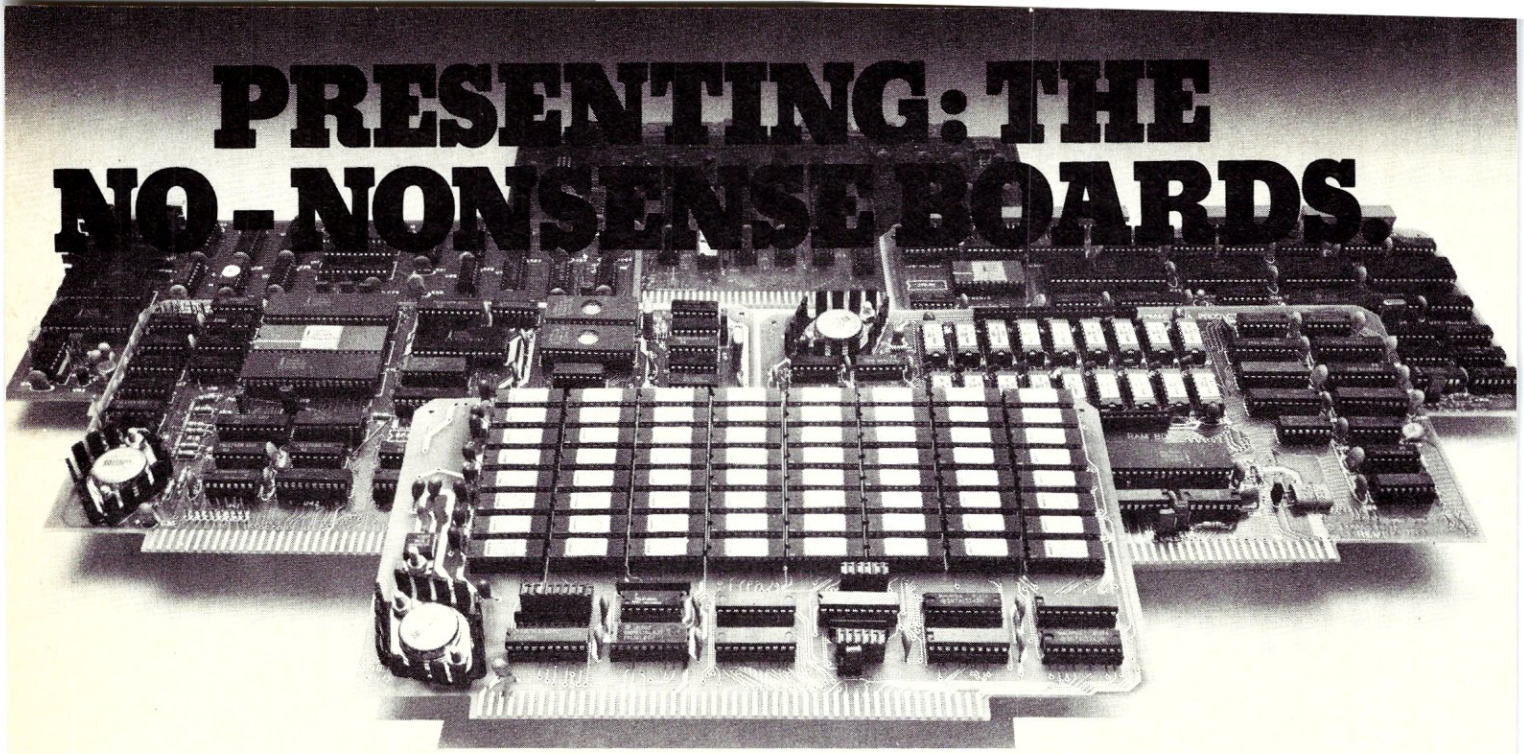
```
        INC     HL              ;NEXT TBUFF
        INC     B               ;COUNT BLANK
PCOPY1:
        INC     B               ;COUNT
        JP      M,PCOPY3        ;QUIT IF >128
        LD      A,(DE)          ;GET PARM
        CP      EOP             ;END OF PARM?
        JR      Z,PCOPY3        ;YES-FINISHED
        CP      'a'             ;LESS THAN 'a'?
        JP      M,PCOPY2        ;YES
        CP      'z'+1           ;GREATER THAN 'z'?
        JP      P,PCOPY2        ;YES
        AND     ODFH            ;MAKE UPPER
PCOPY2:
        LD      (HL),A          ;SAVE PARM
        INC     HL
        INC     DE
        JR      PCOPY1          ;DO NEXT
PCOPY3:
        DEC     B               ;BACK ONE
PCOPY4:
        LD      (HL),A          ;SAVE END ALSO
        LD      A,B
        LD      (TBUFF),A       ;SET LENGTH

                                ;SET UP DEFAULT FCB

        LD      HL,TFCB         ;DEFAULT FCB
        LD      DE,TBUFF+2      ;NOW IN BUFFER
        OR      A               ;ANY?
        JR      NZ,DFCB1        ;YES
        LD      DE,DUMYBF       ;USE DUMMY PARMS
DFCB1:
        XOR     A               ;CLEAR
        LD      (FLAG),A        ; FLAG
        LD      BC,FLAG         ;POINT TO FLAG
        CALL    FILFCB          ;FILL IT
        LD      A,(FLAG)        ;GET RETURN
        OR      A               ;GOOD?
        JR      NZ,DFCB4        ;NO - FILL WITH DUMMY
        LD      A,1             ;SET FLAG
        LD      (FLAG),A        ; FOR NEXT FILE
        LD      BC,FLAG
                                ;CONTINUE <DE> WHERE LEFT OFF
        LD      HL,TFCB2        ;DISK MAP PART
        CALL    FILFCB          ;FILL IT
        LD      A,(FLAG)        ;GET RETURN
        OR      A               ;GOOD?
        JR      NZ,DFCB4        ;NO-FILL WITH DUMMY
        JR      DFCB9           ;CONTINUE

                                ;BAD FILE NAME-FILL WITH DUMMY
DFCB4:
        LD      HL,TFCB         ;START OF FCB
        LD      DE,DUMYBF       ;DUMMY PARMS
        XOR     A               ;CLEAR
        LD      (FLAG),A        ; FLAG
        LD      BC,FLAG
        CALL    FILFCB
DFCB9:

;RELOCATE PROGRAM

        LD      HL,(6)          ;END OF AVAIL MEMORY
        LD      L,0             ;BACK UP TO START OF PAGE
        DEC     H               ;BACK UP ONE PAGE
        PUSH    HL              ;SAVE 'TO'
        LD      DE,RELBEG       ;START OF RELOCATE
        LD      BC,RELEND-RELBEG        ;BYTES TO RELOCATE
RELOOP:
        LD      A,(DE)          ;GET CHAR
        INC     DE
        LD      (HL),A          ;STORE IT
        INC     HL
        DEC     BC              ;COUNT DOWN BYTES
        LD      A,C
        OR      A
        JR      NZ,RELOOP       ;MORE
        LD      A,B
        OR      A
        JR      NZ,RELOOP       ;MORE
        POP     HL              ;GET BACK BEGINNING
        LD      A,H             ;SET 'TO' PAGE NO
        JP      (HL)            ;ENTER RELOCATED RTN

BAD1:                           ;BAD EXIT
        POP     DE
        RET

FLAG:   DB      0               ;FILFCB FLAG
DUMYBF: DB      EOP             ;DUMMY PARM

        PAGE
;ACTUAL CHAIN RTN
;  <H,L> POINTS HERE

RELBEG  EQU     $
        JR      START           ;SKIP DATA STORAGE
MP:     DW      128             ;100H/2
RP:     DB      0               ;CHAIN RTN'S PAGE
FCB:    DB      0,'             ',0,0,0,0,'             ',0
START:
                                ;NEW STACK
        PUSH    HL              ;COPY <HL>
        POP     DE              ; TO <DE>
        LD      H,A             ;OUR
        LD      L,0             ; PAGE
```

PRESENTING: THE NO-NONSENSE BOARDS.



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CIRCLE 23 ON READER SERVICE CARD

```
        INC     H               ; +1
        LD      SP,HL           ;NEW STACK
        EX      DE,HL           ;RESTORE <HL>

        INC     HL              ;PAST
        INC     HL              ; JUMP REL
        PUSH    HL              ;SAVE START OF STORAGE
        INC     HL
        INC     HL
        LD      (HL),A          ;OUR PAGE
NEXT:
        SETDMA
        READ                    ;READ HALF PAGE
        OR      A
        JR      NZ,FINISH
        SETDMA
        READ                    ;READ REST OF PAGE
        OR      A
        JR      NZ,FINISH
        POP     HL
        PUSH    HL
        INC     HL
        LD      A,(HL)          ;NEXT
        LD      B,A             ; PAGE
        INC     B               ;ADJUST FOR NEXT READ
        INC     HL
        LD      A,(HL)          ;OUR PAGE
        CP      B
        JP      Z,WBOOT         ;ABOUT TO OVERLAY
        JR      NEXT            ;READ NEXT PAGE
FINISH:
        LD      DE,TBUFF        ;DEFAULT BUFFER
        LD      C,26            ;DEFINE TO CPM
        CALL    CPM
        LD      HL,(1)          ;WARM START ADDR
        PUSH    HL              ;IN CASE OF RET
        JP      ENTRY           ;EXECUTE NEW PGM

RELEND  EQU     $

        END


TITLE   FILFCB - SUBROUTINE TO FILL IN AN FCB


;       CALL FILFCB (FCB,'D:NAME.TYP',FLAG)

;       FCB  = 33 BYTE AREA (SEE FLAG FOR EXCEPTION)
;       FLAG = 0 TO FILL FULL FCB
;              1 TO ONLY FILL DISK & FILE NAME PART

;       (<DE> WILL POINT TO LAST CHAR OF NAME PARM
;        PROCESSED ON GOOD RETURN, UNLESS TYPE IS
;        EXACTLY 3 CHARS, THEN POINTS ONE PAST LAST)

        ENTRY   FILFCB

FILFCB:
        PUSH    BC              ;SAVE FLAG ADDR
        INC     DE              ;POSSIBLE :
        LD      A,(DE)          ;GET IT
        CP      ':'             ;IS IT?
        DEC     DE              ;RESTORE
        LD      A,0             ;SAY NO DISK
        JR      NZ,FILF0A       ;NO
        LD      A,(DE)          ;GET DISK
        AND     0FH             ;MASK OFF HIGH BITS
        INC     DE              ;PAST DISK
        INC     DE              ;PAST :
FILF0A:
        LD      (HL),A          ;SAVE DISK
        INC     HL              ;TO NAME PART
        PUSH    HL              ;FCB ADDR
        LD      C,11            ;NAME FIELD SIZE
        LD      A,' '
FILF1:
        LD      (HL),A          ;BLANK IT
        INC     HL              ;TO NEXT
        DEC     C               ;COUNT DOWN
        JR      NZ,FILF1        ;DO MORE
        POP     HL              ;BACK TO START
        PUSH    HL              ;AND RESAVE
        LD      C,9             ;MAX NAME LENGTH (INC .)
FILF2:
        LD      A,(DE)          ;NAME CHAR
        CP      ' '             ;LEADING BLANK?
        JR      NZ,FILF3        ;NO
        INC     DE              ;SKIP BLANKS
        JR      FILF2
FILF3:
        LD      A,(DE)          ;GET NEXT CHAR
        CP      0               ;BIN 0 END OF FIELD?
        JR      Z,FILF0C        ;YES
        CP      ' '             ;OR BLANK?
        JR      Z,FILF0C        ;YES
        CP      '\'             ;OR BACKSLASH?
        JR      Z,FILF0C        ;YES
        CP      '.'             ;PERIOD SEPARATOR?
        JR      Z,FILF4         ;YES-DO TYPE
        CALL    CHECK           ;CHECK NAME CHAR
        JR      C,FILF0E        ;BAD NAME CHAR
        LD      (HL),A          ;SET CHAR
        INC     HL
        INC     DE
        DEC     C               ;COUNT DOWN
        JR      Z,FILF0E        ;ERROR EXIT
        JR      FILF3           ;CONTINUE
FILF4:
        INC     DE              ;SKIP PERIOD
```

```
        DEC     C               ;COUNT OFF PERIOD
        JR      Z,FILF6         ;FINISHED WITH NAME
FILF5:
        INC     HL              ;MOVE TO
        DEC     C               ; TYPE
        JR      NZ,FILF5        ; FIELD
FILF6:
        LD      C,3             ;LENGTH OF TYPE
FILF7:
        LD      A,(DE)          ;GET CHAR
        CP      0               ;BIN 0 END OF FIELD?
        JR      Z,FILFOC        ;YES
        CP      ' '             ;OR BLANK?
        JR      Z,FILFOC        ;YES
        CP      '\'             ;OR BACKSLASH?
        JR      Z,FILFOC        ;YES
        CALL    CHECK           ;CHECK NAME CHAR
        JR      C,FILFOE        ;BAD NAME CHAR
        LD      (HL),A          ;SAVE CHAR
        INC     HL
        INC     DE
        DEC     C               ;COUNT DOWN
        JR      NZ,FILF7        ;DO NEXT
FILFOC:
        POP     HL              ;BACK TO START OF NAME
        POP     BC              ;FLAG ADDR
        PUSH    BC              ;RESAVE
        LD      A,(BC)          ;GET FLAG
        OR      A               ;FULL FCB?
        LD      A,0             ;PRESET FOR GOOD RET
        JR      NZ,FILFOF       ;NO-FINISHED
        PUSH    DE              ;SAVE NAME PTR
        LD      DE,11           ;POINT TO
        ADD     HL,DE           ; EXTENT ETC.
        POP     DE              ;RESTORE NAME PTR
        LD      C,21            ;LENGTH OF REST
FILFOD:
        LD      (HL),0          ;ZERO
        INC     HL
        DEC     C               ;COUNT DOWN
        JR      NZ,FILFOD
        XOR     A               ;CLEAR FOR GOOD RET
        JR      FILFOF          ;DO GOOD RET
FILFOE:
        LD      A,1             ;SET ERROR
        POP     HL              ;FIX STACK
FILFOF:
        POP     HL              ;GET BACK FLAG ADDR
        LD      (HL),A          ;GOOD RETURN
        RET
```

```
CHECK:                          ;CHECK FOR VALID FILE NAME CHAR
        CP      ':'             ;LESS THAN :?
        JP      M,OK1           ;YES-OK SO FAR
        CP      '>'+1           ;GREATER THAN >?
        JP      P,OK1           ;YES-OK
        JR      BAD             ;BAD IN THIS RANGE
OK1:
        CP      '.'             ;PERIOD?
        JR      Z,BAD
        CP      ','             ;COMMA?
        JR      Z,BAD
        CP      '*'
        JR      Z,BAD
        CP      '['
        JR      Z,BAD
        CP      ']'
        JR      Z,BAD
        CP      'a'             ;LESS THAN 'a'?
        JP      M,OK2           ;YES
        CP      'z'+1           ;GREATER THAN 'z'?
        JP      P,OK2           ;YES
        AND     0DFH            ;MAKE UPPER CASE
OK2:
        LD      B,A             ;SAVE CHAR
        XOR     A               ;CLEAR CARRY
        LD      A,B             ;RESTORE CHAR
        RET
BAD:
        SCF                     ;SET CARRY
        RET

        END
```

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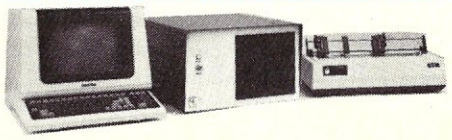

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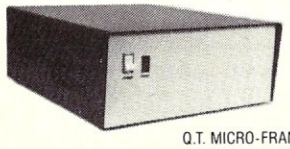

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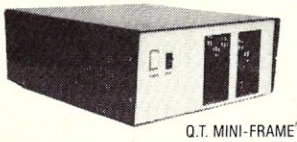

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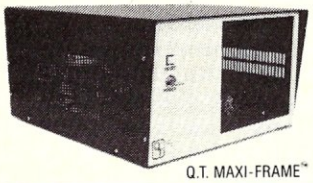

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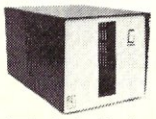
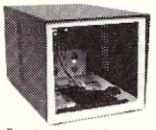
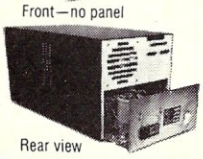


Front—Tandon Panel



Front—no panel



Rear view

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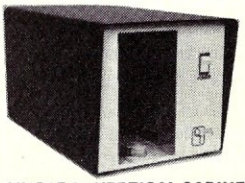

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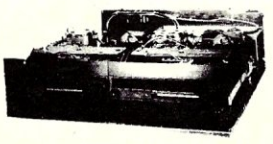

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CIRCLE 30 ON READER SERVICE CARD

S-100 Microcomputer Troubleshooting

by Ron Derynck

As long as his system is working properly, the average computer owner does not give much thought to what he would do if a hardware problem developed. If he owns a prepackaged system such as a TRS-80, he can send it in for repair. However, the owner of an S-100 system may not always have that option, either because he has purchased boards from a number of different manufacturers, or because he has built his own interface boards. In either case, the owner may have no choice but to start troubleshooting the computer himself.

Does this mean you have to go out and get an advanced degree in electronics and then buy tens of thousands of dollars' worth of digital test equipment so you are prepared for a computer failure? If my experiences are any indication, the answer is definitely *no!* It is, however, difficult to provide exact proceedures for troubleshooting, since techniques vary greatly from problem to problem. This article summarizes a number of troubleshooting techniques I have found valuable. To illustrate better how these techniques are used, an actual problem that I had with my computer will be explained and the method used to isolate it documented.

The problem first showed up when I added a parallel interface to my computer. At first I assumed that the problem was in the new circuitry. As it turned out, the problem was caused by my Polymorphic Video Terminal Interface (VTI) and some subtle differences between the way that the Z80 and 8080 chips handle I/O instructions. If you have a Z80 and have noticed some intermittent problems, this article may help explain them. If you have a VTI, you will very likely want to make the modifications suggested. Even if you don't have equipment similar to mine, this article will assist you if you ever have to troubleshoot a defective computer.

System description

One of the keys to successful troubleshooting is a good mental picture of the various boards in your computer system, their operation and interrelationships. One way to obtain this knowledge is to maintain an up-to-date block diagram of your hardware configuration, showing the functions of each board and any memory and I/O addresses used. Figure 1 shows the organization of my homebrew Z80 system. In order to understand the rest of this article, it is necessary that you become familar with the configuration of my system.

It is centered around two S.D. Sales cards, a Z80 CPU, and 16K of dynamic memory addressed from 0000H to 3FFFH. An additional 4K block of static memory is located at E000H to EFFFH. The Polymorphic VTI acts as the principal operator interface device. It has 1K of video RAM addressed at FC00H to FFFFH. It also has a keyboard input port that is addressed at FCH to FFH. Although only one I/O address is required to handle a keyboard, the VTI decodes only six of the eight I/O address bits, and thus the keyboard occupies four I/O addresses.

The final board in the system is a home brew System Monitor Board (SMB) that has 2K of EPROM located at C000H to C7FFH. These EPROMs contain a monitor program that provides the system with its basic operations program and I/O routines. The SMB uses a UART to provide the system with a serial I/O port addressed at C1H. This port can be connected to either a hardcopy terminal or a cassette deck via an external switch and Kansas City Standard cassette interface. Status of the serial port is read from port C0H. My plans for the SMB also included a parallel I/O port to be addressed at C2H. It was while testing the input half of the parallel port that a very strange problem showed up.

Adding a parallel input port

Like the rest of the SMB, the parallel input port was to be built on a Solid State Music IO-2 breadboard card. This board is laid out to use an 8212 IC as an input latch. Figure 2a shows the circuit of the input port as I implemented it. Note that my design is slightly different from the example presented in the IO-2 manual. I routed the output of the 8212 to a separate buffer instead of connecting it directly to the Data Input lines of the S-100 bus so that I could maintain compatibility with other circuits already operational on the SMB.

Eight data lines from the peripheral device are wired to the inputs of the 8212. Another signal called "LATCH" strobes the data into the 8212 when it goes high. At the same time, this signal sets pin 23 low. This pin can be used either as an interrupt or as a status indicating that data has been loaded into the latch. In Figure 2, pin 23 is used as a status signal by feeding it thru a three-state buffer and then tying it to bit 6 of the DATA IN bus. The buffer is enabled by the PC0* signal, which is active when the status port C0H is addressed. Thus the status of the parallel input port is determined by testing bit 6 of port C0H.

The DEVSEL* signal enables the outputs of the 8212 when the CPU reads from port C2. This signal is also inverted and sent to the peripheral as a "read next character" command. Pin 2 is tied low to place the 8212 in the input mode.

My reason for adding the parallel input to the computer was to allow a high-speed paper tape reader to be interfaced to the system. Rather than building the circuit and hooking the tape reader up

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to it to see if it all worked together, I decided to proceed a step at a time and so designed the test circuit (shown in Figure 2b) to verify that the new circuit itself worked properly.

Test program

When working on a computer, it is frequently helpful and often necessary to use software troubleshooting aids to complement hardware test procedures. Listing 1 is an example of this technique. A short program waits for data to be strobed into the input port and then displays it, in binary, on the system console. It is designed to be used with the test circuit of Figure 2, and allows the data printed out to be compared easily with the settings of the test switches.

Example 1 shows the results of running the test program. After starting the program, I turned on the first switch and pressed the ENTER DATA button. *Eureka* . . . it worked! I flipped up the next switch, pressed the ENTER DATA button, and 11000000 was printed. Feeling confident now, I started turning on more switches, hitting ENTER DATA and verifing that the correct binary word was printed. Everything was working perfectly until I set the switches to 11111100, then, as shown in Example 1, the program started to print out the answer over and over again without the ENTER DATA button being activated!

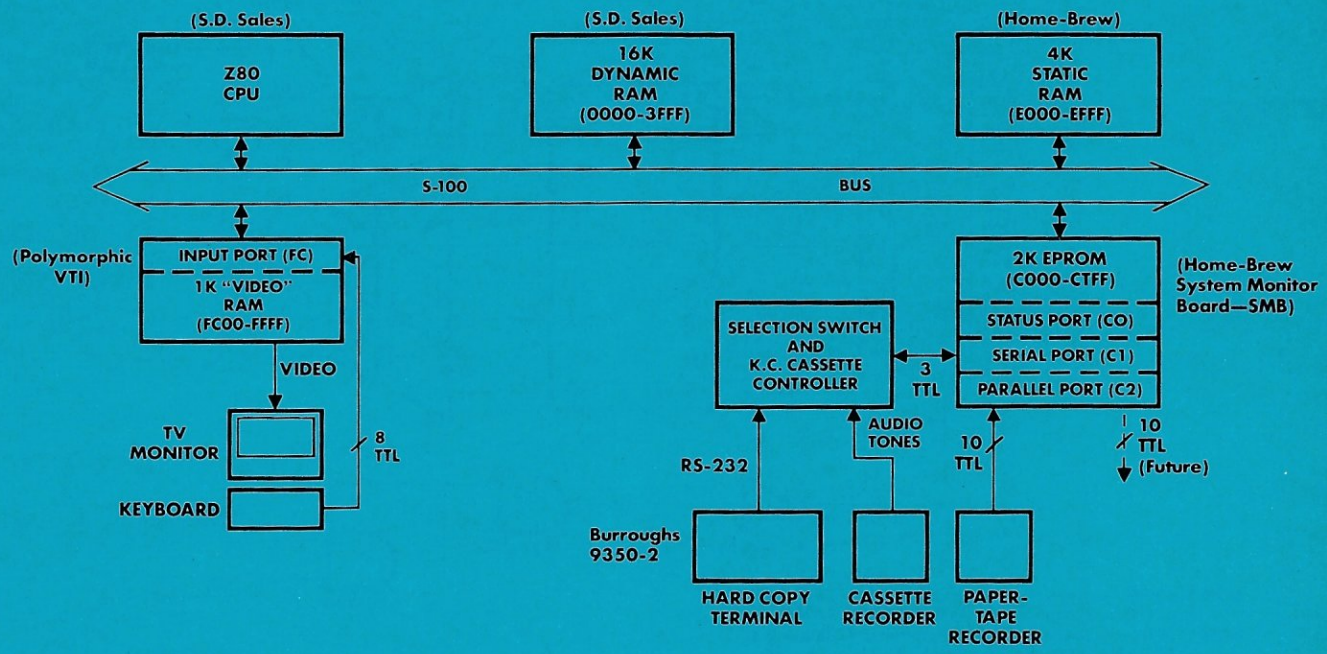
How could this be? The input port itself must be working because each of the eight bits could be read in separately. Hmmm, maybe the program has bombed. No, that couldn't be it, because it can

```
? X                          (X COMMANDS MONITOR TO START A PROGRAM)
EXECUTE PROG                 (MONITOR RESPONDS AND ....)
START  Ø1ØØ                  (REQUESTS A STARTING ADDRESS)
→
 1ØØØØØØØ                    (TEST PROGRAM IS NOW RUNNING)
→
 11ØØØØØØ
→
 111ØØØØØ
→
 1111ØØØØ
→
 11111ØØØ
→
 111111ØØ
 111111ØØ
 111111ØØ
 111111ØØ
 111111ØØ
```

Example 1. *Test run of program in Listing 1. Status of parallel input port at C2H is scanned until a latch pulse is received; switch positions are read in and then printed in binary. Arrows indicate when enter data switch is activated.*

be restarted and works great until that particular pattern is set up on the switches. Well, maybe the program has a bug in it, but if it does I sure can't see it. Could the strobe signal be oscillating? No, because it doesn't make sense that this would occur only for certain switch patterns. What the (expletive deleted) can be wrong then?

As I sat back, not really knowing what to do next, my subconscious mind came up with the idea that the bit patterns causing problems (these included 11111101, 11111110, and 11111111, besides 11111100) just happened to correspond to



NOTE 1: The VTI input port uses addresses FC, FD, FE, and FFH.

NOTE 2: The system monitor board is enabled for I/O addresses C0-C7H, but only C0, C1, and C2H are active.

Figure 1. Block diagram of author's Z80 computer system

the address of the keyboard port on the Polymorphic VTI in my system. You will recall that it occupies input port addresses FCH thru FFH. This idea really didn't make a lot of sense, because the VTI had been operational for over a year and, besides, there is no way that it should be able to interact with an input port addressed at C2H. Still, this was the only lead I had to work on.

Putting the scope to work

In order to use a conventional scope to troubleshoot a computer (instead of a much more expensive logic analyzer), it is necessary that there be some unique, repetitive signal that can be used to trigger the oscilloscope. Often a simple program loop will provide a repetitive trigger. In this case, it is not necessary to write another test program, because the problem itself is causing the program in Listing 1 to loop even though it is not supposed to. Murphy doesn't always cover his tracks!

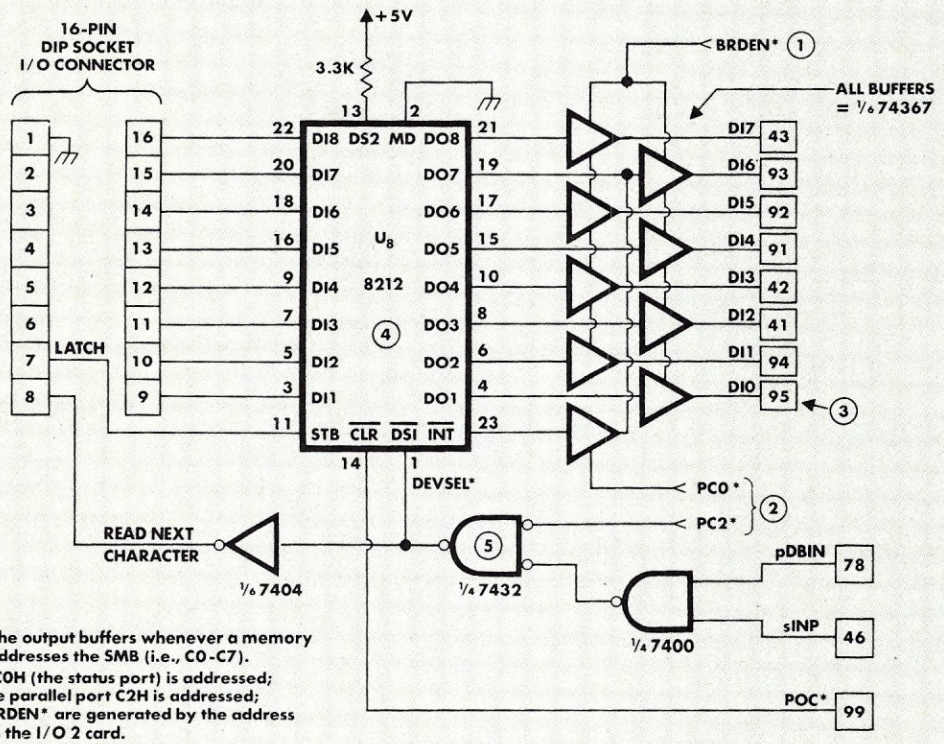
The next problem is to decide what signals to look at. Remember that even though it is not yet clear how, I am assuming that the VTI board is somehow associated with the problem. Figure 3 shows the board address circuit of the VTI. It seems logical that if this board is part of the problem, then maybe it is being enabled at the wrong time. Therefore, one channel of the scope is used to monitor the VTI's board select signal (BS*).

One remaining question is: How do we know what the wrong time is? Examining Listing 1, it is apparent that the only input instructions in the program address ports C0H or C2H, but never port FCH. Therefore the sINP signal on the S-100 bus can be used to trigger the scope, since it will be active only during input instructions. Furthermore, the VTI's board-select signal should never be active (i.e., low) while sINP is high.

From the above discussion it should be apparent that a dual-trace triggered-sweep scope is required to isolate the problem further. If you do any work on your own computer equipment, you should own or be able to borrow such a scope. It is the one piece of test gear that is essential for microcomputer troubleshooting.

The top trace in Figure 4 is the sINP signal seen when the test program has been forced to loop by setting the test switches to 11111100. The first pulse corresponds to the input instruction at address 0100H when the status port (C0H) is read in. The second sINP pulse occurs when the data port at C2H is read in (address 0106H in the program).

The second trace is the BS* (VTI board select) signal, which we stated should never go low during an input instruction that addresses C0H or C2H. However, as shown in Figure 4, BS* clearly does go low while the first sINP pulse is present. We have just made the first big breakthrough toward understanding the problem!



NOTE 1: BRDEN* activates the output buffers whenever a memory or I/O instruction addresses the SMB (i.e., C0-C7).
NOTE 2: PC0* is low when C0H (the status port) is addressed; PC2 is low when the parallel port C2H is addressed; PC0*, PC2*, and BRDEN* are generated by the address decoding circuits on the I/O 2 card.
NOTE 3: Indicates S-100 bus connectors.
NOTE 4: On the 8212, pin 24 = +5V, and pin 12 = GND.
NOTE 5: 7432 OR gate functioning as an AND gate.

Figure 2a. Parallel input port constructed on a solid-state music (SSM) I/O 2 PROM universal board.

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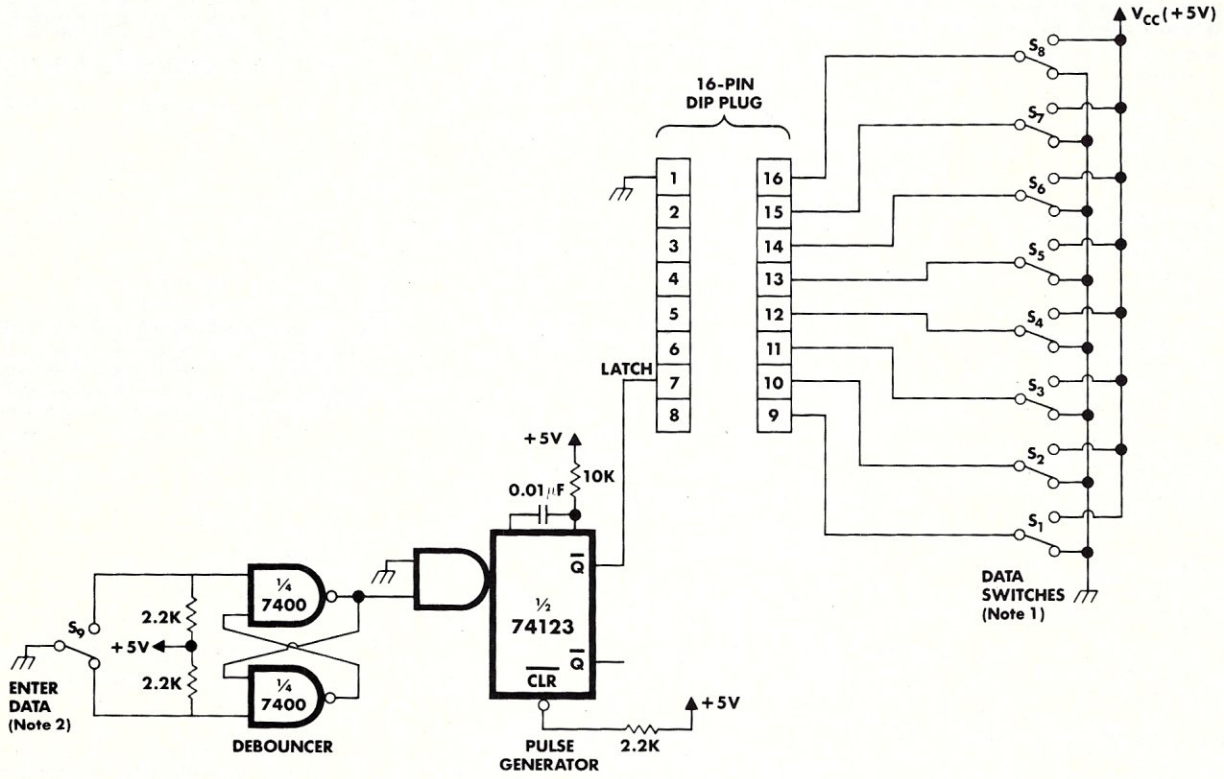

NOTE 1: S_1–S_8 are SPDT switches.
NOTE 2: S_9 is a momentary SPDT switch.

Figure 2b. Test circuit and connector to mate with parallel input port of Figure 2a.

Looking at the first two traces in Figure 4, we can begin to see why the program loops when it's not supposed to. When the first instruction in the program attempts to read the status port, both port C0H and port FCH are enabled at the same time. Thus the parallel port status in bit 6 of C0H is masked out by the simultaneous reading of the data from port FCH. The program then assumes that new data has been loaded into the parallel port, so it reads it, displays it, and jumps back to check the status of the port again. As long as the VTI is enabled while the status port is being read, the program will continue to loop. But hang on a second, let's not start feeling too smug yet: We still don't know why the VTI is being selected in the first place, or why the problem only occurs for certain settings of the input switches.

First, let's see if we can find out why the VTI is being incorrectly enabled. A good place to start is with the address lines at the input to the 8131 chip (refer to Figure 3). This is where a logic analyzer would really come in handy, since there are six lines to examine. However, we can get by with a two-channel scope by using the following procedure. Trigger the scope on the sINP signal as before. It is input on channel B and is used as a reference for measuring the other signals. Copy the sINP signal on to a piece of graph paper, along with the channel A input that had been monitoring the BS* signal. Leaving sINP displayed on channel B, move the channel A probe to pin 11 of the 8131 and copy the address signal A15 onto the graph paper, taking care to maintain the correct timing relationship with sINP. Then move the channel A probe to the next address and then repeat the procedure until all the signals of interest have been copied on to the graph paper.

The eight signals in Figure 4 were obtained using this method. Studying Figure 4, we can see that during the two sINP pulses the address bus is 110000XX (where XX represents the state of lines A9 and A8, which were not monitored). This is the expected result because either port C0H or C2H is being addressed during the input instructions. However, it can also be seen that just before and after the first sINP pulse, the address bus is set to 111111XX (i.e., FCH, FDH, FEH, or FFH, any of which address the keyboard port on the VTI). We are still faced with two questions, namely:

- Why are the six most significant bits of the

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address bus set high before the first input instruction?

- Why does the VTI latch up in the board-enabled condition, considering that the card's address is present for only a very short time before the correct information appears on the address bus?

Final solution

I was not familar with the characteristics of the 8131 IC, so this seemed to be a good area to investigate next. This IC is made by National Semiconductor and is described on page 1-141 of National's 1974 Digital IC databook. The 8131 is a 6-bit comparator with an output latch! The comparator's output is latched when pin 7 (STROBE*) goes from a logic "1" to a logic "0".

Now we are getting somewhere. At least we know why the VTI stays enabled even when a different input port is addressed. But we still don't know how the VTI address got on the bus in the first place. If that address had not been present, the VTI wouldn't have latched up in the enabled condition, and we would not have had a problem.

I started to think about how the address bus could contain the wrong information. The problem is particularly strange because the data appearing on A8-A15, during the glitches shown in Figure 4, is the same as that read in on the parallel input port! Then I remembered that besides offering more I/O instructions than the 8080, the Z80 also differs in the way it handles the address bus during I/O operations.

During an 8080 input or output instruction, the chip's eight most significant address lines (A8-A15) are set equal to the low-order lines A0 through A7. The VTI takes advantage of this fact to allow both memory and I/O operations to address the board, while only decoding A10 through A15 in both cases. This is a fairly common technique, where both memory and I/O ports are constructed on a single card.

On the other hand, the Z80 outputs the contents of either the A or B register on A8-A15 during I/O instructions (see reference 1). External circuits on the S.D. Sales Z80 board map A0-A7 onto A8-A15 during an I/O instruction. However, the only way these circuits can detect when an I/O operation is occurring is by the state of the INPUT/OUTPUT REQUEST (IORQ*) signal from the Z80. As Figure 5 shows, there is a delay of approximately one clock period betwen the time the address bus becomes stable and the time IORQ* goes low. Thus in a Z80 system, address lines A8-A15 will always differ from A0-A7 for a short period at the start of an I/O instruction. Normally, this would not cause a problem unless an I/O port latches onto the address present at the start of the instruction, and this is exactly what the VTI does.

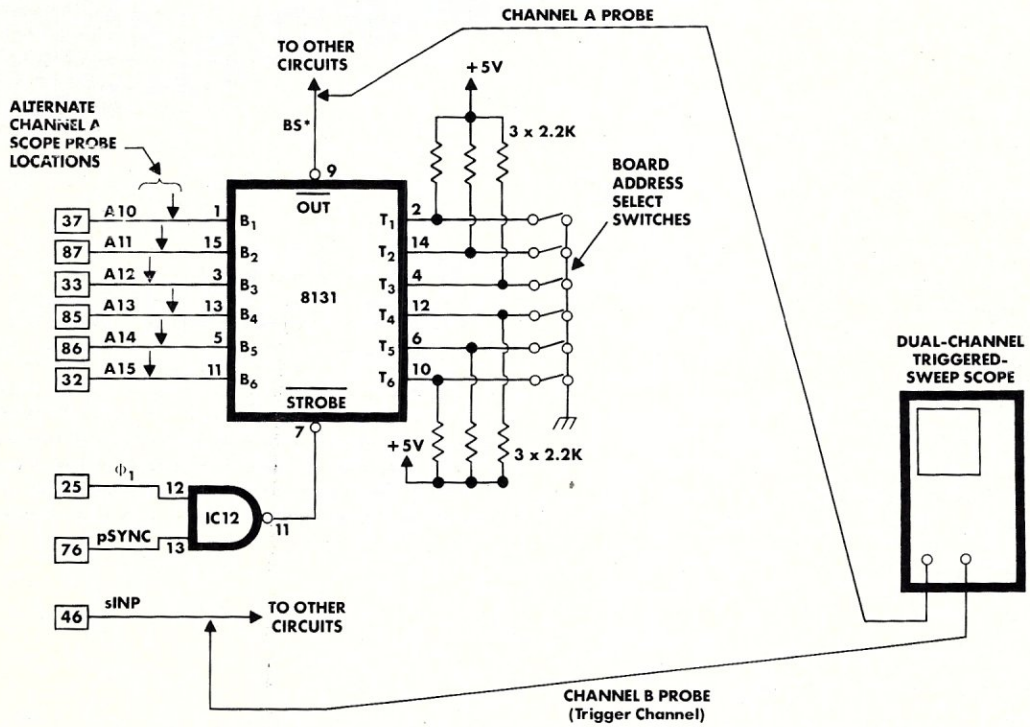

Figure 3. Address decode logic on the Polymorphic VTI. When the board is selected, the output of the 8131 is low (BS*). The measurement set-up for obtaining the traces of Figure 4 is also shown.

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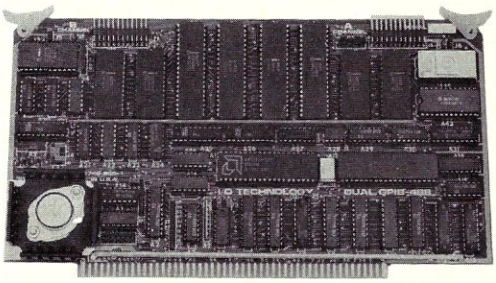

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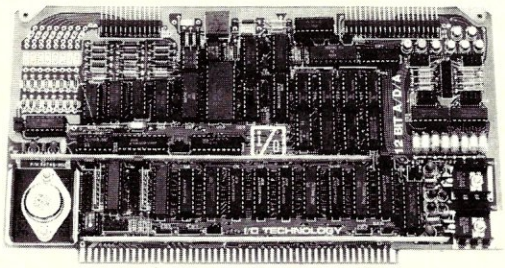

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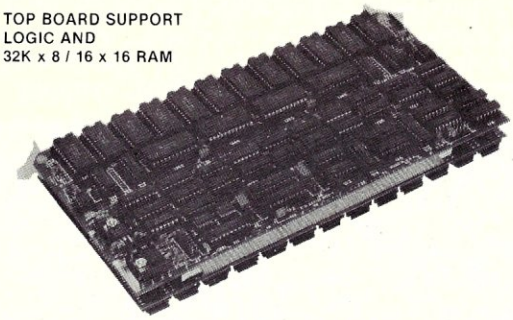

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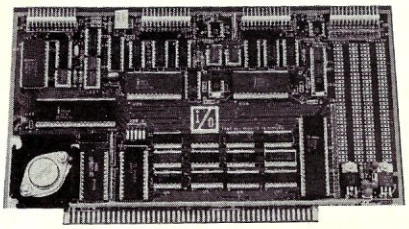

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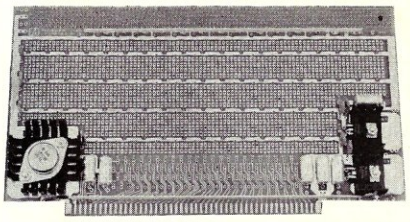

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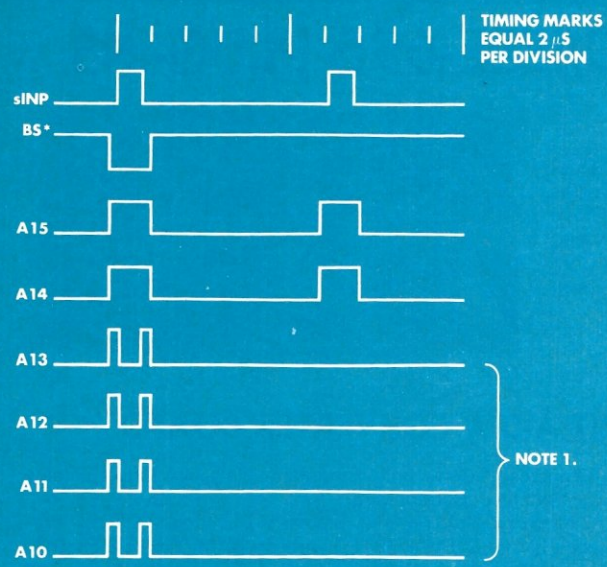


NOTE 1. Glitches are slightly exaggerated for clarity.

Figure 4. Polymorphic VTI waveforms. These traces were obtained while the test program of Listing 1 was being executed and the data input switches were set to FCH.

At last the whole reason that the problem occurs can be understood. Referring to Listing 1, we see that at address 0106H, the data from the switches is read into register A. It will remain there until the problem loops back to its starting point to read in the status port. As explained earlier, the A register contents will appear on A8-A15 at the start of this input instruction. If the data in A (read from the switches) happens to correspond to the address of the VTI card, then that card will latch up in the enabled state for the duration of the input instruction.

Under these conditions, the input instruction at program address 0100H will receive data from both the status port and the VTI. The value of bit 6 of this status word no longer reflects the true status of the parallel input port. Thus the program goes on to 0106H, thinking that new data has been entered. Before this input instruction is executed, the A register contains the status word, which does not equal FCH; thus the VTI does not latch up and the switch data is read in. As long as it equals the VTI address the problem will recur, since each time the program attempts to read the status port the VTI will latch up.

The easiest way to fix the problem is to turn the 8131 into a nonlatching comparator by grounding its strobe input (pin 7). Figure 6 illustrates the revised VTI circuit. In this way the VTI will be enabled for a short period while address lines A8-A15 change from the contents of the A register to the address present on A0-A7. Since the 8131 is no longer latching, as soon as the VTI address disappears, the board will be disabled and it will not interfere with the addressed input port.

Troubleshooting tips

The problem described in this article is a fairly complex one, involving the interaction of three different pieces of hardware. The fact that I was eventually able to isolate and correct the problem can be attributed to applying a number of different troubleshooting techniques. Not one of these techniques by itself yielded the answer, but each one contributed to the final solution.

The next time you have a problem with your computer, you may want to use some of the debugging tools described in this article. A summary of the techniques that I have found to be useful would include:

- *Knowledge of your system.* Sometimes, as in this case, valuable clues as to the nature of a problem result from relating a symptom of the problem to a part of your system.
- *Divide and conquer.* Split up the problem as much as possible. Test each part of the hardware and software as separate units until the malfunction or bug is located. When interfacing a new device to your computer, make sure that both the interface and the device work separately before connecting them together.

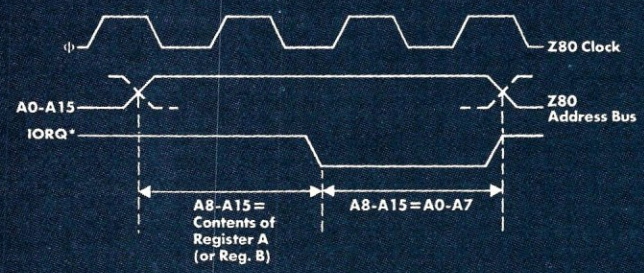
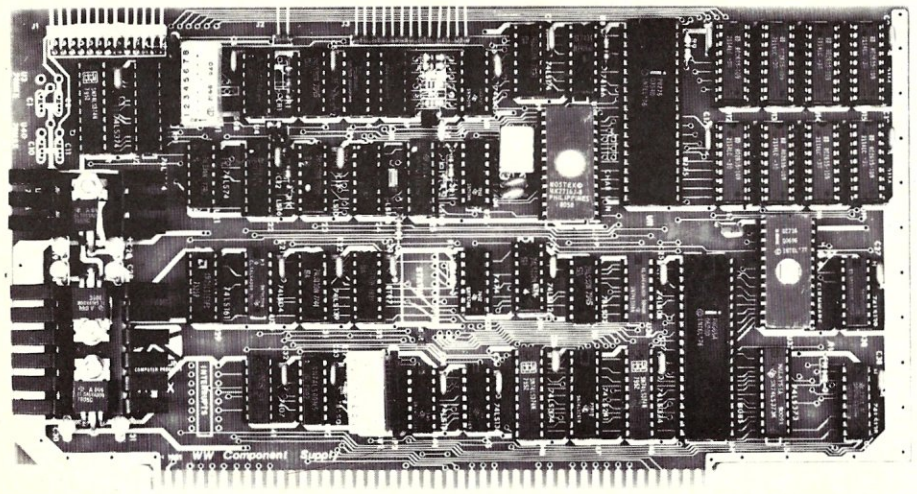


Figure 5. Z80 timing diagram for input or output operations. Note that the address lines stabilize before IORQ* goes low, signifying that this is an I/O instruction. External circuits on the CPU board use the IORQ* signal to gate A0-A7 onto the A8-A15 lines during an I/O operation.

It is frequently helpful and often necessary to use software troubleshooting aids to complement hardware test procedures.

INTELLIGENT VIDEO I/O FOR S-100 BUS



VIO-X

The VIO-X Video I/O Interface for the S-100 bus provides features equal to most intelligent terminals both efficiently and economically. It allows the use of standard keyboards and CRT monitors in conjunction with existing hardware and software. It will operate with no additional overhead in S-100 systems regardless of processor or system speed.

Through the use of the Intel 8275 CRT controller with an onboard 8085 processor and 4k memory, the VIO-X interface operates independently of the host system and communicates via two ports, thus eliminating the need for host memory space. The screen display rate is effectively 80,000 baud.

The VIO-X1 provides an 80 character by 25 line format (24 lines plus status line) using a 5 × 7 character set in a 7 × 10 dot matrix to display the full upper and lower case ASCII alphanumeric 96 printable character set (including true descenders) with 32 special characters for escape and control characters. An optional 2732 character generator is available which allows an alternate 7 × 10 contiguous graphics character set.

The VIO-X2 also offers an 80 character by 25 line format but uses a 7 × 7 character set in a 9 × 10 dot matrix allowing high-resolution characters to be used. This model also includes expanded firmware for block mode editing and light pen location. Contiguous graphics characters are not supported.

Both models support a full set of control characters and escape sequences, including controls for video attributes, cursor location and positioning, cursor toggle, and scroll speed. An onboard Real Time Clock (RTC) is displayed in the status line and may be read or set from the host system. A checksum test is performed on power-up on the firmware EPROM.

Video attributes provided by the 8275 in the VIO-X include:

- FLASH CHARACTER
- INVERSE CHARACTER
- UNDERLINE CHARACTER or
- ALT. CHARACTER SET
- DIM CHARACTER

The above functions may be toggled together or separately.

The board may be addressed at any port pair in the IEEE 696 (S-100) host system. Status and data ports may be swapped if necessary. Inputs are provided for parallel keyboard and for light pen as well as an output for audio signalling. The interrupt structure is completely compatible with Digital Research's MP/M ®.

Additional features include:

- HIGH SPEED OPERATION
- PORT MAPPED IEEE S-100 INTERFACE
- FORWARD/REVERSE SCROLL or
- PROTECTED SCREEN FIELDS
- CONVERSATIONAL or BLOCK MODE (opt)
- INTERRUPT OPERATION
- CUSTOM CHARACTER SET
- CONTROL CHARACTERS
- ESCAPE CHARACTER COMMANDS
- INTELLIGENT TERMINAL EMULATION
- TWO PAGE SCREEN MEMORY

VIO-X1 – 80 × 25 5 × 7 A & T **$295.00**
Conversational Mode
VIO-X2 – 80 × 25 7 × 7 A & T **$345.00**
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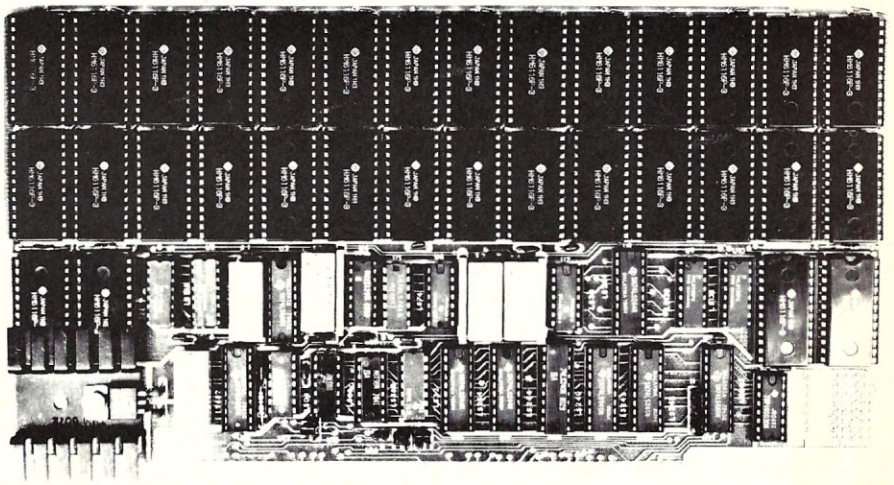

FEATURES

- Conforms to IEEE 696 standard.
- 8 or 16 bit data transfers.
- 24 bit addressing.
- Bank select in 32K-32K or 48-16K.
- Banks selectable/deselectable on DMA.
- Responds to phantom pin 67 or 16.
- 2Kx8 static rams with 2716 pin out.
- Power consumption is typically 600 ma.
- Banks on or off on power up.
- Bank addressable to any of 256 possible ports.
- 8MHz with 150ns parts standard faster speeds available on request.
- Available partially loaded as a 32K board.
- Multiple bank residence.

NEW FEATURES

- Phantoms read only, or read and write.
- Generates onboard M-WRITE, or uses bus M-WRITE.
- Two seperate banks, independently addressable on 16K boundaries. Banks may be overlapped.

OMNIRAM REV. C

OMNIRAM INTRODUCTION:

The Fulcrum Computer Products OMNIRAM for the IEEE 696 (S100) bus provides 64 kilobytes of fast static random access memory. Provision is made for 8 or 16 bit transfers, extended 24 bit addressing, and for control via the bus phantom line. In addition, a number of features are included to make the OMNIRAM compatible with systems designed before the IEEE 696 standard was developed. These include bank selection and provision for operation with IMSAI-type front panels. When the bank select option is activated, the board is divided into two parts which can reside in separate banks. The division of the board may be into two 32K sections or into one 16K section and one 48K section. 2K blocks may be disabled in the upper 16K, or 4K blocks in the upper 32K, of memory. Provision is made for DMA overide of bank select if needed. The board is also compatible with IEEE 696 or IMSAI-type extended addressing.

Omniram 64 United States & Canada Prices Only

	64K	32K
With Hitachi 6116		
150ns. Rams	$425	$300
120ns. Rams	$550	$395
Board Without Ram	$200	

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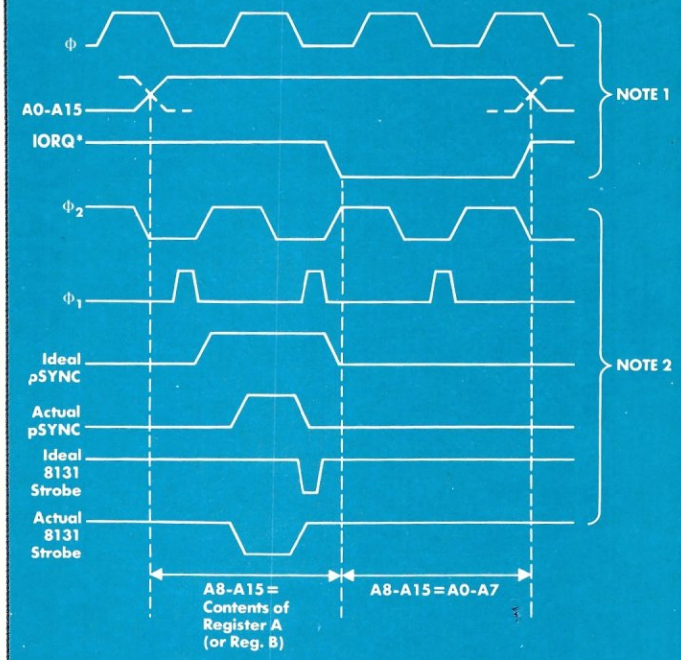
- *Software diagnostics.* A diagnostic is a program that exercises a piece of hardware and indicates whether or not it is functioning properly. As shown in this article, these programs can be very simple, especially when used in conjunction with a hardware test circuit.
- *Program loops.* When using a scope, a repetitive signal is required to trigger the display. A simple program loop exercising the suspect hardware will allow a scope to be used to examine the problem.
- *Use the scope as a logic analyzer.* Once the scope is triggered by some signal, it can be used as a multichannel logic analyzer by using one probe to compare all signals of interest to the trigger signal. Copying each signal onto graph paper allows the timing relationships of many signals to be examined.
- *Reference material.* There are so many ICs on the market that a good set of data books is really necessary to understand what a circuit is designed to do. The reference manuals that came with your hardware are also an important source of information.

Conclusions

By following a specific hardware problem from its discovery through its solution, this article has presented a number of troubleshooting techniques that should be useful to most computer hobbyists. We have seen how both hardware and software troubleshooting techniques are required to isolate a computer problem.



NOTE 1. Signals generated by Z80 chip

NOTE 2. S-100 bus signals generated by the S.D. Sales CPU board and the Polymorphic VTI

Figure 7. Z80 and VTI timing diagram. This diagram shows that if the CPU board were to properly generate all S-100 timing signals, the VTI would still be strobed at the wrong time.

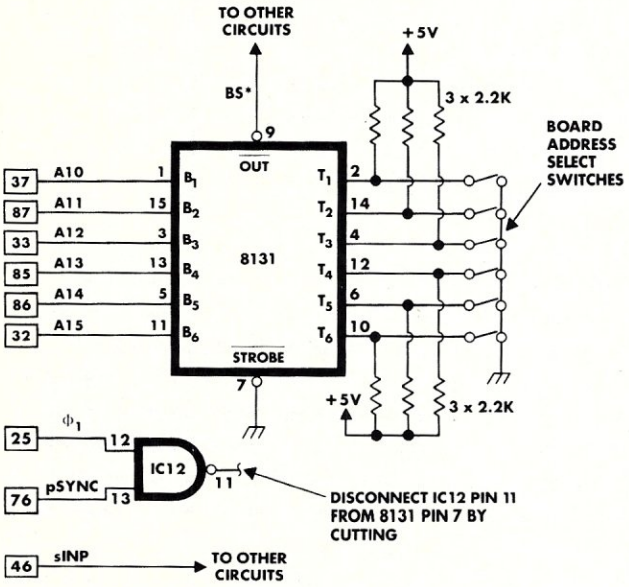


Figure 6. Modified VTI address decode logic, making the 8131 nonlatching

In tracking down the problem, a two-channel triggered-sweep scope was the only piece of test gear used (besides the computer itself). Using the scope to perform some of the functions of a logic analyzer helped considerably in determining the cause of the problem.

Anyone who has a Z80 microcomputer and a Polymorphic VTI, and who has noted strange problems that occur at infrequent intervals, may want to try the modification to the VTI shown in Figure 6.

Since the problem only occurs when the A register contains the address of the VTI card immediately before an input instruction addressing another port, it won't crop up too frequently.

Before adding the parallel input port, which led to the discovery of the problem, I had observed occasional mysterious bugs affecting my computer. Since I modified the VTI, these have all disappeared.

I am not familiar with any other S-100 boards that use a latching address decoder. However, if there are any, they would likely cause the same problem that the VTI did when used with a Z80. In the light of my experiences, the use of latching address decoders in S-100 bus systems with Z80 processors should be avoided.

It is difficult to blame either the S.D. Sales Z80

or the Polymorphic VTI for the problem outlined in this article. Although the VTI is the card I modified, it probably conforms to the S-100 bus timing standards, whereas the Z80 does not. On the other hand, it is unfortunate that the operation of the S-100 bus is so closely tied to the timing of the 8080 processor. This makes it very difficult, if not impossible, to put other processors on the bus and ensure that they will work with every other S-100 card under all circumstances.

Afterword

When I first built my VTI over a year ago, it would not work with my S.D. Sales Z80 CPU. As it turned out, the reason for this was that the pSYNC signal generated by the S.D. board did not conform to the S-100 bus timing requirements. pSYNC and ϕ_1 were never both high at the same time. Therefore the STROBE* signal to the 8131 never went low (Figure 3). To make the VTI work, I had to disconnect the ϕ_1 signal from pin 12 of IC12. This allowed the 8131 to be strobed whenever pSYNC went high.

The problem described in this article was corrected by disabling the latching feature of the 8131 as controlled by its STROBE* input. As I was preparing this article, I began to wonder whether, if pSYNC had been generated properly, the problem would have occurred at all.

Figure 7 is a repeat of Figure 4 with the addition of some of the S-100 signals as generated by my S.D. Sales CPU board. The pSYNC signal as defined in the IEEE S-100 bus standard is shown as IDEAL pSYNC. If this signal had been generated properly, the 8131 would have been strobed as shown by the IDEAL 8131 STROBE. The actual 8131 strobe is shown as the last trace in Figure 7 (remember, I had to disconnect ϕ_1 from pin 12 of IC12).

Note that both strobe pulses occur before the address bus has switched over, so that A8-A15 equals A0-A7. Therefore, the problem *would* have occurred even if the S.D. CPU board had generated the correct pSYNC signal.

The S-100 bus signals are synthesized by the CPU board, but are not locked to the Z80 clock. Therefore, individual Z80 cards may exhibit slightly different timing relations between θ and ϕ_1. However, the timing margins are so close that I suspect any Z80 card will cause trouble when used with peripheral boards employing latching address decoders.

References

1. *MOSTEK Z80 Technical Manual* (MP1031/277 Rev. B).
2. *S.D. Sales Z8800 CPU Card Manual,* 1976.
3. *Polymorphic Systems Video Terminal Interface Manual,* 1976.
4. *Solid State Music I/O PROM Universal Card Manual,* 1976.
5. *National Semiconductor Digital IC Manual,* 1974.

Listing 1

```
TDL Z80 RELOCATING ASSEMBLER VERSION 2.2                    PAGE 1

                        ;*** PARALLEL INPUT PORT TEST PROGRAM ***
                        ;
                        ;THIS PROGRAM WAITS FOR DATA TO BE LATCHED INTO
                        ;THE INPUT PORT (0C2H) AND THEN DISPLAYS THE DATA
                        ;ON THE SYSTEM CONSOL
                        ;
                        ;IT USES TWO MONITOR SUBROUTINES:
                        ;   DSPBIN - WHICH PRINTS THE A REGISTER IN
                        ;            BINARY ON THE SYSTEM CONSOL
                        ;   CRLF   - WHICH ADVANCES THE SYSTEM CONSOL TO
                        ;            THE START OF A NEW LINE
                        ;
                                .LOC    100H            ;RUN IT ON PAGE 1
                                CRLF=0C19AH             ;MONITOR ADRESSES
                                DSPBIN=0C1A9H
0100 DBC0               START:  IN      0C0H            ;GET STATUS BYTE
0102 CB77                       BIT     6,A             ;CHECK BIT 6=0
0104 20FA                       JRNZ    START           ;NO, TRY AGAIN
0106 DBC2                       IN      0C2H            ;ELSE READ DATA
0108 CD C1A9                    CALL    DSPBIN          ;& PRINT IT
010B CD C19A                    CALL    CRLF            ;NEW LINE
010E 18F0                       JMPR    START           ;THEN REPEAT

                        ;       Listing 1. Parallel Input Port Test Program

                                .END
```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It's the writing on the wall

CIRCLE 73 ON READER SERVICE CARD

The Ackerman Digital/Systems Promblaster

A versatile and convenient S-100 PROM programmer

by Ian F. Darwin

What a bewildering array of EPROM types we face! There are two different EPROMs called 2716: One needs only a single voltage, one uses three different voltages. Similar confusion exists for the 2708 and other EPROM types. But people who play the microcomputer game often need to read or write EPROM software. When I decided to buy an S-100 EPROM board, only the Ackerman Digital board seemed to have all the features that I wanted. It was available in bare-board form or as a kit, claimed IEEE-696 standard compliance, was from an established company, and handled a wide range of EPROM types. I ordered the bare board.

The board is cleanly laid out, neatly screened, and is the first board I've seen that had the legend "IEEE-696 Compliance" printed right on it, specifically, "SLAVE I8/16 W2 T250." This shows that it was a slave (generally CPUs are masters, I/O boards can be "temporary masters" or slaves, and memory boards are slaves), can use 8- or 16-bit I/O addressing (i.e., can use 8080/Z80 I/O with 255 ports, or can use 16-bit I/O with 65535 port addresses). The data transfer is 8-bit only; there is no sXTRQ* line. It can also provide up to two wait states and has a worst-case access of 250 nanoseconds. (For more details on these markings, see the article on "The IEEE Standard" in *Microsystems*, 1981: Vol. 2, No. 5, page 46.) The board is designed to work at 1, 2 or 4 MHz. It may work to 6 MHz, but the documentation makes it seem unlikely.

The Promblaster has features beyond those of other boards. There are no "personality modules" such as one finds with other EPROM boards: It's *all* done in software. By comparison, the MicroDynamics board, a newly announced IEEE-696 S-100 EPROM programmer, needs a personality module (a small piece of hardware) for each different EPROM type. When buying the ADS board, do buy the ADS software package, Promwriter; it's worth it! Worth it if you have an 8080/Z80 CPU, that is; the software is in machine code

Ian F. Darwin, 467 Melita Crescent, Toronto, Ontario M6G 3X9 Canada

Table 1. EPROM types

ADS software name	Mfr's capacity rating	Used as	Manufacturer	Official name	Pins	Voltages
INT2708	8Kx1	1Kx8	Intel	2708	24 pin	3 voltage
TMS2708	8Kx1	1Kx8	Texas Inst.	2708	24 pin	3 voltage
MCM2708	8Kx1	1Kx8	Motorola	2708	24 pin	3 voltage
TMS2508	8Kx1	1Kx8	Texas Inst.	2508	24 pin	1 voltage
INT2716	16Kx1	2Kx8	Intel	2716	24 pin	1 voltage
TMS2516	16Kx1	2Kx8	Texas Inst.	2516	24 pin	1 voltage
TMS2716	16Kx1	2Kx8	Texas Inst.	2716	24 pin	3 voltage
MCM2716	16Kx1	2Kx8	Motorola	2716	24 pin	1 voltage
TMS2532	32Kx1	4Kx8	Texas Inst.	2532	24 pin	1 voltage
INT2732	32Kx1	4Kx8	Intel	2732	24 pin	1 voltage
INT2764	68Kx1	4Kx8	Intel	2764	28 pin	1 voltage
TMS2564	64Kx1	8Kx8	Texas Inst.	2564	28 pin	1 voltage
MC68764	64Kx1	8Kx8	Motorola	68764	24 pin	1 voltage

***Note:** Compatible EPROMS can be programmed by using the name of the nearest equivalent; e.g., Hitachi HN462716 may be blasted under the name INT2716.*

and you do *not* get the source. If you need/want to write your own, the documentation should be adequate and does include one example, for programming a 2716 EPROM, in assembler.

The Promwriter software provides complete control over the EPROM board, including reading and writing EPROMs, setting up the board for different EPROM types, and so on. Most of the parameters for the board are set through the four I/O ports.

The software selects the voltages and timing for a number of different EPROM types (Table 1). It will also verify unprogrammed EPROMS and check that an EPROM has been programmed correctly. It will load a .HEX file into memory for programming and even give you a list of .HEX files on your disk! (See Table 2).

Table 2. Promwriter software commands

B—Base port address
C—Check that EPROM is erased
D—Dump memory
E—Exit to CP/M
F—Fill memory
H—Help summary
L—Load .HEX file into memory
O—Offset for subsequent memory references
P—Program an EPROM
Q—Query .HEX files in CP/M directory
R—Read an EPROM into memory
S—checkSum of memory
T—set Type of EPROM
V—Verify that EPROM matches memory

The Promwriter program is not menu driven, but its built-in Help command and its simple commands make it quite easy to use. Only "standard" CP/M facilities appear to be used; it reads .HEX files and the CP/M directory with no trouble on my Intersystems double-density DMA floppy controller. No special assumptions are made about terminal size, speed or smartness.

One curious effect of the lack of "personality" modules is that you must not insert the PROM into the hardware until you have told the software what kind of PROM is used, since strange voltages may be present! In addition, you are not supposed to RESET the S-100 with a PROM in the programmer. I don't know what happens if you do—the manual warns of dire consequences. If you're worried, you might think about bringing the EPROM socket to the front panel via ribbon cable and mounting the socket near your RESET button. ADS has developed this as an add-on kit, but I have not received mine yet.

One feature I'd like to see added to the software relates to port selection. The ADS "Promwriter" software assumes I/O ports CO . . C3 for the board, but I have a PMMI modem board at those addresses. The ADS software has a (B)ase command for changing this, but I keep forgetting to enter it! If they were to publish the locations(s) which the Base command changes, I could use DDT to alter them permanently.

Another "nice feature," although used only infrequently, would be the ability to (W)rite a .HEX file: If you can read them, why not write them? This feature exists in the new software, which I have not yet received.

In assembling the board, I had trouble locating a few parts. I would suggest that if buying the bare board rather than the kit, you buy the 28-pin LIF socket (Low Insertion Force; this makes it easy to insert/remove the EPROM), the 250-μH choke, and maybe (depending on your local supplier) the TL497 switching regulator and the 74LS682 ICs from ADS when you order the board. (The 28-pin is only needed for 64K EPROMs; the 2708 through 2732 all use the readily available 24-pin socket, which you could get by with until 64K EPROMs become commonplace.)

I do wish that manufacturers who sell bare boards would tell you up front when there are hard-to-find parts! These are listed in the ADS catalog, but I ordered the board directly from one of their magazine ads and got the catalog with the board!

The documentation is quite good. The hardware manual is neatly printed and contains complete assembly instructions and detailed checking procedures. It does fail to explain a few jumper options. Most readers of this magazine would be able to figure out most of these from the complete schematic in the manual, but the address decoder switches are obscure and the comparator is a new IC (74LS682) that isn't in most TTL data books yet. ADS has said they will add the missing information in the next version of the manual. There was one small error in the testing instructions in my version. The software manual I received was a faded photocopy of the output from a matrix printer. Despite the poor print quality, the documentation is readable and reasonably complete.

I had to call ADS once or twice for technical

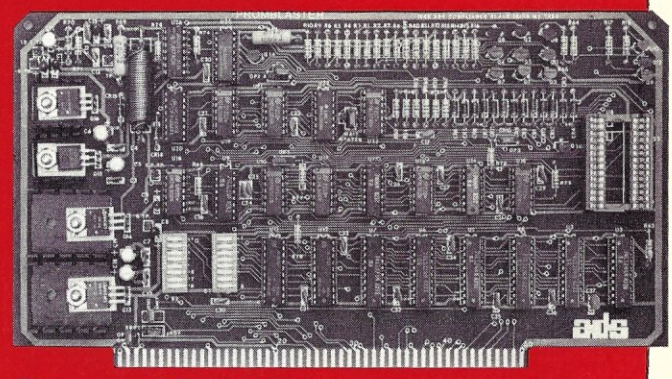

Figure 1. *ADS Promblaster, component side*

The Promblaster has features beyond those of other boards. There are no "personality modules" such as one finds with other EPROMs: It's all done in software, which provides complete control over the EPROM board.

The Ackerman Digital Systems Promblaster continued . . .

assistance; they were helpful over the phone. They are also very good with software updates: I've only had the thing a short while and have received, without charge, two patches to the software (in the form of .ASM source, a dozen or so lines long, to type in and add with DDT).

I haven't gotten the board working with my old S-100 system, but I suspect this is due to a timing problem with my very nonstandard CPU. ADS has an optional hardware mod for such a problem, and I have applied it. The board works fine with my Godbout 8085/8088 CPU board. There are no jumper options for inverted clocks and such things that one finds on some manufacturers' boards.

```
ADS PROMWRITER VER 1.2 #2012 (H FOR HELP)
COPYRIGHT (C) 1981 BY ACKERMAN DIGITAL SYSTEMS, INC.

:TTMS2708                (I tell it I'm going to insert a 2708 EPROM)
                         (I insert the EPROM)
:R4000,44FF,0            (I tell it to read into memory 4000 from EPROM)
SIZE ERROR               (it checks!)
:R4000,43FF,0

:D4000,4010              (dump the first few bytes)

4000 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
4010 FF                  (the EPROM was blank, FF's imply ERASED condition)
:P100,110,0              (Program the EPROM from elsewhere in memory)

:R4000,4010,0            (read it back in for visual examination)

:D4000,4010              (and dump both EPROM data...)

4000 C3 78 01 B6 0C 00 00 05 00 00 00 C0 00 0D 01 10
4010 01
:D100,110                (... and original data)

0100 C3 78 01 B6 0C 00 00 05 00 00 00 C0 00 00 01 10
0110 01
:R5000,5100,0            (here I changed EPROMS, still same type)
                         (now dump contents
:D5000,501F               of newly-inserted EPROM)

5000 C3 40 00 C3 43 00 CD 16 00 CA 06 00 DB 00 E6 7F
5010 FE 03 CA 43 00 C9 DB 01 E6 02 C9 F5 CD 16 00 CA
:
```

Conclusion

If you want a good IEEE-696 S-100 EPROM burner that is moderately priced and well supported, try the Ackerman Digital PromBlaster.

For further reading:

Intel *Memory Design Handbook*, 1977: Santa Clara, CA.
Section on ROMs provides introduction to ROM and EPROM technology and programming, with detailed discussion of the Intel 2708 and 2716. The book is $5 from Intel Literature Department, 3065 Bowers Ave, Santa Clara, CA 95051. Ask for notes on the 2732/2764 if interested.

Croal, Ted: "An S-100 EPROM programmer using the Intel 8255 PPI." *Microsystems*, 1980: Vol. 1, No. 6, page 46.
Describes construction of a low-cost 2708-only programmer.

Golter, L.B.: "Build a low-cost EPROM Eraser." *Byte*, April 1980, page 234.

Ciarcia, Steve: "Build an intelligent EPROM programmer." *Byte*, October 1981, page 36.

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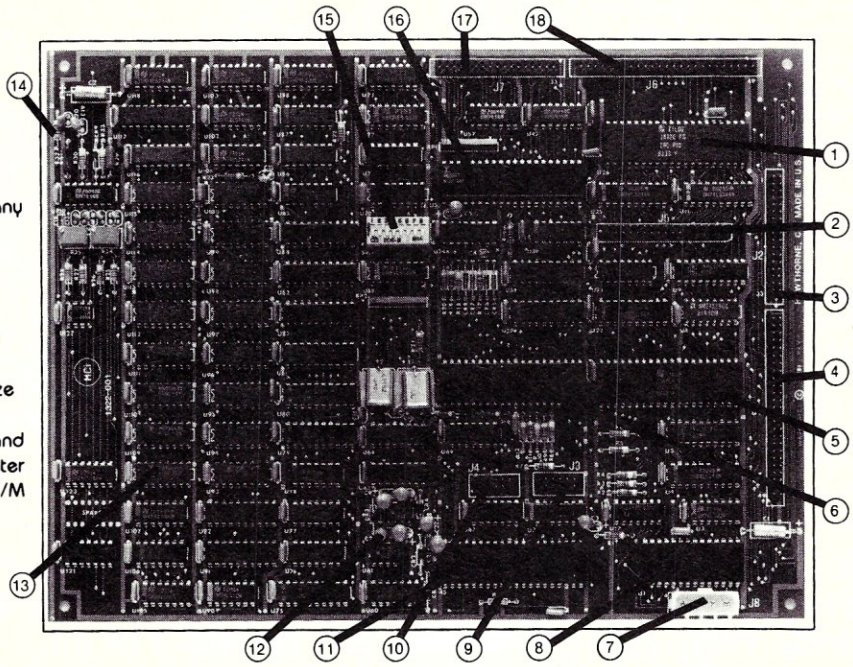

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CIRCLE 63 ON READER SERVICE CARD

Promblaster continued . . .

At a glance

Name: Promblaster (hardware), Promwriter (software)

Use: Programming Erasable Programmable Read-Only Memories (EPROMs) for storing programs and/or data in semipermanent computer memory

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System: S-100, IEEE-696 compliance

Features: Supports wide range of EPROM types from 2708 to 2764, programs from memory or reads .HEX file

Needs: CP/M operating system (or write your own software); S-100 bus system with system clock rate of 1-4 MHz

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CIRCLE 10 ON READER SERVICE CARD

Bring the flavor of Unix to your Z80 CP/M system with Unica

"Unicum: a thing unique in its kind, especially an example of writing. Unica: the plural of unicum."

The Unica: a unique collection of programs supporting many features of the Unix operating system never before available under CP/M. The Unica are more than software tools; they are finely crafted instruments of surgical quality. Some of the Unica are:

bc	-	binary file compare, display differences in hex
cat	-	catenate files (vertically)
cp	-	copy one or more files, even between users
dm	-	disk mapper, reports free blocks and directory space
fid	-	file identification by unique numbers (CRC's)
hc	-	horizontal file catenation and column permutation
ln	-	create file links (multiple names for one file)
ls	-	intelligent directory lister, optional multi-columns
mv	-	move (rename) files, even between users
rm	-	remove (delete) files, with optional verification
sc	-	source file compare, with resynchronization
sfa	-	set/reset file attributes, optional verification
sp	-	spelling error corrector, with 80,000 word dictionary
sr	-	search multiple files for a pattern
srt	-	in-memory file sorter, optional duplicate line omission
tee	-	pipe fitting (copy input stream to multiple outputs)
tr	-	transliterate (translate character codes)
wc	-	word counter, counts characters, words, and lines
wx	-	word extractor, copies each word to a separate line

Each Unicum understands several flags ("options" or "switches") which control program alternatives. No special "shell" is needed; Unica commands are typed to the standard CP/M command interpreter. The Unica package supports several Unix-like facilities, such as filename user numbers:

```
sc data.bas;2 data.bas;3
```

(compares files belonging to user 2 and user 3);
Wildcard patterns:

```
rm -v *tmp*
```

(types each filename containing the letters TMP and asks whether to delete the file);
I/O redirection:

```
ls -a >proj.dir
```

(writes a directory listing of all files to file "proj.dir");
Pipes:

```
dm b: | sr free >lst:
```

(creates a map of disk B:, extracts those lines in the map which contain the word "free", and prints them on the listing device).

The Unica are written in XM-80, a low level language which combines rigorously checked procedure definition and invocation with the versatility of Z80 assembly language. XM-80 includes a language translator which turns XM-80 programs into source code for MACRO-80, the industry standard assembler from Microsoft. It also includes a MACRO-80 object library with over forty "software components", subroutine packages which are called to perform services such as piping, wildcard matching, output formatting, and device-independent I/O with buffers of any size from 1 to 64k bytes.

The source code for each Unicum main program (but not for the software component library) is provided. With the Unica and XM-80, you can customize each utility to your installation, and write your own applications quickly and efficiently. Programs which you write using XM-80 components are not subject to any licensing fee.

Extensive documentation includes tutorials, reference manuals, individual spec sheets for each component, and thorough descriptions of each Unicum.

Update policy: each Unica owner is informed when new Unica or components become available. At any time, and as often as you like, you can return the distribution disk with a $10 handling fee and get the current versions of the Unica and XM-80, with documentation for all new or changed software.

The Unica and XM-80 (which requires MACRO-80) are priced at $195, or $25 for the documentation. The Unica alone are supplied as *.COM executable files and are priced at $95 for the set, or $15 for the documentation. Software is distributed only on 8" floppy disks for Z80 CP/M version 2 systems. All orders must be paid in advance; no COD's or purchase orders, please. Quantity discounts are available. Shipment outside of the US or Canada costs an additional $20. Bank checks must be in US funds drawn on a US bank.

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SOFTWARE PRODUCT REVIEW

A Look at Pascal/MT+

by Jeff Duntemann

I write both APL and Basic code for a living, and neither is my language of choice for a home computer system. Not because they are slow languages; a little planning often makes speed unimportant. APL and Basic make it all too easy to quickly create reams of "write-only" code, in which the algorithm is obvious *now,* but six weeks of doing other things will turn it into ancient Hebrew. Pascal was designed to prevent that sort of thing. From the beginning I decided to settle for nothing less.

I consider P-code languages incomplete; if you've gotten as far as intermediate code, why not go all the way? That narrowed the field considerably: It was Pascal/MT+ by MT Microsystems, or Pascal/Z by Intersystems. I chose MT+. I won't make a judgement here on Pascal/Z, since I don't own it and have never used it, but I will put down what facts I do have, and an informed review of Pascal/Z elsewhere will allow you to make your own decisions.

Toward transportable modular code

Pascal/MT+ is a native code compiler for ISO Standard Pascal. At this writing it supports the 8080, 8085, and Z80 CPUs. (By the time you read this, the 8086/8088 version may well be available.) Future versions will support the 6809, Z8000, and 68000 as well. This was a powerful plus from my point of view. Once all the various MT+ code generators have been released, a single Pascal source program will run on any of the supported machines with only minor (and possibly zero) tinkering. With the dizzying speed at which the microcomputer field moves, I just don't *know* what sort of machine I'll be running in 1985. It could well be the 68000—and I would like to be able to bring five years' worth of hard-won software along as well. Pascal/Z, for the near term, is locked into the Z80/Z8000 family. I prefer not to limit my choices, thank you.

A close look at the MT+ runtime environment illustrates what a straightjacket a 64K address space has already become. The compiler requires a 56K CP/M system at minimum. Even so, MT+ swaps no fewer than four overlay files in and out of memory as it compiles. Using overlays is a way of "folding" a very large program down to runnable size by only running a portion of the program in memory at any one time, and reading in large chunks of code from disk as required. It is both tricky to do and time-consuming, but, sadly, quite necessary for things as sophisticated as Pascal/MT+. Furthermore, the buffer into which the compiler writes its compiled code is only 2K bytes long. This limits (and severely, I sometimes think!) the amount of code that may be present in any given BEGIN/END construct, be it procedure, function, or main program. Good programming practice dictates that BEGIN/END constructs be short anyway, for the sake of readability, but there are times when nothing but a fat procedure will really do . . . .

Jeff Duntemann, 301 Susquehanna Road, Rochester NY 14618

The output of the MT+ compiler is an .ERL (Extended Relocatable) file, which is compatible with the Microsoft Relocatable format. These .ERL files are then linked into a runnable .COM file object program by LINKMT, the MT+ linker. Conceivably, a module compiled under Microsoft Fortran could be linked with Pascal/MT+ modules, but I have not done this, nor have I heard of anyone who has. "Compatible" is often a *very* rubbery word.

The user is encouraged to follow "modular" programming practice—that is, to develop libraries of related procedures and functions that are compiled separately from the actual applications program. Such library functions are declared as EXTERNAL, and "hooks" are left with which the linker can fasten library routines to the main program at link time. This system has the added benfit of encouraging reuse of widely applicable code. I link two libraries of external routines into each applications program: One contains routines that may be applied to all of my Pascal programs (keyboard input routines, sorts and searches) and the other library contains routines specific to that application.

Many of the statements and functions of MT+ are themselves written in Pascal and are linked into the .COM file, just as user-written procedures and functions are. These code segments are stored in a very large library file. The linker is intelligent enough to search the library and link to the .COM file only those statements and functions called by the user in his application program.

There's a worm in it, though: If you decide to market an applications program containing code linked from the MT+ library, MT Microsystems requires a $500 royalty as per the license agreement. These terms are much more liberal than Microsoft's and Digital Research's (which demand the right to insert copyright notices into your code, examine your books whenever they please, and other dubious nonsense) but the concept in general leaves a sour taste in my mouth. Realize that the library does *not* contain utility subroutines, but snippets of the language itself—it is as though Intel were to demand a royalty for the use of its 8080 opcodes. In my opinion this detracts from the sincerity of the wailing we've heard about software piracy lately. Lots of hands are in lots of pockets—who's to throw the first stone?

Filling the holes in the ISO standard

Paraphrasing a popular T-shirt transfer: Pascal

may not be perfect, but parts of it are excellent. The language does have some holes, and MT+ attempts to fill a few of them.

ISO Pascal defines no "else" condition for its CASE statement (which is rather like a Basic ON/GOTO). If your input parameter does not match one of the several choices, program action is literally undefined—an academic's way of saying that the system could well crash. This is madness, and MT+, like all other Pascals I've heard of, allows an ELSE clause. If no ELSE clause is included, control simply falls through to the next Pascal statement.

ISO does not define a mechanism for doing port I/O. You can get away with that on a CDC 6000. An 8080 Pascal, to be useful, needs to be able to talk to its ports. MT+ "invisibly" declares to 256-byte arrays called INP and OUT. These arrays may take part in statements just like any other array, with the port numbers acting as subscripts. Additionally, 16-bit port I/O has been defined for the 16-bit CPU versions under development.

Three additional standard data types exist in Pascal/MT+: BYTE, WORD, and STRING. A BYTE is identical to ISO type CHAR, save that it may take part in mathematical statements. It thus provides a convenient "bridge" between character and integer types for involved character manipulation. A WORD is similar to BYTE except that it uses the full 16 bits—again, looking ahead to the 16-bit CPUs.

The STRING type is perhaps MT+'s finest extension to ISO Pascal. A STRING is an array of CHAR with element zero acting as a dynamic length pointer. MT+ provides a number of string functions for searching strings for other strings, deleting parts of strings, concatenating strings together, and subbing characters and strings into other strings. These functions are written in machine language, and they are *fast*. Strings may be compared via standard relational operators. Strings may be output to the console with a single WRITELN statement.

MT+ also supports the writing of interrupt routines in Pascal. My hardware does not support interrupts, so I have not tested this feature. Briefly, an interrupt procedure is declared in this format:

```
PROCEDURE INTERRUPT [3] KEYPRESS;
```

with code following to process a keypress when 8080 interrupt vector is received. MT+ automatically saves registers and handles the interrupt-enable flag, freeing the user from such housekeeping. However, built-in procedures ENABLE and DISABLE give the user direct control of the enable flag if needed.

Pascal/MT+ code may be written to ROM if desired, although reassembly of parts of the runtime package is required. This feature is poorly documented, and I have not yet tested it.

Math features

I do not do very much number crunching on my machine; my interests simply do not lie in that direction. Math, however, is truly Pascal/MT+'s strong suit. The user may choose either of two REAL types for his application: An 18-digit fixed-point REAL with four decimal digits and sign (22 significant figures all told) for business applications, or a scientific/engineering-oriented floating-point REAL with about 6.5 digits precision.

The scientific REAL format is that of the AMD9511 hardware floating-point chip, with good reason: The software floating-point routines emulate this chip for fast math. For *lightning* math, source given for the system hooks into an actual AMD9511, which should make an 8080/MT+ system outrun any other 8-bit system for number crunching.

All standard Pascal math functions are implemented, including square root, exponent, natural log, all trig functions and inverse trig functions. No random-number generator is supplied, which I sorely miss, though if I wanted one badly enough, writing one would not be difficult.

File I/O

All ISO standard file operations are present: GET/PUT, READ(LN)/WRITE(LN). These procedures are written in Pascal, and source is available at extra cost. Additionally, two procedures are supplied to read and write to files one byte at a time, which is a good deal faster than GET/PUT through the file window (FILENM^). For even faster file access, BLOCKREAD/BLOCKWRITE procedures are given to read and write an entire block (usually a sector) to and from the disk at once.

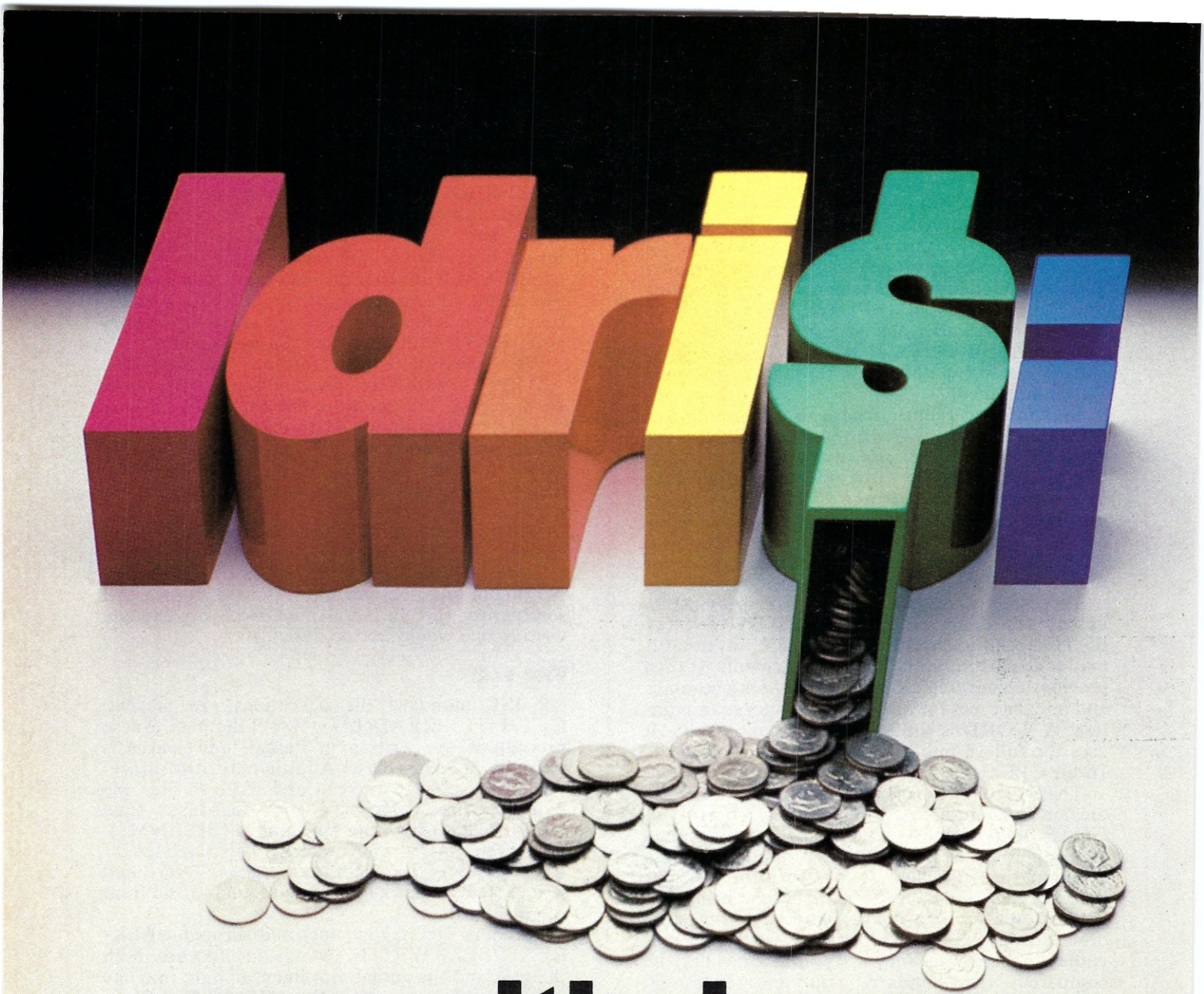
Random file I/O is supported through SEEKREAD/SEEKWRITE, which incorporate both the seek and the actual movement of data into one command. These commands, while not ISO Standard, amount to a random-access GET/PUT, and use the file window in the same manner. Random I/O is reasonably fast, and I have found it extremely convenient. In the first release of MT+, random and sequential files were not compatible. Release 5.2 and later allow sequential access of randomly written files and vice versa. There were some early bugs in the random I/O, but these have been corrected.

I should point out here that Pascal/Z does *not* implement GET/PUT, and thus is not ISO standard. This is a serious omission! That lack above anything else swung my initial decision away from Pascal/Z. Furthermore, Pascal/Z does not support random access of files.

Speed

"Speed" is another very rubbery word when applied to language systems. Compiler speed is claimed in some MT+ ads to be 1000 lines of

All creators of a language system have a responsibility to teach beginners the language. The widespread neglect of user education will ultimately limit the market. . .



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source per minute. This may be true if all lines are comments. I think a better estimate would be 300-400 LPM, and it is *very* sensitive to the type of code being compiled. Generating a .PRN file at compile time also slows things down tremendously. With all the bells and whistles and a .PRN file growing on disk, you should expect a compile speed closer to 150-200 LPM. Since most of the source blocks which I compile are less than 300 lines long, this is entirely acceptable.

The speed of the output code is an even rougher thing to estimate. A published benchmark calculating an Eratosthenes Sieve (which is a method of locating prime numbers) makes MT+ the winner at 25 seconds, followed by Pascal/Z at 129 seconds, UCSD Pascal at 239 seconds and Pascal/M at 450 seconds. If you're into prime numbers that may mean something to you; I am skeptical, especially in the light of another benchmark I found in the *Z Users' Group Newsletter* #6, which indicated that MT+ and Pascal/Z ran a number of Niklaus Wirth's own programs virtually neck-and-neck, speedwise.

My own observation is that programs compiled under MT+ ran like greased rockets compared to anything I ever did in Basic or APL. Choosing one native-code compiler over another on the basis of speed benchmarks is probably unwise. In any intelligently written compiler (both Pascals qualify) the speed-limiting factor is the target CPU, (and the benchmark algorithm!) *not* the output code.

Documentation

Here's where the claws come out! I am very familiar with MT+'s documentation and have looked over that of Pascal/Z, and both get a big, tremendous, bleeding Zero. I spent many agonizing hours flipping through the 120-odd pages (no index was included) trying to pin down the subtleties of Pascal/MT+. MT Microsystems pointedly denies any ability to teach a user Pascal. This may be true, but is it right? In my experience, one learns a language only by using it, so, in a sense, *all* creators of language systems have a responsibility to teach beginners the language.

Furthermore, one would expect, at very least, that the features of the compiler specific to Pascal/MT+ would get exhaustive treatment with numerous examples. Not so. Most of the extensions to Pascal are described in 150 words or less, many without any examples at all. In many cases, the manual directs the user to read and examine the runtime package source to learn how to do certain things. To learn Pascal, then, one has to read Pascal first. Catch 22!

This would be a killer flaw were not all other microcomputer language system user documentation as bad or worse. Ultimately, this neglect of user education will limit the market for microcomputer language systems. Eager hobbyists like myself will continue to bull through scanty, hodgepodge documentation and be glad for it. However, productivity-conscious EDP managers and small businessmen will shake their heads and go to IBM. My suggestion, for all creators of microcomputer language systems: Set aside six or seven thousand dollars as soon as possible and pay a professional tech writer to do a complete, elaborately exampled description of the language, including a beginners' tutorial. If it is written wisely it could even be mass-marketed as a Pascal text, using the vendor's own implementation as a working example. Else, who knows? We could all be buying our compilers from IBM in 10 years.

Conclusion

Pascal/MT+ has my vote as the finest native-code compiler available to the CP/M hobbyist today. There is very little which can be done in assembler that cannot be accomplished in Pascal/MT+. What penalty there is, is paid in code compactness (MT+ object modules tend to be bulky for what they do) but with the plummeting price of memory this will become less and less of a consideration. It is ISO standard and then some. Given a decent manual, it will be unbeatable.

Pascal MT+ runs on any CP/M system with 56K RAM. Price: $495. Available from:

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Build an S-100 E²PROM Board

Take advantage of the latest in PROM technology to save programs in nonvolatile memory

by Randy Reitz

Remember the days when you wanted to change that monitor or boot loader program in EPROM? You turned off your system, opened your mainframe, removed the board containing the EPROM, removed the EPROM from its socket, got out the old trusty EPROM ultraviolet, and so on . . . and about two hours later, if everything went well, you had a reprogrammed EPROM. Well, forget those days because the electrically erasable PROM is finally here, and here's how to get your S-100 E²PROM (also known as an EEPROM) up and running. Now just write to the E²PROM, just like you would to RAM, and it is reprogrammed. Wowee!

A little background

Intel has been offering a sample of their new 2817 E²PROM IC with an applications handbook (265 pages) and set of spec sheets for $10. So I grabbed the opportunity and sent away for one. The 2817 is a 2K x 8 device. It has a 250 ns read time, which means that you can use it in a 4MHz Z80 system without need for wait states.

Erasure and rewriting of the selected byte is accomplished by the application of a 21-volt pulse for 10 ms. The 2817 includes the circuitry to do this, so the designer does not even have to worry about it. However, since writing typically takes 10 ms, one has to do one of two things: either suspend processor operation during this time, or generate an interrupt so that the processor can do some other task in the meantime. The easy way out is just to suspend operation via the ready control input to the microprocessor. Naturally, I choose the easier method.

Incidentally, the 2817 is the newest of several E²PROMs from Intel. It was preceded by the 2816 and 2815. These two earlier devices are pin compatible with the trusty old 2716 2K x 8 EPROM. However, they require additional interfacing circuitry that is internal to the 2817. So although the 2817 is not compatible with any previous EPROMs, it is considerably easier to wire up a circuit.

The 2817 contains all the circuitry for it to do data writes, leaving the processor free to perform other tasks. When data is written to the 2817 it latches the address, data, and control signals, and starts to write. At the same time the READY line goes low, indicating that the 2817 is busy. The CPU can now be either halted or allowed to perform some other task. The 2817 uses the 21-volt supply to erase the selected location, write the new data, and verify that the location is successfully programmed (by comparing the data in the cell to the latched data). When this process is completed (typically 10 ms), the READY line comes back up high. The timing of this process is controlled by the value of the capacitor connected to the TC pin.

When the 2817 is not being written to or read from, it goes into a standby power mode that reduces power consumption by 50%. This occurs when the CE input is high.

Randy Reitz, 26 Maple Street, Chatham Twp., NJ 07928

The S-100 board

The circuitry for the S-100 E²PROM is shown in Figure 1. The +21 volt supply is generated from the +8 volt supply using a Fairchild 78S40 switching regulator IC and is shown in Figure 2. This circuit is a variation on a similar circuit shown by Steve Ciarcia in *Byte* magazine (November 1981, page 43). Note that the inductor is a toroid-shaped coil wound on a ferrite core. The instructions for winding the inductor are given in Steve's article. The 78S40 and inductor core and bobbins are available from MicroMint Inc., 917 Midway, Woodmere, NY 11598 for $11.50. The 25 kilohm potentiometer should be adjusted so that the output is exactly 21 volts. Some adjustment in component values (particularly the inductor) may be necessary to compensate for variations in component tolerances. An assembled and tested 5VDC-to-21VDC converter that can be mounted on an S-100 card is also available for $15 from Elpac Power Systems, 3131 S. Standard Ave., Santa Ana, CA 92705; (714) 479-4440.

If you have a 24-volt DC source available (e.g., disk drive power supply) then you can derive the 21 volts from it, using the circuit that is shown in Figure 3.

The remainder of the circuit consists of an address decoder (74LS30) to put the base address of the E²PROM at E000 hex (a good place in a North Star system), the read/write control circuit, and data in/out control. If more than one 2817 is used, then buffers should be used on address lines A0-A10 to minimize loading on the S-100 address bus.

I do not claim that this is the optimum implementation for this circuit. I designed it this way to use parts that I had readily available. In fact, one should be able to build this interface with fewer ICs, using the interface circuits shown in the book by Sol Libes and Mark Garetz entitled *Interfacing To S-100/IEEE-696 Microcomputers*, published by Osborne/McGraw-Hill.

Also, instead of connecting the READY/BUSY pin of the 2817 to the S-100 RDY line, you can connect it to an interrupt line and write an appropriate interrupt routine to use time better when the 2817 is writing.

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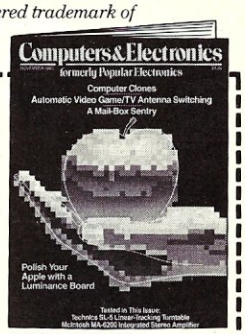

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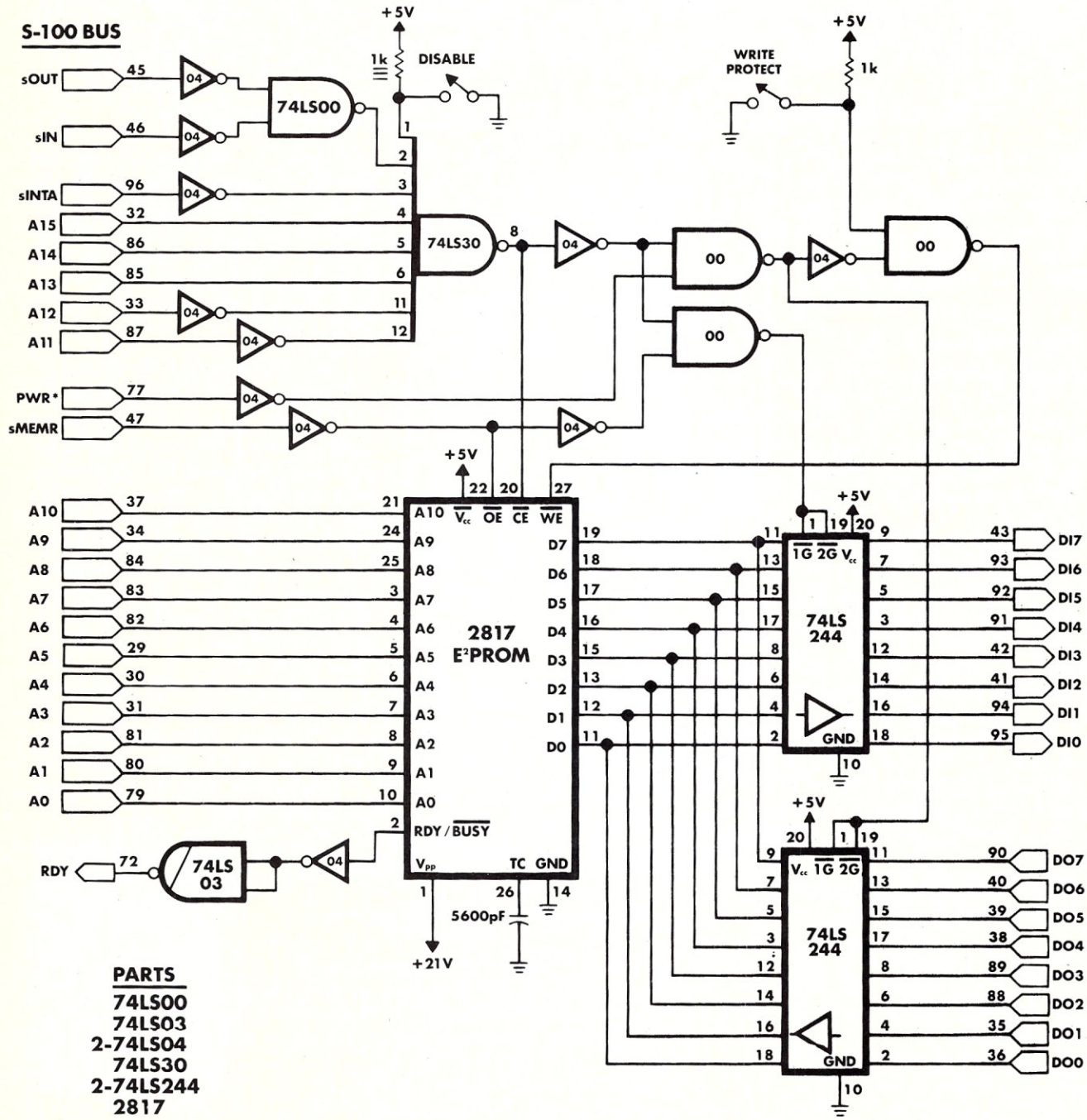

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Figure 1. S-100 E²PROM board circuit

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Utilities: Text file compression/expansion, TRSDOS to CP/M text file conversion, Line Numbered Text Editor, MFT for single drive systems	**Utilities:** None
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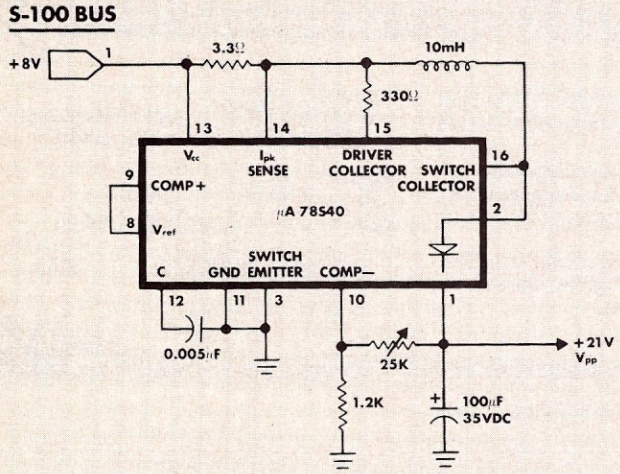

Figure 2. +8V to +21V step-up regulator circuit

Conclusion

An E²PROM opens up tremendous opportunities. I use my E²PROM to hold my monitor communications program. I like to have this program immediately available, since I use it so often. Also, I am still fine-tuning the program and adding features. Thus, the E²PROM is ideal for this application. If you come up with other interesting uses for

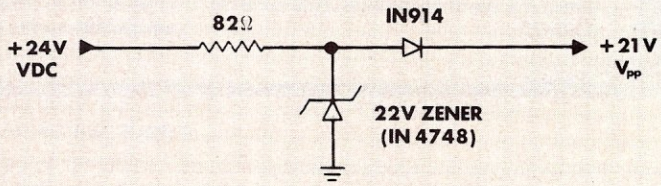

Figure 3. Voltage step-down circuit

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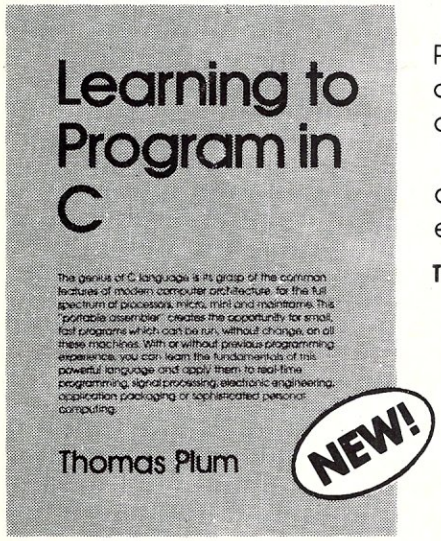

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CIRCLE 77 ON READER SERVICE CARD

E²PROM continued . . .

the circuit, or circuit improvements, please let us know about them.

THE NEW 2817A E²PROM

As this issue of *Microsystems* was being typeset, we learned that Intel plans to introduce, late this year, an improved version of the 2817 E²PROM, to be called the 2817A. It will do away with much of the circuitry shown in this article and make interfacing much simpler.

First, the 2817A will operate from a single +5V power source. This will be accomplished by an internal +5V-to-+21V pump and regulator circuit. Therefore the circuits shown in Figures 2 and 3 will no longer be needed.

Second, an open drain output stage on the RDY/BSY line will be used so that this pin can be tied directly to the S-100 busy RDY line.

Third, the RDY/BSY line will be relocated from pin 2 to pin 1 with address bit 12 on pin 2. This will make the pinout compatible with 64K E²PROMs.

Lastly, the 2817A will not require the timing capacitor previously required between pin 26 and ground.

This will make the 2817A a very cost-effective substitute for CMOS with battery backup where nonvolatile memory is required.

—Sol Libes, editor

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6.000,	6.144,	6.400,	6.5536,	7.000	2.00 each
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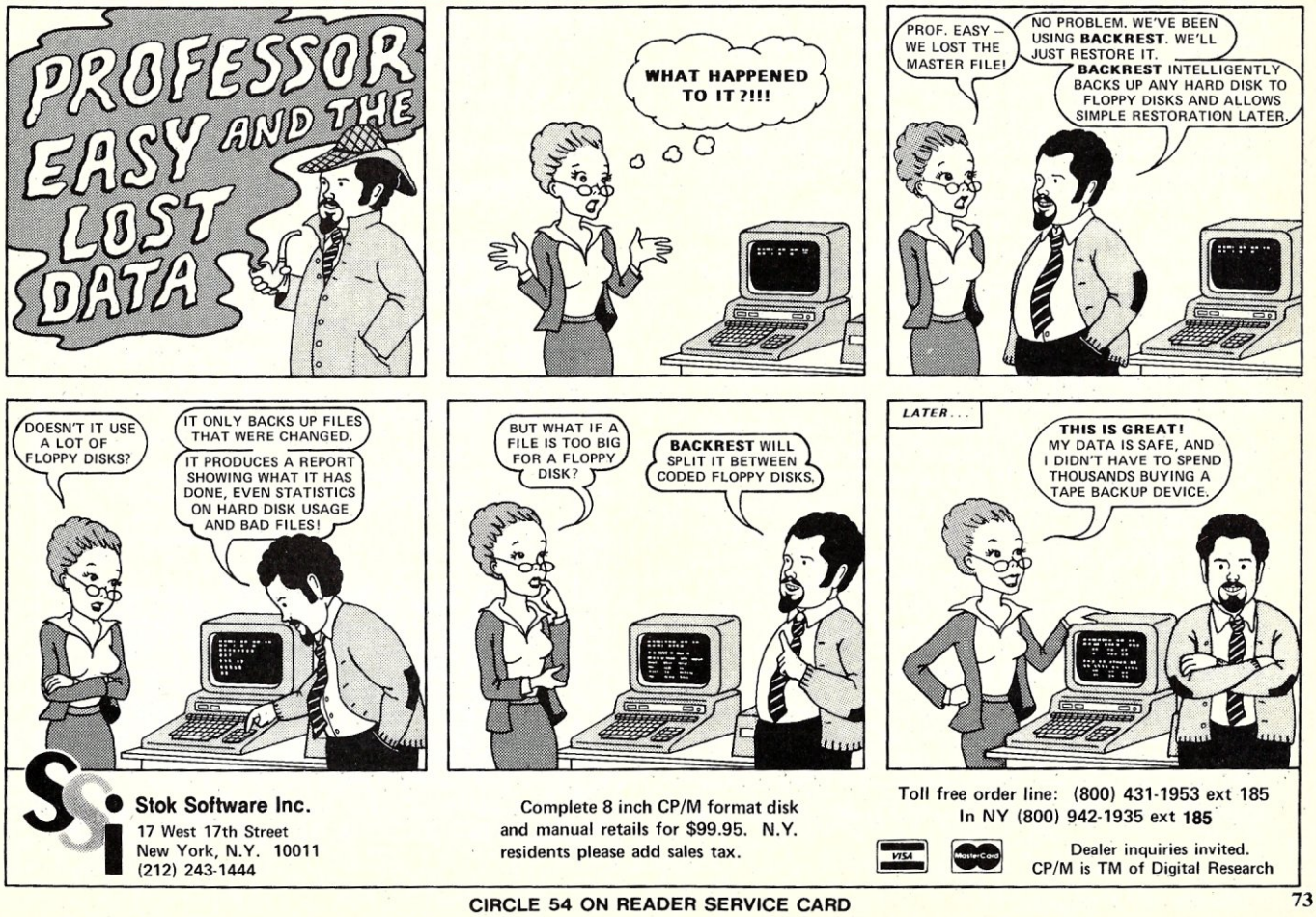

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CIRCLE 54 ON READER SERVICE CARD

Four SBCs Reviewed

A close look at the Advanced Digital Super Quad, Intercontinental Micro Systems CPZ-48000, Teletek SysteMaster, and Sierra Data Sciences SBC-100

by David Hardy

This is a review of four of the most popular S-100 single-board computers currently in production. All four are 64K S-100 "system masters" with on-board RAM, I/O, and floppy disk controllers. Each board is capable of running, without any other boards, as a complete stand-alone CP/M-based S-100 machine. Just add a frame, drives, and a terminal, and you are up and running.

In addition, all of the boards can meet the new IEEE-696/S-100 Standard specs (with certain qualifications—see below), so they can be used with most boards available for S-100 machines.

Although this review is primarily intended to compare the hardware features of each board, the "stock" CP/M software offered with each machine will also be examined. This is necessary because even the most advanced hardware is completely useless without functional software. I have seen many CP/M systems with superior hardware forced to sit idle because of improperly implemented BIOSs. One of the machines I use at work was delivered with a CP/M operating system that wasn't even able to warm-boot! When I asked the programmer who wrote the BIOS for it why the machine would cold-boot whenever it was supposed to warm-boot, he told me that the warm-boot feature was "an option" that Digital Research had never really intended to be used! None of the boards reviewed here has such terrible problems, but I have found some irregularities in each that I feel should be mentioned in order to make the reader aware of any possible problems that might arise in an actual installation.

Although installation was not difficult, none of these boards can really be thought of as an "out-of-the-box" plug-in. Bringing up each board involved several things that the novice probably would not plan for, not to mention installation of the usual I/O cables, etc.

All the boards were tested with 8" double-sided Shugart drives (the "standard" drive by which all others are referenced in the documentation).

A complete discussion of each of these boards could fill an entire book. In fact, I could spend several pages just discussing the hardware features of each board. Fortunately, the boards all have several basic things in common that should be discussed before covering each board separately.

What the boards have in common

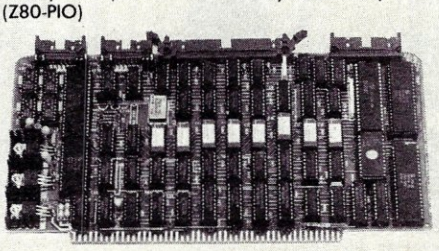
- All of the boards are IEEE-696/S-100 compatible. Well, almost. Certain minor exceptions are listed in each manual, and each manufacturer is, of course, free to use the NDEF lines of the IEEE-696 bus for whatever special purposes he wants.
- All of the boards require forced-air cooling, which is already provided in most S-100 frames. Because of the great number of ICs mounted on each board, these boards all run rather hot and could overheat without proper air flow.
- All of the boards contain circuitry for the following five functions:
  —CPU (Z80)
  —I/O (SIO)
  —Counter/timer (CTC or 8253)
  —64K memory
  —Disk control
- All of the boards use dynamic read/write memory. In fact, all use 64K bit 4164s ICs or equivalent, which is ok, unless you are planning to use your computer on a trip to outer space.
- All of the boards contain on-board EPROM that can be switched off under program control and replaced by on-board RAM (phantomed).
- All of the boards can run MP/M and Turbodos, as well as CP/M.
- All of the boards can function as a bus master as defined by the IEEE-696 rules.
- None of the boards functions as a "slave."
- All of the boards cost about $1000 each.
- All of the boards (when bought with CP/M) are provided with the usual standard CP/M documentation and programs from Digital Research.

Individual descriptions

The Advanced Digital Super Quad board

The Super Quad's advertised features:

- Z80A @ 4MHz
- 1793 floppy disk controller
- 64K dynamic memory (4164), switchable in 16K banks
- 2K or 4K EPROM (2716 or 2732), switchable
- 2 serial ports (Z80-DART or SIO)
- 2 12-bit parallel ports (Z80-PIO)
- Real-time interrupt clock (Z80-CTC)
- S-100 extended addressing (A16-A23)
- Allows *external* DMA devices
- RAMDISK drive option
- CP/M, MP/M, and TurboDos available
- One-year warranty



David Hardy, 736 Notre Dame, Grosse Point, MI 48230

The Super Quad is delivered with a two-manual set: one that covers the Super Quad board and hardware, and another that covers its CP/M implementation. The documentation also includes complete schematics. The supplied CP/M disk contains the source for a CP/M BIOS and loader, a FORMAT program, and a MODEM program (actually a modified MODEM7.ASM from the CPMUG), and the usual programs seen on a CP/M disk (PIP, STAT, etc.). The BIOS requires Microsoft's M80 (a recent version) to assemble. Source for the on-board PROM is available on request. The disk also contains several DOC files for use in system modification, installation, and certain specific hardware applications.

The serial and parallel ports each require a small interface board about 2″ square (called PS NET) in order to talk to the real world. For example, the PS NET board for the serial port contains RS-232 line drivers and receivers that are necessary to connect the serial port to most serial terminals. RS-422 and -499 PS NET boards are also available. The port driver circuitry is built on these small boards to allow the end-user additional interfacing flexibility. Different serial or parallel interface modules can be used by just changing the PS NET boards to suit your requirements. Although the board is very densely packed with ICs, four additional "empty" sockets are provided for user additions or modifications.

The manual is about 150 pages long and includes sections on basic operation, hardware configuration, setting up different disk drives (an absolute *must*), some theory of the board's operation, and several appendices of the various ICs used on the board such as monitoring error codes, application notes, and "recommended additional" S-100 boards.

The Super Quad "comes up" in an EPROM monitor. This is a nice feature when the board is first brought up, since it allows the system to run without any floppy drives connected, and makes it easy to verify that the terminal is properly connected. A new monitor EPROM, now available, can AUTO-BOOT, so the monitor feature can be disabled, if desired. The monitor can be a handy feature for a hacker or system troubleshooting, but makes turnkey operation a bit clumsy. The monitor resides in memory from 0F000H to 0FFFFH and can be easily switched out with a simple output instruction. When the monitor is switched out, RAM is restored, so when you turn off the ROM, you have the full 64K of read/write memory available.

Although two of the four boards reviewed here have the ability to perform DMA operations to the on-board RAM via DMA controllers, the Super Quad is the only board that is able to perform true DMA to external devices (i.e., to other S-100 boards). The board makes use of most of the ports from 0 to 20H, and allows additional boards to use the remaining ports without restriction.

The Super Quad can use either 8″ or 5¼″ drives, although only one size at a time. You have

Table 1. Board Ratings

Item	ADC	ICM	Sierra	Teletek
Documentation	G	G	G	G
Board quality (construction, etc.)	E	E	E	E
Requires external expansion boards	Yes	Yes	No	No
Software quality	G	E	G	G
Source listings supplied	Yes	Yes	Yes	Yes
Circuit diagrams supplied	Yes	ND	Yes	Yes
Ease of installation	G	G	G	G
IEEE-696 compatible	Yes	Yes	Yes	Yes
Can be IEEE-696 bus master?	Yes	Yes	Yes	Yes
Can be IEEE-696 bus slave?	No	No	No	No
Overall speed *(See note 5)*	G	G	G	G
Forced-air cooling required?	Yes	Yes	Yes	Yes
Drive steppers enabled always?	No	No	Yes	Yes
Switched on-board PROM	Yes	Yes	Yes	Yes
Extended memory addressing (A16-A23)	Yes	Yes *(1)*	Yes	No *(3)*
Allows DMA to other S-100 boards	Yes	Yes *(2)*	No	Yes *(4)*
Timer/counter	CTC	8253	CTC	CTC
DMA controller	No	9517A	No	Z80-DMA
Processing benchmark time (sec):	11:13	11:00	11:08	11:02
Disk I/O benchmark time (sec):	5.7	7.0	10.1	6.0
Suggested list price	$ 875	1025	895	895

E = Excellent, G = Good, F = Fair, P = Poor, VP = Very Poor
ND = Requires nondisclosure agreement

1. *Also allows dynamic memory addressing*
2. *Allows DMA via 9517A DMA controller*
3. *Uses bank-switching via I/O ports, instead of extended addressing*
4. *Allows DMA via Z80-DMA controller*
5. *Overall speed is a hybrid evaluation, based on I/O speed and efficiency, processor speed and efficiency, and software efficiency.*

to set jumpers on the board to select whichever size drive you choose, so changing from one size to the other frequently would be difficult.

Bringing up the board is simple enough:

- Read the manual
- Configure the board (set the jumpers for your drives and a few other misc. things)
- Connect the terminal and set its speed
- Connect the drives
- Plug in the board
- Power on

Because the board comes up running the internal monitor, you will immediately see if the board and terminal are working. (If you don't connect the drives, the board will start up in a resident EPROM monitor. If you do, it will just ask you to insert a system disk into the A drive.) Then insert the disk into drive A, and CP/M should load.

That's all straightforward and simple. Setting the jumpers would be the hardest part, although it is clearly explained in the manual.

When I first received this board, the hardware and software were in dire need of improvement. There was a minor hardware problem that kept the "current" CP/M drive *always* selected, and the software had several terrible bugs, including an implementation of CP/M that didn't warm-boot properly, didn't trap BDOS errors, and had several other rather terrible problems. Happily, the software and documentation have since been much improved and these problems have been eliminated. In the new versions, the BDOS error trapping and DPBs have been repaired, and 1024-byte sector size has been added. In addition, the warm-boot problem has been corrected, making the CP/M implementation quite good, if a bit unusual.

The unusual parts involve the use of a ROM-based CCP that is actually based on ZCPR 1.0 (the public-domain Z80-based CCP replacement) and that is simply moved into place at each warm-boot; the use of only a single system track (to hold just a small cold-boot loader); and the "relocation" of the CP/M system from the system tracks into a file called CPM.SYS (shades of CP/M Plus!).

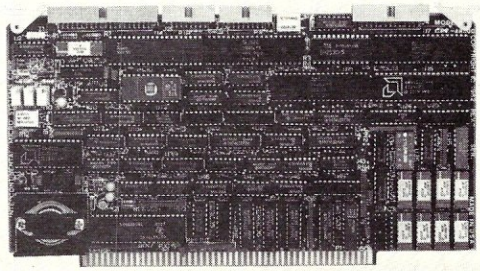
Some notes on the CP/M system provided with the Super Quad:

- *61K system size, TPA is OD700H bytes*
- *1024-byte sectors, 2K blocks*
- *Drives are stepped (initially) at 3 ms*
- *Only 1 system track required*
- *BDOS errors are displayed, but not trapped in the BIOS*
- *CCP (ZCPR) loaded from EPROM at warm-boot*

The Intercontinental Micro Systems Corp. CPZ-48000 board

The CPZ-48000's advertised features:

- IEEE S-100 bus compliance
- Z80A @ 4MHz
- 1793 floppy disk controller in DMA, interrupt, or programmed I/O mode
- 2 serial I/O channels (one programmable in DMA, interrupt, or programmed I/O)
- 2 parallel I/O channels (programmable as above)
- 4-channel DMA controller
- 64K dynamic RAM (4164) with programmable memory deselect of 4-64K
- Extended addressing (A16-A23)
- 8 vectored priority interrupts
- 2K or 4K EPROM on-board, switchable
- Software-selectable baud rates
- Real-time clock
- Z80A SIO
- CP/M, TurboDos, and MP/M available
- Turbo-Disk implementation included
- One-year warranty



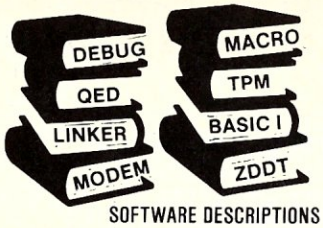
The CPZ-48000 is delivered with a manual of about 60 pages. The manual clearly introduces and explains the CPZ-48000, and explains its operation, options, and implementation. Although the manual can be somewhat intimidating due to its "typewritten" appearance, it is well indexed and easy to reference. Like all manuals, it should be read cover to cover before attempting to bring up the board that it describes.

The CP/M disk provided with the board contains the usual CP/M files: PIP, STAT, etc. Furnished source files include the boot loader, SYSGEN, FORMAT, and BIOS, as well as several disk copy and test utilities. The BIOS is particularly well implemented, and the source file is easy to modify and understand.

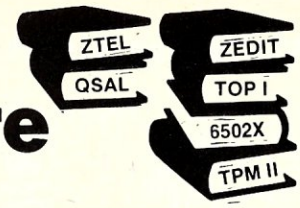
The BIOS includes one very interesting feature called Turbo-Disk (no relation to TurboDos, the operating system). This feature allows a block of RAM memory to be treated as a disk, complete with directory, etc. The result (if you have the RAM) is a lightning-fast drive that comes in real handy for those S-L-O-W linkers and compilers. The Turbo-Disk drivers are included in the BIOS source, which means they are easy to implement, and even easier to figure out.

Like the Super Quad, the CPZ-48000 requires

Although installation is not difficult, none of these boards can really be thought of as an "out-of-the-box" plug-in. Bringing up each board involves things the novice might not plan for.



Z80 Software



SOFTWARE DESCRIPTIONS

TPM (TPM I) - $80 A Z80 only operating system which is capable of running CP/M programs. Includes many features not found in CP/M such as independent disk directory partitioning for up to 255 user partitions, space, time and version commands, date and time, create FCB, chain program, direct disk I/O, abbreviated commands and more! Available for North Star (either single or double density), TRS—80 Model I (offset 4200H) or II, Versafloppy I, Tarbell I, or Osborne I.

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This package is only for the TRS-80 Model I. Note: These are the ONLY CDL programs available for the Model I. It includes: TPM I ($80), BUSINESS BASIC ($200), MACRO I ($80), DEBUG I ($80), ZDDT ($40), ZTEL ($80), TOP I ($80) and MODEM ($40)
$680 Value NOW $680

MODEL II PROGRAMMER

This package is only for the TRS-80 Model II. It includes: TPM-II ($125), BUSINESS BASIC ($200), MACRO II ($100), MACRO III ($150), LINKER ($80), DEBUG I ($80), DEBUG II ($100), QED ($150), ZTEL ($80), TOP II ($100), ZDDT ($40), ZAPPLE SOURCE ($80), MODEM ($40), MODEM SOURCE ($40) and DISASSEMBLER ($80)
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MACRO I - $80. A Z80/8080 assembler which uses CDL/TDL mnemonics. Handles MACROs and generates relocateable code. Includes 14 conditionals, 16 listing controls, 54 pseudo-ops, 11 arithmetic/logical ops, local and global symbols, linkable module generation, and more!

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MACRO III - $150. An enchanced version of Macro II. Internal buffers have been increased to achieve a significant improvement in speed of assembly. Additional features include line numbers, cross reference, compressed PRN files, form feeds, page parity, additional pseudo-ops, internal setting of time and date, and expanded assembly-time data entry.

6502X - $150. A 6502 cross assembler. Runs on the Z80 but assembles 6502 instructions into 6502 object code! Similar features as our Macro assemblers.

DEVELOPER I

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$440 Value NOW $150

DEVELOPER II

Includes: MACRO II ($100), MACRO III ($150), LINKER ($80), DEBUG I ($80), DEBUG II ($100), BUSINESS BASIC ($200), QED ($150), TOP II ($100), ZDDT ($40), ZAPPLE SOURCE ($80), MODEM SOURCE ($40) and DISASSEMBLER ($80) ZTEL (80)
$1280 Value NOW $350

DEVELOPER III

Includes: QSAL ($200), QED ($150), BUSINESS BASIC ($200), ZTEL ($80) and TOP II ($100)
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COMBO

Includes: DEVELOPER II ($1280), ACCOUNTING PACKAGE ($300), QSAL ($200) and 6502X ($150)
$1930 Value NOW $500

LINKER - $80. A linking loader for handling the linkable modules created by the above assemblers.

DEBUG I - $80. A tool for debugging Z80 or 8080 code. Disassembles to CDL/TDL mnemonics compatible with above assemblers. Traces code even through ROM. Commands include Calculate, Display, Examine, Fill, Goto, List, Mode, Open File, Put, Set Wait, Trace, and Search.

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ZTEL - $80. An extensive text editing language and editor modelled after DEC's TECO.

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8DD	8" Double Density (256 bytes/26 sectors/77 tracks)
8XD	8" CDL Extended Density (1024 bytes/8 sector/77 traceks = 616K)
5SD	5.25" Single Density (TRS80 Model I, Versafloppy I, Tarbell I)
5EP	5.25" Epson Double Density
5PC	5.25" IBM PC Double Density
5XE	5.25" Xerox 820 Single Density
5OS	5.25" Osborne Single Density
5ZA	5.25" Z80 Apple (Softcard compatible)

TPM INFO When ordering TPM I or II, in addition to Disk Format, please specify one of the following codes:

	CODE	DESCRIPTION
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	NSSD/Z	North Star Single Density for Zapple I/O
	NSDD/H	North Star Double Density for Horizon I/O
	NSDD/Z	North Star Double Density for Zapple I/O
	TRS80-I	TRS-80 Model I (4200H Offset)
	TRS80II	TRS-80 Model II
	VI8	Versafloppy I 8"
	VI5	Versafloppy I 5.25"
TPM-II:	VII8	Versafloppy II 8" (XD)
	VII5	Versafloppy II 5.25"
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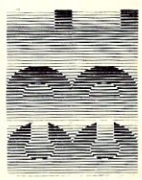

Computer Design Labs

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CIRCLE 84 ON READER SERVICE CARD

small interface boards to expand its on-board functions, like serial and parallel I/O. Unlike the Super Quad, the CPZ-48000 also requires a small interface board to interface to its disk drives. Again, these boards (called personality boards here) are required because all of the ICs necessary to do the job just won't fit on a single S-100 board. There is a distinct advantage here, however, in using an external interface board for the disk drives. By just changing the interface board, the CPZ-48000 can be made to work with both floppy and hard disks.

The CPZ-48000 is the most hardware-advanced board of the four reviewed here. Besides the usual Z80, SIO, PIO, 64K RAM, etc. the CPZ-48000 contains an AM9517A 4-channel DMA controller, an AM9519A UIC (Universal Interrupt Controller), an 8253 timer/counter (sorry, no CTCs), and a 74LS610 MMU (Memory Management Unit). The 8253 is used up supplying the SIO and the UIC; however, so is not of much external use. One of the four DMA channels is used to allow temporary bus masters to "capture" the bus for DMA transfers to off-board memory. A true software/hardware systems programmer would be in Nirvana programming this board. Block memory moves can be done without the Z80, and three times faster than the LDIR instruction; and truly dynamic memory addressing can be done via the 74LS610 MMU.

Booting the CP/M system is the same as starting up the Super Quad, except the baud rate of the user's terminal is determined dynamically by having the user hit returns until the computer can "sense" the terminal's baud rate. Once safely into the monitor, the disk is booted by typing the "B" command (for Boot, what else?).

OK, so much for the good stuff. Here are my complaints. Circuit diagrams are not supplied with the board. You have to sign a nondisclosure agreement to get them. This would not be too much of a problem, except that there is very little information included with the package about how to configure your disk drives to work. The only drive configuration information included is one page for Qume DataTrack 8 drive. In all fairness, however, I should mention that ICM only sells its boards through its dealers and factory-direct, and that factory assistance is provided for system configuration, including setting up various brands of drives.

Another complaint (albeit small) is that all the goodies on the board (DMA controller, Interrupt controller, etc.) take up the top 128 ports! You can't have everything, I guess.

The CP/M implementation is very good. Although the BIOS displays disk errors, it does not trap them, and allows them to properly return back to the BDOS. The BIOS will allow both single-density, single-sided disks and double-density, double-sided disks at the same time. Also nice is the "type-ahead" feature provided by the interrupt-driven BIOS.

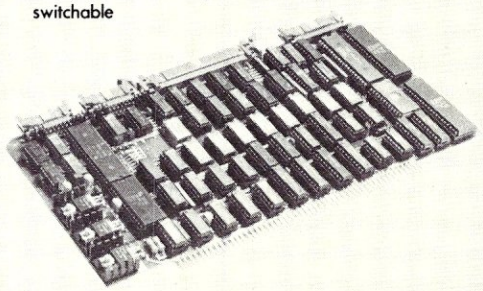
Some notes on the CP/M system provided:

- *63K system size, TPA is 0DF00H bytes*
- *Drives are stepped (initially) at 3 ms*
- *Uses 4K blocks, 512-byte sectors only for double-density*
- *BDOS errors displayed, but properly returned*
- *CP/M system will not fit on a single-density disk*

The Sierra Data Sciences SBC-100 board

The SBC-100's advertised features:

Z80A @ 4MHz
2 serial ports (Z80 DART, SIO is optional)
2 parallel ports (Z80 PIO)
765 floppy disk controller
64K dynamic RAM (6664)
On-board 2732 EPROM, switchable
Optional "Intelligent Winchester Interface" available
IEEE-696 compatible
CP/M, MP/M and TurboDos available



The SBC-100 is delivered with about 100 pages of documentation consisting of two separate manuals in loose-leaf binders. The first (the Product Description Manual) contains an introduction to the SBC-100, describes its hardware characteristics and options, tells how to set up many popular floppy disk drives for the SBC-100, and has an appendix of engineering notices and application notes. The second manual is furnished with the Sierra implementation of CP/M. It includes rather complete step-by-step instructions on bringing up the SBC-100 the "first time," and explains the operation of the several unique utilities provided (including a very nice system configuration program called GENMOD). Also included is a section that tells you *exactly* how to set up your terminals and printers for the SBC-100. This last section is only two pages long, but could easily save the first-time implementor a couple of hours of set-up time.

In addition to the manuals provided with the SBC-100 and its CP/M implementation, a technical manual is available separately that describes

The Super Quad is the only one of the boards reviewed here able to perform true DMA to external devices.

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the SBC-100 and CP/M in greater detail.

The CP/M disk provided by Sierra contains the usual CP/M utilities, BIOS source, an enhanced version of SYSGEN, a format utility, a copy utility, and a program called GENMOD (no relation to MP/M's GENMOD) that permits dynamic changes to several system parameters, such as disk step rate, baud rates, head unload time, drive motor delay, etc.

The source for the monitor program (the EPROM, that is) is also available if you want to sign a nondisclosure form. I would recommend it, since the disk I/O is performed by calls to the EPROM. In addition, source for *all* utilities is also available once the nondisclosure agreement is signed. The source files require DRI's MAC assembler, and (of course) contain Z80 code.

Also included with the SBC-100 is a serial cable that plugs into the board and provides a DB-25 connector that connects to a regular RS-232 data cable: You don't have to buy a special cable to connect your terminal to the SBC-100. No small "personality" or interface boards are required for normal serial, parallel, or disk I/O.

The SBC-100 contains two real-time clocks that are used to generate interrupts at 1-second and 8-millisecond intervals for use by the time-of-day clock, and the system software. Also, the SBC-100 uses ports 80H through 9FH. All other ports are available for user-desired functions.

Booting is fairly simple. After all the hardware is connected, just plug the disk into A: drive, and press reset. The system will sign on, then drop into the "A>" if all is well. If not, well. . . .

All of my complaints about this board are fairly trivial. Although the 765 controller's annoying habit of loading and unloading the drives' heads like a machine gun has been solved in software, the equally annoying characteristic that requires the drives' stepper motors to be constantly enabled has not. This means that some drives (most kinds with "lead-screw" type stepper motors) will run *very* hot. Forced-air ventilation for the drives is a *must*.

The supplied CP/M BIOS traps errors directly to the console and allows a graceful exit via the BDOS, or a cold-boot or retry. This technique is ok for local use, but could be a problem for running some disk diagnostic programs, or for running via a remote "BYE" program. Of course, because the BIOS source is available, the BIOS error trapping can be removed.

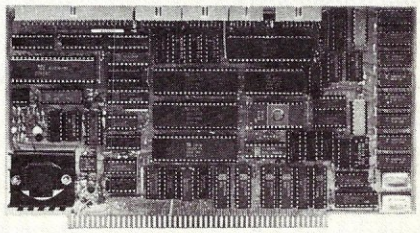
Some notes on the CP/M system provided:

- *61K CP/M; TPA is 0D700H bytes*
- *2K or 4K block size under double-density*
- *Has 256-, 512-, and 1024-byte sector sizes*
- *Drive step rate is initially 8 ms*
- *BDOS errors trapped locally in BIOS*
- *All system tracks are single-density*
- *System will fit on a single-density disk*
- *Time-of-day clock utility*

The Teletek SysteMaster board

The SysteMaster's advertised features:

- Z80A @ 4MHz
- IEEE-696 compatible
- 2K to 8K of 2716/2732/2764 EPROM, switchable
- 2 serial ports (Z80A SIO)
- 2 parallel ports (Z80A PIO)
- Counter/timer (Z80A CTC)
- Z80 mode 2 interrupt driven, also supports S-100 vectored interrupts
- 765 floppy disk controller
- 64K dynamic RAM (4164)
- Bank-switching supported via I/O ports
- Z80 DMA controller for floppy I/O; also user-programmable
- CP/M, MP/M, TurboDos, and MDZOS supported
- RAM drive option available
- One-year warranty



The SysteMaster is delivered with a manual of about 80 pages or so. Although the manual is a bit confusing, it is complete. It contains a complete appendix of set-up information for various floppy drives. The many jumper options are thoroughly discussed, and there is a 12-page theory of operation. The manual gives the necessary information to bring the board up under CP/M; however, the step-by-step start-up procedure is given in a supplemental CP/M manual. A very complete set of set-up specifications is given for more than a dozen different makes of floppy drives, and information on setting up and using additional memory boards is also included. Complete circuit diagrams for the SysteMaster are also included.

The 10-page manual supplement that is included with the CP/M diskette describes the function and operation of each of the utility programs, and tells how to modify or customize the CP/M system. The supplement also explains the BIOS's error codes and details the use of the debugger/monitor program.

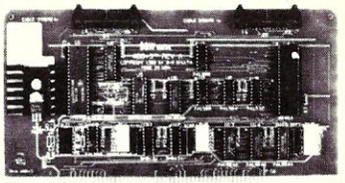
The CP/M disk provided by Teletek contains all of the standard CP/M programs and also includes source files for all of the furnished utilities, source for the CP/M BIOS, source for the on-board EPROM, and even source for a debugger/monitor. A system configuration program (called CONSYS) is also provided (with source, of course) if you like to avoid generating a new system every time you want to change some system defaults or values. The BIOS source is provided in several small modules.

M80 and L80 are required to assemble any of

Teletek's approach to end-user flexibility is to offer additional features on separate S-100 boards.

THE 488+3 IEEE 488 TO S-100 INTERFACE

IEEE-488



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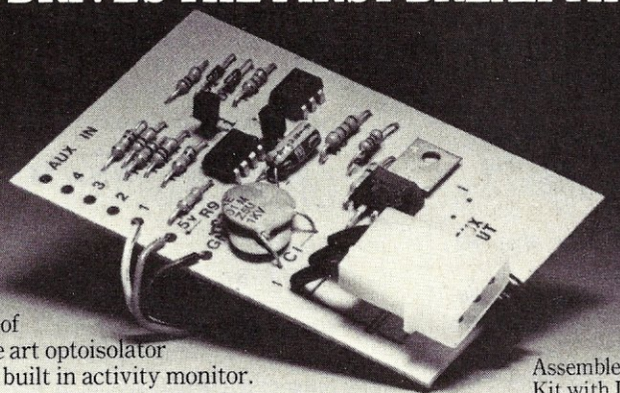

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CIRCLE 155 ON READER SERVICE CARD

the source files. All serial and parallel ports are fully implemented on the board, so no additional interface boards are required. The SysteMaster uses most of the ports from 0 to 1FH.

Bringing up the SysteMaster involved a bit more work than the other boards, due to the many options that needed to be set. The SysteMaster is able to *simultaneously* run 8" and 5¼" drives, and has jumpers to select the various write compensation values required for both size drives. The board also has an option to allow extending the 765 floppy controller's normally short head unload delay from 240 ms to any value up to about 10 seconds, which will eliminate the machine-gun style rapid head load/unload during frequent disk I/O. Options are also included to select wait states, CTC rates, EPROM address and type, and RAM addressing.

Unlike Intercontinental Micro System or Advanced Digital, Teletek's approach to end-user flexibility is to offer additional features on separate S-100 boards. Additional boards available now include a hard-disk controller, a slave processor board, a 256K dynamic RAM board, an I/O board called PSIO with 4 serial ports (2 SIOs), 2 parallel ports (PIO), and a CTC; and "personality" boards to convert a parallel port to serial RS-232 or RS-422.

Again, my complaints about this board are small. The IOBYTE is only implemented for the list device; however, the CONSYS program allows physical device assignments to be changed just as easily. Since BIOS source is provided, the IOBYTE could also be easily implemented. No off-board DMA can be performed, although DMA can be performed via the on-board Z80-DMA controller. The BIOS also traps disk errors, which could create some problems with "universal" programs or remote "BYE" use, as I mentioned before. A special adapter board is required to connect 5¼" drives and 8" drives, although I can see no way to avoid it. The PC board has no legends or silk screening, which makes it rather difficult to locate all of the jumpers, although a board layout is provided in the manual.

Some notes on the CP/M system provided:

- *64K system; TPA is 0D900H bytes long*
- *Traps BDOS errors in the BIOS, but allows proper return*
- *Excellent TYPE-AHEAD ability due to interrupt-driven I/O*
- *Automatic baud rate sense at power-up (i.e., type returns), or baud rate can be preset with CONSYS utility*
- *256-, 512-, and 1024-byte sector sizes available.*

Conclusion

Although a lot of what I have said here has come straight from each manufacturer's manual, I have actually "brought up" and tested each of the four boards reviewed here.

The benchmark tests performed to measure processing speed and load time were by no means exhaustive. The intent was to measure the relative performance of the four boards, not to measure the absolute performance of each board. In addition, all of the boards were tested under the same conditions, using the same frame, drives, and power supplies. No attempt was made to test any of the boards using 5¼" drives.

The frame and test apparatus were all provided by CDP Corp. The Super Quad board was provided by Ken Jackson of Micro Business Systems in Livonia, MI. The CPZ-48000 was provided by Del Helmuth of Micro-Ade Co. The SBC-100 board was provided by Sierra Data Sciences, Inc. The SysteMaster was provided by Teletek Enterprises, Inc. I would like to thank all of these people for their assistance.

Most of the items listed in the "complaints" sections are minor, and would be of little consequence in most word-processing (or similar) situations. Alternatively, many of these items could have a great effect on a system's operation in a software or hardware development environment. I hope that mentioning them is of some use. No doubt, some of the complaints are due to my own personal preferences or prejudices. Bear in mind, also, that all four of these boards are being constantly upgraded by their manufacturers.

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The CPZ-48000 is the most hardware-advanced board of the four reviewed here. A true hardware/software systems programmer would be in Nirvana programming this board.

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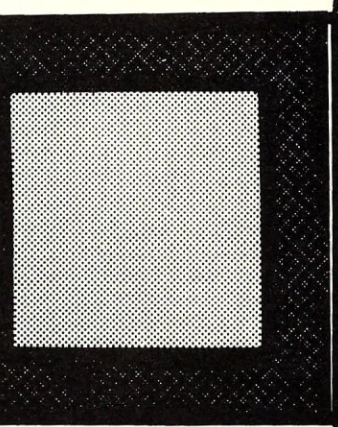

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MICROSYSTEMS TESTS THE:

Morrow Designs Micro Decision

by Bill Machrone

Morrow Designs, headed by George Morrow, is one of the pioneering companies in microcomputers. They are relatively unusual in that they are not only still a viable company today, but have also continued to innovate and lead the industry. The Micro Decision is their latest product, and it breaks new ground, both for Morrow and the computer industry. Unlike their former products, it is not based on the S-100 bus. It is a single-user single-board computer with integrated disk drives and a pair of serial ports.

Overview

The Micro Decision is a marketing-driven machine, not a technology-driven machine. That means that new ground is broken only in price and software features, not hardware or new technology. This is not to say that the unit is not well engineered. The objective of the Micro Decision is to bring CP/M-style computing into a lower price range than has previously been available. In order to accomplish this, they have done some nice design and packaging work.

For $1,790, you get one drive (for $2,140, two drives), 64K of memory, a terminal and a keyboard. A hallmark of CP/M-based systems is the RS-232-based terminal instead of an integral video display and keyboard. This immediately identifies the Micro Decision as more of a "business" machine than a "game" machine. The other determining factor in calling this a "business" machine is the software that comes with it. Seven packages are included: WordStar, Microsoft Basic, BaZic, Logicalc, Correct-It, Pilot, and Micro Menus.

Bill Machrone, P.O. Box 291, Fanwood, NJ 07023

Hardware

The Micro Decision is attractively packaged, using the same general design as the IBM Personal Computer. The drives are integrated into the cabinet, avoiding the "collection of boxes" syndrome common to Apple and Radio Shack products. The terminal and keyboard are the same shade of beige as the cabinet, with charcoal-grey accents. The terminal is actually a Lear-Siegler ADM-20, one of the models intended specifically for OEM applications. It is one of the key factors in the cost-effectiveness of the Micro Decision, since it costs only $595 separately. You can, in fact, buy the Micro Decision without it, which may not be a bad idea (see the section on performance later on).

Looking inside the sheet-steel cabinet, there is a small switching power supply off to one side. The two disk drives are two-thirds height single-sided models with filler panels to bring their front panels up to the normal bezel size. Thus, the designers had the option of making the case even lower, sim-

Figure 1. *Micro Decision system, general view*

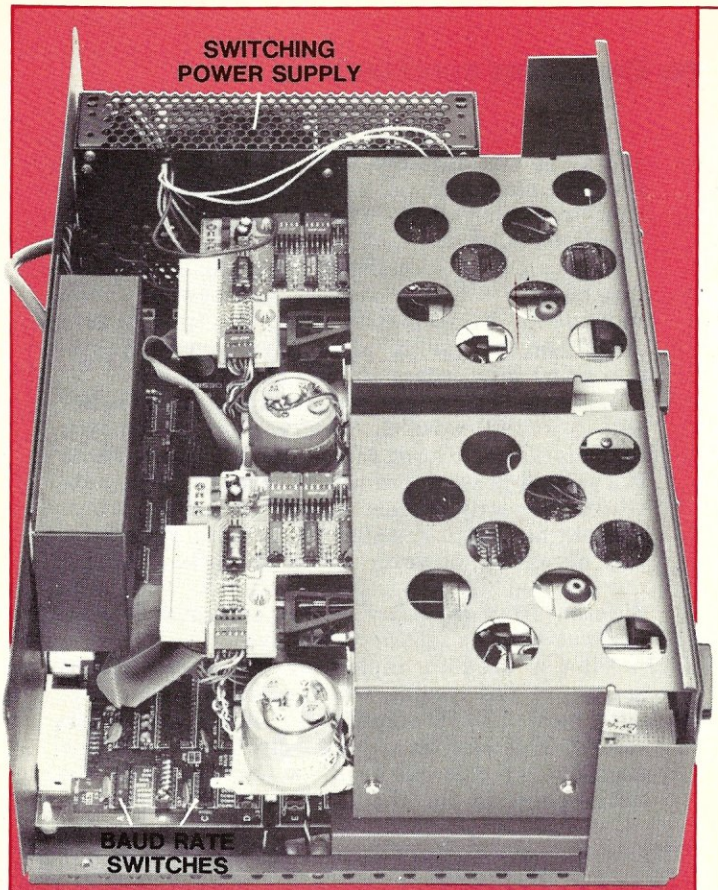


Figure 2. *Computer unit, interior layout*

ply by widening the box a bit and laying the switching supply on its side. You may be glad they didn't, because the availability of half-height drives means that you can fit four drives into this diminutive box. If this is your objective, you would do well to order the Micro Decision with only one disk drive. The drives, by the way, keep the head in contact with the disk surface the entire time the drive access lever is closed. This can be a little unsettling if you are used to drives that load and unload the head, but there is no additional disk wear once the drives stop rotating.

The single-board computer is at the base of the cabinet. Only chips such as the Z80, the bootstrap ROM, the disk controller, and the RAMs are socketed. The two serial ports are brought out on the back of the machine, with plastic female DB25 connectors that right-angle mount right to the circuit board. There are no cable anchor sockets for the screws normally found on RS-232 cables. There is also a card-edge protruding from the rear panel labelled "expansion drives."

The baud rates of the serial ports can be selected by clearly labeled DIP switches on the board, from 110 to 19,200 baud. Each port has a set of jumper pins to enable more advanced configuration, such as operation with a modem or a handshaking scheme other than that provided. The UARTs, by the way, are the popular Intel 8251As. The printer hardware handshaking method provided is keyed to the CTS line. I found this to be somewhat unusual, since DTR seems to be more of an emerging standard. Anyway, a combination of jumper pin changes and some judicious wire wrapping can get the Micro Decision to handshake with just about anything. Not to jump ahead into software, but one of the CP/M logical devices (LST:) supports X-ON/X-OFF handshaking.

The cabinet is convection-cooled, which is quite adequate for the minimal amount of heat generated. There isn't much else to say about the hardware side, other than that the power switch is located at the rear and there is a combined reset switch and pilot light on the lower right front corner. The pilot light is a necessity, since the machine runs dead quiet when the drives cycle off.

Software

CP/M 2.2 is provided with the Micro Decision. After spending a short amount of time with it, it is obvious that some good work went into the BIOS. It intercepts the usual "BDOS ERR ON d:" messages, gives a meaningful error message and says, for example:

Disk error on drive B: Drive not ready.

Type R to try again, A to Abort, I to Ignore.

The overall speed of the machine indicates that there is good work inside the BIOS in other areas as well, such as deblocking and disk access.

Another interesting feature is the Virtual Drive. No, it isn't a memory-resident disk, it's just another intelligent function of the BIOS. Here's how it works: If you ask for a drive that isn't really there (DIR C:, for example) the system tells you that it is reassigning drive A: to C: and to insert a diskette. It then performs the requested operation on

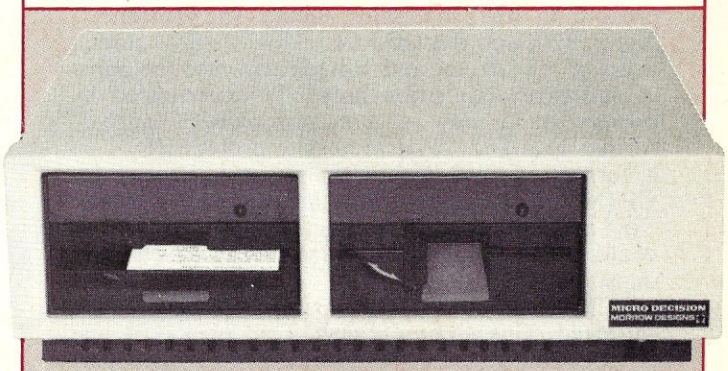


Figure 3. *Computer unit, front view. The sheet-steel cabinet is 16¾" wide, 5½" high, and 11⅜" deep.*

The Morrow Micro Decision is a good little computer. The amount of machine and software you get for the price is simply stunning. . . . It is unlike any other entry-level package offered to date.

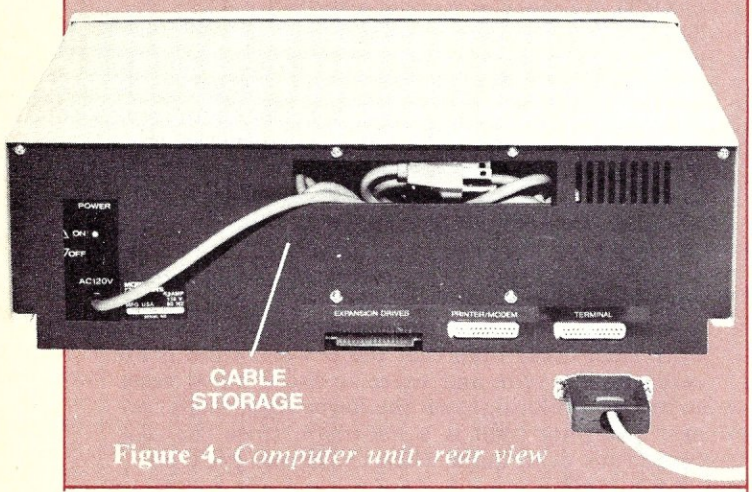


Figure 4. *Computer unit, rear view*

drive C:, even though it is physically in the A: drive. These operations can be reads or writes. After the operation is done, you simply put the original disk back in A: and all returns to normal. This can even be done inside application programs, including WordStar. It's a very handy way to retrieve a block of boilerplate text or an old letter from an archival disk for current editing without a lot of starting and stopping, PIPing and control-C'ing. There is a copy of the CBIOS on the distribution disk, and it makes interesting reading. Morrow doesn't provide any information on regenerating a modified CP/M, but this probably wouldn't be of interest to the typical purchaser of the Micro Decision, anyway.

Lots of utility programs come with the Micro Decision, including the usual disk formatting program. Most interesting are the disk compatibility programs that permit it to read minifloppies created on other machines, such as the Osborne 1, Xerox 820, and the IBM PC. This is a first among users of 5¼" drives and will greatly ease the pains of software acquisition normally experienced by owners of a new system. Morrow's "native" format uses 1024-byte sectors to provide 200K on a formatted disk. After the reserved tracks for CP/M are taken, the net storage space is 186K. This is pretty good for an inexpensive system, but could and should be upgraded to the new higher densities.

All the commercial packages performed as documented. This is not a review of the packages, just a collection of brief statements on how they perform on the Micro Decision. It is interesting and advantageous to have two Basic interpreters, as Microsoft's Basic-80 is the de facto industry standard, while BaZic gives the CP/M user access to the wholly different world of North Star Basic. It offers some unique advantages in channel-oriented I/O and file handling. You may not like its string handling conventions unless you grew up on a Hewlett-Packard.

Logicalc is a spreadsheet program of average capability. Its screen display is somewhat small, showing a 4-by-10 matrix at any one time. It runs quickly on the system, taking advantage of the system's fast disk access and 4MHz processor.

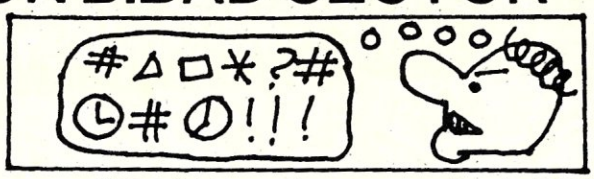
Correct-It is a spelling checker and corrector with a 36,000-word dictionary. It is of the type that marks each word that it doesn't know. There is a second-pass program that permits you to substitute correctly spelled words for marked words without having to re-enter the file with WordStar. It is necessary, however, to use WordStar again if the original file was column justified. This is no different from any other spelling corrector. I found Correct-It to be fast and effective.

Pilot is used to implement the Micro Menus feature of the system, which permits you to execute most CP/M commands from a menu-type screen. This can be a great help to the neophyte user, but is ponderous for the experienced user. No documentation for the pilot interpreter was in-

Figure 5. *Documentation supplied with the Micro Decision*

The overall speed of the machine indicates that there is good work inside the BIOS in other areas as well, such as deblocking and disk access. . . . The disk access speed may, in fact, be the Morrow's single best quality.

BDOS ERROR ON B:BAD SECTOR



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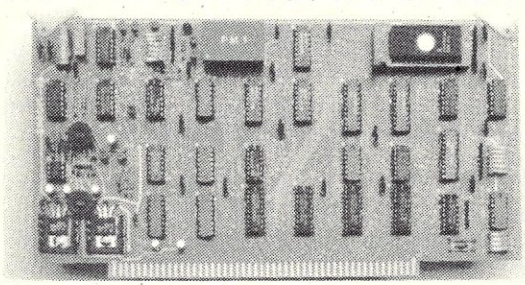

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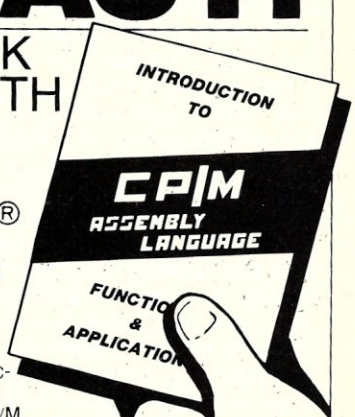

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cluded, but it appeared to be a fairly advanced version, allowing cursor control and chaining to external programs, among other functions.

Documentation

The manual for the Micro Decision itself is quite good. It doesn't make any assumptions about the user's proficiency and tells in plain English how to set up and run the system. It is indexed and is organized from "basic" to "advanced" in terms of what you need to know to make it go. I had no difficulty finding the topics I was interested in, but kept yearning for more technical detail. For example, the terminal appears to behave like an ADM-31, but no list of its escape and control codes is to be found. More documentation on the RS-232 ports would have been more helpful than a suggestion to pick up the Intel data sheets for the 8251.

Morrow was one of the first to distribute the CP/M manuals in a form other than their original multivolume typewritten format. They issued a compact softcover book, instead. Well, they've done it again here, and with two additional manuals that really needed taming: WordStar and Microsoft Basic. There is no change in content for either manual—just a more convenient package. The other documentation is in a three-ring binder. Both Logicalc and BaZic are well documented, but Correct-It is a little brief for my taste.

Performance

I have used only one 5¼″ disk system that is faster than the Micro Decision, the Altos Series 5-15D. All the others are noticeably slower. The speed is truly laudable, as it makes WordStar's overlays unobjectionable, while they are generally excruciatingly slow on most other minifloppy systems. The disk access speed may, in fact, be the Morrow's single best quality. Certainly there is nothing remarkable about the 4MHz 64K Z80.

It's nice that the series ports can go to 19,200, just in case you have a fast terminal. WordStar at that speed begins to rival the memory-mapped systems. With the advent, however, of telecomputing and micro networks, I think that a third serial port would have been a worthwhile addition. It is simply too much trouble to open the system up and reconfigure the printer port for a modem. If they had selected some other UART, such as the Zilog S10, they could have had four ports with no net increase in board real estate. As it stands, the Micro Decision is utterly unexpandable, with the exception of the additional drives.

There is a potential problem area with the disks. Either Morrow's disk duplicator is out of whack, or the data recovery circuitry is too fussy. The distribution disks were very hard to read successfully and generated many disk errors. Disks created on the machine were completely reliable. Another Micro Decision owner that I spoke with had the same problem. We did not have a chance to exchange disks to see if the problem was the distribution disks or the machines. My suspicion is that the distribution disks were at fault; the machine was too mannerly the rest of the time for the fault to lie within.

Figure 6. *Micro Decision keyboard*

The terminal portion of the system is a curious combination of good and bad. The video quality is excellent; the keyboard is execrable. First off, there is absolutely no rollover. This alone puts it outside the viable choices for word processing by a merely competent typist. Second, the keyboard is not stepped or dished and the space bar is higher than the bottom row, making it an easy target for inadvertent striking. If I were George Morrow, I certainly wouldn't have put my name on it regardless of the price.

Summary

Aside from the limitations of the terminal, the Micro Decision is a good little computer. The amount of machine and software you get for the price is simply stunning. Until now, the only other machine to offer so much for so little was the Osborne 1, a system not without some idiosyncracies of its own. Okay, I would have liked a little more horsepower in the I/O department, and I could always make a case for more disk storage. But this is an entry-level package, and it's unlike any other entry-level package offered to date. The basic marketing decisions were right on the money: People don't necessarily want portable computers, they want cheap computers with lots of software.

Would I recommend this system to a first-time user? Sure. But I'd caution him to pick out a terminal that he liked first. With the addition of a database manager, it would fulfill 90% of most people's needs for light business and virtually all home computing.

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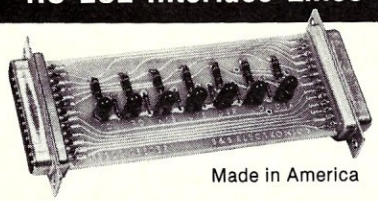

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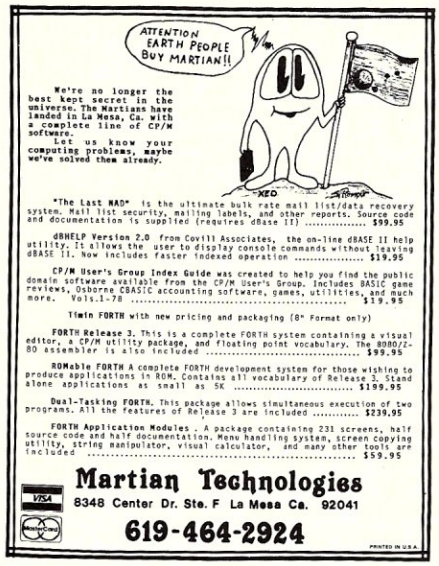

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Software Directory

Program name: SYSTEM-TMS7—Cross-assembler for TI TMS7000
Hardware System: CP/M 8" SD, 5¼" North Star or Micropolis Mod II
Minimum memory size: 16K
Language: Object code
Description: Development software comparable to that offered by microprocessor manufacturer enables any CP/M system to serve as a development station for Texas Instruments TMS7000 series microprocessors. With minor exceptions, assembler features instruction mnemonics and syntax as defined by processor manufacturer. Macro assembler includes full macro and conditional assembly features as well as the ability to chain a series of source files together during a single assembly. The interactive editor/assembler is intended for the rapid creation, modification and test of program modules. A cross-reference generator is included. Programs developed under this system must be off-loaded to the target processor for test. Facilities are provided to implement off-loading as a direct transfer from memory, via a byte stream over a CPU port, or via .COM or .HEX files.
Release: 1982
Price: $150
Included with price: Macro assembler, interactive editor/assembler, text editor, cross-reference generator, documentation, and full user support by mail or phone.
Author: Allen Ashley
Where to purchase it:
395 Sierra Madre Villa
Pasadena, CA 91107
(213) 793-5748
CIRCLE 120 ON READER SERVICE CARD

Program name: WES
Hardware system: WES runs under CP/M-80, CP/M-86, MS-DOS, or IBM PC-DOS
Minimum memory size: 42K + operating System
Language: Assembly
Description: A full-featured word processor with math capability. Integrates visual editing, printing, mail merge, database recall, and formula-free math in one user-friendly program. The math feature allows an operator or a macro command to +, −, *, /, or % any number in the text into an accumulator. Answer can be popped back into text where desired. Interactive prompts, which make WES easy to learn and use, also give the operator power to control the paging, printing, mail merging, and database-recalling activities as they occur. Mail merge and database recall can draw facts and figures from any ASCII file whether created by WES, another word processor, or as output from a Basic, Fortran, Cobol, or other data processing program. WES works with either fixed-width undelimited data fields or variable-width delimited ones.

Features file crash recovery; outside file get and put; multiple text buffers; powerful macro language; control of margins, tabs, word wrap, indention under multiple format lines; undo of kills and deletes; decimal tabulation; immediate on-screen justify, doublespace and collapse; inter and intra buffer block move; paging with headers and footers, footnotes, windows, need lines, page popping and numbering; printing of underlines, superscripts, subscripts, and boldface characters; and MATH.
Release: July 1982
Price: $395
Included with price: Disk with program and 20 training jobs, reference manual, step-by-step job training text.
Where to purchase:
Westerly Business Systems
137 Main Street
Westerly, RI 02891
(401) 596-1811
CIRCLE 121 ON READER SERVICE CARD

Program name: The Optimizer
Hardware system: Any CP/M
Minimum memory size: 48K
Language: C
Description: Financial modeling software for use by small business. Allows "what if" kinds of scenarios. Competitive with SuperCalc and Visicalc, but simpler to use because of self prompts and error traps.
Release: March 1982
Price: $200
Included with price: Object code on disk (any CP/M format) and 72-page manual.
Where to purchase it:
SuperSoft, Inc.
P.O. Box 1628
Champaign, IL 61820
(217) 359-2112
CIRCLE 122 ON READER SERVICE CARD

Program name: SM-MODEM Telecommunications Package
Hardware system: Any CP/M system with a modem. Controls Hayes SmartModem and SmartModem 1200. Version for PMMI.
Minimum memory: 24K
Language: Machine code
Description: This is a major enhancement of MODEM7 by the author of MODEM7. Contains the multiple file transfer of MODEM7 and an enhanced Terminal mode. Will work with any external modem and has special routines for control of the Hayes SmartModem and SmartModem 1200. These special routines may be disabled if the user does not have a SmartModem.

The program is capable of using a separate file that contains names and phone numbers. By entering a name, the number will automatically be dialed. The user may specify continuous dialing until a connection is established. In addition, another ASCII file may be created which contains commands that may be sent while in terminal mode by pressing only two keys. The program also fixes many bugs that were in the original program.
Price: $95, including documentation (32 pages).
Where to purchase it:
Mark Zeiger
198-01B 67th Ave.
Flushing, NY 11365
(212) 454-6985

CIRCLE 123 ON READER SERVICE CARD

Program name: Printing package for MX-80
Hardware system: 8080 CP/M system
Minimum memory: 48K
Language: COM files provided for all programs, Microsoft BASIC source for all but 2
Description: A set of 8 application programs are provided for the EPSON MX-80 printer. Initialize the printer mode to COMPRESS or BOLD (or ITALICS with GRAFTRAX 80) directly from CP/M or even Wordstar. Print mailing and return labels on stock 1 or 2 labels wide. Make banners as long as you want with letters up to 8″ high. List files (with title, page numbering, date, margin and more—all as options). The package also includes a programmable block letter utility for high quality lettering 3 lines high (not for use with Graftrax +, but works fine without GRAFTRAX).
Release: November, 1982
Price: $35 (Documentation only $3.50, refundable with purchase).
Included with price: Manual and 8″ SSSD disk
Where to purchase it:
Microsmith Computer Technology
P.O. Box 1473
Elkhart, IN 46515

CIRCLE 124 ON READER SERVICE CARD

Program name: ACOM
Hardware system: North Star Horizon running DOS 5.2DQ or North Star ADVANTAGE running GDOS
Minimum memory: 24K for the Horizon or 64K for the ADVANTAGE
Language: North Star Basic and Z80 code
Description: ACOM allows North Star Horizon or ADVANTAGE computers to receive and transmit ASCII data via the serial port. Programs and text may be downloaded from and uploaded to remote systems, bulletin boards, information networks, or personal computers. The received text may be saved, edited, and printed. Basic programs may be retrieved from disk and transmitted. Data received from the serial port may be subsequently saved as a text or program file. Full or half duplex modes are available.
When released: May 1, 1982
Price: $49.95 for either version; $69.95 for both
Included with price: Either version includes one mini-diskette and instructions.
Where to purchase it:
The Computer Shoppe
283 Medford Ave.
Patchogue, NY 11772
(516) 758-6558

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Note: *The correct phone number for Stok Software, Inc., formerly Stok Computer Interface (listed in the Nov/Dec 1982 Software Directory) is (212) 243-1444.*

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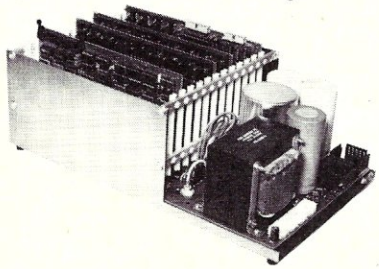
New Products

S-100 12-slot module

The S1-MOD is a self-contained S-100-based computer module that can serve a variety of purposes: (1) An in-shop test system base; (2) Self-contained core for a custom OEM complete design; (3) A hobbyist 'bare bones' system.

The single-board design contains all S-100 and floppy disk power supplies; it also has some extremely useful features that are not readily apparent:

Double density, which is the industry standard today, is very sensitive to hidden DC ground loops common to many hand-wired systems. Therefore, it makes a lot of sense to include the computer power supply along with the motherboard. Besides being simple to assemble and very compact, great advantage is gained from the fact that there is a common ground



area linking the S-100 bus, computer power supply, and disk supplies together.

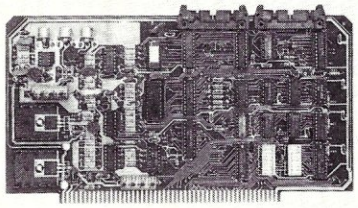
The design of the main power current source (+8V at 30A) contains a custom-wound transformer that is balanced to provide a maximum of dropout immunity under heavy load conditions. 40A stud-mount diodes can handle 100A peak surges at each cycle, transferring more energy from the transformer to the main filter capacitor and minimizing ripple to on-board regulators. This system is guaranteed to be the quietest, most loopless design ever produced due to the nature of the common power board.

Price: Kit, A&T, $225. ***Micro Sales**, 15381 Chemical Lane, Huntington Beach, CA 92649; (714) 891-2677.*

CIRCLE #126 ON READER SERVICE CARD

S-100 speech synthesis board

Speech synthesis with sound effects is the output of the new ADS speech synthesis board, the Synthetalker. Using the powerful Votrax SC-01 chip for speech synthesis, the Synthe-



talker has an on-board DAC and mixer to add tremolo, multiple voices, and many special effects to the 64 phonemes, four inflection levels, and automatic phoneme timing of the SC-01. Equipped with on-board audio amplifier (250 mW into an 8-ohm load), the Synthetalker is also set up for preamp output.

There is provision for external input. Inputs and outputs are connected via on-board RCA-type phono jacks for mating to audio systems with shielded cables. The Synthetalker comes with complete manual including software examples. Unusually clear speech is made possible by software control of pitch on the SC-01 via the 8-bit DAC.

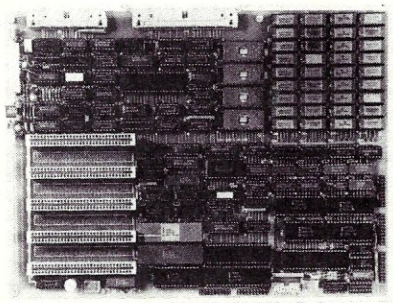
Price: Kit, $279.95; A&T, $310. **Ackerman Digital Systems, Inc.,** *110 N. York Rd., Suite 208, Elmhurst, IL 60126; (312) 530-8992.*

CIRCLE READER SERVICE CARD #127

16-bit single-board computer

The MPX-16 by Micromint—a complete single-board computer system fully compatible with the applications software and hardware peripherals designed for the IBM PC—uses all the peripherals available for the IBM, and overcomes some of the expansion weaknesses of the IBM by incorporating many peripheral devices as part of the basic board.

The MPX-16 is designed around a 5MHz Intel 8088 CPU with addressing for up to 1 MB of RAM. Provision is also made for an Intel 8087 math coprocessor, and a hard-disk drive can be added. The MPX-16 also includes 256K of RAM, 2 serial and 3 parallel I/O ports, a double-density floppy disk controller, and five expansion slots. It was initially designed to use CP/M-86; Microsoft's MS-DOS and other software will be available soon. The CP/M-86 BIOS module is contained in a set of EPROMs on the board.

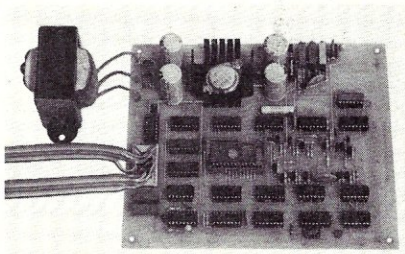


Price: $1,200 in 100 quantity. **Micromint, Inc.,** *561 Willow Ave., Cedarhurst, NY 11516; (516) 374-6793.*

CIRCLE 128 ON READER SERVICE CARD

CP/M EPROM programming system

A stand-alone single board (6" x 7.5") that programs 2708, 2758, 2716, 2732, 2732A, and 2764 EPROMs has been re-



leased by AndraTech. It is software-controlled and does not require changing personality modules or dip switches. The unit derives all power from the AC line and is interfaced via one 8-bit input port and one 8-bit output port. No special handshake or strobe lines are required.

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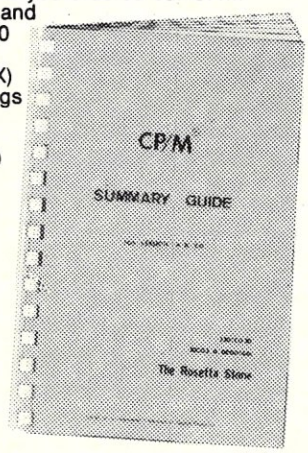

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The menu-driven CP/M-compatible software (8K) provides the following commands: program EPROM from disk file or RAM, copy EPROM, verify EPROM with RAM, and read EPROM. A monitor with 11 commands for RAM display and modification is also supported. The software operates with port or memory-mapped I/O and is configured for the host system easily. It is distributed on 8" disks (SSSD) and requires CP/M 1.4 or greater with 48K of RAM. The system consists of the software on disk, a bare PC board, and a 27-page user/assembly manual.

Price: $75. **AndraTech,** *1235 Village Glen, Batavia, OH 45103.*

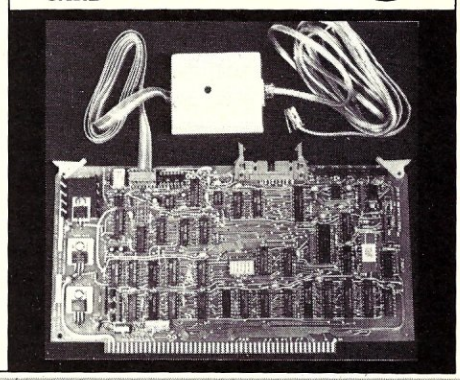
CIRCLE 129 ON READER SERVICE CARD

DTMF encoder/ decoder and speech synthesizer

The MM-VT1 is a DTMF encoder/decoder and speech synthesizer that allows data entry and access from any Touch-Tone® office or pay phone. Computer replies in a synthesized voice. The MM-VT1 uses an unlimited vocabulary, phoneme-type speech synthesizer with adjustable volume, and software-controlled pitch. It sends (and receives) all 16 Touch-Tones, which it has encoded from (decoded to) binary data. Interrupts are fully software-controllable. The MM-VT1 answers and dials (Touch-Tone or pulse) the phone automatically. Additional features include 8-bit TTL parallel port input, 8-bit high voltage open collector parallel port output, plus dial tone and ring detection. The MM-VT1 is FCC-registered for direct connection to the phone line and is IEEE-696/S-100 compatible.

Prices: with speech synthesizer and parallel port, $384.95; without, $259.95. **PMMI Communications,** *5201 Leesburg Pike, Suite 604, Falls Church, VA 22041; (703) 379-9660.*

CIRCLE 133 ON READER SERVICE CARD



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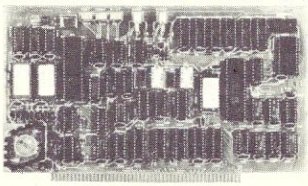

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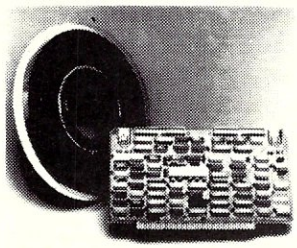

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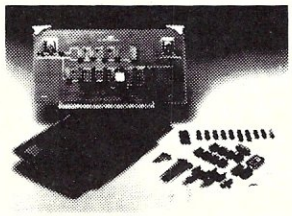

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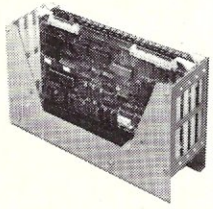

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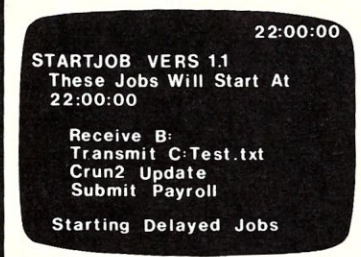

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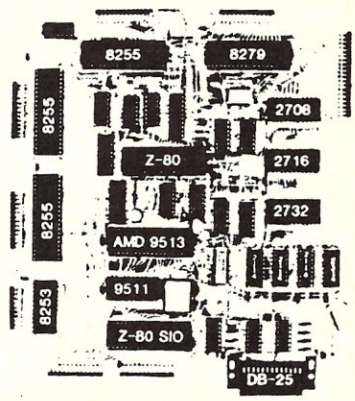

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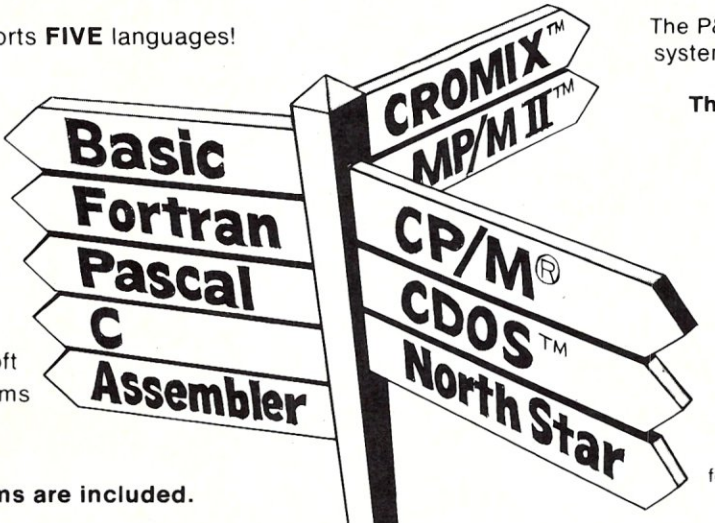
CIRCLE 157 ON READER SERVICE CARD

THE P&T IEEE-488 BUS GOES TO THEM ALL!

The P&T-488 interface enables you to use your S-100 computer and any of these operating systems and languages to communicate with 488 equipment.

The P&T-488 supports **FIVE** languages!

- Basic:
  Microsoft
  CBasic 2®
  Cromemco
  North Star
- Pascal:
  Pascal/M™
  Pascal/MT+™
- Fortran: Microsoft
- C: Quality Systems
- Assembler



Sample Programs are included.

The P&T-488 supports **5** operating systems, **2** of which are multiuser!

The P&T-488 includes useful utilities!

- Interactive **bus monitor** aids setting up test equipment.
- **Self test** checks the interface for proper operation

The P&T-488 is **complete!**
Interface, manual, programs on disk, 18" cable and connector mounting hardware are all included for $450 (domestic, FOB Goleta).

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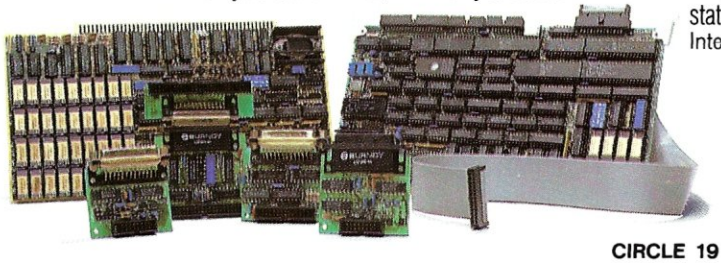

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