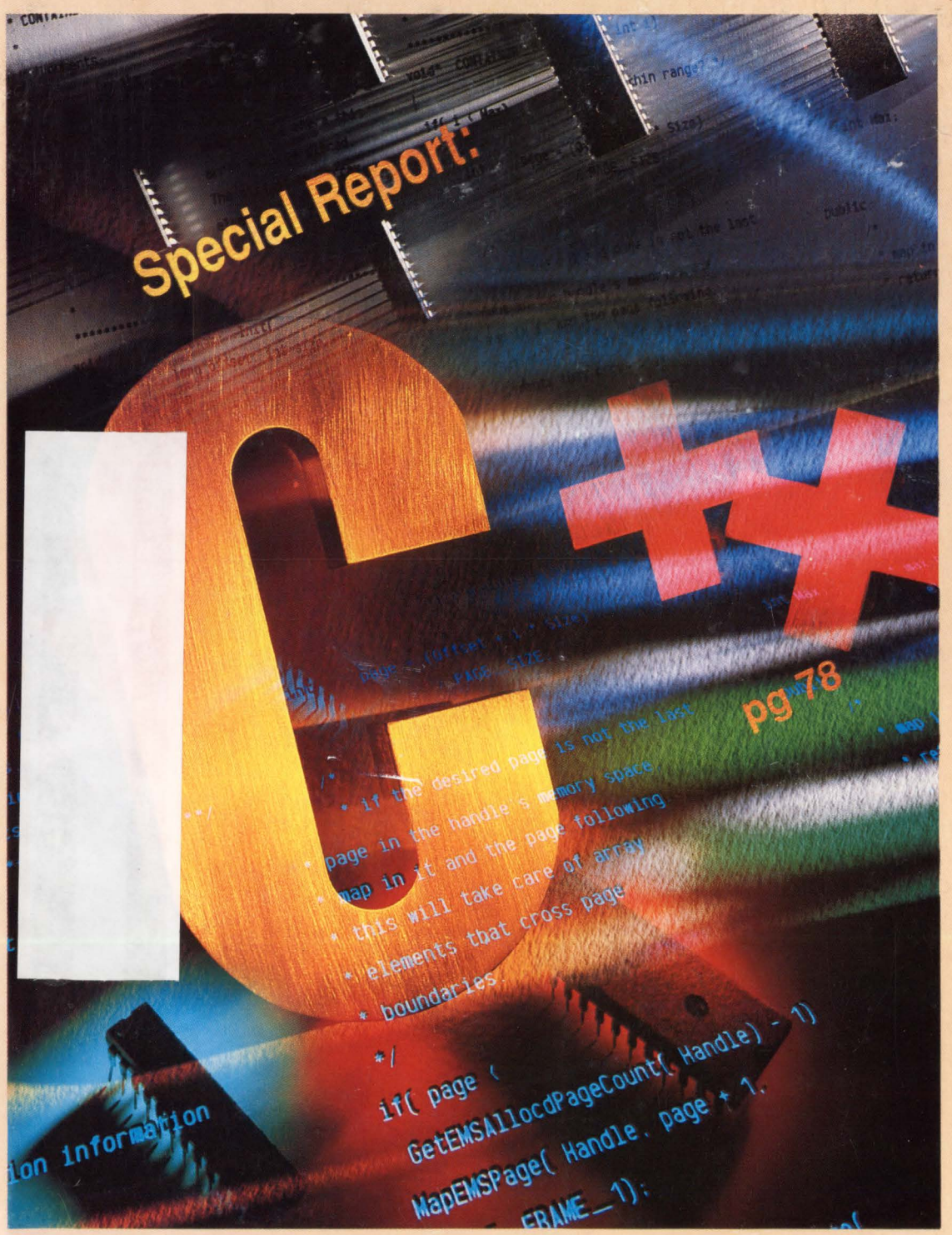
EDN

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

PROCESSOR UPDATES PG 65

A CAHNERS PUBLICATION

AUGUST 6, 1992



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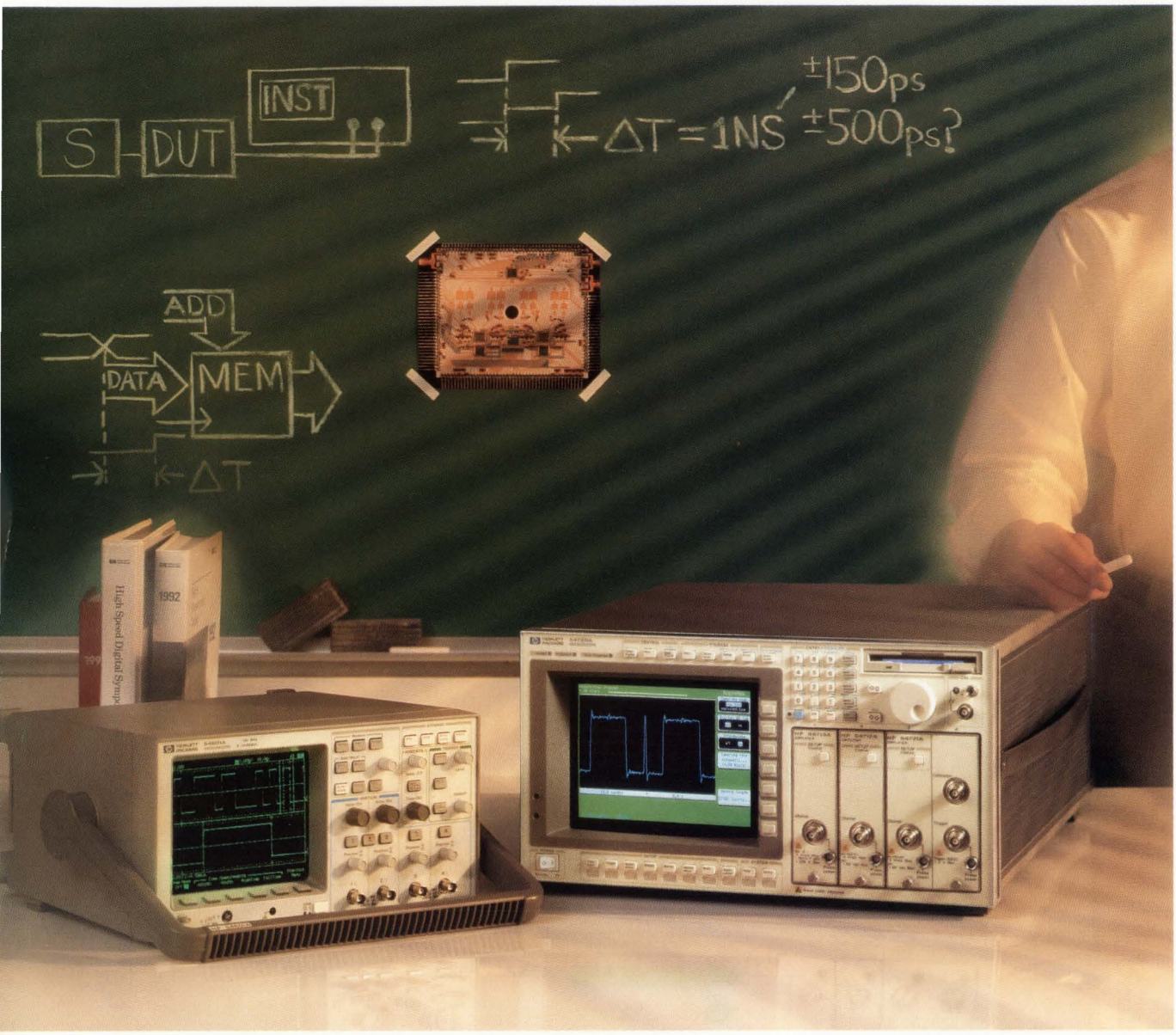
HP scopes make digital designs easier to understand.



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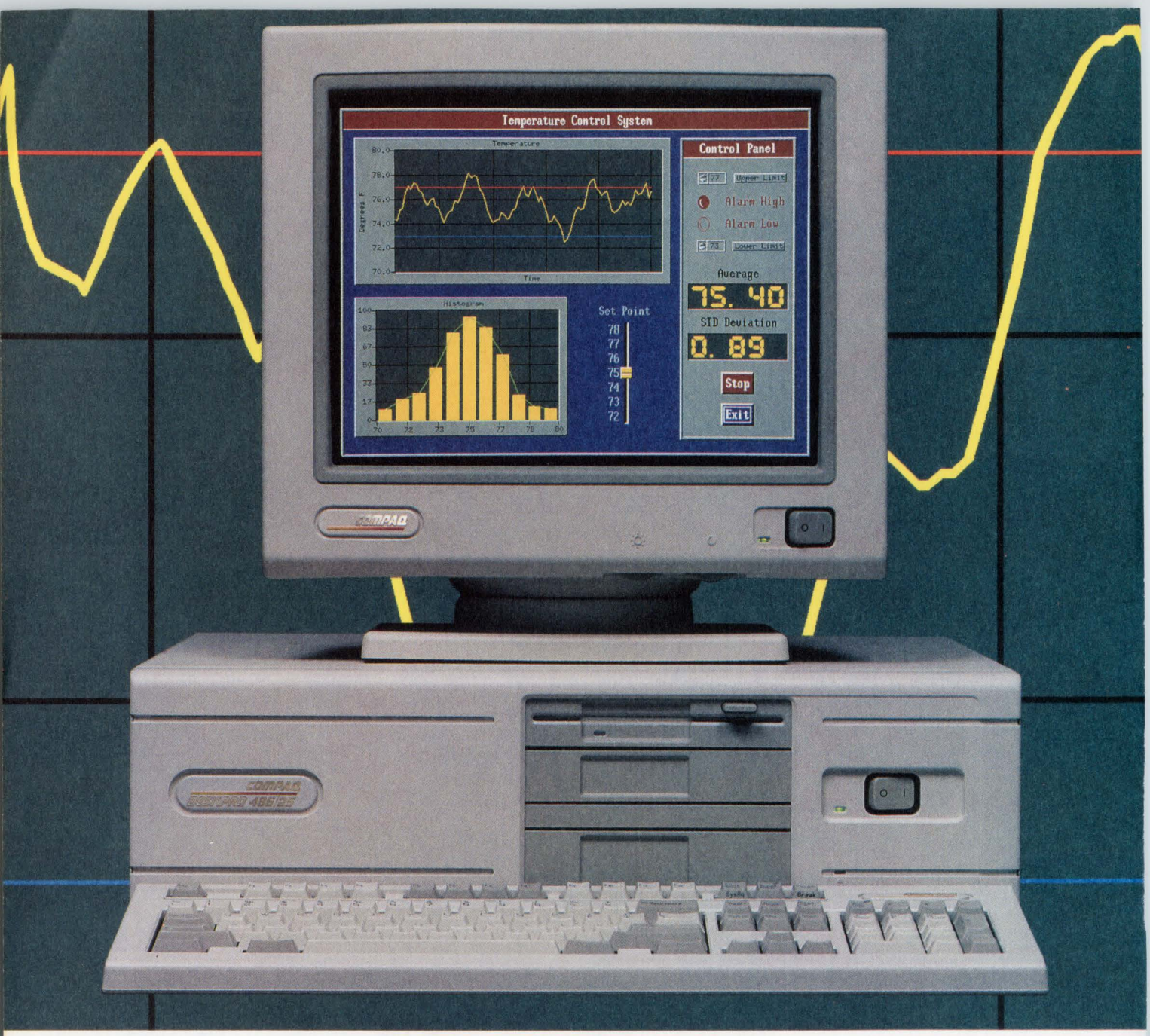

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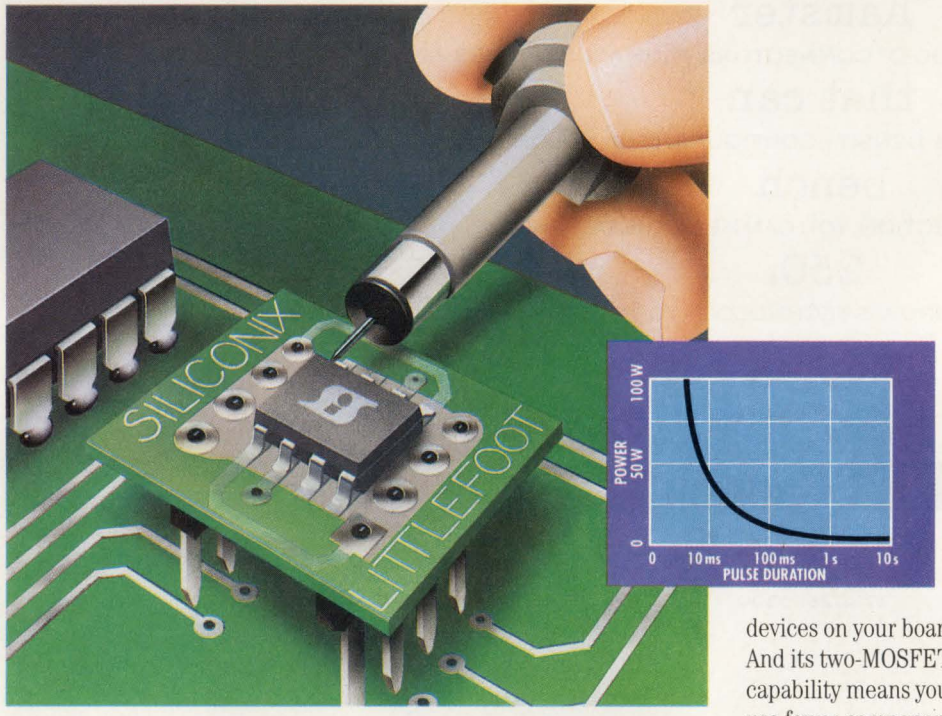
LITTLE FOOT

"SIZE IS POWER" DEBUNKING THE MYTH



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	-25	-2.3	0.25
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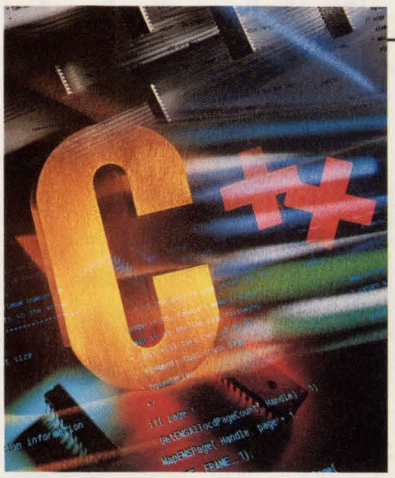


On the cover: With a few exceptions, C++ is a superset of our old and familiar friend, C. And like an old friend, C++ is comfortable, friendly, and has its little idiosyncrasies. (Photo courtesy Borland International; art direction by Ilene Rosenberg; photography by Dave Casteel) . . . . . **PAGE 78**

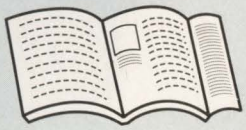
SPECIAL REPORT

DESIGN FEATURES

Continued on page 7

Foldout Contents

Turn to the last information-retrieval service card in the back of this magazine and you'll find a foldout table of contents. Now, instead of flipping back and forth from this table of contents to the articles you want to read, you can have the convenient foldout open at all times while you're reading EDN. Use the foldout contents to mark off articles you'd like your colleagues to read or to remind yourself to copy stories for your files.



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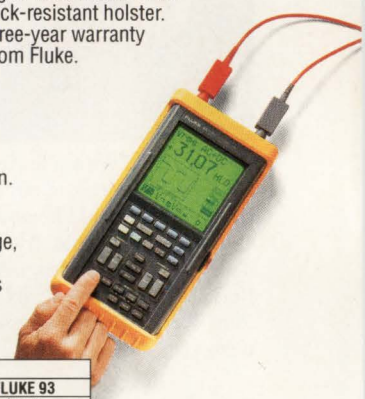

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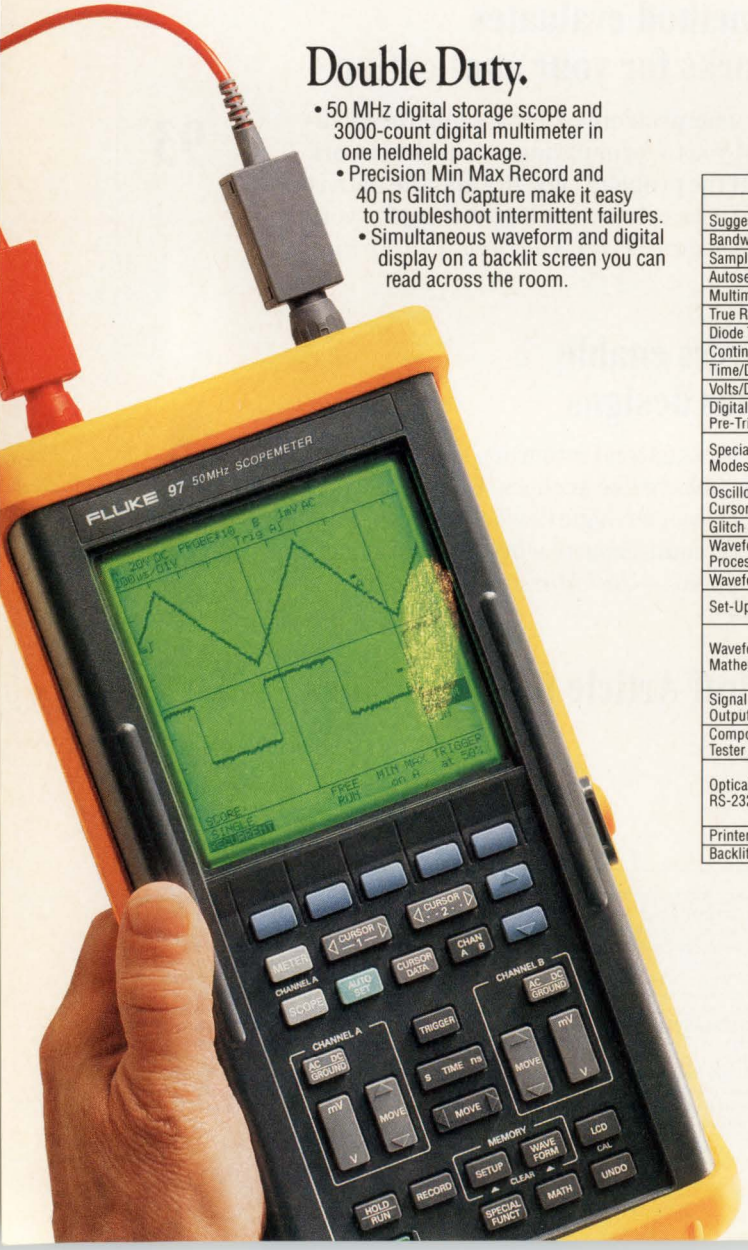

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True RMS Volts	AC or AC+DC up to 600V (1700V Pk–Pk)		
Diode Test	Up to 2.8V		
Continuity Beeper	Yes		
Time/Division	10 ns/div to 60 sec/div		
Volts/Division	1 mV/div to 100V/div		5 mV/div to 100V/div
Digital Delay or Pre-Trigger	By Number of Cycles, Events, Time, or Zoom Mode		By Time
Special Multimeter Modes	Min Max Average Record, Relative (zero), dBm, dBV, dBW, Audio Watts, % Scale, Frequency, Smoothing,™ Change Alert™		Frequency, Smoothing™ Change Alert™
Oscilloscope Cursors	12 Measurements, Display 5 Simultaneously		
Glitch Capture	≥40 ns		
Waveform Processing	Average, Variable Persistence, Min Max Record		
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AUGUST 6, 1992

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TECHNOLOGY UPDATE

ADC architectures: Speed-resolution tradeoff key to choosing ADCs

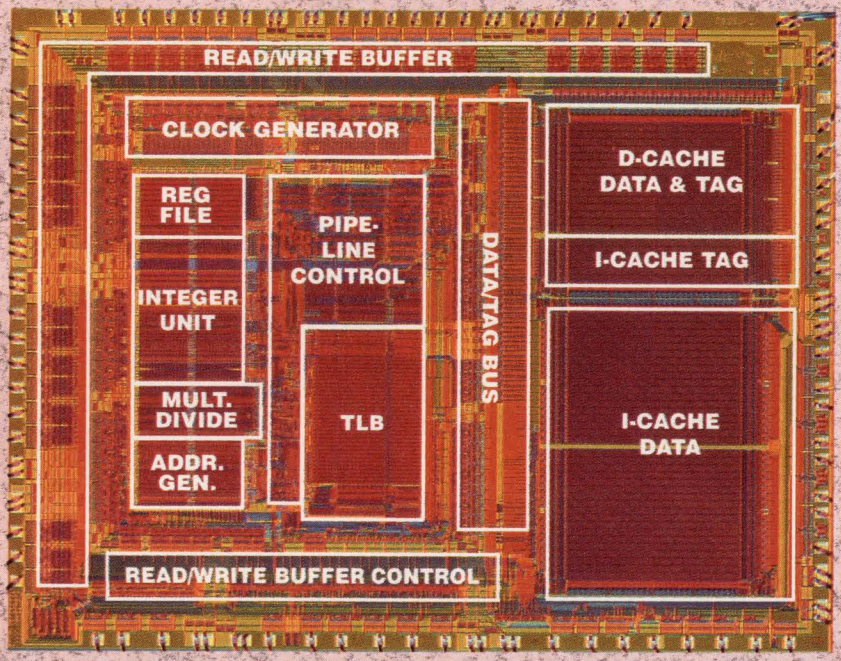
PRODUCT UPDATES

PROCESSOR UPDATES

NEW PRODUCTS

DEPARTMENTS

The Next World Standard for Embedded Systems



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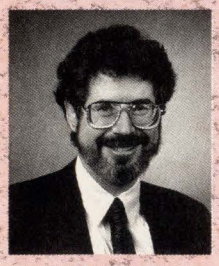

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CIRCLE NO. 6

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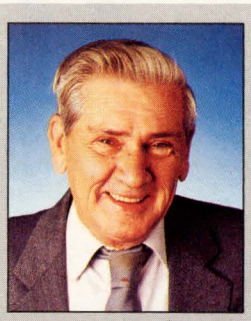
INSIDE EDN

A summary and analysis of articles in this issue

If the confusing and sometimes nonsensical terminology of **object-oriented programming** (OOP) articles has left you reeling, turn to this issue's Special Report. Senior Technical Editor Charles H Small uses concrete examples and diagrams to show how C++ works in the world of OOP. He's used this same nuts-and-bolts approach in his previous articles describing the inner workings of embedded DOS, Unix, diagrammatic compilers, and Windows.

Charles begins by comparing the arrays and array-defining constructs of C to the objects and classes of C++. He asserts that if you have ever programmed in any high-level language, you've been using a class to generate objects all along. He continues the analogy by comparing manipulating C++ objects to manipulating C constants, variables, strings, arrays, and structures. Even if the computer languages you know don't include C, you'll be able to follow along. If you want to learn still more about C++, try browsing through EDN's bulletin-board system (BBS), which has a variety of C++ software including compilers, preprocessors, libraries, and computerized tutorials.

Leaving the software world of OOP, we enter the analog realm of the real world. But much real-world information processing occurs in the digital realm. To get from one realm to the next, you'll need an A/D converter. If your current design needs an ADC—and especially if you're choosing a converter for the first time—you'll want to check out Contributing Editor Dave Pryce's Technology Update on **ADC architectures**. He says that looking at the converters' architectures will help you understand the advantages and disadvantages of each type. The architectures he examines are successive-approximation, flash, subranging, integrating, and sigma-delta.



In this issue, Contributing Editor Dave Pryce's Technology Update focuses on ADC architectures.

Dave concentrates on resolution and speed, which a converter's architecture determines to a great extent. Not only are there speed and resolution tradeoffs among converter types, but also among converters of the same type. You can't usually obtain both the highest possible speed and the highest possible resolution with the same device. For example, successive-approximation converters have speeds of 10 ksamples/sec to 1 Msample/sec and resolutions of 8 to 18 bits. However, their resolution is limited to about 12 bits at the higher speeds. To get you started choosing an ADC, Dave includes a graph that gives you an at-a-glance view of the speed and resolution limits of the five A/D converter types.

Finally, we've heard all your clamoring and at long last we're printing our **technical-article database**. The database indexes by subject matter articles that appeared from November 1991 to April 1992 in *EDN Magazine* and *EDN News Edition*, *Electronic Design*, *Electronic Products*, *Computer Design*, and *Electronics*. A database for articles published from November 1989 to October 1991 is on the EDN BBS, so you've got one more reason to phone (617) 558-4241 with modem settings 300/1200/2400/9600 8,N,1.

Julie Anne Schofield
Senior Associate Editor

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MACH 120	1200	48	15ns	50 MHz	68	MASC 120
MACH 220	2400	96	15ns	50 MHz	68	MASC 220
MACH 130	1800	64	15ns	50 MHz	84	MASC 130
MACH 230	3600	128	15ns	50 MHz	84	MASC 230

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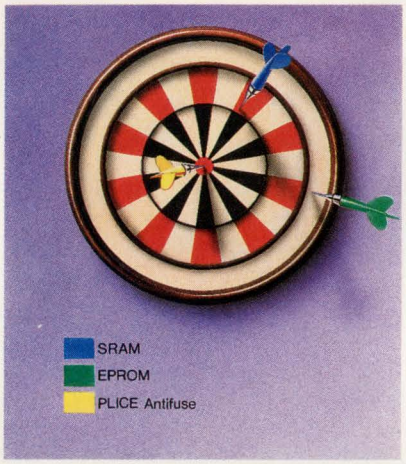
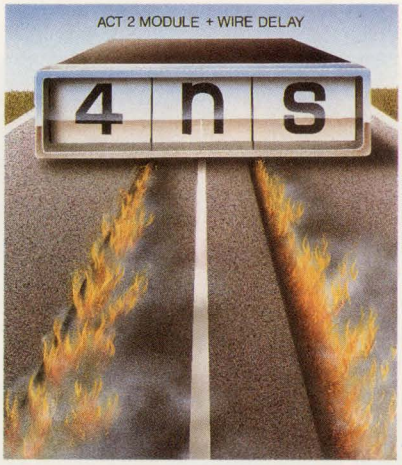
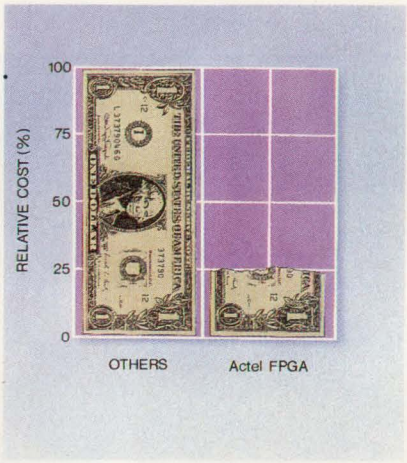






Optimal Programming Element.

PLICE® antifuse elements combine small size and high reliability, giving you FPGAs with higher speed, lower cost, greater ease-of-design, and more capacity than any other.

Superior Performance.

The antifuse-based ACT 2, the most predictable FPGA available, incurs short delays in interconnecting logic functions, which means higher speeds to keep pace with your latest microprocessor.

Lower Cost.

PLICE antifuse technology results in smaller die sizes, saving you as much as 75% off the cost of the alternative solution.

Once You Witness The Performance Of Our ACT™ 2 FPGAs, You'll Know The Real Leader Is Actel.

If you plan to move to the superior capacity, flexibility and cost of FPGAs, you should know the facts. Compare us against the industry "leader." You'll find our ACT 2 FPGAs turn in some very impressive numbers indeed.

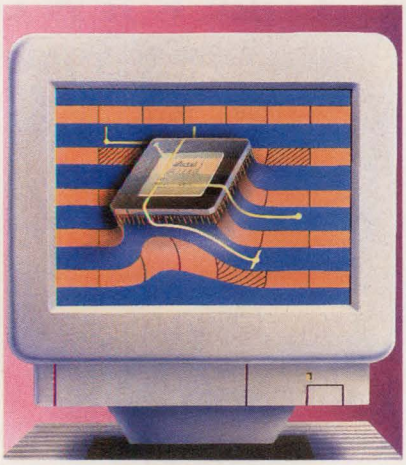
#1 in architecture. The ACT 2 family's innovative PLICE antifuse technology provides the ideal programming and interconnect elements for high-density FPGAs. Our FPGAs offer superior reliability and design flexibility, and give you the most predictable FPGA performance available. And with more than 1 million FPGAs shipped, Actel has more experience manufacturing antifuse-based FPGAs than anyone. That's experience you can count on.

#1 in speed. The fastest ACT 2 family member—the A1225—offers 2,500 gates of pure speed. With a 4 ns logic delay and system-level speeds up to 66MHz, ACT 2 helps you make the most of your design.

#1 in ease-of-use. With ACT 2, designs are easily captured with standard PLD tools like ABEL™ and PLDesigner-XL,™ as well as with your favorite schematic capture program from Mentor Graphics, OrCAD, Valid Logic Systems and Viewlogic. And Actel's Action Logic® System rapidly converts captured designs into programmed Actel devices. For years, our 100% automatic placement and routing has simplified the design process. And it's still faster and easier than any other solution.

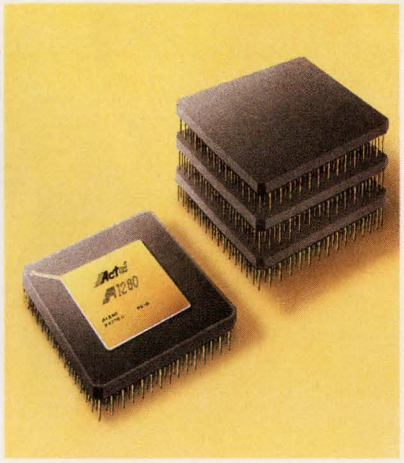
#1 in affordability. Our FPGAs also provide the best price/performance available. Actel offers

PGA Market Leader, Thoughts About Who's #1.



Designing Made Simple.

Actel devices' plentiful routing resources give you 85% gate utilization using 100% automatic placement and routing, letting you place and route a 4,000-gate design in our A1240 chip in only 30 minutes.



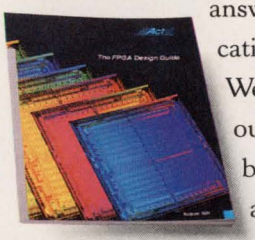
Greater Capacity.

With 8,000 gate-array equivalent gates, the A1280 has led the industry in capacity for over 2 years. And it's still the only high-density, high-performance FPGA available in volume production.

Catch Our Next Act.

We're building on this FPGA technology to set new performance levels with our upcoming ACT 3 FPGAs. Whichever ACT you catch, you'll get a long-term partner and the best performance in town.

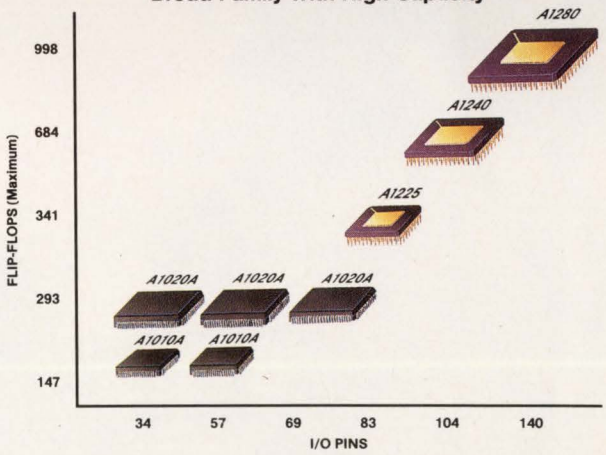
much quicker time-to-market and complete control of the design process, as well as competitive FPGA prices. Which saves you both money *and* time.


The FPGA Design Guide

And #1 in service and support. Customers can call our technical hotline and talk to a real person—not voicemail. Or customers can use our automatic Action FACTS system to fax themselves quick answers to their application questions. We're building on our experience to bring you the most advanced products for any application, and we're committed to establishing a quality, long-term partnership with you for your future success.

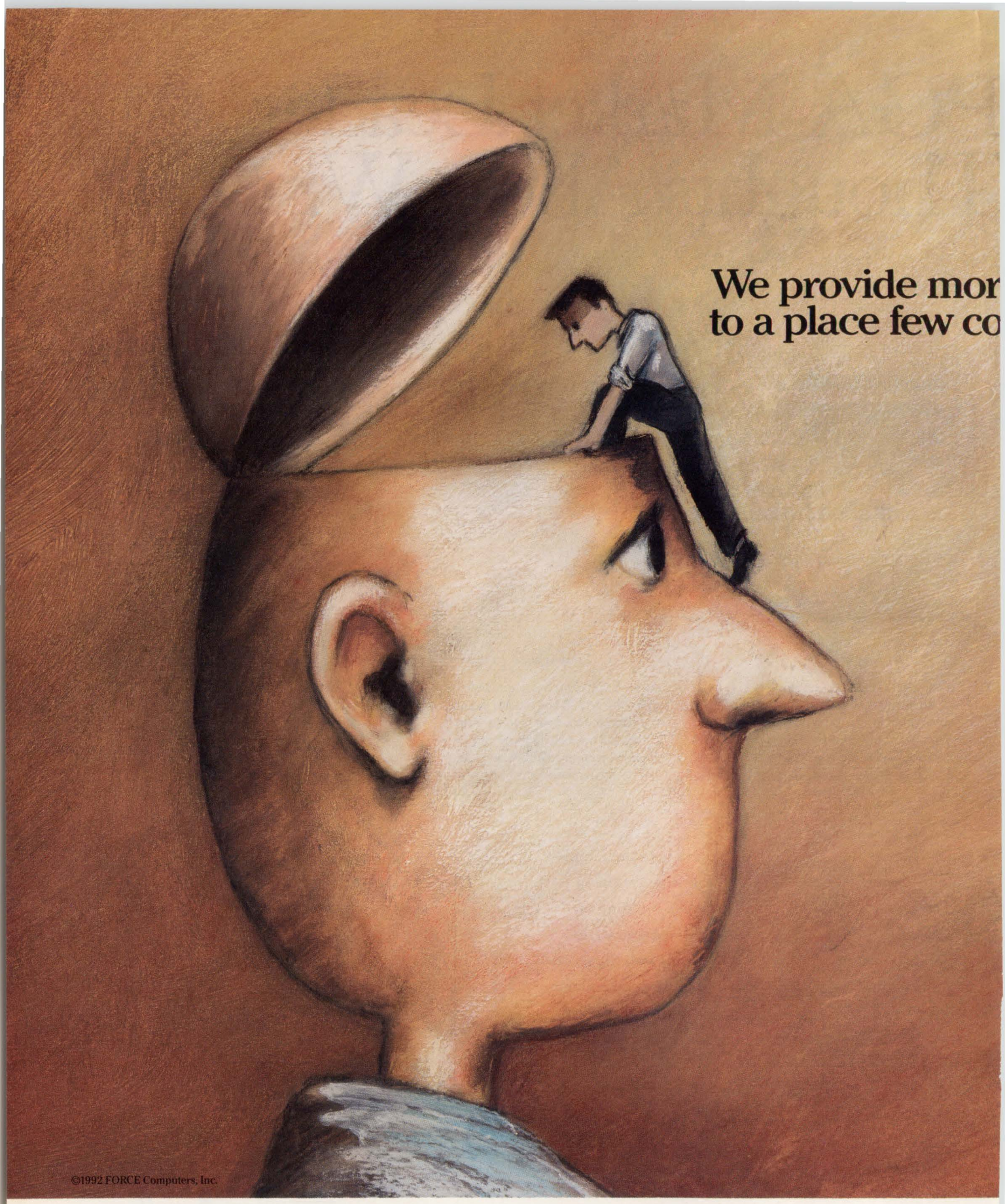
Call **1-800-228-3532** for more information on our powerful family of FPGAs. And discover how far the real industry leader can take you.

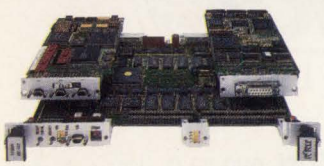
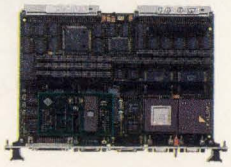
Broad Family With High Capacity

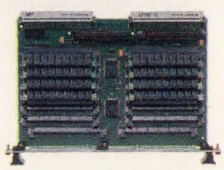


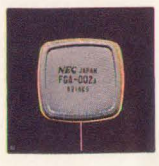
Actel
Risk-Free Logic Integration

CIRCLE NO. 8







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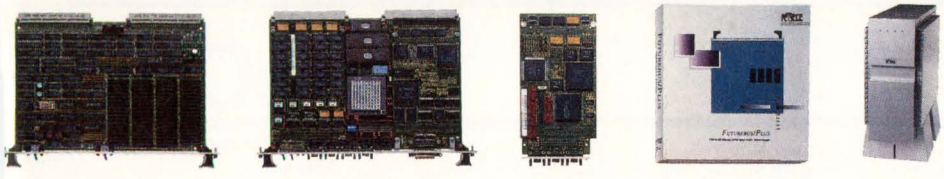

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CIRCLE NO. 9

Last year several hundred Pulse Generator users dumped the one line display and the High Price.

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LeCroy 9210 300 MHz Programmable Pulse Generator			
	with 9211 Module	with 9212 Module	with 9213 Module
TRANSITION SPEED	1 ns - 10 ms	300 ps - 1 ns	6.5 ns - 95 ms
MAX. REP RATE	250 MHz	300 MHz	50 MHz
OUTPUT LEVEL	5V p-p (50Ω)	5V p-p (50Ω)	16V p-p (50Ω)
VARIABLE EDGES	Yes	Yes	Yes
TIMING ACCURACY	±(0.5% + 0.2 ns)	±(0.5% + 0.2 ns)	±(0.5% + 0.2 ns)

LeCroy

Innovators in Instrumentation

CIRCLE NO. 16

EDITED BY SUSAN ROSE

Logic analyzers maximize performance vs price

Hewlett-Packard's 1660A family of portable analyzers suits users who want to maximize performance vs price and do so without a modular analyzer's configurability and expandability. The family includes four members with channel counts ranging from 34 to 136. All units provide 100-MHz state analysis with six clocks, a 3.5-nsec setup-and-hold window that is adjustable in 500-psec increments, 250-MHz timing analysis (500 MHz when you reduce the number of active channels by half), transitional timing at half the maximum timing-analysis speeds, and memory of 4 kbits/channel (8 kbits/channel with half the channels active). The firm has also enhanced the user interface; for example, besides a hexadecimal keypad, the front panel includes a "QWERTY" pad for entering alphabetic labels. Moreover, you can attach a separate keyboard and a mouse. The 102-channel unit costs $10,900; the 136-channel unit costs $13,500; the 34- and 68-channel units cost $5900 and $8500, respectively. Hewlett-Packard Co, Colorado Springs, CO, (800) 452-4844.

PC kit teaches and runs VHDL

For $795 you can buy a full VHDL (VHSIC-Hardware-Description-Language) development system with a step-by-step tutorial that runs on a PC. The VHDL SelfStart_Kit from Topdown Design Solutions bundles the Model Technology DOS-based VHDL development system with a hands-on tutorial. The development system includes a VHDL compiler, simulator, and debugger. With it, engineers can compile and run VHDL models and designs on 286, 386, or 486 PCs. A Windows version, SelfStart_Kit/Windows-B, is available for $2490. On a 25-MHz 486, the Windows version compiles VHDL code at a rate of 1500 lines per minute. For a few hundred VHDL lines, compile and simulation times run 1 to 2 minutes. The system supports the full IEEE-1076 VHDL language, not a subset of the language.

The system's tutorial consists of a core text and a set of lab experiments. It gives users a fast, hands-on start, using VHDL basic structures to build and simulate actual logic designs. Users build a bit-slice processor complete with a 3-port register RAM, input multiplexers, ALU, and shifter. With the tutorial, engineers can get a feel for VHDL basics, as well as familiarity with what it takes to do VHDL compilation and simulation. This is not a high-level, complex course, but rather a nuts-and-bolts tutorial for experienced logic designers who want to get into VHDL. Topdown Design Solutions, Nashua, NH, (603) 888-8811, FAX (603) 888-4258, contact Art Pisani.

Laser system excels on fine-pitch pc boards

LPKF CAD/CAM Systems' multifunction laser system lets you manufacture prototype and production pc boards with the high resolution needed for fine-pitch technology. The system exceeds the capability of chemical etch systems, allowing as many as seven conductor paths between a 0.1-in. grid spacing and three conductor paths between a 0.05-in. grid. System prices start at $160,000. LPKF CAD/CAM Systems, Beaverton, OR, (503) 645-0240, FAX (503) 645-0403.

0.8-μm ASICs operate from 2.7 to 5.5V

The TGC1000 and TGC-1000LV family gate arrays from Texas Instruments feature a sea-of-gates architecture consisting of a new CMOS base cell for low-voltage operation and efficient implementation of memory functions. The cell meets the requirements of systems that adhere to voltage standards from 2.7 to 5V. The two families include 12 base arrays that range in complexity from 16k to 455k gates. Gate utilization is approximately 70%. The LV version dissipates 0.8 μW per MHz per gate. For each base array, the company offers double-level-metal interconnect for I/O-limited applications or triple-level-metal interconnect for core-limited applications. The gate arrays come in a range of packages, including plastic leaded chip carriers, plastic quad flatpacks, and metal quad flatpacks. I/Os range from as many as 558 for conventional packaging to 696 in tape-automated-bonding carriers. NRE costs start at $20,000. Texas Instruments Inc, Semiconductor Group, Dallas, TX, (214) 995-6611, ext 3990.

Pulse generator handles TTL, ECL, and CMOS

Pulse Research Lab's PRL-150 is a 100-MHz time-mark pulse generator that fits in a hand. You can use it to test and calibrate oscilloscopes or as a precision high-frequency signal source for test applications that don't require continuously variable frequency and pulse-width signals.

The $597 generator handles TTL, CMOS, and ECL signal levels. The device generates 151 distinct time markers—from 10 nsec at 100 MHz to 160 nsec at 0.0065 Hz—by dividing the internal crystal-controlled 100-MHz time-base frequency through a counter chain. You use a 10-position decade period switch and a multiplier switch (1× to 16×) to select a time period. The output pulse width is constant, approximately half the output frequency period, and multiplied by the period switch setting. The generator provides 0.2%, 5V dc or 5V p-p, and 1-kHz square wave for amplifier gain check or probe alignment. The generator fits into

a 6.3 × 3.5 × 1.2-in. high-impact plastic enclosure with two BNC connectors. For TTL levels only, you can buy the $385 PRL-155. Pulse Research Lab, San Pedro, CA, (310) 514-1478. FAX (310) 514-0115.

Integrate VHDL into ASIC designs

At this year's Design Automation Conference, Cadence Design Systems demonstrated a VHDL (VHSIC-Hardware-Description-Language)-based design tool set with mixed-level design composition, 1076-language simulation, and VHDL synthesis. Composer ($14,500) with mixed-level design capture and VHDL-XL ($35,000), with support for 135 certified libraries, are available now. The Synergy VHDL Synthesizer ($15,000) and Optimizer ($45,000) will be available in the fourth quarter of 1992. All the tools share the same VHDL intermediate formats, libraries, timing information, delay calculator, and user interface. They work with the company's Design Framework II and with its ICs and ASICs. The tools exchange timing information in the company's public-domain standard delay format (SDF). The software couples a proprietary gate-level simulation algorithm with behavioral algorithms, letting users simulate at different levels with one tool. Cadence Design Systems Inc, San Jose, CA, (408) 944-7339.

Universities receive software

Cadence Design Systems Inc donated more than $12 million worth of electronic-design-automation software to the California Institute of Technology (Pasadena, CA) and the University of Dayton (Dayton, OH). Through the Cadence University Program, the company supports leading educational institutions with real-world commercial software-design applications. More than 270 institutions worldwide have benefited from the program with software donated and supported by the company in excess of $100 million. Cadence Design Systems Inc, San Jose, CA, (408) 944-7339.

Parallel-processing award finalists announced

Finalists for the 1992 Gordon Bell Prize competition will present their projects at Supercomputing 92, November 16 to 20, 1992, in Minneapolis, MN. The competition recognizes the application of parallel processing in practical scientific and engineering problems. The IEEE Computer Society and the Association for Computing Machinery sponsor the conference. Prizes go to spur the transition of parallel processing from computer-science research to useful applications.

The two $1000-prize winners will be chosen from entries submitted in three categories: performance; price/performance; and compiler parallelization. The finalists are:

- Tom Cwik, Jean Patterson (Jet Propulsion Laboratory) and David Scott (Intel Corp)—Electromagnetic Scattering Calculations on the Intel Touchstone Delta
- Anton Gunzinger, Urs Müller, Walter Scott, Bernhard Bäumle, Peter Kohler, Florian Müller-Plathe, Wilfred F van Gunsteren, and Walter Gugenbühl (Swiss Federal Institute of Technology)—The Multisignal Processor System with Intelligent Communication
- Mark T Jones and Paul E Plassman (Argonne National Laboratory)—Solution of Large, Sparce Systems of Linear Equations in Massively Parallel Applications
- Hisao Nakanishi, Vernon Rego (Perdue University) and Vaidy Sunderam (Emory University)—Super-concurrent Simulation of Polymer Chains on Heterogeneous Networks
- Michael S Warren (Los Alamos National Laboratory) and John K Salmon (California Institute of Technology)—Astrophysical N-Body Simulations at 5.4 Gflops.

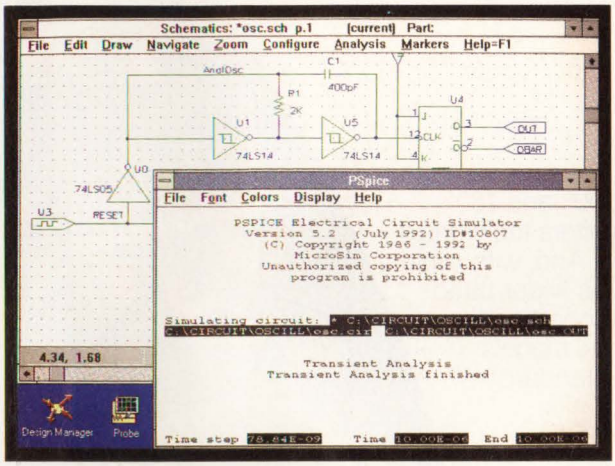
For more information, contact Marilyn Potes at the IEEE Computer Society, Los Alamitos, CA, (714) 821-8380.

Unit combines curve tracer and parameter analyzer

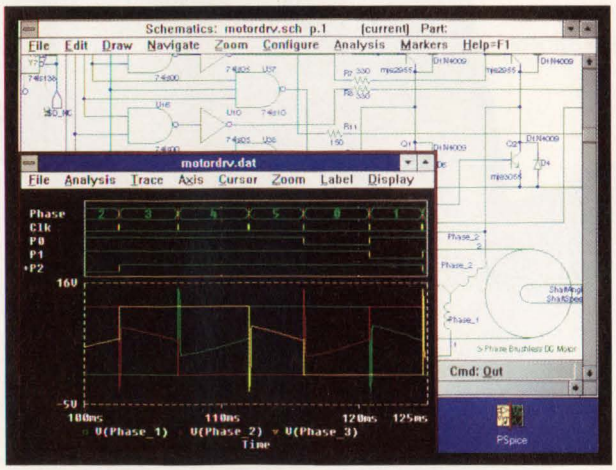
Some of the most important information that designers and users of ICs and discrete semiconductor devices need to learn about these parts has nothing to do with high-frequency or switching properties. The information is contained in the devices' dc parameters and quasistatic characteristics. Traditionally, measuring these dc and low-frequency values has required two types of instruments: a parameter analyzer and a curve tracer. Tektronix's $24,950 372 Semiconductor Workbench combines the functions of these old standbys into a single unit. The system incorporates two source/measure units. Each unit supplies 200V and 400 mA (10W max) and measures current with 25-fA resolution. These capabilities suit bipolar, CMOS, BiCMOS, and GaAs devices. The user interface, which resembles that of a curve tracer, makes the effects of operating-condition changes immediately visible. According to the vendor, the system's ability to perform pass/fail testing is not shared by any parameter analyzer or curve tracer. Moreover, a TTL parallel port lets the system control a device handler. An MS-DOS-compatible floppy-disk drive lets you export files containing the graphical information the system displays on its CRT in any of three industry-standard formats. Tektronix Inc, Beaverton, OR, (800) 426-2200.

Get the Jump on Windowed Environments for Circuit Design!

We did! Now you can too!! All you need is the Design Center™ running under Microsoft Windows.



Schematic capture and PSpice simulation of a mixed analog/digital oscillator



Graphical analysis of the analog and digital signals produced by a DC brushless motor simulation

Native Microsoft Windows Applications — Available Today

The **Design Center** provides you with the analog and digital circuit design software you need, running as fully integrated Microsoft Windows applications on the PC. Whether you are capturing schematics, simulating circuits with PSpice, or graphically analyzing waveforms, you have all of the convenience of windowed environments at your fingertips: relocatable and scalable windows, pull-down menus, dialog boxes, on-line help, and the ability to freely move between different windowed applications.

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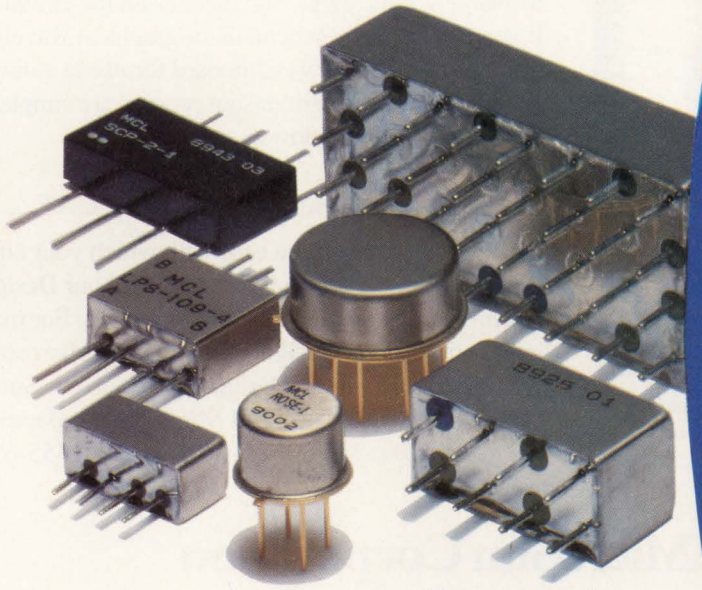
Available for use in military and commercial requirements, models include plug-in, flat-pack, surface-mount, connectorized standard and custom designs. New ultra-miniature surface mount units provide excellent solutions in cellular communications, GPS receivers, Satcom receivers, wireless communications, and cable systems.

All units come with a one-year guarantee and unprecedented "skinny" sigma unit-to-unit and production run-to-production run repeatability. All catalog models guaranteed to ship in one week. Mini-Circuits...dedicated to exceed our customers' expectations.



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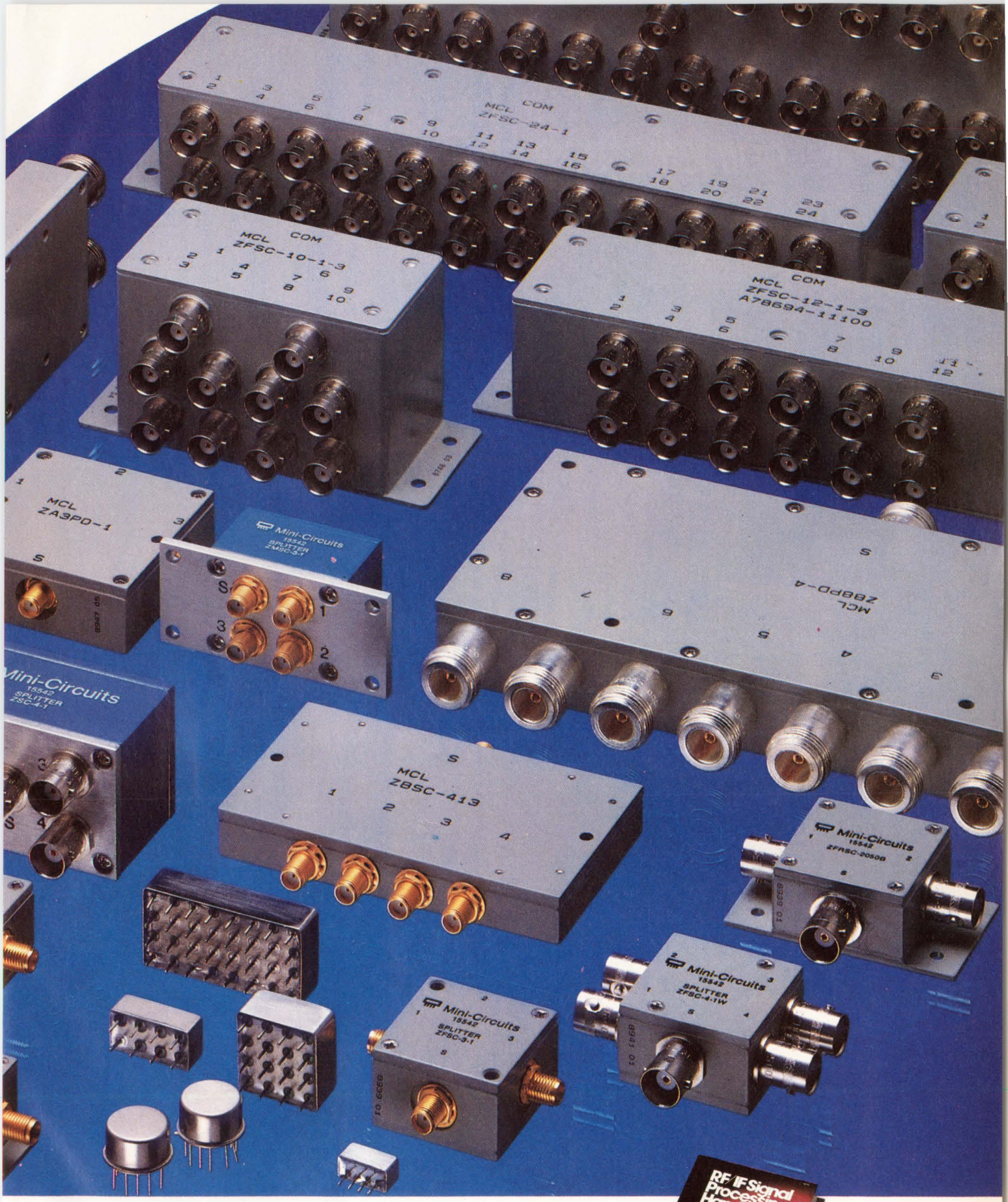
F134 REV. C



For detailed specs on all Mini-Circuits products refer to
• THOMAS REGISTER Vol. 23 • MICROWAVES PRODUCT DIRECTORY
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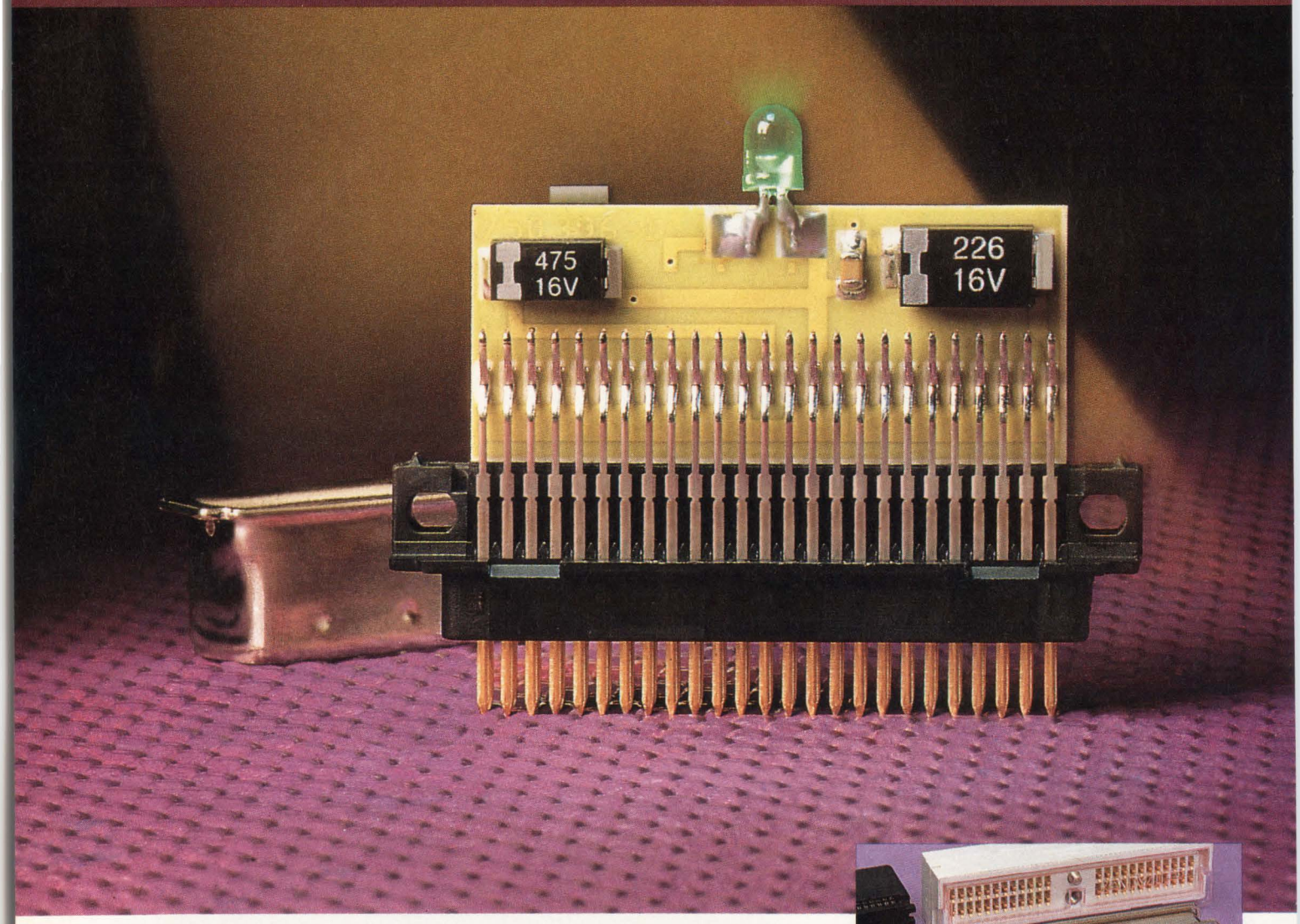
CIRCLE NO. 18

F134 REV. C

Ours is also engineered to terminate the competition.



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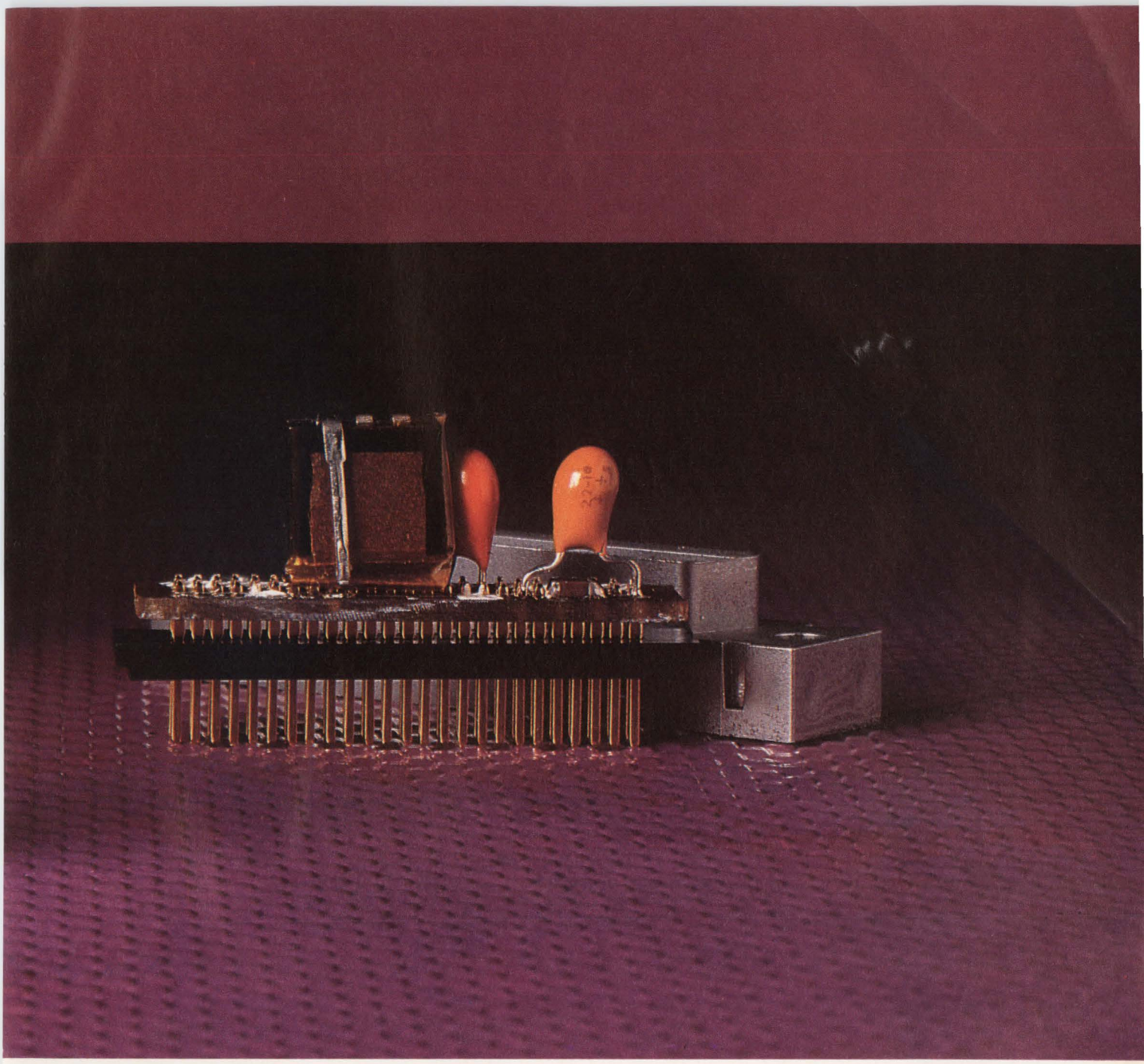


It isn't hard to see why our terminators are catching on with both manufacturers and installers of network systems. The engineering differences are obvious: ours are simply better.

Take the AMPLIMITE .050 Series Terminator, above left. All components are surface mounted (greater inherent reliability). We use a ceramic substrate (better heat dissipation), a front metal shell (more effective shielding), and a variety of shielded and unshielded backshells. Better engineering gives us a major performance advantage while keeping production simple–which is why we're able to offer custom configurations, and optional LEDs. And why we can keep our prices very competitive.

We offer the styles and types you want, too. Choose from single-ended passive or active, differential, bus and tag, even the latest FPT (forced perfect termination) types. Standard versions conform to SCSI-1, SCSI-2, SCSI-3, IPI-1, and IPI-2.

We also have the engineering know-how to offer all the options and specials you need, including loopbacks and feed-throughs, shielding, post molding, and your choice of mounting hardware.

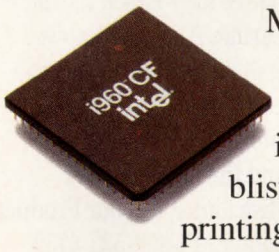
Naturally, you can't compare all those variations with what our competitors offer, but you can compare what matters. Do a one-on-one with your specific application, and see for yourself the difference in engineering. And who knows? That other terminator might become a collector's item.

For more information on AMP terminators and the name of your nearby AMP distributor, call our Product Information Center at 1-800-522-6752 (fax 717-986-7575). AMP Incorporated, Harrisburg, PA 17105-3608. In Canada, call 416-475-6222.

CIRCLE NO. 19

AMP

We've just tested the performance of our new i960 CF processor.



Make no mistake. This is no middle-of-the-road processor. It's our new superscalar i960™ CF chip. And it delivers blistering speed to your high-end printing, imaging, communications and networking applications. Simply put, it outruns every 32-bit embedded processor on the market—and we have over 25 benchmarks to prove it.

You see, only our i960 RISC architecture brings superscalar processing with multiple operations per clock to embedded applications. Our new i960 CF processor is highly integrated with optimized data and instruction caches for throughput up to

twice that of our i960 CA chip. Which makes it the most advanced technology available for embedded applications.

If you're already using our i960 CA processor, you can quickly shift up to higher performance with full code and pin compatibility. And, of course, we offer a comprehensive array of Solutions960 development tools to further speed up your design process.

So step on it. Call 800-548-4725 and ask for literature packet A9A51 for complete benchmarks. And learn what your applications can do with a faster engine.

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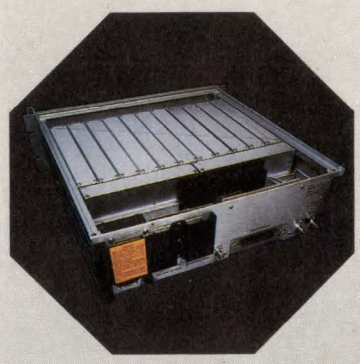
CIRCLE NO. 20

The Race for Quality . . .



They say in the race for quality there's no finish line. But there are milestones, and we passed some long ago:

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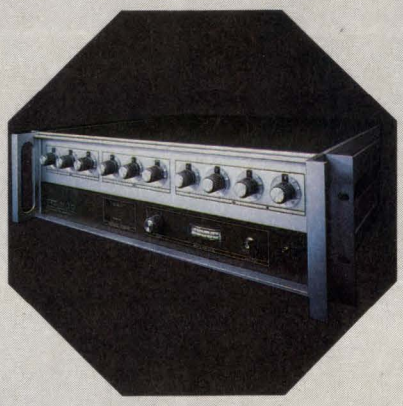

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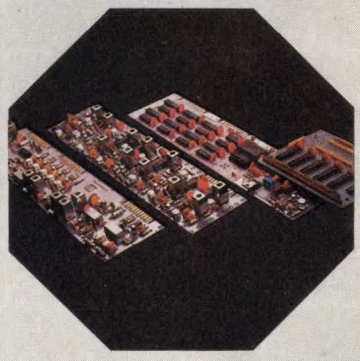

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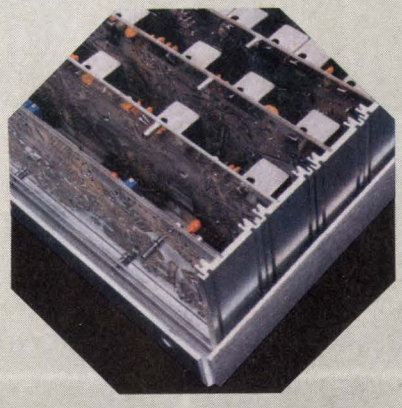

CIRCLE NO. 22

Distinguish between multitasking and task switching

In J D Mosley's article, "Multimedia" (EDN, March 16, 1992, pg 100), she did not distinguish between multitasking and task switching. A simple test for distinguishing them is to place a clock with a second hand on the screen and go to another task. If the clock stops, the operation is task switching. Many big company programs that claim to be multitasking fail this test.

Of course, a single-processor computer cannot really multitask because all it can do is switch from one task to another. But the present convention seems to be that the computer is multitasking if there is no noticeable delay in any task execution. And in the sense of multimedia, the second task must be a different media form from the first.

In the larger sense, a true multimedia, multitasking machine uses several different types of processors, each designed for a particular medium. Mosley chose to concentrate on attaining this by board and program additions. In the process, she ignored the computer, which handles multiple tasks and multiple media right out of the box. I refer, of course, to the Amiga, called by *Byte* "the most capable multimedia platform you can get in a single box." And this is true even for the bottom of the line, at prices below the median level of the boards she lists. The top of the line, expanded, will compete in performance with the top combination of the computer, board, and program she lists—and be much lower in price.

R P Haviland, PE, Retired
Daytona Beach, FL

Reader spots error in Hands-On FPGA Project

In Part 1 of the Hands-On FPGA Project (EDN, April 9, 1992, pg 101), I made an error where I stated that the ALS software automatically combines 2-input gates with flip-flops and latches wherever possible. The software apparently makes the combinations for the Act 2 family, but not for the Act 1 family. You have to make the combinations in the schematic on Act 1 designs. I'd like to thank John Conners at Marquette Electronics, Milwaukee, WI, for bringing the error to my attention.

Doug Conner
EDN Technical Editor

Add it to your Mips list

In our Special Report, Third-generation RISC processors (EDN, March 30, 1992), we inadvertently omitted a vendor from the manufacturers list on pg 103. To the list of companies that produce the Mips R4000, add Toshiba America Electronic Components. The company is located at 9775 Toledo Way, Irvine, CA 92718; contact them by phone at (714) 455-2000.

Address correction

Following is the correct address and phone number for Northern Telecom Inc (EDN, March 2, 1992, pg 62):
Northern Telecom Inc
105 Laurentian Blvd
St Laurent, Quebec H4N 2M3, Canada
(514) 744-8755
Contact: Demetri Elias.

WHAT'S COMING IN EDN

In the August 13 issue of EDN News Edition, look for an article on DSP ICs. In the Careers section of the tabloid you'll find an article on jobs in the video-conferencing area. EDN News Edition's Management Series continues with a story on how to motivate employees.

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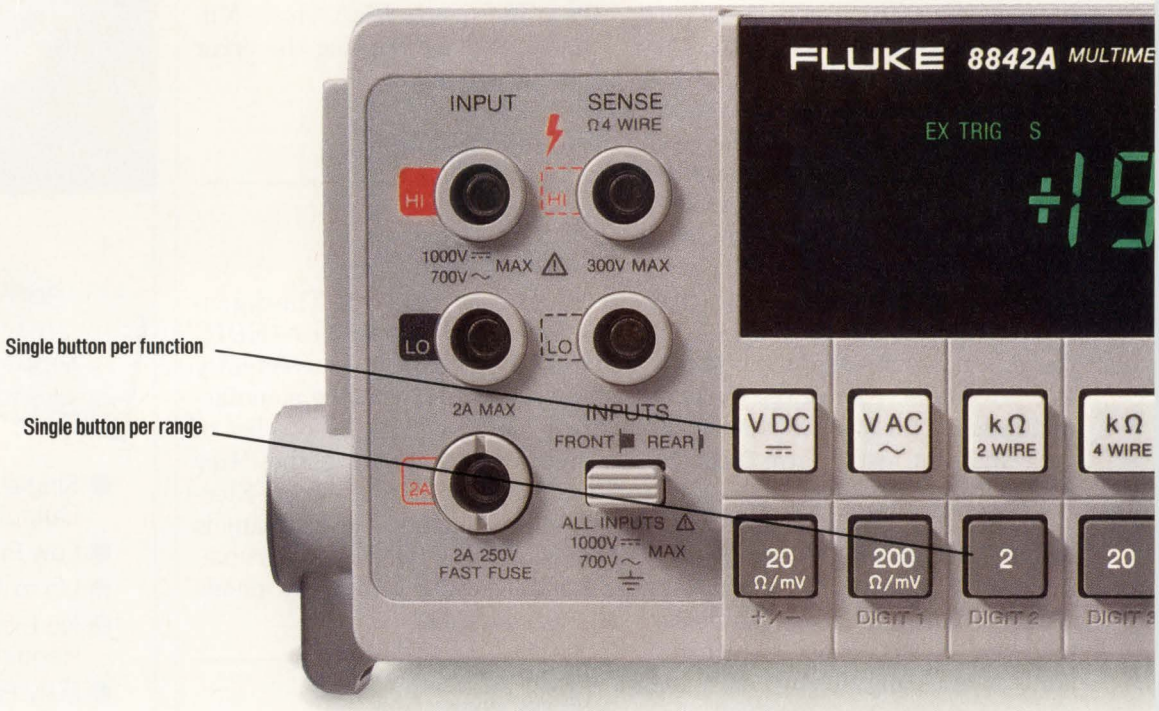

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Input Impedance @ 20V	10,000 MΩ	10MΩ
dV Ranges	Six: 20 mV – 1000V	Five: 100 mV – 1000V
Isolation, Common Mode Voltage	1000V dc	500V dc
Basic One Year DC Accuracy	±0.003%	±0.0035%

Then there's interference. Will common or normal mode noise

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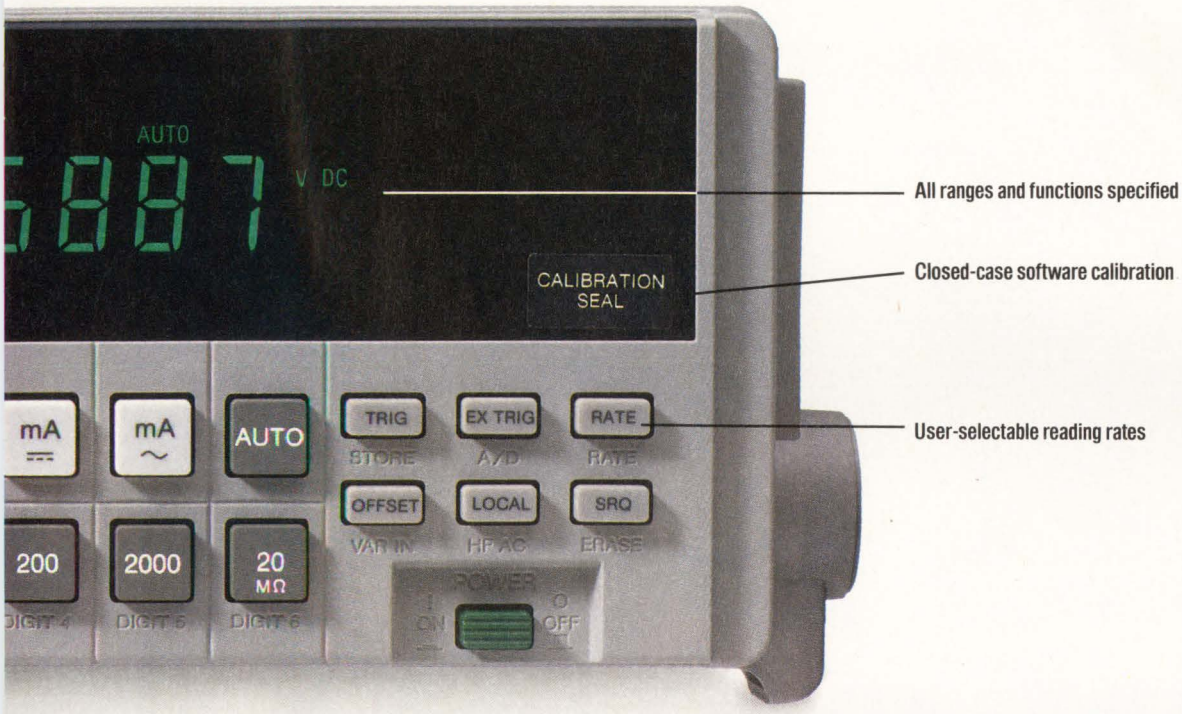

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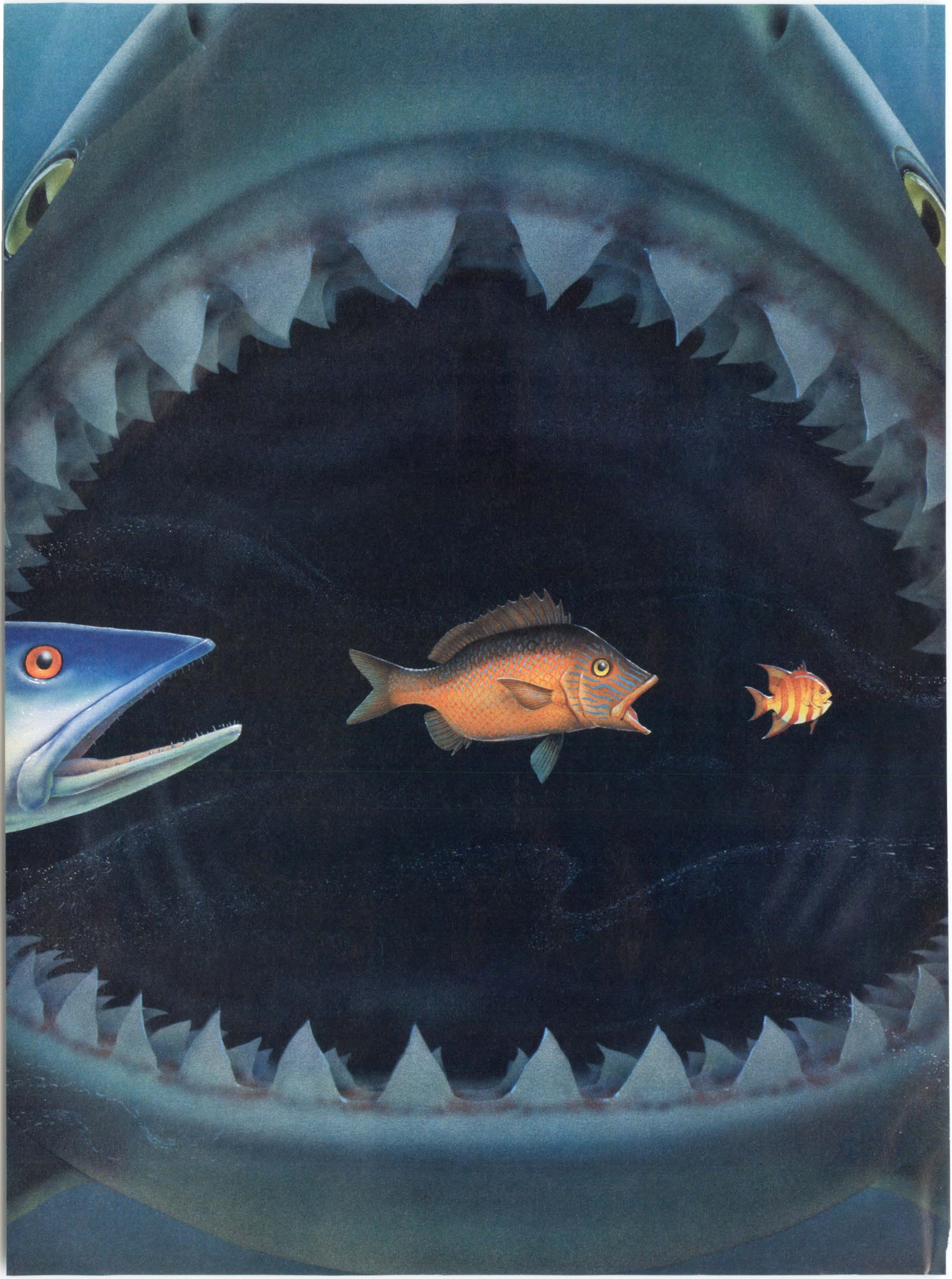

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MCM6706A	**MCM6705A**	**MCM6708A**	**MCM6709A■**	**MCM67082A▲**
32K x 8 bit	32K x 9 bit	64K x 4 bit	64K x 4 bit	64K x 4 bit
8, 10, 12ns	10, 12ns	8, 10, 12ns	8, 10, 12ns	10, 12ns

●3Q92 ■Output Enable ▲Separate I/O

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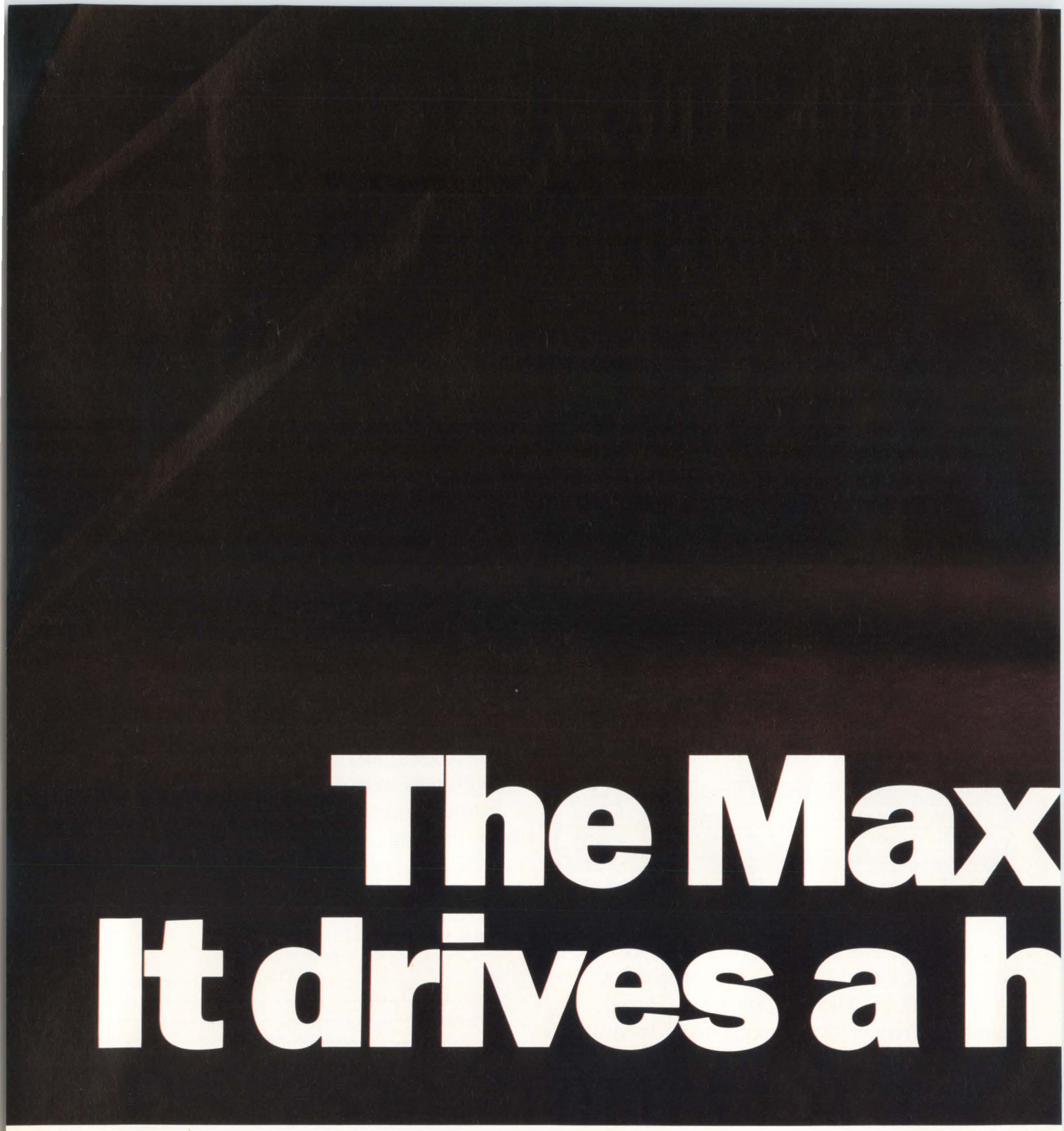

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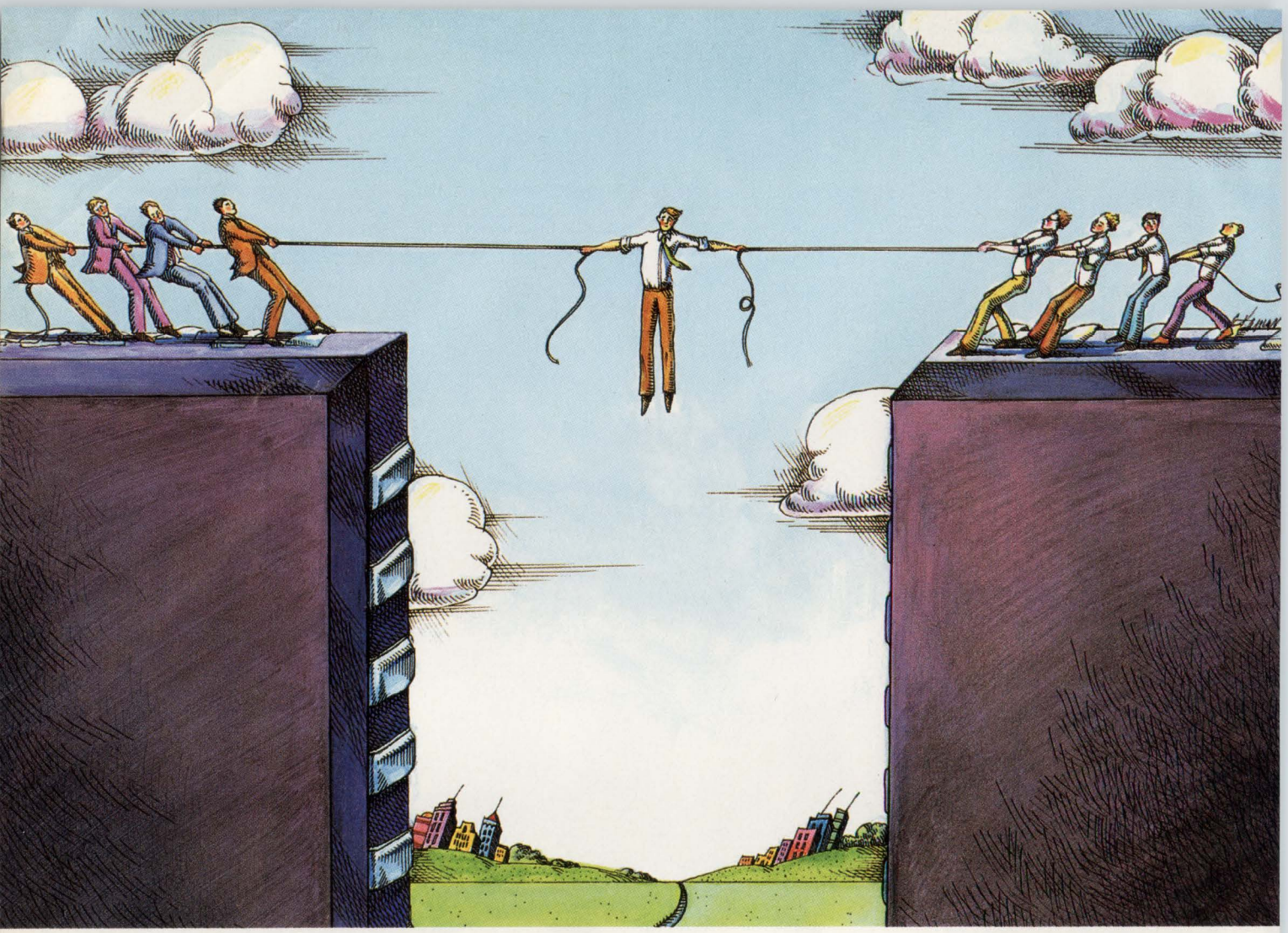

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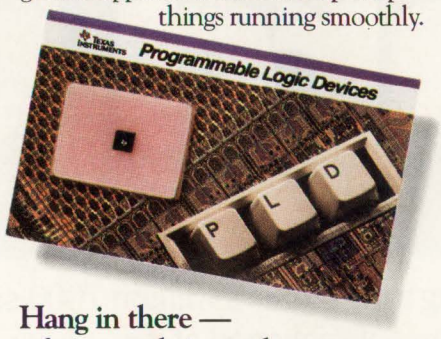

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TEXAS INSTRUMENTS

Science by mail

I remember as a teenager the excitement of getting a package of electronic parts from Lafayette Radio, or a new kit to assemble from Heathkit. It seemed that there was always something interesting in the mail. Today, young people can also participate in "science by mail" through a program sponsored by the Museum of Science in Boston. The program also lets many of us who are young at heart and mind enjoy science and creative thinking right along with the kids. The science program provides a way to help youngsters get interested in science and keep them interested. It can be a lot of fun—and a challenge—for adults, too.

The museum's Science-by-Mail program is an international program meant for young people between about 9 and 14 years of age. Last year, about 24,000 children took part. Three times during the year, the kids in the program receive a science-experiment package by mail. Past packages include one on communications and another on ecology and natural resources. Not only can the kids do science experiments with the simple materials and apparatus that come in each kit, but the kits ask them to think about solving problems. For example, how would you dispose of trash accumulated during a trip to Mars? Or, how would you invent a time-keeping device?

The kids' projects, experiments, and solutions are only part of the program, which encourages participation by parents and teachers. Most of the experimenting takes place during science classes and under teacher supervision. The kids can experiment on their own, too. In addition, a very important part of the program involves scientists and engineers who act as pen-pal mentors for the kids. Typically, four young people work as a team on each experiment kit. During and after their work, they correspond with their mentor, who critiques their work, offers suggestions, and may stimulate more experiments and problem solving.

So, how do you get involved? First, you can sponsor a Science-by-Mail team. If you know three or four young people who would like to try the science kits as a team, sponsoring a group costs $44 for a year. The fee includes a scientist or engineer pen pal. If your company would like to get involved further, consider sponsoring an entire science class. Most important of all, seriously consider being one of the scientist or engineer pen pals. Working with the kids can be an enjoyable—and challenging—experience. It requires a commitment to communicate with as many as five teams of kids for each of the three annual science kits. You can get as involved as you want, even communicating as the projects unfold and continuing your correspondence after the kids finish their formal work. There are 2500 volunteer mentors in the program today.

Many museums throughout the USA have Science-by-Mail chapters, and there are international chapters as well. For information about a chapter nearby, or for more information about becoming a mentor, write to Science-by-Mail, Museum of Science, Science Park, Boston, MA 02114. Phone numbers are (617) 589-0437, or (800) 729-3300; fax requests to (617) 589-0454. The entire program is nonprofit and is underwritten by individuals, corporations, and the National Science Foundation.

When you sign up as a mentor, drop me a note and let me know what your experiences are like. I'll put together some of the brief reports and tell the rest of the readers about the fun and excitement they're missing.

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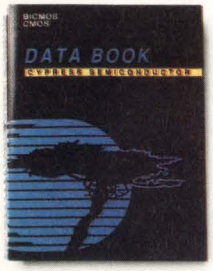

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ADC ARCHITECTURES

Speed-resolution tradeoff key to choosing ADCs

DAVE PRYCE, Contributing Editor

The diverse applications for A/D converters demand that you understand the basic differences in the available architectures.

Many factors influence the choice of an A/D converter for a given application, and among the most important are resolution and speed. To a great extent, the converter's architecture determines the values for these two key parameters and, to a lesser extent, influences other critical parameters. In selecting an A/D converter, designers need to understand the advantages and disadvantages of the various converter types and the tradeoffs associated with their respective architectures. Converter types include successive approximation, flash, subranging, integrating, and sigma-delta.

Regardless of the type of converter you select, the speed and resolution parameters often tend to conflict. For example, flash converters offer blazing speeds—as fast as 500 Msamples/sec at the extreme limit—but their resolution is limited to a maximum of 8 to 10 bits. Conversely, sigma-delta converters have a maximum-speed limitation of about 100 ksamples/sec but their typical resolution is 16 to 18 bits. Satisfying a wide range of applications, successive-approximation converters exhibit speeds from 10 ksamples/sec to about 1 Msample/sec and resolutions from 8 to 18 bits. However, the resolution is limited to about 12 bits at the higher speeds.

As the successive-approximation example implies, the speed-resolution tradeoff tends to exist even among converters of the same type. Although a converter's architecture determines its overall speed and resolution limits, you can't usually obtain both the highest possible speed and the highest possible resolution with the same device.

For example, constructing a flash converter having a speed of 300 Msamples/sec and a resolution of 12 bits may be theoretically possible, but the overwhelming burden of the required 4095 comparators makes such a converter a practical impossibility either in monolithic or hybrid form. Flash converters having 12-bit resolution do not exist, and you're not likely to ever see one. To more completely understand the speed-resolution conundrum and the advantages and disadvantages of each type of converter, it is instructive to look at

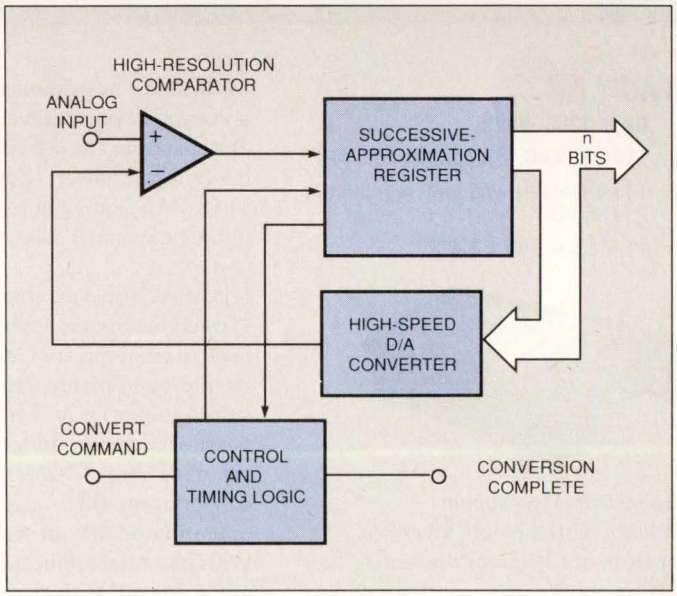

Fig 1—A successive-approximation converter compares an analog input with the output of an n-bit DAC in a series of successive approximations. At the end of the conversion, the contents of the register output a binary word. This type of converter has a speed-resolution limit of about 1 Msample/sec and 12 bits.

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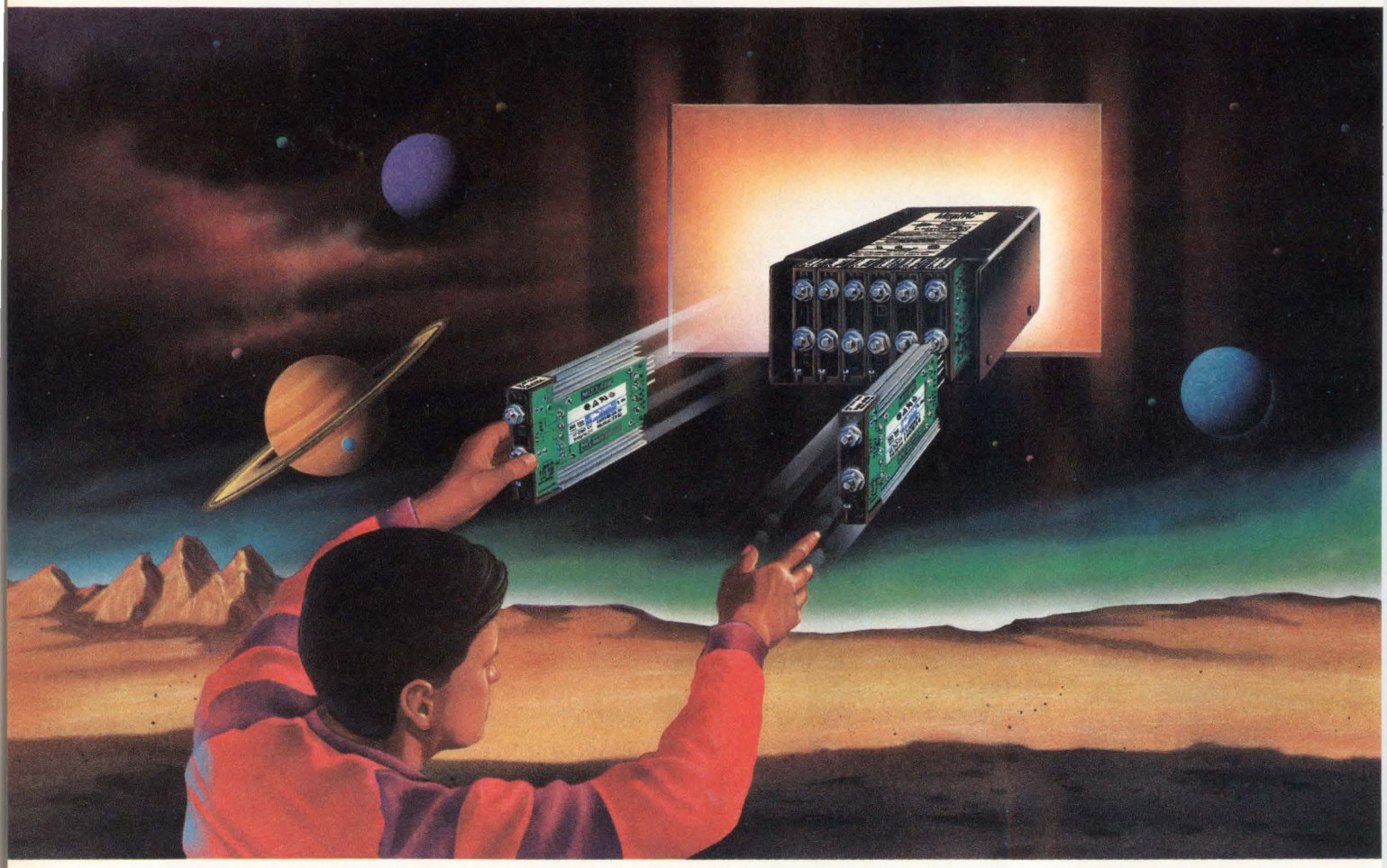

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ADC ARCHITECTURES

the basic characteristics of the individual architectures.

By far the most universally popular converter is the successive-approximation type, which can satisfy a wide range of applications. Used in everything from modems to missiles, this type of converter owes its popularity to its ability to combine relatively high resolution and speed with low cost.

As **Fig 1** shows, the successive-approximation converter uses a comparator, a successive-approximation register, a reference DAC, and control and timing logic to perform n single-bit conversions. The ADC compares the analog input with the output of an n-bit DAC in a series of successive approximations. The approximations start with the most significant bit (MSB) and continue through the least significant bit (LSB) until the output of the DAC is within 0.5 LSB of the input and all bits are latched into the corresponding states. At the end of the conversion, the contents of the register form an n-bit binary word corresponding to the magnitude of the input signal.

During the conversion, each of the bit decisions takes a clock period. As a result, the allowable clock frequency and the number of bits determine the maximum conversion time of a successive-approximation converter. The maximum clock frequency is limited by the DAC settling time, the successive-approximation register's setup time, and the clock-to-data output delay. Depending on the nature of the analog input signal, the converter sometimes needs a sample-and-hold (S/H) or track-and-hold (T/H) circuit. The determining factor is whether the input signal is stable during the conversion period. Many of the newer successive-approximation converters include an on-chip T/H circuit.

The successive-approximation converter has a speed-resolution limit of approximately 1 Msample/sec and 12 bits. Resolutions of 16 bits and higher are possible at slower speeds. The architectural simplicity of the converter makes manufacturing the device in monolithic form easy. Thus, successive-approximation converters are lower in cost than similarly performing hybrid versions as well as most other monolithic converters that have a different architecture. Many industry-standard types having a wide range of speed and resolution combinations are available from several manufacturers.

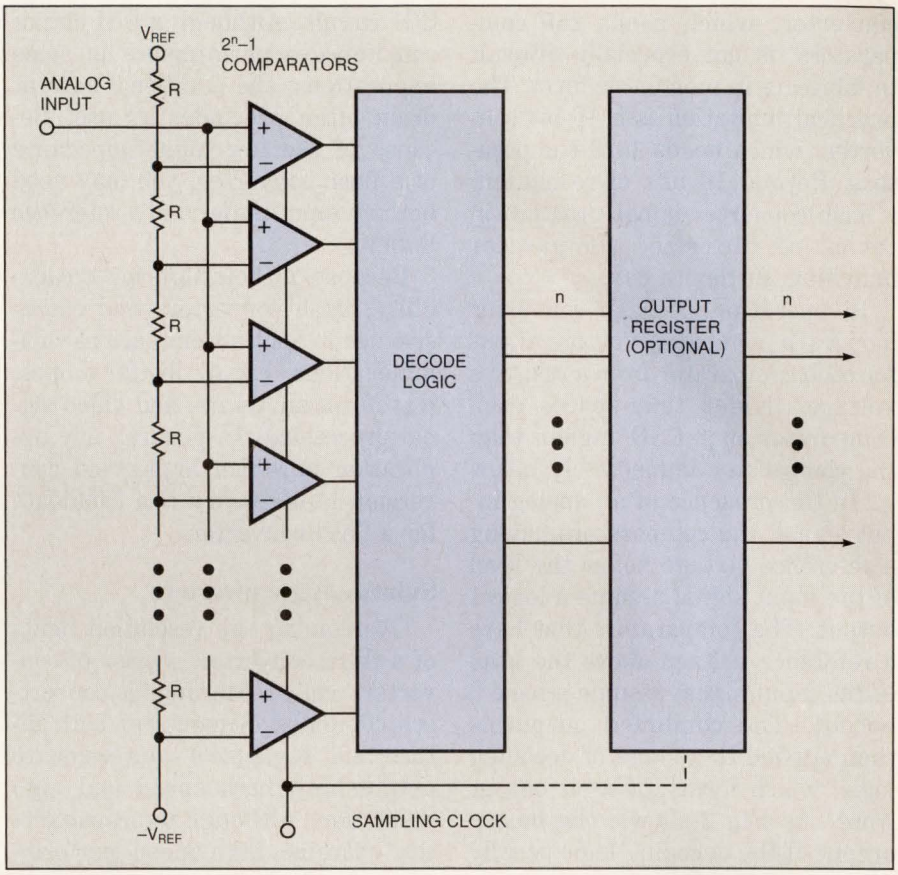

Fig 2—A flash converter processes all bits at essentially the same time rather than through a series of individual steps. Sampling rates of 75 to 100 Msamples/sec are common, and some converters can go as high as 500 Msamples/sec. The main disadvantage of the flash converter is its 10-bit resolution limit, which is due to the large numbers of comparators needed.

Flash converters

The successive-approximation converter uses sequential conversion; a flash converter provides direct conversion. That is, it processes all bits at essentially the same time rather than through a series of individual steps. The parallel nature of the conversion cycle makes the flash converter capable of very high speeds. The speed range extends from about 1 Msample/sec to as high as 500 Msamples/sec for some devices. Sampling rates of 75 to 100 Msamples/sec are common. The main disadvantage of the flash converter is its 10-bit resolution limit.

This limitation is inherent in the flash converter's architecture (**Fig 2**). The flash converter needs 2^n-1 comparators, where n is the number of bits. A 4-bit flash converter, which needs only 15 comparators, is easy to construct. Even an 8-bit

ADC ARCHITECTURES

converter, which needs 255 comparators, is not especially difficult to fabricate in monolithic form. The practical limitation is a 10-bit converter, which needs 1023 comparators. Beyond 10 bits of resolution, a flash converter is not practical in terms of die size, comparator matching, or device cost.

In operation, a flash converter derives a reference-voltage input for each comparator from a resistive voltage divider that spaces each comparator one LSB higher than the comparator immediately below it. In the presence of an analog input signal, the comparators having a reference voltage below the level of the input signal assume a logic 1 output. The comparators that have a reference voltage above the level of the input signal assume a logic 0 output. The combined output is then applied to a stage of decoding logic, which forms an n-bit output word. As **Fig 2** shows, the binary output of the decoding logic usually drives an on-chip output register, or latch.

Flash converters are sampling devices and do not usually need a S/H circuit. Although a S/H circuit can improve performance in some applications, the additional current drain often precludes its use. Because of the low input impedance of a flash converter, you may need both an input buffer and a reference buffer.

Because of their high-speed capability, flash converters find extensive use in applications such as communications, radar, digital scopes, waveform analyzers, and video signal processing. In general, any application in which high-speed conversion is necessary is a candidate for a flash converter.

Subranging converters

Overcoming the resolution limits of a flash converter, a class of converters called subranging converters combines elements of both direct and sequential conversion to obtain both high speed and high resolution. Although not capable of the extreme high-speed performance of a flash converter or the absolute resolution limits of other types of converters, the subranging converter offers an excellent compromise. The converters offer resolutions as high as 16 bits and speeds as fast as 40 Msamples/sec. In general, subranging converters provide remarkable speed-resolution characteristics, particularly at higher speeds.

Subranging converters typically use two or more steps of flash conversion but have an architecture that has a singular advantage over flash converters—a great reduction in the number of comparators. In the simplified 8-bit example of **Fig 3**, the two 4-bit flash converters need only 30 to 32 comparators. By contrast, a single 8-bit flash converter would need 255 comparators. The reduced number of comparators a subranging converter needs greatly reduces chip size and power consumption. Although the 8-bit flash converter and the 8-bit subranging converter have the same resolution, to equal the overall speed of a single 8-bit flash converter, the two 4-bit converters in the subranging converter must be twice as fast.

In **Fig 3**'s 2-step subranging circuit, the first flash converter digitizes the first four bits and applies the binary output to the 4-bit DAC. The summing amplifier then subtracts the DAC's analog output from the held analog input; amplifies the resulting signal, or residue; and applies it to the second 4-bit flash converter. The subranging converter then combines the outputs of the two 4-bit flash converters into a single 8-bit binary word. If the amplified residue signal doesn't fill the range of the second flash converter, the converter can exhibit nonlinearities and missing codes.

Most subranging converters are more complex than this basic example and include digital error-correction logic to minimize nonlinearities and the possibility of missing codes. The error-correction logic, which is usually just an adder circuit, works

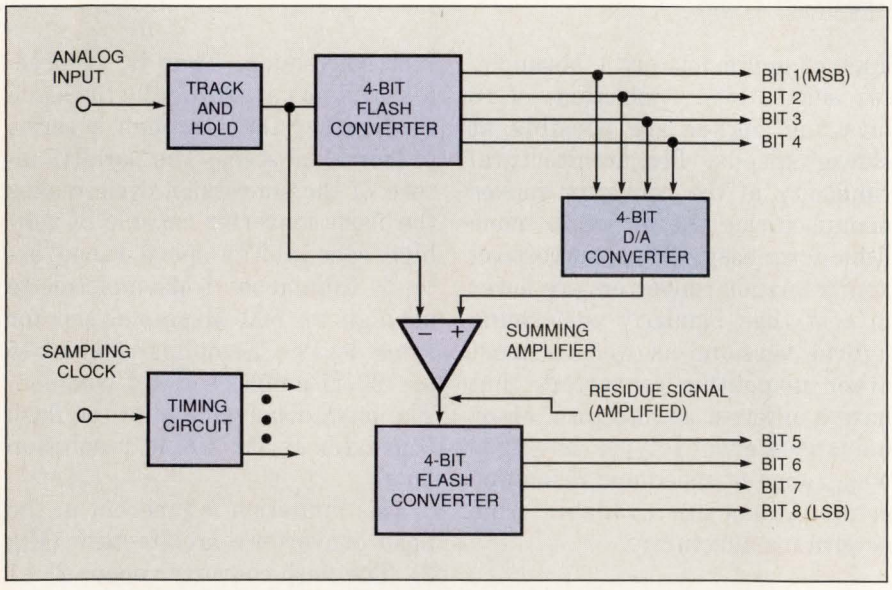

Fig 3—In this simplified example of an 8-bit subranging converter, the two 4-bit flash converters need only 30 to 32 comparators. By contrast, a single 8-bit flash converter would need 255 comparators. Subranging converters permit resolutions as high as 16 bits and speeds as fast as 40 Msamples/sec.

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together with the second flash converter's extra-range capability to correct most of the output-data errors inherent in an uncorrected subranging converter.

Subranging converters can take several forms, including those that use more than two flash converters and those that use only one flash converter. In the latter type, which is called a recursive subranging converter, a single flash converter makes multiple passes until the device obtains the desired resolution. The final result appears at the digital output. To some extent, the multiple passes made by a recursive subranging converter resemble the action of the successive-approximation converter.

All subranging converters require a S/H circuit—some types use several. The accuracy of this type of converter is limited by that of the internal DAC or DACs. Subranging converters are available that have resolutions of 8 to 16 bits and speed ratings of 100 ksamples/sec to 40 Msamples/sec. Although not as fast as a true flash converter, subranging converters offer an effective compromise in applications that require high-speed operation at resolutions greater than 8 or 10 bits. With the addition of image capturing, applications for subranging converters are generally the same as those for a flash converter.

Integrating converters

The converters discussed thus far can all digitize analog inputs at speeds of at least 10 ksamples/sec, typically at much faster rates. In stark contrast with these relative speed demons, the typical 10-sample/sec integrating converter is as slow as the proverbial turtle. Useful for precisely measuring slowly varying signals, the integrating converter finds application in digital voltmeters and processing the output of some transducers. The two

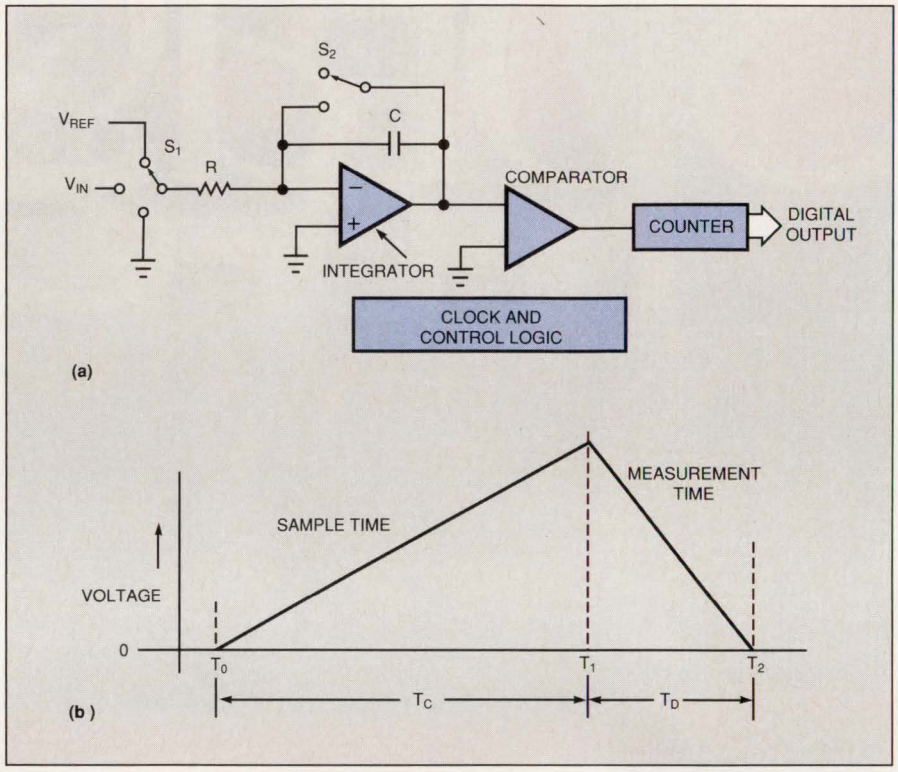

Fig 4—This dual-slope integrating converter (a) contains an analog integrator, a comparator, a counter, a clock, and control logic. The converter's characteristic charge-discharge (T_C/T_D) waveform is shown in (b). As the name implies, the output of an integrating converter represents the average value of an input voltage over a fixed time period.

common variations of the integrating converter are the dual-slope type and the charge-balance type. Designers typically use the latter type as a voltage-to-frequency converter.

As the name implies, the output of an integrating converter represents the average value of an input voltage over a fixed period of time. This integration eliminates the need for a S/H circuit to "capture" the input signal during the measurement period. The dual-slope converter contains an analog integrator, a comparator, a counter, a clock, and control logic (**Fig 4a**). **Fig 4b** shows the circuit's characteristic charge/discharge (T_C/T_D) waveform.

To hold the integrator in the discharged state, switch S_1 initially connects resistor R to ground, and S_2 shorts out capacitor C. To start the conversion, S_1 connects R to the unknown input voltage, and S_2 opens to let C charge. The clock and the counter control the integration time. At the end of the integration period, S_1 connects a known reference voltage to R, and the capacitor discharges until the comparator detects that the integrator has reached the original starting point. The counter measures the amount of time the capacitor takes to discharge.

Because the values of the resistor and integrating capacitor and the frequency of the clock remain the same for both the charge and discharge cycles, the ratio of the charge time to the discharge time is equal to the ratio of the reference voltage to the unknown input voltage. The absolute values of R, C, and the clock frequency do not affect the conversion accuracy. Moreover, any noise on the input signal is integrated over the entire sampling period, which imparts a high

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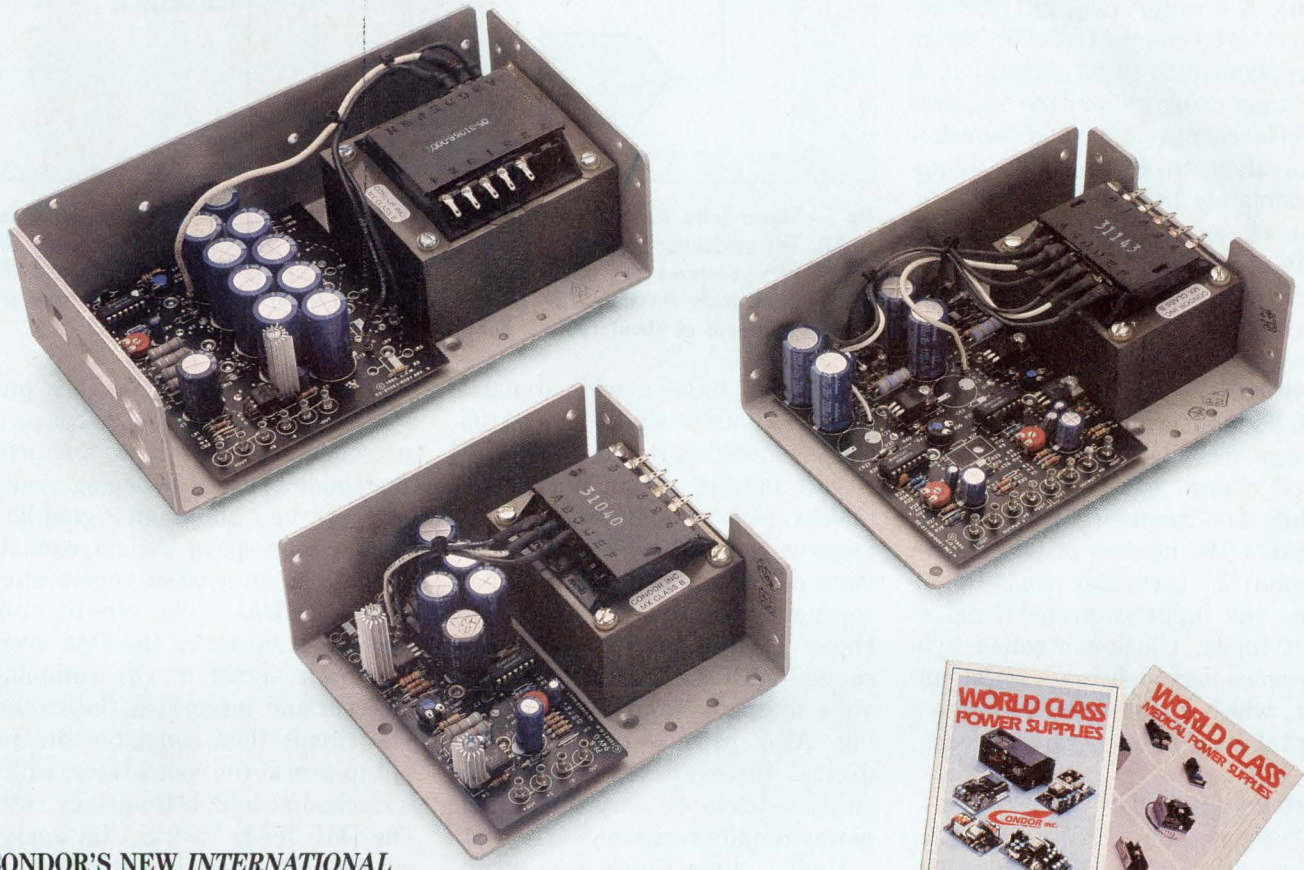

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level of noise rejection to the converter. By making the signal-integration period an integral multiple of the line-frequency period, you can obtain excellent 60-Hz noise rejection.

Typically used in digital voltmeters to provide a display of 3½ to 5½ digits, a dual-slope integrating converter can attain high resolutions. A 3½-digit display (1999) requires 4000 counts (±2000), which is equivalent to 12-bit resolution. A 5½-digit display (199,999) requires 400,000 counts (±200,000), which is equivalent to a resolution of approximately 18.6 bits.

A charge-balance integrating converter incorporates many of the same elements as the dual-slope converter but uses a free-running integrator in a feedback loop. The converter continually attempts to null its input by subtracting precise charge packets when the accumulated charge exceeds a reference value. The frequency of the charge packets (the number of packets per second) the converter needs to balance the input is proportional to that input. Clock-controlled synchronous logic delivers a serial output, which a counter converts to a digital word in many applications.

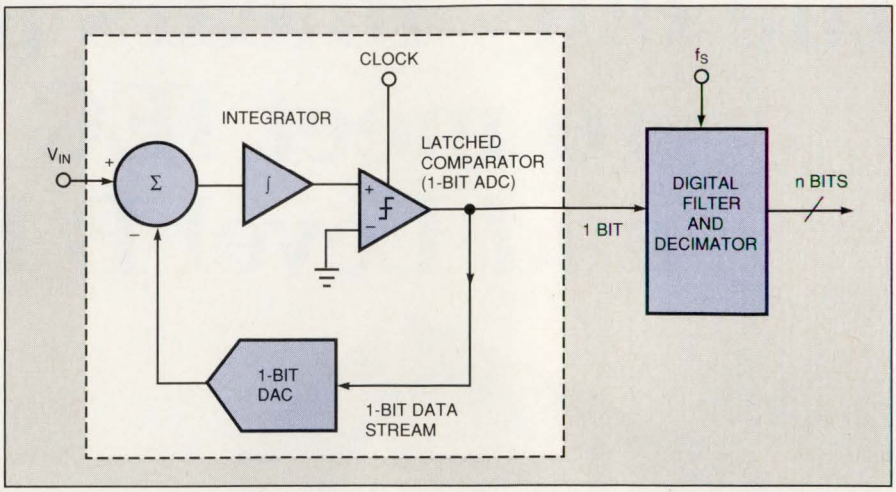

Fig 5—Sigma-delta converters include an analog modulator and a digital-filter/decimator circuit. The modulator converts the input signal to a 1-bit, high-speed data stream. The digital filter removes the high-frequency noise generated by the modulator, and the decimator digitally resamples the filtered output at a lower rate. These converters are limited to speeds of about 100 kHz but have resolutions as high as 20 bits.

Sigma-delta converters

The converters discussed thus far offer a choice of architectures to satisfy nearly any conceivable need, but a relatively new type—the sigma-delta converter—is making its presence known in digital audio and digital signal-processing applications. A close relative of integrating converters, a sigma-delta converter—sometimes called a bit-stream converter—is a 1-bit converter that uses oversampling and noise shaping as the key elements to its operation. Inherently linear because of the 1-bit conversion process, these converters typically have resolutions of 16 to 20 bits.

Because of their high resolution and a good S/N ratio, sigma-delta converters have a wide dynamic range. Another advantage is that these converters do not need a S/H circuit because of their high-frequency 1-bit sampling rate. On the negative side of the ledger, sigma-delta converters are limited to low-frequency applications—typically those in the 10-Hz to 100-kHz range—such as industrial control, voice digitizing, and audio processing. Also, because of the complex digital filtering, the monolithic chips tend to be large and their power requirements high.

Unlike other converters, sigma-delta converters handle conversion, or quantization, noise by moving most of it outside the frequency band of the input signal via oversampling and digital filtering. This technique allows accurate conversion in the desired frequency band but provides no useful information for frequencies outside the specified bandwidth. Sigma-delta converters have bandwidths that are narrower than those of a successive-approximation converter but much wider than those of a dual-slope integrating converter.

The basic sigma-delta converter has three functional blocks: an analog modulator, a digital filter, and a decimator (**Fig 5**). Most converters combine the latter two functions in a single block. The analog modulator converts the input signal into a 1-bit, high-speed data stream. It contains an integrator, comparator, and 1-bit DAC. The circuit subtracts the output of the DAC from the input signal at the summing junction and integrates the result. The circuit then compares the result to zero at the comparator, which is clocked at a high-frequency rate. The DAC feeds back a 1-bit analog representation of the comparator's output—a serial stream of bits.

The comparator generates a single bit containing the quantization noise associated with the input signal. Because the oversampling action of the clocked comparator converts the signal to a high frequency that varies around the average value of the input, the quantization noise increases with frequency. In effect, the analog modulator acts like a lowpass filter for the signal and a highpass filter for the noise. This noise-shaping action moves the noise outside the range of the sampled signal.

The digital-filter/decimator block

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performs three functions. The digital filter removes the high-frequency noise the modulator generates and also acts as an antialiasing filter with respect to the final sampling rate. The decimator then performs the final data reduction by digitally resampling the filtered output at a lower rate. This process reduces the oversampled bit stream to the converter's low-frequency output rate but at high resolution.

The sigma-delta converter of **Fig 5** is the simplest form possible. Most practical converters contain second-order modulators having two integrators, and some use a multibit DAC in the feedback path. For an in-depth treatment of oversampling converters, see **Refs 1** and **2**.

For an at-a-glance view of the speed-resolution limits of the various A/D converters, see **Fig 6**. Prepared by Doug Grant of Analog Devices, this graph depicts the typical speed and resolution characteristics for successive-approximation, flash, subranging, integrating, and sigma-delta converters. By referring to this graph, you can quickly determine what type or types of converters are likely to satisfy the de-

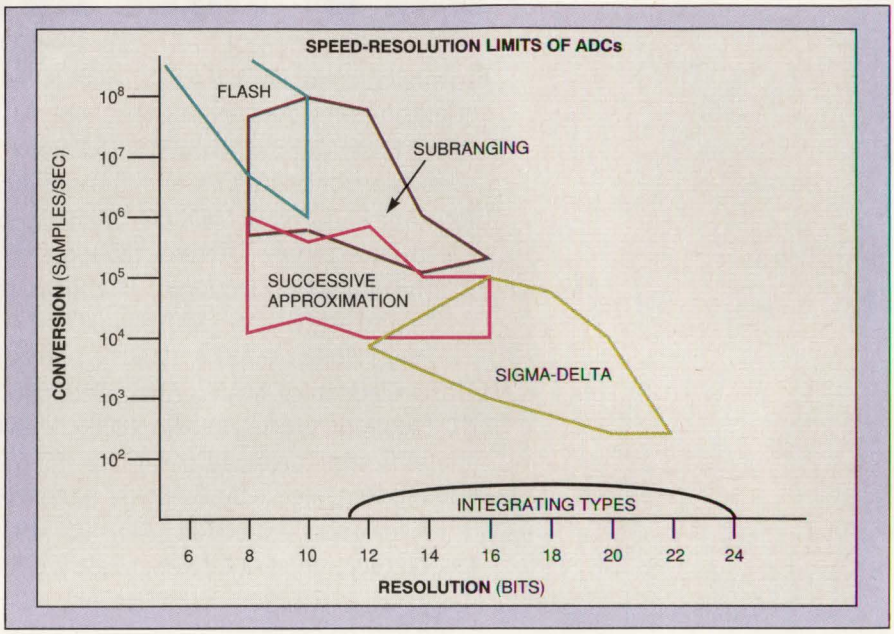

Fig 6—This graph shows the speed-resolution limits of successive-approximation, flash, subranging, integrating, and sigma-delta converters. (Figure courtesy Analog Devices Inc)

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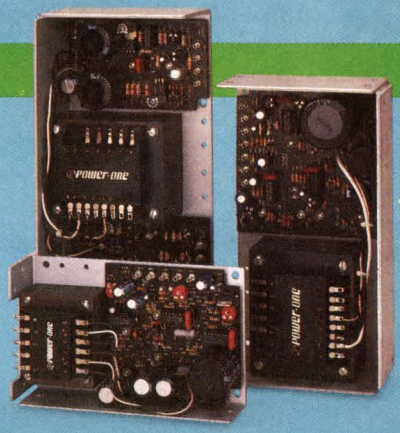

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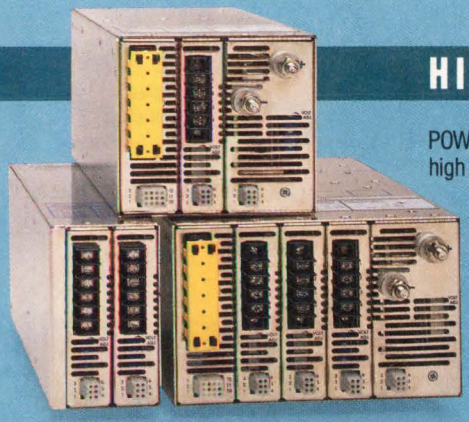

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sign goals of a particular application.

In addition to the five basic converter types in **Fig 6,** you should be aware of another class of converters, the self-calibrating type. These converters are available in several basic architectures, including successive-approximation, subranging, and sigma-delta types.

Self-calibrating converters use a switched-capacitor DAC and on-chip RAM to compensate for linearity and accuracy errors, which are particularly troublesome in many high-resolution converters. Among other advantages, self calibration eliminates the need for laser-trimmed resistors, which are difficult to trim to sufficient accuracy at resolutions higher than 12 bits. For further information on self-calibrating A/D converters, see **Ref 3.**

No single article, particularly one this short, can possibly cover all of the nuances of ADC architectures. In addition to resolution and speed—the distinguishing characteristics covered here—there are a host of other considerations important to designers. These include S/N ratio, harmonic distortion, spurious-free dynamic range, and reference accuracy. All of these factors influence the end application to various degrees.

For detailed information on A/D and D/A converters and their application, you should examine any good textbook on the subject. One example is the *Analog-Digital Conversion Handbook*, written by the engineering staff of Analog Devices and available from Prentice-Hall, Englewood Cliffs, NJ. For an excellent treatise on subranging converters, Datel Inc's application note AN-5, which EDN originally published as a 3-part series, provides a wealth of information. EDN

References

1. *Mixed-Signal Design Seminar Handbook*, 1991. Analog Devices, Box 9106, Norwood, MA 02062.

2. Swager, Anne Watson, "Oversampling data conversion: Technique bolsters dc-to-audio converters," *EDN*, September 2, 1991, pg 77.

3. Pryce, Dave, "Self-calibrating A/D converters: Monolithic devices enhance accuracy and linearity," *EDN*, January 20, 1992, pg 53.

Acknowledgments

Thanks to Doug Grant of Analog Devices for his comments on the characteristics of various ADCs and their applications. Thanks also to George Hill of Burr-Brown, particularly for the information on sigma-delta and integrating converters.

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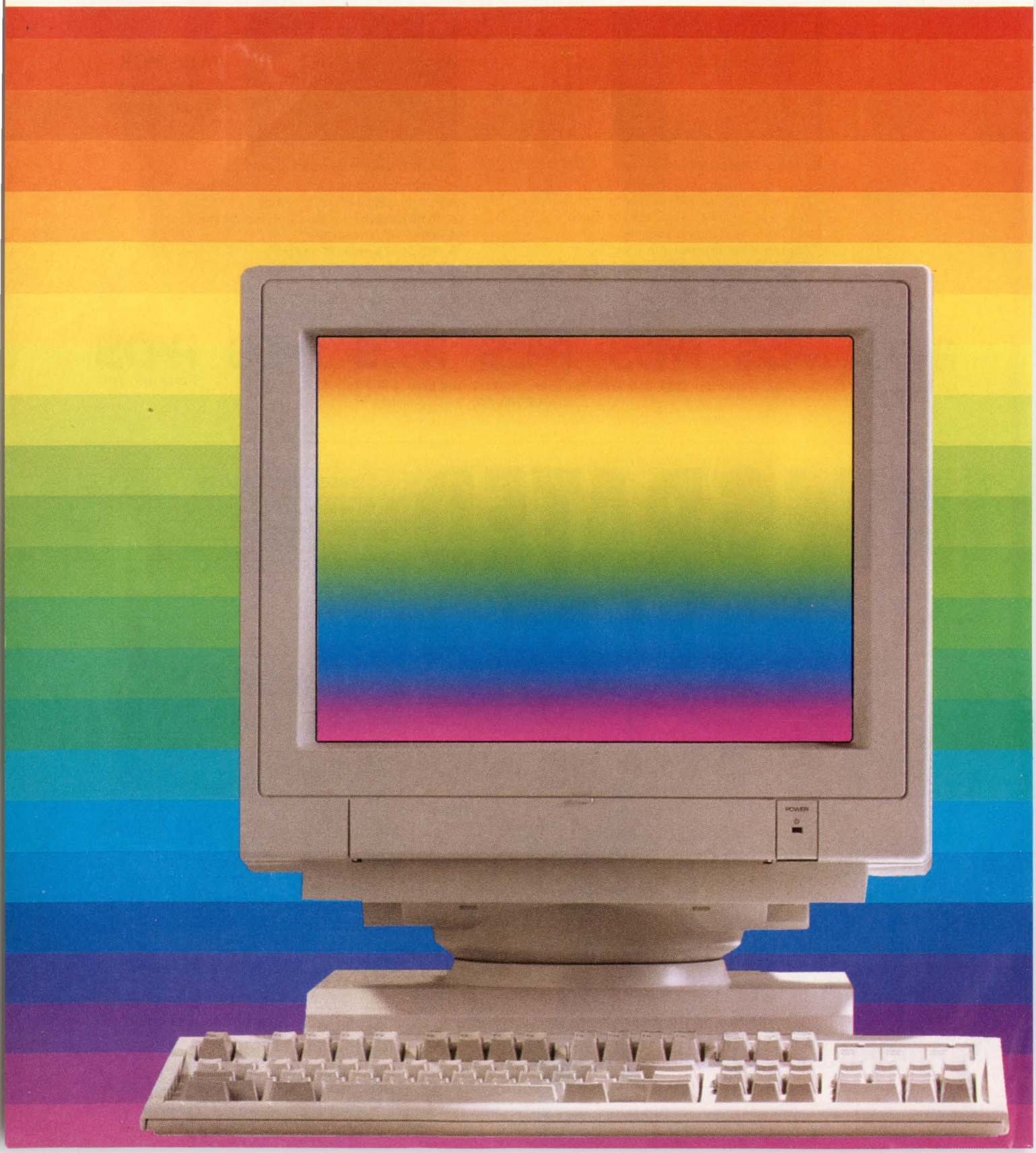

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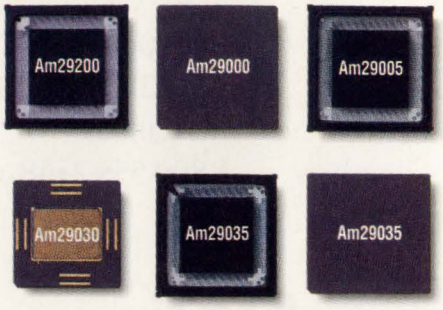

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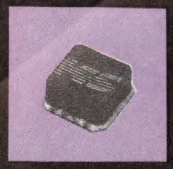

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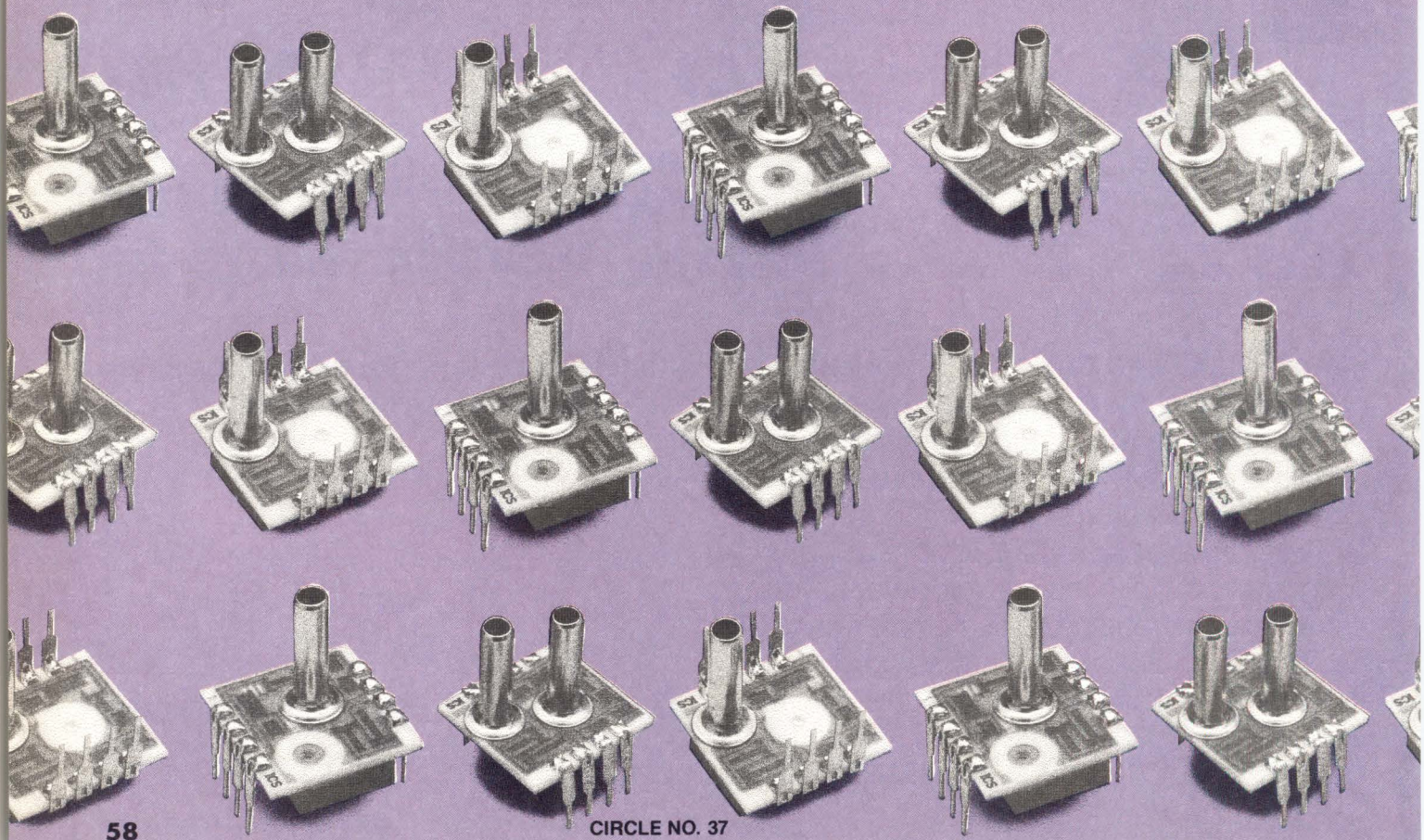


CIRCLE NO. 37

Let a GUI accelerator chip make your graphics whiz

The 86C911 is a graphical-user-interface (GUI) accelerator chip that speeds up Windows or Presentation Manager applications. The accelerator performs essential graphics operations such as moving and resizing windows, operating the cursor, manipulating icons, and generating pull-down menus. In systems that have only a VGA or SVGA (super VGA) display controller, the host CPU must perform these operations in software.

The chip also performs bitblt (bit-block transfer) operations, image transfers, line drawing, and cut-and-paste operations. Because the chip is a dedicated hardware processor, it can execute these functions faster than a general-purpose CPU. For example, the company claims that the chip can perform bitblt transfers four times faster than a 50-MHz 486 μP and can draw lines eight times faster.

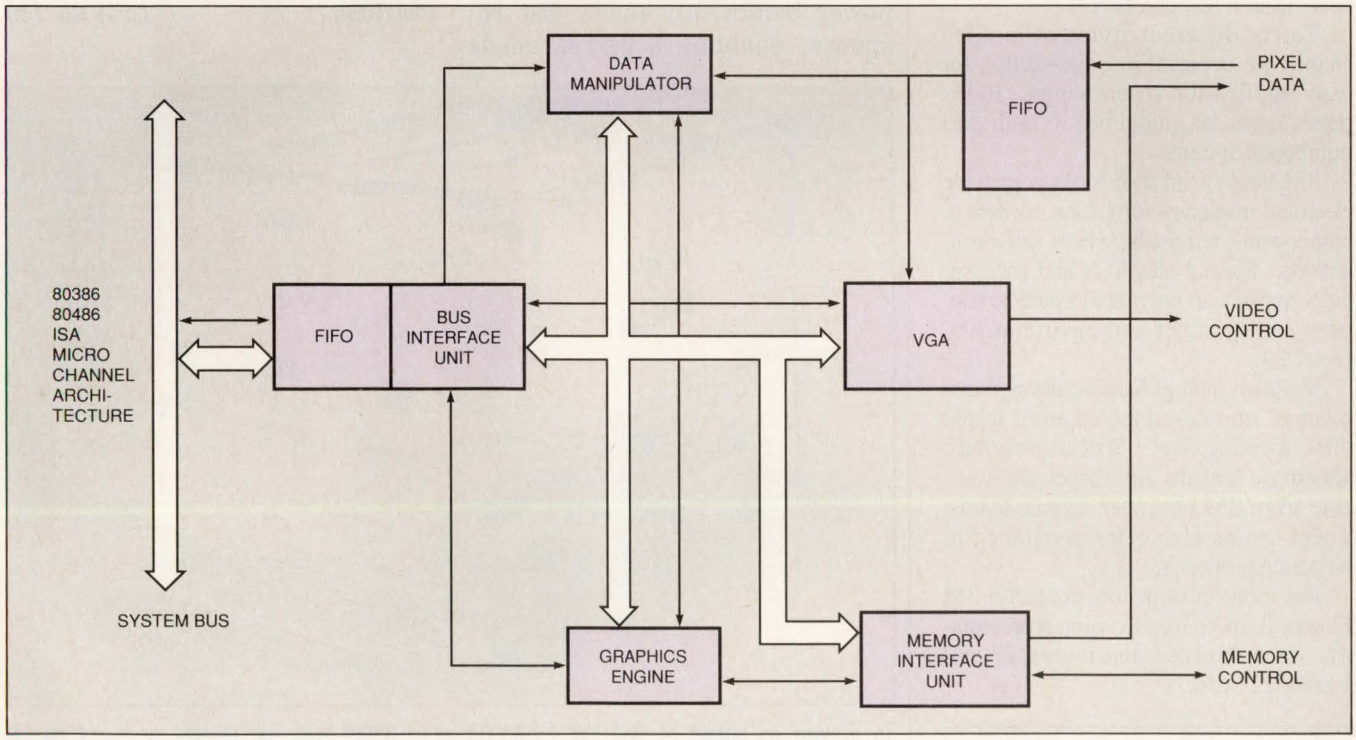
The chip contains a bus interface that features multiple FIFO buffers and directly communicates with an ISA or Micro Channel Architecture bus. It also interfaces with 512-kbyte and 1-Mbyte video RAMs. You can design a 512-kbyte 86C911-based accelerator card using 11 ICs, including the display memory. In addition, the chip can interface to the local bus of an 80386 or 80486 μP, which eliminates the system-bus bottleneck when transferring data to display memory.

The chip drives 1024×768-pixel noninterlaced displays having 72-Hz refresh rates as well as 1280×1024- or 1280×960-pixel interlaced displays having 43-Hz refresh rates. A direct-color mode produces 65,536 colors for 640×480-pixel displays. The chip is also 100% register-level compatible with VGA, MDA/Hercules, and CGA graphics standards.

A package of 14 software drivers allows applications using Windows 3.0, AutoCAD, PCAD, VersaCAD, Microsoft Word 5.0, Lotus 1-2-3, and Wordperfect. An enhanced VGA BIOS, called BOC911, is compatible with the industry-standard VGA BIOS and optimizes the use of the chip's extended VGA text and enhanced modes. $75 (1000).

—John Gallant

S3 Inc, 2933 Bunker Hill Lane, Santa Clara, CA 95054. Phone (408) 986-8144. FAX (408) 986-1457. **Circle No. 731**



The integrated functions on the 86C911 GUI accelerator chip include a bus-interface block that communicates directly with an ISA, Micro Channel Architecture, or CPU Local Bus to speed up graphics operations.

3M Publishes Heat-Shrink Cross Reference Chart

Helps OEM designers find best fit for standard tubings, molded shapes and shield terminators.

AUSTIN, Tex. — Finding the best heat-shrink tubing fast is the purpose behind 3M's new heat-shrink tubing cross reference chart.

It includes hundreds of descriptions and drawings, all cross referenced with part numbers for quick ordering.

Products include single and dual-wall polyolefins, and special purpose tubings of modified fluoropolymer, polychloroprene and polyester elastomer.

Hundreds of listings include applicable UL, CSA, AMS and MIL specs.

Comparisons are made with 3M shield terminators that include NAS and MIL specification part numbers.

Thirty different styles of molded shapes are depicted in cross-section for easy application to drawings. Index pages describe guidelines to both part numbering systems.

3M heat-shrinkable tubings provide electrical insulation for cables, harnesses, components, terminals, splices and terminations. Special adhesives and encapsulants combine to provide mechanical supports, strain relief and environmental protection.

Standard tubings handled through distributors are stocked for shipment within three working days. Special materials, adhesives, sealants and shapes are available from 3M customer service teams. These teams also offer assistance in preparing proposals.

For more information, contact a 3M Electrical Specialties Division representative or authorized distributor, or call 1-800-322-3636.

Filtered power amplifier can develop a 980-kW output

The Model 265 wideband high-voltage PWM dc amplifier includes internal filtering that yields output like that of a linear amplifier. A single module can develop a ±150A at ±330V dc (49 kW), or a 226V ac, continuous output. Peak output equals ±312A. You can parallel as many as 20 modules to develop a ±3000A at ±330V output—980 kW.

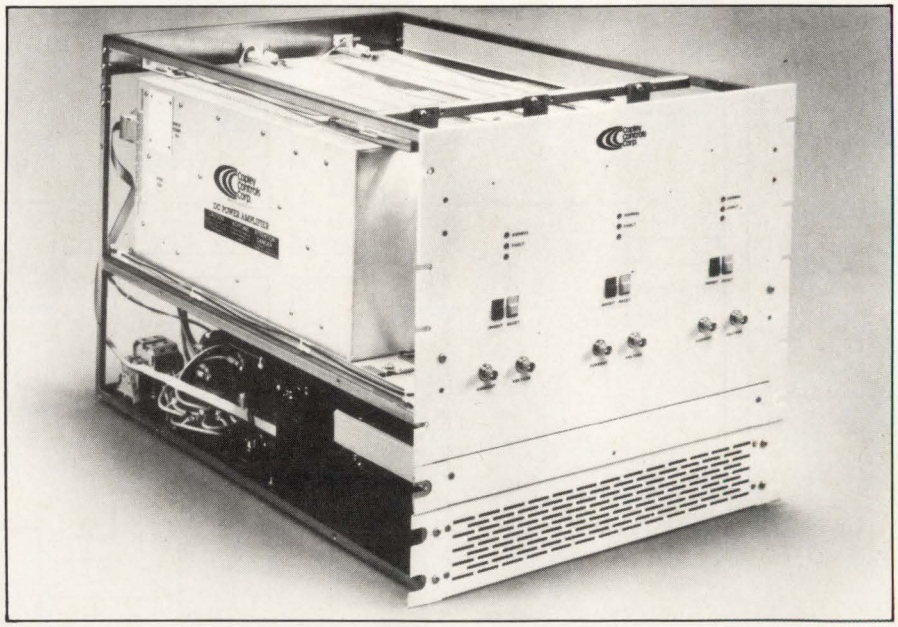
By providing smart power at low cost, the Model 265 can enhance existing programmable power applications. The unit also paves the way for entirely new technologies—variable-frequency power for ac drives, active friction-free magnetic bearings, active magnetic suspension systems, active neutralization of ac power-line harmonics, and active neutralization of ripple on high-voltage dc transmission lines.

The Model 265 can function as either a current source or a voltage source. The 81-kHz switching frequency yields a dc-to-4-kHz full-power bandwidth and a fast response, enabling a current-mode output to settle within 0.2% of its final value in 400 μsec. Maximum harmonic distortion at ±150A rms and 200 kHz equals 0.2%, and input voltage-offset drift is only 3 μV/°C. The unit's 3000W dissipation at a 150A output equates to an amplifier full-load efficiency of 94%.

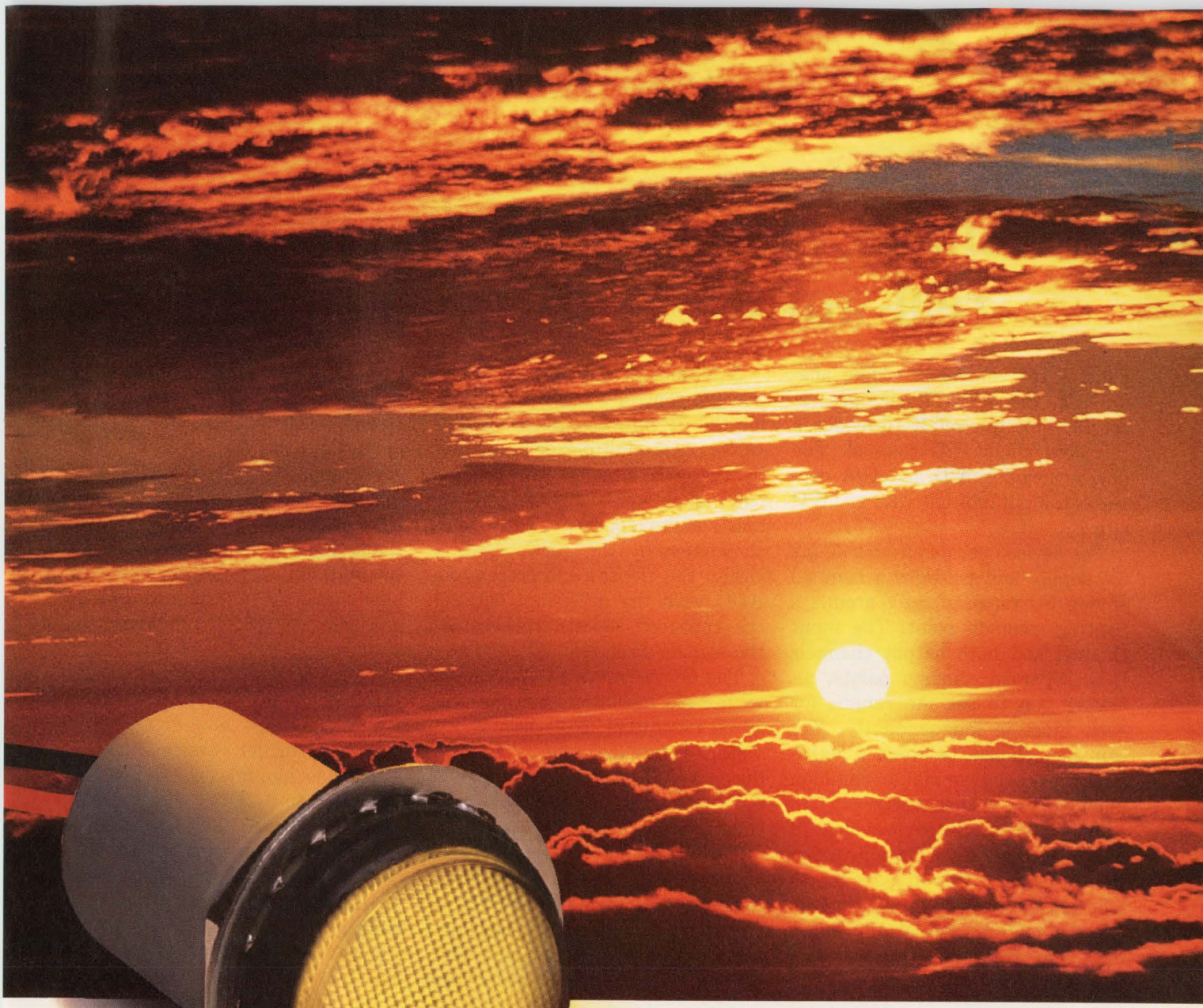
The rack-mountable Model 265 measures 19×10.4×23.4 in. and weighs 88 lbs. The amplifier is protected against short circuits, overload, overvoltage, undervoltage, and excessive operating temperature. The amplifier also provides a current-monitoring analog-output signal, which is calibrated to represent load current in terms of 1V per 25A. A current-limit circuit enables you to set the amplifier's maximum output current between ±19A and ±312A. $15,500.

—Tom Ormond

Copley Controls Corp, 410 University Ave, Westwood, MA 02090. Phone (617) 329-8200. FAX (617) 329-4055. **Circle No. 730**



To develop an output of 980 kW (±3000A at ±330V), you can parallel as many as 20 Model 265 PWM amplifier modules. Individual modules can operate as either a dc supply, a wideband ac supply, or a high-power function generator.

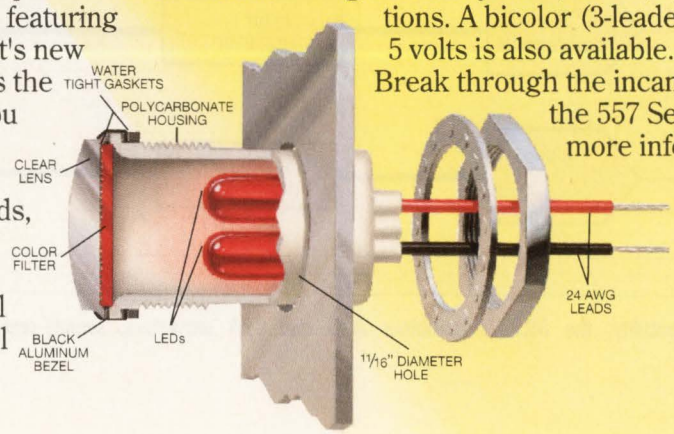


Few things shine brighter or last longer.

Dialight presents the best of both worlds in 11/16" panel mount indication: The 557 Series.

Incorporating unique multiple LED construction and proprietary lens design featuring wide-viewing angle, Dialight's new super-bright array produces the kind of light you thought you could only get from incandescent indicators.

And, as good as that sounds, consider the reliability and long life (100,000 hours) of LEDs. The result is a virtual replacement-free front panel mount indicator.



Watertight, tamperproof and complete with 6" wire leads, the 557 Series comes in single colors (red, green and yellow) in 4.3, 5, 12 and 28 volt configurations. A bicolor (3-leaded red/green) version in 5 volts is also available.

Break through the incandescent light barrier with the 557 Series from Dialight. For more information, contact: Dialight Corp., Dept. PL7, 1913 Atlantic Ave., Manasquan, NJ 08736; Tel.: (908) 223-9400; Fax: (908)223-8788.

CIRCLE NO. 39

ALL INDICATIONS ARE

DIALIGHT

Analog peripheral IC simplifies real-world I/O for processors

Packing the equivalent of four analog ICs, the ML2377 microprocessor (μP) peripheral IC provides a complete analog I/O channel. The device includes A/D and D/A converters, input multiplexers, and S/H circuits.

The device operates from a single 5V supply and provides a nominal analog I/O range of ±2V around a floating common point. The input channel and both output channels have separate common points, allowing you to set the ranges for each function independently. You can also choose between a hardwired or programmable common point for the A/D converter.

The A/D converter provides 10 bits of resolution with a conversion time of 2 μsec. The voltage you provide on a reference input pin sets the converter's full-scale range: 0.8× the reference voltage. The converter's linearity is ±2 bits.

A 6-channel multiplexer, which you can control with or without using the μP interface, feeds the converter. The multiplexer is followed by two S/H circuits. The two circuits allow you to capture two signals simultaneously for subsequent conversion by the ADC. Alternatively, the circuits can present the ADC with the difference between the captured signals, rather than the signals directly.

The device offers two DACs: one with 8-bit resolution and one with 10-bit resolution. Each has its own voltage reference input pin and produces a full-scale output range of 0.8× the reference. Both have settling times of 2 μsec.

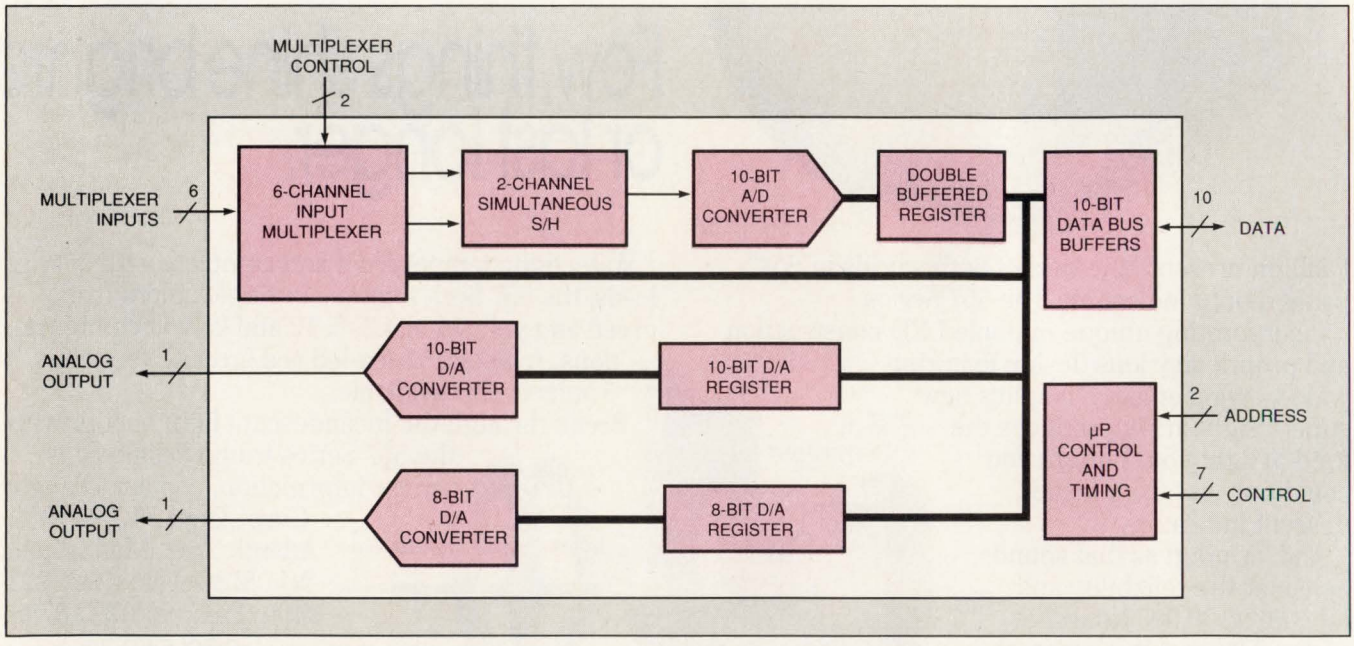
The device's μP interface uses a 10-bit-wide data port that's compatible with the TMS320C14 DSP processor. Four addressable registers control the multiplexer and store the digital I/O values to and from the converters. The interface has an 80-nsec read- or write-cycle time.

Because the chip is based on a semistandard analog tile array, the manufacturer can readily customize the device for your special applications. Some possible options include the addition of an address-latch enable signal for multiplexed address and data and changes to signal pinouts.

The standard version of the ML2377 comes in a 44-pin quad flatpack (QFP) and costs $6.50 (1000). A smaller version with only a 4-channel multiplexer, the ML2375, is housed in a 28-pin shrink small-outline package (SSOP) and will be available in September for $5.95.

—Richard A Quinnell

Micro Linear Corp, 2092 Concourse Dr, San Jose, CA 95131. Phone (408) 433-5200. FAX (408) 432-0295. **Circle No. 732**



Providing complete analog I/O capability, the ML2377 combines A/D and D/A converters; sample-and-hold circuits; and input multiplexers in a single μP peripheral.

Now You Can See True Colors Without Getting Soaked.

New full-featured RAMDACs from Brooktree deliver 24-bit true color for cost-conscious PC designers. Introducing four new RAMDACs that span the spectrum of PC applications, from 640x480 VGA systems to 1280x1024 workstation-quality graphics. They've got the right features, the right prices and are available right now.

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Unplug Sierra. Plug in our totally compatible Bt481 or Bt482. You'll get 24-bit performance at 16-bit prices.

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Introducing the Bt484 and Bt485, our newest mouth-watering RAMDACs. They combine true color with higher resolutions for higher performance graphics subsystems. And they're economical, too.

Bt485 operates at up to 135 MHz to drive pseudo color to 1280x1024 resolutions and gamma correct true color to 1024x768. It has a 64x64x2 cursor and all the serialization and timing to directly interface to a VRAM frame buffer.

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Colors	640x480	800x600	1024x768	1280x1024
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64K				Workstation RAMDACs
16.8M		Bt484/Bt485		

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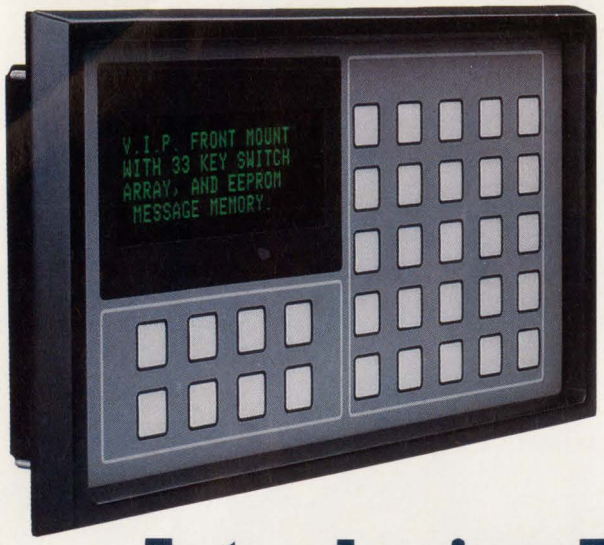

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Sealed Front Panel

The 33-key, rim embossed switch array uses reliable stainless steel metal-dome actuators behind a completely **sealed** membrane overlay.

Slide-In Switch Legends

Slide-in switch legends make it easy for you to quickly generate professional-looking prototypes.

Programmable Through Serial Port

We've gone one step further—you can now program canned messages **directly through the serial port to EEPROM**. Removing PROMs for external programming is a thing of the past!

Only 1″ Deep

Our 4×20 V.I.P. is only 1″ deep behind the front panel—making it ideal solution for door-mounted displays and other tight installations where depth presents a problem.

Applications

The 4×20 V.I.P. is tailored for process control, security, machine tool, and test equipment applications.

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This workstation/mini-terminal operates on 5 VDC and dissipates only 3 watts.

Additional Features:

- Programmable switch outputs
- Horizontal scroll
- Blinking characters
- 5 sets of 6 custom (user-programmable) characters
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- NEMA-12 rated
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- ESD shielding standard
- Operating temperature range: 0 to +70°C
- Up to 127 **canned** messages can be stored in the 7k bytes of onboard EEPROM memory
- Choose from several display viewing filter color options
- Built-in comprehensive self-test function
- Overall dimensions: 11.40×6.00×1.73″ (W×H×D)

Also available as a 3902-9904 "Stripped" V.I.P. without the front panel, keyboard and rear cover. Use your own external keyboard (up to 8×8) and panel mount.

The Finishing Touches

We can add custom overlay graphics, multi-colored key legends, and your company logo to give the 4×20 V.I.P. your personal touch.

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SPARC chip sets provide MBus expandability for high-performance SPARCstations

Cypress Semiconductor's SPARCset is the first MBus-module-based SPARC chip set and board design. The set accepts interchangeable SPARC MBus modules, such as those used in the Sun SPARCstation 10 or Sun Galaxy multiprocessor server. The chip set does not include the modules. The board design uses the 64-bit, 40-MHz MBus as a system bus and the 25-MHz SBus as a mezzanine or peripheral bus. The design is also available from Nimbus Technology. Cypress sells the chips and the board design; Nimbus sells the SPARC Board Set, which comprises the same chips and a board ready for component insertion.

The most successful system paradigm of the 1980s was the PC. For the 1990s, SPARC chip vendors are out to repeat that success using the SPARC RISC (reduced-instruction-set-computer) microprocessor as the base for SPARCstation clones. These vendors' chip sets include SPARC-based support chips and board-level designs, and some sets come with a pc board ready for components. Chip sets from Cypress Semiconductor, LSI Logic, and Fujitsu let engineers quickly turn out clones in much the same way clone vendors spin out PCs.

The chip sets free engineers from having to design cache and memory controllers. Vendors have structured the board designs so that each company can add its own peripheral set and expansion boards. The chip sets let you implement clones ranging from an MBus-module design that accepts Sun/Texas Instruments or Cypress SPARC processor modules to a SPARCstation 2 design having a 40-MHz SPARC CPU.

The SPARCset has two SBus slots and a Sun-compatible graphics controller that works with monitors having resolutions as great as 1152 × 900 pixels with 8 bits color. The graphics controller runs directly off the MBus, unlike most other SPARC implementations, which tie the graphics controller to the slower SBus. Low-level peripherals such as keyboards, mice, and floppy-disk drives have a separate I/O bus. The chip set's main memory uses up to 128 Mbytes of DRAM having 60-, 70-, or 80-nsec access times. The MBus modules may or may not include a cache memory.

Nimbus Technology's NIM6000M SPARC MBus Board Set includes the seven Cypress chips, which were developed by Nimbus, and a mother board. The board takes one MBus module, such as the single- or double-CPU Sun/TI SuperSPARC

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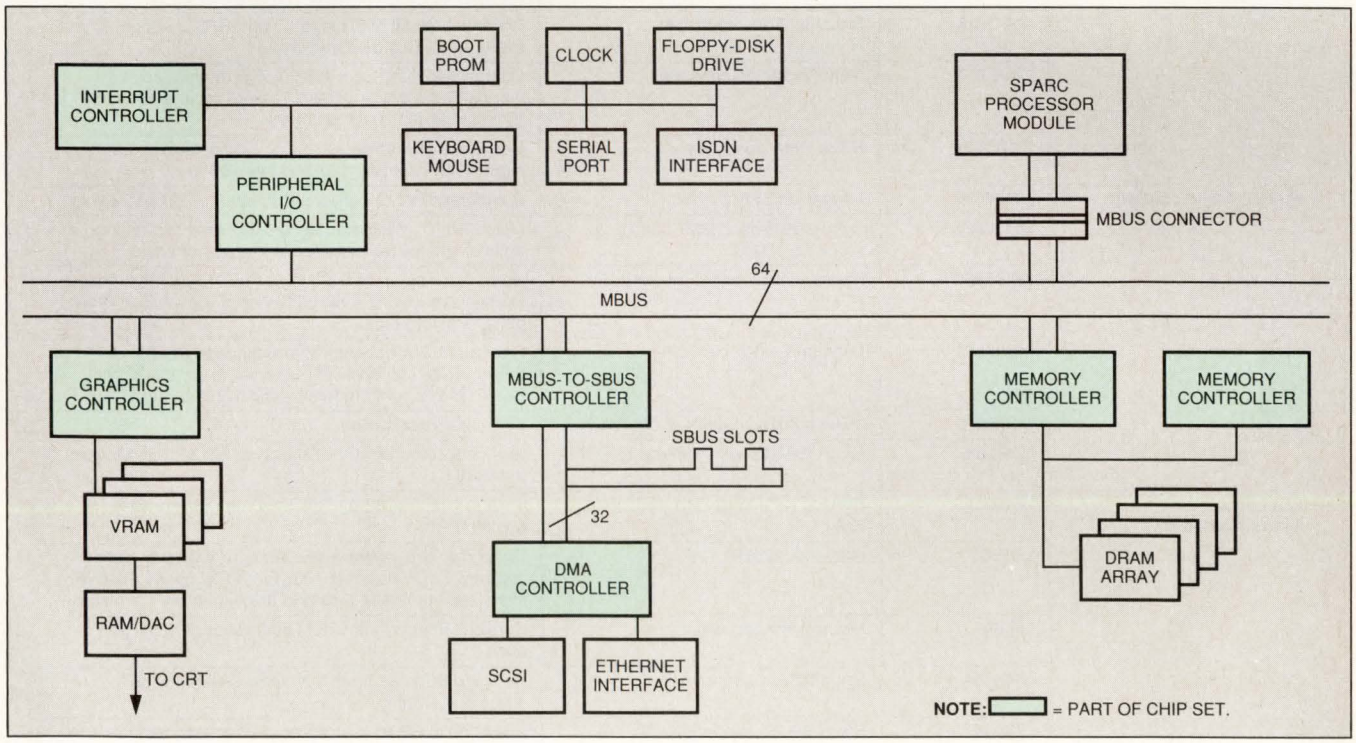

The Cypress SPARCset implements a SPARCstation using the 64-bit MBus for memory and the 32-bit SBus for peripherals. The chip set accepts MBus processor modules, including the superscalar SuperSPARC-based modules that have one or two CPUs.

SPARC chip-set features

	Cypress SPARCset (Nimbus Board Set)	Fijitsu SBus chip set	LSI Logic SparKit-40/MBus
SPARCstation design	SPARCstation 10	SPARCstation 2	SPARCstation 2/IPX
Number of chips	7 chips, 6 different types	6, including CPU	7, including CPU
Clock rate	40 MHz for MBus. CPU can run faster on its own module.	33-, 40-MHz CPU	40 MHz
Performance	52.6 SPECint; 64.6 SPECfp* with 40-MHz TI SuperSPARC	29 SPECmarks at 40 MHz	24 SPECmarks
System bus	MBus	MBus (level 1)	MBus
Memory	8 to 96 Mbytes	As much as 512 kbytes of DRAM and 256 kbytes of cache memory.	8 to 96 Mbytes
Comments	MBus links SPARC module, system chips (except DMA controller, which interfaces to the MBus-to-SBus controller). Chip set works with MBus and CPU modules, which can have cache memory.	32-bit integer-unit bus links CPU, cache controller, and caches. Implements MBus level II and cache coherency for multiprocessing.	32-bit integer-unit bus links CPU, cache controller, and caches. Set can use Super VGA and run Solaris 1.x software.
Price	$250** (100); license to manufacture SPARCset board, $50,000. Nimbus: chip set and board, $350 (10,000).	33 MHz, $660; 40 MHz, $838 (1000).	$629 (100)

*SPECint and SPECfp have replaced SPECmarks.
**Price does not include CPU. CPU supplied in MBus module.

SPARC chip-set chips

Vendor, chip set	Chip	Description	Comments
Cypress SPARCset	CY7C613	MBus interface memory controller	Translates 32-bit virtual address to 36-bit physical address. Includes a 64-kbyte direct-mapped cache controller and SRAM tag bits. Cache data held in cache RAMs.
	CY7C614	MBus peripheral I/O controller	Links MBus to 386SX address and data formats. Can address as many as eight 386-addressed peripherals.
	CY7C615	Interrupt controller	Provides SPARC system interrupts with 15 request levels (14 masked, nonmaskable). Has two 32-bit counters.
	CY7C616	MBus-to-SBus controller	Interfaces 25-MHz SBus to 40-MHz MBus. Controls as many as 4 SBus master/slaves.
	CY7C617	MBus graphics controller	Compatible with Sun's 1152x900-pixel 8-bit color or monochrome display. Has 256-word palette and programmable CRT timing signals.
	CY7C618	SBus DMA controller	Can control Ethernet and SCSI channels. Handles eight 16-bit data paths to and from SBus
Fujitsu SBus chip set	MB86903	Integer unit/FPU	Combines SPARC integer and floating-point processors.
	MB86921	Cache controller, MMU, and cache-tag RAM	Links CPU to MBus and serves as MMU cache controller. Handles as many as 256 kbytes of cache.
	MB86980	Memory and peripheral controller	Controls as many as 512 Mbytes of DRAM. Provides interleaving, parity, error-correction code, and an 8-bit peripheral interface.
	MB86981	DMA and video controller	Provides 3 DMA channels. Interfaces to SCSI, Ethernet, VRAM, and CRT controllers. Implements Sun CG4 color and monochrome frame buffer.
	MB86985	MBus-to-SBus interface controller	Links SBus and MBus.
	MB86986	MBus-to-VMEbus interface controller	Lets chip set work in VMEbus systems. Links VMEbus to MBus.
LSI Logic Sparkit-40/MBus	L64831	SPARC CPU with FPU and integer unit	4-stage pipeline, 32-bit RISC microprocessor with on-chip FPU.
	L64844	Cache controller	Direct-mapped cache with a write-through and buffer strategy. Can handle a 64-kbyte unified cache (32-byte line size). Implements path to main memory via SBus.
	L64841	Memory-management unit	Converts integer-unit virtual addresses to physical ones.
	L64853A	SBus DRAM controller	Hooks to SBus as main bus. Drives as many as 4 banks of SIMMs.
	L64846	SBus DRAM controller	Hooks up to SBus as main bus. Drives as many as 4 banks of SIMMs.

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modules that feature the TI superscalar SPARC processor.

LSI Logic offered the first SPARC chip sets, which let designers implement a 20-MHz, and later a 25-MHz, Sun SPARCstation 1. The company followed with a SPARCstation 2 version. The SparKit-40/MBus is an MBus-based upgrade that can handle CPU rates as fast as 40 MHz. The kit lets engineers implement a SPARCstation 2/IPX system.

The LSI SparKit-40/MBus uses the MBus as the system bus and the SBus as both a mezzanine or high-end-peripheral bus and a low-end I/O bus. The kit includes the 40-MHz L64831, a SPARC CPU that has an on-chip FPU (floating-point-unit) coprocessor. The CPU uses an integer-unit bus, which serves as a memory bus for the processors, the cache, and the cache controller. The cache controller, in turn, links to the system MBus, which handles the main memory and links to the SBus and I/O bus. The main difference between the LSI and Cypress chip sets is that the LSI set includes the CPU, and the Cypress set interfaces to an MBus processor module, which has its own SPARC processor or processors.

Fujitsu introduced its 33- and 40-MHz SPARC chip sets last year. A hardware-design kit lets you use the chip sets to built a busless, SBus or VMEbus SPARC workstation. Fujitsu is the only SPARC chip set vendor to provide a mechanism to build a VMEbus-based system; the VMEbus is the standard base for larger Sun workstations and servers.

The chip set is based on Fujitsu's MB86903 single-chip SPARC processor, which integrates an integer unit and FPU. The processor runs at clock rates as fast as 40 MHz. The set includes a memory-management-unit/tag-RAM chip, which manages cache memory and links the cache and processor to level one of the MBus; a memory and peripheral controller, which can handle as much as 512 kbytes of DRAM; an MBus-to-SBus interface controller; and a VMEbus-to-SBus interface controller.—**Ray Weiss**

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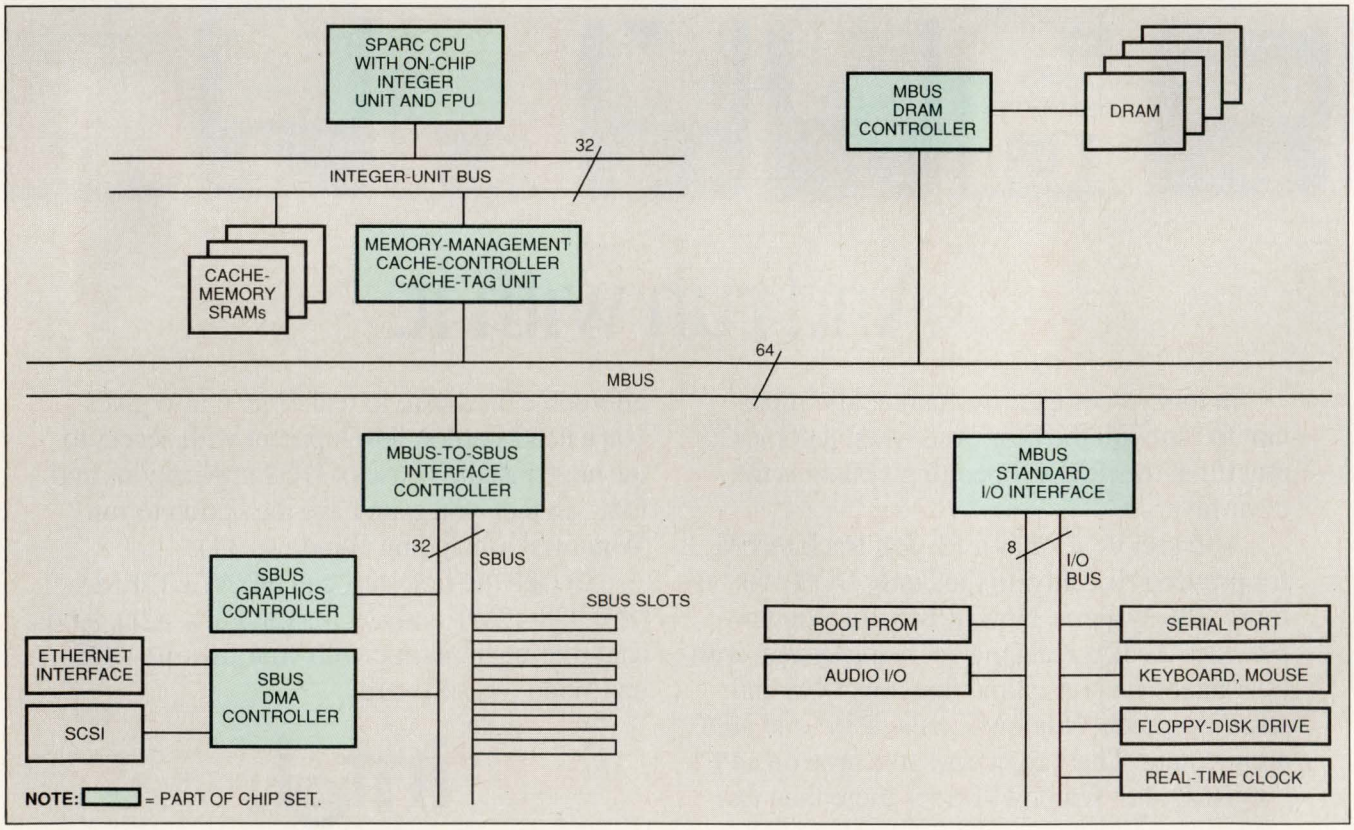

LSI Logic's SparKit-40/MBus includes a 40-MHz SPARC CPU that has an on-chip FPU coprocessor. The kit's design uses the MBus as a main system bus and the SBus for peripherals.

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$27 buys a 16-MHz embedded SPARClite microprocessor

SPARC RISC has made the grade for embedded systems. Engineers can now easily design in embedded versions of the desktop standard. These variants include stripped-down versions with specialized interfaces that minimize expensive glue logic. The MB86933, Fujitsu's low-end, 32-bit SPARClite, delivers SPARC performance at embedded-system prices. A 16-MHz version costs $27.

The original SPARC RISC (reduced-instruction-set-computer) microprocessor (μP) was not easy to design in; it required special, fairly tricky glue logic and lacked on-chip caches. In contrast, SPARClite carries a complement of special controllers to minimize design costs. The chip integrates a dynamic-RAM (DRAM) controller (with page-mode support), a 16-bit timer, and two DMA channels. In addition, the CPU provides a programmable address decoder and a wait-state generator for adapting to slower memories; it handles booting up from 8- or 16-bit memories.

Fujitsu engineers also upgraded the SPARC core processor. SPARClite runs with a static core, where clocks can be dropped to minimize power. A multiply instruction was added, and loads and stores were accelerated, typically taking one instruction cycle (pipelined).

To speed up embedded applications and provide a low-cost memory hierarchy, SPARClite integrates 2 kbytes each of instruction and data cache with the CPU core. The caches are 2-way set associative, with 16-byte, lockable cache lines (the cache block unit). These caches are big enough to hold key algorithms and their temporary data. Moreover, the cache locking feature enables programmers to flag critical code and data as cache resident, minimizing cache trashing and consequent indeterminate time behavior.

The low-end MB86933 has a 104-word register file comprising six overlapping windows. Each window provides the local environment for a function or subroutine. Control can move from function to function without having to save the former context by switching to the next function's register window. This feature minimizes context switching time, but it must be used care-

Fujitsu SPARClite MB86933

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- RISC CPU with 4-stage pipeline; 73 instructions
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- 15 interrupts; 2 USARTs
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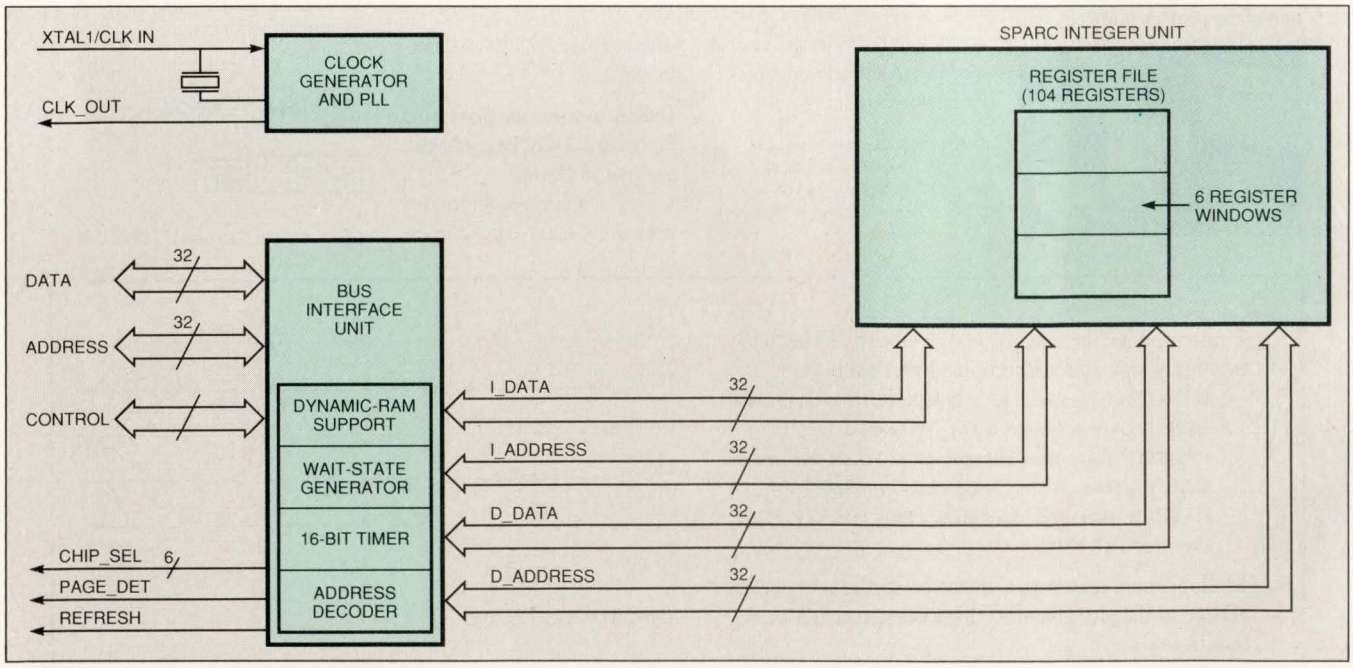

The Fujitsu MB86933 is a low-cost SPARC μP designed for embedded applications. It includes 2-kbyte instruction and data caches and memory controllers to minimize glue logic.

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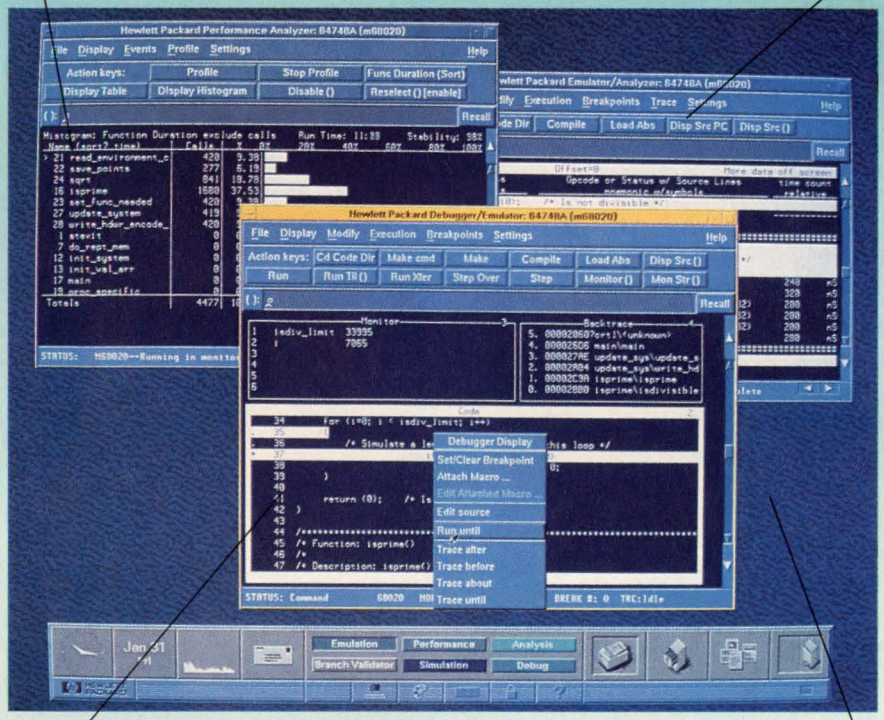

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HEWLETT PACKARD

CIRCLE NO. 40

fully, because of the limited number of register windows. A register window overflow can eat up a large block of time as the filled register windows are saved or restored.

Other SPARClite family members run to 40 MHz and include peripherals such as additional counter/timers, USARTs, a debug support interface, and a 36-entry TLB (translation look-aside buffer). Software and hardware tools include ICEs, logic analyzers, real-time kernels, and complete software-development tool chains.

An MB86933 evaluation board comes with 4 Mbytes of DRAM, 128 kbytes of static RAM, and 2 Mbytes of EPROM. The board has 4 counter/timers, two USARTs, an Ethernet port, and an AT bus interface.

—Ray Weiss

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Circle No. 737

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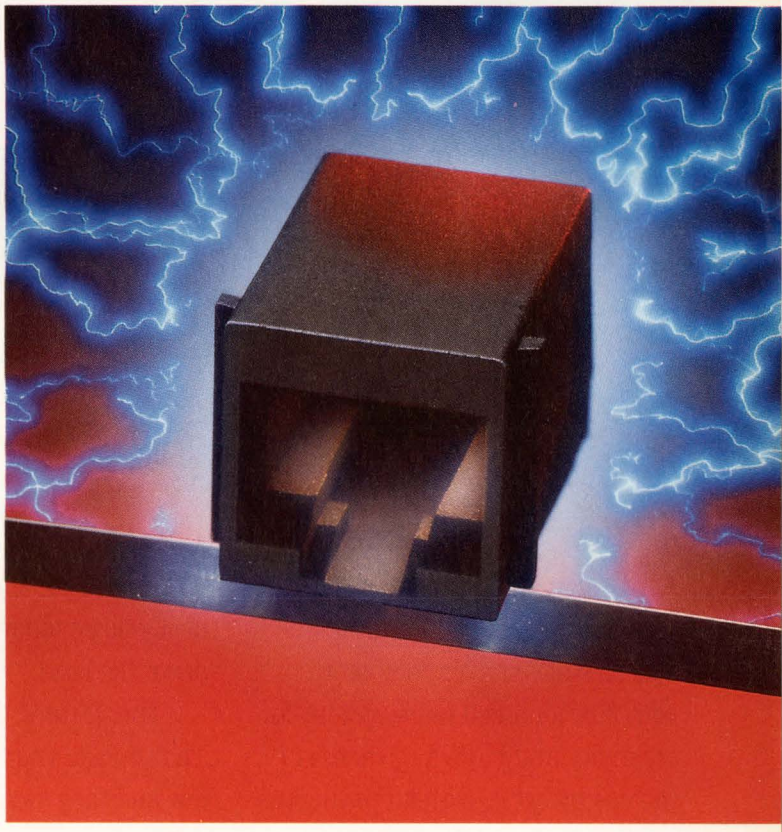

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CIRCLE NO. 46

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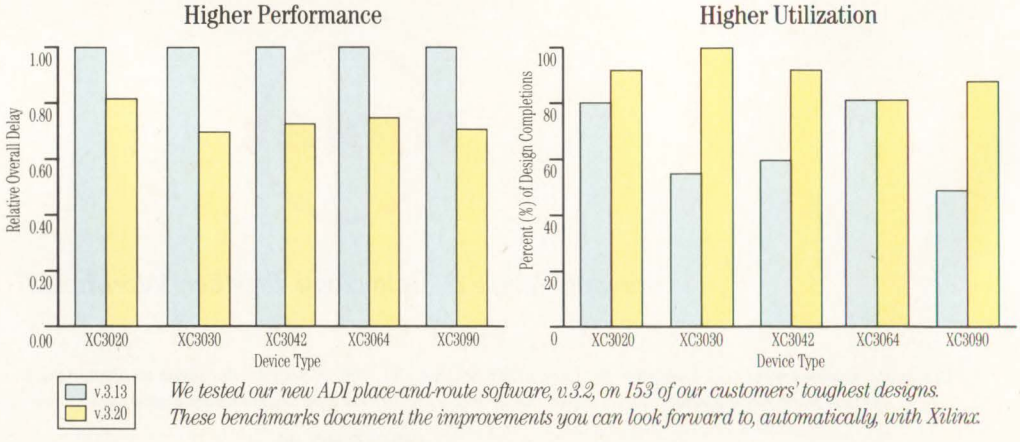

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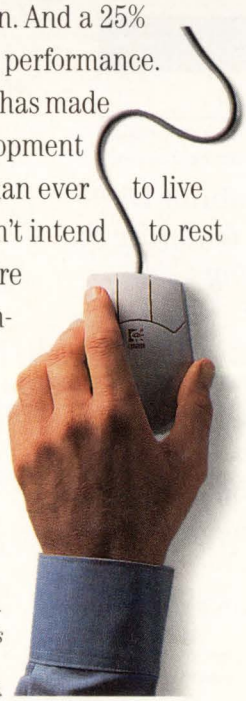

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CIRCLE NO. 47

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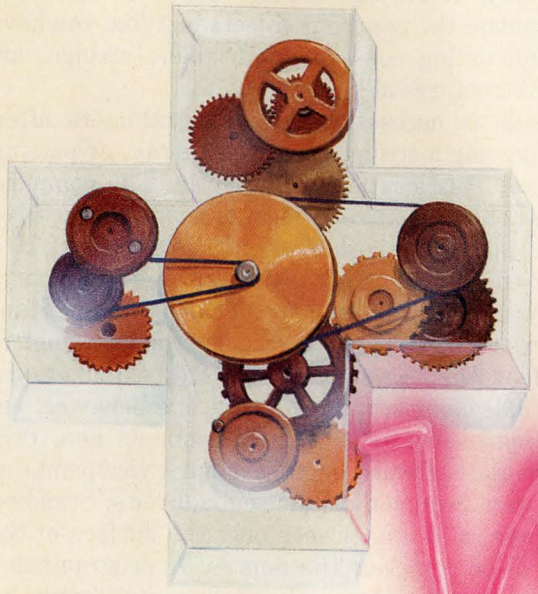
CIRCLE NO. 49

How

Despite the many similarities between C and C++, at run time, a C++ program can take some unexpected twists and turns.

Charles H Small, Senior Technical Editor

C++ tantalizes, proffering an easy upgrade to object-oriented programming (OOP). C++ is, with a few exceptions, a superset of C—an old and familiar friend. OOP will supposedly yield dramatic improvements in programmer productivity because objects are easy to reuse, enhance, and extend. Prophets tell us that the four essential properties of OOP (encapsulation, abstraction, inheritance, and polymorphism) make these benefits possible. Yet, all this OOPspeak can seem like so much self-referential gobbledygook.



Works

Fortunately, like the man who was delighted to find out he had been speaking prose all his life, if you have ever programmed in any high-level language, you have been using a class to generate objects all along. The class is none other than the construct that defines arrays, such as DIM or []. And the objects are the arrays themselves.

The array is the archetype for objects. If you keep the properties of arrays firmly fixed in your mind, you should be able to relate OOP jargon to what you already know.

Consider the array-defining construct (class) as a little software factory that will spit out as many customized versions of its basic model as you choose to summon (**Fig 1**). At run time, the arrays (objects) that the array-defining construct has manufactured not only have defined areas of memory for data storage constructed according to your specifications, but they also have functions associated with them that you can use to manipulate the data.

In OOP terms, the arrays (objects) encapsulate both data and functions. You cannot get at the arrays' data directly; you must use the array functions to access the data. And, the compiler hides the exact details of the functions from you.

Arrays also exhibit polymorphism. What this OOP gobstopper means is that you can have arrays (objects) for different kinds of data—all of which work the same way. That is, you can define an array (object) of 8-bit characters, or 16-bit integers, or 32-bit longs and subsequently use what appears to you to be the same access functions no matter what the size of the individual datum in the array (object). Clearly the code that takes an array index as an argument must be doing different calculations to find data located every 8 bits in memory from those calculations needed to find data located every 16 or 32 bits. The array (object), in good OOP fashion, hides these messy details from you.

Now comes a key implementation detail. Obvi-

ously, every time you invoke an array-defining construct (class), the compiler dedicates a separate area of memory for that array (object). But does the compiler also generate a set of array-manipulating functions for every array? Of course not; doing so would clutter the compiled code with numerous copies of the same functions. The compiler produces only one copy of the array-manipulating functions. Because compilers never forget, the compiler always knows how to connect any particular array's data area with the single copy of the appropriate functions.

Thus, in the case of C arrays, the compiler makes the link between the array-manipulating functions and the arrays at compile time. The OOP term for such linking at compile time is static binding. In some OOP languages, the compilers make no links between objects' data and data-manipulating functions. Instead, each object determines at run time, each time it is invoked, which data-manipulation function to use. The OOP term for linking at run time is late binding or dynamic binding.

For the most part, C++ statically binds objects' data and functions. Dynamic binding is more flexible, but incurs more overhead than static binding does. Where necessary, you can use dynamic binding in C++.

With the model of the array firmly fixed in your mind, you can move on to C++. The guiding ideas for C++ are twofold: the first is to let you set up classes that generate objects; and the second is to let you manipulate the resulting objects just like you have been manipulating constants, variables, strings, arrays, and structures all along in C.

One aside is necessary here: Programmers often speak of passing a string, passing an array, or passing a structure. This locution is imprecise. The compiled code does not move entire strings, arrays, or structures from one place to another. What gets passed is a pointer to the beginning of the defined area in memory.

This article will examine some of the more important new programming constructs of C++ and attempt to explain how they actually work. The explanations, which include compile-time and run-time behavior, encompass more than a C++ programmer's ken. Programmers and software engineers have viewpoints as different as a swimmer's and a scuba diver's. Standing on the shore, a swimmer sees only the surface of the water; a diver perceives the depths. A programmer's view of a program is similarly shallow and limited to

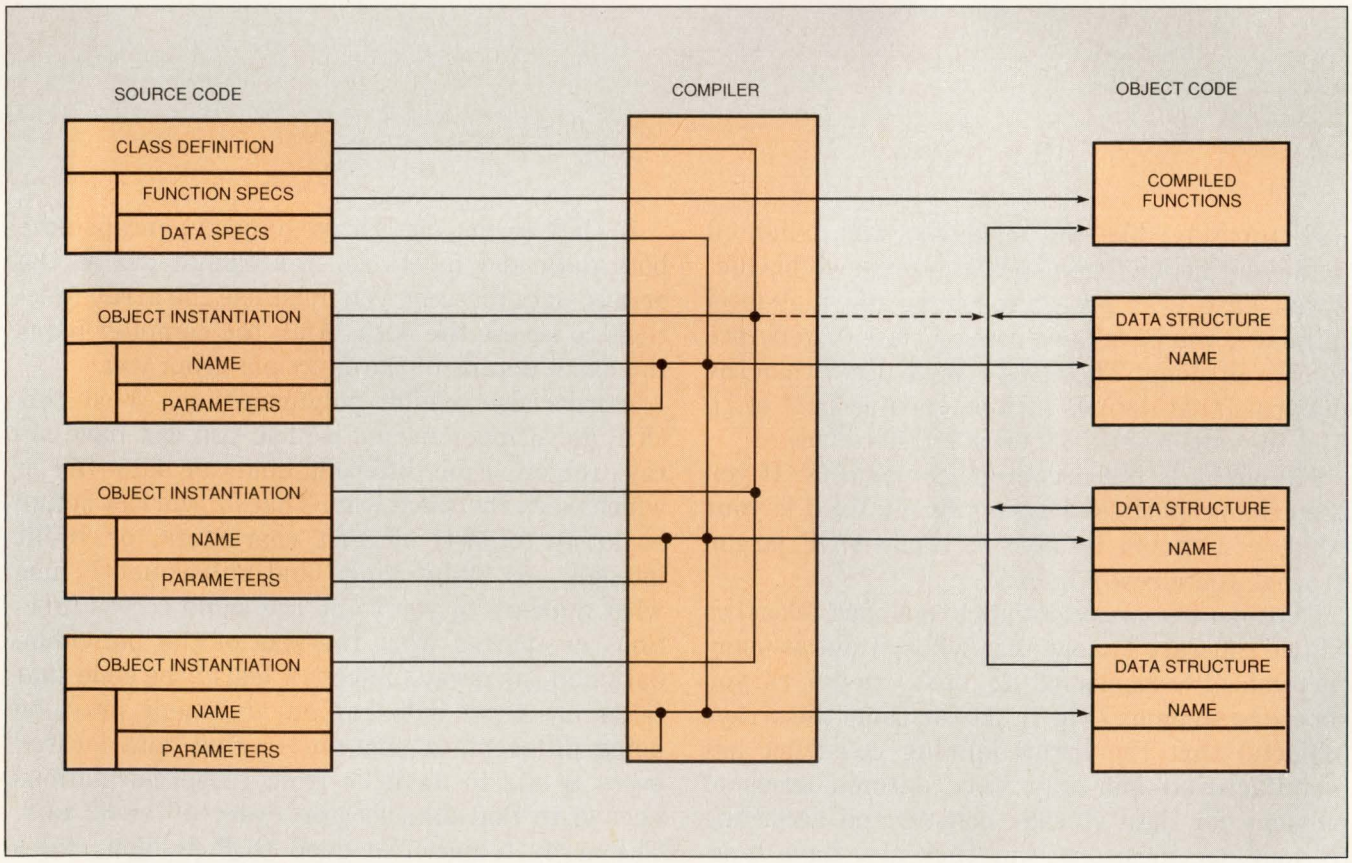


Fig 1—A class is a set of specs for data structures and functions that operate on those data. A class generates objects each of which has its own set of specified data structures and all of which share one copy of the specified functions.

the ASCII file containing the source code. A software engineer's concerns go far beyond the source code, taking in the actual object code and the hardware it interacts with.

You can divide the effects of C++ constructs into two broad categories: those that are internal to the compiler and which result in no run-time code or data structures, and those that result in object code or data structures. Further, the run-time effects of C++ break down into two subcategories: static effects and dynamic, run-time effects (**Fig 2**).

C++ compilers, just like C compilers (and all other compilers, for that matter), do more than simply translate the source code into object code. C++ *adds* hidden code to the source code. Thus, you cannot understand how a compiler works until you become aware of these hidden bits (see **box**, "Compilers slip hidden code into your programs").

The C++ format for defining a class is pretty straightforward. Suppose you are setting up a hierarchy of pc boards. First you need a "base" class from which you will "derive" other, more-specific classes. Remember that a class specification does not compile into run-time code. Using the class to make (instantiate) objects of that class generates run-time code.

```
class board {
  private:
    int model_num;
    int sample_size;
    float reading;
...
  public:
    void  reset() {...}
    int  get_model_num() {...}
    float take_reading() {...}
  };
void main()
  {
  board board_one;
  board board_two;
  board board_three;
  ...
  }
```

This fragment declares a class called *board*. In typical OOP fashion, objects of the *board* class have private data and public functions that operate on those data. The C++ compiler is thrifty. Even though you can make (instantiate) as many *board* objects as you want (*board_one*, *board_two*, *board_three*, etc), the C++ compiler compiles the public functions only once. So **Fig 3** is a simplified memory map of the result of compiling the code fragment. Each *board* object has its own data fields. But they all share the one copy of the *board* class' functions.

Just as with arrays, the compiler always knows where it put each class' functions. So when you invoke a particular object's public function (using the typically cryptic relational operator ".")

```
board_one.reset();
```

the compiler knows which particular function the program needs to jump to and simply plugs the function into the compiled code. Recall that the term for this form of linking an object's code and data is static binding.

Derived functions

The *board* class, by itself, is not very realistic. Not all plug-in boards would be able to use a common *reset()* or *take_reading()* function. So you can derive more specific classes from the base class, *board*, adding functions and data items as necessary.

```
class board {
  private:
    int model_num;
    ...
  public:
    void  get_model_num() {...}
    ...
  };

class io_board : public board {
  private:
   int io_slot;
   int sample_size;
   ...
  public:
   void reset() {...}
   void take_reading {...}
   ...
  };

class prom_burner : public board {
  private:
   int io_slot;
   int sockets;
   ...
public:
  void reset();
  void burn_prom();
  ...
  };

...//more board subclasses defined
```

Now the seemingly mysterious C++ property of inheritance becomes clear. The compiler knows that *io_board* is a subclass of *board*. So when the compiler makes (instantiates) an *io_board* object, for each object it sets up both the data areas specified in the *io_board* class's specification and the data areas specified in the *board* class' specification. Similarly, the compiler remembers that objects of the *io_board* class can use the functions defined in both the *io_board* class and the parent *board* class.

Multiple inheritance, too, is just so much grist for the C++ compiler's mill. The program fragment

```
class mother {...};
class father {...};
class child : public mother, public father {...};
```

results in objects of the *child* class that have all the data structures of both the *mother* and *father* classes as well as access to all the *mother* class' and *father* class' member functions (**Fig 4**). After all, the compiler has complete specifications for all these data structures. Just as the compiler can concatenate dissimilar data items into a C *structure*, it can assemble any number of dissimilar data items into a derived class' object. And the compiler can easily remember where it put all the functions and who can use them. Compilers are very good at this sort of thing.

Note that in actual practice, C++ is a little more complex than the preceding discussion. Actually C++ has some modifiers for a class' own functions (member functions) that allow you finer control over just who can use which functions. For example, you can define functions that only the base class can use and which subclass objects do not inherit using the C++ keyword "private." You can also define base-class functions that subclass objects can use, but that nonrelated objects cannot use using the C++ keyword "protected." The compiler handles all these fine details at compile time. The restrictions on inheritance add nothing to your compiled code.

The objects you create have many of the properties of constants, variables, strings, arrays, and structures. As long as you inform the compiler of what classes of objects you are manipulating, you can "pass" and "return" objects to and from functions. (That is, you can specify an object as a parameter to be passed or returned and then the compiler will actually generate code that passes a pointer to your object.) You can embed objects in structures and assemble arrays of structures. You can define pointers to objects (which, confusingly, entails a new pointer operator "—>" for operation but recycles the old pointer operator "*" for definition). All these operations are possible because the compiler knows that every object is really just a defined, restricted data area—a data area which has some particular functions associated with it.

For example, the code fragment below defines an array named *backplane* of 15 of our old friends, objects of class *board*. Then it uses a combination of array notation and relational notation to call a member function of each object in the array.

```
  ...
  board backplane[15];
for (int j = 0, j < 15, j++) {
  backplane[j].get_model_num(); }
```

Objects can even contain other objects. In this program fragment, the class *overseer* instantiates an ob-

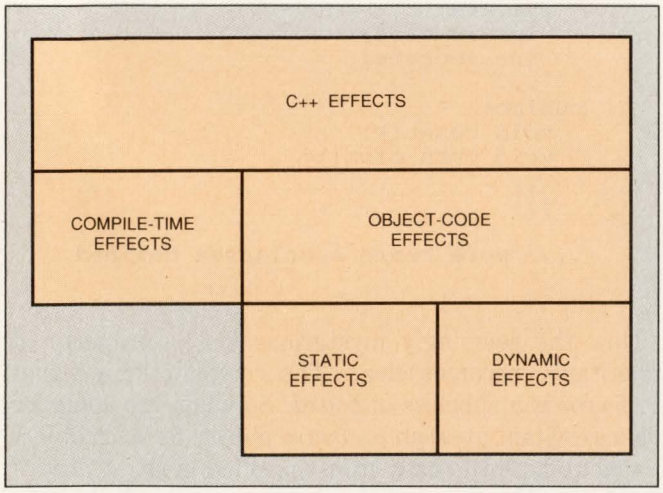


Fig 2—Not everything you type into your source file results in executable code in your object file; some of what you enter goes no further than the guts of the compiler. Conversely, compilers add hidden code that does not appear in your source file to your object file.

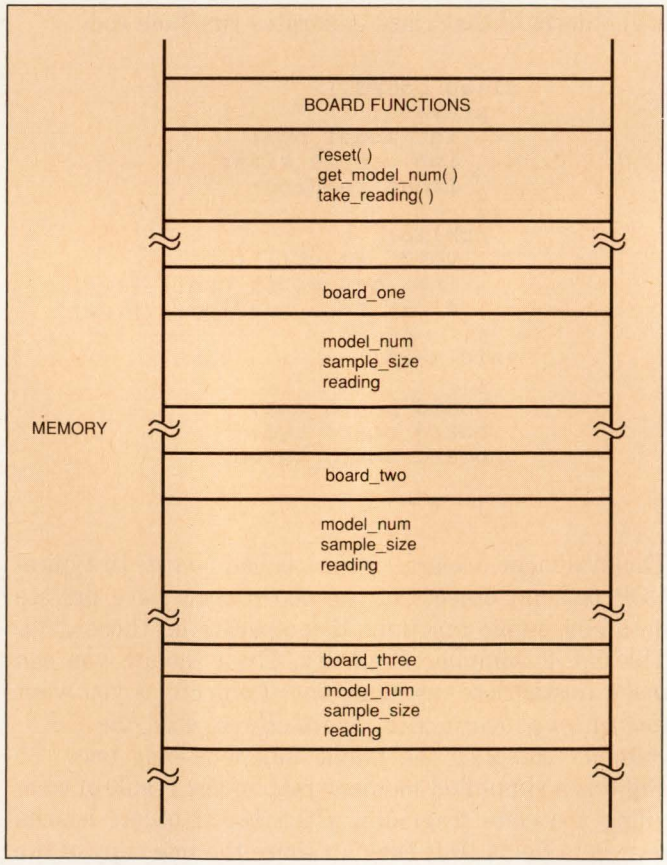


Fig 3—Three instantiations of the class board, board_one, board_two, and board_three, have their own data areas but share one compiled set of the class' member functions.

Compilers slip hidden code into your programs

The most common example of hidden code that C and C++ adds to your program specification is the overhead associated with setting up a so-called stack frame for each function call.

C's designers made good use of the general-purpose registers and the stack pointer possessed by the computers they developed C on. Noting that many variables were used only during the execution of short subroutines, the designers decided to set these variables up on the stack rather than allocate permanent areas of memory for them. Luckily, their host computers' stack pointers could perform relative and relative-indirect addressing. That is, a program could easily access data that was either at some known offset from the stack pointer or was pointed to by a pointer at some known offset from the stack pointer.

C's designers also decided to pass variables by value rather than by reference. Contrasting value and reference makes for a rather murky opposition. Examining the run-time behavior will hopefully clear things up. **Fig A** shows the stack that corresponds to the following C code fragment:

```
...
void main()
 {...
 int m_one=1;
 int m_two=2;
 func_1(m_one, m_two);
 ...
 }
void func_1(int one, int two){...}
```

The compiler, seeing that the integers *m_one* and *m_two* are active only within the body of the main function, will set them up as "automatic" variables on the stack. The compiler will concoct indexed-indirect stack-pointer instructions for any operation on these variables. When the *main()* function calls the function *func_1()*, the compiler inserts hidden code to set up *func_1()*'s stack frame and copies *m_one* and *m_two* from *main()*'s stack frame into *func_1()*'s stack frame.

This arrangement has one big advantage: having only copies of *main()*'s variables, *func_1()* cannot corrupt *main()*'s variables. But this arrangement also has one big disadvantage: because C functions can return only one parameter, *func_1()* cannot return new values for both *m_one* and *m_two*.

Because C's designers had a mania for compactness, they limited C to returning one parameter so that C functions could stand in for variables. Only those who can remember back through the mists of time to the dawn of the computer age can appreciate why C's designers were so fanatical about making C text files as compact as possible. In those days, programmers entered their code line-by-line on electromechanical teletypes using balky line editors. These line editors let you revise a line with minimal pain; revising a paragraph was much harder.

But does the ability to embed functions in a line of code, along with every other trick C uses to compress source code result in correspondingly compact object code? In a word, no; it's just a paper trick.

In C, the solution to this parameter-passing problem is to pass the function's pointers to variables back in the main routine. Then the functions could operate on the calling routine's local variables indirectly. C++ explicitly lets a function access the calling routine's variables by passing parameters by reference like this:

```
...
void main()
 {...
 int @I(m_one)=1;
 int @I(m_two)=2;
 @I(func_1())( @I(m_one), @I(m_two) );
 ...
 }
void @I(func_1())(int& one, int& two){...}
```

The ampersands (&) appended to the definitions of the parameters of *func_1()* mean that instead of obtaining copies of the calling function's variables, *func_1()* will operate, by indirection, on the calling function's variables. Without the ampersands, C++ works just like C. Here a simple change to the source code results in radically different compiled code.

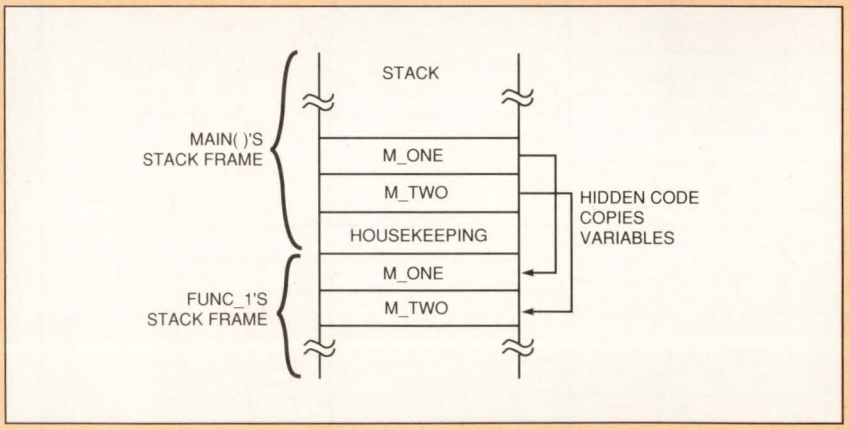


Fig A—C and C++ compilers insert hidden code at the entrance and exit of each function call to set up and tear down, respectively, a stack frame. In addition to the usual housekeeping data that calling a subroutine entails, each stack frame has places for each function's local variables. Further, if the calling routine passes parameters to the called routine, C copies the calling routine's data to the called routine's stack frame.

ject *peon* of the class *wage_slave* as a part of instantiating objects of the class *overseer*.

```
class wage_slave {...};
class overseer
  { wage_slave peon;
    ... };
```

Just like variables, objects can come alive only for the duration of a subroutine. C++ classes can optionally have a constructor that initializes an object's data structure and performs other housekeeping upon the object's creation. When your program kills an object, an optional destructor statement can do any necessary house cleaning. In fine C++ style, a ~ is the keyword that identifies a destructor.

```
class gatekeeper {
  private:
    static int attendees;
  public:
    gatekeeper() { attendees++; }
    ~gatekeeper() { attendees--; }
  };
```

Every time you instantiate an object of the class *gatekeeper*, the constructor *gatekeeper()* increments the private variable *attendees*. Every time you kill a *gatekeeper* object, the destructor *~gatekeeper()* decrements *attendees*.

But in some cases the compiler cannot make the link between data area and function at compile time. Suppose that after defining a workable set of *board* subclasses and creating a number of *board*-derived objects from the various subclasses, you try to manipulate them en masse. Specifically, suppose you make an array of pointers to all your *board*-derived objects and try to step through that array, resetting each pc board. Note that each subclass has its own *reset()* function. This situation certainly makes sense. You would expect different kinds of pc boards to have different reset functions. But the question here is not what do you expect, but what does the C++ compiler expect?

The answer, quite literally, is that in the case of an array of pointers to objects, the compiler doesn't know what to expect. A given pointer could point to an object of any subclass. So the compiler does not know at compile time which *reset()* function to plug in to the statement that indexes the array. So the compiler simply sets up a look-up table of *reset()* functions and jumps to the proper one dictated by the object being accessed.

The C++ term for this scheme is the unevocative and inappropriately named virtual function. The so-

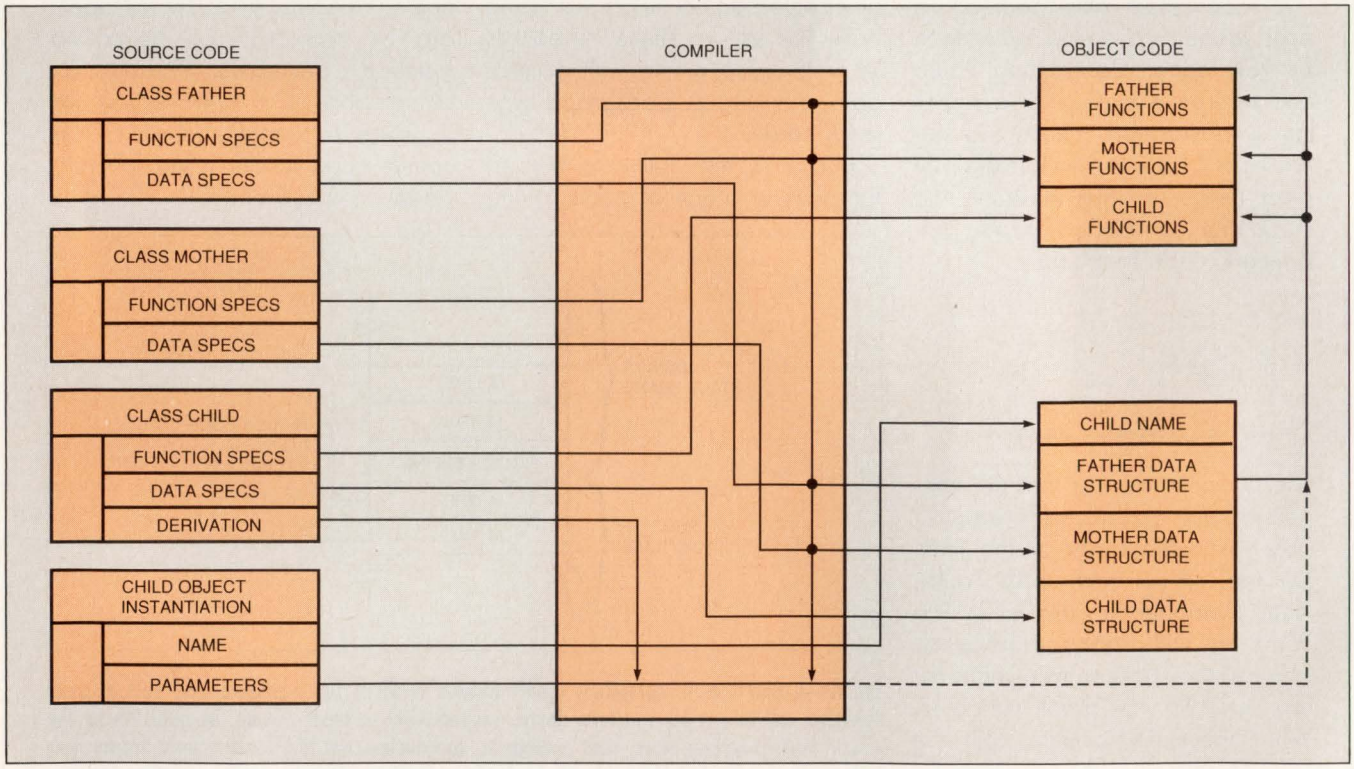


Fig 4—Derived from both the father and mother classes, an object of the child class gets private copies of father and mother data structures as well as access to father and mother member functions. Additionally, the child can have its own unique data structures and functions that the father and mother classes know nothing about.

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called virtual functions are quite real and not the least bit virtual. You define them in your source code and the compiler compiles them into the object code. At run time, they really and truly execute.

The only trick necessary to get virtual functions is to include a dummy declaration of the function that all your subclasses will have private versions of in the base class's definition.

```
class board {
  private:
    ...
  public:
    virtual void reset() { }
    ...
  };
```

Without this opaque subterfuge of the dummy virtual declaration, the compiler would woodenheadedly use the base class' *reset()* function for each subclass even if you had gone to the trouble to equip each subclass with a custom *reset()* function.

Overloading operators

Another key idea of C++, operator overloading, is nothing new either. Many existing C operators are quite overloaded already. Consider the C keyword *. First of all, in some contexts * means multiply. The same * keyword can multiply different types of numbers, sometimes also automatically promoting one member of a mixed-type multiplication. In those other contexts where * defines pointers, the same operator can define pointers to a host of different kinds of data. Think about it: Just like the index operators for arrays, the compiler must be selecting the appropriate hidden code to make the multiplications come out right and the pointers point properly.

C++ does not let you concoct your own operators as some OOP languages do. But C++ does let you make up custom definitions for any of the regular C operators. C++ compilers will use these customized operators only for objects of classes you specify. The syntax for overloading an operator is straightforward.

```
class incrementer {
  private:
    unsigned int incrementee;
  public:
    void operator ++() { incrementee + 50; }
  };
```

If you use the ++ increment operator on any object of the class *incrementer*, the compiler will plug in the code in *incrementer*'s operator statement (which increments by 50 instead of 1) rather than using one of the usual hidden routines for incrementing.

Default values and overloaded functions

The C++ compiler offers a nifty feature that costs you no overhead in your compiled code. If a function's definition specifies default parameter values, you can call that function with none, some, or all of the parameters.

```
void func_2(float fnum=2.3, int inum=6)

void main()
 {...
 func_2();
 func_2(4.4);
 func_2(4.3, 3);
 ...
 }
```

The compiler will plug in your specified default values for any missing parameters. This feature is another example of overloading.

Inline functions

C++'s inline functions hardly merit any justification at all after you realize how much overhead a function

Embedded C++ has single source

C++ compiler vendors obviously don't think that engineers will be using C++ for embedded systems. All the commercial C++ compilers are native-code compilers that run on, and produce compiled code for, a handful of common host computers.

Luckily, the ever fascinating, nonprofit Free Software Foundation's GNU C++ compiler runs on dozens of hosts, compiles code for over 40 processors, and handles any number of obscure file formats. The compiler, complete with source code no less, is available for only a media charge. If you have access to Internet, you can skip the media charge (**Ref 3**).

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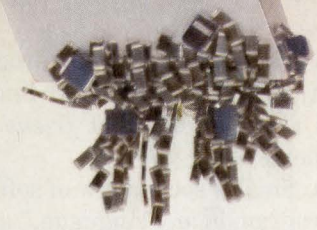

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call entails. An inline function works just like a macro definition in an assembly program.

```
inline float func_3(float temp)
 {
 return 3.414 * temp;
 }
```

A short function such as *func_3* is a good candidate for being an inline function. The compiler will simply plug in *func_3*'s code every place in your program where you invoke *func_3*. Just as for a macro, you must trade off program size for program speed when deciding whether to use an inline function or not.

The OOP precepts of encapsulation and data hiding mean that one object's functions should not be able to access another object's private or protected data. Of course C++ wouldn't be an extension of C if it didn't offer you a way to kluge things up. By declaring a function to be a *friend* function in the definition of two classes, the *friend* function can then operate on data from both classes of objects in one function call.

```
...
class laurel {
  private: int joke;
  public:
    friend int kluge(laurel x, hardy y);
  };
class hardy {
  private: int joke;
  public:
    friend int kluge(laurel x, hardy y);
  };
int kluge(laurel x, hardy y)
  { return ( laurel.joke + hardy.joke; }
void main() {
  int joke_total;
  laurel stan; hardy ollie;
  joke_total =  kluge(stan, ollie);
  }
```

The *friend* declaration is just so much more busy work for the computer. Certainly, the compiler has enough clues about what you intend. The *friend* function *kluge* has a function "prototype" in both the *laurel* and *hardy* classes as well as its own function definition. In *main()*, *kluge* takes objects of the *laurel* and *hardy* classes as arguments, accessing data of two different classes of objects in the same function call. This construction has no particular effect on your compiled code because the compiler is just doing what it does anyway: matching data structures to allowed functions.

What the *friend* construct can do to your program's design is a matter of raging debate. *Friend* functions outrage OOP purists. They predict that *friend* functions will lead to spaghetti code.

OOP is not a panacea. Small's second law of software, "You can write a bad program in any language," applies equally well to C++. A fanatical OOP programmer can compress and condense his source code wonderfully. But at compile time the compact source code could expand into a cumbersome plodder of a program. OOP deliberately emphasizes the relationships between things while suppressing the processes that operate on these things. Thus, you could loose sight of how things work.

Learning the new syntax of C++ is not difficult if you are already familiar with C (**Ref 1**). But changing your mindset from procedural to object-oriented programming takes time; six months is a common estimate. Breaking a problem down into a hierarchy of objects in far from an exact science. And no method exists to test how optimal a given breakdown is.

Proponents fervently hope that C++ will lead to more code sharing and reuse. While a given programmer may be able to reuse his own code more easily, code sharing within and among companies depends on

Editor's analysis

Programmers have a long history of semiliterate, inappropriate, muddled, or just plain silly neologisms. No one knows why programmers feel the need to have many different words for the same thing (function, procedure, subroutine, and method) or use the same word for a multitude of different things (virtual, environment). Programmers put unrelated words in opposition (logical vs real) or confound them (using argument and parameter interchangeably).

This tendency to use real words and nonsense words Alice-in-Wonderland fashion leads to puzzling, unevocative terminology. A classic example from C is dereference. To reference (that is, refer to) a memory location is to get its contents. But some locations are pointers whose contents are the addresses of something else. So far so good. Programmers refer to getting the contents of the memory location pointed to by the pointer as dereferencing the pointer, perhaps by conflating derive with reference. A quick trip to the dictionary reveals that dereference does not accord with any other use of the prefix "de-" in the English language.

C++ continues this tendency with the inappropriately named virtual function. Something that is virtual is present in essence or effect, but not in fact. As demonstrated in the main body of this article, virtual functions are quite real and not the least bit ethereal.

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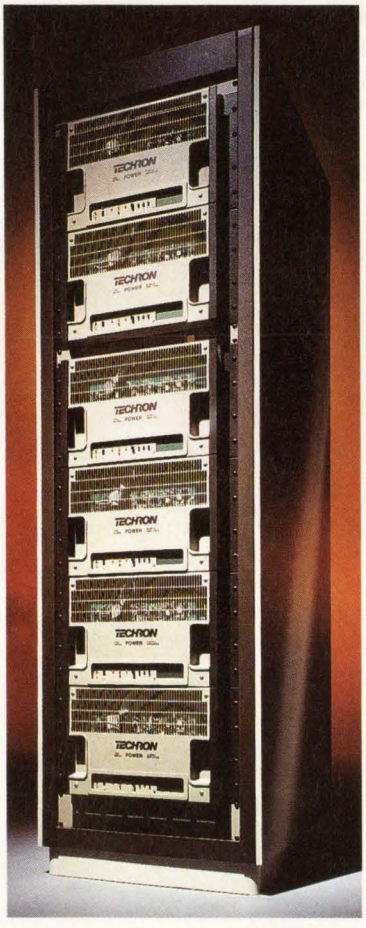

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more than a good language. A host of organizational, territorial, legal, financial, and archival problems overshadow the problems of grafting a foreign bit of code into a program. While **Ref 2** is ostensibly about reusing Ada code, the article actually describes the tough, real-world problems of code reuse that have little, if anything, to do with computer languages.

C++'s objects and operator overloading particularly suit the language to scientific computing. Who knows? C++ might slay the ancient Fortran dragon. But despite past reports of Fortran's impending death, it is still with us, alive and kicking. EDN

The EDN Readers' Electronic Bulletin Board System (BBS) has considerable C++ material. Call (617) 558-4241 (300/1200/2400,8,N,1). Access the /compiler, /util, and /tutorial Special Interest Groups (SIG) and do a keyword search for C++ by entering "rkC++" after you have gotten to each SIG's menu. The EDN BBS has C++ compilers, preprocessors, libraries, and computerized tutorials.

References

1. Ellis, George, "C++ has C's familiarity and OOP capability," *EDN*, January 2, 1992, pg 97.
2. Small, Charles H, "Adopting Ada is first step to code reuse," *EDN*, August 20, 1990, pg 71.
3. Fraser, Jay, "Keeper of the faith: Richard Stallman is leading a crusade to preserve your programming freedom," *EDN*, October 1, 1990, pg 174.

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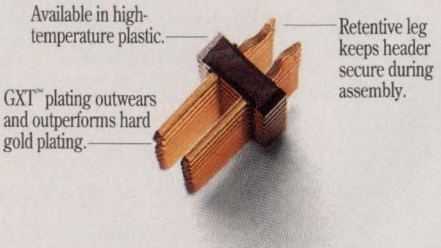

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Three-step method evaluates neural networks for your application

Jeannette Lawrence and Peter Andriola, California Scientific Software

Characterizing your problem and assessing the available data may lead you to formulating a neural-network implementation. If the problem type fits and the data is sufficient, a neural network can do the thinking for you.

Neural networks are the core of many well-known applications, including sonar that can recognize submarines, robots that learn how to avoid obstacles, and computers that read words aloud on the fly. But odds are that you're working on yet another application and you need to determine whether a neural network would be effective for you. Just being familiar with many neural-network applications doesn't give you an answer. You need an organized approach to assessing new problems and evaluating possible ways this technology can solve them. Armed with such a methodology, you can quickly determine the effectiveness of a neural network for any particular project without wasting development time and money.

A good methodology would explain why and when neural networks could be useful and would help you determine when another design approach might be better. The methodology discussed in this article provides you with a general-purpose evaluation broken down into three steps: characterizing the problem, assessing the available data, and formulating a plan for fitting the neural network into the total design. After presenting this methodology, we'll use it to evaluate three ways that you can use neural networks in an automated assembly and test system.

Neural networks perform a unique type of computing, requiring you to look at data and problems differently from when you use traditional techniques. You can forget logic, memorized formulas, and compilers, because neural networks don't read Boolean, calculate well, or understand rules. Neural networks are nonlinear associating devices able to solve complex relationships that are often difficult to express with rules or math. If you give a neural network a set of example situations and results, it will "learn" to generalize for similar cases.

In our experience, only one neural-network algorithm—back propagation—has proven to be widely effective, though many exist. To save time and space, we'll limit our scope to neural networks of this type (see the **box**, "Seven design steps," for a summary of neural-network design). For an in-depth explanation of neural networks' operation, see Maury Wright's Technology Update, "Neural networks tackle real-world problems," in the November 8, 1990, *EDN*, as well as the references at the end of this article.

Defining the problem

Because you define neural networks without math, rules, or programming, problem definition often involves looking for new types of solutions. Neural networks handle certain types of problems well, and often you can redefine an old problem as one of these types. If you can think of a problem as pattern recognition, classification, evaluation, modeling, prediction, or control, a neural network is a good tool to use. Any problem that a system can solve by associating some input pattern with another output pattern offers good potential for solution by neural-network technology.

For example, consider a process-control problem in

which an expert system determines the appropriate control law depending on the state of the process. You can redefine this problem as associating the neural-network input pattern (the state variables) with the output (the control law), as shown in **Fig 1**. This approach allows you to use a neural network to model and control the plant (**Ref 1**). When a process model must include the effects of time (such as the progress of a chemical reaction), the input data would include recent-past data for the previous states.

You can express many such problems as a kind of pattern recognition that identifies the input, perhaps by a set of characteristics, such as round or square, or perhaps by a unique name, such as "capacitor." Signal processing and filtering are examples of pattern-recognition problems that neural networks handle well (**Ref 2**). When filtering a noisy data channel, the receiver must determine which of the noisy signals is the original one. You can train a neural network to do this using samples of noisy inputs and uncorrupted signal output. Classification and evaluation are closely related tasks in which the neural network sorts through lots of data and categorizes the data by such features as quality, physical position, noise level, etc.

You can often redefine a sequential "if-then" problem as a pattern-recognition task. Suppose, for example, that you have collected some results from testing a bad electrical assembly (the input pattern). You can set up a neural network to recognize which pc board to swap out, or which component to replace on a board (**Ref 3**). Rather than program the conditions under which each pc board or component might exhibit various kinds of failures, you can train a neural network on examples collected from failures that repair technicians have diagnosed. When examples are readily available, such a network is often easier to use, cheaper, and more accurate than automatic test equipment or diagnostic software.

If the problem involves modeling some behavior, particularly nonlinear behavior, then a neural network is an excellent tool. You can use a neural network to model any process with an input/output relationship, including production processes and human, mechanical, financial, or chemical behaviors. Neural networks can grasp very complex nonlinear behavior without specific formulas or rules.

Assessing the data

It is critical that you assess the available data before committing to a neural network. If you don't assess data properly, you may waste a lot of time training, redesigning, and retraining a neural network that will not learn to solve the problem because the data set you're feeding it is poor. You must have an ample,

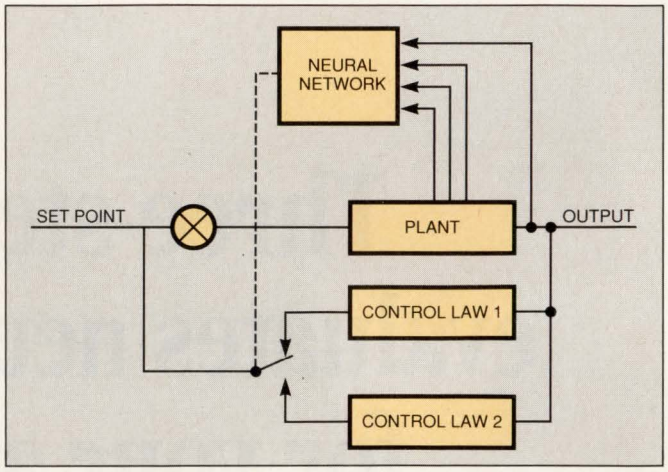


Fig 1—A neural network can choose the appropriate control law, given the current control law and the current state of the plant.

truly representative collection of example data and known inputs and outputs to train and test with. If no examples are available, and you can't generate any, then a neural network is not the tool to use. You're better off with a traditional technique such as a program, an expert system, or digital logic.

The example data can be a historical collection, such as records of production-line failures and the corrective action taken, or experimental results. Alternatively, you can create a training set. For example, a filter's training set could consist of many examples of both data or signals mixed with added noise (network input) and clean data or signals (network output). You can also generate data using simulation software, or by creating random examples (inputs) and having human experts classify them (to identify outputs). In any case, you don't need to define underlying principles, rules, or math. You don't even have to understand how to solve the problem. Knowing which data are relevant is the key.

The most difficult aspect of assessing data is judging its quality. Good data is relatively clean and contains the important variables needed to make associations. The data must include enough examples of sufficient variety for the network to generalize. You should include a good distribution of possible inputs and outputs; if 90% of the examples depict one outcome and 10% of the examples depict another, the neural network may have difficulty learning the latter outcome. The data doesn't have to be perfect or exact; neural networks can tolerate noisy data and will learn to generalize regardless, if given enough examples. However, if two examples contradict each other, the neural network cannot learn that both are true. The best data contains no direct contradictions and very few ambiguous cases. Contradictions and ambiguities often occur

when human experts rate the examples, such as for a quality-assessing application.

Generally speaking, the more examples you can collect for training and testing, the better. Having enough data is even more important than having good data. Unfortunately, no rules or formulas exist for calculating the appropriate quantity, because that depends on the complexity of the problem to be solved. Most applications having 30 or fewer inputs and a few outputs need at least 100 examples, and 1000 is a safer guess. If the data typically falls into categories or tends to cluster around certain examples, then fewer are needed. If the input set could include almost any combination of input values, then you must add more examples for training.

One approach that can save some design time is to identify the border cases, if they are apparent in your data. In a border case, a small change in input causes a notably different output. If you supplement a set of border cases with examples created using randomly generated input patterns, you should have sufficient data to train the network. Be sure to have the corresponding outputs for the random inputs properly rated by experts or generated by a reliable simulator.

Certain problems are too big for neural networks to learn in a reasonable amount of time. If the system has thousands of different continuous-valued input variables and thousands of example input/output sets, then the problem may be too large. The largest, most successful network we know of has 1440 inputs and 20 outputs and was trained with 200 Mbytes of data. This particular network reads a line of text from a medical journal, paper, or book and classifies the material as author, title, publisher, table of contents, abstract, etc. After roughly 100 training runs (which took many weeks on a 80386 machine), the neural network learned all training examples with 96% accuracy. In three months of use with 400 Mbytes of new data, the neural network made no errors. Though a network this size is not out of the question, a design with over 1000 inputs and this much data is very unusual.

If you are unsure about the quality or quantity of data available, you might consider a quick training session to see if the neural network can solve the problem. A good test may take only a few days of effort (if you already have some data) using software you can find for a few hundred dollars.

Designing an implementation

You can train most neural networks using software simulation. Once trained, a neural network can operate in software, hardware (specialized chips), or a combination of the two. You can use neural networks as complete solutions or include them within a larger design

Seven design steps for back-propagation neural networks

Step 1. Decide what you want your neural network to predict, generalize, or recognize. Examples include noise reduction of an ultrasound signal, recognition of a submarine from sonar, and diagnosis of production-line failures.

Step 2. Decide what information you want your neural network to use as inputs for generating its predictions, generalizations, or recognitions. For example, pressure readings, temperature, quantities of chemicals, and material-combining processes may predict the outcome of a chemical experiment.

Step 3. Get some data. To train your neural network, you must have examples of input data (ie, what you know when the network is implemented) matched with output results (what you will be asking the network to tell you). The sample training data is like a set of flash cards that the neural network will learn to generalize from. The data may come from historical databases, tests, simulations, expert opinions, etc.

Step 4. Build a network. The two things you need to create a working neural network are a definition of the network and a collection of data. The definition includes number of inputs and outputs, number of hidden neurons, and possibly other specifications such as the neuron transfer function.

Step 5. Train your network. The neural-network simulation software does this for you. You don't need to train the neural network to 100% accuracy for all training examples. You specify the level of accuracy desired.

Step 6. Test your network. In order to be sure that you have a good network, you must show it data it has never seen before and check the results. If the results are correct, you're ready to use your network. If not, you'll have to get more or better data, or redesign your network. Often, adjusting the number of hidden neurons or connections will improve the ability of the network to generalize for new data.

Step 7. Run your network. Running a network consists of presenting it with new input data and gathering the usable result. You can run a neural network from within the simulation software, from another program, or on a chip (for high-speed operation without the overhead of an operating system).

that is controlled under another scheme, such as an expert system. The trained neural network exists as a matrix of connection values (weights), which you can put on a computer disk, in program memory, or onto a chip. Running the trained neural network involves presenting current data at the inputs and observing the results at the outputs. Many neural-network programs offer compilable code for calling the neural network as a routine.

Speed is one advantage of neural networks over traditional programming techniques, even when the neural network is implemented in software. The output comes as an immediate response to many highly interconnected "neurons" operating in parallel, rather than from a sequence of logical or mathematical operations that define some input/output behavior. For truly fast operation, you can implement a neural network on a specialized chip. The fastest neural-network chip, Intel's ETANN 80170, can cycle through a complete network with up to 128 inputs and 64 outputs in about 3 μsec. It interfaces to either analog or digital signals.

Time and size considerations can make or break a neural-network implementation. **Table 1** offers some guidelines for the response time of various-sized networks running on different chips, boards, and computers.

The following application demonstrates several ways neural networks can be useful. Suppose you want to automate the assembly and test of a 5V dc/dc-converter circuit board. Although conventional board-stuffing equipment is adequate for handling common resistors and capacitors, power supplies have nonstandard parts, such as transformers and inductors, that usually require hand installation. You'll need a more flexible robotic system to handle such parts. Because parts like these can't be lead-taped, the insertion machine will have to handle them in loose form. This kind of handling will require a machine-vision system to identify the part's orientation so that the robot can pick it up.

Because you would want this system to operate unattended most of the time, you should have it perform self-diagnostic testing. The system should also help reduce board-testing costs not only by automatically identifying a nonfunctional unit but also by diagnosing the probable cause of the failure. You can use a neural network to solve these three problems:

1) determining the orientation of parts for robotic insertion
2) performing diagnostics on the robotic equipment
3) testing the completed circuit board and diagnosing component failures.

You should apply the three evaluation steps discussed earlier to determine whether to use a neural network to solve these three problems.

You have two parts, a transformer and an inductor, which you want the robot to insert. Both parts are encapsulated in rectangular potting forms with radial leads on a 0.250-in. pitch. The robot fingers need to align within 20° of the sides of the part for the fingers to properly pick it up. A vibratory feeder delivers parts to a table where they land with random orientation. A camera forms an image of each part delivered by the feeder. The system must process the picture data and assign one of the eighteen (360°/20° = 18) possible orientations to the part. It also must be able to determine the orientation regardless of the location of the part within the camera's field of view.

You can set up the system to determine the orientation of the part in two steps. First, locate the part in the camera's field of view. You can do this by training a neural network to output the location of the center of the part. Another way to do this is to use traditional methods such as calculating the centroid of the part. Once the system has located the center, it can determine the part's angular orientation. You can use a neural network to classify the part's orientation into 1 of 18 categories.

The camera image is 1024 pixels on a side, but you cannot train a network with that many inputs (over a million) in a reasonable amount of time. So you'll have to do some preprocessing of the raw camera data to reduce the problem size, first by locating the center of the part, and second by focusing in on the area around the part. Then the system can determine the orientation. Simply tiling the picture will provide you with data that you can apply to the neural network.

Table 1—Running speed of representative neural-network implementations[1]

	Number of inputs/outputs			
Computer or chip	**20/2**	**100/10**	**1000/10**	**4000/20**
80286 8-MHz PC	0.0039	0.0975	8.221	130.26
80386 25-MHz PC	0.00086	0.02150	1.8129	28.724
80486 33-MHz PC	0.00041	0.01018	0.86428	13.694
Brainmaker Professional Accelerator Board[2]	0.000081	0.00204	NA[3]	NA
Micro Devices MD 1220 chip	0.000024	0.000611	0.0506	0.8016[4]
Brainmaker Accelerator Board	0.000006	0.000153	0.01265	0.20206
Intel 80170 ETANN chip	0.00000012	0.000003	NA	NA

Notes: 1. The number of hidden neurons is estimated at half the number of inputs plus outputs. The speed, in seconds, is the response time of the trained neural network while running. Training times will be greater. Software speed estimates are for the Brainmaker software package; speeds for other packages may differ. Relative speed differences among computers should be similar for other neural-network software packages.
2. 512 inputs max
3. Not applicable
4. Estimated

Tiling means grouping some adjacent pixels (a 16×16 square in this case) into a single value. The first neural network outputs the location of the center of the part, and this data restricts inputs to the second network to just the pixel information from the area local to the part. **Fig 2** depicts the two networks. You train the first network simply by providing it with sample pictures of the part in various locations along with the center X and Y coordinates.

The area surrounding the part takes up ¼ of the full field of view or 512×512 pixels. But a network with this many inputs may take weeks to train, so you can tile the 512×512 area down to 64×64. In a case like this, all the system has to do is identify the orientation of the part's edge that has the leads on it, so losing some granularity is not important.

The second orienting network will need at least a few hundred training examples. You can easily generate these by rotating the part in 0.1° steps. At each step, save the camera's output along with the orientation of the part. The input to the neural network is a layer of 4096 neurons, one for each pixel. The output is a layer of 18 neurons, one for each of the 20° orientation ranges. For each of the training examples, you set the output neuron for the correct range to fully on and the other 17 to fully off.

Path control is another, more-complex application from assembly robotics that neural networks can solve. Once the network has determined the initial orientation of the part and the final orientation required for insertion, another neural network can control the X-, Y-, or Z-axis motion of the insertion device as it picks and places the part (**Refs 4** and **5**). Rather than use tensor math (which is slow and hard to calculate), you could input starting coordinates and desired end coordinates to a neural network and train it to output a path.

For this assembly system, you can afford to wait until the robot has finished handling a part to have the neural network assess the orientation of the next one. Therefore, the system only needs to process a view of one part at a time. An 80486 PC runs the neural network fast enough that it has time to perform frame grabbing and still maintain adequate throughput. So you can implement the network in software on the same PC that hosts the frame-grabber board for the camera. Where you need faster results, the network can run on accelerator boards, which give 10 to 100 times greater throughput. For truly demanding applications, the trained network can run on a special-purpose neural-network chip like Intel's 80170 for performance several thousand times faster than a '486.

Frequently, problems on automated assembly lines do not appear until a defective finished product reaches the inspection and test stations. By the time the first bad product turns up, the pipeline may be full of several hours' worth of defective goods that need rework or have become scrap. Diagnosing the assembly equipment's problem as soon as it occurs is much more efficient. In the case of a power-supply circuit board, rework is feasible but very expensive, because the machine-installed parts must be removed by hand. To diagnose equipment failures, you need access to some signals that reliably describe the system's behavior.

Servos control both the positioning of the head and the gripping force of the fingers on the robotic insertion machine. The commands that control the actuator and the sensor-feedback signals are available for you to

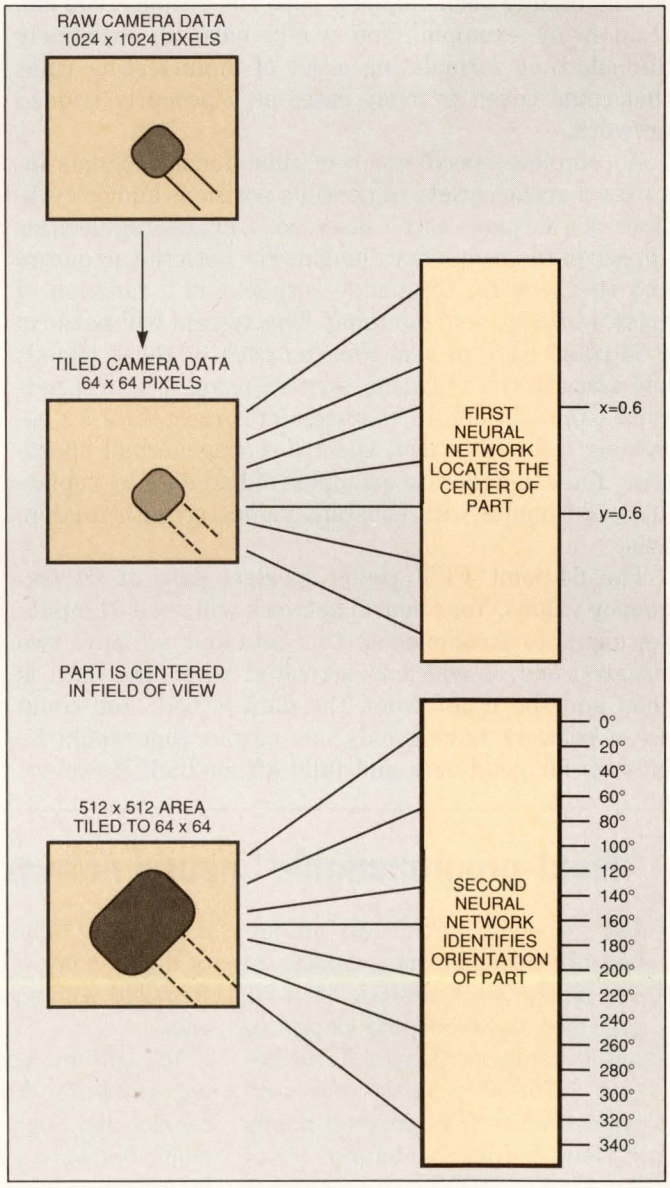


Fig 2—Two neural networks operate together on input from a frame grabber. First, one locates the center of a part. Then the other identifies the part's angular orientation.

observe. What you need is a method of deducing the state of the equipment from the behavior of these signals. As one simple test, you could check that the signals are all within range. Many problems would not be detected by such a scheme, however. For example, the servo amplifier driving the brushless dc motor that rotates the robot's wrist could oscillate because of a failed compensating capacitor. In this case, the wrist could be within legal range but still fail to place parts.

You need some method to look at all the signals in relationship to each other and determine if the pattern is valid or not. A neural network is an ideal tool for characterizing such complex patterns because you can train it by example. You would have an extremely difficult time formulating a set of input-testing rules that could cover as many cases as a properly trained network.

A complete specification of time-domain signals involves a great variety of possible positions and orientations of the parts to be inserted. Certain regularities appear in the frequency domain. For both the actuators and the sensors, frequency response is a function of mass, stiffness, and damping. The system will perform a 64-point FFT in real time on each of these signals and classify the resulting spectra using a neural network. You can obtain examples of correct data by recording a few thousand spectra during normal operation. You can generate examples of bad data by replacing valid inputs with constant values or with random noise.

The 64-point FFT yields spectral data at 64 frequency values. Your neural network will need 64 inputs per signal to accommodate this data and will have two outputs, one of which is activated when the data is good and the other when the data is bad. You could use a network having only one output that would be fully on for good data and fully off for bad. However, using two outputs with complementary values often results in a network that is easier to train because it doubles the number of internal network node weights that you can adjust.

Two linear and four rotary motors control the assembly robot. Each motor has an optical position encoder. One of the linear motors controls the part-gripping fingers, which also have a force sensor. As a result, the system has to analyze 13 signals. The system has 64 inputs per sensor (resulting from the 64-point FFT), so you need a network with $13 \times 64 = 832$ inputs. The system components have bandwidths of approximately 10 Hz, requiring samples to be taken 20 times a second. So the neural network must process inputs in 50 msec to make use of all the data generated. For this network size, 50 msec is about ten times faster than a '486 performs, so you would need to implement this network on a dedicated PC that has an accelerator card.

Diagnosing circuit-board faults

The power supply has three functional blocks: the switching circuit, which controls the transfer of energy from the input to the output; the control circuit, which determines how the switching circuit operates; and the feedback circuit, which measures the output voltage and current and provides error signals to the control circuit. In this case, the power supply is an off-line forward converter with fixed-frequency PWM control. A test fixture automatically varies the line and load. The problem consists of gathering and analyzing data that will tell you whether the circuit is operating correctly. If it is not, you would also want to know which component is at fault. Your methods of analyzing the data should tolerate the effects of normal component variation.

The network should identify four common component

"Field-programmable" neural networks

Two recently introduced neural-network development products let you design your network on a PC and then download the design to run in hardware. Neural Technologies' NT5000 system is one such system, which EDN covered briefly in News Breaks section (pg 24) of the May 7, 1992, issue. Another is the Intel 80170 development system. This board works in PCs having a 80286 or better CPU to program or train the Intel ETANN (Electrically Trainable Analog Neural Network) chip.

You can test your pattern set using software that simulates the ETANN chip, such as California Scientific Software's Brainmaker Back-Propagation simulation software, then download your trained-network file and pattern file to the chip. Alternately, you can perform "chip-in-the-loop" training; that is, use the development system to apply your patterns directly to the chip. If you use direct training, the chip can learn around variations and defects in its own processing elements. Because the chip uses EEPROM technology, both programming approaches allow you to change the weights many times.

problems: low error amp gain, incorrect filter inductance, incorrect transformer turns ratio, and high filter capacitor ESR (equivalent series resistance).

A system based on formal rules would soon become overwhelmingly complex because of the number of line and load conditions that it would have to test to ensure that the circuit functioned properly. A neural network, on the other hand, can much more easily learn complex relationships among data and recognize patterns that are similar (but not identical) to those it was trained on. It also can generalize between example data points. A neural network trained with examples of single failures can even extrapolate for cases of multiple simultaneous failures (**Ref 6**).

Although the supply switches at 100 kHz, a number of relatively low-bandwidth signals are available for you to look at to get a good idea of the state of the circuit. These are the error amp's output voltage, the supply's output voltage and current, the input voltage, and the supply's ripple voltage. An active peak-detection circuit measures the magnitude of the output ripple. (A lowpass filter precedes this circuit to prevent noise spikes from corrupting the measurement.) You measure ripple to detect fault conditions, such as subharmonic oscillation, that may not show up in the other indicator signals because of their low bandwidth. After multiplexing and A/D conversion, these signals become inputs to your neural network.

This network is relatively small (five inputs and four outputs), so you can train it adequately on a few hundred examples. You can generate five hundred examples by taking all combinations of 10 different values of line and load, both with and without single-component failure. In this case, because none of the categorized failure modes are catastrophic, you can easily generate the data experimentally. If a good model of the supply were available, you could even generate the data by simulation.

The closed-loop bandwidth of the supply is 100 Hz. Sampling the signals at 250 Hz requires a 4-msec processing time for the network, which is much faster than the requirement for the robot diagnostic network. Because this network is so much smaller, though, it can run in under 1 msec on a '486. This network can run on the same PC that hosts the data-acquisition card that converts the input signals.

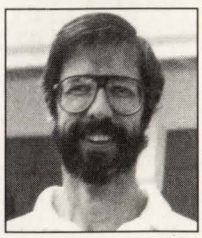
Engineers use neural networks in signal processing, data analysis, robotics, modeling, production control, assembly, and thousands of other areas. You can expect many more applications in coming years, and being able to creatively use this technology will give you an advantage in many designs. As faster and larger neural-network chips become available, taking advantage of this technology may become a requirement for keeping a competitive edge. EDN

References

1. Nguyen, Derrick and Bernard Widrow, "Neural Networks for Self-Learning Control Systems," *IEEE Control Systems Magazine*, April 1990, Vol 10, No. 3, pp 18-23.
2. Widrow, B and R Winter, "Neural Nets for Adaptive Filtering and Adaptive Pattern Recognition," *IEEE Computer*, March 1988, Vol 21, No. 3, pp 25-39.
3. Kagle, B, et al, "Multi-fault Diagnosis of Electronic Circuit Boards Using Neural Networks," *Proceedings of IEEE International Neural Network Convention*, June 1990, Vol II, pp 197-202.
4. Sanner, Robert M and David L Akin, "Neuromorphic Pitch Attitude Regulation of an Underwater Telerobot," *IEEE Control Systems Magazine*, April 1990, Vol 10, No. 3, pp 62-68.
5. Handelman, David A, Stephen H Lane, and Jack J Gelfand, "Integrating Neural Networks and Knowledge-Based Systems for Intelligent Robotic Control," *IEEE Control Systems Magazine*, April 1990, Vol 10, No. 3, pp 77-87.
6. Lawrence, Jeannette, "A Diagnostic Neural Network for Chip Fabrication," November 1990, California Scientific Software, Grass Valley, CA.
7. Lawrence, Jeannette, *Introduction to Neural Networks*, April 1991, California Scientific Software, Grass Valley, CA.
8. Wright, Maury,"Designing neural networks commands skill and savvy," *EDN*, December 5, 1991, pg 86.

Authors' biographies

Jeannette "Jet" Lawrence has held positions at California Scientific Software in the areas of public relations, technical publications, and support. She has worked with neural networks since 1988 and software and electronics since 1979. She is the author of the book, Introduction to Neural Networks.



Pete Andriola, president of California Scientific Software, has managed design of motor drivers, power supplies, and spaceborne sensor and power systems. He has also designed analog and digital circuits for medical instrumentation, industrial control systems, and logic analyzers. He holds BS and MSEE degrees from the California Institute of Technology.

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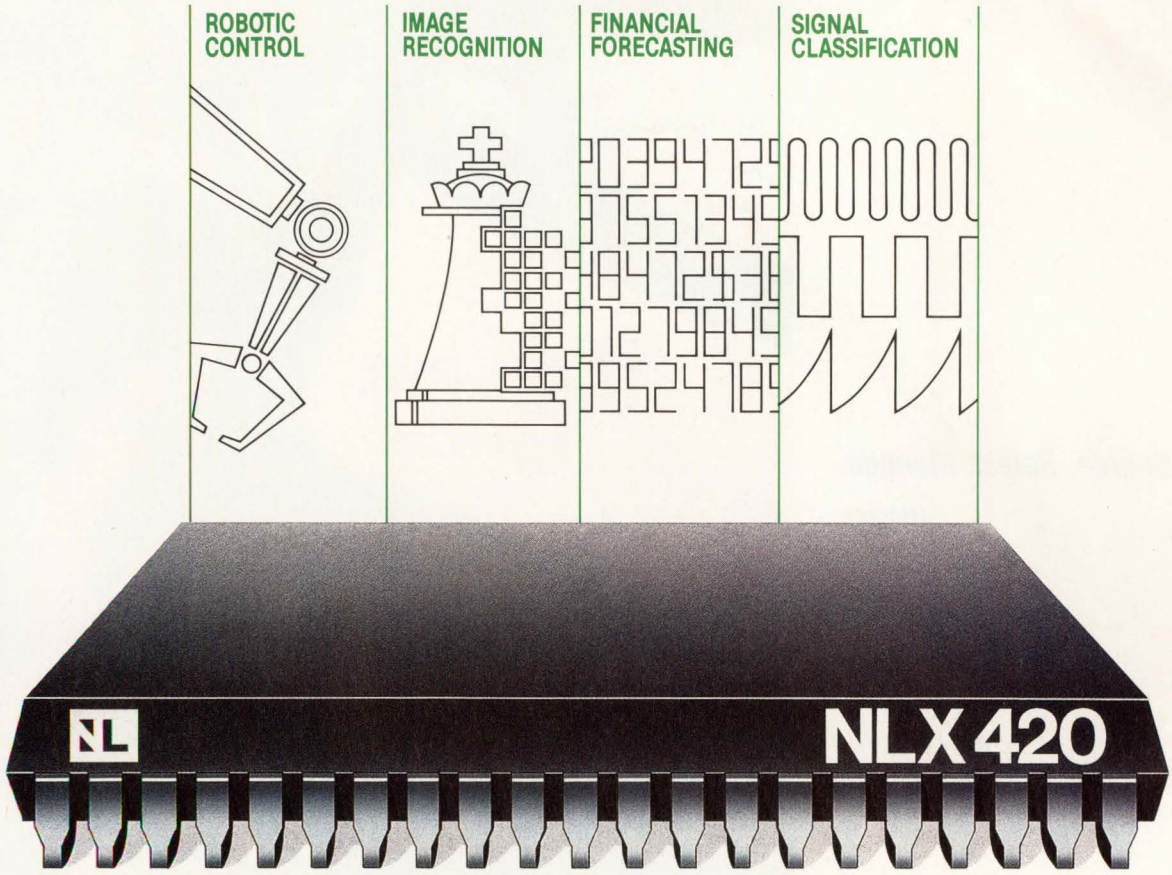

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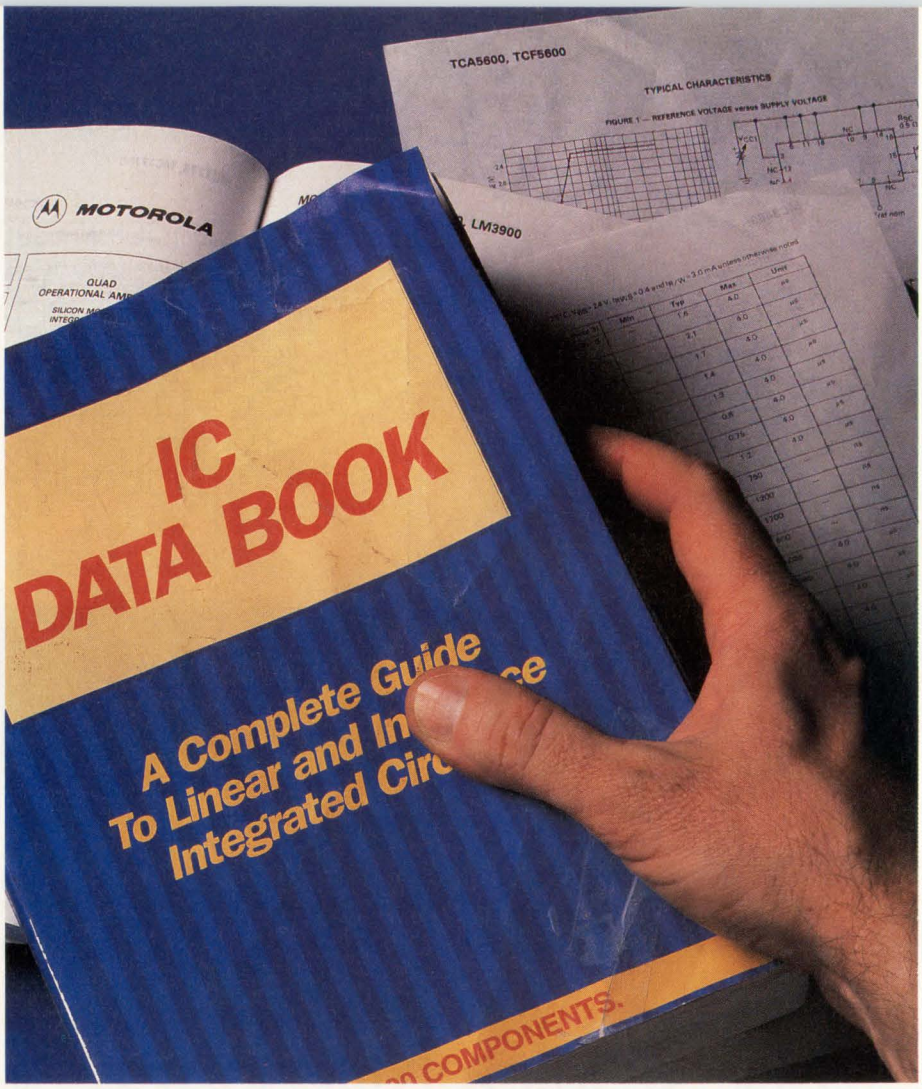

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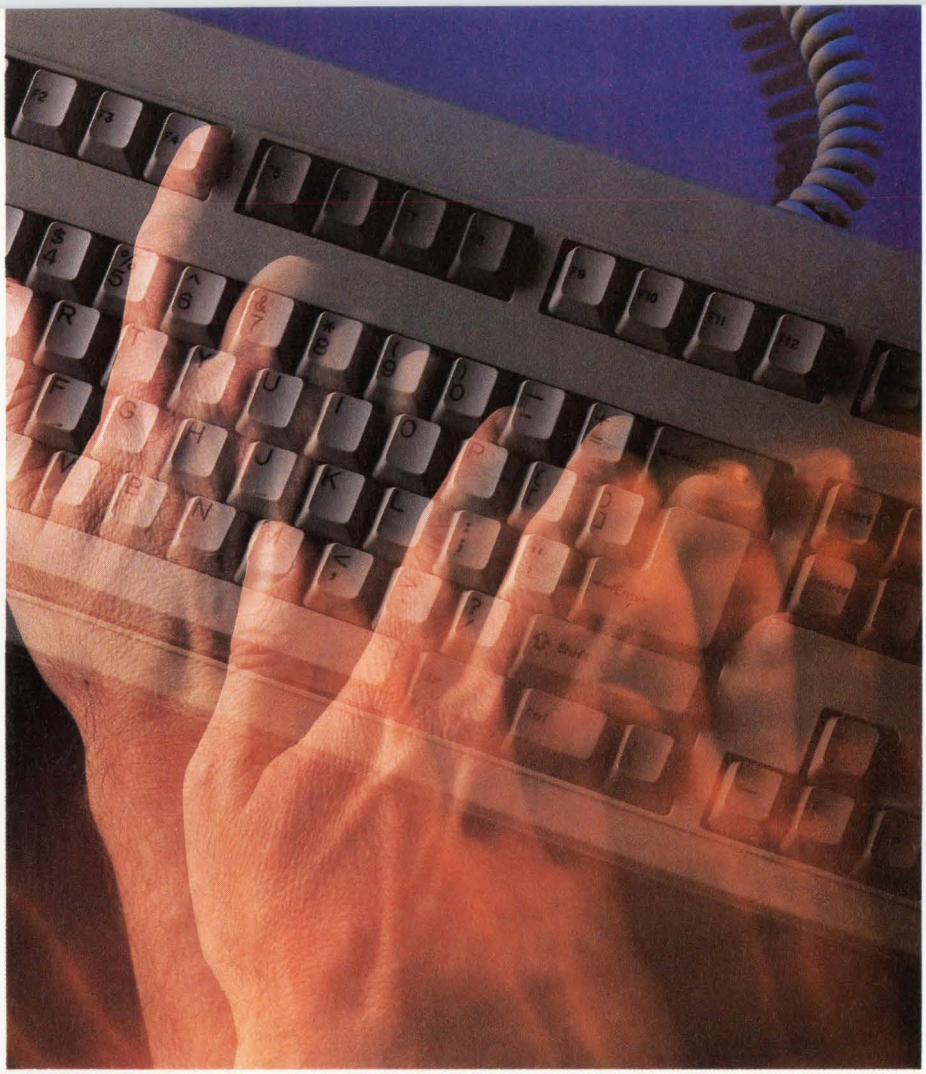

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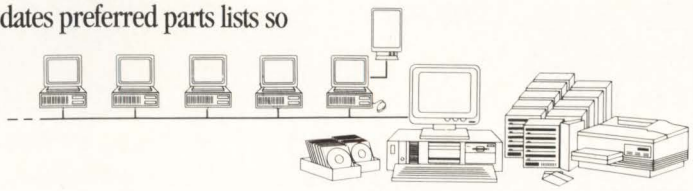

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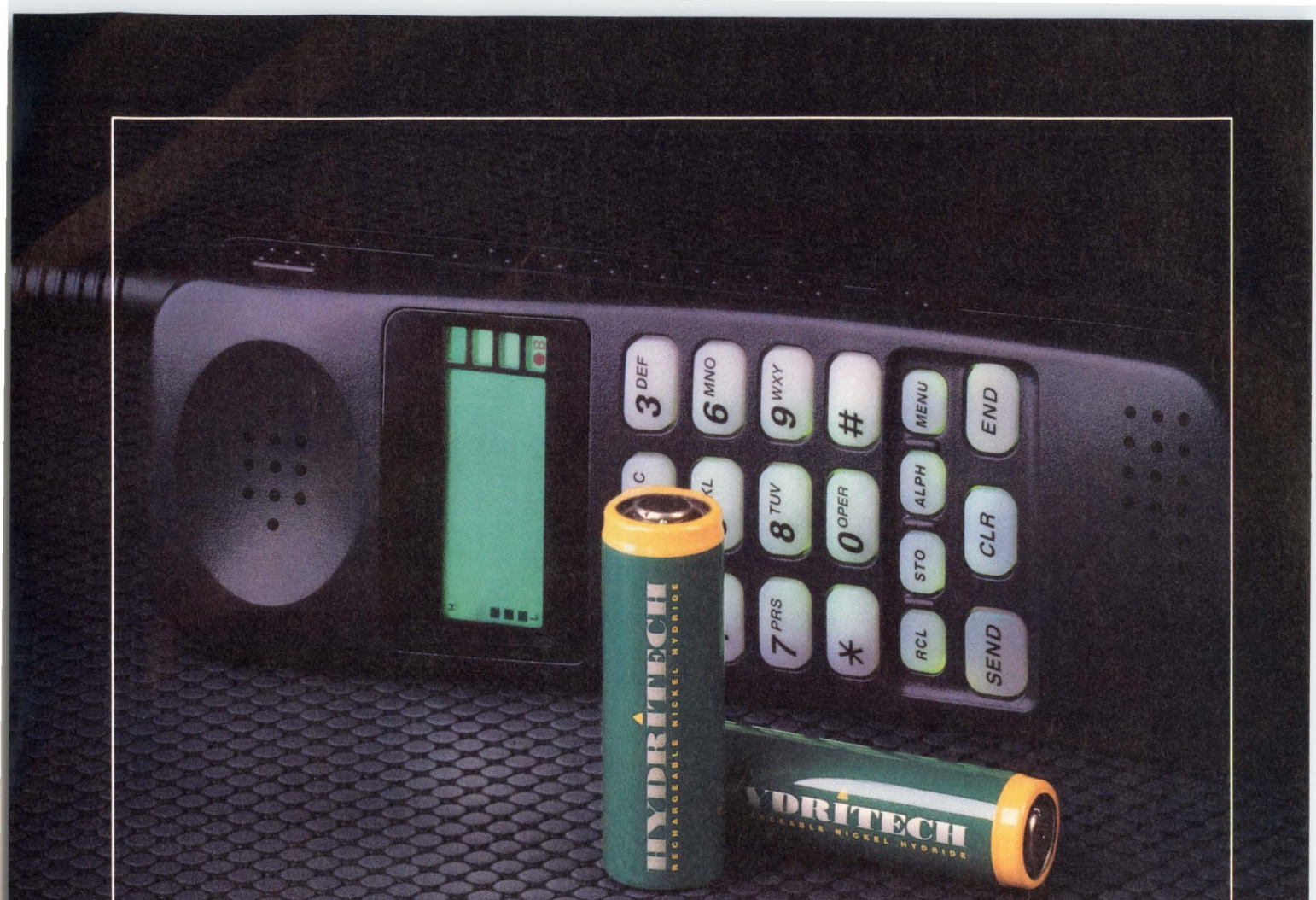

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Joel Martinez, National Semiconductor Corp

As bus transfer rates extend into warp speeds, large capacitive loads can behave like anchors. Low-capacitance backplane-transceiver-logic devices offer advantages over their TTL counterparts when you're trying to maximize throughput.

Speed is the most important consideration when defining a computer bus standard. In many systems the backplane often becomes a bottleneck when high-speed CPUs communicate with shared resources on the bus. The maximum data-transfer rate between two cards on a backplane largely depends on the maximum bus delay, which consists of the bus settling time and propagation delay. The bus settling time is the time required for reflections and crosstalk interference to subside before a receiver can reliably sample data on the bus. The propagation delay depends on the intrinsic inductance and capacitance of the bus media.

Improper bus terminations and inadequate bus drivers can cause the settling time to be several times longer than the propagation delay. For this reason, an IEEE committee defined the IEEE 1194.1 Standard for Electrical Characteristics of Backplane Transceiver Logic (BTL) Interface Circuits. A properly designed backplane using BTL interface circuits not only eliminates the bus settling time, but minimizes the propagation delay of a loaded backplane. BTL can produce the maximum bus throughput. To illustrate the effectiveness of BTL, contrast the bus delay for a transmission line using high-current TTL transceivers vs BTL transceivers.

Fast logic signals, which have rise and fall times significantly shorter than the bus' round-trip propagation delay, determine when to consider the backplane as transmission lines. Transmission lines have an unloaded characteristic impedance (Z_0) and an unloaded propagation delay (tp_0) given by

$$Z_0 = \sqrt{L_0 C_0} \qquad (1)$$

and

$$tp_0 = \sqrt{L_0 C_0}\,, \qquad (2)$$

where L_0 equals the unloaded distributed inductance per unit length and C_0 equals the unloaded distributed capacitance per unit length.

High-speed backplanes often use strip lines (**Fig 1**) as the transmission medium. You can calculate the unloaded characteristic impedance and unloaded propagation delay of a stripline using the following formulas:

$$Z_0 = \frac{60}{\sqrt{\epsilon_r}} \ln\left[\frac{4h}{0.67p(0.8w+t)}\right] \qquad (3)$$

and

$$tp_0 = 1.017\sqrt{\epsilon_r}\,, \qquad (4)$$

where ϵ_r equals the relative dielectric constant of the insulation material, h equals the height between ground planes, w equals the width of the signal trace, and t equals the thickness of the signal trace.

A typical stripline backplane may have the following features:

$$h = 52 \text{ mils}$$
$$w = 12 \text{ mils}$$
$$t = 1.4 \text{ mils (1 oz copper)}$$
$$\epsilon_r = 3.5 \text{ (epoxy-glass).}$$

Substituting these values in **Eqs 3** and **4** produces

$$Z_0 = 70\Omega \quad (5)$$

and

$$tp_0 = 1.9 \text{ nsec ft.} \quad (6)$$

Eqs 3 and **4** let you calculate the parameters of an unloaded transmission line. In practice a backplane consists of plug-in cards having pc-board traces, vias, and connectors that capacitively load the transmission lines. The impedance of a capacitively loaded transmission line is lower than an unloaded line, and the propagation delay of the capacitively loaded transmission line is longer than an unloaded line. When the backplane has a uniformly distributed capacitive load, the loaded characteristic impedance and propagation delay are, respectively,

$$Z_L = \frac{Z_0}{\sqrt{1+\frac{C_L}{C_0}}}$$

and

$$tp_L = tp_0\sqrt{1+\frac{C_L}{C_0}},$$

where C_L equals the distributed load capacitance per unit length.

You can determine the unloaded distributed capacitance (C_0) using **Eqs 1** and **2** to get

$$C_0 = \frac{tp_0}{Z_0}.$$

For the calculated stripline values given in **Eqs 5** and **6**,

$$C_0 = \frac{(1.9 \text{ nsec/ft})}{70\Omega} = 27 \text{ pF/ft.}$$

To calculate the distributed load capacitance, you must make some assumptions for the slot capacitance associated with a connector on the backplane, pc-board traces, vias, and the bus transceiver's input capacitance. Connectors, pc-board traces, and vias typically contribute 3- to 5-pF total capacitance. First, consider the input-capacitive load for a high-current TTL transceiver driving the backplane. High-current TTL transceivers have an input capacitance ranging between 12 and 20 pF. Under a worst-case assumption, the total slot capacitance for a card using high-current TTL transceivers can be as high as 25 pF.

The distributed load capacitance per unit length is given by

$$C_L = \frac{1}{dSLOT}\left(\frac{12 \text{ in.}}{1 \text{ ft}}\right)C_{SLOT},$$

where d_{SLOT} is equal to the slot-to-slot spacing of adjacent cards on the backplane in inches and C_{SLOT} is equal to the slot capacitance. Under the assumption that the slot-to-slot spacing between adjacent cards is 0.8 in.,

$$C_L = \frac{1}{0.8 \text{ in.}}\left(12 \frac{\text{in.}}{\text{ft}}\right)(25 \text{ pF}) = 375 \text{ pF/ft.}$$

Using the above assumptions, the loaded characteristic impedance and propagation delay are, respectively,

$$Z_L = \frac{70\Omega}{\sqrt{1+\frac{375 \text{ pF/ft}}{27 \text{ pF/ft}}}} = 18\Omega \quad (7)$$

and

$$tp_L = 1.9 \text{ nsec/ft}\sqrt{1+\frac{375 \text{ pF/ft}}{27 \text{ pF/ft}}} = 7.3 \text{ nsec/ft.} \quad (8)$$

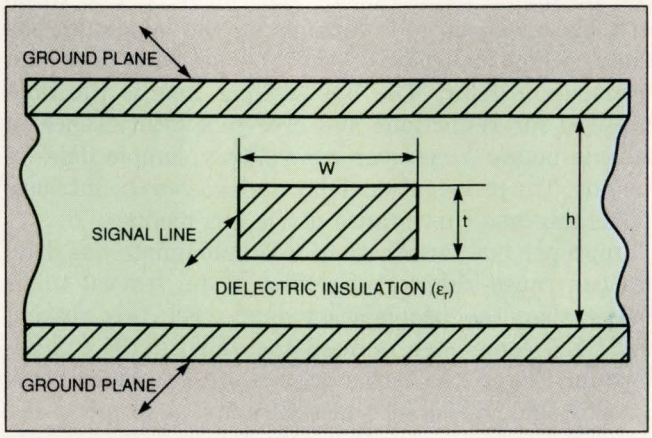

Fig 1—High-speed backplanes must rely on transmission-line characteristics. Striplining provides the advantages of two ground planes, which offer EMI shielding.

Comparing loaded transmission line calculations (**Eqs 7** and 8) with the unloaded transmission line calculations (**Eqs 5** and **6**) reveals that the distributed-capacitive loads increase the bus delay time in two ways. The most obvious impact is the increase in propagation delay from 1.9 to 7.3 nsec/ft. Lowering the line's characteristic impedance from 70 to 18Ω also increases the bus-delay time. A low characteristic impedance makes the transmission line harder to drive, which effectively increases the settling time.

Driving a split transmission line

To illustrate the effect that the line's impedance has on the settling time, consider a TTL transceiver driving a transmission line terminated on both ends by the line's loaded characteristic impedance (**Fig 2**). Because the driver must supply current in both directions, the transmission line presents a load of $Z_L/2$ to the driver. A TTL driver, which produces a nominal 3V swing, must deliver a current of

$$I_D = \frac{3V}{\left(\frac{Z_L}{2}\right)} = \frac{3V}{\frac{18\Omega}{2}} = 333\ \text{mA}.$$

The required drive current is much larger than the current capacity for standard high-current TTL transceivers, which ranges from 50 to 100 mA. **Fig 3** shows the bus settling time when a typical 50-mA transceiver drives a loaded characteristic impedance of 18Ω. Initially, the voltage waveform traveling on the bus is 0.45V, which is the product of the maximum drive current (50 mA) and half of the loaded impedance ($Z_L/2$). However, a 0.45V signal swing is considerably smaller than the upper TTL-threshold voltage necessary to guarantee a logic transition on the bus. Therefore, a receiver must wait several round-trip delays on the bus before sampling the signal.

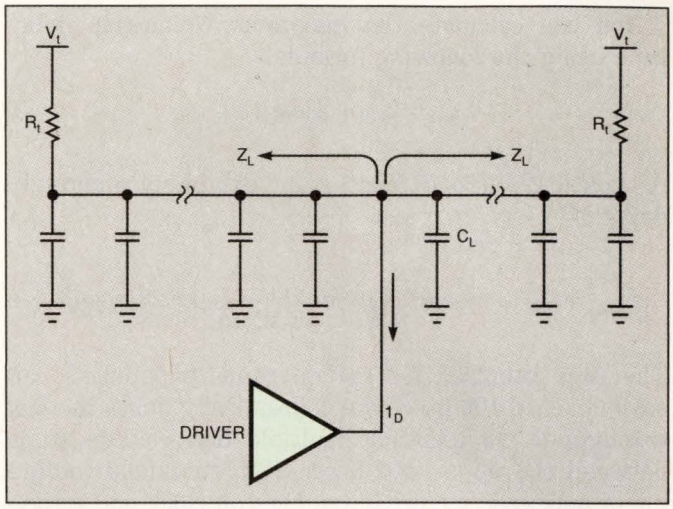

Fig 2—Bus drivers must have enough current drive to launch a voltage in two directions on the backplane. Initially, the line presents a load of $Z_L/2$ to the driver.

Futurebus + rides BTL transceivers into the future

Backplane-transceiver logic (BTL) is the interface circuit of choice for Futurebus+ backplanes. Chapters 6, 7, and 8 of the IEEE 896.2, "Futurebus+ Physical Layer and Profile Specifications" (**Ref 3**) define the electrical specifications for the Futurebus+ Profiles A, B, and F, respectively. The document specifies the unloaded backplane impedance (Z_O) without vias to be 67Ω, unloaded capacitance per unit length (C_O) of 29 pF/ft.

To determine the loaded capacitance per unit length, you must first estimate the capacitance/slot. The capacitance/slot is the sum of an estimate of the capacitance for the backplane via, the backplane connector, and the pc board. Some reasonable estimates yield

$$C_{SLOT} = C_{VIA} + C_{CONNECTOR} + C_{BOARD}$$
$$C_{SLOT} = 0.75\ \text{pF} + 0.45\ \text{pF} + 10\ \text{pF}$$
$$C_{SLOT} = 11.2\ \text{pF}.$$

Using the Futurebus+ slot-to-slot spacing of 30 mm (approximately 1.2 in.), the loaded capacitance per unit length is

$$C_L = 11.2\ \text{pF}\left(\frac{1}{1.2\ \text{in.}}\right)$$

$$\left(\frac{12\ \text{in.}}{\text{ft}}\right) = 112\ \text{pF/ft}.$$

Under the above assumptions, this fully loaded Futurebus+ backplane has a loaded backplane impedance of

$$Z_L = \frac{67\Omega}{\sqrt{1+\frac{112\ \text{pF/ft}}{29\ \text{pF/ft}}}} = 30\Omega\ . \quad (A)$$

The drive current required to launch a 1V signal on this backplane is

$$I_D = \frac{1V}{\left(\frac{30\Omega}{2}\right)} = 67\ \text{mA},$$

which is within the 80mA drive capacity of BTL transceivers.

Both the drive current and the signal swing determine the backplane-termination resistor. After extensive analysis and simulations, the Futurebus+ Electrical Task Group has determined that the optimum termination resistor should be 33Ω, ±1%. The calculated loaded impedance in **Eq A** is within the specified tolerance. The Task Group also specifies a termination voltage of 2.1V ±2%.

BTL Transceivers

You can calculate the maximum round-trip delay time using the following formula:

$$t_{(2d)} = 2(tp_L)(\text{length}).$$

A typical 19-in. loaded backplane exhibits a round-trip delay of

$$t_{(2d)} = 2(7.3\ \text{nsec/ft})(19\ \text{in.})\left(\frac{1\ \text{ft}}{12\ \text{in.}}\right) = 23\ \text{nsec}.$$

The time required for several round-trip delays can easily exceed 100 nsec, which drastically limits the bus throughput. In addition, multiple line voltage steps between the upper and lower TTL threshold-voltage limits may cause multiple triggers on clock and strobe lines, leading to catastrophe.

Higher-current drivers and precision receivers that have narrow voltage region between threshold limits can alleviate multiple triggers by ensuring the first voltage transition exceeds the maximum voltage threshold. The high-current drivers and precision receivers are often used for the clock and strobe line to eliminate multiple triggers. However, wide-data and -address buses present practical limits. The significantly higher current necessary to drive 32- and 64-bit data and address buses often precludes the use of very-high-current drivers. In addition, higher current transceivers exhibit higher input capacitance, which in turn further lowers the loaded line impedance and demands larger drive currents. The situation is a Catch 22.

Diode is a capacitance buffer

Next consider the bus delay for a transmission line using BTL transceivers. The IEEE 1194.1 standard specifies that the maximum I/O capacitance for a BTL transceiver should be 5 pF or less. To meet this low-capacitance specification, BTL transceivers use a Schottky diode in series with an open-collector driver output (**Fig 4**). The small reverse-biased capacitance of the diode isolates the driver's open collector capacitance when the transceiver is receiving data. The Schottky-diode capacitance is typically less than 2 pF, which varies slightly with drive current. Allowing a maximum of 2 pF for the receiver's input capacitance produces a total BTL-transceiver I/O capacitance of less than 5 pF.

BTL transceivers have other features that contribute to fast, reliable bus throughput. For example, the maximum voltage swing on the bus is 1V when you use BTL transceivers, instead of 3V for TTL transceivers. The low-voltage swing not only reduces the current drive requirements, it also reduces induced crosstalk noise between bus lines. The lower voltage swing doesn't make BTL transceivers more susceptible to bus-generated noise either. The reason is that the IEEE 1194.1 standard specifies a precision receiver threshold centered between 1 and 2.1V logic levels.

The tightly controlled threshold region extends ±75 mV about a nominal 1.55V level and is independent of power supply and temperature variations (**Fig 5**). BTL transceivers use a bandgap reference voltage to achieve the specification. Noise generated external to the bus can cause EMI problems, however. A shielded backplane, such as stripline, can eliminate EMI problems.

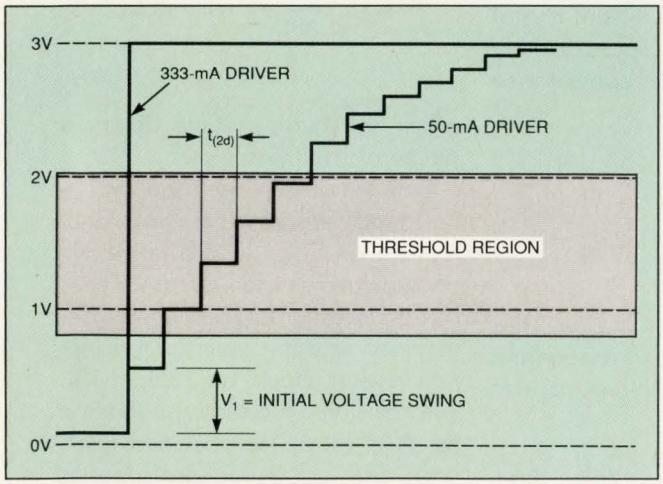

Fig 3—Insufficient current drive can result in many round-trip bus delays before a bus signal comfortably exceeds the TTL threshold region.

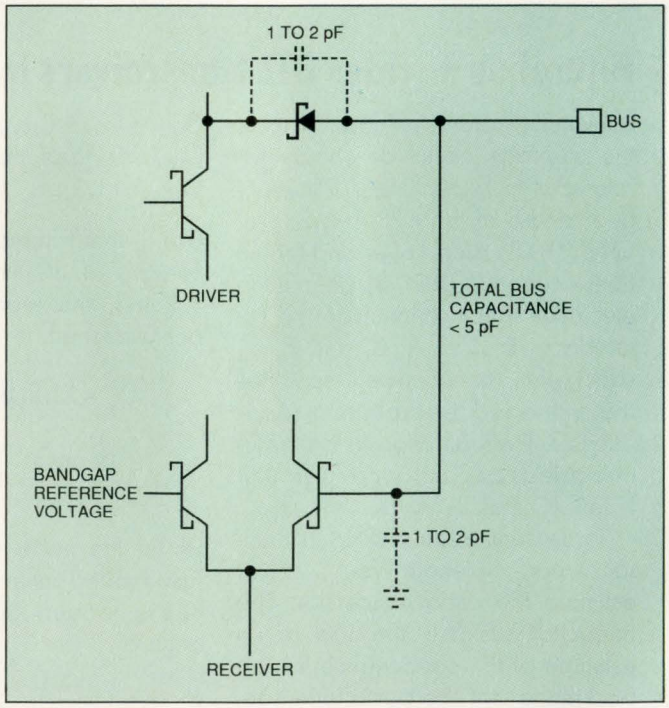

Fig 4—Typical BTL transceivers use a Schottky diode to isolate the capacitance of the driver transistor from the bus. Typical I/O capacitance of a BTL transceiver is <5 pF.

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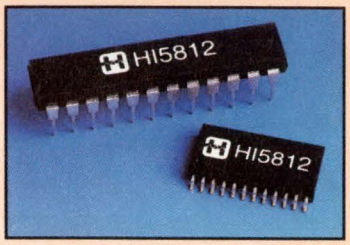


BTL Transceivers

When estimating the slot capacitance using BTL transceivers, you must add the transceiver's 5-pF I/O capacitance to the allotted 5-pF estimated capacitance for connectors, pc-board traces, and vias. The total estimated slot capacitance is 10 pF. The distributed load capacitance per unit length for the chosen transmission line is

$$C_L = \frac{1}{0.8 \text{ in.}}(12 \text{ in./ft})(10 \text{ pF}) = 150 \text{ pF/ft}.$$

The loaded impedance using BTL transceivers is

$$Z_L = \frac{70\Omega}{\sqrt{1+\frac{150 \text{ pF/ft}}{27 \text{ pF/ft}}}} = 27\Omega .$$

Because the loaded impedance is higher when using BTL instead of high-current TTL transceivers, the transmission line is easier to drive. The current necessary to launch a 1V BTL signal on the transmission line is

$$I_D = \frac{1V}{\left(\frac{27\Omega}{2}\right)} = 74 \text{ mA}.$$

BTL transceivers are capable of delivering 80 mA when you terminate the transmission line with its loaded impedance. Because the launched signal exceeds the threshold region by a comfortable noise margin on the first transition, BTL transceivers are capable of incident-wave switching even under worst-case load conditions.

BTL's low distributed load capacitance also contributes to a shorter propagation delay. The propagation delay for the chosen transmission line using BTL transceivers is

$$tp_L = 1.9 \text{ nsec/ftA}\sqrt{1+\frac{150 \text{ pF/ft}}{27 \text{ pF/ft}}} = 4.9 \text{ nsec}.$$

The propagation delay is 30% shorter than the delay using high-current TTL transceivers.

Transmission-line analysis is necessary to get the most out of a high-speed backplane. The large distributed capacitive loads associated with conventional TTL transceivers produce small backplane impedances and long propagation delays. The combination can slow down the backplane's throughput considerably. In contrast, the low I/O capacitance of a BTL transceiver can actually create a high-speed backplane. In addition, the smaller 1V signal swing reduces crosstalk and current-drive requirements. EDN

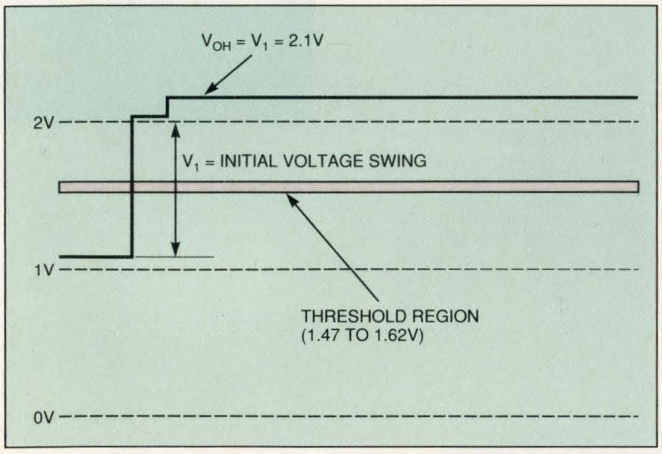


Fig 5—The combination of a tight threshold region, low-voltage swing, and high-current drive, lets a BTL signal comfortably exceed threshold on the initial voltage swing on the bus line.

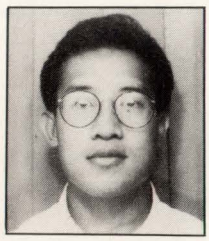
Acknowledgment

Special thanks to R V Balakrishnan's "IEEE 896 Futurebus—A solution to the bus driving problem," on which much of this article is based.

References

1. Balakrishnan, R V, "IEEE 896 Futurebus—A solution to the bus driving problem," National Semiconductor Interface Data Book, 1988.
2. IEEE 1194.1, "Electrical Characteristics of Backplane Transceiver Logic BTL Interface Circuits," 1990.
3. IEEE 896.2, "Futurebus+ Physical Layer and Profile Specifications," 1992.
4. Hayward, Michael, "Backplanes for Bus Systems," Hybrid Corp, 1989.
5. Standard Logic Inc, "High-Speed Printed Circuit Backplane Electrical Design Considerations and Signal Integrity," Technical Bulletin No. 0188.

Author's biography



Joel Martinez is an application engineer for National Semiconductor Corp's interface and peripherals group. In the past five years he has helped develop BTL and Futurebus+ products for the company. He also provides customer support for bus transceivers. Joel has a BSEE degree from San Francisco State University. He was the secretary for the IEEE 1194.1 committee and the draft editor for the 1194.2 Small Computer Expandability Module (SCEM).

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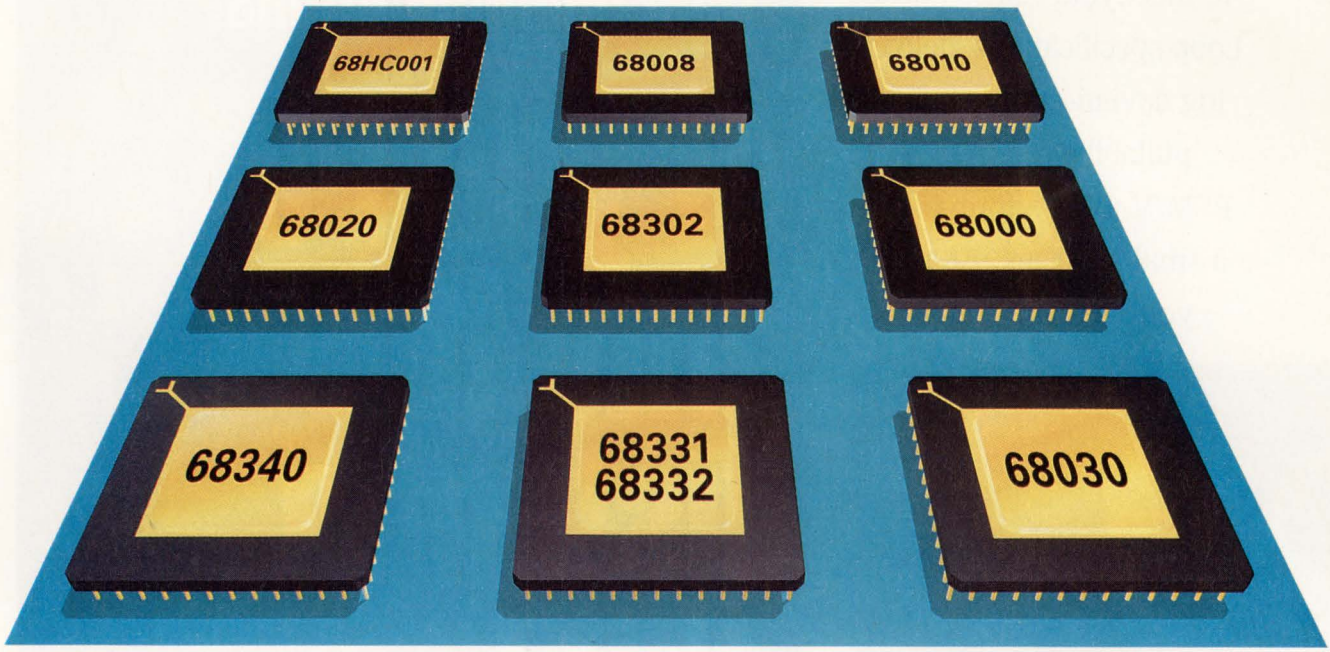

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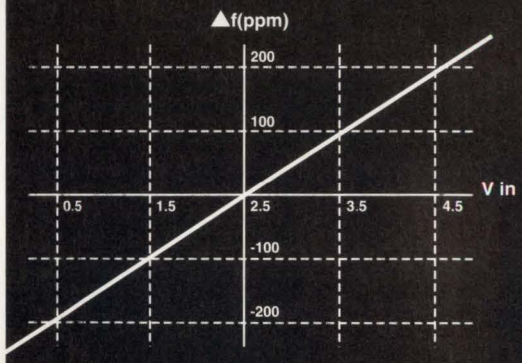

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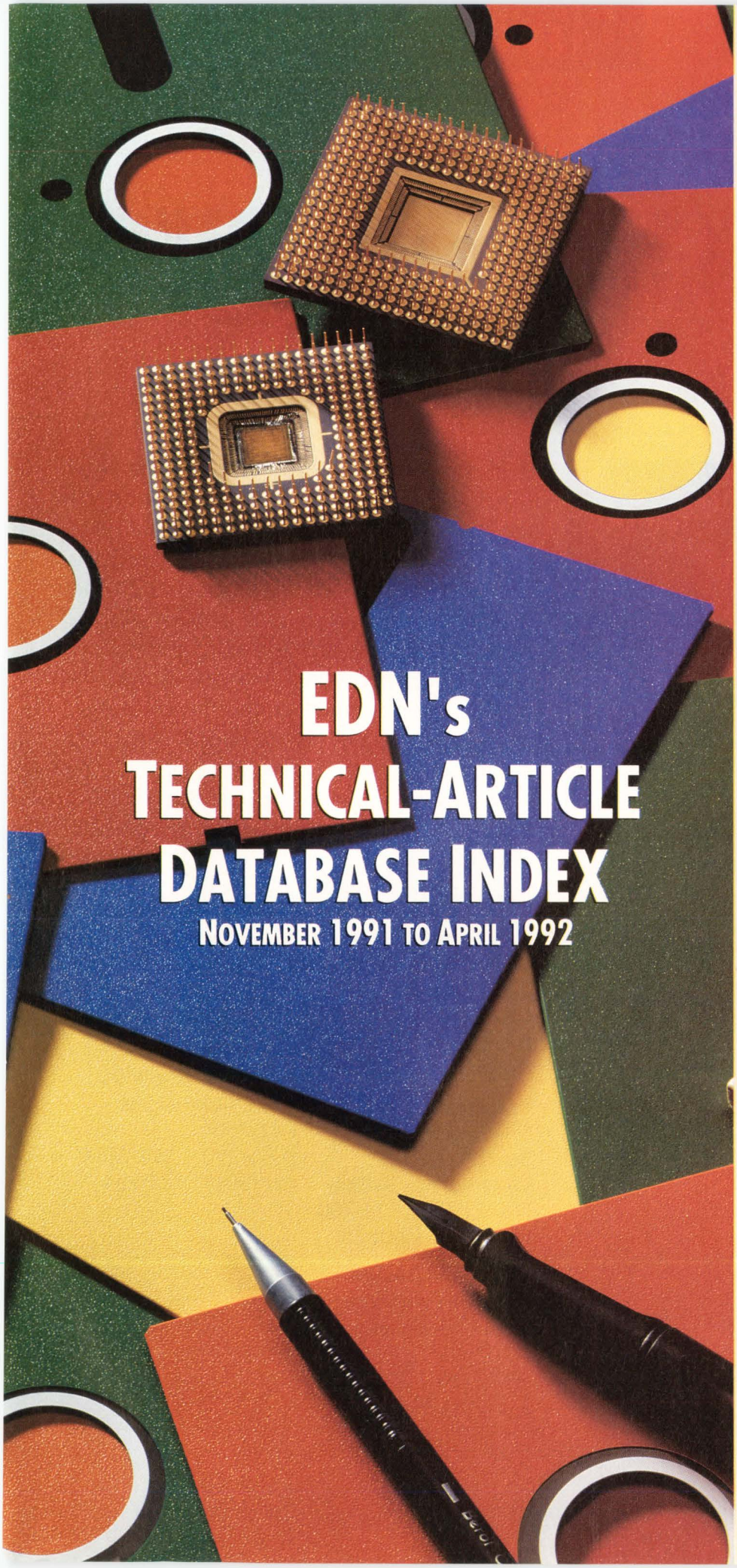

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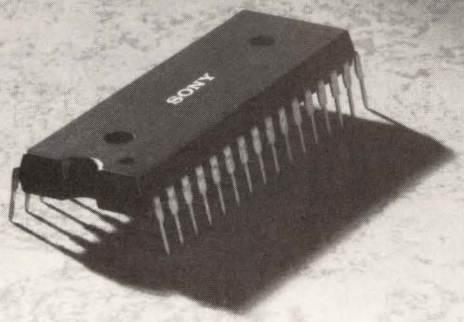

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Wescon/91. Ormond, Tom, Senior Editor; EDN Magazine, 11/07/91, pg 157, 3.5 pgs.

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Employment/labor relations/personnel/recruitment

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Cellular phone designs call for mixed-signal solutions. Wilson, Dave, Senior Editor; Computer Design, 12/91, pg 57, 6 pgs.

Converting PLD and FPGA designs to ASICs. Myrvaagnes, Rodney; Electronic Products, 02/92, pg 21, 4.5 pgs.
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Drive ICs: ASICs or off-the-shelf? Arnold, Bill, EDN News Staff; EDN News Edition, 11/28/91, pg 1, 1.5 pgs.
Laser-printer controllers get ASICs. Martin, Louis, and Jack Vaughan; EDN News Edition, 11/14/91, pg 1, 1 pg.
Mixed-signal ASICs: migrating to a true semicustom methodology. English, Nick, Palumbo, Mike, Harris Semiconductor; Electronic Products, 12/91, pg 25, 5.5 pgs.

Timer ICs/circuits

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Voltage references

Microamps sustain stable sources. Kerridge, Brian, Technical Editor; EDN Magazine, 03/30/92, pg 53, 4.5 pgs.

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Packaging/encapsulation/sealing

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Production/manufacturing/testing, other

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Technology/research

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Table-look-up scheme speeds software correlation

Domingo G Garcia, Texas Instruments, Dallas, TX

In digital-communications systems, a sync-frame code or preamble often delineates the start of a message transmission. Maximum-length sequences, Gold codes, and Barker codes are useful for this purpose because of their good autocorrelation properties. The correlation function of a specific bit sequence is as follows:

$$(1)\quad R(n)=\sum_{i=1}^{N-n}(r_i s_i+n)$$

At a particular sample instant, the correlation function compares the received sequence with a reference sequence and counts the number of matches. When the number of matches is greater than a specified threshold, frame synchronization is established. Assuming that the data rate is slow enough, software can perform the correlation function by replacing the multiplication operations with EXCLUSIVE-OR operations. For long sequences, performing the EXCLUSIVE-OR and sum operations on a bit-by-bit basis is impractical. Fortunately, most µPs can perform the EXCLUSIVE-OR operation on a word basis. Exploiting the word-wide EXCLUSIVE-OR operation and using a table-look-up scheme speeds up the correlation process by approximately a factor of three.

In this example, a TMS320C25 DSP µP implements a 1024-bit digital correlator. The TMS320C25 can perform a 16-bit by 16-bit EXCLUSIVE-OR operation in a single clock cycle. You can exploit this feature to reduce the number of multiply operations from 1024 to 64. However, for such a long sequence, the sum operation presents a problem. The problem is to determine the number of matches (zeros) in the resultant EXCLUSIVE-OR operations. Counting the matches normally involves testing each bit and accumulating the number of matches.

However, you can count the matches in blocks using a table-look-up scheme. **Listing 1**'s scheme (which you can also download from the EDN bulletin board) breaks up the result of the EXCLUSIVE-OR operation into 8-bit bytes and then uses these bytes as an offset into a table of length 256. Each table entry holds the number of zeros in the offset byte. The software retrieves the table entry and adds it to the ongoing sum.

EDN BBS /DI_SIG #1164 EDN

To Vote For This Design, Circle No. 746

Listing 1—Digital correlator using table-look-up scheme

```
*****************************************************************
* FUNCTION:  Performs a L=1024, 1-bit wide, Digital Correlation
*            and shifts the input sequence by one.
*****************************************************************
TEMP1   EQU     1               ; Block B0 variable storage.
TEMP2   EQU     2               ;      "
SUM     EQU     3               ;      "
BYTEMSK EQU     4               ;      "
MSBIT   EQU     5               ;      "
NEWBIT  EQU     6               ;      "
CORBUF  EQU     300             ; Starting address of input
*                               ; sequence to be correlated.
CORREF  EQU     340             ; Starting address of previously
*                               ; loaded reference sequence.
THRESHLD EQU    1000            ; Threshold value.
*
CORREL  EQU $                   ; INITIALIZATION.
        RSXM
        LDPK    4               ; Use Block B0.
        LACK    00FFh
        SACL    BYTEMSK         ; Mask to extract lower byte.
        ZAC
        SACL    SUM             ; Clear ongoing sum.
        LARK    AR2,63          ; Counter for loop.
        LRLK    AR1,CORREF      ; Load start of reference table.
        LRLK    AR0,CORBUF      ; Load start of buffer.
        LARP    AR0             ; Point to buffer.
*
        IN      NEWBIT,PA0      ; New bit is in LSB.
        LAC     NEWBIT          ; Place in accumulator.
        ANDK    0001h           ; Isolate the LSB.
*
LOOP0   EQU     $
        ADD     *,1             ; Shift in new bit.
        SACH    MSBIT           ; Store MSBit.
        SACL    *+,0,AR1        ; Save shifted data word.
        XOR     *+,AR2          ; Compare with Reference word.
        SACL    TEMP1           ; Store temporarily.
        AND     BYTEMSK         ; Extract lower byte.
        ADLK    ZEROTBL         ; Add table offset.
        TBLR    TEMP2           ; Get number of zeros in the byte.
        LAC     SUM
        ADD     TEMP2           ; Compute ongoing sum.
        SACL    SUM
        LAC     TEMP1,8         ; Extract upper byte.
        SACH    TEMP1
        LAC     TEMP1
        ADLK    ZEROTBL         ; Add table offset.
        TBLR    TEMP2           ; Get number of zeros in the byte.
        LAC     SUM
        ADD     TEMP2           ; Compute ongoing sum.
        SACL    SUM
        LAC     MSBIT
        BANZ    LOOP0,*-,AR0    ; Do for 64 times
*
        LAC     SUM
        SUBK    THRESHLD        ; Check for threshold exceedance.
        BGEZ    CORFND          ; Set threshold flag in acc.
        ZAC                     ; 0 : ( < threshold).
        B       DONE
CORFND  LACK    1               ; 1 : ( > or = threshold).
DONE    RET
```

Table 1—Example look-up table

```
*****************************************************************
* Table contains number of zeroes in offset location.
* Example: location offset 00 Hex has eight zeroes.
*          location offset FF Hex has no zeroes.
*****************************************************************
*
ZEROTBL EQU     $
        .word    8, 7, 7, 6, 7, 6, 6, 5, 7, 6, 6, 5, 6, 5, 5, 4
        .word    7, 6, 6, 5, 6, 5, 5, 4, 6, 5, 5, 4, 5, 4, 4, 3
        .word    7, 6, 6, 5, 6, 5, 5, 4, 6, 5, 5, 4, 5, 4, 4, 3
        .word    6, 5, 5, 4, 5, 4, 4, 3, 5, 4, 4, 3, 4, 3, 3, 2
        .word    7, 6, 6, 5, 6, 5, 5, 4, 6, 5, 5, 4, 5, 4, 4, 3
        .word    6, 5, 5, 4, 5, 4, 4, 3, 5, 4, 4, 3, 4, 3, 3, 2
        .word    6, 5, 5, 4, 5, 4, 4, 3, 5, 4, 4, 3, 4, 3, 3, 2
        .word    5, 4, 4, 3, 4, 3, 3, 2, 4, 3, 3, 2, 3, 2, 2, 1
        .word    7, 6, 6, 5, 6, 5, 5, 4, 6, 5, 5, 4, 5, 4, 4, 3
        .word    6, 5, 5, 4, 5, 4, 4, 3, 5, 4, 4, 3, 4, 3, 3, 2
        .word    6, 5, 5, 4, 5, 4, 4, 3, 5, 4, 4, 3, 4, 3, 3, 2
        .word    5, 4, 4, 3, 4, 3, 3, 2, 4, 3, 3, 2, 3, 2, 2, 1
        .word    6, 5, 5, 4, 5, 4, 4, 3, 5, 4, 4, 3, 4, 3, 3, 2
        .word    5, 4, 4, 3, 4, 3, 3, 2, 4, 3, 3, 2, 3, 2, 2, 1
        .word    5, 4, 4, 3, 4, 3, 3, 2, 4, 3, 3, 2, 3, 2, 2, 1
        .word    4, 3, 3, 2, 3, 2, 2, 1, 3, 2, 2, 1, 2, 1, 1, 0
```

Current loop transmits ac measurements

Mark Fazio, David Scott, and Bob Clarke, Analog Devices, Wilmington, MA

Process-control applications use current loops to send information as an analog signal over long distances with high noise immunity. Using the 3-chip circuit in **Fig 1**, you can measure alternating current or voltage and transmit the results on a 4- to 20-mA current loop. The circuit accepts a 0- to 10-mV ac rms input and provides a 4- to 20-mA output.

The input signal creates a floating voltage across sensing resistor R_{SENSE}, whose size produces 0- to 10-mV rms from the expected sensed current. This floating voltage is the input to a differential-input, single-ended AD22050 sensor interface (IC_1). IC_1 operates at a gain of approximately 20 and drives the low-impedance (8-kΩ) input (pin 1) of the AD736 rms-to-dc converter (IC_2). This converter's full-scale range is 200 mV rms. IC_2's output drives IC_3, an AD694 voltage to 4- to 20-mA current-loop interface.

Because of their low power consumption, both IC_1 and IC_2 can operate from the 10V supplied by IC_3's reference output at pin 7. IC_3, and hence the entire circuit, operates from the standard 24V loop supply. Because this circuit operates from a single supply, you must bias IC_2's common input at ½ of IC_3's 10V output, or 5V. The voltage divider comprising R_1 and R_2 divides the 10V to 5V. R_2 is in parallel with a 10-kΩ resistor inside IC_3.

IC_3's internal buffer amplifies the difference between IC_2's output at pin 6 and the 5V rail. This difference ranges from 0- to 200-mV dc for a 0- to 10-mV rms input and produces a 4- to 20-mA current output from IC_3. R_3 allows you to adjust the circuit's gain. R_4 and R_5 set the gain of IC_3's internal amplifier to 10. R_5 matches R_4 to prevent offsets due to the internal amplifier's input-bias current. This circuit's accuracy is 1.2% of readings from 20 Hz to 40 Hz and 1% of readings from 40 Hz to 1 kHz. The −3-dB bandwidth is 33 kHz. **EDN BBS /DI_SIG #1167** EDN

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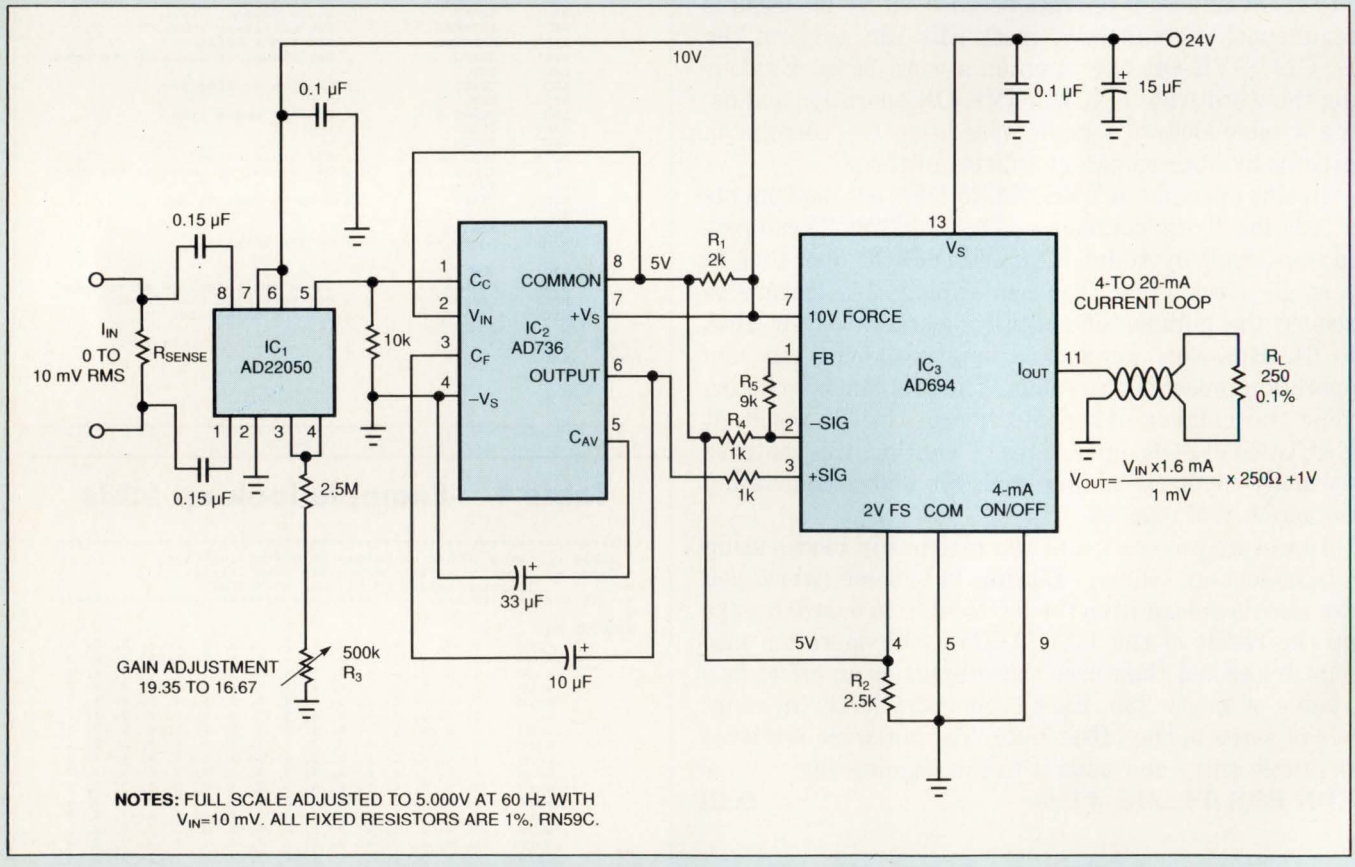

NOTES: FULL SCALE ADJUSTED TO 5.000V AT 60 Hz WITH V_{IN}=10 mV. ALL FIXED RESISTORS ARE 1%, RN59C.

Fig 1—This circuit measures alternating current or voltage and transmits the results on a 4- to 20-mA current loop.

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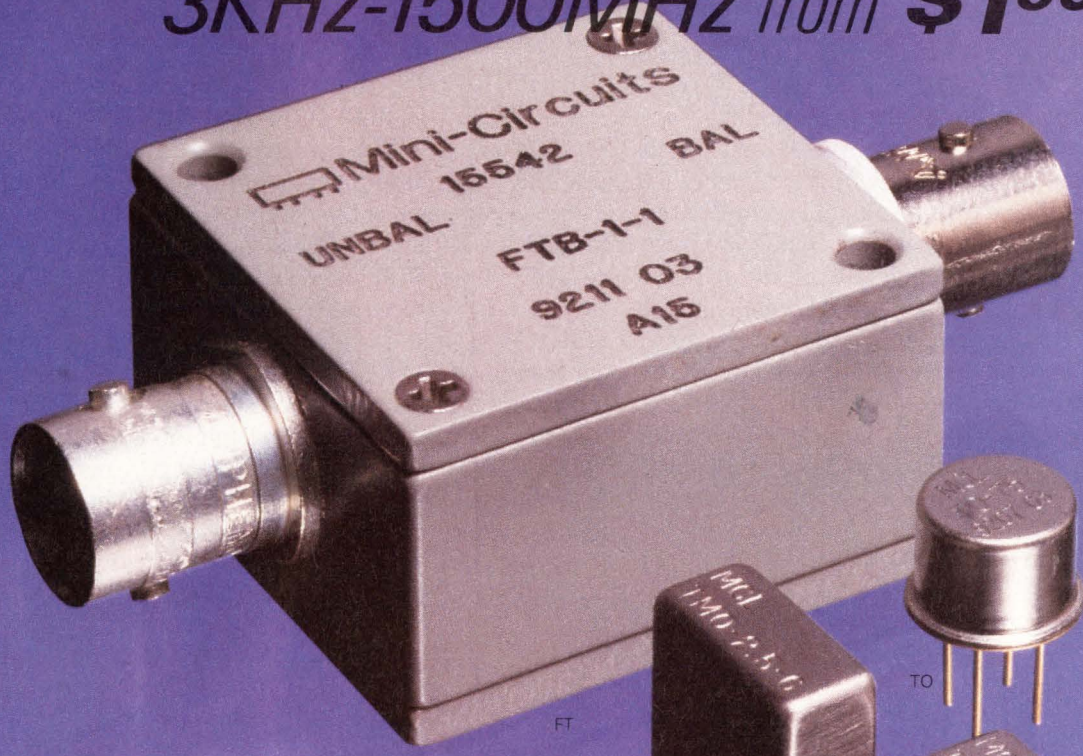

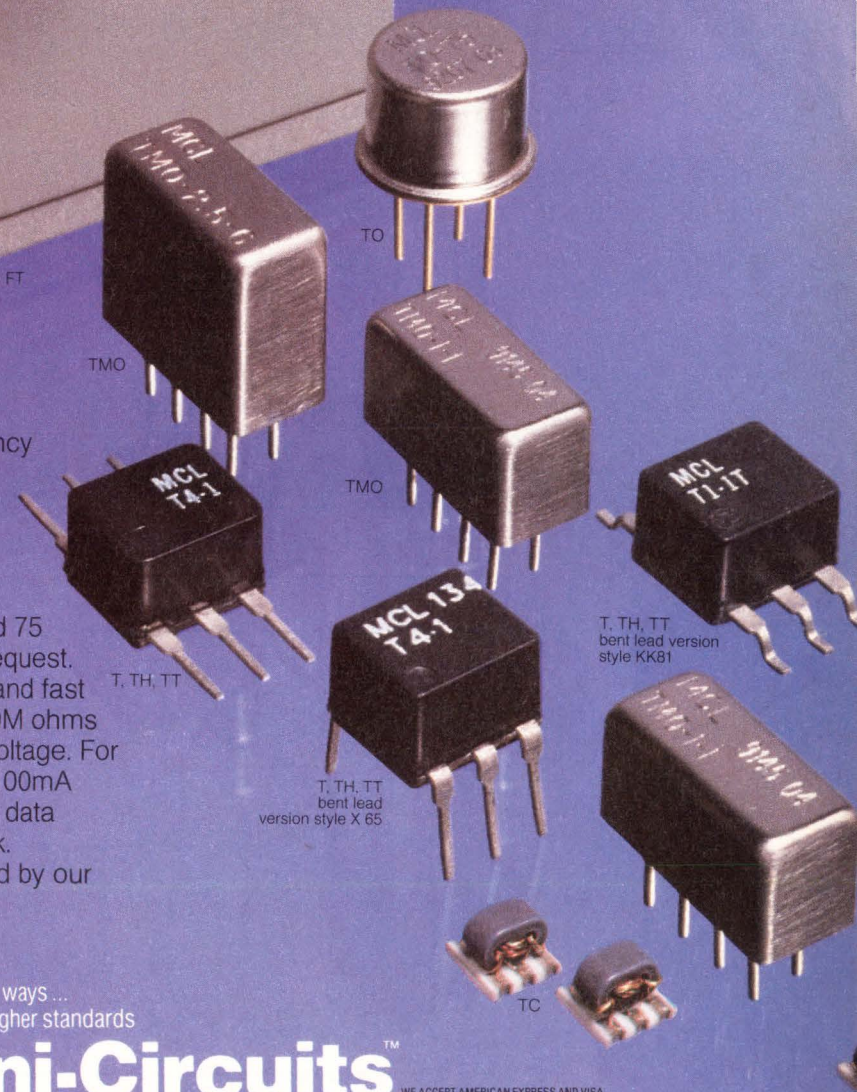

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CIRCLE NO. 68

F71 REV. C

Dual op amp takes absolute difference

Lindo St Angel, Motorola General Systems Sector, Arlington Heights, IL

A traditional implementation of an absolute-difference function comprises a difference circuit followed by an absolute-value circuit; the entire circuit requires at least three op amps. The design problem is complicated in single-supply-only systems, which usually require an artificial ground, typically one-half of the supply. The circuit in **Fig 1** takes the absolute value of the difference of two voltages using only two single-supply, ground-referenced op amps. The circuit is designed for dc or low-speed operation.

For the case where $V_1 > V_2$, IC_{1A} is disabled because diode D_1 is off. IC_{1B} and its associated resistors form a classic difference circuit where

$$V_{OUT} = (R_2/R_1)(V_1 - V_2).$$

For the case where $V_2 > V_1$, diode D_1 conducts, producing the composite amplifier system made up of both IC_{1A} and IC_{1B}, where

$$V_{OUT} = (R_2/R_1)(V_2 - V_1).$$

Using these two equations, the overall function of the circuit for V_1 and V_2 greater than zero is as follows:

$$V_{OUT} = (R_2/R_1)\,|(V_1 - V_2)|.$$

The circuit was built and tested with $R_1 = 10\ k\Omega$ and $R_2 = 220\ k\Omega$. For $V_2 > V_1$, the composite amplifier system has poor phase margin and is unstable. Thus, the circuit compensates the loop with the dominant pole formed by R_3 and C_1. At a gain of 22 and a desired response time of about 300 μsec (the 10 to 90% rise time when V_2 becomes 0.1V greater than V_1), values of $R_3 = 56\ k\Omega$ and $C_1 = 850\ pF$ produced the best empirical results. R_3 and C_1 will vary, depending on the required speed of the response and the closed-loop gain.

Also, when $V_2 > V_1$, the output of IC_{1A} becomes a function of the factor $2V_2 - V_1$. Thus, IC_{1A} may saturate for large values of V_2. The factor's upper limit is as follows, where V_{SAT} is the saturation voltage for IC_{1A}:

$$(2V_2 - V_1) < V_{SAT}(R_1 + R_2)/R_2.$$

For the LM2902 operating from 5V, V_{SAT} is approximately 3.5V. This last equation also implicitly sets a common-mode voltage (V_{CM}) limitation. You can see this limitation by setting $V_1 = V_2 = V_{CM}$ and allowing the factor $(2V_2 - V_1)$ to reduce to V_{CM}.

EDN BBS /DI_SIG #1168 EDN

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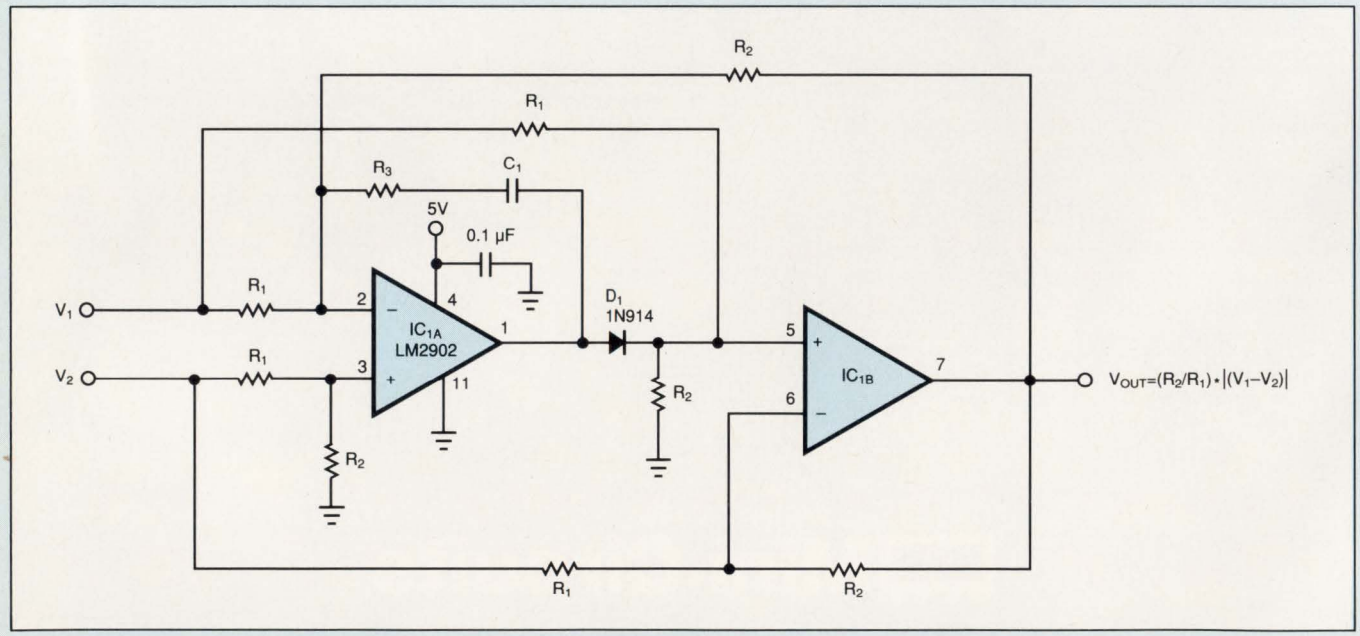

Fig 1—Using single-supply, ground-referenced op amps, this circuit accomplishes an absolute difference function.

LINEAR TECHNOLOGY

DESIGN NOTES

Peak Detectors Gain in Speed and Performance – Design Note 61

John Wright

Introduction

Fast peak detectors place unusual demands on amplifiers. High slew rate is needed to keep the amplifier internal nodes from overracing the output stage. This condition causes either a long overload, or DC accuracy errors. To support the high slew rate at the output, the amplifier must deliver large currents into the capacitive load of the detector. Compounding these problems are issues of amplifier instability with a large capacitive load, as well as the accuracy of the output voltage.

Detecting Sinewaves

The LT1190 is the ideal candidate for this application, with a high 400V/µs slew rate, large 50mA output current, and a wide 70 degree phase margin. The closed-loop peak detector circuit of Figure 1 uses a Schottky diode inside the feedback loop to obtain good accuracy. The 20Ω resistor R_O isolates the 0.01µF load and prevents oscillation. The DC error with a sinewave input is plotted in Figure 2 for various input amplitudes. The DC value is read with a DVM. At low frequency, the error is small and dominated by decay of the detector capacitor between cycles. As frequency rises the error increases because capacitor charging time decreases. During this time the overdrive becomes a very small portion of a sinewave cycle. Finally at approximately 4MHz the error rises rapidly due to the slew rate limitation of the op amp. For comparison purposes the error of an LM118 is also plotted for $V_{IN} = 2V_{P-P}$.

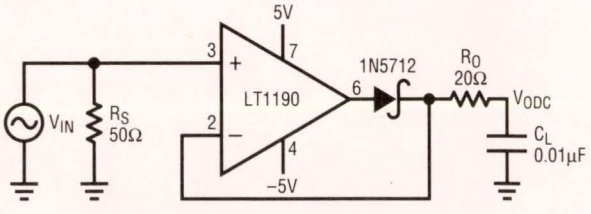

Figure 1. Closed-Loop Peak Detector

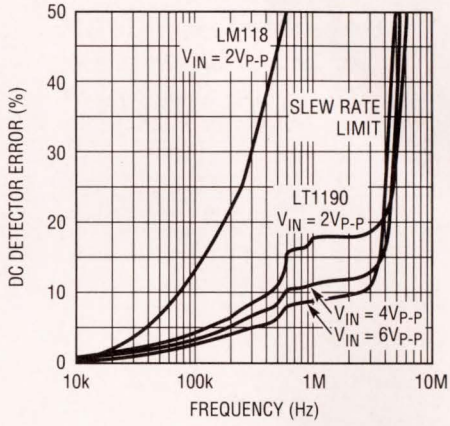

Figure 2. Closed-Loop Peak Detector Error vs Frequency

A fast Schottky diode peak detector can be built with a 1000pF capacitor, and 10k pull down. Although this simple circuit is very fast, it has limited usefulness due to the error of the diode threshold, and its low input impedance. The accuracy of this simple circuit can be improved with the LT1190 circuit of Figure 3. In this open-loop design, the detector diode is D1, and a level shifting or compensating diode is D2. A load resistor R_L is connected to –5V, and an identical bias resistor R_B is used to bias the compensating diode. Equal value resistors ensure that the diode drops are equal. Low values of R_L and R_B (1k to 10k) provide fast response, but at the expense of poor low frequency accu-

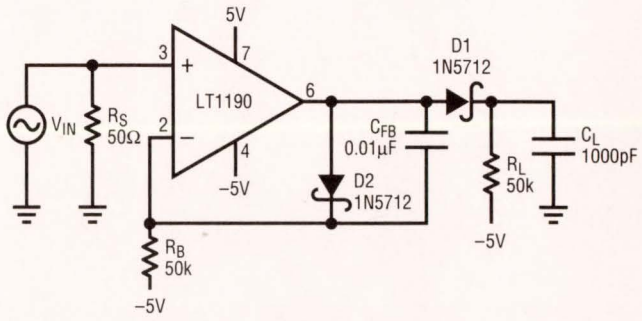

Figure 3. Open-Loop High Speed Peak Detector

racy. High values of R_L and R_B provide good low frequency accuracy, but cause the amplifier to slew rate limit, resulting in poor high frequency accuracy. A good compromise can be made by adding a feedback capacitor C_{FB} which enhances the negative slew rate on the (–) input. The DC error with a sinewave input is plotted in Figure 4 and is read with a DVM. For comparison purposes the LM118 error is plotted as well as the error of the simple Schottky detector.

Detecting Pulses

A fast pulse detector can be made with the circuit of Figure 5. A very fast input pulse will exceed the amplifier slew rate and cause a long overload recovery time. Some amount of dv/dt limiting on the input can help this overload condition, however this will delay the response. Figure 6 shows the detector error vs pulse width. Figure 7 is the response to a $4V_{P-P}$ input that is 80ns wide. The maximum output slew rate in the photo is 70V/µs. This rate is set by the 70mA current limit driving 1000pF. As a performance benchmark, the LM118 takes 1.2µs to peak detect and settle the same amplitude input. This slower response is due in part to the much lower slew rate and lower phase margin of the LM118.

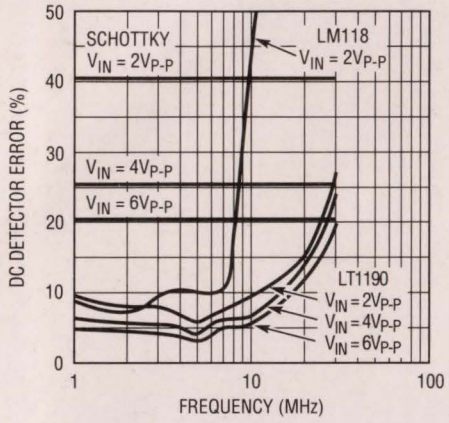

Figure 4. Open-Loop Peak Detector Error vs Frequency

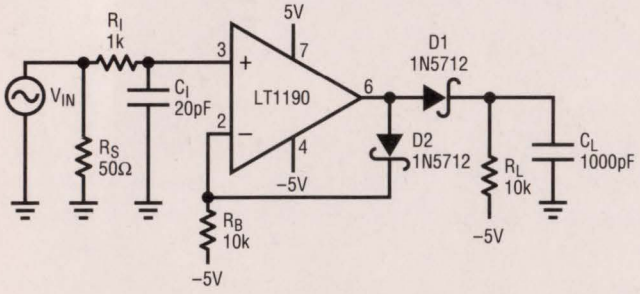

Figure 5. Fast Pulse Detector

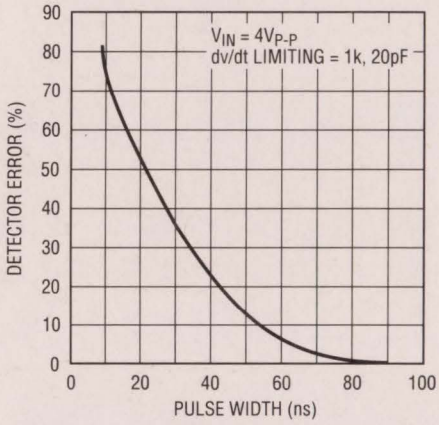

Figure 6. Detector Error vs Pulse Width

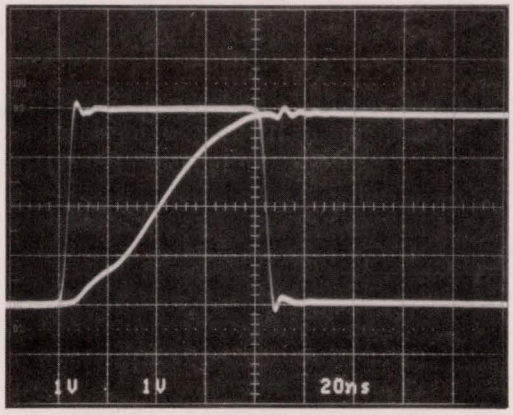

Figure 7. Open-Loop Peak Detector Response

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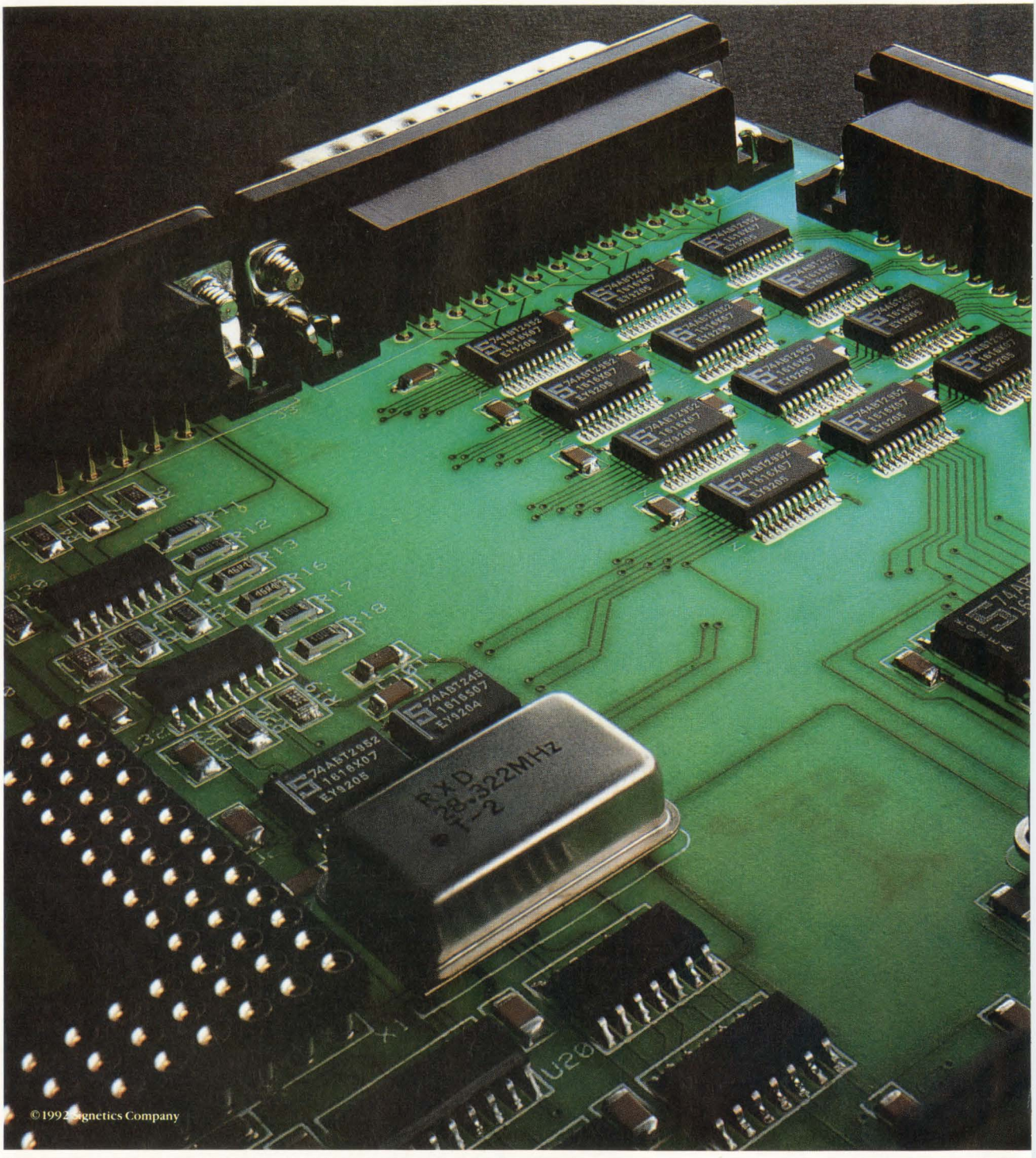

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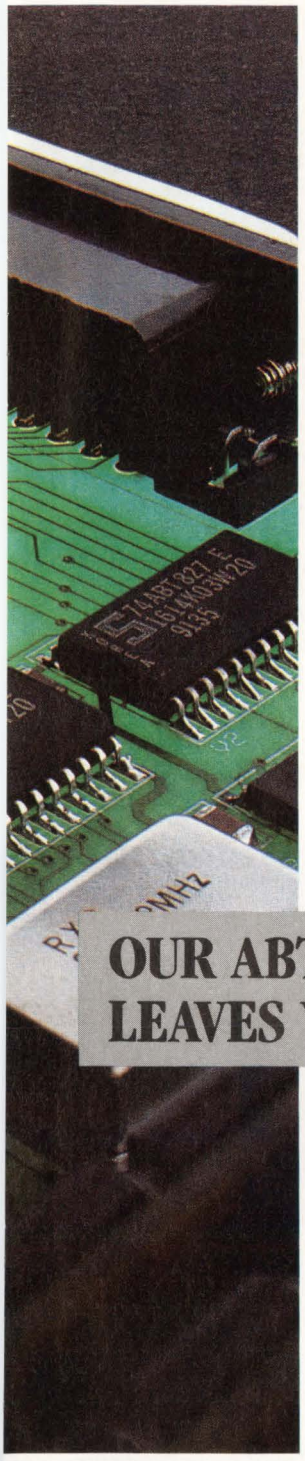

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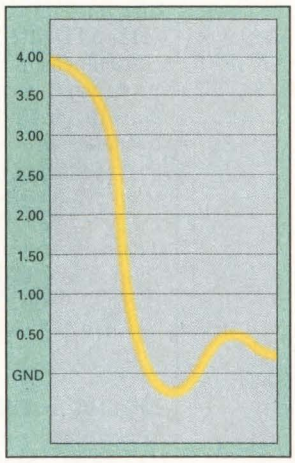

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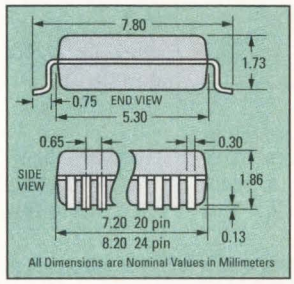

As well as offering you the significant space savings of an SSOP package, each also delivers all the performance you've come to expect from ABT.

Like the highest usable speed available. The lowest possible noise. And 64mA output drive. All of which let you design products that run faster and sell faster.

Also, thanks to our QUBiC BiCMOS process, you dissipate the lowest power. That's perfect for today's power-critical applications. Plus it simplifies thermal management.

And with more than 40 ABT products —and a contracted second source— you're always assured of the right devices at the right time.

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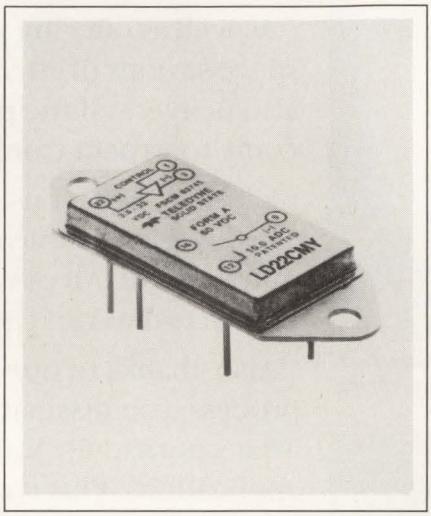
Components & Power Supplies

Redundant power supplies. MPS Series n+1 350W, 3- and 4-output, redundant power supplies feature a zero-wire power-sharing system. This paralleling technique uses a nondissipative droop regulator, which automatically shares output power and ensures glitch-free operation. Main outputs deliver 5V at 50A. The second output delivers 12V at 8A, and the third output provides 12V at 4A; the fourth output provides −5.2 or 12V at 2A, and 24V at 1.5A. $366 (100). Delivery, four to six weeks ARO. **Todd Products Corp,** 50 Emjay Blvd, Brentwood, NY 11717. Phone (516) 231-3366. FAX (516) 231-3473. **Circle No. 351**

Monolithic backplanes. The units in this family of monolithic J1/J2 backplanes meet the 80-Mbps transfer-rate requirement of VME64. Available in versions with 3 to 21 slots, the units feature an 8-layer stripline design that minimizes crosstalk and reflections. The design features onboard terminations and decoupling capacitors at every slot. Electrolytic capacitors distributed throughout the board cause the V_{CC} layers to act as virtual ground planes. $895 for a 21-slot version. **Bustronic Corp,** 44350 Grimmer Blvd, Fremont, CA 94538. Phone (510) 490-7388. FAX (510) 490-1853. **Circle No. 352**



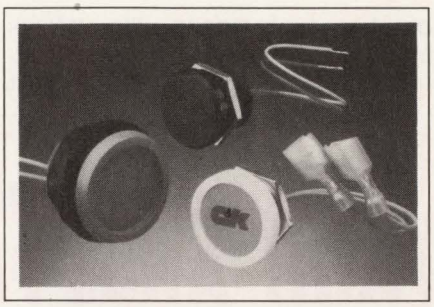
Solid-state relays. LD Series solid-state relays combine short-circuit protection with status information for military applications. The power FET output has a 10A-60V dc rating and a 75-mΩ max on-resistance. The relay suits MIL-STD-704 28V dc systems, and the control circuit is optically isolated for protection against output transients. Options include short-circuit/current-overload protection and switch status to monitor the output circuit for load power and continuity. $94 (OEM qty). Delivery, stock to eight weeks ARO. **Teledyne Solid State,** 12525 Daphne Ave, Hawthorne, CA 90250. Phone (213) 777-0077. FAX (213) 779-9161. TWX 910-321-4610. **Circle No. 353**

Crystal oscillators. VC-7000 Series voltage-controlled oscillators operate to 150 MHz. Stability equals ±25 ppm, and output drive measures 10 TTL loads or 15 pF for HCMOS. Control voltage level ranges from 0.5 to 4.5V and output rise and fall times are 10 nsec or better. Supply requirement equals 5V at 35 mA, and operating range spans 0 to 70°C. $15 (1000). Delivery, 8 to 12 weeks ARO. **Raltron Electronics Corp,** 2315 NW 107th Ave, Miami, FL 33172. Phone (305) 593-6033. FAX (305) 594-3973. **Circle No. 354**

Portable VME towers. PT Series VME towers come as a 4-slot system that measures 4×15.25×13.75 in. The system includes an integral carrying handle, a 150W power supply, a 4-slot J1-J2 backplane-card-cage combination, and a fan for system cooling. From $1150. **Hybricon Corp,** 12 Willow Rd, Ayer, MA 01432. Phone (508) 772-5422. FAX (508) 772-2963. **Circle No. 355**

Magnetic pickup. The 54Z operates over a 0- to 20,000-target/sec range. The unit uses solid-state Hall-effect technology. Voltage range equals 5 to 18V, and air-gap requirement measures 0.005 to 0.03 in. Operating range spans −40 to +105°C. A mounting clamp simplifies installation. $43. **Danaher Controls,** 1675 Delany Rd, Gurnee, IL 60031. Phone (708) 662-2666. FAX (708) 662-6633. **Circle No. 356**

Power amplifiers. Model 265 amplifiers develop ±300V at ±150A continuous and ±312A peak. The 81-kHz switching frequency provides a dc to 4-kHz full-power bandwidth and a 400-µsec current-mode settling time to 0.2% of final output. Efficiency at full load equals 94%. $15,500. Delivery, stock to six weeks ARO. **Copley Controls Corp,** 410 University Ave, Westwood, MA 02090. Phone (617) 329-8200. FAX (617) 329-4055. **Circle No. 357**

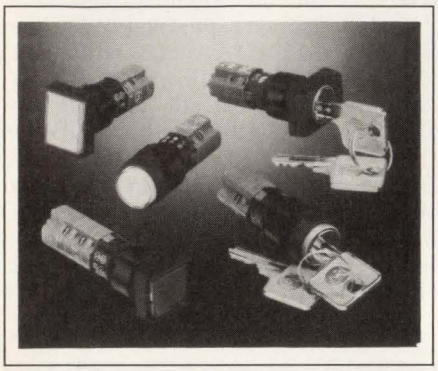


Piezo-effect switches. Based on piezo-effect principles, KP Series NO switches require no moving parts. The switching circuit and the piezo crystal are protected by a hermetically sealed housing. The switches interface with all logic circuitry and switch both ac and dc loads. Load rating equals 250 mA at 50V. A 500-mA load capability is optional. $6.75 to $12 (1000). Delivery, four to six weeks ARO. **C&K Components Inc,** 15 Riverdale Ave, Newton, MA 01258. Phone (617) 964-6400, ext 246. FAX (617) 332-2379. **Circle No. 358**

DMOS transistors. BSN10, BSN10A, and BSN20 n-channel enhancement mode transistors have maximum currents of 175, 175, and 100 mA, respectively. On and off switching times equal 2 and 5 nsec, respectively, for the BSN10 and BSN10A, and 5 and 10 nsec, respectively, for the BSN20. Power dissipation ranges to 830 mW for the BSN10 and BSN10A, and 250 mW for the BSN20. BSN10 and BSN10A, $0.13; BSN20, $0.15 (100,000). Delivery, 8 to 10 weeks ARO. **Philips Components,** 2001 W Blue Heron Blvd, Riviera Beach, FL 33404. Phone (800) 447-3762; (407) 881-3308. **Circle No. 359**

Industrial enclosures. The ZT 250 and ZT 300 are designed for 0 to 70°C operation. Both card cages come with a power supply and a low-noise STD-32 backplane. The enclosures feature a hinged

front panel that contains removable plates for I/O connectors. The 250 comes with an 80W supply and can hold 9-, 12-, or 15-slot backplanes. The 300 has a 150W supply and accommodates a 24-slot backplane. ZT 250, from $880; ZT 300, from $1300. **Ziatech Corp,** 3433 Roberto Ct, San Luis Obispo, CA 93401. Phone (805) 541-0488. FAX (805) 541-5088. **Circle No. 360**



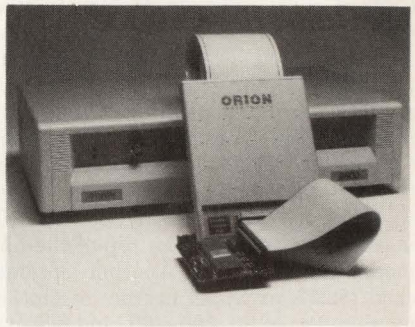
Lighted switches. Series 75 pushbutton switches come in red, yellow, green, black, or clear. Available in commercial (IP40) and industrial-grade, water-tight (IP65) versions, the units feature snap-action contacts in NO and NC configurations. Silver contacts are self-cleaning and are rated for 4A at 250V ac. Gold plating is an option. The units use standard T-4.5 telephone lamps. Engraved legends are optional. $9.25 (100). **Unimax,** Box 152, Wallingford, CT 06492. Phone (800) 624-4308; (203) 269-8701. FAX (203) 265-5398. **Circle No. 361**

Servo amplifiers. The 25A family of PWM servo dc amplifiers includes three members. Model 12A8 develops a 12A pk output from a 20 to 80V dc bus. Model 25A8 develops 25A pk from the same bus levels, and the 20A14 develops 20A pk from bus voltages of 30 to 140V dc. All units are protected against power-supply overvoltage, excessive temperature, and short circuits. Model 12A8, $275; Model 25A8, $295; Model 20A14, $335. **Advanced Motion Controls,** 3211 Corte Malpaso #407, Camarillo, CA 93012. Phone (805) 389-1935. FAX (805) 389-1165. **Circle No. 362**

Outdoor LEDs. TLYA series amber LEDs achieve luminosity levels that satisfy the needs of many outdoor applications. The four units in the line have half-viewing angles of 4° (190P), 8° (180AP), 30° (156P), and 70° (256); the units' luminosities equal 6, 2.5, 0.35, and 0.25 cd, respectively, and have lens diameters of either 10 or 5 mm. $0.90 to $1.70. **Toshiba America Electronic Components Inc,** 9775 Toledo Way, Irvine, CA 92718. Phone (714) 455-2000, or contact local sales office. **Circle No. 363**

Dual-gate MOSFET. The BF998 MOSFET combines a transfer admittance of 24 msec with a 2.1-pF input capacitance. The depletion-type tetrode works as a gain-controlled amplifier at frequencies to 1 GHz. The transistor operates from 12V, has a 1-dB noise figure at 800 MHz, dissipates 200 mW, and comes in a 4-lead SOT-143 plastic surface-mount package. $0.15 (100,000). Delivery four to six weeks ARO. **Philips Components,** 2001 W Blue Heron Blvd, Riviera Beach, FL 33404. Phone (800) 447-3762; (407) 881-3308. **Circle No. 364**

Enhanced data-acquisition-and-analysis software. V4.0 of the Asyst MS-DOS-based high-level programming language for developing scientific and engineering applications includes memory enhancements, more than 30 new commands, additional analysis tools, and counter/timer support. The language works with A/D and D/A converters and with instruments that interface to the host PC via IEEE-488 and RS-232C ports. By using expanded memory for tables and dictionaries, the new version frees more than 300 kbytes of conventional memory. Among the added analysis tools are finite-impulse-response digital filters that you can design using windowing or the Parks-McClellan algorithm. $2295; upgrades for current users, $195 to $795, depending on version upgraded. **Keithley Asyst,** 440 Myles Standish Blvd, Taunton, MA 02780. Phone (800) 348-0033; (508) 880-3000. **Circle No. 365**



Nonintrusive, ROM-based emulator for 68000 and 68302. The 8800 emulator/analyzer can connect to target systems by clipping onto surface-mount μP chips. This method of connection is unlike that of most in-circuit emulators, which plug into the target μP socket. This difference alone makes the emulator usable where other ICEs don't work. The vendor claims to have refined its ROM-based emulation technology to make it completely nonintrusive; that is, the emulators do not usurp any target resources. Moreover, the analyzer, whose bus cycle time is just 30 nsec, can include 2 Mbytes of emulation memory that has a <40-nsec cycle time under all conditions. From $9250 for 68302. **Orion Instruments Inc,** 180 Independence Dr, Menlo Park, CA 94025. Phone (800) 729-7700; (415) 327-8800. FAX (415) 327-9881. **Circle No. 366**

5½-digit DVM virtual instrument for PCs. The Model 70 is a 5½-digit ADC that resides in a small box outside your PC. You can daisy-chain as many as 32 of the units and connect them all to a single RS-232C port. For PCs that use MS-DOS, the vendor provides virtual-instrument software that lets you control the ADCs and display their readings. The software lets you increase the reading rate to 60 samples/sec by truncating the ADC word length to 4½ digits. The normal input range is ±2V. $239 with software, $199 without. **Prairie Digital Inc,** 846 17th St, Prairie du Sac, WI 53578. Phone (608) 643-8599. FAX (608) 643-6754. **Circle No. 367**

Portable spectrum analyzers. HP 8590E-series units accept test setup and measurement instructions from credit-card-size ROMs. The units store these instructions in battery-backed static RAM, which contains between 32 and 128 kbytes. Applications include tests for CT2-CAI (second-generation cordless telephone, common-air interface),

GSM (Group Speciale Mobile cellular system), EMC (electromagnetic compatibility), and several cable-TV system tests; the vendor will develop additional applications on a contract basis. Five models, which range in price from $11,500 to $26,250, collectively cover the RF and microwave frequency range to 22 GHz. An optional card ($2000) boosts the range of the top-of-the-line model to 26.5 GHz. Another optional card ($995) provides narrow-resolution bandwidths of 30, 100, 200, and 300 Hz. Delivery, eight weeks ARO. **Hewlett-Packard Co,** Box 58059, MS 51L-SJ, Santa Clara, CA 95051. Phone (800) 452-4844. **Circle No. 368**

Handheld power meter with waveform display. Like a number of other handheld instruments, the Analyst 2000-P clips onto power lines to measure ac currents; the maximum is 2 kA. The unit measures dc current, too. The device measures dc voltage (to 1 kV), ac voltage (to 750V), ac power (to 2 kW), apparent power (to 2 kVA), power factor (to 0.3 leading or lagging), frequency (5 Hz to 1 kHz), and resistance

(to 400 kΩ). AC measurements can be average, true-rms, or peak. Unlike other meters, the unit incorporates a graphics LCD that lets you view the waveform of the measured quantity. $995. **LEM USA,** 6643 W Mill Rd, Milwaukee, WI 53218. Phone (800) 236-5366; (414) 353-0711. FAX (414) 353-0733. **Circle No. 369**

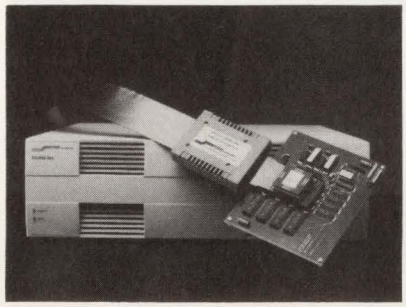
Stereo, telephone, and digital-audio interfaces. The SAIB (stereo audio/telephone interface box) is a 16-bit stereo A/D and D/A converter whose dynamic range exceeds 80 dB. It includes input antialiasing and output-smoothing filters. Software controls the gain, word size, and conversion rate (8 to 48 ksamples/sec). The digital-audio interface (DAI) is an interface to compact-disk players and digital-audio tape decks that use either the Sony/Philips Digital Interface Format (SPDIF) or Audio Engineering Society/European Broadcast Union (AES/EBU) connections. Input and output data rates are 32, 44.1, and 48 ksamples/sec. The unit handles 16- and 24-bit words. Both units connect directly to the vendor's TMS320C30-based boards for the ISA bus, SBus, and VMEbus. SAIB from $595; DAI from $795. **Sonitech International Inc,** 14 Mica Lane, Wellesley, MA 02181. Phone (617) 235-6824. FAX (617) 235-2531. **Circle No. 370**

Automated production IC programmer. The Autosite programmer eliminates adapters by providing test sites

grouped by package style. (Nine styles are supported.) The programmer also uses universal pin drivers and performs functional device testing. From $9995 (44 pins) and $14,995 (88 pins). **Data I/O Corp,** Box 97046, Redmond, WA 98073. Phone (206) 881-6444. FAX (206) 881-6856. **Circle No. 371**

VMEbus 6-channel synchro-to-resolver converters. You can specify each channel of the Model 5410-61 for synchro or resolver input; 12-, 14-, or 16-bit resolution; any frequency from 50 Hz to 10 kHz, and any one standard input voltage from 3.5 to 90V. The boards require no external supplies and have no user adjustments. A self-test feature, accessible via the bus, disconnects all inputs and applies an internally generated fixed angle. The board transmits an alert on loss of the reference or the signal. The 180°-step inputs do not cause the system to hang up. From $2400. Delivery, 8 to 10 weeks ARO. **Transmagnetics Inc,** 210 Adams Blvd, Farmingdale, NY 11735. Phone (516) 293-3100. FAX (516) 293-3793. **Circle No. 372**

AC wattmeter/rms voltmeter/rms ammeter. The 3½-digit WD-768 accepts voltage inputs to 150V and current inputs to 20A. It reads to 1999W. It can display voltage, current, or power, and it can simultaneously provide analog outputs corresponding to all three. $550. **Vector Group Inc,** 189 Horsham Rd, Horsham, PA 19044. Phone (800) 523-3696; (215) 672-6702. FAX (215) 672-3411. **Circle No. 373**



Low-cost development tools for Am29000 series. Eclipse 29K/LCD is a set of development tools for the Am29000, 29030, and 29050 RISC µPs. The tools include a source-level debugger, a compiler, an assembler, a linker/loader, and an in-circuit emulator (ICE). The ICE operates nonintrusively at speeds to 25 MHz. The tools work with several host systems, including the Sun-4. The MS-DOS version runs under MS Windows 3.x. Less than $15,000. The vendor also offers a higher performance version in which the ICE supports µP clocks as fast as 40 MHz. **Step Engineering,** Box 3166, Sunnyvale, CA 94088. Phone (800) 538-1750; (408) 733-7837. FAX (408) 773-1073. TWX 910-339-9506. **Circle No. 374**

Insulated tuning tool. The JFD-7104-8A has a molded plastic body and a plated-steel screwdriver tip. It is intended for adjusting slotted tuning mechanisms in deep cavities that have small-diameter access holes. The 5-in.-long handle is 7/16 in. in diameter. The tip measures 0.082 × 0.117 × 0.015 in. $11.20 (25). Delivery, stock to eight weeks ARO. **Sprague-Goodman Electronics Inc,** 134 Fulton Ave, Garden City Park, NY 11040. Phone (516) 746-1385. FAX (516) 746-1396. **Circle No. 375**

STD Bus DSP card. The DSP-30 is a DSP board for the STD Bus, containing a TI 33-MHz TMS320C30 chip. It operates as a slave on an STD-80 or STD 32 Bus. A development package called Debug30 lets you develop code on an MS-DOS computer and download programs, set breakpoints, run, and perform single-step operations. Other features include two 8-Mbps serial ports and a 32-bit, 1-Mbps parallel port. $2895. **Kinetic Computer Corp,** 82 Grandview Rd, Arlington, MA 02174. Phone (617) 547-2424. FAX (617) 547-7266. **Circle No. 376**

Terminal server. Available in 8- or 16-port configurations, the Micro Annex ELS connects terminals, modems, printers, and other serial devices to an Ethernet. It can access any network using TCP/IP or LAT protocols and provides full modem controls for high-speed modems on selected ports. Network management is via the Simple Network Management Protocol (SNMP). Other features include rotaries and modem pools, port password security, and macros for customizing user interfaces. The 8-port server, $1895; 16-port server, $2495. **Xylogics Inc,** 53 Third Ave, Burlington, MA 01803. Phone (617) 272-8140. FAX (617) 273-5392. **Circle No. 377**

386SX personal computer. The ME 386-SX/33 comes standard with 2 Mbytes of RAM (expandable to 16 Mbytes). The base configuration also includes a 120-Mbyte hard-disk drive, a 1.2-Mbyte, 5-¼-in.- and a 1.44-Mbyte, 3-½-in.-floppy drive, one parallel and two serial ports, a 200W power supply, a mouse, a super-VGA color-graphics card and monitor, DOS 5.0, and a choice of keyboards. $1399. **Micro Express,** 1801 Carnegie Ave, Santa Ana, CA 92705. Phone (714) 852-1400. FAX (714) 852-1225. **Circle No. 378**

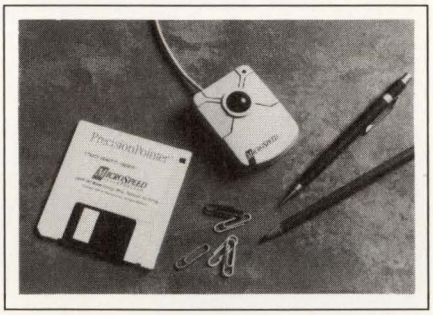
Short-haul modem. Model 420 accommodates any synchronous network configuration supporting bit rates of 32 to 128 kbps. Data streams are handled on a full-duplex basis over distances as great as 8 miles. The unit can pass a control signal end to end or use a multidrop network configuration. The device also includes a selectable RTS/CTS delay. Six LED indicators provide modem-status information. $575. **Telebyte Technology Inc,** 270 E Pulaski Rd, Greenlawn, NY 11740. Phone (516) 423-3232. FAX (516) 385-8184. **Circle No. 379**

Controllers. Personal488/IUX and 488/SCX IEE 488.2 controllers function with PCs running Interactive Unix or

SCO Unix/386, respectively. Each unit is available with either an 8-bit GP488B board that works with 330-kbyte/sec DMA, seven interrupt lines, and three DMA channels, or with a 16-bit AT488 board that works with 1-Mbyte/sec DMA, 11 interrupt lines, and six DMA channels. The software drivers on both controllers offer familiar bus commands. The 8- and 16-bit units, $595 and $695, respectively. **IOtech Inc,** 25971 Cannon Rd, Cleveland, OH 44146. Phone (216) 439-4091. FAX (216) 439-4093. **Circle No. 380**

Development platform. The DSP-1 revision C development platform for the SBus provides standard-bus interface logic, a high-speed DMA controller, and a basic software package. The unit includes the hardware interface, driver software, firmware PROM, prototyping boards, connectors, brackets, and jumpers. A user guide includes source code and schematics. The software comes on a disk. $1095. **Dawn VME Products Inc,** 47073 Warm Springs Blvd, Fremont, CA 94539. Phone (510) 657-4444. FAX (510) 657-3274. **Circle No. 381**

Print server. The Five Printer is an entry-level version of Print Server. It offers a variety of network-management facilities including font, job, printer, and forms management, as well as print resource accounting. The unit reduces the system-administrator's workload and allows management to track network printing usage. $495. **Insight Development Corp,** 2200 Powell St, Suite 500, Emeryville, CA 94608. Phone (510) 652-4115. **Circle No. 382**



Trackball. The Microtrac stand-alone trackball connects to a serial or PS/2 mouse port. Measuring only 2.8×2 in., the unit offers 400-dpi resolution and comes in versions that are compatible with the Microsoft mouse, the PS/2 mouse, and Microsoft Windows. The trackball works in combination with the CQ19M, a trackball module that occupies the same space as the cursor keys. Microtrac, $29; CQ19M, $18 (1000). **Microspeed Inc,** 44000 Old Warm Springs Blvd, Fremont, CA 94538. Phone (510) 490-1403. FAX (510) 490-1665. **Circle No. 383**

Communications adapters. The MPA 100/200/300 adapter cards are capable of synchronous data communications in bit-synchronous SDLC/HDLC modes, as well as byte synchronous in monosync and IBM bisync modes. All are standard with the Intel 82530 and are compatible with the Zilog 85230 and 8530 Serial Communications Controller (SCC) ICs. Onboard hardware allows the units to meet all SCC access-timing requirements, allowing host software to run correctly, independent of the host-computer clock speed. $365. **Quatech Inc,** 662 Wolf Ledges Pkwy, Akron, OH 44311. Phone (216) 434-3154. FAX (216) 434-1409. **Circle No. 384**

Touchscreen monitor. This Touchmonitor consists of a Mitsubishi 3925 19-in. monitor and a touchscreen that employs resistive technology. The monitor has resolutions to 1024×768 pixels, is UL listed, FCC Class A approved, and has CSA approval pending. The unit will accommodate mouse-emulation software for MS-DOS, Microsoft Windows, OS/2, Apple Macintosh, and other operating systems. $2935. **Elographics Inc,** 105 Randolph Rd, Oak Ridge, TN 37830. Phone (615) 482-4100. FAX (615) 482-4943. **Circle No. 385**

S/D converter. STB/SDC Series single-slot STB-bus converters accept any synchro- or resolver-input voltage from 50 Hz to 5 kHz and convert it to 10, 12, 14, or 16 bits of binary data. The binary data is addressable in a 2-byte format over the backplane. Power requirements are ±15 and 5V, and operating range spans 0 to 70°C or −55 to +105°C. $995 (OEM qty). **Computer Conversions Corp,** 6 Dunton Ct, East Northport, NY 11731. Phone (516) 261-3300. FAX (516) 261-3308. **Circle No. 386**

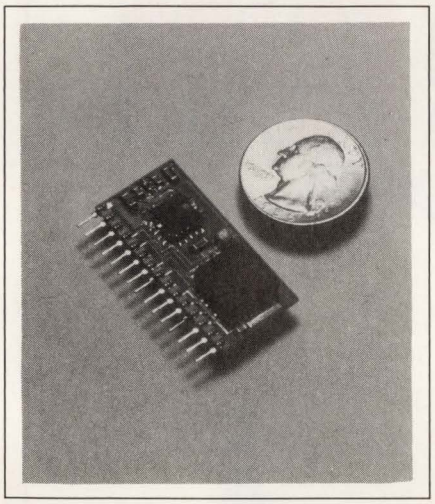
Transceiver. The AT-210TS 10Base-T microtransceiver measures 2.8×1.7×0.9 in. The unit features a switch-selectable SQE/Heartbeat test with an LED indicator, polarity detection and correction with an LED indicator, a link-integrity test function with an LED indicator, and a fourth LED indicator for power. The unit carries a 2-year warranty. $59.95. **Allied Telesis Inc,** 575 E Middlefield Rd, Mountain View, CA 94043. Phone (415) 964-2994, ext 122. **Circle No. 387**

Color interface. The Precisioncolor 24Xp is a color graphics interface for the Macintosh II and Quadra families. A NuBus-based design, it has 24-bit color and incorporates onboard Quickdraw acceleration, support for an array of displays, a resolution of 832×624 bits, and on-the-fly resolution switching. The device is specifically designed for 16-in. displays. $599. **Radius Inc,** 1710 Fortune Dr, San Jose, CA 95131. Phone (408) 434-1010. **Circle No. 388**

Computer module. Despite its 1.7×5.2-in. size, the ESP 8680 module handles a range of computing functions. The module has a fully integrated 8086XT with a nonvolatile-memory-card (PCMCIA) socket, CGA graphics, 1-Mbit-max dynamic RAM, a keyboard interface, one serial port, and connectors for expansion. $995. **Dover Electronics Manufacturing West,** Box 1532, Longmont, CO 80502. Phone (303) 772-5933. **Circle No. 389**

Color printer. The HP Paintjet XL300 uses four 50-color print cartridges to create virtually any color. The unit prints on a variety of media—including plain paper. The unit prints color graphics at approximately 1.5 to 6 minutes per page and prints monochrome text at 1 to 2 minutes per page. The printer comes standard with 2 Mbytes of memory. The printer comes standard with a 200-sheet input tray that can handle letter- and legal-size paper and letter-size transparencies. From $3495. **Hewlett-Packard Co,** Box 58059, MS511L-SJ, Santa Clara, CA 95051. Phone (800) 752-0900. **Circle No. 390**

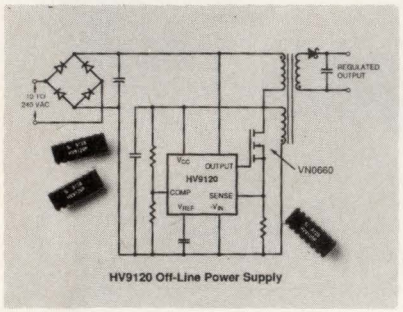
Graphics chip set. The 68800 chip set is a second-generation graphics controller that employs features found on the company's Ultra and VGAwonder boards. It drives 1280×1024-pixel noninterlaced displays and has as much as 4 Mbytes of video RAM. The chip set is compatible with the 16- and 32-bit Micro Channel Architecture bus, EISA, ISA, and Local Bus architectures. The controller displays 16.7 million colors and supports the 8514/A, Super VGA, and VGA standards. $79 (1000). **ATI Technologies Inc,** 3761 Victoria Park Ave, Scarborough, ON M1W 3S2, Canada. Phone (416) 756-0718. FAX (416) 756-0720. TLX 06966640. **Circle No. 391**



Digital frequency synthesizer. The STEL-1479 is a complete direct digital frequency synthesizer in a single in-line package measuring 1.3×0.8×0.35 in. The thick-film hybrid unit employs the company's STEL-1179 modulated numerically controlled oscillator chip driving an 8-bit DAC. The device operates at clock frequencies as fast as 25 MHz, producing an output frequency range to 10 MHz and having a resolution of 1.49 Hz. You can modulate the carrier using 8-PSK (phase-shift keying), binary PSK, or quadrature PSK modulation. $20 (1000). **Stanford Telecommunications Inc,** 2421 Mission College Blvd, San Jose, CA 95056. Phone (408) 980-5684. FAX (408) 727-1482. **Circle No. 392**

Cellular-telephone ICs. Four lines of IC products receive and transmit voice and data signals for cellular phones. Different models in the five FM-amplifier line contain an FM demodulator, receive-signal strength indicator, second mixer, and gain-adjustable IF amplifier. Two modem ICs provide modula-

tion and demodulation, a DTMF generator, and switched-capacitor filters. A frequency synthesizer operates to 1 GHz. Two mixers have typical noise figures of 1.2 dB, and two RF amplifiers have noise figures of 1.6 dB. $0.60 to $10. **Sony Corp of America,** Box 6016, Cypress, CA 90630. Phone (800) 288-7669. FAX (714) 229-4333. **Circle No. 393**



HV9120 Off-Line Power Supply

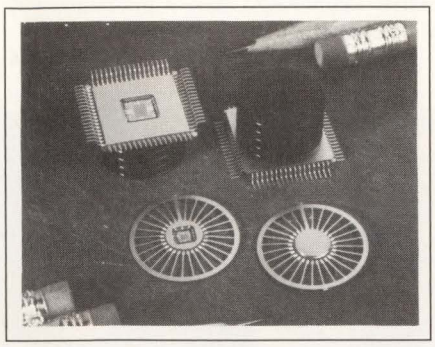
High-voltage PWM ICs. A family of high-voltage BiCMOS PWM ICs lets you build 1 to 150W switch-mode power supplies. DMOS circuitry permits high-voltage start-up. The HV9120 operates from voltages as high as 450V dc, and the HV9110/9111 operate from 120V dc max. The units also operate from 9.4V dc. Fast CMOS circuitry permits 1-MHz clock speeds. Plastic DIP versions, from $1.85 to $2.75 (1000). **Supertex Inc,** 1350 Bordeaux Dr, Sunnyvale, CA 94089. Phone (408) 744-0100. FAX (408) 734-5247. **Circle No. 394**

Fast static RAMs. A family of BiCMOS 1-Mbit fast static RAMs have 10-, 12-, and 15-nsec access times. Two members, the MCM101510 and MCM101514, have ECL-compatible I/O ports and come in 1M × 1-bit and 256k × 4-bit configurations. Two other members, MCM6727 and MCM6726, have TTL-compatible I/O ports and come in 1M × 1-bit and 128k × 8-bit configurations. Three members, the MCM67282, MCM6728, and MCM6729, have TTL-compatible I/O ports and come in 256k × 4-bit configurations. The 10-nsec version, $175; 12-nsec version, $160; 15-nsec version, $85 (500). **Motorola,** Box 52073, M/D 56-102, Phoenix, AZ 85072. Phone (512) 928-7726. **Circle No. 395**

Serial-communications controller. The Z16C32 is a second-generation universal serial-communications controller. The chip's 20-Mbps data-transfer rate doubles the rate of the company's previous Z16C31 chip. A status-control handling feature writes frame status and length data into array tables in link-list DMA mode. Because the chip doesn't need to find the end of frame to locate stored data, there is no need for large onboard status FIFO buffers. You can scatter and gather frames in a 32-bit address range. PLCC 16-Mbps version, $7; 20-Mbps version, $8.50 (1000). **Zilog Inc,** 210 E Hacienda Ave, Campbell, CA 95008. Phone (408) 370-8000. FAX (408) 370-8056. **Circle No. 396**

CMOS gate arrays. The MSM91S000 family of 0.8-µm CMOS gate arrays comes in 35 sizes having as many as 225,000 gates. The sea-of-gates architecture operates from 2.7 to 5.5V. Versions have as many as 840 configurable I/O cells. You can construct random logic using soft macrofunctions that can be merged with memory and hard macrocells. A clock-tree macrocell guarantees that clock skew is less than 1 nsec for more than 2000 fanouts operating

at 70 MHz. Memory macrocells include a 64-kbit static RAM and a 256-kbit ROM. NRE prices, from $53,600; each gate, $0.07 (50,000). Delivery, five to seven weeks ARO. **Oki Semiconductor,** 785 N Mary Ave, Sunnyvale, CA 94086. Phone (800) 654-6388; (408) 720-1900. FAX (408) 720-1918. **Circle No. 397**

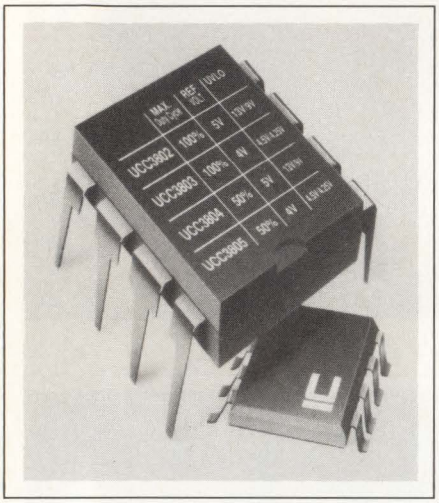


High-frequency ECL ASICs. The E500H and E128VH are ECL ASICs that operate at 3- and 5-Gbps data rates, respectively. The E500H has 504 gates having internal gate speeds of 60 psec and 0.35-mA emitter current. The E128VH has 128 gates having internal gate speeds of 40 psec and 1-mA emitter current. The ASICs employ a 0.3-μm Si-Bipolar process. E500H, $175; E128VH, $140. **Fujitsu Microelectronics Inc,** 3545 N First St, San Jose, CA 95134. Phone (800) 642-7616; (408) 922-9000. FAX (408) 432-9044. **Circle No. 398**

Disk controller. The SX1615 24-Mbps disk-controller chip features internal ECC generation, a 32-bit DMA channel, and DMA transfer rates as high as 50 Mbps. The chip is designed for IPI-2 disk-control service. $172 (1000). **Simulex Corp,** 2832-C Walnut Ave, Tustin, CA 92680. Phone (714) 730-1500. **Circle No. 399**

Mixer-IF FM circuits. The NE/SA625 and SA627 FM circuits have an on-chip mixer/oscillator that accommodates RF and IF signals as fast as 500 MHz and 25 MHz, respectively. Sensitivity is 0.22 μV for an RF input at 45 MHz. The NE/SA624 contains two limiting IF amplifiers, a quadrature detector, and a 90-dB logarithmic received-signal strength indicator (RSSI). The RSSI has rise and fall times of 0.9 and 1.4 μsec for an input-frequency signal at 10.7 MHz. NE624N, $2.84; NE625/7N, $3.55 (100). **Signetics Co,** Box 3409, Sunnyvale, CA 94088. Phone (408) 991-4520. **Circle No. 400**

Cache RAMs. These cache RAMs are available in 16k-word × 10-bit × 2-way (μPD46710) and 8k-word × 20-bit × 2-way (μPD46741) configurations. The units come in 12- and 15-nsec versions and maintain 40- and 33-MHz R3000-based systems. Both the instruction- and data-cache core include on-chip address and chip-enable latches, on-chip instruction and data cache, and 10 I/Os. The 15- and 12-nsec versions, $33 and $65 (10,000), respectively. **NEC Electronics Inc,** 401 Ellis St, Mountain View, CA 94039. Phone (415) 960-6000. FAX (415) 965-6130. **Circle No. 401**



PWM current-mode controllers. The UCC380x family of BiCMOS PWM, current-mode controller ICs features a current-sensing to gate-drive delay of 70 nsec typ. The family contains the circuitry to implement dc-to-dc switching power supplies using a few external components. Typical operating current is 500 μA, and the start-up current is less than 100 μA. The units operate as fast as 1 MHz and deliver 1A output current. Commercial version, $2.08 (1000). **Unitrode Integrated Circuits Corp,** Box 399, Merrimack, NH 03054. Phone (603) 424-2410. FAX (603) 424-3460. **Circle No. 402**

ASIC family. The LCA300K compacted-array series of 0.6-μm ASICs offers as many as 600,000 gates and more than 800 I/O pins. They consist of 14 master slices ranging from 10,000 to 500,000 usable gates. The LCB300K cell-based ASICs implement as many as 200,000 gates, a 512-kbit RAM, and a 1-Mbit ROM on a single chip. The LEA300K embedded-array ASICs embed the LCB300K cell-based memory and complex logic functions in the chip's core to provide fast turnaround. NRE charges, from $30,000. **LSI Logic Corp,** M/S D102, 1551 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 433-7871; (408) 433-7146. **Circle No. 403**

Communications chip set. The HDMP-1000 Gigabit-Link (G-Link) chip set and transmitter and receiver chips provide serial data communications as fast as 1.5 Gbps. The bipolar transmitter and receiver transfer data through a single fiber-optic cable for distances as long as 10 km. The chip set incorporates the circuitry to encode and multiplex parallel input data for serial data rates from 100 to 1500 Mbps. The chip set also decodes and demultiplexes received data. Chip set, $710; transmitter, $355; receiver, $355 (1 to 9). **Hewlett-Packard,** 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900. **Circle No. 404**

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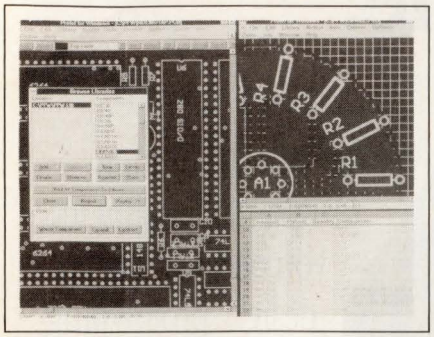


Updated pc-board-design software. Protel for Windows pc-board-design system version 1.1 works with MS-Windows 3.0 or 3.1 and autoplaces component footprints with netlists from other capture packages. It reads PADS-PCB and Tango-PCB files; provides pen plotting down to 0.0025 mm wide; and has a 300-pattern footprint library. The system's binary file size has been reduced an average of 60%. Other features include an arc resolution of 0.001° and placement to a resolution of 0.001 mil. Version 1.1 update supplied at no charge to previous version owners. $3480 for new users. **Protel Technology Inc,** 151 Bernal Rd, San Jose, CA 95119. Phone (800) 544-4186; (408) 281-5858. FAX (408) 225-1863. **Circle No. 405**

Thermal analysis for PC boards. Thermax Designer has a forms-driven user interface and a thermal library of 15,000 components and 700 packages. It requires minimal user knowledge of thermal analysis and operates automatically. As a board layout or circuit designer, you use this product to satisfy thermal constraints during physical design. Heat-transfer specialists use a related product, Thermax Expert, to precisely model all heat-transfer mechanisms for ICs, multichip models, and pc boards. Thermax Designer, $21,000. **Cadence Design Systems Inc,** 555 River Oaks Pkwy, San Jose, CA 95134. Phone (408) 943-1234. FAX (408) 943-0513. **Circle No. 406**

Ada-language system and tool set. The Sun Ada Development Environment version 1.1 enhances user applications by as much as 30 percent over previous versions, according to benchmarks from the Performance Issues Working Group of IEEE SIGAda. In addition, the product is compatible with the Vadscross family of cross-development products from Verdix Corp, giving a common tool set and user interface for both host- and target-system development. The product also comes with network licensing. It includes a compiler, debugger, on-line language reference manual, an X11 tool kit, and an interactive build-and-test tool kit for GUIs. US single-use license, $10,000. **Sunpro Inc,** 2550 Garcia Ave, Mountain View, CA 94043. Phone (415) 960-1300. FAX (415) 969-9131. **Circle No. 407**

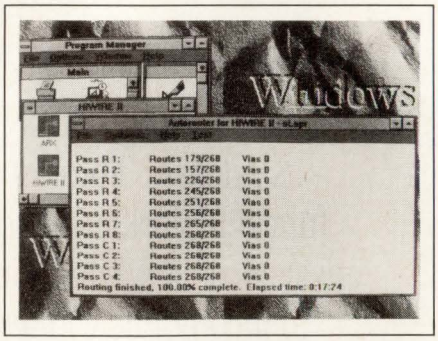
Block-oriented network simulator. Bones Designer 2.0 simulates networks and networking devices including protocols, LANs, WANs, circuit- and packet-switched networks, Integrated Services Digital Network, Switched Multimegabit Data Service, packet radio networks, computer buses and architectures, and satellite-based systems. You use a library of 300 primitives as building blocks for creating modules and models. The user interface is a graphical user interface with mouse-based selection and copy-and-paste functions for building new modules from previously defined blocks. An animation mode displays the flow of data through the model, and you can place probes anywhere to collect data that documents network performance. Available on Sun-4 SPARCstations, DECstations, and HP9000/700 workstations, $12,000. **Comdisco Systems Inc,** 919 E Hillsdale Blvd, Foster City, CA 94404. Phone (415) 574-5800. FAX (415) 358-3601. **Circle No. 408**

Spice simulator. The Analog Interface Kit provides users of proprietary Spice simulators and third-party Spice vendors with an interactive, graphical front end for Spice and Spice-like simulators. It also provides a link to the Design Architect schematic-capture tool, the Simview simulation user interface, and the Falcon framework for concurrent design. The software includes a suite of postprocessing and analysis tools for viewing results of analog simulations interactively or in real time. For Sun and HP workstations, from $13,900. **Mentor Graphics Corp,** 8005 SW Boeckman Rd, Wilsonville, OR 97070. Phone (408) 436-1500. **Circle No. 409**

Top-down ASIC design tool. The ASIC Navigator design system performs behavioral VHDL (VHSIC Hardware Description Language) simulation, design partitioning, and logic and test synthesis. You can use any combination of graphical- and HDL-based specifications to create single- or multichip ASIC systems. Also available with the software are eight ASIC and FPGA libraries that work with all logic-design tools in the design system. Libraries are available from Fujitsu, LSI Logic, Motorola, NCR, SMOS Systems, Toshiba-Siemens, VLSI Technology, and Xilinx. $95,000. **Compass Design Automation,** 1865 Lundy Ave, San Jose, CA 95131. Phone (408) 433-4880. FAX (408) 434-7820. **Circle No. 410**

Virtual instrument library. Using the Anaview virtual instrument library for Labview 2, you can control, monitor, and configure Anafaze 8LS and 12LS PID (proportional integral derivative) loop controllers. The controllers regulate temperature, pressure, and other process variables using PID algorithms. $795. **Software Engineering Group,** 1 Dana St, Cambridge, MA 02138. Phone (617) 492-6664. FAX (617) 661-6483. **Circle No. 411**

R&M software for workstations. SoftPC, a DOS emulator, lets you run the manufacturer's reliability and maintainability software on workstations. SoftPC emulates DOS 3.3 and PC/AT performance. $695. **Powertronic Systems Inc,** Box 29109, New Orleans, LA 70189. Phone (504) 254-0383. FAX (504) 254-0393. **Circle No. 412**



Extended-memory autorouter for PC. The ARX autorouter for Hiwire II pc design software can use as much as 15 Mbytes of extended memory under MS-Windows 3.0. The software, which runs in native 286 or 386 modes, can autoroute boards at least 10 times larger than the maker's standard autorouter. The product is a multipass, 100% completion, gridless router featuring rip-up-and-reroute capability, through minimization and flexible design rules. $1695. **Wintek Corp,** 1801 South St, Lafayette, IN 47904. Phone (800) 742-6809. FAX (317) 448-4823. **Circle No. 413**

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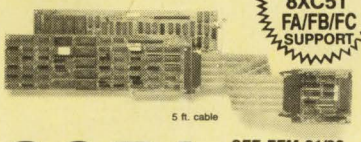

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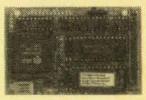

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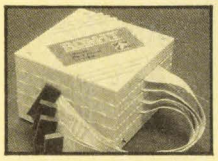

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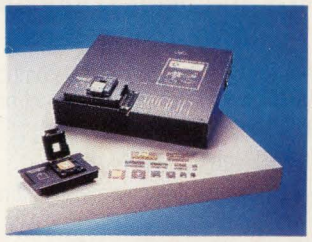

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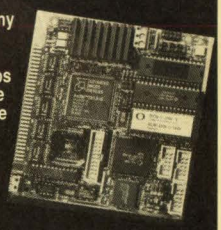

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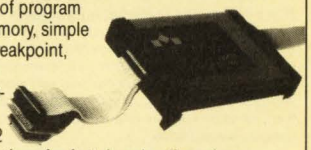

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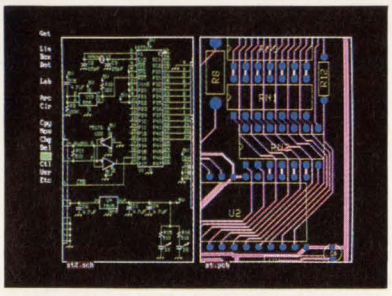

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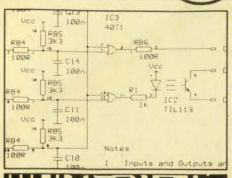

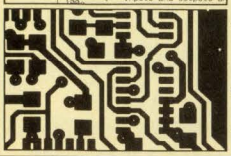

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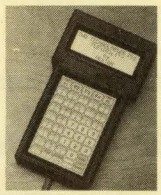

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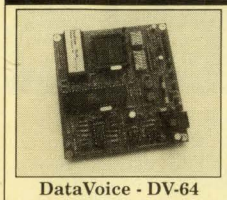

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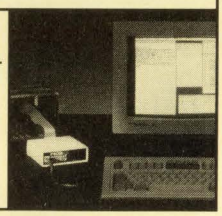

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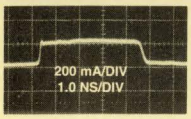

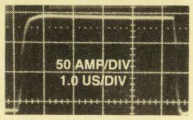

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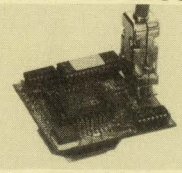

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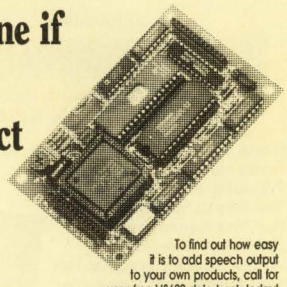

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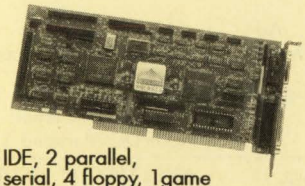

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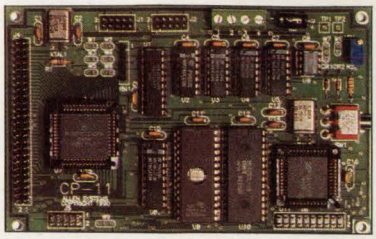

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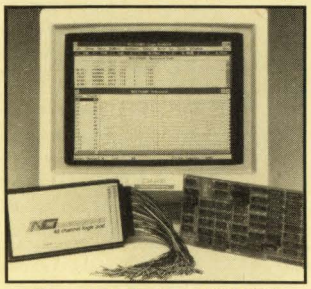

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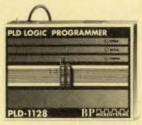

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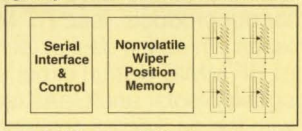

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Magazine Edition	Sept. 3	Aug. 13	ASICs SPECIAL ISSUE CAE Tools & Techniques Computer Peripherals • Computer Buses • Sensors & Transducers • Buscon Show Coverage
News Edition	Sept. 10	Aug. 27	CAE • Test & Measurement Diversity Special Series
Magazine Edition	Sept. 17	Aug. 27	Field-Programmable Gate Arrays DSP Directory • Embedded Computers • CAE
SOFTWARE ISSUE	Sept. 17	Aug. 27	SOFTWARE ENGINEERING SPECIAL ISSUE (To be polybagged with the Sept. 17th Magazine Edition issue)
News Edition	Sept. 24	Sept. 10	Automotive Electronics Sensors • Computers & Peripherals • Regional Profile: Oregon, Washington
Magazine Edition	Oct. 1	Sept. 10	TEST & MEASUREMENT SPECIAL ISSUE • European Technology Update • Data Acquisition Software • Superconductors • How to Design it Right the 1st Time Series—Part I PLD/FPGA Directory
News Edition	Oct. 8	Sept. 24	CAE • PC/Workstation Design • Engineering Management Special Series
Magazine Edition	Oct. 15	Sept. 24	Disk Drives • Portable-Computer Design • Switching Power Supplies • Design it Right Series—Part II
News Edition	Oct. 22	Oct. 8	Data Storage Technology Communications Technology Regional Profile: Michigan, Illinois, Missouri
Magazine Edition	Oct. 29	Oct. 8	ELECTRONICA SHOW ISSUE • Object-oriented Programming • Chipsets for PCs Design it Right Series—Part III Wescon Preview Issue
News Edition	Nov. 5	Oct. 22	COMDEX/WESCON SPECIAL ISSUE • Special Supplement: Design for Portability • Microprocessors • Wescon/Comdex Hot Products • CAE Software • Diversity Special Series
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- C programming on a UNIX platform
- Intel 5081 and Motorola 68XXX processors

LINE CARD DESIGNERS
- Analog and digital
- Voice and data transmission
- Microprocessor control
- High speed backplanes
- X.25, LAN

ASIC DESIGNERS
- HDL design
- Valid running on Sun Workstations
- SONET, ADM, TSI
- EPLD, ASIC, FPOA
- ISDN, T1

COMMON CONTROL DESIGNERS
- ASIC or FPOA
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- Motorola 68XXX microprocessors

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SOFTWARE
- ADA, C
- 1750A, of 68020 Microprocessors
- VAX VMS, Sun UNIX
- Real-time, Embedded Microprocessor
- DOD-STD-2167A, CASE Tool

DIGITAL HARDWARE
- ACTEL FPGAs
- Microprocessor based systems
- 1553 bus interface

DIGITAL SIGNAL PROCESSING
- Discrete Fourier Transforms
- Control Loops
- PSK Demodulation

EMBEDDED CRYPTO
- Security Fault Analysis
- TEMPEST, Red/Black Isolation
- Related interface hardware

RF and MICROWAVE
- Synthesizer Design, Direct Digital
- Power amp and filter design
- MMIC design

ANTENNA DESIGN
- Parabolic Antenna Design
- Gimbal, Positioner
- 10 TO 60 GHz

SYSTEMS
- BSEE/MSEE, minimum 4 years' experience
- Strong communication background
- Requirements Analysis, Functional Analysis
- System Synthesis, System Analysis
- RF Link Budget Analysis
- System Integration/Test
- Customer Interface

Background: Hardware, Software Architecture Cryptographic; BIT/BITE; Antenna Pointing, Tracking, and Platform Stabilization; MIL-STD-1582; SI-1135, SI-2035, LL1005.

MILSTAR or other military satellite design experience a plus.

E-Systems offers very competitive salaries and an excellent benefits package which includes an Employee Stock Ownership Plan, 401(k), and major medical and dental insurance. Qualified candidates should forward a resume and salary history to: Manager of Staffing, E-Systems, Inc., ECI Division, Post Office Box 12248, St. Petersburg, Florida 33733-2248.

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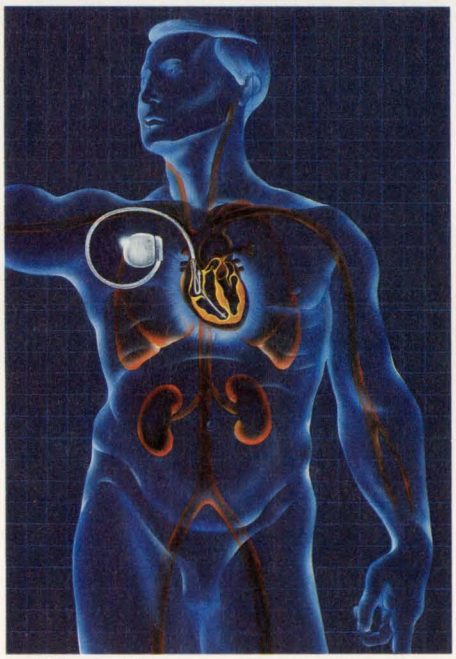
The field of cardiac device therapy has come so far so fast, there's no telling where technology will take us in twenty years. If you need incredible challenges in a high-tech environment and the opportunity to do work that literally saves and changes lives, you'll find your opportunity to make a difference at Siemens Pacesetter, Inc. Future opportunities include:



AUTOMATIC TEST ENGINEER
To perform analog and digital circuit design, SW development and test system integration. Requires BSEE and 3+ years ATE experience in the design/development of computer-based automatic production test equipment. **Respond to Dept. EDN/ATE.**

IC LAYOUT DESIGNER
Utilizing Sun SPARC workstations, will layout CMOS analog/digital circuits with standard cell and fully customized methodologies. Requires 2+ years layout experience and working knowledge of UNIX. **Respond to Dept. EDN/ICDE.**

PROCESS ENGINEER
Will handle machine design projects utilizing electro-pneumatic mechanisms/processes involving YAG laser welding. Requires BSME/EE with 5 years experience in CNC machine control, diagnostics, mechanical fixture design and repair of digital/analog circuits. **Respond to Dept. EDN/PE.**

SR. PROCESS ENGINEER
Will develop/implement new processes, equipment, components and manufacturing methods to support hybrid test and manufacturing. Emphasis will be on improving manufacturing yields, designing SPC systems and conducting hybrid material R&D. Requires BSEE/ME; 5 years hybrid experience preferred. **Respond to Dept. EDN/SPE.**

SOFTWARE QUALITY ENGINEER
Will develop/implement software test designs for validation/verification of product and manufacturing. Requires experience in software development for microprocessor-based products and software test design procedures. A BSCS or equivalent is desirable. **Respond to Dept. EDN/SQE.**

SR. COMPONENT RELIABILITY ENGINEER
Requires BSEE with 5 years experience in reliability engineering, failure analysis techniques and rate predictions. Knowledge of IC and hybrid design/evaluation/qualification techniques and CMOS is essential. **Respond to Dept. EDN/CRE.**

SR. ANALOG ELECTRONICS DESIGN ENGINEER
Duties include designing low power CMOS op amps and switched capacitor circuits and overseeing layout. Will also perform some system design, integration and scheduling. Requires BS/MS in Electronics, 10+ years analog design experience and 5+ years IC design experience. Thorough knowledge of SPICE and FET models a must. **Respond to Dept. EDN/AEDE.**

SR. ELECTRONIC PRODUCT ENGINEER
BSEE and 3-5 years experience in analog/digital design, CMOS/TTL devices and microprocessor-based systems essential. Ideal candidate will have knowledge of hybrid microelectronics involved in the manufacture of high-reliability electronic devices. **Respond to Dept. EDN/EPE.**

SOFTWARE ENGINEER
Utilizing Assembly and C languages, will design/develop system and application SW for real-time embedded microprocessor-based device support products. Requires BSEE/CE or equivalent and 3+ years experience in embedded microprocessor and system-level SW design/development. **Respond to Dept. EDN/SE.**

In addition to our desirable Southern California location, we offer competitive compensation, paid relocation and an excellent benefits package, including employer-contributed pension plan, 401(k), tuition reimbursement, vision care and a choice of dental/health plans. Send resume (NO PHONE CALLS, PLEASE!) to the appropriate department: **Greer A. Brooks, Employment Representative, Siemens Pacesetter, Inc., 15900 Valley View Court, P.O. Box 9221, Sylmar, CA 91392-9221.** AA/EOE

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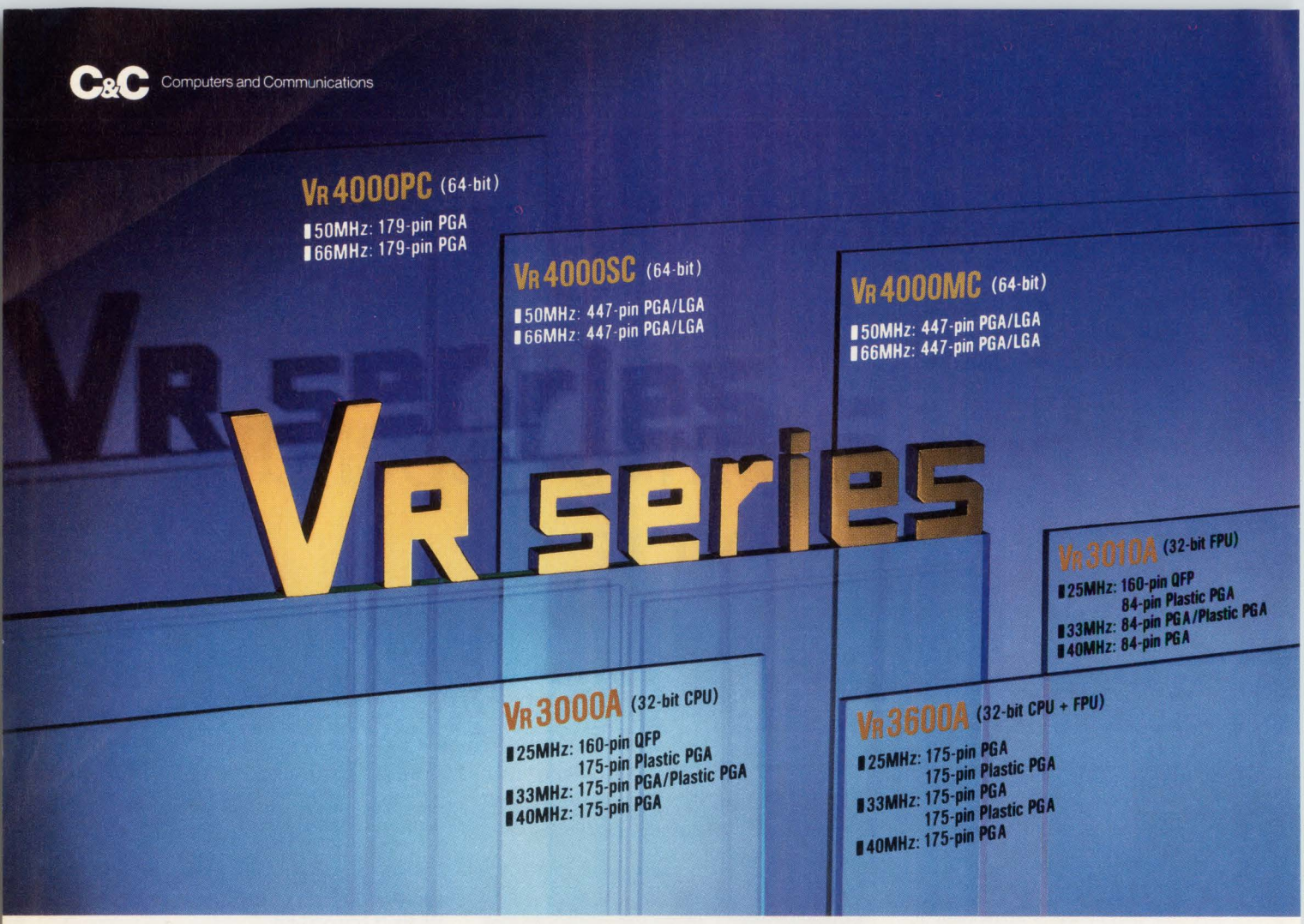

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NEC's 64-bit RISC family offers excellent price/performance and future upgrade paths. VR4000PC gives you a completely integrated set of functions for 64-bit computing. The floating point unit, as well as 8K-byte instruction cache, and 8K-byte data cache are all included on chip. VR4000SC also supports a large secondary cache of up to 4M bytes. VR4000MC features a multiprocessor interface for parallel processing.

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We offer three device types for 32-bit RISC computing: VR3000A CPU, VR3010A FPU, and VR3600A which integrates both CPU and FPU on a single chip. For cost-sensitive applications, try our plastic PGA and QFP versions.

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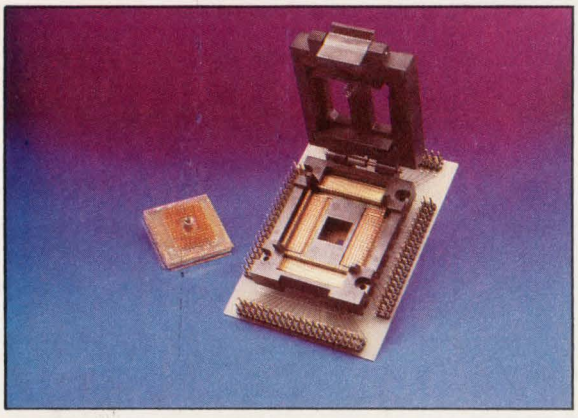
CIRCLE NO. 86

TEST QUAD FLATPACK



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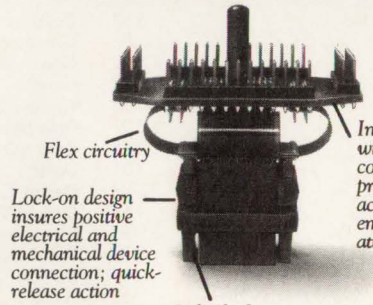
CIRCLE NO. 87

Test Fine-Pitch Devices to 208 Pins



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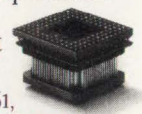
Pomona's new FIN™ (Flexible Interface Network) QFP test clips give you direct access to today's newest 100-, 132- and 196-pin JEDEC devices. Set-up time is drastically reduced, and you can rely on repeatable contact with every pin, every time. And, you can choose among three styles in each pin count to suit your interface needs.

Of course, you'll be able to select from Pomona's complete family of SMD and IC test accessories including IC clip kits and PGA adapters. You can also choose from 18 EIAJ QFP test adapter models.



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CIRCLE NO. 88

Why didn't I think of that?

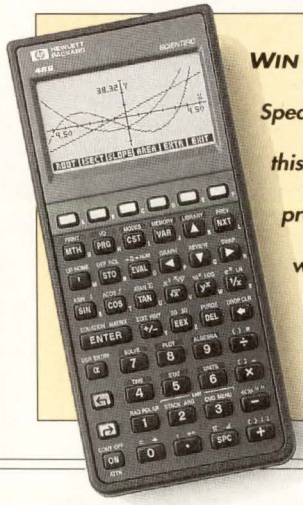
That's what you'll say when you read the details about the Innovation and Innovator of the Year finalists and their products in EDN's Special August 20th Innovation Ballot Supplement.

Each innovation finalist will be the subject of a short feature article that will provide you with interesting information on what's new in the world of electronics. You'll read about innovative products that exhibit high levels of performance and innovative people who display technical leadership in the electronics industry. You'll learn about products that solve problems more effectively, and products or new technologies that allow engineers to design better products at a signification reduction in cost. Most of all, you'll notice that the people behind the nominated products are engineering professionals like you.

Each and every finalist's product is the cream of the crop. But, only a select few will be voted the Grand Winner of EDN's 1992 Innovation/Innovator of the Year in each category. It's up to you to decide which of these products is the most innovative. The best of the best.

So . . . keep your eyes open for the August Innovation Ballot Supplement which will be mailed to you with your August 20th issue. Your peers are counting on you to make the final judgement on their product and their innovative skills. Be sure to cast your vote on the ballot that's inside the supplement.

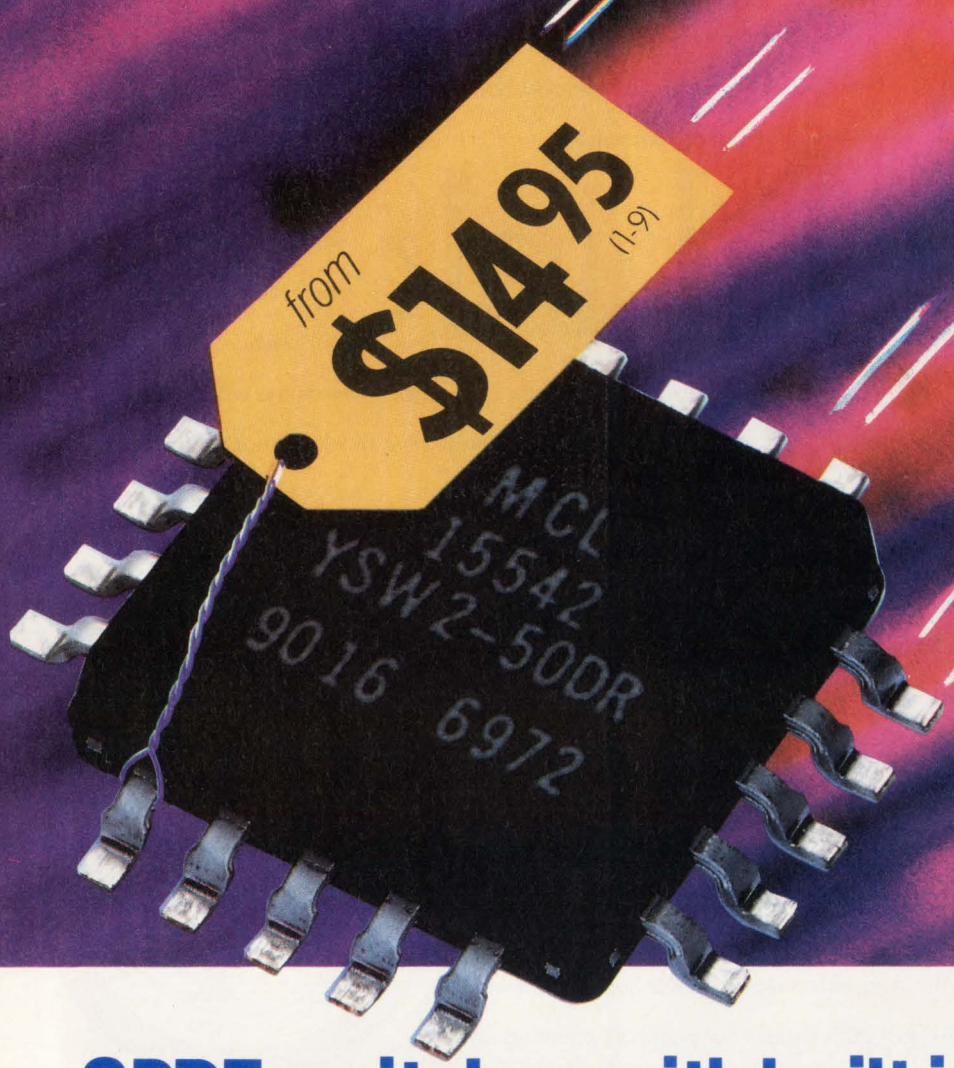
EDN MAGAZINE INNOVATION '92 & NEWS EDITIONS



WIN A FREE CALCULATOR!!! *By simply filling out the innovation ballot inside EDN's August 20th Special Innovation Supplement you can qualify to win a HP 48S Scientific Calculator. Valued at $250, this Hewlett-Packard calculator is the first calculator that enters equations in textbook style and provides interactive calculator graphics. But — just like the innovation finalists — only a select few will win so make sure to send in your ballot! By sending in your ballot, you are automatically entered in a random drawing to be held on September 30th. You will be notified by mail if you are a winner.*

EDN MAGAZINE EDITION NEWS EDITION

incredible!



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ABSORPTIVE or REFLECTIVE dc to 5GHz

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SPECIFICATIONS (typ)	Absorptive SPDT YSWA-2-50DR ZYSWA-2-50DR			Reflective SPDT YSW-2-50DR ZYSW-2-50DR		
Frequency (MHz)	dc-500	500-2000	2000-5000	dc-500	500-2000	2000-5000
Ins. Loss (dB)	1.1	1.4	1.9	0.9	1.3	1.4
Isolation (dB)	42	31	20	50	40	28
1dB Comp. (dBm)	18	20	22.5	20	20	24
RF Input (max dBm)	——	20	——	22	22	26
VSWR "on"	1.25	1.35	1.5	1.4	1.4	1.4
Video Bkthru (mV,p/p)	30	30	30	30	30	30
Sw. Spd. (nsec)	3	3	3	3	3	3
Price, $ (1-9 qty)	YSWA-2-50DR (pin) 23.95 ZYSWA-2-50DR (SMA) 69.95			YSW-2-50DR (pin) $14.95 ZYSW-2-50DR (SMA) 59.95		

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For detailed specs on all Mini-Circuits products refer to • THOMAS REGISTER Vol. 23 • MICROWAVES PRODUCT DIRECTORY • EEM • MINI-CIRCUITS' 740-pg HANDBOOK

F141 REV. D

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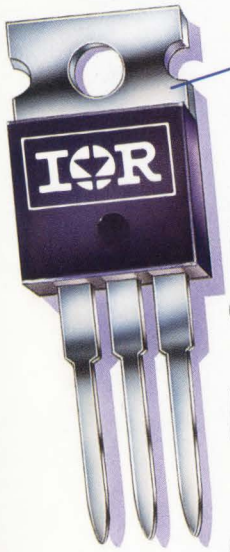

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