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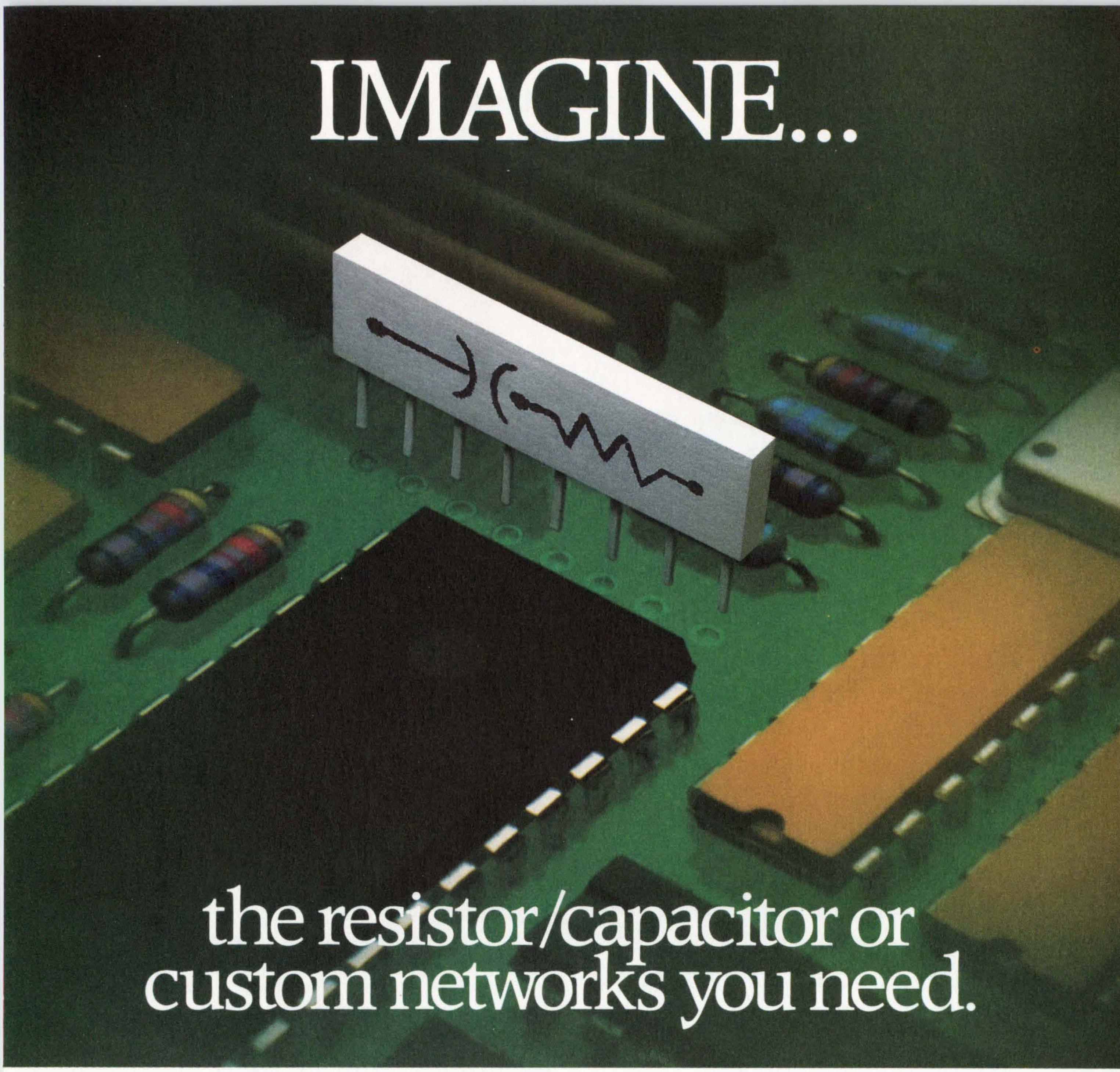
APRIL 25, 1991

EDN®

SPECIAL ISSUE:
Computers & Peripherals

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Special Report:
Cache design quickens memory reflexes pg 136



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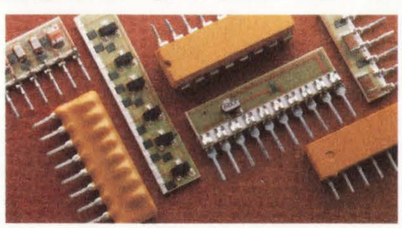

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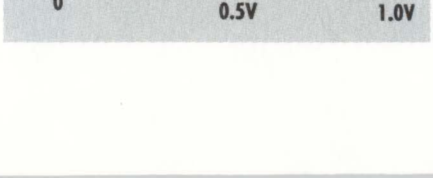

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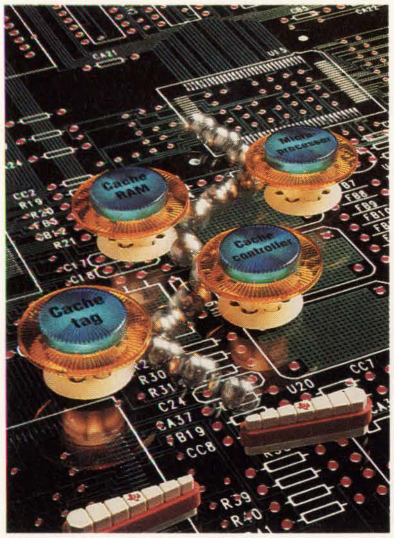
Volume 36, Number 9

EDN® Magazine Edition

April 25, 1991

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *Empower your system to set new performance scores by incorporating cache memory into your design. Serving as a buffer to the main memory, cache memory can speed your average memory-access time to as fast as 10 to 25 nsec. See our Special Report on pg 136. (Photo courtesy Texas Instruments Inc)*

COMPUTERS & PERIPHERALS SPECIAL ISSUE

INNOVATION™ Driving Electronic Technology Into The Next Century

Continued on page 7

EDN® (ISSN 0012-7515, GST Reg. #123397457) is published 48 times a year (biweekly with 2 additional issues a month, except for February, which has 3 additional issues and July and December which have 1 additional issue) by Cahners Publishing Company, A Division of Reed Publishing USA, 275 Washington Street, Newton, MA 02158-1630. Terrence M McDermott, President; Frank Sibley, Executive Vice President; Jerry D Neth, Senior Vice President/Publishing Operations; J J Walsh, Senior Vice President/Finance; Thomas J Dellamaria, Senior Vice President/Production and Manufacturing; Ralph Knupp, Vice President/Human Resources. EDN® is a registered trademark of Reed Properties Inc., used under license. Circulation records are maintained at Cahners Publishing Company, 44 Cook Street, Denver, CO 80206-5800. Telephone: (303) 388-4511. Second-class postage paid at Denver, CO 80206-5800 and additional mailing offices. **POSTMASTER:** Send address corrections to EDN®, PO Box 173377, Denver, CO 80217-3377. Ronald G Segel, Chairman and Chief Executive Officer; Robert L Krakoff, President and Chief Operating Officer; William M Platt, Senior Vice President. Annual subscription rates for nonqualified people: USA, $119.95/year; Canada/Mexico, $169.95/year; all other nations, $209.95/year for surface mail and $329.95/year for air mail. Single copies are available for $15. Please address all subscription mail to Ellen Porter, 44 Cook Street, Denver, CO 80206-5800.

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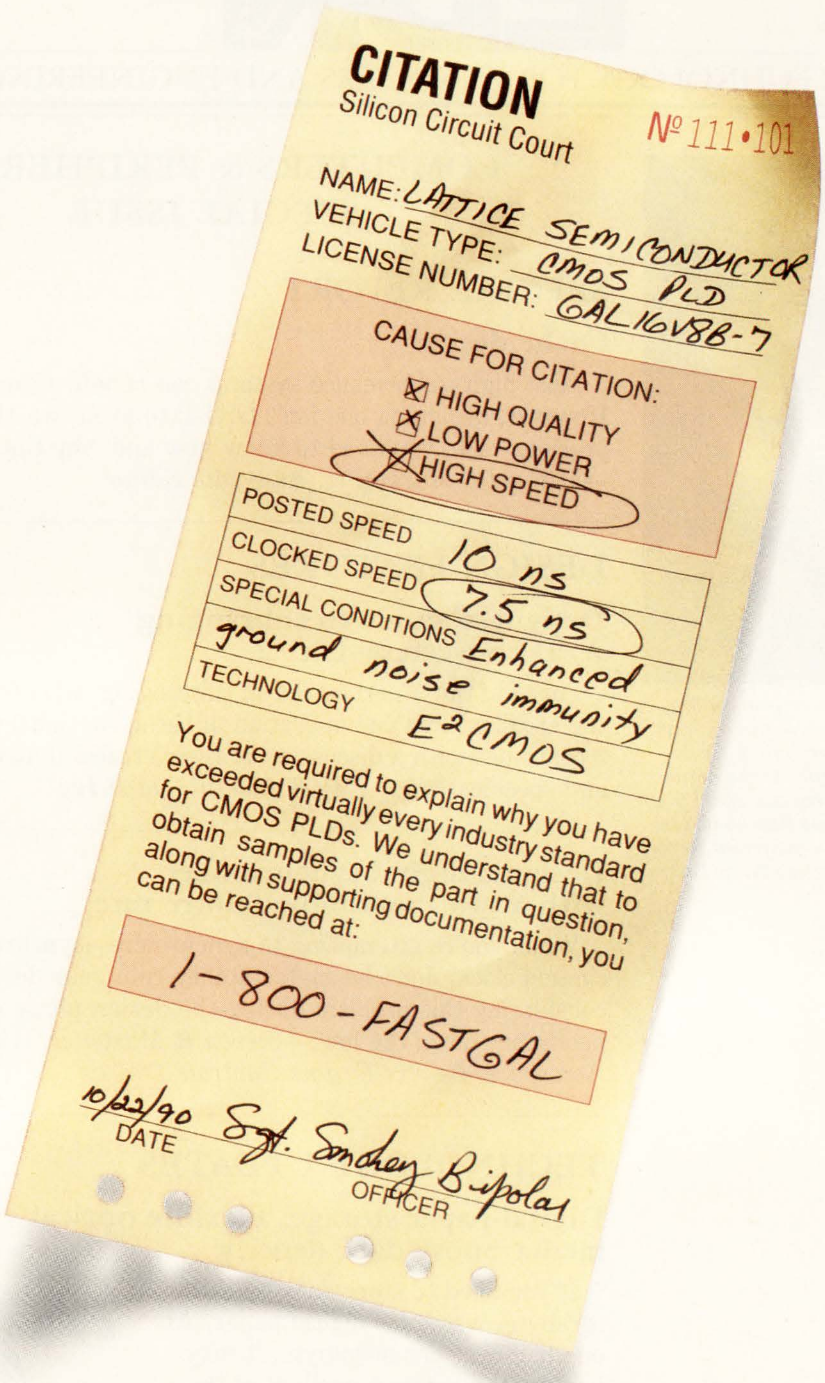
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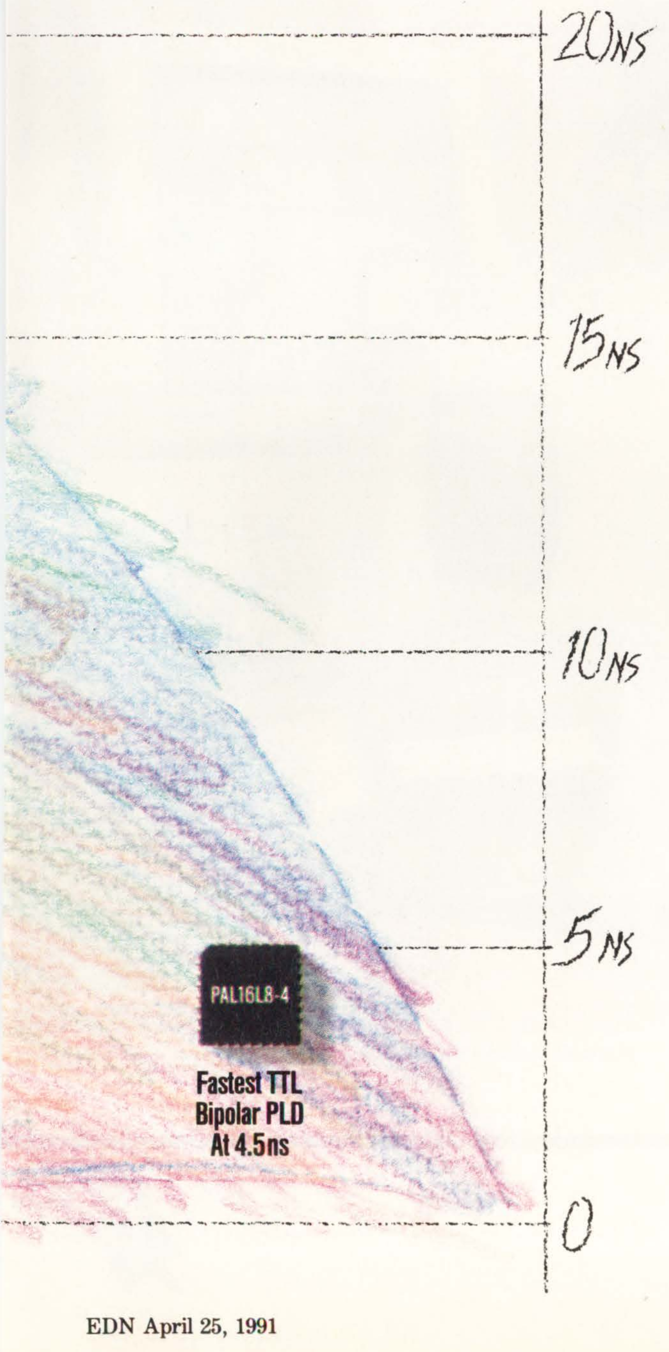

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CISC
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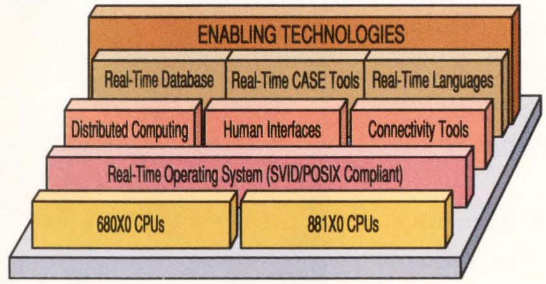

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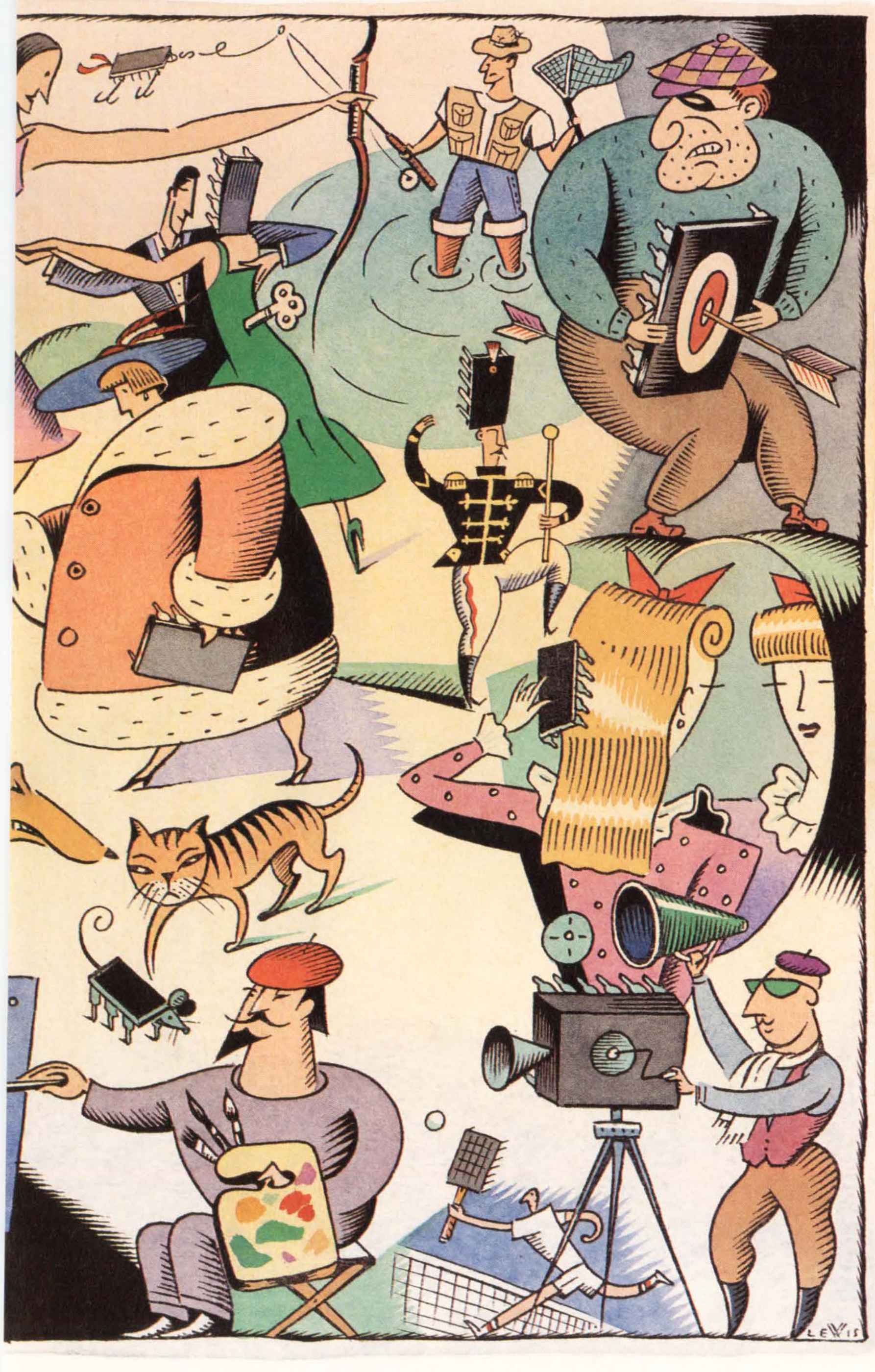

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NEWS BREAKS

EDITED BY SUSAN ROSE

SOFTWARE FINDS FAULTS AND CREATES TEST PATTERNS

CX-Test from Crosscheck Technology Inc provides a method of embedding test electronics onto an ASIC. The software creates test patterns and provides fault analysis using such manufacturing defects as bridging and open transistors in addition to the standard stuck-at faults. According to your vote (EDN, January 3, 1991, pg 41), it was the most innovative test and measurement product of last year. The software's embedded circuitry acts as a bed-of-nails tester to ensure high fault coverage for integrated circuits. The technology is available in arrays from LSI Logic (EDN, March 14, 1991, pg 18). The technology presents four design limitations: you must provide initialization and functional vectors; the circuit can't rely on stored charge at any node; you can't use internal free-running oscillators; and you must reserve four pins for the test bus.

The software accepts netlists and functional simulation patterns in Verilog or LSI Logic's Lsim format and creates patterns for synchronous and asynchronous designs and for circuits containing ROM and RAM. To run, the software requires at least 32M bytes of memory on Sun-3 and Sun-4 workstations. Cost depends on your configuration and ranges from $25,000 to $50,000. The software is currently available in LSI Logic design centers and will be available to ASIC designers in the fall. Crosscheck Technology Inc, San Jose, CA, (408) 432-9200, FAX (408) 432-0907. LSI Logic, Milpitas, CA, (408) 433-4554, FAX (408) 433-7241.—Michael C Markowitz

ASIC FOUNDRY SPINS OFF DESIGN-TOOL GROUP

In a move to make its design tools less proprietary, VLSI Technology Inc has spun off its design-tool business unit and made it a separate company. The new company, Compass Design Automation, will take the existing products and develop them for other vendors' ASIC processes and alternative CAE environments. Compass began its operations with 160 employees from the parent company. Compass Design Automation, San Jose, CA, (408) 433-4880, FAX (408) 434-7820. VLSI Technology, San Jose, CA, (408) 434-7726, FAX (408) 434-7931.—Steven H Leibson

486-BASED COMPUTER CACHE USES UNUSUAL ARCHITECTURE

Mosel's Simulcache consists of the MS441 cache controller and MS443 intelligent dual-port memory chips for 486-based systems. The chip set provides a concurrent write-back cache for 80486 μPs. Unlike other write-back schemes, these devices don't connect in parallel with main memory on the CPU bus. Instead, the dual-port devices fit between the CPU and the rest of memory, including memory-mapped I/O ports.

The controller absorbs CPU memory transactions and reorders them to meet the system's needs. It provides burst read and write between the CPU and cache, allows direct access between CPU and noncache memory, and handles read misses by simultaneously passing data to the CPU while updating the cache. The intelligent memories use an internal 128-bit memory bus, support 4-word bursts with 8-nsec access times, and offer 2-way set associativity. Samples of both devices will be available in the second quarter of 1991 with production slated for midyear. The cache controller costs $65 and the intelligent memories cost $9 (10,000). Mosel, Sunnyvale, CA, (408) 733-4556, FAX (408) 733-2271.—Richard A Quinnell

NEWS BREAKS

IC MULTIPLIES AND DIVIDES ACCURATELY

The $10.55 AD734 from Analog Devices Inc is a high-accuracy, low-distortion analog multiplier/divider. The device performs the mathematical function W = XY/U, where X, Y, and U are fully differential, analog-input signals. Operating with a small-signal and full-power bandwidth of 10 MHz, the device exhibits a slew rate of 450V/μsec, a S/N ratio of 94 dB, and a guaranteed conversion accuracy of 0.25% for high-grade devices. As a 4-quadrant multiplier, the IC can function as an oscillator, filter, or voltage-controlled amplifier. When connected as a 2-quadrant divider, the device can function as an AGC amplifier or an rms-to-dc converter. In multiplier mode, the denominator voltage U can be supplied internally from a 10V buried zener reference. Analog Devices Inc, Norwood, MA, (617) 329-4700, FAX (617) 326-8703. —Anne Watson Swager

12-BIT, 10M-SAMPLE/SEC ADC MODULE RUNS ON ±5V

The CLC922 ADC module from Comlinear Corp works in systems that need to perform 12-bit, 10M-sample/sec A/D conversions but have limited power supplies. The module incorporates an input amplifier, a low-jitter track-and-hold section, an onboard voltage reference, a 12-bit quantizer with error correction, and output latches. The device uses ±5V power supplies and consumes 4.1W. Guaranteed specs include a S/N ratio of 65 dB min, THD of −63 dB at 404 kHz and −57 dB at 4.996 MHz, 1-LSB-max differential nonlinearity, and no missing codes. The device also has a spurious-free signal ratio of 60 dB min. (This rating measures a converter's clean dynamic range.) Industrial and military versions of the module cost $470 and $1565 (100), respectively.

The company's CLC925B uses the same low-power circuits, but requires a 15V power supply in addition to the ±5V supplies. The additional power-supply voltage increases the module's power consumption to 4.2W. Industrial and military versions cost $449 and $1490 (100), respectively. Comlinear Corp, Fort Collins, CO, (303) 226-0500, FAX (303) 226-0564.—Steven H Leibson

DESIGN AUTOMATION CONFERENCE EXPANDS PROGRAM

This year the Design Automation Conference takes place at the San Francisco Moscone Center on June 17 to 21. Targeting CAD tool users, developers, and managers, the conference has evolved over the years from a strictly technical conference to a combination of technical presentations and product exhibits. More than 130 exhibitors will demonstrate their tools, and more than 64 of the exhibitors will give technical presentations. In addition, more than 40 technical conference sessions and seven tutorials are scheduled.

The conference program includes two industry-oriented panels on June 18. The first panel, "Global Strategies For Electronic Design," focuses on the interdependency of design-automation, and ASIC and systems companies, and their impact on global competition in the 1990s. The second panel, "Implementing the vision: Electronic design in the 1990s," will focus on the broader needs of system design.

You can obtain a free pass to the first day of the exhibits by registering before May 17. After May 17 registration is $20. One-day passes for technical sessions, including the panels, are $75. For more information, call MP Associates, (800) 321-4573 or (303) 530-4333, FAX (303) 530-4334.—Doug Conner

NEWS BREAKS

EMULATOR SUPPORTS 68302 μP

The 68302 UEM in-circuit emulator from Softaid Inc debugs Motorola's 68302 μP-compatible systems. The $6495 device provides 256k bytes of emulation memory, a 4k-byte-deep trace buffer, and 131,072 hardware breakpoints. You can set complex breakpoints using the emulator's 5-level nested-trigger specifier using a specific sequence of events, data values, machine cycles, and address accesses. A pass counter lets you delay the breakpoint by as many as 65,536 cycles. The source-level debugger included with the emulator lets you trace and debug your code in its native appearance using C, PL/M, or assembly language. The debugger works with the emulator's 256-bin real-time performance analyzer, so you can optimize your software on a function-by-function basis even when you're programming with a high-level language. The emulator will be available in May. Softaid Inc, Columbia, MD, (301) 964-8455, FAX (301) 596-1852.—Steven H Leibson

HIGH-DENSITY GATE ARRAY FEATURES SPECIALIZED LIBRARY

The LCA200K gate-array family from LSI Logic has 20,000 to 200,000 usable gates in a 0.7-μm, 3-metal-layer CMOS. The family also has a library of more than 1000 specialized macrocells. The cells include conventional logic, MIPS and SPARC CPUs, phase-locked loops for removing interchip system-clock skew, backplane drivers, and differential receivers. Although the chip runs at 5V, its I/O drivers are compatible with 3.3V logic. The I/O drivers also support the JTAG scan-test technique. NRE costs start at $75,000. LSI Logic, Milpitas, CA, (408) 433-4340, FAX (408) 434-6457, contact John Daane.—Richard A Quinnell

LOW-COST CPU CHIP EXPANDS 80486 μP FAMILY

Intel's 80486SX, a derivative of the basic 80486 μP, is a 32-bit μP chip that can upgrade 80386-based computer designs. The $269 (1000) chip is binary-code compatible with earlier 80386- and 80486-family μP chips. The company claims 16-MIPS performance at 20 MHz. The chip preserves the 32-bit data-bus architecture of its parent, but lacks floating-point math. The company expects to offer a $799 device that will supply floating-point math. For now the chips are simply basic 486 chips with disabled and unpowered floating-point math circuits. As production volume increases, the company will delete the floating-point math section of the 486 chip so that the derivative chip exists as a separate device. Pinouts of the two chips are not the same. The derivative chip is available in pin-grid-array and plastic packages. Intel Corp,. Santa Clara, CA, (408) 987-8080.—Jon Titus

DSP CARDS OFFER FAST, 16-BIT, FIXED-POINT PROCESSING

A pair of plug-in DSP cards from Spectrum Signal Processing Inc bring the signal-processing abilities of the Texas Instruments TMS320C50 to the IBM PC/AT bus. The $3495 system and $2495 processor boards combine the signal-processing μP with 32k bytes of program memory and 32k bytes of data memory. You can expand both memory areas to a maximum of 128k bytes. The system board includes two 16-bit ADCs and two 16-bit DACs capable of 50-kHz conversion rates. The boards also provide a 2.7 × 3.4-in. prototyping area for additional circuits. Loughborough Sound Images (Loughborough, England) developed the boards. Spectrum Signal Processing Inc, Burnaby, British Columbia, Canada, (604) 438-7266, FAX (604) 438-3046. —Steven H Leibson

NEWS BREAKS

HARDWARE MODELER STARTS A FAMILY

In an effort to lure more system designers into simulation, Logic Modeling Systems will deliver a lower-priced modeler. The 68020-based LM500 and 68040-based LM1200 hardware modelers aid system simulation by allowing you to augment your software models with actual devices configured as models. The 68020-based modeler, which starts at $35,000, models devices with as many as 160 pins. The $87,000, 68040-based modeler simulates 320-pin devices. Both modelers allow simulations to use multiple hardware models, limited only by total pin count—480 signal pins total for the 68020-based modeler and 2560 for the 68040-based modeler. Although its library of models numbers 600 and includes such devices as the i486, 29050, 68040, and R3000A, the company estimates you can build a model for any device you need in less than two days. Both modelers will be available by the end of June. Logic Modeling Systems Inc, Milpitas, CA, (408) 957-5200, FAX (408) 945-9181.
—Michael C Markowitz

AUDIO INSTRUMENTATION AMP FEATURES LOW INPUT NOISE

A distortion-cancellation network on the input of the INA103 monolithic instrumentation amplifier drops the device's input-voltage noise figure to 1 nV/$\sqrt{\text{Hz}}$ typ and its THD-plus-noise rating to 0.0009% (gain = 100, 1 kHz). The amp's offset voltage is 52 μV max, and the input-offset voltage drift is 1.25 μV/°C. On-chip resistors give the device a gain of 1 or 1000 without additional components, and an external resistor can vary the amp's gain from 1 to 1000. At a gain of 1000, the amp provides a flat frequency response to approximately 20 kHz. A device packaged in a 16-pin plastic DIP costs $4.85 (1000) and ceramic-packaged devices are also available. Burr-Brown, Tucson, AZ, (602) 746-1111, FAX (602) 889-1510, TWX 910-952-1111, contact John Conlon.—Steven H Leibson

TRANSMISSION-LINE ANALYSIS TOOLS UPGRADED

Quantic Laboratories offers a range of transmission-line analysis tools from its Boardscan board screener up through detailed 2- and 3-D analysis using its Greenfield products. The board screener includes signal-integrity specs such as overshoot, undershoot, settling time, noise margins, time delays, and crosstalk. The analyzers' component libraries of drivers and receivers accept Spice transistor-based device models and behavioral models for increased simulation speed. The products are now available unbundled so you can obtain only the tools you need. The board screener starts at $15,000, and the analyzers start at $24,000. Quantic Laboratories Inc, Winnipeg, Manitoba, Canada, (204) 943-2552, FAX (204) 957-1158.—Doug Conner

VIDEO ACCELERATOR STANDARD FEATURE FOR WORKSTATION

The SPARC-based S4000 series of color workstations from Solbourne Computer includes accelerated 2-D graphics at no additional cost. Prices range from $11,495 for a diskless workstation with 8M bytes of RAM and a 16-in. color monitor to $22,095 for a workstation with a 400M-byte disk drive, 40M bytes of RAM, and a 19-in. color monitor. The company's SGA20 accelerated color-frame buffer provides the improved graphics. The buffer can draw 530,000 2-D vectors/sec and can fill areas on the screen at 215M pixels/sec. The workstations accept as many as three SGA20s if you need multiple displays. Solbourne Computer Inc, Longmont, CO, (303) 772-3400, FAX (303) 772-3646.—Steven H Leibson

Z I L O G

Introducing Zilog's Smart Access Controller... Z180 intelligence and SCC communications together in one package.

Don't throw away your old software.

The Z80 family continues to be the most popular group of intelligent peripheral controllers on the market. With good reason. It's a tribute to our Superintegration™ technology and the performance of the controllers themselves. And since each new product in the family, like the SAC™ is based on the same Z80/180 code you'll be able to migrate your existing software easily and effectively. We don't have to tell you how important that is.

Here's a list of the fast-growing family of Z80-based intelligent peripheral controllers. It's a list that's not likely to stop expanding any time soon... stay tuned.

INTELLIGENT PERIPHERAL CONTROLLERS

	System					Serial			Timers		Parallel	
	CPU	OSC	MMU	RAM	DMA	USART	UART	C/S	CTC	C/T	PIA	PIO
Z84C01	✓	✓										
Z84C50	✓	✓		✓								
Z84C90		✓				✓			✓		✓	✓
Z80180	✓	✓	✓		✓		✓	✓		✓		
Z80280	✓	✓	✓	✓	✓		✓			✓		
Z84013/C13	✓	✓				✓			✓			
Z84015/C15	✓	✓				✓			✓			✓
Z84011/C11	✓	✓							✓			✓
Z80181	✓	✓	✓		✓	✓	✓	✓	✓	✓		✓

The Z80181™ SAC™ Controller is the Smart Access Controller™ that combines two powerful standards. You get Zilog's industry standard SCC™ controller for datacom connectivity together with the popular Z180 CMOS controller. And all that utility comes with the user-friendly Z80® code CPU compatible software.

High integration. High performance. Smart communicator.

The Superintegration™ SAC Controller packs the popular high performance Z180 architecture into a new cell suitable for many datacom and peripheral control applications. You get the SCC single-channel communication cell with two additional UARTS, a 4 x 8-bit counter timer (CTC) *and* onboard 16-bit I/O. The SAC Controller runs at 10 MHz and drives fast serial communications at 2.5 Mbits/sec. With the reduced 3 cycles per instruction, the SAC Controller gives you Z80 code performance 25% faster. That makes the SAC Controller the highest performance, low power embedded controller around.

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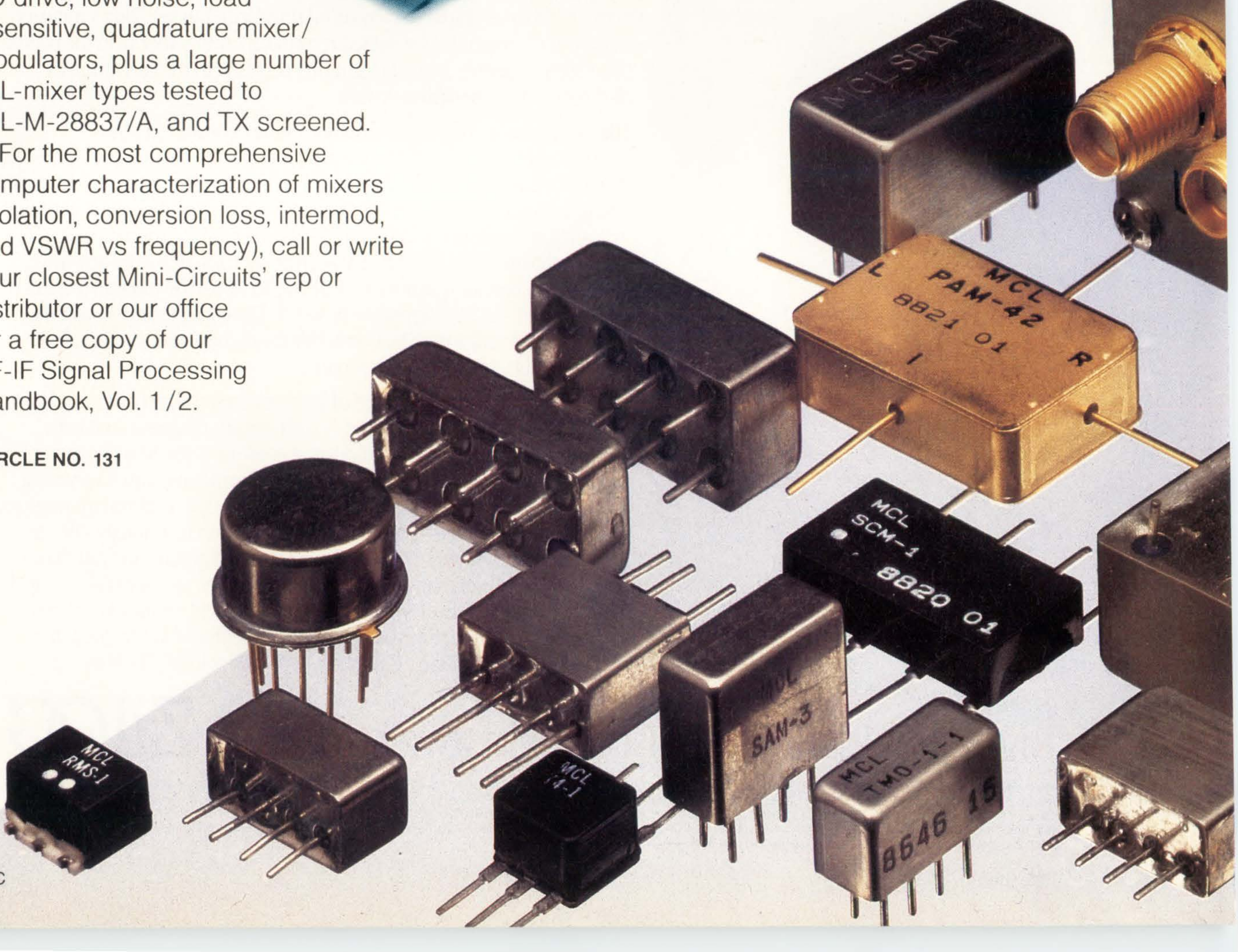
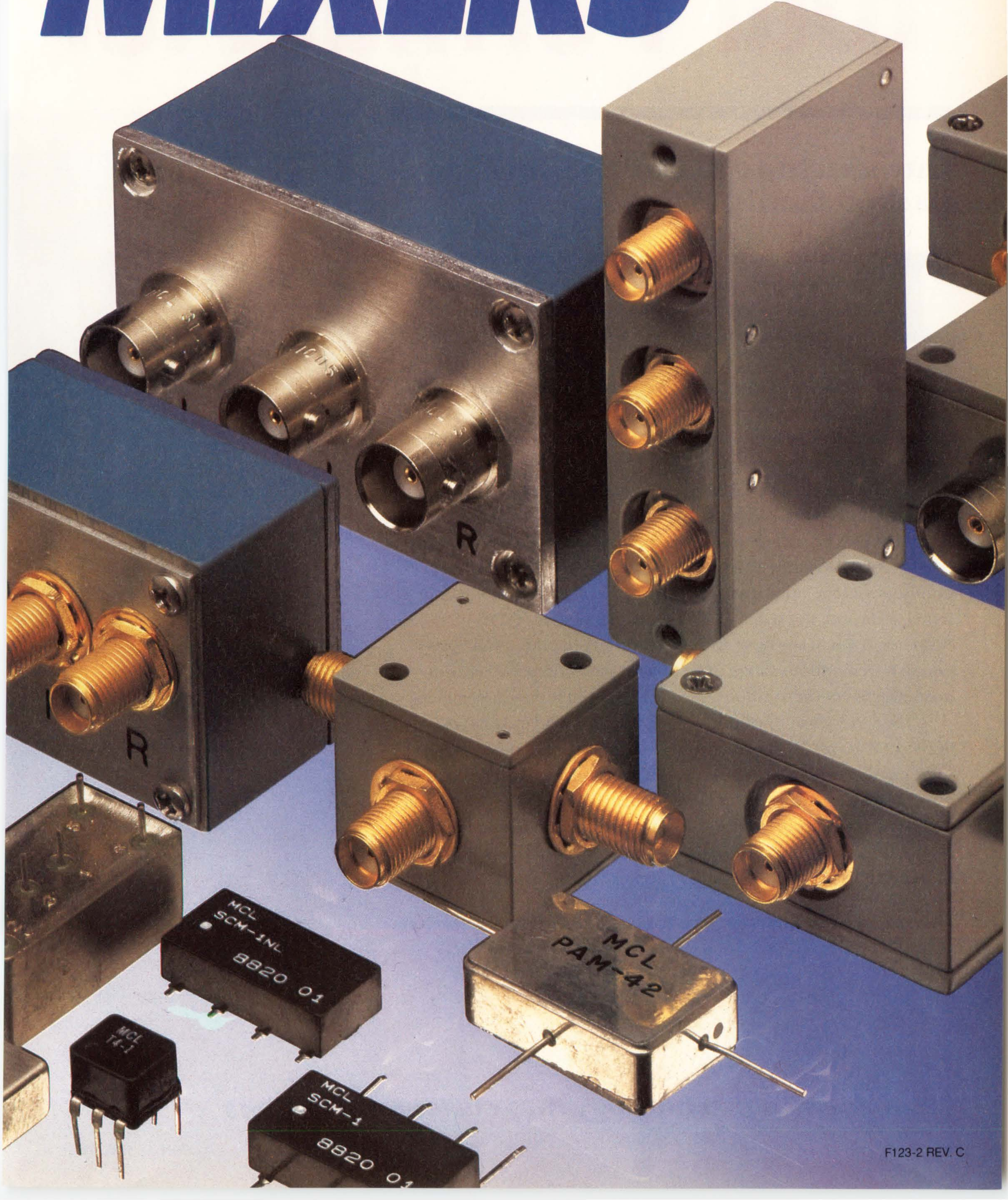
CIRCLE NO. 131



F123-1 REV. C

MIXERS



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Part #	Features	ROM	RAM	Package
65511	32 I/Os, 2x8-bit timers, watchdog timer, serial I/O	4KB	128B	40-DIP 44-PLCC/QFP
65512/ 65P512	32 I/Os, 3x8-bit timers, 1x16-bit timers, serial I/O	8KB	128B	40-DIP 44-PLCC/QFP
65513/ 65P513	Same as 65512 with 24 additional I/Os	8KB	128B	64-SDIP/QFP 68-PLCC
65524/ 65P524	Same as 65512 with 2x8-bit PWM, 8-bit A/D, additional ROM/RAM	16KB	384B	64-SDIP/QFP 68-PLCC
66201/ 66P201 66207/ 66P207 66301/ 66P301	• 48 I/Os • 10-bit A/D • 4x16-bit timers • 2x16-bit PWM • Serial interface • Transition detector	16KB 16KB 32KB	512B 512B 1KB	64-SDIP/QFP 68-PLCC 64-SDIP/QFP 68-PLCC 64-SDIP/QFP 68-PLCC
66417/ 66P417	68 I/Os, 10-bit A/D, 3x16-bit timers, 4x16-bit PWM, serial interface	32KB	1KB	80-QFP
67620/ 67P620	56 I/Os, 3x16-bit timers, 2x8 bit timers, serial interface	16KB	512B	64-SDIP/QFP 68-PLCC

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CIRCLE NO. 133

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Technically speaking, no one builds more advanced thin-film discs and recording heads than Seagate. These core technologies help us put 3 gigabytes of storage in a box the size of a toaster. And because we design our own components, we can bring our new products to market faster.

Of course, a key consideration in building our own parts is the cost. By controlling the manufacturing process down to the component level, we can have a significant impact on the cost of our finished products. The end-result is a better value for the customer without sacrificing quality or performance.

In terms of availability, it's important to know that Seagate shipped over 7 million disc drives last year alone. With volumes like these, building our own components helps us avoid the parts shortages that often plague other disc drive manufacturers.

Most importantly, vertical integration allows us to maximize the quality of every component we produce. With the industry's most advanced equipment and testing techniques, we consistently turn out components and finished products that are beyond reproach.

Obviously, it takes an extraordinary capital investment to pursue this strategy. But the disc drive companies who control their critical component production will be better able to control their own destinies, as well as those of their customers.

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Questions about PLL article

I'd like to comment about the article, "Technique eases design of phase-locked loops" (EDN, August 20, 1990, pg 141). I appreciate seeing this subject published.

However, I found two weak areas in the article. The first area involves the included C-language listings, *Listing B-Key routines used in optimizing PLLs based on the 4046 IC*. When including source code, sparse commenting and the inclusion of calls to subroutines not included in the listing only add to a reader's difficulty in understanding the code. I refer to the subroutine calls, **components()** and **scan2()**. What does "components" do for the program? If it is to read component values, then which components?

Also related to the listing problem is the vagueness of program execution. Which subroutine is executed first, last? In my opinion, had Fred Salvatti omitted the C-code listings, he would not have hindered the technical quality of the article.

The second area with which I'm concerned involves the last paragraph. "You can obtain...the program...for $19.95. Send your request to the author." Surely the cost of a 5¼-in. floppy disk cannot be as high as $20.00. It appears that Fred Salvatti intends to make a profit, small as it may be. That being the case, wouldn't this work classify as an advertisement, and if so, should you not charge the author for advertising space? One might infer that EDN employed unfair discriminatory advertising practice.

Glenn T Inn
Engineering Manager
Sera Solar Corp
Palo Alto, CA

(The author's reply: I'm sorry that Glenn Inn takes offense at the incomplete listing of my program in my article (EDN, August 17, 1990, pg 141). The program is too long to be printed in its entirety. I'm sure the editors did their best to give the readers the maximum amount of information in the space available.

Concerning Glenn's first question: What does "components()" do? Components() is the function that displays the 4046 menu. In answer to Glenn's second question, scan2() is the function that responds to selections from the 4046 menu.

As to my making a profit, my time is worth more than $25 an hour. It takes me about an hour to copy the program to a disk, test the disk for correct operation, write a personal letter explaining something about the program, package the disk, address the package, and finally go to the post office to mail *it. At this point I'm already in the hole more than $5, not to mention all the hours it took to develop the equations and write and debug the program. Surely as an engineering manager, Glenn can see that there's no way I'm making a profit. And, incidentally, I did this work on my own time.)*

How do engineers, et al, fare in the marketplace?

In the article, "The Job-Hunting Blues" (EDN, January 21, 1991, pg 230), Julie Schofield is too kind to big business.

Businessmen are politicians who find some gadget to sell the government or other big business. They [receive] a little money from bankers and a lot of money from suckers; they find talented, but naive people, and they put together a little military machine that obeys the tenets of Socrates, Adam Smith, F W Taylor, Gantt, and others. The politicians and their cronies get rich! The exploited talent and the exploited labor get old or stale. When people see riches passing under their noses, they may want to share in those riches. But people are expendable, so they get expended.

I could let off steam for thousands of pages, but you get the message.

Robert C Gibson
Consulting Engineer
Aurora, IL

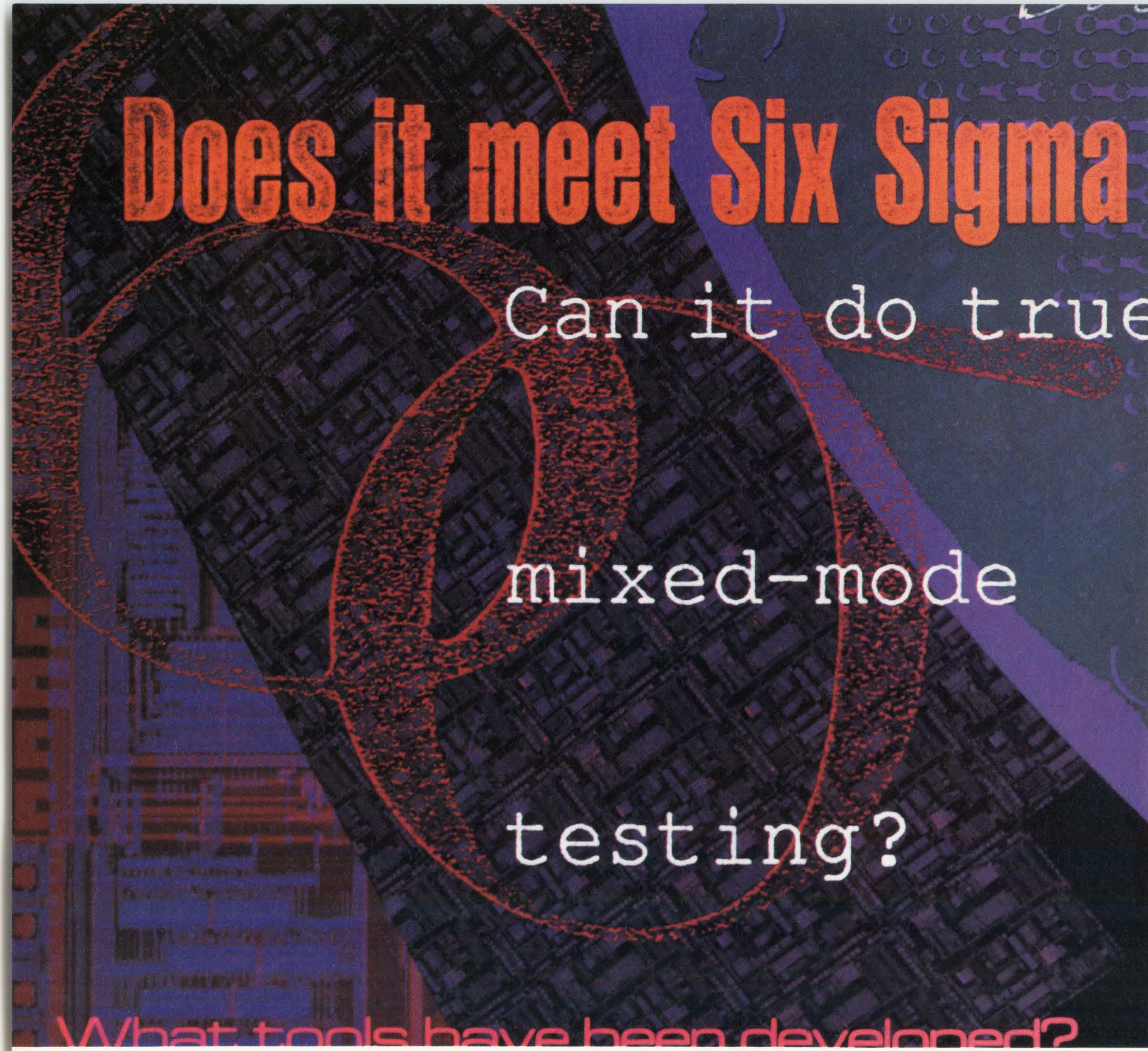
Who did it?

We inadvertently neglected to let you know that Intel Corp supplied the cover photograph for EDN's March 28 Software Engineering Special Supplement. Apologies to all concerned.

IT'S EASY TO HAVE YOUR SAY

EDN's Signals & Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. You can use one of several easy ways to reach us. First, there's always the mail. Send your letters to Signals & Noise Editor, EDN Magazine, 275 Washington St, Newton, MA 02158. Or, send us a message via MCI mail at EDNBOS. Finally, EDN's bulletin-board system is ready for use—and it's free (except for the phone call). You can reach us at (617) 558-4241 and leave a letter in the EDITORS Special Interest Group. You'll need a 2400-bps or less modem and a communications program that is set for eight data bits, no parity, and one stop bit, or 1200/2400, 8N1 in shorthand.

EDN



Before the A500 started testing Motorola's mixed-

"Motorola has adopted a Six Sigma initiative which focuses attention on approaching zero-defect performance in everything we do, including our test systems. Our purchase of the Teradyne A500 test system supports our Six Sigma initiative and our competitive leadership challenge."

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Motorola knows you can't have a Six Sigma process unless you can test to Six Sigma standards. That's why Motorola's MOS Digital-Analog Integrated Circuits Division chose the Teradyne A500 Analog VLSI Test System. Because, in addition to proving the A500 could handle the complex technical requirements of Motorola's advanced ISDN interfaces, we also demonstrated that we could perform to Motorola's stringent quality levels.

"Can it do scan testing? Digitize high-frequency waveforms? Do true mixed-mode testing? Does it have a flexible architecture? Can you give us the support for a Six Sigma process? Applications expertise? Complete documentation? The right tools? In each case, Teradyne answered yes."

Manager, Advanced Test Technology

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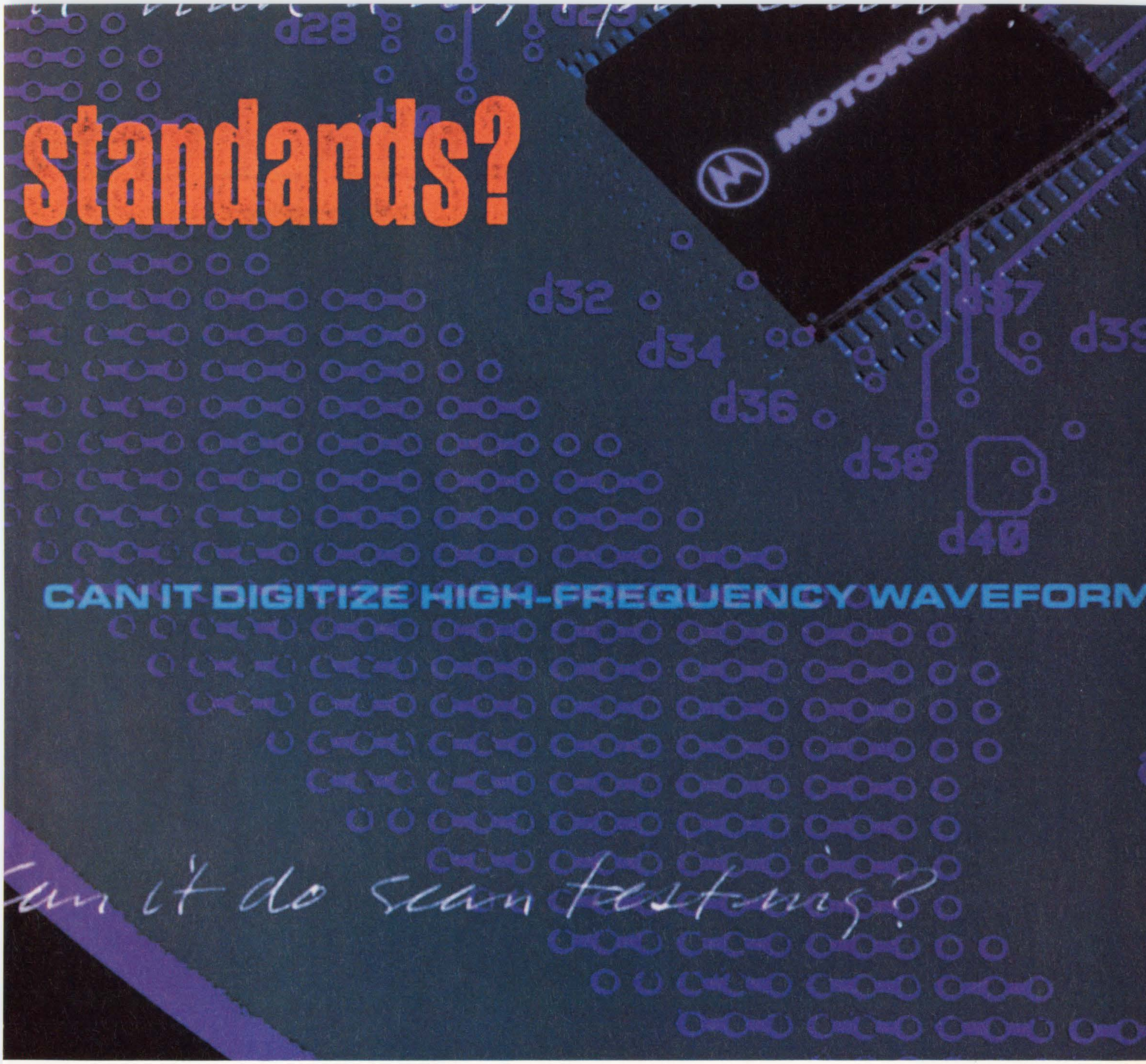

signal technology, Teradyne had to pass a few tests.

With the A500, Motorola had the ability to digitize waveforms at 20 MHz, plus the high pin count necessary to guarantee that their ISDN U-Interface worked the way it was supposed to.

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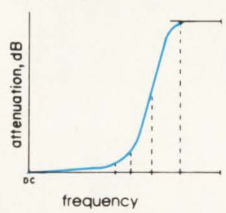
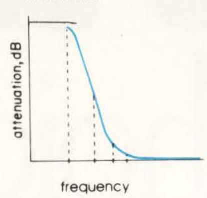
LOW PASS



low pass dc to 1200MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	(loss>40dB) Max.	Min.	VSWR pass-band typ.	stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45

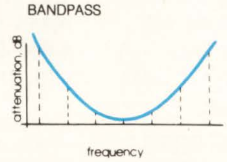
HIGH PASS



high pass dc to 2500MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	(loss>40dB) Min.	VSWR pass-band typ.	stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95

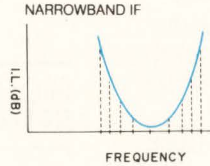
BANDPASS



bandpass 20 to 70MHz

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	Max. F4	(loss > 20 dB) Min. F5	Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95

NARROWBAND IF



narrowband IF

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	F6	STOP BAND, MHz I.L. > 35dB F7	F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

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ASK EDN

EDITED BY JULIE ANNE SCHOFIELD

Have you been stumped by a design problem so long that you don't know who to turn to? Are you having trouble locating parts? Finding companies? Can't interpret a spec sheet? Ask EDN.

This department will serve as a forum to solve nagging problems and answer difficult questions. EDN's editors will provide the solutions. If we can't solve a problem, we'll find an expert who can, or we'll print your letter and ask your peers for help. We can't answer every question, but we'll try to publish the ones that will help you most in your job.

Address your letters to Ask EDN, 275 Washington St, Newton, MA 02158. FAX (617) 558-4470; MCI: EDNBOS. Or, send us a letter on EDN's bulletin-board system. You can reach us at (617) 558-4241 and leave a letter in the /ask_edn Special Interest Group.

Searching for synchronous ICs

Is there a PWM current-mode integrated circuit that can be synchronized to a like circuit by merely connecting one pin of each IC together? This synchronization would be similar to that achieved by connecting two SG1525As. I'd appreciate your help.
Michel Masse
Woodland Hills, CA 91364

Associate Editor Dave Pryce replies: The synchronization you refer to for the voltage-mode SG1525A usually takes the form of a sync input to the oscillator section of the PWM regulator. This sync pin enables the user to slave together multiple units or to synchronize a single unit using an external clock.

A number of current-mode regulators have a sync input pin to the oscillator. Among them are the CS-3865 from Cherry Semiconductor; the LT1846, SG1846, and UC1846 from Linear Technology, Silicon General, and Unitrode, respectively; and the SG1528/SG1530 combination current-mode/voltage-mode chip from Silicon General.

Check with these companies to determine if these chips will perform properly in your particular application. For example, the CS-3865 is a dual unit, and the sync pin may only serve to control each internal unit. Each company offers an extensive line of switching regulators and can provide capable applications support:

Cherry Semiconductor Corp
2000 South County Trail
East Greenwich, RI 02818
(401) 885-3600
FAX (401) 884-0790

Linear Technology Corp
1630 McCarthy Blvd
Milpitas, CA 95035
(408) 432-1900
FAX (408) 434-0507

Silicon General
11861 Western Ave
Garden Grove, CA 92641
(714) 898-8121
FAX (714) 893-2570

Unitrode Integrated Circuits
7 Continental Blvd
Merrimack, NH 03054
(603) 424-2410
FAX (603) 424-3460.

Short persistence pays off

Can you tell me where I can purchase CRT projection tubes with short persistence—less than 1 msec? We need such tubes for shuttered 3-D video projection.
Mohammed Arif
Heinrich-Hertz-Institut für Nachrichtentechnik
Berlin, Germany

Among the companies that sell such tubes are

Hitachi America Ltd
2210 O'Toole Ave
San Jose, CA 95131
(408) 435-8300

Video Display Corp
1868 Tucker Industrial Dr
Tucker, GA 30084
(404) 938-2080

Litton Systems Inc
Electron Devices Div
1215 S 52nd St
Tempe, AZ 85281
(602) 968-4471.

Another obsolete part

I am trying to locate an A/D converter once manufactured by National Semiconductor. The part number is MM5863N, and the device is at least 10 years old. National Semiconductor no longer makes it or has a second source for it. Can you help me locate a source for this device?
Tony De Carvalho
Repair and Product Development Manager
Webb Communications Inc
Tampa, FL

If any reader has a secret stash of MM5863Ns, please drop Ask EDN a line.

EDN

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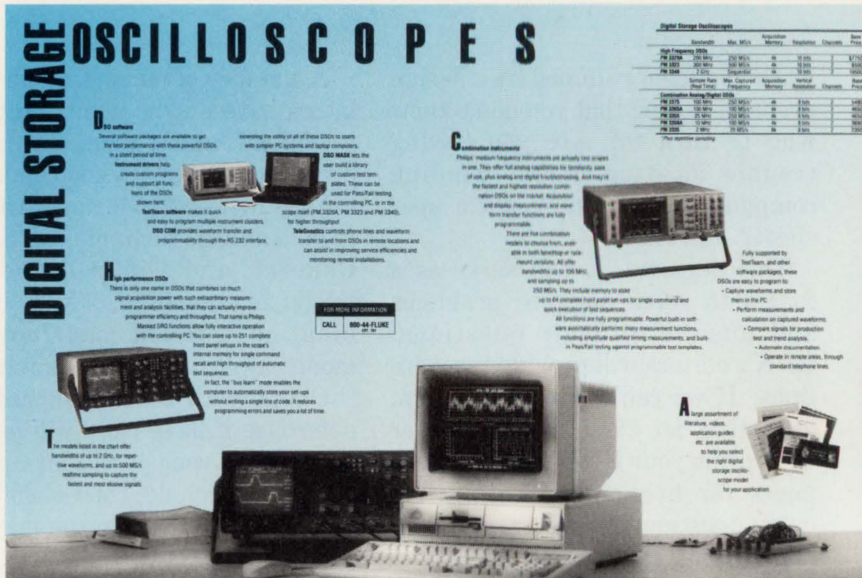

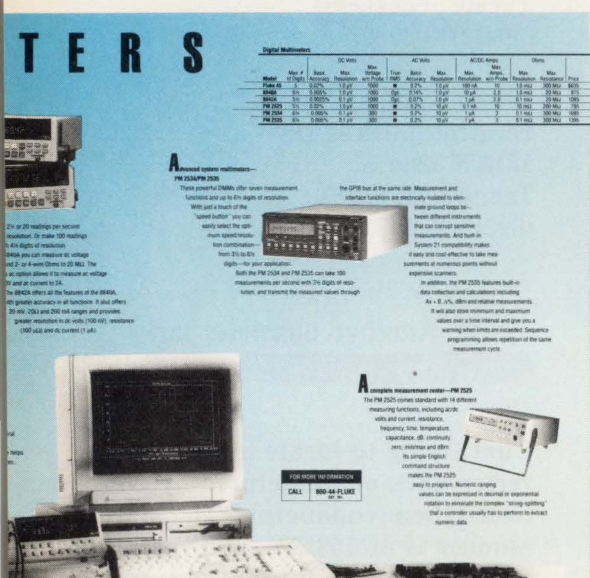

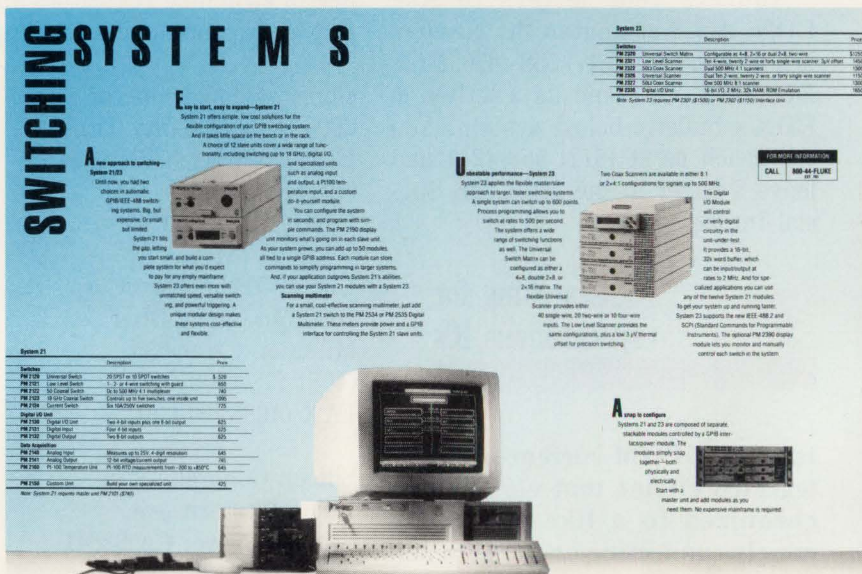

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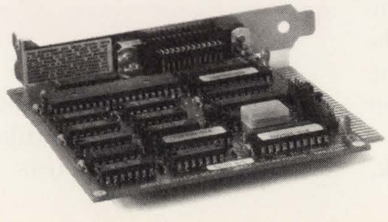

Nor will you be able to take advantage of our other free offer: Buy a power supply or switching system, plus any GPIB instrument and get a $595 PC GPIB interface card.

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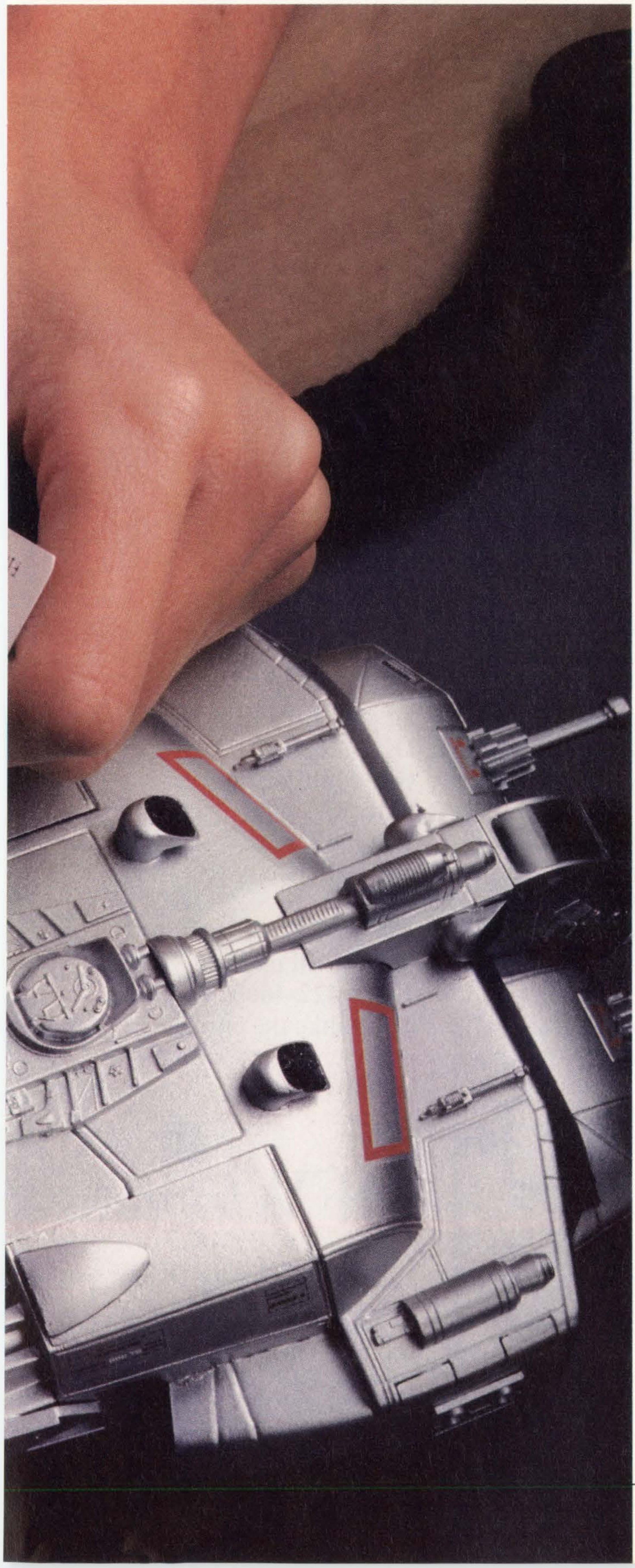
to Price Wars



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Symbol Technologies is a good example. A tiny Raytheon instrumentation amplifier helped them combine both bar code scanner and decoder in a single, lightweight, handheld unit—that's tough enough to take a five foot drop onto concrete.

Symbol also took advantage of our *Win-Win* program. It let them get to market quickly with a semicustom array, then shift to full custom as sales volumes increased.

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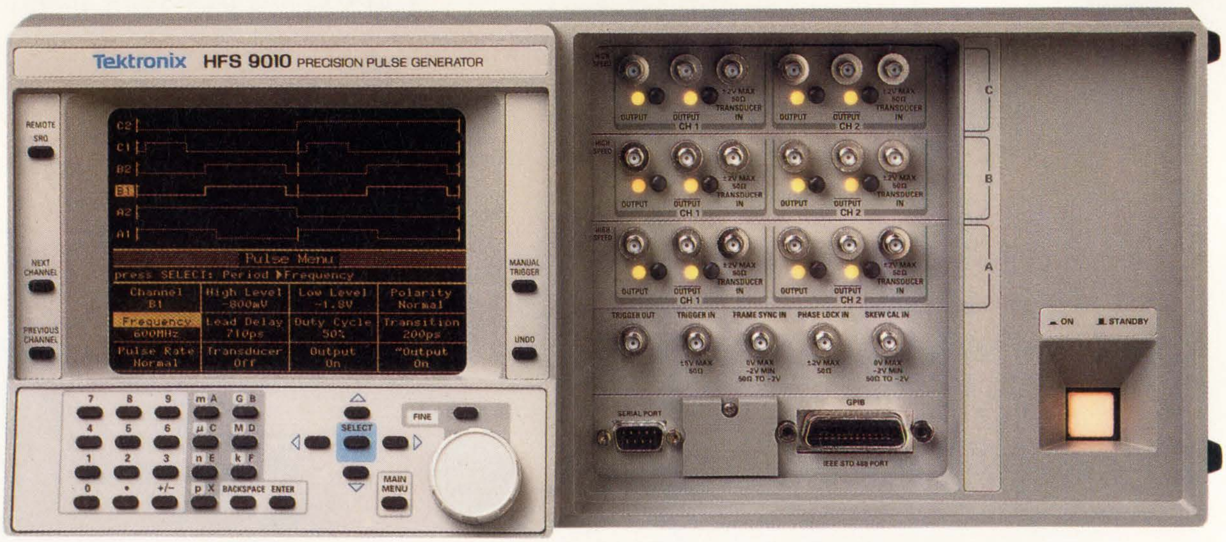

You're looking at the biggest news in signal sources in years: two new families of pulse generators from Tektronix.

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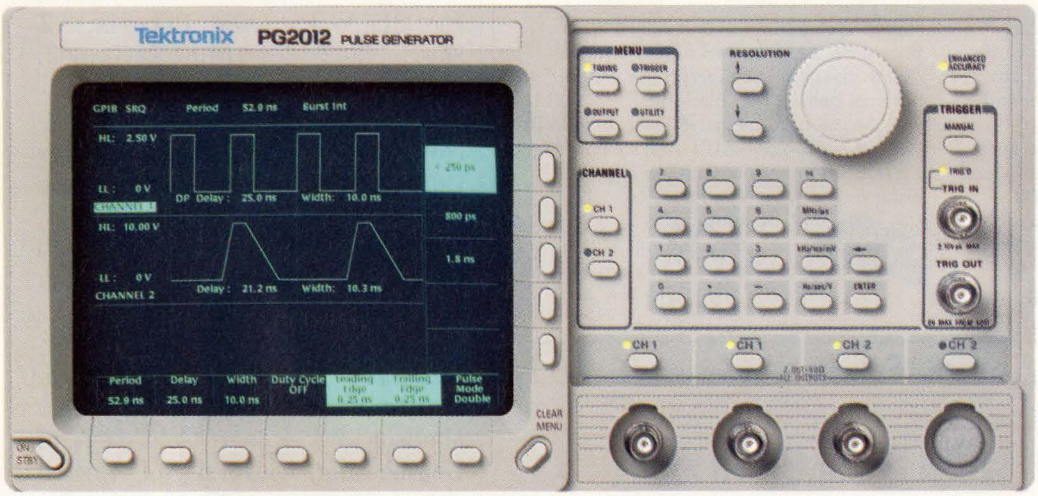

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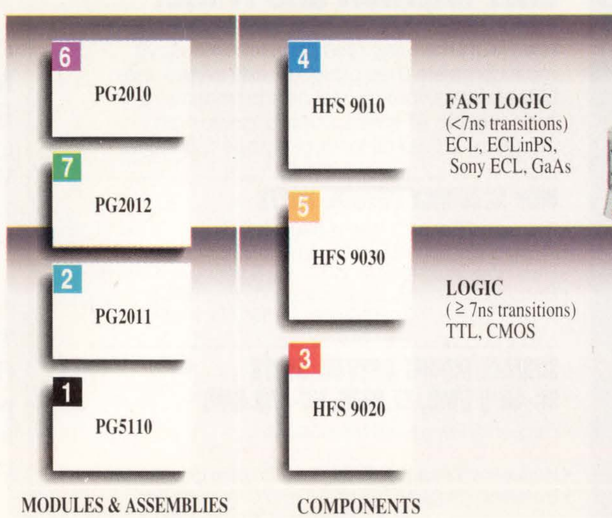

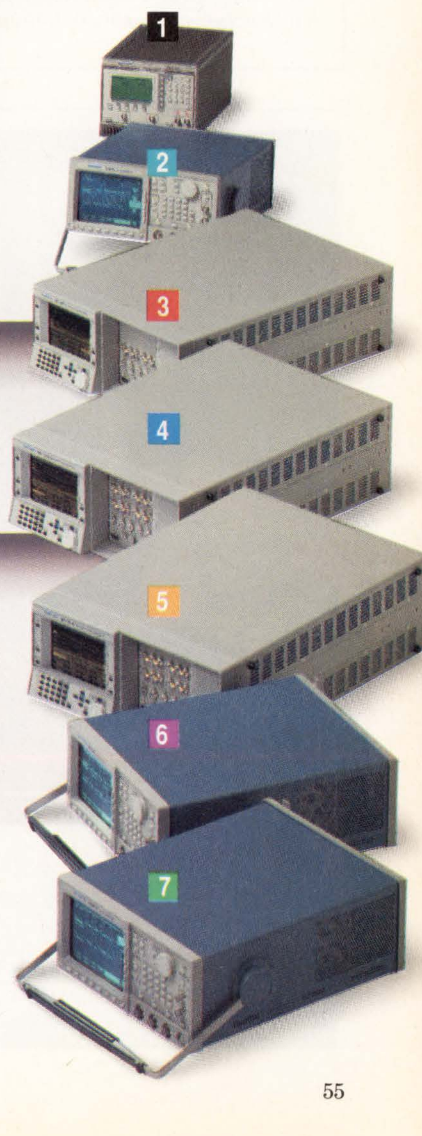

One company measures up.

Tektronix
COMMITTED TO EXCELLENCE

CIRCLE NO. 142

CALENDAR

Monterey Software Conference, Monterey, CA. Digital Consulting Inc, 204 Andover St, Andover, MA 01810. (508) 470-3880. April 30 to May 2.

Seventh Annual Semiconductor Forum, Phoenix, AZ. In-Stat Inc, Box 8130, Scottsdale, AZ 85252. (602) 860-8515. FAX (602) 860-1863. May 5 to 8.

MIL-STD-1533 Seminar, Phoenix, AZ. Mike Milburn, Test Systems Inc, 217 W Palmaire, Phoenix, AZ 85021. (602) 861-1010. FAX (602) 861-1082. May 7 to 8.

North American MAP/TOP User Conference, Nashville, TN. Steve Sickels, COS, 1750 Old Meadow Rd, Suite 400, McLean, VA 22102. (703) 883-2704. FAX (703) 848-4572. May 7 to 9.

Reliability Engineering for Electronic Products (short course), Madison, WI. Robert Gold, Dept of Engineering, University of Wisconsin at Madison, 432 N Lake St, Madison, WI 53706. (800) 462-0876. May 8 to 10.

Custom Integrated Circuits Conference (CICC), San Diego, CA. Roberta Kaspar, Technical Program Coordinator, 1597 Ridge Rd W, Suite 101C, Rochester, NY 14615. (716) 865-7164. FAX (716) 865-2639. May 12 to 15.

41st Electronic Components and Technology Conference, Atlanta, GA. Jim Bruorton, Publicity Chairperson, ECTC, KEMET Electronics Corp, Box 5928, Greenville, SC 29606. (803) 963-6621. May 13 to 15.

Applications of Unix Utilities (short course), Seattle, WA. Specialized Systems Consultants Inc, Box 55549, Seattle, WA 98155. (206) 527-3385. FAX (206) 527-2806. May 14.

UXART
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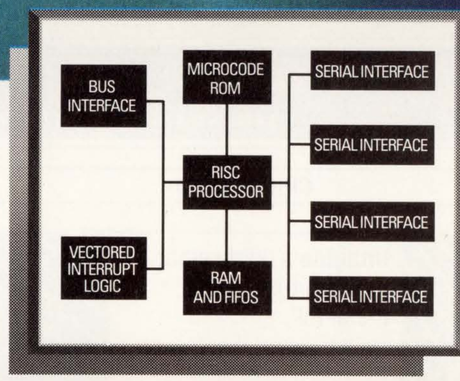
Now there's a serial I/O chip designed for UNIX.



For years, dumb UARTs have been the standard datacom solution. Now there's something better for today's multi-user, multi-protocol datacom environment. Our single-chip solution gives you multiple channels — each capable of full-duplex operation at 115.2 kbps — and replaces up to 10 chips.

Cirrus Logic introduces the UXART — the first and only UART with specific features to simplify and speed up serial I/O efficiency by a factor of ten or more. So your UNIX® system can support more users, with better response time — and less waiting.

The CL-CD1400 UXART™ gives you 4 fully independent datacom channels, each capable of full-duplex operation at 115.2 kbps. Each channel has two 12 byte FIFOs, one for transmit and one for receive. Separate vectored interrupts allow quick entry to the correct service routine.

A number of features reduce the load on the host system. Automatic expansion of Newline to CRNL, plus other CR and NL options. User-definable flow control characters for automatic flow control. All five types of UNIX-specified parity and error handling. And more.

For high-line-count, cost-effective applications, there's the CL-CD180. It offers performance gains similar to the CL-CD1400, plus the advantage of 8 channels in a single 84-pin package.

The CL-CD2400 adds synchronous capabilities. It offers 4 independent, multi-protocol channels, plus an on-chip DMA controller for fast, efficient I/O.

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An on-chip 10 MIPS RISC-based processor handles transmit and receive functions, buffer management, flow control, and all special character processing. On-chip FIFOs reduce host interrupts to give you more efficient interrupt handling. The result: faster system throughput, lower host overhead, and less waiting.

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CALENDAR

Project Management: Skills For Success (short course), San Francisco, CA. Learning Tree International, Box 45028, Los Angeles, CA 90045. (800) 421-8166; in Canada, (800) 267-1824. May 14 to 17.

American Consulting Engineers Council Annual Convention, Baltimore, MD. ACEC, 1015 15th St NW, Washington, DC 20005. (202) 347-7474. May 19 to 23.

International Semiconductor Manufacturing Science Symposium (ISMSS), Burlingame, CA. SEMI, 805 E Middlefield Rd, Mountain View, CA 94043. (415) 964-5111; (415) 940-6901. May 20 to 22.

ANSYS International Conference And Exhibition, Pittsburgh, PA. Jennifer D'Orazio, Swanson Analysis Systems Inc, Box 65, Houston, PA 15342. (412) 746-3304. FAX (412) 746-9494. May 20 to 24.

Midwest Electronics Exposition, Minneapolis, MN. Leslie Tolworthy, Miller Freeman Expositions, 1050 Commonwealth Ave, Boston, MA 02215. (617) 232-3976. May 21 to 23.

SEMICON/West, San Mateo, CA. SEMI, 805 E Middlefield Rd, Mountain View, CA 94043. (415) 940-6961. FAX (415) 967-5375. May 21 to 23.

Troubleshooting and Maintaining IBM & PS/2 (short course), St. Louis, MO. Center for Advanced Professional Development, 1820 E Garry St, Suite 110, Santa Ana, CA 92705. (714) 261-0240. May 22 to 23.

International Symposium on Computer Architecture, Toronto, ON, Canada. Prof Z G Vranesic, Dept of Electrical Engineering, University of Toronto, Toronto, ON, M5S 1A4, Canada. (416) 978-5032. May 26 to 30.

When it comes to affordable DSP, no one has it down like Analog Devices.

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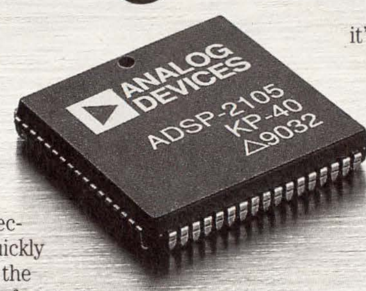

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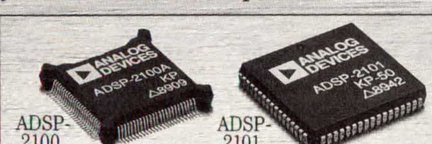

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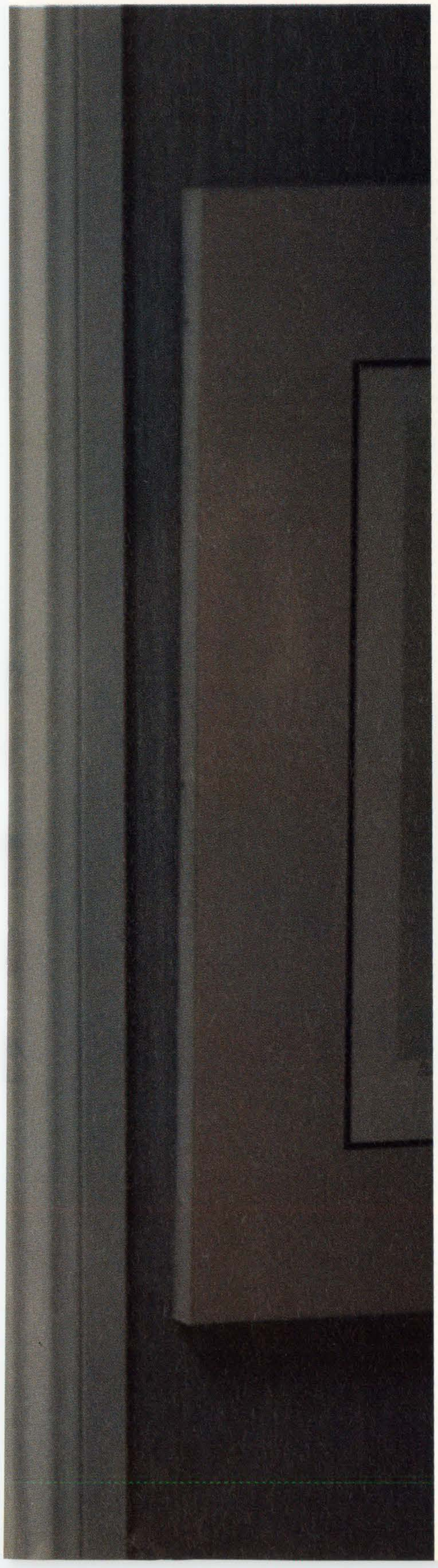

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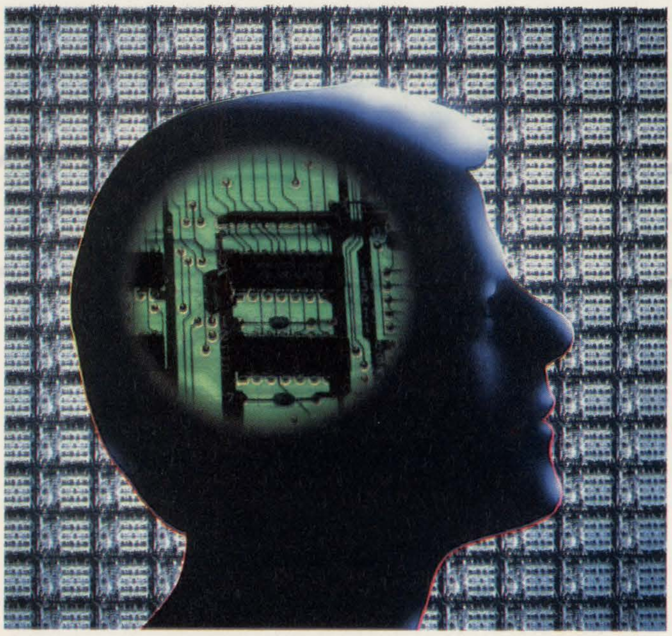

Instrument Specialties helps you integrate EMC into your designs... from the beginning.

Reduce interference problems and costs at their source: The initial design and material selection stage.

If you fail to consider potential EMI and RFI problems at the design stage, meeting FCC or foreign standards and your own performance requirements can become an expensive and time-consuming task. Often, it involves costly corrective shielding measures, complex design retrofits, and possibly compromised system performance.

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When a system exceeds restrictions, designers are often forced to trade efficiency for acceptable EMC performance—with undesirable results. As a finished design is modified to accommodate necessary remedial shielding measures, weight and volume inevitably increase, and overall efficiency drops.

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The three EMC design techniques.

Achieving EMC is largely a function of three control techniques: Suppression, Isolation, and Desensitization. Through a combination of these methods, undesirable signals (EMI/RFI) are suppressed at their origin...generating circuits are isolated...and susceptible circuits are desensitized. When applied from the beginning, these techniques help you create fully integrated designs that offer both optimum performance and the best possible production economies.

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After implementing proper circuit-design controls, the most significant EMC design technique to reduce interference and susceptibility is effective shielding.

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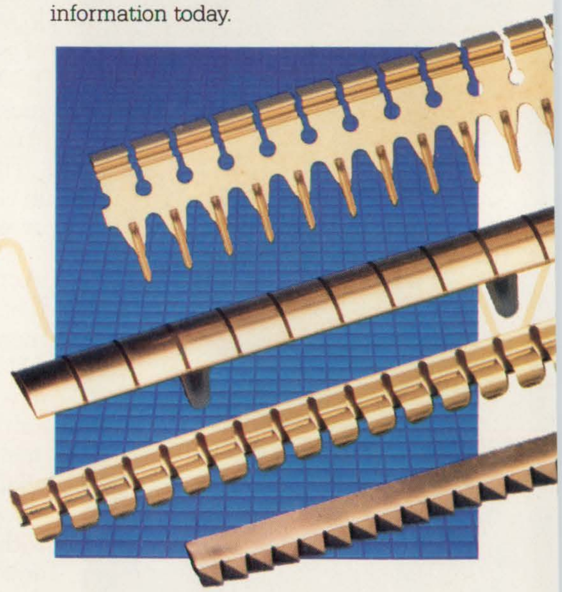

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National Semiconductor

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HOW NATIONAL SEMICONDUCTOR IS HELPING YOU PUSH THE LIMITS OF ADVANCED SYSTEMS PERFORMANCE.

Tom Redfern, National's Director of New Product Development, Interface/Peripherals Group, talks about the challenges of mixed analog+digital technology.

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"Traditional bus protocols are starting to hit the wall. They can't accommodate the wide data paths and high transfer rates demanded of the next generation of 32- and 64-bit microprocessors.

"That's why we've been an active participant on the IEEE's Futurebus+ committee since its founding in 1979. And that's why we invented the Backplane Transceiver Logic (BTL) that makes Futurebus+ a reality today.

"Our first Futurebus+ chipset contains five devices, and they employ some of the most advanced analog+digital integration ever achieved. Our BTL drivers, for example, let the digital CPU send information to the digital memory over the analog bus at peak rates of 2-3 Gbytes/second!

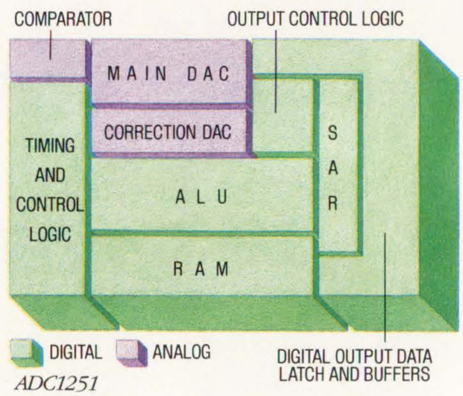
"This is the future—and we've got it today."

Setting the pace in system-level integration.

"Another great example is CLASIC, our powerful Custom Linear ASIC family.

"To reach system-on-chip performance, you've got to integrate analog and digital functions onto the same substrate.

"Well, CLASIC does that.



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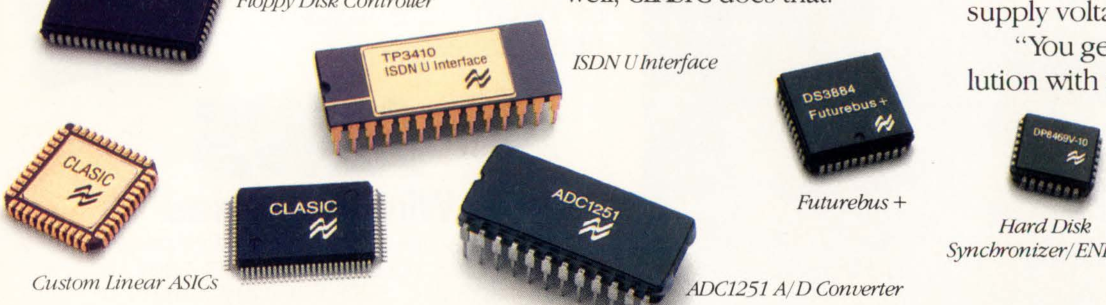

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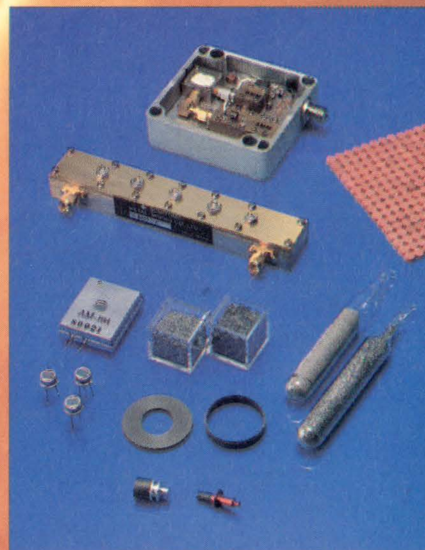

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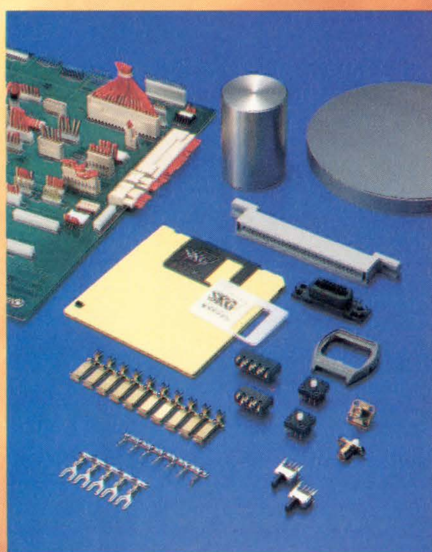

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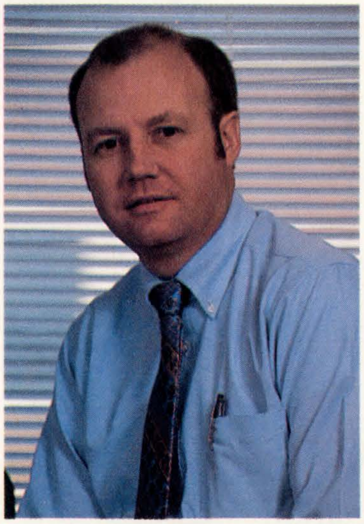
CIRCLE NO. 145

EDITORIAL

It's time for good news



Everyone knows that the US is in a recession. We are bombarded daily with the awful news—unemployment is up, sales are down, companies are retrenching, consumers aren't buying. Almost all of the economic and business reports tell of gloom and doom. Historically, though, the news is worst just before things turn around. Now is the time to look at the positive news and its effect on all of us.

The crazy pattern of borrowing and lending in the 1980s appears to have ended. Banks are more cautious about whom they lend money to, and with good reason. The companies that get credit are the ones unburdened with debt—the ones most likely to survive and to lead recovery. Interest and mortgage rates have also come down considerably in the last few months as the Federal Reserve loosens credit. More people are thinking about buying real estate. Here in New England, an area in which the real estate market has been badly depressed, some agents believe the devaluation of property is at an end.

Oil prices, which shot up at the start of the Middle East crisis, continue to drop and may go lower still if OPEC decides against strict limits on oil production. Cheaper energy and raw-material costs help spur a recovery. Now that the war is over and oil prices are dropping, people are showing signs of confidence that the recession will also end. Retail sales rebounded from −0.9% in January to 0.5% in February. In December, sales were −1.5%. The increase from month to month seems small, but combined with other signs shows a pattern of economic improvement. I'm not an economist, and I cannot make quantitative predictions. However, the fact that most of the economic news in a recent issue of *Business Week* was bad convinced me that we're ready for a steady recovery this year. Over the years I have noticed that when the business press convinces itself times are bad, the economy starts to pick up.

Here in the US there's a tendency to look at the worst and ignore the best. Recovery depends on you and me, and we can start by concentrating on the positives. People are still doing business in this country. Let's talk about it. Let's talk about the orders we are getting and why we got them. Let's be enthusiastic about the good people who work for us and concentrate on keeping them as valued employees. Let's promote ourselves as fair and reliable working partners. Let's trumpet the new technologies and products we're developing, and let's hail our breakthroughs and achievements. We've got a lot of good news to spread. I'm all ears.

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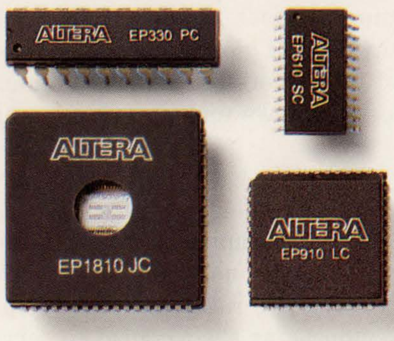

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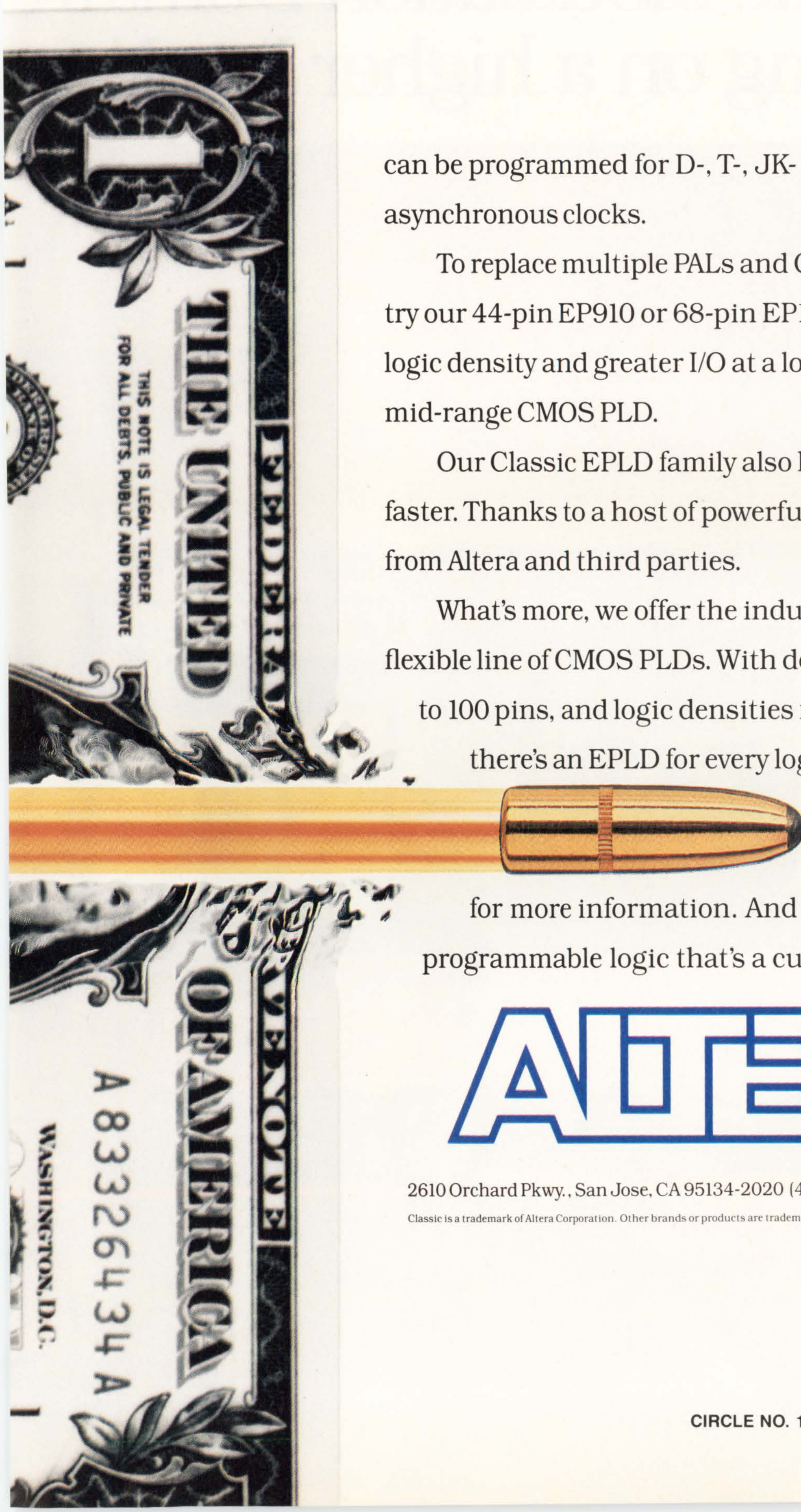

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CIRCLE NO. 146

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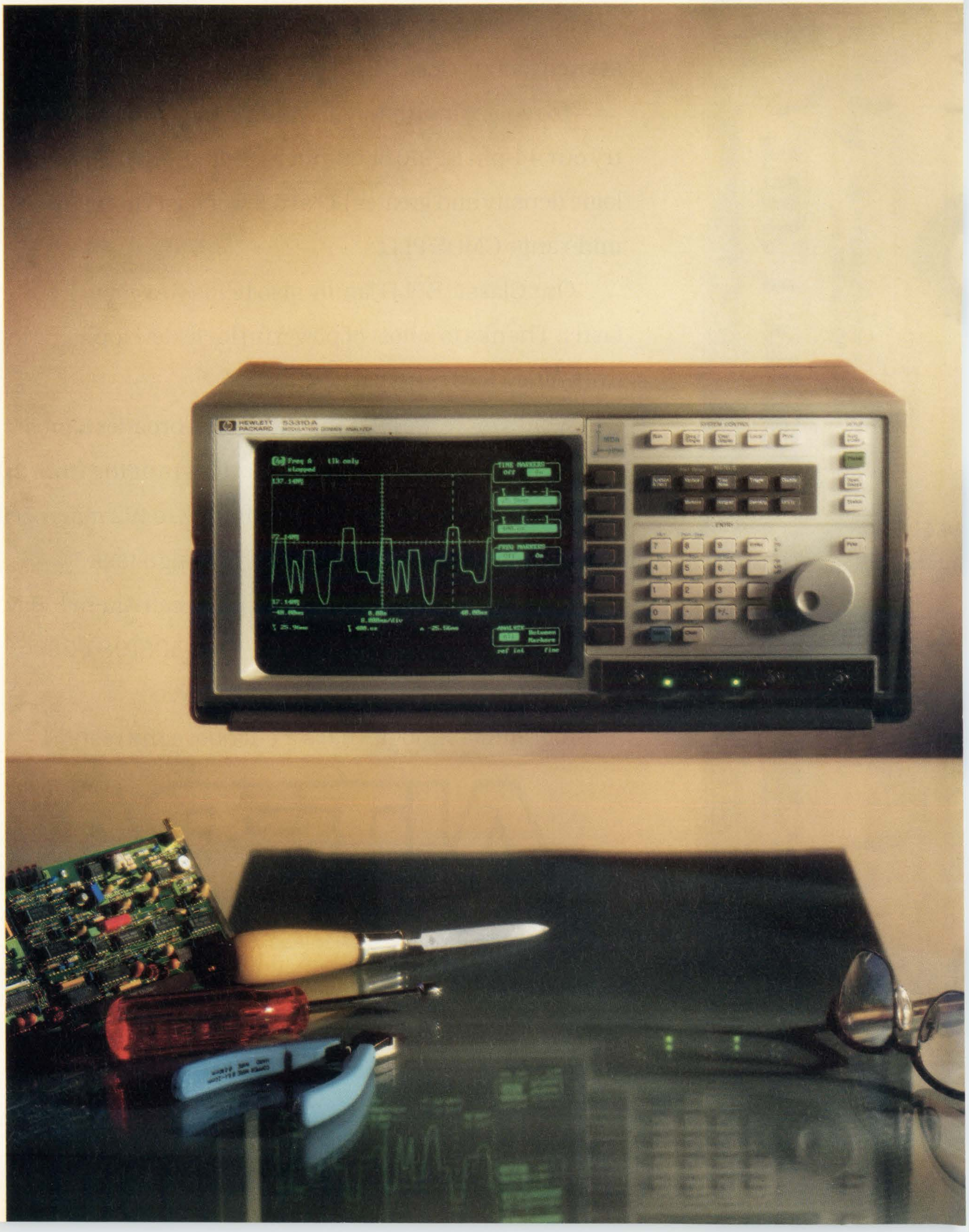

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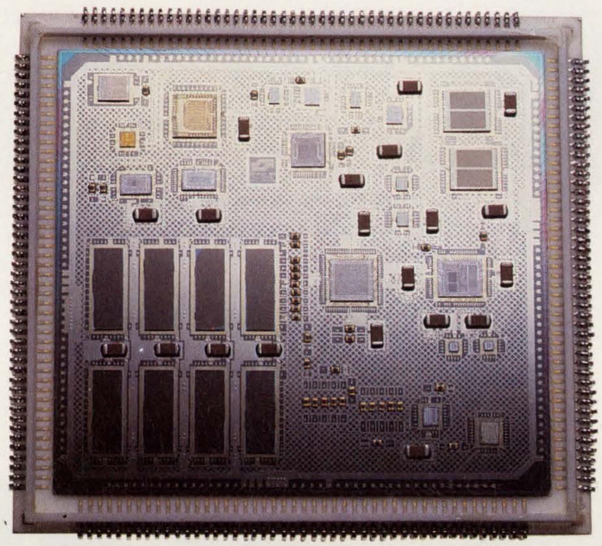

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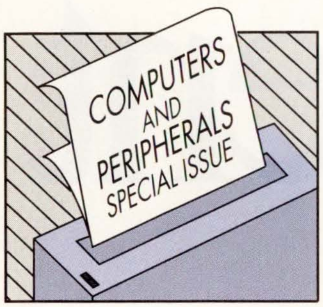
CIRCLE NO. 98

DIGITAL-PAPER STORAGE

Flexible optical media boost data density



If you need to store data by the terabyte, watch for digital paper. At one-half cent per megabyte, it may become the archival medium of the nineties.

Chris Terry, Associate Editor

"Digital paper" is a write-once optical data-storage material that provides prodigious advantages, including

- Far greater data density than any other medium
- Chemical stability that makes it immune to wide variations in ambient temperature and humidity
- An archival life of at least 15 years
- Extremely low cost to the user (one-half cent per megabyte).

The potential applications for digital-paper storage already number in the hundreds. The list of applications is starting to look more and more like a sci-fi description of a 22nd-century all-purpose material. So far, however, only two commercial manifestations have reached the production and marketing stages: write-once optical tape and small identification tags.

Digital paper's high data density goes hand-in-hand with its high data-transfer rate—you can search for any file within a 200M-byte space in less than 1 second.

The small tags can hold more than 1000 bits of information in a space less than one square centimeter and can be read from a considerable distance. Current uses for such tags include identifying machine-tool bits and providing instructions for their use. You can also use similar tags to hold positioning data; mechanisms that employ these tags can identify the position of a moving part with an accuracy of ± 1 μm relative to a previously established reference point.

The optical tape comes in two formats, one for 35-mm open-reel drives (1 terabyte per reel) and the other for half-inch IBM 3480-compatible cartridges (50G bytes per cartridge).

In addition, ICI Imagedata employed Bernoulli Optical Systems Corp (Boulder, CO) to perform a considerable amount of research and development work on Bernoulli-effect floppy-disk drives that employ digital paper as their storage medium. ICI Imagedata expects to license this technology to disk-drive manufacturers. If drive manufacturers fulfill ICI's expectations, we may see 2-in. floppy disks—that hold 100M bytes per side—within a year or two.

The name "digital paper" was coined by the developing company, ICI Imagedata, a Wilmington, DE-based subsidiary of the British chemical firm, Imperial Chemical Industries (ICI) Ltd. The name was intended to suggest that this data-storage medium could become a reliable electronic replacement for almost all archival paper and paper derivatives such as microfilm and microfiche. In practice, however, the name has proven highly confusing and misleading to potential users, who tend to associate the bulk, fragility, and erasability of wood-based paper with the name.

Al Conover, president and CEO of Lasertape Systems (which makes IBM 3480-compatible optical cartridge drives) prefers to call the material "digi-

tal optical tape" (DOT). His sales team finds that this name, by its similarity to the widely known DAT (digital audio tape), more forcibly suggests the high capacity and high performance inherent in the medium. Lasertape Systems has trademarked the new name and its abbreviation. However, they encourage any vendor of devices that employ the material to use both trademarked monikers (with suitable acknowledgement).

Physical characteristics

David Owen, development executive for storage products at ICI Imagedata, points out some of digital paper's technical advantages over other media. Some of these advantages hold good even in applications that currently use erasable rather than write-once optical media.

First, the high data density (200M bits/in.^{2}) makes the medium attractive for applications in which space is at a premium. The high data density goes hand-in-hand with a high data-transfer rate (currently 3M bytes/sec, potentially upgradable to 6M or even 12M bytes/sec) that allows fast searching—you can find any file within a 200M-byte space in less than 1 sec, and any file on a 50G-byte cartridge in less than 15 sec. For Creo's 1-terabyte open-reel drive, average access time is 28 sec, and worst-case access time is 60 sec.

Second, the flexibility of the medium makes it potentially usable in a startling variety of forms. You can cut the material into disks, strips, or tapes, as well as sheets, credit-cards, security badges, and odd-shaped identification tags.

Third, the chemical stability maintains data integrity. By contrast, when you cut magnetic recording web into tapes, it's not always possible to maintain a perfect seal at the cut edges; such sealing defects in metal-particle tapes can greatly reduce data life. Humidity can start corrosion at the outer edge of an unsealed tape, and this corrosion can spread inward toward the center of the tape.

Wear is not an academic issue

Al Conover adds several other advantages of optical tape over magnetic tape. Wear on the DOT, for example, is minimal, mainly because reading and writing do not require physical contact between the head and the tape. Furthermore, in Lasertape's drives the active layer is on the outside of the tape and does not come into contact with rollers and guides. A low-friction coating over the active layer improves the physical flow of the tape by helping to reduce binding between layers on a reel.

Of course, you don't have to worry about wear if you're using erasable or write-once magneto-thermal media or magnetic hard disks (unless a head crash occurs). But if you're using magnetic tape storage, tape wear is by no means an academic issue—it's a serious problem in industrial-strength applications. For example, video rental companies are finding that significant picture deterioration starts to appear after a video tape's tenth rental, and the tape becomes almost unviewable after 15 to 20 rentals. Playing the tape on a variety of old and inadequately maintained machines both abrades the recording surface with dirt and corrupts the picture data with residual magnetic fields that are never degaussed. If the recording were on DOT, however, this deterioration would be eliminated.

As yet there are no VCR drives that can use DOT, but such drives will become a necessity for HDTV. Current VHS tapes could hold only about ten minutes of HDTV material, whereas currently available 50G-byte DOT cartridges could hold about eight hours of HDTV material. These cartridges certainly have the bandwidth needed for video recording, and they would be extremely resistant to the deterioration of magnetic tapes experienced by rental companies today.

Table 1—Lasertape Systems' digital optical tape

Item	Value
Capacity	50G bytes
Transfer rate	3M bytes/sec
Average seek time	600 msec (200M bytes)
Average seek time	15 sec (50G bytes)
Bit error rate	$<10^{-12}$ (corrected)
Dimensions	19 × 8 in. rack mount
Interfaces	SCSI-1 and SCSI-2
	Fully 3480 plug compatible
Expansion	Autoloader for 10 cartridges
Prices	Drive: $25,000
	Autoloader: $1500

The economics are attractive

By now you may be saying, "Sounds wonderful, but why should I switch to a new medium? What's it going to cost me? What about my old drives? Isn't there a catch somewhere?" The answers to these questions will depend on how much data you need to store.

If you need only a few hundred megabytes, then digital paper won't do much for you. If you need to store as much as a terabyte (10^{12} bytes) of data at a time, then you're stuck with Creo's $225,000 35-mm optical tape recorder for the moment. Of course, if your application

Digital-paper storage

needs that much storage on a reel, the price shouldn't be any great shock to you.

But if you need to store tens or a few hundreds of gigabytes, look seriously at Lasertape Systems' DOT cartridge drives from three points of view: drive replacement costs; savings on media; and savings on the labor costs of mounting and dismounting magnetic cartridges.

There's no question that a DOT drive costs more ($25,000) than the corresponding IBM 3480 magnetic cartridge drive ($15,000 to $20,000). But this difference may turn out to be smaller than it seems. Consider that a DOT cartridge drive is little more than a standard IBM 3480 drive with an optical read/write head instead of a magnetic head. Falling prices of laser diodes and Bragg cells (a component of the scanner) are likely to make the price difference negligible within a year or two.

DOT cartridge drives require no changes to the operating system or file system because the DOT drives, like IBM 3480 drives, employ the SCSI interface. Furthermore, DOT cartridges follow the 3480 standard for writing data—no catalogs, merely a series of variable-length records.

You can save as much as $3500 in media costs each time you use a DOT cartridge rather than 3480 cartridges. A 200M-byte 3480 cartridge costs $5, whereas the DOT cartridge costs $250. But the DOT cartridge holds 50G bytes (250 times as much as the magnetic cartridge), so the cost per megabyte comes down from $0.025 to $0.005. If you completely fill your magnetic cartridges, one DOT cartridge will replace 250 3480 cartridges, and you'll save $1000 and about three cubic feet of storage space. However, most users don't fill every 3480 cartridge they store. So, one DOT cartridge may replace as many as 750 average 3480 cartridges—if you fill the DOT cartridge—saving you $3500 and about ten cubic feet of storage space.

Remember, too, that your application often may need to store large volumes of data without needing more than a few gigabytes on line. At these times, mounting and dismounting cartridges can become a labor-intensive—and hence, expensive—operation. Switching to DOT cartridges is likely to reduce the number of mounts and dismounts and therefore your running costs.

The banking industry is just one example of a high-volume user that needs to be able to access archived documents quickly. Banks capture images of checks digitally and then transfer the images to microfiche for archiving. The labor involved in transfer and storage is quite costly. Many such records are never looked at again, but when an image is required for verification, further considerable labor costs are entailed in retrieving it. Check-image storage could benefit from DOT technology.

Another banking application that could benefit is the overnight London-to-New York funds-transfer service. This service would like to log every transaction included in a transfer, but has found that present media do not have either the performance or the capacity to create such an on-the-fly log. Using standard data storage, transactions currently have to be recorded only upon reaching their final destinations. DOT has both the capacity and the performance needed to create a complete log either at London or at the New York center where transactions are regrouped geographically for retransmission to the destination banks.

Likewise, many sites that handle medical records already have as many as 1 million IBM 3480 cartridges (200M bytes each), and the number is increasing daily. That makes for much mounting and handling. A switch to DOT could greatly reduce both media and handling costs at these sites.

What makes a DOT system inexpensive to purchase and run is that it's an extension of well-understood 3840 technology. The substrate of DOT is identical to that of 3840 magnetic tape (see **box**, "How digital optical tape works"). In fact, except that optical cartridges are built to slightly tighter mechanical specs than magnetic cartridges, a standard 3480 drive has no way of telling whether magnetic or optical tape is loaded. In building their optical subsystems, Lasertape Systems could retrofit an optical head (which has no moving parts) to any IBM 3480-compatible drive.

Compatibility with the 3480 extends to the device interface. Effectively, the operating system (OS) uses a magnetic cartridge as a write-once medium; there are no catalogs or directories on the tape, and you cannot perform the record

Text continued on pg 85

Table 2—Creo Products' 1003 optical tape recorder

Item	Value
Capacity	1T byte/880m reel
Transfer rate	3M bytes/sec (sustained maximum)
Seek time	Average random record, 28 sec 60 sec max
Bit error rate	10^{-12} (corrected)
Dimensions	24 x 29 x 77 in. (19-in. rack)
Interfaces	SCSI and serial
Price	$225,000

How digital optical tape works

Digital optical tape (DOT), also known as digital paper, consists of four basic layers **(Fig A)**:

- a substrate of Melinex polyester,
- a metallic reflecting layer,
- a dye-containing polymer layer,
- a protective overcoat.

It's worth noting here that the DOT substrate material is the same as the substrate material of the magnetic tape used in IBM 3480 cartridges. Hence, manufacturers can produce DOT tape using many of the standard methods. Not needing significantly altered production methods, DOT media costs shouldn't adversely affect the cost of DOT systems.

Writing to DOT

To write data to the DOT, the system turns a laser beam on or off. Unlike the ablative techniques of WORM drives, which burn holes in the metallic reflector, the DOT pyroplastic technique merely deforms the dye-polymer layer, producing a pit **(Fig B)**. Because the dye-polymer layer is a very poor conductor of heat, the heat produced by the laser beam does not spread nearly as rapidly as it does when burning a WORM reflector layer, which is highly conductive. Thus, the heating effect of the laser is confined to a very small area of the DOT active layer.

As a result, the pits can be as small as 1 micron in diameter and have very sharp edges. Spacing between longitudinal tracks can be as small as 1.6 microns. The small pits with their steep edges produce very sharp transitions between pit and no-pit conditions and permit data to be written and read at rates as high as 3M bytes/sec. Conventional ablative WORM techniques cannot support such high data-transfer rates. In a WORM disk, losses due to absorption and scattering of the laser beam produce pits whose edges slope more gradually than those of a DOT system.

Reading from DOT

A DOT drive reads data from the tape by means of a low-power laser beam that cannot deform the active layer but can detect the presence or absence of a pit. In the absence of a pit, the distance between the top surface of the active layer and the bottom surface adjacent to the metallic reflector is a whole number of half wavelengths of the laser light. Thus, reflections from the top and bottom surfaces of the active layer reinforce each other. When the beam encounters a pit, however, the distance between top and bottom surfaces of the active layer is not a whole number of half wavelengths, so the reflected rays partially or completely cancel each other **(Fig B)**.

The optical head

Lasertape Systems Inc and Creo Products Inc have taken different approaches to creating multiple tracks. Lasertape Systems, in the interests of robust miniaturization, uses a purely electronic scanner; the creation of 40 tracks on a 3480-compatible optical cartridge does not require any physical movement

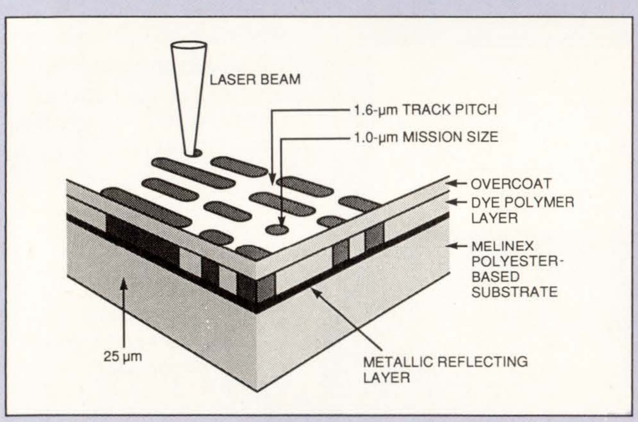


Fig A—Digital paper, or digital optical tape (DOT), has four layers. *The heat of the write laser creates pits in the active dye-polymer layer.*

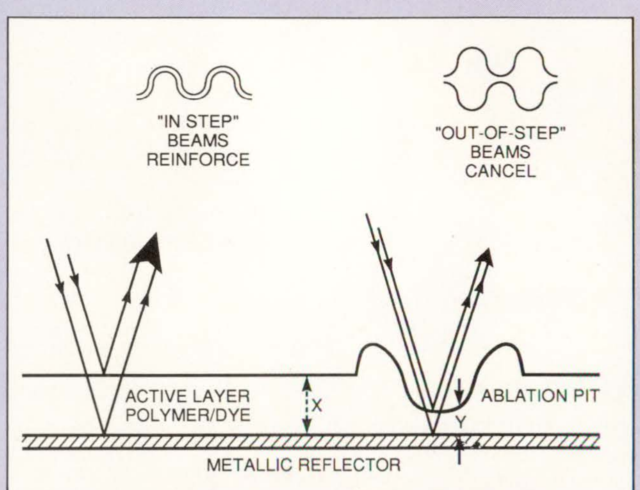


Fig B—Interference effects allow the system to detect pits *or the absence of pits as the read laser passes over the material.*

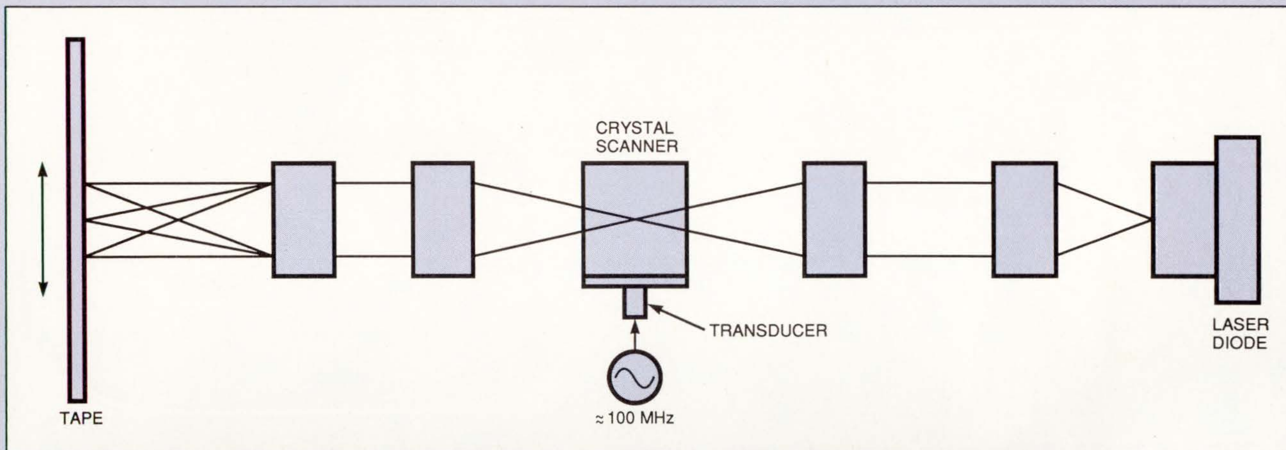


Fig C—A DOT tape scanner has no moving parts; the angle at which the beam emerges from the crystal depends on the radio frequency applied to the crystal via a transducer.

of the head. Instead, Lasertape's method shifts the laser beam by passing it through a crystal to which they have attached a transducer (**Fig C**). Applying a radio frequency of approximately 100 MHz to the transducer creates a supersonic flexing action in the crystal. The angle at which the laser beam emerges from the crystal varies with the precise frequency you apply to the transducer. This type of scanner is small enough to allow an optical head to be retrofitted to a standard 3480 drive. The drive records one track at a time in alternate directions for a total capacity of 50G bytes.

Creo did not have to contend with such rigid size constraints, and therefore adopted the scheme shown in **Fig D**. An array of laser diodes (one for each of the 32 tracks on the tape) send their beams into a collimator. The collimated beam is then positioned and focused on the tape track to be used. A slide running in an air bearing performs the positioning; a lens focuses the collimated beam. The optical encoder of the positioning mechanism turns on the appropriate diode in the laser-diode array. The slide also directs the reflected beam to the sensor associated with the current track. Again, there are 32 sensors in the sensor array (not shown in the diagram). The system writes 32 bits across the tape in one direction, then steps the tape and writes 32 bits in the other direction. Each physical record is 32 bits wide by 20,000 bits long, for a total of 80k bytes. An 880-meter reel of tape has a total capacity of 1 terabyte (1000 gigabytes).

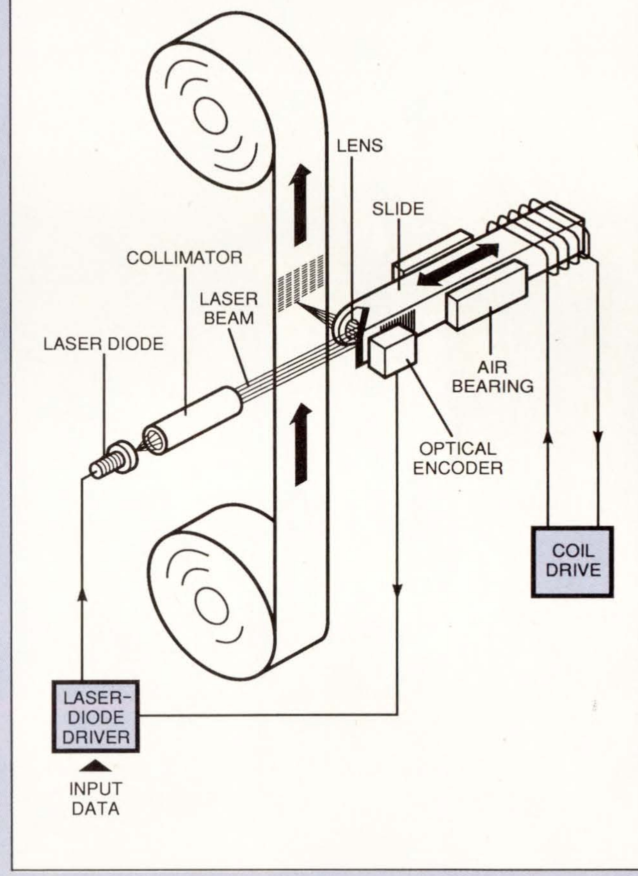


Fig D—Creo's optical tape drive writes 32 bits across the tape in one direction, then steps the tape and writes 32 bits across the tape in the other direction.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Digital-paper storage

updates or random data replacement that characterize magnetic or erasable-optical disks. You erase everything in the cartridge only when all of that data can be discarded or has already been moved to some other medium. The OS expects to write and read only a series of variable-length records, using tracks in alternate directions. DOT systems fulfill all of these expectations. The only differences the OS must take into account are that each track of a DOT holds far more data, and a DOT has 40 tracks instead of the 18 of a standard magnetic cartridge.

A DOT cartridge is potentially erasable and reusable, although nobody has implemented the careful reheating that would be needed to remove the pyroplastic deformations (pits) from the dye-polymer layer.

Large-volume techniques

The Creo open-reel DOT recorder can store 1 terabyte (1000 gigabytes) on a 12-in. reel of 35-mm tape, which satisfies the requirements of most satellite data-logging applications.

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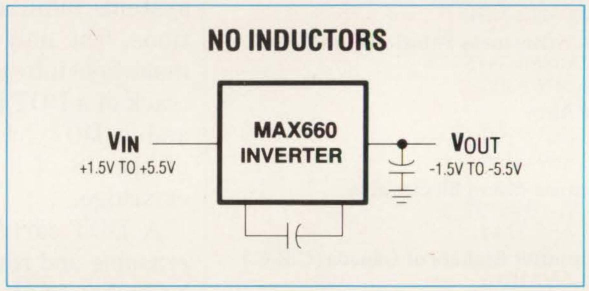

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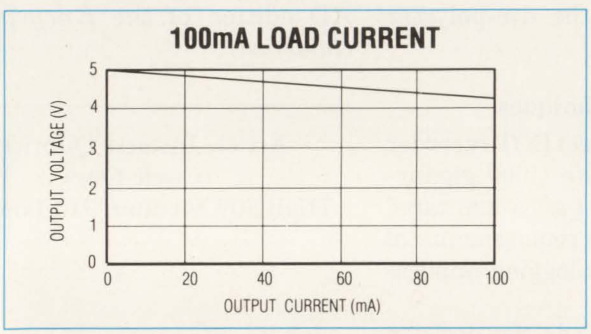

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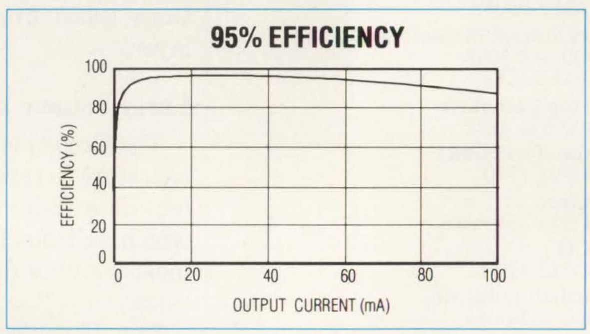

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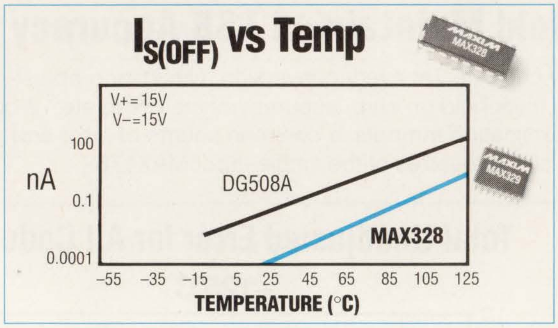

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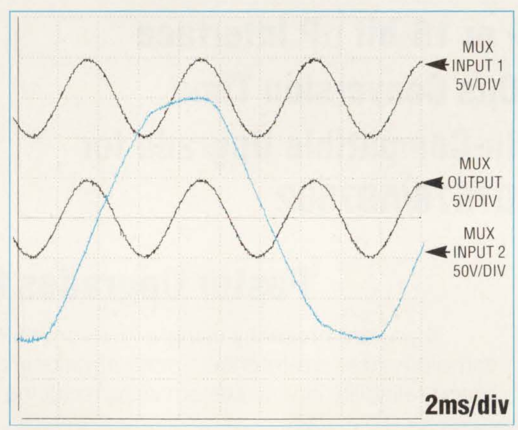

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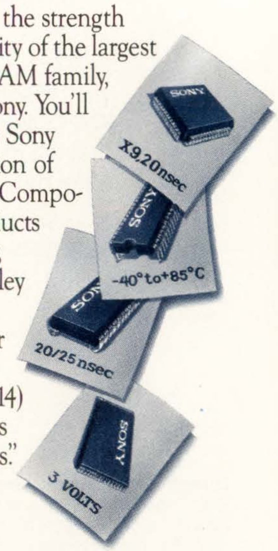
	CXK581000M	100/120/150	SOP 525mil	L/LL	B/X	Now
	CXK581100TM	100/120/150	TSOP	L/LL	B/X	Now
	CXK581100YM	100/120/150	TSOP (reverse)	L/LL	B/X	Now
	CXK581001P	70/85	DIP 600mil	L/LL		Now
	CXK581001M	70/85	SOP 525mil	L/LL		Now
	CXK581020SP	35/45/55	SDIP 400mil			Now
	CXK581020J	35/45/55	SOJ 400mil			Now
128Kx9	CXK77910J	20	SOJ 400mil		Sync ASM	2H '91
256Kx4	CXK541000J	25/30/35	SOJ 400mil			2H '91

L = Low LL = Low, Low B = 3 Volt X = Extended Temperature



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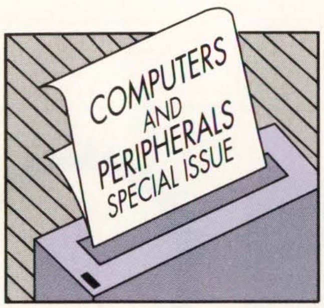
THE IEEE-488.2 STANDARD

IEEE-488.2 products are just now appearing



Long on promise, short on delivery, the IEEE-488.2 standard may one day reduce the work of writing test-system programs. But that day hasn't arrived just yet.

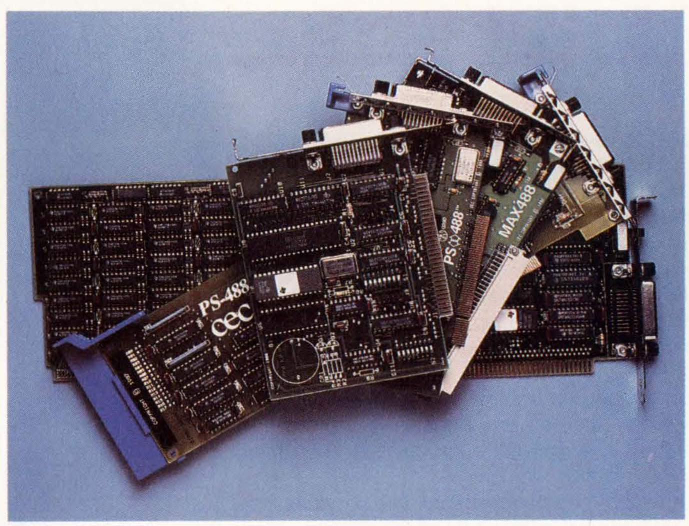
Steven H Leibson,
Senior Regional Editor

When first adopted in 1975, the IEEE-488 (GPIB) standard brought order to the chaotic instrumentation world. Prior to this standard's appearance, an army of incompatible instrument-interface schemes made test-system design a nightmare.

The present roster lists thousands of instruments and instruments with GPIB ports. This adherence to the standard aids the assembly of "rack-and-stack" instrumentation systems, but the unique command sets, syntax requirements, and data structures employed by the many products still give test-system programmers headaches. The IEEE-488.2 standard, adopted in 1987, attempts to resolve many of the remaining problems. Products designed before this standard arrived obviously don't offer its capabilities, but newer products that do have IEEE-488.2 features give you a taste of the future.

First, you should understand that the IEEE-488.2 standard augments the original IEEE-488 spec and does not replace it. To signify the coexistent nature of the two specs, the IEEE changed the number of the original standard to IEEE 488.1. That standard specified the electrical and mechanical characteristics of the interface. It also introduced the concept of talkers, listeners, and controllers. Talkers place data on the bus; listeners consume that data; and controllers assign the roles of talker and listener to the instruments connected to the bus. One IEEE-488 bus accommodates as many as 15 devices.

The IEEE-488 standard also specified the byte-level handshake mechanism and defined the bus-control mechanisms. In the interest of maximizing flexibility, the standard's creators intentionally did not specify message protocols and loosely stipulated that data be transmitted using any "standard" alphanumeric, binary, or BCD code. The IEEE-488 spec did not further define what these standard codes might be. In addition, the creators loosely defined the IEEE-488 standard's method for polling the status of an instrument requesting service over the bus.



Many computers can control IEEE-488.2 systems *using the controller boards now available, such as this group from Capital Equipment Corp.*

The IEEE-488.2 standard

The flexibility permitted by the original IEEE-488 standard did indeed encourage innovative instrument design. In fact, vendors innovated in nearly every direction. Although all of the resulting products communicated over the IEEE-488 bus, every instrument seemed to speak a different dialect. The resulting cacophony created the test engineer's equivalent of the Tower of Babel. Engineers producing test programs had to employ different software handlers for each new instrument. Thus, the original IEEE-488 standard made the job of physically connecting instruments to controllers much easier but did little to ease test-system software development.

After ten years of rampant innovation, several vendors collaborated to add more consistency to IEEE-488 bus usage by developing additional standards. Their work culminated in the IEEE-488.2 spec, which the IEEE adopted in 1987. The IEEE-488.2 standard specifies codes, data formats, message protocols, and common commands to address some of the software-related problems encountered by users of diverse products incorporating the IEEE-488 bus.

The new standard also requires the complying product to have a minimum set of capabilities, including the ability to both talk and listen. The standard adds rigor to the design of complying equipment but does not require vendors to adopt the IEEE-488.2 specification; they can continue to use just the IEEE-488.1 spec.

One of the key components of the IEEE-488.2 standard deals with the possibility that instruments conforming only to IEEE-488.1 might be mixed with IEEE-488.2-compliant equipment on one bus. The IEEE-488.2 spec introduces the ideas of "precise talking" and "forgiving listening" to accommodate such mixed systems.

Talk precisely

Precise talking restricts the way an IEEE-488.2-compliant instrument can generate messages. For example, a data message containing a reading expressed as a floating-point number must always be transmitted as a floating-point number, not as another number type. Thus a 1V floating-point reading may be sent as the string "+1.000E+0" or "+1.0E+0" but not as "1" which is an integer or "1.0" which is a fixed-point value. Precise talking simplifies test software because your program need only accept floating-point numbers if that is all it expects. However, you must remember that equipment conforming only to the older spec may generate messages in any format. If you are working with a mix of old and new instruments, you must still write smarter code to cover all cases.

Forgiving listening is the opposite of precise talking. A piece of IEEE-488.2-compliant equipment must accept messages in any legal numeric format. A forgiving listener will accept and correctly evaluate a 1V reading expressed as "1" (an integer), "1.00" (a fixed-point value), or "+1.00E+0" (a floating-point number). This requirement excuses you from having to precisely format commands you send to IEEE-488.2-compliant equipment. Once again however, you'll need to be more careful when writing programs for mixtures of old and new equipment. Older listeners aren't always so forgiving.

In conjunction with forgiving listening and precise talking, the IEEE-488.2 standard specifies several message formats. Text messages use the 7-bit ASCII code, binary blocks are sent most-significant byte first, and binary floating-point numbers employ the IEEE-754-1985 standard format. The IEEE-488.2 standard also contains

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Table 1—IEEE-488.2 common commands

Command group	Command mnemonic	Description	Required or optional
Auto configure	*AAD	Assign address	Optional
	*DLF	Disable listener function	Optional
System data	*IDN?	Identification query	Required
	*OPT?	Option-identification query	Optional
	*PUD	Protected user data	Optional
	*PUD?	Protected user-data query	Optional
	*RDT	Resource description transfer	Optional
	*RDT?	Resource-description transfer query	Optional
Internal operation	*CAL?	Calibration query	Optional
	*LRN?	Learn device-setup query	Optional
	*RST	Reset	Required
	*TST?	Self-test query	Required
Synchronization	*OPC	Operation complete	Required
	*OPC?	Operation-complete query	Required
	*WAI	Wait to complete	Required
Macro commands	*DMC	Define macro	Optional
	*EMC	Enable macro	Optional
	*EMC?	Enable-macro query	Optional
	*GMC?	Get-macro-contents query	Optional
	*LMC?	Learn-macro query	Optional
	*PMC	Purge macros	Optional
Parallel poll	*IST?	Individual-status query	Required with parallel-poll capability
	*PRE	Parallel-poll enable register	Required with parallel-poll capability
	*PRE?	Parallel-poll enable-register query	Required with parallel-poll capability
Status and event	*CLS	Clear status	Required
	*ESE	Event-status enable	Required
	*ESE?	Event-status enable query	Required
	*ESR?	Event-status register query	Required
	*PSC	Power-on status clear	Optional
	*PSC?	Power-on status-clear query	Optional
	*SRE	Service request enable	Required
	*SRE?	Service-request enable query	Required
	*STB?	Read status-byte query	Required
Device trigger	*DDT	Define device trigger	Optional
	*DDT?	Define device-trigger query	Optional
	*TRG	Trigger	Required with device-trigger capability
Controller	*PCB	Pass control back	Required with system-controller capability
Stored settings	*RCL	Recall instrument state	Optional
	*SAV	Save instrument state	Optional

precise definitions for integers, fixed-point numbers, and floating-point numbers expressed as ASCII strings.

Common commands unify

The IEEE-488.2 standard's designers also provided more ways to exert control over equipment on the bus through a set of common commands. Some of these commands are required in all devices, some are optional, and some are required only if the device has certain features such as the ability to respond to a parallel poll on the bus. All of the common commands must start with an asterisk, whereas the standard forbids device-dependent commands to use an asterisk as the leading character. A list of these common commands appears in **Table 1.**

The common commands do not control measurements. Instead, they manage the operation of an instrument. Internal-operation commands standardize the way you instruct an instrument to perform a calibration cycle, execute a self-test program, reset to a known state, or learn a setup. Synchronization commands allow you to control the sequence of operations in an instrument. Device-trigger commands define a sequence of events that will occur when the instrument receives an IEEE-488.1 group-execute-trigger (GET) command. (The GET command is a way to activate several instruments simultaneously.)

An optional autoconfigure command group allows a controller to detect instruments on the bus and assign them a bus address. Currently, most IEEE-488 equipment employs DIP switches on a back panel to set this address. Using the autoconfigure commands, a system can theoretically configure itself when powered up and can automatically adapt to newly added equipment. Because the autoconfigure feature is optional, and because you can mix IEEE-488.2-compliant and older equipment on the same bus, you may find this new feature somewhat useless now. It does, however, seem to have a useful future.

Standardizing requests

The IEEE-488.2 standard's status and event commands give a test program far more control over an instrument's use of the IEEE-488 bus' service request (SRQ). The SRQ line allows an instrument to request service over the bus asynchronously. The SRQ is the IEEE-488 bus' interrupt. Many existing instruments allow the system programmer to define events that may cause such an interrupt, but IEEE-488.1 doesn't specify how. Consequently, use of the IEEE-488.1 standard's service request varies from instrument to instrument. The IEEE-488.2 standard specifies an extended-status model and the status-and-event command group that at least make an attempt to

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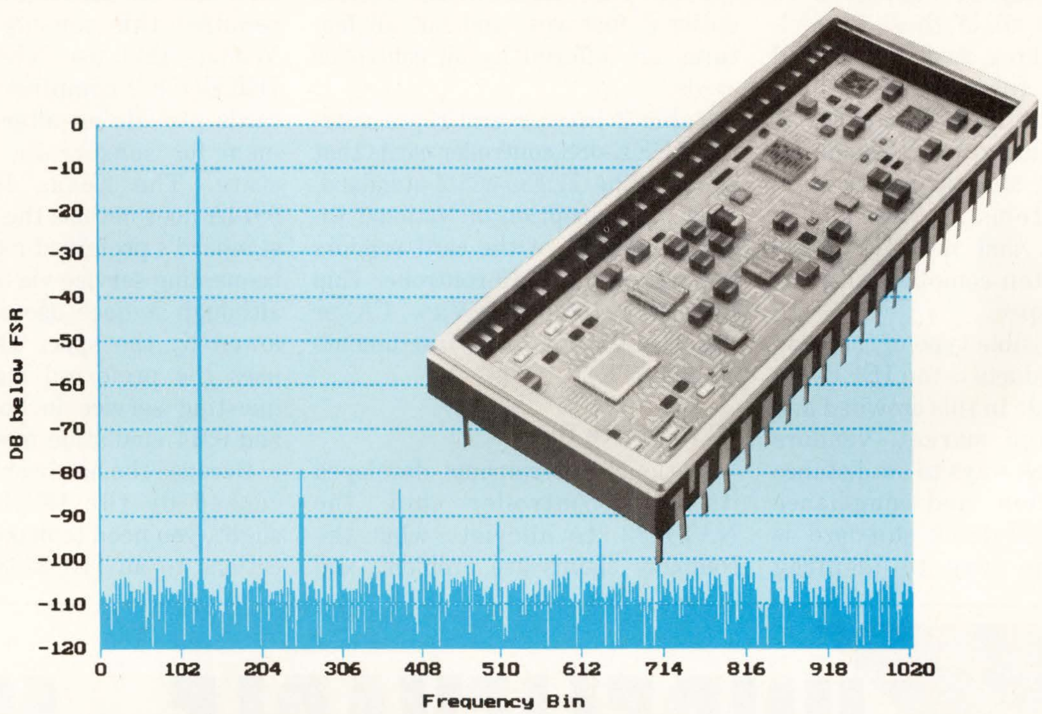

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The ADC-00145 uses a two-step A/D conversion algorithm. The application of a pulse to the Encode Command pin initiates the conversion cycle. The track/hold samples and stores the analog input, then a flash ADC generates a coarse encode of the sampled voltage and stores its 8 bits in the MSB register. At the same time a high-speed DAC and amplifier converts the 8 bits to an analog voltage, and subtracts it from the original input. Next, the flash ADC generates a fine encode of the subtracted voltage and stores these 8 bits in the LSB register. Digital error correction combines coarse and fine data to yield a 14-bit output. This process is repeatable at a 5MHz rate.

Many factors contributed to achieving the ADC-00145's technical breakthroughs in speed, size, and power. Foremost among them were the high-speed T/H, DAC, and the gain amplifier; all are DDC proprietary designs and single custom monolithics. In addition, judicious use of thin- and thick-film hybrid technology resulted in minimum layout area.

With its high speed, small package, and wide operating temperature range, the ADC-00145 is ideal for the most demanding military and industrial data conversion applications. Typical applications are radar, infrared, and sonar digitizing, medical and nuclear instrumentation, and high-speed data-acquisition systems.

For additional information contact Mike Johnson (1-800-DDC-1772) ext 384. ❑

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The IEEE-488.2 standard

standardize this capability. For detailed information regarding the IEEE-488.2 standard's status mechanisms **(Ref 1).**

You may not be surprised to discover that all of these marvelous new features have not caused a stampede. Instrument vendors have shown an understandable reluctance to change the designs of products that already workwell in existing systems. Nevertheless, you will find that new IEEE-488 equipment often complies with the IEEE-488.2 spec.

The most visible type of the new, compliant products is the IEEE-488 controller card. In this crowded and hotly-contested market, vendors constantly seek ways to outdistance the competition, and compliance with the IEEE-488.2 standard is certainly one way to leapfrog ahead. However, you must scrutinize a controller card's conformance with the IEEE-488.2 spec because you may not be getting all that you expect. The standard lists several optional features, and not all features are offered by all controller cards.

Table 2 lists several representative IEEE-488 controller cards that support the IEEE-488.2 standard. With the exception of National Instruments, all of the card vendors use either the 7210 controller chip from NEC (Mountain View, CA) or the 9914A from Texas Instruments (Dallas, TX).

IC remedies flaws

National Instruments developed its own controller chip, the NAT4882, to alleviate what the company claims are problems and deficiencies with the other controller ICs. The one clear deficiency of NEC's 7210 is that it provides no way to sense the state of the SRQ line, and the IEEE-488.2 standard requires this sensing capability. Vendors that use NEC's 7210 for IEEE-488.2-compliant controller cards provide an alternate mechanism for sensing the SRQ line's state. The Texas Instruments 9914A does not use the IEEE-488.2 standard's preferred mechanism for requesting service via the SRQ line, although it does use a method allowed by the spec. The NAT4882 uses the preferred method of requesting service in both the 7210 and 9914 emulation modes.

Because the hardware differences caused by the IEEE-488.2 are slight, you need to make few modifications to an IEEE-488 controller card to achieve compliance. To create compliant products, vendors have altered the software for these controller cards, but the changes are largely invisible. If you look at data sheets for the controller cards listed in **Table 2**, you'll find few specific software features that support the IEEE-488.2 requirements. Again, that's because the IEEE-488.2 spec augments and fills in the details of the IEEE-488.1 standard instead of replacing it.

The biggest changes made by the IEEE-488.2 standard occur in the test-equipment firmware and test-system software. The common commands added by the IEEE-488.2 standard are just text strings sent using mechanisms established in the IEEE-488.1 standard. Further, the extended status- and event-reporting model created by the IEEE-488.2 spec is controlled and interrogated using these common command strings. Consequently, the changes made to the controller-board software are largely invisible.

Software hasn't changed

This transparency allows you to use existing software for test-system program development. For example, TransEra claims that its HT Basic language packages need no changes to be compatible with the IEEE-488.2 spec. The company's language products run on DOS-based PCs and include I/O drivers for most of the IEEE-488 controller cards listed in **Table 2.**

HT Basic emulates HP Basic (formerly called Rocky Mountain Basic). Hewlett-Packard supplies HP Basic with its 82300C and 82324A Measurement Coprocessor boards. HT Basic runs on the PC's processor and costs \$625 to \$925. HP Basic runs on the 68000-family μP residing on the Measurement Coprocessor board and is part of the product. Like TransEra, Hewlett-Packard says it has made no changes to HP Basic relating to the IEEE-488.2 standard.

You'll find most of the changes wrought by the IEEE-488.2 standard in the newest test equipment. For example, Hewlett-Packard's \$11,300 1652B logic analyzer, introduced in 1990, complies with the IEEE-488.2 specifications. The product combines a 100-MHz, 80-channel logic analyzer with a 400M-samples/sec, 2-channel digital sampling oscilloscope. As an instrument with a large number of functions and capabilities, the 1652B makes

Table 2—Representative controller cards for IEEE-488.2 systems

Manufacturer	Product	Host Bus	Maximum transfer rate (bytes/sec) (See Note)	IEEE-488 software interface	Price	Comments
Capital Equipment Corp	Max488	Apple Macintosh II	>650,000	Language extensions and subroutines for Quickbasic, Turbo Pascal, C, and Hypertalk	$450	Package includes Hypercard interactive test stack.
	PC<>488	IBM PC	350,000	DOS device driver and language extensions for Basic, Quickbasic, Turbo Pascal, C, and Fortran	$450	Package includes interactive test program, printer/plotter redirector.
	PS<>488	IBM Microchannel (short card, fits IBM P70)	320,000	DOS device driver and language extensions for Basic, Quickbasic, Turbo Pascal, C, and Fortran	$450	Package includes interactive test program, printer/plotter redirector.
Hewlett-Packard Co	82300C	IBM PC/AT	110,000	HP Basic	$1695	Software runs on an on-board 68000 auxiliary processor.
	82324A	IBM PC/AT	350,000	HP Basic	$2795	Software runs on an on-board 68030 auxiliary processor.
	82335A	IBM PC/AT	205,000	Command libraries for Vectra Basic, GW Basic, Quickbasic, Compiled Basic, Pascal, C, Quick C, Turbo C, and Turbo C++	$525	Package includes printer/plotter redirector.
Iotech	Personal 488plus	IBM PC/AT	300,000	DOS device driver and subroutines for Basic, C, and Pascal	$395	
	Personal 488/2plus	IBM Microchannel	300,000	DOS device driver and subroutines for Basic, C, and Pascal	$495	
	Power 488	IBM PC/AT	1,000,000	DOS device driver and subroutines for Basic, C, and Pascal	$495	Board has a 40-line digital I/O port.
	Power 488CT	IBM PC/AT	1,000,000	DOS device driver, subroutines for Basic, C, and Pascal	$595	Board has a 40-line digital I/O port and five 16-bit timers.
National Instruments	GD-GPIB	Grid System 1500	400,000	DOS device driver or Microsoft Windows dynamic-link library. Interfaces for several programming languages also offered.	$695	Package includes interactive bus-control program.
	GPIB-PCII/IIA	IBM PC	>400,000	DOS device driver or Microsoft Windows dynamic-link library. Interfaces for several programming languages also offered.	$395	Package includes interactive bus-control program.
	GPIB-SE/30	Apple Macintosh SE/30	1,000,000	Device manager calls and interfaces for Quickbasic, Think C, MPW C, and Hypertalk	$495	Package includes interactive bus-control program.
	GPIB-SPARC1-B	Sun Sbus	1,000,000	Multitasking software driver	$995	Package includes interactive bus-control program.
	GPIB-98 Turbo	NEC PC-9801	1,000,000	DOS device driver or Microsoft Windows dynamic-link library. Interfaces for several programming languages also offered	¥ 117,000	
	LC-GPIB	Apple Macintosh LC	1,000,000	Device manager calls and interfaces for Quickbasic, Think C, MPW C, and Hypertalk	$495	Available with 68882 floating-point unit for $745.
	MC-GPIB	IBM Microchannel	1,000,000	DOS device driver, Microsoft Windows dynamic-link library, OS/2 driver, Unix driver. Interfaces for several programming languages also offered.	$495	Package includes interactive bus-control program.
	NB-GPIB	Apple Macintosh II	800,000	Device manager calls and interfaces for Quickbasic, Think C, MPW C, and Hypertalk	$495	
	VXIpc-030	VXI	1,000,000	Device manager calls and interfaces for Quickbasic, Think C, MPW C, and Hypertalk	$14,800	An Apple Macintosh SE/30 on a VXI card with an IEEE-488 interface port.
	VXIpc-386	VXI	1,000,000	DOS device driver	$9000	An 80386-based PC on a VXI card with an IEEE-488 interface port.

Note: Actual transfer rates depend more on the host bus and the software than the interface card. The absolute maximum transfer rate over the IEEE-488 bus is 1M bytes/sec. Actual performance can be less than the maximum.

The IEEE-488.2 standard

a good candidate for the IEEE-488.2 standard's abilities. The 1652B's status register follows the standard's guidelines and it understands the required common commands.

If you need to create IEEE-488.2 test systems, you'll be happy to know the necessary controller boards and software already exist. As time passes, the growing number of instruments that comply with the IEEE-488.2 spec will allow your test programs to become somewhat less complex. When all the instruments in your system understand the IEEE-488.2 common commands, you will be able to create standard routines to manage much of the test-system's overhead. However, until you can equip an entire system with IEEE-488.2-compliant instruments, your programming job really won't be any easier than it has been. Even one exception to the IEEE-488.2 rules forces you to create unique software for the nonconforming instrument. EDN

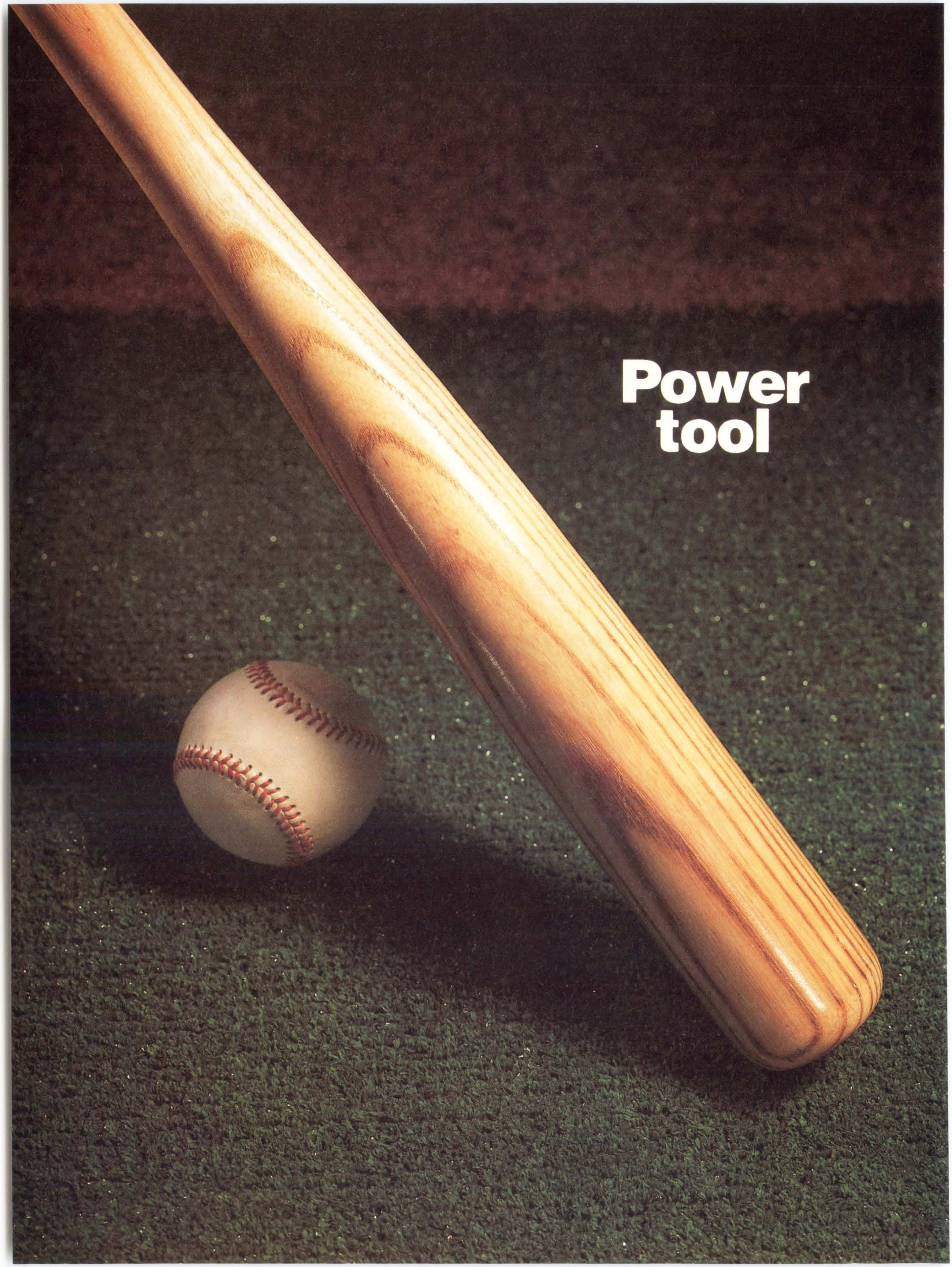
Reference

1. *Tutorial Description of the Hewlett-Packard Interface Bus*, Part No. 5021-1927, Hewlett-Packard Co, Palo Alto, CA, November, 1987.

Article Interest Quotient
(Circle One)
High 515 Medium 516 Low 517

WHAT'S NEXT

Look for EDN Magazine's Analog Technology Special Issue on May 9, 1991. Among other analog-related stories, the issue will include a staff-written Special Report on single-supply, analog-design techniques and a Technology Update on switching regulator ICs. Look for coverage of other topics and regular departments, too.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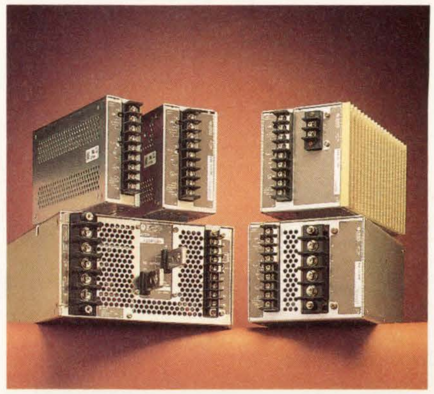

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- ☐ Tested to MIL STD 810D
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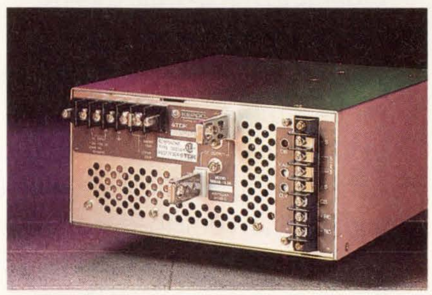

ac to dc power single output 600W

- ☐ 2V-48V dc output
- ☐ jumper selectable inputs: 85-132 or 170-264V ac, 240-370V dc
- ☐ fully enclosed
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- ☐ Tested to MIL STD 810D

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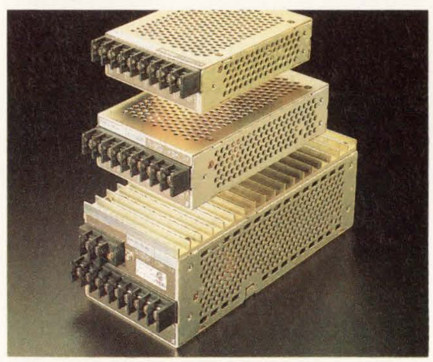
Power tools



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- ☐ 5V-48V dc output
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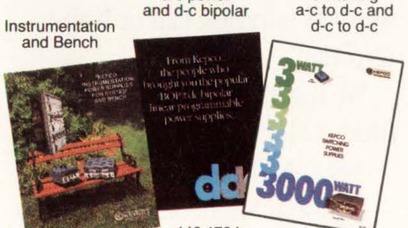

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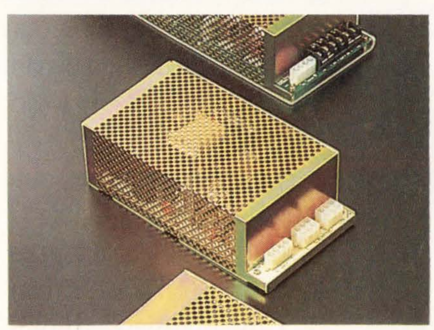

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- ☐ 5V-24V dc output
- ☐ jumper selectable inputs: 85-132 or 170-264V ac, 240-370V dc
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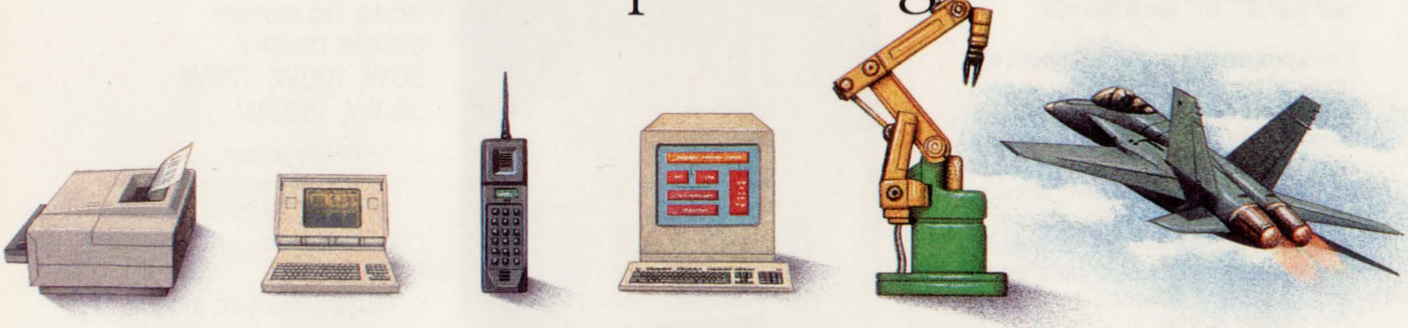

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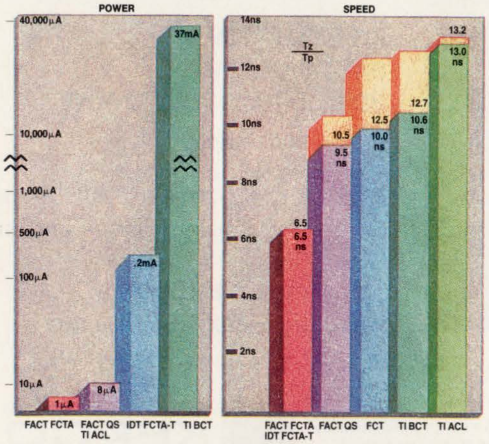

Databook worst case (commercial temp.) Prop delays = '374
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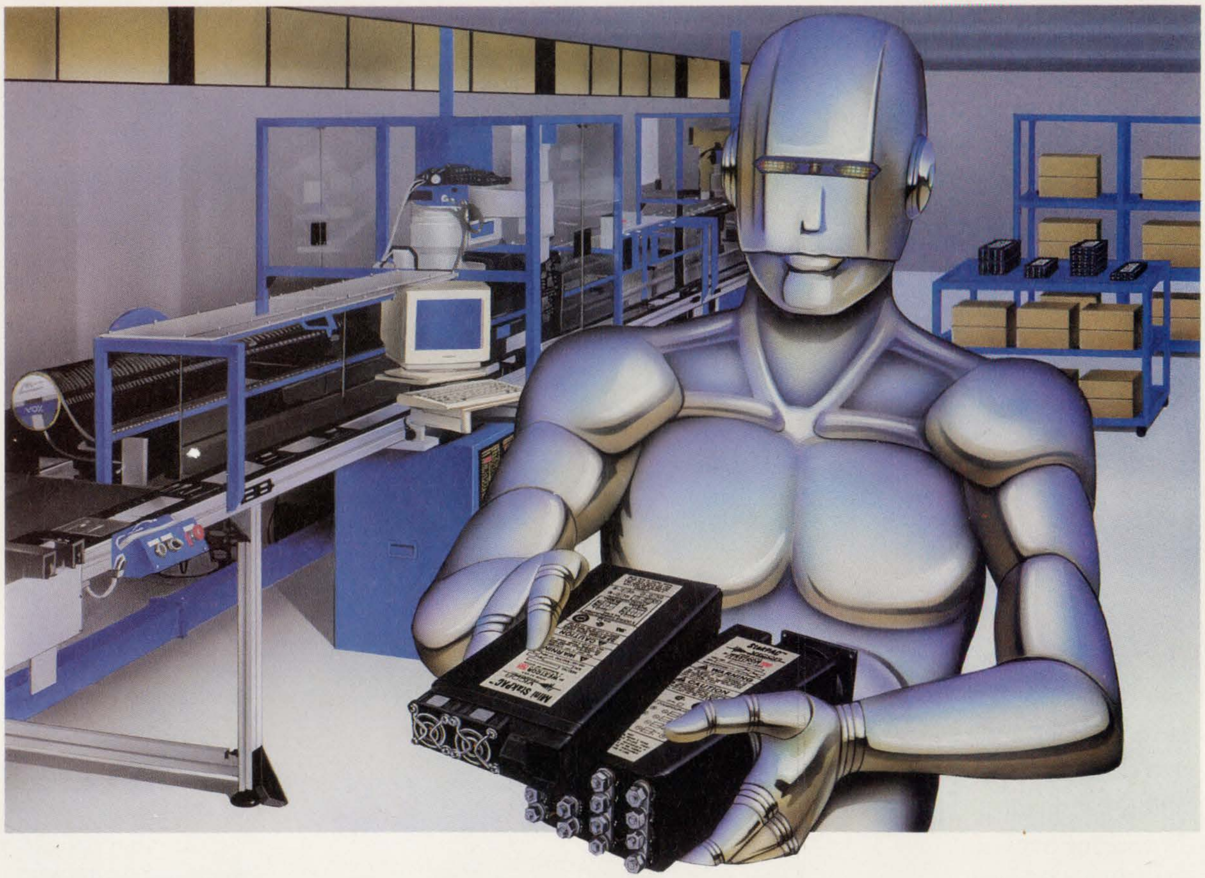
*From a 1990 study conducted by Washington Labs Inc., a subsidiary of Viollette Engineering Corporation.



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STAKPAC™		MINI STAKPAC™
1200 Watts	**Power**	600 Watts
110/220 VAC	**Input**	110/220 VAC
Up to 8	**Outputs**	Up to 5
3.2"x5.5"x11.5	**Dimensions**	1.9"x5.5"x12"
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StakPACs are designed and built by Westcor Corporation, Los Gatos, CA, a Vicor subsidiary. StakPACs are sold world-wide through Vicor Corporation, Andover, MA.

STAKPAC STANDARDS 1200 WATT MODELS

Model	Output Voltage (VDC) and Maximum Current (amperes) per Channel #1	#2	#3	#4	#5
Single Output					
SP1-1801	2 @ 240				
SP1-1802	5 @ 240				
SP1-1603	12 @ 100				
SP1-1604	15 @ 80				
SP1-1605	24 @ 50				
SP1-1606	28 @ 42				
SP1-1607	48 @ 25				
Dual Output					
SP2-1801	2 @ 120	5 @ 120			
SP2-1802	5 @ 120	5 @ 120			
SP2-1803	5 @ 120	12 @ 66			
SP2-1804	12 @ 66	12 @ 66			
SP2-1805	15 @ 53	15 @ 53			
Triple Output					
SP3-1801	5 @ 180	12 @ 16	12 @ 16		
SP3-1802	5 @ 150	12 @ 33	12 @ 16		
SP3-1803	5 @ 180	15 @ 13	15 @ 13		
SP3-1804	5 @ 150	15 @ 26	15 @ 13		
Quad Output					
SP4-1801	5 @ 150	12 @ 16	12 @ 16	5 @ 30	
SP4-1802	5 @ 150	15 @ 13	15 @ 13	5 @ 30	
SP4-1803	5 @ 150	12 @ 16	12 @ 16	24 @ 8	
SP4-1804	5 @ 150	15 @ 13	15 @ 13	24 @ 8	
Five Output					
SP5-1801	5 @ 120	12 @ 16	12 @ 16	5 @ 30	24 @ 8
SP5-1802	5 @ 120	15 @ 13	15 @ 13	5 @ 30	24 @ 8
Seven Output					
SP7-1801	5 @ 60	12 @ 16	12 @ 16	24 @ 8	24 @ 8
	#6	#7			
	5.2 @ 28	2 @ 30			

Total output power may not exceed 1200* watts for any model, single or multiple output. Lower power StakPAC models and many other configurations are available.
*Standard models supply 1100 watts; high-powered version 1200 watts. Please contact the factory.

MINI STAKPAC STANDARDS 600 WATT MODELS

Model	Output Voltage (VDC) and Maximum Current (amperes) per Channel #1	#2	#3	#4	#5
Single Output					
ST1-1401	2 @ 120				
ST1-1402	5 @ 120				
ST1-1301	12 @ 50				
ST1-1302	15 @ 40				
ST1-1303	24 @ 25				
ST1-1304	28 @ 21				
ST1-1305	48 @ 13				
Dual Output					
ST2-1401	2 @ 60	5 @ 60			
ST2-1402	5 @ 60	5 @ 60			
ST2-1403	5 @ 60	12 @ 33			
ST2-1404	12 @ 33	12 @ 33			
ST2-1405	15 @ 26	15 @ 26			
Triple Output					
ST3-1401	5 @ 60	12 @ 16	12 @ 16		
ST3-1402	5 @ 60	15 @ 13	15 @ 13		
ST3-1501	5 @ 90	12 @ 8	12 @ 8		
Quad Output					
ST4-1401	5 @ 30	12 @ 16	12 @ 16	5 @ 30	
ST4-1402	5 @ 30	15 @ 13	15 @ 13	5 @ 30	
ST4-1403	5 @ 30	12 @ 16	12 @ 16	24 @ 8	
ST4-1501	5 @ 30	15 @ 13	15 @ 13	24 @ 8	
ST4-1502	5 @ 60	12 @ 16	12 @ 8	5 @ 15	
ST4-1503	5 @ 60	15 @ 13	15 @ 7	5 @ 15	
ST4-1504	5 @ 60	12 @ 16	12 @ 8	24 @ 4	
ST4-1505	5 @ 60	15 @ 13	15 @ 7	24 @ 4	
Five Output					
ST5-1501	5 @ 30	12 @ 16	12 @ 16	5 @ 15	24 @ 4
ST5-1502	5 @ 30	15 @ 13	15 @ 13	5 @ 15	24 @ 4

Total output power may not exceed 600 watts for any model, single or multiple output. Lower power Mini StakPAC models and many other configurations are available. Please contact the factory.

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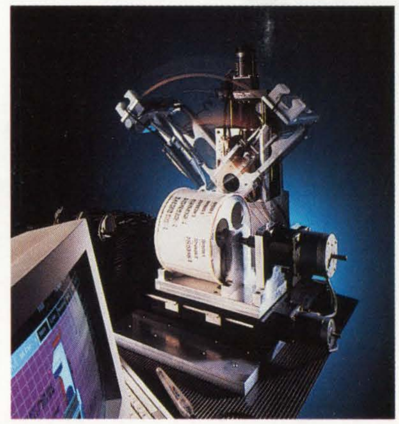
X-Y-Z-Axis translation system provides complex traversing of an arc welding torch head.

Daedal Division is the most recent addition to the growing Parker Hannifin motion control group. Daedal specializes in the manufacture of custom positioning systems as well as standard components including ball slides, stages, and motorized linear and rotary tables.

Together, Compumotor and Daedal provide complete solutions. With fully compatible components from machine controllers, drives and motors to mechanical positioning tables and feedback systems, each system is manufactured, tested and shipped from a single supplier. The net result is an integrated system, tailored precisely to the demands of a specific application.

A fully integrated technical support and service network draws on the combined expertise of Compumotor and Daedal. A pool of factory trained electrical and mechanical field application engineers provides on-site local product support— support that ensures satisfaction from concept through design specifications, system integration and start-up. In addition, a world-wide network of independent factory trained and authorized Automation Technology Centers provides technical assistance, training, local supply, service and complementary products.



An automated system for testing bar-code scanners, from Hewlett Packard, combines Compumotor and Daedal technology.

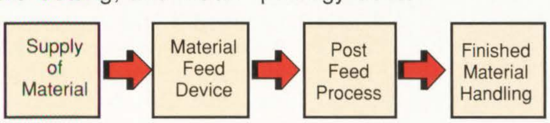
Compumotor and Daedal have the right combination of products, unrivaled support and focused accountability. Take advantage of the new team at Parker Hannifin. In doing so, our aim is to take the risk and the work out of selection, integration, installation and start-up processes, and supply proven quality motion control products. Circle 301

Feed-to-Length Application Solutions

"Everything has been thought of before, the problem is to think of it again."—Johann W. von Goethe.

Each machine design requirement may be unique, but most can be characterized within a basic application category. At Compumotor, our focus is to prevent 're-inventing the wheel.' One such application category, involves the repeated feed of material a specific distance to a stationary position, followed by some other process. Examples include: Thermoforming for tire rubber or plastic film; Labeling/cutting of optical fibers, paper or plastic bags; Drilling; Milling; Bending; Stamping; Core Cutting; and Indexing for a variety of industries.

Compumotor has been providing tailor-made, high performance motion control solutions for more than ten years. With contributions from industry experts, Compumotor has compiled this expertise into a Feed-to-Length Application Handbook to help machine designers and engineers make informed decisions about their applications—to improve machine flexibility and productivity. This reference provides information on important application considerations and insight to application solutions. For a copy of this handbook, contact your local Compumotor Automation Technology Center.



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POSITIONING APPLICATIONS

Dispensing Excellence—Four Axis Motorized Syringe

A unique process requires a metering/dispensing system to apply highly volatile liquid catalysts to a new product. The first catalyst must be applied in a touching off manner from a syringe; the second requires dispensing of 0.3 microliter volumes in a circular path. Inaccurate mechanics and human error in the existing design resulted in liquid flashing and low yields.

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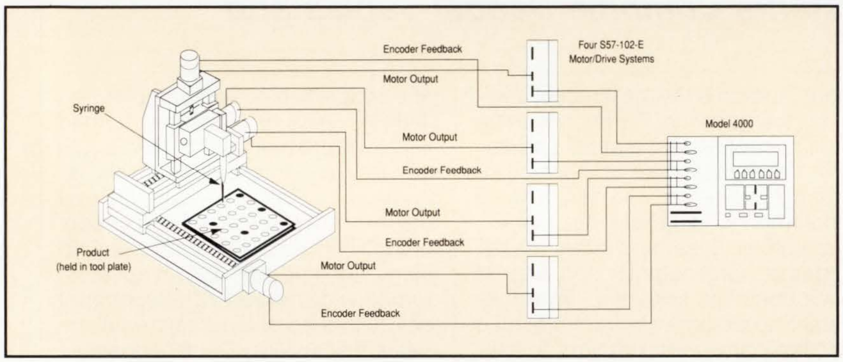
Compumotor's Model 4000 provides a self-contained control for all four axes of motion including the circular interpolation capability. An encoder option on the motor verifies position and provides stall detection. Circle 302

Motion Requirements

- Multi-axis controller—4 axis control of syringe motion
- Contouring—Circular dispensing paths
- High accuracy leadscrew stages—Syringe placement to 0.0001 inches
- Microstepping motor resolution—Smooth dispensing of .3 micro-liter liquid volumes
- Incremental encoder feedback—Ensure position integrity and stall detection

Products Used

- Indexer—Compumotor Model 4000
- Motor/Drives—Compumotor S57-102-E (4)
- X/Y/Z motorized positioning system—Daedal Ball-Bearing Linear Tables
- Transversing positioning system—Daedal 4" Cross Roller Table

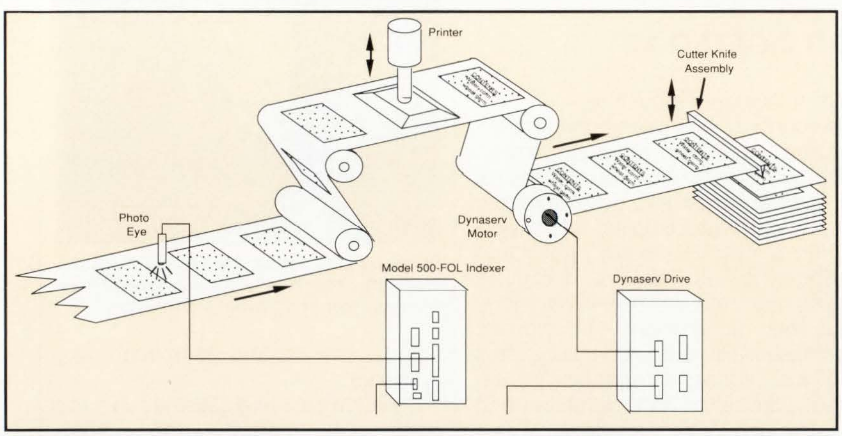


Checkered Flag for High-Speed Feed-to-Length

Problem: A machine manufacturer for the paper, film and foil industry was challenged with an application in which labels were to be printed and cut at high speeds. The design in use had a geared servo motor and drive attached to nip rollers for the material feed. Printing and cutting operations were activated with the feed rollers at rest. This design had unacceptable end-of-move overshoot when throughput requirements were increased. A new design required lower settling times, improved accuracies and adjusting for label shrinkage through the use of registration marks.

Solution: The Dynaserv Direct Drive motor from Compumotor replaces the servo system and its inaccurate mechanical transmission. Directly attached to the feed nip rollers, the Dynaserv provides true servo positioning without harmful backlash. The internal construction of the Dynaserv compensates for the large feed roll inertias better than other motor technologies. These advantages provide the printing operation with a compact solution for high press speeds with minimal end-of-move overshoot.

The Model 500 Indexer provides command signals to the Dynaserv, and I/O interface to the printing and cutting operations. Material feed distances are fully adjustable, and determined by the registration mark on the label. Operator interface is simple thumbwheel input of press speed and feed distance. Nonvolatile storage of the 500 Indexer's command program provides cost-effective stand-alone press control. Circle 303



Motion Requirements

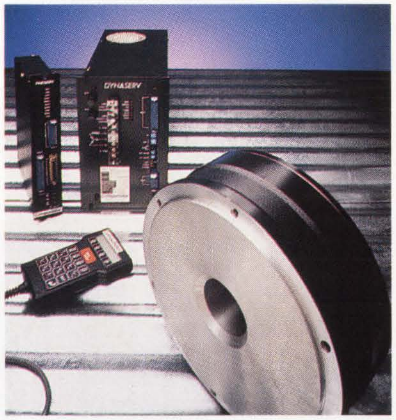
- Servo motor technology—high-speed printing, minimal settling time.
- High resolution/accuracy—labels must be cut to within 1/64 inch.
- Programmable inputs—Photo-eye registration capability
- Direct drive motor, reduced transmission size—Compact web feed mechanism
- Indexer with non-volatile memory and power-up sequences—minimal operator interface.

Products Used

- Indexer—Compumotor Model 500 Indexer
- Motor/Drive—Dynaserv DM1045B Direct Drive motor

POSITIONING PRODUCTS

Rotary Positioning Alternative for Index Table Applications



The Dynaserv, a direct drive servo from Compumotor, is a natural replacement for index table applications.

Index tables—commonly used in industries such as machine tool, cellular manufacturing, welding and large inertia positioning—require accurate rotary positioning while supporting a large load. Mechanical indexing tables requiring gears and cams to produce the desired motion are typically used for these applications. Gears introduce backlash, frictional inaccuracies, and greatly reduced cycle time. The internal clutch of a mechanical table is noisy and subject to wear. In addition, specific cam curves must be ordered for each table required. This adds set-up time and cost, especially if many different tables are needed.

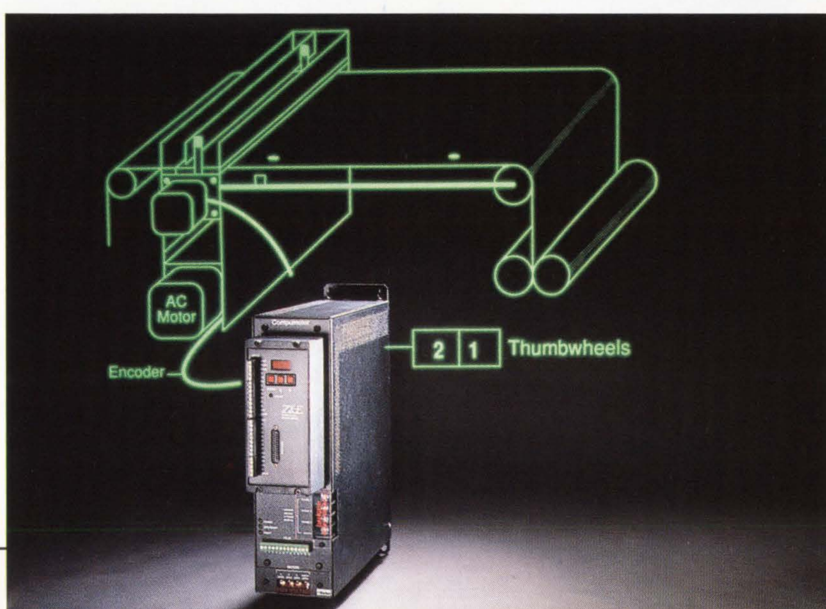
The Dynaserv features a high torque to motor size ratio with stability at all speeds. 1,024,000 step/rev controlled to one step is achievable. A flat speed-torque curve provides greater controllability—with smooth rotation across the system's full dynamic speed range. Because the unit is gearless, faster settling time is realized. This serves to increase productivity, and creates a virtually maintenance-free unit. Circle 304

Follow with the Leader

The ZXF Servo System from Compumotor incorporates a full-functioned velocity and position follower with a digital signal processor-based servo drive in a cost effective package. The ZXF is ideally suited to improve performance in positioning applications such as thermoforming, packaging, labels, tire making, pick and place, automated assembly, winding and stamping. Encoder following capabilities allow the ZXF to be applied in processes requiring operations between separate operations. Features include:

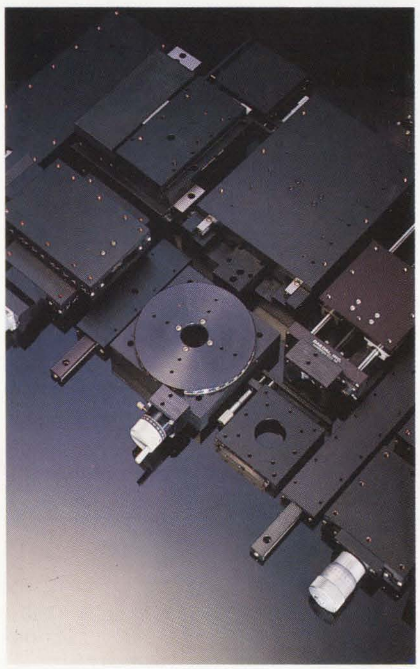
- Velocity and position following
- Recede and advance while following
- Registration while following
- Following a pulse and direction or quadrature encoder signal
- Following data entry through external thumbwheels or RS232 terminal

Programming is easy with Compumotor's powerful and standard extended X-programming language. Circle 305



This bag-maker takes advantage of the accuracy and repeatability of the ZXF Servo System

Metric Table Designs



Daedal offers a variety of metric products for increased systems compatibility, especially in the European and Pacific Rim markets. All components are manufactured to meet current metric standards for both industrial and scientific applications. The new Daedal metric engineering guide highlights these products, most of which are in stock and ready to deliver. The guide features: Manual positioners including ball slides, 1-3 axis linear stages, rotary stages, manual and digital micrometers. Motorized positioning table selection includes ball bearing linear tables, open frame tables, rail tables, cross roller tables and rotary tables.

Tables are available in standard and precision grades, and in single and multiple axis configurations. Travel lengths to 3050 mm (rail table) and payloads to 130 kg are available with life ratings in excess of 2.5 million meters. Rotary tables are available in diameters to 300 mm and loads to 90 kg.

Other points of interest: Daedal stocks more than 1,500 leadscrews and ball screws to tailor table performance to specific applications. Positioning tables and controls are integrated and tested as complete systems.

When your components and systems must measure up, look to Daedal for solutions. Circle 306

SERVICE AND SUPPORT

Putting Service and Support to the Test

A company whose business it is to test and judge quality, demands high standards for equipment—it's their job to. Daedal accepted a positioning challenge for one such company, Ultran, in State College, Pennsylvania.

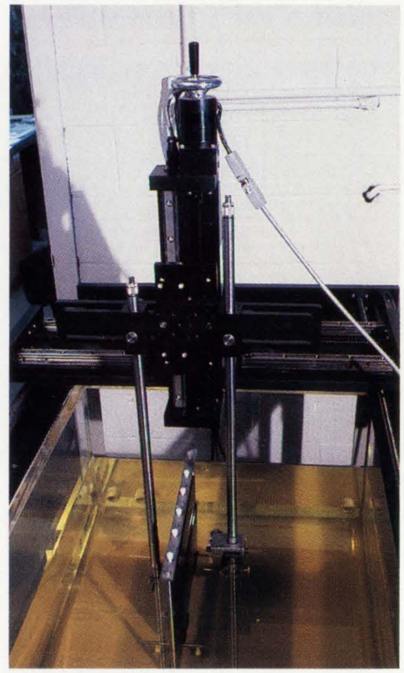
In ultrasonic non-destructive materials testing, an Ultran NDC 7000 Imaging System looks for defects in materials without damaging them. The system requires fine resolution, extreme rigidity, and straight-line accuracy. And because a variety of sizes and weights of material are tested, flexibility in test-equipment configurations is essential.

Daedal worked with Ultran to establish a system that met requirements of existing applications. And flexibility was built in at the onset so Ultran's system can grow with changing needs. The Ultran imaging system is stored on CAD disk and application alterations can be recalled and designed quickly, avoiding the time and talent needed for redesign.

Ultran employees look for defects on images of material which have been scanned via the NDC 7000 Imaging System

In the new system, square rails replaced ball bushing rods, contributing greater rigidity and support throughout the full length of travel. The square rail table construction is ideal for the varying travel lengths and often heavy payloads of this application. Constructed with efficient, double-nut ball screws, the gantry system provides high-speed positioning over travel lengths to 24 by 36 inches.

Ultran will continue to require variations of this system and worked with Daedal to establish a base system for upcoming projects. A standard application has been established, and any variations are easily accommodated such as length, width, payload and Z-axis travel. This helps the company's long-term budgeting and ensures quick turn-around of new products. Circle 307



In Ultran's emulsion scanning tank, a sample is tested with the sweeping motion of a transducer attached to a Daedal table-configured bridge.

LITERATURE

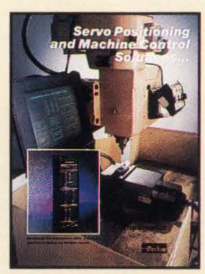
PROGRAMMABLE MOTION CONTROL

From Compumotor—a complete 416-page engineer's guide with specifications, dimensions and performance data presents brushless servos, microstepping motor systems, indexers, linear motors and absolute encoders.
Circle 308

POSITIONING SYSTEMS & COMPONENTS

Daedal's 200-page catalog provides specifications for manual positioners, motorized linear and rotary positioning tables; drives and controls; and optical components and accessories. Includes prices.
Circle 309

SERVO POSITIONING & MACHINE CONTROL SOLUTION



The Compumotor 4400 is a unified approach to motion and machine control. Available in 4 and 8 axis. Features analog servo control, compatible touch screen control, up to 512 discrete or 256 analog I/O.
Circle 310

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Daedal Division
P.O. Box 500, Sandy Hill Road
Harrison City, PA15636
1-800-245-6903

Parker Hannifin Corp.
Compumotor Division
5500 Business Park Drive
Rohnert Park, CA 94928
1-800-358-9070

Parker

ATE PIN ELECTRONICS

Versatile ICs reach beyond ATE systems

IC manufacturers have developed pin-electronic circuits that serve as building blocks for ATE systems. But these high-performance ICs aren't limited to ATE applications.

Doug Conner, Regional Editor

Automatic test equipment (ATE) pin electronics must meet severe demands for speed and timing accuracy. To serve the particular requirements of ATE, IC manufacturers have developed high-performance, moderately priced chips for use as pin drivers, comparators, time-delay generators, and combinations thereof. These chips not only simplify life for ATE designers, but they can also function well in other electronic applications.

To understand what ICs for pin electronics can do, you need to understand the basic functions performed by pin electronics. If you are not familiar with ATE pin electronics, see the **box**, "Basic ATE pin-electronic functions."

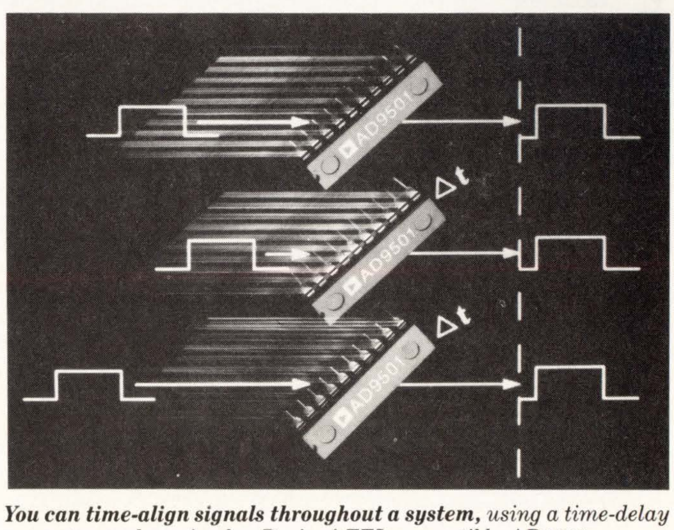
Pin drivers

In high-performance ATE applications, pin drivers output high-quality waveforms. The waveforms need to have a minimum of ringing and undershoot/overshoot. Edge transitions need to be fast and repeatable for accurate timing calibration. Pin-driver ICs typically have slew rates from about 1.5 to greater than 10V/nsec for some GaAs ICs from Gigabit and Triquint (**Table 1**). Devices such as the 16G061A dual pin driver from Gigabit offer variable edge rates for compatibility with different logic families.

Although pin drivers need low propagation delays, accurately calibrating pin-driver timing places emphasis on *stable* propagation delay through the IC. Sensitivity to temperature, duty cycle, and other conditions affecting the propagation delay is more important than the absolute value of the delay. High-speed pin drivers also need to have accurate edge-to-edge matching (a measure of the difference in propagation delay between rising and falling edges).

To achieve the high speeds typically needed for ATE applications, pin drivers are usually ECL compatible. However, some pin-driver ICs will also accept TTL or CMOS logic levels.

A measure of the speed capability of a pin driver is the maximum toggle rate of the device. The maximum toggle rate defines how fast the pin driver can output data and still slew to the final value before changing to the next output state. The maximum toggle rate typically decreases as the voltage difference



You can time-align signals throughout a system, *using a time-delay generator such as Analog Devices' TTL-compatible AD9501.*

ATE pin electronics

between the output logic-high and logic-low states increases.

You should note how well isolated the output of the driver is when you switch the driver to the off or high-impedance state. Some devices have off-state leakage currents lower than a μA. Other pin drivers in the off state still load the circuit with a 50Ω termination to −2V. If you need high isolation when the pin driver is in the off state, some of the pin-driver ICs may not meet your needs.

Pin drivers use analog voltage inputs to set the levels for the logic high and low states. How much the pin driver loads the high and low voltage references can vary. If you have to buffer the voltage references for each pin driver, you'll need to factor in the additional pc-board space, power, and cost.

Pin-driver ICs provide a general-purpose building block for driving digital signals in applications whose logic levels need to be varied. You can use these ICs to build ATE, but you can also use them for the output of variable-level pulse generators. Pin driver ICs can even drive 50Ω transmission lines, although they may not be able to do so over their entire output voltage range.

Table 1—Representative pin-electronic devices

Manufacturer	Product	Key features	Price (100)
A. Pin drivers and combined products			
Analog Devices	AD1321	100-MHz toggle rate; −2 to 7V output range; 200-nA-max off-state leakage.	$45
	AD1322	200-MHz toggle rate, otherwise same as AD1321.	$85
Brooktree	BT698	Pin driver, comparators, dynamic loads; 125-MHz toggle rate with 1V swing; −3 to 8V operating range.	$130
Comlinear	CLC600	200-MHz operation; −2 to 7V output range; 40-nA-typ off-state leakage.	$42.50
Gigabit	16G061A	Dual pin driver; 800-MHz bandwidth; variable slew rate: 2.5 to 17 V/nsec; 50-μA off-state leakage.	$95
Pulse Instruments	PT40B	100-MHz clock rate; 0.3 to 8V output range; 10-pin SIP hybrid.	$36.25*
Triquint	TQ6330	100-psec rise and fall times for 1V swing; −3 to 3V for 50Ω loads.	$115
B. Comparators			
Analog Devices	AD1317	Dual comparator with latch; 10-μA input-bias current; inputs switchable to high-impedance state.	$25
	AD96685	Latching comparator; −2.5 to 5V input range.	$4.60
	AD96687	Dual version of AD96685.	$6.40
	AD9696	TTL-compatible comparator; 4.5-nsec propagation delay.	$3.50
	AD9698	Dual version of AD9696.	$6
Brooktree	BT687	Dual latching comparator; 20-μA input-bias current; −3.3 to 3.3V input range.	$12
	BT688	−4.0 to 10.2V input range; 2-μA-typ input-bias current; 2.8-nsec propagation delay.	$20
	BT681	−4 to 8.2V input range; 2-μA-typ input-bias current; 2.6-nsec propagation delay.	$37
C. Time-delay generators			
Analog Devices	AD9500	8-bit digital delay generator (ECL); 2.5-nsec to 10-μsec range; 100-MHz-max trigger rate.	$16
	AD9501	8-bit digital delay generator (TTL/CMOS); 2.5-nsec to 10-μsec range; 50-MHz-max trigger rate.	$8.60
Brooktree	BT604	8-bit digital delay generator; 4- to 40-nsec delay range; 120-MHz, programmable on the fly.	$33
	BT622	Dual-channel delay line; independently adjust rising and falling edge; 10-, 20-, 30-nsec ranges.	$37
	BT624	Quad version of BT622.	$46
D. Dynamic loads			
Analog Devices	AD1315	Complete dynamic load; ±50-mA range; −2 to 7V compliance range.	$40

*Price for quantities of 1000 or more.

Fast comparator, stable delay

Every electronic engineer is familiar with the performance of analog comparators, but the performance requirements placed on comparators for ATE applications are particularly demanding. ATE applications typically place three tough requirements on comparators.

First, the comparator must be fast. Propagation delays of a few nanoseconds are acceptable, but, as is the case for pin drivers, a stable propagation delay is very important.

Second, the comparator needs a relatively wide input-voltage range. ATE applications typically need a −2 to +7V range, although more is desirable. However, narrower voltage ranges make it easier to design a comparator for speed.

Third, ATE applications often need comparators with a low input-bias current for use in testing low-power CMOS devices. But it is easier to make fast comparators when you can use relatively high input-bias currents.

Like many engineers, ATE designers can't always buy what they need, so they sometimes have to design around the comparator. In the past you might have bought a fast comparator with a limited input-voltage range and a low input impedance. You'd have to add your own circuitry to buffer and scale the inputs to get the needed voltage range and input impedance. Now you can buy comparators off the

Basic ATE pin-electronic functions

The overall function of ATE pin electronics is to drive input pins and measure outputs. To keep ATE general purpose, the pin electronics are usually designed to support both drive and measure functions on every channel.

Pin drivers for ATE provide inputs to the device under test (DUT). Pin drivers **(Fig A)** typically support three states: logic-high, logic-low, and a high-impedance or off state. You program the logic high and low levels with analog voltage inputs. The programmable range of the high and low states is typically −2 to +7V, providing sufficient range for compatibility with TTL, CMOS, and ECL voltage levels.

When measuring a DUT's outputs, the test system switches the pin driver to an off state and measures the output levels with comparators **(Fig A)**.

If you go by the data-book specifications, a device's logic high doesn't occur until the voltage exceeds the minimum logic high, and its logic low doesn't occur until the voltage falls below the maximum logic low. Because ATE systems normally test using data-book specifications, designers usually use two comparators in a window-comparator arrangement. The test system latches the output of the two comparators at the programmed test time, and the state of the comparators shows whether the output pin was in a high, low, or intermediate state.

Testing ICs to data-book specifications also requires testing output-drive capabilities. Output-drive testing verifies the current a device output can source in a logic-high state or sink in a logic-low state. Dynamic-load circuits provide the current sinks and sources needed by ATE to test the output drive.

Fig A diagrams the basic operation. Positive and negative current sources connect to the output pin of the device under test through a diode quad. When the output voltage drops below the threshold voltage set on the opposite side of the diode quad, the DUT must sink the current from the current source. Conversely, when the DUT output voltage goes above the threshold voltage, the DUT must source current to the dynamic load. Dynamic-load circuits, although important in ATE systems, don't have wide application in other electronics systems.

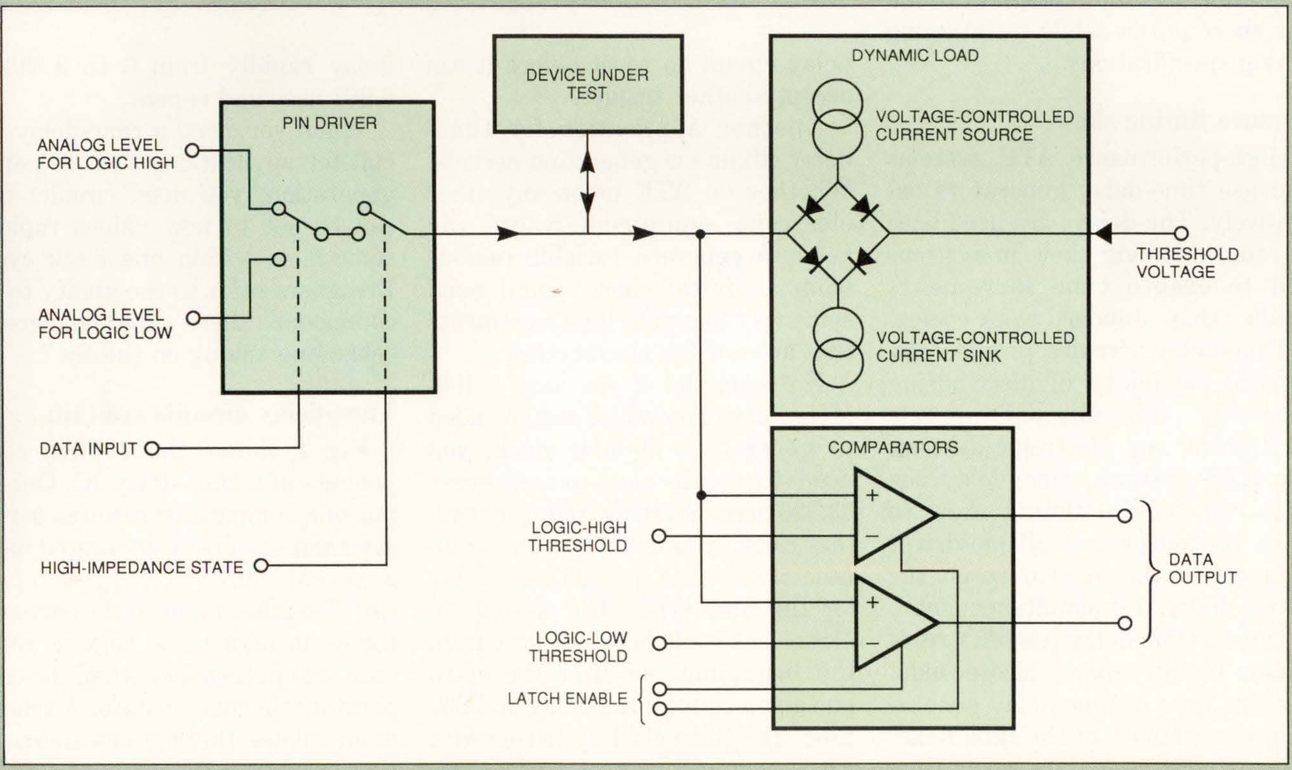


Fig A—The basic ATE pin-electronic devices *are drivers, comparators, and dynamic loads.*

ATE pin electronics

shelf that measure up well against ATE requirements. Hence, you can design with more freedom.

Comparators available from both Analog Devices and Brooktree, some of which have TTL-compatible outputs, offer a range of performance capabilities.

For example, Brooktree's BT681 dual comparator has attractive performance not only for ATE applications but also for instrumentation, line-receiver, and other thresholding applications. The comparator can track inputs that slew at 4V/nsec over a range from −4 to +8.2V. The typical input-bias current is 2 μA, but you can reduce it to 100 nA with a selectable power-down mode when you can afford to trade speed for a lower input-bias current. A level-select control lets you reduce the complementary ECL output swing from a nominal 800 mV to 400 mV. The reduced amplitude lets the comparator follow short pulses while maintaining timing specifications.

Remove timing skew

High-performance ATE systems also use time-delay generators extensively. The delays are used both to remove timing skew in systems and to create time increments smaller than standard clock cycles.

Time-delay circuits provide the general capability of distributing precisely time-aligned signals throughout any electronic system. For ATE systems, time-delay circuits can remove timing skew to make the outputs of all pin-driver channels in the system reach the device under test simultaneously.

Typical time-delay ICs offer resolutions in the tens of picoseconds. For this type of time-delay generation, the stability of the time delay is important, as is the recycle time on the time delay. The recycle time is the time you need to wait for the delay circuit to reset before it can accept another trigger.

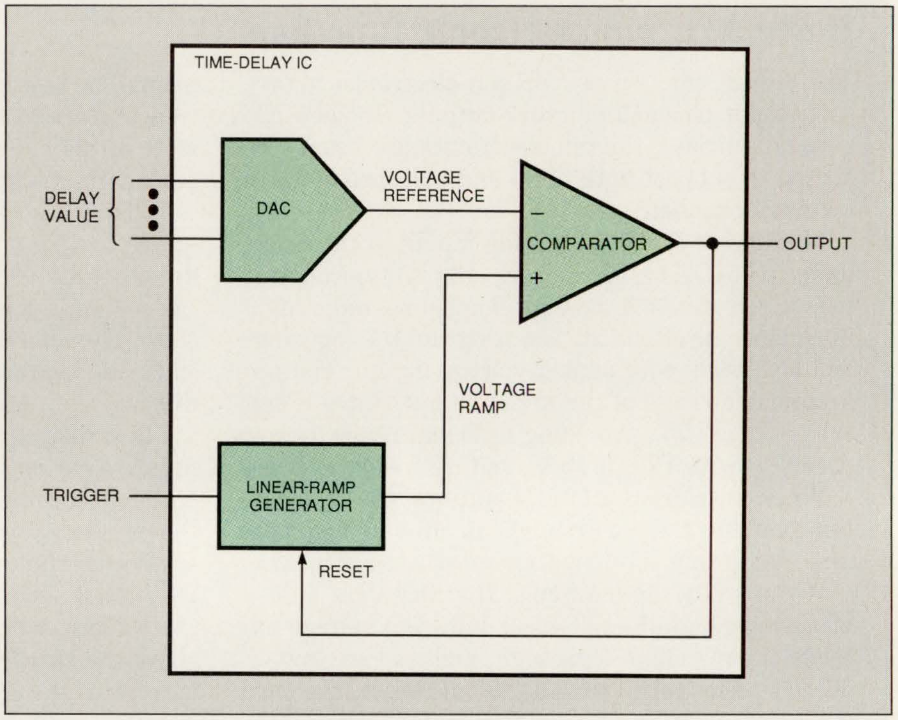


***Fig 1—Time-delay circuits typically contain a voltage ramp** initiated by a trigger input. When the voltage ramp reaches the level of the adjustable reference voltage, the comparator changes state, outputting the delayed edge. An internal DAC or analog input provides the reference voltage.*

Another application for time-delay circuits is generating periods. Whether on ATE or on any other electronic equipment where you need to generate variable periods from a digital clock, you'll need some way to create time increments that are not full clock cycles.

For example, if you have a 100-MHz clock in a system and you need to generate a 30-MHz clock, you need to create clock pulses every 33.333 nsec. Starting from your system clock, you count out three 10-nsec clocks plus a 3.333-nsec delay for the first cycle. The second 30-MHz clock cycle is 66.667 nsec from the beginning, so after the sixth pulse you count out a delay of 6.667 nsec. The third clock cycle coincides with the tenth system clock pulse. In this example, the circuit controlling the time delay must switch the delay rapidly from 0 to 3.333 to 6.667 nsec and repeat.

When you need a time-delay circuit for applications such as period generation, you need circuits that can be set to new values rapidly, sometimes within one clock cycle. Designers refer to the ability to accommodate these rapid changes as "changing timing on the fly."

Time-delay circuits contain . . .

Fig 1 shows the typical components of a time-delay IC. One input of a comparator receives a voltage ramp, typically generated using a current source to charge a capacitor. The other input to the comparator is an adjustable voltage reference that determines when the comparator will change state. A trigger input allows the current source to begin charging the capacitor. When the capacitor charges to the voltage of the reference input, the compara-

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UC1842	*UC1842A	UC3842	*UC3842A
UC1843	*UC1843A	UC3843	*UC3843A
UC1844	*UC1844A	UC3844	*UC3844A
UC1845	*UC1845A	UC3845	*UC3845A
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TECHNOLOGY UPDATE

ATE pin electronics

For more information . . .

For more information on the pin-electronic products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

Analog Devices Inc
831 Woburn St
Wilmington, MA 01887
(508) 657-7960
TWX 710-394-6577
Circle No. 708

Comlinear Corp
4800 Wheaton Dr
Fort Collins, CO 80525
(303) 226-0500
FAX (303) 226-0564
Circle No. 710

Pulse Instruments
1234 Francisco St
Torrance, CA 90502
(213) 515-5330
FAX (213) 515-0068
Circle No. 712

Brooktree Corp
9950 Barnes Canyon Rd
San Diego, CA 92121
(619) 452-7580
FAX (619) 452-7580
Circle No. 709

Gigabit Logic
1908 Oak Terrace Lane
Newbury Park, CA 91320
(805) 499-0610
FAX (805) 499-2751
Circle No. 711

Triquint Semiconductor Inc
Group 700, Box 4935
Beaverton, OR 97076
(503) 641-4227
FAX (503) 644-3198
Circle No. 713

tor changes state, triggering the output.

Time-delay circuits typically accept either digital or analog inputs for the adjustable reference voltage. If the delay circuit accepts digital time-delay inputs, then it contains an internal DAC. If the time-delay circuit accepts an analog voltage for the time-delay input, then you can control the time increments by selecting the resolution of an external DAC. You also may have control over the time-delay range and resolution if the timing capacitor is external.

Some other specifications to watch for on time-delay circuits are how linear and monotonic the delay is. If you can measure when you have set the time delay correctly, then you don't necessarily need a perfectly linear time delay versus voltage. As long as the time delay is monotonic, you can reach the correct value within a few trials. If you'll be changing the time delay on the fly or don't have a way to measure the accuracy of the setting, then linearity may be important.

Delay circuits may respond only to a rising or falling edge and output a fixed pulse, or they may delay both the rising and falling edges. Some time-delay ICs that delay both the rising and falling edges allow you to adjust the two edges independently.

You don't need to be an ATE designer to benefit from the time-delay ICs available. Any time you need to create short, stable time delays adjustable with fine increments, you should consider time-delay ICs. EDN

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ASK EDN

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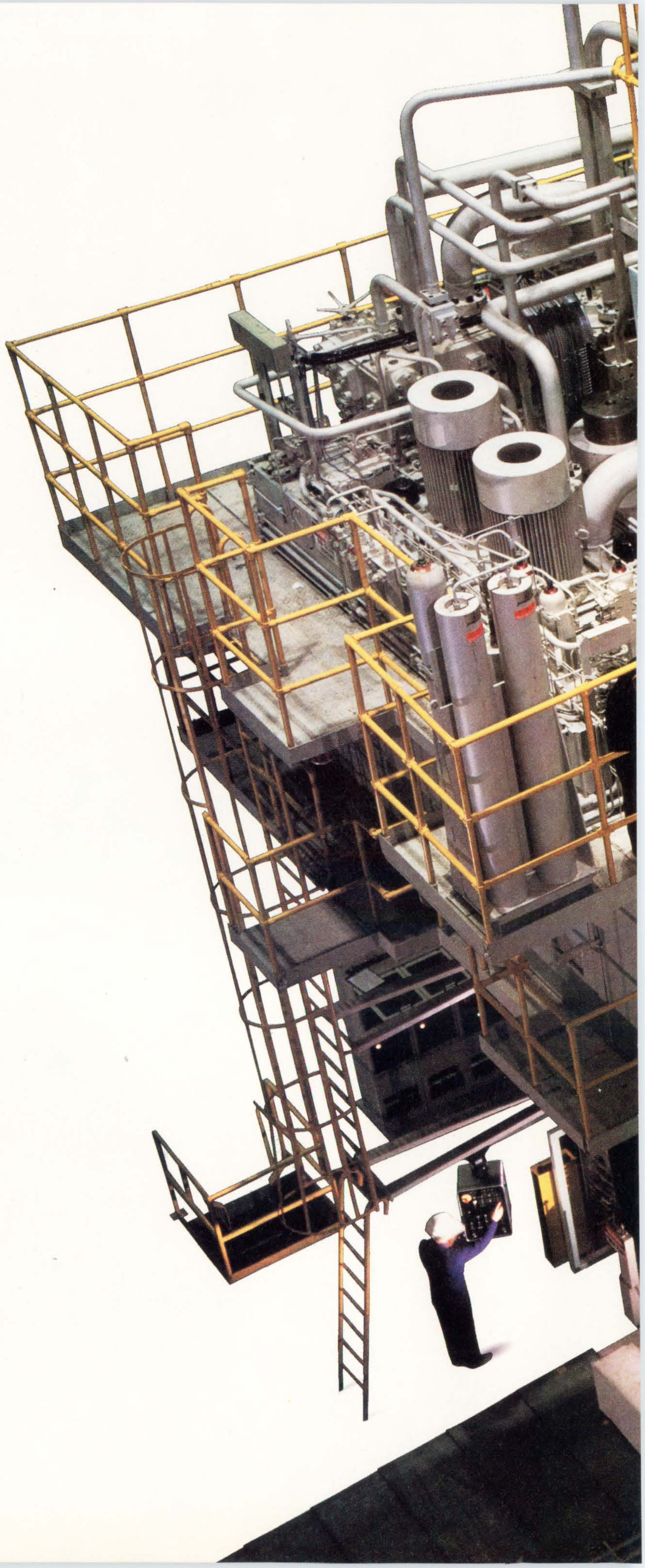


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EDN EDITORS' CHOICE INNOVATION

CAE router uses reconstruct algorithm to increase pc-board layout efficiency

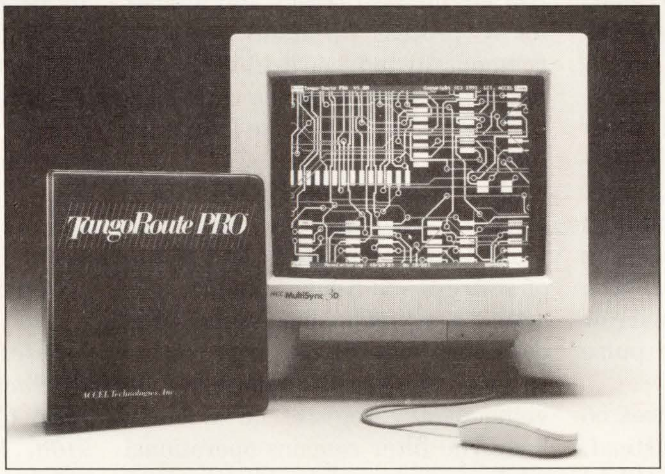
The Tango family of CAE software for PCs now includes an automatic circuit board router that uses a "reconstruct" routing algorithm. The Tango-Route Pro software also performs a pass on completed pc-board layouts using manufacturing-improvement algorithms. These algorithms eliminate extra vias between layers and reduce trace lengths by angling signal routes at 45°.

The reconstruct algorithm allows Tango-Route Pro to handle circuit-layout roadblocks differently from other routers. Router software that uses traditional "rip-up and retry" algorithms removes hundreds of previously placed signals when a roadblock occurs. Such software routes the removed signals in random order on successive retries, solving roadblocks by time-consuming trial and error. Tango-Route Pro analyzes all of the previously placed signals that prevent routing a new signal and reconstructs a single blocking trace to solve routing conflicts.

The Tango router supports board designs as large as 32×32 in. and features a resolution of 1 mil. You can lay out boards having as many as 4000 components, 10,000 signal nets, and 256 connectors. The CAE package supports as many as 15 layers—10 signal layers, 1 power layer, 1 ground layer, and 3 miscellaneous layers.

The Tango-Route Pro software can analyze a circuit design and automatically set routing parameters such as number of layers, grid size, and even general signal direction for specific layers. You can change any settings via Tango's standard user menus.

You can set design rules such as pad-to-pad, track-to-track, and pad-to-track on a layer-to-layer basis.



Simultaneously working on all layers, *the Tango-Route Pro package for IBM-compatible PCs automatically generates pc-board designs optimized for manufacturing with 45° trace angles and minimized trace lengths.*

You can choose uniform grid patterns for a layout ranging from 8 to 100 mils. Also, nonuniform grid patterns such as 40-20-20-40 or 17-16-9-8-8-9-16-17 mils allow the flexible component and signal placement that gridless routers offer.

The router supports surface-mount designs with user-defined line widths and vias, automatic via fanout, and any type of solder pad. You can place SMD (surface-mount device) pads on top and bottom layers, and the software doesn't limit the pitch of SMD components.

Tango-Route Pro works with all layers of a design simultaneously, improving completion rates and producing boards that are easier to manufacture. The software also uses T-routes in the pc-board layout, which makes trace lengths shorter and therefore uses less copper. During the manufacturing pass, the router's special algorithms reduce trace lengths even further.

The software saves the results of each routing pass during operation and at any user-specified interval. Therefore, you can recover from power or human interruptions and resume routes in progress. You can monitor designs in progress on screen, and check the status of operations via user menus. The router also generates a report that documents statistics pertinent to all routing passes.

The Tango-Route Pro software costs $5500 and is available now. The program runs on 80386- (with a 387 numeric coprocessor) or 80486-based computers with MS-DOS 3.3 or later and a minimum of 4M bytes of RAM. The software supports Hercules-compatible monochrome, EGA, VGA, and numerous high-resolution video cards. You must also own Tango-PCB circuit-board-layout software to use the router.

—Maury Wright

Accel Technologies Inc, 6825 Flanders Dr, San Diego, CA 92121. Phone (619) 554-1000. FAX (619) 554-1019.

Circle No. 730

Continuous-time programmable filter spans 1.5 to 15 MHz

The IMP42C55 is a continuous-time lowpass filter IC with a programmable cutoff frequency. Because the device is tailored for serial data recovery, you can also adjust the filter's zeros, allowing you to reshape pulse signals.

The IC provides four filter elements with second-order frequency responses, called biquads. The first biquad section forms an all-pass filter for phase equalization. You can program the section's center frequency and Q, or, if you don't need equalization, you can program the IC to bypass the section.

The remaining sections implement a sixth-order Bessel filter with programmable cutoff frequency. Two of the sections offer programmable zeros, letting you adjust the filter's response to rising and falling edges separately. The effect on pulse signals is to narrow the pulse while making the pulse shape more symmetric.

The 16-pin CMOS IC requires no external filter components. Instead, an on-chip, phase-locked-loop (PLL) control circuit locks onto a user-supplied reference clock to set the filter's cutoff frequency. Because each filter section uses a transconductance amplifier, the ratio of the amplifier's conductance to an integrating capacitor sets the filter's pole. The PLL control circuit controls the filter's cutoff frequency by adjusting the amplifier's conductance ratio in two ways: changing the capacitance and changing the conductance current.

Each filter section forms its integrating capacitor from a bank of eight individually switchable capacitors. The control circuits switch in and out of the eight capacitors as needed for coarse frequency adjustments. The control circuit makes fine adjustments by injecting bias currents into the amplifiers.

The control circuit derives its intelligence from the reference clock. By feeding the clock into a master biquad and developing an error signal from the biquad's quadrature output, the circuit can tune the master biquad to operate at the desired cutoff frequency. The same error signal tunes the four biquads in the Bessel filter, forcing them to track the master biquad. The control circuit also tracks and adjusts for IC process variations and environmentally induced drift in the amplifiers and will hold the cutoff frequency within 10% of the frequency setting.

You program the IC through a 3-input serial interface. You clock in an 8-bit serial data packet (3 bits of address and 5 bits of data), then activate a strobe line to load the data into control registers within the IC. You can also read back the value of any register on a fourth line. The filter remains operational while you enter data, allowing you to dynamically adjust the filter's response as your signal changes.

You can vary the filter's cutoff frequency over a range of 10:1 by programming a reference-frequency prescaler in the PLL control loop. The prescaler yields the cutoff frequency of

$$f_C = \tfrac{2}{3}k/if_{REF},$$

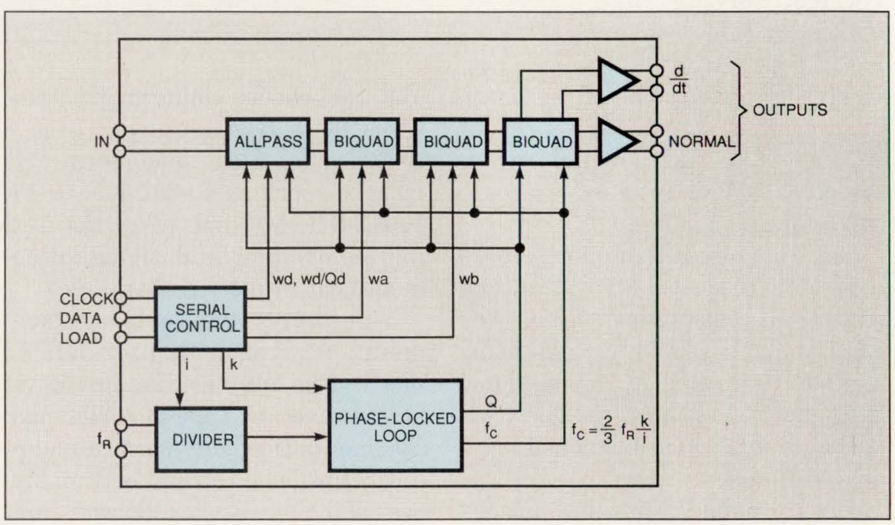
where $i = 1\text{-}4$ and $k = 7.17/(3.17 + n)$, and where $n = 0\text{-}7$. The IC supports a cutoff frequency between 1.5 and 15 MHz.

The IMP42C55 comes in a 16-pin, \$15 DIP or \$15.25 SOIC package. The filter consumes 100 mA when active and 250 μA when programmed into power-down mode. It uses TTL-compatible control lines and accepts 1V p-p analog signals. Both versions are available in sample quantities.

—Richard A Quinnell

International Microelectronic Products Inc, 2830 N 1st St, San Jose, CA 95134. Phone (408) 432-9100. FAX (408) 434-1335. TLX 499-1041.

Circle No. 732

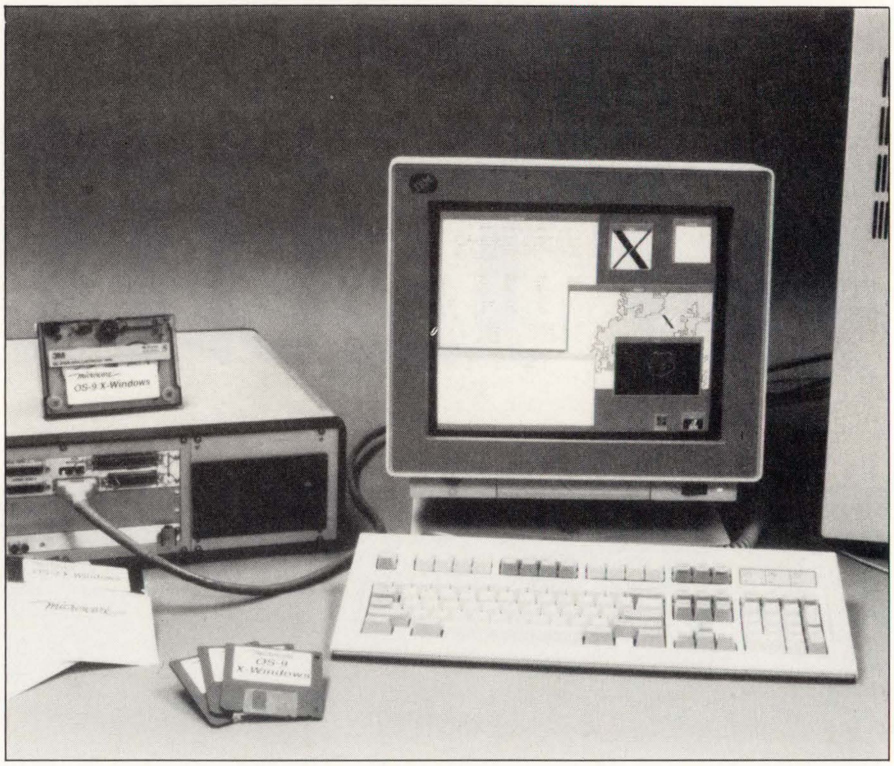


A phase-locked loop ensures the stability *of this programmable sixth-order Bessel filter IC. The lowpass filter offers a cutoff frequency ranging from 1.5 to 15 MHz.*

X-Window package provides user interface for embedded real-time applications

OS-9 real-time operating-system users can add X-Window-based graphical user interfaces to their 68000-based embedded real-time systems. The OS-9/X-Window software package provides a complete X-Window client implementation. You can use the software in OS-9-resident development environments and Unix- or MS-DOS-based cross-development applications. The X-Window implementation is compatible with a variety of networked X-Window servers, and the company offers embedded X-Server support for OS-9 and specific graphics boards.

The software package complies with the X-Window version 11 release 4 package from MIT. The product includes X-Client support including X-Window development libraries, runtime client programs, sample source code for client programs, and the MIT Tab window manager. You can expect the company to add an OSF Motif window manager to the package in the third quarter of this year.



***Users can develop graphical** application programs for real-time systems that comply with industry-standard windowing software with OS-9/X-Windows.*

The X-Window development libraries include Xlib (X-window library), Xt (X toolkit intrinsics library), Xaw (X athena widgets library), Xmu (X miscellaneous utilities library), and Xdmcp (X display manager control protocol library). Runtime client programs enable programmers to perform system-level functions, such as initializing and starting up the X-Window package. The xterm program, for example, lets you open terminal-emulation windows.

The package includes sample source code for several X-Window-client programs including maze, xcalc, and xclock. The package also includes a Unix-compatible library, which adds OS-9 system functions that emulate Unix functions found in X-Window routines. You can therefore port applications from Unix to OS-9, and vice versa.

Initially, the package provides X-Window-server support for OS-9 systems that use the MMI-250 graphics board from Vigra Inc (San Diego, CA). The package also includes sample X-Window-server source code that users can port to other boards.

For now, users can port industry-standard windowing packages to their systems and provide operators with graphical interfaces. The development tools included in the OS-9/X-Windows package simplify developing graphics-based application programs. X-Window real-time systems can operate in X-Window networks of heterogeneous systems.

All members of the OS-9/X-Window family are available now. The full X-Window client development package costs $995. You can buy the client runtime package, a runtime version ready for delivery, for $195. Full source code for the client development package costs $15,000. The server source code package costs $150.—***Maury Wright***

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Circle No. 733

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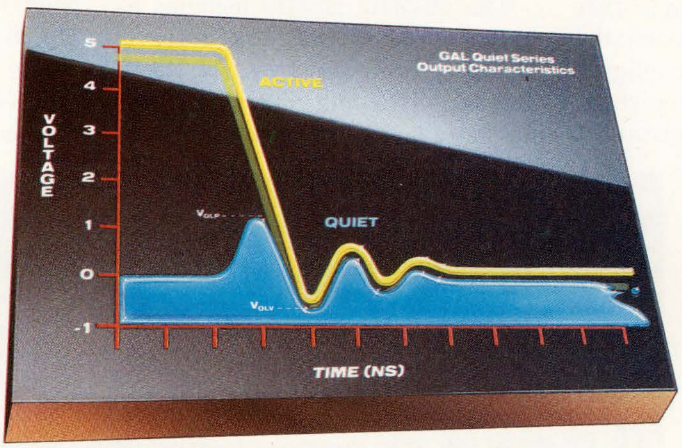

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National	1.18	−.62	1.40	1.78
Competitor A	2.06	−.66	1.10	1.83
Competitor B	1.58	−.66	1.39	1.62
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*V_{ILD}—Dynamic Input threshold low **V_{IHD}—Dynamic Input threshold high

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Microcontroller family features configurable 8- or 16-bit registers

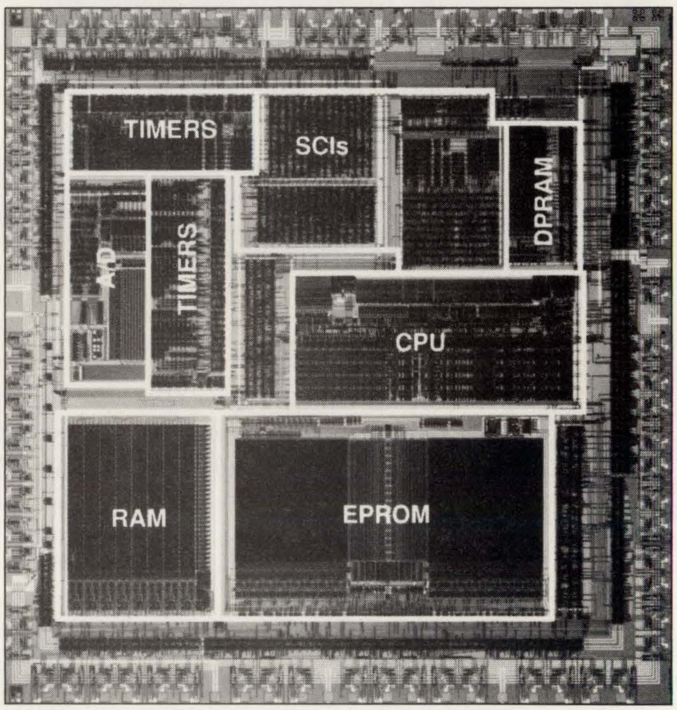
The H8/300 microcontroller (µC) family features an 8-bit external bus and a 16-bit internal bus, although the ALU is 8 bits. The µCs' internal register scheme is a feature that makes this family unusual; under software control, you configure the 16 8-bit or 8 16-bit registers. In addition, the µCs' register-to-register operations allow each register to act as an accumulator.

Although the CPU uses an 8-bit ALU, both 8- and 16-bit adds and subtracts execute in one instruction cycle (two clock cycles). An 8×8-bit multiply and a division of 16-bit dividends by 8-bit divisors occupy seven instruction cycles. At 10 MHz, these add/subtract instructions execute in 200 nsec, whereas the multiply/divide instructions execute in 1400 nsec. The family's 57 instructions are either 2 or 4 bytes, but they aren't compatible with other µC instruction sets.

Software support, running on IBM PCs and sometimes VAX workstations, includes a real-time kernel based on the Industrial TRON (The Real-time Operating System Nucleus) specification. Ready Systems (Sunnyvale, CA) is developing another kernel, based on the VRTX-RTOS. C-language development tools are available from Avocet (Rockport, ME), Microtec Research (Santa Clara, CA), and Software Environments (Dallas, TX).

The µC family also features a fuzzy-logic compiler, developed by Togai Infralogic (Irvine, CA). Other development tools such as assemblers, simulator/debuggers, librarians, and ICEs are available from Hitachi or third-party developers.

The 10-MHz H8/310 includes 8k bytes of EEPROM, 10k bytes of masked ROM, 256 bytes of RAM, and a 1-bit I/O pin. The pin enables fast data transmission and prevents transaction bottlenecks. A write/erase-inhibit function protects stored data from accidental erasure. The µC is tailored for smart-card applications and is sold only in die form for less than $10 (OEM qty).



The H8/330's assorted peripheral functions *complement a flexible 8/16-bit internal architecture that uses register-to-register operations.*

The H8/320, another series in the family, comprises four devices. These µCs differ in their memory configurations, ranging from 8k to 32k bytes of ROM or one-time-programmable EPROM, and 256 to 1k byte of RAM. The family shares one 16-bit and two 8-bit timers, two serial ports, four external interrupts, and 16 internal interrupts. These µCs are available in 6-, 8-, and 10-MHz versions. Prices range from less than $9 (OEM qty) to $14.25 (100).

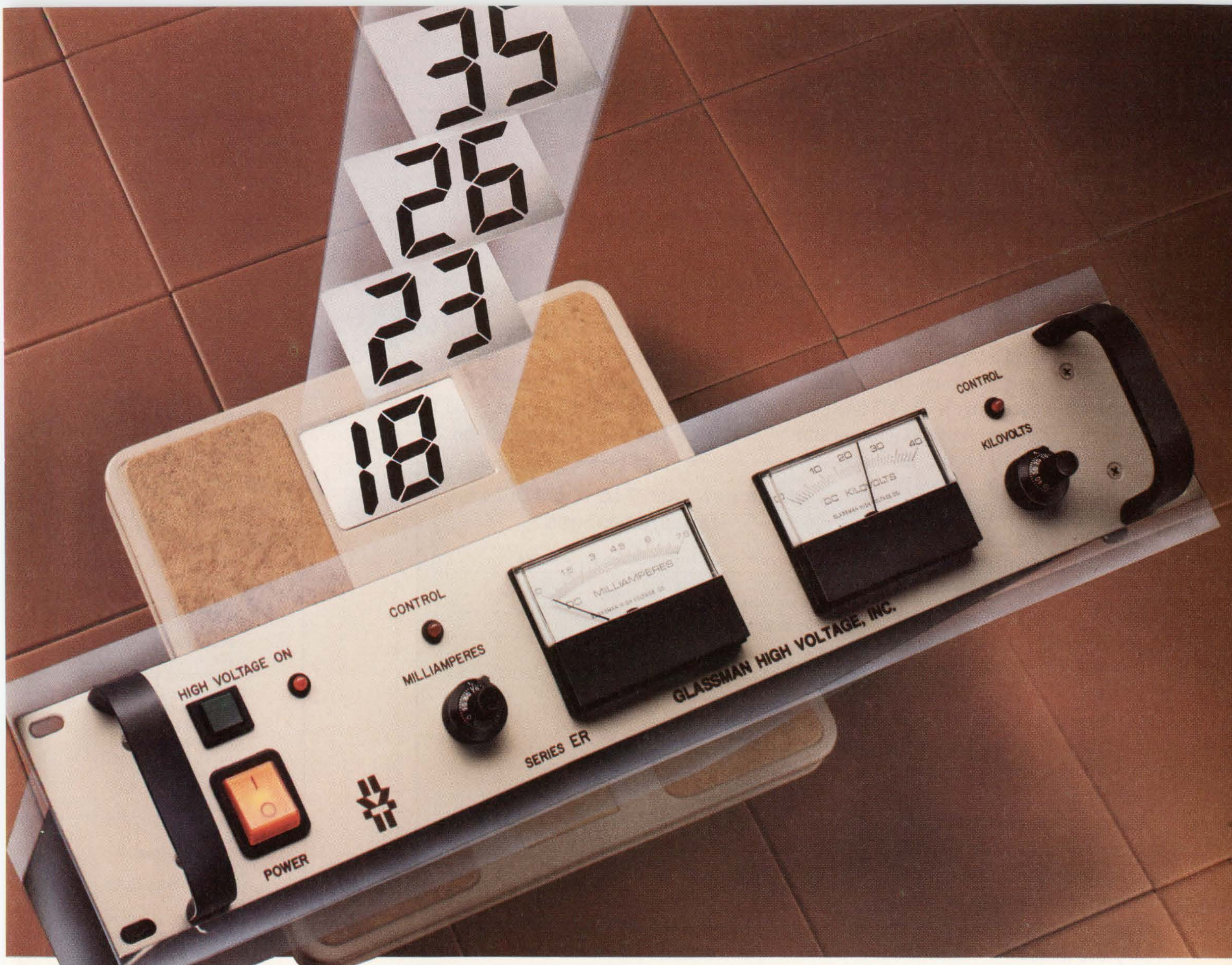
The H8/330 µC includes an 8-bit, 8-channel ADC; 16k bytes of masked ROM or one-time-programmable EPROM; 512 bytes of RAM; 15 bytes of dual-port RAM; an 8-bit, a 16-bit, and two PWM timers; and a serial port. The controller also offers 27 interrupt sources, 9 of which are external. These µCs cost less than $10 (OEM qty) and $17.45 (100). Samples of the 310, 320, and 330 devices are currently available.

Samples of the high-end 350 µC won't be available until later this year. The chip contains an 8-bit, 16-channel ADC; 32k bytes of masked ROM or one time-programmable EPROM; and 512 bytes of RAM. It features one 19-bit, two 16-bit, two PWM, and six 8-bit timers. Under software control, you can configure these timers in many ways. This model offers 56 interrupts, 9 of which are external. Depending on quantity, these devices cost $15 to $25.

—Michael C Markowitz

Hitachi America, Semiconductor and IC Div, 2000 Sierra Point Pkwy, Brisbane, CA 94005. Phone (800) 448-2244.

Circle No. 734



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CIRCLE NO. 56

ADC betters predecessor in speed, sampling, and cost

The AD1674 pin-compatible ADC from Analog Devices includes a S/H amplifier and is four times faster than the company's AD574A converter. The guaranteed conversion rate of the $18 (100), 12-bit ADC is 10 μsec. In stand-alone mode, the device has the same interface requirements as the AD574A and AD674A converters; in full-control mode, slight control-timing modifications are required.

The ADC's internal S/H amplifier avoids problems that are common to other auto-zeroing amplifiers by performing secondary sampling at the output. The additional sampling reduces hold-mode settling time, resulting in a 1-μsec acquisition time, a full-power bandwidth of 1 MHz, and 12-bit performance over the −55 to +125°C temperature range.

The monolithic ADC also includes a 10V reference, a clock, and 3-state output buffers. The device's dc specifications include an integral nonlinearity of ±1/2 LSB and no missing codes at 12 bits. The company tests and specifies the device for ac performance. The converter has a minimum signal-to-noise and distortion ratio of 70 dB, a maximum total harmonic distortion of −82 dB, and a maximum intermodulation distortion of −80 dB.

The converter's power-supply requirements are either 5 and ±12V or 5 and ±15V. Bus access time is typically 75 nsec, 150 nsec max. The device uses laser-trimmed scaling and offset resistors to provide four calibrated input ranges: 0 to 10V, 0 to 20V, ±5V, and ±10V.

The converter is available in five different grades specified over three temperature ranges of 0 to 70°C, −40 to +125°C, and −55 to +125°C. The converters come in 28-pin plastic DIPs and SOICs and 28-pin ceramic DIPs.

Old vs new: AD574A and AD674A standard features

Features	AD574A	AD674A
Maximum conversion time	35 μsec	10 μsec
Resolution	12 bits	12 bits
Internal S/H Amplifier	No	Yes
Minimum signal/noise + distortion ratio	Unable to specify	70 dB
Package	28-pin DIP and SDIC	Pin and package compatible with AD574A
Maximum power consumption	725 mW	575 mW
Price (100)	$22.60	$18

—Anne Watson Swager

Analog Devices Inc, 181 Ballardvale St, Wilmington, MA 01887. Phone (617) 937-1428. FAX (617) 326-8703.

Circle No. 731

ASK EDN

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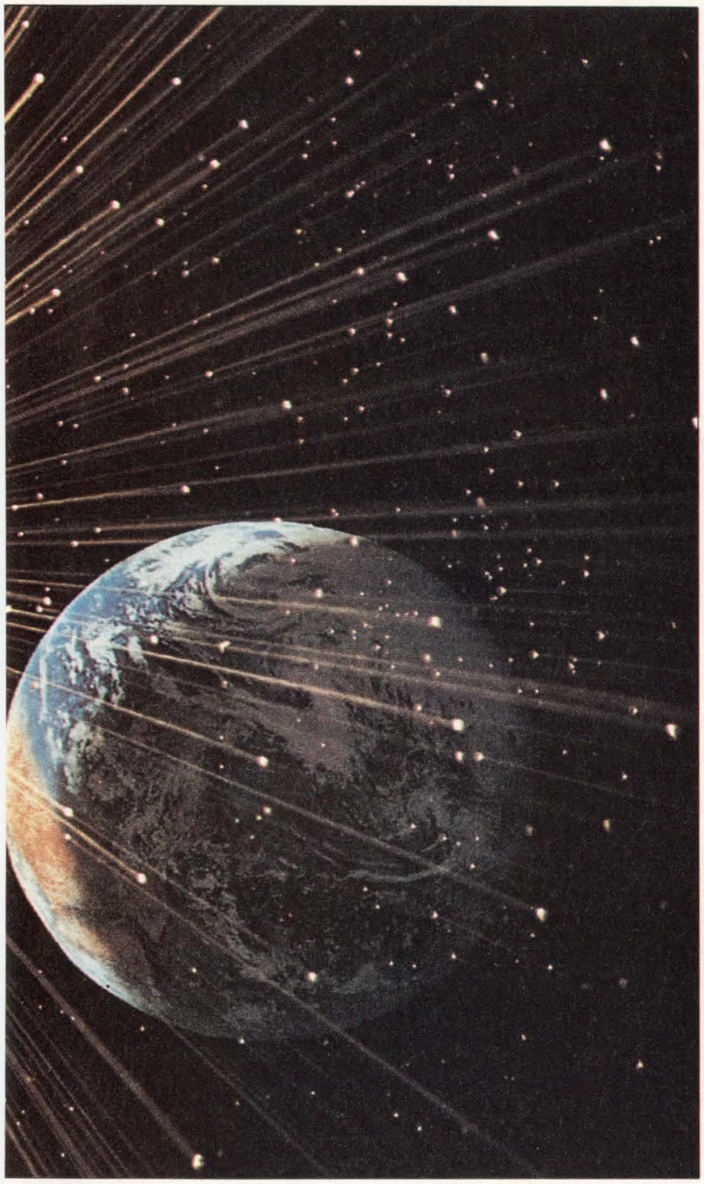

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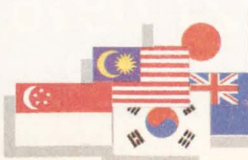

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CIRCLE NO. 68

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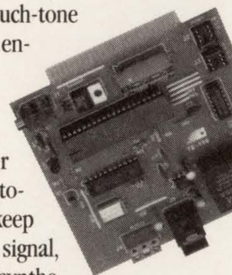
TE-158: $190.00



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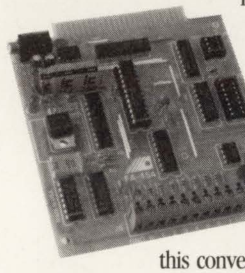

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NEC

CIRCLE NO. 71

CACHE DESIGN

Most high-performance systems can benefit from cache memory. However, designing one isn't trivial; to avoid wasting your precious cash, you need to know how and why the cache works.

Michael C Markowitz, Associate Editor

Deciding how to implement a cache is like buying a car: after you decide which car, you have to choose the color, leather or cloth upholstery, power or crank windows, whether you want a big engine or better economy, and more. Like buying the car, your cost *and* the system's performance is highly dependent on your selections.

A cache is a small, fast, and, therefore, more expensive memory that acts as a buffer between a device that uses large amounts of memory and its large, slow, and less expensive main memory. The cache's purpose is to reduce average memory-access time. This reduction is achieved by maximizing the probability of finding a memory reference in the cache (the hit rate), minimizing the access time to information that is in the cache, and minimizing the penalty of accessing data that is not in the cache. Generally, caches fit between CPUs and main memory; however, they can also operate between main memory and the computer's disk drives (see **box**, "Caches crush disk access times").

Caches are effective because of two properties of software programs: spatial and temporal locality. Spatial locality asserts that because programs are generally composed of subroutines and procedures that execute sequentially, they often use data and instructions whose addresses are proximate. Temporal locality recognizes that since many programs contain loops and manipulate data arranged in lists and arrays, recently used information is more likely to be reused than older information.

Since a cache operates by anticipating data- and instruction-location accesses in memory, you would expect that large caches offer greater performance than small caches. Generally this is true; however, several factors may blunt or invalidate the gains expected by increasing cache size. First, you can expect diminishing returns as you incrementally increase the size of your cache. Where adding a 16k-byte cache might offer dramatic performance improvement over a system with no cache, doubling the cache to 32k bytes could add only half as much performance (**Table 1**). Then, application software and architectural considerations may limit the gains of a cache.

Consider how the μP and the cache work with the memory subsystem during read operations. Without a cache, when the μP needs data, it makes a request to the dynamic RAM (DRAM). It then waits while the DRAM (whose 65-nsec access times are considered high speed) accesses the data and puts it on the bus. With a cache, the μP asks 10 to 25-nsec static RAMs (SRAMs) for the data. The cache controller checks to see

Speed through designs with superfast cache memories. (Photo courtesy Intel Corp; art direction by Peter Morgan; photography by Rick Wahlstrom Photography)

if the cache-data SRAM has the data. Tags, or partial addresses stored in the cache-tag SRAM, tell the cache controller whether or not the cache contains the requested data. If the data is in the cache—a hit—the controller sends the data to the μP. If the data isn't in the cache—a miss—the μP must get it from the DRAM.

Caches can wait for the cache controller to indicate a miss before instigating a DRAM access. These serial caches are called look-through caches. Alternatively, parallel, or look-aside, caches access DRAM and cache-data SRAM concurrently. If the controller finds its data in the cache, it aborts the DRAM access cycle. Look-aside caches are easier to

A cache subsystem consists of a memory to store data, a way to catalog the data, and a controller that acts as a traffic cop.

design and offer faster memory-subsystem performance, but tie up the memory bus during all memory accesses. As a result, DMA and other attempts to use the memory must stall the CPU. Look-through caches pay higher cache-miss penalties and are more complex, but they only use the memory bus during cache misses. If your cache has a hit rate of more than 90%, these penalties may be a minuscule por-

Caches crush disk-access times

Accessing information from a hard disk takes tens of milliseconds, where main-memory reads take hundreds of nanoseconds. Therefore, a disk cache can greatly improve system performance, especially in I/O-intensive system applications and in systems with small main memories. In designing a system, you must match your disk subsystem and cache design to your choice of operating system, host bus, and host architecture.

You can choose to add a disk cache in several forms. You can use SCSI- or IDE-disk drives that include embedded controllers and typically include a cache on the controller. Some manufacturers of intelligent SCSI host-bus-adapter boards include a cache. Likewise, manufacturers offer caching host-bus-resident controller boards for device-level-interface St-506/412 and ESDI drives. And you can choose to dedicate a portion of your system's main memory as a disk cache.

SCSI and IDE drives use 32k- to 256k-byte read-ahead caches to prefetch data that the system will likely request soon. The onboard controller simply continues to read sequential data after satisfying a system I/O request and therefore depends on the theory of spatial locality to operate efficiently. Quantum Corp (Milpitas, CA (408) 432-1110) pioneered the idea of an on-drive cache and offers among the most comprehensive on-drive cache designs.

You can create more than ten active cache segments on Quantum drives via an operating-system driver—essentially the equivalent of making a main-memory cache set-associative. Multiple segments ensure a greater hit rate in multitasking systems. Quantum's drives can also continue to prefetch data while servicing an I/O request from previously cached data. The drives use a least-recently-used algorithm to flush data when segments become full.

A cache-based drive can respond to a read request in less than 5 msecs on hits compared with typical seek and latency delays of 20 to 50 msecs on misses. Companies such as Data Technology (Milpitas, CA (408) 262-7700) perform similar prefetch operations with its host-resident controller boards for use in IBM-compatible PCs. The company's boards use an algorithm that evaluates recent disk accesses to predict whether future accesses are sequential or random.

You do not need a special operating-system driver for better performance from caches on drives, controller boards, and host adapter boards. But, all of these techniques require a 1- or 2-stage movement of data from the cache to main memory. In all three cases, the data is transferred across a system bus. SCSI-based systems must also transfer data across the SCSI bus, incurring delays from bus arbitration and the data transfer. Such caches, therefore, eliminate the electromechanical delays of disk drives, but still suffer from some overhead.

Main-memory caches simply set aside a partition of memory for disk caching. Such caches typically don't perform prefetch operations, but operate on the temporal-locality theory that the system will request once-used data again. Caches in main memory incur the least overhead on hits because retrieving the data requires only a memory-to-memory block move. But either your operating system or an application program must control a main-memory cache.

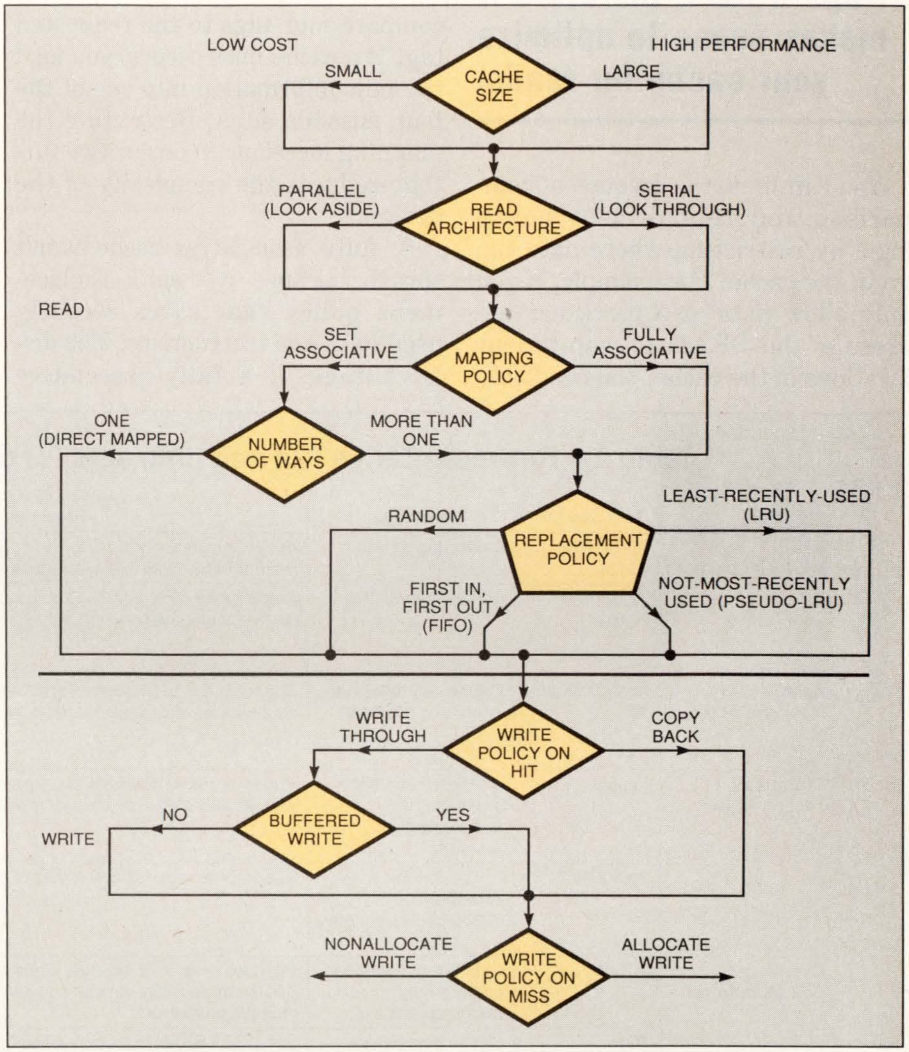
In IBM-compatible PC designs, you must consider the delays caused by a relatively slow system bus compared with an operating system that doesn't have cache support. Drive- and board-resident caches provide the simplest integration path and don't infringe on the limited 640k-byte main-memory map of MS-DOS. However, main-memory cache programs, such as PC-Kwik from Multisoft Corp (Beaverton, OR (503) 644-5644), can perform better and don't use much of your 640k bytes when run in expanded or extended memory.

The Unix operating system, conversely, includes a main-memory cache by design. And many Unix gurus believe that money for extra memory is best spent increasing main-memory size rather than adding auxiliary caches. Others think the combination of a drive-based cache with the main-memory cache provides the best performance, because the two caches operate differently.—*Michael C Markowitz and Maury Wright* tion of overall system performance.

If the data that the μP needs isn't in the cache, the microprocessor gets the data from slower main memory. Since temporal locality suggests that this data is likely to be needed again, while the CPU is accessing this data, the cache is also putting the requested data into its data SRAM. Spatial locality implies that nearby information will also be needed, so the cache also requests and stores several additional bytes of information. The cache needs to keep an inventory of its contents so that it can react the next time the processor asks for this data. The tag SRAM keeps the list of information by using a portion of the requested data's high-order address, called the tag.

The number of bits in the tag depends on how big the tag RAM is, how big the cache is, and the block or line size of the cache. A block, or line, is the minimum number of bits of code or data that move between main memory and cache during a transfer. Although spatial locality recommends larger block sizes, your design must balance the block size against the time and bandwidth it takes to transfer the data on the memory bus.

In order to indicate a match, logic



Designing a cache requires many decisions. This flowchart elucidates the major decision; however, you don't need to follow it explicitly.

compares each tag to the appropriate bits from the requested data. The amount of comparison logic depends on the cache's mapping policy. Allowing any block of data to map to any location in the cache demands that you compare each block's tag to the requested tag. As a result, either you need a small cache, large block sizes, or fast comparison logic to build a cache that fully associates memory with the cache. In addition to the comparison logic, you also need logic to determine where the new data gets stored. The determination of which data to replace, called the replacement policy, determines which information in the cache is least valuable and can be overwritten by new information.

Comparison and replacement logic isn't the only consideration with mapping policy. At the other extreme from a fully associative cache is one that maps each location in memory to only one location in the cache—a direct-mapped (or 1-way set-associative) cache. If the system executes a program that loops between two addresses that map to the same cache location, every memory access will be a cache miss. As a result, the computer will thrash, continually overwriting data that the cache will actually need with data its algorithms think it will need.

Table 1—Cache hit rates

Cache configuration			
Hit rate (nearest %)	Cache size (bytes)	Associativity	Line size (bytes)
41	1k	Direct	4
73	8k	Direct	4
81	16k	Direct	4
86	32k	Direct	4
87	32k	Two-way	4
88	64k	Direct	4
89	64k	Two-way	4
89	64k	Four-way	4
89	128k	Direct	4
89	128k	Two-way	4
91	32k	Direct	8
92	64k	Direct	8
93	64k	Two-way	8
93	128k	Direct	8

Read operations occur more frequently than write operations, therefore it makes sense to optimize your cache for reads.

You can limit the amount of comparison and replacement policy logic by restricting where data can go in the cache. For example, if you only allow data at a particular address in the DRAM to map to four locations in the cache, you need only compare four tags to the requested tag. If a cache miss occurs, you load the new information into one of the four possible sites. Restricting the mapping locations to one or two further reduces the complexity of the design.

A fully associative cache won't thrash because it uses a replacement policy that saves recently used data and instructions. The disadvantage of a fully associative cache is its cost. A cache that minimizes thrashing, but doesn't use as much comparison logic, restricts data in memory to a finite number of banks, called ways, in the cache. Generally, the performance improvement of building a system containing more than four ways is not worth the added complexity of the design. A 2-way set-associative cache allows each location in memory to map to two locations in the

Table 2—Representative ICs and chip sets for cache-based systems

Company	Part number	Part type	Features	Cost
AT&T Microelectronics	7C180 and 7C174	Cache-tag SRAM	4k×4-bit memory with 10- to 25-nsec access times. 8k×8-bit memory with 12- to 25-nsec access times.	$22.85/$28.10 (100) for 10/12 nsec DIPs
	7C183 and 7C157	Cache-data SRAM	8k×16-bit memory with 25- to 45-nsec access times. 16k×16-bit latched, self-timed memory with 20-to 33-nsec access times.	$22 (100) for 25-nsec DIPs $74.90 (100) for 20-nsec PLCCs
Austek Microsystems	A38202SX and A38202	Cache controller with integrated tag RAM	Supports 16k- to 64k-byte (SX) or 32k- to 128k-byte, two-way set-associative or direct-mapped, write-through caches.	$31.74 (1000) for 20-MHz A38202SX $57.01 (1000) for 33-MHz A38202
Chips and Technologies	Peaksx	Chip set with cache controller for 80386sx-based systems	Supports 16k or 32k bytes of cache with a programmable two-way set associative or direct-mapped, write-through cache.	$69 (1000)
	Peak/DM	Chip set with cache controller for 80386-based systems	Supports as much as 256k bytes of direct-mapped cache.	$64 (1000) for 25-MHz set $78.20 (1000) for 33-MHz set
Cypress Semiconductor	7C604	Cache tag, controller, and memory-management unit	Provides control for 64k-byte direct-mapped cache for Sparc. 604 is uniprocessor version and 605 (due late '91) supports multiple processors.	$431 (100)
	7C157	Cache data SRAM	16k×16-bit SRAM that offers a self-timed write mechanism and latched data inputs and outputs.	$83 (100)
Elite Microelectronics	Eagle	Chip set with cache controller and tag RAM for i386- and i486-based systems	Supports 32k to 128k bytes of two-way set-associative or direct-mapped, buffered write-through cache. Also includes DRAM controller for efficient DRAM refresh and memory access.	$168 (1000) for 33-MHz set
Eteq Microsystems	Cougar	Chip set with cache controller and tag RAM for i386- and i486-based systems	Supports 16k to 512k bytes of direct-mapped, buffered write-through cache. Also includes DRAM controller for efficient DRAM refresh and memory access.	$33 (1000) for 33-MHz set
Fujitsu Microelectronics	MB8299-25	SRAM	32k×9-bit SRAM with 12-nsec output enable access time, 25-nsec memory access time.	$17.50 (10,000)
Integrated Device Technology (IDT)	71589	Cache-data SRAM	32k×9-bit SRAM that offers a burst mode that can be synchronized to the CPU, and a synchronous write capability.	$79.25 (100) for 33-MHz version
	71B256, 61B298, and 71B258	BiCMOS SRAM	32k×8- and two 64k×4-bit SRAMs. 5- to 6-nsec output enable times and 12- to 15-nsec address access times.	$69.25 (100) for 15-nsec '256 $86.75 (100) for 12-nsec '298 and '258
Intel	82395SX and 82395DX	Integrated controller, tag and data SRAM	8k- (SX) and 16k- (DX) byte—cascadable to 64k bytes—four-way set-associative, cache that uses a pseudo-least-recently-used replacement policy and has a 16-byte line size.	$44 (1000) for 20-MHz SX devices $90/$109 (1000) for 25/33-MHz DX devices
Matra Design Semiconductor	C395e C395e/C415	i386- and i486-based chip set with controller and tag SRAM	Supports 32k- to 256k-byte and 128k- and 256k-byte, two-way set-associative, four-way set-associative, or direct-mapped caches with copy-back or write-through policies.	$60/$72 (10,000) for 25/33-MHz C395e sets $99/$119 (10,000) for 25/33-MHz C395e/C415 sets

cache. Similarly, a 4-way set-associative cache maps each memory location to four locations in cache. Conceptually, each way is a page, and each location in memory can map to only one location on a page.

Choosing which location on the page to map the data to is the function of the replacement policy. A 2-way cache often uses a least-recently-used (LRU) policy to decide which of the two memory locations to overwrite. An extra bit at each location tracks accesses and keeps the data that was most recently needed.

Guess which data you won't need

A 4-way set-associative cache offers more replacement alternatives. Random replacement is the simplest to implement, though using such a policy may violate temporal locality. First-in, first-out (FIFO) replacement stacks all of the information in the cache and deletes the oldest—even if it is the most recently used. A variation of the LRU policy, called not-most-recently-used or pseudo-LRU, recognizes the importance of temporal locality and the logic efficiency of random replacement by tracking and protecting the most recently used information and randomly overwriting the information at the appropri-

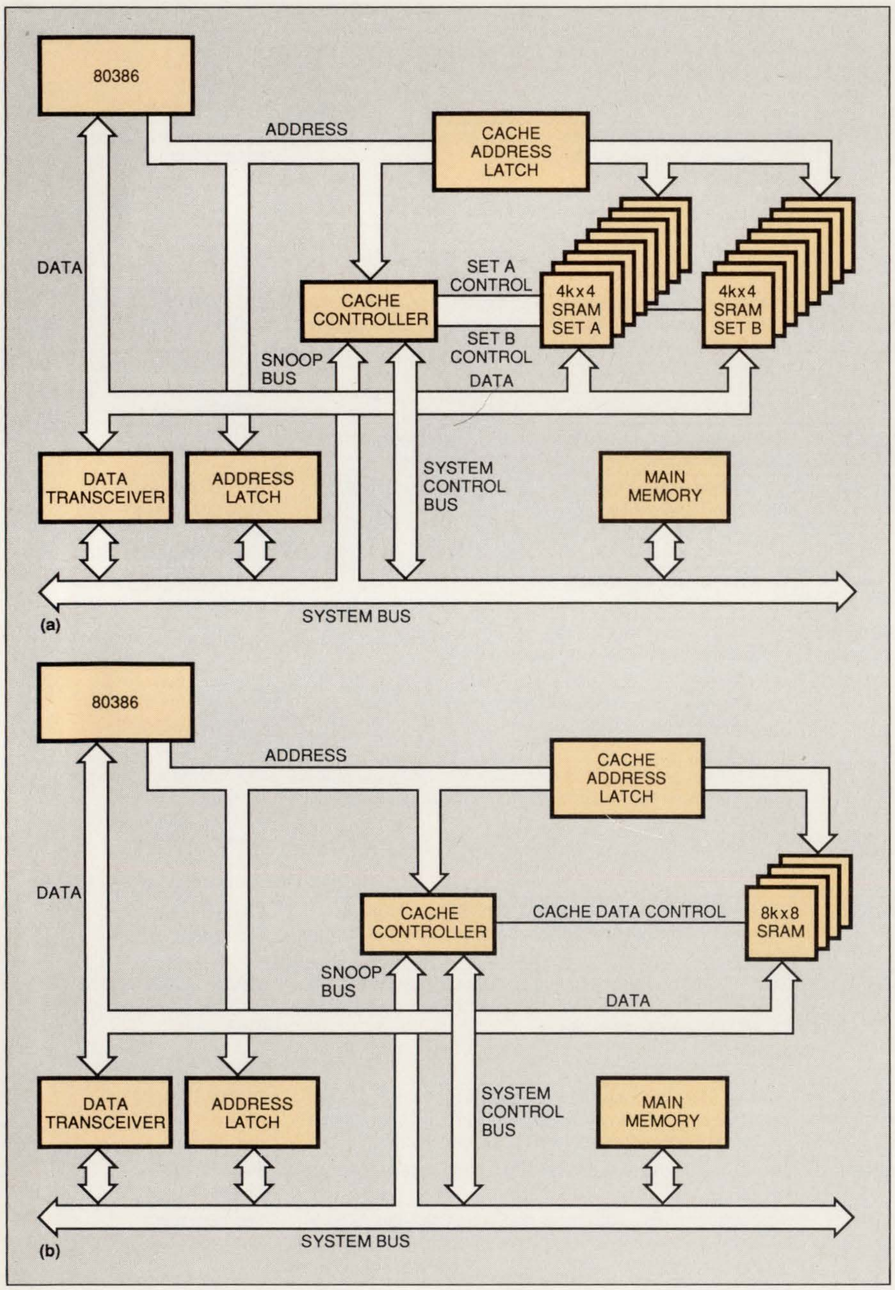
Company	Part number	Part type	Features	Cost
Micron Technology	56C0816 and 56C2818	i386- and i486-compatible cache-data SRAM	8kx16- and 8kx18-bit SRAMs that include address latch and multiplexing between two RAM banks.	Sample pricing: each $15/$17 (100)
Mitsubishi	M5M51014, M5M51001, M5M5159, and M5M5180	SRAM	25-nsec, 1Mx4-bit SRAM, available in June. 25-nsec, 1Mx1- or 256kx4-bit SRAM. June delivery. 15-nsec, 64kx4-bit SRAM with OE. June delivery. 20-nsec, 8kx8-bit SRAM with OE.	$85 $85 $25 $10
Mosel	MS441	Integrated cache controller for i386- and i486-based systems	Uses two concurrent 386/486 bus controllers along with dual-port memories to allow background write back while read and write cache hits continue. Supports 2k-block, 64k-byte, two- or one-way set associative cache.	$65 (10,000) for 25-MHz i386-compatible controller $114 (10,000) for 33-MHz i486-compatible controller
	MS443	Dual-port burst SRAM	16kx9-bit, dual-port SRAMs with parity, input and output registers to buffer bursting and memory accesses.	$9 (10,000)
Motorola	62486, 62940, and 62950	Application-specific SRAM	32kx9-bit memories for memory subsystems for 80486, 68040, and Sparc microprocessors.	$57.20 (500) for 14-nsec 62486 and 62940 $40.12 (500) for 17-nsec 62960
	4180	Cache-tag SRAM	4kx4-bit 18-nsec tag SRAM.	$10.40 (500) for 18-nsec devices
NEC Electronics	46710 and 46741	BiCMOS SRAM for R3000-based systems	8kx20-bitx2-bank and 16kx20-bitx2-bank memories with address latches and 15-nsec access times.	$45 (1000)
Quality Semiconductor	8885, 8886, and 8888	SRAM	All CMOS 16kx4-bit SRAMs with access times as fast as 10 nsec. '85 has 2 CSs, '86 offers OE; both with separate I/O lines. '88 has common I/O.	$30.54 (1000) for 10-nsec 8885/6 $33.75 (1000) for 10-nsec 8888
SGS Thomson	41S80, 48S74/80, and 4202	Cache-tag SRAM	4kx4-, 8kx8-, and 2kx20-bit memories with address-compare access times as fast as 12 nsec. Used to design 32k- to 128k-byte caches.	$13 (1000) for 12-nsec device $18.75 (1000) for 17-nsec device $37.50 (1000) for 20-nsec device
Silicon Connections	SC5204 and SC4109	SRAM and self-timed RAM	5204 is an 8-nsec, 256kx4-bit BiCMOS SRAM. 4108 is a 5-nsec, 8kx9-bit self-timed RAM. Both available third quarter of 1991.	$330 (1000) $257 (1000)
Texas Instruments	2155, 2163, and 2164	Cache-tag SRAM	2kx8- (2155) and 16kx5-bit-cascadable SRAMs with 3-state (2163) or open-drain (2164) Match output. The 2155 supports the 68030 burst-fill capability.	$19.58 (10,000) for 2155 $30 (1000) for 20-nsec 2163 $33 (1000) for 18-nsec 2164
Toshiba America	55187 and 55188	Cache-data SRAM	2kx8-bit SRAMs. Configurable for either direct-mapped or 2-way set-associative caches. Control logic for 2-way cache is on-chip. Memory access time of 20, 25, and 30 nsec.	$11 (1000) for 30-nsec device
	55B417 and 55B88	Cache-data SRAM	16kx4- and 8kx8-bit BiCMOS SRAMs with access times as low as 10 nsec.	$12/$14 (1000) for 12-nsec devices
VLSI Technology	82C325 and 82C335	Cache-controllers (these devices are part of 386SX- and DX-based chip sets)	Supports as much as 32k bytes (325) and 64k bytes (335) of cache memory with look-aside, write-through architectures. Implements 2-way set-associative cache with least-recently-used replacement.	$40/$50 (1000)

ate location on one of the other ways.

Where a 64k-byte direct-mapped cache might have an 80% hit rate, the hit rate rises to about 94% with a 64k-byte 2-way set associative cache and 98% with a 64k-byte 4-way set-associative cache, according to Michelle Larson, product marketing engineer with SGS-Thomson. These hit-rate improvements result from the ability of the different ways to maintain temporal locality.

Replacement, mapping, and look-through or look-aside architectures are all related to memory-read operations. Because in most applications, memory reads account for the majority of memory accesses, you are wise to prioritize your design to speed read operations. However, don't ignore memory writes.

If the data is in the cache when the CPU tries to write data to memory, you have two alternatives. The simplest approach is to write the data to both the cache and main memory. This write-through approach ensures data coherency between cache and memory. The penalty for using a write-through scheme is the wait states that the DRAM controller imposes as a result of the write operation. You can attenuate this penalty somewhat by using a buffer that writes the data from the cache to the memory, relieving the CPU of that responsibility.



Two-way set-associative caches (a) are more complex than direct-mapped caches **(b)**, and as a result, cost more. However, 2-way set-associative caches perform better.

Snooping maintains coherency

Copy back is a more complicated scheme for writing information to cache and main memory. This technique maintains a bit that stores the coherency of the cache and DRAM memory. If the data is inconsistent, or dirty, then whenever the cache controller decides to overwrite the dirty location, it must first copy the valid data back to the DRAM. Similarly, if another device requests the data from the DRAM, the cache controller must monitor, or snoop, the bus to copy back the dirty data to the DRAM before the DRAM supplies that data to the other device. (For a detailed discussion of snooping and cache coherency, see "Protocols keep data consistent," EDN, March 14, 1991, pg 41.)

Deciding what to do on a write operation that causes a cache miss is more difficult than deciding what to do when a write operation results in a cache hit. Temporal locality suggests that information read from a cache once is likely to be read again. Equivalency would suggest that an address recently written to is likely to be accessed again. However, reading recently written information is application dependent and is generally not as common as rereading memory locations you recently read. In addition, write operations consume a small percentage of a system's operating time.

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CIRCLE NO. 82

Caches that load themselves with written data on cache misses are called allocate write. To save logic, you can design a nonallocate-write cache, which doesn't load written data to cache on a miss. The incremental performance improvement of an allocate-write cache may not be worth the effort.

Overemphasizing reads is an effective strategy except when the CPU contains an onboard cache. These generally small caches, called primary caches, already intercept a large percentage of read requests. A secondary cache optimized for read operations is a superset of the on-chip primary cache. As a result, a secondary cache is somewhat redundant and provides a smaller return on your memory and cash investment.

Table 3—Wait-state profile of cache architectures

Operation	Look-aside	Look-through copy back	Look-through write through
Read hit	0	0	0
Write hit	System-memory wait states.	0	0, unless the write buffer is already full with a pending write.
Read miss (excludes line-fill cycles)	System-memory wait states.	System-memory wait states +1 due to an extra look-up cycle.	System-memory wait states +1 due to an extra look-up cycle.
Write miss	System-memory wait states.	0, unless the write buffer is already full with a pending write.	0, unless the write buffer is already full with a pending write.

Alternatively, a secondary cache optimized for write operations can boost performance of the portion of the cache's operation that the primary cache does little to improve. A cache technique under development by Mosel uses dual-port SRAMs and takes advantage of the burst-memory data access. The SRAMs, which will work with 80386- and 80486-based systems, facilitate building 64k-byte, 2-way set-associative caches. The memories operate by simultaneously latching all 128 bits in a 5-cycle, 16-byte burst using 7-nsec latches at

Caching branches reduces pipeline stalls

When designers at Advanced Micro Devices were designing the 29000 RISC µP family (the 29005 16-MHz device costs $50 (1000), they realized their transistor budget would allow them to implement a small cache on-chip. Because the processor has both an instruction bus and a data bus, they needed to decide whether to build an instruction or data cache.

They also realized that, because the processor uses instruction prefetching, it would perform better if they could prevent pipeline stalls. Combining the transistor budget with the need to eliminate stalls, the designers came up with a branch-target cache (BTC).

The BTC functions like a normal cache in that it stores data already in the dynamic RAM (DRAM). However, it differs by only storing the four instructions following a branch. If the branch was previously taken, the processor executes the branch in a single cycle.

When the processor executes a branch for the first time, the cache doesn't contain the succeeding instructions. It takes one cycle to execute the branch from memory and five cycles to refill the instruction pipeline. AMD claims a 60% hit rate for the 512-byte BTC on the 29000.

The BTC is organized as a 2-way set-associative cache. Each way comprises sixty-four 32-bit words divided into 16 blocks of four words each. These four words define a branch target entry. Each block is associated with one 28-bit cache tag. The tag includes 26 bits derived from the address and two bits, called the Space ID, that indicate whether the instructions were fetched from instruction/data memory or from read-only memory and whether the instructions were fetched in user or supervisor mode. Finally, each word in the cache has an associated valid bit that indicates the instruction's validity.

After a branch, the address of the fetched instruction selects a line to store the instruction sequence of the branch, if that branch instruction sequence isn't in the BTC. The processor uses a random replacement scheme based on the processor clock to choose which set to replace. The processor then sets the address tag and the space ID to properly describe the instructions being stored in the cache before loading the instructions into the cache.

BTCs are more efficient than conventional caches when the caches are smaller than about 1k byte, according Dr Mark Hill (**Ref 1**). Conversely, Hill says that conventional caches are preferable when larger than 8k-bytes. He further says that intermediate-sized BTCs and conventional caches offer comparable performance.

the input and output of the memory array. The memories will be available in the third quarter of 1991.

Caches speed sequential writes

The dual-port memories boost performance on a write miss. The miss causes a burst allocate-write cycle that fills the secondary cache with 16 sequential bytes of data. If the next write is to the next memory location, that data will already be in the cache. According to statistics compiled by Mosel, 70% of write operations are sequential. Further, 50% are at least three sequential writes. The company expects its technique to provide write hit rates exceeding 99% while maintaining read hit rates higher than 96%.

After designing your cache, you can evaluate its effectiveness using a trace-driven cache simulator. Two such simulators, written by Professor Mark Hill of the University of Wisconsin Computer Sciences Department, are tycho and dineroIII, which are quasi-shareware packages available on the EDN bulletin-board system (BBS). Both C-based simulators use the same ASCII trace format.

After you create a list of memory references from an executing applications program, you use the list to drive the simulators. In response, the simulators report the behavior of one or more alternative cache designs.

Both simulators evaluate uniprocessor caches. Tycho allows simultaneous evaluation of many alterna-

Manufacturers of cache SRAMs and controllers

For more information on the ICs and Chip sets to implement caches such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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tive caches; dineroIII only evaluates one cache per simulation run. The simulators also differ in their capabilities. Tycho is a more restrictive simulator in that all caches in a simulation must have the same cache size, don't prefetch data, and use least-recently-used replacement. DineroIII allows you to vary more cache design options, such as write-back vs write-through, random vs least-recently-used replacement, and demand fetching vs prefetching.

The simulators have been distributed to both commercial and academic sites. You can obtain copies of either or both simulators either by contacting Mark Hill directly, or via the EDN computer bulletin-board system (BBS). (Phone (617) 558-4241 with modem settings 300/1200/2400,8,N,1. Access */freeware* SIG and specify *(r)ead* option followed by *(k)ey-word* search for "SR #425".) Professor Hill asks for, but does not require, a $500 donation to the University of Wisconsin to support his continuing research.

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Reference

1. Hill, MD, "Aspects of Cache Memory and Instruction Buffer Performance," PhD dissertation, Computer Science Div, UC Berkeley, November 1987.

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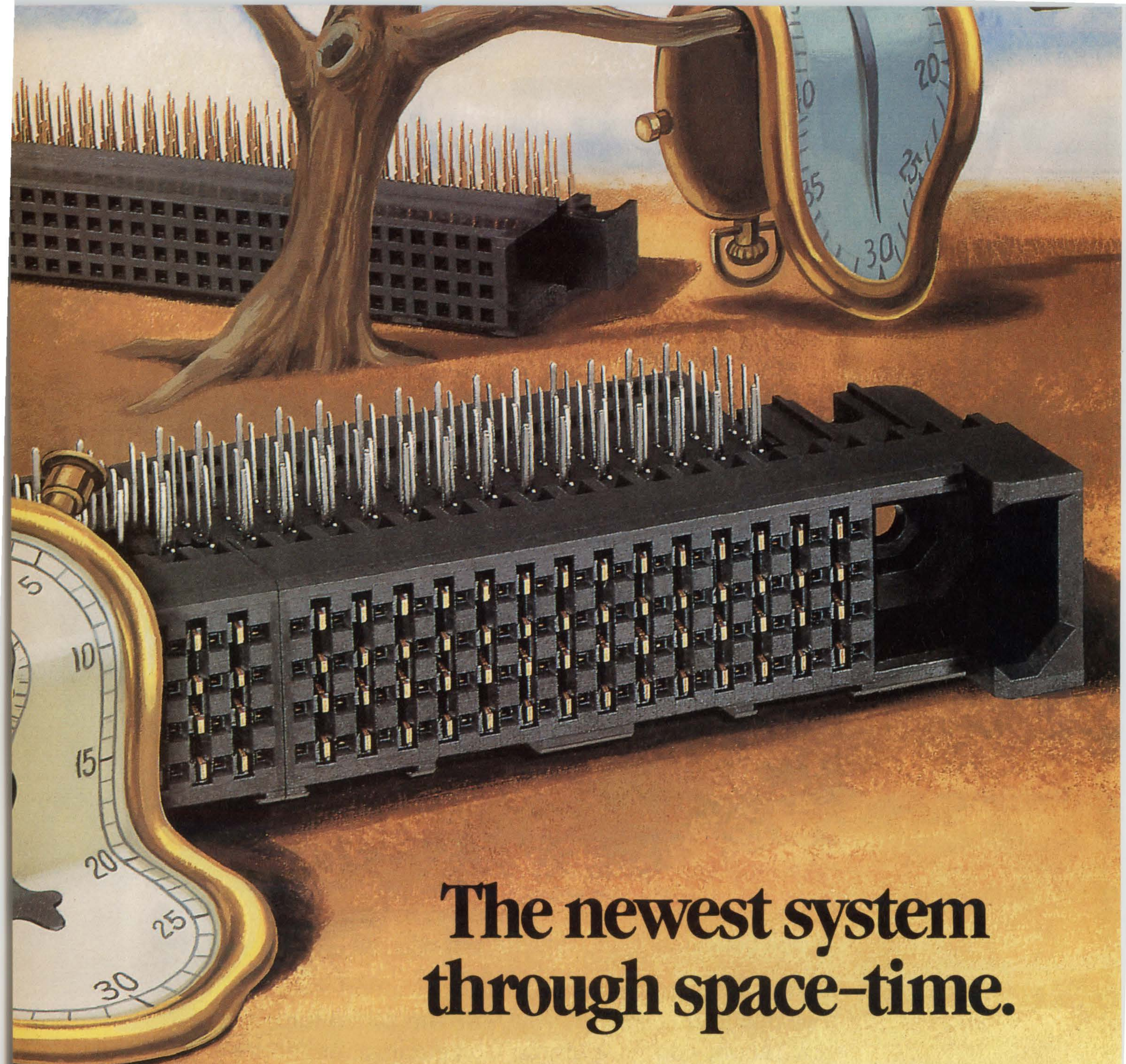
WHAT'S NEXT

The number of linear ICs tailored to operate from a single power-supply voltage has dramatically increased in the last few years. Look for our Special Report in the May 9, 1991, issue and catch up on the developments in single-supply, analog-design techniques and applications.



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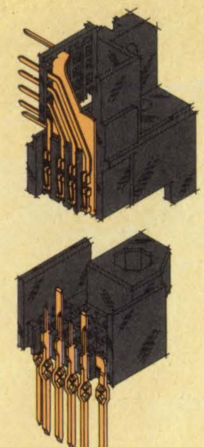

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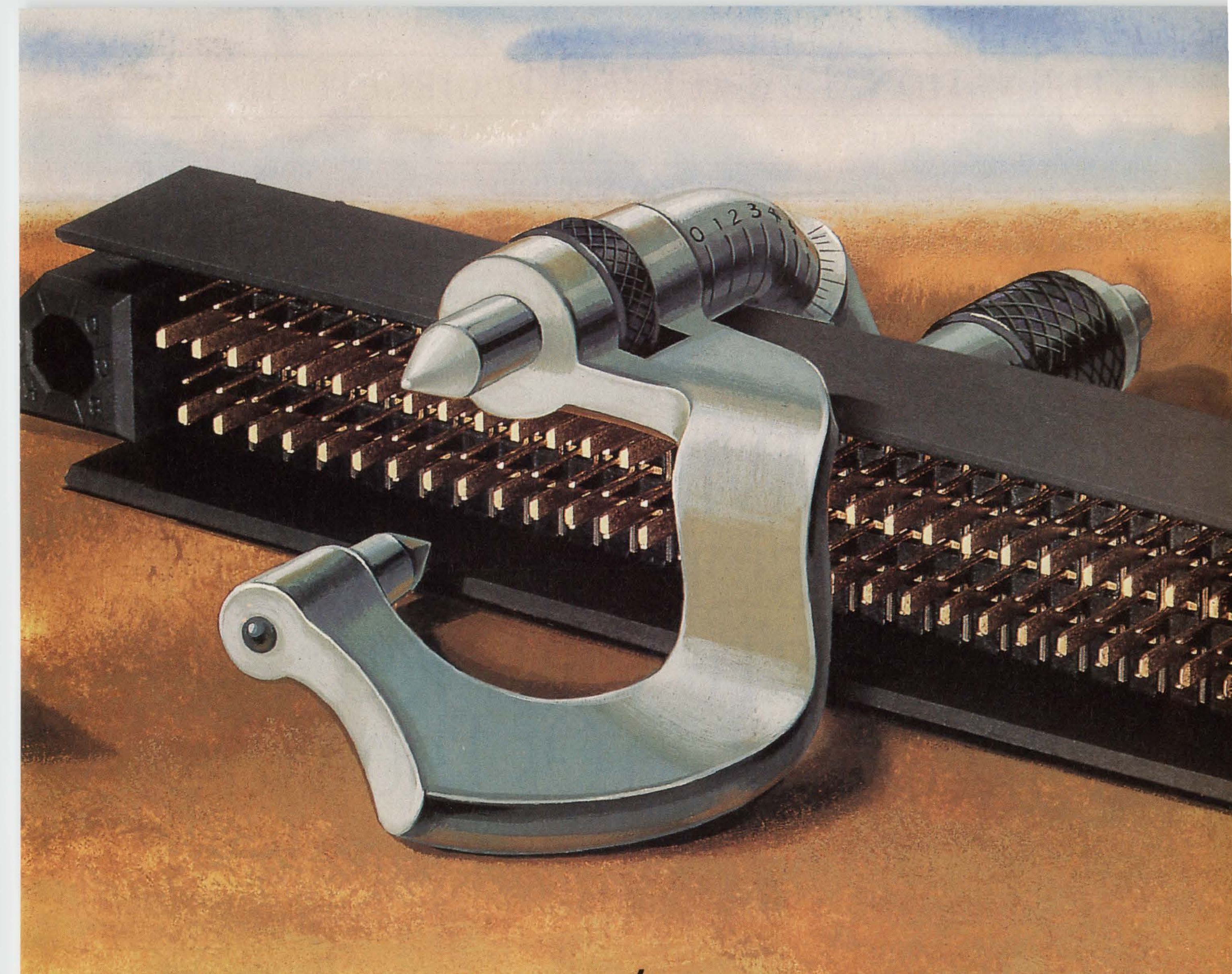

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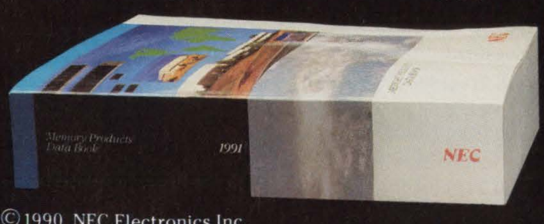

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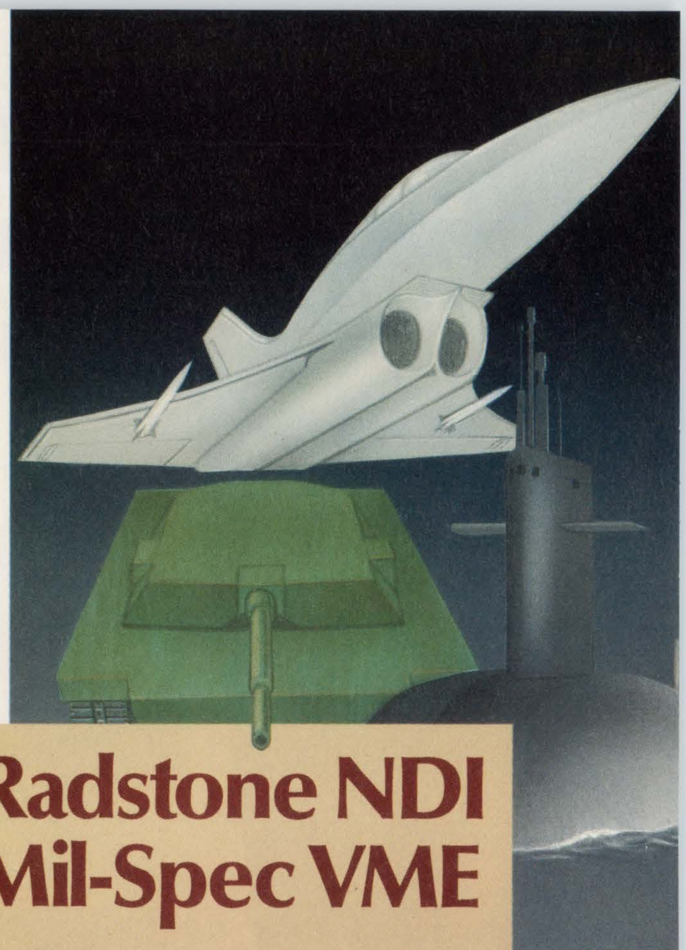

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EDN DESIGNERS' GUIDE TO

subranging ADCs
part 2

Dynamic specifications describe performance of subranging ADCs

Part 1 of this 3-part series on subranging A/D converters covered the architectures and operation of these specialized devices. Part 2 continues with a discussion of their critical dynamic parameters and specifications. Part 3 will conclude the series with a discussion of test and measurement principles.

Ray K Ushani, *Datel Inc*

In the world of high-speed data-acquisition components, the conventional dc parameters are not sufficient to specify the performance of A/D converters. Under dynamic conditions, an ADC's transfer function may exhibit large errors even though the dc test results appear close to the ideal limits. This disparity is especially common in digital-signal-processing applications.

In practice, no single specification or test can completely characterize a high-speed A/D converter's performance under dynamic conditions. Therefore, ADC users and designers should comprehend the significance of every dynamic specification. In all, there are nine dynamic parameters you should understand before attempting any test techniques. These parameters include quantization error, the signal-to-noise ratio, harmonic and intermodulation distortion, and the differential phase and gain.

Quantization maps the analog input range into 2^N digital words. Because the best resolution attainable from an analog input signal is 1 LSB, an infinite number of points are identifiable between any adjacent code centers (**Fig 1**). As a result, quantization causes an error of ± 0.5 LSB max.

Quantization is an irreversible process. Once an ADC quantizes a signal, the signal's original analog information is lost forever—an occurrence comparable to what happens to an analog signal in the presence of white noise. Because of this similarity, many engineers refer to quantization error as quantization noise.

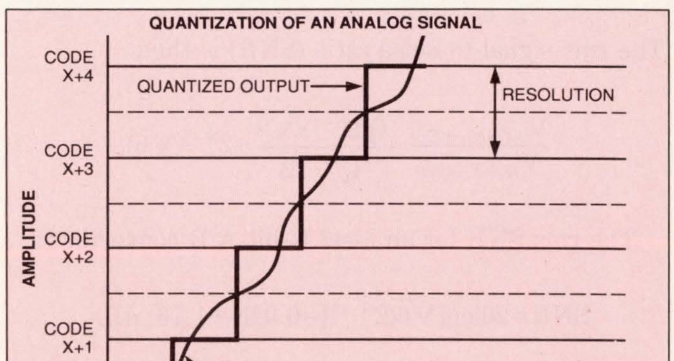


***Fig 1—Quantization maps the analog input range** into 2^N digital words. This process results in a quantization error of ± 0.5 LSB max.*

In applications such as high-speed data-acquisition systems, the dc parameters of an A/D converter are not sufficient to specify the device's performance.

Because the quantization error (QE) is as often positive as negative, its average value is precisely zero, which gives no information about the size of the error. A more meaningful measure is the quantization error's root-mean-square value. The following relationships let you calculate the maximum rms quantization noise ($V_{NOISE\ (RMS)}$):

$$QE=\frac{V_{IN}(I)-IQ}{Q},\ IQ-\frac{Q}{2}\leq V_{IN}(I)\leq IQ+\frac{Q}{2}$$

$$QE_{RMS}=\sqrt{\frac{1}{Q}\int_{IQ-\frac{Q}{2}}^{IQ+\frac{Q}{2}}\left(\frac{V_{IN}(I)-IQ}{Q}\right)^2 dV_{IN}}$$

$$=\sqrt{\frac{Q^2}{12}}$$

$$V_{NOISE\ (RMS)}=\frac{Q}{\sqrt{12}},$$

where Q = LSB weight, QE(I) = Ith code quantization error, and $V_{IN}(I)$ = input range that produces code I.

In an actual A/D converter, the quantization band for certain codes can be significantly larger or smaller than ideal. Nonideal quantization bands represent differential nonlinearity errors.

For a signal with a peak amplitude of $Q(2^N)$ that an N-bit ideal converter quantizes, the maximum rms sine-wave value is

$$V_{SIGNAL\ (RMS)}=\frac{Q(2^{N-1})}{\sqrt{12}}.$$

The rms signal-to-noise ratio (SNR) is then

$$\frac{V_{SIGNAL\ (RMS)}}{V_{NOISE\ (RMS)}}=\frac{Q(2^{N-1})/\sqrt{2}}{Q/\sqrt{12}}=2^{N-1}(\sqrt{6}).$$

The rms SNR for an ideal N-bit A/D converter is

$$SNR=20\log[\sqrt{6}(2^{N-1})]=6.02N+1.76\ \text{dB}.$$

However, for an actual A/D converter, calculate the SNR as follows:

$$SNR=-20\log\sqrt{10^{-SNRWD/10}+10^{+THD/10}},$$

where SNRWD is the SNR without distortion and THD is the total harmonic distortion, both in decibels.

Because most of the noise in an A/D converter appears at the harmonic frequencies, the SNR plus distortion is a good estimate of the total harmonic distortion. Furthermore, SNR is the cumulative effect of many error sources such as quantization error, missing codes, integral and differential nonlinearities, total harmonic distortion, aperture uncertainty, and noise. Because of these myriad contributions, SNR is the primary figure of merit in applications such as radar and signal-detecting systems.

The effective-bits (EB) value is the number of bits an ideal A/D converter requires to yield the SNR previously calculated for an ideal N-bit converter:

$$EB=\frac{SNR-1.76}{6.02}.$$

The effective-bits value is a global description of the ADC's dynamic performance. It provides a general measure of how much the ADC's nonlinearity impairs its overall usefulness at a given input condition. If the quantization noise is uniformly distributed and the quantization errors from sample to sample are statistically independent, the expression for effective bits is

$$EB=\log_2\left(\frac{\text{full-scale volts}}{\sqrt{12}\ E_{RMS}}\right),$$

where E_{RMS} is the error of the digitized signal.

Harmonic and intermodulation distortion

The output signal of a linear device differs from its input signal only in amplitude when you measure the signals in either the time or frequency domain. Any nonlinearity a device introduces will manifest itself as a deviation from the sinusoidal response in the time domain or as new frequencies in the frequency domain. This nonlinearity is distortion.

When an ideal A/D converter with infinite resolution digitizes an ideal sine wave, the digital output fully represents the original sine wave with no distortion at any frequencies. Looking at the discrete-Fourier-transform (DFT) amplitude spectrum of such an output, you can observe a sharp peak at the input frequency. At any other frequency the amplitude will be zero. However, in the case of an actual A/D converter, the amplitude spectrum also contains peaks at integer multiples of the fundamental frequencies. These peaks

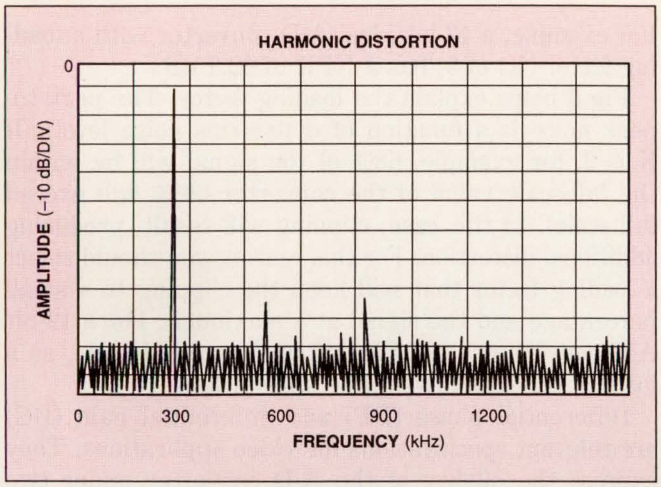


*Fig 2—**This harmonic-distortion plot** shows the fundamental frequency at 300 kHz with harmonics present at 600, 900, and 1200 kHz.*

represent harmonic distortion **(Fig 2)**. From these peaks, you can calculate the percentage of total harmonic distortion (THD) using the following relationships:

$$THD=\sqrt{\sum_{n=2}^{\infty}(HD_N)^2}\times 100\%$$

$$HD_N=10^{-(PEAK\ N)/20},$$

where peak N is the Nth-harmonic distortion peak, and the harmonic distortion (HD_N) is equal to the amplitude of the signal at the Nth harmonic divided by the amplitude of the signal at the input frequency.

For an A/D converter, you can calculate THD in decibels as follows:

$$THD=20\log\sqrt{\sum_{n=2}^{\infty}(HD_N)^2}.$$

The integral nonlinearity of the A/D converter's transfer function can also cause intermodulation distortion (IMD). IMD is the change in one sinusoidal input that the presence of another sinusoidal input at a different frequency causes. For example, let the input of the A/D converter be the sum of two sinusoids with equal amplitudes but different frequencies: $\sin\omega_1 \pm \sin\omega_2$. Not only will harmonic distortion occur at $N\omega_1$ and $N\omega_2$, but harmonics will also appear at

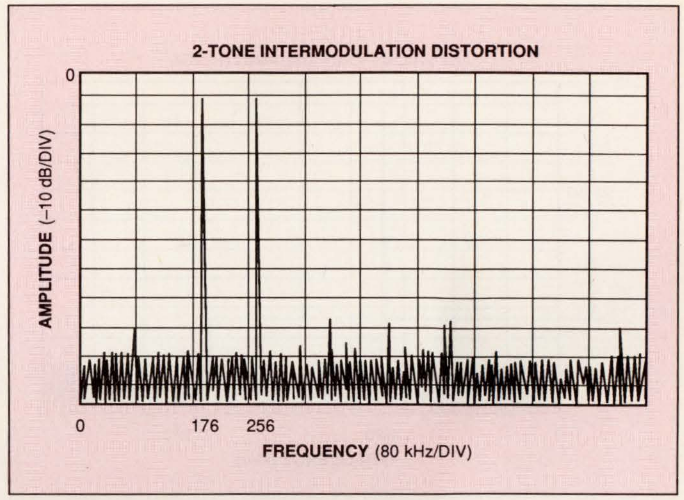


*Fig 3—**This plot of 2-tone intermodulation distortion** shows fundamental frequencies at 176 kHz (F_1) and 256 kHz (F_2). Note the presence of distortion products at 80 kHz (F_2-F_1) and 432 kHz (F_2+F_1).*

$N\omega_1 \pm K\omega_2$, where N and K are any integers **(Fig 3)**. This IMD interaction between input sinusoids is significant in both audio and RF-communications applications. The value, in decibels, for the intermodulation distortion when N=1 and K=1 is

$$IMD\ (\omega_1\pm\omega_2)=20\log\frac{\text{amplitude at } \omega_1\pm\omega_2}{\text{amplitude at } \omega_1 \text{ (or } \omega_2)}.$$

When the input sinusoids are not of the same amplitude, IMD=20log(rms value of the sum and difference distortion products ÷ rms value of the fundamental frequencies).

Spurious-free dynamic range

The spurious-free dynamic range (SFDR) is analogous to the dynamic range for slow, high-resolution A/D converters. As the name implies, SFDR is the range in the amplitude spectrum where no frequency components other than the fundamental exist **(Fig 4)**. SFDR expresses the peak distortion of an A/D converter and is a measure of the device's dynamic range under different input conditions. Mathematically, SFDR = the amplitude of the fundamental − the next highest frequency component, with all values in decibels.

The SFDR parameter is of primary importance for A/D converters in noisy receiver environments where the converter must digitize a small-amplitude signal.

Once an A/D converter quantizes a signal, the signal's original analog information is lost forever.

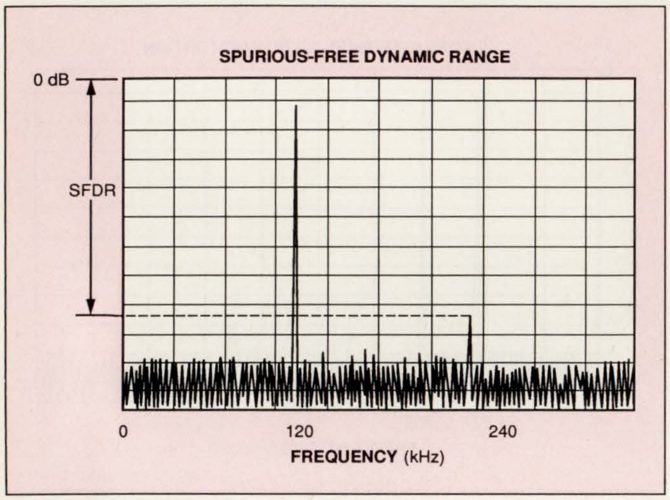


Fig 4—The spurious-free dynamic range *of an A/D converter is the range, in the amplitude spectrum, in which frequency components other than the fundamental do not exist.*

Noise/power ratio (NPR) is another indicator of an A/D converter's dynamic performance. NPR expresses the quality of an A/D converter in broadband frequency-domain applications, such as a multiplexed system. NPR is the ratio of the power of the reconstructed output at two different conditions for a particular frequency (f). The first condition is the full-scale input containing white noise. The second condition is the same input using a notch filter with a center frequency of f. The expression for NPR in decibels is

$$\mathrm{NPR}=10\log\left(\frac{\text{1st condition power}}{\text{2nd condition power}}\right).$$

The NPR caused by quantization noise for an ideal A/D converter is

$$\mathrm{NPR}=\frac{\text{full-scale volts of the ADC}}{\text{K (quantization noise)}}=\frac{Q\ (2^N)}{KQ/\sqrt{12}}$$

$$=\frac{2^N\ (\sqrt{12})}{K},$$

where Q is the quantization level, $Q/\sqrt{12}$ is quantization noise, N is the number of bits, and K is a loading factor equal to the full-scale volts divided by the rms noise level.

The NPR in decibels is

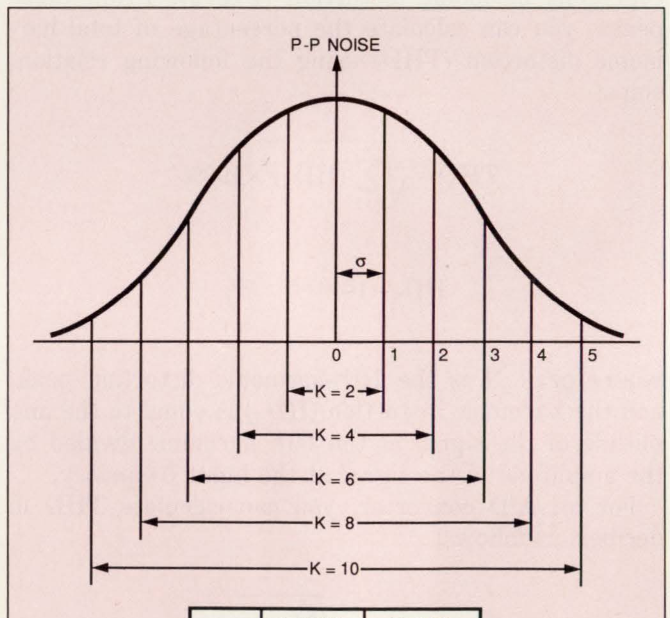
$$\mathrm{NPR}=6.02N+20\log\ (\sqrt{3}/K).$$

For example, a 12-bit ideal A/D converter with a loading factor (K) of 5, has a NPR of 62.7 dB.

Fig 5 helps explain the loading factor. The peak-to-peak noise is a function of σ (σ = rms noise level). If K is 2, for example, 68% of the signal will be within the full-scale value of the converter (32% will exceed full scale). In this case, clipping will result, producing additional distortion. For this reason, you should select a loading factor that will keep the clipping to a small percentage and the signal at a maximum. For a 12-bit A/D converter, the LSB is 0.0248% of full scale, so a loading factor of 8 would be appropriate.

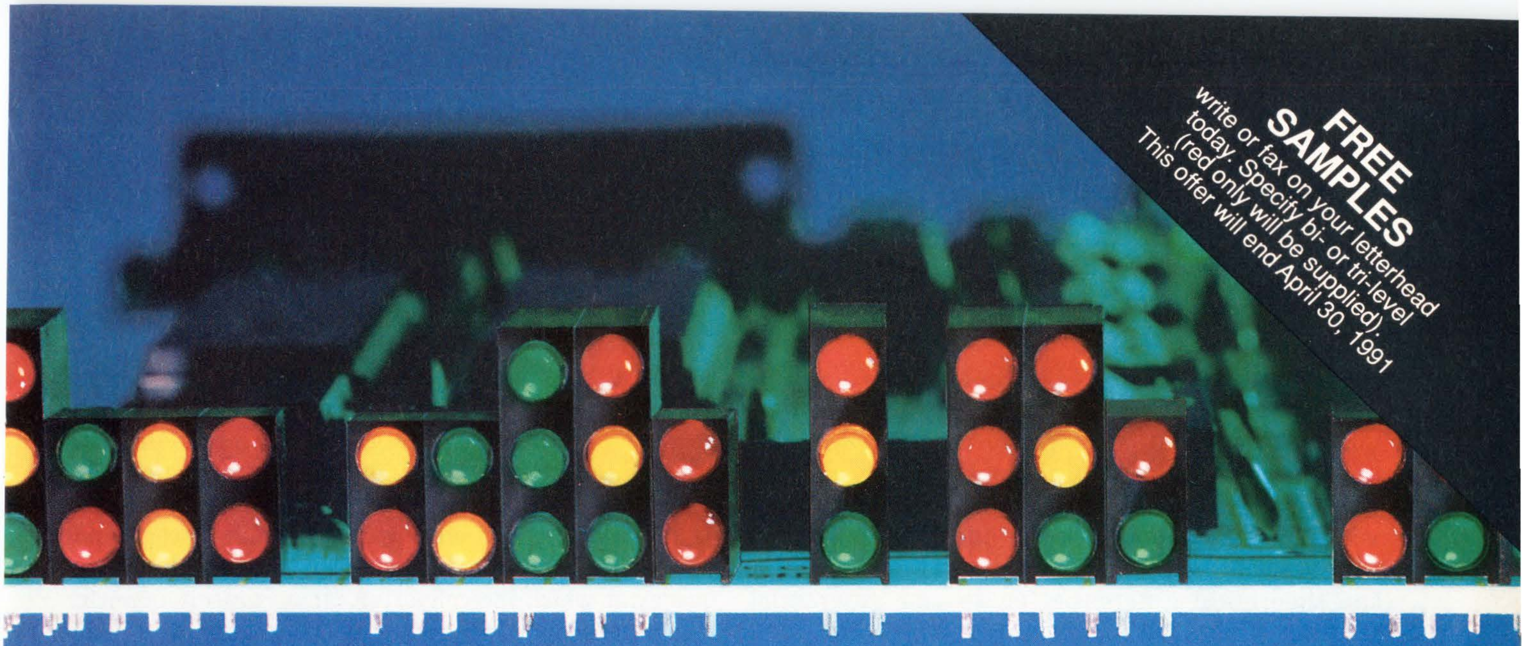
Differential phase (DP) and differential gain (DG) are relevant specifications for video applications. They express the quality of the A/D converter under two different input levels (usually one near zero and the other near full scale).

Differential phase is the difference in the output



K	SIGNAL OUT OF RANGE	SIGNAL IN RANGE
2	32%	68%
4	5%	95%
6	0.3%	99.7%
8	0.005%	99.995%
10	0.0003%	99.9997%

Fig 5—The peak-to-peak noise of an ADC *is a function of its loading factor (K) and statistical deviation (σ). If K is 2, 68% of the signal will fall within the full-scale range of the converter.*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Nonlinearity in the A/D converter's transfer function can cause both harmonic and intermodulation distortion.

phase of an A/D converter when a small, high-frequency sine-wave signal is superimposed on a low-frequency signal at two predescribed amplitudes. Differential gain is the ratio of the output amplitudes of an A/D converter with this small, high-frequency sine-wave superimposed on the low-frequency signal at the two predescribed amplitudes.

The theoretical differential phase and differential gain for an N-bit ideal A/D converter is

$$DP=\frac{Q}{A}\cdot\frac{2}{3}$$

$$DG=100\%\cdot\frac{Q}{A}\cdot\frac{2}{3}$$

$$Q=\frac{\text{full-scale volts}}{2^N}.$$

DP is the differential phase in radians (1 rad = 57°), Q is the LSB size in IRE (Institute of Radio Engineers) units, A is the amplitude of the subcarrier in IRE units, and DG is the differential gain in percent. For example, consider an 8-bit system converting a signal having a peak-to-peak value of 140 IRE units (1V): Q = 0.546 IRE units.

Suppose a test signal consists of a subcarrier having a peak value of 10 IRE units (20 IRE units p-p), then

$$DP=\frac{0.546}{10}\cdot\frac{2}{3}=0.0364\text{ rad}=2.07°$$

$$DG=100\%\left(\frac{0.546}{10}\right)\cdot\frac{2}{3}=3.64\%.$$

These two parameters directly affect the performance of any color-graphic system, such as a high-resolution optical reader or a conventional TV. Differential gain will distort the degree of color saturation. This distortion occurs because the amplitude of a small signal superimposed on another signal represents the saturation of the color. This distortion also affects the brightness of the color. Differential phase will cause incorrect hues in the reproduced picture. In an ADC, the analog section of the converter is the primary generator of these distortions.

The analog input circuitry determines the bandwidth, which tells you at what input frequency you can expect amplitude attenuation to begin. The bandwidth is normally defined as the maximum sinusoidal input frequency at which the amplitude of the output signal, derived from the digital data, decreases by 3 dB with respect to the amplitude of the output for a low-frequency sinusoidal input. A more appropriate parameter for an A/D converter is its full-power bandwidth. This parameter specifies the maximum frequency at which the converter can accurately quantize a full-scale-input sine wave without generating any spurious or missing codes.

Engineers often overlook full-power bandwidth when evaluating a high-speed A/D converter. A wide bandwidth results in reduced amplitude roll-off and less time-delay distortion. It also minimizes the interaction between the poles of the ADC's input and the poles of any antialiasing filter before the input. A narrow bandwidth could cause time-delay distortion due to nonlinear phase response, amplitude error, or rise-time error.

To illustrate the effects of the A/D converter's bandwidth, consider the amplitude attenuation and time-delay distortion when a full-scale 5-MHz sine wave is applied to the input of an equivalent A/D converter that has a 20-MHz bandwidth **(Fig 6)**. Assuming a single-pole model, the equivalent RC network will attenuate the input by 3% of its original value and shift the input's phase by −14.03°. The result of this action is a time delay of 7.8 nsec. The following formulas express the amplitude (A), the phase (ϕ), and the time

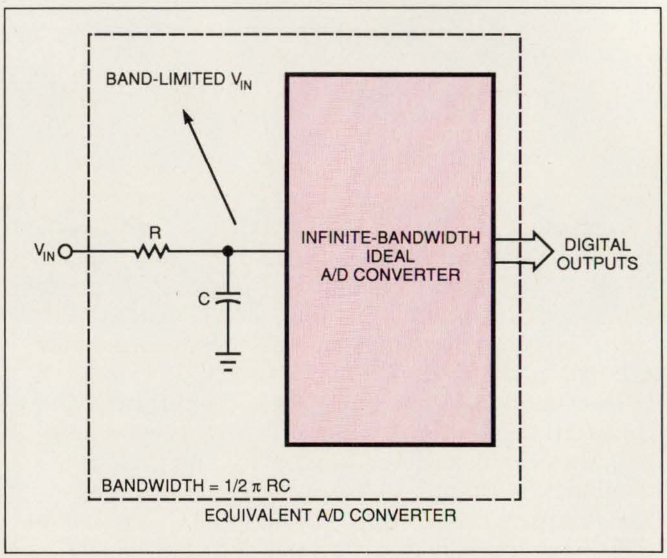

Fig 6—This equivalent circuit *illustrates the effects of a band-limited A/D converter compared with an ideal infinite-bandwidth converter.*

delay (ΔT) of the output of an A/D converter with a bandwidth of Δf, where f is the frequency of the input signal:

$$A=\sqrt{\frac{1}{1+(f/\Delta f)^2}}$$

$$\phi=-\tan^{-1}(f/\Delta f)$$

$$\Delta T=\frac{\phi}{360f}.$$

The transient-response time is the time the A/D converter requires to settle to its final accuracy when the input changes from negative full scale to positive full scale or the other way around. This response time depends primarily on the sample-and-hold acquisition time. Transient-response time is important in transient analysis and in applications in which the input of the A/D converter is multiplexed to increase the number of channels, as in data-acquisition systems.

When the input of an A/D converter exceeds the full-scale range, the analog section of the converter saturates. Because the error amplifier usually has a high gain, saturation is particularly significant for a subranging ADC. If the operating conditions do not let the ADC fully recover from saturation, the converter might produce an erroneous code for a valid input. The time the ADC requires to recover from saturation is called the overvoltage recovery time. The recovery time is measured from the time the input returns to the ADC's operating range until the time that the ADC can make a proper conversion. The recovery time increases as the overrange voltage increases.

Part 3 will conclude this subranging-ADC series with a discussion of test methods for evaluating these dynamic parameters and specifications. EDN

Author's biography

Ray Ushani is the manager of the Advanced Development Group at Datel Inc (Mansfield, MA). He has been with the company for six years and has been instrumental in the development of several A/D converters, multiplexers, and S/H circuits. Ray has an MSEE from Northeastern University (Boston, MA) and is a PhD candidate at Tufts University (Medford, MA). Not one to stray far from his vocation, Ray's hobbies include RF and microwave design.

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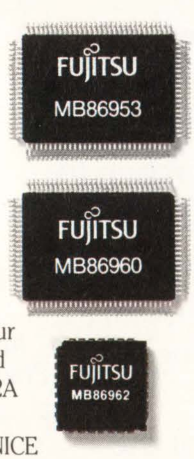

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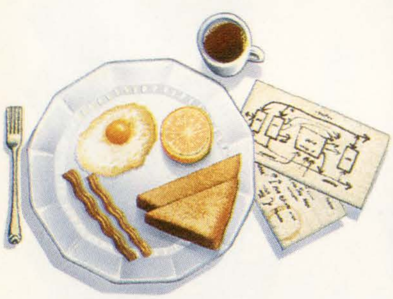

7:05 am : Breakfast
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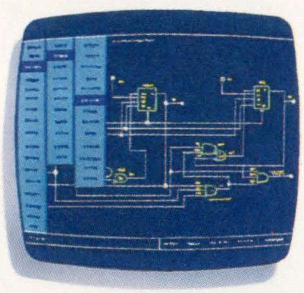

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11:00 am : Place & Route
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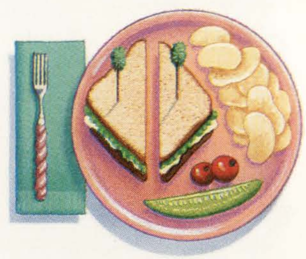

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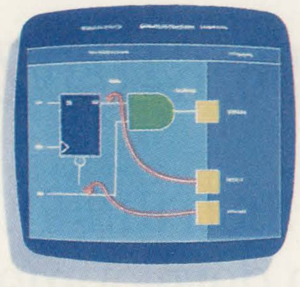
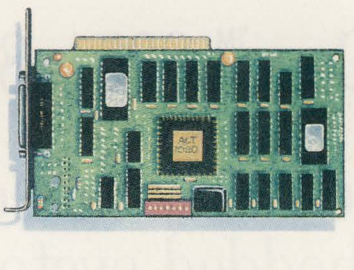
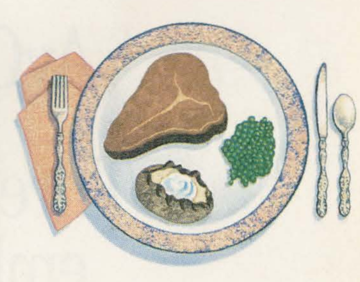
System Clock (MHz)		20-40	20-40
Availability		NOW	NOW
Technology (micron)		1.2	1.2

Breakfast And
n By Dinner.







1:15 pm: Program
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1:25 pm: Test
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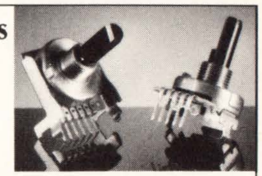

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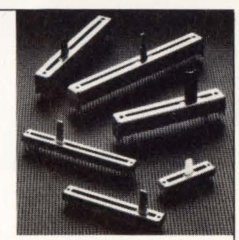

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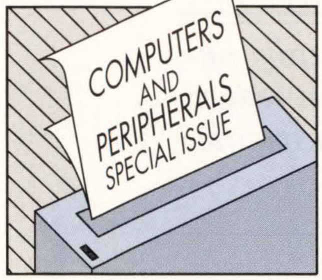

Design a digital synchronizer with a low metastable-failure rate

When you're attempting to synchronize asynchronous data to a system clock, don't let metastability ruin your design. Carefully considering this problem during the design phase can save you headaches down the line.

Steven R Masteller, *Allied-Signal Aerospace, Bendix Engine Controls Div*

Metastability is a type of failure that can occur when digital circuits attempt to synchronize asynchronous digital data. The failure is more prevalent at fast asynchronous data rates and, thus, fast synchronizing clock frequencies. If you don't consider metastability during the design phase, this monster can bite you later by producing intermittent failures that are extremely difficult to diagnose.

Although metastability is theoretically unavoidable in synchronizers, you can reduce the probability that a failure will occur during a specified time period. The common response for combating metastability failures is to use multistage synchronizers, which can reduce the number of failures to an arbitrarily small value. Understanding the various factors that influence metastability leads to a qualitative design procedure for multistage synchronizers that effectively makes the problem negligible.

Digital designers often overlook metastability and its effects because traditional textbooks don't address this type of failure. To understand the problem better, consider the simple SR flip-flop in **Fig 1.** A conventional digital analysis of this circuit gives rise to only two possible logic states for the inputs and outputs: logical 1 and logical 0. However, all digital circuits must pass through an active region when transiting from one state to another. **Fig 2a** shows a typical transfer function, H, for a NAND gate having one input at a logical 1 while the other input undergoes a transition from a logical 0 to a logical 1. The following equation represents the transfer function:

$$V_{OUT} = H(V_{IN}).$$

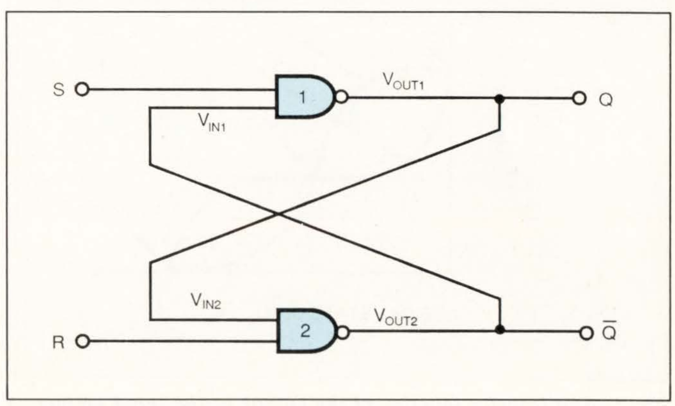

***Fig 1—The cross-coupled NAND gates of an SR flip-flop** can reach a metastable condition because the output of one gate is an input to the other.*

Although metastability is theoretically unavoidable in synchronizers, you can reduce the probability of a failure within a specified time period.

When you cross-couple two NAND gates to create the SR flip-flop in **Fig 1**, the output of one of the gates becomes one of the inputs to the other gate. The following equations define this feedback arrangement:

$$V_{IN1} = V_{OUT2}$$
$$V_{IN2} = V_{OUT1}.$$

You can superimpose the transfer functions for both NAND gates on a single graph to find the points of equilibrium **(Fig 2b)**. Because the previous three equations make the following relationships true:

$$V_{IN1} = H(V_{IN2})$$
$$V_{IN1} = H(V_{OUT1}),$$

the circuit reaches equilibrium at any point where

$$V_{IN1} = H(H(V_{IN1})).$$

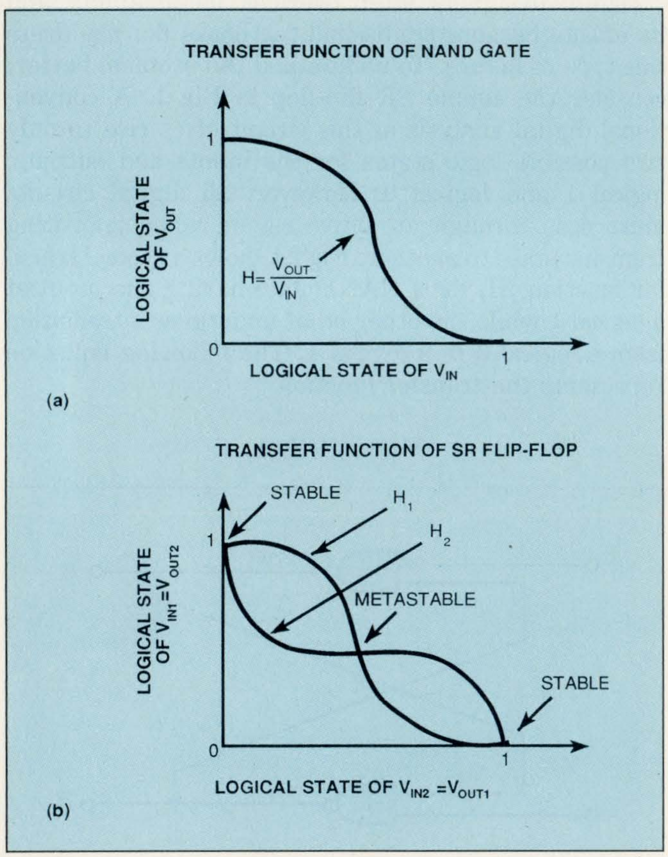

***Fig 2—The transfer function of the output vs the input voltage** of a NAND gate shows the gate's active region **(a)**. Superimposing the transfer functions for both gates of an SR flip-flop identifies two stable and one metastable equilibrium points **(b)**.*

The points where the two superimposed transfer-function curves in **Fig 2b** intersect are the equilibrium points. The equilibrium points labeled "stable" are the logic states conventional analysis predicts. However, the superimposed curves identify an additional equilibrium point labeled "metastable." The logic level for the metastable point is halfway between a stable logical 1 and a stable logical 0. Theoretically, the SR flip-flop can stay in the metastable condition indefinitely if noise or some other disturbance doesn't dislodge the circuit from this state.

It's just like rolling downhill

You can make an analogy between the metastable state and a ball resting precariously at the top of a smooth hill **(Fig 3)**. If you carefully balance the ball at the top of the hill, the ball will sit quietly until disturbed. When you disturb the ball slightly, which is analogous to a noise disturbance in a metastable circuit, the ball will roll to one side or the other and come to rest at the bottom of the hill, which is analogous to the circuit arriving at one of the two stable points. Which point the ball will arrive at is indeterminate. A ball at the bottom of the hill, which is analogous to an SR flip-flop in a stable state, will remain there barring any large disturbances.

Metastability occurs when a circuit violates the timing restrictions that the specification data impose on a flip-flop. Such restrictions include minimum pulse widths and minimum setup and hold times. If you main-

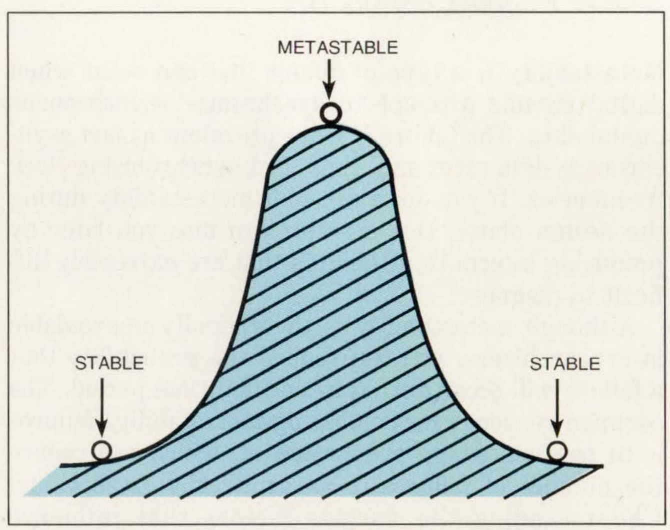

***Fig 3—The metastable state is analogous to a ball balanced** on top of a smooth hill. Any slight disturbance will start the ball rolling toward either of the stable states at the bottom of the hill.*

tain adequate timing margins in a synchronous circuit, metastability will never occur. However, in the many applications in which you must synchronize asynchronous data to a system clock, eliminating the synchronizing circuit's potential for becoming metastable is impossible.

Metastability causes the propagation delay of an SR flip-flop to be greater than its specified value. The metastable state is evidenced by a plateau in the output of the SR flip-flop **(Fig 4a).** The likelihood that an SR flip-flop will remain in a metastable state decreases exponentially with time. Metastability also increases the propagation delay of a D flip-flop from its specified value even though a metastable plateau is not evident on the output of the device **(Fig 4b).** The internal steering latches, which a D flip-flop employs to direct signals to its master SR flip-flop, smooth out the plateau region. Metastability can cause both types of flip-flops to generate a runt pulse. The runt pulse occurs when the flip-flop returns to the original stable state from the metastable state instead of making a transition to a new stable state.

Metastability in D flip-flops can cause two types of failures. One type occurs when a metastable condition prevents a D flip-flop from changing to a different state. In this case, an entire event can be lost. Timing failures can be even more insidious. The worst case occurs when the output of a flip-flop drives several destination flip-flops via circuit paths that have different propagation delays. A delayed output signal caused by a metastable condition may reach some of the destination flip-flops before the next clock occurs; the same output signal would arrive at other destination flip-flops after the next clock. This condition can cause some circuitry to recognize an event, such as an interrupt, one clock cycle late.

A simple equation predicts the MTBF

You can estimate a synchronizing flip-flop's mean time between failures (MTBF) due to metastability if you know the asynchronous data rate, F_D; the synchronizing clock frequency, F_C; the synchronizing flip-flop's propagation delay, T_P; the synchronizing flip-flop's inverse gain-bandwidth product, G; and the total gate delay between the synchronizing clock edge and any destination flip-flops that receive the synchronized data, T_D. The equation is as follows **(Ref 1):**

$$\mathrm{MTBF}=\frac{e^{((1/F_C)-T_D)/G}}{2F_CF_DT_P}.$$

Theoretically, you should include the circuit's rise and fall times as well as the average time for the circuit's noise to dislodge the flip-flop from the metastable state in the T_P term. However, the exponential factor dominates the MTBF equation for MTBFs greater than a few years. Therefore, the propagation delay of the synchronizing flip-flop is an adequate approximation

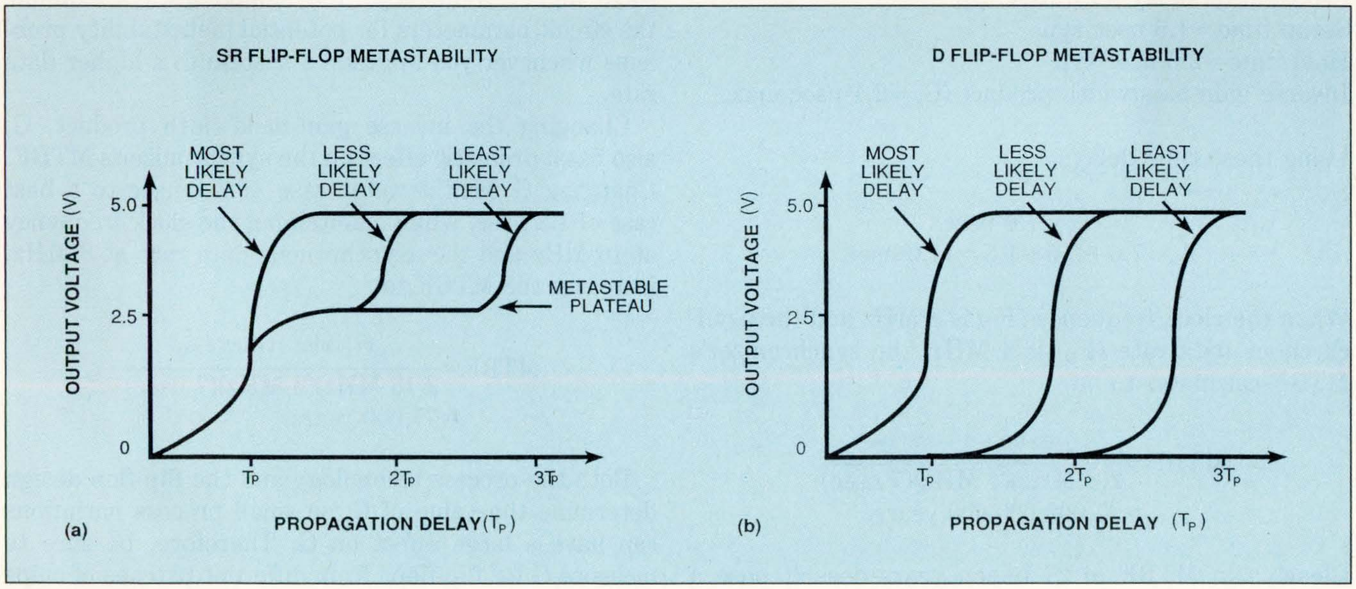

Fig 4—The metastable plateau *in the output of an SR flip-flop causes an increase in the device's propagation delay* ***(a).*** *Although a plateau is not evident in the output of a D flip-flop* ***(b),*** *metastability still increases the propagation delay.*

Metastability occurs when a circuit violates the timing restrictions that a flip-flop's specification data impose.

for T_P. An increase in the circuit noise or the rise and fall times only marginally improves the MTBF.

The G term is in the exponential factor of the MTBF equation and thus has a large effect on the resulting MTBF. Essentially, you'll produce more-reliable synchronizers by using flip-flops with large inverse gain-bandwidth products. G depends on both the internal design of the flip-flop and the process technology used to construct the device. As a general rule, fast technologies result in large G values and, consequently, synchronizers with high MTBFs for a specific clock frequency. **Ref 2** describes a method for measuring G for a flip-flop.

The T_D term is the sum of all the time delays between the synchronizing clock edge and a destination flip-flop. The sum includes not only the propagation delay of the synchronizing flip-flop but also any intervening-gate propagation delays as well as the setup and hold times of the destination flip-flop. The T_D term is in the exponential factor of the MTBF equation and has its most pronounced effect on the MTBF at high clock frequencies. Minimizing T_D can be an effective way of increasing the MTBF but is usually difficult.

To illustrate the effects of the circuit parameters on a synchronizer's MTBF, consider the following typical time delays and a worst-case inverse gain-bandwidth product for a single-stage D flip-flop built using a 2-μm process (**Fig 5**):

Propagation delay = 7.0 nsec typ
Setup time = 1.5 nsec typ
Hold time = 2.5 nsec typ
Inverse gain-bandwidth product (G) = 2.1 nsec max.

Using these time delays,

$$T_P = 7.0 \text{ nsec}$$
$$T_D = 7.0 + 2.5 + 1.5 = 11.0 \text{ nsec.}$$

When the clock frequency (F_C) is 8 MHz and the asynchronous data rate (F_D) is 4 MHz, the synchronizer's MTBF calculates to be

$$\text{MTBF} = \frac{e^{((1/8 \text{ MHz}) - 11 \text{ nsec})/2.1 \text{ nsec}}}{2(8 \text{ MHz})(4 \text{ MHz})(7 \text{ nsec})} = 27{,}000{,}000{,}000 \text{ years.}$$

Clearly, an MTBF of 27 billion years doesn't pose a significant risk of metastable operation in this synchronizer at these frequencies. However, when you double

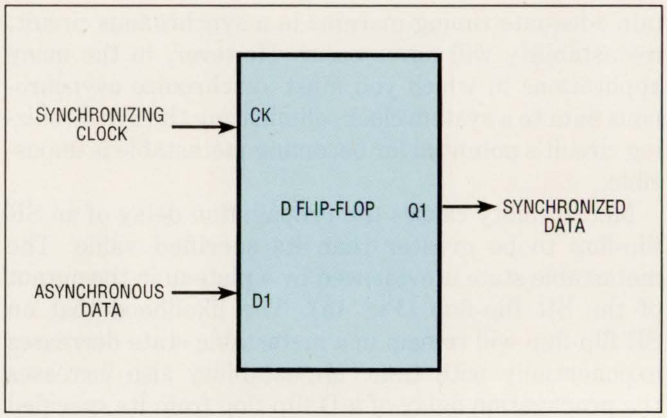

Fig 5—One of the simplest *single-stage data synchronizers is the D flip-flop.*

the clock frequency and the asynchronous data rate to 16 MHz and 8 MHz, respectively, the same synchronizer's MTBF calculates to be

$$\text{MTBF} = \frac{e^{((1/16 \text{ MHz}) - 11 \text{ nsec})/2.1 \text{ nsec}}}{2(16 \text{ MHz})(8 \text{ MHz})(7 \text{ nsec})} = 6.9 \text{ hours.}$$

Simply doubling the operating frequency causes the synchronizer's MTBF to plummet from billions of years to approximately seven hours. And any synchronizer—no matter how well behaved at a particular operating frequency—will produce unacceptable failure rates at some higher frequency. You should always examine the circuit parameters for potential metastability problems whenever you upgrade a system to a higher data rate.

Changing the inverse gain-bandwidth product, G, also has a dramatic effect on the synchronizer's MTBF. Changing G from a worst case of 2.1 nsec to a best case of 1.2 nsec, while maintaining the clock frequency at 16 MHz and the asynchronous data rate at 8 MHz, increases the MTBF to

$$\text{MTBF} = \frac{e^{((1/16 \text{ MHz}) - 11 \text{ nsec})/1.2 \text{ nsec}}}{2(16 \text{ MHz})(8 \text{ MHz})(7 \text{ nsec})} = 77{,}000 \text{ years.}$$

Both the process technology and the flip-flop design determine the value of G, so small process variations can have a large effect on G. Therefore, be sure to measure G for flip-flops from different batches of chips to establish a worst-case value. Process variations and, therefore, G tend to be constant for all chips from the

Decisions, Decisions, Decisions...

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Small changes in a circuit parameter can drastically change the calculated MTBF.

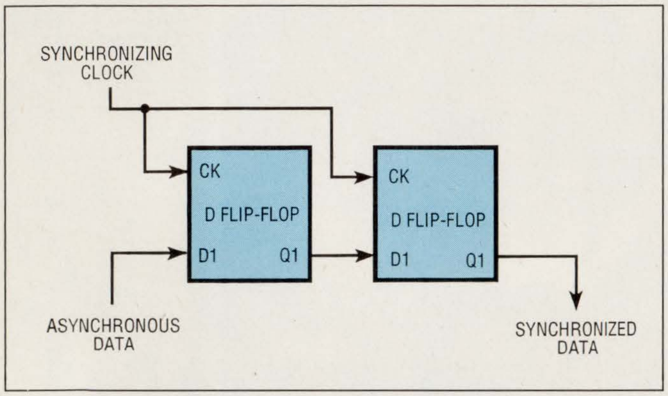

***Fig 6—You can build a 2-stage synchronizer** by cascading two D flip-flops that have a common clock. Continue adding D flip-flops to build a multistage synchronizer.*

same batch. Obtaining one batch of chips that doesn't exhibit metastable operation for a given set of conditions and another batch of chips that exhibits frequent metastability failures under the same conditions is indeed possible.

Although the clock rate, synchronous time delay, and process technology have pronounced effects on the MTBF due to metastability, you'll often have no control over these variables. In these cases, you should consider a multistage synchronizer to reduce metastable failures. You can construct a multistage synchronizer by cascading stages of multiple D flip-flops and providing a clock frequency that is common to all stages.

To illustrate the effectiveness of a 2-stage synchronizer (**Fig 6**), consider the same circuit parameters that produced the previous MTBF of 6.9 hours, or 24,958 sec, in a single-stage D flip-flop synchronizer. Only unsynchronized data caused by metastable operation in the first stage can cause a potential metastable failure in the second stage of a 2-stage synchronizer. Therefore, you can use the MTBF of the first stage to calculate the asynchronous data rate of the second stage. Using the following circuit parameters:

$T_P = 7.0$ nsec
$T_D = 7.0 + 2.5 + 1.5 = 11.0$ nsec
$G = 2.1$ nsec
$F_C = 16$ MHz
$F_D = 1/24{,}958 = 40.1\ \mu$Hz,

the MTBF of the 2-stage synchronizer is

$$\text{MTBF} = \frac{e^{((1/16\text{ MHz})-11\text{ nsec})/2.1\text{ nsec}}}{2(16\text{ MHz})(40.1\ \mu\text{Hz})(7\text{ nsec})} = 16{,}000{,}000 \text{ years.}$$

Adding one more stage to the synchronizer increased the MTBF from 6.9 hours to 16 million years. Although this failure rate is comfortably large, adding a third stage would effectively eliminate metastability as a problem.

These examples show that a small change in a circuit parameter can cause a drastic change in the MTBF. Small variations in the data can cause large variations between the calculated MTBF and the actual MTBF. A rule of thumb for designing a highly reliable synchronizer is to achieve a calculated MTBF of at least 10,000 years. This large MTBF figure should provide an adequate safety margin against small parameter variations causing excessive field failures.

Another suggestion is to multiply the 10,000-year MTBF times the number of units you expect to sell to arrive at a calculated MTBF for a single unit. For example, if you expect to sell 100 synchronizers, the calculated MTBF of a single synchronizer should be at least 1,000,000 years. This extra margin guards against field failures that you can't repeat in the laboratory. **EDN**

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Author's biography

Steven R Masteller has been a design engineer with the Bendix Engine Controls Div of the Allied-Signal Aerospace Co (South Bend, IN) for the past three years. He currently specifies and develops standard-cell ASICs for high-reliability, high-performance electronic engine-control circuits. Steven has a BSEE from Purdue University and enjoys travel, sky diving, and science fiction in his spare time.

EDITED BY CHARLES H SMALL

Regulator accepts high or low input

Brian Huffman
Linear Technology Corp, Milpitas, CA

The switching regulator in **Fig 1** produces a constant 12V dc output from inputs ranging from 8 to 20V dc, a typical requirement for battery-powered applications. The circuit uses a simple inductor, L_1, instead of the more common, and more expensive, transformer.

The circuit is a buck-boost switching regulator. Its switches (D_1, D_2, Q_1, and IC_1's internal switch (V_{SW})) alternately connect the inductor L_1 across the input and then the output.

IC_1 has a high-side switch, which connects one end of the inductor to the positive rail (−1.5V). Q_1 connects the other end of the inductor to ground. IC_1's V_{SW} pin provides enough drive to turn on Q_1. During Q_1's on period, the inductor accumulates energy. D_1 blocks the output capacitor from discharging through Q_1.

When IC_1's power switch turns off, the voltage on IC_1's V_{SW} pin decreases until the clamp diode, D_2, is forward-biased. At the same time, the falling voltage on the V_{SW} pin turns off Q_1, causing Q_1's drain voltage to rise until D_1 clamps it. D_1 and D_2 then provide a current path for the inductor to transfer its energy to the output. If you need to handle a higher input voltage, be sure to clamp the gate of Q_1 below its 20V-max rating.

IC_1's internal pulse-width modulator controls the energy transfer. IC_1's feedback pin, V_{FB}, samples the output from the 11.0-kΩ/2.49-kΩ divider. IC_1's error amplifier compares the feedback pin's voltage to its internal 2.21V reference and controls the duty cycle, completing a control loop. You can change the output voltage by varying the resistor-divider ratio. The RC damper on IC_1's V_C pin provides loop-frequency compensation.

The inductor supplies output current in pulses. The output capacitor, C_2, smoothes the current pulses. During the time IC_1's switch is on, the output capacitor delivers current to the load. The input capacitor, C_1, provides a low-resistance ac path for the inductor's current during this period. The input capacitor reduces the ripple seen on the V_{IN} pin.

The circuit's efficiency can exceed 70% for output currents greater than 0.5A. Also, for input voltages above 15V, it can supply more than 2A of output current. **(EDN BBS /DI_SIG #943)** **EDN**

To Vote For This Design, Circle No. 746

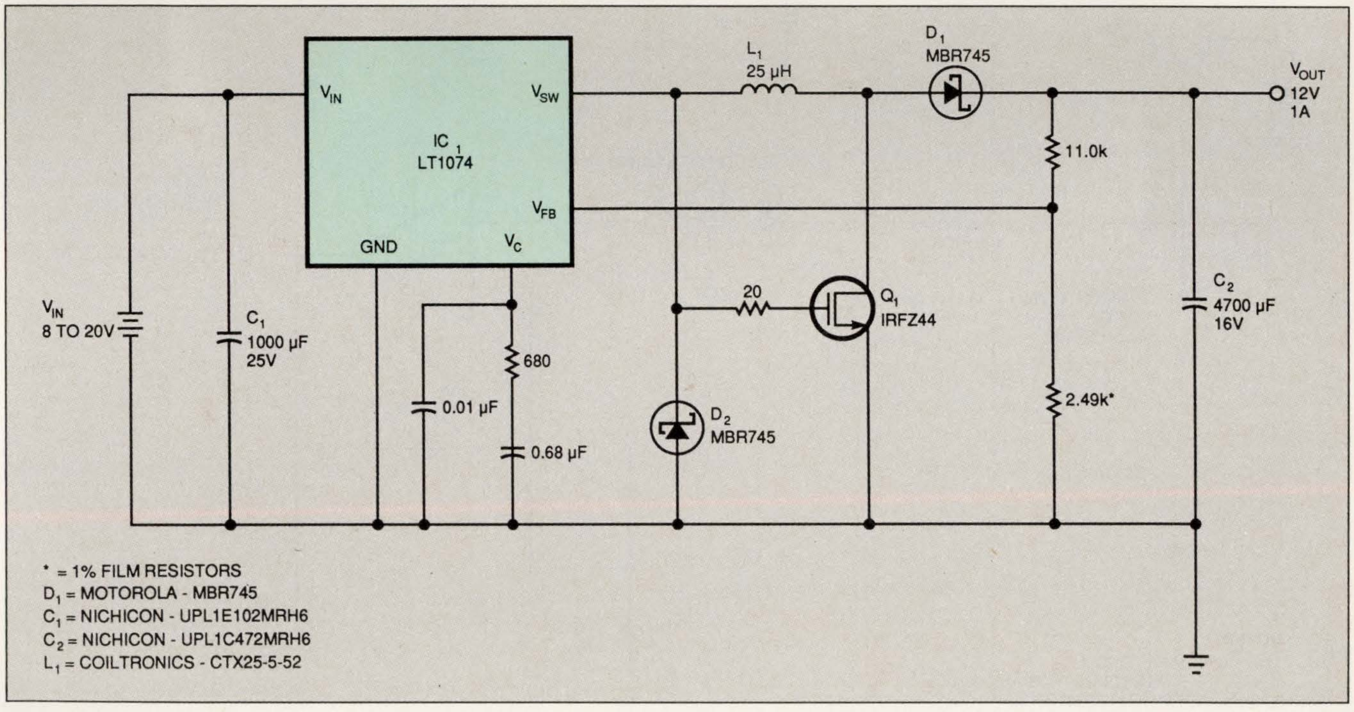

Fig 1—This switching regulator is suitable for *battery-powered applications because it produces a 12V dc output from inputs ranging from 8 to 20V dc.*

Transistor sensor needs no compensation

Jim Williams
Linear Technology Corp, Milpitas, CA

The thermometer circuit in **Fig 1** uses an inexpensive transistor to accurately measure temperature without compensation or calibration. Almost all transistor sensors use the base-emitter diode's voltage-shift with temperature as their sensing mechanism. Unfortunately, the *absolute* diode voltage is unpredictable, necessitating circuit calibration each time you fit a new transistor sensor.

The circuit in **Fig 1** overcomes this limitation. The circuit provides a 0-to-10V output corresponding to a 0-to-100°C input. Unadjusted error is $< \pm 1\%$.

The basis for the circuit is the predictable relationship between current and voltage in a transistor's V_{BE} junction. At room temperature, the V_{BE} junction diode shifts 59.16 mV per decade of current. The temperature dependence of this constant is 0.33%/°C, or 198 μV/°C. The ΔV_{BE}-vs-current relationship holds, regardless of the V_{BE} diode's *absolute* value.

An internal oscillator controls the state of the switches in IC_1, the LTC1043. The 0.01-μF capacitor at pin 16 sets the IC's oscillator frequency at about 500 Hz. Q_1 operates as a switched-value current source, alternating between about 10 and 100 μA as IC_1 commutates switch pins 12 and 14. The two currents' exact values are unimportant, so long as their *ratio* remains constant.

Because of this constant ratio, Q_1 requires no reference, although its emitter resistor's ratio must be precise. The alternating 10/100-μA stepped current drive

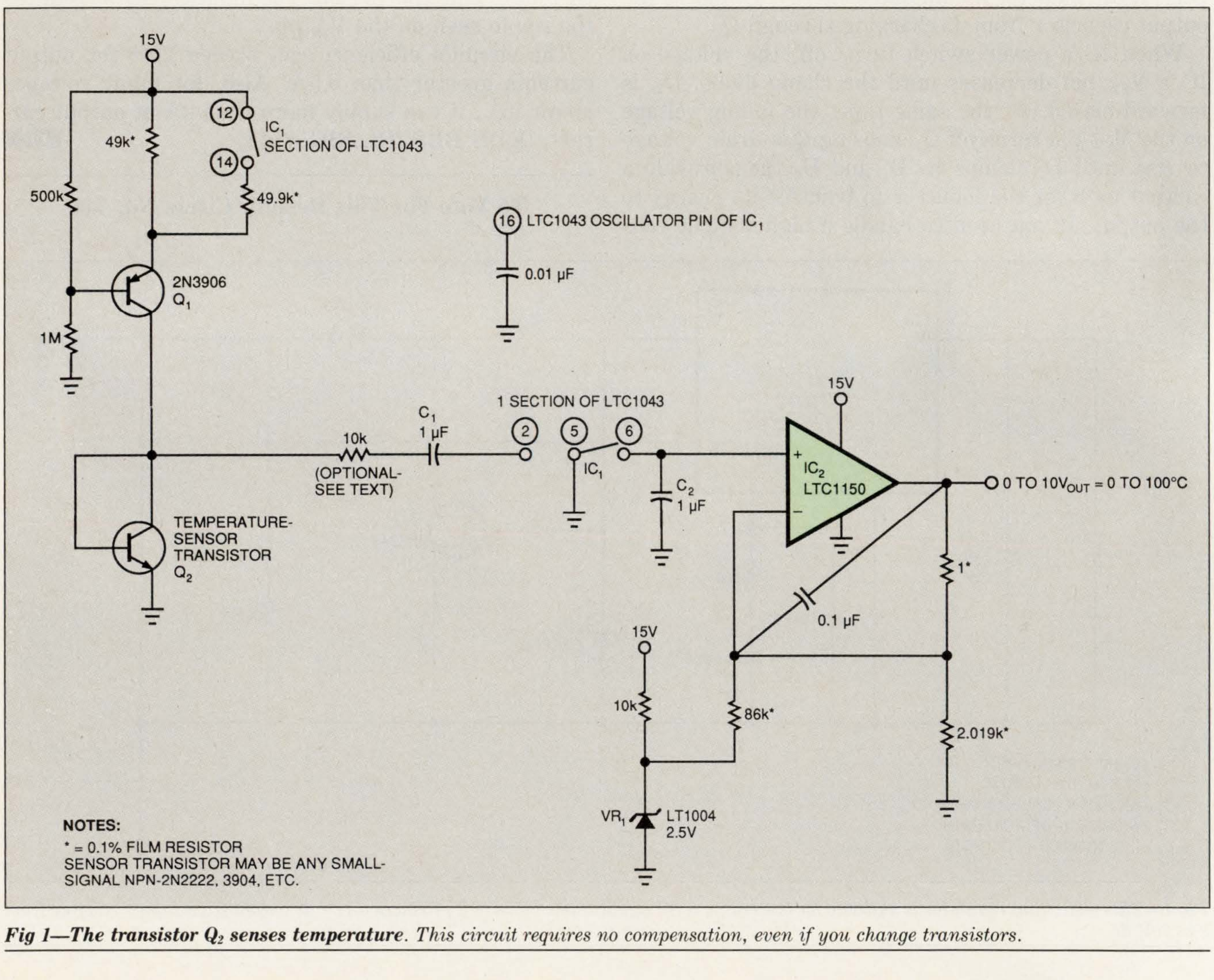

***Fig 1—The transistor Q_2 senses temperature**. This circuit requires no compensation, even if you change transistors.*

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•RMS-1W	2.0-750	DC-750	+7	5.8	45	6.75
RMS-2	5-1000	DC-1000	+7	6.8	38	6.95
•RMS-2D	5-1000	DC-1000	+7	6.8	40	7.25
RMS-2U	10-1000	10-1000	+7	6.5	46	11.45
RMS-5	5-1500	DC-1000	+7	6.0	41	13.95
RMS-1LM	2.0-500	DC-500	+10	5.8	47	7.95
RMS-2LH	5-1000	DC-1000	+10	6.6	40	8.95
•RMS-5LH	10-1500	DC-900	+10	5.4	38	14.95
RMS-1MH	2.0-500	DC-500	+13	5.7	44	8.95
RMS-2MH	5-1000	DC-1000	+13	6.6	44	9.95
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CIRCLE NO. 111

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to the sensor transistor, Q_2, causes the theoretical 59.16-mV excursion at 25°C to appear across the V_{BE} junction.

C_1 couples this signal to a switched demodulator that strips off Q_2's dc bias. Thus IC_1's pin 2 sees only the 59-mV waveform, which the demodulator action at pins 5 and 6 references to ground. Pin 5, connected to capacitor C_2, sits at pin 2's peak dc value. IC_2 amplifies this dc signal, with VR_1 providing offset so that 0°C equals 0V output. The optional 10-kΩ resistor protects against ESD (electrostatic discharge) events, which may occur if Q_2 is at the end of a cable.

Using the components in **Fig 1**, the circuit achieves ±1% error over a sensed 0-to-100°C range. Substituting randomly selected 2N3904s and 2N2222s for Q_2 showed less than 0.4°C spread over 25 devices from various manufacturers. **(EDN BBS /DI_SIG #945)**

EDN

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To Vote For This Design, Circle No. 747

Feedback tames detector overshoot

Jerald Graeme

Burr-Brown Corp, Tucson, AZ

The peak detector in **Fig 1** employs positive feedback, rather than using phase compensation or reducing the circuit's feedback factor (increasing gain), to control overshoot. A peak detector must control overshoot because uncontrolled overshoot leads to errors of 30% or more. Using positive feedback for control expands your choice of op amps beyond those that allow only external compensation.

Resistors R_1 and R_2 provide the necessary positive feedback. Op amp IC_1 buffers and charges the holding capacitor, C_H. Voltage follower IC_2 isolates the hold capacitor from the load. A feedback loop removes IC_2's errors from the output.

Diode D_1 switches the feedback loop to control peak detecting. As long as the voltage on C_H is higher than the input, D_1 is reverse-biased, and the feedback loop is open. When the input rises above the voltage on C_H, IC_1 charges the holding capacitor to this new value and D_1 switches on the feedback loop, ensuring an accurate stored voltage on C_H.

Without overshoot, the circuit's error is just the input error of IC_1 ($\sim V_{OS}+V_{IN}/A$). But three factors make peak detectors prone to overshoot: normal op-amp overshoot, capacitive output loading, and having two amplifiers in a feedback loop.

Most op amps have 50 to 60° of phase margin. This compensation offers the best settling time and best real-time accuracy for most applications. However, for peak detectors, this phase margin causes 10 to 15% overshoot. The inherent capacitive loading and the 2-op-amp design result in even greater overshoot.

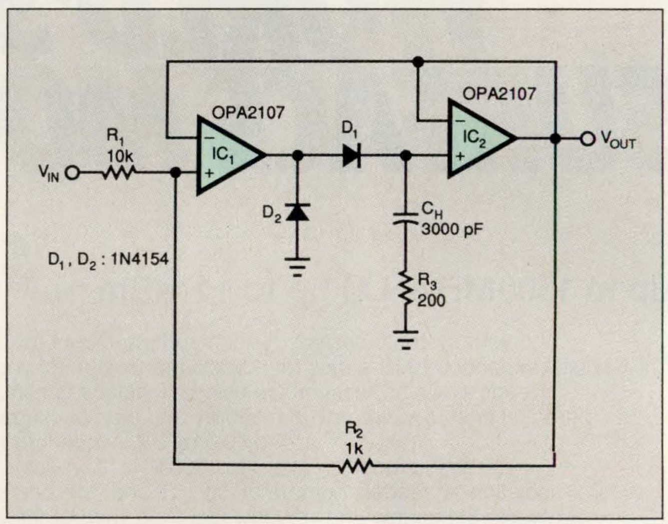

Fig 1—This peak detector's positive feedback reduces overshoot by reducing the circuit's feedback factor—without resorting to increased gain.

The positive feedback via R_2 and R_1 has a positive feedback factor β equal to $R_1/(R_1+R_2)$. This positive feedback combines with the unity negative feedback from the output of IC_2 to the negative input of IC_1.

Thus the circuit has a reduced feedback factor without resorting to increasing its gain.

For the components in the **figure**, the overall feedback factor β is 0.09, which has the same stabilizing effect as raising the circuit's gain to 11. Overshoot is now a residual 0.2% resulting from feedback-delay oscillations.

Adding R_1 and R_2 does not alter the circuit's gain because the input signal does not appear across these resistors. For unity gain, the voltage across R_2 must, after all, be only the error signal. This error voltage injects a small current into R_1. The resulting voltage differences on R_1 and R_2 define an input-to-output voltage difference equal to $(V_{OS}+V_{OUT}/A)/\beta$. This difference is small because $V_{OUT}\approx V_{IN}$ during continued operation.

This analysis also demonstrates two other effects of the positive feedback. First, the circuit amplifies the input-error signal of IC_1 by $1/\beta=11$ rather than by unity. Second, the circuit's input resistance is much higher than you would expect. An input signal driving a feedback network normally suggests a low input resistance for an op-amp circuit. However, the positive feedback bootstraps the circuit's resistance in the critical sample interval. The current R_1 draws from the input equals $V_{OUT}/A{\cdot}R_2\approx V_{IN}/A{\cdot}R_2$. Thus, the circuit's input resistance is $A{\cdot}R_2$ during the sample interval. **(EDN BBS /DI_SIG #944)** EDN

To Vote For This Design, Circle No. 748

8051 program converts BCD to binary

John T Hannon
Stewart Warner Alemite, Charlotte, NC

The assembly language program in **Listing 1** for 8051-family single-chip μPs converts a BCD number to binary. Unlike other special-purpose, BCD-to-binary routines, you can easily extend this program to convert numbers larger than the 5-byte BCD numbers allowed here.

Before kicking off the program, you must store the 5-byte BCD number in a 5-byte register and allocate a 2-byte register for the binary result. During initialization, the program sets up pointers to these two registers and clears the binary register. Then the program stores the first BCD digit in the result register.

The program has two routines. After initialization, the first routine sets up the conversion factor for the first bit of each BCD digit. The initial value for the

Listing 1—8051 BCD-to-binary conversion program

```
LABEL     MNEMONIC                    COMMENT

BCDBIN:   MOV       RO,#REGBCD        ;BCD REGISTER POINTER
          MOV       R1,#REGBIN        ;BINARY REGISTER POINTER
          MOV       @R1,#OOH
          INC       R1
          MOV       @R1,#OOH          ;ZERO BINARY REGISTER
          DEC       R1
          MOV       A,@RO
          ANL       A,#OFH            ;SAVE FIRST BCD DIGIT
          MOV       @R1,A
          MOV       R4,#OAH           ;CONVERSION NUMBER FOR FIRST BIT
          MOV       R5,#OOH           ;OF SECOND BCD DIGIT (10)
          CALL      BCDCON
          MOV       R4,#64H           ;CONVERSION NUMBER FOR FIRST BIT
          MOV       R5,#OOH           ;OF THIRD BCD DIGIT (100)
          CALL      BCDCON
          MOV       R4,#OE8H          ;CONVERSION NUMBER FOR FIRST BIT
```

Listing 1—8051 BCD-to-binary conversion program *(continued)*

```
          MOV     R5,#03H          ;OF FOURTH BCD DIGIT (1000)
          CALL    BCDCON
          MOV     R4,#10H          ;CONVERSION NUMBER FOR FIRST BIT
          MOV     R5,#27H          ;OF FIFTH BCD DIGIT (10000)
          MOV     R2,#03H          ;CHECK ONLY 3 BITS OF FIFTH DIGIT
          CALL    BCDCN1
          RET

BCDCON:   MOV     R2,#04H          ;CONVERSIONS PER BCD DIGIT
BCDCN1:   INC     R0               ;INCREMENT BCD REGISTER TO NEXT DIGIT
          MOV     A,@R0            ;GET BCD DIGIT
          ANL     A,#0FH           ;MASK OFF UPPER FOUR BITS
          MOV     R3,A             ;AND STORE IN TEMPORARY REGISTER
BCDCN2:   MOV     A,R3             ;GET BCD DIGIT
          RRC     A                ;SHIFT DIGIT ONE BIT RIGHT
          MOV     R3,A             ;STORE SHIFTED DIGIT AGAIN
          JNC     BCDCN3           ;IF NO CARRY, DO NOT ADD FACTOR
          MOV     A,@R1            ;GET FIRST BYTE OF BINARY RESULT
          ADD     A,R4             ;ADD FIRST BYTE OF CONVERSION FACTOR
          MOV     @R1,A            ;STORE FIRST BYTE OF BINARY RESULT
          INC     R1               ;INCREMENT TO 2ND BYTE OF BINARY REG
          MOV     A,@R1            ;GET SECOND BYTE OF BINARY RESULT
          ADDC    A,R5             ;ADD (WITH CARRY) 2ND BYTE OF FACTOR
          MOV     @R1,A            ;STORE SECOND BYTE OF BINARY RESULT
          DEC     R1               ;DECREMENT POINTER TO FIRST BYTE OF
                                   ;BINARY REGISTER

BCDCN3:   MOV     A,R4             ;DOUBLE VALUE OF CONVERSION NUMBER
          CLR     C                ;FOR EACH BCD DIGIT BY SHIFTING R4
          RLC     A                ;AND R5 ONE BIT TO THE LEFT.
          MOV     R4,A
          MOV     A,R5
          RLC     A
BCD12:    MOV     R5,A
          DJNZ    R2,BCDCN2        ;DECREMENT CONVERSION COUNTER
          RET                      ;REPEAT UNTIL ALL BITS CHECKED
```

conversion factor is 10_{10} ($000A_{HEX}$). Then the first routine calls the second routine as a subroutine to do the actual conversion. If the BCD digit's bit is a one, the subroutine adds the conversion factor for that bit to the partial binary result. Then the program adjusts the conversion factor to correspond to the next bit in the selected BCD digit. The program checks each bit in a similar fashion.

The program uses a loop counter to check all four bits of each BCD digit. When the loop counter reaches zero, the program increments the BCD-register pointer, gets the next BCD digit, and masks off the digit's upper four bits in case the number is in ASCII. The program then shifts one bit to the right through the carry bit and stores the shifted number.

Checking the carry bit determines if the conversion factor gets added to the binary result or not. If the bit is a zero, the conversion factor does not get added; if the bit is a one, the conversion factor does get added.

To repeat the bit-conversion loop, the program shifts the conversion factor one bit to the left, doubling its value. The result of decrementing the bit counter determines if the loop needs to be repeated or not. This test allows the conversion routine to test each bit in a BCD digit and add 10_{10}, 20_{10}, 40_{10}, and 80_{10} for each bit, respectively, that is a one.

After converting the first digit, the program returns to the initialization section, adding 100_{10} (00064_{HEX}) to the conversion factor. The program then repeats, converting the second, third, and fourth BCD digits. For the fifth—or ten-thousands—digit, the bit counter's value is only 3 instead of 4 because a 5-digit BCD number cannot be greater than 65,535.

You can easily extend this program by expanding the registers and extending the counters. You can obtain the **listing** from the EDN BBS (617) 558-4241, 300/1200/2400, 8, N, 1—from main menu, enter (s)ig, <s/di_sig>, rk941). **(EDN BBS /DI_SIG #941)**

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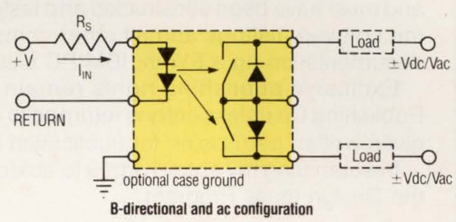
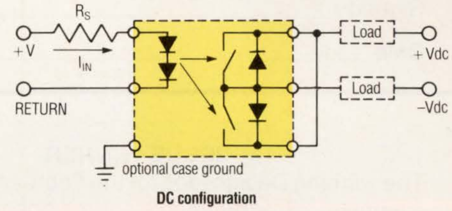
Input Current (Guaranteed On)	10		mA_{DC}
Input Current (Guaranteed Off)		100	μA_{DC}
Input Voltage Drop at (I_{IN}) = 25mA		3.25	V_{DC}

OUTPUT ELECTRICAL CHARACTERISTICS (–55° to + 105° unless otherwise noted)				
Part Number	FB00CD	FB00FC	FB00KB	Units
Bidirectional Load Current (I_{LOAD})	±1.0	±0.50	±0.25	A_{DC}/A_{PK}
DC Load Current (I_{LOAD})	2.0	1.0	0.5	A_{DC}
Bidirectional Load Voltage (V_{LOAD})	±80	±180	±350	V_{DC}/V_{PK}
DC Load Voltage (V_{LOAD})	80	180	350	V_{DC}
ON-Resistance (R_{ON}) at (I_{LOAD}) max.	0.72	1.8	12.9	Ohms
Turn-On Time (T_{ON})	800	800	500	µs
Turn-Off Time (T_{OFF})	300	600	500	µs

Notes: 1. A series resistor is required to limit continuous input current to 50mA (peak current can be higher).
2. Rated input current is 25mA for all tests.
3. Loads may be connected to any output terminal.
4. ON resistance shown is for the bidirectional configuration. The DC ON resistance is ¼ of these values.



B-directional and ac configuration



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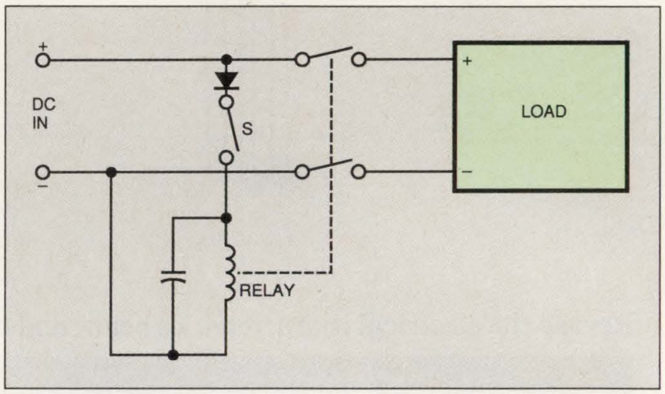

***Fig 1—This simple relay circuit provides** absolute reverse-polarity protection because it will not apply power to the load unless the power's polarity is correct.*

The simple circuit in **Fig 1** will not apply power to the load *unless* the power's polarity is correct to begin with. The circuit consumes little power, causes no voltage drop, and does not impair regulation. Switch S is an optional on/off switch. **(EDN BBS /DI_SIG #942)**

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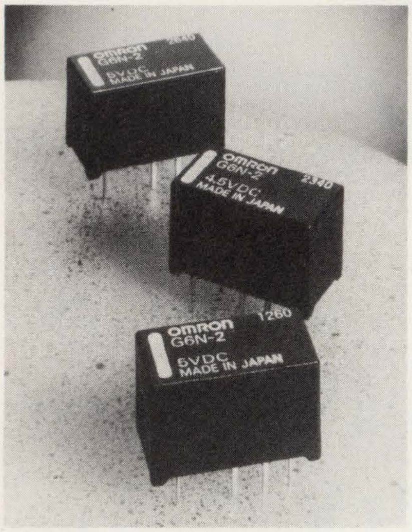
COMPONENTS & POWER SUPPLIES



Electromechanical Relay

- *Handles 2500V surges*
- *Rated to switch 1A*

Housed in a 12-pin DIP measuring 11×7.5×15 mm, the G6N electromechanical relay has a 2.5-kV-surge withstand voltage rating. The unit has a 2 Form C (dpdt) contact arrangement and handles currents of 1A max; maximum switched power rating equals 30W or 62.5 VA. Coil pick-up power requirement equals 140 mW, and contact resistance measures 50 mΩ max. Operate and release times equal 3 and 2 msec, respectively. Dielectric strength measures 1000V ac between each contact and 1800V ac between contacts and coil. The relay service life is 500,000 operations with a 1A, 30V dc load and 200,000 operations for a 0.5A, 125V ac load. Operating range spans −40 to +85°C. The relay is fully sealed to accommodate water-soluble flux immersion cleaning methods. $4.05

Omron Electronics Inc, 1 E Commerce Dr, Schaumburg, IL 60173. Phone (708) 843-7900. FAX (708) 843-7787. **Circle No. 357**

Power Oscillators

- *Provide a 5-VA output*
- *Output frequency ranges from 0.4 to 10 kHz*

Series 110A100 solid-state power oscillators develop a 5-VA sine wave output. Designed for synchro, resolver, LVDT/RVDT, or inductosyn conversion systems, the oscillators operate over a 0.4- to 10-kHz range and develop output voltages of 6 to 115V rms. The power-output stage is short circuit and overload protected. The units also have an automatic-thermal-shutdown feature to protect against failures caused by long-term overloads. A potentiometer allows you to adjust the output amplitude by ±10%. Two additional 2.5V rms outputs are also available; one has a 90° phase advance with respect to the other output. The oscillators are housed in a 2.6×3.1×0.82-in. module, which has an integral metal top surface that provides all required heat sinking. From $495. Delivery, stock to 10 weeks ARO.

Control Sciences Inc, 9509 Vassar Ave, Chatsworth, CA 91311. Phone (818) 709-5510. FAX (818) 709-8546. **Circle No.** 358

FDDI Data Link

- *Operates at 125M bps*
- *Has a 21-dB power margin*

The ODL 125 Series II lightwave data link will transfer data in accordance with the FDDI standard. For NRZ (nonreturn to zero) signals, it can operate at data rates ranging from 20M to 125M bps at a typical distance of 3 km. The link has typical beginning-of-life power margin of 21 dB. The devices employ complementary bipolar IC technology and are housed in 16-pin DIPs that include ST-style optical connectors. The link is optimized for 62.5/125-μm fiber, but it can function with 50/125-, 85/125-, and 100/140-μm fibers as well. The transmitter consists of a long-wavelength LED and a silicon IC. It operates from a single supply of 4.5 to 5.46V. The receiver is equipped with a PIN photodetector and operates at the same supply levels as the transmitter. $175/pair (1000).

AT&T Microelectronics, Dept 52AL040420, 555 Union Blvd, Allentown, PA 18103. Phone (800) 372-2447; in Canada, (800) 553-2448; in PA, (201) 771-2826.

Circle No. 359

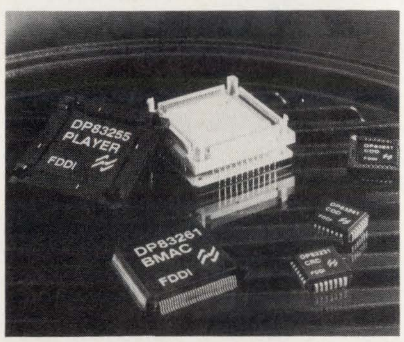
DIP Sockets

- *Include decoupling capacitor*
- *Accommodate 6- to 48-pin devices*

Series 451 DIP sockets come complete with a surface-mount decoupling capacitor and are available in sizes of 6 to 48 pins. The units incorporate a large-area ground plane across the entire surface of the socket. This plane helps eliminate the effects of noise before it reaches the chip. The ground plane surface is insulated with a masking material to protect nearby components from any electrical interference. The sockets are stackable end to end or side by side and are available in versions with 0.3- and 0.6-in. center spacings. A variety of terminal styles, contact pressures, plating configurations, and capacitor values is available. From $0.47 (100).

Andon Electronics Corp, 4 Court Dr, Lincoln, RI 02865. Phone (401) 333-0388. FAX (401) 333-0287.

Circle No. 360



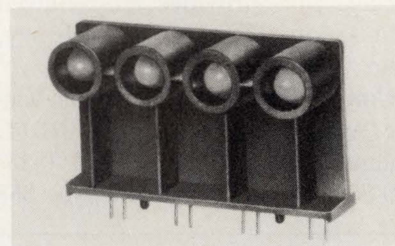
FDDI-Chip Sockets

- *Have a 2-piece design*
- *Accept plastic leaded chip carriers*

Micro-Pitch sockets accept the 132-pin basic media-access-controller and physical-layer-controller FDDI chips. The low-profile plastic-leaded-chip-carrier (PLCC) sockets accept the 28-position clock distribution device and the clock recovery device chips. The 2-piece Micro-Pitch units feature a 0.025-in.-contact centerline spacing and have a 0.375-in. mounted height. Low-profile units have a mounted height of 0.185 in. and feature an open-bottom design. The high normal-force contacts are phosphor bronze with tin-lead over nickel plating. Housing materials withstand the rigors of vapor-phase and infrared reflow surface-mount soldering systems. Micro-Pitch, $0.07 to $0.08/line (1000); low-profile, $0.003 to $0.044/line (10,000). Delivery, four to six weeks ARO.

AMP Inc, Box 3608, Harrisburg, PA 17105. Phone (800) 522-6752.

Circle No. 361



Quad LED Assemblies

- *Have a light shield to minimize false indications*
- *Available in three colors*

Series 5644H right-angle quad LED assemblies feature a light shield that eliminates false indications caused by light bleeding from adjacent LEDs. The units have a 0.75-in. mounted height and feature press-in pins, which provide consistent alignment with front panels. The units are available in red (5644H1), green (5644H5), and yellow (5644H7). They have a 120-mcd brightness level at a drive of 2V and 20 mA. The assemblies are housed in a 94V-0 UL-rated black housing. The housing features built-in standoffs that prevent flux entrapment, thereby simplifying the board-cleaning process after the soldering operation. From $0.89 (OEM qty).

Industrial Devices Inc, 260 Railroad Ave, Hackensack, NJ 07601. Phone (201) 489-8989. FAX (201) 489-6911.

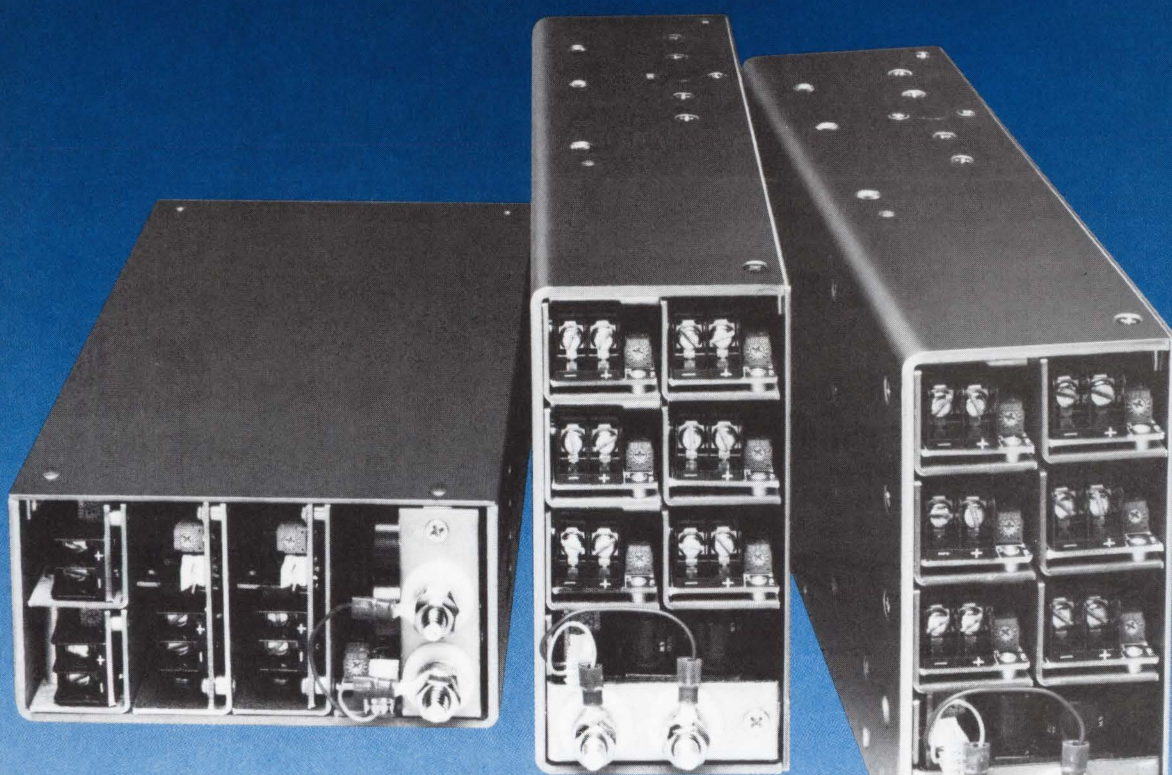
Circle No. 362

VM SERIES
BUS SWITCHERS–
VME, VXI, FUTUREBUS

10 Watts/Cu.In. @ 50°C!

Unique Deltron MODUFLEX Design

- Modular High Density Construction
- FINTEGRA – Distributed Thermal Management with Cooling Fins Integral to Each Module



- 1 to 7 outputs
- 400 to 1500 watts
- 120 kHz. MOSFET design
- Current mode control
- All outputs regulated and floating

Call Toll Free 1-800-523-2332
In PA: 215/699-9261

Deltron inc.
POWER PRODUCTS

VM-101 3/91

SPECIFICATIONS

INPUT
90-132 VAC or 180-264 VAC, 47-440 Hz. Strappable.

INPUT SURGE
Less than 68 Amps peak from cold start. For 1000W and 1500W units less than 136 Amps peak.

HOLDUP TIME
20 milliseconds from loss of nominal AC power.

OUTPUTS
See model selection table.

ADJUSTABILITY
±5% trim adjustment. All 5VDC outputs are adjustable up to 5.2VDC @ full output.

OUTPUT POLARITY
All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

LINE REGULATION
Less than ±0.1% or ±5mV for input changes from nominal to min. or max. rated values.

LOAD REGULATION
±0.2% or ±10mV for load changes from 50% to 0% or 100% of max. rated values.

MINIMUM LOAD
Main output requires a 10% minimum load for full output from auxiliaries.

REMOTE SENSING
On all outputs except those less than 100 watts and less than 20 Amps.

RIPPLE & NOISE
1% or 100mV pk-pk, 20 MHz bandwidth.

OPERATING TEMPERATURE
0-70°C. Derate 2.5%/°C above 50°C.

COOLING
A min. of 10 LFS cooling air directed over the units for full rating. Two test locations on chassis rated for max. temperature of 90°C. 1000 and 1500 watt units have built-in fan.

TEMPERATURE COEFFICIENT
±0.02%/°C.

EFFICIENCY
80% typical.

SAFETY
Units meet UL 1950, CSA 22.2 No. 220, CSA bulletin 1402C, EN 60 950, DIN VDE 0805/05.90. Certifications in process.

DIELECTRIC WITHSTAND
3750 VRMS input to ground.
3750 VRMS input to output.
700 VDC output to ground.

SPACING
8 mm primary to secondary.
4 mm to grounded circuits.

LEAKAGE CURRENT
0.75 mA at 115 VAC 60Hz. input.
1.5 mA for 1000 watt and 1500 watt models.

EMISSIONS
Units meet FCC 20780 Part 15 Class A and VDE 0871/6.78 Class A for conducted emissions. Compliance with Class B limits by use of additional external filter. 1000 watt and 1500 watt models require optional filter for Class A.

DYNAMIC RESPONSE
Peak transient less than ±2% or ±200mV for step load change from 75% to 50% or 100% max. ratings.

RECOVERY TIME
Recovery within 1%.
Main output – 200 microseconds.
Auxiliary outputs – 500 microseconds.

AC UNDERVOLTAGE
Protects against damage for undervoltage operation.

OVERVOLTAGE PROTECTION
Standard on main output.

REVERSE VOLTAGE PROTECTION
All outputs are protected up to load ratings.

OVERLOAD & SHORT CIRCUIT
Outputs protected by duty cycle current foldback circuit with automatic recovery. Auxiliaries have additional backup fuse protection.

THERMAL SHUTDOWN
Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

SOFT START
Units have soft start feature to protect critical components.

FAN OUTPUT
Nominal 12 VDC @ 12 watts maximum.

INHIBIT
TTL compatible system inhibit provided.

SHOCK
MIL-STD 810-D Method 516.3, Procedure III.

VIBRATION
MIL-STD 810-D Method 514.3, Category 1, Procedure I.

MECHANICAL

CASE	WATTS	H	x	W	x	L
1	400 W/500 W	2.5"	x	5.05"	x	9.0"
2	750 W	2.5"	x	5.20"	x	9.63"
3	1000 W	5.0"	x	5.05"	x	10.4"
4	1500 W	5.0"	x	5.20"	x	11.0"
5	860W	2.5"	x	5.0"	x	6.85"

POWER FAIL MONITOR
Optional circuit provides isolated TTL and VME compatible power fail signal providing 4 milliseconds warning before main output drops by 5% after an input failure. Available on units with a high current 5 volt output.

AUTO RANGER
Optional circuit provides automatic operation at specified input ranges without strapping. Not available on single output units.

PILOT BIAS
Optional circuit provides SELV output of 5 volts at 1 Amp independent of the main power converter. Output isolation compliant to safety specifications referenced above. Not available on single output units.

EMI FILTER
For Class A on 1000 and 1500 watt units.

COVER
Optional flat cover recommended when customer supplied fan cooling is directed through the length of the unit.

FAN COVER
Optional cover with brushless DC fan which provides the required air flow for full rating of VM power supplies.

POWER FACTOR CORRECTION
Refer to Bulletin FM-101 for FM Series units with 0.99 power factor and harmonic currents compliant to IEC 555-2.

DESCRIPTION

VM Series switchers comprise a line of open frame power supplies with output combinations that are required for a large variety of bus systems such as VME, VXI, and FUTUREBUS. Units in this fully modular family offer power density up to 10 watts per cubic inch. The small size and high power available permits more system hardware to be packaged in a given enclosure. The extended function without additional cabinet overhead will give your product a competitive edge in the marketplace.

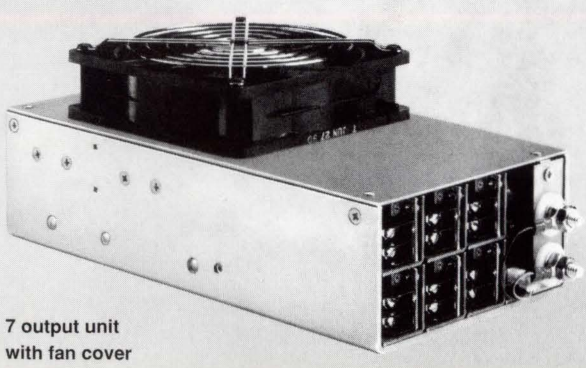
VM Series feature outstanding quality, insuring full compliance to specifications, reliable field operation and long service life. This exceptional quality is a result of three major efforts.

- Meticulous innovative engineering design.
- Total modular mechanical design.
- Excellent thermal management.

VM Series are available in power ratings from 400 to 1500 watts and with 1 to 7 outputs in a single package.

FEATURES

- TUV, UL, CSA.
- 10 watts per cubic inch.
- 120 kilohertz MOSFET design.
- Current mode control.
- All outputs:
  - *Adjustable.*
  - *Floating.*
  - *Overload and short circuit proof.*
- System inhibit.
- Load proportional DC fan output.
- Options include:
  - *Auto ranger for continuous input operation.*
  - *Power fail monitor.*
  - *Pilot bias.*
  - *EMI filter for 1000 and 1500 watt units.*
  - *Cover.*
  - *Fan cover – 1000 and 1500 watt units have fan built in.*



7 output unit with fan cover

SINGLE OUTPUT MODELS

Model	VDC	Amps	
VM12D0-YY	2VDC	150A	Nominal Power 860 W Case 5
VM12D1-YY	3.3VDC	150A	
VM12D2-YY	5VDC	150A	
VM12D3-YY	12VDC	72A	
VM12D4-YY	15VDC	57A	
VM12D6-YY	24VDC	36A	
VM12D9-YY	48VDC	18A	

MULTIPLE OUTPUT MODELS

Model VM1A-YY
Total Power: 400 Watts
Case: 1
Ratings: 5VDC @ 50A, 5VDC @ 10A, 12VDC @ 12A, 12VDC @ 6A

Model VM2A-YY
Total Power: 400 Watts
Case: 1
Ratings: 5VDC @ 50A, 12VDC @ 6A, 12VDC @ 6A, 24VDC @ 6A

Model VM1B-YY
Total Power: 500 Watts
Case: 1
Ratings: 5VDC @ 80A, 5VDC @ 10A, 12VDC @ 12A, 12VDC @ 12A

Model VM2B-YY
Total Power: 500 Watts
Case: 1
Ratings: 5VDC @ 80A, 12VDC @ 12A, 12VDC @ 6A, 24VDC @ 6A

Model VM3B-YY
Total Power: 500 Watts
Case: 1
Ratings: 5VDC @ 80A, 12VDC @ 12A, 24VDC @ 6A, 5VDC @ 10A, 12VDC @ 6A

Model VM1D-YY
Total Power: 750 Watts
Case: 2
Ratings: 5VDC @ 120A, 12VDC @ 12A, 24VDC @ 6A, 5VDC @ 10A, 12VDC @ 6A

Model VX1B-YY
Total Power: 500 Watts
Case: 1
Ratings: 5VDC @ 30A, 2VDC @ 10A, 5VDC @ 10A, 12VDC @ 6A, 12VDC @ 6A, 24VDC @ 3A, 24VDC @ 3A

Model VX1D-YY
Total Power: 750 Watts
Case: 2
Ratings: 5VDC @ 60A, 2VDC @ 12A, 5VDC @ 12A, 12VDC @ 8A, 12VDC @ 8A, 24VDC @ 4A, 24VDC @ 4A

Model VX1E-YY
Total Power: 1000 Watts
Case: 3
Ratings: 5VDC @ 80A, 2VDC @ 20A, 5VDC @ 20A, 12VDC @ 10A, 12VDC @ 10A, 24VDC @ 5A, 24VDC @ 5A

Model VX1F-YY
Total Power: 1500 Watts
Case: 4
Ratings: 5VDC @ 120A, 2VDC @ 30A, 5VDC @ 30A, 12VDC @ 15A, 12VDC @ 15A, 24VDC @ 8A, 24VDC @ 8A

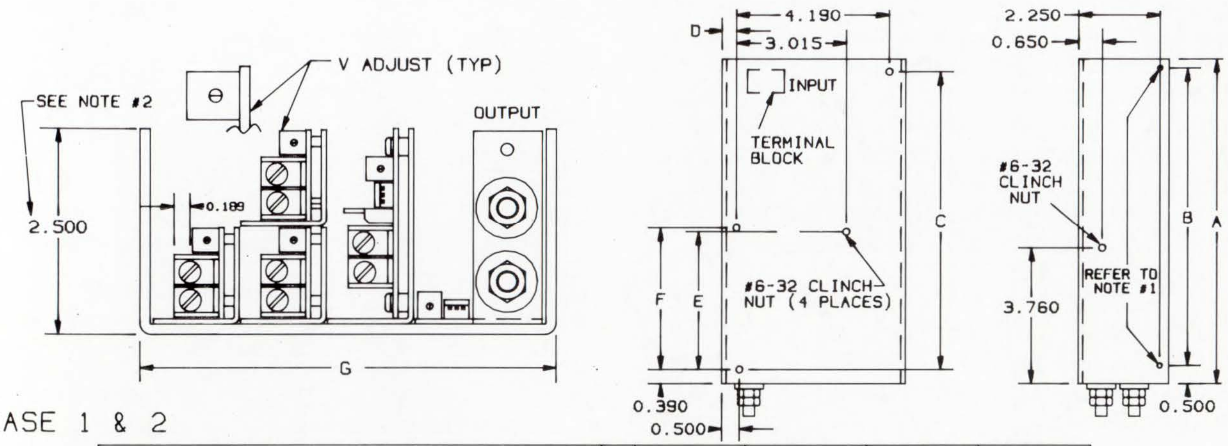
OPTIONS

Code	Function	Code	Function
00	None	04	EMI Filter
01	Power Fail	32	Cover
02	Auto Ranger	64	Fan Cover

Notes:

1. All 5VDC outputs adjustable to 5.2VDC. Others trim adjustable ±5%.
2. On models VX1E-YY and VX1F-YY the max. total power for the sum of outputs #1 to #3 must not exceed 500 watts and 750 watts respectively.
3. Models VX1E-YY and VX1F-YY include built-in fan.
4. Models VX1E and VX1F require EMI Filter option to meet FCC and VDE Class A for conducted emissions.

DIMENSIONS



CASE 1 & 2

NOTES:

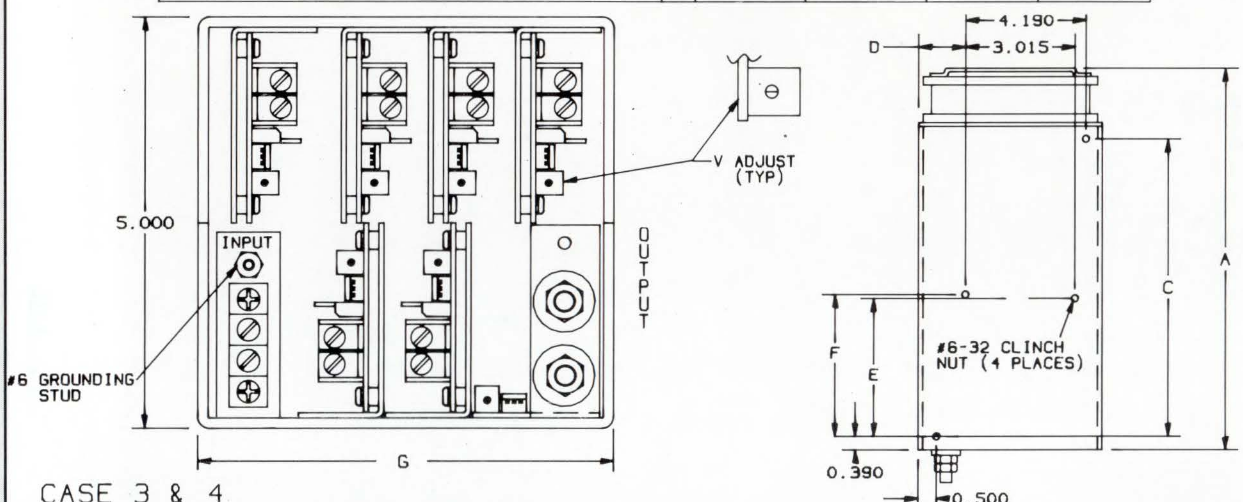
(1) WITH COVER (#6-32),
W/O COVER (.150 DIA.)

(2) W/FAN COVER UNIT HEIGHT (4.100)

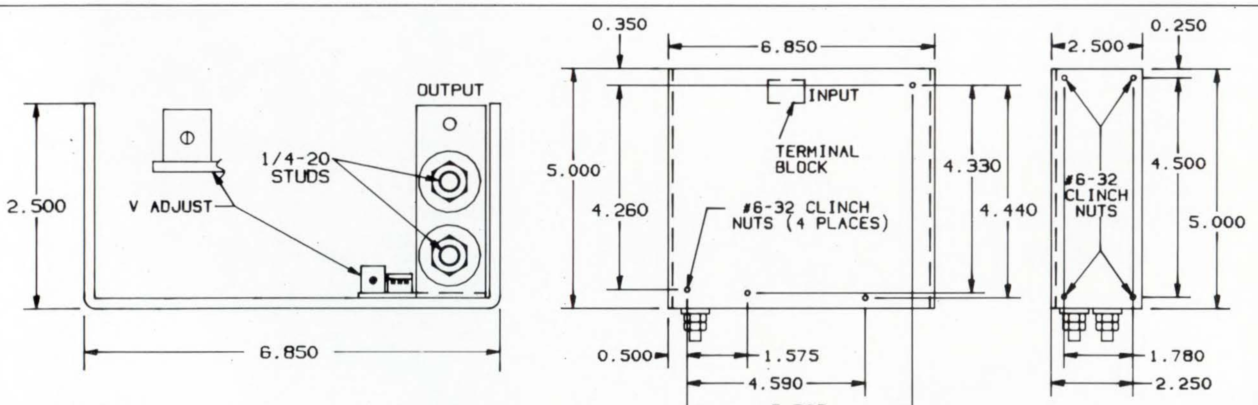
(3) TERMINAL BLOCKS (#6-32)

(4) STUDS (1/4-20)

	CASE 1	CASE 2	CASE 3	CASE 4
	400/500 W	600/750 W	1000W	1500W
A	9.000	9.630	10.400	11.000
B	8.250	8.880	-----	-----
C	8.260	8.890	8.260	8.890
D	.410	.425	.410	.425
E	3.820	4.450	3.820	4.450
F	3.930	4.560	3.930	4.560
G	5.050	5.200	5.050	5.200



CASE 3 & 4



CASE 5

Deltron inc.

290 WISSAHICKON AVENUE, P.O. BOX 1369, NORTH WALES, PA 19454
PHONE: 215/699-9261 • FAX: 215/699-2310

Int'l. Units: Delaire • Sallynoggin Road, Dun Laoghaire, Co. Dublin, Ireland. Tel: (01) 851411 Prefixes – from U.K. – (0001)–Int'l. + 353–(1) Telex: 30442DEL EI
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CAE & SOFTWARE DEVELOPMENT TOOLS

Enhanced Real-Time OS For 68000 Family

- *Provides SCSI support for hard- and floppy-disk drives*
- *Lets you install boot files on magnetic tape*

OS-9 version 2.4 is an enhanced version of the real-time operating system for Motorola's 68000 family of µPs. You can perform all software-development tasks either on a PC or Unix host computer, or on the target 680X0 system; the compilers (C, Fortran, Pascal, or Basic) produce position-independent, re-entrant, ROMable code. New communications facilities support the 68332 communications controller, as well as evaluation boards that use this chip. Other new features include the SCSI common-command set, as well as SCSI connect/disconnect and device-installation commands. A random block-file manager supports write-through caching; you can set the cache size and enable or disable the cache, and you can get a report on usage statistics. The random block-file manager also supports variable sector sizes, which can be any integral power of 2—from 256 to 32,768 bytes. The file manager supports noncontiguous boot files whose size is limited only by the hardware device. Professional OS-9 includes the OS, a compiler, a screen editor, a debugger, file managers, and utility programs. 32-bit 680X0 CPUs, $1150; 16-bit CPUs, $800; industrial OS-9, including OS, a sequential-character file manager, and interprocess-communications manager, 32-bit CPUs, $425; 16-bit CPUs, $275.

Microware Systems Corp, 1900 NW 114th St, Des Moines, IA 50325. Phone (515) 224-1929. FAX (515) 224-1352. **Circle No. 351**

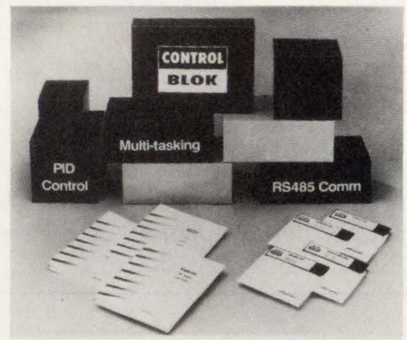
Spice Postprocessor

- *Provides custom windowing interface*
- *Lets you view and compare waveforms from several output files*

Intuscope version 3.1 is a major upgrade of postprocessor and graphical data-analysis package. Version 3.1 provides a custom windowing interface that allows you to select, view, and compare waveforms from several Spice output files simultaneously. Special program options let you display data from ac, dc, transient, and distortion analyses without having to manipulate the net list. The waveform calculator lets you perform cursor-based measurement, waveform arithmetic, and engineering functions, such as waveform construction, polynomial regression, smoothing, convolution, or filtering. You can direct report-quality graphics to laser or dot-matrix printers, or to pen plotters. The program works with data produced by any Berkeley Spice-compatible simulator, including the vendor's IsSpice. The program runs on IBM PCs that have at least 640k bytes of RAM, a math coprocessor, an EGA, VGA, or Super VGA monitor, and a DOS 3.1 or later version. Version 3.1, $325. Current users can upgrade for $100.

Intusoft, Box 710, San Pedro, CA 90733. Phone (213) 833-0710. FAX (213) 833-9658.

Circle No. 352



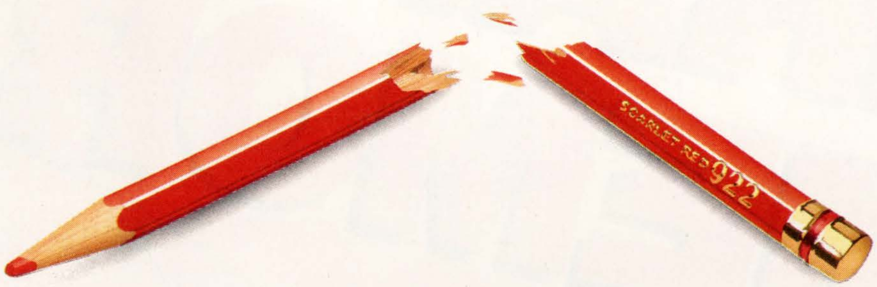
Process-Control Library Of PID Functions

- *Routines keep track of a loop's setpoints and coefficients*
- *Triggers alarms when outputs exceed a specified threshold*

The PID Blok library contains routines for creating, tuning, and executing feedback control loops that use PID (proportional, integral, derivative) algorithms. These routines calculate the difference (error) between the current value of a process variable and the desired setpoint, as well as the values that control hardware should receive in order to bring the variable back to the setpoint. Using the PID routines in combination with the vendor's multitasking library, Divvy, you can update as many as 16 PID loops in real time. The PID routines can set alarms whenever control outputs fall outside a preset range applicable to the controlled device; they can also set independent high

CADRE THE SHORTEST DISTANCE BETWEEN PROMISE AND PRODUCT

Maybe it's time to re-evaluate your software maintenance tools.



It's the biggest job you have. And probably one of the most important. So why does it have to be so difficult?

Too often, the burden of software maintenance falls onto people who weren't around when the code was written. People who need a long time to get up to speed on it, especially when the documentation is poor or when lines of code run into the millions. The risk is high for errors, frustration, lost time — even staff turnover.

Wouldn't it make sense to give your staff a tool that lets them analyze the high-level structure of your existing code — before they're overwhelmed by the details?

Cadre has just what you need. Our reverse engineering tools — for both C and Ada — let you view your source code from an architectural level, shedding light on its structure and purpose. Your people have an easier time maintaining, upgrading, or reworking the code to achieve your maintenance or reuse objectives.

The benefits are obvious. Virtually at a glance, you know what you have and what you can do with it. You know whether it needs just a little rework or a major rewrite. And you don't waste time, because you can see up front how any work you do will affect other parts of the program.

On top of that, those brave souls who tackle your software maintenance suddenly become more efficient, less likely to be frustrated, able to work faster and give you more real value for the time they put in. And they feel better about themselves.

Reverse engineering is just one of the Team*work*® life cycle solutions made possible by Cadre's *Unified* CASE® strategy. Cadre eases your development process with an open architecture that integrates the best tools — yours, ours, or anybody's — into your unique environment. The philosophy is simple: to minimize the distance between what you promise and what you deliver.

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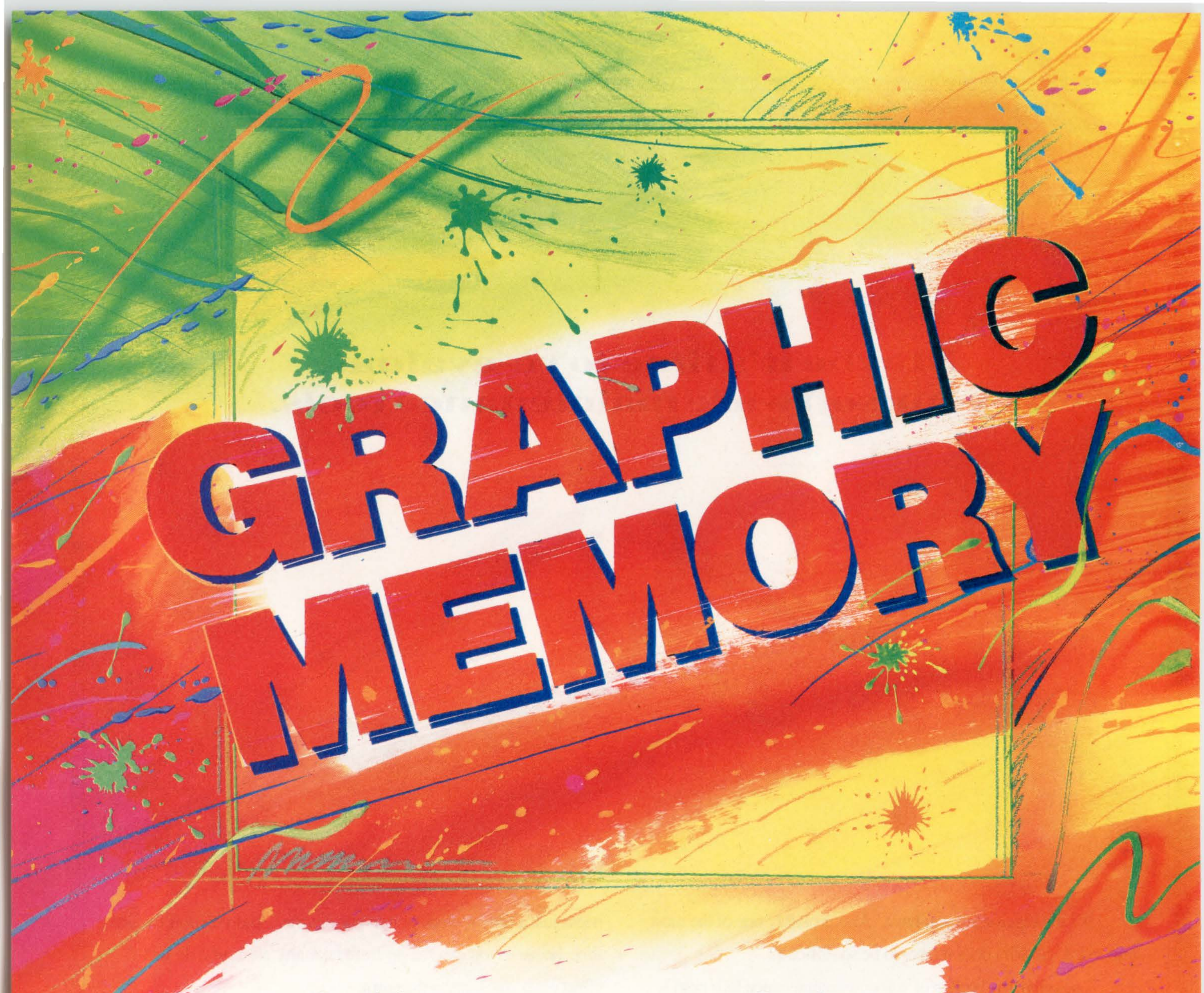


A full spectrum of choices.

Device	Organ-ization	Speed (ns)	Package	Micron Part #	Availability	VGA	8514	Super VGA	TIGA-340™	XGA	MAC®	Work-station	Multi-media
						Applications							
1 Meg DRAM	x4*	70 – 100	DIP, ZIP, SOJ	MT4C4256	Now	●		●					
	x16*	80 – 100	ZIP, SOJ	MT4C1664/65/70	Now	●	●	●		●			
4 Meg DRAM	x16*	60 – 100	SOJ, TSOP	MT4C16256/7	Samp. Q4 '91; Prod. 1H '92		●	●		●			
256K VRAM	x4	100 – 120	DIP, ZIP	MT42C4064	Now	●	●	●	●		●	●	
1 Meg VRAM	x4	80 – 120	ZIP, SOJ	MT42C4255/6	4255 Now; 4256 Q4 '91		●	●	●	●	●	●	●
	x8	80 – 120	ZIP, SOJ	MT42C8127/8	8127 Now; 8128 Q4 '91		●	●	●	●	●	●	●
2 Meg VRAM	x8	70 – 100	SOJ	MT42C8256	Samp. Q4 '91; Prod. 1H '92			●	●	●	●	●	●
1 Meg Triple-Port DRAM	x4	80 – 120	SOJ	MT43C4257/8	Now							●	●
	x8	80 – 120	PLCC	MT43C8128/9	Now							●	●

*Also in low power versions.

MICRON
TECHNOLOGY, INC.

2805 E. Columbia Rd., Boise, ID 83706 (208) 368-3800

CIRCLE NO. 156

and low alarms. The PID Blok library is supplied in C source code that you can compile with Microsoft C or Turbo C compilers. PID Blok, $149; Divvy, $229.

Drumlin, 1011 Grand Central Ave, Glendale, CA 91201. Phone (818) 244-4600. FAX (818) 244-4246.

Circle No. 353

Reverse Engineering Tool For VMS Languages

- *Analyzes source code to generate program structure charts*
- *Works with any of the languages supported by VAX/VMS*

Teamwork/C Rev is available to VAX/VMS users and extends the tool's reverse-engineering capabilities to programs written in Fortran, Pascal, Basic, PL/1, Macro, and Bliss, as well as C. The program interfaces to the VAX source-code analyzer (SCA), which creates libraries that include structural information about programs. Teamwork/C Rev extracts this structural information and produces structure charts within the Teamwork project environment. If you need to modify a module, the software lets you use your preferred editor or the appropriate VAX language sensitive editor from the VAX tool set. You need the VAX/VMS operating-system version 5.2 or later, and VAX SCA version 3.1 or later. Teamwork C Rev processor, $7500; browsing capability, $100/seat.

Cadre Technologies Inc, 222 Richmond St, Providence, RI 02903. Phone (401) 351-5950.

Circle No. 354

File-Transfer And Flash-EPROM Programming Tool

- *Lets you remotely update solid-state disk emulators*
- *Hosted on half-sized PC expansion board*

Flashlink, a high-speed file-transfer and flash-EPROM programming software package works with the vendor's PROMdisk III disk-emulator board. The disk emulator can emulate either a 1M-byte floppy-disk drive or as many as three floppy-disk drives, using both flash-EPROM and RAM solid-state memory. A common arrangement is to put the operating system in standard EPROM that emulates a bootable drive (A:); the application program (which may change) in flash-EPROM that emulates drive B:; and read/write files in nonvolatile static RAM that emulates drive C:. The program lets the host send new application files to remote embedded systems via modem or direct connection between RS-232C ports, at data rates as high as 115k bits/sec; automatic error detection maintains the integrity of the data. PROMdisk III disk emulator board, including Flashlink software and 1M byte of flash-EPROM memory, $495.

Micro Computer Specialists Inc, 810-208 Los Vallecitos, San Marcos, CA 92069. Phone (619) 744-8087. FAX (619) 744-9256.

Circle No. 355

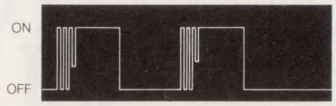
Upgraded Schematic-Capture Software

- *Provides improved user interface*
- *Net-highlighting feature includes pads and connections*

Version 4 of Schema-PCB provides an improved user interface and user-defined keyboard macros. A new net-highlighting feature indicates both the pads and the connections that you're currently routing interactively. Version 4 comes with printer drivers for both HP Laserjet and Postscript printers as well as facilities for generating editable CAM output. Options include autorouting, autoplacement, AutoCAD DXF interface, and CAM output. $975.

Omation Inc, 801 Presidential Dr, Richardson, TX 75081. Phone (800) 553-9119; in TX, (214) 231-5167.

Circle No. 356



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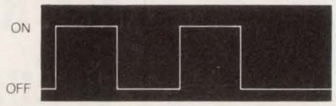

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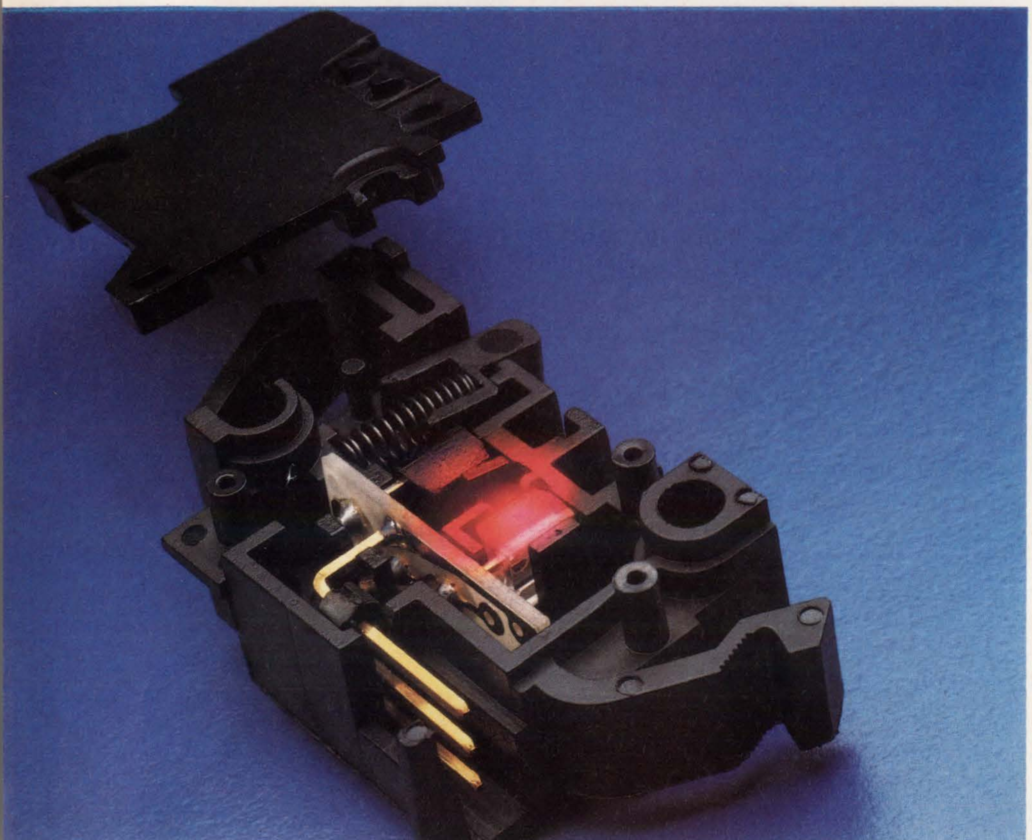


NEW PRODUCTS

INTEGRATED CIRCUITS

High-Performance Voice-Coil Drivers

- *For 5 or 12V disk drives*
- *Provide 0.5 to 1.0A drive*

The ML4406, ML4407, and ML4408 provide a voice-coil drive for either a 5 or a 12V hard-disk servo drive. The devices integrate power amplifiers, head-retract circuitry, gain switching, and power-fail detection on a single chip. The ML4406 and ML4407 can drive coils requiring 0.5A of peak current in 12V systems. The ML4408, which is targeted for smaller disk drives such as those used in laptop computers, can provide 1.0A of peak current in either 5 or 12V systems. The ML4406 and ML4407, which include on-chip power transistors, have a voltage drop of <1.5V at rated current. The ML4408 uses external pnp transistors to reduce the voltage drop to <0.8V. ML4406 and ML4407 in a 20-pin plastic leaded chip carrier, $3.50 (1000); ML4408 in a 24-pin SOIC, $3.65 (100).

Micro Linear Corp, 2092 Concourse Dr, San Jose, CA 95131. Phone (408) 433-5200.

Circle No. 363

BiCMOS Quad 12-Bit DAC

- *Has four 12-bit voltage outputs*
- *Settling time is 15 μsec*

The BiCMOS SP9345 integrates four low-power CMOS DACs with bipolar output stages to provide four 12-bit, voltage-output DACs on a single monolithic chip. The device accepts input data in either 8-bit- or 12-bit-wide words, and you can use the separately addressable double latches in front of each DAC in either conventional, semitransparent, or fully transparent modes. The DACs provide a ±10V output range with offset binary coding. Other key specifications include full-scale settling time of 15 μsec, integral and differential nonlinearity of ±½ LSB, and 12-bit monotonicity. The quad DAC, which operates from ±15V supplies, is available in 28-pin ceramic packages and 44-pin plastic leaded chip carriers. From $65 (100).

Sipex Corp, 6 Fortune Dr, Billerica, MA 01821. Phone (508) 663-9691. FAX (508) 670-9001.

Circle No. 364

Low-Voltage Quad Op Amp

- *Operates down to 1.8V*
- *Needs only 700-μA/amplifier*

The NE/SA5234 matched quad op amp operates as low as 1.8V and features rail-to-rail operation for both its input and output. The device can accept common-mode inputs as much as 250 mV greater than the supply rails, optimizing the dynamic range and helping to prevent distortion of input signals. The output swings to within 50 mV of the supply rails. The op amp has a unity-gain bandwidth of 2.5 MHz and consumes only 700 μA/amplifier, an important feature in battery-powered applications. The op amp is available in 14-pin DIPs and SOICs. From $1.56 (100).

Signetics Co, Box 3409, Sunnyvale, CA 94088. Phone (408) 991-2000. **Circle No. 365**

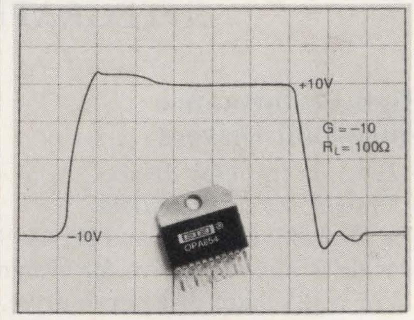
Modem IC

- *Has 2400-bps speed*
- *Compliant with CCITT standards*

The SSI 73K324L 2400-bps modem conforms to CCITT V.21, V.22, V.23, and V.22 bis standards. The quad-mode IC interfaces with standard microprocessors for control of modem functions through its 8-bit multiplexed bus. An optional serial controller bus is also available. In addition to the basic FSK modulation and demodulation sections, the modem includes synchronous/asynchronous buffering, DTMF, guard, and calling-tone generator capabilities. Handshake pattern detectors simplify control of connect sequences, and tone detectors allow accurate detection of call-progress, answer-back, and calling tones. The modem also provides diagnostic test modes. Samples of the 73K324L, which comes in DIPs and plastic leaded chip carriers, will be available in the second quarter of 1991. Approximately \$20 to \$25 (10,000).

Silicon Systems, 14351 Myford Rd, Tustin, CA 92680. Phone (800) 624-8999; in CA, (714) 731-7110. FAX (714) 669-8814.

Circle No. 366



High-Current Op Amp

- *200-mA output capability*
- *700-MHz bandwidth*

Offering a combination of high output current and high speed, the OPA654 op amp can deliver 200 mA into a 50Ω load (±10V), and can slew to 750 V/μsec. The op amp also features a gain-bandwidth product to 700 MHz, a maximum settling time of 150 nsec to 0.1%, and an input bias current of 50 pA. The device, which operates from ±5 to ±18V supplies, uses external compensation. This feature lets the user optimize the device's open-loop gain and phase characteristics to the desired closed-loop gain, load, and dynamic characteristics. OPA654, in 8-pin metal TO-3 package, \$22.95; in 11-pin plastic SIP, \$14.30 (100).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (800) 548-6132; in AZ, (602) 746-1111. BBS (602) 741-3978 (300/1200/2400 8,N,1).

Circle No. 367

Caller-Identification IC

- *Identifies incoming phone numbers*
- *Decodes FSK modem signals*

The SC11210 caller-identification IC supports the caller-number-delivery feature in the switched telephone network. The chip receives and decodes FSK modem signals sent through telephone lines between the first and second rings. These signals transmit the caller's number to a user's premises while the phone is on hook. The CMOS device integrates a differential-input buffer, a 4-pole bandpass fil-

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featuring:
- 1 through 5 outputs: 2V, 5V, 12V, 15V, 18V, 24V, 28V, 36V, & 48V.
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Switching Power Supplies

The DCS 3kW Series power supplies designed to provide highly stable, continuously variable output voltage and current for a broad range of development, system and burn-in applications. The series currently is comprised of 3 models with voltage ranges from 0-40Vdc to 0-80Vdc and current outputs from 0-37A to 0-75A.

featuring:
- 200-250 Vac input voltage, 47-63 Hz single or three phase.*
- Ten turn voltage and current controls permit high resolution setting of the output voltage and current from zero to the rated output.
- Optional internal PFC available.
- Flexible output configuration: Multiple units can be connected in parallel or series to provide increased current or voltage.
- High frequency switching technology allows high power density, providing increased power output in a small, light package.
- Optional internal IEEE 488 interface for complete remote programming and readback capability.

*Maxmum output power must be limited to 2500 watts for single phase input below 220Vac.

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5 Output/400W Switching Power Supply

2-YEAR WARRANTY!

Incorporates features for stable, heavy duty operation, including parallel MOSFETs in a forward converter technology and overrated electrolytic capacitors. The KSA400 is designed for demanding service in computer and data processing equipment, as well as others needing multiple, adjustable outputs. Built to meet UL, CSA and TUV requirements, and provides EMI protection to FCC and VDE 0871, level 1.

featuring:
- 5 voltage ranges: Main output V1, 5V: outputs V2, V3 & V4, 5-15V; output V5, 12-24V.
- 300 W output (convection); 400W output (forced air cooling).
- 115/230 Vac selectable inputs, 47-63 Hz, single phase.
- Overvoltage protection standard (V1 output).
- Overload protection standard (all outputs).
- Remote sensing standard (V1 output).
- Power fail standard.
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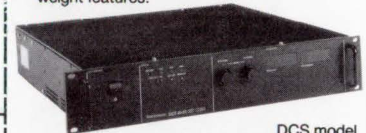

DCS model

3kW DCS Model

5-YEAR WARRANTY

The DCS series 1kW Programmable Switch-mode power supplies are a lightweight, low cost solution to many DC requirements. New design provides excellent performance for a wide variety of applications and complies with FCC Part 15, subpart J, Class A, which clearly defines the limitations of conducted and radiated noise. Choose from 9 models: 0-8 to 0-600 Vdc. Standard features include remote programming, 10-turn V&I pots, indicator lamps (V, I, OVP, remote shutdown & remote/local), On/Off switch (with resettable circuit breaker), 3.5 digit voltmeter on sense line, 3.5 digit ammeter (green LED type). Optional IEEE 488 plug-in programming PC card. Line & load regulation: 0.1%; Ripple: 10-100 mV rms. Dual selectable input: 100-132/200-264 Vac, 47-63 Hz, 1 phase.

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ter, an FSK demodulator, a user-selectable energy-detect circuit, and a clock generator. Depending on the setting of the energy-detect circuit, the IC will either pass or block the data from the FSK modem. The IC accepts a 3.57-MHz clock and uses it to generate the internal timing. The IC comes in an 8-pin package. The 14-pin device provides support for power-down and call-progress detect functions and has four energy-detect levels. Approximately $2 (10,000).

Sierra Semiconductor, 2075 N Capitol Ave, San Jose, CA 95132. Phone (408) 263-9300. FAX (408) 263-3337. **Circle No. 368**

Pro-Logic Dolby Surround-Sound Decoder

- *Features autobalance function*
- *Includes center-mode control*

The SSM-2125 combines all the core functions of a complete Dolby Pro-Logic surround-sound decoder on a single chip. The first to integrate an autobalance function, the device also includes an active decoding matrix, center-mode control, and a noise generator. Autobalance provides dynamic correction of left-right input signal-level imbalance, eliminating the need for manual adjustments. According to the company, the on-chip autobalance function replaces as many as 24 active and passive components. In all, the decoder integrates 30 op amps, 10 voltage-controlled amplifiers, a conveyor amplifier, two dual-output rectifiers, two log-difference amplifiers, comparators, random logic, and a digital noise source. A user-selectable bypass mode provides a 2-channel signal path without the need for external relays. Thin-film resistors and laser trimming eliminate the need for external gain and offset trimming. The decoder's 100-dB dynamic range and 0.015% THD provide an 18-bit equivalent performance. The decoder comes in a 48-pin plastic DIP. From $15 (100).

Analog Devices Inc, Precision Monolithics Div, 1500 Space Park Dr, Santa Clara, CA 95052. Phone (408) 562-7513. **Circle No. 369**

Analog I/O Subsystem For Workstations

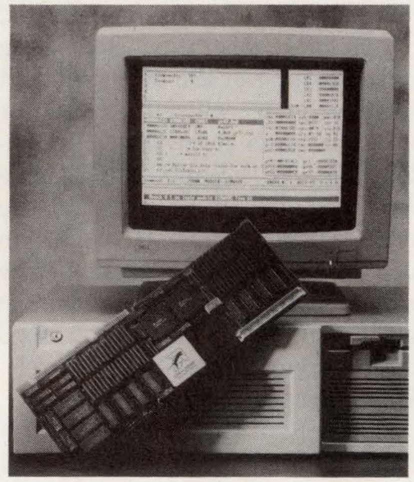
- *Records, replays, and allows graphical editing of data*
- *Handles two 14-bit inputs and 14-bit output at once*

Desklab, a 14-bit analog input/output subsystem (two inputs, one output) connects to Unix- and VMS-based workstations via a SCSI interface. To the workstation, the subsystem appears to be a disk drive. The system records, replays, and permits editing and analysis of real-time data. You can access application-development tools from the command line, from shell scripts, or via program calls to a C-language function library. Application programs (for example those for speech recognition) can also access the subsystem. The system includes a microphone input, 16 digital I/O lines, and two RS-232C ports that operate to 38.4k bps. The system can include an optional 1.44M-byte MS-DOS-compatible floppy-disk drive and 45M-byte hard disk. $5500.

Gradient Technology Inc, 95B Connecticut Dr, Burlington, NJ 08016. Phone (609) 387-8688. FAX (609) 387-5001. **Circle No. 374**

Development-Tool Set For Am29000

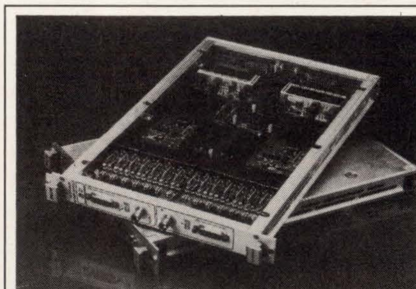
- *Has debugger interface, compiler, and downloader*
- *Execution board can include 32M bytes of memory*



The Nice-29K is a set of software and hardware development and debugging tools for code written to run on Advanced Micro Devices' AM29000 RISC µP. The tools work with IBM PC/ATs and compatible machines. Included in the tool set are a native compiler, an interface to Microtec Research's Xray29K debugger, and a high-speed download facility. The hardware portion of the tool set is a 33-MHz execution board that can contain as much as 32M bytes of RAM. With these tools, the typical duration of a compile/download cycle for a moderately large C program is 2½ minutes. Tool set, $11,600; evaluation board, $4995.

Step Engineering, Box 3166, Sunnyvale, CA 94088. Phone (800) 538-1750; in CA, (408) 733-7837. FAX (408) 773-1073.

Circle No. 375



C-Size VXIbus I/O Modules

- *16-bit ADC takes 200k samples/sec*
- *Simultaneous S/H circuit has 16 channels*

The DBS 8700 is an 8-channel, 16-bit A/D conversion module that takes 200,000 samples/sec. The DBS 8710 is a 16-channel simultaneous sample/hold board compatible with the ADC. It maintains time correlation between channels to ±200 psec. The DBS 8720 is a 32-channel multiplexer also compatible with the ADC. Each of the three modules is a C-size plug-in for the VXIbus. The ADC board includes an instrumentation amplifier whose software-programmable gain can be changed on a channel-by-channel basis. The board also incorporates a sequence controller that permits continuous data acquisition without host intervention. Onboard RAM stores scan sequences that include gain and sample rate for each channel. DBS 8700, $4000; DBS 8710, $3900; DBS 8720, $1295. Delivery, six to eight weeks ARO.

Analogic Corp, 8 Centennial Dr, Peabody, MA 01961. Phone (508) 977-3000. FAX (508) 532-6097. TLX 6817144. **Circle No. 376**

Icon-Based Test-Development Software

- *Provides graphical prompts to operators*
- *Includes Dispatch and Execute icons*

Wavetest, an icon-based software package, facilitates development of programs for control of data acquisition and testing. Version 3.0 offers these features: The Dispatch icon performs case selection for control of program flow, and the Execute icon lets you run other programs from within Wavetest. You can create graphical prompts to aid test operators in connecting to the unit under test or to guide them through fault diagnosis. Possible graphical prompts are schematics, block diagrams, and pictures. Version 3.0 runs under MS Windows 3.0. Wavetest 3.0, $1495; Version 2.6 users' upgrade, $495.

Wavetek San Diego Inc, 9045 Balboa Ave, San Diego, CA 92123. Phone (800) 874-4835; in CA, (619) 279-2200. **Circle No. 377**

Evaluation Board For DSP Analog I/O Components

- *Includes ADC, DAC, clock, and trigger generators*
- *Connects to the vendor's DSP boards*

The DEM-DSP102/202 evaluation board helps you evaluate and test the vendor's DSP-processor-compatible I/O components. It contains a socketed, 2-channel, 18-bit, 200k-sample/sec A/D converter (the vendor's DSP102JP); a socketed, 2-channel, 18-bit, 500k-sample/sec D/A converter (the DSP202JP); sample-rate and bit-clock generators;

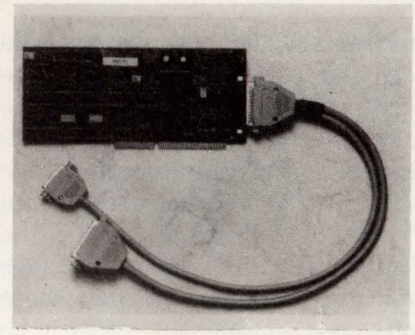
digital I/O interfaces; removable 20-kHz, 6-pole, lowpass filters; and a prototyping area. The board is compatible with the vendor's ZPB34 and ZPB3212 DSP boards. $375.

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (800) 548-6132; in AZ, (602) 746-1111. FAX (602) 889-1510. **Circle No. 378**

16-Bit Analog I/O Card

- *Includes eight analog inputs and two analog outputs*
- *Has three timers and four digital I/O lines*

The DAQ-16 1-card, 16-bit data-acquisition system runs on IBM PC/ATs and compatible computers. The board includes eight overvoltage-protected analog-input channels, two analog outputs, four digital I/O lines, and three 16-bit interval-counter/timers to control sampling of data. The ADC's maximum sampling rate is 100k samples/sec. $1395; 50k sample/sec unit, $1295.



Quatech Inc, 662 Wolf Ledges, Akron OH 44311. Phone (216) 434-3154. FAX (216) 434-1409.

Circle No. 379

Logic-Analyzer Support Package For i486

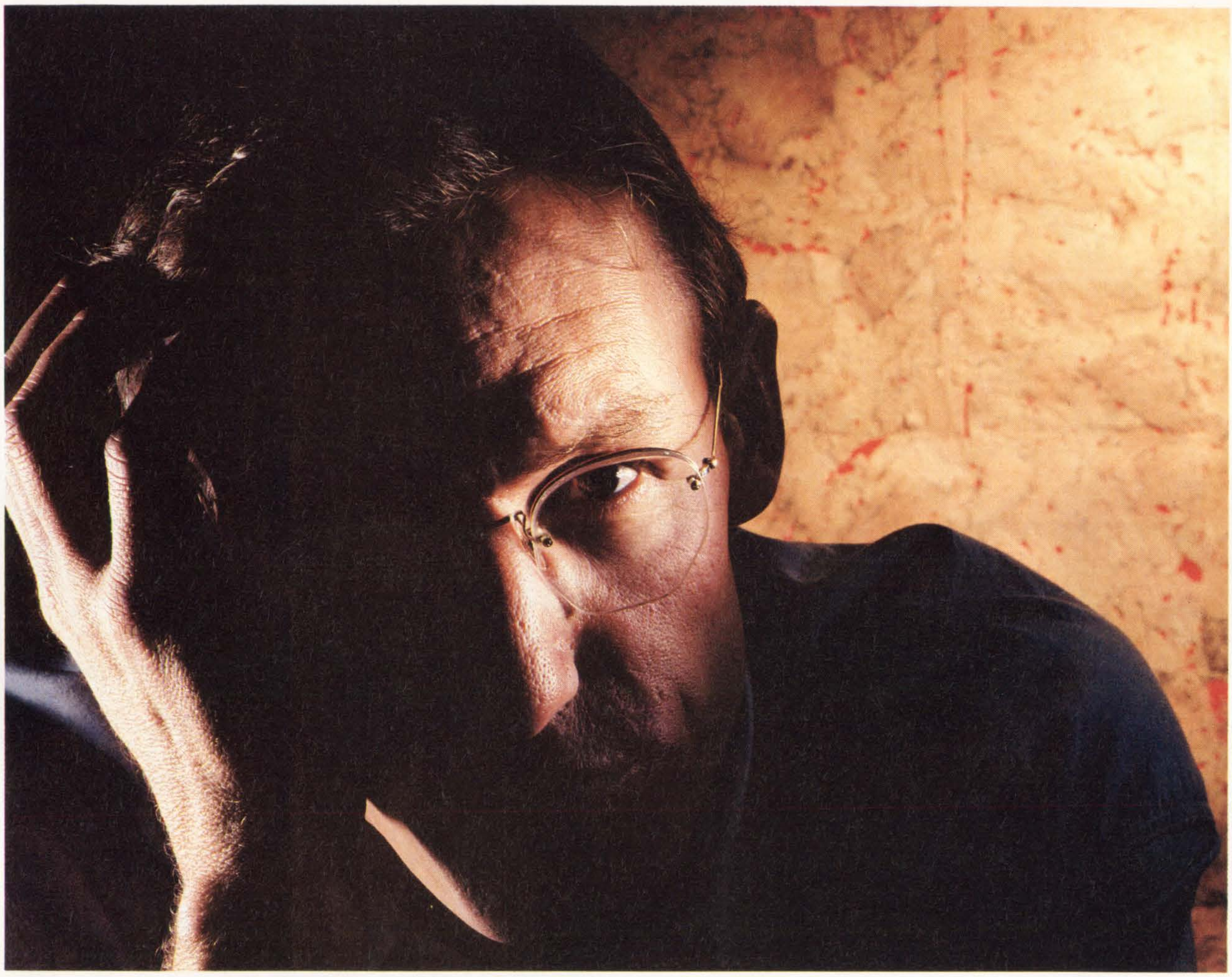
- *Displays disassembly in standard mnemonics*
- *Allows replacement of addresses with symbols*

The 80486 Map (μP-analysis package) adapts the vendor's Clas 4000 logic-analysis system to work with Intel's i486 32-bit μP. The adapter will support μP operation to 50 MHz. Among the package's functions are a display of disassemblies in Intel standard mnemonics and replacement of addresses with symbols. Included in the package is a probe board that measures $1.75 \times 5.3 \times 0.75$ in. The board fits between the μP's 179-pin package and the chip's socket in the target system. To permit use of the board where components are close to the μP socket, the package includes a zero-insertion-force socket. $2950.

Biomation Inc, 19050 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 538-9320; in CA, (408) 988-6800. FAX (408) 988-1647.

Circle No. 380

• COMPLEX EVENT TRIGGERING • REAL-TIME PERFORMANCE ANALYSIS • SOURCE LEVEL DEBUG • SIMPLE POP-UP MENU INTERFACE • UNLIMITED MACRO FLEXIBILITY FOR SUPERIOR PRODUCTIVITY • TOLL-FREE TECHNICAL SUPPORT • SUPPORT FOR 8051, 68HC11, Z80/64180, 80X86, 68000, 80C196 AND OVER 100 MORE • SURFACE MOUNT SUPPORT • BUILT-IN EPROM PROGRAMMER • ONE YEAR WARRANTY • HIGH SPEED PARALLEL INTERFACE AND MORE



THIS MAN WAS *unhappy.* THEN HE BOUGHT AN EMULATOR AND NOW HE'S *miserable. Funnily* ENOUGH WE CAN SEE WHY.

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INSTEAD HE CHOSE ANOTHER COMPANY'S EMULATOR. A MORE EXPENSIVE ONE. AN EMULATOR WITH EVEN MORE BUGS THAN HIS OWN DESIGN.

THE WHOLE SITUATION MAKES HIM WISH HE'D LISTENED TO HIS MOTHER AND GONE TO LAW SCHOOL.

BUT MORE THAN ANYTHING ELSE, IT MAKES HIM WISH THERE WAS SOME WAY, SOMEHOW, TO GET OUT OF THIS JAM WITHOUT SPENDING A FORTUNE OR WORKING ENOUGH OVERTIME TO RUIN HIS MARRIAGE.

■ THIS IS WHERE THE *UniLab 8620* ANALYZER-EMULATOR SHOULD HAVE ENTERED THE PICTURE.

IT'S A POWERFUL DEVELOPMENT SYSTEM THAT WOULD HAVE TAKEN HIM FROM START TO FINISH IN NO TIME. THANKS IN PART TO THE MANY FEATURES WE OFFER.

■ INSTEAD OF PHONING THE OTHER EMULATOR COMPANY TO GIVE THEM A PIECE OF HIS MIND, THIS MAN WOULD HAVE PEACE OF MIND.

BECAUSE THE *UniLab 8620* IS BACKED BY 11 YEARS OF ORION EMULATION EXPERIENCE. AND COMPLETE SERVICE AND SUPPORT.

■ SO DON'T MAKE THE SAME MISTAKE THIS MAN DID. CALL ORION NOW AND ASK ABOUT OUR RISK-FREE EVALUATION PROGRAM. WITH MORE EMULATION FOR LESS, YOU'RE CERTAIN TO FIND HAPPY HUNTING WHILE SEARCHING FOR THOSE MISERABLE BUGS.

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TRANSMISSION LINES

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Meta-Software's transmission line model is fully functional for transient, DC, AC, optimization and Monte Carlo analysis. HSPICE transmission lines exhibit resistive loss, time delays and reflections. A compact model allows thousands of transmission lines in a single circuit simulation.

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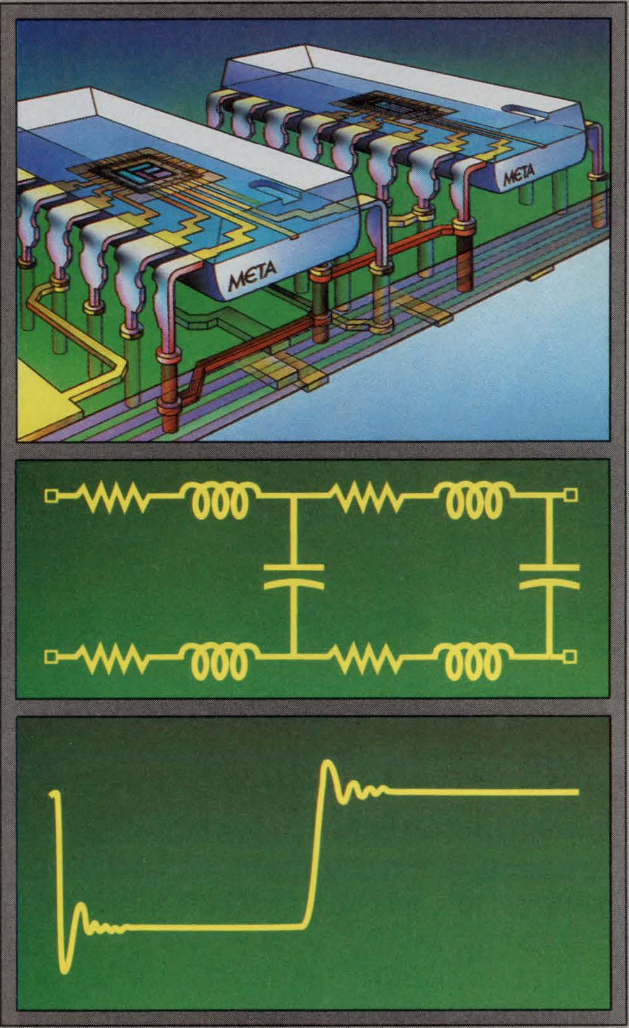

Transmission line analysis with HSPICE: Measure physical sizes of conductors (top). Simulate using output buffer and transmission line models (middle). View results (bottom).

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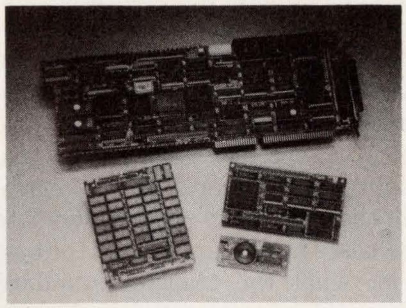


SCSI Controller Board

- *Has an option for adding a disk cache*
- *Supports the enhanced AT-attachment protocol*

The Smartcache Plus is a SCSI disk-drive controller board for ISA bus computers. It has an emulation mode for controlling one SCSI-2 or two SCSI-1 disk drives or two floppy-disk drives without the need for special-device drivers or BIOS ROMs. An optional cache module converts the board to a caching controller. The module provides from 512k to 16M bytes of cache RAM. Access time using the cache RAM is <0.5 msec. Using its enhanced AT attachment protocol, the board becomes a bus master, allowing it to overlap commands, scatter and gather data, and queue commands. Features include a 68000 µP, a 16-bit SCSI controller chip, and several ASICs. Controller board, $595; cache module with 512k bytes of RAM, $555.

Distributed Processing Technology, 140 Candace Dr, Maitland, FL 32751. Phone (407) 830-5522. FAX (407) 260-5366. **Circle No. 370**

EISA Bus Computer

- *Has 33-MHz 80486 µP and eight 32-bit slots*
- *Options include SCSI-2 bus master adapter board*

The Vectra 486/33T PC, an enhanced version of the company's Vectra 486 PC, is an EISA bus computer. It has a 33-MHz 80486 µP and eight 32-bit expansion slots. The computer supports more than 200 LAN users or 100 terminals on a Unix system. The unit's custom memory controller handles burst mode and a 128k-byte external-cache memory. Its 4M bytes of zero-wait-state memory is expandable to 64M bytes. Other features include a Weitek 4167 coprocessor socket; two serial ports; one parallel port; and hard- and floppy-disk controllers. Options include a 440M-, 670M-, or a 1G-byte SCSI-2 disk drive. A bus-master SCSI-2 adapter board is optional. The computer has certification to run Novell's Netware and Banyan's network software. It runs on SCO Unix, MS-DOS, and MS-OS/2 operating systems. Vectra 485/33T with 4M bytes of RAM and no hard-disk drive, $9499.

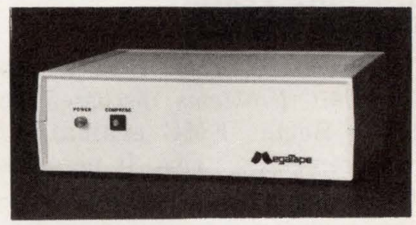
Hewlett-Packard Co, 300 Hanover St, Palo Alto, CA 94304. Phone local office. **Circle No. 371**

3-D Graphics Controllers

- *Feature 1280×1024-bit resolution and a 16-bit Z buffer*
- *Incorporate VCAD 3-D graphics engine*

The Animator and the Shader 3-D graphics controllers for IBM PCs and compatible computers have 1280×1024-bit resolution. They also feature the company's VCAD 3-D graphics engine, a TI graphics processor, a 25M-flops Mathbooster, and a 16-bit Z-buffer for real-time display of 3-D images. In <6 sec, the Shader draws the rotated crank, a common 3-D test file. The boards can draw more than 22,000 3-D shaded triangles/sec and can display as many as 16.7M simultaneous colors. The Animator has dual-frame buffers, allowing the board to construct an image in one buffer while displaying a completed image in the other frame. Both boards provide realistic images with color gradation and without banding. Shader, X/Series Model 3D-S, $5995; Animator, X/Series 3D-A, $6995.

Vermont Microsystems Inc, 11 Tigan St, Winooski, VT 05404. Phone (800) 354-0055; in VT, (802) 655-2860. **Circle No. 372**

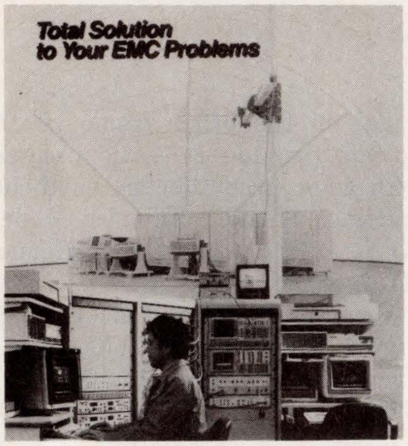


Data-Compression Module

- *Compresses data for SCSI tape drives*
- *Achieves compression ratios from 2:1 to 5:1*

The MSB-8400 Squeezebox stand-alone data-compression module compresses data from a host computer to a SCSI tape-backup drive. It features Centronics D-type input and output connectors. A high-speed VLSI chip implements a proprietary compression algorithm. Because hardware accomplishes the data compression, the unit doesn't require any modifications to the operating system, utilities, or disk drives. The module achieves compression ratios from 2:1 to 5:1 on 8- and 4-mm tape drives. The 8-mm tape drive attains a capacity of 10G bytes. The same drive also achieves a data-transfer rate as fast as 1230k bytes/sec, which is equivalent to a throughput of 73M bytes/minute. The unit measures 8.1×2.5×6.3 in. and requires a 110 or 220V ac power source. $1750.

Megatape Corp, Box 317, Duarte, CA 91010. Phone (818) 357-9921. FAX (818) 357-2369. **Circle No. 373**



Brochure Features EMC Systems

The brochure, *Total Solution to Your EMC Problems,* discusses the R2500 Series EMC evaluation/ measurement systems. It presents an evaluation of various EMC countermeasures and measurement levels. After examining various testing situations for a particular application, including counter measures, noise terminal voltage measurement, and shield-material evaluation, the publication recommends the optimal R2500 system from the company's 11 configurations. Charts and graphs complete the booklet.

Advantest America Inc, 300 Knightsbridge Pkwy, Lincolnshire, IL 60069. **Circle No. 381**

Catalog Presents VXI Products

Catalog 5091-0223EUS, *HP 75000 Family of VXI Products,* contains the manufacturer's entire line of VXI products, including the latest digitizing oscilloscope and universal counter. The text presents the system approach to VXIbus instrumentation. It also provides product descriptions, specifications, illustrations, and ordering information. The book focuses on three categories: software, an interactive test generator; firmware, standard commands for programmable instrumentation; and hardware, mainframe series B and C, DMMs, oscilloscopes, power meters, counters, sources, switches, interfaces, computers, and development tools.

Hewlett-Packard Co, Box 10301, Palo Alto, CA 94303.

Circle No. 382

Study Focuses On Pick/Unix Impact

This publication is an "executive summary" of the 1991 IDBMA (International Database Management Association) Pick Industry-Impact Study. It contains information for the Pick and Unix markets and discusses the merge of the Pick business-applications software market with the Unix mainstream. The 100-pg document discusses how the mainstream has chosen Pick, and it elaborates on promises and realities of the market.

IDBMA Inc World Headquarters, 10675 Treena St, Suite 103, San Diego, CA 92131.

Circle No. 383

Troubleshooting Approach To Test Sensors

This 4-color poster, *Troubleshooting Electronic Components,* provides a well-illustrated, troubleshooting approach for testing automotive engine sensors and actuators, using a digital multimeter. The chart presents testing of oxygen sensors, manifold absolute-pressure sensors, mass-air-flow sensors, cam and crankshaft position sensors, fuel-injection systems, the feedback carburetor, idle air-control motors, temperature sensors, and throttle-position sensors. Also included is a step-by-step diagnosis of a real-life automobile electrical problem. The poster features the 88 automotive meter as the diagnostic tool used in the examples.

John Fluke Mfg Co Inc, Box 9090, Everett, WA 98206.

Circle No. 384

Noting Semiautomatic AC Verification Of Calibrator

This application note explains how to semiautomate the calibration and verification of high-accuracy ac calibrators. The method described is a system solution, using a multirange ac/dc thermal transfer standard, the 792A, in conjunction with Met/Cal calibration software. After describing the calibration system, the note discusses how to implement the system, what the transfer standard linearity requirements are, how to determine delay times, how to verify software, and the final results.

John Fluke Mfg Co Inc, Box 9090, Everett, WA 98206.

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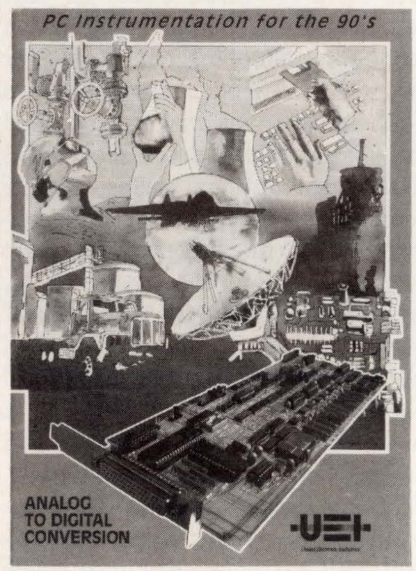

Publication Discusses PC Instrumentation

The 72-pg catalog, *PC Instrumentation for the 90s,* describes the vendor's line of PC-based data-acquisition boards, software, ADCs, DACs, and solid-state relay controllers. It provides specifications, photographs, and schematics. A selection guide and an appendix complete the publication.

United Electronics Industries, 10 Dexter Ave, Watertown, MA 02172. **Circle No. 386**

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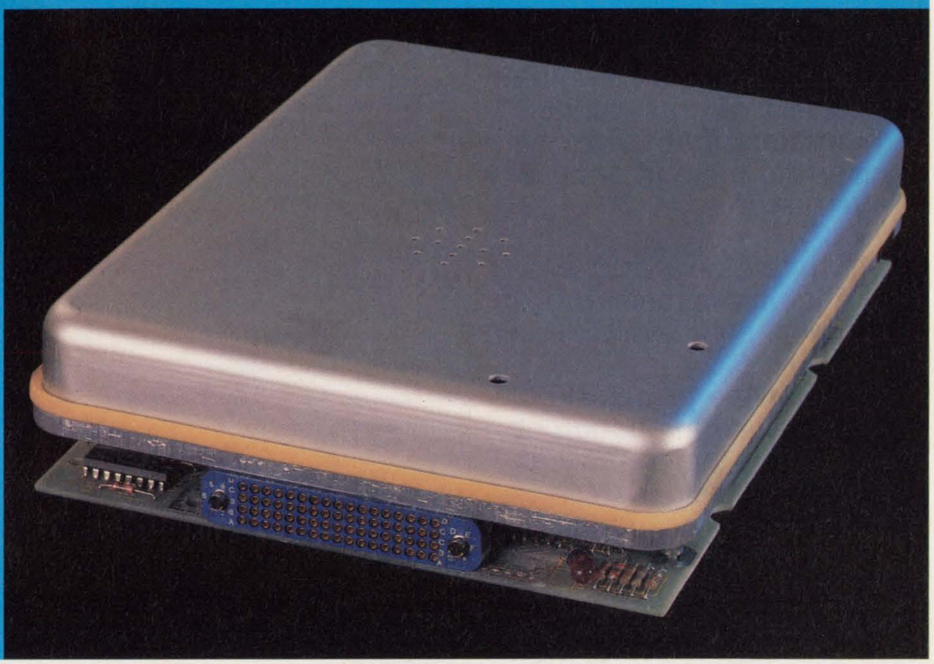

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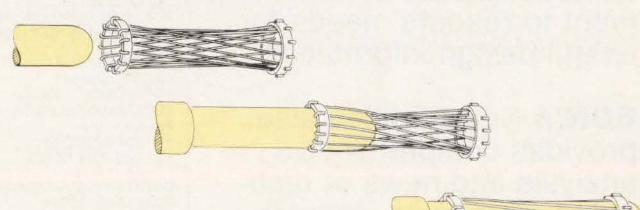

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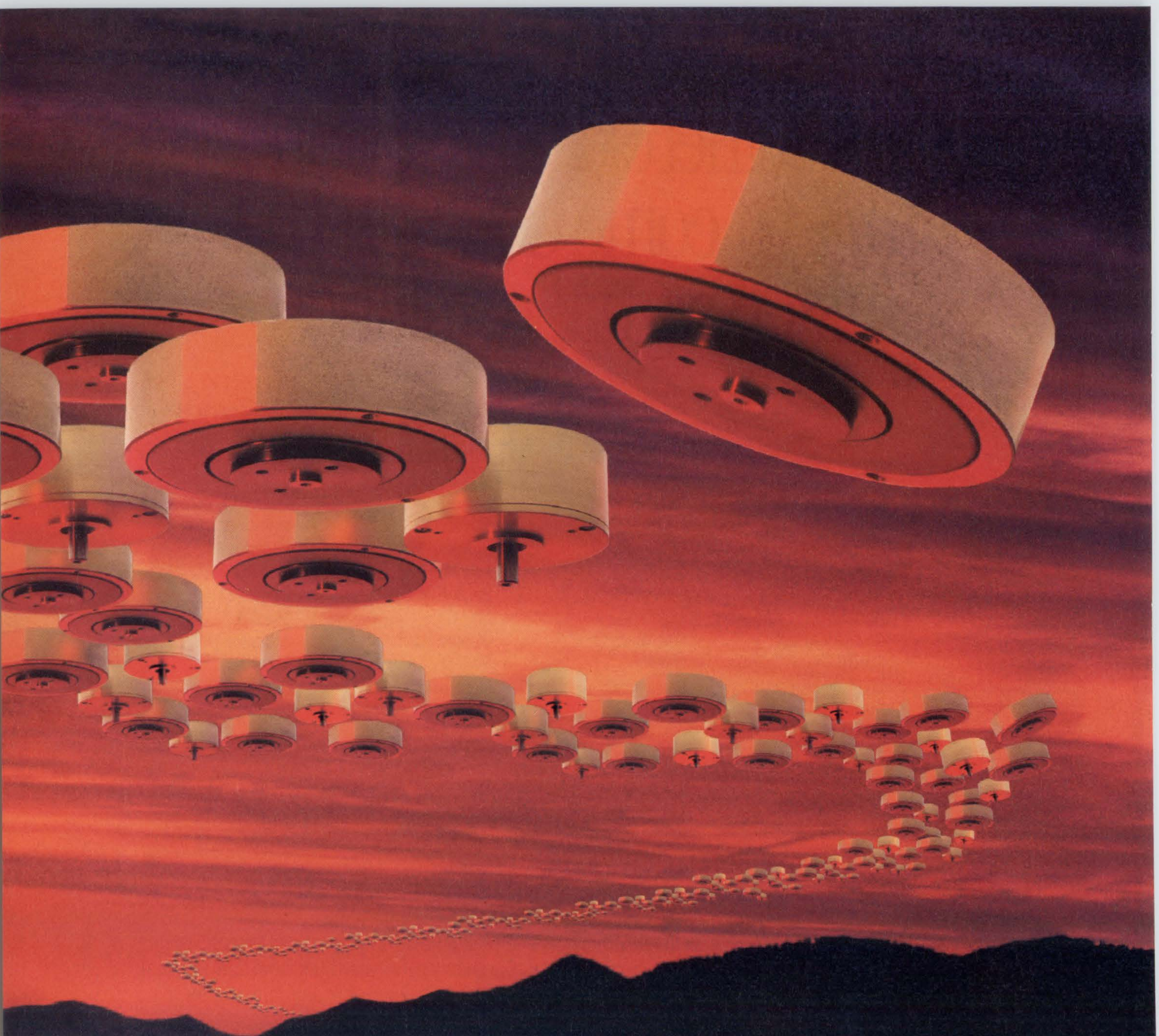

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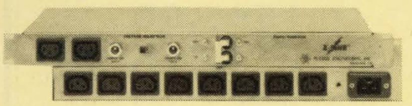

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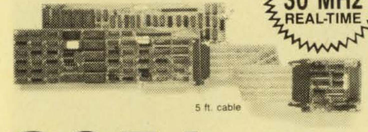

8051

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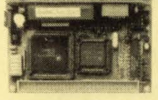

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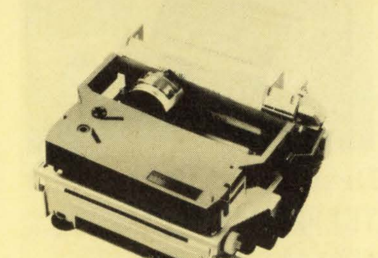

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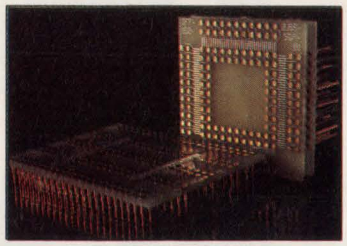

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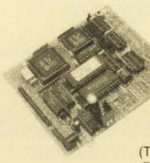

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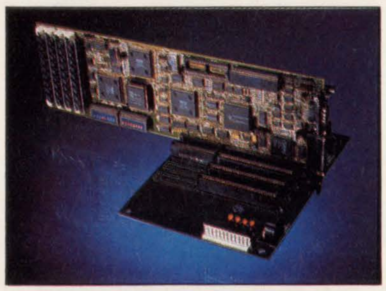

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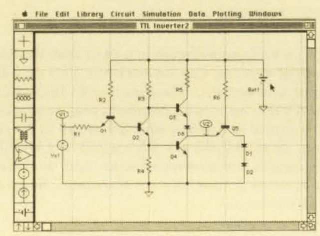

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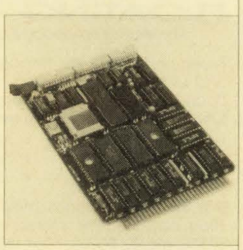

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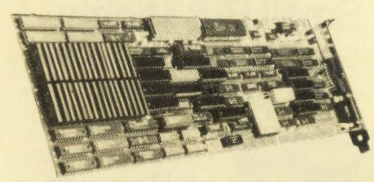

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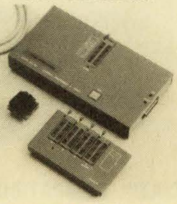

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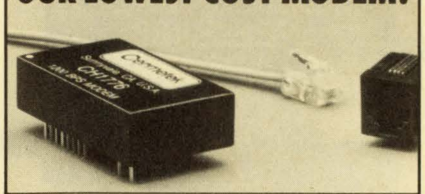

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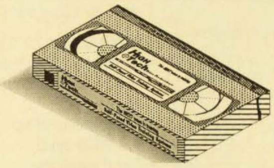

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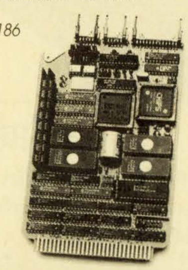

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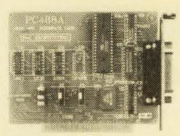

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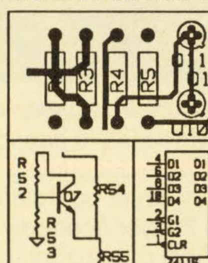

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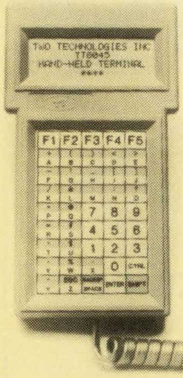

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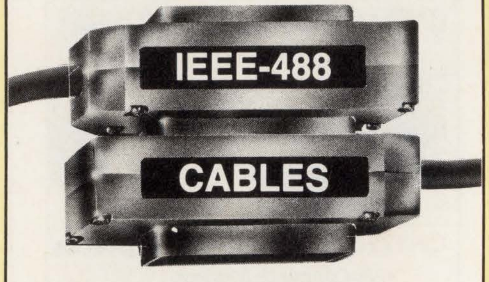

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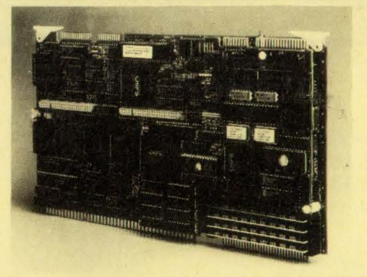

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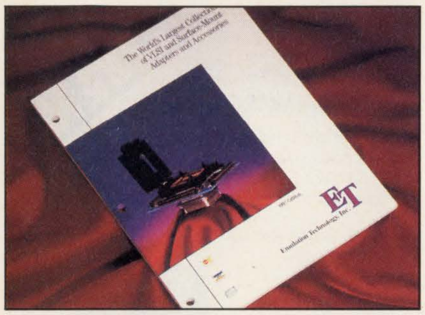

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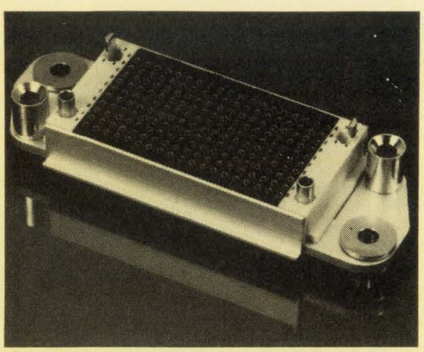

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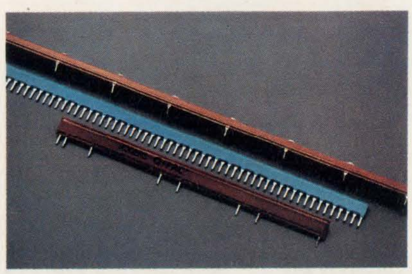

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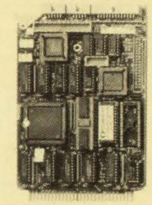

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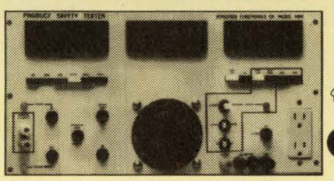

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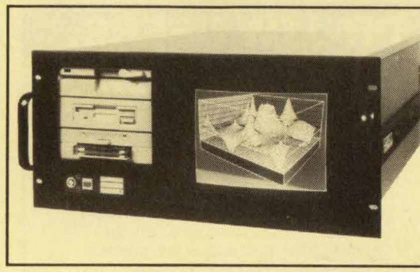

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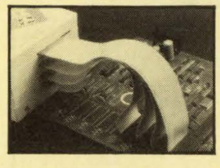

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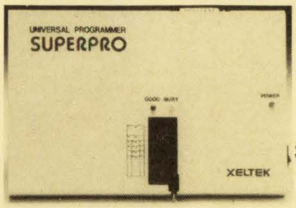

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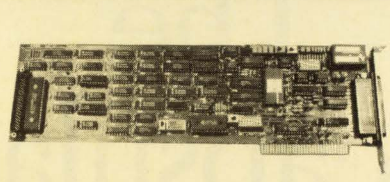

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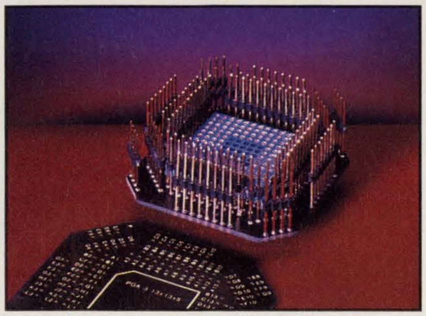

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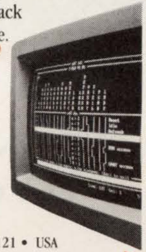

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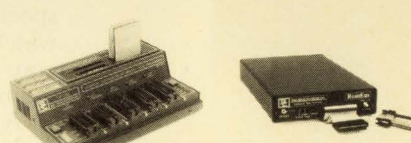

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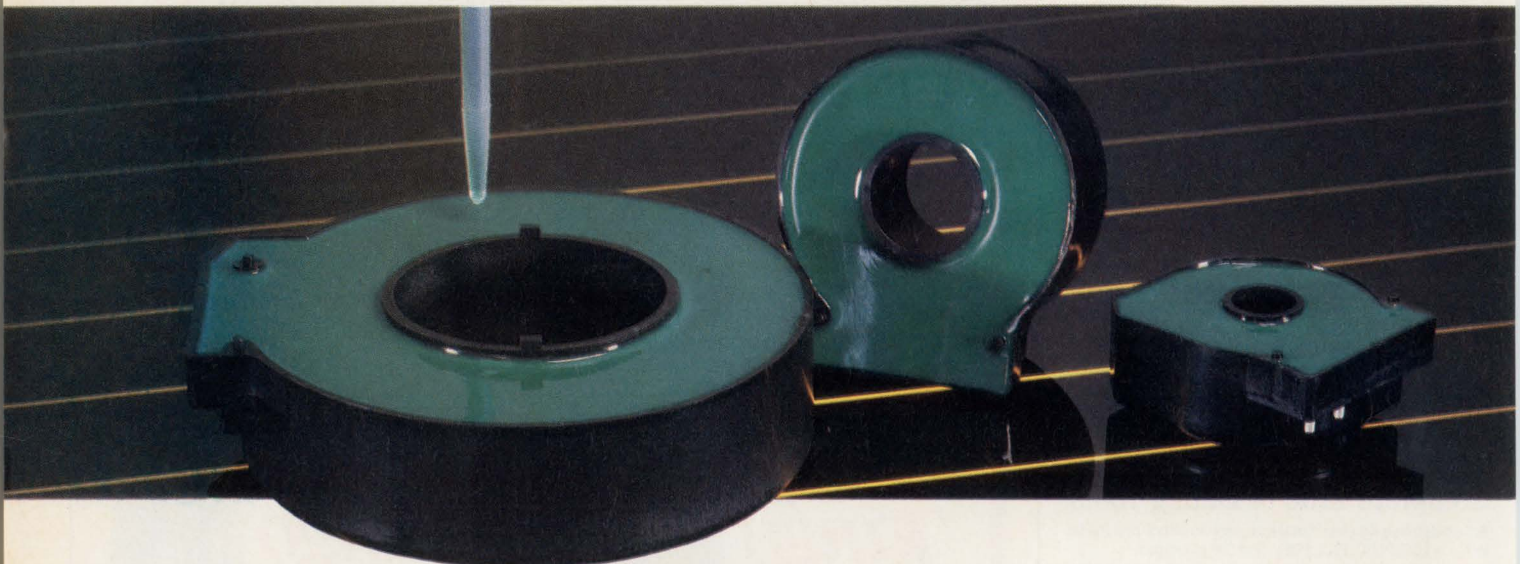

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QUESTION #1

Would you be willing to join an engineers' union?

☐ YES
☐ NO

Unions claim they have much to offer, but most engineers remain indifferent to them.

Professionals such as schoolteachers, college professors, and white-collar government workers all have large and long-established unions to represent them. For example, there are approximately 2.2 million elementary and secondary schoolteachers in America today, and more than 1.8 million of them—82%—belong to the NEA.

Very few engineers, on the other hand, are members of unions. The Council of Engineers and Scientists Organizations (CESO) is an umbrella group representing 10 small and widely scattered unions (or professional associations as most of them prefer to be called) that include engineers as members (see **box**, "The members of CESO"). CESO represents about 70,000 people—less than 3% of the estimated 2.3 million engineers in this country. Although CESO is not a union itself, it lobbies for its member organizations.

Many engineers have legitimate complaints about their salaries, benefits, and working conditions. And those are exactly the sort of concerns that unions or professional associations are supposed to deal with. Yet most engineers are reluctant to join them.

"I think it has to do with the way engineers are educated," says Edward Olson, president of the Southern California Professional Engineering Association (SCPEA). "College professors teach this idea of professionalism, that you negotiate for yourself. Students also have a tendency to believe that engineers are a part of management. Early on, the thinking is that it's unprofessional to belong to a labor union.

"As a result, when a young engineer first gets out into the workplace, he feels that he can negotiate his own wages, hours, and benefits. It takes a while before he realizes it's very difficult to negotiate those things when you're working for a large company."

Daniel Mahoney, general counsel for the Seattle Professional Engineering Employees Association (SPEEA), shares Olson's views. "Perhaps it's the indoctrination they get in engineering schools that they are professionals," he says. "They believe that it's somehow demeaning to be categorized with what they perceive to be the traditional American labor-union member."

Engineers' image of themselves

Many engineers see themselves as rugged individualists, working on projects that are almost personal, which makes them unwilling to join any organization. "The analogy I use is they come out of school and they hit a strainer," says Harold Ammond, executive director of the Association of Scientists and Professional Engineering Personnel (ASPEP). "They go off into computers, physics, all the gradations of electrical engineering, and the result is that there's nothing that makes them homogeneous."

Jay Fraser,
Associate Editor

This idea of independence that so many engineers hold dear also leads some of them to change jobs frequently. They don't join unions because they don't expect to stay very long with any firm. Ammond explains, "When he goes to work for a company, the average young person says, 'Well, I'll stay here for two years, then I'll go to another company for two years, then I'll go to a third company for two years, and every time I change jobs I'll pick up a 10% wage increase.' They think of themselves as individual entrepreneurs."

"The best union organizer is bad management."

Engineers have other doubts about unions. Some are afraid that if they joined a union and weren't happy with it, they'd find it very difficult to get out and would be obligated to continue paying dues. Union dues can run into hundreds of dollars per year. Some engineers think the dues are too high. And many engineers simply aren't convinced that a union can do anything for them.

In addition, membership in most professional organizations is voluntary. Yet the National Labor Relations Act (NLRA) requires that a union negotiate a contract for all the employees in its collective bargaining unit, whether or not they are members of the union. Some engineers see no reason to join a union when they automatically receive exactly the same benefits as union members.

This law is a constant irritation to union officials. It hinders recruiting efforts and leaves the unions with less support than they might otherwise have. "There's no question that the nonunion people are getting a free ride," says Ammond. "They get the benefits, but they don't help us in getting the maximum. That's a burden, but that's the way the law is written."

Even though the vast majority of engineers don't belong to unions, the 10 professional associations that make up CESO have been successful. Some of them have been in existence for decades and are still growing.

SCPEA was founded more than 40 years ago and currently represents about 6000 engineers and technicians, mostly at McDonnell Douglas facilities in Long Beach and Huntington Beach, CA. SPEEA is the largest member of CESO. Its membership is made up of approximately 28,000 engineers and other professionals who work for the Boeing Co in the Puget Sound area of Washington and in five other states. ASPEP was founded in 1946. It currently represents about 2000 engineers and scientists who work for the General Electric Co in Camden and Moorestown, NJ.

In some ways these professional associations act like typical unions. They negotiate the standard articles of contracts—salaries, benefits, working conditions, vacations, holidays, cost-of-living raises, and overtime compensation—and they try to protect their members' job security.

"Our contract contains the clause that nobody can be disciplined or discharged without just cause," Mahoney explains. "If someone does get disciplined or discharged, we can challenge it in arbitration and get it turned around. We provide a lot of job security for our people that wouldn't necessarily exist in a company that operated under the employment-at-will doctrine."

Professional associations also point to the protection that an established grievance procedure offers employees. "It's a very valuable thing for a professional to have that protection in regards to termination," says Olson. "The company must show just cause before they can terminate you. If you're not protected by a contract, they can let you go any time they want."

Mahoney adds, "From our observation, when they work in a collective bargaining environment, our engineers and scientists are able to act in a more professional manner. They can challenge supervision and say, 'Look, you're doing it wrong. Try it this way.' In other words, they have a forum to articulate their professional analysis of problems without fear of being disciplined. It's a win-win situation."

Different approaches to problems

These professional associations also differ significantly from ordinary unions. "We are a union within the meaning of the NLRA, but we're not a typical trade union," says Ammond. "Our problem-solving approaches aren't standard."

ASPEP developed a complex method for evaluating an employee's performance called the retention credit system. It's based on a formal review where the employee is given a numerical score. It also takes into account factors such as the type of degree an employee has, how long it has been since that degree was earned, and how long the employee has worked for the company. The retention credit system allows for more flexibility than a straight seniority system.

"I'm sure if I submitted that contract to some of the AFL-CIO unions they'd look at me and say, 'What are you, crazy? Whoever heard of a solution to a seniority problem being this complex?' But that's a reflection of the unique community we represent," says Ammond.

Some of the large national unions that belong to the AFL-CIO are staffed by full-time, salaried administrators who sometimes have no hands-on experience doing the work the average union member does. The small professional associations, by contrast, are mostly run by and for working engineers. About 85% of the members of ASPEP are electrical engineers, and there's nobody involved in the decision-making process who is not an engineer. In addition, the work that they do is mostly on a volunteer basis.

Officials of professional associations have noticed that as engineers become older and more concerned with job security they are more likely to become members. Economic hard times and the layoffs that come with them also increase interest in unions. The recession in the mid 1970s gave a big boost to union membership. But what spurs most engineers to join professional associations is what they consider to be mistreatment by their employers. "The best union organizer is bad management," says Ammond.

Of the 10 professional associations, only ASPEP has ever gone out on strike. In 1967 the members went on a 30-day strike for a new layoff policy. Before that, in 1958 and 1960, they walked out for three days each time in order to establish a merit rating system. Ammond points out that a typical trade union might strike to eliminate a merit system because management could use it to discriminate against some employees. The fact that engineers went on strike to establish one, he feels, is more proof of the special quality of their professional organization.

Although CESO has been successful, its officials see no large-scale expansion of the union movement among engineers in the near future. This is partly due to the reasons—good and bad—many engineers can give for not joining unions, but it is also partly due to the nature of the unions themselves and the limited resources they have to make their case.

"We have no budget to go out and put on a PR campaign to educate people, so what we do is not perceived by many individuals," says Ammond. "We are very introspective by nature. We work with the problems of our community and ASPEP. We really don't have the capability or the wherewithal of going out and proselytizing, or, to use the trade union term, organizing. We're just not made that way."

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The members of CESO

The Council of Engineers and Scientists Organizations (CESO) is an umbrella organization of 10 unions and professional associations that include engineers. Contact the following for more information on CESO and the 10 member organizations.

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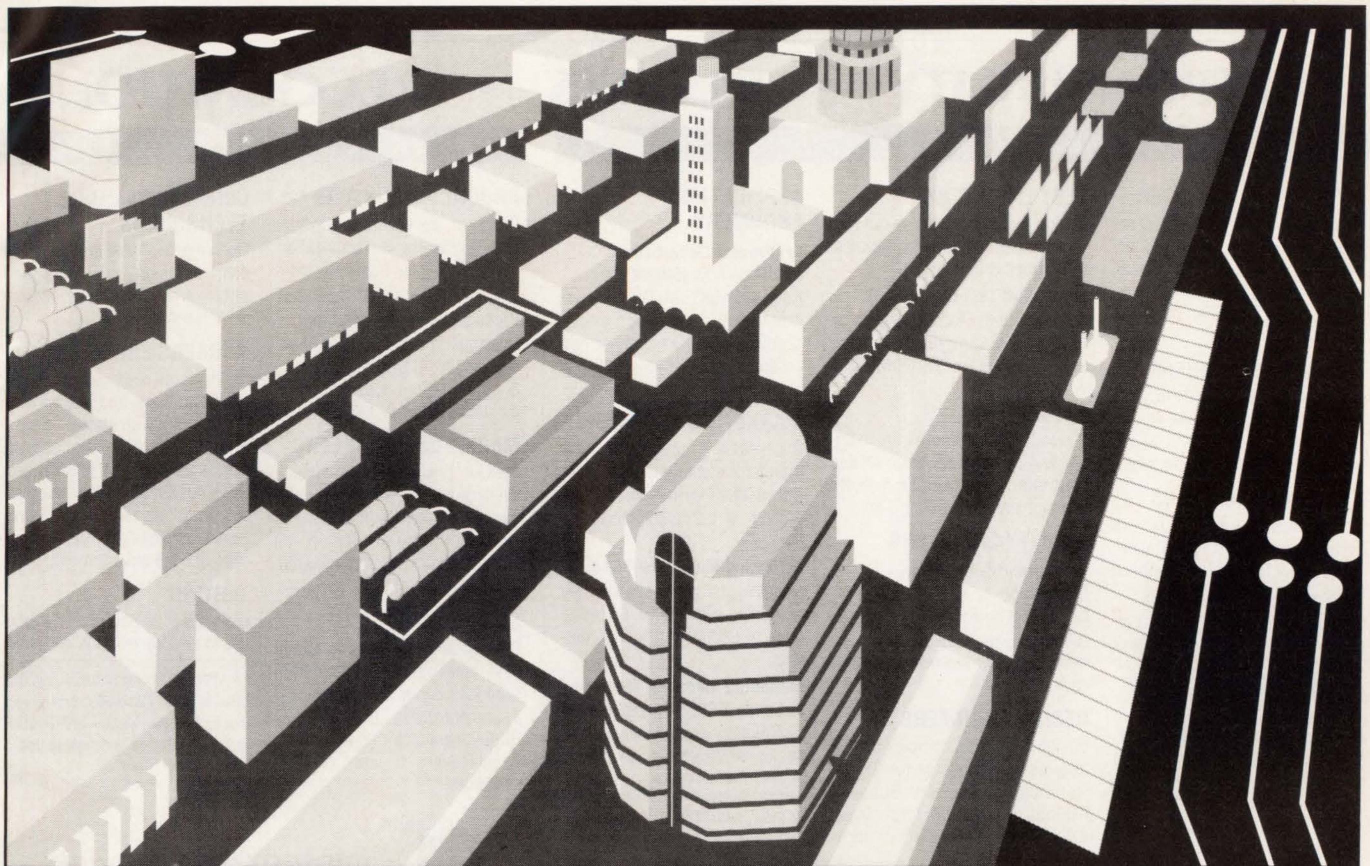

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Automatically.

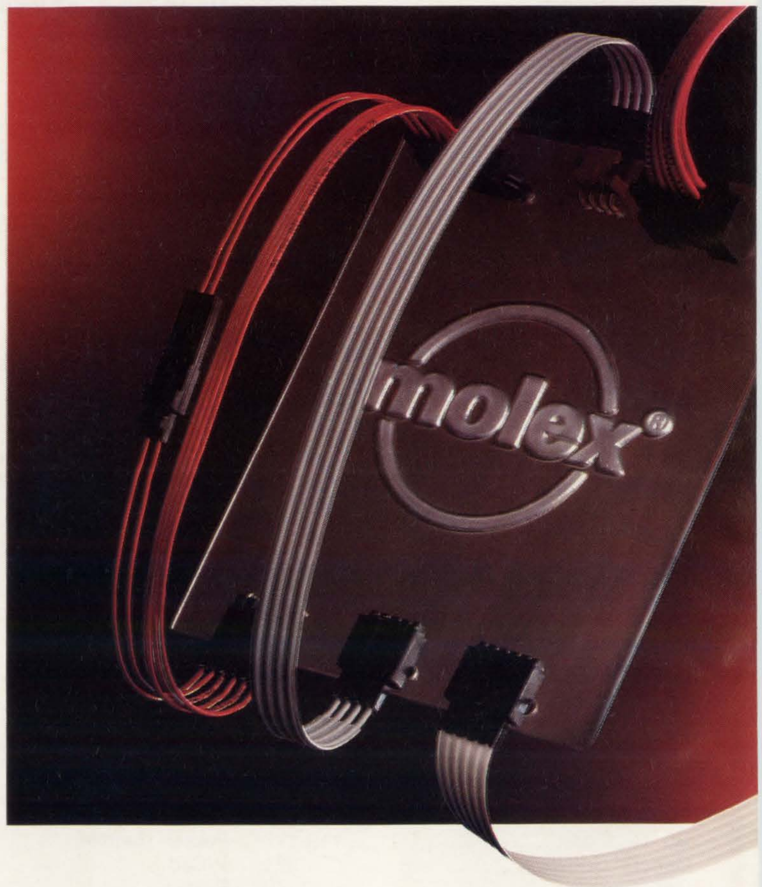
You'll find Molex SL connectors in some of the world's leading—and most dependable—makes of electrical and electronic equipment. Of course, reliability is a big reason for this preference.

But the versatility and lower applied cost that SL provides are critical factors, too, especially in systems with several interconnections.

Modular, stackable, and lower in profile, SL connectors give you virtually unlimited flexibility when you're designing wire-to-wire, wire-to-board, and ribbon cable systems.

The single-piece IDT connectors feature, pre-assembled terminals in the housings, and interconnects with locking shrouded headers. In short, they're ideal for high-speed, high-efficiency automated assembly.

Ask your Molex representative about SL connectors, and learn how they can multiply design options and automate assembly.



molex®

Bringing People & Technology Together, Worldwide℠

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CIRCLE NO. 105

NEW TRANSFORMERS FOR CLASS 2 APPLICATIONS.

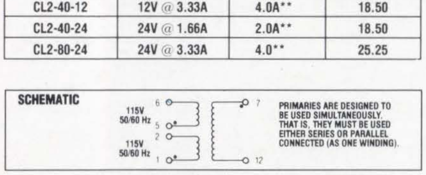
DUAL BOBBIN DESIGNS FEATURE 4000 VRMS PRIMARY AND SECONDARY ISOLATION.

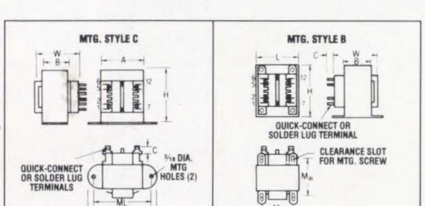
*INHERENTLY LIMITED
**NON-INHERENTLY LIMITED
MAXIMUM FUSE VALUE SPECIFIED

ALL PRIMARIES ARE 115/230 VOLT 50/60 HZ

PART NO.	SECONDARY RMS RATING	FUSE REQD.	PRICE
CL2-25-12	12V @ 2.10A	2.5A**	14.50
CL2-25-24	24V @ 1.05A	N/A*	14.50
CL2-40-12	12V @ 3.33A	4.0A**	18.50
CL2-40-24	24V @ 1.66A	2.0A**	18.50
CL2-80-24	24V @ 3.33A	4.0**	25.25

SCHEMATIC

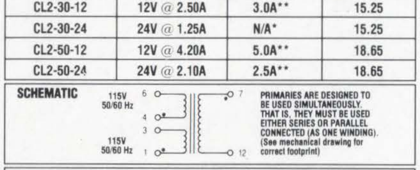


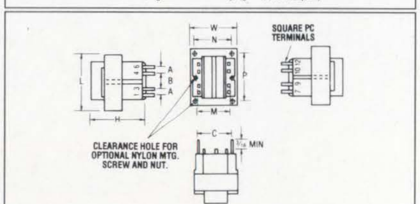


DIMENSIONS								Mtg.	Mtg.		Mtg.	
VA	L	W	H	A	B	C	Terminals	Style	ML	MW	Screw	Lbs.
25	2 13/16	1 7/8	2 5/16	2	1 1/8	5/16	3/16 (.187)	C	2 3/8	–	#6	1.25
40	3 1/8	2 1/16	2 11/16	2 1/4	1 1/8	5/16	3/16 (.187)	C	2 13/16	–	#6	1.6
80	2 1/2	2 3/8	3	–	1 3/8	5/16	3/16 (.187)	B	2	2 3/16	#6	2.8

PART NO.	SECONDARY RMS RATING	FUSE REQD.	PRICE
CL2-2.5-12	12V @ .20A	N/A*	9.00
CL2-2.5-24	24V @ .10A	N/A*	9.00
CL2-5.0-12	12V @ .42A	N/A*	9.75
CL2-5.0-24	24V @ .20A	N/A*	9.75
CL2-10-12	12V @ .83A	N/A*	10.90
CL2-10-24	24V @ .42A	N/A*	10.90
CL2-20-12	12V @ 1.66A	N/A*	13.25
CL2-20-24	24V @ .833A	N/A*	13.25
CL2-30-12	12V @ 2.50A	3.0A**	15.25
CL2-30-24	24V @ 1.25A	N/A*	15.25
CL2-50-12	12V @ 4.20A	5.0A**	18.65
CL2-50-24	24V @ 2.10A	2.5A**	18.65

SCHEMATIC





DIMENSIONS							Pin	Mtg.			Mtg. Screw		
VA	L	W	H	A	B	C	Dimensions	M	N	P	Size	Quantity	Lbs.
2.5	1 5/8	1 5/16	1 1/8	.200	.250	1.000	0.025SQ	1 1/16	–	–	#4	2	0.25
5.0	1 5/8	1 5/16	1 3/8	.200	.400	1.000	0.025SQ	1 1/16	–	–	#4	2	0.37
10.0	1 7/8	1 9/16	1 3/8	.200	.400	1.140	0.038SQ	1 1/4	–	–	#4	2	0.53
20.0	2 1/4	1 7/8	1 5/8	.400	.400	1.460	0.038SQ	1 1/2	–	–	#4	2	0.90
30.0	2 5/8	2 3/16	1 9/16	.550	.275	1.680	0.045SQ	–	1 3/4	2 3/16	#6	4	1.15
50.0	3	2 1/2	1 13/16	.600	.300	1.900	0.045SQ	–	2	2 1/2	#6	4	1.70

Signal "The American Original" introduces a new family of transformers for 2.5 to 80 V applications that require low power and a high degree of isolation. These new "Class 2" transformers feature the same dual high-temperature bobbin construction and insulating shroud originally developed for the company's very successful International Series. Available in both PC and chassis mount versions, they offer a choice of inherently limited or non-inherently limited designs and feature 4000 VRMS primary and secondary isolation.

Signal's insulation system results in very high isolation between the primary and the secondary windings, and between either winding and the core. The dual bobbin design reduces capacitance and eliminates the need for an electrostatic shield. The Class 2 dual bobbin series satisfies UL 1585 requirements and CSA safety and performance standards.

Signal transformers are available through Signal's **PRONTO** 24-Hour Off-the-Shelf shipment program. For additional technical data, contact Signal Transformer, 500 Bayview Avenue, Inwood, N.Y. 11696.

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CIRCLE NO. 108