A MORGAN-GRAMPIAN PUBLICATION

DIGITAL DESIGN

SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS MARCH 1985

- THE WORKSTATION'S ROLE IN GATE ARRAY DESIGN, PART III
- RISC MACHINES – AN ARCHITECTURE FOR THE FUTURE?
- INTELLIGENT KEYBOARDS ENHANCE SYSTEMS INPUT
- A/D CONVERTERS
- Q/UNIBUS


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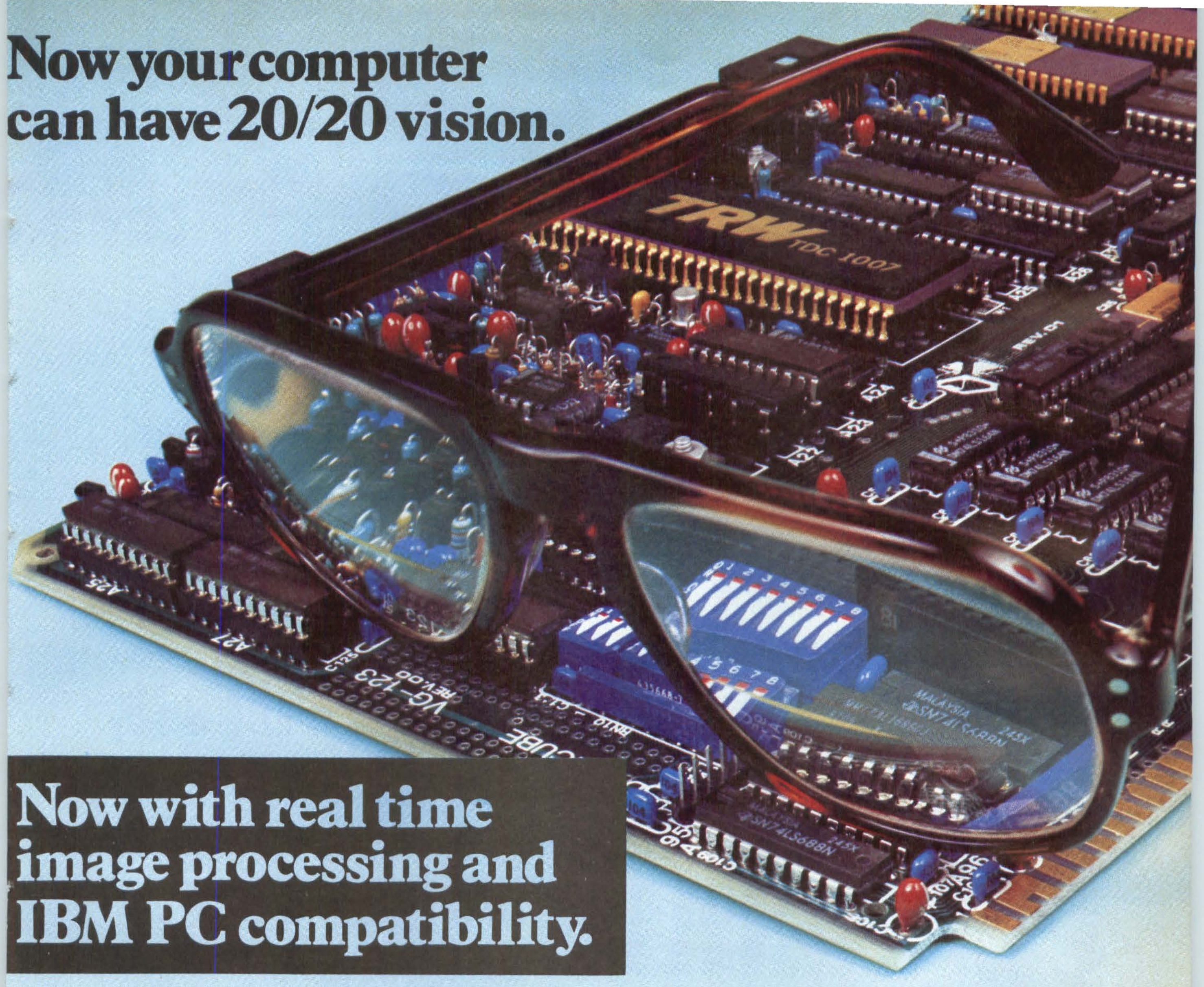

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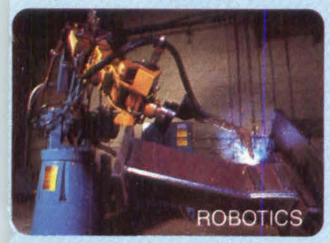

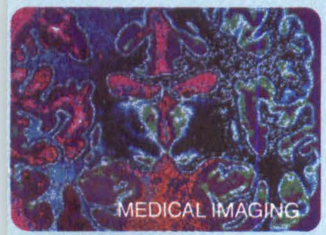

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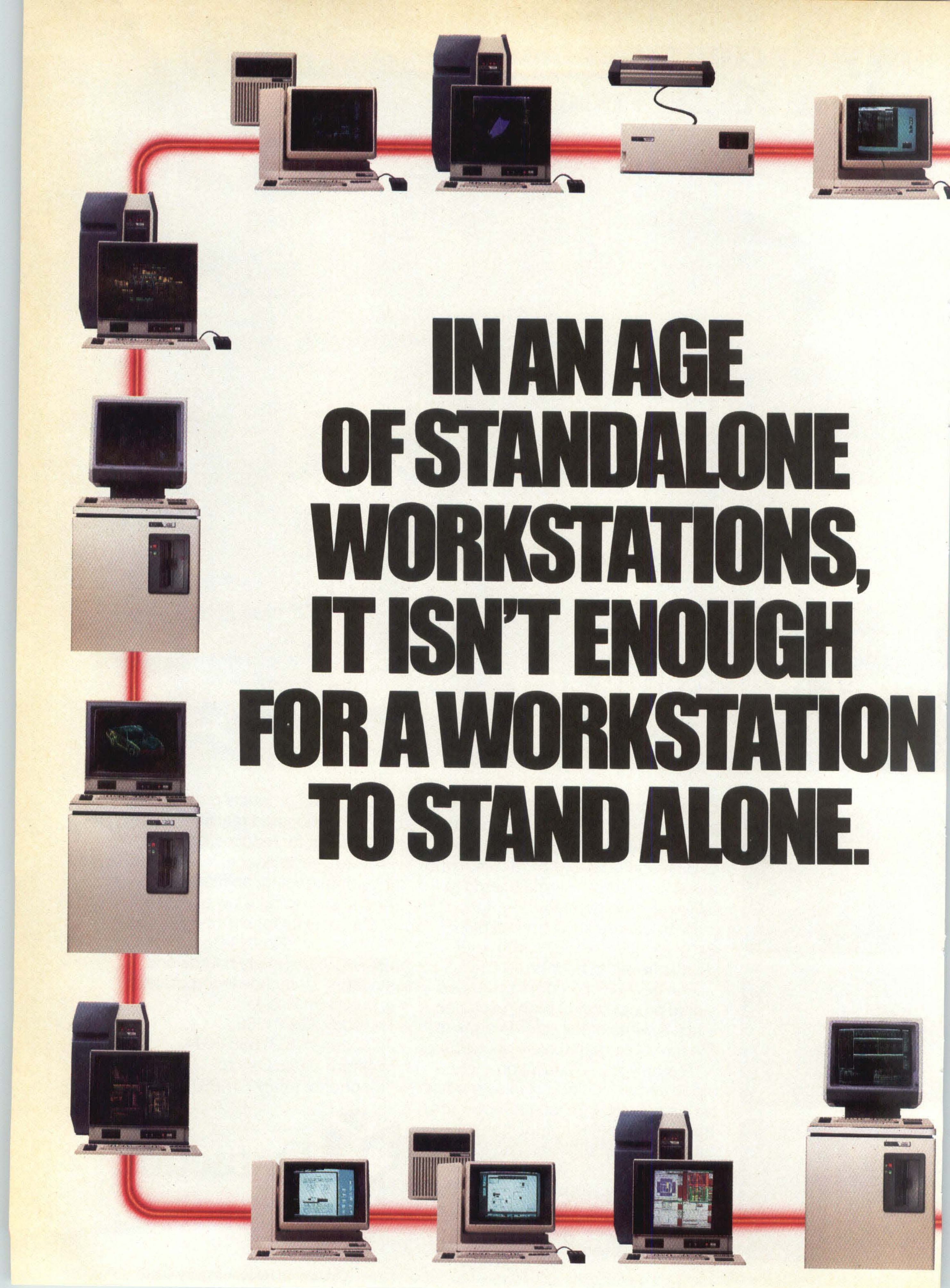
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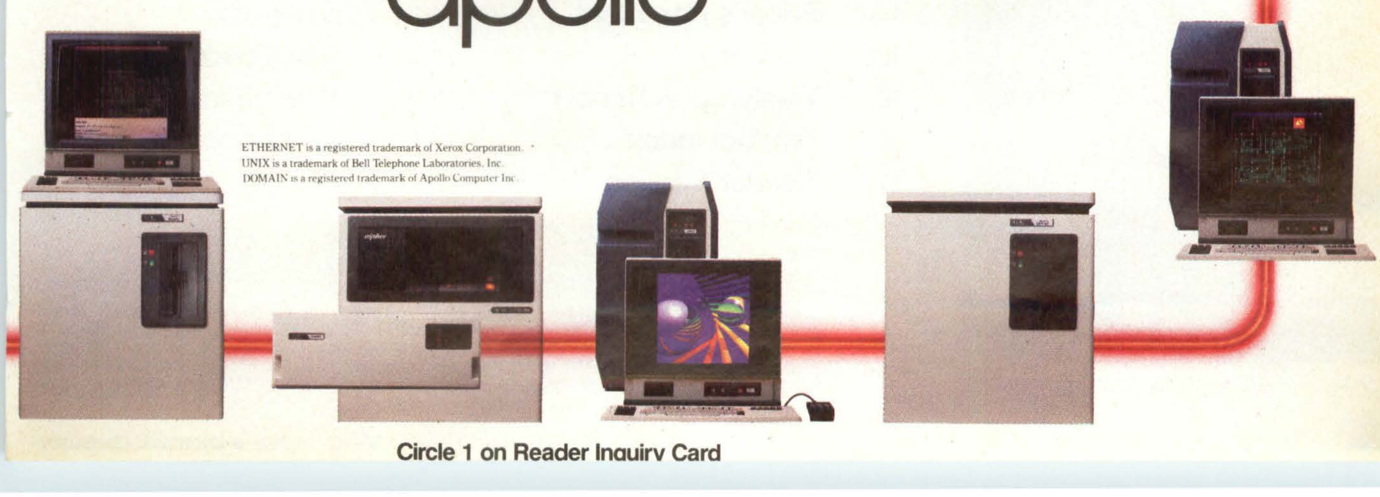

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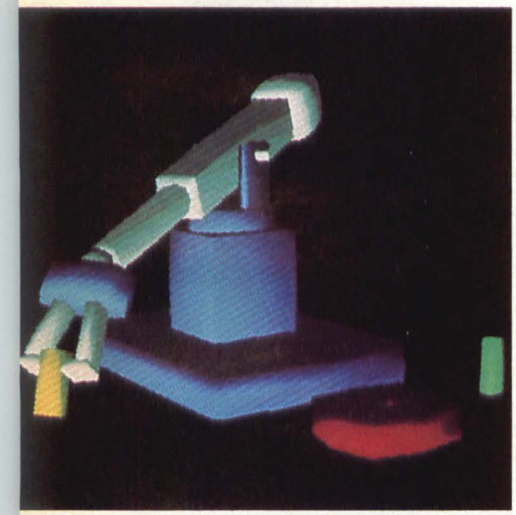

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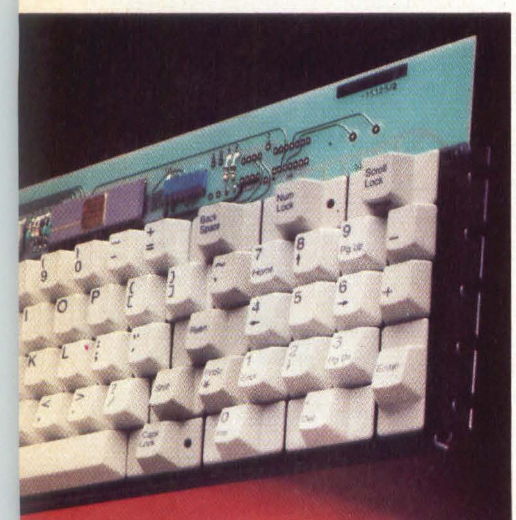

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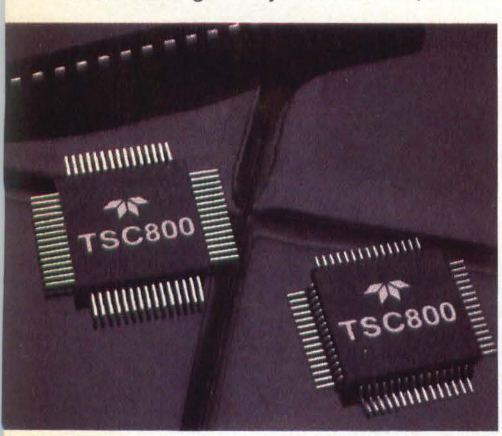

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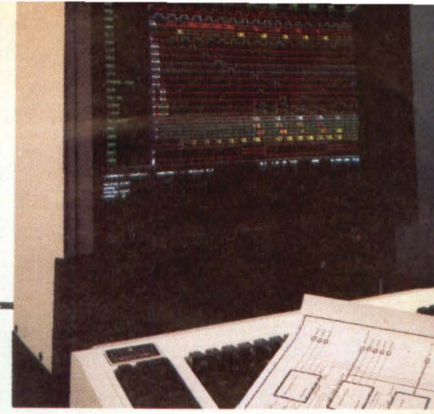

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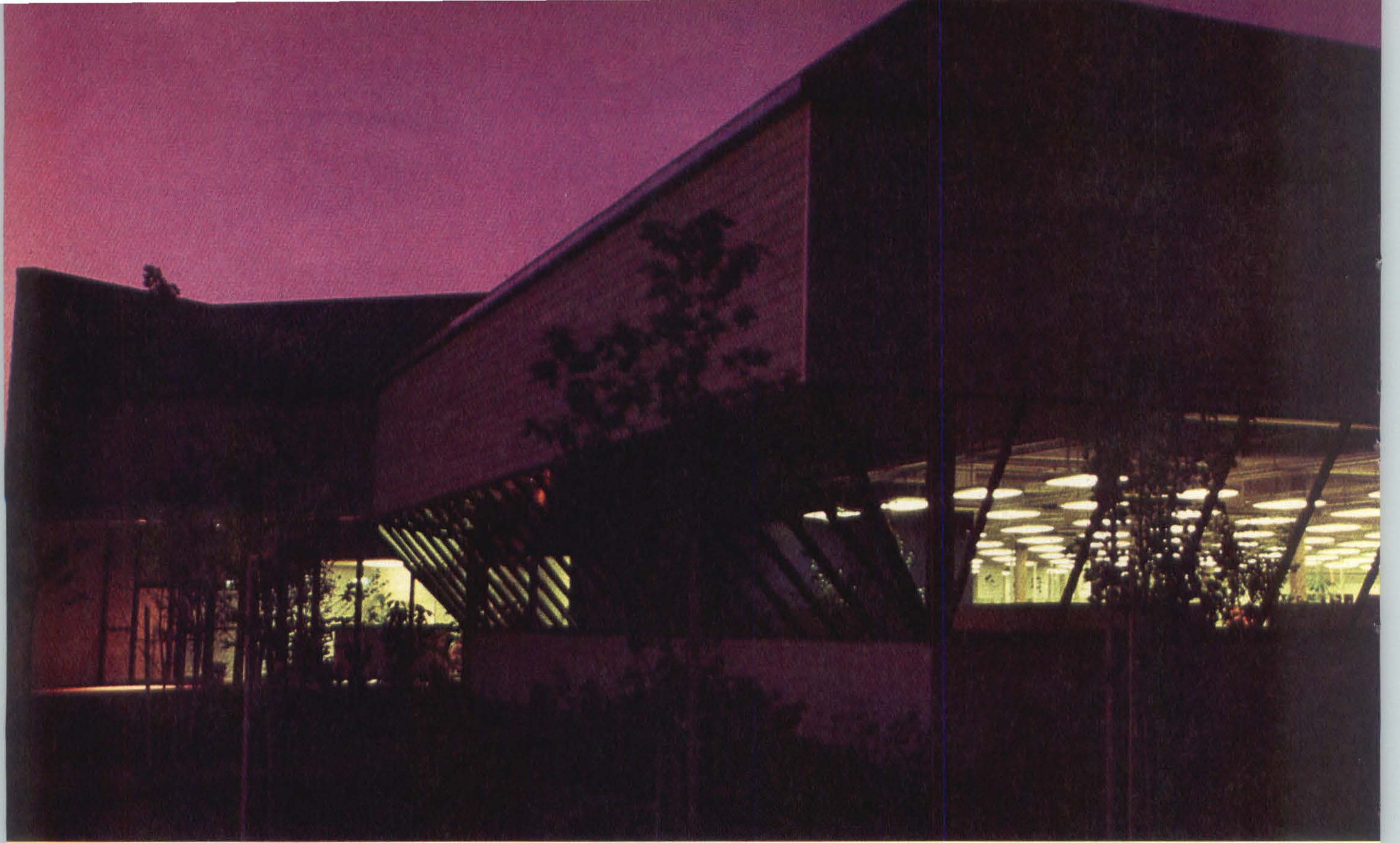

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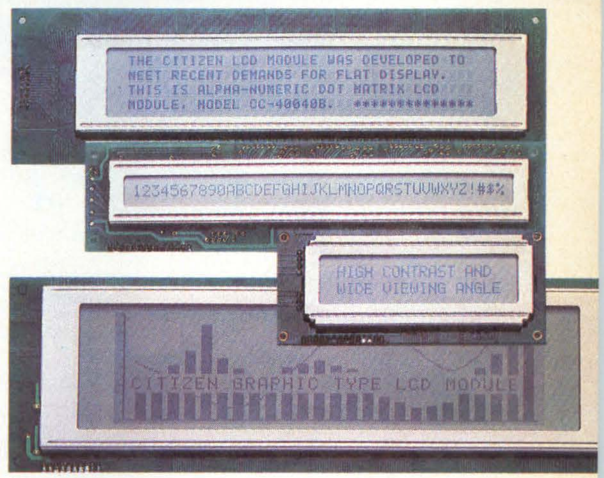

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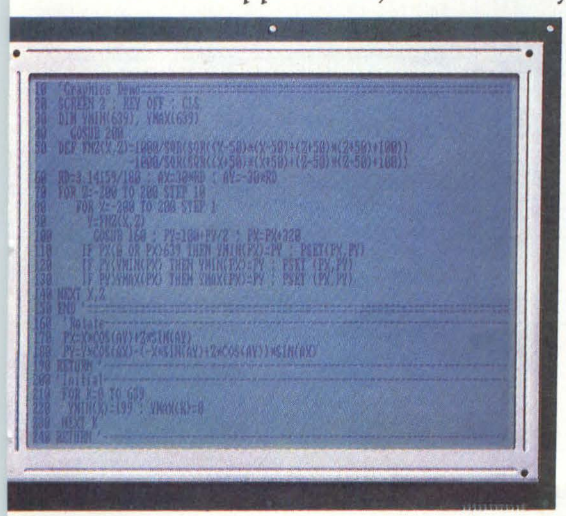

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40 x 2	195 x 50 x 8.85	163.0 x 21.0
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480 x 128	279 x 110 x 10.30	228.0 x 74.0
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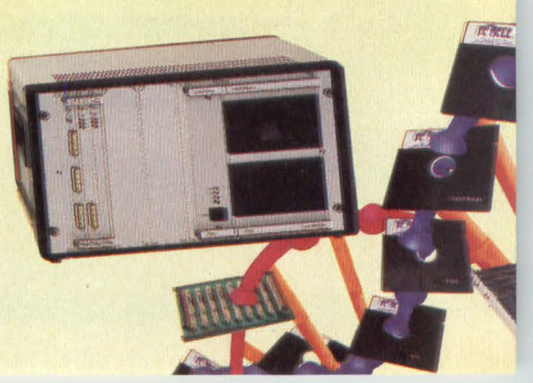


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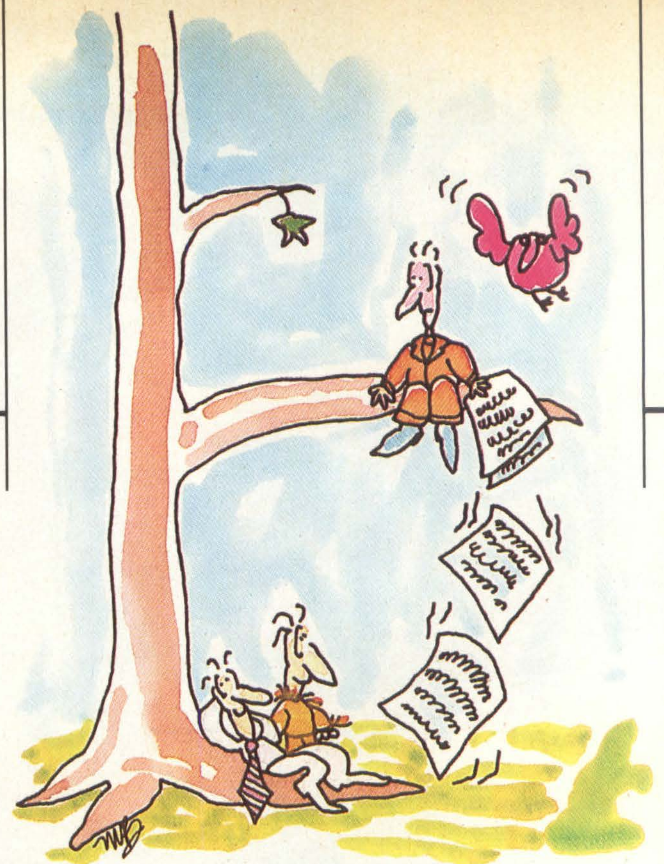
Let's Get Drugs Out Of The Classroom Or How We Got To Be Number One



EDITOR'S COMMENT

Despite the headline I haven't, as yet, defected to the gonzo school of trade journalism espoused by certain West Coast practitioners. It is just that being new to this editor in chief business, I've been perusing the work of my associates on other magazines for tips on editorial writing. In this rather tedious process I've discovered that most editorials can be classified by the two broad categories represented in the headline.

"Let's get drugs, etc." refers to the editorial that sets up some straw man that no sane person could possibly support and proceeds to demolish it with righteousness. This exercise makes the editor feel good because he has come out foursquare against drugs in schools, for democratic principles or against wage slavery for engineers. Furthermore, he hasn't offended anyone except, perhaps, a few drug dealers who probably don't advertise anyway. Thus, "Let's get drugs, etc." is the perfect editorial for editors who wish to appear forceful but don't really want to gore anyone's favorite ox. Braver souls might try to get drugs out of Silicon Valley, and the especially foolhardy could make a big thing about drugs in the publisher's office. But most of us courageous editors are perfectly content to rail against the obvious. I am no braver than my counterparts on other magazines but I promise not to write this kind of editorial – simply because it's boring and obvious.

That other type of essay, "How we got to be, etc.," is an even more common disorder of editorial writers. Gentlemen and ladies of the pen who would normally squirm if forced to promote themselves too blatantly, nonetheless, exhibit no such false modesty about their marvelous editorial product. Thus, we are treated to delightful essays on awards the magazine has won, why it has the most pages, why it reaches the right people and serves them best, why it wins readership studies, and so on. On occasion such articles may help explain the magazine to the reader. Done too often, these editorials appear transparently self-serving. Worse than that, they bore the reader. So I won't do that unless, of course, I become so overwhelmed with self-congratulation that I just have to share it with the readers. But I'll try not to bend my self-imposed rule.

From time to time there are editorials in the trade press that address genuine issues of interest to engineers. These can be technical, political or professional. They are recognizable by their strength of conviction, even if the idea or causes they present are unpopular, wrong or just idiosyncratic. This is the kind of essay favored by most editors if they have sufficient time to think about such things. Of course, such editorials are harder to come up with than the formulaic approaches mentioned.

However, there is some danger, that in straining too hard for conviction, one may come across as merely quirky and cranky. A recent editorial in a competing magazine lambasted Lee Iacocca (my nomination for a Hero of Capitalism medal), Who's Who and the Japanese car of the editor's wife. Thus, an editorial writer, who I normally admire, fell into this trap, creating yet another subclass of editorial: "The paranoids are after me." Nonetheless, such aberrant editorial material is still more interesting than the usual pap most of us editors dish up because it springs from genuine conviction, no matter how weird.

A successful editorial describes or generates controversy and thus involves the readers. Editors know this even if they don't always practice it, or so it seems, because they often generate controversy in oblique ways. One such ploy is to support (or denounce) something that the IEEE has done. This will almost always result in a letter from Irwin Feerst who disagrees (or agrees) with the editorial. The editor can appear balanced in his judgement while Feerst puts in writing what the editor may really think. It's the best of both worlds. Controversy is generated but the editor continues to appear reasonable.

I don't know Feerst, but I have read many of his letters and agree with much of what he has to say. Nevertheless, baiting Irwin Feerst is an overworked editorial ploy that I promise not to indulge in – or have I already done so?

By now I have thoroughly painted myself into the corner for all future editorials: no straw men, blatant self-congratulation, paranoia or getting Irwin Feerst excited. I may never be able to write another editorial without violating my own guidelines. At the very least I will have to be clever in my transgressions. So, don't let me get away with anything. It keeps me straight.

John Bond, Editor In Chief

UPDATE

Custom Chip Set To Implement Token-Passing Network

Gould AMI Semiconductors and Concord Data Systems are jointly developing a three-chip set that will implement the IEEE-802.4 standard. The chip set consists of a data chip with baseband or broadband modem interface, a direct memory access (DMA) interface and protocol controller chip linked via a private bus. The chips utilize a double-metal CMOS process implemented in VLSI to reduce part count and board space.

Hitachi Develops 32-Bit, 5 MIPS CMOS Microprocessor

Hitachi, Ltd. has developed a CMOS 32-bit microprocessor test chip with full 32-bit address and data structures. The test chip is fabricated in 1.3-micron CMOS, 2-layer metal process technology, contains over 300,000 transistors and executes at five million instructions per second.

Digital Research Software For NEC Microprocessors

Digital Research Japan is adapting CP/M, CP/M-86, Concurrent DOS and other system software for use on the initial microprocessors of NEC Corp.'s V-Series, the V20 and V30. NEC will provide the necessary microprocessor information for Digital Research Japan to complete the project by mid-1985.

Automation Control Graphic Systems

Industrial Data Terminals is providing high-end graphics terminals and systems to General Electric Co. for use with the GE series six programmable controller line. The graphic systems coupled with the controllers produce industrial control systems for factory automation. The system will be marketed by GE.

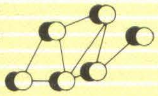
CMOS EPROM Technology

WaferScale Integration, Inc. (WSI) will supply Sharp Corp. with its proprietary 2-micron CMOS EPROM technology. Sharp will use the patented technology to manufacture high density, high performance 64K and 256K CMOS EPROM products. In return, WSI will obtain product manufacturing capacity for the CMOS EPROM products marketed by WSI and an undisclosed sum of money in royalties. Sharp expects to reach full production of EPROM and products in the second half of 1985.

Ada Compiler Development

Sperry Corp. and Intermetrics Inc. are developing an Ada programming language processor for use with Sperry Series 1100 large scale computers. Intermetrics will develop the Sperry 1100 Ada Compiler System (1100 ACS) and expects it to be validated by the Ada Validation Facility of the US Department of Defense's Ada Joint Program Office.

Excelan Licenses Ethernet Front-End Processor



Excelan, Inc. has set up a licensing program for its Exos 200 Core Module Ethernet front-end processor. The generic hardware bus and software interface of the Core Module will enable computer builders to design networking into their new systems as well as allow simplified networking of their installed systems. Excelan provides design assistance, and the deliverables include CAD support circuit layout film, firmware object code and two prototype Exos 200 boards.

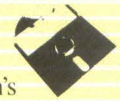
Intel Sells System 2000

Intel Corp. sold part of its Austin operation to SAS Institute Inc. The agreement gives SAS Institute design information, source code, product rights, and support responsibilities to Intel's System 2000 Data Base Management System, including System 2000, Quest, Plex, and Report Writer. Intel's iDIS Database Information System and the Fast 38xx semiconductor disk systems are not included in the agreement.

DOD Validates Alsys Ada Compiler

The first Ada compiler from Alsys, Inc. was validated under the new version of the US Department of Defense test series. Effective January 1, 1984, the use of Ada was mandated by the DOD for mission critical applications. Alsys expects to offer the Ada compiler by April and produce four additional compilers by the end of 1985.

Brown Disc Expands Floppy Disk Activities



Under an agreement with Brown Disc Manufacturing, Rhone Poulenc, Inc. acquired 73.5% of Brown's total outstanding stock. The transaction includes the purchase of 2,150,000 new shares of common stock and the purchase of all Brown Disc securities currently held by Dysan Corp.

Tektronix Acquires CAE Systems

Tektronix, Inc. and CAE Systems, Inc. have agreed in principle to a corporate acquisition in which CAE Systems will become a wholly owned subsidiary of Tektronix. Under the terms of the proposed transaction, Tektronix will issue common stock valued at $75 million to CAE's shareholders. The proposal is subject to a number of conditions, including the negotiation of a definitive agreement and formal approval by both companies.

React Purchases Zitel Memory Systems

Zitel Corp. is supplying high-speed semiconductor memory systems to React Corp. for use as a disk replacement product geared at improving the performance of Burroughs Corp. computer systems. Using the Zitel memory system in combination with a React proprietary interface, React intends to improve the speed and overall performance of Burroughs' systems.

Teknekron Affiliate Acquires Emulogic

A subsidiary of Teknekron Industries, ROI Consulting, has acquired Emulogic, Inc. and purchased most of its outstanding stock. Called Teknekron Emulogic, the company develops, manufactures, and markets universal microprocessor development systems, in-circuit emulators, and advanced software tools for the design engineer/software developer.

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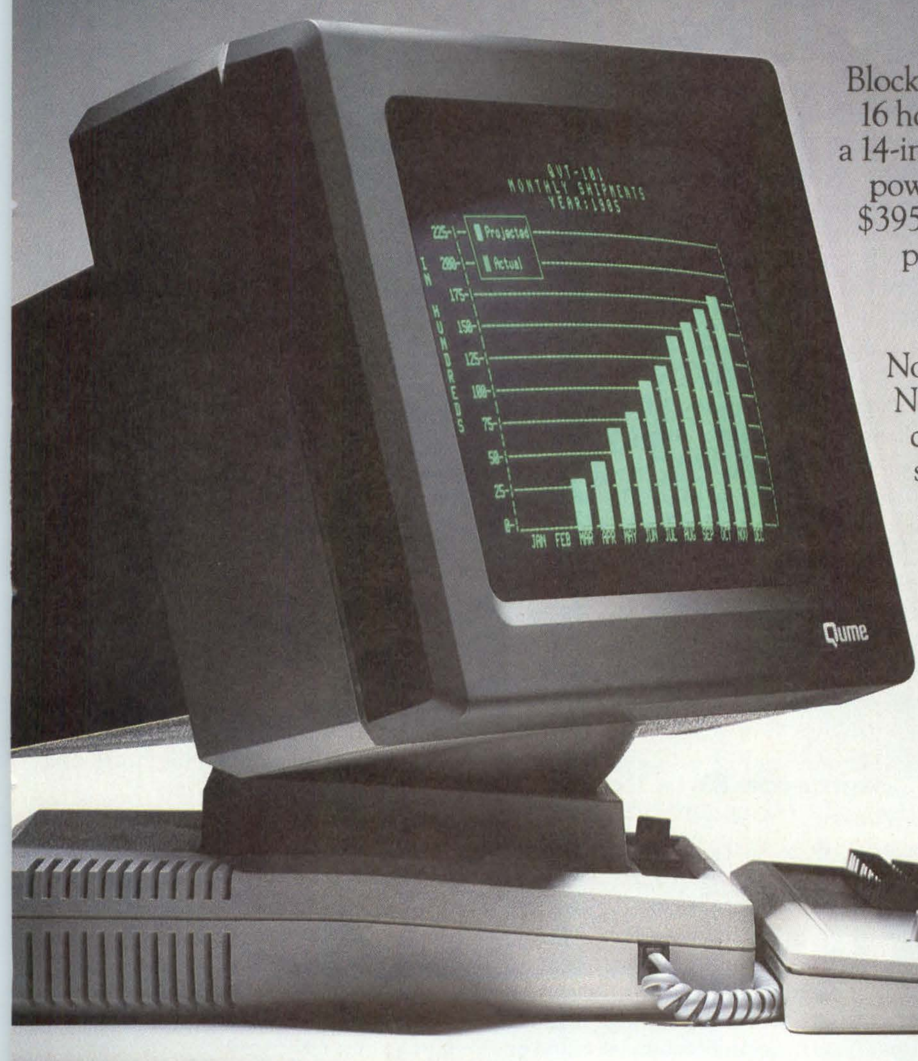

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WASHINGTON REPORT

by Anne A. Armstrong

First IC Masks Registered With Copyright Office

A bright spot for semiconductor manufacturers faced with a depressed market was the passage of the Semiconductor Chip Protection Act at the end of the last session of Congress. Three companies marked the effective date of the new legislation by registering the masks used to manufacture individual chips with the Library of Congress' Copyright Office.

Intel Corp. was the first to formally apply for the 10-year protection when it registered its 256K EPROM chip model 27C256. Quickly following suit, Motorola registered its 68020 32-bit microprocessor, and Harris Corp. applied for protection for its 64K PROM.

The initial registrations were part of a ceremony held at the Copyright Office to celebrate the beginning of a new form of intellectual property protection. Carrying penalties of up to $250,000 for infringement, the new copyright legislation may make possible the development of chips which were economically marginal before, said Congressional sponsors of the bills.

Foreign companies will also be able to register chip masks if their countries offer reciprocal protection to US products. Japan is reportedly considering some similar legislation.

Bell Expands Into Computers And Communications

The regional Bell operating companies have received approval from Judge Harold Greene, who is overseeing the breakup of the monopoly, to expand their businesses into some previously forbidden areas—such as computer sales and equipment leasing, service, overseas selling and real estate. Among the new endeavors which now have approval are the following:

• Bell Atlantic's entrance into computer equipment leasing through its purchase of Tri-Continental Leasing Corp. and into service through its acquisition of Sorbus.

• Nynex, Ameritech US West, and Pacific Telesis' entry into foreign markets to sell telecommunications equipment, computers and software or to set up cellular telephone operations.

• And with some limitations, US West and Pacific Telesis' move into real estate ventures.

Judge Greene's approval of 13 requests for a waiver of the conditions under which the regionals must operate gives the green light to a major expansion of the operating companies presence in the marketplace, according to industry observers.

Federal Electronics Market To Grow 6.75%

The Electronics Industries Association and the Aerospace Industries Association have completed an analysis of the expected spending by the federal government on electronic systems and products during the calendar year 1985. After adjusting for the differing government fiscal year, the associations estimate that in 1985 government spending on electronics will grow 6.75% to $56.3 billion.

The bulk of that figure, of course, is Department of Defense spending, estimated to reach $52.5 billion over the course of the year. EIA officials say in the past, their estimates of DOD spending have been accurate within 3%. Within DOD, the biggest categories of electronics spending are for missiles, the space program and electronic systems and communications.

Telecommunications is expected to be a big gainer this year—funding is up dramatically in both Air Force and Navy budgets. For DOD as a whole, EIA projects a $3 billion increase in fiscal year 1985 and nearly that in fiscal 1986.

The civilian agencies will increase their spending for electronics only slightly – up from $3.5 billion last year to $3.8 billion this year. The biggest gainer on the civilian side will be NASA, whose funding increases $.2 billion to $2.4 billion.

Commerce Lifts Some Export Regulations

Early in the year, the Commerce Department continued its effort to get some kind of new export regulations established. Based on fall meetings of the CoCom group of western allies, Commerce removed controls from many low-end 8-bit microcomputers, but set stringent limitations on military microcomputers and on minis comparable to the DEC VAX series.

Washington watchers of the long running feud between Commerce and the Department of Defense, over who is to establish and review the export of high tech equipment, believe the battle between the two cabinet departments is not over yet. Despite Commerce's action, new export legislation must still be moved through the Congress and many see DOD pressing its case on the Hill.

Regulations and restrictions changed so fast last fall that what was accurate when *Digital Design* went to press, could have completely changed by the time the issue reached readers. With that caveat, we can report that in mid-January Commerce lifted the need for export licenses from 8-bit microcomputers with processing data rates below 2 Mbits per second. Also, all restrictions have been removed from OEM equipment with embedded computers, providing the OEM product does not require any special export licenses and the embedded computer does not exceed established processing rates. In addition, floppy disks and most CRTs are now free to be exported without controls, unless they possess some special features.

Intel Wins Army Micro Contract

When the Navy and the Air Force decided to band together and select a single micro for both services, the Army chose not to participate. Instead, Army officials held a separate selection and bidding process. Officials have just announced they have awarded a contract, expected to be worth some $66 million, to FMS Data Products Co. of McLean, VA for up to 8,500 Intel 86310 and 286310 microcomputers. The firm beat out 16 other manufacturers and distributors.

The contract is open ended – with indefinite quantity and delivery. All Army commands funnel their orders for micros through this one distributor. The pact runs through December 1989. The award marks the first large presence of Intel computers in the government. Zenith Data Systems won both large Navy/Air Force contracts.

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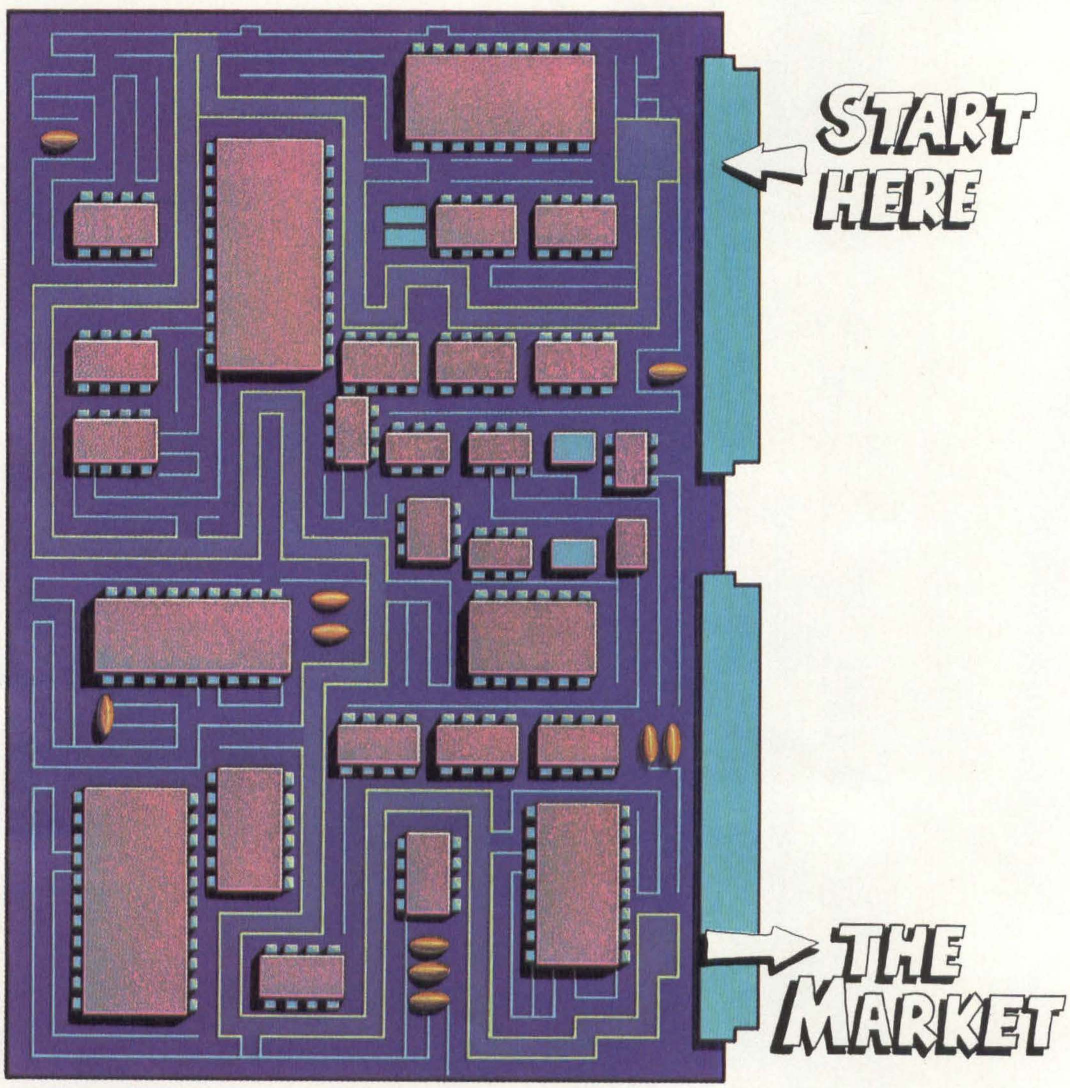

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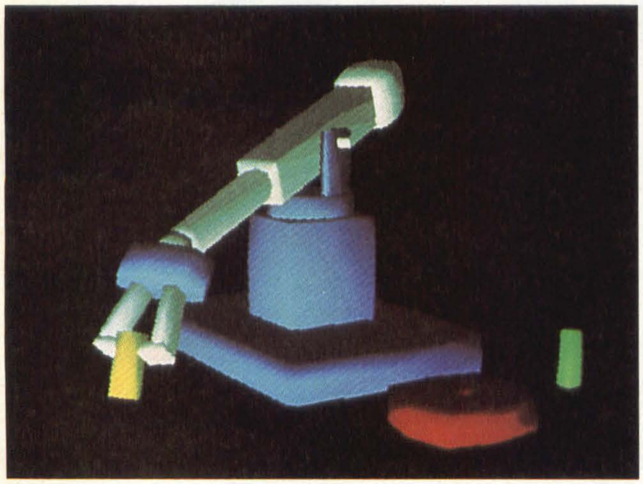
Graphics Processor Performs 3D Calculations



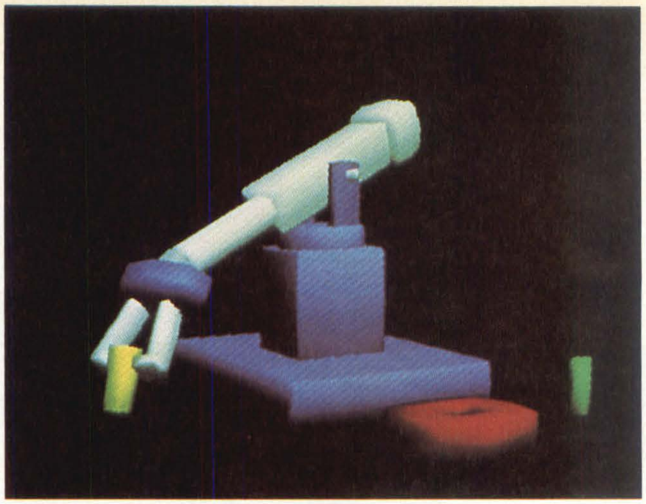


Figure 1: The Model One/380 from Raster Technologies allows the user to specify multiple local light sources and to define both specular and diffuse reflective surface properties for locally stored objects. (Left): Directional light source is coming from below the object from the left. Ambient lighting is present at a low level. (Right): Directional light source coming from above the object from the right. Ambient lighting has been increased to reduce the contrast between light and dark areas.

Raster Technologies has introduced a system, the Model One/380, that performs all the 3D calculations to create a rendered object. All rendering calculations are performed by the graphic display processor. Traditionally, the host had to render an image on each scanline, pixel by pixel. As a result of integrating the display process, local manipulation with realistic shading of complex objects can be displayed with near real-time rates. The Model One/380 software is compatible with the Model One series. The One/ 380 offers a high resolution of 1280×1024×24 bits at 60 Hz, noninterlaced. Available as a deskside tower enclosure, it includes a keyboard, 19" monitor, tablet and mouse. A 4 Mbyte display list memory is optional.

The four major functions associated with 3D modeling are hidden surface removal, shading, light model calculations and 3D coordinate transformations. The One/380 executes these calculations through pipelining and a 32-bit floating-point processor. This allows the host to tesselate complex surfaces into complex patches, specifying color and light sources while the 380 performs the rest of the rendering pipeline. The standard 1 Mbyte local display list contains the graphics database. Up to eight local light sources can be specified. The diffuse and specular reflective properties for objects can also be specified. The light model consists of the base color, the surface characteristics and the number and description of light sources, including ambient light. This is a step beyond local Gouraud shading which is also supported. The shading process may be speeded up for previewing using constant shading, so that polygons are drawn in a constant color.

An additional feature for shading during previewing is the ability to dither an 8-bit deep color. Few colors can create lines of intensity changes but dithering can soften these effects to about 12 bits. This feature is useful when 8 bits are used for color and 16 bits are used for the Z-buffer, in contrast to using the full 24 bit color depth capability of the One/380. After transformation and light modeling, a 16-bit Z-buffer performs hidden surface calculation. The process is further hastened by the ability of the coprocessor to disregard backfaces, if desired. The Z dimension can extend to 65,535 units. The advantage to Z-buffering is that the surfaces do not have to be in any predetermined order, and incremental viewing of objects is possible. The alternative, scanline-based algorithms, creates objects in scanline order so the objects are seen after all calculations are finished.

Software features of the One/380 include the ability to set the refresh rate from 60 to 30 Hz interlaced. This is useful for using low-cost monitors and video hardcopy devices. The One/380 also includes a local debugger common to the Model One series. This allows single stepping through programs, listing defined macros and returning to the program. Program development is further enhanced through the use of an online help facility. Multiple windows which can be placed anywhere on the screen are included. They can have selectable priority with nondestructive overlay.

The hardware of the One/380 is similar to the One/80 and uses the Z8000 as a central processor, 2901 bit-slice processor for graphics output and several gate arrays. The largest gate array has 8000 gates. Unique to the One/380 is the use of Weitek's floating point coprocessor chips to execute the 3D functions. Both the Weitek 1032 and the 1033 are used. The capability of the coprocessor reaches 10 Mflops. Housed in four boards, the standard One/380 consists of a graphics processor board, image memory board, floating processor board and the local display list memory board. Two more slots are available for additional memory.

The primary markets for the One/380 are CAD, geophysical applications such as siesmic display, the automotive industry, simulation and modeling and aeronautical applications. Because of the ability of the One/380 to display wire frame objects in real time, render 3D objects with realistic shading and display objects with full 24 bit color depth, new applications will undoubtedly appear.

–MacNicol

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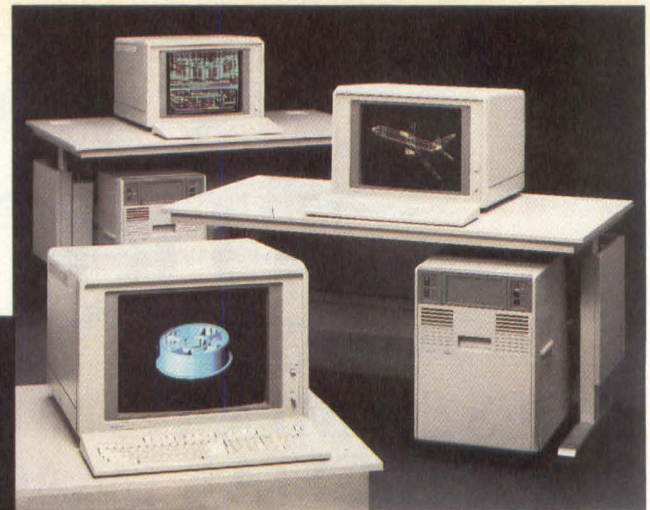
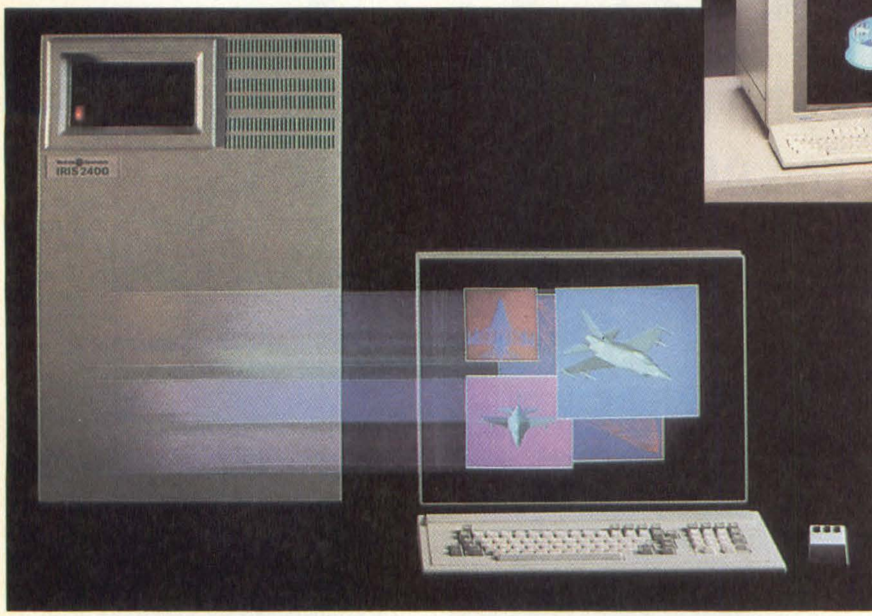
Graphics Workstations Compete For Top Performance



Above: The Tektronix 4125 color graphics workstation and the 4128 and 4129 3D graphics workstations feature a dynamically converged in-line display; 80286/80287 processor; up to 800K of display list RAM; 32 bit coordinates; up to 8-bit planes, and a highly interactive keyboard supporting a joystick and mouse.



Left: All four models of the Iris Series offer 1024 × 768 resolution, a 60 Hz noninterlaced display and a 16-bit Z-buffer.

A new family of graphics workstations from Silicon Graphics (Mountain View, CA) may be the pacesetter for 1985. Designated the Iris Series 2000, this line of systems boasts 3D interactive graphics performance 100 times greater than its nearest competitor. The Iris family is composed of four workstations: models 2000, 2200, 2400 and 2500. All are 68010 based (10 MHz), run under UNIX, are equipped with an Ethernet interface (optional on the 2000) and use the XNS and TCP/IP protocol. According to Silicon Graphics, the systems' high performance is due to their multiplicity of full-custom ICs which enable a high level of parallelism.

The heart of the workstation's design rests in the Geometry Engine which consists of four 32-bit floating point ALUs and a microcoded control store. All Iris systems incorporate a pipelined array of 10 or 12 Geometry Engines with each engine responsible for one of three graphics operations (**Figure 1**). Four-by-four matrix transformations are performed by the first four Engines (e.g., rotation, translation and scaling). The next four to six clip the object in two or three dimensions; and the last two Engines perform a perspective division and map the 3D coordinates to screen space.

Assisting the Geometry Engine, the Geometry Accelerator provides FIFO buffering and floating point conversion (**Figure 2**). Buffering is necessary because the CPU, Geometry Pipeline and frame buffer controller generate data at different rates. The Geometry Accelerator also converts the user's data to the Geometry Engine floating point format. After undergoing Geometry Engine processing, the data is converted back to the user's format. Silicon Graphics claims that executing this conversion in hardware results in a tenfold speed increase of light-source shading and hidden surface removal.

Transformed and clipped data leaving the pipeline is primarily a set of commands in absolute screen coordinates. With these coordinates, the raster subsystem updates the image memory and refreshes the display. The raster subsystem consists of three basic sections: the frame buffer controller, the update controller and the display controller. Bresenham coefficients for rendering lines and polygons are computed by the frame buffer controller which is a 16-bit 2903 bit-slice processor with 4K of writable control store. Resulting images are placed in the frame buffer by the update controller which also does the scan conversion. The display controller refreshes the display using one of three display modes: single-buffer, double-buffer and red-green-blue (RGB). In single buffer mode, all bit-planes are divided into halves, and one half is viewed while the other is modified. When the modified frame is complete, the halves are exchanged and the new frame appears. In both instances, a color map specifies the red, green and blue intensity values.

Gouraud shading, depth cueing and 16-bit Z-buffer operation are other features of the Iris 2000. Depth cueing enhances 3D wireframe drawings by modulating the intensities of the lines and points that comprise the drawing. Consequently, images closer to the viewer are brighter than those further away. Depth cued vectors are drawn at a rate of 1.5 million to 3.0 million pixels per second. Another feature is an interactive 3D Window Manager that allows users to work on several designs simultaneously and run multiple 3D application programs.

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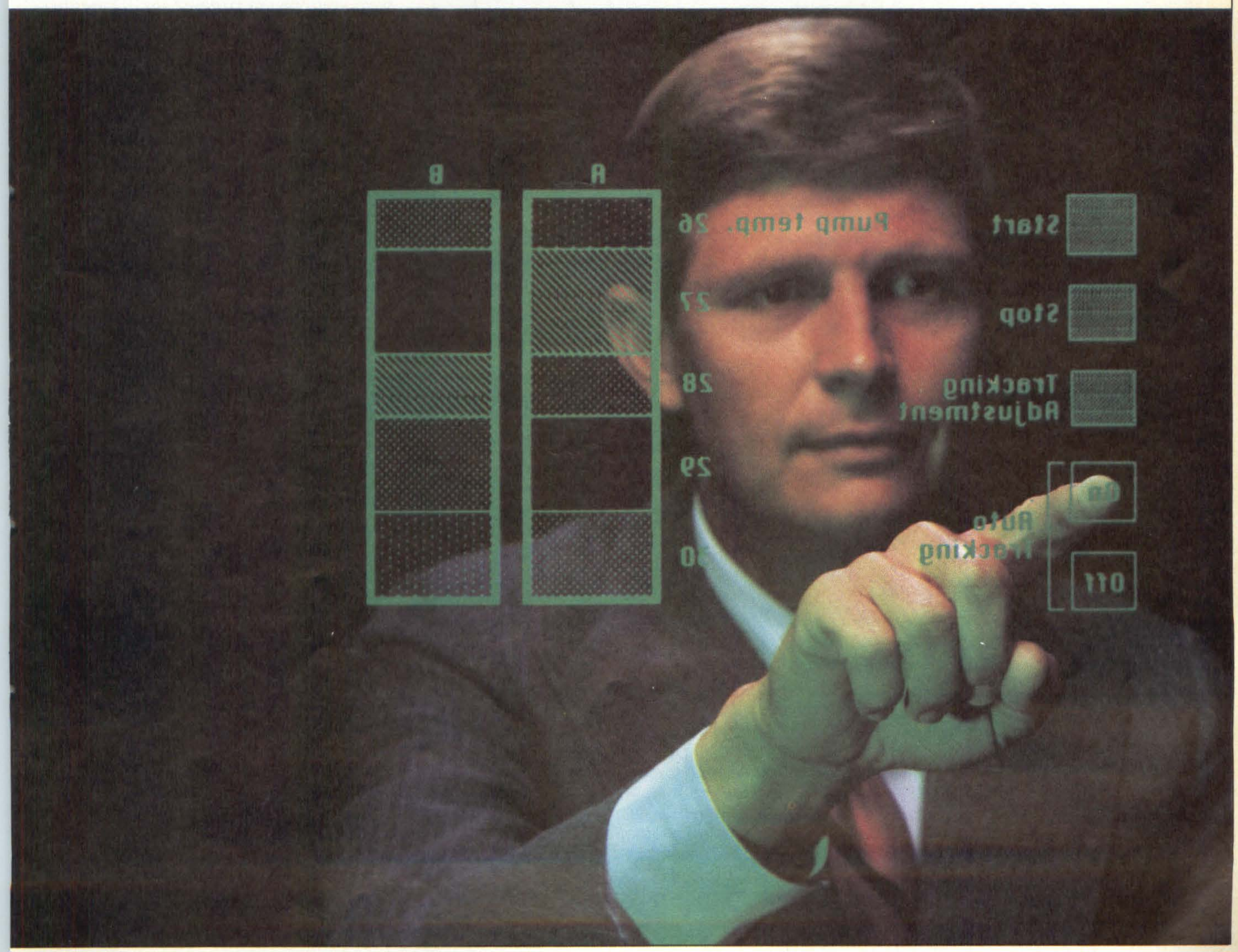

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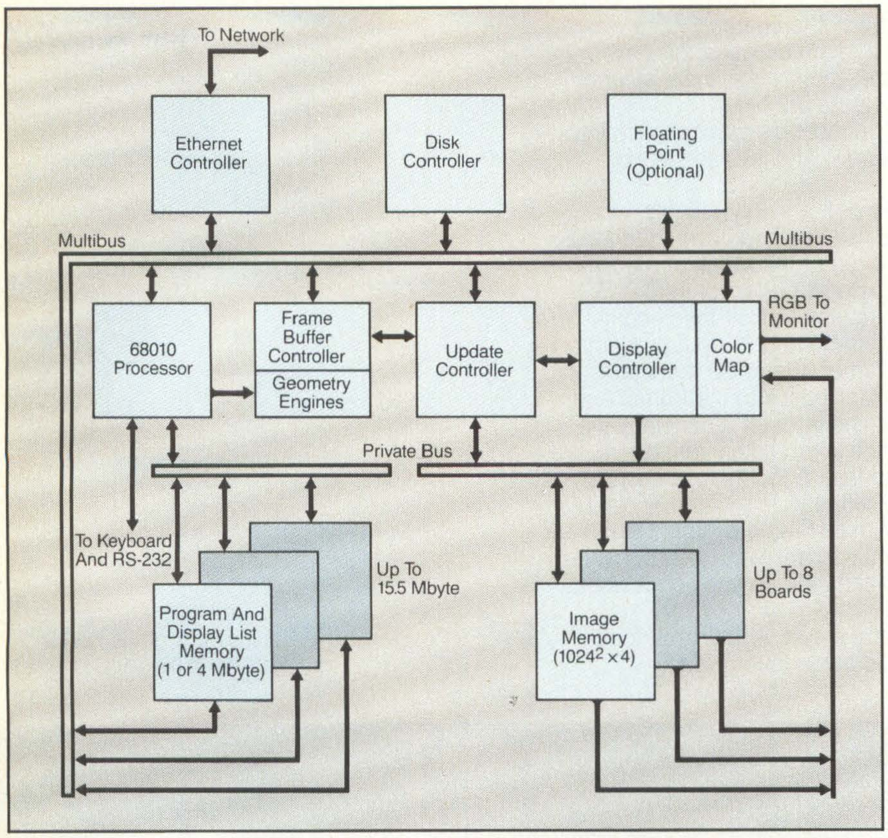

Figure 1: The Iris architecture is made up of three pipelined components: the central processing system, the Geometry Pipeline and the raster subsystem. The three sections communicate over the private bus while disk and network communication occurs over the system Multibus.

been recognized as a key parameter in workstation performance, IBM recently measured response time as a function of output productivity. The results of the study show that a one second decline in response time results in a quadrupling of hourly engineering output.

Silicon Graphics is not alone in the race for graphics supremacy. Tektronix (Beaverton, OR) is offering a major upgrade to their present line of graphics workstations. Intended for CAD applications in mechanical engineering, electrical engineering, cartography and analysis, the 4120 series of workstations is compatible with Tektronix's line of graphics products. Each of the three models – 4125, 4128 and 4129 – feature 2D, 3D wireframe and 3D solid shading capabilities respectively. The 80286/80287-based systems offer 1280×1024 pixel resolution for display on a 19" dynamically converged display at a refresh rate of 60 Hz, noninterlaced. A delta gun, utilizing autoconvergence, is available and each unit is upwardly compatible.

The 4125 basic workstation has firmware for segment editing, fast draw and panel fill, local zoom and pan, 2D image transformation and segment subroutine commands. This last feature is particularly useful for referencing a segment as part of another segment, such as using the function for local storage of repeated elements typical of integrated circuit design, schematic capture and mapping. This saves both memory and editing time. The 2D transformation capability allows drawing of 50,000 vectors per second at maximum resolution. A 4125 supports up to 64 scrollable windows on screen simultaneously and pop-up menus that can be saved and recalled from local memory. Coordinate space is 32 bits deep.

The 4125 hardware includes 288K of memory, expandable to 800K. Two-bit planes are standard, and it can be upgraded to eight. The keyboard has eight dedicated function keys, a numeric keypad and ports for a mouse and a joystick. A wireframe treadmill is optional.

Both 4128 and 4129 color graphics workstations are targeted for 3D applications, but also provide all the 2D capabilities of the 4125. They offer a 24-bit integer space for complex polygons where 2D and 3D information can be displayed simultaneously while executing local pan, zoom and rotation of 3D objects. Data types such as triangle lists, quadrilateral lists and quadrilateral meshes are supported for creating planar polygon definitions. Both units provide the ability to perform local 3D segment matrix transforms, in addition to parallel or perspective viewing through the use of a single

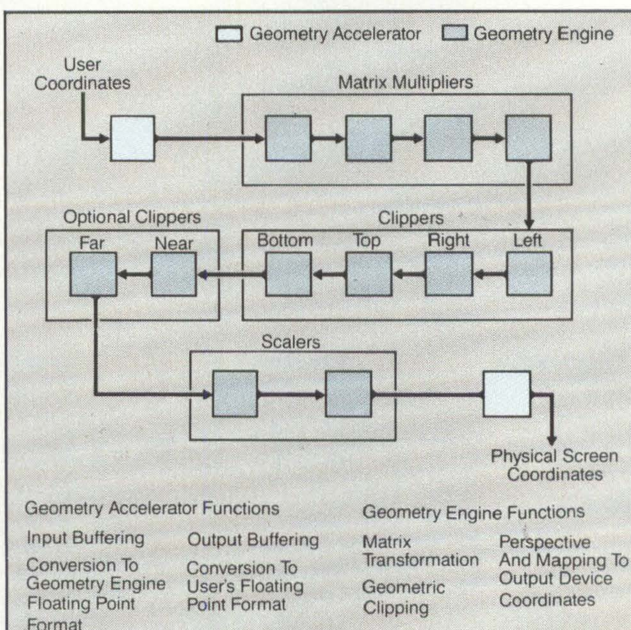

Figure 2: The Geometry Pipeline comprises the Geometry Engine and Accelerator which are VLSI full-custom ICs. By using multiple Geometry Accelerators, the Iris manipulates geometric data, with clipping and perspective division, at an effective rate of 65,000 transformations per second.

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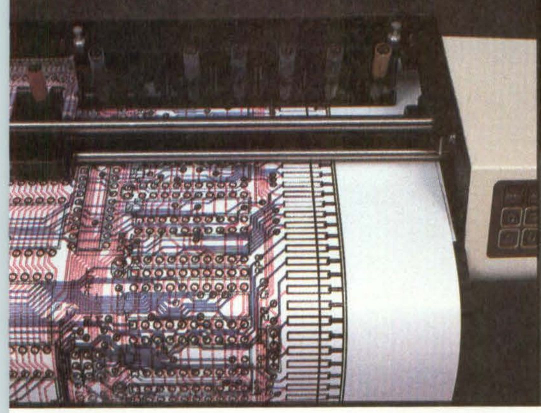

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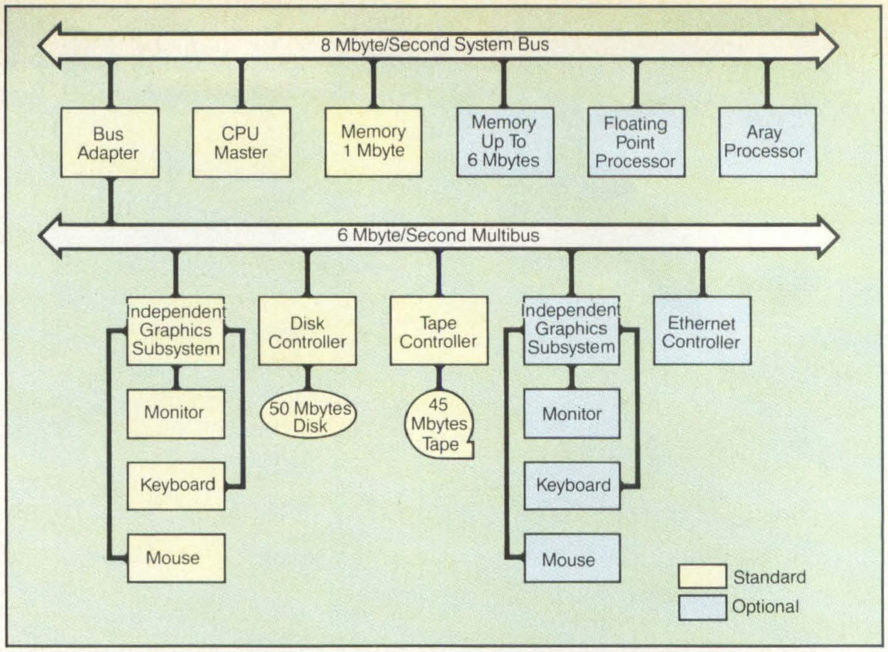

Figure 3: The architecture of Harris HS-10 and HS-20 workstations is built around the 68010 and 68000 processors. Graphics is handled by a third processor, a 68000, running at 12 MHz.

keystroke. Multiple views can be displayed and manipulated by the thumbwheels on the keyboard. Users can also control the depth clipping for front or back, eliminating unnecessary visual information.

One difference between the 4129 and the 4128 is the number of bit planes: four for the 4128 and eight for the 4129. Hidden line and surface removal is provided from the 4129's display list. The 4129 also includes enhancements for shading 3D surfaces. Shading can be either constant, cosine or Gouraud. Constant shading, where an object has the same color intensity across its surface, is useful for high speed display and previewing. Cosine shading provides a more realistic lighting effect with a local light source. Gouraud shading, the slowest method, provides the most realistic lighting where up to 16 local light sources may be used. Colors used to shade a surface are defined in a contiguous shade of indexes that represent a range of intensities. The illusion of a larger map equaling 1024 colors is allowed by 4×4 dithering. It also allows better smoothing and less "banding" to surfaces.

Harris' Computer Systems Division (Ft. Lauderdale, FL) has also jumped into the workstation arena with two UNIX-based systems: the HS-10 and HS-20. Both utilize a dual processor architecture (68000 and 68010) running at 10 MHz. A block diagram of the systems' configuration is shown in **Figure 3**. A dual bus architecture enables primary system modules to communicate via the 8 Mbyte per second system bus, while peripherals connect through a 6 Mbyte per second Multibus. Multitasking is aided through the use of 24 sets of 32-bit double precision registers. Moreover, performance can be raised by adding an optional floating point processor which operates in parallel with the CPU. Similarly, an optional array processor can be directly tied onto the system bus to further increase speed. An Ethernet interface is also a standard feature.

—Collett, MacNicol

Tektronix .... **Circle 234**
Silicon Graphics .... **Circle 238**
Harris .... **Circle 239**

DEPARTMENTS/Communications

Low-Cost 1200 bps Modem Modules Interface Directly To UART, Phone Jack

Users are demanding expanded communications capability from systems; and integral modems for low-speed transmission serve that need in many products. Though ICs are available for modem signal processing, extensive auxiliary circuitry may be needed to provide even a 300 bps line. Modules are available from several sources that include more functions and eliminate most external circuitry. Two new Bell 212A products from Cermetek (Sunnyvale, CA) ease interface and make costs of 1200 bps capability more attractive.

Cermetek introduced the CH1770 to be the first 212A-compatible (1200/300/110 bps) modem component that OEMs can purchase for under $100. For large arrays of modems or security-sensitive applications, the newer CH1763 module's third port allows communications control and monitoring without disturbing the data. Both are complete modems to be mounted on a PC board.

The basic 1770 is 8" square (2.54"×3.74" ×.75") and comprises auto dial/auto answer, tone or pulse dialing, auto-speed and auto-parity adjustment, and diagnostics in addition to the signal processing. With these components and FCC approval of the telephone line interface (DAA), communication can be a standard design feature by interfacing to a UART and a standard RJ11C telephone jack (**Figure 1**).

The larger 15" square CH1763 includes


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a third, parallel, port to connect to the host and an intelligent command interpreter, so the host can reconfigure connections to the modem or to an array of modems. Over the 8-bit parallel bus to the modem DTE, a host can scan several lines without separate UARTs and extra circuitry for each. In situations where security over telephone lines is in question, the host can disconnect the line and, after verifying the password, re-dial a call for transmission. Auditing, diagnostics and status reporting, features common on larger standalone modems, are also possible with this module.

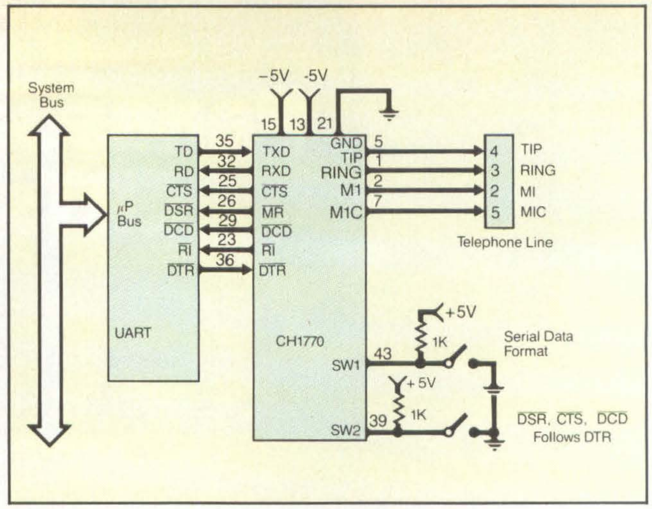


Figure 1: An integral 212A modem requires only a UART and standard modular telephone jack in addition to the CH1770.

Cermetek is not the only company offering 1200 bps modem modules. Rockwell (Newport Beach, CA) also has a 212A product; and TI (Dallas, TX) offers a 28-pin DIP for 1200 bps modem signal processing. Neither includes the DAA, which needs FCC approval. Several other IC manufacturers are expected to introduce 1200 bps products this year, but meantime companies like National Semiconductor (Santa Clara, CA) are introducing complete 300 baud modules with DAA.

The advantages of integrating modems into terminals, home computers and instruments are even greater as 1200 bps products become available. Eliminating a set of RS-232 drivers/receivers and hardware and the external power supply can be significant in such cost-sensitive systems. Firmware in the modules also lessens the demands communication puts on software.

Advances in LSI are allowing higher speeds, more features and lower prices with increasingly smaller footprint modems. Though the single-chip modem is ideal, integrating auto-dialing and DAA functions into a monolithic IC may be over a year in coming. Until then, complete PC board mounted modem modules will lead in ease of modem interface and design. *—Pingry*

Circle 237

Floating Point Chip Outperforms Competitors

The MC68881 floating point coprocessor (FPCP) from Motorola calculates basic math functions twice as fast as any other single chip math processor. According to Motorola, a 16.67 MHz version of the MC68881 will perform an add or a subtract in 2.76 μsec while a 12.5 MHz version of the chip will take 3.68 μsec. This compares to 7.5 μsec for National Semiconductor's 10 MHz NS32081 floating point processor. Intel's i80287 5 MHz chip requires 17 μsec per add.

The long-awaited Motorola chip does floating point calculations in accordance with the latest draft of the IEEE floating point specification (P754 Draft 10.0). In addition, the MC68881 can perform transcendental and other functions. Such operations include trigonometric, exponential, hyperbolic and logarithmic functions as well as root values. All functions are calculated in hardware to 80 bits of precision.

Although the FPCP is primarily intended to operate as a closely coupled coprocessor with the 32-bit MC68020, it can also operate as a memory-mapped peripheral with other 68000 family processors. Consequently, floating point functions can be added to the reduced bus MC68008, the 16/32-bit MC68000, the virtual memory 68010 and the expanded virtual MC68012.

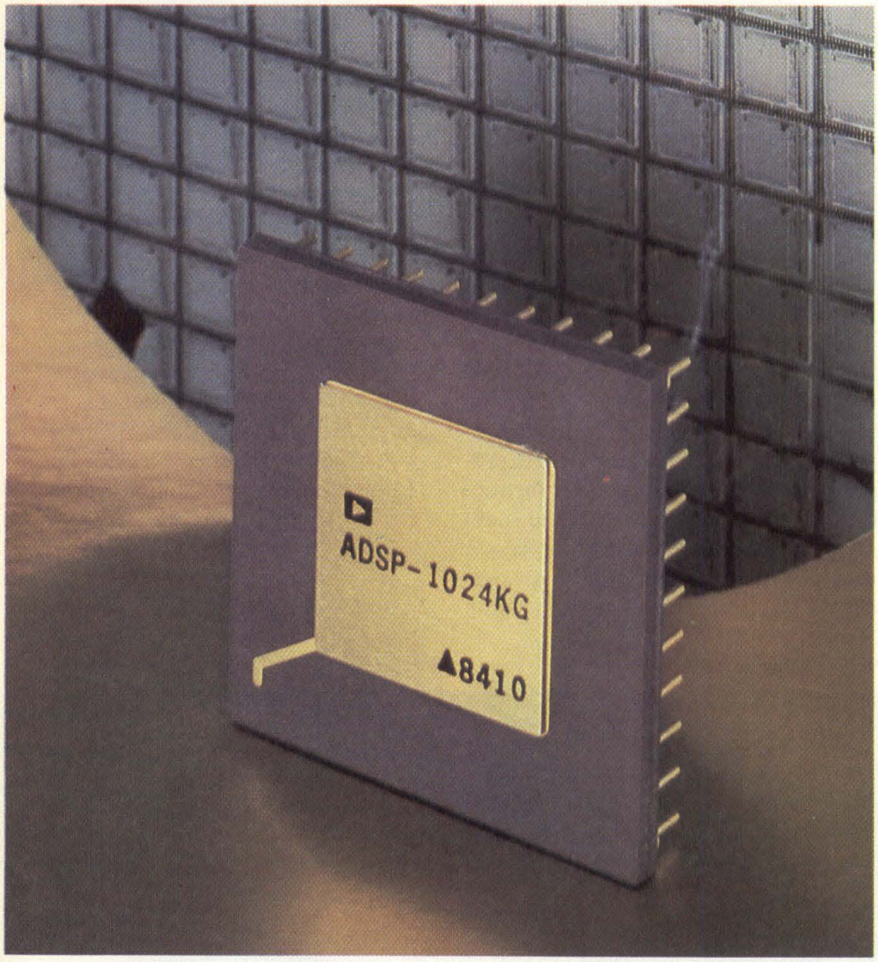
In MC68020-based systems, MPU and FPCP communicate via the MPU's coprocessor interface with the 68020 passing instructions to the 68881. The coprocessor interface is transparent to programmers because coprocessor instructions are written as part of the main instruction stream. Since the coprocessor runs concurrently with the main processor, the instructions are executed in the coprocessor while the CPU is free for other tasks. For present 68000 family processors, other than the 68020, instruction sequences must emulate the protocol of the coprocessor interface. However, future 68000 family processors will use the coprocessor interface.

The MC68881 includes a 67-bit arithmetic unit, a barrel shifter and eight 80-bit general-purpose registers. The 2-micron HCMOS process used for the chip permits 155,000 transistors on a chip measuring 270 × 330 mils. Power dissipation of the 68-lead pin grid array is less than 1 W. Standard clock frequencies are 12.5 MHz and 16.67 MHz. Samples will be available this month for $375 each. Limited quantity production is expected for July.

–Bond

Circle 233

24×24 CMOS Multiplier— An Industry First



Analog Devices' (Norwood, MA) parallel array CMOS multiplier, the ADSP-1024, packaged in an 84-pin grid array, bridges the gap between resolution and cost. Processing operands at a 5-MHz rate, the 24-bit multiplier is specified (worst case) with multiplication time of 195 nsec (commercial grade) and power dissipation of 200 mW. It features two input ports and one output port. By multiplexing the Most Significant Product (MSP) and the Least Significant Product (LSP) through the output port in a single cycle, it achieves a full 48-bit product without sacrificing throughput.

Additional features on the ADSP-1024 include the ability to shift the output for format compatibility with the external system, status flags for normalized product and overflow and rounding capabilities on one of three different bits. Such capabilities enable the device to be configured with external adders to perform 32-bit floating point multiplication with a 24-bit mantissa and an 8-bit exponent.

David Birkner, Vice President of Engineering at array processor manufacturer Computer Design & Applications Inc., believes the Analog Devices part may make its presence felt mainly in the development of floating point multipliers. Systems architects not wanting to implement single chip IEEE format floating point multipliers in their designs will be able to build floating point multipliers in other formats, such as DEC or IBM.

According to Louis Schirm IV, President of DSP Systems Corp., the ADSP-1024 offers impressive specs and a sensible design. The architecture of the multiplier is such that the device will be fairly easy to use since neither the MSP nor LSP are multiplexed with the input ports. He predicts the 24-bit multiplier will be of definite use for systems architects working in specialized applications of digital signal processing (DSP) such as digital audio and seismic exploration and array processor development.

Designers of high accuracy DSP systems are often faced with the problem of choosing between lower resolution and more expensive multipliers. Unacceptable levels of digital noise, caused by either insufficient coefficient accuracy or the maintenance of too few bits, may require the systems architect to search for higher precision multipliers in order to perform digital filtering and fast Fourier transforms (FFTs).

Performing double-precision operations with several parallel 16-bit multipliers reduces the throughput of the device in addition to raising the cost. Although floating point multipliers provide greater dynamic range, they do so by increasing system complexity and cost. The latency period for such multipliers is longer, sometimes up to 900 nsec. In addition, some DSP applications may not require a full 32-bit floating point for precision. Analog Devices intends to give systems architects more design options by offering the 24×24-bit CMOS multiplier.

TRW's LSI Products Division (La Jolla, CA) made two attempts to manufacture a 24×24 bit multiplier. The first in 1978 resulted in a bipolar part which was slow, power hungry and difficult to implement. The chip did not proceed past the initial silicon stage.

In 1981 TRW announced another 24-bit multiplier; after preliminary sampling, the part was never manufactured. According to a TRW spokesperson, the MPY-24HJ was abandoned because there was a lack of interest among systems architects. Designers of the TRW bipolar part also had difficulty forcing the multiplier to desired power dissipation specs. Even with the achievement of the 24-bit multiplier at Analog Devices, TRW has no plans to resume development of a similar device within the current calendar year.

—Meng

Circle 232

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STRAIGHTALK

No claims. No boasts. Just straight facts and commitments from Jeffrey Liu, president of Microscience, on our growing family of half-height Winchester disk drives.

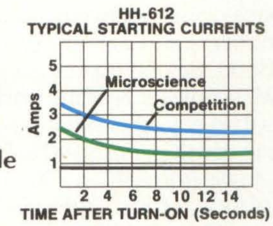
"By introducing the new HH-725 20 MB 5.25" and HH-312 10 MB 3.5" half-height Winchester disk drives to our product line, we now offer the proven quality and performance most OEMs need in volume today.

"Combined with our HH-612 10 MB 5.25" half-height disk drive, Microscience now provides a product family of superior quality and better performance than any other drives available.

"Time after time, we have proven that Microscience has the performance, quality, and price personal and portable computer manufacturers demand.

"The secret is the way we design and manufacture drives for you.

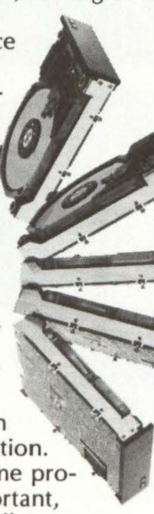
"Microscience disk drives have extremely low voltage requirements because small business and portable computers don't have the luxury of excess power or cooling capacity.



"We've used procedures and components that will be power misers, yet they still provide long-term performance and reliability.

"Our drives feature a thermally isolated stepper motor for precise head alignment and optimum seek performance. A proprietary linear actuator assembly was employed to ensure data reliability and provide greater drive durability.

"A buffered seek mode and highly accurate proprietary microprocessor-controlled closed-loop servo positioning system keeps the head precisely on track. This maintains data integrity through a wide range of operating conditions regardless of thermal expansion, system hysteresis, or long-term wear.



"Microscience drives are not limited to functioning horizontally. Because of the growing use of portable computers and increasingly compact packaging, we designed our Winchester drives so you can use them in almost any position.

"While volume production is important, what you're really concerned about is the quality of product you use in your system or application. We have made a major commitment to manufacturing and quality programs.

"Microscience test equipment and tooling have been carefully selected to meet our exacting standards.

ZD

"This ensures Microscience ships only zero defect half-height Winchester product that does not eat away at your profits . . . and your reputation.

"There's a lot more I could say about the Microscience half-height Winchester disk drive family. But what will convince you is using a Microscience drive in your application.

"For more straightalk regarding your half-height Winchester needs, call or write us today."

Jeffrey Z. Liu

President,
Microscience
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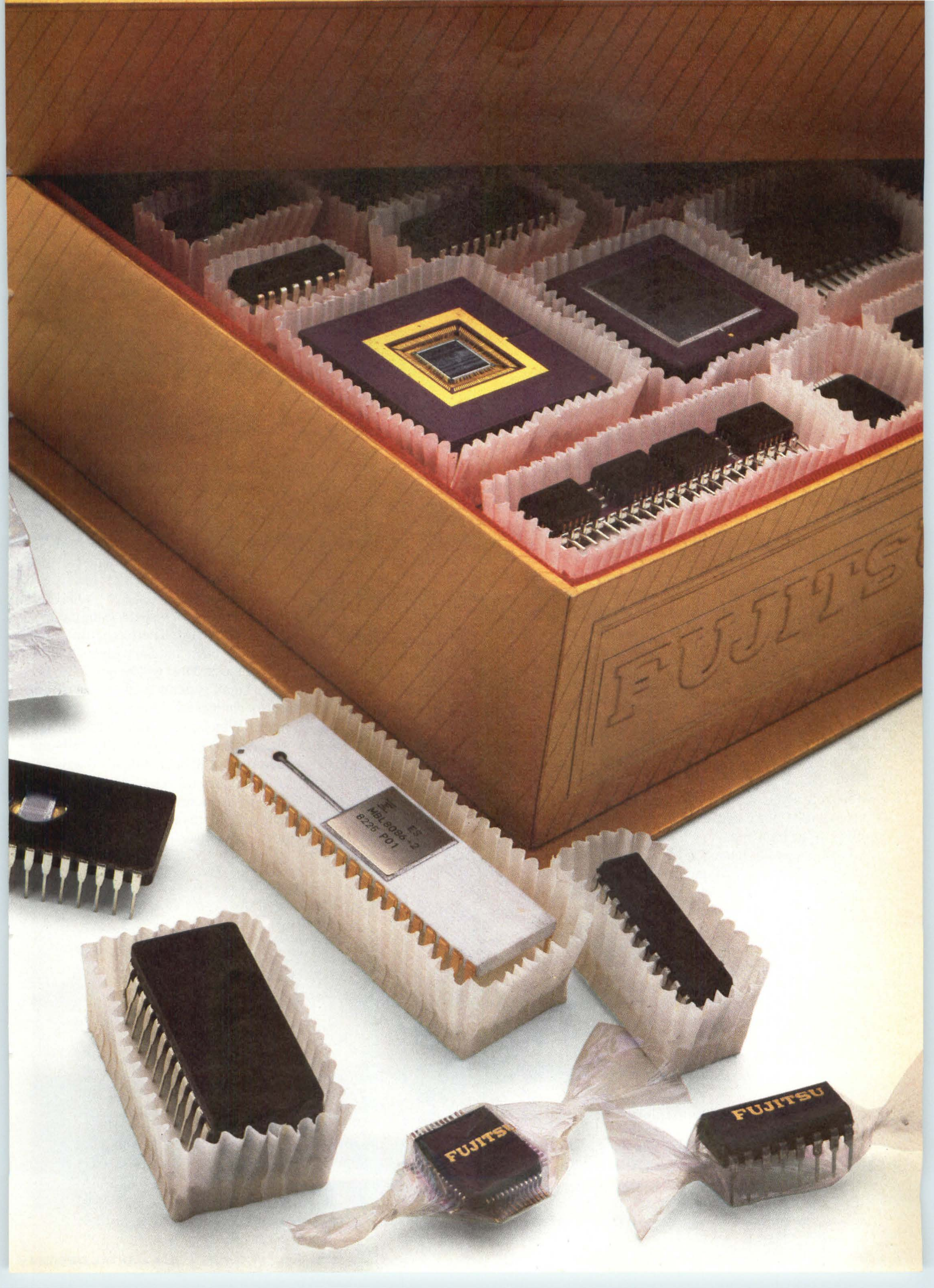
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Micro Winchesters Slowly Penetrate Small System Designs

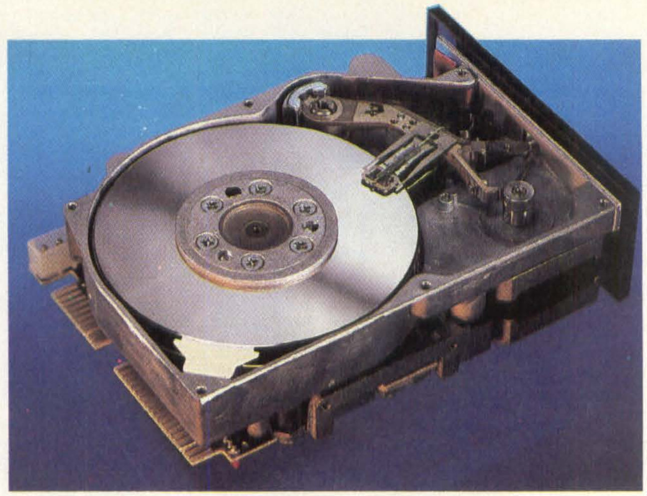

Figure 1: Though systems with micro Winchesters will just be appearing this year, Rodime has been shipping 3½" rigid disk drives for over a year.

Disk drives have been getting smaller for years, and the generation of portable and desktop systems now being designed provide further impetus for this trend. Though most products using sub-4" micro Winchesters won't be announced for some time, at least two companies are manufacturing the small drives now.

Shipping 10 Mbyte drives for over a year now, Rodime (Boca Raton, FL) claims to have over 100,000 units in the field. They admit competition is finally heating up, but find it a potential benefit since integrating a micro Winchester is no longer the risk it was with a single source. Next into the field was Microcomputer Memories Inc. (Van Nuys, CA); both firms now have 20 Mbyte as well as lower capacity drives.

With predictions that 3½" drives will dominate in systems needing 30 Mbytes or less of storage, several companies have announced sub-4" products. Microscience International (Mountain View, CA), Seagate (Scotts Valley, CA), Newbury Data of the UK (with offices in Woburn, MA) and Hewlett-Packard (Palo Alto, CA) announced micro disk drives late in 1984. The products range from 5 to 20 Mbytes formatted; Newbury has introduced a 40 Mbyte unit to establish themselves at the high end.

Though costs to make 3½" drives are similar to those for 5¼" and prices may be higher now, several other advantages result from the size. In addition to space saving, smaller drives' lower mass improves shock and vibration isolation. Forces from 30G to 50G can be tolerated when the drives are not operating without destroying data; this allows them to be transported when already recorded. This feature may allow use of micro Winchesters as an exchangable drive. Removing the mass storage from a system especially aids data security.

Smaller drives also consume and dissipate less power. These units require +5V or +12V at 0.3A to 0.8A (except the Newbury unit, which requires +12V at 2.0A) and dissipate only from 9W to 15W. Good thermal qualities are the result of less mass to spin coupled with the CMOS surface-mount electronics.

These heat characteristics permit high track and bit densities without over-extending recording technology. For extra insurance, many use a closed-loop servo for positioning. Even with the servo bits taking space, 3½" drives now pack an average of 10 Mbytes per platter or 5 Mbytes per surface, formatted. Metal disk media is used in most of the 10 and 20 Mbyte products for high density recording.

Although Winchesters can be internal to the system, adherence to the microfloppy form factor could aid product design. In this area, SyQuest (Fremont, CA), making 3.9" fixed/removable drives since before the microfloppy 3½" standard was firm, falls short, as does Hewlett-Packard, whose drive is higher than the current standard 3½" form factor.

At the other extreme, Rodime and Microcomputer Memories offer frame mounts so the small drives will fit into a 5¼" space. This will not only allow the drives a wider market, but permit shock mounting and isolation. Until enclosures and system mechanical specifications change, this will be an option for integrating drives into systems where weight, power consumption or heat are problems. Since these 3½" products use the standard ST-506/412 interface (HP drives use SCSI or IEEE-488), integration into existing designs is no problem.

The coming year or two should see announcements of systems using the 3½" drive as standard. There is a rumor that IBM and lesser industry giants will be among those. Most will be portables, but other small systems could benefit from the mechanical and thermal qualities of micro Winchesters. In single-user applications, a hard disk is still a high-end feature, and 10 or 20 Mbytes should accommodate most needs. As capacities of 5¼" drives increase, micro Winchesters may gain rapidly for relatively unsophisticated systems.

—Pingry

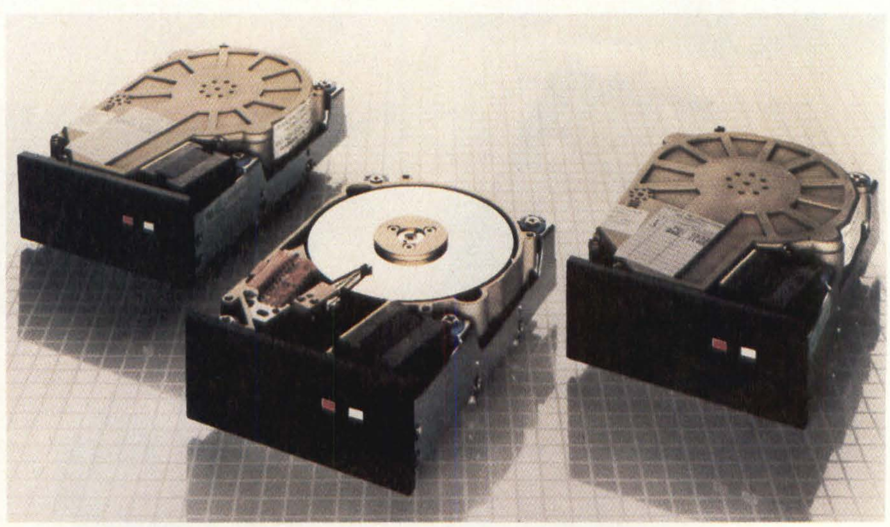

Figure 2: Microscience offers 10 and 20 Mbyte drives to the micro form factor.

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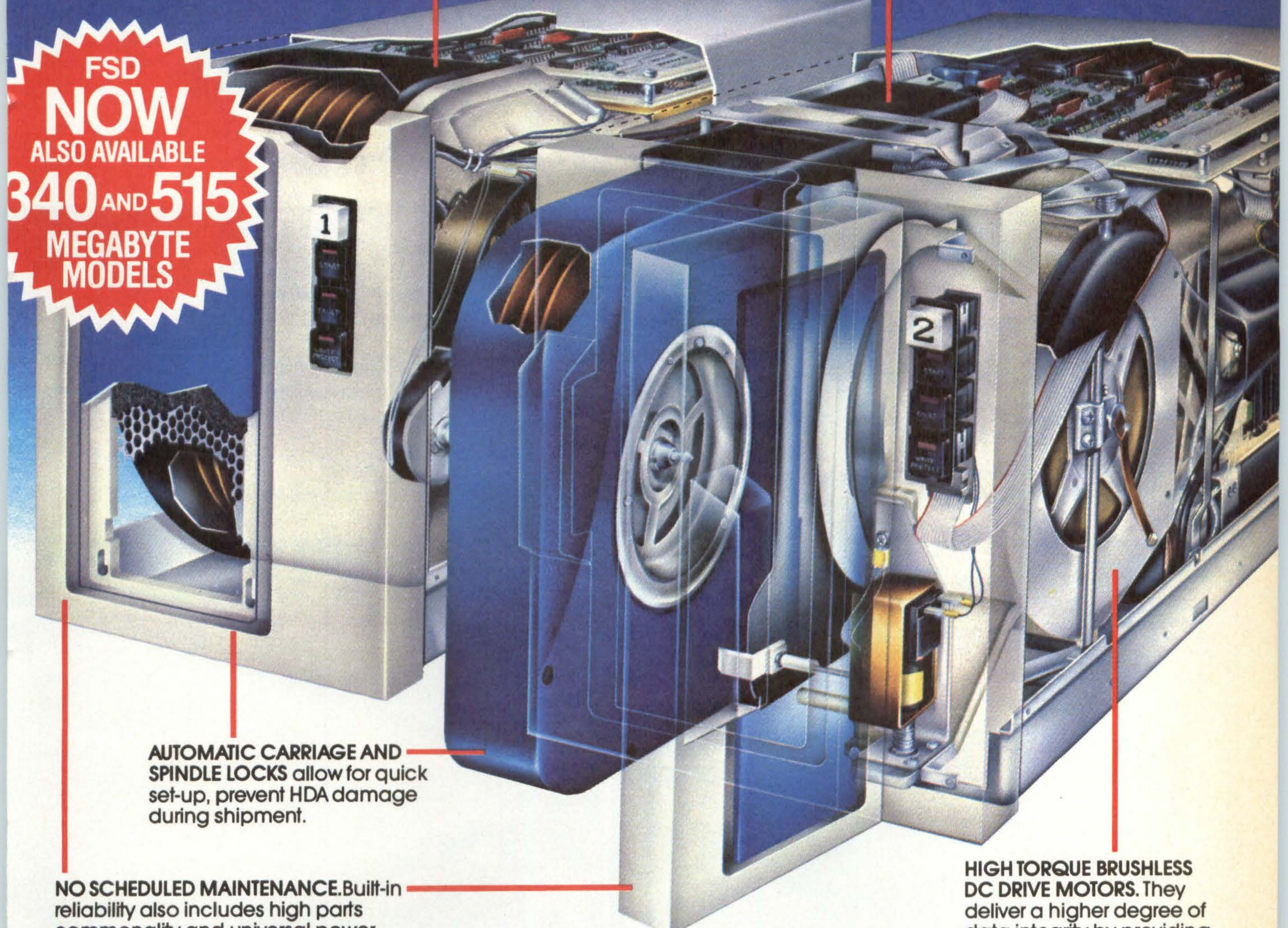

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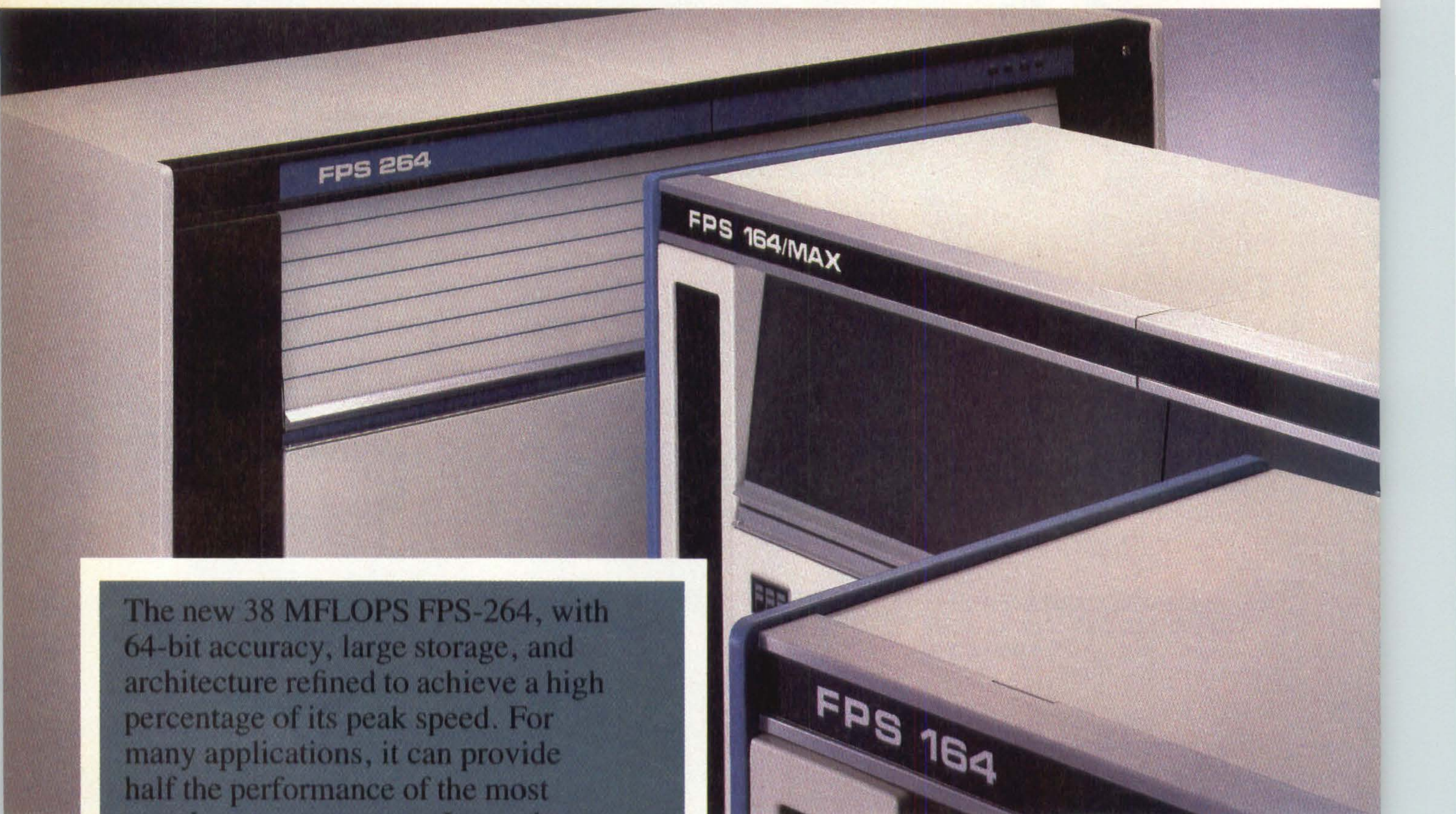

The new 38 MFLOPS FPS-264, with 64-bit accuracy, large storage, and architecture refined to achieve a high percentage of its peak speed. For many applications, it can provide half the performance of the most popular supercomputer. Its moderate price and exceptional support liberates supercomputing from the realm of major corporate investment and puts it within practical reach of departments and teams.

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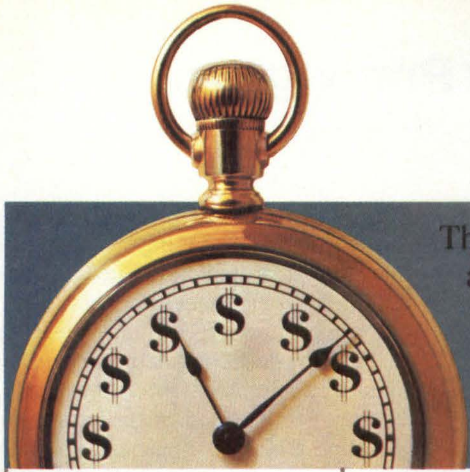

The FPS optimizing FORTRAN-77 Compiler lets you easily adapt code to FPS' pipelined architecture in a form that is nearly as efficient as hand-coded assembly language. With extensions for asynchronous I/O and for enhancing compatibility with other compilers, it is one of most comprehensive tools of its kind.

likely to find that the advantage of immediate, local access is well worth the sacrifice of standing in line for the "fastest" machines.

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Family Specifications

	FPS-264	FPS-164/MAX	FPS-164
Peak speed, MFLOPS	38	33-341	11
Dynamic range	2.8×10^{-309} to $9.0 \times 10^{+307}$	2.8×10^{-309} to $9.0 \times 10^{+307}$	2.8×10^{-309} to $9.0 \times 10^{+307}$
Logic format	64 bits	64 bits	64 bits
Main memory capacity	4.5 MWords	15 MWords	7.25 MWords
Maximum disk storage capacity	16 Gbytes	3 Gbytes	3 Gbytes
Precision	15 decimal digits	15 decimal digits	15 decimal digits
Vector registers	4 x 2K	124 x 2K (max.)	4 x 2K
Scalar registers	64	184 (max.)	64
Host interfaces	IBM, DEC	IBM, DEC, Sperry, Apollo	
Program Development Software	FORTRAN Compiler, Overlay Linker, Assembler, Object Librarian, Interactive Debugger.		

Family Performance Measures

	FPS-264	FPS-164/MAX		FPS-164
		15 accelerators	**1 accelerator**	
Peak MFLOPS	38	341	33	11
Peak MOPS	190	1705	165	55
Peak MIPS (Multi-instruction partcels)	19	5.5	5.5	5.5
Typical MFLOPS, LINPACK Benchmark	9.9	20.0	6.0	2.6
Whetstones (64-bit)	20,100	5800	5800	5800
1000x1000 matrix multiply, seconds	53	10	66	189
$K/MFLOPS (system price/peak speed)	$16.8K	$2.5K	$12.3K	$27.1K

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New Technologies Challenge Laser Printing

With the increasing demand for high speed and high quality hard copy in the electronic data processing environment, nonimpact printing is becoming more popular. The high volume of copy printed in these settings requires sophisticated and reliable printers; 20,000 to 1,000,000 prints per month is typical. In this large volume area, three technologies currently dominate: electrophotography (laser xerographic), magnetography and ion deposition.

In the distributed data processing environment, typical print speed is 35 to 80 pages per minute; printer prices range from $40,000 to $100,000. In the centralized location, 80 or more prints per minute is average with prices starting at $300,000.

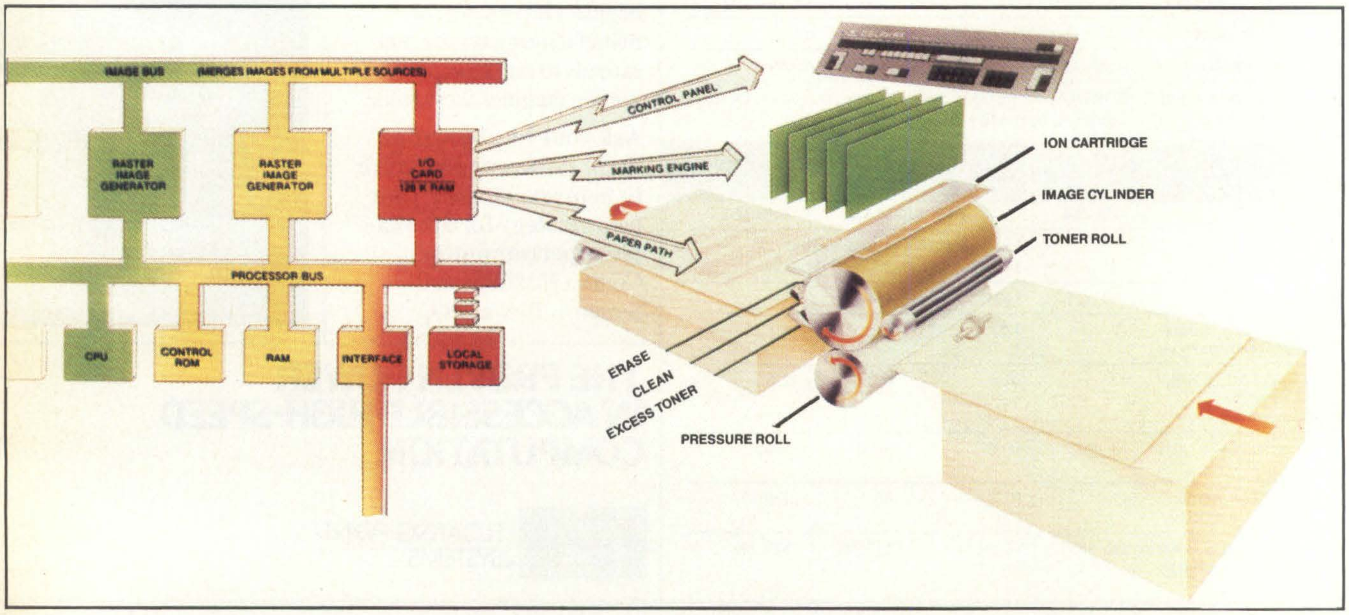
The credibility of nonimpact printing has been enhanced by the commercial success of the laser technology, the first to reach maturity. Electrophotography, first developed for photocopiers, has since become a widely accepted and well-supported printing technology. The process involves a photoconductor drum that receives an electrical charge and is optically exposed to the image. Developed by a toner, the charged latent image is then transferred to the paper.

Electrophotography is unique because it provides direct optical imaging and can print from an electronic video signal. This provides the capability for reproducing standard forms and makes it easier to design a system to operate in the local copy mode. Xerox Corp., (El Segundo, CA) one of the first companies to use the technology, is the major contender in this area. The Xerox 8700 laser xerographic printer produces 10,500 lines per minute and sells for approximately $200,000. Their 9700 printer produces two pages per second (18,000 lines per minute) and is priced at $392,000. These printers are the fastest in their league and, therefore, the most expensive.

The maturity of electrophotography has inhibited the commercial exploitation of magnetic printing, though developments in the technology show its potential to gain an edge in the marketplace. Magnetography is a relatively simple technique using a metal drum, rather than a photoconductor as in laser technology. The less complex drum offers a longer lifetime (10 million page) than a photoconductor. An additional advantage of magnetography is the virtually unlimited lifetime of the magnetic image. When the printing system is properly configured, the magnetic image will retain its quality throughout the toning and transfer process, allowing many copies to be produced. Magnetic printing can also produce high quality pictorial images containing differing shades of gray.

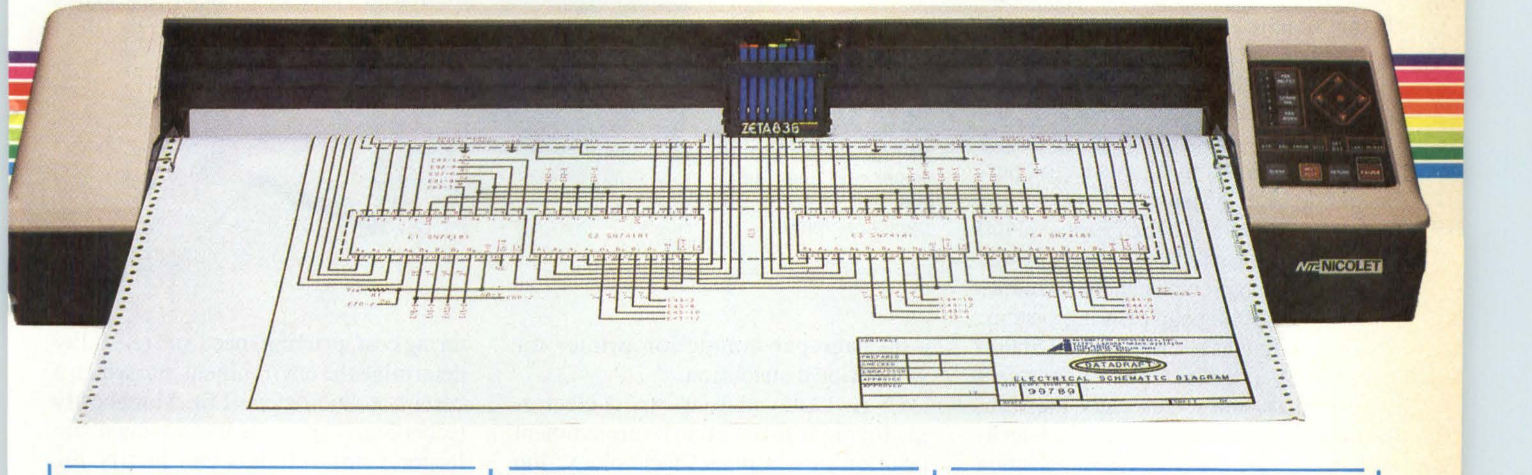
Cynthia Peripheral's (Sunnyvale, CA) MP 6090 magnetic printer produces 6,000 lines per minute and is priced at $60,000. It features fanfold, continuous form paper handling and uses a heat lamp fusing technique (as opposed to pressure roll fusing used in most laser systems) that reduces jam rates significantly. An easily replacable imaging head offers a long lifetime; in a 500,000 to 1,000,000 volume range, the head should last the life of the machine. In most laser printers, when the optics or a laser fail, the entire machine will have to be replaced. Multiple imaging, a major strength in this technology, is available in electrophotographic printers but at some cost and complexity.

Introduced as an alternative to laser and magnetic printing, ion technology was brought to market and patented in 1980 by Delphax Corp. (Westwood, MA). The technology is geared toward large volume operations requiring 100,000 to 1.5 million copies. The unique feature of the ion deposition architecture is the ion print cartridge consisting of a multiplexed matrix of three electrodes which generate, control and focus charged



Delphax's S6000 ion deposition printer produces 60 pages per minute for large volume operations requiring 100,000 to 1.5 million copies per month.

CAD system integrators think our newest plotters were designed just for them.



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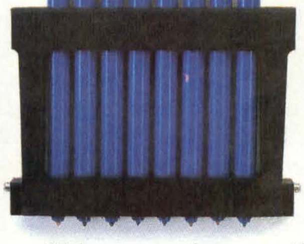

Incredibly, some plotters still grind to a dead stop to change pens.

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Circle 15 on Reader Inquiry Card

Cynthia Peripheral's MP6090 magnetic printer uses fanfold paper and heat lamp fusing, printing 90 pages per minute.

particles. The process includes the cartridge, a toning system that develops the image and a pressure roller that transfers the image to the page. This method of transfixing requires less power and has the advantage of avoiding the warm-up times normally associated with thermal fusing systems. A notable consequence, however, is that pressure fixing can crush the fibers in the paper and produce a shiny surface on the page. In addition, the imaging process is simple and does not require numerous mechanisms to operate, as do laser systems.

Introduced in 1982, the Delphax 2460 print engine spurred the growth of this technology and precipitated the introduction of the S6000 page printing system. Printing 60 pages per minute, the S6000 is not as fast as the Xerox 8700, but offers a 25% cost savings. Currently, there are no other companies involved in ion technology because Delphax's patent position makes it very difficult for firms to explore this area of nonimpact printing. However, in December 1984, Delphax and Xerox announced a joint agreement to develop a 60 page-per-minute ion printer for worldwide distribution.

C. A. Pesko analysts expect electrophotography to maintian its pre-eminent position in nonimpact technology. Ion deposition and magnetography are definitely decisive competitors in this field, but laser has the advantage of having been around for over 20 years. Unit manufacturing cost, printing speed and reliability determine the environment into which a certain technology will fit. More costly technologies appear in those areas where larger print volumes can justify the higher cost. However, speed and reliability determines whether the technology can compete in a high volume environment. *—Lamneck*

DEPARTMENTS/Memory

New Technique Secures System Access

In the past, several methods have been proposed to secure system access, each with its own relative drawbacks involving ease of use, cost and speed. The most common and least expensive method for system security is the software password. One reason for its popularity is the technique's inherent simplicity—a major benefit in systems involving many users. Unfortunately, it is relatively easy to break into, and that is its greatest drawback.

Securing data more cautiously was one of the driving forces behind the development of the Data Encryption Standard (DES) developed by the US Department of Commerce/National Bureau of Standards in 1977. The standard provides protection of computer data via encryption or cryptography. Basically, transmitted data is enciphered before transmission and must be deciphered upon receipt to facilitate a secure communication channel.

The DES encrypts 64 bits of data at a time utilizing a 56-bit key. Although the algorithm is public knowledge, the code is considered unbreakable if the key is not known at the receiving end of a given transmission. The process of multiple encryption or decryption is a way to increase the size of the key to any desired length. For example, the sender may successively encipher, decipher and encipher a block of data using one key for the encipher operations and another for the decipher operation. The receiver would then have to decipher, encipher and decipher the data using the same pair of keys.

Another way to increase security without reducing throughput is to perform the DES algorithm in reverse. Data or keys can be deciphered by the sender and then enciphered by the receiver to yield the original message. Several vendors currently offer products designed to work using the algorithm specified by the DES. These include the WD2001/2 from Western Digital Corp. (Irvine, CA), the MC6859 from Motorola (Austin, TX) and the 8294A from Intel Corp. (Santa Clara, CA).

Any cryptographic implementation using the DES can be broken into four fundamental timing sequences. First, the key is loaded into the device. Second, the data to be encrypted is loaded and the DES is executed. And, third, the result of the DES is unloaded from the device.

An alternative approach recently pro-

DESIGN TECHNOLOGY UPDATE NO. 1 FROM EATON CORPORATION

A practical guide to specifying dot matrix impact printers.

BEGIN AT THE END.

Dot matrix impact printers are very popular today for three simple reasons. They're rugged. They're reliable. And they're reasonably priced.

Still, specifying the right impact printer isn't easy. So we suggest you begin with a few questions targeted to the end-user.

For example, what form of hard copy would be needed? On cards or roll paper? And if paper, how many plies are needed?

And what about characters per line? And pre-printed forms? Is through-put speed or transaction time critical? How important is graphics capability?

TAKE A TEST DRIVE.

Dot matrix impact printers come in all shapes and sizes. But the biggest variable is speed.

In most impact printers, speed is affected by the shape and density of the characters—both of which can be changed. Another key factor is the method of moving paper through the printer.

By compressing the matrix, you can get more characters per line. By using stepper motors rather than solenoids, you can greatly improve paper speed.

As you can see, the possibilities are endless. So take a test drive first.

To assist you, Eaton Printer Products offers a development kit complete with expanded driver board and printer mechanism to help test & evaluate your complete prototype.

FACE-TO-FACE INTERFACE.

A prime factor in specifying a printer is the supplier's willingness to work one-on-one with you.

Rather than costly trial-and-error on your part, Eaton provides the necessary technical advice, either in person or in written form.

And Eaton offers you customized service for your customized design. Because there's nothing standard about your work.

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There are two other important considerations in your design process: product changes and short lead times.

Eaton offers you a direct line to their engineering staff. So as problems, changes, or deadlines develop, your answers are a phone call away.

PROVEN VALUE.

Investigate the track record of both printer and manufacturer. For example, Eaton pioneered dot matrix impact printers . . . earning a reputation as a specialist in today's highly competitive market. And Eaton's 40 column dot matrix printer has a field-proven performance record that has set industry standards. It can be a solid complement to your design, too. It's a high performance printer. It's reliable. And it offers one practical feature that no other printer has . . . it's built in the U.S. and backed by Eaton worldwide.

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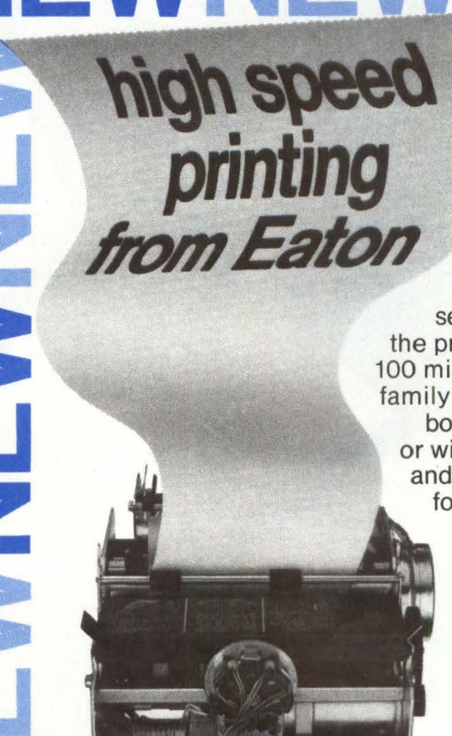

Eaton's new M-4 family of stepper motor printers feeds paper at a brisk 20 lines per second. With a printing speed of 3 lines per second bi-directionally. Plus, the printhead has a rated life of 100 million characters. The M-4 family includes journal printers, both single and split roll, with or without multi-line validation, and slip or document printers for single or multi-ply forms. For M-4 custom applications, just contact Eaton Printer Products, Technical Research Park, Riverton, WY 82501. Phone: 307/856-4821.

EATON

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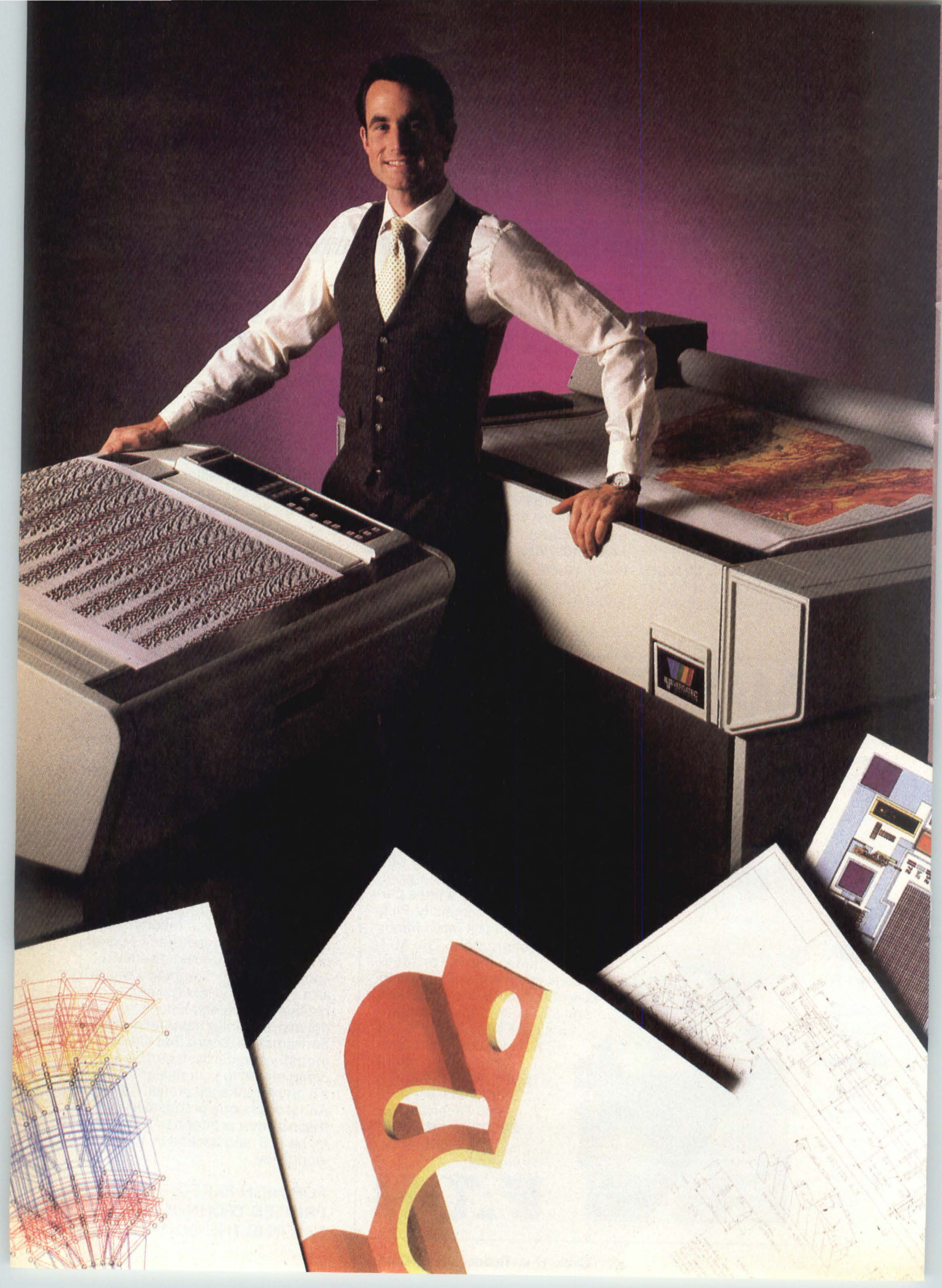

posed by Intel is to provide a data protection mechanism on-board an EPROM memory array. This device, the 27916, known as a KEPROM, is essentially a 27128 memory augmented by peripheral functions, such as random number generator, encryption circuitry, key, lock and control circuitry, that provide the authentication capabilities. Access to a locked 27916 is permitted through an initialization sequence called the authentication handshake. The handshake consists of a series of byte transfers between two KEPROMs. Initially, one 27916 internally generates a random number and passes it to the other device. Both KEPROMs internally encrypt this random number. The two resulting encrypted numbers are then compared within the 27916 now generating a random number. If this second comparison is favorable, both 27916s have been authenticated and their contents may be read by any system user.

All 27916 devices contain the same encryption circuitry which implements a proprietary logical combination of a random number and a KEY. The KEY, a designer-defined 64-bit number that has been programmed into a special portion of the device, is at the core of the authentication capability of the 27916. It is the key that prevents an unauthorized user from gaining access to the memory array. Consequently, for an authentication handshake to be successful, both 27916s involved in the handshake must contain the same key. Since the key is what the ultimate security of the software depends upon, it can never be read and is known only to the system designer or software designer.

In addition to system access security, the KEPROM is a safeguard against firmware copying. For example, if a standard EPROM is substituted for a 27916, the second part of the handshake will prevent it from being used. Because Intel's KEPROM device can be plugged into the same sockets as a standard 128-Kbit EPROM, an OEM can protect its investment in proprietary system code by designing keyed-access EPROMs into the system.

– Wilson

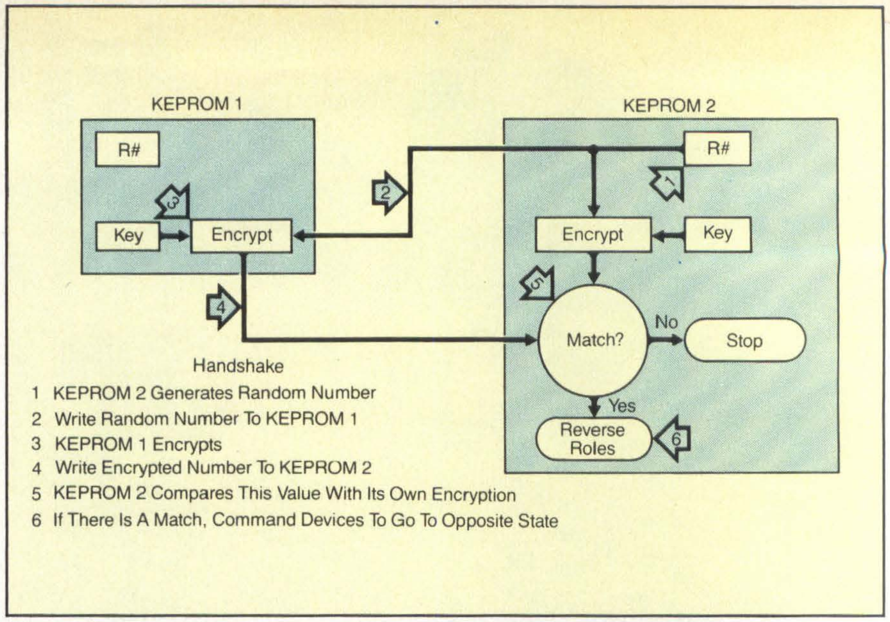

Figure 1: The authentication sequence between the two KEYPROMS.

DEPARTMENTS/Systems

Supercomputers At Supermini Prices

Traditionally, extremely high price tags have limited supercomputers to use in government laboratories, where they are used for very specialized purposes, such as fusion energy research, fluid dynamics studies and atmospheric science. In the past, many large computer manufacturers, including Burroughs and IBM, entered the supercomputer fray, only to withdraw because of what was viewed as a very small market, leaving Cray and Control Data Corp. (CDC) as the only large contenders. Both firms are still active in the market. Cray's latest model, the XMP/48 is a four processor

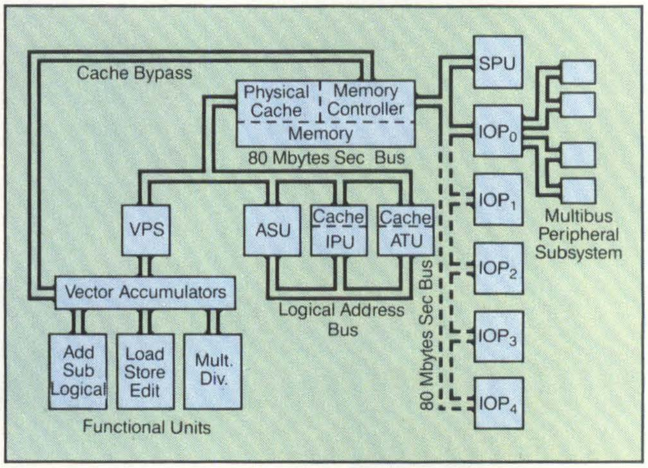

Figure 1: The architecture of the C1 computer resembles that of the Cray.

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■ **Automatic pen settings** always set the correct pen speed and force for the types of pens you're using–so you don't have to worry about these details.

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And Hewlett-Packard's designed-in quality and reliability means plotting performance you can rely on, job after job. So your plotter will always be ready when you are.

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Hewlett-Packard drafting plotters bring you the plotting ease, performance and reliability that have made us leaders in the plotting industry. So when you make the decision to go with Hewlett-Packard, you know you've made the best choice.

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HEWLETT PACKARD

version of the XMP with a peak performance rating from 250 MFLOPs to 1,000 MFLOPs at a price from five million to fourteen million dollars.

Future supercomputer development from CDC will be done by ETA Systems, a 1983 spinoff started by former CDC people. ETA plans to develop an eight-processor system that is compatible with the CDC Cyber 205 software and capable of 10,000 MFLOPs. Its price tag will be $20 million. Three Japanese companies entered the supercomputer market during the past two years. Fujitsu delivered its first system in January 1984. Its single and dual-pipeline VP100 and VP200 offer performances ranging from 250 MFLOPs to 500 MFLOPs. Hitachi's S-810/10 and S-810/20 supercomputers are rated at 315 and 630 MFLOPs and were introduced in December 1983. NEC plans to deliver its SX-1 and SX-2 machines next year. These are rated at peak performances of 650 MFLOPs and 1,300 MFLOPs.

Over the past few months, several firms have introduced products intended to offer the performance of supercomputers at prices currently being paid for superminicomputers. A variety of architectural approaches have emerged in the marketplace. The first implements an architecture similar to Cray's. In effect, this is the approach taken by Convex Computer (Richardson, TX) in its C1 computer. Whereas conventional scalar processors must execute multiple instructions for each single data element, vector processors can execute one instruction for multiple element arrays, vectors and matrixes. The C1 integrates scalar and vector processing into a single processing system (**Figure 1**). Through this architectural design, both scalar and vector processors can function concurrently.

Two compilers are currently available with the system. A C compiler allows the C1 to use UNIX and applications written in C. In addition, a proprietary optimizing and vectorizing Fortran 77 compiler performs data flow analysis on interactive sequential procedures to produce a parallel executable code that utilizes the intergrated vector processing capabilities of the Convex hardware. Initial installations have reported performance of about 10 to 20 times that of a VAX 11/780. Minimum prices for the system start at $500,000.

Multiprocessor makers represent another class of competitors in the scientific computer market. Denelcor's Heterogeneous Element Processor (HEP) is a modular system reportedly capable of 160 MIPS. The company expects to produce HEP machines with performance ranges up to 1,000 MIPS. Elxsi also manufacturers a modular multiprocessor system, the System 6400. Each CPU consists of an ECL processor packaged on three boards. From one to ten processors can be included in the system providing calculation speeds ranging from 4 to 40 MIPS. System prices range from $350,000 to $5 million.

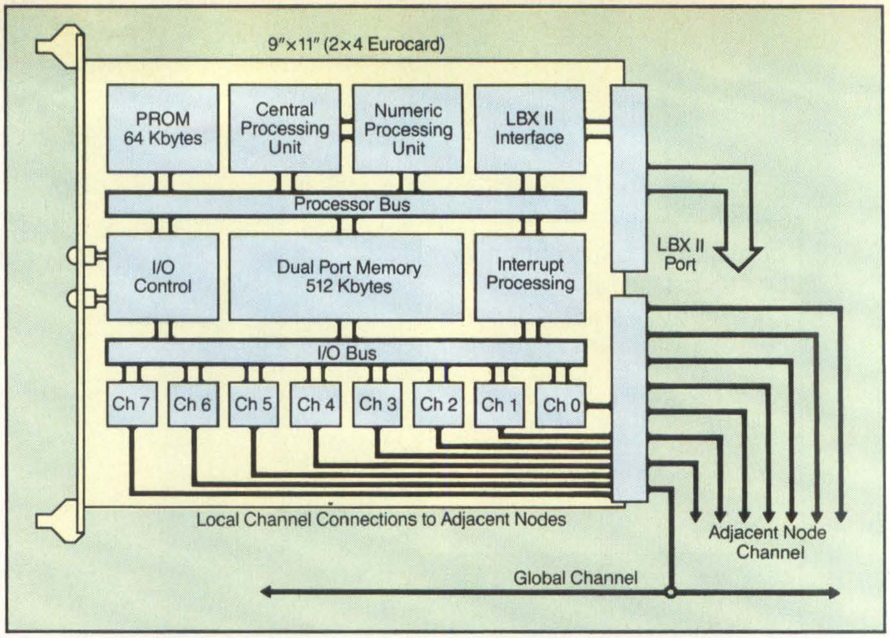

Figure 2: A single node on the Intel Cube.

The third approach recently disclosed by Intel Corp. (Beaverton, OR) is based on the hypercube topology developed at Caltech. The basic iPSC system consists of 32 microcomputers connected to each other via multiple high speed communication channels. This group of processors is connected via a global communications channel to a local host processor called the cube manager which supports the programming environment and the system management. Each microcomputer or processing node is comprised of a 286 processor, a 287 floating point unit, 512 Kbytes of CMOS RAM and 64 Kbytes of ROM contained on a Eurocard printed circuit board (**Figure 2**). In addition each node contains seven point-to-point bidirectional communications channels and a single global channel. Each channel is controlled by a dedicated communications processor. These processors move messages between nodes via dedicated point-to-point communications channels, with integrated DMA to the associated nodes RAM.

The initial iPSC family contains three products, the iPSC/d5 with 32 nodes, the d6 with 64 and the d7 with 128. Each node runs under the iPSC Node Kernel, a message-based operating system that manages each node's resources. It provides the nodes with distributed processor communications, multiple process management and dispatching, and process debugging. The cube manager in the system is an Intel 286/310 microcomputer running under the Xenix operating system. It serves as a local host for the cube and supports local diagnostics. Intel claims that initial iPSC products will provide a performance range approximately 0.1 to 0.4 that of Cray 1.

It is important to note that compilers used to generate process code for the cube do not automatically find a way to run sequential programs concurrently. In fact, because efficient concurrent algorithms may be quite different from their sequential counterparts, the Caltec researchers regarded the translation as implausible. They attempted to formulate and express a computation explicitly in terms of a collection of communicating concurrent processes. This would place the Intel product firmly in the academic world. However, Intel is committed to work with these researchers and with third party vendors in developing application software that will accelerate commercial use of the iPSC systems in coming years.

—Wilson

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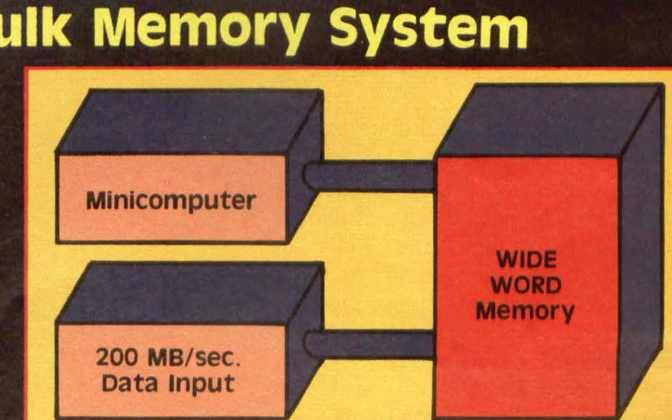

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Supermini Series Ranges From Entry Level To 10-Processor System

Innovations in architecture provide minicomputers with the speed and balance they need for complex, time-sensitive applications. Multiprocessing systems greatly improve computation speed. Additional processors for the new high-end 3260MPS system from Perkin-Elmer (Oceanport, NJ) speed not only number crunching, but also I/O. This modular parallel processing architecture is one that they plan to extend throughout the 32-bit product line.

Tightly coupled multiprocessing is not new to the PE 3200 series; earlier 3200MPS systems use up to nine APUs on the global memory bus. But the single CPU performs all I/O operations as well as executing the operating system and user tasks. So I/O bottlenecks may offset some of the computation speed advantage.

Processors for the new 3260MPS can be APUs or I/O processors (IOPs). All are connected by the 32-bit paths of the global memory bus (up to 64 Mbits/sec), and RTSM 8-bit parallel interprocessor links. For more than 10 processors or fault-tolerant standby, two systems can be cross-coupled and share memory.

IOPs are microcoded to support I/O operations and instruction sets, an auto-driver channel and task communications with the CPU. They also have 4K of cache, bus switches for CPU or IOP control of devices, a shared memory interface and 4K × 32 of RAM. In addition to peripheral operation, IOPs can be programmed for applications such as data compaction, limit testing and handling special devices.

Distributed logical I/O allows indexed file transfer to be offloaded from the CPU to APUs. This feature may increase file transfer throughput as much as five to ten times, as well as increasing CPU availability from an estimated 52% to 87%. PE's OS/32 operating system provides transparency of multiprocessing and I/O processing.

With processors that can be added, programmed and configured as desired, expansion and customization are eased. The base price for a 3262 (3260MPS with two memory banks) with one APU or IOP is $185,000; each additional processor is $42,000. These processor modules are compatible with all 3200 systems, and APUs of installed systems can be upgraded to IOPs for $11,000.

This high-end supermini was introduced with an entry-level machine in the series. Rounding out the low-cost end, the 16-user 3203 comes in a small desk-high enclosure. The 3203 fills the gap between microcomputers and superminis, while maintaining compatibility with larger PE systems.

Not only is the look of the 3203 comparable to supermicros (**Figure 1**), the $10,292 quantity 100 ($16,600 unit) price is competitive. Integral to the basic unit are ½ Mbyte of memory in single-in-line packages (SIPs), 51 Mbytes on a 5¼" disk, a 60 Mbyte streaming tape backup, one printer port and eight terminal ports.

Three of the five slots are used for the base system. The CPU board includes the memory (from ½ to 4 Mbytes) and floating point capability as well as the 334 Kbit/sec multiplexor bus and 1.5 Mbit/sec selector channel bus. A 68000-based controller has 8K loader storage, bootloader, clock and the parallel printer and RS-232 ports. The third card is for SCSI peripheral control; it is also 68000-based and has up to 128K of RAM.

To support the low-end products, PE has enhanced their Reliance PLUS software. Its main thrusts are in transaction processing, database management, communications and query, update and report tools. 3200 communication allows SNA and other IBM modes as well as Ethernet and X.25 gateways. Up to 16 IBM PCs, IBM or PE terminals may be connected to the 3203.

The 3203's small footprint is pointing the way for superminis. Some peripheral manufacturers will be hard put to pack supermini capacity and performance in a 5¼" form factor. Peripheral makers will also feel pressure to support the SCSI bus as more large system firms move away from the old proprietary interfaces.

This product is an indication that microcomputer features of small size and standard interfaces are being designed into mid-range products. Multiprocessing may also become feasible for a broader range of products. Though initial innovations have been from start-up companies and in high-end products, parallel processing and other new architectures will become more important for all systems. With these products, Perkin-Elmer is not only broadening their 3200 line, but also indicating where some of the future trends may lie for minicomputers.

—Pingry

Circle 236

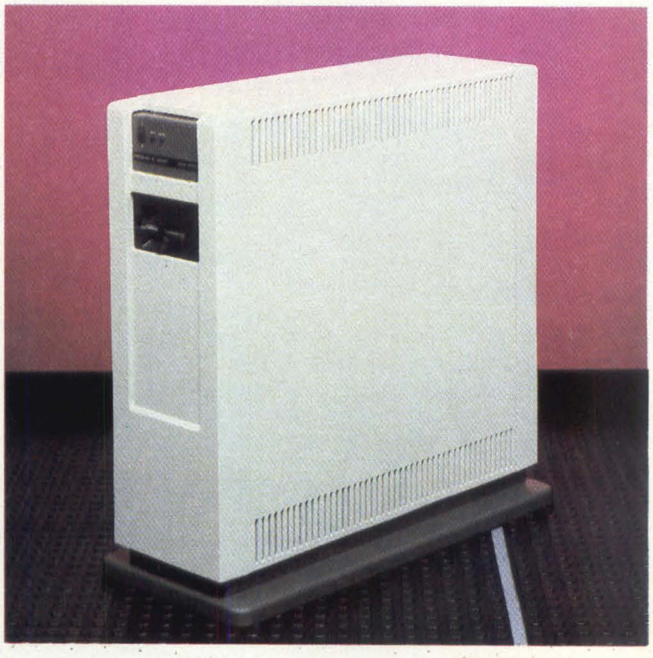

Figure 1: The entry-level 3203 is packaged in the free-standing desk-high enclosure made popular by supermicrocomputers.

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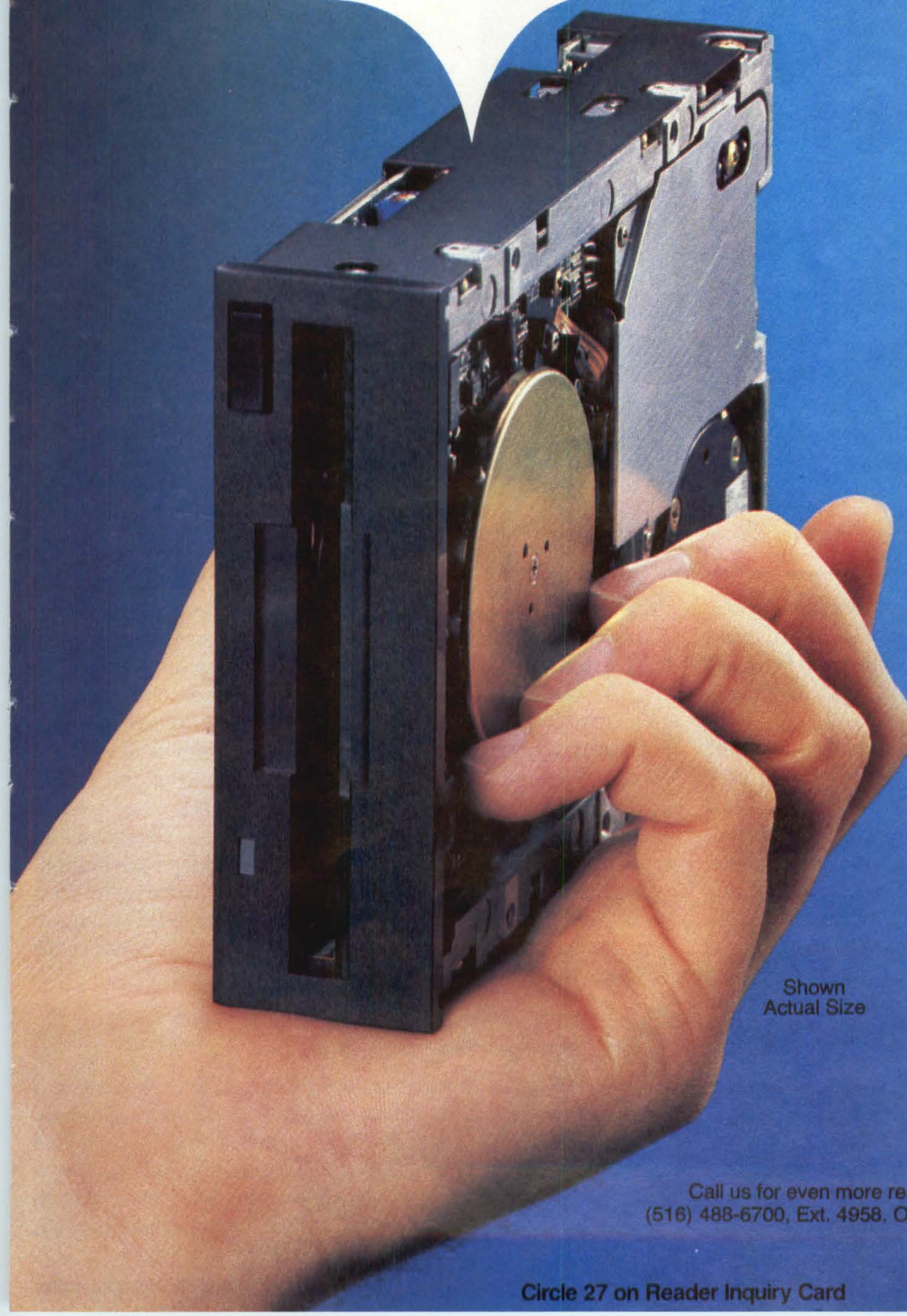

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MD351: 135 TPI, single sided, double density, .5 Mbyte.
MD352: 67.5 TPI, double sided, double density, .5 Mbyte.
MD353: 67.5 TPI, single sided, double density, .25 Mbyte.

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With the gate array finding widespread use, new tools are required in the design process: is the workstation a viable solution?

Unlocking The Mysteries Of Gate Array Design, Part III

by Ronald Collett, Sr. Technical Editor

Having full control over the design cycle is the key factor in gate array design. In this report, the third in our series (Parts I and II appeared in January and February 1985), we examine whether or not workstations provide that added control.

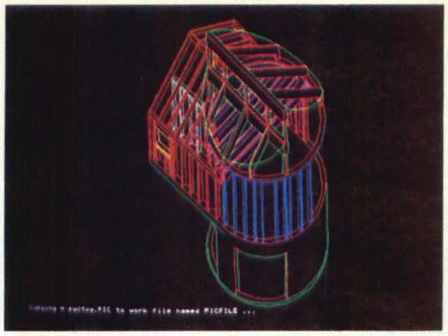
Workstation vendors often paint a colorful picture depicting a turnkey CAD/CAE system as the ultimate tool providing the designer with full control over a design cycle's front end. While this is true in some situations, the workstation is clearly inadequate in others. Moreover, several viable alternatives do exist.

The first is for the customer to hand over his schematic and test vectors to the array vendor, allowing the vendor to perform the entire task. In this case, schematic capture, simulation and timing verification are among the vendor's responsibilities. Not only is this the most costly method, but the chance of a design oversight increases. Despite this drawback, many customers prefer to absolve themselves from the design implementation. A second alternative is to use the vendor's in-house CAD/CAE system where the customer performs all of the front-end stages of the design. In this situation, computer charges are a variable cost. Larger designs incur higher computer charges. A fourth option is to purchase a mainframe or a supermini computer along with third-party software. With this solution, however, CAD/CAE programs among third party suppliers are often incompatible with each other and the gate array vendor's cell library. A final alternative is to use a low cost personal workstation for schematic capture and perhaps small simulations.

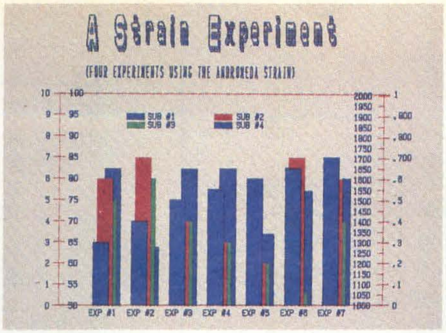
Although a certain percentage of designs are completely implemented by the IC vendor, the clear trend is for the customer to assume responsibility for timing analysis, simulation and test vector generation. Thus, the issue is whether to use the IC vendor's CAD/CAE system, purchase a large host or buy a workstation. Each class of designs is accompanied by a particular set of variables which in turn reflect a unique CAD/CAE solution. Aside from finances, the technical issues influencing the decision include the following: (1) number of arrays to be designed in the future, (2) size of the arrays, (3) operating speed of the chips and (4) length of time alloted for the design.

Behind The Scenes Of Design Verification

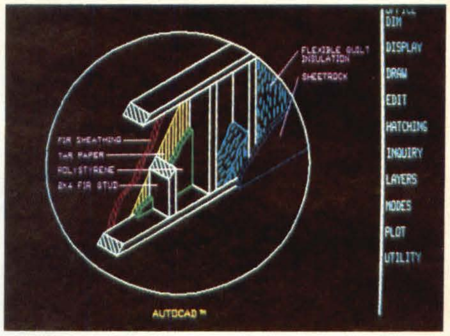
Comprehensive timing analysis is the crucial element in a design cycle's front end. Because of its significance, LSI Logic (Milpitas, CA) developed a timing analysis program called the Design Verifier. Normally, when LSI Logic's CAD/CAE system is used for gate array design, the Verifier is incorporated into their software and overall design methodology. Recently,



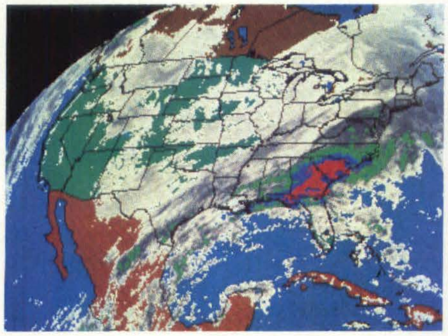
1. High Speed (MicroCAD Software)



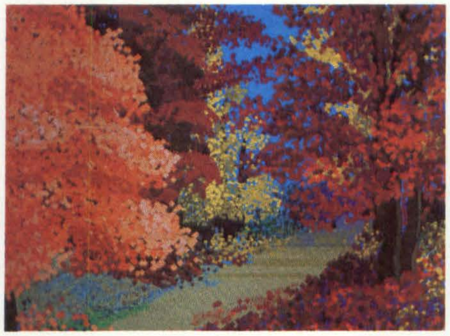
2. Dual Display Modes (Energraphics Software)



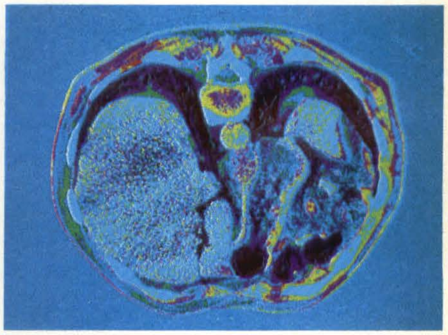
3. Simplified Processing (AutoCAD Software)



4. 9 Bit Planes (Courtesy WSI Inc., Bedford, MA)



5. 16.8M Color Shades (Courtesy Catherine Del Tito, Wave Graphics)



6. High Resolution (Courtesy University of North Carolina at Chapel Hill, Depts of Computer Science and Radiology)

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however, LSI Logic ported the Verifier to workstations offered by Mentor, Daisy and Valid.

With the Design Verifier, the user gets the most accurate representation of the circuit's timing characteristics before layout. In short, fabrication process deviation and estimated wire lengths along with actual fanout are combined to yield a statistically-based delay model at each node in the circuit. In contrast, many gate array vendors that port their cell libraries to third party workstations incorporate fixed propagation delays into the library's models. In this fashion, a wide variation may exist between the CAE timing analysis and the circuits actual performance. Design verification of high speed circuits demands fabrication process deviation, wirelengths and actual fanout be included in the delay model. There is only one drawback to the Design Verifier: a $28,000 price tag. Since it is expensive, its cost can be justified only in high speed designs where fabrication process technology is pushed to the limit.

Like most other array vendors, LSI provides a low cost version of their cell library (approximately $2,000), the so-called Software Databook. Unlike the Design Verifier, all propagation delays are fixed.

Workstation Advantages

Generally speaking, engineering workstations offer schematic capture, logic/circuit simulation, timing verification and documentation software. Although Valid Logic's (Mountain View, CA) Scaldsystem I was chosen to implement our design, *Digital Design* examined competitive products from Mentor Graphics (Beaverton, OR) and Daisy Systems (Mountain View, CA). Like Valid's system, both were viewed in the context of gate array design. All of these products allow the front-end design tasks to be completed with minimal reliance on the IC vendor. This reduces computer charges, which typically amount to about $1.25/CPU-sec. A $20,000 computer cost would not be unusual for an 2000-gate array.

An increasing number of firms are recognizing that graphical schematic capture is a vital element in the designer's tool box. In most instances, engineers given the opportunity to use a graphics editor find it difficult to retreat to traditional alphanumeric methods of schematic entry. Even more significant, graphical methods drastically reduce the number of wiring errors associated with conventional alphanumeric design entry. In designing our gate array, we found that a graphics editor together with a puck significantly facilitates design.

Comparing one schematic entry system to another requires focusing on exactly how many steps a particular operation requires. Look at the sequence necessary to move a chunk of circuitry from one point to another. Also note the procedure for connecting wires and check whether components can be easily flipped sideways and upside down. These are just a few of the basic features that a schematic capture tool should possess. Every drawing task that a draftsman could do by hand should be easily within the workstation's grasp.

Schematic checking eliminates drawing oversights. Once the schematic is entered and the "schematic checker" is invoked, the machine culls flagrant wiring and signal name errors. Typically, a design with a few thousand gates is completely checked in less than a minute.

Compilation of the circuit is the next step in the design cycle. Circuit elements are compiled into a format suitable for input to the verification software. Depending on the size of the design, this process takes anywhere from a few minutes to several hours. When executed on an IC vendor's mainframe, compilation time is much shorter. Nonetheless, CPU costs are completely avoided in workstation-based designs. Once the circuit is compiled, electrical rule violations are flagged.

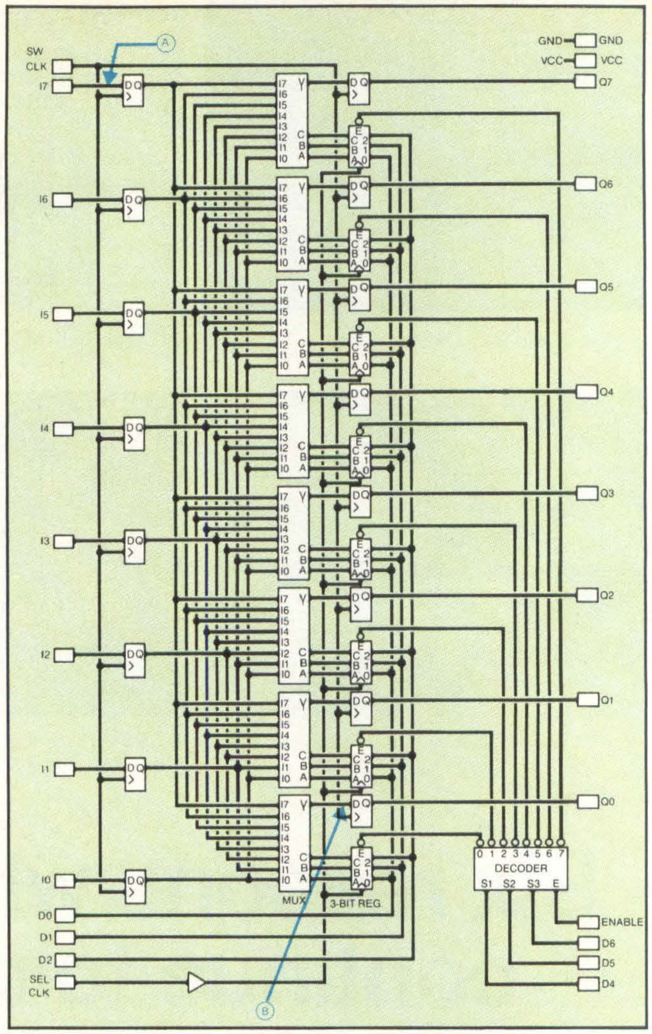

Figure 1: In this circuit, the critical path lies between points A and B where the propagation delay can be no longer than 43 nsec. The timing verifier would determine if the delay is longer than 43 nsec.

Simulation and timing verification consume the most time in the design cycle's front end. Consequently, when utilizing the IC vendor's CAD/CAE system, this stage dictates computer costs. However, hardware accelerators have added to the workstation's performance. Accelerators implement simulation algorithms in "hardware" and thus increase simulation execution speeds by several orders of magnitude. For complex large arrays, this is a must.

When simulating logic, timing considerations are usually not taken into account. Instead, the logic's functional operation is checked. After the circuit is logically correct, timing analysis is performed. Timing verification searches for race conditions, pulse-width violations and delay problems (**Figure 1**). Again, depending on the size of the circuit, the time per simulation or timing verification run ranges from a few seconds to several hours.

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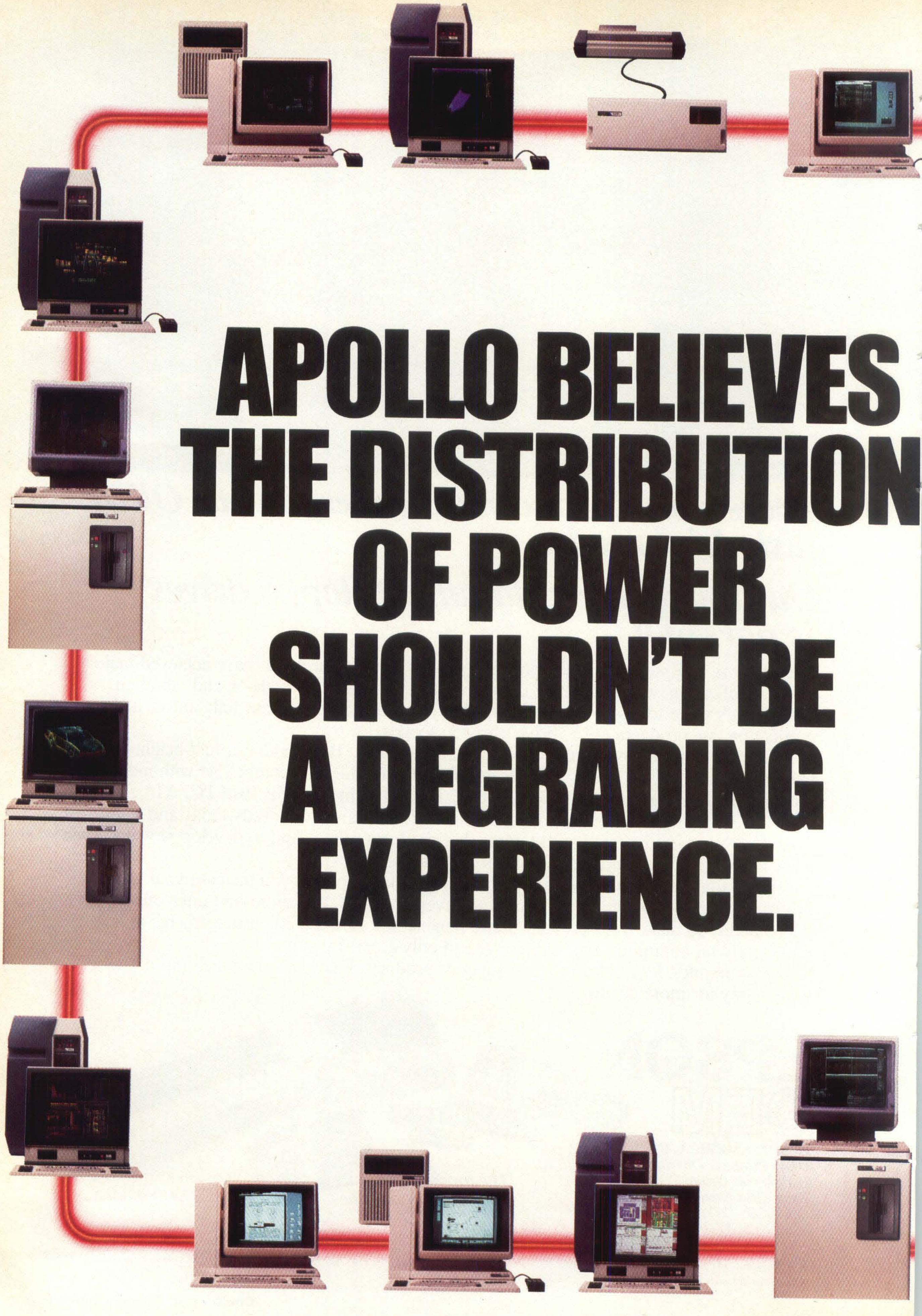
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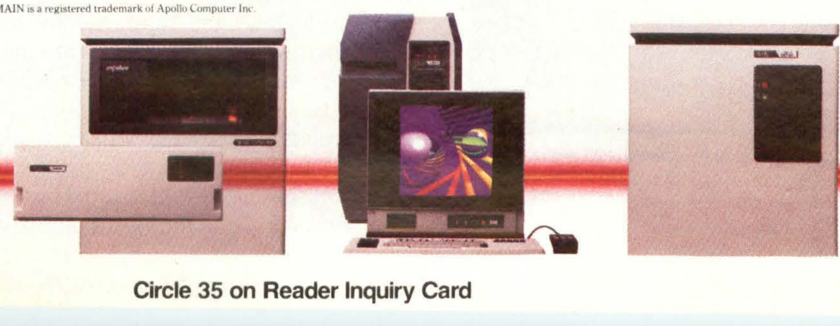

Workstation Disadvantages

Compared to a mainframe, workstations perform very slowly. Even if these systems could run as fast as a VAX 11/780, larger arrays demand mainframe-based CAD/CAE systems with execution speeds of 4-5 MIPS. Although hardware accelerators drastically reduce simulation run times, compiling times are still excessive. Thirty minutes to two hours is not unusual for a single compilation on a workstation. With a mainframe, however, the time shrinks to a few minutes.

Workstations purport to exist as single-user systems. Due to their high cost, however, sharing one unit among three to five designers is not uncommon. Prices for these machines range from $70,000 to $100,000, not including a hardware accelerator.

Hardware accelerators are designed to function as a network resource, allowing several users to simultaneously access the device. Therefore, only one accelerator is necessary for multiple workstations. Although this is some consolation, it is of nominal benefit. A comparison between the cost of a mainframe design environment and workstation configuration demonstrates the point. The cost of 25 workstations plus a hardware accelerator ranges from $1.6 million to $2 million. On the other hand, a design environment consisting of a VAX 8600, a low-end Zycad (St. Paul, MN) hardware accelerator, 25 PC-based schematic capture systems and LSI Logic's CAE software (LDS III) costs about $1.6 million. Advantages of a VAX 8600 are execution speed, versatility and the number of users that can simultaneously access the system. For large design environments, the better bargain is the mainframe solution.

Figure 2: Valid's Scaldsystem I is currently being used by *Digital Design* to implement a crosspoint switch on a CMOS gate array from LSI Logic. Valid's system excels in the graphics area. In addition, all software runs under both UNIX and DEC's VMS operating system.

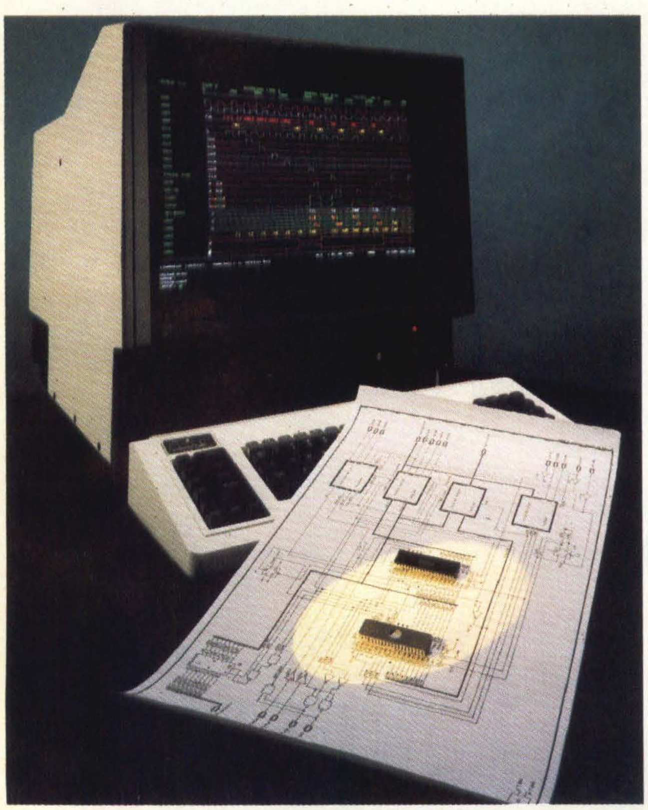

Figure 3: Daisy's Megalogician offers good execution speed with respect to compilation. As indicated, waveforms are displayed in a format similar to a logic analyzer and thus allows the designer to rapidly interpret the data.

One criticism of Zycad's machine is that it simply moves the simulation bottleneck from the execution stage to the compilation stage. More specifically, running a simulation on the accelerator requires that the logic be compiled into Zycad Intermediate Format (ZIF) first. Compilations have been known to require anywhere from a few minutes to many hours.

Like LSI Logic, Valid's CAE software runs on the VAX. Because of its graphics capabilities, many labs use Valid's Scaldsystem I primarily as a schematic capture tool. Running compilations and simulations on a mainframe is the only way to complete large array designs rapidly. Neither Daisy nor Mentor offer application software that runs under a common operating system such as UNIX or VMS. However, Daisy is currently porting their software to run under UNIX. The effort is expected to be completed in the next four months. Likewise, Apollo Computer plans to provide UNIX on their systems in the near future.

One complaint about mainframe computers is that they get bogged down during peak hours of operation and cannot adequately handle the workload. As a result, many claim the distributed processing power of a network of workstations yields greater productivity. Although this may be true to a certain extent, a mainframe executing 4-5 MIPS is not likely to be "brought to its knees" unless 25 to 30 users are simultaneously running memory intensive tasks such as logic simulation.

Realizing many systems manufacturers are not in a position to make a $1 million-$2 million investment in design tools, the issue remains whether to purchase a high-end workstation or buy computer time from the array vendor. Based on our gate array design experience, workstations do not provide the performance necessary to complete a large gate array in a timely manner; 1200 to 1500 gates would be pushing the limit of workstations from both Daisy and Valid. Mentor would be slightly higher since their workstation is based around a higher performance machine – the Apollo DN660. Excessive compilation and simulation times are the primary reasons for our criticism. Memory capacity is another significant workstation shortcoming in large designs. This is not to say that the job cannot be completed on a workstation, rather the rapid turn-around time found with gate arrays is lost to the workstation's slower execution rates.

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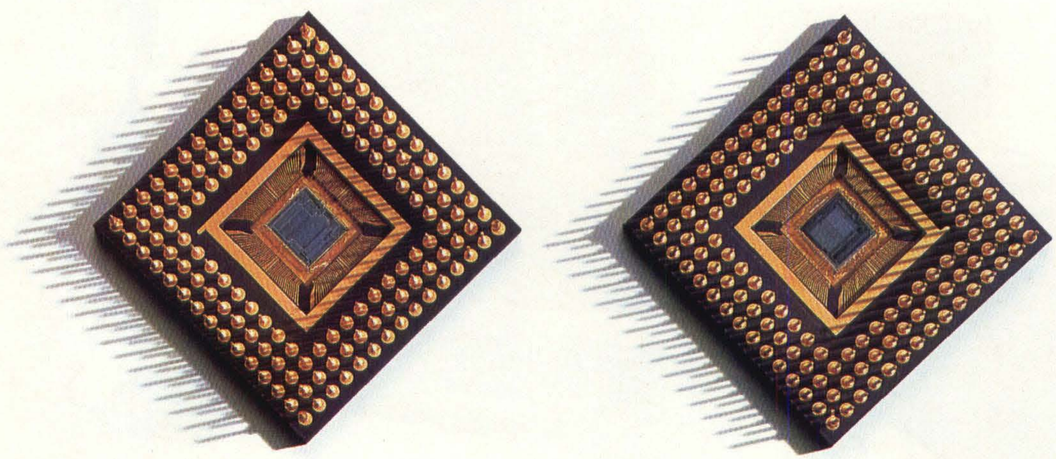

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For smaller array projects, the workstation is a viable solution. However, if only a few small arrays are to be designed, the IC vendor's CAD/CAE system is probably the better solution because computer charges will remain low anyway. High-end workstations become cost effective when many small arrays are to be designed.

Comparing Daisy, Mentor And Valid

Approximate prices for workstations from Daisy, Mentor and Valid are as follows: Daisy's Logician is $100,000, and the version of the Logician that includes the hardware accelerator (Megalogician) is $125,000; Mentor's DN660-based workstation is $90,000, with the hardware accelerator price set at an extra $180,000; Valid's Scaldsystem I is priced at $70,000 ($130,000 for the four-user configuration) with the hardware accelerator priced at an additional $38,500. Mentor's hardware accelerator, which is manufactured by Zycad, performs 500,000 evaluations per second; Valid's performs 500,000 evaluations per second; and Daisy's performs 100,000 evaluations per second. From a price performance standpoint, Valid is the better choice. Although when the Scaldsystem I supports four users, this load drastically slows the system.

Schematic capture and graphics capabilities of Daisy, Mentor and Valid were compared. Valid was the best, with Mentor running a close second. Valid's ease of use and limited number of steps per change or addition were the deciding factors. However, Valid's superiority is tainted if a design is entered "flat," because the time necessary to compile and simulate the drawing increases significantly. As noted in Part II (February 1985), exploiting the Scaldsystem I to the fullest requires the schematics be captured in a streamlined fashion. This method, which employs the "sizing" command, yields a drawing that is often difficult to decipher.

As indicated earlier, the ideal configuration employs the Scaldsystem I as a front end to a mainframe. Thus, schematics are entered in the traditional "flat" style with the compilation executed on the mainframe. If a larger computer is unavailable and a workstation is to be the sole source of computer power, Mentor's DN660 would be the more favorable alternative. Valid is reportedly revamping their compiler to increase compilation speeds by a factor of 10.

Unlike Daisy and Valid, Mentor's system automatically divides the display so there is an entire schematic in one window and a close-up of the area under construction in the other. With interwindow communication, the cursor is located at the same point on the schematic in both windows. Without this feature, the designer can easily lose track of which area of the schematic is under construction. Although this extra window consumes screen space, it is very useful for entering large complex circuits. Both Mentor and Valid permit "point and drag." This allows the user to pick up a component and drag it across the screen; rubberbanding is also standard on Mentor and Valid systems. These features are a tremendous benefit in schematic capture.

In comparing the compilation speeds between Daisy and Valid, we found Daisy to be faster if the design is entered "flat" on each system. Daisy does not require the user to "size" drawings to exploit their system's performance. Although we did not have an opportunity to measure the compilation speed of Mentor's DN660-based system, we assume it offers the highest performance of the three since it uses a full 32-bit processor.

Figure 4: Mentor's high-end workstation, based on the Apollo DN660, offers very good graphics and provides execution speeds just below that of a VAX 11/780. Like Daisy and Valid, Mentor offers a hardware accelerator that significantly speeds logic simulation.

Incremental compilation capability is a major advantage that both Daisy and Mentor have over Valid's Scaldsystem I. With this feature, designers make changes in schematics without completely recompiling the entire design. For instance, instead of rerunning a 35 minute compilation, the task is completed in less than five minutes. Sometimes, however, when a particular change affects several different portions of the circuit, incremental compilation is not possible. From a functional standpoint, timing verification and simulation capabilities were comparable among the three systems. However, waveform data is displayed most informatively on Daisy's workstation (**Figure 3**). Again, Mentor runs a very close second in this category.

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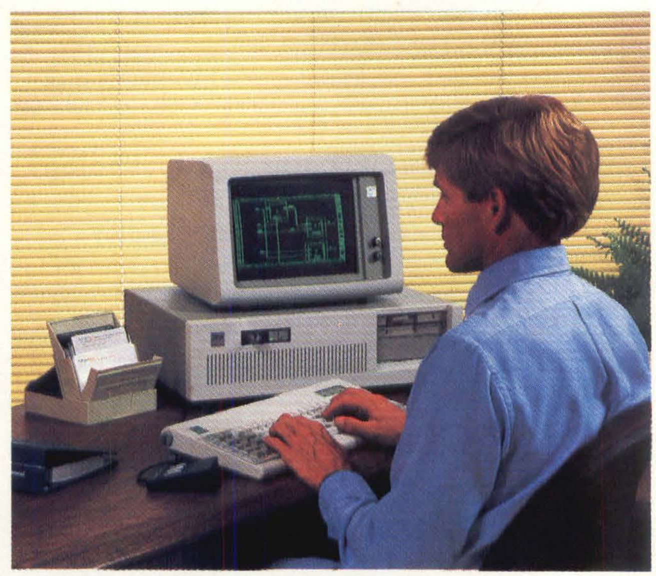

Figure 5: Futurenet's Dash-1 and Dash-2 can be configured on the IBM PC XT or AT. In addition, these systems can be equipped with the Dash Cadat, a 32016 co-processor board with 1 Mbyte of RAM, providing designers with simulation and timing verification.

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Keyboards Range From Simple Components To Intelligent Input Subsystems

by Julie Pingry, Senior Editor

Integrating the keyboard into a system poses choices of technology, intelligence and layout to system designers. Both keyswitch and electronics technology have advanced to allow data entry keyboards to be self-contained systems. European DIN standards for ergonomics that dictate detachability are further impetus for intelligent keyboards. With the microprocessors currently used, basic keyboard control and functions to control many elements of an input system are available.

At the other extreme, many computer-based systems are now low-cost commodity items. These applications require a keyboard that is inexpensive and ready to integrate. Since the lifespan of personal computers and low-end terminals is short, many reliability features like non-contact switching, double-shot molded keycaps and life cycles up to 100 million keystrokes are more than the application demands.

So the data entry full array, full travel keyboard business can be divided into at least two distinct categories. Simple, low-cost devices for integral use and high-end, reliable, intelligent peripheral products both can use any of several technologies for switching. Important differences will be in customizing, delivery, marketing and support. Switch technology will still be a choice, even after the vendor has been chosen.

Ergonomic standards have changed more than where the electronics are placed; the demand for a low profile package has opened the market. Many designs are calling for a new keyboard to meet standards or special requirements, and some firms are now looking beyond their long-standing supplier for comparison.

Technology Trends

Glass reed relay and electromechanical switching were mainstay keyboard technologies for many years. Over the past 10 years, other technologies have gained

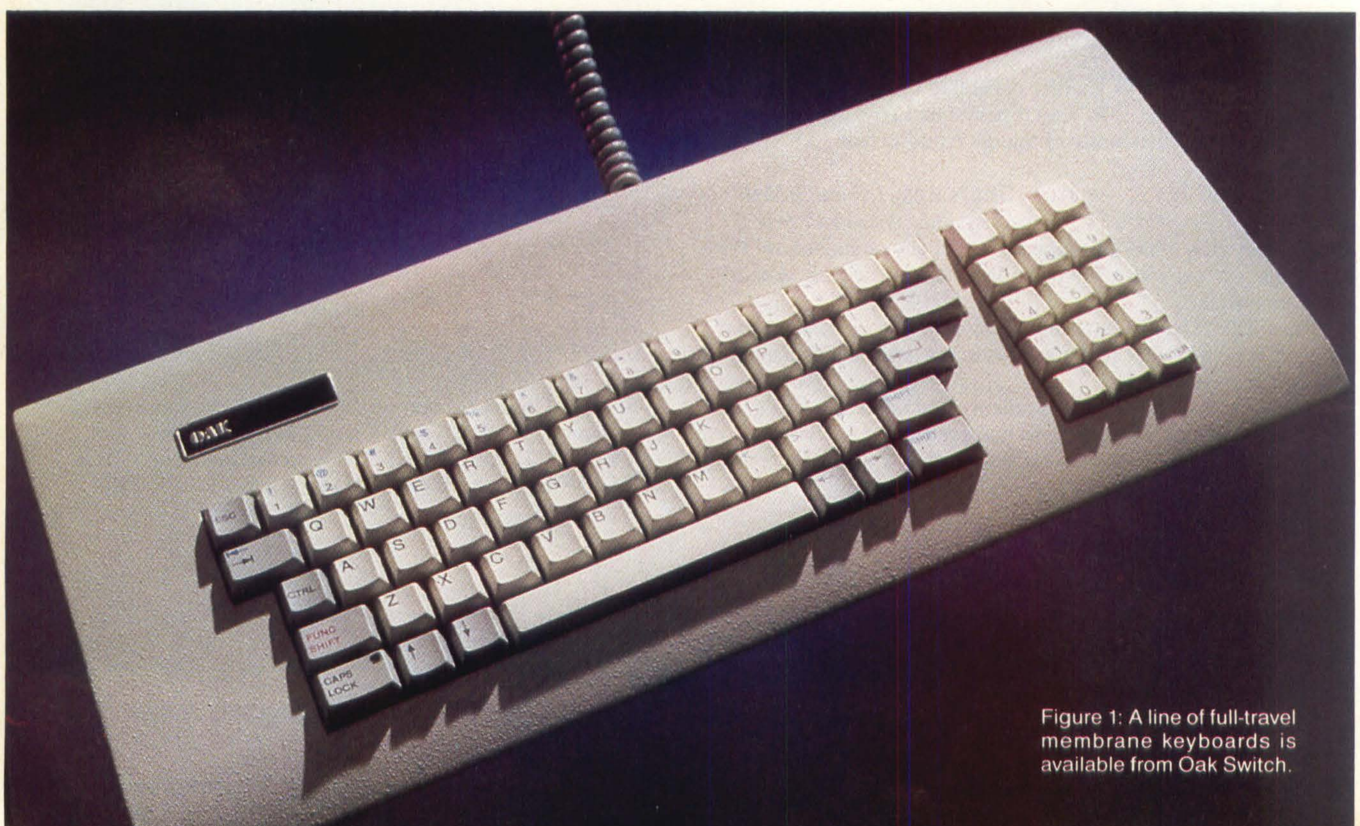

Figure 1: A line of full-travel membrane keyboards is available from Oak Switch.

prominence; nevertheless, reed and mechanical keyboards are still available from several sources. In the mid-1970s, inherently reliable noncontact technologies had a surge in popularity. More recently, membrane and elastomer (or rubber) switches have gained market share. All these types of switches will be used for data entry keyboards throughout this decade. And though functionality, quality and supplier capability may be the major factors in choices, the technologies do differ and each has strong features.

Reed relay switching is still useful for very hostile environments. The sealed contact switches are impervious to oil, gas and humidity, and may be found in point-of-sale, machine tool and process control applications. Though not a volume production offering, Keytronics (Spokane, WA) and Maxi-Switch (Minneapolis, MN) supply reed relay boards. A major drawback to reed switching for data entry keyboards is that the switches are too tall to meet DIN standards for low-profile.

Electromechanical (often called mechanical) switching was not very reliable in its original form, partly because the physical contact points could wear and were not sealed from contaminants. Most mechanical keyboards are now specified for 20 million-50 million keystrokes; Hi-Tek's (Garden Grove, CA) IBM PC-compatible products are specified at 100 million cycles.

One design change that contributes to enhanced mechanical switch reliability is a move away from the single gold contact for closure. One firm focusing on this field, Stackpole (Raleigh, NC), uses twin bifurcated contacts, for four contact points, rather than one. Hi-Tek similarly uses trifurcated contacts. Cherry (Waukegan, IL), another leader in mechanical keyboards, uses gold wire crosspoint switches, for extremely high pressure on a small contact area closing. Mechanical keyboard manufacture is relatively low cost; and since single keys can be made, customizing doesn't cost much.

Figure 3: Stackpole's KS-600E mechanical hard-contact keyboard meets DIN low-profile specifications and can easily be made in custom configurations.

In 1968, Micro Switch (Freeport, IL) introduced new levels of reliability with the Hall-effect keyboard. This magnetic switching technique eliminates the hard contact, and its introduction marked the beginning of electronic noncontact keyboard availability. Hall-effect switching, though highly reliable, is a relatively costly technology.

Another noncontact switching method, capacitance, has gained a large market share since the mid- to late-1970s. Though electronic in the switch function, capacitive products are not as expensive to manufacture as Hall-effect. The wide use of these two contactless technologies increased the industry standard life cycle specifications to 100 million cycles. Capacitive keyboards are available from many firms, including Keytronics, General Instrument (El Paso, TX) and some whose product line began with other technologies. All noncontact keyboards have generally been more expensive than hard-contact types, though many models are now comparably priced.

Membrane keyswitching has come onto the scene fairly recently for data entry products. For some time, peripheral, instrument and other keypads for relatively low-speed use have used conductive screening on membrane layers for flat panels. A full-travel membrane keyboard (**Figure 1**) was introduced by Oak Switch (Crystal Lake, IL) in August 1980, just two months before IBM's PC with that keyboard technology was announced. The layers of a membrane keyboard may switch either by hard contact or by capacitance, depending on what material is screened onto the switching layers.

Figure 2: The PC-84D from Hi-Tek uses the Dvorak key layout, with often-used keys in convenient positions. Note that vowels are on the left side of the home row.

A similar layered approach to keyboards is offered by conductive elastomer or conductive rubber materials. Rubber may be used in a dome configuration for hard contact switching or screened for capacitance. Like membrane, rubber switching has primarily been used in minimal travel key panels. The costs are low, and with appropriate full-travel keys over the rubber layers as actuators, companies like Advanced Input Devices (AID) (Coeur D'Ilene, ID) and Maxi-Switch offer products for data entry. There have been some doubts about the

wear tendencies of elastomer keyboards since switching actually deforms the rubber layer. However, AID specifies a minimum of 60 million keystrokes with their non-silicone rubber dome keyswitches.

Each switching technology has advantages, and the system design will determine which characteristics are most important. The quality of the finished product in feel, life specifications, delivery time and cost are the main factors to consider. These may be largely independent of the technology, but vary between suppliers.

The Low End

Since computers are no longer necessarily large, expensive machines and, more importantly, since technology advances occur very frequently, the useful life of many systems has dropped. The volumes for these micro systems are often very large and profit margins accordingly small. As systems drop in cost and high-volume applications like personal computers and terminals become more competitive, keyboard costs must be kept low.

Membrane and rubber keyboards do not need to be placed directly on a printed circuit board. For a detached DIN-standard keyboard, some of this advantage is lost. But many low-end systems still use integral keyboards. These keyboards can be "wired-only" or unencoded, with electronics for keyboard control included with the computer or terminal boards.

Portable computers may demand an integral keyboard. Another consideration with portable systems is low power consumption. Electromechanical keyboards, whether membrane or mechanical, drain little power when keys are not depressed. Since capacitance switches are scanned for data, they drain more power than desirable for battery-driven computers.

Many simple computer-based products are designed for relatively inexperienced users, or for infrequent use. Even poorly manufactured computers last as long as most companies and individuals want to keep a particular model. The common 100 million keystroke spec of Hall-effect and capacitance products is clearly more than needed for these systems, which might not even reach the 20 million-50 million keystrokes of many low-cost hard contact models.

Simple unencoded keyboards, commonly mechanical, membrane or rubber, are generally inexpensive. But costs to makers of mechanical keyboards using

A natural extension of the keyboard is control of other input devices in the enclosure or connected to it.

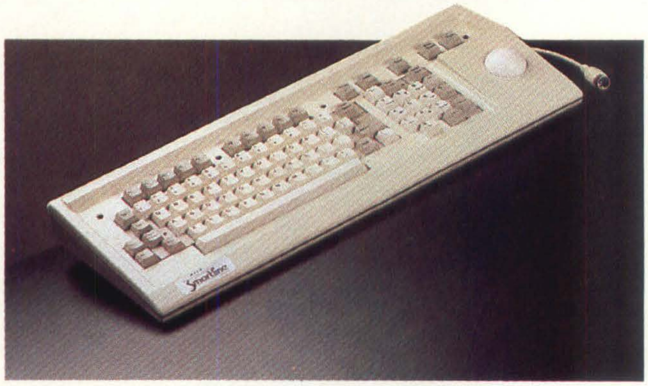

Figure 4: Trackball and keyboard are included in one enclosure in the programmable Wico Smartboard; it can be used either as a Dvorak or standard Qwerty device.

precious metal contacts such as gold can vary greatly with market forces. Rubber keyboards may also use these variable-price metals on the controlling PC board.

Many companies currently supply unencoded keyboards at low prices. But as in other commodity markets, Japanese and other far-East companies' labor force usually produce for much less than US laborers. Several Japanese companies have offices in the US: Alps is based in San Jose, CA, now; Panasonic's Electronic Components Division in Secaucus, NJ, handles their keyboard line; and Fujitsu America's keyboard operation is based in Lake Bluff, IL.

Though many US keyboard manufacturers are using automation and off-shore manufacturing, these Asian firms are difficult to compete with for simple mechanical products. Some US makers of rubber and membrane products have a lead on the Japanese in these inherently low-cost technologies. Despite the furor over the IBM PCjr chicklet keyboard, supplier AID is shipping large volumes of inexpensive rubber dome keyboards. Many other domestic firms are looking to value-adding and higher-end market segments for their livelihood.

Flexible Keyboards

Detached keyboards with other ergonomic and OEM design features are the mainstay for most US manufacturers. For heavy-use systems, feel, layout, configurability and, above all, reliability, are critical. To compete in this market, firms must be able to customize keyboard appearance and electronics to customer specification and turn out consistent products in a reasonably short time.

Again, many technologies compete. As for reliability, noncontact is inherently good. To compete with Hall-effect and capacitance, keyboards using other types of switches are also specified at 100 million cycles. In membrane, the layers themselves have an almost unlimited life, and, as mentioned earlier, several approaches to mechanical contacts have improved their performance.

In harsh environments, reed relay has long been the standard. But the sealed membrane technology used for flat controls in many factories can also prevent contamination in a properly designed full-travel keyboard. In a capacitive membrane product, Micro Switch uses six layers; three are for venting so that external air pressure or temperature changes do not destabilize air pressure in the three switching layers of the sealed unit. Cherry uses membrane technology to provide a seal for silver hard contacts.

One of the main considerations for data entry devices is operator comfort, or ergonomics. European DIN standards sug-

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Our new low-profile Silent-Tactile keyboard gives you a unique combination of quiet operation and positive tactile feedback.

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Figure 5: This Keytronics subsystem with touch pad and keyboard also has ports for other input devices.

gest a home row height of 30mm or less from the desktop, with a profile angle at 15° or less. Except for reed-type switches, all switch technologies can be made to the low-profile size dictated.

In addition to height, ergonomic standards call for some form of feedback for the operator. Though tactile feel keyboards have long been available and gained popularity for a while, most full-time data entry operators find the make-point change in force tiring on the fingers. Most keyboard models are available with either linear or tactile feel. And if linear feel is wanted as well as some sort of feedback, an audible click may be used. The office environment may, however, benefit from an approach like Micro Switch's Silent-Tactile series.

Another feature that can promote accurate data entry at very high speeds is N-key rollover. This feature assures that when several keys (up to a set N or the total keys on the board) are depressed in more rapid succession than they can be processed, all are retained in memory in the sequence they were entered. This feature is standard on some noncontact keyboards, and it is an option on many products. Multikey rollover is sufficient for most uses and, with mechanical technologies, usually less expensive.

Optimum operator throughput requires a new layout of the keys. The standard Qwerty layout was developed when all typing was on mechanical devices. Before this standard, keyboards were laid out serially A-Z. Anyone who has used a mechanical typewriter has experienced key lock-ups if they type rapidly; strike two keys in succession and the first will tend not to be out of the way of the second as it comes up. The Qwerty arrangement helped avoid some key clashes by separating some keys and also slowing down typing speed.

Another arrangement, called Dvorak after its designer, places the most commonly used keys in the easiest positions to reach (**Figure 2**). Studies show vast improvements in entry speed with the Dvorak keyboard, and some schools are teaching touch typing on them. But until the education process is further along, the Dvorak keyboard options from many of the leading manufacturers will be small-run production items.

Though most designs require a custom-manufactured keyboard, the IBM PC keyboard and the DEC VT 220 configuration have become popular semistandards for layout and look. Many systems can use one of these types of keyboard and get very good turnaround time and price from the supplier. Nevertheless, most designs will vary at least the color or placement of some keys.

A vendor's ability to meet specific design requirements is important. Though rubber and membrane keyboards are generally screened all at once with a new pattern needed for each different customer order, the technologies are generally inexpensive on large runs. Mechanical keyboards can be custom-configured easily, as illustrated in Stackpole's KS-600E (**Figure 3**), for which they have keys already made and simply cut a new metal plate for the placement of the keys. The model EKS from AID is a similar single-key approach with rubber domes.

Some keyboards can be configured for various applications with PROMs or EPROMs. Essential to using other input devices connected through the keyboard, PROM can also provide flexibility as to what function keys do, where functions will reside and type of rollover. Fast production turnaround can also be achieved when a standard physical keyboard is customized via PROM programming.

One of the most interesting ergonomic dictates from the DIN group is for detachable keyboards. The standard was set for comfort and flexibility. Detaching the keyboard has several effects: information out of the keyboard must be converted from its parallel form out of the matrix into serial for transmission; and all electronics must be in the enclosure. In the past, many keyboard companies worried little about enclosures, let alone microprocessors. For the future, these detached keyboards may provide the basis for intelligent input subsystems.

Input Subsystems

The trend toward intelligent peripherals is nearly universal, and now that most keyboards are attached to the system via a serial connection, they must also have a microcontroller. Most keyboards use the Intel 8048/49/50/51 family or an equivalent or similar 8-bit part. These devices are not used to their fullest on only keyboard encoding/decoding, scanning and control.

A natural use for the processing power is to incorporate other input devices into the enclosure, or at least connect them through a port on the keyboard. The keyboard processor can then control several input devices, as well as minimizing the tangle of cords out the back of the system.

Though this is a new idea, several firms already have products with other devices included in the keyboard enclosure. Wico (Niles, IL), traditionally a manufacturer of controls for video games, has entered the keyboard market with their Smartboard keyboard with an integral trackball (**Figure 4**). The trackball quadrature output is translated into keystrokes through a Motorola 6802 processor.

Keytronics' 5153T (**Figure 5**) has an integral touch pad; the keyboard also has ports for connecting barcode scanners and voice input systems through it. Such a configuration, with one other type of input control included in the keyboard enclosure and ports for others, may become common.

In their PC AT, IBM has provided the bidirectional interface needed to connect more than one device through the keyboard. The new interface allows the computer to respond to the keyboard, for acknowledgement of a mode change, often signaled by an LED indicator on the keyboard. This is needed to switch from keyboard operation to another form of input, if both are controlled by one set of electronics.

Initially, the inclusion of multiple devices in the keyboard means only some


You can put a better keyboard in your enclosure without modifying the enclosure.
Stackpole's new KS-600E keyboard–featuring snap-in modular switches–gives you a low-cost encoded keyboard that will retrofit into your present enclosure without retooling.
The discrete snap-in modular switches assemble into a metal plate to give you any kind of main or ancillary array layout you need. The metal plate assures alignment of the switches, adds rigidity and aids in RFI/EMI suppression.
You don't have to tool up for a new enclosure or modify the present one. We'll do the retrofitting for you on the backplate, and all you do is drop it in and connect it up.
And we can provide our custom encoded scheme, or design to your proprietary encoded format. Plus we let you choose between tactile or linear feel–at no additional cost.
The ergonomically designed full travel switches have a total stroke of .140 (3.6 mm nominal), are rated at 50 million cycles, are wave solderable and field repairable. The switches contain Stackpole's patented twin bifurcated contacts, with four make-point redundancy, which assures you of switch closure. And today's sophisticated electronics make mechanical switch operation reliable and dependable...at lower cost.
Stackpole also gives you the option of purchasing our modular switches individually, or in sets of configured arrays for your in-house assembly.
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changes in the interface electronics. For the inclusion of many input controls in a single subsystem, a more powerful processor may be needed. And for voice I/O, extensive electronics are needed. A variety of relatively low-cost processors can handle keyboard control as well as translation of other types of signals into keystrokes. This scheme allows the host of common application packages written for keyboard entry to use mice, touch pads, light pens and other devices with no drivers.

As many keyboard manufacturers point out, they cope with most of the elements that a computer manufacturer does now: processors, interface electronics, PC board assembly, enclosures and plastics. Some hint that they may pursue systems since keyboards are one of the elements that cannot be significantly reduced in size for portable systems. Still, that would mean competing with current customers.

For the present, count on the power of low-cost processors within the keyboard to control several input devices. Simplification of peripheral hardware and interfaces as well as software interfaces for input options may be eased by keyboard subsystems.

Human Interface

A variety of keyboards and suppliers compete in nearly every segment of the market. Technology, customization, feel, delivery speed and prices are relevant in the choice. In many cases, trust in the supplier, an affinity for a particular feel or layout or a desire to have extremely good lifecycle specification may outweigh other criteria.

Specific operating conditions of the system must be considered in choosing a keyboard. Harsh environments benefit from sealed keyswitches, reed or membrane. For inexperienced users, tactile feel may be desirable (although in general, desired key feel is highly individual). Mechanical contact products tend to be less expensive. If integral to the system, separate electronics, as with a membrane keyboard, may be easier to service.

Turn-around time is critical in having designs completed within short market acceptance periods. Supplier ability to aid in design, to configure products and to vary the production run for a system are always important. The custom nature of the keyboard business has changed very little, even with the popularity of PC and VT 220 configurations.

To meet DIN standards, purchasing a keyboard will generally include the enclosure and electronics. Such peripheral products offer potential for a single-box input subsystem. And with graphics and other menu-driven software, mouse, touch pad or trackball input can increase efficiency. Should the market for data entry become sufficiently interested in productivity to push for education, even the Dvorak keyboard layout may take off. DD

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Useful	605
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(continued from p. 62)

The Low Cost Alternative

Valid, Mentor and Daisy each offer low-cost workstations that provide an excellent solution. Using the smaller workstation for schematic capture and then performing the design verification on the gate array vendor's CAD/CAE system is the most appropriate solution for the majority of gate array designs.

Prices for these machines are roughly $20,000. In comparing the offerings from the three firms, Valid's Scaldsystem IV was the favored choice, with Daisy's Personal Logician (AT) running a close second. Both workstations offer the basic capabilities, other than computational horsepower, found in the Scaldsystem I and Logician, respectively. Futurenet (Canoga Park, CA) is another vendor offering a low cost system compatible with LSI Logic's cell library (**Figure 5**). In contrast, Mentor's Capture Station is only a schematic capture system. Although verification software can be added to the system, it is not part of the standard $20,000 configuration.

Until the price of the larger systems comes down, or the performance increases, low-cost workstations are a better buy. Simply stated, the additional computational horsepower found in the higher priced systems is not worth the extra cost.

Where We Stand

Like most design projects, we ran into a few snags. The most significant difficulty was the incompatibility between Valid's simulator and LSI Logic's Design Verifier. The software permits the use of statistical delay data (for wiring and fanout) to be incorporated into the design verification process. However, in order to utilize this data, Valid's simulator must be invoked. The Design Verifier requires a "delay" command be placed inside the simulator command file, but the simulator was unable to understand the command.

To rectify the problem, Valid recently tailored their simulator to meet the Design Verifier's requirements. This new version of the simulator (7.5) is just reaching beta-site testing. Unfortunately, this stumbling block consumed a large chunk of time. Since we are still in the process of designing our chip, update reports will be published periodically. DD

Acknowledgements

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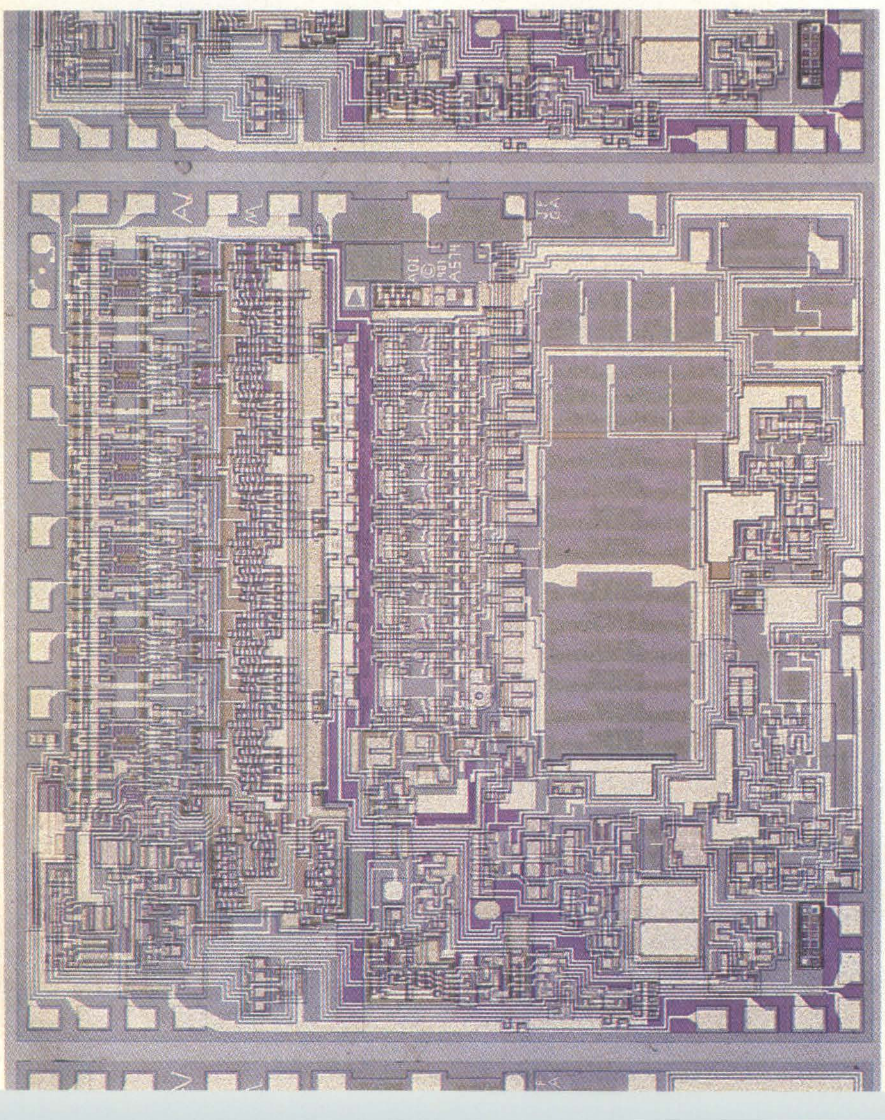
High Resolution A/Ds Approach Performance Limits

by Brita Meng, Technical Editor

The integration of functions onto high resolution A/D converters increases design options, but component limitations may make higher resolutions more difficult to attain.



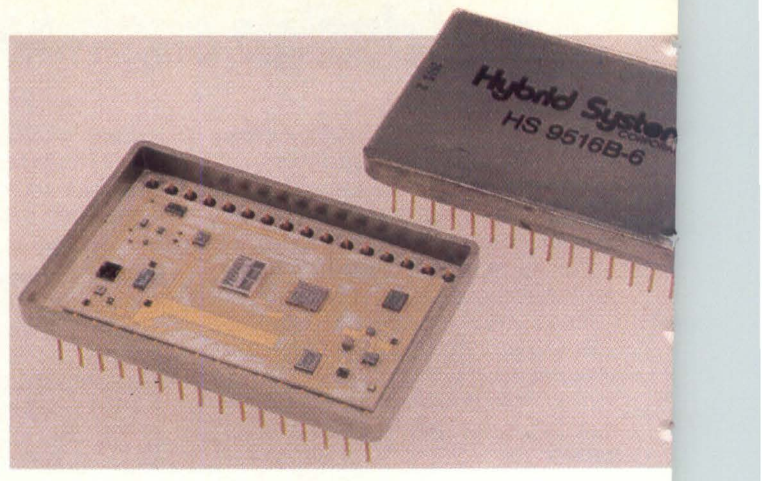
The need for higher resolution analog-to-digital converters—those with more than 12-bit outputs—is growing as the demand by systems architects for higher precision "real world" inputs increases. Applications such as telecommunications, industrial process control, digital audio, seismic exploration, robotics and instrumentation demand high resolution to obtain either high accuracy, better resolution or expanded dynamic range. In addition to higher resolution, integrated functions such as sample and hold circuits on the analog side and microprocessor interfaces on the digital portion of the A/D converter are also in demand by systems architects.

Several types of modular, hybrid and monolithic high resolution A/D converters exist, each with a distinct conversion technique having inherent advantages and disadvantages. Successive approximation, integrating and two-stage series parallel are among the most popular approaches.

The heart of the successive approximation A/D converter (**Figure 1**) is the digital-to-analog converter in a feedback loop with a comparator and a successive approximation register. The conversion algorithm consists of switching the bits of

Analog Devices' AD574, a microprocessor compatible 12-bit A/D converter, will appear in monolithic form in late 1985.

the D/A converter, which are in digital form, and comparing those bits with the analog signal input. The bit in question is set to one. If the D/A converter output is less than the input, that bit is left at one; if the D/A converter output is greater than the reference, the bit is set to zero. The register then proceeds to the next bit. At the completion of the conversion, the output voltage of the D/A converter should match the A/D analog input voltage to within one-half least significant bit (LSB). Further differences between the two voltages make up the quantization error of the converter.



Hybrid Systems (Billerica, MA) offers a 16-bit successive approximation A/D converter providing full 0.0008% linearity at conversion times of 100μsec.

This comparison algorithm can begin either with the most significant bit (MSB) or the LSB. Forward conversion starts with the MSB at high and all other bits low; the initial state for backward conversion is MSB low and all other bits high. In either algorithm implementation, the output will be the same.

The primary advantage of the successive approximation A/D converter is its high conversion speed. Another is that every conversion takes the same amount of time, possibly simplifying system design and implementation of the converter.

Disadvantages of the successive approximation converter are its need for high precision D/A converters and comparators as well as a lack of noise immunity. For example, the design of a fast 20-bit successive approximation A/D converter necessitates the availability of D/A converters and comparators accurate to 20 bits or more in order for the A/D converter to be accurate to 20 bits. Sample and hold circuits may be necessary to freeze the input signal during the measurement period since no averaging of that signal takes place. The slew rate of the input signal is, therefore, an important limitation of the accuracy of the successive approximation A/D converter.

In situations where high noise immunity and not high conversion speed is important, the integrating A/D converter (**Figure 2**) may be the ideal choice. Integrating converters operate by an indirect conversion method, and the output of such a converter represents the integral or average value of an input voltage over a fixed period of time. The dual-slope, or dual-ramp, configuration is the most popular integrating A/D converter; other variations exist, including the quad-slope converter which cancels offset and scale errors by two additional integration phases of digital subtraction.

Dual-slope conversion begins when the unknown input voltage is switched to the integrator input. Simultaneously, the counter initiates clock pulse counting up to overflow. At this point the control circuit switches the integrator to the negative reference voltage until the output returns to zero. Upon detection of the zero crossing by the comparator, the clock pulses stop. The counter output is then the converted digital signal which represents the ratio of the input voltage to the reference.

The accuracy of an integrating A/D converter is independent of the stability of the clock and integrating capacitor since each affects the up-slope and the down-ramp in equal proportions. Missing output codes will never exist since all outputs are generated by a clock and a counter. Counter resolution is the sole factor affecting differential nonlinearity.

The noise immunity of the integrating converter is due primarily to the rejection of unwanted high frequency noise by the input signal integration; changes in the signal that occur during the sampling period are also averaged by the integrating technique of conversion.

The disadvantage of this type of A/D converter is that integration is a slow con-

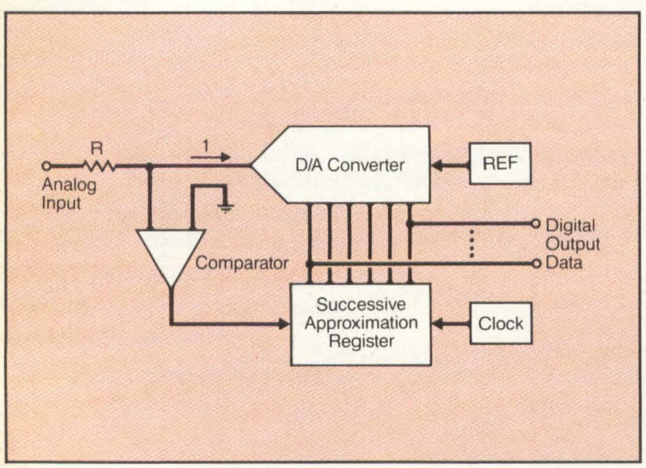


Figure 1: The successive approximation A/D converter is the most popular converter for moderate to high speed applications.

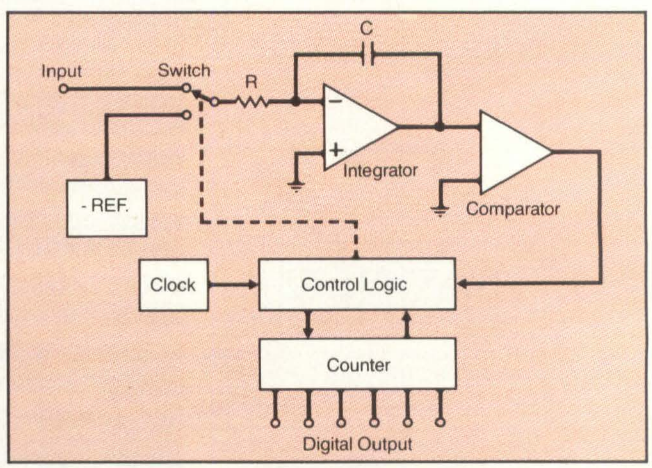


Figure 2: The dual slope A/D converter has excellent linearity characteristics and the ability to reject input noise.

version method, typically with 3 to 100 readings per second. In many applications, averaging the analog input signal over several milliseconds is unacceptable. Although a sample-hold circuit may be used to freeze the input, systems demanding short measurement windows usually require high speed conversions.

A two-stage series parallel A/D converter (**Figure 3**) operates on the principle of digitizing the quantization error between the D/A output and the analog signal input in successive approximation A/D converters. If the D/A converter has more accuracy than resolution, then the second digitization may extend the overall resolution of the A/D converter. In general, the development of the two-stage series parallel technique has helped to improve the speed, not the resolution of converters.

Such A/D converters make extensive use of parallel (flash) converters as the initial stage; the input must be digitized quickly, but with low resolution. The resulting digital output is passed to a low resolution, high accuracy D/A converter. The difference between the original analog input and the output from the D/A converter is as accurate as the D/A converter. That difference, or residue, is amplified and then digitized to extend the resolution of the converter.

Devices designed with this conversion technique are high speed, high resolution converters. However, the relatively expensive components – such as the flash converters – make the two-stage series parallel converter a tradeoff of speed for power, complexity and cost.

For many systems architects, conversion speed is vital. Some manufacturers, however, feel that the successive approximation conversion technique is beginning to reach its speed limit. Increasing the clock speeds to decrease the time intervals between trials may help. According to Bill Sheppard, Marketing Engineer at Analog Devices' Measurement and Control Division (Norwood, MA), customers would like to see 15- or 16-bit A/D converters with sampling speeds of around 5μsec, currently beyond the limit of successive approximation converters. Two-stage series parallel A/D converters may become the best way to attain such speeds.

The achievement of A/D converters with resolutions over 16 bits is likewise a problem for converter designers. Chuck Sabolis, Manager of Strategic Planning at Micro Networks (Worcester, MA) feels that most improvements in A/D converter design have been architectural in nature, not technical. Adjustments in the physical layouts of converters have helped to decrease interference between the analog and digital portion of the devices. The ability to laser trim thin film resistor ladders has solved the problem of resistor matching only up to a point.

For example, an 18-bit successive approximation A/D converter requires a D/A converter which cannot drift more than one-half LSB over time and the A/D converter's temperature range. If one-half LSB is approximately equal to 1.9 parts/million of full scale, resistor matching becomes almost an impossible task. Laser trimmed resistors, says Brian Conant, Marketing Manager, Data Products Division of Burr-Brown (Tucson, AZ), have helped to achieve converters of 14 bits; however, such trimming cannot be relied upon to maintain accuracy for 16 bits and beyond. Temperature stability is another problem.

One more potential stumbling block to the development of higher resolution A/D converters is comparator accuracy. An ideal comparator would have zero offset, infinite gain, infinite input impedance and a zero comparison time. Comparators for fast, high resolution A/D converters must have input noise levels significantly less than overdrive levels of one-half LSB. The same comparators must respond quickly to such overdrives. The greater the overdrive, the faster the response time. Obviously, high accuracy (high gain) and high speed are not parameters which are easily compatible.

Since the only devices which fit such requirements are of discrete design, modular and hybrid technologies have an advantage in the design of high resolution A/D converter design. In the past, data converters have been mostly discrete component devices, available in instrument cases and then modules. The modular design approach enables the combination of optimum components of all types.

For example, for very high levels of speed and precision, a high speed comparator may be combined with precision, high speed current switches utilizing low temperature coefficient resistors and a reference. Whole data acquisition subsystems are available in high performance modules.

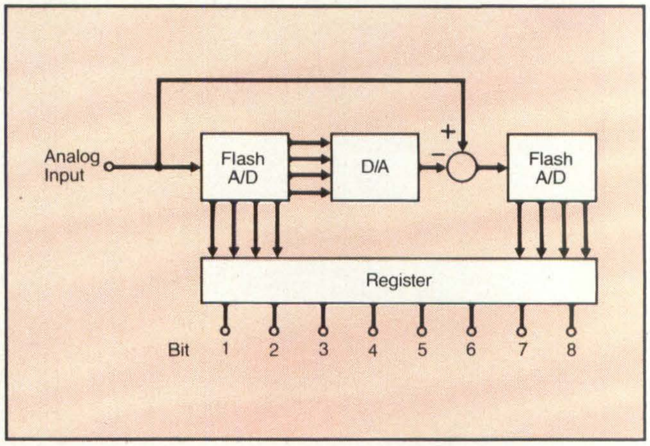


Figure 3: With high conversion speed in much demand by systems architects, the two-stage series parallel A/D converter is growing in popularity.

Although the design of hybrid converters is almost as flexible as that of modules, two limitations do exist. Not all of the semiconductor components needed for a high resolution hybrid A/D converter are readily available in monolithic form. To produce a feasible hybrid, the number of chips must be kept to a certain minimum.

Hybrid manufacturers cite the availability of low cost switches, monolithic successive approximation registers and laser trimmable thin film resistors as important developments in technology for reducing hybrid costs. Hybrid substrates are able to physically isolate the analog and the digital portions of the chip, reducing the transfer of analog and digital noise on the chip. A pretested, pretrimmed package can be of great use to a systems architect.

Some manufacturers of hybrids, after adding microprocessor interfaces to the converters, are predicting the integration of memory chips or buffers in order to store Fast Fourier Transform values; an intelligent A/D converter with multi-

(continued on p. 91)

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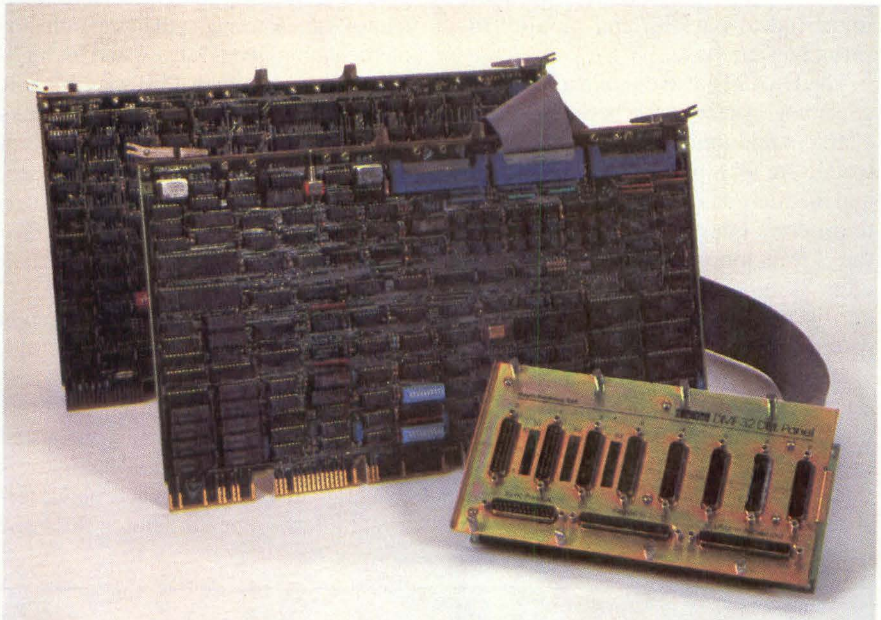
Systems Architect's Guide To The Q/Unibus



Digital Equipment Corp.'s DMF 32.

by Dave Wilson, Executive Editor

Offering enhancements or additional features not found on DEC products has always been the key to success in the DEC-compatible marketplace. However, in many cases, third party vendors cannot lead the technology but are restricted to a "wait-and-see" approach before building products. Often designing to meet the DEC specification is a difficult enough task, as is bringing other features to the OEM. Nowhere is this more evident than in the disk and tape arena (*Digital Design*, October 1984, p. 67). The Digital Storage Architecture (DSA) and the Mass Storage Control Protocol (MSCP) have taken many third party suppliers a great deal of time to work around. Inevitably, the larger suppliers (such as Emulex) were first to market with such products, but it has only been very recently that the smaller houses have introduced products to conform to the architecture.

DEC's first product that brought the Digital Storage Architecture and the Mass Storage Control Protocol down to the Q-Bus was the RQDX-1, which received poor acceptance in the marketplace and left the door open for third party introductions. Recently, two new Q-Bus dual height controllers that claim to be compatible with the MSCP have been announced from Andromeda Systems (Canoga Park, CA) and Webster Computer Corp. (Sunnyvale, CA).

Whereas DEC's RQDX-1 controller permitted two RD51 or RD52 Winchester drives, one RX50 floppy drive, or both to be hooked to a Q-Bus system, the UDC11 from Andromeda can control up to four Winchesters, cartridge and floppy drives. Operating under the MSCP, the UDC11 permits the use of ST506 interface disk drives of any manufacturer or capacity. Though the Webster card allows only one 5¼" drive to be connected to each controller, up to three controllers may coexist in one system. Undoubtedly, DEC is committed to supporting both the Q-Bus and the Unibus in the long term. The Q-Bus-based MicroVAX-1 and the new MicroVAX-2 are undoubtedly only stepping stones to placing the VAX architecture on the higher performance VBI bus (to be announced this year). New announcements continue to be made from both the systems and the OEM board division of DEC in support of the older bus structures.

Many of the leading vendors of disk and tape controller products also offer a wide range of communications multiplexers for both the Q-Bus and Unibus. Like the disk and tape arena, these products usually offer enhancements and additional capability to emulate a number of DEC products. Early DEC products were characterized by a limited number of asynchronous lines and by Programmed I/O. Later versions were able to automatically select one of two methods to transfer data from the host to multiple terminals. They include buffered Programmed Input/Output (PIO) and Direct Memory Access (DMA). PIO transfers are more efficient for short burst transmissions, but tie up the computer for longer data relays. By offering DMA transfers for longer relays, the controller is able to access main memory directly. The size of the FIFO buffers on early boards was also small. FIFO buffers are important when a large amount of data is being input during peak periods.

By implication, the larger the FIFO, the greater the amount of data that can be handled at one time and the greater the system throughput. The majority of vendors producing DEC-compatible controllers increased the size of the FIFO capacity as a standard or selectable feature.

Until now there have only been a few approaches to providing multiple terminal connections to a system. Each of these approaches has advantages and disadvantages. One approach is to provide 8 or 16 channels on-board that must plug directly into the CPU bus. This requires many board slots for a multiple terminal system and all terminals clustered around the CPU.

Typical of the early DEC offerings was the DZ11, an asynchronous multiplexer that provided an interface between a PDP-11 processor and eight asynchronous lines. Each module provided for eight asynchronous lines; but since each module interfaced to these channels with a 16-line passive distribution panel, 2 DZ11 modules could be used with one panel. Two versions of the DZ11 (EIA or 20 mA) consisted of different module and panel types, allowing the user to mix EIA and 20 mA by using multiple DZ11s.

For higher performance than the DZ11, DEC introduced the DH11 series. The unit included PIO for input operations but used DMA for output transmissions to reduce the load on the CPU. Although it was possible to do 16-bit word transfers, the multiplexer was not capable of processing these transfers, handling them one byte at a time. The DH11 slowed throughput operations by transferring each DMA word twice in order to process both bytes in the word.

As many as 16 DH11s may be placed on a single PDP-11 processor to create a total of 256 lines. **Figure 1** shows a typical system implementation. Since DEC does not offer a Q-Bus version of the DH11, several vendors jumped in to fill the gap that was open and many products are currently available to the OEM ranging from look-alikes to products with enhanced features.

The disadvantage of having to add several multiplexer boards into a single cabinet space was solved by an approach that allowed the board to interface to an active distribution panel. Emulex, for example, provides for its DH11-compatible controller to interface to a distribution panel that contains up to two eight-

Data communications products offer the systems integrator a wide variety of options to choose from.

channel line card adapters and an integral power supply (**Figure 2**). The line adapters provide the data and modem interface circuitry plus USARTs that allow for serial-to-parallel and parallel-to-serial conversions.

The USARTs also contain a baud rate generator. Data transfers between the line adapters and the communications controller are on a parallel character basis and the line adapters may be configured to different interface standards (such as the current loop). Channels can be added in 8- rather than 16-line increments, and the type of interface can be changed, mixed and matched as needed.

If more than 64 lines are needed, only one additional standalone board must be placed on the bus to handle a second group of 64 lines. The disadvantages of this approach are that it requires expensive active distribution panels and the panels end up clustering into one or two adjoining cabinets.

Providing a multifunction board often gives the systems integrator additional features at a lower cost than separate implementations would. Designed for higher performance than DZ11s on VAX-11 series machines, DEC's DMF 32 breaks down into three major components: an 8-line asynchronous terminal interface, a synchronous port and a parallel port. The asynchronous terminal interface portion of the controller supports a feature unavailable on most other DEC multiplexers, automatic internal selection of buffered programmed I/O or DMA output of characters. Recognizing the value of this feature, some manufacturers chose to eliminate the synchronous and parallel ports and to provide multiplexers that emulate only the asynchronous terminal interface portion but at the same

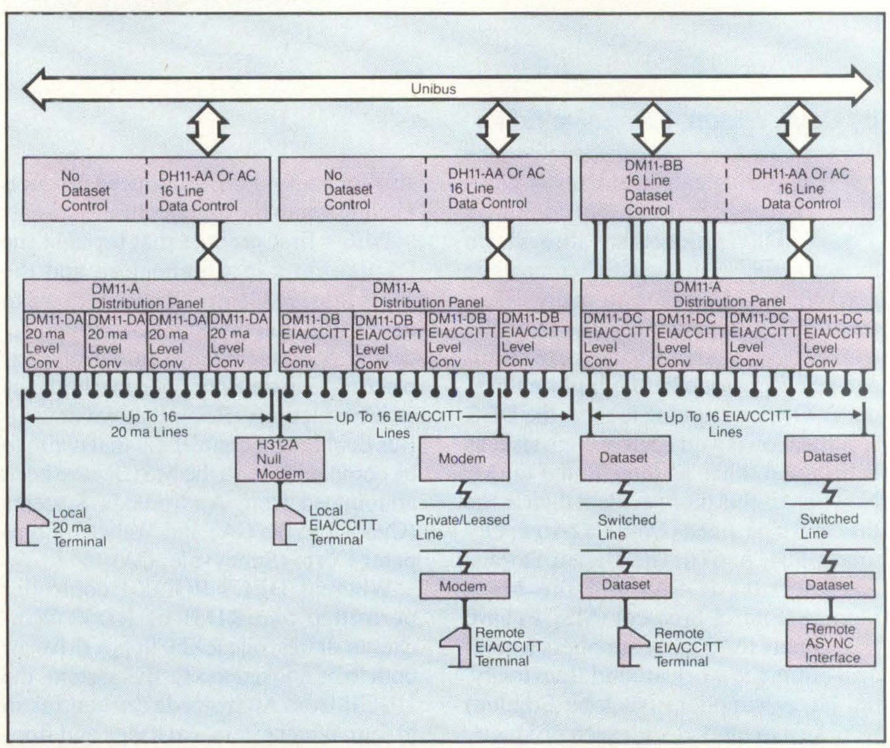
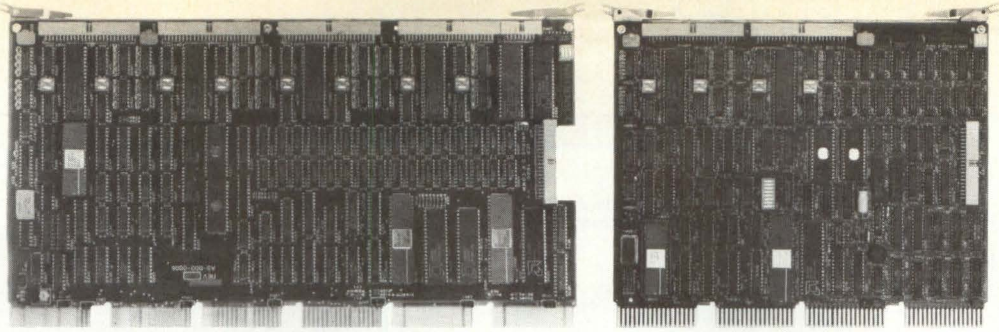


Figure 1: Typical system implementation using the DH11.



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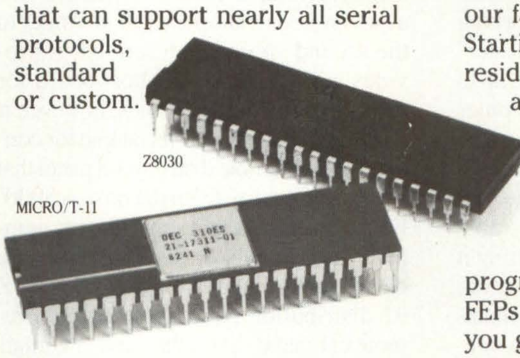

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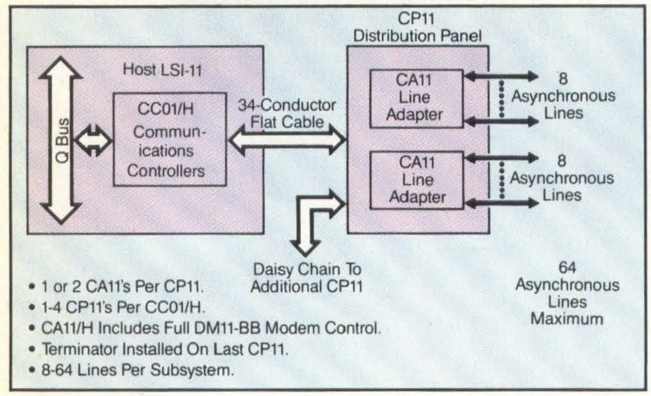

Figure 2: The Emulex DH11-compatible board interfaces to an active distribution panel.

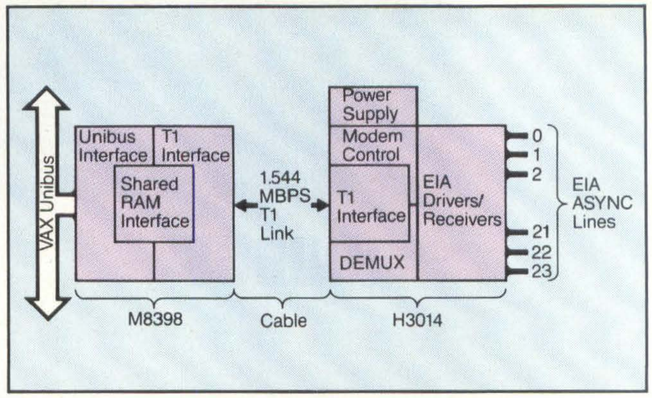

Figure 3: DEC's DMZ 32 consists of a Unibus Interface Module and a remote distribution panel.

time allowing for a large number of lines to be supported.

In their emulation of the DMF 32, MDB Systems chose to also provide a unique alternative to the conventional methods of interfacing to the host. The MDB approach for a multiterminal system is a single host board connected directly to the CPU bus that generates a 1000' bus which allows up to 16 separate attachment points for terminal clusters anywhere along its entire length supporting up to 128 terminals in total. Up to 32 terminals may be connected through a single card. This requires a single system slot to provide power and connector panel that can be mounted in the rear panel of the DEC Micro-11 or similar boxes. The system is comprised of a microprocessor board, one or more asynchronous channel boards and a connector panel for each channel board.

The microprocessor board plugs into the system bus and generates the Parallel Bus Interconnect (PBI) signals over a dual 34-pin cable that connects as many as 16 slave boards over 1000'. The slave board developed for the PBI controls 32 asynchronous channels. It can be plugged into a Q-Bus slot anywhere in a system and only requires power. A connector panel is for each CRT terminal and converts a flat ribbon cable from the 32 channel board to 32-DIN connectors.

Traditionally, users have been limited when it comes to satisfying both remote and local communications requirements for a single host minicomputer system. Traditional remote communications provided no means for the multiplexing of data. Each remote terminal line consequently required an attendant pair of dedicated modems, its own distribution panel port and its own dial up or leased telephone line. The primary advantage of this method is that no changes to the resident software are required. However, the redundant hardware, cabling and line-usage costs of this method are unnecessarily severe for any application involving a number of terminals.

An alternative is to use master/slave data concentrators to eliminate redundant telephone lines and modem costs. Here, one data concentrator unit operates at each end of a transmission line. Working with a multiline controller, the "master" concentrator multiplexes data from up to 16 physical ports at the host computer site, sending it across a single line to the "slave" concentrator at the remote site. The slave is configured and instructed by the master and demultiplexes the transmitted data, dividing and transmitting it to a number of terminals. In this method, the relationship between parts (communications interfaces) and terminals is one-to-one. In addition to eliminating redundant line and modem costs, all communication protocol and any error correction procedures used between the concentrators are embedded in the controller, the concentrator firmware or both; no changes to the resident software are necessary.

Although this system does significantly reduce hardware requirements/costs, each channel still requires one distribution panel port at the computer interface. Adding port concentration at the computer site to the master/slave data concentration method allows the multiplexing/demultiplexing of up to 256 remote and local lines to be handled by a single controller board. Multiplexed data from up to 16 channels passes through a single asynchronous RS-232-C port to a port concentrator. The port concentrator aids the controller in its multiplexing tasks and establishes and maintains the link with the remote concentrator and buffers data during peak loading periods.

The latest approach to providing a communications controller that can work in both a local or remote location has been announced by DEC in the form of the DMZ 32, a Unibus-based 24-line asynchronous multiplexer. It is similar to the second approach described. It provides a bit-sliced-based host board for connection into the CPU bus, however, it generates a high speed serial line for connection to a remote distribution panel that can be as far away from the host as 5000'. For VAX systems that support large numbers of terminals or VAX systems in a cluster environment, placing the DMZ 32 distribution panel in a common remote cabinet reduces the need of Unibus expander cabinets for each system.

The DMZ 32 system consists of two components: the Unibus Interface Module with shared RAM and T1 interface and the Remote Distribution Panel. The T1 interface controls all data going on and off the high speed (1.544 Mbit/sec) T1 trunk (**Figure 3**).

The second component of the DMZ 32 asynchonous multiplexer is the remote distribution panel. The active panel is responsible for coordinating all data transfers between any of the 24 asynchonous lines and the T1 trunk. The panel decodes the incoming T1 formatted serial data. In the reverse direction, it places outgoing asynchonous terminal data and modem control signals into the T1 serial bit stream, using bipolar encoding techniques.

The disadvantage of this system is that it only supports one distribution panel, or with additional hardware, two. In actual practice, although the terminals can be remoted farther from the CPU, the terminals must all cluster around one or two distribution panels for the entire multiterminal system.

Unlike the disk and tape arena, implementing a solution to link a single mini to many different terminals presents the systems architect with a variety of alternatives, compounded by the fact that the location of the terminals are in a local or remote site or a mixture of the two.

The opportunities for third parties to provide alternatives to existing DEC products is assisted by the fact that to provide compatibility between its future generation and previous generation products, DEC has retained older bus structures such as the Q-Bus and Unibus, often increasing system performance by employing coprocessing techniques to offloading bus traffic. The VAX line, for example, recently boosted by the announcement of the VAX 8600, retained the Unibus as a method of supporting I/O, gaining its speed improvement through the use of custom ECL. Likewise, the latest in the PDP-11 minicomputer family, the PDP-11/84, retains the use of the Unibus, but gains its speed over older models through the use of a private memory bus across the CD interconnect slots on the Unibus as well as through an 8 Kbyte direct-mapped cache.

Many of the vendors of Q-Bus products currently promote the fact that their boards will work with the LSI-11 range of machines as well as with the MicroVAX-1 product that DEC currently offers. In reality, however, the MicroVAX-1 as a Q-Bus-based machine runs under a different operating system (MicroVMS) than the LSI-11 line. Since MicroVMS has only been available since October 1984, it will take some time before third party vendors can produce products to meet the specifications. DD

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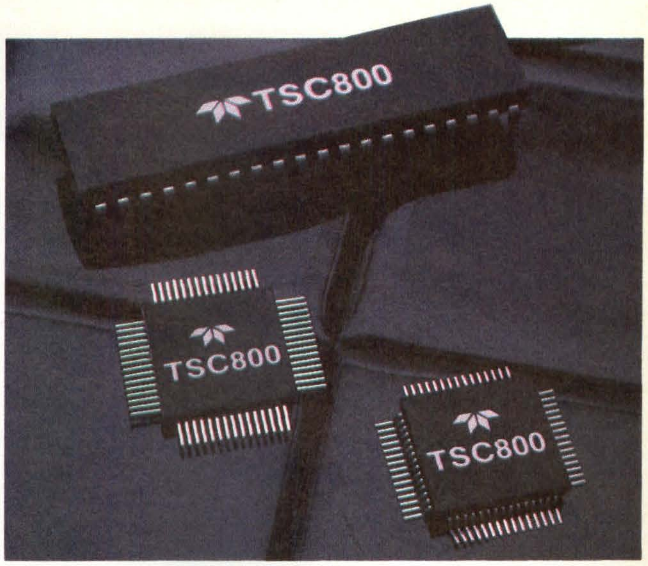
(continued from p. 78)



The TSC800 from Teledyne (Mountain View, CA) is a 15-bit plus sign integrating A/D converter designed for microprocessor interface.

pliers, accumulators and a dedicated microprocessor to perform digital signal processing calculations is possible. Designers are discussing on-chip EPROMs as a way to improve error correction techniques. Network protocols and communication processors, also on the digital portion of the A/D converter, may appear. Sample and hold circuits, presently available on the front end, may be joined by optional programmable gain amplifiers to increase dynamic range.

Monolithic A/D converters are generally a step behind modular and hybrid units in performance due to inherent design limitations. The prevention of noise interference between the digital and analog parts presents a greater challenge for designers of such devices. In addition, these converters usually require various external components for proper operation – although their lower prices may compensate for the added cost of additional components.

Single chip converters have been manufactured in both CMOS and bipolar technologies. In the past, bipolar components have proved to be better linear devices, whereas CMOS components were considered to be logic oriented. Better switches and input devices are being developed with the improvements in MOS technology and, as a result, CMOS has become a viable processing method for high resolution A/D converters, due to reasons other than low power dissipation.

Several manufacturers feel that a mixed technology may provide the ideal solution for monolithic converters by combining the best features of MOS and bipolar. Most important, bimos allows the wide analog voltage range required by high resolution converters. Leakage currents are also low. Analog Devices has two separate divisions working on such manufacturing methods, the Semiconductor Division (Wilmington, MA) from a bipolar to CMOS direction and the Microsystems Division (Limerick, Ireland) from a CMOS to bipolar angle. Other companies are working on merging the two technologies as well.

Finally, the search for high resolution A/D converters of 18 bits and more continues. Modular and hybrid manufacturers seem to have the advantage in developing such devices; however, the physics of noise may affect their attempts as it already has seemed to affect monolithic manufacturers. Systems architects may find themselves having to make more serious choices between resolution and accuracy, especially since few 16-bit converters can offer full 16-bit linearity now. Differential linearity specs may become more controversial due to difficulties in testing high resolution A/D converters. If successive approximation, integrating and two-stage conversion methods are reaching limits, the time may have come when the only possible way to achieve accurate, higher resolution converters will be to invent a new sampling algorithm or a very innovative architectural approach. DD

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A Risky New Architecture For The Future?

by Gregory MacNicol, West Coast Technical Editor

As the race for higher speed in computers continues, new alternatives are proposed promising better price/performance. One of these new architectures that is gaining momentum, press and venture capital is RISC – Reduced Instruction Set Computers.

The departure from conventional Complex Instruction Set Computers, or CISC, is based around several fundamental problems facing modern computer architects. High computational speed means higher cost. More importantly, a computer should be designed for greater efficiency in program generation through a supportive operating system and higher level languages. Computer architecture resolves the division of labor between hardware and software. Thus, microcomputer manufacturers provide a rich set of commands on chip that allow software designers to build operating systems, languages and hardware specific programs. An example is the iAPX 432 from Intel which was intended to directly support the Ada language. Enhancements added to CISC systems to increase performance have been floating point processors, array processors, memory management units, cache memory and multiple buses. The alternative to such complexity is to use RISC-based architectures.

The RISC concept is not new. Seymore Cray, of Cray Research, has been a leading proponent of reduced instruction sets for the last 20 years. Considered an academic path of computer science, RISC remained in the research labs of universities and large corporations until recently. The most notable of the RISC researchers is David Patterson, who first coined the term, from the University of California at Berkeley.

What Is RISC?

The foundations of reduced instruction set computers are based on three primary attributes:

- The instruction set is minimized to execute only the most used instructions.
- Each instruction is executed in one machine cycle.
- Memory is accessed only by load/store instructions, where as all other instructions operate between registers.

RISC derives from the analysis of computer program execution. Tracing instructions in programs indicated that load, store, branch and integer add accounted for most of the execution time. In addition, accessing data in registers is much faster than accessing data in memory. This means that the more data that can be kept in registers, the faster a program will run. Part of RISC implementation, thus, includes large register files, overlapping register windows and a simple pipelined data path. Instructions also have fixed length with a small variety of formats. The single cycle instructions allow a simplified architecture which, in turn, leads to streamlined organization. The overhead in each instruction can be reduced, allowing a shorter clock cycle time. Ultimately, all of this results in a smaller, much faster and less expensive computer.

There are several reasons why this architecture is becoming attractive, after being overlooked in the past. Microprocessors evolved from mainframes with operating systems written in assembly language. Attempting to facilitate operating system design with VLSI, chip designers offered functions that made software development easier. Now that higher level languages are being used to write operating systems, it is possible to use a small but effective instruction set in combination with an optimized compiler and omit the secondary process of assembly interpretation. Another major reason for RISC's current implementation is the present state of VLSI. Due to the small instruction set, the chip's die size and gate count is also smaller which provides a better cost/speed ratio. The alternative has previously been to use expensive ECL for cache memory. The small size not only allows better bus utilization for passing of operands, but also faster clock rate and execution speed due to fewer interchip paths.

The reduced instruction set is only a small aspect of RISC architecture. An important part of the concept is a truly optimized and integrated compiler. This supports the concept of shifting complexity from the hardware to software. Better

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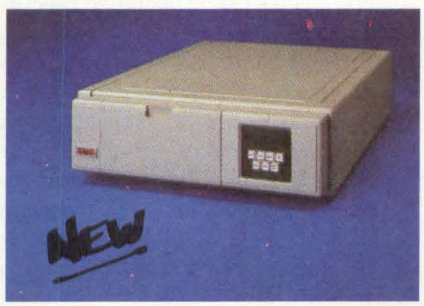

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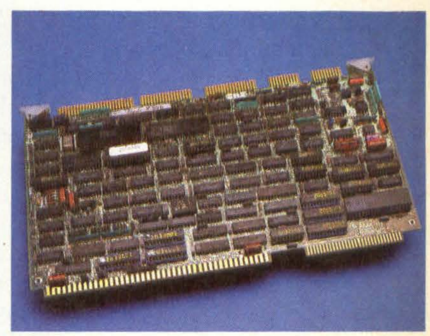

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The Reduced Instruction Set Computer architecture is touted as being a replacement for everything from microprocessors to VAXs. Are these claims valid?

algorithms are available for compilers optimizing the theory and use of register handling. The advantage of these compilers is that changes can be made in the future. RISC is based on a memory hierarchy from cache memory to registers to main memory. The organization of the architecture is critical for proper implementation.

The concept of the reduced instruction set was developed by several independent researchers. For example, at IBM, where work was done on the new IBM 370, it was realized that a sequence of load instructions is faster than a load-multiple instruction for fewer than four registers, which accounts for over 40% of these instructions in typical programs. Another example was at DEC where the INDEX instruction on the 11-780 was replaced with several low level instructions. The result was an increase in speed of 45%. If the compiler took advantage of the set of low level instructions, the program ran 60% faster. The lesson learned is that bigger instructions don't necessarily mean faster execution.

A serious attempt at a minicomputer RISC goes back to IBM's 801 project, 10 years ago. Trace tapes which followed the path and frequency of execution of computer instructions indicated that relatively simple instructions such as STORE, LOAD, ADD and SUBtract were used more frequently than complex instructions. Several implementations of RISC have been researched at IBM and the research continues. Reports indicate that an in-house system works at 10 MIPS (million instructions per second), which compared to the 370/168's 2.4 MIPS, is quite impressive.

What IBM is facing is common to other major computer manufacturers. If they make a computer that is faster but not compatible with their present computers, languages and operating systems, it could affect the sales of their mainline systems. The ability of a computer manufacturer to stay in business does not depend on the speed of the computers but on upward compatibility, service, support and total functionality. It is no surprise that large computer manufacturers have not been tempted to build systems based on a technology that is not compatible with their present line.

The academic world has been the leading force in RISC. The result of the Berkeley RISC project, which David Patterson led after a leave of absence from DEC, was a 32-bit NMOS RISC chip. Patterson realized that building a computer like a VAX on a chip would include difficulties, such as a writable control store. So, he chose to depart from the current 16-bit approach of mimicking a PDP-11 to implement RISC architecture.

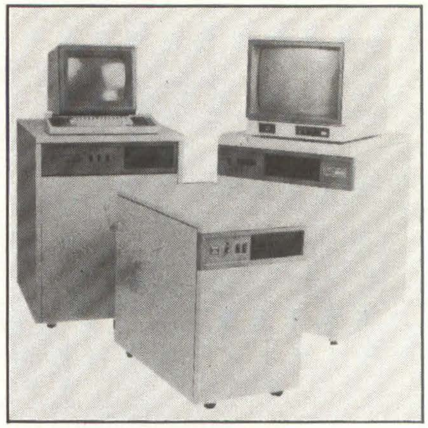

Figure 1: The Ridge 32S from Ridge Computers is a 32-bit, single-user workstation capable of executing up to 8 MIPS.

The result was a 39 opcode chip that can support 8-, 16-, and 32-bit data and 32-bit addresses. The NMOS chip uses 41,000 transistors, was fabricated using 1.5-micron geometry, and runs at a clock cycle of 330 nsec. Floating point arithmetic is intended to be calculated externally.

One problem often encountered in programs is the handling of temporary data from several origins. The Berkeley group solved this problem by using several sets of registers, called register windows, to ensure local variables are kept in registers until needed. This method of register switching is faster than placing the variables in memory and returning them back to the registers. Overlapping register windows further increase efficiency by automatically passing variables. Register design is essential to RISC architecture because RISC creates more procedure calls than CISC.

At Berkeley, there is a project that may potentially test the overall power of RISC. SOAR, Smalltalk on RISC, is a MOS chip under development sponsored by DARPA. (DARPA is also funding a LISP chip at TI.) Smalltalk-80 is an AI language with object-oriented storage man-

Table 1: UNIX C compile-time benchmarks.

Compiled Program		VAX 11/780 C Compiler					RISC C Compiler				
					VAX/RISC					VAX/RISC	
name	size (lines)	on VAX (secs)	on RISC 8MHz	on RISC 12MHz	8	12	on VAX (secs)	on RISC 8MHz	on RISC 12MHz	8	12
ld.c	1587	27.9	21.0	13.9	1.3	2.0	35.2	22.4	14.8	1.6	2.4
sort.c	873	17.4	13.2	8.7	1.3	2.0	20.0	13.2	8.7	1.5	2.3
puzzle.c	118	5.2	3.6	2.4	1.4	2.2	7.3	4.8	3.2	1.5	2.3
Total	2578	50.5	37.8	25.0	1.3	2.0	62.5	40.4	26.7	1.5	2.3

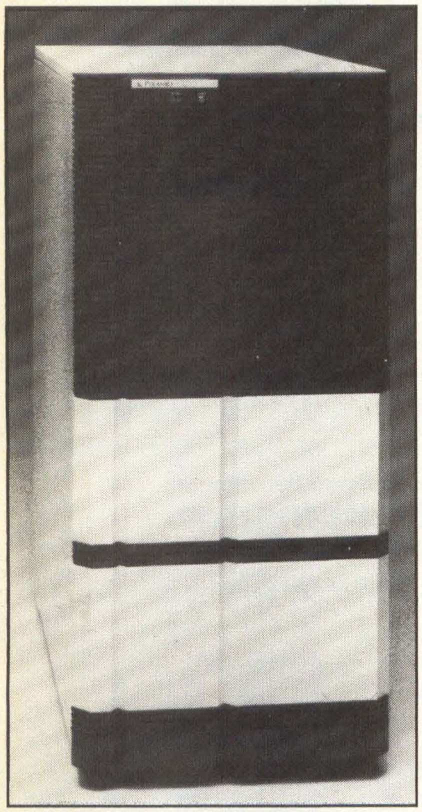

Figure 2: The Pyramid 90X is a 32-bit, virtual memory computer with memory from 1 to 80 Mbytes.

agement and operates like a stack-oriented virtual machine. The usefulness of Smalltalk is overshadowed by problems that make almost all implementations slow. Smalltalk has no type declarations, resulting in variables to be discovered during run time. There are more procedure calls than in other languages because of its object-oriented storage and high overhead. Despite Smalltalk's inherent difficulties, the prototype chip compares favorably with Xerox's Dorado, an ECL minicomputer. Results indicate that procedures such as call/return are about four times faster on the Dorado, eight times faster on a 68000 and 30 times faster on a VAX 11/780. Some of SOAR's speed is partially due to overlapping register windows, zero delay in initializing local variables and a cache that holds the results of destination addresses.

At Stanford University, the Center for Integrated Systems is also conducting RISC research. The primary difference is that Stanford has been implementing in software what the Berkeley group is exploring in VLSI. Led by John Hennessay, Stanford has been designing an architecture called Microprocessor without Interlocked Pipe Stages (MIPS). The basic philosophy is the design of a compiler-driven instruction set that provides little or no decoding due to close correspondence with the microcode. Instead of using hardware on the chip for registers, MIPS uses sophisticated compiler theory for an ideal of zero idle time in the pipeline. Although the processor is pipelined, there is no pipeline interlock hardware because it will be implemented in software.

The MIPS compiler consists of several closely integrated parts. A pipeline organizer sets up the sequence of commands through instruction packing. An instruction scheduler and branch scheduler further optimize the process. The MIPS architecture can pack two instructions per 32-bit word. Two operands per word and two cycles per instruction make one operation per machine cycle. The result is a processor that is six times faster than a 68000 running at 8 MHz.

Criticism

Despite its great promises, RISC is criticized by microprocessor or CISC supporters. A group led by Robert Cowell at Carnegie-Mellon University is objectively evaluating both sides of the issue. The results are not clear and raise further questions. The problem is that no one has been able to prove whether multiple register sets or reduced instruction sets are more important for RISC performance. Both architectures use different compiler technologies, virtual memory techniques and operating system overheads, making comparison complicated. The object-oriented architecture which minimizes the programming errors and multiprocessing features are not designed for rapid execution. The group is continuing its efforts, however, to evaluate more accurately the differences between the two architectures.

Another issue concerns the use of the register window scheme. The window register scheme is important to RISC because RISC designs create more procedure calls than CISC, which handles complex instructions as opcodes. The problem exists in the nesting of procedures. If the depth is large enough, an additional stack is created in memory. Depending on the frequency of register overflows and underflows, the physical registers may not be visible to the machine language programmer at any given time. The Berkeley group has developed a sophisticated scheme using overlapped register windows. The result is 2 μsecs for a typical call, compared to 20 μsecs with the VAX 11/780. However, some critics believe the success of the Berkeley project was due to the register architecture rather than the RISC implementation. The Berkeley group responded by pointing out that the critics have ignored a critical point in RISC design. The decrease in complexity in control logic area on a chip that supports complex instructions is an important factor that allows more space for the large number of registers.

An important feature found on most 32-bit computers, but not on the Berkeley RISC system, is virtual memory. An early attempt at incorporating this feature with a memory management chip that translated virtual memory to physical memory actually slowed performance 25%. One solution is the use of faster 256K RAMs or a cache similar to those

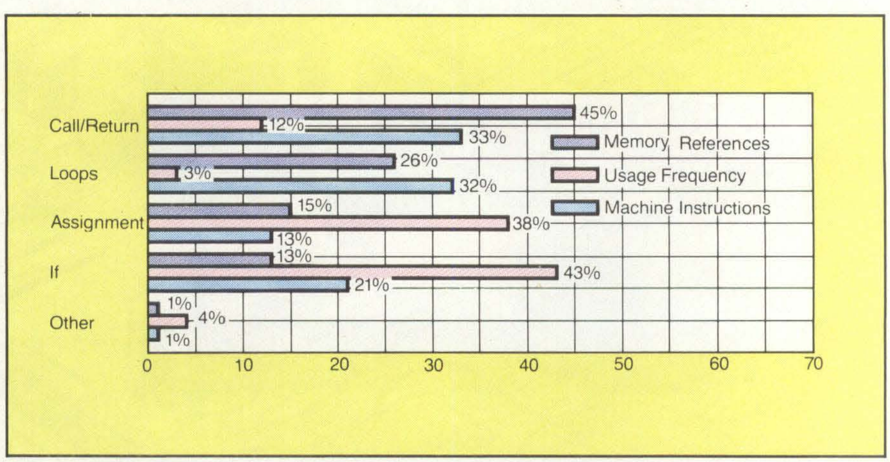

Figure 3: Statement usage in typical C programs on a traditional architecture.

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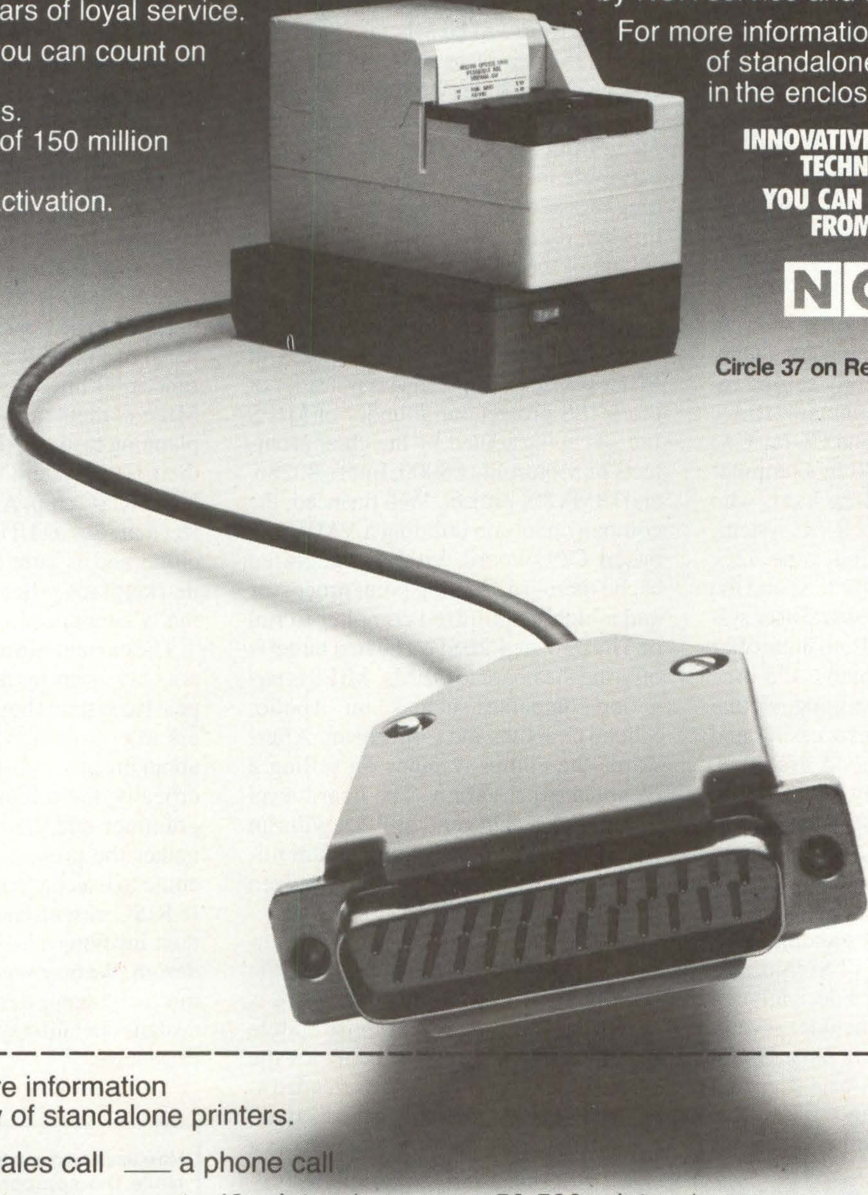

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Benchmarks are truly unfair judges for new computers and languages. Although it is fair to say that RISC machines are faster than conventional computers, other qualities make the judging process more complicated. The Ridge, for example, is intended for only a few users, while the Pyramid is designed for a multiuser capacity of over a hundred. Additionally, one of the important components of a RISC-based computer is the compiler, which is a technology in itself. Regardless, several in-house and independent groups have made extensive evaluations using C programs, such as Id.c, sort.c, and puzzel.c. Solving complex linear equations in full precision indicates very positive results using RISC architecture. One group, Argonne National Laboratory, tested and published the performance times of over 150 computers with different compilers.

RISC Takers

There are several manufacturers who are developing RISC-based computers. Only two companies are presently selling reduced instruction set computers; Ridge and Pyramid. Ridge (Santa Clara, CA) was founded in May 1980 by computer designers, from Hewlett-Packard, who were already working on a RISC system. The Ridge 32 series includes the 32C, providing multiuser capabilities; and the 32S (**Figure 1**), a smaller single user system designed for OEMs. Both units offer 32-bit data and address paths, 125 nsec cycle time, four stage pipelining, virtual memory, floating point processing and high resolution bit-mapped graphics. Variations of the Berkeley RISC design were implemented to satisfy market needs. These include fast context switching supported by hardware to allow many I/O devices, users and processes. In addition, the Ridge 32 uses standard TTL instead of a single custom VLSI chip. The operating system is ROS, a derivative of UNIX V and 4.2BSD. It includes several capabilities not included in most UNIX implementations such as paged virtual memory, a high performance file system and a fast message-oriented interprocess communication system.

A unique quality of the Ridge 32 is the bit-mapped graphics support. A 19″ color display has 1024×768 pixel resolution with eight planes, at a 33 Hz refresh rate. The controller board has its own 128K of memory for graphics, which allows refreshing the display 60 frames per second, similar to the way memory is paged in and out from a disk. Additionally, ROS has a multiwindow, screen-oriented editor for efficient graphics interfacing.

The focus of Pyramid Technology (Mountain View, CA) differs from other RISC developments because they seek to match the needs of minicomputer users who want large multiuser capabilities with UNIX. As a result, neither Ridge nor Pyramid sees the other as a competitor. The Pyramid 90X (**Figure 2**) is a 32-bit, virtual memory computer with memory from 1 to 80 Mbytes. The CPU has a 125 nsec cycle time, fits on three boards and includes a 68000 for system support and diagnostics. Deviations were made from the RISC criteria, such as a two-cycle instruction time, but overlapping register sets and parameter passing through register windows is supported.

One of the more ambitious efforts to commercialize RISC took place in August with the incorporation of MIPS (Mountain View, CA) from the Stanford MIPS project. John Hennessay, leader of the MIPS project and founder of MIPS Inc., is being joined by the chief architects of Motorola's 68000, Intel's 80286, and IBM's 801 project. Well financed, the company plans on building a VME bus-based CPU board with an integrated cache memory, floating point processor and a highly optimized compiler to run on UNIX V or 4.2BSD. The first target is offering the board to OEMs. MIPS is targeting companies such as Sun, Apollo, Silicon Graphics and Convergent. Afterward, the company plans on selling a complete workstation. The board level product, due at the end of 1985, will run five to ten times faster than standard microprocessors because of the optimized compilers.

NCR (Dayton, OH) is the first company to offer a RISC-based board on the Multibus I. The NCR/32-796A board is a 32-bit wide system that must double buffer the input and output data for the 24-bit Multibus. The board is intended to be installed on an NCR 3200-based development system and can either act as a coprocessor or emulate a computationally intensive processor. The instruction cycle is 150 nsec which translates to executing 6.5 MIPS. NCR plans to make the board available for 32-bit buses.

The unannounced proprietary work on RISC being done at several large companies will undoubtedly change the course of commercial RISC. IBM's 801 project may be announced, possibly, as a CAE system running on VM. According to rumors, IBM has two RISC projects, both called ROMP. One is probably an experiment because of its incompatibility with IBM's present line. The other project, being researched in Austin, TX, is said to be a part of IBM's effort to develop an advanced workstation. DEC is also involved with two projects. The first is thought to be a high-end ECL computer that performs at 10 MIPS. Forest Baskett, from the Stanford RISC project, is leading the project at the company's Los Altos facility. A 2 MIPS system is the other project. It is aimed at the engineering workstation market and would have the ability to run some of the software of the VAX series, but would not be upwardly compatible. Hewlett-Packard's work continues, despite the fact that they dropped RISC years ago. They are believed to be working on two RISC projects, one of which is to replace the current 3000 line. It is to be a 64-bit, 5-6 MIPS computer. Hewlett-Packard is also planning to use a RISC-based system for their CAE system which will include a VLSI RISC chip. AT&T's new RISC project that runs on UNIX is called the C machine and is sure to change the RISC marketplace when the product is formally announced.

The current wave of RISC architecture not only promises faster, smaller, less expensive systems but also requires designers to consider more global questions about the process of programming. Specifically, the role of the computer, programmer and the human interface that makes the process of instructing a machine to execute complex chores easier. If RISC researchers are correct about their invoking a major trend in computer design, we may see profound changes in microcomputer design, VLSI, compiler design, operating systems and computers in general. **DD**

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Using The Signetics 8X41 In Bus Repeater And Bus Switching Applications

by L. A. Lehmann, DigiRad Corp., Palo Alto, CA and Mike Ashtiani, Applications Engineer, Bipolar LSI Division, Signetics Corp., Sunnyvale, CA

Information processing systems are increasingly being limited by the channel rates of the bus or buses that interconnect system components. High speed disk memories, image storage and processing, and multiprocessor systems are examples of computer environments which can overtax the conventional single bus, sequential operation structure.

Conventional single backplane bus structures, on which all machine cycles take place and for which the various masters compete, lack flexibility. The systems designer must design the backplane (and power supply) to accommodate a worst case population of boards. Exceeding these design parameters creates an awkward situation, typically requiring use of repeaters. The repeater itself is frequently a design problem since many bus signals are bidirectional. While signal regeneration and amplification are desirable, there may be no easy way to determine the direction of signal propagation for the control of repeater transceivers.

The Signetics 8X41 auto-directional bus transceiver contains eight channels of bidirectional receiver/drivers and, for each channel, a simple asynchronous state machine to control signal direction. No external direction controls are necessary, but there are provisions for disabling one or both driven directions. This feature allows a very simple, fast and elegant bus switching architecture. (The part should not be enabled for driving into an established low level signal once the 8X41 has been disabled. An inherent race condition can cause the internal state machine to err in its determination of signal direction.) The 8X41 is fully TTL-compatible, with low (less than 100 μA) input current and with open collector outputs capable of sinking 70 mA. Propagation delay is less than 30 nsec.

Perhaps the simplest use of the 8X41 is an uncontrolled bus repeater (**Figure 1**). This structure is applicable to a wide range of bus types. **Figure 1b** shows the termination details for one channel of the repeater. In practice, the length of the repeater cable is often limited by its RC charging time. The designer should be fully aware of allowable skew and additional propagation delay. Many modern buses are very tolerant of additional delays since they are asynchronous and perform a full control signal handshake with every data exchange.

Bus-switched applications include systems in which data transfers occur simultaneously and asynchronously on multiple buses. Simultaneous CPU and disk controller transfers, for example, result in high data transfer throughput. Typically, a master within one bus environment will occasionally wish to communicate with resources on another bus. At these times, the buses are connected so that they are logical extensions of one another. After an interval, the buses are detached again so that they can continue independently.

Bus switching is an alternative for configurations in which the separate buses communicate by some slower form of networked I/O (i.e., by RS-232 or Ethernet). When data exchange rates are high, when the component systems are in close proximity (generally within the same rack or enclosure), and when a general purpose CPU in each component system would be an unnecessary hardware and software expense, bus switching is preferred.

The bus switching described here is also an alternative to another more popular form, in which multiple masters own local resources on their board and rarely request the off-board bus for transfers to a slave which is a joint resource. This form is adequate for many multiprocessing applications, but it is imperative that each master confine most of its accesses to on-board resources; otherwise, the system bus remains a bottleneck for data transfers.

Bus switchers can be subdivided into two broad categories: those in which a master must explicitly request connection or disconnection by writing to a control port (reminiscent of the way many

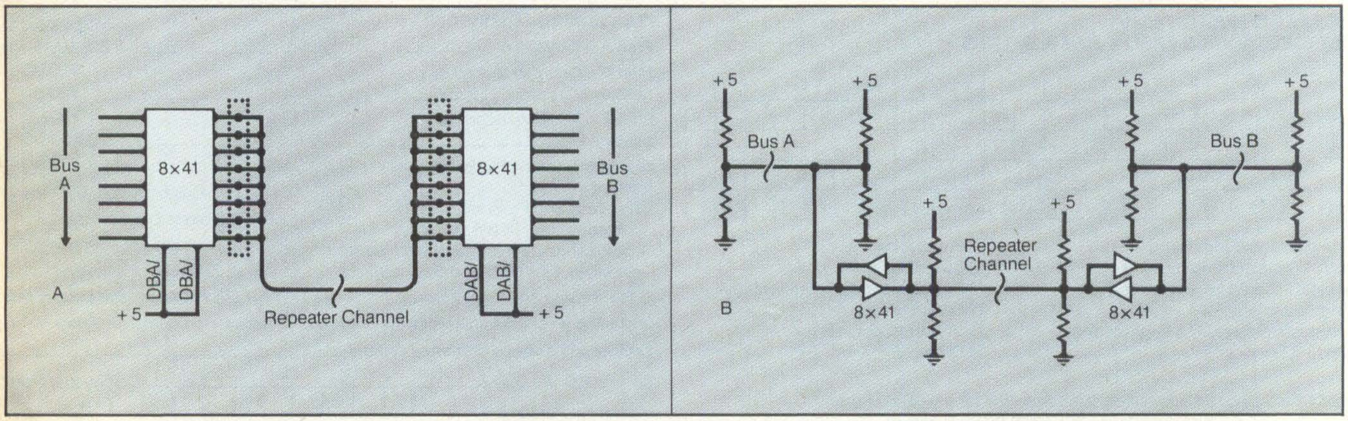

Figure 1: The 8X41, a: as an uncontrolled bus repeater; b: repeater terminations for a single channel.

CPUs maintain a memory mapping look-up table in external hardware to select from all existing physical memory), and those configurations which imply bus selection by the address of the data transfer operation.

System configuration and protocols for bus switching are very application dependent. However, the general concept is illustrated through the following example. Suppose an application calls for a fast image display station which is disk I/O intensive. A general purpose CPU is also required, but it has real-time processing commitments and must not be burdened by image transfers from disk. Program and data memory are too large to combine memory and CPU onto a single board.

In this system there are two masters that must communicate with off-board resources at high rates and without interference: the CPU must access program and data memory slaves, while the disk controller must transfer data at high rates to the display subsystem. At times, the CPU must have access to the disk. At other times, the disk controller must have access to data memory so that it can read and write I/O parameter blocks (IOPBs).

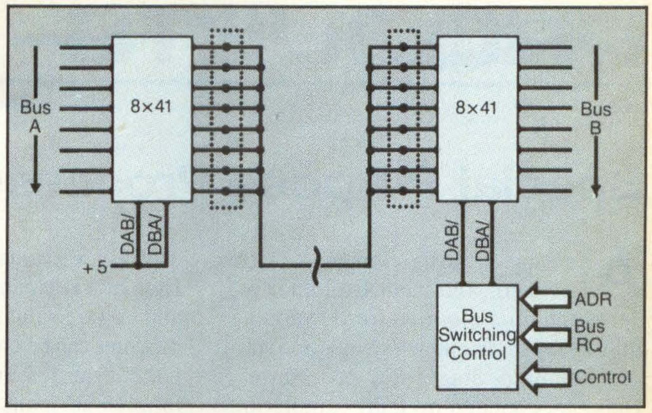

Figure 2: An example of bus switching using the 8X41.

A solution utilizing the 8X41 as a bus switcher is shown in **Figure 2**. The two buses are ordinarily connected through the 8X41, giving the CPU full access to the display subsystem and to the disk at bus speeds. When the CPU directs the disk controller to begin an operation, the disk controller requests mastership of its local bus. A control circuit responds to that request from the controller. The disk controller places an address on the bus, defining the bus location of the addressed slave. If that address matches a slave in the display subsystem, the slave will record and the transfer will continue normally without burdening the CPU. If that address points to a slave within the CPU's bus, the 8X41 link is re-established.

Circle 230

CALENDAR

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UNIX Seminar. Boston, MA. (Also in Atlanta, GA, April 17-19.) Contact: Center for Advanced Professional Education, 1820 E. Garry St., Suite 110, Santa Ana, CA 92705. (714) 261-0240.

April 2-4
Modern Integrated Circuit Technology. Santa Clara, CA. Contact: Technology Seminars Inc., PO Box 487, Lutherville, MD 21093. (301) 269-4102.

April 9-12
Implementing Local Area Networks. Philadelphia, PA. Contact: Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

April 9-12
Programming In C: A Hands-On Workshop. Los Angeles, CA. Contact: Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

April 9-12
Knowledge-Based Systems And Artificial Intelligence. Anaheim, CA. (Also in Palo Alto, CA, April 23-26.) Contact: Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

April 10-11
Nepcon Southwest '85. Dallas, TX. Contact: Ruann International, PO Box 1877, Des Plaines, IL 60018. (312) 296-2191.

April 10-12
Hands-On UNIX For Programmers. Bellevue, WA. Contact: Specialized Systems Consultants, PO Box 7, Northgate Station, Seattle, WA 98125-0007. (206) 367-8649.

April 14-18
Computer Graphics '85. Dallas, TX. Contact: National Computer Graphics Assoc., Suite 601, 8401 Arlington, VA 22031. (703) 698-9600.

April 16-18
ATE Silicon Valley '85. San Mateo, CA. Contact: Morgan-Grampain Expositions Group, 1050 Commonwealth Avenue, Boston, MA 02215. (617) 232-5470.

April 23-25
Electro '85. New York, NY. Contact: Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045. (213) 772-2965.

April 23-25
Mini/Micro Northeast '85. New York, NY. Contact: Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045. (213)772-2965.

April 24-26
UNIX Systems Expo '85 Spring. San Francisco, CA. Contact: Computer Faire Inc., 181 Wells Ave., Newton, MA 02159. (617) 965-8350.

April 30-May 2
Modern Electronic Packaging. Philadelphia, PA. Contact: Technology Serminars Inc. PO Box 487, Lutherville, MD 21093. (301) 269-4102.

April 30-May 2
Artifical Intelligence Exhibition. Long Beach, CA. Contact: Tower Conference Management Co. 331 W. Wesley St., Wheaton, IL 60187. (312) 668-8100.

May 6-8
Seminar And Trade Show For Printed Circuit Board Fabricators. San Jose, CA. Contact: PMS Industries Inc., 1790 Hembree Rd., Alpharetta, GA 30201. (404) 475-1818.

May 6-9
Modern Data Communications. Washington, D.C. Contact: The George Washington University, Washington, D.C. 20052. (202) 676-6106.

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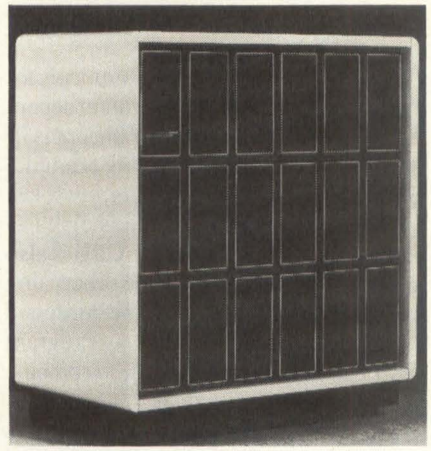
Comdex/Spring. Atlanta, GA. Contact: The Interface Group Inc., 300 First Ave., Needham, MA. (617) 449-6600.

NEW PRODUCTS

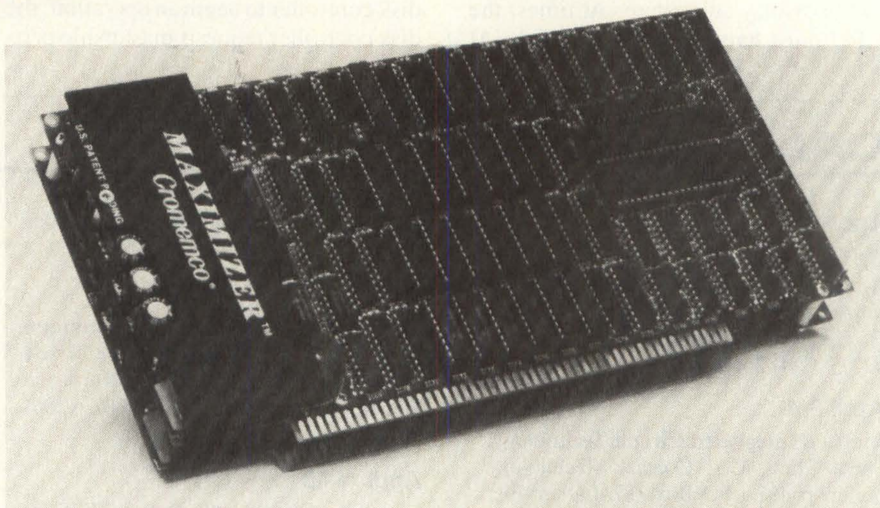
Special Purpose Processor



As an upgrade to the company's Logic Evaluator, the Fault Evaluator reduces the time required for developing fully tested semiconductor chips and subsequent chip diagnostic procedures. Using a concurrent fault simulation algorithm, the Fault Evaluator can simulate 16,000 faults per pass, rather than one per pass, as with the Logic Evaluator. In the form of ZIF modeling elements 500,000 differences can be maintained in each Fault Evaluator module. The Fault Evaluator is expandable up to 16 modules, and Logic Evaluator and Fault Evaluator modules can be combined in one cabinet. Other features include user controlled number of faults per pass, user select serial or concurrent algorithms, incremental loading of test vectors, initial release to handle unidirectional gates, RAM and ROM. **Zycad**, Arden Hills, MN **Circle 126**

12 MIPS Coprocessor

When used with the firm's software languages, this coprocessor subsystem, the Maximizer, performs IEEE double and single precision math functions. Executing an average of 12 MIPS, the Maximizer contains a 48 MHz (master clock rate) bit-slice processor. With 16 Kbytes of data memory (50 nsec cycle time), 16 dual-port registers and 4096 48-bit words of downloadable microcode instructions, the Maximizer is microprogrammable using the 4 Kbytes of microcode RAM. Most instructions execute in 62.5 nsec, but up to 125 nsec are allowed for complex operations. To support the Maximizer, a microcode assembler software package – Model Maxasm – is available. The Maximizer is available now to run under the CROMIX operating system and will soon be available under UNIX. Price is $3,495. **Cromemco**, Mountain View, CA **Circle 127**



300 Mbyte 5¼″ Winchester Drive

Based on 14″ drive design methods, MegaFile, a 5¼″ Winchester disk drive, consists of a shell-like Head Disk Assembly (HDA) containing up to 12 read/write heads and seven platters, spindle with an integrated motor, absolute filter and a voice coil positioner. The MegaFile also features a dual servo system: one dedicated servo surface plus embedded servo on all surfaces. Twin bearings on both top and bottom of the spindle and the positioner allow track density of 1207 tpi and recording density of 19077 bpi. With capacity up to 300 Mbytes per drive and a 25 msec average positioning time, the MegaFile has a 25000 hours HDA Mean Time Between Failure (MTBF). **Siemens**, West Lake Village, CA

Circle 128

COMPUTERS/SYSTEMS

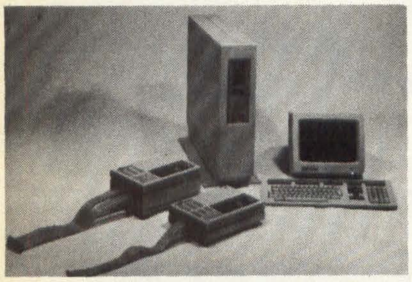
Word Pattern Generator

The latest feature of the Step-2700 Development Station, this Word Pattern Generator may be used as a separate device or with other design tools of the Step-2700. The pattern width is provided in 16-bit increments. The system also offers a fully programmable sequencer and a symbolically-oriented assembler. Patterns may also be uploaded or downloaded onto any host computer via RS-232. Prices start at $25,000. **Step Engineering**, Sunnyvale CA **Circle 173**

Multiplexer System

Allowing cluster controllers to be located at any position on two 1,000′ composite links made up of a twisted pair cable, the Mux Master Multiplexer System features 8 or 16 line modules, both of which can support local async devices at 50 to 38,400 baud/second. The Mux Master single host board supports up to 8 Q-Bus or 16 Unibus cluster controllers at 1 Mbyte/second. The system is software compatible with VMS, RSX and RSTS. Available in a desk-top, wall-mount or floor-stand model, the Mux Master is priced at $5,800. **Able Computer**, Irvine, CA **Circle 162**

Microprocessor Development System



Incorporating the Zax ICD-series in-circuit emulators and DEC's MicroVAX I, the ZAX/VAX, 32-bit universal microprocessor development system, provides 2 Mbytes of RAM, 31 Mbyte hard disk storage, 8-port RS-232 controller, disk controller and 400K floppy disk. Development software includes C, Pascal and PLM 86 language support, cross assemblers and the Zax interface (Zice). Zice features symbolic debugging capability, file control of the emulators, automatic journaling and help features. Price for the ZAX/VAX Development System is $56,000. **Zax**, Irvine, CA **Circle 168**

11/73-Based System

The 11/73-based Micro/11 system, Micro/11-73, contains a 20.8 Mbyte Winchester subsystem and a dual 8″ floppy, 1 Mbyte diskette subsystem. Supplied with dual size 256K or 512K RAM memory modules or a quad-size 1 Mbyte RAM module, the system is expandable to 4 Mbytes of memory. All memory boards feature full byte parity with CSR and block mode capability. A 250W switching power supply provides +5VDC, +12VDC and +24VDC to the backplane and disk subsystems. The backplane card guide accomodates eight quad-size modules and provides 22-bit addressing on all slots. Price is $13,150-$15,050. **MDB**, Orange, CA **Circle 172**

68000 Emulator

The SA700-68K emulator for the 68000 combines software development capability with a 68K mini-assembler, a real-time 10 MHz in-circuit emulator, CRT display, fold-down ASCII keyboard, 8″ floppy disk drive and a built-in PROM programmer. It accepts executable object code and symbol files in Motorola's S-record format from development hosts such as the VAX running VMS or UNIX. A batch Debug command language in the SA700 allows the user to develop and execute debug routines on the emulator. **Sophia Computer Systems**, Santa Clara, CA **Circle 163**

Color Workstation

An addition to the CAE 2000 product line, the CAE 2000/550 color workstation is based on the Apollo Domain DN550. Operating as a standalone or as a node in a "Worksystem," the CAE 2000/550 uses a 32-bit 68010 processor and a dedicated bit-sliced graphics processor. The system is available with up to 3 Mbytes main memory and can support up to 24 concurrent processes, each with 16 Mbytes of virtual address space. CRT resolution is 1024 × 800, displaying eight colors simultaneously. All color features of the CAE 2000/550 are user-configurable. Price is $62,800. **CAE Systems**, Sunnyvale, CA **Circle 166**

Multiuser UNIX Workstation

Based on the 68000/68010, the Minibox multiuser UNIX system offers a built-in C compiler, six Multibus card slots (five open for users), single or dual 5¼″ floppy drives, 30 Mbyte to 280 Mbyte Winchester storage and an interactive streamer tape drive. The Minibox is built around the HK68 microcomputer featuring an 8 or 10 MHz CPU, quad-channel DMA, Winchester interface, streamer tape drive (or definable dip switches), 64 Kbytes EPROM, 512K to 1 Mbyte RAM, two iSBX expansion connectors, MMU (addresses 16 Mbytes of RAM), four serial I/O ports (expandable to 12) and three 16-bit counter timers plus two parallel I/O ports. **Heurikon**, Madison, WI **Circle 171**

32-Bit Processor Systems

An addition to the firm's family of 32-bit multiprocessor systems, the 1200 Series of multiprocessor systems contains up to four 12.5 MHz 68000 CPUs, 12 68000-based I/O controllers, 16 Mbytes of EDAC main memory and up to 88 async and sync serial communications ports. With up to 4 internal and 44 external disk drives, the 1200 provides up to 9 Gbytes of storage for up to 88 users. The system also features a 33.3 Mbyte/second I/O transfer rate, and like the earlier 1100 series, supports both the ARIX and RM/COS operating systems. Price is $70,000-$150,000. **Areté**, Mountain View, CA **Circle 165**

IBM PC-Compatible Multiuser Computer

An extension of this company's Personal Mini Family, the PM/4T and PM/16T multiuser computers are IBM PC compatible. The PM/4T 4-user version contains a 20 Mbyte formatted Winchester drive, a 4 tpi, PC-compatible floppy drive and an integrated 20 Mbyte streaming tape drive. The PM/16T incorporates a 20 Mbyte streaming tape drive, 512 Kbytes of RAM, a 44.5 Mbyte formatted Winchester drive and a 48 tpi, PC-compatible floppy drive. Price is $5,995 (PM/4T) and $9,995 (PM/16T with Infoshare/M and PM/Office Manager). **TeleVideo Systems**, San Jose, CA **Circle 170**

Logic Programmers

Combining menu-driven protocols, this multiuser prototyping tool (60A) programs devices inserted manually into a socket, while the 60H combines the capabilities of the 60A with a software and hardware interface to an automatic device handler. The handler automatically inserts devices into a socket and the 60H programs and tests them. No device codes are required and both models operate as standalone or remote-controlled programmers. Price is $3,425 (60A) and $4,425 (60H). **Data I/O**, Redmond, WA **Circle 161**

PERIPHERALS

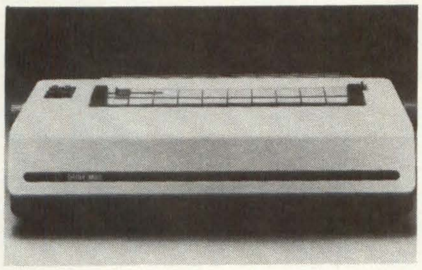
Capacitance-Sensing Touch Screen

An addition to this firm's series of capacitance-sensing touch screens, the TK-1000D series has a touch response time under 50 msec. The unit consists of a monolithic glass sensor and circuit board that contains touch sensing circuitry and an RS-232-C interface. Standard screen types are flat, cylindrical curved and spherical. Standard sizes are 9″, 12″, 13″, 15″ and 19″ diagonals. Price in quantities of 1,000 is $450. **Interaction Systems**, Newtonville, MA **Circle 181**

LCD Modules

With an 80 column × 25 line format, the two new LCD modules, CG-6402000G and CG-6402001G, have a 640 × 200 dot display. Effective display area of the CG-6402000G is 224 mm/8.8" wide × 70 mm/2.8" high, and the CG-6402001G is 224 mm/8.8" × 168 mm/6.6". Corresponding pixel size is 0.31 mm square and 0.31 mm × 0.79 mm rectangle. The modules require +5V and -12V DC. Price in quantities of 1,000 is $200 (6402000G) and $300 (6402001G). **C. Itoh**, Los Angeles, CA **Circle 182**

Daisy Wheel Printer



Compatible with most Diablo, Qume and NEC printers, the M20 daisy wheel printer prints 20 cps bidirectional. Horizontal formats include 10, 12, 15 pitch and proportional spacing, printing each line 15.7" wide on paper up to 16.5" wide. It also allows six, eight or twelve lines/inch. A separate motor drives the multistrike ribbon cartridge, creating longer ribbon life. In plotting, a resolution of 23,000 dots/square inch is used. **Daisy Systems Holland BV**, The Netherlands **Circle 187**

Protocol Converter

By emulating an IBM 3278-2 display station, the PC-1000E microprocessor-based protocol converter can link ASCII terminals and PCs to the IBM 3270 network. Featuring multilevel password security, help screens, substitution of English commands for IBM functions, dial-up connection and default terminal type selection, the PC-1000E may be used in BSC, SNA/SDLC protocols or in channel-attached operations. Able to connect to a modem, the PC-1000E is accessible by any remote terminal or PC dialing in through switched or leased lines, or through a data switch. Price is $995. **International Data Sciences**, Lincoln, RI **Circle 184**

½" Streaming Magnetic Tape Drive

With a MTBF of 7,400 hours, the DMT 2000 ½" streaming magnetic tape drive features automatic tape loading and self diagnostics. Reel sizes are 10½", 8½" or 7", and phase encoded, 9-track tape format is fully ANSI/IBM-compatible at 1600 bpi. The DMT 2000's drive mechanism reduces the amount of uneven roll on the tape-up reel and guarantees uniform tension during rewinding. With a dual tape speed of 100/25 ips, the unit also offers a switch-selectable interblock gap with four settings: 0.6", 1.2", 1.8", 2.4". **Anritsu**, Oakland, NJ **Circle 185**

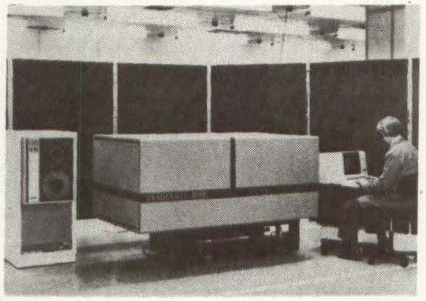
Enhanced Network Bridge

Designed to interconnect multiple Net/One communications systems in the same geographic location, the enhanced network bridge, Net/One Local Bridge, allows connection between frequency channels on broadband networks. The enhanced Net/One Local Bridge forwards information from network to network or channnel to channel on a per-packet basis at rates of 1,000 packets/second. The new Local Bridge can also forward network management messages from network to network. Price is $9,850. **Ungermann-Bass**, Santa Clara, CA **Circle 183**

2400 BPS Modems

All five of these full-duplex auto-dialing modems, 2400PA, VA4224, VI2422S, 2400V and 2400PC, operate at 2400, 1200, and 0 to 300 bps, automatically selecting the appropriate speed. At 2400 bps, these modems comply with CCITT recommendation V.22 bis. Various features include automatic dialing, call-progress detection, security passwords, user diagnostics, public switched-telephone network support and two-wire leased line operation. Price ranges from $925-$995. **Racal-Vadic**, Milpitas, CA **Circle 179**

Automated PCB Plotter



The EP530 precision photo plotter can be controlled and operated interactively with the VDT and keyboard. Users can also input via punched paper tape, magnetic tape and an on-line interface. Diagnostic routines are built into the microprocessor to increase availability of the plotting system. The unit features linear motors rather than gearbox drive systems and uses fiber optic light transmission to reduce weight. **Ferranti Infographics Division**, Huntington Beach, CA **Circle 174**

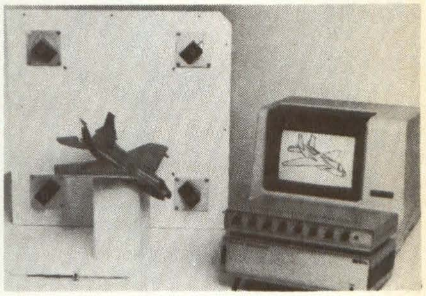
7" Liquid Crystal Shutter

Providing contrast in high ambient light, this 7" liquid crystal shutter consists of a liquid crystal switch (pi-cell) set between two color polarizers and a neutral polarizer. Combined with a monochrome CRT, the Liquid Crystal Shutter transmits the green part of the light when a voltage is applied and the red part when the voltage is removed. Any combination of the two primary colors is accomplished by varying the CRT beam current. Available in a red/green/yellow color combination, the 7" liquid crystal shutter is offered with a 7" monochrome CRT with red/green phosphor. Single unit price is $200. **Tektronix**, Beaverton, OR **Circle 175**

5¼" Winchester Drives

The Miniscribe 6000 family of 5¼" full-height Winchester disk drives comprises four models: the 6085 with unformatted storage of 85.3 Mbytes, the 6074 with 74.7 Mbytes, the 6053 with 53.3 Mbytes and the 6032 with 32 Mbytes. With an average access time of 30 msec, all model 6000 drives have an ST412 track capacity of 10,416 bytes and 5.0 Mbit/second data transfer rate. Other features include a single printed circuit board, low power requirement and automatic actuator lock. **Miniscribe**, Longmont, CO **Circle 186**

3D Digitizer



The GP-8-3DP sonic digitizer uses sound to determine the distance between a digitized point and four microphone sensors that are mounted on a plane. The host computer then converts these distances into Cartesian X, Y and Z coordinates. Users can adjust the active volume to up to 10' × 10' × 10' with a .01" resolution throughput. Choice of formats include ASCII or binary RS-232-C or parallel packed binary. Optional multiplexers that digitize up to 16 points in space sequentially are offered. Price is $7,500. **Science Accessories**, Southport, CT **Circle 180**

COMPONENTS

FIFO Buffer Unit

As an addition to the family of Z8000 and Z8500 peripheral products, the Z8060 FIFO buffer unit and FIO expander features bidirectional, async data transfer, 128-bit × 8-bit buffer memory and 3-state data outputs. With two-wire, interlock handshake protocol, the Z8060 operates in temperature ranges of 0°C to +70°C and -40°C to +85°C. Other operating characteristics include 6 MHz and 4 MHz clock frequencies, -0.3V to +7.0V max operating voltages, and a storage temperature of -65°C to +150°C. Price in quantities of 1,000 is $15. **SGS Semiconductor**, Phoenix, AZ **Circle 134**

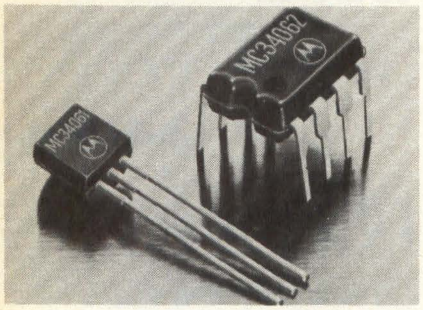
Multiplexed Comparators

Allowing the user to program 256 different comparator threshold levels, the ADC0852 and ADC0854 CMOS analog comparators are powered from a single +5V supply and dissipate 30 mW. A choice of 2- or 4-input multiplexers is provided, with both single-ended and differential input capability programmable in either device. Total untrimmed error (accuracy) of ± 1/2 lsb of reference includes comparator offset, threshold DAC nonlinearity and multiplexer errors. Packaged in an 8-pin mini DIP, price in 100s is $2.65-$2.85. **National Semiconductor**, Santa Clara, CA **Circle 133**

Bipolar Op Amp

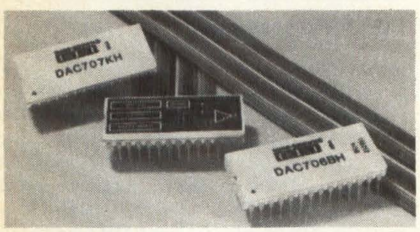
The HA-2541 wideband, unity gain stable, bipolar operational amplifier achieves a unity gain bandwidth of 40 MHz and a 300V/μsec slew rate. With an 80 nsec settling time, a 5 MHz power bandwith and an output voltage swing of $\pm$10V, the HA-2541 is pin compatible with the HA-2540, HA-5190 and LH-0032 wideband op amps. Price in quantities of 100 ranges from $6 (DIP, commercial temperature range 0° to +75°C) to $24 (TO -5 metal can package). **Harris**, Melbourne, FL **Circle 131**

Overvoltage Sensing Circuits



These two overvoltage sensing circuits (MC34061, MC34062) offer a choice of power supply overvoltage trip points ranging from 2.5V to 40V. The MC34061 three-terminal device includes a voltage reference of 2.5V bandgap type with tolerances of $\pm$1.0% at room temperature and $\pm$2.0% over temperature (a suffix device). The internal comparator provides 250 mV of hysteresis, and drain current is 1.5 mA over its power supply voltage range (3.0V to 40V) and temperature range. The MC34062 Pin Programmable overvoltage sensing circuit provides a six-resistor network which can program 120 different overvoltage trip points from 25V to 39V. **Motorola**, Phoenix, AZ **Circle 142**

μP Compatible 16-Bit DACs



Designed to interface to a 16-bit μprocessor bus, the DAC705, DAC706 and DAC707 are complete digital-to-analog converters. Each model features a maximum linearity error of $\pm$0.003% of FSR and maximum differential linearity error (BH grade) of $\pm$0.006% FSR. With a guaranteed monotonicity to 14 bits over the 0°C to +70°C (KH grade) and -25°C to +85°C (BH grade) temperature range, gain drift is $\pm$15 ppm/°C typical (RH), $\pm$25 ppm/°C (KH). All models operate from $\pm$12V and $\pm$15V supplies. Prices in 100s start at $44. **Burr-Brown**, Tucson, AZ **Circle 137**

Dual 12-Bit DAC

Matching DAC ladder resistances to 3% (maximum), this dual 12-bit DAC (AD7549) occupies one-half to two-thirds of the area occupied by two separate DACs. Both DACs in the AD7549 have separate reference inputs and feedback resistors, are loaded from double-buffered latches and provide four-quadrant multiplication capability. Guaranteed monotonic over the full military temperature range, the AD7549's maximum gain error is restricted to three and six lsb for K/B/T and J/A/S grades; relative accuracy is one-half and 1 lsb max for the same grades. Packaged in a 0.3" wide 20-pin DIP, the price is $16.95 to $80. **Analog Devices**, Norwood, MA **Circle 141**

Hermetic Color Dot Matrix Displays

Available in yellow (HDSP-088X) and two versions of high-efficiency red (HER) (low power–HDSP-078X and high brightness–HDSP-079X), this family of dot matrix displays operate as single digit, numeric, hexadecimal or overrange indicators. Featuring a hermetic seal, the displays are end-stackable and operate over a -55°C to +100°C range, offer TTL compatibility and are end-stackable. Price in quantities of 1 to 99 is $64-$72. **Hewlett-Packard**, Palo Alto, CA **Circle 140**

BOARDS

IBM PC/XT-Compatible Controllers

An expansion of the firm's data controller line, these two controllers (OMTI 5500, OMTI 5700) can attach up to two ST506/412 interface-compatible fixed and/or removable drives. The OMTI 5700 supports Winchester drives as well as a QIC-02 interface-compatible streaming tape drive and offers three bidirectional data paths. Using the Winchester cartridge as backup, the OMTI 5500 provides up to 10 Mbytes of backup on a single media volume. The OMTI 5700 provides up to 60 Mbytes of backup using the QIC-02 tape capabilities. Price is $245 (5500) and $365 (5700). **SMS**, Mountain View, CA **Circle 146**

VMEbus Serial And Parallel I/O Board

Fitting into a single slot in a card cage, this serial and parallel I/O module for a VMEbus system offers up to eight async serial communications channels, 24 parallel I/O lines and an on-board control latch. The 24 parallel I/O lines provide one Centronics-type printer port plus 12 bidirectionally buffered lines, or two printer ports. All parallel I/O is accommodated through the board's P2 connector. A 24-bit programmable counter/timer can be used to generate system interrupts, to perform real-time clock functions or to act as a watchdog timer. Price is $1,130. **General Micro Systems**, Ontario, CA **Circle 145**

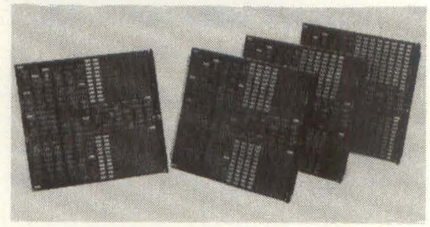
Front-End Communications Processor

Available in dual-ported RAM configurations of 64, 256 and 512 Kbytes, sharing a 64 Kbyte memory space with the IBM PC, the DCP-88/VM single-board front-end processor for the IBM PC family and compatibles can support up to four multiprotocol communications lines and parallel printer port. Memory is addressable on a bank-select basis from the host PC or directly from the DCP-88/VM processor. Price is $695. **Emulex**, Costa Mesa, CA **Circle 144**

32-Bit Multibus Board

Featuring three members of the NCR/32 chip set, the NCR/32-796A 32-bit microprocessor on a Multibus board includes a 32-bit ALU and 32-bit process or memory (PM) bus. The addressing range available is 4 Gbytes virtual and 16 Mbytes real memory. Operating with a 13.3 MHz clock, the board has 150 nsec access time and dual port main memory access via Multibus or iLBX. The NCR/32's external microprogrammability is supported with 16K words of RAM microcode instruction storage. A 128-word scratch pad memory for temporary data storage is also available. Price is $895. **NCR**, Dayton, OH **Circle 160**

Add-In Memory Cards

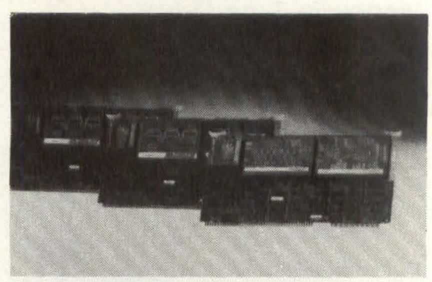


Compatible with the Prime 2250, 2550, 9650 and all older 50 Series CPUs, these memory cards use 256 Kbyte RAMs for capacities of 1024 to 4096 Kbytes. The 1 Mbyte E9-1 is functionally equivalent to Prime's E9 module including self-interleaving, wide word and error check and correction. The E9-2 features 2 Mbytes of RAM, E9-3, 3 Mbytes, and E9-4, 4 Mbytes. This new series of memory cards incorporates all of the additional features of the company's earlier Prime-compatible memories including on-line/off-line comfort switch. Prices are up to $5,530. **EMC**, Natick, MA **Circle 152**

Auto Dial Card

Designed for 110 and 300 bps operation, the 103 Auto Dial Card features auto dial, auto answer, analog and digital test modes. All functions of this modem card assembly are controlled by serial data commands; and it is compatible with the Bell 103A and the CCITT V.21 standards for direct connection to the switched telephone network. The assembly is available with either the Novation or the Hayes-compatible command set. The 103 measures 3" × 4". **Novation**, Chatsworth, CA **Circle 151**

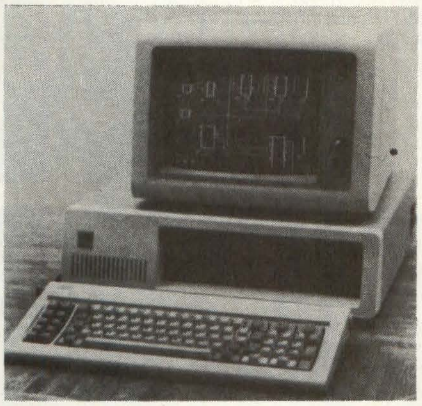
Multibus A/D Boards



Consisting of three boards: DT772 for high level analog inputs, DT774 for low level analog inputs, and DT778 for simultaneous sample/hold analog input system, the DT772 Series of Multibus boards offers 8- and 16-bit data transfer rates and 24-bit addressing capabilities. Both the DT772 and DT774 provide up to 40,000 samples/second throughput rates with 12-bit resolution. The DT778 allows the user to take a snapshot of up to 12 single-ended analog input channels, freezing their values within a $\pm$5 nsec aperture uncertainty. Price is $895-$1,695. **Data Translation**, Marlboro, MA **Circle 157**

SOFTWARE

Design Automation Software



Tailored for the IBM PC/XT and compatibles, this schematic-capture software package, Dasoft 16S, comes with a component library, design and library editors, a graphics-oriented design entry routine, documentation programs and plotter drivers. Allowing users to build schematics on the CRT screen, Dasoft 16S displays and positions symbols as they are called up from the library. The system automatically checks for duplicate designators; title blocks are defined and revision blocks are optional. Price is $12,000. **Dasoft Design Systems**, Berkeley, CA **Circle 194**

Updated UNIX-Compatible Operating System

An enhanced version (Revision 5) of the UNOS operating system supports VMEbus, Versabus, runs larger disks and data files, supports ISO standard LANs and interconnects with IBM systems. This UNIX-compatible operating system runs on Charles River Data's Universe 68 and 2203 families of supermicros. Identical versions of UNOS Revision 5 run on the VMEbus-based Universe 6 computers. UNOS Revision 5 also supports Universe NET, the company's LAN as well as disk files up to 2 Gbytes. **Charles River Data Systems**, Framingham, MA **Circle 195**

CP/M For Macintosh

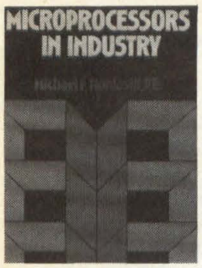
Resulting from a contract between Digital Research and I.Q. Software, the CP/M operating system is now available for the Macintosh Computer. Two programs that run on the Macintosh now are Wordstar and dBase II. Each CP/M package includes two volumes of documentation from Digital Research and I.Q. Software, six diskettes of programs including CP/M, C Language Compiler, Modem 7 compatible program, Macro Assembler, Terminal Emulation and Standard Printer Drives. Price is $395. **I.Q. Software**, Ft. Worth, TX **Circle 192**

Graphics Support Software

Designed to run on the AT&T PC 6300 and compatibles equipped with the Video Display Adapter or the Image Capture Board, the Paint and Image Processing Software and Business Graphics Presentation Software provide continuous-tone graphics capabilities. The paint and Image Processing Software has functions for adjusting color, adding to or eliminating elements in a photo, combining photos, cropping as well as color manipulation, text overlay, merging of multiple images, drawing and layout. The Business Graphics Presentation Software generates two- and three-dimensional bar and pie charts and is compatible with the Paint and Image Processing Software. **AT&T**, Indianapolis, IN **Circle 199**

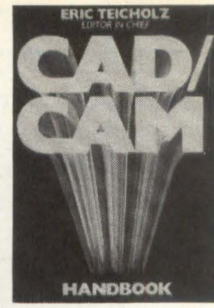
Fault Isolation Software

Enabling fault isolation in IBM PCs to the component level, the IBM PC Test modular software package is designed for Fluke's 9010A or 9005A Micro-System Trouble Shooters and Fluke's 8088 Interface POD. The package consists of five tape modules and a manual, allowing for guided fault isolation (GFI) or self-guided tests. Tapes one and two perform auto-tests and functional go/no-go IBM PC testing. The other three tapes contain GFI programs for the main board, disk controller and monochrome video board. Price is $1,500. **Fluke**, Everett, WA **Circle 198**



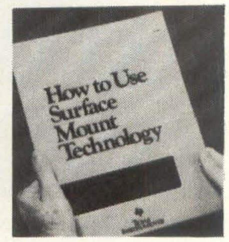
Microprocessors Book. This 544-page book from Van Nostrand Reinhold provides information on microcomputer system design and control theory for industrial applications of microprocessors. Microprocessors are discussed in relation to sensor systems, data acquisition, microcomputer products, and automatic control systems. Also explained are interfacing, programming, control system elements, and systems application and design.
Van Nostrand Reinhold — **Circle 257**

CAD/CAM Handbook. This 432-page book from McGraw-Hill contains contributed sections from 20 specialists on their areas of expertise in CAD/CAM technology. The book explores effective ways to evaluate and acquire CAD/CAM systems, and demonstrates how they are currently used. Described are the hardware and software involved as well as applications.
McGraw-Hill — **Circle 254**



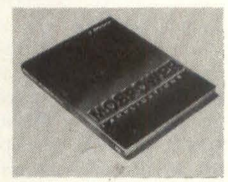
Integrated Circuit Mask Book. This 281-page book from McGraw-Hill covers aspects involved in making an integrated circuit mask, including substrate imaging, quality control, production techniques, etching, pattern design and measurement, mask quality glass and coatings for mask blanks. Included are illustrations, photos and line drawings.
McGraw-Hill — **Circle 258**

Surface Mount Technology Manual. This 112-page manual from Texas Instruments provides an overview of surface mount technology, including terminology, the connection process, testing and reliability consideration and current surface-mounted products. Also covered are the thermal characteristics of surface-mounted component (SMC) assemblies and techniques for combining SMCs and DIPs on the same board.
Texas Instruments — **Circle 252**



Micro-Products Handbook. This 176-page book from Emulex Corp. provides information on its line of micro products, including host adapters, disk and tape controllers, micro subsystems, and the Persyst line of products for the IBM PC. An overview of each major product line is presented and includes background on the operational environment, as well as characteristics of the peripheral devices supported.
Emulex — **Circle 250**

Power Mosfets Applications Handbook. This 512-page technical reference book from Siliconix contains articles and application notes that will aid in the design of power Mosfet circuits. Provided are information and solutions to power Mosfet design problems. Subjects covered include power Mosfet structures, electrical characteristics, thermal design, SOA precautions, practical design considerations, and device testing and reliability.
Siliconix — **Circle 251**



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