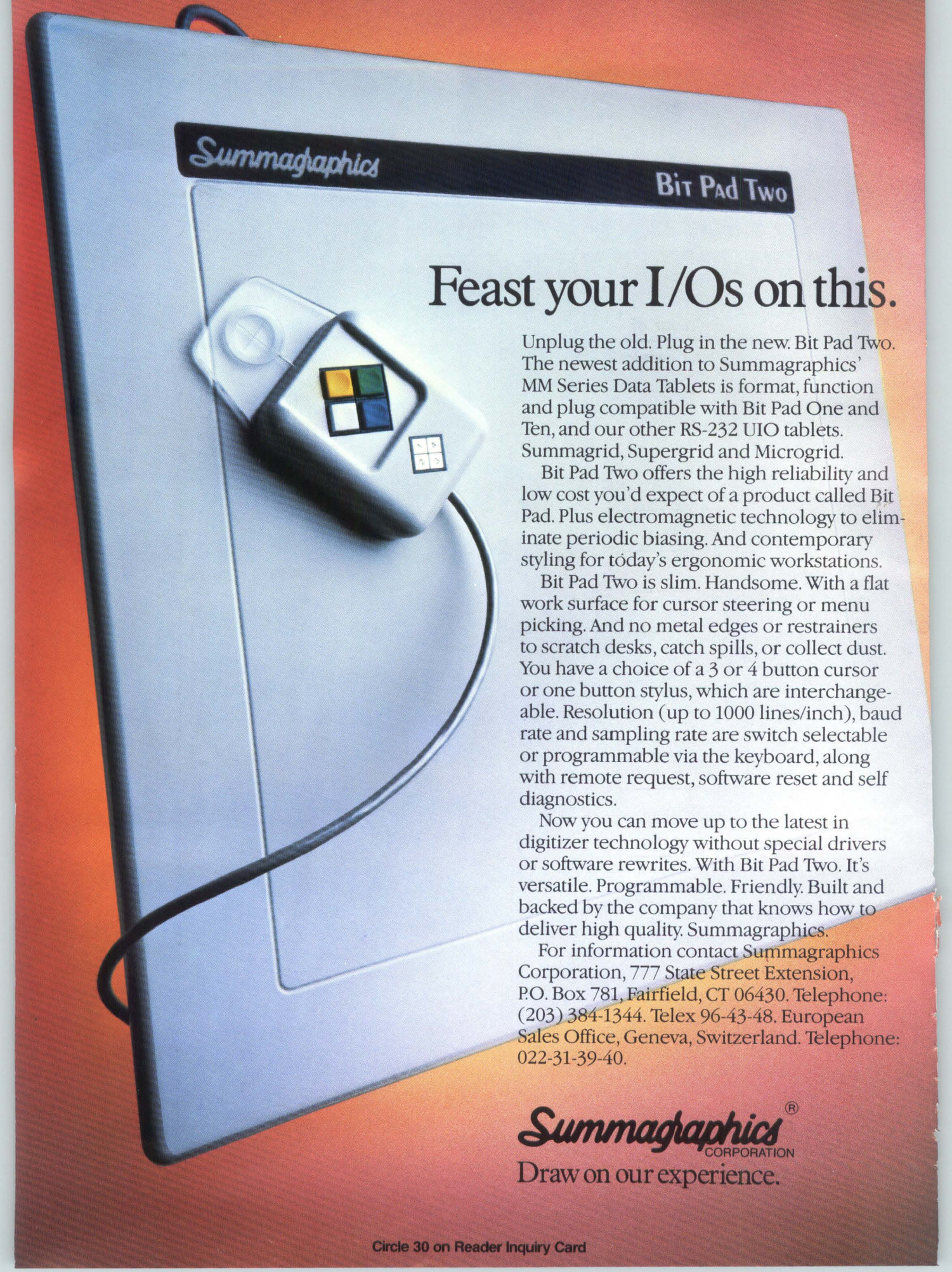
A MORGAN-GRAMPIAN PUBLICATION

DIGITAL DESIGN

SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS JANUARY 1985

- DIGITAL DESIGN BUILDS A CHIP WITH A WORKSTATION TO UNLOCK THE MYSTERIES OF GATE ARRAY DESIGN, PART I
- INTEGRATING HIGH PERFORMANCE DISK DRIVES
- APPLICATION AREAS BROADEN FOR 256K DRAMs
- OPERATING SYSTEMS
- MINICOMPUTERS

PLETHORA OF BOARDS OFFERS FLEXIBILITY IN MULTIBUS DESIGNS



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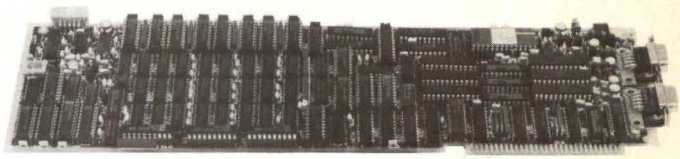

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If you want to significantly enhance your OEM product offerings and enable your products to fit in easily with your customers' distributed computing environments, consider the advantages of Digital Network Architecture.

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DIGITAL NETWORK ARCHITECTURE, YOUR WINDOW TO THE WORLD.

Digital Network Architecture (DNA) is the most comprehensive communications strategy yet developed, and currently implemented in proven, deliverable products. It supports several communications technologies. And it can accommodate future standards as they emerge because DNA is implemented in a layered structure consistent with the ISO Open Systems Interconnect model.

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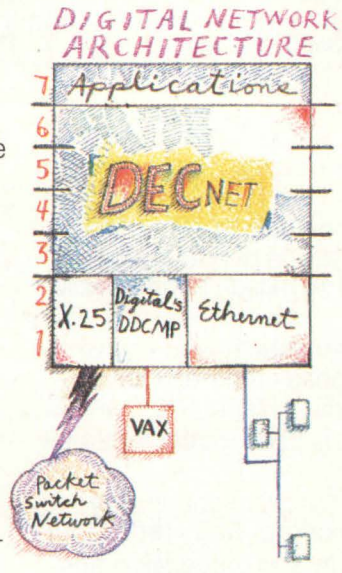

You can communicate with mainframe systems. You can match the technology to the job. And, most importantly, you can keep pace with your customers' distributed processing needs as they develop.

DECnet™ software lets you link Digital's systems in both local and wide area configurations. It supports high-speed local area network communications using Ethernet. And it provides gateways to allow Digital's computers to communicate with other vendors' systems over private lines or packet switched X.25 networks. This means you can tailor your products to fit in with your customers' current and future networks.

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The benefits you and your customers get by incorporating Digital's networking capabilities are virtually unlimited.

First of all, your systems can incorporate recognized industry standards. Such as Ethernet (IEEE 802.3 specification), X.25, and others.

In addition, our growing set of network-based products, including a distributed database system, allow your single systems to easily grow into networks. Your applications can access remote data and other resources transparently, with no extra development required.

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In short, DNA and Digital's products do the most to ensure that your systems will fit in with both new and existing networks.

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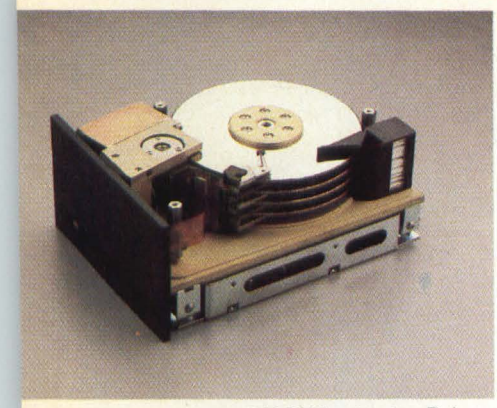

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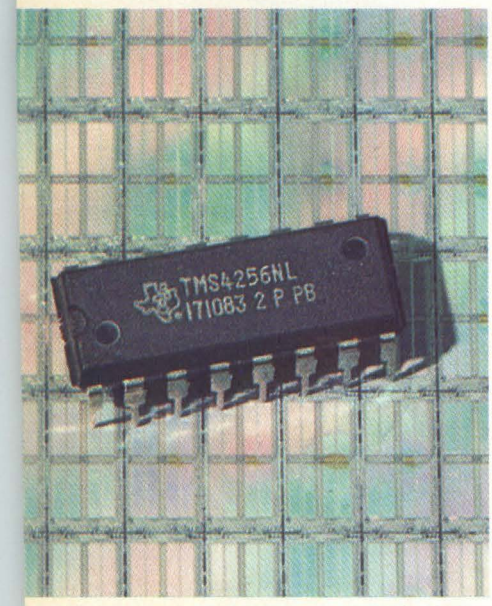

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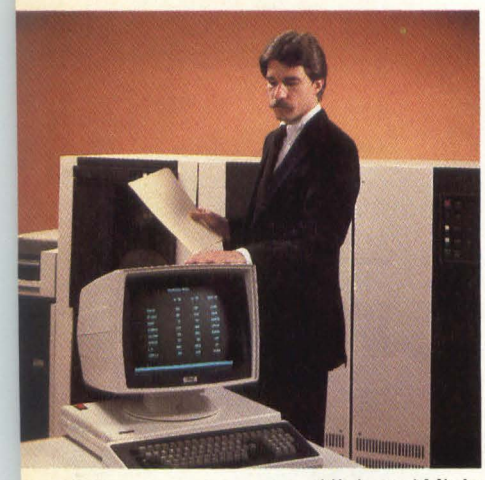

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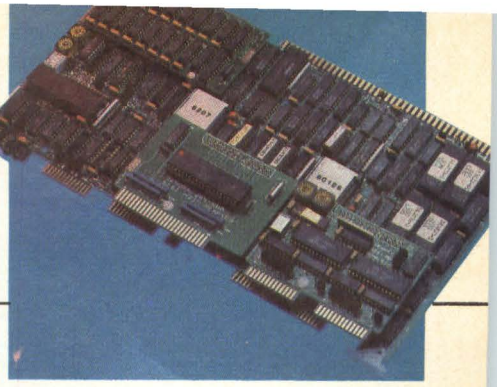

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FEATURES

ON THE COVER

The options available to the systems architect when implementing a Multibus system are now even greater. As newer technologies, such as surface mount devices and SIPs find their way onto boards, the Multibus will meet market demands for greater functionality at lower cost. Photo courtesy Intel Corp.

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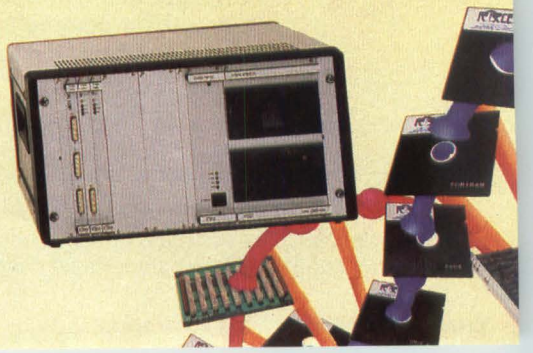

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READER INVOLVEMENT

A recent issue of *Business Marketing* featured an editorial entitled "Journalism Close To Your Wallets." The question was asked, "Can business/industrial advertisers simply sit back, offering nothing more than good wishes to the foundation, and enjoy its long-term benefits?"

Jim DiFilippo, Publisher of *Digital Design* (second from left) presents a Sony Watchman to Bill Schilp, Sr. Member of Technical Staff, RCA Corp. (Somerville, NJ). Mr. Schilp was the winner, randomly selected from those responding to a recent *Digital Design* Benchmark Study. Also pictured are (far left) David Wilson, Executive Editor, *Digital Design* and (far right) Dale Ludlum, Public Relations Director, RCA Corp.

The author answered his own question by saying: "We think not. Advertisers should support vigorous, high-quality trade journalism by limiting buys to publications that really earn reader involvement. Buying the best editorial vehicles serving a market is, clearly and simply, good business sense.

"Instead, however, advertisers buy publications in the same cavalier way they buy direct mail lists and postcard decks. Or they make a snap buy of the top-selling book in the field, or the one that the media rep claims has the most circulation among potential buyers. But all this ignores readership."

Reader involvement is a vital ingredient for the success and value of any publication. You, the readers of *Digital Design*, have shown a great deal of involvement. This is evidenced by the tremendous response we receive from our bound-in studies, our editorial benchmark study and other research surveys that we've conducted during the past year.

Surveys and studies can be a detriment rather than a help if they're used simply to guide action. Reliance upon them is a sure-fire way to become followers rather than leaders. The editors of *Digital Design* agressively research a range of topics. On the basis of information gathered from competing manfacturers, they objectively analyze technologies and products. There are no followers here.

At *Digital Design*, we realize that each of you are faced with a number of design choices in your day-to-day activities. The appreciation that these design choices exist is what makes *Digital Design* unique to the marketplace. We feel that to serve our readership, the editorial content should focus on addressing the design issues of the present and future.

Your input in all areas of research has provided the editorial staff with vital information and direction in addressing your needs. In addition to written research, we recently assembled several of you at a round table and conducted a reader focus group. We will continue to enlist your support and involvement in every way possible. Without it, we have no purpose to serve.

The new year is upon us. What we will offer you in 1985 is the most comprehensive editorial package of any magazine in the marketplace. Our focus will continue to address the issues of systems architecture, integration and applications. Our scope will discuss these issues at the IC, board and systems level. Within each of these categories—chip, board and box—you are faced with options. We will help you explore these options.

Publishing today demands flexibility. But flexibility and adaptability must not be achieved at the cost of personality. A publication must attain and project a consistent personality or each issue becomes a disparate miscellany within covers bearing the same title. *Digital Design*'s personality stems from a consistent, readily recognized editorial approach. Without it, continuity of attention and interest—and reader loyalty— are lost because the competition for attention from trade publications has never been greater.

I look for your continued involvement with *Digital Design*. Your involvement and our commitment will allow us to provide you with the most complete magazine in the industry—one that you cannot wait to get your hands on month after month.

Best personal regards,
James R. DiFilippo, Publisher

DIGITAL DESIGN
SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS

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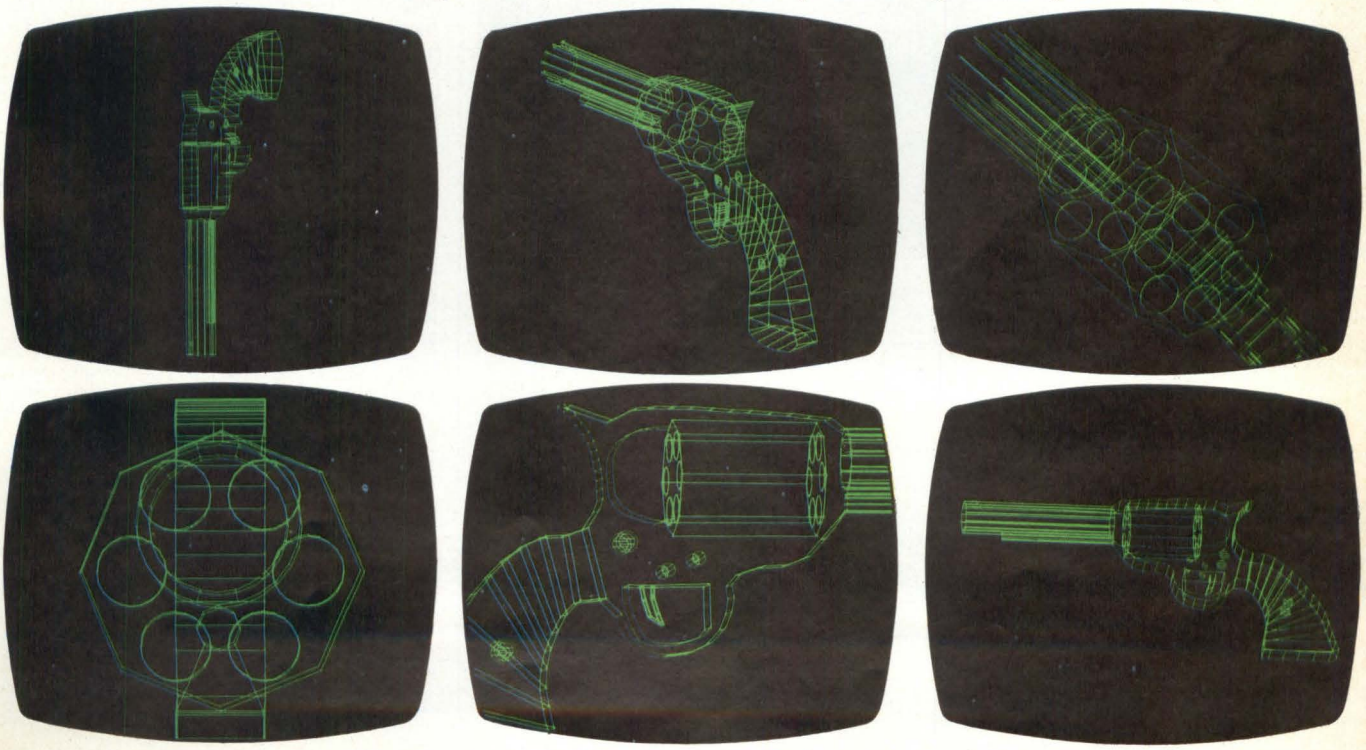

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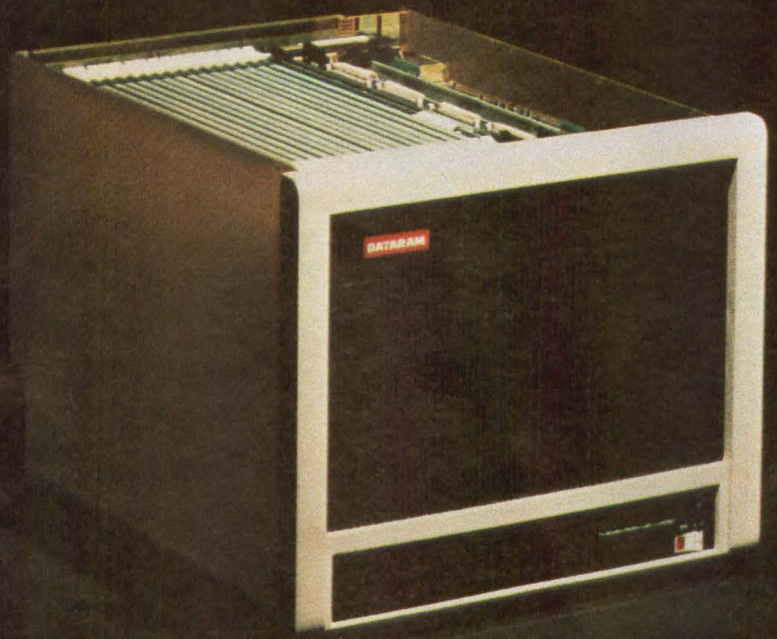

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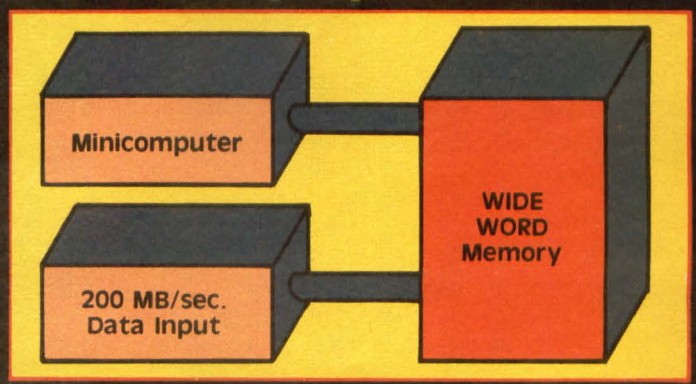

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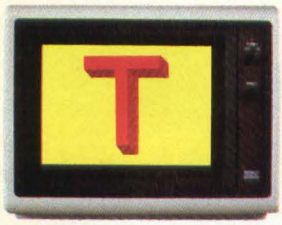

here's a lot more to a Fujitsu gate array than glass, gold, and aluminum; it's the human element that really sets our product apart.

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That's how you get numbers like these:

CMOS

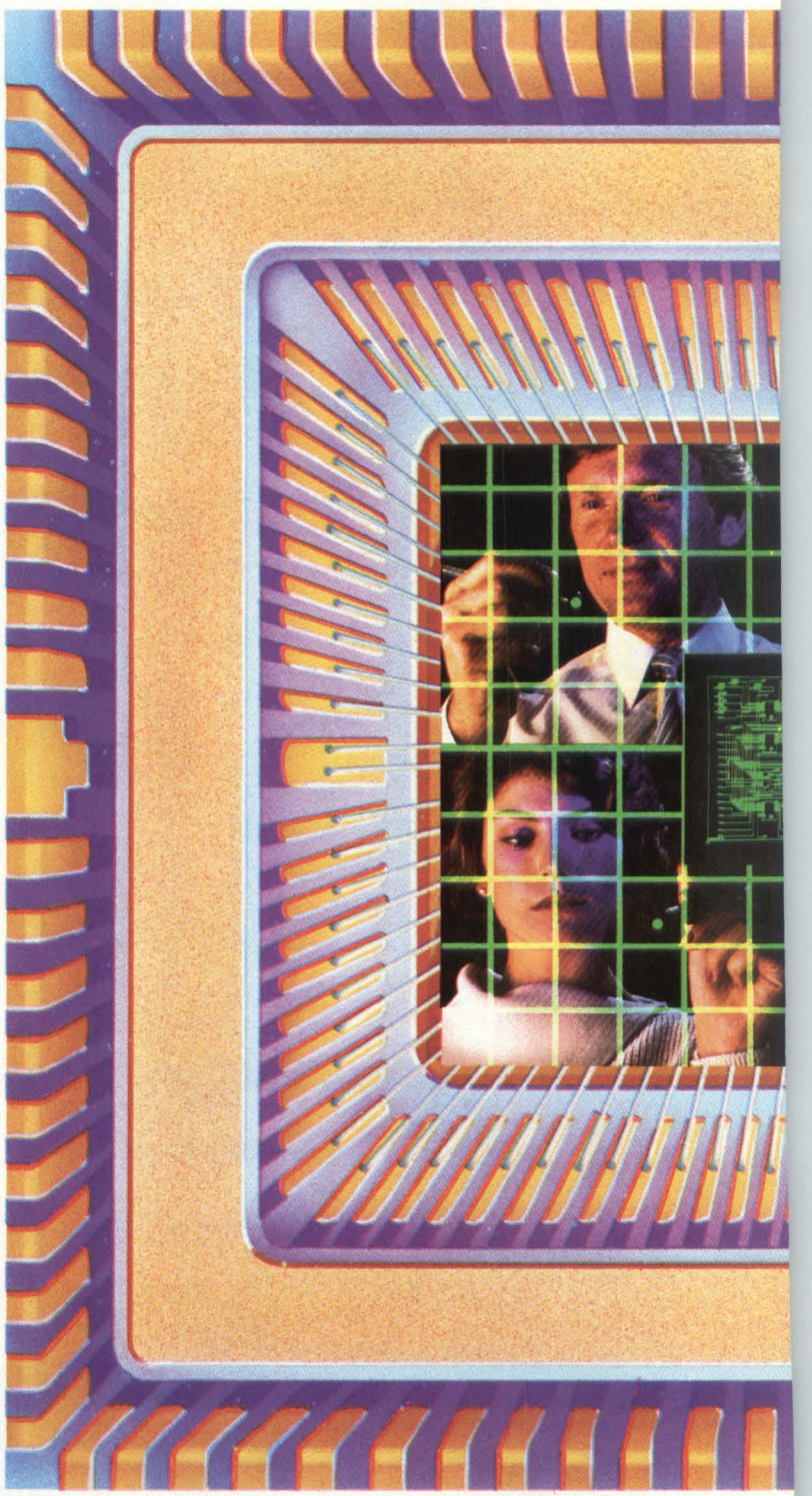
TECHNOLOGY	GATE LENGTH	PROP DELAY TIME*	GATE COUNT
STD CMOS	3.6 μ	7.0 ns	700-3900
H CMOS	2.8 μ	5.0 ns	440-3900
VH CMOS	2.3 μ	2.5 ns	2600-8000

*2-Input NAND Gate, F/O = 2

BIPOLAR

TECHNOLOGY	PROP DELAY TIME*	GATE COUNT	POWER DISSIPATION PER GATE
LSTTL	1.8 ns	500	2.3 mW
LSTTL	1.9 ns	240-1100	0.8 mW
LSTTL	0.95 ns	2000	0.65 mW

*3-Input NAND Gate, F/O = 1



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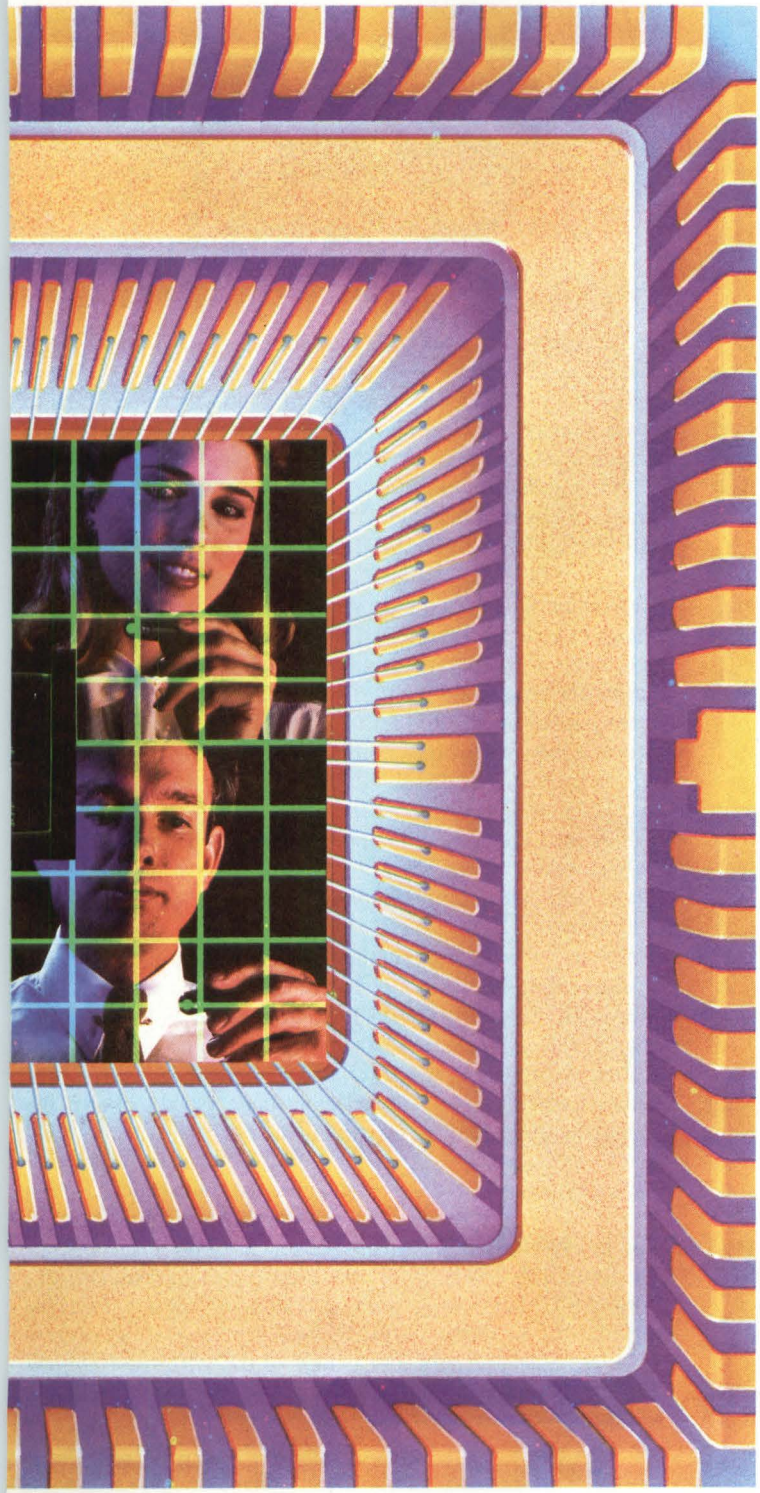

There are now three fully equipped Fujitsu Gate Array Design Centers in the U.S.; in Boston, Dallas, and Santa Clara. There's a sophisticated telecommunications network between centers, and high-speed leased-line and satellite communications with FMI host computers in Japan. All that, and a first-class gate array design team, too. With you as star player.

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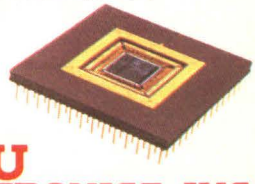

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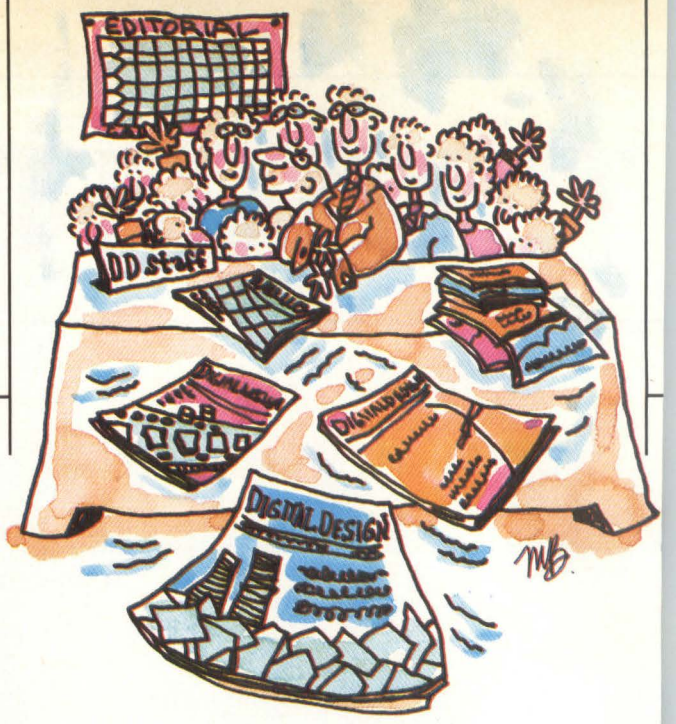
"Three additions to the editorial staff of *Digital Design* have recently been made with the intent of providing our readers with an even greater perspective on the industry."



EDITOR'S COMMENT

Keeping track of developments in the computer industry is no easy task for the systems architect or for an editor. Often a number of interrelated issues must be considered when conceiving and implementing a product. Most times, developments in one field cannot be viewed in isolation because they impact other areas of technology.

It was with this rationale in mind that the editors of *Digital Design* developed this year's editorial calendar. Five main subject areas will be covered in each issue; they relate to overall systems architecture, integration of peripheral devices into systems and applications of ICs, board level products and systems. In addition, our advanced technology series will examine those developments just starting to emerge from the laboratories in order to give our readers a feeling for what the future may hold.

To execute this task and still remain objective, *Digital Design* has been assembling a team of editors over the past two years who will be contributing heavily to this calendar. Today, we are the most comprehensive group of writers in the technical publishing field.

Over the past two years we have been given a charter to expose not only the options available to you but the problems you may encounter in your day-to-day work designing OEM equipment. Recently, three additions to the editorial staff have been made with the sole intent of providing even greater in-depth industry coverage. They bring to the magazine an experience that goes beyond that of simply reporting upon issues that affect the industry. In some cases, our editors are evaluating products and using and testing some of the same equipment that you are.

In November of last year, Brita Meng, our East Coast Technical Editor, joined *Digital Design* after completing a BSEE at Princeton University. This issue marks her first contribution to the magazine. In her article, "Design Options Increase For Users Of 256K DRAMs," Brita examines the latest parts on the market, their organization and addressing modes – important considerations in choosing the right devices for a particular application.

With the continuing development in Silicon Valley, the recent addition of our second West Coast Technical Editor, Joe Aseo, will prove invaluable. Over the past year, Joe has been working at a leading IC house. Prior to that he was based in Los Angeles as the West Coast Editor for *Computer Design* where he specialized in the area of disk drive and related interfacing issues. Joe brings to the magazine a BS in communications and is currently working on a BSEE in Computer Science. He will be working out of our Los Gatos office in Northern California and can be reached at (408)356-0405. He will join our other West Coast Technical Editor, Gregory MacNicol.

For his part, Gregory has set up a lab where he plans to evaluate many new product introductions in order to bring a greater level of objectivity to his writing. Gregory's involvement with the industry does not stop there. His enthusiasm for the graphics business has led to his election to a chair for SIGGRAPH and the SIGGRAPH conference in 1985. His position there will be to accept and choose the material for the art, technical and industry slide sets.

Closer to home, Ron Collett, our Senior Technical Editor, has started his work on the design of a gate array. In this issue, he begins the first of a three part series that will trace the design from start to finish. Ron will be using a Valid Logic workstation and the part (a cross point switch designed by Datacube) will be produced by LSI Logic. Those readers considering gate array design will gain considerable insight by reading a series that unveils the pros and cons of the semi-custom approach. Others who have already gone through the process using different vendor equipment may like to discuss their experience with Ron.

One important comment that we consistently hear from our readers relates to the objectivity of contributed articles to the magazine. Realizing that fact, Senior Editor Julie Pingry, in charge of the Applications Notebook, is making a push to solicit features from users, not just manufacturers of the latest ICs. Those readers who would like to contribute to that section of the magazine should call Julie in the Boston office to discuss their ideas.

Finally, it is my pleasure to announce that John Bond has been appointed to the position of Editor-in-Chief of *Digital Design*. For the past two years, John has been Senior Editor at *Computer Design*. John brings to his position extensive industry experience. He has held positions at General Dynamics, Texas Instruments and Digital Equipment Corp. as well as several leading trade journals. On behalf of the editors of *Digital Design*, I welcome John in heading up a team of individuals whose output is second to none.

David Wilson, Executive Editor

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UPDATE

Qume, AT&T Printer Contract

AT&T Information Systems has selected daisywheel printers from Qume Corp. to be integrated with their new business computers. The contract calls for deliveries of Qume's Sprint 11/55 Plus letter-quality business printers and accessories for AT&T's 3B Series of business computers and PC6300 Personal Computer.

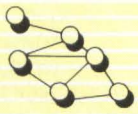
VTI, Lattice Cross License

VLSI Technology, Inc. (VTI) and Lattice Semiconductor Corp. signed a technology and product cross licensing agreement, under which VTI will receive alternate sourcing rights for very high performance EEPROMs, static RAMs and programmable logic devices currently in development by Lattice. In exchange, VTI will provide Lattice with wafer fabrication, assembly and test capacity, product engineering and equipment leasing support.

RCA Kicks Off JAN Qualification

A program to qualify 23 logic device types of the CD4000 "B" series for high reliability applications is underway at RCA Solid State. The JAN program will qualify the standard-product "B" series ICs to MIL-M-38510 Class B and Class S for inclusion on the Qualified Products List (QPL). It is expected that the logic devices will be on the QPL by 1985.

FutureNet, Augat Link



FutureNet DASH workstations can be used to directly link the electronic design engineer to the board level design and manufacturing services of Augat's Interconnection Systems Div. Information created on the workstation can be transmitted electronically to Augat's VAX computer systems for quick turnaround prototype fabrication of Wire-Wrap board. When additional production is required, the design engineer may choose to stay with Wire-Wrap, or to use the same FutureNet database to have Augat design, route, and fabricate boards.

DEC, Cullinet Development

Digital Equipment Corp. plans to integrate Cullinet Software Inc.'s Information Database (IDB) with its VAX family of computer systems. Under a development agreement, both companies will cooperate to enhance their respective information center and distributed database products in settings where Digital Equipment and IBM systems coexist. They also will cooperate to market existing products and develop new ones to improve communications and database interfaces between DEC's VAX/VMS-based family of management information products and those on IBM-based systems.

3M Purchases CD ROM Mastering System

3M has purchased from North American Philips Corp. its Compact Disk Mastering facility for mastering of Compact Disk Read Only Memory (CD ROM) disks. Both companies will jointly support CD ROM as an industry standard for optical Read Only Memory disks. The purchase coincides with a 100,000-square-foot expansion of 3M's optical media production facility in Wisconsin.

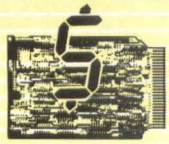
ITT Forms Multicomponents Division

ITT Components plans to expand into boardline electronic component distribution with the formation of a new division called ITT Multicomponents. The division will stock passive electromechanical and active components at the recently relocated and expanded headquarters in California.

Carnegie Selects Symbolics' Computing Systems

Symbolics, Inc., has sold 50 computing systems to Carnegie Group Inc. for use in artificial intelligence and other symbolic computing applications. Carnegie will use the systems for software development in two areas, PLUME and SRL+.

Intel Supplies Board-Level System



Intel Corp. will supply NetExpress Inc. with $10 million in single-board computers and memory boards for a worldwide image-transfer service, providing its iSBC 286/10 single-board computer and its iSBC 010 CX memory board. The 286/10 computer is based on the Intel 80286, a high-performance 16-bit microprocessor. The service will allow worldwide distribution of text and images to be distributed through digital signals via satellite or land lines.

Motorola Acquires CTX International

Motorola, Inc. has acquired CTX International to become part of its New Enterprises organization. CTX develops and markets information systems and software for semiconductor manufacturing and related industries. The goal of New Enterprises is to build new businesses in emerging high-growth, high-technology industries.

Mostek offers IPI Operating Systems

Industrial Programming, Inc. will integrate Mostek Corp.'s 16-bit MK68000 and 8-bit MK3880 microcomputer systems with several versions of its real-time, multi-tasking MTOS operating system. Both companies will cooperate to offer design and development support so computer system integrators and designers, software developers, and end-users may use a single source for 16- and 8-bit microcomputer hardware and real-time software.

Remote LANs Interconnection

Vitalink Communications Corp. and Digital Equipment Corp. will cooperatively market TransLANs, a hardware/software product that transparently connects LANs via satellites and/or terrestrial lines. TransLAN is designed to connect several Ethernet or IEEE 802.3 LANs so they appear as one large network. LAN information sent to remote sites is automatically forwarded across the digital transmission network in a data-link-layer relay that screens and forwards information to protect the LAN and transmission system from unnecessary traffic.

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WASHINGTON REPORT

by Anne A. Armstrong

SCSI Standard Nearing End Of ANSI Approval Process

Racing to complete a new standard for hooking up intelligent peripherals to small computers before the industry bypasses the process and adopts one of its own, the American National Standards Institute's subcommittee, X3T9.2, has finished the second version of the 14th draft of the Small Computer Systems Interface standard and sent it out for the 4-month publication and public comment period.

An arduous task of reconciling many different ideas and needs, standards drafting frequently takes years to do properly—years in an industry that has become so fluid that a whole generation of equipment may last only two or three years.

"The market will not wait for the ANSI standard," said William Burr, chairman of the subcommittee that has been working on the SCSI standard. Manufacturers will go ahead with products even without the standard, but it is better for customer confidence if the public knows that there are not going to be 10 different versions of products that will not work together, he told us. The proposed SCSI standard is based on a Shugart Corp. interface that was used in 1982 as a starting point for writing a standard to connect intelligent peripherals to small computers, but with the power and flexibility of the input/output channels found in large mainframe computers.

Since the interface can handle large amounts of data very quickly, the adoption of the standard is also expected to prompt greater use of VLSI chips in future computers and peripherals. Interface chips and disk controller chip sets that support the proposed SCSI standard have already hit the market, even though formal approval of the standard is six months to a year away.

"You can always tell when a standard is catching on," said Burr," "because the connector firms start showing up at meetings. At the last SCSI meeting, the connector houses were out in force."

Burr believes that most problems with the SCSI standard have been ironed out in committee and he does not foresee any serious opposition during the public comment period. One possible exception would be formulating standards for cache disk controllers, although Burr said that is likely to be handled in a supplementary document, rather than holding up the primary standard while it is written.

The SCSI is only one of 22 standards that are in the works at X3, which is the information processing committee of ANSI. Coordination and support for the work is handled by the Computer and Business Equipment Manufacturers Association, which acts as secretariat for the X3 committee. Other X3 subcommittees are working on a whole stream of intelligent peripheral interface standards that cover specific and generic command sets for a variety of storage devices, including optical and magnetic disks.

Signetics Chips Also Found With Testing Irregularities

Just as many contractors were beginning to finish the paperwork necessary to have shipments containing suspect TI chips resumed, the industry learned that similar source control drawing chips from Signetics also had testing irregularities. Signetics was reportedly a second source for TI chips and so many companies with systems that had just been cleared of problems with TI chips, found they were on hold again until the second problem could be resolved.

The Defense Logistics Agency outlined in its alert to prime government contractors that some 2,300 different Signetics semiconductor devices dated from January 1981 to the present could have been improperly tested. More than 250 contractors are said to be involved.

The embargoes of many weapons systems have created chaos in the industry and have prompted several trade associations, including the Aerospace Industries Association and the Electronics Industry Association, to look for solutions other than the stop shipment approach now employed by Defense.

An EIA spokesman told us it is the association's policy not to get involved in questions between buyer and supplier; however, the stopping of whole shipments in which there are suspect parts has become a big problem plaguing OEMs currently. "DOD is penalizing a lot of innocent people," he said. "We are trying to find a way to cope with the problem and avoid the disadvantages of stop shipments."

Charged with the job of finding other solutions is a task force of industry experts, headed by Mike Michaelis of General Dynamics. At press time, no specific suggestions had been made public; however, the group has been meeting with Defense officials to discuss ways of handling suspect parts.

While negotiations are going on, most contractors have been working with Defense officials to get waivers for specific systems. Although the procedures being followed are up to each government agency, several contractors report that they have been able to get waivers on retesting TI chips if they can show that they performed 100% inspection tests on components before they were included in a larger system. Others have offered to warrant the system regardless of the chips in question.

It is too early to tell how great a financial impact the systems embargoes will have on the prime contractors. Sperry Corp., however, did cite the delay of defense shipments as one reason for a decline in profits in its quarterly statement. Texas Instruments—whose chip testing failures started the whole mess—reported a profit of almost $86 million in the third quarter, ending Sept. 30. However, even the $13 million loss in this quarter's figures that TI attributes to the chip testing problem looks good compared to the $110 million loss in the third quarter a year ago as the company was getting out of the home computer business.

Defense Restricts Publication Of Technical Data

In a follow-up to a decision made more than a year ago, Secretary of Defense Caspar W. Weinberger has signed a directive (#5230.25) that restricts the publication of certain technical information and establishes a tiered system of data classification ranging from no release to full disclosure.

Exempted from the new regulations would be most academic and research centers conducting "fundamental research"; defense contractors, on the other hand, would be required to become certified to receive the unclassified, but "sensitive" data. Contractors would have to agree to protect the information and see that it is not released to anyone without DOD permission.

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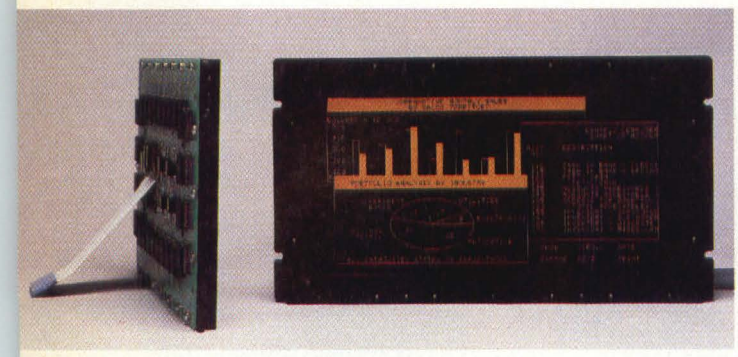
Electroluminescent Development Pays Off In Thinner Commercial Flat Panel Display



The Planar EL6648 MX can display 256 × 512, though a total system is only ¾" thick and weighs 16 ounces.

Flat panel displays have long been an area of great interest, particularly with the trends toward shrinking footprints and portable computers. But the expense of driver electronics and problems of resolution and viewability have largely prevented flat displays from penetrating the commercial market. The use of custom ICs and surface mount devices (SMD) has allowed Planar Systems (Beaverton, OR) to reduce the size of their electroluminescent (EL) display by 50%; the EL6648 MX is .75" deep × 5.7" high × 10.3" wide, including the driver and control electronics, bezel, frame and panel.

Though Planar is only one year old, their product is based on development begun in 1976. The firm was founded in 1983 by former Tektronix (Beverton, OR) employees when Tek decided it would not set up facilities to manufacture EL displays. Like their EL6648 M introduced last year, the EL6648 MX has a 256 × 512 pixel matrix, for 80 columns and 25 rows using a 5 × 7 matrix for characters. New drivers and insulators have improved reliability. Meanwhile, automation and increased quantity runs are improving the manufacturing process. The price of the new EL panel is $775 in quantities of 1000, and it is available this month.

Other firms working on this resolution EL display are Sharp (Tokyo, Japan, with US offices in Paramus, NJ) and Lohja (Finland). Lohja has not yet shipped. Sharp's product is used in Grid System's portable computer, but the Japanese system uses five boards compared to the one board in Planar's new product.

Electroluminescence is only one technology for making flat panel displays. Efforts to make thinner CRTs cannot solve the problem of curvature. Liquid crystal (commonly used in watches and small clocks) and plasma displays make thin, flat displays. Plasma displays are high quality, but heavy; they require more power than is desirable for portable or smaller systems. Liquid crystal panels are non-emissive, so legibility depends on ambient light. In addition, they are relatively difficult to address. An advantage EL has over the other two is that it is solid state, ideal for harsh environments.

Liquid crystal technology is popular for small screens needed to relay only a few characters due to its extremely low power consumption and relatively low cost. Plasma displays are more easily enlarged than the others, so their cost may not prevent them from finding applications in large mainframe-level systems. An intermediate marketplace including mobile and harsh environments appears open for EL panels as they develop.

One aid to acceptance of the EL6648 MX may be that it is designed to work with CRT controllers. The board in the system converts a standard CRT controller's signals to signals needed by the flat display. For graphics, each pixel is individually addressable. The device requires 768 drivers (512 × 256) which, until recently, was an expensive proposition. Planar uses Texas Instruments (Dallas, TX) drivers that now cost $0.11 per line, compared to $1.25 18 months ago.

In addition to the cost of drivers, EL panels have suffered reliability problems due to a lack of uniformity in the glass insulator layer. A proprietary process for depositing the insulator has improved the efficiency and reliability of that layer greatly.

Since flat panel technology is often chosen to reduce size, the fact that the volume of this display is 5% that of a standard CRT with the same usable display size may prove critical. Fitting all of the electronics onto a single circuit board has allowed that size, a reduction in volume by half over the model they introduced last year. Surface mount devices and custom ICs are used extensively in the EL6648 MX.

Another important factor in the thinness of the Planar display is the interconnect system. The driver board and panel both have gold contact patterns that are interconnected by a gold-plated, metal-on-elastomer connector. Clamped pressure contacts have proven not only resistant to environmental effects, but also easy to assemble and dissassemble for on-site repair.

Planar is devoted exclusively to EL display manufacture and plans for future developments include a full page display (scheduled for before mid-year), capabilities for two colors, and in several years, full color. Improvements in brightness, lower power consumption and lower costs are also in the works. The firm claims to be the only EL manufacturer offering custom configurations.

If all continues to develop well, hostile environments as well as mid-range systems in which a flat, thin display is desirable may be well served by EL displays. Planar has been shipping some of the older model panel already and with the product improvements, more may follow.

Price has been a major barrier for EL displays. Because the panel technology, SMDs, drivers and interconnect scheme are new, the downward curve for costs must take place. But as a solid-state product, the ongoing developments in electronic components will likely continue to help prices and availability of EL technology-based products. *—Pingry*

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Test Equipment Manufacturers Unite With Workstation Vendors

Caesar, from Dolch Logic Instruments, is an upgraded version of the firm's Atlas 9600 which can be linked to a workstation or function as a standalone system.

Since the introduction of the first workstations in the early part of the decade, workstation vendors have sought to provide the systems architect with the complete design solution. Taking an objective view of these systems, most users agree that they do an adequate job at facilitating the front end of the design cycle (i.e. schematic capture, simulation, verification) as well as presenting a hierarchical partitioning of the design. However, the integration of test capabilities into the workstation seems to have been put on the back burner.

As a result, a new breed of agreements between test system manufacturers and workstation vendors has emerged. New hardware and software which links existing workstations to test equipment is surfacing. For instance, Integrated Measurement Systems (Beaverton, OR) recently unveiled the Logic Master I & II which provides 40 MHz functional test capability to workstations such as those from Valid Logic (San Jose, CA), Daisy (Mountain View, CA), and Apollo (Chelmsford, MA). (For a more complete description of the Logic Master I & II, see *Digital Design*, November, 1984, p. 30).

Unlike IMS, whose systems are targeted for functional testing of prototype chips, Dolch Logic Instruments (San Jose, CA) announced Caesar (Computer Aided Engineering System Analyzing Resource) which is an upgraded version of their Atlas 9600 and focuses on test analysis via test instrumentation. At the hardware interface level, Caesar has a GPIB interface, an RS-232 port and an Ethernet interface. (The software supporting the Ethernet will not be available until mid 1985.) The basic difference between Atlas and Caesar is the number of instrumentation slots in each system; Atlas has two slots, while Caesar offers four. Plug-in instrument modules are available for word generation, data acquisition, logic analysis, signature analysis, waveform analysis and emulation for microprocessor development. In essence, Caesar provides the user with an integrated test and measurement cluster which can be tied to CAE Systems' workstations.

Other differences between the two systems are the user interfaces, the optional imbedded CP/M-based computer and the physical packaging. Atlas is built around a CRT display but since Caesar works in conjunction with a workstation, the user interface is the workstation's display. Atlas also comes equipped with an imbedded CP/M-based computer system. With Caesar, however, users have the option of purchasing the system with, or without the computer. As far as the physical package is concerned, Atlas is a benchtop system whereas Caesar is a floor unit.

In conjunction with the unveiling of Caesar, Dolch also announced a joint technology agreement with CAE Systems (Sunnyvale, CA). CAE Systems, a workstation manufacturer, offers Apollo-based systems which focus on the needs of the electrical engineer. According to Dolch, Caesar can be directly interfaced to CAE's model 2000 workstation. CAE Systems' President, Phillips Smith, commented that "the intent of the agreement with Dolch is to develop a fully integrated system for design automation and test."

Another joint development agreement recently announced comes from Daisy Systems and Factron (Billerica, MA). (Factron was formerly known as Fairchild Test Systems). The first product from the Daisy-Factron venture is a software interface package that provides a link between Daisy's workstations and Factron's test systems. The new package allows system engineers to capture simulation data that is generated in the design phase to be translated into a test program to be used in the debugging or production stage. Dave Stamm, Executive VP of Daisy noted, "the link between Daisy and Factron is a significant event for the design and test engineering communities since it will provide a sizeable reduction in the total design-to-manufacturing cycle."

Judging from the recent introductions from the various test and workstation manufacturers, it appears that the long awaited interface between the two disciplines has arrived. The result of the merging fields will undoubtedly bring about a significant improvement of efficiency. Finally, these first introductions are likely to be just the tip of the iceburg, a host of other workstation and test vendors will surely aim to secure a piece of this huge market. —*Collett*

Integrated Measurement Systems . . . . . **Circle 231**
Valid Logic . . . . . **Circle 232**
Daisy . . . . . **Circle 233**
Apollo . . . . . **Circle 234**
Dolch . . . . . **Circle 235**
CAE Systems . . . . . **Circle 236**
Factron . . . . . **Circle 237**

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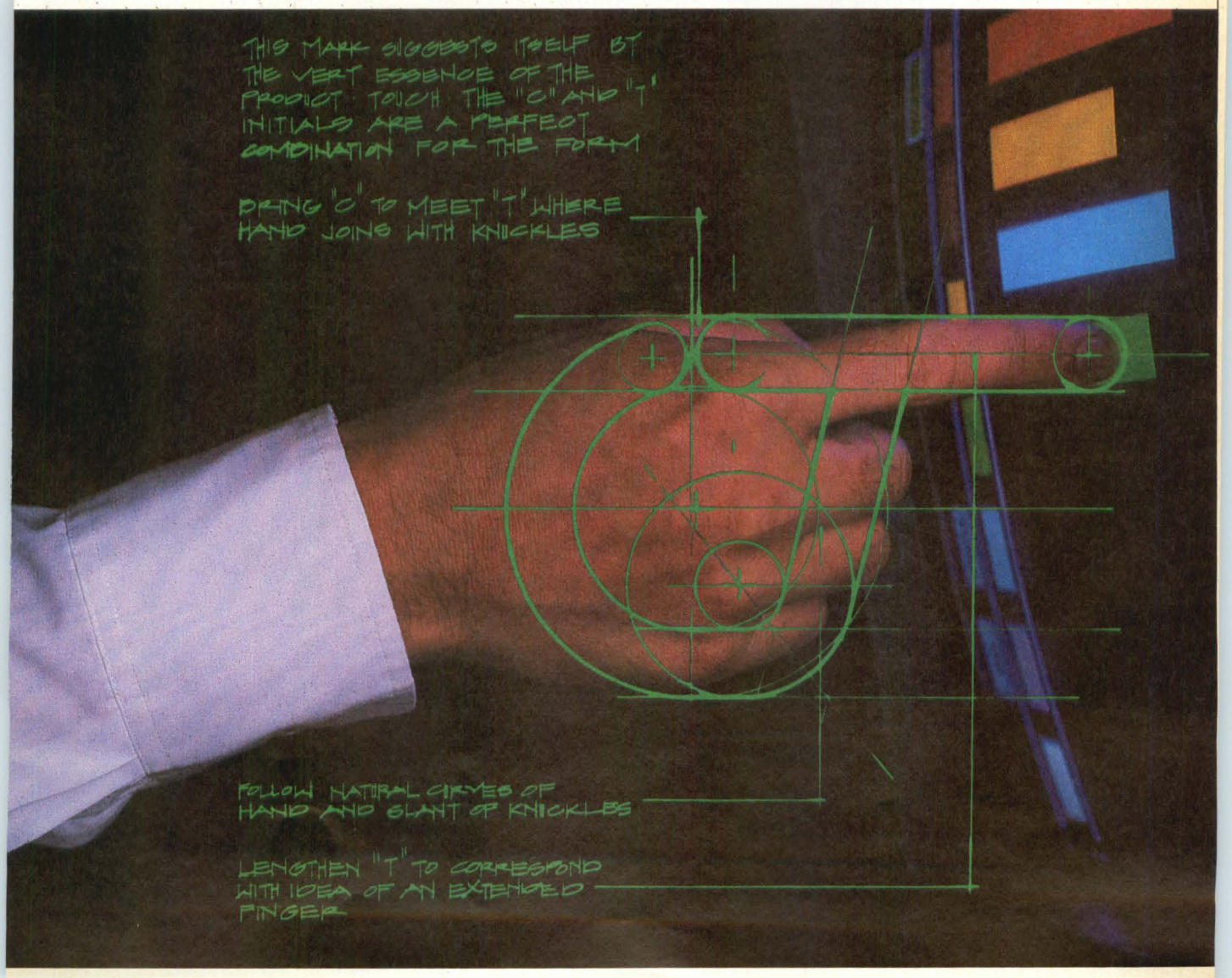


Options For Implementing LAN Protocols Before Standards Gel

Thanks to the IEEE 802 committees, most of us now understand what a local area network (LAN) is and the standard hardware implementations available. Unfortunately, the difficult part of LAN standardization is still underway. The question of what software protocols to use has several answers with strong arguments for each.

The main options for LAN communication software are: to implement custom protocols optimized for the specific equipment offered and provide bridges and gateways to other networks; to offer Xerox XNS protocols, which are relatively well defined and available; to use TCP/IP, developed by the DOD for ARPA, also well documented and available; and to implement ISO (NBS supported) standard protocols, still being defined, but available in subsets adequate for basic LAN communication. If the network is specifically for MS DOS PCs, Microsoft's (Bellevue, WA) Networks is the emerging standard. Further possibilities are X.25 and IBM's SNA, but they are not designed specifically for peer-to-peer communications in a local area.

There are examples of success with all of these options. Implementing any set of network protocols takes a good bit of work. Standards do not specify exact implementations, leaving the designer both the task of implementation and the possibility of incompatibility even with others using the 'same' protocols.

There is general agreement that a layered approach, as in the ISO's seven-layer OSI (Open Systems Interconnect) model, is desirable. One advantage is that each level is directly dependent on only the next lower layer; this allows various low layer (physical, access and link) network types to use common software. It also means that changes or variations in implementation at one level may require only localized system revision.

A brief description of the functions of the ISO network layers, and how different protocols currently address them is shown in **Table 1**. Note that there are several gaps in the ISO network at present; within a few years, most of these will no doubt be specified. XNS has no defined Session level, and DOD has specified only one set of protocols for layers 5-7. The NBS demonstration at NCC this summer similarly used a null implementation of level 6.

Other important facts are that TCP/IP is designed as part of UNIX 4.2 BSD, but was originally conceived as a wide area network protocol set (for ARPA in the Defense Department). XNS has very well defined and developed internetwork-

ISO OSI Model Protocol Level Number: Name: Description	International Standards Organization (ISO)/ANSI		National Bureau of Standards (NBS)	DOD ARPAnet (TCP/IP)	XEROX XNS	IBM
1: Physical: Electrical, mechanical, functional control; topology of net	IEEE 802 Stds (802.3, 802.4, 802.5)		NBSNet/IEEE 802		Ethernet (IEEE 802.3)	Token ring (no spec published)
2: Data Link: Medium access, logical link control, some error and flow control	IEEE 802 (2 levels: MAC & LLC. LLC1	LLC1 or 2			Ethernet (IEEE 802.3 & .2)	?
3: Network: Routing, switching, internetworking, error recovery, flow control	Connectionless Protocol (CLNS) Internet	CCITT X.25 Connection-Oriented (CONS)	ISO connectionless protocols	Internet Protocol (IP) (ARP for address resolution)	Internet Datagram Protocol	?
4: Transport: End-to-end transparent transfer, control, mapping, multiplexing on the internet	ISO Class 4 Transport	ISO Class 1 Transport	ISO Class 2 & 4 Basic & Enhanced Transport Protocol	Transmission Control Protocol (TCP)	Sequenced Packet Packet Exchange Routing Error	LU 6.2 (SNA compliant)
5: Session: Control and administration of data exchanges between two points, esp. longer-term connections	Session Protocol (approved standard late 1984) Kernel requires specification of 2- or 1-way simultaneous; implementation open, features likely to be added still		ISO kernal using 2-way simultaneous data delivery	File Transfer Simple Mail Transfer Trivial File Transfer	none (some password functions by Authentication listed in 7)	?
6: Presentation: Format and code conversion so all devices appear the same, for location independence; syntax	early draft standard now; may have 2 parts: negotiation of semantics and standard data objects or types being sent		Use null implementation until ISO std. is final	Name Server TELNET	Courier (closed set of data objects)	?
7: Application: User interface and applications, as well as management	FTAM in works (File Transfer, Access & Management); Simple File Transfer now	CCITT X.400 Message Handling recommended as a working subset, X.409 for syntax	ISO standards		Clearinghouse Authentication Interpress Time	?

Table 1: The seven layers of the ISO OSI model, and how various standard protocols address each.

New PC display system reduces down-time, increases productivity

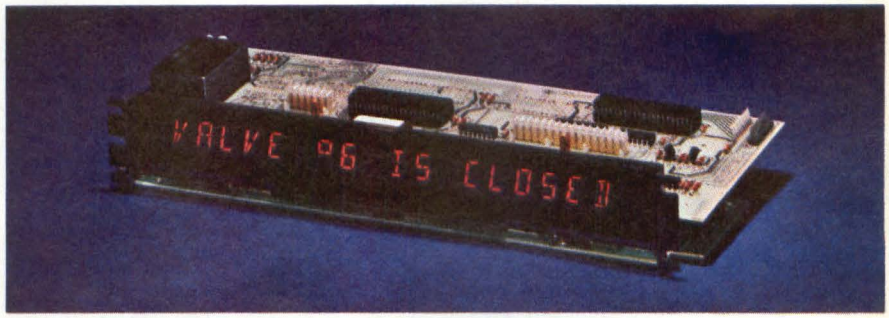
F. A. Amendola
Cherry Electrical Products Corp.
Waukegan, IL

Cherry unit adds diagnostics and operator prompting in understandable printed messages to any programmable controller. Cost: less than $300

If your programmable controller is not equipped with a serial ASCII output port, you may not be realizing all of its potential productivity. In its present state it is unable to output information for operator prompting or provide diagnostic information in immediately understandable messages for your maintenance staff. Of course the information is being supplied by your PC, but in the form of signals or shut-offs or complicated codes.

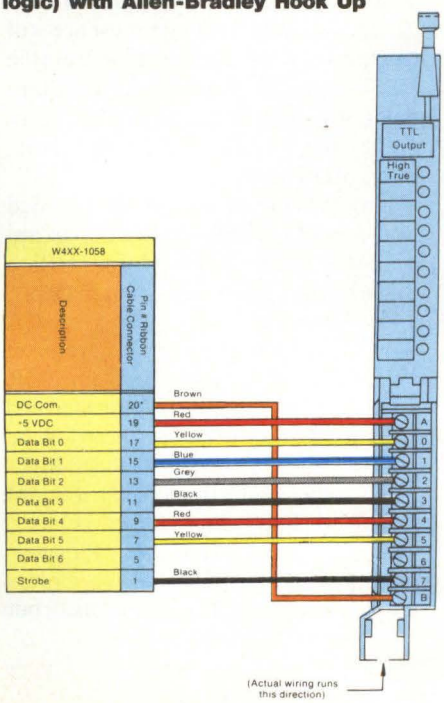
The new Cherry display system literally adds literacy to any programmable controller with TTL output drivers, 5 VDC. Instead of using cumbersome look-up tables to translate output codes, your operator is given any of up to 64 messages of up to 32 characters each, spelled out on a bright, easy-to-read display panel. A flashing mode attracts attention to potential trouble such as slipping belts, stuck valves or overheating. Your operator is constantly and instantly supplied with pertinent, *understandable* information about all critical phases of production under your host system's control.

At a cost of less than $300 in OEM quantities this new unit compares with others costing over $1000. It is estimated that the addition of this Cherry display system to your host system will pay for itself in just a few months by decreasing frequency of down time, in improved maintenance and increased machine efficiency.



Cherry No. W424-1058, 24 character display system complete with all on-board electronics.

Typical configuration (positive logic) with Allen-Bradley Hook Up



Easy to install— a complete message center

You just connect two color-coded cables (one power and one signal) and the Cherry unit is ready to take the PCs output drivers and provide output decoding of up to 64 easily programmable messages...anything from "BIN 4 EMPTY" to "ET PHONE HOME." No hardware changes or additions.

This new Cherry unit is a piece of straight-forward engineering consisting of complete on-board electronics and a flat gas discharge display panel of 24 half-inch high characters in bright orange easily readable in any ambience. (Longer messages may be scrolled.) Unit has built in capability for longer scrolled messages and a flashing mode.

Sample Program (message: VALVE #6 IS CLOSED) Starting location HEX 000

HEX CODE	DESCRIPTION
10	Blank Display—all messages must start with this
0A	Line Feed—clears display
0D	Carriage Return—puts cursor to far left
12	Display Recall—turns on display
56	V
41	A
4C	L
56	V
45	E
20	Space
23	#
36	6
20	Space
49	I
53	S
20	Space
43	C
4C	L
4F	O
53	S
45	E
44	D
89	All messages must end with this

Complete information and specs available

Cherry will send you an 8-page instruction booklet that includes typical connections to various PCs plus application notes on sample programs and ribbon cable connections and Hex Number Addresses for messages in user's EPROM. Send for it today.

ing protocols, since it was designed as a protocol for Ethernet and the need for interconnections between LANs is apparent. It is not, however, as easily used with UNIX systems as the ARPA protocols.

One advantage of implementing a standard protocol package is that hardware (network controller boards and cable schemes) can be from several sources. The range of functions and costs for hardware is broad, and particular machines may perform best with one board or another. And while boards to certain form factors like the Multibus are available from many sources, others are not so common.

On the other hand, if a network is to be a complement to an OEM line of computers, a proprietary approach may offer room for optimization. Most major computer vendors do offer specialized networking. Apollo Computer's (Chelmsford, MA) Domain is an example of an effective non-standard network. They contend that most LANs are of limited scope to link a small group of people and internet gateways are adequate for other communications. With an operating system designed for networking, their overhead is minimal. But not many system houses are going to begin from the ground up building software.

A traditional method of implementing a local area network is to get a hardware/software end-to-end solution from a turnkey network vendor. This may be the best answer for systems that need to be on the market or installed soon with networking. These turnkey LANs may use proprietary protocols. This means that computers supported by that network vendor and equipped with the firm's hardware and software, can communicate.

Some leading firms in this field are Ungermann-Bass (Santa Clara, CA), Sytek and Bridge (both of Mountain View, CA), Concord Data Systems (Waltham, MA), and Proteon (Natick, MA). Another group of firms provides the same service specifically for microcomputers. Several hardware companies now offer software as well, including Interlan (Westford, MA) and Excelan (San Jose, CA). Significantly, lower-level protocols are now put in firmware on their boards. This reduces the protocol overhead on a system.

Those wishing to have options as to what LAN controller boards they use as well as what computers are connected in the same network, can use standard protocol packages. Companies leading the network protocol software field are ACC (Santa Barbara & Soquel, CA) and Network Research (NRC) (Santa Monica, CA). Xerox offers their XNS licenses, and specifications for ISO, TCP/IP and X.25 are also readily available.

Until ISO protocols are completely specified, XNS and TCP/IP will likely gain ground. Both ACC and NRC now offer TCP/IP and XNS for Ethernet, though originally NRC began with TCP/IP, while ACC originally focused on XNS. These focuses are still apparent, though recent announcements have expanded both NRC's Fusion and ACC's ACCES protocol families.

The most recent version of Fusion, 3.0, will run XNS or TCP/IP protocols with DEC VMS, as well as UNIX, VENIX and MS-DOS. Fusion services to the user include file transfer, remote execution, virtual terminal and internet routing. This version also accommodates newer interface boards (*Digital Design*, November, 1984) with on-board intelligence: the 16K kernel can be relocated to an Excelan or Communications Machinery (Santa Barbara, CA) intelligent board. NRC points out that this leaves only 2K in the host for interface to the board.

Additions to ACC's ACCES protocols for VMS and UNIX are a file management system and a virtual terminal service. These are actually utilities to the application level software. The file management sits on Courier (which ACC describes as XNS's Presentation/Session level), so it is specific to that protocol set. File attributes are permanent, so although each host may use the format it requires, a file transferred back to the originating machine will be restored with all its features. The virtual terminal package decouples local service from the remote server. Not only the terminal, but also the host is virtual through servers. Users thus always see a computer's native user interface and formats.

An important aspect of ACC's XNS is that it implements the Courier protocols at level 6 fully. Most current offerings of XNS protocols use a null or minimal implementation of that level. Incomplete sixth level protocols usually mean networking puts a burden on applications programs. Just as others have incomplete XNS packages, ACC is still working on completing TCP/IP.

Most suppliers of current standard protocols plan to also support ISO protocols when they are complete. And some have implemented all of the available specifications, with best guesses until then. Concord Data Systems, for example, supplier of the only 802.4 compatible broadband token passing hardware, uses ISO protocols.

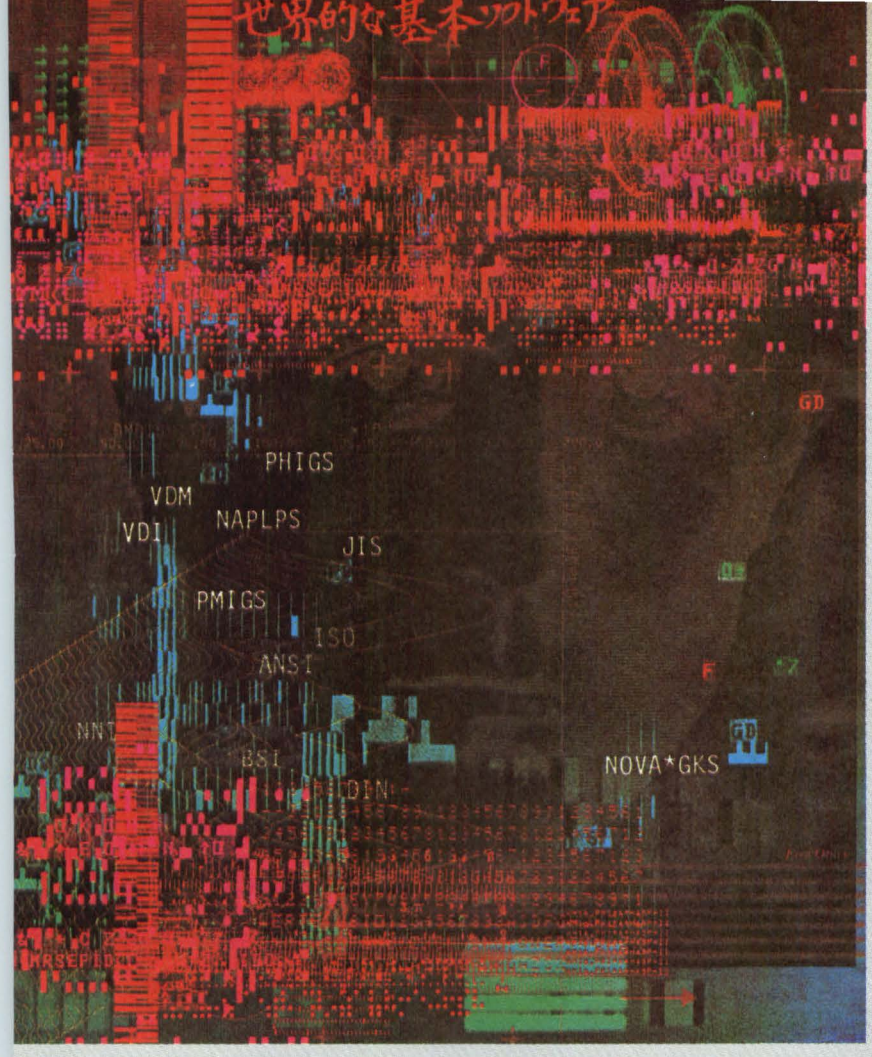
As CDS's Manager of Software Engineering, Dave Thompson, points out, current ISO protocols are adequate for loosely coupled networks. Tighter coupling will demand standards for internet as well as transport functions. Meanwhile, ISO networks use a null implementation at the Presentation level and a minimum subset at the Session level.

The demonstration of ISO protocols at an NBS-sponsored booth at July's NCC shows that current standards allow multivendor communication. Applications sit on a subset of level five protocols. The broad base of support for ISO means that finalizing standards may take quite a while, but the advantages are great. For one, the NBS is developing tools to test and verify protocols. The resources required for testing are often not feasible for a single company.

To implement the standard ISO protocols, specifications are available from: ANSI (American National Standards Institute), Information Processing Systems Dept., Attn: Joan Gardulski or Lisa Rajchel, 1430 Broadway, New York, NY 10018. A list of currently approved standards is available, though most are still unapproved drafts. Information from the NBS is available from Center for Computer Systems Engineering, NBS, Technology Building Room A 231, Gaithersburg, MD 20899.

If more complete protocols are needed immediately, XNS specifications are available from: Xerox Corp., Office Systems Div., Ethernet Literature Dept., 3450 Hillview Ave., Palo Alto, CA 94304. For DOD protocols, request MIL-STD-1777 for IP, -1778 for TCP, -1780 for File Transfer, -1781 for Mail and -1782 for Telnet protocols (these are the portions that have been adopted as MIL-STDs; others have limited distribution) from Naval Publications Informs Center, Code 3015, 5801 Tabor Ave., Philadelphia, PA 19120, (215) 697-3321. Orders are taken by phone, telegram or mail, but the preferred method is by form DD 1425.

—Pingry



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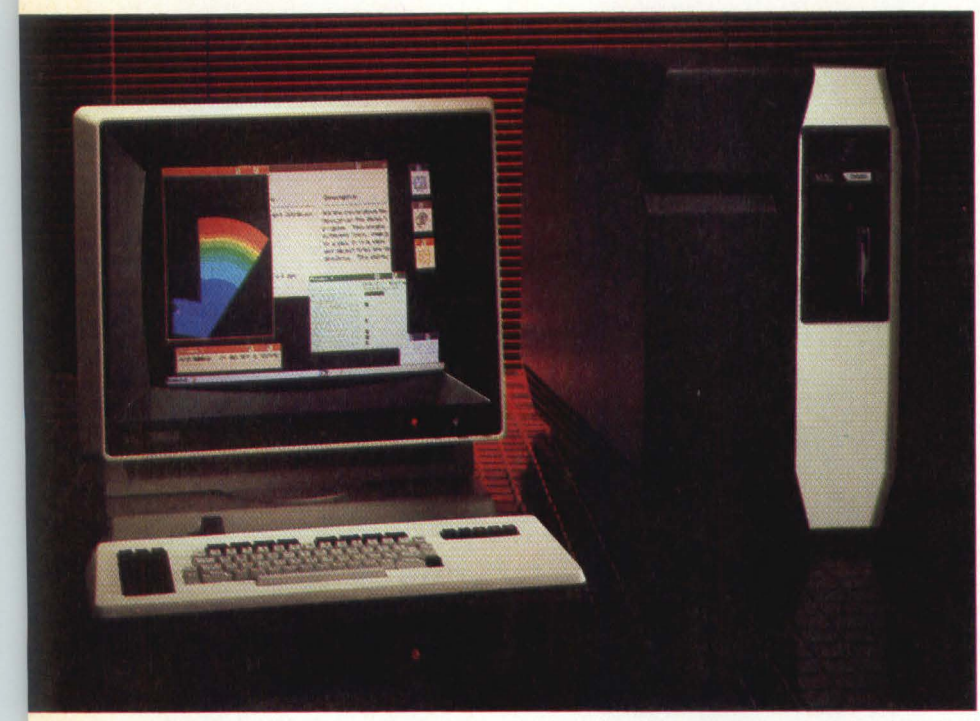
Circle 19 on Reader Inquiry Card

A Graphics Architecture For Apollo's Workstations



The Apollo DN550 incorporates the Graphics Metafile Resource (GMR), a software package providing a sophisticated set of graphics capabilities.

Intended to work with Apollo's entire family of workstations, the Graphics Metafile Resource (GMR) is a software package providing a sophisticated set of graphics capabilities designed for high throughput. The target host, the DN550, is a 68010-based workstation with a dedicated bit-slice processor for graphics. Display resolution is 1024×800 pixels at 256 displayable colors. It comes with 3 Mbytes of main memory and 2 Mbytes of double buffered display memory. The 550 supports both their own AEGIS virtual memory operating system and AUX, Apollo's implementation of UNIX system III with Berkeley extensions. The GMR package is included as a standard feature with all Apollo workstations.

The GMR is a graphics architecture that supports emerging graphics standards such as the Graphical Kernal System (GKS), the Programmer's Hierarchical Interactive Graphics Standard (PHIGS), and the Virtual Device Metafile (VDM). The reason why the GMR is compatible but not an emulation of these standards, is because each standard lacks important features that are required for advanced graphics applications. The software was developed to maximize graphics throughput using hardware for system calls as well as integrating the most common graphics functions into one package.

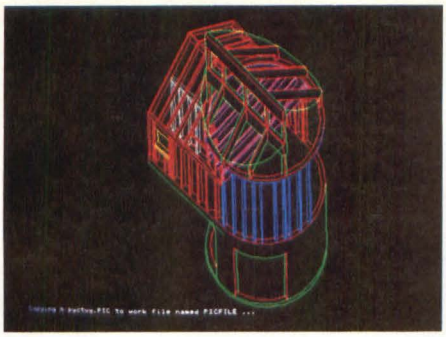
The GMR is an addition to their Domain Graphics Resources (DGR) which provides a set of graphics support tools. The GMR is based on the Siggraph Core functions including capabilities for 2D and 3D graphics. While Core capabilities are good for smaller graphics programs, it is not recommended for large, interactive applications that require speedy transformations of complex graphics images. The primary role of the DGR is graphics primatives and I/O management.

The Metafile, a virtual file capable of storing up to 256 Mbytes of world coordinates, is the heart of the GMR. It is a tree structured database with editing capabilities and integrated graphics primatives. The integrated structure of the GMR is responsible for its speed optimization. The architecture allows graphics data in the metafile to be shared among any workstations within a Domain local area network. This also means that data from a schematic done on a logic layout system could be used by a board test program. The GMR's segmented graphics database supports nesting and instancing. Nesting allows segments to contain other segments for creating larger bodies, while instancing makes efficient use of storage of repetitious data by changing only the attributes of the data. In addition, non graphics data can be stored with the graphics database such as comments.

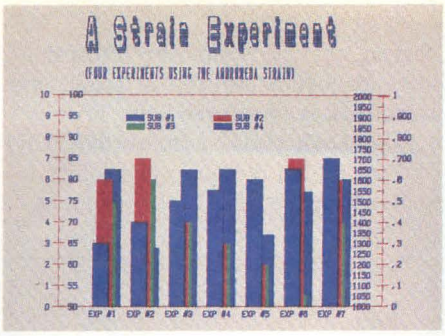
Graphics data in the metafile can be displayed in multiple viewports within multiple windows. Any changes in world coordinate data are reflected in all views. For example, if a user were to position an object in front of another object by dragging it across the screen, the object being moved would be seen in all the views displayable. Translation, rotation, clipping, and scaling are all viewable using active windows.

The GMR can accept world coordinate data in 16-bit or 32-bit integer words, in addition to single precision floating point. Single icons may require 16-bit integer, while complex IC diagrams may require 32-bit integer data and both data sets can be used together.

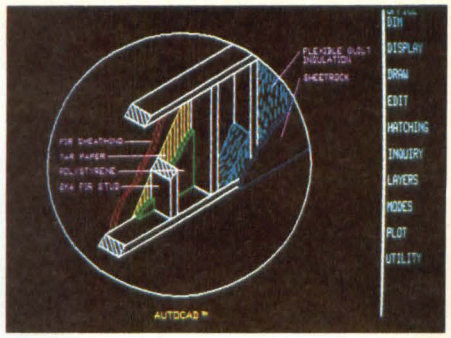
Because there is a lack of general agreement of standards in computer graphics, manufacturers must still create their own formats. Plot-10 is old and limited but has many applications packages. This is supported by the GMR. GKS is gaining momentum as a graphics standard but provides only simple, not nested, segmentation. It is also limited to 2D. Core, proposed by Siggraph, has some industry support but is being eclipsed by GKS. PHIGS is advanced and sophisticated but is still in the proposal state. The GMR is a result and embellishment of these emerging standards. Still, there remain limitations. The VDM is intended for 2D storage of graphics data for plotters and printers and contain no structure. Although it is not intended as a database, GMR metafiles could be converted to VDM files but the initial release does not provide that capability. Initial Graphics Exchange Standard (IGES) is a popular standard for transferring 3D database information in CAD systems. Until GMR is extended to 3D, it will not be incorporated. The present version of the GMR, however, does provide formats for I/O to external files. Input to the GMR allows input devices such as a mouse, graphics tablet, or switches. Bitmaps created on the screen can be dumped for hard copy output.



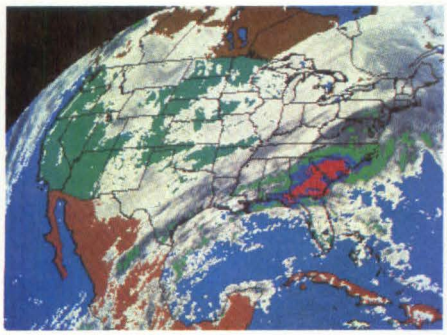
1. High Speed (MicroCAD Software)



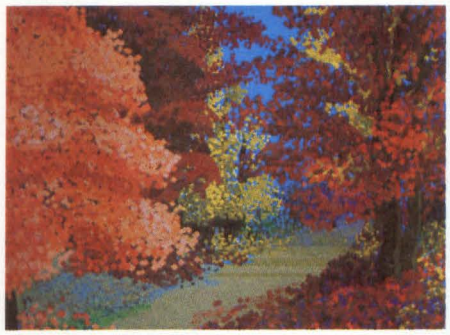
2. Dual Display Modes (Energraphics Software)



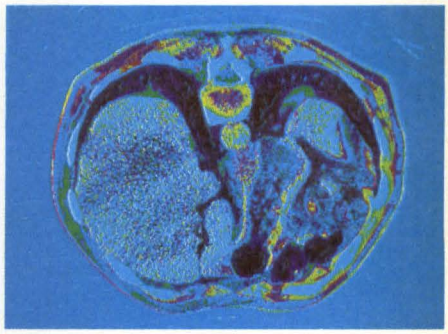
3. Simplified Processing (AutoCAD Software)



4. 9 Bit Planes (Courtesy WSI Inc., Bedford, MA)



5. 16.8M Color Shades (Courtesy Catherine Del Tito, Wave Graphics)



6. High Resolution (Courtesy University of North Carolina at Chapel Hill, Depts of Computer Science and Radiology)

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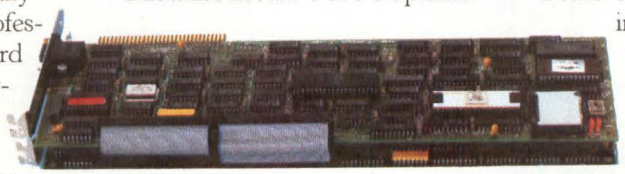
Even though IBM offers a color graphics card, professionals still choose Vectrix. It's not surprising. Especially once they've seen us in action. Professionals know that our VX/PC Board Set delivers the quality and performance they need for serious color graphics.

The VX/PC Board Set provides advanced features that help simplify sophisticated graphics design. Besides displaying 512 simultaneous colors from a palette of 16.8 million, the VX/PC supports an extensive library of on-board graphics macros for ease of programming and fast design, as well as full emulation of the IBM color card. And, an on-board 16-bit microprocessor frees your computer to concentrate on other tasks.

But that's not all. Our 9 bit planes



add an extra dimension of sharpness and clarity to your image that must really be seen to be appreciated. That's why it's not surprising to see Vectrix color cards in applications such as medical imaging, weather satellite data mapping, computer aided design and drafting, and graphics arts, to name a few.

What you will find most surprising, however, is the price. Our VX/PC Board Set was designed with the OEM in mind. So when comparing the performance of Vectrix with the competition, check the price too. You'll like what you see. For more information, contact Vectrix Corporation, 2606 Branchwood Drive, Greensboro, North Carolina 27408. Phone (919) 288-0520. Telex 574417.

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Circle 22 on Reader Inquiry Card

The graphics capability of the GMR on the DM550 is impressive. Ten thousand 2D vectors/sec can be transformed and clipped while simple vectors can be drawn at 1 million pixels/sec. Area fills execute at 35 million pixels/sec and bit-block transfers are supported. Although 3D capabilities are not now available in the present version, it is considered a first priority.

The most important feature of the GMR is that it runs on the family of Apollo systems which uses a fast LAN to communicate with other units. In addition, its use as an OEM system allows potential for the GMR to become a major force in the increasing need for graphics standards.

—MacNicol

Circle 239

Dedicated Image Processing Chip Provides Low Parts Count And Greater Functionality

As the demand for greater graphics capability steadily increases, so does the demand for graphics support chips. An area getting less attention than the spotlight of graphics display is image recognition and image processing. Image processing applications such as robotics, automatic image inspection, and vision systems require fast processing typically beyond the power of 8-bit processors. One problem has been the multitude of methods and architectures to accomplish processing. Another problem is speed. Object recognition and image enhancement require tremendous processing power at high speeds, typically in real time at video rates. The alternative route is downloading the image for off line image processing or hardware incorporating pipelining or parallel processing.

An integrated circuit from Hitachi, called the image signal processor (ISP), is a dedicated image processing chip aimed at real time video applications. It performs most of the important two dimensional image processing needed for gray scale video image processing at a resolution of 256×256 pixels. More importantly, it claims to yield speeds of 1000 times faster than systems based on conventional 16-bit microprocessors and 100 times faster than many 32-bit computers. Designated the HD-61840R, the CMOS chip uses 3-micron geometries to hold its 60,000 transistors. It will be offered in a 64 pin dual inline package.

Image processing typically requires five steps: image input, sampling and quantizing, preprocessing, feature extraction, and object recognition. The process originates from a video camera to a digitizer where the information is converted from analog to digital for processing. Preprocessing is required to subtract random noise and set proper level and contrast values. The features are then extracted digitally with the goal of object identification. Preprocessing and feature extraction consume the most time. A dedicated integrated circuit such as the HD61840R can decrease processing time from several seconds to milliseconds. A 256×256 pixel image can be processed by this chip in just 10.9 msec, which is fast enough to process the video frames produced by a video camera. Optimized for noninterlaced images, the processor uses 8-bit words for calculations using single instruction, multiple data stream processing and pipelining. Increasing the power of the chip can be done through the use of multiple chips in parallel.

There are five basic subsections of the ISP: data memory, processor, linkage, evaluation, and control units. The heart of the unit is the processor which consists of four subsections called processor elements. Each processor element works on four 8-bit data words in parallel, simultaneously performing the same operation. The data unit includes four 8-bit shift registers which shift the data both to the processor element and the register to the right. This is one of the key elements that make it fast and efficient. The memory unit holds the data for spatial convolution in its four 16-word by 8-bit RAMs. The evaluation unit then performs binarization and clustering, sending the data to the linkage unit where the data is placed on the bus.

Timesharing the ISP is possible and cuts the chip count. The timesharing approach increases processing time of a 256×256 image from 10.9 msec to 43.7 msec and for a 512×512 from 43.7 msec to 174.8 msec.

—MacNicol

Circle 238

DEPARTMENTS/ICs

Multiple Technologies Merge Onto One IC

Perhaps the most significant problem plaguing the gate array industry is the inflexible nature of the chip itself. For instance, high-speed requirements (above 20 MHz) typically require a bipolar technology, but at the cost of excessive power dissipation. At the same time, CMOS offers low power consumption but can only operate at speeds up to about 20 MHz. Attempts at integrating the two technologies have resulted in arrays that have CMOS cells at the center and bipolar cells at the edges. In most instances the bipolar cells do not have the performance necessary for signal processing applications and thus are primarily used as high-drive interfacing circuits.

In answer to the call for more flexible arrays, Hitachi America (San Jose, CA) has developed a new 2-micron fabrication process that combines ECL and CMOS transistors on a single array. Unlike other customized bipolar/CMOS

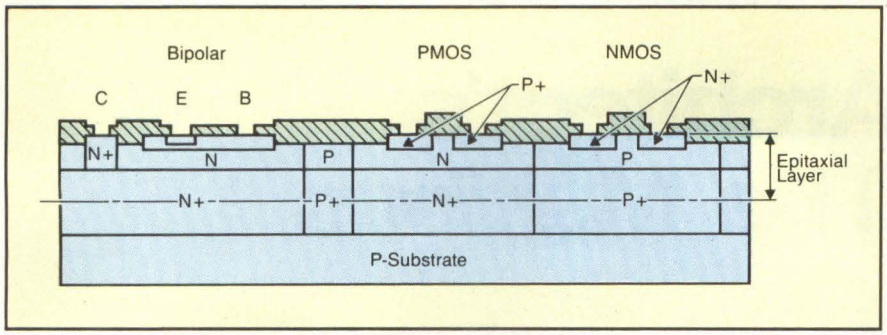


Figure 1: A cross section of Hitachi's new Advanced Bipolar-CMOS device which provides both ECL and CMOS transistors in a single cell.

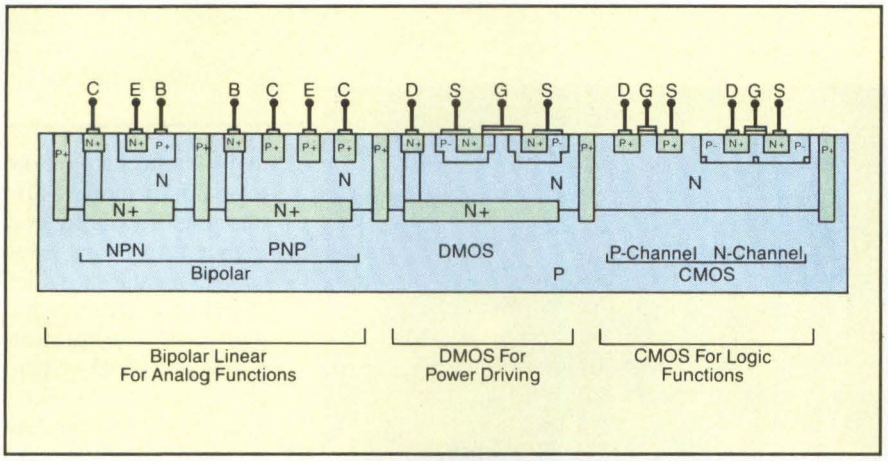


Figure 2: SGS' new MD-MOS technology combines bipolar linear, CMOS and power DMOS on one chip.

chips the Advanced Bi-CMOS array from Hitachi implements both ECL and CMOS devices in a single cell. According to the Japanese-based firm, the propagation delay time of a 2-input nand gate has been recorded at 0.71 nsec with a load capacitance of 0.85 pF. Using this technology, a 1500-gate ALU chip was fabricated and dissipated 160 mW while running at 10 MHz; typical power dissipation is 0.15 mW/gate.

The new process, presented at the International Conference on Computer Design, is presently on its way out of the research laboratory and into the market. Hitachi expects to incorporate the process into its product line by late 1985.

Similarly, SGS Semiconductor (Phoenix, AZ) has unveiled its MD²MOS technology which combines bipolar linear, CMOS, and power DMOS circuits on a single chip. The combination of analog, power-driving and logic functions provides increased flexibility and efficiency for high-frequency switching and high current applications. In high-frequency implementations (500 KHz), the technology delivers up to 200W output power and 10A of output current. For high-current applications, MD²MOS provides output current up to 10A output power reaching 500W. (On resistance is 0.15 ohms).

DMOS offers several advantages over conventional bipolar transistors. For example, the output stages need no driving power, thereby allowing simpler voltage controlling circuits (as opposed to current controlling) to be used to drive the transistor. In addition, since there is no secondary breakdown, the safe operating area is only limited by power dissipation which improves switching reliability. Finally, the negative temperature coefficient facilitates the paralleling of devices.

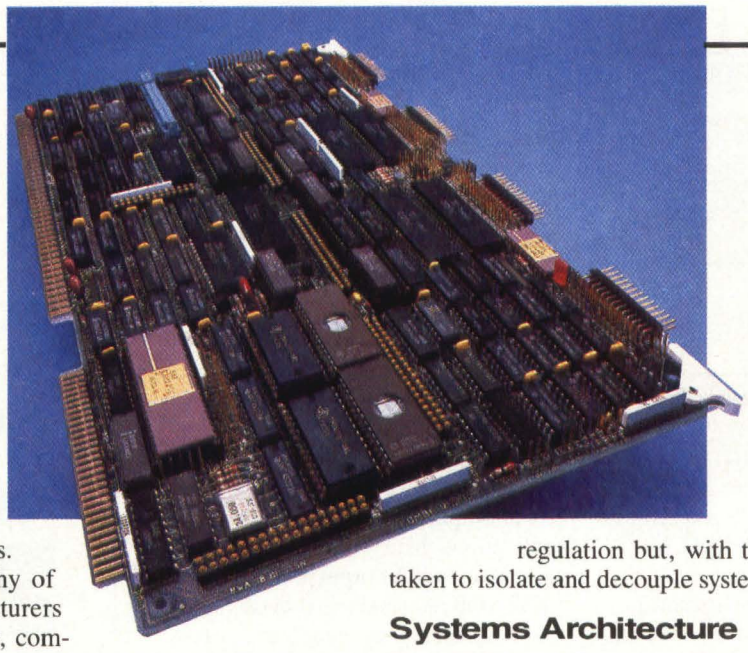
Power MD²MOS (DMOS-1) is currently being tested as the B4309, an H-bridge circuit configuration that is housed in SGS's high reliability Multiwatt packaging. Future applications include the development of 250V/100W DMOS-2 telecommunication power supplies and off-line converters for the US market. Similarly, 450V/50W DMOS-3 is being developed for off-line converters to be used in Europe.

—Collett

Circle 230

Systems Architect's Guide To The Multibus

by David Wilson, Executive Editor



Over the past year the activity surrounding the Multibus has brought forth a number of new product introductions; yet the Multibus still retains its lead as the most popular bus in the OEM market today. This scenario is unlikely to change during the foreseeable future since many Multibus customers will find an easy upgrade path from currently installed 8-bit designs to newer 16-bit solutions.

The marketing philosophy of some of the Multibus manufacturers appears to be changing; thus, competition over the next few years may become intense. In the past, Intel (inventors of the bus) have held the market share in the CPU arena and a myriad of smaller vendors have taken the remainder of the pie by specializing in memory, disk and tape controllers and communication boards. However, Intel's recent announcement to private label the Xylogic's disk controller line, albeit beneficial to the customer base, may force those smaller controller manufacturers to downplay or abandon their efforts on the Multibus altogether. Yet in other announcements, it appears that Intel is going head-to-head with some smaller vendors. Intel's latest Multibus product offering the iSBC 188/48 Advanced Communicating Computer, an intelligent 8 channel SBC, is obviously chasing after the same customer base as the Metacomp product line.

Whether Intel has enough dedicated resources to engineer a product for each of these vertical markets and to compete in performance is only part of their problem. They must also overcome the mindset of the systems architect who may be reluctant to abandon the tried and proven product of the smaller vendor. Whatever the outcome, the Multibus marketplace continues to grow rapidly with currently over 200 vendors of products available to the systems integrator.

While Multibus presents relatively few questions to the systems architect at the low level, it provides all-important flexibility at a higher level. Low level choices include the width of address and data paths, multimaster arbitration technique (serial or parallel), interrupt handling (bus vectored or non-bus vectored) and power distribution. The method of power distribution is an important design factor to consider. Multibus employs efficient off-board regulation but, with this method, care must be taken to isolate and decouple system components properly.

Systems Architecture

The Multibus family consists of a number of different bus structures, each aimed to expand the capabilities of the basic system bus. Three extensions—the iSBX bus, the Multichannel bus and the iLBX bus have found different levels of acceptance in the marketplace. The iSBX bus, for example, a low-cost local or board I/O expansion bus, is supported by a number of vendors and offers the system integrator an easy way to upgrade or add additional functionality to the Multibus board. On the other hand, the multichannel bus, a high speed path for block transfers between a Multibus-based system and peripherals or other remote computer systems, has yet to receive any attention primarily because of the number of IC devices needed to implement the structure at the present time. Although a single chip solution will be offered by Intel in the future, most vendors are turning to solutions that are available now, such as the SCSI. The iLBX bus, introduced in 1983, is similar in concept to Microbar Systems' Dual Bus introduced in 1981. It is a high speed, memory-only execution bus that makes it possibile to expand the local memory of a microprocessor on a single board computer by using multiple boards.

Figure 1. The COM16 from Microbar Systems can function as an intelligent 16-line communications controller or as a standalone SBC.

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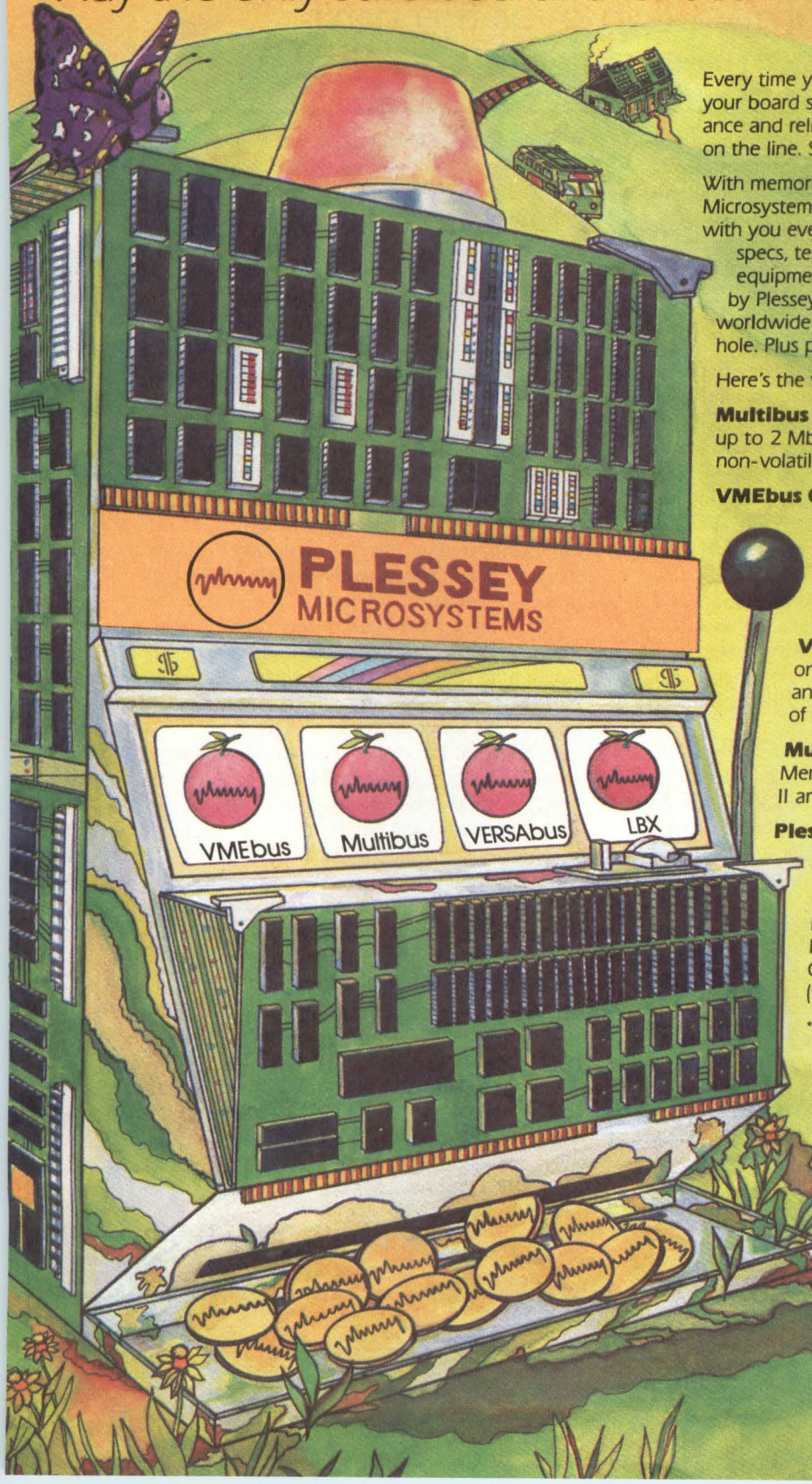

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The marketing philosophy of some Multibus manufacturers appears to be changing; thus, competition over the next few years may become intense.

The architecture provides a great deal of flexibility in the system design. The system bus is used only for interprocessor communication and I/O, yet the structure allows the memory to be expanded to the limits of bus loading, bus length and memory addressability. For some application, the high speed bus may be used as an I/O interface for special purpose peripherals that may approach the limits of the Multibus bandwidth.

Enhancements To The Architecture

Many effective mechanisms currently exist that are improving the performance of the Multibus structure but do not involve the redefinition of signals on the bus. However, one modification to the bus structure can significantly improve performance, that is, making the bus wider. Two recent proposals from Microbar are aimed specifically at effectively doubling the bandwidth of the LBX bus through pin redefinition.

Since the LBX already has an address strobe signal and a data strobe signal, the control lines exist to allow a multiplexed address/data bus. All that would be required would be an additional byte control line so that the existing signals byte and word operation could be signaled. The disadvantages of this approach are that address pipelining could no longer be supported and maintaining compatibility with the existing LBX definition is more complicated.

Another approach is to provide the wider data path by eliminating the address cycle for the second transfer of 16 bits. Thus, the processor would assert the address for the 32-bit word, and the first 16 bits are presented on the data bus, followed in a specified time by the second 16 bits. This approach also requires an additional line but it can be multiplexed with an existing control line. Compatibility is achieved by allowing downward compatibility via a jumper option. In other words, a 32-bit card could be configured to supply only 16 bit transfers for downward compatibility. A system that plans to use 32-bit transfers must have all cards on the enhanced (LBX+) bus capable of 32-bit operation. Such a bus is suited to many of the 256K memory components now appearing on the market (see "Design Options Increase for Users of 256K Dynamic RAMs" by Brita Meng in this issue). Many have a nibble mode that allows successive memory location to be read without the necessity of restrobing the address information.

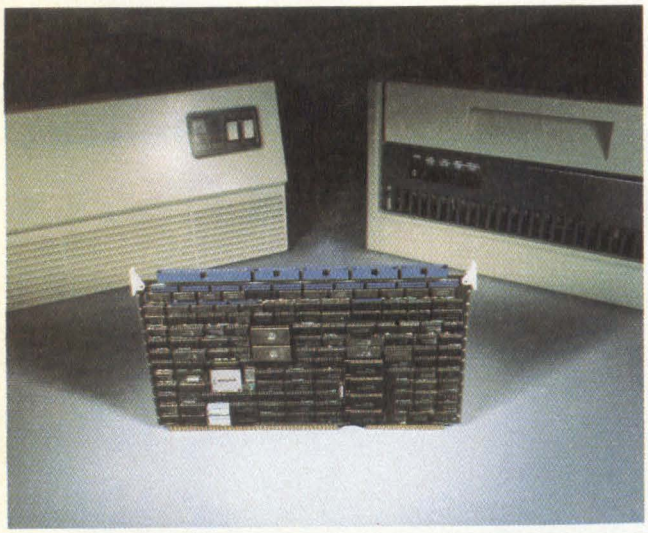


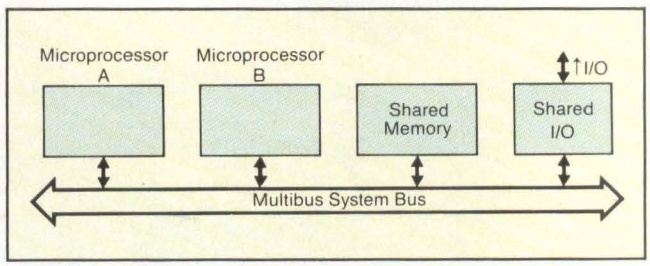
Figure 2. The RIMFIRE 50 from Ciprico shown connected to two different disk drives.

Multiprocessing Vs. Multicomputing

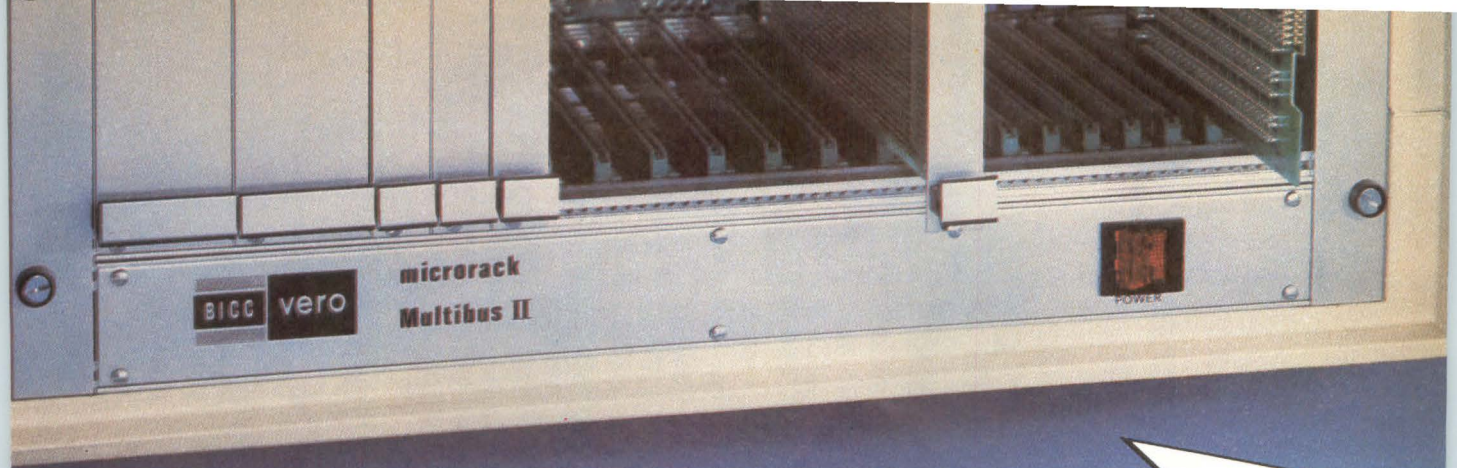
An important difference between multiple computer systems and multiprocessors is the extent to which common resources are shared. A multiple-microprocessor system consists of two or more separate and discrete computers that can communicate, whereas a multiprocessor is a single computer with multiple processing units.

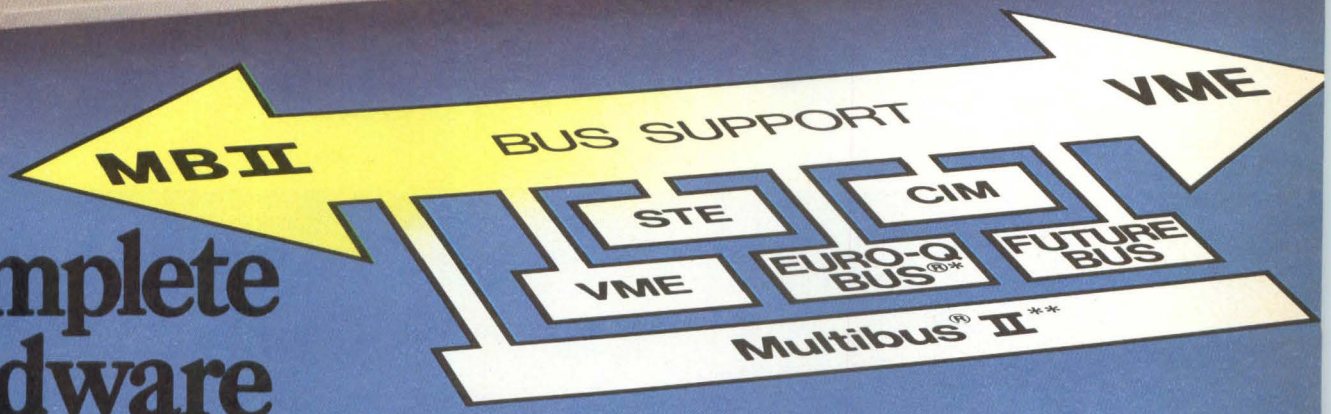
The limited bandwidth of the Multibus system bus is the reason multiprocessing architectures have not been popular. A single time-sharing bus system may be limited to supporting only two processors. Even with the addition of a cache memory between the microprocessor and the system bus, the bus may only allow for three or four processors but the cost of implementation may be considerably higher. Another alternative, a functionally partitioned single time-sharing bus system, provides dedicated local environments for each of the processor modules called functional modules. It permits each of the processor modules to operate at maximum speed, independent of the system work load except when using common resources, such as I/O. The hardware design complexity is similar to that of the single time-sharing bus design and provides better performance than the single time-sharing bus with cache. The major disadvantage of the functionally partitioned approach is that the memory usage is higher than in the other two approaches.

Most companies currently producing multiprocessing architectures have chosen to develop their own higher speed bus structure to support their designs. However, Multibus 2 is a



A multiprocessing configuration.





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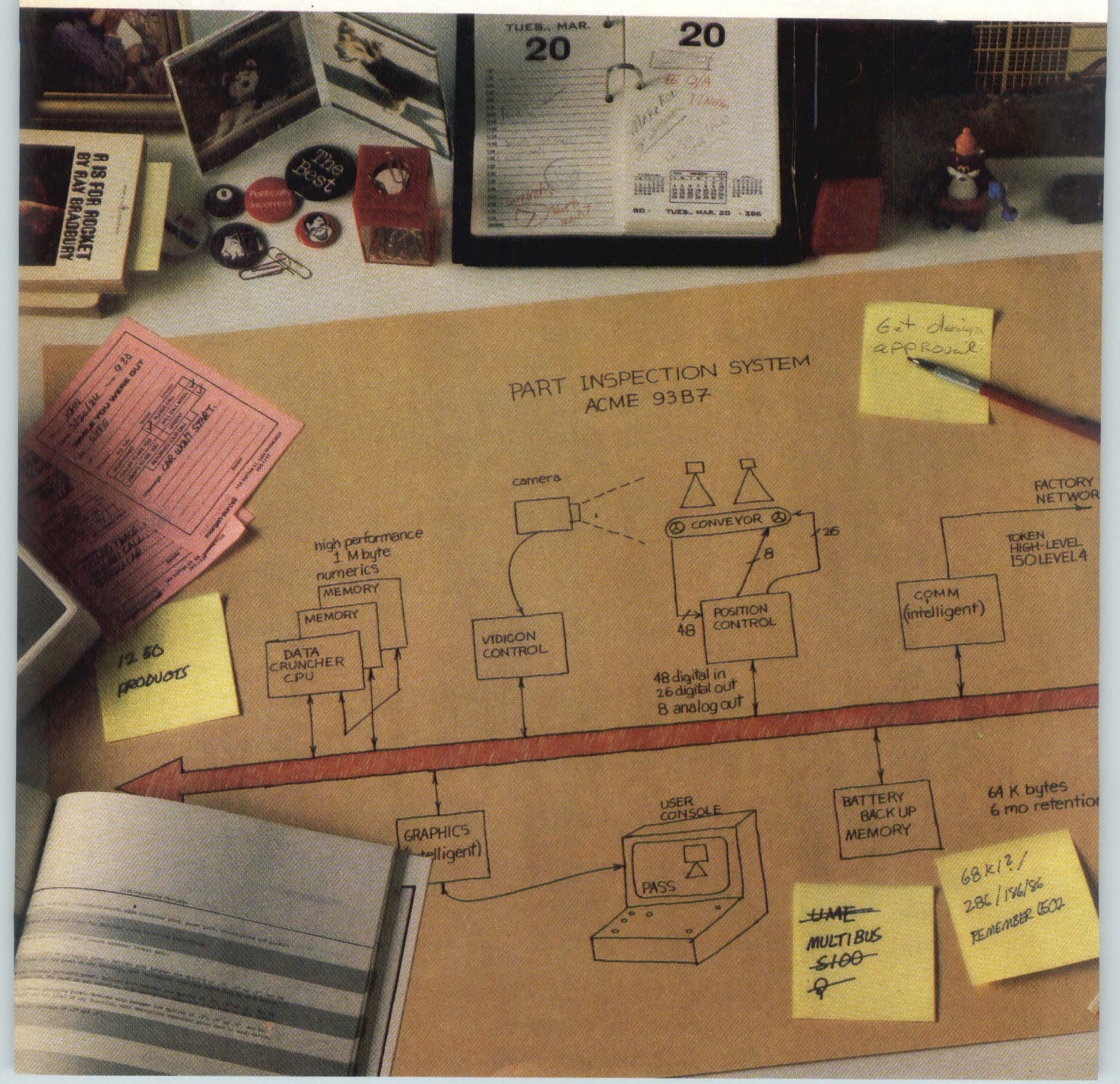

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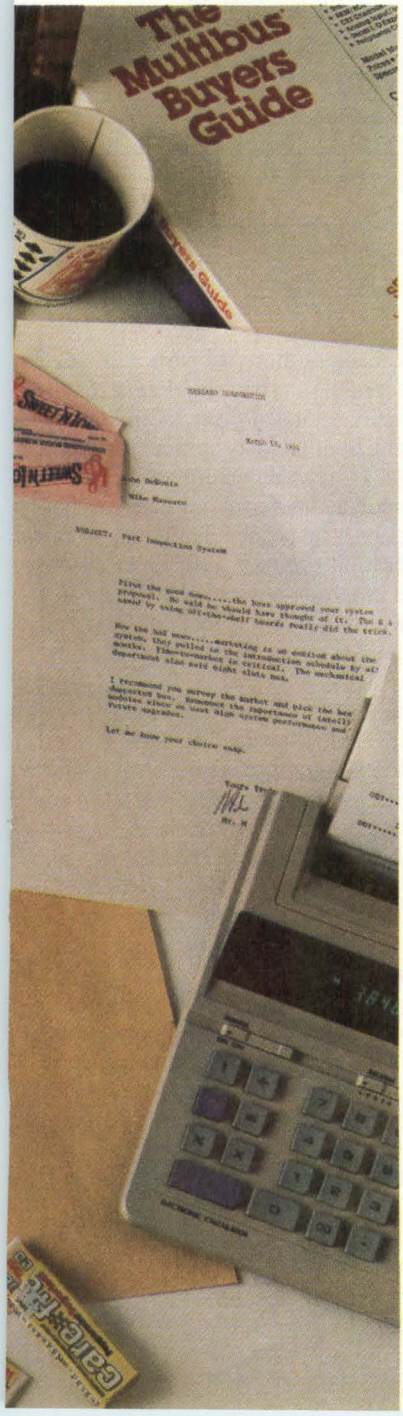

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prime candidate for this sort of application, and it is expected that many computers will be announced towards the end of next year based on that bus structure.

To be announced at the same time as Intel's range of Multibus 2 boards will be the specification for Digital Equipment's VBI bus. It will be interesting to see whether DEC's spec will support the same sort of multiprocessing architecture.

Clearly, the market for Multibus products falls into two categories; there are those vendors that offer general purpose systems and those that offer board level products. Often a vendor will offer both to the marketplace. The profit margin on a system level product is obviously greater than the board business can provide, but the systems architect ought to be aware that many of those vendors in both businesses may have become too diffuse and the systems businesses may have taken away the resources needed to develop the next generation of board level products. One demand the systems architect is placing on the board vendors is higher levels of integration, such as board sets with supporting software, or other portions of the OEM system such as an integrated disk controller subsystem. The vendors of iSBX boards, for example, may in the future offer drivers for specific Multibus boards to make the integration task easier.

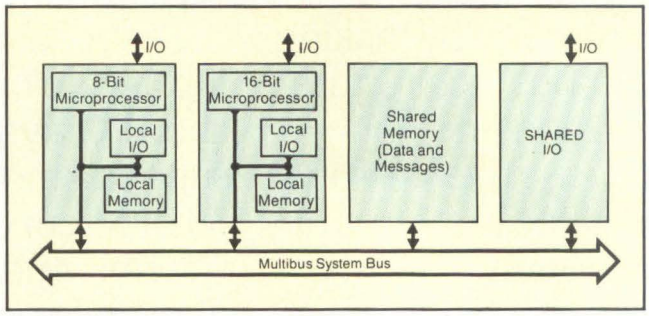
The UNIX marketplace has been beneficial to the Multibus for two reasons. Some single CPU-based systems are built entirely around the Multibus, offering board vendors an opportunity to provide a wide range of upgrade products. The Logical Microcomputer Company's (Chicago, IL) Megamicro is, for example, based around National Semiconductor's 32016 processor and floating point unit. Other UNIX systems that provide single or multiprocessing environments for UNIX (although they may be based upon their own proprietory bus structure) offer a Multibus I/O adapter. This allows the OEM customer the opportunity to customize the system for the addition of boards to handle functions that the system house may not be able to provide directly. The wide vendor support of the Multibus makes it a natural choice in this environment.

One vendor taking this approach was Apollo Computer, who based its DOMAIN network on a 12 Mbps token passing ring technology. Communications to remote heterogeneous systems, however, require a different network protocol and transport. After reviewing the needs of its customer base, Apollo selected Ethernet, and announced its Com-Ethernet product in mid 1983. Apollo uses the Multibus to interface peripheral devices and selected Interlan's Ethernet Communications Controller to perform the data link and physical channel functions required to interface to Ethernet. The board plugs into an Apollo communication server running the Apollo Software and the DOD-compatible TCP/IP protocol. Another vendor, Arete Systems (whose own bus structure was optimally designed to support multiprocessors and dynamic load balancing), uses the Multibus as an effective form of I/O.

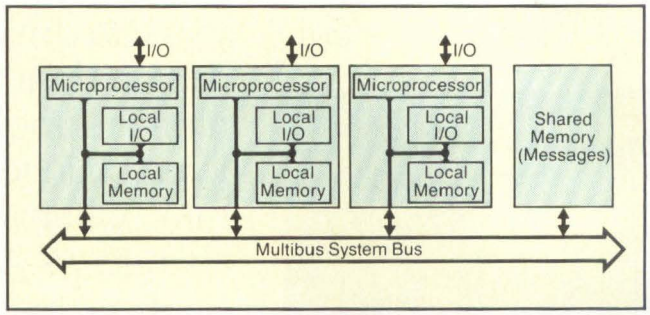
Multicomputing

The area of most interest to systems architects as it relates to the Multibus is the area of industrial automation. Here, the areas of multicomputing and locally distributed processing are far more important than the multicomputing environment described earlier.

Unlike multiprocessing, a multicomputer architecture is a top-down design philosophy that is based on a functional partitioning of the solution of a problem into a number of smaller



A multicomputing configuration.



One locally distributed processing configuration.

and simpler subcategories. Each of these subparts is divided into a separate well-defined module and each module performs a dedicated set of functionally bounded tasks. A multicomputing system is built by using multiple microprocessors, each a dedicated task or function. Increased performance is based on the concurrent execution of a number of unrelated events. The advantage to this approach is that each functional unit can be upgraded as next generation products emerge from the manufacturers. It is in this environment that placing greater functionality on a single Multibus board is most evident as it both decreases the cost and increases the modularity of the final system.

One technology sure to have an impact here is the use of surface mount devices. Already Little Machines, a newly formed San Diego-based manufacturer, has announced such a product – the DPX86/ME. Two processors, a 286 and a 186, take care of application and I/O subsystems. The board can support Ethernet, RS-232-C and a Centronics interface that can double as an SCSI interface. Memory on board can go as high as 1 Mbyte RAM and 400 Kbytes of ROM. In order to support an expanded system the iLBX is also supported allowing a system to contain up to 16 Mbytes of RAM.

The advantage of squeezing that amount of capability onto a board brings with it numerous advantages to the systems architect. System power consumption is decreased, and the exchange of data between the peripherals and the user is increased. System cost is decreased since fewer physical components are needed when eliminating bus logic from multiple cards, and system configuration becomes easier because major system elements have been integrated onto one card.

Like surface mount technology, SIP technology is also seeing widespread use for similar reasons. Like the Little Machine board, the Omnibyte OB68K/MSBC1 also uses SIP devices for its memory implementation. In this case 64K SIP DRAM

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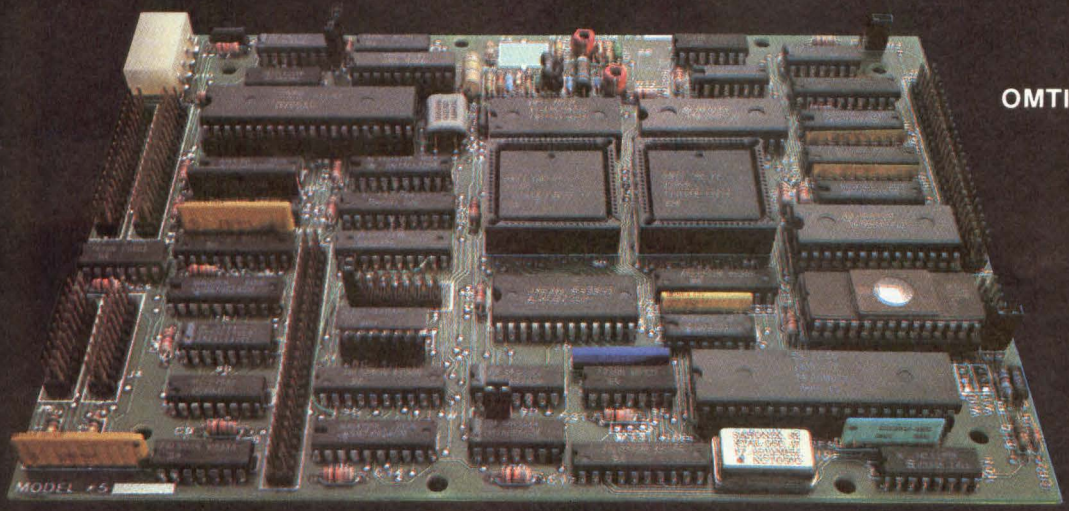

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devices give up to 512 Kbytes of zero wait state, dual ported RAM with parity. Use of 256K devices will allow up to 2 Mbytes of RAM on the board. A board like this with integrated CPU and RAM takes up only one slot and may represent a saving of several slots since the integrator may not need to use external I/O and memory boards. This becomes important in a system where the number of available Multibus slots is limited. It may also prove more cost effective than buying separate memory or I/O boards.

As remote I/O exceed card cage capacity (a problem in process control remote data acquisition and control systems), usually a remote is spit into two units, each with associated processor, power supply, communication interface and modem. Likewise, in standalone situations, where card count exceeds the usually 26 slot maximum Multibus card cage size, a unit is usually split into a master and remote with the added complication of communications software. However, by use of a bus repeater, the above two scenarios can be avoided.

Procise Corporation (Issaquah, WA), manufacturers of such a product, recommend that seldom used memory boards and all input/output boards be placed in the expansion card cage to minimize added unit states. Input/output boards usually have access times far exceeding spec and can be repeated at some distance without adding wait states. Slow access time main program memory would obviously be the poorest choice for expansion.

CMOS Helps Industrial Designs

Today, industrial system design dictates a comparatively small central computer which assumes a supervisory role over smaller, smart remote computers performing the actual control function on the plant floor. Many of these remote locations often are severe environments that require a computer in a sealed enclosure. Using CMOS system level technology, it is now possible to place the remote computer in locations where previously it was not economically feasible because heat removal equipment needs to be added. **Table 1** shows equipment pricing and specifications for two systems used in an application involving a shop-floor, machine-tool control computer. No analog I/O is used in this example since actual control interfaces are provided by a numeric controller unit that is an integral part of the machine. One system was configured with typical TTL/NMOS technology and the other with CMOS technology boards. Components common to both configurations, such as the card cage and enclosure, were not considered.

CMOS SYSTEM			NON-CMOS SYSTEM		
equipment	price	power req.	equipment	price	power req.
CBC860/05	$1395	+12V, 11 mA −12V, 11 mA 5V, 200 mA	iSBC86/05	$1645	+12V, 25 mA −12V, 23 mA 5V, 4.7 A
CBC256/24	$1989	5V, 100 mA	iSBC254	$2570	12V, 1.4 A 5V, 3.0 A
totals	$3384	+12V, 11 mA −12V, 11 mA 5V, 300 mA	totals	$4215	+12V, 1.425A −12V, 23 mA 5V, 7.7 A
total power: 1.764 Watts			total power: 55.876 Watts		
(Data obtained from manufacturer's published specifications)					

Table 1. CMOS vs. non-CMOS systems comparison (courtesy of Diversified Technology).

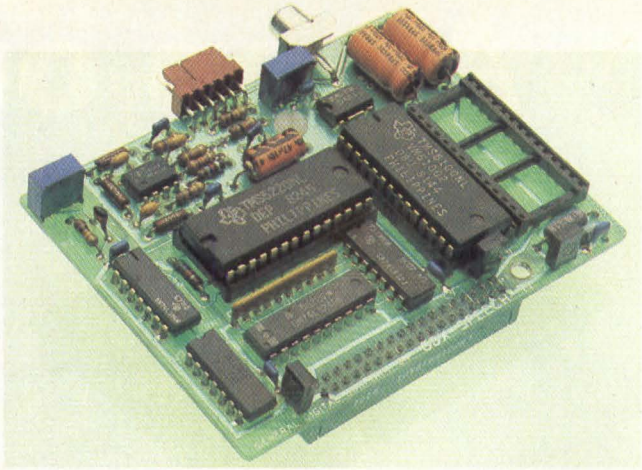

Figure 3. An SBX module from General Digital allows the systems architect to add synthesized speech to a Multibus board.

If other I/O functions had been required (such as analog inputs), standard Multibus cards could have been used since the CMOS boards meet all the Multibus timing and drive current specifications. Even if other cards are added, the power savings obtained by using CMOS processors and memory boards will in many cases still allow the enclosure to be sealed without the use of cooling equipment.

In those cases where the central supervisory computer may be an IBM PC and the remotes are Multibus based, the systems architect can use an IBM PC to Multibus adapter to facilitate the integration process.

Disk And Tape

The characteristics and projected use of a peripheral device must be taken into account by the systems architect when choosing peripheral subsystems and evaluating system performance. The task of the controller in such a system is to provide for the most efficient use of the peripheral when measured in the environment of the complete system.

Disk and tape subsystem performance is as much dependent upon the tape or disk controller as upon the drives themselves. Today, state-of-the-art controllers are microprocessor-based and capable of not only speeding up the data tranfer but reducing service time, making system integration easier and, in many cases, performing self diagnosis functions. Disk drives must be able to handle large numbers of random requests for usually small blocks of data. The time required to transfer the data is usually not a large percentage of the total access time. The controller's primary function therefore is to reduce system overhead and to increase throughput significantly.

Key performance parameters include sector caching, on board microprocessor and overlap seeks. Sector caching becomes important because data from sectors directly following the one being accessed are often called for in subsequent requests. Many controller boards offer some cache memory specifically for this purpose. By having a processor on board, programmable options are easily installed, whereas before cumbersome changes to the firmware or hardware were neces-

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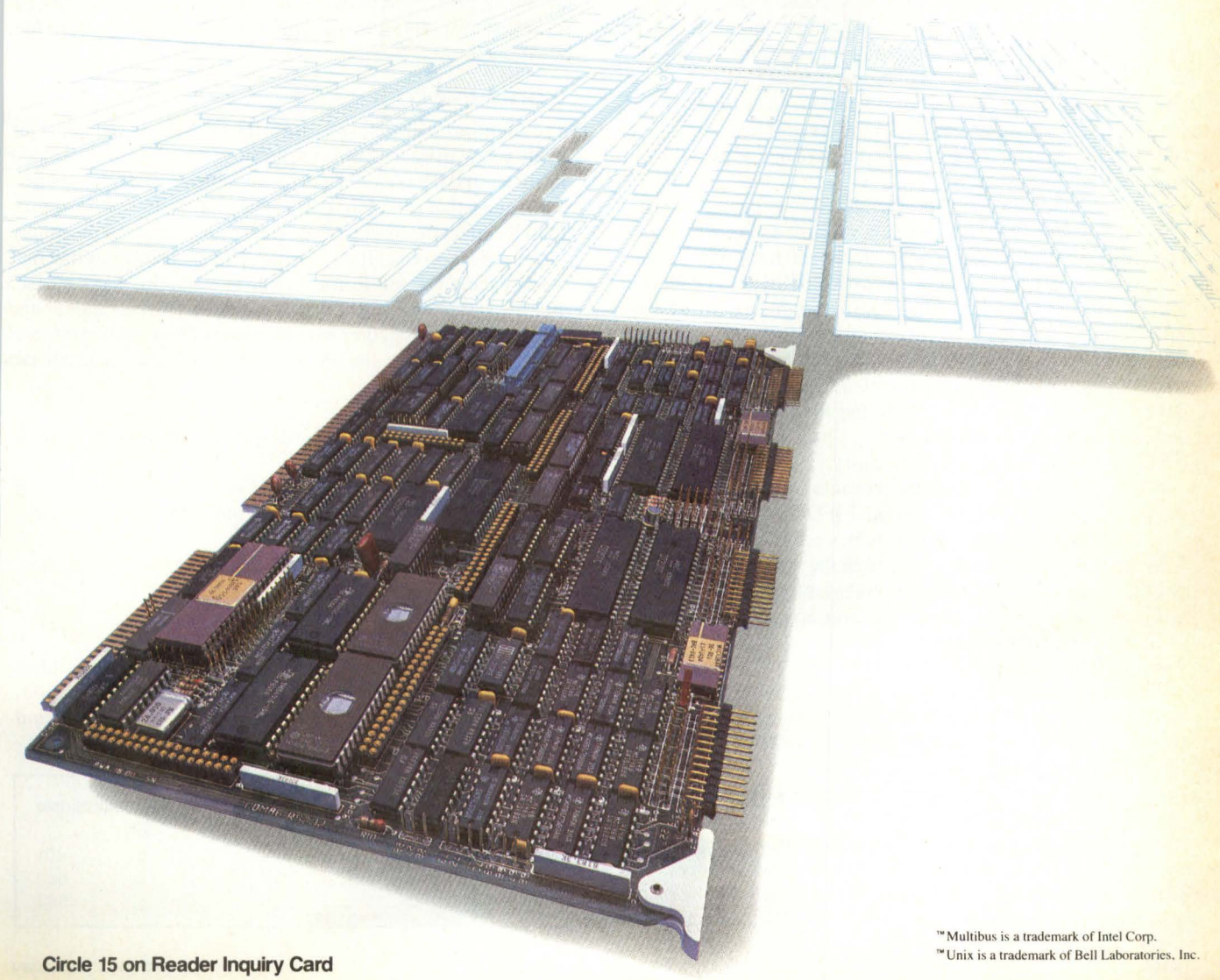

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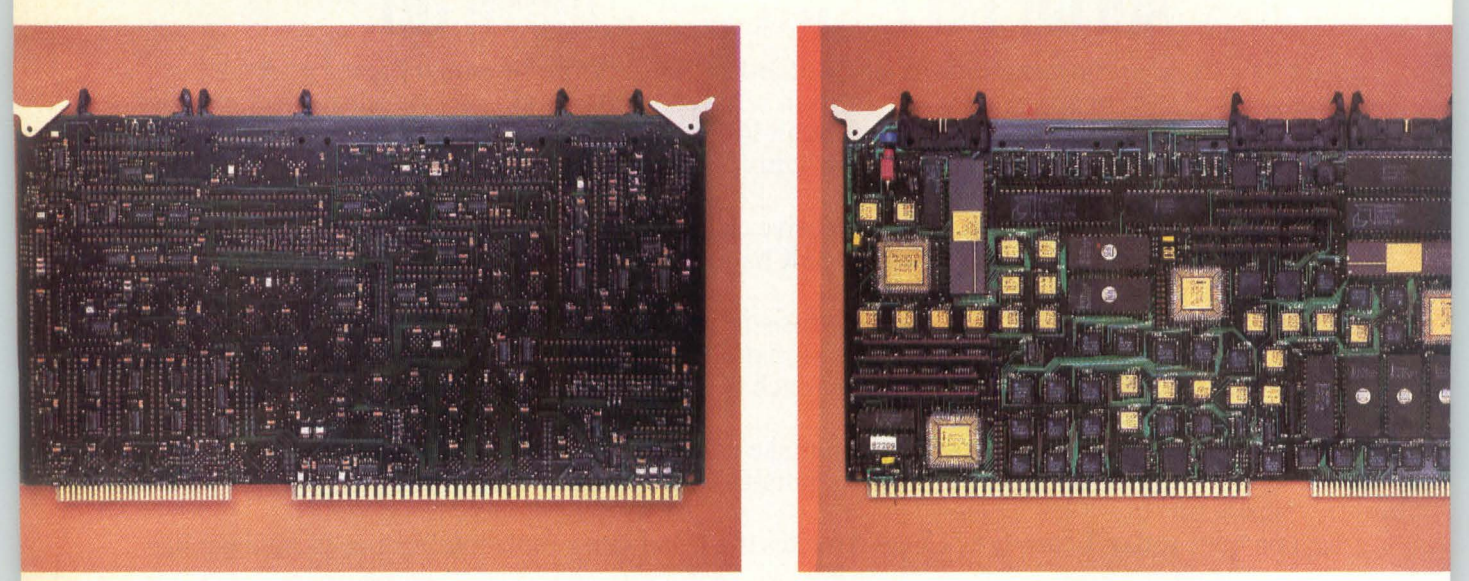

Figure 4. The Little Machine board makes extensive use of surface mount and SIP devices.

sary. Thus, it becomes easier to adapt the controller to the application, i.e., mixed drives, sector size, variable formats, custom functions and new drive features. Rather than handle requests sequentially, overlap seeks allow multiple operations to be concurrent across all the drive, reducing the average time to store or to retrieve information. A consideration vital to the systems integrator is to ensure that the board vendor can supply or recommend drivers to interface to standard operating systems such as UNIX and RMX.

A tape drive is normally not considered an integral part of an operating system but is used primarily for file and transactional backup or archival storage. Data is stored and retrieved sequentially, usually in large blocks (512 bytes to 20 Kbytes). Thus, system overhead, transfer rate and ease of integration are all key factors in controller design. Given the operating characteristics of the tape drive, the single most important feature of the controller is bus speed—the rate at which the controller transfers data across the Multibus. While the theoretical maximum attainable data rate is 10 Mbytes/sec, a practical limit is about 4 Mbytes/sec with a 250 nsec memory.

For a GCR drive at 100 ips, the data rate is 625 Kbytes/sec on the average. Several factors, such as a FIFO front-end or a cache data buffer on the drive, could increase this rate to about 1 Mbyte/sec, but even this is only 25% or the maximim bus bandwidth. In most systems, a FIFO of 64 bytes to 1 Kbyte would be adequate. But in a system that has a large amount of bus traffic or is subject to extensive data bursts by other controllers, a larger FIFO may be desirable.

The above reference to bus speed assumes a burst data rate. Since bus arbitration on the Multibus occurs in series with bus transfers, efficient use of the bus demands a method of controlling data bursting. Throttling is a method of programmably selecting a data burst length. It can be one of two types, demand or count throttling. Demand throttling allows the user to select the maximum of transfers that occurs each time the controller arbitrates for the bus. Count throttling is somewhat more complex in that it guarantees that a number of bytes will always be transferred with each grant of the bus. A variation of count throttling, called time throttling, allows the user to specify one amount of time, rather than the number of bytes transferred. In some systems, this allows another level of control over how the bus is used.

Conclusion

The Multibus will retain its lead in the OEM board business for many years, primarily through the large installed base of existing users and the wide variety of available product. Even those companies that abandon their support of the bus will not profoundly effect the market since smaller vendors will inevitably pick up their product line. When AMD dropped their line that was picked up by Jeff Roloff's Central Data, this was the case. For the systems architect developments in surface mount and SIP technology, together with support software for board level products, will make the task of systems integration easier. DD

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Acknowledgments

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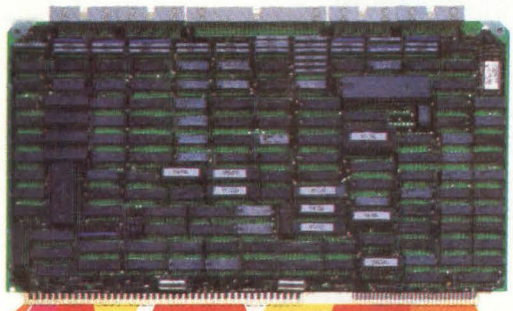

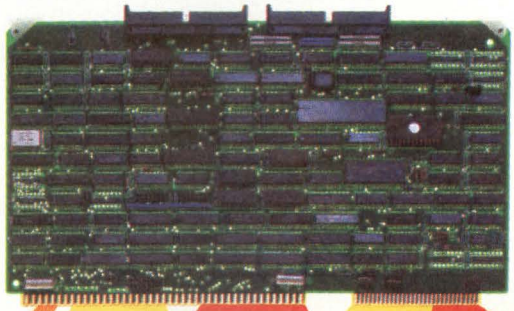

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Making The Most Of 5¼" Winchester Drives For Improving System Performance

Data integrity, cost, capacity tried versus high-performance technologies, ease of integration and supplier track record are traded off in drive choices.

by Julie Pingry, Senior Editor

Access times, capacities and error recovery on all disk drives are improving very rapidly. The largest segment of the current disk drive market is for 5¼" units. Many companies have improved drive parameters within the constraints of the mini form factor. Effectively utilizing the potential of these drives is a challenge now facing system architects.

A critical issue for high-performance 5¼" drives is interfacing. Having a standard drive interface (ST506/412) has helped integration, but it may no longer be fast or flexible enough for new drives and systems. Several higher performance interfaces for 5¼" drives have potential, and until a standard emerges, choices are critical to integrating storage.

One trend is for drive manufacturers to incorporate some of the functions traditionally left to a host controller board into the drive unit. One advantage of intelligent disk drives is the possibility of specifying drive performance in a system with greater precision since only one manufacturer is involved. But for multi user systems, multiple drives may be more desirable and separate intelligence for each drive can be wasteful.

Since rigid 5¼" disks have only been available for four years, most suppliers are either young companies or have a history in either lower- or higher-performance disk drives. Each type of supplier, and each company, has a different focus. Some focus on volume; others' designs

Figure 1: A thin film disk being inserted into a Tandon drive. Even their 10 Mbyte models use this high-performance medium they make themselves.

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use new technology and parts not readily available in large quantities. In choosing a disk drive, cost, reliability, quantity availability, technological merit and supplier reliability must be balanced and traded off against each other.

Improving The 5¼" Rigid Drive

Manufacturers of mini-Winchesters have begun to use the technologies of larger high-performance disk systems such as closed loop servos. In order to pack upwards of 40 Mbytes into a standard 5¼" form factor, more data per unit area must be read and written, and positioning systems must be more accurate.

Closed loop servo systems are essential to high-performance drives. Though costs are higher, the accuracy of relative positioning can be important in fighting the thermal and shock effects prevalent in small systems. More efficient motors that dissipate less heat are in development. For shock, many manufacturers claim 40G isolation, but beware of shock mounting that makes a drive larger than the form factor. An interesting idea is Microcomputer Memories' (Van Nuys, CA) 3 ½" drive shock mounted in a standard 5¼" package.

Thin film recording surfaces are coming into play; several dozen firms are now involved in manufacturing sputtered or plated metal recording surfaces, and drive makers using the disks seem satisfied. Metal recording surfaces allow the same size disks to pack nearly double what oxide platters do now.

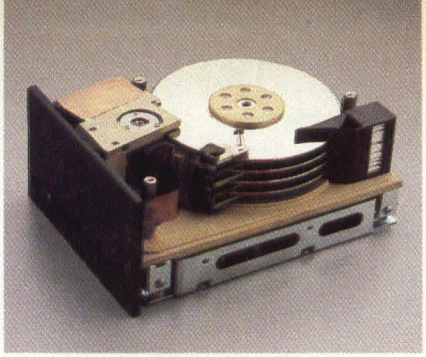

Figure 2: This Vertex drive packs four plated-media platters into a standard full-height package.

As thin film metal disks enter high-volume production, they will likely drop in cost and continue to improve in quality. Some companies still complain that thin film is not up to volume reliability. At the other extreme, drive maker Tandon (Chatsworth, CA) makes their own thin film media, and claims that it is more cost-effective for them to use metal disks (even on their 10 Mbyte units) than to purchase oxide disks outside.

Another drive component critical to recording density is the read/write head. Besides the standard Winchester head, mini-Winchester (or mini-monolithic) heads with smaller mass are available. These provide better shock immunity, as well as allowing more platters per package. Small thin film Whitney heads and advanced mini-composite heads for increased track density are now difficult to get in dependable volume production quantities.

Thinner heads are only a minor part of the mechanical squeezing involved in designing a high-capacity 5¼" drive. To get more disks in the standard package, and thus more recording surfaces, Maxtor (San Jose, CA) pioneered (with patents pending) the in-spindle motor. Recording closer to the inside and outside edges of each platter is another way to pack in more data. Eliminating the dedicated zone for head landing has been proposed, but with little success since data integrity suffers greatly.

Denser packaging of the electronics has also aided the capacities of small drives. With a single PC board, there may be room for an extra disk. Most drive manufacturers are looking to custom analog circuitry. Though these ICs must be specially designed in many cases, companies using the circuits in several drive models can demonstrate adequate demand for a semiconductor house to profit.

Half-high 5¼" drives are overtaking the full-high drives for many low- to medium-performance applications. Housing both a 10 (or, recently, 20) Mbyte fixed drive as well as half-high backup in a standard form factor is extremely attractive for small system designs. Demand is such that companies like Microscience (Mountain View, CA) have been formed exclusively to produce half-high drives. The constraints of packaging are even more severe for these drives.

The net effect of much mechanical and electronic packing is lower part counts. In addition to lowering costs and shrinking packages, fewer parts leads to easier manufacturability and enhanced product reliability. And, along with supply, product reliability is the most important parameter of a disk drive to be designed into systems with a healthy future.

Another method of increasing capacity of a disk drive is coding data. As shown in **Table 1**, Run Length Limited Coding (RLLC) increases capacity by as much as 50%. As opposed to mechanical and technological means of increasing storage per package, coding allows capacity improvements with the same heads, media and servo system.

In creating a high-performance disk drive, capacity is just one specification to consider. The other main factor is access time. Access times for very high performance drives have dropped below 30 msec, and improvements are apparent in

CAPACITY IMPROVEMENT: RLL vs MFM

DISK DRIVE MANUFACTURER	CYLINDER	HEAD	SECTOR/ TRACK	USABLE CAPACITY	INCREASED CAPACITY	READ FORMAT
SEAGATE, TANDON, CMI, NEC, IMI	306	2	17 26	5326848 8146944	2820096	MFM RLL
SEAGATE, TANDON, CMI, NEC, IMI	306	4	17 26	10653696 16293888	5640192	MFM RLL
SEAGATE, TANDON, CMI, NEC, IMI	306	6	17 26	15980544 24440832	8460288	MFM RLL
OTARI	306	8	17 26	21307392 32587776	11280384	MFM RLL
MINISCRIBE	480	4	17 26	16711680 25559040	8847360	MFM RLL
TULIN	640	6	17 26	33423360 51118080	17694720	MFM RLL
CDC	697	5	17 26	30333440 46392320	16058880	MFM RLL
VERTEX	987	7	17 26	60135936 91972608	31836672	MFM RLL

Table 1: By using Run-Length Limited Coding (RLL) capacities of standard drives can be increased substantially with very minor additions of electronics. *Source: Sunol Systems.*

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many lower capacity units as well. Voice-coil positioners and refinements on rotary motors have helped access specs.

Combining improvements in bit density with lower access times has produced 5¼" drives with performance to compete with larger units. For small system design, the availability of a range of products in the standard "minifloppy" form factor is important. New technologies and extremely high-performance may need to be traded off with reliability and manufacturability.

Interfacing To 5¼" Drives

As drive makers hone their products' performance, the interface to the host computer being served must also improve. There are two levels of interfacing concerned: drive level between disk drive and controller, and host (or control) interface between controller and adaptor in the host computer.

One of the largest advantages that 5¼" hard disks have enjoyed to date is a de facto standard drive-level interface, the ST506/412. This interface was introduced about the same time as 5¼" drives. But in order to pack greater amounts into the package size, many are looking to higher bit densities, which, unless the normal 3,600 rpm is changed, means higher transfer rates off the disk surface.

Several interfaces have been proposed to operate at higher data transfer rates. They differ in functions, implementation, cost and speed ranges (**Table 2**). Some other high-performance interfaces are available, but seem better suited to larger drives and non-microprocessor-based hosts.

Feature	ST506/412	ST412HP	ESDI	ANSI X3.101
Transfer rate	5 Mbits/sec	5,10,15	5 to 15	1.2 Mbytes/sec (9.6 Mbits/sec)
Data format	MFM	MFM	NRZ	NRZ
Cables	1, 15 ft.	1, 15 ft.	2, 10 ft.	1/device, 50 ft.
Cable/Connector pins	34-pin & 20-pin	34-pin & 20-pin	34-pin & 20-pin	50-pin
Data Separator location	controller	controller	drive	
Status reporting	minimal	minimal	minimal	extensive
Access to	step pulse	step pulse	cylinder address	cylinder address
Main advantages	standard low cost	similar to standard, but faster	separator in drive, flexible speeds, config. reporting	error recovery, configuration reporting, relatively low cost

Table 2: Comparison of drive level interfaces for 5¼" rigid disks.

The life of the standard ST506/412 can be extended with Run Length Limited Coding. Adding only new coding/decoding circuitry, capacity of 5¼" drives can be improved until it is clear which high-performance interface will become best accepted. Among others, what was Vertex, now merged into Priam (San Jose, CA) is promoting RLLC for high-performance drives (**Figure 2**). Until higher track-per-inch plus coding are exhausted for capacity expansion, widely available, low cost ST506/412 products can be used with coding.

ESDI and ST412HP were originally thought to be the major competitors. But so far, even Seagate (Scotts Valley, CA), originators of the 412HP, have only used the interface at 5 Mbits/sec and (until Comdex) on an 8" drive. The 412HP does keep costs low by its similarity to the older standard. But like the ST506/412, only MFM encoded data can be used; minimal status reporting is provided, and operation is quite host-dependent.

Most now see ESDI as the next step in drive interfaces for 5¼" drives. Having been developed by committee is one big bonus for ESDI. The main similarities between ESDI and ST506/412 is that both use a 34-pin and a 20-pin connector and status reporting is still relatively scanty. But data is used in NRZ format, so that none of the interface bandwidth is used for clock signals. Ten Mbit/sec bandwidth can thus be achieved with existing cables and connectors, with microcode and circuitry changes for ESDI in the controller.

Another important feature is that data separation is moved from the controller into the drive itself. This means that only one manufacturer is responsible for the entire data read/write path, for less supplier finger-pointing. Eliminating the cable at that point increases data reliability as well.

ESDI also includes configuration reporting, so various drives can be used with the same controller. Upgrades by drive swapping are thus made very simple. Assuming, of course, that manufacturers' implementations are similar. The ESDI spec allows for various options, so implementations may vary from one firm to the next.

ESDI options Micropolis (Chatsworth, CA) offers include hard or soft sectoring, programmable sector length, diagnostics, defect reporting, power sequencing and track and data strobe offsets (**Figure 3**). ESDI includes both step and serial mode operation. Step mode is similar to ST506, providing few advantages over the older interface.

A third higher-speed drive interface has been approved as ANSI standard X3.101. When committee work began in 1979, 5¼" drives were not yet popular, and 8" was originally part of the title. X3.101 was designed to provide status information and allow diagnostics and error recovery. The lack of these features and high costs were seen as problems with SMD.

The control bus for this interface consists of eight signals plus a parity line. Control and status functions are extensive, with over 40 commands available. The spec also provides nearly 40 drive

Figure 3: The 1350 Series of drives from Micropolis uses the ESDI, with data separation on the drive.

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attributes which a controller can access in a table to format and operate the disk.

Though the costs to implement the ANSI interface on the controller are less than ESDI, implementation at the drive is more expensive. At this point, many of the 5¼" drive support ESDI. Ready availability of ICs for another interface could change that picture. But meanwhile, more 8" drives than 5¼" may be released with ANSI spec. Many predict that ESDI is only an interim solution to the 5¼" high-performance interfacing problem. More extensive status reporting and error recovery will likely be needed eventually.

Interface To The System

Until recently, interfacing to the host system was an issue dealt with only by controller and subsystem manufacturers. But a new movement is emerging to integrate the controller functions into the drive. Often called intelligent drives, these products present the control or host level interface directly out of the drive.

The two interfaces at this level most talked about to accommodate high-performance 5¼" drives are SCSI (Small Computer System Interface)and IPI (Intelligent Peripheral Interface). Both are peripheral interfaces, not specifically disk drive interfaces. The I/O flexibility and standardization provided with such generic buses are major advantages for system integration.

SCSI is an extended version of SASI (Shugart Associates System Interface), developed for disk drives in 1980-81. A vast majority of 5¼" drives now being shipped use the SASI interface. With SASI as a base, the ANSI X3T9.2 committee added provisions for bus arbitration and variable command lengths (seen as major limits on SASI) and modified the interface to common needs; SCSI is near final approval as a standard now.

Using a 50-pin cable bus, the interface consists of 18 non-multiplexed signals. Of these, nine are control signals; of the nine data signals, eight are data lines and one is used for parity. Since signals are not multiplexed, an SCSI bus can accommodate eight devices, but with arbitration, more than one of the eight devices can be a host (**Figure 4**).

The bus can operate up to six meters with single-ended drivers or 15 meters with differential. There are also two modes of operation, synchronous for up to 4 Mbytes/sec and asynchronous for up to 1.5 Mbytes/sec. Since current implementations are asynchronous, they are limited to 1.5 Mbytes/sec.

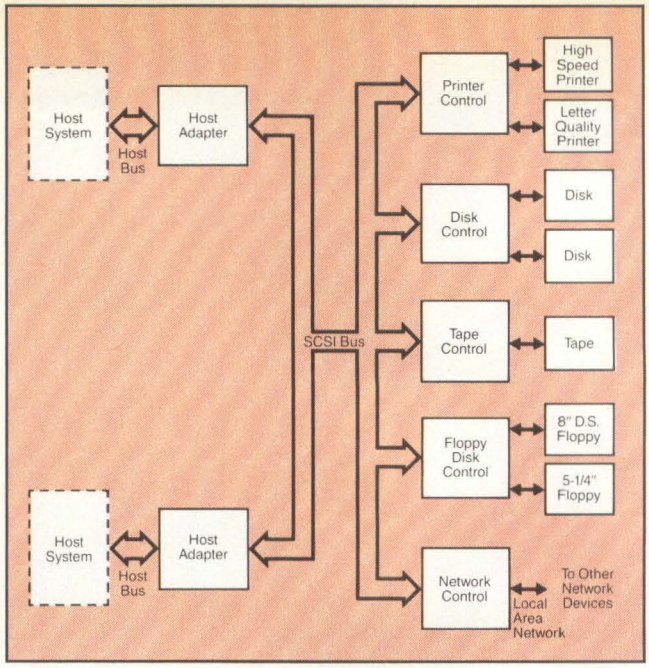

Figure 4: SCSI architecture includes the ability to have more than one host, and various types of peripheral devices. Eight SCSI ports are possible on one bus, with any mix of hosts and targets as well as controllers with several devices attached.

One of the most attractive aspects of SCSI is that many controller, disk and tape drive manufacturers have announced support of the standard. A group of these companies began the SCSI Forum (now independent), to travel the country and explain the interface.

The ability to arbitrate between more than one host means resource sharing, both for common access to files and for amortizing the cost of high-performance peripherals. The interface is also self-configuring, so no SysGen is needed for various devices. SCSI can also ease host burden and I/O tie-ups: target (peripheral) devices can time-out off the bus while performing a host-commanded operation. This makes overlapping seeks possible. With a direct copy command, copying disk to tape requires only initialization and final okay from the host across the bus. In addition, SCSI uses logical addressing so no host mapping of physical parameters of the peripheral is needed.

SCSI's relatively simple architecture and support of multiple devices per controller allow low cost system implementations. Breadth of industry support has produced enough demand that ICs for SCSI interface and protocol control are becoming available from firms such as NCR (Colorado Springs, CO). The cost advantages of integrated components are multiplied by multiple sourcing at all levels, from chips to controllers.

When SASI was first brought to ANSI, another host interface, the Intelligent Peripheral Interface (IPI), was already in committee. IPI, under ANSI X3T9.3, is not an outgrowth of any existing interface. Like SCSI, commands and data are transferred across the bus in parallel. IPI uses one cable up to 125 meters (400') long and transfers are at speeds to 10 Mbits/sec. Only one host is allowed, with up to eight slave devices. This difference from SCSI may make it less flexible, but single host set-ups generally have lower associated software overhead.

Both the structure and the documentation for IPI are in levels. The physical and link protocol levels, in the first document, have won ANSI committee vote, and primitive (Level 2) and upper-level commands (Level 3) are nearly complete.

Five of the six control signals used in IPI sequence transactions; two are controlled by the slave, or control unit and three, by the host, referred to as the master. Viewing the IPI structure as a state machine, these five control signals have 32 possible states; twelve are not allowed, leaving 20 valid states in which the bus can exist. SCSI, in comparison, has eight phases. The sixth control signal is an interrupt from a slave to indicate that it requires service from the host.

IPI allows single or double byte wide transfers, as it has two eight-bit plus parity data buses that can be concatenated. Normally, data Bus A is controlled by the master and Bus B, by the slave. Each is a byte-wide bus with parity. Like SCSI, slave devices can be any of a variety of peripheral devices.

These host-level interfaces can be incorporated directly into the disk drive, if desired. Controller manufacturer Xebec (San Jose, CA) has entered into the drive market, using their controller experience to produce drives with the SCSI directly to the host. These 5¼" drives are not,

however, at the high end. The S1410 Owl drive is 10 Mbytes formatted, using four heads; it is targeted at single-user systems. With a single drive and single computer, integrating the interface into the drive is easier and more cost-effective than having two interface levels.

When several drives are to be connected to the same system, as in applications requiring the speed of overlapped seeks, one controller with several drives will be less expensive. On the other hand, when a moderately sophisticated microcomputer system is being designed, using an intelligent drive could allow integration to be speeded enough to meet a narrow market window. At the high performance end, Priam's 507 SCSI 5¼" drive packs 153.5 Mbytes unformatted, and average access time is quoted as 25 msec.

It looks as though several manufacturers will soon offer similar drives in regular and intelligent configurations. More choices will be available for systems in various applications without changing suppliers. As system configurations expand, there will no doubt be room for several interfaces and different segmentation of the disk drive functions.

Choosing A Drive

The range of products available in the 5¼" form factor is expanding rapidly, and as other small drives, some will have short life spans. In the longer term, systems may demand 20-100 Mbytes for a vast middle range and as much as several hundred Mbytes for high-end systems.

Technological advances that allow fast access to large volumes of information are available already. But availability may be spotty for some time, both due to demand and to advanced parts. The more new technologies a drive uses, the more emphasis should be placed on testing and reliability. Conservative technologies can pack 80 Mbytes and up, and companies from Seagate to Computer Memories (Chatsworth, CA) are stretching the limits to compete with new technologies.

Choosing an interface and deciding where to place data separation and controller electronics may be another decision that can be delayed. Using RLL coding and using drives with increased track, but not bit densities, ST506/412 will remain the overwhelming standard for a while. But it may be wise to consider newer interfaces for easy product upgrade.

Reliability is the largest item to consider in choosing a drive. Off-shore manufacturing is prevalent, and though usually satisfactory, the distance between home office and manufacturing plant could be a problem for drive suppliers.

In the current unstable rigid disk drive market, choosing a supplier should be the prerequisite for any drive choice. The shakeout is beginning now, and firms that do not have both a firm customer base and financing could be risky. That does not count out young companies; many have well-designed drives and good backing. Some of the firms that look like they are in trouble, on the other hand, have volume manufacturing ability that is hard to equal. DD

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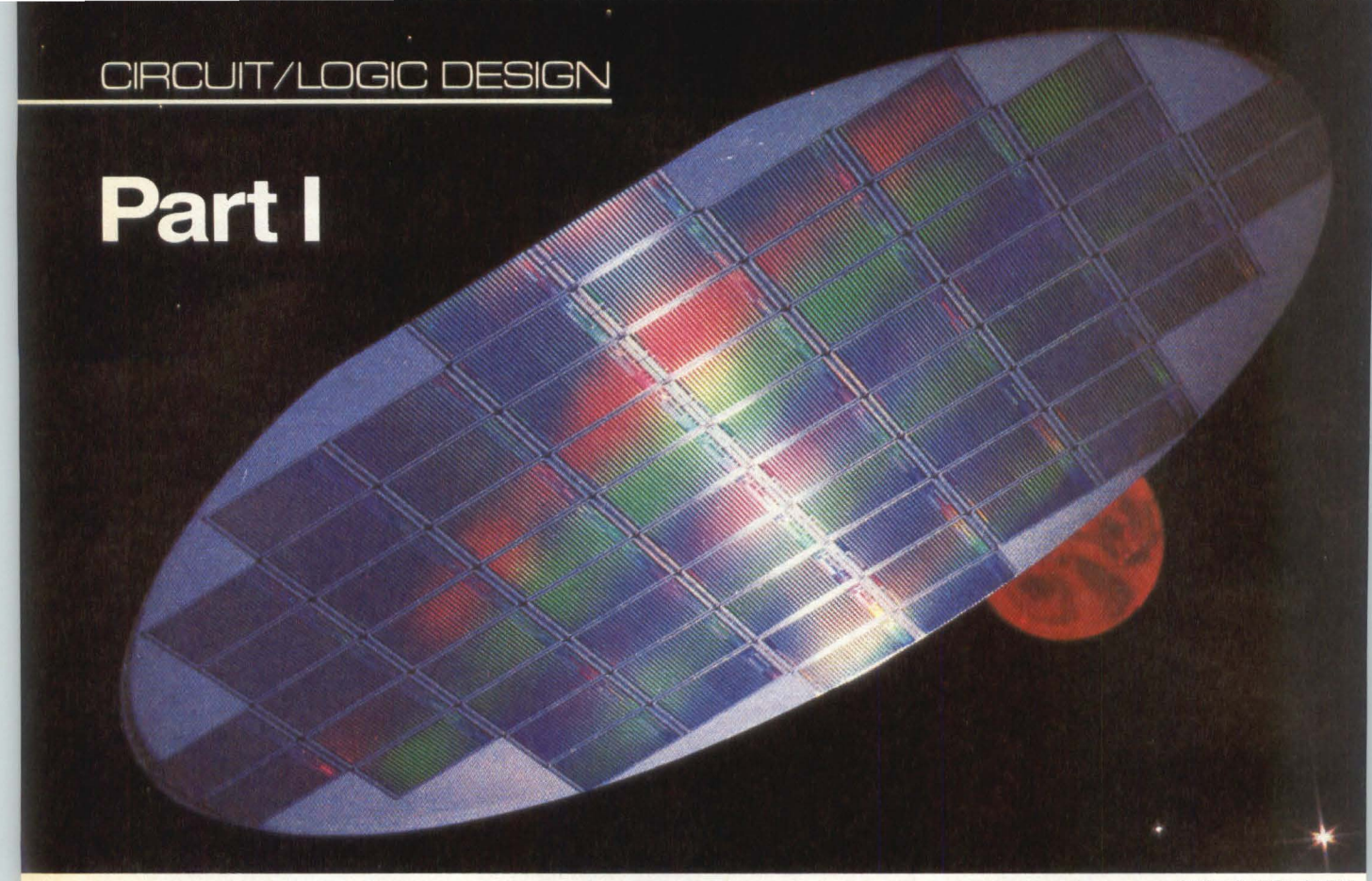
Part I



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Unlocking The Mysteries Of Gate Array Design

by Ronald Collett, Sr. Technical Editor

Without a doubt many OEMs in the industry are not in a position to make a "trial and error" analysis of the tools and technology that surround gate array design. With this in mind, *Digital Design* is undertaking a project to uncover the facts, uncertainties and mysteries of using an engineering workstation to design a gate array.

Preparing an article on a particular aspect of the electronics industry requires three ingredients: performing a fair amount of background research, speaking with selected experts in the field, and making an analysis of the product offerings from the various manufacturers. Following this path usually leads to a reasonably good overview of the industry's recent technological advances, but in some instances, this approach falls short.

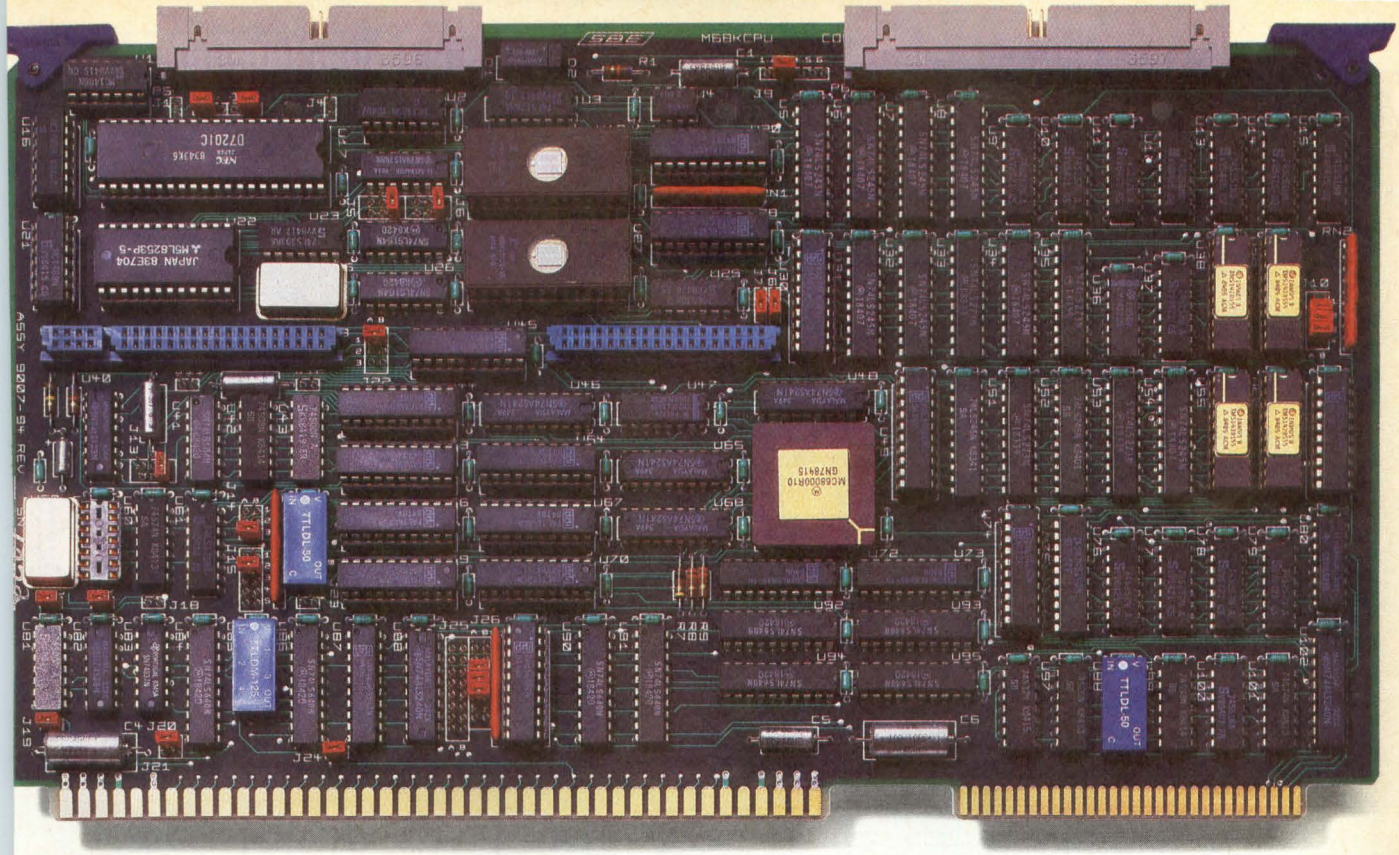
Such is often the case when a developing technology gains acceptance and grows in popularity at an overwhelming rate. Frequently, the literature published about fast growing areas consists of biased opinions from a few key manufacturers, as well as a summary of the various offerings from the individual competing vendors. This is not to say that such a review is useless, rather it serves as a product update and a cursory look at the technology.

From our perspective, unless we are able to get behind the scenes and design our own chip, digging out the subtle quirks, problems, and potential stumbling blocks is virtually impossible. In addition, not only is the gate array market growing at a phenomenal rate, but the use of engineering workstations is expected to increase drastically as well. So the goals of our project are twofold: to investigate the issues of gate array design and engineering workstations.

Areas Of Concentration

Similar to most design projects, a gate array development cycle can be divided into two phases—the front-end and the back-end. The front-end includes all design tasks that take place before handing over the design data (netlist, simulation/verification data, test vectors) to the gate array vendor for fabrication. Once the vendor receives the chip specifications, the project is in the back-end phase and is essentially out of the customer's control.

In this multipart series, our primary area of reporting will focus on the front-end of the design cycle. In short, the areas to be covered include the following:
(1) differences between using off-the-



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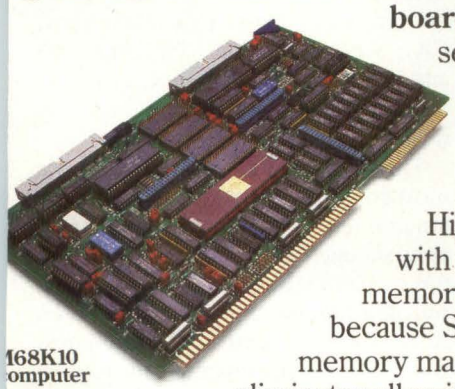

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shelf components and a cell library; (2) workstation capabilities: schematic capture, timing analysis, and logic simulation; (3) gate array vendor requirements; (4) packaging, I/O and technology considerations (CMOS vs. bipolar); (5) equipment and design methodology training courses.

After the front end is completed, we will monitor the chip's progress, especially with respect to turn-around time. Furthermore, any follow-up vendor-customer interfacing that takes place during this time period will be documented. And finally, we will report on whether the array functions as specified and performs as expected when implemented in a system.

Selecting The Workstation And Vendor

Choosing the vendor and the tools is the first step in a gate array design project. Unfortunately, the two are not independent of each other, and thus must be considered simultaneously. In making the selection, we looked at three of the most common situations that exist.

First, the systems architect may be only concerned with finding a gate array vendor and not interested in purchasing a workstation. If this is the case, the vendor's proprietary CAD/CAE system will be used, and the designer will take a one to two week course to learn how to operate the system, master the firm's design methodology and get some hands-on experience.

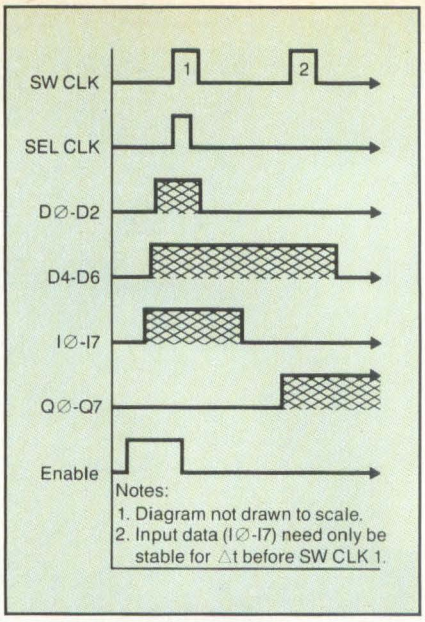

Figure 2: The timing diagram of the Digital Crosspoint Switch illustrates the relatively simple operation of the device. Note that two clock pulses on Switch-Clock are required to transfer data from I (0-7) to Q (0-7).

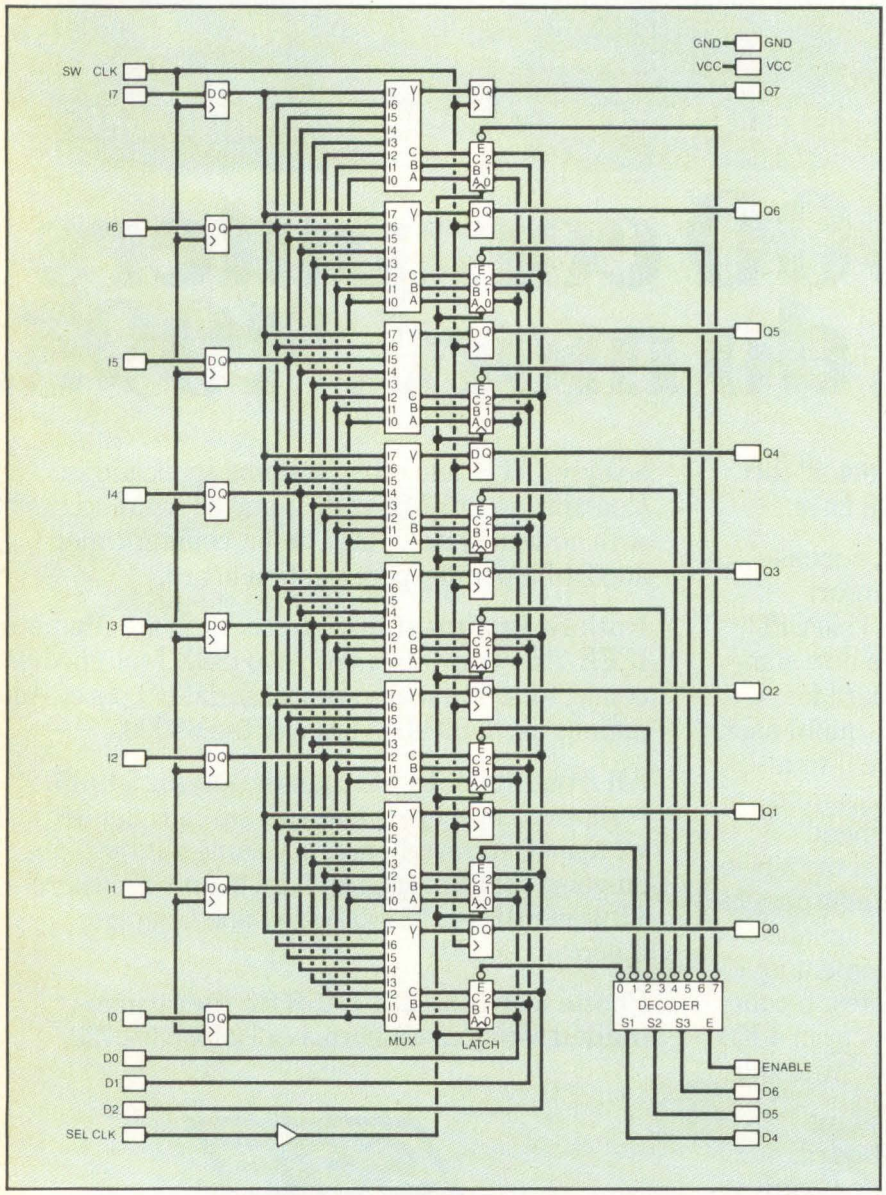

Figure 1: The Digital Crosspoint Switch allows any data-bit on I0-I7 to be switched to any output line (Q0-Q7). It will be implemented using a CMOS gate array and will operate to 20 MHz.

The second possibility manifests itself when the customer already owns, or plans on purchasing, a particular workstation. In this situation the systems architect must search out a gate array vendor that supports the particular workstation. In short, the vendor must be willing to accept a netlist in a format unique to that workstation and reformat the data to make it compatible with their own CAD/CAE system and fabrication process. Presently, Daisy (Mountain View, CA), Mentor Graphics (Portland, OR) and Valid Logic (San Jose, CA) are the workstation manufacturers that gate array houses most commonly support.

The third possibility, and perhaps the most common, crops up when the customer is unfamiliar with the various gate array suppliers and workstation manufacturers. If this is the case, we strongly recommend that the chip-maker be chosen first, since getting ICs is the foremost goal. (For a more complete analysis of choosing a vendor, see *Digital Design*, June 1984).

Workstation Selection

If we assume that a particular vendor has been selected, then as far as the CAD/CAE tools are concerned, the systems architect can use either the firm's proprietary tools or commercial workstation.

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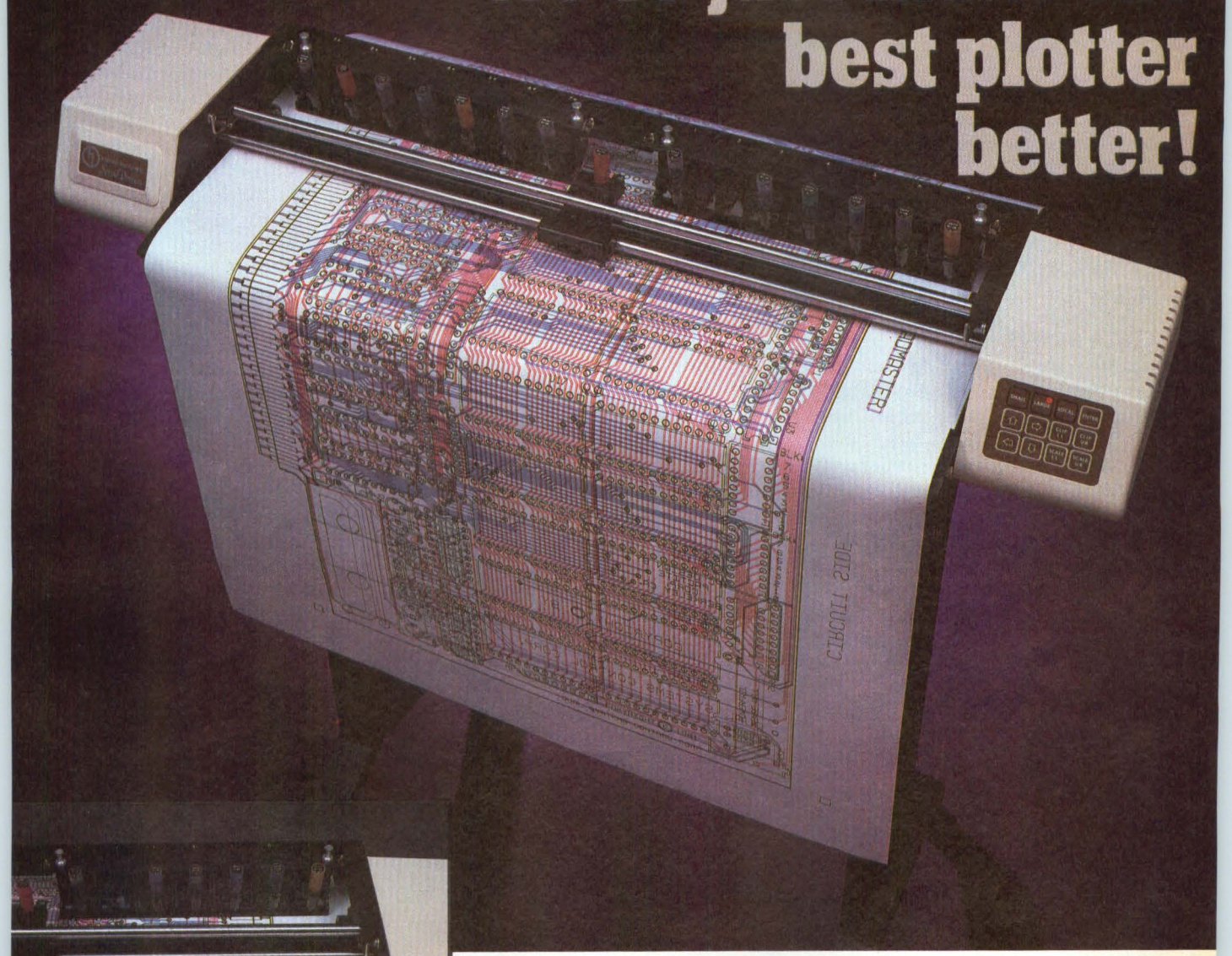

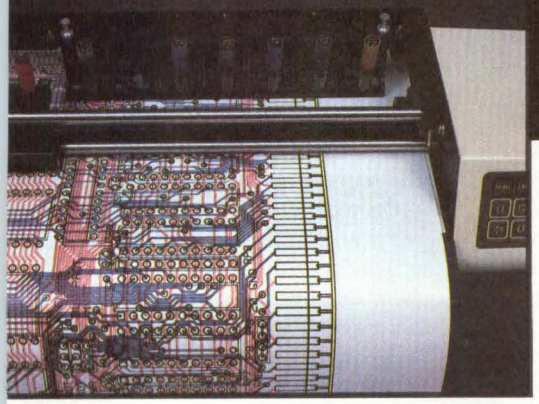

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Often, the vendor will have one or more of these third party CAD/ CAE systems available at their design centers. (Design centers are typically located in cities throughout the United States and Europe). If the systems architect chooses to do a design on a commercial workstation owned by the gate array vendor, then the design must be performed at the design center. (No vendors, to our knowledge, will allow you to haul away one of their workstations.) This may not present a problem if the design center is located near the OEM's facility; however, if this is not the case, it may not be feasible for the customer to remain there for a lengthy time period. Alternatively, the customer may be able to lease a line which is linked between his facility and the vendor's proprietary CAD/CAE system.

For our design project we chose to use a Valid Logic workstation and to execute the design outside of the design center. In essence, the situation is parallel to a customer purchasing a Valid Logic system, having it reside at his facility and installing the gate array vendor's cell library on the system.

Cost savings is the primary advantage of using a commercial workstation, as opposed to a proprietary CAD/CAE system. When using the vendor's host, computer costs incurred for a single design can range anywhere from $2 to $7 per gate. In comparison, costs of a design executed on a workstation can be as much as 80% lower. For those considering designing multiple arrays, doing the front-end of the design on a workstation is clearly more cost effective. If designing a gate array is an isolated event (i.e., a customer plans to do only one design), then the likely choice would be to use the vendor's proprietary system.

Although we are only performing one design, we put ourselves in the position of an OEM who would be designing several arrays and wished to purchase a particular manufacturer's workstation. In deciding which workstation to use, the top three contenders were Daisy, Mentor and Valid. The reason these three were nominated is because of their agreements with a multiplicity of gate array houses. Upon investigating their capabilities, we found each to be a high quality system tailored specifically for the electrical engineer.

In addition, all three are completely integrated systems. We were concerned about the possibility of encountering compatibility problems between various application software packages if we selected a general purpose system and then acquired third party software.

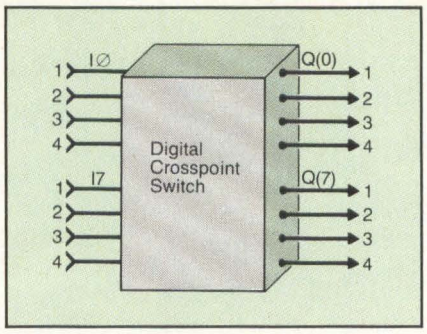

Figure 3: In the expanded configuration, the Digital Crosspoint Switch can transfer four data-bits simultaneously. If two of the devices are daisychained, eight bits can be transferred concurrently, etc.

We also reasoned that since UNIX is becoming a recognized standard, many potential buyers would select a UNIX-based system. Consequently, we demanded that our workstation be able to run a well accepted version of the operating system. The UNIX requirement eliminated Mentor from the running since their system is Apollo based, and the UNIX porting effort at Apollo Computer Corp. (Chelmsford, MA) is still under development. This was not an easy decision since the Mentor system offers more computational horsepower (equivalent to a VAX 11/780) than either Valid or Daisy—at a higher pricetag of course.

Daisy claims that their workstation runs UNIX, but the porting effort was only recently completed, and the success has not yet been fully validated. When UNIX is ported to fit a particular processor, much of the source code must be altered, and this can lead to subtle, yet significant bugs in the operating system. The UNIX issue, however, did not eliminate Daisy since the firm does offer the capability. So with both Daisy and Valid remaining, it was a "toss-up."

In the final analysis, the choice was made by speaking to present users who were familiar with both vendors' equipment. We chose the Valid Logic workstation for several reasons. First, although most users cited the similar computational horsepower of the two, several users claimed that entering a schematic on the Valid system was an easier task. (It should be noted that with any random sampling, some bias may exist.) Second, all of Valid's software can run both UNIX and DEC's VMS operating system. And since many OEMs currently own or have access to a VAX, such an OEM would perhaps purchase a system whose software can run under the VMS operating system. And finally, the Valid system was originally designed to run UNIX, so problems that may have occurred during the porting have most likely been eliminated.

When we evaluate the performance of Valid's Scaldsystem I, a 68010-based system, some of the capabilities that will be examined include schematic capture, timing analysis and logic simulation. We will also make an effort to compare the various capabilities among systems offered by other vendors, since Valid is obviously not the "only game in town."

Vendor Selection

When we selected the Valid workstation, we also had an eye on those gate array vendors that supported Valid's line of products. Several vendors were considered before narrowing the selection down to LSI Logic (Milpitas, CA) and Fujitsu Microelectronics (Santa Clara, CA).

From word of mouth, recommendations were provided which substantiated the reputations of both. LSI Logic's faster CMOS arrays, however, became the deciding factor. Our circuit, which we chose to implement in CMOS, will be operating at a minimum clock speed of 20 MHz, and Fujitsu's CMOS has a maximum clocking speed of 16.3 MHz. Fujitsu has a line of bipolar arrays that would have met the speed requirement, but again, our circuit specification called for CMOS technology. LSI Logic also offered a larger selection of array sizes and this was a critical issue. (Selecting a vendor that offers a wide range of array sizes may seem influential but not critical. However, in Part II we will expand on why this is indeed significant.) And finally, although both vendors have agreements with Valid Logic, Fujitsu's Valid-based cell library was still in beta-site testing. (We were given permission to use it, but it was not yet available for commercial use.)

The Digital Crosspoint Switch

The design which we plan to implement is shown in **Figure 1.** Briefly, the Digital Crosspoint Switch, designed by Datacube (Peabody, MA), allows any single bit of input data (I0-I7) to be switched to

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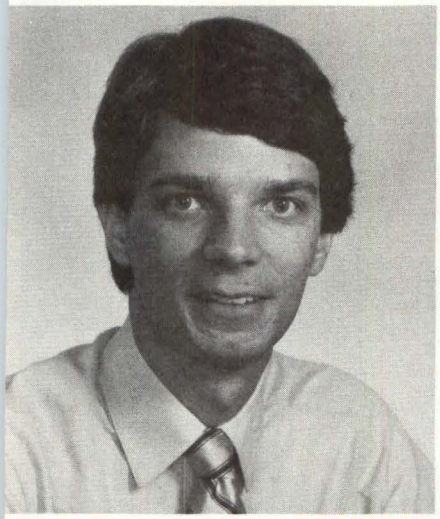

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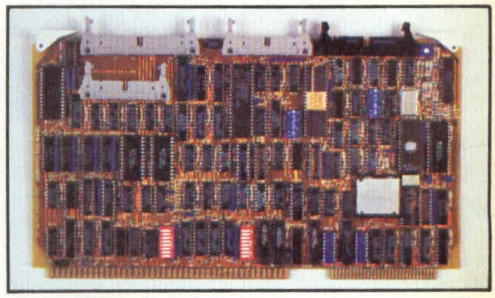
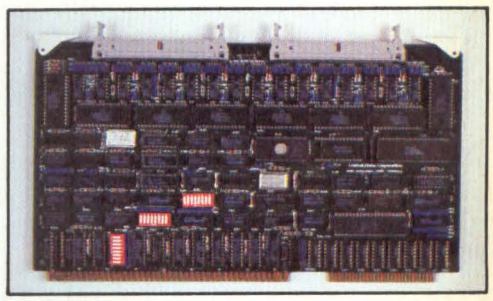


The new **Multibus Multi-Media Controller** is the industry's first to support up to 12 storage media — four each 5¼" Winchester disks, floppies and QIC-02 streaming tape drives, and at an economical price. On-board buffers provide 1:1 interleave transfers and the board supports both bus-vectored and non-bus-vectored interrupts. The board self-tests internally and corrects up to 11-bit burst errors with a 32-bit ECC for Winchester drives. For even greater performance, an optional iLBX* DMA interface is available with the board's (80188) 8/16-bit processor. The **B1030** is available in 100 up pricing at $895.



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any output (Q0-Q7) line. Pipelined architectures are one of the primary applications for the crosspoint switch since it can be used to route data through various processing stages.

The primary impetus behind integrating the crosspoint switch onto a gate array is to reduce the number of ICs necessary to implement the function. Its present implementation in programmable logic uses 12 PALs for a single 4-bit wide switch. Since an 8-bit datapath is used on the board where the switch is found, 24 PALs are being utilized. So as far as the number of ICs saved, the gate array represents an improvement ratio of 12:1.

The operation of the switch is quite simple, but requires a short explanation. The data is first routed to one of the eight input lines. The appropriate multiplexer is then selected via the 3-to-8 decoder. (The output of the decoder actually enables that multiplexer's 3-bit select register). Once the multiplexer is selected via the 3-bit register, the output stage of the crosspoint switch is in the proper mode. The multiplexer data input (I0-I7) signal is then selected via the three data select lines (D0-D2). When the three lines are stable, a clock pulse (Select Clock) is sent to the 3-bit register to move the mux-select data into the multiplexer; although the Select Clock is common to all 3-bit registers, the only latch enabled is the one selected by the decoder. At this point, the input and output stages of the crosspoint switch have been configured, and the firing of the Switch Clock is all that remains to transfer data from the input to the output stage. Note that two Switch Clock pulses are required to transfer the data completely—one to get the data through the input stage and a second to get the data through the output stage; see the timing diagram of **Figure 2**.

Another aspect that makes the device even more useful deserves mention. Suppose, for the moment, that the device were to be implemented as shown in **Figure 1**. In this configuration, only a single bit of data would be switched from the input to the output. And since data usually travels in 8-, 16- or 32-bit chunks, switching serially a byte, or word, would require 16, 32 or 64 clock cycles. For this reason, the switch would be far more valuable if it could transfer several bits simultaneously, i.e., in parallel. To accommodate this need, we plan to incorporate four of these switches into a single chip. As a result, only two chips will be required to simultaneously switch 8 bits; four chips for 16 bits; etc.

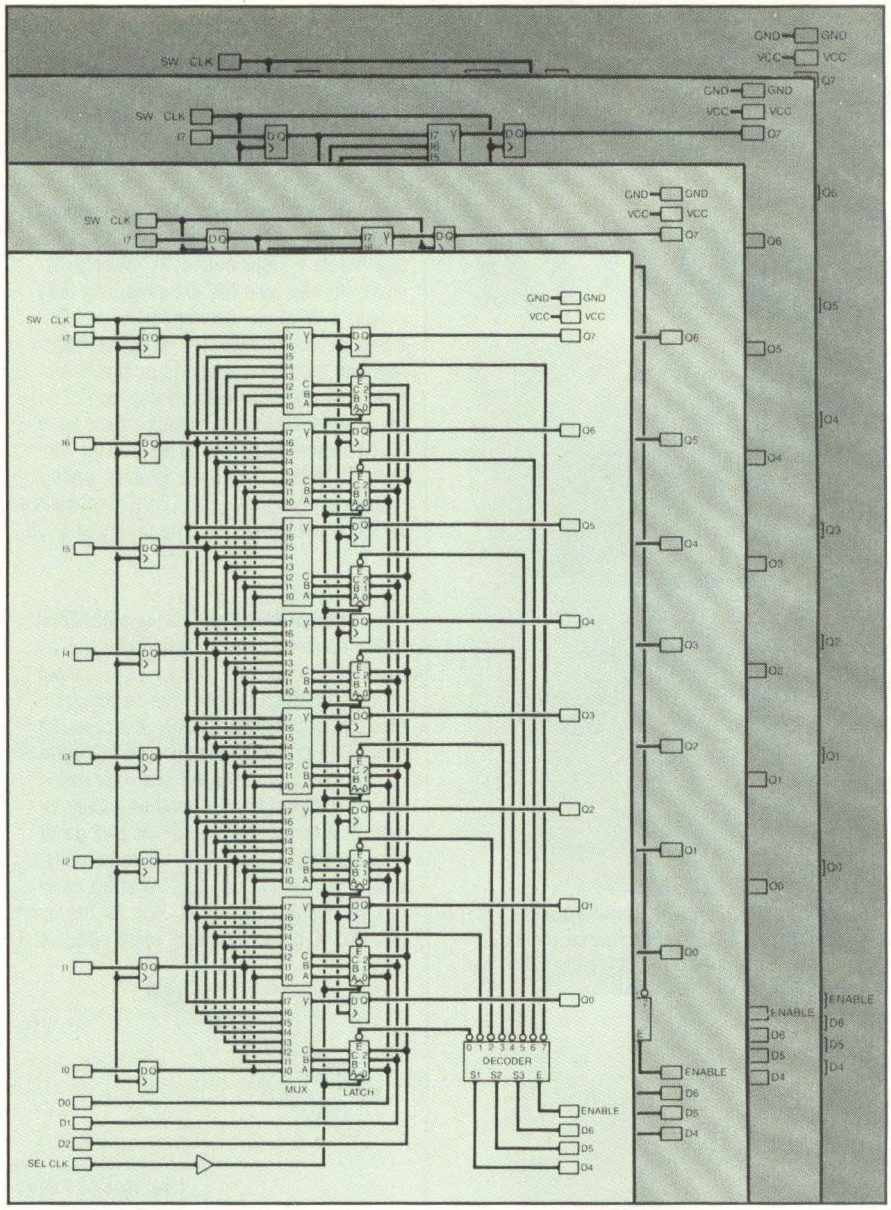

Figure 4: Implementing the expanded configuration of the Digital Crosspoint Switch requires duplication of all input flip-flops, output flip-flops, and multiplexers. But the reward is a 400% increase in efficiency.

To make this enhancement, the input and output flip-flops and the multiplexers will have to be duplicated four times; see **Figures 3 and 4**. But neither the 3-bit registers nor the 3-to-8 decoder need be added. This expanded configuration increases the efficiency of the device by 400%. Instead of only one data-bit being switched on each pair of clock pulses, four bits are switched.

Conclusion

In Part II we will discuss the substantive design issues, our accomplishments, and the problems that we have encountered. In addition, we will be taking a close look at both the Valid Logic workstation and the LSI Logic design methodology, as well as the compatibility between the two vendors. DD

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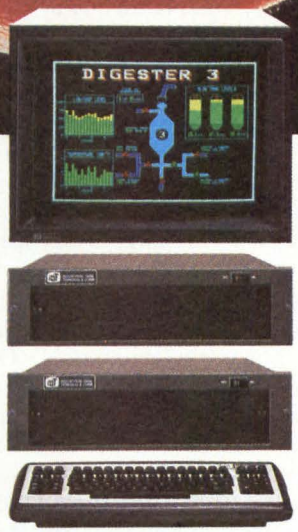

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Design Options Increase For Users Of 256K Dynamic RAMs

by Brita Meng, Technical Editor

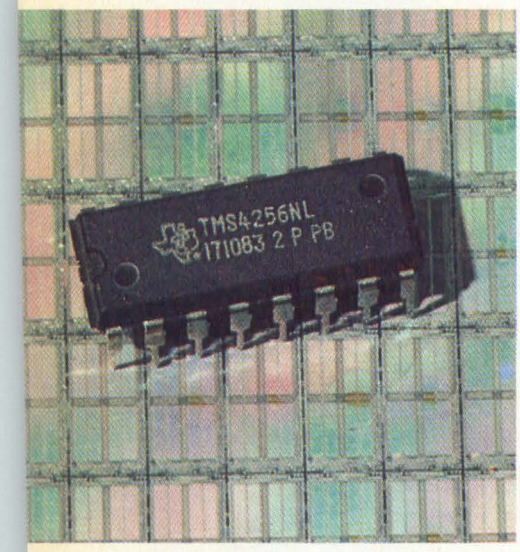

Figure 1: The Texas Instruments 4256 operates in page mode and is upward pin compatible with TI's 64K DRAM, the 4164.

With the advent of the 256K dynamic RAM, the market for memory devices has grown large enough to support the application-specific development of memories; the era of the commodity chip is over. The new generation of 256K dynamic RAMs (DRAMs) are not only ideal for mainframe applications, but also for applications such as graphics systems, workstations, portable computers and microcomputers hungry for larger, faster memories. As **Table 1** illustrates, more options for DRAM operation are available on the 256K DRAM generation: manufacturing technology, data access and refresh modes, redundancy, architecture and packaging.

CMOS Vs. NMOS

Soft errors, aggravated by the higher density demands of the 256K DRAM, have caused manufacturing technology to become more of a concern to designers and users of DRAMs. CMOS technology may prove to be the most cost-efficient solution for manufacturers seeking increased immunity to soft errors because the fabrication method inherently provides a reflecting barrier to alpha particles. Currently, Intel Corp.'s Memory Components Div. (Hillsboro, OR) is the only group producing CMOS-based 256K DRAMs. Advanced Micro Devices (Sunnyvale, CA) is in the process of developing a CMOS 256K DRAM which, according to an AMD spokesman, will be in production by the third quarter of 1985.

Designers of NMOS-type 256K DRAMs have overcome the problem of soft errors for the 256K generation either by using insulators such as silicon nitride, which has a higher dielectric constant than the traditional silicon dioxide, to increase the stored charge in the capacitors or by employing folded bit lines, which are made of aluminum rather than n+ diffusion, to decrease bit line capacitance. The upgradability of NMOS devices may reach its cost limit soon with the development of even higher density memories such as the 1Mbit DRAM. Comparisons of costs for high volume production of high density NMOS and CMOS DRAMs cause most engineers to view CMOS technology as the most cost-efficient manufacturing method for future generation DRAMs.

Power requirements are also important considerations in selecting a DRAM. Since all DRAMs require periodic refresh charging to maintain data storage, the amount of power needed to perform this refresh is an important consideration. Average operating power dissipations for NMOS and CMOS devices are similar, ranging from approximately 200-350 mW. On the other hand, standby power dissipations for the devices can differ drastically: CMOS DRAMs require about 0.5 mW, whereas NMOS devices need up to 30 mW. However, CMOS devices do not eliminate the necessity of charging internal nodes and therefore may achieve high peak current levels similar to NMOS DRAMs. As a result there may be little difference in current requirements between the two technologies when each memory is cycled at maximum speed, regardless of the lower standby power in CMOS devices. Nevertheless, the low standby power requirements of the CMOS 256K DRAM make it the ideal choice for engineers designing systems needing low power consumption, battery backup or both. If low power is not a vital consideration, the price of a CMOS DRAM may deter engineers from its use.

Enhanced Operating Modes

The 256K DRAM operates as a read/write random-access memory, in addition to several optional data access modes. For the most part, companies seem to be following the strategy of offering both page mode and nibble mode on their 256K × 1 DRAMs. Other operating modes either currently offered or in development are extended nibble, streaming, static column and clocked static column modes. All of these higher bandwidth modes of operation apply to single-ported memories; there are several manufacturers working on dual-ported memories for applications in data acquisition and high speed graphics.

Page mode was developed in the mid 1970s as a way to increase memory bandwidth. Any combination of read, write or

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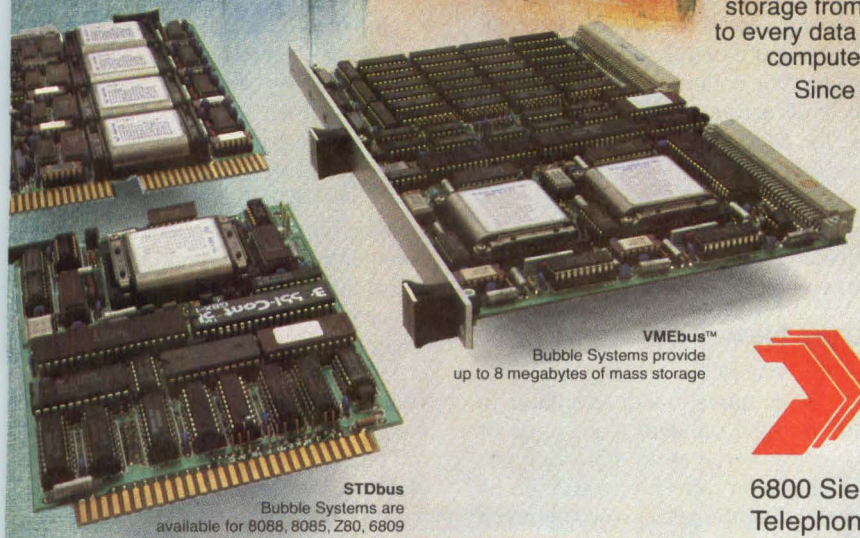

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Until now high density DRAMs have been known primarily for their increased storage capacity, but new features make these devices far more versatile.

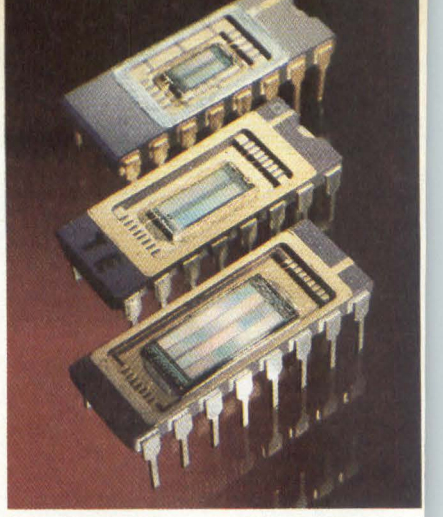

Figure 2: Generations of DRAMs by Siemens (Iselin, NJ); the 16K DRAM (top), the 64K DRAM which has 10,000 transistors per mm²

read/modify/write may be performed in page mode. It enables the system user to access the data from the entire row of 256 memory cells with fast access times. The row address strobe ($\overline{RAS}$) is left low in order to latch in sequential column addresses by the column address strobe ($\overline{CAS}$). Page mode enables the user to perform multiple column address cycles, thus decreasing the normal cycle time of both row and column address strobes to just the access time of the $\overline{CAS}$. Since each $\overline{CAS}$ addresses and decodes, page mode allows random addressing to any location on the accessed row. The number of cycles in page mode is limited by the amount of time $\overline{RAS}$ can remain active; however, manufacturers of page mode DRAMs have been able to begin extending this time period. For example, Intel's Ripplemode feature enables a user to transfer a full page of 256 words within a single $\overline{RAS}$ cycle.

Nibble mode is another attempt to take advantage of the internal organization of the address multiplexed DRAM. A 4-bit serial shift register enables one of four output decoder logics, selecting the data bit for the output buffer. The register is incremented by cycling $\overline{CAS}$. Nibble mode provides moderately high bandwidth for 4 bits because the data and the output buffer are adjacent and because new addresses need not be latched and decoded. However, since nibble mode is only a 4-bit operation, multiple access must be performed for most microprocessors which require either 8 or 16 bits. An extended nibble mode allowing 8 bit nibbles or a streaming mode allowing sequential access of the entire row address field may solve this problem for future 256K dynamic RAMs. The apparent fourfold increase in bandwidth due to implementing nibble mode is limited by the time overheads needed to precharge $\overline{RAS}$ for the next cycle and to access the first bit of data. If precautions are not taken during system interleaving, designers may experience drops in this bandwidth increase.

Static column mode offers the random access feature of page mode without the 4-bit limitation of nibble mode. Only the row addresses are latched; the column address buffers are static. The column address becomes stable after decoding the row address field and sending the desired row of data. As long as the address lasts, the output will remain valid. Again, the bandwidth increase for static column mode is limited by the time required for the system to latch the data and to change the address.

Clocked static column mode currently provides the highest bandwidth available for single port architectures. In this mode, the $\overline{CAS}$ precharge time is hidden within the column address time. As soon as the column address satisfies its hold time, it can be changed. While $\overline{CAS}$ is inactive, the column address ripples through the address decoders; when $\overline{CAS}$ is active, the address is latched and enables data output. For designers deciding between static RAMs with external registers and dynamic RAMs utilizing clocked static column mode, the performances of each are about the same. However, the cost per bit of the DRAM is much less. The achievable bandwidths may allow designers to decrease the amount of interleaving between memory device and system and to decrease the word width.

Other New Features

The new generation of 256K DRAMs makes three refresh modes available in addition to the standard read, write or read/modify/write cycle. $\overline{RAS}$ only refresh enables a refresh operation to be performed on the select row anytime a $\overline{RAS}$ signal occurs. Hidden refresh which toggles $\overline{RAS}$ while $\overline{CAS}$ is low allows memory refresh by subsequent row addresses after the initial $\overline{RAS}$ cycle. The data read during the first row cycle remains valid during the following refresh cycles. $\overline{CAS}$ before $\overline{RAS}$ refresh takes advantage of the fact that all manufacturers specify that $\overline{RAS}$ goes low before $\overline{CAS}$ for standard memory operation; the opposite sequence causes a refresh prompt. Upon receiving the prompt, a refresh address is loaded into the row address buffers from an internal address counter, causing the address counter to be incremented and accomplishing a refresh maneuver.

Although all other companies in the DRAM market seem to feel that offering all refresh options to designers is necessary, Intel manufactures its DRAMs solely with $\overline{RAS}$-only refresh because the company feels that most engineers prefer the $\overline{RAS}$-only mode to either $\overline{CAS}$ before $\overline{RAS}$ or hidden modes. If the latter two refresh modes do become standards, Intel may find itself in the position of revising its chip to make the options available.

To most manufacturers, redundancy, implemented by either electrically-blown or laser-blown fuses, is a necessary characteristic of the new 256K DRAMs. Only one 256K DRAM manufacturer, NEC (Mountain View, CA), does not implement some form of redundancy, eliminating it through production techniques and quality control. Whether NEC's stance will change due to escalating production and development costs of future generations of DRAMs remains to be seen. Most large memory houses feel that the purpose of redundancy is not to control quality or reliability, but to enhance yields during the early production stages.

Micron Technology (Boise, ID), a smaller company in the 256K DRAM market, has developed an error-correction scheme to increase the reliability of

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Table 1: Manufacturers of 256K Dynamic Random Access Memories.

COMPANY	ARCHITECTURE	PART NUMBER	TECHNOLOGY	ACCESS TIME (ns)	MAXIMUM POWER DISSIPATION (mw) Active, Standby	DATA ACCESS MODE	AVAILABILITY	PRICE@100*
Fujitsu	256×1	81256-10/12/15	NMOS	100/120/150	314, 25	Page	Now	$25.00
	256×1	81257-10/12/15	NMOS	100/120/150	314, 25	Nibble	Now	$25.00
Hitachi	256×1	50256-12/15/20	NMOS	120/150/200	350, 23	Page	Now	$24.50
	64×4	50464-12/15/20	NMOS	120/150/200	350, 23	Page	Now	$28.00
	64×4	50465-12/15/20	NMOS	120/150/200	350, 23	Nibble	Now	$28.00
Intel	256×1	51256L-15/20	CMOS	150/200	325, 0.5	Ripplemode	Now	$128.20/ $115.45
		51256H-15/20	CMOS	150/200	325, 0.5	Ripplemode	Now	$160.10/ $141.10
		51256HL-15/20	CMOS	150/200	325, 0.5	Ripplemode	Now	$179.50/ $160.30
	64×4	51259L-15/20	CMOS	150/200	325, 0.5	Static Column	Q1'85	
		51259H-15/20	CMOS	150/200	325, 0.5	Static Column	Q1'85	
		51259HL-15/20	CMOS	150/200	325, 0.5	Static Column	Q1'85	
Micron Technology	256×1	1256-12/15/20	NMOS	120/150/200	200, 10	Read/Modify/ Write	Q1'85	
	64×4	4064-12/15/20	NMOS	120/150/200	200, 10	Page	Q1'85	
Mitsubishi	256×1	4256S-15/20	NMOS	150/200	330, 22/ 275, 22	Page	Now	$32.50/ $31.00
		4256P-12/15/20	NMOS	120/150/200	360, 22/ 330, 22/ 275, 22	Page	Q2'85	
	256×1	4257S-15/20	NMOS	150/200	330, 22/ 275, 22	Nibble	Now	$34.10/ $32.55
		4257P-12/15/20	NMOS	120/150/200	360, 22/330, 22/ 275, 22	Nibble	Q2'85	
Mostek	256×1	4556-8/10/12	NMOS	80/100/120	412, 22	Page	Q3'85	
	32×8	4856-10/12/15	NMOS	100/120/150	275, 27.5	Page	Q3'85	
Motorola	256×1	6256-10/12/15	NMOS	100/120/150	350, 22.5	Page	Q1'85	
	256×1	6257-10/12/15	NMOS	100/120/150	350, 22.5	Nibble	Q1'85	
National Semiconductor	256×1	41257-10/12/15	NMOS	100/120/150	412, 22	Nibble	Q2'85	
NEC	256×1	41256-15/20	NMOS	150/200	385, 28	Page	Now	$27.50
	256×1	41257-15/20	NMOS	150/200	385, 28	Nibble	Now	$30.00
	64×4	41254-15/20	NMOS	150/200	413, 28	Page	Now	$33.00
Oki Semiconductor	256×1	41256-15/20	NMOS	150/200	385, 28	Page	Q2'85	
Siemens	256×1	41256-12/15/20	NMOS	120/150/200	385, 28	Page	Q3'85	
Texas Instruments	256×1	4256-12/15/20	NMOS	120/150/200	300, 12.5	Page	12-Q2'85 15/20-Now	$39.00/ $35.00
	256×1	4257-12/15/20	NMOS	120/150/200	300, 12.5	Nibble	12-Q2'85 15/20-Now	$39.00/ $35.00
	64×4	4464-10/12/15/20	NMOS	100/120/150/ 200	250, 12.5	Page	Q1'85	
Toshiba	256×1	41256C-15/20	NMOS	150/200	275, 28	Page	Now	$23.00/ $20.00
		41256P-12/15	NMOS	120/150	275, 25	Page	Now	$24.50/ $23.00

*1985 prices not available at compilation time; prices given are subject to change by manufacturers.

its memory device and to compete in the market. The approach actively corrects single-bit hard and soft errors by accompanying each 8-bit word with a 4-bit check word generated with a Hamming code. According to Micron, the automatic scheme avoids the necessity of probing wafers for bad memory cells and enhances the reliability of smaller systems that, due to cost and space considerations, do not have error correction.

Various architectures for 256K DRAMs have become prominent in the market. Along with the standard 256 × 1 chip, manufacturers offer options for 64

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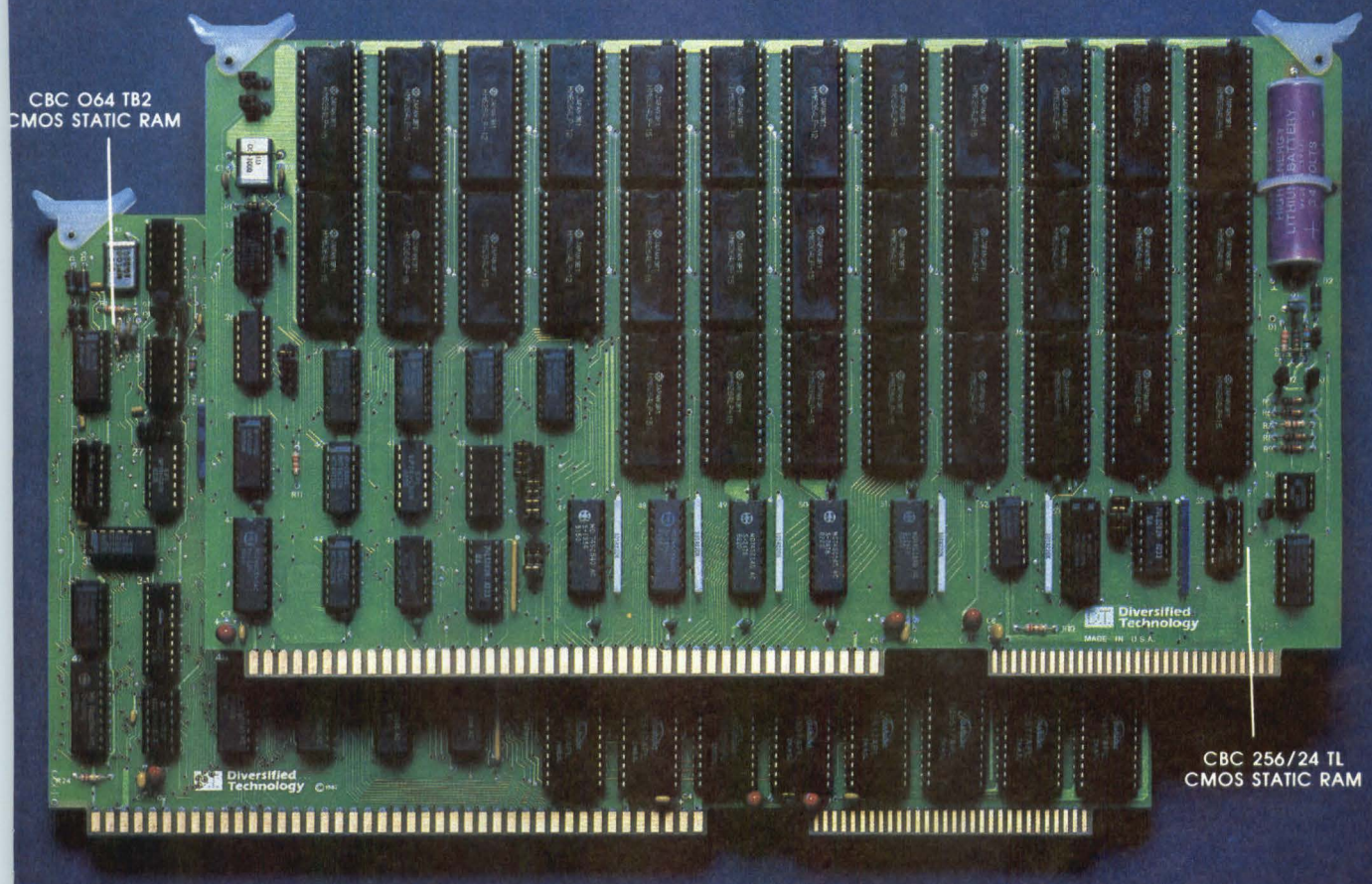

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× 4 and 32 × 8 DRAMs. This is another indication of the increasing application-specific direction of the market. Whereas the 256 × 1 devices are designed for use in mainframe computers and telecommunications, the 64 × 4 DRAMs are more suited for terminals and graphics and video applications. Mostek Corp. (Carrollton, TX) manufactures a non-multiplexed address 32 × 8 chip for the microprocessor market. More options for designers in satisfying memory size and memory speed requirements as well as expandability are available. Future generations of 256K DRAMs may be organized in architectures of 16 × 16 and 32 × 9, for example.

Packaging selection is also an increasingly complicated issue for design engineers. Currently, virtually all dynamic RAMs are supplied in DIP packages, plastic, ceramic or both, with standardized configurations. The 256K DRAM is also available in a single-in-line plastic package (SIP), a standup through-hole device. However, growing emphasis on the use of surface mounted devices exists due to the demand for methods to increase component density. Several manufacturers offer plastic leaded chip carriers (PLCCs) with either J-bend or gull-wing leads and leadless chip carriers (LCCs), feeling that through-board technology may no longer be practical for high density parts. The establishment of an industry standard configuration for such packages is now being examined by the JEDEC Memory Committee although there is indecision on the part of users as to which surface mount configuration best serves their requirements. DIPs are still first priority for the 256K memory manufacturers in a market where high volume and low cost are key considerations.

Conclusion

The achievement of the 256K DRAM means that the 1 Mbit DRAM is fast approaching. Three companies announced the successful fabrication of 1 Mbit DRAMs at the 1984 ISSCC, and four more 1 Mbit DRAMs will be presented at this year's conference. Although CMOS technology is not the predominant one for these first Mbit DRAMs, memory designers do feel that CMOS DRAMs will eventually take over the memory market. Manufacturers may take closer looks at either the triple-polysilicon cell approach or polysilicon sandwiches. More exotic materials will replace the traditional metal or polysilicon used for interconnections as cell sizes approach 1 μm. Photolithographic limits will cause memory designers to pay increasing attention to vertical processing as a way to increase the density of memory chips. Finally, the increasing number of options available for dynamic RAM operation will allow the design engineer to choose from several families of memory devices the one that best meets the requirements of his system and application. DD

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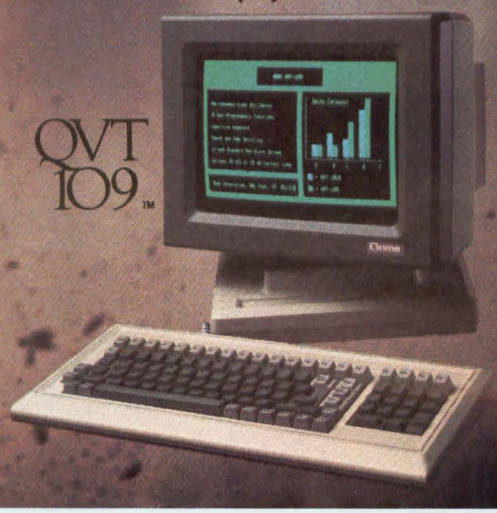


High-End Minis Forge New Application Areas

by Mary Rose Hanrahan, Associate Editor

Cockpit simulation application (Courtesy Perkin-Elmer).

To meet the demands of computationally intensive applications, computer manufacturers are now employing some basic architectural principles across the board—specialization, concurrency, parallelism, and new pipelining techniques.

The transition of the minicomputer into 32-bit architectures has fostered a debate over semantics, with many manufacturers now calling their high-end 32-bit machines superminis. As 32-bit supermicros encroach the minicomputers' domain, competency in such areas as specialization, parallel processing and pipelining is necessary to meet the applications-specific demands of today's supermini market.

The high-end mini or supermini arose from architectural innovations such as internal 32-bit architecture, 32-bit registers, fast floating point units and expanded I/O capabilities. The generalized minicomputer architecture consists of a CPU, memory, I/O controllers, I/O devices and a bidirectional communications path through which all system components are allowed to interact.

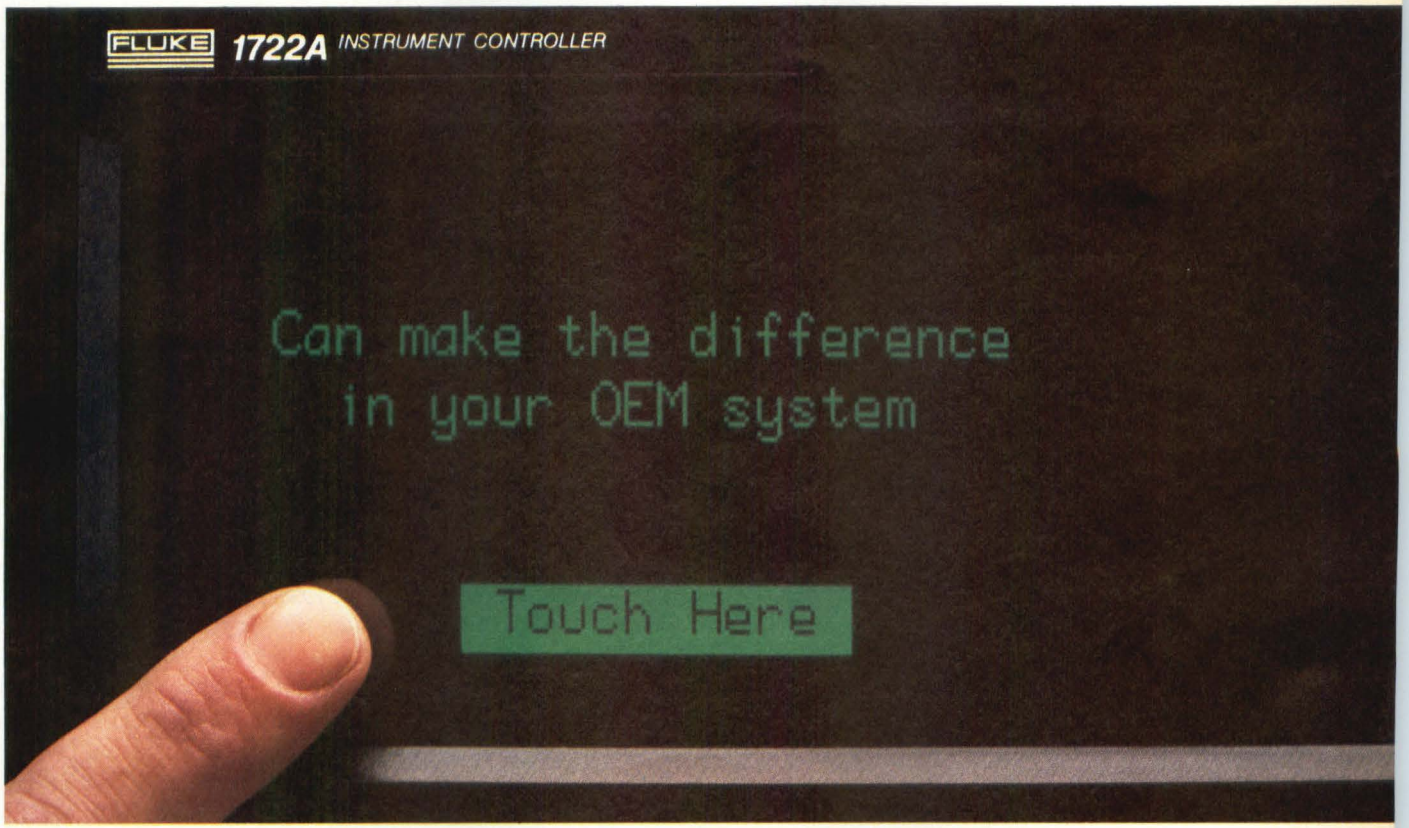
Some factors to consider when examining a minicomputer's suitability to a particular application are MIPS or execution speed, word size, instruction set and ability to handle interrupts. The advent of semiconductor memory and LSI circuitry has added to the minicomputer boom by allowing faster manipulation, greater accuracy, smaller size and reduced cost. Performance modification in high-end minicomputer design should strive to maintain hardware and software compatibility with earlier models while increasing performance.

Manufacturers such as Perkin-Elmer, Digital Equipment Corp., Data General, and Prime have recently augmented existing minicomputer product lines with high-end superminis targeted toward some non-traditional application areas. Applications for superminis have diversified from their initial office automation and database management niches, although these areas are still viable markets.

Non-Traditional Applications

Perkin-Elmer's (Oceanport, NJ) Model 3200MPS brought multiprocessing capabilities to their Series 3200 minicomputer family. The Model 3200MPS is a tightly coupled multiprocessor system; a system composed of more than one processor operating on a single global memory. This multiprocessor system's performance is achieved through a modular approach to multiprocessing. By adding Auxiliary Processing Units (APUs) to the central processor, the user can achieve an increase in system performance. In addition to its CPU, the model 3200MPS can

Fingertip control



The Fluke 1722A Instrument Controller

Of course, the biggest difference is 1722A touch-sensitivity. It will make your system truly user-friendly. And that sells systems!

But there's much more.

The 1722A Controller provides your customers with predictably controlled procedures. Even semi-skilled personnel can easily operate complex systems at the touch of a finger.

Designing the 1722A into your system is no problem. It's fully integrated and features a high-performance microcomputer, graphics display, 400K disk drive, complete software packages, plus RS-232-C and IEEE-488 I/O ports.

Most importantly, with the 1722A you get Fluke support. You're working with a multinational corporation and worldwide service organization.

Panel or rack mountable, the 1722A fits right into your OEM system.

The 1722A Instrument Controller is available, on an OEM basis, in as few as 20-piece quantities for under $6000. For further details, contact your local Fluke Sales Engineer or Representative. Or call us at **1-800-426-0361.**

Consider the 1722A in your next development. It will make your OEM system easier to build, to sell, to use, and to support. That's a big difference!

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206-356-5400, Tlx: 152662

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Fluke (Holland) B.V.
P.O. Box 5053, 5004 EB,
Tilburg, The Netherlands
(013) 673973, Tlx: 52237

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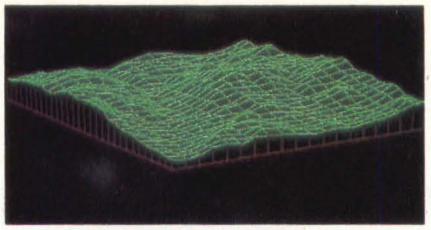
take on up to nine Auxiliary Processing Units. Each APU includes a global memory interface with its own cache, a Memory Address Translator (MAT), a floating point processor, writable control store and an instruction processor.

The 32-bit parallel architecture features 64-bit floating point and 32-bit fixed point arithmetic units and dual 32-bit data paths in the global memory bus. Each Model 3200MPS system supports one shared memory interface (SCACHE) to other systems. Through this SCACHE, a number of Model 3200MPS systems can be interfaced to an external shared memory system (**Figure 1**). The shared memory interface also allows two Model 3200MPS systems to be interconnected. Perkin-Elmer's proprietary OS/32 operating system supports these configurations by defining fixed partition global task common areas during system generation.

Applications have evolved as these types of systems become more prevalent and their price goes down. Energy exploration, inventory distribution, electronic banking and securities trading are new growth areas for 32-bit minicomputers. Among the more advanced applications are those in image processing and simulation.

Space Shuttle Simulation. At the Johnson Space Center in Houston, TX, NASA space shuttle crews are training on the most advanced flight simulators ever built. Contracted through the Singer Company, Link Division, the Space Shuttle Simulator System utilizes multiple Perkin-Elmer 32-bit minicomputers. Within the system, the shuttle procedure simulator employs five Perkin-Elmer 32-bit processors which interactively generate cockpit instrumentation responses. The Shuttle Mission Simulator uses fifteen 32-bit processors, which control all audio, visual and motion cues to the trainers and use communications links to Mission Control Center.

The Space Shuttle Simulators use eight banks of shared memory. Sharing system data in this way reduces the memory requirements for each processor and speeds real time data transfers. This particular system includes a writable control store for microcoding commonly used routines, a floating point processor for double precision arithmetic, the Fortran Enhancement Package for improving Fortran execution times and high speed disks and magnetic tapes, line printers and CRTs.



Seismic application (Courtesy Perkin-Elmer).

Remote Sensing Research. Today, remote sensing by satellite is helping many local, state, federal and private organizations to better manage their natural resources. Remote sensing is the acquisition of electro-magnetic spectral data from instruments on board satellites, aircraft or both. This data can then be processed by a computer system to derive information about the condition of the land, water surfaces and intervening atmosphere of the earth.

Data is transmitted from satellites as they pass within range of NASA receiving stations. Four spectral bands, or colors, are sent at once. One image of approximately 24 million pixels is transmitted every 25 seconds. From these receiving stations, the data is relayed to a processing center where it is reformatted and stored on tape. A minimal image processing system configuration developed by NASA includes the Perkin-Elmer Series 3200 computer system with 512 Kbytes of main memory. The system also includes an array processor, floating point hardware as well as a CRT with a high resolution color display.

Process Control. In power plant control and simulation, the system must handle a large number of calculations per timeframe, service numerous console requests, and distribute the results of processor calculations. The large volume of memory-resident application code required for power plant control and simulation was configured with four 32-bit Perkin-Elmer Model 3244 MEGAMINI processors interconnected to a 256 Kbyte Series 3200 shared memory system. Model 3244 processors are also interconnected via multidrop processor-to-processor interfaces. Additional Model 1610 16-bit processors are interconnected to the Model 3244 processors in a similar manner. By interfacing these eight processors, the simulator system is subdivided by functionality. The 3244s

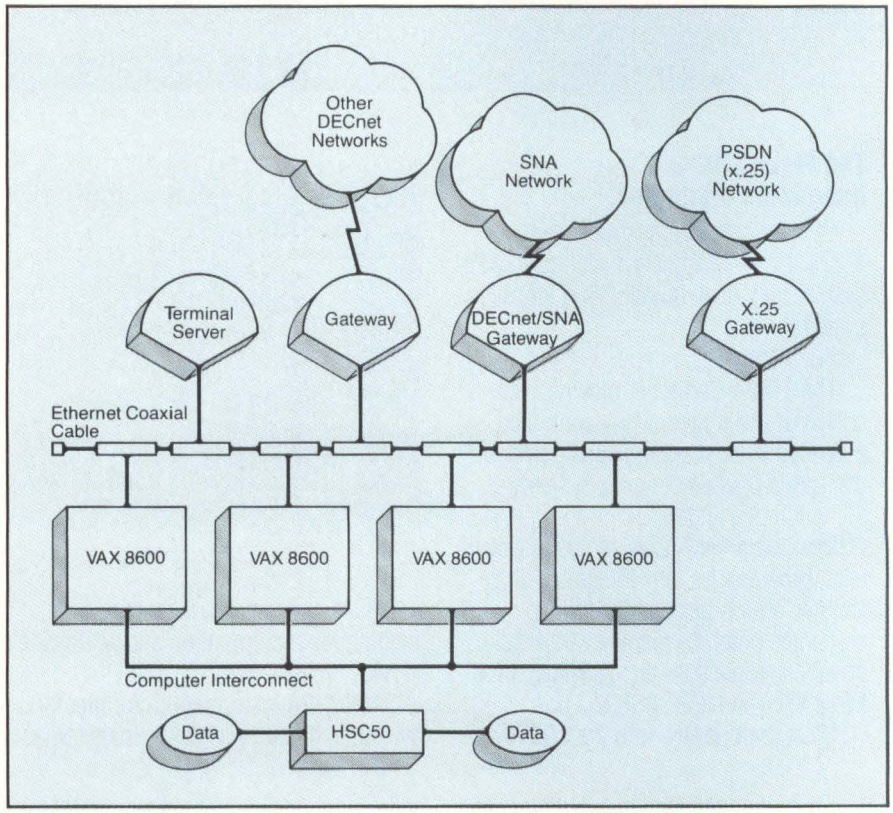


Figure 1: A VAXcluster allows VAX systems to be coupled into one single multiprocessing environment to facilitate balancing workloads, share data and provide availability.

STRONG STATEMENTS FROM PEOPLE WHO GIVE YOU . . .

STRAIGHTALK

No claims. No boasts. Just straight facts and commitments from Jeffrey Liu, president of Microscience, on our growing family of half-height Winchester disk drives.

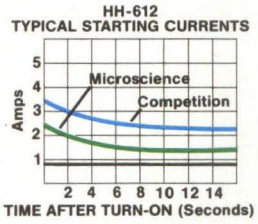
"By introducing the new HH-725 20 MB 5.25" and HH-312 10 MB 3.5" half-height Winchester disk drives to our product line, we now offer the proven quality and performance most OEMs need in volume today.

"Combined with our HH-612 10 MB 5.25" half-height disk drive, Microscience now provides a product family of superior quality and better performance than any other drives available.

"Time after time, we have proven that Microscience has the performance, quality, and price personal and portable computer manufacturers demand.

"The secret is the way we design and manufacture drives for you.

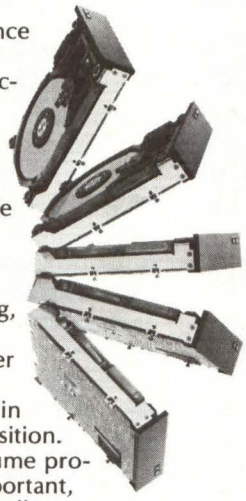
"Microscience disk drives have extremely low voltage requirements because small business and portable computers don't have the luxury of excess power or cooling capacity.



"We've used procedures and components that will be power misers, yet they still provide long-term performance and reliability.

"Our drives feature a thermally isolated stepper motor for precise head alignment and optimum seek performance. A proprietary linear actuator assembly was employed to ensure data reliability and provide greater drive durability.

"A buffered seek mode and highly accurate proprietary microprocessor-controlled closed-loop servo positioning system keeps the head precisely on track. This maintains data integrity through a wide range of operating conditions regardless of thermal expansion, system hysteresis, or long-term wear.



"Microscience drives are not limited to functioning horizontally. Because of the growing use of portable computers and increasingly compact packaging, we designed our Winchester drives so you can use them in almost any position.

"While volume production is important, what you're really concerned about is the quality of product you use in your system or application. We have made a major commitment to manufacturing and quality programs.

"Microscience test equipment and tooling have been carefully selected to meet our exacting standards.

"This ensures Microscience ships only zero defect half-height Winchester product that does not eat away at your profits . . . and your reputation.

"There's a lot more I could say about the Microscience half-height Winchester disk drive family. But what will convince you is using a Microscience drive in your application.

"For more straightalk regarding your half-height Winchester needs, call or write us today."

Jeffrey Z. Liu

President,
Microscience
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handle the modeling, real time I/O communication, training console and program development. The 16-bit processors are only used for data acquisition. The simulator system may generate between 1,000 and 5,000 analog/digital inputs/ outputs per 200 μsec frame. The A/D and D/A equipment used in the system is interfaced directly to the DMA bus or the multiplexor bus of the 16-bit processors. It uses I/O switches to extend the multiplexor buses permitting the A/D and D/A equipment to be located up to 100′ feet from the processors.

Software Development Environments

Adapting to the ever increasing application demands of multiuser environments Data General (Westboro, MA) has extended the range of 32-bit ECLIPSE MV/Family Systems with the ECLIPSE MV/4000 SC (small cluster). With the Eclipse MV/4000 SC, Data General intends to lower the entry barrier for applications requiring 32-bit performance in the business automation, commercial and technical environments. With an emphasis on performance, compact packaging and cost per workstation (under $8,000), the MV/4000 complements the existing MV/8000 II and MV/10000 family of 32-bit superminis.

Operating with Data General's Advanced Operating System/Virtual Storage (AOS/ VS), the MV/4000 supports all existing AOS/VS software. The MV/4000 optionally runs the DG/UX native UNIX operating system and in this configuration can support up to eight users. It is compatible with UNIX system V and Berkeley 4.1. The DG/UX implementation is a demand paged, virtual memory UNIX operating system that is compatible with the 4.1 Berkeley Software Distribution (BSD). Users may select the BSD "C-shell" user interface or the AT&T Bourne Shell.

DG is claiming a complete UNIX implementation allowing software portability through a standard UNIX operating system among all DG 32-bit products. It is targeted toward OEMs and CAE/CAD end-users who require transportability, access to a large group of programmers and the software tools available on the UNIX operating system. Using DG/UX gives users the ability to transport software developed on one machine running UNIX to another vendor's system, and provide access to the C programming language.

To encourage software development, DG now provides users a choice of UNIX environments with DG/UX and MV/UX, a hosted UNIX environment. MV/UX is integrated with Data General's AOS/VS software and runs concurrently with AOS/VS, allowing users to take advantage of a wide range of languages including C, Fortran 77, programming aids, productivity tools as well as the Ada Development environment. The native UNIX operating system also supports UNIX-to-UNIX protocol programs so that files can be transferred between DG/UX, MV/UX and any computers running the UNIX operating system.

Electronic Design Management Systems

For digital electronic design and production, Prime Computer (Natick, MA) offers the Electronic Design Management System (EDMS) which integrates database management, interfaces to applications software and spans logical design to physical implementation while running on the 50 Series of 32-bit superminis.

As in comparable 32-bit systems, Prime's 50 Series runs on a proprietary operating system, PRIMOS, which ensures total software portability across all PRIME systems. The 9950 is Prime's high-performance machine targeted toward computational, commercial, office automation or CAD/CAM/CAE applications in standalone or distributed environments. The 9950 includes a 32-bit CPU featuring ECL circuitry and pipelined architecture, up to 16 Mbytes of error-correcting MOS memory, burst-mode I/O, hardware instruction assists, 16 Kbytes cache memory, any standard peripheral subsystem, asynchronous line controllers and PRIMENET Networking Software Nodes.

For the design environment, the 50 Series runs EDMS which combines a component library, a design database, editing, writing and electronic design utilities. Included in EDMS is the Library Management System which is used to create component libraries. EDMS also incorporates the Prime wire wrapping software module. With this package, engineers can easily create wire wrapping boards using English commands.

Also available on the 50 Series superminis is Prime's own hierarchical logic simulation system, THEMIS. THEMIS provides capabilities to model at the switch, gate, functional and compiled language levels, and to run simulations much faster than with some other competitive systems. EDMS also offers an integrated interface to THEMIS. Therefore, an input file containing a list of parts used in the design and circuit interconnections can be extracted from EDMS and input to THEMIS for circuit simulation.

EDMS also supports interfaces to a variety of third-party electronic design software packages. These include MERLYN for gate array routing, MP2D for standard cell layout, TEGAS-5 for logic simulation as well as PRANCE and SCICARDS for printed circuit board design. The 50 Series running EDMS has also been designed to accommodate

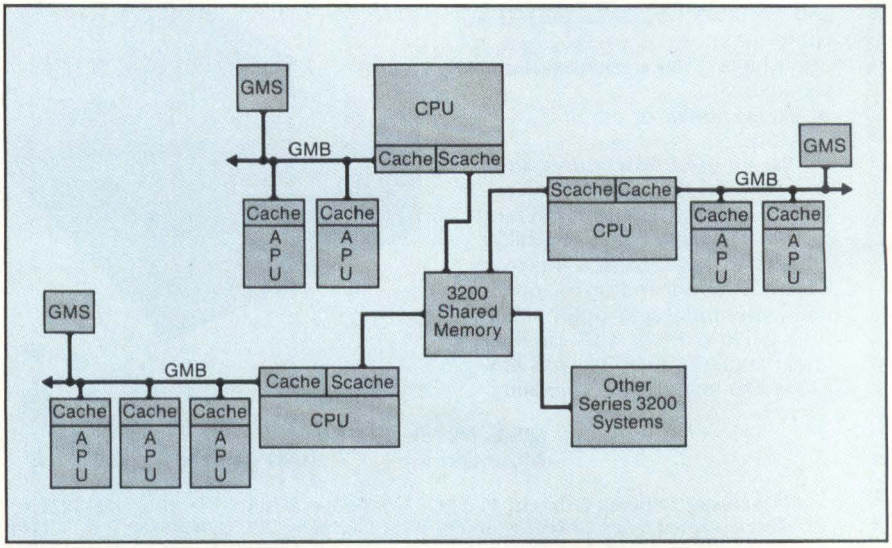
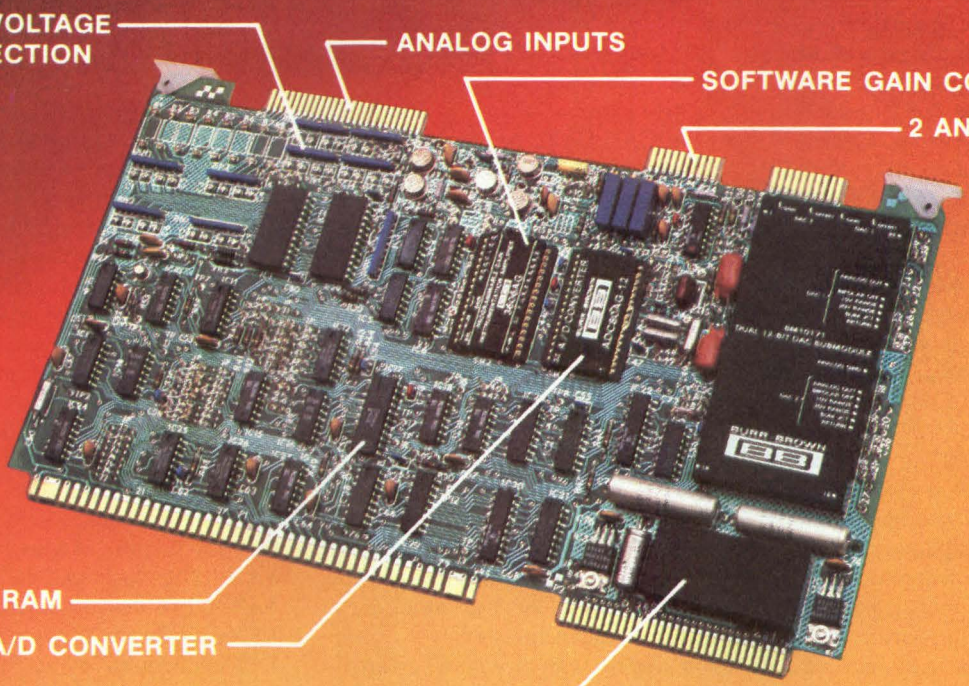


Figure 2: The Model 3200MPS and shared memory system from Perkin-Elmer.

How To Handle 127 Channels of 10mV to 10V Analog Inputs With Minimum Space/Cost!



If your analog input signals range from 10mV to 10V; if you have to input up to 127 channels; if you must isolate some of those channels—the MP8418 family of Multibus™-compatible analog I/O peripherals offers a cost effective solution!

MP8418 is the basic I/O board: it's 12-bit accurate and provides resistor or eleven software programmable gains ranging from 1 to 1024 V/V. When your host converts a channel by reading a memory location, the MP8418's onboard RAM sets the amplifier gain for that channel—transparent to host and operator! Analog inputs have overvoltage protection to 26VDC and up to fifteen 4-20mA inputs can be accepted. The input section has MUX, amplifier, S/H and 12-bit ADC. Optional analog output adds two DACs and control logic. DC/DC converters are included in all models.

MP8418-EXP: Used with the basic MP8418; differential input capacity is increased from 15 to 63 channels; single-ended input capacity from 31 to 127 channels.

MP8418-ISOE: Use up to three with MP8418 to gain an additional 48 *isolated* analog channels. The basic MP8418's 15 channels are non-isolated CMOS multiplexed inputs.

Use MP8418 expander boards to achieve higher analog input channel capacity with fewer I/O boards and at significantly lower total cost.

For specifications on these three I/O peripherals call or write:

Data Acquisition and Control Systems Division
3631 E. 44th St., Tucson, AZ 85713
(602) 747-0711

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interfaces to other application software packages as they become available.

The Clustering Concept For Large Applications

Today's information processing manager faces two major problems—an ever increasing applications and systems development backlog and the fact that many systems will be obsolete by the time they are implemented. In large organizations with a complex mix of computing, information management and data communications needs at various levels, applications development backlog can be years. In contrast, new hardware and software advances appear in the marketplace overnight. On this premise, Digital Equipment Corp. (Maynard, MA) is promoting the concept of "clustering" its VAX line to expand existing applications and to create new ones all within the context of a software architecture designed for long-term stability.

More than 30,000 of DEC's 32-bit virtual memory computers are working in diverse commercial and technical applications worldwide. The advantages of VAX power is well-known. VMS is the operating environment that adapts VAX systems for real time, timesharing, batch and interactive data processing. The 32-bit instruction set, common to all VAX systems, contains 300 instructions and the 32-bit virtual memory addressing simplifies application design. The 32-bit word length and virtual memory management provide more than four billion bytes of address space. Half of this is for user programs, half is used for the system. In effect, every VAX user has over two billion bytes of address space available for application design, development and execution.

Ideal applications for VAXcluster systems include research, transaction processing, CAD/CAM, process control and communications. The VAXcluster can be defined as a multiprocessing system of several VAX computers. This configuration of up to 61 VAX 11/750, VAX-11/780 series and VAX 8600 processors, in certain combinations, and intelligent storage subsystems function as a single, large, highly powerful system. Advantages of such a system include redundancy (for data availability should a fault occur) and global data sharing (for data updates and access). With several processors sharing the load, speed is gained, data is protected and disk storage optimized.

Perkin-Elmer's 3200 Series Superminicomputer.

System availability is critical in the large applications such as geophysical research, finite element analysis, simulation systems with or without an artificial intelligence base and others that require high speed processing of enormous amounts of complex data. The VAX 8600, DEC's largest single-processor VAX, supports several hundred users. An advanced internal processor structure previously found only in mainframe class systems, overlaps processing of up to four instructions simultaneously. The resulting system holds up to 4.2 times the performance of the VAX-11/780. Through the use of a terminal server in the VAXcluster environment, a user can continue working on a second processor if one processor becomes unavailable. With a single keystroke, work can be continued on a second VAX that offers the same service, so that time is not lost. New methods of error logging, analysis and recovery, formerly used in much larger machines, have been built into the VAX 8600. This is especially important when several systems support an organization, as in a VAXcluster configuration.

At John Fluke Manufacturing, a manufacturer of electronic test and measurement devices, engineers at CAD workstations create designs which are then converted into patterns for printed circuit boards. The VAX 8600 was used to shorten, by a factor of four, the conversion of designs to actual PC layout.

Prime's 9950 Supermini.

The Accelerator Ring at the Fermi National Accelerator Laboratory (Fermilab) in Illinois, examines and records the characteristics of subatomic particles with short lifetimes. VAX-11/780s support the 2400 scientists conducting experiments in particle physics.

The VAXcluster at Strategic Information (Burlington, MA) is composed of a VAX-11/785, four VAX-11/780s, and two VAX-11/750s, with additional VAX-11/750s, VAX-11/730s and MicroVAXes within a DECnet network. Strategic Information provides timesharing services to users in areas such as financial planning software, trust accounting and investment analysis software, portfolio evaluation and electronic publishing.

The VAX 8600 system will also be used in computer integrated manufacturing (CIM) and factory automation applications where high-end general purpose superminis are required to manage, analyze and consolidate data from factory floor devices.

The strong foothold minicomputers have found in the industry will increase as users find it possible to port many man years of software effort to higher performance machines. The leaders in the marketplace will be those that offer the broadest spectrum of computers across wide price ranges that remain software compatible with one another. DD

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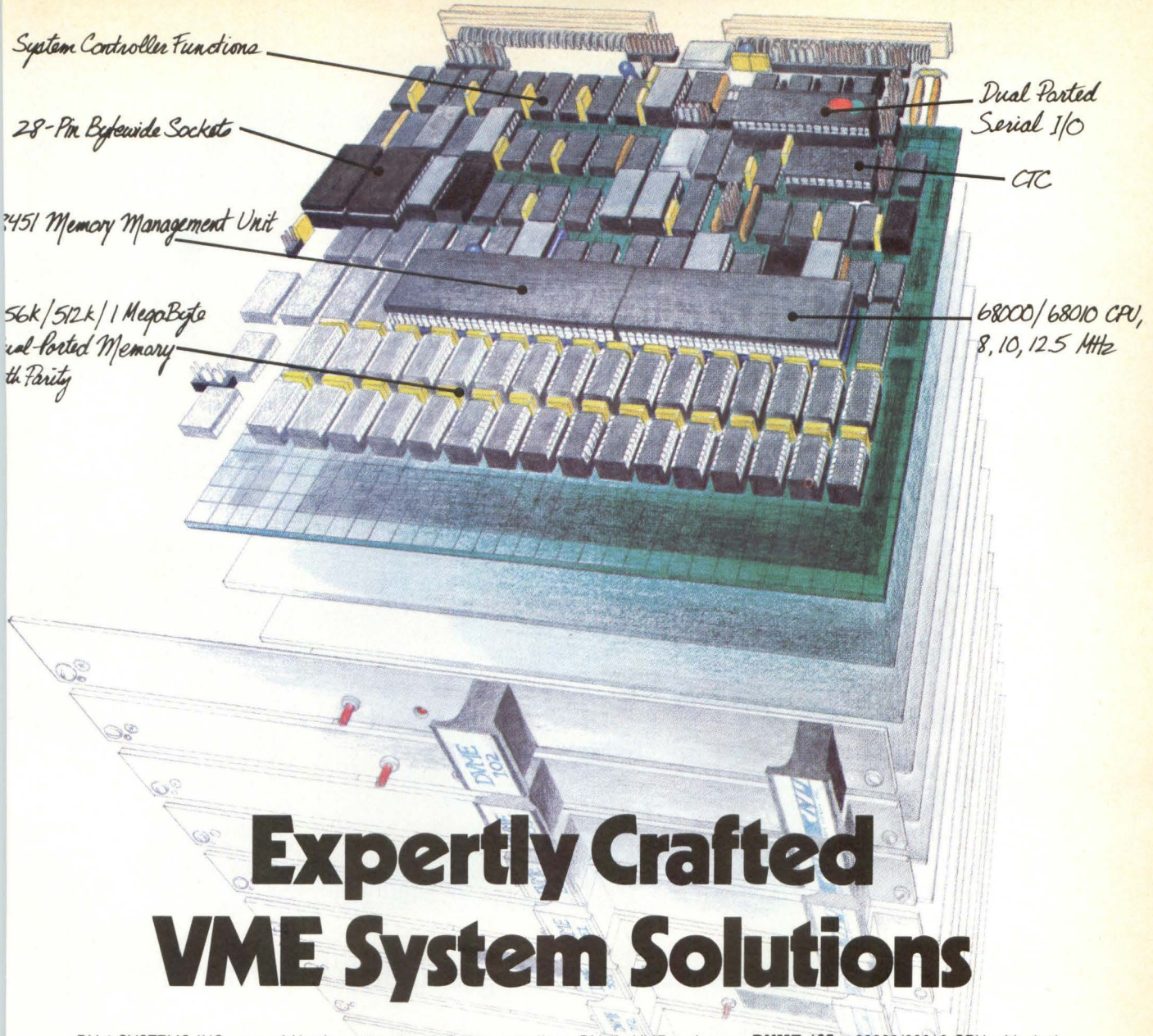


Expertly Crafted VME System Solutions

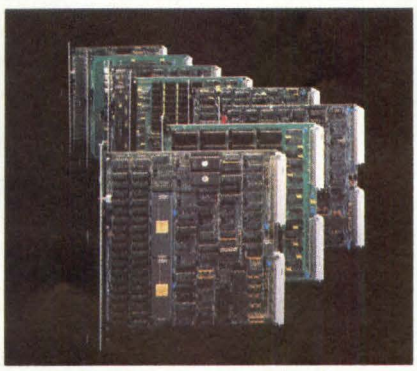
DY-4 SYSTEMS INC., one of North America's most successful producers of board level products, now offers a fine array of expertly crafted VME modules and UNIX based development systems – perfect for all your demanding 16/32 bit applications. Stringent manufacturing and quality control ensure a reliable product with maximum power and integrity.

DY-4 realizes the full potential of the powerful VMEbus architecture by using an extended depth Eurocard format of 233mm × 220mm. By increasing functionality and allowing processor, memory and I/O combinations, and bus controller functions on a single board, DY-4's format offers higher performance than competitors' equivalent configurations.

DY-4's commitment to R&D is reflected in its continuing new VME product development, including intelligent communications controllers, SMD/ESMD controllers and 9-track tape controllers. DY-4's VME series currently includes:

DSM-*6816* – a UNIX based development system.

DVME-*102* – 68000/68010 CPU with MMU, dual-ported serial I/O and 256K/512K/1Mbyte DRAM.



DVME-*105* – 68000/68010 CPU with dual-ported serial I/O and 14 bytewide sockets.

DVME-*201* – with 8 serial RS-232C/422 channels and 2 parallel I/O ports.

DVME-*351* – A 512K Byte memory board with 10Megaword per second raster video port. Supports 16/32 bit VMEbus read/writes.

DVME-*503* – Universal memory board with 32 28-pin bytewide sockets. Supports 16/32 bit VMEbus read/writes.

DVME-*712* – Intelligent Z80A peripheral controller with RS-232C/422 I/O, 64K DRAM with parity, floppy disk controller, SASI interface and DMA.

DVME-*778* – Colour graphics controller supporting 640 × 480 × 4 (1024 × 768 × 2), NEC 7220 GDC, look up table, 3 4-bit D/A converters, mouse input and parallel printer port.

DVME-*909* – A 19-inch rack-mountable system chassis with 9 slot VME card cage, power supply and forced air cooling.

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'STEMS INC.
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DY-4 SYSTEMS INC.
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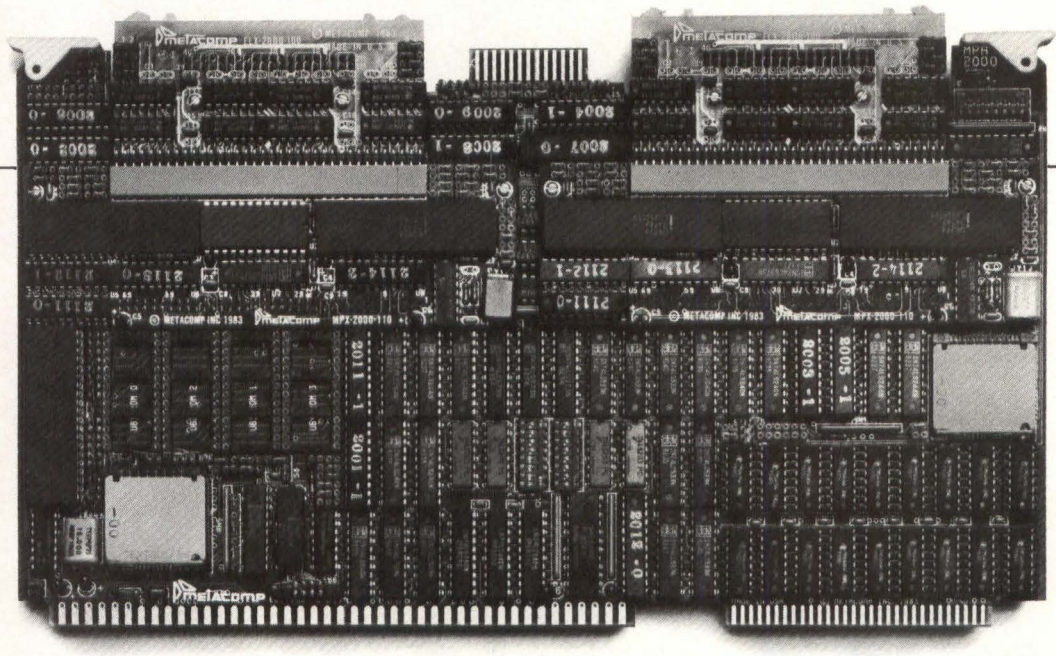
Chairman of the boards



The first true Multibus single-board computer

The MPA-2000 is highly qualified for the top slot. It's the first to offer the iAPX-186 CPU. The first to offer 512KB of dynamic RAM. And, the first with architecture that allows plug-in modules with multiple DMA channel support.

That makes it the first CPU and I/O processor that combines: data processing, data communications, local area networking, disk I/O and similar peripheral functions. Standard data communications packages available include; CCITT-1980 X.25, IBM-3270 SNA (LU 1, 2 & 3), SDLC, HDLC (LAPB) and IBM-3270 BISYNC. Operating system portations include; PC-DOS, iRMX-86, VRTX/86 and MTOS-86. In all, it has the performance and capability to replace 2, 3 or 4 board members in most applications.

With that outstanding resume, it's easy to see how the MPA-2000 became the unchallenged Chairman of the Boards.

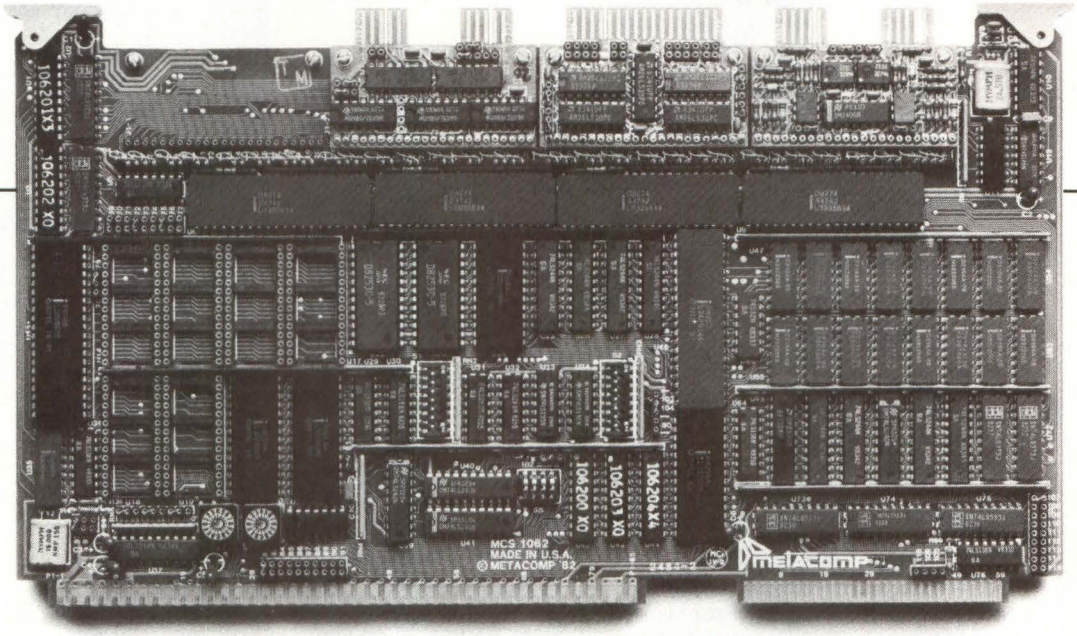
For complete specifications and ordering information, call or write METACOMP, Inc., 9466 Black Mountain Road, San Diego, California 92126, (619) 578-9840. TWX 910-335-1736 METACOMP SDG.

Ask for the resume of the Chairman of the Boards.

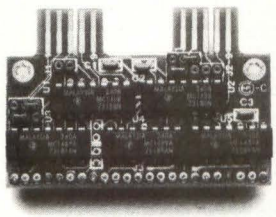
METACOMP™

THE MULTIBUS BREAKTHROUGH PEOPLE

California Serfboard



Get eight channels of intelligent slave serial I/O with this new wave Multibus controller



The versatile California Serfboard, MCS-1062, is the first serial I/O controller with eight intelligent slave channels. Plus all the features highlighted below. That's double the typical capacity in a single cardslot. And the on-board CPU means performance and programmable flexibility that leaves the competition treading water.

Product Highlights:

- ☐ Eight individual channels, programmable for ASYNC, SYNC, or BITSYNC.
- ☐ Programmable timers for ASYNC data rates to 76.8K Baud.
- ☐ Wide range of modular interface adapters available, each field interchangeable. RS-232, RS-422/RS-423 Optical Current Loop, MIL 188-114.
- ☐ On-board Intel 8088 CPU. 96K bytes EPROM (using 27128's), 128K bytes RAM.
- ☐ Simple "handshake" architecture for user software interface.
- ☐ Dual Port RAM. Supports 8 or 16 bit memory accesses, 24 bit Multibus addressing.
- ☐ Standard Multibus architecture. One unit load, single card slot, vectored or nonvectored Bus Interrupts.
- ☐ Terminal I/O firmware available.

For complete specifications and ordering information, call or write: METACOMP, Inc., 9466 Black Mountain Road, San Diego, California 92126, (619) 578-9840, TWX 910-335-1736 METACOMP SDG. Ask for the hot sheet on the MCS-1062. The California Serfboard.

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Operating Systems For Micros — Too Much For Too Little?

by Gregory MacNicol, West Coast Technical Editor

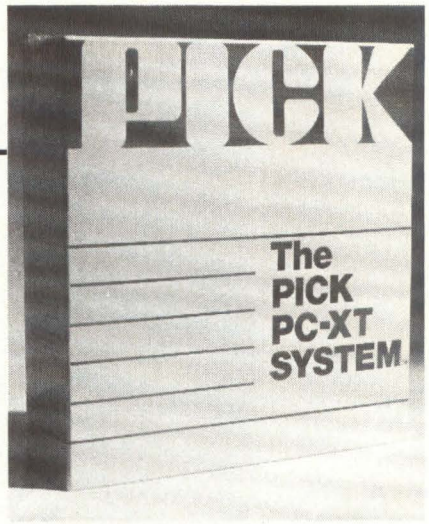

PHOTO COURTESY PICK SYSTEMS

Intended to be invisible from users and software developers, the omnipresent operating system is critically important for the operation of computer systems. The primary role of an operating system is to interface with and provide efficient management of the hardware resources of a microcomputer such as disks, I/O and memory. The basic operating system is responsible for fluent control by the user avoiding device dependent control for the application program.

With these primary goals in mind, additional features such as multitasking, multiuser, fault tolerance, windowing, and data control become desirable. In addition, today's operating systems require application programs to interact with graphics, light pens, touch screens, mice, various communications protocols, multiple file system formats, multiple operating systems, graphics standards and multiple application programs. The problem quickly becomes an issue of compromise. With finite memory and limited speed, all of these features cannot fit on one system. As some of the newer operating systems become more complex, they tend to lose flexibility and require more memory space. Performance speed also suffers. Software maintenance requirements increase, and the operator learning curve gets longer. As a result, there are now many operating systems in the marketplace, each targeted at specific problems. Worse yet, they remain so different from each other that applications written for one do not work with another. Ultimately, one realizes there is no perfect operating system.

Many new operating systems have been introduced in the last six months, and many more will be announced in 1985. Whereas many of the newer operating systems are extensions to existing ones, the activity in the operating system business is high and reflects the need for specific applications for different priorities.

The first operating systems were humans. One of the chores involved replacing vacuum tubes that burned out. Although the requirements of today don't preclude the replacing of burned out VLSI devices, the concept of operating systems has changed dramatically. The first computer systems required all programs to be written in machine code. These operating systems, called job-to-job monitors, controlled I/O and had the ability to manage several user programs stored in memory. Time sharing systems pushed the concept of operating systems towards greater sophistication, allowing real time applications processing with responsive interactivity.

The First Operating System

Microcomputer operating systems of today descended from early mainframe computers. The IBM 360 was the first commercially acceptable operating system. It could support multiprogramming, batch time sharing and real time applications. Using job control language (JCL), the user gained access to the system's resources through the OS/360 which acted like a shell surrounding the hardware.

The concept of what the shell should do created two divergent viewpoints with respect to microcomputer systems. Some computer analysts feel that an operating system should provide as many functions and services as possible. Control of I/O, display and hardware control should be handled completely to prevent application software from becoming too complex, inefficient in hardware management, and too large. On the other hand, some analysts feel that the operating system should be minimal, providing greater portability from one system to the next. The services provided in the application program should run on any standard operating system and be able to maximize the capabilities of the hardware without being a burden on the system.

Current developments in computer technology are creating an increasing burden to future operating systems. Networking, database control, distributed processing, security provisions, user happiness and on-line transactional processing are some of the major demands that are turning an operating system into more than a host to an application program. As each trend in technology changes, the operating system is expected to perform with these new and special goals in mind. Fast graphics applications, for example, may require bit mapped displays to be swapped to and from the display driver. Business applications require operators, programmers and users to work directly with a central system which is constantly updating its database. Demands such as these require the operating system to work intimately with the hardware to provide maximum speed and efficiency. *(continued on p. 85)*

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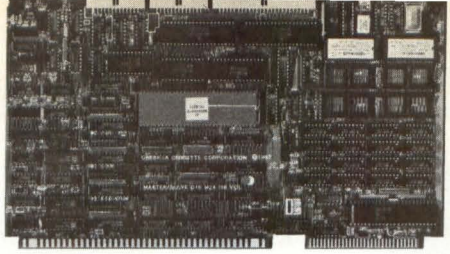

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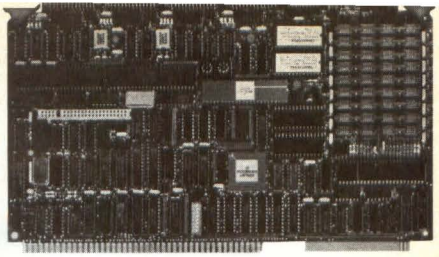

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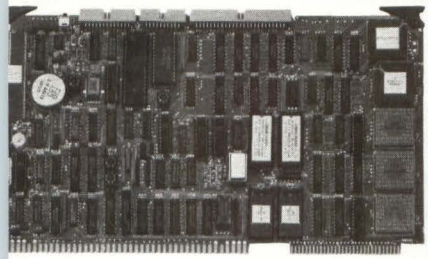

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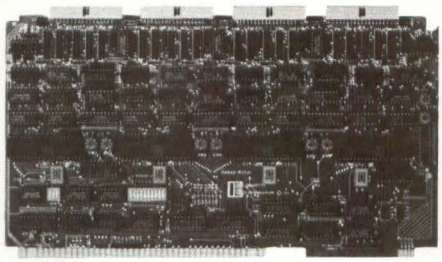

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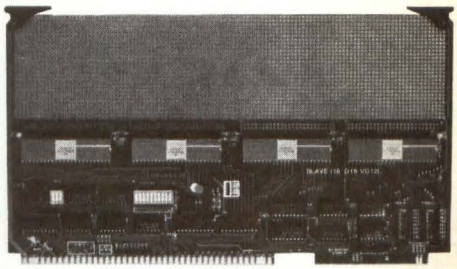

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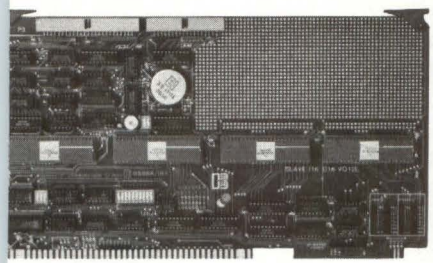

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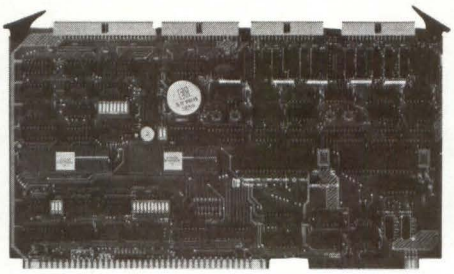

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(continued from p. 78)

The Basic Operating System

An operating system should have three basic capabilities: hardware resource management, run time services and command language processing in real time. The operating system must efficiently allocate main memory and disk memory and allow operations to be invisible of hardware used. Memory management may include bank switching, overlays, static and dynamic relocations of main memory, chaining and memory protection. Peripheral management is very important. If interrupt handling, device drivers, DMA support and spooling are not handled well, the peripherals can bring a system to its knees. File management, too, is critical where control of sequential/random/contiguous files and indexed sequential files is essential. Run time services include the primary functions such as processor allocation management comprising intertask communication, task synchronization and task start/stop/delete functions. Operations such as these should not be a burden to the user. The operating system should straddle the spectrum of human interfacing from advanced programmers to unsophisticated application operators.

Beyond these basic capabilities, extra features that add greater functionality are becoming commonplace. Although many application programs add some of these features to a program's menu, it is sometimes preferred to have these features present at all times in the host operating system. Some of these optional features include graphics, data management, screen format management, communications protocols, networking capability, compilers, diagnostic and utility programs. The real difference between one operating system and another is the extent to which these features are implemented. Some operating systems infer protocols from prior operations. One very useful utility is the ability to read disks in other formats. All too often though, the more advanced the features, the more difficult it is to implement them.

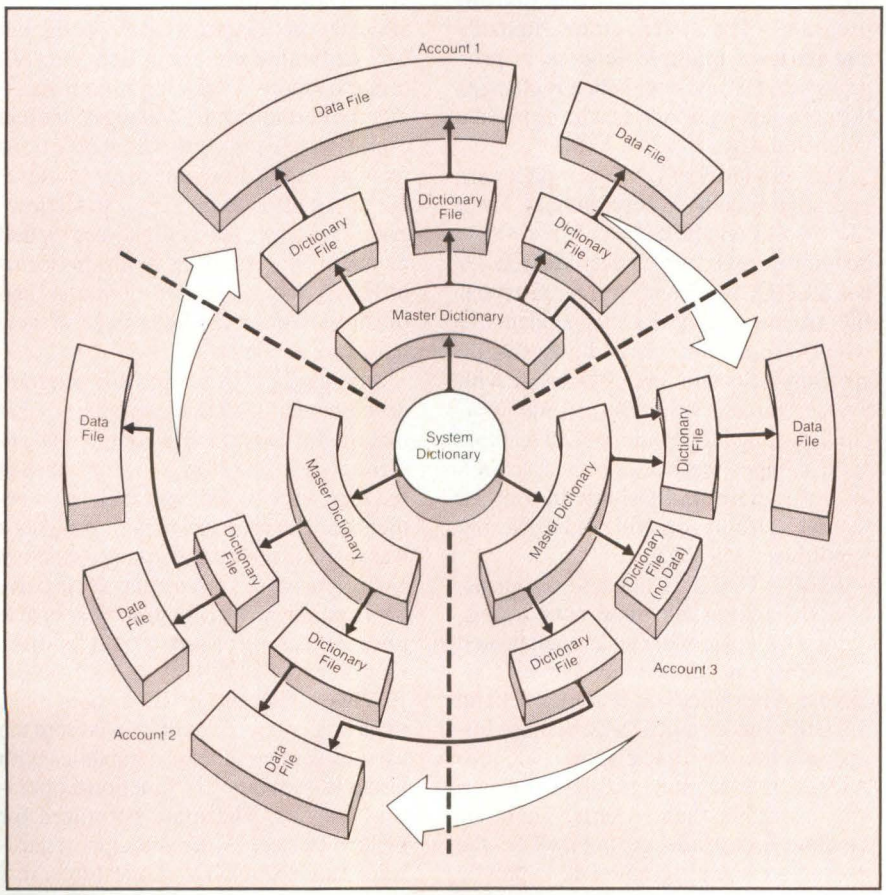

Figure 1: In the PICK operating system everything revolves around the system dictionary and both data files and dictionary files can be shared.

For that reason, on-line help is becoming essential for optimization of a user's time. This quality is often overlooked while circumventing the most important feature of an operating system: user effectiveness.

One of the more popular functions to add to an operating system is local area networking (LAN). While all the primary functions are active, the operating system that wants to latch onto another network with remote resources has a special problem. It must communicate with other operating systems or the network is useless. The most popular method to avoid this problem is implementing software as extensions to all the network's operating system, creating a new environment. The interface can then take the place of translator software for each different computer. Until the International Standards Organization (ISO) fully agrees upon its seven layer model and protocol software is available, the software can temporarily serve as an adequate interface. Several companies have realized this particular bottleneck and are providing operating system extensions. PC-NOS from Applied Intelligence (Mountain View, CA) and Orchid Technology (Fremont, CA) are two such examples for providing network operating system extensions. Telenova (Los Gatos, CA) provides another approach in computer communication. Combining voice and data transmission on a proprietary time division multiplexing network, Telenova has departed from the more traditional approach of token passing and collision detection.

An emerging trend in the migration from mainframes to micros is concurrency – the ability to perform several tasks simultaneously. Programmers, who have taken advantage of multitasking on mainframes, have brought the concept to micros with the goal of increasing productivity and efficiency. The appreciation of concurrency is not limited to programmers. Today, unsophisticated users prefer to execute programs simultaneously rather than sequentially. Concurrency allows the interruption of one job and the beginning of another. Moreover, it is possible to interrupt a program with a single keystroke, start another program and continue the original program where it left off. This is important to office productivity. A user can work on a word processor, run a graphics application program and receive electronic mail at the

same time. Newer 16-bit operating systems, combined with inexpensive RAM-based storage, can benefit from efficient use of new hardware schemes offering greater speed. With a concurrent operating system running three or four programs at once, the system's resources may be more effectively used.

A Standard For Operating Systems

With seemingly as many operating systems as there are languages and little way for one system to fully communicate with another, the situation appears grim. The IEEE's Microprocessor Operating System Interface (MOSI) Task Group 855 has taken the problem seriously and is creating a standard called the MOSI interface. Using the MOSI interface, a programmer can develop software which, in turn, communicates with the specific operating system. The process is similar to the proposed ISO virtual terminal protocol. Naturally, the standards task force is bringing up fundamental issues about the basic functions of an operating system. Memory management, time management (specifically what software process is to be delayed), synchronization and communication and exception handling, such as parity errors, are some of the hot issues. In addition, how I/O will be handled and what functions are to be expected in the MOSI interface is still an issue. A major topic is how the standard is to deal with file systems. Every operating system handles files in a unique manner, each offering a different set of compromises.

The popularity of operating systems, like languages, is based on personal preference and familiarity. Whether or not a standard will be adopted remains to be determined. As a result, the committee has opted for four classes of standardization: A, B, C and D. The difference lies in the extent to which it is employed. As much as the industry needs some kind of standardization, time will tell if the MOSI standard will take hold.

UNIX

AT&T developed UNIX after their withdrawal from a joint project with MIT, GE and Honeywell. The intent of the project was to create a general purpose operating system for diverse users. After the project broke off, AT&T developed the system for programming research and development with a powerful control language that could operate independent of specific hardware. The system was then written in the high level C language, which increased portability and readability. Although it was designed for a PDP-11, it also was available on a wide variety of computers. Now it is available in many versions with differing levels of complexity.

Because it was intended to be portable, UNIX leaves as much as possible to the application program. Its greatest strength lies in its power of program development.

Because it was intended to be portable, UNIX leaves as much as possible to the application program. Its greatest strength lies in its power of program development. It comes with text editors, compilers, debugging tools, utilities and public domain programs. The system stores, updates and retrieves multiple versions of programs and text and automatically changes the pertinent data such as who did what, when and why.

The popularity of UNIX is influencing operating systems in development. Even Microsoft's (Bellvue, WA) MS-DOS is becoming more like UNIX. Version 2.0 has a UNIX-like multilevel hierarchical file structure and device independent I/O with I/O redirection. In addition, the file structure associates each I/O device with a device directory file. Developments include porting UNIX utilities and features such as pipes, networking, and version 4.0 will handle multitasking. In contrast to UNIX, Microsoft will not be offering a multiuser MS-DOS.

AT&T's UNIX is not without drawbacks. Lacking adequate networking, memory management and sophisticated file management, the University of California at Berkeley has Berkeley 4.1 and 4.2 BSD versions of UNIX that are improvements over the original version. AT&T's UNIX manages data through streams rather than records. This may facilitate independence, but it forces the user to write a program code to handle data management. In addition, because UNIX uses only random file access, the user is required to write a data management code for control. The shell concept, which is popular and provides a powerful command interpreter, requires rewriting the shell for different applications.

UNIX was not designed for multiprocessing, where each processor shares a copy of UNIX and programs run concurrently with each other. Sequent (Portland, OR) offers such a system. Using UNIX 4.2BSD as the operating system, the Balance 8000, the multiprocessor computer, offers true dynamic load balancing where the system automatically allocates processors in the most efficient way to handle changing demands. In order to modify UNIX for multiprocessing, the kernal required changes: mutual exclusion preventing different processes from accessing the same data structure; the distribution of interrupts to all processors; process scheduling; and virtual memory. Modifications of various forms of UNIX such as this are common, and these versions take advantage of new hardware schemes.

Although UNIX is strong on program development, it lacks many facilities that make it difficult to use in commercial environments. The slow learning curve of novices, lack of efficient data management and the recovery handling makes it less than ideal for day-to-day production environments. Use in execution intensive environments, such as graphics, is also poor and is a reason why it is often modified.

While UNIX and UNIX versions make their marks, there are offerings from the various semiconductor companies with lesser known but very functional operating systems. These are optimized for their microprocessors and support hardware and have UNIX-like features, real time operating systems and development systems geared to supporting the micro-

processor architecture. Xenix from Microsoft may easily be the most widely sold UNIX look-alike. It is also sold through Intel, National and even IBM for one of its scientific workstations.

The Future

One of the problems of designing future microcomputer operating systems lies in the desire to make all features for all people. The microprocessor performs functions such as multitasking, multiuser, LAN, data base control, memory management, graphics and I/O control. Because these functions can be a burden to the microprocessor, the classic problem of compromise must determine what has the greatest priority. Nevertheless, operating systems planned for the future show great promise and indicate concern for the end user.

One of the features to look forward to is the support of databases where the ability to examine and manipulate data from different viewpoints is possible. The current method of file access through sequential and random reading of records is inadequate. The indexed sequential access method is also insufficient for advanced database applications. The importance of commonly shared databases is often overlooked but the advantage of databases is the nonredundancy of data. In order to make full use of a common database, there must be a common database dictionary with usable primatives from a high level language.

Communication is another major function. An operating system that has adequate communications ability can properly use concurrency where the communication program can monitor the communication link and report events that might require operator intervention. Communication is essential with LANs. Now that microcomputers have allowed multiuser systems to become more affordable, it seems ironic that few of them can communicate with each other. The question of whether to require the operating system or the application program to control the protocol is still an issue, but regardless, compatibility with old and newer systems is essential.

As the demand for better graphics increases, so does the demand for an operating system to support it. Graphics capabilities are quickly becoming more sophisticated, complex and commonplace. The graphics interface should provide for control of multiple devices at the same time, use of normalized coordinates as well as raster coordinates, the ability to draw primitives and characters and the ability to interface with graphics databases. Standardization is already helping form the support of graphics standards such as the graphics kernal system and the virtual device interface. These allow hardware to be controlled in predictable and controllable manners such as the Shugart Associates Standard Interface (SASI) to control disk drive systems. Where a standard impedes optimal operation of a hardware device, there should also be a routine to address the hardware more directly. In addition, operating systems of the future should maximize user productivity through the use of graphics, specifically icons, mice, menus and windows.

The operating system of the future will not only have to make the best use of hardware but also allow current databases and programs to be read and executed. Both software vendors and users are looking forward to portability which allows programs to be executed on various machines without modification. The operating system that is limited to reading only fixed size files is no longer acceptable.

Whatever operating system is going to be used in the future is not an issue of better or worse. As operating systems become more sophisticated, targeted functionality of intended usage will become a more important factor.

Conclusion

New microcomputer operating systems are being designed and developed for the next generation of hardware and microprocessors. These new systems and concepts attempt to give users and advanced programmers the necessary tools for developing and executing programs of the future. Although advanced architectures are featuring greater power, future operating systems will have to straddle the fine balance between optimizing the power of the hardware and ultimately making the computer easier to use. DD

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The Rise Of Korean Semiconductor Imports

Fueled by governmental policies to encourage private spending for R&D as well as increase national R & D expenditures, Korean IC manufacturers are on the rise. Four of the largest Korean electronics manufacturers are working toward displacing a portion of the Japanese share of the semiconductor market.

South Korea's four largest electronics firms, Gold Star Semiconductor, Samsung Electronics, Hyundai and Daewoo, have a combined projected investment over the next five years that totals over $1 billion, according to Integrated Circuit Engineering Corp. (Scottsdale, AZ), a high tech consulting company. Gold Star had an expected investment in 1983/84 of $30 million and up to $160 million over the next five years. Samsung planned to invest $150 million in 1983/84, possibly totaling $500 million by 1987. Hyundai anticipated an investment of approximately $150 million to $200 million during 1983/84 and as much as $500 million over the next five years. Daewoo will have invested $50 million to $100 million in 1983/84 and possibly $200 million over the next five years.

The rise of Korean semiconductor imports (in US dollars/thousands).

	1982	1983	Percent Growth
Integrated Circuits			
Production	$490,047	$661,379	35.0
Export	497,845	658,049	32.2
Indirect (export)	8,213	17,204	109.5
Domestic	6,847	11,050	61.4
Other Semiconductors			
Production	$158,080	$188,783	19.4
Export	125,608	154,384	22.9
Indirect (export)	17,637	29,424	66.8
Domestic	18,685	13,358	– 28.5
Total Semiconductors			
Product	$648,127	$850,162	31.2
Export	623,453	812,433	30.3
Indirect (export)	25,850	46,628	80.4
Domestic	25,532	24,408	– 4.4

Source: Electronic Industries Association of Korea.

The aforementioned manufacturers have established US operations, yet continue to manufacture products in Korea. Each of the four companies is taking slightly different approaches, however. Hyundai has plans to invest $50 million in the Santa Clara-based Modern Electro Systems Inc. over the next five years. They also plan to develop 16K RAMs and 128K ROMs, later offering complete computer systems suitable for business applications. It's wholly owned US subsidiary, Hyundai Electronics America, headquarters marketing, engineering and manufacturing operations in the US. Hyundai Electronics America's parent company, the Hyundai Group, is 37th on *Fortune* magazine's 1983 list of the world's 500 largest industrial companies outside the US.

Samsung has an $8 million investment in Tristar, which has a wafer fabrication facility located in Santa Clara, CA. Its first products will include high-demand parts, such as 64K DRAMs and 16K EEPROMs.

Gold Star, which has targeted the telecommunications market, has established an office in Sunnyvale, CA to act as a liaison with VLSI Technology Inc., with whom they have a technology agreement.

Daewoo established ID Focus (IDF) as its US operation. Initially, IDF will concentrate on the design of packages for television sets, microwave ovens and video cassette recorders. By 1985, it plans to build ICs for those items.

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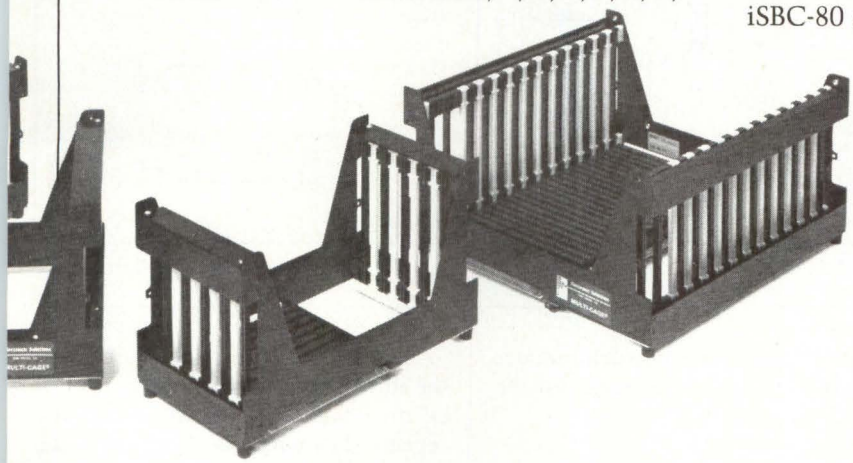

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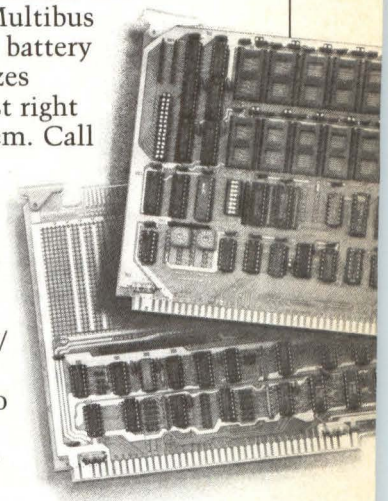

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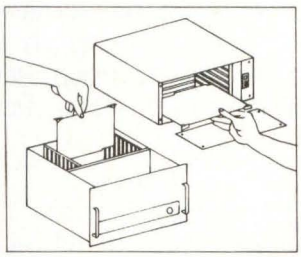

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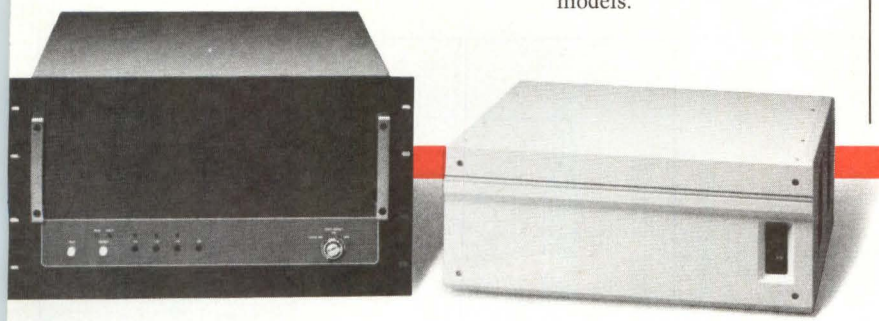

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16-Bit CMOS Pipeline Register Replaces Multiple Circuits In DSP Delay Functions

by Kevin Kiely

Kevin Kiely, Vice President of Technology, Logic Devices Inc., Sunnyvale, CA, is one of the founders of Logic Devices Inc. He previously worked in process development and process engineering at Fairchild Camera & Instrument and Advanced Micro Devices, and holds a B.S. in physics from the University of Santa Clara.

Digital signal processing (DSP) operations involving the delay of an operation or instruction are fundamental to filtering, convolution, and correlation functions. In most DSP systems, registers are used as the short-term memory elements for these delay or staging processes.

However, the devices needed to implement the delay function with conventional TTL circuits consume valuable board space and require what some designers consider to be excessive power.

These limitations can be overcome with a CMOS multilevel pipeline register with four 16-bit registers (**Figure 1**). The circuit can replace eight octal registers or two 8-bit pipeline registers, and offers the traditional CMOS advantages of low power consumption and low operating temperature.

The pipeline registers, the LPR520 and LPR521, are fully TTL-compatible and operate at access speeds of 25 nsec or less. Each can be configured as two pairs of two registers or as a four level pipeline, and features two sets of output/input instructions for increased flexibility. All four registers are individually selectable at the output, and all 16 data outputs have three-state capability.

The LPR520 and LPR521 differ only in how data is handled and retained between registers on a load instruction. The LPR520 shifts data through its registers as new data is loaded, and overwrites the data in the last register. The LPR521 retains data in the subsequent registers and overwrites in the first.

Configuration of the circuit for a chosen application is determined by the instruction code entered at the I0, I1 inputs. Data is latched into a register on the rising clock edge.

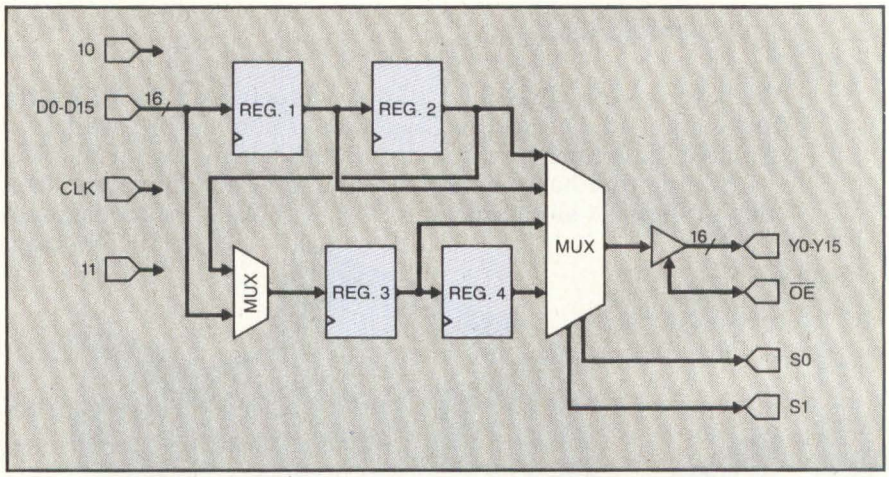

Figure 1: Functional block diagram of CMOS multilevel pipeline register with four 16-bit registers.

Depending upon the instruction code, data is shifted through the registers in the following manner:

Instruction

I1	I0	LPR520			
0	0	D→R1	R1→R2	R2→R3	R3→R4
0	1	HOLD	HOLD	D→R3	R3→R4
1	0	D→R1	R1→R2	HOLD	HOLD
1	1	HOLD	HOLD	HOLD	HOLD

I1	I0	LPR521			
0	0	SAME AS LRP 520			
0	1	HOLD	HOLD	D→R3	HOLD
1	0	D→R1	HOLD	HOLD	HOLD
1	1	SAME AS LPR 520			

A logic low on the enable line enables the three-state outputs. Another set of control lines, S1 and S0, select the register data which is to appear at the output. As follows:

S1	S0	Output
0	0	Reg. 4
0	1	Reg. 3
1	0	Reg. 2
1	1	Reg. 1

The independent operation of the input (I) and output (S) instruction sets allows data to be written to a register while it is being read from any independently selected register. This feature enables use

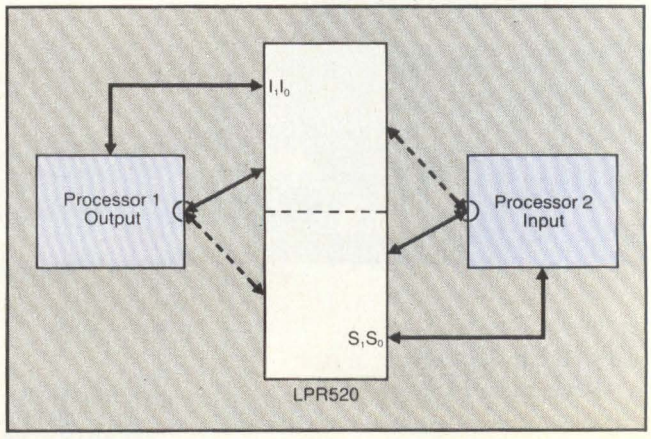

Figure 2: The LPR-520's ping-pong configuration.

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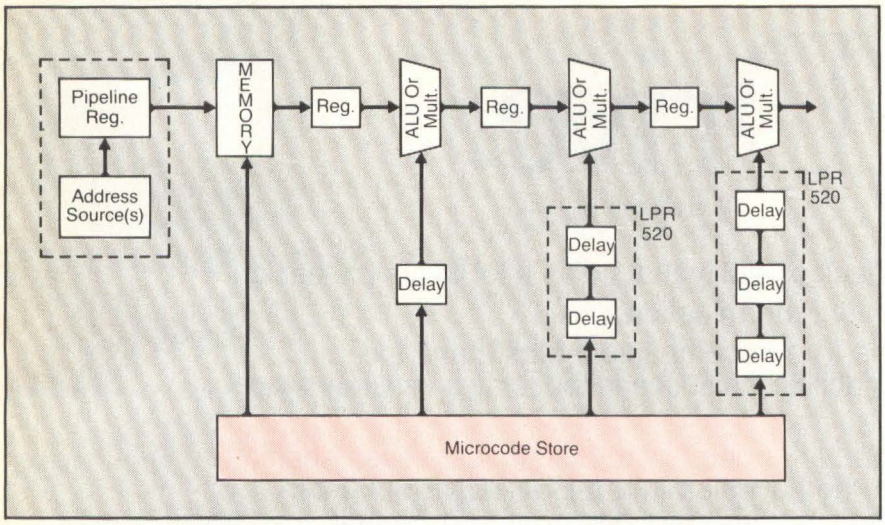

Figure 3: Instruction pipelining.

of the LPR520 as a double buffer or "ping-pong" memory element. For example, **Figure 2** shows two processors which transfer data or results from one to the other. As processor 1 writes data to the buffer, processor 2 can read the result placed into the other register bank. The operation might involve the following sequence:

CLK 1 is initiated. Processor 1 asserts I=2 instruction and writes to register 1, while:

Processor 2 asserts S=1 instruction and reads register 3.

CLK2 is initiated. Processor 1 asserts I=1 instruction and writes next data to register 3, while:

Processor 2 asserts S=0 instruction and reads register 1.

The LPR520 and LPR521 can also be used as delay elements when two or more delays are required to synchronize microfields with data flowing through a pipeline architecture, and they can provide the reconfigurable delay or address staging required by exception conditions or branches in some pipeline circuit designs.

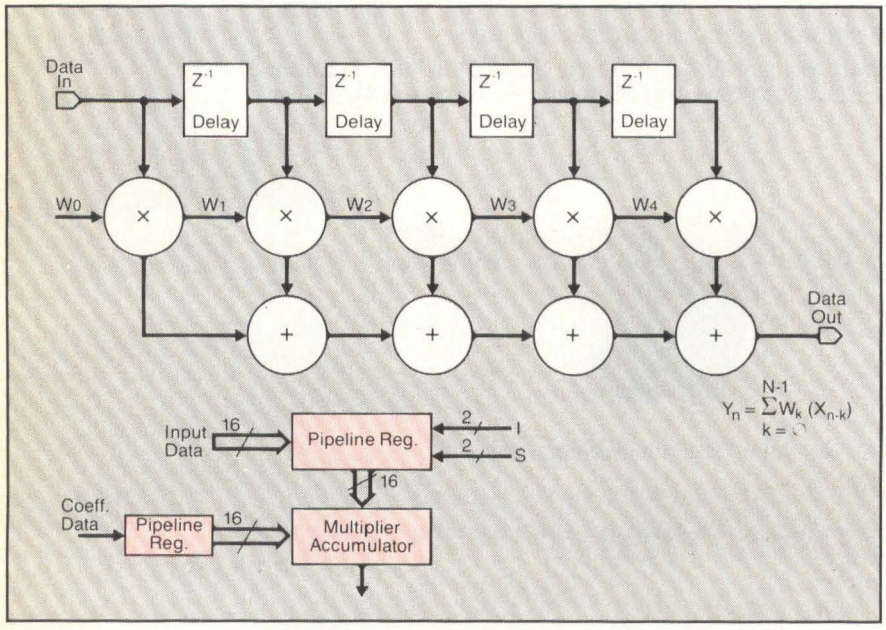

Figure 4: FIR Filter Implementation.

In pipelined digital signal processing operations computation or operations are divided into separate stages, each of which processes a different piece of data at a given time. The data is then shifted further along the pipe into the next stage (operation).

Once such configuration is shown in **Figure 3**. The delay element of the "data stationary" architecture stages the microcode field(s) such that they become synchronous with the appropriate data flowing through the pipeline. The LPR520 is appropriate as this delay element when two or more delays are required.

The pipeline register also complements the flow of addresses *into* the pipeline memory. In systems where operation is highly parallel, addresses must be pipelined to memory (see dashed-in area of **Figure 3**). Through appropriate use of the control ports I and S, the LPR520 and LPR521 can provide reconfigurable delay or address staging necessitated by an exception condition (such as a branch) in the pipeline.

The ability of the pipeline register to act as a delay element is also useful in an application such as the finite-impulse-response (FIR) filter frequently found in digital signal processing. For a non-recursive N-th order filter, each output sample consists of the sum of the past N points each weighted by a filter coefficient. That is:

$$Y_n = \sum_{k=0}^{N-1} h_k(X_{n-k})$$

where: Y_n = the nth order output sample
n = the data index
k = the coefficient index
N = order of the filter
h = kth filter coefficient
x = the input sample
X_{n-k} = input sample *delayed* by k sample periods

A flow diagram representation and equivalent circuit implementation are shown in **Figure 4**. By applying the proper S1, S0 combinations, one can successively read the data values to the multiplier/accumulator (MAC). Of course, the pipeline register clock must allow for sufficient time for the MAC to read each of the LPR520 registers.

Because the number of multiplications and additions needed in the filtering process can be large, a common technique is to employ time decimation to reduce the number of computations. This method

simply involves selecting only regularly-spaced output samples of a lowpass filter. Thus, by applying several clock pulses to the LPR520 between computations of successive filter output points, an easily realizable decimation is accomplished with resultant reduction in multiply and add operations.

Multiple LPR520/521s can be cascaded to implement a filter requiring more delay as shown in **Figure 5**. In this setup, when $\overline{OE}$ is high, the S1, S0 inputs are used to read the first four registers. When $\overline{OE}$ is low, data can be read sequentially from the second device and presented to the MAC.

Circle 241

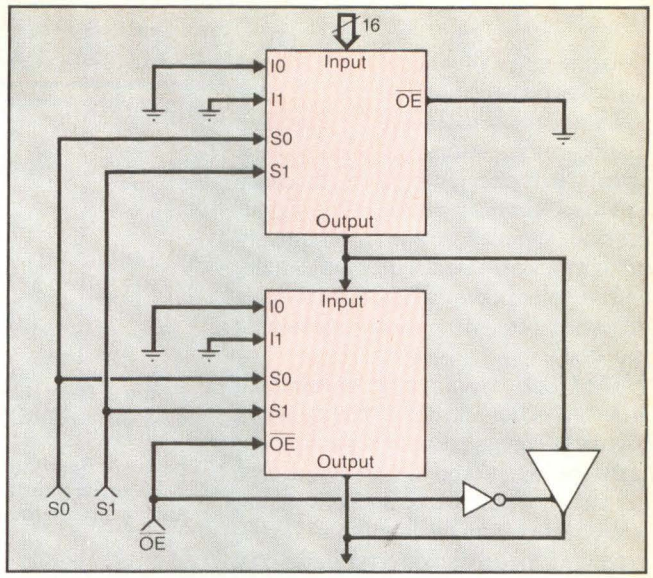

Figure 5: Cascading of LPR520.

Speech Compression Made Easy With An ADPCM Speech Encoder/Decoder

by Sayuri Tung

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Since the encoding bandwidth of speech is directly proportional to the required transmission bandwidth, speech compression has been a subject of intense study. One promising approach for reducing bandwidth and yet retaining toll quality speech is to use adaptive differential pulse code modulation (ADPCM). (Toll quality is defined as equivalent quality to 56 Kbps μ-law PCM.) Until recently, ADPCM compression techniques required expensive hardware implementation, and were economical only in less cost sensitive applications. The rapid advances in VSLI technology and system architecture, however, offer an alternative hardware solution: a single-chip digital signal processor. The inexpensive yet high-performance digital signal processing microcomputer can be programmed to perform ADPCM encoding and decoding. One such device is the NEC μPD7730, a speech encoder/decoder (SED). The specific ADPCM used employs a proprietary robust adaptation scheme for a quantizer and a predictor to withstand transmission bit errors. Using these devices, toll quality speech can be realized at 32 Kbps, providing lower bandwidth at lower cost.

Adaptive Differential Pulse Code Modulation (ADPCM)

Adaptive Differential Pulse Code Modulation is a medium-bandwidth coding technique used to compress speech signal by coding the differential signal between consecutive samples. In order to cover the

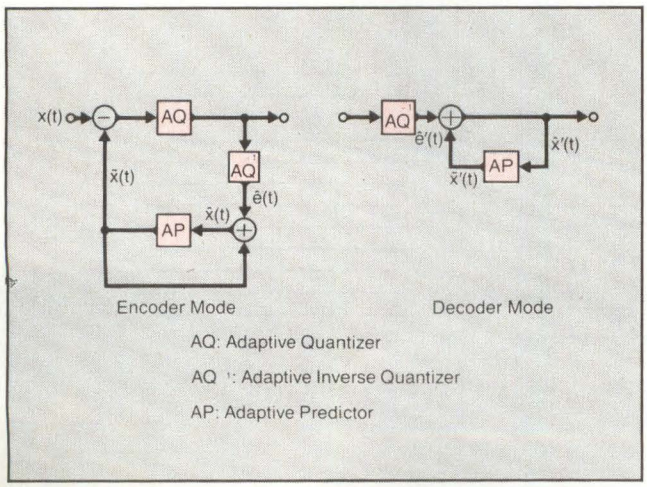


Figure 1: Conventional ADPCM system.

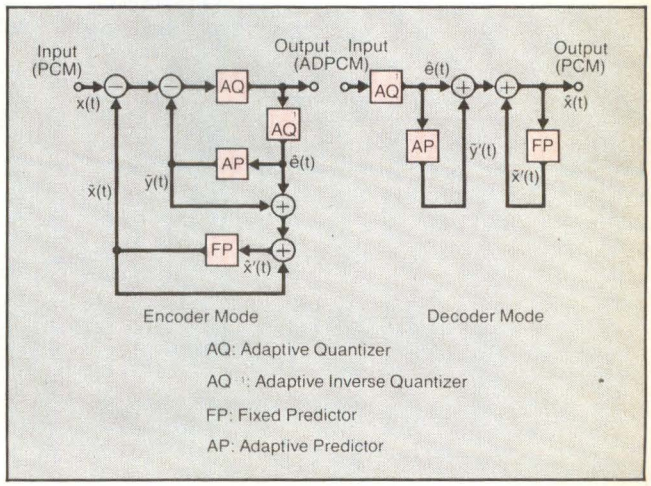


Figure 2: Proposed robust ADPCM system.

dynamic range of voice signals and yet minimize quantization noise, an adaptive quantization scheme is used (i.e. the quantization step size varies as a function of the signal). To further remove the redundancy and to reduce the variance of the signal, previous samples are used to adaptively predict the next value of the next sample, and the value of the difference of the predicted sample and the successive sample is coded.

The block diagram of a conventional ADPCM coder and decoder is shown in **Figure 1.** The system operates as follows: in the encoder, the predicted value at time instance t, $\tilde{x}(t)$, based on previous values, is subtracted from the input signal, x(t), to produce the prediction error signal e(t).

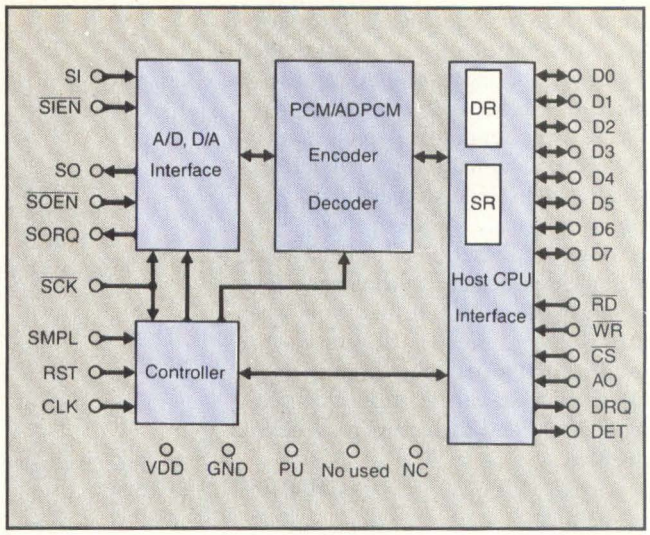
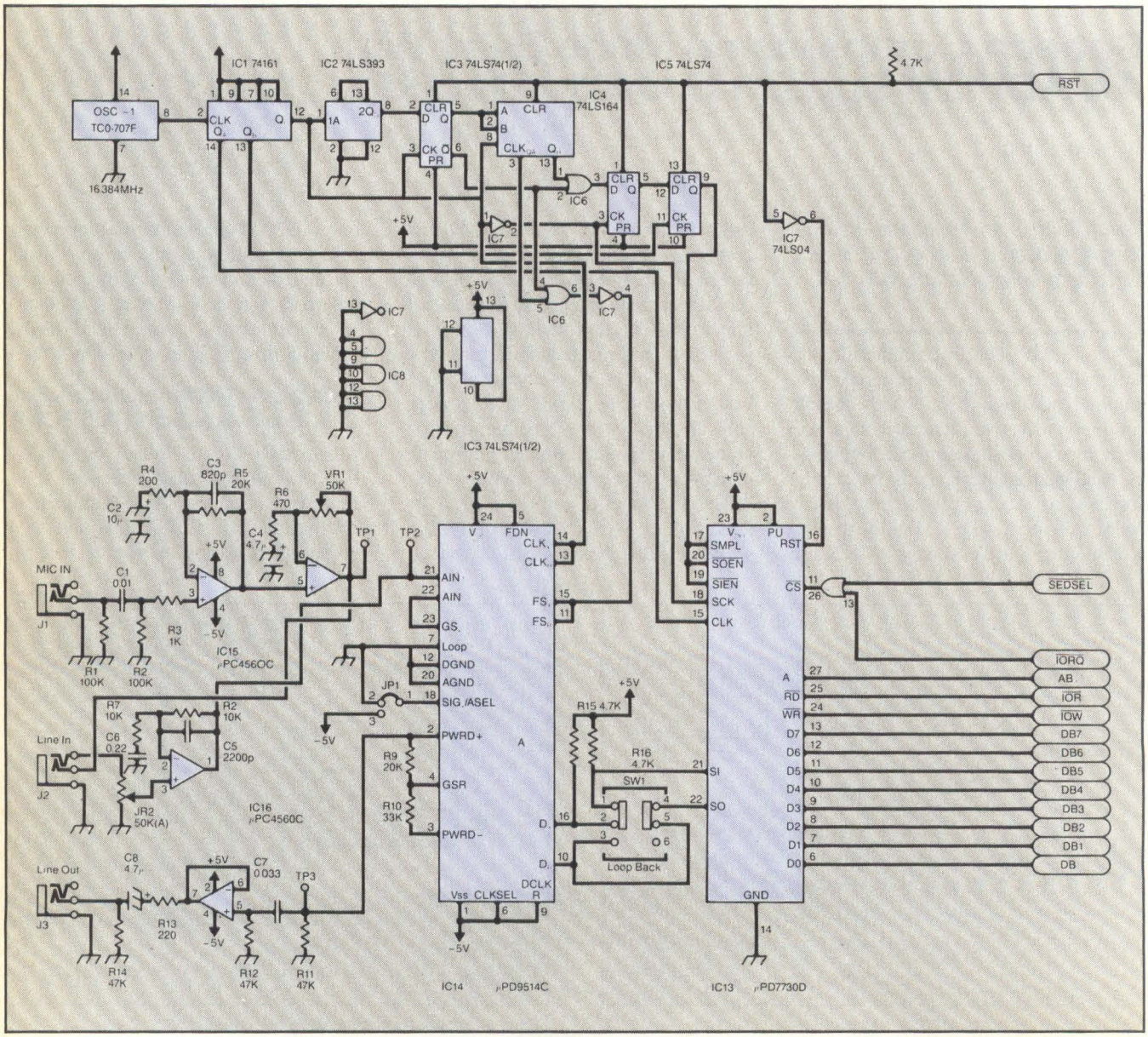
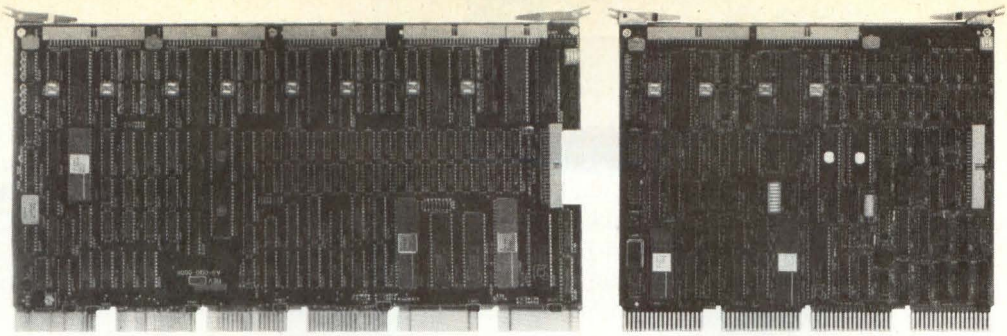


Figure 3: Right, block diagram of μPD7730.

Figure 4: Below, μPD-7730 serial interface and timing control.





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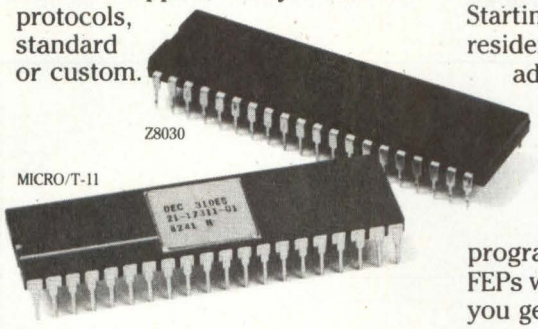

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The error signal is quantized by the adaptive quantizer, AQ, and transmitted to the receiver. In decoding the ADPCM code, the code passes through an inverse adaptive quantizer and the predicted signal $\tilde{x}'(t)$ is regenerated. If the transmission was error free, then $\tilde{x}(t)$ is the same value as $\tilde{x}'(t)$.

A common way to model the predictor is to use a weighted linear combination of past output values, i.e.

$$P(z) = \sum_{j=1 \text{ to } N} a_{jz-j}.$$

Although the all-pole model generates good prediction, this transfer function can become unstable in the presence of transmission errors. The instability can occur because the transmitted error signal can influence the reconstructed output speech for an infinite amount of time. Under noisy transmission conditions, the received error signal can cause the adaptive pole position to shift outside the unit circle, and result in an unstable IIR filter.

One approach to designing a robust encoder/decoder that is immune to transmission error is to approximate the all-pole model with fixed poles and adaptive zeros. The resulting transfer function has the form

$$V(z) = (1 + \sum_{i=1 \text{ to } M} b_{jz-i}) / (1 - \sum_{j=1 \text{ to } N} a_{jz-j})$$

where a_j determines the positions of fixed poles and b_i determines the positions of adaptive zeros.

A block diagram of this robust ADPCM system is shown in **Figure 2.** The encoder has two levels of prediction: the fixed poles and the adaptive zeros. This decoder is composed of a cascade of an adaptive non-recursive filter (FIR) and a fixed recursive filter (IIR). FIRs are inherently stable because with no feedback, the effect of the input signal can only affect the output signal for a limited sample time (equal to the order of the filter.) Since the IIR filter is fixed and cannot drift to become unstable, the whole cascaded system will remain stable. The prediction value, $\tilde{x}(t)$, is

$$\tilde{x}(t) = \sum_{j=1 \text{ to } N} a_j x(t-j) + \sum_{i=1 \text{ to } M} b_i e(t-i)$$

The above structure, with fixed poles and adaptive zeros, attains both high prediction capability and robustness, and is the algorithm used in the NEC μPD7730 speech encoder/decoder.

Hardware Environment

The μPD7730 can operate in two different modes: encoder mode and decoder mode. Although each μPD7730 can perform both encoding and decoding function, it can only be set to one of the two modes at one time. Therefore, for simultaneous encoding and decoding, two μPD7730s, one for each direction, are required.

In encoder mode, the μPD7730 takes in either linear or μ-law PCM data from its serial voice interface, encodes it to ADPCM data format, and passes the ADPCM data through the parallel data bus to the host system. In the decoder mode, the μPD7730 receives the ADPCM data from the host system, decodes it to either linear or μ-law format, and sends it out to the output port of the serial voice interface.

The μPD7730 provides serial interfaces that can be directly connected to a single-chip PCM CODEC. It interfaces easily to a host CPU through its parallel bus. With its standard microprocessor bus interface, the μPD7730 can be simply viewed as a complex peripheral circuit. A functional block diagram of the μPD7730 is given in **Figure 3.**

The A/D, D/A interface can accept either linear or μ-law PCM data. The timing of the serial data is controlled by the SCLK. When the μPD7730 has data to transmit to the serial interface, it raises SORQ. The data is clocked out serially at the rising edge of the SCLK after SOEN* pin is asserted. When the serial data is ready to be received at μPD7730, SIEN* pin is asserted, and data at SI pin is clocked in at the rising edge of SCLK. SMPL pin signals the μPD7730 firmware when a new PCM data has been received at the serial interface. SMPL signal is the same as the sampling clock used in the CODEC.

An example of the serial interface using a COMBO (combined filter and CODEC) chip, μPD9514C, is given in **Figure 4**. The COMBO chip provides both the lowpass filtering function and the conversion from an analog signal to digital PCM μ-law representation. As illustrated in **Figure 4**, with a proper timing controller, the interface to the analog input signal is a straightforward connection with the COMBO chip.

The μPD7730 interfaces to the host CPU through its bi-directional tristated parallel bus. The host CPU can send two types of commands to the μPD7730: control commands and threshold commands. Control commands select the mode of operation by writing to the Control Register. The Control Register selects the following functions: operation mode –

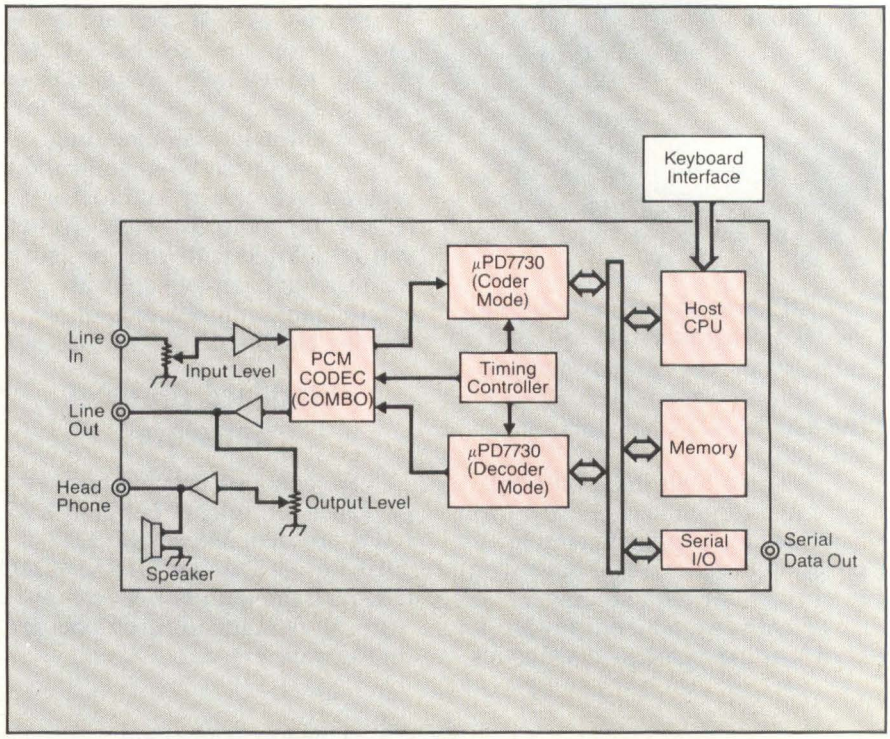

Figure 5: Block diagram of a voice store and forward system.

encoder or decoder mode; ADPCM data length – 3 bits/sample or 4 bits/sample; PCM data format – linear or μ-law. The threshold set command is given in the encode mode to establish the threshold of the input PCM data. The host CPU can also find out the status of the μPD7730 by reading the Status Register. After properly setting the Control Register, the μPD7730 automatically processes the input speech signal without further attention from the host CPU.

The parallel bus is also used to transfer ADPCM data to and from the system bus and the μPD7730 under the direction of the host CPU. When the μPD7730 is in the encoder mode, the DET pin signals the host CPU when encoded ADPCM data is available. In the decoder mode, the DRQ pin requests transfer of ADPCM data from the host to the μPD7730. Data is transferred to and from the CPU by memory mapped I/O operations.

The μPD7730 allows system designers to design a speech compression system without speech processing expertise. Besides the analog interface, the rest of the system can be designed as a standard microprocessor system. As an example, a block diagram description of a voice store and forward system using μPD7730s is illustrated in **Figure 5**. The analog interface is the same as the interface shown in **Figure 4**. Since the speech processing is transparent to the designer, the μPD7730 can be viewed simply as a complex peripheral.

At initialization, the host CPU will program one μPD7730 to encoder mode, and the other μPD7730 to decoder mode. When voice store function is requested through the user keyboard interface, the host CPU sends a stored prompt message (in compressed ADPCM representation) to the decoder μPD7730, which outputs the message in audible form. The speaker inputs his utterance through a microphone. The encoder μPD7730 signals the host when input ADPCM data is available. The host reads the coded speech through the parallel bus and can store the input speech in either the on-board memory or auxiliary memory through the serial I/O. To play back stored messages, the host sends the encoded speech to the decoder μPD7730. The decoded speech is sent to the COMBO chip and output in analog form. The host CPU's function is only to move the ADPCM coded speech. It does not have to further process or to massage the coded speech at any time.

Conclusion

The μPD7730 offers toll quality speech encoding and decoding capabilities in a single chip at 32 Kbps. It integrates speech coding with a high-performance signal processor. Rapid advances are being made today in the area of communications. New communication services, such as voice store and forward system, are now being offered. The μPD7730 can be part of this new development for applications which require either less transmission bandwidth or less storage capacity for voice. **Circle 240**

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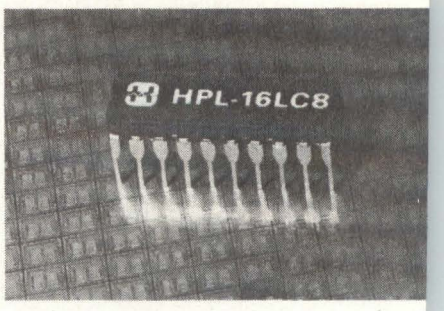

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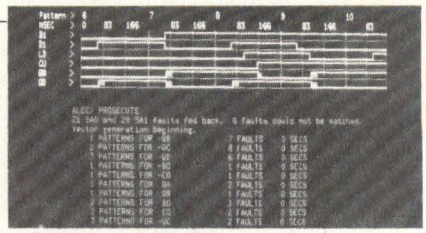

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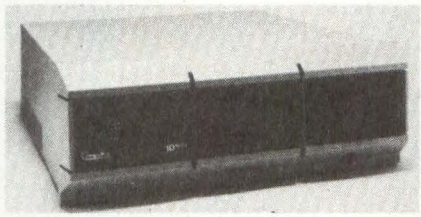
The 21A EPROM programmer programs over 120 MOS and CMOS EPROMs and EEPROMs up to 256K. The 21A incorporates comprehensive self-testing and device testing. Features include 32K × 8 data RAM, full hexadecimal keyboard, RS-232-C serial I/O, comprehensive data editor, seven data transfer formats, front-panel entry of baud rate, parity and stop bits, remote control software and comprehensive error reporting. Price is $1,450. **Data I/O**, Redmond, WA **Circle 159**

Dual 68000-Based Supermicro

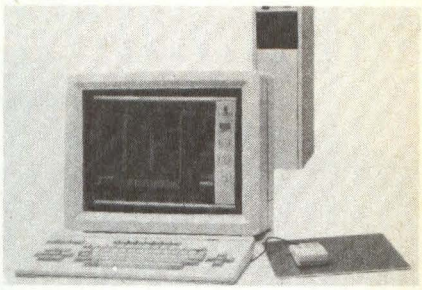
The 1124 32-bit processor system features a dual 68000/UNIX engine. The system includes mirrored disk drives, power margining, EDAC memory protection, redundant cooling and an optional UPS. The 1124 architecture provides a series of data paths that optimize memory access, interprocessor communications and data transfer. The 1124 has ten card slots: three for CPU and memory cards, six for I/O expansion and the remaining for a memory controller that manages the data flow among the cards. Memory is available in 2-Mbyte increments. Price is $60-$75,000. **Areté**, Washington, DC **Circle 174**

Multi-User Business System



The CompuPro 10 Plus, an enhanced version of the CompuPro 10, is a four-user microcomputer. The CompuPro 10 Plus gives each user his own dedicated 8-bit CPU with the capability of accessing 16-bit power. The system includes an 8 MHz, 16-bit 8088 central processor with 768 Kbytes of main memory, four 8-bit Z80B user processors each with its own 64 Kbytes of RAM, seven serial ports including a modem port, a Centronics printer port, up to 512 Kbytes of solid state disk memory, and dual 96 tpi 5¼" floppy disks each storing 1 Mbyte. An optional 20 or 40 Mbyte hard disk is available. Price is $4,995. **CompuPro**, Hayward, CA **Circle 160**

Electronic Design Workstations



Cadnetix has added the CDX-5000A, a cost-reduced version of the CDX-5000 workstation with virtual memory capability; the CDX-50000, a high performance CAD system with a graphics accelerator engine; and the CDX-59000, a design and layout workstation with CAE/CAD capability. All three MC68010-based systems are equipped with a 1024 × 800, bit mapped, 64 color, 120 Hz interlaced display and a 40 Mbytes Winchester and 1 Mbyte floppy for storage. The CDX-5000A has the same 32-bit architecture as the CDX5000. The system includes 1.5 Mbyte of internal memory, exandable to 2.5 Mbytes, with a virtual memory operating system. The CDX-50000's graphics accelerator engine is based on a bit-sliced processor with an 88-bit wide microcode work. Features of the CDX-59000 include the CADAT 12-state logic simulator and a Scald-based timing analyzer. **Cadnetix**, Boulder, CO **Circle 161**

BOARDS

Wire-Wrap Board

The DSSEWRAP board is a double Eurocard wire-wrap board with a fully decoded VME bus interface (master or slave). It interconnects directly to and is compatible with the VME bus. Features include address decoding for words up to 32 bits, TTL-compatible buffered inputs for the address and control bus, and 3-state TTL compatible buffered inputs and outputs for the data bus. The base address is jumper selectable anywhere in the 16 Mbytes memory map. The DSSEWRAP requires +5 V and ± 12 V and draws 3 amps, maximum. The board is supplied with 40-pin front panel connector. Price is $495. **Data Sud Systems**, Tempe, AZ

Circle 157

2 Mbyte LSI-11 Memory Board

The MM22 memory board for the DEC Q bus is compatible with LSI-11/23, 11/73 and MicroVax I processors. It is a single dual-width module with a typical access time of 30 nsec in the block transfer mode. The MM22 is compatible with 256K and 64K DRAM for maximum capacities of 2048 Kbytes. It features low power consumption and requires 1.0 amp at +5 V. The MM22 includes user programmable jumpers for 22- or 18-bit addressing, 16 or 256 word block mode capability, 4K or 2K word I/O page, standard or optional CSR address, CSR disable and parity logic disable. Price is $1,295. **Andromeda Systems,** Canoga Park, CA

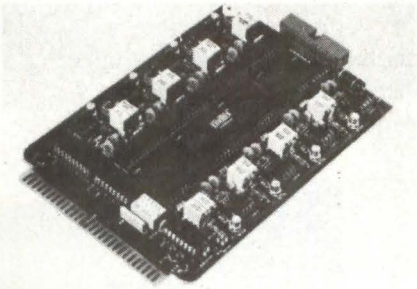
Circle 149

Intelligent STD Bus Boards

The MDX-I488 and MDX-ISIO STD bus boards feature an on-board Z80 CPU, a Z80 DMA chip, byte-wide sockets for RAM and ROM, and a Mostek-developed gate array that serves as an interface for the STD bus and local bus on the board. The MDX-I488 implements the GPIB with data transfer rates of up to 300K bps. The MDX-ISIO implements dual RS-422 serial communications channels via a Zilog 8530 serial communications controller. It features bit sync, byte sync, and async operation, and has software programmable baud rates up to 1 Mbaud. Both boards may be used in systems with clock rates of up to 4.0 MHz. Price is $550 (I488) and $620 (ISIO). **Mostek**, Carrollton, TX

Circle 150

STD Boards



The MP6202 EPROM/RAM memory board, MP6303 analog input board, MP6309 DC power supply board, MP6304 parallel input/output board and the MP6305 8-channel D/A converter board are all STD bus compatible. The MP6202 offers up to 32 Kbytes memory support. The MP6303 is a 32-channel, 12-bit differential input A/D converter board for STD bus-related data acquistion applications. The MP6309 generates a precision ± 15 V from the +5 V STD Bus. The MP6304 provides 48 bits of user configurable inputs and outputs. The MP6305 features an average settling time of 2.3 μsec to ± ½LSB, and relative accuracy of ± 0.1% FSR. In the current mode, 4-20 mA typical may be provided on or off board. In the voltage mode, the output is configurable for unipolar (0-10 V) or bipolar (± 5 V) operation. **Burr Brown**Tucson, AZ.

Circle 148

PERIPHERALS

Matrix Line Printers

The HP 2566A matrix line printer prints up to 900 lpm, the HP 2565A, 600 lpm. Up to 14 fonts may be installed at one time and mixed in a line of print. Both printers can print bar codes, labels and can handle multi-part forms. Both printers feature high speed graphics. The standard character set in the HP

2565A and the HP 2566A is 8-bit Roman8. Optional OCR-A and OCR-B character sets are also available. Horizontal positioning of four paper tractors is motor-driven to simplify paper loading and alignment. The printers can link up to HP 3000 and HP 1000 computer systems through HPIB. Optional interfaces include RS-232-C, RS-422A, Centronics parallel and HP 2608A. Price is $18,766-$21,766. **Hewlett-Packard**, Palo Alto, CA **Circle 184**

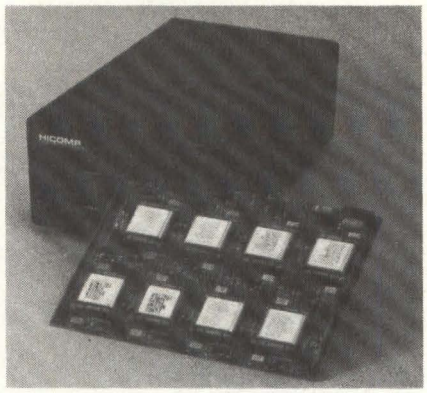
Gas Plasma Touch Input Display System

The VuePoint II employs a 12 line × 40 character, gas plasma display and a wide angle viewing cone of 120°. Other features include 12 × 20 resolution, optical touch-sensor design, a sealed screen design, formatting, field definition and cursor control. Interfaces include RS-232-C, 422A, 423A, 449, 485, TTL, 20 mA and others. The VuePoint II NEMA-12 19″ enclosure protects against dust, dirt, airborne debris, seepage, splashes and external condensation of non-corrosive liquids. **General Digital**, Hartford, CT **Circle 179**

Aperture Card Scanner

ACRIS (Aperture Card Raster Input Scanner) enables transmission of aperture card images to remote Versatec plotters or standard Bisync 3780-compatible host at line speeds from 2400 to 19.2 Kbaud. A complete system includes transmitter, receiver, ACRIS scanner, Versatec plotter, and customer-supplied modem. Options include disk spooling at receiver for non-stop high quality plotting, added console and 56 Kbaud data transfer. ACRIS digitizes silver or diazo film aperture card images for plotting on any 200 or 400 point/inch Versatec electrostatic plotter. Price is $13,500. **Versatec**, Santa Clara, CA **Circle 180**

Bubble Memory Storage System



The MBM-1A is available with 0.5 or 1.0 Mbyte of solid state, non-volatile, bubble memory in an enclosure the size of an 8″ floppy disk drive. It can be interfaced to a computer as a floppy disk drive or as a block access peripheral. In the floppy disk mode it can function as up to four separate 5¼″ or 8″ disk drives. The required interface is a Shugart compatible floppy disk controller. In the block access mode, individual blocks of bubble memory can be randomly accessed in 512 byte block segments; the required interface is an RS-232-C compatible serial I/O port. Price is $4,950 (1Mbyte) and $3,450 (0.5Mbyte). **Hicomp**, Redmond, WA **Circle 175**

X.25 Multi-Port Pad

The PDN5220, a high performance X.25 multi-port pad, acts as a gateway between SNA users and packet switching data networks that have interfaces complying with CCITT recommendation X.25. It offers transparent communication between remote SNA clusters and SNA host processors in a network. The PDN5220 performs automatic call setup, packetizing of SNA path information units, local polling of the cluster and flow control. It supports the standard error recovery procedures for each communications protocol, detects modem failure and recovers automatically. It is available with 2, 4, 6 or 8 ports and with 3270 SNA/SDLC, 2780/3780 BSC and Asynch protocols. Price is $6,500. **Paradyne**, Largo, FL **Circle 183**

Intelligent Page Printer

The GQ-300 is an intelligent page printer which combines a liquid crystal shutter with electrophotographic technology. It prints seven pages/minute with character density of 240 dpi. The GQ-300 features multifont and software selection capabilities. Other capabilities include portrait or landscape printing, gray scaling, underlining and justification. Price is $4-$5,000. **Epson**, Torrance, CA **Circle 177**

COMPONENTS

Semicustom ICs

The V1200, V1700 and V3500 bipolar macro arrays can simultaneously interface with external ECL and TTL logic and provide equivalent internal gate delays of 800 psec at 1 mW gate. The arrays are composed of a logic cell and an I/O cell. They are packaged in pin grid arrays, leadless ceramic chip carriers and ceramic DIPs. The process yield technology yields 1.9 μm effective gate lengths and a typical loaded delay of 2.5 nsec for a 2 input NAND gate. The VL400 and VL800 bipolar linear arrays are interconnected components on second level metal to create custom linear integrated circuits with supply of 20 V maximum. Components on the array include five different NPN transistors capable of handling from 30 mA to 100 mA and five different PNP transistors. Price, in quantities of 10,000, is $3.25-$13.50. **Vatic Systems**, Mesa, AZ
Circle 138

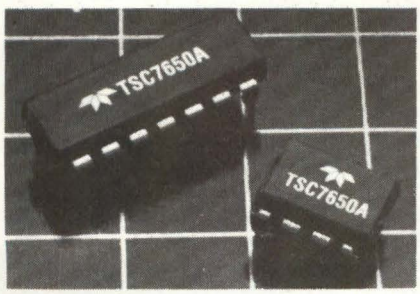
12-Bit D/A Converters

The DAC1265A and DAC1265 12-bit D/A converters use 12 precision high speed bipolar current steering switches, a control amplifier, a thin film resistor network and a buried zener voltage reference to obtain analog output current. They have 10-90% full-scale transition time under 35 nsec and settle to less than LSB in 20 nsec. The converters feature precision thin film resistors that can be used with external op amps for voltage out applications or as input resistors for successive approximation A/D converters. **National Semiconductor**, Santa Clara, CA
Circle 137

256K Dynamic Random Access Memories

The μPD41256, a 256K × 1 page-mode device, μPD41257, a 256K × 1 nibble-mode part in a ceramic package, and the μPD41254, a 64K × 4 device are all 256K dynamic RAMs. Access times for all three parts are 150 and 200 nsec. They are implemented in NMOS technology with double poly interconnects and are all non-redundant. Price is $27.50 ($\mu$PD41256), $30 ($\mu$PD41257) and $33 ($\mu$PD41254). **NEC Electronics**, Mountain View, CA
Circle 134

CMOS Operational Amplifier



The TSC7650A is a chopper stabilized operational amplifier with a 5 μV maximum offset voltage specification. It is pin compatible with the ICL7650 device but with a 2.5 mA maximum supply current specification. The offset voltage drift is 0.2 μV/°C. The TSC7650A nulling scheme corrects DC offset voltage error and offset voltage drift with temperature. An internal nulling amplifier corrects its own Vos error and the main amplifier Vos error. Offset nulling voltages are stored on two user supplied capacitors. System error sources are further reduced by 120 dB minimum open loop voltage gain, common mode rejection and power supply rejection specifications. A 1 V common mode signal causes a 1 μV Vos change. Operating from ± 5 V supply, the common mode voltage range extends from -5.0 V to 1.5 V minimum. Slew rate is typically 4.0 V/μsec and the unity gain bandwidth is 1.0 MHz. Price is around $2-$7. **Teledyne Semiconductor**, Mountain View, CA.
Circle 129

HCMOS Arrays

The LL8000 Series is a 2-micron, 2-layer metal HCMOS array family with 10 mA buffers reconfigurable to 20 mA output. Gate counts range from 880 to 3200 (2 input NAND). Delay times are identical to the LL7000 Series. The LL8000 Series is supported by more than 200 LL7000 macrocells, and more than 400 LL7000 Series macrofunctions with better than Schottky TTL speeds. **LSI Logic**, Milpitas, CA
Circle 143

CMOS 8-Bit Video DAC

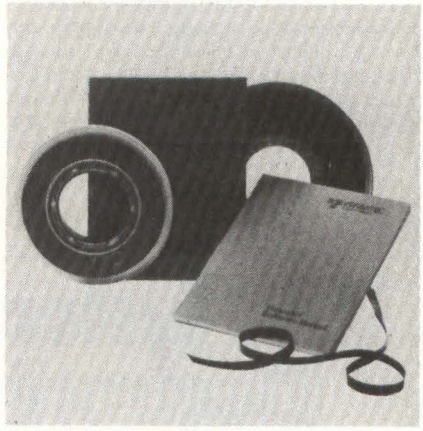
The TML1842 8-bit video DAC for graphics terminals has composite sync, composite blank, and 10% bright signals. Packaged in a 20-pin plastic 0.3 wide DIP, the TML1842 can drive 75 ohm or 37.5 ohm loads while operating at a minimum conversion rate of 25 MSPS. The TML1842 has a linearity of one bit, requires a single +5 V power supply and is TTL/CMOS compatible. The TML1842 directly drives the cables to the monitor; no external buffer amplifier is required. Price is $18.11. **Telmos**, Sunnyvale, CA **Circle 135**

8-bit CMOS Microprocessor

The single-chip CDP6805E3 is an improved model of the CDP6805E2 and can address 164 Kbytes of external memory. The E3 has 13 I/O lines and the E2, 16. Both are fully static CMOS devices that contain a CPU, on-chip RAM (112 bytes), I/O and an internal 8-bit timer with a software programmable 7-bit prescaler. The typical full speed operating power is 35 mW when operating from a 5 V power supply. Both operate on 8-bit multiplexed address and data buses and offer indexed addressing. Two hardware interrupts, timer and external, and one software interrupt can be used. Master and power-on resets are provided. The E2 and E3 are packaged in a 40-lead plastic DIP specified for a temperature range of 0 to 70°C. Price, in quantities of 1,000, is $8.34 (E2) and $9.18 (E3). **RCA**, Somerville, NJ **Circle 140**

SOFTWARE

Electrostatic Plotting Software Support



Universal Versaplot 9 software generates plots on Versatec monochrome electrostatic plotters using any 32-bit computer operating system. Versaplot offers user-definable clipping window, plotting viewport and pen attributes. The software supports remote applications on qualified systems, automatically strips plots wider than the plotter in use, and provides for area toning, plot rotation and grid generation with line masks. Price is $2,000. **Versatec**, Santa Clara, CA **Circle 191**

PL/M On A VAX

The Bridge Development System enables users to compile and run PL/M-86 programs from any terminal attached to a VAX. The Bridge runs an ISIS emulator on the user's embedded microprocessor; Bridge operates as a normal task which attaches to a "cell" on the coprocessor board. Intel-supplied compilers and debuggers may be run directly under the ISIS emulator. VMI-supplied utilities will allow transfer between the ISIS and VMI environments. Bridge executes many MS-DOS development and business applications. Price is $9,900. **Virtual Microsystems**, Berkeley, CA **Circle 188**

Software Interface Package

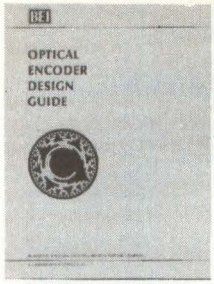
The Daisy-factron software interface package links Daisy's CAE workstation to Factron's test systems. The package allows engineers to capture information generated in the design phase. The information is then translated into a test program to be used for production test or debugging of complex VLSI-based boards through a guided-probe technique. Price is $3,800. **Daisy Systems Corp.**, Mountain View, CA **Circle 193**

New Software Packages

ABEL 1.1 supports over 95 programmable logic devices. It features logic descriptions by Boolean equations, truth tables and state diagrams in any combination, direct use of Boolean, relational and arithmetic operators, automatic DeMorgan conversion, logic reduction, a debugging simulator with trace and breakpoints, diagnostic error messages and debugging list files. The PROMlink allows an IBM PC to control Data I/O programmers by using simplified programmer menus. PROMlink runs under PC DOS on any IBM PC or XT with at least 125 Kbytes memory and a single floppy drive. Price is $895 (ABEL 1.1) and $295 (PROMlink). **Data I/O**, Redmond, WA **Circle 192**

NEW LITERATURE

Optical Encoder Design Guide. This 12-page booklet is a primer on optical shaft angle encoders from BEI Electronics' Industrial Encoder Division. It differentiates between absolute and incremental styles of encoders and explains the use of tachometer and quadrature type outputs. It also describes count multiplication techniques and contains a glossary of terms and application notes.



BEI **Circle 263**

IC Products Guide. This 36-page guide from Ferranti Semiconductors organized according to product applications, contains technical information and highlights on its IC devices for telecommunications, data conversion, referencing, instrumentation and consumer products. Contained are color photographs of the applications of the product groups, an overview of the technological developments, as well as device circuit implementation. Also listed are data conversion devices.

Ferranti **Circle 261**

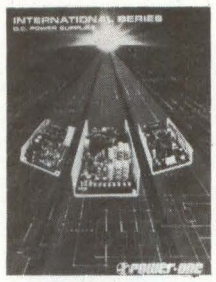
Optical Waveguide Brochure. This brochure describes optical waveguide market and product trends to 1990 and market applications. Also described are its Corguide optical fiber product lines of multimode and single-mode fibers. Outlined are factors researchers and engineers take into consideration during product design. Separate market application sheets explain long-haul, subscriber feeder, military and local-access uses of optical fiber.

Corning **Circle 258**

Micro Interface Book. These two volumes from Support Systems International contain diagrams, instructions, and research reports on interfacing micros to printers, CRTs, modems, and plotters; micros to minis; and micros to mainframes. The publication is updated quarterly by Command Computer Corp. and is offered on a subscription basis.

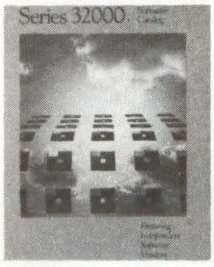
Support Systems **Circle 259**

Power Supply Catalog. This 28-page 1985 catalog from Power-One provides information, including photos and mechanical drawings, of its line of linear and switching DC power supplies. Specifications and prices are included for over 200 "off-the-shelf" models. An applications section discusses safety agency requirements for domestic and international marketing.



Power-One **Circle 267**

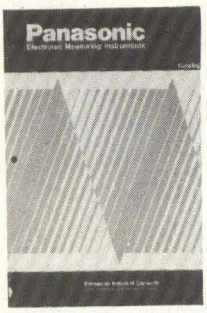
Software Catalog. This 138-page catalog from National Semiconductor details application, development and operating system software for the Series 3200 family. Described are its Genix and Exec operating systems, as well as other operating systems for the series. Also described are cross-software, languages and compilers, other systems software and application programs. Included are indices and cross-references by software type and more than 100 pages of product data.



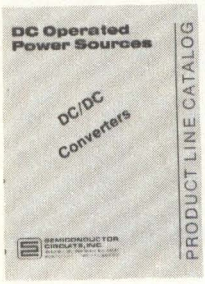
National Semiconductor **Circle 260**

NEW LITERATURE

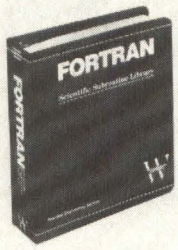
Multibus Product Catalog. This 72-page catalog from Central Data Corp. describes its product line of boards including CPUs, memories, disk controllers, I/O boards, and other boards and accessories. Descriptions include photographs, specifications and ordering information. A price list with terms and conditions is also attatched.
Central Data **Circle 251**



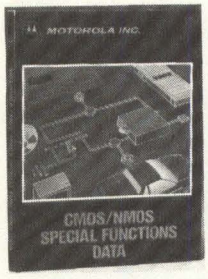
Electronic Measuring Instruments Catalog. This 48-page, 1984/85 engineering catalog of electronic measuring instruments from Panasonic Industrial Co. contains specifications on over 36 measuring instruments and/or models. Descriptions include a photograph, features and specifications.
Panasonic **Circle 266**



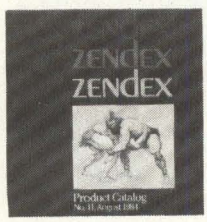
DC/DC Converters Catalog. This 24-page catalog from Semiconductor Circuits describes its high-performance DC/DC converters. Product descriptions include a photograph, general specifications, a chart showing dimensions and connections, and ordering information. Also included is a section on AC operated power supplies and a product selection guide.
Semiconductor Circuits **Circle 252**



Subroutine Software Library. This software from Wiley offers formulas designed to save programming time, solve practical problems and increase reliability of software design. The library consists of 114 pretested and precompiled subroutines. Contained are three diskettes, the source code, the subroutine library and the test programs, plus over 400 pages of instructions and reference materials.
Wiley **Circle 253**



CMOS/NMOS Data Manual. This manual from Motorola Logic and Special Functions Div. provides product specification and application information for more than 60 special function VLSI integrated circuits. Data sheets with specifications cover topics such as pin connections, block diagrams, testing and application information, and electrical characteristics. Handling and design guidelines are also provided.
Motorola **Circle 256**



Multibus Product Catalog. This 16-page catalog from Zendex Corp. describes over 75 Multibus products from single board computers to multitasking systems, relating them to application areas and computer systems. Covered are CPUs, as well as peripheral controllers including floppy, floppy/Winchester, serial I/O, serial communications and parallel I/O controller boards.
Zendex **Circle 262**

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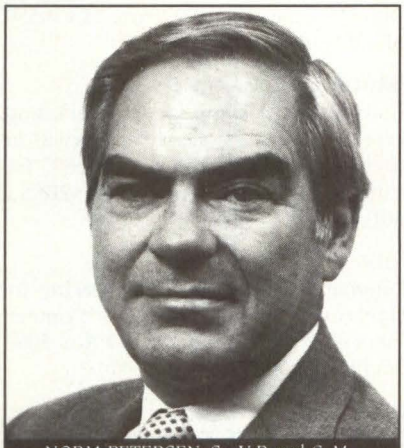

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Sept. 6, '84	Newton/Boston, MA
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Oct. 10, '84	Cherry Hill, NJ
Oct. 23, '84	Englewood/Denver, CO
Jan. 8, '85	Irvine, CA
Jan. 29, '85	Houston, TX
Jan. 31, '85	Dallas, TX
Feb. 26, '85	Ft. Lauderdale, FL
Mar. 19, '85	Palo Alto, CA
Apr. 2, '85	Nashua, NH / No. MA

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DD1/85

CALENDAR

January 14-17
CADCON/ATE West '85. Anaheim, CA. Contact: Morgan-Grampian Expositions Group, 2 Park Ave., New York, NY 10016-5667. (212)340-9780.

January 28-February 1
Advanced Pascal. Minneapolis, MN. Contact: Pam Kerwin, Institute for Advanced Technology, 6003 Executive Blvd., Rockville, MD 20852. (301)468-8424.

January 31-February 1
Data Communications and Networking for the IBM PC and Other Personal Computers. San Francisco, CA. Contact: Software Institute of America, Inc., 8 Windsor St., Andover, MA 01810. (617)470-3880.

February 3-5
Engineering Workstations. Monterey, CA. Contact: Institute for Graphic Communication, 375 Commonwealth Ave., Boston, MA 02115. (617)267-9425.

February 5-7
AOS/VS System Performance Workshop. Washington, D.C. Contact: Seminars, Educational Services—MS F019, Data General Corp., 4400 Computer Dr., Westboro, MA 01580. (617)366-2900.

February 12-15
Designing Digital Control Systems. Washington, D.C. (also in San Diego, CA on February 26-March 1.) Contact: Ruth Dordick, Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213)417-8888.

February 12-15
Digital Signal Processing. Boston, MA. Contact: Ruth Dordick, Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213)417-8888.

February 14-15
C Language: An Introduction. Boston, MA. Contact: Seminars, Educational Services—MS F019, Data General Corp., 4400 Computer Dr., Westboro, MA 01580. (617)366-2900.

February 25-March 1
Systems Analysis and Design Workshop. San Francisco, CA. Contact: Pam Kerwin, Institute for Advanced Technology, 6003 Executive Blvd., Rockville, MD 20852. (301)468-8424.

February 26-28
Automated Design and Engineering for Electronics. Anaheim, CA. Contact: Cahners Exposition Group, PO Box 5060, Des Plaines, IL 60018. (312)299-9311.

March 6-8
DEXPO Europe '85. London, England. Contact: Expoconsul International, Inc., 55 Princeton-Hightstown Rd., Princeton Junction, NJ 08550. (609)799-1661.

March 11-15
Data Communications Systems and Networks. Washington, D.C. Contact: The George Washington University, Continuing Engineering Education, Washington, D.C. 20052. (202)676-8521.

March 18-29
Comtel '85. Dallas, TX. Contact: International Computer and Telecommunications Conference, 13740 Midway Rd., Suite 600, Dallas, TX 75244. (214)458-7011.

March 24-29
Simulators Conference. Williamsburg, VA. Contact: Charles A. Pratt, Executive Director, SCAS, PO Box 2228, La Jolla, CA 92038. (619)459-3888.

March 26-28
Comdex in Japan '85. Tokyo, Japan. Contact: The Interface Group, 300 First Ave., Needham, MA 02194. (617)449-6600.

March 27-29
IEEE Built-in Self-Test Workshop. Charleston, SC. Contact: BIST Workshop Chairman, BITE, Inc., Penn Plaza Office Complex, 120 Pennsylvania Ave., Oreland, PA 19075. (215)576-5650.

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