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DIGITAL DESIGN

SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS NOVEMBER 15, 1984

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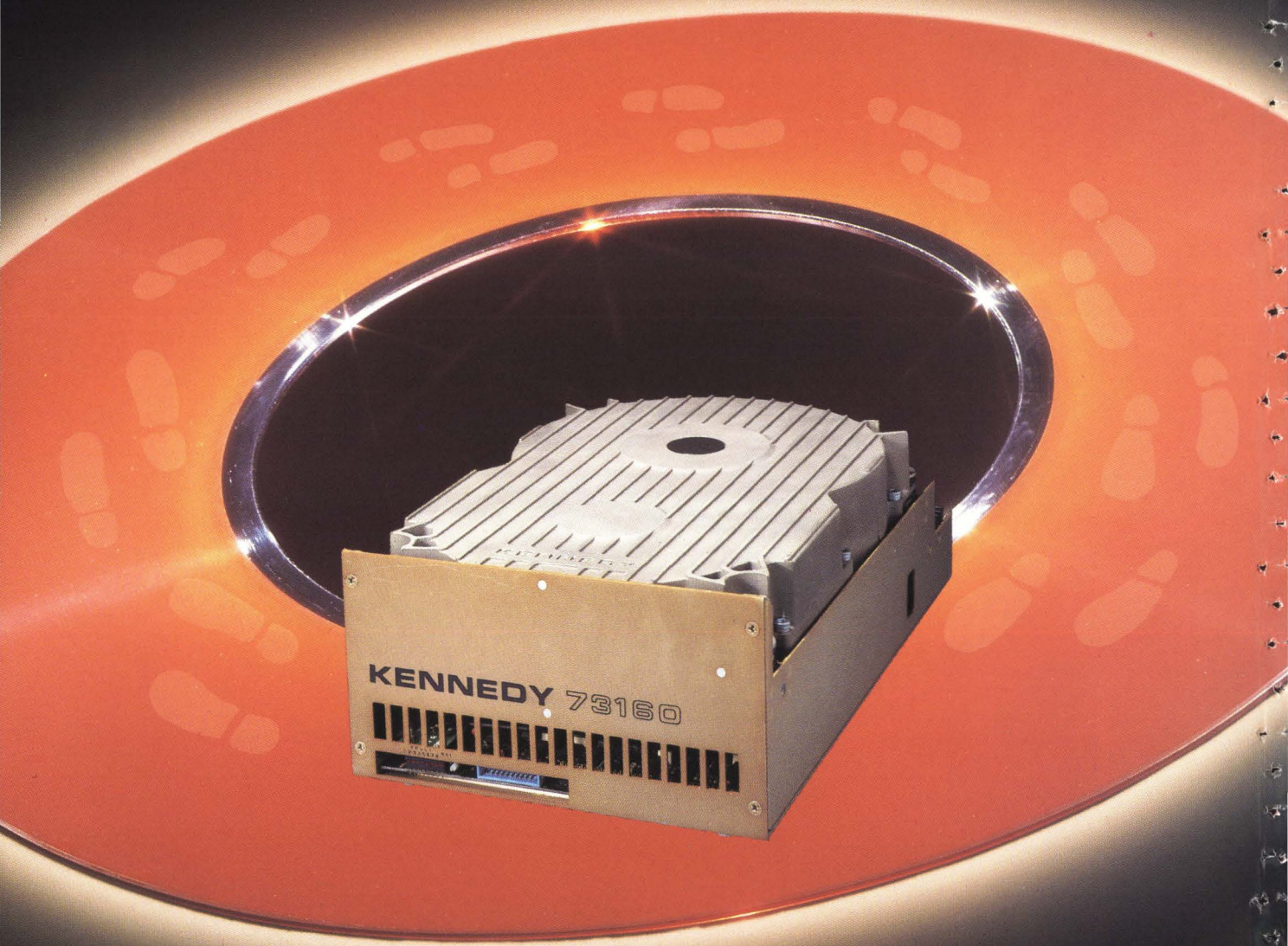

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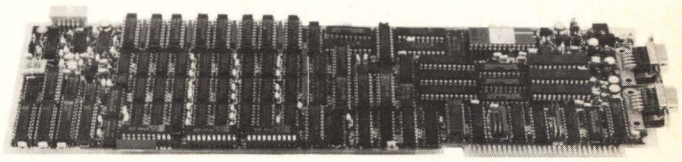

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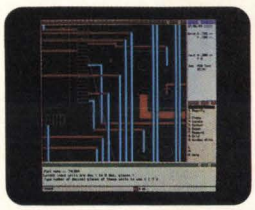
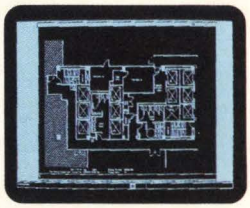
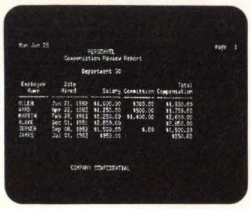


Printed circuit board layout.

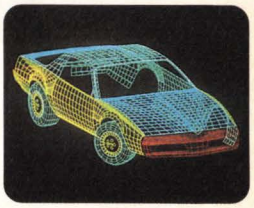


Space plan of a facility.

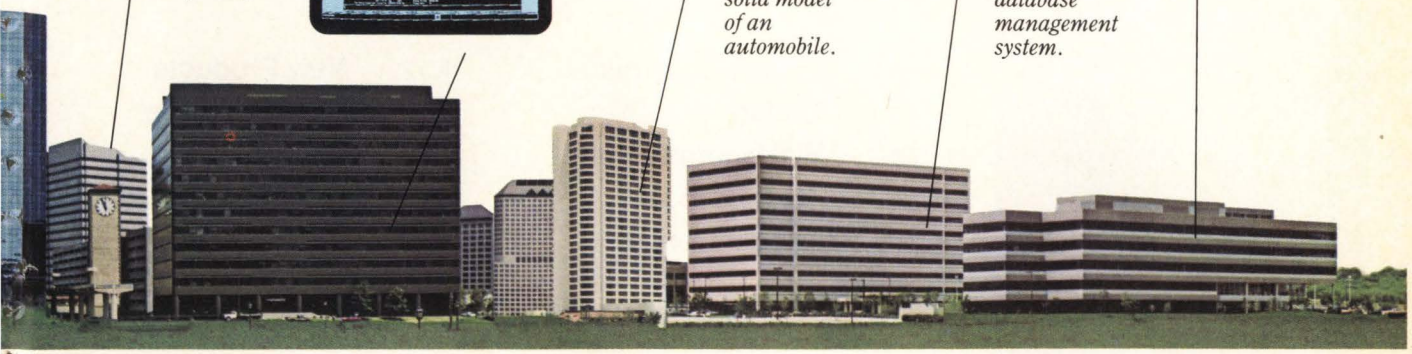
Exploded solid model of an automobile.



Relational database management system.



3D surface model.



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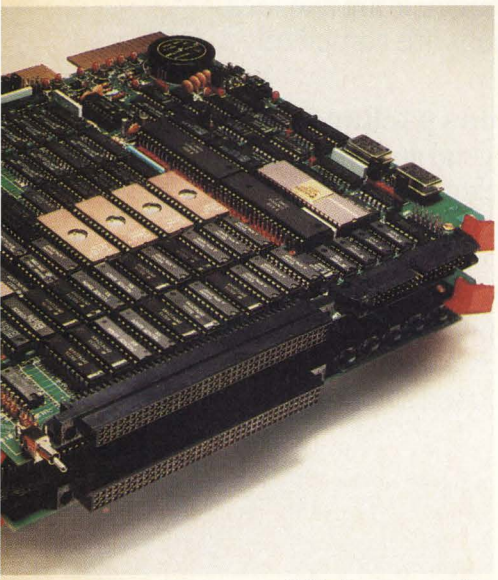

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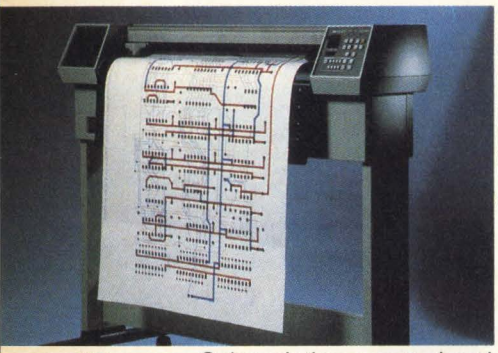

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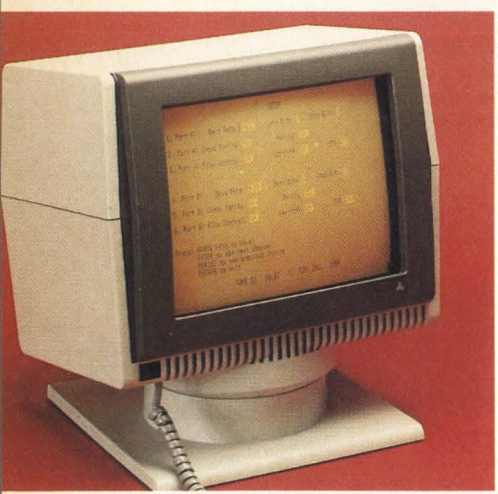

COURTESY FALCO

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DEPARTMENTS

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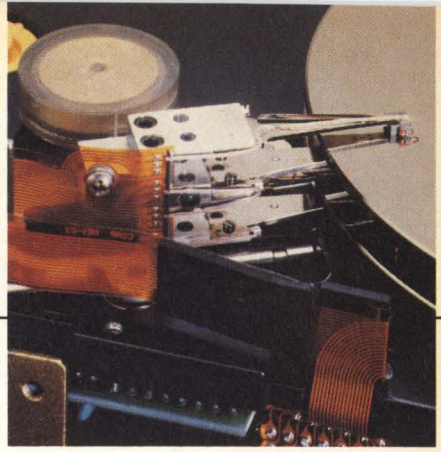

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FEATURES

ON THE COVER

Scaling down technology developed by IBM for their large, 3380 Winchester disk drives, today's small disk drives are beginning to incorporate low-mass Whitney flexures. The stiff, lightweight read/write head assemblies provide improved flying stability and increased resistance to shock and vibration. Photo courtesy Seagate Technology.

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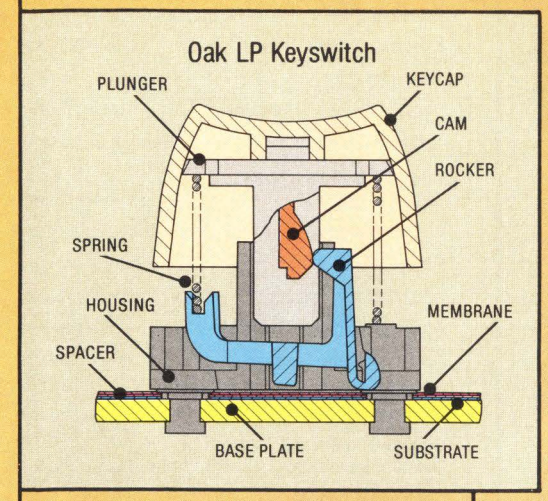

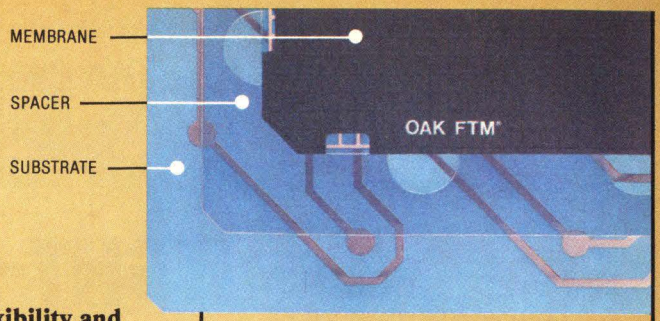

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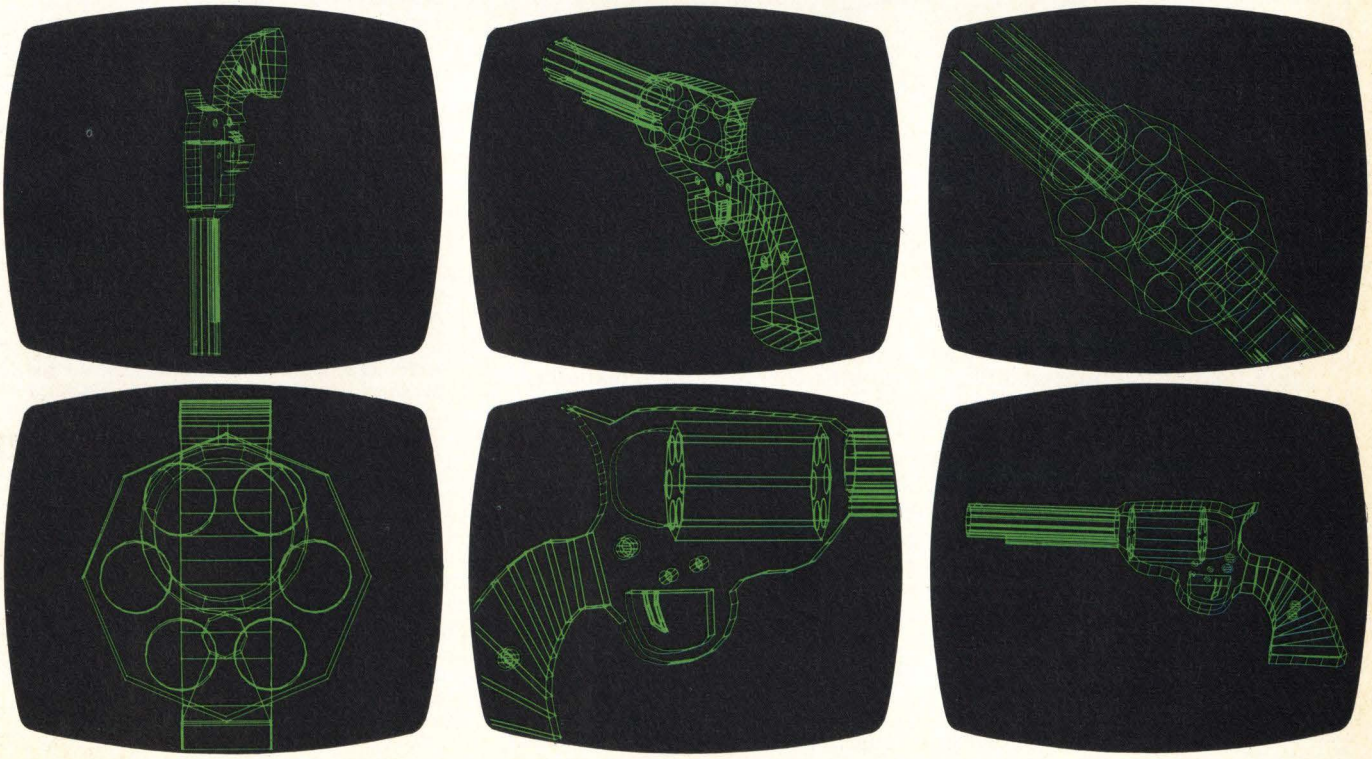

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SOLVING THE MYSTERY OF THE BLUE SKY PHENOMENON.

This is the 2nd in a series of technical papers from Zilog, designed to give engineers new insights into Zilog microprocessors—what advantages they provide for particular products and why they are the choice among engineers who need optimum performance.

In the microprocessor world, the "Blue Sky Phenomenon" refers to microprocessor development code crashes. The code simply and quite mysteriously disappears. The most common culprits are bugs. And the fact is, simple program bugs will crash most microcomputers.

The hosts for some of these bugs have famous names. What they all have in common is an absence of mechanism to protect against crashes. There is one exception.

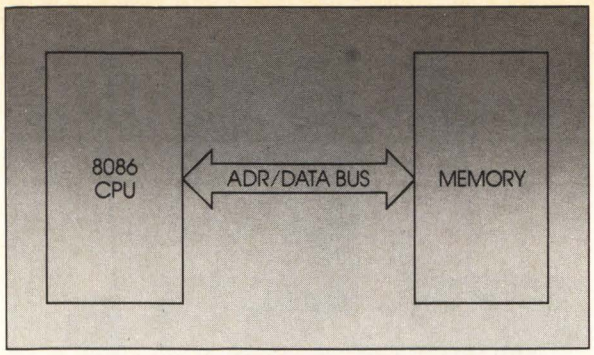
The Zilog Z8000® family provides comprehensive hardware protection to help create systems that are resistant to system crashes so common in primitive architectures. The Z8000 CPU is not only more reliable in this sense, but it's easier to learn how to use. Especially if you already know how to use the ubiquitous Z80® CPU.

LOST IN THE WILD BLUE YONDER.

There is a technological reason why some microprocessors are so prone to corruption. It stems from the direct connection of the memory to the processor. Without any checking hardware between the processor and memory, the processor can change any area in its memory at will—without regard to the consequences. Such a lack of restrictions allows illegal operations such as changing program memory stack underflow (running the stack into the data area), and even modifying the code of the operating system. This lack of appropriate technology has two glaring results:

- Illegal operations cannot be detected before damage has occurred.
- Any damage to the program and data cannot be undone.

There are far-reaching implications for a lack of memory protection. Systems designed without it do not support multiple users, nor even UNIX™ very well. The simplest bug will crash the system. There is no protection and no recovery mechanism against even minor problems of access violations. The ability to handle more than one user is usually not allowed, or is strongly discouraged.

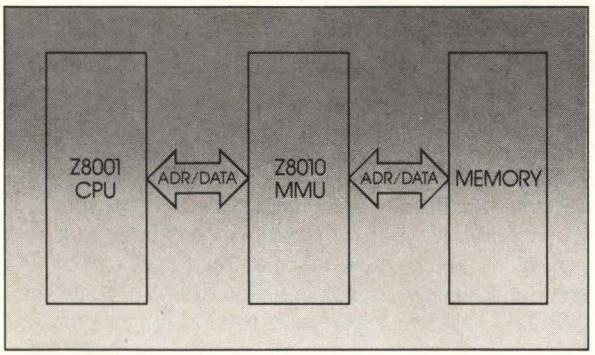


A typical Intel 8086-to-8088 configuration, the lack of memory checking hardware—the memory to the processor. The processor can change any area in its memory at will, without regard to the consequences. The result: illegal operations cannot be detected before damage has occurred; and any damage to the program and data cannot be undone.

THE Z8000 CPU—THE FULL-PROTECTION MICROPROCESSOR.

Zilog's Z8000 CPU solves these problems by inserting a chip called the Z8010 MMU (memory management unit; available in paged or segmented versions) between the processor and memory. This chip normally passes addresses from the processor to the memories—checking each memory access for its address and type of operation as it occurs. If the MMU chip detects an illegal operation, or the use of an unauthorized address, it suppresses the illegal operation and interrupts the program. It passes control to the operating system. Once the program is stopped, the operating system can inspect, correct, or abort the program that caused the error. All with no wait states.

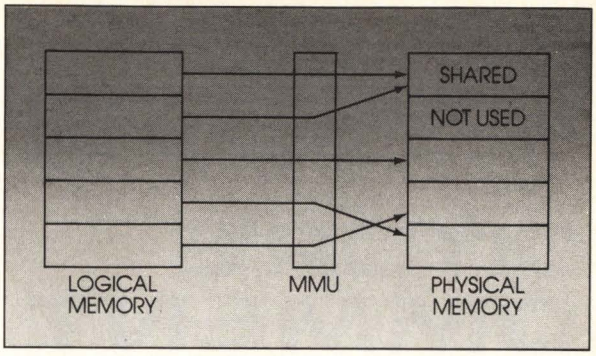
A system constructed with the Zilog MMU can allow many different programs to run without the fear that one program could entirely stop the rest or even corrupt the rest. But, the memory management hardware goes beyond providing protection. It also simplifies system implementation.



Zilog's configuration system prevents the Blue Sky Phenomenon by inserting a chip called the Z8010 Memory Management unit between the processor and memory.

HIGH LEVEL LANGUAGES REQUIRE MEMORY MANAGEMENT.

One of the strengths of 16-bit microprocessors—and the Z8000 CPU in particular—is that they support high level languages such as C, PASCAL and FORTH. A goal of most users is to allow more than one of these high-level language programs to execute in the processor at the same time (multi-user/multi-tasking)—gaining more effective utilization of the computer. The challenge is to provide an architecture that allows a language compiler to produce code targeted to run at one address, but allows the actual placement at a different physical address. This mapping is known as logical to physical translation—a feature of the Z8010 MMU.



Zilog satisfies the common requirement for systems to share information with our MMU. The logical-to-physical translation capability allows more than one logical area to access a common physical area.

SHARED MEMORY IN THE Z8000 CPU.

Another common requirement for systems is the need to share information. With Zilog's Z8010 MMU, the logical-to-physical translation capability allows more than one logical area to access a common physical area. When combined with the protection capabilities of the Zilog MMU, you can set up areas that can be common read-only while the same physical area could be read AND write when accessed under different conditions (operating system access).

For example, you could construct a process control system that posts status information into a common area. The central core of the system is allowed to read and write this common area. Application programs that need access to this information can read it through a totally different segment that is translated into the proper physical address—but with the provision that all access must be reads, not writes. If an application program were to run wild and attempt to corrupt the common area by writing into the read-only space, it would be intercepted before any write could occur.

The key benefit to using Zilog's MMU to implement shared memory is its flexibility to make multiple logical segments access a common physical area with all of the protection—or lack of protection—desired. All with no overhead per access. What's more, Zilog's MMU and other Z8000 devices are available from a host of reliable second sources.

Solving the problem of the "Blue Sky Phenomenon" is only one of the technological hallmarks of the Z8000 CPU. Others will be discussed in this continuing series of technical papers from Zilog, Pioneers of the Microworld. For details on the Z8000 CPU, call our Literature Hot Line at 800-272-6560.* Or write: Zilog, Inc., Technical Publications, 1315 Dell Avenue, MS C2-6, Campbell, CA 95008.
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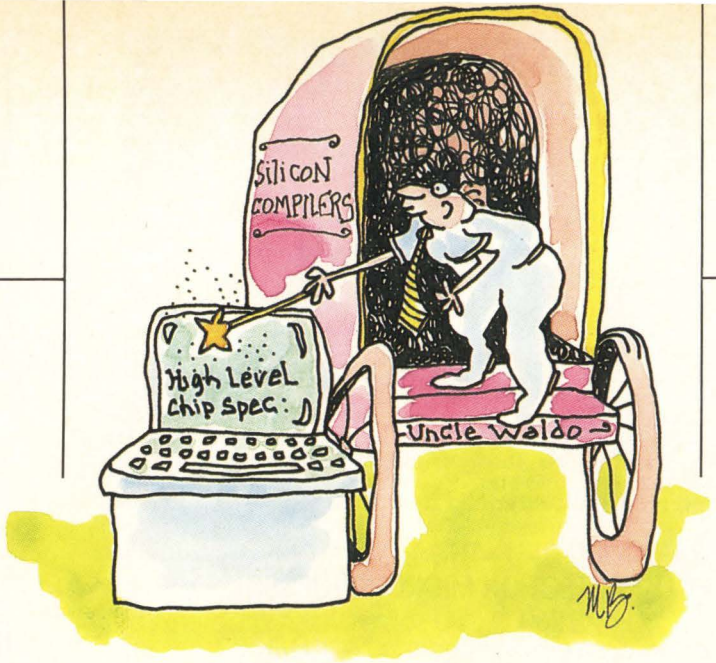
'sil·i·con com·pil·er, *n.* **1.** nebulous term used to describe a system that automatically synthesizes integrated circuits. **2.** a term primarily used for marketing hype.'

EDITOR'S COMMENT



The term silicon compiler is a new phrase that will soon become part of the electronic-jargon dictionary. But what is the new super-cala-fragilistic design tool? If I'm correct, this question will continue to be answered differently without a clear definition. At the present time, if you ask nine silicon compiler experts, "So what is a silicon compiler, anyway?" you'll probably get 17 different answers. Let it suffice, for the moment, that a silicon compiler does the "grunt" work of designing an IC, i.e., implementing the gates and transistors. The designer provides the compiler with a high level description of the chip's various functions and the compiler then automatically synthesizes the logic.

Seems like a fairly straightforward description, so what's all the fuss about? Well, unfortunately, in all likelihood a multiplicity of CAD/CAE vendors will shortly introduce this sort of design tool and each will use the term: silicon compiler. However, silicon compiler is just a name, it does nothing to distinguish its capabilities. As a result, it is more than probable that a silicon compiler from one manufacturer will be much different, in terms of sophistication, from that of another manufacturer. Yet both will have the same generic title.

An analogous situation would be choosing between two methods of transportation: either a camel or a car. The camel salesman tells the naive buyer not to invest in a car because the camel can perform the same transportation function as the car, and on top of that, the camel need be refueled only once per week. Of course most people would know the difference between a car and a camel, but can the same be said for a silicon compiler?

The implications to the potential buyer reflect that the manufacturers of so-called silicon compilers must clearly highlight the level of sophistication of their wares. By clearly specifying the extent to which the system architect is removed from designing the functions, vendors will be doing a great service to the potential user.

The ideal silicon compiler, which probably won't arrive for quite a few years, would design a chip by simply telling it (via voice recognition, of course) a few of the chip's general specifications. With this kind of IC design tool, the design engineer will be completely removed from the architectural tradeoffs of designing an IC. Future silicon compilers will be tightly integrated with expert systems that will automatically optimize both the architecture and layout of an IC.

As far as the capabilities of today's silicon compilers are concerned, for the most part, they do not allow designers to divorce themselves from decisions about architectural considerations. The designer must have a preconceived notion of how the IC's functions are to be implemented. The various functions are then called up and compiled.

Don't misunderstand, I'm not belittling today's silicon compilers, I'm just pointing out that there must be a way to differentiate one compiler from another by measuring the extent that the designer is removed from the actual design. Using our futuristic silicon compiler as an example, this wonderous widget would be the most sophisticated of all compilers.

At the other end of the spectrum lies parameterized cells which allow the designer to build a customized function. Take a simple register, for example: the designer would specify such parameters as set-up and hold time, number of bits, drive capability, etc. So instead of calling upon a register from an existing library (as with a gate array or standard cell IC), the designer can build a customized register tailored to a particular set of requirements. Yet these parameterized cells might hide under the guise of silicon compiler — which connotes a higher level of sophistication.

The ideal silicon compiler is still very far into the future, but as interim compilers are introduced, there must be a scheme to categorize the more advanced compilers from those that are just given the name silicon compiler. There is a strong possibility that a great majority of the so called silicon compilers, soon to hit the market, will be no more than parameterized cells.

One solution to removing the confusion of this new jargon might be to divide silicon compilers into two distinct categories: (1) garden variety silicon compilers (2) real silicon compilers. This would remove the confusion before it even becomes an issue.

Much of the marketing strategy will undoubtedly be similar to "Uncle Waldo's Magical Elixir: Guaranteed to design anything." Of course this is somewhat of an exaggeration, but I remember the first time a workstation and its salesman were put before my eyes and he extolled its virtues, but forgot to mention that this engineering marvel could not transfer files to a VAX, or any other host for that matter. Although silicon compilers will some day make IC design as easy as discharging a capacitor, BEWARE of the term silicon compiler!

Ron Collett, Technical Editor

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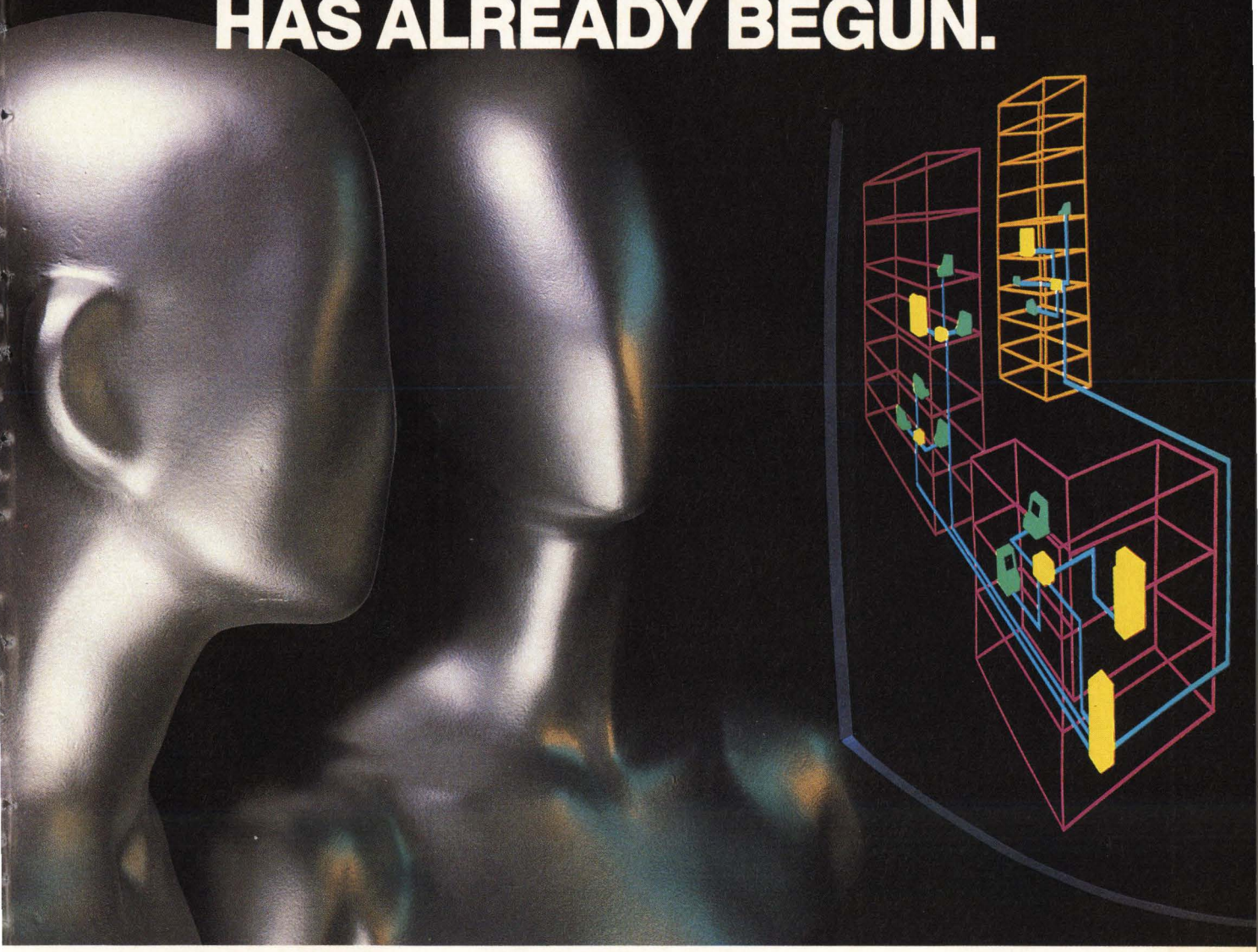

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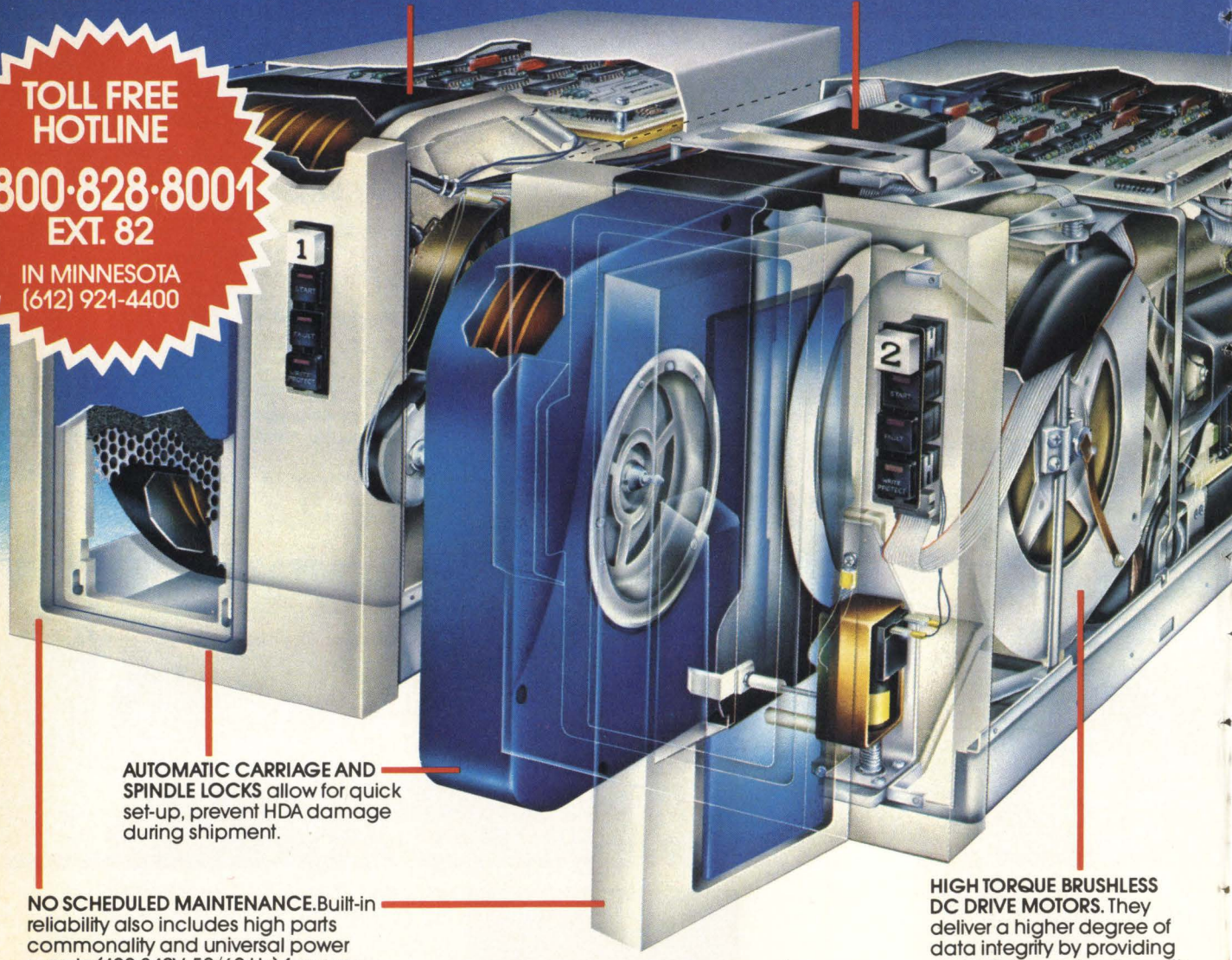

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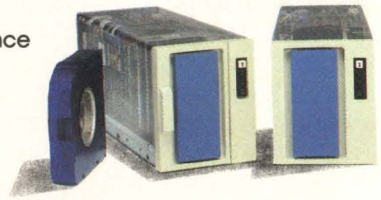

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UPDATE

Intel Supports IBM's SOEMI

Intel Corp. will support IBM's Serial OEM Interface (SOEMI). The SOEMI feature can provide an interface on the IBM 4361 family of mainframe processors allowing for the attachment of OEM systems and devices. In the first half of 1985, Intel intends to announce a Multibus-based (IEEE 796) board-level product to support the IBM 4361 processor-attachment capability.

Harris Plans UNIX Implementation

The Computer Systems Div. of Harris Corp. will implement the UNIX operating system on its line of virtual memory super-minicomputers. The development program calls for an interactive, multi-user environment combining the high performance features of Harris VOS virtual operating system and the functionality of UNIX System V. The UNIX shell and all necessary support software will be implemented on top of the VOS kernel.

Floating Point Systems, Honeywell Interface

Floating Point Systems, Inc. and Honeywell Information Systems will market a hardware and software interface that links the FPS-164 Scientific Computer and Honeywell's DPS 8/C large-scale computer systems operating under CP-6. The interface will be available in the fourth quarter in System Job Executive (SJE) or in Apex mode. The System Job Executive mode supports complete processing on the FPS-164 while the Apex mode supports execution of CP-6 subroutines on the FPS-164.

Distribution Rights In Japan

Shoko Co. Ltd. has granted exclusive distribution rights in Japan to Denelcor, Inc. and concurrently ordered one Denelcor HEP H-1000 Process Execution Module (PEM) computer system. The system will be installed in the fourth quarter 1984 and will be used for customer demonstration and development of image processing, CAD/CAE, molecular modeling and other application software for science and industry.

Fujitsu, Ridge Agreement

Fujitsu America, Inc. signed a $20 million contract with Ridge Computers, a manufacturer of 32-bit mainframe computers, to market its high-performance 8″ and 10½″ disk drives. The three-year contract involves the M2312, an 8″ 84 Mbyte drive, the M2322, an 8″ 168 Mbyte drive; and the M2351 Eagle, a 10.5″ drive with storage capacity of 474 Mbytes.

China Orders Computers

Gould Inc. received a $5.8 million order from the People's Republic of China for 11 Gould computer systems, related software, spare parts and special training. The systems will be used at 11 universities in China for software development and academic studies. As part of the contract, Gould will provide special training for 44 students who are professors from the Chinese universities.

Celerity Receives Second Round Financing

Celerity Computing, a manufacturer of engineering workstations, received $8.5 million in second round of equity financing. In September 1983 they received a $4.4 million first infusion of equity financing. The funds are being used for continuing development, initial marketing and production of its C1200 Professional Workstation.

Supermini Integration

Canaan Computer Corp. signed a $3 million OEM agreement with VG Systems, Inc. to supply its superminicomputer for VG's System 9000. The system is designed as a high-performance CAD/CAM/CAE workstation supporting CADAM application software in either a standalone or distributed environment.

DDC Facility Certified

The Defense Electronics Supply Center (DESC) notified ILC Data Device Corp. (DDC) that they are the first company to have its facilities certified under MIL-STD-1772. The MIL-STD-1772 requires hybrid manufacturing lines and process qualification methods to be audited according to a uniform code of procedures.

Linking Graphics

Sanders Associates will link high-resolution graphics workstations with Artel Communications Corp.'s 120 MHz Fiber Optic System. The system consists of two compact, self-powered transmit and receive modems, which allow the graphics controller and monitor/keyboard to communicate high resolution RS-343A video and bi-directional RS-232C digital data signals over a fiber optic cable. The system bandwidth accommodates up to 1280 × 1024 pixel resolution, 60 Hz non-interlaced refresh. Coaxial BNC input-output connectors are plug-compatible to most monitors and display generators.

Data General Offers CAD Tools

Four computer-aided software engineering packages from Softool Corp. will be available on Data General Corp.'s 32-bit Eclipse MV/Family systems. They are: Change Configuration Control (CCC) Environment; Programming Environment (PE); VAX-11 Fortran to DG Fortran 77 automatic conversion tool; and DG Fortran 5 to DG Fortran 77 automatic conversion tool.

Memorex's Disks Qualified

Memorex Corp. has been qualified as a supplier of 3.3 Mbyte 5¼″ flexible disks by Drivetec, Inc., a flexible disk drive manufacturer. They plan to use the flexible disks in its super minifloppy disk drive. Shipment of the flexible disks have begun with full scale production and volume deliveries are scheduled for the fourth quarter of the year.

Nibble Mode 64K Military DRAM

Inmos Corp. announced the availability of the IMS2600M, a nibble mode 64K × 1 Military Dynamic RAM. Manufactured in sub 2μ NMOS technology, it is designed for high end performance exhibiting RAS access times of 120 nsec and 150 nsec with cycle times of 190 nsec and 230 nsec respectively. This is the only Military DRAM offering both nibble mode and CAS-before-RAS refresh features. The nibble mode feature allows sequential access of four bits at a data rate of 65 nsec.

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WASHINGTON REPORT

by Anne A. Armstrong

DLA Questions Testing Of TI Chips

The Defense Logistics Agency stunned a host of defense contractors in early fall with the news that it was suspending acceptance of any systems containing Texas Instruments' chips which DLA says may have been improperly tested. The magnitude of the problem became clear as DLA, TI and the contractors began trying to sort out which chips were involved; what contractors had put them in which weapons systems; and what, if any, tests were improperly carried out.

In the days immediately following the suspension, neither TI nor DLA were able to identify all the part numbers involved, the names of all the contractors to whom the parts had been shipped, or even ball park figures on the total number of parts involved. Some 15 million were delivered to IBM alone.

The first hint of a problem came in May 1983 when inspectors from IBM's Federal Systems Division toured the TI plant in Taiwan. Some testing irregularities were reported and IBM and TI began trying to resolve the problems. In January of 1984, IBM reported to DLA that it had been unable to settle its questions about the testing of the chips. IBM also began testing TI chips itself.

DLA officials will not say what information finally prompted them to refuse shipments containing TI chips, but some sources say the action was connected to the news that it was a TI chip that failed in the shuttle Discovery's onboard IBM computer. Texas Instruments denies the connection and says the moisture on the shuttle chip which caused the corrosion was introduced after manufacture and that the shuttle chip was not among those whose testing has been questioned.

TI's best estimates show that 4700 chips described as source specification control devices may have been improperly tested. Some 80 defense contractors are mentioned as receiving the parts, but DLA director of public affairs John Goldsmith told *Digital Design* that figure is misleading. If the many different divisions of a company are counted, like General Dynamics, the total is closer to 200 contractors, he said.

At press time, TI was in the midst of a massive review of all the testing paperwork and was trying to determine exactly which parts had been adequately tested and which had not. TI officials emphasize that although the testing procedure has been questioned, no failures of weapon systems due to chip failure have been reported. TI has also issued, at the request of DLA, an urgent data request to all contractors. The message asks for any information about failures in systems containing the questionable chips.

Early indications from the review process show that 90% of the chips in question were properly tested, according to TI spokesman Norman Neureiter. The extensive review will take weeks to complete, he said. Cost estimates for the review have not been made, but DOD officials say that all involved are keeping track of money spent and negotiations on payment will come later.

National Gets Clean Slate From DLA

In the meantime, National Semiconductor and the Defense Logistics Agency resolved the final issue stemming from another chip testing case. In March 1984, National pled guilty to a 40-count indictment that grew out of its admitted failure to fully test some microcircuit devices between 1978 and 1981. As a result of that action, the company paid a fine of $247,000 and paid the government $1,510,000 in compensation for the undertesting.

DLA, however, wanted National to provide the names of specific individuals who were responsible for the improper testing and National, while accepting corporate responsibility, would not name individuals. DLA then began proceedings to bar National from competing for any Defense contracts.

As part of the settlement, DLA has dropped the debarment proceedings and restored the company to full contracting eligibility. National agreed to pay $373,200 to cover DLA's administrative and investigative costs and to withdraw a lawsuit it had filed challenging the propriety of DLA's move against the company.

The biggest stumbling block – National's unwillingness to provide individual names to DLA – was resolved when the parties agreed that employees could voluntarily describe their own responsibility under a court order assuring confidentiality.

"For several months the company was unable to reconcile the legitimate demands of the government for information about the circumstances that led to the undertesting, with the company's strong commitment to those employees who were involved in an industry pattern beyond any one individual's responsibility," said Charles E. Sporck, President and Chief Executive Officer of National. "We are gratified that the proceeding that has been developed is a fair way to meet both concerns and at the same time removes any cloud from National's position as a leading military supplier."

Sporck emphasized that throughout the dispute, no military equipment failures were ever attributed to National parts and that special retesting conducted during 1982 confirmed their reliability. He also pledged that no such incidents would occur again at the company.

Military and aerospace sales represent approximately five percent of National's business, which in fiscal year 1984 (ending May 31) posted sales of $1.66 billion.

Martin Leaving DOD For Boeing

Edith Martin, Deputy Undersecretary of Defense for Research and Technology, resigned in October to take a job with Boeing Aerospace Co. as vice president of technology assessment. Martin was in charge of the DOD's VHSIC program.

Commerce Changes Export Rules — Again

In what is turning out to be a constantly changing proposal, the Department of Commerce has responded to a storm of protest from the industry over its attempts to police exports of high tech equipment. Under the latest proposed revision of the export licensing rules, Commerce would essentially let the industry monitor itself. Commerce would approve an exporter's internal procedures for monitoring shipment under its distribution licenses, and if the company's controls are working properly, they would be allowed to ship under the distribution license. Some restrictions and regulations have still been placed on powerful computers and specialized high-tech equipment, but generally the new proposals would relax the rules considerably.

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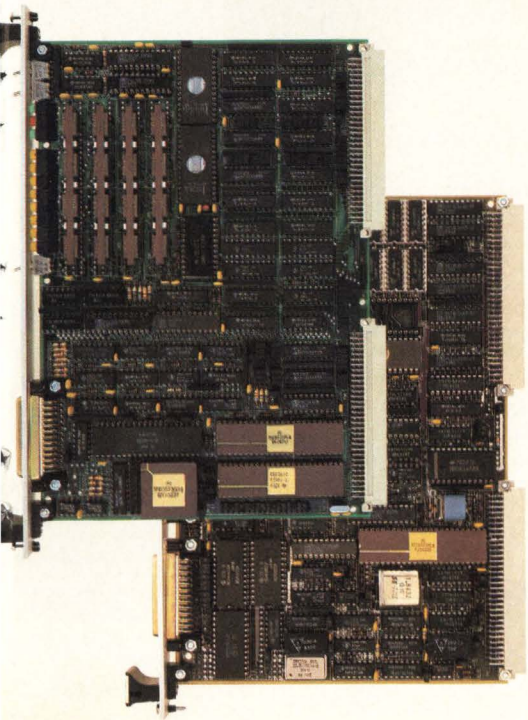

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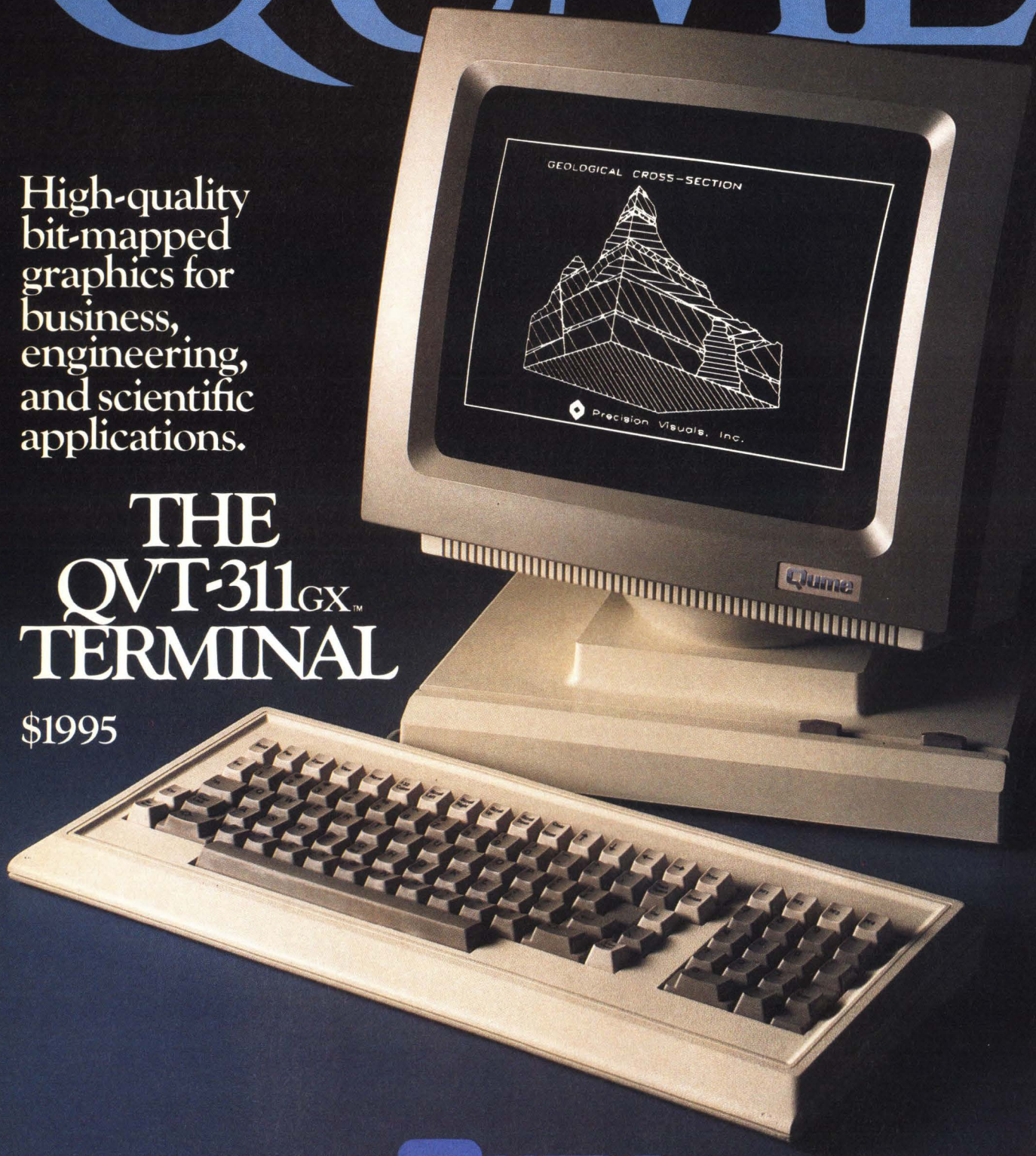

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Data Rate:	50-19.2 K baud
Communications Interface:	RS-232C
Transmission Mode:	Half duplex/full duplex/asymmetric asynchronous

Display

Medium:	Snow white phosper
Screen Size:	14 inches
Screen Surface:	Non-glare
Refresh Rate:	50 Hz or 60 Hz, non-interlaced

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Detachable, low-profile, with telephone type modular connector. Optionally available in multiple languages.

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Addressibility:	
VT 125 Mode:	800 x 600 points
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Tek 4014 Mode:	4096 x 4096 points
QVT 311 (native) Mode:	800 x 560 points
Resolution:	640 x 480 pixels (visible)
Line Types:	Solid, dashed (various types)
Graphic Command:	PLOT 10 compatible and ReGIS command set compatible
Graphic Primitives:	Vectors, panels, polygons, text and markets
Two Full Graphics Planes:	4 shades of gray

Alphanumeric Mode

Character Set:	X3.64—1979 for seven bit character set or X3.41—1977 (ASCII) for eight-bit character set
Character Format:	7 X 9 dot matrix in 8 X 14 dot character cell. 34 rows by 80 columns, the 33rd and 34th rows are the status/set-up/user-programmable lines

Auxiliary Port

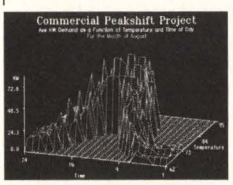
Compatible with:	Digital LA 30 and Epson FX80 or MX80

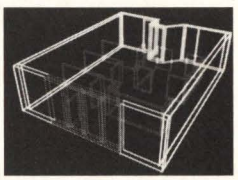
AC Power

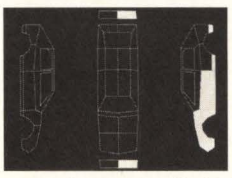
Line voltage:	90 to 135 VAC or 180 to 270 VAC
Line frequency:	50 to 60 Hz with ±3% variation

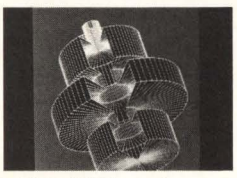
Physical Characteristics

Dimension	Display	Keyboard
Width	14½″	18″
Height	16″	1½″ with two-step height adjustment
Depth	14½″	8″









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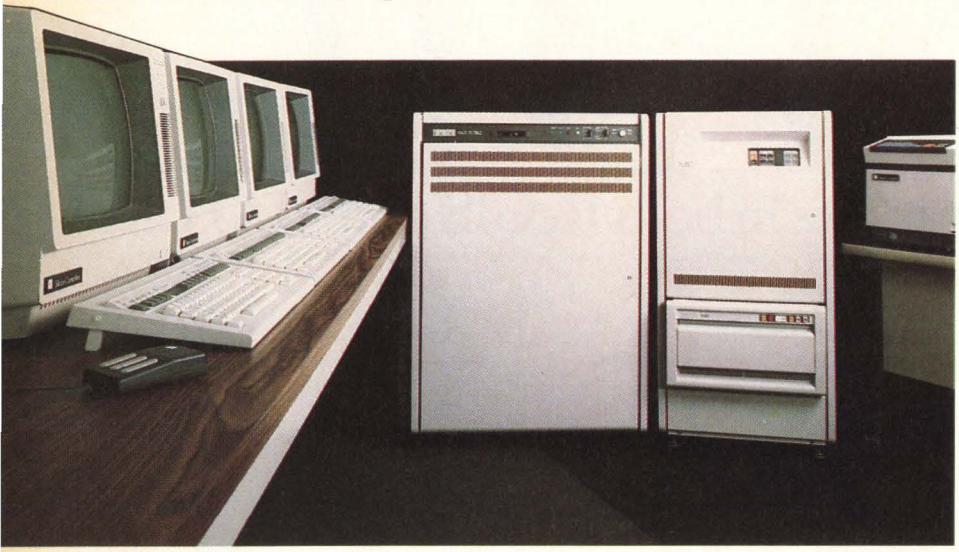

The Genesil Silicon Development System is made up of a VAX 11/750-based turnkey system running under UNIX, supporting up to four users and offering user I/O options.

In the world of VLSI design, the term silicon compilation has been tossed around for several years. Although there is no clear-cut definition of a silicon compiler, it is generally construed to be a CAD/CAE system that synthesizes ICs via a high level description from the system architect. The aim of these sophisticated systems is to provide the designer with a tool that drastically simplifies chip design. By removing the designer from tedious logic design tasks, and allowing him to focus on architectural considerations, there is a greater opportunity to exploit architectural creativity. (For a complete explanation of silicon compilation, see *Digital Design*, August 1984).

Silicon Compilers Inc. (SCI, Los Gatos, CA) have been promoting their recently introduced silicon compiler for the past eight months. On the other side of the fence, however, Valid Logic (San Jose, CA) have been silent in their silicon compilation efforts – until now.

SCI's new Genesil I sells for $545,000 while Valid's Concorde-I costs from $100,000 to $150,000. It is still too early to make effective evaluations of the two systems since users have yet to experiment. Concorde-I is actually only $25,000 to $75,000 if purchased without Valid's Scaldstar workstation, but it is necessary to have this host to run the silicon compiler.

Scaldstar software includes: the Scald Graphics Editor, timing verifier, logic simulator, packager, layout editor, design rule checker and electrical rule checker. Unlike Genesil which was designed by SCI, Concorde-I was developed by Seattle Silicon Technology, or SST, (Bellevue, WA), and then integrated into the Valid workstation. Valid is aiming to capitalize on their completely integrated self-contained workstation that includes everything necessary for VLSI design.

Concorde-I prompts the user to specify functional descriptions and parametric options, and the compiler generates the physical implementation of the function to the selected process design rule set. The resulting module can be automatically interconnected to I/O pads through the system's pad ring compiler, or it may be used as with other similarly constructed modules to build more complex functions.

Genesil, on the other hand, consists of a VAX 11/750, 450 Mbytes of Winchester disk storage, 4 Mbytes of semiconductor memory, a 1600 bit/inch drive and four color terminals (1024 × 780). System software includes packages for: block synthesis, place-and-route, functional simulation, timing analysis, design for testability and mask data generation.

A major difference between the two systems is that the Concorde-I can synthesize both analog and digital functions while Genesil is currently limited to digital applications. As far as process technologies are concerned, Genesil generates NMOS chips whereas Concorde I designs are implemented in CMOS. According to Valid, several ICs have been designed and synthesized with their system, including a raster chip. They also claim that SCI's compiler was used to design a similar raster chip and the functional difference between the two was negligible. Valid does, however, point out that since their design was implemented in CMOS, it was smaller, faster and uses much less power than SCI's NMOS design.

Designs generated by Genesil are hierarchically described: chip-set, chip, module and block. Blocks are the lowest level of objects in the hierarchy. Modules are made up of several blocks, chips are composed of modules which have pads, and chip-sets are collections of chips. At the outside of the design cycle, the design is typically a set of modules.

Six classifications of functions can be synthesized using Genesil: memory, complex logic, datapath, random logic, pads and test. The memory functions include RAMs, ROMs, FIFOs and Stacks; RAM functions can be either single, dual or triple ported. PLAs, decoders and encoders fall under the complex logic category.

The Datapath generator is one of the more sophisticated sections of the system since it yields parallel data processing operations that operate on datapaths from 4 to 32 bits wide. This section of the compiler is based on several sub-compilers that contribute to the synthesis of the whole data path. The ALU compiler provides 32 operations and the barrel shifter generator can synthesize a function that performs full-width data shifts in one clock cycle. The Interface compiler helps to manipulate data between several datapath blocks by providing multiplexers, inverters, shifters and latches.

Silicon compilers, such as those introduced from SCI and Valid, represent a new generation of IC design tools that aim to slash full-custom IC design cycles by as much as 75%. Smaller companies that traditionally have been unable to meet tight market windows because of the lengthy turn-around times of full custom

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ICs will likely be among the first to benefit.

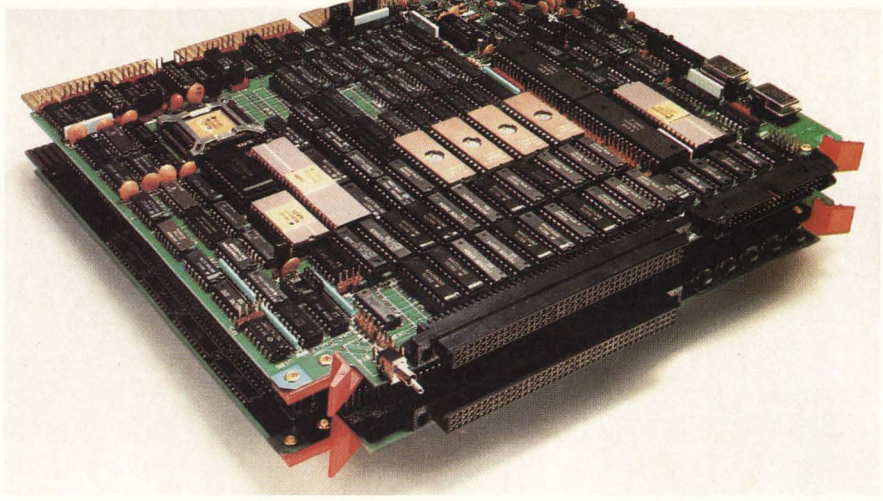
Although SCI and Valid are the first to make official product announcements, several other manufacturers will soon join in the competition. Among those that have made their efforts known, Metalogic (Cambridge, MA) and Silicon Design Labs (Basking Ridge, NJ) are likely to be the next vendors to offer a silicon compiler. —*Collett*

Valid **Write 231,** *SCI* **Write 232**

DEPARTMENTS/Systems

32-Bit UNIX System Coprocesses With PDP-11 On Q/Unibus

Figure 1: The AIS/3210 Supermicro system.



Designers of Q-bus and Unibus systems may now purchase an implementation of National's NS32032 microprocessor to give their users full use of 32-bit data processing, 24 bits (16 Mbytes) of uniform demand-paged virtual memory, up to 64-bit floating-point operations, and a multiuser UNIX-based operating system.

Developed by American Information Systems (Palo Alto, CA), the AIS/3210 SuperMicro System consists of a CPU board (AIS/3212) and from one to six memory boards (AIS/3218), which are inserted into the Q or Unibus backplane. Each memory card provides from 512 Kbytes to 4 Mbytes, depending on the configuration purchased, and the entire AIS System is interconnected by a proprietary backplane that allows high-speed data transfers of up to 32 Mbytes/sec. In addition, the Unibus version of the AIS/3210 contains from 512 Kbytes to 2 Mbytes of high-speed RAM directly on board.

Other features of the AIS/3210 include a RAMless Monitor with hardware autotest and maintenance support, a RAM monitor with symbolic debugger, four UART serial ports, automatic terminal baud-rate generation, and a time-of-day clock with battery backup. Although the UNIX-based operating system will support C language, compilers are also available for Fortran-77, Cobol-74, PL/1, Pascal, and Basic.

For Q-bus systems, AIS offers both a "Bus-Master" and an "Enhancement" version of the 3210 with a UNIX-based operating system (Bell Lab's System V and Microsoft's XENIX-32K). The difference is that the Bus-Master (AIS/3210-A) replaces the Q-bus processor (LSI-11 or PDP-11) as the primary CPU, and the Enhancement System (AIS/3210-AE) supplements the primary CPU (LSI-11, PDP-11, or AIS/3210-A) as a peripheral processor. For Unibus systems, only the Enhancement version is available (AIS/3210-BE). Plans to port the basic design to other bus structures – including micros, minis, and mainframes are now being completed.

According to Mark Ursino, President of Technology Services Corp. (Bellevue, WA) it would normally be a difficult task to transport operating software from one computer design to another, since its I/O implementation is extremely hardware-dependent. AIS has developed an approach, however, that requires very little reworking when adapting an operating system to another host machine. Essentially, they have devised specialized software – called VIO (Virtual I/O System) – that contains a generalized I/O message protocol completely independent of the host operating system. In effect, all service calls are directed to "virtual" rather than real devices. Since all peripheral devices and interfaces are described on a higher level, they can be configured in any number of ways, and therefore are not tied to any particular host machine. As a result any software that is written for one AIS system is capable of being transported to any other AIS system with the same operating software, regardless of the host.

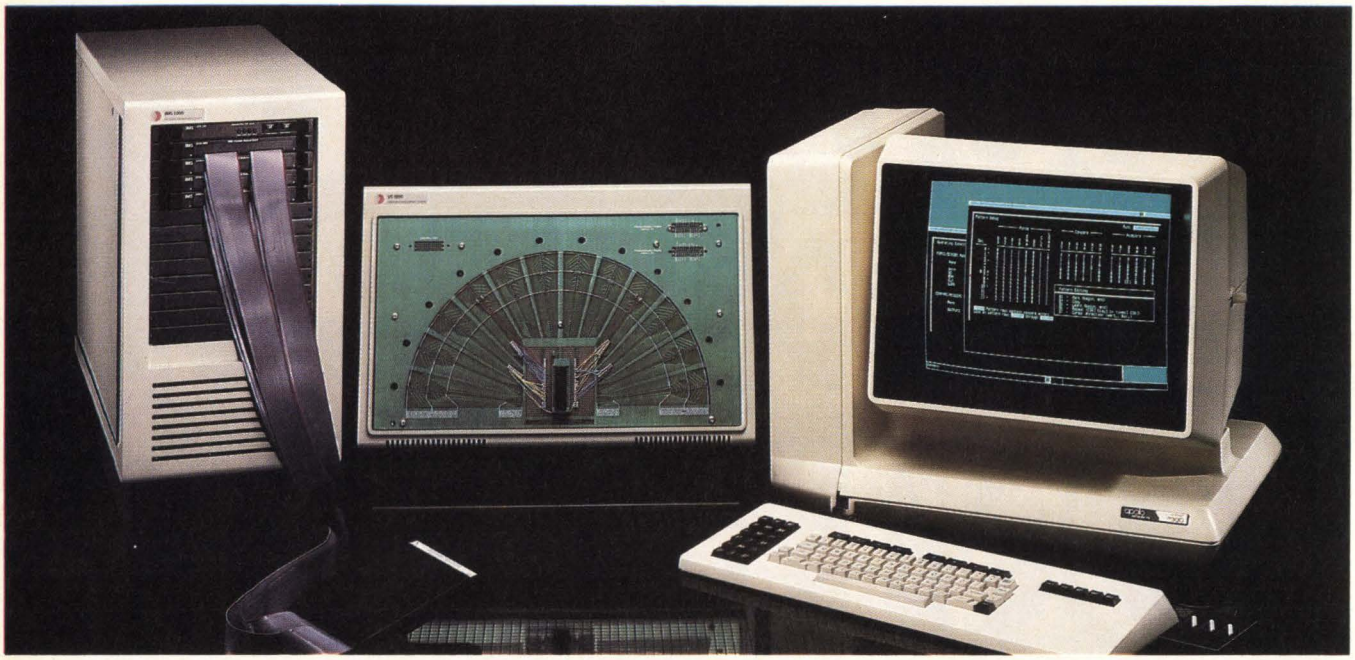
The benefit to the DEC user, of course, is that software written for the AIS/3210 can be operated on both a Q-bus and a Unibus system, provided the user has the UNIX-based AIS boards plugged into each system. According to Glenn Leedy, President of the company, AIS has also entered into an agreement with PICK System to port its highly popular relational data base operating system to the AIS/3210.

Write 241

SUDDENLY THE TAPE CONTROLLER IS OBSOLETE.

SPECTRA LOGIC

Engineering Workstations Find Missing Test Link



The Logic Master test system interfaces to both engineering workstations and computers. ICs can be functionally tested at speeds up to 40 MHz.

Engineering workstations have attempted to provide design solutions for all phases of the design cycle except one: prototype test. From schematic capture to logic verification, these CAD/CAE systems boost productivity and facilitate design. But when the first few ICs off the fab line are sent to the customer for verification, the workstation is useless. This void has set the stage for the development of systems that will provide test capabilities for the engineering workstation.

The first product introduced to meet prototype test needs comes from Integrated Measurement Systems, or IMS, (Beaverton, OR). Shown for the first time at Wescon last month, the Logic Master interfaces with virtually any computer system or workstation and provides functional verification of ICs. The most attractive attribute of the new system is its price, which ranges from $29,200 for the Logic Master I to $39,200 for the Logic Master II.

Until now, two relatively unappealing solutions were available to test prototype ICs. The first route entailed purchasing a full-blown automatic test equipment (ATE) system, like those used for high volume requirements. These systems, however, cost anywhere from $200,000 to one-million dollars. Even worse, there has been no compatibility between workstation generated test data and the ATE required data, so simulation vectors developed on a workstation could not be directly downloaded from the workstation to the ATE.

Designing a home-made test system using test instrumentation was the alternate solution. But this test path can usurp a significant amount of vital engineering time and may cost from $20,000 to $70,000 and in many instances, the test set-up will have to be completely revamped for subsequent test jobs.

In contrast, the Logic Master is programmable and designed to easily shift from one test job to another. By simulating the prototype IC, and acquiring the resulting output from the chip, Logic Master verifies whether the part functions properly. The system generates test vectors at 20 MHz but this can be increased to 40 MHz by decreasing the number of channels by one-half. This need only be done, however, on the particular channels that require higher speeds, which gives the user tremendous flexibility in tailoring the system. Both Logic Master systems (I and II) have 64 channels but can be easily upgraded to 192 channels. For larger I/O requirements, two systems can be coupled to provide 384 channels.

One of the more noteworthy features of Logic Master is its ability to branch to a diagnostic mode during a functional test routine – in real time. For example, suppose that a particular fault was only appearing when a unique set of conditions were applied to the chip. In other words, this situation would look like an intermittent problem. To solve this problem, Logic Master would provide the unique set of conditions and upon detection of the fault, would branch to a diagnostic routine to isolate the problem.

Logic Master interfaces with computer systems that have RS-232 or IEEE-488 or terminals (VT100 or ANSI 3.64) to receive and execute test commands and to report the results of test procedures. Of course workstations from vendors such as Daisy, Mentor, Valid Logic, Calma and most others can be readily linked to the Logic Master.

Daisy and Valid have also attempted to capitalize on this market by introducing simulators that allow the actual chip to be plugged-in into the simulator (Valid's Realchip and Daisy's PMX), but these systems are primarily geared towards simulating systems as opposed to testing chips. *–Collett*

Write 236

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	SPECTRA 15*/ SPECTRA 25	SPECTRA 111*/ SPECTRA 121	SPECTRA 12*/ SPECTRA 21
BUS	Q-BUS (Block-mode)	UNIBUS	UNIBUS
Disk Emulation	RM02/05, RM80, RP06 (2 drives)	RM02/05, RM80, RP06 (4 drives)	RK06/07 (4 drives)
Tape Emulation	TS11 (4 drives)	TS11 (4 drives)	TS11, TM11 (4, 8 drives)
Disk Transfer Rate (SMD)	2.0MB/sec	2.0MB/sec	2.0MB/sec
Configurable On-Line	Yes	Yes	No
*Single function disk controller			

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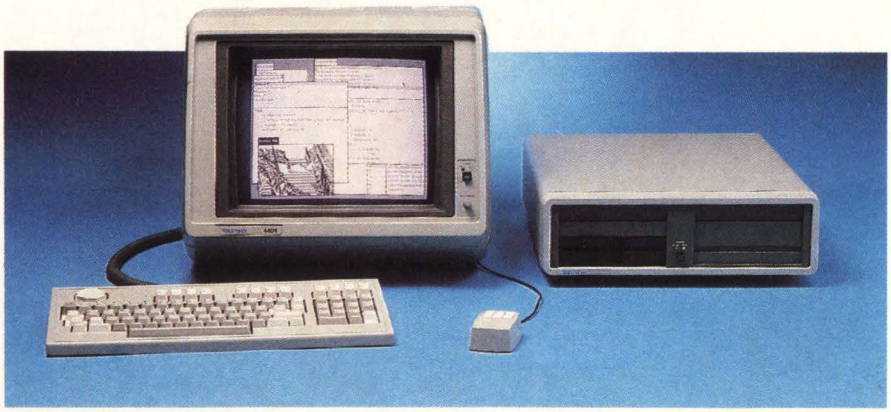
Tektronix Enters AI With Dedicated Workstation



The standard Tektronix 4404 Artificial Intelligence System, listed at $14,950 (U.S. only), features a monochrome bit-mapped display; keyboard; mouse; 32-bit microprocessor with virtual memory management; hardware floating point; 1 Mbyte RAM; and a 20-Mbyte hard disk with a single 5¼″ floppy disk. The system comes with the Smalltalk-80 (a trademark of Xerox Corporation) language, an interactive, graphics-oriented exploratory programming language.

Recently there has been a major surge of interest in AI, partly due to the Japanese dedicated push for the next generation computer. The fifth generation computer is intended to use non-von Neumann architectures that are capable of making inferences and decisions, associating, learning and procesing concepts and relationships. Instead of merely executing instructions quickly, the next generation of computers are designed to make decisions based on ambiguous facts, something that humans do matter of factly. This particular ability helps in image processing and recognition, robotics, and speech recognition. Expert systems that combine the facts from experts in a logical manner and allow a novice to reach the best conclusion through questioning, are becoming very powerful and useful. Ultimately, the next generation of computers is geared toward making computers more useful.

The creation of expert systems requires development tools that facilitate the process of AI program development. Many of these tools are dedicated Lisp machines that cost over $100,000. Tektronix (Beaverton, OR) makes an artificial intelligence system for under $15,000 called the 4404. The 4404 comes with the Smalltalk-80 programming language and operating environment. Franz Lisp and Prolog languages are available as options in addition to the Emacs visual text editor. The operating system is a multitasking operating system with a hierarchical file system. A C compiler is included with a standard library.

The basic hardware configuration includes a 10 MHz 68010 microprocessor with a floating point accelerator (IEEE standard format). One Mbyte of RAM (2 Mbyte is optional) is used for transient memory while a 40 Mbyte, 5¼″ hard disk and 320 Kbyte, 5¼″ floppy disk both provide storage. For very large programs which easily occur with AI, an additional 40 Mbyte hard disk is available as an option and includes a streaming tape backup system. Demand paged virtual memory support is provided up to 8 Mbytes of address space. This minimizes page swapping and omits the need for program segmentation and overlays. ROM and EPROM expansion sockets are available. Also included is a clock/calendar with battery backup. A three button mouse, in addition to a low profile keyboard, is used for data input.

The graphics capability of the 4404 is impressive. A monochrome display of 640 × 480 pixels is bit mapped at 60 Hz, noninterlaced. The display is a window of the 1024 × 1024 virtual graphics area, allowing smooth scrolling. Smalltalk, which is a very visual language using icons, symbols, and pop-up menus, takes advantage of the graphics capability of the 4404; screen refresh is fast enough for animation.

The 4404 is designed to provide AI programmers with a development system and environment that allows fluent program development of expert systems, natural languages, intelligent robotics, vision systems, automatic programming and theorum proving. After further development, the system will also accommodate end users.

Smalltalk was chosen as the host environment because it lends itself easily to AI applications. Developed at Xerox PARC, this extensible object oriented language was designed expressly for exploratory programming. Extensibility allows defining new instances of an object class, each with its own internal state, or defining new object classes with their own dinstinct set of rules. Smalltalk provides a class structure that allows multiple inheritance and hierarchical inheritance mechanisms with each new member inheriting aspects of its parent classes. This means new behaviors can be added to the characteristics of an object. In addition, classes can be used as a foundation of knowledge frames to organize complex information clearly.

Rapid prototyping and experimentation is implemented easily, allowing great interactivity. Smalltalk is object oriented, where objects are entities representing a collection of information and a description of how it can be manipulated. Tasks are accomplished by sending information between objects resulting in new information being returned or operations being performed. A unique quality to Smalltalk is that messages describe what should happen, not how. The implementation of operations are intrinsic to the definition of each object. Thus, the same message or information to different objects will not necessarily invoke the same response. Objects can then be progressively defined and used in a program without all operations being specified. Complex operations can be easily changed due to Smalltalk's ability to translate and relink changes. In contrast to conventional languages, objects in Smalltalk allow symbolic descriptions of problems with internal expressions that operate as rule processors.

The Tektronix 4404 is a low cost alternative for exploratory programming for research and development of artificial intelligence. — *MacNicol*

Write 242

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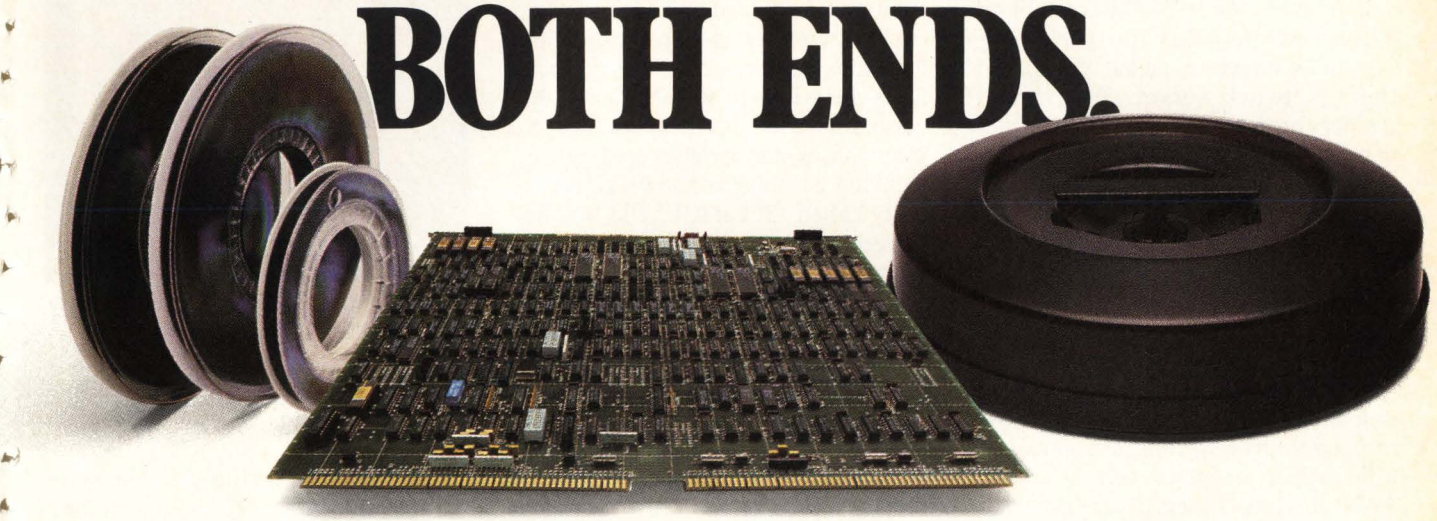

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BUS (Disk)	Burst Multiplexor Channel	Data Channel	Data Channel
Disk Emulation	60XX, 61XX (4 drives)	60XX, 61XX (4 drives)	606X (4 drives)
Tape Emulation (Data Channel)	6021, 6125	6021, 6125	6021
Operating Systems (without OS patches)	RDOS, AOS, AOS/VS	RDOS, AOS	RDOS
Disk Transfer Rate (SMD)	2.0MB/sec	2.0MB/sec	2.0MB/sec
Supports FCC Chassis	Yes	Yes	No
*Single function disk controller			

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Networking System Serves Both Local And Wide Area Networks

The Banyan Networking Server is a virtual networking device which combines previously incompatible local area networking (LAN) schemes with a wide area network in one system.

Banyan (Westboro, MA) has combined 32-bit hardware and a virtual networking system architecture, called Vines, into their Network Server. The virtual memory processor contains three Mbytes of memory and the system utilizes a six-slot I/O bus which supports four 43-Mbyte Winchester disk drives. It has floppy and tape cartridge storage, battery backup and storage expansion capability.

Most of today's networking schemes involve LANs for short distances and modems connected to dedicated digital telephone lines for longer distance communications. What has previously been missing from networking alternatives is a device that can interconnect the various LANs that link clusters of personal computers to each other and mainframes and groups of such networks.

The most popular architectures for LANs are the token-passing ring or bus and the carrier sense, multiple access/collision detection bus scheme. The Network Server is organized into a three-bus structure which incorporates a high speed memory bus, an IBM PC bus and a SCSI bus.

The Virtual Networking System consists of three major functional elements: front end, back end and services. The front end connects the server to multiple local area networks. The back end connects the server to various "host" processors and wide area networks. The services consist of proprietary applications, including a naming and addressing capability called "StreetTalk," file sharing, shared printing, mail and communications administration.

The IBM PC bus is located in the front end of the system and connects the local area networks. It operates at a cycle time of 1.6 msec, which is twice the speed of the bus when used in an IBM PC. Local network communications include a datagram protocol with built-in internetwork routing capability. As of now, the server supports Ethernet, Applebus, RS-422, Pronet and Omninet. Because it supports an asynchronous network, remote desktop computers can call into the server which has an auto answer capability. It also supports full Applebus hardware and software protocol.

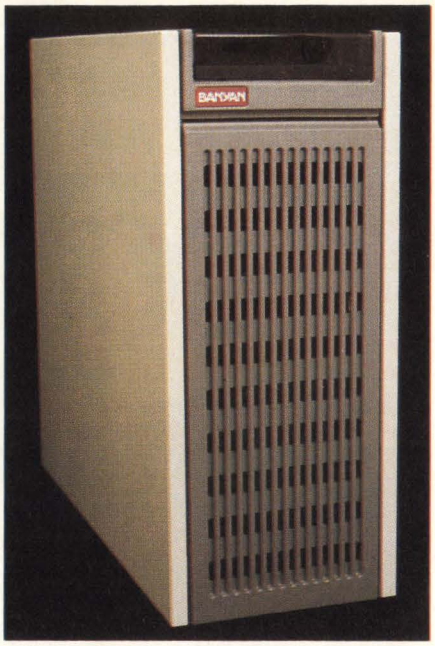

Figure 1: The Banyan Network Server is based on a 32-bit virtual memory processor.

The high speed memory bus operates at a 400 nsec cycle time. The system contains up to 3 Mbytes of memory and utilizes a Memory Management Unit (MMU) with 16/64 contexts, 1024/4096 entry segments map and 1024/4096 entry page map. The memory bus is located in the back end of the system, which also contains the internetwork communcations. The system supports server-to-server networks using Ethernet HDLC/synch, Pronet and X.25. For asynchronous networks, the server supports connection to external host computers, public information services (e.g., Dow Jones) and autodial modems. It provides ASCII terminal emulation on the asynchronous desktop computers. The system uses X.25 packet exchange and X.29 pad service into public data networks.

The third bus, the SCSI, operates at 1.6 msec and contains lines for disk, tape and floppy controllers. The bus meets industry standard specifications and supports simultaneous multiple controllers. Peripherals included with the system are a 5¼" Winchester disk with 43/60-Mbyte formatted capacity and an average access time of 35 msec. The ¼" cartridge tape drive has the same formatted capacity as the Winchester and operates as 90 ips. The 5¼" floppy disk has an average access time of 158 msec and has a 625-Kbyte formatted capacity.

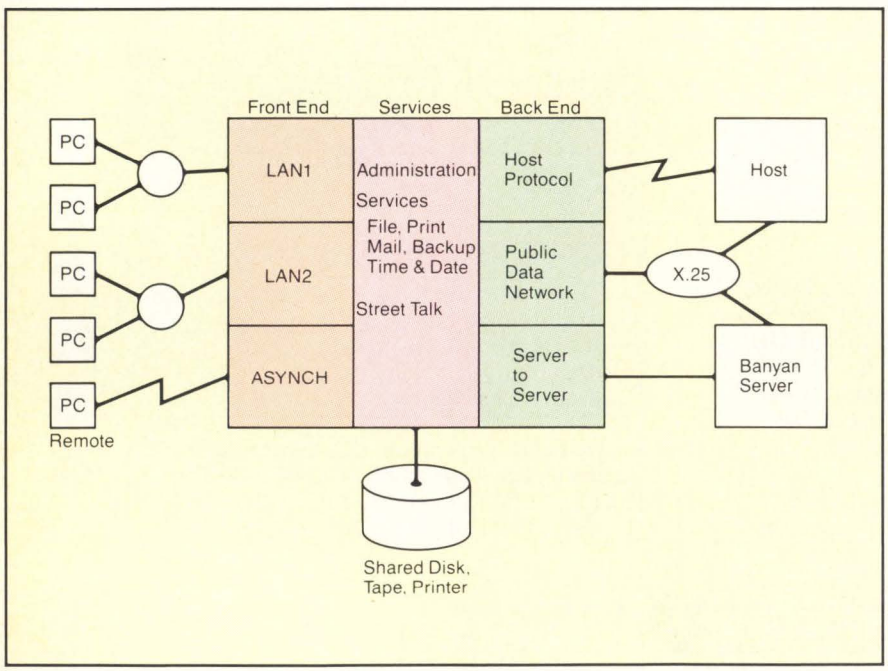

Figure 2: Illustration shows the three functional elements of the network server, which incorporates the three bus structures.

DON'T GAMBLE WITH YOUR SLOTS

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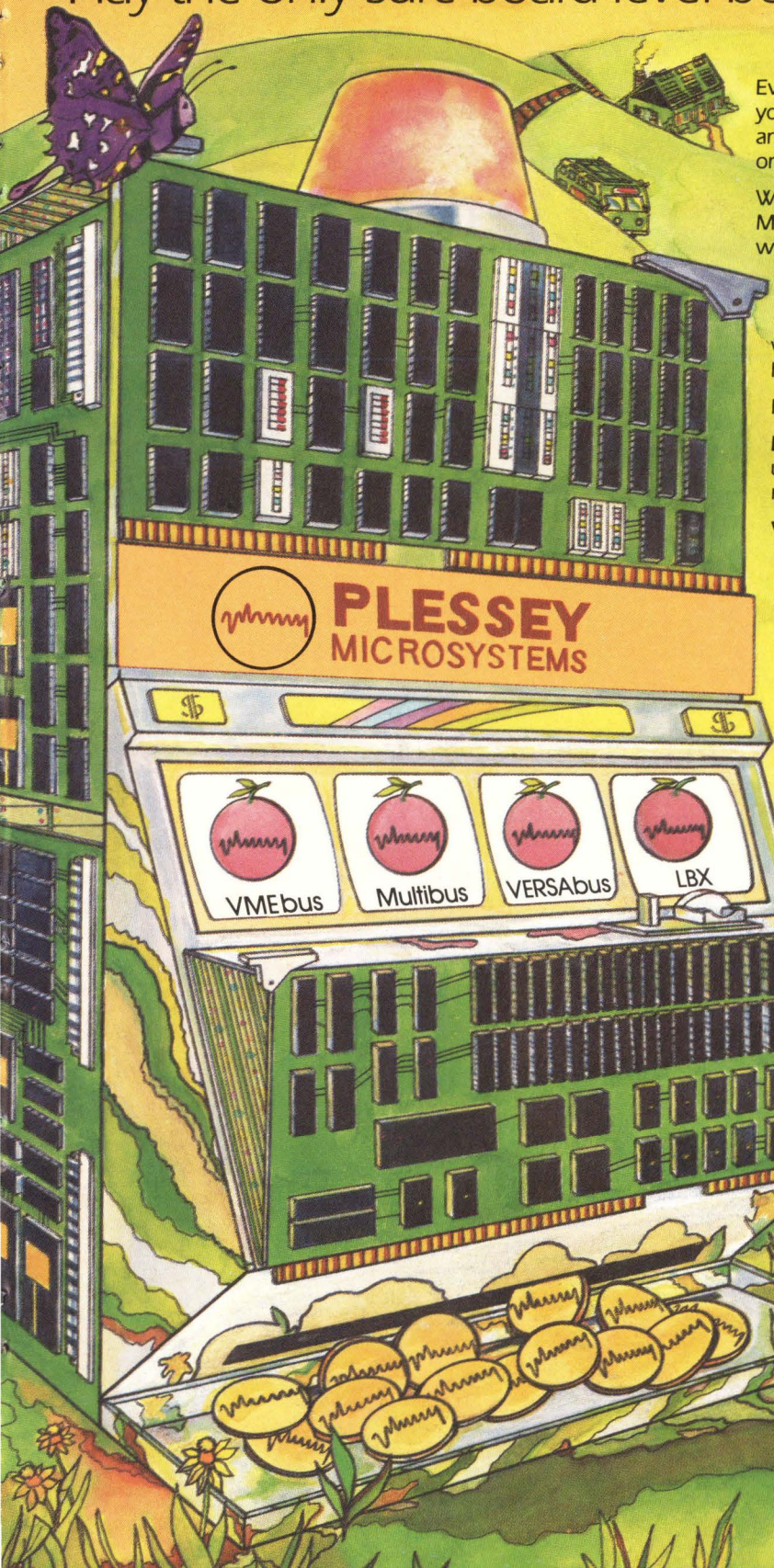

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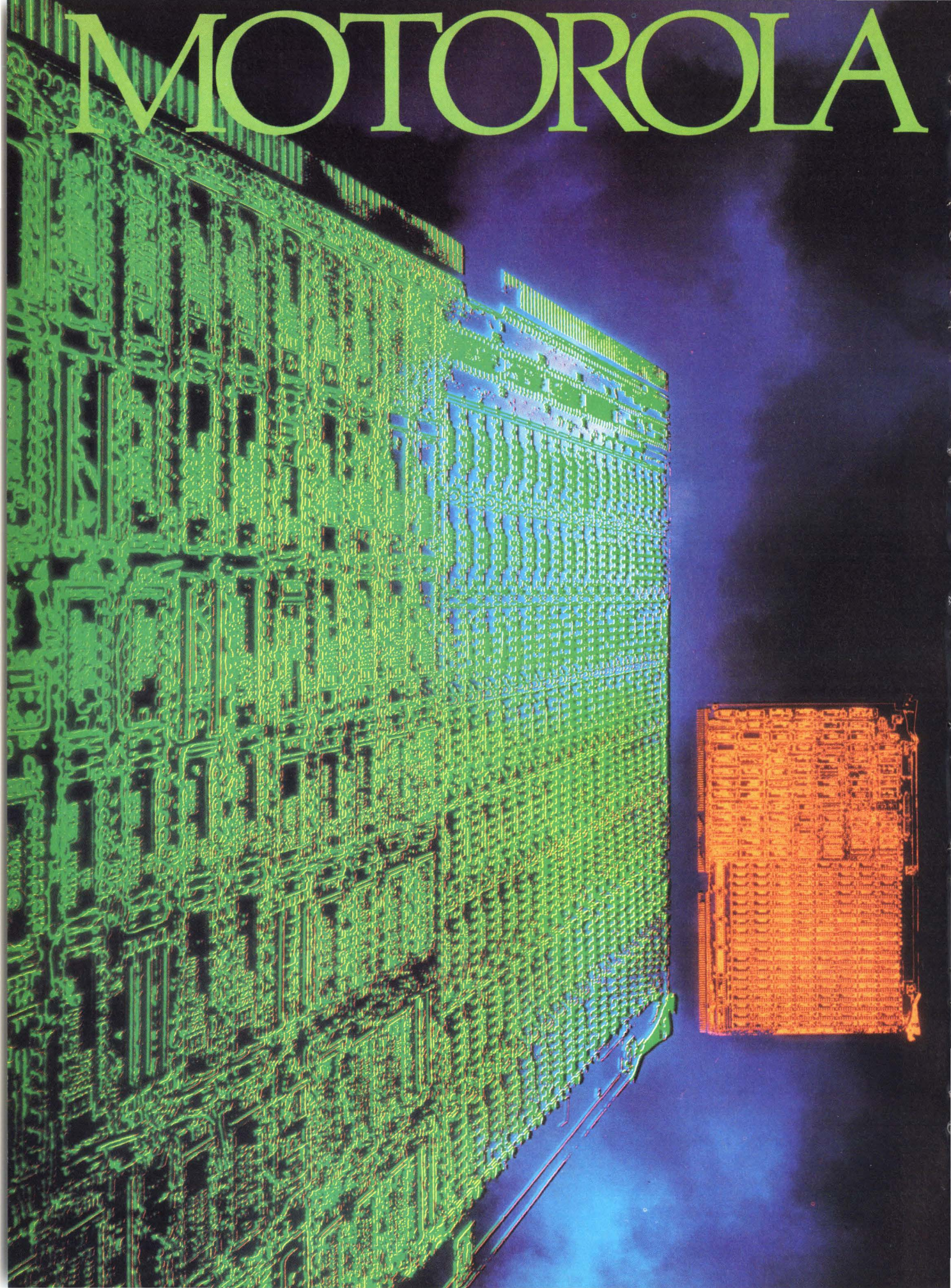

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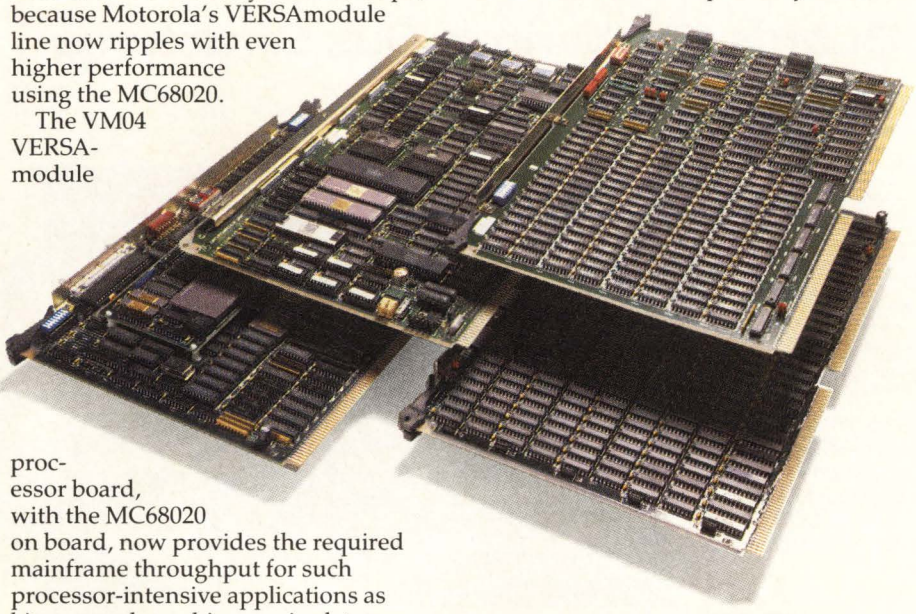
VERSAmodule microcomputer boards have already proven themselves in performance-demanding communication, industrial, laboratory and imaging applications. You knew these boards were powerful workhorses before, but hold on to your bootstraps, because Motorola's VERSAmodule line now ripples with even higher performance using the MC68020.

The VM04 VERSAmodule processor board, with the MC68020 on board, now provides the required mainframe throughput for such processor-intensive applications as bit-mapped graphics manipulators, scientific data acquisition systems and artificial intelligence machines. Applications that, before this, required mainframe machines.



Gaining speed, adding power, lowering overhead.

The new VERSAmodule VM04 processor board can access more than 4 billion bytes of data and manipulate or process 32 individual pieces of information every 180 billionths of a second (180 nanoseconds). Measured in millions of instructions per second (MIPS), the VM04 operates at a sustained rate of 2 to 3 MIPS, with burst rates exceeding eight MIPS, challenging the speed of some mainframe computers.

16K bytes of instruction/data cache on-board help reduce off-board memory accesses to ensure top performance. When off-board access is needed, the VM04 calls on the interface capabilities of Motorola's MC68020-specific RAMbus™ to eliminate most arbitration overhead and speed memory transfers.

The VM04 monoboard is the first MC68020 processor board to offer paged memory management hardware, plus an interface to support the soon available MC68881 floating point math co-processor.

These new modules add to a broad offering of board-level products including processor, memory, controller and communication modules with complete evaluation and development systems.

Broad VERSAmodule line.

Two new high density memory boards have been added to the line to complement the MC68020-based monoboard.

The VM12 includes 1 or 4 Mbytes of RAM and supports the full 32-bit address width of the M68000 Family.

The VM13 dynamic RAM module provides 1 or 4 Mbytes of random access memory dual ported to both RAMbus™ and VERSAbus.™ A perfect system mate for the VM04 32-bit monoboard, the VM13 has error detection and diagnostic capability.

For system applications requiring high-capacity rotating mass storage, the VM22 disk controller supports four SMD drives and four SA 400/800 floppy disk drives. Data transfer speeds up to 3 Mbytes/sec are maintained by the direct memory access feature of the disk controller.

A choice of real-time and whose-time-has-come operating systems.

The VERSAmodule Family is supported by both of Motorola's M68000 operating systems: the VERSAdos™ operating system for real-time applications, and the SYSTEM V/68™ operating system where a UNIX™ operating system environment is desired.

Full operating system support, including VERSAdos real-time device drivers, is available today for MC68000- and MC68010-based VERSAmodule monoboards. Porting is under way to assure their early availability on the VM04 monoboard.

Continued Motorola support.

Add to all this Motorola's expertise, proven products, training and service support and you can understand why VERSAmodules continue to be your best high-performance choice for board-level applications.

For more detailed information on VERSAmodule system components, mail in the coupon or call your local Motorola semiconductor sales office, authorized systems distributor or systems representative.

We're on your design-in team.

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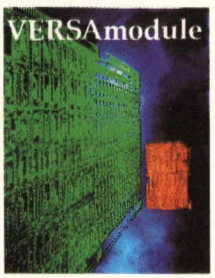
Please send me more information on the VERSAmodule system.



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The system base is the UNIX (Version V) operating system. In order to simplify the system's operation and make it transparent to users, StreetTalk, identifies and locates different users, resources and services.

Names have three parts: local, group, and organization identifiers. Within each group, local names must be unique; within each organization, group names are unique. When a name is referred to, hierarchical directories search for the node. In large networks, directories can be distributed among multiple servers which automatically refer requests to the appropriate directory.

This introduction is an example of a virtual networking system that can be adapted to an evolving data communications environment. It also provides the solution to the incompatibility of existing LAN schemes.

– Coville

Write 238

Intelligent Ethernet Boards For Various Bus Structures

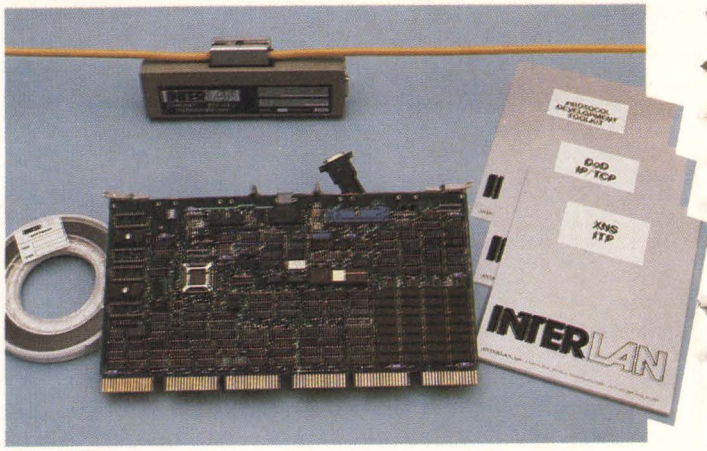
Despite all of the talk of local area networking and Ethernet standards, most of the equipment that has been offered has either been for only one or a few vendor's products or has offered only a physical link, with no protocol software to allow intercommunications. Over the past year, two Ethernet board vendors have brought out an entire series of boards at once to at least partially address that shortcoming.

In the spring, Excelan (San Jose, CA) introduced the EXOS 200 Series. These boards, for the Multibus, Unibus, Q-bus and VMEbus all use the Intel 80186 processor and a networking operating system called the EXOS NX 200 in 16K of EPROM firmware. The resulting front-end networking processor is not a new concept for Excelan; however, they originally had products only for the Multibus. Extending the improved technology of the Series 200 to other bus structures (**Figure 1**) required only that they change the host interface portion of the card; the Ethernet circuitry is all in a "core" area of the board.

Similarly, Interlan (Westford, MA) introduced a series of intelligent network processor boards this summer. Adding higher level protocols on board is new for Interlan. Their approach had been to offer a range of boards for various bus structures, but the new series, also based on the 80186 and Intel's Ethernet chip, adds 16K EPROM storage for either IP/TCP or XNS protocols above the link level (**Figure 2**). Intelligent processor/controllers for Multibus, Unibus and Q-bus were introduced, as well as a lower-level only board for the IBM PC.

In addition to hardware for the most popular bus structures, an intelligent LAN front-end offering must include network protocol software and firmware offerings. Interlan has focused most of their efforts on XNS, but also introduced IP/TCP (Department of Defense standard) for the new boards. In addition, they brought out Protocol Development Tool Kits for OEMs wishing to develop their own software. Excelan has offered IP/TCP with their products from early on, when it was the only one well defined to all seven ISO model layers. Though Excelan's own XNS protocols are not yet announced, they do have third party agreements to allow their hardware to run XNS.

Applications, the seventh layer of the ISO protocol model, are not defined by XNS, so every networking company has



The NP100 Unibus board can be used with on-board protocol packages for the Xerox ITP and DOD TCP/IP user-written protocols.

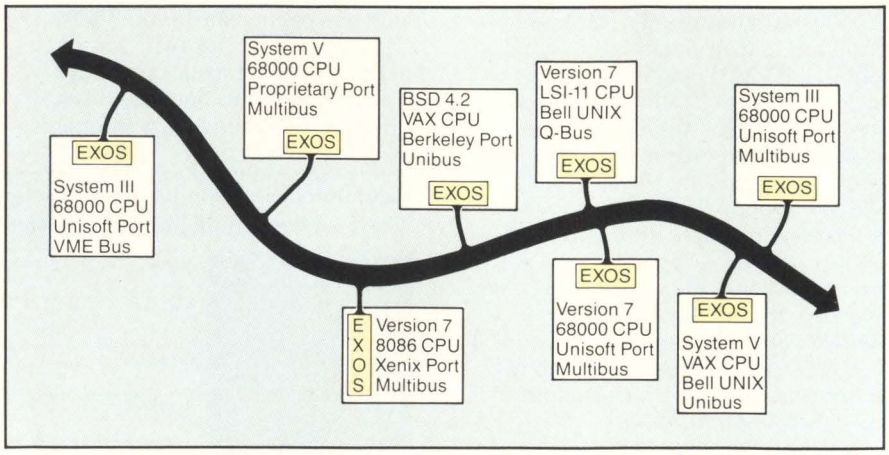


Figure 1: An example of UNIX systems on Excelan's Ethernet using Series 200 front-end processors and their 8010 IP/TCP protocols; file transport, remote copy, login, shell, and electronic mail are available to all users.

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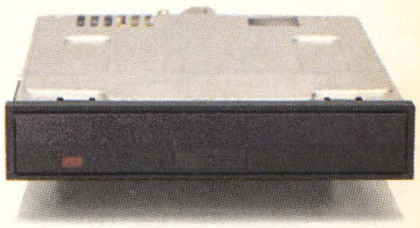

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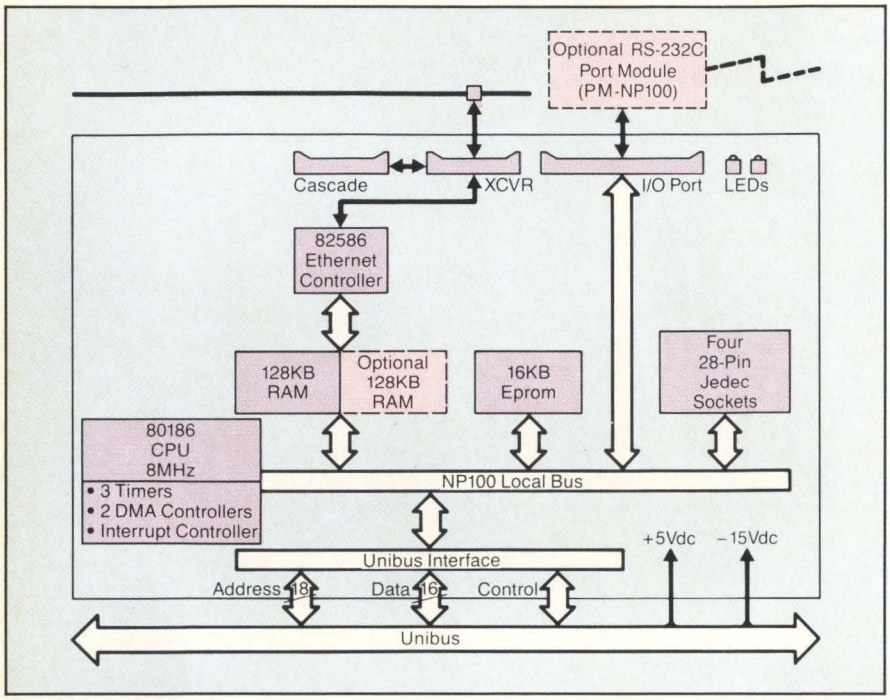


Figure 2: Interlan's NP100 board for Unibus systems, as well as those for other buses and Excelan's 200 series boards, provide Ethernet protocols on board in EPROM. With the power of an 80186 processor and 128 or 256K RAM, host systems are offloaded of communications processing.

defined their own. Bridge, Ungermann-Bass and similar turnkey LAN system houses do interconnect different kinds of equipment, but only if they are hooked up by their own products. With standard protocols like IP/TCP and XNS through even applications, OEMs will be able to create products for interconnection between communications and computer equipment.

Originally, it was believed that XNS would be faster than IP/TCP. Though in theory that is true, the implementation of a network is a far larger factor than protocols in network speed. Reasons that IP/TCP has become popular enough for Interlan to add it include the government's demands that it be used as standard and its suitability to use with UNIX.

These products show that the local area network market is ripening. No longer can computer-based system suppliers afford to let turnkey communications companies supply networking for their products; built-in communications are an important feature now. The intelligence of an 80186-based board with 128K, upgradable to 256K of RAM and network protocols in firmware is evidence that communications overhead on the host processor is also not acceptable.

Providing products for a range of popular bus structures gives OEMs further leverage in integrating networking. Intel has a similar approach for front-end networking, but only offers it to Multibus form factor. This will probably be a drawback for their product offering, now that a similar board is available for various systems. Look for further inroads into protocol standards and compatibility, as well as added bus structures and products like the protocol tool kit from Interlan to allow OEMs to customize Ethernet networking for their products. —*Pingry*

Excelan **Write 233**
Interlan **Write 234**

DEPARTMENTS/Graphics

Video Frame Grabber And Co-processor For IBM PC

A joint development effort between two leading board manufacturers, Data Translation (Marlboro, MA) and Sky Computer (Lowell, MA) has led to the announcement of a video grabber and co-processor subsystem for the IBM PC. Sharing a common data link, the boards allow video data to be acquired by the frame grabber and passed to the co-processor without going over the IBM PC bus. Once the co-processor has processed the data, it is tranferred back to the

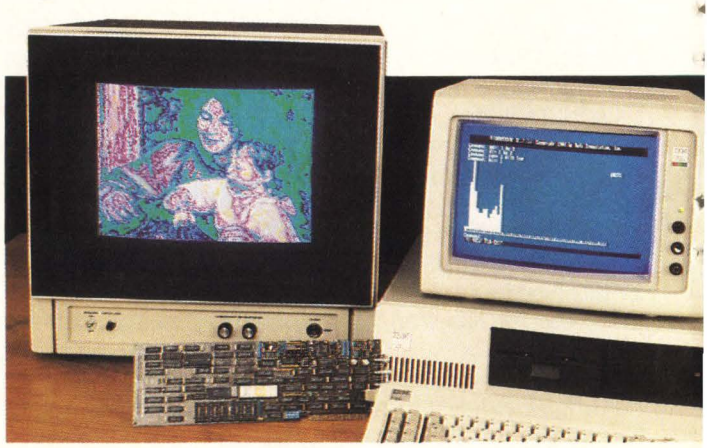
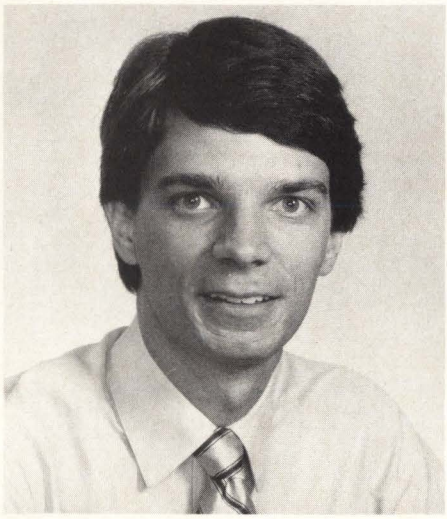


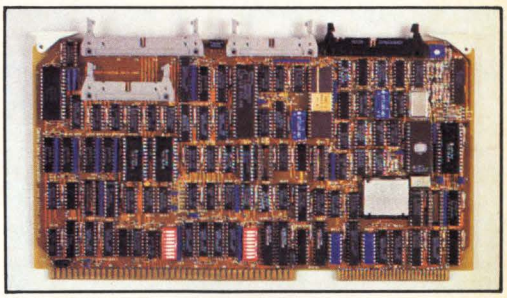
Figure 1: Two new boards from Sky Computer and Data Translation turn the IBM PC into an imaging system.

Central Data is Multibus* I/O Control

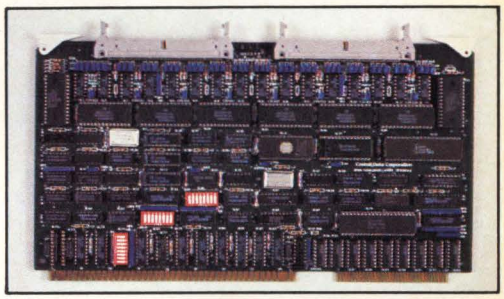


Jeff Roloff, President

"Our commitment to excellence is clearly visible in our Multi-Media Controller and High Performance Terminal Controller. Both offer you the quality and performance you have come to expect from Central Data."



The new **Multibus Multi-Media Controller** is the industry's first to support up to 12 storage media — four each 5¼" Winchester disks, floppies and QIC-02 streaming tape drives, and at an economical price. On-board buffers provide 1:1 interleave transfers and the board supports both bus-vectored and non-bus-vectored interrupts. The board self-tests internally and corrects up to 11-bit burst errors with a 32-bit ECC for Winchester drives. For even greater performance, an optional iLBX* DMA interface is available with the board's (80188) 8/16-bit processor. The **B1030** is available in 100 up pricing at $895.



The new **High Performance Terminal Controller** can operate at 9600 baud-full duplex to all eight channels without loss of input characters. Each channel can be programmed for baud rates to 19.2Kb. The powerful Intel 8088 processor handles all I/O interrupts, freeing time for the host processor. 64K of dual-port RAM is used as buffers for data in and out, with bus lock and parity error detection supported on both ports. Bus-vectored and non-bus-vectored interrupt modes are supported. And for maximum convenience and reliability, the board comes complete with two 60-pin locking right angle headers. The **B1031** is available in 100 up pricing at $705.

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Write 58 on Reader Inquiry Card

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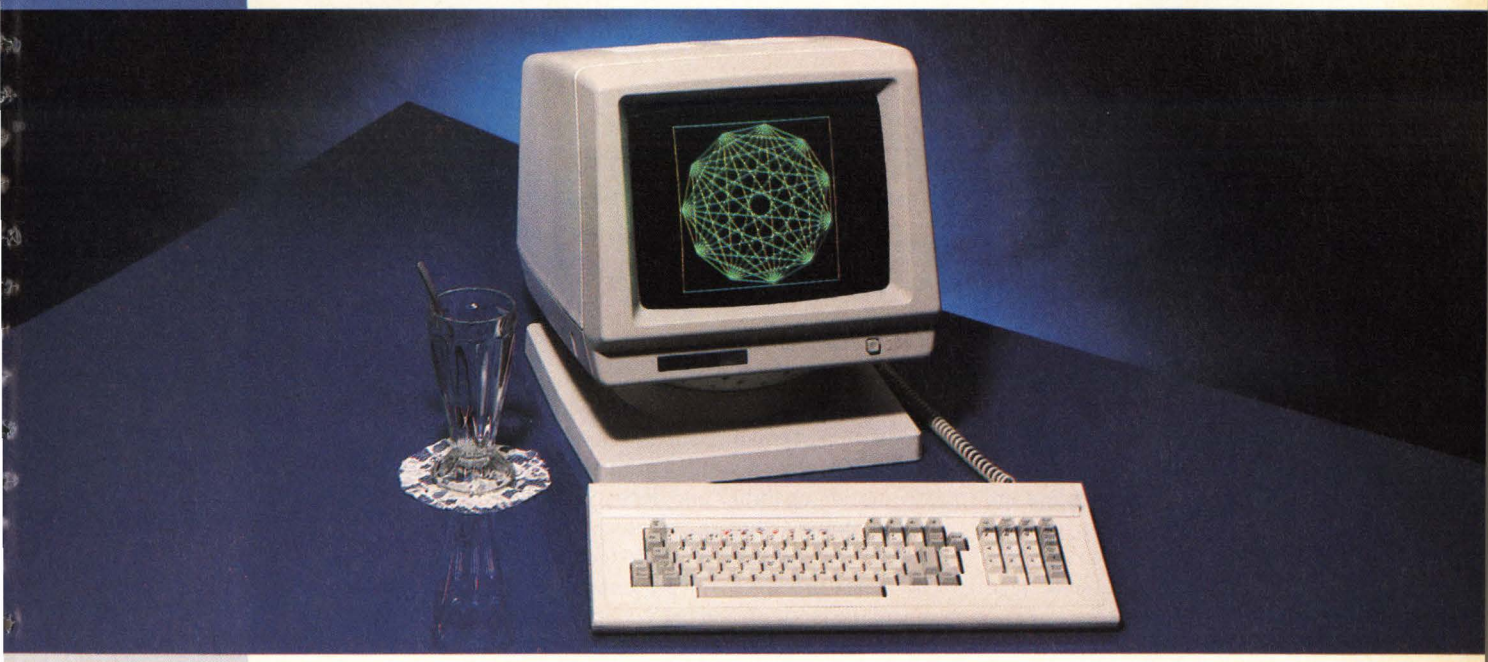

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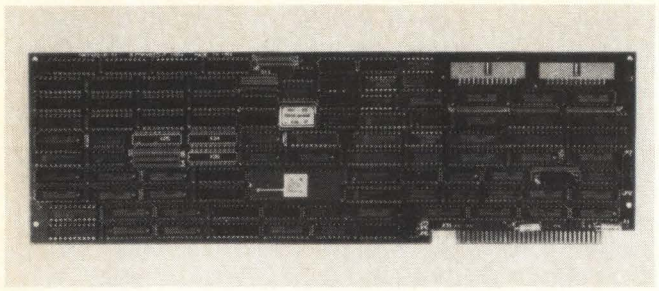


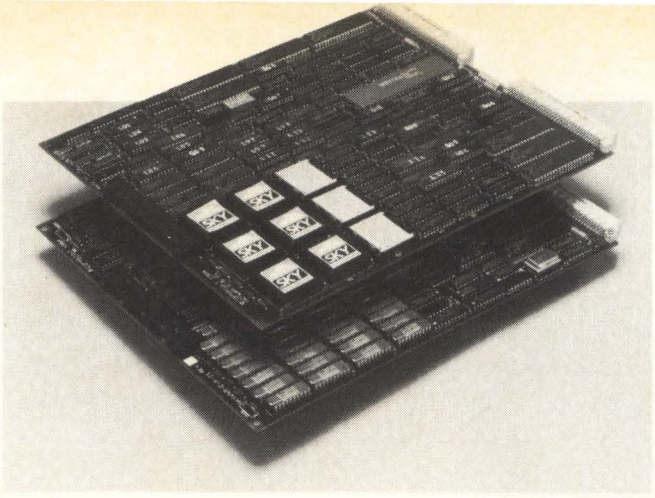


Figure 2, above: Sky Computer's TMS320 based co-processor.
Figure 3, right: The VME-based Warrior from Sky Computer.

frame grabber for display.

Data Translation's DT2803 frame grabber digitizes a video field every 1/30 second and the image is stored in a 256 × 256 × 8 frame memory. Eight input look-up tables (LUTs) are available in PROM and four output look-up tables are provided in RAM. The 256 × 12 output LUTs allow the user to define the output color and intensity attributes for each of the 256 possible byte values that can be contained in the 8-bit memory pixels. This allows a set of 256 (64 colors × 64 intensities) display attributes to be chosen out of a possible 4096 for use in the output display.

Based on the Texas Instruments TMS 320, Sky's SKY320 is a single board add-in co-processor with up to 64K words of 120 nsec four-ported memory, allowing access from the IBM PC, the TMS320 and two auxillary 16-bit I/O ports which operate independently of the PC's 8-bit bus. In addition to providing a C compiler for the product, Sky also provides a macro preprocessor, assembler and interactive breakpoint debugger. A library of mathematical primatives is also offered, enabling FFT, convolution and matrix operations within the users application program.

Announced at the same time was a two-board VME-based array processor, dubbed the Warrior. The Warrior performs concurrent arithmetic and I/O in a manner transparent to the user who accesses the AP through a library of over 100 subroutines. Users' microcoding is supported through a set of development tools. The ALU consists of VLSI floating-point devices and custom registers file gate arrays designed by Sky.

In addition, a 16K × 32-bit cache memory enables processor memory execution without access to the system bus. This memory may be used as the source and/or destination of data for vector arithmetic operations. Double buffering of I/O between the cache and host memory is performed automatically, easing the programmers task.

—Wilson

Data Translation	**Write 239**
Sky Computer	**Write 240**

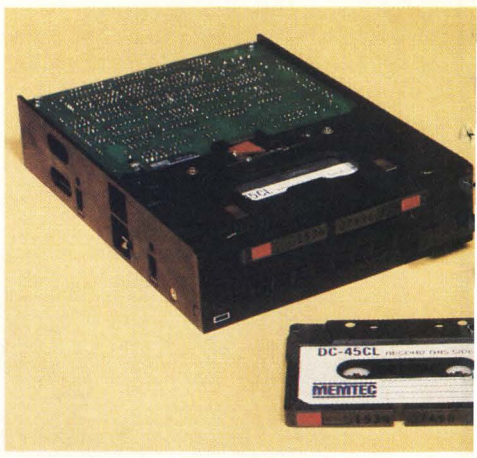
DEPARTMENTS/Peripherals

Digital Cassette Tapes Offer Options For Winchester Backup

As lower-end computer systems acquire large capacity Winchester disk storage, the floppy disk becomes less and less adequate for backup storage. With about 43 times the recording surface area of a 5¼″ floppy in a small cassette, tape offers a solution.

Unlike the huge reels used for mainframe computer storage, tape for small computer systems must be used by a variety of people, fit into a small drive and be very low cost. Traditional tape systems use sophisticated mechanical alignment and tensioning systems to operate reliably. And most tape drives available today are based on that approach. But the mass production of small computers and their peripherals also demands a simple design for interchangability and dependability and economical quantity manufacturing.

One very successful tape product is the 3M Data Cartridge; with proven technology of the medium and back coating and careful drive design incorporating a third order PLL for fast reaction, the product is reliable. At the low end, Wangtek and Cipher have had some success with small form factor drives. At NCC, Interdyne introduced an interesting design for a 3½″ but it appears to have some problems and is not in production at this writing.



Memtec's Companion 400 half-height series uses compact cassette recording media for 10, 20 or 40 Mbytes of storage.

The design developed by the D/CAS group for a cassette (*Digital Design*, July, 1984) rather than a cartridge medium holds promise for its supporters Memtec (Salem, NH), Teac (Tokyo, Japan), Ray-

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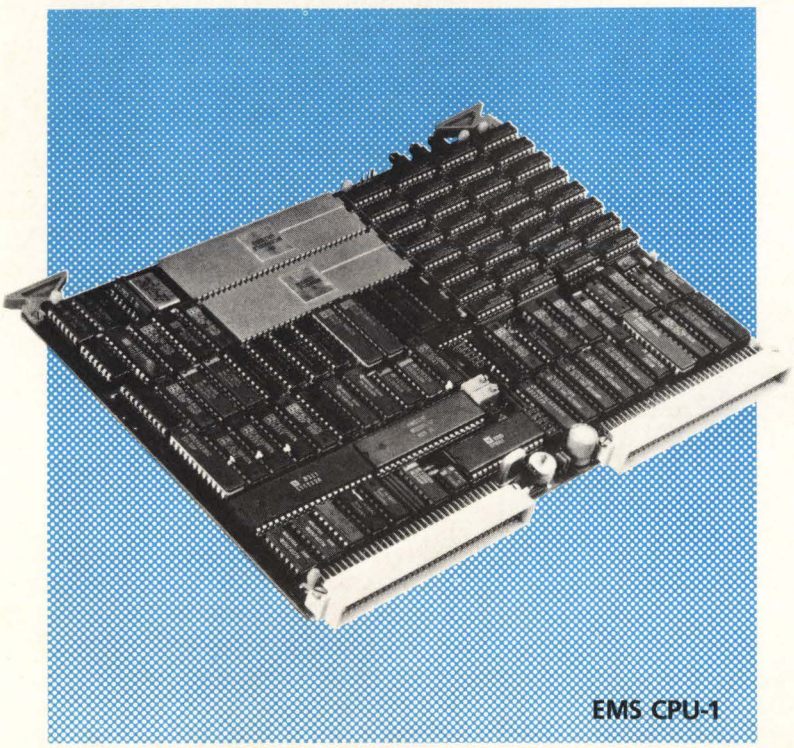

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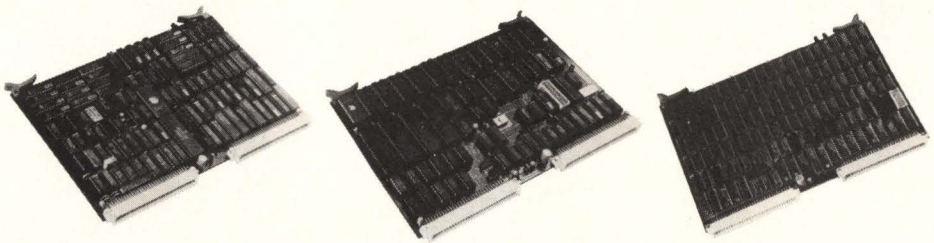

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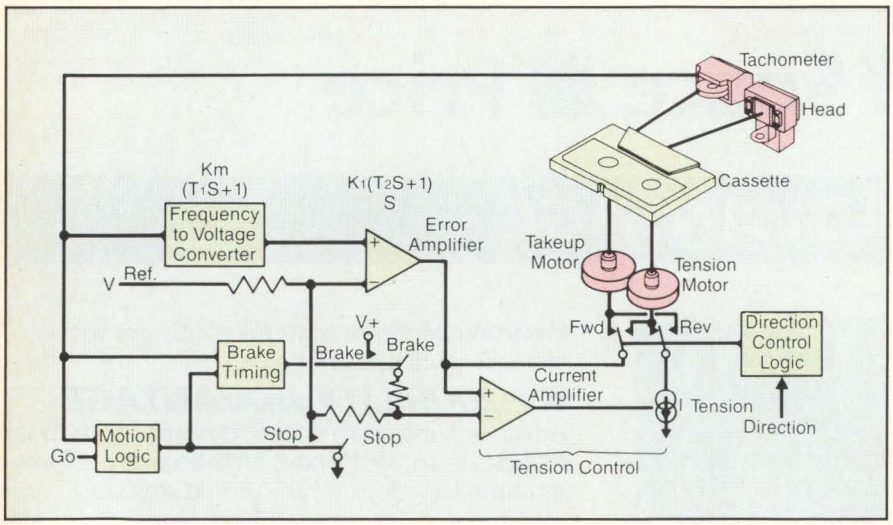


Figure 1: Only four moving parts comprise the design of the drives; tension is electronically controlled.

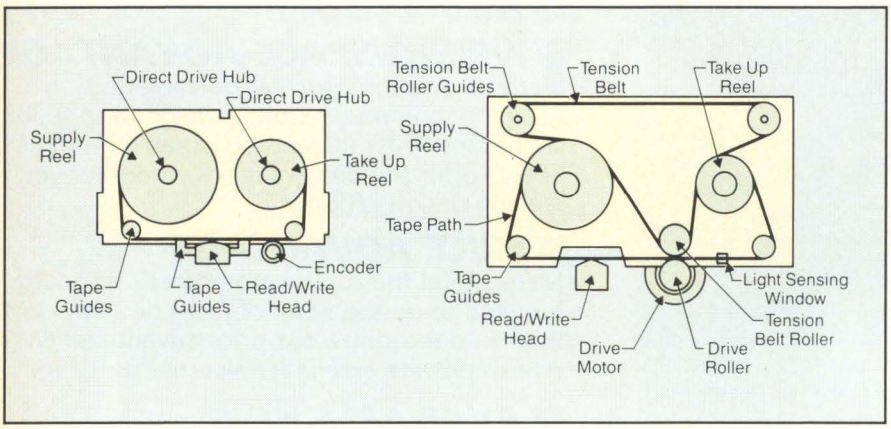


Figure 2: The D/CAS cassette is only 4″ × 2½″ × 7/16″, compared to 6″ × 4″ × 11/16″ for a standard tape cartridge.

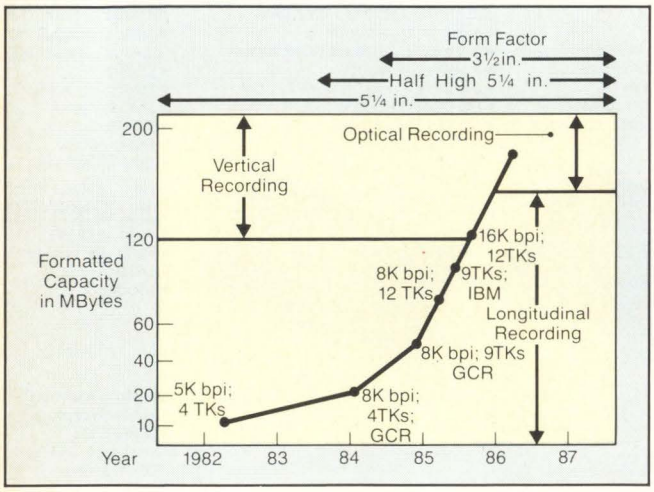


Figure 3: Capacity of digital cassettes has room to grow; by using vertical or optical recording technology, Winchester capacities are rivaled.

mond (Middletown, CT), and media maker Verbatim (Sunnyvale, CA). Similar in appearance to an audio cassette, the medium is well-suited to use in small form factor drives. Especially in the emerging 3½″ backup market, where no backup devices have become accepted, cassettes may win acceptance.

Memtec's drive design for the Companion series uses electronics rather than mechanics for tape positioning and control. In fact, they use only four moving parts (**Figure 1**). The tape floats in the cassette for coarse positioning, and fine positioning is performed dynamically by optical or guide means right on the head. With positioning on the head, interchange between drives and tapes recorded on different drives is not a problem.

To date, full- and half-height 5¼″ drives have been announced by Memtec. In adapting the drive for a half-high package, the solenoid was replaced by a stepper and the door mechanism for cassette insertion altered. Electronics were shrunk by using a 50-pin equivalent gate array. Further compacting schemes to use a 3½″ package are on the drawing board: rotating the cassette in the drive and further reducing discrete components is planned, with no changes to motors, head or basic drive configuration.

A 3½″ drive package for use with the 3M DC100 tape cartridge will very likely also be developed by some manufacturer. The cartridge is a slightly larger package than the cassette (**Figure 2**), however, with good engineering, it will also fit into the 3½″ form factor.

Current cassette products adhering to the D/CAS standard hold 10 or 20 Mbytes, formatted. IBM's new PC/AT is seen as a boost to the market potential of the 20 Mbyte product. Meetings this fall will bring the group closer to agreement on a 40 Mbyte format, but final decisions will likely be next year. The chart in **Figure 3** shows the potential capacities of digital cassettes, with a time line estimating their appearance as products. Arrows at the top suggest the drive form factor, as well. Note that the same cassette medium has potential for being optically recorded, as well.

Originally, the Companion drives were used with the QIC-02 interface; Memtec has since introduced SASI, for higher performance. The QIC-36 basic drive interface originated for cartridges was altered slightly to accommodate cassettes and cartridges.

As small computers increase in sophistication and Winchester disk storage improves in both capacity and footprint, backup will have to keep pace. With the simplicity of design, standards cooperation and potential for using the same medium for both mini and micro form factors, cassette technology will provide a good choice alongside traditional cartridges.

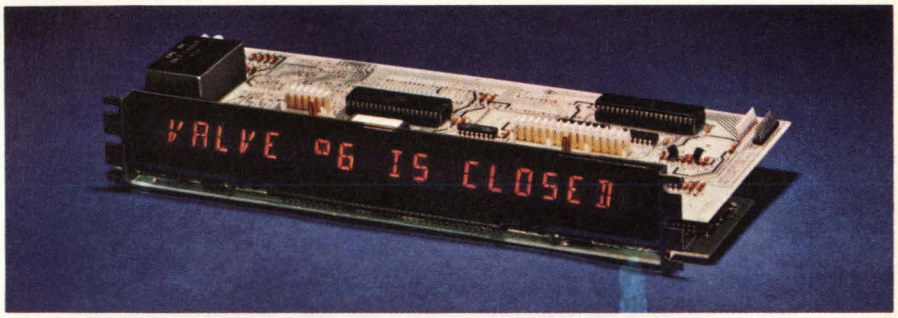
—Pingry

Write 235

New PC display system reduces down-time, increases productivity

F. A. Amendola
Cherry Electrical Products Corp.
Waukegan, IL

Cherry unit adds diagnostics and operator prompting in understandable printed messages to any programmable controller. Cost: less than $300



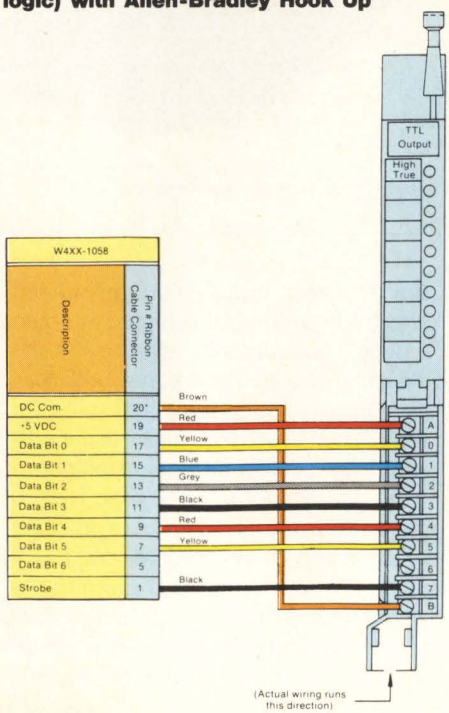
Cherry No. W424-1058, 24 character display system complete with all on-board electronics.

If your programmable controller is not equipped with a serial ASCII output port, you may not be realizing all of its potential productivity. In its present state it is unable to output information for operator prompting or provide diagnostic information in immediately understandable messages for your maintenance staff. Of course the information is being supplied by your PC, but in the form of signals or shut-offs or complicated codes.

The new Cherry display system literally adds literacy to any programmable controller with TTL output drivers, 5 VDC. Instead of using cumbersome look-up tables to translate output codes, your operator is given any of up to 64 messages of up to 32 characters each, spelled out on a bright, easy-to-read display panel. A flashing mode attracts attention to potential trouble such as slipping belts, stuck valves or overheating. Your operator is constantly and instantly supplied with pertinent, *understandable* information about all critical phases of production under your host system's control.

At a cost of less than $300 in OEM quantities this new unit compares with others costing over $1000. It is estimated that the addition of this Cherry display system to your host system will pay for itself in just a few months by decreasing frequency of down time, in improved maintenance and increased machine efficiency.

Typical configuration (positive logic) with Allen-Bradley Hook Up



Easy to install— a complete message center

You just connect two color-coded cables (one power and one signal) and the Cherry unit is ready to take the PCs output drivers and provide output decoding of up to 64 easily programmable messages...anything from "BIN 4 EMPTY" to "ET PHONE HOME." No hardware changes or additions.

This new Cherry unit is a piece of straight-forward engineering consisting of complete on-board electronics and a flat gas discharge display panel of 24 half-inch high characters in bright orange easily readable in any ambience. (Longer messages may be scrolled.) Unit has built in capability for longer scrolled messages and a flashing mode.

Sample Program (message: VALVE #6 IS CLOSED) Starting location HEX 000

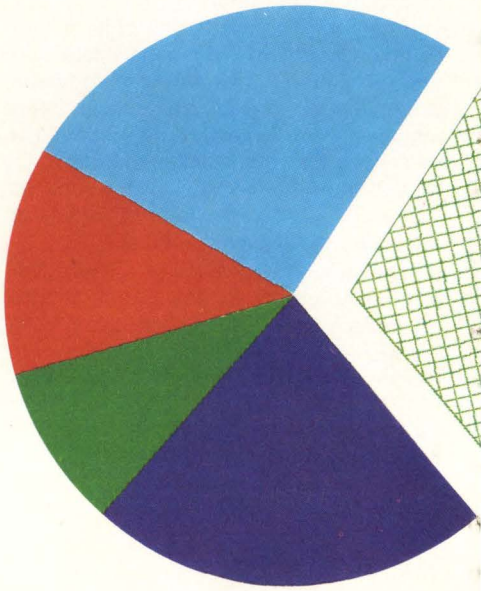
HEX CODE	DESCRIPTION
10	Blank Display—all messages must start with this
0A	Line Feed—clears display
0D	Carriage Return—puts cursor to far left
12	Display Recall—turns on display
56	V
41	A
4C	L
56	V
45	E
20	Space
23	#
36	6
20	Space
49	I
53	S
20	Space
43	C
4C	L
4F	O
53	S
45	E
44	D
89	All messages must end with this

Complete information and specs available

Cherry will send you an 8-page instruction booklet that includes typical connections to various PCs plus application notes on sample programs and ribbon cable connections and Hex Number Addresses for messages in user's EPROM. Send for it today.

Industry Review: Demand Heightens For Color Printers

by Andrea Coville, New Products Editor



PHOTOS COURTESY TEKTRONIX

The demand for electronic color printers, once a fraction compared to that of black and white printers, is increasing rapidly. What is now a trend will become a de facto standard because of factors such as decreasing semiconductor memory prices, the development of sophisticated graphics hardware (like workstations and color displays) and advances in various printing technologies. As display technology begins providing better color and as third party software and primary vendors provide ready access to color displays, users will see a real need for color hardcopy.

The simple explanation behind the demand is that the technology has become available to print color output economically. The applications for color have fallen into two general areas: business and engineering. The color printing technologies used in both environments are ink-jet, thermal transfer, electrostatic, electrophotographic, impact, photographic and pen-plotters.

The most important of the selection criteria involving each of these color hardcopy technologies is image quality. As output moves from monochrome to color, users have begun to place emphasis on devices that offer better quality images. Other factors that influence the suitability of color printers for business and engineering applications are their data processing times, the range of media they can accept, and their reliability.

In the business environment, a broad range of image quality is acceptable. For draft or working copy, a clear interpretation of text and graphics is suitable so high image quality is not as important. But for making transparencies of limited distribution reports, image quality and high color saturation are vital. In electrical or mechanical engineering applications, where color printing is used to delineate layers of complex integrated circuits or in modeling shaded solids, image quality is also paramount.

Important Advances

Recent advances in the printing technologies themselves have contributed to the demand for color printing. This article will address the mechanics of these technologies, but the following is a brief overview of some general trends in color hardcopy.

In thermal transfer technology, where tiny resistors in a thermal printhead selectively melt spots of colored wax onto a donor medium and then transfer the design to heat sensitive paper, advances have been made in thick and thin film head design which have meant better reliability, lower cost and higher resolution.

Ink-jet technology has gone from a good idea in the laboratory to a practical solution for many applications. Early attempts were notoriously unreliable which limited them from gaining a sizable market share. But now, with advances in mechanisms, inks, and media, this

As display technology begins providing better color and as third party software and primary vendors provide ready access to color displays, users will see a real need for color hardcopy.

technology, along with thermal transfer, is forecasted to be the dominant color printing technology for the future.

Impact printing is a more mature technology with less room for improvement. Yet there have been improvements in manufacturing efficiency as well as innovative methods in converting monochrome to color.

Another mature technology, pen-plotters, have benefited from simple design changes such as the microgrit printwheel introduced by Hewlett-Packard, which greatly decreased the complexity and cost of the drive mechanism for "A" and "E" sizes.

Finally, photographic color printing, a relatively new and low cost technology, has taken advantage of especially fast film which can be developed on-sight. The result is a new generation of instant low cost slide-making printers which use commercially available film and processors, and produce full color slides in minutes.

Printers vs. Plotters

The question for the systems integrator or end-user is what color printing device best suits the overall system or application. In the broadest sense, any color hardcopy device which can put computer-resident information into a graphics format can be thrown into the stream of competition.

Pen-plotters and raster-based technologies are direct alternatives for each other in certain applications. A pen-plotter, by virtue of the way it puts ink on paper, is a strong contender in fine line graphics. It is a relatively simple technology, and for the size of the device, economical for applications which require lines and a limited color palette. The maximum number of pens a plotter can drive is eight, although vendors can claim more color by using interchangable pens.

Pen-plotters are the oldest and most popular color hardcopy devices. One reason is their ability to produce smooth-edged diagonal lines. Printers are restricted to laying color dots at the intersection of a matrix, giving a jagged appearance to diagonal lines. This shortcoming is lessened as addressability increases because the printer can generate more printed dots per unit of distance.

A key limitation to plotting technology is the size of its color palette. In applications such as solids modeling, mapping, and graphics art which involve complex shading and area fill, they are slow. This limitation may become more severe as color hardcopy technology becomes prevalent and the available software increasingly sophisticated.

Another limitation to plotting technology is the speed at which they can produce large vector drawings. As users move to large color palettes and make use of solid area fills, there is a necessity to use a raster approach in putting ink on paper. An example of this is a 4G, 40 inches per second (ips) pen-plotter doing a 2,000 short vector drawing in 90 seconds, the same speed as a typical raster color printer. But if the complexity of that image is multiplied by a factor of 10, to 20,000 vectors, the raster printer would still take 90 seconds and the plotter might take 15 minutes. Hence, vector plotting has a key advantage because it is simple, doesn't require conversion and gives good line quality. The drawbacks are limited color, speed, and flexibility.

Most raster-based technologies have suffered from low addressable resolution. But many are starting to show increased addressability. The development of hardware and software rasterizers by manufacturers such as Versatec, who use data processing algorithms to convert vector format data into raster format data at full resolution, are narrowing the advantages of pen-plotting technology.

The Technologies

The following technologies, which were mentioned earlier to illustrate general advances in color printing, represent the raster-based printing technologies which are used for the majority of color printing applications.

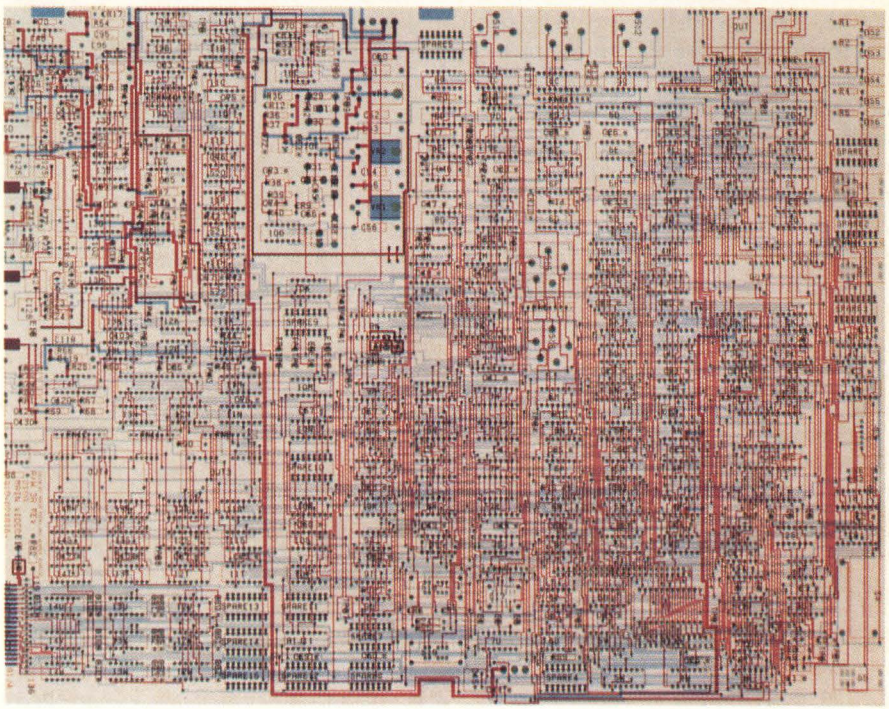


Figure 1: Output sample from the Versatec color plotter.

Figure 2: The Xerox 6500 Colorgraphic Printer.

Ink-Jet—

Ink-jet printers place small drops of ink onto paper in dot sizes ranging from 8 to 20 mils. Printing is of medium accuracy and addressability varies between 80 to 200 points per inch. Some of the leading manufacturers of these printers are Tektronix, ACT, Benson, Radio Shack, Applicon, Canon, Diablo and Printacolor.

There are considerable variations in the methods used by these companies' products, but most use some variation of the drop-on-demand technique. This involves a printhead, containing multiple ink chambers controlled by piezoelectric crystals, which is scanned over the paper. An electrical pulse is applied to the piezoelectric crystal when a drop is needed. The pulse causes the crystal to constrict, causing a pressure wave to be sent through the ink chamber, forcing ink through the nozzle. To boost the speed of the process, several ink-jets are combined in an array.

Ink-jet printers deposit all the colors to be printed in one pass over the paper. This can be done by two methods. In one, the paper is attached to a rotating drum on which a traveling carriage containing the ink is mounted. This carriage contains several printheads with jets which drop ink as the carriage traverses axially. The second method combines the color jets onto a single printhead that scans the paper and prints all colors in the one pass.

Ink-jet technology suffered some early problems, such as dried ink clogging the printhead nozzles, plots smearing from ink that didn't dry fast enough, and poor color saturation. However, an advantage is that the color from the dyes used in ink-jet transmit light. Ink-jet researchers have experimented with aqueous and non-aqueous inks. Non-aqueous inks, which are oil-based, don't clog as easily, but require a long drying-time on transparency media. Vendors who have chosen aqueous inks have tried to circumvent clogging with mechanisms which purge malfunctioning jets as well as wash and cap the heads.

Thermal Transfer—

Thermal transfer printing became available about a year ago. These printers, manufacturered by companies like Shinko, Oki and Seiko, have addressabilities which range from 100 to 150 points per inch with dot sizes of 7 to 10 mils. Printer accuracy is on a par with ink-jet technology.

Thermal transfer printers, as opposed to direct thermal printers, can use plain paper, rather than heat sensitive paper. This is accomplished through the use of donor film which is comprised of a variety of pigments, waxes and softening agents. This donor film is placed over the plotting medium (paper or transparency film) with the pigmented layer in contact with the medium which is in turn against a rubber roller. A variety of media may be used as long as the surface is smooth. The printhead contains resistors which heat and cause the colorant to melt onto the paper. This process is done one dot line at a time and each color is laid down on the page in sequential order. The colorant is fixed to the donor film which can be used only once and is expensive. (Cost per "A" size print is 25 cents.)

One of the design issues inherent in thermal technology is registration. For all printing technologies which lay down their color in a three or four pass process (thermal, electrostatic, electrophotographic), it is necessary to have extremely precise control over the paper. An example of this is the Versatec electrostatic printer, for which much of the design effort was spent on control registration.

One side effect which adds to registration problems, especially in the large format electrostatic technology, is that under certain environmental conditions a lot of ink will deform the paper. The deformity occurs in bands which appear as a rippling effect. When the paper deforms, registration becomes even more difficult. The solution necessitates a controlled temperature environment. Registration is also a problem in low-cost thermal printers when using difficult-to-handle transparency paper.

Another factor affecting image quality in thermal transfer printers is that the reflective, nearly opaque pigments used for color give a waxy look to the output. Use of these almost opaque pigments has two effects: one, when two colors are laid down to form a third color, the top one tends to block the color of the underlying pigment; and two, when used on transparencies, the colors appear duller and darker, because, although the pigments are well-suited to reflecting light, they are poorly suited to transmitting it. However, these printers are gaining wide acceptance and are a good choice as color terminal copiers.

Dot Matrix —

Color dot matrix impact printers are made by several manufacturers including Centronics, IBM, IDS, Ramtek, Anadex, GE, Trilog and Envision. They are suited for office environments and have addressabilities of 70 to 240 points per inch and a dot size of 18 to 19 mils.

In this technology, printhead wires strike a colored inked ribbon impressing the color on the paper. Impact technology is limited by its design from attaining high image quality. First, the printer hammers are often too large to generate the small dots needed for high quality printing. (The print hammers must be less than .010″ in diameter.) Second, the ribbon which contains the primary colors becomes contaminated if the second color to be printed picks up some of the first. The ribbon also loses color gradually with use.

These printers have strong advantages,

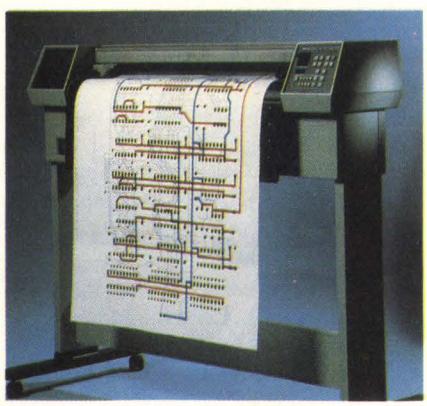


Figure 3: This output sample from Hewlett-Packard 7585B shows an example of PCB layout.

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however, in applications which require a clear working copy and the ability to mix text and graphics. They are well suited for graphics used for emphasis and in a printed document. Also there has been progress in ribbon technology as some manufacturers have designs that allow one ribbon for each primary color. The impact printer is very competitive in cost, being one of the lowest priced color hardcopy technologies, and can be downloaded from a central processor, and buffered to at least one line of memory.

Electrophotographic —

The first color electrophotographic printer was introduced in 1978 by Xerox, still the only manufacturer of this printing technology. At a price of $39,000, the 6500 has an addressability of 100 points per inch and a dot size of 15 mils.

The process involves a photoconductive drum which is given an electrical charge. The data for the blue component of the image is used to modulate the intensity of a laser beam which scans the photoconductive drum, leaving a charged latent image. The latent image picks up charged cyan toner and transfers the image to paper. The drum is then cleaned, and the process is repeated for the other two color components of the image. The toners used in order of transfer are cyan, magenta and yellow. After the color process is complete, the image is thermally fused to the paper.

Xerox is interested in several markets, but the largest two are the office environment and those areas associated with electronic publishing. According to Xerox, they expect to see competition to the 6500, but it has not appeared yet due to differing projections concerning the electrophotographic market.

Image quality in this technology is dependent on the resolution of the laser, dot size and the quality of toners used. The 6500 prints three original hardcopies a minute at about six cents a copy. Images are first created for viewing on a color display and are transmitted by the terminal data input channel to the 6500 where they are printed on plain paper or overhead transparency material. The device can operate in either the computer mode or as a xerographic color copier, or in both modes if specifically formatted reproductions are needed. Enlarged copies of 35 mm slides are possible with a slide adapter.

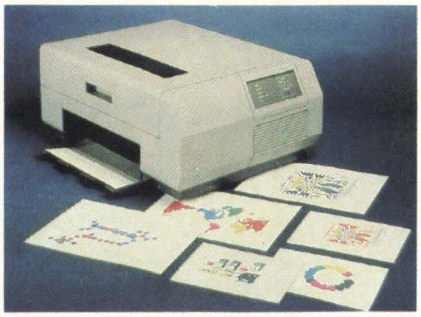

Figure 4: The Tektronix 4691 color graphic copier uses ink-jet technology for business graphics applications.

Electrostatic —

Electrostatic printers, whose leading manufacturer is Versatec, became available in color only recently. The price for the Versatec printer is formidable at $98,000, but the addressability of 200 points per inch and dot size of 8 mils, coupled with high image quality and large format size make it suitable for electrical and mechanical engineering applications. The main disadvantage of this technology is its price; the head and high voltage drivers account for the largest portion of cost.

Electrostatics compete mainly with pen-plotters but the technology is substantially faster and can accomplish an "E" size drawing of 40 million elements in 8 minutes, lending it nicely to CAD/CAM and seismic applications.

The process involves cycling the print medium through the copier five times. During the first cycle the medium is conditioned, and a black registration track is placed along the edge of the print. In the next four passes the cyan, magenta, yellow and black portions of the image are created and held in color-to-color registration over the length and width of the image. The print medium is a plastic layer that is coated with a conductive substrate. Two rows of offset metal nibs contact the medium, forming a charged, latent image when the nibs are pulsed to a high potential. As the paper advances the process starts again and is developed by liquid toner applicators.

Photographic Printers —

Photographic technology is the only method by which 35 mm slides can be made from video sources. They generate true continous tone images at an addressability of 85 to 800 points per inch with a dot size of 20 to 6 mils. Price ranges from $3,000 to $15,000.

Photographic printers make a color print by separating a video image into red, green and blue components and then relaying this separation to a special monitor. The monitor projects the images sequentially onto film through color filters. Manufacturers of photographic printers

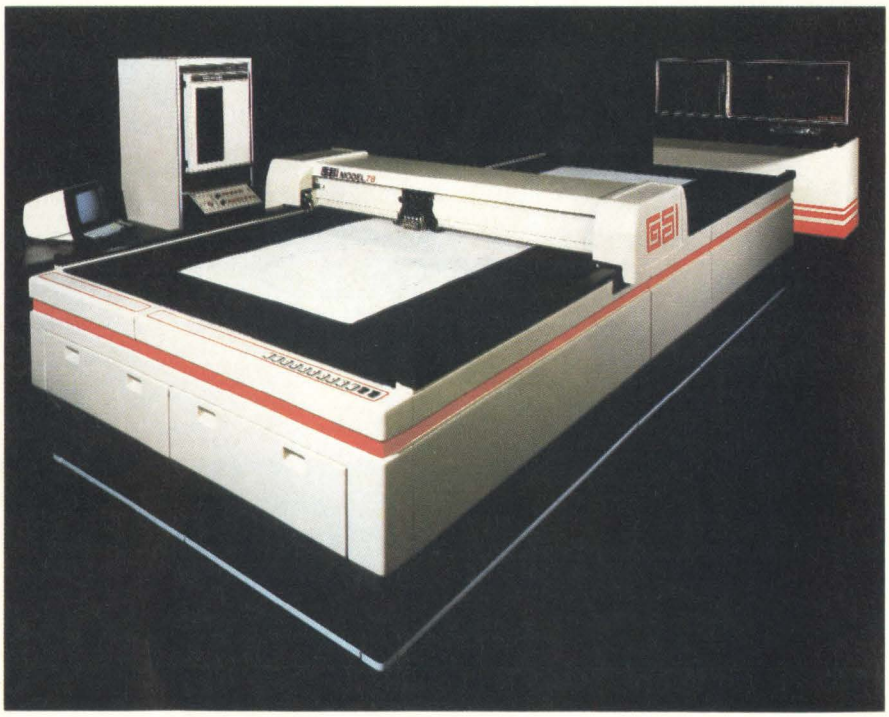

Figure 5: Gerber Scientific's Model 78 flatbed plotter.

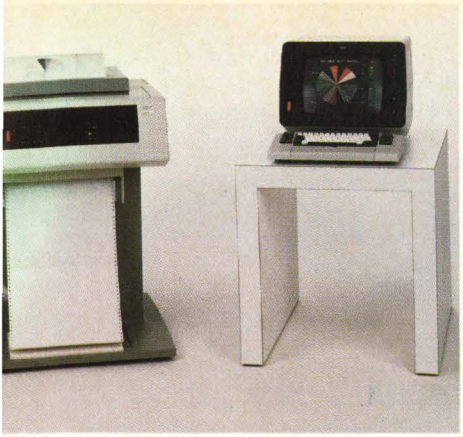

Figure 6: The 32 serial printer from IBM operates at 340 cps.

include Polaroid, Dunn Instruments, Image Resource, Matrix Instruments, Lang, Celtic, NISE and Kodak.

Addressability and Resolution

Addressability and resolution are two often quoted specifications which are more often than not misleading and used in the wrong context. Harry Watkins, Product Manager for Tektronix, says, "Addressability is what all manufacturers who are quoting a resolution specification are talking about. They are talking about the ability to place a certain number of dots within a linear area. But addressability is the ability to address points in a given area. For example, when one company claims to have a resolution of 344 horizontal and 144 vertical, what they are talking about is the fact that their mechanism allows the nibs to hit the ribbon 344 times within an inch."

"Another factor which affects resolution is dot size," explains Watkins. "Resolution is the number of parallel lines per unit distance, and it is a function of the combination of addressability and dot size. In the case of impact printers, some of them can address many points in a given area, but their spot size might be 12 mil and as a result, their ability to resolve lines is approximately 60 or 80 lines per inch."

"In the case of thermal transfer, spot size is relatively good, ranging from 10 to 6 mils. So when a vendor quotes 200 dpi, they are able to come somewhat close."

Another way to make the most of addressability is by using hardware and software rasterizers. Much of the computer information to be printed is resident in vector format mode which has to be converted to raster information prior to printing the image. A raster printer may have a very high resolution, but if it is getting information at a low resolution level, image quality will suffer. An example of this is the devices which provide RS 170-type interfaces to color displays. Many of them are tied to color displays which run 640 × 480 or 1024 × 1024 pixels. If these displays are used with printers that have 80, 100, or 120 dot addressability, the match is fine. But with future printer introductions which will have extremely high resolutions, a problem will arise. A straight screen dump into the printing device would not be taking advantage of the ability of the hardcopy device. Hence, the need for a hardware or software rasterizer. Versatec and Tektronix both provide their own rasterizers.

Future Trends

The technologies described in this article are projected to do well over the next three years. Pen-plotters have a dominant share of the market, a large amount of software support, and have been driven down in cost. Their shortcomings, which involve speed and a limited color palette, will become more apparent as other technologies advance.

Dot matrix printers will serve applications that emphasize alphanumerics, line printing and limited color requirements. Electrostatic technology shows great promise. These printers will be priced high, but the advantages will be equally high. The question remains as to whether they can be cost effective for "A" and "B" size formats, but they have a strong feature in that they can make vector to raster conversions. Thermal transfer and ink jet offer the best throughput for small formats. Thermal transfer's limitations reside with the opaqueness of their pigments, and controlling the residual heat of the nib. Cost per copy is approximately 25 cents a sheet, but as volumes increase, the price will drop.

On a final note, the next step in color hardcopy technology will be to incorporate signal processing algorithms into the conversion process. Some of the techniques that were developed in Landsat technology may be applicable. The goal of high image quality is becoming attainable as image processing is applied to color hardcopy technology. DD

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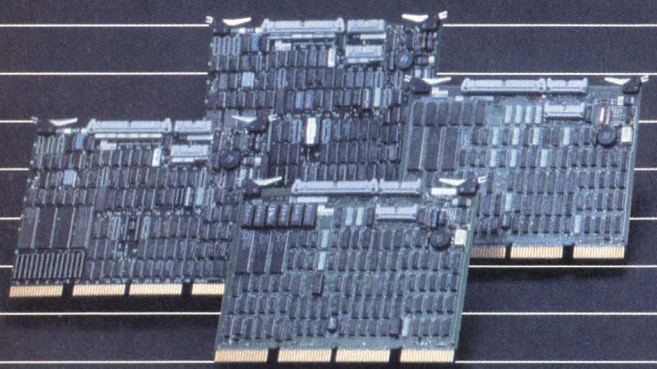
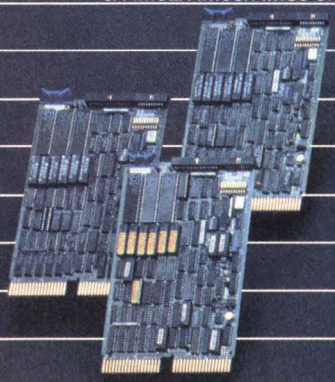


8″ & 14″ WINCHESTER—SMD I/0
- RL01/RL02, RP02/RP03, RK06/RK07 & RM02/RM05/RM80 emulations



WINCHESTER 5¼″—ST506/412 & DMA I/0
- RL01/RL02, RK06/RK07 emulations

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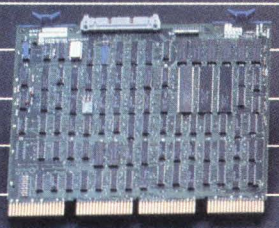
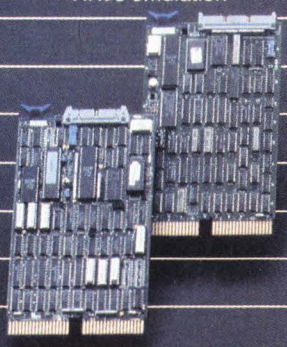
8″ & 14″ WINCHESTER—SA4000 & PRIAM I/0
- RL01/RL02, RP02/RP03 emulations



CARTRIDGE—14″ DISK—DIABLO 44B
- RK05 emulation



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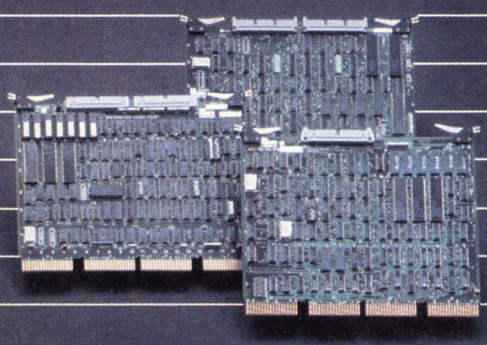
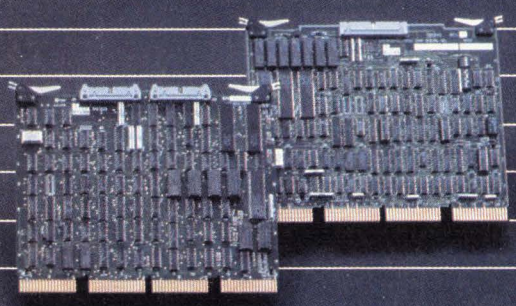
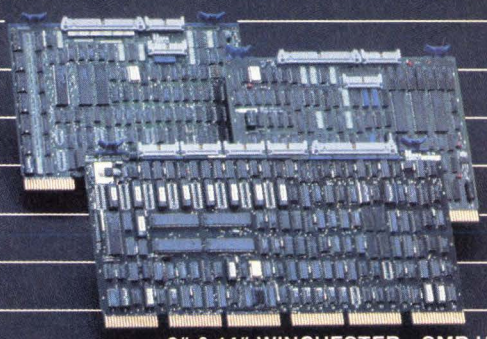


½" TAPE—CONTROLLER/COUPLER PERTEC I/O
- TM-II, TSV05/TS-II/TU80 emulations

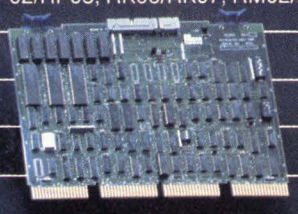


¼" TAPE—KENNEDY 6455 & CDC SENTINEL I/O
- TM-II/TS03, TS-II/TU-80/TSV05 emulations

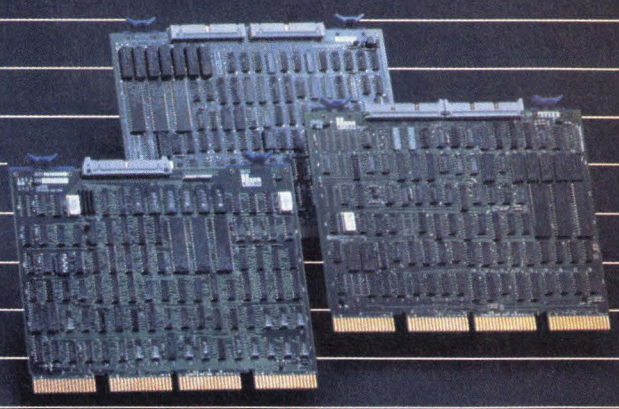
UNIBUS



8" & 14" WINCHESTER—SMD I/O
- RP02/RP03, RK06/RK07, RM02/RM05 emulations



¼" TAPE—CDC SENTINEL I/O
- TS-II emulation



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Designer's Guide To Winchester Disk Drives

by Bob Hirshon, Contributing Editor

Rigid disk drives are turning up in the most unusual places lately. For example, one Microscience International (Mountain View, CA) customer complained that their drives were malfunctioning due to "excess moisture." "When we got there," explains Ron Schlitzkus, Microscience Director of Marketing, "we found they were mounting the drives in the heads of torpedoes."

As disk drives get smaller, tougher and cheaper, such surprises are becoming more common. Today's drives are being designed into military hardware, factory tools and portable computers – not at all the sorts of places one would expect to find Winchesters.

Traditionally, Winchesters have been one of the touchiest, and therefore the most protected, of peripherals. "Reliability" has consistently topped the list on *Digital Design* reader surveys as the most crucial characteristic designers look for in Winchesters, and Winchester malfunction consistently tops the list as the most common cause of computer system down-time.

Recently, however, a number of advances have contributed to making Winchesters more reliable, and resistant to severe environments (see accompanying box "Ruggedizing Winchester Disk Drives"). At the same time, the technology has enjoyed sharply increased capacity and performance, lower power requirements, and lower cost.

The Sub-4" Drives

The technology that best exemplifies how far Winchesters have come is the sub-4" class of drives. Specifically designed to withstand the rigors of the portable computer environment, these drives employ the latest shock mounting techniques, vibration resistant mini-composite heads, and other techniques to protect them from rough treatment.

One unique feature employed by LaPine Technology (Santa Clara, CA) is retractable, locking read/write heads. Most drives lock the heads in place, but don't isolate them from the media surface. LaPine retracts and locks the heads when the drive is not in operation, protecting both the heads and the media.

Bob Hirshon is Contributing Editor, Peripherals for Digital Design, *and Editor-in-Chief of* Memory Update *(78 Oldham St., Pembroke, MA 02359. Tel. 800-962-2001), a twice-monthly news journal of mass memory technology.*

Small Winchesters are becoming more rugged and even more compact; makers of high-end Winchesters are finding it hard to follow IBM's lead; and Winchesters across the board now offer more capacity at lower cost.

In addition, LaPine offers an optional external shock mount system which raises the drives' resistance to shock from 40G (the de facto standard) to 100G, when in a non-operating mode. The external mounts add considerably to the drives' effective dimensions, but it may be the only way a designer can get 10 Mbytes of highly shock-resistant memory into a format anywhere near that small for the price (around $500).

Microscience International's 3½" drive incorporates plated media, closed-loop servo head positioning system and linear actuator assembly. These three features should give the drive an advantage in extreme environments, since: plated media is somewhat harder and more resistant to moisture than oxide; closed-loop positioning compensates for temperature variations; and linear actuators provide accurate head registration even under high stress conditions.

Nippon Peripherals (Kanagawa-ken, Japan) and Microcomputer Memories Inc. (Van Nuys, CA) are the first two companies to offer 3½" Winchesters with 20-Mbyte capacities. But already companies are talking about 50-Mbyte models, and at least one company – Epelo – is working actively on a product.

Other sub-4" Winchesters on the market are made by Rodime (Boca Raton, FL), and SyQuest Technology (Fremont, CA). A number of other introductions are expected at or just before the COMDEX show, probably from Qume (San Jose, CA) and Seagate Technology (Scotts Valley, CA).

The 5¼" Half-Heights

Thanks primarily to the flourishing IBM PC-compatible subsystem market, half-height 5¼" Winchester disk drives are enjoying immense popularity, and several relatively new companies are devoted exclusively to the format.

The half-height 5¼" Winchesters allow subsystem manufacturers to add value to their products by letting them offer a variety of different mass storage options in the footprint normally occupied by a single 5¼" Winchester. A half-height 5¼" Winchester may be coupled with a half-height minifloppy drive, or a quarter-inch cartridge tape drive, or a streaming cassette drive, or even a removable Winchester cartridge drive.

The de facto capacity standard for these drives, set by IBM's PC-XT, is 10 Mbytes. Demand for 10-Mbyte drives is expected to continue very strong, due primarily to the installed base of PCs that may be upgraded by the addition of a Winchester.

"There are over a million PCs out there," says Andrew Roman, Vice President of Marketing for Cogito Systems (San Jose, CA). "Even if 20% of those are upgrade candidates to a 10-Mbyte drive, there's a tremendous market." Add to those the many PC-look-alikes, and the many other small computers that may be upgraded, and the demand is even more impressive. "Our research indidates that the combined industry shipments for 10-Mbyte drives throughout '84 will total easily over a half million OEM units," says Roman.

Despite this optimistic outlook for 10-Mbyte drives, most of the half-height drive manufacturers are prepared for the next de facto standard – 20 Mbytes – set by the IBM PC-AT. Just about every half-height drive manufacturer introduced 20-Mbyte Winchesters at last summer's NCC – just before IBM officially announced their PC-AT, multiuser system, based on a 20-Mbyte disk drive.

When IBM set 10 Mbytes as the "floor" in disk drive capacity by introducing the PC-XT, many drive manufacturers were surprised at how quickly 5-Mbyte Winchesters became practically extinct. Will the AT do the same for 10-Mbyte drives? Probably

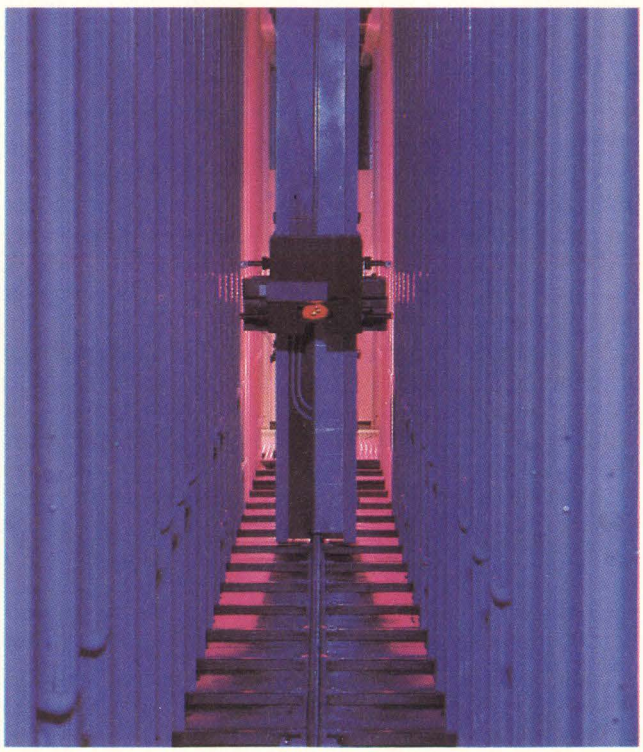
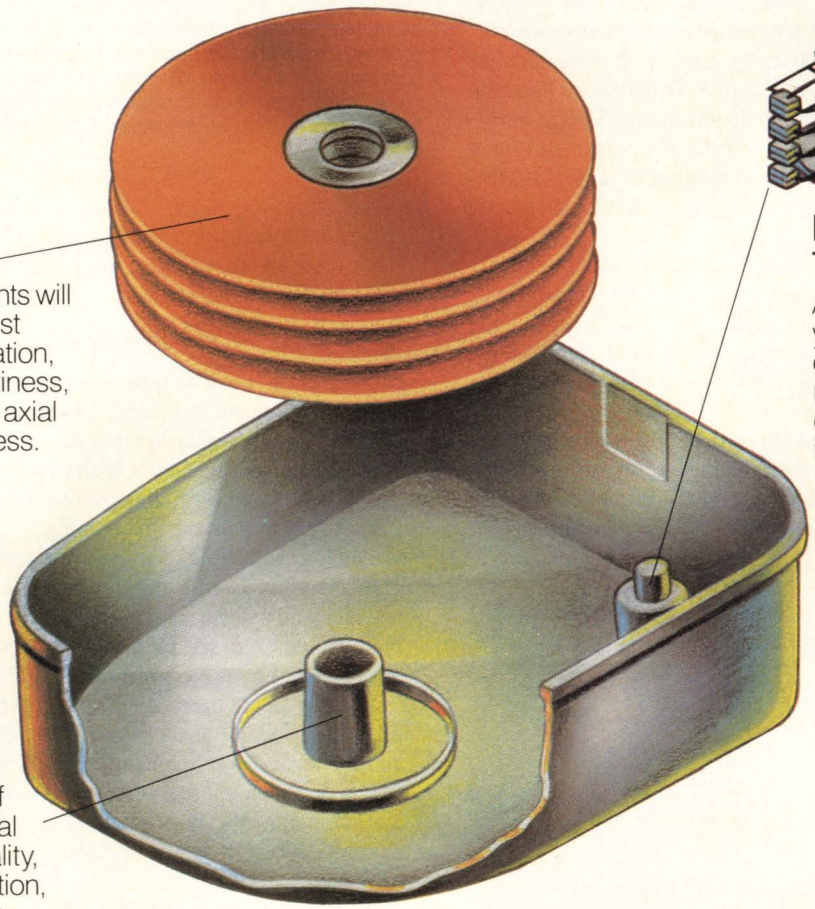
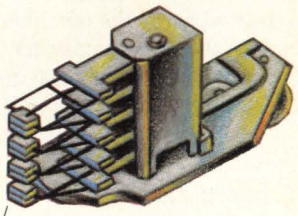


Figure 1: Increased use of automation is improving throughput and quality at many Winchester disk drive manufacturing facilities, and helping to keep more manufacturing plants on-shore. Above, a Litton ToteStacker system moves nearly completed Winchesters through a series of final tests at Priam's new automated manufacturing facility in San Jose, CA.

A CRASH COURSE IN DISK AND DRIVE TESTING:





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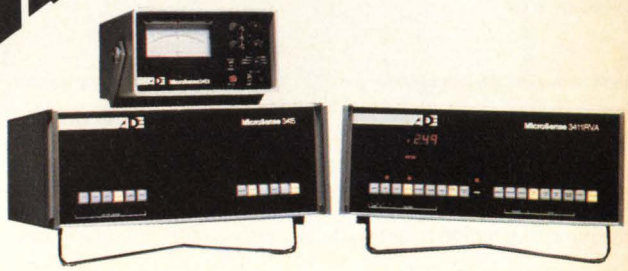

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not, predicts Roman. "10 Mbytes is more than sufficient for a single-user workstation," Roman explains. "20 Mbytes is really aimed at two or three users – and the operating system on the AT is initially for two or three users. So the impact on the 10-Mbyte drives will be negligible."

The half-height drive manufacturers are hoping that the AT will open up a whole new market on top of the XT upgrade market. The large amount of publicity that the AT has received, combined with the ease with which the AT may be enhanced using a variety of hardware options, should result in a flurry of add-on subsystems announced at this year's COMDEX show. Many of these will add value by using half-heights.

"IBM did a very thoughtful deal on the controller," explains Roman. "They made it into an intelligent controller, so that you can download the drive from the controller – you can plug in a variety of different drives, as long as it's a two-platter configuration with four data surfaces. The controller can then quickly summarize what are the parameters of the drive and compensate for it in the operating system software and firmware."

This makes things very easy for a subsystem designer. For example, with regard to disk format, the AT calls for 17 sectors with 512 bytes per sector. The industry standard ST412, developed by Seagate, is 32 sectors of 256 bytes per sector. But since the AT sectoring is soft-sectored, the number of sectors is arbitrary, and can be set by the firmware in the controller; bytes per track may be any multiple of 256.

All of which makes half-height Winchester manufacturers very happy. IBM could easily have made it difficult for the add-on subsystem makers, greatly limiting their market. But IBM plans on becoming the leading force in small multiuser systems – despite any challenge from AT&T – and knows that a large offering of enhancements from third-party vendors will help their cause. Not that IBM plans to let the add-on memory vendors go uncontested – IBM's own enhancements are very competitive. But they've left the door open for companies offering lower volume, value-added subsystems, and, since half-height drives are a key component in such systems, they've created what may turn out to be a sizable market for the half-height Winchester drive manufacturers.

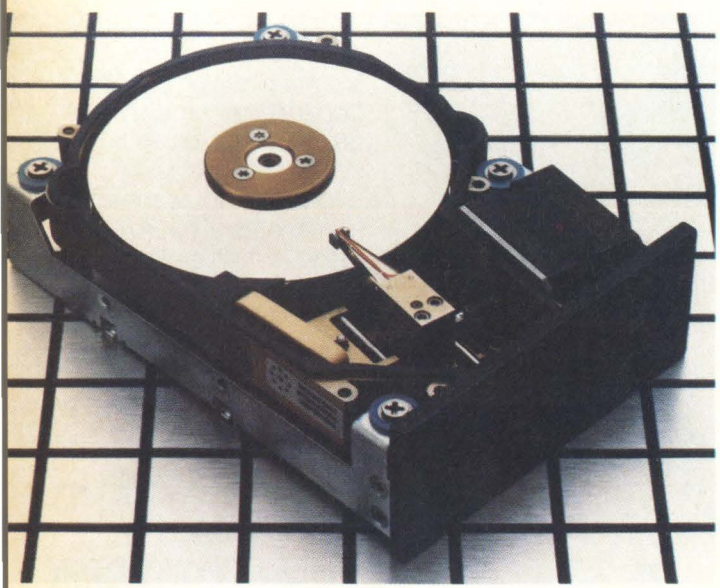

Figure 2: A big future is forecast for small, sub-4" Winchesters, especially those that prove to be reliable in harsh environments. This Microscience drive features plated media, closed-loop positioning and linear actuator to maintain data integrity under adverse conditions.

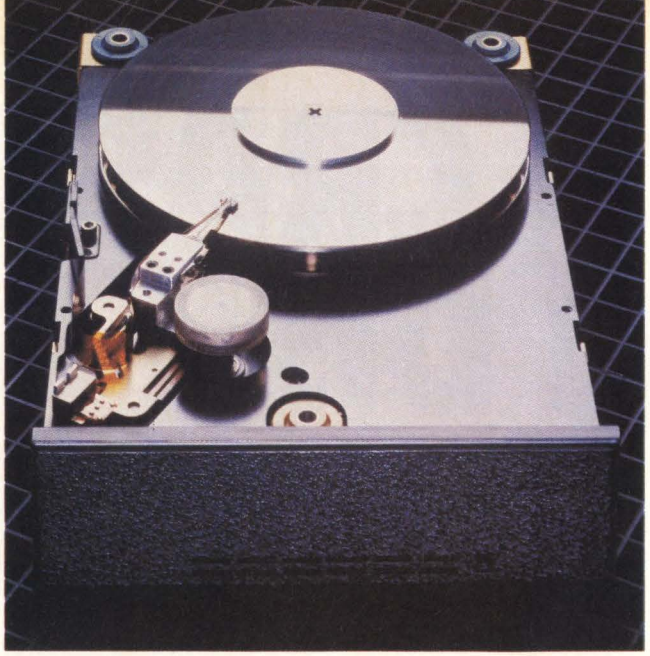

Figure 3: Manufacturers of half-height, 20-Mbyte Winchesters are hoping that IBM's announcement of a 20-Mbyte drive in their PC-AT will create a big market for their drives, just as IBM's PC-XT created a huge demand for 10-Mbyte Winchesters. Cogito's PT925, shown here, is designed for portable applications, and features Whitney-style mini-slider heads, thin film media, and 12-watt power consumption.

The 5¼" Full-Heights

Full-height 5¼" Winchesters today fall into one of two categories: the low performance, low capacity drives built for the personal computer market (primarily IBM and IBM-compatible); and high performance, high capacity drives built for multiuser systems and for memory intensive applications, such as CAD/CAM and image processing.

The low-end Winchesters have become commodity items, cranked out at the rate of thousands per day in Far East factories, and sold at a fraction above cost. The difficulties of competing in this area are apparent from looking at the companies involved in the market. International Memories Inc. (Cupertino, CA), one of the earliest small disk drive manufacturers, went up for sale when they couldn't match tumbling drive prices and still turn a respectable profit. The several other drive manufacturers still competing in this area have shown extreme financial fluctuations – huge profits one quarter, followed by precipitous declines the next. For designers, the positive side of the heavy competition is very low prices on 10-Mbyte drives.

With high-performance 5¼" Winchesters, volume production is the chief problem. While a variety of companies have demonstrated drives ranging from 40 Mbytes all the way up to 500 Mbytes, few have managed to ship them in quantity on schedule. This is because many of the drives require components which are themselves behind schedule in production, such as thin film heads, mini-composite sliders, or sputtered media. In addition, many of the high performance Winchester companies are start ups adept at creating new designs, but less skilled at producing them by the thousands.

8" Drives

8" disk drive technology is a large part of the market, but a rela-

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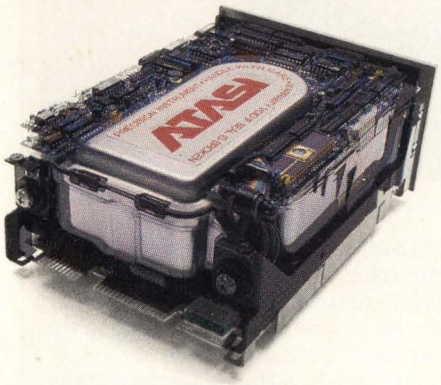
Here's a shocking fact: when someone sets a computer down on a desk, the disk drive inside can be subjected to a pulse shock as high as 30 g's. Obviously, if the disk drive (or any other component in your system) can't handle that kind of shock, your system runs the risk of breaking down under rather ordinary conditions—like every time there's an office shuffle and people move their computers. What follows is some technical information on how we handle the problem in our high performance 5¼- inch Winchester disk drives.

Shock and vibration: twin problems

Shock, and the closely related problem of vibration, have come under intense study at ATASI Corporation, and for good reason: both can cause loss of data. A severe pulse shock can cause a

AN ENVIRONMENTAL IMPACT REPORT.

drive's head to "slap" against the disk, removing a "divot" of oxide material, along with the data written there. Severe vibration can cause the head to overshoot or undershoot a track, so that the head can't find the data it's seeking. In addition, vibration can fatigue components over time, and perhaps lead to premature failure.

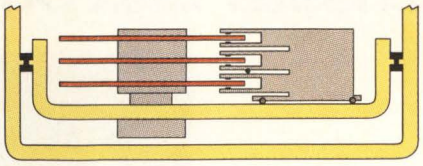


ATASI's 46 Mbyte, 5¼-inch Winchester disk drives are available in production quantities immediately.

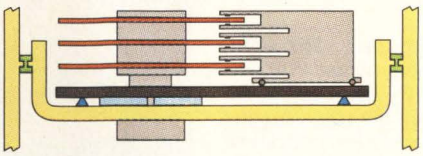
Double shock isolation

In order to sustain high shock loads, the ATASI design incorporates a unique dual system for shock and vibration isolation. Like most disk drives, ATASI drives have isolators between the frame and the head/disk assembly bowl. In addition, ATASI's proprietary design includes elastomere isolators inside the bowl, between the bowl and baseplate on which the head/disk assembly is mounted. A foam pad with high damping properties, also located between the baseplate and the bowl, further protects the head/disk assembly from vibration.

The grommets ATASI uses for isolators are far from ordinary. To handle both pulse shocks and vibration effectively—to avoid a declining spring rate with displacement while maintaining adequate damping properties—ATASI tested 330 different options before making a choice. These tests involved the use of a laboratory shaker as well as computer models.



Most disk drives only have shock and vibration grommets (black) between the frame and the bowl.



ATASI's proprietary design also includes isolators (blue) between the bowl and baseplate.

ATASI's double isolation system more than protects its drives—and the data they store—from the shocks of the office environment.

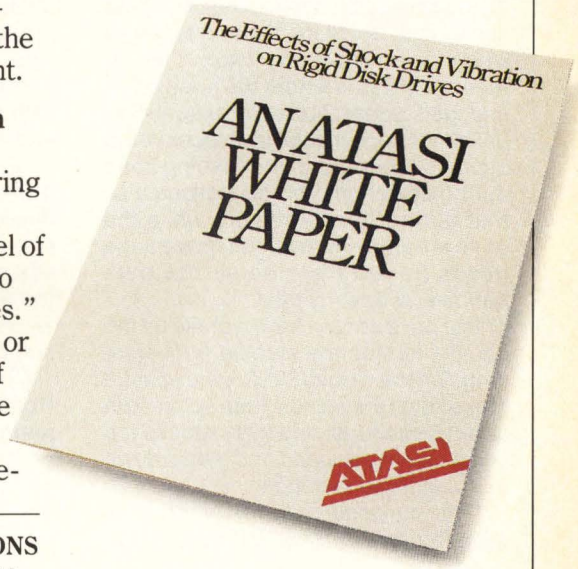
Beyond the shock/vibration problem

Shock and vibration engineering is only one of a number of ways ATASI achieves such a high level of data integrity. ATASI drives also feature dedicated "landing zones." Upon powerdown—intentional or emergency—the back e.m.f. of the motor is used to position the carriage over data-free landing zones. A carriage lock then mechanically holds the carriage in place, protecting the data field from any head contact.

The ATASI White Paper

At ATASI, we are proud of the quality we build into every drive we make, and we encourage clients to test our products rigorously. To help, we have prepared a White Paper on shock and vibration for systems integrators. It discusses test methods and the interpretation of test data in detail.

If you are a systems integrator, contact ATASI Corporation now to receive your ATASI White Paper. Corporate headquarters: 2075 Zanker Road, San Jose, CA 95131, (408) 995-0335; Eastern region: (617) 890-3890; Southwest region: (714) 432-0757.



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CAPACITY	33 MB	46 MB
ACCESS TIME (AVG.)	30 ms	30 ms
DATA RATE	5 Mbits	5 Mbits
INTERFACE	ST 506	ST 506

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MODEL NO.	3065	3075
CAPACITY	65 MB	75 MB
ACCESS TIME (AVG.)	24 ms	24 ms
DATA RATE	5 Mbits	5 Mbits
INTERFACE	ST 506	ST 506

Available second half, 1984.

ATASI

Ruggedizing Winchester Disk Drives

Today's smaller, lighter, lower-power Winchester disk drives are perfect for portable applications. But before specifying a drive for any application which might subject the drive to excessive shock or vibration, system integrators must ensure that the drive was designed for such environments.

There are five key features system integrators should look for when examining any drive intended to withstand rough handling, according to Andrew Roman, Vice President of Marketing for Cogito Systems (San Jose, CA).

1) It should use a Whitney technology 3370/3380 head/spring assembly. The reason is that the loading force on the Whitney head spring is much higher than that of a conventional Winchester assembly — 15 grams compared to 9 grams. The higher loading force presents that much more force to overcome for any mechanical shock and vibration forces that might cause a head crash.

2) The drive should have a head landing zone. This consists of several tracks which do not have any data written on them, and this is where the head stops and rests during power off sequences.

3) The actuator should have a lock which secures the head in the landing zone during power off. This is necessary so that during transportation, while the drive is being shipped and moved, the heads do not traverse across data bands and destroy data.

4) The drive should have a brake on the spindle to stop the spindle from spinning. On the Cogito PT925, the spindle brake stops the spindle from spinning in about 6 seconds, and this reduces the contact between head and media down to about three seconds.

"The purpose here really is not to save the media," says Roman, "but to save the heads, because in that head/media interface, the head is the weaker link in the system."

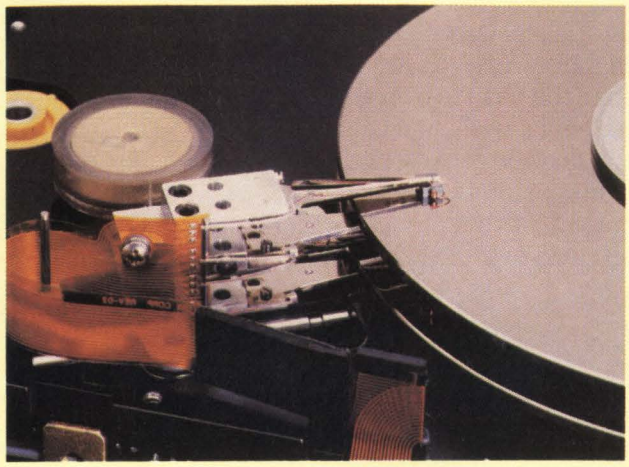


Figure 1: The lightweight, rigid Whitney-style head/spring assembly offers greater resistance to shock and vibration. (Photo courtesy Cogito Systems)

5) Finally, says Roman, the drive must have shock mounts at strategic points on the drive's three axes — one shock mount for each of the X,Y, and Z axes. Shock mounts isolate the head/disk assembly (HDA) mounted in the frame of the microcomputer, or in the memory subsystem, from shock and vibration.

Another related characteristic of a true ruggedized design is that the HDA dimensions should be reduced by several millimeters. This is necessary so that when the shock mounts are installed, the 5¼" footprint isn't exceeded, and also so that the shock mounts will have sufficient sway space to work properly.

Conspicuous by its absence from Roman's list is plated media, which many drive manufacturers insist is a necessity for portable applications. But although Cogito's PT925 uses thin film media, Roman doesn't believe that it is mandatory for ruggedized drives.

"Oxide media, contrary to what some of the plated media people say, isn't that fragile and sensitive. The surface of plain iron oxide media is hard enough to withstand any damage from the head, such as the head touching the surface or nicking it. The one thing iron oxide media does not have which plated media does is that oxide media is a little more sensitive to moisture and moisture absorption."

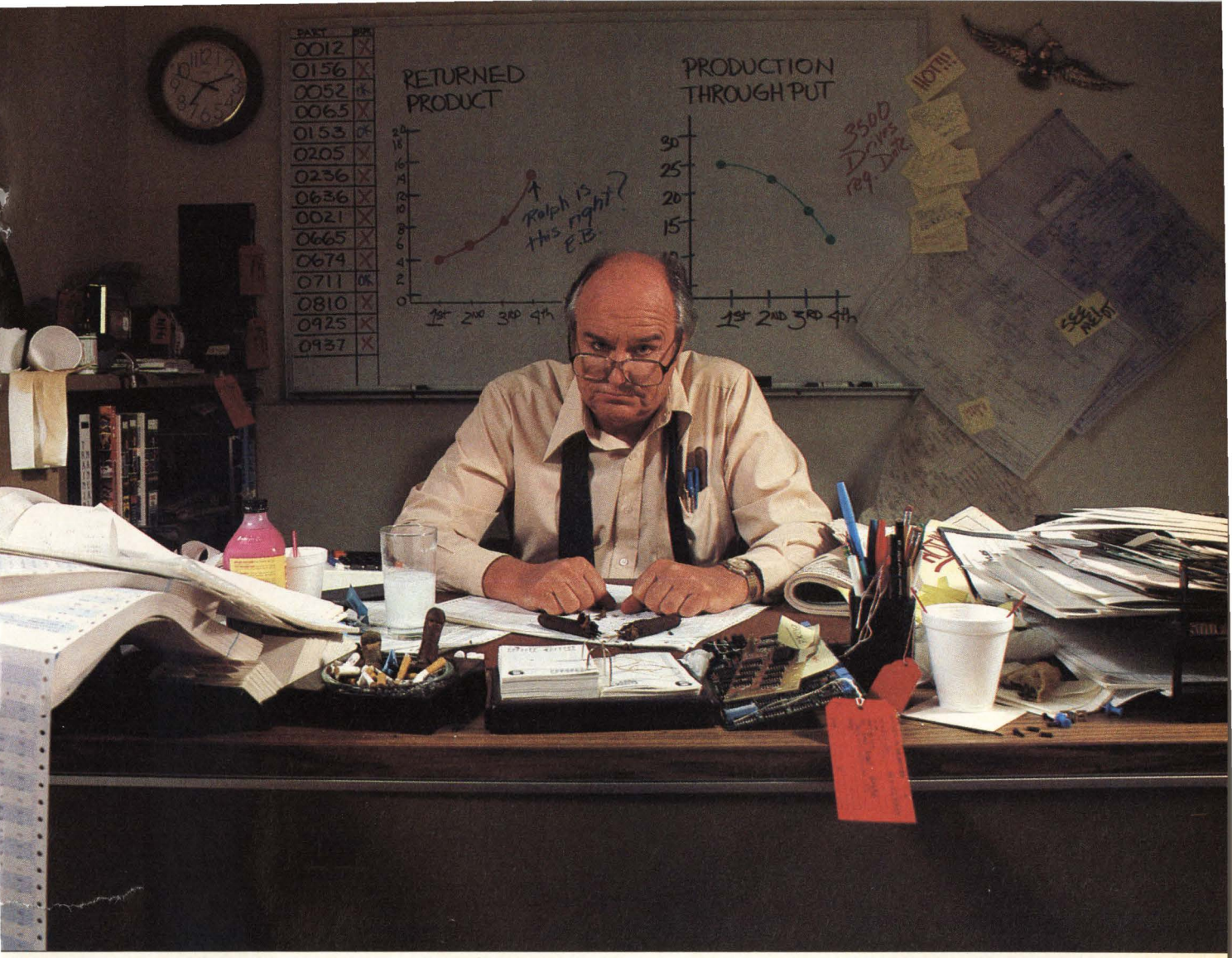
A drive should be able to withstand shocks of at least 40 Gs when in the static, or non-operating, mode, according to Roman. "While the drive is operating and the computer is working, not too many people are going to swing the thing around and jar it against the wall or against the desk," says Roman. "It's in the static mode when you're carrying it to the airport, or throwing it in back of your car, or onto the luggage loading belt of the airline — that's when you want to have your maximum protection, so you've got to have a minimum of at least 40 Gs."

tively quiet one. The only recent exceptions have been Seagate's introduction of a half-height 8" drive designed for small multi-user computer systems (MUMS, short for Multi-User Memory System) and MegaVault Memory's Parallel Random Access Memory (PRAM) MVP212 drive.

MUMS, it could charitably be said, was not extremely well-received. Introduced at last autumn's COMDEX show, it is a 100-Mbyte, high-performance (30 msec access time) three-platter 8" disk drive in a half-height configuration. It was especially targeted for the IBM-PC marketplace, and could be packaged into a subsystem that fit on top of the PC. In conjunction with Western Digital, Seagate also announced a companion controller capable of handling two of the drives. It was based on Seagate's ST412HP high performance drive level interface, and SCSI on the host side.

The biggest reason for the industry's lack of enthusiasm for MUMS was probably lack of a second source. System designers were reluctant to specify a drive that would make them completely dependent on one supplier.

MUMS is significant in that it is the first attempt at using large diameter disks combined with the latest low-mass, low-profile sliders and heads to create a product for the small computer marketplace. Virtually all the attention has been focused on smaller diameter media. Despite MUMS' lack of success, other companies have hinted that they are at least looking into similar projects.



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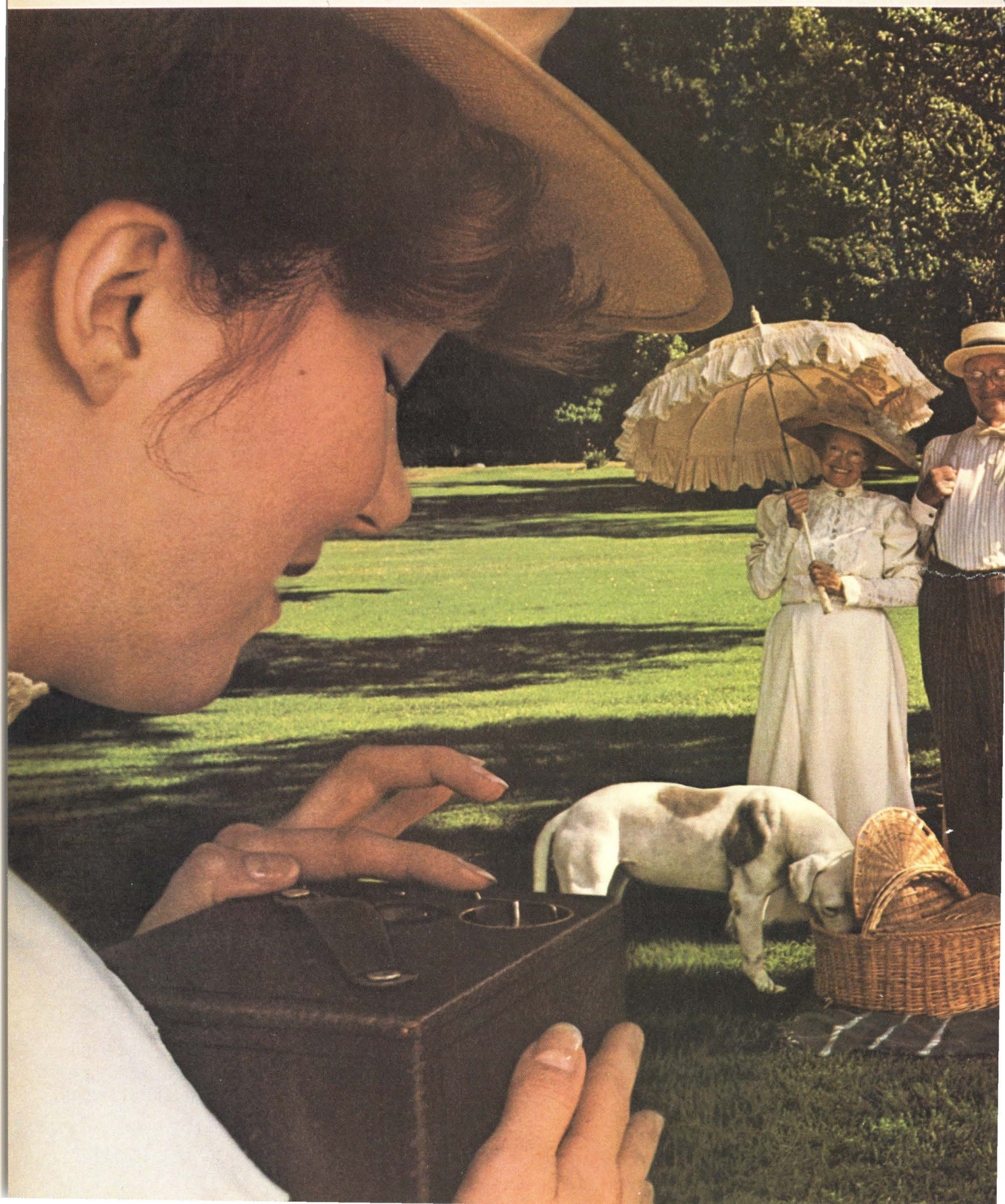

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A hundred years ago, taking photographs meant using a camera the size of a crate, a glass plate holder, a tripod, a darkroom tent and a silver nitrate bath.

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Also, MUMS was Seagate's first ST412HP-based drive. Its poor showing has hurt the interface's chances for survival, and given a boost to the other high-performance drive-level interface, ESDI.

Another development in 8" Winchester technology is MegaVault Memories (Woodland Hills, CA) Parallel Random Access Memory (PRAM) drive. The name may be somewhat misleading; at least one trade magazine described the MVP212 as a "RAM-based drive." However, MegaVault calls it a PRAM not because of any semiconductor memory, but because the drive's eight data surfaces are broken up into two sets of four parallel read/write channels. This allows any read/write combination on four surfaces, increasing the drive's "random access" capability. The MVP212 has an SMD interface, with a data transfer rate of 9.67 MHz. By using all four channels, the effective data rate increases to 38.6 MHz. Intended applications for the drive include computer graphics and image processing, which require large, high speed mass memory.

Large Disk Drives

In the mainframe disk drive market, things have gone pretty much IBM's way. In 1980, they set the pace with their 3380, and they're still doing it today. Even after four years, the plug-compatible manufacturers (PCMs) of 3380-class disk drives are behind schedule, and some are just beginning to ship in volume.

But now that the PCMs are finally getting ramped up, rumors have surfaced that IBM will introduce their next generation mainframes and associated disk drives early in 1985. As if to confirm the rumors, IBM recently cut the price of their current line of mainframes, 3380 drives and controllers, by 10% and more – a practice of IBM's just before the introduction of a new line.

Of course, the announcement of the next generation of IBM mainframe products, whenever it occurs, won't dry up the demand for 3380-class drives by any means. But it will have an affect on the PCMs, as some customers wait for the next models, and as the PCMs are forced to match IBM's price cuts as they occur, eroding the profits on what few drives they have shipped.

Ibis Systems (Westlake Village, CA) is one company that left the IBM plug-compatible market to sell to OEMs (a wise move, in retrospect, when one looks at the difficulties of the companies who remain). Ibis makes a 14" Winchester with 1.4 Gbytes of storage, a data transfer rate of 12 Mbytes/sec, and average access time of 16 msecs. Currently, they are producing them for Cray Research supercomputers.

More recently, Control Data Corp. (Minneapolis, MN) left the 3380-class PCM market, leaving only StorageTek (Louisville, CO), Memorex (Santa Clara, CA), NAS (Mountain View, CA) and Amdahl (Sunnyvale, CA) to compete with IBM. CDC will now refocus their drive efforts on the sub-3380 class OEM market.

Alpha Data (Chatsworth, CA) also produces a drive for the OEM market. Their Atlas stores up to 160 Mbytes, with an average access time of 18 msecs, and an average latency of just 8 msecs, due to the drive's high rotation speed of 3600 rpm. Cylinder size on the Atlas is 1 Mbyte; with proper formatting, this large cylinder size can increase throughput considerably.

During design of the Atlas, Alpha Data determined that 54 heads per chamber was the optimum number for applications with a large number of access commands per second. According to Alpha Data, the Atlas easily handles 50 to 60 access commands per second, while other SMD drives with 5 to 19 heads per chamber become saturated.

Figure 4: While production of low-end disk drives has moved largely offshore, high performance drives can, in many cases, be made efficiently at on-shore automated production facilities. After passing through an automatic testing sequence, Priam drives (above) are shuttled directly to shipping.

As in LaPine's sub-4" drive, Alpha Data's Atlas features retractable heads which never touch the disk surface. This eliminates the need for a dedicated landing surface on the disk and, presumably, greatly decreases wear on the heads.

Media Advances

More and more Winchester manufacturers are using plated media, especially for smaller diameter disk drives. The result is a shortfall in supplies of the media. Currently, Ampex and Tandon's Megastor subsidiary are the two leading suppliers, and both are rapidly increasing their production capabilities to produce over a million disks per year. About two dozen other companies are also gearing up to produce either plated or sputtered thin film media. Still, it may not be until 1986 that they can catch up with demand.

The reasons most drive designers give for using thin film media are thin film media has a higher coercivity than standard oxide media, which translates into higher data density, which in turn translates into higher capacity; and thin film media is somewhat harder than oxide media, making it more suitable for harsh environments in which the heads may get bounced around on the media surface.

Most media manufacturers agree with these pronouncements, and are planning to move increasingly towards thin film media. Dysan (Santa Clara, CA), however, says they have no such intentions. Instead, they have introduced a new sort of oxide media they term "Chocolate," which they claim offers the performance of thin film media at a lower cost.

Chocolate media is cobalt-treated particulate gamma ferric oxide. It has a coercivity of 600 oersteds, compared with 350 oersteds for conventional oxide media. This allows linear density of 15K flux changes per inch (fcpi) and track density up to 1200 tracks per inch (tpi). These densities translate into 20 Mbytes per 5¼" disk, and 40 Mbytes per 8" disk.

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in most applications," claims Bob Johnson, Dysan Director of Marketing and Sales, OEM Products. "Disk drive manufacturers can cut their costs and double their capacity at the same time."

Most industry analysts predict that thin film media will be the dominant media for small disk drives within two years. For their part, Dysan remains somewhat more modest in their predictions. They expect that it will take at least two years for their Chocolate disks to replace plated media.

A different sort of media altogether which may affect both predictions is stretched surface recording (SSR). Developed by 3M (St. Paul, MN), and announced nearly a year ago, the technology was expected to find its way into some Winchester designs at this year's NCC. Drive manufacturers, however, postponed their announcements until later in the year, or early 1985.

SSR uses flexible disk media stretched over a plastic substrate, just as a drum head is stretched over a drum. The taut but resilient surface combines excellent recording characteristics with high resistance to damage from contaminants, claims 3M.

Perhaps even more significant is that plastic SSR disks can be manufactured for a fraction of the cost of standard disks. "There's nothing in that fabricated structure that should cost more than fifty cents," says magnetic media consultant Laurence Lueck (Magnetic Media Information Services, Chicago, IL). That won't stop 3M from selling the disks at a predicted price of $5 each in OEM quantities, but this is still a substantial savings over conventional disks selling at $20 to $100 each. And since media, especially in multi-platter drives, is a large part of Winchester's total cost, SSR could significantly reduce drive prices – if and when the technology is proven and accepted.

The Evolving Market

Regardless of whether or not SSR becomes accepted as a media for Winchesters, it provides an insight into the volatility of the disk drive business. Just that single technology, affecting only one aspect of the Winchester's design could have profound affects within three years. It could cut the price of drives by 10% or more, and greatly alter the plans of manufacturers heavily committed to other media. Since, unlike other Winchester media, it is suitable for removable applications, it could reverse the current trend forecast by many industry observers away from removable media Winchesters – a reversal which would, in turn, have an immense impact on current removable media, such as flexible disks and tape, and on future removable media, such as optical disks.

Of course, SSR may prove to be unviable as a media technology, for some unforeseen reason. But dozens of other research projects in every area of Winchester design have equally profound possibilities. Some, like sputtered media and vertical recording, have received considerable attention. Others are under wraps, waiting for a surprise introduction at an upcoming trade show. At the same time, developments in non-Winchester technologies are threatening to turn technology forecasts upside down. Most Winchester manufacturers are anxiously waiting for the announcement of a product based on erasable optical technology – a development which many Winchester makers fully expect will signal the decline of Winchester drives. Skip Kilsdonk, Marketing Manager for Maxtor (San Jose, CA) sees it as a repeat of the contest twenty years ago between core memory and semiconductor memory. "Every year, the core memories would get cheaper and smaller and keep chasing the semiconductor memories. And I think that what we're looking at here is the same thing. I don't think that anyone would doubt that in the long term it's going to be optical rather than magnetic."

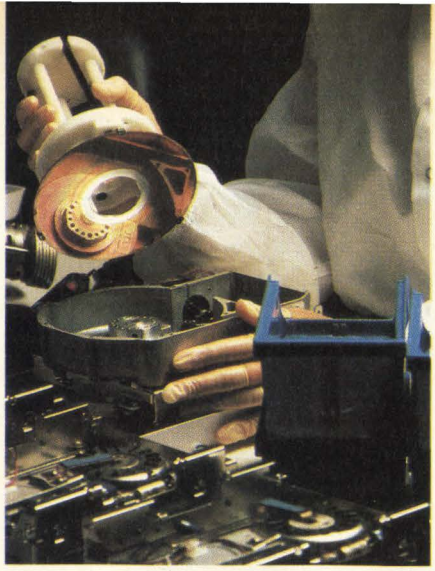

Figure 5: Despite the growing demand for thin film media, iron oxide disks, like this one being installed into a Seagate 5¼" Winchester, are still the most popular media for rigid disk drives in all size categories. (Photo courtesy Seagate Technology.)

At the low capacity end, semiconductor memory may affect Winchesters. As cost per bit decreases, RAM cartridges with integral batteries to refresh the memory may provide a Mbyte or more of very fast memory for portable and other small computers. Sinclair Research Ltd. is developing such a product using wafer scale integration, and other companies are planning offerings which use conventional RAM technology, once cost per bit declines sufficiently.

All of which makes things very difficult for anyone looking forward five, or even three, years. It has never been easy; no 1979 forecaster could have begun to predict where, for example, 5¼" Winchesters would be in 1984, in terms of either market or technology. But today, with so many variables from so many magnetic and non-magnetic technologies, even three-year predictions are shaky.

"Three or four years ago, you could look out on the planning horizon, and you had a reasonably good idea where you had to be two years from now," explains Kilsdonk. "Only when you got into the four or five year horizon did things get a little bit fuzzy. In terms of specific products, it's not that clear anymore."

But although long term product planning has become nearly impossible, current Winchester technology already is sufficient to keep pace with short term demands. "We can take a two-platter design to over 100 Mbytes," asserts Cogito's Andrew Roman. "Of course, that would involve thin film media and thin film heads. But every year we technically can keep on doubling what we've done so far: we've gone from 12 Mbytes to 25 Mbytes, and we can go from 25 to 50, and 50 to 100 later on."

The one certainty in the industry is that the demand for mass storage will continue to increase. While the product mix is unknown as well as the impact of new magnetic technologies in the short term and non-magnetic technologies in the long term Winchester drives as a whole will continue to satisfy the largest portion of that demand for at least the next few years. DD

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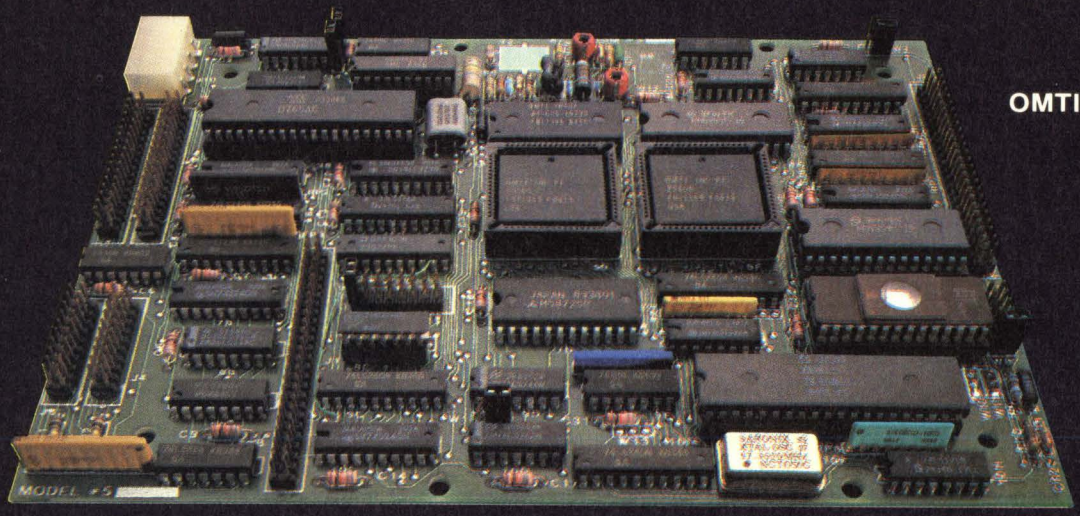

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Advances In Signal Processing Drive Speech Recognition Developments

by Mary Rose Hanrahan, Associate Editor

The advent of computers that can carry on a coherent, if not stimulating, conversation with its user may still be a long way off. Although speech synthesis and recognition are closely tied as research topics, the challenge presented by speech recognition has proven more difficult. With computers of the late 1980s expected to speak and listen, making decisions on grammar, syntax, and contextual meaning, speech recognition must evolve toward the knowledge-based systems that are developing along with advances in artificial intelligence. Currently, speech recognition processes are exploiting the well-defined technologies of adaptive filtering techniques, statistical analysis, and other communication theories, and the refinement of these techniques that lead to further advancement of the recognition process. The most recent breakthrough for speech recognition systems is a dramatic reduction in cost, driven by advancements in semiconductor technologies.

The Verbex Series 4000 Voice Recognizer. Users insert a voice cartridge containing their voice patterns and the application vocabulary.

In speech analysis for synthesis, parameters are derived from natural speech. These parameters are chosen to be ones which have some correspondence to the more perceptually significant aspects of speech, such as the short term magnitude spectrum of the spoken word. In speech synthesis, these parameters are used to control a synthesizer which produces speech. In speech recognition, these parameters are compared with other sets of parameters representing words to be identified.

In contrast, acoustic recognition is based on perceptually significant differences between words. As one would expect, classes of parameters that are good for synthesis are also good for recognition. Typical of such parameters are reflection coefficients, rectified and smoothed bandpass filter outputs, formants, and Fourier transform magnitudes. Some features that are critical for proper production of speech, such as pitch, however, must sometimes be ignored for the identification of words. **Figure 1** illustrates the basic comparison of a)the speech analysis/synthesis process, b)acoustic recognition of speech, and c) a model of speech understanding.

Speech recognition carries its own host of problems, depending on the input method. Isolated or "discrete" input requires that an utterance is followed by a timed pause in order for the voice pattern to be matched accurately by the processor. Continuous or "connected" input contrasts with the isolated method in that the words are strung together in a continuously flowing phrase. In both types of systems a constraint is placed by the bit

An in-depth understanding of human speech production and perception processes as well as high level computing and mathematics are necessary for signal processing designs.

rate, or number of samples taken per second when capturing voice data for further reconstruction. A higher bit rate insures the accuracy necessary in speech recognition systems. Present systems operate in bit rates ranging from 4,800 to 14,400 bits/sec.

Once a signal is captured, the pattern must be matched by the processor. Another difficulty in speech recognition is time registration. If a reference word is uttered normally and then repeated with one of the syllables stretched out, allowing the rest of the word to remain the same, the comparison of corresponding spectral qualities yields a bad match. Researchers devised the "dynamic time warp" to counter the problem. This algorithm warps the time axis of the waveform to give the best match to each reference. The "distance" factor is important in pattern matching. It is the part of the template(digital representation of vocal input) matching process that measures distance between waveform peaks of a voice input and the same word stored in memory. Pattern matching algorithms measure the total distance between peaks for the two words. If it falls within specified and adjustable "recognition" limits, a match results. Thus an essential voice processor function in word recognition or speaker verification modes is dynamic programming pattern match. Although computationally intensive, it allows for variations in the way people talk. Dynamic programming provides superior discrete word recognition, primarily based on proprietary algorithms, as longer, more complex words are now recognized.

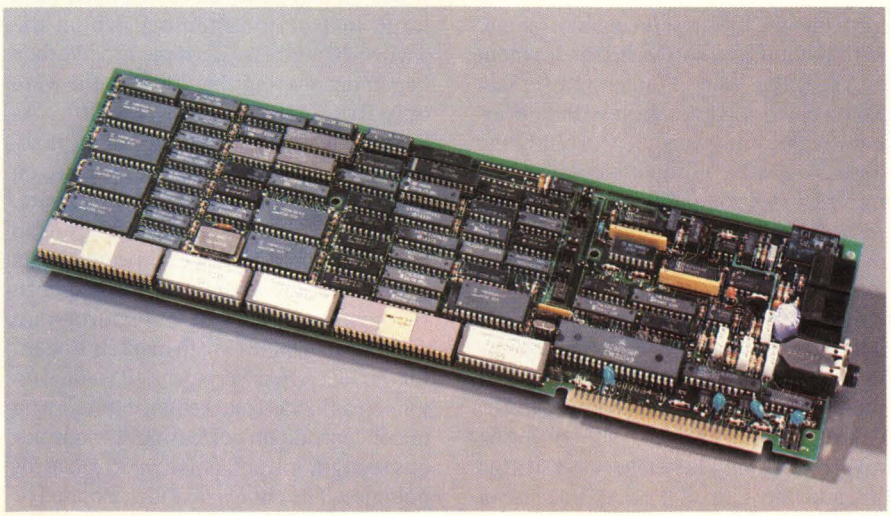
Speaker Dependence Vs. Speaker Independence

Speaker dependent recognition systems recognize previously trained words from a particular user's private library of word templates, with the user selecting a limited amount of vocabulary words. Training is accomplished by speaking the intended words into a microphone one or two times causing the digitization and storage of voice patterns, to be later matched when running the relevant application program. A speaker independent system recognizes a wide range of speakers without prior training and development of individualized vocabularies through the use of a universal word template.

Presently the vocabularies are predetermined by the manufacturer, and remain at the primitive level, usually consisting of numbers zero through nine, yes/no, and other simple words. The most apparent application of speaker verification systems has been in extensive voice print analysis for security use. This "verbal fingerprinting" works by merely reciting a name or password into a microphone. The vocal input is uniquely characterized by the spectral qualities of the speaker's voice. To check for a match, this voice print is compared to a voice print library stored in memory. Speaker dependent systems are "trained" by a user reciting an applications-oriented set of vocabulary words which are digitized, compressed, and stored.

System Solutions

Speech system architecture requires flexibility and expandability to adapt to the wide range of user environments in which voice I/O technology is being applied. The demand for more memory is ever increasing with some speech boards being comprised of over 60% memory. Speech recognition system manufacturers have started marketing total solutions to speech recognition requirements, ranging from custom speech chips to speech boards for PCs, to high level recognition systems. Votan (Fremont, CA) has incorporated voice recognition, speech compression, and complete telephone interfacing facilities on a single voice processor board, the VSP 1000, which replaces their former configuration requiring three boards. The VSP 1000 is based on the Multibus and allows the user to speak in normal conversational flow, in a continuous speaker dependent mode. A word spotting capability enables the system to pick out words in its vocabulary which are located anywhere within a stream of normal conversation. As described previously, speaker independent recognition capability is also available as an option,



Votan's VSP-1000 board.

for the digits zero through nine, yes/no, and custom vocabularies.

Digital signal processing is performed by Texas Instruments' TMS-320 and control functions are handled by a Motorola 6809 processor. As in most systems of this type, custom LSI chips perform proprietary pattern matching functions. Voice processor boards are controlled by means of a voice control block located in system memory which contains control parameters and data pointers for recognition templates or buffers for compressed speech. The voice processor reads the control block in system memory and then transfers the needed data into its local memory. Results of the function are transferred from local memory into system memory, and completion is signaled with an interrupt to the system processor. The system processor may be any single board computer (8- or 16-bit) which interfaces to the Multibus. Votan also supplies a Multibus compatible system processor board using an Intel 8086 specifically designed for controlling voice applications.

Interstate Voice Products (Orange, CA) makes their own chip set to be used as building blocks for speech recognition systems, which is capable of recognizing 100 words or short phrases, and expandable to 200 words using additional RAM. With the VRC100-2 (**Figure 2**) speech input is analyzed by a 16-channel spectrum analyzer within the speech preprocessor and converted to a digital representation of the characteristics of the spoken input. This digital data is then converted to a fixed-size pattern that preserves the information content of the spoken inputs while discarding redundant features. During word training, these patterns are used to derive reference templates for each vocabulary item. The templates are then used in the recognition process for comparison with incoming words. Vocabulary templates are stored in an external RAM, while the processing algorithms are contained in the recognition/control program (EPROM).

Verbex (Bedford, MA) recently introduced at Autofact '84 a continuous voice recognition system in which users simply insert a voice cartridge containing their voice patterns and the application vocabulary. The Series 4000 (**Figure 3**) is actually a VLSI-based peripheral that adds speech recognition capability to any PC, micro, mini, or mainframe host computer system. Although based on speech recognition technology first implemented in the Model 3000, the 4000 is Verbex's first entry into the low-cost recognition arena. With the aid of a software development package, the Voice Planner, a user can create custom application vocabularies and user training scripts. Currently the 4000 is IBM PC compatible with plans for DEC VAX compatibility soon. Essentially the Series 4000 is dumb memory and emulates an ASCII keyboard; the voice pattern is the key and the 4000 cartridge is capable of holding 100 words of continuous voice. Translation is done by an Intel 8088, while the TMS-320 recognizes speech patterns. According to Dr. Mike McCallig, Director of Engineering at Verbex, it was chosen because "it's the first and only chip of its kind. Because of the requirements spectral analysis imposes on a system, there is a need for a large instruction memory which the TMS-320 addresses." At the time Verbex began developing the 4000, there were only five TMS-320 chips available. As the chip becomes more prevalent, however, predictions are that systems based on signal processing chips will proliferate.

IBM PC plug-in voice recognition boards are an offshoot of advancements in speech technology, and most speech recognition system manufacturers are now offering them. Votan markets a board for the PC, while Verbex has hesitated on joining a flooded marketplace, preferring to concentrate on perfecting its continuous recognition and noise rejection technologies. The choice to utilize isolated or

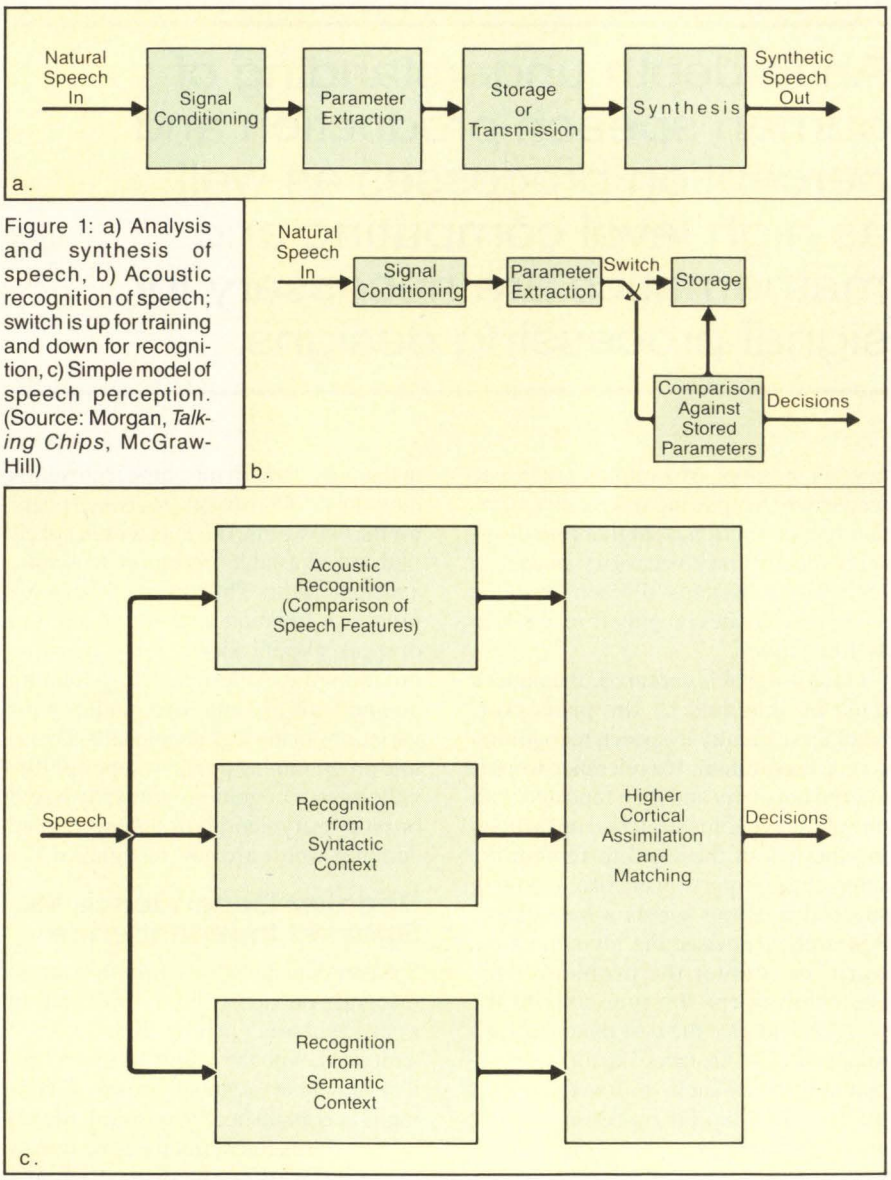


Figure 1: a) Analysis and synthesis of speech, b) Acoustic recognition of speech; switch is up for training and down for recognition, c) Simple model of speech perception. (Source: Morgan, *Talking Chips*, McGraw-Hill)

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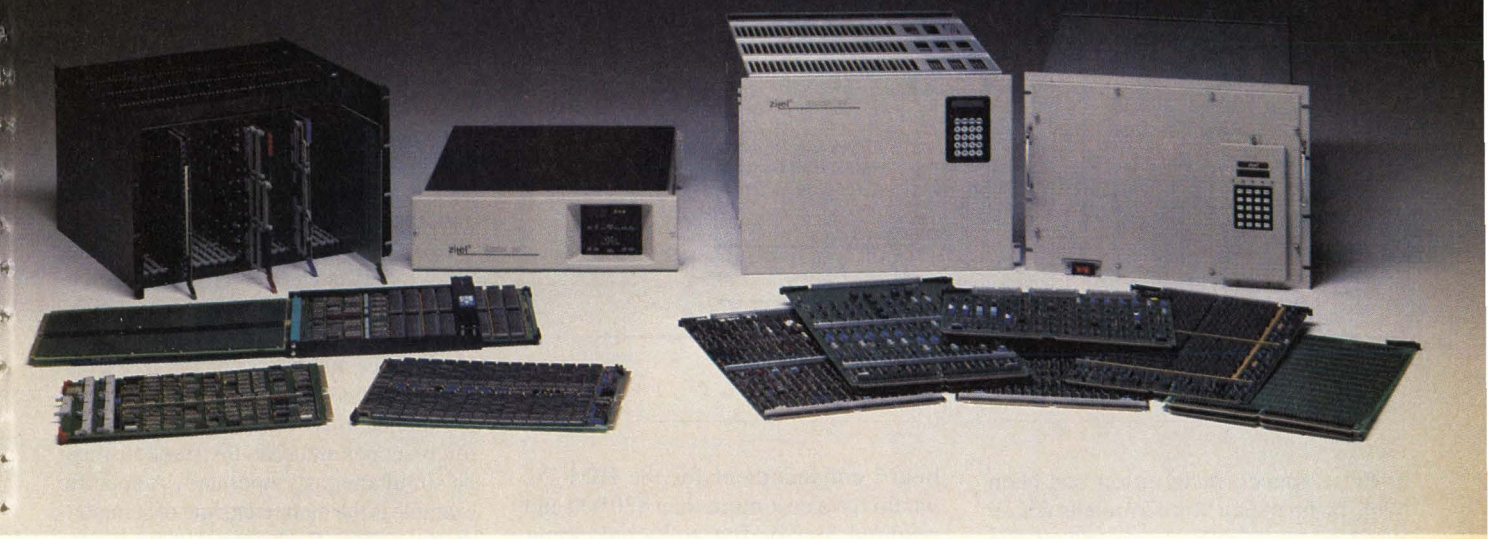

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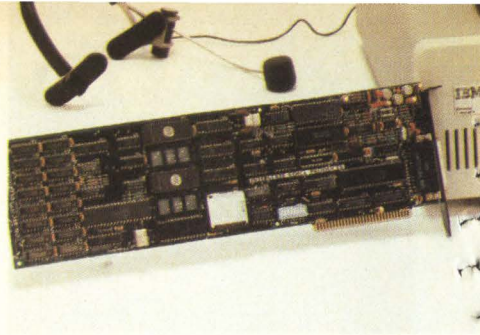

Interstate Voice Products' speech recognition board for the IBM PC.

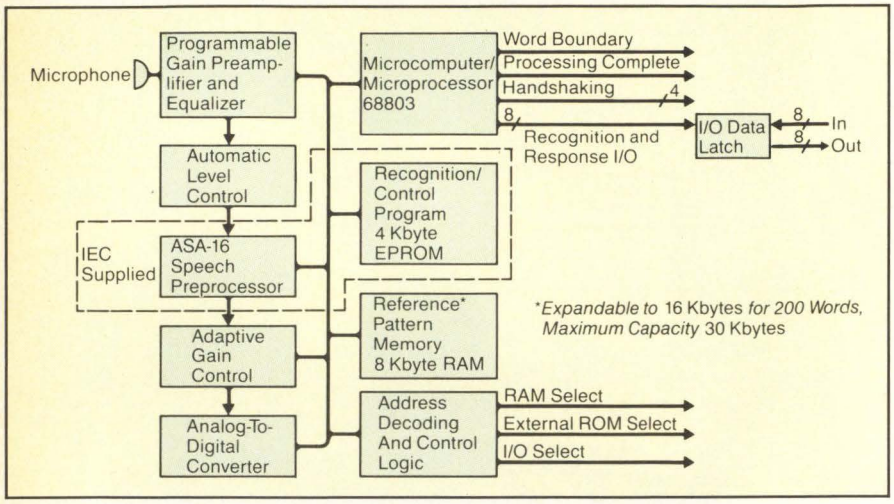

Figure 2: Interstate Voice Products' VRC100-2 simplified block diagram.

discrete speech recognition has been made by Interstate Voice Products whose VocaLink product line incorporates voice recognition chips, boards for the IBM PC and XT, and self-contained voice recognition systems. Interstate's latest market entry, a 240-word vocabulary speech recognition board for the IBM PC, can be integrated with off-the-shelf software. According to Sam Viglione, company President, the price of real-time voice recognition systems with vocabularies large enough for effective use has been brought within reach hundreds of productivity-increasing applications. "Just a few years ago, the voice system which we have incorporated on a $1,650, single-board enhancement for the IBM PC would have cost more than $20,000 and required four or five full-sized circuit boards."

The SRB (Speech Recognition Board) from Interstate based on an Intel 80186 controls the sampling, analog-to-digital conversion and data transfer.

Application Areas

Choice of recognition technology depends upon the nature of the application, number and characteristics of the user base, and the amount of control or security needed. Opportunities for speech recognition or voice I/O applications are grouped into five major horizontal markets: data entry and retrieval, remote transaction processing, messaging, equipment control, and security. Current and anticipated vertical markets are in the areas of finance/banking, manufacturing, retail/merchandising, medical and scientific as well as office environments. Speech recognition really came into prominence in the "busy hands/busy eyes" environments such as inventory taking, or lab applications in which test equipment, microscopes and scan instruments must be simultaneously operated. A specific example is the manufacturing of semiconductor wafers. Each chip is inspected for defects through a high power microscope while the operator notes the type of defect along with brief comments as to its nature and likely source, all through a voice I/O system.

Future Trends

Speech understanding systems differ somewhat from recognition systems in that they have access to and make effective use of task-specific knowledge in the analysis and interpretation of speech. Speech perception is the next frontier for manufacturers of speech systems, incorporating not only analysis and recognition, but defined sources of knowledge and symbolic representation of speech signals within a given context.

An in-depth understanding of human speech production and perception processes as well as high-level computing and mathematical ability are necessary for any design with its basis in signal processing. Speech recognition systems' ultimate goal is that of speaker-independent handling of connected speech which provide contextual clues to word recognition. **DD**

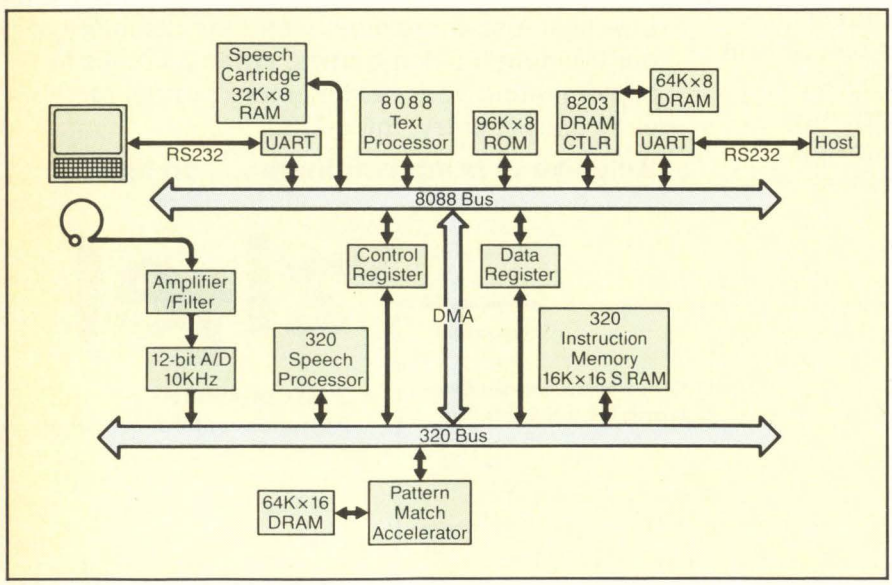

Figure 3: The Verbex Series 4000 block diagram.

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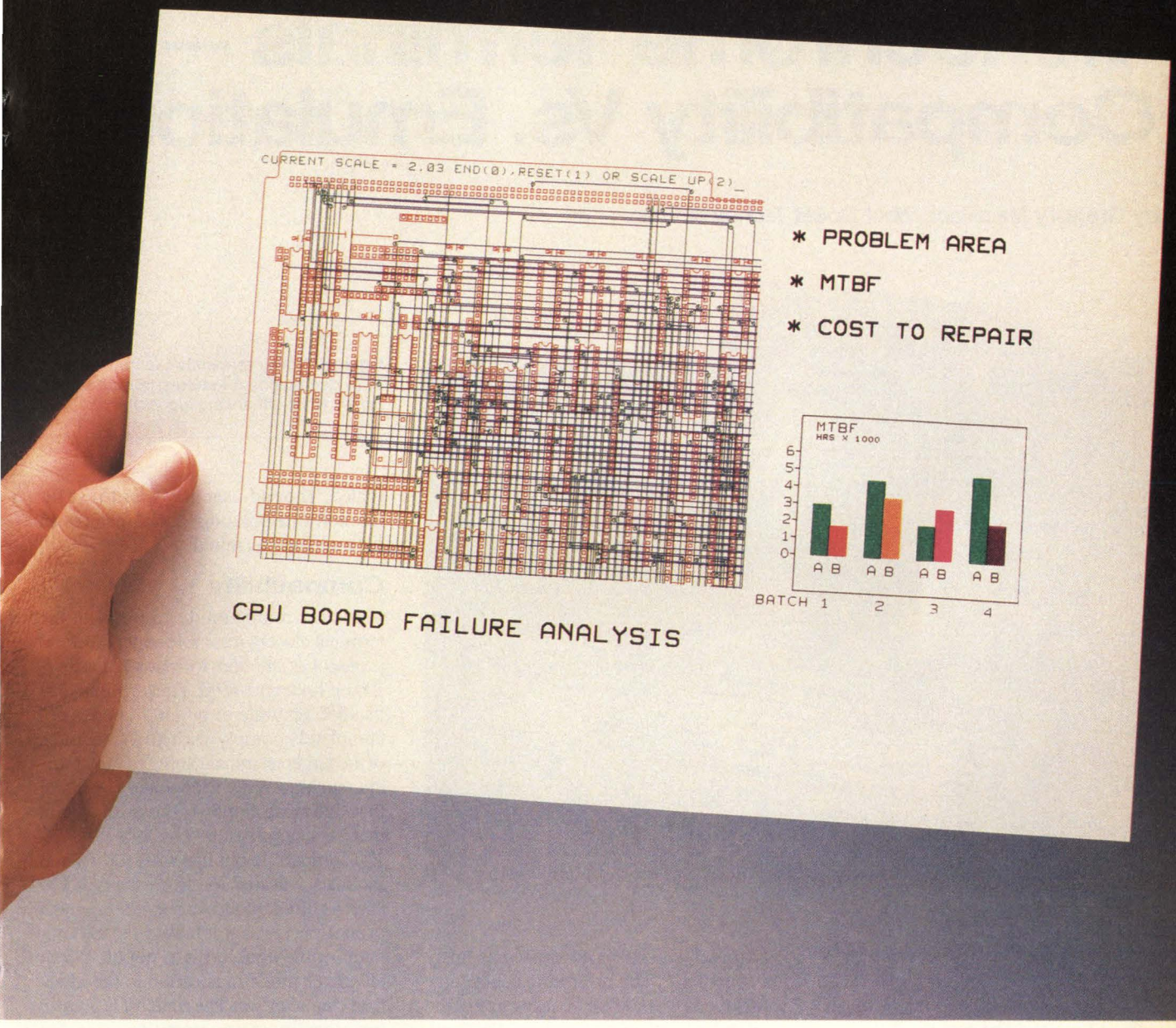

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INSTRUMENTS

Monochrome Terminals — Compatibility Vs. Emulation

by Gregory MacNicol, West Coast Technical Editor

Figure 1: Newer terminals like the 924 from Televideo combine features from other terminals while enhancing ergonomics.

With over 180 terminal manufacturers, one might think it would be easy to select a suitable terminal. This is not the case. The competitive pressures on monochrome terminal manufacturers are not only creating higher performance terminals at lower costs, but a dizzying array of choices, specs and features that few people can effectively evaluate. Even after all the comparisons are complete and the choices are narrowed down, one problem may be invisible until the user runs into it after purchase. While the specifications indicate "software compatibility," the terminal may not be 100% compatible, and some application programs simply won't work properly.

An example that has often been repeated illustrates the seriousness of the problem and how the issue may be hidden until suddenly encountered. A user is currently running a program on a new terminal which was advertised as "truly compatible." The program, a data entry form, has worked for years on any of the other 20 terminals in the office. Suddenly the screen of the new terminal is filled with underscores mixed with letters and then scrolls upward. What has happened is that a feature called "non-embedded attributes" was not fully emulating the original terminal. Underscoring occupies one character, so three times as many characters are on the screen, alternating between underscores and letters, making the program unreadable. This may have been the only program using this feature, and it may have been an important one. The missing feature that defines the difference between compatibility and emulation could unexpectedly create disaster.

The words "emulation" and "compatibility" are critically important for OEMs and systems integrators designing systems for end-users looking for add-on capabilities after a system has been integrated. The end-user may wish to use future software utilizing special features on the emulated terminal.

Compatibility

The term compatibility means that the terminal closely resembles operation and protocol of another format such as VT-100 or Tektronix 4010. The terminal may be 95% accurate or better, but does not completely comply with all the features of the target terminal. Some manufacturers, such as Wyse (San Jose, CA), feel that following trends is more important than strict emulation. The WY-75 is VT-100 compatible but has a 14" screen and includes features found in the VT-220 such as block mode, editing keys, and a printer port. What it lacks in total compatibility is double-high, double-width character mode in addition to the alternate character set. The tradeoff is greater functionality at a competitive price, for absolute emulation.

Televideo (Sunnyvale, CA) has also taken the approach of optimizing original functions while adding more. Their 922 is VT-220 compatible but has more functions than the DEC counterpart. It offers a low profile keyboard, a tilt and swivel screen, a 10 key accounting pad, eight character fonts, and a space for an auxiliary graphics board. After agonizing over whether to emulate the VT-220 keyboard, Televideo decided against DEC's use of the Rainbow microcomputer version. Instead, Televideo chose a layout that users were more accustomed to—the VT-100. The placement of the "escape," "break," and "shift" keys are where most typists expect. An optional graphics board can upgrade the 922 to match DEC's VT-240 monochrome and text ter-

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Modgraph

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The difference between emulation and compatibility can spell disaster to an OEM.

minal in addition to performing Tektronix graphics functions. The versatility and functionality is more advanced than an emulation of the VT-220.

One reason some OEMs choose compatibility over emulation is because a terminal may have the capability to closely resemble many terminals at once. Ampex (Redneck City, CA), for instance, makes a terminal that is compatible with 18 other terminals. Multiple compatibility not only can provide access to applications programs written on different terminals but can also make operations possible within multiple environments. It is becoming more common for installations to have more than one operating system and to use different application programs that depend on the intelligent qualities of a particular terminal.

Compatibility can be important with regards to appearance. The psychological impact that a familiar terminal has on productivity has been clearly documented. Consistency of working tools is an important factor in maintaining efficiency, even down to the same color scheme.

Emulation

Emulation, on the other hand, means 100% identical operation in every way, of the target system. The user should not be able to notice any difference in operation, including the feel of the keyboard.

Use of the term "emulation" can not only be misleading but can mean entirely different things to different people. To some, it denotes total functional compatibility. To others, it may mean identical effect of keystrokes. To add to the confusion, some functions listed in a manufacturer's manual may differ from the terminal's operation.

Emulation terminals can range from the basic "dumb" terminal to sophisticated multifunction enhanced versions. Some manufacturers add more features, saying that the terminal is 150% accurate because there are additional features that enhance the terminal. Some of these features are emulations of other terminals, higher communication rates, additional function keys, and bidirectional ports while still retaining true compatibility. One company added a feature that eliminates a problem on an emulated terminal that users complain about, a noisy keyboard. The solution was to add a volume controlled click generator that could be set by the user. But, in all other regards, the terminal emulated the original.

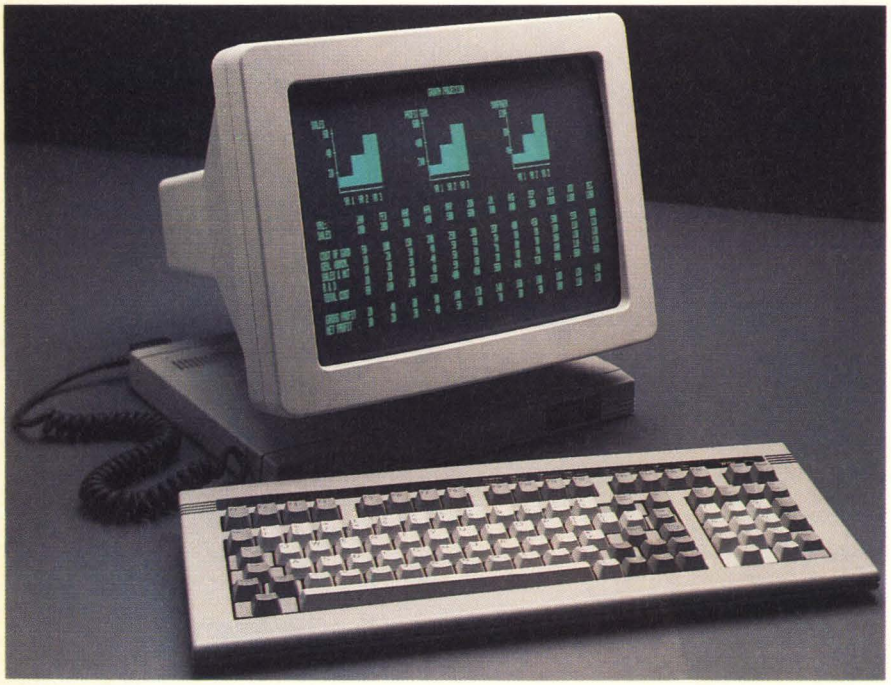
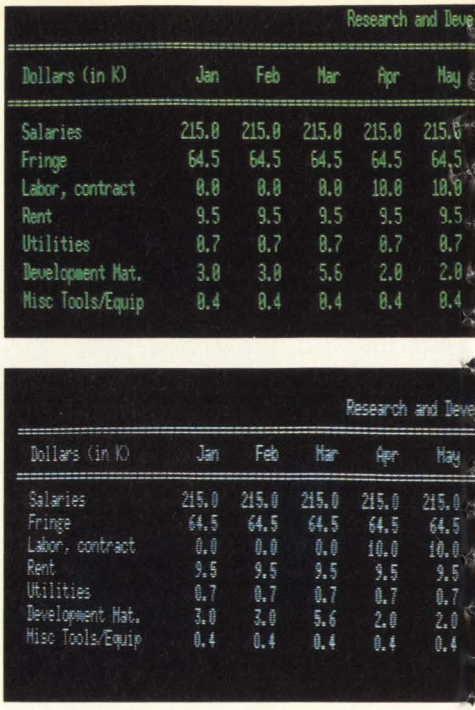


Figure 3: Wyse has chosen compatibility over 100% emulation for a better price/performance ratio.



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Utilities	0.7	0.7	0.7	0.7	0.7
Development Mat.	3.0	3.0	5.6	2.0	2.0
Misc Tools/Equip	0.4	0.4	0.4	0.4	0.4

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Utilities	0.7	0.7	0.7	0.7	0.7
Development Mat.	3.0	3.0	5.6	2.0	2.0
Misc Tools/Equip	0.4	0.4	0.4	0.4	0.4

Figure 2: Graph-On (top) enhances the quality of emulating DEC's (bottom) terminals by increasing vertical resolution to 390 scan lines in contrast to DEC's 240 lines. Increased clarity of the 132 column mode is the result.

One reason for choosing an emulation terminal is its upward compatibility. While the terminal might be emulating another terminal now, ergonomics, more memory, and many enhancements make the terminal useful for a longer time. It may fit the need for a badly backlogged machine and still be targeted at tomorrow's replacement offering many more features. Emulation is important if the terminal is expected to perform predictably as a system expands into new applications. An OEM may avoid obsolescence by providing customers with routes to allow new technologies to be incorporated with fewer expenses.

Some of the so-called standards are really emulations of other terminals such as the DEC VT-100, VT-52, VT-102, VT-220; Televideo 910 and 925; Adds Viewpoint; Lear-Siegler; and Hazeltine. The monochrome terminal industry is not driven by technology but driven by marketshare, and the terminals that are being emulated are the result of sheer volume, the most popular being the DEC series.

(continued on p. 87)

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PRODUCT INDEX

To help you find the products that you need, we've compiled a subject index of the ads and new products that appear in this issue. Organized by general product area, the listings include the name of the manufacturer, the page on which the product appears and a write number for additional information on that product. Bold type indicates advertised products.

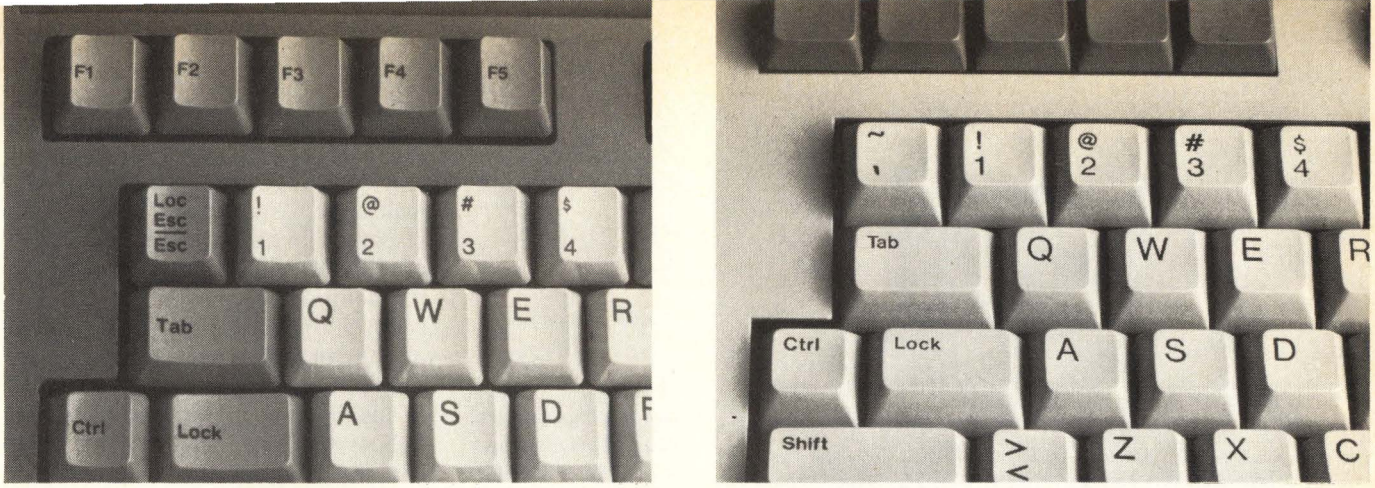

Figure 4: DEC (left) changed the position of the escape key on the newer VT-200 series. Televideo (right), opting for user familiarity with the VT-100 series, decided to retain the escape key position of the VT-100 on their 922, rather than fully emulate the VT-220.

(Continued from p. 80)

Emulation can be difficult even for companies that emulate themselves. DEC has a mode on their VT-220 that emulates the VT-100 but not 100%. Users claim discoveries of the VT-100 emulation while running specific application programs that typically run on the VT-100.

An example of a company that has dedicated itself to 100% emulation is Falco (Sunnyvale, CA). One of their latest products, the Fame II, has the capability of emulating the Televideo 925, DEC VT-100 and VT-52, and includes the additional extended memory feature of the 925. It includes a 25th line for status and 50-user programmable non-volitile function keys with 900 bytes of storage. Eight terminals make up the Falco product line, each having perfect emulation of set standards. One standard, the ANSI ×3.64, is becoming popular, especially in relation to DEC terminals, specifically the VT-100. Recently, the popularity of the VT-220, with long lead times and an increase in price of $100 is causing this terminal to be emulated by other manufacturers.

The difference between compatibility and emulation is often highlighted in advertisements. One company states total VT-220 compatibility but lacks the 132 column display mode. This means many of the popular spreadsheet programs will not work properly. Other advertisements refer to a VT-100 "mode." This means that the terminal responds to cursor control sequences, but may not execute proper characters. A serious buyer should rely on more than advertised specifications of the terminal before considering purchase.

Qume (San Jose, CA) is another company dedicated to 100% emulation. The QVT-102 was their first terminal and can emulate the Televideo 910, Lear-Siegler ADM3 and 5, Hazeltine 1500, and a powerful native mode. All other Qume terminals such as the QVT 103, 108, and 109 are each addressing a distinct market emulating other terminals in addition to adding enhanced features. What is unique about Qume is their incorporation of additional ergonomics and a pleasing design to their line of terminals. Another important issue is speed. Some terminals can emulate satisfactorily but are limited to a slow baud rate. Qume has maintained emulation at the popular 19.2K baud.

It is interesting to note that emulating most or all of the popular terminals is not realistic. The internal architecture, bit-mapping scheme, and artifacts from prior technologies make it nearly impossible to incorporate all of these features on one terminal.

Standardization

The American National Standards Institute (ANSI) has helped erode some of the standards problems. Both users and manufacturers benefit from ANSI implementations in terminals which eliminate obsolescence. Because of the broad acceptance of the standards, users can be assured their terminals will remain functional for years to come. Many of the ANSI recommendations refer to cursor positions, such as "home cursor," as defined by escape sequences. If ASCII can be considered words, then these sequences act like grammar.

DEC (Maynard, MA) led the way in standardization years ago by being the first to implement the ANSI ×3.64 standard. The terminal was so well received that the company couldn't meet the demand. As a result, a new market opened up with second sources. In addition, the VT-100 is often used as an equivalent for the ANSI standard.

As terminal technology advances, new functions will become possible, but will more than likely use the ANSI mnemonics. The remaining problem is which of the newer models using the ANSI standards use subsets and supersets of the standard. The problem in the past was that terminals with the same functions had different ways of invoking these functions. This makes it difficult for different terminals to communicate with each other.

Ergonomic features are not just for looks. The DIN (Deutsches Institut fur Normung) standard specifies the features that increase operator productivity. The standard calls for low profile, sculpted keyboards, and visual attributes that makes it easier for operators to work with a terminal eight hours a day. American terminal manufacturers must be conscious of the DIN standards if they want to sell in Germany because terminals must comply with the standard after January 1, 1985.

Figure 5: Qume's commitment to emulation on the QVT-103 also combines ergonomics and special native functions.

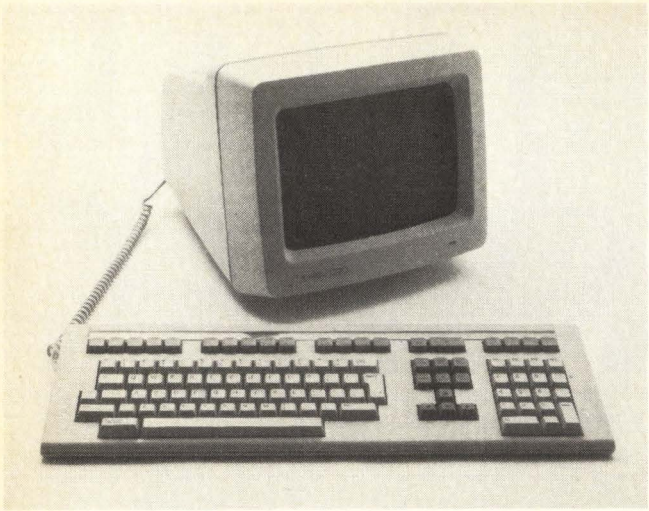

Figure 6: The DEC VT-220 text-only terminal is the newest successor to the VT-100, which is easily the most emulated terminal in the industry.

The Graphics Picture

Emulation of graphics functions on monochrome terminals can be more critical than alphanumeric terminals. There are more complex routines with subroutines that interact with each other. In addition, the investment cost of graphics terminals is greater.

The most popular emulations are modeled after Tektronix, such as the 4010, 4012, and the 4013 modes. Even DEC is emulating some of these modes in their VT-240 and VT-241. Although most emulations are running at a lower resolution than the Tektronix 1024 × 790, these terminals are used as inexpensive alternatives or as previewing devices for existing programs that run on mainframes, minis, and some micros. The emulation is important for running PLOT-10 and advanced software packages such as DISSPLA, SASGRAPH, TELL-A-GRAF, and DI-3000. The emulation must work in every way including subtle physical qualities such as actual screen size which relates to aspect ratio. Circles should look like circles, not ellipses.

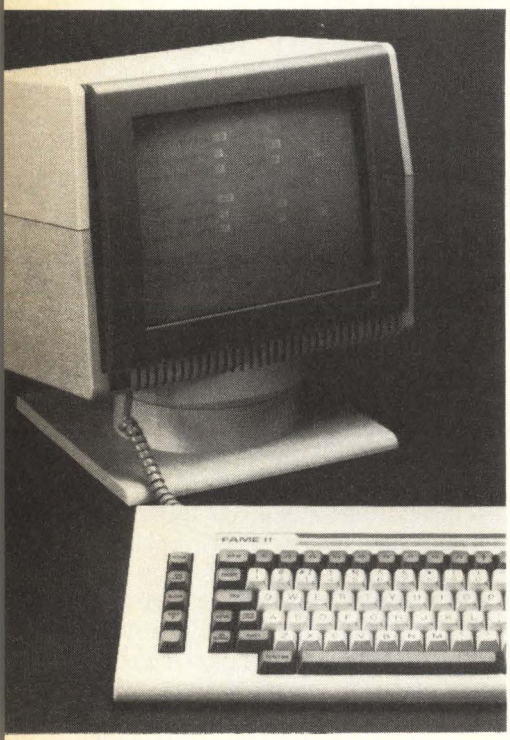

Figure 7: From the beginning, Falco has made a commitment to 100% terminal emulation.

Graph-On (Santa Clara, CA) makes a true emulation of the Tektronix series in addition to emulating the VT-100 and the VT-52. The GO-140 has additional enhancements such as reverse screen, selective erasure, block fill for large areas to be filled, erased or highlighted, and programmable function keys. 512 × 390 pixels are bit-mapped for a 4:3 or 1:1 aspect ratio. This aspect ratio is an exact scaling of 1:2 of the 4010, still preserving the correct aspect ratio. Although other terminals emulate the 4010, an odd size may produce difficult software modifications, aliasing problems, or unclear characters. Emulations with lower vertical resolution have a problem in producing 35 rows of lower case characters with descenders, and have difficulty displaying the APL character set of the 4013. An important feature is the ability to execute all of these functions at a reasonable rate, in this case 19.2 K baud. Having accurate interfacing with popular graphics packages, the GO-140 also interfaces with popular printers for direct graphics output.

Some of the strict emulation codes are obsolete or impossible to implement. One command on the Tektronix allows defocusing of the image. This command is often interpreted as an additional feature or ignored.

Graphics terminals that emulate 4010 and 4014 modes are aimed at engineering and CAD markets and a smaller business market. Modgraph (Waltham, MA) makes the GX-1000 with 1024 × 780 resolution for high resolution emulation of 4010/4014 with a 15″ display screen. In addition to 100% emulation, the terminal adds some features that are not possible on a vector display such as block erase. The terminal is typical in addressing the trends in newer terminals by having a DIN standard ergonomic design, printer port, digitizing tablet port, and a port for a mouse. VT-100 emulation is also possible. VT-200 lacks 100% emulation in omitting the reGIS graphics mode. Henry Kunicki of Modgraph indicates, "We haven't had one customer ask for it yet." The lesser resolution, GX-100, has two pages of 768 × 585 resolution also on a 15″ screen. The display has the unique quality of being able to subtract or add one image with another.

Tektronix 4010/12/15 emulation is offered in high resolution by Cybernex (Ottawa, Ontario). 1024 × 780 pixel resolution creates very clear images that lower-resolution devices lack. One of several additional features of the 4010 is a 9 Kbyte communications buffer which allows information to be stored in the terminal temporarily during graphics execution.

The Future

As terminal manufacturers scramble to satisfy a demanding and cost conscious marketplace, there will be some predictable trends. Ergonomics will play a vital role and incorporate features that will become standards of their own. But more importantly, standards such as ANSI, GKS, and NAPLPS will be used as guides to create greater functionality and versatility in emulating terminals, emphasizing long life.

Emulation is important for user familiarity and correct operation of application programs. As designers of terminals realize the importance of these two qualities, more features directed to the support of these functions will be implemented. In the meantime, it is the buyer's responsibility to earnestly evaluate a terminal's specifications and operation completely to avoid a catastrophic surprise later. DD

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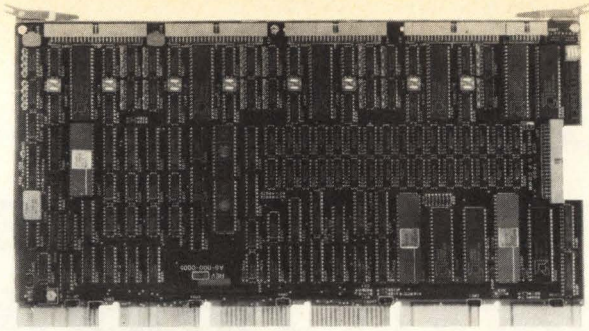

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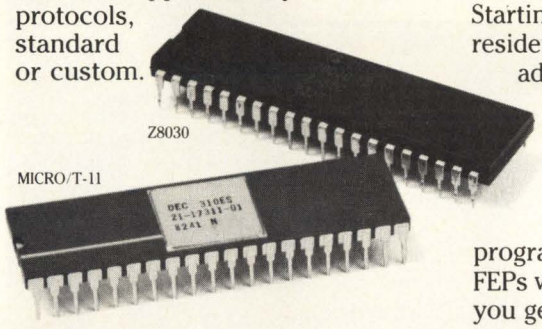

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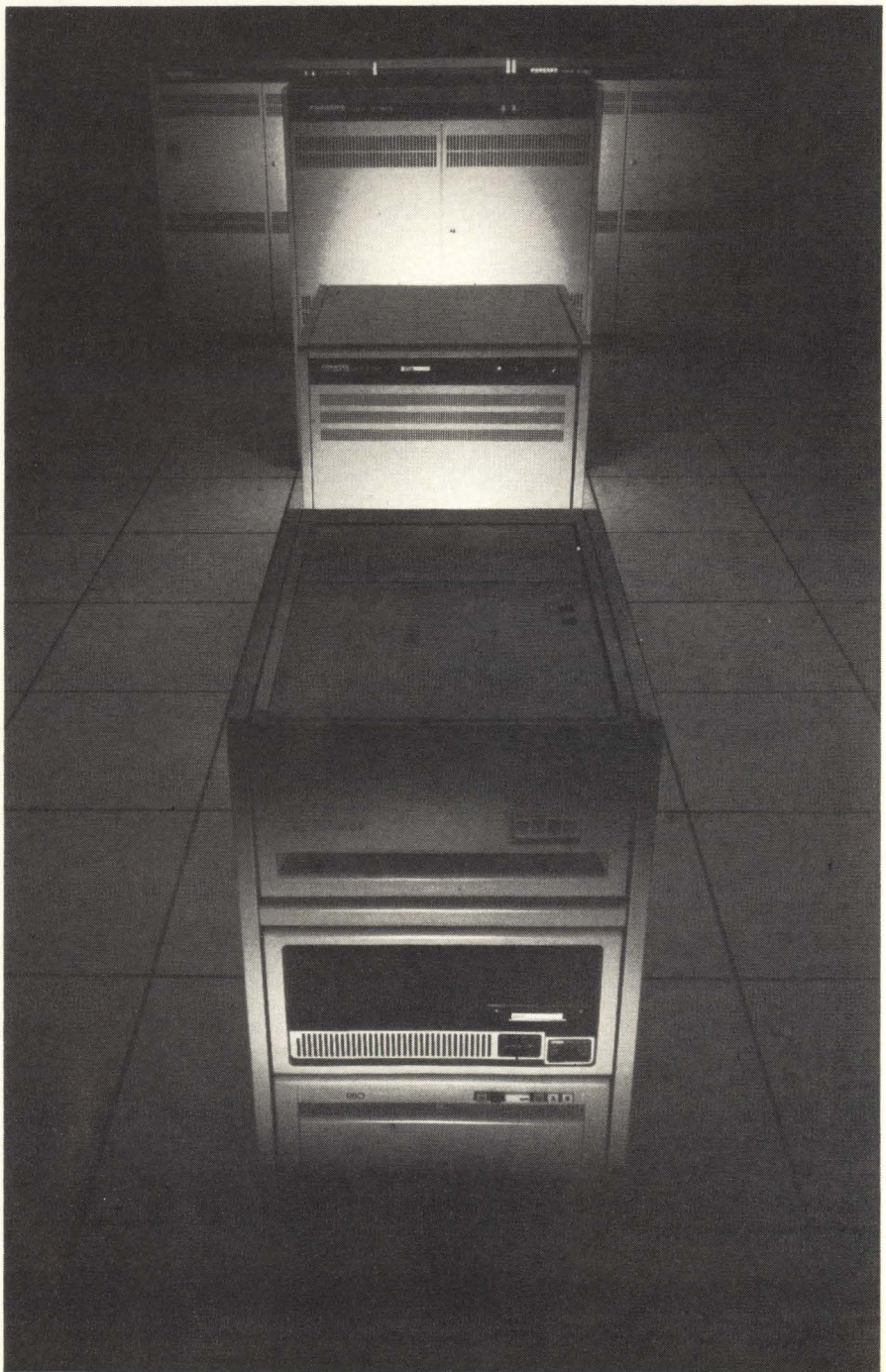
CPU Architecture, Part I: Problems And Limitations Of von Neumann Computers

Although DEC's VAX is undoubtedly an excellent piece of engineering, it too suffers from the von Neumann bottleneck.



by Ronald Collett, Technical Editor

All of today's commercial mainframes, superminis, minis, supermicros and microcomputers are based on the architecture defined some 30 years ago by mathematician John von Neumann. Using this architecture as a reference point, computer designs can be classified as either von Neumann or non-von Neumann. Although there are many derivations of the von Neumann style, the basic configurations still hold the same structure. As demands placed on today's computers continue to grow, the question arises: will these machines be capable of meeting future computing needs?

What is the problem with today's computers and why are researchers striving to develop alternate architectures? The answer is that all von Neumann computers contain the so called von Neumann bottleneck which strains computational performance. Simply stated, the von Neumann bottleneck is the channel of communication where instructions and data sequentially pass back and forth between the processing unit and the global memory (**Figure 1**).

Further examining the von Neumann bottleneck reveals two prevalent characteristics. First, during program execution, a central memory is used to store data and instructions while the program continuously updates the memory. Second, a program counter informs the processor of the memory location that holds the next instruction scheduled for execution. This method of centralized program control limits the performance of the computer.

This breach in performance is due to the sequential nature of the instruction decode mechanism. In other words, even

Until now, computer designs have been based on von Neumann architectures, but can this architecture keep pace with tomorrow's computational demands?

though many portions of a program could be executed simultaneously, this parallelism is never exploited. For instance, a von Neumann computer evaluating the expression $x=(2\times2)+(3\times3)$ would first multiply the term (2×2), then (3×3) and finally add the two terms together. Although the two terms could be evaluated concurrently, the sequential nature of the von Neumann computer does not allow this to happen. Some von Neumann computers, however, attempt to exploit parallelism by using several processors or pipelining, but they can be very tricky to implement and do not really solve the problem. Cache memory is also used to reduce the bottleneck, but it too can create some problems.

With this in mind, decentralizing program control is the key to eliminating the inefficiencies of the von Neumann architecture. This is, in fact, precisely the goal of a data flow computer. Unlike von Neumann computers, data flow machines are not driven by sequential lists of instructions. Instead, data (operands) flow throughout the system in search of instructions. When all of the operands for an instruction are available, the instruction is accessed and executed. The end result is a computer that is data driven as opposed to instruction driven.

Computer architects have long been aware of the von Neumann bottleneck which has led to the design of many computers that try to reduce or remove this narrow channel. The most successful computers that seek to circumvent the von Neumann bottleneck and exploit parallelism contain: multiple processors, cache memory, instruction prefetching and pipelining. By examining some of the best attempts at improving computer efficiency as well as the problems with these designs, there is little doubt that the von Neumann architecture is the crux of the problem.

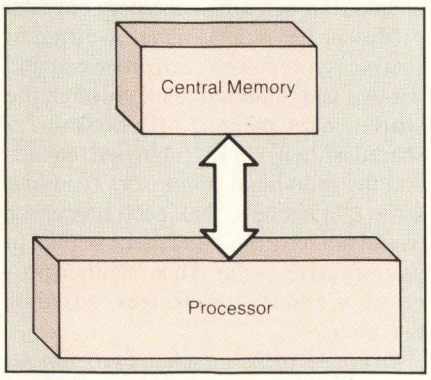


Figure 1: The link between the processor and central memory of a von Neumann computer is known as the von Neumann bottleneck.

Multiprocessor Computers

Computer systems that have several processors make a bid to exploit parallelism, but when the computations become too demanding, the task of synchronizing the various processors, as well as sharing data between resources, becomes overwhelming (**Figure 2**). When programming a multiprocessor system, both write-write and read-before-write race conditions can be potentially crippling problems. Write-write race conditions occur when two processors try to write data into the same location. By using a run-time check algorithm, however, or perhaps some other software, this problem can be avoided. On the other hand, such a problem does not exist in a data flow machine because updating a variable's value in a data flow functional language has no meaning.

The second race condition, read-before-write, is far more serious. To illustrate the problem, consider two routines running on two different processors, both accessing a uniform two dimensional array of numbers. One processor is sequentially creating and writing the elements into the array while the other processor is waiting to read the elements. If the processor reading the elements tries to access data before the data has stabilized (or before the data has even been written) the result is either an incorrect value read or perhaps a system crash. To avoid this condition, the entire array can be written before attempting a read operation. Although this solution avoids the synchronization problem, it fails to utilize any type of parallelism.

Synchronizing each row or each column before attempting a read operation is a more common approach which constrains parallelism less but increases overhead. Synchronizing the two processors on a per-element basis is another approach, but it is extremely difficult. This approach is also impractical if synchronization takes more time than storing an element.

This read-before-write problem has been somewhat oversimplified. Consider the increased complexity if the elements are created and accessed in a non-sequential manner or result in a non-uniform data structure. Unfortunately, with a von Neumann computer it is usually necessary to sacrifice parallelism for proper read-write synchronization. With a data flow machine, parallelism need not be compromised for synchronization.

Memory Latency

Memory latency, the time between issuing a memory request and receiving a response, is another major problem of von Neumann machines. As the number of processors and memory elements in a computer increase, the average memory request latency lengthens (**Figure 3**). This is caused by the finite bandwidth of each memory element and the fixed memory request rate of the processing elements. As a result, when several processors are requesting data, the memory units may be unable to respond to a particular processor's request without causing a processor to idle.

Allowing each processor to issue multiple memory requests in succession without intervening memory responses is one scheme to eliminate this problem. If we assume this is possible, then it is also necessary to assume that contention may cause memory responses to arrive out of order, unless certain constraints are put on the memories and network interconnections. According to computer architecture researchers at the Massachusetts Institute of Technology (MIT), the problem of being unable to issue many memory requests before receiving responses is unsolvable for a scalable (i.e. computer systems that allow processing units to be added or removed) multiprocessor system unless some assumptions are made about program behavior; such as the distance between processors and memory units remaining constant. A recent report from

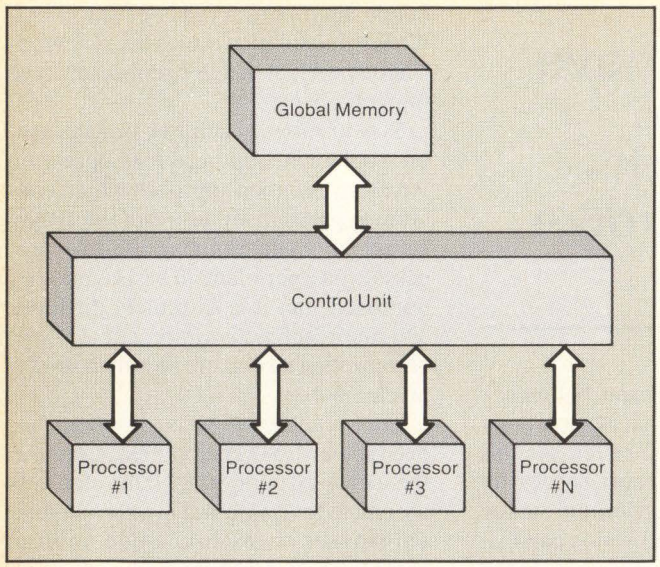


Figure 2: In theory, using multiprocessor von Neumann computers to exploit parallelism seems viable. In practice, however, synchronizing the processors and sharing data becomes very difficult.

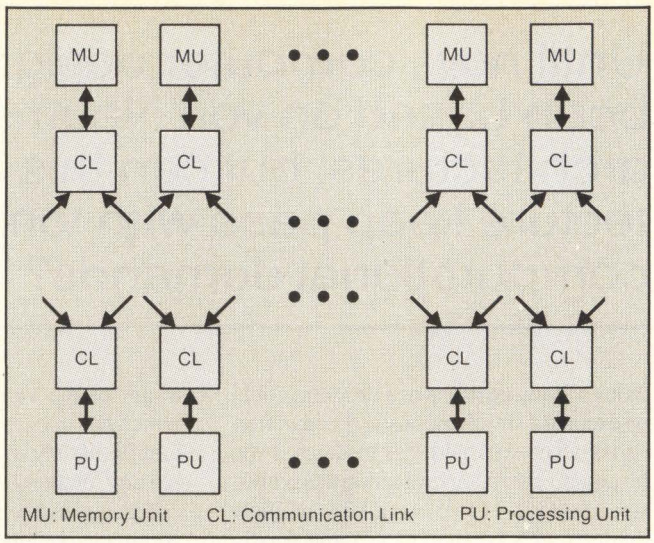


Figure 3: In a scalable multiprocessor system, memory units and processors can be added by simply plugging them together. Increased memory latency, however, is one of the problems with scalable von Neumann machines.

MIT, however, claims that this assumption is both unwarranted and unjustifiable.

Low level context switching, another effort aimed at tolerating memory request latency, allows the processor to undertake a parallel task while waiting for the memory to respond. Again, the goal is to increase parallelism without increasing memory latency. This is possible only if the context switching itself does not generate memory references. By duplicating (in hardware) some of the processor's registers, the processor can switch between different computations by accessing the value held in particular register that relates to that particular computation. For example, a processor could have several accumulators and depending on the particular task at hand it would access the proper accumulator, while the other accumulators would contain the data for the other tasks (**Figure 4**).

For single processor systems, such as the Symbolics 3600 (Cambridge, MA) processing system, the scheme works well. This machine uses microcode-level context switching to allow CPU resource sharing by the I/O device adapters.

The overall objective, however, is to create a truly scalable machine so that as the computation's parallelism grows, additional processors and memory can be added to meet the demand. Unfortunately, complexities drastically increase when this scheme is applied to a multiprocessor environment. Although both multi- and uniprocessor systems are based on duplicating state information, the single processor system needs only a finite number of separate contexts. In other words, for a fixed number of processors the memory latency value can be predetermined and thus the amount of available time for parallel computing is known.

To create a scalable multiprocessor system requires an unbounded number of separate computations and duplicate registers. As memory is added to such a system, the processor-memory communications network expands. As a result, the number of contexts to be maintained must be increased to match the lengthened memory latency time. And if the number of processors also increases, the housekeeping problems become even more unmanagable.

Instruction Prefetch and Cache

Instruction prefetch and cache memory attempt to utilize spatial and temporal locality, respectively. The spatial locality theory basically states: if a particular instruction or piece of data is accessed, then other required instructions or data are probably located in nearby memory locations. Instruction prefetch buffers rely on this principle since the inherent sequential nature of von Neumann machines assures some degree of locality. This is often the case when indexing data in an array or matrix, however, spatial locality applied to data elements (as opposed to instructions) is much more difficult to implement.

Temporal locality is also a statistical-based theory which says: if a word is read from memory, the probability of it being used again increases. Cache memory is the hardware that tries to capitalize on temporal locality. The effectiveness of a cache memory is known as the so called "hit ratio." Given a certain number of instructions (or data) that must be fetched, the hit ratio is the number that can be accessed from the cache verses how many must be accessed from main memory.

Caches seem to work fairly well with single processor computers, but because of cache coherence problems, they are difficult to incorporate into multiprocessor systems. Cache coherence relates to the uniformity of data between the various caches within a system. For example, suppose a two processor system is tightly-coupled through a main memory but each processor has a data cache. A different routine is running on each processor and the two tasks communicate through the shared main memory. If, however, a shared address is present in both caches and the individual processors read and write that address, then each processor would not have the same piece of data in its respective cache. Thus, neither processor would see the changes caused by the other.

Of course there are schemes to remove this problem. Invalidating all cached copies of a location when a processor writes a new piece of data to that address,

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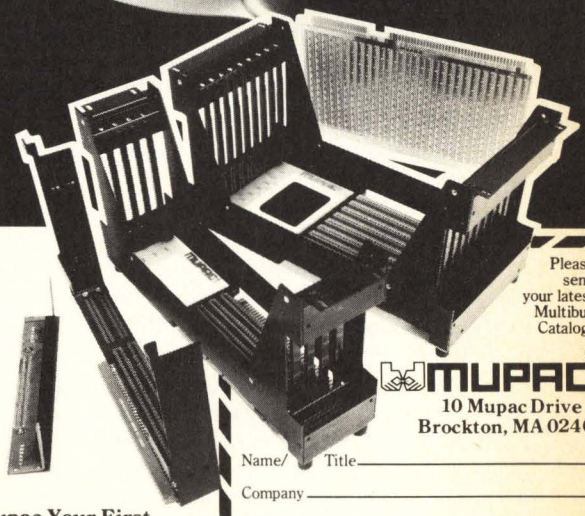

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and then loading each cache with the most recent value is one possibility. Designs that explicitly interlock writing or bypass the cache on a write have been studied, but as the system size grows, the performance declines and the complexity becomes unmanageable. There are other solutions aimed at maintaining cache coherence, but all incur overhead and/or reduce parallelism.

Pipelining

In addition to prefetch buffers and cache memories, pipelines usually increase the speed and efficiency of a von Neumann computer. Basically, pipelines provide some measure of parallelism to reduce latency (**Figure 5**). Keeping the pipeline full is the key to maintaining efficiency. For example, if a pipeline has 10 functional blocks, keeping it full requires that the results contained in stages one through nine be independent of the pipeline's new incoming data. If this new data does depend on the results of an intermediate stage, it cannot proceed until the intermediate data is finished. This may cause the pipeline to partially, or completely empty. In short, executing a particular pipeline operation before the previous data is processed demands total independence between the two data elements.

Most high speed machines are pipelined, but even these systems contain great inefficiencies. For instance, if a branch statement is encountered in an instruction pipeline, the program must wait for the pipeline to empty. In many cases, it is simply impossible to guarantee data independence. This is one of the primary reasons that a supercomputer (such as a Cray) runs at 10 to 12 MFLOPS rather than 240.

By implementing hardware to detect interlock conditions, data dependencies can be partially circumvented. In a pipelined system, interlocking occurs when a particular instruction depends on a previous instruction. By detecting that one instruction depends on another (which has entered the pipeline but is not yet finished), the incoming instruction can be prohibited from entering until the first instruction finishes. If these detection mechanisms are implemented correctly, the program will execute properly and in the worst case the pipeline will not offer an advantage. In summary, interlocking insures that the program is not adversely affected by the pipeline.

Some operations such as vector instructions work extremely well in a pipelined architecture because all of the operations are independent. If 100 numbers are to be added to 100 other numbers, all of the addition operations are independent. On the other hand, if 100 numbers are to be summed, two numbers must first be added, then the sum must be added to the third, etc. In this circumstance, the calculation is full of dependencies.

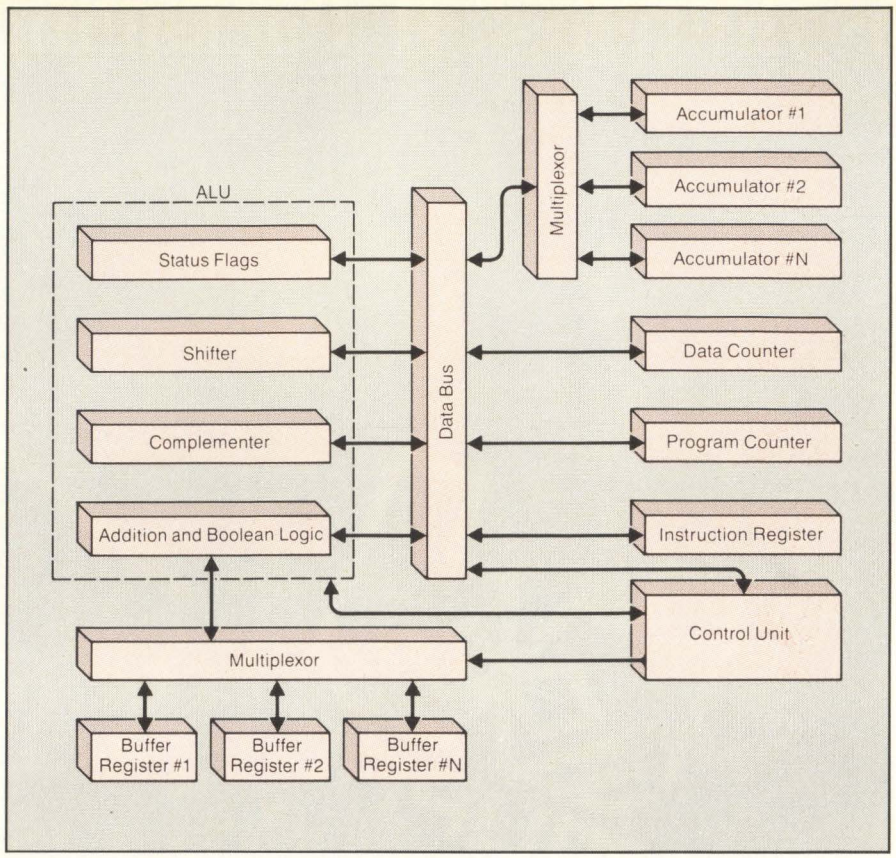

Figure 4: Multiple buffer registers and accumulators enable the processor to concurrently perform several tasks.

Conclusion

When John von Neumann conceived the basic architecture found in all of today's computers, undoubtedly he could not

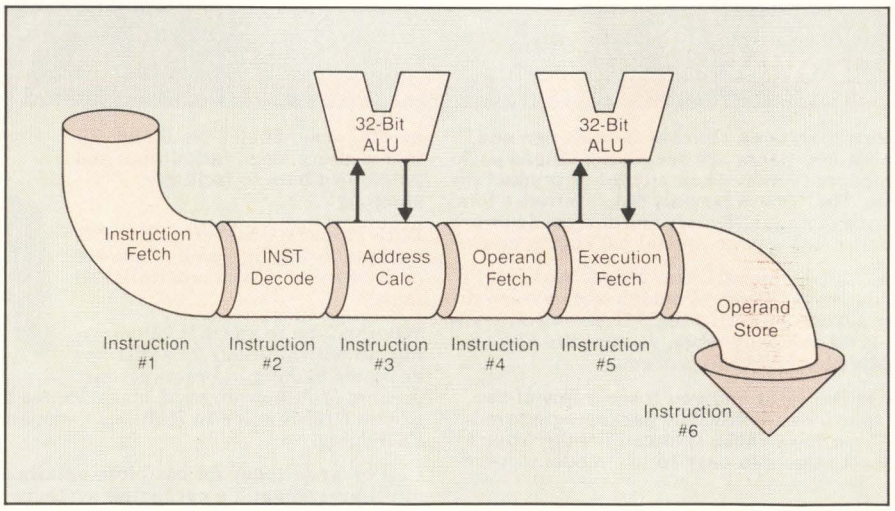

Figure 5: This instruction pipeline will be used in Zilog's new Z80,000 32-bit microprocessor (to be introduced in February 1985). Keeping a pipeline full is critical to exploiting its usefulness.

have foreseen its omnipresent future. If he could have looked into the future and seen the growth of the computer, would he have altered the basic architecture to remove the bottleneck? That question will most likely never be answered, but the point is whether the time has come to change the face of computers by adopting some less constraining architectures.

Of course such a transition would not occur overnight, but nonetheless it would be foolish to put on blinders when alternate computer architectures begin to appear. With such a huge amount of software written for von Neumann machines, non-von Neumann systems would need quite a few years to catch up.

Regardless of tricks like cache memory and instruction prefetch buffers, von Neumann machines will continue to be inefficient for parallel processing. According to ongoing research at MIT, most of today's software programs contain much parallelism, although in many cases it is hidden.

The von Neumann machines in use today have served and will continue to serve quite well, but what about future computing needs? Aside from research at MIT, manufacturers such as NEC and Texas Instruments are delving heavily into the exploration of alternate computer architectures. NEC, in fact, has a dataflow IC scheduled for sampling in December. In part 2 of this series (*Digital Design*, December 1984) several alternate architectures will be analyzed including MIT's data flow machine which will use 64 of TI's new AI computers configured as a multiprocessor data-flow testbed. DD

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FutureNet's "DASH" Schematic Designer Widens The Scope Of PC CAD

Amidst a flurry of announcements throughout 1984, FutureNet (Canoga Park, CA) has continued to bring CAD to the personal computer level by making available its DASH-1 and DASH-2 schematic designers to a wide variety of PCs. Companies such as HHB Softron (Mahwah, NJ) have also joined the FutureNet bandwagon by offering their CADAT logic simulator with the DASH-1 Schematic Designer. The recent acquisition of FutureNet by Data I/O (Redmond, WA) has resulted in a promise of combined product lines and an exchange of technical expertise which should push FutureNet into an even broader market segment.

FutureNet has also developed an interface translator to transfer designs created on its DASH-1 Schematic Designer to Racal-Redac's printed circuit development system. The interface eliminates the task of manually entering, and perhaps translating design net lists so designers can now proceed more quickly to board layout. Interface translation systems such as these are aimed at enhancing the overall efficiency and cost-effectiveness of the larger system. Once the schematic is transferred from the front-end IBM PC or XT-based DASH-1, the designer can move on to use the fully integrated CAE/CAD/CAM system to link phases of product development.

The DASH-1 is also available for designers using the TI professional personal computer. The package consists of a graphics editor, an RS-232 mouse and complete set of part symbol libraries, turning the TI computer into a tool for board-level and chip-level system design. The DASH-1 is presently available for the IBM PC, XT and AT; and FutureNet began shipping CAE workstations based on the DEC Rainbow in October. The system turns the DEC Rainbow into a design station which can create IC designs, discrete components, and higher-level VLSI chip designs. Because of the Rainbow's heritage, the DASH-1 Rainbow is an effective front-end to larger, more powerful DEC computers, such as a VAX.

An interface created to transfer the schematics generated by DASH-1 to the IBM Circuit Board Design System (CBDS) facilitates integration of functions, automatic component placement and trace routing, and on-line digital logic simulation for early design modeling. The IBM CBDS has a centralized component database and supports digital, analog or a mixture of layouts.

The DASH-2 Schematic Designer, which began deliveries this September, offers a higher level of design capabilities than the DASH-1. DASH-2 adds a coordinated set of enhanced mouse-driven editing features, a proprietary graphics controller and mouse interface. New capabilities include: "Tag and Drag," enabling a user to pick a symbol, a drawing area or alphnumeric field and drag the targeted selection across the screen while maintaining connections; and "Snap," in which a user, when drawing a wire, can position the cursor in the vicinity of a pin, snapping the connection in place.

The DASH-2 Add-On package for the IBM PC is priced at $5,980, with the complete DASH-2 system, including the IBM PC and printer, selling for $9,980. DASH-2 for the IBM XT is priced at $6,280, and $12,980 for the complete system. FutureNet provides upgrade packages at $250 each or a $400 Software Maintenance Plan which entitles the user to automatic upgrades for one year.

FutureNet's development of new interfaces linking large CAD systems and personal computers is calculated to save money already invested in equipment and dramatically speed up the design process. Larger popular systems like General Electric's TEGAS for test generation/simulation, and Scientific Calculation's Scicards for printed circuit board layout provide capabilities that low-end workstations are not necessarily going to provide. By making the PC-based workstation a front-end to the system, many shortcomings of the expensive equipment, such as being difficult to access and learn, are overcome.

—Hanrahan
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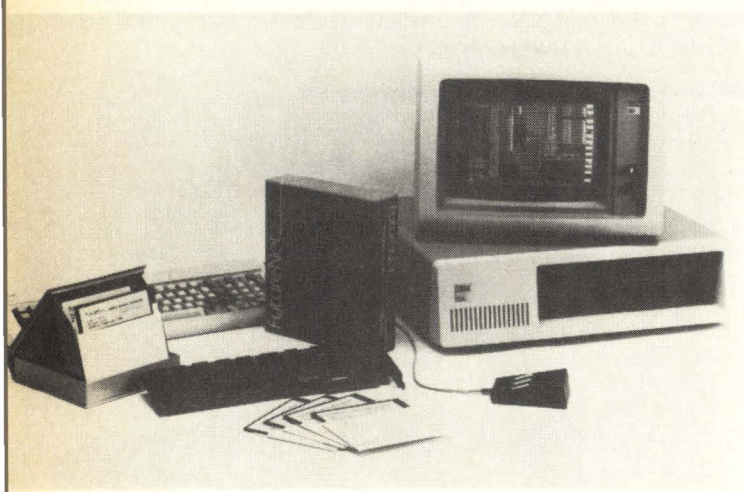

Figure 1: FutureNet's DASH-1.

Figure 2: The DASH-2 Schematic Designer.

Texas Instruments And Signetics Combine Standard Cell Expertise

Since September of 1983 Texas Instruments has been planning standard cell products for external customers based on prior development of standard cell ICs for internal use. The new SN54/74SC standard cell family is based on 3 micron, twin-well CMOS technology. Through an alternate sourcing agreement with Signetics, both companies will market and manufacture TI's standard cell family as well as Philips/Signetics library of complex MSI cells. In addition to its standard cell family, TI will offer a broad line of CMOS and bipolar gate arrays. These arrays are a result of an alternate sourcing agreement announced earlier this year with Fujitsu Ltd.

The family of CMOS arrays will address complexities to 8000 gates at 2.5 nsec speeds and the bipolar arrays will service complexities to 1100 gates at 1.9 nsec speeds.

Both TI and Signetics' libraries are 3 micron CMOS with compatible processes and can be used together to implement IC designs. In addition to providing an alternate source for each company's standard cell products, the agreement provides for each party to design and develop new standard cells to extend the common library. Initial plans to co-develop future standard cell libraries also include reduction of the geometries of the existing 3 micron CMOS library to 2.3 microns for performance improvement and to extend the library to include more complex functions.

According to Dataquest, Inc., the worldwide market for standard cell products will more than triple in size by 1989 to approximately $1.2 billion (**Figure 1**). CMOS is predicted to be the technology of choice for standard cells.

For the short term, the contract amalgamates nearly 200 cell designs in the present libraries into a new common standard cell library. It also commits resources to new cell designs with advanced process technology for future generations of products. TI will immediately transfer approximately 150 SSI, MSI and I/O cells; Philips/Signetics, will contribute 40 complex MSI cells. For the 2.3 micron library, Philips/Signetics will prepare and transfer an additional 80 MSI cells. Work will begin immediately by both parties to implement the existing library in 2.3 micron technology.

The establishment of a common design interface may allow users with minimum training to engage in semicustom IC creation. The TI/Signetics standard cell library will be supported on third-party systems, such as Daisy, Mentor, FutureNet, P-CAD and Valid Logic. As EDIF (Electronic Design Interchange Format) standards evolve, users will be able to employ EDIF as the standard interface format between third-party design systems and the cell libraries.

—Hanrahan

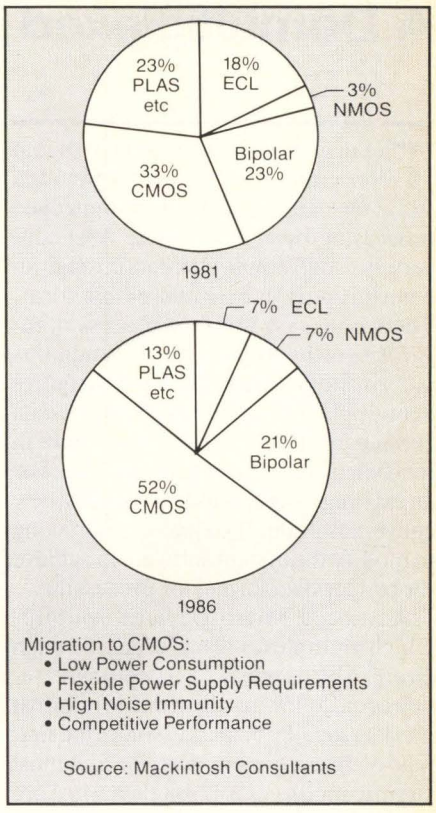

Figure 1: Worldwide merchant semicustom market by technology.

A Demultiplexed Analog Subsystem

The new monolithic analog to digital converters generally do not provide a 16-bit formatted data word for immediate processing by a CPU. These A/D converters usually multiplex data through an eight-bit port in byte and nibble form. There is no easy way for a processor, regardless of the ALU bit size, to handle this unformatted data directly since it requires demultiplexing and reformatting the data coming from the converter. This results in inefficient and slow data processing. For an existing system to use one of these new converters it could be a major undertaking to modify the system software to achieve the proper data format for processing.

Advanced Micro Devices' Am6112, which multiplexes 12 bits of data through an eight-bit port in two's compliment, requires the following algorithm to reformat the data for a 16-bit processor. In the first read of the converter's port, the four most significant bits of a 12-bit data word are read into one of the processor's registers (bit locations B0 through B3). In the second read, the eight least significant bits are read into a different register (bit locations B0 through B7). To merge the two registers, the processor must do a logical shift of the four most significant bits to locations B8 through B11 in the first register. B11 is tested for sign, and, if negative, bits B12 through B15 are set. The shifted and corrected register must then be merged with the second register to get a formatted data word of any value for processing. An analogous operation must be done if the conversion code is one's offset. The added processing time required is now equivalent to five or six instructions per data fetch.

The following design, using a PAL device, is a hardware/software solution for the interface of the Am6112 to a 16-bit processor – shown in **Figure 1**. This hardware design doesn't require the five or six instructions for formatting to be used each time there is a data fetch, thus avoiding an untenable software modification or an increase in processing time.

The first step in the design is to construct a timing chart (**Figure 2**). The chart shows the timing interactions between the PAL device and the Am6112. After working out the timing, schematics are drawn and the allocation of inputs and outputs can be assigned to the PAL device (**Figure**

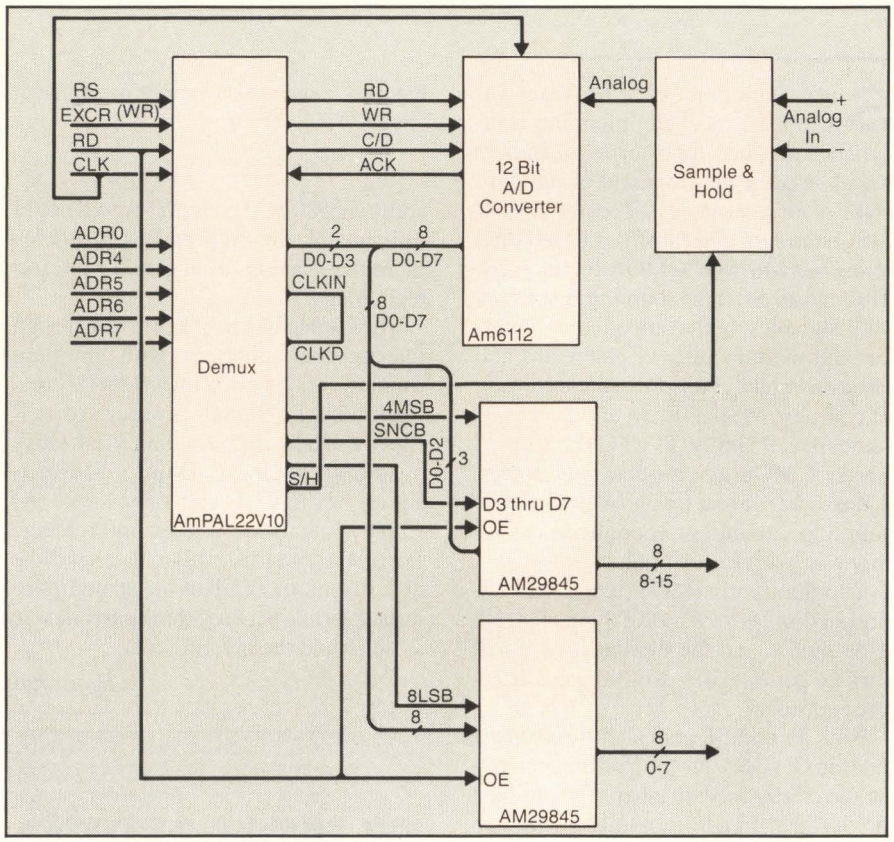

Figure 1: Circuit diagram showing AMD's Am6112, ADC, controlled by AMD's new AmPAL22V10 PAL with a parallel 16-bit bus interface. The AmPAL22V10 functions as a state machine to initialize and control the sample and hold device, the Am6112, and provide the logic necessary to demultiplex 12 bits of data from the Am6112 and place it into a 16 bit data format with corrected sign bit.

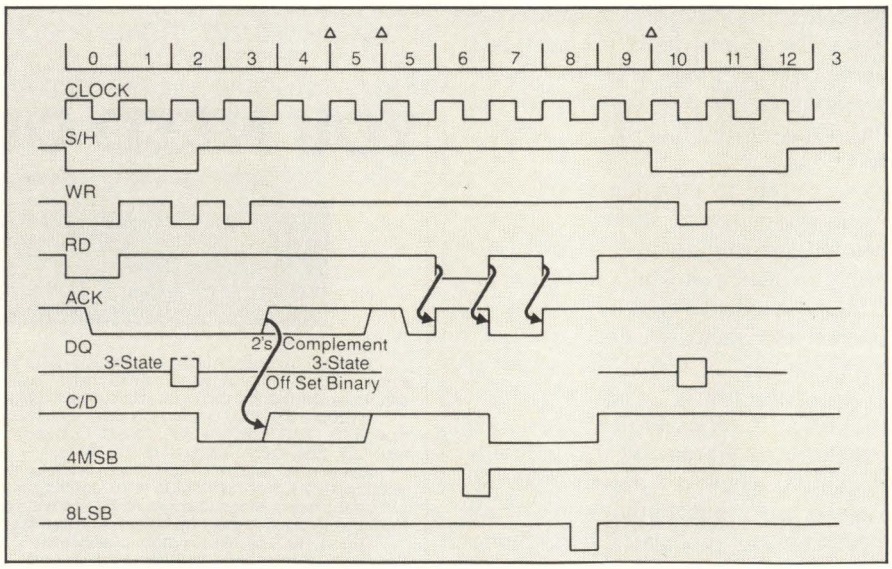

Figure 2: Analog to digital conversion cycle showing power up initialization – states 0 to 2, start of conversion – state 3, conversion cycle – states 5 and 6, and latching of data from conversion – states 6 and 8. The first entry point is the power up sequence in state 0 and the second is in state 9. In states 5 and 9 the clock does not run until conversion is complete or an external conversion is requested, respectively.

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1). Finally, the sequential states and the Boolean equations are defined and assembled. In this instance the sequential states are the successive binary states of the timing.

The parts used in the interface design are Advanced Micro Devices' AmPAL22V10, the Am6112 12-bit analog to digital converter, and two Am29845 bus registers. The AmPAL22V10 is mnemonically called "DEMUX," meaning de-multiplexer.

The design requires minimal clocking during the actual conversion of the analog signal in the Am6112. This is done by gating the acknowledge signal from the Am6112 and one of the binary states from the state counter with the clock signal through the PAL device. There is also minimal clocking when the Am6112 is idle. Again, by gating the clock with a binary state from the state counter and the signal that requests a conversion, clocking in the circuit is minimized. In the PALASM source listing, the clock control equation has ADR4 through ADR7 factors. These factors are the I/O address lines from the CPU. The I/O address decoding for chip select is done in the AmPAL22V10 for the conversion circuitry.

After an external conversion request, the clock is gated on to start the Am6112's conversion. The external conversion request signal is the control bus' write signal. Thus the first equation for the PAL device is state 5 and acknowledge low, or state 9 and external conversion request low which allows the clock to run the state counter.

Not clocking during conversion or while idle prevents unwanted noise, especially in the analog signal, and minimizes the overall system noise generation due to output switching. Using these design rules does not alter the actual conversion time in the Am6112. The Am6112 requires approximately 14½ clock periods for a conversion. The state machine requires 13 clocks but three overlap with the clocking of the Am6112. Thus, the total number of clocks in a conversion is 24½ from the leading edge of the control bus' write signal.

Creating the Boolean equations for the interface design is a heuristic process using the timing chart. For example, in defining the read equation from the timing figure, read must be low during state zero, state six and state eight. The actual logic for the read signal is implemented as shown in **Figure 3**, and its Boolean expression is in the accompanying PALASM listing (**Figure 4**). In states two and three, the write signal will go active low during only the first half of each state's clock cycle rather than for the whole period as in the read signal. For the command/data signal the timing figure shows it going low in the

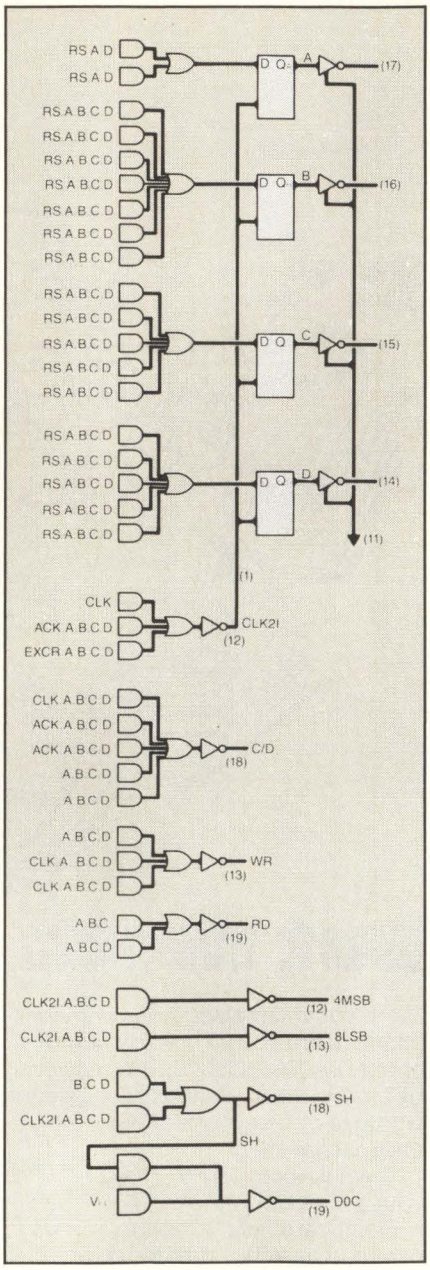

Figure 3: Graphic representation of the functions expressed in the PALASM source listing DEMUX for the AmPAL22V10 PAL.

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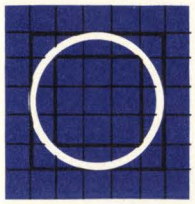

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Bearing noise can have a substantial effect on performance. Hoover-NSK employs an anechoic chamber to establish noise levels for its prototypes and to test production samples. The result is a disk drive bearing capable of performing to levels as low as 30 db.

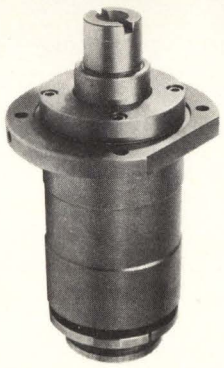
5. Minimum Torque

Starting torque generated by most bearings can eventually ruin a DC brushless motor. Hoover-NSK has minimized this problem in two ways: first, through manufacturing techniques that produce a virtually frictionless bearing; and, second, through the use of an exclusive patented V Labyrinth Seal. This seal retains the lubricant without actually contacting the bearing inner ring.

6. High Lubricant Integrity

In some cases ordinary bearing-seal designs can permit the volatile compounds of a lubricant to evaporate. Hoover-NSK has developed a special contact seal for these applications. When paired with a V Labyrinth Seal, this combination provides excellent lubricant integrity and maintains low torque characteristics.

Send for your copy of the Hoover-NSK Design Reference Guide for Disk Drive Bearings. It contains all the information you'll need for proper design and specification, including data not normally easy to find.



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Disk Drive Bearings

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Write 36 on Reader Inquiry Card

```
CLKIN RS EXCR SYSRD ACK CLK D3 ADR0 ADR4 ADR5 ADR6 GND
ADR7 A B C D D0 CLKO /SH /CD /WR /RD VCC

; CONTROL SIGNALS
RD = /A*/B*/C* + /A*B*C*/D

WR = /A*/B*/C*/D + /A*B*/C*/D*CLKO +
     A*B*/C*/D*CLKO + /A*B*/C*D*/CLKO

CD = /A*B*/C*/D*/CLK + A*B*/C*/D*/ACK +
     /A*/B*C*/D*/ACK + /A*/B*/C*D + A*B*C*/D

SH = /A*/B*/C*/D + A*/B*/C*/D*CLKO +
     /A*B*/C*D +A*B*/C*D +/A*/B*C*D*CLKO

; CLOCK OUTPUT FOR STATE COUNTER
CLKO = CLK + A*/B*ACK*C*/D +                    ; EXCR & 10 @ I/O ADDR CX
       A*/B*/C*D*EXCR*ADR4*ADR5*/ADR6*ADR7

; CONVERSION MODE CONTROL
IF (/A*B*/C*/D*CLKO*/ADR0 +          ; I/O ADDR C0H AND C1H
   /A*B*/C*D*/CLKO*/ADR0) D0 = SH    ; ADR0 = LOW IS 1's & IF HIGH is 2's.

; STATE COUNTER AND ADDITIONAL CONTROL SIGNALS
A: = /A*/D*RS + /A*D*RS

IF (/A*B*C*/D*/D3)      B: = A*/B*/C*/D*RS + /A*B*/C*/D*RS + ; [SNCB]
                             A*/B*C*/D*RS + /A*B*C*/D*RS + ; SIGN CONTROL
                             A*/B*/C*D*RS + /A*B*/C*D*RS + ; BIT
                             /A*/B*C*D*RS

IF (/A*/B*/C*D*/CLKO)   C: = A*B*/C*/D*RS + /A*/B*C*/D*RS + ; [8LSB]
                             A*/B*C*/D*RS + /A*B*C*/D*RS + ; STROBE
                             A*B*/C*D*RS

IF (/A*B*C*/D*/CLKO)    D: = A*B*C*/D*RS + /A*/B*/C*D*RS + ; [4MSB]
                             A*/B*/C*D*RS + /A*B*/C*D*RS + ; STROBE
                             A*B*/C*D*RS
```

FUNCTION TABLE

CLK	CLKO	CLKIN	EXCR	ACK	RD	WR	CD	SH	D0	D3	D	C	B	A	RS	
H	H	C	X	X	X	X	X	X	Z	X	X	X	X	X	L	;0
H	H	H	H	X	L	L	H	L	Z	X	Z	Z	Z	L	H	;0
L	L	L	X	L	L	L	H	L	Z	X	Z	Z	Z	L	H	;0
H	H	C	X	L	H	H	H	L	Z	X	Z	Z	Z	H	H	;1
H	H	H	X	L	H	H	H	L	Z	X	Z	Z	Z	H	H	;

Figure 4: PALASM listing and example of function table for application.

latter half of state two, remaining low through states three and four and rising to the high state, inactive, in state five. It also has a synchronous relationship to the acknowledge signal from the Am6112: command/data is "anded" such that it will not go inactive until the acknowledge signal becomes inactive.

The other control signals are similar to the read, write, and command/data signals. The data signal, D0 of the PAL, going to D0 of the Am6112, serves as an output during initialization in the first half of state two.

To generate all of the control signals, a four-bit counter was created in the PAL device to count from zero to 12. At reset, or power-up, the counter starts at zero and goes through one cycle, or counts to nine, then stops until the CPU exerts an active low on the write control line. States 10, 11 and 12 occur after the active leading edge of the write signal, and provide a sampling window for the sample and hold circuit. In state 12, the state counter is loaded with a four-bit binary value of three. On the next clock edge, that which would sequence a counter to state 13, the counter is synchronously loaded with the value three and sequencing of the converter occurs for a conversion.

The B, C And D outputs of the counter are normally tri-stated. B, C and D out-

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puts are pulled to ground via resistors. When a strobe for data enable is needed for one of the bus latches, either C or D's output is taken out of tri-state and driven active high. B's output state is determined by the sign bit from the Am6112 converter. It drives input bits B12 through B15 of the high half of the data bus latch in order to move the sign bit to the most significant bit position; this eliminates the need for software modifications. If the sign bit is positive, or active low, the output is not taken out of tri-state. If the sign is negative, or active high, the output is taken out of tri-state and driven active high. **Write 237**

– Garret Spears, Field Applications Engineer, Advanced Micro Devices, Sunnyvale, CA

Transmitter/Receiver Chip Set Allows 802.4 Networking Or Point-To-Point Modem Communications

A new bipolar chip set that makes frequency-shift-keyed (FSK) asynchronous modems, allows OEMs to design-in rather than buy a board-level solution for local networks in point-to-point or token-passing bus service. The NE5080 High-Speed FSK Modem Transmitter and NE5081 Receiver chips from Signetics (Sunnyvale, CA) could reduce manufacturing costs for integral communications.

The 5080/5081 set provides phase-continuous FSK modulation and demodulation at high carrier frequencies and filtering to reject EMI and RFI noise frequently encountered in computer and industrial environments. Though the set is designed to meet IEEE 802.4 specifications for token-passing bus local area networks, they can be tuned for various frequencies, data rates and modes of operation, for use with twisted pair, coaxial or fiber optic cable. Transmission distances depend on the center frequency and cable type used (**Table 1**). The carrier frequency is externally adjustable from 50 KHz to over 20 MHz. As specified by the 802.4 standard, the 5080 transmitter is designed to operate with 5 MHz center frequency, or 6.25 MHz high and 3.75 MHz low. External trimming components allow the center to be changed, but the 25% ratio is always maintained. The transmit gate pin (**Table 2**) allows the FSK output to be disabled. Though both the internal oscillator and the output buffer are disabled, the 5080 can return to full transmission within one μsec.

For networking, the 5080 has circuitry to avoid "jabber" created when a code fault causes a transmitter to remain active. The jabber control circuit on pin 3 sources a current during transmission. This current can be used to set the maximum transmit time; when a signal is received indicating a fault, the transmitter is disabled. Three options for the jabber control pin are: to use the current to charge a capacitor, so a logic low resets the jabber function via open collector output and a logic high disables the transmitter; to use it to sense the current and have external circuitry control, however long the transmitter is on; or the pin can be made inactive by tying it to ground. The jabber flag pin goes high when the control pin shuts off the transmitter. A logic low to the jabber control pin makes this latch for resetting.

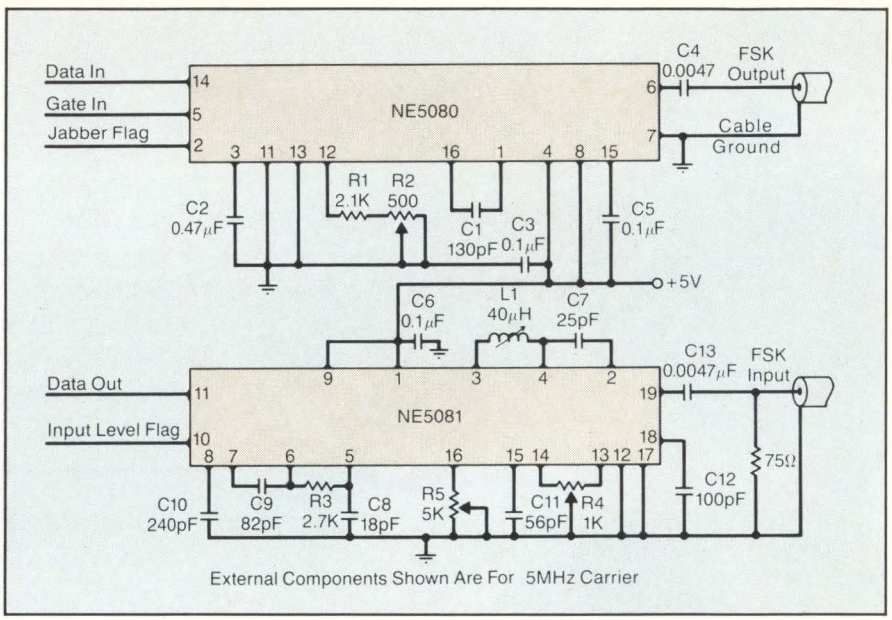

Figure 1: Connection of the NE 5080 and 5081 as a DC to 2 Mbaud full-duplex modem.

At the receiving end of the link, the 5081 demodulates the FSK and outputs digital data. Like the transmitter, it is tuned to discriminate signals that are 25% above and below the carrier at various frequencies set by external components. Normal acceptable input levels range from 16 mV RMS to 1 V RMS, and the levels are adjustable to minimize the effect of noise. The BER is reported as 10^{-12} for the device; 802.4 specifies only 10^{-9}.

Carrier Frequency	Maximum Data Rate	Cable			
		RG-59	RG-11 (Foam)	JT34125	JT3750J
1MHz	0.5 Megabaud	6000 Ft	21000 Ft	33000 Ft	50000 Ft
3MHz	1.0 Megabaud	5000 Ft	12000 Ft	20000 Ft	32000 Ft
5MHz	2.0 Megabaud	4200 Ft	9500 Ft	15000 Ft	25000 Ft

Table 1: Transmission distance for a single 5080 receiver as a function of center frequency and cable type.

Table 2: Pin functions of the NE 5080 transmitter chip.

PIN	FUNCTION
1	**OSC 1**—one end of an external capacitor used to set the carrier frequency
2	**JABBER FLAG**—this pin goes to a logic high if the transmitter attempts to transmit for a longer time than allowed by the Jabber control function
3	**JABBER CONTROL**—used to control transmit time. See note on Jabber function
4	V_{CC_1}—voltage supply
5	**TRANSMIT GATE**—a logic low on this pin will enable the transmitter; a logic high will disable it
6	**TRANSMITTER FSK OUTPUT**
7	**CABLE GROUND**—the shield of the coax cable should be connected to this pin and to Pin 11
8	V_{CC_2}—Connect to pin 4 close to device
9	**No Connection**
10	**No Connection**
11	**GROUND 2**—connect to Analog ground close to device
12	**OSC 3**—a variable resistor between this point and ground is used to set the carrier frequencies.
13	**GROUND 1**—connect to Analog ground close to device
14	**DATA INPUT**
15	**REGULATOR BYPASS**—a bypass capacitor between this pin and V_{CC_1} is required for the internal voltage regulator function
16	**OSC 2**—one end of a capacitor that is between pin 1 and pin 16 and is used to set the carrier frequency

Jitter output is a maximum of +/− 40 nsec.

Modems using the 5080/5081 can be used for multidrop party lines such as local area networks, point-to-point full- or half-duplex links over one or two cables. The modem has a 30 dB dynamic range, so it can be attached to the cable at any point without gain adjustment. Signals can be driven further on point-to-point line than over a network.

The design of a full-duplex modem using the 5080 transmitter and 5081 receiver is shown in **Figure 1**. At DC to 2 Mbaud, the modem will perform under many communications conditions. Other designs allow use over fiber optic lines as well as coaxial cable. Such high-frequency use requires short lead lengths for lines carrying RF, and a good ground plane on the board.

Write 230

— Signetics, Sunnyvale, CA

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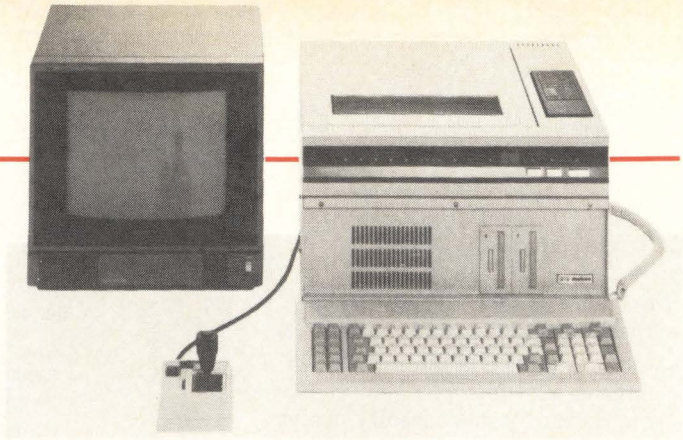
NEW PRODUCTS

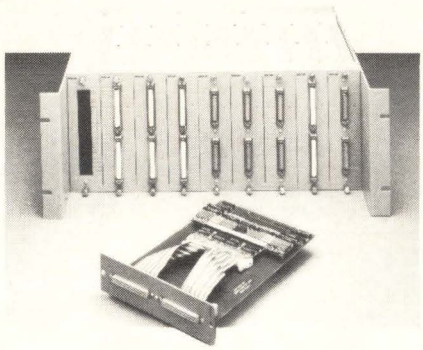


Laser Microcomputer

The LPC-1000 Laser Microcomputer from Matrox Inc., integrates laser video disks and microcomputers into a single system. Its digital data encoding scheme allows compression of text, program and audio data stored on a 12″ laser video disk. In general, information that can be put on a video disk can be motion sequences lasting from less than one second to one hour, 100,000 slides, 100 hours of audio information including speech, one million pages of alphanumeric text and one Gbyte of digital data. All these information forms can be combined on the same disk in any ratio from 0 to 100%. The LPC-1000 includes a high resolution color graphics generator (640 × 400 or 320 × 400) which can be overlaid onto the video disk picture. In its microcomputer mode the LPC-1000 is used as a general purpose 8086-based microcomputer with CP/M-86 operating system and Pascal, Fortran and C high level languages. The laser optical disk is used as archival 2 Gbyte ROM. The digital data files on the optical disk are accessed in the same way as files on floppy or Winchester disks. All application programs which run under the CP/M-86 operating system will run on the LPC-1000. An authoring language, PILOT PLUS can be used in this mode to develop optical disk software for premastering tape. Price is $9750. **Matrox**, Quebec, Canada **Write 141**

Modular I/O Subsystem

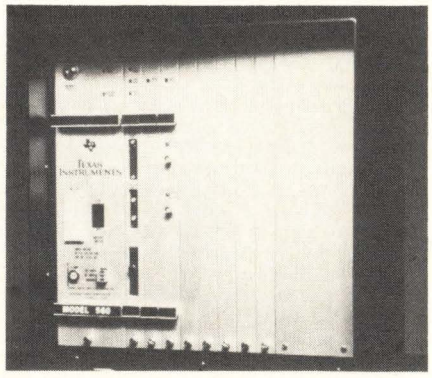
The MSX-2000 Modular I/O Expansion Subsystem from Metacomp adds more I/O capacity to the MPA-2000, an iAPX-186-based CPU and intelligent I/O controller for the Multibus. The MPA-2000 is suited for controlling I/O applications such as data communications, data acquisition, and process control. The number of I/O channels which it can service is determined by the resources provided by two plug-in I/O adapter module sites. The MSX-2000 utilizes a separate 19″ rack



mount chassis which supports eight plug-in I/O modules. Up to eight chassis may be daisy chained. Custom I/O system applications can be developed and packaged onto MSX I/O adapter modules. A typical data communications application for the MSX-2000 Modular I/O Expansion Subsystem would be one MPX-2000-140 and seven MPX-200-170 I/O adapters installed in an MSX-2000 chassis, which in turn is connected to an MPA-2000. This configuration would support 14 ASYNC terminals and two HDLC data links. Price is $1,375. **Metacomp**, San Diego, CA **Write 180**

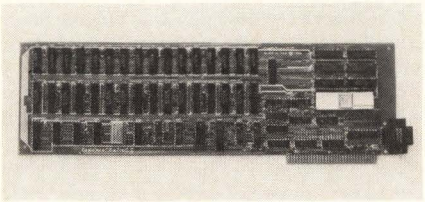
Programmable Controllers

Models 560 and 565 are two programmable controllers recently introduced by Texas Instruments. The Model 560, now TI's largest P/C, is designed to handle the discrete operations in applications such as machine control, material handling and conveyors. Model 565 is designed for discrete, batch, continuous, and data manipulation applications by adding a parallel special function CPU card to the Model 560 chassis. Based on multiple 68000 microprocessors, the Models 560 and 565 are contained in a 19″ card rack. The unit's core is its discrete CPU card, with 48 Kbytes memory, day clock and two peripheral ports. The CPU card uses the Series 500 discrete instruction set that includes 32 pre-defined function blocks with scan matrix compare. The parallel special function CPU card for the Model 565 has dedicated process control functions that add 32 menu-driven PID loops, user-configurable analog alarms and 24 pre-defined special functions. The I/O system can be increased to 8192 I/O points of Series 500 I/O and can be located up to 15,000 feet from the controller. All Series 500 I/O modules are compatible with the remote I/O system



including digital, analog, intelligent, and TIWAY I/O modules. The Models 560 and 565 CPU card(s) can also be programmed via the VPU200 video programming unit. **Texas Instruments**, Dallas, TX **Write 181**

COLOR GRAPHIC DISPLAY ADAPTER

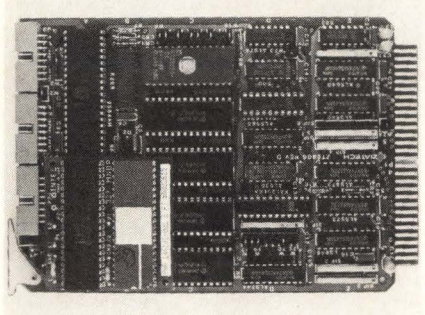


The Chromagraphic I is a color graphic display adapter for IBM compatible personal computers. It provides a 16 color 640 × 408 pixel display at a 60 Hz, flicker free refresh rate. The Chromagraphic I contains an on-board GDC which has been enhanced to draw all color planes simultaneously and to provide replacement and rubberband modes of operation as well as a simplified software interface. A direct drive video port is provided. Price is $800. **Chromagic,** Milpitas, CA **Write 198**

C4 BASIC LANGUAGE

The C4 Basic language from VersaLogic is designed specifically for use in ROM based control systems. The C4 basic language features program execution directly in PROM and automatic program execution at power-up. The companion Non-volatile Operating System software allows C4 Basic programs to be created and tested directly on the target hardware. The C4 Basic and Novos software are supplied on a 4K ROM for use with VersaLogic's "Z80 Smart Card" STD Bus processor board. Price is $150. **VersaLogic,** Eugene, OR **Write 190**

8088-BASED PROCESSOR BOARD



The ZT8806 is an 8088-based processor board for automation applications. MAX mode operation allows the addition of the 8087 Numeric Data Processor using Intel's iSBC 337 piggyback processor option. Five 28-pin byte-wide JEDEC memory sockets provide space for up to 64 Kbytes of PROM and 32 Kbytes of static RAM. The I/O capabilities include one serial port, 5 counter/timers, two 8-bit parallel I/O ports, and an interrupt controller. Price is $465. **Ziatech,** San Luis Obispo, CA **Write 210**

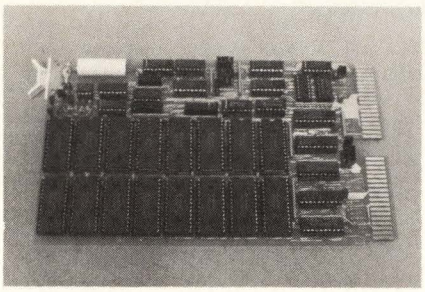
I/O CONTROLLER BOARD

The SAM ISCC/8 is an intelligent serial I/O communications controller board that is Multibus compatible. The board has eight RS-232C serial channels controlled by a 16-bit microprocessor, with both RAM and ROM on-board memory which allow software drivers to be executed remotely. One speed, operating system resides on the SAM-ISCC, coordinates I/O processing and interfacing between the SAM-ISCC and the host processor. Another is available which provides a set of communication protocols. Price is $1,490. **SBS Semiconductor,** Phoenix, AZ **Write 205**

4 MBYTE MEMORY BOARD

The 4 Mbyte memory board from Pyramid Technology doubles the memory capacity of its 90x supermini computer, a 32-bit, UNIX-based machine. The board uses 256K DRAM chips. In addition to the 4 Mbyte board, another introduction, a 2 Mbyte board uses 256K DRAM chips. Both of the boards can be installed in new or existing 90x systems and use the present memory control unit without modification. Price is $22,000 (4 Mbyte) and $11,500 (2 Mbyte). **Pyramid Technology,** Mountain View, CA **Write 189**

STATIC RAM BOARDS



THE LM1164 is a 128 Kbyte static CMOS RAM board which has a two month minimum data retention time, 22 address lines, LSI-11 bus interface, user selectable starting address and a maximum operating current of 400 mA at 5V. Automatic memory protect logic is provided on-board resulting in a self-contained nonvolatile memory system. The board has jumper selectable starting address on 4K word boundaries and a memory write protect on 8K word boundaries. The LM1164 is fully compatible with DSC LSI-11 and Micro VAX microcomputers. Price is $1,494. **Diversified Technology,** Ridgeland, MS **Write 197**

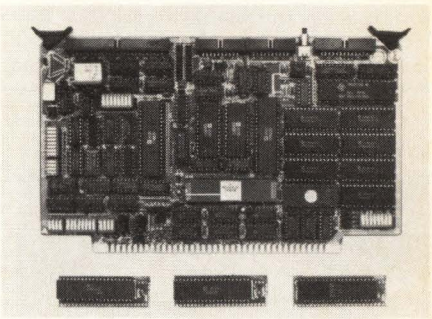
DATA BUS TRANSCEIVER

The Bus-63104 Data Bus Transceiver is form-fit-function replacement for the CT3231. The receiver section accepts Manchester phase-modulated bipolar data at the input and produces a biphase TTL signal at the output. The BUS-63104 transmitter section accepts biphase TTL data at the input and produces a 30V nominal p-p differential signal across a 145 ohm load. The transceiver operates over a −55°C to +125°C temperature range and requires a 5V power source. Price is $295. **ILC Data Device,** Bohemia, NY **Write 215**

LOGIC DEVELOPMENT SYSTEM

Data I/O has updated its Programmable Logic Development System to program 41 PAL and IFL devices from four manufacturers. These devices include the AMD22V10, Signetics IFLs, and MMI's P, RS and RP devices. The PLDS uses four plug-in adapters to program and test the new parts. Each adapter handles one manufacturer's parts. After programming, the PLDS allows users to test devices by entering their choice of structured test vectors. Price is $395. **Data I/O,** Redmond, WA **Write 207**

65K SINGLE BOARD COMPUTER

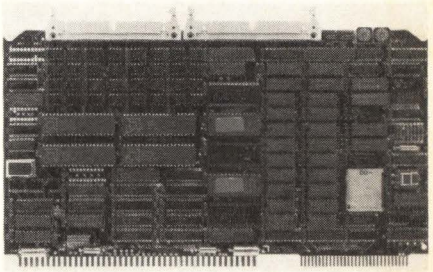


The GMS6507 is a SBC with a choice of 16- or 8-bit CPUs, 65K of on-board memory, two serial and two parallel ports, an IEEE-488 port, and an Opto 22 port that can be used to directly control industrial relay modules. The module can be supplied with 8-bit 6809, Z80, 6502 or 9900 CPUs in 1 or 2 MHz. the GMS6507 includes two RS-232C ports with 15 programmable baud rates. Two parallel printer ports, or one printer and 10 additional user programmable I/O lines, are also offered. Price is $685. **General Micro Systems,** Ontario, CA **Write 195**

4 MBYTE Q-BUS MEMORY

The CI-1173 memory board is designed for Q-BUS compatible systems in configurations ranging from 128 Kbyte to 4 Mbyte. Access and cycle times are 130 nsec and 300 nsec respectively. Memory project logic and battery backup power busing allow the user to operate in a battery backup mode. An on-board control status register, addressable at any of 16 reserved locations in the I/O map, allows instant status of the memory and location of any failing RAM on the board. Price is $1,695 (1 Mbyte) and $7,595 (4 Mbyte). **Chrislin Industries,** Westlake Village, CA **Write 216**

SERIAL INTERFACE BOARD

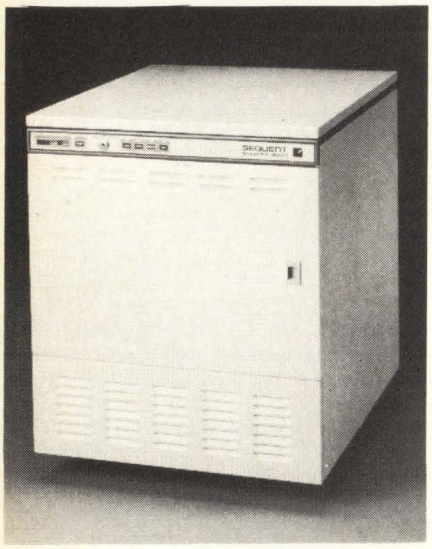


The Am 96/3500 is an eight-channel serial communications controller board, featuring an 80186 CPU. The Am96/3500 can operate as a slave controller or a bus master. The Am96/3500 has eight independently programmable serial channels based on the Z8530 serial communications controllers and is compatible with RS-232C and RS-423 protocols. The SCCs can be programmed to handle all asynchronous and synchronous formats. Price is $2,795. **Advanced Micro Devices,** Sunnyvale, CA **Write 214**

DEC-COMPATIBLE MICROCOMPUTER

The Micro-11 and Super Micro-11 are powered by DEC 11/23 or 11/73 CPUs allowing both systems to run PDP-11 and VAX operating systems. The Micro 11 configuration includes 256 Kbyte memory, 4-line interface, 140 Mbyte 5¼" Winchester, and a 5¼" magtape. The Super Micro-11 has a 140 Mbyte Winchester 5¼" disk with MSCP emulation and 190 Mbyte cartridge tape with 90 IPS and DEC TS11 emulation. Prices start at $14,150 (Micro-11) and $15,150 (Super Micro-11). **California Computer Group,** Costa Mesa, CA **Write 140**

MULTIPROCESSOR SYSTEM



The Balance 8000 is a UNIX-based 32-bit multiprocessor computer system which can include from two to twelve National Semiconductor Series 32000 processors. The Balance 8000 can support a varying number of processors without any software changes, and dynamically and automatically balance the processing load among the available processors. All processors share a single copy of enhanced UNIX, which may be executed by all processors simultaneously. PC Interface allows integration of two operating systems environments. A two-processor Balance 8000 system is priced at $41,500. A 12-processor system, which includes the necessary memory and peripherals to support it at up to 5-7 MIPS performance, is priced at $110,000. **Sequent Computer,** Portland, OR **Write 126**

CAE WORKSTATION

The SystemNode 120H system is designed for hybrid circuit design. Software includes design tools for layout, precision resistors, substrate design rule checking, squares counting and data conversion. The system is controlled by a PDP 11/23 CPU with 256 Kbyte of main memory. It includes a 35 Mbyte Winchester disk drive with controller board, 800/1600 bpi ½" magnetic tape, a color graphics display, an alphanumeric keyboard with user programmable function keys and software. Price is $89,900. **Via Systems**, North Billerica, MA **Write 128**

COLOR WORKSTATIONS

The CDS 3000 systems which are used for CAE and CAD/CAM applications feature 900 × 1152 resolution and support for 16 colors out of a palette of 4096. The CDS 3421 is designed for standalone applications; the CDS 3420, which includes an Ethernet controller, is designed for networked applications. The workstations have a 32-bit, microprocessor-based systems architecture, UNIX operating system, and Fortran 77, Pascal, and C software capability. Prices are $51,600 (CDS 3421) and $42,800 (CDS 3420). **Computervision,** Bedford, MA **Write 135**

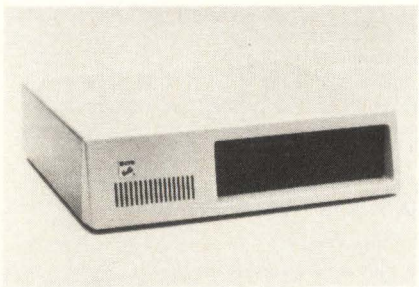
280 MBYTE EXPANSION KIT

The Backup and Restore Utility is a hard disk and ¼" tape drive internal upgrade kit for IBM's PC/AT. As a solution for the transfer of files to a removable medium, one 60 Mbyte tape acts as a librarian for retired files. Users may archive their existing floppies to tape. The expansion systems are available in hard disk capacities of 40, 65, 140 and 280 Mbytes. The kit uses IBM's hard disk controller and the integral ¼" tape unit takes 12 minutes to backup 65 Mbytes. **Emerald Systems,** San Diego, CA **Write 166**

ELECTROSTATIC PLOTTING SOFTWARE

The Versatec software enables plotting on any Versatec plotter from CalComp 921/925 tapes. The utility supports color and monochrome plotting and requires Versaplot Random or Color Random plotting software. Individual submenus have plotter, plot, viewport, color, and CalComp options. User may define line colors, pen width, plotter model, clipping window, plot origin, and transformation viewport for the plotted output. Plots can be generated with different units of measure, scaled within the viewport area, and rotated 90° counterclockwise. The utility supports 6-bit or 8-bit character formats, generation of multiple plots, labeled or non-labeled tapes, and fixed or variable length tape records. Price is $1,000. **Versatec**, Santa Clara, CA **Write 136**

PC NETWORK SERVERS



The Unite Series is a family of UNIX-based network servers for personal computers. The models range from a single-user system to one which will accommodate 32 PCs. The systems are based on Motorola's MC68000 processor, Multibus architecture and AT&T's UNIX System V operating system. Two communication speeds are available: 9600 baud using twisted pair wire, and 10 Mbit/sec using Ethernet. PCs with modems may also have remote dial-up access. The Unite Series consists of five models. Price ranges from $9,000 – $35,000. **CYB Systems,** Austin, TX **Write 164**

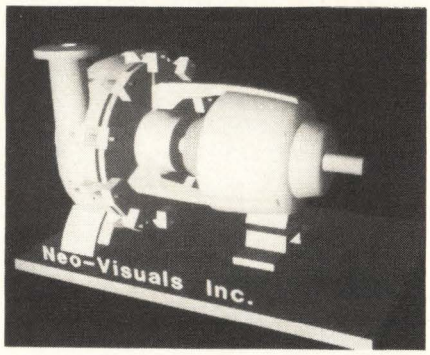
GRAPHICS GENERATOR

The Inovion Personal Graphics System is a graphics generator with a 780K memory and a choice of 2.1 million simultaneously displayable colors. The system provides a 512×480 pixel display with an icon menu overlay plane. Menu software is driven via a mouse or trackball. Features include a frame grabber/digitizer that enables the user to take a signal from a television, VCR, or video camera and digitally freeze the picture for further manipulation, synthetic color routines and menu-driven kernel software. Price is $3,495. **Inovion,** Layton, UT **Write 133**

SCHEMATIC DESIGN SYSTEM

The Dash-1 schematic design system for the TI Professional consists of a graphics editor, a special FutureNet RS-232 mouse and a set of part symbol libraries. Schematic data created on the Dash-1 can be used as input for other local documentation programs, such as net list and list materials. An optional Design Check program is available. The parts library includes templates for almost all standard TTL, CMOS, ECL, Intel and Motorola parts, in addition to popular microprocessors and ROM and RAM chips. Also included are symbols for transistors, diodes, zeners, capacitors, resistors, potentiometers, relays, LEDs, inductors and other discrete devices. Price is $4,980. **FutureNet**, Canoga Park, CA **Write 142**

MODELING PROGRAM

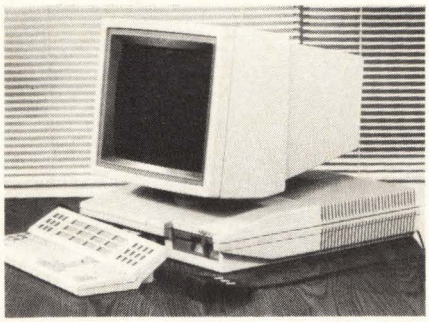


The three-dimensional modeling program defines vectors, arcs, circles and spline curves and includes resident 2D and 3D text fonts. Primitives may be grouped into multiple object definitions and assigned one or more axes-of-rotation. The software includes a set of transformation options to create curved surfaces and volumes. Translations track moving components, trace paths, join irregular surfaces and volumes and perform rotations around moving vectors. Rendering algorithms include smooth shading with specular reflectance, multiple colored light sources and anti-aliasing to remove jagged edges. Real time three dimensional animation and color cycling at up to 60 frames per second is also available. **Neo-Visuals**, Willowdale, Ont. **Write 129**

SOFTWARE FOR PCB DESIGN

The DNA2000 is a task-oriented software system which automates the electronic design process from schematic entry through phototools and manufacturing documentation. The DNA2000 contains multiple autorouter routines, automatic schematic entry, circuit placement and interactive design, checks the PCB for mechanical errors and electrical connection, and contains a selection of post-processing programs. Its distributed process architecture enables the DNA2000 software to be used without downloading the VAX processor. Price is $5,000. **Vectron,** Santa Clara, CA **Write 137**

GRAPHICS WORKSTATION

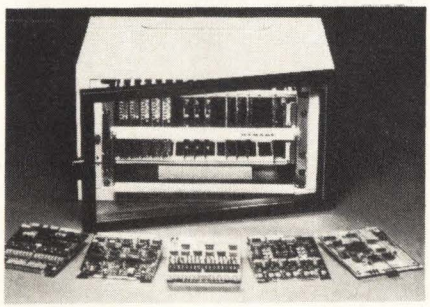


The Interpro 32 is a 32-bit workstation, based on National Semiconductor's 32000 microprocessor. The workstation supports four modes of operation, functioning as: a standard graphics workstation, operating with an Intergraph VAX-based or Micro VAX-based data processing system; a general-purpose workstation using the UNIX operating system and running user-developed or third-party software; a terminal emulator, functioning as a Digital Equipment VT200, a Tektronix 4014, or an IBM 3270 Series terminal; or a standalone personal computer, running user-developed or third-party software under MS/DOS. The unit has system software to support Ethernet networking capabilities. The Interpro 32 has 1¾ Mbytes of parity memory and the main processor runs a virtual memory version of the UNIX operating system. **Integraph,** Huntsville, AL **Write 139**

COLOR GRAPHICS TEST SYSTEM

The Q2/52 Memory Test System is an interactive bit map color graphics station for testing semiconductor memories. It displays 1 Mbit of data simultaneously on the 19″ high-resolution color monitor, and bit manipulation capabilities are accessible through keyboard and joystick controls. The system stores up to eight planes of 1 Mbit each and, when coupled with color, displays single-level or composite bit maps. Price is $60,000. **Megatest**, San Jose, CA **Write 131**

PROGRAMMABLE I/O SYSTEM



The Safe 8000 Basic Programmable Intelligent Front End can be used as a local standalone process computer or as a remote front-end for distributed control and/or data acquisition applications. It communicates to a host computer over two RS-232/RS-422 ports. Programmed in Safe BASIC, the system provides 64 PID controls algorithms, software timers, priority interrupts and multitasking. Applications include setpoint control, data acquisition, batching control and sequential control. The 8000 supports 128 analog channels and 2048 discrete signals. Input/output modules are available. Prices start at $3,767. **Dynage/Controls,** Cromwell, CT **Write 130**

SOFTWARE FOR INTEL 286/310

These hardware and software enhancement packages from Intel are designed for its 80286-based family of 286/310 supermicrocomputers. The enhancement packages include larger mass storage peripherals and main memory, I/O controller options, peripheral expansion capability, a new release of the Xenix operating system application software packages, programming tools, such as Cobol, C, Basic, and system software. The expansion options include 1- and 2-Mbyte error-corrected RAM boards. Other enhancements include a 40-Mbyte Winchester disk drive and the 311 45-Mbyte tape cartridge drive. Price ranges from $14,800-$16,500 for technical and commercial systems. **Intel**, Hillsboro, OR **Write 134**

GEOMETRIC MODELING SOFTWARE

GMOS is an interactive solid geometric modeler which uses a polygonal boundary representation. Primative objects can be combined thru the use of the Boolean command to produce more complex objects. Various viewing manipulations are provided which allow the user to view a given object from any position. Multiple views of an object can be displayed to produce conventional drafting style output. The command interface is threefold; alpha-keyboard entry, screen menus with cursor entry and screen menus with tablet entry. All input is error checked. GMOS provides for the creation of blocks, cylinders, cones, spheres, tubes, objects of extrusion, and objects of revolution (both with arbitrary cross sections). These cross sections may be described by keyboard input or cursor/tablet input. **JML Research,** Madison, WI **Write 132**

DATA ANALYSIS SOFTWARE

Pro 350 is data analysis software for the DEC Professional 350. Included are descriptive statistics, multiway cross tabulations, correlations, simple, multiple and stepwise regression, one- and two-way analysis of variance, one- and two-sided t-tests, nonparametric statistics, time series analysis, exploratory data analysis and matrix operations. Data can be represented graphically by scatterplots, histograms, stem-and-leaf displays and boxplots. Minitab runs on any Professional 350 with 256 Kbytes of memory, a 5 Mbyte hard disk, P/OS and the floating point option. **Minitab**, University Park, PA **Write 127**

ARTIFICIAL INTELLIGENCE SOFTWARE

The KEE system is an artificial intelligence-based software product that enables its users to construct knowledge-based "expert" systems. It is a logic-based language which combines a database query-type language with the deductive power of knowledge-based systems. The software has systems-supported legality checks that insure the integrity of large and complex knowledge bases and provide for the representation of knowledge when the user has only partial or incomplete information. The KEE system includes a rule system which uses the Tell-AndAsk assertion and retrieval facilities. **Intelli-Corp,** Menlo Park, CA **Write 146**

GKS GRAPHICS TOOLS PACKAGE

The GK-2000 is a graphics software subroutine library which is compatible with Precision Visuals device-intelligent drivers. GK-2000 is a tools package consisting of 190 user-callable subroutines which enable programmers to develop 2D applications that are independent of a specific output device. The package's capabilities include interactive 2D image manipulation, support for 11 concurrent device drivers, 24-stroke-precision fonts, 256 line types, and a range of graphics input devices. Prices range from $4,500 to $21,000. **Precision Visuals,** Boulder, CO **Write 145**

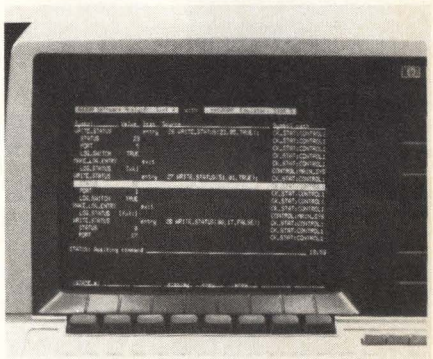
GRAPHICS BUILDER

The Blox Graphics Builder for VAX/VMS and VAX/UNIX systems is used to prototype and develop graphics applications interactively. The screen layouts consist of menus, work areas and message areas, and can contain both text and graphics. The interactive menus and screen layouts can be used immediately, without application code. Blox links the developer's application code to the defined screens, menus and events and generates an application help file with help keywords for each part of the screen. Blox includes a Core grpahics library and a user-interface library. License is $8,000. **Rubel Software**, Cambridge, MA **Write 144**

ELECTRICAL SIMULATION SOFTWARE

The SPICE Electrical Circuit Simulator software program is designed for operation on Cromemco's multi-user microcomputer systems. The SPICE program (standard Berkeley SPICE2, version 2G.6) is a general-purpose circuit simulation program for use by electrical/electronic engineers in circuit design applications. The program can generate tabular and graphic data. The package includes several versions of the program, the implementation of which varies according to the amount of memory available and the presence or absence of support for floating point hardware. The program is configured for 1 Mbyte or 3 Mbytes of RAM. Price is $595. **Cromemco,** Mountain View, CA **Write 143**

SOFTWARE ANALYZERS



The HP 64330 series of software analyzers support debugging and troubleshooting for programs written in high-level programming languages for microprocessor applications. The first two high-level software analyzers support 68000 microprocessors (HP 64331A) and 8086 microprocessors (HP 64332A) for C and Pascal programming languages. Both analyzers are available as subsystem of the HP 64000 logic development system. Each of the H P 64330 series high-level software analyzers operates with the corresponding HP 64000 emulator and HP 64302A emulation-bus analyzer. Price is $3,000. **Hewlett-Packard,** Palo Alto, CA **Write 138**

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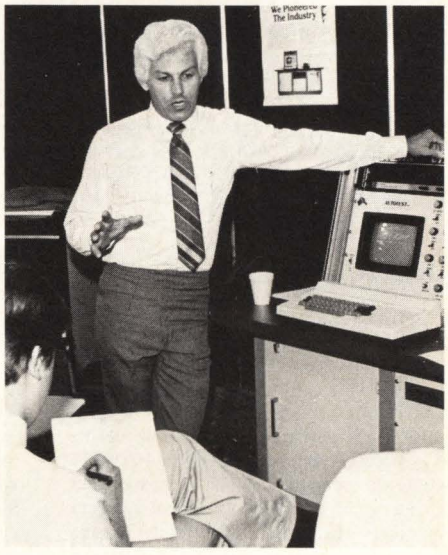

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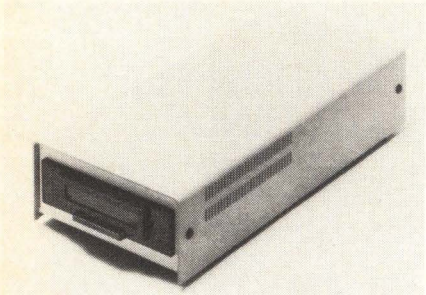
DD

5¼″ HALF-HEIGHT TAPE DRIVE



This series of 5¼″ half-height removable cartridge tape subsystems have storage capacities ranging from 10 to 60 Mbytes. Designed to interface with standard Winchester and SA450 floppy disk drives, tape drives are compatible with IBM personal computers and compatibles. The tape systems use a MFM or GCR data encoding model. **I² Interface**, Canoga Park, CA **Write 170**

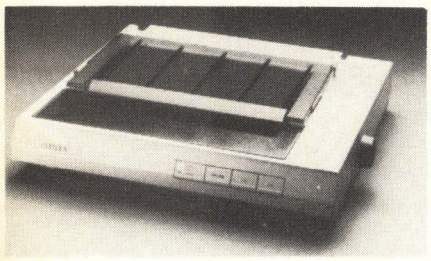
DISK DRIVE

The Atlas Disk Drive contains 160 Mbytes of memory and designed for multi-user network environments. Average on-line access time is 18 msecs, and the drive incorporates 50 read/write heads on three platters which can be stepped to a total of 160 cylinders or 8000 individual tracks. The system is interface and format compatible with ANSI/SMD specifications. **Alpha Data**, Chatsworth, CA **Write 159**

ANSI STANDARD TERMINALS

The XL series of ANSI-Standard terminals can be mixed and matched maintaining software compatibility. The Genie+Plus XL is used for form filling or block mode operation. For text editing, the Ambassador XL full-page has a portrait or landscape display of 80 characters and up to 60 lines. The Ambassador GXL features Tektronix 4010/4014 compatible vector graphics. The Guru has a 28 Kbyte memory and 66 X170 display format with both horizontal and vertical zoom. All terminals include a low-profile capacitive keyboard with a coil cable connection. Special function keys have 32 possible programmable levels. **Ann Arbor Terminals**, Ann Arbor, MI **Write 158**

DOT MATRIX PRINTERS



The MSP-10 and MSP-15 are the first printer products introduced by Citizen America. The printers operate in two modes, correspondence and graphics and utilize a push tractor paper feed. The MSP-10 is an 80 column printer which prints at 160 cps and the MSP-15 is a 136 column model which operates at the same speed. Their designs include nine-wire printheads and printing is bi-directional in text mode, and uni-directional in graphics mode. Prices are $549 (MSP-10) and $799 (MSP-15). **Citizen America**, Santa Monica, CA **Write 167**

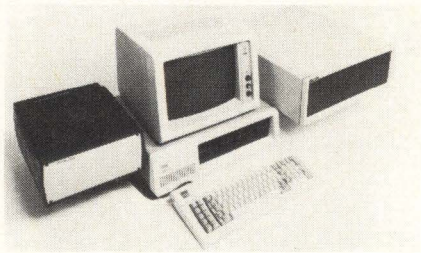
STANDALONE MODEM

The FI925L and the FI92IL models are equipped with a 32 character LCD that allows users to monitor operation, check signal quality, perform local and remote loopback, and change both local and remote strape settings. The FI925L modem provides 14,400 bps synchronous data transmission over unconditioned, leased lines, and has a built-in six-channel time division multiplexer. Fallback speeds of 9600, 7200 and 4800 bps, in full compliance with CCITT V.29, can be selected. A 9600 bps modem for use on four-wire, unconditioned leased lines, the FI92IL can accommodate an optional, four-channel time division multiplexer. Available port speeds are 9600, 7200, 4800, and 2400 bps. Price is $6,500 (1925L) and $2,500 (1921L). **Fujitsu**, Vienna, VA **Write 161**

STREAMER TAPE DRIVES

The 5¼″ streaming tape drives have interactive software support for Heurikon Minibox UNIX development systems. The drives can image copy entire disks or selectively back up and extract individual files. The drives use 3M data cassettes with 60 Mbytes of data storage capacity and have 90-ips read and write speed. **Heurikon**, Madison, WI **Write 173**

STD SUBSYSTEM



The Lynx I hardware/software system is an integrated Z80A-based STD subsystem for PC's which are used in distributed processing applications. Lynx can be permanently connected using the PC as a host, either via direct cabling or through modem communications, or used to download programs from the PC and operated completely independently. The Lynx I System uses Pro-Log's 7806 Z80A multifunction CPU card with dual UART and includes 2K PROM-based communications management system software in a 2732A EPROM and is supported by 2 Kbytes of RAM. The communications management system software includes a system initialize module, data transfer manager, asynchronous manager, I/O port, memory and UART drivers, all in the EPROM. Price is $695. **Pro-Log**, Monterey, CA **Write 162**

X.25 INTERFACE

The X.25 Release 4 is an enhancement to the Comten X.25 Interface to PDN software. It includes a packet adapter, PA5DSP, which supports the 3270 DSP and a terminal interface adapter, TIA1. Release 4 also supports Comten CNS in conjunction with packet-switched networks. The packet adapter connects to packet-switched networks and dynamically access SNA and pre-SNA IBM host applications. Using the X.25 terminal interface adapter, TIA1, asynchronous terminal users in a packet-switched network can access hosts connected to the Comten 3600 that are channel-attached IBM or compatible hosts. The X.25 also allows users to use CNS trunks to send data over packet-switched networks. **Comten**, St. Paul, MN **Write 175**

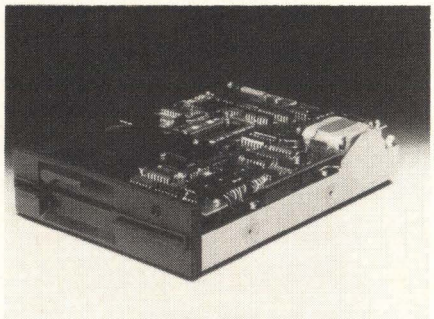
WINCHESTER SUBSYSTEMS

The MD4000 series Winchester subsystems are desk-top enclosures using 5¼″ form factor drives. The MD4260 is a 30 Mbyte Winchester subsystem incorporating a 60 Mbyte streaming tape drive for backup. The MD4260 has a Q-bus controller, a ¼″ streaming tape cartridge controller with a QIC-02 interface and emulates DEC's TSV05. The MLV11M 5¼″ Winchester controller, together with the 30 Mbyte drive, emulates three DEC RL02 drives. The MD4110 is a combination 30 Mbyte fixed Winchester and 10 Mbyte removable Winchester drive. The MD4910 integrates two 10-Mbyte removable Winchester drives. **Micro Technology**, Placentia, CA **Write 169**

DISK MEASUREMENT SYSTEM

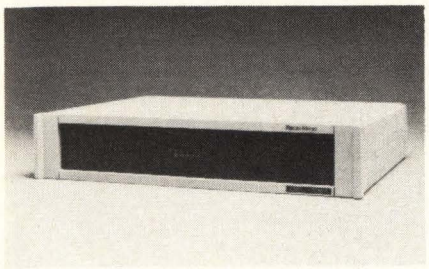
The SpectraScan PR-703A is a system for measuring the gap between a magnetic hard disk surface and its read/write head, or slider. The system uses spectroradiometry to interpret spectral patterns generated during the measurement process. The system uses a spectral scanning head to acquire the slider-to-disk interference spectra, and a PR-702AM Control Console with software algorithm to analyze the colors and compute and display flying height data. The optical detector consists of a 256-element thermoelectrically cooled diode array, with each diode sensitive to only a narrow band of wavelengths within the visible spectrum. Resulting measurements are reproducable to within .3 μin. **Photo Research**, Burbank, CA **Write 157**

HALF-HEIGHT 5¼″ DRIVE



The YD-380-1714 is a half-height 5¼″ floppy disk drive. It has a dual-speed feature which allows it to work with either the current standard format for 5¼″ media, or high capacity 5¼″ media. The drive can read and write data at 96 tpi track density on either the 1 Mbyte double-density, double-track format, or the high-capacity 1.6 Mbyte-unformatted 1.2 Mbyte-formatted disk. Using the YD-380-1714 to replace an 8″ drive does not require data to be rearranged. Price in quantities of 1,000 is $200. **C. Itoh**, Los Angeles, CA **Write 168**

MODEM DIAGNOSTIC UNIT



The CMS TCM-7 is a diagnostic unit which electrically surrounds modems to provide performance and alarm information to central site operators. Users gain centralized control to detect and diagnose problems at remote sites without having to replace non-diagnostic modems in the network. CMS TCM-7 can be installed with existing modems in single or mixed vendor networks operating at 1.2 to 16.8 Kbps, and can be used in either point-to-point or multidrop configurations. The device utilizes a secondary channel, carrying alarm and diagnostic information, without interrupting main channel data. Alarms provided by the CMS TCM-7 include main channel streaming, modem power failure and line failures. Diagnostic tests include modem self test, DTE loopback, line loopback, end-to-end error test and 1004 Hz tone generator. Price is $850. **Racal-Milgo,** Miami, FL **Write 179**

DISK SUBSYSTEM

The DML600 compatible disk subsystems encompass DEC's Micro-VAX and Micro PDP-11 Q-bus systems. The DML660 is a self-contained controller housed in a separate chassis for 19″ rack mounting with power supply and Q-bus extender. The system has 51-sector speed matching buffer, command stacking, seek overlap, concurrent data transfer, 170 bit ECC, and a 3.2 Mbyte/sec data transfer rate. It is available with Winchester disk drives in 404.5 Mbyte or 640.5 Mbyte capacities. **DML**, San Jose, CA **Write 171**

INTERNAL MODEM BOARD

The Cermetek 1200 PC is a 1200, 300 and 110 bps modem board for personal computers and compatibles. The modem is compatible with the Hayes communications control standard. The board is also Bell 103 and 212A compatible, permitting communication with 300 and 1200 bps modems. The 1200 PC automatically selects either touch-tone or rotary pulse dialing. It uses one expansion slot and can be used as an auxiliary RS-232 port. It has automatic speed and parity selection, diagnostics, and on-screen call monitoring. Price is $495. **Cermetek,** Sunnyvale, CA **Write 176**

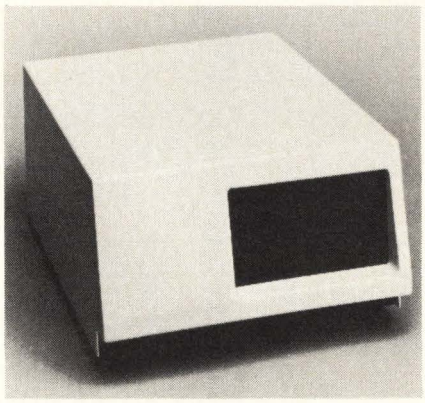
SCSI OPTION FOR RIGID DISK DRIVE

The Arapahoe 7110S fixed/removable disk drive has a SCSI logic module installed inside the drive enclosure. The drive stores 53.9 Mbytes on two 8″ rigid disks, with capacity equally divided between one fixed disk and one contained in a removable cartridge. Seek time is 35 to 20msecs and the disk has full-track caching buffer memory. Price is $3675. **Amcodyne,**, Longmont, CO **Write 174**

LASER PRINTER

The 2400 is a 24-page-per-minute laser printer based on the Xerox XP-24 engine. The Talaris 2400 has a resolution of 300 dpi, horizontally and vertically. The controller has a full-page bit-map for 8½″ by 11″ or 14″ output. A Motorola 68000 and 2 Mbytes of bit-map, program, and font storage provide for the creation of merged text and graphics. Paper capacity is 2000 pages. **Talaris Systems**, La Jolla, CA **Write 156**

WINCHESTER/FLOPPY SUBSYSTEMS

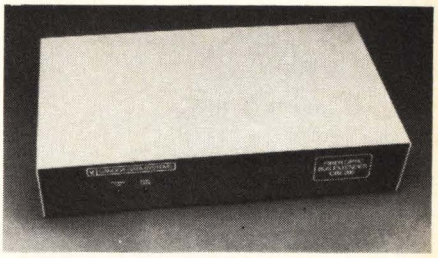


The CI-550 is a Winchester/Floppy Subsystem for Q-Bus Computers (including Micro/PDP-11 and MicroVAX). Each subsystem is formatted with 10 Mbyte of Winchester and 400 Kbyte of floppy storage. The CI-550 uses DEC's RQDX1 controller, utilizing the MSCP protocol. The CI-550 will read and write RX-50 floppy format and the Winchester drive has an average access time of 75 msec and a transfer rate of 625 Kbyte/sec. The CI-550 includes error detection and correction, error retry, block mode DMA, and bad block mapping. The CI-550 will operate in any Q-Bus 18 or 22 bit environment. Price is $2,295. **Chrislin Industries**, Westlake Village, CA **Write 160**

STORAGE CONTROL UNITS

Models 21 and 23 are recently introduced models of the IBM 3880 storage control unit. The units have a capacity of 8, 16 or 32 Mbytes of memory. Cache storage is composed of 2- and 4-Mbyte cards containing the 256 K-bit DRAM chips. The 3880 model 23 operates at data rates of 3 Mbyte/sec when attached to IBM 308X, 4381, 4341, and 303X processors equipped with 3 Mbyte/sec data streaming channels. The model 23 with 3380 DASD attached, handles application data for VM and MVS operating systems. The model 21, with its associated 3350 DASD, attaches to large IBM processors through 1.5, 2, or 3 Mbyte/sec channels. It operates as a paging device for VM and MVS systems and may be attached to two or four processor channels. Price ranges from $149,975 – $269,975. **IBM**, Rye Brook, NY **Write 172**

FIBER OPTIC LINK



The CBE-202 Fiber Optic Interprocessor Link comprises a parallel-to-serial multiplexer and a Bus Interface Module (BIM) which plugs into DEC PDP and VAX backplanes. A duplex fiber optic cable links the two multiplexers. The link operates at 250 kilowords/sec and can be as long as 2 kilometers. The Bus Interface Modules are software compatible with the DEC DR11-B or DR11-W modules. Price is $4,500. **Canoga Data Systems**, Canoga Park, CA **Write 177**

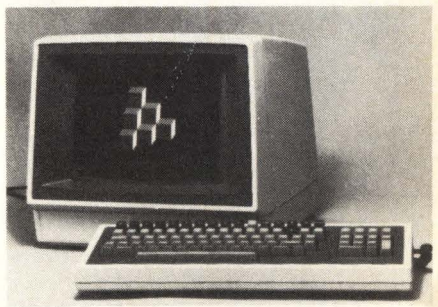
MASS STORAGE SUBSYSTEMS

The PC-8000 VM series of disk/tape subsystems is available in 42-, 85-, 168-, 335- and 480-Mbyte capacities. Average seek time is 165 msec and data transfer rates are 2.4 Mbytes/sec. The PC-8000 VM series is fully hardware and software compatible with the IBM 370-VM. Desktop models are available with capacities up to 335 Mbytes. Rack mounted versions have capacities of 1,000 Mbytes. Price is $9,900 and $13,900. **NMS**, Livermore, CA **Write 165**

TELECOMMUNICATIONS PACKAGE

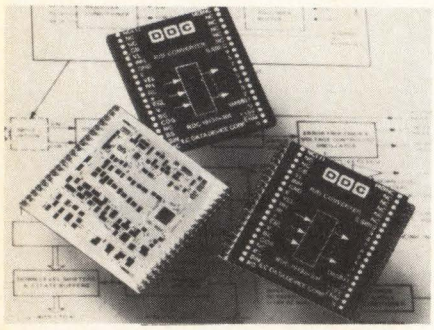
The Smartcom II 2.0 telecommunications software has terminal emulation and two protocols, working on IBM personal computers. Smartcom II 2.0 includes a Batch Command Set directory for storing up to 26 command sequences. Users can switch back and forth between voice and data transmission. **Hayes Microcomputer Products,** Norcross, GA **Write 178**

GRAPHICS TERMINAL



The GP-29 graphics terminal has Tektronix compatible graphics and DEC compatible text mode operation. It is offered as a stand-alone terminal or as a retrofit board for the Zenith Z29 terminal. The GP-29 has 128 Kbytes of memory and dual memory plane operation, where the user can create graphics with shades of gray or overlap two separate images on the screen. In the graphics mode, the GP-29 offers both 512×250 low resolution and 1024 × 500 high resolution operation. In the text mode, the GP-29 offers compatible operation with the DEC VT100 and VT220 terminals. Four text display formats are standard. Price is $1,695. **Northwest Digital**, Seattle, WA **Write 163**

HYBRID RESOLVER TO DIGITAL CONVERTER

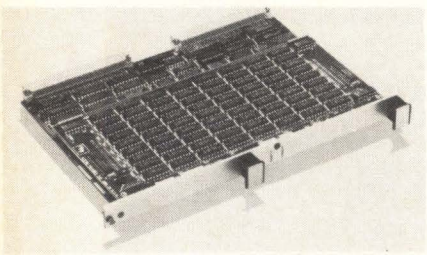


The RDC-19190 series of hybrid resolver to digital converters provides 1% linearity velocity. Converters are available in 10-, 12-, 14- and 16-bit resolution with accuracies to ±21, ±8.5, ±2.6 and ±1.3 min., respectively. Input frequency ranges for the various models are 360Hz – 22KHz, 600Hz – 22KHz, 1KHz – 3.5KHz and 360Hz – 3.5KHz. Resolver or direct inputs at 11.8V and 2.0V line to line are also offered. All units operate with a reference voltage range of 4–50V. Maximum tracking rates range from 400 to 6.3 RPS for 10- to 16-bit converters respectively. Price starts at $133. **ILC Data Device,** Bohemia, NY **Write 225**

64K S-RAM

The SRM2064C15 is a 64K bit static RAM with an access time of 150 nsecs. The device is fabricated using a proprietary 2-micron selectox silicon gate CMOS process. The SRM2064 operates at 150nsec while typically using 2 Ma of standby current and 25 mA while operating. Organized as 8K by 8 bits, the SRM2064C15 device is pin compatible with the HM6264. Price in quantities of 1,000 is $24.70. **S-MOS Systems,** San Jose, CA **Write 220**

VMEBUS MEMORY BOARD



The MM6200D/MM-6250D VMEBus memory module has a 4 Mbyte capacity with a 32-bit data path. The module employs a main board and an expansion board, each 2 Mbytes. Control circuits and DRAMs are contained on the MM-6200D main board, and the MM-6250D expansion board contains DRAMs. The expansion board is electrically connected to the main board via two connectors. DRAMs employed on either board must be either 64K or 256K and cannot be intermixed. Features include cycle times of 350 nsec, access times of 220 nsec and module selection of 10000 boundaries in the 4 Gbyte address field. Prices are $1,200 (MM-6200D/512A) and $750 (MM-6250/512A). **Micro Memory,** Chatsworth, CA **Write 184**

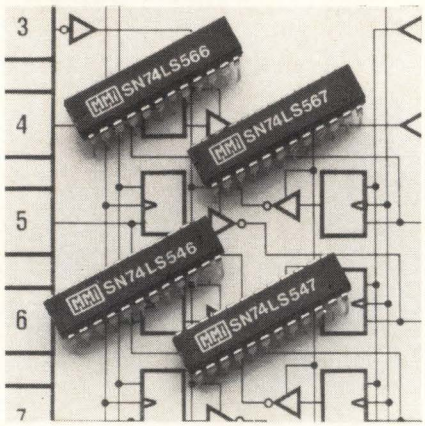
MEMORY BOARD FOR VME BUS

The IV-1612 Universal Memory board has 24 universal 28 pin memory sockets which can contain ROM, EPROM, EEPROM, or CMOS RAM. Chip sizes can be configured at 2K, 4K, 8K, 16K or 32K×8 bits. The IV-1612's 24 sockets are arranged into two separate banks of 8 and 16 chips. Each bank can be configured independently allowing a combination of memory chip types and sizes on the same board. The IV-1612 features 8-, 16-, and 32-bit data transfers, jumper programmable DTACK delay, write protection, and power up/down protection for battery powered CMOS RAM. Price is $695. **Ironics,** Ithaca, NY **Write 206**

SOLID STATE RELAYS

This line of AC Solid State Relays includes standard and custom design packages in both conventional chassis mounts and printed circuit pinouts. The line utilizes in-line pinouts such as SIP, DIP and Double DIP. The SSR's are designed to simplify mounting in standard IC pinouts for specialized applications in energy management. **Electronic Instrument & Specialty Corp.,** Stoneham, MA **Write 188**

INTERFACE DEVICES

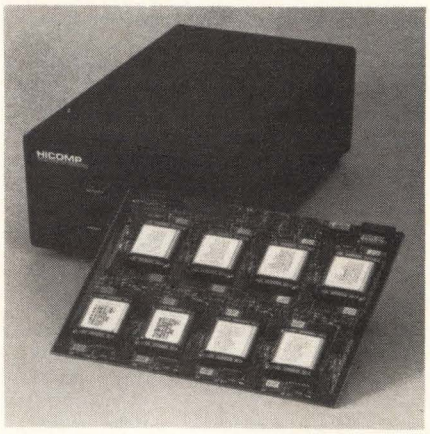


Two 8-bit registers and two 8-bit latches, each with a high output drive of 32 mA, are recent introductions from Monolithic memories. These devices have been designated SN54/74LS546, SN54/74LS547, SN54/74LS566, and SN54/74LS567. Both registers (SN74LS546/566) and latches (SN74LS547/567) have readback capability, or the capacity to register or latch data through their input pins and then return their contents back to those pins upon request, while continuing to function as conventional registers and latches on their output pins. The SN74LS546/47/66/67 interface circuits are bidirectional. The SN74LS546/547/566/567 interface circuits are available in plastic and ceramic, 24-pin packages. In quantities of 100, price is $6.18 (plastic) and $7.25 (ceramic). **Monolithic Memories,** Santa Clara, CA **Write 183**

DIAGNOSTIC PROM

The 53/63 DA841 is a PROM device which integrates system-level DOC. Internal nodes are both controllable and observable without external hardware. Organized 2,048 words deep by 4 bits wide, the 63DA841 PROM has edge-triggered registers, user-programmable initialization, synchronous and asynchronous output enable options, and three-state outputs. An on-chip output register provides a 2:1 chip count reduction, resulting in less power consumption while operating at a faster speed. PROM has a maximum set-up time of 40 nsec and a clock-to-output time of 20 nsec. Price in quantities of 100 is $27.85. **Monolithic Memories,** Santa Clara, CA **Write 199**

BUBBLE MEMORY STORAGE

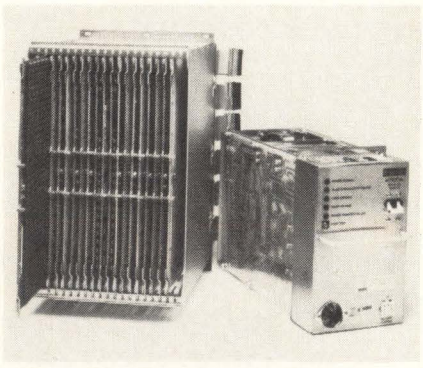


The Bubble Drive is a bubble memory storage board for the IBM PC. It provides either 256 Kbytes for 512 Kbytes of non-volatile, mass storage on a single card which plugs into the PC's I/O slot. It functions as a floppy disk and is fully compatible with PC-DOS 1.1 and 2.0. Standard features include write-protect, boot-enable and a self-installing feature which installs the Bubble Drive software after power-up. Price is $995-$1,495. **Hicomp,** Richmond, WA **Write 185**

CMOS MICROCOMPUTER

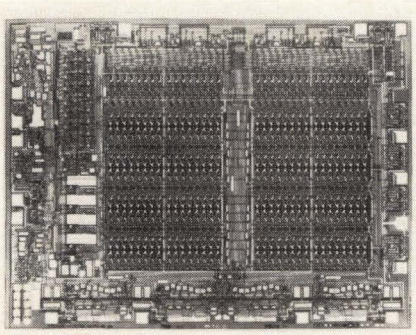
The 80C50 is an 8-bit single-chip CMOS microcomputer which is upward op-code compatible with HMOS devices supplied by Intel Corp. and NEC. The 80C50 is a static device that has an operating frequency range from 0 to 6 MHz and a Vcc range of 2.5V to 6.0V. The 80C50 has hardware and software-programmable powerdown features, typically consuming 15 mw of power in standby mode. Operating range is −40°C to +85°C. Price in quantities of 100 is $11.50. **Oki Semiconductor,** Sunnyvale, CA **Write 223**

64K RAM MEMORY SYSTEM



The EMCVT-780-4MB Memory System is designed as a field replacement for the original 16K RAM memory in VAX 11/780 CPUs and as an add-on upgrade system for any 11/780 CPU. When installed as an add-on system, the memory is configured in a CPU Expander Cabinet, which can also house two option slot assemblies for peripheral adapters. The 64K RAM memory system consists of 20-slot backplane, interleaved memory control set, a minimum of 4 Mbytes of memory, power supply and related hardware. The system uses EMC's VX-2MB-780 memory cards, which allow the 11/780 to have 32 Mbyte of memory per backplane. Price is $27,000-$31,000. **EMC,** Natick, MA **Write 208**

NONVOLATILE RAMS

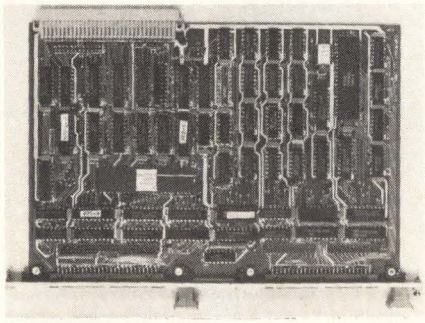


The H3500 is a 5V 256-bit non-volatile RAM. The circuit is organized as 64 × 4 bits with R/W operations performed in CMOS RAMs. A store operation transfers data in the RAM cells in parallel to the background EEPROM array. The recall operation restores the data to the foreground RAM cells. RAM access time is 300 nsec. The store operation requires 10msec and the recall operation requires 1 μsec. Typical operating current is 2mA and standby current is 100μA. Price is $6.30. **Hughes Solid State Products**, Newport Beach, CA **Write 202**

A/D CONVERTER

The ZAD-2735 is a 15-bit Sampling A-D Converter that is a drop-in replacement for Analogic's MP2735. The ZAD-2735 occupies the same footprint as the corresponding Analogic units and uses a monobit ladder network. In this network, equally-weighted current sources are used to add or subtract a single unit of current to the output as the input code changes incrementally. Because no switch or resistor can affect a current more than an eighth of full scale, the monobit approach is four times less sensitive to resistor errors than a binary coded network, where the most significant bit is half of full scale. The S/H amplifier has aperture uncertainty that supports 15 bits. Hold mode feedthrough is −90 dB. Aperture delay is typically less than 10 nsec. The ZAD-2735 has straight offset binary outputs. Price in quantities of 25 is $359-$379. **Silicon General**, Concord, CA **Write 186**

VME BUS INTERFACE



The IoVME-402 is a VME Bus Master which interfaces the VME bus to most 9-track tape drives and has SCSI interface, dual RS-232 I/O ports and vectored interrupts. The interface has an AM9516-based dual channel DMA controller. All DMA functions are programmable and chain loadable including: 24-bit addresses, 16-bit transfer counts, 8- or 16-bit data transfers and byte to word funneling. Price is $1,850. **Io Incorporated,** Tucson, AZ **Write 192**

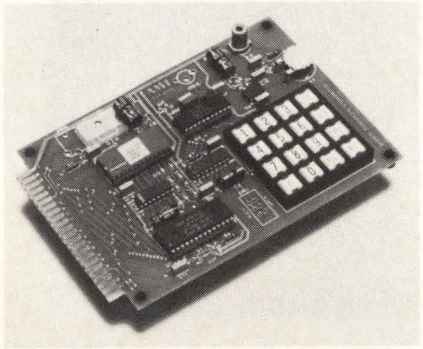
FLOATING POINT COPROCESSOR

The HP 200 is a Floating Point Coprocessor for the Hewlett-Packard 9000 Series 200 Desktop Computers. The FP200 is transparent to users of BASIC and Pascal and links by plugging the coprocessor board into an available I/O slot and adding the Infotek Systems software to the boot disk. Pascal operating system is now linked to the FP200. The Floating Point Coprocessor can be integrated with Assembly language programs. **Infotek Systems**, Anaheim, CA **Write 227**

DUAL WIDTH CONTROLLER

The Webster SRQD11-A is a dual width controller which interfaces to ST506 compatible 5¼" Winchester disk drives. It couples any size disk in this classification to all standard DEC operating systems without software modification. It supports drives ranging from 2 to 200 Mbtye with access times of 20 to 200 msecs. It interfaces to a range of Qbus CPUs including DEC's LSI11 and MicroVAX series as well as the Motorola 68000 and National 32032. Features include block mode DMA, bad block replacement and on-board self diagnostics. Price is $1,440-$1,110. **Webster Computer Company**, Sunnyvale, CA **Write 228**

SPEECH ROM

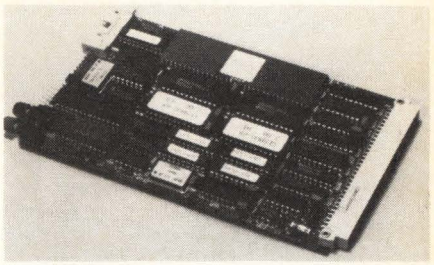


The S36128 Female Speech ROM specifically supports the S3620 LPC-10 Speech Synthesizer so that users can create their own messages using 100 seconds of stored speech. Pre-programmed into the chip are words and phrases suitable for telecommunications and industrial applications. Pauses of 40 msec to 200 msec in duration are included. Organized as 16,384 words by 8 bits, the S36128 is a static NMOS ROM programmed at mask level. TTL compatible on all inputs and outputs, the device operates from a single +5 power supply. Price in quantities of 1,000 is $12 -$15. **Gould**, Santa Clara, CA **Write 187**

DATA ACQUISITION SYSTEM

The ANDS 5600 data acquisition system features fiber optic communications links and local system intelligence. The ANDS 5600 can acquire data according to a predetermined list, and transmit the data back to the host. Data can be output from the ANDS 5600 under host control. All commands from the mainframe computer are acknowledged by the data acquisition equipment. Two fiber optic cables provide a 2 MHz serial link with 2000 feet separation between sites. The ANDS 5600 Data Acquisition System has a library of 90 analog and digital I/O module configurations which provide processing at 10 msec/point with 14-bit resolution. **Analogic,** Peabody, MA **Write 226**

MC68000 EUROBOARD



The Gesmpu-4A is a microcomputer board built around the MC68000 16-bit microprocessor. The microprocessor operating at an 8MHz clock rate. Clock frequency is generated by an onboard crystal oscillator. The board has four JEDEC sockets to accommodate 128 Kbytes of EPROM and 16 Kbytes of static RAM. The Gesmpu-4A has a triple 16-bit timer and an RS-232-C serial interface with fully programmable baud rate. Price is $475. **Gespac**, Mesa, AZ **Write 224**

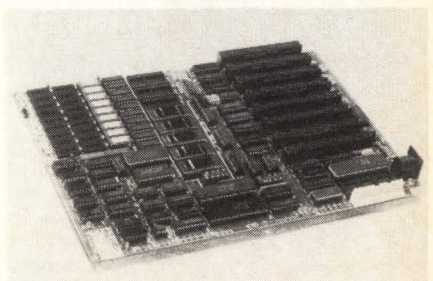
BUBBLE MEMORY MODULES

The FBM-M128TA and TC are 128 Kbyte bubble memory modules which include a timing generator, sequencer, voltage detector, controller and a diode. The modules use TTL level I/O and have file memories with an access time of 12.5 msec. Transfer rates are 100K bits/sec and 64 byte clock transfer. The modules are 3-bit burst error correctable. Price in quantities of 1,000 is $177. **Fujitsu America,** Lake Bluff, IL **Write 191**

256K EPROM

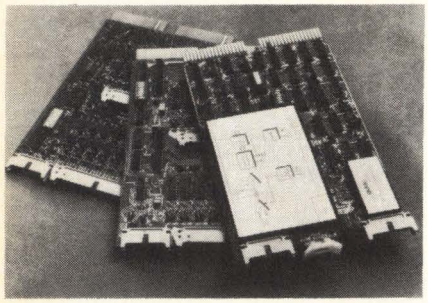
The 27256-2 is a 256K EPROM with a read access time of 200 nsec. Each type of high-density 27256 EPROM offers 32 Kbytes of storage capacity and has applications in storing operating systems, diagnostic programs and application programs for data processing, industrial and communications systems. The 27256 is compatible with high-speed Intel microprocessors and microcontrollers such as the iAPX 186 and the 8031. Price in quantities of 10,000 is $78. **Intel**, Santa Clara, CA **Write 196**

IBM PC COMPATIBLE MOTHER BOARD



The PC-128 mother board is hardware and software compatible with the IBM PC/XT. The PC-128 includes 128 Kbyte (256 Kbyte optional) RAM internal memory and a 16-bit 8088 CPU that can address 864 Kbyte of additional system memory. Eight IBM-compatible I/O interface slots support disk controllers, multifunctions boards, expansion memory, monochrome or color monitor controllers, and modems. Three DMA channels are available on the I/O bus. Eight extended ROM sockets are included for use with either 8K × 8 or 16K × 8 EPROM chips. Price is $445. **Sigma Information Systems,** Anaheim, CA **Write 219**

Q-BUS A/D BOARDS

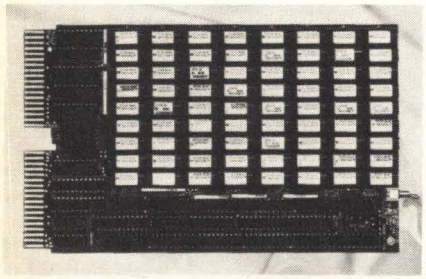


The 1114AD is a Q-Bus compatible 1114AD board which has 8 software programmable ranges from 10mV full scale to 10V full scale. The 1114AD has unrestricted mixing of high and low level signals plus 12-bit resolution. For fixed and changing I/O environmnets, the 1114AD has software selection by channel of thermocouple type, RTD, load cell and strain gauge inputs. Companion boards provide expansion to 128 channels with 250V common mode protection. **Adac,** Woburn, MA **Write 213**

MULTIBUS II BACKPLANES

The microrack combines the Multibus II system with the Multibus I by incorporating a 6 slot Multibus I backplane with a 10 slot Multibus II PSB backplane and a 6 slot LBX. It consists of a 9U high, 19″ wide KM6 sub-rack in an enclosure and is wired for immediate use. There are four cooling fans and an extracter fan with a 400 Watt BICC-Boschert open frame switched mode power supply. Space is allocated within the system for memory storage in the form of a Winchester hard disk drive or two half 5¼″ Shugart compatible floppy disk drives. Space has also been allocated for single height Eurocards for expansion. **Bicc-Vero**, Hauppauge, NY **Write 201**

TWO MBYTE ADD-IN CARD



The Pincom 23SX is a 2Mbyte dual wide card for Q-Bus systems. The 23SX uses 64K or 256K of RAM and has block mode, CSR parity, and standard 22-bit addressing. Other features are socketed RAMs, On-line/Off-line switch, LED Run/Error indicator and additional RAM. **Standard Memories,** Santa Ana, CA **Write 182**

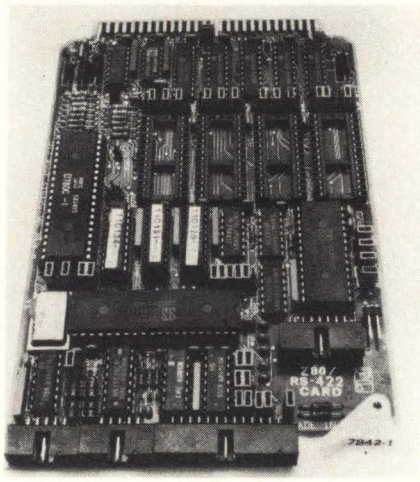
ANALOG I/O BOARDS

The DT1771 series consists of analog I/O boards and real-time support software for the UNIBUS. Each product in the series is equipped with A/D, D/A, digital I/O, and programmable timer subsystems. The architecture is based on an on-board, 8 MIPS, 16-bit, bit-slice processor optimized for analog I/O operations, and a 64K memory buffer. Eight different modes of analog I/O are available: continuous data acquisition, countdown data acquisition, pre- and post-event sampling, signal averaging, histogramming, continuous D/A and D/A with external initiation. Other features include multiple channel scanning modes, data collection modes, and triggering schemes as well as digital I/O. Price is $7,170-$7,870. **Data Translation,** Marlboro, MA **Write 194**

CACHING DISK CONTROLLER

The PM-3010 is a single board disk controller with an integral 128 Kbyte cache RAM. The cache can be expanded up to 16 Mbytes by adding optional memory expansion boards. The PM-3010 uses a true sector caching algorithm as opposed to a track cache. Up to 128,000 sectors can be individually stored in cache with an access time not exceeding 400 μs. Up to four ST506, SA1000 or SMD Winchester drives plus four floppy drives can be controlled by a single 5¼″ extended form factor board. The controllers are SCSI compatible and have an average data rate of 1.0 Mbyte/sec. Price is $740. **Distributed Processing Technology,** Maitland, FL **Write 193**

Z80A-BASED CPU

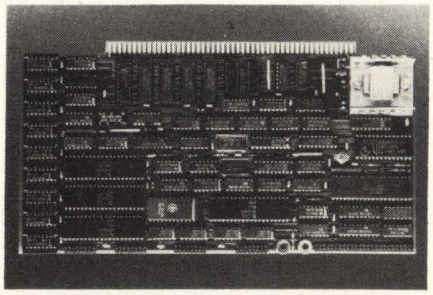


The 7842 is a STD multifunction Z80A-based CPU card which has two independent serial data communications channels with multi-drop capability. One channel provides RS-422 interface levels, and the other is configurable to either RS-232 or RS-422 interface levels. The 7842 operates with a maximum synchronous data-signalling rate of 500K bits per second and data transmit/receive distances of 4,000 ft at 90K baud. The 7842 supports asynchronous, byte-synchronous and bit-synchronous protocols. It has onboard dual UART Serial I/O, and two 8-bit programmable counter/timer channels with Z80 mode-2 vectored interrupts. Four memory sockets provide 128 Kbytes of onboard memory capacity. Price is $425. **Pro-Log**, Monterey, CA **Write 209**

128K STATIC RAM MODULE

The 9634 static RAM Module is a static random access memory module compatible with any M6800/M6809 microprocessor. Designed to comply with the timing and signal level requirements of a buffered M6800/6809 bus, it is configured as a single 128K block. It occupies two 64 Kbyte pages of memory. The 9634 is equipped with the circuitry and a connector to permit its use with the 9639 memory management processing module allowing dynamic task allocation in the memory map under software control. Up to 1.0489 Mbytes are addressable with this system. Price is $1,350. **Creative Micro Systems,** Los Alamitos, CA **Write 204**

S-100 SINGLE BOARD COMPUTER

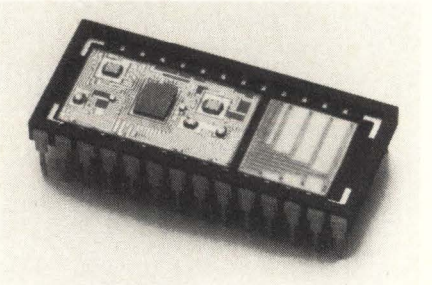


The Systemaster II is an S-100 master SBC which uses Zilog Z80B CPU, or optional Z80H running at 8MHz. The 128K of parity checked RAM is divided into two 64K banks. Two RS-232 serial ports provide either synchronous or asynchronous communications with software programmable baud rates. Two 8-bit Centronics-compatible parallel ports may be combined to provide a 16-bit port; modified to provide a SCSI interface; or with an optional adaptor, configured to provide an IEEE 488 interface. Price is $679.50. **Teletek**, Sacramento, CA **Write 221**

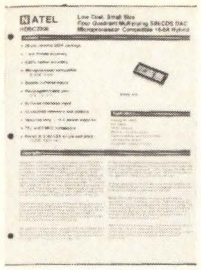
FLIP-FLOP ICs

The CD54/74HC175 Quad D flip flops are intended for high-speed CMOS designs and the CD54/74HCT175 devices are speed, function, and pin compatible with LSTTL logic devices. These latter types directly replace LSTTL devices in existing systems that can benefit from lower power consumption of CMOS technology. Changes on the Q and $\overline{Q}$ outputs occur on the positive edge of the clock pulse. All four flip flops in a package are controlled by a common clock signal. Resetting of each flip-flop is accomplished independently of the clock by a common Master Reset input. Typical propagation delay from a clock input to a data output at the Q or $\overline{Q}$ terminal is 14 nsec with a capacitive load of 15 pF and Vcc = 5V. Typically, the devices can operate up to a maximum clock frequency of 50 MHz. Price in quantities of 100 is $.83. **RCA**, Somerville, NJ **Write 211**

SIN/COS DAC

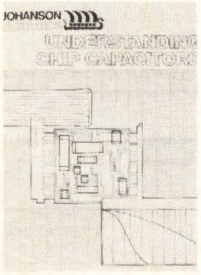


The HDSC2306 is a four-quadrant multiplying sin/cos DAC for industrial applications. It is compatible with 8- and 16-bit microprocessor and has 1 arc-minute accuracy and 16-bit resolution. It requires ±15V power supplies and has a radius accuracy of 0.03%. The 2306 is used for coordinate conversion, low frequency oscillators, axis rotation and digital-to-resolver conversion. Features include double buffered inputs, buffered reference input, dc-coupled reference and outputs, TTL and CMOS compatibility and pin-programmable gain. Price is $180. **Natel Engineering,** Simi Valley, CA **Write 203**



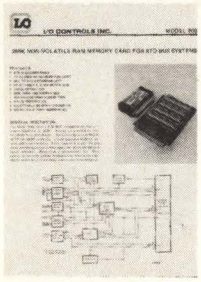
Data Converter Data Sheet. This 8-page data sheet from Natel Engineering describes the HDSC2306, a four quadrant, 16-bit, multiplying sin/cos DAC, that is packaged in a 28-pin hybrid ceramic DDIP. The converter has 8- and 16-bit microprocessor compatibility, 1 arc-minute accuracy, 0.03% radius accuracy and pin-programmable gain. The brochure includes features, specifications, ordering information, and applications information.

Natel **Write 257**



Chip Capacitor Booklet. This 25-page booklet from Johanson Dielectrics describes multilayer ceramic capacitor chips. It covers the electrical properties of capacitors, classes of dielectric materials, methods of testing electrical parameters and answers questions concerning geometries, terminations and attachment methods.

Johanson Dielectrics **Write 261**



256K RAM Memory Card Bulletin. This bulletin from I/O Controls Inc. describes its model 2002 STD Bus Card. The card has a non-volatile memory capability of 256K RAM and is 8085, 8088 and Z80 compatible. Also included is a block diagram showing the circuitry and major components.

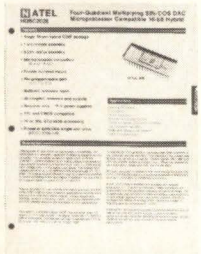
I/O Controls **Write 266**

EMI/RFI Filter Catalog. This 24-page filter catalog for printed circuit board applications from Murata Erie North America contains technical information on its line of feed thru capacitors; ferrite bead inductors for noise suppression and spurious oscillation prevention; EMI suppression filters; and noise filters. Also included are performance specifications, quality assurance standards and application information.

Murata Erie **Write 256**

Product Guide. This guide from Data I/O describes its line of PROM and logic device programmers, programming systems, and software. Product descriptions include applications in software development, programmable logic design, or programming, as well as specifications are included.

Data I/O **Write 260**



Sin/Cos DAC Data Sheet. This 8-page data sheet from Natel Engineering Co. describes a four-quadrant multiplying sin/cos DAC. The HDSC2026 is both 8- and 16-bit microprocessor compatible and is packaged in a 36-pin hybrid DDIP. Also included are features, specifications, description, ordering information and applications.

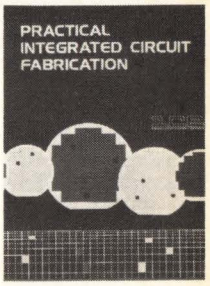
Natel Engineering **Write 263**

Satellite Communications Brochure. This 18-page brochure from the Satellite Communications Div. of M/A-COM DCC provides an overview of satellite communications products. Included are TDMA, SCPC, digital speech interpolation, voice, audio, and video codes, and video teleconferencing, as well as a general description of turnkey earth station projects and support services.

M/A COM DCC **Write 264**

A/D Converter Bulletin. This bulletin from Gould's Defense Electronics Div. describes its enhanced Delta Modulation Encoder model G-500. The bulletin covers the 20-bit EDME's design and characteristics. The publication also compares data acquisition via EDME vs. conventional analog-to-digital converters.

Gould **Write 254**



Integrated Circuit Guide. This 350-page guide from Integrated Circuit Engineering Corp. provides an overview of IC processes. The advanced silicon-gate CMOS process (HCMOS) is emphasized. Illustrations include charts, diagrams and photographs.

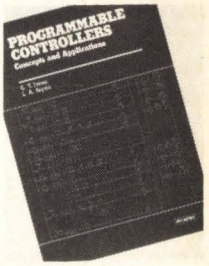
Integrated Circuit Engineering Corp. **Write 267**

Fiber Optics Application Note. This four-page application note from Artel Communications Corp. describes its fiber optic system designed for remote Computervision Corp.'s Instaview C color workstations. The note explains how the system uses fiber optics to obtain transmission of high resolution RGB graphics video and data. System examples and a section on set up and operation are also provided.

Artel **Write 258**

Computer Equipment Catalog. This 132-page catalog of computer equipment from Digital Equipment Corp. describes terminals, software and communication products for VAX, PDP-11, and personal computers. New products featured include DECtalk, OPS5 Artificial Intelligence software and LVP16 color graphics pen plotter. Product categories include personal computer add-ons, graphics, communications, and VAX-clusters. Ordering information and an add-on consulting telephone number are provided.

DEC **Write 255**



Programmable Controllers Book. This 324-page book from International Programmable Controls provides information concerning the design and construction of programmable control systems. Topics discussed are basic concepts of programmable controllers; understanding hardware and software components; and outline procedures for installation, start-up and maintenance.

IDP **Write 265**

CALENDAR

November 28-30

The UNIX Applications Forum: Directions '85. Los Angeles, CA. Contact: Yates Ventures, 4962 El Camino Real Suite 111, Los Altos, CA 94022. (415)964-0130.

December 1

Computer China '84. Peoples' Republic of China. Contact: Kallman Associates, 5 Maple Court, Ridgewood, NJ 07450. (201)652-7070.

December 3-4

Discovering Lotus 1, 2, 3. Ft. Lauderdale, FL. Contact: Data-Tech Institute, PO Box 569, Nutley, NJ 07110. (201)661-2300.

December 3-5

Power of Personal Computers. Phoenix, AZ. Contact: The Institute for Professional Education, 1515 N. Court House Rd., Suite 303, Arlington, VA 22201.

December 4-7

Designing Digital Communications Systems. Washington, D.C. Contact: Ruth Dordick, Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213)417-8888.

December 4-7

Implementing Local Area Networks. Palo Alto, CA. Contact: Ruth Dordick, Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213)417-8888.

December 10-12

Personal Computers in Business—The Micro-Mainframe Connection. New York, NY. Contact: National Institute for Management Research, PO Box 3727, Santa Monica, CA 90403. (213)450-0500.

December 11-14

Computer Network Design and Protocols. Palo Alto, CA. Contact: Ruth Dordick, Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213)417-8888.

December 13-14

Computer Aided Design and Manufacturing Technology. New Orleans, LA. Contact: The American Society of Mechanical Engineers, 345 E. 47th St., New York, NY 10017. (212)705-7722.

December 18-20

Data Communications: Network Design Integration and Applications. Boston, MA. Contact: Software Institute of America, Inc., 8 Windsor St., Andover, MA 01810. (617)470-3880.

January 8

Invitational Computer Conferences. Irvine, CA. Contact: The Invitational Computer Conferences. 3151 Airway Ave., Bldg. C-2, Costa Mesa, CA 92626. (714)957-0171.

January 14-17

ATE West '85. Anaheim, CA. Contact: Morgan-Grampian Exhibitions Group, Two Park Ave., New York, NY 10016. (212)340-9780.

January 16-21

COMMTEX International. Anaheim, CA. Contact: NAVA, The International Communications Industries Assoc., 3150 Spring St., Fairfax, VA 22031-2399. (703)273-7200.

January 16-18

The Business Telecommunications Exposition. Parsippany, NJ. Contact: T.E.G. Inc., The Exposition Group, 83 Barnegat Blvd., Barnegat, NJ 08005. (609)698-7020.

January 23-24

10th Annual Electronics Show. Del Mar, CA. Contact: San Diego Electronics Show, c/o Epic Enterprises, Show Manager, 6151 Fairmount Ave., Suite 115, San Diego, CA 92120. (619)284-9268.

January 28-31

Communication Networks Conference & Exposition. Washington, D.C. Contact: Communication Networks, Box 880, Framingham, MA 01701. (617)879-0700.

January 29-31

Industrial Productivity Conference and Exposition. Orlando, FL. Contact: Society of Manufacturing Engineers, PO Box 930, Dearborn, MI 48121. (313)271-0023.

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