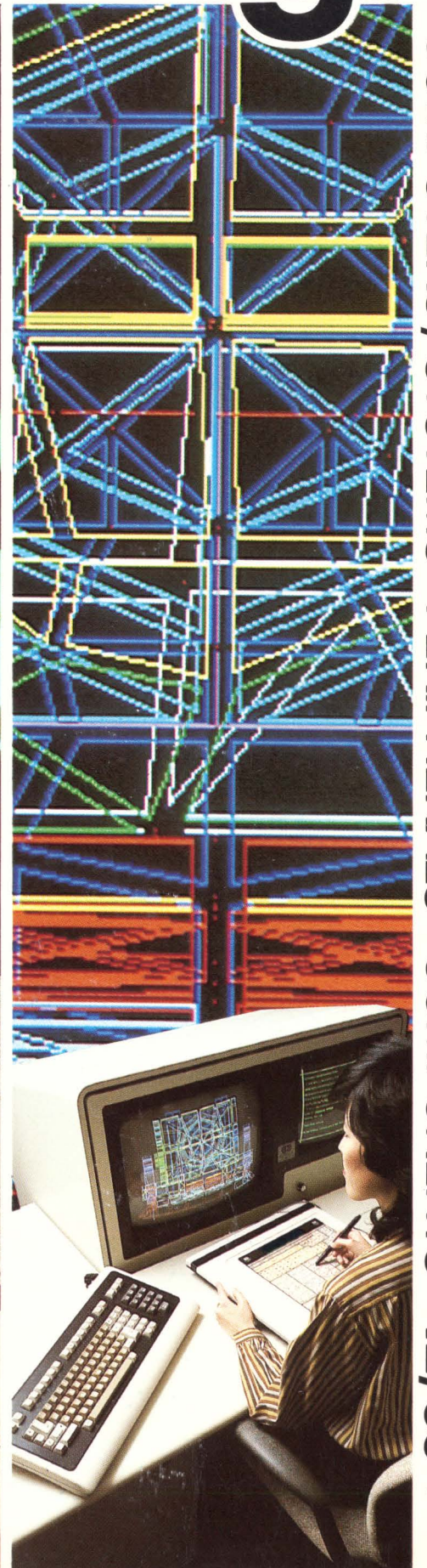
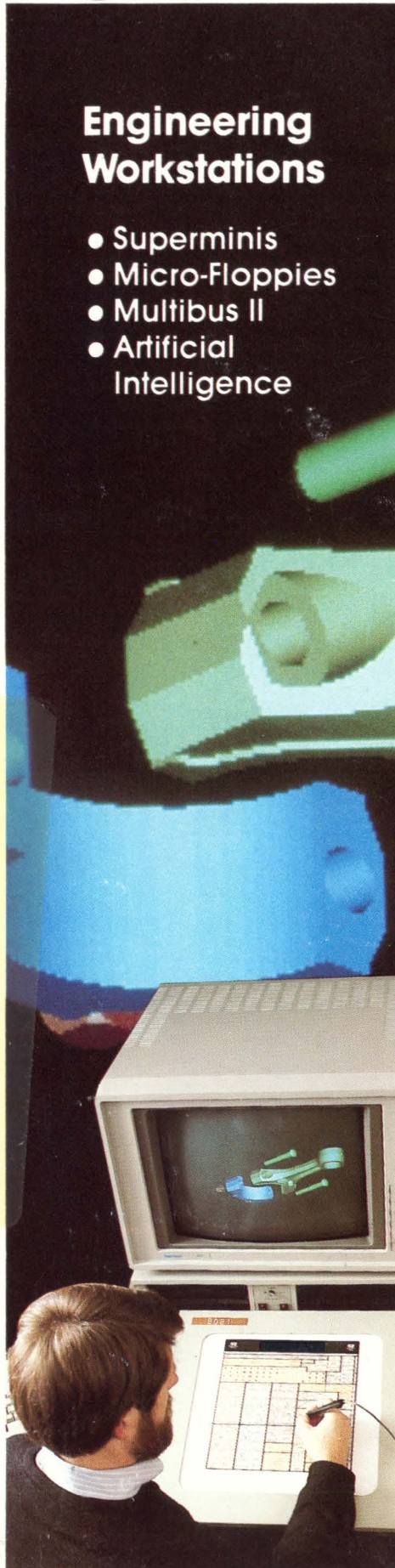
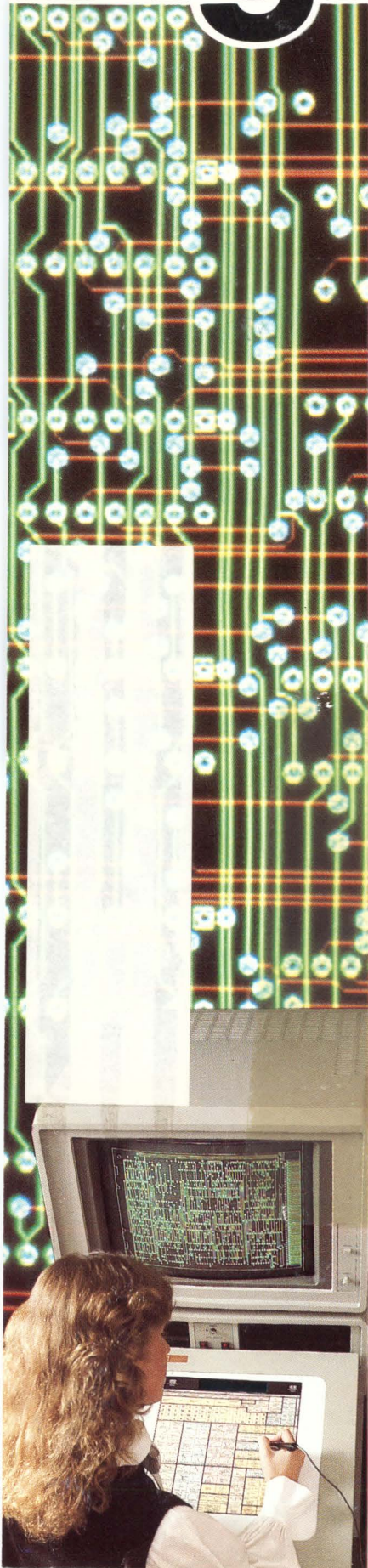


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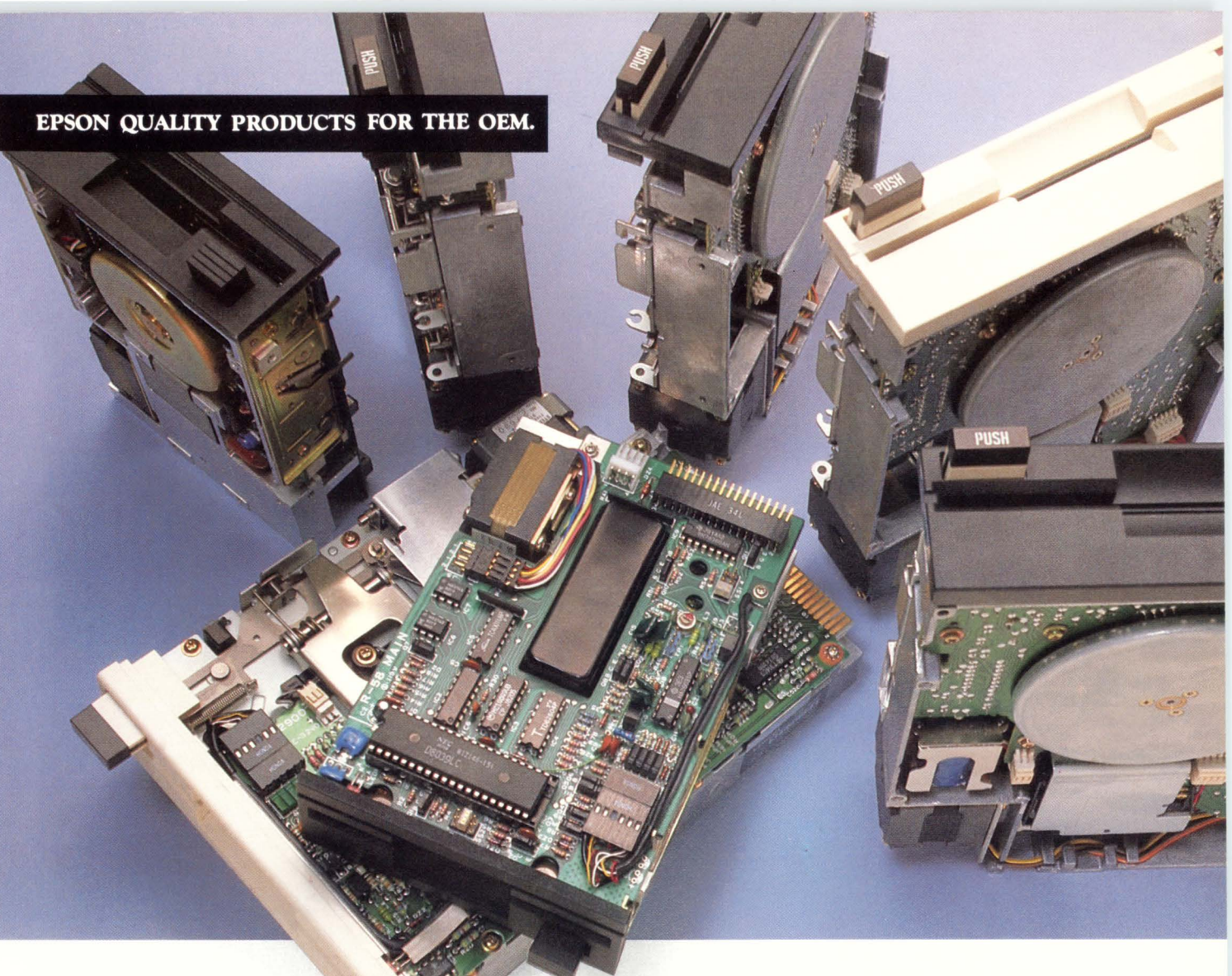
COMPUTERS/SYSTEMS - PERIPHERALS - COMPONENTS - 12/83

Engineering Workstations

- Superminis
- Micro-Floppies
- Multibus II
- Artificial Intelligence



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	4" x 1.57" x 5.98"		5.75" x 1.6" x 7.68"			5.75" x 1.1" x 9.27"
Max. Capacity (2 Sides) (Unformatted)	500 KB	1000 KB	500 KB	1000 KB	1604 KB	500 KB
Drive Motor Speed	300 RPM	300 RPM	300 RPM	300 RPM	360 RPM	300 RPM
Track Density	67.5 TPI	135 TPI	48 TPI	96 TPI	96 TPI	48 TPI
Access Time	6 msec	3 msec	6 msec	3 msec	3 msec	15 msec

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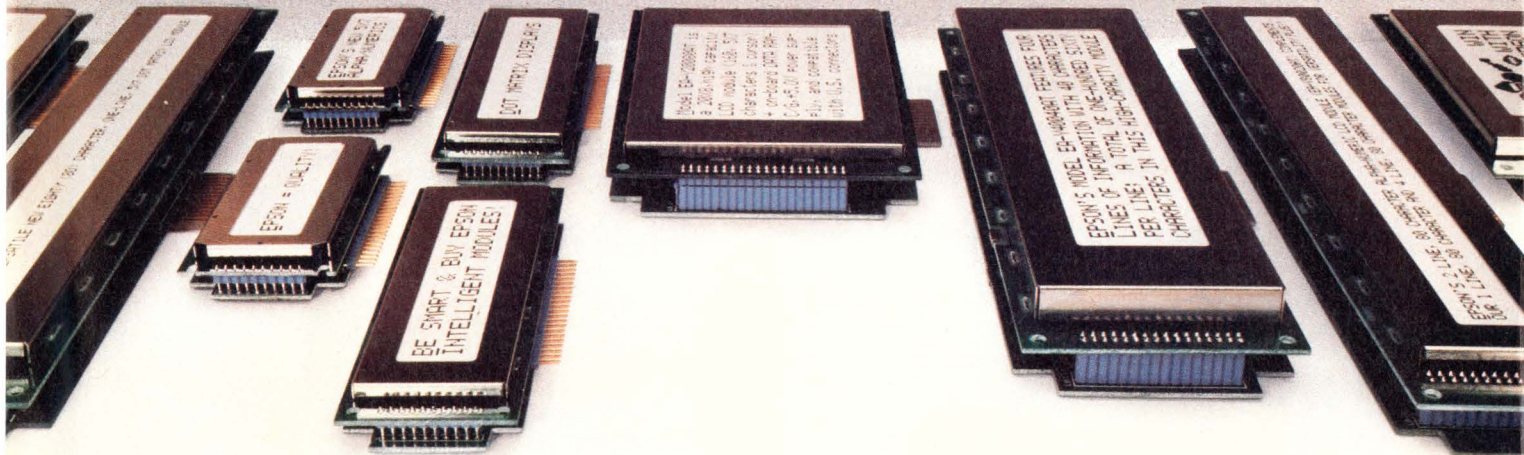
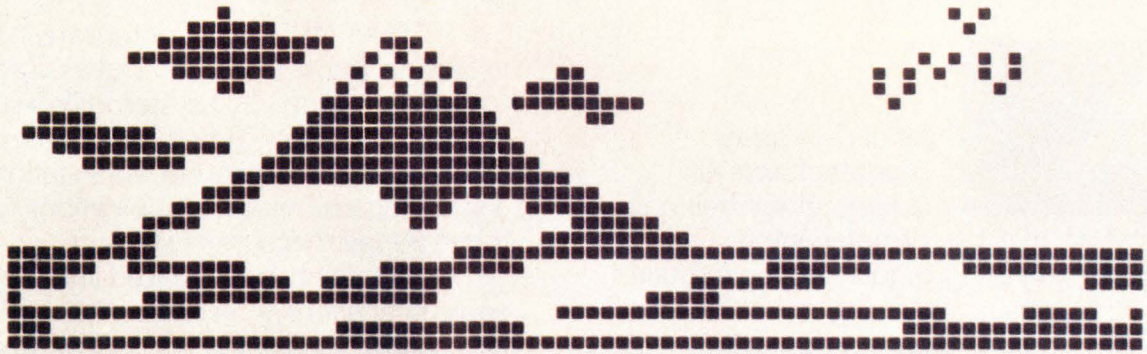
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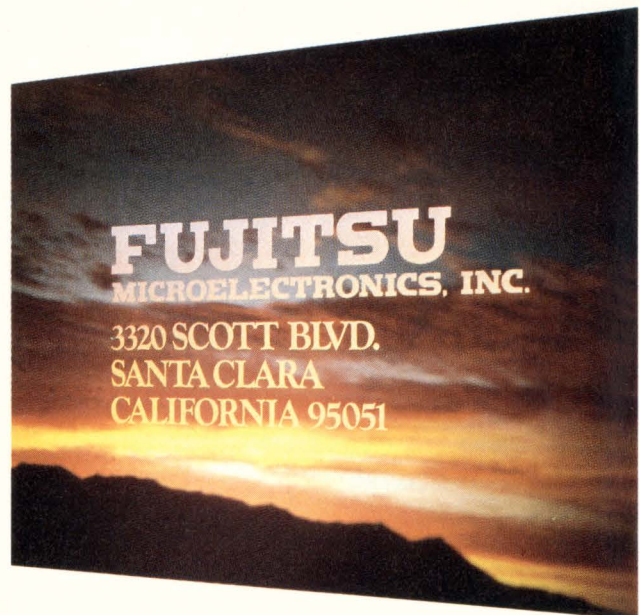
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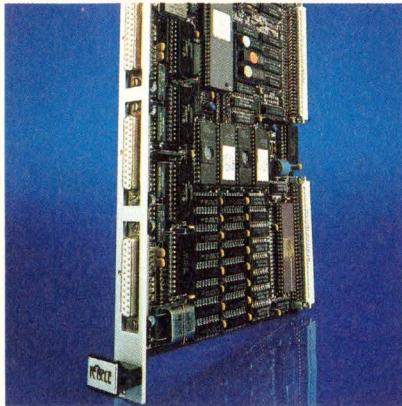
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Write 18 for LSI-11

Write 19 for Micro/32

Write 22 for REGULUS

Digital Design



p. 39 (Photo courtesy Force Computer)



p. 87 (Photo courtesy Aydin Corp.)



p. 94 (Photo courtesy Harris Corp.)

Cover

Photos of high performance workstations courtesy of Control Data Corporation, Minneapolis, MN. The new ICEM Ergonomic Workstation (right) is shown displaying a color wire frame of a radar screen. Tektronix 4115 workstations (center and left) display Control Data's ICEM (Integrated Computer-aided Engineering and Manufacturing) applications. An exploded view of an automotive connecting rod (center) uses ICEM Solid Modeling and the complex printed circuit board layout (left) is designed with ICEM Schematics.

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COMPUTERS/SYSTEMS

Industry Spotlight

Looking Ahead: A Forecast For The '80s 58

The predominant trend in computer systems in 1983 and continuing into 1984 is for an increase of performance at lower levels of cost.

1983 Salary Survey And Employment Trends 66

An increasing hope for the industrial sector resides not only in the continual modernization of plants and equipment, but in a new emphasis on employee satisfaction.

The Debut Of Second Generation Artificial Intelligence 82

Artificial Intelligence is that part of computer science that is concerned with the symbol-manipulation processes that produce intelligent action.

Engineering Workstations Meet Demands For Individual Design Needs 87

While there has been new development of workstations, it is the performance not the applications that are radically changing.

Superminis Offer A Cost-Effective Solution For High Throughput 94

Superminis have been preferred to mainframes for a variety of applications, primarily due to their lower cost.

Integration Issues For The First All Digital Commercial Aircraft .. 101

The ability to quickly and accurately diagnose conditions and potential problems prompted the move to digital systems.

PERIPHERALS

The Micro-Floppy Race Tightens 78

With the demise of IBM's Demi Diskette, three micro-floppy media contenders remain in the running.

Graphics System Design 34

Filtering Improves Effective Resolution

COMPONENTS

The Designer's Guide To The VME Bus — Silicon Simplifies Building Block Approach 39

The definition of the VME bus is a departure from previous architectures that may have grown haphazardly around the support of one particular processor.

Multibus II — A Top Down Approach 71

Today the Multibus is one of the most popular busses in the marketplace, and over 1,000 boards are available for the designer to choose from.

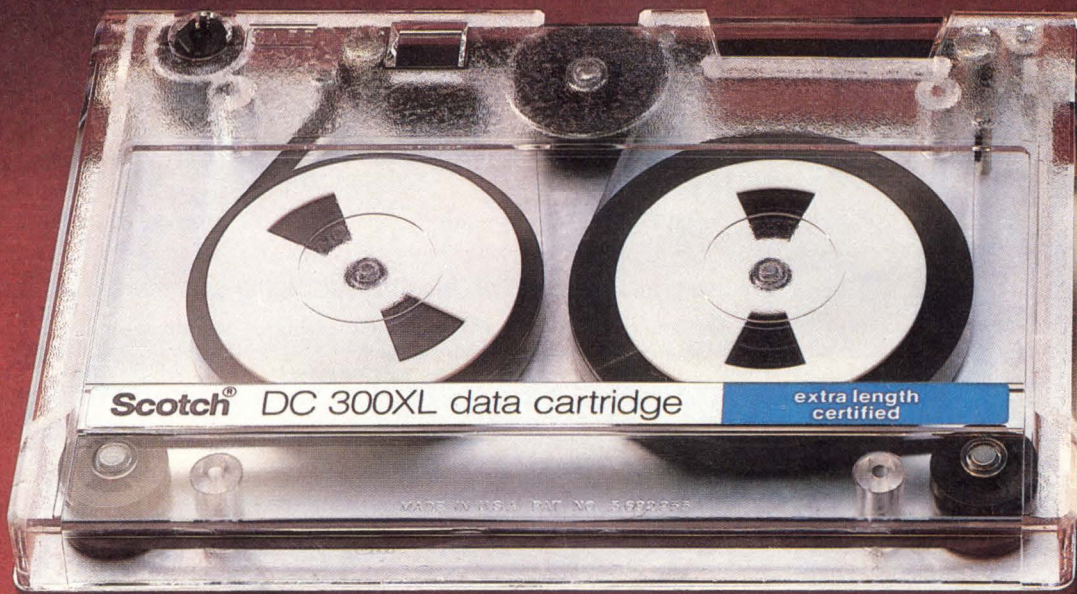
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The One-Board Solution • Custom Chip Boosts Speed Of Workstation

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Expanding The Bandwidth Of Optical Fiber Systems

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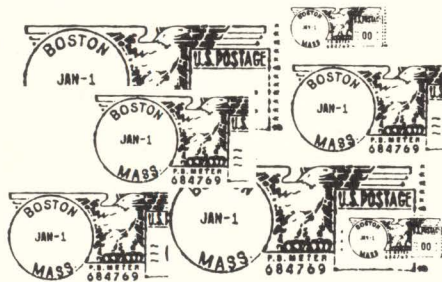
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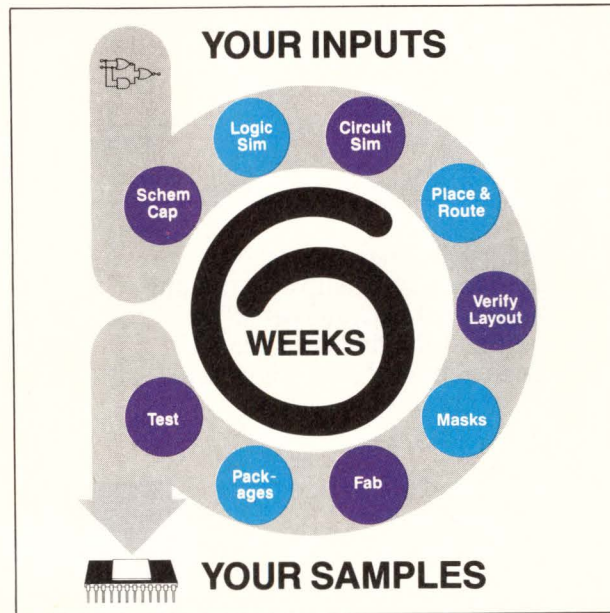
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2. Tomography Preprocessing	60 sec.	25 sec.	16 sec.	12 sec.
3. Multispectral Image Classification (512 x 512 pixels 8 Bands, 4 classes)	49 sec.	25 sec.	13.3 sec.	10.5 sec.
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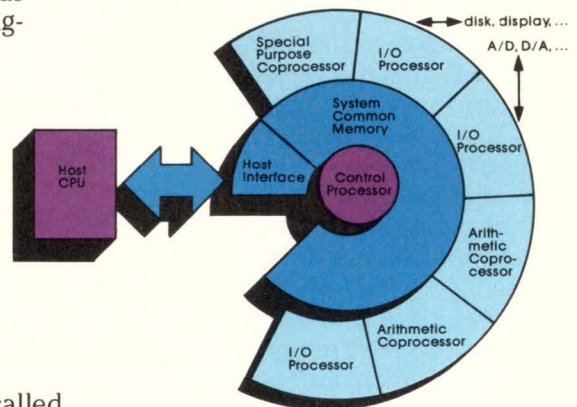
*Based on U.S. Domestic Prices

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FPS-5000 Series Architecture



introduces the first the \$2,000/MFLOP barrier.

by a combination of independent I/O Processors and the central Control Processor.

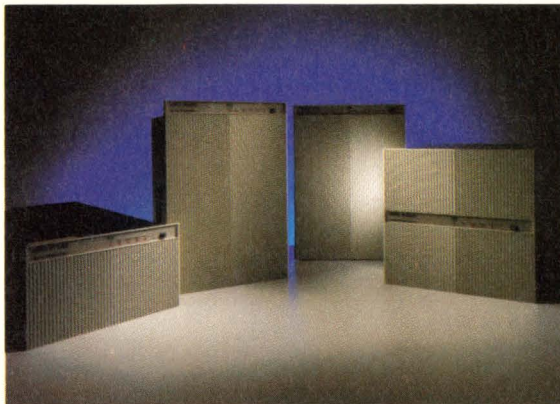
Each Arithmetic Coprocessor, with synchronous architecture to allow simple application debugging, functions as a self-contained unit.

The new Multiple Array Processor Execution Language (MAXL), based upon FORTRAN 77, allows the user to construct an integrated system environment which can be tuned to application requirements.

Increased performance can be achieved by adding Arithmetic Coprocessors as a field-installable upgrade as the user's requirements evolve.

Compatibility

The FPS-5000 Series maintains software compatibility with previous FPS 38-bit processors and is supported on a range of host computers. Thus, the extensive



software support developed for FPS-100 and AP-120B products is maintained and users are able to move existing applications onto the FPS-5000 Series with minimal effort.

Quality and Reliability

The FPS-5000 Series was designed and built with the same quality standards inherent in all of the previous Floating Point Systems products—standards that have earned those products a reputation for unprecedented reliability and one of the best

meantime between failure (MTBF) rates in the industry.

The Series is backed by the same outstanding worldwide support services that distinguish Floating Point Systems from other manufacturers.

For more information about how the FPS-5000 can be used in your specific application, call (800) 547-1445 or your local sales office.

The world leader in array processors.



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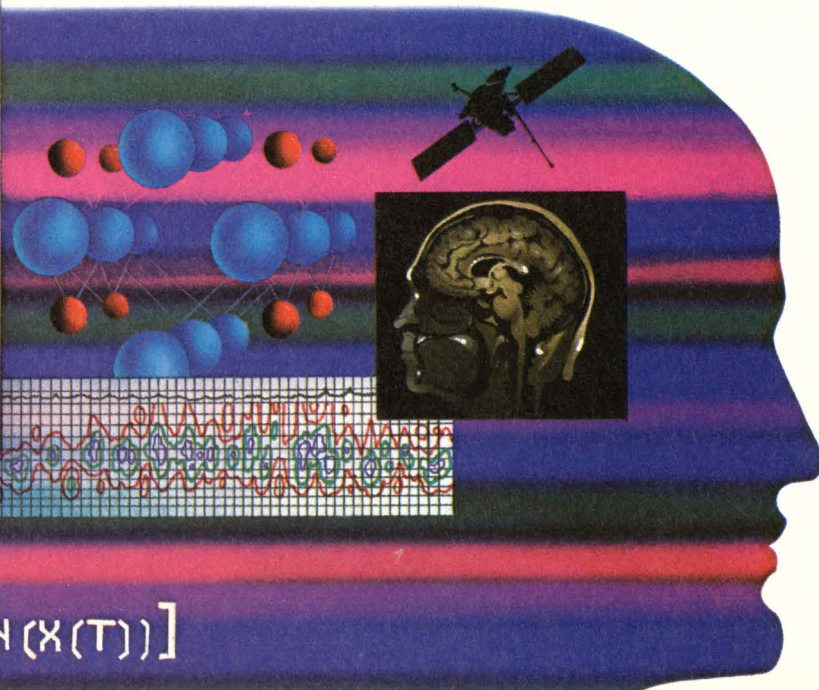
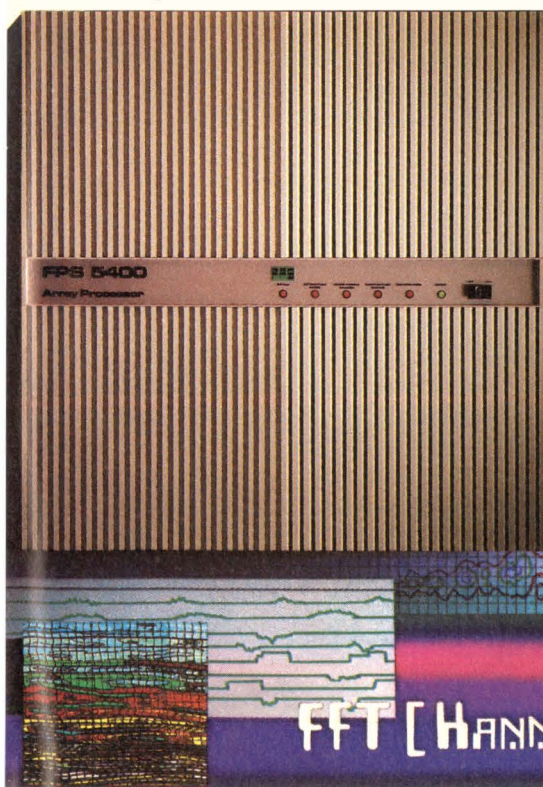
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EDITOR'S COMMENT

The articles in this issue reflect several subtle changes taking place in engineering and design. During the last few months, the editors of *Digital Design* have observed an increase in the number of production tools which support engineers. A great deal of this activity is due to the designing of new 16/32 and 32 bit microprocessors. Much of the trade press has been actively reporting on the new announcements; however, we hope to examine some of the implications, both for the designers of workstations and the designers using them.

In working with manufacturers across the country, several issues relating to the design process were apparent. One group of topics dealt with the enhancement of drafting efficiency, storage and transmission, editing, design capture, and so on. Many of these aspects are quantifiable or easily demonstrated. There is, however, a second group of issues about the changing nature of the design process itself.

Some engineers believe that while computers will assist the engineer, the activity will remain organized much as it is to date with drafting, analysis, design, and the interface to manufacture as separate disciplines within the overall work environment. Others perceive a coalescence of both organizational job descriptions and actual job skills. That is, just as the computer-based workstation will provide more functional tools to the engineer, the individual who will operate the system will begin to take on a multi-disciplinary role.

Given the increasing sophistication of today's workstations this is an obvious oversimplification. Some of today's systems not only require months to learn to use efficiently, but may also be best used by someone with experience in a specific field—either drafting, engineering, or design.

There are several implications here, such as a greater need to train engineers in multiple disciplines, or to lose jobs through automation. Displacement in the marketplace seems almost implausible given the demand for engineers, but the publishing industry has certain similar analogies where electronics has both increased the demand for technical editors and displaced other workers in the printing process.

In this analogy it is the operators of systems which use older technology that are initially made redundant. As the integration of electronics gradually becomes more complex, the nature of organizations changes more dramatically. It is not necessary to ask whether the nature of design will change but when and in what form the changes will occur.

Many users of engineering workstations raise questions about possible homogenization or uniformity brought about through the use of popular software packages. Finite Element Modeling or analysis is a pertinent example where packages such as Nastran or Ansys have become de facto standards. While the code for these packages is complex and the ways in which they are applied are sophisticated, their increasingly wide use makes a good case for a uniform design approach. The general response to them is positive (because they represent excellent pro-



E. L. Busick, President, Spectragraphics Corp. and Jerry Borrell

ducts and promote sound design).

On the negative side, these tools could promote uniformity, or worse, limit the creative process. It may be fair to say that the powerful software packages being developed for today's systems will make the work of the less competent designer/engineer better, and provide possible detraction from the more competent designers.

To date, the emphasis on fifth-generation computers in the US has been primarily on how to bring companies together and coordinate resources, and in planning an agenda. Over three years ago in Tokyo, Chairman Moto-Oka of the Japanese Fifth Generation Project outlined the four goals of their decade-long project. One of these is to develop "intelligent" CAD tools. Combined with another goal: the compilation of "knowledge databases," the project was to bring about the third stage of fifth generation computer architectures.

Can it be that within the next two years engineers in the Japanese project will be working in research centers with intelligent CAD systems which will not only span applications such as electrical and mechanical design, but whose programming will allow their users to work with a new approach to design? One of the key concepts in combining CAD with a knowledge data base is in providing a system with the ability to query the designer not only on what the intent of the work is, but about possible design solutions given certain performance criteria.

Our December issue reflects the vigorous activity in the US market for systems, devices and design tools that may change the way designers work. The effort that we must make over the next year, then, is not only to continually improve the quality of our reportage, but to look critically towards the future. We have developed a series for 1984, the Advanced Technology Series, that addresses future trends and their implications.

Jerry Borrell
Editor-in-Chief

MULTIBUS* PLUS

PERFORMANCE

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Monolithic Systems Corporation has always been synonymous with Multibus technology. In fact, MSC has the distinction of having designed the first patented single board computer. Other firsts include: the first use of 64K RAM elements, on-board EPROMS, floppy disk controllers, APU's, user selectable addressing and multimaster CPU configurations. These board level accomplishments have benefited OEM's for over 12 years and have culminated into a powerful line of systems, the MSC 8800 series.

As the leading innovator in Multibus products, Monolithic Systems offers a family of systems intended to do things never done before. Systems to assist and create test programs for the scientific and industrial markets, to be multi-user and multi-tasking, to be expandable, rugged and reliable beyond anyone's expectations. Available with operating systems by Digital Research, the MSC 8800 series and board level products will be prominent factors in Multibus applications now and in the future.

For more information about Monolithic Systems Corporation and its Multibus product line call Toll Free 1-800-525-7661.



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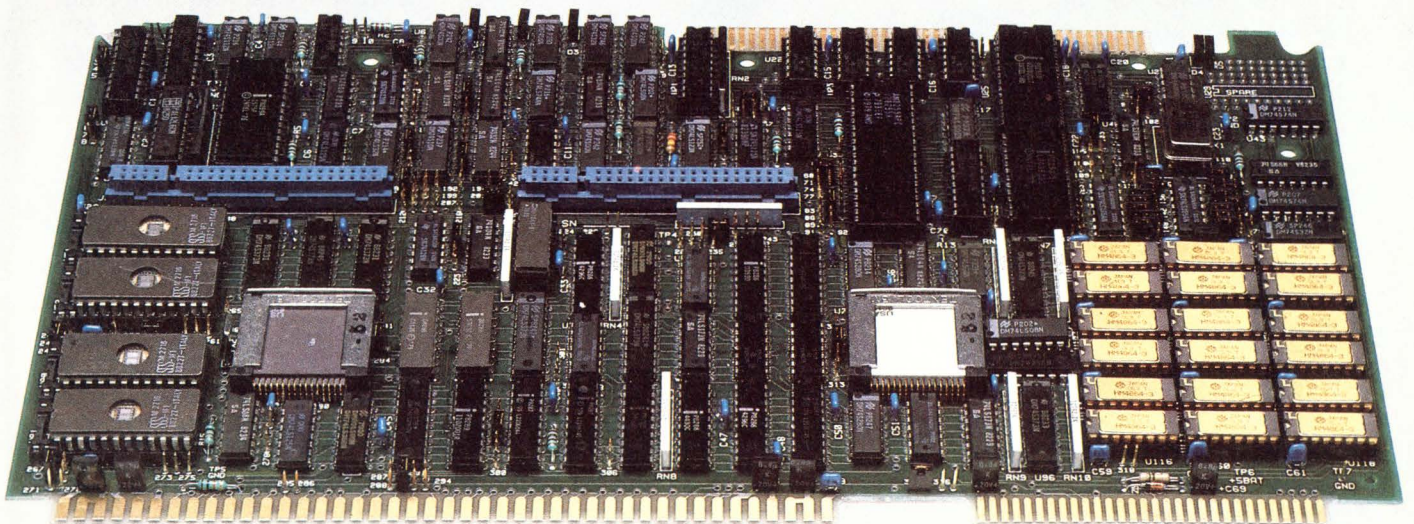
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16 BIT PROCESSING

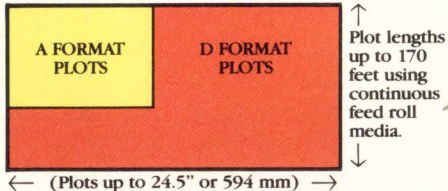
- iAPX 186 8 Mhz. CPU
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- UP TO 128 KBYTES EPROM
- FOUR 16 BIT COUNTER TIMERS
- TWO iSBX CONNECTORS
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*The most flexible "D" format
8-pen plotter ever.*

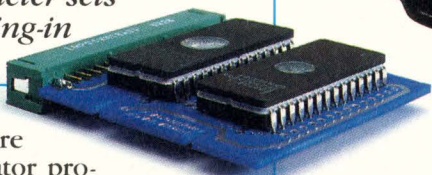


Now you can create virtually any size plots you want up to 24.5" wide, including ANSI sizes A-D and ISO sizes A4-A1, on cut sheet or roll media. Use standard bond paper, glossy bond, vellum, clear film or mylar.

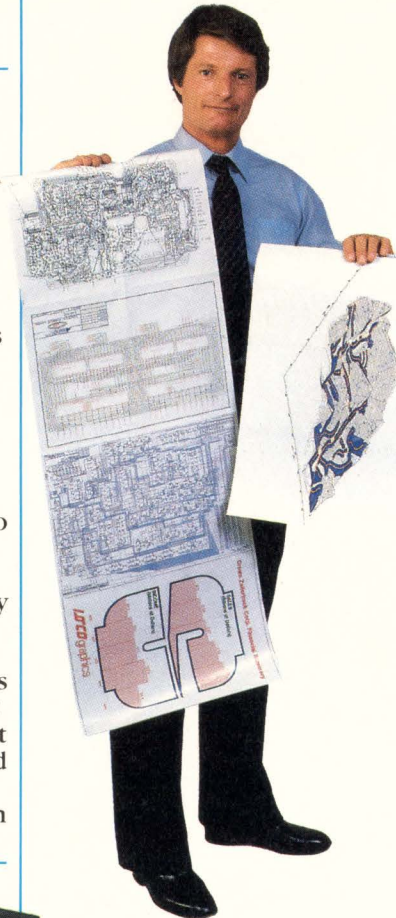
Run dozens of entirely different plots automatically thanks to a built-in microcomputer that can be pre-programmed to plot on roll media up to 170 feet. Then quickly switch to cut sheet plotting – great for your pre-printed forms. The ZETA 822 is the only plotter that can do both.

Best of all, we've got line quality and throughput at a price that makes us the cost-effective choice for just about anybody's plotter applications. You'll get vector independent speed of 25 ips. And 2 g acceleration insures the plotter reaches top speed fast. With resolution of one-one thousandth's of an inch.

*Change character sets
just by plugging-in
a ROM chip.*

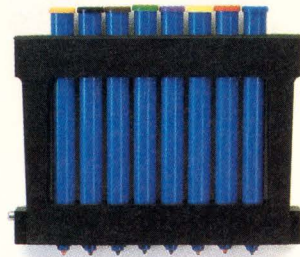


Our firmware character generator produces typeset quality lettering similar to the popular Helvetica font with



user-controlled proportional spacing. Now you can add special character symbol sets for both engineering and architecture simply by plugging in a new ROM chip.

Eight color, carriage-mounted pens eliminate time-consuming pen changes.



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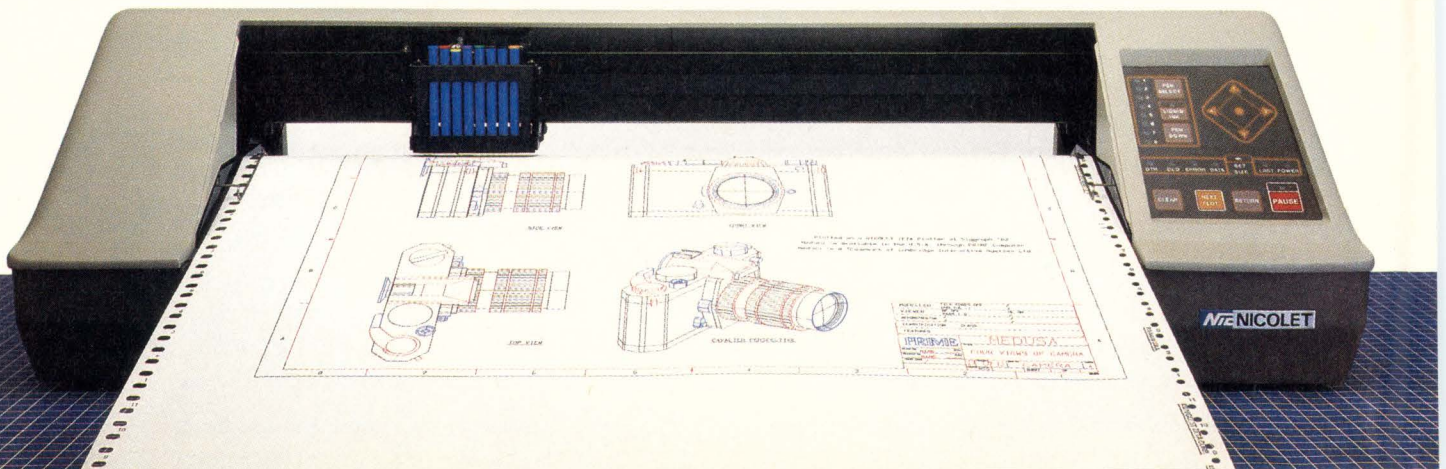
You have total user control over such variables as speed, pen pressure, acceleration and pen up/down delay times. Touch controls automatically adjust the ZETA 822 for perfect liquid ink plots.

Naturally, we support most computer protocols. And you can use the ZETA 822 on-line, off-line or remotely via RS 232C or IEEE 488 interfaces.

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Comprehensive Graphics Capabilities: 1024 x 1024 workspace; 1024 x 768 displayable; 4096 x 4096 virtual addressing for extended Tektronix 4014 compatibility. High-level graphics primitives, including polygon fill. Bit-mapped 19" screen. Three dot-addressable bit planes. Separate alphanumeric plane. Hardware pan and zoom. Expanded peripheral support. Simple menu set-up. Host programmable function keys.

Fast Response: 2.5 million pixels/sec. direct screen memory access port.

Industry Standard Protocol: ANSI X3.64/VT100 command protocol.

Compatibility: VT100, TEK 4010/4014/4014-1 and enhanced Intecolor 8001R.

Raster Color: Palette of 4,096 colors, 8 concurrently displayable.

Advanced Processor Design: Three graphics processors (7220D-1); separate alphanumeric processor; plus terminal processor (Z80) and keyboard processor.

*100-piece OEM price and single-unit introductory price through 12-31-83; includes color monitor, graphics display processor and keyboard. Trackball is optional at \$330. U.S. Domestic prices.

From the same company that pioneered the world's first micro-processor-based color terminal (Intecolor 8000) way back in 1973. And the same company that continually leads the color graphics industry with new product innovations. NOW, a bold, new addition to the fastest growing area of the industry: *Intecolor VHR-19 high resolution graphics workstation.*

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NEWS UPDATE

EEPROM Joint Effort

INMOS Corporation and General Instrument announce a joint effort involving 64K EEPROM technology. Specifically, INMOS is naming General Instrument as second source for its IMS3630 8K x 8 EEPROM, a high performance +5V only non-volatile memory device. The joint effort involves a complete technology transfer, including masks and processing information.

China Trade

Digital Sound Corporation, developer and manufacturer of the DSC-200 audio digitizing peripheral unit, has received an order for the system from the Institute of Acoustics in the People's Republic of China. This underscores a current softening in the United States position regarding trade of high technology equipment with the People's Republic of China. The DSC-200 provides a complete interface between conventional audio equipment and computer disk storage and has broad applications in speech research, music synthesis and speech product development.

Multibus II Specs Gain Support

Intel Corp. announced that 68 companies support specifications for a new microprocessor data bus — the path over which information moves from the central processor to memory and peripheral devices in a microprocessor-based system. Called Multibus® II, the new architecture meets the needs of advanced 8-, 16- and 32-bit high-performance, microprocessor-based systems. The Multibus Manufacturers Groups (MMG) was recently formed to preview the new bus specifications.

Designs For Porsche

Intergraph Corporation will supply Porsche AG, a West German car maker, with interactive computer graphics systems for research and development. The company expects to use the system for car body and engine design, as well as other general mechanical and electrical applications. The Intergraph computer-aided engineering system purchased by Porsche includes a VAX-11/780-based Intergraph computer

equipped with the company's Graphics Processor and three of its latest dual-screen engineering workstations.

GTE Telenet Approval

Bridge Communications, Inc., received certification from GTE Telenet Communications Corporation to operate its Ethernet local area network gateway products over GTE Telenet's public and private data networks. The certification will allow Bridge's Gateway Server/1 (GS/1) units to connect Xerox Network System (XNS) Ethernet networks to host computers or other XNS Ethernets via GTE Telenet's packet-switching network, using the CCITT X.25 protocol for the LAN-to-Telenet interface.

One-Stop Design Center

Control Data Corporation and NCR Corporation's Microelectronics Division announced the opening of an electronic computer-aided design (ECAD) services center that is believed to be the first of its kind in the nation. Control Data, NCR, and Array Technology, NCR's Bay area sales representative and design group, have combined their expertise in systems, semiconductors and computer-aided design to offer a combination of consulting, training and computing resources at the center. The center is designed to assist integrated circuit manufacturers and systems houses apply state-of-the-art ECAD technology from initial design concept to the production stage.

First Flexible Disk Cartridge

A major breakthrough in magnetic media storage technology has brought Verbatim Corporation and Iomega Corporation together in a licensing agreement to produce the computer industry's first flexible disk cartridge. Under the terms of the agreement, Verbatim, manufacturer of magnetic media products, will supply the media for Iomega's flexible disk cartridge. Iomega, based in Ogden, Utah, is the first disk drive manufacturer to successfully employ Bernoulli technology in the development of magnetic media storage products.

The new cartridges are considered

significant because they are the first magnetic media storage products to combine flexible media with the density and access speed characteristics of more costly rigid media. As a result, the cartridges are expected to sell for half to one-third less than other commercially available removable cartridges using rigid media.

Bernoulli technology dates back to the 18th century when Swiss mathematician Daniel Bernoulli developed his theory of fluid mechanics. Bernoulli's work has played a major role in aircraft wing design and, most recently, in flexible disk cartridge technology.

Transmission Security

A new data encryptor designed to prevent unauthorized access to computer information during transmission has been added by Racal-Milgo to its family of link encryption devices. The new product, Datacryptor III, secures data over point-to-point wideband circuits at data rates up to 112 Kbits per second. It operates synchronously on full duplex, leased line facilities and is equipped with both V.35 and RS 232 interfaces wired in parallel. Either interface may be used depending upon network data rate requirements, V.35 for higher rates and RS 232 for lower ones. No configuring or strapping is required.

G.E. Sells Printer Dept.

General Electric Company and the Genicom Corporation announced a definitive agreement whereby Genicom will purchase General Electric's Data Communication Products Business Department, including all operations in Waynesboro, Virginia and Reynosa, Mexico.

Genicom, a new company, which was formed to operate this business in the future, will purchase the Data Communication Products Business Department assets from General Electric. The Waynesboro plant manufactures and markets teleprinters, line printers and serial printers, which are used in a wide range of data processing and telecommunications applications and electromechanical relays, which are sold primarily to the aerospace/defense industry.

Put powerful instrument control at your fingertips. IEEE-488

The new Fluke 1722A Instrument Controller combines the computational ability and interfacing flexibility you need with the rugged packaging and easy-to-use human interface your factory demands. All at a new, low price. Now you can integrate your next factory test, process control or OEM system faster and put your people to work sooner.

The power of the 1722A is a 16-

bit single-board computer with 136K bytes of main memory. Its 12 MHz speed puts it in the same class as many minicomputers. Four programming languages are available to simplify programming, including Interpreted and Compiled BASIC, FORTRAN and Assembly. Each includes special adaptations for controlling IEEE-488-compatible programmable instrumentation. And if you

already own a 1720A Instrument Controller, you can run existing software on the 1722A—without modification.

The modular mainframe easily mounts in a standard 19 inch rack and allows you to configure the interfaces and memory to your exact needs. The IEEE-488 (1980) and RS-232-C interfaces can be expanded with an optional IEEE-488 and RS-232-C interface card, parallel interface card or dual serial interface card. Onboard memory is expandable to 2.6M bytes with RAM cards or 1.4M bytes with bubble memory.

The 1722A's touch-sensitive display dramatically simplifies system operation. Once programmed, your system can be operated entirely from the CRT. The 1722A displays only the pertinent options, allowing you to structure the user's response to a system. This helps reduce mistakes and increase throughput.

The 1722A is priced at \$7450 (U.S. list), including BASIC Interpreter, documentation and a limited one-year factory warranty. So get in touch with your local Fluke Sales Engineer or Representative. Or call us toll free at 800-426-0361 for more information.

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Use the new graphics capability of our 16-line, 80-character touch-sensitive display to create more effective operator prompts.

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Computer Controlled Systems Include Robotic Vehicles

Veeco Instruments Inc. announced the formation of a previously announced joint venture (August 22, 1983) to design and manufacture automated systems for companies that fabricate semiconductor wafers. Automated wafer fabrication will extend the Veeco product line of semiconductor processing equipment. The company plans to develop a state-of-the-art computer controlled system that will be housed in clean rooms with robotic vehicles controlling all movement involved in the operation.

Allen E. Busching, President, said that the elimination of workers from the actual fabrication area will improve productivity substantially. "There are more than 200 semiconductor wafer fabrication factories worldwide and their yields on new VLSI products generally are below 50% due primarily to the contamination of the sensitive silicon wafers that results from workers

involvement in the facility."

The company plans to open a customer demonstration laboratory in Dallas during 1984, and expects to begin delivery of systems in 1985.

Full CAD/CAM for ASEA

ASEA, a world industrial group, has turned to Racal-Redac to help complete a major computerized manufacturing program at its Electronics Division in Vasteras, Sweden. ASEA currently has four Redac Maxi systems for PCB design, as well as a DSM 6 host computer. Two newer Maxi systems are expected to be linked this year to the DSM 6 VAX 11/780 computer, which will be at the hub of the new computerized production system.

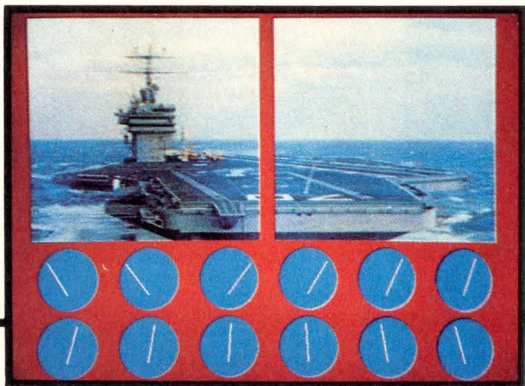
Timeplex Contract

Timeplex, Inc. signed an agreement with GTE to supply data multiplexers to their Business Communication Sys-

tems division. Three lines of Timeplex products offered by GTE are statistical multiplexers, data concentrators for smaller installations, and standalone modems that operate synchronously.

Quantum Pacts

Quantum Corporation signed three new agreements for the distribution and purchase of the company's 8- and 5-1/4-inch Winchester disk drives. Future Electronics, Montreal, Quebec, Canada, signed a distribution agreement for Quantum's Q2000 and Q2080 8-inch disk drives. A two-year contract, valued at \$4.5 million, was signed by Pixel Computer Inc., Wilmington, Mass., for Quantum's Q2000 and Q2080 8-inch drives and Q500 5-1/4-inch products. A second OEM agreement was signed by Telesis Systems Corporation of Chelmsford, Mass. The \$3 million contract calls for Quantum's Q2000, Q2080 and Q500 disk drives.



COMPOSITE PICTURE: HI-RES GRAPHICS and NTSC VIDEO

The GraphOver 9500 is a high-speed computer graphics generator that gen/locks to any NTSC video input and overlays its high resolution color graphics. This creates a composite picture in both RGB and NTSC. For more information, call us at: 617-272-8844



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ATTENTION LA36 USERS

The DS120 Terminal Controller makes your LA36 perform like a DECwriter® III.

The Datasouth DS120 gives your DECwriter® II the high speed printing and versatile performance features of the DECwriter® III at only a fraction of the cost. The DS120 is a plug compatible replacement for your LA36 logic board which can be installed in minutes. Standard features include:

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- Page Length Selection
- 110-4800 baud operation
- 1000 character print buffer
- X-on, X-off protocol
- Self Test
- RS232 interface
- 20 mA Current Loop interface
- Top of Form
- Adjustable Margins
- Double wide characters
- Parity selection
- Optional APL character set

Over 9,000 DS120 units are now being used by customers ranging from the Fortune 500 to personal computing enthusiasts. In numerous installations, entire networks of terminals have been upgraded to take advantage of today's higher speed data communications services. LSI microprocessor electronics and strict quality control ensure dependable performance for years to come. When service is required, we will respond promptly and effectively. Best of all, we can deliver immediately through our nationwide network of distributors. Just give us a call for all the details.

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Digital Design ■ December 1983

Four Answers To Your S-100, Multi-User Problems.

Intercontinental Micro Systems makes everything you need for S-100 bus multi-user systems, networks or single user systems.

At a price that won't break your budget.

Quite simply, our single board computers, slaves, 256K memories and personality boards let you build a system *now*, not later. The hardware works, the software works.

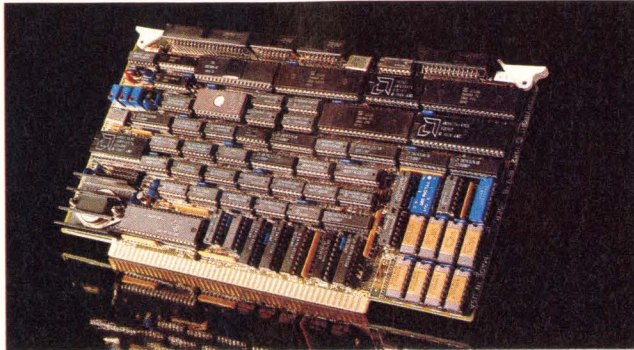
and the prices are what you'd expect from a company that uses the most advanced design, software and production techniques to keep costs down.

What you won't expect is the almost awesome sophistication of Intercontinental Micro Systems' products.

So stop messing around with multiple sour-

ing, hardware integration problems and software nightmares. Come to Intercontinental Micro and get it all — price, performance and delivery.

Read the specs, then call, write or circle the bingo number below. We'd be glad to send more information and help solve your S-100, multi-user system problems.

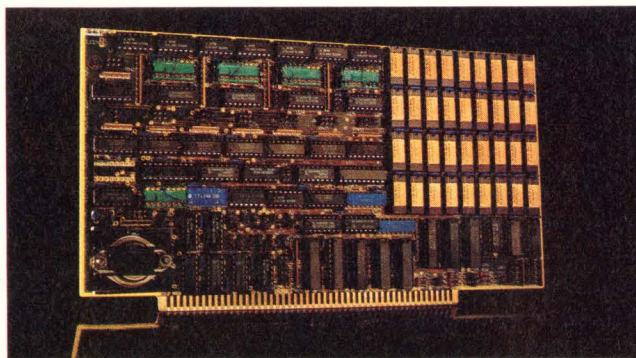
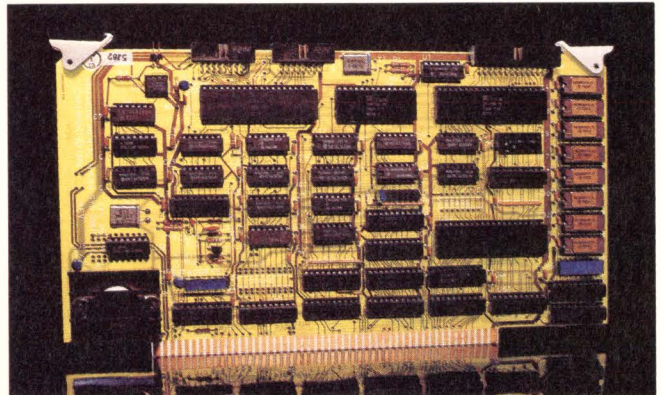


1 CPZ-48000 SINGLE BOARD COMPUTER.

- IEEE 696.1/D2 S-100 compliance. Z80A™ 4MHz Operation.
- Floppy disk controller (FDC). Single or double sided. Single or double density. 8" or 5 1/4".
- Two synchronous or asynchronous serial I/O channels (SIO). Two parallel I/O channels (PIO).
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- IBM Bisync, HDLC, SDLC and other protocols. CP/M™, MP/M™ and TurboDOS™ operating systems available. Turbo-Disk™ implementation included.

2 CPX-MX SLAVES.

- IEEE 696.1/D2 S-100 compliance. Compatible with CPZ-48000 SBCP; any Z-80A based CPU with extended address capability or 16 bit based CPUs complying with IEEE 696.1/D2 bus specification.
- Z-80B™ 6MHz (CPS-6X) or Z80A4MHz (CPS-4X) operation. Two synchronous (CPS-MS) or asynchronous (CPS-MA) serial I/O ports. TurboDOS™ & CP/NET™ compatible. Master confiscation of slave memory for diagnostic purposes.
- Two parallel I/O ports: eight data bits + 2 handshake lines per port. 64 Kbytes of onboard dynamic RAM.
- Master/slave memory-to-memory transfers under DMA control @ 571 Kbyte/sec transfer rate when used with CPZ-48000 SBCP. Software selectable baud rates. Usable as an intelligent I/O processor in single user system.



3 256KMB-100 256K MEMORY.

- IEEE S-100 bus, spec 696.1/D2 compliance. The 256KMB-100 is compatible with most IEEE S-100 board products now on the market.
- Linear addressable to 2 megabytes. 225 nano-second access time, maximum, 160 nano-seconds, typical.
- 295 nano-second read-write time, minimum. Bank selectable 16K increments. I/O port address bank selection.
- Configures for phantom deselection. Parity error detection, visual and/or interrupts. Bank selection compatible with CROMIX™, CP/M2.2™, MP/M™, Alpha Micro, and other major systems.

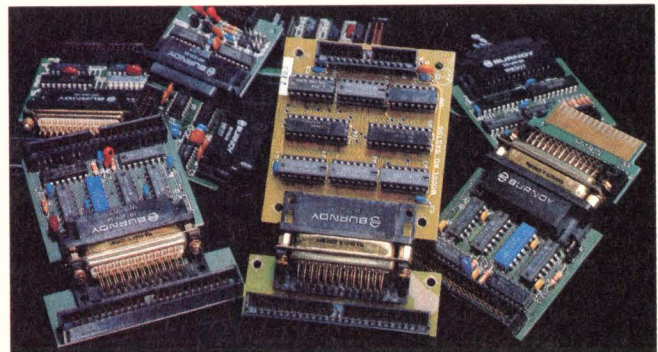
4 PERSONALITY BOARDS.

- Centronics printer. 8 inch floppy disk. 5 1/4 inch floppy disk. RS232 serial communications. Synchronous/asynchronous modem. Priam smart/smart E hard disk.
- Long distance serial communication (2000 ft @ 9600 baud).
- Shugart Associates Systems Interface (SASI). Clock/calendar. Konan David, Jr.™ hard disk. Archive tape drive.

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WASHINGTON REPORT



by Anne A. Armstrong

The debates over policy which seem to drag on endlessly in Washington usually have little effect on the bottom line for business, but a campaign now shaping up over "industrial policy" could significantly change the financial climate and the tax situation for many computer manufacturers.

Begun as a call for increased growth and support of high-tech industries by a group dubbed the "Atari Democrats," the idea of a "new industrial policy" has caught the imagination of a widening group that now includes Republicans and even the executive council of the AFL-CIO.

Like most catch phrases, the notion of a new industrial policy means different things to different people. In common, however, is the belief that it is in the interest of the nation's economy for government to support the growth of high-technology by creating a favorable business climate. One way to do that is to provide tax incentives.

The 1981 Economic Recovery Act was a big help to traditional industries such as steel and oil, but did very little for high technology companies because the short life of most high tech equipment precludes taking advantage of the ERA's long-term equipment depreciation. A whole host of legislative solutions is currently under consideration on Capital Hill.

Lobbying efforts have increased and a new group, the Ad Hoc Electronics Tax Group, has been formed to concentrate pressure for new legislation. Directing the group is Robert Kirkwood from Hewlett-Packard's governmental affairs office. Another entry is the Computer and Business Equipment Manufacturer's Association (CBEMA), which recently adopted a position on industrial policy and has begun to lobby the Hill for support.

Not everyone sees tax cuts as a solution. Rep. Richard A. Gephardt, (D-Mo.), suggests an Economic Cooperation Council, which would be a forum for discussion about economic

issues and a place where information could be exchanged. He is not in favor of continued tax changes.

"We are destroying our tax system. We have made the tax code our direct spending program. The 1981 tax bill made the significant decision to allocate capital to older industries to the detriment of other industries. We no longer stop to see if it works, we just do a new tax bill every year. Two-thirds of the bills introduced each session include tax preferences for someone," Gephardt told executives at a recent CBEMA meeting on industrial policy.

Also cautious about government involvement and aid to high technology companies is Rep. Ed Zschau, (R-Calif.), who founded a high tech firm — System Industries — before he was elected to Congress from the district which includes Silicon Valley. "The proper role of government is to create an environment in which risk taking and innovation flourish," he said. Japanese style agencies — such as MITI — which provide centralized planning and targeting for industry would probably not work in this country, Zschau believes. "Government is not known here to be the servant of business."

"The legislative agenda should focus on making sure that bottlenecks for business are removed. The four main points of industrial policy should include 1) a commitment to basic research 2) incentives for investors, 3) educational opportunities to provide an adequate supply of trained engineers, and 4) expanding market opportunities brought about by reducing trade barriers," Zschau said.

Since no one bill has emerged as a consensus solution to the industrial policy problem, Congress is faced with more than 100 bills purporting to help high technology companies in one fashion or another. Industry efforts are concentrated on tax relief, but most observers see a long battle ahead. CBEMA's president Vico Henriques says, "Industrial policy promises to be a key point in the debates surrounding the coming 1984 elections."

ARPANET Split Into Two Networks

The Department of Defense's pioneering packet-switching network, ARPANET, has been divided into two systems to insure greater security for military information. Originally designed as an experiment into advanced networking techniques and as a way for researchers working for the government to communicate and trade information, ARPANET has evolved into an operational electronic mail and messaging system used by more than 10,000 people.

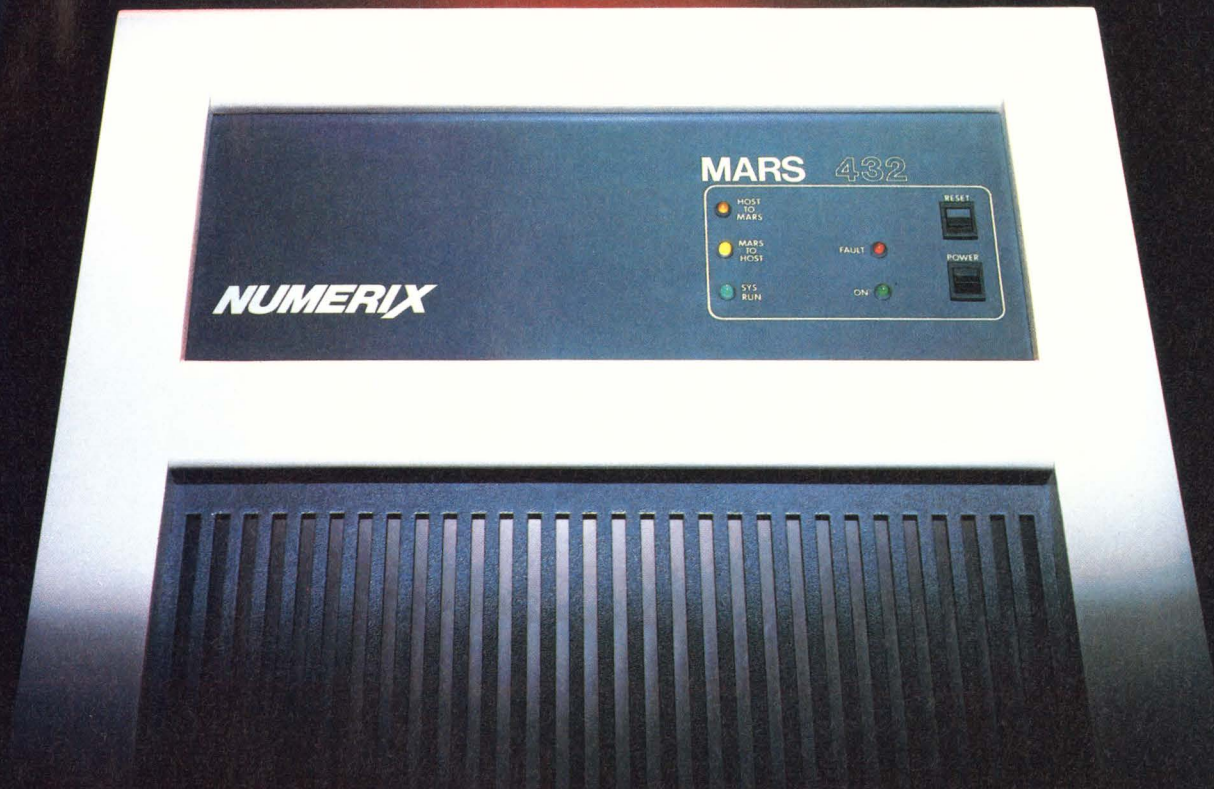
The civilian system will continue to be called ARPANET and will remain the link between universities and laboratories doing government research and the government. MILNET, the new defense system, will be used for military communications only and will be part of what DOD expects by 1985 to be a secure, top-secret communications system. There will be gateways or mail bridges between the two networks, but the systems are designed to be completely independent.

FCC Delays Access Charges

In a move that surprised many and angered AT&T, the FCC delayed implementation of the access charge plan and AT&T's related long-distance rate reduction proposal. The Commission says it needs a 3-month delay (until April 3, 1984) in order to adequately review voluminous new tariffs filed earlier this month by local phone companies for their planned new system of payments by users and intercity carriers for access to the long-distance network. AT&T's plan was to reduce long-distance rates \$1.75 billion overall. Both plans were tentatively scheduled to take effect January 1, 1984, the same date as AT&T's divestiture.

For the equipment industry, a key change in a bill passed by the House Telecommunications Subcommittee last month is the Bliley (R-VA) amendment that called on the FCC to review access charges for existing non-profit users of Centrex service.

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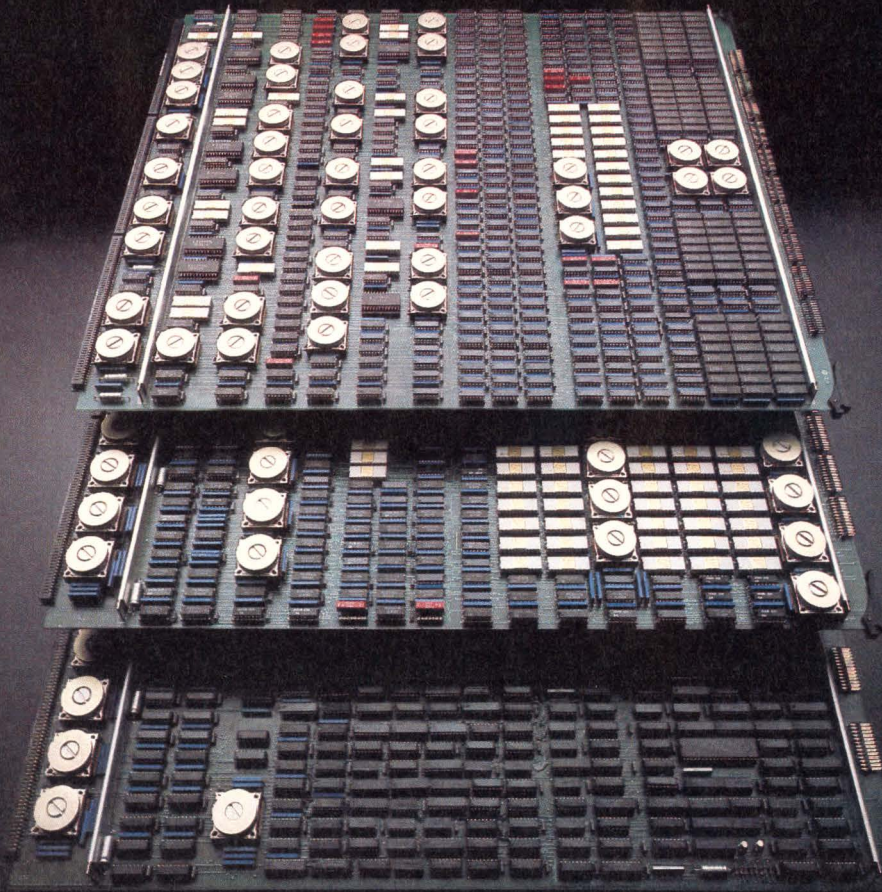
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Expandable Supercomputer Uses Semi-Custom ECL Gate Arrays

Available in configurations capable of processing from 4 to 40 million instructions per second, the ELXSI 6400 is a multi-purpose system that can be used in time-sharing, real-time or batch environments from large number crunching tasks to high-volume transaction processing.

The system consists of a modular multiprocessor computer, a proprietary operating system called EMBOS (Elxsi message-based operating system), peripherals configured to customer specifications and data management tools. Each basic system includes a Gigabus high-speed central bus, CPU units, memory system, input/output processors (IOPs) and service processor. A variety of programming languages are available, including Pascal, C, Cobol-74 and Fortran-77.

In the past the limiting factor in multiple computer architectures has been the central system bus. Elxsi's solution is to provide a 64-bit wide synchronous bus with an effective bandwidth of 320 Mbytes/sec. Taking into account all bus overheads for memory access, usable data rates range from 160 to 213 Mbytes/sec. The Gigabus allows for the attachment of up to 32 identical modules, which can be configured as the user requires.

At the heart of the 6400's I/O subsystem are dedicated I/O Processors (IOPs), up to four of which can be configured in a single system. All physical I/O is handled by the IOP, freeing the CPU's for computational tasks rather than array processing. Key performance features of the IOP include a 50ns processor cycle

time, microcoded control of all I/O and virtual-to-physical memory address translation for data transfers between memory and devices. Each IOP can have two sub-busses, each of which can operate at 8Mbytes/sec, giving a total bandwidth of 16M Bytes/sec per IOP. Each sub-bus can support up to 16 device controllers which may be dual-ported across two sub-busses belonging to the same or different IOPs.

The controller types that are currently supported include a disk controller, a combined tape/printer controller, a communications controller and a DEC DR11-compatible interface. An IOP can function with any mix of controller types. All con-

Above: The ELXSI 6400 multi-purpose system.

trollers are self-identifying, allowing dynamic configuration of the I/O subsystem.

The operating system (written almost entirely in Pascal) is implemented as a collection of indepen-

dent processes which communicate with each other and with user processes via an inner kernel that provides a microcoded message system. The interactive interface to EMBOS is a user-friendly command language

interpreter, or shell. The system 6400, typically priced from \$600,000 to \$4,000,000, is available now with a 60 to 90 day delivery time.

Elxsi Corp.

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Data Storage Breakthrough

By offering a combination of very high capacity and media removability at a significantly lower cost than current random access storage devices, the pending generation of optical disk drives will be well suited for a wide range of traditional computer applications as well as new market opportunities. In addition, the optical disk drive's low power consumption and small footprint will be advantageous in the large office automation market projected to mature in the second half of the 1980s.

Based on laser rather than magnetic technology, optical disk drives are significant primarily because they will help satisfy the world's exploding demand for data storage capacity. With early products expected to offer 1,000 Mbytes on a 12" disk, they will offer a solution to the challenge of satisfying tomorrow's data storage requirements in local area networks, small business computers, minicomputers, mainframes and imaginal storage applications.

Imaginal storage, or the ability to store the representations of documents or graphics, is an area not adequately addressed by current storage products, but is an application for which high-capacity optical disk drives are well-suited.

Despite offering many advantages, optical disk drives will not render floppy or Winchester disk drives obsolete. Magnetic technology-based products will remain the correct choice for many system applications; the two technologies will complement each other within the same system and can co-exist for at least a decade.

Shugart Corporation became the first American OEM company to announce a laser-based optical disk drive with the introduction of the Optimem 1000, a device capable of

storing one gigabyte of information (one billion characters or about 400,000 typed pages of text) on one side of a removable 12" disk.

Using non-erasable laser technology, the Optimem 1000 provides up to 10 times more on-line storage capacity than comparably priced magnetic disk drives, greatly reducing the cost-per-byte for stored information.

Developed by Shugart's Optimem division, the new drive writes and reads information on the disk using non-erasable, laser technology (write once, read many times). Unlike magnetic recording technology, which uses a mechanical read/write head to record data, the Optimem product uses a laser beam to perform this function. Information is recorded and played back on a removable 12" disk which is protected during operator handling, transport and storage by a hard shell cartridge. The cartridge also accommodates labeling information and incorporates write protect and operator interlock features. The Optimem media is pregrooved for servo-tracking and preformatted with sector address information.

The Optimem 1001 cartridge contains a single-sided optical disk. This disk features a sandwich construction consisting of two 1.2mm-thick PMMA (polymethylmethacrylate)

layers permanently bonded together with the recording layer on the inside surfaces. The 1.2mm of PMMA functions as protection for the disk as well as serving as a substrate material. The Optimem 1002 cartridge contains a double-sided disk; the second surface is accessed by flipping the cartridge over.

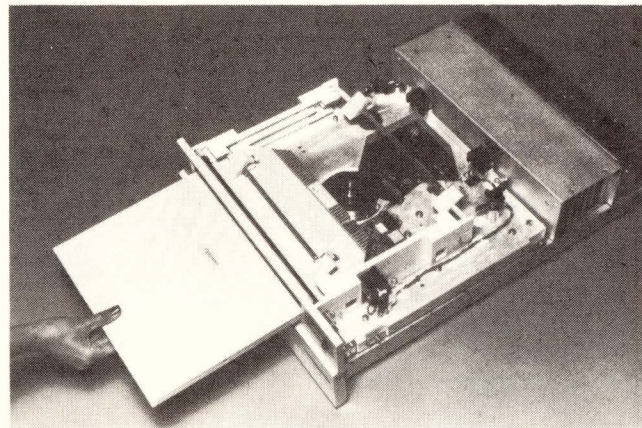
System integration is simplified through the industry standard controller-to-host Small Computer System Interface (SCSI). Each SCSI controller can operate up to eight peripheral devices.

Key specifications of the new Optimem 1000 include a five megabit-per-second transfer rate and an average access time of 100 milliseconds. The Optimem drive is only 7" high, 19" wide, and 24" deep. It requires less than 230 watts to operate, greatly reducing power and cooling requirements. Built-in microprocessor-controlled electronics and modular design simplify field maintenance and repair.

The Optimem 1000 will be offered for \$6,000 in quantities of 250, not including the controller. Shipments will begin in the first quarter of 1984, with volume production scheduled for the third quarter.

Shugart Corporation.

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Cartridge being inserted into the Optimem 1000.

Market Expands For Unenhanced IBM PC Look-Alike

Most manufacturers of compatible products have put new technology and techniques to work to make products with greatly enhanced features and capabilities from the equipment they are designed to replace. But on a different tack, Faraday Electronics (Palo Alto, CA) has made an effort *not* to enhance their IBM PC compatible single board computer. The response from a variety of OEMs seems to indicate that this "standard format" approach is a good one.

The reasoning behind producing as exact a replica of the IBM PC as possible is that, as software becomes more and more important, both in terms of cost and functional attractiveness of computers, machines that run the largest body of software exactly as it was intended will have the greatest advantage in the market. And they quote that "distributors report that over 50% of new software programs are now written for the IBM PC format."

Most companies that have produced "compatibles" of any kind will agree that as tricky as getting an enhanced product onto the market without infringing patents can be, making a look-alike respond to software as does the original can be even worse.

Faraday's FE 64 single board computer has the exact physical dimensions of the IBM PC, and the keyboard port, expansion slots and software are IBM compatible; it uses the 8088 processor like the IBM, as well. The only enhancements of the FE 64 are one parallel and two serial ports, memory expandability to 256K and some added diagnostics.

In their effort to maximize compatibility with the IBM PC, Faraday is positioned "at the trailing edge of low technology," as their VP of Marketing and Sales, Chuck DeVita, puts it. They feel this will be an advantage for their design, however, it can really go wherever IBM does.

One large difference, however, is

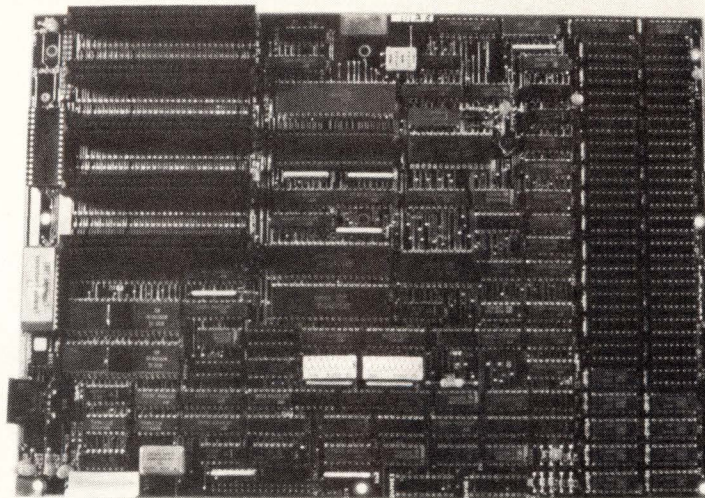


Figure 1: Faraday Electronics' FE 64 for single board computers.

cost; on an OEM high-volume contract basis, the FE 64 goes for only \$249; quantity one price is \$495. And unlike manufacturing start-ups, OEM quantities are available, since Faraday only designs and sells these boards. Manufacturing is done by Flextronics Singapore, who already have quantity production running for PC boards, such as the Apple.

Several firms have shown interest and will soon be introducing products integrating the FE 64. Faraday has targeted three main OEM markets: terminals, instrumentation and control and microcomputer companies.

The firm says it has turned down offers to buy large quantities of the board from companies who would use it in retail IBM PC look-alikes systems. With the current state of the personal computer market, Faraday understandably does not see a great future for their boards in products competing with the PC in retail stores.

Such wide OEM interest in this relatively low-technology product may point to a significant trend in the compatible market. For many applications, enhancements that exactly match specific demands will undoubtedly continue to drive a market for technically advanced compatibles. But standard format products such as the FE 64 do allow software portabil-

ity and thus, wide applications.

Another factor in using standard format products made with widely available components is the ability to meet quantity OEM demands early in the life of a company and its product. Quantity manufacturing is a perennial problem for start-ups, but by going to an established mass-producer and using standard parts, this can be solved.

The importance of standards, especially de facto standards, pops up repeatedly in this industry. IBM's PC is one de facto standard having a huge impact on all of the microcomputer industry, and Faraday's strategy is testimony to that.

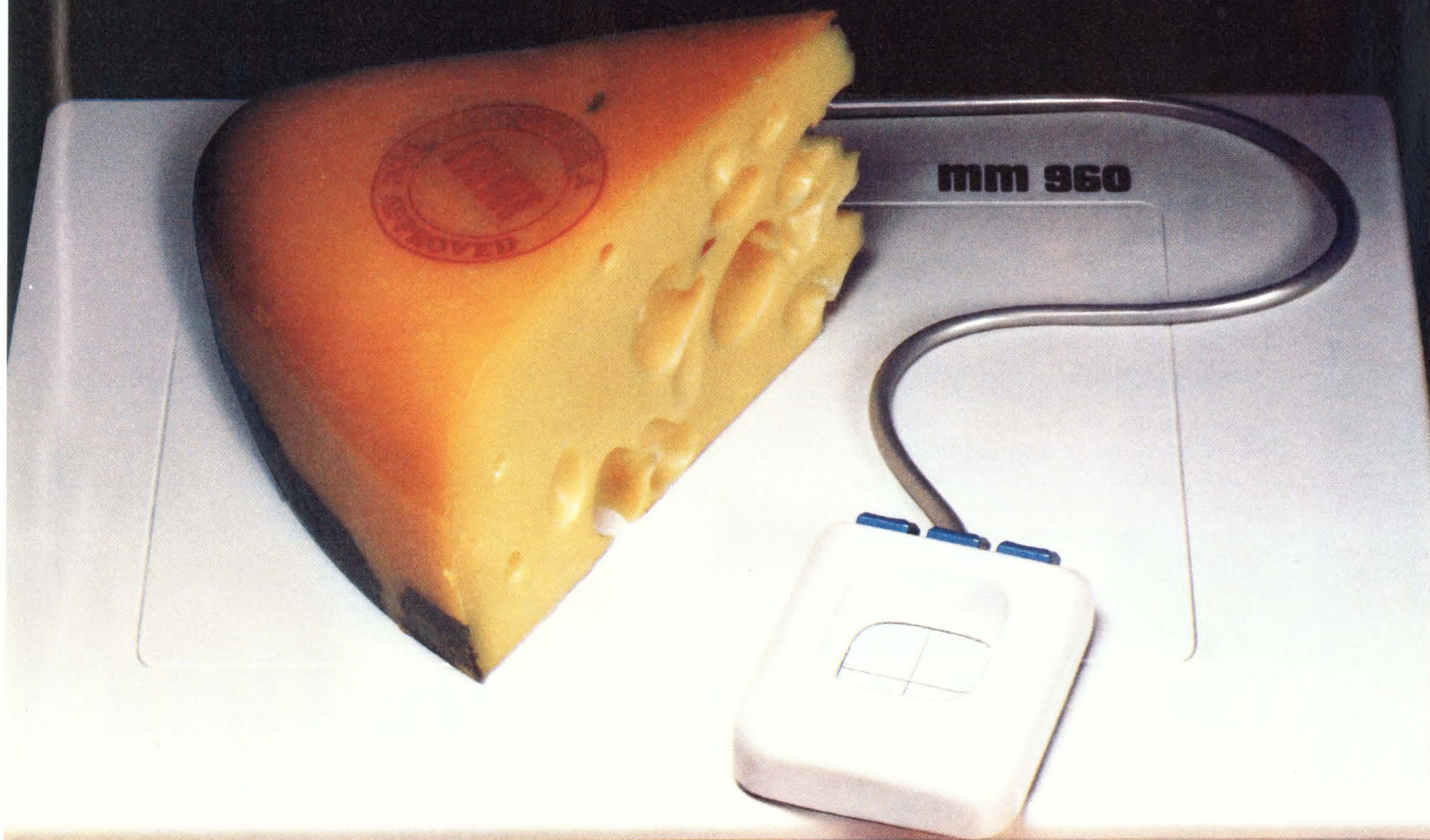
The question remains whether this will become an industry trend. Will other formats achieve the sort of popularity to give this sort of "standard format" compatible a market share to rival the innovative technologies of traditional enhanced compatibles?

If software really does begin to drive hardware, we may see other such new designs, driven by maximizing compatibility, especially software compatibility. But surely for many markets in which hardware costs are higher, compatible products will be technologically superior, innovation-driven products.

—Pingry

Write 231

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Filling the Market Gap With Graphics Extensions

Digital Research's (Pacific Grove, CA) Graphics Systems Extension (GSX) software extends an operating system to include graphics output and input functions. With GSX, graphics applications programs can be ported much the way CP/M provides portability for non-graphics applications.

Because GSX provides interfaces to graphics peripherals, it gives an operating system the ability to control a wide range of graphics devices, from CRTs with pointer devices to plotters and printers.

GSX provides a consistent graphics interface across all major operating systems—CP/M, PC-DOS and MS-DOS. GSX-compatible CP/M operating systems include the 8-bit CP/M-80, the 16-bit CP/M-86 and Concurrent CP/M-86—a 16-bit multi-tasking operating system.

GSX is made up of two major

components: the Graphics Device Operating System (GDOS) and the Graphics Input Output System (GIOS). GDOS is the device-independent portion of GSX and is based on the emerging ANSI standard for graphics software, called Virtual Device Interface (VDI). GDOS intercepts and services calls from graphics applications programs and loads the device driver (GIOS) modules to support different input/output devices. GIOS modules are the device-drivers which translate the GDOS interface calls into the unique protocols of graphics devices.

Applications Portability

Because it provides a consistent interface across a wide variety of graphics input and output devices, GSX greatly increases the portability of graphics applications. A graphics program written for GSX and a specific oper-

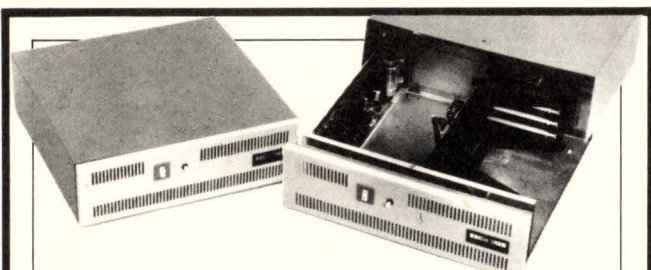
ating system can run on any computer equipped with GSX and that operating system, regardless of the particular hardware.

GSX is intended to fill the gap between a lack of standards and the boom in graphics applications. It frees software developers to concentrate on the quality and sophistication of graphics applications rather than on specific hardware configurations.

Availability

GSX is designed to serve a number of markets. OEMs can configure GSX to specific hardware combinations, selecting from Digital Research's library of device drivers. Independent software vendors will be able to include GSX with their graphics applications.

Write 241



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The BIT 3 Model 301 TABLE TOP MULTIBUS CABINET is an excellent choice to house your MULTIBUS card set. It permits the system integrator to offer an attractive low cost package suitable for table top or desk top use. A display monitor or additional cabinets can be placed on top of the chassis. It has color and styling compatible with the popular IBM PC. The chassis also makes an excellent companion to the BIT 3 Model 401 BI-DIRECTIONAL BUS TO BUS MULTIBUS TO PC ADAPTOR CARD SET.

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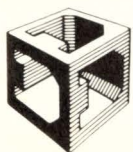
The single board VG-124 interfaces directly to a wide variety of monochrome/RGB cameras, video tape recorders, and video disks. It also provides a software selectable sync source as well as an enhanced DUAL-PHASE-LOCK LOOP.

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The One-Board Solution



Figure 1: The GraphOn GO-140 integrated alphanumeric/graphics terminal that uses a single-board design.

GraphOn Corporation (Santa Clara, CA) is now beginning volume shipments of the GO-140, an integrated alphanumeric/graphics computer terminal, which emulates DEC's VT-100 and the Tektronix 4010, 4012, and 4013. The company was founded in 1982 by former Synertek and United Technology principles who recognized marketing opportunities in the popularity of the VT-100 and the Tektronix 4010 series' broad range of business and scientific users.

A need existed for a sophisticated yet reasonably priced alphanumeric graphics terminal, while other manufacturers were producing terminals that required add-on graphics boards. GraphOn prices are comparable to a terminal plus an add-on feature. In targeting a market segment, GraphOn opted for the Tektronix user base with an added emphasis on the DEC VT-100 emulation segment. They were not looking for a captive market, but wanted to provide the VT-100 alphanumeric personality for non-graphics applications, and compatibility with the large base of existing applications software for both the VT-100 and the Tektronix terminals.

The GraphOn GO-140 uses a single controller board design, as opposed to most other alphanumeric/graphics terminals in its price range that have a graphics board retrofitted to an existing alphanumeric board. The single board design results in increased capabilities and a competitive price

for which systems integrators and OEMs can now offer customers a reliable graphics and alphanumeric terminal at about the same price or lower than a DEC VT-100.

Its alphanumeric features include 24 lines of 80 or 132 characters, selectable status line, 96 displayable ASCII characters, and bidirectional split screen smooth scrolling. Graphics features include 512 by 390 pixel bit-mapped display resolution for a 4:3 display aspect ratio. A 1:1 pixel aspect ratio for equivalent horizontal and vertical pixel spacing eliminates image distortion. Thus, when used with the DEC LA50, Epson FX-80, or Epson FX-100 printers, the GO-140 produces an exact hard copy, without distortion, of the graphics display. The GO-140 is compatible with PLOT 10, DISSPLA, TELL-A-

GRAF, DI3000/GRAFMAKER, and other graphics software packages.

The GO-100, the alphanumeric version of the GO-140, has character graphics capabilities and shares the same alphanumeric features as the GO-140, as well as the display, keyboard, communications and physical specifications. Plug-compatible with DEC's VT-100, the GO-100 includes advanced video and printer port options. Both models feature a detached VT-100 style keyboard with programmable function keys. The new terminals communicate via an RS-232 asynchronous ASCII half or full duplex host computer interface, and they are ANSI X3.64 compatible. Users can select 15 communication speeds from 50 baud to 19.2 baud. The single unit price for the GO-100 is \$1495, and \$1995 for the GO-140.

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Another DEC/TEK Personality

The CIG-267, a new color graphics plug-in card that combines DEC alphanumeric software commands and the Tektronix 4027A color graphics command structure, has been introduced by CIE Terminals, Inc. (Irvine, CA).

The CIG-267's dual DEC/TEK personality allows CAD, engineering and scientific designers to simultaneously use generic DEC alpha commands — in color, and the 4027A terminal's color graphics capabilities. The CIG-267 card was developed in

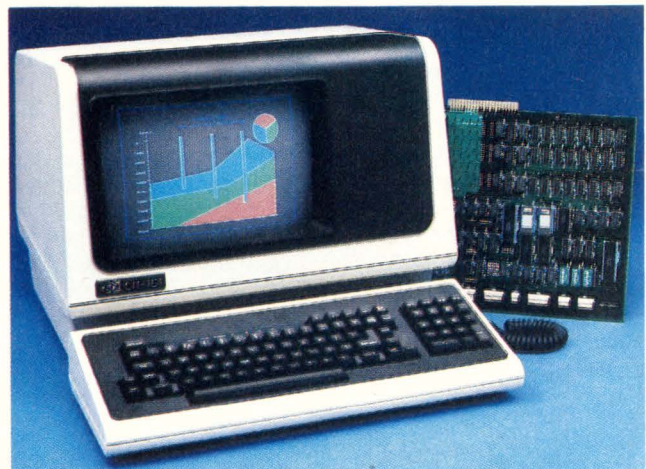


Figure 2: CIE Terminals' CIG-267 Color Graphics Card and terminal.

response to user surveys undertaken by CIE Terminals that show the 4027A's alpha mode accounts for less than 10% of the terminal's use.

The CIT-161 color terminal, hosting the CIG-267 card, provides designers with a 572 x 480 dot resolution and a 75-Hz refresh rate for flicker-free displays. ANSI X3.64-compatible, the terminal has 64 programmable color combinations of its eight primary colors.

With the CIG-267 graphics card

list priced at \$1,195, and the DEC-compatible CIT-161 terminal at \$2,595, the total list price of the DEC/TEK terminal is \$3,790. The Tektronix 4027A's announced list price is \$10,900.

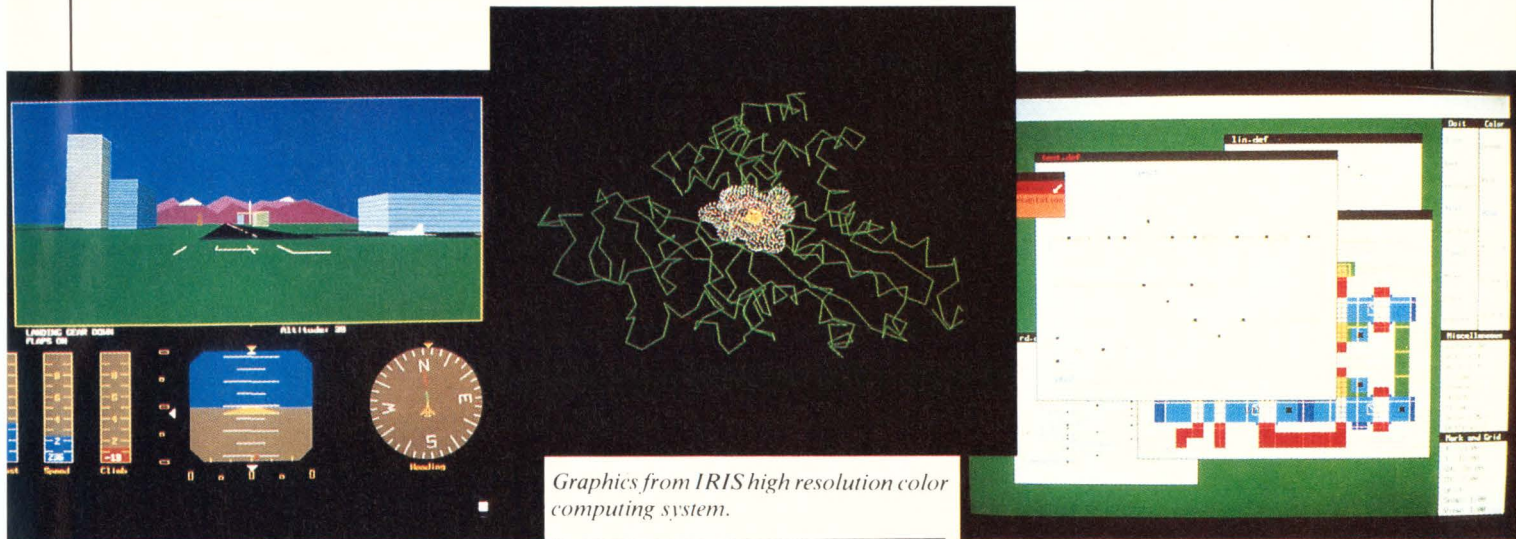
In addition to the CIG-267 card, CIE Terminals offers the CIG-261 color graphics card which extends the CIT-161's performance to include graphics capabilities of the Tektronix 4014 monochrome terminal, though displayed in color. While the com-

mand structures of the 4014 monochrome and 4027A color terminals differ, the CIG-267 integrates both terminals' graphics/plotting commands. CIE Terminals also offers the CIG-201 monochrome plug-in card for its DEC-compatible CIT-101 monochrome terminal that makes the CIT-101 compatible with Tektronix 4010/4014 models, yet still allows the CIT-101 to retain its DEC-emulating capabilities.

— Hanrahan

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Custom Chip Boosts Speed Of Workstation



Graphics from IRIS high resolution color computing system.

Many computer systems aimed at today's workstation market make use of widely available off-the-shelf components, such as the 68000, commonly used bus structures, such as the Multibus, and widely accepted operating systems, such as UNIX. Faced with these design criteria, the workstation designer must aim for an implementation of hardware and software that will bring a unique price/performance ratio to his product in what is rapidly becoming an extremely crowded market.

Silicon Graphics' (Mountain View, CA) answer was to make use of the Geometry Engine, a custom VLSI device patented at Stanford University that helps to bring extremely high speeds to its IRIS Terminal and workstation products.

The IRIS (Integrated Raster Imaging System) is a high performance, high resolution color computing system for 2D and 3D computer graphics. The IRIS Terminal or workstation is a graphics system consisting of a general purpose microprocessor, the Geometry Engine System, a raster subsystem, a high resolution monitor, keyboard and graphics input device. Conceptually, the IRIS hardware is divided into three pipelined components, (Figure 1). The processor, a 68000 manages the display lists and controls the Geometry engine and raster subsystems.

The Geometry engine subsystem includes two custom ICs, the Geometry Engine and the Pipe Adaptor, that provide 2D and 3D integer and floating point geometric processing.

The raster subsystem features a 2903 bit-slice machine and other custom hardware that control up to 24 bit-planes of image memory. The subsystem draws vectors, areas and characters of arbitrary color. Both vectors and polygons may be generated with arbitrary user defined textures with no loss of speed. Both bitmapped and object characters can be displayed. The path connecting the raster imaging system to the display processor can be used to return transformed, clipped and scaled co-ordinate data to the application program. This operation makes the Geometry Engine system available to the user as a hardware subroutine.

The IRIS Graphics Library makes the IRIS graphics hardware available to the applications programmers. This

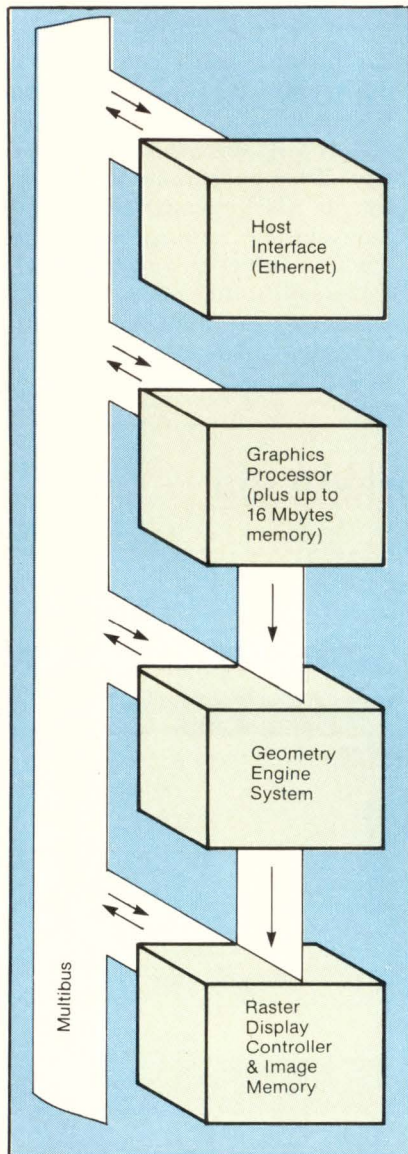


Figure 1: Graphics Processor (68000), Geometry Engine System and color display system.

general display processing system allows the programmer to describe and manipulate objects in world space.

The graphics software divides a program into two processes. The applications process is written by the user and issues graphics commands. Commands are messages to the display process, which controls the IRIS graphics hardware. The display process runs on the IRIS. On an IRIS Terminal, the application process runs on a remote host; on an IRIS Workstation, it may share the processor with the display process.

Graphics commands are issued in one of two modes. In the immediate mode, the commands are immediately interpreted and drawn on the screen; in display list mode, they are stored in data structures and drawn later. In both modes, the drawing commands specify co-ordinates in a user defined co-ordinate system.

The applications process has access to a library of subroutines callable from a high-level programming language. Procedure calls to this library causes messages to be sent to the display process, where the graphics processing is done. If the IRIS is functioning with a remote host, the inter-process communication process might be an Ethernet interface or a serial line. If the host is local, as in a workstation, the communications interface is a simple procedural call. The application program is independent of the communication structure, and may be written in C, Pascal or Fortran.

—Wilson

Write 232

price of a lower resolution terminal.

Anti-Aliasing Techniques

When an infinitely thin line is to be drawn over a grid of points, the job is to find the dots closest to the line, and turn them on. Since in reality pixels are areas, and lines have width, the lines are "sampled" by the pixel centers. Any time a two-dimensional interaction of shapes is represented by a single number in a frame buffer, "sampling" has occurred, so there is no way to get around sampling. What is desired, then, is to compute a color for each pixel to help the eye to perceive the line of width one. Signal processing theory says that if a signal (the image) contains frequencies up to F_{max} , then it should be sampled at twice F_{max} to allow proper reconstruction. Unfortunately, the crisp edges of an ideal line, circle, or square contain frequencies up to infinity, so no finite sampling will be perfect. When the sampling rate is too low, aberrations known as "aliases" appear, and show up as stairsteps and moire patterns. For scenes in motion, the effects are even more noticeable.

The energy of aliasing is inversely related to the sampling frequency, $E = 1/F_s$, which is why the stairsteps are not so objectionable on higher resolution systems. But if the signal were low-pass filtered to eliminate the high frequencies, then the picture would look better yet. Intuitively, low-pass filtering the image corresponds to blurring the edges. Although contradictory, it amounts to the best that the system can do; if higher frequencies are included, the picture will only look worse. The better low-pass filters are all very costly in computation and would make the terminal slow or expensive. It is possible, however, to convolve the image with a filter that is simple to compute and whose spectrum diminishes at higher frequencies. The resultant spectrum is the product of two diminishing spectra, and becomes small in amplitude even faster.

For example, the box filter shown in Figure 1 has a spectrum that diminishes as $1/f$. If a signal is convolved with the box before sampling takes place, the energy of aliasing decreases inversely as the square of the fre-

Filtering Improves Effective Resolution

Image clarity is the target of high resolution terminals, but contrary to the common notion, higher resolution is not necessarily the best method to improve image clarity. The unsightly stairsteps that accompany raster scan terminals are known as "aliasing artifacts," a term from signal processing circles. "Anti-aliasing" techniques reduce the stairsteps and moire patterns and allow finer detail to be drawn without requiring more

pixels in the display.

Until recently, "anti-aliasing" techniques were considerably more expensive and slower than simply adding more resolution, but the development of novel algorithms has reversed the situation. The EG-12000 color terminal from WICAT Systems uses a new filtering technique, embedded in the hardware, to provide the image clarity of a 1440 x 1080 resolution display, while maintaining the speed and

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With VMEbus, you have no limit on the number or types of processors you can use. You can add as many bus masters as you need, when you need them . . . and you can mix 8-16-and 32-bit processors in the VMEbus backplane. It operates asynchronously at high speed, providing seven interrupt and four bus arbitration priority levels for total flexibility. Couple its multiprocessing capability with its reliability and integrity features, its multiple sourcing, and its 20-megabytes-per-second performance, and you see why it's today's international bus of choice.

The logical extension: VMEsystem architecture.

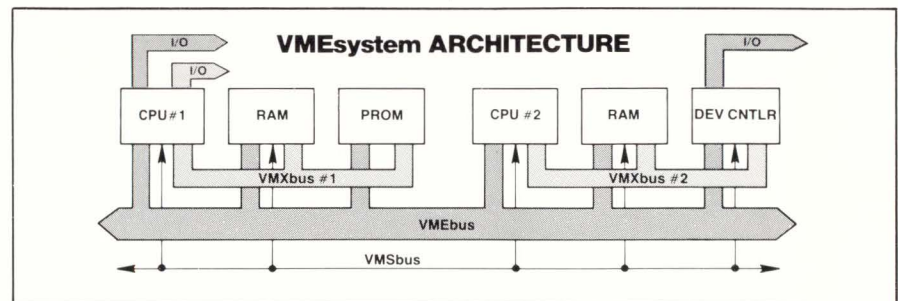
Two supporting VMEbus structures have been recently announced by Motorola and other suppliers: VMXbus, a high-speed memory expansion bus, and VMSbus, a self arbitrating high speed serial bus. With VMEbus, these two new buses expand the total VMEsystem architecture. These speci-

fications will be expanded throughout 1984 to meet demand, and products will be available soon to take advantage of these new architectural features.

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requiring up to five million, 32-bit data transfers each second. You can choose from a variety of I/O Channel-compatible modules available today to meet widespread requirements for analog conversion, discrete I/O, parallel and serial, plus mass storage I/O.

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While not limited to M68000-based systems, VMEbus and I/O Channel are ideal complements for any application employing the high performance MC68000 MPU. A complete line of MC68000-based VME modules is already available, and an aggressive

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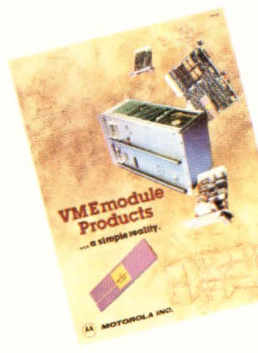
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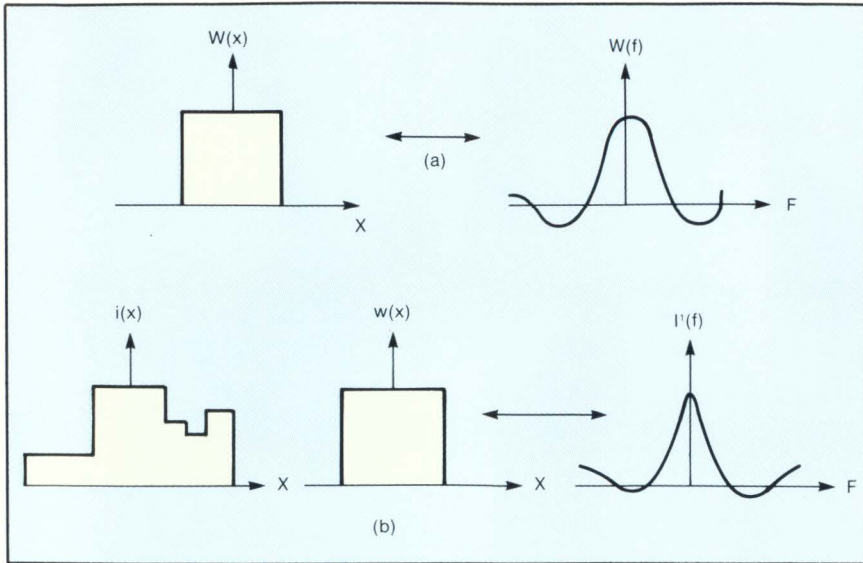


Figure 1: The frequency spectrum of a box is $\sin(f)/f$. When the sharp edges of the image are convolved with the box filter, the resulting spectrum drops as $1/f^2$.

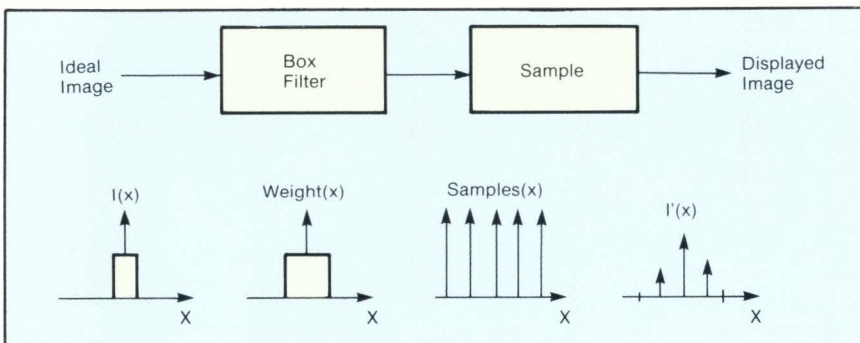


Figure 2: Low-pass filtering an image. The ideal image is the one made of "lines" and "rectangles," objects with sharp edges and high frequencies. (a) shows a system in which the image is convolved with a box filter before being sampled. In (b), a dot (side view) is shown being convolved with a box filter two pixels wide, and then with a sample stream of one pixel intervals. The result is that three pixels on the display are affected by the dot. When the dot moves, even subtly, the brightness of the display will change accordingly and the small motion will be visible.

quency, $E=1/f^2$, and the aliasing artifacts diminish. **Figure 2** shows a system in which the input signal is convolved with a box filter two pixels wide before sampling occurs. A small orange input signal (the edge-on view of a line or dot) is convolved with the box filter and then sampled. In the output image, three dots are affected. Unlike a pure sampling, this system is able to represent subtle movements of the line, as the three dots will change in brightness according to the movement.

Architecture Affected

When put into practice, one problem arises: what to do when lines cross

each other. The solution to this problem will change the architecture of the system. The solution used in the WICAT EG-12000 is to have two "pixlets" at each pixel, so that two different colors may be stored in every pixel. The memory requirement is now only $720 \times 540 \times 8$. Lines on the display are taken to be opaque bars one pixel thick which hide each other. The lines drawn last cover the lines drawn earlier. Each pixel is capable of retaining a history of the last two lines which covered half the pixel. Most of the time, a pixel will contain the background color and one line. But the pixlets are organized as a stack so that when a new line

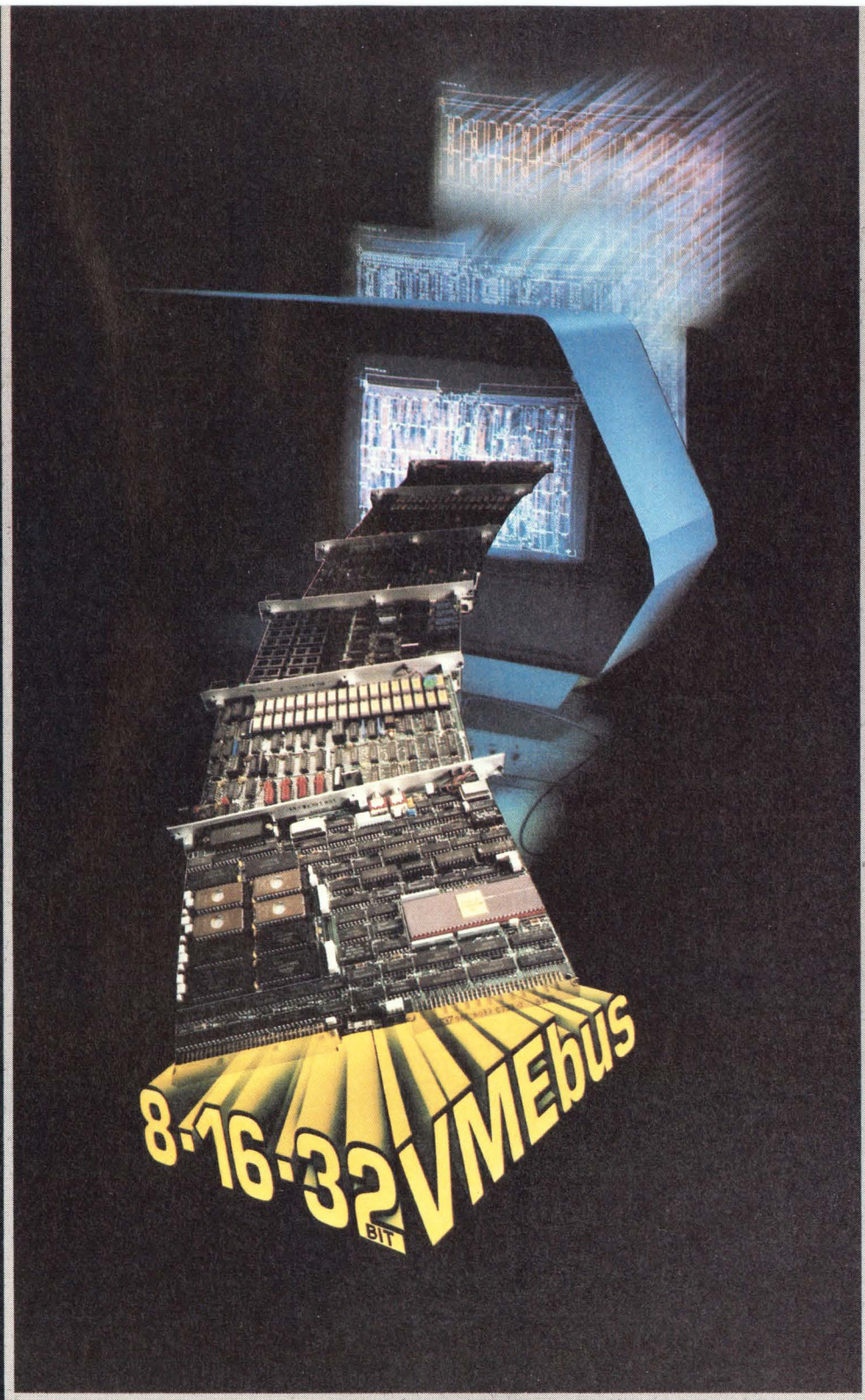
crosses the pixel, the oldest occupant is dropped to make room for the new one.

The advantages obtained are: (1) the frame buffer acts locally as if it has double the resolution. But the double resolution is invoked only when needed, and always in the direction that is needed, not just horizontally or vertically, so that there ends up being a better representation of the image than comes from simply doubling the resolution. (2) Color numbers are stored instead of color values. The advantage of storing color numbers is that there is no loss of information from mixing old and new data. Furthermore, the benefits of separate image planes and color-map animation are still available to the programmer. (3) Should the programmer ever decide to demand full control over the frame buffer, he/she now has eight bits of storage available at each pixel.

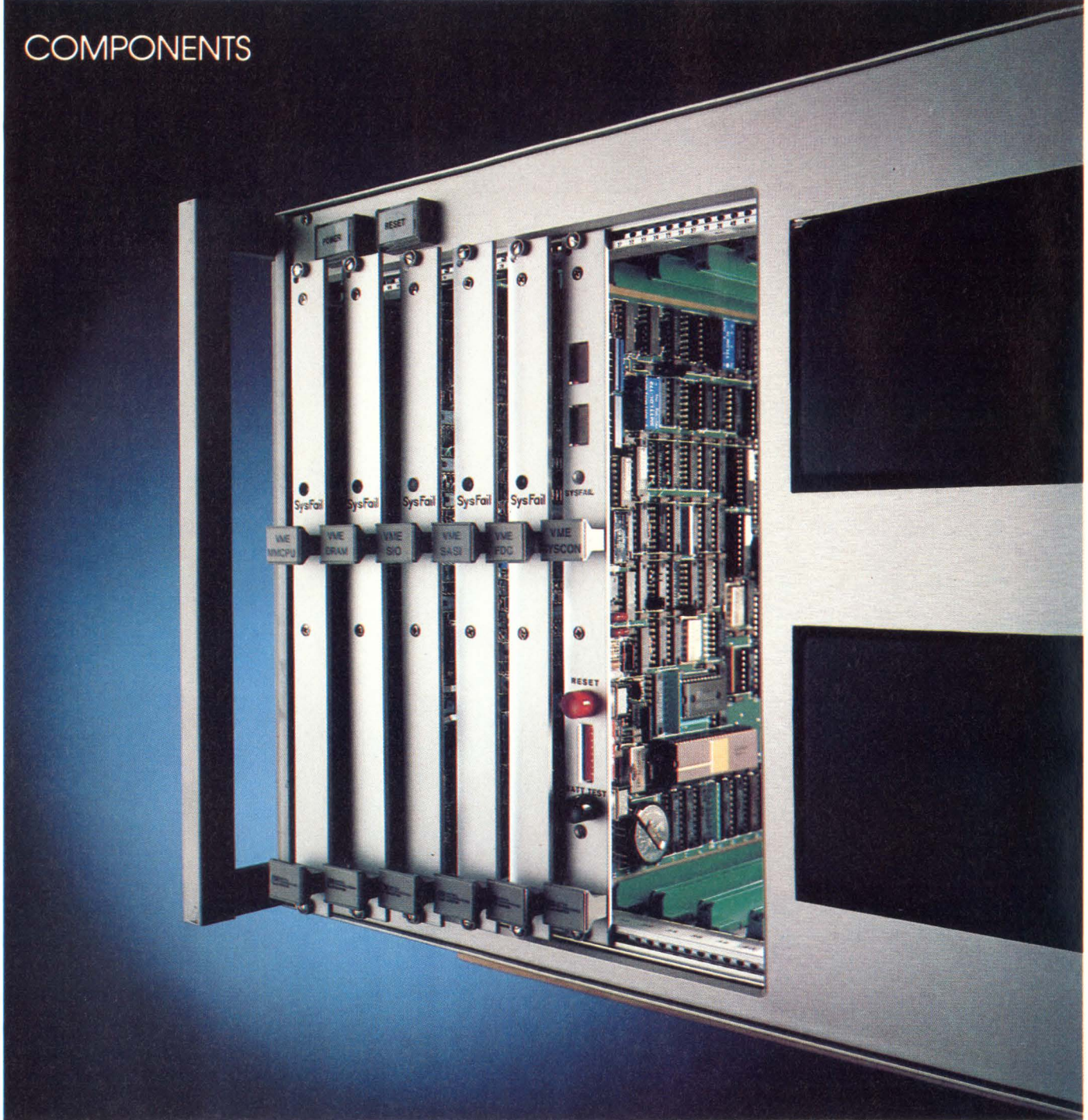
Since the granularity of the system is half a pixel, the vector generator must decide not "what dot is closest to the line," but "how much of each pixel area does this line cover?" It then requests of the memory none, one, or both of the pixlets of each pixel in the path of the line. The pixlets are arranged so that no matter what the slope of the line, if the line covers between one-third and two-thirds of the pixel, it is rewarded with half say-so about the color of the pixel. Finally, given that the memory contains significant information about the lines passing through each pixel area, it becomes feasible to low-pass filter the true colors at the output of the terminal.

The result is a display having effective resolution of 1440×1080 with less objectionable aliasing artifacts, and the speed and price advantages of a medium resolution terminal. "Anti-aliasing" is a generic term which only indicates that some measure has been taken to reduce the stairsteps. Adding resolution counts as "anti-aliasing," as does the averaging together of four samples. But the real benefit comes when the image is low-pass filtered to reduce the high frequency components present in the initial description of the picture.

—Alistair Cockburn, Engineer, WICAT Systems. **Write 234**



Designer's Guide Series **VME Bus**



Preceding page photo courtesy Motorola

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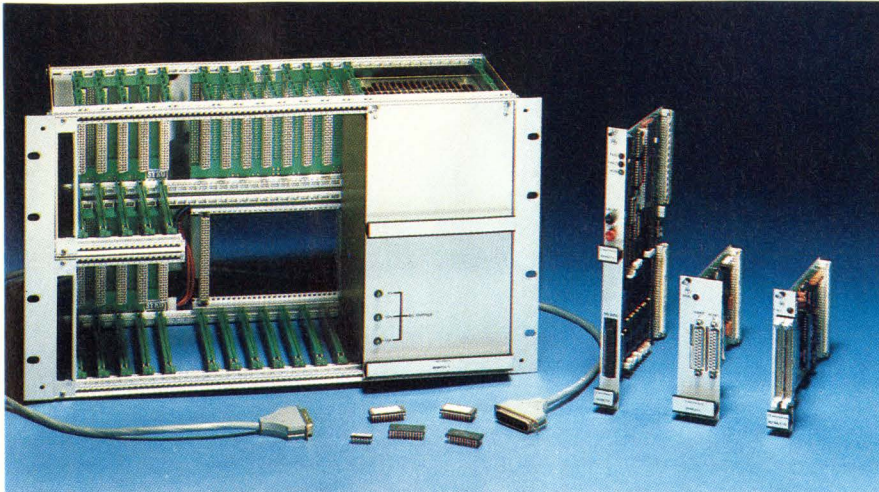
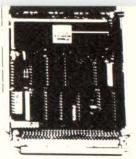
Designer's Guide To The VME Bus- Silicon Simplifies Building Block Approach

by Dave Wilson, Technical Editor

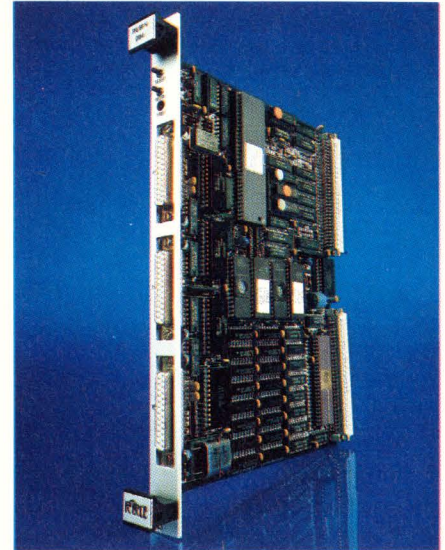
Introduction

The definition of the VME bus is a departure from previous architectures that may have grown haphazardly around the support of one particular processor. The difference is that many other bus specifications focused on the signal lines and the timing of the signal transition on those lines. The VME spec, on the other hand, specifies what logic is on the boards by defining a set of functional modules, and then defining the behavior of these modules. Two primary motives emerge for this approach. First, it allows the IC houses to incorporate the functional modules into silicon, and second, once it is defined in silicon, it eliminates the need for board designers to learn in great detail the specifics of the interface.

The interface functions of the VME bus have been



Motorola's VMEbus chassis, VME 110 Double Eurocard 68000-based computer, Model 400 2-port RS232 serial interface and Model 410 dual 16-pin parallel interface.



The CPU-1 board from Force Computer.

divided into four categories. Each consists of a bus and associated functional modules that work together to perform specific duties within the system interface. **Figure 1** illustrates the individual function modules and the busses contained in the VME definition.

On early products, each of the functional were implemented with discrete SSI or MSI; today, a number of these products, namely the bus arbitration and the bus interrupter have already been integrated into silicon. Since the VME board size is smaller than many other currently used cards, the availability of these ICs may prove implemental in the acceptance of the VME in the marketplace. The VME bus contains a high-speed asynchronous parallel data transfer bus (DTB), that can be logically subdivided into address, data and control line groups. It is used by a processor or DMA device to select a desired peripheral or memory device and to transfer data to or from that location. The number of lines in each of the groups varies with the particular VME bus options selected by the user. These relate to the data path width, that may be 8-, 16-, or 32-bits wide, the address path width, that may be 16-, 24-, or 32-bits wide, the bus time out (BOT(n)), and the sequential access line.

Each data transfer on the DTB occurs between a functional DTB master and a functional DTB slave; the data transfer is initiated by DTB master. The addressed slave must then acknowledge the transfer. The asynchronous nature of the DTB allows the slave to control the amount of time taken for the transfer. After receiving the transfer acknowledge, the DTB master terminates the data transfer cycle.

A set of six address modifier lines allow the master to pass additional information to the slave during transfer (Table I). Slaves in the system may be configured (either statically or dynamically) to respond to a single address modifier code. If there are several masters on the bus, each may be assigned a code to be used when accessing the slaves. This allows for system partitioning and reduces the likelihood that a single malfunctioning master will take down the system.

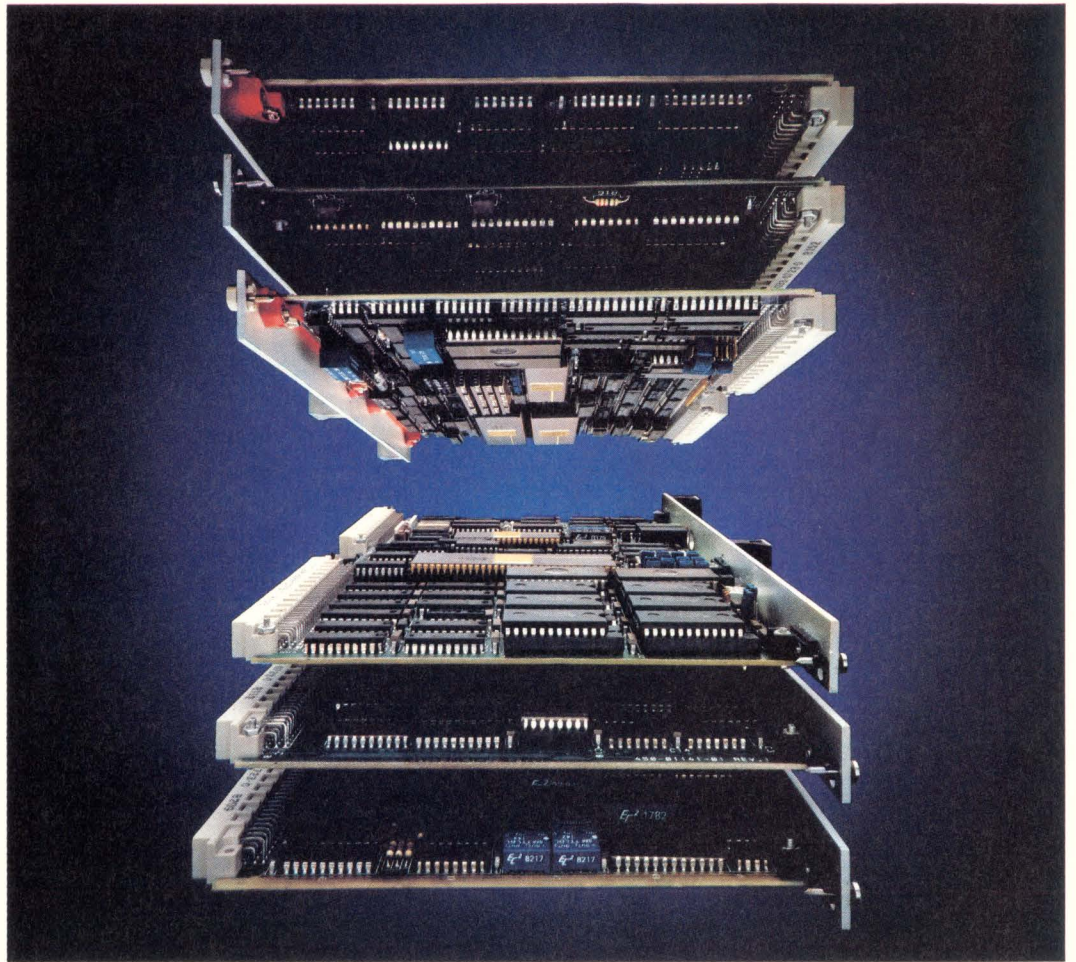
The VME Spec specifies what logic is on the boards by defining a set of functional modules, and then defining the behavior of these modules.

Slaves may be designed to respond at different addresses depending upon the address modifier received. This allows the master using the bus to place the system resources in selected map locations (or eliminate them from the map) by providing different address modifier codes. The AM codes may also be used to specify a special type of transfer cycle; at the moment the VME specification defines a sequential access cycle. The idea behind sequential accessing is to provide a means for accessing several locations in memory without having to provide an address over the bus each time. There are four sequential access AM codes, and when one of these is placed on the bus, the memory boards in the system latch the address into a counter and increment the counter after each data transfer.

Because slaves can be designed to respond to some address modifiers and not to others, it is possible to establish a number of privilege levels. Each master would provide an address modifier indicating its privilege level when accessing a slave. If the slave did not receive an appropriate AM code, it would not respond.

The VME bus provides 31 address lines to allow direct addressing to over 4 billion bytes of memory. For most slaves, however, the extra logic required to decode all 31 address lines is a needless expense. For this reason, the VME spec defines three address ranges — short addressing,

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Third, there's our VME BASELINE System to get you started. It includes three boards (SBC, DRAM, SIO) and a power supply in a 10-slot card cage.

Finally, coming later this year will be UNIX, the high-performance, program-development operating system that opens the door to Pascal and C, as well as our Assembler/Linker software and RADIUS™ development station.

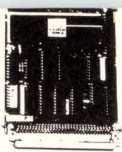
Together, it all adds up to the most powerful and versatile way yet to hit the ground running with a 68000 system solution. To find out more, contact Mostek Corp., 1215 W. Crosby Rd., MS2205, Carrollton, Texas 75006. (214) 466-6000. In Europe, Mostek International (32) 2.762.18.80. In Japan, Mostek Japan KK (81) 3.404.7261. In the Far East, Mostek Asia Ltd. (852) 5.296.866.

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VME Bus

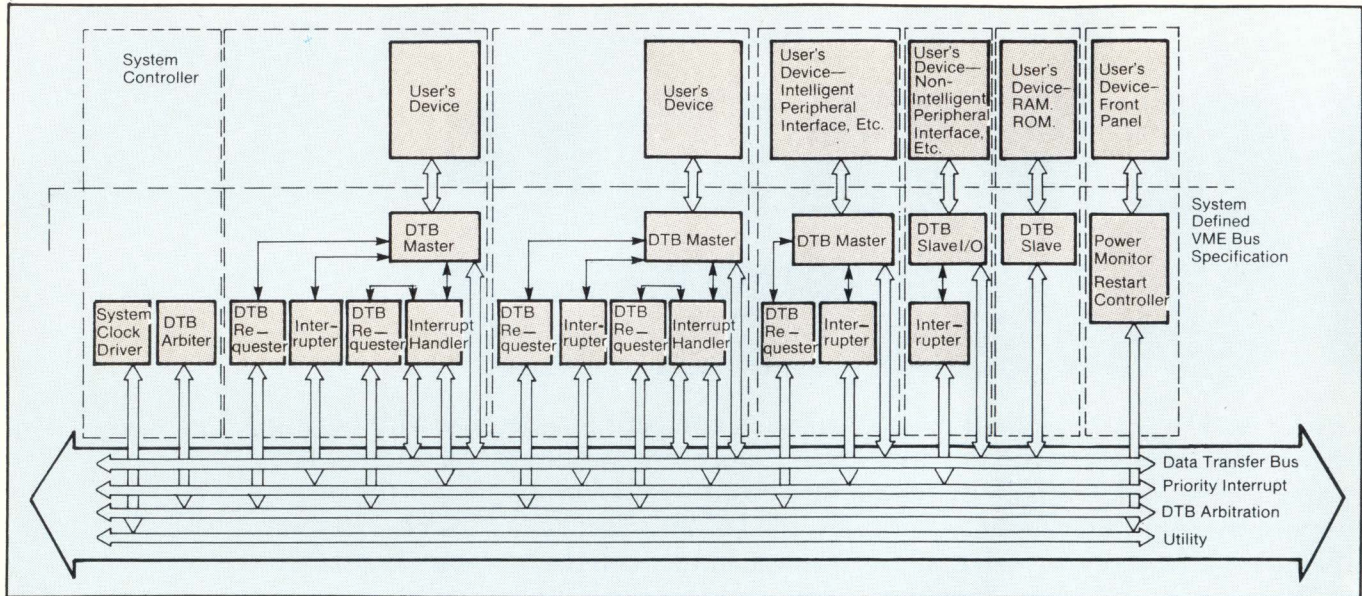


Figure 1: Individual functional modules and busses contained in the VME specification.

64 Kbytes, standard addressing, 16 Mbytes, and extend addressing of 4 Gbytes. A group of address modifier codes is set aside for each group of addressing. By routing the AM lines into the address lines of PROM; the user can program a PROM that gives the decoding required by his system.

Although the concept of address modifiers is a powerful one, it has already led to some incompatibility issues in the marketplace. Some early CPU boards did not make use of the lines, and the designer may have a problem mixing those CPU boards that do not drive the lines with those memory boards that decode them.

Allocating System Resources

In multiprocessing systems that share resources such as memory and I/O, a method of allocating the resources must be established. For example, two processors in a distributed processing system may share a common resource, such as a printer. The resource is allocated by a bit in memory, if the bit is set, the resource is busy; if clear, the resource is available. To gain use of the resource, processor A must read the bit and test to determine whether it is cleared. If the bit is cleared, processor A sets the bit to lock out processor B. This operation takes two bus cycles: one to read and test the bit; the other to write the set bit. However, a difficulty may arise if the bus is given to processor B between these two bus cycles. Processor B may also find the bit clear and assume the resource is available. Both processors will set in the next cycle and attempt to use the resource. This conflict is avoided by defining a read-modify-write cycle which prevents arbitration from taking place between the read and write. This cycle cannot be interrupted by the bus arbitration because AS* (address strobe) is driven low continuously through both cycles, and control of the DTB may only be transferred while AS* is high.

As microprocessor costs decrease, it is becoming more cost effective to design systems with multiple processors sharing global resources. The most fundamental of these resources is the data transfer bus through which all other

global resources are accessed. Therefore, any system supporting multiprocessing must provide an allocation method for the data transfer. In the VME bus, a hardware allocation scheme is provided for bus arbitration. It is designed to prevent simultaneous access of the bus by two masters and schedule requests for optimum resource use. The logic used to implement the bus allocation algorithm is called the arbiter. It may be used to control the arbitration in one of three ways.

An option PRI (Priority) Arbiter always assigns the bus

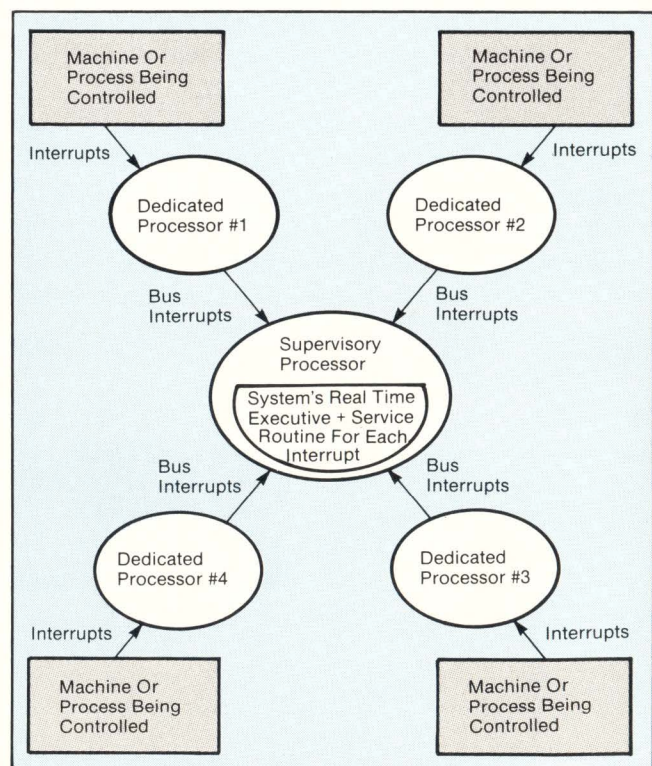


Figure 2: Interrupt structure of a single handler system.

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Electronic Solutions has carefully thought out the problem of VME system building, and we think you will be pleased with the results. VMEasy card cages, for example, come completely assembled with multilayer backplane and termination networks. They are ready to use, ruggedly built, and can be mounted in your system on the bottom or on any side.

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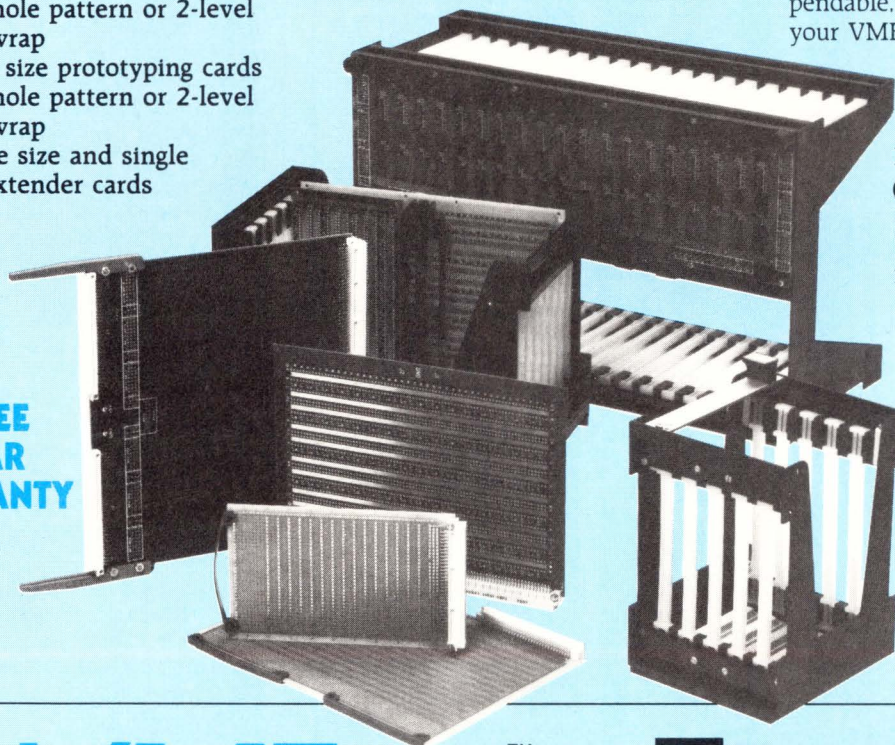
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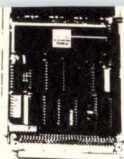
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Form Factor is Critical in VME Bus Design

The VME bus interconnection standard offers designers a multi-processor design capability at 8-, 16-, and 32-bits, which opens up many new markets for board level products, in addition to existing markets in Europe, where the standard has been

used for several years. The VME bus is designed around DIN Eurocard standards, DIN 41612 and DIN 41494. It provides expansion with its unified approach to systems built with true distributed intelligence capabilities. Its wide acceptance in Europe means that vendors wishing to penetrate this market must move quickly to develop products to meet European requirements. Currently, over 60 manufacturers with from one to 20 VME bus products have been identified by the VME bus Manufacturers Group of the IEEE-VME committee, an obvious reflection of the number of suppliers reacting to the VME bus market.

The VME bus is designed to be used in both large and small micro-computer systems. No theoretical upper limits on multi-processors or interrupting units are applied by VME standards, which are rigidly defined in the DIN specifications.

Form Factor is Critical

With our experience at both board design and system implementation levels, we are firmly convinced that the full capabilities of the DIN digital and electrical standards for the VME bus can best be accomplished on a board with physical dimensions of 233 mm by 220 mm. In the prevailing North American standards development activity, in which dy-4 participates as a committee member, the "big three" major manufacturers — Motorola, Signetics and Mostek — have opted for a form factor of 233 mm x 160 mm.

The rationale for designing our VME bus products using the extended (220 mm) board depth is fourfold:

- higher functionality on a single board
- faster memory rates because functional components are located closer to each other, eliminating latency associated with inter-board transfer rates
- capability of combining processors and I/O's on a single board
- allowance for ease of expandability from 16- to 32-bit processor
- long lead times in developing other microelectronic technologies, such as VLSI, which may eventually offer reduced board size for the same functionality.

The extended VME bus boards have been used to enhance board-performance in a number of VME bus boards, for example, on two memory boards, the DVME-102 and the DVME-351.

3 Reasons

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2. **Improve performance** - 16 bit power in a small (100 x 160 mm) size.
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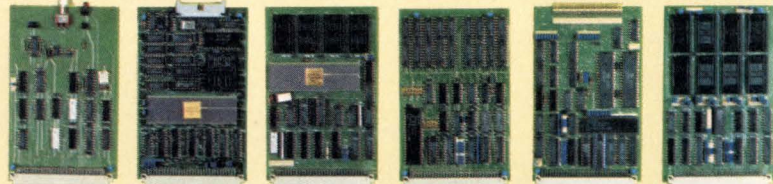
Complete your design quickly with easy-to-package single height VME microprocessor modules from MIZAR. All the features you want are already designed into our modules. If you are looking for a low cost software development system, our VME9000 includes an 8 slot



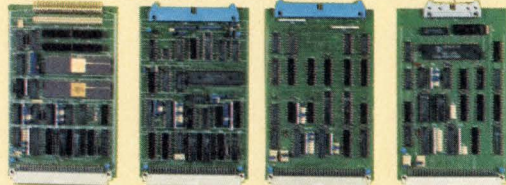
Software Development System

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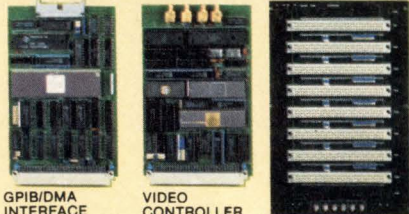
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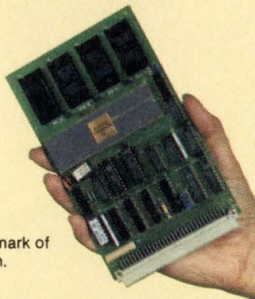
System Controller, 68000 CPU ROM/RS232, 68000 CPU ROM/RAM, 128K Memory, QUAD SERIAL, BYTEWIDE MEMORY



QUAD PARALLEL, FLOPPY CONTROLLER, SCSI INTERFACE, GPIB INTERFACE



GPIB/DMA INTERFACE, VIDEO CONTROLLER, MOTHERBOARD

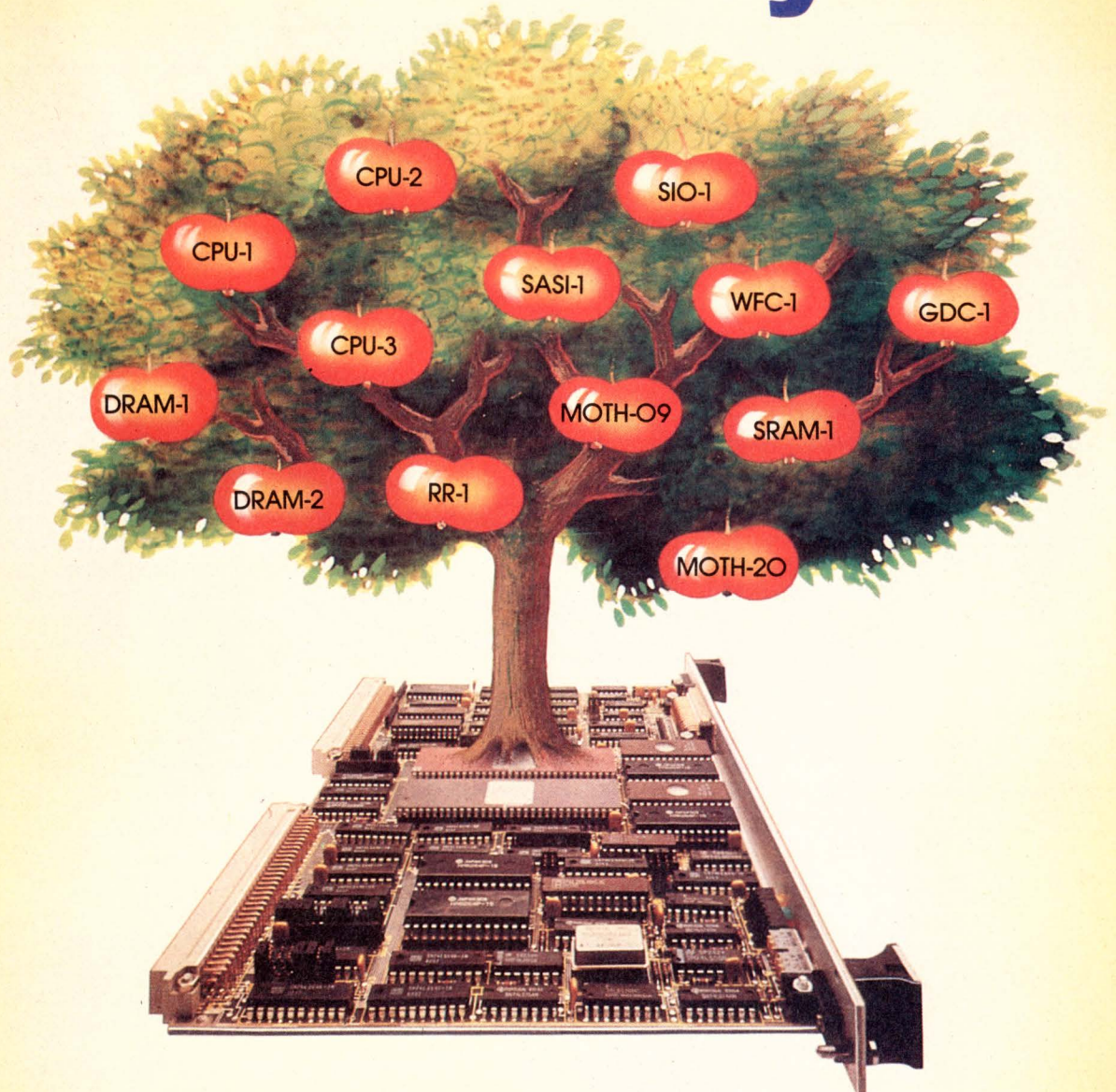


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The VME Family Tree



SYS68K/CPU-1, 68000MPU 8 MHz (10 MHz) 128KB DRAM expandable to 512KB, RTC, 3xRS232, Price \$ 1.450,- + Tax, available.

SYS68K/CPU-2, 68000MPU 8 MHz (10 MHz) 128 KB dual ported (512KB) DRAM, RS232, parallel I/O, slave bus arbitration, Price \$ 1.795,- + Tax, available Oct. 83.

SYS68K/CPU-3, 68000MPU 10 MHz optional, DMAC, MMU, bus arbitration, Price \$ 2.200,- + Tax, available Dec. 83.

SYS68K/DRAM-1/-2, 512KB/2MB byte parity, write acc. 210 ns (max.), read acc. 320 ns (max.),

Price DRAM-1 \$ 1.680,- + Tax, DRAM-2 \$ 5.590,- + Tax, available.

SYS68K/SRAM-1, 128KB SRAM expandable to 512KB, battery back-up, Price \$ 1.600,- + Tax, available.

SYS68K/MOTH-09/20, 9/20 DIN 41612C Female connectors, Price MOTH-09 \$ 470,- + Tax, MOTH-20 \$ 980,- + Tax, available.

SYS68K/SASI-1, handling processor, DMA-controller for up to 4 MByte per sec. transfer rate and interrupt capability. Floppy, Winchester, and Tape control via SASI Bus, Price \$ 1.680,- + Tax, available.

SYS68K/SIO-1, 6 serial multi protocol channels RS232 and RS422, programmable Baud rate, Price \$ 985,- + Tax, available.

SYS68K/RR-1, 8 memory banks max. 512KB, mixed use of ROM's, EPROM's, PROM's or SRAM's, each bank separately jumperable, battery back-up, Price \$ 885,- + Tax, available.

SYS68K/WFC-1, up to 4 Floppy + 3 Winchester drives, 5 1/4 inch, programmable sector size, ECC diagnostics, Price \$ 1.680,- + Tax, available Oct. 83.

SYS68K/GDC-1, min. 16 colors, 256KB display memory, 1Kx1K

Pixels, handling processor, Price \$ 2.780,- + Tax, available Dec. 83.

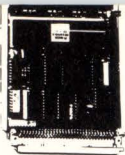
Available Software: Monitor, Editor/68000 Ass., Basic-68K, Forth-68K, Realtime multitasking Nov. 83, Multiuser operating system Dec. 83. All CPU boards are prepared to run UNIX* and CPM68K**. *UNIX is a trademark of Bell Labs **CPM68K is a trademark of Digital Research

FORCE COMPUTERS INC.
2041 Mission College Blvd.
Santa Clara, California 95054
Phone (408) 988-8686
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Telefon 0 89/9510 41-44
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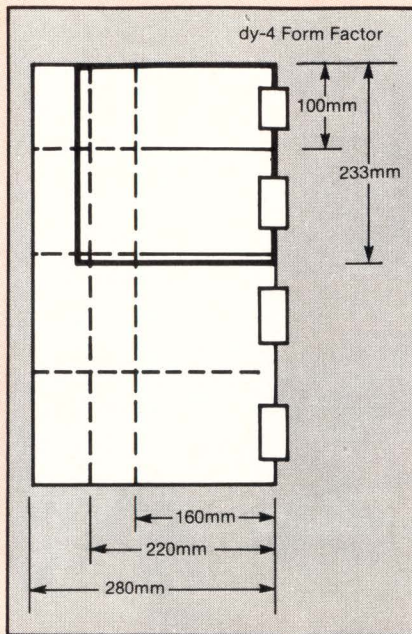


VME Bus

On the DVME-102, the additional board area provided enabled our designers to place both CPU and 256 Kbytes of memory on one board, which means much faster memory access. On the DVME-351, the design criteria was to achieve a 10M wds/S (16-bit word) pipeline transfer rate with 512 Kbytes of memory, and this could only be accomplished on the larger board.

In the case of the DVME-712, using the extended card resulted in a true single-board processor on an I/O card. This board is designed so it can fully access the bus through its own window, so that it looks like an intelligent DMA device. Similar characteristics are provided on our other VME bus boards, with the primary features being faster transfer rates and significantly enhanced functionality — all on a single board.

The form factor specification for VME bus boards should be far-sighted enough to allow for the full range of design capabilities. The VME bus has numerous applications in sophisticated systems with distributed processing and intelligent peripherals.



Using the extended board as a physical basis for the digital functions provides the board designer with the flexibility to optimize board design to take into consideration all of the fac-

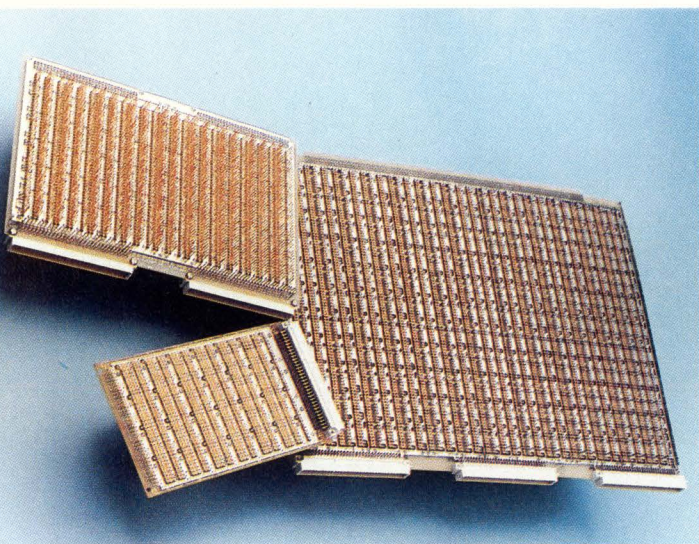
Figure 1: Various board form factors, showing dy-4 Systems proposed VME bus form factor.

tors mentioned above. As well, this capability is obviously of significant benefit to the user in improving data rates, providing high reliability and resulting in an economical board product. The dy-4 form factor concept is represented in **Figure 1**.

As a high performance alternative to other bus offerings, such as Multi-bus, we believe that the extended board is the only configuration which can currently meet the single-board functional capability demanded by the marketplace. Until technologies such as VLSI are proven, our position is that both 160 and 220 mm formats should be incorporated in the VME bus specification, to preserve the credibility of the bus concept.

Kim Clohessy
Vice-President, Engineering
dy-4 Systems Inc.
Ontario, Canada

Write 304



Some Hybricon Corp. customers required VME boards with 3 DIN connectors.

on a fixed priority basis. Wherein each of the four bus request lines are assigned fixed priorities from the highest to the lowest, BR3* to BRO*. An option RRS (Round Robin Select) Arbiter assigns the bus on a rotating priority basis. If the current bus master is at "level n", the highest priority will be given to "level n-1" and proceed sequentially from there. An option one (single level) Arbiter only honors requests on BR3* and relies on the daisy chain structure for priority

determination.

The choice of arbitration scheme depends on the sort of system the designer intends to build, be it a control system or data processing application. In most control applications, fixed priority may be a necessity, whereas for less critical processes, a round robin scheme may be more suitable.

Priority Interrupt

Interrupt subsystems may be divided into two groups: single handler systems and distributed systems. Single handler

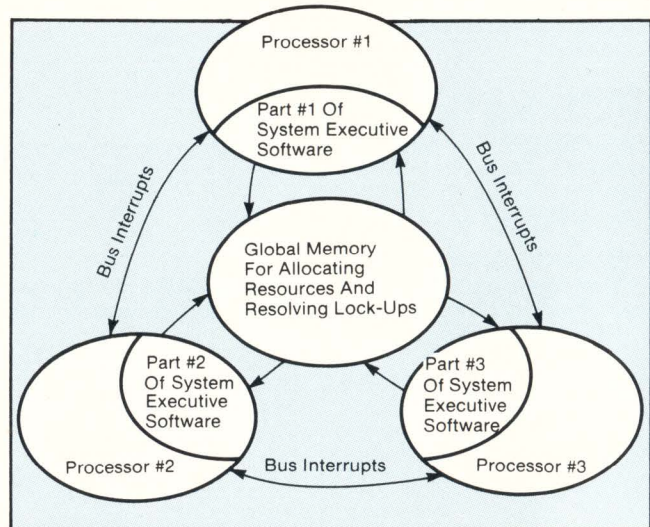
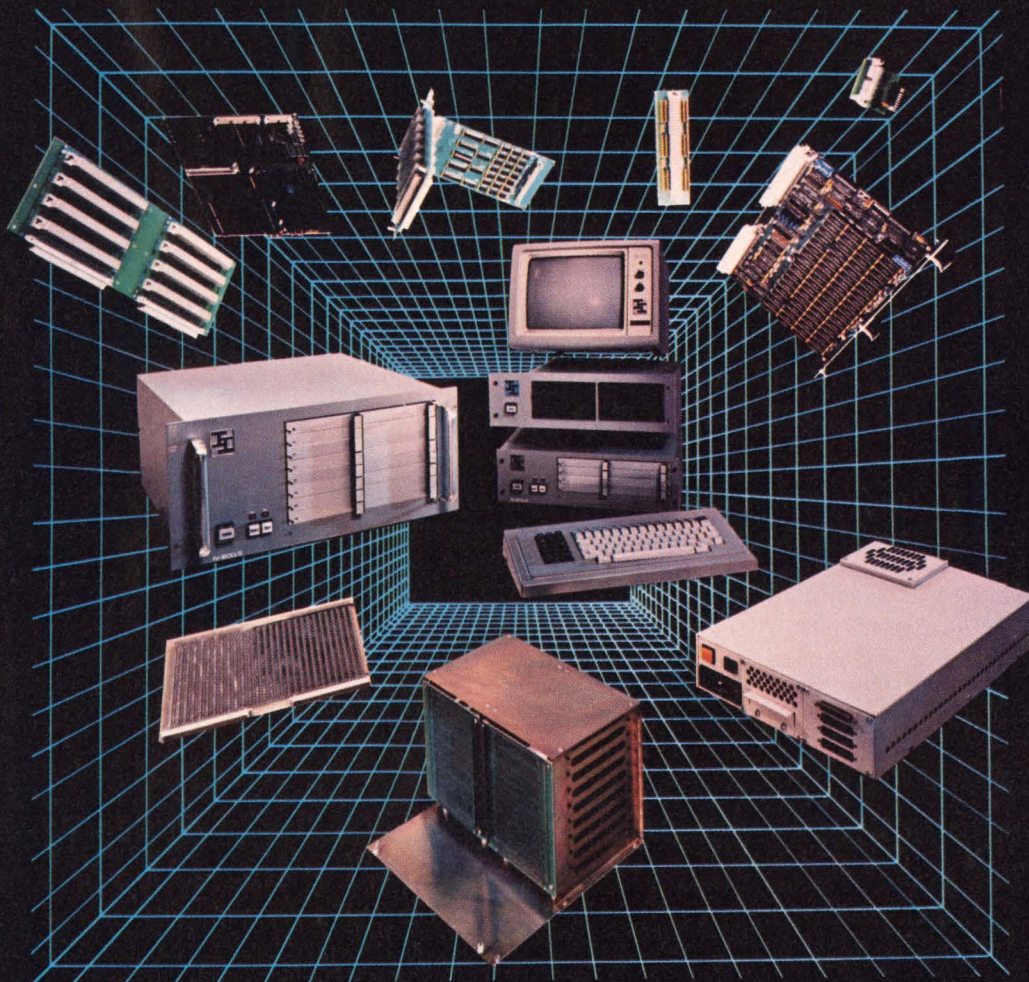


Figure 3: Interrupt structure of a distributed system.

Good News

VMEbus + 68000 + UNIX*



All the best ideas of the 80's integrated into the Ironics development system/workstation.

Better News

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- 68000/68010 12.5 Mhz, no wait states
- Proprietary MMU accelerator boosts throughput
- 256K (1Mb) dual-port RAM

RELIABILITY

- DIN 41612 pin and socket connectors
- Single board SYSTEM FOUNDATION MODULE minimizes interconnects
- Rugged steel card cages and enclosures

EXPANDABILITY

- International standard VMEbus interface
- 512K (2Mb) RAM w/32 bit transfers
- VMEgraf™ high resolution color graphics
- VMEcrt color character display w/downloadable character set
- Intelligent SIO; Industrial PIO • GPIB, A/D/A

SOFTWARE SUPPORT

- IMON68 Debug Monitor
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- CP/M68K** • VRTX*** Real Time Executive
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The Best News!

Ironics development stations are the quickest and least expensive pathway to your end product. They are also the most economical way to get the edge on your competition. Ironics boards, systems, software, and accessories are *available now!*

For all your VMEbus needs... Isn't it **IRONICS**

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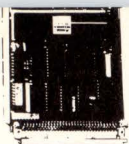
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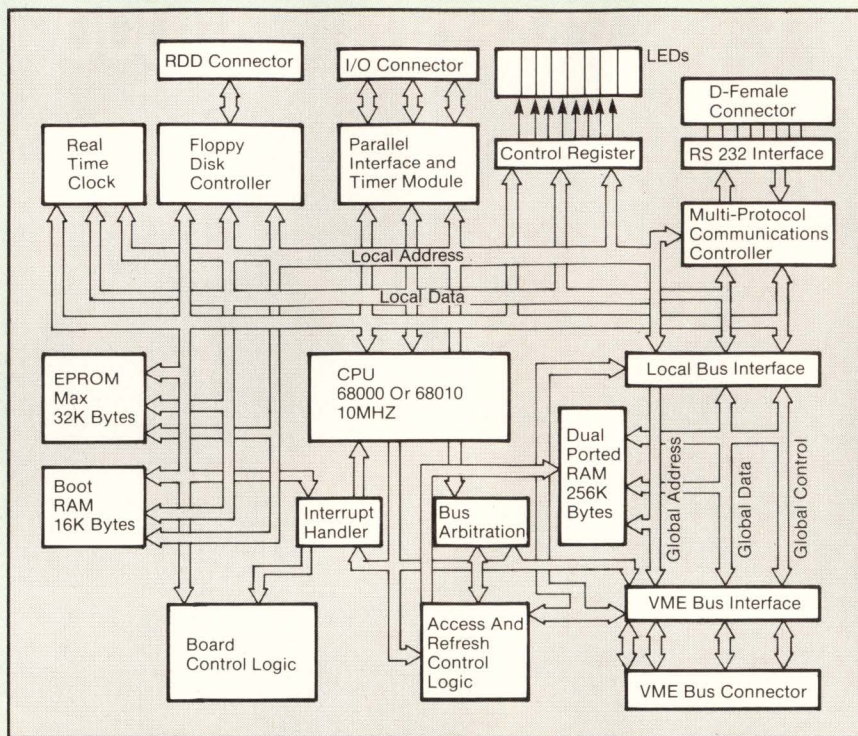
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SBC Includes Dual Ported Memory

Claiming to be second only to Motorola in the VME marketplace, Force Computer (Santa Clara, CA) has recently announced a set of new VME-based products that include the SYS68K/CPU-2 board. Available with a 68010 CPU, it also contains a special I/O interface (PI/T 68230) with 24 bidirectional I/O lines. The board provides variable insertion of 64K or 256 Kbit DRAMs in stacked dual in-line sockets or single in-line chip carrier modules. Parts of the memory can be jumpered to become global memory accessible from the bus, whereas other parts are only accessible from the on-board CPU. An on-board floppy disk controller is compatible with the Shugart interface to floppy disk drives.



systems have one supervisory processor that receives and services all bus interrupts, and distributed systems may have two or more processors for that function.

Figure 2 shows the interrupt structure of a single handler system; the executive software and all the interrupt routines are handled by one processor. This type of architecture is suited to machine or process control applications. The dedicated processors are the ones typically interfaced to the machine being controlled, so it is important that their processing is interrupted as little as possible by bus activity.

The task of controlling machines may consist of several subtasks, some of which are non-interruptable. Therefore

the dedicated processor may mask some or all of its interrupts while executing these non-interruptable subtasks. **Figure 3** shows the interrupt structure of a distributed system. This type of architecture is suited to applications where incoming tasks may be assigned to the next available processor. Each of the co-equal processors executes part of the

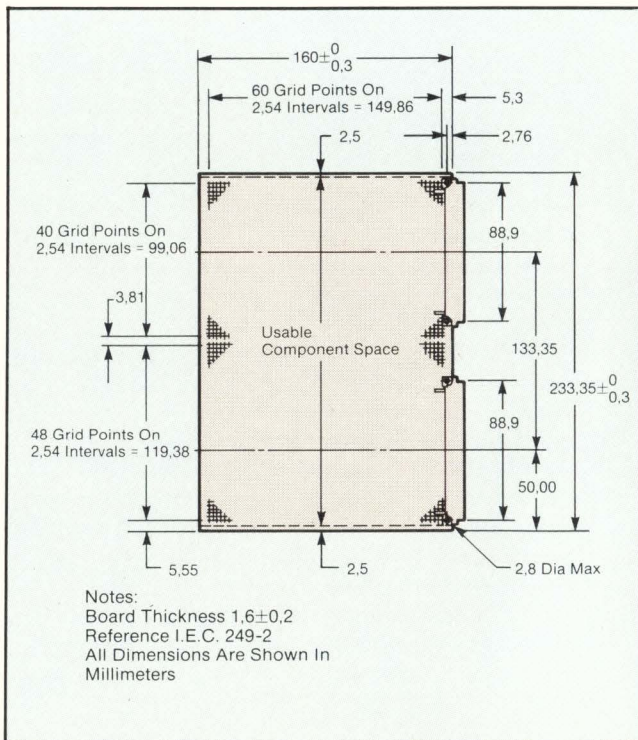
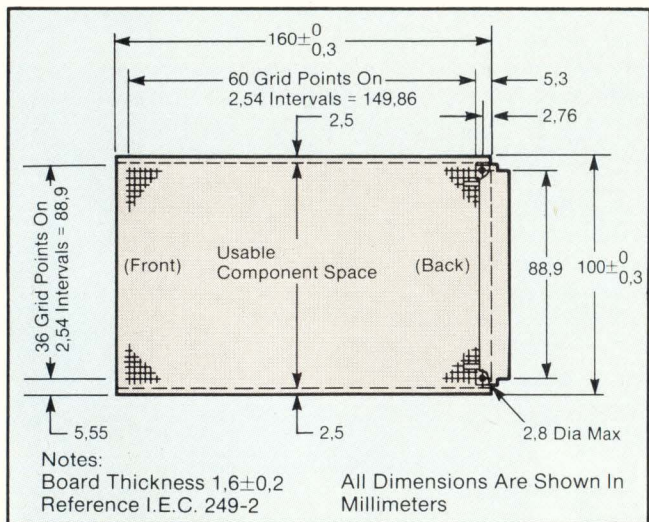


Figure 4 and 5: Single and double height mechanical dimensions.



Ad
Council

Photo: Peter B. Kaplan

If you still believe in me, save me.

For nearly a hundred years, the Statue of Liberty has been America's most powerful symbol of freedom and hope. Today the corrosive action of almost a century of weather and salt air has eaten away at the iron framework; etched holes in the copper exterior.

On Ellis Island, where the ancestors of nearly half of all Americans first stepped onto American soil, the Immigration Center is now a hollow ruin.

Inspiring plans have been developed to restore the Statue and to create on Ellis Island a permanent museum celebrating the ethnic diversity of this country of immigrants. But unless restoration is begun now, these two landmarks in our nation's heritage could be closed at the very time America is celebrating their hundredth anniversaries. The 230 million dollars needed to carry out the work is needed now.

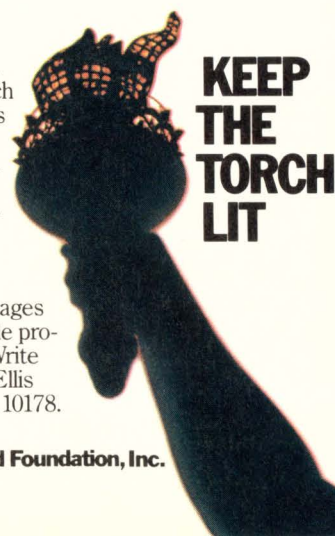
All of the money must come from private donations; the federal government is not raising the funds. This is consistent with the Statue's origins. The French people paid for its creation themselves. And America's businesses spearheaded the public contributions that were needed for its construction and for the pedestal.

The torch of liberty is everyone's to cherish. Could we hold up our heads as Americans if we allowed the time to come when she can no longer hold up hers?

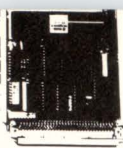
Opportunities for Your Company.



You are invited to learn more about the advantages of corporate sponsorship during the nationwide promotions surrounding the restoration project. Write on your letterhead to: The Statue of Liberty-Ellis Island Foundation, Inc., 101 Park Ave, N.Y., N.Y.10178.



Save these monuments. Send your personal tax deductible donation to: P.O. Box 1986, New York, N.Y. 10018. **The Statue of Liberty-Ellis Island Foundation, Inc.**



HEXADECIMAL CODE	ADDRESS MODIFIER						FUNCTION	DEFINED BY
	5	4	3	2	1	0		
3F	H	H	H	H	H	H	Standard Supervisory Ascending Access	VMEbus Spec.
3E	H	H	H	H	H	L	Standard Supervisory Program Access	VMEbus Spec.
3D	H	H	H	H	L	H	Standard Supervisory Data Access	VMEbus Spec.
3C	H	H	H	H	L	L	Undefined	Reserved
3B	H	H	H	L	H	H	Standard Non-Privileged Ascending Access	VMEbus Spec.
3A	H	H	H	L	H	L	Standard Non-Privileged Program Access	VMEbus Spec.
39	H	H	H	L	L	H	Standard Non-Privileged Data Access	VMEbus Spec.
38	H	H	H	L	L	L	Undefined	Reserved
30-37	H	H	L	X	X	X	Undefined	Reserved
2F	H	L	H	H	H	H	Undefined	Reserved
2E	H	L	H	H	H	L	Undefined	Reserved
2D	H	L	H	H	L	H	Short Supervisory I/O Access	VMEbus Spec.
2C	H	L	H	H	L	L	Undefined	Reserved
2B	H	L	H	L	H	H	Undefined	Reserved
2A	H	L	H	L	H	L	Undefined	Reserved
29	H	L	H	L	L	H	Short Non-Privileged I/O Access	VMEbus Spec.
28	H	L	H	L	L	L	Undefined	Reserved
20-27	H	L	L	X	X	X	Undefined	Reserved
10-1F	L	H	X	X	X	X	Undefined	User
0F	L	L	H	H	H	H	Extended Supervisory Ascending Access	VMEbus Spec.
0E	L	L	H	H	H	L	Extended Supervisory Program Access	VMEbus Spec.
0D	L	L	H	H	L	H	Extended Supervisory Data Access	VMEbus Spec.
0C	L	L	H	H	L	L	Undefined	Reserved
0B	L	L	H	L	H	H	Extended Non-Privileged Ascending Access	VMEbus Spec.
0A	L	L	H	L	H	L	Extended Non-Privileged Program Access	VMEbus Spec.
09	L	L	H	L	L	H	Extended Non-Privileged Data Access	VMEbus Spec.
08	L	L	H	L	L	L	Undefined	Reserved
00-07	L	L	L	X	X	X	Undefined	Reserved

Table 1: A set of six address modifier lines allow the master to pass additional information to the slave during transfer.

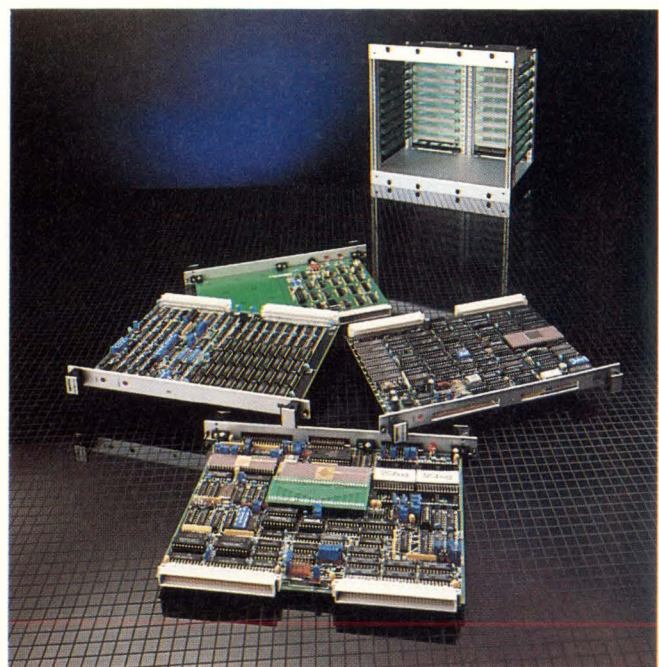
system executive software, and services only those interrupts directed to it by other processors within the system. Since the servicing of some of these interrupts may require an access to system resources, the parts of the executive software must communicate through globally accessed memory to allocate resources and resolve lock ups.

Both types of interrupt subsystems are defined by the VME specification through use of the DTB, the arbitration bus and the interrupt bus. Although the VME bus initially appears to many to be an industrial bus due to its ruggedized appearance and its recent support by Allen-Bradley, it is clear that this does not preclude its use in distributed systems such as described above.

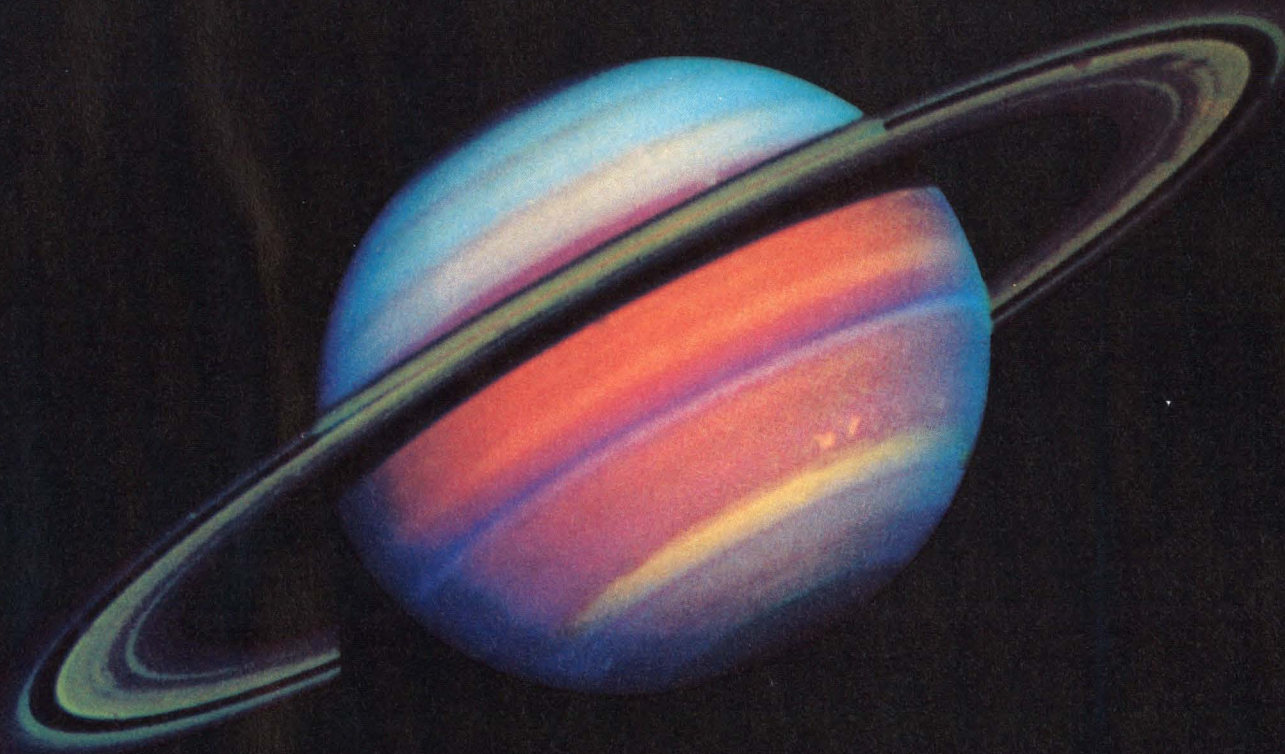
The VMS Bus

When the VME bus spec was originally written, two lines were reserved on the P1 connector for the VMS bus. Its purpose is to provide an alternative path for communication between boards in a multi-processor system. As an example of its use, refer to the example earlier of the two bus process, sharing a common resource or printer.

While one processor is using the resource, the other will be constantly sampling the semaphore on the I/O card to



VME bus modules from Signetics.

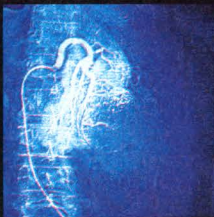


Only your imagination can limit the application of Comtal's new Vision Ten/24 Image Processing System.

Whether you're exploring the outer regions of space or exploring for oil in some remote area of the world, Comtal's new Vision Ten/24 is the only digital image processing system that processes and displays 1024 x 1024 high resolution images with a clarity never experienced before in image processing. It's a powerful tool for interpreting and analyzing images for such diverse applications as LANDSAT, meteorology, seismology, graphic arts, earth resource management, medical imagery, or something only you know about.

Four times the resolution at 30% lower cost.

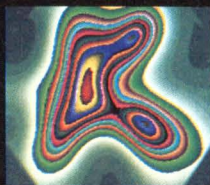
The Vision Ten/24 is the only image processing system capable of processing and displaying images at a 1024 x 1024 resolution in real time (1/30 second) with a 40 MHz video output rate. That's four times the resolution of the industry-standard 512 x 512 systems. With it, whole new worlds open up. Inter-



pretation and analysis become more precise. Best of all, the basic Vision Ten/24 system price is 30 percent less than our previous 1024 x 1024 system because of our design and manufacturing refinements. Giving you incomparable price/performance.

Building block flexibility.

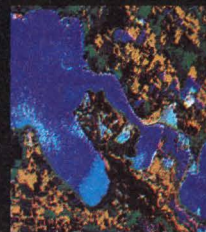
Our modular design approach with the architecture of the Vision Ten/24 gives you flexibility along with easier system upgrades. You can increase video paths, memory size or processing power by simply adding modules. Making the Vision Ten/24 able to keep pace with your image processing requirements. In addition, the system can operate as a standalone image processor or can be interfaced to a variety of host computers.



Comtal—a generation ahead in image processing.

Our new Vision Ten/24 is a generation ahead of any other digital image processing system. It's not surprising since our systems have consistently been the state-of-the-art in image processing. For example, our 512 x 512 systems offer more exclusive features and options, and give you more standard models to choose from, than anyone else. With a decade of experience in image processing and more than 600 systems installed worldwide, only Comtal gives you the leading edge of image processing technology.

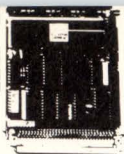
Put your imagination to work and give Comtal a call today for a firsthand look at our new Vision Ten/24. Comtal, a subsidiary of 3M, 505 West Woodbury Road, Altadena, California 91001, (213) 797-1175



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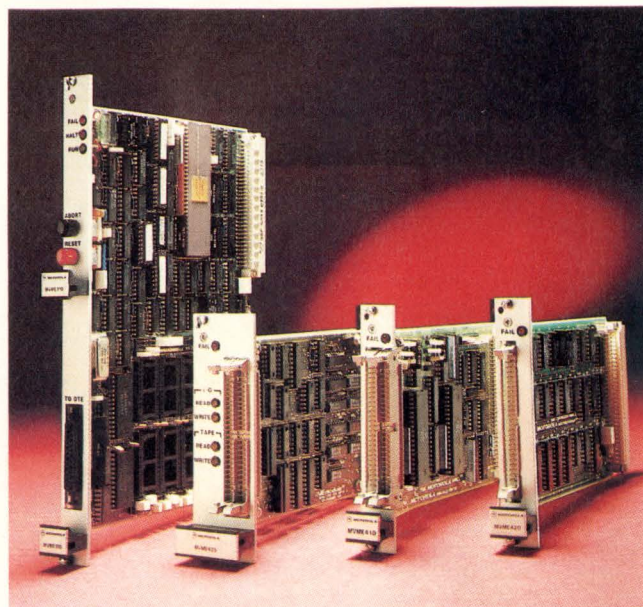
determine when the resource is available. This constant sampling uses up bus bandwidth, and is one reason why multiprocessing systems do not behave in a way that one might predict from a linear analysis. The VMS bus enables the designer to make optimum use of the high-speed, high-throughput bus by moving traffic over to the secondary line.

All boards may have a set of semaphores on them; whenever one semaphore on the system is changed, the corresponding ones on all other boards are changed simultaneously via the serial lines. This eliminates the need to go out to the system bus in order to set a semaphore. The VMS bus also provides a redundant communications path to promote system reliability and fault tolerance.

It is conceivable that the hardware and/or software of a processor module may fail in such a way as to prevent proper system operation. If the failure "ties up" or prevents proper operation of the data transfer bus, the system may fail. The secondary communications path allows the malfunctioning board to be shut off but allows the systems operation to continue in a "limp-along" mode.

The VMX Bus

Standardized bus formats such as the VME bus provide a finite amount of real-estate on each board. Given the addressing capabilities of present day CPU's, it is not physically possible to place adequate amounts of memory directly on each SBC. The VME bus memory-expansion (VMX) bus defines a method of extending the local bus from the



VME 110, VME 435, VME 410 and VME 420 boards from Motorola.

CPU on each SBC through 64 pins on the "A" and "C" row of the P2 connector. This interface then connects the SBC to memory boards that would not be accessed over the main

Use of VME Based Components in Sophisticated Machine Control

Requirements for a low-cost computer system with a small packaging constraint which, at the same time, is able to provide the processing power required for sophisticated real-time machine control, presents conflicting goals for the computer systems designer. In the case of the computer control system for the Varian VLS-1000 Electron-beam Lithography System, used in the production of VLSI devices, the ability to interface such a system to off-the-shelf and custom inhouse-built machine interfaces is a key added requirement. With this background, the decision was made to use a VME bus-based computer system on two points. First, the use of the Motorola 68000 microprocessor interfaced to the VME bus provided the processing power required. Second, interfacing custom inhouse-built machine interfaces to the bus, with its reliable DIN connectors, was possible because of its architecture and non-proprietary nature.

The VLS-1000 (Figure 3) uses six microprocessors in its control system as illustrated in Figure 1. They are organized into three levels, with the computer system at the top dealing

with overall system control, user-interaction, and data storage, the two in the middle performing high-speed sophisticated machine subsystem control, and the three at the bottom level performing low-level, less intensive, subsystem control operations.

It is the two computer systems at the middle level which are M68000 VME bus-based. Performing the calculations required keeps the MPUs

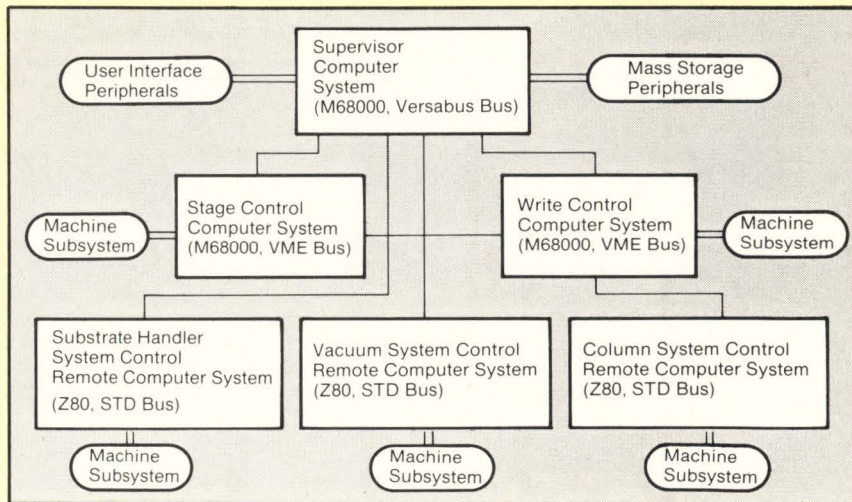
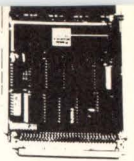


Figure 1: Varian VLS-1000 Computer Control System.



very busy while these systems interact with their controlled subsystems and each other. The communications between these two systems constitutes the primary traffic activity in the tri-legged, point-to-point network connecting the three M68000 MPUs. Although these computers are in constant contact with their subsystems and each other, the data flow within these computers is such that the VME bus' bandwidth and data transfer width were not required selection criteria.

From several points of view, in particular the manufacturing and servicing aspects, it is highly desirable to incorporate a distributed computer control system as used here where the number of similar computer systems with identical components (such as memories and communication links) is maximized. It is here that the technical appeal of the VME bus has been tarnished by practical concerns over the actual availability of required VME bus interfaces not to be produced inhouse, but instead purchased "off-the-shelf". In referring to **Figure 1**, it was designed to have all three M68000-based systems in the top two levels be VME bus-based systems identical except for the machine-specific interfaces. This design was reluctantly changed to incorporate a Versabus-based supervisor which readily delivered the required elements lacking in a VME bus environment — high-level multitasking software and disk, magtape, bulk semiconductor memory, and color graphics display interfaces. In fact, the problem of availability of the VME bus has been prevalent since Varian's selection of it, as the photograph in **Figure 2** of a VME single-board-computer built inhouse while awaiting "off-the-shelf" versions, illustrates.

Fortunately, more and more of these unavailable items are becoming available, allowing the use of VME bus-based systems in more applications such as the supervisor system in **Figure 1**. With respect to the computer systems in the bottom level of **Figure 1**, it appears that it will be some time before these STD bus-based systems can be replaced with VME bus-based systems similar to the others in the control system. The STD bus provides a much greater selection of interfaces, such as pneumatic relays and stepping motor controls, and it was for exactly this reason that this bus was chosen for the bottom level

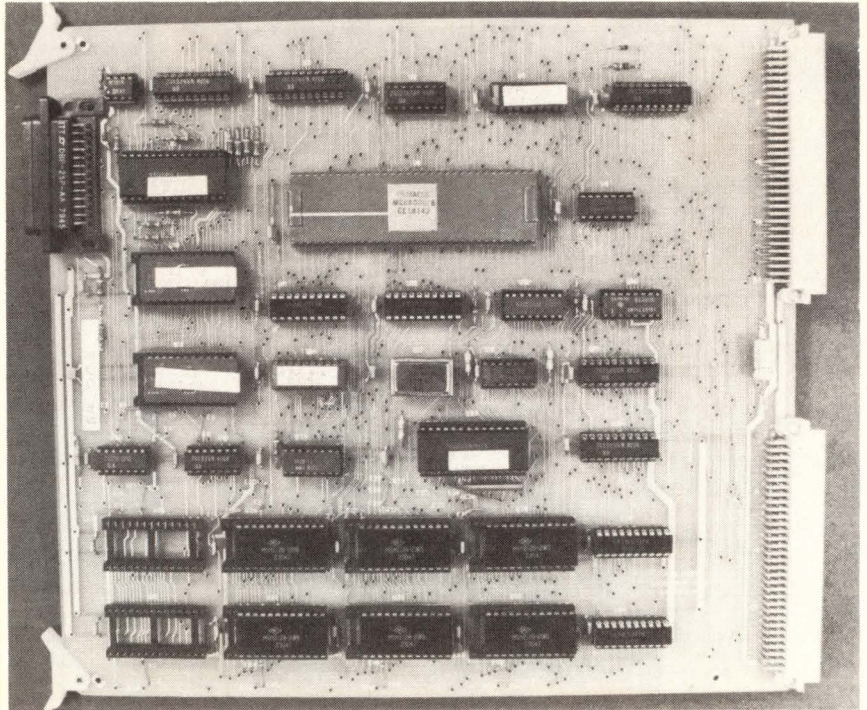


Figure 2: VME Single Board Computer.



Figure 3: Varian VLS-1000 Electron-beam Lithography System.

applications.

From Varian's perspective, the promise put forth by the VME bus and the various manufacturers involved with it, that of standardization, high performance, and small form factor, will continue, at least for the near term, to be overshadowed by a lack of component availability and a firm footing in the marketplace. But from a

technical approach and as it gains further acceptance, our use of the VME bus in the VLS-1000 has been trying yet successful.

—Glenn M. Cooley, Manager Computer R & D, Varian Assoc., Lithography Products Div., Blackburn Ind. Park, Gloucester, MA 01930 **Write 303**



PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	DB0	+5 Volts	DB1
2	DB2	GND	DB3
3	DB4	RESERVED	DB5
4	DB6	A24	DB7
5	GND	A25	DB8
6	DB9	A26	DB10
7	DB11	A27	DB12
8	DB13	A28	DB14
9	DB15	A29	GND
10	DB16	A30	DB17
11	DB18	A31	DB19
12	DB20	GND	DB21
13	DB22	+5 Volts	DB23
14	GND	D16	DB24
15	DB25	D17	DB26
16	DB27	D18	DB28
17	DB29	D19	DB30
18	DB31	D20	GND
19	A0/12	D21	A1/13
20	A2/14	D22	A3/15
21	A4/16	D23	A5/17
22	GND	GND	A7/19
23	A8/20	D24	A9/21
24	A9/21	D25	A10/22
25	A11/23	D26	GND
26	LAS*	D27	UAS*
27	R/W*	D28	GND
28	LDS*	D29	UDS*
29	BERR*	D30	MATCH1*
30	ACK*	D31	MATCH2*
31	LWORD*	GND	GND
32	SMRQ*	+5 Volts	SMACK*

Table 2: J1/P1 (right) and J2/P2 (above) pin assignments.

PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK (1)	A17
22	IACKOUT*	SERDAT (1)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

NOTE:

(1) SERCLK and SERDAT represent provision for the special serial communication bus protocol.

system bus, but privately over the VMX bus.

Due to lack of arbitration for mastership of the VMX and benefits from optimized timing for MMU and DRAM, memory access cycle performance will approach "on-board" memory performance.

Up to five VME boards may be connected to each VMX system and up to ten VMX systems (2 boards on each VMX) may exist in a maximum VME bus system (20 boards).

The VMX uses 12 multiplexed address lines and 32 non-multiplexed data lines together with a dozen control and command lines. Two data strobes (upper and lower byte) and two address strobes (upper and lower 12-bit address) with one acknowledge line complete the basic interface.

Dimensions

There are two sizes of VME boards defined in the specification. The single high board has only one 96-pin DIN connector (P1 on its back edge) while the double height board has two. The 96-pin DIN connector must be used when the board is designed to use P2 for address and data bus expansion.

Figures 4 and 5 show the single height and double height

mechanical dimensions; although some third parties have proposed other form factors that are Eurocard compatible (see "Form Factor Is Critical In VME Designs").

Conclusion

There are now two contenders in the advanced systems architecture marketplace: the VME bus and the Multibus II. While many have expressed their concern over some of the features that the VME lacks, such as no parity on data transfer and poor ground and power layout leading to backplane noise and crosstalk, the fact remains that the product is available now, whereas none exists for the Multibus II. Interestingly, Intel has chosen a multiplexed synchronous bus, whereas the VME is non-multiplexed and asynchronous.

With the Multibus II design, a full 32-bit design may be placed on a single height card; the VME needs a double height card. Due to card size and packaging, both these structures will initially cost more than conventional Multibus boards. As VLSIC's and pin-grid ICs come to their aid, they will gain greater market acceptance. □



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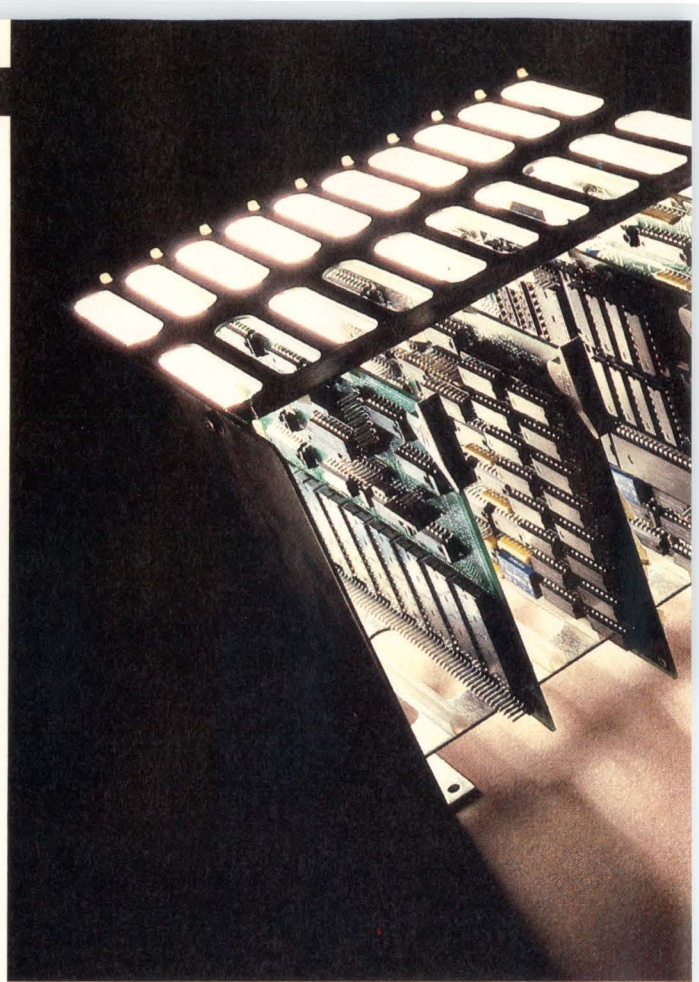
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Looking Ahead: A Forecast For The '80s

1984 appears to be the key year when manufacturers will begin to examine issues such as design and architecture for the fifth generation computer systems.



by *Digital Design Staff*
M. R. Hanrahan, Editor

The predominant trend in computer systems in 1983 and continuing into 1984 is for an increase of performance at lower levels of cost. The driving factor is the new generation of 32-bit microprocessors. Proprietary chips from Hewlett-Packard and Bell Laboratories have been used for systems, however it will not be until 1984 that we see 32-bit processors from National, Intel, and Motorola reaching manufacturers. As manufacturers rush to implement these new products, applications software will limit their use.

16-bit processor systems are coming into their own, as software is finally available for wide applications. The IBM PC is the largest contributor to growth in this area, and its impact will be not only on small business applications, but also on large industrial and manufacturing uses — especially in light of the IBM announcement for the new PC for home use and the dual Motorola 68000-based mainframe PC system. HP has already established a strong presence in this market and if secondary announcements for software and upgradeable hardware are forthcoming it will be a powerful part of the new "desktop mainframe" market.

Multiuser Systems

Multi-user systems have also been an area of rapid growth. By the end of 1983 there were over 60 manufacturers producing systems for this market. At the top end of performance were companies such as Convergent Technologies, Naked Mini, Momentum, Charles River, and others. Some manufacturers claim performance sufficient to support 64 or 128 users, and the claims are not exaggerated.

The dominant shaping factor for all of these systems is their operating system design, for even with more powerful or multiple processors, performance depends upon the ability to serve many users without prohibitive delay. Not surprisingly then, UNIX, which is suited for multi-user OS environments, was one of the most intensely developed areas. 1983 saw such a proliferation of efforts to develop the OS that a key issue for 1984 is the continuing work towards standards for its use and implementation.

Communications

A related trend has been for manufacturers to use an existing version of UNIX as a core set of functions for their development of a proprietary operating system. Charles River Data's

UNOS, and Prime Computer's PRIMOS are examples.

A second factor contributing to the growth of multi-user systems is the rapid decrease of cost for online memory from hard disk drives. The use of 40 to 60 Mbyte drives became practical in production quantities during 1983, and 1984 should see system builders making use of 100+ Mbyte drives. Many system integrators already provide several hundred Mbyte options through the use of larger 8" or 14" drives, or by incorporating several of the available smaller drives into the systems' central chassis.

Both of these developments in multi-user systems implies another requirement for the systems — that of communications. With more terminals to compete for processor and memory resources, the system builder must be able to provide efficient communications channels if performance is to be maintained. Two approaches have seen increasing use: that of dedicated communications networks and/or the use of processors dedicated to serving access to peripheral devices. Proprietary networks grew rapidly in 1983, with Apollo's Domain being the most prominent. As a result of the rapid growth of networks such as Domain

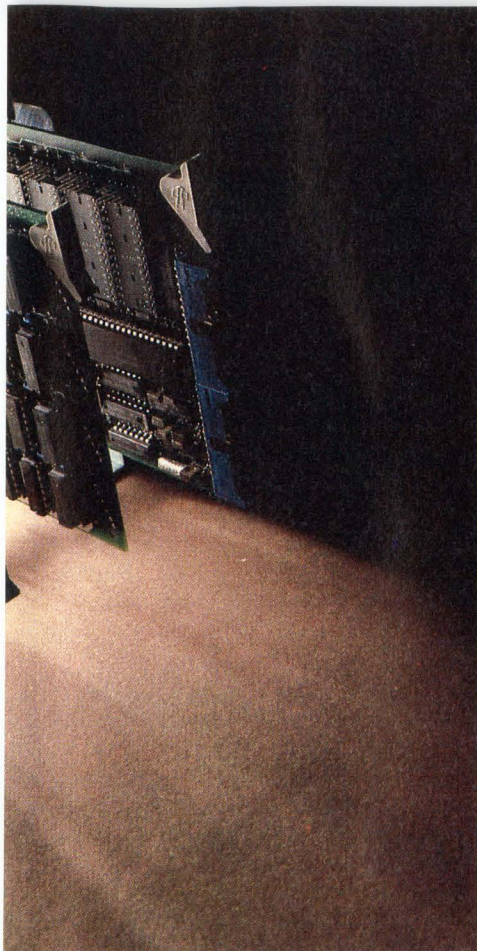


Photo courtesy Mostek Corp.

and others such as Ungermann-Bass' Net One, many manufacturers indicate that they are going to use more standardized networks such as Ethernet.

Array Processors

If the computer industry has its giants in IBM and Digital Equipment Corporation, the array processor business has its analogy in Floating Point Systems. FPS and DEC are similar in many ways. Both have conventionally provided high-end systems and both have recently been attacked at the low-end by a number of companies. However, both companies have a large base of installed systems, accompanied by many man-hours of user software that provides some buffer for them against the competition.

Over the past two years the competition has been coming too thick and fast for either company to ignore. DEC reacted to the supermicro market with the Micro-VAX I and the FPS-5000 is clearly a pointer as to how Floating Point intends to move into the low-end.

At the board level, Sky Computer (Lowell, MA) has carved a market niche that has little competition, perhaps with the exception of Marincos (San Diego, CA), a company that got off to a rough start this year with some

peculiar claims relating to the performance of its Multibus board.

At present, Sky supports the Multibus, Versabus and VME standards. The choice of busses, according to Gerald Shapiro, President of Sky, relates to both engineering and business judgment. The business side involves market size—that is, how many bus slots can be filled, likely candidates for the product, both now and in 18 months. The engineering judgment revolves around the amount of specialized engineering and production work required. Examples include: can an asynchronous bus interface model be used, what sort of IC packing density is required, and what unique mechanical considerations must be considered.

These board level products are aimed at increasing the processing power of microprocessor-based computers. Omegatek (Henderson, NV) has discussed building a workstation around an Intel 286/IO board coupled with the Marincos Multibus board, and Charles River Data has already used the Sky product in some Universe 68000-based systems.

Moving up to more expensive designs, two announcements this year from Numerix (Newton, MA) and Mercury Computer Systems (Belmont, MA) fall into the market area currently occupied by products like Analogic's AP500.

The Numerix 432 has come as an extension to its current product line that currently includes the Mars 132 and 232 fixed point processors, whereas the Mercury 3216 comes from a newcomer to the field. If benchmarking the performance of computer systems is a difficult task, evaluating the performance of an array processor is next to impossible; the processing times are highly application specific, and the MFLOP rating or single function execution times (such as the FFT) are only partial indications of performance.

Perhaps a more important criteria is ease of programmability. Today, programmers may be required to program an AP at a number of different levels, including high level, assembly language or machine code. Clearly, the machine that offers the greatest flexibility in this area may be at a considerable advantage to the competition.

Recognizing this, one company, Mercury Computer, allows programmers to generate application routines in a C-type language that are then callable from a high-level language, such as Fortran. At the high end, Star Technologies recently announced its first shipment of the Star ST-100 product to Geo-X systems of Calgary, Alberta. Star Technologies, (Portland, OR) is a spin-off, start-up from FPS and are definitely aiming to walk directly into the FPS backyard with this product.

The market for array processors is healthy and dynamic and should continue to be so into the 90's. The availability of dedicated signal processing VLSI products, such as AMD's 29116, TRW's multiplier range and future products from Analog Devices and TI can only fuel the market.

Supercomputers

At an even higher performance level than array processors is Control Data's system to supplement its own and other companies' supercomputers. The new CDC system device is said to be capable of 11 gigaflops per second. All of these systems are intended to speed mathematical processes such as floating point operations. For image processing or real time graphic displays, these systems should provide users with dramatic capability for 1984.

1984 appears to be the key year when America will begin to examine issues such as design and architecture for the fifth generation computer system. Some systems designers noted in 1983 that systems such as the Cray and Cyber supercomputers were recognized as high performance systems within the current generation of computers, while approaches such as those discussed by the Micro Computing Consortium and by Trilogix Corp. are indicative of new approaches that will lead to higher orders of performance.

It is work in this area that is likely to be shared by the rapidly developing field of custom and semi-custom development tools.

CAD

Computer aided design tools for the next generation of computer systems

have achieved recognition. The primary thrust of the year's announcements were for increased capability of both integrated circuit and printed circuit design, but this year and next will see the availability of systems that place more of the design engineers' function onto systems as software libraries. Not only is the range of functionality of these systems expanding to include schematic capture, logic diagrams, simulation, verification, artwork, and mask generation, but the newer systems are able to provide designs for specific silicon products allowing the designer to not only automate the design function but to increase his interaction to include manufacture functions.

Bus Architectures

For decades, the Von Neumann architecture has been implemented in computer designs. Although the technology used to implement the architecture may be different, today it can be seen in products ranging from personal computers to mainframes. The '80s has seen new standards for VLSI densities for microprocessors, memories and support logic. New techniques for gaining performance are emerging to address the need for ultra-high performance low-cost systems for the '90s.

But the two largest computer markets, commercial and industrial, each dictate their own unique set of requirements to the designer. Conventionally, the commercial environment has been dominated by high-speed single processor systems time-shared between a number of users.

In the '80s, microprocessor-based computers emerged with a dedicated CPU for each user. Although this approach eliminated some of the delays associated with a multi-user single processor system, it creates a possibility of redundancy; a resource could be idle if the system is not fully loaded.

Obviously what is required is a multi-processor, multi-user system capable of dynamic task allocation, i.e., one central processor allocates a series of other machines' tasks from the user as they need to be executed. This type of system could be built in a number of ways using today's technology.

A multiple 68020-based system would be one approach. The problem here is that the 68020 is a general pur-



Photo courtesy Lexidata Corp.

pose processor. An alternative approach would be *configurable* processors in a multiple-processor system. Processors that could be tailored to execute only a specific set of instructions would give a significant speed advantage. This is a good concept, but making it reality on a broad scale may be closely tied to the sorts of non-proprietary systems architectures that are now emerging in the Multibus II and the VME bus.

Architectures also play an important role for the industrial computer designer, although industrial designs are more loosely coupled and find their way into more distributed computing environments. In a sense, meeting the needs of the application is most important in industry, not building a large number cruncher that could be overkill for the application.

For that reason, the STD bus, with its small form factor, has provided a very low cost tool for many designers in the field. The availability of a large number of boards for the bus has alleviated the headache of in-house designs, and brought systems to market quickly. As more powerful microprocessors have become available, the bus has evolved, and today 8-bit and 16-bit machines are on single boards.

If the STD bus evolves further, it may be through the use of the DIN connector, whose 96 pins would provide an additional 20 over today's STD card. Then if true plug compatibility could be maintained between 76-pin and 96-pin systems, the market could be wide open for the STD bus into the '90s. As it stands, it may meet some serious competition from Multibus II and VME.

One company that already has a large foothold in both the industrial and the commercial market is Digital

Equipment Corporation. At present fighting battles on all sides, from the personal computer division to its VAX product sector, it seems certain that DEC will have to make some radical changes to its product line to survive.

A spokesman for the company would make no comment about the industry-wide rumors of the BI bus, predicted to be DEC's upgrade to the Q-bus, but it is certain that a new bus structure is needed for that end of DEC's business to fight off the Multibus I and II and the VME bus. Putting the Micro-VAX I onto the Q-bus must only be a stepping stone towards another bus structure more suited to high performance systems.

As time to market becomes increasingly important, the flexibility of advanced computer bus structures will play a vital role. Currently the Multibus and VME bus have both taken a sophisticated systems level approach to the problem of computer design. Time will tell whether DEC's BI bus or the Texas Instruments NUBus take the same approach.

Graphics Systems

Developments in graphics systems have been primarily in four segments of the field: processors associated with graphics, displays, peripherals and input technology.

Over the course of 1983, several trends appeared for processors associated with graphics displays. One prevalent trend was the continued growth in the use of graphics chips, with NEC's 7220 (second sourced by Intel) in the lead. Other products of import for graphics processors were the new generation of multiplier chips from producers such as TRW and the new 29016 family of bit slice processors from AMD.

However, over the long term, the demand for speed will require a shift to semi-custom or custom logic. One of the problems hindering the implementation of graphics function on silicon is the relatively low quantity of devices in demand. Until quantity increases, manufacturers of high-performance systems will continue to build custom processors from ECL and PAL logic, causing cost to remain high.

Another reason for the high cost of graphics processors is the need for fast semiconductor memory. Because the



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large amounts of data manipulated for displays must be processed quickly, typical RAM configuration are not sufficiently fast for graphics. While 1984 will see wider use of 256K RAMs, the first implementation will be for CPU/software memory. Newer 64K RAMs with 4 x 16 bit data paths will assist speed, and more manufacturers will apply 16K static RAMs for higher performance.

Display manufacturers again showed products with increased capabilities. However, several sources have questioned the ability of producers to supply devices shown at trade shows in large quantities.

While several systems were shown with 1280 x 1024 resolution and 64 Hz refresh rates, the majority of systems are well below this. Nevertheless, 1984 will see several monochrome systems with resolutions approaching 2000 x 2000 and color with a displayable resolution of 1500 x 1200.

An increase in the use of color flat panel devices such as vacuum fluorescent and liquid crystal is likely, but primarily in instrumentation. Both color for electroluminescent and plasma suitable for graphics display are foreseeable, but not in the near term. High-resolution plasma displays such as the 1024 x 600 display from Sony, are likely to be found in new portable computers. Flat CRTs produced by both Sony and Sinclair of Great Britain are in wide commercial use for television and may appear in computers for alphanumeric display during the year.

There has been a resurgence in monochrome systems from makers such as Apollo, Sun, Symbolics and others. Most of these have also been seeking to support color, so these monochrome systems probably won't change the trend towards color workstations for all applications. One trend that will emerge during the next year is that new display tube sizes, notably 15 and 12 inches, will be offered by system integrators.

There have been advances on several fronts for graphics hardcopy. One of the most important was the release of a host of plotters for under \$1000 with remarkable quality. In with newer pen technology (faster ink, better tips) these small plotters offer users the ability to produce overhead transparencies and

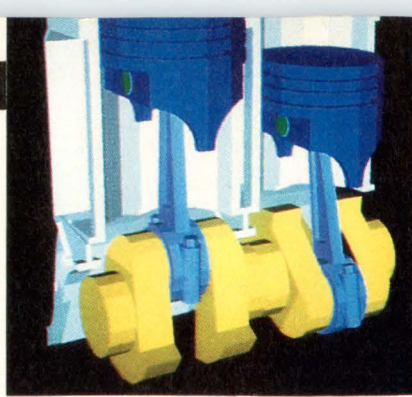


Photo courtesy GE CAE International

printed charts with solid surfaces.

The integration of microprocessors into plotters at all cost levels means that, for the first time, the type produced is publication quality, even on the smaller devices. Features such as the ability to work with multiple color pens have also benefitted from increased intelligence.

Color cameras have improved on all fronts with 4000 x 4000 line resolution from Matrix, and a 64 Hz interface on the Modgraph camera. On the low cost end, Poloroid introduced a 1300 camera that offers the lowest priced camera system available.

Electrostatic technology, long seen as stable, was shaken by Versatec's announcement of a color printer capable of near-photographic quality large format images.

Thermal technology has appeared in Seiko and Sony systems; the former has been more successful in graphics applications. The Seiko device has grown in popularity since its introduction and is likely to compete widely for the fast and cheap hardcopy market in 1984.

Ink jet systems from Printacolor, ACT, Diablo and Tektronix also received wide attention as having solved the maintenance problems long associated with the technology. Algorithms for interpreting and driving the jets made noticeable advances throughout 1983, and 1984 should see the output from devices under \$5000 approaching photographic quality.

1983 held few surprises in input, but some notable advances were made. The first is the decreasing cost of scanners such as those shown to capture halftone images from Xerox and Panasonic. A related announcement came late in the year from Wang Laboratories, whose desktop system provides office users with a scanning technology to capture images for storage and transfer via the company's network.

The graphics tablet is becoming merely a cursor controller, with more

tablets used for workstation operation. Mouse technology has been effected by the introduction of optical mice, but it remains to be seen whether the mouse will play a major role in system interaction.

While joysticks remain popular as cursor controllers, they seem to be used less in lower performance systems. Less known devices such as the touch pad have proven less than popular, and others such as the trackball retain their limited applications markets.

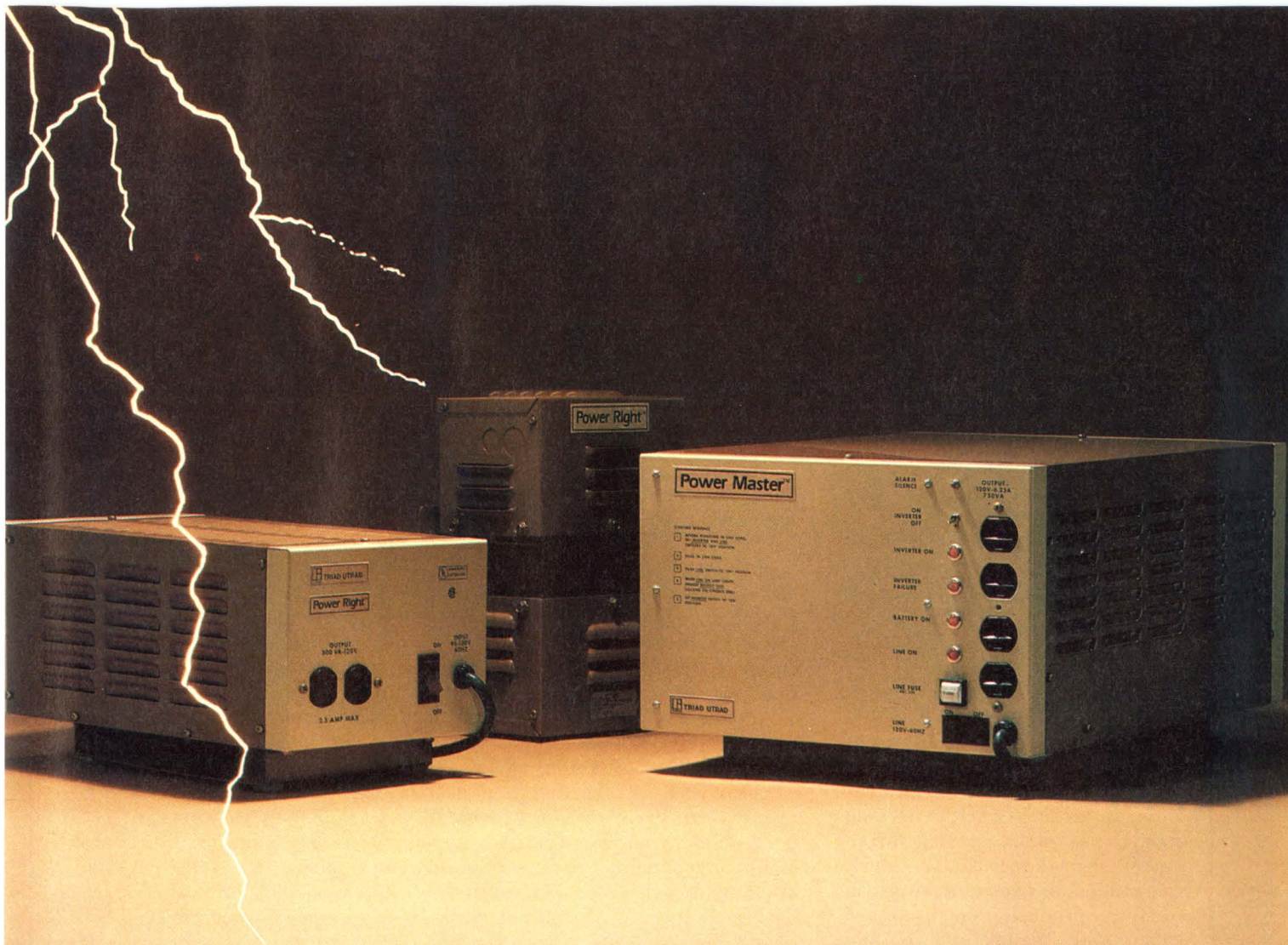
In graphics systems, high-end manufacturers will continue to add capability to remain ahead of the larger marketplace in low cost applications in the office and for consumer electronics. Workstations, especially for engineering and design applications are making a shift from 16 bit to 16/32 and 32 bit systems and 1984's trade events will see the 16032, 68010/68020 and iAPX 386 being implemented in demonstration models.

Hewlett-Packard will continue to increase performance and capability of its 9000 line under the 600 series. HP has purchased the right to certain products such as a graphics board from Metheus, but 1984 may see further enhancements to the system from HP itself. The most significant HP announcement will no doubt be the price cut for this system. And the market segment for higher performance workstations long dominated by Apollo will be more competitive with entries from Sun, Symbolics, ICL/PERQ, Masscomp and Ithaca Intersystems, as each increases performance.

Mass Memory

In mass memory, 1983 was year of innovation; in 1984, those innovations will be tested in the marketplace. The test increasingly will be one not only of performance, but of reliability, serviceability and field support, and of high-volume, on-time delivery.

Most severely tested by these factors will be Winchester disk drives. Winchesters are considered weak links both in the design stages of a system and in the final system itself. During design, late deliveries can hold up production, as can spec variations. In the final system, Winchester malfunctions are a leading cause of system down-time. Many innovative new products enjoyed success in 1983 based on their high



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performance. Their continued success in 1984, however, will be based more on their companies' performance—their ability to deliver the products as promised and service them as needed.

Many companies are betting on the popularity of half-height micro-Winchesters in 1984. Seagate's ST212 is indicative of this trend, as is the proliferation of small companies announcing high-performance half-heights. Sub-micro-Winchesters (with platter diameter less than four inches) will develop more slowly, in direct proportion to the development of their chief potential market, portable computers. Seagate is leading an effort to standardize media for sub-micro drives, but have yet to announce a product (in all likelihood, they will in 1984).

More plated media and thin-film heads will be available in 1984, but demand will continue to exceed supply. Delays in meeting these demands are due to the enormous cost of setting up production facilities. These costs result not only from initial equipment investment, but from the need to laboriously refine production techniques to deliver a uniform product in high enough yields to make the operation profitable. Still, a number of new companies are gearing up for production in 1984, and many disk drive manufacturers will produce some of their own media in-house to help alleviate the shortage.

Only one company—Appied Information Memories (Milpitas, CA)—has announced a vertical-recording Winchester drive for 1984, but considerable amounts of effort and money are going into development of the technology at a number of companies. Most see vertical recording not as a flash-in-the-pan technology, but as an inevitable next step in the evolution of high-performance disk drives. Many are enticingly close to having a marketable product, and this is one area in which we may see some surprise announcements in 1984, for products to be delivered in 1985.

As is the tradition, flexible disk technology is a step ahead of small Winchesters. Half-height floppies are already shipping in large quantities, sub-4" drives have already reached the point where a number of companies are arguing over a standard, and a vertical-recording product is scheduled



Photo courtesy: Priam Corp.

for shipment (of evaluation units) in about a month.

While flexible disks hold down the low end of Winchester back up, various types of tape drives (cassette, quarter-inch cartridge, and half-inch) will divide up most of the middle- and high-end. Increasing availability of media (thanks to a number of manufacturing and second-source agreements), interface and format standardization (notably the QIC quarter-inch cartridge standards) and even lower costs per byte (already, tape is the cheapest mass storage medium) will boost tape drive's popularity in 1984.

Another 1983 innovation that must prove itself in 1984 is the optical disk drive. Introduced by Optitem, a division of Shugart, the optical drive offers extremely high capacity (a Gbyte per disk side) at a low cost per byte. Its ability to gain market acceptance will affect not only the future of Optitem, but also the future of a number of other optical disk products at a variety of companies, each waiting to see how the Optitem product fares.

For the mass memory industry, 1984 will be a pay-off year. In 1983, many system designers were impressed enough with the new generation of high-performance mass memory offerings to evaluate them. 1984 will show whether or not they are now impressed enough to design with them.

Semiconductors And IC's

The phenomenal increase in the density of integrated circuits over the past ten years has presented the IC houses with the problem of putting VLSI devices into increasingly smaller packages.

Advanced bus structures, such as VME and Multibus II compound the issue, since their size constraints will limit the number of equivalent DIPs that may be placed on a board. Both Motorola and Intel have taken steps already to solve the problem. The 286 and the 68000 are both currently available in leadless Chip carrier Formats. Motorola, for its part, has also made its MPU available in a Pin Grid Array

providing up to 100 pins in about one third the space of a traditional DIP package.

But it is not only the processor companies that are involved. NEC (Mountain View, CA) this year announced its 1Mit CMOS ROM in a 52-pin flat-pack, and TRW made its 16x16 parallel multiplier available in a 68 contact leaded or leadless chip carrier.

Many designs have already taken advantage of the new packaging technology. Force Computer, for example, has a VME-based product out on the market (their CPU-2) that not only uses the 68000 in a pin grid array, but also makes use of SIP RAM technology as well. SIP's have been around for a long time, and have in the past mainly found use in shrinking passive component density. Allen-Bradley, for example, have a wide range of standard circuits and ohmic values in 6, 8, or 10 pin packages. Recently, however, active components, like RAMs have been reaching the market from both custom and the IC houses. Okj Semiconductor, for example, offers 64K x 4 SIP RAMs.

As processors shrink due to packaging, so their power consumption is being reduced by the use of CMOS; and this is true not only in 8-bit designs. Harris Semiconductor, for example, announced the CMOS version of Intel's 16-bit 8086. CMOS processors, however, must be supported by the appropriate glue logic, memory, and gate arrays to enable the designer to put together a system. This year saw a rapid increase in the number of available ICs that should continue unabated into the nineties. National Semiconductor is pushing CMOS hard, as is Texas Instruments with its Lin CMOS telecom circuit range. LSI logic and International Microcircuits have also continued their commitment to CMOS gate array processes. Perhaps more importantly, however, it looks as though gallium arsenide may finally be coming out of the lab and into the commercial world.

Although many discrete packages are already on the market, the next few years should see the first SSI devices, such as latches and flip-flops. The future promises devices such as memory in LSI giving the mainframe designer a power of ten speed improvements over conventional silicon devices. □

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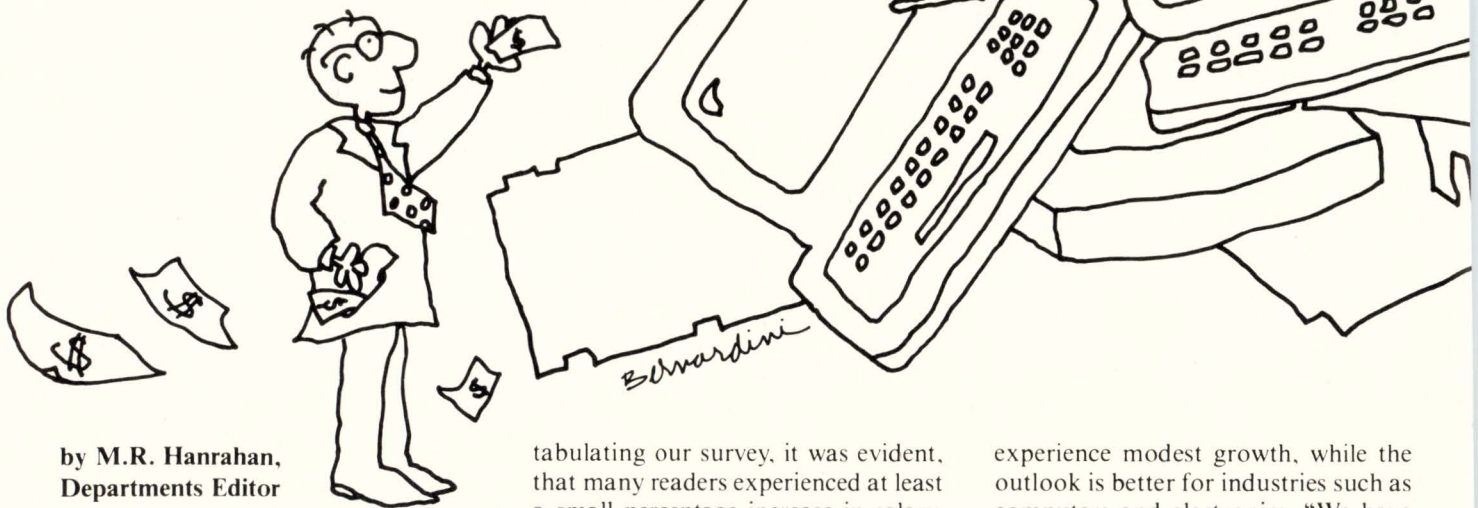
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1983 Salary Survey and Employment Trends

An increasing hope for the industrial sector resides not only in the continual modernization of plants and equipment, but in a new emphasis on employee satisfaction.



by M.R. Hanrahan,
Departments Editor

There are several factors surrounding job satisfaction and longevity in the electronics engineering and computer design fields. Challenging state-of-the-art projects put an emphasis on technological sophistication and universal importance of products. An engineer's involvement in projects such as these is obviously rewarding. However, there are simpler top priority needs which determine job satisfaction.

Digital Design's 1983 Salary Survey represents a diverse cross-section of age, educational background, job function, and geographical locations. In

tabulating our survey, it was evident, that many readers experienced at least a small percentage increase in salary, however salary freezes and job lay-offs also characterized the '83 employment curves. Yet in light of the current economic rebound, salaries and job mobility should be on the upswing.

Economic Factors

The U.S. faces a consumer-led economic recovery during 1983-84, but high real interest rates will keep real growth modest — at a level of about 2.25%. According to 3M Corporation's corporate economist, John McDevitt, industries sensitive to interest rates, such as automotive and housing, will

experience modest growth, while the outlook is better for industries such as computers and electronics. "We have shifted from an industrial/production economy to an information/communications/service economy, and that has implications for every region of the country."

Hope for the industrial sector may reside in the economic program passed in 1982, which encourages modernization of plants and equipment. This coming reindustrialization will restructure the U.S. economy through greater productivity improvements. "Unemployment can be expected to remain at higher rates than we would like," remarked McDevitt, "while skilled

labor will become harder to find.”

Factors that could cloud the picture of modest growth include the electronics industry's move toward protectionism. Restrictions on imports, McDevitt said, could result in retaliation and could damage jobs and industries, and abort the expected business upturn. The 1983 unemployment levels are expected to ease, but slowly. Continuing corporate costs weigh heavy despite lower inflation, lower prime rate lending, more housing opportunities and overall consumer confidence.

Two basic unemployment trends were evident in 1983. Almost half of those jobless in the electronic industry fall into the category of structural or dislocated unemployment. Employees laid-off never return to the job due to basic shifts in the U.S. economy based on changes in science, technology, and domestic and foreign competition. Others are temporarily unemployed due to the recession cycle only. It is projected that the mid-80's will witness a return to full employment based on a 5-7% jobless rate.

Survey Profile

The 1983 Salary Survey is based on a random 1000 responses to the survey questionnaire bound into the July '83 issue of *Digital Design*. Of the total respondents, 40% are involved in the design and development of computer-related products sold by their company. Another 30% are involved in the design of products utilized within their own company, while 16% list both functions and 3% are third-party systems designers.

Only 2% of those surveyed are part of corporate management. Engineering management comprises 14%, and

Participants Current Annualized Salary	
Salary	Percent
\$11-15K	.7%
\$16-20K	2.2
\$21-25K	8.2
\$26-30K	24.4
\$31-40K	38.1
\$41-50K	18.6
Over \$50K	7.6
Total-998	

the largest percentage, 64% are engineers at various design levels. R & D personnel represent 14% of the survey and 1% of the respondents are in marketing management.

The largest percentage of participants, or 37%, are in the 30-40 year-old range, followed by 25% who are 25-30 years old, and 19% are between the ages of 40-50. Those over-50 total 9% and only 1% are over 60.

Of the participants representing various regions in the survey, 30% are from the Northeast, 11% from the Southeast, 19% from the Midwest, 5% from the Northwest, and 35% from the Southwest.* No responses were received from the states of Wyoming, Alaska, South Dakota, and Maine.

*For tabulation purposes, respondents were grouped into five regions as follows:

- Northeast = CT, DC, MA, MD, NH, NJ, NY, PA, RI, VT, ME, DE.
- Southeast = AL, AR, FL, GA, KY, MS, LA, NC, SC, TN, VA, and WV.
- Midwest = IA, IL, IN, KS, MI, MN, MO, NE, OH, OK and WI.
- Northwest = AK, CO, ID, OR, UT, WA, WY, and MT.
- Southwest = AZ, CA, NM, NV and TX.

After July ('83) salary freeze I was compensated with substantial 18% raise!

—Test Equipment Design Engineer

For the last 3 quarters, my division has required a mandatory 48-hour work week for all exempt employees.

—Project Engineer

After averaging almost 10 years at each previous job, my present employer recently had an “economy” cut-back that eliminated all over-50 engineers . . . management must realize the stupidity of age discrimination.

—Engineer, System Design

In 1982 I received a 10% increase, in 1983 my 3% increase represents a loss of spending power.

—Manufacturing Engineer

What recession????

—Video Design Engineer

Our company has not given any raises since June '81.

—Engineer, Control Systems Design

My salary has tripled in the last 6 years.

—Sr. Software Engineer/Project Leader

	Salary vs. Job Function							Total
	\$11-15K	\$16-20K	\$21-25K	\$26-30K	\$31-40K	\$41-50K	Over \$50K	
Corporate Management		2		2	4	7	7	22
Engineering Management	2	1	1	10	49	51	26	140
Engineering	3	11	64	192	251	93	24	638
Marketing Management				3	7	2	2	14
Research & Development	2	2	11	29	53	28	14	139
Other		6	6	6	13	5	3	39
								Total=992

Education

Engineering salaries are somewhat influenced by educational experiences, but only to the extent that these visibly contribute to present performance or have realistic potential to contribute to future assignments. It is not unheard of in the engineering field to advance on practical knowledge gained through work experience rather than placement by degree earned. However, a B.S./B.A. is still considered necessary for advancement.

Over 50% of the survey respondents hold a B.S./B.A. degree and 23% went on to get an M.A./M.S. degree. M.B.A.s represent 2% of the survey and 4% have received doctoral degrees.

Sixty percent surveyed received their degree in electrical engineering, compared to a 12% Computer Science degree response, and mechanical engineering and physics each had a 5% response. The emphasis placed on engineering education has left the realm of theorist and entered the world of practitioners. Engineering graduates are more inclined to join short-term product projects rather than engage in long-term research.

Esquire Magazine, in a May 1983 article entitled "The Mass Production of Engineers" charted this trend as a response to the mood of the times. Students are now focused on getting the degree and going to work with financial rewards forefront in their minds. The public sector is worried about reviving a declining industrial base. Funding for many of the engineering programs comes from major corporations — Xerox, Exxon, ITT, General Motors — which hope to benefit from the results. In the meantime, the need for long-term research and theory development is an important concern.

The question is whether universities' engineering programs can afford to support all concerns at a time of shrinking resources and rising enrollment pressures. The surge is creating serious stresses in the educational system.

Projected Shortages

The American Electronics Association (AEA) forecast an annual shortage of nearly 23,000 EEs and computer scientists for the years 1983-87. In its report, "Technical Employment Projections,

Education vs. Salary								
Salary Highest Degree Earned:	\$11-15K	\$16-20K	\$21-25K	\$26-30K	\$31-40K	\$41-50K	Over \$50K	Total
No college	1		4	6	5	4	4	24
Under two years of college	1	5	6	5	11	4	1	33
Two years of college or more (but no degree)	1	2	10	27	22	9	4	75
Associate degree		7	9	24	13	6		59
B.S./B.A. degree	2	6	50	145	200	73	28	504
M.A./M.S. degree		1	2	30	101	70	21	225
M.B.A. degree	1			2	9	8	3	23
Doctoral degree				1	16	11	12	40
Other (not listed above)	1		1	4	4	1	2	13
Total=996								

1983-1987", the AEA surveyed 815 companies, employing a 370,881 person technical workforce at the end of 1982. After tallying the returns, it projects that by 1987, the demand for EEs and computer scientists will reach 197,662.

Teaching positions in electronics and computer science programs are vacant due to the inability of universities to compete with the salaries offered by industry. *Esquire* cites California's San Jose State University, where an EE graduate going into industry with a B.A. can make up to \$6,000 more than a professor with a Ph.D., resulting in 40% of the faculty jobs left unfilled.

Those who have been out in the field for some time are also facing gradual obsolescence of their training and must supplement their knowledge with continuing education programs. One such program that addresses this problem is Northeastern University's State-Of-The-Art Engineering Program. Older engineers wanting a career transition are realizing the need to upgrade skills and knowledge. Recent graduates turn to continuing education programs to increase their marketability in very specific areas.

The challenge to educators was recently stated in the U.S. Senate's

Morrill Technology Act: "The future international industrial competitive position of the U.S. depends on maintaining U.S. scientific and technological leadership, increasing the rate of innovation, and increasing the productivity of our basic industries, all of which require a well-educated, motivated, and technologically proficient work force."

Job Security

Despite the economic constraints of the last 16 months, 80% of the survey participants received some sort of salary increase in 1982/83. In avoiding employee lay-offs, corporations instituted across-the-board freezes resulting in 17% of total participants receiving a salary freeze, 2% experienced a cut-back in salary, and less than 1% were actually laid-off.

Mobility

The apparent mobility found in engineering is supported by the phenomenal employee migration from company to company. Over 50% of the respondents have been with their present employer between 1-5 years, and 55% had been with their previous employer 1-5 years. Considering that most respondents fall into the 30-40

Salary vs. Age								
Age	\$11-15K	\$16-20K	\$21-25K	\$26-30K	\$31-40K	\$41-50K	Over \$50K	Total
20-24	2	5	23	43	7			80
25-30	1	10	30	96	94	8	5	244
30-40	2	5	25	72	176	67	24	371
40-50		1	4	21	69	71	22	188
50-60	2			9	25	32	20	88
61-65				3	8	5	2	18
Over 65					1	1	2	4
Total=993								

year-old range, it can be assumed that the length spent at each employer lengthens with age and experience. Regarding long-term employment with only one employer, 6% had been with their company 15-25 years, and 2% had been at the same company for over 25 years. It is interesting to note that 22% had been with their previous employer less than one year. Job switching in the EE and computer design fields is acceptable, and at times recommendable, considering the life-spans of technology related operations. Of those respondents in supervisory positions, less than 1% supervised over 100 employees, while 49% did not have any supervisory responsibilities, and 48% supervised between 1-10 employees.

Job Functions And Salary

When comparing salaries to job functions, those paid the highest salaries fall under engineering management. In the over \$50K range, 26% are engineering managers. At the engineering level, 24% are in the over \$50K range. However, the bulk of the responses were received from engineers whose salary is between \$30-40K. The next largest group, 19%, are engineers in the \$26-30K range.

Age vs. Salary

The comparison of the age to the salary found the largest percentage of respondents are 30-40 years old and are in the \$31-40K salary range. Of the 993 total responses, the extremes included 7 of the 20-24 year-olds are in the \$31-40K range and 24 of the 25-30 year-olds are in the over \$50K category. Most 25-30 year-olds are in the \$26-30K category representing 24% of the whole.

Regions

Regional break-outs of salary clearly indicated those with the highest median salary are in the "technology centers" such as Silicon Valley and areas surrounding Boston and Northeastern New England. In determining a median salary range for a region, the total number of participants were divided in half with an equal number above and below the middle salary value.

Of an approximate 30% response from the Northeast region, 10% are in the \$31-40K range constituting the bulk of participants. This value is surrounded by 7% in the \$26-30K range and 6% in the \$41-50K salary range. The Northeast is definitely centered in the high-tech area surrounding Bos-

We've just experienced about 40% lay-off/transfer, but are starting to gear up for a new program.

—Sr. Engineer/Computer Design

Lay-off just meant an opportunity to get a better job with a good raise.

—Program Manager

ton, with the State of Massachusetts garnering the highest salaries and most participants. Roughly 2% or 21 participants make over \$50K in a region where job mobility, start-up opportunities, and research facilities are abundant.

The Southeast region is a developing area with the "research triangle" area of North Carolina, Georgia and South Carolina. The median salary is \$31,000. Of the 112 participants from this region, 3% are in the \$26-30K range, with the bulk of respondents in the \$31-40K range. The Midwest showed the lowest median salary at \$30,500 and a relatively high percentage in the \$16-20K salary range.

The Southwest including the state of California and its Silicon Valley predictably included the most respondents and the highest salaries. The \$34,250 median salary of the total 358 respondents is surpassed by 70 participant's \$41-50K salaries and 37 in the over \$50K category.

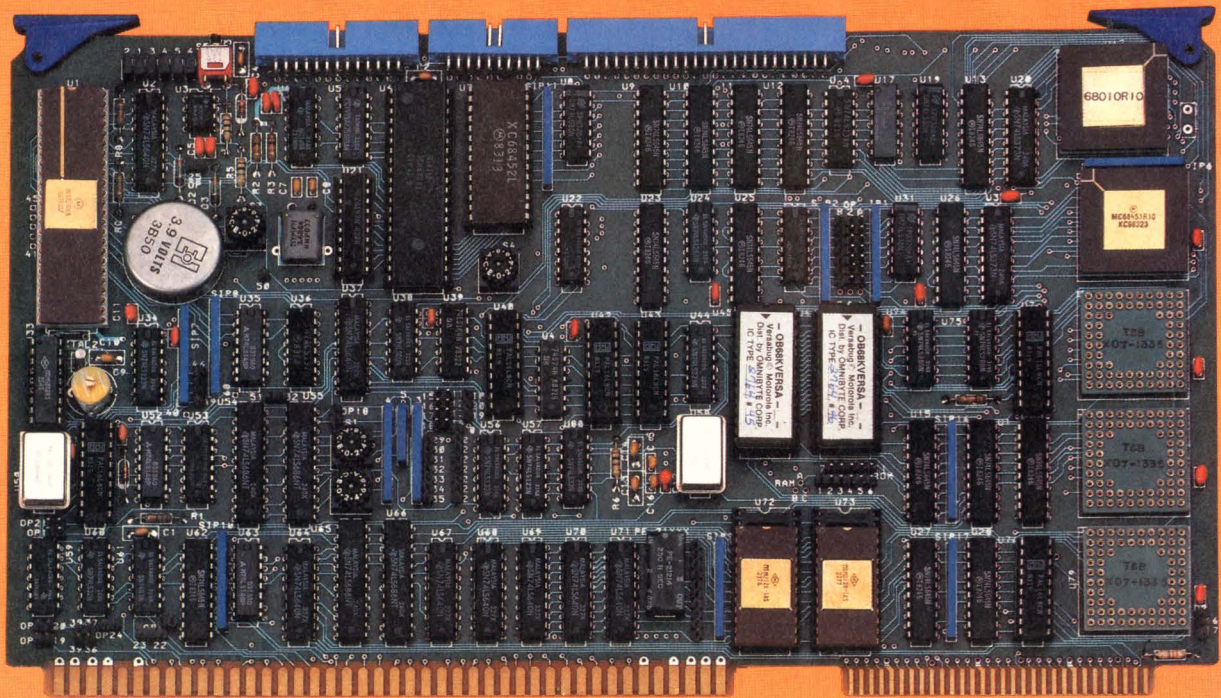
Summary

In surveying the 1983 salaries and employment trends in the engineering and computer design fields it is evident that the recession and economic hardship of 1983 did not have the devastating effects on this industry as it did on other sectors. With an emphasis on education and the job mobility allowed EEs, a high demand for technical professionals will continue throughout the 1980s. □

Regional Salaries									
Salary	\$11-15K	\$16-20K	\$21-25K	\$26-30K	\$31-40K	\$41-50K	Over	Total	Median Salary
							\$50K		
Total = 987									
Region									
Northeast	2	3	18	70	101	56	21	271	\$33,000
Southeast	1	1	12	29	42	20	7	112	\$31,000
Midwest	1	13	22	51	64	26	9	186	\$30,500
Northwest	1	1	6	14	27	9	2	60	\$33,000
Southwest	1	4	21	79	146	70	37	358	\$34,250

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OB68K/MMU™



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The OMNIBYTE OB68K/MMU is a Central Processing Unit (CPU) that has been designed specifically for use in larger memory-managed computer systems. Although, without making use of the MMU capability, this computer may be used as a normal fixed memory mapped microcomputer. Special attention has been given to fulfilling the needs of modern operating systems.

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Features include:

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- ★ Prioritized 8-channel DMA port with address translation
- ★ Realtime Calendar Clock with battery backup
- ★ Two 28-Pin RAM (4K Bytes) standard/ up to 16K Bytes optional
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- ★ Flexible 68230 parallel input/output 24-bit timer circuit
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- ★ Multi-Processor bus arbitration
- ★ Optional VERSAbug terminal monitor/debugger firmware program
- ★ IEEE 796 BUS compatible
- ★ Compliance-MASTER D16 M24 I16 V02L
- ★ A two year limited warranty

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Multibus II — A Top Down Approach

The Multibus II bears a great deal of resemblance to its predecessor Multibus I.

by David Wilson, Technical Editor

A system's integrator working with board level products is faced with a disheartening set of compatibility problems. These problems have arisen because the evolution of bus-related cards has haphazardly grown out of the availability of low-cost microprocessors and support circuitry from the IC houses. Early busses simply mimicked the pin-out of a specific processor, timing varied between cards from different manufacturers, and no thought was given to how the busses would evolve over time to fill the needs of the designer.

Indeed, many design attempts to put newer microprocessors onto old bus structures resulted in subsets of the old bus. As a result, the only claim to compatibility lay in the size of the card and the number of pins on the connector.

Intel's Multibus fared well in these early days, primarily due to its ability to support newer generations of VLSI products as they became available, without kludging. From an initial support of

8-bit machines, Multibus boards are available today that support the 8086, 286 and 68000 processors. Although it may have been a stroke of luck that Intel chose 20-bits of addressing initially (on P1), then dedicated 4 more pins (on P2) to allow for 24, today the Multibus is one of the most popular busses in the marketplace, and over 1,000 boards are available for the designer to choose from.

As the success of the Multibus grew, Intel continued to enhance its architecture. This year (*Digital Design*, February, 1983, p. 76) two additional bus structures were added (the iLBX bus and the Multichannel I/O bus) to meet the need for higher performance systems designs.

As their Multibus product line continues to gain a large proportion of market-share (comparable only to Digital's Q-bus), many manufacturers have expressed concern with the old problem of finding themselves trapped in a market niche due to the limitations of their bus. This was specifically brought home by the joint announce-

ment of support for the VME bus by Motorola, Mostek, Signetics and Thompson — CSF. The VME bus appeared to many to be the panacea for the '80s, addressing problems in the high-performance area such as CAD/CAM and robotics where designers are pushed for loss of computing power and memory addressing space on conventional busses. A 32-bit address and data path coupled with the DIN Euro-card standard offered a serious viable alternative to the Multibus I. Understandably, Intel's answer was to produce an evolutionary growth path for the Multibus I, which it has done with the recent introduction of Multibus II.

The architecture of Multibus II bears a great deal of resemblance to its predecessor. It consists of the parallel system bus (iPSB), the local bus extension (iLBX II), the serial system bus (iSSB), and the iSBX I/O expansion bus and the Multichannel DMA I/O bus (Figure 1).

While the Multibus I interface pioneered the multiple bus approach, the Multibus II system architecture has refined it and extended its range, both at the high and low end. Each multiple bus structure is tailored for a particular purpose. This is part of a design philosophy called "functional partitioning," a modular design approach that entails breaking an overall problem into manageable pieces based on function. For

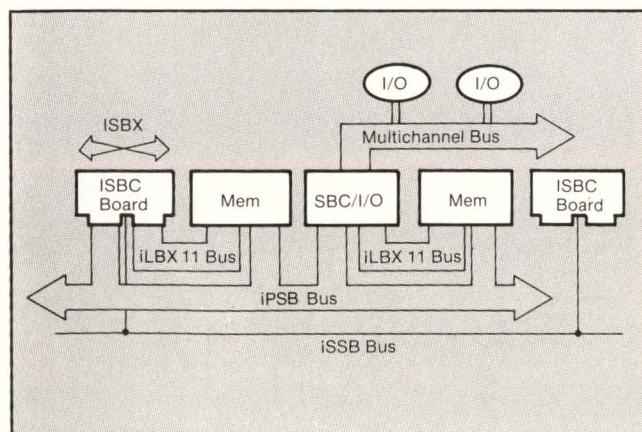


Figure 1: Multibus II System Architecture.

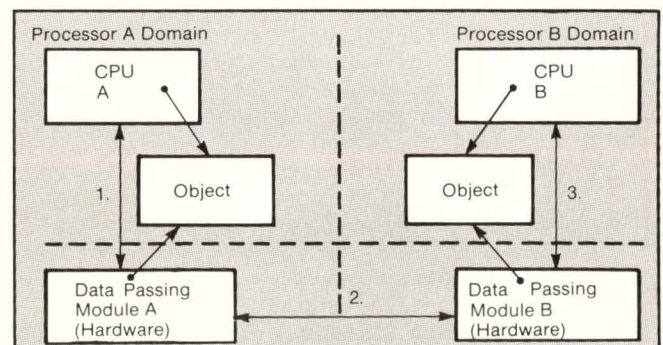
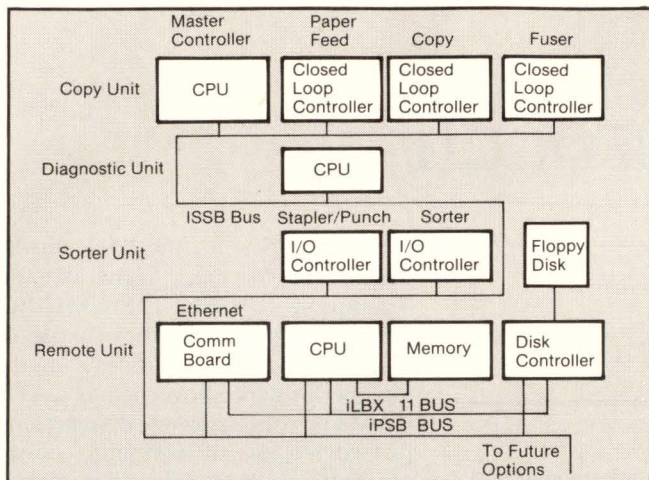


Figure 2: Multibus II Message Passing. 1. CPU A requests transfer of object; 2. Data Movement is negotiated; data movement is independent of either processor; 3. Processor B assigns memory for object and is signaled of object availability.

Multibus II



example, typical microcomputer system functions are processing, mass storage, communications and graphics.

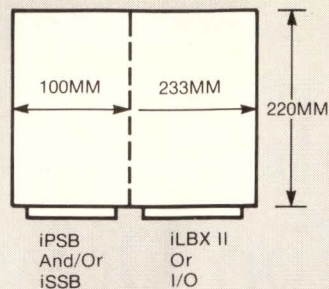
In typical functionally partitioned systems, data movement between modules is minimized. Requests for data movement between modules is kept to a minimum and critical real-time data is kept to the local environment. Once the modules have been defined, they are implemented by optimizing each for its specific requirement. The Multibus II system architecture defines standard interfaces between each functional module and tailors each interface to its specific function. For example, the parallel system bus (iPSB bus) is optimized for interprocessor communication and data movement. The local bus extension (iLBX II bus) is similarly optimized for high

▲ *Figure 3: iSSB bus used in a photocopier design.*

► *Figure 4: Form factor, connector and PC board dimensions.*

speed execution. And the serial system bus (iSSB) is optimized for low-cost interprocessor communication, allowing the designer cost-effectiveness over a wide range of configurations.

The iPSB supports four address spaces: a 32-bit wide memory address space, a 16-bit I/O address space, a 16- or 32-bit message address space and a 16-bit interconnect address space. Data



- 79.6 Sq. In. (Multibus I 81 Sq. In.)
- Optional Single Connector Size

Connector

	Multibus I	Multibus II
Pins/Spacing P1	86 @ .156	96 @ .1
P1	60 @ .1	96 @ .1
Insertion Force P1	54 Lbs. Max.	19.8 Lbs. Max.
P2	36 Lbs. Max.	19.8 Lbs. Max.
Extraction Force P1	2.69 Lbs. Min.	3.24 Lbs. Min.
P2	1.94 Lbs. Min.	3.24 Lbs. Min.
Current Capacity	3 Amps/Contact	1 Amp/Contact
Contact Resistance	10 mΩ Max.	20 mΩ Max.

P.C. Board

	Multibus I	Multibus II
Board Size	12.00" x 6.75"	9.177" x 8.651"
		3.94" x 8.651"
Board Area	81 Square Inches	79.4 Square Inches
16 Pin IC Capacity	160	160
Connector Style	Card Edge	2 Piece
I/O Pins P1	86	96
P2	60	96
+5V Capacity	24 Amps/Board Max.	14 Amps/Board Max.

is clocked at 10 MHz and can be up to 32 bits wide. It has a burst transfer capability (similar to Digital Equipment's block mode transfer on the Q-bus) that can yield a maximum sustained bandwidth of 40 Mbytes/sec. The burst is implemented as a single address cycle followed by multiple data transfers which maximize bus bandwidth.

Test Board For The Bus

A single board design aid for the Multibus has recently been introduced by Zendex (Dublin, CA). Priced at \$565, the ZX-906B, provides nine latching hexadecimal displays that display 20-bit address and 16-bit data values as they occur on the bus and selects the bus cycle type for the values to be displayed. An 8/16 bit selector switch blanks unused portions of the display to present simple readouts. The ZX-906B's FAST/LAST selector switch allows the user to lock the first or most recent activity occurring on the Multibus. This feature can be used as a test point and to trigger an oscilloscope or a logic analyzer. An XACK transfer acknowledge momentary contact switch lets the user single-step through programs.

Write 301

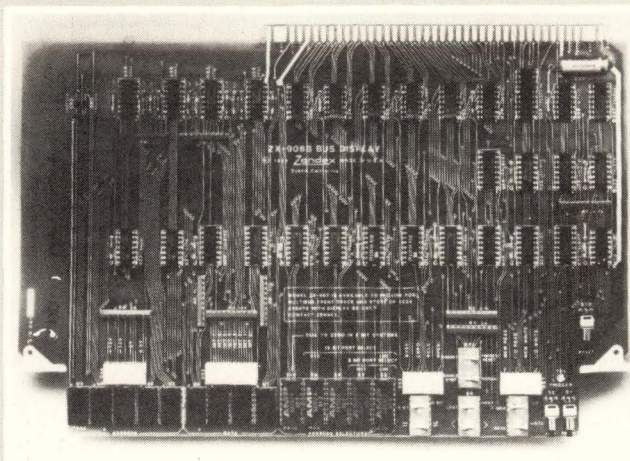


Figure 1: The ZX-906B from Zendex Corp.

CPU Features Dual Bus Addressing

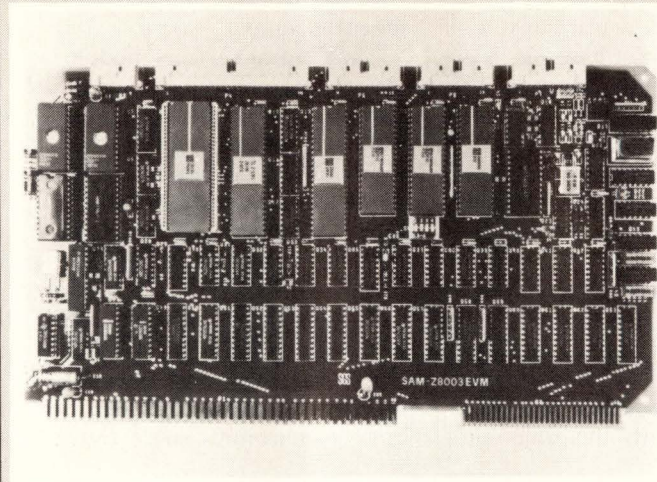


Figure 1: The SAM-Z8003EVM evaluation module, virtual memory capability with a Multibus format.

One late entry into the Multibus I marketplace came from SGS Semiconductor Corporation (Phoenix, AZ). Its offering comes in the form of three boards — an evaluation module, a virtual memory processor board and a dual-ported RAM memory board. As others have done in the past, SGS has defined some of the pins on the P2 connector for its own use (**Table 1**). Dual-bus addressing is a SGS unique feature that allows simultaneous access of the memory bank by either Multibus P1 or the SAM-Bus on P2. The Z8003VMP Virtual Memory Processor Board features the Z8003 processor and the Z8015 paged memory management unit, as well as RAM, EPROM sockets, serial and parallel I/O and priority interrupt-logic. Designed to be integrated with the processor board, the memory board incorporates parity checking that will detect any single bit errors, optionally generating an interrupt. The CPU can then read the input parts to determine which physical address generated the error.

Write 300

P1 - Multibus compatible meeting all IEEE 796 standards including 24-bit addressing.

P2 - Private Processor Bus with buffered signals, pin assignments are as follows:

PIN	SIGNAL	DESCRIPTION
1,2	GND	Signal Ground
3-18	DATA0-15	DATA BUS
19	PFIN	Power-fail Interrupt (Multibus standard compatible signal)
20	BAS	Buffered CPU Address Strobe
21	BDS	Buffered CPU Data Strobe
22	BR/W	Buffered CPU Read/Write
23	BB/W	Buffered CPU Byte/Word
24	BN/S	Buffered CPU Normal/System
25-28	BSTO-3	Buffered CPU Status Lines
29	BTCLK	Buffered TTL CPU Clock
30	DBUSY	Device Busy, Request for Wait (Multi-bus standard compatible signal)
31-54	ADR0-23	Address Bus
55	A22	Multibus address ext-line
56	A23	Multibus address ext-line
57	A20	Multibus address ext-line
58	A21	Multibus address ext-line
59	PE	Parity Error
60	MC	Memory Command (Memory access on P2)

P4 - Unbuffered Processor and PMMU Bus (top edge connector).

Table 1: SGS's pin definitions.

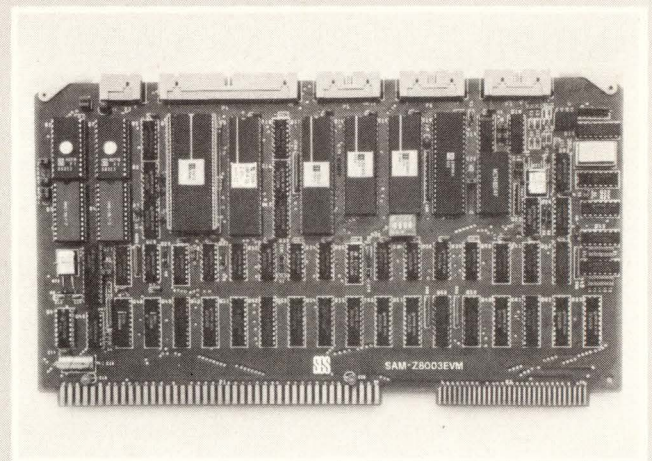


Figure 2: The SAM-Z8003 EVM (Evaluation Modules).

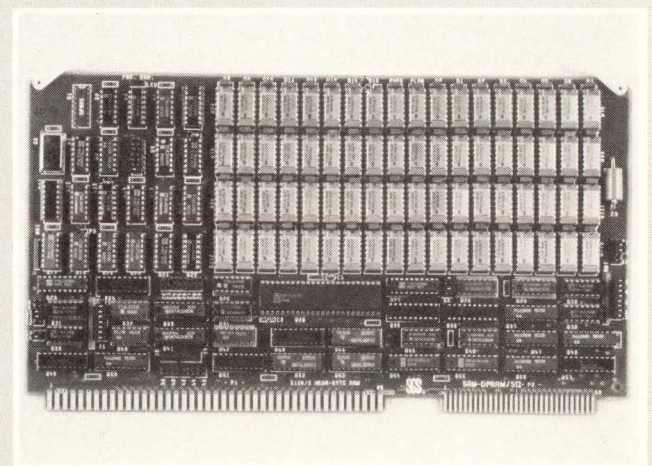


Figure 3: The SAM-DPRAM (Dual-Port Ram).

Message passing is a very important attribute of the parallel system bus (iPSB). Intel's objectives were to define a standard interface for multiple processor systems, to provide high-performance support of functional partitioning and to ensure software compatibility on both the parallel and serial bus.

The iPSB bus method of message passing provides the facility for moving data from one functional module to another without the worry of memory management or synchronization problems at the bus interface. This is achieved by data passing modules that will be implemented in VLSI on each of the functional modules (Figure 2).

The iPSB supports multiple master processor agents. That is, the arbitration features can support up to 20

requests for the bus at the same time. This supports the functional partitioning approach and maximizes the effectiveness of each function.

One primary concern of the system designer relates to the processor — independence of a particular bus structure. The VME bus for example, lays claim to processor independence, and a brief glance through Fred Mazanec's VME Buyers Guide (Ironoak, La Jolla, CA) shows that although Motorola's 68000 has the lion's share of support, there is also some support for the Z8000, and 16032.

Multibus II also lays claim to processor independence, can support 8-, 16- and 32-bit machines, and is capable of transferring 8, 16, 24 or 32 bits of data. General system-wide functions, such as power-up/power-fail, bus-time-out,

system-timing references, time-of-day clock, etc. are centralized into one function called the Central Services Module. In multiple agent (board) systems, centralization of such functions reduces system cost and frees up board area for other functions.

The Central Services module can be located on a unique board dedicated to that function or on any board in the system. The interconnect address space is provided for dynamic configuration of Multibus II boards. This feature allows board options to be programmed or read from the interconnect space which simplifies the configuration of a system and allows system resources to be identified. It also allows system level diagnostics for system confidence reports. Unlike the VME bus, the iPSB bus is synchronous, so the signals only

Processor Independent Multibus Cache Memory

Central Data Corporation introduced at the Fall, 1983 Comdex show a processor independent cache memory board. This board images the entire Multibus address base (16 Mbytes) through the iLBX extension to the Multibus. The access time when a cache hit occurs is less than 100 ns.

The iLBX extension to the Multibus was announced by Intel at last year's fall Comdex show. Although Central Data is not the first company to support any devices on this bus, it is unique in that a cache memory is being supported instead of the normal dual-ported RAM which was intended for the bus.

The cache memory will store the most recent 4 Kbytes of data that have been accessed through the iLBX bus, and provide a fast response time for any subsequent accesses to the data. At any time when a cache miss occurs (and the data is not in the cache), the cache memory board automatically accesses the Multibus, updates the cache, and provides the data to the host.

This cache memory board can be used in lieu of many expensive dual-ported iLBX memory boards. It allows relatively slow Multibus memory cards to seem fast to the host, due to the caching effect. Assuming an 85% hit rate and a 500 ns Multibus cycle time, the average access time to the cache board (including miss cycles) is only 160 ns. This is more than twice the speed of any currently available iLBX memory board.

Unlike any cache memory developed for microprocessors today, the board is processor independent. This means that an iAPX 186 will work with the board, as will a Z8000 or a 68000. Central Data also announced a high-speed Z8000 board and a high speed 68000 board at the Fall 1983 Comdex show.

The cache is arranged in a way that only mainframe or minicomputer caches have been arranged to date. This is

an arrangement with two sets rather than one, increasing the performance of the cache considerably. The two set algorithm requires the board to determine which set will be overwritten during a cache miss cycle where new data must be put onto the board. This is done on at least-recently-used basis. Typical microprocessor cache memories have only one set, resulting in a simplified control circuit but lower cache performance.

The cache memory has parity checking on all of its data and tag memory, feeling that without such checking 85% of system access would essentially be to unchecked memory. Various error conditions that the board detects (including parity errors) cause the board to go into a soft shutdown, with the processor not seeing any effect other than slower accesses. In such a mode, all accesses are automatically directed to the Multibus, and the processor can optionally be interrupted to handle the error.

The board contains a monitoring circuit for the Multibus, which buffers write cycles that are performed on the bus by other masters. This allows the cache to invalidate any locations that have been updated on the Multibus, making sure that the processor always has correct information. When the host tries to access a location that has been invalidated, the Multibus is automatically accessed, and the new value of that location is read into the cache. This causes the cache memory to be totally invisible to the host, requiring no host intervention once the board has been tested and initialized at power-up.

A feature not found on any previous cache board is the Forced Miss Map. This map breaks systems memory into 1,024 pieces, each 16K long. There is a bit in the map for each block, indicating whether the cache should operate for that block or not. This allows the cache to bypass areas of dual-ported memory on the system bus. Such areas of memory may be contained on other processor boards, where the Multibus is not written, although the memory may be updated (by the on-board processor). This map can be used to force a miss cycle for any access to such a location, causing the cycle to be performed on the Multibus.

Write 302

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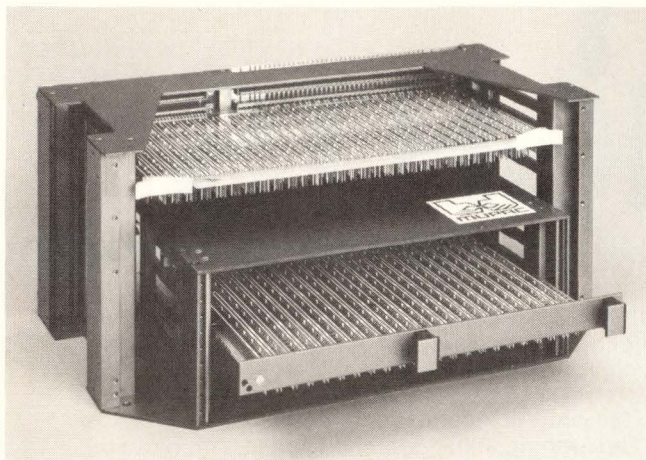


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Multibus II



have to be valid at specific intervals. Thus noise induced signals are not likely to be erroneously interpreted as data or control. Reliability is also enhanced by features such as parity on transfers, DIN connectors and distributed ground pins. Byte parity is checked and generated for address, data and command lines. Also, the isolation of critical signals with adjacent ground pins reduces noise in nearby circuits on the backplane.

Conceptually similar to the iLBX bus for the Multibus, the iLBX II bus helps to maximize performance in Multibus II systems by providing arbitration — free local memory expansion to 64 Mbytes and a maximum bus clock rate of 12 MHz. It will support 8-, 16-, and 32-bit processors and up to six boards. An alternate very high bandwidth path (48 Mbytes/sec) to the processors memory resources, the synchronous iLBX II can also support

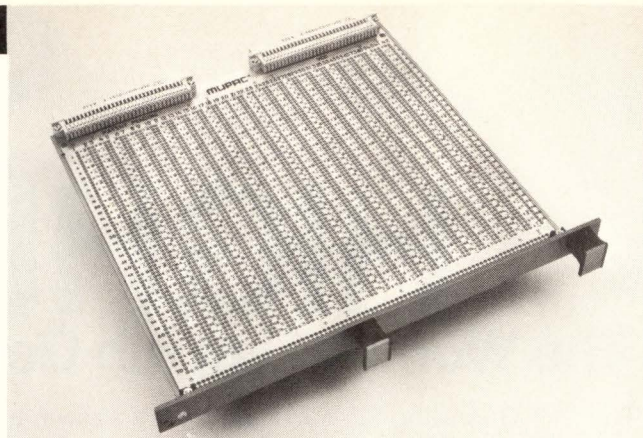


Figure 5: Mupac's Hybrid Card and Multibus II prototype board.

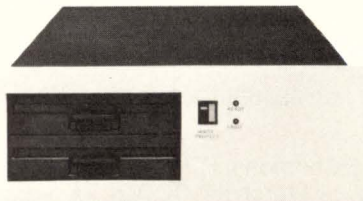
block transfer.

Interestingly, the VME manufacturers are also currently standardizing upon a dedicated CPU to memory highway (the VMX bus) endorsing Rich Bader of Intel's claim that this sort of bus is a necessity in high performance systems.

The serial system bus is very closely tied to some characteristics of the parallel system bus since it implements the message passing functions of the iPSB bus with low-cost serial interconnect. The iPSB bus 32-bit wide parallel transfers and runs at 10 MHz,

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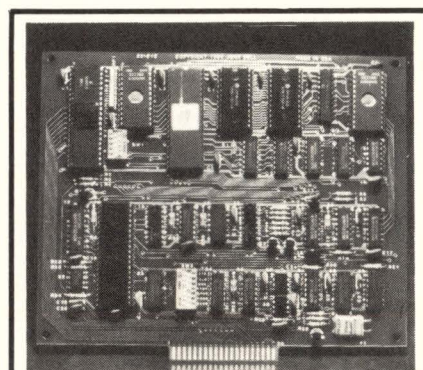


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Digital Design ■ December 1983

but the iSSB is a single serial line and runs at 2 MHz. Thus cost and performance are 2 orders of magnitude less.

The electrical requirements of the iPSB bus require it to be implemented in a tightly controlled manner. The iSSB, on the other hand, may be extended a distance of 10 m, allowing boards to be scattered within a box or even be in separate boxes. **Figure 3** shows the bus used in a photocopier design.

Carried over from the Multibus I system architecture, the Multichannel bus provides a standardized I/O interface with full speed operation at up to 15 meters with a simple asynchronous protocol. Allowing 8 Mbytes/sec block transfers of data, the bus can support up to 16 devices, both 8- and 16-bit and provides 16 Mbytes of memory or register address space per device. Typical uses of the bus include computer graphics, specialized peripheral control, data acquisition and high-speed Multibus system-to-system communication.

Also a carryover from the Multibus I system architecture, the iSBX I/O expansion bus allows incremental on-

board system expansion through the use of small iSBX Multimodule boards. Currently, iSBX boards add capability in the areas of speech, graphics and added math functions, without the need for adding another full expansion board. Some unexpected activity may be seen around the iSBX in future months, due to the fact that the VME standards group now plan to allow VME Boards the capability of using Intel's small plug-in modules as well.

Particularly in the European marketplace, the pin-in-socket connector and the Eurocard format have been implemental in the acceptance of bus related products. The pin count on such cards is higher than a corresponding edge card type and the contacting surfaces are fully protected from foreign body intrusion by the plastic shrouds.

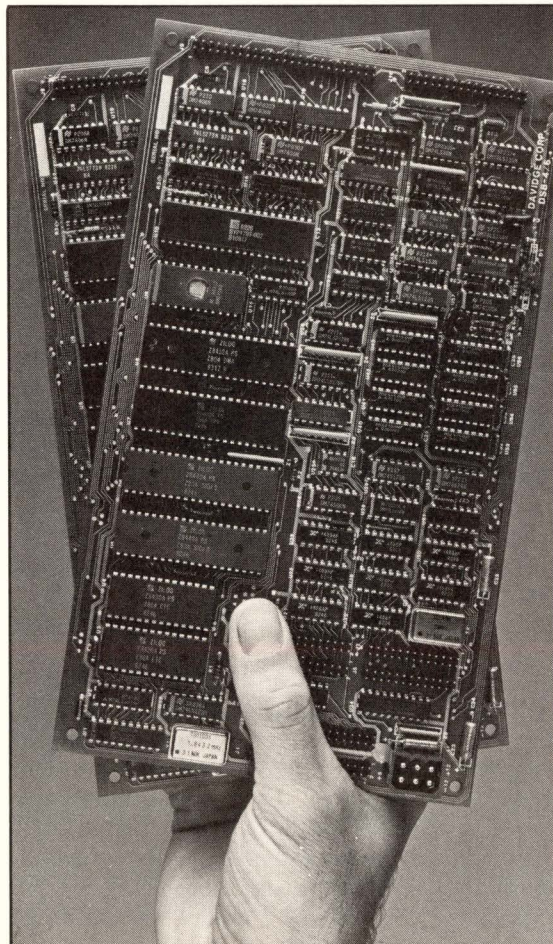
With the introduction of Multibus II, Intel has opted to go the European route. The new boards will have two 96 pin DIN connectors (for P1 and P2) and come in two sizes, single height and double height (**Figure 4**).

One of the concerns of the 3rd party

suppliers of Multibus boards was that Multibus II should provide a tie to the existing Multibus I. Intel's answer is to provide a link board that physically sits in the Multibus I backplane, and via an over the top connector maps Multibus I into Multibus II space through another board that resides in a Multibus II slot. Physically, the two sizes of board may both reside in a hybrid card cage (**Figure 5**) allowing the designer to protect his investment in Multibus I while allowing a short time to market on new products.

Because the bus structure of Multibus II is aimed to cover such a broad market area, from STD bus low-end systems through Multibus I and beyond VME, it will be interesting to note the lifetime of the hybrid systems. To an extent, it will depend on the availability of Multibus II boards from Intel and its large base of Multibus manufacturers.

With the weight of interest Intel has already gained from Prime, NCR, Foxboro and Tektronix, Multibus II should prove to be a serious contender not only to the VME bus, but to the STD as well. □



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The Micro-Floppy Race Tightens

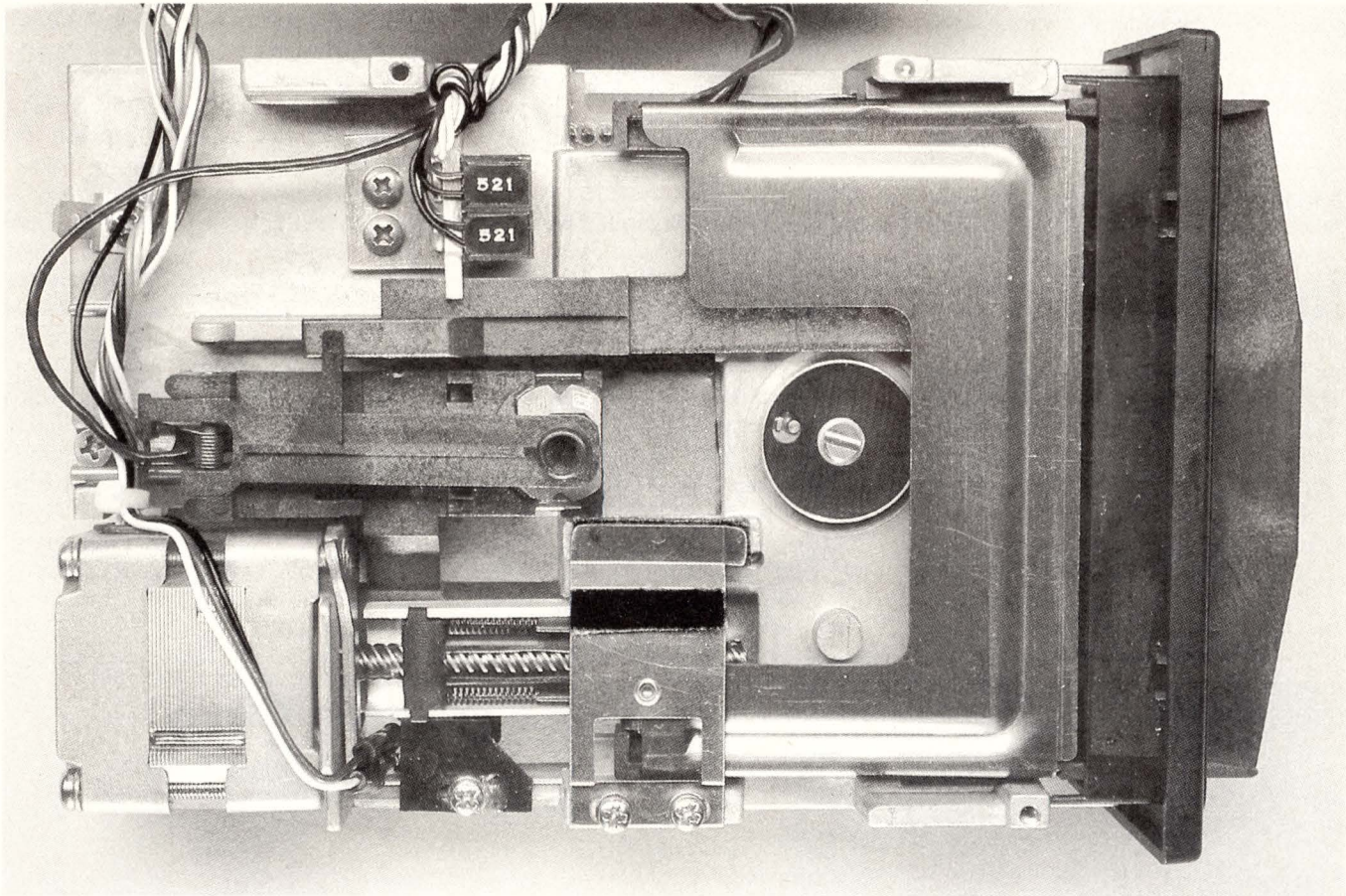


Photo courtesy Tabor

by **Bob Hirshon, Contributing Editor**

IBM learned the hard way that the days are gone when a single company can impose a standard on the mass memory market. Of four proposed standards for sub-4" floppies, theirs was the only one that wasn't designed and supported by several manufacturers. And theirs was the first to be withdrawn because of total lack of market acceptance.

The remaining three micro-floppy designs, each with strong support from a number of large manufacturers, will be around considerably longer. In fact, any system designers waiting for a

Bob Hirshon is Contributing Editor, Peripherals, for Digital Design, and Editor-in-Chief of Memory Update, a bi-weekly news journal of memory technology.

definitive standard to emerge shouldn't hold their breath.

All of the remaining designs are basically sound, and each has unique advantages over the others. This separates them from IBM's drive, which suffered from, among other things, low capacity, large size, and complete incompatibility. Therefore, the three drives still in the running, unlike IBM's device, should each capture a share of the market.

Also, the micro-floppies remaining each have the support of a variety of different companies, some small and some large. Many of these companies have too much invested in a design to allow it to die as gracefully as IBM's.

Three Contenders

The three micro-floppy designs currently being offered are: a 3.5" hard-shell media drive, based on the original

microfloppy introduced by Sony three years ago, and modified by the recommendations of a large group of manufacturers known as the Microfloppy Industry Committee (MIC); a 3" hard shell media drive, introduced by Hitachi, Matsushita and Maxell (HMM); and a 3.25" soft-jacket media drive (**Figure 1**), introduced by Tabor, and supported by Seagate and Micro Peripherals, Inc.

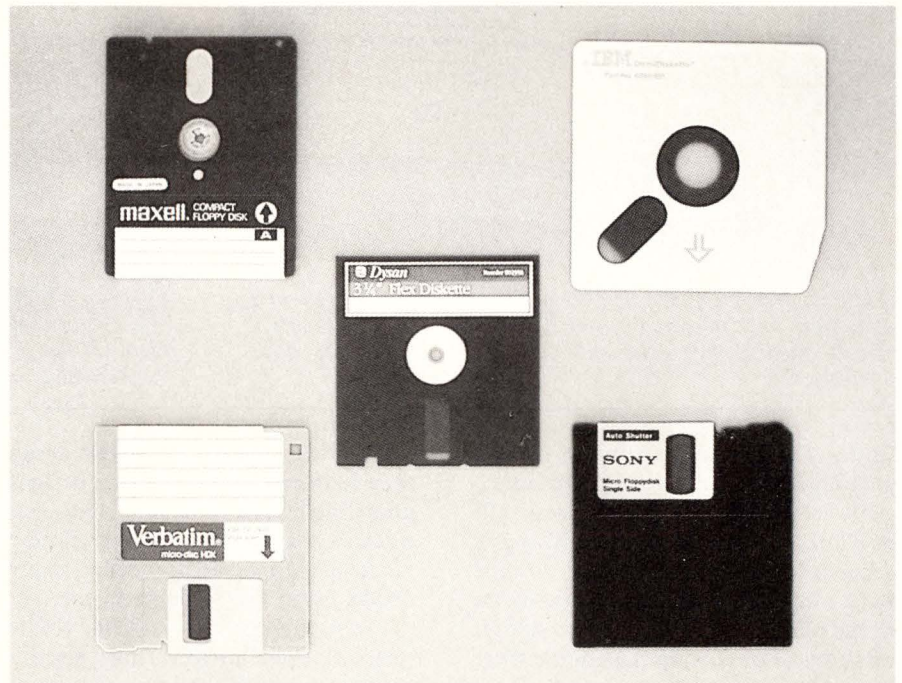
The MIC design has a number of factors in its favor, including the greatest amount of industry support (including Shugart, Control Data Corp. and Verbatim) and the most recording area per diskette (twice the available area of the 3" diskette). In addition, in September, ANSI committee X3B8 voted to accept the MIC design as a working standard. The vote was 17 for, 15 against, 12 abstaining and 15 not present.

With the demise of IBM's Demi Diskette, three micro-floppy media contenders remain in the running.

Although the vote was close and shows that there is still considerable question about the choice of a standard design, it is significant in that it indicates that currently the MIC design clearly has more support than the other two contenders. On the other hand, it should be noted that 27 of the committee members either opposed acceptance of the document or indicated ambivalence toward it by abstaining. Also, even some of the members voting for it did not preclude acceptance of other proposals for consideration.

More important than ANSI-acceptance is market acceptance, and here, too, the MIC micro-floppy has an edge, albeit an indirect one. Although the MIC drive hasn't been shipped in quantity, the Sony drive upon which it is based has. Hewlett-Packard, in particular, has been shipping the Sony drives in quantity for over a year, as part of H-P's personal computer systems (Figure 2), and reports good field performance. In addition, H-P reports that their sales of micro-floppy drives are outstripping their 8" and 5.25" floppies combined. This doesn't directly endorse the modified MIC version of the Sony drive, but it is an endorsement of the 3.5" form factor and the hard-shell cartridge.

There are also a number of disadvantages of the MIC micro-floppy compared to the other two proposals. It is the largest and most awkward of



With the departure of the IBM DemiDiskette (upper right), four microfloppy media remain, in three size formats. Sony's 3.5" microfloppy (bottom right), used in Hewlett-Packard desk-top computers, differs from the Microfloppy Industry Committee (MIC) microfloppy (bottom left) in coating thickness and functional specs. (Photo courtesy Dysan).

the three diskettes—not very noticeable when comparing one disk at a time, but definitely noticeable when carrying around a half dozen, or trying to send one through the mail.

Compared to the 3.25" microfloppy, both the media and the drive for the MIC microfloppy are more complex

and have more parts, which could be disadvantages in manufacturing and in long-term product reliability. Production quantities being equal, the MIC drive and media will also be more costly to produce; MIC opponents say the difference will be considerable, while MIC proponents say that in large quantities the difference in production costs will be insignificant.

Finally, MIC opponents claim that the MIC design suffers from being an older, ill-suited technology that was redesigned by committee. The original Sony product was "quickly assembled from existing video-tape, video-recording head, audio tape cassette loading, and plastic molding technology," claims Jim DeStefano, Business Strategist for Dysan, who support the 3.25" soft-jacket design. "Because of the number of compromises made and the performance limitations imposed by the original product design," DeStefano con-

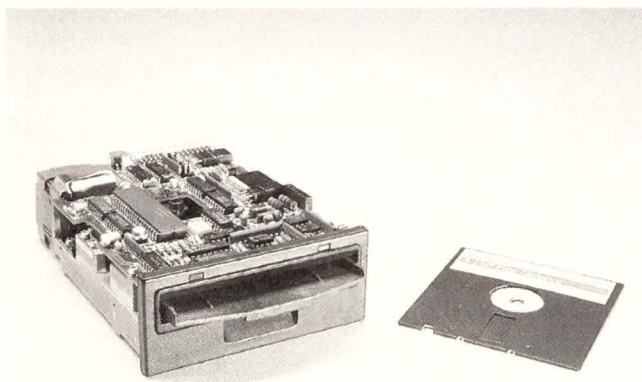


Figure 1: Tabor's Drivette micro-floppy, available in 500 Kbyte and 1 Mbyte models, is supported by Seagate and MPI.



Figure 2: Hewlett-Packard personal computers have used the original Sony micro-floppy for over a year. Today, H-P sales of 3.5" drives outstrip their sales of 8" and 5.25" flexible disk drives combined.

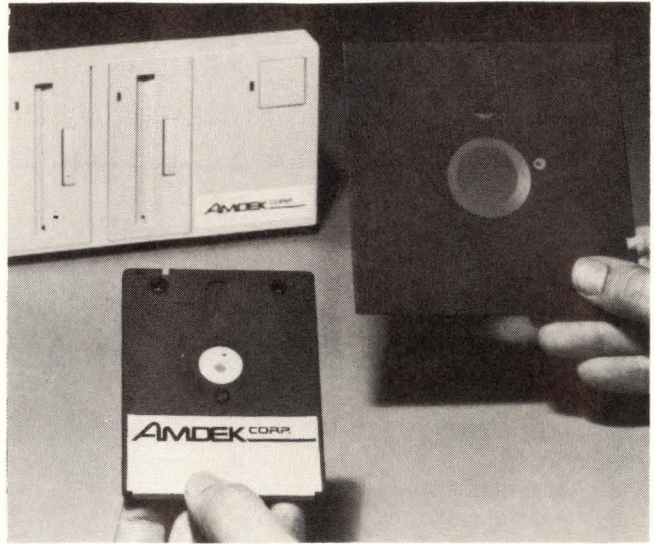


Figure 3: The 3" HMM hard-shell micro-floppy is the smallest of the remaining micro-floppy contenders (Photo courtesy Amdek).

tinues "the resultant, to-be-proven product is far from an optimal design."

If accurate, these limitations still don't preclude the MIC micro-floppy's acceptance; less-than-optimal designs have often become industry standards in the past. In the marketplace, design often is less important than marketing.

The Littlest Micro

The HMM 3" hard-shell design (Figure 3) has one big advantage in Japan: it fits neatly into a standard Japanese mailing envelope. This is one reason the design is supported by most major Japanese floppy manufacturers. Like the MIC media, the 3" media is encased in a plastic cartridge, and therefore resists puncture and can be written on with a ballpoint pen. Also like the MIC micro-floppy, it has an automatic shutter that opens upon insertion into the drive, to allow the R/W heads access to the disk surface, and closes upon removal from the drive—to prevent fingers from accidentally accessing same.

One perceived disadvantage of the HMM design is that both the media and the drive are even more complex than the MIC design, positioning it as the high-end entry in a largely low-end market. Also, with the least surface area of any of three contending micro-floppies (half that of the MIC media), the HMM media must use two sides to hold 500 Kbytes, and will require higher recording densities to go beyond that.

For these reasons, the HMM design seemed the weakest of the three designs, and didn't appear to offer any clear advantage over the MIC micro-floppy. As such, it appeared destined to follow IBM's Demi Diskette into history.

A new drive based around the HMM micro-floppy, however, has given a shot in the arm to the design (Figure 4). Introduced by Janome Sewing Machine Ltd., the drive was engineered for cheap, high-volume production.

*For the present,
micro-floppy
technology is
several steps ahead
of demand.*

Since they had no experience with computer electronics, Janome hired an American engineer, David Stoddard, to design the drive for them. Stoddard's no-frills design uses a manual disk seating mechanism, an indirect spindle drive motor, and a cam-controlled head actuator.

The bed upon which the disk cartridge sits in the Janome drive pivots at the back. To load a cartridge, the user must insert it and then press down to seat it. This manual system replaces an automatic, spring-loaded system in the Hitachi drive, saving some parts and increasing durability at the expense of

some user convenience.

A low-cost, high-torque DC motor drives the spindle via a belt and pulley. Optical sensing of disk rotation speed feeds back to the motor, to maintain rotation timing and to compensate for mechanical tolerances. Rather than the conventional lead screw head positioner, Janome uses a barrel cam.

The drive is slightly smaller than the Hitachi drive, and is available in a mechanics-only version. In this configuration, four drives can be mounted vertically in a standard 5.25" mounting, with the electronics located behind the drives.

With an average seek time of 245 msec and a capacity of 250 Kbytes per disk side (500 Kbytes per disk), high performance was clearly not Janome's goal. But Janome quotes the quantity price of the drive at \$125, making it extremely attractive to the portable computer designer. In this market, the performance should be adequate, if not very impressive. Furthermore, should a price battle between the various micro-floppy drives ensue, the Janome design, with its low parts count and simple mechanics, should fare well. Essential to acceptance in the U.S., however, is a strong American second-source for the drive.

Soft-Jacket 3.25"

If the Janome drive is the Volkswagen of micro-floppy drives, then Dysan's soft-jacket, 3.25" micro-floppy is the Volkswagen of micro-floppy media. It

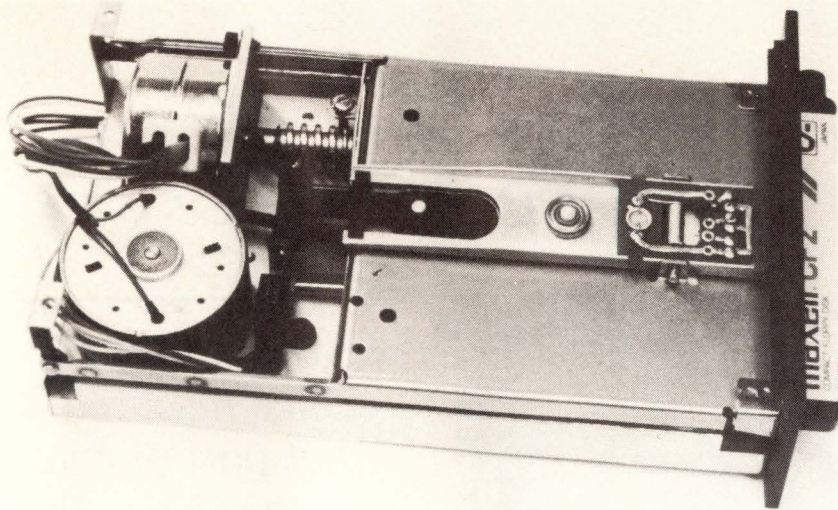


Figure 4: Janome's HMM-media based micro-floppy was designed for low cost and mass manufacturing.

is lighter than the hard-shell media, has fewer parts, and is cheaper to produce. Also, it's made of materials widely used in larger form factor diskettes.

Dysan manufactures the 3.25" diskettes under the name Flex Diskettes, and uses the same media as they use in the high capacity 5.25" diskettes. As a result, Dysan claims that the media is best able to handle the increased data densities that will be required in future drives.

The soft-jacket micro-floppy diskettes are less puncture-resistant than the hard-shell micro-floppies (they can't be written on) and are also more exposed to careless fingers, since they lack a shutter. As such, they are probably not as well suited to hostile environments inhabited by inexperienced users.

Except for puncture and fingerprint resistance, however, Dysan claims that the hard-shell of the other two micro-floppy designs offers no real advantage. Since they are not air-tight, they are still susceptible to particulate, liquid and gas contamination. "None of the designs protect the diskette from a three-year-old with peanut butter on his fingers," says Dysan's DeStefano. In fact, according to DeStefano, hard-shell media may be more vulnerable in some situations. For example, soft-jacket micro-floppies may be bent and still remain functional, while hard-shell micro-floppies will be damaged.

"We won't guarantee you that our

diskette will survive earthquakes, floods and other natural disasters, including little children," says DeStefano, "but by comparison to any of the other products out there, as far as protection goes,

we feel it's equivalent, and as far as the issues of cost and reliability, it's clearly superior."

Ahead of the Market

Everyone predicts a healthy market for sub-4" flexible disks—eventually. In fact, according to a report published by Venture Development, by 1987 micro-floppy diskette sales will generate more revenue than will the sale of any other form of removable media. But for the present, micro-floppy technology is several steps ahead of demand. The market for under-\$1000 portable computers, which is one key area where high volume demand for micro-floppies will be, simply has yet to develop.

Other lower-volume applications, such as test instrumentation, field recording instruments, and smart typewriters, are developing slowly. In the meantime, drive and media companies will continue to jockey for position, each trying to claim the largest share possible as the micro-floppy market gains momentum. □

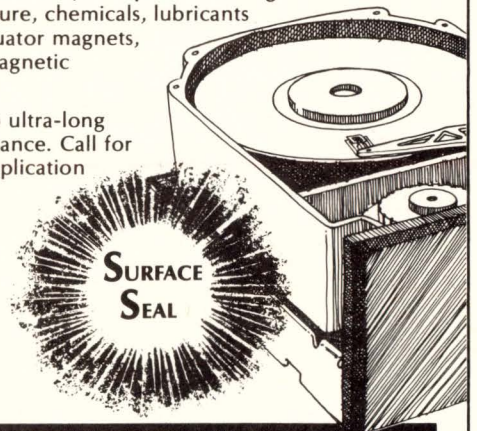
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The Debut Of Second Generation Artificial Intelligence



Figure 1: The Lambda, a new LISP-based computer from LISP Machine Inc., features the industry's first virtual control memory.

by **Mike Cashman,**
West Coast Technical Editor

Though its usage is not yet widespread, it is clear that the age of artificial intelligence (AI) has begun. Some computer experts see this development equivalent in significance to the industrial revolution. With AI, and the first payoffs of narrowly focused expert systems, one gets an even greater advantage, other than the outright speed advantage, compared to humans. One gets unexpected answers and observations to generalized questions.

The need for these systems is great. NASA is moving toward an expert system (a narrowly focused AI system) to perform automated Space Shuttle launches, thus freeing the seasoned launch support technicians for other missions. There appears to be a need to have expert systems inside nuclear power plants to serve as a consultant to managing these complex control environments.

While the defense establishment has always financed projects and studies into AI, it is commercial applications that should make these new kinds of

Artificial Intelligence research is that part of computer science that is concerned with the symbol-manipulation processes that produce intelligent action.

systems all but explode in popularity. And there is already a handful of successful AI applications. It is difficult to date the first unqualified success. When Prospector, an AI system, was programmed with the specs used by geologists to analyze potential resource-bearing formations, it successfully suggested geologists take a closer look at a prospective mineral deposit in Washington State. Thus the credibility of expert systems was established.

It has been said, somewhat cynically, that the definition of AI is revised as soon as researchers in the field reach each new definition. But the term intelligence is very difficult to define. Stanley Feigenbaum, of Stanford University, offers a reasonable definition that is no more generalized than the definition of intelligence itself. "Artificial intelligence research is that part of computer science that is concerned with the symbol-manipulation processes that produce intelligence action. By 'intelligent action' is meant an act or decision that is goal-oriented, arrived

at by an understandable chain of symbolic analysis and reasoning steps, in which knowledge of the world informs and guides the reasoning.”

While the success of generic expert systems, such as Prospector, offshore oil drilling, and perhaps nuclear power plant consultants will truly launch expert systems, these systems remain difficult to develop. Development is typically accomplished by debriefing experts in narrowly focused fields and codifying their analytical techniques into hundreds and sometimes even thousands of rules. But as experience has been gained in developing systems, it has helped better define what is needed in the way of better tools. As second-generation tools for developing AI systems begin to appear, they will almost certainly quicken the pace of announcements, and perhaps breakthroughs, in the field.

“To date, development systems have differed very little from what was developed inside the research laboratories,” according to Morris J. “Mache” Creeger, Director of Marketing at LISP Machine Inc., Culver City, CA. “They were barely sufficient to probe the problems of building systems, much less being able to assist in development.”

His company’s answer to the problem is the just announced (August, 1983) Lambda Machine (**Figure 1**) which addresses the shortcomings of previous development tools. Says Creeger “AI systems are almost uniformly going to require very large memory capacities.” For this reason, the Lambda Machine is offered in two sizes: a 24-bit (67 Mbyte) virtual address space and a 4K cache. The 64K by 64-bit virtual control store is paged 16 words at a time into a 16K by 64-bit physical control memory, of which 8K is reserved for basic system control. The second version is a 40-bit LISP processor that provides a 32-bit (21.5 Gbyte) virtual address space.

The Lambdas are based on the 32-bit NuBus communications-oriented architecture developed at MIT’s Computer Science Laboratory. The processor, or processors, and subsystems all share a 40 Mbyte/sec bandwidth resource. A separate board senses what kinds of devices are appended to the system and logically configures the system automatically. The Lambda also

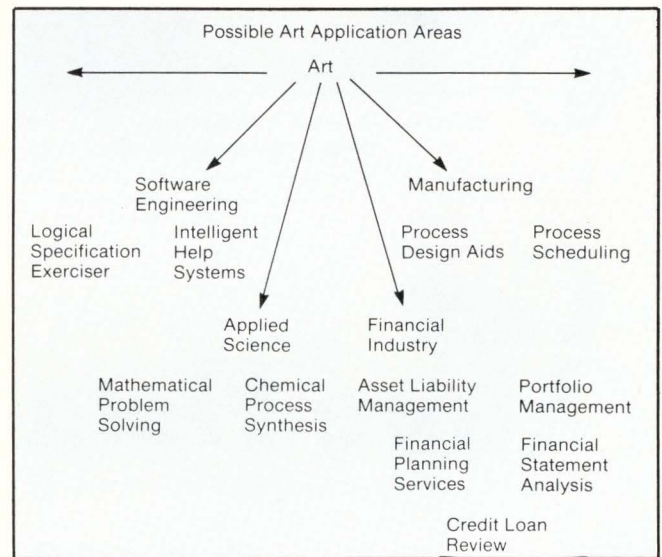
features a 16 x 16 matrix multiplier, a 256K by 32-bit error-correcting physical memory, a 470 Mbyte Winchester disk, display, and mouse for \$72,500 in 32-bit version.

A UNIX processor and software license is also available for the Lambdas. It can be installed to run concurrently with the LISP processor, communicating with it on a process-to-process basis. A typical application for the dual-processor Lambda would be to use the UNIX processor as a multi-user front end to package and send requests to the LISP processor. Since the August announcement, Creeger states that eight Lambdas have been shipped, most to the defense/aerospace community, which has to constantly worry about being outflanked on potentially important technological issues like AI.

accompanying infighting. It would be useful if we could all sit down and synthesize where we are and what we can and cannot do. 3) The learning problem. How can AI systems learn new facts about the world?”

Williams sees two very different paths in the immediate future in the development of expert systems and AI. These are, generic systems for large markets, say in the medical and resource prospecting fields, and developing systems that would use the data stored in today’s existing data bases. For this market, Inference Corp.’s President, Dr. Alexander Jacobson, sees considerable customer hand-holding, and a great deal of user interaction at the systems level. He feels that joint ventures between his firm and others in the AI field, together with companies with needs in various knowl-

Figure 2: Possible ART (Advanced Reasoning Tool) application areas. Courtesy Inference Corp.



By and large, AI will predominantly be a software and problem definition problem, according to Chuck Williams, Vice President of Technology at Inference Corp., Los Angeles, a developer of software tools for the AI market. “There’s lots of room for progress in the AI field, but I’d rank the problems confronting us starting with these three. 1) The search/control problem, especially in knowledge rich domains. Humans can go down a solution path to a problem while almost simultaneously wondering whether another approach might be more suitable. AI today isn’t very good at that. 2) The need for synthesis in the field. There are a lot of techniques for representing and applying knowledge, and lots of

edge sectors, are the best way to promote the technology’s capabilities.

Toward this end, Inference Corp. has just announced the Advanced Reasoning Tool, or ART (**Figure 2**). ART makes possible the creation of expert systems by providing two capabilities: A representational formalism for expressing all of the knowledge contained in the expert system’s knowledge base, and an automated process for organizing and applying this knowledge in order to solve the problem. According to Jacobson, ART can explore deductive consequences, propose and evaluate alternative hypotheses and reason about the utility of knowledge in its knowledge base. One of the first joint-venture targets for

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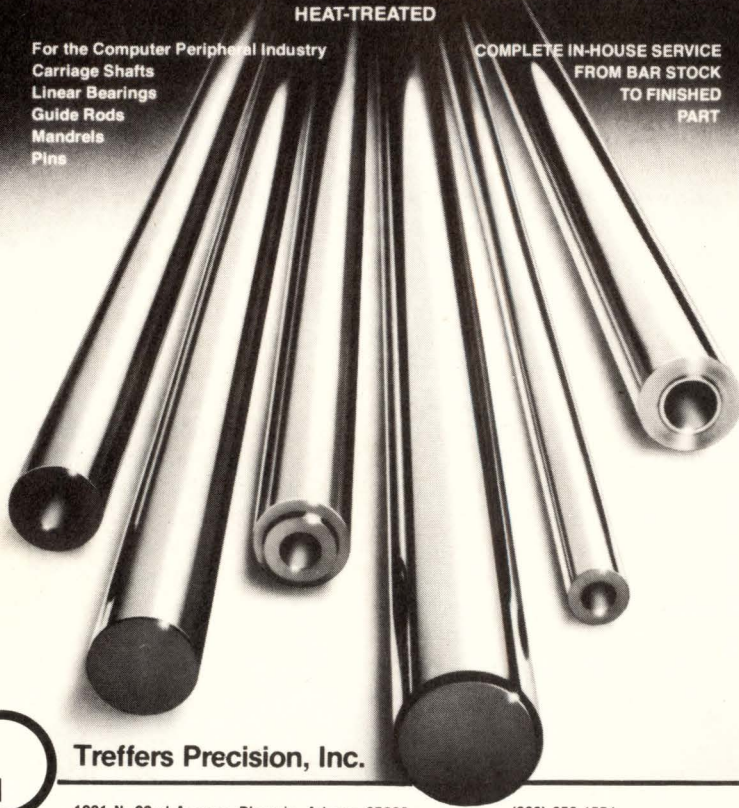
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Artificial Intelligence

Inference Corp., says Dr. Jacobson, is the development of an assets and liabilities management system that would develop a funds allocation strategy for a financial institution. The system could determine the financial state of the company and that of the marketplace. By interacting with management, the system could develop financial constraints and consider hypothetical results in a stable funds portfolio.

But that's an example of a separate, generic product that might be developed to operate on existing data. How are existing systems to gain from progress in AI? For example, what might be done with the tremendous amount of information stored in airline reservations systems (which is retrievable for several years), and how might AI be used?

Inference Corp.'s Williams feels that highly interactive, questioning systems will be required. "That's one of the first uses that comes up, something to back-end an existing data base. But AI and expert systems won't be plug-in types of approaches. For systems designers currently defining projects, Williams has a word of warning. "Keep it as modular as possible so that maturing AI techniques can be applied without having to throw the entire system away."

Williams defines three types of user scenarios with various types of expert systems that are coming. 1) Fully automatic ones that might, for example, launch routine Space Shuttle missions with little, if any, human interaction within a few years. (NASA is very interested in this possibility.) 2) Users are not experts in the task undertaken. An example might be assistance in selecting banking services and options. And, 3) users who are experts working in conjunction with an expert system, or using it as a consultant. One possible system that is being considered would be an expert system for a nuclear power plant.

Much of what is occurring in AI today can be compared analogously to a nebulous cloud just beginning to take shape. But one thing seems certain: Experience gained with these second generation commercial tools will bring two events closer — third generation tools, and less modest accomplishments. □



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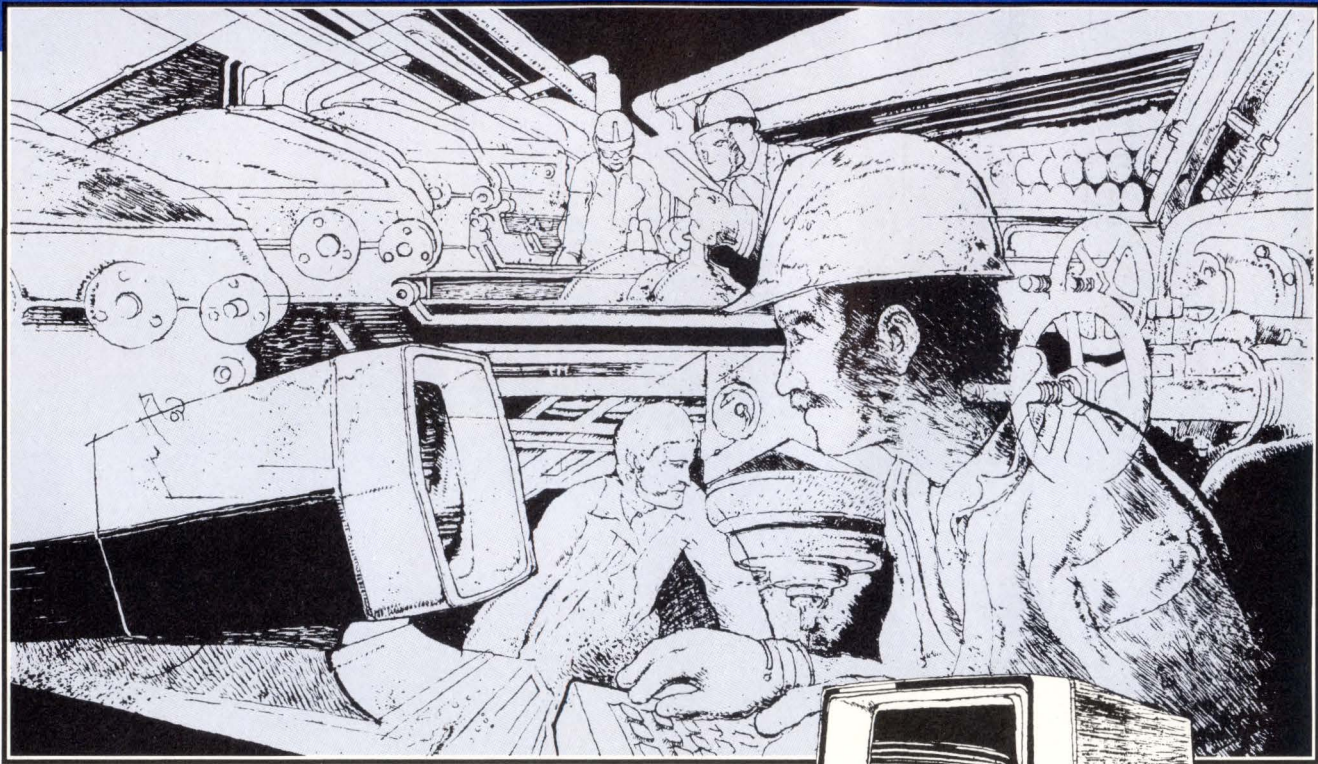
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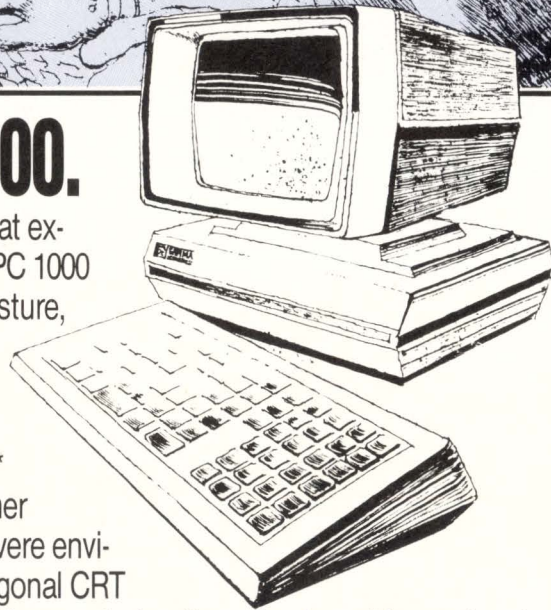
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Engineering Workstations Meet Demands For Individual Design Needs

The workstations of today allow for either greater specialization within applications, or allow a single designer to become involved in a greater portion of the entire design process.



by Jerry Borrell, Editor-in-Chief

One of the misleading concepts related to engineering workstations is that their development has been recent, or related to the field of IC/PC design. Computers in support of electronic design functions, such as test and technical or project support, have been in use for nearly ten years. The use of graphics-based workstations for these applications is almost as old as the use of computer workstations for layout of designs, simulations, and verifications.

The work over the last two years which has attracted a great deal of attention is more realistically described as providing workstations more capable of interactive design and engineering, for the individual engineer. In addition, software is being developed for the increasingly powerful workstations that formerly required minicomputer or mainframe support. Thus while there has been new development of workstations, it is the performance, not the applications, that is radically changing.

Several of the manufacturers consulted in researching this article noted that the success of relatively new firms such as Daisy or Mentor demonstrates

the frustration of engineers who have worked with less responsive minicomputer or mainframe supported workstations. Another source of recent improvements in workstations is their increased productivity potential. In a marketplace driven by competition, it is important to be the first into production with the most effective product. Today's workstations must offer more timely design production to survive.

Electronic Applications

The electronic workstation differs from the mechanical workstation primarily in its significantly lower requirements for graphic displays. Typically, mechanical design systems do not need real-time interaction, but the ability to display smooth shaded images. Graphics display tasks for integrated or printed circuit design conversely demand fewer colors, and much less intensive tasks for display dynamics. The CPU demands of both fields are dependent upon the applications, and not the display, so are less open to ready comparison. Both fields do have similarly demanding analytic tasks, leaving the system builder with the decision of which marketplace is most profitably addressed. It may be overly simplistic,

Figure 1: Avera's 2100 Engineering Design System. Avera's recently introduced workstation is based upon the Hewlett-Packard 500 Series 32-bit computer. Avera uses this powerful engine to support schematic design, logic simulation, test, circuit simulation, circuit layout, verification, and artwork generation.

but nevertheless fair to say that none of the subfields of electronic workstation design rivals the complexity of the mechanical subfields, such as finite element analysis. Users' application programs may contain a quarter of a million lines of code. The effort by firms such as Avera, however, begins to rival these levels of complexity because of the broad set of applications being offered on the company's system.

Hardware/Software Interaction

Apart from the bewildering array of products and services (see box) which the designer must evaluate, there are the more subtle considerations of hardware and software interaction. This aspect of any system may prove to be the most difficult to evaluate because unlike functions of an applications software package, interaction may require extensive use to be appreciated.

There are several areas of interaction that can be readily considered, including the recently popular ergonomic aspects. Such features include work surface (rounded edges and a lip for working materials), the ability to adjust the height and angle of both work surface and display, and the type of interactive devices offered, i.e., joysticks, stylus, or lightpen. Beyond these are several features not readily evaluated. Because the systems' display, either monochrome or color, is the focal point for all work, it should receive attention.

The rate at which the display is refreshed is probably the most important of the factors. With either monochrome or color, refresh rates of less than 30 times per second can cause problems, and for applications such as monochrome reverse video (black on white) a minimum of 60 times per second is needed. Insufficient refresh rates cause the screen to flicker, that is, the information displayed has an unsteady appearance. Color displays, particularly of photographic quality may have similar problems. Problems such as these may be aggravated in fluorescent lighting, producing a series of flowing waves of light and darkness across the screen, generally described as a "beat."

Among the devices supplied for design use, the graphics tablet has become most popular. In the recent past this device was primarily used for digitizing, to enter line or point information for a design. More recently it has been used as both a cursor control and picking device. For example, many companies will provide menus of software functions that are overlaid on the tablet and the engineer picks functions from these overlays. In other cases, the tablet allows the cursor to be positioned for screen-based menu interaction. Two firms, Intergraph and Applicon, even allow the tablet to take on keyboard functions, allowing the user to call up an operation by sketching a command directly on the tablet.

The joystick has been an integral part of the older generation of workstations, particularly among high performance graphic systems. However, few manufacturers of new workstations are including it. Many engineers have expressed a dissatisfaction with the need to adapt to a technique that is



Figure 2: AED's new S11 workstation makes use of its 767 graphics processor and is representative of the competitive products for low cost color, high performance terminals available to systems integrators.

unrelated to a typical drawing function. Apollo, for instance has withdrawn a finger operated cursor controller. The method of controlling cursor motion with a stylus appears to be preferred over joystick control for either mechanical or electrical design. The mouse, a device popularized by Xerox, has also helped to erode the use of the joystick. Like a stylus, the mouse allows more natural drawing motions to be used by the designer. A recently announced optical mouse from Mouse Systems allows the device to be used on any surface, addressing the problem of limited physical working space.

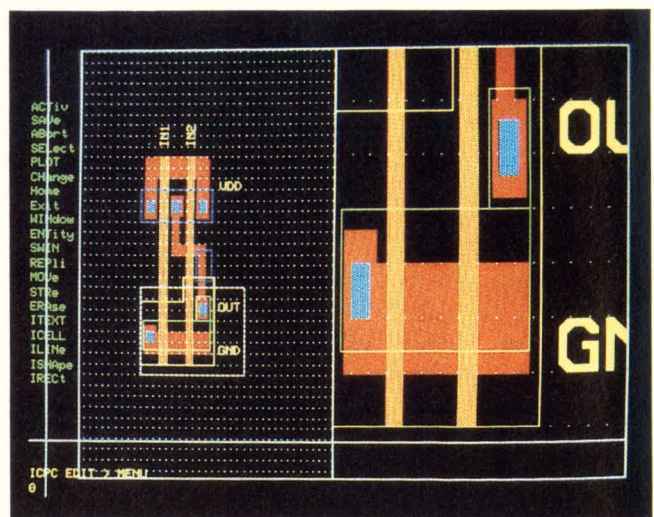
Two companies have recently introduced workstations based upon direct screen interaction: Telesis' PC design

station has a waist level pen interaction that requires the user to depress a pen on the screen surface, and Spectra-graphics offers light pen use on its color IBM compatible products. Hewlett-Packard offers light pen options on many of its workstations, and now provides a touch interaction capability for one of its terminals.

Finally, the workstation user must consider all of these options in light of the software interaction capabilities offered by the vendor. There are several levels of interaction that should be evaluated, and few standards to assist the engineer in doing so. Among these are the hierarchical considerations, data base management, and input/editing techniques. The basic approaches to software interaction in terms of hierarchy include menus, prompts, and command structures. The well established firms who have provided engineering workstations, usually provide the user with the capacity to switch between one or another approach. Considering that many different types of users may have to access a system, this is well worth the extra expense. Each of the approaches may be appropriate for certain users: prompts for novice users, menus for intermediate, and commands for the accomplished designer. Few of the new systems integrators have had the time to adequately address these issues.

As workstation manufacturers offer more software applications on their systems they must be able to support efficient database management systems. While the applications programs will vary, the designer should be able to

Figure 3: The ICPC electronic system development tools software family of products available from UNIRAS is one of the system independent software packages with applications in IC layout (shown), PCB layout, schematic capture, logic simulation, and verification.



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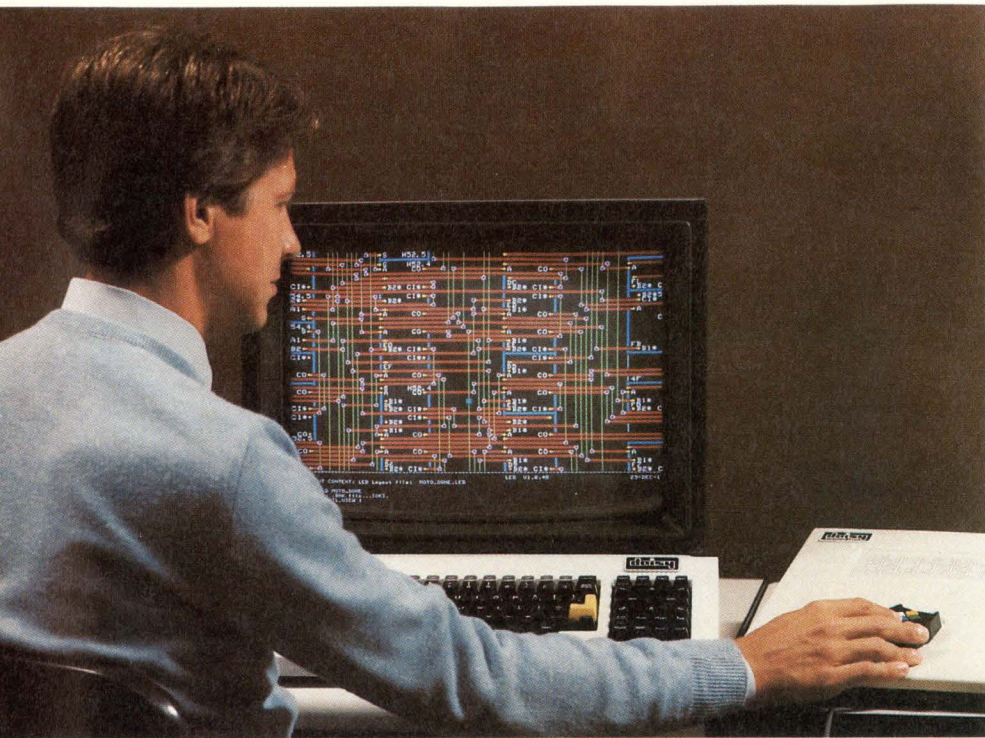


Figure 4: Daisy's Gatemaster design workstation is aimed at supporting gate array and standard cell design of products from Motorola, TI, AMI, CDI, IMP, National, Fujitsu, LSI Logic, and Control Data. The company is one of those providing a common set of design tools for a diverse range of silicon products.

access common system commands among all applications, and to move file information freely among applications. Among the newer systems, however, there is no assurance the designer will find this to be true. Editing and input interaction may be the most important consideration in terms of day to day design work. The techniques available here are tremendously diverse with some suited for either two or three dimensional work, some for dynamics, and others that are unique to certain applications. The oldest set of interaction functions relate to geometry input and range from tech-

Choosing A Workstation

One of the inevitable questions facing the design engineer is how to obtain access to an engineering workstation. The needs of engineers require different types of access be available. The design engineer at a semiconductor firm may work throughout the day on a workstation. The engineer at another manufacturer may need to access an electronic design station for use with a single product. For example, he may want to evaluate the potential of bringing several components onto a chip set, or onto a semi-custom device such as a gate array. In both cases, the designers must be able to not only use a system for the design process, but also to determine the suitability of a design process to the project under consideration and the needs of the final project. Thus, even the design engineer is faced with a bewildering array of products which offer to perform some or all of the functions that the designer requires. Several manufacturers offer programs that provide alternatives to the purchase of systems or services. The General Electric subsidiary, Intersil, for example, has established several design centers across the country. Designers can rent time on in-house systems, and after an initial training period on the system, can design their own products. Control Data has similar design centers. In addition, both of the companies have silicon devices with which their design products are linked.

One of the other recently developed programs, from Harris Computer Corporation, is called the Dial a Chip program. Harris, like Control Data, produces mainframe computers and benefits by providing timesharing services on its own systems. Another Harris division produces semiconductor products, including semi-custom gate array devices. Dial a Chip unites these products and serv-

ices to allow remote users the opportunity to produce custom designs without purchasing costly design stations. A prerequisite to use of the system is that the designers be trained on the company's software, and become familiar with the semiconductor devices used in the program. With this ability, the user is able to select a workstation based upon alphanumeric or graphic displays. Harris is working with the new color graphics terminal from Chromatics in the latter case. Purchasing a graphics terminal of course costs more for the user, but offers the additional capability of supporting art work design for editing, modification or layer connections. The Harris program, on the other hand, offers a wide range of functionality including: net list entry, schematic capture (also on the workstation), logic simulation (this includes fault simulation and timing simulation), routing, net checking for net logic verification, logic simulation, and a direct interface to Harris's mask production and wafer making capability.

The overall effect of this program and others like it will be to provide a competitive alternative to those companies which only offer products for sale. One immediate advantage is that the user has a much closer connection to the entire process of layout, design, and fabrication. The approach taken by Matra Design Systems of San Jose offers the best of both worlds. Matra sells a low cost stand-alone design station based upon the 400-1000 gate products from Harris as well as providing fabrication (metalization of the devices), but plans to support design on other chips as well. Thus, while it is not clear which approach will be more successful for a marketer of systems, the effect is to provide the designer with a greater opportunity to make use of semi-custom technology.

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Engineering Workstations



Figure 5: Aydin's AYCAD is a 8086/8087 based generalized CAD workstation initially targeted for VLSI design, but intended to provide users with a low cost entry system for workstation applications.

Figure 6: Hewlett-Packard has recently organized its workstation-designed products into the Series 200 Personal Technical Computers. The company produces three systems in the 200 series based upon the Motorola 68000, the 16, 26, and 36, in addition to its Series 500 (formerly the HP 9000).



niques for the input of line and point information to the ability to scale, rotate, or display designs. Newer techniques based upon recently available solid modeling or mechanical design allows for facile manipulation of three dimensional shaded models. The presence of a comprehensive set of these techniques varies from system to system, the cause being either limited resources or lack of experience on the part of the systems designers. The lack may be unnoticed, in any case, for many users of today's engineering workstations have had no background with other graphics systems, and don't perceive a compromise in performance.

Summary

One of the most important changes in engineering workstations has been the development of increasingly sophisticated applications specific systems. As a result of the need to provide both more powerful systems and to integrate complex bodies of software, the

marketplace is divided into producers of the engines or workstations, upon which the sector of system integrators base their products. Manufacturers such as Hewlett-Packard and Apollo now produce engines that are the basis of at least a dozen other systems. Despite a seemingly rapid growth of workstations, there are many questions that relate to the financial origins of these companies. The companies appear, for instance, less able to fulfill additional demands for workstation capability than to address potentially lucrative segments of applications markets. The venture capital market has potentially influenced growth for some products and applications that might not have occurred. The volatility of this marketplace, given that influence, may be great over the next several years. As computers in analysis became tied to graphic display, the functions of drafting, manufacture, and analysis have combined to allow workstations to become the basis for a new generation of engineering and design. □

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Superminis Offer A Cost-Effective Solution for High Throughput

by Ram Appalaraju

Multi-user environments were limited to large mainframe systems such as the IBM System/360 series until the late sixties. The dominance of such systems has been challenged by the emergence of "expanded" versions of minicomputers since the early seventies. The result was a superminicomputer boom. Since then, superminis have been preferred to mainframes for a variety of applications, primarily due to their lower cost.

The precise definition of supermini-computer is a computer which: has a Central Processing Unit with an internal word length of 32 bits or more, has at least 1 Mbyte of main memory and has the ability to perform in a multi-user environment.

Since the early seventies, many manufacturers have been involved in the supermini market. The focus of development initially was on an expanded I/O structure, an operating system that caters to multiple users, etc. Later innovations have been based on a virtual memory system that erases the "fear or limited memory" from the user. However, since the late seventies, the industry in general has aimed for speeds comparable to, if not greater than, mainframes. This, in essence, means that manufacturers have now more than doubled the CPU throughput of their earlier models.

Various design improvements like parallel processing, pipelined architecture and advanced logic technology have allowed this enhanced throughput. The technology improvement here is the switch to ECL technology from Schottky TTL, primarily an improvement in switching speed response time. But this has resulted in increased cost.

Supermini manufacturers may be broadly classified into those who support virtual memory and those involved in producing systems for realtime process control applications. The two manufacturers actively involved in the latter category are Gould SEL and Perkin-Elmer. While the first category is more apt for multi-user applications, the latter is best when very high throughput is needed (**Table 1**).

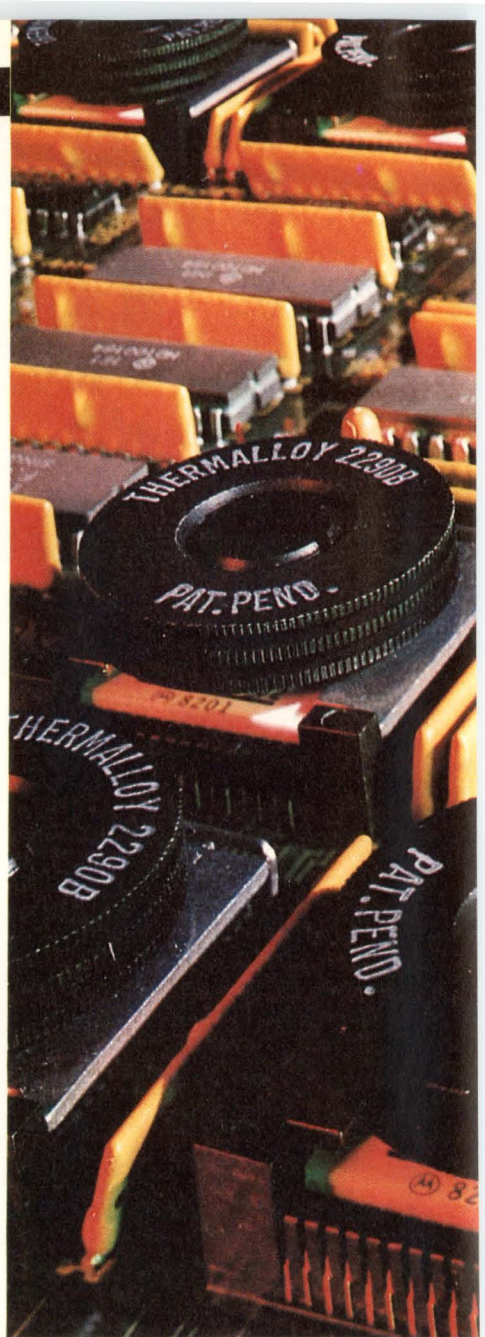
System throughput of supermini systems is upped to mainframe speed by implementing a pipelined architecture or incorporating an asymmetrical multiprocessor structure or both.

Virtual memory is largely implemented by Digital Equipment, Data General, Prime Computers and Harris Corporation. It is logical to compare capabilities of these systems in terms of how many concurrent users each can support. But though the number of terminals that can be physically connected is often more than 128, seldom does the system perform well under full load.

A reasonable estimate is that the degradation in performance starts when 70% of the stated maximum number of terminals are in use. The factors in the efficient functioning of these numbers of terminals are the operating system, virtual memory, memory management, CPU throughput and the I/O (communications) processor's ability.

The VAX 11/780 and Prime 9950 support memory management in hardware. However, virtual memory is achieved essentially by software. The page (address) registers are loaded and reloaded by the software depending on the number of users.

The Prime 850 performs without degradation for 80 users or more. But in the case of the 9950, because of the



logic and pipelined architecture, this is improved by 50%.

Harris claims that in their H1000, the virtual memory is completely hardware implemented. Each of the page address registers are dedicated to the user, once the user is logged on. The logging in of a new user is, then, transparent to the original users. This is a primary factor in the H1000's ability to provide good performance even when the number of users approaches the stated maximum.

The VAX family of superminis essentially have four modules: CPU, console subsystem, memory and I/O adapter. In the VAX 11/780, these modules are linked together through a Q-bus, a Unibus and a Massbus (**Figure 1**).

The function of the console subsys-



Photo courtesy Harris Corp.

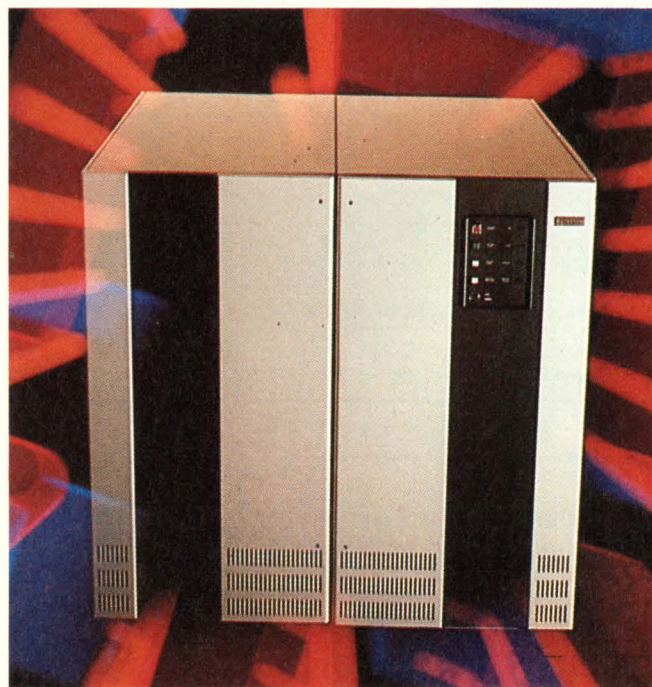
tem is dependent on the mode of the LSI-11 processor unit. The LSI-11 operates either in an I/O mode or in a console mode. When in the console mode, Z interprets all console terminal output to perform diagnostic and maintenance functions. Though the 11/780 architecture is not pipelined, the 8KB two-way set associative cache makes the system perform well under multi-user conditions. The VAX 11/780 is well-suited for an university application and, perhaps today, is the most popular system for scientific applications.

The VAX 11/782 is a tightly coupled asymmetrical multiprocessor system that consists of two VAX 11/780 CPUs. The system performs twice as fast as the VAX 11/780 and is best suited for applications involving intensive calcu-

lations. The highend superminis from Prime, Data General, and Harris are all pipelined and provide a higher throughput than VAX 11/780. But for research and scientific applications, the VAX has been largely used and its large base of software support is the reason why Digital Equipment Corporation is the leader in the supermini market today.

The MV10000 from Data General is implemented in Schottky TTL technology, making the system less expensive than the Prime 9950 and Harris 1000. The MV10000 uses a dedicated address generator to accelerate the system performance by generating logical address prior to their use by the instruction processor. The system also uses a two-board floating point unit — a feature unique in the Eclipse family.

Various design improvements like parallel processing, pipelined architecture and advanced logic technology allow enhanced throughput.



The Prime 9950. (Photography by Grohe of Boston)

The pipelined MV10000 CPU consists of five separate microcode-controlled subsystems: Instruction processor, Microsequencer, Address Generator, Address Translation unit and Arithmetic and Logic Unit. All the five logical units are connected by a 32-bit wide central processor data bus (Figure 2).

The higher-end products of Prime, the 750, 850 and 9950, all support a pipelined architecture. However, the Prime 850 is a multiprocessor system like VAX 11/782. The Prime 9950 incorporates a five-stage pipelined central processing unit. The five stages perform synchronously with the time taken by each stage equal to 80 nsecs.

The highest level of pipelining is achieved by Harris' 1000. The Harris 1000 can execute up to seven instruc-

Superminis

	VAX 11/780	VAX 11/782	PRIME 850	PRIME 9950	DG MV8000 II	DG MV/ 10000	PE 3200 MPGS	HARRIS 1000	GOULD 32/87	GOULD 32/8780
Virtual Memory	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	No	No
Maximum Memory Size	8MB	8MB	8MB	16MB	8MB	16MB	16MB	12MB	16MB	16MB
Max Cache Size	8KB	8KB	32KB	16KB	16KB	16KB	8KB	6KB	64KB	128KB
Effective (avg) memory access time w/cache	280ns	280ns	130ns	84ns	275ns	168ns	500ns	250ns	94.5-153ns	94.5-153ns
Approx Whetstone MIPS	1.2	2.0	2.2	2.5	1.3	2.7	NA	4.0	3.7	6.6
No. of Terminals	96	96	128	128	128	192	64 (1023)	192	112	112
I/O MB/SEC Throughput	13.3	13.3	8.0	9.0	18.2	28.6	10	19.0	26.67	26.67
Architecture	32 bits	32 bits	32 bits	32 bits	32 bits	32 bits	32 bits	48 bits	32 bits	32 bits
Operating System	VMS	VMS	PRIMOS	PRIMOS	AOS/VS	AOS/VS	OS/32	VOS	MPX-32	MPX-32



The Harris 1000 superminicomputer.

Table 1: Superminicomputer characteristics compared.

tions simultaneously (cycle time = 75ns). Implemented in 100K ECL, as against 10K ECL in the Prime 9950, the Harris 1000 is the fastest performing supermini in the market today with a throughput of 4 MIPS.

The Harris computers are the only superminis to have memory word lengths of 48 bits. The single processor Harris 1000 performs at 3.912 MiPS in a single precision and 3.729 MIPS in double precision in Whetstone benchmark testing. This, according to Harris, is 350% faster than VAX 11/780 in single precision and 400% faster in double precision. The unique feature

of the Harris 1000, is that the transcendental functions such as trigonometric, exponential and logarithmic functions are implemented in hardware in the CPU for a quicker response.

Another innovation in superminis is the improved cache bit ratio. In order to reduce the number of main memory write cycles in the MV10000, the system cache is directly mapped to main memory and employs a write-back technique. Write-back technique means that when cache transfers data in or out of main memory, it moves an entire 16byte block. When a port (CPU or I/O) writes to the cache, it does not

affect the main memory unless the written location is not currently in the cache. When the written location is not in the cache, the MV/10000 brings the new cache block into the cache, and then the port writes to the location. The processor moves the old cache block to a temporary location, and then into main memory.

The Prime 9950 has a branch cable memory apart from system cache. The branch cache memory allows overlap of cache access and performs some functions in a pipelined architecture. The branch cache memory comprises 256 entries to keep track of program branches and to predict which way a branch will go.

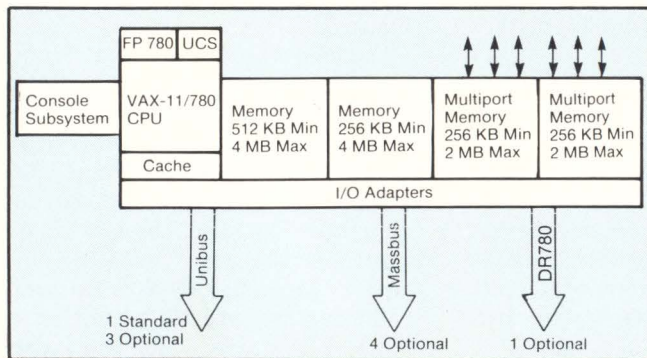
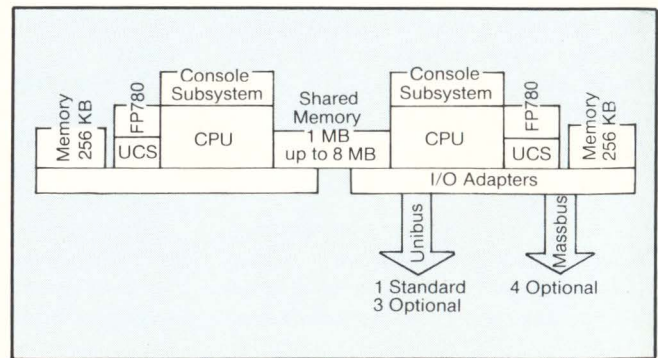


Figure 1: Configuration of VAX 11/780 and 11/782.



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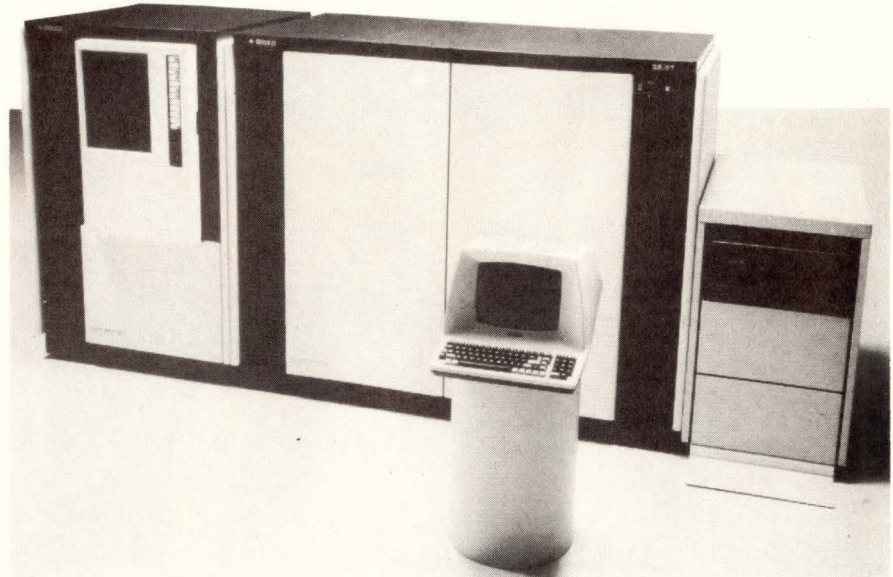
Working Together To Be The Best

The Gould Concept Series superminis from Gould S.E.L. offer solutions in applications requiring a high throughput. The latest in the series, Concept 32/8780 is suited for rigorous engineering applications (apart from number crunching applications which require a large memory), such as real-time applications and simulation.

The processor of 32/8780 is implemented in ECL technology with a 75 nsec cycle time. The processor consists of two units: The Central Processing Unit (CPU) and instruction processing unit (IPU). The architecture of the system consists of a high-speed synchronous bus called the SEL bus that has a transfer rate of 26.67 Mbytes/sec. The CPU, the IPU, the main memory, and the input/output subsystem are connected to this bus. The four stage instruction pipelined system is supported by two four-stage eight-bit set associative cache memory.

The 32/8780 is supported by a hierarchical memory system made up of various levels; each level is successively faster than the one below. Working together with cache, the CPU/IPU can access the data at the rate of 75 nsecs. The main memory is a high density memory subsystem that includes up to 1 Mbyte of dynamic MOS RAM. Also housed on the memory module are the memory controller, error connecting logic and refresh circuitry.

The 3200 series from Perkin-Elmer has been in the supermini market since 1974. The latest in the series, Model 3200MPS, is a tightly coupled multi-processor system that contains, apart from a CPU, up to nine auxiliary processing units (APU) (Figure 3). Each APU includes a global memory inter-



The Gould CONCEPT 32/8780.

face with its own cache, a memory address translator, a floating point processor, writable control store and an instruction processor.

The CPU loads all tasks within the system and dispatches application tasks to the APU's for execution. Each APU has a general purpose processing unit and a queue of ready tasks that function in a first in/first out fashion via a microprogrammed scheduler. When the APU completes a task, it is placed at the back of the APU task queue and the next task in the queue is initiated.

The high memory bandwidth (64 Mbyte/sec) allows a high DMA I/O throughput. Further, the system performs with an I/O throughput of 40 Mbytes/sec over 4 independent channels. The global memory system of Model 3200MPS supports up to 16 Mbytes of directly accessible memory

implemented on 1 and 2 Mbyte boards with 64K MOS RAMs.

The memory is shared by the CPU and the APU's. In the system organization, the memory is connected to the global memory bus, which consists of two unidirectional, asynchronous 32-bit busses. One bus transfers addresses and data to be written while the other is used for reading data only.

In the recent past, Gould's Concept 32/8780, Perkin-Elmer's 3200 MPS, Harris 1000 and similar computers are competing with IBM 3081 and 3083. The performance comparison is based on specific applications; usually Whetstone values serve as guidelines for comparison. No complete testing method has been developed yet which considers the variables such as cache memory, writable control store and software optimizer. In effect, the

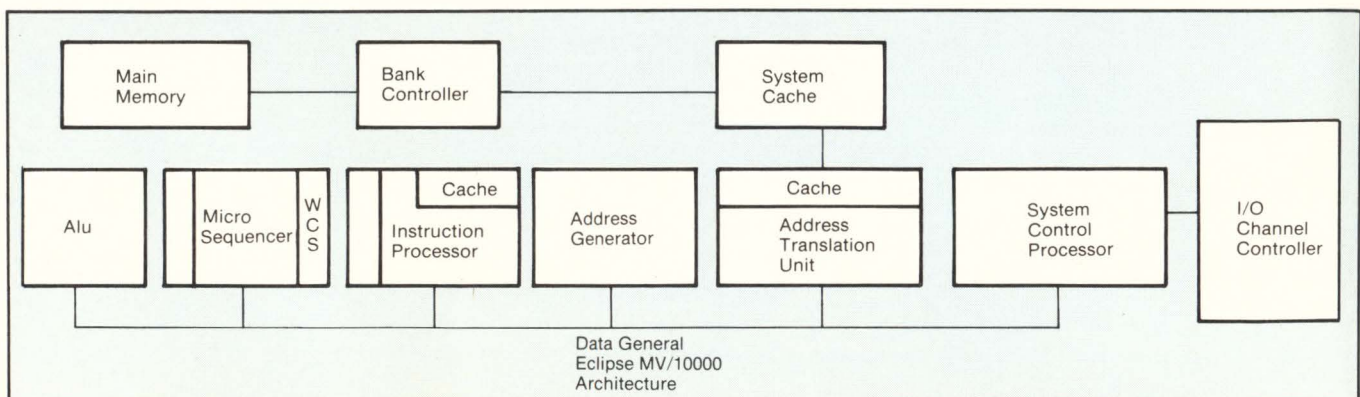


Figure 2: Data General ECLIPSE MV/10000 architecture.

Rx FOR HEALTH

INSTALLMENT TWO



By Lawrence Lee, MD

Dr. Lee is a leading Southern California Internist, specializing in cardiology. He is a co-founder and board chairman of LH Research, Inc. This column is presented as a public service for better understanding of topical medical problems and possible solutions.

HERPES!

SIMPLEX TYPE 1 VIRUS

The Herpes virus most commonly recognized by laypeople is Herpes Simplex, which as we previously stated comes in two types; Simplex-1 (HSV-1) and Simplex-2 (HSV-2). These, along with another type of Herpes called Varicella Zoster, attack the human nervous system.

Herpes Simplex-1 is the virus which most commonly infects the mucous membranes of the mouth, the skin around the mouth and lips, the eyes, and other areas of the body *above the waist*. Other common names for this are "fever blisters", "cold sores", or Herpes Febrilis (occurring with fever in the area of the lips and nose).

HSV-1 can be acquired any time *during childhood*. It appears to be spread by close contact between infected and susceptible individuals, with a normal incubation period (time between contact and clinical signs of the disease) of from 2-20 days, with a mean of 6 days.

Latent infection then occurs, in which the virus remains dormant *within* the body without giving rise to signs of infection. When a *Trigger Mechanism* occurs (such as nutritional deficiency, fatigue, emotional strain, fever, infection, certain diseases, exposure to certain levels of sunlight and other unknown reasons), the virus emerges as an acute infection by migrating from the body of the nerve (Ganglion) in which it has been dormant down the nerve fiber (Axon) to the sensory organ (mouth, nose, eyes, etc.), causing the small blister-like lesions with which we are familiar.

HSV-1 apparently resides *only* within the sensory nerve cells, which conduct impulses *from* the sensory organs (nose, skin, etc.) to the brain or spinal cord. It does not affect motor nerves, which control or stimulate muscle contraction *from* the brain or spinal cord. The most common significant infection caused by HSV-1 is HERPES KERATITIS (inflammation of the cornea of the eye), which can lead to blindness. There are medicines available for its treatment.

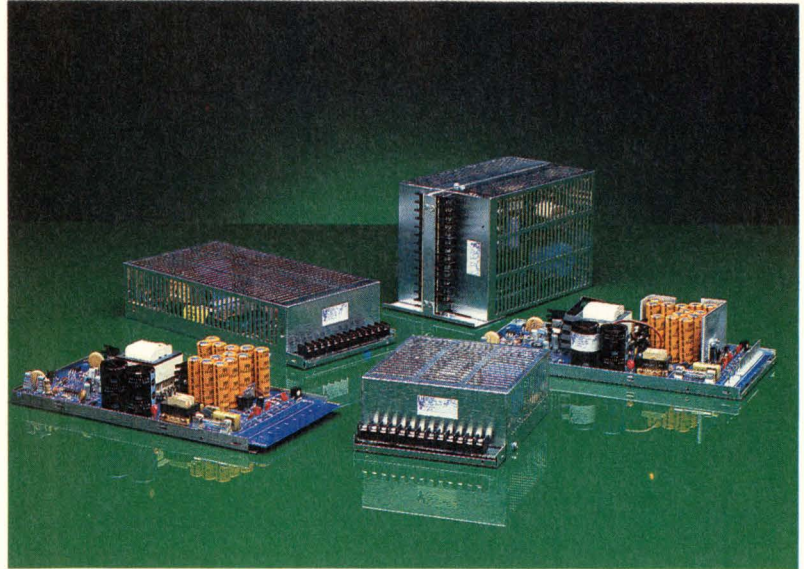
HSV-1 virus are commonly identified by the cluster of small blisters (vesicles), but can be verified by blood tests or fluorescent antibody staining of the tissues. Treatment depends on the site involved. While many different treatments have been tried for HSV-1, including polio and smallpox vaccinations and antibiotics, none have proven successful. One of the best deterrents, however is avoidance of known Trigger Mechanisms. We will cover further advances in treatment, and other types of Herpes virus, in subsequent columns.



The Power Supplier.

This is the second in a series of columns by Dr. Lee on medical subjects of current interest, although perhaps not fully understood, by the public. If you have a question, please write Dr. Lee at LH Research, Tustin, CA 92680.

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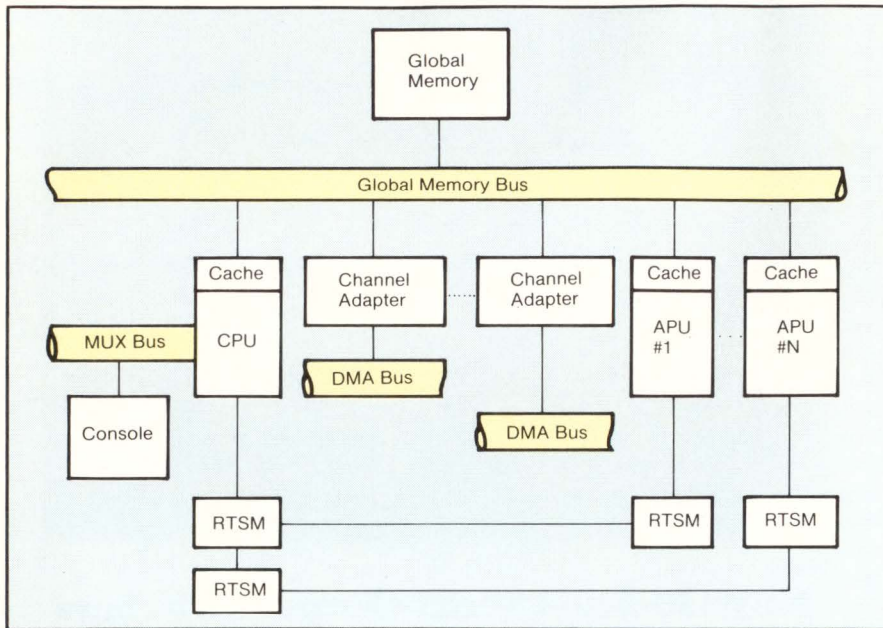


Figure 3: Block diagram of Perkin-Elmer Model 3200 MPS.

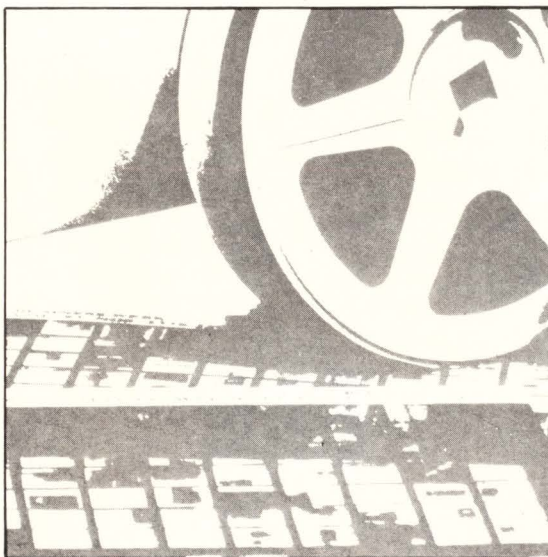
there is market demand for superminis. Even the microcomputer boom and the latest advancements in 32-bit microprocessors are not expected to hinder this market. According to Venture Development Corporation (Wellesley, MA), worldwide shipments will grow at a compound annual rate of a striking 31.9%, thus becoming one of the fastest growth rates for any product in the industry. Further, the market is expected to expand from \$1.2 billion in 1981 to \$4.8 billion by 1986.

Superminis are also broadening into different application areas. These computers were popularly used for time sharing and computational applications. VAX systems even today are very prominent in university research environments. But the growth lately has been in general purpose business and applications such as CAD/CAM. In all, superminis have practically entered in all spheres where large mainframes once dominated. It's just a matter of time to prove the prowess of superminicomputers. □

throughput only serves as a reference and only the application can determine the best suited computer.

The rapidity with which every manufacturer is producing an improved model bears testimony to the fact that

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Photo courtesy Boeing Commercial Airplane Company

Integration Issues For the First All Digital Commercial Aircraft

by Mike Cashman,
West Coast Technical Editor

It was just a matter of time until digital computers began to show up on commercial aircraft and help manage the complex job of flying. After all, digital systems had participated in every other aspect of aircraft development, design, and testing.

For a long time, it appeared that the transition from the purely hydraulic and analog world of flight management would occur in the mid '70s with the development of the American supersonic transport. Together with NASA, the Boeing Commercial Aircraft Company set out to define the requirements of operating large commercial aircraft routinely and safely at speeds approaching 2,000 mph. A great deal of effort was put into developing an array of digital instruments that would help manage this ambitious goal.

The aircraft which finally became the first all-digital commercial airplanes, according to the Federal Aeronautics Administration are the Boeing 767 and 757 currently entering service.

Digital Alternatives

The number of ways digital systems

The ability to quickly and accurately diagnose conditions and potential problems prompted the move to digital systems.

can be used on board an aircraft to improve its operating cost is relatively limited. Systems might be used to:

- decrease the weight of subsystems, and therefore the overall weight, and thus effect a reduction in the amount of fuel required to lift the structure
- improve the flight crew's ability to manage fuel consumption parameters in flight
- provide additional levels of detail in general flight-oriented information that would decrease fuel utilization.

Indirectly, digital systems would provide other advantages by:

- improving specific and general

systems reliability

- improving flight safety
- making comprehensive maintenance checks easier and more accurate.

There is one more strong advantage to using on-board digital systems strictly from the overall designer's viewpoint. Systems can be "soft designed" to enable tuning and potentially optimum performance.

Before a digital airplane could be built, however, an almost unparalleled degree of cooperation would be required among the manufacturer and the customer. Contrary to airline desires in the past, they would have to agree to, in effect, obsolete their spare parts inventory for almost every system that would be aboard the new airplanes. And this was a basic requirement during a time when the airlines were not at their healthiest. There was also the question of whether the airlines could agree on what the characteristics of an on-board digital information interchange standard should be.

On these questions, Aeronautical Radio, Inc. (AIRINC) played a key role. This organization, which is principally known for the worldwide inter-airline communications net it operates, was able to define

Product Index

To help you find the products you need, we've compiled a subject index of the ads and new products that appear in this issue. Organized by general product area, the listings include the name of the manufacturer, the page on which the product appears and a write number for additional information on that product. Bold type indicates advertised products.

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the 429 Digital Information Transfer System. This is an asynchronous standard designed for the requirements of commercial transports. It operates at 12.5 KHz and 100 KHz. Once the airlines had agreed on the inventory issue, had agreed on the AIRINC 429 DITS standard, and had indicated interest in the new fuel-efficient aircraft, engineering and design on the new planes swung into high gear.

The result is that when you fly aboard one of these craft today, you are flying alongside approximately 139 on-board computer systems on the 767, and slightly more than that on the 757.

The computers are everywhere—at least in function. As one might guess, they're in the cockpits to a greater extent than ever before in commercial planes. But they are also used in some perhaps less suspected applications. They monitor the pressure and temperature in all areas of the cabin. They are regulating power flow automatically to adjust to flight requirements and generator performance. There's

more than 1.5 Mbytes aboard in RAM and ROM; more is stored in non-volatile disk memory.

Evaluating Vendor Designs

Modern aircraft are too complex for one manufacturer to build totally. Many subsystems are subcontracted, with the major manufacturer/integrator issuing a generalized set of specifications and then tightening the specifications as the design firms up.

When guidelines for the 767's landing gear were issued, they were sufficiently generalized to allow a number of alternative design approaches. One of the most important functions of the landing gear is to provide anti-skid capabilities. Previous systems used by Boeing had been analog in nature. According to John Ward, Boeing Commercial Airplane Company's senior project engineer for systems, there was no bias at the outset of procurement toward an analog or a digital solution. However, the supplier submitted an analog design "that wasn't tremendous." The ven-

dor was also working on a prototype for a digital system, and Boeing wanted to test both designs in its landing gear analysis laboratory.

Two aspects of the digital landing gear design led to its being chosen over the conventional analog design. The system's timing was much superior to the analog version, and there was a built-in capability for easier and more comprehensive maintenance and testing.

Additional On-Boards

The ability to quickly and accurately diagnose conditions and potential problems was another advantage seen by the airlines in the move toward digital systems. An airliner thrown off schedule for an hour can create havoc in airline scheduling departments and potentially lose the operation thousands of dollars.

An optional system called the ARINC Communications Addressing and Reporting System (ACARS) is a development aimed at improving maintenance quality.

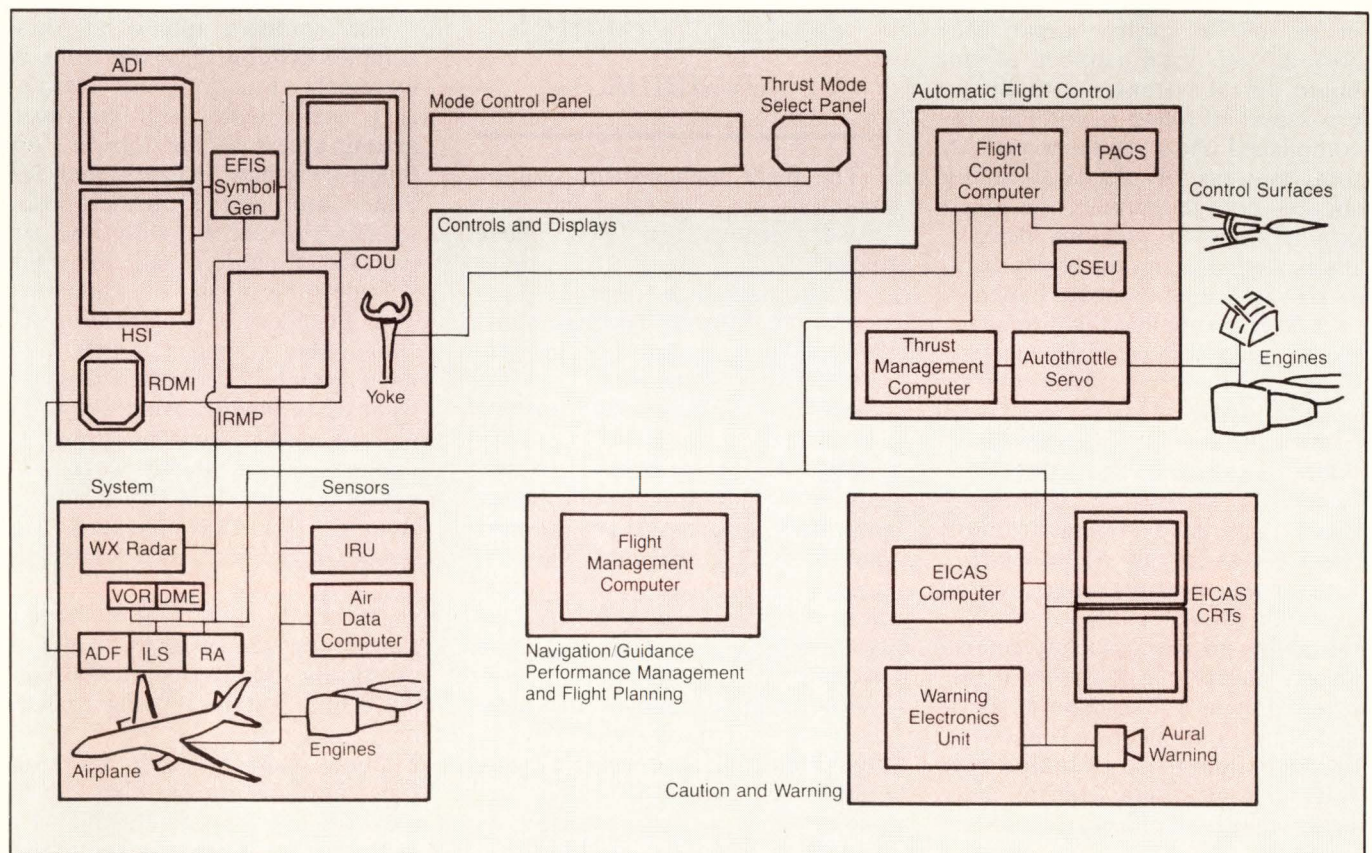


Figure 1: Schematic diagram of flight management computer system.

This Teledyne-supplied TI-9900-based 16-bit micro can relay aircraft performance parameters from a variety of systems over a radio link to ground maintenance engineers. Maintenance personnel will thus have access to data regarding selected anomalies as they occur under load, rather than from reading cryptic flight-log write-ups.

Other micros monitor the power circuitry, protecting digital buses against surplus voltages or under frequency power. They are also charged with the task of automatically shedding non-essential loads in the event of a generator failure. This capability made it possible to direct a larger percentage of available power to the aircrafts' galleys so that meals could be cooked faster.

Additional systems are responsible for window heating, air conditioning unit temperature control, ice detection, and other non flight management system-oriented functions.

On The Flight Deck

The number of digital systems used in the 757/767 cockpits approaches 50% of the total number of on-board digital systems. Virtually every aspect of flying is normally accomplished under digital control. A total systems or electrical failure should not jeopardize the flight critically; as in previous designs, the new planes can proceed a limited distance using on-board batteries.

A Sperry-supplied flight management computer performs navigation, real-time automatic performance optimization, and can control the craft through the autopilot, autothrottle and other components of the system. This capability may have dramatic future implications for air traffic control, for it makes possible what is called four-dimensional guidance. This is the ability to automatically control an airplane so that it arrives at specific points in a flight plan at specified times and speeds. This development would make possible easier and safer air traffic control practices as well as increased system capacity.

The ARINC 429 digital informa-

tion transfer system bus consists of approximately 122 twisted, shielded pair interconnections between the flight management system components. Each subsystem uses a separate bus. The flight management computer and the electronic flight instruments each listen on 23 busses. Some non-flight management systems, including the anti-skid and the flap control systems, also use the 429 standard. Additionally, a 1 MHz ARINC 453 bus is used between the weather radar receiver/transmitter and Electronic Flight Instrument System to enhance the weather radar image in the cockpit.

The number of digital systems used in the 757/767 cockpits approaches 50% of the total number of on-board digital systems.

The flight management system's functions are segmented into four closely integrated sets. These include:

- automatic flight control
- performance management, guidance, and navigation
- crew operation, and
- advisory, caution, and warning display.

The philosophy behind the system is to monitor virtually every important aspect of flight progress and only alert the crew when an anomaly occurs, or to add information regarding any selected task that might assist in decision making.

For example, one of the flight deck subsystems is called the engine indication and crew alerting system, EICAS. This system replaces panels of engine gauges by displaying, often in graphic form, important performance parameters.

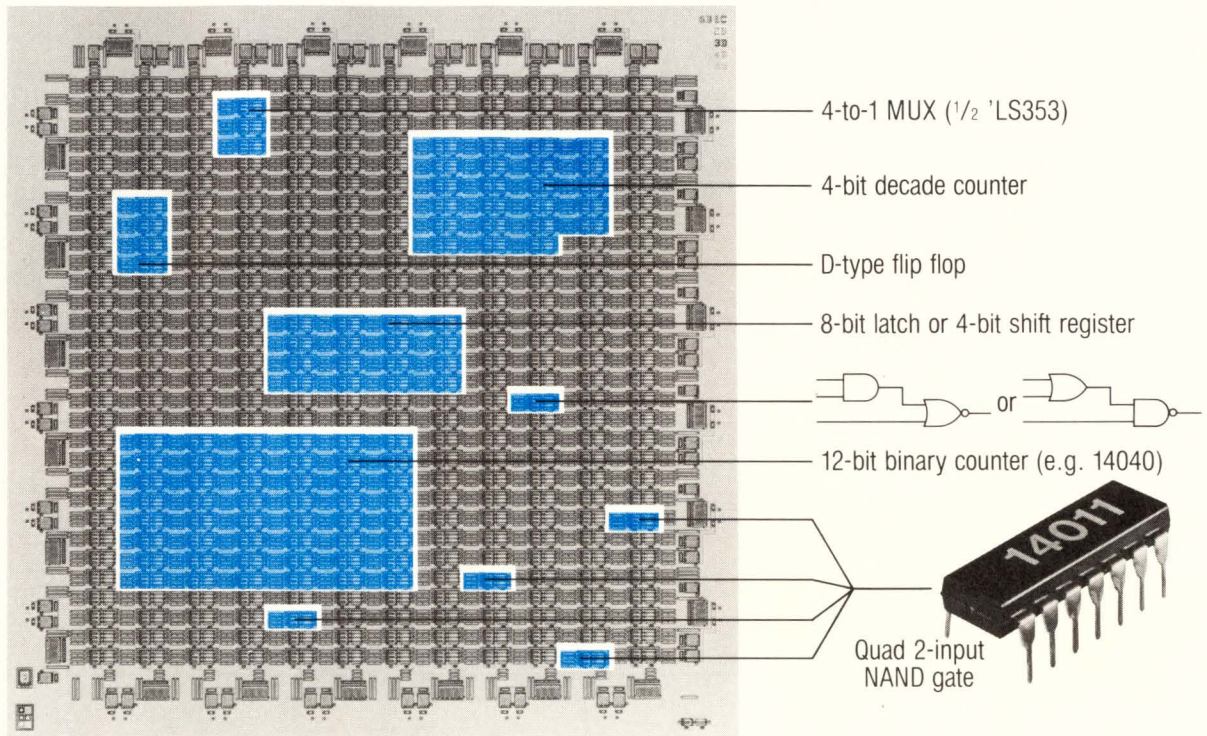
The upper screen in the cockpit (see photo) is reserved for important information. During takeoff, for example, the display shows critical engine thrust readings a semicircular graphics, complete with color coding, much like a conventional instrument. Additional textual information is displayed as well.

The lower display can show a number of incidental displays. For example, digitized Jeppesen charts, analogous to roadmaps for pilots, can be displayed showing the correct procedures for approaching and departing hundreds of airfields.

Sometimes it seems that systems like EICAS work almost too well. The logical design for the unit calls for the system to "latch" or continuously display anomalies for crew evaluation. This has happened to the EICAS, which has "latched" an out-of-boundary engine reading even though the event was spurious. This is just one of what promises to be numerous software modifications until the digital systems are thoroughly tuned.

The software tuning of these complex systems turns out to be an extremely touchy issue: Boeing isn't comfortable with customers getting access to the software on-board their new airliners, and customers are "united" in their desire to gain this access. Only one airline, Delta, chose to talk about this volatile subject, and the company's Vice President of Engineering, C. Julian May commented that "like most people, we want to know what we're buying. We'd like to be able to modify some programs, to understand how things work, and get a feel for how it operates." Boeing's Ward commented that tamper proof seals is a subject of not insignificant interest within his organization. And as far as the fear that airlines are going to be able to drastically modify operational coding, "that just isn't going to happen," according to the F.A.A.'s Edmund Ross. "There are strict procedures set up on what can be touched and what can't, and what recertification testing is required." □

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Write 84 on Reader Inquiry Card

Controller Overcomes Disk Inefficiencies

Today, a typical disk subsystem is not run efficiently under UNIX and its look-alikes. For file-oriented transactions in which files consist of multiple contiguous disk sectors, the operating system usually asks for only a single sector, or, at most, a block of a few sectors at a time. Each time a sector or block is transferred, all the overhead associated with setting up disk access is incurred.

A solution can be found in the SMD 2190 high-performance disk controller from Interphase Corporation (Dallas, TX). The SMD 2190, featuring UNIX-optimized firmware, is the first third generation hard disk controller. According to Michael Cope, Interphase's president, what makes the 2190 so advanced is the added cache memory as well as an intelligent caching scheme. The scheme can be customized for different operating systems and application mixes. Cope predicts that over the next few years, "all the state-of-the-art controllers will adopt this caching concept."

Traditionally, a high-performance disk controller has been built on a design for maximum speed so the disk that is contiguously formatted can be accommodated; the process is known as 1:1 interleave. But UNIX cannot efficiently use a disk that is contiguously formatted because it typically asks for data only one sector or block at a time. By the time that first sector is retrieved, the next sequential sector will have already passed under the head. As a result, any controller using this approach has not been able, under UNIX, to retrieve more than one sector or block per revolution, thus degrading performance.

The SMD 2190 formats the disk in programmable groups of contiguous sectors. Each logical group's size can be varied to fit requirements of the operating system and application. In most applications, the disk will be formatted contiguously, all the way around. But in other situations, groups themselves can be interleaved, if needed, to accommodate special operating system characteristics.

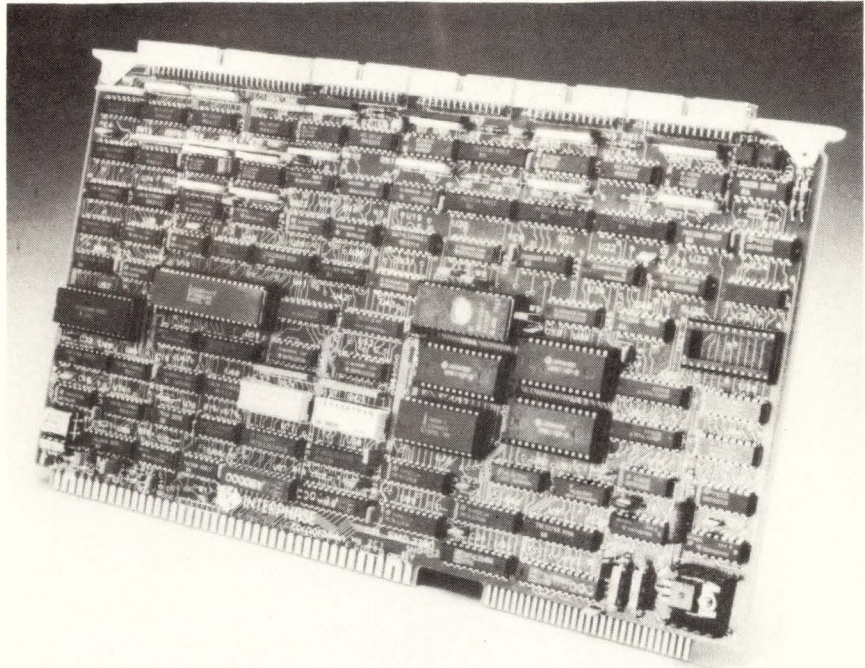


Figure 1: The SMD 2190 is a high-performance, UNIX-optimized disk drive controller for Multibus-based systems.

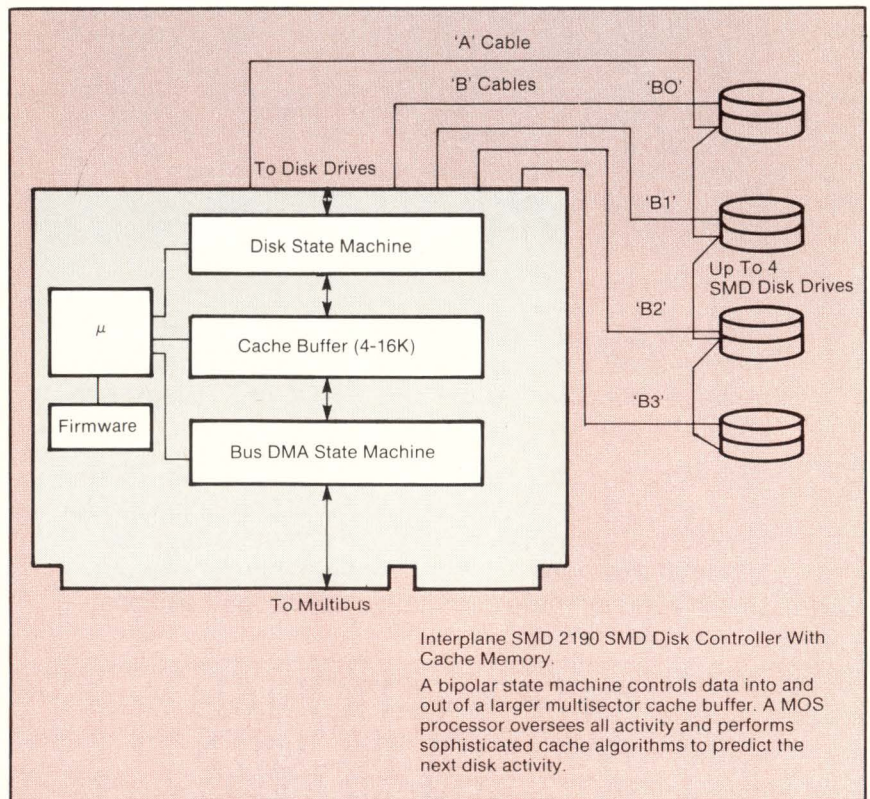


Figure 2: A bipolar state mechanism controls data into and out of a larger multisector cache buffer. A MOS processor oversees all activity and performs sophisticated cache algorithms to predict the next disk activity.

With the Interphase disk controller, the operating system accesses data normally. But the 2190 also automatically predicts what data will be accessed next, and retrieves that as well — a process known as pre-fetching. Cached in the controller's memory, data is available immediately when requested by the operating system. Since most transactions are file-oriented, throughput rates are significantly increased.

On the other hand, for some transactions such as demand paging in virtual memory systems, caching may not be desirable. For that reason, the SMD 2190 offers a selective override capability that allows reading on a non-cached basis.

Another feature of the 2190 is its direct Mode. Designed for special-

ized high-speed data acquisition applications, Direct Mode bypasses the controller's on-board buffering and provides a direct connection between the bus and the disk. This allows a full track of information to be transferred for each revolution of the disk. Spiral formatting allows multi-track operations to occur without missing a disk revolution.

The SMD 2190 is compatible with hardware systems using Intel's Multi-bus. The 2190 supports microcomputers based on the Intel 8085/8086/8088; Motorola 68000; National 16000 and many other popular CPUs.

Occupying a single slot in a micro-computer chassis, the controller features high-speed DMA with full 24-bit addressing; disk data rates to 20 Mb/s; automatic error correction;

overlapped seeks and other features. The SMD 2190 controller is compatible with a wide range of SMD drives, from suppliers such as Control Data, Fujitsu, NEC and Ampex.

The programmer's interface to the SMD 2190 is accomplished through the simple concept of an IOPB—a memory based control block containing macro-level commands and parameters.

Available now to OEMs, the SMD 2190 costs under \$1000 in single quantities. Interphase will also provide complete SMD subsystems, including the SMD drive, the 2190, cables, termination block, manuals and, as an option, software drivers.

— Interphase Corp.

Write 235

LSI Error Correction Hardware Provides Up To 28 Mbytes ECC Memory

The MegaFrames distributed intelligence architecture is a significant advance from the shared logic attempt at providing a single CPU for multiple users.

The MegaFrame, from Convergent Technologies' Data Systems Division, is a system of multiple processing units tied together on a high speed 32-bit wide, asynchronous bus. Each of the processing units on the bus consists of a CPU and memory; most also have I/O interfaces. The bus can be extended across multiple enclosures, each with a 6-slot backplane, up to a maximum of 6 enclosures for a total of 36 slots. Each enclosure supports integral mass storage.

The system in its largest configuration contains as much as 24 Mbytes of memory. This large amount of memory is also the largest contributor in decreasing the systems mean time between failure MTBF rate. This system would have a single bit memory error every 24 days without any form of error correction. The failure rate of all the other hardware excluding memory is approximately 625 days. By adding error correction logic, the memory MTBF rate can be

(continued on p. 113)

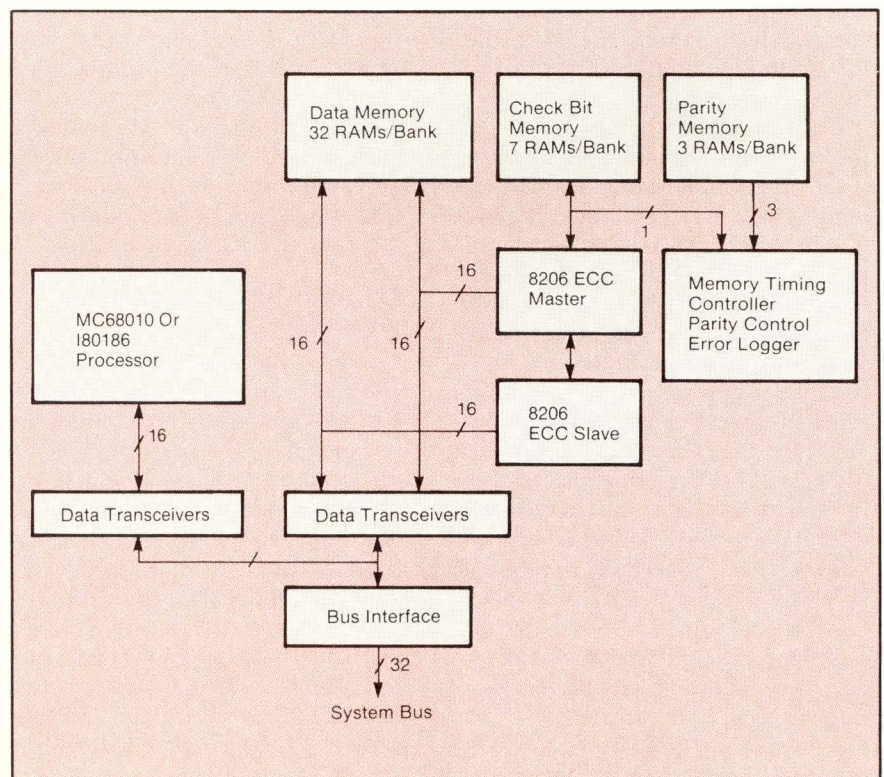


Figure 1: The memory block diagram. The seven check bits are required for double detect/single correct of 32 bits of data. The three parity bits are used for fast determination of single bit errors. Since one of the seven check bits computes byte parity, it is also used as the fourth parity bit. Transceivers control the multiplexing between the MC68010 or I80186 and the 32 bit memory.

Expanding The Bandwidth Of Optical Fiber Systems

Major advances in op-amp performance made in the last decade were related to transistor and processing technology. Great strides were made in reducing noise, offset voltage and current through the use of JFETs and clever front end designs. New transistors made possible higher voltage and power handling capacity. Although monolithic op-amps were able to increase in bandwidth and slew rate by an order of magnitude, they still cannot be considered to be high speed in the view of today's signal processing needs. The hybrid op-amps that were once able to meet these needs have not kept up the pace. Some manufacturers have begun using microwave transistors in their op-amps to try to boost bandwidth, but the result is barely noticeable when compared to such mainstays of the last ten years as the 3554 and 0032. The limitation is not the transistors, but the design.

To achieve another factor of ten improvement in bandwidth and settling time Comlinear Corp. (Loveland, Co.) felt a totally different design topology was needed. Transit time of the signal through the amplifier needed to be reduced to increase the phase margin for better pulse response and greater stability. Traditional designs gave rise to transit times of several nanoseconds, and at 100MHz 3ns of delay is 108 degrees of phase shift. Therefore, the number of stages of gain in Comlinear's CLC103 amplifier had to be kept to one (this also reduced the number of poles by avoiding extra stages) yet high open loop gain could not be sacrificed either. The level shift stage had to be incorporated into this gain stage as well, to reduce delay.

Previous designs were critically sensitive to compensation, and it was often difficult to prevent oscillation let alone achieve good pulse response. At the higher frequencies of operation contemplated by the CLC103 designers, stray reactance in pc-board

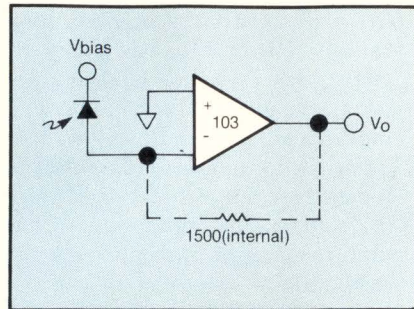


Figure 1: the circuit has a gain of 1500 V/A and is DC coupled.

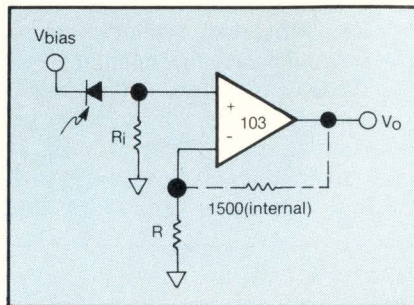


Figure 2: Circuit provides higher gain.

traces alone made external compensation impractical, so a way had to be found to optimally compensate the op-amp for all gains, inverting or non-inverting, on chip. Finally, the entire op-amp needed to be DC coupled throughout. A technique such as AC feed-forward was not acceptable because it reduces non-inverting gain performance and increases overload recovery time.

Using A Transimpedance Amplifier

For high speed operation at up to 150MHz and medium gain, the CLC103 can be used in the transimpedance mode. The circuit in **Figure 1** has a gain of 1500V/A and is DC coupled. Since the diode sees a very low impedance "virtual ground" at the inverting input, diode capacitance does not reduce the bandwidth. For higher gain, the circuit in **Figure 2** provides higher gain, equal to: $v_o/i_d = R_i(1 + 1500/R)$. In this situation, diode capacitance C_d will act with R_i to reduce the bandwidth to $(2\pi R_i C_d)^{-1}$.

"Bootstrapping" A Solution

A "Bootstrapping" technique allows a photodiode to drive a high impedance load (in order to increase gain

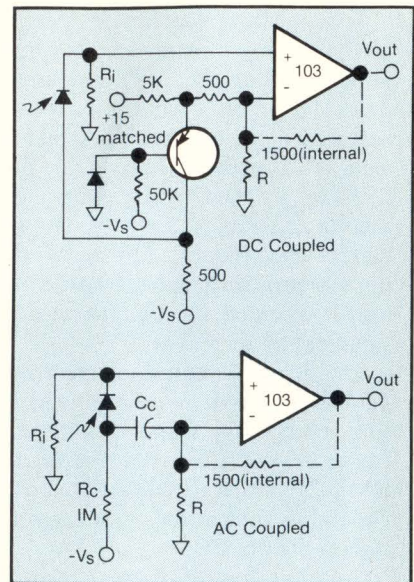


Figure 3: DC and AC coupled versions of the circuit.

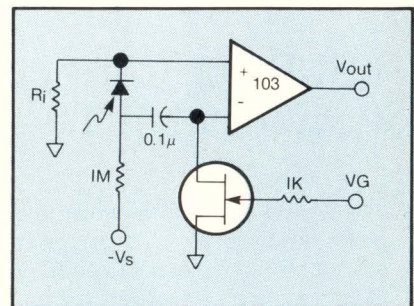


Figure 4: The CLC103 can also be used for voltage-controlled gain by substituting an FET for the gain resistor.

and reduce noise) without suffering from the typical bandwidth reduction caused by the combination of R_i and C_d . Bootstrapping causes the voltage across the photodiode to remain constant, even though the voltage $i_d R_i$ at the amplifier input is changing. Thus, C_d does not see a net change in voltage and no charging or discharging of C_d occurs. This allows much wider bandwidth, even at high gain set by $R_i(1 + 1500/R)$. **Figure 3** shows DC and AC coupled versions of this circuit. In the AC coupled circuit, the low frequency -3dB point is $(2\pi R_i C_d)^{-1}$.

The operation of the DC coupled circuit can be understood by noting that for an incremental increase in the voltage across R_i due to i_d , the inverting input voltage of the CLC103 will increase by the same amount since it

is a "virtual ground" with respect to the non-inverting input. This same increase in voltage will also be seen at the collector of the common base transistor. The AC coupled version functions similarly except that its high frequency performance will be slightly better since there is less time delay of the signal through C_c than there is through the transistor.

Comlinear op-amps have a unique circuit topology which gives them a factor of 10 higher performance than other high speed op-amps and which makes it possible to bootstrap a photodiode. To attempt this with an ordinary op-amp would be futile.

A potential problem with this bootstrapping technique is the medium-level noise that may be too high for some very noise-critical applications. For example, with $R_i=750$ ohms and $R_{gain}=100$ ohms, the noise floor (from several hundred KHz to 100MHz) is -127 dBm (1Hz) measured at the output.

Voltage-Controlled Gain

The CLC103 can also be used for voltage-controlled gain by substituting a FET for the gain resistor, as shown in **Figure 4**. In this circuit, the FET is used as a voltage-controlled resistance for setting gain.

This circuit also works well without a diode (delete R_c and C_c as well) across the CLC103 inputs, so it could be used as an AGC stage following the initial transimpedance stage. To do this, simply disconnect R_i from ground and connect it to the voltage to be amplified. The gain will be $(1 + 1500/R_{DS})$, where R_{DS} is a function of V_G . A GaAs FET would work well in place of a JFET, since capacitance is an order of magnitude lower, thereby reducing peaking, and R is smaller, allowing higher gain and more dynamic range. Noise would be much worse as well, however. (To protect the CLC103 from damage from excessive current into the inverting input, refer to the section on protection in the CLC103 data sheet.)

As fiber optics systems continue to proliferate, new products and techniques will have to be developed to meet the demanding requirements in this field.

— Comlinear Corp.
Write 238

(Continued from p. 111)

increased to above that of the remaining hardware. The resultant system MTBF is then limited by the non-memory components.

For a system to run at a failure rate higher than the memory failure rate it is necessary to correct all single bit errors. Double bit errors are detected and treated as a catastrophic system failure.

To be able to detect errors, it is necessary to append additional bits of information to the data. Parity allows single bit error detection with only one additional bit of information but gives no clue as to the bit in error. Data correction requires that the appended bits contain information to indicate which bit is in error, including the appended "check bits." A 32-bit data word would then require at least six bits to indicate which of the data or check bits was in error.

One of the encoded check patterns is reserved for indicating no bits are in error. To detect two bits in error requires one more check bit. Seven check bits are therefore required for double bit error detection and single bit error correction. The encoding method proven to be the most efficient for double detect single correct codes is a modified version of the "Hamming" code. The implementation of this code is done by computing parity over specific combinations of data bits to generate a check bit pattern. The check bit pattern is then stored along with the data. Upon reading, the check pattern is again computed and compared to the check

bits retrieved. The result of this comparison is a syndrome word which indicates that zero, one, or two or more bits have changed. Since, for a single bit change, the syndrome can indicate which bit has changed, error correction may be performed by simply inverting that bit.

Figure 1 is a block diagram of the memory system. The memory array uses 64K RAM chips organized into two banks each 32 bits wide. Seven RAM's are required for each bank to store the ECC check bits. Two Intel 8206 Error Detection and Correction chips are cascaded for 32 bit operation. One 8206 is designated as the master and is connected to the check bits. The other 8206 is designated as the slave and passes partial parity information back and forth to the master. The modified Hamming code used in the 8206 allows the master and slave to compute partial parity over their respective 16 data lines. The partial parity is combined in the master to produce the syndrome, then supplied to the slave for data correction information.

A data width of 32 bits was chosen for the system bus and memory primarily to support DMA operations and to provide an easy upgrade path to 32-bit microprocessors. By making the memory data width 32 bits instead of 16 bits reduces the number of memory chips required to support ECC for large memory arrays.

— John Burger, Hardware Engineer,
Convergent Technologies Write 236

Letters

Alpha Data Inc.

Dear Sir:

The article, "Solid State Disks Optimize Throughput" (*Digital Design*, October, 1983), was very interesting, however, we are unhappy to note the absence in the chart on page 97 of any reference to our company's products. Briefly, our M/CORE mass memory is directly competitive with the Ampex Megastore.

James S. Howard
Sales Manager

Alpha Data Inc.
20750 Marilla St.
Chatsworth, CA 91311

Correction

In the Printer Manufacturers list following our feature "Keeping Pace With Printers" in *Digital Design*, September, 1983, we omitted Datel (Mansfield, MA). Datel manufactures 7-, 20- and 48-column direct thermal panel-mount printers, including MIL spec printers for mobile use.

PERSONAL COMPUTER

64-128 Kbyte Memory

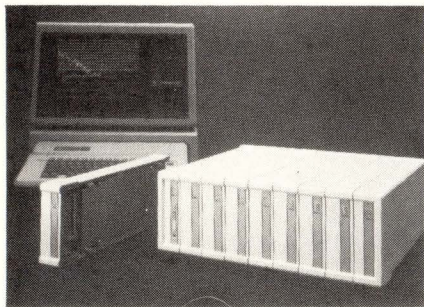
The PCjr, dubbed the Peanut, is the newest product in IBM's line of personal computers. The PCjr is offered in two versions with a \$600 cost difference. The lower priced system has a cordless infrared keyboard, uses cartridge programs, and has 64 Kbyte of memory. The higher priced version has 128 Kbyte of memory and diskette application programs as well those on cartridge. The computer features a 16-bit microprocessor and microchip technology. (The game controller, serial port, light pen interface, and colorgraphics are located on the main circuit board.) Also included are power-on self test diagnostics and individually programmed keys. Options for the PCjr are



an internal communication device, thermal printer, joysticks, and software programs. The computer is compatible with many diskette programs written for other IBM personal computers. The two versions cost \$669, and \$1269. **IBM**, Delray Beach, FL **Write 146**

CONTROL SYSTEM

Eight I/O Modules A/D



The Acrosystem-800 combines a 8088 microprocessor driven front end with the Apple personal computer for automated test, data acquisition and control applications. It is modular and provides isolated floating inputs and outputs for noise immunity. The system's configuration consists of a DC supply and a microprocessor control module on either side and 8 I/O modules in between. Any combination of I/O modules is permitted. Standard Apple software is required for operation of the system. The system offers general purpose, thermocouple, integrating, and RTD input modules. Price is \$650, to \$1,000. **Acrosystems**, Beverly, MA **Write 137**

SUPER MICROCOMPUTER

Independent I/O Processor

The Pixel 80 super microcomputer system features an MC68000 microprocessor CPU with an independent I/O processor. The system includes 6 Mbytes of main memory, separate controllers for graphics, diskette or Winchester-disk storage and communications. The system provides eight terminal ports, eight RS-232 serial ports and two parallel printer ports. Operating system software includes UNIX and the system supports 13 computer languages. Price is \$14,000. **Pixel**, Wilmington, MA **Write 140**

FAULT TOLERANT SYSTEM

Supports 24,000 Users



The Eternity Computer System provides fault-tolerant operation for on-line transaction processing applications. The system supports from six to 2,400 users. Each computer module contains two 32-bit 32032 microprocessors. One microprocessor runs UNIX and the other, a real-time I/O processor, controls I/O transactions on line. The modules have one Mbyte of main memory, with options available for expanding to 16 MB. A (64-bit) memory bus connects all modules which may have one or two I/O channels. Each channel supports 15 peripherals and/or communication processors. Price is \$74,000. **Tolerant Systems**, San Jose, CA **Write 134**

GRAPHICS SYSTEM

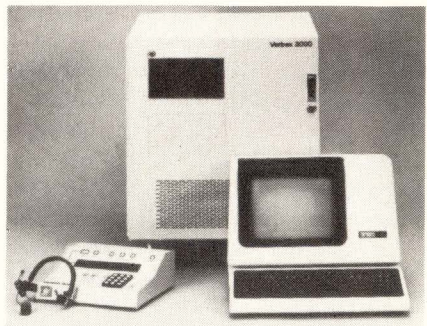
1024 x 1024 Resolution

The Whizzard 3355 2D graphics system is software compatible with the Whizzard 1600 and

7200 microcomputers. The system features a 1024 x 1024 pixel, 60 Hz non-interlaced raster scan monitor and a 12-bit (4096 x 4096) virtual addressing system which allows pixel access to the memory mapped display. The system can simultaneously display 16 colors from a palette of 4096. Optional features include a surface fill processor, a graphics digitizer tablet, color hard-copy and additional memory. Price is \$22,500. **Megatek**, San Diego, CA **Write 138**

TERMINAL

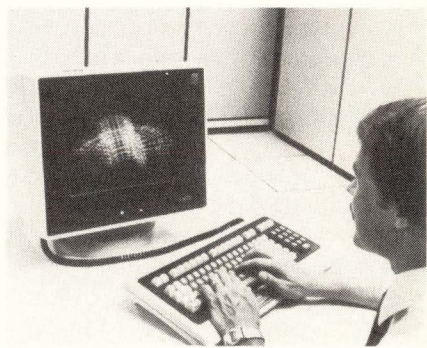
Features Interactive Prompting



The Spads terminal is a I/O computer peripheral which allows users to develop and implement customized continuous speech voice data entry applications. Users can design applications-specific vocabularies containing 120 words (with options to 360 words). The Spads terminal features interactive prompting and a testing capability for successive levels of development. It provides evaluation reports of vocabulary as well as enrollment and training scripts. A digitized voice response is included. **Verbex**, Bedford, MA **Write 136**

PARALLEL PROCESSOR SYSTEM

16 billion Calculations/Sec.



The Cyberplus parallel processor system is designed for such applications as simulation, large-scale structural analysis, petroleum exploration, aerospace, manufacturing, weather forecasting, research and image and signal processing. 64 processors can be linked to one 800 Series computer. The system's ring concept interconnects 16 processors to form a communications channel capable of transferring data at the rate of 800 million bits/sec. Four rings can be linked to one Cyber 800 system. **Control Data**, Minneapolis, MN **Write 128**

COMPUTERS/SYSTEMS

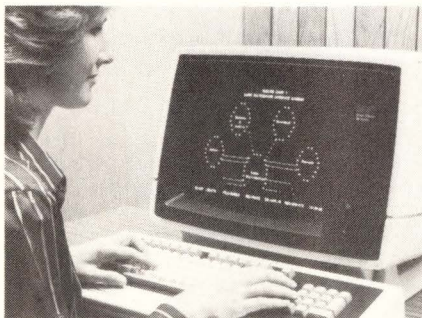
GRAPHIC DISPLAYS

1024 x 784 Resolution

The 1015 graphic display has a 640 x 490 resolution and is compatible with the Tektronix 4010, 4012 and DEC terminals. The 2015 and 2019W feature 1024 x 784 resolution and have a scrolling multi-page text memory. Options include a vector generator and local graphic commands. Price ranges from \$3,250-\$10,950. **Westward**, Cambridge, MA **Write 127**

SOFTWARE DEVELOPMENT SYSTEM

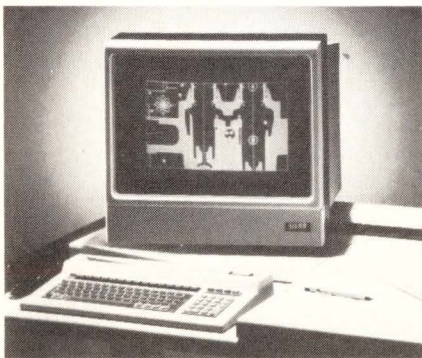
Supports 24 Workstations



The Maestro is a software development computer system which supports phases of development from system specifications through final release. It provides word processing, text editing, electronic mail, automated calculator, information retrieval and project management. Syntax menus are available for COBOL, FORTRAN, PL/I, and other languages. The Maestro supports 24 workstations and has a standard configuration consisting of a CPU, 480 Kbyte memory, 24 Kbyte NP/80 memory, disk controller, two 67.5 Mbyte disk drives, 450 LPM line printer, two communication controllers and a software license. Price is \$197,000 **Four-Phase Systems**, Cupertino, CA **Write 135**

GRAPHICS WORKSTATION

1448 x 1024 Resolution



The S6100 Series of graphics workstations provides local GKS standard graphics display primitives with individual or bundled attributes, segmentation, workstation transformation and an integral GKS input model with logical device support. The S6100 Series operates in both the Lundy native and the Tektronix 4014 emulation modes. The workstations feature a Motorola M68000 processor with a 20" diagonal color or

monochromatic monitor (1448 x 1024 resolution), detachable keyboard and automatic self-diagnostic routines. **Lundy**, Glen Head, NY **Write 131**

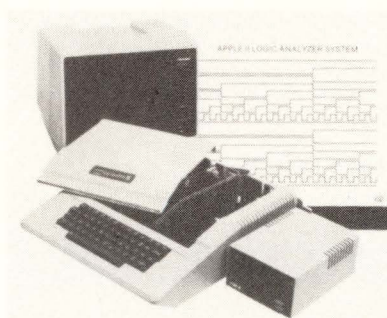
COLOR GRAPHIC TERMINAL

16 Color Palette

The CGT 680 color graphic terminal can be used as a stand-alone workstation, computer terminal, or as a front end to a CAD/CAM system. In the graphic mode, the CGT 680 displays 16 colors from a palette of 512 in a 640 x 480 format. In alphanumeric mode, the CGT 680 displays 48 lines of 80 characters. Double height/double width characters are supported, as are blink, reverse video and underline. The 8MHz Motorola 68000 processor is equipped with 4 Kbyte RAM and 16 Kbyte EPROM. The CGT 680 VME 4-slot backplane contains two expansion slots for floppy disk, Winchester disk, digitizer, additional memory, or plotter. Two synchronous/asynchronous I/O ports are capable of supporting SDLC/HDLC. **General Digital Industries**, Huntsville, AL **Write 129**

LOGIC ANALYZER SYSTEM

1024 Word Memory



The LA-100 is a hardware/software system that converts the Apple II computer into a logic analyzer. It is comprised of a plug-in card, connector cable, and software. The LA-100 includes a 16-bit data path, 1024-word memory, and clock inputs. A 16-bit trigger word allows data collection to begin with or without a programmable delay. The system stores and recalls data and instrument setups using the Apple disk system. Price is \$795. **Total Logic**, Ft. Collins, CO **Write 130**

SOFTWARE

For Emulating IBM 3270

Micro/Remote 3270 software allows any microcomputer to emulate an IBM 3270 mainframe computer terminal. It is designed for software developers who wish to build integrated access to mainframe data bases into a micro based product; users access the mainframe's data bases through a screen buffer which contains the 3270 data translated into ASCII. The local program can examine the virtual screen buffer after a screen image is received, modify it and transmit it to the mainframe on the next poll. The emulator

program is modular and available in source form to OEMs. Minimum memory requirements in the ROM configuration are 15K ROM and 6K RAM. **Aton**, Santa Clara, CA **Write 143**

16/32-BIT COMPUTER SYSTEM

With 256 Kbytes RAM

The SBE 200/10/F is a 68000-based computer system with floppy and hard disk storage and a Multibus expansion capability. It is compatible with several operating systems, including Unix. The SBE 200 has a 10MHz 16/32-bit microprocessor, 256 Kbytes of RAM, parallel I/O, dual multiprotocol serial I/O, and Multimodule/IEEE P959 compatibility. Other features include two RS-232C serial ports for connection to the system terminal or printer, 24-bit parallel I/O configured as a printer port, triple counter timer, and two 8-bit iSBX Multimodule connectors. **SBE**, Palo Alto, CA **Write 144**

OPERATING SYSTEM

Unix Compatible

uNETix is a multi-tasking operating system that is compatible with UNIX software and is designed for the networking of microcomputers. Three versions are available, a stand-alone system and two networking products. uNETix has the capability to run 10 applications simultaneously and to transfer data between windows through its internal memory. All versions have an MS-DOS emulator and are compatible with UNIX software. **Lantek**, Sunnyvale, CA **Write 133**

GRAPHICS PACKAGE

For Industrial Applications

Classimate II is a hardware/software color graphics package designed for industrial graphics applications. The system consists of three devices, a color monitor, development keyboard, and an IDT-2200 video processor. Its graphics development package includes a mass store unit with a 10 Mbyte Winchester disk drive. CLASSIMATE II can simulate animated PC graphics without being connected to a PC. **Industrial Data Terminals**, Westerville, OH **Write 126**

COMMUNICATION CO-PROCESSOR

With 48K Buffer

The Envax 600 is a communication co-processor that allows the IBM PC to communicate with several networks. The 600 is connected to the serial communication port of the IBM PC and the software supplied is copied to the system disk. It has a 16 or 48K buffer, 103/108 or 212 modem, directory, editor, forms generator, delay transmission, and automatic sending and receiving. Price is \$1,395. **Envax**, Irving, TX **Write 142**

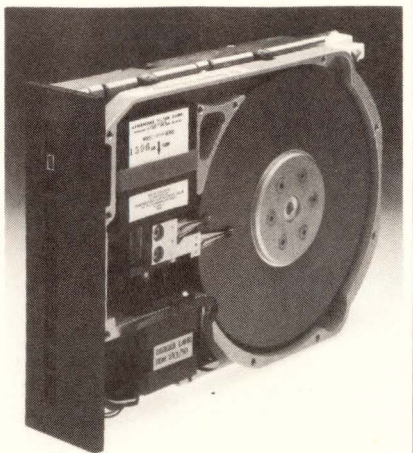
NEW PRODUCTS

PERIPHERALS

WINCHESTER DISK DRIVE

12 Mbyte Capacity

The ST212 is a single platter, 12 Mbyte Winchester disk drive developed by Seagate Technology for portable computers and desktop systems. Because it utilizes minislidder ferrite read/write heads, it is capable of withstanding shocks of up to 40 G. Each of the four read/write heads address 306 cylinders and the drive is compatible with Seagate's model 412 rigid disk drive. Average access time is 65 nsec and the ST212 operates at track densities of 550 t.p.i. with a total of 612 tracks per surface. The electronics are packaged on two boards which include circuits such as index detection, head and drive select, write fault detection and power and speed control. Price is



\$690, in 1,000 lot quantities. Single units are \$1,265. **Seagate Technology**, Scottsvalley, CA **Write 181**

compatible with IBM, Apple, Tandy, Kaypro, Commodore, and Eagle personal computers. It has 2 Kbytes of buffer memory, expandable to 8K and a Centronics parallel interface. Price is \$699. **Juki**, Saddle Brook, NJ **Write 164**

KEYBOARDS

IBM Plug Compatible



Two series of Keyboards offer an IBM and modified user friendly configuration. The plug compatible series connects directly to the IBM PC or other emulating units. The Look Alike series provides asynchronous 300 baud TTL ASCII output. Keyboards are available in either the IBM or user friendly layout. Both keyboards have 31 character buffers, and matte finish sculptured keycaps which feature sublimated printing. Price is \$68 in 10,000 piece pricing. **Hi-Tek**, Garden Grove, CA **Write 163**

MULTIPLEXOR

Diagnostic Capabilities



Megalink is a bit synchronous time-division multiplexor that provides voice and data transmission with network management and diagnostic capabilities. Megalink comprises its own standalone network or integrates into any DCA network. The multiplexor features trunk speeds of 50 to 1.544M bps, support of 128 ports, which expand in increments of four, and dynamic bandwidth contention. Megalink has redundant power supply, common logic options and a bit interleaved multiplexing technique for shorter, character assembly delays. Price starts at \$3,800. **DCA**, Norcross, GA **Write 162**

COMMUNICATIONS PROCESSOR

With On And Off Line Diagnostics

The MC-80 600-1 communications processor emulates the IBM 3274-51C communications controller running configuration support level A. The device converts a DEC VT-100 compatible terminal into an IBM 3277-1, 3277-2, 3278-1, 3278-2 terminal communicating with the IBM

MINIFLOPPY DISKETTES

48 T.P.I. Density



The 5 1/4" diskettes from Comrex are available in three capacities which feature different storage densities and surfaces. The Model CR-10005 records on a single disk surface with single density. Model CR-10010 has single-sided, double-density recording. Model CR-10015 features double-sided, double-density recording. The diskettes are configured with a soft-sectored format, a single index hole, 48-t.p.i. density, and 40 tracks for each recording surface. Recording density is 2800 b.p.i. for the single-density model, and 5600 b.p.i. for the double-density models. Prices, in ten pack quantities, are \$29.95 (CR-1005), \$44.95 (CR-10010) and \$49.95 (CR-10015). **Comrex**, Torrance, CA **Write 167**

ETHERNET TRANSCEIVER

Operates at 10 Mbits/sec

The Model 2110 MultiPort Transceiver operates at 10 Mbits/sec and is designed to accept a maximum of eight transceiver modules and one sta-

tion module. The station module can be connected to either a standard Ethernet transceiver, which is attached to a network coaxial cable, or to a mininet adapter that allows the computing devices and the MultiPort transceiver to operate as a stand alone mini-network. The transceivers can be cascaded to increase the number of allowable computing devices per cluster to 64. Price is \$441. **TCL**, Santa Clara, CA **Write 166**

CABLE BANDIT

With Eight Ports



The FM-1608 is a fixed eight port multiplexor which can be configured to interface with IBM 3271/72/74 A and B type controllers. When used with the Fibronics FM-1632, an expandable 32 port multiplexor, the FM-1608 functions with multidrop networks. The system operates with fiber optic or coaxial transmission cable. Price is \$3000. **Fibronics**, Hyannis, MA **Write 165**

DAISY WHEEL PRINTER

Prints At 18 cps

The model 6100 daisy wheel printer prints bidirectionally at 18 cps, utilizes 100 character daisy wheels and has 10/12/15 pitch and proportional spacing. It supports word processing functions including superscript, subscript, bold shadow printing, double strike, underlining and has graphic capabilities. The printer is

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<i>Mini/Micro Southeast</i>	Orlando, FL	January 17 - 19, 1984
<i>Mini/Micro Northeast</i>	Boston, MA	May 15 - 17, 1984
<i>Mini/Micro Midwest</i>	Dallas, TX	September 11 - 13, 1984
<i>Mini/Micro Northwest</i>	Seattle, WA	October 2 - 4, 1984
<i>Mini/Micro West</i>	Anaheim, CA	October 30 - November 2, 1984



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NEW PRODUCTS

PERIPHERALS

host using the EBCDIC BSC protocol. ASCII terminals can be used in local and dial-up applications. The MC-80/600-1 performs on screen sizes of 480, 960, and 1920 characters. Testing features include on and off line diagnostics. Price is \$1,495. **Innovative Electronics**, Miami, FL. **Write 161**

WINCHESTER DISK DRIVES

42-160 Mbyte Capacities

The Megablue 8" Winchester disk subsystem is available in 42, 84 and 160 Mbyte capacities. The subsystems enclosure accepts any 8" Winchester disk, and uses a SMD interface. Features include a head arm with read preamplifier, a universal switching power supply and a 100/105 CFM fan. **Transduction LTD**, Missauga, Ontario. **Write 160**

LAN DEVELOPMENT TOOL

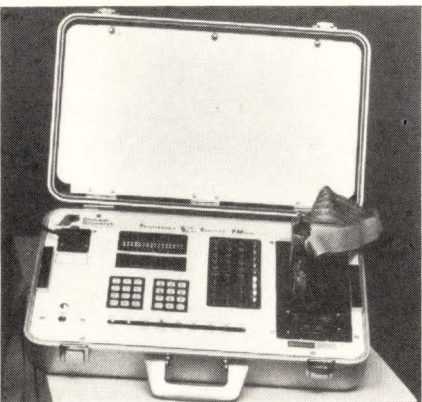
Analyzer/Simulator



The Excelan Nutcracker is a LAN system analyzer/simulator for developing, debugging, testing, characterizing, maintaining, and managing Ethernet-based systems. It operates at 10 Mbit/sec with an 8086-based CPU and features 900 Kbytes of RAM, a 20 Mbyte Winchester disk drive, and a 600 Kbyte floppy disk drive. The Nutcracker includes a 12" monochromatic CRT with 82-key keyboard and an external 100 c.p.s. matrix printer with graphics capability. Price is \$49,500. **Excelan**, San Jose, CA. **Write 159**

REMOTE CONTROL OPTION

With Self Test Feature

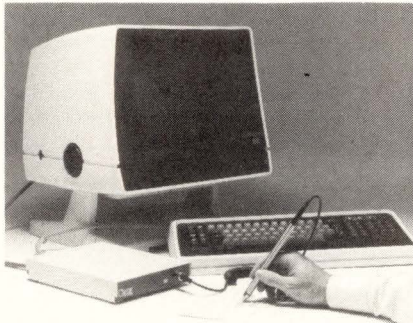


The remote control option for the Pioneer Research PM-4000 Qualifier allows SMD disk drive maintenance to be controlled from a distant location using the telephone lines for com-

munication. The PM-4000 qualifier has canned error diagnostics such as self-test, sequential read, sequential write, random seek and read, and butterfly seek. It may be single-stepped, is operator-programmable and can test any SMD drive size or configuration. Hard and soft error detection and checking of specific track, head and sector problems are provided through use of a 32-bit ECC. **Pioneer Research**, Santa Monica, CA. **Write 158**

BAR CODE SCANNERS

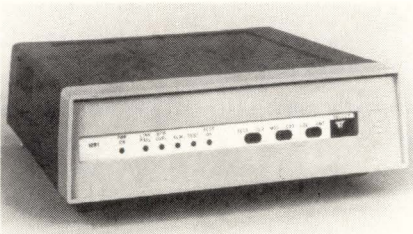
With Upgrade Provision



The 200 series of bar code scanner interfaces to most industrial and administrative CRT serial computer terminals and SDLC displays. The 240 PCScanner provides users with an integrated board that is a program-transparent keyboard interface. The scanner is offered with an upgrade provision that allows the user to add OCR capabilities to the bar code scanner. Price is \$745. **Caere Corp.**, San Jose, CA. **Write 157**

DATA CONCENTRATOR

Multiplexes Eight Terminals



The Gen net 1261 is a data concentrator designed to multiplex four or eight asynchronous terminals over one communications link. The 1261 has composite data rates to 19.2 Kbps, as well as down line loading and diagnostics, CCITT compatibility, and local echoplex. Price is \$1,330. **General DataComm**, Danbury, CT. **Write 156**

Z80 EMULATOR

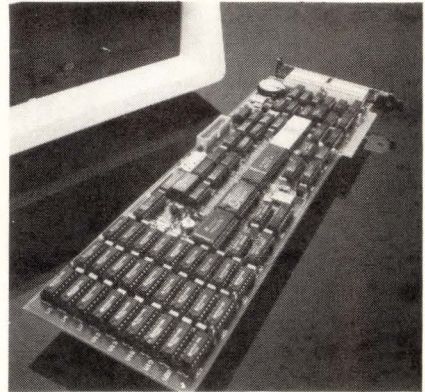
Features Assembly And Disassembly

The Nice is a miniaturized 3" x 3" Z80 emulator which does not use the target system's memory or I/O address space. Its command set permits the user to examine and modify registers; display, move, fill, substitute, and test memory; monitor and control I/O and interrupt operations; trace software and set breakpoints; and assemble and disassemble Z80 programs. The module plugs directly into the Z80 socket of the system under test. In applications where space

around the socket is restricted, an extender cable is provided. Price is \$550. **Nicolet Paratronics Corp.**, Fremont, CA. **Write 170**

HARD DISK SYSTEM

15 Mbytes Storage



The PC eXtender is a hard disk system which provides 10 or 15 Mbytes of mass storage, an online storage equivalent to 45 floppy disks. The system includes a serial port, clock/calendar, sockets for 192K of RAM, and software back up utilities. The controller occupies one expansion slot and pin configuration selections can be made for direct connection to a modem or printer. Price is \$2,295. **Falcon**, Kent, WA. **Write 169**

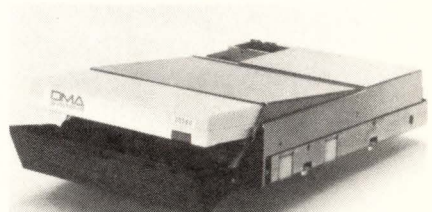
ADAPTER

640 x 400 Resolution

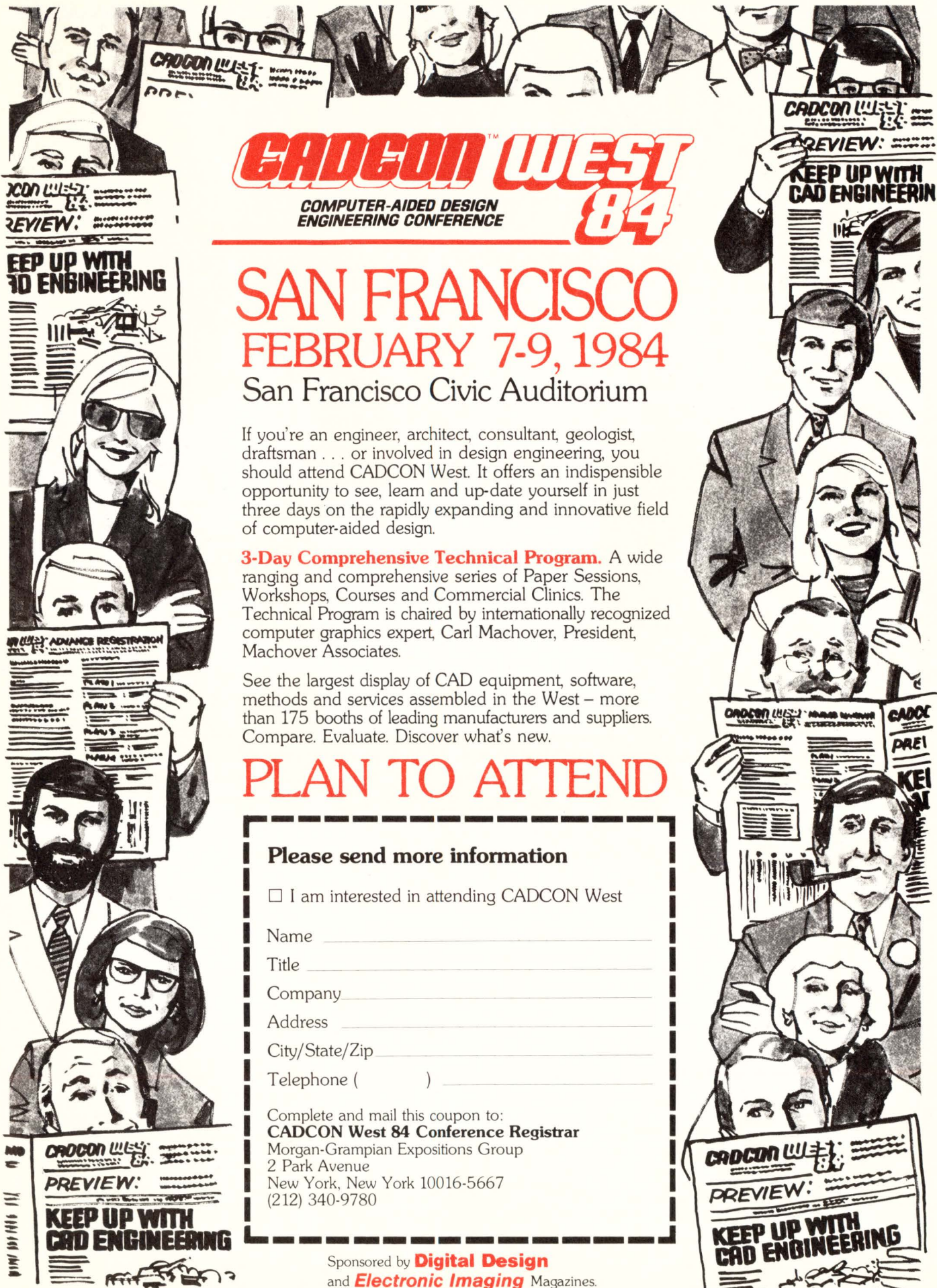
The Cono-Color adapter is a substitute for the IBM Color Graphics Adapter for the IBM PC and compatibles. It features 256 colors, two character sets, resolutions of 640 x 400 and 512 x 512, conic curves, and 128 Kbytes of display memory. The adapter supports IBM-compatible character and graphic modes, allowing existing software for the IBM Color Graphics Adapter to run without modification. The Cono-Color adapter is available in two versions, one of which is expandable to include high speed graphics hardware. **Conographic**, Newport Beach, CA. **Write 171**

WINCHESTER DISK DRIVE

With 7.5 Mbyte Capacity



The DMA 360 is a 5.25" Winchester cartridge disk drive for desktop and personal computers. The drive has a 7.5 Mbyte cartridge and an average access time of 98 msec. Other features include a purge cycle, air filtration system, and retracted heads. On-board firmware permits users to format a blank cartridge when inserted into the drive, eliminating the need to write servo data on the disk surface prior to shipment. Price is \$500. **DMA**, Goleta, CA. **Write 168**



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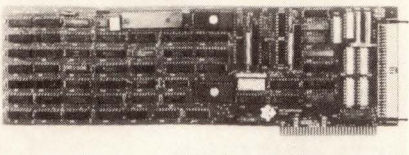
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COMPONENTS

RIGID DISK CONTROLLER

16 To 800 Mbyte Storage Capacity

The Maverick SMD PC-80 from Interphase Corp. is a Winchester disk controller for the IBM PC or any microcomputer with architecture similar to the PC such as those from Compaq, Eagle, Columbia and Micpoint. The controller accommodates 8" disks, without hardware or software modifications. In a 50 station network each file server supplies 10 Mbytes of storage to each PC, expanding the capacity needed for database management. The Maverick supports two SMD disk drives,



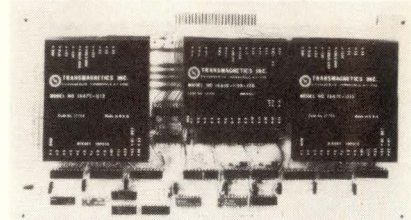
has a disk storage capacity of 16-800 Mbytes as well as a reduced parts count (60 integrated circuits) on-board. Software drivers are available for IBM-DOS 2.0 and uNETix. Other features include buffered architecture, a CMOS processor, dual porting, and 32-bit ECC. Price is \$1,895. **Interphase Corp.**, Dallas TX **Write 210**

I/O 4 Async/4 Sync, with four asynchronous serial channels and four synchronous/asynchronous channels. All boards support the 24 bit address space of the IEEE-696 specification. The boards use eight S-100 I/O ports, addressable to an 8 byte boundary in 64K with user selectable switches. A clock/counter with 56 bits of battery backed up RAM is included. The I/O 8 series operates in polled I/O or interrupt driven operation. Three interrupt types are generated on-board; serial I/O, real time clock, and standby real time clock. Software programmable baud rates from 50 to 19,200 are supported. Price is \$600.-\$795. **SDSystems**, Dallas, TX

Write 197

D/S AND S/D CONVERTERS

With Multibus 8085/8086 Interface

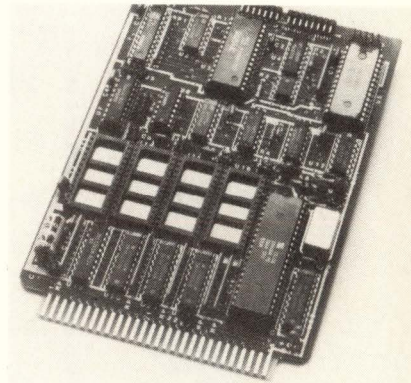


Series 5401 is a synchro/resolver-to-digital and digital-to-synchro/resolver PC board containing logic to interface with the Intel Multibus 8085/8086 system. The board includes either combinations of three single-speed converters or two 2-speed S/D converters. The 2-speed converters are designed to interface with pancake resolver transducers. High power versions are available to drive size 23 torque receivers or equivalent loads. **Transmagnetics**, Farmingdale, N.Y.

Write 198

STD BUS COMPUTER

With Z80 Processor

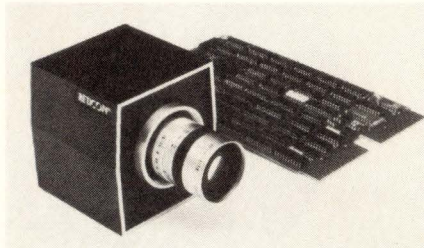


The SB8010 single board STD Bus computer operates as either self-contained controller or as the center of a multi-card system. The board contains a Z80 or Z80A processor, 32Kbytes of memory, an RS-232C port, and a counter/timer/interrupt controller. The memory system allows a mix of four 28-pin, JEDEC-pinout SRAM, ROM, or EPROM. The RS-232C serial port supports communication at software-selectable baud rates of 50 to 4800. Signals supported include TXD, RXD, CTS, RTS, and DTR. In quantities of 10-24, price is \$365. **Micro/sys**, La Canada, CA

Write 200

INTERFACE BOARD

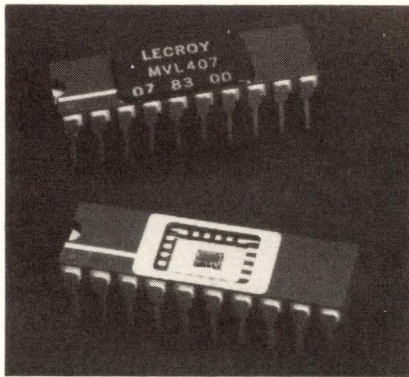
Camera to Q-Bus Systems



The Model RSB6320 camera/computer interface board is designed to accept digital 1 bit binary images from Reticon Line Scan and Area Image Sensing Cameras. Image data is processed by the RSB6320 into a run length encoded format. Two modes of encoding can be selected; one stores the pixel address of an image transition, the other mode stores the transition data as pixel groups between transitions. Data is stored in a 253 word memory. Price is \$895. **EG&G Reticon**, Sunnyvale, CA **Write 204**

QUAD COMPARATOR

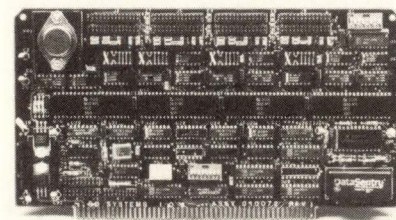
2.5 nsec Propagation Delay



The model MVL407 quad comparator features power dissipation of 140 mW/channel and 2.5 nsec propagation delay at 2X overdrive. The outputs of the MVL407 are complementary ECL levels and can drive 50 Ohm transmission lines. A special feature built into the MVL407 is hysteresis of typically 2 mV. This helps prevent multiple outputs caused by noise on slowly varying input pulses. The four comparators feature 2 mV hysteresis and operate from ± 5 V supply voltages. Price is \$10.80. **LeCroy**, Spring Valley, NY **Write 205**

I/O EXPANSION BOARDS

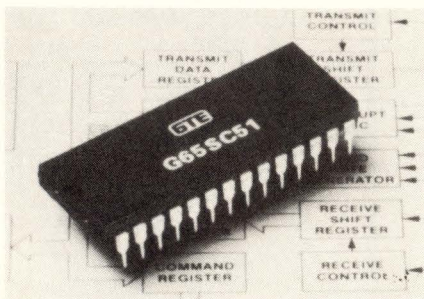
Supports Baud Rates Of 50-19,200



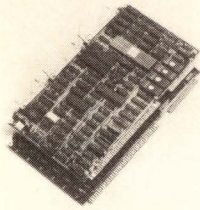
The I/O 8 family of serial I/O expansion boards are designed for the IEEE-696 (S-100) bus. Models include the I/O 4 Async, with four asynchronous serial channels, the I/O 8 Async, with eight asynchronous serial channels, and the

INTERFACE ADAPTOR

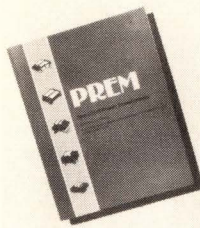
For CMOS Asynchronous Communications



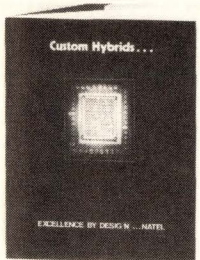
The G65SC51 is a CMOS asynchronous communications interface adaptor with an on-chip baud rate generator that allows 15 programmable rates (50 to 19,200 baud). The G65SC51 includes programmable interrupt and status registers, full-or half-duplex operating modes, and 5, 6, 7, 8 or 9-bit transmission rates. Price in quantities of 100 is \$7.90. **GTE**, Tempe, AZ **Write 190**



Microprocessor Board Brochure. The CD68K Microprocessor Systems Board is described in this brochure from Callan Data Systems. The four page publication lists the features and functions of the CPU and local memory board, and includes descriptions of memory management and protection, local memory interface and IEEE 796 bus interface.
Callan Data Systems Write 256



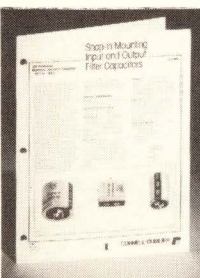
Transformer Catalog. The 12-page catalog describes Prem Magnetics' line of printed circuit power transformers, whose ratings range from 1.1VA to 36VA. Several models feature 3-flange bobbin construction for isolation between primary and secondary windings. Secondaries are split for either series or parallel connection. Catalog includes parallel and series performance ratings and mechanical specifications.
Prem Magnetics Write 260



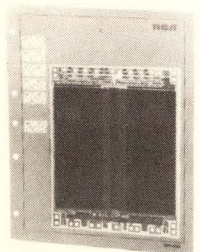
Custom Hybrid Brochure. The custom hybrid facilities and capabilities of Natel Engineering Co. are described in this 16-page, 4-color brochure. Included are discussions of engineering, substrates, assembly quality, manufacturing flow, assembly flow, electrical and environmental testing and basic products. The facility is in compliance with MIL-M-38510 and suitable for high-rel hybrid microcircuit manufacturing.
Natel Write 266



Connector Catalog. The 30-page catalog from TRW covers their line of MIL-C-26500 cylindrical connectors. Charts, photos, diagrams and illustrations are provided in the application/specification guide. The catalog covers the design of the TRW C-48, CO909A MMB, CN0915 and CN0942 Series of connectors.
TRW Write 253



I/O Capacitor Brochure. The data sheet from Cornell-Dubilier describes its Type FPC capacitor line designed for use with switching power supplies. The capacitors have an operating temperature range of -40°C to +85°C. The brochure gives performance, electrical and environmental specifications as well as dimensional drawings. A selection chart details 49 types available in 18 case dimensions with a maximum height of 2" and ratings from 150µF to 10,000µF.
Cornell Dubilier Write 262



CMOS ROM Brochure. This brochure describes RCA's line of CMOS ROMs that can be mask-programmed to meet customer application requirements. The brochure explains features and options for each ROM type, which are shown together with a pinout diagram. Information is provided on the three methods for submitting instructions on programming CMOS ROMs: a master device (ROM, PROM, or EPROM), a floppy diskette, and standard 80-column computer cards.
RCA Write 251

Amplifier Bulletin. This bulletin from Amplifier Research provides information on its RF amplifier line, including the ultrabroadband W-Series (100 kHz to 1000 MHz; 1 W to 50 W) and L-Series (10 kHz to 300 MHz; to 10 kW) models. The guide explains what to consider when selecting an amplifier and the available RF-testing accessories.
Amplifier Research Write 250

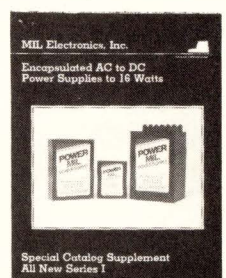
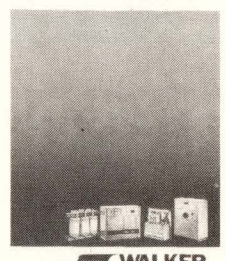
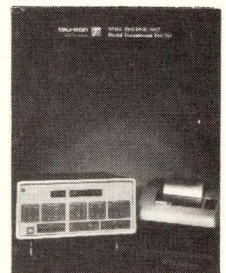
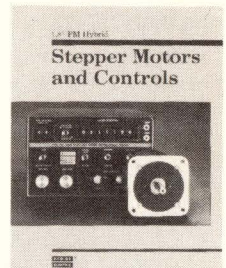
Stepper Motor Catalog. Stepper motor performance specifications are detailed in the 48 page catalog from Bodine Electric Company. Included are application guides, check lists and thermal characteristics showing motor temperatures when using the manufacturer's controls. The catalog gives specifications and features of translator and indexer modules, and provides sizing nomographs, control options, and power supply requirements.
Bodine Electric Company Write 257

Digital Transmission Test Set Brochure. This brochure from Tau-tron describes the S5104 digital transmission test set. The unit characterizes digital transmission systems operating at DS1, DS1C, and DS2 transmission rates. System controls and indicators are described as well as receiver and transmitter specifications.
Tau-tron Write 267

Transformer Brochure. This brochure outlines Walker Power's capabilities to design and manufacture dry-type transformers and saturable core reactors. Also covered are AC and DC inductors, power supplies with various control options, and plating rectifiers with ratings and capacities.
Walker Power Write 259

Power Supply Catalog. The 8-page catalog from MIL Electronics describes computer-optimized encapsulated AC-DC power supplies under 16 watts. Included is an application for a free analysis of power supply performance. It covers special load regulation circuitry which permits a dead short at the output with no effect on the power supply. Load regulation is .1%; max ripple is 1 mv P-P. All customized I series power supplies are treated as standard orders.
MIL Electronics Write 265

Connector Catalog. This catalog from Lemo U.S.A. features a part number reference and specifying guide and an overview of the characteristics of the "B" Series, as well as cable assembly instructions. Contact configurations range from 2-64 contacts and are available in mixed coaxial, multi-contact, and high voltage and multi-contact configurations. The inserts can be provided with either solder or crimp contacts.
Lemo Write 263



Calendar

December 6-8

Software Maintenance Workshop. Monterey, CA. Contact: N. Schneidwind, Computer Science Dept., Naval Postgraduate School, Monterey, CA 93940. (408) 644-2719.

January 4-6

HICSS-17, Hawaii International Conference on System Sciences. Honolulu, HI. Contact: Bruce Shriver, Computer Science Dept., University of Southwestern Louisiana, P.O. Box 44330, Lafayette, LA 70504. (313) 264-6606.

January 17-18

IEEE Instrumentation and Measurement Technology Conference (IMTC). Queen Mary, Long Beach, CA. Contact: Frank Kiode, Rockwell International (714) 632-3923.

January 17-19

Southcon '84 and Mini/Micro Southeast (IEEE et al.). Orlando, FL. Contact: Nancy Hogan, Electronic Conventions, Inc., 8110 Airport Blvd., Los Angeles, CA 90045. (213) 772-2965.

January 18-23

COMMTEX International. Dallas, TX. Contact: Robert Milko, (703) 273-7200.

January 19-20

Measurement Science Conference (MSC). Queen Mary, Long Beach, CA. Contact: Chet

Crane, Teledyne Microelectronics, (213) 882-8229, ext. 449.

January 22-27

SPIE Technical Symposium and Instrument Exhibit. Los Angeles, CA. Contact: The Society of Photo-Optical Instrumentation Engineers, P.O. Box 10, Bellingham, WA 98227. (206) 676-3290.

January 24-26

Advanced Semiconductor Equipment Exposition (ASEE) and Technical Conference. San Jose Convention Center, San Jose, CA. Contact: Joyce Estill, Cartlidge and Assoc., Inc., 4030 Moorpack Ave., Suite 205, San Jose, CA 95117.

January 24-26

1984 Annual Reliability and Maintainability Symposium (IEEE et al.) San Francisco, CA. Contact: N.H. Kutner, Westinghouse Electric Corp., Hedy Ave., (71-21), Sunnyvale, CA 94088.

January 25-28

Electrotest Japan '84. Tokyo, Japan. Contact: Anne Lawlor, Ruann International, P.O. Box 1877, Des Plaines, IL 60018. (312) 296-2191.

January 31-February 2

Communications Networks '84. Washington, D.C. Contact: Judie McDaid, National Sales Manager, Hajar Assoc., 280 Hillside Ave., Needham Heights, MA 02194. (617) 444-3946.

February 2-4

1984 SCS Multiconference. San Diego, CA. Contact: The Society for Computer Simulation, P.O. Box 2228C, La Jolla, CA 92038.

February 6-8

Software Process Workshop. Egham, England. Contact: M.M. Lehman, Dept. of Computing, Imperial College of Science and Technology, Huxley Bldg., 180 Queens Gate, London SW7 2AZ England. Tele. 01-589-5111.

February 6-9

1984 International Symposium on Logic Programming. Atlantic City, NJ. Contact: Doug DeGroot, IBM Research, P.O. Box 218, Yorktown Heights, NY 10598. (914) 945-3497.

February 7-8

ATGP Workshop. Arlington, VA. Contact: Jerry Kunert, Naval Air Engineering Center, Code 92A3, Lakehurst, NJ 08433; (201) 323-2663.

February 14-16

ACM 1984 Computer Science Conference. Philadelphia, PA. Contact: Aaron Beller, Computer and Information Science Dept., Temple University, Philadelphia, PA 19122.

February 17-18

SIGCSE Technical Symposium. Philadelphia, PA. Contact: Richard H. Austing, Dept. of Computer Science, University of Maryland, College Park, MD 20742.

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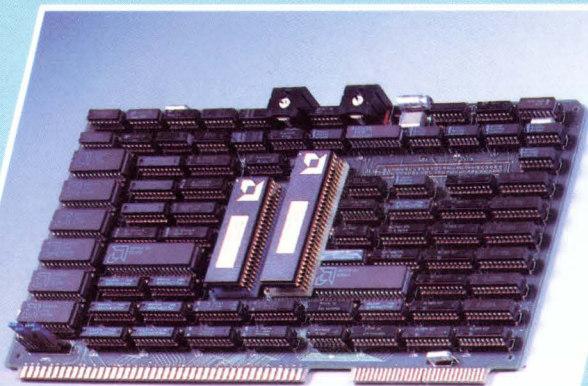
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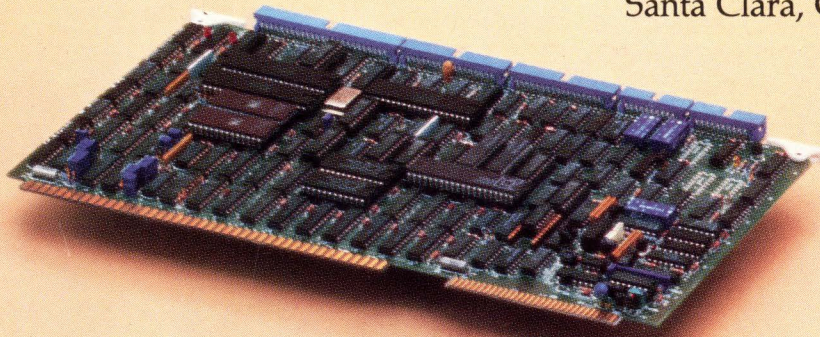
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