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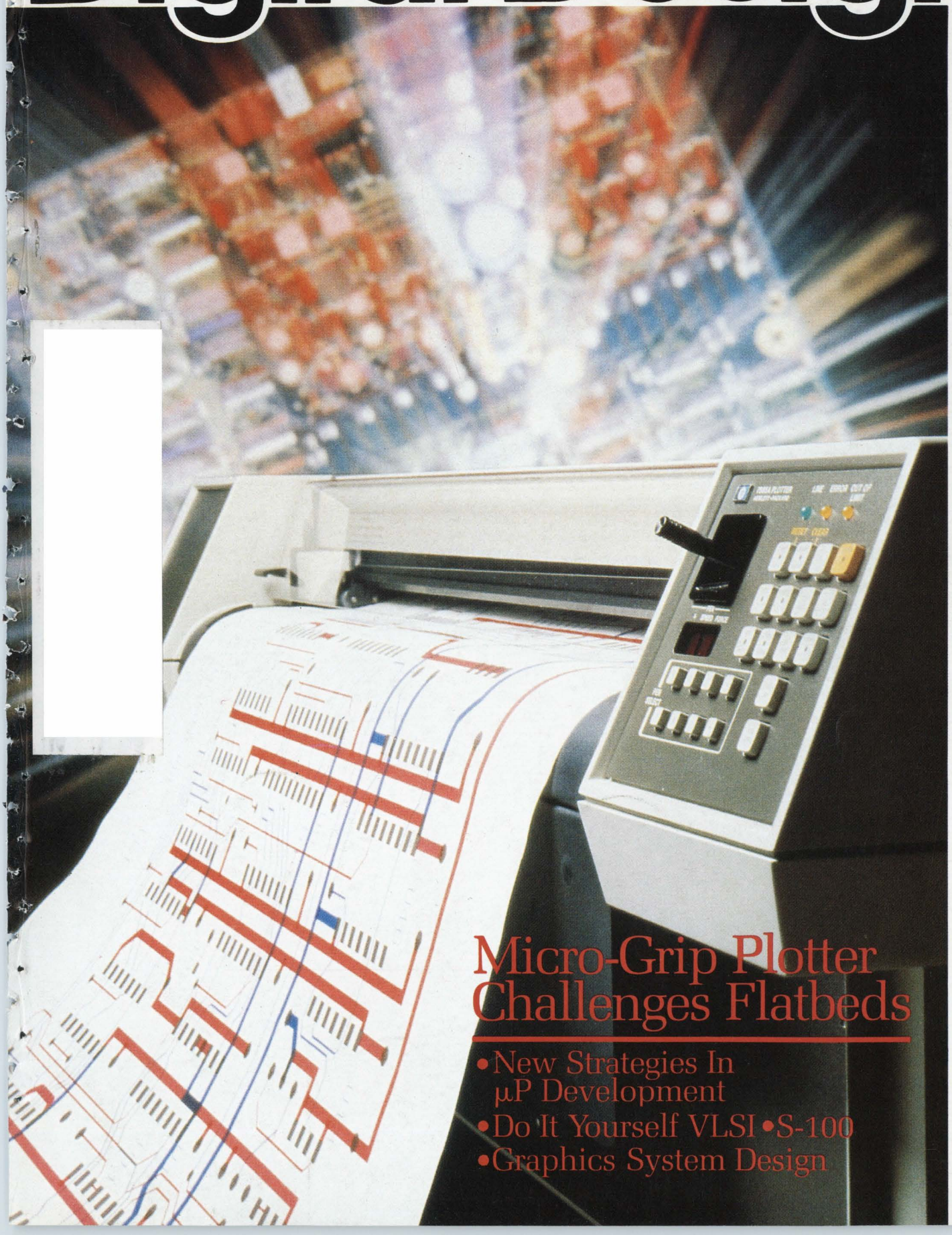
Digital Design



Micro-Grip Plotter Challenges Flatbeds

- New Strategies In μP Development
- Do It Yourself VLSI
- S-100
- Graphics System Design

COMPUTERS/SYSTEMS · PERIPHERALS · COMPONENTS · 9/82

VOL.12
NO. 9

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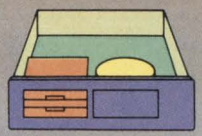
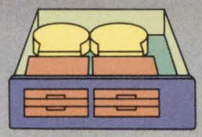


5.5 MB Winchester/floppy combination.



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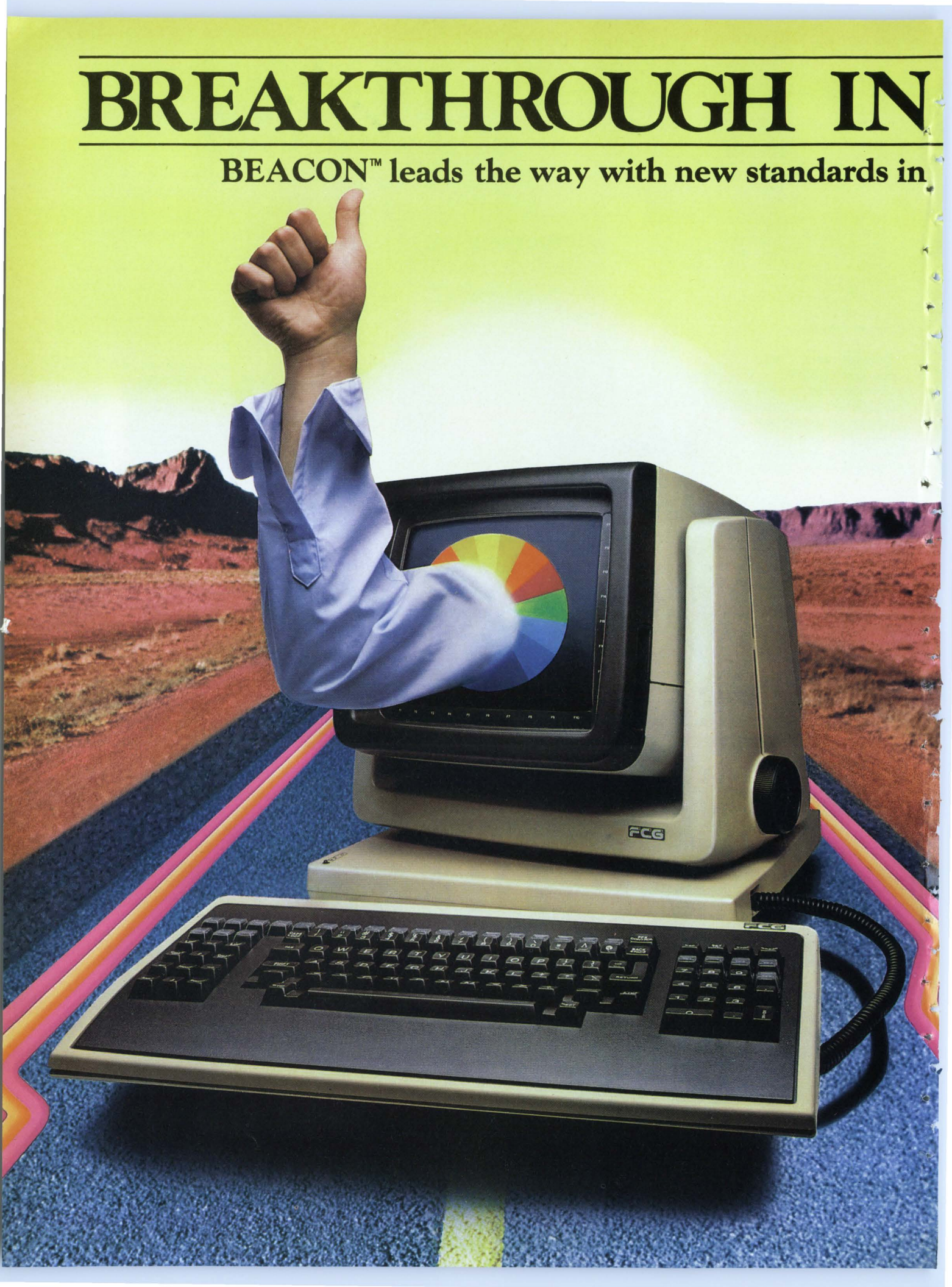

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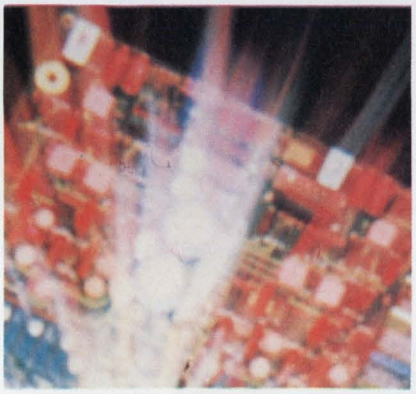
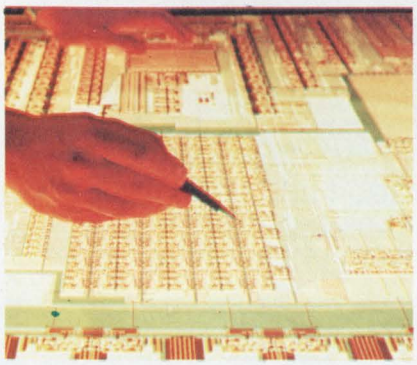
SEPTEMBER 1982
VOL. 12, NO. 9

Digital Design

p. 74 (photo courtesy Florida Computer Graphics)



p. 44 (photo courtesy Hewlett Packard)



p. 60 (photo courtesy AMI)

Cover

H-P's 7585A plotter represents a major step forward in making large-scale plotters smaller, cheaper and faster (see p. 44).

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COMPUTERS/SYSTEMS

μP Development Systems: More Choices For The User 32
New development strategies mean designers must analyze a variety of cost/performance trade-offs.

Designers' Guide To The IEEE-696 Bus 53
This article examines the S-100's rapid growth, its future and various aspects of its design.

Market Trends.....23
PABX And LAN Integrate With Energy Management Systems

Graphics System Design 74
High Graphics Performance Through Multiprocessor Architecture

PERIPHERALS

Micro-Grip Plotter Challenges Flatbeds 44
H-P's latest entry into the graphics hard copy arena provides flat-bed size plots, but at low cost and with lower floor-space requirements.

Technology Trends.....20
High Capacity 5¼" Winchester Offers 30ms Access Speed

Market Trends.....23
Keyboard Input Favored Over Touch And Voice • Floppies To Pass The $1 Billion Level In '84

COMPONENTS

Do It Yourself VLSI 60
The rapidly expanding custom logic field will provide designers the opportunity to maximize board space and to make proprietary designs.

Innovative Design 76
Winchester Controller Designed For Multitasking Systems

Technology Trends.....18
High-Growth Of Surface Mounted Packages Forecast • Stackable Module Houses 16K-Byte Static CMOS RAMs.

Letters 10
Calendar.....12
News Update 14
Product Index 48
New Products 77
Advertisers' Index 82
New Literature.....83
Viewpoint 84

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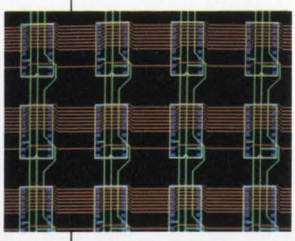

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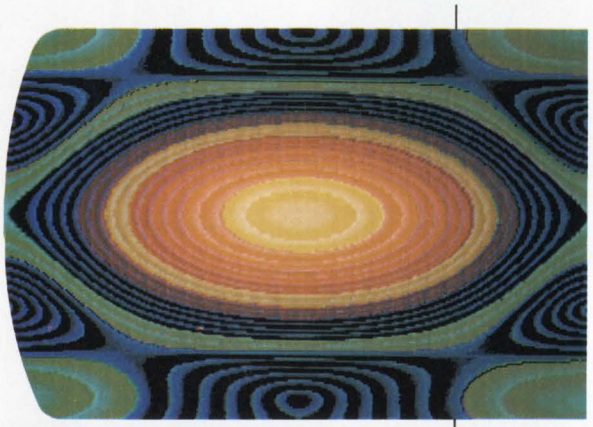

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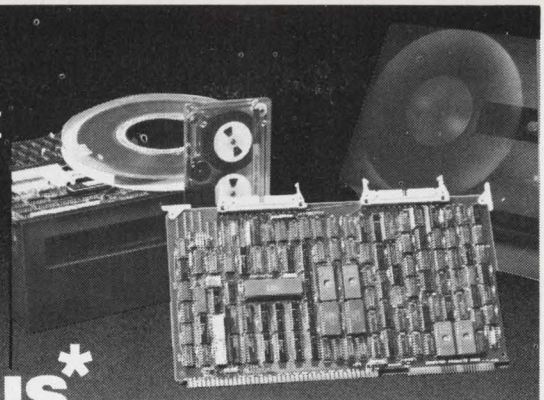

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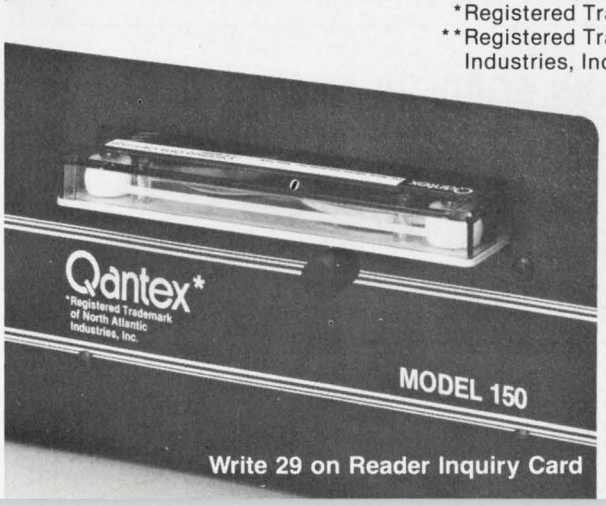

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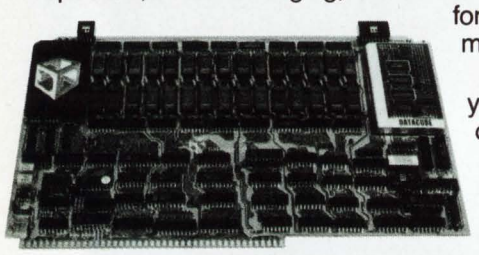

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Letters

Unpaid Overtime

Dear Editor:

As an example of how engineers are being exploited during this recession due to the lack of a union or IEEE support, at our company (a large brewing company located in Milwaukee) all engineers are "expected" to work 4 hours on Saturdays, and if needed, on Sundays. On holidays, and even such days as Memorial Day, Independence Day, etc., a notice is sent out stating the engineering buildings will be open. This indicates all engineers are again expected to work 4 hours—all without pay!

Not satisfied with that, the Corporate Engineering Building has installed a time lock at the door, so all engineers must "clock in" and the door is "locked in" until 5PM. Engineers are expected to travel to other company plants on their own time and come home late (after 5PM)—all without pay. If you protest or do not show up on Saturdays/holidays it is construed as a "protest" and your salary increment/promotion is affected. Verbal protests have been settled by "firing."

How does one fight this situation? National publicity or a boycott is the only solution. Why don't you investigate this work situation? Salary is not all we should be fighting about! (Viewpoint 3/82)

A Brewing Co.
Corporate Engineer
Milwaukee, WI

Quite Impressed

Dear Editor:

We just received your April issue of *Digital Design* and were quite impressed by the article written by Paul Snigier entitled, "Designer's Guide to the STD BUS." It's a very well written article and one that accurately portrays the design considerations of the STD BUS.

Mary C. McDougal
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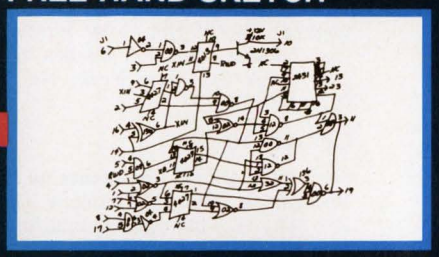

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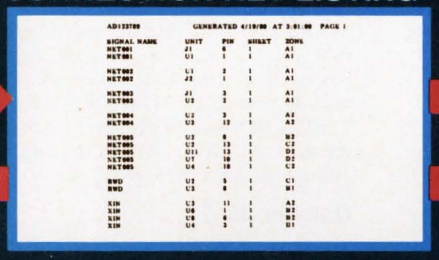
IBM, plus others

Computer straightens slanted lines, uses correct size symbols and enters alignments among symbols entered by user during input. Drum plotter or Electrostatic plotter output.

CONNECTION NET LISTING



BILL OF MATERIALS

BILL OF MATERIALS FOR DRAWING NUMBER AD123789

ITEM	QTY	PART NUMBER	DESCRIPTION
1	4	054-4000	SN7404N
2	12	054-002	SN7402N
3	8	054-6080-67	RESISTOR 1.5K 1/2W 5%
4	2	079-5784-1	ZENER DIODE 1N821 6.2L

REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
CR1	079-5784-1	ZENER DIODE 1N821 6.2L
R1	054-6080-67	RESISTOR 1.5K 1/2W 5%
U1	054-4000	SN7404N
U2	054-002	SN7402N

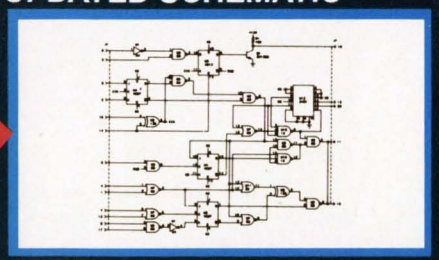
"DS1" automatically provides Net and Bill Lists directly from data base of digitized schematic.

P.C.B. ROUTER INTERFACES

ASI-PRANCE
AUTOMATE '80
COMPUTERVISION
REDAC
SCICARDS™
others available

"DS1" interfaces to P.C.B. Routers, Wire Wrap, Simulation and Test Programs.

UPDATED SCHEMATIC



"DS1" performs Back-Annotation from a "Was-To" list derived from the P.C. Router. "Back-Annotation" automatically updates the schematic to agree with the circuit board component placement.

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DESIGN AIDS inc.

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Calendar

September 29–October 2

COMMON Fall '82 Conference. Biltmore Hotel, Los Angeles, CA. An IBM Computer users' group features user and IBM speakers. Contact: David G. Lister, COMMON-F82, 435 N. Michigan Ave., Suite 1717, Chicago, IL 60611; (312) 644-0828.

September 30–October 2

Phoenix Computer Expo. Phoenix Civic Plaza, Phoenix, AZ. Contact: Carol Houts, Judco Computer Expos, 2629 N. Scottsdale Rd., Scottsdale, AZ 85252; (800) 528-2355, (602) 990-1715 in Arizona.

October 1

"Computer Animation." Essex House, New York, NY. Features presentations by six of the leading computer animation houses. Contact: Perry Jeffe, Pratt Center, 505 White Plains Rd., Tarrytown, NY 10591; (914) 631-8772.

October 4–6

Convergence '82. International Congress on Transportation Electronics. Hyatt Regency, Dearborn, MI. Contact: M.J. Asensio, SAE, 3001 W. Big Beaver Rd., Suite 602, Troy, MI 48084; (313) 649-0402.

October 4–6

VLSI and Software Engineering Workshop. Port Chester, NY. Contact: J.A. Rader, 7372 W. 83rd St., Los Angeles, CA 90045.

October 4–8

AdaTec Tutorial and Conference on Ada. Arlington, Va. (Tutorial: Oct. 4–5; Conference: Oct. 6–8) Contact: Anthony Gargaro, Computer Sciences Corp., 304 West Route 38, Moorestown, NJ 08057; (609) 234-1100, ext. 2280.

October 5–8

Microprocessor Troubleshooting Course. Boston, MA. A four-day course provides participants with the opportunity to learn practical troubleshooting techniques. $895. Contact: Ruth Dordick, Integrated Computer Systems, 3304 Pico Blvd., PO Box 5339, Santa Monica, CA 90405; (213) 450-2060.

October 5–7

MICRO 15. The 15th Annual Workshop on Microprogramming. Palo Alto, CA. Contact: Will Tracz, IBM-FSD, 101BM44, Owego, NY 13827.

October 6–8

20th Annual Allerton Conference on Communication Control, and Computing. Monticello, IL. Contact: Prof. H.V. Poor, Coordinated Science Lab, University of Illinois at Urbana-Champaign, 1101 West Springfield Ave., Urbana, IL 61801.

October 7, 13, 19

Invitational Computer Conference. Amsterdam, Oct. 7; Milan, Oct. 13; Munich, Oct. 19. These one-day shows of operating equipment displays and technical seminars are designed to reach OEMs, system houses and quantity end users. Contact: Susan Fitzgerald, B. J. Johnson & Associates, Inc., 3151 Airway Ave, #C2, Costa Mesa, CA 92626; (714) 957-0171.

October 11–13

Seventh Conference on Local Computer Networks. Minneapolis, MN. (Tutorials: Oct. 11; Conference: Oct. 12–13.) Contact: Harvey A. Freeman, Architecture Technology Corp., PO Box 24344, Minneapolis, MN 55424.

October 11–14

INFO '82. New York Coliseum, New York, NY. Information Management Exposition and Conference. Contact: Clapp and Poliak, Inc., 708 Third Ave., New York, NY 10164; (212) 661-8010.

October 11–15

Computer Communications Systems and Networks. George Washington University, Washington, DC. Intensive program devoted to the state of the art of modern data communications systems. Course No. 596DC. Contact: Computer Engineering Education, George Washington University, Washington, DC 20052; (800) 424-9773.

October 12

NECOM '82. Boston Marriott Hotel, Newton, MA. A single source computer show for OEMs, sophisticated end users, dealers and distributors. 1-7PM. Contact: Norm DeNardi Enterprises, 289 S. San Antonio Rd., Suite 204, Los Altos, CA 94022; (415) 941-8440.

October 14–15

Man Machine Interface. Columbia Inn, Columbia, MD, and November 4–5, Hyatt Regency, Austin, TX. Contact: Continuing Education Institute, Oliver's Carriage House, 5410 Leaf Trader Way, Columbia, MD 21044; (301) 596-0111.

October 17–20

International Telecommunications Forum 1982. Marriott Waterfront Hotel, Boston, MA. "The Changing Basis of Competition in the '80s." Sponsored by Arthur D. Little, Inc. Contact: Patricia K. Finnegan, Arthur D. Little, 25 Acorn Park, Cambridge, MA 02140; (617) 864-5770.

October 17–20

MILCOM '82. IEEE Military Communications Conference. Stouffer's Bedford Glen, Bedford, MA. Contact: MILCOM '82, PO Box 208, Bedford, MA 01730; (617) 271-2809.

October 18–22

Third International Conference on Distributed Computing. Ft. Lauderdale, FL. Contact: Distributed Computing, Box 639, Silver Spring, MD 20901; (301) 589-3386.

October 19–20

1982 International Display Research Conference. Cherry Hill, New Jersey. Contact: Thomas Henion, Palisades Institute, 201 Varick St., New York, NY 10014; (212) 620-3384.

October 19–22

Sixth International Conference on Pattern Recognition. Munich, Germany. Contact: Prof. Dr. H. Marko, Lehrstuhl für Nachrichtentechnik, der Technischen Universität München, 8000 München, Federal Republic of Germany.

October 25–28

First Annual Workshop on Interative Computing: CAD/CAM: Electrical Engineering Education. Charlottesville, VA. Contact: Dr. Harlan Mills, IBM-FSD, 6600 Rockledge Dr., Bethesda, MD 20034; (301) 493-1495.

October 26–28

CAM-I 11th Annual Meeting and Fall Technical Conference. Reno, NV. "Beyond CAD/CAM — Extending the Limits" will focus on both immediate and long range user needs as well as the latest advances in computer aided design and manufacturing (CAD/CAM) technology. Contact: Rhonda Gerganess, CAM-I Conferences, 611 Ryan Plaza Dr., Suite 1107, Arlington, TX 76011; (817) 860-1654.

October 26–27

The Ottawa High Technology Show. Civic Center, Lansdowne Park, Ottawa, Ontario, Canada. Contact: Ron Connelly, Show Manager, 2487 Kaladar Avenue, Suite 107, Ottawa, Ontario, Canada, K1V 8B9; (613) 731-9850.

October 26–28

Fifth IEEE Symposium on Mass Storage Systems. Boulder, CO. Contact: Bernard T. O'Lear or Karen Friedman, National Center for Atmospheric Research, PO Box 3000, Boulder CO 80307; (303) 494-5151, ext. 293 or 387.

October 28–31

Mid-Atlantic Computer Show. Armory/Starplex, Washington, DC. Contact: Computer Expositions, Inc., PO Box 3315, Annapolis, MD 21403; (301) 263-8044.

October 30–November 2

Sixth Annual Symposium on Computer Applications in Medical Care. Washington, DC. Contact: Bruce Blum, Symposium Program Chairman, Johns Hopkins University, Traylor 514, Baltimore, MD 21205; (301) 955-8375.

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News Update

Digital Research Develops NS16000 SW

Digital Research will develop and market a multi-tasking version of its CP/M operating system for National Semiconductor's NS16016 16/32-bit μP. The NS16016 was selected by Digital Research because it supports the industry standard 8080 instruction set. The NS16016 runs 8080 instructions more than four times faster than the currently available 8080 8-bit μP.

AMD Announces Latches

AMD has announced availability of six new members of its Am29800 Family of High-Performance Bus Interface devices. The new products, designated Am29841 through Am29846, are 8-, 9- and 10-bit parallel latches. Designed to eliminate the extra packages required to buffer existing latches and to provide extra data width for wider address/data paths or buses carrying parity, the 24-pin, 0.3-inch space-saving devices feature fully TTL-compatible inputs and outputs. All of the bipolar Am29800 latches are manufactured using AMD's proprietary IMOX ion-implanted oxide-isolated fabrication process.

Forward Technology Adopts Standard

Forward Technology, Santa Clara, CA has announced that it has adopted the standard two-dimensional software graphics package proposed by the Association of Computing Machinery's Siggraph group for its Forward Gateway Workstation. The specific implementation of the standard package was developed by Graphic Software Systems, Wilsonville, OR. It operates under the Xenix operating system used by the Gateway Workstation.

Rockwell/Seeq Agreement

The Electronic Devices Division of Rockwell International has signed a license agreement with Seeq Technology, San Jose, CA, under which the Division will obtain Seeq process technology and product design. It is also contemplated, Rockwell said, that the Division will be a second source for the Seeq 16K electrically erasable read-only memory (E^2ROM, Part #5213) and the 64K ultraviolet-erasable programmable read-only memory (UV EPROM, Part #5133). The D5213 has 5V programmability, a worldwide first in the semiconductor industry.

Graphics Standards

Digital Equipment, Intel and Tektronix, have announced their adoption and joint support of two emerging graphics standards. The companies plan to incorporate the standards into their future products. The first is the North American Presentation Level Protocol Syntax (NAPLPS), developed by the Canadian Dept. of Communication. The Virtual Device Interface (VDI), the second proposed standard, is being developed by the ANSI Technical Committee X3H3, Computer Graphics Programming Languages.

Streaming Tape Standards Group

Four manufacturers of ¼" cartridge tape drives have formed an international group to promote widespread use of such drives by encouraging standards that will lead to industry-wide compatibility. Any other maker of ¼" drives that wishes to become a member is welcome to join. Initial members of the Group are Archive, Costa Mesa, CA, Cipher Data Products, San Diego, CA, Data Electronics, San Diego, CA and Tandberg Data A/S Oslo, Norway.

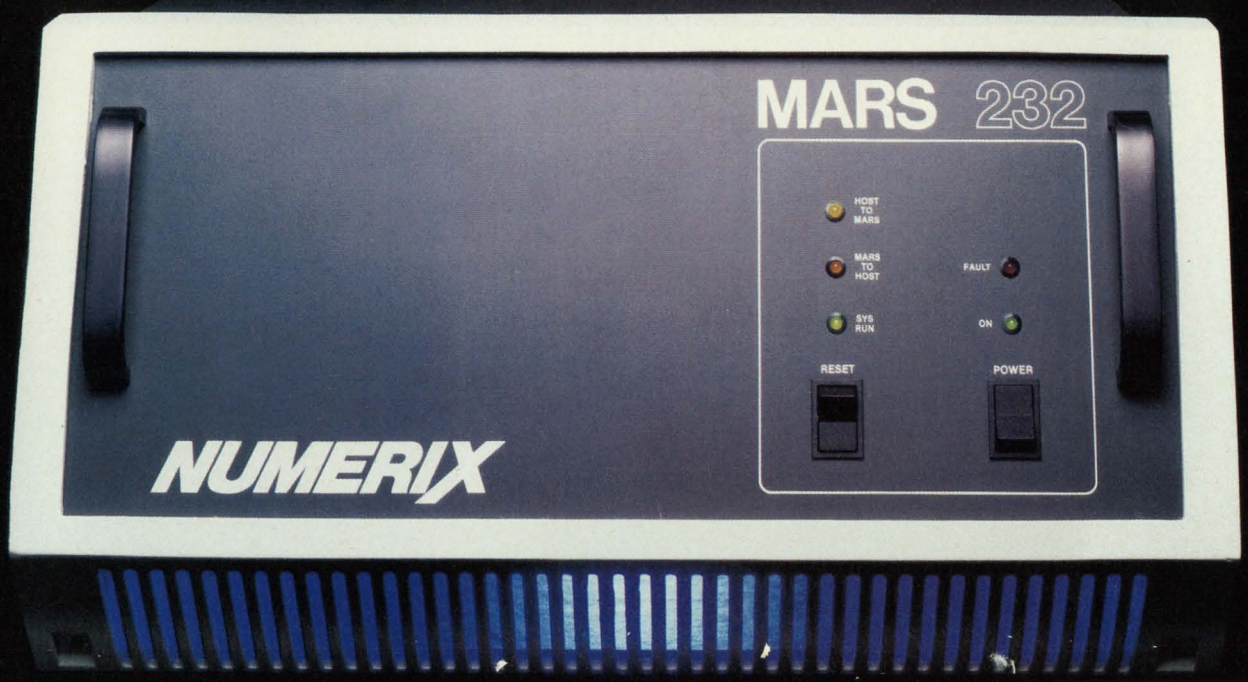
Array Processors

Perkin-Elmer and CSPI, have entered into a joint development agreement for operating 32-bit and 64-bit array processors with Perkin-Elmer's Series 3200 computer systems via a shared memory interface. The development effort is directed at the seismic and scientific calculation markets where Perkin-Elmer will be able to address computationally intensive requirements at a 10-100 times speed improvement.

Zilog Samples Virtual Memory μP

Now available in sample quantities the Z8003 and Z8004 Virtual Memory Processor Units from Zilog are 16-bit MOS μPs offering all the features of Z8001/2 CPUs, plus integral provisions for operation in a virtual-memory environment. The VMPUs operate at clock rates of up to 10 MHz and are fully binary-, function- and pin-compatible with the Z8001/2.

1K Complex FFT in 0.5 msec and faster...



MARS-232 Array Processors Support the User
who needs:

Signal Processing
with programmable high-speed arithmetic, logical, and decision-oriented operations for real-time applications.

Data Acquisition
directly into the processor at sample rates up to 20 MHz via a prioritized multi-port bus structure.

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using 32-bit digital I/O, A/D and D/A modules with speeds up to 5 MHz, all with software support for ease of integration.

Architectural Modularity
to configure ultra-high performance multi-processor systems reaching to 300 million arithmetic operations per second and beyond.

OEM Capabilities
where, as a development system, the MARS-232 supports low-cost ROM-based MARS-132's or customized user-defined VLSI implementations.

MARS-232 Array Processor Features Include:

- 1K Complex FFT Performance
  1.05-msec Single Data Processor
  0.5-msec Dual Data Processor
- 100-ns Clock
- DMA Transfers at I/O Bus Rates of 20 Mbytes/second
- Modularized 16- or 32-bit Arithmetic Units
- Multiple Processor Configurations for Application Flexibility
- Low-cost OEM Configurations
- Full Software Support at Systems/Utilities/Applications Levels

MARS-232 Array Processor Software
In today's world it is not enough to have outstanding hardware. Our interactive software system, GSP, allows hands-on assembly/disassembly, loading, debugging, and diagnostic services – with multiple processor support built-in. For the real-time environment, we use ESP, a host-resident executive. It provides intelligent supervision for host programs that call applications library or user-defined subroutines, without compromising the speed of MARS.

MARS-232 Applications
With its high computational capacity and low cost, the MARS family provides solutions for a broad range of application areas – on-line video inspection and image analysis; front-end data acquisition, compression, and formatting; spectral analysis, filtering and thresholding.

MARS- a new world of performance for medical, seismic, radar, sonar, and communications systems.

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For additional information on the MARS Family of High Speed Array Processors, write or call:
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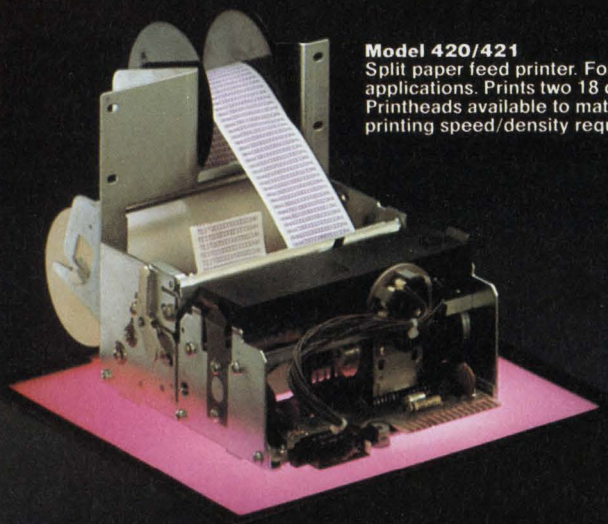
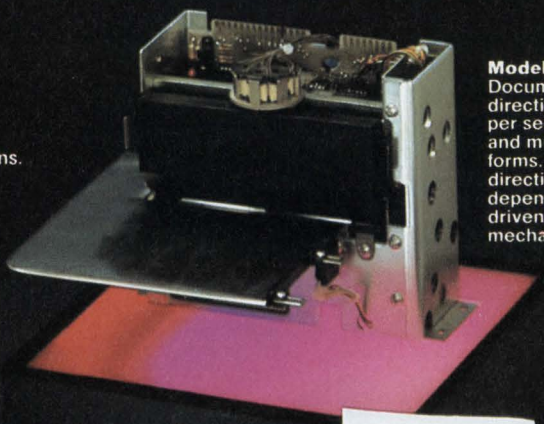
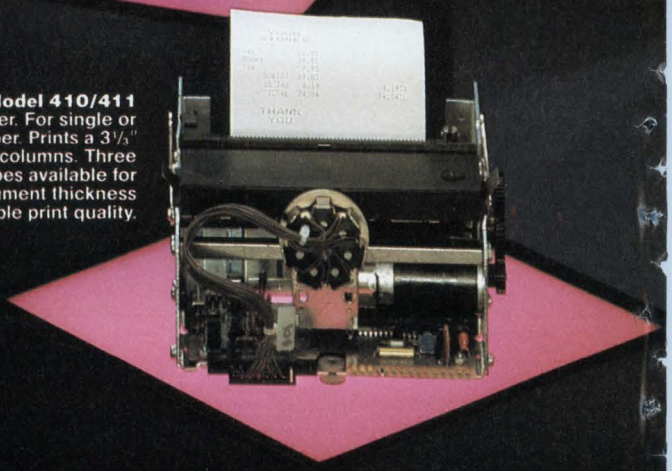


Model 420/421
Split paper feed printer. For receipt/audit applications. Prints two 18 character columns. Printheads available to match paper and printing speed/density requirements.

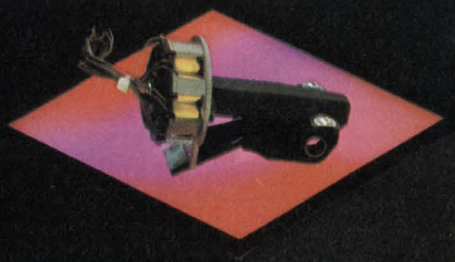


Model M-400
Document printer. Prints bi-directionally up to 3 lines per second. Handles single and multi-ply tickets and forms. Speed 3 lps bi-directionally. Has a quiet, dependable stepper motor driven paper advance mechanism.



Model 410/411
Single roll printer. For single or multi-ply paper. Prints a 3⅓" line up to 40 columns. Three printhead types available for various document thickness and dependable print quality.

Printheads
Choose from 3 printhead models for integration with your own equipment. All with a minimum of 100 million characters and lifetime, low maintenance reliability. Short, medium, and long stroke models. Available in either 40 or 24 VDC.



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Model 7000
Designed for commercial and industrial needs. Simple design, no special paper needed. Attractive case. 40 or 64 character capacity.

EATON Printer Products

News Update

Arcnet To Be Sold On Open Market

Datapoint Corporation, San Antonio, TX, has signed an agreement under which Standard Microsystems Corp, Hauppauge, NY was granted a non-exclusive license to market Datapoint's Arcnet transceiver chip. Together with Datapoint's RIM (Resource Interface Module) chip, Arcnet provides the electronics necessary for Arcnet interfacing.

Archive Streaming Tape For Plexus

Archive Corporation, Costa Mesa, CA, has been awarded a $1 million contract from Plexus Computers, Santa Clara. Plexus will incorporate the 20 Mbyte Intelligent Sidewinder ¼" streaming cartridge tape drives into their P/25 minicomputers. The Sidewinder will back up 8" Winchester disk drives with 22, 36, or 72 Mbytes of formatted capacity.

iAPX 286 Development Packages

The first software development and high level language packages for the iAPX 286 microsystem were announced by Intel Corp of Santa Clara. The new packages provide the first system and application design tools geared to the 286.

A price cut of over 50% was recently effected for the Intel 8087 numeric processor device for the iAPX-86 and iAPX-88 systems. Volume pricing is projected to drop further by half in 1983.

Rockwell Relocates Electronic Devices

The Electronic Devices Division of Rockwell Int. will relocate its headquarters from Anaheim to Newport Beach, CA, in an attempt to reduce facility costs and improve interdepartmental communication.

EXATRON'S RS-232C STRINGY/FLOPPY MASS STORAGE SYSTEM.

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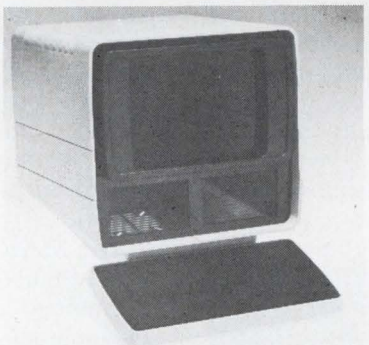

NEW!
Model 770
12" Monitor Housing
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High-Growth Of Surface Mounted Packages Forecast

The completion of a year-long study on electronic packaging has been announced by Integrated Circuit Engineering, Scottsdale, AZ. Entitled, "Electronic Packaging Strategies for the 80s," the major study encompasses seven volumes and represents distillation of technology gathered from Europe and Japan as well as the US.

ICE forecasts high growth of surface-mounted packages and makes a strong case for leaded, rather than leadless, chip carriers. The quad version of the cerdip (that ICE calls a "cerpack") could be a winning approach for hermetic packages that must mount on organic printed circuit boards—which ICE sees around for many years, yet. For non-hermetic packages, ICE sees the post-molded plastic quad pack as the replacement for the plastic dual-in-line package (DIP), and the quad structure lends itself to future assembly automation.

With the price of metallized tape falling and I/O densities rising, ICE sees that automated bonding (TAB) will attain significant growth, after languishing as a niche technology for a number of years. For IC I/O counts between 100 and 300, ICE sees TAB-like connection pads in the active area of IC chips, as opposed to being constrained to the periphery of the die.

For very high pin counts, however, ICE sees the "flip-chip" approach championed by IBM as the best way. ICE feels that improved substrate material and advances in wafer processing will allow this controlled-collapse solder bonding technique to accommodate up to 1,000 interconnects per chip.

The study predicts return of US-owned offshore package assembly as overseas wages rise and the value of individual components increase drastically. Computer modeling was used to determine life cycle costs of a number of typical device/package configurations to review impact on packaging. In-process inventory and process control will become more critical than the hourly labor rate by the end of the decade. Cost per interconnect will be reduced by a factor of four over the decade, and good cost payoffs are seen for multilayer polyimide substrates, new hermetic approaches, TAB chips directly on substrates and automatic die bonding.

Stackable Module Houses 16K-Byte Static CMOS RAMs

National Semiconductor has introduced a 16 Kbyte static CMOS RAM module, which includes decoding logic and decoupling capacitors, that not only requires only one-fourth the circuit board space of conventionally-packaged devices, but can also be stacked eight times to add memory up to 128 Kbytes.

The "stackability" feature of the MA2016 module, which enables increased packing densities, provides for vertical interconnection of up to eight modules to obtain a total memory capacity of 128 Kbytes. The module is also designed for horizontal "stacking" but requires suitable circuit board interconnection of the module.

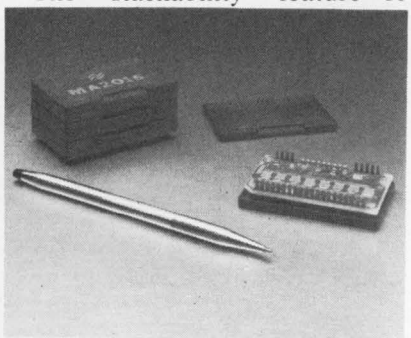


Figure 1: National Semiconductor's 16 Kbyte static CMOS RAM module includes decoding logic and decoupling capacitors, requiring only a quarter of the circuit board space used by existing devices.

The MA2016 stackable module was designed using a space-saving technology developed to reduce the number of parts required in the manufacture of calculators and handheld game modules. As the result of the substantial savings in board space, the MA2016 is suited for use in handheld computer terminals, handheld instrumentation, portable computer systems, telegraphics and telecommunications.

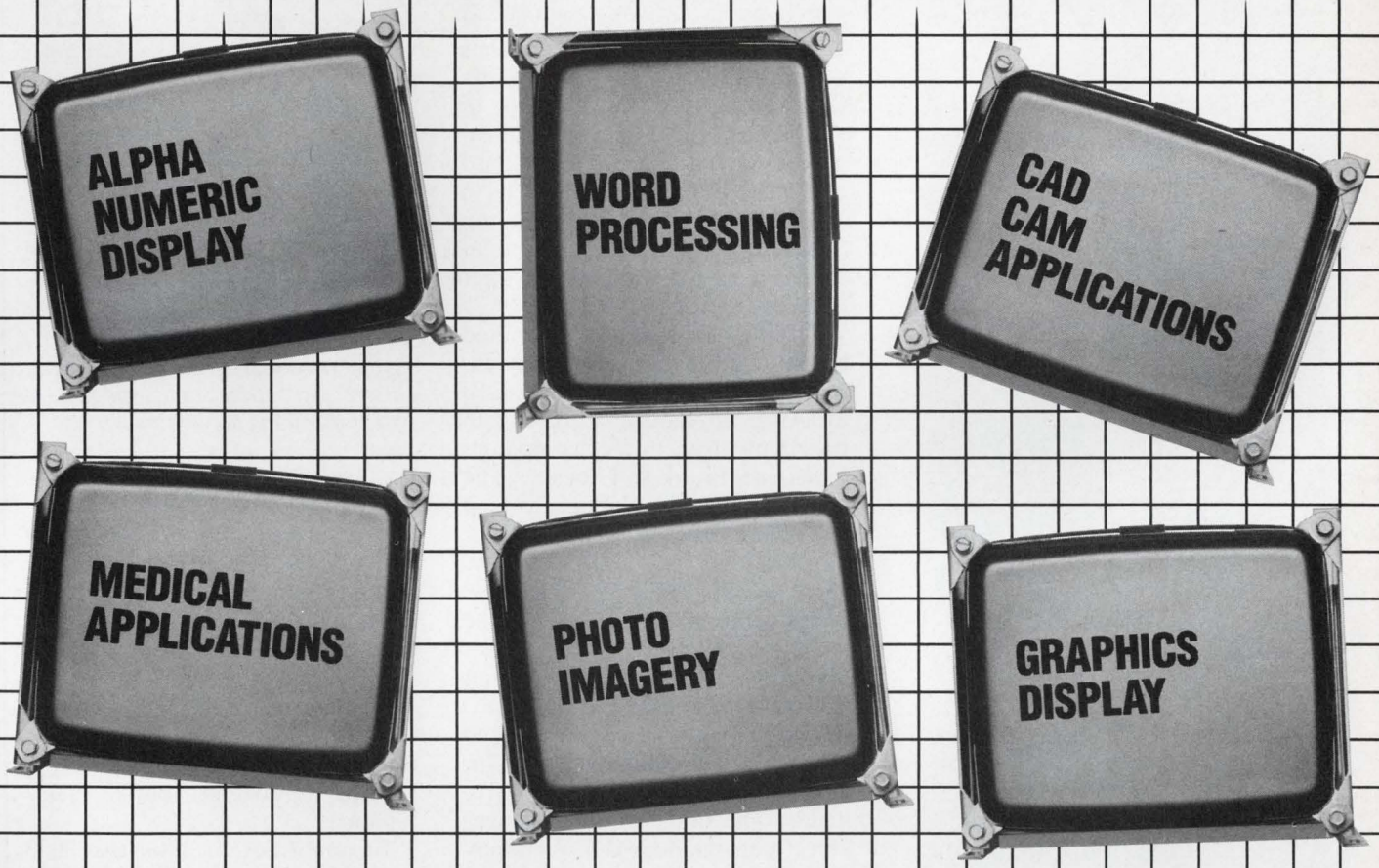
The MA2016 stackable module contains eight 6116 16 Kbyte RAMs, a high-speed P^2CMOS decoder, several fast CMOS gates, and two power-supply decoupling capacitors.

The complete module measures only 1.6" by 2.5" and is 0.35" high—about twice the width and the same length as a standard 40-pin DIP. The package has 40 pins on the bottom with the leads spaced 1.3 inches apart to facilitate mounting directly onto a printed-circuit board. Sockets on the top enable additional modules to be easily plugged in.

The memory of each module is structured as a 16 Kbyte by 8-bit block with an access time of only 250ns. Two jumpers located in a notch in the side of the module determine the address range of the 16 Kbyte block.

The module requires low power for operation—only 40mW—obtained from a single supply voltage of only 5V. Data can be retained at voltages as low as 2V. All inputs and outputs are TTL-compatible. Evaluation units of the MA2016 are available for $250 each.

Audiotronics... the American company that can satisfy your data display needs.



Yesterday's ideas might not be good enough for today or tomorrow, and selecting the proper data display has never been more significant. Recent studies in the computer marketplace indicate the CRT display has become the single-most important element in today's computer systems. An easy-to-read, jitter-free display is of course a dynamic part of this critical man/machine interface.

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High Capacity 5¼" Winchester Offers 30ms Access Speed

The first products of a family of 5¼" Winchester disk drives that can store up to 46.3 Mbytes of data and can be accessed in 30ms was introduced at this year's Comdex Spring show, held in Atlantic City, NJ. These high-capacity and fast access speed hard disk drives compare favorably in capacity to current 5¼" disks on the market but also perform at speeds usually found in the larger 8" disks.

The breakthrough is attributed to the combination of drive technology and the type of heads used by Atasi engineers, according to the San Jose, CA company's president, Frank C. Gibeau. "The combination of high capacity and fast access is vital for multi-user, multi-tasking μC systems," says Mr. Gibeau. While 5¼" hard disk manufacturers have pushed the available capacity on their products they have generally not met the need for fast access time.

The drive is a closed-loop servo with a linear actuator and Winchester-type ferrite read/write heads. The units are interchangeable with standard 5¼" floppy disk drives and can be mounted vertically and horizontally. Three initial members of the family are the 3020, 3033, and 3046—a 19.84 Mbyte, 33.07 Mbyte and 46.3 Mbyte-capacity units respectively.

Atasi's president says that the products are the first in the industry to use a closed-loop servo system with a linear voice coil positioner in the 5¼" package. Precise positioning is ensured through the ball bearing supported carriage. The bottom surface of the lowest disk contains the continuous servo code that is usually only found in the higher-priced 14" disks. Up to 4 disks may be loaded. The μC servo control provides self-test during the power-up sequence and access control during the track seeking mode. The servo system controls to within ±1% the speed of the eight-pole dc brushless spindle motor.

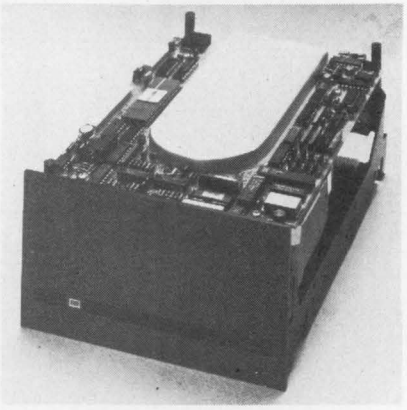

Figure 1: Model 3033 is a 5¼" Winchester disk drive that offers 33M bytes and 30 ms access time.

The recording media consists of a lubricated thin magnetic oxide coating on a 130-mm diameter aluminum substrate and the recording heads are composed of manganese zinc ferrite sliders.

So sure are Atasi engineers of their products' ruggedness that the company does not require the user to conduct preventive maintenance.

In quantities of 1000 the 3033 and 3020 units are priced at $1800 and $1470, respectively. Production is scheduled to start in September while the 3046 will premier in the fourth quarter this year and production will start in the first quarter of 1983. Price will be determined at introduction.

Atasi, which was formed in 1981, is making its task to provide the OEM market with 5¼" disk drives that will be price/performance competitive with their larger 8- and 14-in. counterparts. Two primary market segments will be served: the small business computer and local area network markets. Gibeau has assembled so far six individuals who together comprise 112 years of combined head, disk media, and drive manufacturing experience to meet that task—*Nicolas Mokhoff*

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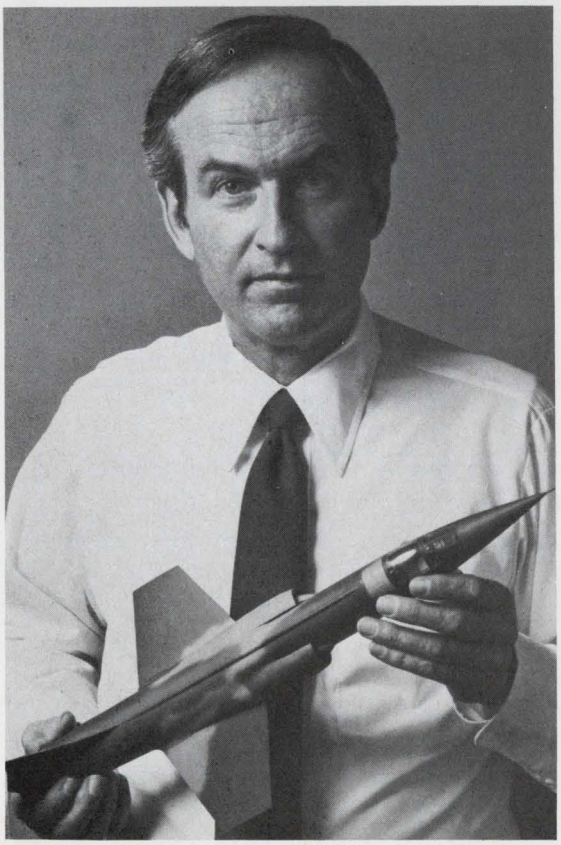

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Floppies To Pass The $1 Billion Level In '84

Very rapid increases in the use of 5¼" and 8" floppy disks, together with an upsurge in the new 3½" size, will push shipments of floppy disk media past the $1 billion mark by 1984, according to a new report from International Resource Development Inc. Flexible disk media (which recently overtook traditional hard disks in terms of media shipments) will lead the storage media market throughout the 1980's. Although optical disks will become commercially available in 1984, the principal applications will be in very large memory systems, leaving most of the memory market to magnetic media. By 1990 only about 9% of the media market will be for optical media, compared to almost 50% for floppies and 30% for Winchester media. **(Figure 1)**

Optical Versus Magnetic Media (Percentage By Shipment Value

	1982	1985	1990
Floppy	51.3	52.8	46.9
Winchester	8.4	16.7	28.7
Hard Pack	40.3	27.3	14.9
Optical	-	3.3	9.4
TOTAL	100.0	100.0	100.0

Figure 1: By 1990 only about 9% of the media market will be for optical media, compared to almost 50% for floppies and 30% for Winchester media.

Venture Capital

According to the report there will be a new round of opportunities for innovative start-up firms, paralleling the success in the 1970's of such firms as Verbatim, Maxell and Dysan. "Drexler Technology looks like the leader today in the optical disk media market," said International Resource Development's Ken Bosomworth, who cautions industry-watchers to note, however, that Drexler's main sales to date have been of evaluation kits to optical drive manufacturers. Bosomworth sees BASF, 3M and DuPont as all being threatened in the magnetic media field by ultra-thin metal coatings, deposited on new types of substrate materials by sputtering techniques. "It may turn out to be a horserace between the Japanese manufacturers—particularly Sony—and a new set of Silicon Valley startups," suggests Bosomworth.

IBM, which pioneered the flexible disk concept and was the leading supplier of floppy drives and media for many years, has been pushed out of first place in the floppy media market by Verbatim. Verbatim and other vendors frequently manufacture floppies on a "private label" basis to be sold by mail order companies, office supply stores, etc.

Computer Stores

In an analysis of distribution channels for floppy media, IRD concluded that computer stores had now pulled ahead of other types of distribution channels (including mail order computer products vendors, office supply stores and hardware manufacturers). The trend is expected to continue, both because of attractive pricing (some computer stores use floppy disks as "loss leaders" to attract traffic) and because of the convenience factor—when a user runs out of floppies, he tends to not want to wait one or two weeks for a new supply.

3½" Disks

With the expected introduction this year of 3½" floppy disk drives from several manufacturers, a new market will open up for 3½" floppy disk media. According to the IRD report, Sony, Hitachi and Maxell are already gearing up to supply this market with media. IRD analysts expect Verbatim and 3M to follow quickly.

Optical Disk Media

In analyzing the state of the art in optical disk technology, researchers are looking at several different materials for the substrate and the recording layers. Recording material might be metal and polymer compositions, vesicular films, bilayers or infrared-absorbing organic materials. Metals considered for the recording layer include tellurium, silver, gold, platinum, selenium and bismuth. Other possibilities are absorbing organic materials such as cross linked gelatin, by Drexler; homogeneous grain free films, by Kodak; and metal composite films in polymerized plasma, by Nippon Telephone and Telegraph.

Substrate materials are also very important. Possible materials include aluminum, glass, polycarbonates and microtextured-Teflon based polymer materials. The latter enhances the heating effect and reduces the power required to modify the recording film. "Many of the aspiring optical disk drive manufacturers are faced with an awkward choice right now," reports Bosomworth. "Almost everyone is having pesky dropout problems with experimental optical media, and a number of manufacturers are leaning towards the use of Drexler's Drexon material. But industry rumors are that Control Data and at least two other vendors have rejected Drexon because of problems with error rates."

International Resource Development Inc.'s report (#502) entitled Optical And Magnetic Disk Media is available at $1,285. For further information contact: IRD, 30 High Street, Norwalk, CT 06851 (800) 243-5008 (in CT or outside the U.S. (203) 866-6914); Telex 64 3452.

PABX And LAN Integrate With Energy Management Systems

Strong market potential throughout the 1980s for PABX, local area network (LAN) and energy management markets will motivate suppliers to integrate systems to provide new applications. Combined revenues for shipments of PABXs, LANs and energy management systems (EMSs) will nearly double this market's current 1.3 billion figure to reach $2.3 billion by 1985.

Technological achievements in the areas of wideband digital transmission and very large scale integration (VLSI), increased market competition, the deregulation of the communications industry, as well as continued energy conservation, are all factors driving the integration of energy management with communications networks. A complete breakdown of the LAN/EMS/PABX market is shown in **Figure 1.**

Energy management features are used to generate new revenues for PABX manufacturers while providing customers with energy savings to offset the costs of a PABX purchase. They may be provided on a PABX by total system integration or a two-vendor approach. Total system integration provides the highest market sophistication in which the PABX processes information in addition to switching information. Currently, one single-vendor approach exists and is used by American Telephone and Telegraph Company (AT&T). However, a two-vendor approach will better meet the immediate needs of many suppliers and ensure adequate energy management and PABX expertise. The two methods for this approach are:

- Separate processors and separate communications networks with a processor interface capability. This provides a single user interface and is used by Stromberg-Carlson.
- Separate processors and shared communications networks. This approach is used by CEDCO, Inc. and Universal Communications Systems.

The large installed base of PABX systems is the first market for PABX suppliers to penetrate with energy management capabilities. The AT&T Dimension-based EMS, priced at $400-$700 per point, is not cost competitive and offers only basic energy management features. However, the industry-specific approach taken by the large Bell marketing network has been very successful. Initially, PABX-based systems have been marketed to the less sophisticated hotel and health care sectors. However, significant customer savings make systems appealing to other sectors as well, as shown in **Figure 2.** The maximum potential EMS market will reach $14.5 billion if 100% penetration is achieved. New suppliers should provide advanced features including optimum start/stop and HVAC reset, demanding two-way communications capabilities to penetrate various industry sectors.

An analysis of this market potential is outlined in the recently published MAPTEK USA Worldwide Energy Opportunities Programs report entitled, "Energy Management Opportunities On PABX Systems." For further information, contact: Quantum Science Corp., 1114 Avenue of the Americas, New York, N.Y. 10036, (212) 997-0070.

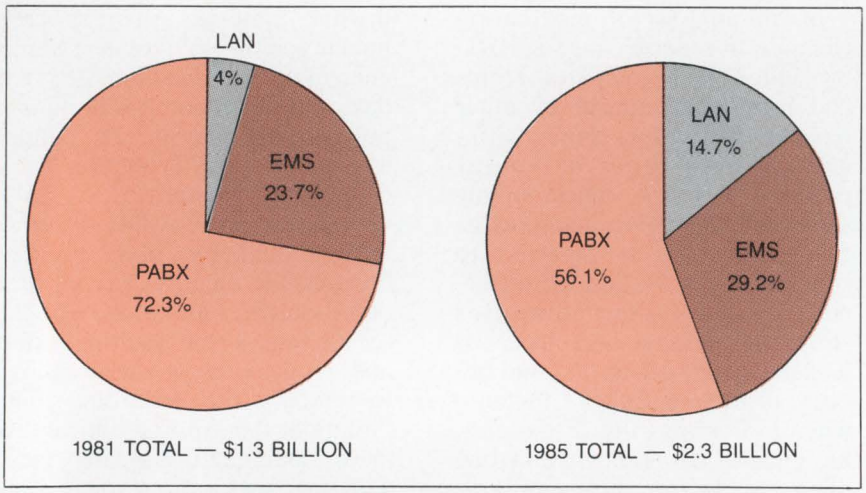

Figure 1: Total PABX/Energy Management System/Local Area Network Shipment Forecast shows the market nearly doubling by 1985.

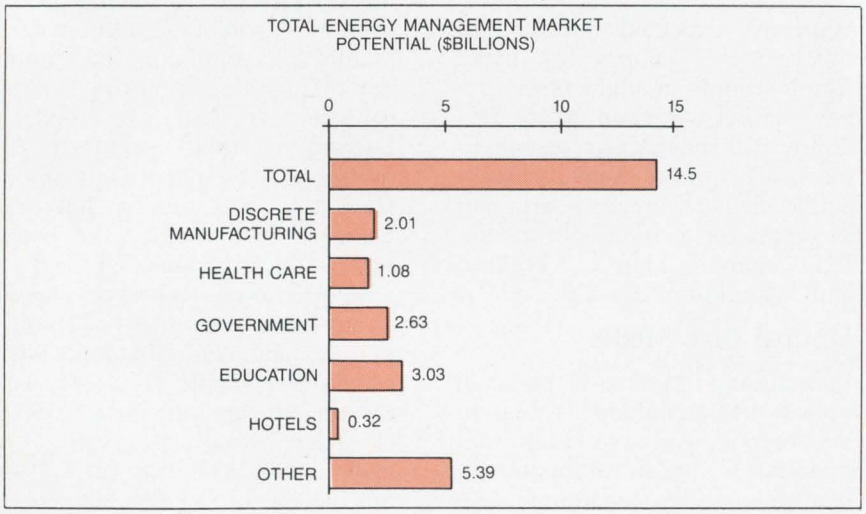

Figure 2: The maximum potential EMS market could reach $14.5 billion.

Keyboard Input Favored Over Touch And Voice

Managers place a significantly higher value on a full keyboard than on either a touch screen or voice input devices according to a recent market study on management workstations. Advanced Resources Development, a Boston area consulting firm, found that the recently acquired experiences of managers in the operation of interactive printer terminals, CRT terminals, word processors and personal computers are responsible for their increasing acceptance of keyboarding. Even though managers may not want to key in long documents or piles of data, they have come to view the full keyboard as the major control device on a computer system.

Office automation vendors have recently introduced new operator interface devices to allow managers to use workstations without keyboarding. The "mouse" cursor control used on the Xerox Star workstation allows the user to select icons or pictures representing common office functions or menu items listed on the screen. Touch sensitive screens provide another alternative to permit the user to point directly to items on the screen. Excalibur Technology has introduced voice recognition of simple commands on a workstation geared for executives. Preprogrammed keys, which perform a complex series of operations with one keystroke such as "find" or "select" are also being designed on workstations. Programmable keys, such as those offered on the Corvus workstation, allow changing functions for the keys with each application.

While managers will appreciate the added convenience of the new interface devices, most are not willing to trade in a full keyboard for a bank of "idiot" buttons, "cartoon" graphics, or a touch screen. Most of these workstation interface enhancements are best suited for aiding the infrequent user in accessing stored information.

IBM and Wang have recently announced voice messaging systems touting them as "breakthroughs" in overcoming resistance to office automation. Voice messaging systems enable users to record messages for electronic storage distribution while eliminating the need for keyboard input. However, ARD found that voice storage was not a highly valued workstation feature. While voice is the most heavily used communication method for business interaction, managers do not appear to be quite ready to talk to machines.

It is projected that the workstation market will grow at a healthy 40% per year through 1986. More than 4,500,000 workstations valued at $25 billion will be shipped during the five year period from 1982-86. **(Figure 1)** Four types of computer products including desktop business computers, multifunctional word processors, computer terminals, and specialized workstation devices will be configured with software and communications to support management workstation applications. By 1986, specialized workstation devices based largely on the microcomputers used on desktops today will account for 32.3% of the unit shipments. General purpose desktop computers will continue to play an important role in the management workstation market due to their lower cost compared to more specialized products.

More information on this study of the management workstation market entitled, "Management Workstations: Markets and Strategies 1981-1986," is available from Advanced Resources Development, 28 A Park Street Station, Medfield, Massachusetts 02052. (617) 359-8090.

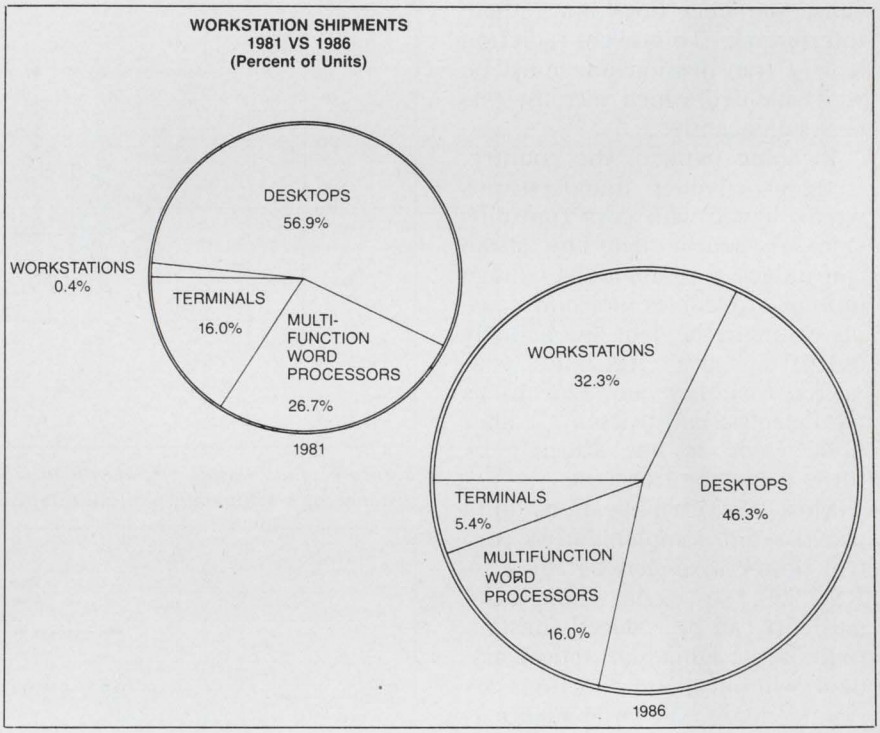

Figure 1: By 1986, specialized workstation devices based largely on the μP used on desktops, will account for 32.3% of the unit shipments.

Fiber Optic Modem Provides Good Noise Immunity

One of the most common applications of fiber optics is the transmission of RS-232 computer data. The outstanding noise immunity of fiber optic cables allows them to be installed in existing cable trays near noisy power cables without interference causing data errors.

Stricter FCC regulations regarding EMI (electro-magnetic interference) or RFI (radio frequency interference) also make a fiber optic system attractive because the fiber does not radiate interference. To prevent radiation a wire transmission line must be well shielded which increases its cost significantly.

In some parts of the country, frequent summer thunderstorms wreak havoc with data transmission. A nearby lightning strike can induce a tremendous voltage in long wire cables, not only causing errors in the data, but actually destroying any electronics connected to either end. Due to its all-dielectric construction, a fiber optic cable is not affected by these damaging transients.

Most RS-232 applications don't use the full complement of control protocol spelled out by EIA RS-232C, so circuit complexity and cost can be reduced substantially by designing an optical modem without these functions. A simple circuit, shown in **Figure 1,** will give excellent performance at minimum cost. A bit error rate (BER) of 10^{-9} or better can be achieved over a distance of more than 5 kilometers without a repeater. Cable selection will determine how far the modems will transmit. **(Table 2)**

With the circuit shown in **Figure 1,** simplex, half-duplex or full duplex operation is possible between modems. A dual-fiber cable (or two 1-fiber cables) can be used to transmit the optical data. A system block diagram is shown in **Figure 2.**

The circuit **(Figure 1)** consists of a Burr-Brown fiber optic transmitter and receiver with level-shifting circuitry to convert the TTL levels required by the FOR110KG and FOT110KG to standard bipolar RS-232.

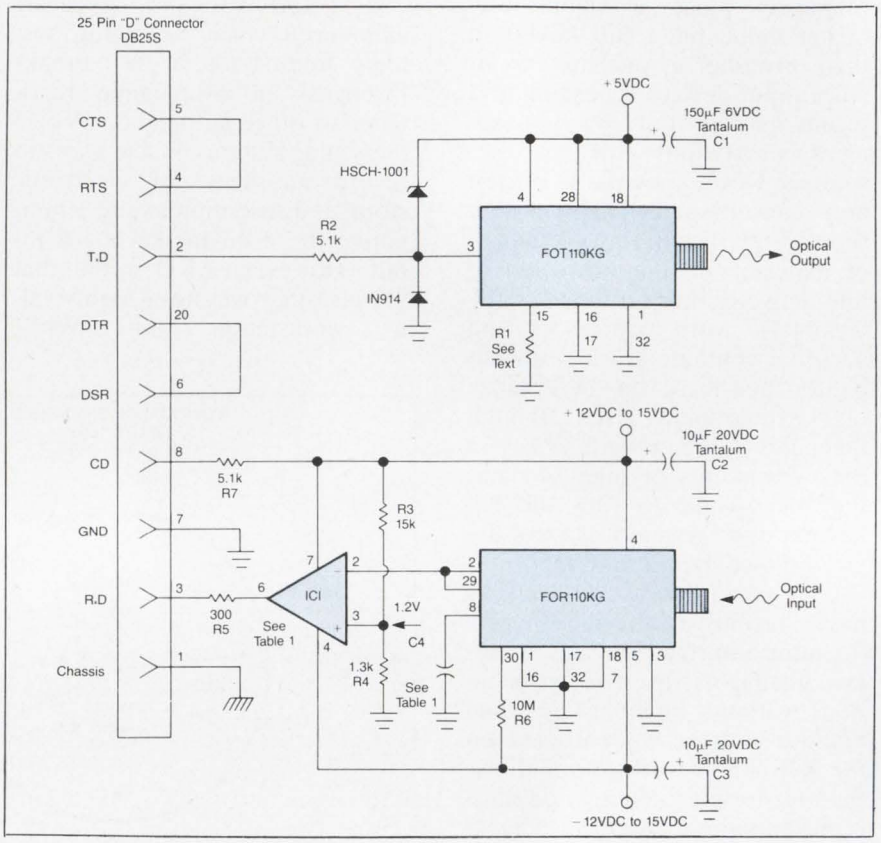

Figure 1: This simple circuit will provide bit error rates of 10^{-9} or better over a distance of 5 kilometers without a repeater.

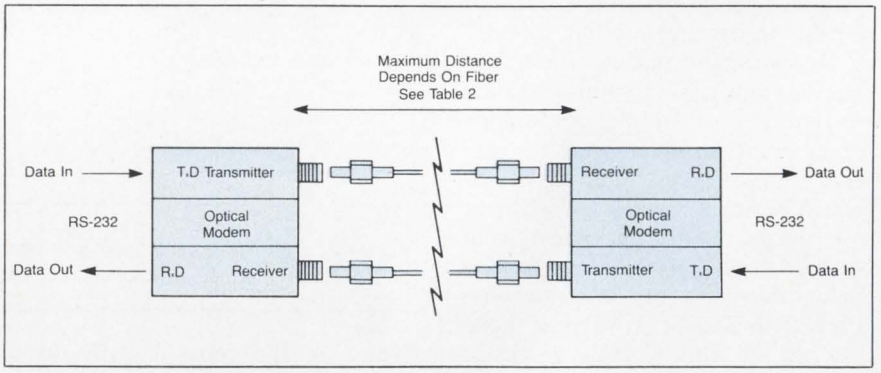

Figure 2: System block diagram.

R_2 determines the input impedance and together with D_1 and D_2 clamps the $\pm 3V$ to $\pm 25V$ input to a safe level. R_1 is used only when it is necessary to reduce the transmitter output power to prevent receiver overload which could occur with very short links. **Figure 3** shows the transmitter output power vs. R_1. For maximum power, pin 15 is simply grounded. A "Mark" input will turn ON the transmitter LED.

The TTL output of the FOR110KG is converted to about $\pm 12V$ by using an op-amp, IC_1, as a comparator. The voltage divider formed by R_3 and R_4 set a

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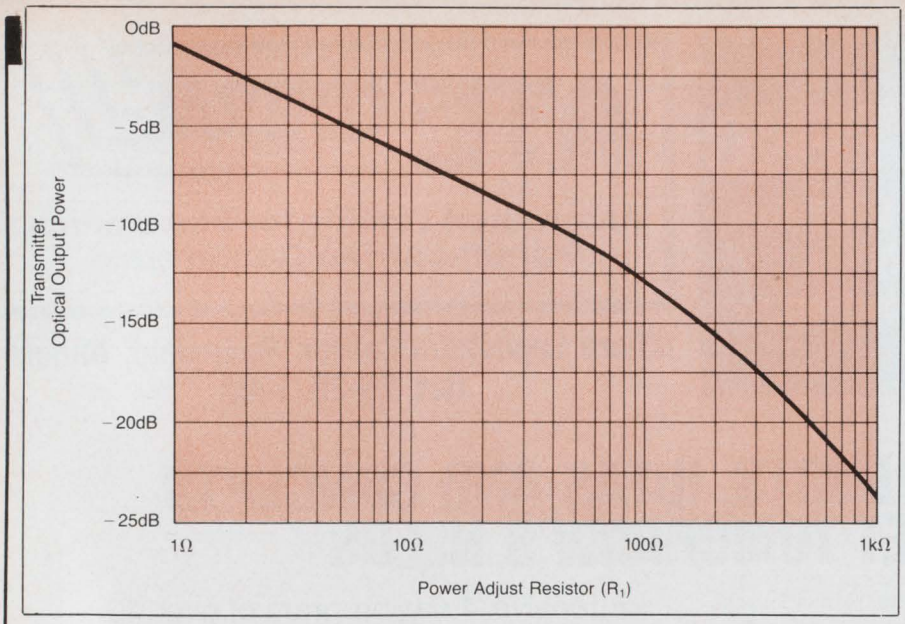

Figure 3: Transmitter optical output power vs. power adjust resistor.

±1.2V threshold for IC_1. Depending on baud rate, a 741 or NE530 is used to purposely limit the output slew rate. Internal op-amp current limits and R_5 serve to meet the RS-232 requirements for driver output short-circuit current and power-off output resistance. The receiver's automatic threshold detector allows hands-off operation, as no adjustments are required to compensate for age or temperature.

To transmit true DC so that the link can be totally "transparent" (in other words, the baud rate can go to zero) the squelch function of the FOR110KG is used. This overrides the auto threshold circuit when the input signal drops to zero for more than a few seconds, keeping the bit error rate very low. Below an input of about 40nW, the open collector squelch output clamps the data comparator output to prevent the internal comparator from triggering on noise. With pin 30 open, the squelch level will be about 20nW, giving a little more receiver sensitivity but with a small BER penalty (10^{-9} instead of 10^{-14}) if the baud rate is less than about 2 or the optical line is broken. The receiver is phased so that an idle optical line (LED ON) gives a "Mark" output.

Excess bandwidth which contains more noise than information is rolled off by C_4. This capacitor isn't absolutely necessary but since it improves the BER significantly, it's worth including.

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The key to the M23 System, Dataram's proprietary memory management Q-MAP enables you to use the full 4.0MB power of the LSI-11/23. It provides I/O mapping, which supports a wide range of existing peripheral controllers on an 18-bit bus (Q18). While still maintaining the 22-bit bus (Q22) for 4.0MB main memory addressing.

DEC® software compatibility?
The M23's Q-MAP emulates DEC's KT24 memory management, which means it operates with RSX11-M, RSX11-M PLUS, RSTS, UNIX, and all other DEC operating systems which support the KT24.

Memory?
A 1.0MB quad board is contained in the basic M23 configuration. Think of it, a full 4.0MB on only four DEC quad boards! And each additional 1.0MB is only $3400.

System configurability?
The 5¼" M23 provides an incredible 27 DEC dual slots. And since the basic configuration (LSI-11/23, OCU, two SLUs, Q-MAP, bootstrap/diagnostic PROMs, and 1.0MB memory) occupies only six of those 27 slots, that leaves you 21 slots to configure a high-performance LSI-11 system.

5.0 volt current?
36 amps.

Price?
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More information?
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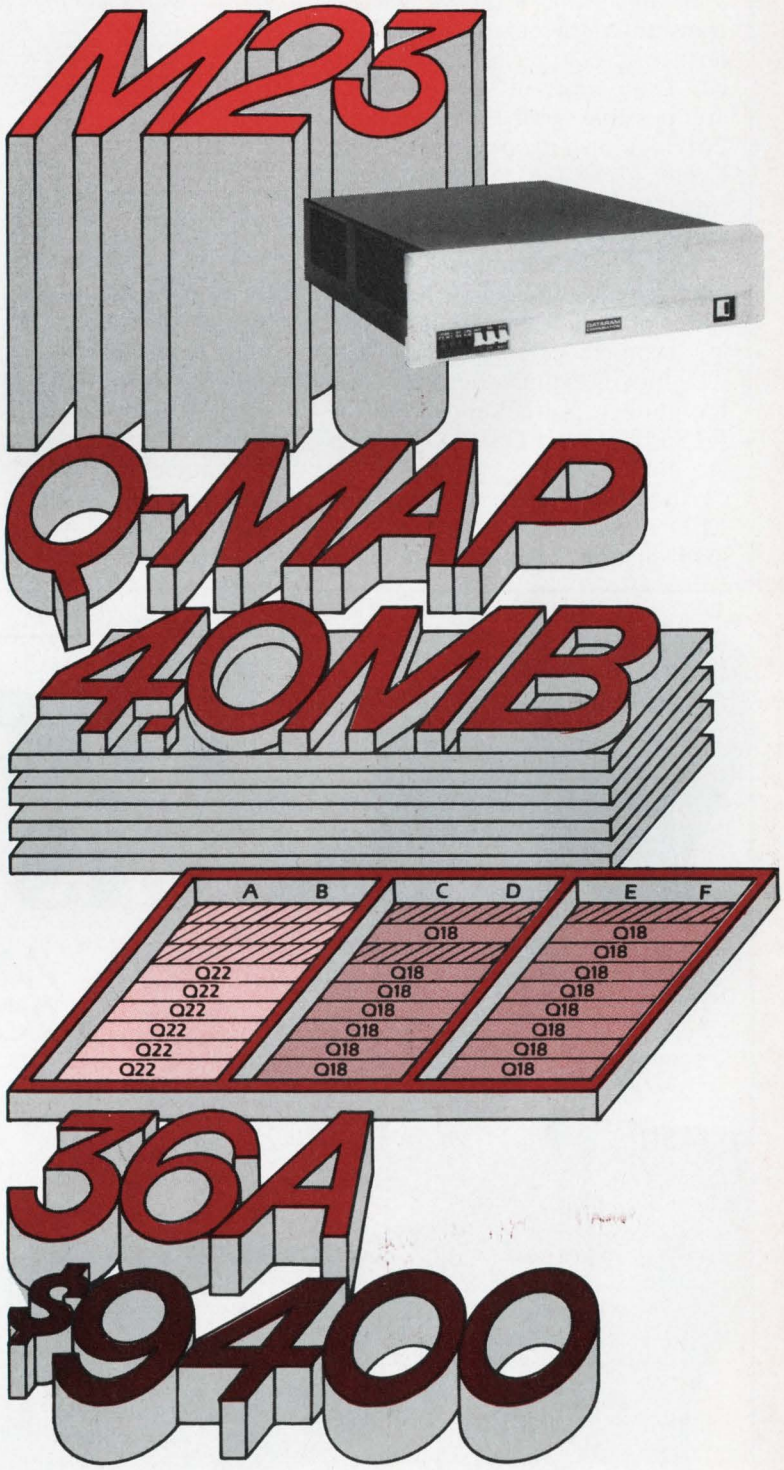

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scope probe on pin 8. This signal appears as a negative voltage of about −1V per mW of optical input power. Excellent BER performance is assured if a comfortable signal input margin is detected at pin 8 **(Figure 4).**

If only TTL level signals are transmitted the extra RS-232 interface circuitry can be eliminated. Data rates of 2 MB/S NRZ are possible with this TTL link. For high speed operation reduce C_4 to 47pF and avoid excessive capacitive loading of pin 8 by the scope probe.

The RS-232 connector is a 25 pin female D connector with some provision for accommodating protocol oriented lines. The CD line is simply derived from the modem power supply and the RTS/CTS and DSR/DTR lines are looped back.

Additional circuitry such as LED indicators for T_x or R_x, or handshaking protocol could be added, of course, if desired. A fully functional CD line can be derived from the open-collector squelch output (pin 29) of the receiver. The data output can also be squelched by AND'ing the data out (pin 2) with the squelch out (pin 29).

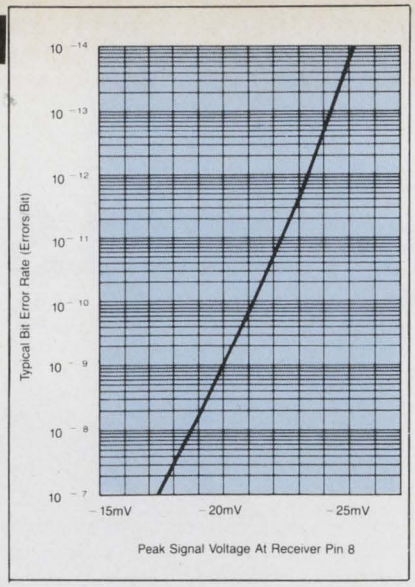

Figure 4: Typical bit error rate vs. peak signal voltage at receiver pin 8.

To select a fiber optic cable for use between modems, first determine the desired link length. If the distance is less than 100 meters the FOT110KG can be used with an all-plastic fiber such as Eska or DuPont PIFAX. The 665nm visible red wavelength transmitter performance is excellent with plastic fiber and its visible output makes optical troubleshooting very easy. It can also be used with other cables to give links of over 2 kilometers.

For applications requiring very long links without repeaters, the higher power FOT110KG-IR infrared transmitter will have good performance with appropriate fibers to over 6 kilometers. Do not use the -IR transmitter with plastic fiber since the attenuation of most plastic fiber is so high in the infrared (880nm) that performance would be very poor despite its higher output power.

Link lengths for a variety of fibers are shown in **Table 2.** These

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TABLE 1

NRZ BAUD RATE	IC1	C4
0 to 9.6kB/s	741	4700pF
0 to 100kB/s	NE530	470pF

Table 1: Values of IC1 and C4 and the NRZ baud rate.

TABLE 2

MAXIMUM DISTANCE	FIBER	TRANSMITTER
6.1 to 8.4km	AM FOX 2010	FOT110KG-IR
2 to 3.8km	SIECOR 142	FOT110KG-IR
1.7 to 3km	ENSIGN-BICKFORD HC-310-TA	FOT110KG
1.1 to 2.3km	MAXLIGHT MSC200A	FOT110KG

Table 2: Selection of cable will determine how far the modems will transmit.

distances are calculated for both typical and worst-case performance specifications for the transmitter, receiver and (where possible) for the fibers. If splices or connectors are added between modems the link lengths will be reduced. When buying fiber optic cables, a maximum attentuation specification at the system operating wavelength should be negotiated with the cable manufacturer. Don't place your system in jeopardy by relying on "typicals".

Although a fiber optic system is capable of achieving very low error rates **(Figure 4)** because of the optical fiber's immunity to noise pickup, noise can still enter the system through the modem electronics. Mounting the circuits in shielded metal housings and providing RFI filtering on AC power lines will help preserve data integrity. Since this circuit's power requirement is very low, a modular triple supply such as a Wall Industries W15T100 can even power a secondary channel. Simply duplicate this circuit and use the RS-232 secondary input and output pins in the 25-pin D connector.

Using these hybrid fiber optic data link components, a high quality optical modem can easily be built on a small PC board.

Neil Albaugh, Burr-Brown Research Corp, Tucson, AZ.

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μP Development Systems: More Choices For The User

by Dave Wilson

Several different strategies have emerged in recent years from the vendors of μP development systems. The semiconductor manufacturers, such as Intel, Motorola, etc., have sought to support their own users as they migrate towards a greater level of functionality in their μPs. The instrument makers, such as Tektronix and Gould, have sought to cover a broader base of μPs from many different chip houses. A third slice of the business consists of independent software companies, such as Boston Systems Office, Boston, MA, who write translation programs running on general purpose minicomputers and mainframes.

With the personal computer firmly entrenched in many engineering labs, some engineers are now using them for μP-based project development. For less software intensive applications, this is a very cost-effective route to take. The Gloucester Computer Bus Co., in MA, for example, supports the Commodore VIC-20 computer with a cartridge that provides EPROM programming, operating and emulating capability specifically for that computer.

Intel has recognized this section of the market and has designed a product (the Intel personal development system) at a price comparable with those of general purpose personal computers.

One newcomer to the market that has not come from these more conventional sources is from Digital Equipment. With the decision to sell μPs such as the T-11, DEC has introduced support in the form of their MDT/T-11 development system.

Product ranges will continue to broaden so the prospective buyer will have a wide variety of cost/performance trade-offs to analyze and interpret before making his final decision.

Design Steps

The major steps for a μP design project are outlined in **Figure 1.**

The product is first defined, and the hardware and software assignments are divided. The hardware team then begins an independent effort to design the prototype circuitry. If the software program to be written is large, the software team may divide it up into modules—code will be written for each module in high level and/or assembly language, using an editor to create source code files. A compiler or assembler translates these files into object code and a linker/loader then combines these object modules into object code executable by the prototype hardware. Finally, the code is ready to be in-

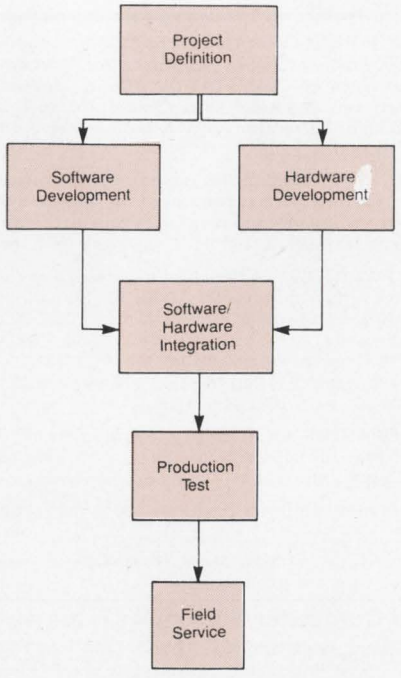

Figure 1: Major steps involved in developing a μP-based product. After product definition, the hardware and software assignments are assigned. If the software program is large, the software team may divide it up into modules and combine the modules into code executable by the prototype hardware. The specific nature of the design aids will depend to a great extent on the design environment.

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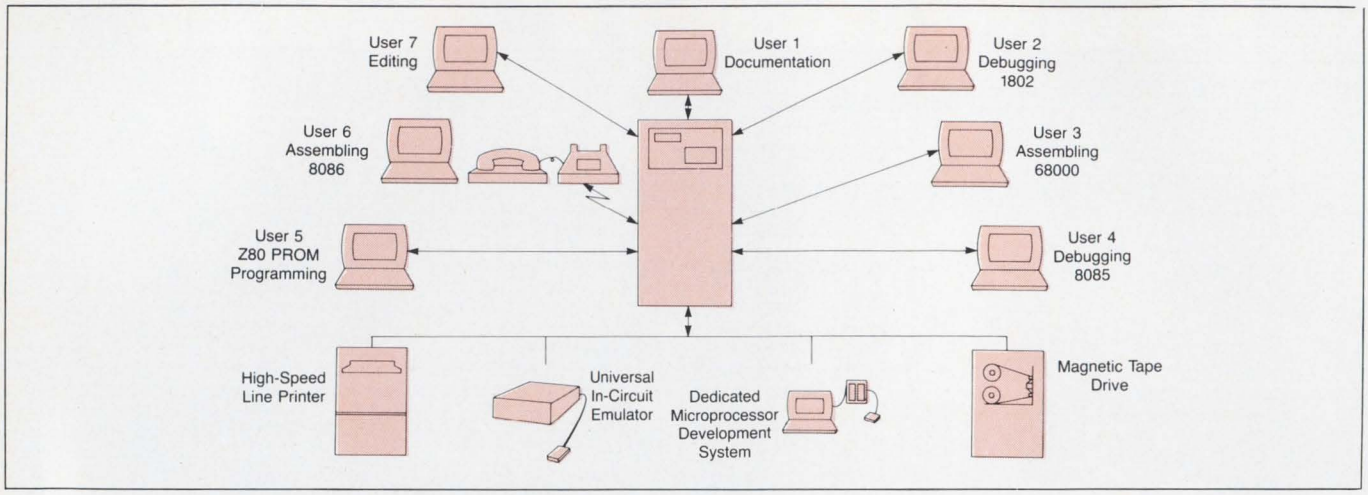

Figure 2: A Universal Development System can support a large number of terminals for software development.

troduced to the prototype hardware. According to Tektronix, the actual hardware/software integration often consumes up to 50% of the project's labor time.

After each round of debugging, the source code must be updated, reconverted to object code, linked and then loaded for further execution in the prototype hardware.

The specific nature of the design aids used will depend to a great extent on the design environment.

At the Eascon conference, Michael Rooney of Boston Systems Office presented a paper that made some very pertinent comments about the choice of development systems. The choice of programming in assembly language or high level language depends on whether the program will be used in just one or two products or a large number.

When the quantity being produced is small, the time it takes to develop either the hardware or the software is a much higher percentage of the total system cost than the price of the processor and its memory. This is especially true the more complicated the program and the larger the sale price of the completed system.

Alternatively, if the production run will be important then assembly language may be the choice to keep down the number of chips used.

Universal Development Systems

Universal development systems, typified in **Figure 2** from Boston Systems Office, can support from one user to more than 100. The BSO line is based on high-speed 16- or 32-bit computers from DEC. (Alternative systems may be based on Data General's computers.)

With the advent of 16-bit machines with larger address space, it seems evident that programs will be written in multiple modules, then joined into one complete program with a linker program.

BSO provides MLINK that has the capability to link an unlimited number of program modules. The final output of MLINK is a complete program in absolute object format.

The concept of increasing software productivity by moving software intensive activities away from the traditional MDS to a more powerful minicomputer, and leaving the MDS for system integration and final test, is also supported by Systems and Software Inc., Downes Grove, IL and Virtual Systems, Walnut Creek, CA.

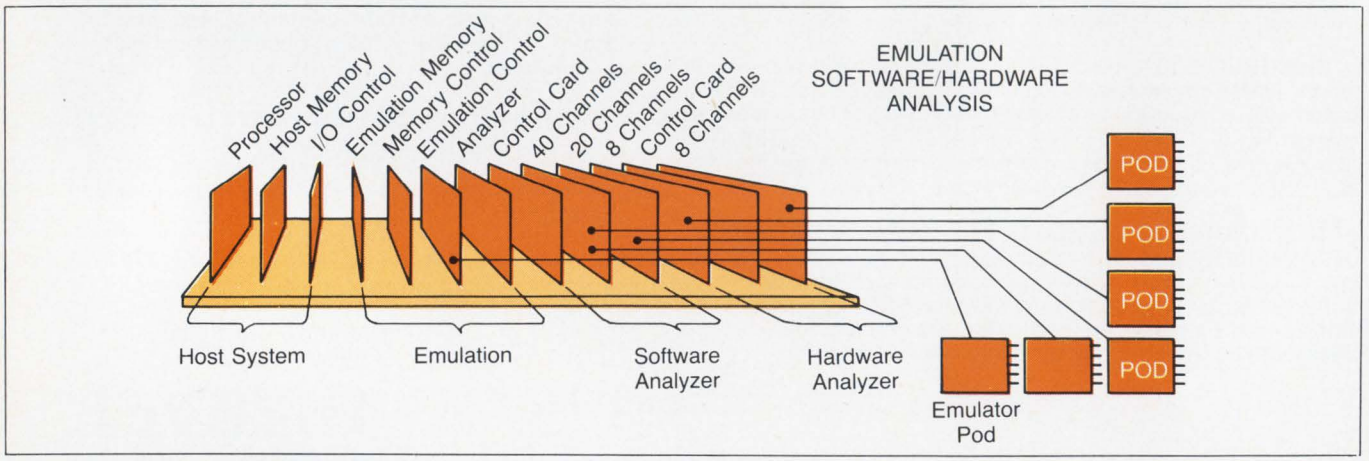

Figure 3: A number of plug-in boards allow the user to configure the HP64000 to solve his particular problem.

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Package To Perform Real-Time Emulation Of 6 MHz Z80B

Designed for Starplex and Starplex II development systems, this 6MHz Z80B package from National Semiconductor, Santa Clara, CA supports program development and single-processor emulation. In the program development mode, the user is permitted to develop and debug his software in real time even when no prototype hardware is available. In the single-processor-emulation mode, the user's hardware provides the actual clock signal, allowing the entire Z80B ISE package to operate at the actual clock rate of the user's prototype system. Included in the Z80B ISE package are the emulation board, lightweight plastic cable pod, cables, complete software, trace board, high-speed (55ns) 32 Kbytes mappable memory board and TTL status pod.

New Emulators For Z80 & 8085

The ZAX (Westminster, CA) Model ICD-178 In-Circuit emulators function as either stand-alone emulators for product development and production testing or as a lightweight portable tool for field service use. As a stand-alone device, the ICD-178 may be tied to a computer for downloading of development software. The ICD-178 features a full 64K of mappable memory for both the Z80 and the 8085 eliminating loss of development time caused by inadequate memory capacities. Another key feature of the ICD is it's ability to patch software in symbolic code. For field applications, the ICD-178 can be connected to any communications device that accepts an RS232C or 20mA current loop input.

Basic 3 Interpreters Simplify Program Development

A pair of ROM-based Basic 3 high level language interpreters for use with Cosmac Microboard Computer Development Systems (MCDS) are available from the RCA Solid State Division, NJ. The CDP18S841 Basic 3 Interpreter is offered in two versions: the first is designed for an RCA MCDS equipped with a cassette tape drive; the second, called Run-Time Basic, CDP18S842, is intended for use in target systems comprised of RCA Microboard modules.

6809E Cross Assembler Released

In keeping with it's expanding support of Motorola processors, Millennium Systems has announced cross assembler support for the Motorola 6809/6809E μPs. The cross assembler is designed to run under CP/M 2.2 and MP/M 1.1 operating systems on the 9520 Software Development System. It is compatible with all other Millennium cross assemblers and consistent with the manufacturer's instruction mneumonics. Millennium macro cross assemblers generate relocatable code, and are supplied with a linker. They are designed to run on Millennium's 9520 Software Development System as well as other Z80 CP/M and MP/M based systems providing system software/hardware support for 6809/6809E product development. Other CP/M compatible cross assemblers are available for Intel 8080/8085, 8048 family (absolute only), Motorola 6800/6802, 6801/6803, 6809/6809E and Zilog Z80.

Systems and Software's product line runs on DEC's PDP-11 or VAX series; they provide support packages that include the REX-80/86 real-time executive, PASCAL run-time support, and multiple processor extension-MPX. All run-time support packages are organized as object libraries that are managed by the object-code librarian and are directly compatible with the linker.

The REX-80/86 real-time executive supports powerful real-time programming facilities including task synchronization, device independent operations, time based management and dynamic buffer management. REX-80/86 requires less then 4 Kbytes of code space and 256 bytes of RAM for operations and is totally RAMable.

Virtual Microsystems' product, INCOMM, allows data transfer between PDP-11 and Intel MDS systems via local cable or switched telephone networks using standard RS-232 communications. Programs may be assembled or compiled on the PDP-11 system, transmitting, via INCOMM, the resulting binary code for testing. Even source programs written to Intel Fortran-77 or PL/M language specs may be developed and maintained on a PDP-11 system, and via INCOMM, downloaded to the Intel MDS for compilation, with the listings being uploaded for printing on the PDP-11.

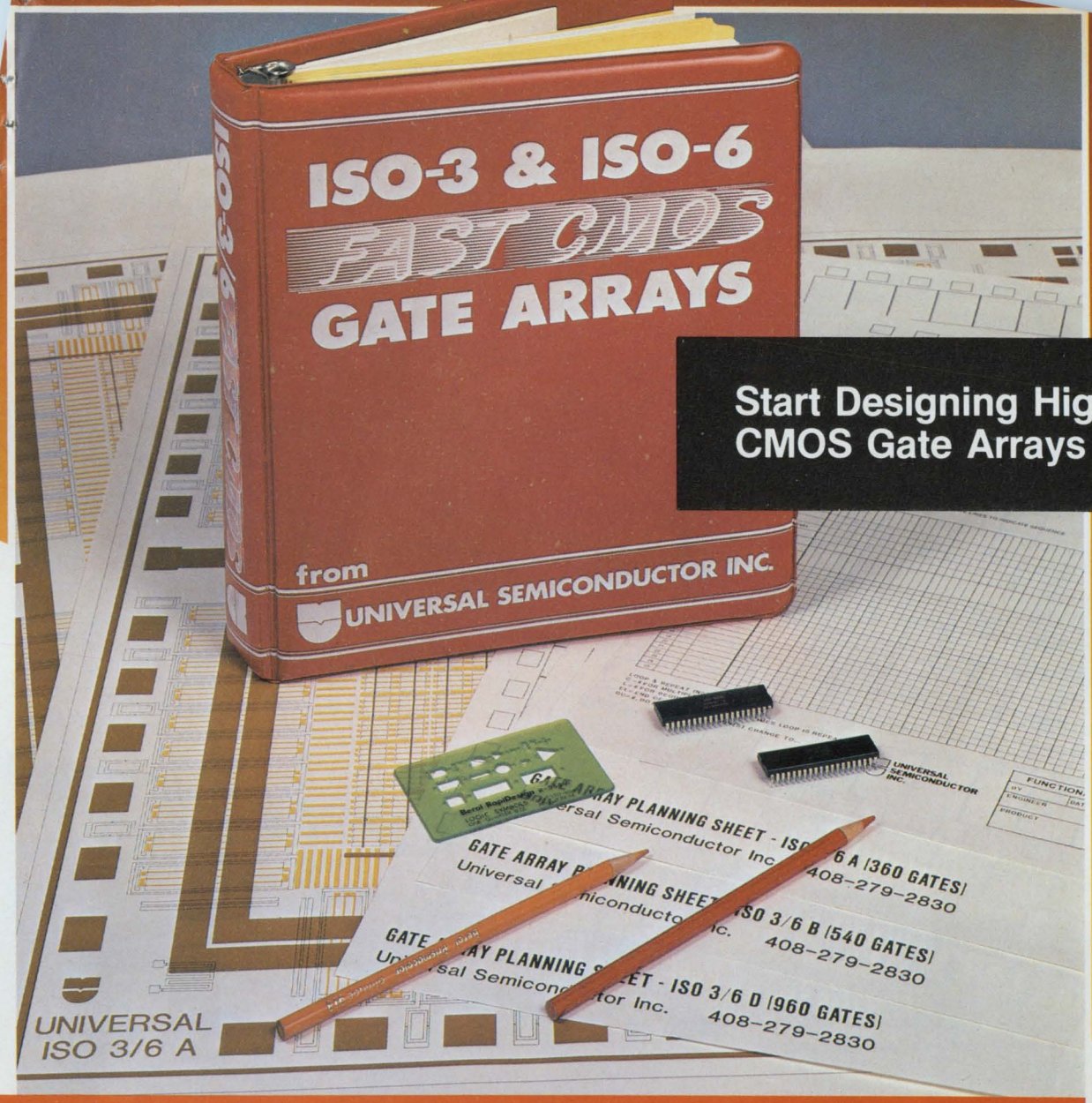
INCOMM consists of two programs. XFR operates on PDP-11 systems under either RT-11 or RSX-11, while PDPCOM operates on the MDS 800 series II or III systems under ISIS-11. XFR is delivered in object format on diskette, RK05 disk pack or 9-track 800 bpi magnetic tape. PDPCOM is delivered on either single or double density diskette media.

Another package, recently announced by Nicolet Scientific, Northvale, NJ, is a cross-assembler/loader for the Motorola 68000 designed to run on the Data General Eclipse. The package, that has already been used in the development of the Nicolet product line, is available on 9-track 800 bpi magnetic tape.

As the conventional mini and mainframe houses are now offering devices to the market, the IC houses are building devices with the comparative power of existing minis and mainframes. One of the latest and most powerful devices is the NS16032 μP from National Semiconductor. Since the company launched their new 16-bit range, they have introduced a range of software support packages to back it up.

Latest of the bunch is the ISE/16, an in circuit emulator that complements the software development and debug tools. ISE/16 has been designed to interface to a variety of software development hosts; it is provided with two RS232C serial ports and an IEEE-488 interface.

When used with most standard host computers, interfacing is



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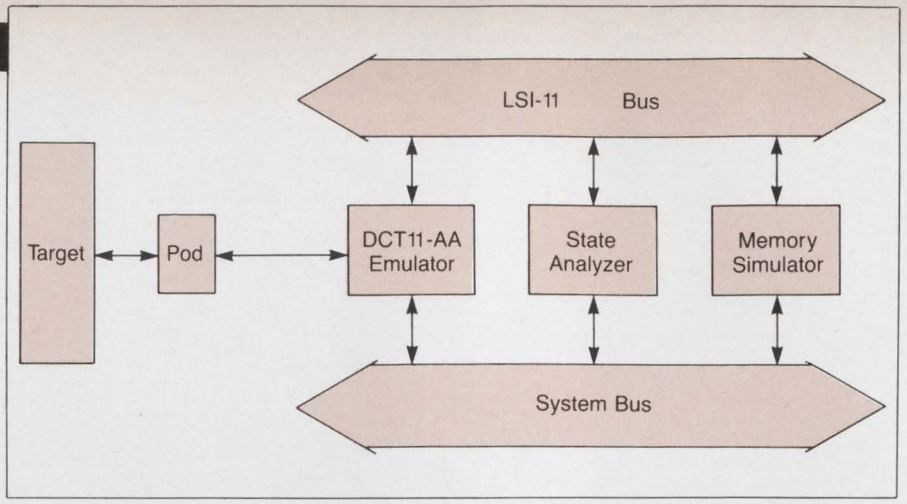

Figure 4: Supporting DEC's entry into the μP world, the MDE/T-11 will run up help menus to aid the user.

achieved via the RS232C ports. Two configurations are possible. In the case of a host with an integral terminal, the typical configuration is via one RS232C port to a serial port on the host. In the case of a host with a remote terminal, the typical configuration is that of one port connected to the terminal and the other to the host. In this configuration, ISE/16 can become transparent under software control so that host-terminal communication may be achieved.

ISE/16 consists of three parts: the emulation support unit, the emulation pod and the external status pod. The emulation support unit houses the interface logic, the trace memory, emulation memory and breakpoint logic. The emulation pod unit, which connects to the support unit over a 4′ twisted-pair cable, contains the NS16032 processor (CPU), the NS16201 timing control unit (TCU), an optional NS16082 memory management unit (MMU), EPROM-based code for ISE control, mapping logic and buffering. The emulation pod connects to the target via 12″ twisted-pair cables that plug into the sockets for the CPU, TCU and MMU (optionally). The external status pod provides eight independent channels that can be used as events to trigger the breakpoint and trace logic.

Currently, ISE/16 is designed to operate with two specific hosts: National's STARPLEX II running the STARPLEX II operating system and Digital Equipment's VAX 11 series running the VMS operating system.

All In One

Some companies are now providing development tools that combine software development, emulation and analysis in an interactive sys-

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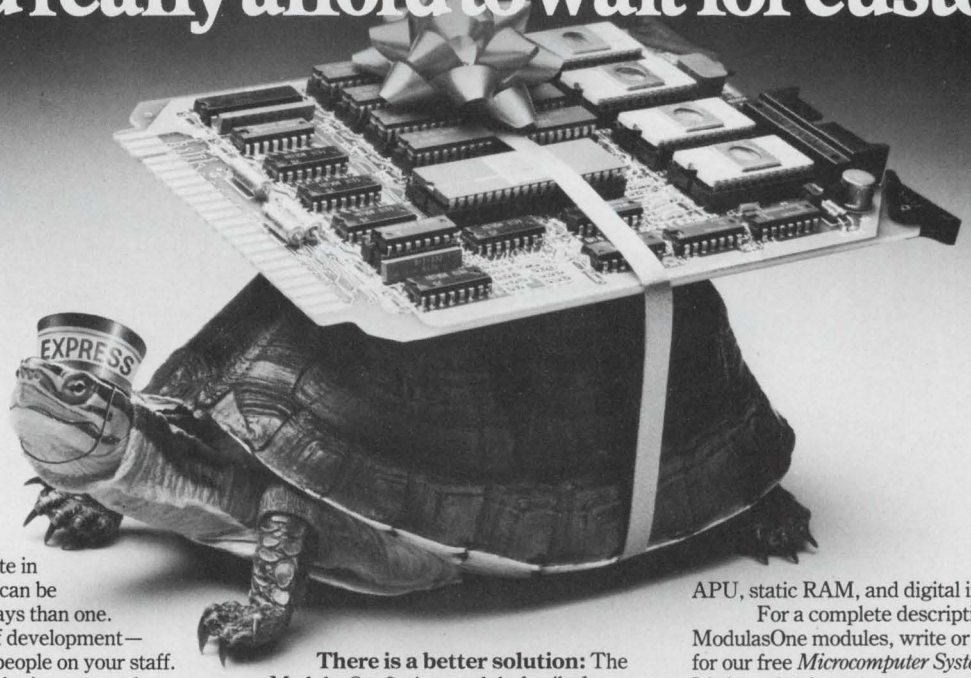

Going the 'custom' route in micro system design can be expensive in more ways than one. First, there's the high cost of development—whether done outside or by people on your staff.

Then there's the loss in time-to-market for your product. By the time you get the first production unit in your hand, what you thought was a 'red hot' feature may not be so hot anymore. And while you're waiting for delivery of your prototype boards, your competition, insensitive as it may seem, will be slowly chipping away at your market share.

There is a better solution: The ModulasOne® micromodule family from Adaptive Science Corporation. This is a *comprehensive* set of microcomputer cards... all 4½" by 6½", all One-Bus compatible, and all off-the-shelf. So you can build your system without those high development costs and without delay. Choose from a menu of 28 pc cards including 16-bit address MPUs, APU, static RAM, and digital interfaces etc..

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	12	180	180	—	—	120
	12.5	—	—	150	150	—
	13.3	200	200	—	—	—
	15	—	—	180	180	150
	16.4	—	—	200	200	164
Enhanced	10	—	—	—	—	100
Expanded Print (Double Width)		Yes	Yes	Yes	Yes	Yes
Dot Addressable Graphics (Dot/In., H/V)		60/72	60/72	75/72	75/72	72/72
Max. Line Width (In.)		8.0	13.2	8.0	13.2	13.2
Audible Alarm		Opt.	Opt.	Opt.	Opt.	Yes
Out-of-Paper Sense		Yes	Yes	Yes	Yes	Yes
Ribbon, Continuous Loop Cartridge (Yds)		30	30	30	30	30
Interfacing: Parallel Cent. Comp.		Yes	Yes	Yes	Yes	Yes
RS-232-C Serial		Yes	Yes	Yes	Yes	Yes

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tem. Such a system is the Hewlett-Packard HP64000, a product that the company has dubbed the Logic Development System. The stations accept a number of plug-in boards that may be configured by the user for his own particular application (**Figure 3**).

For a software development or emulation station the user selects the appropriate hardware and software options. Having once configured a system, it can be reconfigured for another function as the need arises. For team efforts, the stations may be configured into a distributed processing system. Each station has a dedicated 16-bit processor; up to six stations can be combined on a single disk.

The multistation system allows one designer to perform emulation at one station while a programmer debugs software at another. A third user could be optimizing performance using real-time, non-intrusive software analysis. For the user with a large investment in another development system, minicomputers or a time sharing system, an RS232C interface and terminal mode software are provided so that HP's system can be added on. The user can retain his in-house development procedures and then download to the HP system for debugging, testing and PROM programming.

As the project develops to the hardware/integration phase, the same station may be used for non-intrusive hardware and software analysis to test, debug and optimize performance under real-time operating conditions.

Supporting the T-11 μP, Digital Equipment Corp. has also adopted the approach of offering a very user-friendly development system (the MDE/T-11) that can provide the necessary hardware components for real-time application development: the DCT11-AA emulator, the memory simulator, and the state analyzer (**Figure 4**).

Communication between the three hardware components is accomplished in real-time by the system bus, which is a high-speed bus integral to the MDE/T-11 backplane. Major development system components include a VAX/VMS host system, MDE/T-11 system hardware, and the target hardware in which the DCT11-AA μP and software are installed. The VAX/VMS host system provides the environment in which application programs are written, edited, assembled and linked. During these stages of DCT11-AA software development, no system hardware is involved except the console terminal and the LSI-11 system hardware operating as a virtual terminal connected to the host system. The host provides all file access for

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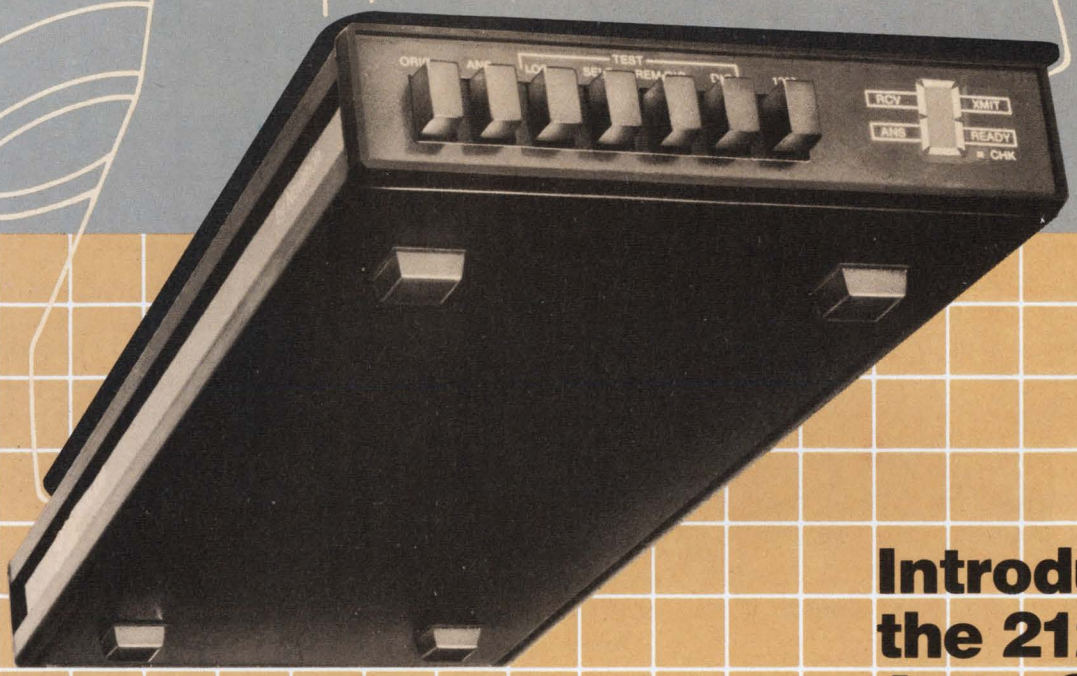

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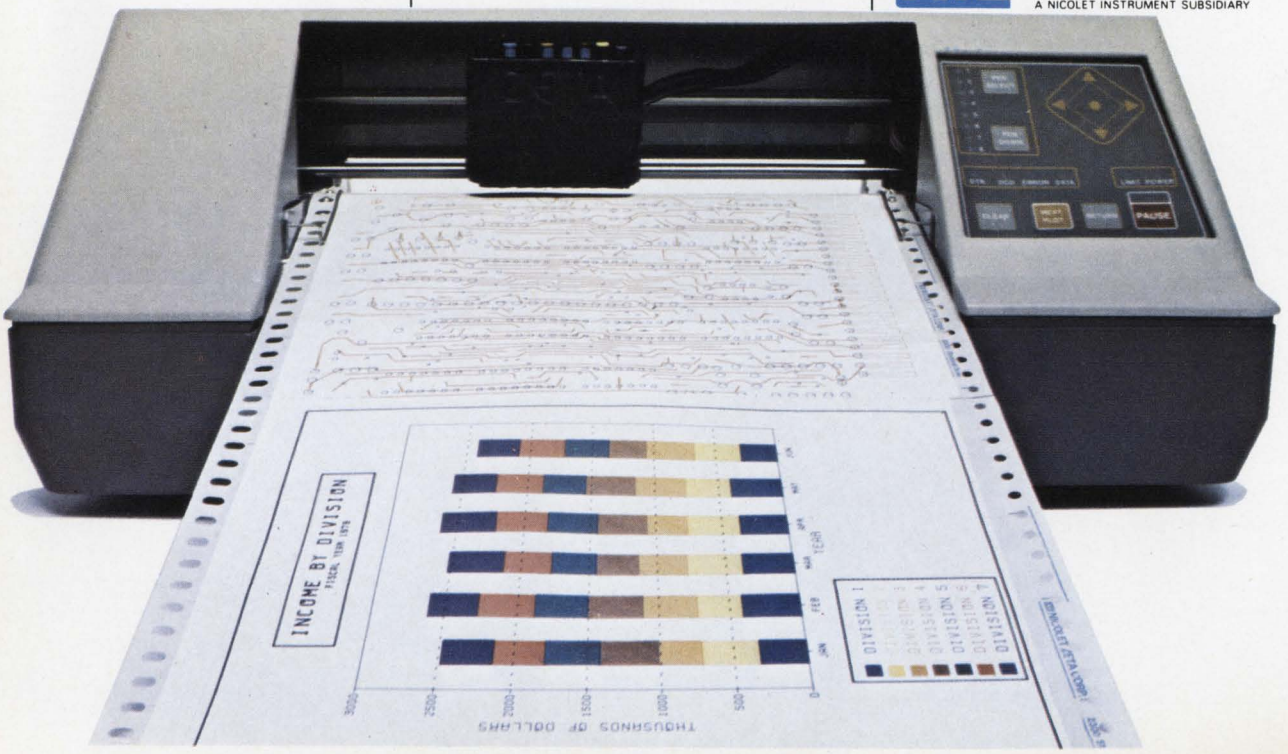

MDE/T-11 software and application programs.

Team Effort

Supporting up to eight workstations for the team development effort, Tektronix's 8560 Multi-User Software Development Unit has at its heart a minicomputer that runs under the TNIX Operating System, a derivation of Bell Labs UNIX Version 7.

The 8560 includes a range of software design tools that includes assemblers and compilers for both 8-bit and 16-bit devices, loader/linkers to combine object files into executable object codes and two types of editors including a screen oriented version, and a text processing package.

Pascal computers with features such as structured constants, bit manipulation and re-entrant code were recently also made available.

Ethernet Too

It was almost inevitable that a company with experience in both Ethernet and development systems would not fail to realize the implications of bringing the two together to produce a system that would permit existing development stations to become networks stations.

To shorten development time (which may be particularly long in 16-bit environments) several tasks must be handled concurrently, such as compilation and source code editing.

Intel's new NDS II system (**Digital Design** April, p. 94) may be connected to up to eight Intellec development stations to upgrade the systems for use as NDS II resources via the NDS II communication board set. The two board set plugs into the Multibus chassis and provides the physical and data-link network requirements.

The Future

The choice of a development system rests to a great extent on present board level design decisions and future product plans a company is involved with. As the semiconductor companies produce more complex devices, their own development stations may be the only tools immediately available for the designer to handle his software development.

As the role of distributed processing becomes more evident, particularly so in the area of graphics systems design, the designer will need tools to handle more than one μP; already some systems are available (such as the Emulogic product). Systems must become more user friendly with interactive display and help menus to aid the user and to cut down development time. □

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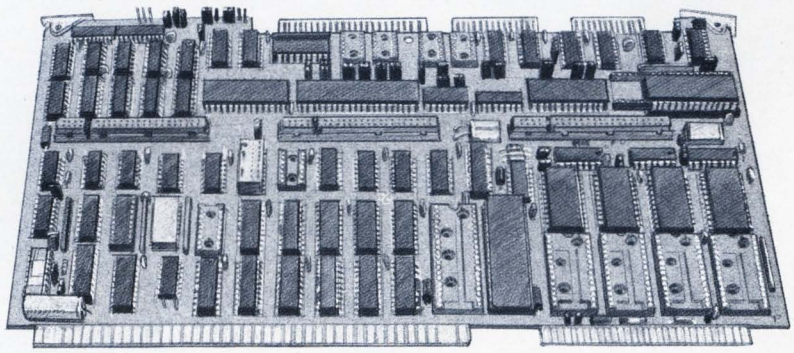

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The ZX-86 is an 8086 based single board computer which is fully software transparent to code written for the Intel *SBC-86/05. The ZX-86 offers additional features not found on the Intel boards including an on-board socket for an 8087 numeric data processor, three SBX connectors and two serial ports. The ZX-86 can be ordered with 5, 8, or 10 MHz Processors thus providing higher performance, expandable and flexible solution for OEM applications.

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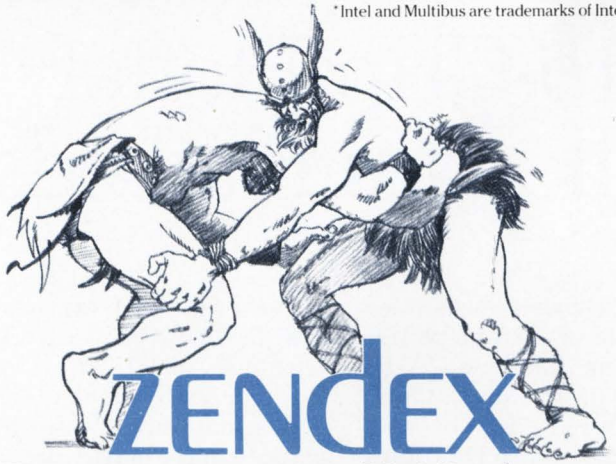

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HP's micro-grip paper handling gives their new plotters the speed and resolution of flatbeds, but at lower cost and compact size.

Micro-Grip Plotter Challenges Flatbeds

In mid-July, Hewlett-Packard expanded its line of drafting plotters by introducing the model HP 7585A for industry standards E/AO size drawings 36.5″ by 46.8″ (927 by 1189 mm). Designed around HP's micro-grip drive technology, the new plotter features μP control, high resolution, high repeatability, 4g acceleration and speeds up to 24″ per second. It can also turn out drawings as small as 8″ by 10.5″. Priced at $22,750, the plotter should offer some serious competition to large flatbed plotters, not only in price but in high speed and compact size.

New Drive System

In the past, conventional plotters have been based on either heavy moving arms to transport the pen, or drums and belts to transport the paper. To avoid the high inertia intrinsic to these designs, HP designers developed the micro-grip drive.

Micro-grip is based on the principle of moving the drawing medium in one direction (the X-axis), while the drawing pen travels in the second direction (the Y-axis). This by itself is nothing new, since the earliest chart recorders also were based on this principle, but they required sprocket holes and mechanisms to drive the paper.

HP's micro-grip plotter transports the drawing medium, rather than attempt to move the underlying platen or bed upon which the drawing medium rests (which is how drum and belt-drive plotters operated). Micro-grip moves a single sheet of the drawing medium only.

Because a micro-grip-based plotter such as the HP 7585A must overcome only the mass of a single sheet of paper, it has better control, faster speed, and higher acceleration. What this means is that less power is required to produce a plot, and fewer control problems are encountered in dealing with inertia and momentum.

The micro-grip drive consists of a series of rotating metal grip wheels underneath the gull-shaped plotter bed, two of which secure each side of the drawing medium firmly against a hard-rubber pinch wheel when the plotter is instructed to hold the plot.

The surface of the grit wheel itself is coated with a layer of aluminum oxide containing the microsharp edges of grit particles. These

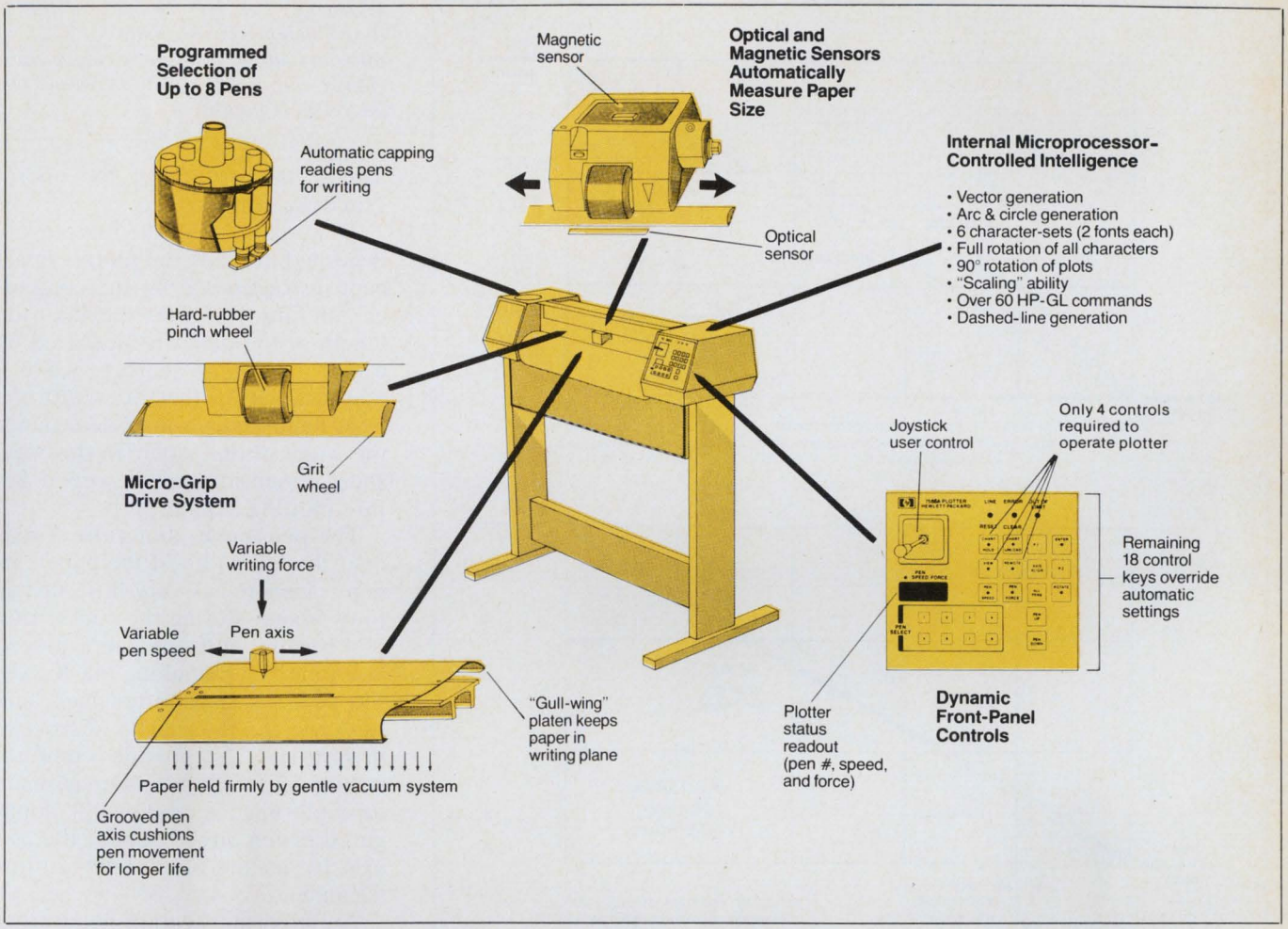

Figure 1: In addition to micro-grip drive, the HP 7585A drafting plotter features internal μP control, optical and magnetic sensors for paper measurement, and programmed pen selection.

particles indent the surface of the plotting paper at thousands of points along the edges as the paper is first passed through the plotter.

Each time the paper makes a pass through the plotter, thousands of microscopic indentations, unseen by the naked eye, realign themselves with the same grit particles that created them. In this way, regardless of how many times the plotting medium passes through the plotter, a micro-grip registration pattern ensures excellent repeatability and graphic quality.

Simplified Plotting

The graphics-performance capabilities of the HP 7585A enable it to perform complex plots with a minimum of programming. To draw a vector, one need define only the end-points, and the plotter automatically joins them with a line. Circles and arcs are drawn by merely inputting the radius and starting position.

To distinguish between different plot data, a user can specify up to seven different internally stored line types: solid, dotted, dashed, and combinations of dot and dash. The plotter's μP automatically scales each line pattern between vector end-points to provide uniform line-style appearance and output quality.

To label a finished plot, a user may choose from six resident character sets (English, French, German, Spanish, Scandinavian and special symbols) in either of two different font styles—stick-figure or a Leroy-like, arc-based font. Text can be tailored to a particular plot by defining character size, slant, spacing and direction.

Pens are selected individually under program control from an 8-pen carousel and then returned and capped automatically after each use. A pen carousel can hold up to eight pens of varying colors and line widths. The drawing medium used on the HP 7585A can be paper, vellum or polyester film. To accommodate differences in plotting media, a user may select from an assortment of pen types: fiber-tip, liquid-ink or rollerball. Pen force and velocity are set automatically for each pen type.

The plotter readily accommodates industry media sizes from E/AO to A/A4. μP-controlled, edge-sensing system automatically sets plot limits to allow scaling of plot data to fit the sheet exactly.

Easy Interface

Offering industry-standard interfaces and communications protocols, the HP 7585A operates with

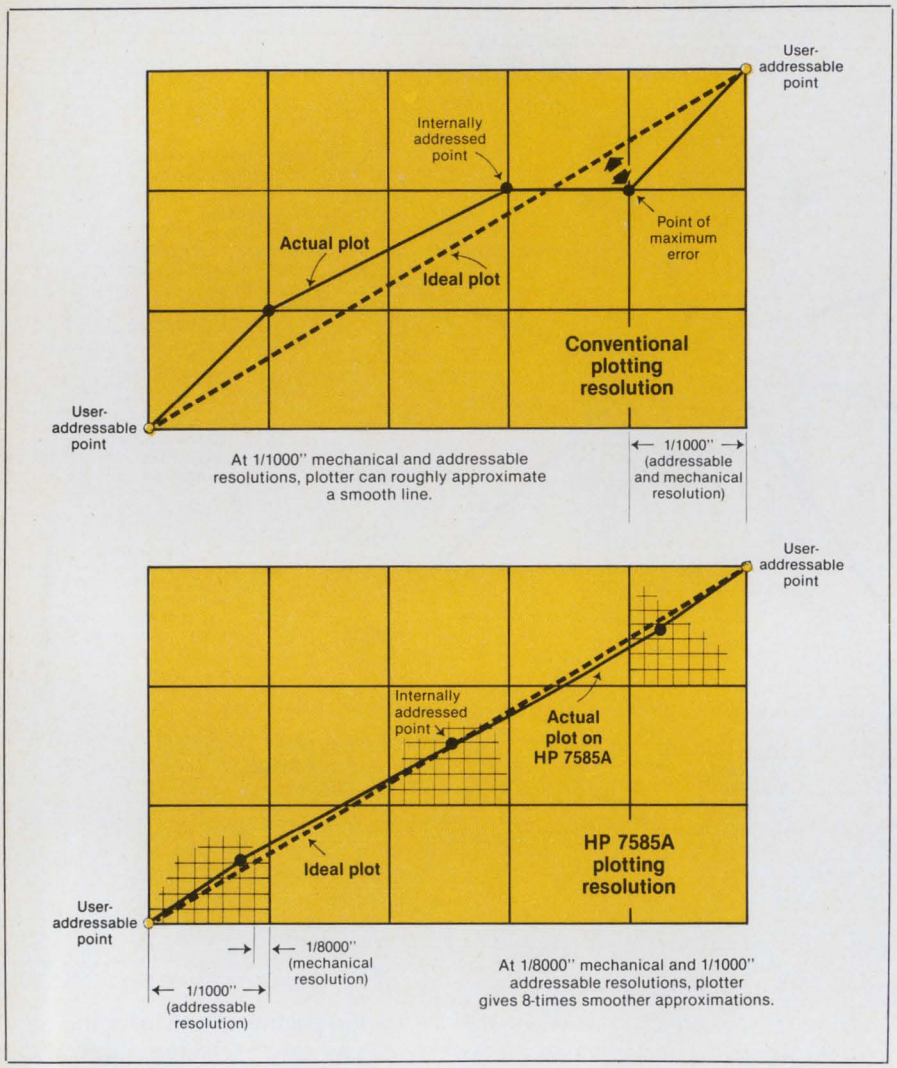

Figure 2: The HP 7585A's ability to draw increments as small as $^1/_{8000}$" (3 microns) allows it to approximate more closely the ideal path between two addressable points.

HP or non-HP personal computers, desktop computers, minicomputers, mainframes and graphics-terminal systems. Support for most existing plotter software is provided through HP's industry-standard plotting package. Communications with the HP 7585A are achieved through either an HP-IB (IEEE 488) or RS-232-C/CCITT V.24 interface.

High Resolution

The HP 7585A has an addressable resolution of 0.001" (0.025 mm), a mechanical resolution of 0.00012" (0.003 mm), and a repeatability of 0.002" (0.05 mm).

This can be understood by comparison with other plotters. For example, one with both an addressable and a mechanical resolution of $^1/_{1000}$" (0.025mm) will plot lines that can appear jagged, especially in diagonal directions (**Figure 2**). The HP 7585A on the other hand, although addressable to $^1/_{1000}$" (25 microns), has the ability to draw increments as small as $^1/_{8000}$" (3 microns). This means it can approximate more closely the ideal path between two addressable points, resulting in plots that are smoother to the eye.

The HP 7585A uses single sheets of plotting media. When loading the plotter, the user slides the paper between the platen and Y-axis carriage, positions it against two left-hand stops, slides the right-hand pinch wheel over the right edge of the paper and presses the chart-hold key. With this instruction, the plotter lowers the two rubber pinch wheels, one on each edge, to hold the paper firmly against the surface of the micro-grip drive wheels.

To initiate a plot, the remote key is pushed to ready the plotter to accept instructions from the computer. Before the plot begins, the length of the paper is measured by a pair of optical sensors, while a magnetic sensor that rides with the right-hand pinch wheel determines the width of the paper. In this way, sheet dimensions are recorded before plotting begins.

The pen moves along the Y-axis over the full width of the paper; its pen transport has very little inertia to overcome during the course of a plot because only one pen is moved at a time. To plot along the X-axis, the paper is transported back and forth via the low-inertia micro-grip drive wheels. To provide a uniform writing surface, the paper is made to conform to a "gull-wing" configured platen directly under the pen axis by means of a slight airflow vacuum.

An important feature believed to be exclusive to the HP 7585A is that its speed and acceleration are controlled by the μP independent of writing direction. The plotter can be set to a maximum speed for a given drawing surface and pen type and will not exceed that speed even when drawing diagonal lines. Plotters without this feature require program "work arounds" to maintain uniform speed and plot quality. For optimum throughput, pen-up movements always are conducted at maximum speed.

Competing with plotters selling for $15,000 to $20,000 more, the HP 7585A is expected to fill a definite need for a low-cost, high-resolution plotter. It appears to be suited to many CAD/CAM systems for mechanical and electrical/electronic industries. The price should also make it useful for architectural and civil engineering applications as well as mapping where the larger size drawings are most important. □

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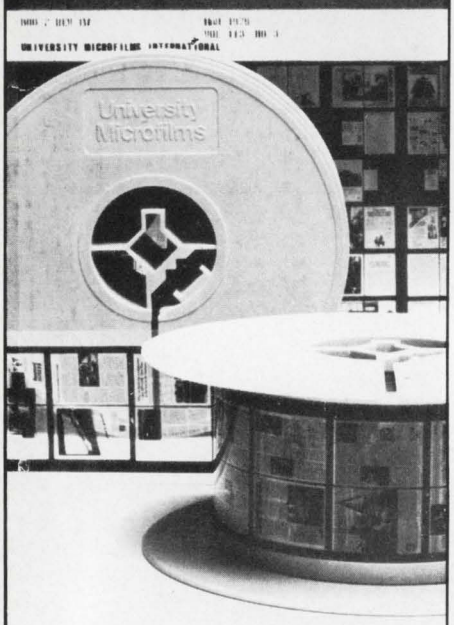

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	Page #	Write #
Add-In/Add-On Memory		
Plessey Peripheral Systems	13	12
Communications		
Bo-Sherrel	28	38
Novation	41	6
Digilog	81	207
Digital Communications Associates, Inc.	81	208
General Dynamics Communications	79	145
Neff Instrument Corp.	77	133
Components, Hardware, Packaging		
Electronic Solutions	59	32
Hettinga	17	37
MDB	9	3
Chicago Switch	77	128
Epson America	77	129
Licon	77	132
Oak Switch Systems Inc.	77	134
Computer I/O		
GR Electronics	78	49
Mouse House	28	36
Addmaster Corp.	80	205
Cybernetic Micro Systems Inc.	82	174
Computers/Systems		
Adaptive Science	38	26
Dataram	29	22
Design Aids	11	7
Distributed Computer Systems	31	39
dy-4 Systems	58	46
Florida Computer Graphics	2,3	5
Micro Link	35	30
Numerix	15	17
Zendex	43	48
Quay Corp.	78	149
Controllers, Interfaces		
D.W. Digital	80	40
Hard Copy		
Anadex	39	15
Calcomp	4	13
Eaton	16	11
Hecon	8	27
Memodyne	30	28
Nicolet Zeta	42	16
Printer Products	79	33
Mass Memory		
Exatron	17	35
Kennedy	C2	1
Moya	78	41
Qantex	7	29
Fourth Dimension Systems	81	209
Innovative Data Technology	80	191
Olivetti, OPE	80	212
Rosscomp Corp.	80	194
Western Dynex Corp.	80	204
Power Supplies, UPS, Line Conditioners		
Controlled Power	C3	2
Panel Components	78	42
Gould Inc.	82	178
Power/Mate Corp.	77	135
Semiconductors, ICs, μPs		
International Micro Inc	63	19
Universal Semiconductor	37	8
Software		
Applied Analytics	21	24
Musys	57	31
Computing!	78	141
Signal Technology Inc.	79	151
Test, Instrumentation, Development		
American Automation	40	10
Dolch Logic Instruments	4C	4, 14
Hilevel Technology, Inc.	33	9
Wintek	82	43
International Microsystems	77	131
Interstate Electronics	77	130
Weston Instruments	77	138
Video Display/ Image Processing		
AED	1	20
Audiotronics	19	25
Datacube	10	21
Modgraph	6	23

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Designers' Guide To The IEEE-696 Bus

Once a hobbyist bus, the S-100 has matured into the IEEE-696 standard.

by Paul Snigier,
Contributing Editor

In late 1979, the S-100 bus (now IEEE-696), supported by undercapitalized cottage businesses selling to the cost-conscious hobbyist market, was the most popular bus around, but also one with a bleak future. Industry prognosticators predicted a gradual decline of the S-100. But, in late 1980, the bus entered a period of unexpected growth that saw some firms reporting a fourfold growth in S-100 compatible products. In this article, we will examine the reasons for this rapid growth, the bus' future and its engineering design aspects. To understand the present situation, it is necessary to understand the bus' history.

An Unexpected Standard

Never intended to be a standard, the S-100 bus grew into an overnight *de facto* standard within the early hobby microcomputer field. The S-100 succeeded because it filled a vacuum in a specific period of time. Ed Roberts, president of MITS, introduced the S-100 bus in early 1975 on the 8080-based Altair. IMSAI and Cromemco adopted the S-100, as did other hobbyist firms, with the notable exception of Commodore's PET (which interfaced over the GPIB). Being the first major bus on the block, S-100 was certain to have problems.

The S-100 was designed with no expectation of the enormous success that the bus accomplished. MITS provided no formal description of signal levels and timing, letting Intel's 8080 specs handle the signal definition. Pinouts were left unassigned, allowing other firms to customize the bus. Most S-100 compatible cards, peripherals and computers were anything but, and in the resulting confusion and blame throwing, the S-100 quickly created ill will.

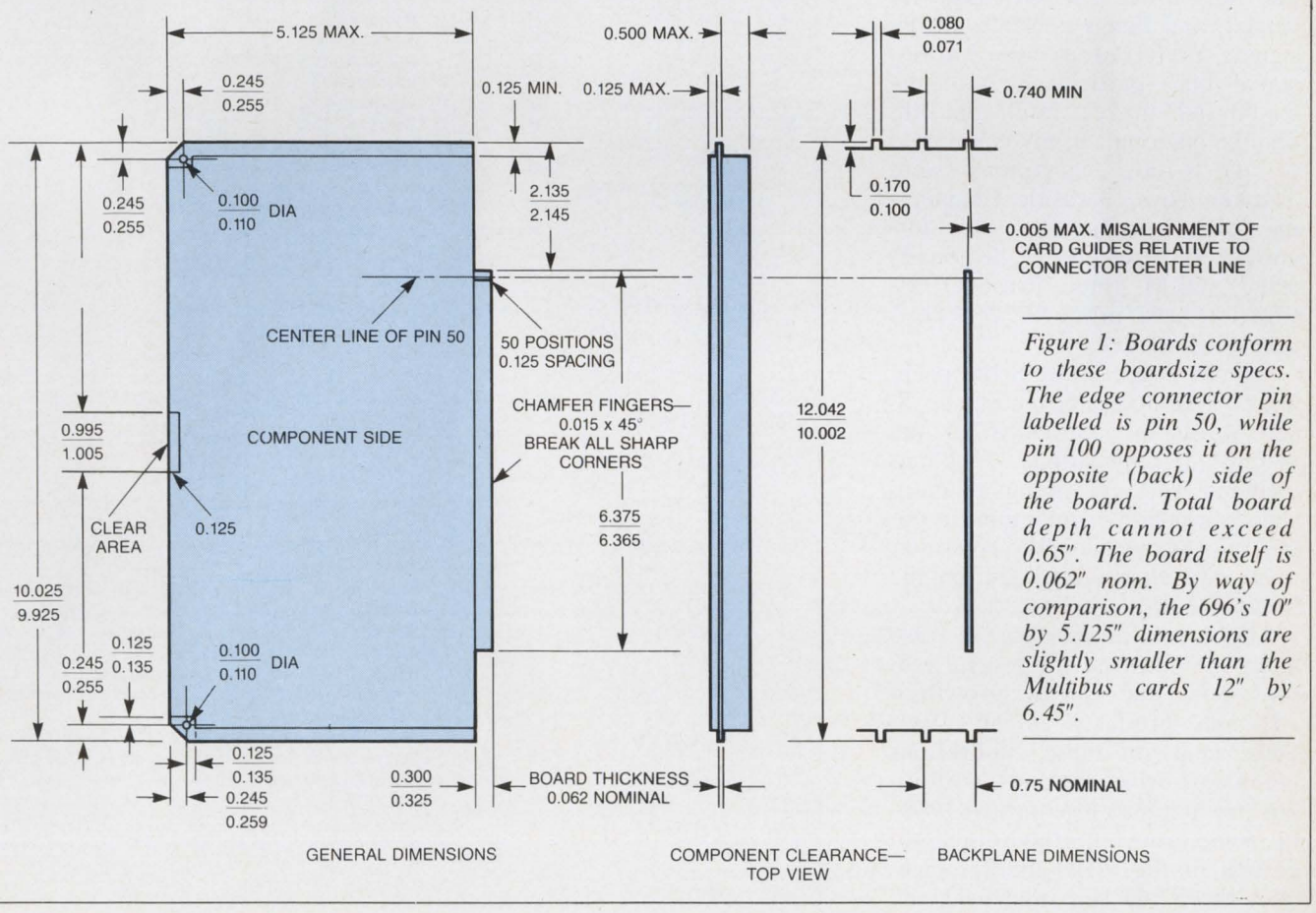


Figure 1: Boards conform to these boardsize specs. The edge connector pin labelled is pin 50, while pin 100 opposes it on the opposite (back) side of the board. Total board depth cannot exceed 0.65". The board itself is 0.062" nom. By way of comparison, the 696's 10" by 5.125" dimensions are slightly smaller than the Multibus cards 12" by 6.45".

Figure 2: The 696's eight signal lines carry all information or messages. These include eight signal lines: 16 or 24 address; 16 data; 8 status, 5 output, and 6 input control; 8 direct memory access (DMA) control; 8 vectored-interrupt; and 20 utility lines. Their pin numbers, signals/types, active levels and descriptions are as listed here.

PIN NO.	SIGNAL & TYPE	ACTIVE LEVEL	DESCRIPTION
	+8V (B)	1	Instantaneous minimum greater than 7V, instantaneous maximum less than 25V, average maximum less than 11V.
2	+16V (B)		Instantaneous minimum greater than 14.5V, instantaneous maximum less than 35V, average maximum less than 21.5V.
3	XRDY (S)	H	One of two ready inputs to the current bus master. The bus is ready when both these ready inputs are true. (See pin 72.)
4	VIO* (S)	LO C	Vectored interrupt line 0.
5	VI1* (S)	LO C	Vectored interrupt line 1.
6	VI2* (S)	LO C	Vectored interrupt line 2.
7	VI3* (S)	LO C	Vectored interrupt line 3.
8	VI4* (S)	LO C	Vectored interrupt line 4.
9	VI5* (S)	LO C	Vectored interrupt line 5.
10	VI6* (S)	LO C	Vectored interrupt line 6.
11	VI7* (S)	LO C	Vectored interrupt line 7.
12	NMI* (S)	LO C	Nonmaskable interrupt.
13	PWRFAIL*(B)	L	Power-fail bus signal.
14	DMA3* (M)	LO C	Temporary-master priority bit 3.
15	A18 (M)	H	Extended address bit 18.
16	A16 (M)	H	Extended address bit 16.
17	A17 (M)	H	Extended address bit 17.
18	SDSB* (M)	LO C	The control signal to disable 8 status signals.
19	CDSB* (M)	LO C	The control signal to disable 5 control output signals.
20	GND (B)		Common with pin 100
21	NDEF		Not to be defined. Manufacturer must specify any use in detail.
22	ADSB* (M)	LO C	The control signal to disable the 16 address signals.
23	DODSB* (M)	LO C	The control signal to disable the eight data-output signals.
24	ϕ (B)	H	The master timing signal for the bus.
25	pSTVAL* (M)	L	Status-valid strobe.
26	pHLDA (M)	H	A control signal used in conjunction with HOLD* to coordinate bus-master transfer operations.
27	RFU		Reserved for future use.
28	RFU		Reserved for future use.
29	A5 (M)	H	Address bit 5.
30	A4 (M)	H	Address bit 4.
31	A3 (M)	H	Address bit 3.
32	A15 (M)	H	Address bit 15 (most significant for nonextended addressing).
33	A12 (M)	H	Address bit 12.
34	A9 (M)	H	Address bit 9.
35	DO1 (M)DATA1 (MS)	H	Data-out bit 1, bidirectional data bit 1.
36	DO0 (M)/DATA0 (M/S)	H	Data-out bit 0, bidirectional data bit 0.
37	A10 (M)	H	Address bit 10.
38	DO4 (M)/DATA4 (M/S)	H	Data-out bit 4, bidirectional data bit 4.
39	DO5 (M)DATA5 (M/S)	H	Data-out bit 5, bidirectional data bit 5.
40	DO6 (M)/DATA6 (M/S)	H	Data-out bit 6, bidirectional data bit 6.
41	DI2 (S)/DATA10 (M/S)	H	Data-in bit 2, bidirectional data bit 10.
42	DI3 (S)DATA11 (M/S)	H	Data-in bit 3, bidirectional data bit 11.
43	D17 (S)/DATA15 (M/S)	H	Data-in bit 7, bidirectional data bit 15.
44	sM1 (M)	H	The status signal indicating that the current cycle is an opcode fetch.
45	sOUT (M)	H	The status signal identifying the data-transfer bus cycle to an output device.
46	sINP (M)	H	The status signal identifying the data-transfer bus cycle from an input device.
47	sMEMR (M)	H	The status signal identifying bus cycles that transfer data from memory to a bus master, which are not interrupt-acknowledge instruction-fetch cycles.
48	sHLTA (M)	H	The status signal that acknowledges execution of a HLT instruction.
49	CLOCK(B)		2-MHz (0.5%) 40 to 60% duty cycle. Needn't be synchronous with any other bus signal.
50	GND (B)		Common with pin 100.
51	+8V (B)		Common with pin 1. .
52	−16V (B)		Instantaneous maximum less than −14.5V, instantaneous minimum greater than −35V, average minimum greater than −21.5V. Common with pin 100

By 1980 it looked like a showdown between Intel's Multibus and the S-100. It didn't look good for the S-100. Major board makers had adopted Multibus. Few large firms backed the S-100 and many of the minor firms that used the S-100 had cash flow problems due to poor management skills that saw them underpricing products. As for the IC manufacturers, not one had adopted the S-100. There were good reasons. Multibus (designed for the now-ancient Intellec line) offered more although it was expensive. It was designed for an industrial market, whereas the S-100 was targeted for hobbyists. At first the hobbyist market grew explosively, while the industrial market did not. Once the situation reversed, and things normalized, designers preferred a more professional bus (particularly with the leading μP maker, Intel, and others like National firmly committed to it). S-100's champions were Thinker Toys, Parasitic Engineering, SLAC, and lesser, now forgotten and bankrupt "lemonade stand" OEM firms. These OEMs sold low cost products to a cost-conscious market.

As μP usage grew, S-100 problems (once tolerated) cost the S-100 a loss in acceptance for the higher-end applications. Problems included varying timing relationships, poor line termination, multiple returns, bus length, crosstalk, noise and unregulated DC on the backplane.

The S-100 renaissance in 1980 and 1981 occurred for several reasons. First, the explosive growth of μP-based products had an effect. Since many of these applications are in cost-driven markets, a Multibus product may lose out. In 1980–81, some firms reported a threefold growth in the S-100 market. Second, the S-100 had (and has) one

PIN NO.	SIGNAL & TYPE	ACTIVE LEVEL	DESCRIPTION
53	GND (B)		
54	SLAVE CLR* (B)	LO C	A reset signal to reset bus slaves. Must be active with POC* and can also be generated by external means.
55	DMAO* (M)	LO C	Temporary-master priority bit 0.
56	DMA1* (M)	LO C	Temporary-master priority bit 1.
57	DMA2* (M)	LO C	Temporary-master priority bit 2.
58	sXTRO* (M)	L	The status signal that requests 16-bit slaves to assert SIXTN*
59	A19 (M)	H	Extended-address bit 19.
60	SIXTN* (S)	LO C	The signal generated by 16-bit slaves in response to the 16-bit request signal sXTRO*.
61	A20 (M)	H	Extended-address bit 20.
62	A21 (M)	H	Extended-address bit 21.
63	A22 (M)	H	Extended-address bit 22.
64	A23 (M)	H	Extended address bit 23.
65	NDEF		Not to be defined.
66	NDEF		Not to be defined
67	PHANTOM* (M/S)	LO C	A bus signal that disables normal slave devices and enables phantom slaves—primarily used for bootstrapping systems without hardware front panels.
68	MWRT (B)	H	pWR*-sOUT (logic equation). This signal must follow pWR* by not more than 30 nsec.
69	RFU		Reserved for future use.
70	GND (B)		Common with pin 100.
71	RFU		Reserved for future use.
72	RDY (S)	HOC	See comments for pin 3.
73	INT* (S)	LO C	The primary interrupt-request bus signal.
74	HOLD* (M)	LO C	The control signal used in conjunction with pHLDA to coordinate bus-master transfer operations
75	RESET* (B)	LO C	The reset signal to reset bus-master devices. It must be active with POC* and can also be generated externally.
76	pSYNC (M)	H	The control signal identifying BS_1.
77	pWR* (M)	L	The control signal signifying the presence of valid data on DO bus or data bus.
78	pDBIN (M)	H	The control signal that requests data on the DI bus or data or data bus from the currently addressed slave.
79	A0 (M)	H	Address bit 0 (least significant).
80	A1 (M)	H	Address bit 1.
81	A2 (M)	H	Address bit 2.
82	A6 (M)	H	Address bit 6.
83	A7 (M)	H	Address bit 7.
84	A8 (M)	H	Address bit 8.
85	A13 (M)	H	Address bit 13.
86	A14 (M)	H	Address bit 14.
87	A11 (M)	H	Address bit 11.
88	DO2 (M)/DATA2 (M/S)	H	Data-out bit 2, bidirectional data bit 2.
89	DO3 (M)/DATA3 (M/S)	H	Data-out bit 3, bidirectional data bit 3.
90	DO7 (M)/DATA7 (M/S)	H	Data-out bit 7, bidirectional data bit 7.
91	DI4 (S)/DATA12 (M/S)	H	Data-in bit 4 and bidirectional data bit 12.
92	DI5 (S)/DATA13 (M/S)	H	Data-in bit 5 and bidirectional data bit 13.
93	DI6 (S)/DATA14 (M/S)	H	Data-in bit 6 and bidirectional data bit 14.
94	DI1 (S)/DATA 9 (M/S)	H	Data-in bit 1 and bidirectional data bit 9.
95	DI0 (S)/DATA8 (M/S)	H	Data-in bit 0 (least significant for 8-bit data) and bidirectional data bit 8.
96	sINTA (M)	H	The status signal identifying the bus input cycle(s) that can follow an accepted interrupt request presented on INT*
97	sWO* (M)	L	The status signal identifying a bus cycle that transfers data from a bus master to a slave.
98	ERROR* (S)	L OC	The bus-status signifying an error condition during current bus cycle.
99	POC* (B)	L	The power-on clear signal for all bus devices; when it goes LOW, it must stay LOW for at least 10 msec.
100	GND (B)		System ground.

of the most widely installed computer system bases in existence. Over 120 firms provide S-100 compatible boards, and over thirty 8-bit and 16-bit CPU's of significance are available. Third, the new IEEE-696 Standard Committee's S-100 standard, introduced last year after two years of preparation, was delayed by changes, such as handling the 16-bit μP's and multiprocessing. Though delayed, it is finally having a strong positive impact. The standard also did not obsolete most pre-standard S-100 products. S-100 board makers are now offering boards that are jumper-compatible with existing pre-standard S-100 boards and systems. Due to this, OEMs feel safer using the S-100.

Indirect Competitors

The S-100 and Multibus are not direct competitors. Physically, the two boards are different in size: 10 × 5.55″ packed on 0.75″ centers or spacing for the S-100, and 12 × 6.75″ packed on 0.6″ centers for the Multibus.

The S-100 connector pin spacing is 0.125″; Multibus, 0.156″. The S-100 signals appear on one 100-pin dual readout card-edge connector; Multibus, 86 pins, plus an optional 60-pin auxiliary connector. Incompatibility extends to bus arbitration, power distribution and loading among other items. Only in the loosest sense of being targeted at many of the same applications are they competing. The choices between the two are easy to make, due to these differences.

Mechanical Specifications

At 10″ (W) × 5.3″(H) × 0.062″(T), the typical S-100 board connects to a so called "motherboard" (really a backplane) through an offset 100-pin edge connector, so that reverse board re-insertion is impossible. Pins 1–50 are on the component side, from left to right (looking towards the edge connector edgewise). It is offset to the left.

To reduce crosstalk and noise, ground traces are interleaved between signal traces. To eliminate ringing, signal lines have termina-

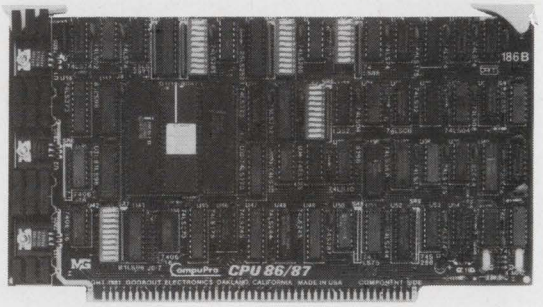
CPU Board Uses 8086/8087

An 8086/8087 μP board providing 16-bit capability with provisions for adding a mathematics co-processor and operating system firmware has been introduced by CompuPro, Oakland Airport, CA.

Compatible with IEEE 696/S-100 standards, CPU 86/87 is available in either 8- or 10-MHz μP versions. Accommodating 8- or 16-bit words, its on-board logic can read or write two bytes serially for 8-bit applications, or pass world-wide values for 16-bit operation. As a result, users can mix 8- and 16-bit devices in the same system.

In addition, CompuPro's new board accepts Intel's 8087 math processor and 80130 operating system firmware. The math processor offers a high-speed number crunching capability, while the firmware adds an 8-level vectored interrupt controller, three interval timers, and a choice of silicon-based operating systems: the iRMX-86 kernel or CP/M-86.

A clock-switching circuit permits slave processors to share a bus with the board, thereby eliminating bus conflicts by running the slave and the master at different clock rates.



Suggested retail price is $695 for the 8-MHz and $850 for the 10-MHz version. OEM pricing is available.

tion circuitry to keep the unconnected lines high, as well as to stop multiple reflections from improperly terminated lines (due to impedance mismatching). Board thickness is 0.062″ (nom.); component height clearance, 0.500″ (max.); and component clearance, 0.125″ (max). The edge connector is 6.375/6.365″ wide by 0.300/0.325″ deep. Pin 51 opposes pin 1 on the opposite, trace (solder) side of the board.

Unexpectedly successful, the S-100 bus is gaining still wider acceptance, thanks in part to standardization.

Eight 696 Signals Groups

As the GPIB/488 has talker and listener devices, (covered in the June and August issues) the S-100's equivalent is the bus masters and slaves. A permanent bus master, contained in all S-100 systems, provides key signals. A temporary bus master may request to take over the bus; if the permanent master grants control, this specific temporary bus master completes its task and passes control back. The transfer process is not simple, and there are a maximum of 16 temporary bus masters. Slaves (such as I/O interfaces, memory boards and so on) receive/transmit data from/to the master.

The eight bus signal groups include: 16 or 24 address lines, eight status lines, five output control lines, six input control lines, eight TMA (DMA) control lines, eight vectored-interrupt lines and 20 utility lines.

The address bus (A0-23) addresses memory and I/O devices. It is used to select a specific slave. With the pre-696 bus, directly addressable memory was 64 Kbytes, as only 16 address lines existed (A0-15). The 696 can address 16 Mbytes. Unlike pre-696 S-100, which addressed 256 I/O ports (A0-7), 696 address 64K ports (A0-15).

Only the current bus master addresses anything. A temporary master used A0-23; a permanent master A0-15.

The data bus operates in either of two modes: for 8- or 16-bit data transfers. If it is an 8-bit transfer, two unidirectional buses exist (DO0-7 and DI0-7) where DO/DI respectively signify data output and input, which is defined relative to the current master to slave data flow direction. The DO bus floats on the permanent master when line 23, DODSB or Data Out DiSaBle, is taken LOW.

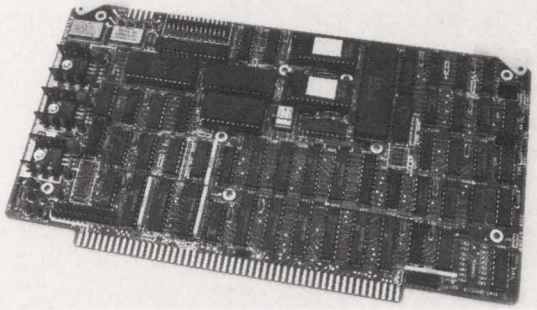
Mixing 16- and 8-bit data transfers in the same system is possible by control lines 58 and 60. Ganging the two buses permits bidirectional data flow, permitting the use of 16-bit μPs.

The status lines let all devices determine the bus state. These include memory read and writes, I/O, interrupt and halt acknowledges, data transfer request and op-code fetch.

The control output bus provides strobes, enabling timing control to initiate action such as: R/W strobing, beginning of bus cycle and halt acknowledge.

The control input bus, on the other hand, tells the master when to execute a task. In this way, the slaves can communicate to the master. If a slave can handle a 16-bit data transfer, it will use this (pin 60); and, if the temporary master wants the permanent master to relinquish bus control, it

10MHz 8086 and 256K RAM for S-100 Bus



Two of the latest introductions to the market from Piiceon, San Jose, CA, have been the PC86 series and the Superam 50B.

The PC86 series is an 8086-based, 16-bit CPU card with the CPU available in three speeds, 5 MHz, 8 MHz and 10 MHz.

The cards feature an 8253 interval timer with two uncommitted timer outputs, an 8259 interrupt controller that serves up to eleven interrupt signals, and an RS232C serial interface (110 to 19.2 Kbaud).

The cards are designed to provide additional expansion options by the use of an add-on Supermodule that plugs directly onto the PC86 board. Options available include use of the 8087 numeric data processor and a multimaster capability that allows the PC86 to operate as one of up to 16 bus masters, either as a permanent or temporary master sharing the S-100 bus.

The Superam 50-B is a 256 Kbyte dynamic RAM board with a board level access time of 175ns (max) over the 0–55°C temperature range. Operation with a 10MHz 8086-based CPU without wait states has been demonstrated. Extended addressing allows the Superam 50B to be placed at any 156 Kbyte boundary in a 16Mbyte address field. It may be configured for bank select addressing with a 64 Kbyte banks for memory protection applications.
Piiceon, 2045 Lundy Ave., San Jose, CA 95131.

S-100 Bus Buyers Guide

The new 1982 exclusively S-100 Bus buyers guide lists more than 450 S-100 Bus compatible board-level products from over 65 manufacturers. The publication includes 23 μC-product categories such as single-board computers, peripheral controllers, and video boards. Thorough product descriptions include design and performance specifications, prices, delivery-availability and date first manufactured, as well as manufacturers local sales offices. Purchase of the guide also includes new S-100 Bus product announcements between issues. *The S-100 Bus Buyers Guide* is published semi-annually and is available for $25.00 prepaid, from the publisher, (Add $10.00 per copy outside the continental USA), each additional copy $9.95, included in the same order to the same address. Contact: Ironoak Company, 3239 Caminito Ameca, La Jolla, CA 92037; (714) 450-0191.

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pulls LOW the hold request line (pin 74).

For critical realtime or multiuser applications, the interrupt bus permits any slave to interrupt the master to do another task. The interrupted program completes the second task and returns to its primary one. Priority is assigned by line, VI0 has the highest, VI7, the lowest; VI7 is serviced last if simultaneous interrupts occur. The INT line, unless masked by the master, interrupts the master. In the event that an imminent disaster or critical task needs immediate attention, the NMI or non-maskable interrupt line gets the master's attention and cannot be masked.

The TMA or Temporary Master Access bus permits temporary masters to request and receive access to a slave without using the permanent master's program. Otherwise, the permanent master would access the slave via a program. The old term DMA is obsolete, as the TM can perform any type of bus cycle, not just memory; and, unlike the pre-696, which had only one TMA device, 696 permits up to 16. If conflicts occur, the highest priority TM requestor gets bus control. The TMA process is more complicated than the others we have discussed.

The final bus group, the utility bus, has two subgroups: utility signals that did not fall into the previous seven groups, and the power/ground lines. The 696 has three voltage lines: ±16VDC and ±8VDC (nom.)—all unregulated, which can be a problem. Five primary ground reference lines (pins 20, 50, 53, 70, 100) exist.

Utility signals include the master clock signal, an independently running 2–MHz clock, memory write strobe, bootstrapping, power on clear, reset, slave clear, impending power failure and an error-has-occurred line.

S-100 Or Multibus?

From the start, Multibus was defined to be more "designable". Knowing the maximum capacitive dynamic load, how much maximum shunt capacity per board (to its connected signal lines), capacity per connector, plus wiring, it is then easy to determine the greatest allowable number of cards for your system. This generally comes out to 12 or 17 cards.

The S-100 system designer has it a lot rougher. Traditionally, he has had problems working out the rated capacitive loading, the propagation delays and how big his dynamic load can be (yet not exceed rated use and fall-times). This procedure is more one of iterative convergence, rather than one of clear cut easy to calculate parameters. In the end, it's necessary to do more benchtop debugging of the prototype board. This is one of the reasons, aside from lower costs, that

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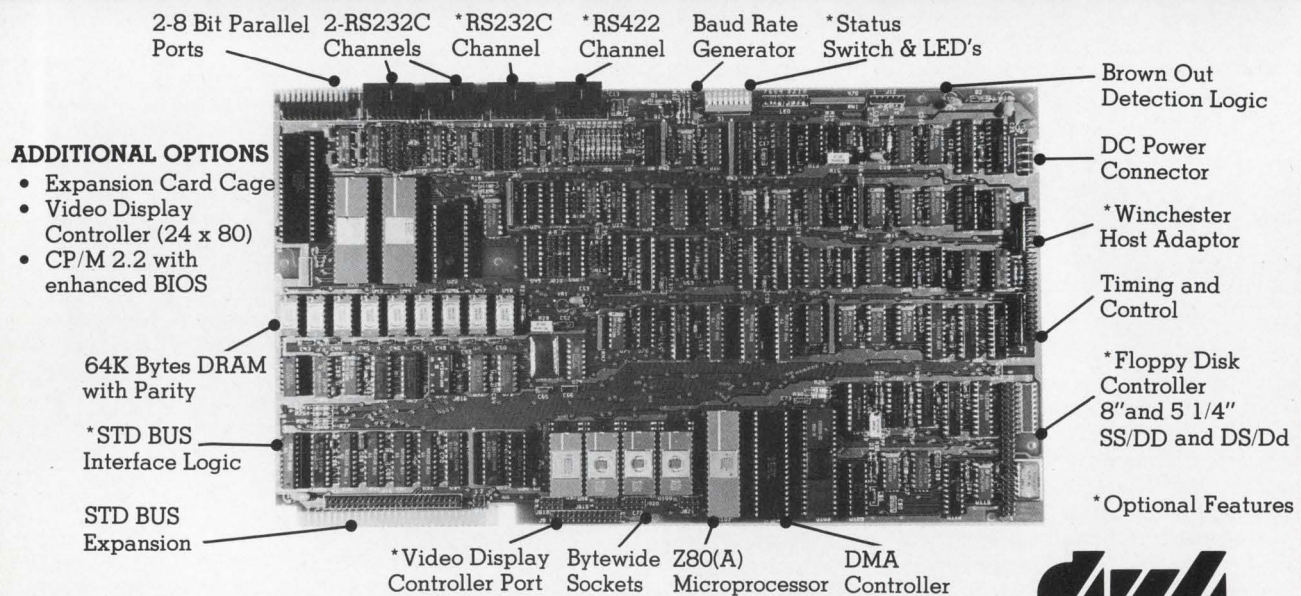

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cottage shops can do well with the S-100. The many ingenious, engineers-turned-entrepreneurs possess the design knowledge and time, that a larger established company will not want to (or be able to) be bothered with.

As for power, the S-100 supplies unregulated DC on the backplane (not at the supply, as does Multibus), so that each card can have a couple of regulators dissipating heat near sensitive components. This helps boost MTBF's downward and users' tempers upwards.

Since the S-100 traditionally had a potential for formidable transient swings near TTL-compatible signals, crosstalk became a thorny design problem. Worse yet, if bench top testing of the prototypes wasn't adequate, the system could create glitches in signal lines under certain conditions not discovered until after a few months in the users' environments. In large firms, testing is likely to be more thorough, whether it includes chattering relay, zap gun, hot box, surge and other testing. The cottage shops or small OEM businesses are less likely to do extensive testing, either because their designers are less knowledgeable about electronics test or because the equipment and resources are inadequate. Getting back to transients, grounding is a help. But with the S-100 it is not easy to ground out noise.

As for bus arbitration (something discussed first in the IEEE-488 article) Multibus' multiple mastering is superior. It supports multiple SBC's, each with its own program and data storage. Use of the data bus is for memory references to be shared among SBC's. This means that the data bus is used less, as the CPUs will spend more time referring to their own memory or peripheral circuitry. This improves intersystem throughput.

The Future

The cottage and "lemonade stand" firms of the mid to late 1970's either went bust, as most did, or grew up and usually out of the hobbyist market.

Since many sold originally to hobbyists, they had to sell on a lower margin to capture sales and compete against the hordes of cottage/basement industries sprouting up like weeds. Retail prices should be 1.5 to 2.0 times material costs, yet were not. This meant that many of the survivors of the "hobbyist wars" of the 1975–80 time frame developed some bad marketing practices that were to hurt them. Once they received financial backing, expanded plant equipment purchases, hired more personnel and began spending more, these bad management practices took their toll. Such price-ignorant entrepreneurs are now less significant, and the markets for S-100 products are more professional today. A big impetus to the S-100 is the rapid opening of new niches in the small business computer and industrial markets. Costs dropped below a critical threshold in early 1981. This threshold was passed quietly, without fanfare or publicity, but is beginning to make a large impact.

The standardization of the S-100 bus has also added to the bus's resurgence. Designers no longer need feel uneasy about the bus. The 696 bus now compares quite well against other 16-bit buses and does well against other high-performance buses. In standardizing the S-100, the IEEE committee extended address paths to 24 bits, added two handshaking lines for multiplexing 8- and 16-bit memory cards and gauged the data-in/out buses to create a 16-bit data bus. The committee wisely added extra ground lines and took additional measures to overcome source-to-load ringing, loading and termination woes. A multi-master arbitration bus enables up to 16 masters at one time on the bus. An error, power fail and three specialized user lines were added, making 696-based systems more reliable and flexible. □

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Do It Yourself VLSI

by Bill Groves

Uncommitted logic arrays, programmable logic arrays, or simply gate arrays, have been around for a long time. Now they appear ready to take off and dominate the random logic market in this decade. If the 1970's was the decade of the μP and memory, then the 1980's may be on the way to becoming the decade of the gate array due to two main driving forces. First, computer-aided design techniques now available make it relatively simple to deal with arrays containing 5000 to 10,000 equivalent gates. Second, the cost of using discrete SSI/MSI logic packages on a PC board has increased, mainly due to inflation without a corresponding improvement in price or performance of the devices. The discrete SSI/MSI TTL, CMOS, and ECL devices may very well be at or past their point of peak efficiency for new designs in both cost and performance.

VLSI For Everyone

Gate arrays consisting of gates or logic cells offer all of the economy and reliability of large scale integration. John Carey, Motorola's gate array product manager, predicts that gate arrays have the potential to replace about 50% of the standard discrete SSI/MSI logic as early as 1985. Most array suppliers have almost identical forecasts and see the market exploding just as μPs did in the 70's. In today's dollars, 50% of the discrete TTL/CMOS/ECL business could amount to $1.0 to $1.5 billion by 1985.

Gate arrays begin moving from semi-custom to semi-standard products.

That big a market in such a short time has attracted a large number of companies to the gate array business. Some vendors feel that there are 30 to 40 serious companies now—a few place the number much higher. Since gate arrays are still considered a semi-custom product, there are as many design variations as there are companies in the business. A systems designer with zero experience in IC design should be able to implement his logic in an array with a minimum understanding of device physics or semiconductor processing in a few months.

What Are Gate Arrays?

During the mid-1970's, gate array technology began to serve the larger digital equipment market with quick turnaround LSI random logic devices. IBM was a leader in developing arrays for internal use and now has a gate array capability that can produce finished silicon from a logic diagram in a few weeks (some say a few days).

Arrays are basically very simple devices consisting of transistors and resistors arranged in a very orderly fashion. The semiconductor house is able to mass produce these basic wafers in most cases using their standard TTL, CMOS, and ECL process. Arrays are completely

Process	Product No.	Gates	I/O Pads
Single Metal	GA-2500	2500	84
	GA-2000	2025	74
	GA-1500	1500	64
	GA-1000	1020	52
	GA-500	500	36
Double Metal	GA-5000D	5000	120
	GA-4000D	4000	100
	GA-3000D	3000	84
	GA-2000D	2000	74

Table 1: AMI's 3-micron CMOS gate array configurations.

processed except for the metal interconnects that connect the resistors and transistors into logic gates or functional blocks. Up to this point, all of the array manufacturers are doing virtually the same thing.

The next step, metalization interconnect, is where they begin to differ. Some use a single level of metal to interconnect all of the components at one time into a complete logic function. Others use a double metal process to first connect resistors and transistors into well-defined logic cells, then a second level of metal connects the logic elements into the complete logic array; some vendors, like AMI, offer both. Each of these approaches can result in the same type of end product, but the double-metal approach may be the easiest when complexities of 10,000 or more gates are involved.

Where To Start

If you are now designing logic for a system based on SSI/MSI IC's, you could begin using gate arrays today with very little change in your basic design approach. Most of the array suppliers will take your logic diagram and return a product in silicon in about three months. You had better move fast, however, because the array vendors are trying to discourage this type of business. They would prefer that you design, debug, simulate, and test your own gate array. Some have made it easy for you to use your own CAD system and their software to design at home, while others want you to plug into their large design computer. A third approach requires you to do your design on the array maker's site.

The differences in these approaches for the system designer may be a matter of personal preference. Some designers, especially first-time users, may want to take the easiest possible approach with least involvement. This may be an overly cautious approach—it certainly will be more costly. All of the array suppliers interviewed for this article have some sort of formal training and complete documentation available to help the first-time array designer do it right as quickly as possible. It is important to remember that the array vendors have spent a lot of time trying to make the device physics and processing transparent to the user. Most compare designing an array with the complexity of doing the same function on a double-sided PC board with discrete logic devices. If you can do that, you can design a gate array. It is simply integrating your logic design into a piece of silicon.

Arrays are not the Mead-Conway approach to systems design in silicon. To fully implement the Mead-Conway philosophy, the systems designer would have to understand a lot more about device physics and semiconductor processing. Arrays do offer some of the advantages, but they can keep the logic designer from becoming a semiconductor designer. Gate arrays may very well be the bridge to the Mead-Conway approach.

Array Economics

Development costs for a gate array exist because the products are semi-custom. Full use of the CAD techniques available can reduce these front end costs; volume can make the difference. The more you use, the less they will cost per unit. Quantity is a very important consideration in deciding to use a gate array. Generally, the array suppliers feel that if you use less than 5000 devices in a year, they may not be the best way to go. Once you commit to an array, you cannot change it without paying a high penalty. Under 5000 devices per year should make you look seriously at field programmable logic arrays. Both Signetics and Monolithic Memories offer a large selection of fuseable link programmable logic arrays. These products suffer the same disadvantages as PROM's in high volume applications, and they are also limited in complexity to a few hundred gates.

Hybrid circuits may also be an economically attractive solution to low-volume production where a semi-custom solution is needed. Hybrids can get expensive and are mainly limited to existing devices. They are more reliable than components on a PC board, but not as reliable as a design implemented totally in silicon. Many consider hybrids a packaging solution only.

High volume applications for gate arrays (over 100,000 devices per year) should also be examined very carefully. At some point over 100K devices, a full custom solution may make economic sense. Gate arrays have the distinct advantage of rapid turnaround—today they can be produced in three or four months; by next year it may be three or four weeks. Full custom designs normally take 1 to 1½ years, which can be a very long lead time in today's competitive world. Arrays are not as efficient in the use of silicon and do not offer the performance potential of a full custom design. They do offer many of the custom advantages at reasonable cost, quickly. These are important tradeoffs that should be considered very early in your design cycle. If the array producers

do shave turnaround time to a month or less for the full cycle to finished silicon, they may be able to beat the long lead times required to get discrete SSI/MSI devices in today's IC market. Full custom design turnaround will get better as CAD techniques improve—but not dramatically for awhile.

Retrofit

Arrays for new designs make both technical and economic sense. The same may not be true for converting existing designs into arrays. It may be very easy to justify the economy of replacing 30 or 40 IC's and a large PC board with a single gate array. However, if your product is at the mid-point of its life cycle, it may not be worth this effort. Changes to retrofit an existing system may be more expensive to manufacture, service, train, document, etc. than the product is capable of returning.

If you are early in a product's life cycle, or you need a performance improvement, then gate arrays may be a valid economical solution. Certainly many areas in peripheral controllers, graphics terminals, etc. can benefit by eliminating costly circuit boards and their overhead.

Technology Options

Just about every technology found in discrete logic IC's can be had in gate array form—TTL, CMOS, ECL, I^2L, etc. By 1985, most array producers predict that the market will divide into three main technologies: 20% going to ECL for super high-speed applications, 50% to CMOS for most general applications, and the 30% remaining will go to TTL, ISL, I^2L and STTL.

Many array producers, like LSI Logic Corp, are now bringing a 2-micron dual metal HCMOS technology into the array market. It is quite possible that this small geometry CMOS will squeeze out the TTL and other popular bipolar logics, leaving the array market to ECL for the high performance and CMOS for the other applications. To get the speed and performance in ECL, the obvious penalty is high power dissipation, and this may put some limits on ECL array complexity. The heat and power problems, while not severe, also apply to the other bipolar technologies. CMOS performance is at least equal to most of these bipolar technologies with the added advantage of its very low power consumption.

A

Type	Technology	Gates	Typ. Gate Delay
Q400	Linear/Digital	1500	15 ns
Q401	Linear/Digital	800	15 ns
Q410	Digital CMOS	1000	15 ns
Q411	Digital CMOS	500	15 ns
Q412	Digital CMOS	300	15 ns
Q413	Digital CMOS	700	15 ns
Q415	Digital CMOS	1000	15 ns

B

Type	Gates	Typ. Gate Delay	Chip Power Description
Q720	250	1.3 ns	540 mW
Q710	500	1.75 ns	940 mW
Q700	1000	1.75 ns	1.63 W

Table 2: (a) AMCC Quick Chip CMOS arrays. (b) AMCC Quick Chip bipolar arrays; these are ECL arrays with a choice of TTL or ECL 10K I/O's. TTL I/O reduce performance because of level shifting.

Design Approaches

Since arrays come in all sizes and technologies from perhaps 40 different vendors, there is little in common among the arrays. There are really two basic design approaches. First is the dedicated macrocell approach pioneered by Motorola; we will call this a hard macro. Second is a software macro used primarily in the single-level metal products; we will call this a soft macro. These are design techniques that make it easier for the logic designer to convert his logic (usually specified in TTL 7400 series devices) into an array.

Hard macros are normally created by first-level metalization of the array. Individual transistors and resistors on the macrocell array are grouped into convenient cells. Motorola, for example, offers an option of major and minor cells that can be placed on the array at designated locations. Minor cells might be easily configured as I/O, while flip-flops, clock drivers, multiplexers etc. are created in the major cell locations. During first metal, the cells are connected into individual functional elements. Power and other chip housekeeping are also performed on first level. Next, vias are created where needed to connect first-level metal to second-level metal. The second level of metalization is then applied to connect the logic functions in the cells to form the complete gate array.

Soft macros go through the same two-stage wiring process. The macros, however, are not placed on predetermined locations but are connected at random on the array to form the individual macro functions. At the same time, the functional elements are being connected to form the complete array. The soft macro essentially resides in software where the hard macro becomes a characterizable function that can be repeated in silicon over and over.

The soft macro is a product of computer-aided routing and placement, while the hard macro was originally developed for manual layout. The hard macro looks as if it may become the most popular design approach since it fits nicely into the two-level metal process needed for higher performance CMOS and for higher array complexities. Today, most hard macros are also auto routed and placed.

There is a small tradeoff be-

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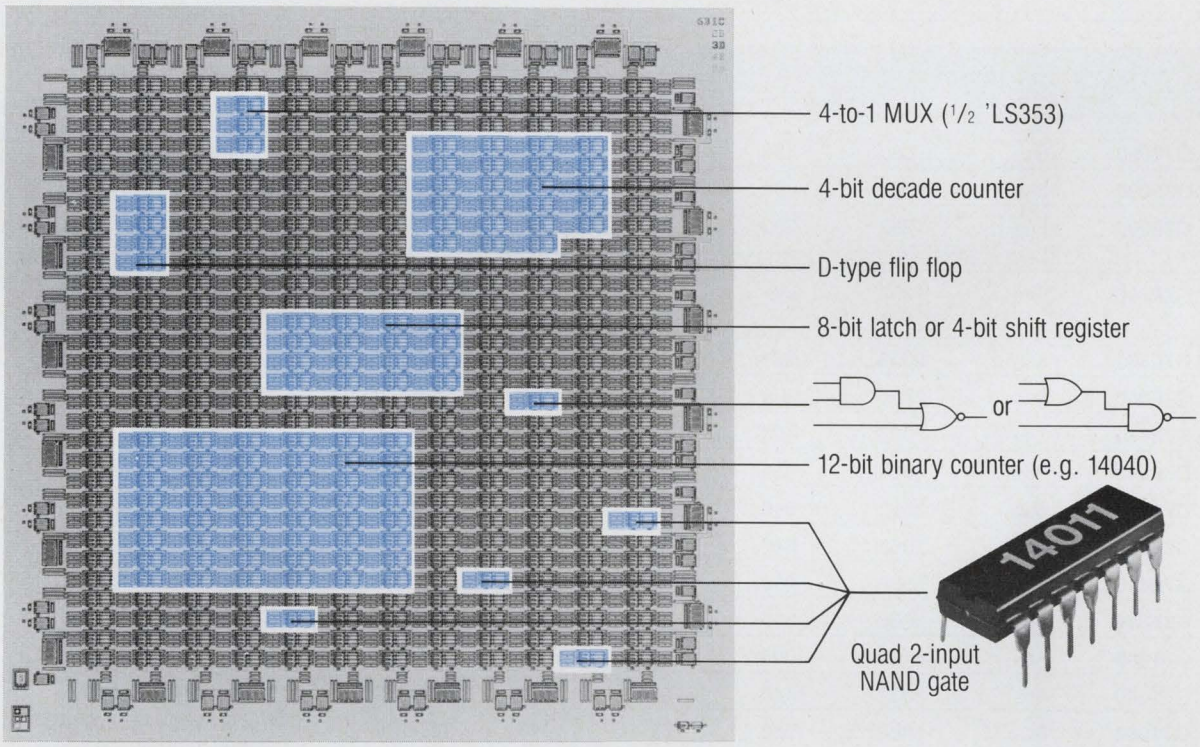

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Write 19 on Reader Inquiry Card

A

Part Number	Total Transistors	Available Gate-Cells	Available I/O Pins	Die Size (mils)
G4060	340	60	23	78x87
G4112	614	112	29	98x108
G4160	862	160	35	108x129
G4220	1174	220	38	129x138
G4264	1400	264	41	138x150
G4312	1648	312	43	150x158
G4364	1916	364	47	158x171
G4420	2200	420	49	171x178
G4480	2508	480	53	178x192

B

Part Number	Inverter Delay	Total Transistors	Logic Cells	Output Drivers	Interface Pads	Die Size
G70090	5ns	580	90	28	32	80x90
G7F090	3ns	580	90	28	32	80x90
G70200	5ns	1292	200	19	40	111x131
G7F200	3ns	1292	200	19	40	111x131
G70360	5ns	2256	360	25	52	150x150
G7F360	3ns	2256	360	25	52	150x150
G70490	5ns	3000	490	54	58	175x175
G7F490	3ns	3000	490	54	58	175x175
G70640	5ns	3968	640	33	68	189x189
G7F640	3ns	3968	640	33	68	189x189
G70810	5ns	5008	810	72	76	216x216
G7F810	3ns	5008	810	72	76	216x216
G71000	5ns	6160	1000	41	84	229x229
G71440	5ns	8832	1440	48	100	268x268
G71960	5ns	11984	1960	57	116	308x308

Table 3: (a) G4000 series metal gate CMOS arrays; (b) G7000 series silicon gate CMOS arrays.

tween soft and hard macros in terms of most efficient use of silicon, with the hard macro requiring better-defined routing channels. This is mainly of concern to the array manufacturer; however, it could in some cases, like ECL arrays, have a minor impact on performance.

Logic partitioning, simulation, design verification, and test program generation are the key parts of the array design process that remain unique to each vendor. They will be presented with each manufacturer's product description.

Second Sources

Sorry, but they don't exist in the world of gate arrays, yet. Many of the design approaches and processes are very close, but the semicustom nature of arrays makes it extremely difficult, if not impossible, to get a second source for an array. Transportable software will solve this problem to some extent. Users who do their own design and furnish the vendor with a tape containing partitioned logic and a full simulation will find it easier to get a vendor to convert a design to his system. Some of the front end tooling costs will have to be paid to get a second source. Even then it will not necessarily be a 100% compatible second source product.

A better way to approach the second source problem may be on the front end negotiations with the vendors to make sure that designs and processes are actually moveable from vendor to vendor.

Standards do not yet exist for arrays, and this presents even more problems trying to find multiple sources. With design approaches varying from colored pencils and a mylar grid, up to super computers that automate the entire design process combined with every vendor's process variations, second sources, as we know them, with discrete logic devices and memory may never exist.

How close can you come to a second source? Motorola and National Semiconductor have a second source agreement for ECL macrocell arrays. LSI Logic also claims to have an independently developed ECL macrocell design that is also a second source to Motorola. Since all three companies use different design systems, their commonality may be marginal.

Packaging

If you need a 5000 gate array and want to put it into a 40-pin package, you had better look at your last PC board design. Since you are compressing 50 or so SSI/MSI devices into a single gate array, you can only eliminate *some* of the I/O's. If the array is under 1000 gates, it may need a 64-pin dual-in-line package. Between 1000 and 6000 gates, pin counts range from 100 to 180 pins, and beyond 6000 gate arrays to 10,000 gate arrays, expect to see about 224 or more pins.

Pin grid arrays and leadless chip carriers appear to be the most practical solutions to the high pin count problems at present. Both present handling problems that will be solved by better chip design in the future, but considering complexity and testability, dramatic reductions are not likely.

Testing Dilemma

Most of the hard macrocell array suppliers have made it very easy to generate test programs and the A/C test data as part of the design and simulation.

The hard macrocells are specified with typical delays in catalog

Companies In The Gate Array Business

While it is very difficult to get an exact feel for the size of the gate array market today, estimates place it in a range from $400 to $500 million. Growth to $1 or $1.5 billion in the next two years will require more suppliers or more design capacity. Although not comprehensive, the following list of array suppliers gives some idea of the number of companies in the field. Use the accompanying write numbers and the Digital Design inquiry card to obtain further information.

Gate Array Suppliers

Analog Innovations, Inc. Los Gatos, CA (Write 300)	Western Design Center for Cherry Semiconductor Linear/digital arrays and I^2L
Applied MicroCircuits Corp. Cupertino, CA (Write 301)	Si Gate CMOS
American Microsystems, Inc. Santa Clara, CA (Write 302)	Si Gate CMOS
California Devices, Inc. San Jose, CA (Write 303)	Metal and Si Gate CMOS
Cherry Semiconductor E. Greenwich, R.I. (Write 304)	I^2L and Linear/digital
Custom Integrated Circuits Minneapolis, MN (Write 305)	I^2L
EXAR Integrated Circuits Sunnyvale, CA (Write 306)	Metal Gate CMOS and I^2L
Fairchild Semiconductor Mountain View, CA (Write 307)	ECL, I^2L, and STTL
Ferranti Semiconductors Commack, NY (Write 308)	CML and CMOS
Fujitsu Microelectronics Santa Clara, CA (Write 309)	Si Gate CMOS and I^2L
General Instruments Hicksville, NY (Write 310)	Si Gate CMOS
GTE Microcircuits Tempe, AZ (Write 311)	Si Gate CMOS
Harris Semiconductor Melborne, FL (Write 312)	Si Gate CMOS, I^2L, and STTL
Hughes Solid State Newport Beach, CA (Write 313)	Si Gate CMOS
Interdesign, Inc. Sunnyvale, CA (Write 314)	Metal Gate CMOS, CML, NMOS and bipolar/linear
International Microcircuits, Inc. Santa Clara, CA (Write 315)	Metal and Si Gate CMOS
LSI Logic Corp. Milpitas, CA (Write 316)	ECL and Si Gate CMOS
Master Logic Corp. Sunnyvale, CA (Write 317)	Metal and Si Gate CMOS
Microcircuit Technology Santa Clara, CA (Write 318)	Metal Gate CMOS
Mitel Semiconductor Kanata, Ontario, Canada (Write 319)	Si Gate CMOS
Monolithic Memories Sunnyvale, CA (Write 320)	Field Programmable Logic Arrays
Monosil, Inc. Santa Clara, CA (Write 321)	Metal Gate CMOS
MOSTEK (UTC Microelectronics) Carrollton, TX (Write 322)	Metal Gate CMOS
Motorola Semiconductor Phoenix, AZ (Write 323)	ECL, Metal and Si Gate CMOS, STTL
National Semiconductor Santa Clara, CA (Write 324)	ECL, Si Gate CMOS
Nitron Cupertino, CA (Write 325)	Metal and Si Gate CMOS (alternate source to Universal Semiconductor)
Plessey Irvine, CA (Write 326)	ECL and Si Gate CMOS
Raytheon Mountain View, CA (Write 327)	STTL
RCA Somerville, NJ (Write 328)	Si Gate CMOS
Semi Processes Inc. Santa Clara, CA (Write 329)	Si Gate CMOS
Signetics/Philips Sunnyvale, CA (Write 330)	ECL, Si Gate CMOS, ISL and STTL Field Programmable Logic Arrays
Synertek/Honeywell Santa Clara, CA (Write 331)	CMOS
Texas Instruments Houston, TX (Write 332)	STTL and I^2L
Telmos Santa Clara, CA (Write 333)	Metal and Si Gate CMOS
Universal Semiconductor San Jose, CA (Write 334)	Metal and Si Gate CMOS
Western Digital Newport Beach, CA (Write 335)	Metal Gate CMOS

form much like their SSI/MSI counterparts. These can be used for preliminary performance calculations. During simulation of the array, when the exact wire lengths have been determined, the actual wire delays and circuit delays can be combined to provide very accurate delay data. John Carey at Motorola indicates that wire delays for ECL arrays can be estimated at 4 psec/mil of wire with a capacitive loading of 0.008 ppf/mil. These figures can then be calculated to exact value during simulation to verify array performance.

Array complexity makes testing more complicated. Pin counts up to 200 push the limits of many popular testers. Wafer probing at these pin densities is pushing current probe card technology. Automated handling for the newer packages and high pin count devices is almost nonexistent.

Probably the most important aspect of array testing takes place in the preliminary design phase. It should be clearly defined very early—know what to expect from the supplier before you get into silicon.

Full Service

The most common message received from the array manufacturers is that it is a service-oriented "hand holding" business. Some will guide you through the design process making it as easy as possible. Universal Semiconductor and LSI Logic are willing to work on a one-to-one basis with their customers, while others prefer that you get up and running on a CAD system as soon as possible. For the array user, the choice is to pick an approach that you feel comfortable using. It is wise to select a total package of design and product rather than zero in on product alone.

Array suppliers that offer the full service from design to silicon also help minimize risks in a semi-custom design. This one-stop shopping is also a trend among the suppliers, with many companies that provided only array design in the past quickly adding wafer fabrication facilities. A small supplier that has invested in a fab facility will probably be around for a long time.

The major problem in any semi-custom product is error. Assuming that your logic design is valid, the conversion to an array is capable of introducing errors. All of the array suppliers have built-in error checks, etc., but no system is perfect. The ultimate responsibility for a design working in array form rests with the logic designer. The array manufacturers will help manage the risks, but they are not system designers—more important they may not really understand your logic; they are chip makers.

If your logic is valid and you go through the design cycle with the array supplier, the probability of gross error is remote and the risks are minimal. Full logic simulation is a must in the design cycle.

Factories And Foundries

Many large systems companies have their own internal semiconductor capabilities from small pilot lines all the way up to full fab facilities. These companies may begin to do their own metalization in-house, buying basic unwired arrays—some may even go as far as designing their own arrays from the wafer up.

Few of the array manufacturers see this as a wide spread practice;

A

Part Number	Gate Complexity	Max. Pins	Major Cells	Interface Cells	Output Cells	Major Cell Gate Delay (ns typ.)
LCA 600 ECL	600	68	24	25	18	0.9-1.3
LCA 1200 ECL	1200	68	48	32	26	0.9-1.3

B

Part Number	Gate Complexity	Max. Pins	LS Output Buffers	TTL Output Buffers	Gate Speed (ns) Typ.
LC 3100	300	40	17	20	5
LC 4100	400	46	23	20	5
LC 5400	540	52	25	24	5
LC 7700	770	62	31	28	5
LC 10000	1000	70	35	32	5
LC 12600	1260	78	39	36	5
LC 17800	1782	92	43	46	5

C

Part Number	Gate Complexity	Max. Pins	Metal Level	Gate Length (μ)	Gate Speed (ns) Typ.
LSI 5080	880	74	2	3	2.5
LSI 5140	1404	84	2	3	2.5
LSI 5220	2224	114	2	3	2.5
LSI 5320	3200	138	2	3	2.5
LSI 5420	4200	148	2	3	2.5
LSI 5600	6000	180	2	3	2.5

D

Part Number	Gate Complexity	Max. Pins	Metal Levels	Gate Length (μ)	Gate Speed (ns) Typ.
LSI 7080	880	68	2	2	1.5
LSI 7140	1480	84	2	2	1.5
LSI 7200	2010	128	2	2	1.5
LSI 7320	3200	144	2	2	1.5
LSI 7420	4200	160	2	2	1.5
LSI 7600	6000	180	2	2	1.5
LSI 7800	8000	200	2	2	1.5
LSI 71000	10000	224	2	2	1.5

Table 4: (a) LCA 1200 series oxide isolated ECL macrocell array; (b) LC 3100 series silicon gate CMOS macrocell array; (c) LSI 5000 series silicon gate HCMOS macrocell array; (d) LSI 7000 series silicon gate HCMOS macrocell arrays.

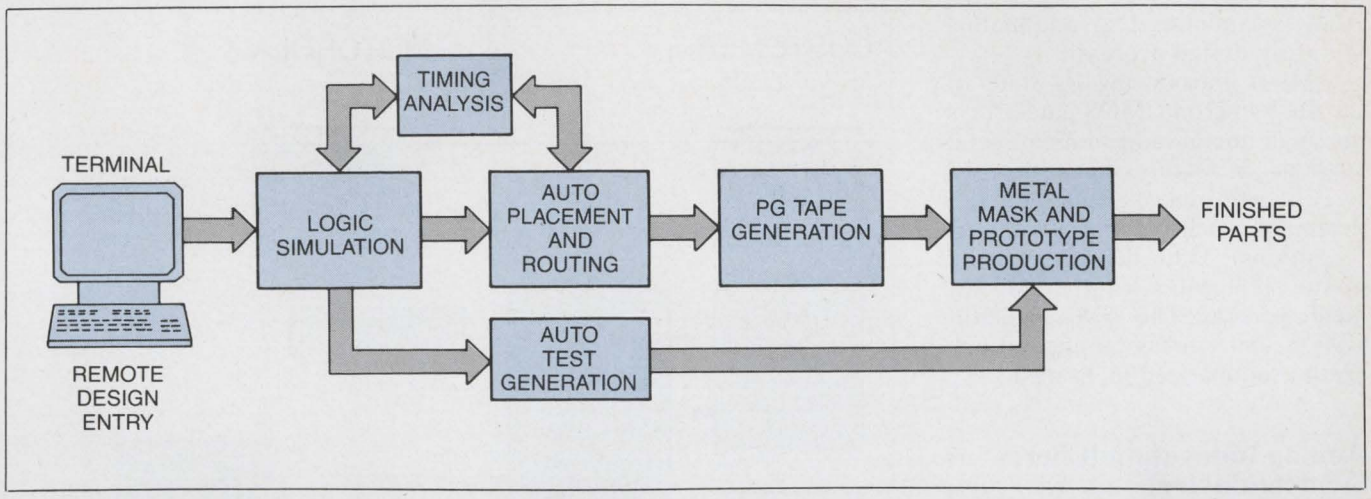


Figure 1: LDS-1 functional outline from LSI Logic Corp.

however, Joe Mingione of AMCC predicts as much as 20% of the arrays produced by 1990 could be in captive metal plants.

It is doubtful that many systems houses would consider adding full wafer fab facilities when a modest facility costs between $15 and $30 million today. Only with an internal consumption of thousands of array types, or a large volume of other products, could any systems organization justify a full fab line.

Metal at home may have some attraction to the military systems houses to protect classified chip designs and systems. The novelty value of doing the metal may not last very long, especially as array houses get more competitive.

Design-Only Houses

Many array design companies offer standard array designs; many have produced excellent arrays, but lack fab facilities. These third party designers depend on semiconductor manufacturers for their basic wafer lab in a silicon foundry style of operation. Their ability to purchase wafers is good in today's economy, but if and when the semiconductor companies return to full capacity operation, these design-only organizations may experience long delays in getting their wafers processed. If your system has a critical turnaround on an array, the design-only companies could be the wrong place to shop. There is also the question of assigning blame if the design does not work in silicon. With three parties involved in an array, it may be very difficult to assign blame for a failure.

Arrays From Distributors

Don't be surprised if you find your local distributor selling gate arrays in the next few years. Right now, those providing engineering support for μPs could easily make the transition to remote design centers for gate arrays. In fact, with minimal equipment investment, most distributors could get into the business. The larger semiconductor companies may welcome this buffer in the sales chain in a short time. Motorola, for example, is beginning to train its field applications engineers in gate array. When Motorola adds the terminals to its field offices, they will have over 100 mini-design centers.

Who Owns The Tooling?

To create tooling for a gate array, the customer's proprietary logic design is implemented in silicon using the array manufacturer's proprietary design system and process. Once the array tooling (a CAM program, etc.) exists, it is a combination of these two proprietary pieces. This is a point to consider, especially in second sourcing an array. Can you really take the tooling from one array house to another? What if any of the parts of the tooling are transportable? While this does not appear to be an issue at present, it could come up as the competition in the array business gets tougher.

MA5050	252 gates	38 I/O's
MA5100	480 gates	48 I/O's
MA5150	720 gates	62 I/O's

Table 5: CMOS arrays available from Mitel.

Where Will It End?

In the not-too-distant future, it is possible that arrays will be produced by simply entering logic equations into the computer, and the arrays will be turned out by a direct writing E-beam on the wafers. Until then, there are a lot of rough spots that have to be fixed. Computer-aided design holds the key to gate arrays achieving the market potential possible. Better CAD systems and smarter software are needed right now.

American Microsystems

In the custom IC business since 1966, AMI has moved into gate arrays in a big way. Trying to remain flexible as possible, they produce CMOS arrays using both hard and soft macro approaches in single and double metal processes. Late this year, a 3μ Si Gate process will be added to the current 5μ family of devices.

John Edward, director of array products at AMI, looks at arrays as a low-cost quick-turnaround semi-custom solution for the customer.

AMI is committed to automating the array design process.

AMI is introducing its state of the art 3-micron CMOS gate arrays in single-metal and double-metal versions. It features high speed (2 to 3 ns gate delays) and total I/O flexibility (each pad can be one of 13 options). Gate densities can be up to 5000 gates for the double-metal version. The AMI 3-micron CMOS gate array configurations can be summarized in **Table 1**.

Analog Innovation (Cherry Semiconductor)

A design house specializing in custom ICs, Analog Innovation has recently established a design center in Los Gatos, CA, to provide design and engineering services for the Genesis line of arrays manufactured by Cherry Semiconductor.

The Genesis series of semi-custom IC's includes 5 linear arrays (187 to 815 components), one 335 component linear flip-chip array and 3 I^2L gate arrays (192 to 288 gates). The I^2L arrays include analog capability as well as opto electronic custom capability via silicon photo detector chip and an array housed in a transparent package. These products may have some very interesting special purpose applications, particularily in analog to digital interfaces.

Applied Micro Circuits

AMCC claims to be the most automated array company in the business, but compared to many other array houses large and small, they do not appear to have any significant advantage. The company's design process is highly automated based on a TEGAS simulation system through the CDC Cyber Net. AMCC also offers TEGAS file development with test pattern generation. By comparison, AMCC not only lacks an extra edge in the CAD area but also has a fairly limited line of products.

Joseph Mingione, AMCC's Vice President, does have some interesting points to make about the market. Like many people he sees the dollar potential over $1 billion by 1985. Mingione also sees automated design software generally available and very wide-spread use of color graphics for design display terminals. His most interesting prediction is that array users will begin to bring their own metalization factories on line beginning in 1984 with the semiconductor manufacturer granting array licenses to end users.

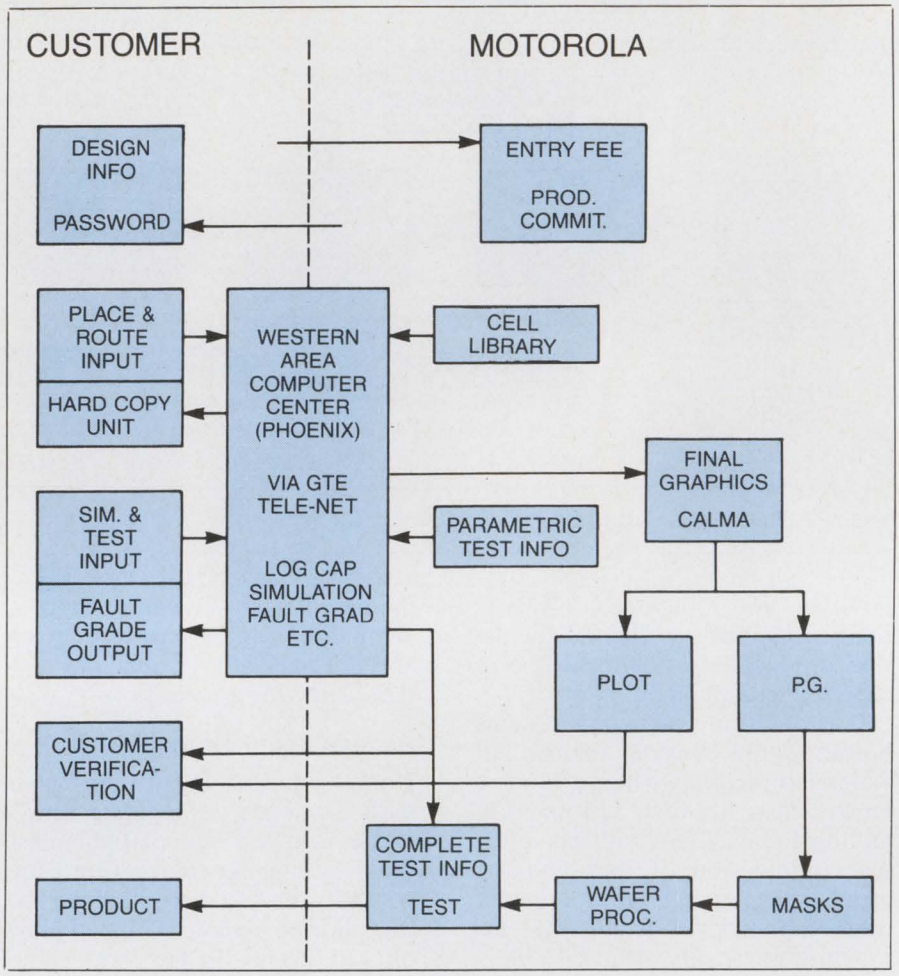


Figure 2: Motorola's macrocell array option development flow.

By the end of the decade, Joe Mingione sees logic equations being entered directly into standalone array design computers with software interface to direct write-on-wafer technology. At this point, more than 20% of the metalization would be performed in user-owned metalization factories.

AMCC has developed one very interesting design aid—a Benchmark System Array. It is a standard AMCC series Q700 array interconnected with a variety of logic and I/O configurations enabling the systems designer to benchmark array performance characteristics. The Benchmark Array has 10 logic and I/O combinations to provide a method to evaluate, measure, and analyze propagation delays, toggle rates, I/O loading, output drive, ECL threshold tracking and input stability.

AMCC is also one of the very few array suppliers producing CMOS arrays with both linear and digital array functions on the same chip **(Table 2)**. Operational amplifiers and comparators and other linear functions are available in one quadrant of the chip, with the other quadrants devoted to digital functions. Functions such as switched capacitor filters, finite state machines, charge distribution A/D converters, current mirror function generators, multiplexed LCD display drivers, and digital filters can be implemented on these

ECL Arrays	
600 Gates	These are alternate source products to Motorola.
1200 Gates	
2400 Gates	This is also a second source to Motorola although no second source agreement has been completed.
CMOS Arrays (Double Metal Oxide Isolated)	
1200 Gates	All of these devices are built with 2 to 3μ geometries and are expected to achieve a 1 ns typical gate delay late this year versus a 2 ns delay currently offered.
2400 Gates	
4800 Gates	
6000 Gates	

Table 6: ECL arrays and CMOS arrays (Double Metal Oxide Isolated). All of the NSC ECL arrays are available with a choice of ECL or TTL I/O's. Gate delays average 1 ns typical, and NSC expects to achieve 0.5 ns by next year. All of the CMOS arrays can be supplied with TTL I/O's.

linear/digital CMOS arrays.

In May, AMCC announced that its 4" wafer fabrication facility located in San Diego would be available to support outside array manufacturers. Many of the smaller design-only gate array houses may take advantage of this facility to process their wafers silicon-foundry style. In July, AMCC signed an alternate source agreement with Thompson-EFCIS in France. Thompson will operate an independent design and manufacturing facility. Signetics/Philips is also an alternate source of the AMCC Q700 series of arrays.

California Devices

Single mask programmable Si and metal gate CMOS arrays, ranging from 300 to 1782 gates, are available in 7 options from California Devices, Inc. (CDI). Internal gate delays are in the order of 3.5 ns. CDI offers a variety of customer interface points from simple logic diagrams up to full CAD inputs with many alternatives along the way. They are also capable of generating Sentry test programs for production testing. As part of their array design training program, CDI supplies the user with a complete design manual, data base tapes, and a soft macro cell library to make design as easy as possible.

Ferranti Semiconductor

Ferranti announced its entry into the US gate array market last February with about 20 different array types, each with many performance variations. These bipolar and CMOS arrays range in complexity from 100 to 2400 gates, with 4000 and 10,000 gate products scheduled for design availability sometime during 1982. Ferranti has been producing gate arrays or, as they prefer to call them, ULA's (uncommitted logic arrays) in the UK since the early 1970's.

The design process used by Ferranti is highly automated. They offer a DEC-based CAD system that they will sell to the serious array user for over $100,000. The system is impressive, and they offer extensive customer training on their CAD system in their design approach. If you find $100K more than you can afford for your first array design, you have the option of using the system at the Ferranti Design Center in Commack, New York.

Without the ULA Designer CAD system, Ferranti does not specify any other preferred interface for less affluent customers.

Ferranti also has its manufacturing operations in the UK. Signetics/Philips seemed to have solved the geography problems, but in this case, Signetics is a major US semiconductor firm, and Philips is a major European one. Ferranti lacks this type of support in the US. If the majority of the US array manufacturers continue to treat gate arrays as a service intensive business, they may make it very difficult for Ferranti to compete.

Fujitsu Microelectronics

Many Japanese companies have been active in gate arrays for some time. Fujitsu recently announced an 8000 gate CMOS array—one of the most complex available. Four others, ranging from about 700 to 4000 gates with 7 ns gate delays, and 2000 and 4000 gate CMOS arrays with 4 ns delays, were already available in 2 level metal CMOS. Fujitsu also has 3 TTL gate arrays. The CMOS arrays compete with low-power Schottky TTL with lower power requirements.

Six I/O cell options and an 86 cell macro library are available to design these arrays. Fujitsu is willing to interface at the logic diagram level or in a logic description language; the company provides software and CAD support to its customers.

International Microcircuits

An old timer in the gate array business, International Microcircuits Inc., began producing arrays in 1974, calling their approach "Master Slice." In 1976, they developed a medium speed family of CMOS arrays with over 500 gates. By 1978, IMI added linear arrays, and today they are capable of producing metal gate CMOS arrays with more than 5000 gates.

Frank Deverse, IMI's President, feels that offering service to the customer is still the key to the business, and to do this, he is attempting to cut cycle time from valid logic design to prototype arrays in silicon to 3 weeks by the end of this year. Deverse is a firm believer in CAD and thinks it may offer the only error-free method of converting logic into arrays. Another key to the future is a guarantee from the array manufacturer of quality, and to get there, Deverse feels that a successful array company today must own its own wafer fabrication line. "Kitchen table" array designers may disappear when you consider the $15 to $30 million needed to invest in a full wafer fab facility today.

At IMI, the philosophy is fairly simple—they hope to help their customer manage the risks of a

semi-custom array design. To accomplish this, they depend extensively on CAD systems from Daisy Systems and software provided by Silvar-Lisco. With more than 600 designs completed, IMI seems very well qualified to predict the future of the array business depending on service, CAD, and full wafer fab facilities.

Interestingly enough, as a by-product of IMI's array experience, they have found it practical to develop a family of array-based standard products. IMI now offers direct Si Gate CMOS replacements for the complete line of TRW high-speed bipolar multipliers with performances very close to the bipolar devices. This line of TRW devices has lacked a real second for some time, and now IMI offers not only direct replacements but lower power (50 μW vs. several watts for the TRW 8×8 multiplier) CMOS versions. This was more of a target of opportunity for IMI than a trend toward turning out standard products based on gate arrays.

Frank Deverse finds that the major problems facing the array producers today are improving the CAD software from bits and pieces into a total design solution, and creating better testing data. He places the greatest emphasis on service and feels that IMI must take full responsibility for converting a design into silicon.

IMI offers arrays in Standard Metal Gate CMOS and oxide isolated CMOS technology and have delivered arrays with a complexity of 5100 gates **(Table 3)**. They use a hard macro cell design approach.

Description	Number of Cells
1. Triple 4 i/p NAND	2
2. Dual 4 i/p NAND, single 3 i/p NAND	3
3. Triple 4/2 OR-NAND	2
4. Triple 2 i/p NAND	1
5. Dual 3 i/p NAND	1
6. 4/2 AND-NOR + single inverter	1
7. 4/2 OR NAND, or AND + inverter	1
8. Quad inverter	1
9. Triple 2 i/p NAND with complement	2
10. Triple 2 i/p NOR latch	2
11. 2:1 MUX	1
12. Triple clock buffer	1
13. Dual NAND latch + single 2 i/p NAND	1
14. 4 i/p NOR	1
15. Dual TRI-STATE®	2
16. Triple 2 i/p NOR	1
17. Triple 3 i/p NOR with complement	2
18. D flip-flop with set and reset	3
19. D flip-flop	2
20. D flow-through latch	1
21. Dual 3 i/p NOR	1
22. Triple 2 i/p NOR with complement	2

Table 7: National Semiconductor's SLX 6324: typical functions available.

LSI Logic

Founded in January, 1981, LSI Logic is headed by Wilfred J. (Will) Carrigan, who ran Fairchild Semiconductor from 1974 to 1979. LSI Logic is perhaps one of the best funded start-up companies to enter the array market. LSI Logic offers both ECL and CMOS arrays **(Table 4)**. No other products are being offered.

LSI Logic has a very automated design process supported by an Amdahl computer and extensive CAD software. They do prefer that their customers perform their design at their facility in Milpitas, CA. The user is first put through a training program in LSI Logic's design procedure. During the training and subsequent design, they also assign an applications engineer to work with the customer on a full-time basis. The training and design cycle can be as short as three weeks for a silicon prototype.

LSI Logic is now offering a cell library of 150 macro primitives for its CMOS products, and the customer is also able to create his own unique macros on the CAD system. They also use extensive color graphics editing during the design and simulation process to correct errors. A "Gate-Eater" is built into the design program to drop out unused macros.

Rob Walker, vice president of engineering at LSI Logic, is very optimistic about the future of gate arrays. He pegs the market at near $1.5 billion by 1985. Walker is also outspoken on some things that the array manufacturers need to do to make it happen in an orderly fashion. Walker cites these key needs:

(1) Standardization of interfaces and specifications for arrays

(2) High level design language

(3) Electronic breadboarding

(4) Suppliers must remain service-oriented and get better

(5) Education and training of users must get better

(6) Documentation must be improved.

LSI Logic uses their own array development system for arrays called LDS-1 for LSI development system 1. It is used for logic simulation, design verification, test pattern generation, layout and mask design. Combined with the TEGAS simulation and partitioning software, this system is able to turn around complex designs in a few weeks **(Figure 1)**.

Dr. Donald Soderman, applications engineering manager at LSI Logic, feels that the main advantage of their design system is that the user has an opportunity to completely verify the logic function of the array before it is built. Although LSI Logic prefers customers to use its design facility, they also are willing to work with customers using their own CAD systems. LSI Logic also has a remote design terminal available (very similar to the Motorola offering) for installation at the customer site, and as another option, they are willing to install a turnkey LDS-1 development system in your facility.

Mitel Semiconductor

This Canadian semiconductor firm is doing some interesting ISO–CMOS array designs that can be used for random logic and μP bus oriented designs as well as performing simple analog/linear functions. Mitel uses a transistor cell design that permits dynamic or static logic and the use of transmission gates. By using the switching characteristics of the CMOS transistors, a simple comparator can be constructed with on-chip capacitor

A

Products	Gates	I/O's	Availability
ACE 600	600	58	Now
ACE 900	900	70	Now
ACE 1400	1400	91	Now
ACE 2200	2200	120	Now
ACE 1320M*	1000	90	Mid-'83

*320 bits of RAM included, configurable as A x B, where A x B = 320.

B

Products	Gates	I/O's	Typ. Gate Delay
8A1200	1144	36	4 ns
8A1260	1144	60	4 ns
8A1542	1408	42	4 ns

Table 8: (a) Signetics Advanced Customized ECL (ACE); (b) Integrated Schottky logic gate arrays.

and resistor arrays to form simple operational amplifiers that can be used as A/D conversion or for analog interface. Three CMOS arrays are available from Mitel **(Table 5).**

Motorola Semiconductor

Producing gate arrays since the early 1970's, Motorola has a great deal of design experience in both bipolar and CMOS arrays. Motorola pioneered the hard macrocell (data book specified array macrocells) approach and has been a leading advocate of customer interface throughout the design via their vast Western Area Computer Center in Phoenix.

Motorola has also led the way in establishing remote design centers in the US and Europe. Eventually, Motorola expects to be able to offer remote design facilities in over 100 regional sales offices in the US. Today, most Motorola customers have access to their computer center via the GTE Telenet system available in 200 or more cities, that provides local access via the error corrected data network. During 1982, Motorola expects to cut its development cycle time from 9 to 7 weeks, and by early 1983 to an average of 5 weeks. Shorter development turnaround is possible, but there is an extra charge. **(Figure 2)**

Motorola Products:

MCA 500 ALS: up to 533 gates; 77 cells (24 major, 26 input, 27 output); 75 Macros in cell library; basic gate delay 2.5 ns typical; power 1.1W; technology-series gated ECL internal with TTL translators, LSTTL compatible.

MCA 1300 ECL: up to 1192 gates; 106 cells (48 major, 32 interface, 26 output); 109 Macros in cell library; basic gate delay 0.8 ns typical; power 4W; technology-series gated ECL MECL 10K compatible.

MCA 1200 ECL: up to 1192 gates; 106 cells (48 major, 32 interface, 26 output); 109 Macros in cell library; basic gate delay 0.8 ns typical; power 4W; technology-series gated ECL MECL 10K compatible.

MCA 1300 ALS: 1280 gates; 140 cells (60 major, 40 input, 40 output); 75 Macros in cell library; basic gate delay 2.25 ns typical; power 1.6W; technology-series gated ECL internal with TTL translators, LSTTL compatible.

MCA 2500 ECL: 2720 gates; 178 cells (100 major, 68 output, no specialized interface); 44 Micros defined; basic gate speed 300 pS: power not specified; technology-series gated ECL 10KH and 100K ECL level compatible (new product).

Planned Products:

MCA 1000 RECL: 512-bit register file on a chip with up to 1000 customizable peripheral gate cells, same macro library as MCA 2500 ECL. Scheduled for First Quarter 1983 release.

MCA 2800 ALS: 130 major cells; up to 2800 equivalent gates with 120 I/O parts. Scheduled for First Quarter 1983 release.

In addition to these bipolar products, Motorola is also producing 1200 and 6000 gate products in silicon-gate CMOS.

National Semiconductor

National, like many other array houses, is betting on CMOS and ECL dominating the array market. Denny Sabo, National's gate array marketing director, hopes to see dual metal-oxide isolated CMOS devices with 1 ns gate delays by the end of 1982 with 2μ geometry products. National departs somewhat from the main body of array suppliers by insisting that its customers provide CAD compatible inputs. National is not willing to accept designs that are simply at the partitioned logic level because they feel that most of their customers want to interface directly at the CAD level.

National is planning a worldwide network of CAD centers with Santa Clara, Munich, and London now in operation. Boston will be added in the very near future, followed by 6 to 8 other regional centers in the US. For larger customers, National will also provide a portable CAD system for installation at the customer's site. These systems range from a simple B&W graphic entry system for $18K. Adding a printer and plotter moves the price up to about $30K, while a full color graphics system with editing costs $75,000 when purchased from CDC.

An average 4- to 6-week turnaround is claimed by National using the design system with the customer entering and simulating the array design. An added 8 weeks or more is required for NSC to route and place the array and to check the simulation. Shorter turnaround can be arranged at higher cost (Motorola offers a similar extra charge to shave turnaround.)

Hard macro cells are used in National's ECL arrays consisting of a library of 41 cells. NSC also offers a soft macro option to build macro cells into higher order functions us-

ing a software route and place technique.

These higher order functions have an upper limit of 100 gates. For example, a CMOS 4006 device can be duplicated on an array using 100 gates or 20 macro cells. A 74157 can be created using 20 gates or about 5 macros, and many other standard TTL and CMOS functions can be reproduced in a similar fashion. (Products are shown in **Table 6**).

The SLX 6324 is a high speed 2.4K gate, Si gate CMOS array. The array itself is composed of 795 cells organized in 15 columns, 53 cells deep. The sample library provided in **Table 7** defines the basic functions available now. The library will be extended to 80-100 functions in the near future. In addition, any functions essential to the user and *not* available in the listings (when required) can be readily incorporated.

In addition to this listing, "software functions" will be provided; i.e. various denominations of counters, shift registers, arithmetic logic, etc.

The user may typically utilize up to 80% of the cells to create any option. As the number of cells per basic function is provided, the user may readily interpret the total utilization of the array for his logic configuration.

Signetics/Philips

Signetics has been in the bipolar array business since 1978 combined with its parent company, N.V. Philips. At present, Signetics supplies ECL and Integrated Schottky Logic arrays up to 2100 gate complexities, and by the end of 1982 they will complete the introduction of four new Silicon Gate CMOS arrays ranging from 250 to 1800 gates.

Herb Jesse, bipolar arrays marketing manager at Signetics, sees savings to the systems house averaging 60% or more using gate arrays. Jesse goes way out, placing the market for arrays at $7 billion by the end of this decade.

Signetics has a well defined customer interface program beginning with the customer defining his product and producing a basic logic diagram (typically in series 7400 logic functions). Three or four days of customer training are provided at the Signetics plant in Sunnyvale, CA where the customer learns how to implement the logic and do simulation with Signetics' supplied software. At this point, the customer may elect to use the Signetics IBM 3033 computer or his own system, which can be as simple as a TI Silent 700 terminal connected to the Signetics computer via GTE Tele-Net. Signetics prefers the customer to use the logic simulation to verify logic performance. They have a logic check program called LOCKER.

Type	Gates	Gate Delay	
TAT004	540	2.5 ns	4 micron
TAT008	1080	2.5 ns	
TAT010	1260	1 ns	2 micron
TAT020	2420	1 ns	
TAL002	320	5 ns	Low-power
TAL004	500	5 ns	Schottky TTL

Table 9: TI Advanced Schottky Transistor Logic.

Once the simulation has been completed, either the customer or Signetics can do the automatic place and route on a Calma system. If the customer prefers, he has the option of doing manual interconnect of both levels of metal at this point. For arrays under 1000 gates, manual interconnect is feasible; above 1000, it gets very difficult. Customers electing to do their own routing can make substantial savings.

Numerous CAD checks are built into the Signetics design system. TEGAS is the basic design program, but it is supplemented with a program called GASPAR that checks for design rule violations. The LATCH program matches chip layout with the simulation to make sure logic has not changed. Actual wire delays are measured by the WIGIT program and are used to update the simulation to provide exact AC performance parameters. Another program, SENGEN, generates test tapes for a Fairchild SENTRY tester.

All this can happen in as little as 8 weeks; however, Herb Jesse cautions the first-time array designer to allow much more time until first samples are delivered. Development costs can range from $16K to $40K, and the high number is most likely for a first design. Of course, the development cost can be amortized over the production volume.

Most of the arrays offered by Signetics are being produced by Philips in Europe. The ECL and ISL arrays are actually manufactured by RTC, a Philips subsidiary in France. CMOS wafers are being fabricated in Germany and metalized by Signetics US. All Signetics CAD is performed in Sunnyvale. There is little doubt that Signetics/Philips can mass produce and inventory the same uncommitted logic arrays around the world and produce the finished product in every country.

Designs at Signetics are accomplished via the hard macro approach using the double level metal. Signetics also offers a variation called "Composite Cell" Logic similar to the macro cell approach based on 7400 series TTL functions. Up to 200 cells are available, and total gate count is under 500. This Composite Cell approach is aimed at lower complexity 100 to 200 gate applications and offers a variable chip size depending on the number of cells used. It may be more efficient for implementing smaller functions, but it costs more since the entire process is customized, requiring more masks, etc. The design cycle is about the same as a full gate array, but turnaround is also longer since each design starts with a blank wafer.

Signetics 700 Family Silicon Gate CMOS:

Silicon gate CMOS is just being

Designation	Chip Size	Gate Count	Bonding Pads	Tpd	Toggle Rate	Proto Cost*
ISO-6A	118x140	360	44	3ns	30MHz	$ 6,500
ISO-6B	132x167	540	58	3ns	30MHz	$ 8,200
ISO-6C	159x167	720	64	3ns	30MHz	$ 9,500
ISO-6D	161x208	960	70	3ns	30MHz	$12,000
ISO-6E	188x208	1200	74	3ns	30MHz	$16,000
ISO-6F	188x244	1500	80	3ns	30MHz	$18,000
ISO-3A	118x140	360	44	1ns	75MHz	$ 8,800
ISO-3B	132x167	540	58	1ns	75MHz	$11,000
ISO-3C	159x167	720	64	1ns	75MHz	$12,800
ISO-3D	161x208	960	70	1ns	75MHz	$16,200
ISO-3E	188x208	1200	74	1ns	75MHz	$21,500
ISO-3F	188x244	1500	80	1ns	75MHz	$24,500

*Universal is one of the few array companies to publish its prototype costs. The prices shown are for customer supplied layout.

Table 10: Universal Semiconductor ISO 3/6 family of high speed CMOS gate arrays.

introduced by Signetics, and it will consist initially of 450 and 1100 gate products. By year end, 250 and 1800 gate arrays will be added. These arrays use the same oxide isolated CMOS process as the Signetics 4000 series LOCMOS. Gate delays range from 5 to 15 ns, but process improvements and smaller geometrics will reduce delays to the 2.5 to 8 ns range by the end of the year (product range is shown in **Table 8**).

Texas Instruments

TI, of course, claims to have originated the concept of logic arrays back in the early 1960's, and they have several basic patents to prove it. One granted to Jack S. Killy, (the co-inventor of the integrated circuit) in 1972, describes the computer-aided interconnection of a matrix of logic cells. However, with all of this background, TI has only managed to announce six arrays, with the two most recently announced arrays being only 320 and 500 gate, low power Schottky TTL.

TI uses both junction isolated (4μ) and oxide isolated (2μ) Schottky TTL for its arrays. TI customers are required only to describe their LSI array requirements in two high-level structured design languages provided by TI—HDL and TDL. HDL (Hardware Description Language) permits a behavorial as well as structural description of the designer's logic function. In addition, predesigned software functions are available to implement over 70 standard digital IC's. TDL (Test Description Language) is used to describe the required input stimuli and output response characteristics of the desired custom function to develop test programs.

Design support is available from the TI Houston facility and from five TI Regional Technology Centers located in Boston, Chicago, Atlanta, and northern and southern California. Additional design support is provided by pre-defined functions that are equivalent to many standard low-power Schottky TTL functions. The soft macro library also has new functions which take advantage of unique features of ASTL and STL technology. The HDL macro library facilitates conversion from standard low-to-moderate complexity functions to achieve a specific LSI array system implementation.

TI, like Signetics and Motorola, has a vested interest in the discrete TTL and CMOS SSI/MSI market which may be severely impacted by gate arrays. All of these companies are producing arrays to minimize their future risks. Motorola has taken the most aggressive position, followed closely by Signetics. It is almost certain that TI has some very big designs on the array market very soon. The products announced so far may just be TI's beachhead in arrays to buy time to develop a more comprehensive product line (**Table 9**). It is doubtful that a company like TI will ignore CMOS arrays.

Universal Semiconductor

Founded in late 1979, Universal Semiconductor has been producing metal gate CMOS arrays since early 1980. Like many of the newer companies dedicated to only the gate array business, Universal has its own 4″ wafer fab facility. George Stephan, Universal's president, firmly believes that the gate array business will remain a service-oriented business and that customer participation throughout the design process is critical. Stephan admits that the level of participation is variable, but more is better on the customer's part.

USI has one of the most complete design manuals available to lead the user through the design process. Universal is also one of the most flexible companies in terms of what type of input they will accept and in how the customer participates in the design process. Every approach is offered from color pencils and mylar overlays through the most sophisticated CAD system entry levels. Stephan also points out that a customer willing to do more of the design on his own can save money on the tooling costs.

Universal has also produced arrays using Si Gate NMOS for game applications, but today its product line consists of Si Gate and Metal Gate CMOS products ranging from 360 to 1800 gates with both 3μ and 5μ channels (**Table 10**). Their hard macro library consists of about 100 defined macro functions.

George Stephan doubts that any competent company in the array business can avoid being successful. One of the main problems that Stephan sees relates to the education of customers to accept the fact that they can really do their systems in silicon. □

High Graphics Performance Through Multiprocessor Architecture

The multiprocessor architecture of Florida Computer Graphics' Beacon system was developed to meet the performance needs for an interactive color graphics workstation in current and future applications, now only vaguely defined. The primary need was for high-performance graphics that could be easily merged with data and word processing applications. From the user's point-of-view, the performance goal was a system that could paint a high resolution (640x480) color screen with graphics intermixed with text in nearly the same amount of time that an ordinary 1920-character terminal screen could be painted.

This performance goal was met with the system design shown in **Figure 1**, which uses a Z80A administrative processor (AP), a 16-bit bit-slice graphics processor, and intelligent disk controllers. Other μPs control the keyboard and the function keys along the bezel of the display.

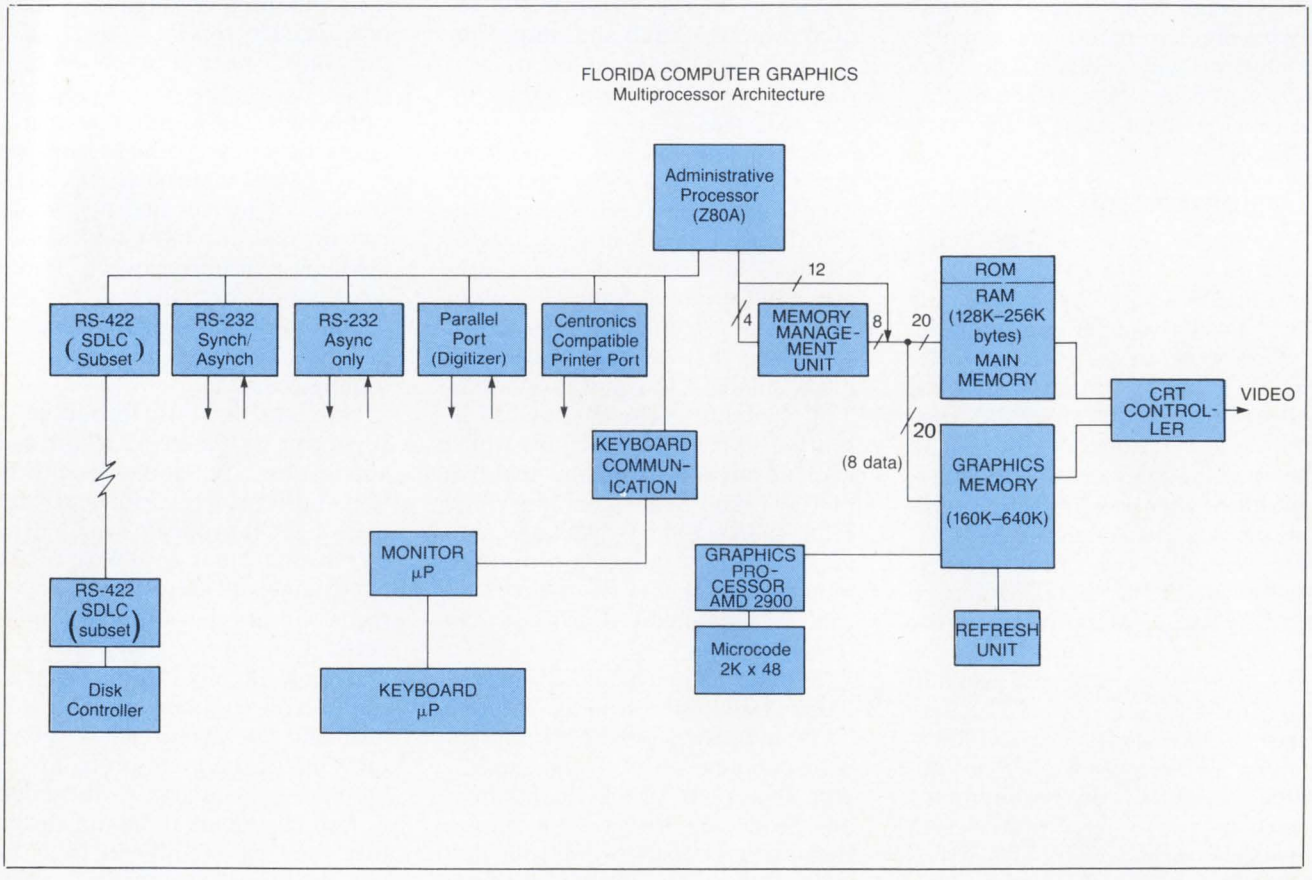
A single processor design was determined to lack the graphics performance needed by the envisioned applications. Two bottlenecks limit the performance of single processor designs. The first is the computational horsepower that is needed when graphics generation is performed by software. The second is processor involvement in I/O operations, which is especially severe with floppy diskettes.

The multiprocessor approach solves these two problems. The increase in computational power for graphics may be quickly demonstrated: 8-bit commands in the Z80 take from 4 to 21 cycles to execute—that is, roughly between 1 and 6 ns per command. Floating point operations and algorithm-based graphics functions are even slower. A faster 16-bit administrative processor performing graphics may reduce the time required, but not sufficiently. The dedicated graphics processor, on the other hand, executes a 48-bit microcoded command in 200 ns. With a complex algorithm such as the one controlling area fills, the performance advantage of the graphics processor may exceed one hundredfold.

Architecture

The administrative processor was chosen for its speed and effi-

Figure 1: The multiprocessor architecture of Florida Computer Graphics' Beacon system includes a Z80A administrative processor, a 16-bit bit-slice graphics processor, intelligent disk controllers, plus other μPs to control the keyboard and function keys.



ciency, its well-developed command set, and the availability of the CP/M operating system and other software. Other processors were considered and eliminated by lack of software or support chips, or by complexity beyond that required by the application.

The administrative processor is configured with 128K RAM, expandable to 256K RAM, and supports two RS-232 ports (one asynchronous, one asynch or synchronous), a Centronics-compatible parallel port, a parallel port for digitizers or other parallel I/O devices, and an RS422 port supporting a subset of the SDLC protocol, which is presently used for I/O to disks.

The graphics processor is based on AMD 2900-series components to form a 16-bit bit-slice processor controlled by 48-bit microcode. The 48-bit microcode allows a number of operations to be executed simultaneously in a 200 ns cycle. Specific instructions for drawing vectors, arcs, rectangles, and polygon fills, as well as mathematics operations are microcoded.

A memory management unit uses the highest 4 bits of an address to enter a 16 x 8 sector lookup table. The 8-bit result is concatenated with the lowest 12 bits to form a 20-bit physical address space, divided as 256 4096-byte sectors.

The administrative processor communicates with the graphics processor through memory. When the AP encounters a graphics command, it passes the command and all associated parameters to graphics memory. The Z80A performs range checking and other validation checks on the parameters. The graphics processor polls a command register in graphics memory and, upon finding a command, begins to decode and execute it. Floating point arithmetic and integer multiply/divide operations are similarly passed and executed. The graphics processor informs the administrative processor when it has completed execution through either a status register or by sending an interrupt.

Graphics memory may be accessed by the AP, the graphics processor, the CRT controller, and a refresh unit. Graphics memory is arranged as 640 x 480 x 5-bit pixels, expandable to 1280 x 960 x 5; or, when used by the AP, as 160 Kbytes RAM plus parity, expandable to 640 Kbytes plus parity. There are 100 16K or 64K RAM chips, which are read broadside, yielding 100 bits/read. The CRT controller gets at least every other memory cycle. A separate refresh unit relieves the graphics processor of refresh duties, thus maintaining performance. The design allows the administrative processor to access the graphics memory plus its own memory, which yields up to 896 Kbytes for very large applications. The instruction loops for the graphics processor were optimized for the every-other-cycle availability of memory.

To eliminate another bottleneck— disk transfers—the Beacon's disk controller is an intelligent device based on a Z80A with 16 Kbytes memory. Serial I/O (SIO) and Direct Memory Access (DMA) chips in the controller and the administrative processor establish transfers with minimum administrative processor involvement. The AP places disk commands and parameters into memory. The SIO chips establish the transfers, and the DMA chips establish addresses.

The intelligence in the disk controller aids in disk reliability and can greatly speed disk transfers. Reliability is enhanced by fast and easily variable disk error retry procedures, and by an error logging facility that can be used to build a record of error messages in main memory. Speed is enhanced by lookahead buffering which reads additional sectors of disk into the controller memory, greatly speeding accesses when the next disk operation is sequential, as in program loading.

The line is a high speed RS422 line, with communications formatted according to a subset of the SDLC protocol. This differentially-driven communications was chosen for applications requiring sizeable distances between stations, and the synchronous transmission decreases the overhead of the AP.

Modular Design

The Beacon's multiprocessor architecture was designed so that future growth in performance could be easily achieved. The administrative processor by itself can function as a color graphics computer, albeit much more slowly than with the graphics processor. The intelligent disk controllers are also complete microcomputer systems. The system designers were free to choose all processors according to their suitability for their specific tasks.

John B. Cottrill, VP R&D
and Joseph D. Lamm,
Principal Engineer,
Florida Computer Graphics.

Write 197

Digital Design Launches Graphics Column

In this issue, Digital Design inaugurates a new section: **Graphics System Design**. Graphics System Design focuses on problems encountered by system designers attempting to evaluate and then integrate graphics hardware and software products. In addition, the column examines some of the design philosophies behind various products, how these approaches affect the end product, and what this means to the system designer.

Simultaneously, the subject of compatibility, covered by Compat Design, the column formerly occupying these pages, has outgrown its space. As a result, we're devoting a special 13th issue to the subject. The Computer Compatible Directory, available in October, features articles and directory listings aimed at the compatibility problems encountered by system designers integrating products from a variety of manufacturers.

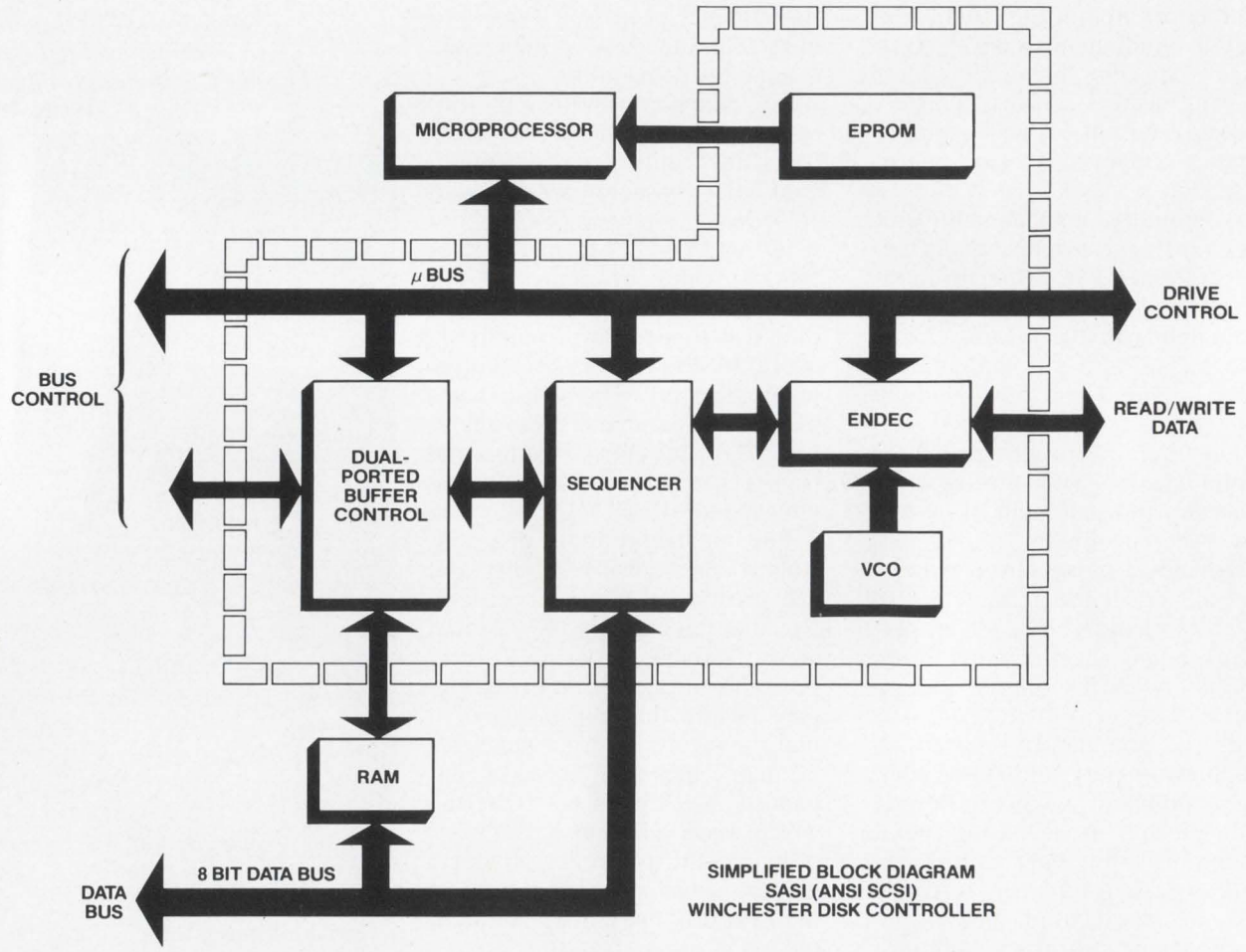
Winchester Controller Designed for Multitasking Systems

Enhanced Winchester disk drive performance and capacities have helped enlarge the application of μCs from single-user, single function systems to multi-user, multi-function systems. With Adaptec's announcement of the ACS-500, a set of 5 LSI devices, the ACB-2000 series of controller boards and a Winchester controller chip, the company is offering the support of multi-tasking operating systems required by these advanced applications.

The ACS-500 5-chip set includes four proprietary LSI devices and an EPROM containing the microcode for operation of the four proprietary chips in a SASI bus environment. The four proprietary chips include all control and data handling functions for Winchester drives and are divided into logical blocks, including the encode-decode function for MFM; sequence and serialization/deserialization; voltage controlled oscillator; and a dual-ported buffer control which allows a FIFO-type multi-sector buffering.

The ACS-500 chip set is designed for high performance drive and system manufacturers who desire to lower their recurring costs by manufacturing their own boards. Adaptec will provide these volume manufacturers PCB design and manufacturing information along with a manufacturing license. Adaptec says a complete board can be manufactured using the 5-chip set with the addition of only one 8085 and 22 low cost, off-the-shelf chips. The chip set is priced at $190 in quantity 1000. Complete Adaptec-manufactured controller boards can be purchased for $350 in quantity 500. Both products will be available for evaluation at the end of September.

Adaptec, 1625 McCarthy Blvd., Milpitas, CA 95035. **Write 198**



SIMPLIFIED BLOCK DIAGRAM
SASI (ANSI SCSI)
WINCHESTER DISK CONTROLLER

The following are some of the New Products that may be seen at Wescon '82, September 14–16 in Anaheim, CA.

MINIATURE SWITCHES

Wave Solderable Units

Mr. Clean II is a wave solderable, contamination-free, miniature slide switch. It features: 2-piece assembly; eliminates solder flux and cleaning residue problems; insert molded base; gold contacts for reliability; standard configurations include SPST, SPDT, DPST, DPDT and Form "Z"; and is compatible with fluorinated, chlorinated and aqueous cleaning methods. $.62 ea. in 1000 qty in SPST version. **Chicago Switch Inc,** A Subsidiary of Illinois Tool Works Inc, 1714 N. Damen Ave, Chicago, IL 60647. **Write 128**

LCD's

80, 160 And 320 Characters

The Intelligent Modules EA-Y80015AT, EA-Y80025AT and EA-Y80040AT feature 80, 160, and 320 characters (1 line × 80 char/line, 2 lines × 80 char/line and 4 lines × 80 char/line respectively) in 5×7 dot matrix formats with cursor. They feature character heights of 0.133" (less cursor) and display up to 96 ASCII characters which are contained in the "on-board Character Generator." In addition to its row and columns drivers, other on-board features include Data RAM and Display Data Controller. **Epson America Inc,** 3415 Kashiwa St, Torrance, CA 90505. **Write 129**

PULSE GENERATOR

Dual Channel and Summing Options

Model 2021 is a single channel, 20V p-p, 50 MHz pulse generator with variable rise/fall (transition) times from 5 ns. Model 2021DS is a dual channel, summing pulse generator. In summing mode, the 2021DS can deliver a 40V p-p output pulse. Standard features include "Autocal" continuous automatic calibration of frequency, voltage levels, delay and width. Other features are user-friendly controls and display and IEEE 488 interface for remote control and readout. The 2021's memory can hold up to 10 store/recall messages or complete settings for a particular pulse signal. The 2021DS provides a second output channel with independently programmable voltage levels, output impedance, waveform, delay width, duty cycle and transition times. **Interstate Electronics Corp,** Signal Source Operations, 1001 E. Ball Rd, PO Box 3117, Anaheim, CA 92803. **Write 130**

EPROM PROGRAMMER

Multi-Master Production

The IM3016 can program up to 16 different EPROM images at one time. Multi-Master programming allows manufacturing and development engineers to create in one operation the entire set of PROMs used in their computer products. When EPROMs used for micro-computer memory are programmed in sets as opposed to multiple copies of one master, the programming time, EPROM inventory requirements and personnel handling can be significantly reduced from that needed by a universal or gang PROM Programmer. Complete system prices with one module start at $6900. **International Microsystems Inc,** 11554 C Ave, Auburn, CA 95603. **Write 131**

SWITCHES

Lighted Manual Pushbutton Units

The Series 50 lighted manual pushbutton switches offer a choice of solid state or mechanical pushbutton control switches and matching indicators. Available with LED, incandescent, non-illuminated, and a selection of 8 colors, 3 different display methods and custom legending to provide complete display flexibility. **Licon,** Div. of Illinois Tool Works Inc, 6615 W. Irving Park Rd, Chicago, IL 60634. **Write 132**

ANALOG MULTIPLEXER

Operates With 300V CMV

With 12 input ranges from 5mV to 10.24V (f-s), the Series 430 features 0.05% accuracy, sample rate to 200 channels/sec and includes a two-pole, passive R-C filter on each channel for noise rejection. Other components include a programmable gain amplifier, 12 or 14-bit ADC, I/O interface and associated control logic. The computer can sample input channels in sequence or at random. Channel capacity is established by the number of 16-channel multiplexer cards installed, up to 16 per assembly. From $6800 for 16 channels. **Neff Instrument Corp,** 700 S. Myrtle Ave, Monrovia, CA 91016. **Write 133**

ROTARY SWITCHES

Sealed Against Contaminants

The series 500 are sealed ½" diameter rotary switches that surpass military communications requirements (MIL-S-3786) as well as the demand for high reliability in civilian communications systems. The Series 850 switches are only 0.850 in. sq. In addition to being sealed against wave soldering contaminants and solvents, they feature a life expectancy of 50,000 cycles (minimum) and resistance to shock and vibration. Also available is an 81-position FTM keyboard that combines the price and reliability of membrane keyboards with the industry standard, human engineered feel and touch of a full-travel key design. **Oak Switch Systems Inc,** PO Box 517, Crystal Lake, IL 60014. **Write 134**

POWER SUPPLY

Regulates Switcher Output Voltage

The EVD-65 Series multiple output switching regulated power supply incorporates a control reactor and programmable zener to regulate output voltage, thereby eliminating the traditional control chip. Input EMI filtering meets FCC 20780 Class B and VDE 0871/6.78 Level B. The series provides 65W of continuous output power and up to 90W peak power. DC outputs are +5V @ 6A, +12V @ 2.0A and −12V @ 1.0A. They can also be customized to produce various output power ratings within their maximum continuous output. $159 (1–10). **Power/Mate Corp,** 514 S. River St, Hackensack, NJ 07601. **Write 135**

DIGITAL MULTIMETER

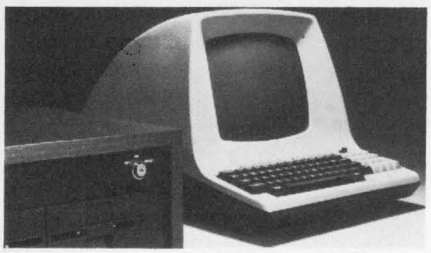
With Bus Interface

As a Talker, the 6500B can send measurement data, including function and range information, over the standard IEEE-488 bus. It can interrupt the controller using SRQ when a measurement is complete. It is also capable of reporting status information via a Serial or Parallel Poll. As a Listener, the 6500B can be triggered by the controller for single measurements, or measurements can be made on a timed basis. In addition, the LCD display can be commanded by the controller to display numbers or individual segments for status messages. Average sensing Model 6502B, $905; RMS sensing Model 6504B, $925. **Weston Instruments,** 614 Frelinghuysen Ave, Newark, NJ 07114. **Write 138**

MICRO PACKAGES

Includes A Quay Desk-Top μC, Conversational Terminal And Cabling

Applications for the 3 packages include data collection, word processing, accounting and planning functions. The Model 500T system includes a Quay Model 500 μC with 64 Kbytes of dynamic RAM and a CP/M 2.2 disk operating system with Quay utilities. It has serial and parallel line printer ports and two 5¼" floppy disk



drives providing 400 Kbytes of storage capacity. Model 520T has two double-sided, double-density drives for 800 Kbytes of storage. The 1.6 Mbyte system is the Model 540T package. The conversational terminal has an 80-character × 24-line display format. **Quay Corp,** 527 Industrial Way W., Eatontown, NJ 07724.

Write 149

CP/M SOFTWARE

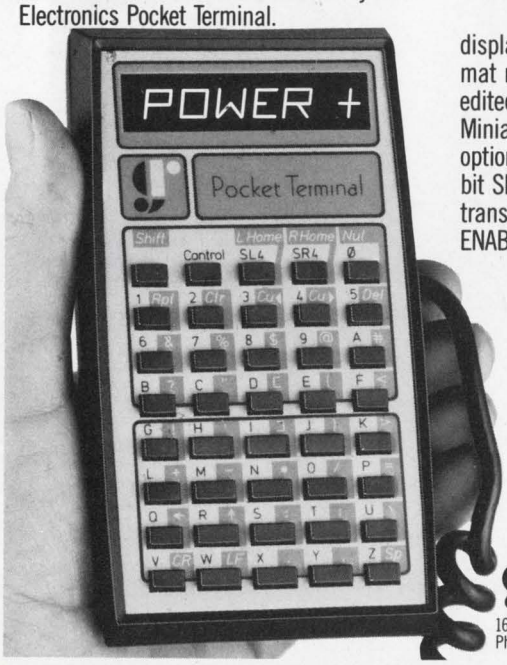
Series Of Housekeeping Programs In One Package

CPM POWER is a series of 45 user friendly housekeeping CP/M programs in one 12k package. They range from a menu function to save you from typing mistakes to the most sophisticated monitor available for a μC. Users can transfer files without typing file names, the computer does it. Files are selected by number from a screen menu, erase and type out files to screen or printer, and run programs from the same numbered menu. It also allows errors to be corrected with a reclaim function that restores accidentally erased files. A disk test function salvages glitched or flakey disks by gathering bad sectors into a special invisible file. Available in all disk formats at $149. **Computing!,** 2519 Greenwich, San Francisco, CA 94123.

Write 141

A Smaller Alternative.

Need a quick, easy way to talk to a computer? Here's a hand-held, fully portable computer terminal that gives instant access to any ASCII transmitting data system with an RS232 interface. It's the revolutionary G.R. Electronics Pocket Terminal.



The silent, solid-state terminal has a 40-key, positive click-response keyboard. From its 32-character internal memory it displays eight bright 16-segment LED characters through a one-line window.

You may select from two alternate display modes. Entries may be in any format required, and all memory data can be edited as desired.

Miniature switches allow selection of these options • Single or dual stop bits • Parity bit SET/RESET/EVEN/ODD • 300/110 baud transmission rates • Control code response ENABLE/DISABLE.

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GR Electronics

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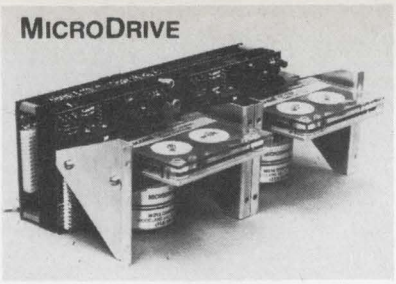
MICRODRIVE



DC100 CARTRIDGE DRIVE HAS SMART I/O

MicroDrive/OEM now features a micro processor based I/O. This unit performs all control and formatting for quick systems integration. A high level command set (22 commands) allows full peripheral status for the model 125I/O. Serial and parallel options are available priced as low as $400 in OEM qty.

MOYA CORPORATION
9001 Oso, Unit B
Chatsworth, Ca. 91311
Tel: (213) 700-1200

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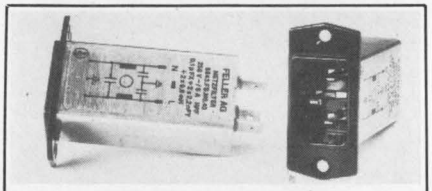

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New international RFI power line filters with integral CEE-22 connectors are recognized, approved, or tested by UL, CSA, SEV, SEMKO, and VDE. Available in 1, 2, 4, and 6 amp configurations, all filters offer common mode attenuation of at least 40 dB from 1-100 MHz. Because they satisfy both European and North American test agencies, these filters may be used interchangeably in equipment made for domestic or export markets. SEE US AT WESCON/82, BOOTH 2251-2257.

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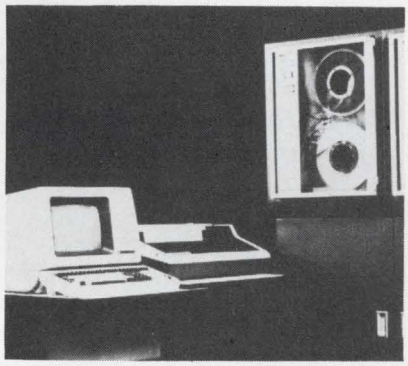
DATA COLLECTION

Multi-Task, Multi-Processor System

The NP9000 collects telephone call records from remote locations and stores the information on two magnetic tapes at a central point. Each tape will store up to 435,000 call records. Designed for sophisticated telecommunication and data network applications, the NP9000 provides centralized collection of the station message detail record (SMDR) data, which when processed, enables a telecommunication manager to: track all



phone calls made from every corporate or field location on the basis of usage; optimize the configuration of network facilities; and look for calls that do not appear to be legitimate business calls. **General Dynamics Communications Co.,** 10151 Corporate Sq, St. Louis, MO 63132. **Write 145**

VAX DBMS

User-Friendly System

OMNIBASE is a complete end-user Database Management System for the VAX/VMS family of computers. User-friendliness is achieved with a complete relational model. The Interactive Query Language (IQL) front-end contains direct buffer editing with the user's choice of VAX editor, ability to execute VAX DCL commands from the IQL prompt level, and a sophisticated macro expansion capability for user-defined abbreviated commands. It also interfaces with the VAX Digital Command Language (DCL) and the VAX Forms Management System (FMS); and, includes Embedded Query Language (EQL) preprocessors for both VAX-FORTRAN and VAX-COBOL. The VAX-COBOL preprocessor supports all VAX-COBOL data types including large number (18 decimal digit) representation. **Signal Technology Inc,** 5951 Encina Rd, Goleta, CA 93117. **Write 151**

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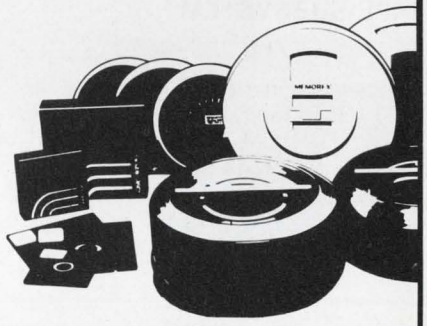
Recording Performance Engineer

Flexible Disc Media Division



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In this position, you will be responsible for defining product performance and evaluating competitive products. Provides technical requirements for development of media equipment, specifications and standards. Assists in design and specification of lab and manufacturing test equipment.

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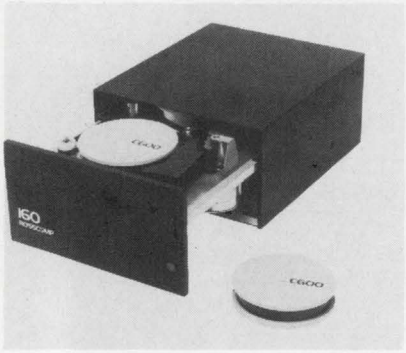
MAGNETIC TAPE SYSTEM

160 Mbytes In 8" Floppy Envelope

The 160's primary applications are as backup for Winchester disk drives, file restructuring, data exchange, data security, and archival storage. Stor-

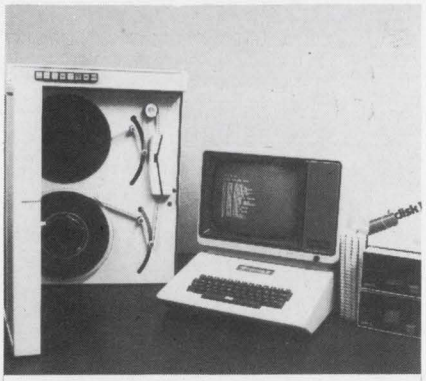


age medium for the drive is selfloading, enclosed 4" diameter reel containing 600' of ½" industry standard computer grade tape. A 300' tape is also available for those users requiring only 80 Mbytes of storage. The 160 has up to 140 Kbytes/sec. transfer rate, 20 min. dump/restore time for 160 Mbytes, start/stop time of 200 ms, soft error rate of 1 in 10^8, hard error rate of 1 in 10^{10}. **Rosscomp Corp.,** José C. Elaydo, 16643 Valley View Ave., Cerritos, CA 90701. **Write 194**

TAPE SUBSYSTEM

For Apple II And III Systems

Configured in a ½" format, the SCDR-1050 tape drive features IBM, ANSI and ECMA compatible hardware and software for Apple's computers. It effectively removes data exchange problems between the Apple and larger systems by standardizing data storage and transfer routines.



Apple users will now be able to communicate with most IBM-compatible large mainframes utilizing 9 track (NRZI 800 cpi and/or 1600 cpi PE) magnetic tape. A typical 2400', 10½" tape reel will accommodate over 40 Mbytes of formatted data for any application, including backup. **Innovative Data Technology,** 4060 Morena Blvd., San Diego, CA 92117.

Write 191

5¼" WINCHESTER

Utilizes ST506 Interface

The WD505 meets the ANSI packaging requirements providing the same dimensions as a standard 5¼" fixed disk Winchester. It is 3¼" high and 5¾" wide with a depth of 8". It utilizes a μP for the following control functions: cartridge insertion and removal control, high speed access control, track location calibration, and drive motor start/stop. The drive is designed to utilize the ST506 interface with no impact to the majority of existing controllers, and also takes advantage of standard power supply inputs. $495 in OEM qty. **Western Dynex Corp.,** 3536 W. Osborn Rd., Phoenix, AZ 85019. **Write 204**

96 TPI DRIVES

Two Flexible Disk Models

The FD 591 (single-sided) and the FD 592 (double-sided), offer an unformatted capacity, respectively, of 250/500 Kbytes and 500 Kbytes/1Mbyte. Average access time is 80 ms and track-to-track access time is 3 ms. They incorporate several innovative features, including a brushless DC motor, a unique split-band head positioning mechanism and a reduced parts count. MTBF is 10,000 hours. The FD 591 is $435, $250 (qty 1000); the FD 592 is $545; $320 (qty 1000). **Olivetti OPE,** 505 White Plains Rd, Tarrytown, NY 10591. **Write 212**

PAPER TAPE READER/PUNCH

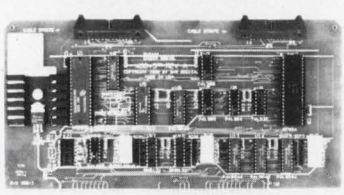
Apple II And TRS-80 Compatible

These parallel interface boards and data handling programs interface a paper tape reader and punch to the Personal Computer. The interface is designed for the Model 600-1 punch and Model 605 reader, and both are interfaced with one board and cable, $90. The Data Handling Program is $115, a 600-1 Punch is $1249, and a

605 Reader is $575. Adds complete paper tape capability to Apple II Plus for under $2100. Applications include numerical control and secure communications systems. Code translation options available. **Addmaster Corp.,** 416 Junipero Serra Dr., San Gabriel, CA 91776. **Write 205**

THE 488+3 IEEE 488 TO S-100 INTERFACE

IEEE-488



S-100

- Handles all IEEE-488 1975/78 functions
- IEEE 696 (S-100) compatible
- MBASIC subroutines supplied; no BIOS mods required
- 3 parallel ports (8255A-5)
- Industrial quality; burned in and tested
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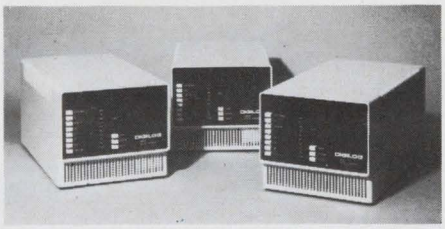
PERIPHERALS

4800 BPS μP MODEMS

For Dial Lines, Point-To-Point Or Multipoint Lines

The new line features state-of-the-art signal processing functions such as scrambling/descrambling, encoding/decoding, filtering, timing recovery, and fast train of 27 ms. Other capabilities include: built in diagnostics with a unique error rate display, B.E.R., alternate dial interface,

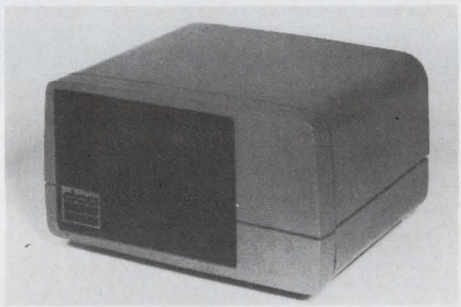


echo protect, data/voice mode, auto/manual answer, front panel interface indicators and optional secondary channel. Three different 4800 bps sync modems provide a variety of special characteristics. **Digilog,** Network Control Div, 1370 Welsh Rd, Montgomeryville, PA 18936. **Write 207**

MULTIPLEXORS/PROCESSORS

Support For Up To 32 Ports

The System 110 is a μP-based statistical multiplexor that can be used in a point-to-point configuration or as a slave unit in a full-function network. It can service both terminals and host computers at either end of the network. The



System 110/4 supports from 2 to 4 ports over a single line; the System 110/8 supports from 2 to 8 ports over a single line. $1495 for a 4-port capacity. The System 120 network processor provides the same features as the System 110, but can support up to 32 ports. It eliminates the need for expensive WATS lines or long-distance service. A basic System 120 starts at $2450 for a 16-port capacity. **Digital Communications Associates Inc,** 303 Technology Park, Norcross, GA 30092. **Write 208**

5¼" DISK DRIVE

Apple Compatible

Super Drive, with enhanced R/W electronics and a track zero microswitch, allows faster and more accurate reading of data while reducing noise level on initial boot. It also reads ½ track software and has a storage capacity of 143,360 bytes when using DOS 3.3. The unit is compatible with most popular operating systems (DOS 3.2.1, DOS 3.3, PASCAL or CP/M). Data integrity standards meet or exceed professional user requirements. $419, dealer and OEM qty. discounts apply. **Fourth Dimension Systems,** 3100 W. Warner Ave, Suite 7, Santa Ana, CA 92704. **Write 209**

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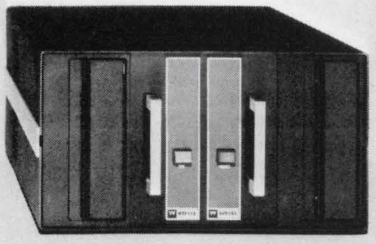
Sprint 68 Microcomputer



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PROGRAMMABLE CONTROLLER

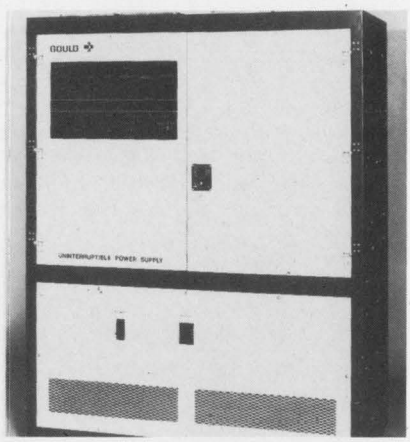
Three Level Architecture

The CY750 programmable controller provides counting, timing, sequencing and monitoring operations in a single 40 pin, 5V package. Designed to add high level intelligence to any computer output port, it allows background counting or timing processes to continue while a stored control program is executing in the on-board program buffer, and even allows live commands to be executed while both of the lower levels are operating. $75 in singles; $45/100; $20/1000. **Cybernetic Micro Systems Inc,** PO Box 3000, San Gregorio, CA 94074. **Write 174**

UPS

Computer Optimized Features In Each Critical Area

The 6000 series includes 4 main elements. The Battery Charger delivers the DC power necessary to drive the inverter and simultaneously charge the battery reservoir. It features a new 12 phase design to minimize input current distortion. The Inverter determines the quality of the AC power output. Its hybrid design combines the best features of the pulse width modulated technology and the step wave technology. The Transfer Switches include both Manual and Static Transfer switches as part of the basic design. The Status Display Panel features high reliability LEDs and digital panel meters which give full operating status at a glance. **Gould Inc,** 2727 Kurtz St, San Diego, CA 92110. **Write 178**



Advertiser Index

Adaptive Science 38
Advanced Electronics Design . . 1
American Automation 40
Applied Analytics 21
Anadex 39
ATE Central 27
Audiotronics 19

Bo-Sherrel 28

Cadcon 81
CalComp 4
Comdex 47
Computer Products 7
Controlled Power C3

Datacube 10
Dataram 29
Design Aids 11
Distributed Computer Systems 31
Dolch C4
D.W. Digital 80
DY4 58

Eaton 16
Electronic Solutions 59
Exatron 17

Florida Computer Graphics . 2, 3

G. R. Electronics 78

Hecon 8
Hettinga 17
Hilevel Technology 33
International Microcircuits 63

Kennedy C2

MDB 9
Memodyne 30
Memorex 79
Micro-Link 35
Modgraph 6
Mouse House—a division of Howly Labs 28
Moya 78
MuSYS 57

Necom '82 31
Nicolet Zeta 42
Novation 41
Numerix 15

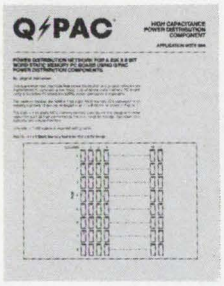
Panel Components 78
Peripherals '82 22
Plessey Peripheral Systems 13
Printer Products 79

Qantex 7

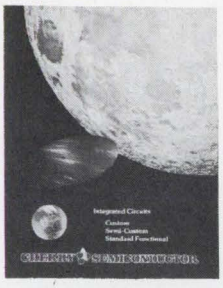
Universal Semiconductor 37

Wintek 82

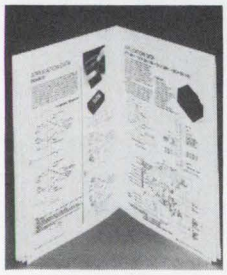
Zendex 43



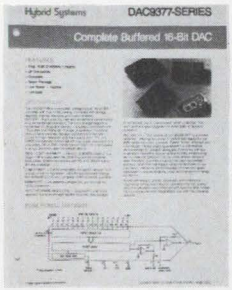
Q/PAC Application Note. Literature describing Q/PAC high capacitance power distribution components on a 45K by 8-bit word static memory board illustrates the features of power distribution and ground networks implemented to construct a low noise, cost-effective, static memory board. Available in either vertical or horizontal configurations, Q/PAC components facilitate design of high density, low-noise memory boards.
Rogers Corp. **Write 269**



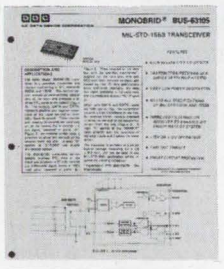
Integrated Circuits. Custom, Semi-custom and Standard Functional IC production is described in a full-color 12 pp. booklet that serves as an introduction to IC production, and includes all the important, useful elements of both a capabilities and facilities brochure. The booklet follows a step-by-step approach to product design, production, quality assurance and service.
Cherry Semiconductor Corp. **Write 251**



DC Servo Amplifiers. This 20 pp. catalog provides general description, specifications, thermal data, application notes, functional schematics, connection diagrams, photos and outline drawings of a complete line of encapsulated and fan cooled linear DC Servo Amplifiers. Units range from 25 to 1000 W, including dual channel units and special units for high altitude use.
Frequency Control Products **Write 256**

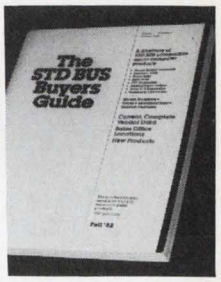


D/A Converters. This 4 pp. technical brochure details the electrical and mechanical specifications on the new complete family of low cost 16 bit D/A converters model DAC9377 Series. The DAC9377 Series features a complete 16 bit DAC family of converters having linearity grades from 14 bit to 16 bit (0.0008%)—all packaged in a 24 pin DIP. Also featured are block diagrams, technical notes, and applications.
Hybrid Systems **Write 258**



Monolithic Transceiver. A 4-pp. product data sheet describing the MONOBRID BUS-63105 MIL-STD-1553 transceiver contains a general description, applications, features and detailed specifications along with figures, tables, outline drawings and an "actual size" photo of the BUS-63105.
ILC Data Device **Write 259**

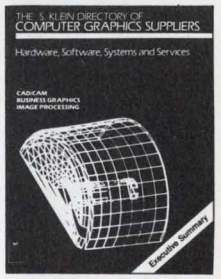
Data Acquisition Components. The 48 pp. short form catalog contains product listing and information on hybrid and monolithic modules such as A/D-D/A converters, S/H, MUX's, etc. Also, Analog I/O boards, DPM's, Digital Panel Printers and Power Supplies. All products are organized into quick selection charts and are categorized by function and performance.
Datel Intersil **Write 254**



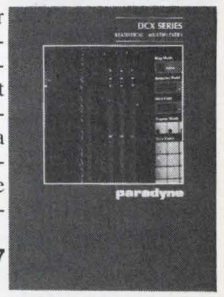
STD BUS Buyers Guide. Lists more than 500 STD BUS compatible board-level products from over 85 manufacturers. The publication includes 23 μC-product categories such as single-board computers, peripheral controllers, and video boards. Thorough product descriptions include design and performance specifications, prices, delivery-availability and date first manufactured as well as manufacturers local sales offices. $25.
Ironoak Co. **Write 261**

UCSD p-System. This book provides readers with a total understanding of the UCSD p-System—the operating system which supports the Pascal programming language on many microcomputer systems. Feature-by-feature descriptions of the file system, screen editor and Pascal compiler, as well as complete instructions on how to write and run a wide range of Pascal programs are included. *Introduction to the UCSD p-System,* Charles W. Grant and Jon Butah, 300 pp., $14.95.
Sybex **Write 271**

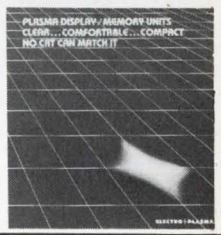
Power Supply. A Power Supply Engineering Reference Pak provides important technical information to the design engineer for selecting and specifying DC power supplies. The Reference-Pak features short-form power supply catalogs with electrical/mechanical specifications and ordering information on hundreds of AC/DC linear and switching power supplies and DC/DC converters.
Power Products Group **Write 268**



Computer Graphics. The 1982–83 edition of the "S. Klein Directory of Computer Graphics Suppliers" pinpoints industry suppliers of hardware, software, systems, and services in CAD/CAM, business graphics, and image processing. Also included is demographic data on the computer graphics industry. $47.
Technology & Business Communications **Write 253**



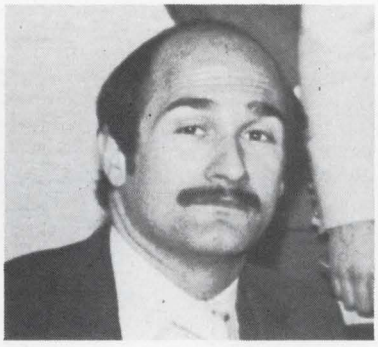
Multiplexer Brochure. The 14 pp. color brochure explains the advantages of statistical multiplexing and describes Paradyne's fully integrated family of intelligent multiplexers. The DCX (Data Concentrating Exchange) Series provides all the data channels a user needs to connect his various terminals and computers, using the absolute minimum number of communications lines.
Paradyne **Write 267**



Plasma Display/Memory Units. A 6 pp. full-color brochure details Electro-Plasma's knowledge, expertise, and commitment in the manufacture of plasma display/memory units. Key features include a rugged and compact design, ergonomic superiority, safety, inherent memory, viewing clarity and comfort.
Electro-Plasma **Write 255**

What Constraints Will Shape The Future μP Development System Product?

by Simon Wieczner
Boston Systems Office
Waltham, MA



Two major forces, I believe, will impact the future requirements of μP development systems products. One is the growing number of 16 bit (and 32 bit) μP applications. The other is the increasing software sophistication of the μP application designer.

To effectively create products using the newer, more sophisticated μPs, more rigorous program modularization and definition methods will come into use. When several engineer/programmers are simultaneously developing a product, they require systems that permit the sharing of source files and of subroutine libraries. Sharing will prevent divergence of sources that results in program incompatibility at system integration time. Additionally, the use of identical development aids will be deemed to be necessary to prevent different kinds of development systems from permitting slightly different program syntax and instructions which may also prove to be incompatible at system integration time.

High-powered linkers in conjunction with relocatable assemblers, compilers and librarians will be necessary to reduce duplication of effort from project to project over commonly used program modules and thereby speed the product to market. Development tools similar to the ones available in the main-frame and mini-computer area will be vital to insure timeliness in program development. These tools will permit reduced errors through facilities for controlling and enforcing more rigorous program design rules and definitions.

To handle the increasing software sophistication of the designer, new products providing features such as symbolic debugging and interactive program execution/modification will come into use. For example, it will be important to have the capability to determine that e.g. variable COUNT is wrong and to instantly replace it and test the correction. Another important feature will be automated software QC. It will be performed by creating test input and output data files that can be automatically read or written from the executing program and tested against correct, standard test data. Whenever a program is modified, that data will be used to validate the program again.

As engineers learn about some of the development tools potentially available to them, they will learn to appreciate their benefits of speedy debugging, thorough and rigorous testing after every modification, testing the software in an environment protected from the undependability of prototype hardware and a user interface that is understandable and clear, but still sophisticated.

As product managers, as well as engineers, realize that their most expensive resource investment is software and their greatest maintenance costs are related to software errors, better development tools and techniques will be required and used.

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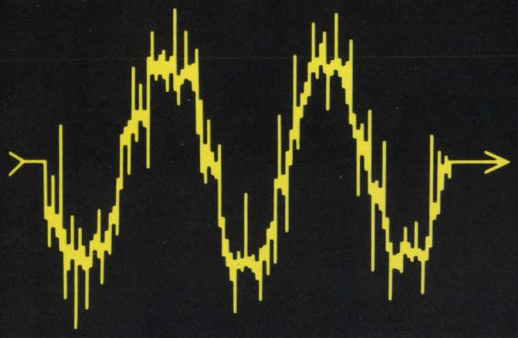

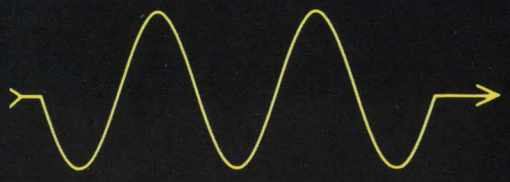

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