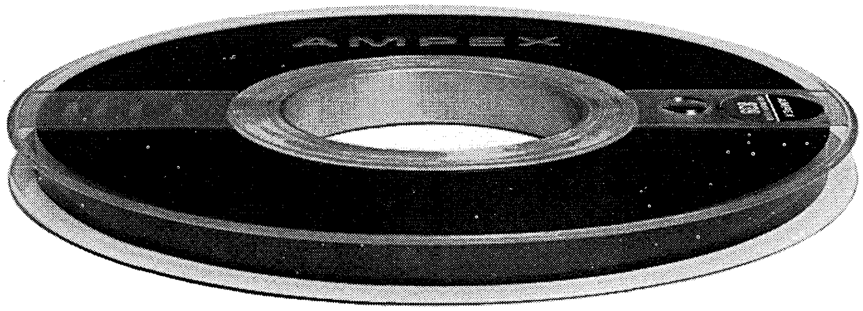
DATAMATION

68

February

Clean and comfortable



when we ship it

when you store it

Our computer tape is clean and error-free. We think that our superior cleaning process makes it cleaner than anybody else's, but of course we're prejudiced. Point is, to be computer tape at all, it has to be clean and free from dropouts.

But we don't stop at merely making clean tape; we make sure that it gets to you clean and that you can keep it clean. Here's how:

Our exclusive environmental shipper which we call the Tape-Safe keeps dust out and your tape "clean and comfortable." Clean, because the polystyrene foam won't shed like cardboard; comfortable, because it cushions the tape in transit against shock and damaging fluctuations of temperature and humidity. Best of all, it's free with your minimum order of Ampex tape for IBM and IBM-compatible computers.

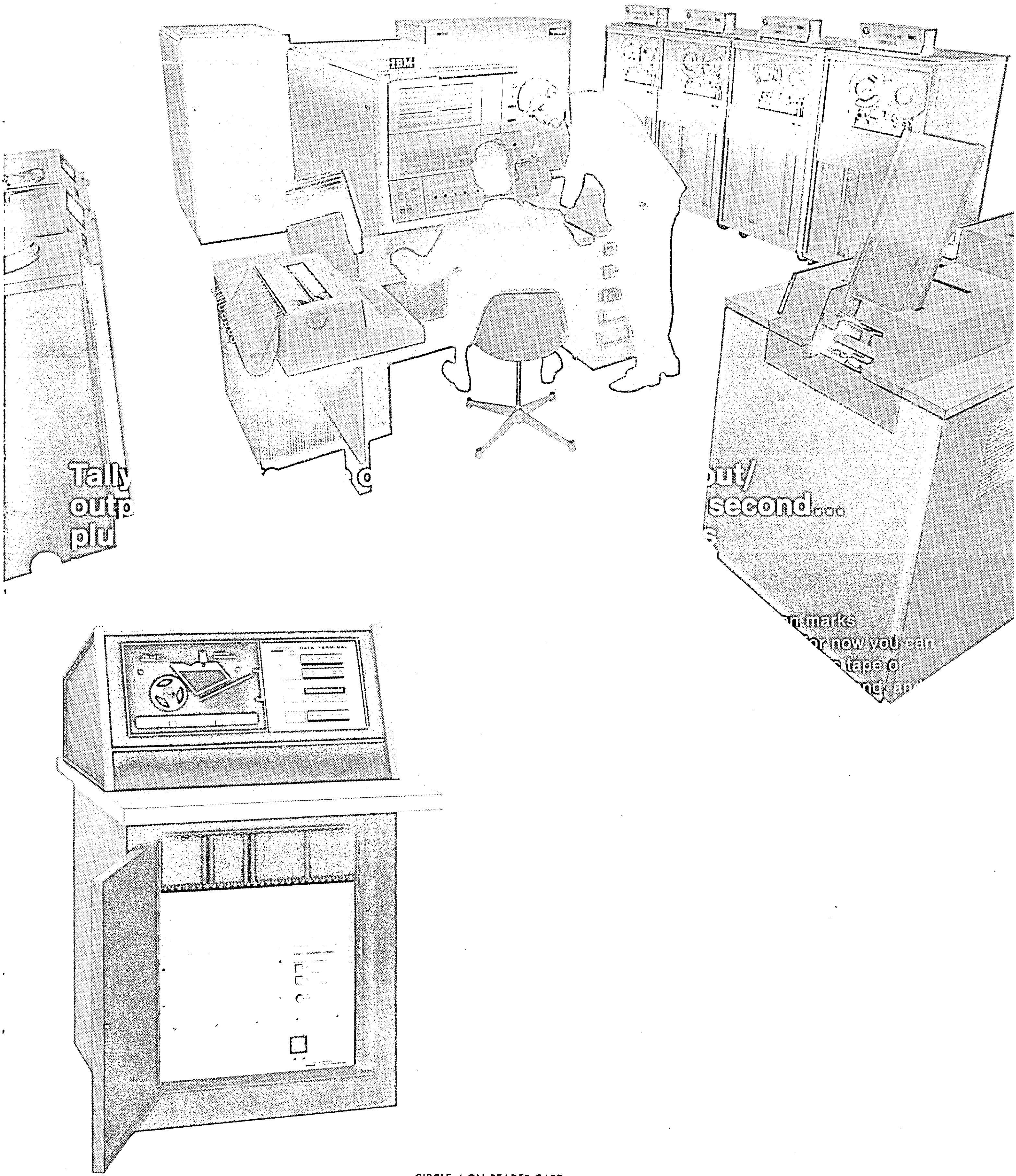
Then, for the only sure protection in storage, we pack our tape in a unique all-plastic canister. It keeps tape clean because it cannot generate contamination and its positive seal prevents outside dirt from getting in; comfortable because it protects against shock and humidity. This canister is even encased in an airtight poly bag during shipment. From then on, it's up to you.

FREE! If you'd like a few suggestions on how to keep tape clean, write Tape-Safe, Ampex Corporation, 401 Broadway, Redwood City, California 94063, for a copy of our TRENDS Bulletin No. 12, "Care and Storage of Computer Tape."

AMPEX

Career opportunities? Write Box D, Redwood City, California 94064.

Tally Data Terminals go "on line" with the IBM 360!



KEYED TO MOVE DATA FAST...AND AUTOMATICALLY

It's 5:00 p.m. in Los Angeles! In the branch sales office of a nationwide company, the day's work is done. All sales orders and other vital data have been recorded on punched tape by an operator using a Teletype automatic send-receive set.

As she leaves for home, the operator inserts the tape into a Telespeed 750 high-speed tape-to-tape sending set, flicks the "on" switch, then forgets about it!

Later that evening, the home office a continent away, in sequence polls this and other Telespeed 750's in similar sales offices scattered throughout the country. Thus, the day's accumulation of data is transmitted to the home office automatically, unattended, and at low cost.

For any multibranch operation, especially where time differences are a factor, Telespeed 750 high-speed tape-to-tape data communications equipment offers many advantages.

Operates unattended! Once the Telespeed sending set is loaded and turned on, it requires no further attention. It is polled automatically by the company's data processing center. After polling, the sending set shuts off automatically.

Table model Telespeed 750 sending set requires no operator during transmission; shuts off automatically.

Reduces cost. By confining transmission to night hours, data can be sent when communication lines are less busy, more economical.

Even if transmission is done during the day, the speed and efficiency of Telespeed data communications equipment lets you take advantage of every minute of line time.

Because transmission is automatic, the operator can devote her entire working day to logging of data. Thus, she can process all orders and other data received at the branch for later transmission; no need to carry over to the next day, no delay in handling important information.

Teletype equipment is fast. The Telespeed 750 machines operate at 75 characters per second; 750 words per minute. The time required to transmit a full day's sales orders, or other data, can be reduced to a matter of minutes.

Increases accuracy; improves customer relations. A major acceptance corporation, providing installment loan service for thousands of their retail outlets, uses Telespeed 750 equipment to good advantage.

Their many branch offices across the country average 300 transactions daily. Every afternoon, the processing center contacts the branches allowing each branch three minutes time, including the time required to make the connection. Thanks to the speed of Telespeed 750's, the transmission of the punched-tape data, almost 60 feet daily from each office, can be handled in 1½ to 2 minutes.

The company's computer is now able to update each account, determine collection action, and prepare notices daily.

Results: streamlined office procedures; increased accuracy in handling accounts; improved customer relations for the retailers! They no longer worry about payment reminders being sent to customers who have already paid.

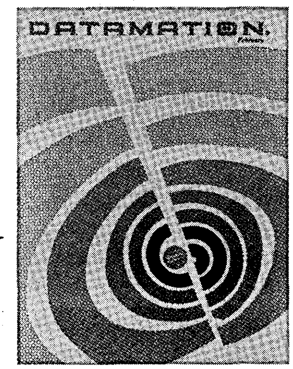
The Telespeed 750 receiving set collects all branch office data recorded on the punched tape; all automatically, all unattended.

Gives you the jump on competition. With competition ever-increasing, the company that "services" best is the one that gets the most business. Telespeed 750's, working with data processing equipment in auditing, production, inventory control, and shipping, give any company a competitive edge.

High-speed tape-to-tape transmission is but one example of the many capabilities of Teletype data communications equipment. Discover why Teletype equipment's versatility is the low-cost answer to your data communications needs. Read our new brochure, "HOW TELETYPE EQUIPMENT MOVES DATA FOR YOUR BUSINESS OR INDUSTRY." For your copy contact: Teletype Corporation, Dept. 81B, 5555 Touhy Ave., Skokie, Ill. 60076.

TELETYPE ®

CIRCLE 5 ON READER CARD



february
1968

volume 14 number 2

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february
1968

volume 14 number 2

automatic
information
processing
for business
industry & science

datamation departments

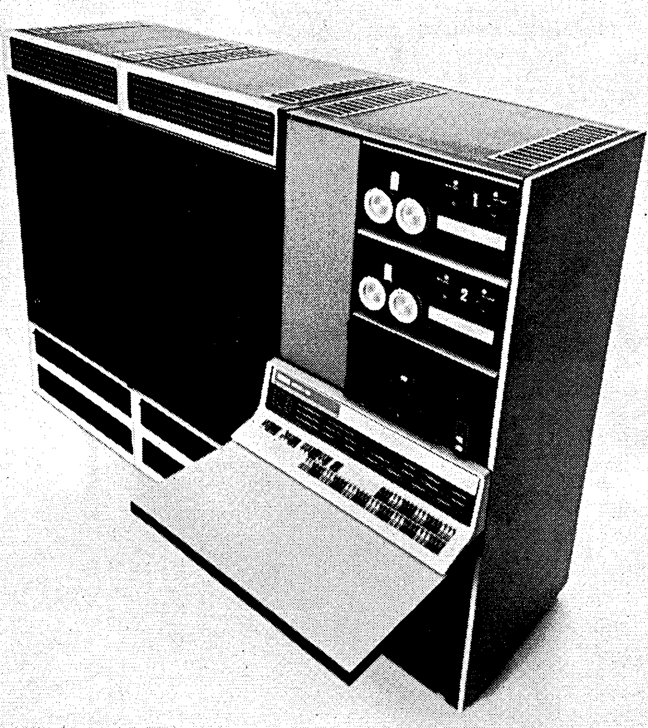
Quiz for Big-Computer experts. Part 1:

1. Open ended time-sharing PDP-10's are being delivered. Other companies delivering time-sharers are____________________.

2. Complete time-sharing software is now being delivered with the PDP-10 hardware. Others delivering completely integrated hardware/software time-sharing systems are__________.

3. Digital's PDP-10 can directly address up to 262,144 36 bit words. It has a 1 usec memory cycle time, a logically complete order code, 7 fully nested programmable interrupt levels, 16 accumulators (15 of which can be used as instantaneous index registers), a high speed, full word multiplexer, and floating point hardware. An equivalent computer might be__________.

4. Basic PDP-10's go for as low as $113,000 but most customers usually buy everything they need to solve big problems. The typical PDP-10 time-sharing system actually sells for between $300,000 and $400,000. An equivalent problem solver from another company probably costs____________________



5. General purpose, multi-user PDP-10 systems can handle multiple jobs simultaneously — conversational time-sharing, real-time simulation and control, batch processing. What other computing system can do this?__________.

6. How much does it cost?____________________.

7. **PRIZES:** Part one of this quiz will be followed by part 2 and part 3. What, beside a PDP-10 brochure, do you consider an appropriate prize for answering all questions in the three parts correctly?____________________And what would you consider an appropriate prize for the man who suggests the most appropriate prize?

Send Entries to Dept. A, Digital Equipment Corp., Maynard, Mass.

digital

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CIRCLE 9 ON READER CARD

calendar

DATE	TITLE	LOCATION	SPONSOR/ CONTACT
Mar. 11-13	Life Insurance Automation Forum	Chase Park Plaza Hotel, St. Louis	LOMA, 757 Third Ave., New York, N.Y. 10017
Mar. 12-15	Spring Joint Conf. Univac Users Assn. & Univac Sci. Exchange	Benjamin Franklin Hotel, Philadelphia	Harry Rayner, Univac, P.O. Box 8100, Philadelphia, Pa. 19101
Mar. 14-16	6th Annual Symposium on Interface of Computer Science & Statistics	Shamrock Hilton Houston, Texas	Univ. of Texas, Div. of Cont. Educ., P.O. Box 20367, Houston 77025
Mar. 14-16	2nd Annual Indiana Computers Users Mtg.	Purdue Univ., Lafayette, Ind.	ACM/D.G. Fryer, G-161, Math Sci. Bldg., Purdue Univ., West Lafayette, Ind. 47907
Mar. 18-21	International Convention & Exhibit	Coliseum & N.Y. Hilton Hotel, New York, N.Y.	IEEE/W. C. Copp, 72 W. 45 St., N.Y.C. 10036
Mar. 29	Seminar: Computers in Graphical DP. Fee: $40-50	Holiday Inn Hampton, Va.	ACM/J. M. Adams, Jr., 211 E. 43 St., New York, N.Y. 10017
Apr. 3-5	Numerical Control: Tomorrow's Tech. Today	Philadelphia	Numerical Control Society, 44 Nassau St., Princeton, N.J. 03540
Apr. 8-10	Users Meeting: Small IBM Computers	Pick Congress Chicago	COMMON/Laura Austin, Adm. Div., General Motors Inst., Flint, Mich.
Apr. 16-18	2nd National Symposium on Law Enforcement Sci. & Tech.	IIT Research Inst. Chicago	IIT Research Inst., 10 W. 35 St., Chicago 60616
Apr. 23-25	4th Annual Conf. on Data Processing	Sheraton-Chicago Chicago	NRECA, 2000 Florida Ave., N.W., Washington, D.C. 20009
Apr. 26-27	Users Meeting	Bellevue Stratford Hotel, Philadelphia	DECUS, Maynard, Mass. 01754
Apr. 30-May 2	Spring Joint Computer Conference	Convention Ctr. Atlantic City	AFIPS
May 1-3	Annual Convention	Ft. Worth, Tex.	Assn. for Educational Data Systems
May 3-4	5th Annual National Colloquium on Info. Retrieval	Univ. of Pa. Philadelphia 19104	Dr. David Lefkowitz, Moore School, Univ. of Pa., Philadelphia

letters

census tapes

Sir:

"Look Ahead" (Oct., p. 183) made reference to trouble with "Census Bureau county/city data bank summary tapes." Your description made it appear that the tapes in question were those of our County and City Data Book series (latest edition, 1967), which are in wide current use and which, to our knowledge, have no defects of the type described. The item was intended to refer to documentation discrepancies for an entirely unrelated computer file comprising county summary records of the 1960 population census. The difficulty with respect to this documentation has been corrected.

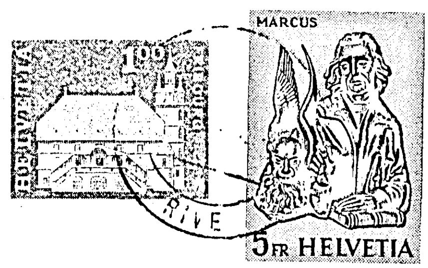
EDWIN D. GOLDFIELD
Chief, Statistical Reports Div.
Bureau of the Census
Washington, D.C.

time-sharing review

Sir:

In "Time-Sharing Tally Sheet" (Nov., p. 42), R. L. Patrick attempts to assess the results of five different statistical experiments, although he is, by his own admission, ". . . overwhelmed by the statistics involved. . . ." His repeated disparaging remarks concerning the statistical content of the various papers reviewed by him reveal a personal bias which has perhaps been nurtured by his own failure to understand the basic notions of sampling theory. Surely, Mr. Patrick cannot be so naive as to believe that numerical data derived from very small samples can be extrapolated and generalized to the point of supporting sweeping conclusions, without at least undergoing an objective appraisal of the relative magnitudes of sampling errors and measured effects!

In commenting on the paper by Schatzoff, Tsao and Wiig, Patrick states, "For reasons academic or political, the authors neglected to draw any hard conclusions from their experimental measures. The dissertation trails off into a lengthy discussion of mathematical statistics, primarily of interest to those who do not produce results for a living . . . ." This type of remark can serve no useful purpose in a forum designed to promote the interchange of knowledge and ideas, for it is as devoid of intellectual content as it is of factual support. The ". . . lengthy discussion of mathematical statistics . . . " alluded to by Patrick consists of one short paragraph (bottom of page 262) aimed at helping the intelligent reader to interpret the



large array of data presented in Tables II and III, and a paragraph at the very end of the paper describing how one might use the results of the study as a guide to the statistical design of future experiments of this type. The criticism on lack of conclusions is equally unfounded, since much of sections 3 and 4 of the paper is in fact devoted to an assessment of what conclusions might be *reasonably* drawn from the data, in light of the very small sample size. Perhaps Mr. Patrick should re-assess the "hard conclusions" drawn by him from the data of all five studies, and answer up honestly to the question of whether he is ". . . producing results for a living."

MARTIN SCHATZOFF
Visiting Associate Professor of Statistics
Yale University
New Haven, Connecticut

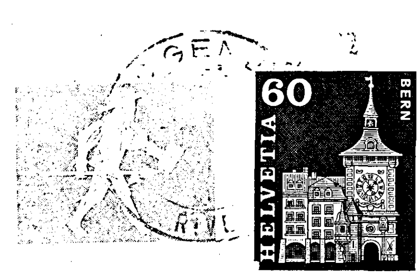
Mr. Patrick responds: My apologies to the good professor. Perhaps with my quill dipped in vinegar I pressed too hard. Upon re-reading the Schatzoff Communication I find that it parses into 32.7 column inches devoted to title, abstract, intro, and design; 17 ci of analysis; 16.6 ci for tables of experimental results; 16.6 ci of "implications"; and 1.2 ci of references for a total of 84.0 column inches. I objected to the 16.6 ci of implications on how to design a better statistical experiment and 0.0 ci on what time-sharing had to offer that batch did not or conversely. This, of course, causes one to wonder: Why was the experiment performed?

Sir:

R. L. Patrick's "Time-Sharing Tally Sheet" was accurate and readable.

Several more points are relevant to any time-sharing/batch comparison, however:

1. No time-sharing system is yet very powerful or convenient from the user's point of view—there is no good communications terminal, few facilities for incremental assembly and compilation, and little in the way of display and edit features for typical TS users. Until TS can exploit its medium as well as batch



does, any comparison is really between two particular systems.

2. In complexity and operational overhead, a good large-scale multiprogramming system is nearly as "bad" as a TS system, since the latter requires only time-slicing over the former, in which sophisticated memory allocation, interrupt handling, data management, etc., are already inherent. One reason progress has been so slow is that TS depends on good multiprogram-

letters

ming, which is also being developed for the first time.

Since manpower costs are climbing while computational costs are decreasing, the TS economic position improves even as the state of the art stands still. One hopes that TS will have more to recommend itself in the future than that!

TAD PINKERTON
Ann Arbor, Michigan

on program protection

Sir:

Mr. Puckett's article (Nov., p. 55) presents an excellent summary and extension of frequently expressed views on the legal protection of computer programs.

However, copyrights are conceptually unsuited for "utilitarian" objects, since a copyright on a description of an art gives no protection against the *use* of the art disclosed. The definition of "copy" is also unsettled. A hardware computer is not a copy of an equivalent program; a program made from a flow chart is probably not a copy of the flow chart; a program on magnetic tape may not even be a copy of an identical printed program. Also, paradoxically enough, copyrights may give too much protection to programs. Their standard of "originality" is extremely low, well within the ordinary skill in the art; almost any routine program would be copyrightable in this regard.

Patentability of programs has been largely premised on the characterization of a program as either an entity in itself or as a new use for an old machine. It is suggested, however, that a program may be patentable as either: (a) a product in itself, if it has a physical structure; (b) a process of constructing a computer, whether or not the computer configuration constructed by the program is new; or (c) as the computer so constructed, if the configuration is also new. This "Tinker Toy" view sees a computer as a high-entropy collection of idle pieces which are brought to a particular state of operative order by a template furnished by the program; it may be analogized somewhat to von Neumann's approach to the theory of self-reproducing machines. Patents are more suited theoretically to the protection of programs than are copyrights. Furthermore, the writing and examination of software patents might easily turn out to be far less costly and time-consuming than that for any other type of patent.

In my opinion, both patents and copyrights are desirable for programs, in addition to trade secrets. Patents would protect the more inventive programs, while limited copyrights would cover the routine but very laborious programs. An alternative scheme would be to slant protection of the program toward the type of protection which would be afforded the product of the program: e.g., patents for CAD programs (since the circuits thus designed may be patentable), copyrights for data-compilation programs (the data produced being copyrightable), etc.

Three final points. First, it has been stated that statutory protection would impair standardization. Quite the opposite is the case; secrecy impedes standardization and leads to wasteful duplication of effort. Secondly, the low capital investment required by programming, coupled with defined and enforceable rights, may rejuvenate in this area the small or independent inventor whose decline has occasioned much grumbling against the patent system in recent years. Finally, the concept of the "program" remains undifferentiated in legal circles. The more mathematical aspects of program concepts and classifications by those versed in machine theory and programming theory would be most helpful in this area. Lawyers, businessmen and legislators have already spoken. Perhaps the mathematicians should now be invited to express their thoughts.

J. MICHAEL ANGLIN
Indianapolis, Indiana

software in europe

Sir:

Mr. Yasaki's article (Dec., p. 27) was a cogent summary of the European software market. We noted with interest, however, that Mr. Yasaki was not acquainted with the European operation of our firm, Data Systems Analysts, Inc.

DSA has maintained a self-supporting operation with a staff of more than a dozen people in the common market for over two years. This does not include that portion of our European business which is serviced in the U.S. Our European operation has been returning a small profit, which (we infer from Mr. Yasaki's article) seems to be unusual for American software firms in Europe. Unlike other firms, DSA's European effort has steadily grown and is expected to double within less than a year.

The omission, however, is understandable as we have been far too busy serving our clients to publicize our operation. Our work has been with European firms, rather than with the U.S. government or with European branches of American firms. As such, the publicity we have had has been largely in the European press.

CHARLES H. MARGOLIN
Data Systems Analysts, Inc.
Pennsauken, New Jersey

who knows?

Sir:

Perhaps the answer to the question you pose at the bottom of p. 21 of the December issue ("Given the marvelous benefits of the machine, what will [man] do with it?") can be found on p. 78 of the same issue.

D. W. DRAWBAUGH
Pittsburgh, Pennsylvania

Ed. note: Mr. Drawbaugh may be referring to a story concerning computer-produced horoscopes, the charge of illegal use of edp gear at the Chicago Board of Education, the forthcoming order for $150 million worth of command/control equipment . . . or all three.

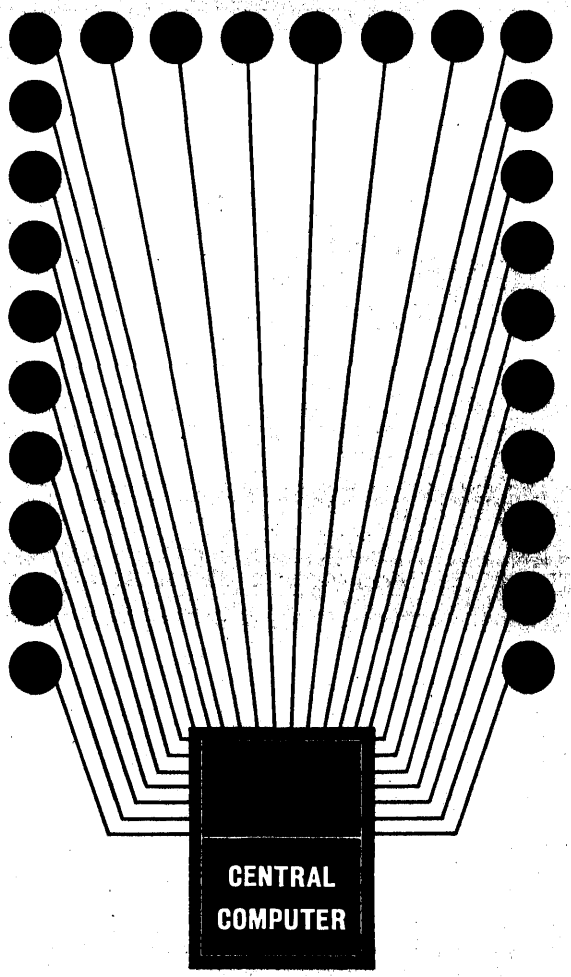
t-s economics

Sir:

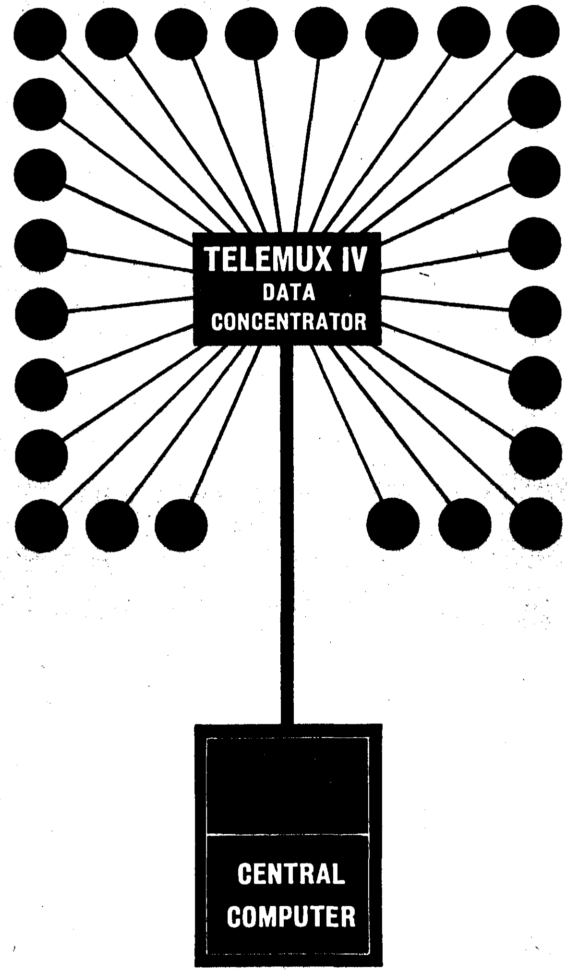
In Part II of their article "Economics of Time-Shared Computing Systems" (Dec., p. 41), Messrs. Bauer and Hill published a table of commercial time-sharing systems (p. 49) which they claim is "adapted" from data published by Computer Research Corp. The information they published in this table is over a year-and-a-half old, and they have omitted mentioning many fine organizations which provide time-shared computer service today, and included one organization which has since closed its doors.

The data which Bauer and Hill "adapted" is published periodically by Computer Research Corp. in its copyrighted publication "The Time-Sharing System Scorecard."

I would also like to make one technical comment about the Bauer-Hill piece. The economics of using a time-shared system, or comparing one time-sharing system with another cannot be



Conventional Transmission
26 Telegraph Lines
—HIGH COST—



Telemux IV System
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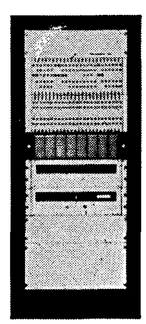
—LOW COST—

TIMED-SHARED COMPUTER USERS

save the cost of multiple communications lines to your central computer–

a remote TELEMUX IV concentrates data from many different types of low speed input terminals over one voice-grade line



for example, as many as 26 individual ASR-33 teleprinters as input devices can be concentrated over a single 2400 baud line

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CIRCLE 12 ON READER CARD

letters

analyzed by simply dividing the cost of operating the system by the number of users. For example, it is misleading to wonder about "a factor of six spread ($5-$30) in the per terminal hour charge" of various systems. What really counts is the problem-solving effectiveness that is gained from spending an hour on a particular system.

A point missed by the authors is that the cost per terminal hour of

a time-shared computer is roughly equivalent to the cost of a man hour. It follows that a system which costs twice as much as another but which allows a user to solve a problem five times faster would be a real bargain. One must therefore consider the economics of a time-sharing system, not only when it is executing debugged programs, but in all the steps from problem conception to solution. The cost effectiveness of a time-sharing system will of course depend upon the types of problems that are presented to it as well as the skill of the user. Unfortunately, due to lack of space, I cannot go into all the ramifications of these concepts. The point is that a great body of literature exists on the subject, and while we still can learn a great deal more, I must disagree with the authors who say " . . . more experience is required before cost factors in time-shared systems are well understood."

LEWIS C. CLAPP
Computer Research Corporation
Newton, Massachusetts

Sir:

"Economics of Time-Shared Computing Systems—Part II" was well done and fairly accurate.

The authors focus on some relatively important system design areas which bear heavily on the quality of service one makes available to users. The quality of service is best gauged by the (1) response time of the computer to queries during the debugging stages of program development and (2) the execution speed when running the program. Response time for searches of files and retrieval of information is also given substantial import by those who evaluate and select TSS capabilities.

Table 1 in this article, however, omits any mention of Dial-Data, Inc., which offers a commercial time-sharing system in the Boston area. DDI services users with an SDS 940 computer.

THOMAS A. WELCH
Dial-Data, Inc.
Newton, Massachusetts

MISery

Sir:

Hooray for correspondent David M. Jones (Letters, Dec., p. 12). It takes courage to take on the sacred cow of MIS, and Bob Head as well. However, Mr. Jones is quite accurate in his appraisal of Mr. Head's appraisal.

I have always felt that MIS Systems (MISS?) were designed by people in a MIST (Management Information Systems Team), headed by a Mismanager. I am sure, however, that until we define management in the structured manner required by a "system," we face an impossible task. Perhaps the answer is a new verb in COBOL: MANAGE. Followed, of course, by MOVE (WITH RESUME). Let us try to get the payroll working first.

DICK H. BRANDON
New York, N.Y.

Ed. Note: Mr. Head declined an invitation to reply to Messrs. Jones and Brandon.

wanted: paper tigers

Sir:

The TSS Project of SHARE has formed the Advanced Time-Sharing Study Group whose charter is to prepare a position paper outlining functional specs for both an operating system and appropriate hardware for the large-scale, general-purpose time-sharing system five years hence. The group meets about every two to three months, and has held discussions on the virtual machine approach, segmentation, and computer architecture and devices of the next five years. At the last meeting, the primary topic was an examination of auxiliary storage requirements for a large-scale t-s system.

The group includes Ted Dolotta of Princeton, Oliver Selfridge of Lincoln Labs, Pete Markstein and Norm Rasmussen of IBM, Bob Woodruff of Yale, Al Irvine of Jacobi Systems Corp., and myself (chairman).

Although the membership of the group represents considerable experience with various aspects of the design, implementation and use of t-s systems, we cannot do an effective job without the support of the technical community. We therefore encourage anyone who would like to express his opinions on any aspect of the large-scale t-s system of the future (hardware, operating systems, user requirements, etc.), to write down his thoughts and forward them to me.

ANDY KINSLOW
John Morrissey Associates
18 East 41st Street
New York, New York 10017

new terminology?

Sir:

I think it's time to introduce a new word into the edp vocabulary: "manageware." With this word we can classify the development of information systems into the following three generations:

1st—hardware—the computer
2nd—software—the computer's work
3rd—manageware—management with computers.

LUIS ARROYO
Madrid, Spain

binary history

Sir:

As I was browsing through an old arithmetic book, I stumbled across a mutilated IBM card which had written on the back (in part):

"100 score and 111 years ago, our 100-fathers landed upon this continent and brought 100th a new nation . . ."

Do you think this might have historical significance?

JACK ALLEN
Virginia Beach, Virginia

on-line solution

Sir:

Re the time-sharing scheduling problem: It is well-known that a human being's respiration rate is directly proportional to his level of frustration. Hence, there is no need for scheduling algorithms. All we have to do is attach an electrode to each user and vary their priority levels directly in proportion to their jitter-level.

ANTHONY AMORT
Beloit, Wisconsin

DATAMATION welcomes correspondence about the computer industry and its effects on society, as well as comments on the contents of this publication. Letters should be typed, double-spaced, and brief. Only those reaching the editors by the 5th can be considered for the next month's issue. We reserve the right to edit or select excerpts from letters submitted to us.

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Now there is a family of electronic data processing systems which can't be outgrown. The Burroughs 500 Systems family—the broadest line of EDP equipment you can find.

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Detroit, Michigan 48232

CIRCLE 15 ON READER CARD

look ahead

A LOUD GOOD WORD FOR THE MODEL 67

Although many IBM 360/67 users have expressed dissatisfaction with the system's on-line capability, the Univ. of Michigan says its interim MTS (Michigan Time-Sharing) system is going full blast. Using a 512K 67 with 2314 disc plus a drum, the system has gone from four TTY's to saturation, with 30 lines coming in without taxing the system.

Using 67 relocation hardware full steam, the system offers a beautiful, dramatic improvement, gushes Michigan's Bernie Galler, who anticipates 40 lines coming in soon. OS-compatible, MTS offers Fortran G and F-level assembler with file management, plus PIL, a Joss-like language out of the Univ. of Pittsburgh, Snobol IV, and five other languages. Terminals include the 1050, 2741, 2250, Teletypes, and several small computers around the campus, with data coming through a home made concentrator to a 67 cpu (second 67 cpu due this summer). Background includes one to three streams which look like terminals to the supervisor. Work was restricted up to Jan. 1 to sponsored and faculty thesis work, but is now open to the entire campus, including student course and thesis work.

MTS is not using full segmentation capability; programs are being run using two segments, but using full paging capability.

BURROUGHS PLAYS NUMBERS RACKET

Burroughs will announce this month a B 500 which is not part of the series 500. The upgraded 300 cpu with 96K core, 2.4 megacharacter disc (23 msec access), printer, card reader and punch, three-mag tape cluster and typewriter will lease for around $4600/month. System will handle up to 64 communications lines, is buffered for on-line work, offers Cobol. Non-disc systems will also be available.

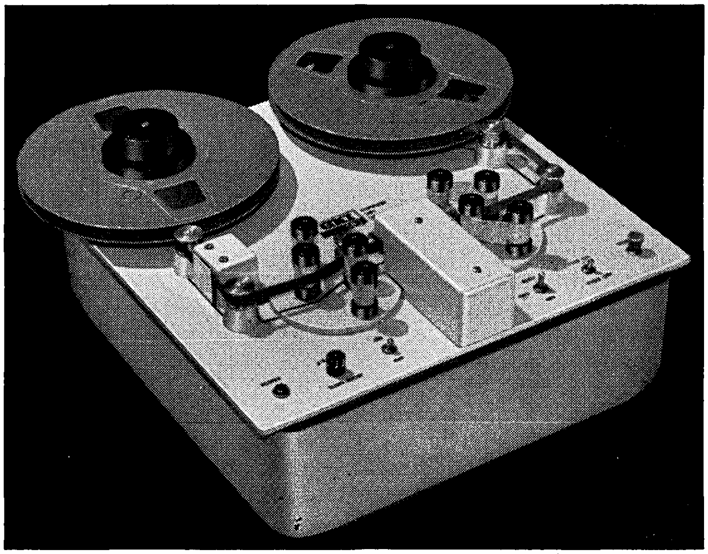
FROM T-S ASHES, A SOFTWARE PHOENIX

An L.A. firm which found its original time-sharing service bureau plans temporarily uneconomical has converted into a proprietary software house.

Time Sharing Services, Inc., under ex-Hughes and North American man Jim Foust, is busy peddling a program checkout package which creates test data, allegedly cuts checkout time in half for the 360/40 and up. Also available: a Cobol-Cobol converter for second to third generation or Brand X to Brand Y machines. And they're working on a Mark IV-type generalized file management system.

The company is also brokering time on a 360/50 offering the checkout package, logged 100 hours the first month. Plans are to install on-line IBM 2250's for an unnamed customer, offer time nationally. Now 11 men strong, TSSI hopes to do $500K this year, is eyeing $1 million within a year and a half.

40% of the computer libraries in the USA have fewer than 400 tapes



in the last two years 20% of that number bought this cleaner

and there is good reason for this. The GKI Model 580 Magnetic Tape Cleaner does everything a blade cleaner is supposed to do—and does it better. It maintains the initial condition of high quality tape and extends its useful life. It cleans both surfaces of the tape more effectively, efficiently and safely than any other presently available blade cleaner. It is more effective because the design of its unique Controlled Motion Blade permits the optimum positioning of the working edge, and Bidirectional Cycling insures maximum coverage. It is more efficient because the self sharpening, self cleaning blade never needs replacement and always presents a clean and precise edge to the surface debris. It is safer because there is no danger of scratching or dirt pile-up due to a dull scraping blade.

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MARSHALL LABS JOINS DISC DRIVE MAKERS

Although the disc pack business is one of the current big winners in the marketplace, only three firms have been making the disc drives--IBM, Control Data, and Memorex. Now comes Marshall Laboratories of Torrance, Calif., a subsidiary of Marshall Industries. Their first commercial products in the computer field will be the Model 2500 drive, directly compatible with the IBM 2311. In fact, you can just plug it into the 2841 control unit.

Due to be announced early this year, the 2500 will beat the competition in access time: maximum access time is 70 msec, average random is 50 msec. And it's said to be less prone to errors and maintenance problems. Cost will be about $19K, with bargains for large quantities, and deliveries are scheduled to start in June.

NEW ENGLAND SOFTWARE: YEAR OF THE ACQUISITION

In recent months, two New England software houses have been swallowed--Computer Associates by Applied Data Research, Wolf Research by EG&G. Now industry pioneer Charles Adams, we hear, has been conducting merger talks with Control Data, which recently acquired software and service bureau biggie CEIR. Adams Associates is some 60 technical people strong, specializes in consulting and special applications design and implementation. Money acquired by acquisition would probably be pumped into ailing Adams' subsidiary Keydata, one of the first commercial time-sharing service bureaus, and reportedly not part of the acquisition talks. Keydata ran into early hardware troubles, has since paid the price of offering special application packages to on-line users, as opposed to t-s bureaus which offer only assemblers and compilers. Adams declined comment.

IBM FIRST WITH PLAN FOR TECH REP COMMISSIONS

IBM is working on an incentive program for systems engineers--carrying on the sound, long-standing theme that "at IBM, everybody sells." The problem is to figure out how to measure the SE's contribution; the proposed solution is to relate it to the success of the salesman he's helping to support.

The pilot project sets up a group of 4-6 salesmen and their systems engineers—about a dozen. The latter's performance is then checked as a team by the success of the salesmen. The rewards are arranged so that big losses or gains are most unlikely --the commission might represent 20% of the SE's total income.

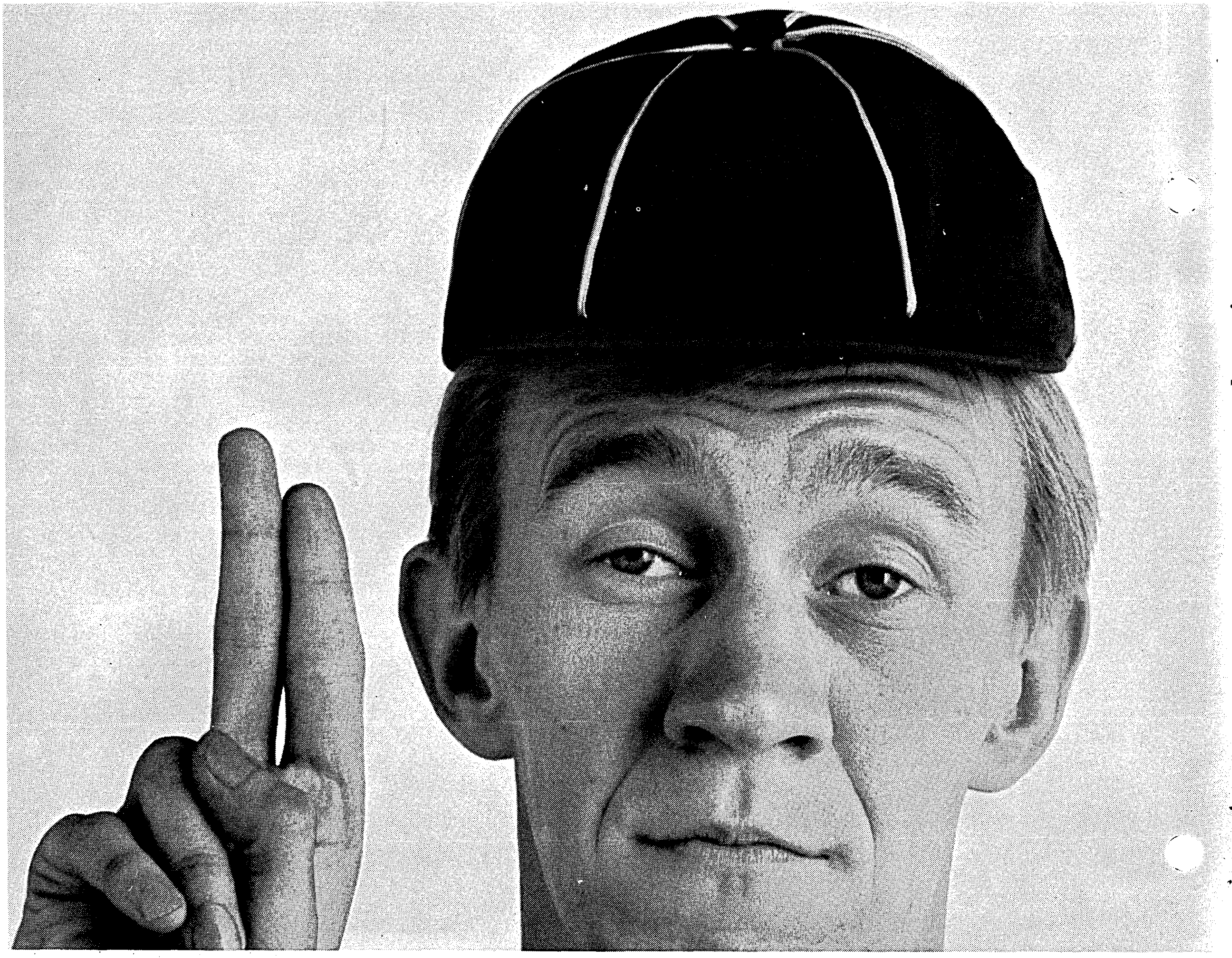
ACM FOR DOVES

Action against the war in Viet Nam is being organized among programmers, engineers, and mathematicians by employees at a New York software house. The Anti-Complicity Movement (ACM), led by Robert Kirkland, is urging that doves in the computer field not work on contracts contributing to the war effort. The group intends to work with other peace movements, hold debates, and publish a newsletter containing data on defense projects and suppliers. Those interested in ACM and its newsletter may write to P.O. Box 7, Fleetwood Station, Mt. Vernon, N.Y.

THE GAME OF THE NAME

Vying for a place in the sum, a proliferation of small service bureaus and software houses are bravely battling anonymity with unusual names. LDV Systems,

(Continued on page 121)



Anyone can promise you time-sharing software.

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Nearly every computer manufacturer has some sort of time-sharing hardware ready to deliver.

Including us.

But when you ask a computer salesman about software, he's likely to start talking about the future. Because what most computer manufacturers have to offer is an operating system, a primitive FORTRAN, and a tape full of promises.

Not us.

When we sell you a 940 time-sharing system it comes complete with an operating system, plus BASIC (a programming tool for beginners) plus a conversational algebraic language, plus a conversational FORTRAN IV, plus a FORTRAN II, plus a powerful text editor, plus a two pass assembler, plus a machine language debugging package, plus a whole library of programs and subroutines. All operating and ready to work.

Now.

The reason we have more is that we've been at it longer. We started working on time-sharing in prehistoric times, almost two years ago. Since then we've sold our 940's to companies, to research institutes, and to time-sharing utility service centers. And they have used them for everything from character recognition to locating a 4-door sedan with red upholstery in a car dealer's inventory.

So when you ask an SDS salesman about time-sharing software he won't start talking about the future. He'll plug in his teletype unit and put you in direct contact with our 940 computer.

It can speak for itself.

SDS

Scientific Data Systems, Santa Monica, California

CIRCLE 17 ON READER CARD

editor's readout

A NEW SEASON

The long, *long* football season is over and, miffed by the fact that we didn't receive Art Buchwald's TV football watching award, we turn our attention to baseball. It's spring training time, after all, and as the pitchers start the long warmup, as chewing tobacco sales rise, as the sports-page cliché level once more rises sharply, it's time for a quick peek at how Computing's '68 major league season shapes up.

IBM. Still hustling despite the fact that they've purloined the pennant umpteen years running, the Giants have everything it takes to cop it all in '68 and '69 and '70 . . . and so on. As with the Yankees of old, the cry continues, "Break 'em up." Even should the Feds step in, a big and varied arsenal, strong bench, a stronger front office make the pinstripes' lead almost insurmountable.

Univac. A well organized, profit-oriented front office has halted the slide of this famous old team. Changing emphasis from walk-and-steal-sacrifice 1004 thinking to the long-ball 1108, the Blue Bells have even forced the Giants to look for more power in their lineup. Strong in some positions; solid upper division team.

RCA. Trying to emulate the Giants, the Cherry Hill Choppers are pleased with box office biz which hasn't yet been translated into steady profits. Lack the long ball; attempts to meet the enemy across the board hurting short-term chances for number two spot. Wait'll next decade.

Honeywell. Anticipating the '64 Giant pennant drive, the Honeydos unleashed their plan to liberate the fans, have since been slow to react to the reaction of the league leader. Have been trying to appeal to the minor league fan with more than moderate success. It's a long haul, but first division finish assured.

Control Data. The Conmen from the land of many lakes don't have water on their brains, have recovered from a disastrous '65, are once more surging back into contention with primary emphasis on the long-ball 6000 series and farm-system peripherals. Strong head man, weak coaching staff, lousy bench.

General Electric. The management reorganization cycle has stepped up, following some near-fatal lineup decisions which wrecked '66 and '67 for the Lightbulbs. Slow to translate minor-league time-sharing successes into big-league results. Lack the long ball, majority of lineup over the hill. Look for new blood soon.

Burroughs. The Mules are still sticking with lineup rushed to majors too soon, but now beginning to prove selves. The power-hitting 8500 strikes out too often, not yet a proven big-timer. Peripheral farm systems strong; beginning to make move in time-sharing league. Solid, dull. Lacks finances and imagination to move swiftly.

NCR. The best of the bush leaguers, the Cash Registers somehow survive with good field, no hit. New lineup with same old coaching staff may mean second division for some time to come.

Scientific Data Systems. Pennant ardor has cooled for the Sigmas, seemingly content to make money in the second division. Hit lots of singles and doubles, get runs in bunches, with long dry spells in between. Rumors of management changes; lots of veterans riding out their options.

That's about it. The first person to make any sense of our projections gets a free season pass to the biggest show on earth.

LARGE-SCALE INTEGRATION: A STATUS REPORT

coming on big

by DONALD E. FARINA

The term "large-scale integration" (LSI) generally refers to the technology of making very complex integrated monolithic circuits. This article will attempt to substantiate that LSI is now an existing technology and will describe the various techniques used. Examples of existing LSI products and some of the problems encountered in their design and manufacture will be discussed. The influence LSI is having on computer architecture will also be discussed.

One might define large-scale integration as that technology which enables the functional complexity of a monolithic integrated circuit to be increased to the point where the integrated circuit is in itself a subsystem function rather than an arbitrary increase in the number of identical gates or flip-flops. To be classified as practical LSI, it must also offer a significant economic advantage over that attainable with conventional integrated circuits.

In the early 1960's—as technology progressed—semiconductor transistor geometries became smaller and smaller. It became obvious that many transistors could be contained in a reasonable sized chip of silicon with reasonable yield. Methods were devised to isolate active areas of transistors to build what was known as monolithic circuits.[1] Monolithic circuits contained 20 to 30 transistors and resistors and were the elemental building blocks necessary to build digital equipment such as gates and flip-flops. Many classes of monolithic circuits evolved, covering the speed and power spectrum.

As the technology progressed further, it became evident that reasonable yields could be obtained if more transistors or functions were contained in a single chip of silicon of similar area. The challenge was to identify subsystems functions that could employ a multiplicity of gates and flip-flops and yet be useful in many types of equipment.

Important assumptions were made about the semiconductor technology that influenced the approach to LSI. Two of these assumptions were as follows:

The cost of making an LSI silicon chip is primarily a function of the silicon chip area and only somewhat a function of the complexity of the circuitry within that silicon area. This statement was reasonable if the technology was constant. In other words, device geometries were the same and the masking and alignment tolerance requirements were the same.

Although the packaging and testing costs would be higher for LSI, the cost per function attainable would be considerably lower if the functional density were increased

Mr. Farina is technical staff specialist for the director of marketing at Philco-Ford's Microelectronics Division. He has been active in research and engineering for MOS devices there and was previously with Fairchild Semiconductor, working on bipolar structure development. He has a BSEE from New York Univ. and has done graduate work in mathematics and physics at Adelphi and Temple Univs.

The author wishes to acknowledge the work of the R&D and Engineering activities of Philco-Ford Microelectronics Division.

1. William H. Richmond, "Integrated Circuits for Commercial Computers," *DATAMATION*, November, 1965.

ten times over the conventional quad two-input gate or J-K flip-flop.

technologies used in lsi

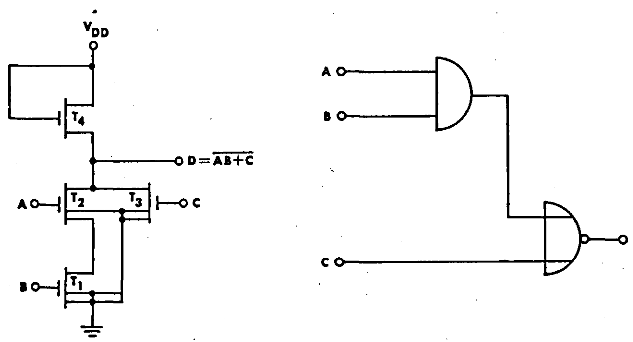
Two technologies are employed: bipolar and MOS, or metal-oxide silicon. Each has advantages and disadvantages, such as differences in achievable complexity level, cost per function, and speed vs. power.

Elaborating on these, the bipolar approach to LSI is characterized by more process steps than MOS, including the requirement for epitaxial growth and for isolation regions to electrically separate active devices. The MOS device is self-isolating and the number of active elements required to perform a typical computer function is considerably less. Since there are fewer active components for the MOS function, there are an order of magnitude fewer contacts to silicon required for the aluminum metallization. Fig. 1 shows a typical MOS logic gate layout illustrating the small size.

It is important to realize that the yield or cost is not necessarily related to the number of process steps. More important is the control required for the critical process steps for each technology and the yield of each step. As an example, the number of aluminum to silicon contacts is not an important yield contributor since this part of the technology is well under control for both bipolar and MOS. The number of contacts, however, does affect the number of devices or functions that can be placed in a given area of silicon.

One might compare the control of bipolar emitter diffusion with the control of MOS mobile and immobile charge in the oxide. (This determines MOS gate threshold voltage and device stability.) The latter is actually at this time even more critical. Photo-resist uniformity, mask alignment, oxide etching and metallization opens and bridging are next in difficulty and are common to both technologies.

The cost per function is primarily related to the size of the silicon chip for N functions since this determines the



AND-OR-NOT Gate and Logic Symbol

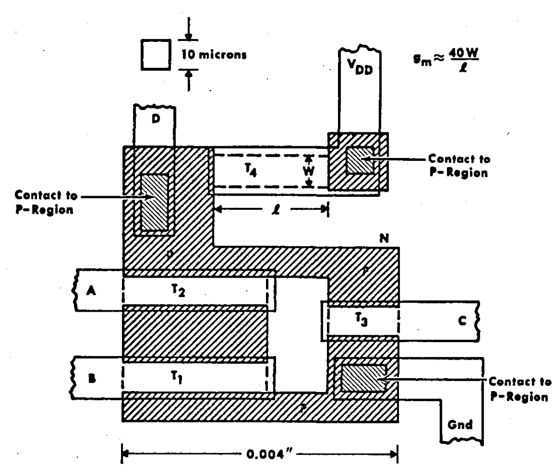
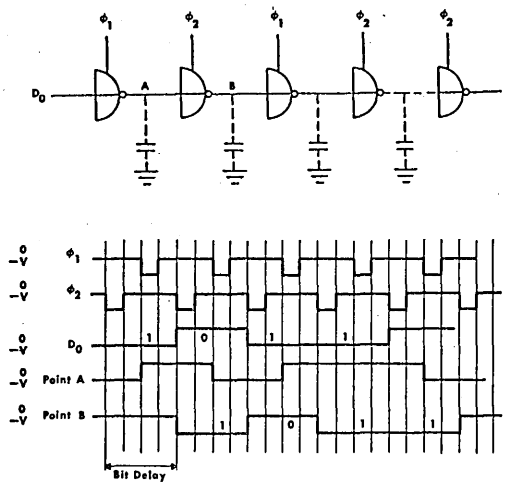
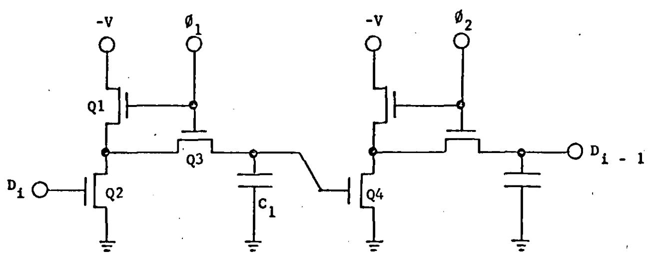


Fig. 1 Representative Layout of AND-OR-NOT Gate
This entire AND-OR-NOT circuit occupies only 4 x 4 mils² — approximately the size of a transistor base. There are only three ohmic contacts as opposed to 18 or 20 in a comparable double-diffused integrated circuit.

number of chips per wafer and the effect of defect density. The percentage yield for any given size chip can be similar for bipolar and MOS. Practical chip areas for both are presently under 8,000 mils² or an 80 × 100 mil die. The MOS presently can accommodate two to five times the number of functions within this area, compared to bipolar complex arrays. The big difference rests in the speed advantage of bipolar over MOS. Also, the MOS is speed limited—particularly at the interface of the chip. Large geometry output devices are required to drive



N-Bit Delay Using Temporary MOS Storage and Two-Phase Clock: Logic and Timing Diagrams



One-Bit Delay

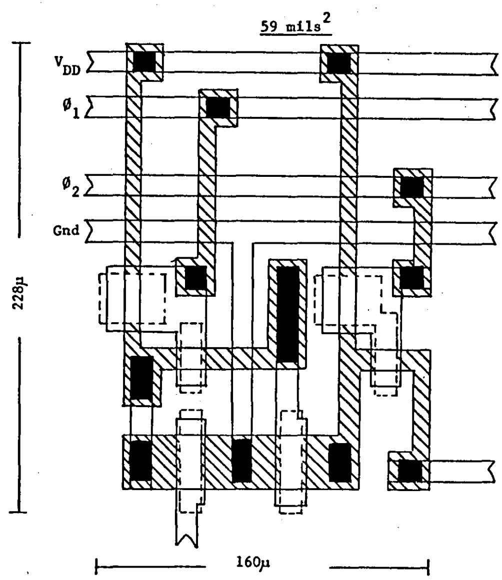
Fig. 2a Basic 2 Phase Shift Register
Demonstrates how the important shift register function is implemented through use of the unique properties of the MOS transistor. The unique features used are:

- The use of an active MOS transistor as a loaded resistor (Q1) which is controlled by a clock pulse (Phase 1)
- The use of the inherent gate capacitance (C1) for temporary storage charge.
- The use of the bilateral properties of the MOS transistor (Q3)

printed board capacities. Significant progress is being made, however, in devising circuit forms to economically solve this interface problem. Through the use of a single NPN transistor and a diode clamp interface circuit, it is now possible to approach the inherent higher speed of the internal MOS circuits and not have the output capacity severely limit speed performance.

MOS integrated circuits are assisted through the use of diffused crossunder regions to form the second layer of interconnection. In the case of bipolar circuitry, it is necessary to incorporate two levels of aluminum metallization to achieve two layers of interconnect. Most MOS integrated circuits made to date get by without requiring a second dielectric insulator and a second aluminum layer of metallization. Even though these crossunders are on the order of a few thousand ohms, this is small compared to the equivalent resistance of the active MOS load resistors, on the order of 100,000 ohms.

The MOS is also characterized by the ease with which one can fabricate the shift register or memory function, as illustrated in Fig. 2a. Fig. 2b shows a layout of such a stage of register and Fig. 7 shows a higher speed, lower power technique. Although the MOS is narrowing the gap rapidly, at the present time the bipolar technology offers considerably higher speed capability than MOS. The cost-per-function advantages of MOS, however, make the use of this technology for LSI very attractive indeed. (This is illustrated in the trends graphs, Figs. 9 and 10.)



Q	μmhos
Q1	10
Q2	100
Q3	40
Q4	100

Fig. 2b 2 Phase Ratio Type Shift Register
In the shift register layout shown, the diffused MOS source and drain and diffused crossunders are shown as crosshatched "P" regions. The aluminum to silicon contacts are the solid squares and rectangles. The gate regions are indicated by the dotted lines.

special lsi technologies

Each approach to LSI is enhanced by relatively new technologies necessary to effectively accomplish higher complexities. These are:

Multilayered interconnects with deposited dielectrics
Computer-aided array layout and design
Computer-aided mask fabrication
Computer-aided testing
Face-down or flip-chip bonding techniques

Multilayered Interconnects. Both the MOS and bipolar technologies can take advantage of the use of an additional dielectric insulator on top of which is deposited a second level of metal interconnect. Fig. 3 illustrates a bipolar integrated circuit containing two levels of aluminum interconnect. Multilayer interconnects are achieved in various ways, the popular ones being vapor deposition and sputtering of silicon dioxide in the range of 400°C to achieve a dielectric insulator approximately one micron thick.

Computer Aids to LSI Design. As mentioned previously, in order to economically fabricate custom arrays of subsystem functions, it is necessary to reduce the tooling costs and design turn-around time. In order to do this, the need for rework or correction of errors has to be reduced to zero. Errors occur in logic implementation, adherence to mask dimensional design rules, adherence to circuit performance design criteria, and attention to chip layout or partitioning of the logic to minimize chip area. Computer aids have been devised over the past two years to accommodate these design considerations.

Automatic Computer-Aided Mask Making. Techniques are being developed to generate photolithographic tooling plates directly from the output of the computer-aided LSI chip design. The main objective is the reduction of human errors in cutting LSI masters. Quicker turnaround time is also achievable but is of secondary importance. As an example, a typical LSI device containing 100 logic functions requires the accurate location of 8,000 coordinates on a cutting table. Generally, the cutting tool cuts a rubylith master at 500X size and requires accuracies of .001 inches or 1 mil.

It is possible to store on magnetic tape information pertaining to the design of computer functions. These computer functions can then be reordered on tape to minimize the interconnection complexity. The computer tape can be used to control a cutting table for purposes of cutting a master. The tape can also control or scan a cathode ray tube from which a picture is taken of the mask. These techniques can be very fast and, most important, very accurate, hence reducing the error rate.

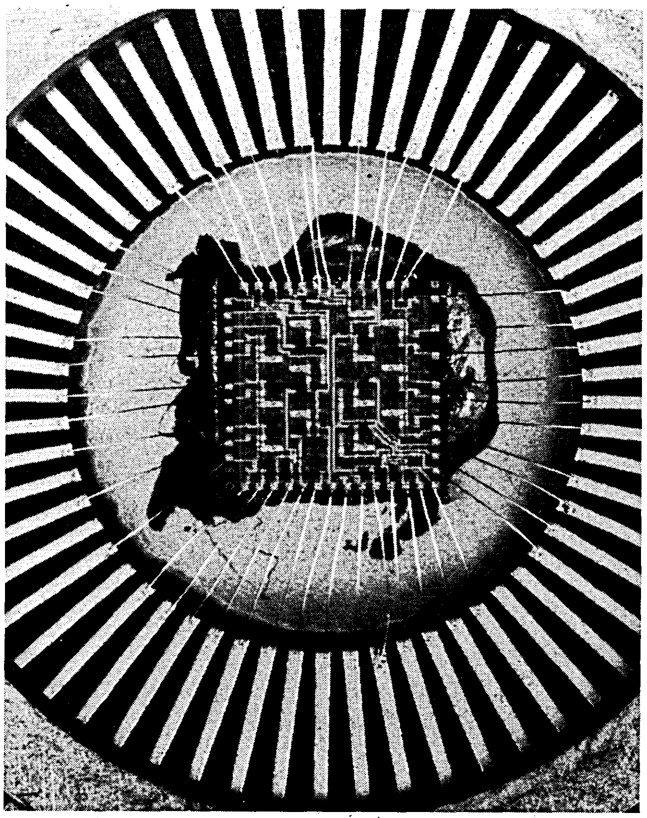


Fig. 3 Typical LSI Complex Circuit in a 60-Lead Package
Shown is a complex bipolar LSI array contained with a 60-lead package. The array contained in a 1/27 diameter package consists of a 27-bit parity checker and contains within a single chip 520 NPN transistors and 234 diffused resistors. The components are interconnected with three levels of metallization separated by vapor deposited silicon dioxide insulators. The chip size is 90 x 85 mils square.

Automatic Computer-Aided Test Program Generation. Testing a complex LSI device is analogous to testing a printed circuit card containing 100 conventional bipolar integrated circuits all in separate flat packs or TO-5 packages. One could test a subsystem function for all possible input conditions. This would be a lengthy procedure and generally only those inputs actually occurring in the specific application are used. Usually even this is reduced to only the difficult test conditions and probabilities are used. The problem is not quite the same for LSI in that the type of failure is not necessarily the same, although there is a great similarity. The dominant failure in the case of the complex array would be open metallization; and, in the case of the printed circuit card, it might be an open solder connection. It is possible to devise a test routine that does not necessarily simulate the actual operation of the LSI device in the machine but, instead, is designed to exercise all inputs of all gates and flip-flops to make sure that opens and shorts are not present. This reduces the test time considerably but requires a computer to generate such a test program effectively.

Flip-Chip Modules of Subsystems. Fig. 4 shows a package containing 10 large scale array chips attached to a metallized interconnect pattern which has been evaporated onto an oxidized silicon wafer. This technique, when fully developed, will significantly affect the cost and performance of systems employing LSI. The package shown contains 2,000 bits of shift register storage wherein each LSI individual chip contains 200 bits. Using such an assembly procedure, one might combine bipolar large scale arrays with MOS on the same interconnect substrate. As an example, a scratchpad memory might contain arrays of MOS random access memory elements and bipolar sense amplifiers. When interconnected in close proximity, as shown in the figure, considerable speed and power performance advantages can be realized. This is due to the order of magnitude reduction in wiring capacitance each chip must drive. Just as important, one can achieve maximum economy in cost per function by not overextending the individual chip complexities.

design and fabrication approaches

There are four fundamentally different ways to design and fabricate custom LSI devices. These four techniques, all compatible with the technologies discussed so far, are:

- Hand-crafted
- Discretionary wiring
- Building block
- Micro-matrix

Even though these techniques—to be described—are considerably different, each has merits and they supplement one another.

Hand-Crafted. The hand-crafted technique involves taking the equipment designer's logic diagram and converting it by hand to a detailed composite mask drawing of the array. In this approach, one tries to minimize the chip area by using only those transistors or components that are absolutely necessary to perform the actual functions. The array is partitioned in an optimum manner to reduce chip area. Although a small chip can be achieved using this technique, it is crude, time-consuming, and requires draftsmen or designers knowledgeable in MOS circuit technology. They must understand circuit design trade-offs and process design rules, and this technique is prone to human error. However, until recently, practically all complex arrays have been fabricated with this technique. Conventional IC's have always been developed in this manner.

Discretionary Wiring. Discretionary wiring is a technique of yield enhancement through 100% testing and mapping of all functions on a wafer to select good from bad functions. A function may be a gate or a flip-flop. Each function is tested to see that the devices are actually interconnected within the function, do not contain opens or shorts or possess abnormally high leakage currents. These tests then define good from bad functions. Wafers containing these identical functions are tested at the wafer stage by means of micro-probing techniques, and a plot is made of the wafer to distinguish the good ones from the bad ones. This mapping information is then fed into a computer along with, for example, a logic expression of a desired complex array. The computer then tries to determine if the mapping data of a particular wafer can accommodate the particular logic function submitted to the computer. The computer performs iterative trials of multilayer interconnections to devise a suitable two-layer metallization interconnect pattern to accommodate the good and the bad devices.

This technique, although having the potential of quick turnaround time, offers the drawbacks of having to micro-

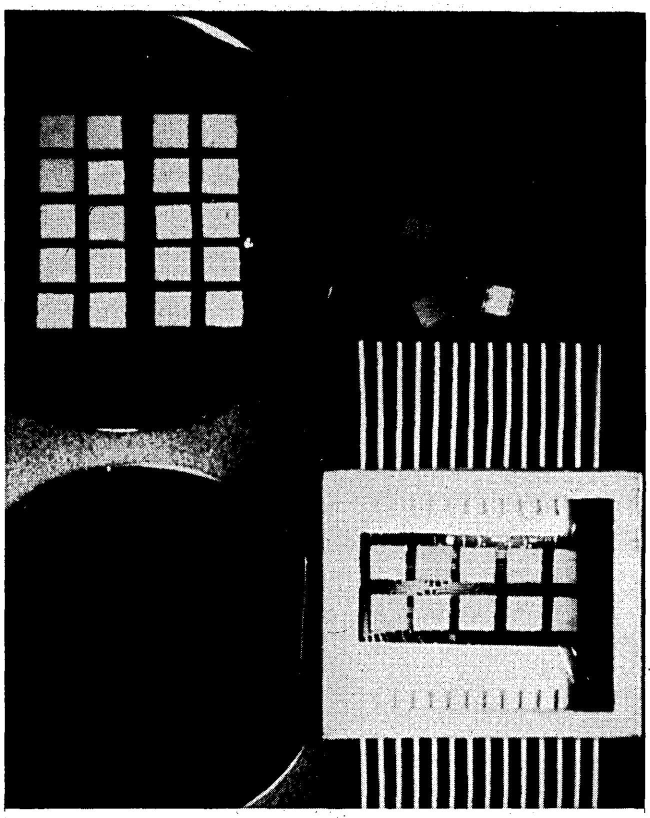


Fig. 4 Multiple Chip Face Down Bonding Complex Subsystem
An oxidized silicon wafer contains an aluminum deposited interconnection. Onto this interconnection pattern, ten 200-bit shift register chips are connected using face down bonding techniques. The wafer is then scribed apart and mounted in a ¾ x ⅞ inch package using conventional lead bonding techniques.

probe devices on the wafer and making a working plate or tooling plate for each and every wafer. In addition, one depends on the high yield of multilayer interconnects which involves the deposition of an insulating dielectric and the deposition and delineation of two layers of interconnection. In general, it is difficult to combine logic with memory and shift register functions in the same chip of silicon. One of the important drawbacks of the approach is that the resulting array is inefficient in use of silicon and the masks are not well suited to production volume.

Building Block Approach. The building block approach is a technique by which the equipment manufacturer can participate in the actual design of the LSI chip. In this approach, the customer is provided a set of decals which are scaled replicas of typical digital functions varying from the complexity of a single logic inverter to perhaps a full add-subtract unit. The customer is then shown how to design a complex chip using these decals; he pastes them down on scaled paper and draws in the interconnection of the building blocks. The advantage of this technique is that the customer gains full control of the logic partitioning of an LSI device and hence can retain this proprietary system design information. The customer can also make changes as time goes on or machine requirements change, and obtain more engineering efficiency than would be otherwise achievable. In addition, this technique minimizes silicon area in that only the proper building blocks necessary to perform the particular function are used and hence memory, logic and shift register functions can conveniently be combined along with special input and output buffers.

The equipment manufacturer then hands the LSI design to the semiconductor manufacturer, who in turn makes the tooling plates. The library of building block designs could be composed of hundreds of types, as opposed to the 10-15 conventional IC's. This approach depends on the usual yield vs. chip area considerations. It depends on packaging the specific functions as tightly as possible through chip partitioning to minimize interconnect length and using only those functions that are

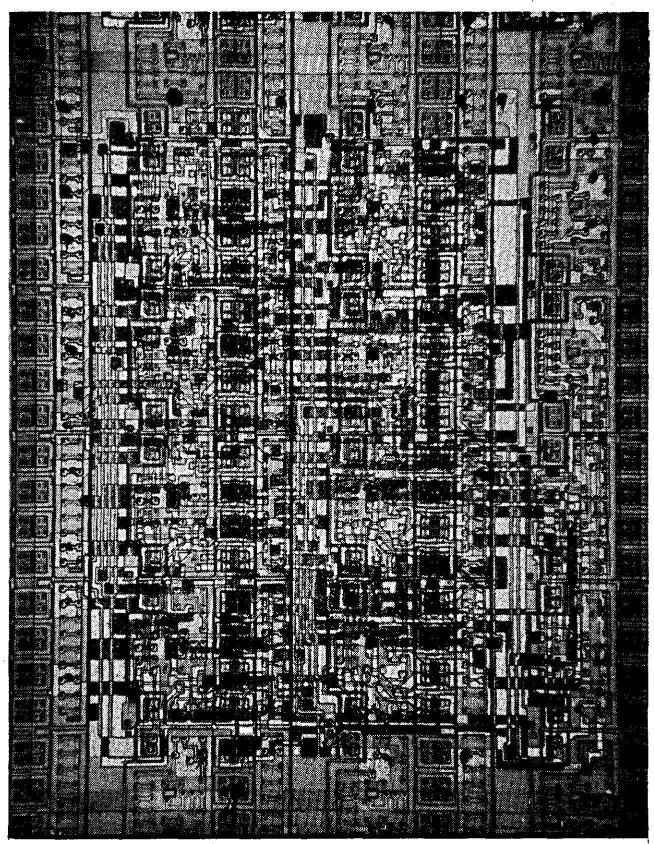


Fig. 5 Philco-Ford Complex Bipolar LSI Chip Using The Micro Matrix Approach
This Philco-Ford microcircuit is a dual function bipolar complex array designed to operate either as a four-stage binary counter (divide by 16) or as a BCD counter (divide by 10) by changing the logic level of a control input. Internal memory elements are provided for the temporary storage of any count. This device is part of an LSI development which utilizes a unit cell array and custom made double-layer metallization approach.
Over 50 gates are contained in the chip which measures 110 mils by 88 mils. The power dissipation is 200 mW. Typically the input frequency is 10 MHz for the BCD mode and 25 MHz for the binary counter mode. The device can be made to dissipate only about one half as much power for applications with lower operating frequency.

required. At this time 50 to 100 logic functions can be placed in a 100 × 100 mil die and there are approximately 150 such die per wafer. Therefore, 30-50 good LSI chips can be expected from each wafer.

a compromise method

Micro-Matrix Approach. The micro-matrix approach is similar to the discretionary wiring approach in that a fixed array of very elemental gates is used. However, this fixed array is small compared to a whole wafer. Typically a 100 by 100 mil die, of which there are perhaps 100 identical arrays on a silicon wafer, is used. Wafers are stockpiled containing the standard diffusions and a two-layered metal interconnect mask is fabricated for a particular subsystem function. This technique is a compromise between the discretionary approach and building block or hand-crafted technique in terms of silicon area efficiency per device. The technique has potential for quick turnaround bipolar integrated circuits, especially where the processing is quite complex and takes weeks. The method does suffer, however, from the inflexibility of combining various computer functions and also is a compromise in the area required to perform certain functions.[4] Examples of this approach have already been demonstrated. Fig. 5 illustrates a bipolar micromatrix which is interconnected with two layers of metal to perform a specific custom product complex function. Each of the above approaches offers certain improvement advantages; however, it is most important that the user be able to play an active role in the design of large scale integration. This encourages, if nothing else, the equipment manufacturer to learn some of the capabilities and limitations of the device technology so that he can best take advantage of it and keep abreast of the advancements.

lsi and new systems

It is generally felt that the low-cost-per-function capabilities of LSI will lead to new system architecture. Little new work, however, has been reported in this area. Many of the ideas that have been suggested depend on the following concepts:

Read-Only Memories. The use of read-only memories, with a single chip of silicon to store one to two thousand bits of information, has been discussed. This suggests the use of hardwired subroutines and code converters in lieu of programs to accomplish the same functions. Some work has been suggested along the lines of using read-only memories to perform algorithms or complex sequential logic. However, little of this has been put into practice. At the present time MOS arrays containing 1,024 bits of fixed storage are being fabricated. Such arrays are ideal for small machine prewired subroutines and table lookup type multipliers, dividers, square root and sine-cosine generators. They also make excellent code converters.

Distributed Memory and Control. Fig. 6 shows how one might combine logic with memory and control in the same chip to result in a more efficient computer arithmetic section. One might consider, for instance, the use of a very small read-only memory for the storage of basic constants continually used in arithmetic operations. In the example shown, an arithmetic unit LSI chip performs parallel logic arithmetic within the chip and the data inputs are serial with a dual-rank, time-shared output data register. The chip also contains an operation code register and decoder wherein the decoder looks for operation codes for only those functions that are applicable to the arithmetic unit.

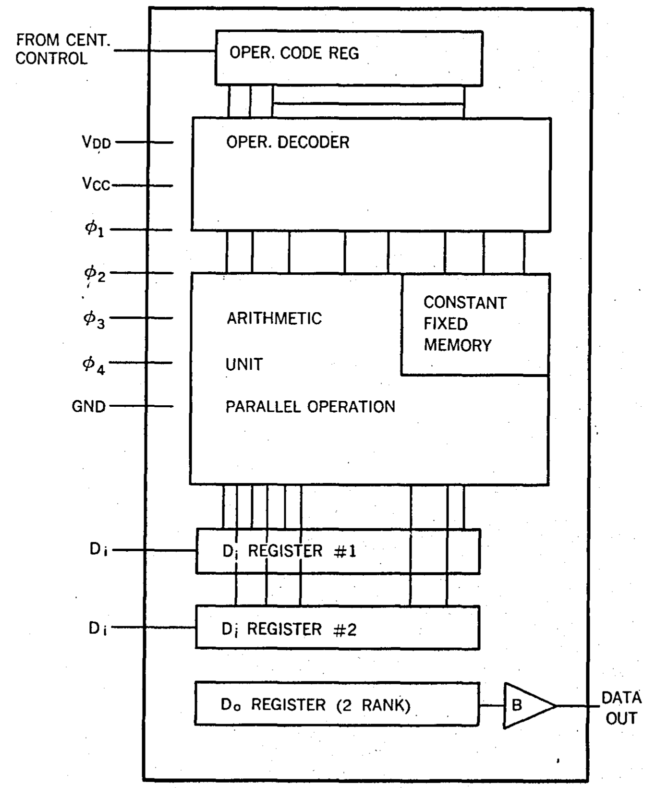


Fig. 6 New Computer Architecture Example — Arithmetic Unit LSI Chip

This arithmetic unit, LSI chip, takes full advantage of the ability to combine logic memory and shift register together with the same process technology. The result is a microprogrammable arithmetic section containing only 11 terminals.

Digital Differential Analyzers. DDA computers have been built in the past. However, these have primarily used drum or delay-line memories. With the ability to combine shift registers and logic in the same chip, it is reasonable to consider an entire integrator on a single chip of silicon which contains two storage registers and two full adders. It then would become possible to build an incremental computer employing perhaps one to two hundred of these identical chips. DDA computers are particularly well suited to navigation and airborne computer problems involving solutions of differential equations.

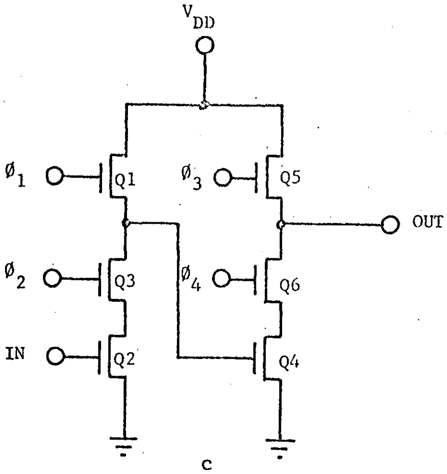
Matrices of Arithmetic Units. The ILLIAC-IV computer is a research program to utilize arrays of identical arithmetic units to achieve extremely high computation rates by means of a combination of serial/parallel arithmetic. Such a technique would begin to take full advantage of the low cost of logic and the ability to distribute memory and control and shift register within each of these arithmetic units.

Random Access Read-Write Scratchpad Memories. LSI is particularly well suited to complex functions that are repetitive in nature—such as memory arrays. Again, it has been demonstrated that memory as a selection matrix can be incorporated in the same chip of silicon. This makes it very convenient to distribute memories in close proximity to the arithmetic operations and the input-output operations of a computer. It is interesting to envision a small computer consisting almost exclusively of read-only memories for the instruction, storage and conversion of input-output data, a small scratchpad random access memory for temporary storage of results, and the combination of

4. "Current Status of Large Scale Integration Technology," Richard L. Petritz, Texas Instruments, Inc. AFIPS Conference Proceedings, Vol. 31, 1967 FJCC.

both memories for performing sequential logic or arithmetic type algorithms.

Associative Memories—Time-Shared Computers. The MOS is ideally suited to combining memory storage along with logic. These are the requirements for an associative memory. An associative memory can be used to supplement a core memory. As an example, consider a time-



Q	μmhos
Q1	40
Q2	40
Q3	40
Q4	40
Q5	40
Q6	40

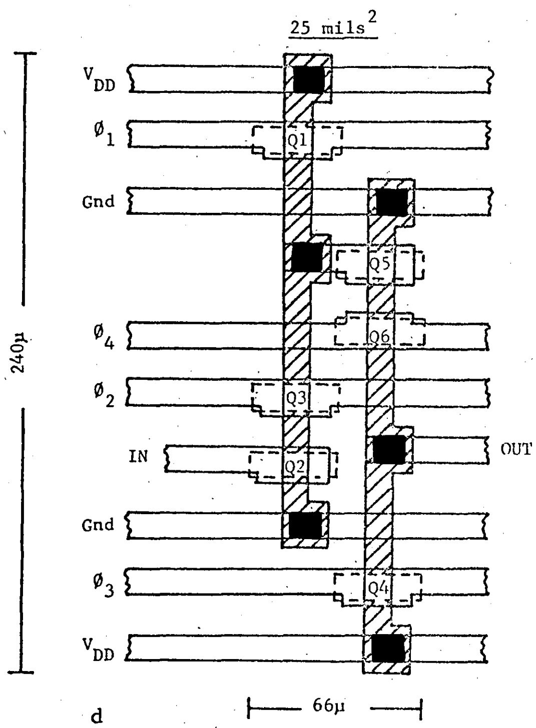


Fig. 7 4 Phase Ratioless Type Shift Register
The MOS circuit technique shows the topological layout for an MOS shift register using a ratioless principle. This circuit technique is capable of 10 megacycle operation and dissipates only 1 microwatt per bit at that.

shared computer wherein 500 subscribers are tied into the computer via remote terminals. As many as 50-100 of these subscribers may be interrogating the memory simultaneously or almost simultaneously. The brute force approach would be to make the main mass core store faster and faster to accommodate this situation. This runs up the cost per bit of storage and is self-defeating.

An alternate approach is to augment this mass program store with small LSI associative memories and small LSI random access read-write memories. For example the control unit transfers the subscriber's program from main store to the associative store and a scratchpad memory is then also assigned to him for storage of the results of calculations. In actual implementation only the next 10-100 program instructions are placed in the associative store at a time.

The scratchpad, being small, can have 0.5 microsecond cycle time thus permitting the core memory to be low cost 2.0 microseconds. The effective access then, as far as each subscriber is concerned, is somewhat greater than 0.5 microseconds.

examples of available lsi

It is fair to say that all of the production-available LSI rests with the MOS technology. This is primarily because high densities can be achieved without the need for multilayer interconnects or for isolation diffusion. A lot also has to do with the fact that MOS is particularly well suited for the important shift register function and the memory function. These functions are best distributed throughout the LSI chips.

Although there has been a great deal of custom MOS activity to perform various complex functions, most of the off-the-shelf standard functions that have been made to date fall in the area of the following:

- Shift registers
- Read-only memories and random access memories
- DDA integrators
- Binary scalers and counters
- Data multiplexers and commutators
- Code converters

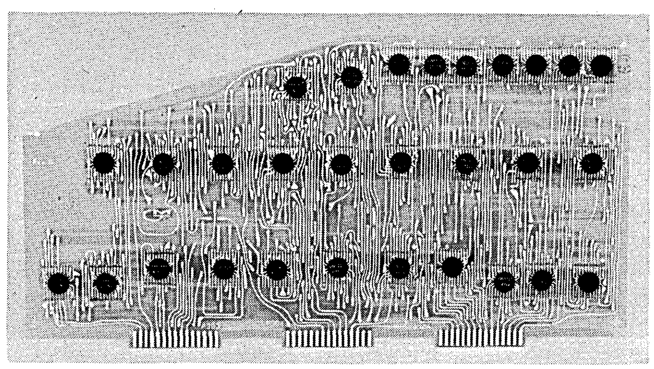


Fig. 8 The Victor Calculator logic card consisting of 29 complex MOS devices. Contains all the machine logic and memory.

It is interesting to note that in the short span of two years considerable increase in functional density has been achieved with MOS technology. This has been achieved primarily through circuit innovation rather than the shrinking of geometries and design tolerances or the introduction of new processes such as multilayer interconnects. The shift register is a prime example of this. In 1965 a 20-bit shift register was introduced; in 1967 a 200-bit shift register was available. This order-of-magnitude density improvement requires only a factor of three increase in silicon area—from 2,500 square mils to approximately 8,000. This can be seen more graphically by referring to the shift register topological mask layout of Fig. 7. This is referred to as a "ratioless" circuit technique in that one does not depend upon the "on" resistance of the inverter being small compared to the equivalent "on" resistance of the active MOS load resistor. Instead, four clocks are used and further use is made of charge storage and transfer of charge. This circuit is only 20 square mils compared to the 59 square mils of Fig. 2. The mask design rules or tolerances are the same in each case. For more details of the MOS circuit evolution refer to Footnotes 2, 3 and 5.

The economics of LSI are vividly demonstrated in what was probably the very first commercial application of LSI. Fig. 8 illustrates the logic card used in the Victor 3900 Desk Top Caculator. This card incorporates all the logic and memory required to operate the machine. There are 24 different types of complex LSI devices and each of them contains about 50 functions or 300 MOS transistors. The logic card is equivalent to approximately 1,500 singly packaged conventional gates and flip-flop integrated circuits and represents two orders of magnitude reduction in solder joints and interconnection complexity. The logic card includes a chip to convert BCD to character information displayed on the cathode ray tube. It includes circuitry to perform the conventional calculator functions of add, subtract, multiply, divide, round off, zero suppression, and complete floating point decimal operation. The

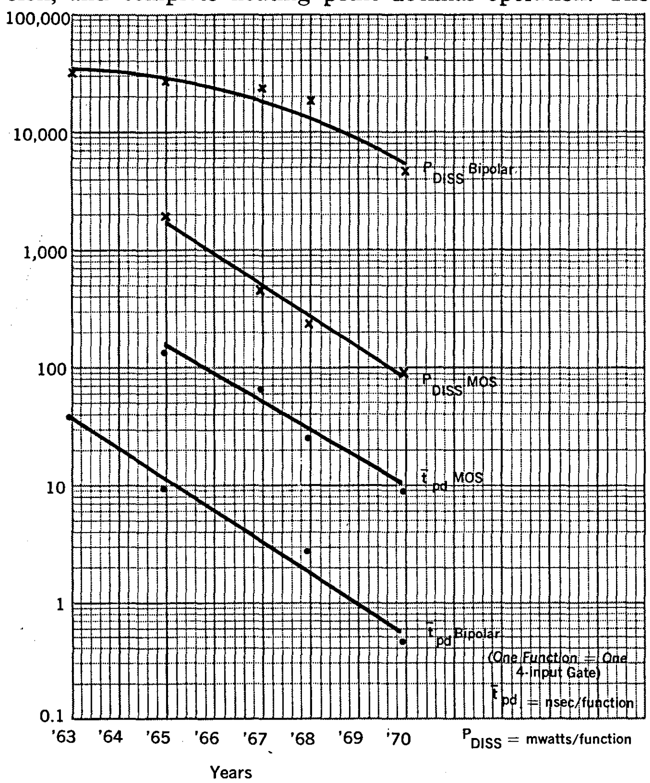


Fig. 9 Comparison of Power Dissipation Per Function and Propagation Delay Per Function From 1963 Through 1970 for MOS and Bipolar General Logic.

logic card also contains the 20-digit keyboard register, as well as two accumulator registers and two additional registers to represent multiplicands, divisors, partial products, etc.

conclusions and the future

Over the past two years, LSI has already demonstrated significant cost savings over conventional IC's. The graphs (Figs. 9 and 10) illustrate some of the performance and cost trends of the integrated circuit technology through 1970. These graphs are based on the following conditions and assumptions:

1. The bipolar curves assume conventional IC's through 1968, with LSI being in production in 1969 and 1970.
2. The MOS curves are for single polarity "P" type devices only and don't assume the production of complementary MOS or MOS/bipolar devices in significant quantities until 1970.
3. The graphs assume that in 1969 and 1970 both bipolar and MOS will be fabricated with smaller geometries (0.1 to 0.2 mil) and will employ at least two levels of metal interconnection.
4. What is meant by a "function" is stated in each graph.
5. The power dissipation per function is at 1 MHz.

It has already been demonstrated that the basic principles of lower cost per function achievable with complexities of 10 to 100 times that of conventional IC's are sound. In the same silicon area previously required to make a single transistor in 1958, it is now possible to manufacture 30 computer functions or 200 transistors. By 1970 this same area will contain 100 functions or 600 transistors and it will cost about the same to process it.

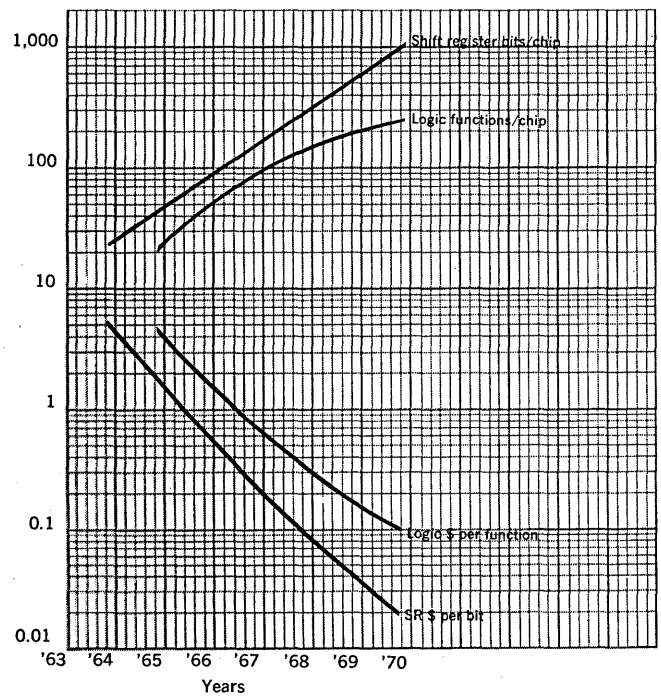


Fig. 10 Comparison of Functions Per Die and Cost Per Function From 1964 Through 1970 for MOS Shift Registers and Logic Functions.

The challenge remaining is simply this: How can digital systems be better partitioned to take advantage of these complexities to reduce the types of LSI required? In addition, can computer aids and automation make it reasonably economical to custom-design every LSI array for maximum flexibility? The next few years will shed light on these questions. Most likely, progress will be made in both areas and there will be a place for both standard complex LSI and custom LSI.

In addition there will be applications where the unique advantages of both bipolar and MOS will be utilized. In some cases these LSI technologies will be used in combination; the performance/cost trade-offs constantly are being re-evaluated.

Computer aids to facilitate custom LSI will continue to reduce the cost and turnaround time. But the most interesting LSI contribution of all will probably be the development of small systems that heretofore were economically or physically impractical to consider. The impact that new systems architecture will have on the market capabilities will be interesting to watch. ■

2. "MOS Monolithic Subsystems: A Revolution in Microelectronics," Microelectronics Division, Philco-Ford, Santa Clara, Calif.
3. J. Leland Seely, "Designing with MOS Field Effect Transistors," *Semiconductor Products and Solid State Technology*, November, 1966.
5. Joel Karp, "Use Four-Phase MOS IC Logic," Philco-Ford, Microelectronics Division, *Electronic Design*, April 1, 1967.

for how much?

WHAT'S NEXT IN MEMORIES?

by DAVID MAYNE

The computer industry, which presently has a new generation of core memories in production, is now faced with the question: What's next in memories? This attempt to answer the question examines existing technologies and extrapolates future development trends.

This discussion is confined to mainframe memories for commercial computers in sizes up to about one million bits. It should also be mentioned that aerospace and military computers have their own particular problems to which the ideas expressed here are not necessarily applicable.

Cost is of major importance to the manufacturer of any commercial product, and the computer manufacturer is certainly no exception. Cost will be a primary influence on the direction of future memory developments and, therefore, is the main subject of this discussion.

At the birth of a new technology there is usually an initial period of intensive technical development yielding big improvements in performance, followed by the evolution of mass production techniques resulting in large cost reductions. Subsequent generations of equipment are further improved and produced at lower cost, but the changes are less significant. Finally, the time and effort spent are affected by the law of diminishing returns. The technology is then developed to exhaustion, and a cost plateau is reached.

At this point, a radically new idea is needed if further significant changes are to appear. With this concept in mind, the future of computer memories is considered.

core memories — current state-of-the-art

For the past decade, core memories have been the backbone of the computer industry. Large sums of money applied to intensive development over this period of time have resulted in the excellent core memory systems we have today. However, this technology is now exhausted, and core memories have reached the point of diminishing returns. Although further development effort can and will still be applied to bring about improvements, these improvements will be less and less significant.

Cost is the prime consideration, however, and core memory costs are discussed here so that they can be related to the costs of other types of memory to be considered later.

The basic core memory breaks down into two parts: the core planes, and the electronics. With core planes the prime constituents are the cost of the core itself and the cost of labor for stringing and testing. When all technical problems are solved and yields are good, the main contributors to core cost are the pressing and the testing operations. Because ferrite is abrasive, press tools are good only for a limited number of cores before they wear out, and amortized pressing cost is approximately in the region of ¼¢ per core. The test equipment used to grade cores is expensive and can only test a dozen or so cores per second. The capital outlay and maintenance of these machines adds another ¼¢ to each core.

The stringing costs, even in Hong Kong or Mexico, are probably in the region of about ¾¢ for the present 3-wire 2½D memories. Testing and rework of the finished planes add at least another ¼¢; hence, a tested plane will cost about 1½¢ per bit.

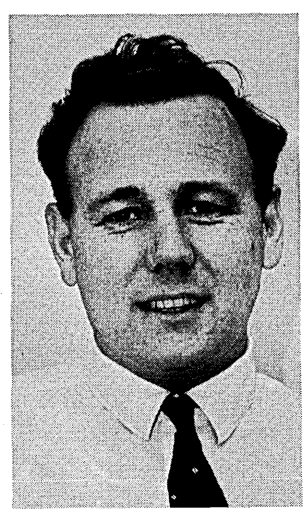
In the electronics portion of the core memory, the main limitation of the drive systems is the number of cores driven on one line. The trade-offs available relate transistor quantity and cost with stack drive voltage and rise time. It is not necessary here to derive the costs, but the designer has done a good job if the drive electronics cost around ½¢ per bit in a large 2½D memory.

In the sensing circuitry, the maximum number of cores that can be sensed on one sense line is usually considered to be about 4,000. The cost of sensing these cores is around $10, adding another ¼¢ per bit.

Peripheral electronics and hardware add a little more to the costs, placing the figure for the complete memory at about 3¢ per bit. This figure represents a cost plateau below which it will be difficult to push core memories.

Speed is also a consideration in core memories. A good 20-mil core (which is current "state-of-the-art") will switch in about 200 nsec. A memory cycle takes two switching times plus the tolerancing allowance of the drive circuits. This latter item is approximately 100 to 200

*The arguments presented and the conclusions drawn in this article are the views of the author and do not necessarily represent the views of Scientific Data Systems.



Mr. Mayne is a memory engineer on the technical staff at Scientific Data Systems. Before joining SDS in 1964, he was with the Ampex Corp., working on advanced development of high speed memories. He holds a BSC in physics from London Univ.

nsec for the low-cost drive circuits we have considered. Hence, the cycle time of large commercial core memories is likely to stay in the 500 to 600 nsec region for the next few years.

film memories

First, a note of clarification. The term "film" can include deposited planar-magnetic films and plated wire. The wire is often made of beryllium-copper plated with a nickel-iron magnetic alloy. Both types of element, when formed into arrays, can be referred to as "planes"—the planar film on some form of supporting substrate, the plated wire sometimes woven into a mat.

Core memories and film memories are similar in that they both have a plane or stack of magnetic elements with drive lines and sense lines and with drive electronics and sense electronics.

However, films have two prime advantages over cores. First, they switch about ten times faster, and second, they have a magnetic peculiarity (anisotropy) that enables them to be non-destructively read, which means that a read cycle need only allow one switching time of the magnetic element instead of two. (In a core memory, a second switching time is needed to restore the information that is destructively read out in the first switching period.) At first sight it would appear that a film memory could operate 20 times faster than a core memory, perhaps with a 30 nsec cycle time. However, a quick survey of the market shows that there are few megabit film memories with cycle times of less than 200 nsec, and those that are faster are extremely expensive.

The reason for the relatively slow cycle time is that, although the element itself will switch in 20 nsec, the film memory is still plagued with the same problems that core memories encounter: those of decoding a large drive-line array and of raising currents of a few hundred milliamperes in the inductance of the magnetic array and interconnect wiring. These processes take time; time that is inversely proportional to the cost of reducing it.

In short, a low-cost large film memory is unlikely to be more than two to three times faster than a core memory. Certain costs are also inherent in film memories. The stack or plane is the most likely area in which a cost reduction can be effected. The plated wire approach possibly has the greater potential since plated wire can be produced in a continuous process. Furthermore, the end product can be electrically tested as it emerges from the plating tanks, enabling correction and control of the plating processes to be handled in a closed-loop fashion (acceptance of good wire and rejection of bad wire being part of the automatic process). Cursory calculations on the capital cost of the setup, maintenance, and operation costs show that the potential cost of plated wire is about 0.05¢ per bit; an order of magnitude less than cores (but of course only when all technical problems are solved).

Considering assembly of the wire into planes, several methods have been used: weaving on a loom, insertion into a grooved or holed frame containing the drive wires, etc. Undoubtedly, much ingenuity can be brought to bear on this problem, and to put a figure on the ultimate cost plateau is somewhat presumptuous. However, it could conceivably drop to an order of magnitude below core stringing costs—about 0.15¢ per bit. At this point, although a low-cost array has been achieved, the problem (as with core memories) of driving and sensing remains.

Depending on the organization employed (linear or word select, coincident current, or hybrid), there are trade-offs between drive circuitry, decode circuitry and sense circuits; but the basic problems, costs, and similarities to core memories are still there. Thus the prospects of cost reductions over current practice are poor. In the drive circuits, there is little likelihood that a significant degree of integration will appear because of inherent power dissipation problems. In the sense area, the signals to be sensed contain one order of magnitude less energy than those from cores. Inevitably, it is even more expensive to sense film memories than core memories.

In summary, film memories should be two to three times faster than core memories, with an ultimate cost plateau approximately half that of core memories—perhaps around 1.5¢ per bit.

The higher speed and reduced cost would appear to present an almost unassailable argument for a switch to film memories. However, another approach—integrated circuit memories employing large-scale integration techniques—may not only have greater potential for development but may offer an ultimately lower cost plateau (Fig. 1).

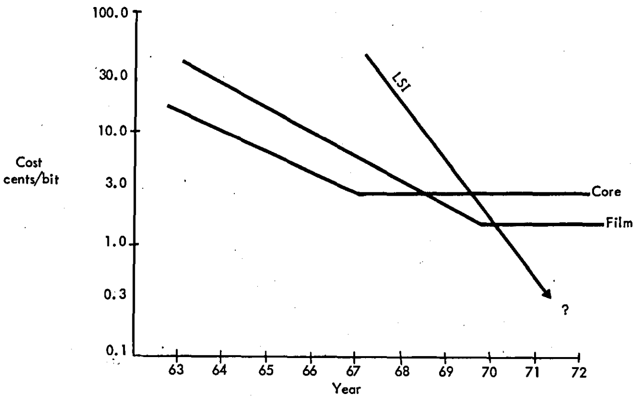


Fig. 1 Comparative Memory Costs

large-scale integration

Large scale integration (LSI) is a recent phenomenon, more discussed than practiced. There are two basic approaches, one using conventional bipolar integrated circuit techniques and the other using metal oxide semiconductor (MOS) field effect techniques. In recent years integrated circuit development has bypassed the MOS techniques in favor of bipolar techniques for two reasons: (1) speed (the MOS device is high impedance and hence more likely to be slowed by stray capacities) and (2) a fundamental problem that existed with the long-term stability of the parameters of the MOS devices. This problem, one of ion migration in silicon oxide, has now been solved by recent advances in technology.

Another problem that is impeding the progress of LSI is that of yield. There are two schools of thought as to how this problem should be solved. One group favors "discretionary wiring." Discretionary wiring tests all circuit groups on a chip after fabrication, selects the working ones, computes the optimum interconnection pattern, makes the interconnections, and tests the final unit. The other group proposes to solve the yield problem by intensive process development to improve yields to near the 100% point.

The MOS integrated circuit is probably of more interest for potential memory applications because of the greater bit density that can be achieved. Bipolar integrated circuits require an isolation region around each transistor, whereas the "isolation" space could be used for anything up to ten more transistors if the MOS technique were employed. Thus the MOS technique offers the potential of one order of magnitude more complexity in the same chip area.

The speed of MOS circuits is largely dependent on the resistance capacitance (R-C) time constant of the circuit element. The resistor is a function of the power that one is prepared to dissipate per element, and the capacity depends on the physical size of the element.

Possibly a good compromise, with present techniques, would be a dissipation of less than a milliwatt per bit, which would yield an element speed of perhaps 50 nanoseconds or so, giving a memory cycle speed in the region of a few hundred nanoseconds (allowing a few stages for decoding, etc.).

An interesting observation at this point is that, as it becomes possible to get larger numbers of bits on the same size chip, the capacities are reduced, enabling the dissipation per element to be reduced with no loss of speed, and allowing the total chip dissipation to remain unchanged.

Integrated circuit memories have numerous advantages, one of the more obvious being that they use only digital logic level signals and do not rely, as do core and film memories, on the interpretation of millivolt analog signals, often buried in extraneous noise. The usual element reliability of digital circuits and insensitivity to environmental changes can be expected.

In contrast to magnetic memories, the cost per bit of an integrated circuit memory will be almost independent of memory size, making a range of memory sizes available without the cost penalties now incurred on smaller sizes.

Objections currently raised to the application of LSI in computers are: (1) if successful, the computer would be comprised of a number of chips, each different, limiting the production volume build-up on each, and negating some of the advantages of mass production of the chips; and (2) the number of leads needed to connect into and out of the chip would be very great, increasing the manufacturing problems and costs prohibitively.

A few moments' consideration will show that LSI is a "natural" for memories, regardless of its future in the computer. The first point is that all chips could be identical and that, with a density of some thousand or so bits per chip, there would be some hundreds of chips per memory. The second point is that, if the chips were organized with internal decoding (as a unit of many addresses of one-bit word length), the pin count could be reduced to a reasonable figure. For example, a chip could contain 4,096 (2^{12}) addresses that can be decoded from information on 12 wires; and, with one wire for data in, one wire for data out, and a few more wires for power supplies, 16 to 20 leads should be quite sufficient.

Another objection raised concerning integrated circuit memories is "volatility," the loss of information in the event of power failure. Volatility is a serious problem in military or aerospace applications, but in commercial computers there are several approaches to its solution that could be considered. One approach is the provision of some form of sustaining power for the memory, independent of the line supply. Another approach is the dumping of key locations into disc memory during the few milliseconds between detection of power loss and the time the regulated supplies become unusable. Unquestionably there is a problem here, presently unsolved, and demanding solution before practical commercial utilization of LSI memories is achieved. The performance and cost benefits available to the manufacturer who achieves that solution, however, insure that a major development effort will be expended.

Lastly and most important, what will be the cost of LSI memories? To answer this question, the cost history in the semiconductor industry over the past decade should be reviewed. The first transistors were expensive (perhaps ten dollars or so), and the price fell rapidly (as technology and yields improved) to a plateau. That plateau, in the region of 50¢ per can, has existed for several years now.

Small-scale integrated circuits began to appear a few years back at tens of dollars per can, but the price fell rapidly. Today it is possible to buy simple ICs (containing a dozen or so components) for less than a dollar a can, and costs appear to be approaching a plateau in the general area of 50¢ to a dollar.

Why the cost plateau? As yields improve to close to the 100% point, the prime costs are incurred in the basic masking and diffusion processes, testing and encapsulation. These costs tend to be somewhat fixed, regardless of the complexity of the circuit, provided again that there is nothing in the circuit design or test specification to impair the yield.

Thus, if circuits are designed with generous tolerances and testing is kept simple, the cost of LSI memory circuits could fall into the region of a few dollars per can in the next few years.

A review of present cost will help clarify this projection. It is possible today to buy a 100-bit MOS register (composed of around 500 active elements) for $50.00 or 50¢ per bit. All indications are that the 100 bits will be increased tenfold (to 1,000 bits) in about two years—a bit increase that will reduce cost to 5¢ per bit and make LSI costs competitive with core and film memories. Allowing for another two years of development, technology and yields will have improved so that the can may be bought for $5.00, bringing the cost down to ½¢ per bit (undercutting cores and films).

Can LSI memory costs be still further reduced by continued development? To obtain the answer another question is posed: What are the fundamental limits that will eventually give rise to a plateau in LSI memory costs? In all probability, the practical limits will not be known for some time, possibly only when they actually begin to limit progress. Still, it is interesting to speculate on the more obvious theoretical limits.

One of these limits is that of physical size and the extent to which the art of photolithography can be developed. The number of elements that can be placed on a chip is roughly proportional to the square of the number of lines per inch that can be resolved in the photolithographic process. Today that number is in the region of 2,000 lines per inch. The limits of optical resolution, determined by the wavelength of light, are in the region of 20,000 lines per inch. Thus, densities of components up to perhaps 100 times those achievable today are possible.

Another consideration is posed in the area of circuit power dissipation. What is the minimum theoretical energy needed to switch a circuit? Several writers have speculated on this point: Keyes offering the relationship between circuit power, delay and capacitance

$$P \sim (C/\tau) \times 10^{-2} \text{ watt;}$$

Fubini and Smith suggest a minimum integrated circuit element capacitance based on optical limitations of around 10^{-14} farad, giving a power-delay product of 10^{-16} watt seconds.

Present MOS integrated circuit elements might consume ImW and switch in 50 nsec yielding a product of 50×10^{-12} wattseconds, almost six orders of magnitude greater than the theoretical limit.

conclusion

An article of this type, by its very nature, is based on broad generalizations to which, inevitably, there must be many exceptions. Still, it is clear that the potential for development in the field of semiconductor integrated circuits is enormous. The trend is unmistakable; LSI memories will supplant core and film memories. The only question remaining is: when? ■

clamp down

PROJECT CONTROL FOR DATA PROCESSING

by MAX GRAY and HERBERT B. LASSITER

One of the great hopes for automated information handling systems is that they will enable management to apply principles of control and rules of judgment without being overwhelmed by the volume of data to which management is exposed. These systems are intended to provide an improved data base for management decision-making and to create more precise control over the operating activities of the company.

Many of the purposes to which automated information systems are applied deal with planning and control functions such as inventory management and control, financial planning and forecasting, profit and loss analysis, and production control and forecasting. Ironically, data processing professionals, entrusted with the mission of designing systems based on these principles of planning and control, have made little headway in applying comparable techniques to the planning and control of data processing resources and projects.

Systems analysts and other data processing personnel are often frustrated when operating organizations within the company resist change because "we have always done it this way." However, it is interesting to raise some similar questions with the same data processing personnel, namely:

a. Why don't we estimate personnel resource requirements for a systems design or programming effort?
b. Why don't we have a project implementation schedule?
c. Why don't we have a more comprehensive project reporting and project evaluation effort?

The answers may differ in wording, but, in essence, they say, "data processing is a very dynamic business that doesn't lend itself to such control" or "we have always done it that way because we are creative people." It may be personally satisfying for data processing personnel to be creative and, over a period of time, through their familiarity with certain files or systems, to become indispensable.

It is totally *unacceptable* from a management control point of view to have these valuable and expensive resources operating behind a self-created veil of mystery built on the premise that data processing personnel, projects and activities are different from all other activities in the business. The corollary to this premise is that proper management control and management disciplines are not readily applicable to data processing. The idea, "we may be sloppy, but we're creative," is intolerable in light of current salaries paid to systems analysts and programmers and the cost of the computers currently installed or on the market.

If many data processing organizations are immature in their approach to management and disorderly in their approach to development of information systems, responsibility for such conditions must be shared by the non-data processing management of the company. Manufacturing companies apply their best management to planning capital expenditures for equipment, to analyzing product effectiveness and diversification and to selecting factory sites. Financial organizations spend extensive management resources in the analysis and selection of financial investment

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opportunities. Yet, these same companies have virtually abdicated management responsibility in the acquisition of data processing machinery and in planning how that machinery and the supporting personnel can be used to maximize their contribution to the company's profit or general well-being. In the absence of corporate direction, it is not surprising that data processing personnel, whose experience rests primarily in technical rather than in business areas, are stumbling in trying to determine the direction their efforts should take to best support corporate policy and corporate planning.

The effect of this lack of direction can result in either or both of the following conditions:

a. Data processing, as an organization, can make decisions for company management relating to priorities applications for development and implementation;

b. It can operate by reaction rather than by response, living in an environment of continual "crash" projects.

There are, therefore, two primary prerequisites to establishing and operating successfully a project control system for data processing—management commitment and a long-term data processing program.

management commitment

Data processing management and the executive office to which it reports must formally define as policy the requirements for precise control over data processing projects and the resources applied to such projects.

This commitment must include the necessary personnel (on an uninterrupted assignment for the time required) to develop a control system and to enforce and monitor the system in operation. Implicit in this commitment is that non-data processing management, as well as data processing management, will review the reports generated by the project control system, will take timely corrective actions as required and will disseminate to the appropriate management such items as project status, resource allocations, and schedule revisions.

An effective project control system needs an attentive management, particularly when all subordinate personnel are required to follow specified rules and practices.

Also implied in this commitment is that management at all levels:

a. Will accept the disciplines embodied in a project control system,

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b. Will accept the requirement for their participation, particularly in reviewing and approving budget estimates,

c. Will accept their responsibility for participating in the assignment of priorities to projects, and

d. Will not violate the procedures for establishing such priorities.

long-term data processing program

An over-all data processing plan for design and implementation of information handling systems must be prepared. Data processing management is responsible for constructing the initial version of this plan and for resolving competitive requirements for resources in joint user discussions. It must include:

a. A listing of anticipated new systems.

b. A tentative schedule for their implementation.

c. A listing of operational systems which will require maintenance and other sustaining efforts.

d. A catalog of systems to be converted from one processing form or mode of operation to another.

e. A listing of systems requiring corrective action to eliminate or reduce the impact of operational deficiencies and the estimated resources required to execute such actions.

f. Maintenance requirements.

The long-range plan should identify the projects to which resource commitments must be made and the projected allocation of equipment use to such development and operational requirements. It will also indicate the chronology in which these events will take place and will establish priorities.

In addition to these two prerequisites, methods standards must exist to specify the policies, procedures and practices which govern all of the tasks dealing with systems development and implementation. Such standards would encompass the following tasks:

The systems survey
Data gathering for systems analysis
Data analysis
Data base organization and design
Process design
Systems documentation
Logic design
Coding
Test planning
Program testing
Program documentation
Systems testing
Conversion planning and installation of the system
Post-installation evaluation
Systems and program maintenance
User training

These methods standards provide a common frame of reference for the performance of the above tasks and thereby provide a common base for estimating resource requirements, reviewing the expenditure of such resources by task and determining the causative factors of performance deficiency.

A major factor, which bears on the type of control system to be employed, is the project mix of the organization. Projects within an organization may be classified by purpose and by development time. The three primary control elements of quality, time and cost may be emphasized in varying degrees depending on the project type.

Fig. 1 illustrates how these three control elements may be given varying importance depending on which element is to be the constraining influence; which, a flexible factor; and which, the crucial control coordinate. Although some organizations may not have the full range of projects

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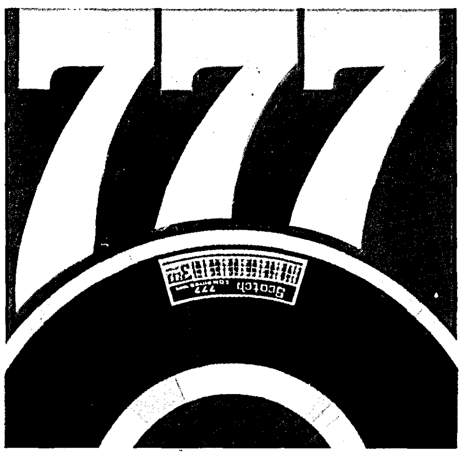

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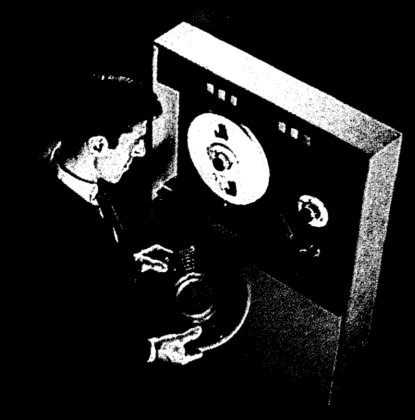

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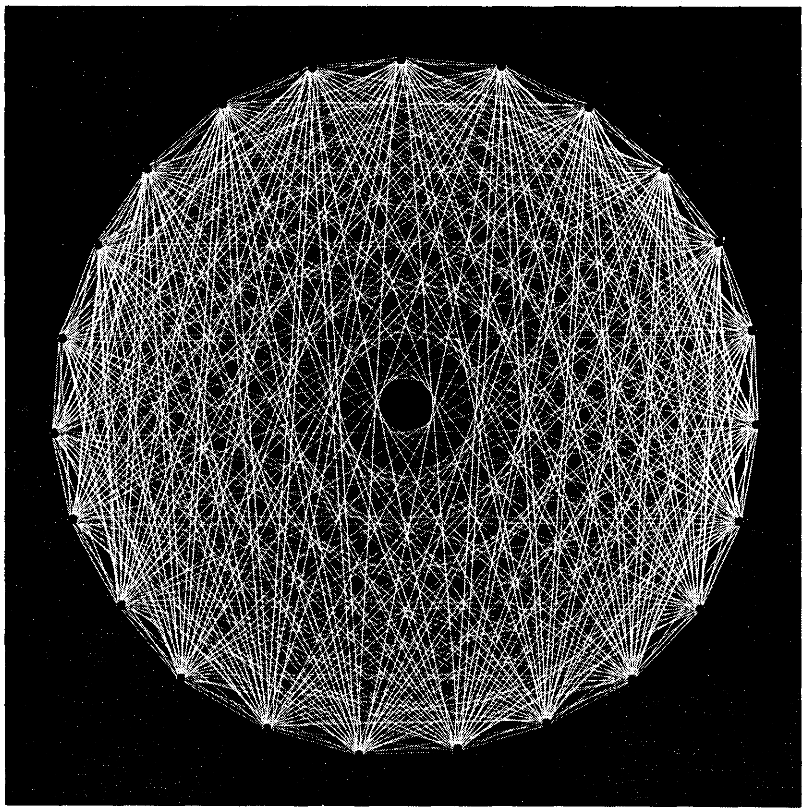


shown or, in some instances, may have project types in addition to those indicated on the horizontal axis, this exhibit illustrates the manner in which the proper relationship can be established. At the inception of a project in data processing, the initial judgment must be the determination of project type and the emphasis of these major control elements.

Fig. 2 illustrates typical control points for a project control system and represents those which must have formal recognition in any long-term development project. An indicator is presented to show which control points would be applicable to other project types.

Development and implementation of a project control

Control Element \ Project Type	Developmental Long Term	Developmental Short Term	Sustaining Projects and Maintenance Modification
Quality	Constraint 1	Constraint 2	Constraint 1
Completeness Correctness	X	X	X
Turnover-Documentation	X	X	X
Development Doc. (historical)	X		X
Efficiency of System/Program	X		
Time	Constraint 3	Constraint 1	Constraint 3
Resources	Constraint 2	Constraint 3	Constraint 2
D. P. Staff	X		X
Equipment	X		X
User	X		

Fig. 1. Analysis of Control Elements by Project Type

Control Points \ Project Type	Long-Term Development	Short-Term Development	Maintenance Modification	Maintenance Rescue
Project Initiation				
1. Project Selection	X		X	
2. Project Authorization	X	X		
3. Planning	X			
4. Personnel Assignment	X			
5. Estimating	X			
6. Scheduling	X	X	X	X
7. Budgeting	X		X	
Project Fulfillment				
8. System Study—First Stage	X			
9. System Study—Completion	X			
10. System Analysis Completion	X			
11. System Design—Data Base	X			
12. System Design—Completion	X	X		
13. Programming—Coding Completion	X	X	X	
14. Program Testing—First Stage	X	X		
15. Program Testing—Final Stage	X	X	X	X
16. System Test Plan Completion	X			
17. System Test—Interim Stage	X			
18. System Test—Completion	X	X	X	X
19. Volume Test Plan Completion	X	X		
Project Conclusion				
20. Pre-Conversion Prep. Completion	X	X		
21. Post-Implementation Audit	X	X	X	X

Fig. 2. Analysis of Typical Control Points by Project Type

system should involve representation of the systems, programming and operating functions. In effect, a project team comprised of specialists in each function should be formed to ensure that all special interests and problems are considered.

The project team should:

1. Review and define installation project mix to formalize that portion of the environment.

2. Study project performance for a representative period, selecting typical projects. This step should identify strengths and weaknesses in present controls and focus project effort on critical deficiencies. Included in the analysis would be:
   a. An examination of the amount and type of maintenance being performed.
   b. Comparison of budget to actual resource expenditures.
   c. Review of operations and user problems in operating the system and using the results.

3. Design a preliminary control system for use in a series of pilot tests. The system must be fully documented and must include instructions for executing and reviewing project control forms. Fig. 3 presents a sample table of contents which illustrates the type and level of content to be prepared for a project control manual.

1. Project Organization
   - Definition of Project Phases
   - Documentation Requirements by Phase
   - Designation of Managerial and Review Responsibilities
2. Definition of Project Types
   - Project Types
   - Standards for Specifying Project Type
   - Minimum Controls for Each Type
3. Project Initiation Procedures
   - Selection Criteria
   - Authorization Procedure
   - Planning Procedures
   - Standard Estimating and Scheduling Procedures
   - Guides to Establish Review Points
4. Project Monitoring Procedures
   - Responsibility for Review
   - What to Review at Checkpoints
   - What to Review at Periodic Reporting Points
   - How to Conduct Review
   - Guides to Taking Corrective Action
5. Post-Project Review Procedures

Fig. 3. Project Control Manual—Table of Contents

4. Test the control system in two steps:

   a. Apply the forms and estimating techniques to a project that has been completed and then validate estimates and control points against actual past performance. This test should provide some insight into the workability of the system and should show the effects that could have been expected if the proper controls had been exercised.

   b. Apply the system to a new project of reasonable size and complexity, using all forms, procedures and checkpoints. To ensure the validity of the test, project standards for documentation and other project tasks must be enforced throughout the selected project. If the project mix is highly varied, several projects may be required for an adequate sampling.

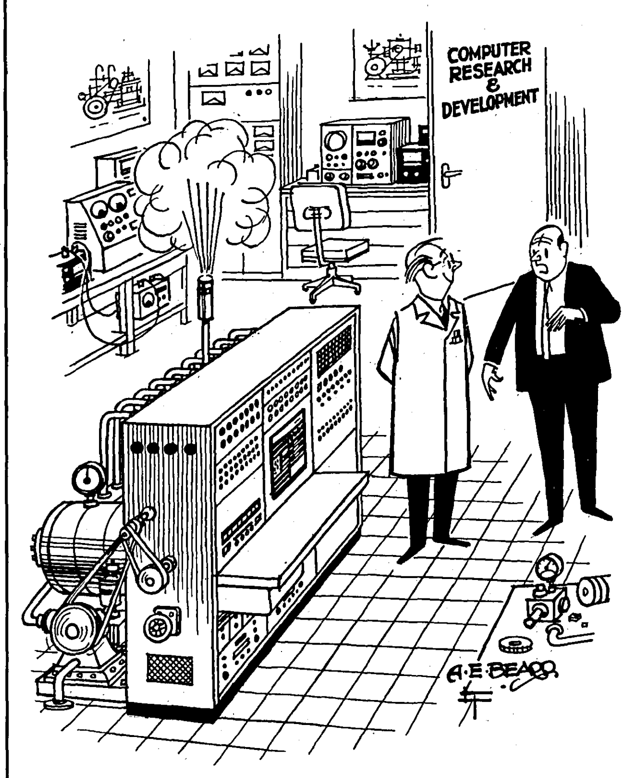
5. Revise the preliminary control system based on test experience. Adjustments to forms, procedures and estimating factors may be required and must be reflected in the project control manual.

6. Train all data processing staff on the use of the manual and their relative roles of responsibility for executing the control system. It also may be desirable to prepare a brief orientation for major users of data processing services to inform them of their roles in supporting the control system.

7. Install the project control system. Installation of the system requires extra management attention during its inception. Adequate project time should be allotted to allow for personnel adjustment to the new approach. In addition, management should be given sufficient time to supervise and coordinate the installation.

8. Audit the system after four to six months of use. The post-installation review should determine whether or not:
   a. The forms and procedures are workable and are being used properly and consistently.
   b. The estimating techniques are realistic and the statistical base developed during the period is reliable for future estimating.
   c. The project control system requires excessive time to perform and administer.

The project control system is dynamic and, thus, requires periodic review and validation. Environmental changes, diversified project mix and improved professional staff skills may necessitate adjustments to the control system. Permanent monitoring and administrative responsibilities for the system should be assigned for at least the first 18 months. By that time, responsibility for the execution of the systems should become a normal data processing management function. ■



"But for god's sake, man, what's the *point* of a steam-driven one?"

COMPUTER TECHNOLOGY IN COMMUNIST CHINA

a historical view

by P. RUSSELL NYBERG

The recent announcement by the New China News Agency of a new large transistorized computer developed by the Chinese Academy of Science's Institute of Computer Technology has renewed interest in the development of that country's computer technology. The purpose of this article is to review the high points of the development of China's computer technology since 1956.

organizational framework

The basic direction of research and development in computer technology in Communist China was set down in 1956 in the formulation of the Twelve-Year Plan for the Development of Science and Technology which established 57 priority fields including electronics, computer technology and automation and remote control. This was further supported by the creation of the Academy of Military Sciences (1958) and a number of new institutes within the Chinese Academy of Sciences' Department of Technical Sciences. These included the institutes of electronics (1958), automation and remote control (1959), computer technology (1957), semiconductors (1956), as well as two branch institutes of computer technology, and a semiconductor laboratory (1957). In 1958, two universities of science and technology, one in Peking and the other in Shanghai, were established with departments of automation, applied mathematics and computers, and radio electronics.

The accompanying chart* (Fig. 1, p. 41) depicts an overview of governmental organizations responsible for the development of computer technology and automation in Communist China, and the relationships that exist among the government, the academic community, research organs of the Academy of Sciences, and the military. Although not shown on the chart, it is significant to note that industrial enterprises associated with computer technology and the electronics industry actually function as an integral part of the research and development process, and they are attached to a university or one or more research institutes as a production element. The success of the Chinese nuclear program has been attributed in large measure to the close coordination between study, research and production, and it is probably correct to assume that the same success has accrued to developments in the computer field.

An example of the three-way coordination is the case of the development and production of a medium general-purpose analog computer capable of solving 20th-order differential equations produced by the Peking Radio Plant No. 1. This computer was designed and built with the cooperation of the Institute of Electric Power Construction Science and Technology of the Ministry of Water Conservancy and Electric Power and the Peking Electric Power Company. The Northeast Bureau of Electric Power Management participated in the initial drafting of specifications. Furthermore, project members were joined by representatives of the Institute of Electrical Engineering, of the Academy of Sciences, and the Research Institute of Electric Power of the Ministry of Water Conservancy and Electric Power. Upon completion of the production phase, the Peking Aeronautical College supplied the plant with a difficult differential equation to test the machine against announced capabilities. This analog computer, now in production, was designed to implement more economical distribution in electric power systems.[1]

period of soviet aid

Any discussion of the development of computer technology in Communist China must inevitably touch upon the first decade in Sino-Soviet relations, 1950-60. It is impossible to overemphasize the importance of Soviet aid and assistance during this ten-year period. According to a recent statement in the Soviet press, by Professor M. Kapitsa, ". . . [The] Soviet Union sent 8,500 specialists to China . . . [and] 10,000 Chinese engineers, technicians

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* Adapted in part from Leo A. Orleans, "Research and Development in Communist China," *Science*, July 28, 1967, pp. 392-400.

[1] *Ta Kung Pao* (Hong Kong), December 15, 1965, p. 1; *Jen-min Jih-pao* (People's Daily), December 16, 1965, p. 2; *Pei-ching Jih-pao* (Peking Daily), March 1, 1966, p. 2.

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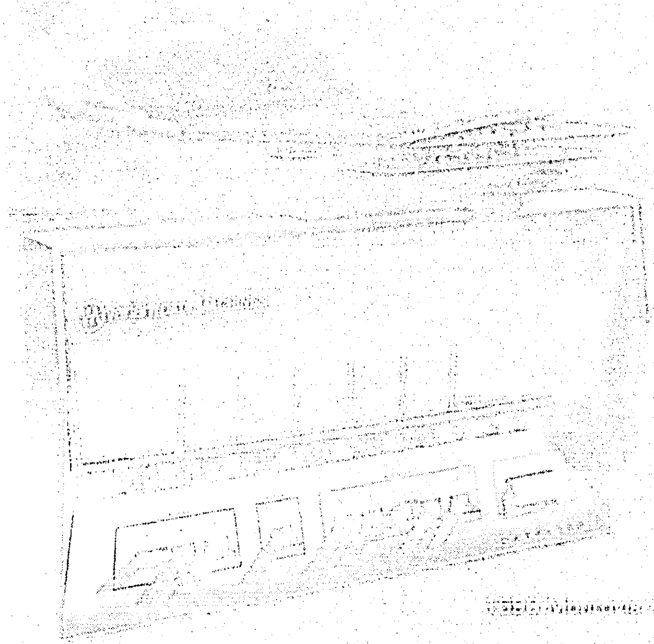

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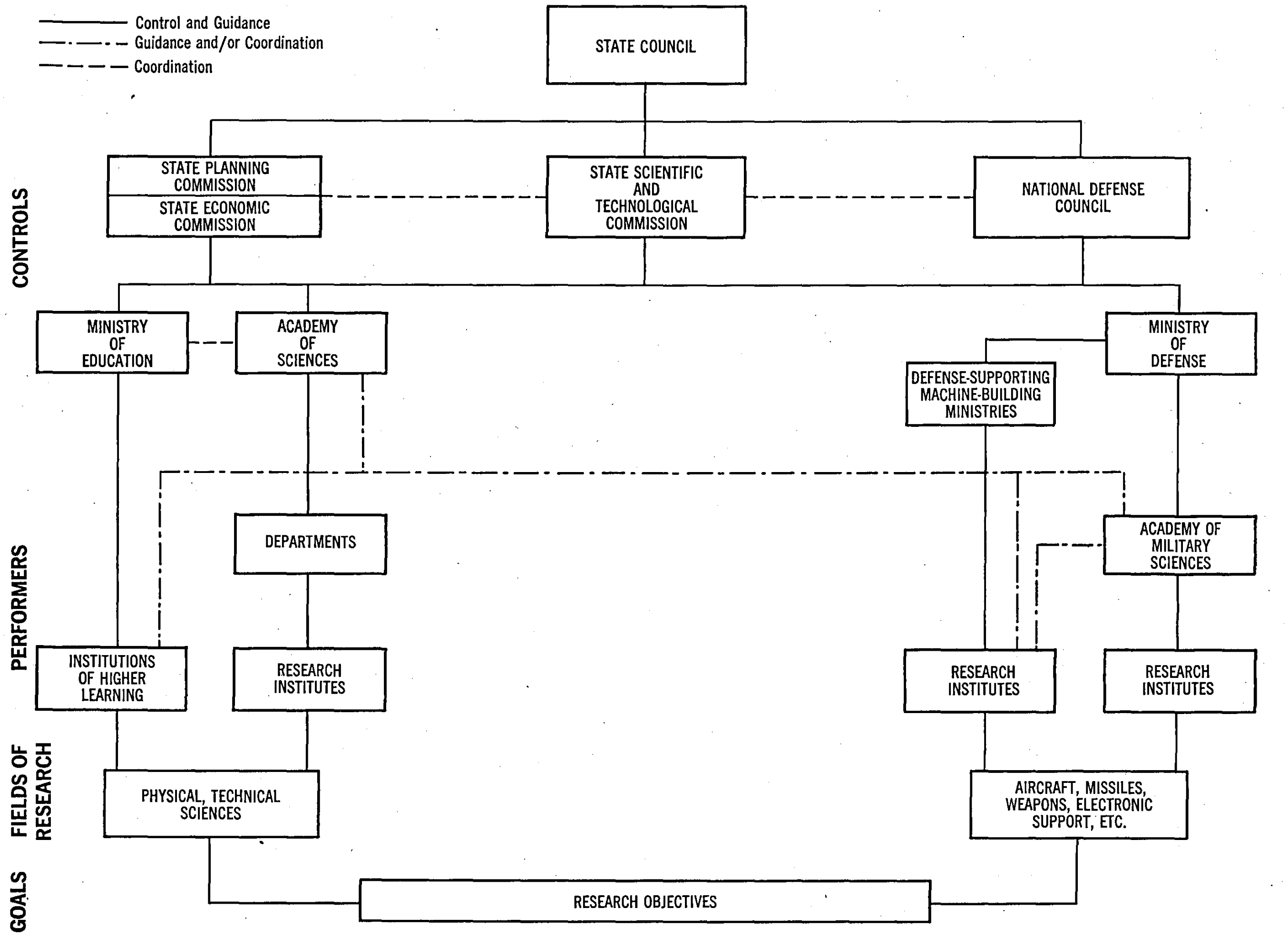


Fig. 1 Chart of organizations responsible for development of computer technology

and skilled workers, and about 1,000 scientists were trained and gained their practical experience in the Soviet Union. Over 11,000 Chinese students and post-graduate students graduated from Soviet institutes and universities."[2] Kapitsa also states that the Soviet Union, under the terms of the Agreement on Scientific and Technical Co-operation of October 12, 1954, ". . . between 1954 and 1964, handed over to the Chinese People's Republic 21,000 sets of scientific and technical specifications."[3] Undoubtedly, a critical part of this technical aid and assistance must have been earmarked for the electronics industry and the field of computer technology.

Certainly, earliest attempts to produce both analog and digital computing machines were based on Soviet equipment and designs. Such was the case, for instance, with the "August 1" transistorized digital computer at the Computation Center of the Academy of Sciences in Peking, in 1958; the three computer groups in Peking building a BESM, an M-3 and a MARK III (a parallel drum machine), in 1958-59[4]; and the first small and large analog computers, in 1958-59.[5]

Although the Chinese reportedly were building their own computers as early as 1959[6], it is convenient to take 1960 as the real beginning of a computer technology base in China. In that year, the world witnessed an exodus of Russian specialists from China which set them back at least two years. Dismal failure of the Great Leap Forward, together with the withdrawal of Soviet aid and assistance, meant a general regrouping of all sectors of the economy. Very little information concerning computers appeared in the Chinese press until early 1964. Then, a few photographs and some articles appeared describing in general terms one or two new machines. One of these machines, the FM-8 medium analog computer, a product of the Tientsin Electronic Instruments Plant, had been "the winner of a State prize."[7] An article by Wang Hung-sheng[8] described the FM-8 as "a fifth-generation, minia-

[2] M. Kapitsa, *Moscow News*, October 1, 1966, p. 6.

[3] *Ibid.*

[4] Nelson M. Blachman, "Central-European Computers," *Communications of the ACM*, Vol. 2, No. 9, September 1959, p. 16. Based on the author's conversation with Dr. Antonin Svoboda, member and former director of the Research Institute of Mathematical Machines, who spent two weeks in China.

[5] John Yamaguchi, "Electronics in Communist China," *Electronics*, December 23, 1960, p. 33; also DATAMATION, May/June 1959, pp. 36-37.

[6] Willis H. Ware, *et al.*, "Soviet Computer Technology—1959," *IRE Trans Electronic Computers*, EC-9, March 1960, pp. 72-120; also RAND Report, RM-2541, March 1, 1960. "The Chinese are also supposed to have developed a machine which is completely their own design."

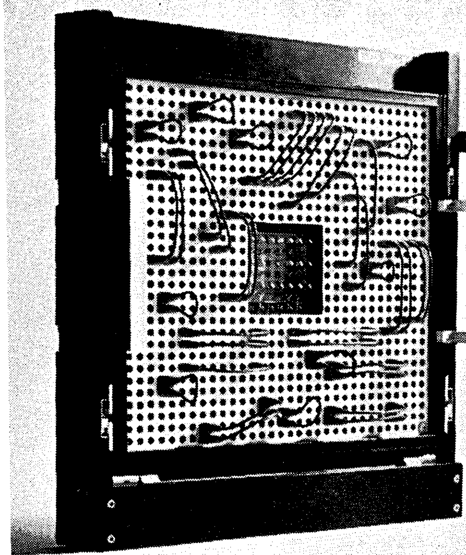
Laurence Clarke, "Notes on the State of Digital Computing in the U.S.S.R.," *The Computer Journal*, Vol. 3, October 1960, pp. 164-167. ". . . [The] Chinese have made a copy in one year from scratch."

Yao Lin, *et al.*, in the Introduction to *Tien-tzu Chi-suan-chi Yuan-li* (Principles of Electronic Digital Computers), July 1961, pp. i-iii. "In 1959, China built and placed into operation its first high-speed large digital computer."

[7] *K'o-hsueh Ta-chung* (Popular Science), No. 8, August 1964; also *Wu-hsien-tien* (Radio), No. 10, October 1964.

[8] Wang Hung-sheng, "FM-8 Analog Computer Produced in Tientsin," *K'o-hsueh Ta-chung*, No. 2, February 1965, p. 19.

Unheard-of quiet.



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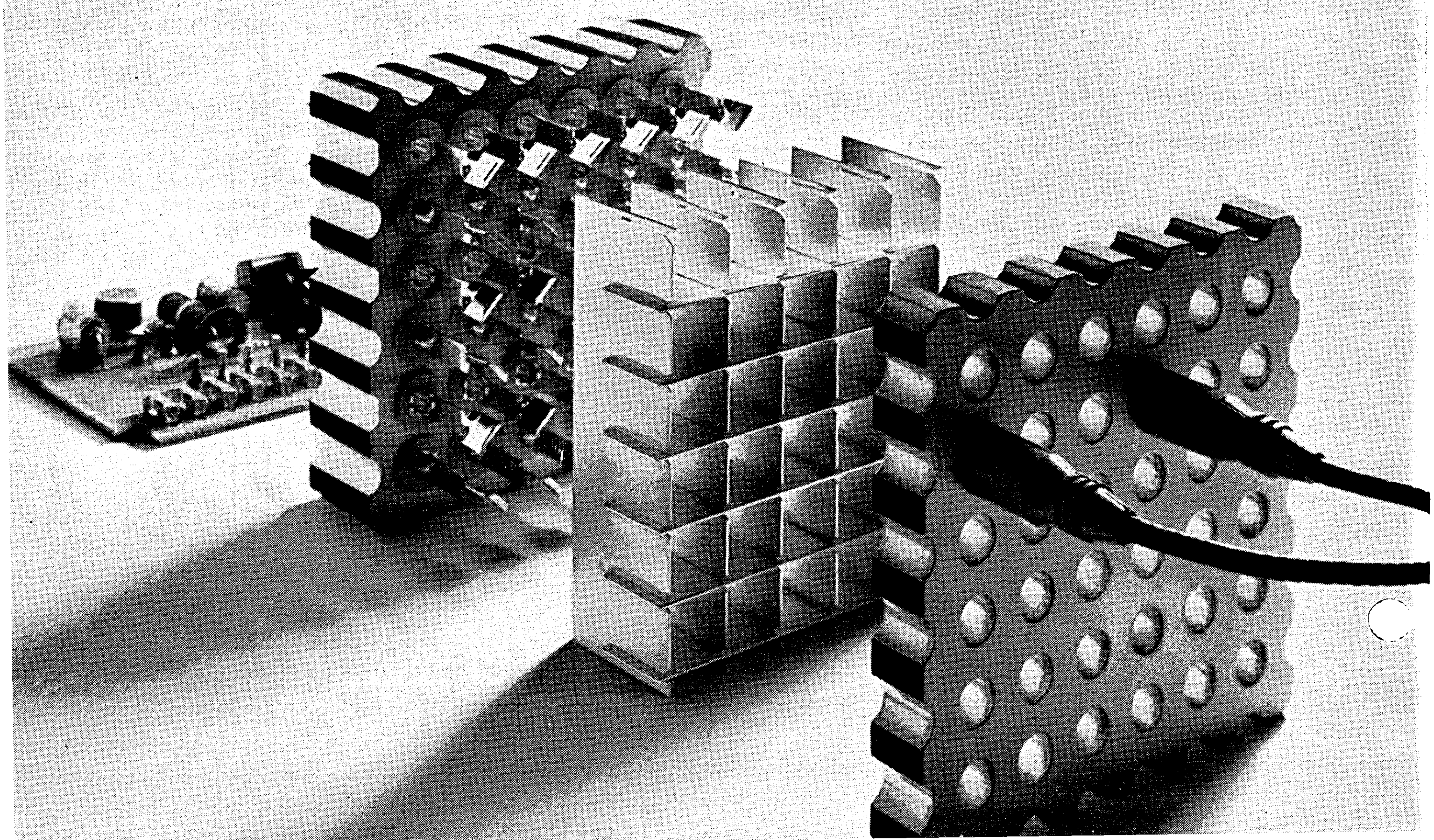

turized computer." The FM-8 was the result of four years of developmental effort. Thus, we know, that the years 1960-64 had not been completely devoid of activity. In another article on the FM-8 analog computer, Tu Tien[9] refers to this machine as "the fifth model of computing machine developed by the Tientsin Electronic Instruments Plant . . . [the] first machine to be built at that plant of medium size." Yu goes on to explain that the FM-8 is composed of 14 modules and it is capable of solving 24th-order linear and non-linear differential equations. Apparently, this machine was designed to perform calculations involving wind tunnels, missile flight trajectories and aerodynamics.

Another photograph showed "a Chinese-built high-speed digital computer . . . [with] magnetic drum and main frame containing 8,000 electron tubes and diodes."[10] By all appearances, this is probably the machine referred to by Ware, et al.,[6] or it may be a later modification of that machine. If this is the case, the machine referred to is probably the Model 103 or Model 104. Principal specifications of the Model 104 are:

- Medium-size, high-speed digital computer
- 8,000-10,000 operations per second
- Three-address, floating-point, binary system
- Internal Storage: Ferrite core memory, 2,048 39-bit words
- External Storage: Magnetic drums (2)
  Speed: 800 characters/second
  Magnetic type units (4)
  Speed: 2 meters/second
  No direct transfer of data between internal storage
- Input Devices: Two high-speed photoelectric paper tape devices
  Speed: 2 meters/second, 15 characters
- Output Devices: High-speed printer
  Speed: 900 lines per minute, 12 symbols per line

In 1966, before the disruptive Cultural Revolution got up a full head of steam, several new computers were announced. Among these were the DMJ-3 medium analog computer and the DMJ-2 small analog computer, both products of the Lien-hu Radio Plant, in Peking; the SJ-1 medium analog computer, made through the cooperation of the Analog Computer Division of the Third Office, Shanghai Municipal Mechanical and Electrical Products Design Institute, and the Shanghai Relay Plant, featuring a main patch panel of 102 operational amplifiers and capable of solving equations to the 24th order; the M24 medium analog computer, built by the Tientsin Electronic Instruments Plant. Also, in February 1966, the results of research done at the Tsinghua University were turned over to the Peking Radio Plant No. 3, in preparation for the task of manufacturing a transistorized digital computer capable of performing 6,000 operations per second.[11]

October 7 of this year, *People's Daily* published the announcement of a "new transistorized, large, general-purpose digital computer," successfully trial-produced at the Institute of Computer Technology of the Chinese Academy of Sciences. No specific details were given in the article other than to state that this machine represented one of several pre-production models that had been studied and built, ". . . mostly during the period of the Cultural Revolution." In view of the lack of information concerning the new computer, the most significant conclusion to be drawn from the announcement is that there is every reason to believe that the social, political and economic upheaval caused by the Cultural Revolution left unscathed workers engaged in activities associated with computer technology. Supportive evidence may be found in two edicts of the central government which spared scientists in China's nuclear and military establishments. The first, point 12 of the Decision of the Central Committee of the Chinese Communist Party of August 8, 1966, stated: "Special care should be taken of those scientists and scientific and technical personnel who have made contributions. . . ." This decision was further reinforced when, in October 1966, a political meeting "of Defense Department [sic] scientists and technicians" heaped praise on military technicians for their contributions to the national defense effort.[12]

conclusions

Several conclusions can be drawn concerning the development of computer technology in Communist China:

(1) China still lags behind the West in every aspect of the development of computer technology, but the gap has narrowed over the past decade. According to statements made by T. C. Tsao, Columbia University, in 1960 and 1967, China *was* "behind the Western World by at least fifteen years,"[13] and is *now* "technically about five years behind the U.S. in the field."[14]

(2) It is unlikely that the Chinese will deviate from the current pattern of assigning top priority to the development of defense-oriented projects. This means that computer technology, so vital a part of the modern defense establishment, will continue for some time in the future to be subordinated to a role of supporting the military sciences in China.

(3) Assuming that the development of computer technology is to a large measure determined by military requirements, and given the present "publish *and* perish"[15] attitude in China, it is safe to say that little information will be forthcoming from that country in the foreseeable future.

(4) It is doubtful whether the latest development, the "large transistorized digital computer," represents any kind of a technical breakthrough.

In summary, the Chinese benefitted greatly from Soviet aid and assistance during the first decade after the founding of the People's Republic. During the second decade of Mao Tse-tung's ascension to power, Soviet aid was withdrawn from China and the Chinese began a policy of "self-reliance" in order to accomplish the goals set forth earlier in the Twelve-Year Plan. Developments of the last eight years indicate that China has the skilled, competent manpower required to further these goals, and they possess the organizational machinery to allocate resources when and where they are needed. The development of China's computer technology has borne the fruits of these conditions as reflected in the ability of the computer industry to flourish and grow even during periods of adversity. ■

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[9] Yu Tien, "The Application of Analog Computers to Aeronautics," *Hang-k'ung Chih-shih* (Aviation Knowledge), No. 9, 1965, pp. 6-8.

[10] *K'o-hsueh Ta-chung*, No. 2, February 1964.

[11] *Ta Kung Pao* (Hong Kong), February 10, 1966, p. 3.

[12] Stanley Karnow, "Red Chinese Purges," *The Washington Post*, October 9, 1966, p. M1.

[13] Don Kirk, China's Three-Way Stretch," *Electronics*, August 21, 1967, p. 131.

[14] Sidney H. Gould (Ed.), *Sciences in Communist China*, Publication No. 68, American Association for the Advancement of Science, Washington, D. C. (1961), "Electrical Engineering," pp. 747-770.

[15] C. T. Hu, "The Chinese University: Target of the Cultural Revolution," *Saturday Review*, August 19, 1967, p. 69.

COMPUTERIZED LIBRARY CATALOG

cross-indexing for the navy

by RICHARD D. FRANKE

How to avoid reinventing is a problem ever present in the modern complexities of national defense, perhaps to an extent greater than in commerce and non-defense industry. Whether the reinvention is an electronic device, a computer program, or an instruction in how to use a piece of equipment makes no difference in principle. Weapons systems and anti-weapons systems are becoming so extensive, with thousands of people and hundreds of thousands of parts, that even the highly educated right hand does not always know what the highly educated left hand is doing. A research engineer specializing in missile launches may be almost totally uninformed about the guidance system that takes over the control of his bird following the launch. This situation has recurred often enough in engineering circles to become well known under the category of interface problems. Perhaps as frequent, and probably more costly, are the instances of lack of contemporary knowledge within a single category of skilled specialization. An expert in the fire control system of any surface-to-air missile may not know what specialists in the fire control system of another surface-to-air missile are doing.

In the Naval Ship Missile Systems Engineering Station at Port Hueneme, California, we deal with Talos, Tartar, Terrier and Standard missiles for more than 70 surface ships of the U. S. Fleet, and for 20 foreign ships from Australia, France, Germany, Italy, and Japan. A significant part of our task has been to cross-feed data, not only to reduce the number of interface problems, but also to keep people who are involved with one missile system informed of significant progress made in another missile system. It is much more economical to cross-feed the information than to reinvent wherever a similar problem may arise. The cost premium on useful knowledge means that investment in mechanizing our information today is mandatory, because traditional methods have proved inadequate.

The problem, of course, is not unique with us. Our computerized catalog has been a modest pioneering effort, to help us fulfill our mission economically. We are reaping benefits that make possible the funding of continuing experimentation in mechanization that hopefully will lead to further economy. Perhaps the cross-feeding of experience so far, with people who are faced with a similar urgent need, may help all of us to keep reinvention to a minimum.

objectives and development

The technical library catalog project at the Missile Engineering Station began in 1963 with decisions that: 1) all hard-copy information materials, regardless of format, would be maintained and indexed at a single location; 2) the most extensive cross-indexing practicable with available data processing equipment would be provided, and 3) programming would maintain a statistical inventory automatically, from updated inputs for items added, changed, or deleted.

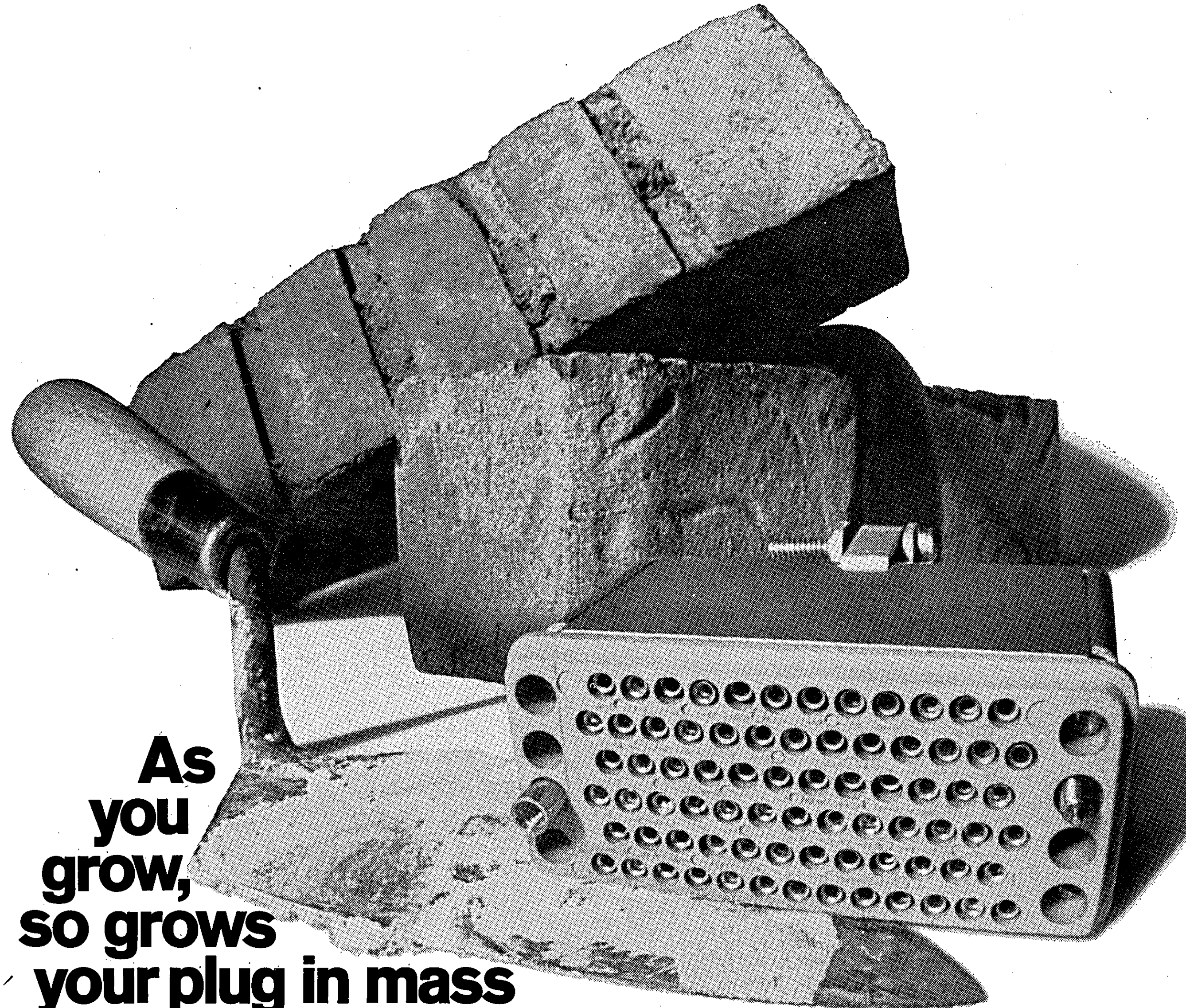
Achievement of an adequate mechanized process for the catalog listing of all books, periodicals, technical reports, report-type publications, charts, drawings, transparencies, training films, and both full-size and microfilm specifications required a development time period of nearly two years. Programming was initially available, but solutions had to be worked out for problems that were encountered.

The original design concept of maintaining a single basic index and sorting four ways to produce cross-index catalogs was found to involve excessive amounts of computer time. The problem was alleviated by dividing the basic file into four separate files in proper sequences.

Each book, drawing, film, or other item requires a control number for several uses. By abandoning traditional library shelf numbering systems, desirable simplification was attained in the programming. Starting with the number 1, accession numbers were assigned individually to inputs, and the accession number itself was used as a shelf number, for physical retrieval of the item upon request. Deletion of items releases the accession numbers for reassignment to new inputs, conserving file space, and maintaining numerical order. An updating change instruction to the program deletes all records of an obsolete item or maintains the latest revision and date for a needed item, operating by means of the accession number. Accession number printout serves as locator for an item, as it also lists title, date, and report number. The accession number listing is printed out quarterly, but a cumulative supplement is produced each week so that a complete statement of current library holdings is available.

The other three catalogs that have served to meet the

Commander Franke is director of technical data at the Missile Engineering Station, Port Hueneme, Calif. He is an Annapolis graduate and also has an MS degree in mathematics from Stanford Univ.



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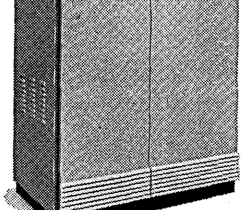

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needs of the technical library are a title printout in alphabetical order, a keyword printout, and an alphanumeric printout by report number. The title printout is a necessity for any library, because an item may be known to the requestor only by its title. The other two listings are of a specific nature to handle volume requests at Port Hueneme, because of the tendency to deal with certain topics identifiable by keyword, and because of a natural flow of information from other government agencies and vendors identifiable readily by their numbering methods for technical reports. What is of general interest about the mechanized system developed for the library at the Missile Engineering Station is the fact that considerable descriptive material can be made available with the program, in the form of cross-index catalogs in book form. The actual keywords and report numbers are specific for the needs of people engaged in ship missile systems technical support. Capabilities for cross-indexing in general are described in the portion of this article dealing with programming.

summary of results

The mechanized catalog production system, in less than four years, has grown to a content of over 100,000 accession numbers. The average physical retrieval time for a single catalog item is two minutes, as the accession numbers are immediately available. About 600 items per week are checked out on loan. Reference use of documents that do not leave the library numbers about 1,000 items per week, and requested copies of various kinds go out at about the same rate. Items are requested by telephone, Teletype, letter or memorandum, and in person by military and civilian employees alike. Requests from ships, other naval facilities and contractors account for 60% of the traffic, while nearly all of the remainder is attributable to use at the Missile Engineering Station itself.

Configurations of missile systems installed aboard more than 90 ships are maintained, with two or more types of missiles being used on some ships. The fact that hull numbers of each ship are listed in cross-indexes on hand has made possible accomplishments that are spectacular when compared with former methods of literature search. In answer to questions as to how many and what documents pertain to a ship under discussion, full tabulation sheets have been supplied to conferences on ten minutes' notice, a task that previously required 150 to 200 man-hours of work. The current configuration is completely documented, and in addition most research and development reports from both in-service engineering and vendors can be supplied immediately. This permits a quick look at existing installations, and at possible changes under consideration.

mechanized processing

Each incoming item is recorded by a member of the library staff on a loading form, illustrated in Fig. 1 (p. 48). The following details are recorded: 1) accession number, usually, but not necessarily, in ascending sequence of receipt; 2) department three-digit code number, indicating probable user, on station, shipboard, off-station at other facilities, or for use under security restrictions; 3) unclassified, or classification; 4) weapon system applicable, or "none"; 5) Julian date on which indexed; 6) type of change, as A, new accession, B, revision, etc.; 7) publication date of item; 8) report number. Two or more numbers for the same document, such as one familiar for Navy use, and another assigned by the Government Printing Office, are entered in card column 9 (shaded lines); 9) author's last name and initials; 10) title, or "title classified." For identification ease, the first word of a title is never abbreviated; 11) keywords, up to four in number.

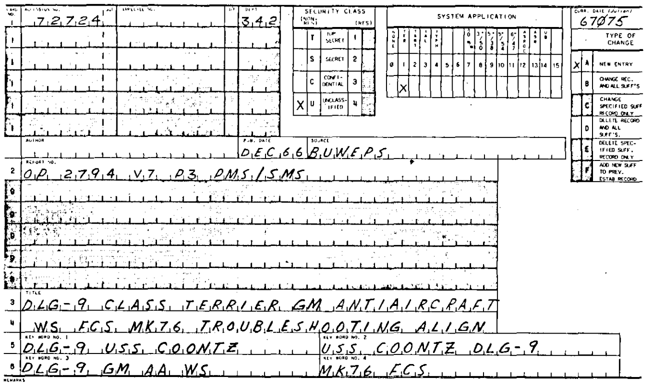


Fig. 1

A keyword may consist of several words, with or without abbreviations. Keywords are use-oriented and contained in a thesaurus derived from systems experience and from MIL-STD-12B. For example, one keyword for Guided Missile Launching System, Mark 7, Modification 1, is GMLS MK7MOD1. Additional entries of keywords are LAUNCHER MK7MOD1, TRAIN AND ELEVATION SYSTEMS, and ELEVATION SYSTEMS MK7MOD1. Many of the keywords are permutations of the terms within the original keyword. Keywords in the library system now total 105,560.

Other entries on the loading form are made when the computer program has added a suffix to the accession number of an item in the library. Such suffixes are, for example, A or B. A indicates a listing on the first line 9 of the original loading form, and B indicates a different report number for another copy of the same item.

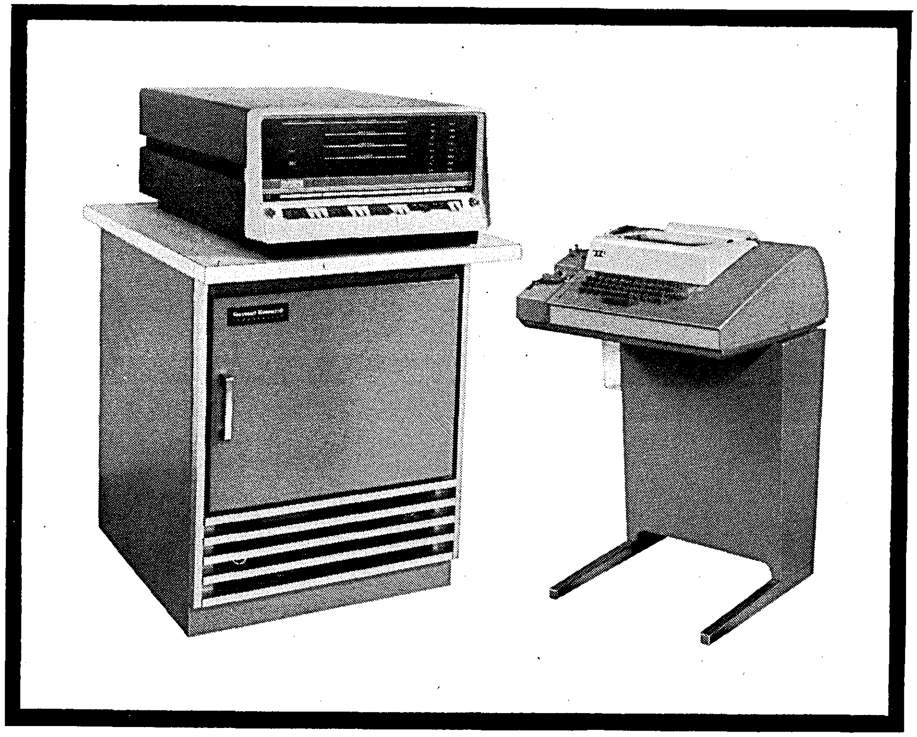
Other entries worthy of mention are made with regard to type of change. A type C entry indicates that a revision affects an accession number with a suffix. A type D entry instructs the program to delete all records of that accession number. A type E change indicates a deletion of an accession number with a suffix. A type F change will add a new suffix to an entry already in the record.

When the loading form is complete, it is sent to data processing to be keypunched, and the input is transferred after verification to a computer input tape. The item itself is prepared by the library staff for use, according to its format, and is filed by accession number.

The four output cross-indexes previously mentioned are printed and bound in catalog form, primarily listing accession number, title, keyword, and report number. Two copies are kept in the library for reference use, and single copies are distributed to reference focal points in particularly active departments. Normally, six copies of each of the four listings are available from the line printer.

computer programming

Available computer center for the current programs is a three-shift, shared-time installation operated by the Naval Construction Battalion Center, at Port Hueneme, and including an IBM 705 computer, 40K memory, with ten 727 tape drives and a 711 card reader, and an IBM 1401



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Major files are: 1) Teclib master file containing bibliographic and descriptive data for all items in the library, including all data listed on the loading form, arranged in sequence by accession number; 2) report master file, identical in content with the Teclib master file in format and content. Its sequence is by report number and accession number; 3) keyword master file, an inverted file containing classification, keyword, title, source, data, system application, and accession number. It is arranged in sequence by keyword; 4) title master file, containing the title and report number of all items in the library. It is arranged in sequence by title.

Flow chart for the programs is shown in Fig. 2. File changes in sequence by accession number are posted to

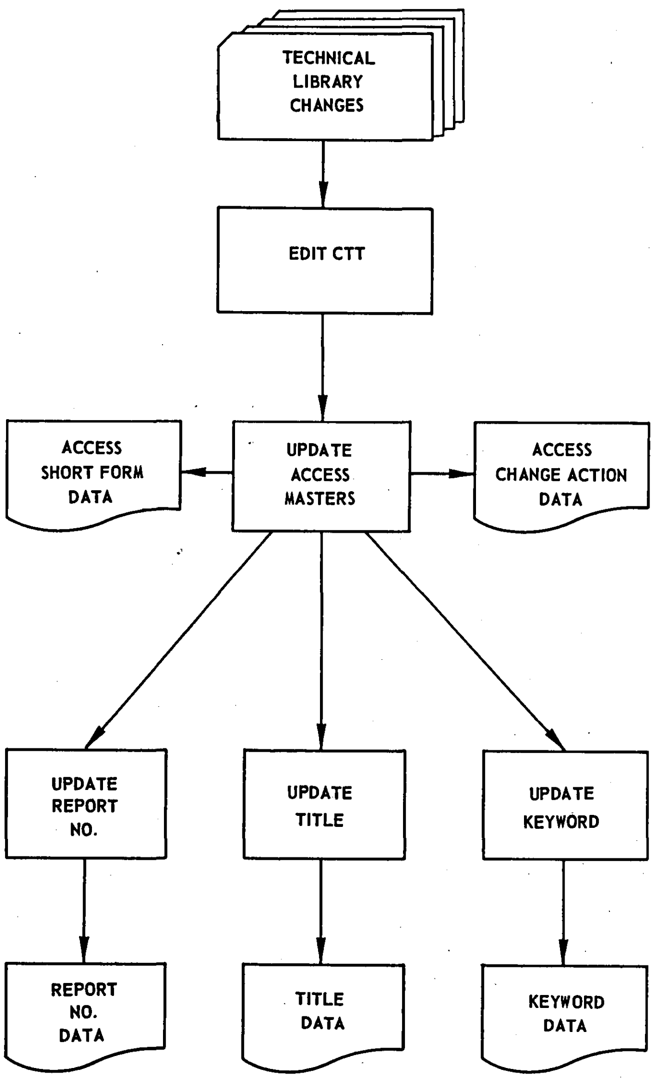


Fig. 2

the Teclib master file. Error messages are taped for printing. Updated records are written on three separate tapes—report number changes, keyword changes, and title changes—for input to the three other master files. The program runs about 0.6 hours weekly.

The accession number listing is printed from the Teclib master file. Accession changes generated by the Teclib maintenance program are printed weekly as a proof list for verification. Report number changes are sorted by report number and accession number, and are posted to the report master file. Error messages are taped for printing. The report number listing is printed weekly from the report master file. The program runs about 0.6 hours weekly.

Keyword changes are sorted by keyword, and are posted to the keyword master file. Error messages are taped for printing. The program runs about 0.2 hours a week. The title listing, or bibliography, is printed from the title master file monthly.

Programs are now being developed to use an IBM System/360 Model 40 computer recently installed at Port Hueneme. The system consists of a 132K memory, with six 9-track tape drives and two 7-track tape drives, two 2311 disc drives, one card reader, one card reader-punch and two high-speed printers. Increased capabilities of the 360 make possible expansion of the loading form, as illustrated in Fig. 3. Note that card controls are expanded for growth potential. Hull numbers are called out with

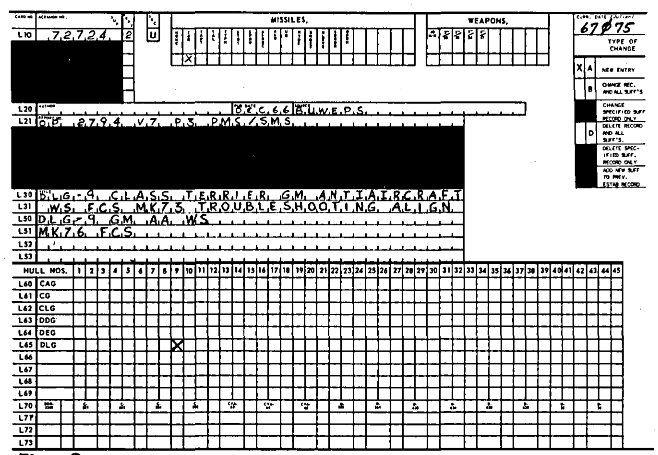


Fig. 3

minimum manual effort. Keywords are expanded for internal program compatibility. Provision is made for separate indications of missile systems from weapons systems of traditional naval armament.

Flow chart for the 360 programs is shown in Fig. 4 (p. 52). The 360 makes possible the introduction and retrieval of additional data, most obvious of which is the author and date printout on a regular basis. Other advantages are increased editing and file-maintaining mechanization, availability of new reports expected to bridge existing gaps with other Navy records, retention of data not previously accessible, shorter hours of shared-computer time, and minimum conversion effort, because existing data is compatible with expanded operation.

related facilities

Three Missile Engineering Station facilities related to the technical library, but dependent on separate mechanization, are the federal specifications file, the engineering drawings file and the charge-out/circulation file.

The federal specifications are kept on 16mm microfilm, indexed alphanumerically by an independent contractor. Some 80,000 documents are stored with a standard reader-printer in about ten cubic feet of library space. Fast mechanical operation facilitates reading or printing a hard copy of any desired specification.

The engineering drawings are maintained as microfilm records at the station, using Department of Defense aperture cards with keypunched address. With more than 1,650,000 drawings, the file has its own computer system and environmental controls to prolong film life. This

voluminous file supplements the printed illustrations included in library documentation.

The charge-out/circulation file for the library has been punched-card oriented since 1965, although it has not been computerized. With a keypunch and card sorter, it was found useful to obtain printouts of delinquent items. In 1966, the security task of accounting for classified documents was added to the charge-out operation, using a color-coded system of data cards, and it was found practicable to eliminate more than half of the manual tasks of document security with which every military facility and almost all defense contractors are charged.

summary

The Missile Engineering Station developed a mechanized catalog production system for all information items, regardless of format, at a single location, indexed by IBM 705 computer processing into four cross-reference catalogs

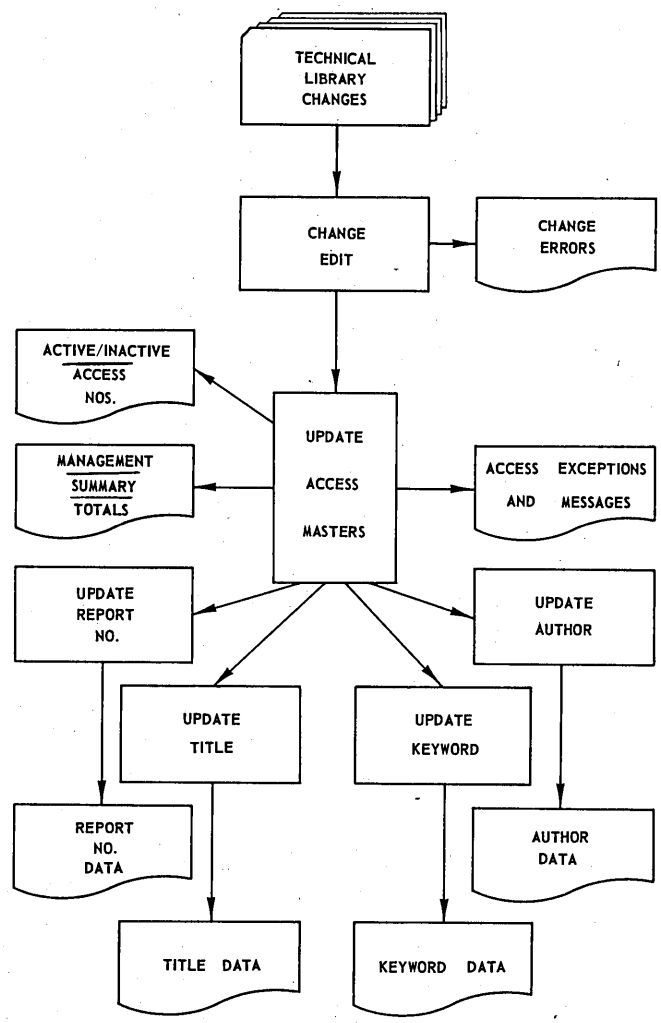
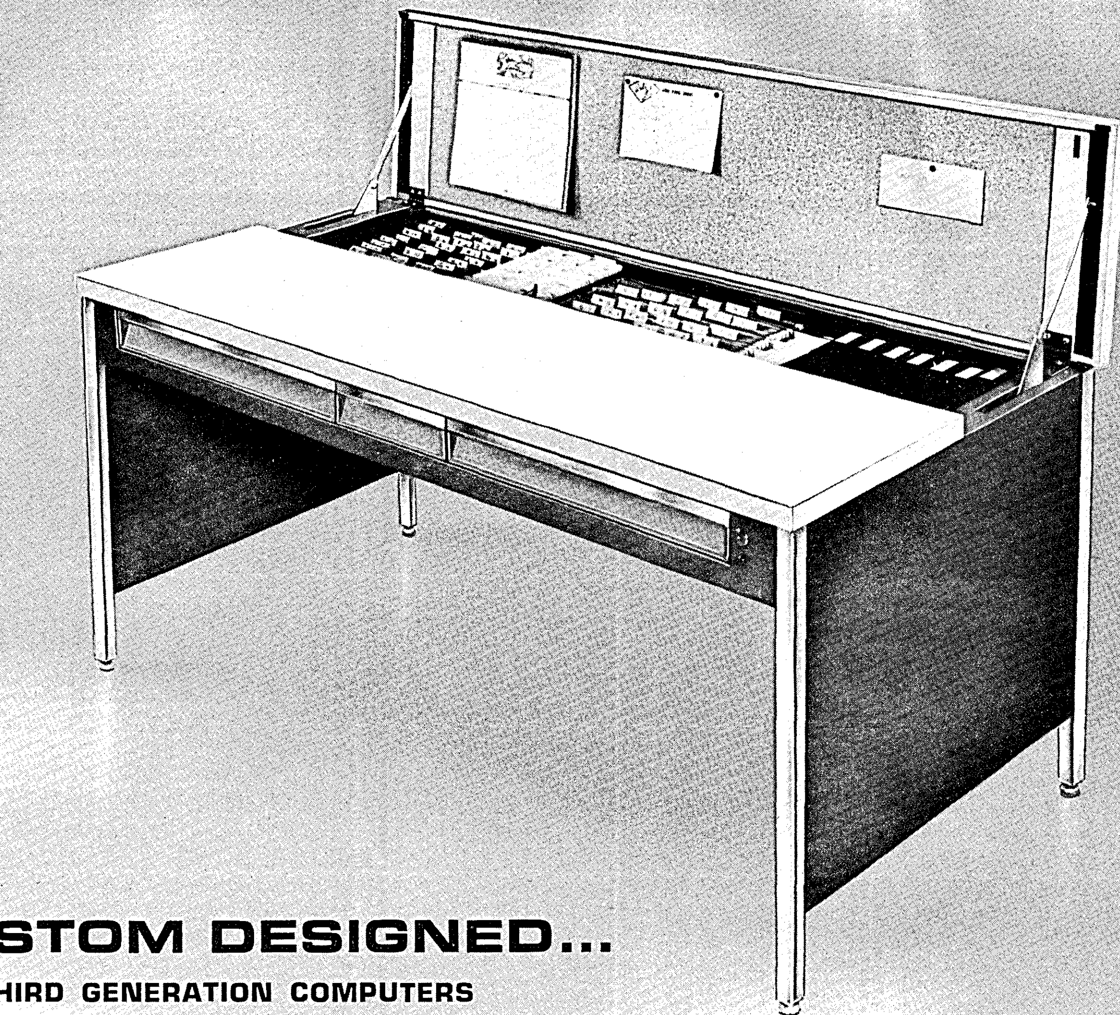


Fig. 4

in book form. A statistical inventory is maintained automatically. Physical retrieval time for masses of related data has been cut to a small fraction of that required by traditional library methods. Economies effected have led to more ambitious programming, using an IBM System/360 computer, with improved results. The facilities are available, by prearrangement, to interested organizations that may wish to obtain detailed information by observation. ■



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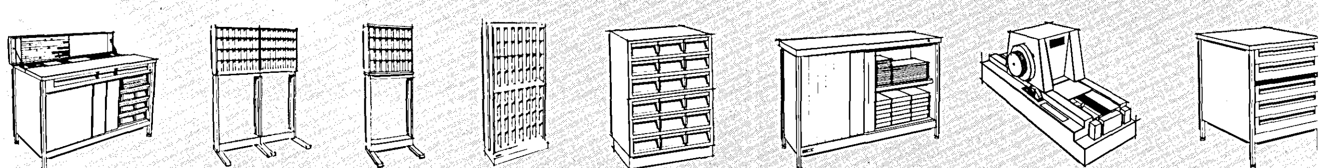

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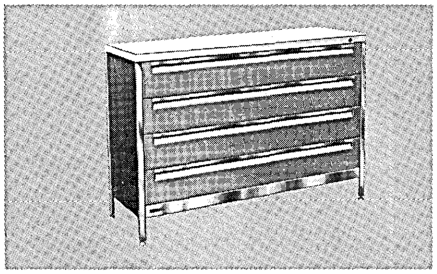

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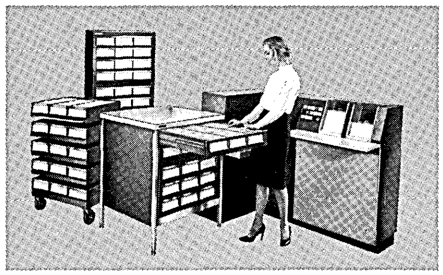

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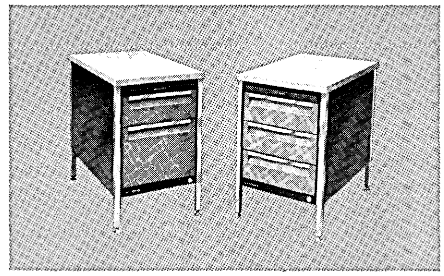

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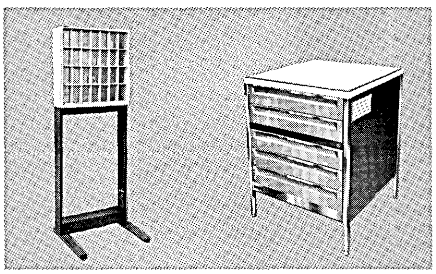

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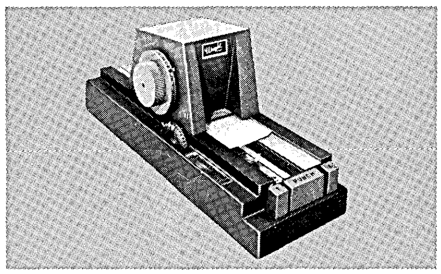

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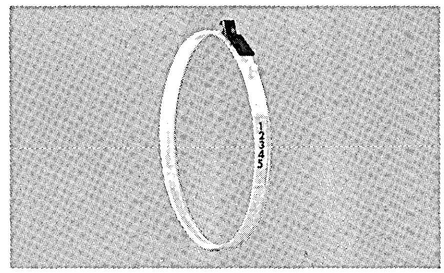

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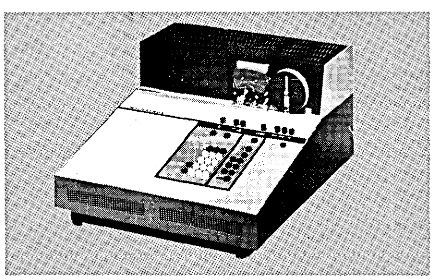

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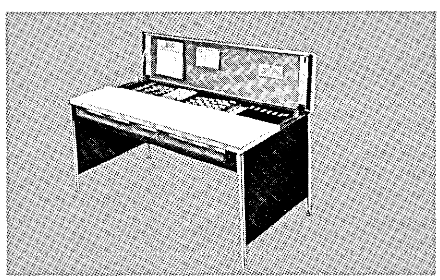

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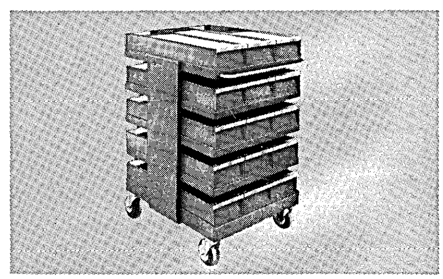

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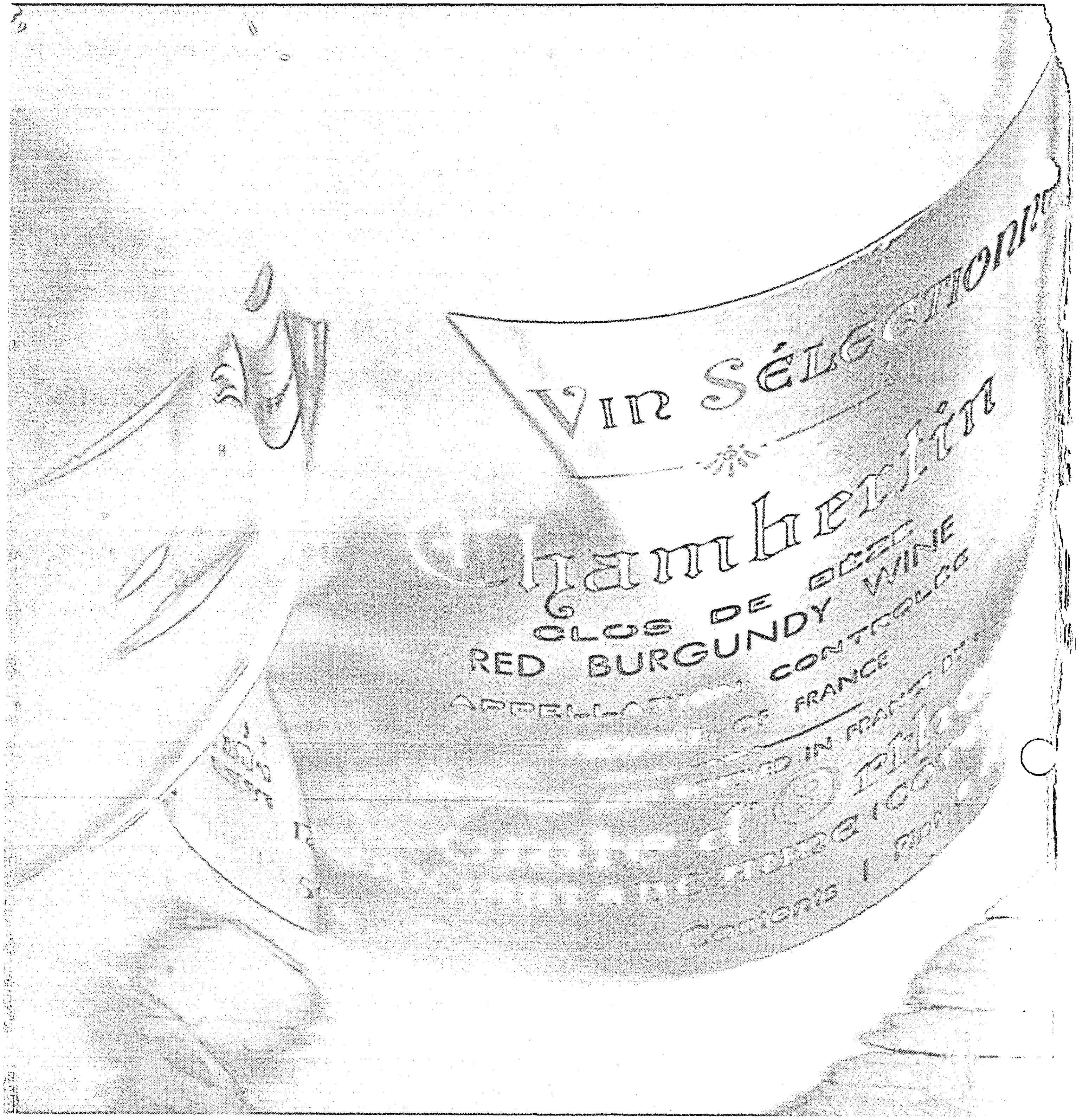

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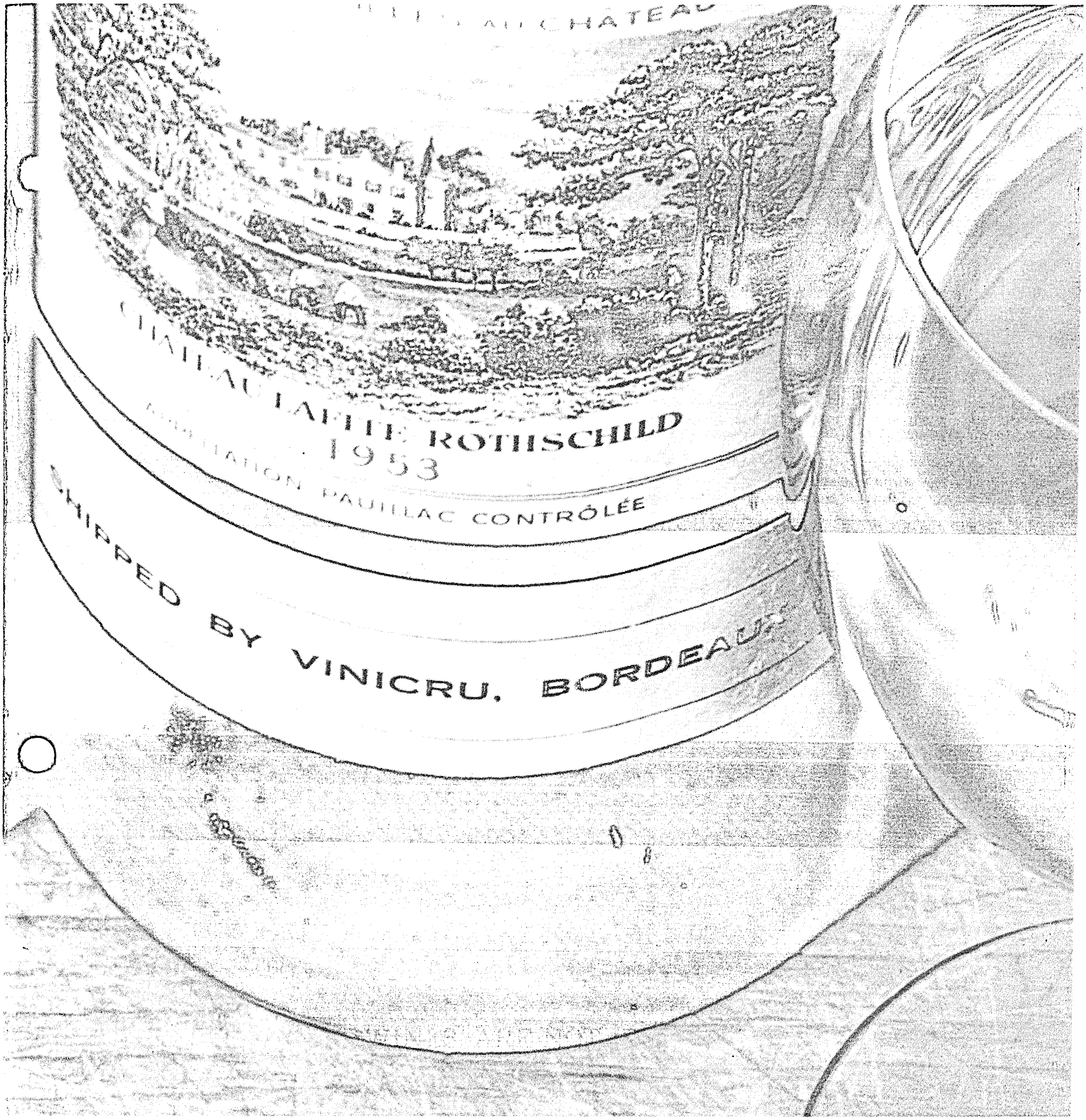

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WHAT IS SYSTEMS PROGRAMMING?

a home study course

by FRED H. OTTE

The apparent difficulties of understanding systems programming can be cleared up quickly if an analogy is considered using a more familiar environment, such as food preparation. Instead of computers and programs we'll use stoves and recipes.

terminology

To begin with, we must define our terms. Kitchen is renamed SPOON for Systematic Processing Operation Of Nutrition. The stove becomes the CCU for Central Culinary Unit. Since there are gas stoves and electric stoves, we must differentiate between gas driven (GDCCU) and electrically driven (EDCCU). Since there might be at least one potential customer using a wood stove, we will also provide full support for a wood driven WDCCU. It is conceivable, of course, that some CCU's have the ability to be powered selectively or simultaneously by one or more fuel sources, or a combination of two or more CCU's may be installed, which may or may not be powered uniformly.

To properly handle such configurations we will have a CCUVAR (Central Culinary Unit, Variable Powered).

In addition to the CCU, the SPOON will have a number of optional peripheral devices which we conveniently name POTS for Pans On Top of Stove, PANS for Pots for All Needs and Soups, OVEN for On-line Variable Energy Nucleus, etc. The input will mainly come from Containers for All Necessary Somethings (CANS) and the output will more often than not be self-defined as GARBAGE.

language design

Our software must be flexible enough to encompass all kinds of hardware configurations, from a large hotel installation to the bachelor's hotplate. An automatic processing system will only do what it is told to do, so to make our system work we need recipes. We differentiate between user recipes and systems recipes which are written by user recipe writers and systems recipe writers. Adequate software enables us to produce any kind and any volume of food by saying EAT and DRINK and by providing a few parameters. The formula for the number of parameters needed is approximated as:

$$16^{256-n}$$

where n ranges from 0 to 256. For example:
n = 1 for a 12 course dinner for 6000 persons,
n = 256 for one slice of toast, medium brown.

symbolic language logic

All cook code is written in Basic WITCH, which is then processed by the WITCH assembler producing one or more relocatable object WITCH recipes, which are processed by the Linkage Switcher to produce one or more absolute subject WITCHES, which finally are loaded by SWITCHFETCH to in turn produce absolute and executable dual-switched WITCHBREW. It resides in protected DISH. It is imperative for the recipe writer to know at all times which SWITCH switches which WITCH.

organization and management

Appropriate Cook Libraries (CLIB) are provided for dynamic recall. This, of course, necessitates the creation of a Cook Library Catalogue (CLIBCAT), which is kept in removable frying pans under the raised floor. To retrieve the CLIBCAT we need a directory called Catalogue Synchronized Information Table (CATSIT), which provides real-time access at all times, because a pointer to the active CATSIT is always provided at the entry point to SPOON. The unique system of integrated libraries provides us with a random addressability to an infinite variety in diet.

Components are stored with the macro CRAM (Calculated Risk Access Method) and when an item can no longer be located it can be deleted with the macro GUFD (Give Up For Dead).

generalized, flexible recipes

A typical recipe, as used before automation, is inflexible, inaccurate and confusing. It may look like this example:

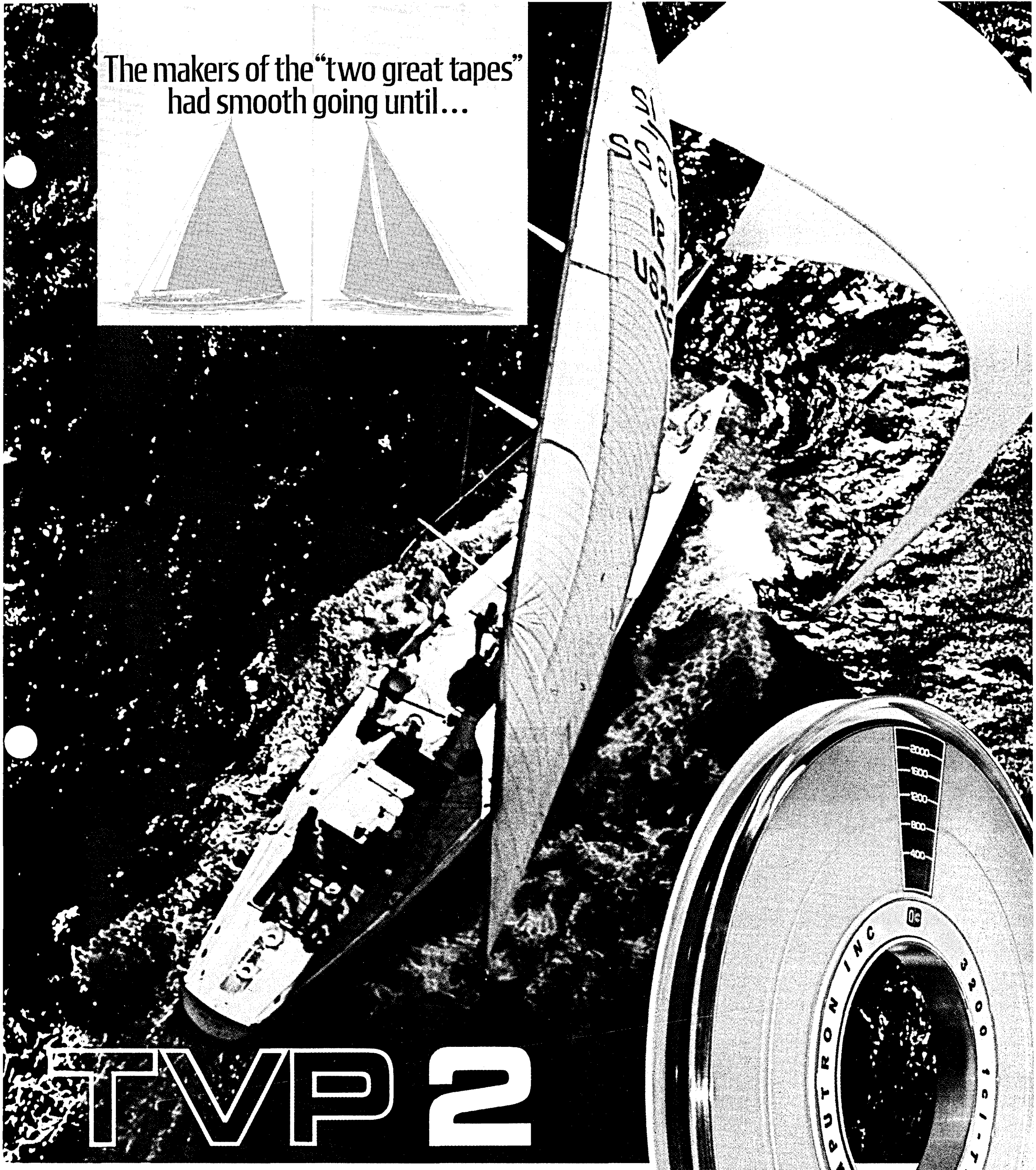
2 large Bermuda onions
1 cup whipping cream
½ cup shortening
1 teaspoon salt
2 cups vinegar
1 egg, separated
2 tablespoons sugar
Bake at 325° F for 1 hour 15 minutes
Makes 25 servings

The SPOON system, in contrast, features an easy, logical and flexible notation for the problem recipe writer. It provides a generalized model recipe which applies to all the world's recipes.

the model recipe

Ingredient Division
UNIT = L (large)
1. N*UNIT = M (medium), (geographical origin, coded)
UNIT = S (small)

(Continued on p. 63)



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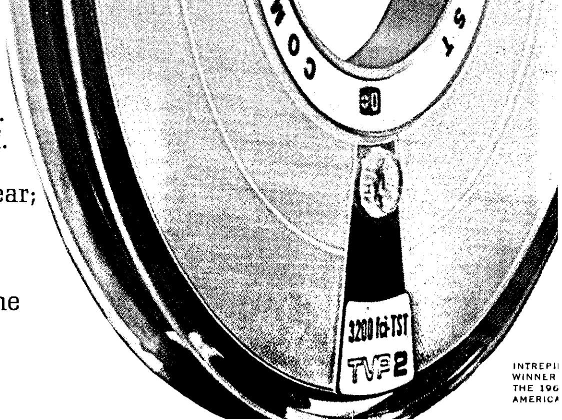


INTREPI
WINNER
THE 196
AMERICA

$$\left\{\begin{array}{l}\text{fruit}\\ \\ \text{object}\\ \\ \text{subject}\end{array}\right\} \begin{array}{l}\text{sliced}\\ \text{whole}\\ \text{chopped}\\ \text{boiled}\\ \text{separated}\\ \text{other}^{**}\end{array}$$

$$\text{2. N} \left\{\begin{array}{l}\text{TS (teaspoon)}\\ \text{P (pound)}\\ \text{C (cups)}\\ \text{SS (soup spoon)}\\ \text{TBS (tablespoon)}\\ \text{QT (quart)}\\ \text{PT (pint)}\\ \text{OZ (ounce)}\end{array}\right\}, I_1, I_2, I_3, \text{CD} = \text{condition}^{***}$$

Environment Division

$$\text{DO,} \begin{array}{l}\text{B (bake)}\\ \text{F (fry)}\\ \text{BR (broil)}\\ \text{CK (cook)}\\ \text{S (steam)}\\ \text{R (raw)}\end{array}, \text{T} = \begin{array}{l}\text{(time in}\\ \text{decimal}\\ \text{milliseconds)}\end{array}, \text{HT} = \begin{array}{l}\text{(temperature in}\\ \text{3-digit hexadecimal}\\ \text{centigrees)}\end{array}$$

Procedure Division

USE $P_1, P_2 \ldots\ldots P_n, P_n{}^{*}\, P_n$ (in this order)

Output Division

$$\text{PORT} = \text{N (portions), SERV} = \left\{\begin{array}{l}\text{P}\\ \text{C}\\ \text{S}\\ \text{B}\end{array}\right\} \begin{array}{l}\text{plate}\\ \text{cup}\\ \text{saucer}\\ \text{bowl}\end{array}$$

Legend:

N	quantity, expressed in binary numbers
I	ingredient, coded
CD	condition, coded
P	procedure, catalogued (may be added, subtracted, multiplied, and divided)

Below is our example as coded in Basic WITCH:

```
INGRED
10, UNIT = L, LOC 348 (FOREIGN), WHOLE
01, C, I9684WC, , , (CD = FRESH)
.1, C, I1489SH,
01, TS, (SCB = SCB1)
10, C, I003IVG, , , (CD = SOUR)
1, UNIT = M, , , (CD = SEP)
10, TBS, (CHB = SUG2)
ENVIRON
B, 75, (T = 4500000), (HT = 0A3)
PROC
USE = P642, P391* P005+P1619, P8, , P846/2
OUTPT
(POR = 11001), SERV = P
```

This example illustrates that inherent in this system is not only clarity but also a considerable amount of time-saving.

multitasting

To more efficiently utilize our system we must abandon the idea that only one meal is prepared at a time in favor of multitasting. Under this system, which is optional, but strongly recommended, many meals are being prepared concurrently. The same facilities are utilized, by many operators harmoniously and asynchronously. Operators or meals not immediately dispatched can be stored temporarily or permanently in the Library Of Stored Tastes (LOST).

The Taste Supervisor will control the system by allotting time slices to each recipe under process and by sharing resources, so that one POT might be allocated to cook a layer cake and shrimp sauce simultaneously. Increased throughput results.

operation

Various dials on the CCU control console allow the operator to communicate with the automatic operation. This feature has been included to give the system an opportunity to interpret its possible malfunctioning as an operator error.

Black output will indicate that the system is in a loop and that the product has been overcooked. As an added service the system will, in such a case, type out names and addresses of nearby restaurants.

As a special feature, a manually operated device with 4096 sequentially numbered pushbuttons can be attached. It is called PANIC for Pick A Number If Confused and is used only in emergency.

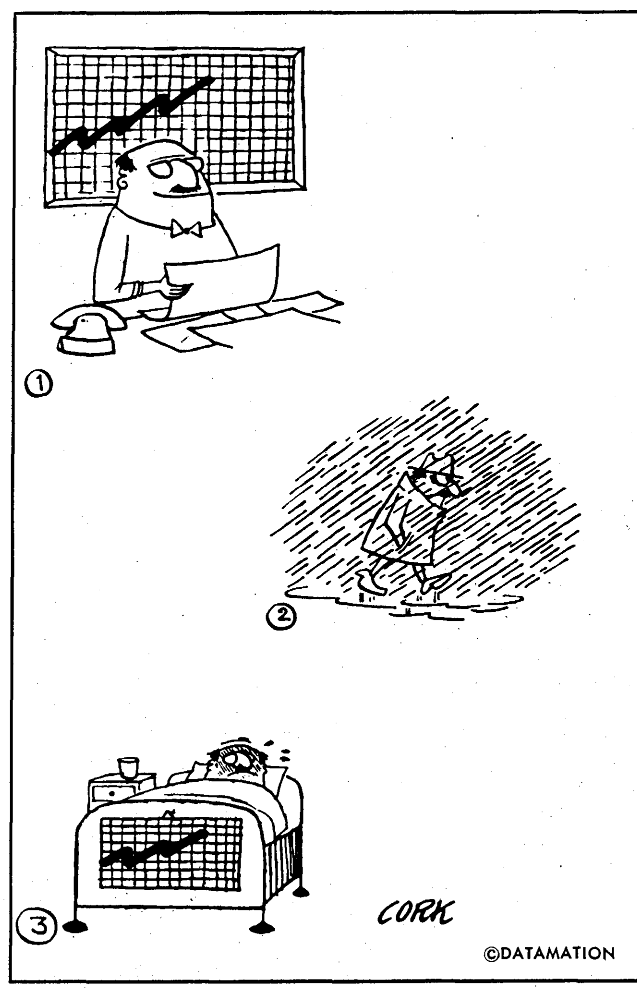
summary

The system provides us with aids that enable food preparation to be expressed in a language and terms that can be easily understood. It includes:

Facilities for easily storing, retrieving and tasting ingredients and recipes.

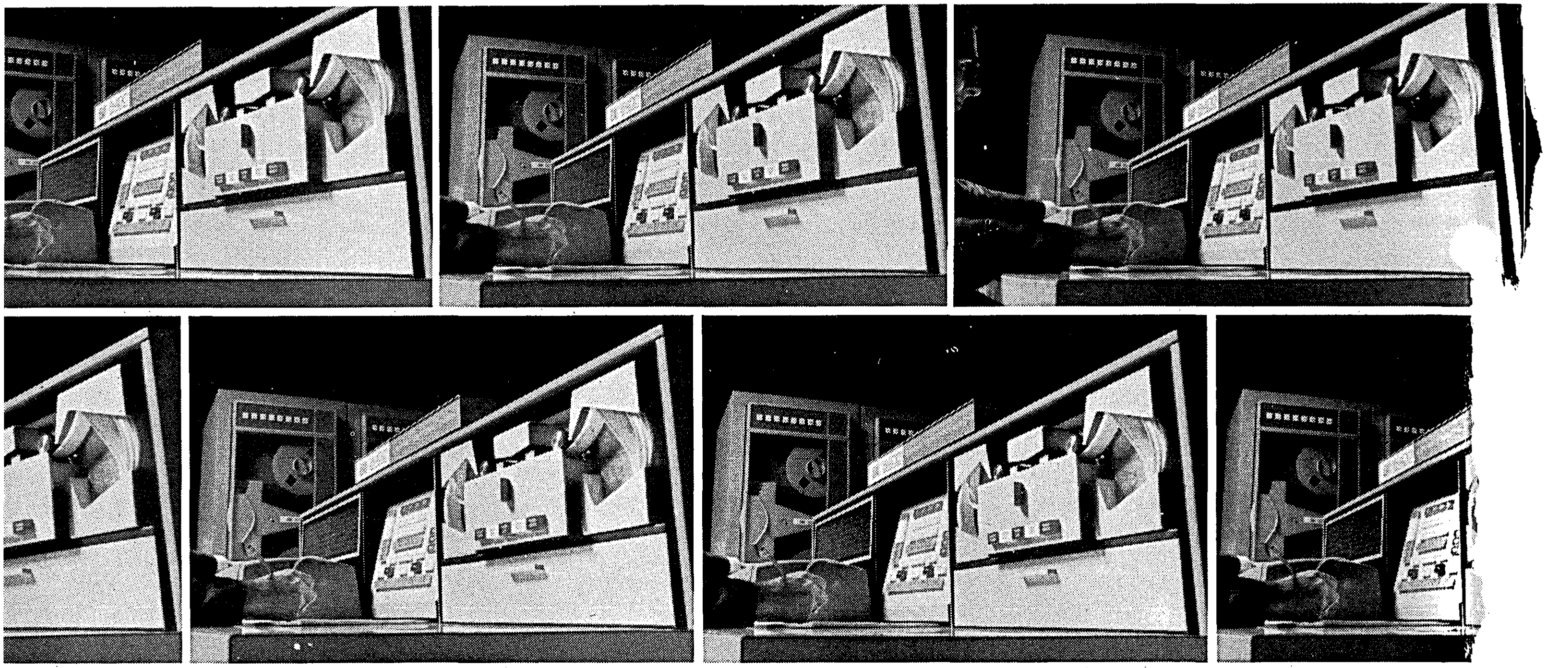
A system of control that relieves us of all concern.

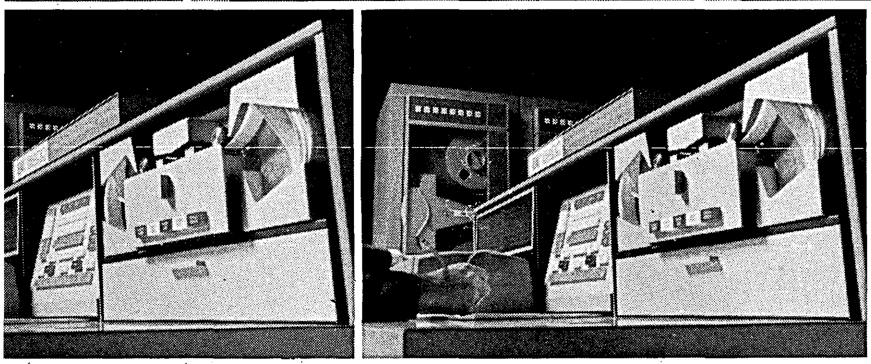
An open-ended design that ensures compatibility as food consumption grows or another spouse causes design changes. ■



** live seafood subset available in extended system

*** excluding dead fish, except in systems exceeding 32K.





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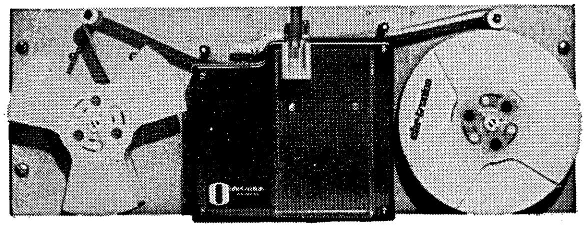
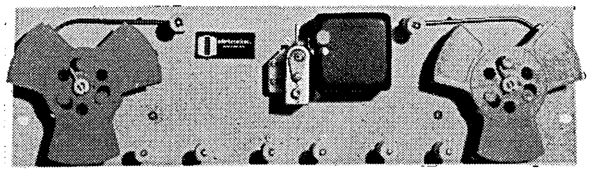
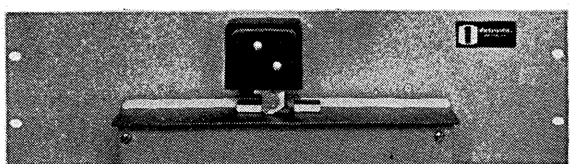
CIRCLE 35 ON READER CARD



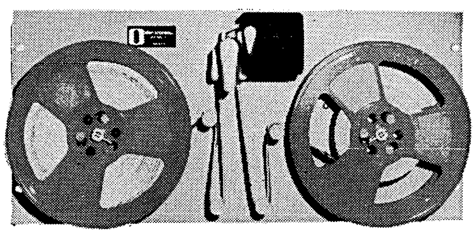
Model 110, Paper Tape Punch . . . punches standard 5 to 8 channel paper tape asynchronously at speeds up to 30 CPS. Powered by continuously running induction motor. Error detection achieved by parity checking switches. Tape can be back-spaced. 7″x 19″ panel, 24 or 48 VDC. **Price: $599.00**



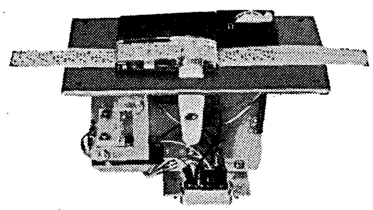
Model 119R, Paper Tape Reader . . . reads up to 8 channel punched paper tape with spooling mechanism for bi-directional tape supply and take-up. A switch out-put for tight tape and end-of-tape is provided. Panel is 3½″ x 19″ with optional 24, 48 or 90 VDC. **Price: $578.00**



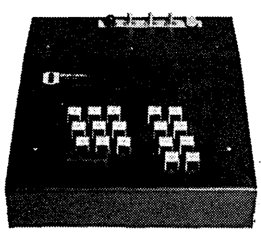
Model 131, Edge-punched Card Reader . . . bi-directional capability to read single, hand-fed edge-punched cards that have standard 8 channel paper tape codes punched along edges. Same mechanism as Model 119R. **Price: $457.00**



Model 121, Paper Tape Reader . . . 60 CPS with inclusive solid-state Drive-Pak at lowest cost! Advanced reader head features full 180° tape surface. 750′ reel supply or take-up. Tape Lever indicates non-reading or broken tape. Panel is 8¾″ x 19″ with 24, 48 or 90 VDC. **Price: $605.00**



Model 153-60, Flatbed Reader . . . new, speedier reader at 60 CPS. Unidirectional starwheel sensing device permits mounting on horizontal surface. Panel 4½″ x 5¾″. Same mechanism as Model 121. **Price: $413.00**



Model 117, Encoding Keyboard . . . 18 key . . . converts key depressions into coded (8 level) arrays of switch closures designed to interface with tape punches, printers, plotters, computers or other automatic machinery. Any code configuration can be supplied. Keys can be mechanically or electrically interlocked. **Price: $435.00**

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CIRCLE 36 ON READER CARD

SAM ALEXANDER, 1910-1967

"Sam Alexander was the most accessible boss I ever worked for," recalls one of his associates. "You could go into his office at any time and talk to him; he'd drop whatever he was doing, no matter how important it was. Back in the early days, Sam's office had windows made of one-way glass. Characteristically, the glass was transparent from the outside, rather than the inside. He wanted people to know when he was in."

Another associate remembers a technical meeting in Paris when she counted the number of times Sam met someone he knew. "When I stopped counting, early in the afternoon, he had shaken hands 500 times."

But Sam Alexander's most memorable characteristic was his mental agility, his talent for "jumping to conclusions while most of us were still trying to sort out the facts," says Russell Kirsch, a National Bureau of Standards mathematician who worked with Alexander for several years. "Many people jump to conclusions, of course, but Sam's conclusions were usually correct."

Sam Alexander died of cancer Dec. 19, 1967, at the age of 57. He "probably influenced, more than any other individual, the introduction and development of automatic data processing techniques and systems into the federal government," according to his official biography. Alexander did much more than that, however.

He was one of the first, back in the natal days, to see the potential uses of computers outside the scientific community, as a planning and accounting tool. Throughout the '50's he pioneered dozens of applications which helped create major markets for software and hardware later on. He also guided many of the marketers—for example, IBM's Manny Piore, SDC's Wes Melahn, and Fred De Hoffmann of General Dynamics. They were among the bright young engineers and mathematicians who worked under Alexander in the NBS Electronic Computer Laboratory and its successor, the Data Processing Systems Division. Today, these operations are more familiarly, and perhaps more accurately, referred to as "The Sam Alexander Post-Graduate School."

Despite his accessibility and warmth, Alexander was not universally loved and admired. Like many men of conviction, he made some enemies. At a hearing on the Hill once, for instance, Alexander indicated to one questioning Congressman that he doubted if the Representative had the background to understand the answer to his question. And he was strongly criticized for his attempts to maintain an NBS project to build its own computer in recent years. His insistence on this pilot project was completely contrary to the thinking of Jack Brooks, leading Congressional edp watchdog, and Norm Ream, the man Brooks picked to run the NBS Center for Computer Sciences & Technology, bypassing Alexander in the process.

Alexander was born in Wharton, Texas, and earned degrees at the University of Oklahoma and MIT. He joined NBS in 1946 after spending the previous five years with the Navy and with Bendix Aviation Corp. developing electronic instrumentation. His first major assignment at the Bureau was to write the specs and supervise the procurement of Univac I, the machine Eckert and Mauchley had been commissioned to build for the Census Bureau.

"At that time," says an official history, "it did not appear unreasonable to expect such a system to be in operation by late 1948."

But by 1948 Eckert and Mauchley were in serious trouble. The bureau decided to help them out by building,

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Flexibility means Model 25 will even run existing IBM 1401, 1440 and 1460 programs without reprogramming. It means Model 25 can use high-level operating systems as well as PL/I, FORTRAN and COBOL—the same program languages used in larger systems. It means utility programs are ready and waiting in IBM's program library—as are System/360 application programs tailored for such industries as finance, manufacturing, process and distribution.

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That's Model 25... a system to grow with.

IBM®

SAM ALEXANDER— 1910-1967 . . .

in-house, an "interim" computer on which new approaches could be tried. The result was the Standards Eastern Automatic Computer. SEAC, despite its "interim" label, remained in operation 14 years, and despite its limited original mission became the most versatile of the first-generation computers. It may also have been the most significant one.

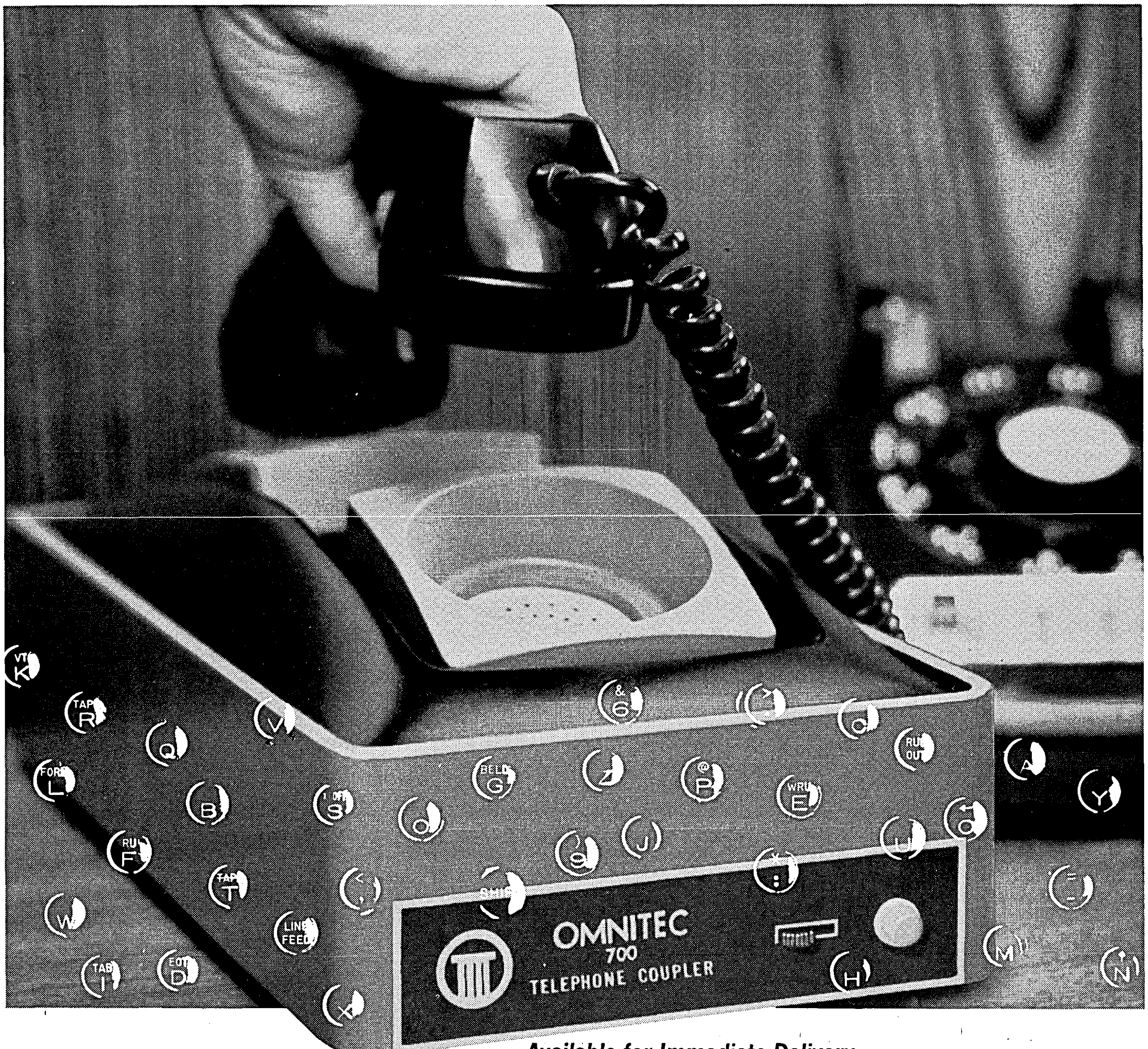
SEAC was the first to utilize a stored program, the first to make extensive use of diode logic, the first to employ semiconductors as logic elements. Even more important, perhaps, SEAC performed reliably from the day it was completed in 1950. It demonstrated to potential computer users inside and outside the government that dependable computers could be built despite the troubles that other developers were having.

Alexander and his team at NBS used SEAC to explore, and advance, every major field of data processing art. They developed new components as well as new applications, and SEAC mothered many children, each of which made additional contributions.

Shortly after SEAC was built, it produced a cost-effectiveness study of Air Force operations; this was at least a decade before the term or the basic concept was popularized. In 1954, NBS connected SEAC to a remote terminal and provided the Army Quartermaster Corps with an on-line real-time system for selecting low bidders on military contracts. In 1956, SEAC tested one of the first computerized information retrieval systems when it made a topological survey of Patent Office files.

Besides directing the bureau's computer development effort, Alexander consulted with most of the other developers, both in this country and abroad. In 1956, Sweden awarded him a distinguished service medal for his labor on their behalf. He also received two gold medals from the U.S. Department of Commerce.

Alexander's last honor, bestowed a few months before his death, was the Harry Goode Memorial Award. Only five others have received it, and all but one of these shared the honor with someone else. It was a fitting tribute to a man who, in the words of the citation, had made "outstanding contributions to computer technology and government applications over the past 21 years." ■



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CIRCLE 40 ON READER CARD

news briefs

ADAPSO LOSES GROUND IN ITS WAR WITH THE BANKS

The Association of Data Processing Service Organizations (ADAPSO) lost a battle last month in its effort to prevent bankers from operating data processing service bureaus, but a spokesman says the war is far from over. The association plans to appeal, "as soon as possible," a Jan. 9 decision by a federal court judge in St. Paul, Minn., who ruled that ADAPSO and a local service bureau, Data Systems, Inc., have no "legal standing" to block American National Bank and Trust Co. of Minneapolis from providing contract data processing services. The ADAPSO spokesman thought the appeal could go to trial "as early as next May."

The case is significant because banks throughout the country are providing such services and more are planning to do so.

A closely related suit is now being tried in Providence, R.I. The plaintiff there is the Wingate Corp., a local dp service bureau. The defendants are the Industrial National Bank of Rhode Island, which does work for the city of Providence, and the Comptroller of Currency, who regulates the national banking system. He is also a defendant in St. Paul. The American Bankers Assn. has entered both cases as a friend of the court.

Each bank set up its data processing service bureau under authority first granted by the Comptroller of the Currency in 1959. For many years the courts held that private parties were not legally entitled to protest such federal government actions through lawsuits. But recently, individuals and groups have been granted legal standing to oppose banks which operate travel agencies, sell insurance, and deal in revenue bonds. These operations, like the service bureaus, stem from authority granted by the comptroller.

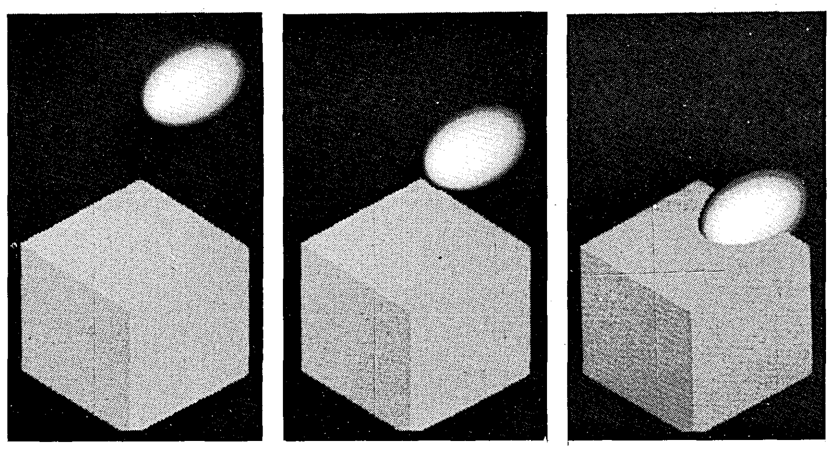
If last month's decision in St. Paul is overturned, service bureau operators will then have to prove that selling contract dp services is not authorized by the National Bank Act.

Last month, ABA submitted a brief in the Providence case which contended that Congress believes that bank service bureaus *are* authorized under the act. The brief explained that last year, when a bill prohibiting the banks from selling lottery tickets and performing related services was enacted, Congress specifically removed data processing from the list of such prohibited services. If banks didn't have the authority to provide these services, asked ABA, why would Congress go through this exercise? To support its conclusion, the ABA quoted extensively from the Congressional debate on the lottery bill. The most relevant statement came from Rep. Tom Ashley, Ohio Democrat:

"The deletion . . . of the prohibition . . . against the performance by banks of data processing services in connection with lotteries is not . . . in itself a grant of authority to perform such services," said Ashley. "Such authority must be found elsewhere in the statutes, primarily in the National Bank Act . . . and in the state banking codes . . . It is appropriate, however, to point out that the prohibition would have been unnecessary and meaningless unless there was authority elsewhere."

The National Bank Service Corporation Act, passed in 1962, is also involved. It permits banks to form dp subsidiaries but prohibits them from engaging "in any activity other than the performance of bank services for banks." ABA insists that this language applies only to the subsidiaries, not to the individual banks per se. Wingate

3-D SIMULATED GRAPHICS OFFERED BY SERVICE BUREAU



Mathematical Applications Group, Inc. (MAGI), White Plains, N.Y., has developed a graphics system that uses a computerized program to simulate a camera, light sources, and an object, to produce a three-dimensional representation on a CRT display.

In the FORTRAN program, the object to be projected is converted into mathematical representations on a punched card with additional data on the simulated light sources, camera position and focus. The cards are then fed to the computer—the company is currently using a Philco Transac with 120K 8-bit-byte memory. The computer traces the simulated light rays from the illumination sources to the simulated object, and to and through the simulated camera lens to a point on the CRT. When the calculation is complete, the intensity of the light at a number of points on the tube is determined.

A real camera then photographs the image on the CRT and produces a picture of the object. As illustrated in the photograph, an action sequence of two objects can be produced by changing the data. The third photograph shows no "hidden lines" (of the "box" behind the "egg") because of the technique of simulating the paths of the light rays. (Other attempts at three-dimensional graphics have often had a "hidden lines" problem because the program calculated an equation of lines.)

MAGI plans to offer this system to the public this spring on a service bureau basis, running it on either a System/360 or a Control Data 6600. For information:

CIRCLE 124 ON READER CARD

claims that the legislative history of the National Bank Service Corporation Act constitutes "a clear recognition by Congress that national banks are not authorized to (provide) data processing services for the public at large."

ADAPSO has vowed to carry its argument to the U.S. Supreme Court if necessary. ABA has done likewise.

IBM ADDS DUAL 65 TO SYSTEM/360 LINE

The 360/65 multiprocessing system is a direct swat at Univac's 1108 II, announced in 1965. The two-cpu system, to be delivered first quarter 1969, is an answer, says one user, to IBM's "increasingly nervous scientific customers." It also aims at commercial buyers who need a larger data base, more reliability, and more efficient management of multiple-computer installations.

The 65's used are essentially the same internally as the stand-alone counterpart, but through a combination of hardware and software modifications the multiprocessing system will share all resources. Job processing is not dependent on any one cpu; it can be started on one cpu and continued on the other. A conflict (failure or busy signal) on one processor's channel is automatically bypassed and an alternate channel is taken through the other cpu to reach a peripheral device.

Specifically, hardware changes include:

The memory boxes (up to four of 256K bytes each) will have second leads to permit connection with both cpu's, and, of course, the cpu's will be connected to each other. A configuration panel will permit allocation of I/O devices and memory and permit change of addressing scheme in assigning memory. Through this panel, the systems can be made to run as independent 65's as well. Floating address switches are added to permit assigning the memory boxes in any order. And the mechanism for instruction set systems math (SSM) has been changed to a multiprocessing mode to control simultaneous or sequential execution by the cpu's in the supervisor.

Software features include the following:

The entire system, which requires a minimum 512K bytes, uses one control program. Programming support is OS/360 Multiprogramming with a Variable Number of Tasks; the version containing multiprocessing features (requiring 100-200K for MVT, about 32K for multiprocessing) will be ready in Feburary, 1969. The VARY command in the multiprocessor has been extended to permit the operator to tell the system not to use any component that is down; thus the system can continue operation without key elements, from the cpu to an I/O device. (At program load time, however, a hardware feature senses what is available for operation.) A new program addition to both the 65 and the 65 multiprocessor is recovery management for OS, which recognizes and in some cases corrects intermittent failures in the cpu and channels. This program, extended VARY, and the online test capability in the executive (standard in 360's) are intended to enhance reliability of the system.

Other major capabilities of the system include insuring that the tasks being executed are highest priority, inter-cpu communications on abnormally terminated tasks, and communication to the operating cpu when the other goes down.

Several features of the new configuration are now being tested. Reportedly, 65 users can convert to the multiprocessing configuration, with field modifications. A typical system rents for $125K/month; purchase price is $5.6 million. For information:

TO BURROUGHS GO PHASE II SPOILS

The extra eight months between the first, rescinded award of the Air Force Phase II contract to IBM worked most to the advantage of Burroughs, which walked away with the award on the second go-round. The result is a $54 million difference between the equipment cost (based on 135 units) of the IBM systems—$114-plus million—and Burroughs—$60 million. The Air Force figures that the net savings is $36 million because the delay cost the government over $2 million a month in the operational savings to be accrued by Phase II implementation.

It was basically a Burroughs 3500 computer and Friden 7311 terminal configuration which beat out RCA's 7025 and 35, IBM's 360/30 and 40 and Honeywell's 200 series (rumored to have been rated in that order). As opposed to the first time, when IBM was the only bidder that successfully passed all requirements, all four manufacturers were responsive this time. And the Air Force, though not providing details, noted that all systems and bids were significantly better this time. Some vendors increased memory by 100%.

Honeywell, said to be first runner-up last time, was the firm whose protest to the Government Accounting Office and Congress led to the rescinding of the IBM award last July. Under the stipulations of GAO procurement procedures, the Air Force was persuaded that the $65 million price discrepancy between IBM and its competitors was sufficient to warrant further investigation, even though the losers did not meet all requirements. Indeed, the controversy has helped spur investigations of government procurement practices by all branches of the government. Although the original IBM award still leaves observers perplexed, if only about the obviousness of the price difference, the Air Force evaluation group still stands as one of the most revered in the government.

Specifically, Honeywell argued that it had erred in its timing calculations, thinking its equipment operated under the 200-hour requirement, when in fact the benchmarks showed it didn't. The Air Force found that—based on additional hours needed for the 200 series to do functions required—the system cost was not significantly less than IBM's. Honeywell argued the AF should have figured on cost of additional equipment to meet requirements, which it said would only be $1.25 million. The AF also did not favor the 6-bit 200 series in an 8-bit environment, although Honeywell claimed the time lost in translation was not significant.

There was also some argument by vendors over the benchmarks, tests during which a malfunction can disqualify a bidder who has spent upwards of a million for his bid. The Air Force, however, with the blessing of such Congressional leaders as Jack Brooks, contends the benchmark is the best way available, but is making efforts to improve all procedures involved to reduce the cost of bidding. For example, it uses the COMET simulator to provide systems descriptions in condensed form and tries to provide programs in higher-level languages where possible to alleviate the programming costs for the benchmarks.

The AF made only one major change to the bidding procedures on the second go-round: providing the manufacturer with life cycle cost information so that he could estimate total cost, rather than equipment and maintenance alone. This included transportation, personnel, and utilities costs, which normally the AF would compute.

The award to Burroughs means new income to replace the loss of the B-263's now used in Phase I. The Air Force must decide whether to purchase or lease the B3500 systems, and determine the total number of installations, which can range from 100-160. Use of 160 systems will mean an additional $12-15 million in equipment to Burroughs; maintenance is estimated at $15-20 million, so the potential of the contract is nearly $100 million.

The AF and Burroughs have begun preparation for installation. Five will go in this year: two to AF Systems Design Center in Washington and the Military Personnel Center at Randolph AFB, Texas, in March; two to Sheppard Technical Training Center in April and May; and one for operational testing at Langley AFB, Virginia. No more will go in until the AF has evaluated the implementation status and the capability of the vendor to meet software commitments. By July, 1970, an undetermined number will be installed at AF commands around the world for accounting and finance, civil engineering, transportation, maintenance engineering, and military and civilian personnel.

Four sizes of installation will go in: A,B,C,D. Beginning with A as the smallest, the configurations will include: B3500's with 80K bytes (A and B), 100K, and 150K; 40,60,80, and 90 million bytes of random access storage; 3, 5, 9, and 10 Friden 7311 remote keyboard printers (called Burroughs 9350's); six tape drives, printers, card reader and card punch and remote card readers at each level.

L.A. SHERIFF MAY FINALLY GET SYSTEM—OR PART OF ONE

The Sheriff's Dept. of Los Angeles County, which had grandiose plans for a multi-megabuck on-line system of its own, will have to settle for only part of a $1-2 million system—at least for now. The county late last December went to IBM for its Courts and Law Enforcement computer system, a 256K 360/40 that will be used by the municipal and superior courts, the probation department, and the offices of the sheriff, marshall, county clerk, district attorney, and public defender.

This comes to quite a savings for the county, right? Wrong, says RCA, which lost out to IBM in the final runoff. By selecting Spectra 70 over System/360, said RCA, the county could have saved from $350K to $500K. Not so, said the county, which did admit to "an approximate $320K price advantage to RCA." But the price difference was reportedly outweighed by IBM's experience, its operating software, and a 360/40 in City Hall that could serve as backup for the county system.

RCA's insistence, however, forced a final decision on the top governmental body, the county's Board of Supervisors. This five-man group then paid the consulting firm of Ernst & Ernst $9K to evaluate "the soft goods and the hard goods and all of the stuff that we don't understand at all in the first place" and come up with a recommendation. E&E opted for IBM.

For both RCA and the sheriff's office, it was a good fight. From the start, the sheriff reportedly favored RCA. This dates back to 1961, when studies were begun for a real-time law enforcement system, and invitations went out for proposals (see Sept. '63, p. 19, and Nov. '63, pp. 13, 19). The bidders—IBM, ITT, and the consulting firm of Daniel, Mann, Johnson and Mendenhall—came in with systems that would have cost from $14-20 million over 10 years. But the county decided it wasn't economical to put such a system in.

According to Inspector Victor Riesau of the sheriff's office, all was not lost. Not only did this study effort spawn interest in such systems nationwide, but the office was determined to try again on a narrower approach. A $35K contract was awarded to DMJM to design a jail records-keeping system, which will be the first application they'll place on the 360. Following that will be a wants and warrants file, a record of all the warrants out in the county. Currently being placed on the city's computer by the L.A. Police Dept., this will be transferred to the county system, and its coverage broadened.

Studies for the county's integrated approach were undertaken a couple of years ago. Since the using departments work together and often have need for information from others' files (indeed, some files are duplicated within the county), a central system makes sense. But if everyone gets as many remote terminals as they say they need, there will be quite a load on the computer's I/O channels.

The sheriff, who handles an average jail population of 10,000, is proposing some 100 terminals, including more than 50 badge readers, 33 CRT/keyboard units, and Teletypes and printers. Everyday, 2,000 of the inmates must be scheduled for and moved to 200 courts in southern California. The courts, it seems, will need a dozen or more for a "traffic prior" system, which keeps track of previous traffic citations; repeat violators are then subject to a higher fine.

The $1.3-million computer system

was originally slated for an October '68 delivery date. This, no doubt, will be delayed; selection of the vendor was set back by six months because RCA hung in there. Yet to be decided is who will supply the communications gear and terminals.

Even more serious, no decision has been made as to who will run the new center. Odds favor the county administrative office, which at least would be a disinterested party. But none of the using agencies, much less the CAO, has even the nucleus of a staff.

Thus, any delivery of hardware before the end of the year would be a crime. —EKY

BRANDON, PANEL DISCUSS DP MANAGEMENT PROBLEMS

It becomes "our challenge to convert second generation managers with third generation equipment, first generation software, and prehistoric business practices into third generation managers." With this, Richard Brandon, president of Brandon Applied Systems, kicked off the firm's first conference on dp management problems, "Data Processing '68: A Useful Look Ahead," last month.

Speaking to an audience of 100 computer users, Brandon noted that most of the current crop of 25,000 dp managers are ex-tab shop heads and promoted programmers and analysts who have never been trained in applying complex management skills. And they are responsible for equipment, software, and personnel representing an annual expenditure of more than $16 billion.

Resource management, personnel, and communications are the most difficult problems facing this group, he said. Re personnel, the shortage of analysts, managers, and programmers may reach 250,000 within three years. Salaries have doubled in the past five years, and the turnover averages 30-40% in these prime categories.

The general public doesn't understand the role or import of computation and dp people have failed to communicate with top management completely; they talk about management information systems without understanding management processes.

Thinking wishfully, Brandon offered the ultimate solution: We should appoint a data processing czar with full power to (1) combine DPMA, ACM, and SPA; (2) tax each computer user $50 a year, and (3) tax each vendor .1% of equipment value. With the $20 million thus raised we could then develop, he said, a better system-oriented language, set up a universal standards manual, establish a resource management system, build executive training programs, educate the press and general public, develop a good systems analysis training course, set up better selection and performance standards for technical staff, and encourage more entrants in the field.

Last year did see the first full course in systems analysis offered—by IBM for $5800; third generation software began working; COBOL, remote testing, and AUTOFLOW were accepted as management tools; and leasing companies came into maturity. The few developments for management in 1968, he said, will probably be the acceptance *(and definition?)* of the difference between systems analysts and programmers, the first usable documentation standard to come out of USASI, a test for systems analysts, and some new "management crutches parading in the form of software."

The task of expounding further on economic, personnel, software, and hardware considerations for management fell to the panel of speakers: Dr. Morris Rubinoff, Pennsylvania Research Assoc.; John Postley, Informatics; Robert Reinstedt, The RAND Corp.; and Roland Eppley, Jr., Commercial Credit Computer Corp.

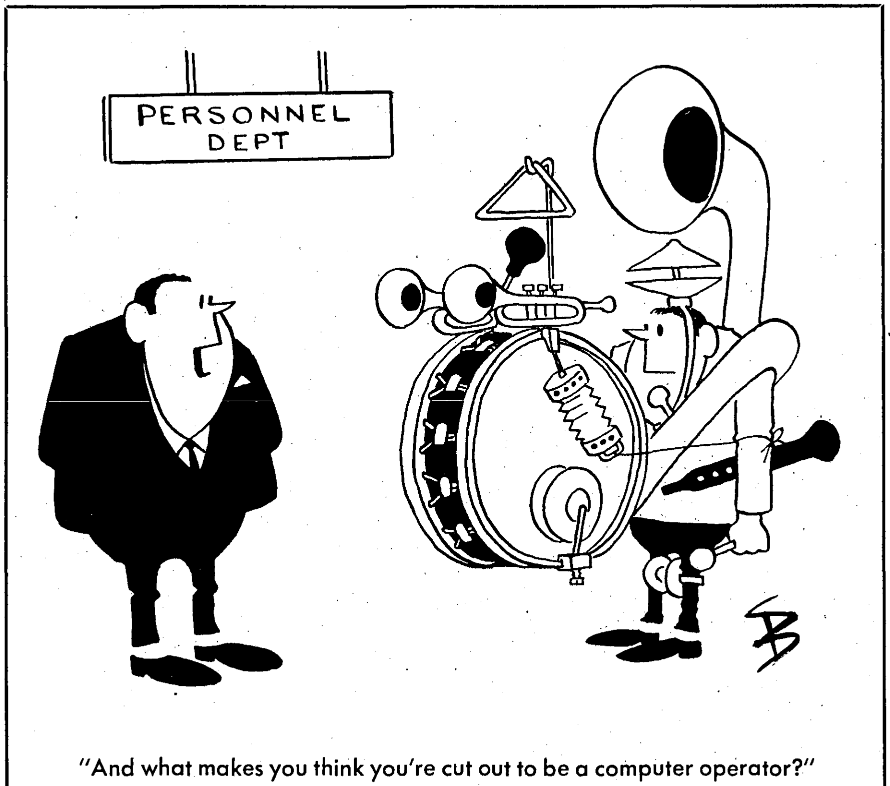
Roland Eppley detailed the reasons for the increasing complexity of equipment financing. Rental from the manufacturer used to be the most common method because the technology changed so fast and the user had little faith in the longevity of the equipment. But obsolescence of any kind in third generation systems will not be a significant factor for the next five to ten years, said Eppley, and the alternatives of purchase—or lease from a third party—are becoming attractive.

The manufacturers are not likely to come out with a fourth generation for some time because of the massive investment; IBM, alone, it is estimated, will invest a total $5 billion in System 360. And it will be another three to five years before even the most sophisticated users are fully exploiting system capability; about 80% of new-computer time today is used in emulating second generation programs.

What are the economics of purchase vs. lease vs. rental? Some general rules of thumb: a one-year lease can be obtained at about a 10% discount; a short-term (five-year) lease can be had for about 20% off manufacturer's rental; an eight-year lease can result in about a 40% reduction; and a purchase, depending on life expectancy and method of write-off, could result in more than a 50% reduction.

Another consideration is computer- or time-sharing. It is estimated, said Eppley, that by 1980 up to 50% of the dp activity will be in computer-sharing (including remote batch, t-s, and service bureau batch processing).

The man-machine interface was



"And what makes you think you're cut out to be a computer operator?"

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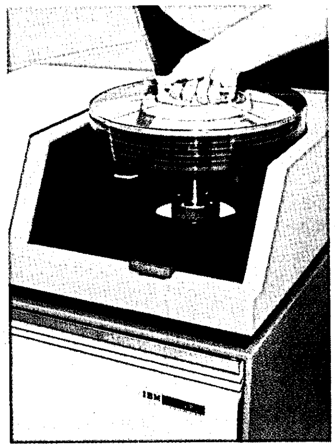

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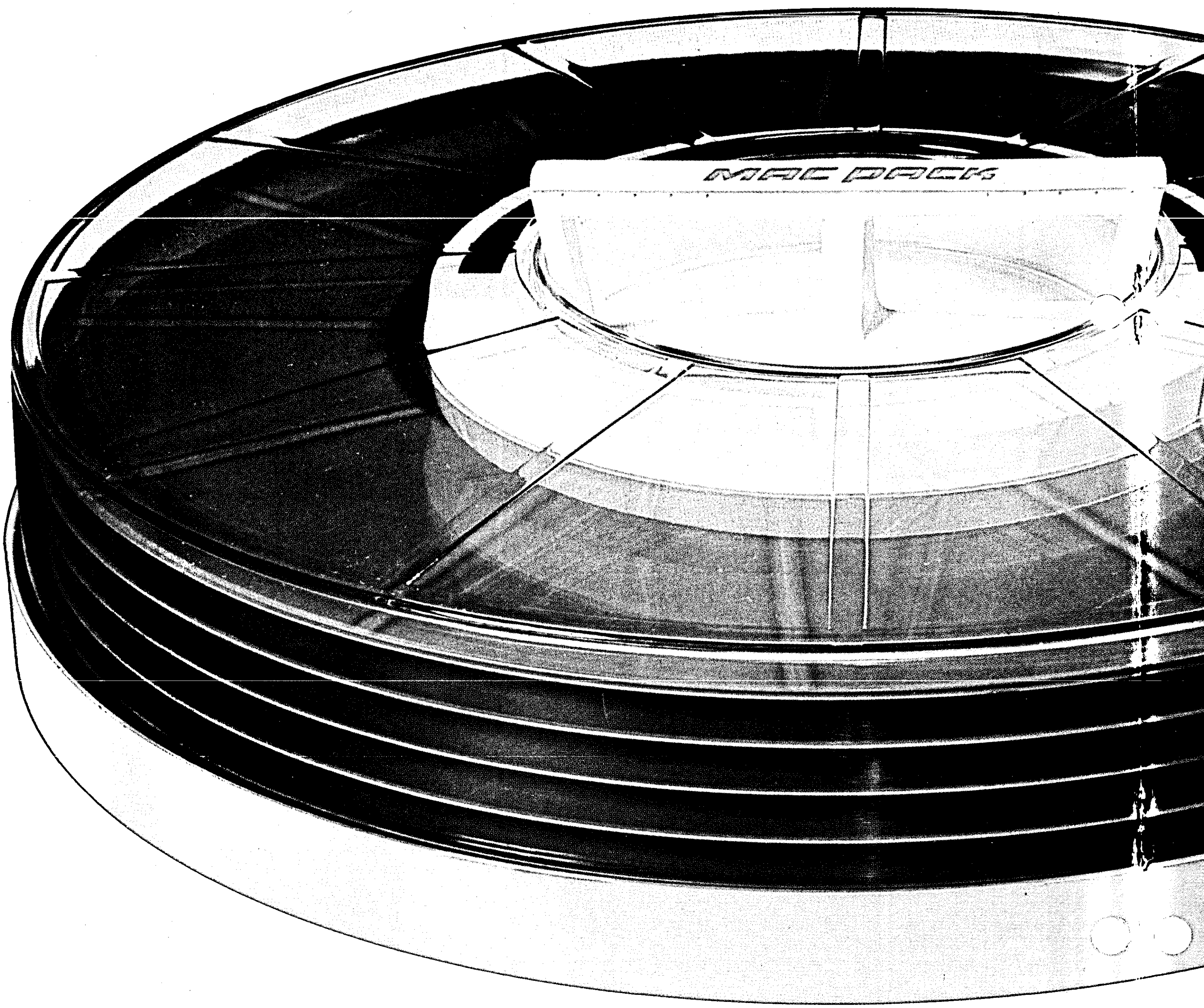

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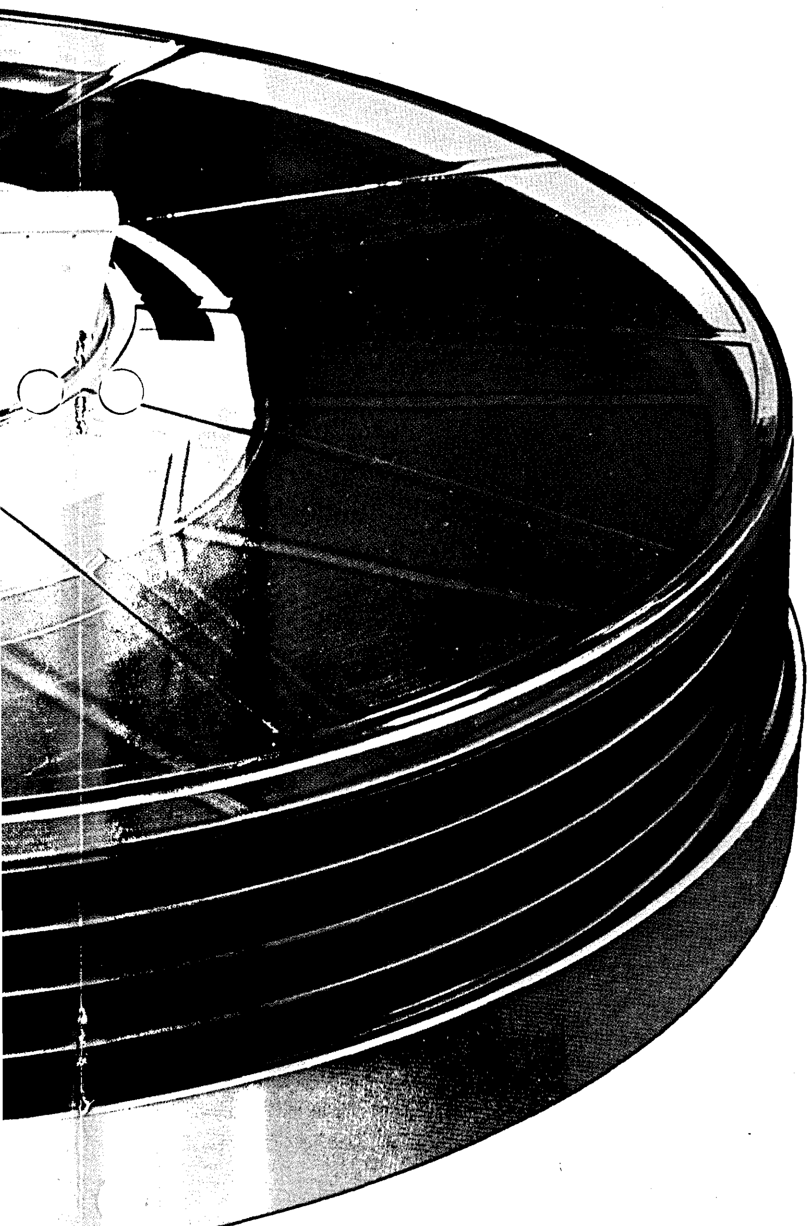

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System The kit contains a complete FORTRAN programming system consisting of a compiler, linking loader, object time package, function library and utility routines. All I/O interfaces are isolated and simple so that the system can operate either standalone or under an operating system.

The compiler accepts and interprets the entire IBM FORTRAN IV (G level) language. Compilation is single pass batch, producing locally optimized object code. The optional source listing contains complete diagnostics and the object program memory map. The entire compiler is core resident occupying between 3200 and 7000 words, depending primarily upon word size. For example, 3600 words are required in a 36 bit machine and 5500 in a 16 bit machine. About 1000 words additional are required for table space to give a capacity of 500 source cards. Capacity increases rapidly with table areas greater than 1000 words. No backup storage of any kind is required. Compile speed exceeds 1000 cards per minute on most computers.

The linking loader places object programs in core, performs data initialization, and loads and links required sub-programs from the system library. It is overlaid by the I/O editor prior to program execution.

The object time package contains the I/O editor and associated conversions, routines for double precision and complex arithmetic, and miscellaneous FORTRAN routines such as subprogram argument transfer.

The function library contains all of the internal and external functions recognized by FORTRAN.

Implementation Implementation of the compiler requires little knowledge of the compiling process. Most of the compiler (all the hard part) is already programmed in a special machine independent language (operator-operand) designed for this purpose. All that needs to be programmed is a simple old-fashioned interpreter of this language, consisting of 90 small routines totalling about 1500 lines of code. Detailed flowcharts, data layouts, and checked out coded examples are provided for each routine. Proven test cases are provided.

The linking loader and the object time package are produced from detailed flowcharts, data descriptions, and coded examples. The loader requires approximately 1800 instructions and the object time package, 3000.

The function library is supplied coded and checked out in FORTRAN IV.

In all cases, the programming required is easily segmented into tasks and is relatively unsophisticated, garden variety system work.

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singled out as the most important development in third-generation equipment and software by Dr. Rubinoff and John Postley. Terminal, user-oriented general-purpose languages, file maintenance and updating software systems, operating systems, multiprogramming, and other features are giving the user hands-on capability and changing the function and professional requirements of the programmer. Postley particularly noted that "no longer can we expect to draw programmers from less exacting disciplines and then find them operating as expert programmers within six months or a year."

Robert Reinstedt, however, in discussing personnel problems, felt that the industry is robbing itself of good apprentices by becoming "too selective." While higher levels of programming are developing, there is still opportunity for the high school and nonmath college graduate. "We should give more a chance to succeed," he argued. Reinstedt, who has developed a vocational interest profile at RAND, also argued against tests—certifications, personality, interest—as a selection tool.

During the luncheon, Cong. Cornelius Gallagher worked over the national data bank concept again. "I will recommend," he said, "in the upcoming session of the 90th Congress, the formation of a Citizen's Advisory Group made up of representatives of all the various fields of expertise to inform and advise the Congress . . ."

PERFORMANCE MONITOR DESCRIBED FOR L.A. ACM

A project that sounds like a big step forward in accurate measurement of computer system performance was described by Vinton Cerf of UCLA at the Los Angeles ACM chapter meeting.

The present methods of measurement—benchmark programs, functional simulation, on-line diagnostics—are generally considered rough approximations while Cerf's GASP (General Analysis of System Performance) is designed to "find out what's really going on in there." In addition, it's hoped that the finding out can be done with minimum delay and distortion, during the normal running of production programs. The work is part of Dr. G. Estrin's computer instrumentation project at UCLA's school of engineering (Oct. News Briefs, p. 112).

GASP will use special-purpose hardware, now being designed and built, hooked to a Sigma 7. It will be capable of recording, for example, how many times a program went through a particular branch. Sampling rates, with a maximum of 25 megabytes/second, can be adjusted to minimize program delay but accumulate data to build up a statistical picture of activity.

Cerf made a plea that all future computers include at least one instruction that can put out information diectly, showing that processing has reached a specific point. Such instructions are already included in the Sigma 7 and IBM 360 line.

The project group is now working on instrumenting a 7094. If the custom hardware works as well as they expect, they would like to make a mobile version that could be wheeled into an installation and produce output for use in analyzing a whole range of system performance—input/output channel activity and memory use as well as cpu performance.

A long-range goal of the project is to influence manufacturers in the design of future machines—a purpose that was greeted with some scepticism from the audience, with one listener pointing out that he had been telling IBM what was wrong with their equipment for years. In a spirited defense of his position, however, Cerf explained that there is a difference between giving a design group your opinion and showing them overwhelming evidence that certain changes will be beneficial in specific ways.

HONEYWELL HOPS ON THE DISC PACK BANDWAGON

A new plant in Newton, Mass., for the production of disc packs has been dedicated by Honeywell. Production has already begun and is scheduled to reach a rate of 1400 units a month by the middle of the summer.

The first unit introduced is the model M4005 and is said by the company to be "completely compatible with all drives currently marketed."

Although there are a few independents who have recently begun marketing disc packs, IBM has been the only computer maker supplying its own. Reasons for the growing activity are easy to see—considering that Honeywell estimates the 1967 market at $60-70 million and expects this to leap to $200 million a year by the end of 1969. They also think that the dollar volume of disc packs will exceed that of magnetic tape by about 1970.

Disc packs are the first "consumable" product to emerge from Honeywell's special products division, set up last May to turn out such supply items as mag tape, cards, and printer ribbons.

The Model M4005 pack, with six 14-inch-diameter discs, will sell for $490 or lease for $15/month. Current delivery schedule is 30 days.

NEW YORK POLICE TO CUT EMERGENCY RESPONSE TIME

The first moments of a fire, an accident, a robbery or other emergency situations are "life-death" critical and New York City is going to spend $4.7 million on a computer-based system (IBM) to trim the time it takes to dispatch police help from 100 seconds to 50. To be fully installed by 1970, the Special Police Radio Inquiry Network, SPRINT, will handle all emergency calls through a central police communications bureau, rather than through bureaus in each of the five boroughs under the present system.

When calls are received at the bureau, officers manning 36 keyboard displays (IBM 2915's) will key in the borough, location, and type of incident. A 360/40, containing 300,000 locations and data on the city's 1400 patrol cars, will search the file and transmit block number, precinct, nearest intersection, nearest hospital, and the numbers of three available patrol cars to the appropriate radio dispatcher. (There will be 18 keyboard display terminals for the dispatchers, each of whom covers a specific area of the city.) The dispatcher then will order a car to the scene and tell the computer of his action.

SPRINT will also notify bureau personnel via the CRT when the number of available cars falls below a certain point. The system will also contain a file of stolen vehicles so that officers throughout the city will be able to radio in license numbers for checking. The 360/40 used will be a 256K-byte system with a 2314 disc drive (9 disc packs).

RCA PHOTOTYPESETTER COMES WEST

The first installation west of the Mississippi of an RCA Videocomp phototypesetter is at Auto-Graphics Inc., Monterey Park, Calif. It is the seventh Videocomp installation. According to Auto-Graphic's Robert S. Cope, it makes possible the (printing) production of a book in six weeks that would require four months using hot metal typesetting. And instead of taking 60 hours on a Photon 713, the book would be set in only four hours on the Videocomp.

One of the leaders in the use of

computers among typesetting houses, A-G already has two Photon 713's and a B-R 230-B computer. Among the jobs being run on the latter configuration is computerized drafting—electronic schematics, block diagrams, etc. (see June '67, p. 19).

A Sigma 2 mentioned as a possible acquisition in the earlier story on A-G never materialized; instead, they got a 64K Spectra 70/35 with six tapes, disc pack, and a 1200-lpm printer. Unlike the recently-announced IBM 2680 phototypesetter, of course, the Videocomp operates off-line. Thus, two of the tape drives are connected to the typesetter, four to the mainframe. Underway is an attempt to get the two banks of drives to talk to each other.

One of the jobs being typeset is the catalog for a local college. The school inputs its catalog data (course name, credits given, prerequisites, etc.) and schedule data (course number, room number, prof's name) into the IBM Datatext system. When completed, both files are delivered to Auto-Graphics for merging and formatting prior to photocomposition. Software for editing, conversion, pagination and formatting are part of A-G's services.

Does the speed of the Videocomp mean lower typesetting costs? In time, says Cope, prices may be reduced by from 25-50%. The new equipment, however, increases A-G's capability to cover four major needs—that of the book production industry, the directory and list industry, and engineering and educational documents.

CDC, PRC EXECUTIVES QUIT TO SET UP TRAINING FIRM

Another company proposing to do its bit to overcome the programmer shortage has been organized, headed by three ex-executives from Control Data Corp. and one from Planning Research Corp.

Computer Learning Corp. will have former CDC vp Thomas E. Stone as president. Swen A. Larsen, who established and was president of Control Data Institutes and also headed Automation Institutes of America, will be vice president of Computer Learning education centers. Robert F. McIntosh, from Planning Research, will be vp for education development and consulting services. William C. Thompson, another CDC alumnus, will be vp for management education and special services.

The Falls Church, Va., organization plans to open 12 education centers in metropolitan areas during the next three years. They will be going after three levels of prospects: new students, computer people wanting advanced instruction, and management interested in practical applications. Courses will be offered for programmers, operators, and technicians—as well as advanced work in such subjects as time-sharing, communications, and graphic applications.

DECADE COMPUTER CORP. ENTERS MAINFRAME FIELD

From the start of the computer industry, profit-seeking firms have come and gone. An early period that saw the entrance of several firms was followed by one that resulted in their merger or dropout. Even today, rumors persist that one or more of the survivors in the industry is trying to buy out another.

In the midst of this consolidation period, which may never end, we are seeing the entrance of new firms again, this time on a smaller scale. Among these are Business Information Technology of Natick, Mass., makers of the BIT 480, and Interdata, the 1½-year-old Eatontown, N.J., firm with its Interdata 3 computers.

Joining this latter group is another new firm, Decade Computer Corp., Huntington Beach, Calif., formation of which was announced late last year. They will "manufacture and market a line of small computers" whose use would require a minimum of programming effort. Currently in the midst of their product development program, they reportedly will begin marketing in the spring or summer of this year. By that time, they plan to have about 75 people, up from 20 at year end.

Three of the officers were formerly with Pacific Data Systems, a subsidiary of Electronic Associates Inc. They are president Paul J. Linebarger, ex-vp and general manager at PDS, Jon L. Nickerson, new vp and director of marketing, and Dale H. Swett, vp-treasurer at Decade. The vp and director of engineering is Walter G. Edwards, formerly with the Nortronics division of Northrop Corp.

McDONNELL AUTOMATION GOES INTO TIME-SHARING BUSINESS

McDonnell Automation Co. is joining the commercial time-sharers, offering a service they call Direct Access Computing. The big service bureau firm has been selling remote access batch processing for some time.

McDonnell will use a GE 420, based on the 415 and a Datanet-30, with access by dial lines from Teletype ASR 33 or 35 terminals on the subscribers' premises.

The company now has computing facilities worth about $43 million, employs 1400, and has offices in five cities besides the St. Louis headquarters.

OHIO HIGHWAY PATROL STARTS COMPUTER NETWORK

A system appropriately called LEADS (Law Enforcement Automated Data System) is now in operation by the Ohio State Highway Patrol. Some 155 IBM 1050 terminals (with the possibility of later changing to ASR mod 33 and 35) in communication centers throughout the state will be tied into the three-computer center at the State Dept. of Finance in Columbus. Already installed are an IBM 360/30 and 40; a second mod 40 is due early this year.

Three separate files of information will be included in the system: registration numbers on over five million vehicles; operator's license information on more than six million drivers, including current records of arrests, convictions or traffic violation points compiled; and a file of information on stolen vehicles and parts, missing license plates, and vehicles driven by persons with suspended or revoked operator's licenses.

The files are contained on four IBM 2321 data cells, each with a capacity of 400 million characters, and two IBM 2311 disc drives.

Through LEADS, Ohio is able to tie in with the FBI's National Crime Information Center in Washington, D.C., and with the Law Enforcement Telecommunications System, a cooperative information exchange between police units in the continental states.

Via a switching system, the terminals also provide intra-state police communications.

EXPERIMENTAL TOUCH-TONE CAN GENERATE CHARACTERS

Among the host of Touch-Tone applications now being considered is an experimental program at Bell Labs grafting a small display screen onto the pushbutton unit. The device would be useful for telephone communication between deaf people.

The buttons generate a sequence of letters, digits, end-of-word, and end-of-sentence signals. The 2 button, for example, is used to produce A, B, or C—depending on whether it is depressed one, two, or three times. The signals are stored until a character is fully coded, then released by pressing the zero. Practical limits of output are 8 to 16 words per minute. Further experimentation, including the use of simple printing attachments, is under way.

FARRINGTON WILL MARKET NEW CREDIT CARD SYSTEM

Farrington Manufacturing Company plans to market a new credit card reader-imprinter before next summer which will report the card holder's credit status. Reportedly, the device will also use a new technique to verify the cardholder's identity, one that "is simpler and more foolproof than a personal code number," says a Farrington spokesman.

Retail stores are expected to be among the major users. Now, many of them access a credit file whenever a card holder wishes to buy more than a certain amount. The Farrington system, says the company, will reduce such queries substantially.

The new credit card equipment is described as an "off-line, solid state countertop unit which can be used at any bank, store, gas station, or other consumer outlet." It was developed by Telecredit, Inc., Los Angeles, but Farrington has acquired all rights to the device. Norville E. White, Farrington's president and chairman, said Telecredit has been developing the device for two years.

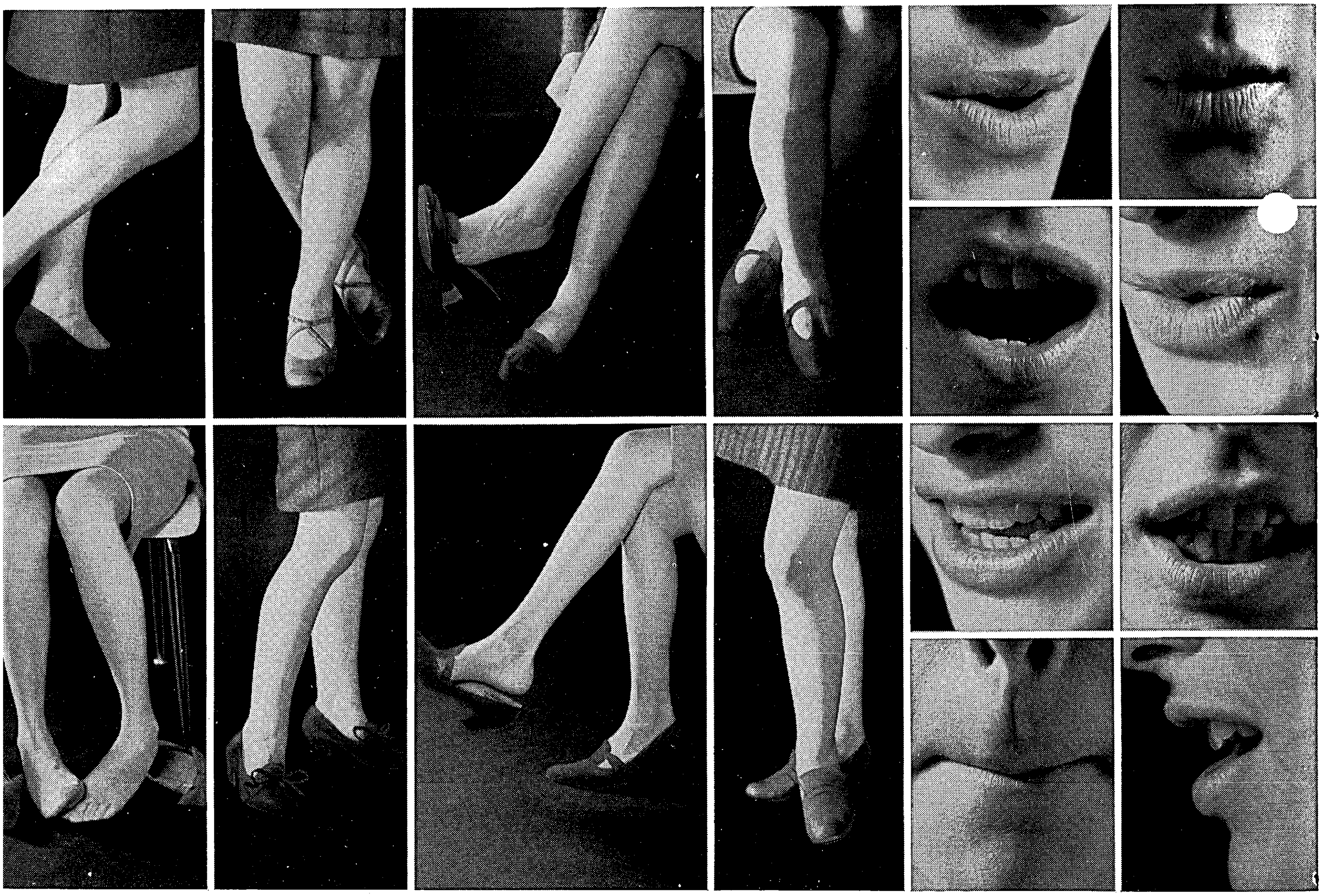
REDSTONE CENTER SHOWS ON-LINE LIBRARY SUBSYSTEMS

From December, 1966, to October, 1967, the Redstone Scientific Information Center in Alabama (RSIC) installed and demonstrated on-line patron registration and book circulation subsystems as forerunners to the overall ALPHA-2 System (Automated Literature Processing, Handling and Analysis). The center is an element of the Research and Development Directorate, U.S. Army Missile Command, and is jointly financed by the command and the Marshall Space Flight Center, NASA. Director of the center is Fred E. Croxton.

The demonstration was conducted using one, and later two, IBM-1050 remote terminals (typewriter, card reader, and punch) which communicated with an IBM-7740 switching computer and an IBM-7010 as the central processing unit (CPU). The library-related data files attached to the CPU were on a dedicated 2301 disc unit; a 1311 disc pack unit attached to the 7740 contained the programs and message cues. Computers and files were about half a mile from the terminals.

The computer system was in constant teleprocessing use by others during this period and also handled background batch work.

The patron registration module contained registration data for about 7,000 patrons; the records for each contained 27 separate data elements. The programs provided for the addition or deletion of patrons, modification of any data elements, and look-up



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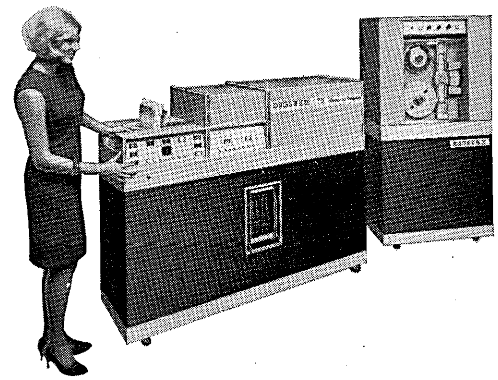

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CIRCLE 47 ON READER CARD

with controlled output either by name or by social security number, the element used by RSIC as a registration number. The book circulation module contained circulation, overdue and recall data on about 33,000 books. Only call number, short title, and certain house-keeping data about the books were on the file. (Full bibliographic data will be included in ALPHA-2.) The functions which could be performed were loan, return, recall, reserve, list, and locate. Only entry by call number and borrower were provided in the demonstration.

The demonstration modules were designed to determine what difficulties in systems design, programming, and use would be likely to be encountered in operating on-line in a library environment and to show if full-scale implementation of ALPHA-2 as an on-line library system would be feasible.

The demonstration showed that there was every reason to believe that a full-scale on-line library system such as ALPHA-2 could be designed, programmed and operated successfully provided multiprocessing hardware was used. It also showed that the use of sequential processing of inquiries without priority interrupts and without very short time limits would not be satisfactory.

A number of problem areas were uncovered and will get attention in the full-scale ALPHA-2 design. Examples are work sequence, display, delay, and function. Some of the more significant of these are mentioned below.

Delay in response was a major problem. When first operated, there was no limit on the CPU time which could be used for a transaction; in some cases, inquiries waited 20 minutes in the transaction cue because of the processing of other actions. Later a one-minute time limit was used which greatly improved this situation. It was noted that the patron gets impatient in a very few seconds unless activity is apparent. Apparently, 6 to 10 seconds is the maximum allowable turnaround time for a transaction for a waiting patron.

Exact matching of file (or index) entries was entirely successful; however, the technique of "near match" on names using the selection of a name from a list derived from short truncations showed that more sophistication in "near match" is required. It also led to the same conclusion reported by Dr. Rubinoff's group at the University of Pennsylvania: There must be a way to stop a long printout and to restate the problem.

The format of the output produced by the IBM-1050 remote typewriter is almost as important for rapid use of this device as is its length.

Storage costs for the files are more important than computing costs.

Keying is to be avoided in as many transactions as possible if a patron is waiting. It was concluded that the use of function keys and badge or card readers would be preferable to keying wherever possible, although this was not tested directly by equipment comparisons.

When the second remote terminal was added to the system, certain transactions in the registration module were enabled on the second terminal and prohibited on the first; similarly, certain transactions in the circulation module were enabled on the first terminal and prohibited on the second. Numerous transactions were possible on both. This technique, which was coupled with an "override code" known only to the analyst, was wholly successful as a file security method to limit what each terminal could do to a data file and what each terminal could receive from the file.

The follow-on effort, design and programming on the first phase of ALPHA-2, is under the design leadership of L. J. Cooney, RSIC systems analyst, and is now approximately 80% and 50% complete, respectively. Phase 1 of the ALPHA-2 effort covers a full-scale book control system consisting of ordering, receiving, cataloging, circulation and subject heading control subsystems as well as patron registration. Phase 2, which is in the early design stage, covers the serials subsystems. Phases 3 and 4 cover subsystems for documents and for current and retrospective retrieval. This ALPHA-2 system will operate on the Univac 1108 now being installed for the Marshall Space Flight Center (MSFC), NASA. Programming is in COBOL.

The programming and computer assistance required for this work was furnished by the Computation Laboratory of MSFC with most of the work being performed by personnel employed by its contractor, Computer Sciences Corp. (CSC). R. Clayton McGee (MSFC) was responsible for managing this support and W. G. Aldrich (later D. L. Power) (CSC) led the programming team under the design guidance of Mr. Cooney and Mr. Croxton.

PITTSBURGH GETS FIRST TIME-SHARING SERVICE

On-Line Systems, Inc., a new t-s service bureau, recently opened in Pittsburgh. The company is headed by John Godfrey, former manager of t-s development at GE/Phoenix. Senior vp is Raff Ellis, another GE alumnus.

On-Line is the first and only supplier of t-s dp service in the Pittsburgh area, says the company. Its hardware consists of a GE 255 with 15K main frame and 18 million char. disc file. Programs and written in BASIC, FORTRAN and ALGOL. Customers include R&D, educational, and industrial organizations in the greater Pittsburgh area. On-Line's 255 system can handle 40 customers simultaneously, and up to 60 concurrently. Each pays $15 per on-line hour.

A PDP 10/50, which On-Line hopes to have operational by mid-'68, will treble the company's dp capacity, reports Ellis. The company is planning to open two more dp centers—one in the Eastern U.S., the other out West—within the next two years.

Among the company's present customers is the North Allegheny School District, in north suburban Pittsburgh. The district is now using the 255 for analysis and computation of student test scores, using programs developed by On-Line. Next fall, Allegheny district officials plan to integrate On-Line's system into a new data processing course for senior high school students.

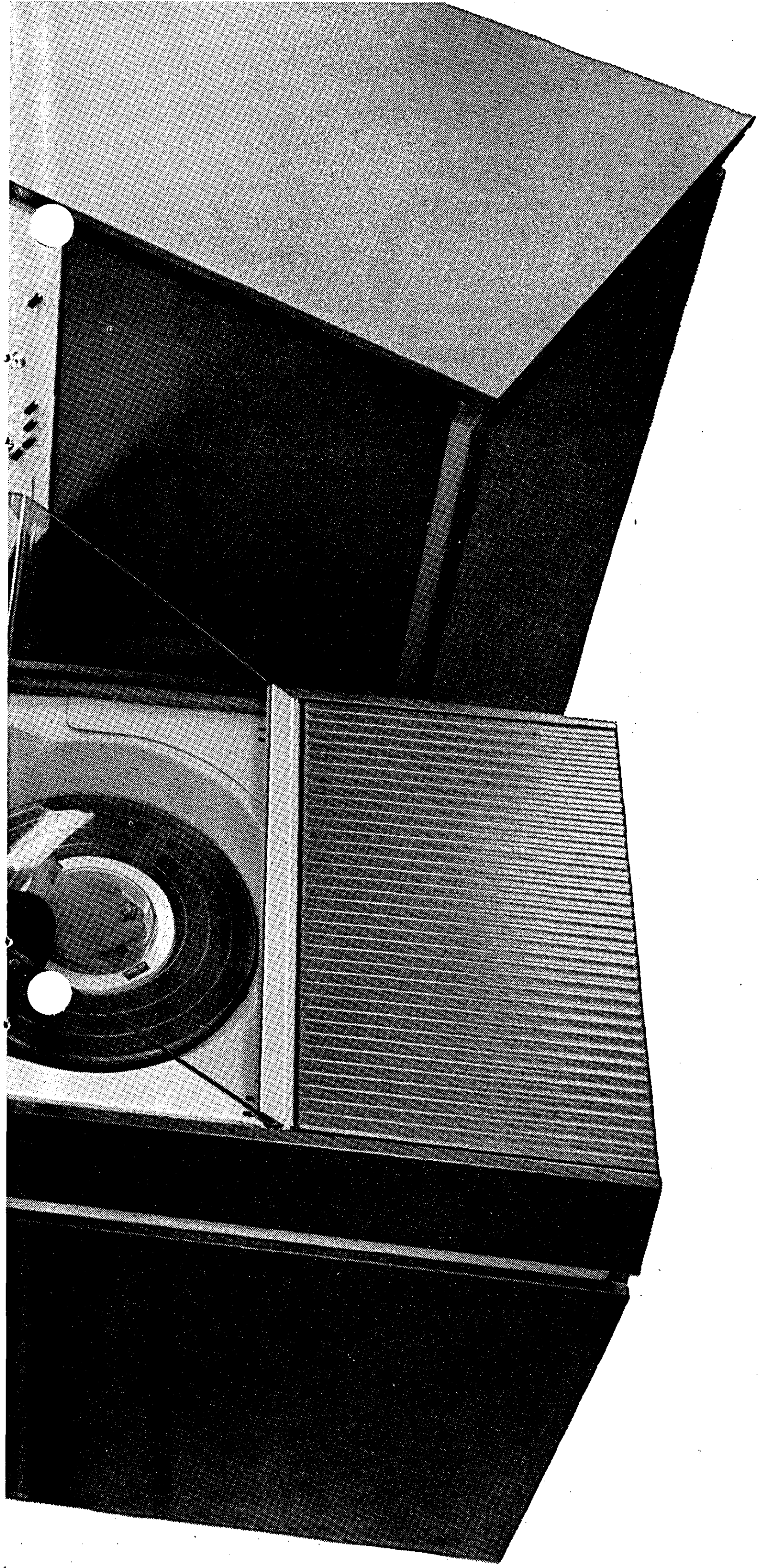
FUND AMERICAN INVADES COMPUTER LEASING FIELD

Third-party leasing of computers, until recently the province of new and bold entrepreneurs, is now attracting the big-money boys.

Latest entry is Fund American, a holding company based in San Francisco and formed in January, 1966, to take over the reorganized Fireman's Fund Insurance Co. It then acquired North American Securities Co., operating four mutual funds. Now it's starting a new subsidiary for computer leasing, to be called SSI Computer Corp.

Fund American is putting up $10 million and other financing will bring initial capital to $80 million. They plan to spend that amount on System/360's during the next 18 months, which will put them among the biggest companies in the business.

SSI president is Peter S. Redfield and executive vice president is Gary B. Friedman. Redfield was director of administrative services at Transamerica Corp., which recently decided not to go through with the proposed acquisition of pioneer leasing company MAI. Friedman is a veteran IBM marketing man, most recently branch manager of the San Francisco metro-



First: 45 day delivery.

Now: 10 to 20% price reductions.

SEL 810A 4K—$18,000
SEL 840A 8K—$60,000

When we put over 100 of these computers in the field last year, we learned two things: What excellent machines they are. How to produce them more efficiently.

So we doubled our production capability. Result: in August we were able to announce 45-day delivery. Now we can announce across-the-board price reductions of 10-20% on typical computer and peripheral configurations.

Same great features. Nothing changed.

For example, the 16-bit SEL 810A has all integrated circuits. Three priority interrupt levels. 4K memory. Input/output typewriter. High-speed multiply and divide. Real time I/O structure.

The 24-bit SEL 840A features include: all integrated circuits. 8K memory. Three hardware index registers. Hardware multiply and divide. Power fail safe. Input/output typewriter. Multi-level indirect addressing. Real time I/O structure. And a real time monitor.

Call, don't write, Joe Popolo in our Marketing Department. Give him your specs. He'll give you a quote. Probably within two hours. The number: Area Code 305/587-2900.

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politan office.

In addition to insurance companies and mutual funds, Fund American owns a real estate and office equipment leasing organization—for a grand total of $1.3 billion in net assets.

JOINT MEDICAL GROUP STARTS PILOT STUDY

In the biomedical field, there appears to be a frantic effort to get more patients on-line to a computer, especially for the diagnosis and treatment of cardiovascular diseases.

At the Latter-Day Saints Hospital in Salt Lake City, Utah, there's a pilot study underway to study the feasibility of using a central computer to process a variety of physiological signals from patients in remote hospital locations. Also involved are the National Institutes of Health and the Univ. of Utah.

They're using a CDC 3300 which joins a 3200 that has been installed at the hospital for several years. On-line terminals, including the CRT variety, are to be used. They'll be performing the on-line classification of EKG patterns, computation of pulmonary physiological parameters, processing of on-line data from patients in intensive care wards, and the analysis of on-line pressure and oxygen saturation data during heart catheterization.

OREGON ADVISED TO FORM COLLEGE COMPUTER NETWORK

All of Oregon's colleges and universities will be linked by a computer network if the Oregon State System of Higher Education follows recommendations of the Interinstitutional Committee on Computer Activities (ICCA).

Recommendations from a two-year study by ICCA are to set up an experimental system linking the institutions to existing computer centers at the Univ. of Oregon (Eugene) and Oregon State Univ. (Corvallis). UO has an IBM 360/50, PDP-7, IBM 1620 and 1410; OSU operates a CDC 3300 and an IBM 1620.

The other schools, many of which already have smaller computers under research grants, should have a satellite for most on-campus uses with access via one console per 500 students to the larger machines for backup, overflow, research, CAI, and administrative reporting. Such a statewide system would give even small institutions access to large computers without duplication of equipment. Among other possible benefits, ICCA notes those of better programs for institutional management, CAI curricular development, improved college library operation, and standardization of administrative reports.

SURPLUS SAGE CRT'S FOR BIOMEDICAL STUDY

A biomedical computing complex with an octopus-like array of processors built around the EMR 6130 computer is under development at Loma Linda Univ., San Bernardino, Calif. They have the first 6130 to be delivered, an 8K system, plus a dozen surplus SAGE display CRT's. The latter were acquired gratis when the SAGE system was dismantled at nearby Norton AFB.

Under Dr. Ivan R. Neilsen, Loma Linda has developed a math model of a heart, which enables them to simulate heart problems and display the results on a scope. Driving the display till now has been the UCLA 360/75.

MICHIGAN BLUE SHIELD REPORTS ON DATA-RECORDERS

Michigan Blue Shield, Detroit, increased input data conversion in the first 11 months of 1967 from 31,860 to 120,000 items per day, and saved 34% of cost, by going from key punches to Data-Recorders (86 Mohawk 1101s, 10 NCR 735s).

Data conversion takes 142 people (of 232 at the facility) in three groups: Medicare, Medicaid, and regular subscriber accounts. Working from 102 forms, each claim is broken down into single services (Medicare claims average five services, Medicaid two, regular subscribers 1.4) keyed onto 200 bpi D. R. mag tapes, verified, and later converted into 800 bpi computer tapes.

At the advent of Medicare, MBS set up a dp center for handling its Part B program using one Honeywell 200 and keypunching data conversions. In the past 1½ years an H2200 and another H200 were added.

Input data is checked for possible duplication, regular subscribers through BS-Blue Cross Unifile at Blue Cross. Medicare tapes go daily to the Social Security Administration in Baltimore for verification of deductible payments and there is a daily flow of verified tapes back to MBS. Medicaid eligibility is furnished on monthly tapes by the state of Michigan. Checks are written weekly for the two government programs.

The utilization file, a six-million-case history, is undergoing long term review by MBS to determine what and how services are used. The case history, when properly authorized for use, could also furnish emergency information on ailments, medication, and doctor should a client be hospitalized in a coma.

By 1975 MBS will need the ability to handle 383,000 inputs a day including prescription drugs and dental services which are seen as inevitable additions to present services. Thus MBS is casting about for ways to capture data at its source.

NEW FIRM WILL SPECIALIZE IN LSI/MOS TECHNIQUES

A company called Electronic Arrays has been formed in Mountain View, Calif., to produce microelectronics, concentrating on large scale integration using MOS techniques.

The company's president is Dr. James J. McMullen and he, as well as the other founders, was with General Micro-electronics—leaving when the company was bought out by Philco-Ford. In the meantime the group has been in business as McMullen Associates.

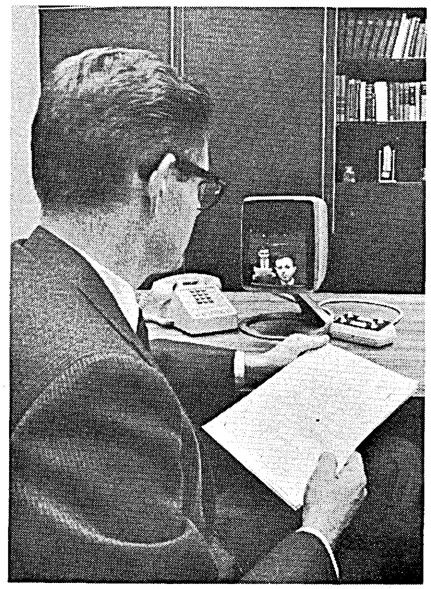
Besides McMullen, who was director of the semiconductor division at GMe, the principals are Earl Gregory, who was director of marketing; Dave Stiefbold, formerly manager of technology development; and Gene Stephenson, who was manager of commercial equipment development and responsible for design of the first commercially available MOS integrated circuit, a 20-bit serial shift register.

The first microelectronic array products are expected to be announced this fall.

NEW MODEL OF PICTUREPHONE WILL GO TO WESTINGHOUSE

AT&T has developed a Picturephone Model II at Bell Labs for possible introduction in the early 1970's and Westinghouse will give 40 sets a trial starting this September.

The earlier model had several such



tests, including use at the 1964 New York World's Fair. The Model II has a new camera tube that can handle a wider range of lighting conditions and allows either close-up or wide-angle viewing. A two-mil-thick silicon wafer is used in the tube, containing over a half-million silicon photodiodes and produced with the same techniques as those used for integrated circuits.

● A Council on Computer Centers and Computer Science Education and Research has been established by the Southern Regional Education Board (SREB) under a grant from the Esso Education Foundation and IBM Corp. The purpose of the council is to promote better use of computer facilities at colleges and universities in the South. Of 640 institutions of higher education in the South, about 200 have computers; only a few now offer, or are preparing to offer, degree programs in computer sciences. The new council will initially consist of four ten-member committees for computer centers, computer science degree programs, administrative information systems and CAI.

● An annual forecast by the Columbus Laboratories of Battelle Memorial Institute predict total 1968 R&D expenditures to reach $26.5 billion, an increase of $700 million (3.3%) over estimated 1967 spending. For the first time since reliable figures became available, it is expected that the increase in federal spending on research in the social sciences will exceed the increase in physical sciences.

● Responding to a $450K contract, Systems Engineering Labs will deliver a dual computer multi-experiment data acquisition system for use in nuclear research to the Oak Ridge National Laboratory (Tenn.) operated by Union Carbide for the AEC. The system will incorporate two SEL 810B 16-bit computers.

● Modesto Junior College (Calif.), with a student body of over 4,200, is testing a computer registration system during the spring semester on a recently purchased 1401. Students will write on special worksheets the classes, instructors, alternate choices, and hours available for class time. These worksheets will be fed to the computer, and the number of students wishing to enroll in each course will be tallied. This tally will be used to determine if enough course sections are offered. Program sheets will then be input to the system to obtain class schedules for each student. The school is using a program written by De Anza College of Cupertino, Calif. In addition to De Anza, similar programs are in effect at Bakersfield (Calif.) College and Washington State University.

● Grumman Aircraft has accepted the first of a series of microelectronic digital computers developed by Control Data for use in the Mohawk OV-1 aircraft. Designed to MIL-E-5400 specs, the computer measures 4½" x 6¾" x 8½" and weighs under 13 pounds. With a 4 usec cycle time, the computer's memory has a capacity of 1,280 12-bit NDRO words, expandable to 7,680 words; and a scratchpad memory of 128 24-bit NDRO words, expandable to 256 words. The entire

Been searching for the low-cost computer? Honeywell to the rescue.

Introducing the Model 110 computer. Honeywell's newest and smallest yet. The computer that opens the door to electronic data processing for literally thousands of organizations.

"What's so special about the new 110?"

The 110 is a well-balanced third-generation Series 200 system of hardware and software. It works equally well with magnetic tapes or disks. It comes with a complete range of support features, including a nationwide chain of Customer Support Centers, a COBOL programming system, and a big selection of pre-coded application systems.

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That's our idea of a rescue.

The Other Computer Company: Honeywell

news briefs

system-CPU, memory, I/O unit, display, keyboard and power supply—fits as a complete package into the aircraft's avionics system.

● By order of the FCC, ITT World Communications, Inc., has filed a tariff allowing users of overseas voice-grade communications channels to subdivide them to produce additional circuits of not more than 22 telegraph circuits on a cable channel or 24 telegraph circuits on a satellite channel. Service will be offered to any point to which the charges for an individual full-speed telegraph circuit do not exceed 40% of those for an individual voice-grade quality channel.

● Inflation in France has forced Bull-GE to raise the sales price, though not the monthly rental, of the Gamma-55 computer. No information was available on the amount of the increase because of the configuration variations, except that the price will correspond to 48 months' rental. A typical configuration of the 55 will sell for approximately $50,000, but there was no information available on what a typical configuration is and its previous price. The increased price also reflects the increased performance and capacity added to the 55 since its mid-1966 introduction.

● EG&G, Inc., Bedford, Mass., an electronics and engineering corporation, has announced plans to acquire Wolf Research and Development Corp., a 350-man consulting firm with current annual sales of over $5 million. The acquisition will involve an undisclosed amount of EG&G common stock in exchange for all the outstanding stock of Wolf, which will be operated as a wholly owned subsidiary.

● The ACM has chartered a new Special Interest Committee on Digital Simulation (SICSIM) under the chairmanship of David Brandin of IIT Research Institute. The committee will attempt to provide distinctions between techniques useful in simulation of continuous and discrete models, guidelines for development of simulation languages, dissemination of programming techniques, related computational mathematics, information on new applications, and other topics in digital simulation. Membership requests and suggestions for activities should be sent to Mr. Brandin, IITRI, 10 W. 35th St., Chicago 60616.

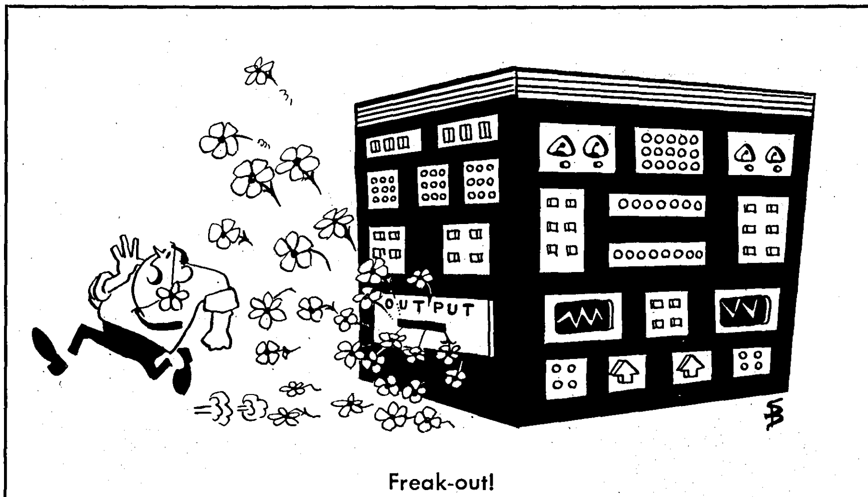
● The 1968 IEEE Microelectronics Symposium scheduled for June 17-19 in St. Louis, Mo., is soliciting papers on the theme "Microelectronics and Electronic Systems." Requested topics include developmental and experimental approaches in design, materials, processing, packaging, applications and production in microelectronics. Prospective authors need not be members of IEEE. Three copies of 350-word summaries should be submitted before March 15 to Dr. Remo Pellin (Program Chairman), Director, Semiconductor Materials Dept., Monsanto Co., 800 N. Lindbergh, St. Louis, Mo.

● A call for sessions has been issued by the technical program committee for the 1968 Western Electronic Show and Convention (WESCON) to be held in Los Angeles, August 20-23. A deadline of March 15 has been given for submission of letters of intent—outlines describing a proposed session topic and listing individual participants (authors or panelists) and their subjects. Letters of intent should be sent to Dr. Robert M. Ashby, WESCON Technical Program Committee, 3600 Wilshire Blvd., Los Angeles, Calif. 90005.

● A new peripheral manufacturer—Paragon Systems, Inc.—has been formed in Houston under the presidency of William W. Witt. Mr. Witt, former vice president and general manager of Geo Space Computer Div.'s Computer Products Dept., is assisted by chief engineer Robert E. Williams, former manager of analog engineering at Geo Space's Instrument Div. Paragon has already been contracted to supply peripheral I/O equipment to Digital Seismic Corp. for the PASS/1 geophysical dp system.

● Stockholm County, Sweden, plans to build an advanced medical dp system around a Univac 494 (with two Fastrand II mass memory drums, an FH-880 high-speed drum, three Uniservo 8-c mag tape units, a 1004 and eight Uniscope 300 visual display terminals). A pilot system is slated for Danderyd Hospital (1500 beds) early this year. When finished, the system will cover all medical management, control, treatment, operations of the pharmacy, clinical labs and inventory control. Later the system will be extended to all 15 hospitals (13,000 beds) in the county, including their two million outpatients annually.

● IIT Research Institute, Chicago, and electronic firm sponsors are concluding the first year of CADEP (Computer-Aided Design of Electronic Products) with a program developed for analog circuit design. The second-year project expansion will seek a program as a design aid for digital or logic circuits. Data communications between IITRI Computational Services Center and participating plants allow fast turnaround of data analysis of circuit specs. ECAP (Electronic Circuit Analysis Program), used primarily for DC and small signal AC analysis, will be modified to produce automatic plots by Teletype printer. SCEPTRE (System for Circuit Evaluation and Prediction of Transient Radiation Effects) provides transient analysis and can handle non-linear devices. IITRI has a measuring lab to gather



Freak-out!

news briefs

transistor performance data and is assembling a library of electronic device models for design use.

● The Univ. of Southern California's demonstration project on the drinking driver and traffic safety is a three-year study under contract with California's Transportation Agency. This unique program will attempt to ferret out the repeat offender so that rehabilitation may be undertaken before driving licenses are issued or renewed. A profile is being prepared, with data collection techniques and computer use, to discover what characteristics are peculiar to repeat offender drunken drivers. A probability model will be developed to judge an individual's chances of becoming such an offender. Where a person is identified as a probable future re-offender, the project hopes to be able to influence such a person toward rehabilitation. The project is an interdisciplinary effort adding to the staff of the Youth Studies Center a psychologist, computer programmer and field research assistants, plus a number of consultants from various disciplines.

● The proposed COBOL standard is expected to be approved by X.3 after the second letter ballot is completed Feb. 22. Last month, the first ballot netted yeses primarily on the condition that the random processing module be removed and revised. Once this and other minor changes are done, another revised COBOL standard will go out for approval.

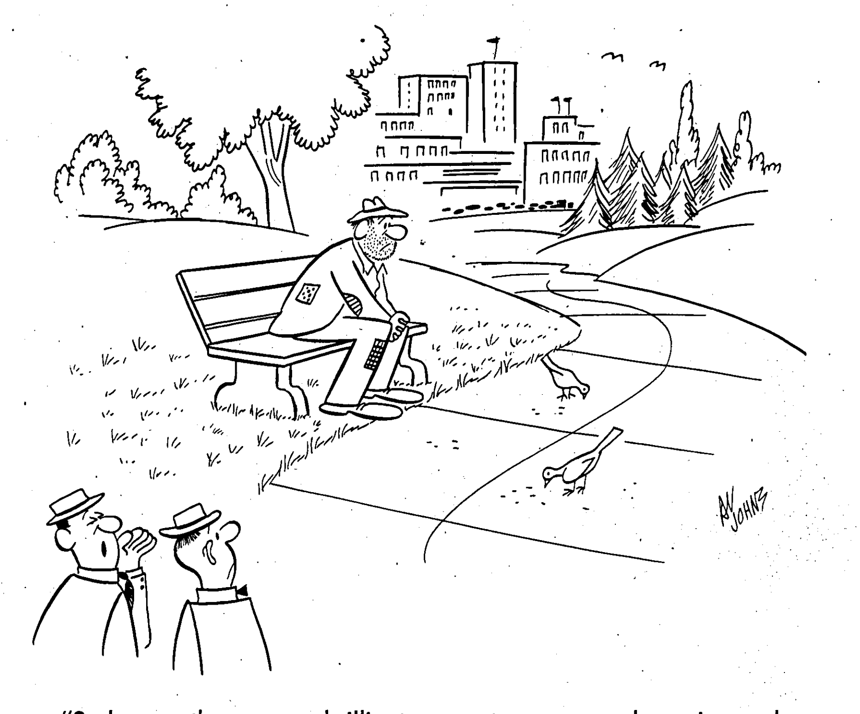
● A selected group of students, enrolled in Russian I at Stanford Univ., are being taught the fundamentals of the language on teletypewriter terminals connected to a central PDP-8 computer. The computer, preprogrammed by the course instructor, prints out the instructions to the students; questions are asked in Russian by a tape-recorded voice. If the student gives a wrong answer, the computer prints out, "No, try again." If the answer is still incorrect, the right answer is printed out in the Cyrillic (Russian) alphabet. The computer is also programmed to keep track of the student's progress and to give him new material as his competence increases. The project, sponsored by a $100K grant from the U.S. Office of Education, has been devised by Professor Joseph Van-Campen, associate professor of Slavic languages at Stanford.

● Price reductions from 10% to 20% on typical configurations of the SEL 810A, 840A, and 840MP computer systems have been announced by Systems Engineering Laboratories. A 4K 810A will sell for $18,000 and an 8K 840A for $60,000. Delivery schedule is 45 days.

● Control Data Corp. has consolidated its educational business into an Education Services Organization to handle both the CDI and the recent acquisition (along with CEIR) of Automation Institutes of America (AIA). General manager of CDI, L. G. Kinney, and president of AIA J. E. Wright will both report to N. R. Berg, vp, administration and personnel, CDC.

shortlines . . .

The Wright Line Div. of Barry Wright Corp. has acquired ElectroMechanics Corp. of High Point, N.C., whose portable punches Wright Line has been marketing. Albert Raulston will be manager of the department and James V. Simone will be development engineer . . . Ohio State Univ. will grant its first degrees in computer and information science at the end of the winter quarter . . . Control Data has given $296,056 to the Courant Institute of Mathematical Sciences at New York Univ. for work on time-sharing; the group has developed SHARER for the 6600 . . . In the U.K., Pergamon Press Ltd. has taken over the publishing activities of Computer Consultants Ltd. . . . Getting ready for the coming decimalization of Britain's currency, Woolco Department Stores (a division of F. W. Woolworth and Co. Ltd.) has ordered an optical character recognition system from NCR . . . The Third National Convention of the Association for Educational Data Systems will be held in Fort Worth, Tex., April 30 through May 3 . . . NCR has given $150,000 to the National Retail Merchants Association for development of a new computer-based system for reporting operating statistics to the NRMA membership. . . . We hear that IBM has over 100 2250 graphic terminals in the field . . . An ad hoc I/O interface committee under USASI X.3.2, studying the feasibility of a standard peripheral adapter for the last nine months, still can't determine whether such a system would ease the problem of interfacing different equipment makes or create more costly problems . . . ■



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Communications configurations provide for up to 64 duplex line terminals, with the number of possible remote devices almost unlimited. Utilizing an intermix of codes and speeds, the UNIVAC 9400 can communicate with a full range of peripheral terminals, the UNISCOPE® 300 visual display unit and the DCT-2000 as well as many other processors such as the UNIVAC 1108 and 494 Systems.

Designed with a supervisor control program for multiprogramming, the UNIVAC 9400 will run up to five main-chain programs at the same time. For example: 1) responding to inquiries from remote terminals, 2) updating accounts receivables, 3) updating "in process" inventory, 4) sorting disc or tape files, 5) solving complex mathematical equations —all can be processed concurrently.

Peripherals include industry standard discs and tapes. Tape systems can be expanded from 4 to 16 drives, from 34 to 192 KB. Disc configurations provide from 2 to 8 UNIVAC 8411 Disc Drives. Each has a 7,250,000 byte capacity and 75 millisecond average access time.

The complement of software includes full COBOL and FORTRAN, RPG and BAL, among others, in tape and disc-oriented systems plus other proven programming and testing packages.

A basic UNIVAC 9400 tape or disc system is available at monthly costs beginning at about $6,000. Extend it, expand it, make it grow with you. Yet—no matter how big you make it—it can still be part of one large computer family—the UNIVAC 9000 Series.

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world report

PRICE/PERFORMANCE NOD GOES TO ICT OVER IBM

ICT picked January to unveil its next phase of evolution in the 1900 series. The suffix A has been added to the models 1901, 02, 03, 04 to indicate the latest machines with improved cost-performance. This 25-bit-word, six-bit character range has been transformed into an integrated circuit series. Because of devaluation, most foreigners importing into the U.K. have hiked their prices around 10%. With the lifted performance of the 1900 series, ICT has raised throughput rates.

Coupled with the new price structure of the market, ICT has widened the gap in its own favor by as much as 15% when compared with IBM systems. This is on the 1902A which competes with the new model 25. But the real advantage has come at the bottom end of the market. The 1901A sells at $75K for the basic card or paper tape system. But twin exchangeable disc pack stores are available on a configuration costing $120K. This gives ICT its big inroad into the carefully nurtured "direct access" pitch of IBM to the small to medium dp user.

These areas are already under attack. But the big success for January came in the clinching of an order from one of the companies belonging to the giant Imperial Chemical Industries. This number one chemicals and plastics group in Europe went standard on 360 shortly after its announcement. Like many other powerful managements, its dealings with IBM were straight into New York. Breaking through the curtain into ICI was a major achievement for ICT.

INTEREST RISING IN OPTICAL MASS STORAGE

Intense interest in optical methods for cheap mass storage has begun to emerge in the U.K. ICT has a photographic system under wraps. It depends on fairly conventional photographic techniques for holding millions of characters of information in a backing store. The equipment is expected to surface in applications with massive library-type files.

At a much earlier research stage is a storage device made from crystals of common salt (sodium chloride). This has been produced at the Physics Department, University of Warwick, by Dr. M.R. Tubbs. On a crystal of salt two centimeters square Dr. Tubbs can store up to 20 million bits. Tubbs says that retrieval times in the microsecond range are feasible for such a device. The difficulty is finding a fast optical scanning method needed for a read-out mechanism.

The sodium chloride memory element came from research into solid state materials at Warwick. Electron microscope analyses of substances in earlier work has shown that colour changes could be brought about in quite common compounds in the alkali halides (e.g., sodium chloride and potassium chloride). Further study of the reasons for the colouring showed that various materials could be first coloured and then bleached by electrons, laser beams, and intense

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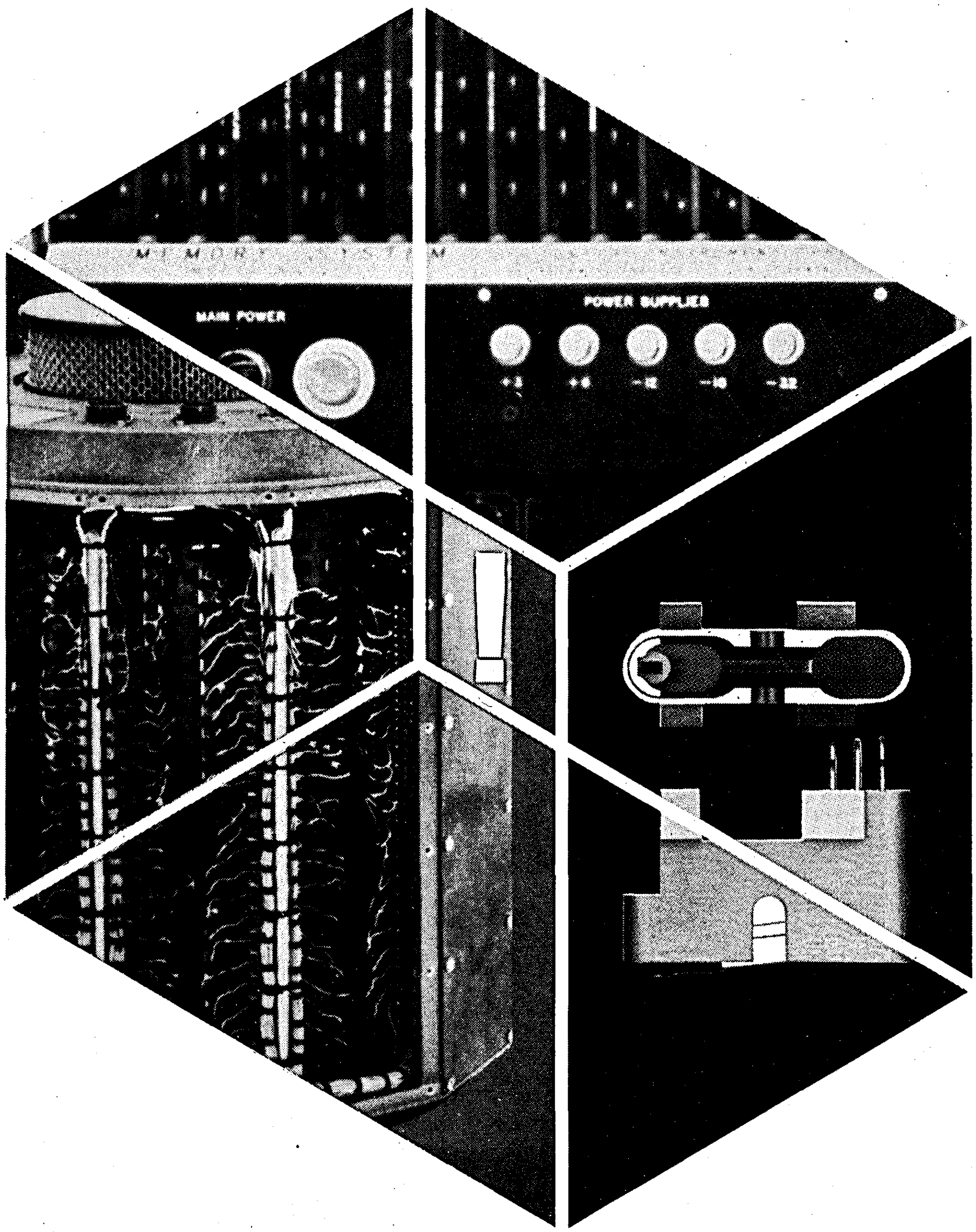
MAIN POWER
POWER SUPPLIES

light. Tubbs describes a practical memory made from a crystal of salt as being about postage stamp size. It would be divided into a grid of millions of storage locations, each about two microns square.

NEW CODING SYSTEM FOR INFORMATION RETRIEVAL

Serious consideration is being given in the U.K. to a new coding system designed to crack problems inherent in information systems built on a very broad data base. Author of this latest piece of software is Gordon Hyde, scientific director of Datatrac Ltd.—one of Europe's youngest consultancies. He has come up with a package which can be applied to administrative dp and technical information retrieval.

Hyde has an algorithm and a thesaurus that covers the medical and chemical fields. The thesaurus is coded in non-commutative manner (allowing for fine discriminations such as the difference between black shoe and shoe black). The mathematics of the system are hexadecimal and so OK for eight-bit-byte machines. Hyde's claims are being heeded by national institutions in medicine and chemistry that would like to unravel the incompatibilities and restrictions which have built up in information retrieval.

JAPANESE GOVERNMENT HELPS HOME COMPUTER INDUSTRY

All signs seem to point to a strengthening of Japan's indigenous computer technology and to indicate that national policy is bent on further improvement. After a long hassle the Ministry of International Trade and Industry and the Post Office have agreed on terms of expenditure and management of the new Japanese Data Processing Development Centre. The Ministry has also slapped some heavy terms on the leasing contracts made through the Japan Electronic Computer Co. Financed by the Japan Development Bank and the Government, the leasing company acts as money lender for the majority of rental deals. Government edict has gone out that the terms of rental should ensure that a large percentage of any system has been made locally. Little help will be forthcoming for any machine with more than a token volume of imported components on board.

NEW U.K. FIRM WILL DELIVER IN MAY

In spite of governments intervening right, left and centre, there is still some free enterprise left abroad. After some teething troubles, a new U.K. firm, Computer Technology, is getting on its feet. Its product, Modular One, was mentioned briefly at conception a year ago. And it pitches directly at Digital Equipment Corp., which has been scooping up the European market in the under $25K class with little opposition. Modular One is a 16-bit system aimed at a slightly wider market with the first machine at $24K. Deliveries start in May and 30 systems are scheduled for this year. CT's design-king is Ian Barron, ex-Elliott Automation, who designed the logic for the Elliott 803--five years ago the most successful European machine of that generation.

ANOTHER SMALL ONE— AND AT UNDER $10K

A more modest effort to meet the demand at the small machine end has come with Micro 16: again a 16-bit-word machine. But this one is priced at $9,600. The basic system includes a 4K core, I/O typewriter, and 10 characters/second paper tape I/O. The basic model goes on a desk top. Expansion upwards is in 4K core blocks, a hardware multiply-divide, 16K drum and faster I/O including mag tapes. The company, Digico Ltd., is headed by Keith Trickett and Abo Hiiemae. It's their second machine off the drawing board since the company was registered in '66.

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Ici on parle ALGOL
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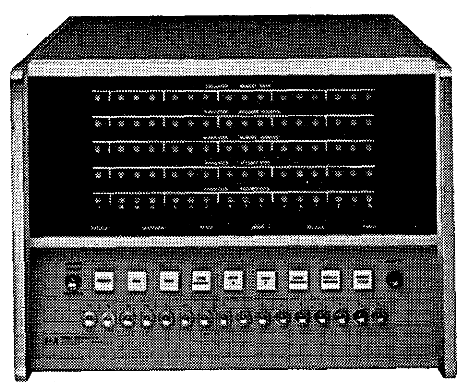
Powerful software available for HP's computers includes FORTRAN, ALGOL and BASIC Compilers, Assembler, and Basic Control System (BCS) with modular I/O drivers for device-independent programming. Compilers and Assembler generate relocatable code—linked by BCS loader at execution time.

Two computers available—2116A and 2115A—fully software compatible. Start speaking to an HP computer now—with a call to your local HP field engineer or by writing Hewlett-Packard, Palo Alto, California 94304. Europe: 54 Route des Acacias, Geneva.



The 2115A has 16-bit words, 2 μsec cycle time, 4K memory (expandable to 8K) and a $16,500 price including Teleprinter.

HEWLETT hp PACKARD

DIGITAL COMPUTERS

06721

CIRCLE 55 ON READER CARD

washington report

GSA TAPE CONTRACT AWARDED; ONLY ONE MAKER GETS TOP RANK

Ampex and 3M will supply the federal government with $10-13 million worth of 7- and 9-channel mag tape under contracts awarded by GSA.

Ampex won about 85% of the total procurement. Prices accepted by GSA ranged from $12.25 to $15.10 a reel and up to a million reels will be purchased. All QPL suppliers bid on the contract.

Nine tape manufacturing plants are now on the quality products list. U. S. Magnetic Tape has the only Type I certification (maximum of one permanent error per 30 reels). Suppliers for Type II (permits up to 20 permanent errors per 30 reels) are Audio Devices, Ampex, RCA, 3M, IBM and Memorex.

A conference will be held in Washington this month to hear industry gripes about QPL test procedures. Revisions will then be proposed by GSA and submitted to manufacturers before adoption. A new tape testing lab at NBS, which will take over the work now being done at NSA, should be ready in about six months.

REVOLVING FUND STARTS OPERATION

The first expenditures from the Brooks Bill's dp revolving fund include the purchase and lease of a 7074 to the Labor Dept., and a Honeywell 1200 for the Patent Office. Further investments will include a small test of a keypunch pool in NYC; a programmer pool in GSA's sharing exchange program on a pilot test basis; and possibly a service bureau (GSA calls it a "joint-use facility") in Denver, under tabs of the Interior Dept.

FCC EXTENDS UTILITY INQUIRY, OK'S WU SERVICES

Computing & Software, Inc. advocated a new toll-free data transmission service in response to FCC's computer utility inquiry last month. C&S also maintained that commercial service bureaus are custodians, not controllers, of data, and shouldn't be held legally liable for invasion of privacy.

Responding to a request from BEMA, FCC allowed another 30 days for participants in the inquiry to file statements. The new deadline is March 5th.

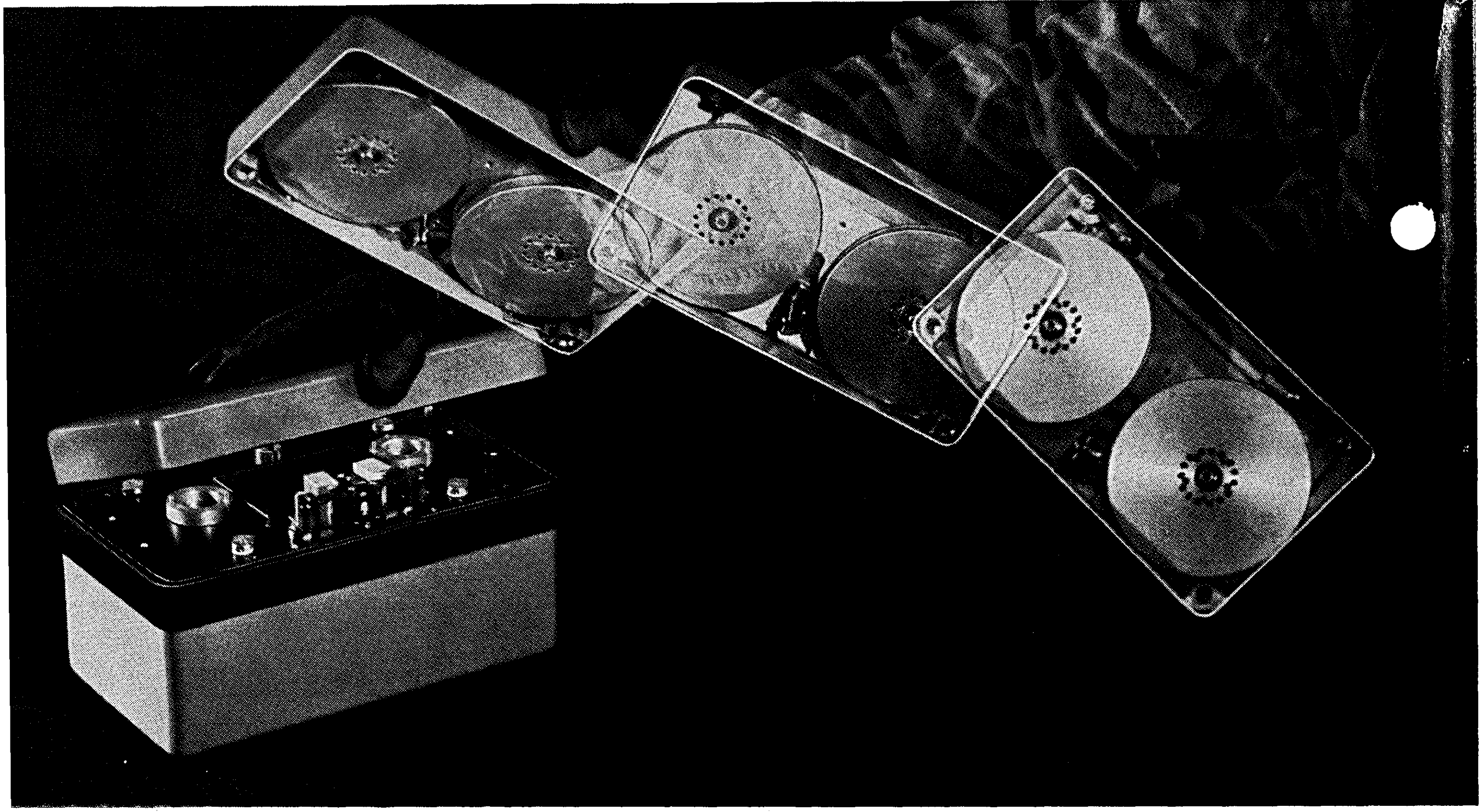
Meanwhile, the commission allowed WU to begin its SICOM and INFO-COM services. Objections of Bunker-Ramo and Scantlin Electronics were denied mainly because WU's new services encompass "functions...(which) can... find (their) counterpart(s) in other common carrier communication services." This determination, however, is "without prejudice to our further examination of this question in the...computer inquiry."

The commission added that, "as we see it, SICOM... will make available...a package communications service without the variety of data processing services available, for example, in the Bunker-Ramo TOPS service. The choice of either SICOM...or TOPS...would appear to be a reasonable choice for a (stock) broker to make."

The FCC, says one source, "seems primarily concerned with maintaining a competitive balance between carriers and data processors, rather than excluding carriers completely from the commercial dp market."

CAPITOL BRIEFS

Despite reservations about the new ASCII 800BPI standard inside and outside the federal government, BOB intends to make it binding on all federal dp users within the executive branch. An order, publicly signed by LBJ, is expected soon...PILOT was recently junked and sold to Frank's Used Auto Parts, Marlboro, Md., for $226.75. Sic transit gloria.



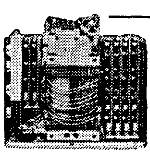
Fly Now – Play Later

In a surprisingly compact package, Sanders gives you an Airborne Magnetic Tape Recorder with the ease and convenience of cartridge loading, designed so you can reload the recorder even with flight gloves on and without removing the recorder from the aircraft.

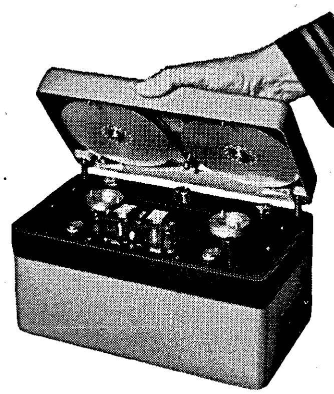
We designed it to take a lot . . . and give out even more. Built to fly in the most rugged environment, it will record up to 24 hours of continuous data and reproduce it on the spot or play it back later on your favorite laboratory instrumentation recorders.

Analog versions with complete record/playback electronics are fully compatible with IRIG standards. Digital versions with complete write/read electronics are computer-compatible and available for synchronous or asynchronous operation.

Our brochure SA-202 covers the complete story on Sanders DS-4100 Series Airborne Recorder. Call Sanders Associates, Inc., Data Storage Department, Nashua, New Hampshire 03060. Phone: (603) 883-3321.



Sanders also has the logical choice for airborne core memories that are MIL-E-5400 qualified. Write for bulletin SA-196.



- Meets full MIL-E-5400 requirements
- Operates at 50 watts input power from −54°C. to +71°C. at altitudes up to 70,000 feet
- Two, four, seven or nine tracks
- Tape speeds up to 37½ ips.
- Total package weight: 16 pounds
- Package dimensions: 6x6x11

Creating
New Directions
In Electronics

SA SANDERS ASSOCIATES, INC.
DATA STORAGE DEPARTMENT

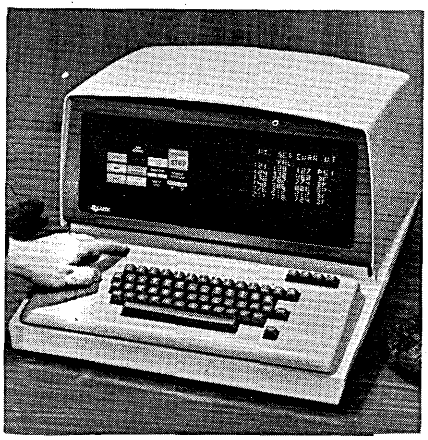
*T.M. SANDERS ASSOCIATES, INC.

CIRCLE 56 ON READER CARD

new products

crt/panel terminal

The Data-Screen Display Terminal is made to customer specs, featuring both a CRT for dynamic data and a panel for fixed information. The latter section, which can be on either side or in the middle, accommodates up to 144 fixed alphanumeric messages and symbols, visible only when illuminated. The 8" rectangular CRT displays 128 stroke-written characters ⅜" high in eight rows of 16 charac-



ters each; displays of 200 and 512 characters are also available as standard models. The character repertoire includes 26 alpha, 10 digits and six punctuation marks, plus a flashing cursor for character and line indication; data can be added, changed or deleted by the operator. The system uses an 8-bit code. TRANSISTOR ELECTRONICS CORP., Minneapolis, Minn. For information:

CIRCLE 130 ON READER CARD

gp computer

The third and largest system in the Univac 9000 series is a 9400, compatible with the 9200/9300 announced mid-1966, and intended to add multiprogramming and real-time capabilities to the line. The monolithic system uses a plated-wire memory with capacity ranging from 24,576-131,072 (8-bit) bytes. Cycle time for two bytes is 600 nsec, or an effective 300 nsec one-byte time; add time for two 32-bit words is 6 usec.

The tape and/or disc 9400 has a 67-instruction set and 32 full-word general purpose registers. Seven levels of interrupt are featured: supervisor call, program execution, interval timer, selector channels 1 and 2, and shared and non-shared multiplexer channel. The tape system which comes with a Basic Tape Operating System and Tape Operating System, uses 4-16 tape drives for 34K-192K byte read/write speeds. Simultaneous read /read, read/write, write/write is optional. A disc system, also with two operating systems offered, can have 2-8 8411 drives for 14.5-58 megabytes capacity. The 8411 has a transfer rate of 156K bytes per second.

For communications, the 9400 has a multiplexer channel with eight shared sub-channels each able to accommodate a standard control unit handling 16 I/O devices.

A combination of four control units and four Data Communications Subsystems (each DCS handling 32 simplex or 16 duplex lines) can also be used. Two selector channels for high-speed devices are optional. Among remote devices available with this system are the Uniscope 300 CRT terminal and the DCT 2000 terminal. For remote print stations, Univac 1004, 1005, 9200 or 9300 systems may be connected on-line to the 9400 by means of one of the eight subchannels of the multiplexer channel.

Multiprogramming capabilities incorporated in the four operating systems provide for processing up to five concurrent programs, such as sequential batch and random processing, disc or tape sorting, communications. Other software included is data management system, job control stream operating, basic assembly language, COBOL 65, ASA FORTRAN, and service

PRODUCT OF THE MONTH

The 101 information retrieval software system is intended for maintenance of large files and interrogation in ways the user has not predicted. Response to a query is reportedly orders of magnitude faster than any system that uses a sequential search of the total file; the reason is that developer Computer Corp. of America has employed proprietary software techniques (making heavy use of the hash coding principle) which permit direct retrieval, without search, of the data required.

CCA has run benchmarks of system speed using a 128K 360/40 with a 24,000-record U.S. Census file. One example is this request:

1) Find all items for which sex = female, race = white; 2) Count items in 1; 3) Print count in 2. The count was 10,770 and took 2.68 seconds to read the request card, print them out, perform the request, and print out the count. A sequential search would probably take upwards of 10 minutes, says CCA. An increase in file size has almost no effect on 101 speed.

The 101, which has a query language learned in a few minutes, permits a non-programmer to query update, store and edit files. Up to 1.5 million fields can be stored by the 101. The files do not have to be in fixed format, so each record can have any amount of information in it. Data is stored by attribute: value pairs (name = Jones), and each of these pairs can have up to 255 characters. (Consistency in file is up to the user, who can call for a printout of all attributes when updating).

The 101 also permits interrogation of several files and cross-referencing among them. The system also has a formatting capability which lets the user specify how the data will be laid out on the printout.

Required minimum configuration is a 65K-byte IBM 360/30 with DOS, 2311 disc drives (one to four), three mag tape drives, line printer and card reader.

For $25K, CCA will install the system, help set up the file if needed, provide one-week consulting and user education and an instruction manual. A six-month warranty is given against programming bugs. The 101 can be installed and operating within 60 days of contract. The firm is also making plans to lease the system.

Future CCA systems planned include the 102 IR system for OS 360 and a 103 version for on-line retrieval. COMPUTER CORP. OF AMERICA, Cambridge, Mass. For information:

CIRCLE 131 ON READER CARD

and utility programs.

Peripherals available include two printers (900-1100 lpm, 1200-1600 lpm), 600-cpm card reader, 250-cpm punch.

Monthly rental for a basic configuration with 24K byte memory, four tapes, 1100 lpm printer, card reader and punch is $5880, or $5175 with a five-year lease. Purchase price is $204,940. Delivery begins second quarter 1969. No plans for the 9500, originally to have been announced fall '66, were mentioned. UNIVAC DIV., SPERRY RAND, Philadelphia, Pa. For information:

CIRCLE 132 ON READER CARD

bank credit software

The Comarecs master revolving credit system includes planning, programming, technical assistance, forms, etc., provided by the firm. Written in COBOL, it reportedly "combines all types of loans in a bank's installment credit department used by each customer into a single account, including check credit, overdrafts, guaranteed bank checks, personal and home improvement loans . . . as well as 30-, 60-, and 90-day charge accounts for bank loans." Applicable to any size bank, it calls for at least $100 million in deposits and a trading area of 100,000 people. COMARECS INC., Washington, D.C. For information:

CIRCLE 133 ON READER CARD

data acquisition

Data acquisition system configuration includes a 4K Raytheon 703 computer (expandable to 32K) with up to four mag tape units, buffering amplifiers and a Multiverter data system. The Multiverter performs signal multiplexing and A/D conversion; throughput rates from 15 KC to 55 KC for up to 96 channels of multiplexing in increments of eight channels are available. Channel sampling, under program control, is either sequential or random; resolution of the Multiverter is 10-15 bits including sign. Maximum system error, excluding analog playback equipment, is 0.02%. RAYTHEON COMPUTER, Santa Ana, Calif. For information:

CIRCLE 134 ON READER CARD

direct access storage

The 8410 disc file is a direct access storage system for the Univac 9000 series; the file provides removable storage of 3.2–12.8 million bytes, or 6.4–25.6 million digits in packed decimal format. The basic 8410 system includes a master dual disc drive expandable in increments of one to a total of eight drives. Each drive holds a reversible disc cartridge with two storage surfaces, one of which is online. By interchanging disc cartridges, "unlimited" storage is provided for applications which require serial processing. Each drive can access 10,000 160-byte records plus an 8000-byte fast-access track. All drives contain a fixed head for reading and writing on the Fastband and a movable arm with two heads for the remainder of the disc surface. Average time to locate and read a record is 135 msec.

The file also has a buffer that permits all disc reading, writing, checking or searching to be performed simultaneously with processing and peripheral operations. Programming support for the system includes RPG, supervisor, system file and disc loader, assembler, IOCS, utility programs, control stream operations and library services. UNIVAC DIV., SPERRY RAND CORP., Philadelphia, Pa. For information:

CIRCLE 135 ON READER CARD

program simulator

Unite I allows simulation of SDS 900 series computers on a Sigma 5 or 7. Object decks for the former can be run on the latter without re-assemblies, recoding, systems tape conversions, or tape file conversions. It simulates all of the CPU and I/O features of the 900, assuming corresponding I/O gear, and also includes built-in selective trace, core snapshots, console interrupts, and the ability to use direct Sigma code. Thus, the user could save mainframe time by recoding only the inner program loops. UNITED COMPUTING CORP., Redondo Beach, Calif. For information:

CIRCLE 136 ON READER CARD

payroll package

The payroll accounting system, written in basic assembly language, handles five categories of standard taxes, including state and local tax withholding and reporting requirements, producing also a variety of management reports. The system allows checks to be written or deposited to bank accounts as desired. It is operational on 360's under DOS, and requires 32K bytes and three discs. The package also provides for multiple payrolls within the same company, and each employee record can contain multiple categories of rates, hours and earnings. SOFTWARE RESOURCES CORP., Los Angeles, Calif. For information:

CIRCLE 137 ON READER CARD

incremental recorder

Model I is a large reel incremental recorder capable of handling all sizes, including the standard 10½" 2400-foot tape reel. The unit has stepping rates to 400 steps a second, and is available in both 200 and 556 bpi density. Standard features offer lateral parity, LCC and IRG generation, and rewind by switch control. Priced at $2500, delivery is approximately three months after receipt of order. DELTA-CORDERS, INC., Burbank, Calif. For information:

CIRCLE 138 ON READER CARD

microfilm printer

The Series F Electron Beam Recording system is an off-line microfilm printer that uses the new dry-silver 16mm microfilm, which is developed by heat, instead of liquids. The unit has a speed of 60,000 cps, which is translated into a maximum 20 frames/second. The standard system has 60 printable characters, all upper case. Optional are 26 lower-case characters, plus 10 Greek characters. Also optional is the ability to merge the computer-generated data with graphics recorded on 35mm microfilm. The tape drive in this system is a 7- and/or 9-track unit reading 200, 556 or 800-bpi densities at 75 ips. 3M CO., St. Paul, Minn. For information:

CIRCLE 139 ON READER CARD

shop data acquisition system

The Shoptrol Monitor and Data Collection system establishes a central control area which provides the means for efficient job scheduling, machine loading, and employee job assignments; individual time cards and production reports from the floor are eliminated. The end product is a complete departmental performance report with employee efficiency printed 15 minutes after the end of each shift. During report printing, every transaction is stored on mag tape for payroll, inventory and accounting processing. Throughout the work day, summaries by employee, by machine, or by job are available on request.

The basic system consists of three units: a data collector, a transmitter, and a badge reader. Input to the badge station is from 15-column alphanumeric Hollerith-code plastic cards; information thereon is trans-

new products

mitted to the collector at speeds up to 120 cps. The transmitter can accept either the plastic cards or 80-column punched cards and also transmits this to the collector at up to 120 cps.

The Shoptrol collector can accept information from up to 10 data transmitters and as many as 26 badge or attendance stations. This information is output in the form of paper tape, cards or magnetic tape, or (in the more sophisticated on-line system) output directly to a computer.

In the on-line system a 32K Interdata 3 computer with 500K drum memory is currently being used, but the system is "basically" compatible with any computer system.

In the system, all productive and nonproductive times are entered as they occur; the computer makes efficiency computations as often as desired and prints out exception reports whenever efficiency falls below any preset percent of standard for a 15 minute period. Requests for further information may be obtained from the computer by use of up to 16 remote Teletypes transmitting through standard interfaces in USASCII code. Shoptrol also provides an alarm system, and a management communication system with paging and plug-in telephones. ELECTRON OHIO, INC., Cleveland, Ohio. For information:

CIRCLE 140 ON READER CARD

tape transport

The SC-1030 tape transport has bidirectional tape speeds to 37.5 ips at 800 bpi, NRZI, as well as 1600 bpi phase modulated recording. The unit is 7- or 9-channel compatible; semiautomatic tape loading is accomplished in less than 15 seconds. Rewind speed is less than 4 minutes on a 2400-foot reel; speed tolerance is ±5%; dynamic skew is 5 usec. POTTER INSTRUMENT CO., Plainview, N.Y. For information:

CIRCLE 141 ON READER CARD

system/360 addition

The 360/25 is identical to the 360/30 in instruction set, offers the same programming support and peripheral options, and also provides emulation for 1401, 1440 and 1460 programs. But it costs less than the 30, has an internal speed only .67 times as fast, a smaller memory capacity, and a slower data rate for peripherals.

The price range is from about \$3900-\$10K a month, or \$192K-480K for purchase. A typical disc system goes for about \$5330/month and includes a 16K-byte, two-disc drive with a 1403 mod 2 printer, 2540 card reader/punch, and a 1052 mod 7 console typewriter. The same configuration in a model 30 would rent for about \$1200 a month more.

Main memory comes in four sizes of 16K, 24K, 32K, or 48K bytes. Cycle time is 1.8 usec for two bytes or an effective time of 900 nsec per byte. This appears to be faster than the 1.5 usec cycle time (one byte) of the 30, but the 30 takes only 22 usec for a one-byte add versus 35 usec for the model 25. (Control store in the 25 takes 900 nsec versus 750 nsec for the 30, and the control store access width of the 25 is 18 bits versus the 30's 58 bits.)

The 25 also has a free floating point option to accommodate scientific applications.

Rather than a read-only memory used by the 30 and larger 360's, the 25 has a reloadable control storage for the instruction sets of either the 360 or 1400 series. The 25 also has a scratch pad memory of monolithic circuits which can switch up to 64 bytes in and out of storage in 180 nsec.

Another first for the 360 line is mainframe-integrated control units, which afford a more compact system. These units, which perform the same functions as the 2821 and 2841 systems, can handle up to four 2311's, a 2540 card reader/punch, 1403 mod 2 or 7 printer, and a 1052 console printer keyboard. The 25 has an optional multiplexer or selector channel, which can handle up to eight more control units at a 30 KB data rate. The multiplexer channel will provide up to 32 subchannels (versus 224 on the 30).

The 25 can use all peripherals available to the small- and medium-size 360's, including the 2260 display, audio response units, and process control devices. A new feature on the operator's console is that a variety of commands and inquiries may be entered via the keyboard, rather than dials or switches. Programming support includes the BOS, TOS, and DOS systems; and COBOL, FORTRAN and PL/I. One observer noted that the limited memory size of the system would attract users to the 16K PL/I subset rather than the available COBOL compilers, the smallest of which are 24K and 32K.

The 25 competes with several computers in price and/or performance: both the RCA 70/25 and 35 (the 30 is not as fast as the 35 and has less memory than both), the Burroughs 2500 (56 usec add time), the Honeywell 125 (which is slower but offers program conversion aid rather than emulation of the 1400 series). The 25 slides in between Univac's 9300 and its recently announced 9400. IBM DP DIV., White Plains, N.Y., For information:

CIRCLE 142 ON READER CARD

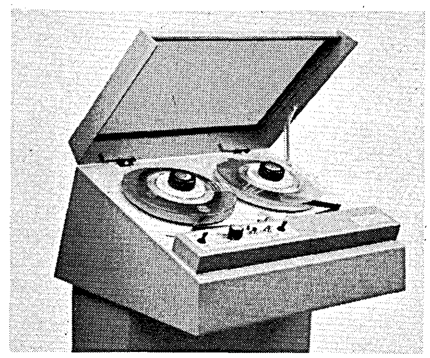
l-p package

A linear programming package, OMEGA, prepared by Bonner & Moore Assoc., Houston, Texas, is for the 1107/1108 systems, and is available through Univac data centers. It reportedly allows the user to state the problem in his problem-oriented terminology, and generates results in user-determined format. UNIVAC DIV., SPERRY RAND CORP., Philadelphia, Pa. For information:

CIRCLE 143 ON READER CARD

plotter transport

The Series 407 is a read-only mag tape drive designed to operate digital incremental plotters. It reportedly has plug-in compatibility with incremental plotters from Benson-Lehner, CalComp, and Houston Omnigraphic. It can read any IBM-compatible 7-track half-inch tapes (200, 556 or 800 bpi) on an 8½-inch reel. Standard features



include high-speed rewind, beginning of tape and broken tape detector, single or continuous plot mode switch, and data read indicator. Various configurations allow local or remote plotting via phone lines. TRANS-CONTROLS INC., Monterey, Calif. For information:

CIRCLE 144 ON READER CARD

communication terminals

Model 5072, a punched paper tape transmitter and hard copy printer-receiver, interfaces with dial telephone circuits through a type 202C data set. For leased line service, the modem is a type 201B or Rixon Sebit 48 data set. Punched paper tapes are read at speeds of up to 300 characters/second and incoming data is printed at 300 lines/minute. The standard hard copy format measures 120 column inches wide, contains six lines/inch vertically, and utilizes a 64-character alphanumeric font. Up to six carbon copies are obtainable. The unit may be operated off-line to convert punched tape into printed copy. A paper tape handler, available as optional equipment, permits fully unattended operation.

Model 5079, a punched paper tape transmitter/receiver, interfaces with the type 202C and 201B data sets. Information is transmitted at 300 characters/second, received at 100 characters/second. Blocks of any size can be accommodated. This equipment can also be operated unattended when linked to a tape handler, and on an off-line basis, copy punched paper tape.

The 5072 rents for $750/month; 5079 for $300/month. Both units employ integrated circuits and handle all EIA 5-8-level punched paper tape codes. DIGITRONICS CORP., Albertson, N.Y. For information:
CIRCLE 145 ON READER CARD

selection and reporting program

SCORE (Selection Copy and Reporting) system is for use with the 360/30, and requires no program logic or computer debugging. The user specifies the basic criteria for selection and reporting on a card; reporting options allow for heading information, editing capabilities and control break processing. A copy option provides for the specification of output files in any format, and the selection option specifies the criteria by which input records are chosen. PROGRAMMING METHODS, INC., New York, N.Y. For information:
CIRCLE 146 ON READER CARD

keyboard printer

The TEN-10 input/output keyboard printer is basically a Selectric typewriter with added magnetic read relays and electronics to interface with a computer system. Offered as an on-line peripheral to the OEM market (it is not a remote terminal), the unit operates at a speed of 15 characters a second, and will accommodate 15" paper widths. The TEN-10 can receive and output data at standard 0 and +5 volt logic levels. DATEL CORP., Palo Alto, Calif. For information:
CIRCLE 147 ON READER CARD

optical font adders

The NCR 11 series is a family of 10-key adding machines, including models that print in a machine-readable optical font. They have plus and minus multiplication keys, which give the operator a choice of regular, short-cut and negative multiplication, and an automatic stepover capability. NATIONAL CASH REGISTER CO., Dayton, Ohio. For information:
CIRCLE 148 ON READER CARD

terminal interface

For users of the IBM 1130 computer, there's now an interface system that requires no modification to the mainframe. It allows attachment of up to 15 Teletypes, 1050's or 2741's; a real-time clock is also available. The interface attaches to the storage access channel. HONIG TIME SHARING ASSOC. INC., Hartsdale, N.Y. For information:
CIRCLE 149 ON READER CARD

test data generator

An automatic test data generator—TDG/IMI—which can be used with any computer equipped with a COBOL compiler, creates a test data base to automatically check the various logic paths of COBOL programs. In accordance with DATA DIVISION specs, it achieves this by creating the following kinds of test data: random data within specified ranges, data with parts clustered around a specified value, data dependent upon previously specified test data, and invalid data to check out the error detection capabilities of the program. TDG/IMI accepts instructions in a COBOL-like language provided to a systems analyst or a user who knows the data being processed. INFORMATION MANAGEMENT, INC., San Francisco, Calif. For information:
CIRCLE 150 ON READER CARD

card readers

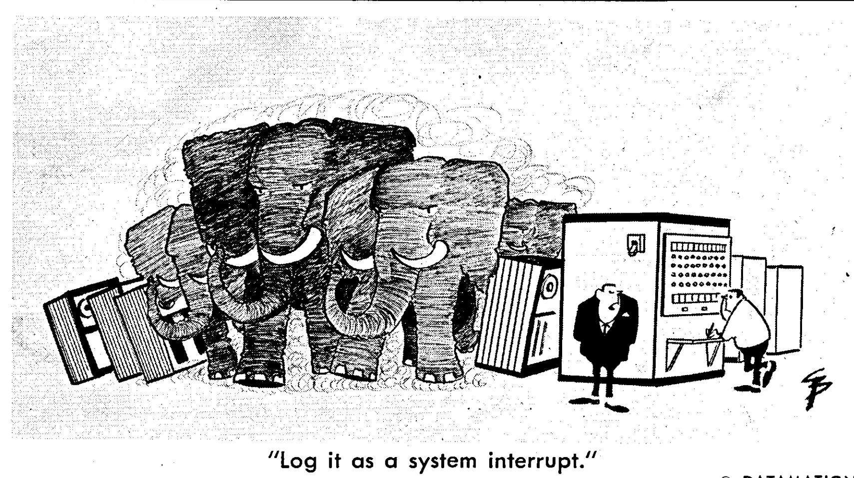
The 0707 card reader can be interfaced, via a teletypewriter and modem, to most communication terminals. Line transmission is in USASCII. The 0708 unit is designed to work in applications which require slow card reading with the ability to stop and hold on to each column. Both models, available to the OEM market, can read column-by-column in incremental mode at up to 10 cards a minute, or 40 cpm in a continuous mode. I/O magazines have a capacity of 500 cards. UNIVAC DIV., SPERRY RAND CORP., Philadelphia, Pa. For information:
CIRCLE 151 ON READER CARD

tape transport

Model 959 is an IBM-compatible unit with speeds of 60-120 ips; and 200, 556 or 800 bpi density. Options include 7- or 9-channel head, read/write electronics, write inhibit, erase head and address select. TEXAS INSTRUMENTS, Houston, Tex. For information:
CIRCLE 152 ON READER CARD

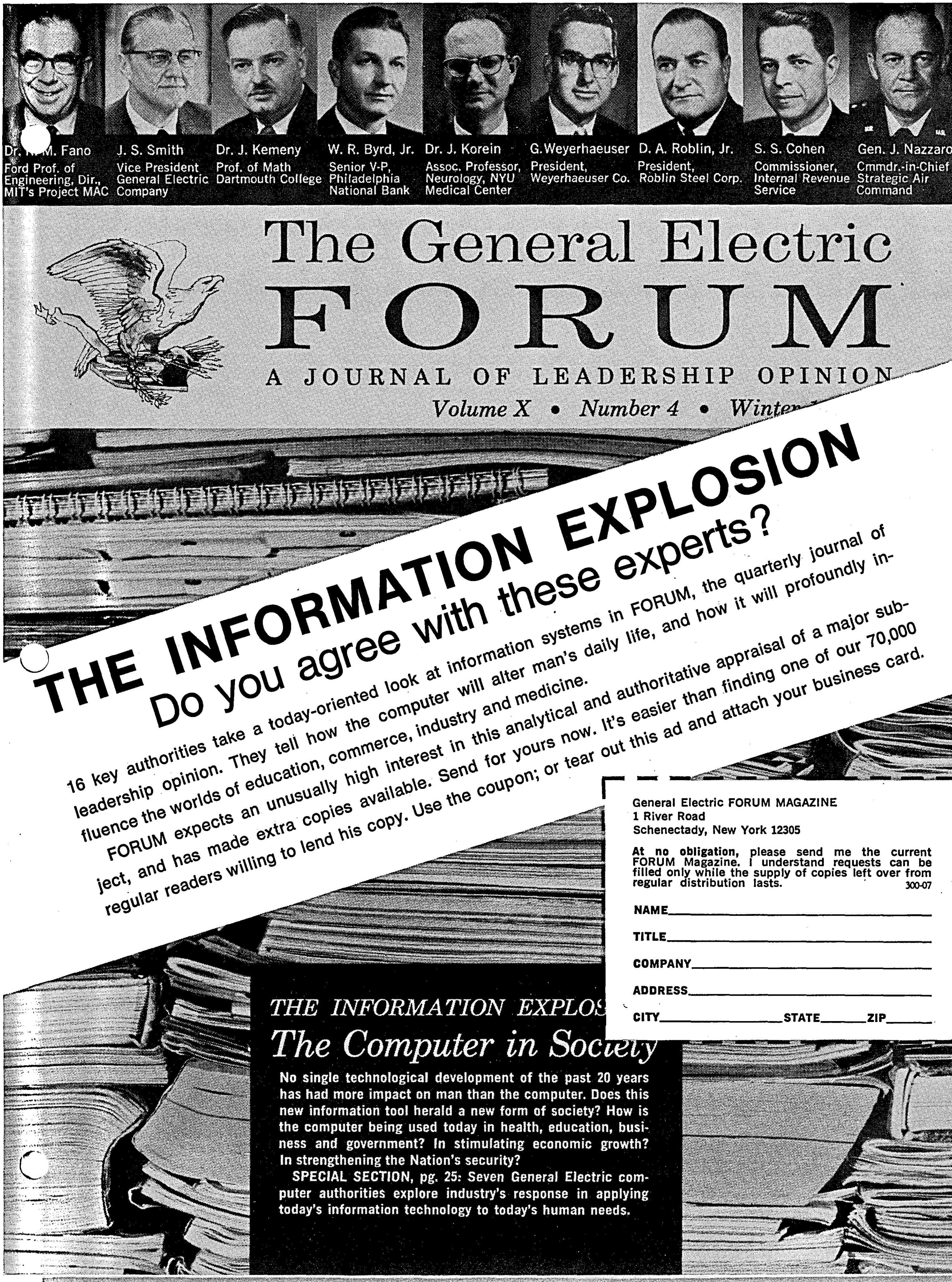
systems analysis forms

The ADS (Accurately Defined Systems) forms are designed for the systems analyst, and replace the narrative: the analyst's guidelines and concept which outlines the problem for the programmer and details the process for management. ADS is based on five forms which are filled out consecutively. The Report Definition states the objectives of the system and details the origination of the data; this form is then cross-referenced to other pertinent forms, either the Input Definition, the Computation Definition or the History Definition. Finally, the Logic Definition lists special rules for the handling of specific data. For use with any computer system. NATIONAL CASH REGISTER CO., Dayton Ohio. For information:
CIRCLE 153 ON READER CARD



"Log it as a system interrupt."

FOR G.E. CIRCLE 29 ON READER CARD→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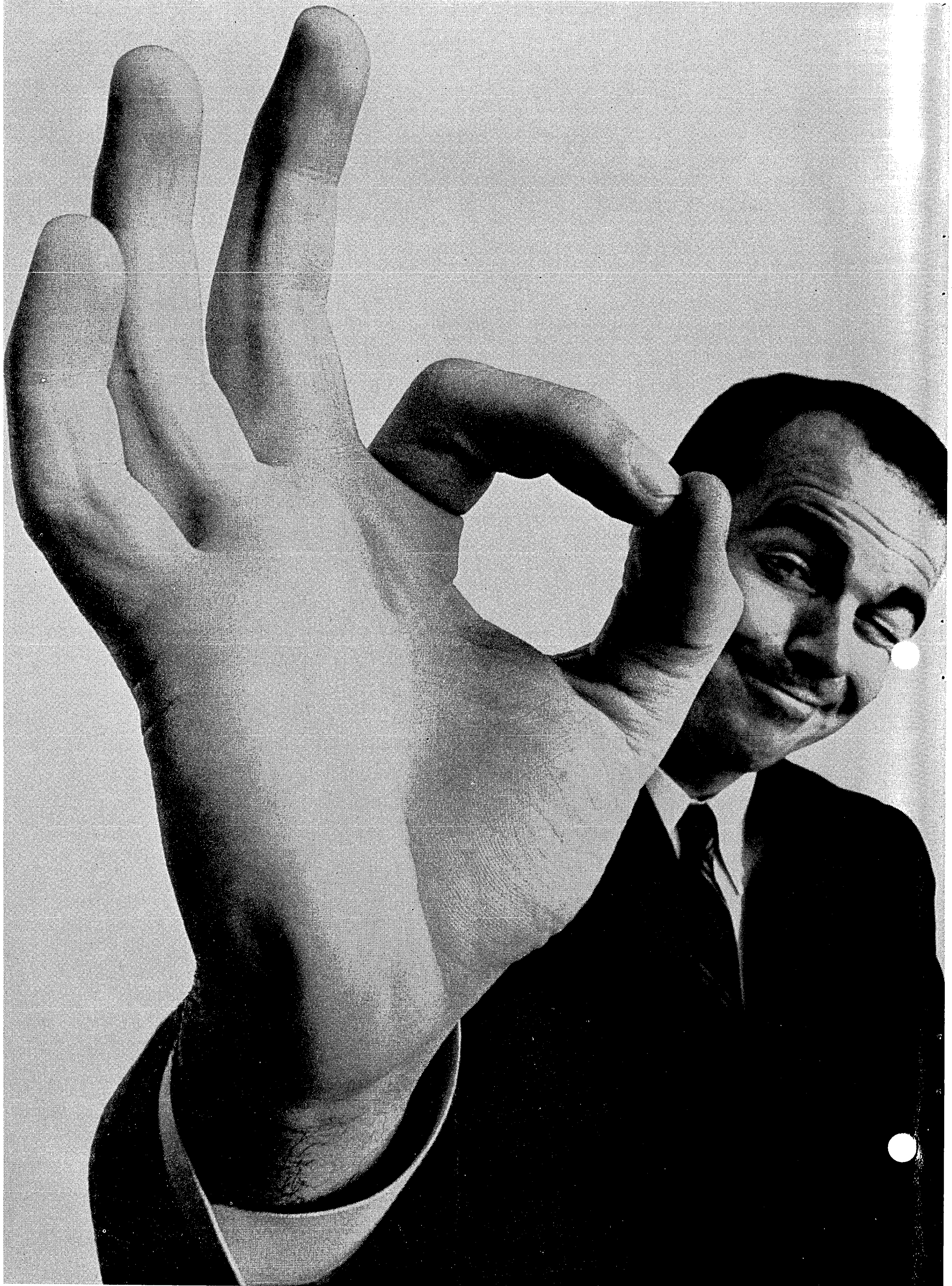
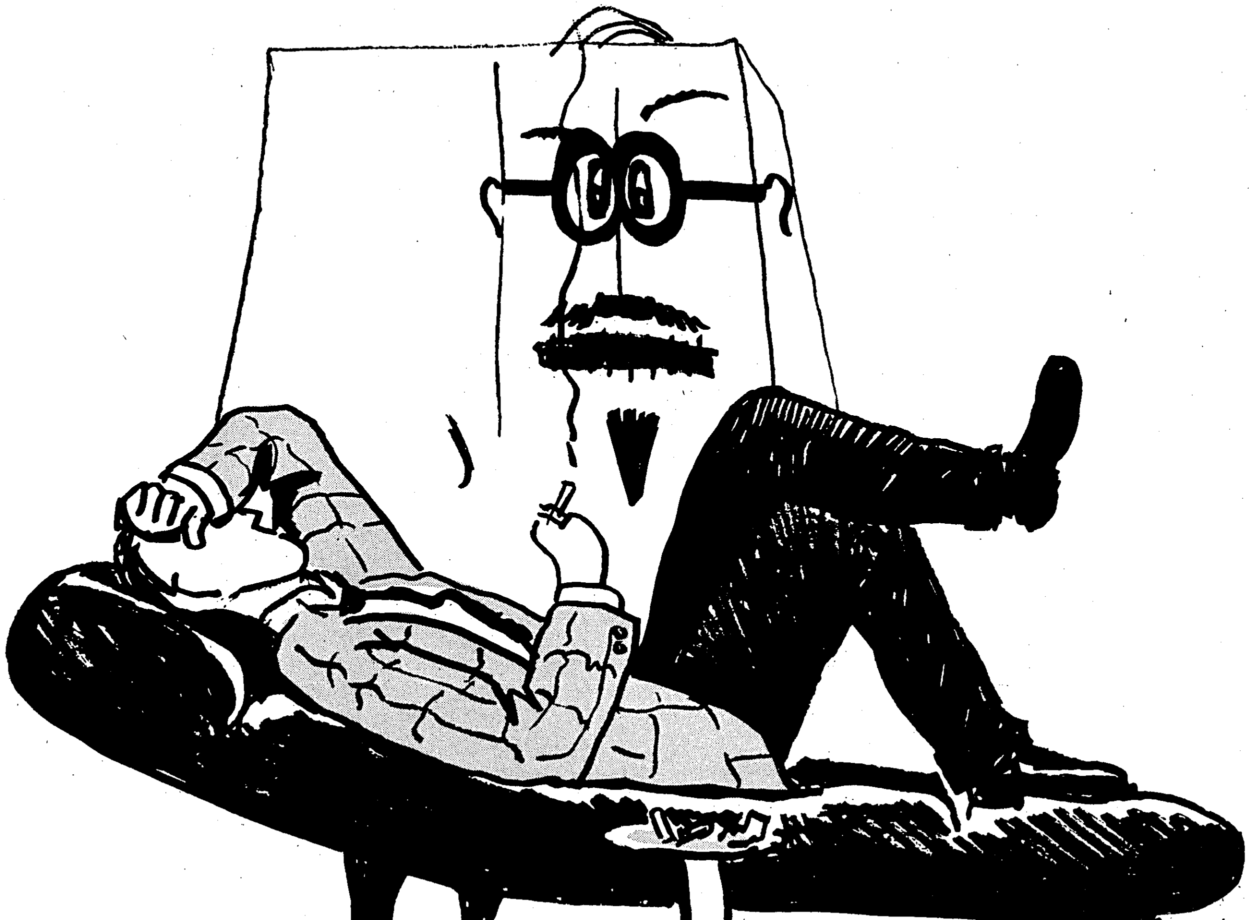
SPECIAL SECTION, pg. 25: Seven General Electric computer authorities explore industry's response in applying today's information technology to today's human needs.





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You can pour out your 24-bit problems to the SCC 655. This fully parallel, binary computer has a versatile and complete instruction repertoire that makes programming understandable. With 38 instructions, it stands out as the lowest investment in a 24-bit machine — $15,900. Features include: Integrated circuits ■ Direct memory access ■ Hardware multiply/divide ■ Indexing ■ Multi-level indirect addressing ■ Flexible input/output structure ■ Automatic subroutine linkages

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new literature

JOSS LANGUAGE: An introduction to JOSS (an on-line, time-shared computing service) for people having some programming experience. Presents summaries of actions that can be requested of JOSS and of the language for requesting these actions. Summaries are presented in three forms: 1) a pocket-size book for personal use; 2) a larger and more detailed piece for desk-top or console use; and 3) a poster-size summary for the bulletin board. AD-661 259. 33 pages. Cost: $3; microfiche, $.65. CLEARINGHOUSE, U.S. DEPT. OF COMMERCE, Springfield, Va. 22151.

ANALOG/HYBRID SYSTEM: 18-page brochure on model 580 desk-top analog/hybrid computing system describes the system's analog and hybrid features, design and operation of the master control panel and analog readout panels, programming, the digital logic system, the individual computing components, system expansion and options, applications and company support. ELECTRONIC ASSOCIATES, INC., West Long Branch, N.J. For copy:

CIRCLE 180 ON READER CARD

OPTICAL SCANNING SYSTEM: Six-page applications brochure describes how The Equitable Life Assurance Society speeded up processing of Medicare claims with Digitek 70 optical mark scanning system, which reads pencil marked forms and transfers the information directly to magnetic tape. Flow chart shows how keypunching and verifying are eliminated in the process. OPTICAL SCANNING CORP., Newtown, Pa. For copy:

CIRCLE 181 ON READER CARD

TIME-SHARING SCORECARD: Survey of on-line multiple user computer systems features data on 15 commercial time-sharing organizations and 35 research-oriented systems and on the cost of time-shared services. COMPUTER RESEARCH CORP., Newton, Mass. For copy:

CIRCLE 182 ON READER CARD

MEMORIES: Eight-page brochure includes descriptions and specifications for the company's 500-to-600-nsec ICM-500, 670-nsec ICM-47 1-usec ICM-40 1.5-usec ICM-42 and 5-usec TCM-32 integrated circuit core memories. HONEYWELL COMPUTER CONTROL DIV., Framingham, Mass. For copy:

CIRCLE 183 ON READER CARD

MEMORY SYSTEMS: 22-page catalog and standard price sheet contains specifications on the company's 513 standard coincident-current magnetic core memory systems with word and bit capacities from 128 x 8 to 4096 x 32. Operational theory, applications and packaging are illustrated and discussed in detail. FERROXCUBE CORP., Englewood, Colo. For copy:

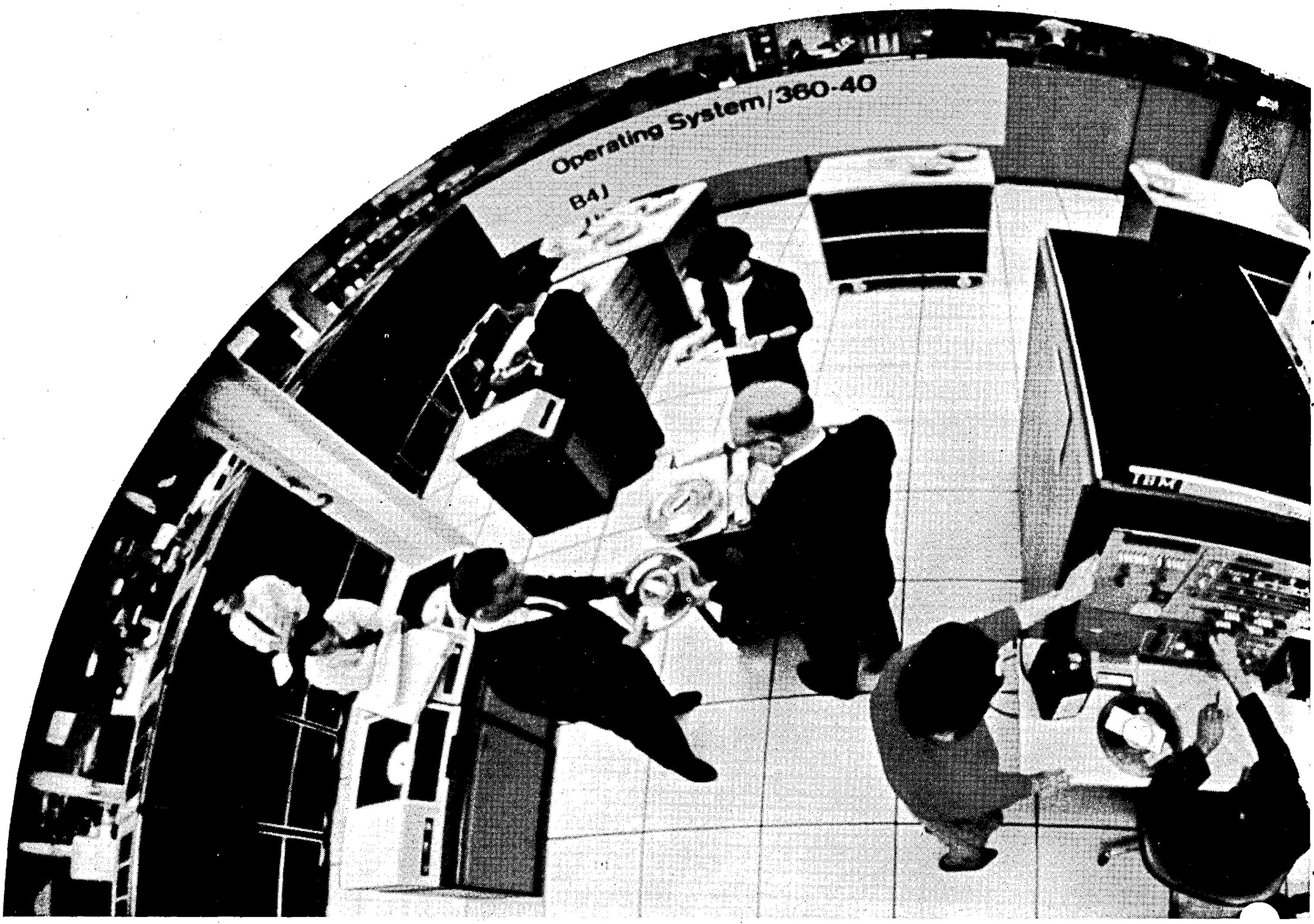
CIRCLE 184 ON READER CARD

GRAPHICS SYSTEM: Six-page brochure describes 816A computer graphics system, which in its basic configuration includes a 16-inch CRT masked to a 10.24 by 10.24 inch image area, vector generator, intensity compensation logic, electromagnetic deflection network, maintenance controls and a digital control unit. Standard options include character generator, line texture control unit, light pen, function switches and a computer graphics processor. SYSTEMS ENGINEERING LABORATORIES, Ft. Lauderdale, Fla. For copy:

CIRCLE 185 ON READER CARD

CDP DIRECTORY: 160-page directory lists names and company affiliations of over 7,000 holders of the Certificate in Data Processing and includes a geographically arranged cross index. Cost: $6 for CDP holders and DPMA members; $10 for all others. DPMA, 505 Busse Highway, Park Ridge, Ill. 60068.

COMPUTER CONTROL FOR CEMENT PLANTS: Four-page bulletin describes how computer control of cement mills with on-line digital process control systems can give better return on investment by minimizing raw material costs and increasing productivity and



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new literature

quality control. Brochure outlines applications to kiln control, raw materials blending, raw and finish grinding, and silo storage control. WESTINGHOUSE ELECTRIC CORP., Pittsburgh, Pa. For copy:

CIRCLE 186 ON READER CARD

FEDERAL EDP: 118-page report discusses the edp activities in seven government agencies chosen to be surveyed because they represent a fair cross-section of government edp activity in terms of size of operation, applications, machines and languages employed. In addition to detailed descriptions of each agency's activity, the report presents an analysis of answers to the questions posed and offers recommendations for handling existing problems. PB-175 701. Cost: $3; microfiche, $.65. CLEARINGHOUSE, U.S. DEPT. OF COMMERCE, Springfield, Va. 22151.

DATA SETS: Two technical bulletins describe data sets which use the narrow band technique for data transmission and are available in models transmitting at rates of 2400 and 4800 bps. MILGO ELECTRONIC CORP., Miami, Fla. For copy:

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GP COMPUTER: 50-page illustrated brochure describes medium-sized system, PDP-9, designed for problems in data acquisition, process or instrument control, computation or man/machine communication. Processor and memory specifications, I/O facilities, instructions, software, options and detailed applications information are included. DIGITAL EQUIPMENT CORP., Maynard, Mass. For copy:

CIRCLE 188 ON READER CARD

LINEAR INTEGRATED CIRCUITS: 352-page manual includes information on design, packaging, and application of linear integrated circuits. It is intended primarily as a guide for circuit and system designers in determining optimum design specifications with regard to integrated circuit capabilities and system requirements. Cost: $2. Commercial Engineering, RCA ELECTRONIC COMPONENTS AND DEVICES, Harrison, N.J. 07029.

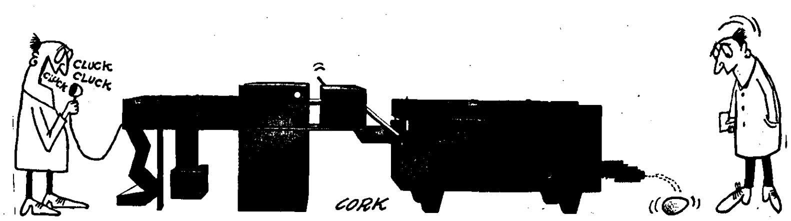
DATA ENTRY SYSTEMS: 12-page bulletin describes C-Dek computer data entry keyboard designed to enable untrained operators to make entries from areas such as the production floor, warehouse, and other locations where data usually requires transcription, keypunching, etc., before it becomes useful. The desk-top unit is built to customer specification from standard modules. Also included is how complete systems can be developed with the use of optional equipment. COLORADO INSTRUMENTS, Broomfield, Colo. For copy:

CIRCLE 189 ON READER CARD

PLOTTER: Six-page brochure describes incremental CRT plotter with matrix of up to 4096 x 4096 raster elements and plotting speed of 100K points/second. Maximum random repositioning time is 20 microseconds. Equipment is compatible with IBM 360 8- or 9-track tape unit off-line and all 360 models except /20 on-line. LINK GROUP, GENERAL PRECISION SYSTEMS, Sunnyvale, Calif. For copy:

CIRCLE 190 ON READER CARD

SIMULATION CONCEPTS: Part of a continuing series of reports on techniques of digital computer simulation, this 62-page report discusses basic concepts and the design and construction of simulation models, provides a rationale for simulation, and relates simulation as a technique to current problems in simulation technology. AD-658 429. Cost: $3; microfiche, $.65. CLEARINGHOUSE, U.S. DEPT. OF COMMERCE, Springfield, Va. 22151.



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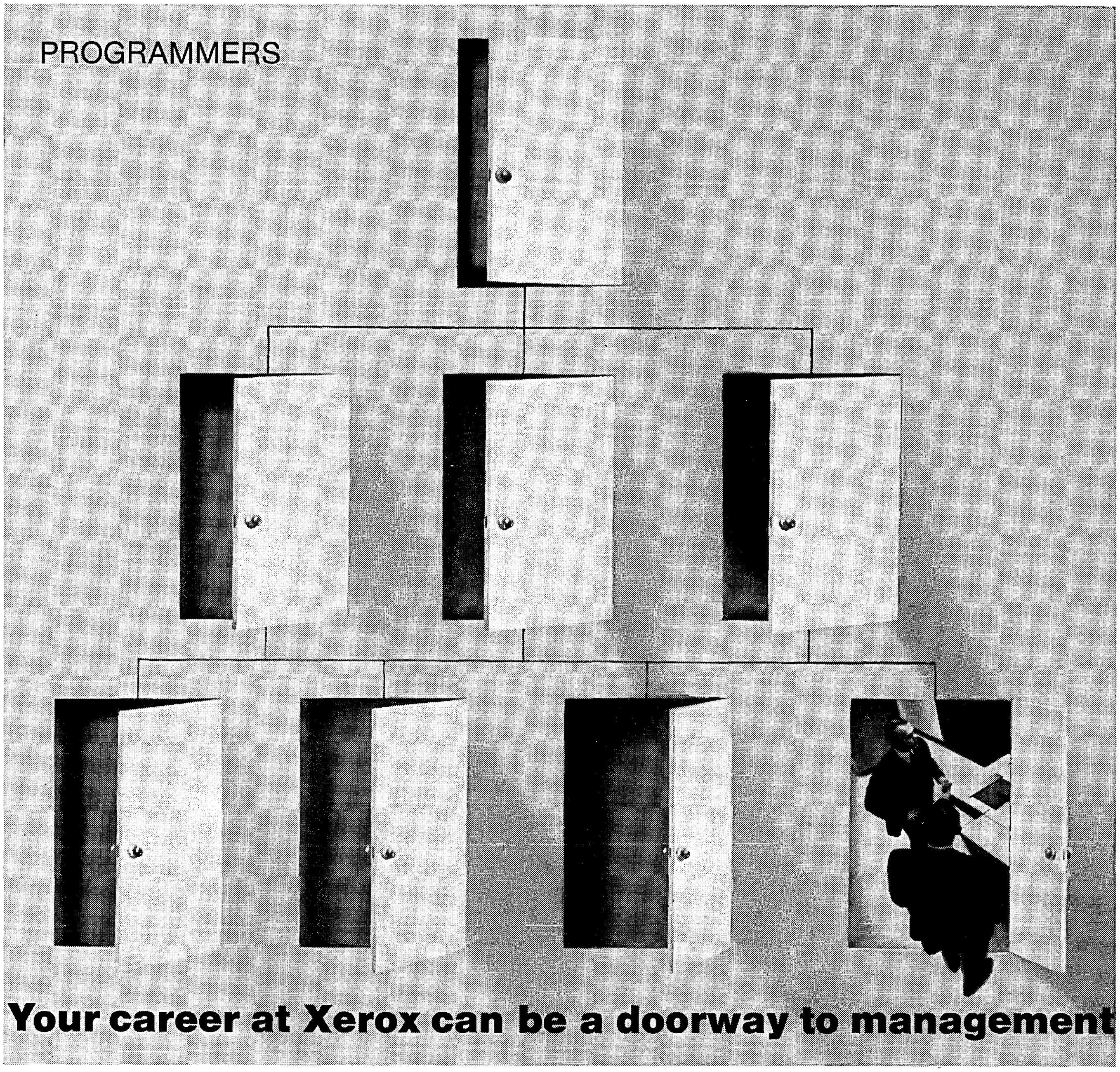

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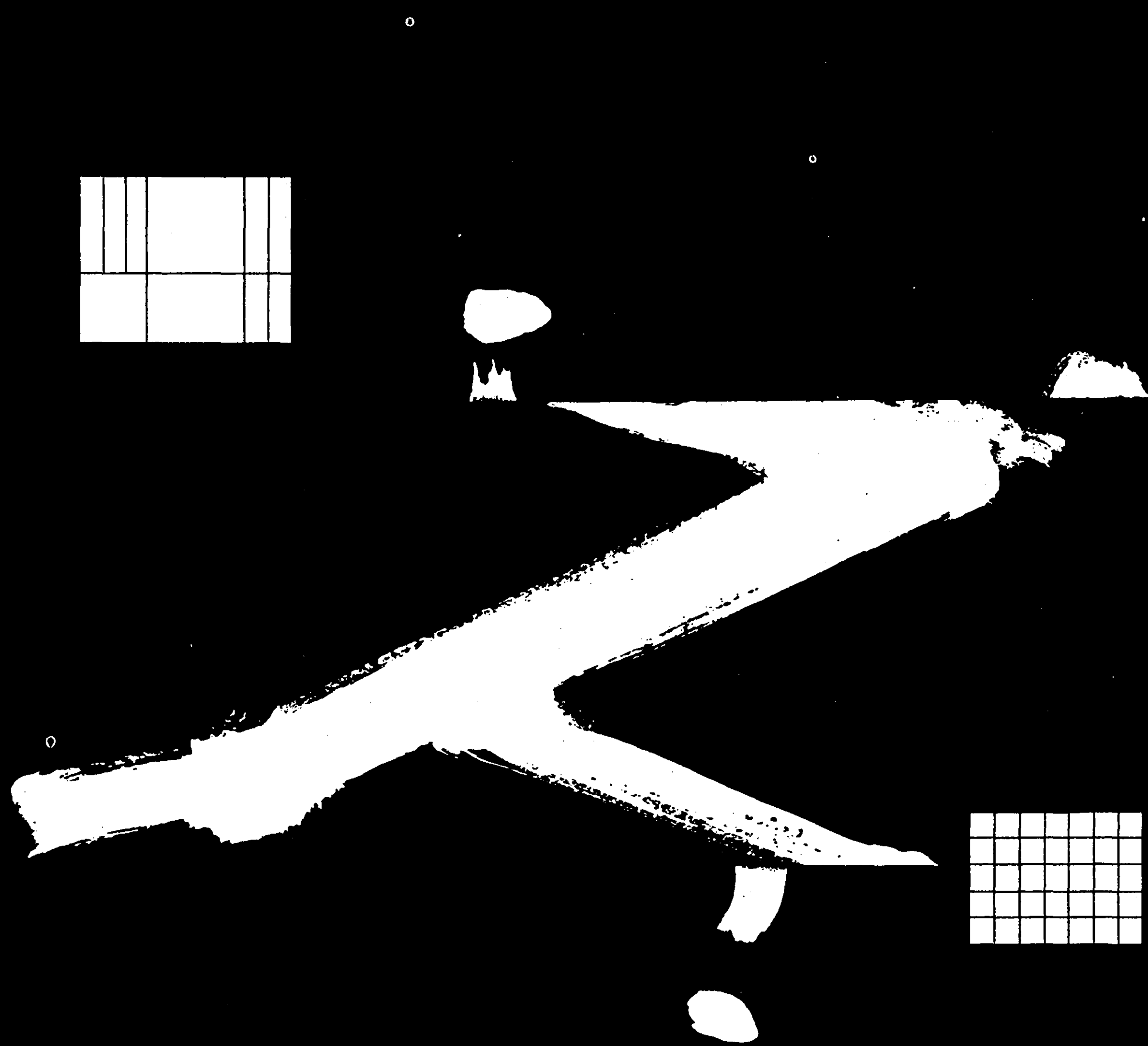

CIRCLE 305 ON READER CARD

books

The Computer in American Education*, edited by Don D. Bushnell and Dwight W. Allen, *John Wiley & Sons, New York, N.Y., 1967. Cloth, $6.95; paper, $3.95.

In November, 1965, the Association for Educational Data Systems and Stanford University, School of Education, co-sponsored a conference on the present and future role of computers in education, and this book includes the papers presented at that conference.

The subject matter of this collection covers a wide range of topics of interest to computer specialists and educators, and includes the uses of computers in the instructional process and in the administration of schools and colleges, the current practice and problems in gathering and analyzing data on education at local, state, and federal levels, secondary school and college courses in computer technology, and the relationship between school architecture and the instructional process. There is a fine foreword by I. A. Richards, in which he raises all the right issues concerning society's use of technology to achieve its goals. The book includes a 393-item bibliography (compiled late enough in the publication cycle to include *some* 1966 items), and a list of selected conferences on educational data processing.

The individual papers concern problems and future plans which are still important enough so that the book suffers minimally from the obsolescence to be expected in a report of a conference held in November, 1965.

Some of the articles deserve special comments.

Patrick Suppes describes the CAI work at Stanford, and categorizes CAI systems into three levels of interaction —drill-and-practice, tutorial, and dialogue—in order of increasing complexity. In discussing dialogue systems, Suppes lists, as one of the two central problems, the ability of the computer program to interpret freely constructed questions from the student. "The central intellectual problem at the moment is not that of writing information to give an answer, that is, of having in storage information that will give an answer to any question. Rather it is to recognize from the standpoint of the program precisely what question has been asked." (p. 19). The comment here is that this same problem arises in a slightly different form in tutorial systems, where the central intellectual problem is to recognize from the standpoint of the program precisely what answer has been given.

The paper by Robert H. Anderson summarizes the major changes occurring in American education today—from curriculum reform through innovation in school unit organization. He points out the glaring mismatch between our aspirations for universal high quality public education and the ". . . appropriate levels of financial support or . . . well-conceived policies to facilitate the achievement of truly excellent programs." (p. 27). He argues that ". . . one urgent need is greater flexibility in both the governing policies and the administrative and pedagogical machinery through which the goal is being pursued." (p. 27). Taking individualized instruction as an example of one such goal, he shows how its attainment involves such diverse factors as school building design and construction, and the teacher's ability to access and sequence instructional materials.

Judson T. Shaplin's contribution warns of pitfalls in the area of computer innovations: "The demands of research and development lead the computer innovators to neglect the need for relating their work to existing practices in the mainstream of American education, particularly recent reform efforts, and to ignore the implications of their work for personnel organization and training, all potent factors in future acceptance patterns." (p. 36f). He discusses the shortcomings of the present teacher-training apparatus, in terms of the funding and personnel demands of even modest current goals.

Dwight W. Allen describes many of the available computer programs for class and student scheduling, and urges more use of computers in simulation studies related to organizational and curricular changes. "No organizational change can ever replace the importance of what is taught, but what is taught can be greatly enhanced, limited, or eliminated by organizational demands on the people involved." (p. 58).

Don D. Bushnell presents a free-wheeling summary of some of the educational implications of selected computer applications, such as automated libraries, simulation and gaming, and community time-sharing systems.

Karl L. Zinn discusses the details of work in progress under the headings: author languages (including diagnostics and editing features), use of student responses (including the important unanticipated ones). Zinn's discussion is followed by an appendix listing significant details connected with 26 different CAI projects.

James K. Rocks presents an articulate statement of the challenges facing the Office of Education's National Center for Educational Statistics. In this very well-written article, the reader is exposed to the magnitude of the problems without being overwhelmed by the details, and is clearly shown the opportunities for improvement, even though the specification of the system to define the opportunities is still unclear.

The editors themselves contributed the last chapter, which lists the recommendations of the AEDS-Stanford Conference participants. Almost all of these recommendations can be applauded. The one exception is: "Criteria must be established for determining the disciplines or areas within disciplines in which either of the distinctive forms of computer mediation, computer-assisted or computer-augmented instruction, is appropriate and feasible." (p. 230). The danger here is that the too early setting of "criteria" can distract research from fruitful paths. One is reminded of the early days of programmed instruction, when many "experts" were advising that the new technique would never be useful for teaching more than rote learning materials. The subsequent successes in applying the principles of behavioral technology to skills such as interpersonal communications showed the folly in specifying in advance what any technique can and cannot be used for. In practice, such limits are generalizations from field experience, and the most appropriate role of associations and conferences is to collect, summarize and disseminate the results of such experience.

All-in-all, this is a good and valuable book. The computer specialist will find a wealth of information about the needs of education, and the challenging problems to be solved in meeting those needs. The educator will find incisive comments on the changes which must occur in current pedagogy and school administrative policy if computers are to be used effectively.

—James L. Rogers

***Exploring the Computer*, by Paul Allen III, Addison-Wesley, Palo Alto, Calif., $3.95, paperback.**

The purpose of this book is to teach you what the main parts of a computer are, how they work, and what

they do. There is a test in the back of the book to take *before* you read the book. Your score can tell you how much you know about computers.

The form in which this book is written is called programmed instruction. It presents material to you, and then asks questions about it. If you answer incorrectly, you can go back and read over the material again. When you finish the book, you take the same test (on different pages, of course), and compare your scores, to see how much you have learned. There is an appendix in the back of the book. If you wish to learn more about the computer than just the parts and how they work, then you should read it. There is also a glossary. If you run into any words you don't understand, then you can look them up there.

I would recommend this book for anyone who wants to learn generally about the computer—maybe just because it is an interesting subject—like I did.

SARAH ROLPH
Sixth Grade, White Point School
San Pedro, California

book briefs

(For further information on the books listed below, please write directly to the publishing company.)

***Digital Computer Programming*, by Peter A. Stark. The Macmillan Co., New York, N.Y. 1967. 525 pp. No price given.**

A heavy book written for the beginning programmer with very little emphasis on mathematical abilities, includes real problems, pre-solved on a computer. Instruction in machine, symbolic assembly and problem-oriented languages is included. Intended as a textbook, the book has several teaching aids, and is illustrated.

***The Programmer's ALGOL*, by Charles Lecht. McGraw-Hill Book Co., New York, N.Y. 251 pp. Price not given.**

Written as a reference book for the programmer, this volume describes ALGOL and gives detailed examples of its statements and declarations. Included is a long introduction by R. W. Bemer in which he gives the history of the language and commends it to independent thinkers.

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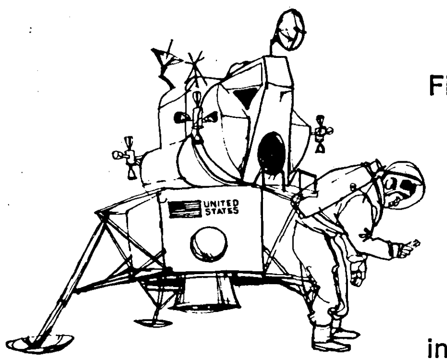

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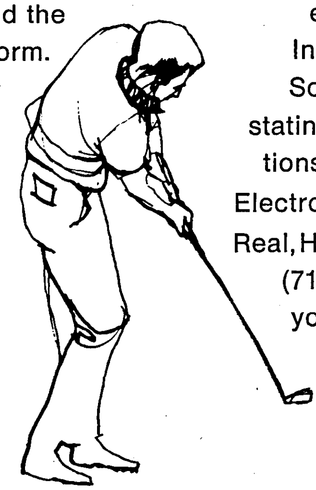

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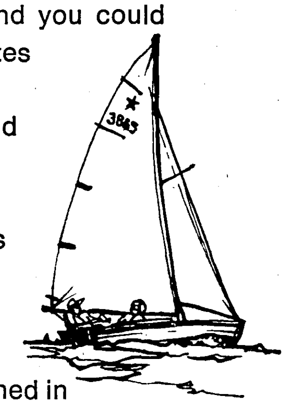

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Inc., runs a portrait of Leonardo da V. to ease the obscurity; others, such as Code, Inc., are a little less subtle. Think, Inc., is, according to its president, "a closely-held corporation. Just owned by us and IBM. — That's a joke," he added sadly. Pied Piper Programming is rumored to lure married mothers to cottage programming; has a disconnected phone. And if you think Alpha Omega Computer System rings of 1984, Apex Data Processing won't leave any doubts: under a picture of an imposing brontosaurus, it announces: "Adapt or Die." All are L.A.-area firms.

IBM SIGNS FIRST MODEL CONTRACT

IBM has signed the first model contract (July '67, p. 19) with California, will offer the state an almost verbatim standard contract, including liquidated damages and standards of performance including delivery dates for hardware and software. IBM's contract, which calls for software to show "substantial conformance to the contractor's specification," will undoubtedly be used in all states.

RUMORS AND RAW RANDOM DATA

CSC narrowly averted another top-level defection recently, talked top financial man Dave Layser into returning after he had joined Marshall Industries... R. Paul Niquette, an early SDS-er who is vp, plant operations for Standard Computer Corp., rejoins his old firm this month as assistant to president Max Palevsky...Other rumors about the 360/85, not announced January: 7090-compatible, 120 nsec cycle time, thin-film memory, and an operating system being done by Computer Sciences...Look for 3M, Computron, other tape makers to leap into the disc pack bizness...Joe Costello, who recently resigned as executive vp of Fabri-Tek, has formed Computer Peripherals Corp. in San Diego. Firm will make OEM peripherals...Atlantic Software Inc., Philadelphia, will market proprietary packages. The five-man firm, headed by Walter Brown and Richard Thatcher (ex-RCA and IBM), is gathering software from developers in any industry, plans a technical and marketing staff of 25-50 by year-end... Transamerica Corp., after giving up acquisition of MAI, has set up its own leasing firm headed by Jim Ritter, who has been controller of IBM's edp division. They have $100 million to spend--on System/360's...In the next month or two, the National Association of Securities Dealers should be asking for bids from vendors on a massive system to keep track of quotations for the Over-the-Counter market, plus corporate and municipal bonds--just about everything not now listed on an exchange. Some 3000 terminals will be needed and the whole system will be well up in the multimegabuck range...There are rumors of fading interest in time-sharing by the biggest companies. Apparently what they really wanted was fast response time, which can be had with remote batch. The limited need for conversational jobs can be handled by the outside commercial time-sharers...Honeywell's Computer Control Div. announces the DDP-324 this month. The 24-bitter features twin cpu's of up to 24K core each, plus 8K shared. Cost of an 8K x 8K x 8K system: $163K. They've sold three already to Conductron-Missouri for flight simulation.

Programmers, if you're ready to give more to the present, you're sure of a solid future at RCA.

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RCA Electronic Data Processing is in a period of unprecedented growth as a direct result of the success of the Spectra 70 product line, a true third generation computer system. Here EDP professionals can find unmatched opportunities for career development.

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RCA Graphic Systems Division is busy adding the speed of electronics to typesetting.

At this division we've combined computers with new electronic typesetters that can set the text for an entire newspaper page in less than two minutes. Together, they do the complete job: store and recall manuscripts, size and lay out pages, and set the type.

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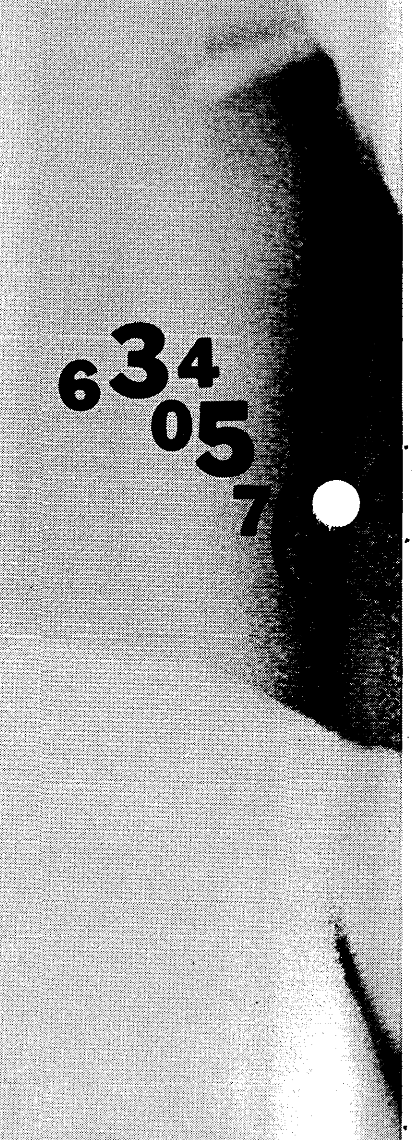
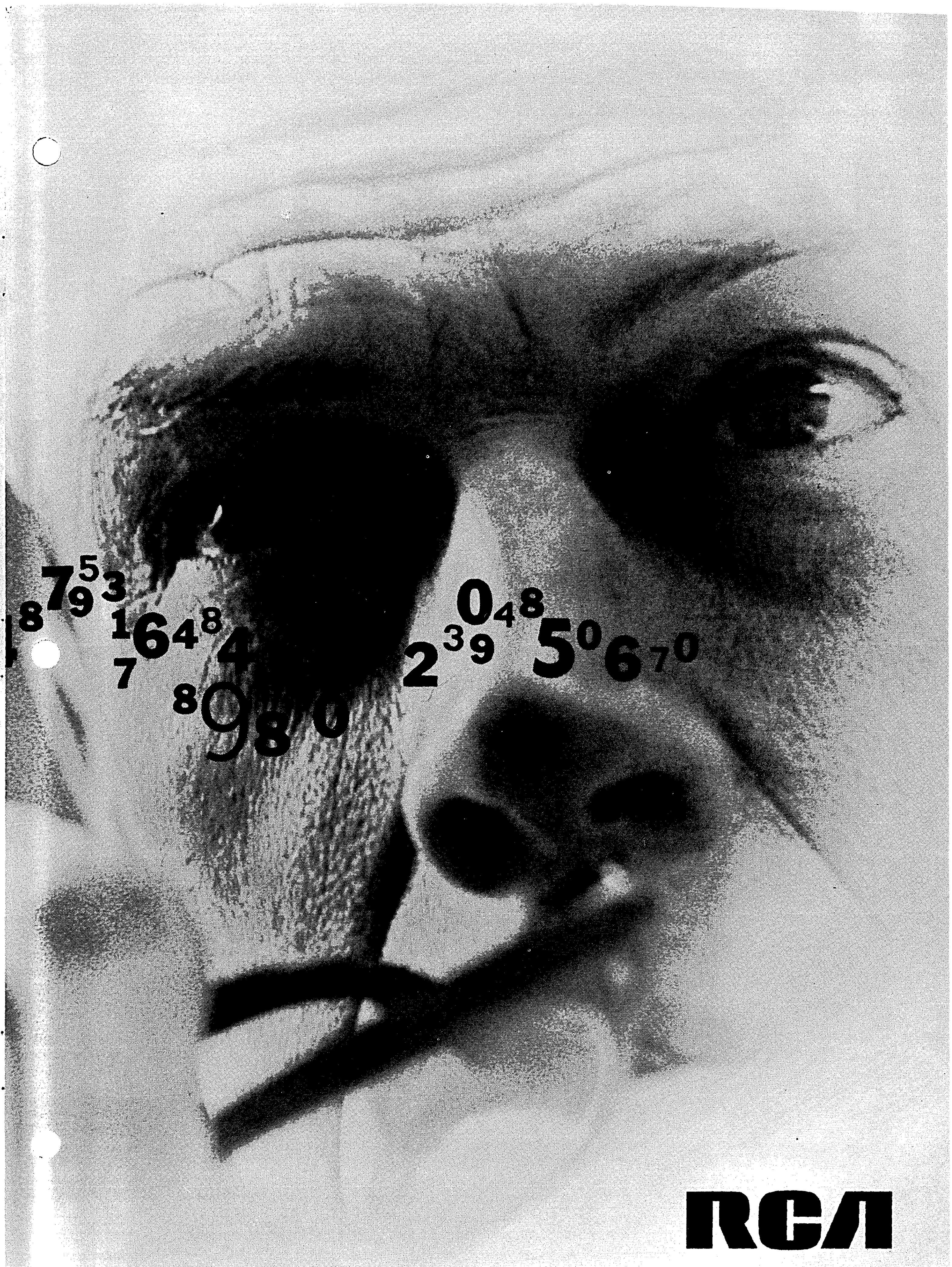
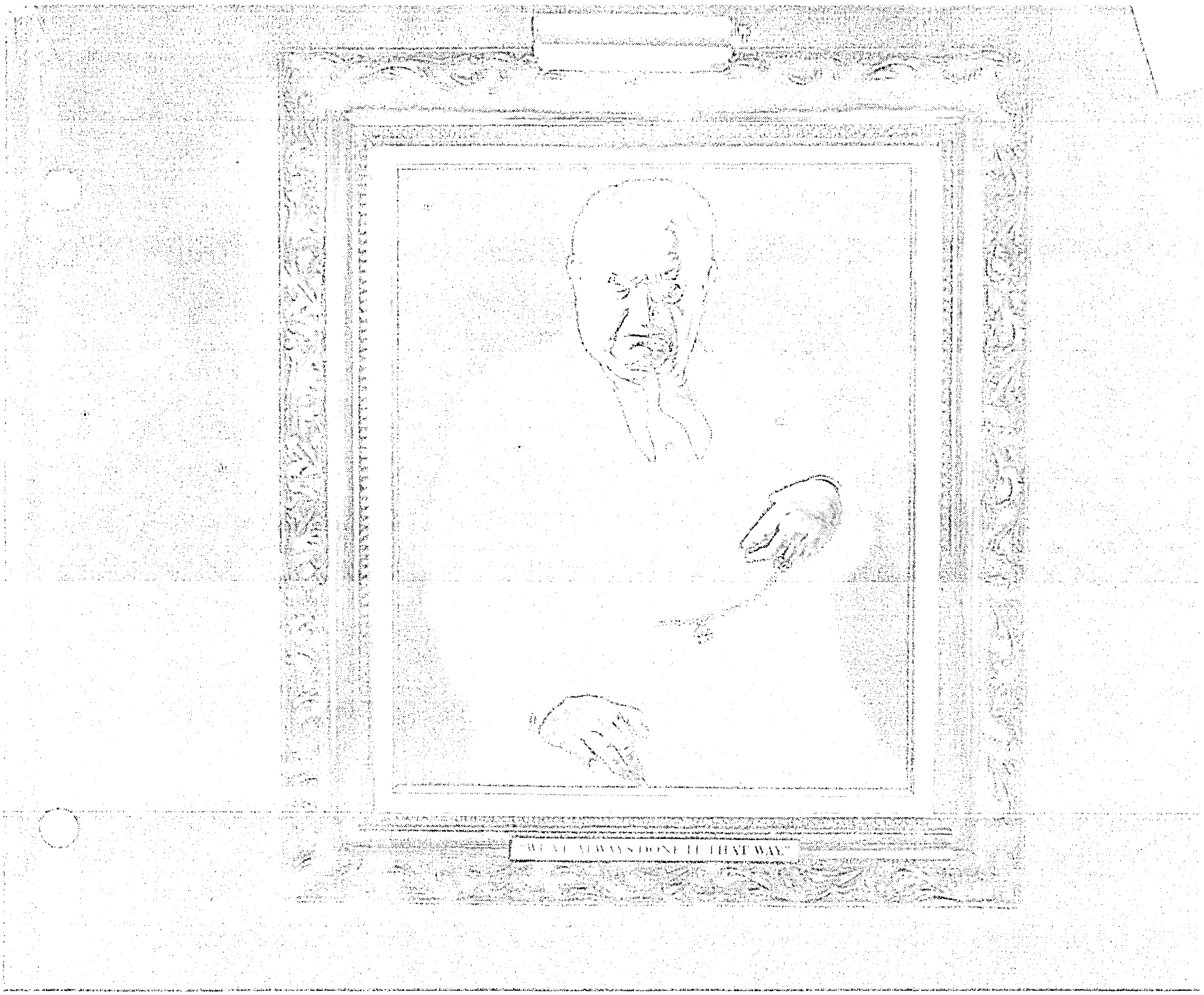
Openings are at all levels for those with a minimum of 2 years programming experience. Location is Princeton, New Jersey.

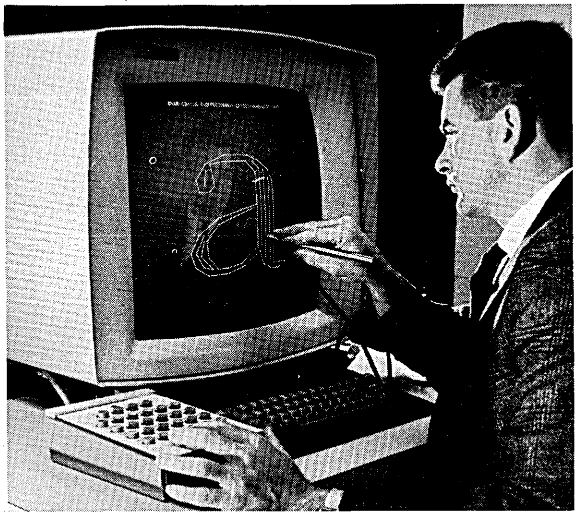
To find out more about these major areas of programming at RCA, write to: Mr. T. Beckett, RCA, Dept. SW-2, Bldg. 2-2, Camden, New Jersey 08102. We are an equal opportunity employer.

CIRCLE 318 ON READER CARD




RCA





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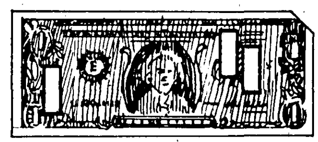

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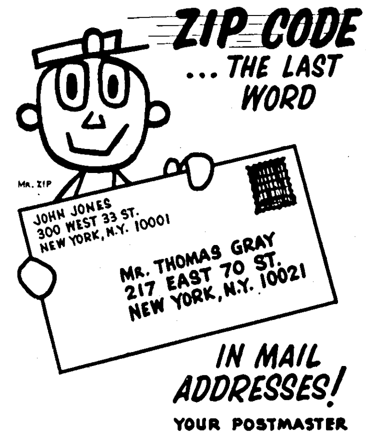

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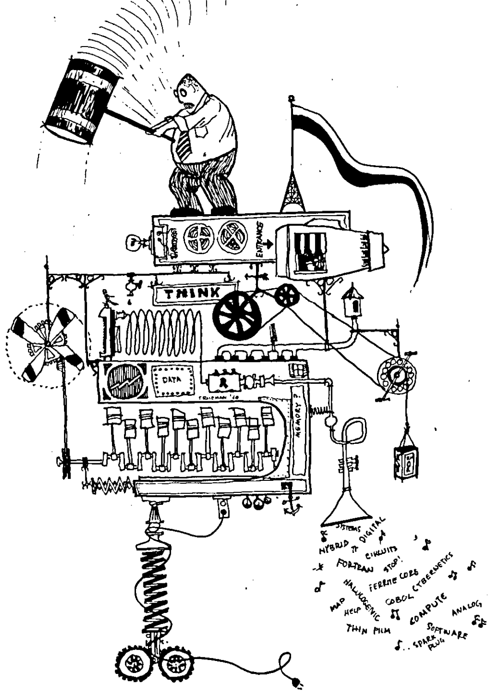

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people

■ Alexander Grove, formerly director of standards information for USASI, is now director of standards of the data processing group for BEMA. He replaces Paul Goodstat, who has joined Price Waterhouse as senior consultant.

■ Dr. Jack Moshman, formerly managing director-management sciences for EBS Management Consultants and vp and gm of the applied research and management sciences division of CEIR, has joined Leasco Systems and Research Corp., Great Neck, N.Y., as vice president.

■ Nova L. Smith is president of Nova Computer Systems Co., new San Diego software firm. Prior to forming the company, Smith had been San Diego resident manager for Univac.

■ Kenneth P. Clancy has been appointed a vp of Keystone Computer Associates, Willow Grove, Pa., subsidiary of University Computing Co. He will also continue to direct the company's systems programming department.

■ Werner E. Mangold, of Univac's international division, has been elected chairman of the numerical control language committee of the International Standards Organization.

■ Beckman Instruments has appointed Joseph G. Neuland as manager of its newly formed Medical Systems Operations unit, whose products will be sold and serviced by the company's Spinco Div., Palo Alto, Calif.

■ Edward E. Strickland has been elected board chairman of National Computer Systems, Minneapolis-based electronics company specializing in optical scanning techniques for computer input. He had been with Control Data, most recently as vp for corporate development.

■ Dr. J. C. R. Licklider has rejoined the faculty of Mass. Institute of Technology and will be associated with research at Project MAC. Since 1964 he had been director of research at IBM.

■ Kenneth W. Kolence and David Katch, both formerly with Control Data, have formed a software firm, Boole & Babbage Inc., Palo Alto, Cailif.

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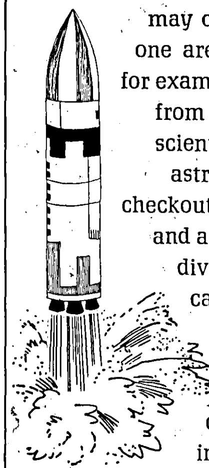

may choose to specialize in one area (reentry problems, for example) or they can move from one area to another—scientific areas as varied as astrodynamics, automatic checkout and graphic systems; and administrative areas as diverse as business applications and government information systems. Lockheed offers the widest range of computer assignments in the country today so programmers will always find a field to stimulate their imaginations.

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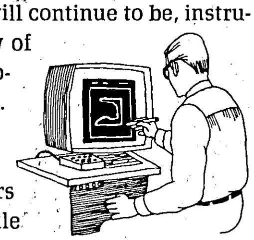

to the Program Evaluation and Review Technique (PERT) developed by Lockheed programmers in conjunction with the Navy. Now Lockheed programmers are developing configuration data management systems for on-line, real-time computer analysis of manufacturing, financial, and personnel related data.

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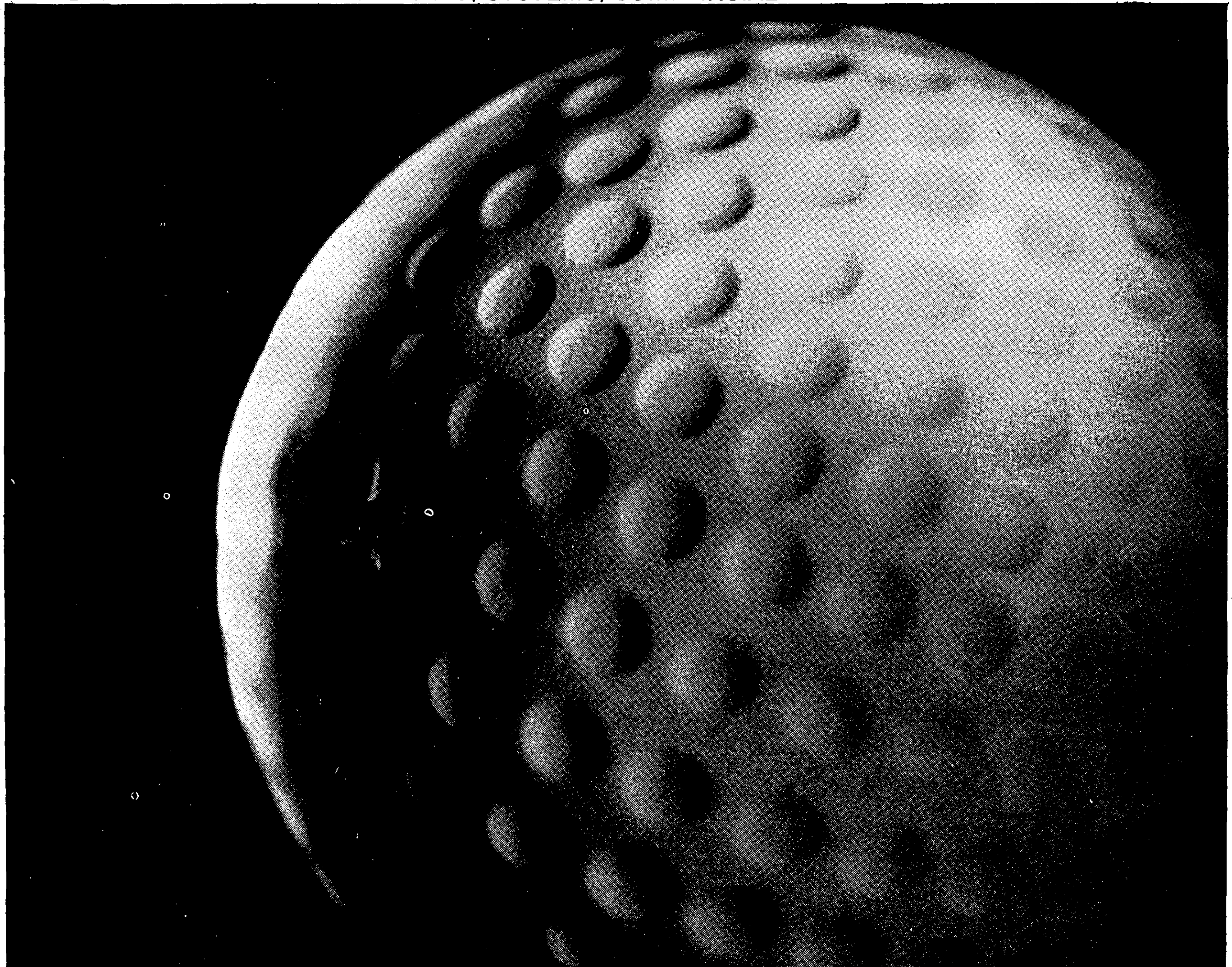

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THE NEED FOR IMPRECISION

The growing interest in decision tables as a tool for programming business dp applications is a symptom of disenchantment with the conventional techniques—by which I mean logic flowcharts and procedural languages. I'm all on the side of the disenchanted; these conventional techniques are hardly ever the right ones to use in business dp; mostly they're used because no alternative is available, and because programmers are pretty conservative people anyway. But it seems to me that we are overlooking one of the most important disadvantages of procedural programming, and that the benefits we could gain by eliminating it are in danger of being missed.

The usual indictment runs like this. Writing procedural programs is difficult, and unreasonably so. Given a specification, the programmer is required to devise a logical structure which is related to it in a particular, non-obvious way; the complexity of this relation accounts for most of the difficulties. Devising the structure is itself an arduous activity for all but the simplest specifications; it is easy to make mistakes and, in repairing them, to cause fresh errors. The procedure defined by the logical structure will usually have several properties which the programmer did not intend; when conditions arise which he has not foreseen, these additional properties are likely to cause trouble. Also, it is impossible to check the operation of the procedure on a particular set of input data except by simulating the program (or actually running it); there is no analytical method of debugging.

So far, so good; the case for finding a better, nonprocedural technique is well-founded. But the indictment does not go far enough: the worst crime is committed in our attempts to mitigate the difficulties above. Because programming is so difficult, we have been driven to adopt a rigorous methodology. We decree that specifications should be complete and precise; that they should be "frozen" while the program is being developed; they should be self-consistent and exhaustive, and without redundancies. We make these rules because without them we may not be able to write programs at all. But they are inherently bad rules, imposing constraints that are irksome and often unacceptable. As soon as possible, we should kick over the traces and be free.

Unfortunately the prisoner doesn't always notice when the door of his cell is opened; and too often he prefers the security of his prison to the more demanding air of freedom. In a typical article on decision table techniques we read: "Tables force the analyst to make a complete and accurate statement of the problem logic . . . tables provide for better optimization, since computer programs can check tables for completeness, redundancy and contradictions." This seems to me to be very wrong-headed. We should be positively looking for and developing programming methods that do allow inconsistency, redundancy, ambiguity and incompleteness; we should recognize that these seem to be vices only because the error-prone techniques of procedural programming make them so.

But allowing that we need no longer call them vices doesn't in itself make them virtues. It would be ludicrous to complicate our dp systems by wantonly introducing confusion and inconsistency into situations where none existed before; and we must recognize that some problems can only be solved by extreme rigor and precision. My theme is concerned with those situations where confusion and inconsistency are inherent elements of the problem and where we cannot hope to write successful programs unless we are able to deal properly with these factors.

Consider, first, those cases where no specification can be agreed for the program to be written; the most obvious instance is machine translation of natural human languages. We know what we are trying to achieve, but we cannot pin it down in any but the broadest of specifications; arguably, many of the most sophisticated attempts to devise systems for machine translation have failed precisely because they have relied on a detailed specification (usually of some lexical or parsing algorithm). When the specification proves faulty, the techniques used allow no substantial modification without complete redesign. Programming in this fashion is like playing golf with crazy rules—rules which demand that if you don't hole in one you must go back and drive from the tee again; to play like this is to miss the crucial point that makes golf possible: you get to the hole by a convergent series of strokes, and it doesn't

the forum

matter if you can't see the hole from the tee.

Consider, next, the specification that is incomplete. In a complex payroll application, for example, the rules determining what each employee is to be paid will be based on legal requirements, on piecemeal agreements with several labor unions, on practical difficulties, such as widely dispersed paying points, and so on. When the systems analyst tries to formulate the programming specifications he discovers that these rules are not easily reduced to an ordered scheme; in particular, his attempts to do so may reveal areas in which the rules are simply not defined at all. He may ask "how is gross pay calculated for an employee on code 17 who is working on a scheduled rest-day when that day happens also to be a public holiday, and the total number of hours worked is less than a normal working day?" And there may be no answer to this question because the case has never been considered before. The analyst has to put the question only because he needs an artificially complete and tidy specification.

Then consider the inconsistent specification. It is common for the rules of a manual data processing system to develop by allowing exceptions to the general rules, then exceptions to the exceptions, and so on. The systems analyst cannot represent this situation correctly by distilling out of it a firm and consistent specification; he needs to be able to describe the system naturally, in its own terms.

Too often in the past computer systems have been designed in defiance of their users' needs and wishes. It is too easy to castigate the user who isn't sure what he wants, who can't define his needs precisely, who seems to be pursuing incompatible objectives. Of course he is often just being muddleheaded about a simple problem, or too lazy to think it out properly; of course he is often pursuing a confused policy that badly needs to be rationalized. But often he is recognizing that the complexity of his task needs a more subtle and flexible treatment than the analyst and programmer seem able to provide. One of our most important aims in moving away from procedural techniques should be to equip ourselves to meet this need.

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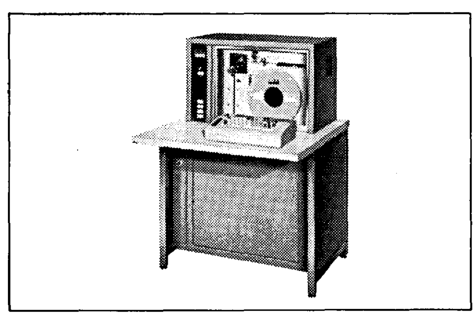

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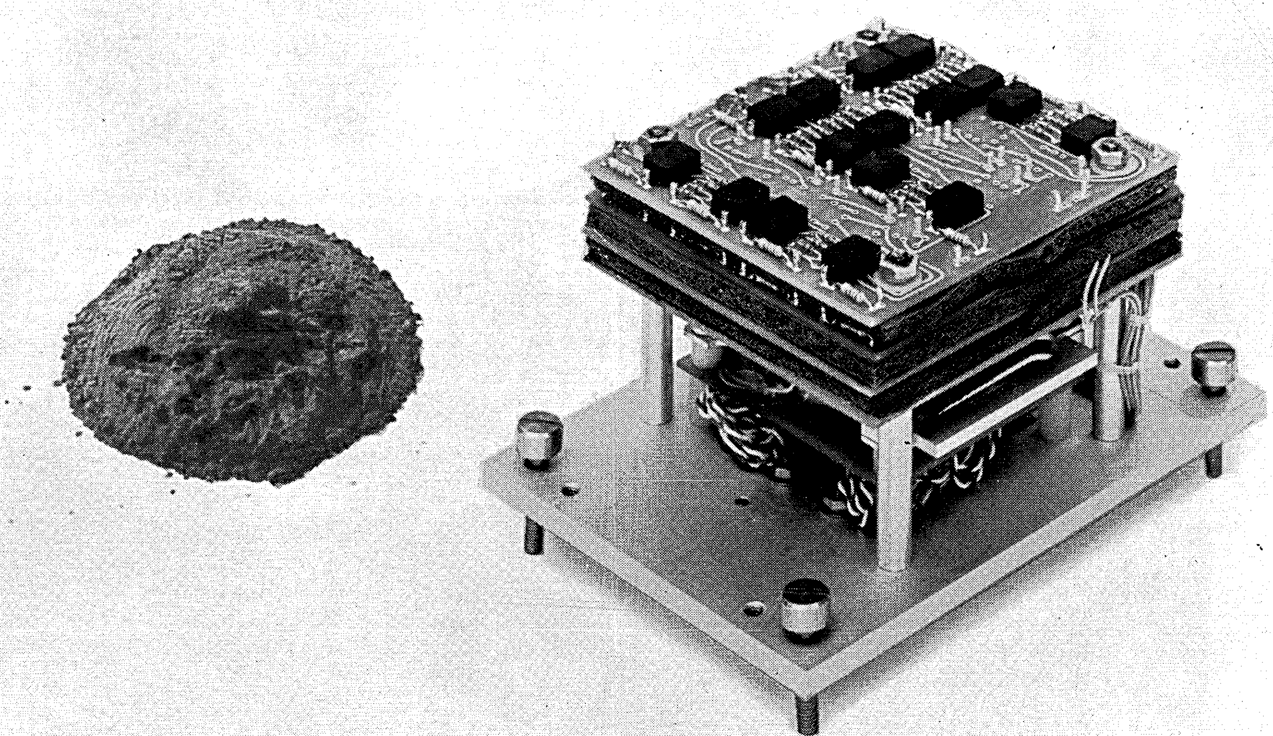

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