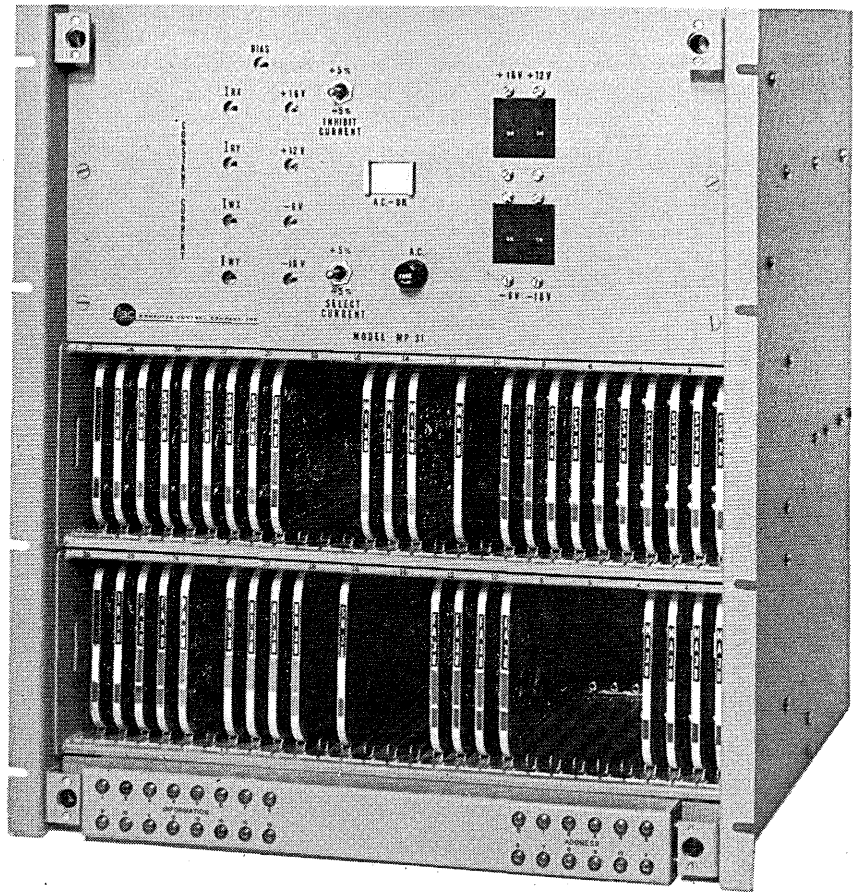
Edmund F Klein, Chf Sys Engr
Natl Cash Register
Electronics Div
1401 E El Segundo
Hawthorne Calif 13-15

BURKS GOLDSTINE

VON NEUMANN — *the conception*

QUALITY GOES DEEP



CORE MEMORIES
with unique logic flexibility

Coincident current 3C Core Memories are all solid state, have true logic flexibility. They mate well in a system because they are tailored from an extensive line of standard 3C modules. Operating margins are broad. Model pictured stores up to 130,000 bits, with word lengths of 6 to 40 bits. Read-write cycles are 5 to 10 μsecs. You select features. Example: 3½ to 6 μsec split-cycle operation. Another: power supply test switch marginal checking. No extra charge—for these features. Memory self-checking is extra, but not much. Other features, other capacities available. Experience? Three and one-half years. Quality? It goes deep.

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CIRCLE 4 ON READER CARD

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BASIC FACTS: THE PHILCO 212 HAS 960KC TAPE-ABILITY

- **Unrestricted 4-Way Multiplexing**
- **240KC Instantaneous Transfer Rate**

Philco's new High-Performance Magnetic Tape System, like other Philco 212 System components, makes the 212 a well balanced EDP system. The Philco combination of high-speed tapes (Instantaneous Transfer Rate: 240,000 alphanumeric characters a second; Effective Rate: up to 220KC with variable-sized records), and Philco's unrestricted 4-Way Multiplexing (any 4 of up to 32 tapes, each reading or writing in any mixed choice), provides a new standard of computing system efficiency and balance. This combination also permits a tape-ability of 960KC. Result: more throughput per dollar.

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The Philco 212 System operates with either the standard high-speed 90KC or new high-performance 240KC tape systems. To change from 90KC to 240KC tapes requires no reprogramming. Philco High-Performance Tape Systems will be available in 1963.

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CIRCLE 5 ON READER CARD

DATAMATION 62

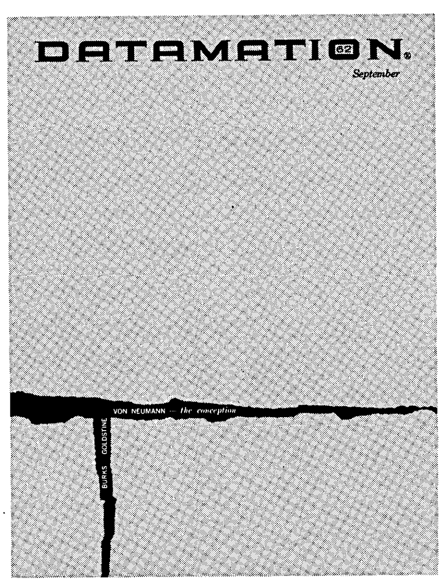
the automatic handling of information

volume 8, number 9

Feature Articles

Departments

THIS ISSUE—40,825 COPIES



Cover

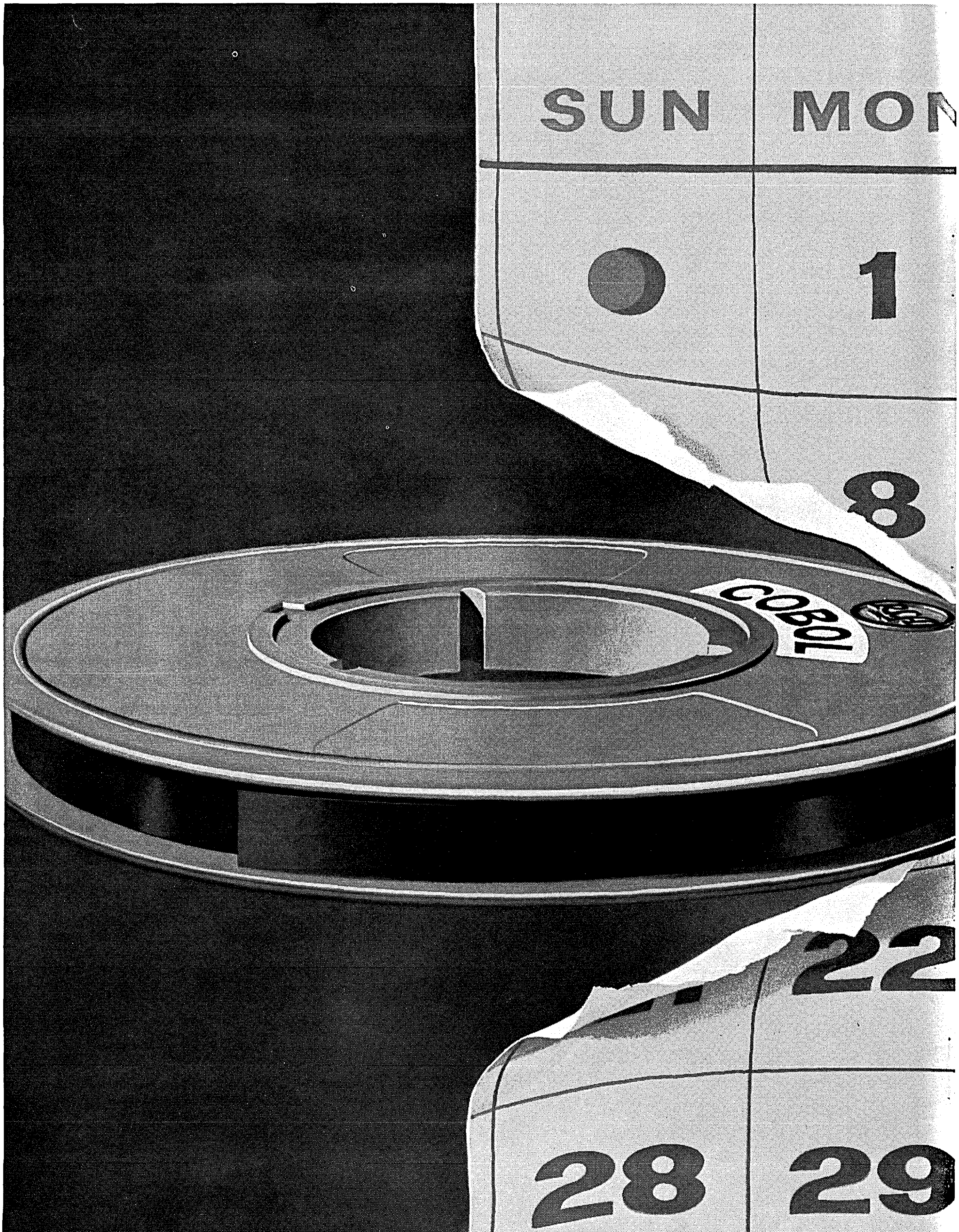
The conception of stored programming was first reported by Burks, Goldstine and von Neumann in a paper prepared in June, 1946. Their paper is published for the first time in this issue of DATAMATION. The nature of this work was and in every respect, remains, a "breakthrough" in both the literal and graphic sense of the word, interpreted for this month's cover by Art Director Cleve Boutell.

Circulation audited by Business Publications Audit — BPA

Member, National Business Publications — NBP

DATAMATION is published monthly on or about the tenth day of every month by F. D. Thompson Publications, Inc., Frank D. Thompson, president. Executive Circulation and Advertising offices, 141 East 44th St., New York 17, N.Y. (MUrray Hill 7-5180). Editorial offices, 10373 West Pico Blvd., Los Angeles 64, Calif. (BRadshaw 2-0817). Published at Chicago, Ill. Accepted as controlled circulation at Columbus, O. Form 3579 to be sent to F. D. Thompson Publications, Inc., 201 N. Wells St., Chicago 6, Ill.

Printed by Beslow Associates, Inc.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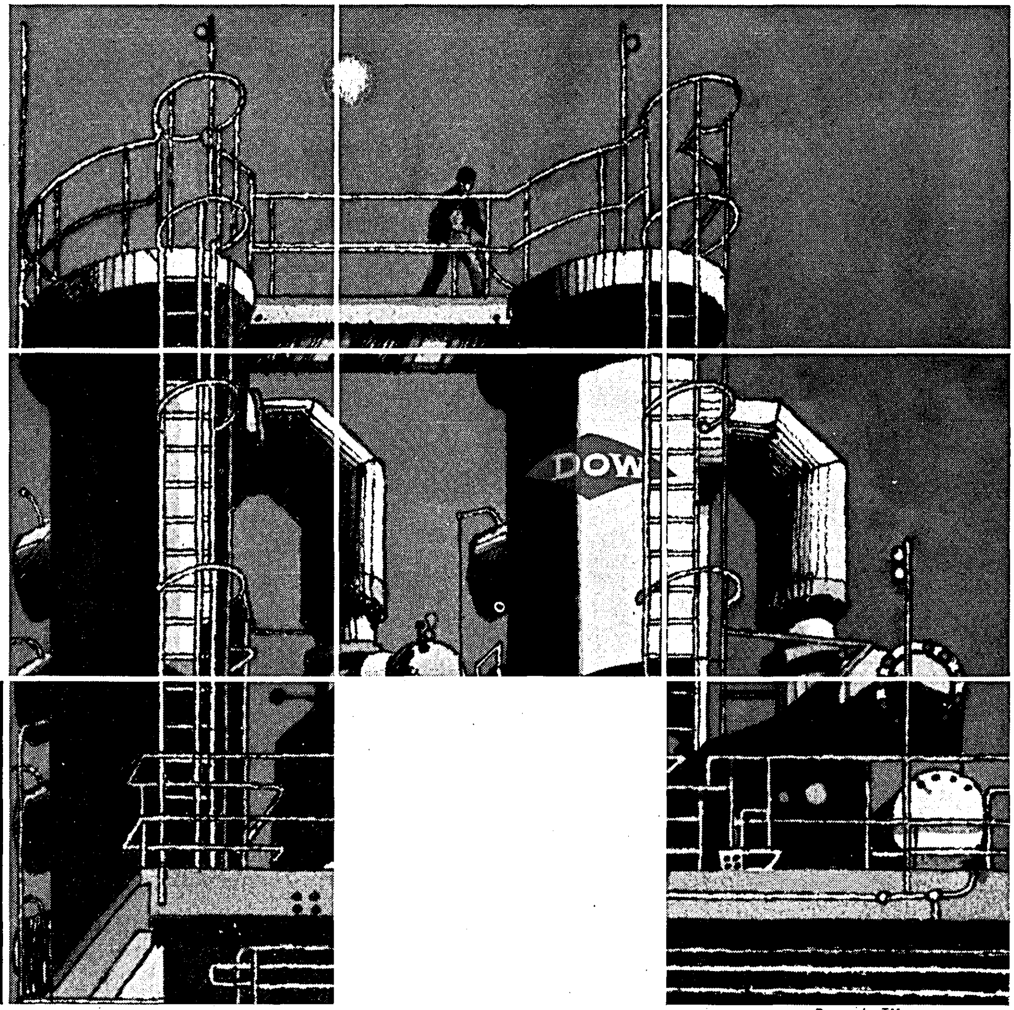
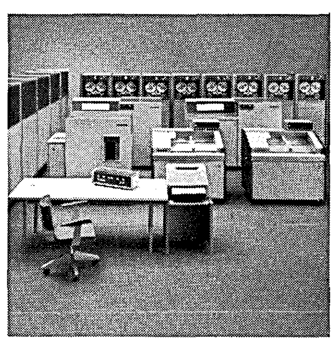
why Dow Chemical ordered a Burroughs B 5000



Burroughs-TM

Dow, the nation's fourth largest chemical company, is now using an intermediate-scale Burroughs computer system in its Computations Research Laboratory. With it, Dow scientists are solving a wide variety of scientific and engineering problems. ■ To help them stay ahead in their research efforts, a large-scale system will soon be needed. Dow scientists will use the new large-scale, medium-priced Burroughs B 5000 system.

The B 5000 accepts the modern, simplified programing languages, Algol and Cobol, directly. It was specifically designed for this purpose to sharply reduce programing time and expense. And it translates these quickly written programs into B 5000 language instantaneously. It can run several independent programs simultaneously. ■ For more information, write us at Detroit 32, Michigan.



Burroughs B 5000 Electronic Computer System

Burroughs Corporation

so many data processing problems end with Burroughs

CIRCLE 8 ON READER CARD

important DATES

- The 3rd annual Symposium on Switching Circuit Theory and Logical Design will be held Oct. 7-12 in Chicago, Ill. under the sponsorship of the AIEE Computing Devices Committee.
- The 15th annual International Systems meeting is scheduled for Oct. 29-31 at the Hotels Statler Hilton and Sheraton Plaza, Boston, Mass.
- A Conference on Spaceborne Computer Engineering will be held Oct. 30-31 at the Disneyland Hotel, Anaheim, California.
- The Operations Research Society of America will meet from Nov. 8-10 at the Sheraton Hotel, Philadelphia, Penna.
- The AIEE Winter General Meeting, Jan. 27-Feb. 1, 1963, will feature special sessions on Artificial Intelligence. The meeting is scheduled for New York City.
- Armour Research Foundation is sponsoring the 1962 Computer Applications Symposium, to be held Oct. 24-25 at the Morrison Hotel, Chicago.
- The 1962 Fall Joint Computer Conference will be held on Dec. 4, 5 and 6th at the Sheraton Hotel, Philadelphia, Pennsylvania.
- The AIEE/IRE International Conference on Nonlinear Magnetics will be held at the Shoreham Hotel, Washington, D.C., April 17-19, 1963.
- The 1963 Spring Joint Computer Conference will be held May 21, 22 and 23rd, 1963, at the Cobo Hall, Detroit, Michigan.
- The 1963 ACM National Conference will be held Aug. 28, 29, and 30th in Denver, Colorado.
- The 1963 Fall Joint Computer Conference will be held in the Las Vegas, Nev., Convention Center, Nov. 12-14, 1963.
- The 1964 ACM National Conference will be held in Philadelphia, Penna., Aug. 25-28, 1964.
- The IFIP Congress 65 is scheduled for New York City in May, 1965. It is the first International Congress scheduled for the United States.

letters

glossary progress?

Sir:

The glossary situation is really not as bad as you painted it in the June issue. In the first place, the IFIP glossary is progressing well and should be in draft form by the end of this year. The BSI glossary, which was used as a starting point by IFIP, has been published as a British standard. With respect to U. S. work, the Business Equipment Manufacturers Association (BEMA) (sponsor of X3.5) distributes two interim glossaries upon request. One of these is the IBM glossary and the other is a glossary by Martin Weik. IBM published 10,000 copies and distributes them freely, so the emergency is not as critical as you indicate. In this glossary you will find the word "computer" unshamefully defined.

Many people do not understand the value of the IFIP glossary work. National products, such as the BSI glossary or any U. S. glossary, could not be accepted as an international standard, because they have not considered the variations in usage and concepts. IFIP work seeks to resolve these difficulties at the concept stage. Furthermore, one could not take a national glossary and simply modify it for differing usage, because the inter-relation of definitions is so crucial and exists in so many different forms that only an integral group of international composition can hope to be consistent. I've seen many an instance where the German or French member asked for a revision to the English definition because he knew it would not translate well.

R. W. Bemer
Director,
Systems Programming,
Remington Rand UNIVAC,
New York City

(*Editor's Note:* DATAMATION fully appreciates the methodical efforts and problems of the international and U. S. glossary committees. However, it is also our feeling that an interim glossary should be made available earlier than current expectations indicate in order to rectify some current and major sins in professional communication.

We have asked BEMA for a copy of the Martin Weik glossary and it is *not* available. IBM's glossary however, is very definitely available; in fact, it commits many of the aforementioned sins. For example, we referred to page III-13 on which a definition of "computer" appears as "A device capable of accepting, processing and reporting information." While the breadth of this definition is commendable, it may be applied with equal accuracy to a cash register.)

voice for intuition

Sir:

I hereby nominate Col. Jordan to join Commander Sheppard, Col. Glenn, and the X-15 pilots in receiving presidential recognition for activities in the far out reaches of space. Obviously the good Col. is another of those gentlemen caught up by and impressed with his own verbiage.

I cannot help but think that here in the Colonel we have an apprentice of H. R. J. Grosch. Younger, to be sure, but possessing the same inherent capability to cloak the real problem with impressive sounding exposition. For example, would the Colonel really have us believe that the number of assemblies is worth a maximum of 10 points whereas the complexity of the program is only worth something less than five? Under such a system as the Colonel proposes all thinking programmers will reduce given programs to say five programs thus assuring them of a beautiful profile.

Also the Colonel states "the rapidity with which a program is written is a facet in optimizing." Really, it is quite apparent that the Colonel does not have a working knowledge of programmers. This is quite understandable as it is a standard reflex action for data processing managers who have no feeling of programmer capability to ivorytowerize the problem in a paper such as Jordan's. A competent manager knows intuitively which are his best programmers and, in a minute could array all his programmers in order of merit. I am certain if we were to select the top 10 automatic programming specialists and compiler language experts from each of the manufacturers and evaluate them using Col. Jordan's system we would set back the software program development five years.

Perhaps the Colonel phrased it very well himself when he said "the success or failure of profiling programmers is not in the writing but in the doing."

Take heed Colonel.

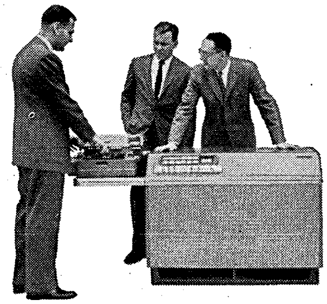
JOSEPH MORGAN,
Manager
Pettes Computer Services
Minneapolis, Minn.

($$=$)

YOU CAN GET ANOTHER COMPUTER TO DO WHAT THE RPC-4000 DOES—FOR ONLY TWICE AS MUCH MONEY

These performance specifications need no elaboration. □ 8008 word, 72,000 digit memory with special fast access features. Computer speeds of up to 230,000 operations per minute. 30,000 characters per minute input — 18,000 characters per minute output. □ Which adds up to the largest memory, greatest problem-solving capacity and flexibility in the low- or medium-priced field. It's actually a desk-size transistorized computer with room-size computer capacity. □ Performance is formidable—operation isn't. Even non-technical personnel can program and operate the RPC-4000 at optimum levels. You can easily master it yourself in one day—and free yourself forever from dependence on a computer specialist. (More than 3000 students were taught programming in less than one day with PINT, an interpretive routine developed especially for the RPC-4000 by Purdue University. A film of this training will be shown on request). The RPC-4000 plugs into conventional outlet, requires no expensive installation. □ All this plus a Library of Programs for the RPC-4000. It is the most extensive in this computer class — and may well include the program you need. Programs for Fortran and other computer languages also ready to go, as well as PERT programs. Here alone are possible

major savings. □ Only one other desk-size computer gives so much value per dollar. And that's the LGP-30 — little brother (or sister) to the RPC-4000 and the most powerful, biggest memory, complete computer system in its class, at $1100 per month rental. For more information about rental or purchase, write Commercial Computer Division.



GENERAL PRECISION

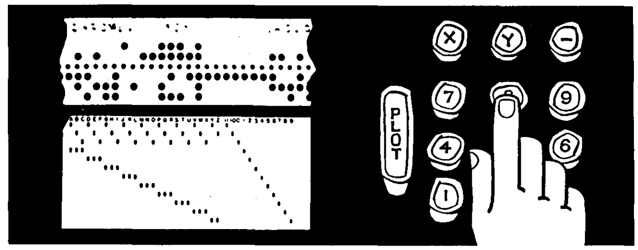
COMMERCIAL COMPUTER DIVISION/GENERAL PRECISION, INC./BURBANK, CALIFORNIA

CIRCLE 12 ON READER CARD

PLOT FOR ECONOMY

SAVE TIME... SAVE MONEY...

CONVERT THIS



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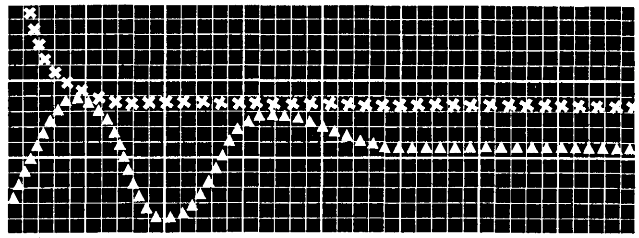

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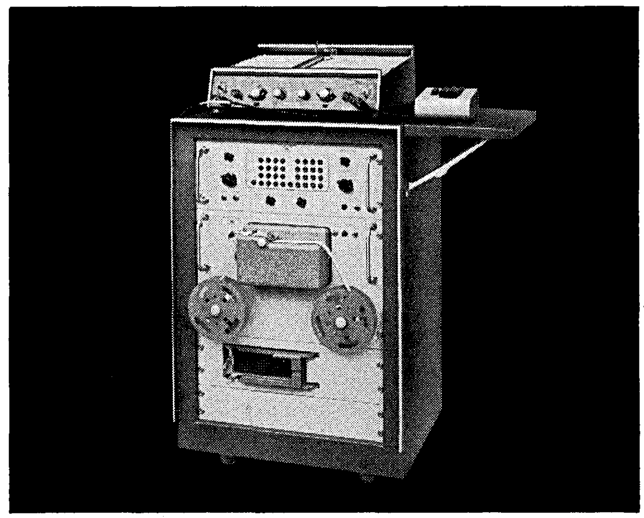
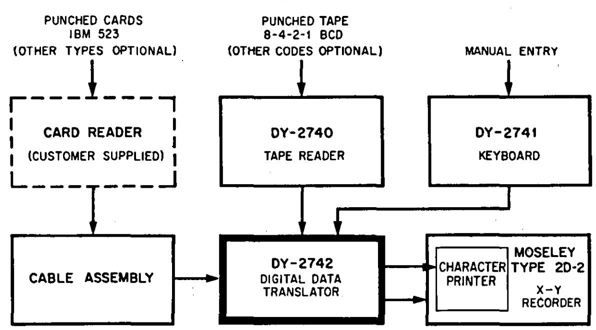


Here's rapid, economical, time-saving conversion of digital data to easy-to-read X-Y charts. Data stored on punched tape or punched cards or tabular data entered manually on a keyboard is quickly plotted with Dymec DY-6242 Digital Data Plotting System. DY-6242 system ability to accept most standard format computer tapes minimizes the need for special computer programming.

The Dymec system is ideal for rapid translation conversion and graphical presentation of data in such areas as stress analysis—verification of numerically controlled machine tool program tapes—pulse height analyzer display—business situations, profit-loss and trend data—thrust analysis—fluid flow and aerodynamic studies—space vehicle trajectory and orbit information—real-time analog parameters acquired digitally, frequency, voltage, current, transients—in any application where large amounts of digital data are more easily understood in graphical form.

Here's the DY-6242 System:



Here's what it offers: Card, perforated tape or keyboard input • Up to 50 points/min. plotted with cards • Up to 80 points/min. with tape • Plot accuracy better than 0.15% • Resolution: 4 digits and sign accepted for both X-Y axes • Zero suppression up to 10,000 counts for convenient placement of plot • All for $8,700.00

Write or call your nearest Dymec/Hewlett-Packard representative or Dymec for full information.

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CIRCLE 14 ON READER CARD

BUSINESS & SCIENCE

THE 1004: A UNIVAC SPIRIT LIFTER

At UNIVAC, the 1004 has proven a potential boon to the dispirited. Announced late in June, there are now over 700 orders in house. For an externally programmed machine, this stripped 1401 competitor appears to have been well received by the burgeoningly ripe punched card market. Most UNIVACites however, wish the 1004 had been announced two years earlier as they anxiously await IBM's Fall counter move.

On another optimistic note, first installation of the Univac III has been made to U.S. Steel in Pittsburgh and there are presently 65 orders in house.

THE 1000: A PHILCO POTENTIAL

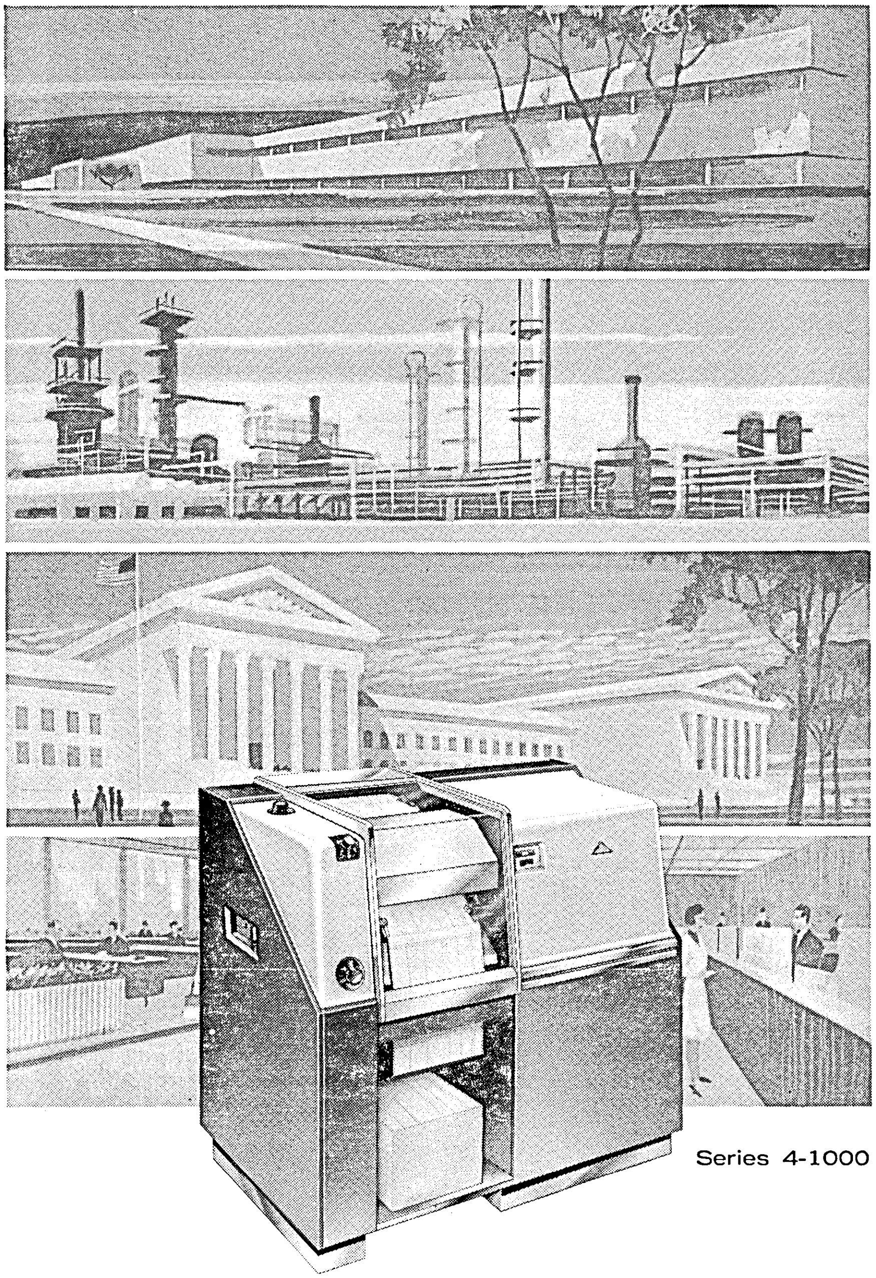
At Ford, a decision has been reached to purchase only Philco computers for both U.S. and overseas installations. First installation in this program is a 2000-211 system (1.5 usec. memory) headed for Dearborn in the latter part of '62. Early in '63, another 2000-211 will be installed at Aeronutronic. Valued at more than 10 megabucks, about 4-5 systems are involved in this most recent declaration of Ford support which may encourage 90 users to review their specs on the 2000.

Philco's peripheral computer first announced in May, has been formally designated the 1000 and with some measure of field success should be eligible for marketing as an independent, small scale machine. This move, expected later this Fall, will require a substantial and broadening of the sales and support staff at Philco and in fact, would guarantee their permanent residence among the major vendors.

ALGOL: A DIMMING GLOW

At a recent meeting in New York City of U.S. representatives influential in ALGOL development, a general feeling expressed was that the future of the language appears dim indeed, not only in this country but in Europe as well. While admittedly superior to Fortran, the economics of implementation and adoption are prohibitive for both the present and foreseeable future.

Therefore, work which has been scheduled for ALGOL



Series 4-1000

BETTER PRINTER PERFORMANCE AT LOWER OVER-ALL COST

That's why more than 40 leading computer manufacturers include Anelex High Speed Printers as standard equipment in their data processing systems.

Further economies are the result of combining print head, power electronics, buffers and logic in a single compact unit. For systems designers, responsibility is clearly defined; for computer manufacturers, engineering and manufacturing costs are reduced.

This work horse of the computer industry provides printing speeds to 1000 lines per minute of full alphanumeric characters on forms 19″ wide by 22″ deep as well as many other types and sizes of paper stock. 120 columns are standard; additional columns to 160 available.

ANELEX

SYMBOL OF QUALITY

Write for new brochure, Series 4-1000.

ANELEX CORPORATION

155 Causeway Street, Boston 14, Mass.

CIRCLE 17 ON READER CARD

MEMO

Re: COMPUTER TIME

Solve your computer problems efficiently and economically by using our: 32K, 10 tape IBM 7090 at $450 per hour or 10K, 10 tape IBM 7070 at $225 per hour.

Whether you need long or short runs, they can be scheduled for all shifts at the same attractive rates.

Included in these low rates is the use of IBM 1401 tape systems on a 2 hours for 1 basis with the 7090, and 1 hour for 1 basis with the 7070, operators and nominal use of all EAM equipment together with card and paper supplies on a limited basis.

Send or mail your program or programs to us, with instructions for running time, and we will return the hard copy within 24 hours.

P.S. Programming or Analysis Assistance Available

This service is YOURS by writing or phoning

CD

COMPUTER DYNAMICS CORPORATION

American National Bank Bldg.
8701 Georgia Avenue
SILVER SPRING, MARYLAND
JU. 8-8054

CIRCLE 38 ON READER CARD

implementation as a U.S. standard is being pursued with comparatively little vigor pending further input from overseas. The following resolution lends support to this inactivity:

"September 6, 1962
American Standards Association, New York City
Subject: USA Resolution to Working Group E
Chairman: R. F. Clippinger, Working Group E
Dear Sir:
The USA presents the following resolution for submission to Working Group E:
Resolved that Working Group E invite IFIP TC-2 to submit to ISO a specification of ALGOL for consideration as an international standard.
From: Howard Bromberg, USA Representative, ISO/TC 97/WG-E"

DPMA: A COMING FORCE

Equipped with a new name and a continuing influx of members (16K in 183 chapters), the Data Processing Management Association (formally NMAA) has shown every indication of usurping the role of ACM in business dp.

One of the more impressive, recent contributions of DPMA is its certification program. (See DATAMATION, p. 25, March, 1962) An examination is now being offered at 45 university test centers. Over 350 candidates were given the original exam in June at New York University.

In education, the DPMA sponsors orientation classes for high school seniors. Courses consist of field trips and 10 weekly sessions of two hours each. Most important, the program is national in scope and in fact.

At their last national convention in New York City, DPMA drew almost 4,000 registrants and 100 exhibitors. The meeting has been generally referred to as outstanding.

Recognition for business data processing has been slow in coming by the ACM. Last December, a Special Interest Group was officially recognized by the national council and this year there were three general sessions and a Hall of Discussion held at ACM's Syracuse conference on this subject. Still the industry's principal scientific professional society, an expansion of interests at a more rapid pace should be encouraged by ACM officers.

THE SOFT SELL . . .

The current emphasis placed on the manufacture of computers may vary widely among the many contenders although a general tendency has been toward overemphasis. An exception worth noting is the following excerpt from a recent news release announcing the opening of New York City offices for El-Tronics, Inc.:

"El-Tronics has manufacturing plants in Warren and Clarendon, Pa., in Jamestown and Mineola, New York, and in Hawthorne, Calif. The company's subsidiaries manufacture incandescent lamps, fluorescent tubes, decorative lighting, photo flash lamps, electric fuses and electronic computers."

AN ANALOG COMPUTER TO YOUR ENGINEERING LAB

A "fully expanded" 20-amplifier PACE® TR-10 analog computer can be delivered to your office or laboratory for as little as $50 a week and the larger 48-amplifier TR-48 computer is yours for a few dollars more. Both of these machines can provide your research or engineering staff with a unique understanding of the dynamics of complex systems, making system design and optimization simpler and faster. Thus, for a fraction of the salary of the average engineer, you can significantly expand the creative output of your present engineering or research effort. This is the reason why hundreds of these computers are already operating in research and development laboratories throughout the world. ☐ The TR-10 and TR-48 computers are fully transistorized and virtually maintenance free. They can be set up on your desk and plugged into any 110-volt outlet. They can be easily understood and readily operated by your present engineering staff and require no extensive operator or programmer training. Here, then, is the "individual engineer's" computer available at a rental rate that makes it practical for every laboratory. ☐ EAI has several advantageous leasing plans. Whether you are interested in lease or purchase, write for full information on these desk-top analog computers today.

EAI

ELECTRONIC ASSOCIATES, INC. *Long Branch, New Jersey*

CIRCLE 18 ON READER CARD

440,000 bits are on this 7″ disc

ACTUAL SIZE

(a world record for magnetic data storage!)

Developed by Soundcraft for use in the RCA 301 Computer Disc File, this disc offers the highest pulse packing capability of any system today. From outer to inner tracks, 200 to 888 bits per inch can be recorded flawlessly—for a total of 220,000 bits per side! (7″ diameter) Two basic Soundcraft accomplishments contribute to this remarkable performance, the magnetic medium and the special disc base. Soundcraft's new heavy duty high density oxide formulation combines remarkable wear life and recording characteristics. This same formulation is used in Soundcraft LWD Computer Tape, the finest heavy-duty, high-density digital tape made today. To assure perfect head intimacy, Soundcraft also developed the special polycarbonate *resilient* disc base to which the incredibly thin oxide coating is applied. And, the cost of this disc is up to 1,000 times less than that of comparable disc-type storage media! Whether your data storage and acquisition requirements call for Computer Tape or rigid surface devices, you'll do best with Soundcraft.

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CIRCLE 19 ON READER CARD

In the time it takes you to read this line
and turn the picture around

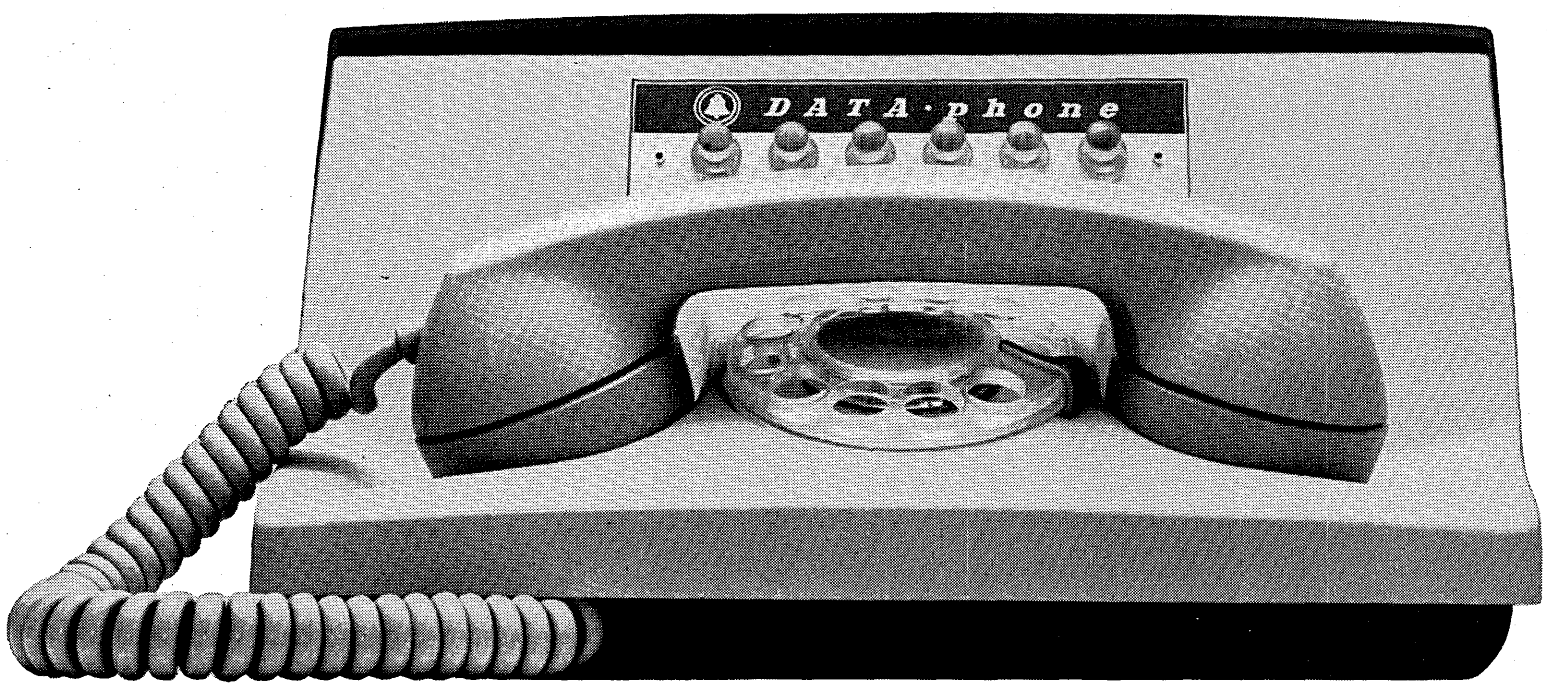
...Bell System DATA-PHONE service could send 200 words of data 3000 miles by telephone!

DATA-PHONE service makes it possible for data processing machines to transmit information by "talking" to each other in high-speed electronic language—over regular telephone lines.

Any kind of data that can be recorded on punched cards, paper or magnetic tape can be transmitted across town or across the country—at regular telephone rates. The result: more efficiency, lower costs, greater profits.

One of our trained Communications Consultants will gladly show you how DATA-PHONE service can be integrated into your data handling operations to save you time and money. Just call your Bell Telephone Business Office and ask for him.

BELL TELEPHONE SYSTEM



CIRCLE 20 ON READER CARD

EDITORS' READOUT

.06 IDEA PER KILOMANYEAR

a guest editorial
by FRED GRUENBERGER

A casual remark made by *Datamation's* genial editor in a recent editorial got me to thinking.

He pointed out that the total number of original, good ideas developed in the entire field of computing was pitifully small. Why not try to quantify this idea?

Let's first try to arrive at an input figure for brain work in the field. The number of people in the field 15 years ago was counted in the hundreds — the low hundreds. By "in the field" we can mean everyone: salesmen, users, designers, maintenance men, branch managers, students — anyone whose business it is to think about computers and how to use them. Now, suppose the figure a year ago was 100,000. What we need to do is integrate the curve of these figures. The 300 or so people active in 1947 (assuming they're all active yet) have piled up now 4,500 man-years of thinking. The 100,000 of last year (who include those 300, to be sure) have expended 100,000 man-years to date. Add it up any way you like (which isn't too easy, since no one was smart enough to keep census figures over the years). The figure I get is this: 500,000 man-years. You may get 400,000 or 600,000; it doesn't matter. It's a lot of man-years. Turning to the other side of the ledger, let's list all the bright ideas we've managed to create. My list follows. It has 30 entries, some small and some earth-shaking. If I've missed some of your favorites—throw 'em in.

Stored Programming	Delay Lines	Disc Files
Assemblers	Indirect Addressing	Transistorization
Compilers	Table Lookup Arithmetic	Thin Films
Self-written Compilers	Look Ahead	Convert Instruction
Interpreters	Parallel Processing	Execute Instruction
Closed Subroutines	Buffering	Addressable Stops
Floating Point	Parity Checking	Alteration Switches
Index Registers	Simulators	Generators
Character Addressable	Monitors	Decimal Capability
Magnetic Cores	Addressable Clocks	Two Headed Tapes

From the first item, which started the whole thing by creating computers (as opposed to externally controlled calculators), we've had about 30 good, solid ideas, collectively.

It figures out to one idea for every 50,000 man-years. If you teach computing, kid, there's one to impress on your classes. If one of your students could come up with the next good idea (it really takes only a fresh pair of eyes and a few seconds of thought), he'd be 'way ahead of the crowd.

You might ask, "What's so different about these figures from those we'd find in any other industry — automobiles, for instance?" The answer is twofold.

First, ours is the industry devoted to extending brainpower. We should be (and, I think, are) receptive to new ideas and eager to use the good ones. We don't have operating in our industry the factors which depress good ideas in other industries.

Secondly, a good idea can gain currency much easier in computing. *Anyone* can try out a software idea to see if it works. It's a bit harder with hardware ideas, but we still have 19 competitive manufacturers and a good new idea should find fertile ground somewhere. ■

(Editor's note: As the first conceptual paper on an internally programmed computer, the following presentation of Burks, Goldstine and von Neumann's *Preliminary Discussion* appears in two parts, the second of which is scheduled for *Datamation's* October issue.

Two reasons are offered for this somewhat unusual decision to regress:

1. Readers may enjoy a brief reflection on the early days of their rapidly advancing profession, and
2. It is possible that someone will ask, "How far have we actually advanced since 1946?"

To the best of our knowledge, this is the first formal publication of *Preliminary Discussion*. The work was originally accomplished at Princeton's Institute for Advanced Study in June, 1946. It appears here in a slightly edited version with much of the detailed mathematical support deleted. However, readers may soon reference the complete paper in one of the forthcoming volumes on the writings of von Neumann to be published this Fall by Pergamon Press, New York City.

To place the paper in its proper historical context, *Datamation* has asked Paul Armer of The RAND Corp. to provide the following introduction:)

an introduction

by PAUL ARMER, The RAND Corp., Santa Monica, California

One frequently hears "There's been nothing really new in machine organization since von Neumann!" Indeed, one would be hard pressed to name a dozen significant differences in logical design between the machine proposed by Burks, Goldstine and von Neumann in 1946 and the machines in use today. One surprising aspect of this story is that their proposed design was never published in a form other than a report to the U. S. Army Ordnance Department under the terms of a contract with the Institute for Advanced Study (IAS) at Princeton. In light of this, *Datamation* has elected to reprint a condensed version of the paper.

Who invented stored programming? Perhaps it doesn't matter much to anyone other than to the principals involved just who gets the credit—we have the concept and it will surely stand as one of the great milestones in man's advances. It could well be one of those things—like the calculus—that emerged simultaneously from several minds when the need and the technology met. The leading contenders are the authors of the paper reprinted here and the group at the University of Pennsylvania led by J. Presper Eckert and John Mauchly. Others undoubtdly contributed, not the least of whom was Babbage, who lived at a time when

PRELIMINARY DISCUSSION OF THE LOGICAL DESIGN OF AN ELECTRONIC COM

by ARTHUR W. BURKS, HERMAN H. GOLDSTINE, and JOHN von NEUMANN

a preface

This report has been prepared in accordance with the terms of Contract W-36-034-ORD-7481 between the Research and Development Service, Ordnance Department, U. S. Army and the Institute for Advanced Study. It is intended as the first of two papers dealing with some apsects of the overall logical considerations arising in connection with electronic computing machines. An attempt is made to give in this, the first half of the report, a general picture of the type of instrument now under consideration and in the second half a study of how actual mathematical problems can be coded, i.e., prepared in the language the machine can understand.

It is the present intention to issue from time to time reports covering the various phases of the project. These papers will appear whenever it is felt sufficient work has been done on a given aspect, either logical or experimental to justify its being reported.

The authors also wish to express their thanks to Dr. John Tukey, of Princeton University, for many valuable discussions and suggestions.

The Institute for Advanced Study

28 June 1946

neither the need nor the technology were present. I do not pretend to know to whom the honor belongs.

Nevertheless, the paper reprinted here is *the* definitive paper in the computer field. Not only does it specify the design of a stored program computer in detail, but it anticipates many knotty problems and suggests ingenious solutions. The machine described in this paper (variously known as the IAS, or Princeton, or von Neumann machine) was constructed and copied, (never exactly,) and the copies were copied. One version of it, built at RAND, was affectionately called JOHNNIAC (over von Neumann's objections). Most of the copies are still in operation although the IAS machine now has its place in history at the Smithsonian.

At the time the paper was written, the principle of automatic calculation was well established (with Harvard's Mark I) as was the great advance gained by electronics (with ENIAC). The jump from that state-of-the-art to the detail of their paper is difficult to measure objectively today. Perhaps it is analogous to someone considering the system of transmitting pictures by means of a rotating scanning disc and a jump to writing a description of compatible color TV.

The reader's attention is called to the lack of phrases like "it might be possible" or "a means might be devised" in this treatise. The tone is entirely one of "here's the way to build it." And they actually built it pretty much that way, the only real differences being in engineering detail and not in the logical design. The selectron tube around which the storage had been planned did not become operational in time and instead a parallel Williams memory utilizing cathode ray tubes was developed. (The selectron was used in RAND's JOHNNIAC and operated quite successfully although with only 256 bits per tube compared with the 4096 discussed below.) The CRT store finally realized at Princeton had a capacity of 1024 40-bit words. Getting it into being was one of the most difficult engineering tasks faced by the Princeton team. The machine also ended up being asynchronous whereas the synchronous approach is discussed in the paper. Nor was a second machine built for checking purposes. With minor exceptions, von Neumann and his group produced what they said they would.

The analysis in this paper of whether or not to build into the hardware the operations of multiplication, division, and square root is exceedingly insightful. On only one point has history shown them to be very far wrong—the utility of built-in floating point operations. To their credit however, they did consider it. They also considered buffering Input/Output but deferred it, and proposed viewing tubes for graphical portrayal of results.

The portions deleted from the following reprint are concerned primarily with extremely detailed descriptions of the arithmetic processes of the machine, since von Neumann felt compelled to prove rigorously that every process would work under every possible condition.

The use of boldface type is the choice of the editor, to highlight many ideas that were not only prophetic, but indicated a deep understanding of what a computer should be like. ■

PUTING INSTRUMENT

1.0 principal component of the machine

1.1 Inasmuch as the completed device will be a general-purpose computing machine it should contain certain main organs relating to arithmetic, memory-storage, control and connection with the human operator. It is intended that the machine be fully automatic in character, i.e., independent of the human operator after the computation starts. A fuller discussion of the implications of this remark will be given in 3 below.

1.2 It is evident that the machine must be capable of storing in some manner not only the digital information needed in a given computation such as boundary values, tables of functions (such as the equation of state of a fluid) and also the intermediate results of the computation (which may be wanted for varying lengths of time), but also the instructions which govern the actual routine to be performed on the numerical data. In a special-purpose machine these instructions are an integral part of the device and constitute a part of its design structure. For an all-purpose machine it must be possible to instruct the device to carry out any whatsoever computation that can be formulated in numerical terms. Hence there must be some organ capable of storing these program orders. There must, moreover, be a unit which can understand these instructions and order their execution.

1.3 **Conceptually we have discussed above two different forms of memory: storage of numbers and storage of orders. If, however, the orders to the machine are reduced to a numerical code and if the machine can in some fashion distinguish a number from an order, the memory organ can be used to store both numbers and orders.**

1.4 If the memory for orders is merely a storage organ there must exist an organ which can automatically execute the orders stored in the memory. We shall call this organ the *Control*.

1.5 Inasmuch as the device is to be a computing machine there must be an arithmetic organ in it which can perform certain of the elementary arithmetic operations. There will be, therefore, a unit capable of adding, subtracting, multiplying and dividing. It will be seen that it can also perform additional operations that occur quite frequently.

The operations that the machine will view as elementary are clearly those which are wired into the machine. To illustrate, the operation of multiplication could be eliminated from the device as an elementary process if one were willing to view it as a properly ordered series of additions. Similar remarks apply to division. In general, the inner economy of the arithmetic unit is determined by a compromise between the desire for speed of operation – a non-elementary operation will generally take a long time to perform since it is constituted of a series of orders given by the Control – and the desire for simplicity, or cheapness, of the machine.

1.6 Lastly there must exist devices, the input and output organ, whereby the human operator and the machine can communicate with each other. This organ will be seen to constitute a secondary form of automatic memory.

2.0 first remarks on the memory.

2.1 It is clear that the size of the memory is a critical consideration in the design of a satisfactory general-purpose computing machine. We proceed to discuss what quantities the memory should store for various types of computations.

2.2 In the solution of partial differential equations the storage requirements are likely to be quite extensive. In general, one must remember not only the initial and boundary conditions and any arbitrary functions that enter the problem but also an extensive number of intermediate results.

a) For equations of parabolic or hyperbolic type in two independent variables the integration process is essentially a double induction: to find the values of the dependent variables at time $t + \Delta t$ one integrates with respect to x from one boundary to the other by utilizing the data at time t as if they were coefficients which contribute to defining the problem of this integration.

Not only must the memory have sufficient room to store these intermediate data but there must be provisions whereby these data can later be removed, i.e., at the end of the $(t + \Delta t)$ cycle, and replaced by the corresponding data for the $(t + 2\Delta t)$ cycle. This process of removing data from the memory and of replacing them with new information must, of course, be done quite automatically under the direction of the Control.

b) For total differential equations the memory requirements are clearly similar to, but smaller than, those discussed in a) above.

c) Problems that are solved by iterative procedures such as systems of linear equations or ellipitic partial differential equations, treated by relaxation techniques, may be expected to require quite extensive memory capacity. The memory requirement for such problems is apparently much greater than for those problems in a) above in which one needs only to store information corresponding to the instantaneous value of one variable (t in a) above), while now entire solutions (covering all values of all variables) must be stored. This apparent discrepancy in magnitudes can, however, be somewhat overcome by the use of techniques which permit the use of much coarser integration meshes in this case, than in the cases under a).

2.3 It is reasonable at this time to build a machine that can conveniently handle problems several orders of magnitude more complex than are now handled by existing machines, electronic or electro-mechanical. We consequently plan on a fully automatic electronic storage facility of about 4,000 numbers of 40 binary digits each. This corresponds to a precision of $2^{-40} \sim .9 \cdot 10^{-12}$, i.e., of about 12 decimals. We believe that this memory capacity exceeds the capacities required for most problems that one deals with at present by a factor of about 10. The precision is also safely higher than what is required for the great majority of present day problems. In addition, we propose we have a subsidiary memory, which is also automatic, of much larger capacity on some medium such as magnetic wire or tape.

3.0 first remarks on the control and code.

3.1 It is easy to see by formal-logical methods, that there exist codes that are in abstracto adequate to control and cause the execution of any sequence of operations which are individually available in the machine and which are, in their entirety, conceivable by the problem planner. The really decisive considerations from the present point of view, in selecting a code, are more of a practical nature: simplicity of the equipment demanded by the code, and the clarity of its application to the actually important problems together with the speed of its handling of those problems. It would take us much too far afield to discuss these questions at all generally or from first principles. We will therefore restrict ourselves to analyzing only the type of code which we now envisage for our machine.

3.2 There must certainly be instructions for performing the fundamental arithmetic operations. The specifications for these orders will not be completely given until the arithmetic unit is described in a little more detail.

3.3 It must be possible to transfer data from the memory to the arithmetic organ and back again. In transferring information from the arithmetic organ back into the memory there are two types we must distinguish: transfers of numbers as such and transfers of numbers which are parts of orders. The first case is quite obvious and needs no further explication. The second case is more subtle and serves to illustrate the generality and simplicity of the system. Consider, by way of illustration, the problems of interpolation in the system. Let us suppose that we have formulated the necessary instructions for performing an interpolation of order n in a sequence of data. The exact location in the memory of the $(n + 1)$ quantities that bracket the desired functional value is, of course, a function of the argument. This argument probably is found as the result of a computation in the machine. We thus need an order which can substitute a number into a given order —in the case of interpolation the location of the argument or the group of arguments that is nearest in our table to the desired value. By means of such an order the results of a computation can be introduced into the instructions governing that or a different computation. **This makes it possible for a sequence of instructions to be used with different sets of numbers located in different parts of the memory.**

To summarize, transfers into the memory will be of two sorts: *total substitutions*, whereby the quantity previously stored is cleared out and replaced by a new number. *Partial substitutions* in which that part of an order containing a *memory location-number*—we assume the various positions in the memory are enumerated serially by memory location-numbers—is replaced by a new memory location-number.

3.4 It is clear that one must be able to get numbers from any part of the memory at any time. **The treatment in the case of orders can, however, be more methodical since one can at least partially arrange the control instructions in a linear sequence. Consequently the Control will be so constructed that it will normally proceed from place n in the memory to place (n + 1) for its next instruction.**

3.5 The utility of an automatic computer lies in the possibility of using a given sequence of instructions repeatedly, the number of times it is iterated being either preassigned or dependent upon the results of the computation. When the iteration is completed a different sequence of orders is to be followed, so we must, in most cases, give two parallel trains of orders preceded by an instruction as to which routine is to be followed. This choice can be made to depend upon the sign of a number (zero being reckoned as plus for machine purposes). Consequently we introduce an order *(the conditional transfer order)* **which will, depending on the sign of a given number, cause the proper one of two routines to be executed.**

Frequently two parallel trains of orders terminate in a common routine. It is desirable, therefore, to order the control in either case to proceed to the beginning point of the common routine. This *unconditional transfer* can be achieved either by the artificial use of a conditional transfer or by the introduction of an explicit order for such a transfer.

3.6 Finally we need orders which will integrate the input-output devices with the machine.

3.7 We proceed now to a more detailed discussion of the machine. Inasmuch as our experience has shown that the moment one chooses a given component as the elementary memory unit one has also more or less determined upon much of the balance of the machine, we start by a consideration of the memory organ. In attempting an exposition of a highly integrated device like a computing machine we do not find it possible, however, to give an exhaustive discussion of each organ before completing its description. It is only in the final block diagrams that anything approaching a complete unit can be achieved.

4.0 the memory organ.

4.1 Ideally one would desire an indefinitely large memory capacity such that any particular aggregate of 40 binary digits, or *word,* would be immediately available—i.e., in a time which is somewhat or considerably shorter than the operation time of a fast electronic multiplier. This may be assumed to be practical at the level of about 100 microseconds. **Hence the availability time for a word in the memory should be 5 to 50 microseconds.** It is equally desirable that words may be replaced with new words at about the same rate. It does not seem possible physically to achieve such a capacity. **We are therefore forced to recognize the possibility of constructing a hierarchy of memories, each of which has greater capacity than the preceding, but which is less quickly accessible.**

The most common forms of storage in electrical circuits are the flip-flop or trigger circuit, the gas tube, and the electro-mechanical relay. To achieve a memory of n words would, of course, require about 40 n such elements, exclusive of the switching elements. *We saw earlier that a fast memory of several thousand words is not at all unreasonable for an all-purpose instrument. Hence, about 10^5 flip-flops or analogous elements would be required! This would, of course, be entirely impractical.*

We must therefore seek out some more fundamental method of storing electrical information than has been suggested above. One criterion for such a storage medium is that the individual storage organs, which accommodate only one binary digit each, should not be macroscopic components, but rather microscopic elements of some suitable organ. They would then, of course, not be identified and switched to by the usual macroscopic wire connections, but by some functional procedure in manipulating that organ.

One device which displays this property to a marked degree is the iconoscope tube. In its conventional form it possesses a linear resolution of about one part in 500. This would correspond to a (two-dimensional) memory capacity of $500 \times 500 = 2.5 \cdot 10^5$. One is accordingly led to consider the possibility of storing electrical charges on a dielectric plate inside a cathode-ray tube. Effectively such a tube is nothing more than a myriad of electrical capacitors which can be connected into the circuit by means of an electron beam.

Actually the above mentioned high resolution and concomitant memory capacity are only realistic under the conditions of television-image storage, which are much less exigent in respect to the reliability of individual markings than what one can accept in the storage for a computer. In this latter case resolutions of one part in 20 to 100, i.e. memory capacities of 400 to 10,000 would seem to be more reasonable in terms of equipment built essentially along familiar lines.

At the present time the Princeton Laboratories of the Radio Corporation of America are engaged in the development of a storage tube, the *Selectron,* of the type we have mentioned above. This tube is also planned to have a non-amplitude-sensitive switching system whereby the electron beam can be directed to a given spot on the plate within a quite small fraction of a millisecond. Inasmuch as the storage tube is the key component of the machine envisaged in this report we are extremely fortunate in having secured the cooperation of the RCA group in this as well as in various other developments.

An alternate form of rapid memory organ is the feedback delay line described in various reports on the EDVAC. (This is an electronic computing machine being developed for the Ordnance Department, U.S. Army, by the University of Pennsylvania, Moore School of Electrical Engineering.) Inasmuch as that device has been so clearly reported in those papers we give no further discussion. There are still other physical and chemical properties of matter in the presence of electrons or photons that might be considered but since none is yet beyond the early discussion stage we shall not make further mention of them.

4.2 We shall accordingly assume throughout the balance of this report that the Selectron is the modus for storage of words at electronic speeds. As now planned this tube will have a capacity of $2^{12} = 4{,}096$, or approximately 4,000 binary digits. To achieve a total electronic storage of about 4,000 words we propose to use 40 Selectrons, thereby achieveing a memory of 2^{12} words of 40 binary digits. (Cf. again 2.3.)

4.3 There are two possible means for storing a particular word in the Selectron Memory—or in fact in either a delay line memory or in a storage tube with amplitude-sensitive deflection. One method is to store the entire word in a given tube and then to get the word out by picking out its respective digits in a serial fashion. The other method is to store in corresponding places in each of the 40 tubes one digit of the word. To get a word from the memory in this scheme requires, then, one switching mechanism to which all 40 tubes are connected in parallel. Such a switching scheme seems to us to be simpler than the technique needed in the serial system and is, of course, 40 times faster. **We accordingly adopt the parallel procedure and thus are led to consider a so-called** *parallel machine,* **as contrasted with the serial principles being**

considered for the EDVAC. (In the EDVAC the peculiar characteristics of the acoustic delay line, as well as various other considerations, seem to justify a serial procedure. For more details cf, the reports referred to in 4.1.) The essential difference between these two systems lies in the method of performing an addition; in a parallel machine all corresponding pairs of digits are added simultaneously, whereas in a serial one these pairs are added serially in time.

4.4 To summarize, we assume that the fast electronic memory consists of 40 Selectrons which are switched in parallel by a common switching arrangement. The inputs of the switch are controlled by the Control.

4.5 Inasmuch as a great many highly important classes of problems require a far greater total memory than 2^{12} words, we now consider the next stage in our storage hierarchy. Although the solution of partial differential equations frequently involves the manipulation of many thousands of words, these data are generally required only in blocks which are well within the 2^{12} capacity of the electronic memory. Our second form of storage must therefore be a medium which feeds these blocks of words to the electronic memory. It should be controlled by the Control of the computer and is thus an integral part of the system, not requiring human intervention.

There are evidently two distinct problems raised above. One can choose a given medium for storage such as teletype tapes, magnetic wire or tapes, movie film or similar media. There still remains the problem of automatic integration of this storage medium with the machine. This integration is achieved logically by introducing appropriate orders into the code which can instruct the machine to read or write on the medium, or to move it by a given amount or to a place with given characteristics. We discuss this question a little more fully in 6.8.

Let us return now to the question of what properties the secondary storage medium should have. It clearly should be able to store information for periods of time long enough so that only a few percent of the total computing time is spent in re-registering information that is "fading" off. It is certainly desirable, although not imperative, that information can be erased and replaced by new data. The medium should be such that it can be controlled, i.e., moved forward and backward, automatically. This consideration makes certain media, such as punched cards, undesirable. While cards can, of course, be printed or read by appropriate orders from some machine, they are not well adapted to problems in which the output data are fed directly back into the machine, and are required in a sequence which is non-monotone with respect to the order of the cards. The medium should be capable of remembering very large numbers of data at a much smaller price than electronic devices. It must be fast enough so that, even when it has to be used frequently in a problem, a large percentage of the total solution time is not spent in getting data into and out of this medium and achieving the desired positioning on it. **If this condition is not reasonably well met, the advantages of the high electronic speeds of the machine will be largely lost.**

Both light- or electron-sensitive film and magnetic wires or tapes, whose motions are controlled by servo-mechanisms integrated with the Control, would seem to fulfill our needs reasonably well. We have tentatively decided to use magnetic wires since we have achieved reliable performance with them at pulse rates of the order of 25,000 per second and beyond.

4.6 Lastly our memory hierarchy requires a vast quantity of dead storage, i.e., storage not integrated with the machine. This storage requirement may be satisfied by a library of wires that can be introduced into the machine when desired and at that time become automatically controlled. Thus our dead storage really is nothing but an extension of our secondary storage medium. It differs from the latter only in its availability to the machine.

4.7 We impose one additional requirement on our secondary memory. It must be possible for a human to put words onto the wire or other substance used and to read the words put on by the machine. In this manner the human can control the machine's functions. It is now clear that the secondary storage medium is really nothing other than a part of our input-output system.

4.8 There is another highly important part of the input-output which we merely mention at this time, namely, some mechanism for viewing graphically the results of a given computation. This can, of course, be achieved by a Selectron-like tube which causes its screen to fluoresce when data are put on it by an electron beam.

4.9 For definiteness in the subsequent discussions we assume that associated with the output of each Selectron is a flip-flop. This assemblage of 40 flip-flops we term the *Selectron Register*.

5.0 the arithmetic organ.

5.1 In this chapter we discuss the features we now consider desirable for the arithmetic part of our machine. We give our tentative conclusions as to which of the arithmetic operations should be built into the machine and which should be programmed. Finally, a schematic of the arithmetic unit is described.

5.2 In a discussion of the arithmetical organs of a computing machine one is naturally led to a consideration of the number system to be adopted. **In spite of the long-standing tradition of building digital machines in the decimal system, we feel strongly in favor of the binary system for our device.** Our fundamental unit of memory is naturally adapted to the binary system since we do not attempt to measure gradations of charge at a particular point in the Selectron but are content to distinguish two states. The flip-flop again is truly a binary device. On magnetic wires or tapes and in acoustic delay line memories one is also content to recognize the presence or absence of a pulse or (if a carrier frequency is used) of a pulse train, or of the sign of a pulse. (We will not discuss here the ternary possibilities of a positive or negative or no pulse system and their relationship to questions of reliability and checking, nor the very interesting possibilities of carrier frequency modulation.) Hence if one contemplates using a decimal system with either the Iconoscope or delay line memory one is forced into a binary coding of the decimal system—each decimal digit being represented by at least a tetrad of binary digits. Thus an accuracy of ten decimal digits requires at least 40 binary digits. In a true binary representation of numbers, however, about 33 digits suffice to achieve a precision of 10^{10}. **The use of the binary system is therefore somewhat more economical of equipment than is the decimal.**

The main virtue of the binary system as against the decimal is, however, the greater simplicity and speed with which the elementary operations can be performed. To illustrate, consider multiplication by repeated addition. In binary multiplication the product of a particular digit of the multiplier by the multiplicand is either the multiplicand or null according as the multiplier digit is 1 or 0. In the decimal system, however, this product has ten possible values between null and nine times the multiplicand, inclusive. Of course, a decimal number has only $\log_{10}2 \sim .3$ times as many digits as a binary number of the same accuracy, but even so multiplication in the decimal system is considerably longer than in the binary system. One can accelerate decimal multiplication by complicating the circuits, but this fact is irrelevant to the point just made since binary multiplication can likewise be accelerated by adding to the equipment. Similar remarks may be made about the other operations.

An additional point that deserves emphasis is this: an important part of the machine is not arithmetical, but logical in nature. Now logics, being a yes-no system, is fundamentally binary. Therefore a binary arrangement of the arithmetical organs contributes very significantly towards producing a more homogenous machine, which can be better integrated and is more efficient.

The one disadvantage of the binary system from the human point of view is the conversion problem. **Since, however, it is completely known how to convert numbers from one base to another and since this conversion can be effected solely by the use of the usual arithmetic processes there is no reason why the computer itself cannot carry out this conversion.** It might be argued that this is a time consuming operation. This, however, is not the case. Indeed a general-purpose computer used as a scientific research tool, is called upon to do a very great number of multiplications upon a relatively small amount of input data, and hence the time consumed in the decimal to binary conversion is only a trivial percent of the total computing time. A similar remark is applicable to the output data.

In the preceding discussion we have tacitly assumed the desirability of introducing and withdrawing data in the decimal system. We feel, however, that the base 10 may not even be a permanent feature in a scientific instrument and consequently will probably attempt to train ourselves to use numbers base 2 or 8 or 16. The reason for the bases 8 or 16 is this: since 8 and 16 are powers of 2 the conversion to binary is trivial; since both are about of the size of 10, they violate many of our habits less badly than base 2.

5.3 Several of the digital computers being built or planned in this country and England are to contain a so-called "floating decimal point." This is a mechanism for expressing each word as a characteristic and a mantissa—e.g., 123. 45 would be carried in the machine as (0.12345, 03), where the 3 is the exponent of 10 associated with the number. There appear to be two major purposes in a "floating" decimal point system both of which arise from the fact that the number of digits in a word is a constant, fixed by design considerations for each particular machine. The first of these purposes is to retain in a sum or product as many significant digits as possible and the second of these is to free the human operator from the burden of estimating and inserting into a problem "scale factors"—multiplicative constants which serve to keep numbers within the limits of the machine.

There is, of course, no denying the fact that human time is consumed in arranging for the introduction of suitable scale factors. We only argue that the time so consumed is a very small percentage of the total time we will spend in preparing an interesting problem for our machine. The first advantage of the floating point is, we feel, somewhat illusory. **In order to have such a floating point one must waste memory capacity which could otherwise be used for carrying more digits per word. It would therefore seem to us not at all whether the modest advantages of a floating binary point offset the loss of memory capacity and the increased complexity of the arithmetic and control circuits.**

There are certainly some problems within the scope of our device which really require more than 2^{-40} precision. **To handle such problems we wish to plan in terms of words whose lengths are some fixed integral multiple of 40 and program the machine in such a manner as to give the corresponding aggregates of 40 digit words the proper treatment.** We must then consider an addition or multiplication as a complex operation programmed from a number of primitive additions or multiplications (cf. Chapter IX, Part II). There would seem to be considerable extra difficulties in the way of such a procedure in an instrument with a floating binary point.

The reader may remark upon our alternate spells of radicalism and conservatism in deciding upon various possible features for our mechanism. We hope, however, that he will agree on closer inspection, that we are guided by a consistent and sound principle in judging the merits of any idea. We wish to incorporate into the machine—in the form of circuits—only such logical concepts as are either necessary to have a complete system or highly convienient because of the frequency with which they occur and the influence they exert in the relevant mathematical situations.

5.4 On the basis of this criterion we definitely wish to build into the machine circuits which will enable it to form the binary sum of two 40 digit numbers. We make this decision not because addition is a logically basic notion but rather because it would slow the mechanism as well as the operator down enormously if each addition were programmed out of the more simple operations of "and," "or," and "not." The same is true for the subtraction. Similarly we reject the desire to form products by programming them out of additions, the detailed motivation being very much the same as in the case of addition and subtraction. The cases for division and square-rooting are much less clear.

It is well known that the reciprocal of a number a can be formed to any desired accuracy by iterative schemes. One such scheme consists of improving an estimate X by forming $X' = 2X - aX^2$. Thus the new error $1 - aX'$ is $(1 - aX)^2$, which is the square of the error in the preceding estimate. We notice that in the formation of X^1, there are two bonafide multiplications—we do not consider multiplication by 2 as a true product since we will have a facility for shifting right or left in one or two pulse times. If then we somehow could guess 1/a to a precision of 2^{-5}, 6 multiplications—3 iterations—would suffice to give a final result good to 2^{-40}. Accordingly a small table of 2^4 entries could be used to get the initial estimate of 1/a. In this way a reciprocal 1/a could be formed in 6 multiplication times, and hence a quotient b/a in 7 multiplication times. Accordingly we see that the question of building a divider is really a function of how fast it can be made to operate compared to the iterative method sketched above: **in order to justify its existence, a divider must perform a division in a good deal less than 7 multiplication times.** We have however conceived a divider which is much faster than these 7 multiplication times and therefore feel justified in building it, especially since the amount of equipment needed above the requirements of the multiplier is not important.

It is, of course, also possible to handle square roots by iterative techniques. In fact, if X is our estimate of $a^{1/2}$, then $X' = \frac{1}{2}(X + a/X)$ is a better estimate. We see that this scheme involves one division per iteration. As will be seen below in our more detailed examination of the arithmetic organ we do not include a square-rooter in our plans because such a device would involve more equipment than we feel is desirable in a first model.

5.5 The first part of our arithmetic organ requires little discussion at this point. It should be a parallel storage organ which can receive a number and add it to the one already in it, which is also able to clear its contents and which can transmit what it contains. **We will call such an organ an *Accumulator*.** It is quite conventional in principle in past and present computing machines of the most varied types. (e.g.: desk multipliers, standard IBM counters, more modern relay machines, the ENIAC.) There are, of course, numerous ways to build such a binary accumulator. We distinguish two broad types of such devices:

static and dynamic or pulse-type accumulators. It is first necessary to make a few remarks concerning the arithmetic of binary addition. In a parallel accumulator, the first step in an addition is to add each digit of the addend to the corresponding digit of the augend. The second step is to perform the carries, and this must be done in sequence since a carry may produce a carry. In the worst case, 39 carries will occur. Clearly it is inefficient to allow 39 times as much time for the second step (performing the carries) as for the first step (adding the digits). **Hence either the carries must be accelerated, or use must be made of the average number of carries or both . . .**

5.7 . . . It is convenient to discuss at this point our treatment of negative numbers, and in order to do that right, it is desirable to make some observations about the treatment of numbers in general.

Our numbers are 40 digit aggregates, the left-most digit being the sign digit, and the other digits genuine binary digits, with positional values $2^{-1}, 2^{-2}, \ldots, 2^{-39}$ (going from left to right). Our accumulator will, however, treat the sign digit, too, as a binary digit with the positional value 2^0—at least when it functions as an adder. For numbers between 0 and 1 this is clearly all right: the left-most digit will then be 0, and if 0 at this place is taken to represent a + sign, then the number is correctly expressed with its sign and 39 binary digits.

Let us now consider one or more unrestricted 40 binary digit numbers. The Accumulator will add them, with the digit-adding and the carrying mechanisms functioning normally and identically in all 40 positions. There is one reservation, however: if a carry originates in the left-most position, then it has nowhere to go from there (there being no further positions to the left), it is "lost." This means, of course, that the addend and the augend, both numbers between 0 and 2, produced a sum exceeding 2, and the accumulator, being unable to express a digit with a positional value 2^1, which would now be necessary, omitted 2, i.e. the sum was formed correctly, excepting a possible error 2. If several such additions are performed in succession, then the ultimate error may be any integer multiple of 2, i.e. the accumulator is an adder which allows errors that are integer multiples of 2—it is an adder *modulo* 2.)

It should be noted that our convention of placing the binary point immediately to the right of the left-most digit has nothing to do with the structure of the adder. In order to make this point clearer we proceed to discuss the possibilities of positioning the binary point in somewhat more detail.

We begin by enumerating the 40 digits of our numbers (words) from left to right. In doing this we use an index h = 1, ., 40. Now we might have placed the binary point just as well between digits j and j+1, j=0, 1, . , 40. Note, that j=0 corresponds to the position at the extreme left (there is no digit h = j = 0); j=40 corresponds to the position at the extreme right (there is no position h= j+1 = 41); and j=1 corresponds to our above choice. Whatever our choice of j, it does not affect the correctness of the Accumulator's addition. (This is equally true for subtraction, cf. below, but not for multiplication and division, cf. 5.8.) Indeed, we have merely multiplied all numbers by 2^{j1} (as against our previous convention), and such a "change of scale" has no effect on addition (and subtraction). However, now the accumulator is an adder which allows errors that are integer multiples of 2^j—it is an adder *modulo* 2^j. We mention this because it is occassionally convenient to think in terms of a convention which places the binary point at the right end of the digital aggregate. Then j=40, our numbers are integers, and the accumulator is an adder *modulo* 2^{40}. We must emphasize, however, that all of this, i.e. all attributions of values to j, are purely convention—i.e. it is solely the mathematician's interpretation of the functioning of the machine—and not a physical feature of the machine. This convention will necessitate measures that have to be made effective by actual physical features of the machine—i.e. the convention will become a physical and engineering reality—only when we come to the organs of multiplication.

. . . Since x and y are 39 digit binaries, their exact product xy is a 78 digit binary (we disregard the sign digit throughout). However, A will only hold 39 of these. These are clearly the left 39 digits of xy. The right 39 digits of xy are dropped from A one by one in the course of the 39 steps, or to be more specific, of the 39 right shifts. We will see later that these right 39 digits of xy should and will also be conserved. The left 39 digits, which remain in A, should also be rounded off, but we will not discuss this matter here.

To complete the general picture of our multiplication technique we must consider how we sense the respective digits of our multiplier. There are two schemes which come to one's mind in this connection. One is to have a gate tube associated with each flip-flop of AR in such a fashion that this gate is open if a digit is 1 and closed if it is null. We would then need a 39 stage counter to act as a switch which would successively stimulate these gate tubes to react. A more efficient scheme is to build into AR a shifter circuit which enables AR to be shifted one stage to the right each time A is shifted and to sense the value of the digit in the right-most flip-flop of AR. The shifter itself requires one gate tube per stage. We need in addition a counter to count out the 39 steps of the multiplication, but this can be achieved by a six stage binary counter. Thus the latter is more economical of tubes and has one additional virtue from our point of view which we discuss in the next paragraph.

The choice of 40 digits to a word (including the sign) is probably adequate for most computational problems but situations certainly might arise when we desire higher precision, i.e. words of greater length. A trivial illustration of this would be the computation of π to more places than are now known (about 700 decimals, i.e. about 2,300 binaries). More important instances are the solutions of N linear equations in N variables for large values of N. The extra precision becomes probably necessary when N exceeds a limit somewhere between 20 and 40. A justification of this estimate has to be based on a detailed theory of numerical matrix inversion which will be given in a subsequent report. It is therefore desirable to be able to handle numbers of 39k digits and sign by means of program instructions. One way to achieve this end is to use k words to represent a 39k digit number with sign. (In this way 39 digits in each 40 digit word are used, but all sign digits, excepting the first one, are apparently wasted.) It is, of course, necessary in this case to instruct the machine to perform the elementary operations of arithmetic in a manner that conforms with this interpretation of k-word complexes as single numbers. In order to be able to treat numbers in this manner, it is desirable to keep not 39 digits in a product, but 78. To accomplish this end (conserving 78 product digits) we connect, via our shifter circuit, the right-most digit of A with the left-most non-sign digit of AR. Thus, when in the process of multiplication a shift is ordered, the last digit of A is transferred into the place in AR made vacant when the multiplier was shifted.

5.9 To conclude our discussion of the multiplication of positive numbers, we note this:

As described thus far, the multiplier forms the 78 digit product, xy, for a 39 digit multiplier x and a 39 digit multiplicand y. We assumed $x \geqq O$, $y \leqq O$ and therefore had $xy \geqq O$, and we will depart from these assumptions only in 5.10. In addition to these, however, we also assumed $x < 1$, $y < 1$, i.e. that x, y have their binary points both immediately right of the sign digit, which implied the same for xy. One might question the necessity of these additional assumptions.

Prima facie they may seem mere conventions, which affect only the mathematician's interpretation of the functioning of the machine, and not a physical feature of the machine. Indeed: if x had its binary point between digits j and j+1 from the left and y between k and k+1, then our above method of multiplication would still give the correct result xy, provided that the position of the binary point in xy is appropriately assigned. Specifically: let the binary point of xy between digits χ and $\chi+1$. x has the binary point between digits j and j+1, and its sign digit is 0, hence its range is $0 \leqq x < 2^{j-1}$. Similarly y has the range $0 \leqq y < 2^{k-1}$, and xy has the range $0 \leqq y < 2^{1-1}$. Now the ranges of x and y imply that the range of xy is necessarily $0 \leqq xy < 2^{j-1}\, 2^{k-1} = 2^{j+k-2}$. Hence $\chi = j+k-l$. Thus it might seem that our actual positioning of the binary point—immediately right of the sign digit, i.e. j=k=l—is still a mere convention.

It is therefore important to realize that this is not so: the choices of j and k actually correspond to very real, physical, engineering decisions. The reason for this is as follows: it is desirable to base the running of the machine on a sole, consistent mathematical interpretation. It is therefore desirable that all arithmetical operations be performed with an identically conceived positioning of the binary point in A. Applying this principle to x and y gives j = k. Hence the position of the binary point for xy is given by j+k-l = 2j-l. If this is to be the same as for x, and y, then 2j-l = j, i.e. j = l ensues—that is our above positioning of the binary point immediately right of the sign digit.

There is one possible escape: To place into A not the left 39 digits of xy (not counting the sign digit 0), but the digits j to j+38 from the left. Indeed, in this way the position of the binary point of xy will be (2j-l) — (j-l) = j, the same as for x and y.

This procedure means that we drop the left j-l and right 40-j digits of xy and hold the middle 39 in A. Note, that positioning of the binary point means that $x < 2^{j-1}$, $y < 2^{j-1}$ and xy can only be used if $xy < 2^{j-1}$. Now the assumptions secure only $xy < {}^{2j-2}$. Hence xy must be 2^{j-1} times smaller than it might be. This is just the thing which would be secured by the vanishing of the left j-1 digits that we had to drop from A, as shown above.

If we wanted to use such a procedure, with those dropped left j-1 digits really existing, i.e. with $j \neq 1$, then we would have to make physical arrangements for their conservation elsewhere. Also the general mathematical planning for the machine would be definitely complicated, due to the physical fact that A now holds a rather arbitrarily picked middle stretch of 39 digits from among the 78 digits of xy. Alternatively, we might fail to make such arrangements, but this would necessitate to see to it in the mathematical planning of each problem, that all products turn out to be 2^{j-1} times smaller than their a priori maxima. Such an observance is not at all impossible, indeed similar things are unavoidable for the other operations. (E.g. with a factor 2 in addition [of positives] or subtraction [of opposite sign quantities]. However, it involves a loss of significant digits, and the choice j=1 makes it unnecessary in multiplication.)

We will therefore make our choice j=1, i.e. the positioning of the binary point immediately right of the sign digit, binding for all that follows. . . .

(To be concluded next month) ■

an educational package from UNIVAC

THE 422 & PREP

The UNIVAC 422, described as a miniature computer with large-scale characteristics, has been announced by UNIVAC. Specifically designed for programmer, operator and general data processing training, the 422 has a core memory of 512 15-bit words and a cycle time of six microseconds.

The computer is the main element of a new education system called PREP (PRogrammed Educational Package) and is sold with teaching aids for classroom use. Price of the 422 is $40,200; delivery will be made approximately six months after receipt of order.

A repertoire of 16 basic instructions can be expanded to 64 through the use of modifiers. Instruction times are: add, 12 usec. (total execution time); multiply, 30-60 usec.; divide, 57 usec. Two channels are available for I/O, using a typewriter keyboard with a tape punch and reader.

Plug-in transistor diode circuit boards, full parallel operation, and program-step running modes are other features. The computer mav be operated from any 60 cycle, 115 volt AC source supplying 500 watts of power. Overall dimensions are: length, 54″; height, 26″; depth, 9″.

The educational package includes a programmed teaching textbook, designed to stimulate students to progress individually according to their learning rate. A course outline, aimed at simplifying preparation of laboratory and classroom sessions, completes the PREP system.

Four areas may be covered: teaching of dp fundamentals through student participation in console interpretation, use of binary and octal notation, and logic circuits; orienting the beginning programmer as well as permitting the intermediate student to advance by realistic duplication of large-scale systems programming problems, flow charting, coding, indexing, debugging and interpretation of results; enabling potential operators to learn how to prepare program tapes, load programs, use a control console and read and interpret console indicators; and providing first-hand experience in maintenance procedures, including fault diagnosis, isolation of troubles, use of test equipment, diagnostic routines, and testing and replacement of circuit modules. ■

PROGRAMMING SCHISMS

and their future

by CHRISTOPHER J. SHAW
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In the very early days of the computing profession fifteen years ago, as some of you may remember, the people who designed and built computers were the ones who programmed them, and usually the ones who used the tabulated results of the computation, as well. Since then, of course, we have come a long way toward specialization. We are no longer computer specialists, but computer designers, computer programmers — and a growing few are even computer users. In very rough terms, the distinction is this: the designer builds them, the programmer trains them, and the user watches them perform — or, occasionally, they watch the user perform.

This trend toward specialization may be unfortunate, but it's probably inevitable, and it's certainly increasing. These three sub-specialties are even now being partitioned into sub-sub-specialties. Take the case of computer programmers for example, since this is what I'd like to discuss. Two major and orthogonal schisms are currently splitting this field into four parts.

The first schism, more spectacular and therefore more superficial, is the growing breach between the scientific and engineering computation boys who talk ALGOL and write programs in FORTRAN (which is something of a comedown) and the business data processing boys who talk English and write programs in COBOL (which is even more of a comedown.) It has already reached the point where the FORTRAN programmers and the COBOL programmers couldn't talk to each other if they wanted to — which, of course, they seldom do. We may hope, however, that this breach will be only temporary, and that COBOL and FORTRAN will both eventually pass away — to be replaced by what is entirely feasible: a *Uni*versal, *P*rocedure-*O*riented *L*anguage (which I hereby christen, UNIPOL.)

The other schism, which is less immediately apparent but deeper and likely to be more enduring, is between the systems programmers — who must tame the beast the computer designers build — and the applications programmers — who must then train the tamed beast to perform for the user. This split will probably grow to be the fundamental one in the computing profession. The basic difference will then be between those who are interested in machines and how to use them, and those who are interested in various problems and how to solve them. Thus, the computer designers and the systems programmers will probably amalgamate into one, fairly homogeneous, professional group, and this long-awaited marriage may eventually prove so fruitful that the computer users will be able to dispense almost entirely with full-time, professional applications programmers, and communicate with the resulting systems directly. The applications programmers, on the other hand, will probably dissolve, with the computer users, into the various problem disciplines, becoming archeologists, botanists, information retrieval specialists, or what have you.

By excluding the crass problem specialist types, who actually want to use these wonderful computer toys for mundane purposes, the merging of computer designers and systems programmers into computer specialists and the decomposition of applications programmers and computer users into problem specialists of various stripes will bring the computing profession back almost to its pristine beginnings, back to when there was only one professional type: the all-around, computer specialist.

This will probably be the best thing that's happened to computing since the advent of alphabetic input-output. But whether this will be the programmer's millenium, I leave to the reader to decide. ■

LET'S SETTLE ALGOL!

with less heat and more light

by HERBERT M. TEAGER, Computation Center,
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Far from leading to unification or an exchange of information and progress in our profession, ALGOL has led to considerable discord and confusion. An issue which drags this long can hardly be considered as a healthy, technical debate. The time is now ripe for easing the current discord.

At this point there is little to be gained by questioning the motives or the intelligence of many people who have discussed ALGOL, in and out of print, and instead it should perhaps be conceded that in the time-honored tradition of the blind men and the elephant, no one has very strongly bothered to clarify his viewpoint or concede that there are other views.

Perhaps the most fundamental difficulty in the area of artificial languages in general and ALGOL in particular is the lack of clarification of what set of standards or criteria apply in judging it, i.e., is this a problem of esthetics; of mathematics; or of science in general, and linguistics in particular. It might not be completely self evident that the standards used in each of these areas of knowledge differ greatly, and in fact may conflict. Yet it is clear that the criteria of beauty and elegance in art; generality, economy of expression, and axiomatic construction in mathematics; or proof in the discovery and verification of truth in natural phenomena differ greatly, and in fact may not be at all appropriate for the question of language design.

In my opinion, the problem of proper design of an algebraic language lies totally in the realm of engineering, and the utilitarian and pragmatic criteria of that field are far more suited for handling such a many-faceted problem. After all, engineers must constantly live with approximate solutions to problems for which science is not yet able to exact precise answers, yet there is little acrimonious debate on such topics as "I like two phase induction motors" or "I think that large motors are more general than small ones."

Historically, engineers have learned (sometimes the hard way) that if they are to make any progress, they must lay out *all* of the objectives for their systems, working with what knowledge or insight that science can provide, and attempt to come up with some sort of optimal design, with the knowledge that nature or the public stand ready, willing, and able to demonstrate (a la Tacoma Narrow's Bridge) the error of his ways. They have also learned both the virtues and defects of standardization, and by and large, do standardize in areas that make sense in terms of lightening their own load or cost of manufacture.

Now, it seems that in an engineering context, one might inquire as to the basic objectives of an algebraic language. If one did this, he might conclude that in this context many of the present loud shouts about ALGOL turn out to be somewhat meaningless. My list for a set of objectives would be the following:

1. The basic objective of an algebraic language is to minimize the amount of human effort and elapsed time required from the formulation of a given numerical model, to the production by digital computer of results pertinent to that model.

As *corollaries* of this basic objective, one might also list the following sub-objectives:

a. The language should be somewhat commonly accepted as a publication medium for sharing "programs" and thus minimizing unnecessary duplication.

b. The language should allow for operations (such as function evaluation, array manipulation, storage allocation) which, while straight-forward, become tedious and error prone if done by humans.

c. The language should be compact (in the sense of requiring a minimal number of symbols to express a computation or declaration), yet should be readable enough in so that changes can be easily made in a program where the process is made as apparent as possible. Otherwise, there would be a valid argument for making machine code the standard language, because it is obviously sufficiently general to carry out any process described in other languages.

d. The language should not itself be error prone in the sense of having many built-in restrictions which are not readily apparent to the programmer. If at all possible, the language should even be somewhat redundant and forgiving of minor clerical error.

e. The language should allow for operations upon variables of any type for which expressions in a statement form are less cumbersome than in machine language form, and conversely should not allow for operations upon variables where this is not true.

f. The language must, of course, be logically consistent and not equipped with built-in possibility for ambiguity.

g. Changes in the language should not require relearning or re-programming, rather they should come as easily-learned additions to available experience.

2. The *language,* to be *usable,* must be easily transliterated into an equivalent form for which a *translator* (compiler) exists to produce a machine-coded object program.

As *corollaries* to this basic objective, we might list the following:

a. Symbols used in the basic language should have 1:1 equivalents.

b. No implied or explicitly-stated operations should be included in the language if there are no reasonable methods available for implementing them.

3. The translators for the language (and thus the language itself) cannot afford to lose sight of *economics*. Machine time represents a cost (or the expenditure of a resource), and thus the translators and object program produced should use a *minimal* amount of machine time, consistent with the frequency of their use, i.e., while there is no virtue in making efficiency the *only* goal, there is no payoff in producing bad code, if minor modification can produce good code. A second item in this question of economics might be the *cost* of programming the translator itself, and maintaining it.

4. No *language* can or should expect to remain unchanged for the indefinite future. Initial approaches to such a language are bound to evolve in order to meet the objectives stated above. Such changes as are *minor* should be allowed for, but *major* changes must not be legislated lightly. I.e., again there must be adequate cause for making major changes. A "major" change is defined here as a change wich requires a large amount of re-education on the part of the user, or a large amount of re-programming for the translators.

A valid opinion on this topic might be the observation that languages of all types, even those used in science and engineering, *evolve* both laterally and vertically (in the direction of more capability and also more compactness), and that historically even the languages of differing fields of science tend to fragment and become specialized for the specific needs of a given field, rather than becoming broader to include all fields.

It is in the context of these objectives that I should like to discuss ALGOL, so that my opinions can at least be traced to a set of objectives, and the objectives themselves can be a basis for discussion.

To an outsider, not involved in the development of ALGOL, it would appear that in the early, "classical" stages of ALGOL, (i.e., ALGOL '58) the above listed objectives were in the minds of the originators, but in the "rococo" stage (ALGOL '60), they became lost or obscured. It would probably be easier at this point to discuss the ALGOLS relative to FORTRAN in order to make the points more clearly. Parenthetically, I should add that by the above objectives, I do not consider either language as very "good" or "bad," merely somewhat different.

Since a large number of computer users are moderately familiar with FORTRAN, and most have followed ALGOL from a respectful distance, it might be wise to discuss ALGOL as it compares to FORTRAN with respect to the aforementioned objectives.

Objective 1a. — **acceptance**

FORTRAN is cerainly more widely accepted as a de-facto standard for an algebraic language than ALGOL. This is, of course, not true with respect to areas not thorougly infiltrated by "the Collossus" and leaves many users on the outside looking in, and some manufacturers with hardware on their shelves. ALGOL, while widely discussed in the ACM journals and in Europe does not seem to have achieved the acceptance among the rank and file users that the ACM is assuming. ALGOL "algorithms" are nevertheless being published in the ACM *Communications*. While part of the acceptance question is due to inertia, lack of motive, and the fact that FORTRAN came first, a large role was played by the way in which ALGOL itself was introduced.

Objective 1b. — **Operations**

FORTRAN allows for the usual arithmetic operations plus such functions as exponentiation as part of the basic language for the computation of a variable in a statement. Other functions are handled by special identification of the function name (an "F" after the name). The variables in FORTRAN may be arrayed up to three dimensions, and may be integer or floating point. FORTRAN allows for iteration by counting ("DO statements"); and one type of conditional branch (the "IF" statement for testing negative, positive, or zero expressions). FORTRAN also allows for card, magnetic tape, and printer I/O utilizing the somewhat rigid character set and formats of these media. Finally, FORTRAN allows for the inclusion of subroutines, either in FORTRAN or machine language.

It is in this area that ALGOL clearly scores highest. It allows all of the capability of FORTRAN, but in addition, allows for Boolean variables, more freedom in mixing the modes of variables within expressions, higher dimensionality on arrays, and a far wider class of conditional expressions and functions, allowing their free use anywhere in an arithmetic expression. Because of the way in which the "mode" of variables are declared, the language itself has the clear capability of being expanded, whereas the mechanism used in FORTRAN (the initial letter of a variable) is limited.

ALGOL allows functions to use themselves as arguments (recursion) of which more will be said later. Neither language handles symbolic manipulations with any ease, and machine code or special-purpose language is thus preferable for non-numerical computations.

This by no means is a complete list of the virtues of ALGOL over FORTRAN in this area. It might, however, be noted that there is no operation in ALGOL that cannot be carried out in FORTRAN, at the expense of more steps, and neither language goes beyond the specification of algebraic procedures. ALGOL, however, has the major defect of completely ignoring I/O and thus any form of intermediate (tape or disc) storage.

Objective 1c. — **Psychological Match — Readability**

FORTRAN was obviously designed around unit records (card input) whereas ALGOL was designed for continuous input (tape). Thus FORTRAN must use one line per statement, whereas ALGOL *can* use a line, but must use a semicolon (since line skips and spaces have no meaning in the language). Publication ALGOL uses a wider character set for operations than FORTRAN could allow itself, and thus, ALGOL expressions *can* be more readable. Both languages are, however, still constrained to a one dimensional string of symbols (and thus superscripts, subscripts, and denominator factors have to be handled in ways other than location above or below a line).

ALGOL also considers a string of expressions as a single expression, utilizing the symbols "begin" and "end" to "delimit" the expression. In the case of nested expressions or iterations, it can become difficult to keep track of the nestings. FORTRAN uses the handier dodge of labeling statements by number, and thus making the nesting much more apparent. Since there is ample psychological and linguistic evidence that there is a limit of about seven items than can be kept in the human mind at any time*, the general practice of utilizing unlimited numbers of parentheses, and begin-end delimiters is highly suspect. It does not appear that any "natural" language (including ordinary mathematics) has ignored this constraint.

One other issue is the question of how easy it is to learn or teach ALGOL vs. FORTRAN. Despite the impression that may come from the approved ALGOL write-ups, or IBM manuals, both languages are equivalently easy to learn, and having learned one, it is relatively easy to

*See "A Model and an Hypothesis for Language Structure." V. Yngve, Proceedings of Am. Phil. Society, October 1960.

pick up the second. But, between learning a language and fully understanding its quirks, there is a wide gulf, and ALGOL in any machine version is likely to have as many idiosyncrasies as FORTRAN.

Objective 1d. — **Proneness to Error**
FORTRAN itself is highly error prone, and although it may be a simple process to write a correct procedure in the language, the existence of such pitfalls may lead to many tries before a result is in hand. Among these pitfalls are the use of prefix and suffix letters to indicate modes of variables and functions, respectively. This, coupled with a six letter maximum for variables, restricts the choice of names for variables. Since the designers' choice of FORTRAN also assumed that integers should not exceed memory size, the full range of integer variables is highly truncated, and in fact, the *order* of computation for integers can become highly important. (A non-zero expression can become zero with ease.)

The use of format statements in FORTRAN is also a prime source of unnecessary error. ALGOL, on the other hand, has none of the above objections, but its readability can lead to other types of error, and since it ignores I/O completely, it cannot even be compared in this respect.

Objective 1e. — **Range of Variables** (mode)
As has been stated, FORTRAN has only two modes with no provision for more. ALGOL does have three, and *if* the language were to be considered expandable, does have a simple mechanism for more.

Objective 1f. — **Logical Consistency**
FORTRAN is logically consistent to a great extent at the expense of requiring annoying conventions. ALGOL seems to be overly consistent. The stress on "syntactical" definition, the treatment of the language consistently as one long symbol string, delimited by parentheses, or special word "symbols" all speaks to an intensively thought-out logical construction. There is, however, no meta-language for specifying the *implications* of this logical consistency as will be considered under objective 2.

Objective 1g. — **Change**
Change in a language can be a double edged sword, pariculary if the changes are major, somewhat inexplicable, and timed wrong. (See Pavlov's research on dogs.) FORTRAN can hardly be accused of rapid or drastic changes. Those changes that have been made have been "compatible" to such an extent that they haven't accomplished a great deal. The two year hiatus between ALGOL '58 and ALGOL '60 was in fact marked by a great deal of progress and work. ALGOL '60, however, implied such a sweeping set of changes that shock, followed by apathy resulted. The major changes of recursion, dynamic storage allocation, etc., accompanied by a far more truculent attitude with respect to compliance, universality, and timelessness, (i.e., the end of the "let many flowers bloom" policy), seems to be mainly responsible for the suspended animation of the language with all of its virtues.

Objective 2a. — **Existence of Translator, Symbol Set**
Although FORTRAN was billed as a "machine independent" language, it was clearly written with the limitations of the 700 series machines in mind. The publication language of ALGOL (which has been considered as synonymous with all machine realizations) clearly is written with no machine limitations of any sort in mind. For example, variables or constants may be indicated by symbol strings of *any length*. To mechanize this feature alone, in any translator is going to be difficult, and the inclusion of unbounded number strings is clearly at variance with the normal, fixed precision (or fixed number or significant figures) available in *any* machine. Double, triple, or n-tuple precision routines are still dealing with fixed length numbers.

ALGOL also uses a very large symbol set, that is *not* going to appear on new machines overnight. Therefore, transliteration is necessary, and should have been allowed for in an orderly way. Finally, in ALGOL, all symbols are *not* represented by single characters—some 30-odd *words*, such as "begin," "end," "array," "do," which while printed in bold face type for publication, are going to have to be recognized as a single symbol by any translator. Presumably, then the translator will have to distinguish by context (a time consuming feat) beween the appearance of any of these words or their inadvertant use as a symbol string in naming some other variable.

Objective 2b. — **Existence of Translator — Difficult Operations**
FORTRAN exists as a translator. ALGOL '60 does not. There are in fact many features of ALGOL '60 for which no methods exist. For example, ALGOL *implies* that arrayed variables need only be declared as such with *no* information as to the size of the array or clue as to ordering for multidimensional data. While this problem can be classed as "dynamic storage allocation," no reasonably efficient methods exist for such allocation. As has been stated before, the non-existence of any form of I/O rules out all but core storage of finite extent.

Finally, there are features in ALGOL, such as recursive use of functions, which if allowed for will inevitably result in both a time consuming compilation and a slow running program; high prices to pay for a feature of dubious merit in the context of numerical or logical computation. (If ALGOL allowed for symbolic manipulation, there would be a better reason for having this feature.) The fact that special-purpose machines can be designed to handle recursion easily is not germane to the issue of whether this feature is needed for ALGOL per se.

Leaving aside for the moment a discussion of dialects of ALGOL, there can be no discussion at this point of what a *pure* ALGOL translator *can* be in terms of its own efficiency or of the efficiency of the program it produces. No one seems to know how to solve the problems that are *implied* by ALGOL's features.

Objective 3. — **Economics**
Pure ALGOL translators do not exist, FORTRAN does, and in the area of economics, the standard version of FORTRAN is no prize package.

FORTRAN, particularly when embedded in standard operating systems, can be a horribly time consuming compiler. One minute, on a 7090 to compile and run the single operation of two times two is hardly a high water mark to point at with pride—particularly, on a machine with a 2-microsecond memory access time.

There is no easy figure of merit to point at with respect to the balance between compile, run, and debug times, and much of the existing data is influenced by somewhat error-prone compilers which inflate the percentage on the side of compilation.

It should not, however, be declassé to suggest that machine time is valuable, without at the same time, implying that the programmers' time is not. Both are important, and the cardinal engineering virtue of not using a 16-inch gun to swat a mosquito can still apply, even if some trade-offs are needed.

Finally, there is the issue of the investment of human and machine time to produce an acceptable translator. It should again be taken as realism to expect that an overly-complicated task is going to take longer to write, check out, and debug. Trade-offs, in symbolism and conventions, if they can make the job easier, may be worthwhile.

Objective 4. — **Changes**

We have already commented on the change between ALGOL '58 and ALGOL '60 and implied an effect. It should, however, be evident that the computer business, if we allow it to do so, has a far greater impact to make on our intellectual habits. To do so, it is felt in some quarters, better problem descriptive languages will be needed, as will newer devices, such as graphical inputs and outputs with close human interaction.

For example, some types of symbol manipulation and numerical work (integration, algebraic manipulation with complex as well as real numbers, etc.) can almost, as of today, be handled by machine, and with the proper languages (such as GM's DYANA, Bell Lab's BLODI, etc.) can be utilized directly.

These and other higher level languages need some standard, algebraic language into which they can compile. Would it not make more sense in the long run to settle on a reasonable standard for ALGOL, encompassing those features which are within the state of the art, and while allowing provisions for some growth at the ALGOL level, swearing off for the moment from features and objectives which are out of bounds of what is presently feasible?

So much for my objectives, now let me summarize my feelings with respect to the current situation of ALGOL and what might be done with it.

I think that from the foregoing set of objectives, it can be seen that I am very much in favor of improvement in algebraic language, and definitely not for the status quo.

Now, at present, it seems as if there are at least five major camps on the ALGOL question:

1. There is the committee that set up ALGOL, accompanied by many eminent people in the computing profession, whose attitude can be summarized as "Adopt ALGOL Now," and purge all other obsolete languages. This group is also apparently serving as a board of review to decide when a language is or is not ALGOL.

2. There are the compiler writers who periodically are producing translators which are billed as "ALGOL," "Dialects of ALGOL," "ALGOL-like" languages or non-ALGOL "Algebraic Languages."

3. There are those who are working on problems for which ALGOL is either *not* the best language, or at best, it might be used as an intermediate language.

4. There is the bulk of the computing fraternity who have no strong bias, are content to use what is available, but wish the dust would settle.

5. There are those who are violently anti-ALGOL, possibly because of a heavy investment in some other translator; or because of a reaction to the way ALGOL has been introduced; or because of ignorance.

The first two groups it would appear hold the key to resolving the situation. The first group by making a few changes in ground rules, and the second by getting to work.

Let me explain what I mean here by referring to two particular "ALGOL-like" processors: the "MAD" language of Michigan, and the ALGOL processor of Duke University, because it would appear that these are highly typical of what can be achieved, as well as the pitfalls in acceptance.

"MAD" is a language which is not being accepted as ALGOL, though it is largely patterned on ALGOL '58, and provides for *some* of the provisions of ALGOL '60.

The major difference appears to be primarily in the area of transliteration of symbols, primarily the "words" which ALGOL defines as single symbols. This difference is mainly dictated on the basis of the trade-offs necessary to produce a fast compiler. All of the "symbol words" in MAD are longer than six characters, while all of the function and variable words are six or less. Thus, "if" becomes "whenever," "step" becomes "through," "do" becomes "execute," etc. Since MAD is meant to be punched on cards, one statement per card, there is no need for a semicolon delimiter, since it is implied. The other major difference is in the "begin-end" symbology of ALGOL which becomes for procedures: "internal function," and "end of function." For iterations the delimiting in MAD is handled by the device of labeling the last statement to be executed with a name, and referring to it by name in the "through *name*" statement. Functions are identified as such by a terminal period ".", and the inequality operators $=$, $\geqslant$, $<$, etc., are identified by a string: ".E.", ".GE.", ".L.", etc. Since MAD is an existing translator, it could *not* ignore I/O, and has a full set of tape and off-line I/O commands. It *allows* for recursion and list processing, and all of the operations of ALGOL with respect to multi-dimensioned arrays, conditional expressions, and modes of variables.

It is small, fast, and amenable to future change, yet it is condemned as not "being" ALGOL. On the other hand, we have an article in the June issue of DATAMATION, "ALGOL at Duke" which describes a language even less "ALGOL-like" than MAD; openly billed, described, and apparently accepted as ALGOL.

Yet it does not allow "recursion," "parameters called by name," "variable array bounds," "switches," etc. Because of a limited character set, Duke has done much transliterating using dollar signs, etc. In fact, the program (nicely indented) which they compare to a FORTRAN (poorly formatted) version on Page 34 is *not* ALGOL (or is incorrect ALGOL) and is certainly not markedly superior, as is implied.

To nit pick the same example for a moment: ALGOL merely requires arrayed variables to be declared as such, not given bounds of size; the arrayed variable "A" is never declared as "real," the integers I and J should have been declared as "integer;" there is no "write" statement in ALGOL (and the FORTRAN version "punches" anyhow), and the compiler does not know the users' intentions with respect to format.

This is not at all intended to pick a dispute with Duke, for it appears as if they too are making their own set of modifications (as anyone must) in order to come up with a workable version of an ALGOL translator.

Now let me come to the point of this article. I should like to recommend that the originators of ALGOL have themselves another meeting, with or without their European colleagues, and loosen up their definitions to such an extent that languages, such as Duke's ALGOL and MAD, can legitimately be considered as acceptable ALGOL.

Specifically, this would seem to involve:

1. A more liberal attitude toward *transliteration* (if a word is to be considered as a single symbol, then the choice of words can after all, be dictated by other reasons such as efficiency of compilation).

2. Some leeway on the begin-end convention to allow for more readability (i.e., labels).

3. A workable set of I/O statements, recognizing the existence of tapes, cards, and printers.

4. Removal of dynamic storage allocation and recursive procedures as *necessary* parts of the language, and instead allowing for their provision, if possible.

5. Stop fanning a totally unnecessary controversy, and let it cool down.

Computers and computation hold within them the promise for future advances if we do not succumb to needless debate on the number of angels that can sit on the head of a pin, or the present "loyalty oaths" to various languages. It is in this sense and spirit that I feel we should settle ALGOL and move to more vital problems. ■

UCLA & WDPC

eight megabucks of IBM affection

by IRWIN SCHORR, Assistant Editor

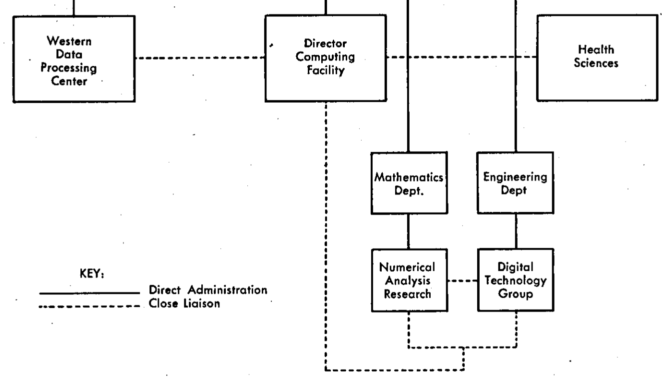
While there are detractors who maintain that the Western Data Processing Center at the University of California, Los Angeles, is "IBM's West Coast Showroom," this fact is hardly of major concern to WDPC management who are responsible for a major computing effort, involving the participation of 73 western schools in WDPC.

The current keystone of UCLA's computing efforts is the 7090, which, while physically located at the WDPC (which is heavily supported by IBM) is owned by the university, and administered by the university's Computing Facility. Responsibility for machine usage is divided into two parts: WDPC's concern is limited to problems generated by its participants, and for business research problems. All scientific and other campus-originated computing at UCLA comes under the purview of the Computing Facility, an inter-departmental organization reporting directly to the vice-chancellor of UCLA.

These lines of subordination will be rewritten when the WDPC, the Computing Facility, and the UCLA Medical Center, will each operate its own large-scale equipment. This fall, the Medical Center will install an IBM 7094 and 1410, and in March, 1963, the 7090 at the WDPC will be moved to the Computing Facility, while the WDPC will put a 7094 into operation. The total value of hardware on the UCLA campus will be over eight megabucks.

At present, to help defray the cost of the 7090, the Computing Facility sells machine time to IBM, who in turn donates most of the time to the WDPC; the bulk of the remaining IBM time is devoted to applied programming. One half of the machine time available to WDPC — a minimum of five hours daily — is used for jobs originating from participants, and the remainder to business research problems.

While intra-university cooperation is evident at WDPC, the fact that the university is the owner of the 90 has led WDPC director George W. Brown to observe that the mutual accomodation is a rather unusual relationship. This association extends to the utilization of portions of the 90 configuration. For example, the university owns two data

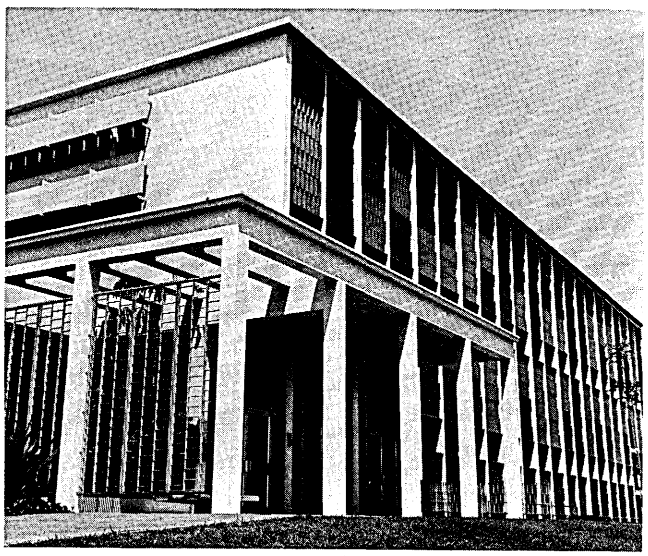


channels and eight 729-IV tape unit of the overall configuration of four data channels and 20 tape units. However, the Computing Facility is free to use the entire combination, and does so.

The annual operating budget for operation of the WDPC is covered by IBM and UCLA, while some additional financial support is provided through a Ford Foundation grant, administered by the Western Management Science Institute, Graduate School of Business Administration. While IBM tells WDPC what equipment will be installed, WDPC determines what it will do with the equipment, with the aid of advisory committees.

Under the terms of the original agreement entered into by IBM and UCLA in 1956, the Center's equipment is supplied and serviced by IBM, operating costs are shared, the equipment is available for use by UCLA and participating institutions at least five hours each working day, and available machine time is divided equally between UCLA and participating institutions. Research and educational activities are carried on without charge, and the agreement also stipulates that the Center may not undertake service activities for business and industry.

Since the Center's function is strictly for educational pursuits, WDPC is a great boon for the independent investigator without a budget, Dr. Brown states. Of the 73 participants, about half are consistent users. Even so, WDPC has what Dr. Brown calls a safety valve—a policy of never giving any participant a commitment for proposal purposes, nor will WDPC sign an agreement to process any particular job.



Formally dedicated in January, 1959, the Western Data Processing Center provides 25,000 sq. ft. of space for computing equipment, classrooms, conference rooms, offices, and a library.

Productivity of the 90 is dependent on the use of a monitor system, when the load consists mainly of small jobs. In a five-hour period, some 50 or so jobs falling in this category can be processed.

Users from UCLA and nearby participating institutions generally discuss their projects and programs with WDPC program consultants, while users from more remote schools submit their jobs by mail. They can usually obtain advice from either the WDPC representative at their school or by mail from a WDPC consultant.

Many users travel to the Center to conduct all or part of their research. At the Center, the library, educational and consultation services are available, in addition to programming manuals and office space.

Administratively, the WDPC is a division of the Graduate School of Business Administration, and is not a teaching unit of the university. In this regard, Dr. Brown's small staff provides counsel. Although WDPC doesn't program for its members, Dr. Brown says that he and his staff try to educate the member schools by providing consultation service, with the ultimate goal of having people help themselves.

Several non-credit courses in data processing are regularly offered. These include a one-day course in Beginner FORTRAN Programming, and longer Advanced FORTRAN Programming Classes. For the beginner class, a programmed text, "Computer Language: An Auto-Instructional Introduction to FORTRAN," by Colman and Smallwood (McGraw-Hill Book Co.) will be used when the book is published this fall. Participating schools will also use this material, which is based on the Skinner teaching machine method.

A variety of publications has been prepared by WDPC, including a Users Manual; FAP (FORTRAN Assembly Program) Reference Manual, and Program Write-Ups. The latter includes FAP Buffered I/O Subroutines; Correlation Analysis Program (WDCORR); Questionnaire Analysis Program 4 (QUAP 4); BIMD 01 through BIMD 26, and QUAP Key Punching Data Form. The BIMDs were prepared by the Department of Preventative Medicine and Public Health, and QUAP by John Whittelsey, Psychiatry Department. WDPC participated in the preparation of these programs.

Four data channel consoles (right) are part of the 7090 configuration which includes 20 729-IV tape units.

Current and future projects include improving the current FORTRAN Monitor System; preparing for IBM COBOL; selecting and installing a set of linear programming systems; investigating the SPS-1 Simulator Compiler; and research on multi-programming.

Also under consideration is a microwave link between the three campus computing centers. Recently, data transmission facilities were installed between the WDPC and some of the participants.

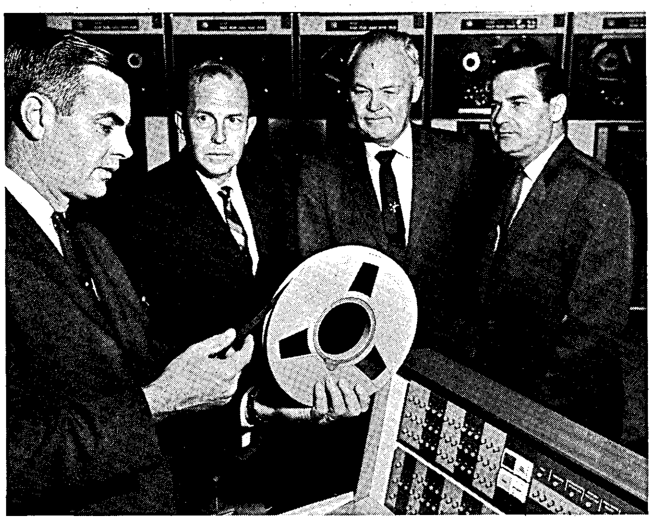
the computing facility

Unlike the WDPC, which operates under clearly defined financial terms, the Computing Facility carries on its extensive task of furnishing computer time for university research projects and data processing education without a budget. For this reason director Charles B. Tompkins says the Facility is "highly interdisciplinary – and we know exactly what we want to accomplish. The objective of the Computing Facility includes the encouragement of people to learn computing sciences – without electrocuting themselves!"

Operating with alternate periods daily of closed and open shop, and extensive open shop runs on week-ends, the Computing Facility will not accept every problem that a sponsor may want to put on the machine. Each job is carefully screened by an advisory committee of scientists to determine whether the problem fits the computer, and whether the job actually should be run on the Facility's equipment. (A recent problem was estimated to require a thousand hours of machine time. It was returned to the researcher who was advised to reprogram the problem a little more judiciously.)

To support the Computing Facility, users are charged for machine time if their research projects are aided by grants. If there are not outside grants, the university department in which the research is being conducted is billed for the time used. (The exception to this is the arrangement where IBM buys time for the WDPC.)

In addition to the 7090, the Facility operates SWAC, built a decade ago by the National Bureau of Standards, and a 1401. One piece of equipment, which might be classified as a "computing curiosity," is an IBM 797, an electronic version of the CPC, with 1K core storage. Although the 797 is the property of the Engineering Department and has no administrative connection with the Computing Facility, Dr. Tompkins observes that the machine, which came as a "gift" from IBM, is used by some for informal "puttering."



Leonard E. Clark (left), VP and western region manager of IBM's Data Processing Div., describes the 7090 system to (left to right) Franklin D. Murphy, Chancellor of UCLA; Magnus R. Hestenes, Professor of Mathematics, UCLA, and Dr. George W. Brown, Director, Western Data Processing Center.

A project headed by Dr. Gerald Estrin, in charge of the Digital Technology Group of the Engineering Department, is underway to develop a variable logic computer. When completed, the computer will be used by the Computing Facility. Since the acquisition of the 7090, some of the work in Numerical Analysis Research, such as language study, has been taken over by the Computing Facility. Both the Digital Technology Group and N.A.R. have strong liaison with the Computing Facility, but there is no administrative connection.

About 80% of the jobs processed by the Facility are written in a modified FORTRAN, with the remainder in FAP. "FORTRAN is quite easy to learn," remarks Dr. Tompkins, "So we let WDPC do the actual instruction. We do, however, teach FAP at the Facility, so our users can make more efficient use of the equipment."

The Facility's full-time staff numbers 16 at present, and each member is expected to be a "jack-of-all-trades – a progrommer, operator, and at times, a repairer." It is felt that future staffers should be drawn from the ranks of graduate students, as "outsiders" tend to suffer from what was described as a lack of versatility.

In the area of computer education, there are 20 classes devoted to numerical analysis and computer programming and design, on both the undergraduate and graduate levels. The Computing Facility also lends support to UCLA's Computer Club, which claims about 200 members.

the medical center

"The research activities of the Medical Center have grown so rapidly," reports Dr. Will Dixon, director of the Computing Group of the Health Sciences Department, "that computing requirements have overtaxed our existing hardware."

The hardware that Dr. Dixon refers to consists of a CDC 160A (the only non-IBM machine at UCLA used for major research), utilized by the Brain Research Institute, and as a participant in the WDPC, the Institute also uses time on the 7090. But giving credit where due, Dr. Dixon attributes the development of the Medical Center's computing activities through the availability of the WDPC's facilities.

The 7090 system at the Western Data Processing Center will be replaced by a 7094 in March, 1963, while the Medical Center will install its own 7094 in the Fall of 1962.

With the acquisition of large-scale equipment, the Medical Center will undertake more extensive research projects without facing the handicap of the comparatively limited time that would have been made available to them on the 90. The new 7094 system will not completely overshadow the 160A, but rather will enable researchers to utilize the 160A to better advantage.

One project contemplated involves on-line recording of physiological data directly to the 160A, where the information, on mag tape, will be converted from analog to digital data, and then be further processed on the 7094.

Major research efforts will be directed in the field of information retrieval, and with the faster speed of the 7094, expanded projects centering around pathology and radiology will be facilitated. ■

The results of a private survey of computer installations with respect to utilization of programmer's time are given in Table 1. Only the uninitiated will be surprised that two items, "Preparing Demonstrations" and "Inventing Acronyms" take up almost fifty percent of the average programmer's time. What is surprising is that so little effort has been expended to "Automate" these areas. The other areas (with the exception of "Analysis," "Flow Diagramming" and "Testing," which have been rightfully neglected because nobody wastes time on them anyway) have been the subject of much research and development work. This paper, then, proposes a system which strikes at the core of these two neglected problems.

with painful ease

HOW TO AUTOMATE DEMONSTRATIONS

by G. M. WEINBERG, IBM Systems Research Institute, New York City

Everyone knows the importance of demonstrations. There comes a point in the life of every programming project when it must produce a dazzling demonstration or suffer the agonizing death by drying of the money glands. What few project managers seem to know, however, is that the odds against producing a true demonstration of the system are thousands to one. The wastage of time comes, then, from *attempting* to make a real demonstration, when the end result is inevitably a phony demonstration rigged up hastily — and poorly — in the final few hours.

The argument that the overall project is aided by the attempt to make a real demonstration is patently fallacious. The most knowledgeable programmers on the project must always be used, thus halting all current progress, not to speak of the convalescent period. What we want, then, is a way of producing really good, phony demonstrations using the least skilled trainee programmers in the shop. For this purpose, I propose a *General Purpose Demonstration Generator.*

There are two parts to the Demonstration Generator: the language and the compiler. Since the compiler is machine-dependent, we will not discuss it here except to point out that one machine may compile demonstrations for another — a handy feature when the demonstration machine is not in very good shape and may not hold up through a compilation *and* a demonstration.

Table 1
Breakdown of Programmer Activity

Analysis	.7	
Flow Diagramming	1.2	
Coding	6.3	
Testing	15.4	
Documentation	11.8	(seems like 91.8)
Preparing Demonstrations	31.2	
Inventing Acronyms	16.8	
Non-programming Activities	14.2	
	97.6*	

*The figures do not total 100% because there seems to be a bug in the tabulation program.

The language is machine independent; though, of course, those statements which call for specific peripheral devices may only be used on configurations which contain those devices. One can hardly hope to give a good demonstration without an adequate supply of peripheral devices. Unfortunately, this rule is often overlooked in specifying machine configurations. The Demonstration Generator, however, will always give the best possible demonstration with the available equipment, and, under sense switch control, will give a priority list of additional devices which, if ordered, will surely enhance the demonstration.

The language consists of a number of basic statements, together with their modifiers, and the modifiers of the modifiers. The statements are described below.

INPUT D

The INPUT statement tells the compiler that there will be input on device D. If there is more than one source of input, several may be listed consecutively, separated by commas. No other specification is needed, as the object program will not actually use any of the input data and will set the sequence of input so as to harmonize with the rest of the demonstration. (NOTE: Just in case there is a sophisticated executive in the audience, you can rest assured that the object program will always read in at least one input before any output is generated.)

Example: INPUT CARD READER, TYPEWRITER

OUTPUT N, D, R(r)
list

The OUTPUT statement specifies how many lines of output are desired (n) on device D during the demonstration. R specifies the rhythm at which the output is to be written and may take the values RANDOM, INTERMITTENT, SPASMODIC, or METER (r). When METER is chosen, the modifier, r, enclosed in parentheses, selects one of a number of popular meters built into the system. Standard values of r are WALTZ, FOX TROT, ROCK-N-ROLL, TWIST, GAVOTTE, MINUET, and, for the Department of Defense, MARCH. Additional meters may be added to the compiler's repertoire to suit individual executive's taste.

The "list" may be any number of lines long and is simply the literal output wanted in the course of the demonstration. If a great deal of output is desired and the programmer wishes to save the labor of writing it all, the list may consist of only a few representative lines. The object program will print these lines first, and then print additional authentic-looking random variations of them until the specified number (n) of lines has been printed.

Example:

OUTPUT 100, PRINTER, METER (FOX TROT)
+3.97672 +8.53491 −6.12385 +8.81837

SPIN TAPE n, R(r)

SPIN TAPE will cause the object program to move n tapes in an impressive manner. R(r) specifies the meter, as described under OUTPUT. To put several tapes in motion with different metric patterns, more than one SPIN TAPE may be written, and the object program will, to the best of its ability, integrate their rhythms. Example:

SPINTAPE 2, RANDOM
SPINTAPE 3, SPASMODIC
SPINTAPE 2, METER (WALTZ)

This sequence will move seven tapes in a delightful pattern.

FLASH CONSOLE n, R(r)

The FLASH CONSOLE statement has the same parameters as the SPIN TAPE statement, but naturally refers to the twinkling of the console lights. Although most machines have only one console, the parameter, n, provides for the possibility of additional ones. These may be pseudo-consoles, obtained by a minor modification of the compiler which allows defining separate parts of the console as individual consoles.

Example:

FLASH CONSOLE 1, INTERMITTENT
FLASH CONSOLE 1, GAVOTTE

will send each half of the console off on a separate gyration, pleasing to the eye and puzzling to the brain.

MESSAGE T

No demonstration is really complete without a few messages being typed out on an on-line typewriter. Nothing else but that one character at a time revelation quite gives such a feeling that the machine is trying to tell *you* something, thereby enhancing that secret, unutterable feeling that there *is* somebody in there — really. The MESSAGE statement is written once for each message the programmer desires to have appear during the demonstration. The parameter T specifies the tone of the messages, which will be taken from a carefully pretested repertoire. The standard tones available with the compiler are listed below, with examples.

BUSINESSLIKE:	"All summary totals zero balance to batch adjusted net figures."
HUMOROUS:	"Please move away from the typewriter so those people in back can see."
DRAMATIC:	"Program has just completed Pass 1A, 2.2 milliseconds ahead of deadline. Program will now attempt Pass 2x, if you are willing."
ESOTERIC:	"The recursive algorithm was preempted on the n(j)th iteration by an error probability signal from the timing ring. Index registers contain X$**)(,AXZ—$$."

These four have been found to be most popular, but should you have an executive whose tastes run to GRUESOME or SEXY, for example, others may be added to the compiler.

One special additional parameter is PERSONAL. The statement

MESSAGE PERSONAL

followed by a comma followed by somebodies' name will print out a personal message to that person. Nothing will soften up a hardened executive faster than a nice

MESSAGE PERSONAL, J.P.

SPECIAL F(T)

Many machines come equipped with hardware features which may be used to add special flavor to a demonstration. By using the SPECIAL statement and specifying (F) the feature available, the programmer may use this device in his demonstration, modified by an appropriate tone. Features built into the compiler are as follows:

STILL PICTURE — this feature may be used on any machine with a printer, but is far more effective when an on-line plotting device is available. All of the standard tones (see MESSAGE) are available. (NOTE: If you have a touchy executive, you should avoid using a MESSAGE PERSONAL in the same program as a STILL PICTURE HUMOROUS, for you may get out a picture of Alfred E. Newman with the executive's name under it.)

MOTION PICTURE — When a cathode ray tube output is available, MOTION PICTURE will produce a scenario in the requested tone. (NOTE: It was the initial tests of this statement which forced the decision to remove SEXY from the set of standard tones. The user who wishes to replace it does so at his own risk.)

MUSIC — If some sort of sound generator is available, all sorts of musical effects may be attained through the use of MUSIC with appropriate modifiers. Both the standard tone and meter modifiers are available, written, for example, in the form

SPECIAL MUSIC BUSINESSLIKE (TWIST)

COBOL A

As everyone knows, executives have a burning desire to read programs. COBOL was invented to give them the impression that they know what this computer business is all about, without of course, actually doing so. This represents a step in the right direction, but since we have seen that real demonstrations are a waste of time, we know that a real program listing is equally redundant. The COBOL statement causes the demonstration to begin with a printout of a genuine phony COBOL program which looks to any executive like the application specified by A. Thus the statement

COBOL PAYROLL

will produce a payroll-looking COBOL program.

For demonstrations of *integrated* data processing, several A's may be used, separated by commas. For example,

COBOL BILLING, ACCOUNTS RECEIVABLE, SHIPPING, INVENTORY, ORDERING, ACCOUNTS PAYABLE, MANAGEMENT INFORMATION SYSTEM

New A's may be added to the compiler by supplying a list of O.K. words plus at least one formula appropriate to that application.

ACRONYM P_1, P_2, P_3, etc.

The ACRONYM statement attacks that 16.8 percent of programmer time spent trying to pick system names (a "system" is merely a program requiring an "S" in its acronym). The importance of program names is not to be underestimated, for the program's name is not only a catchword which will cement your project in the public mind but a sort of continuing demonstration of the originator's genius (e.g. SAP). Therefore, an important part of any demonstration is the effect of the program name on the audience, so the inclusion of the ACRONYM statement in the Demonstration Generator is amply justified.

ACRONYM has two modes: synthetic and analytic. The analytic mode is distinguished from the synthetic mode by the presence of a single — as opposed to multiple — parameter, P_1. In the analytic mode, P_1 is the literal name you wish to give the program, for which the demonstration generator will furnish suitable "nyms" whose "acros" will form the desired name.

Example: The statement

ACRONYM ASTRONAUT

yielded the following ouput from a test version of the system:

ASTRONAUT: *A* *S*ystem *T*o *R*eplace *O*ld *N*avigational *A*nd *U*tility *T*ables

ACRONYM can be integrated with payroll accounting so as to seek out appropriately initialed employees who will then become systems programmers. For example:

ACRONYM ANALYSIS

yielded in a test:

*A*rthur *N*ussbaum's *A*lgorithmic *L*anguage for *Y*esterday's *S*emi-*I*nterpretive *S*ystem

plus a payroll change card for lucky Arthur.

In the synthetic mode, the parameters P_1 . . . . P_n are n words to be included in your acronym. The compiler will attempt to compose an acronym using all and only these words, but failing this, will add extra words (including names if integrated with payroll) as necessary to fill out a desirable acronym. For example,

ACRONYM SYSTEM, NAVIGATIONAL, UTILITY, TABLE

yielded

NUTS: *N*avigational *U*tility *T*ables *S*ystem

Occasionally, the generator may produce a word which is unsatisfactory for some reason. By pressing START twice in rapid succession after the first name is produced, you will cause the computer to choose a new name. Following this procedure in the previous example yielded

DONUTS: Demonstration of Navigational Utility Tables System and a subsequent try gave

YOURENUTS: Yves Own Uncontrolled Random Experiments on Navigational Utility Table System.

(NOTE: A special feature is available which scans all existing computer program acronyms to avoid duplications. This feature, however, requires at least 10^7 characters of random access storage.)

GAME, N

One of the more popular forms of demonstration is the game, because of the feeling of participation it is supposed to impart to the spectators. Executives, however, never really comprehend games like Nim or 3-dimensional tic-tac-toe, but must pretend to do so during the demonstration. Thus parameters specifying the game are superfluous, and the only parameter necessary is N, specifying the name of the highest ranking executive present — who naturally will be the only one to beat the machine at the random game produced by the compiler.

END n, K

One of the most frequent mistakes of inexperienced demonstration writers is failing to fit the demonstration into the busy schedule of the executive's tour. A second error is producing a demonstration which more or less dribbles to an end, whereas a good demonstration must always end on the upbeat. The END statement solves both of these problems. The parameter n specifies the time, in seconds, which the demonstration will take, while K specifies the kind of ending desired. Values of K built into the compiler are STATISTICAL — which provides an awesome array of pseudo-statistics about the job — CHECKLIST — which types out a meaningful-looking set of check point conditions, each followed by the symbols AOK — and PATRIOTIC — which, prints a picture of the American flag and, if MUSIC is available — plays the "Star-Spangled Banner" (in Britain, the Union Jack and "God Save the Queen"). The PATRIOTIC ending has the advantages of getting all spectators on their feet and ready to herd out the door before questions arise.

FALSE START n

Any danger that someone will suspect the phony demonstration is eliminated by the FALSE START statement. No real demonstration ever runs without a hitch, and FALSE START insures that phony hitches (n of them) will be included in the phony object program to give the realism you need. Do not be alarmed at anything that happens when the program stops (though you must *look* alarmed), for all symptoms of malfunction are as meaningless as the normal operation. You may make whatever adjustments to switch settings, input decks, tape positioning, and so forth that you feel are needed to convince the audience of the depth of your understanding and mastery of the program, secure in the knowledge that none of these things have any effect on the demonstration. When you have finished, press the START button. After n depressions of this button (with intervening ritual to taste) the demonstration will proceed in the desired manner. (NOTE: The object program will deduct the false start time from the desired running time, so the schedule will not be interrupted. Be careful not to hog the whole show, however; give the computer a chance.) ■

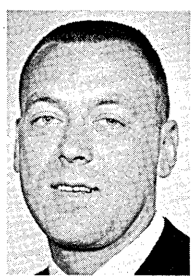
The Demonstration Generator, you will notice, has no catchy name. Naturally, we are saving this job for the ACRONYM statement, to be completed shortly. Also although the Demonstration Generator is not quite completed, we are preparing a demonstration for interested parties. That is, we are going to use the Demonstration Generator to generate a demonstration of the Demonstration Generator generating a demonstration.

The subject of information processing in command and control is not new to DATAMATION readers, having been discussed in our June issue (p. 58) by authors Christie and Kroger. It is felt that the following thoughts on this topic will also be of interest and especially noteworthy in light of the transcript of The RAND Symposium, to be published next month. As stated in the June presentation, DATAMATION's editorial policy is not reflected in the following article.

an editorial commentary

THE PROGRAMMING PROBLEM IN COMMAND & CONTROL

by W. H. WATTENBERG, University of Calif. Lawrence Radiation Lab., Livermore, Calif.



Computer Command and Control systems are the most complex data communication and processing systems in existence. The complexity of new systems being developed and those planned for the future stagger the imagination. These systems demand the most laborious type of programming since each system includes a wide variety of special purpose input/output data acquisition and display equipment which must be controlled by computer programs. The large C & C programs now running were generated by hundreds of programmers using the machine language of a particular machine since no better programming tools were available. However, the programming requirements of present Command and Control systems are small compared to those of systems planned for the near future.

The problem is obvious. The cost and delays in producing operational programs for new systems will be prohibitive unless much better programming tools and methods are available.

Both the Department of Defense and Defense contractors have recognized this problem and proposed solutions. The heart of the solution is a standard programming language for Command and Control. The definition of the standard language is by no means the total solution to the programming problem, but it is the necessary beginning. Efficient compilers and operating systems must also be developed, and these will require standards in hardware as well as software.

The Institute for Defense Analysis has studied the programming problem in Command and Control systems, and has issued a report entitled, "Computers in Command and Control." The report points out that a standard language for Command and Control can be developed without the need for further research in programming languages. The report also points out, "Neither ALGOL nor COBOL alone is sufficient in scope for Command and Control system programming," and that blending these with additional features "would create a monster which would be neither fish nor fowl." IDA studied three languages—CL-2, JOVIAL, and NELIAC, each of which reflect some consideration of Command and Control programming problems, and concluded that none was sufficient for the total Command and Control problem. IDA recommended that a standard Command and Control language be adopted which was a blending of the three languages. However, the IDA recommendation did not point out what parts of the three languages would be desirable in a standard Command and Control language. Neither did it mention those areas in which the languages were lacking.

At present, no existing language is adequate for the varied tactical programming problems in computer Command and Control systems. For example, none of the three languages mentioned above is sufficient for describing the very important real-time processing requirements of tactical systems. Unfortunately it is exactly the requirement for real-time operation which distinguishes Command and Control programming from the areas in which most of the language development has occurred.

There are three basic requirements which an acceptable standard language for Command and Control must satisfy.

1) The facilities of the language must be adequate to describe Command and Control problems of major concern.
2) The language must be easy to learn and use.
3) It must be practical and possible to construct compilers and operating systems for the language which produce efficient object programs.

The first requirement is obvious, but it will not be easy to satisfy. It is doubtful that anyone has described in detail all the various Command and Control operations being performed by computers, in particular the real-time data processing and communication operations. The Command and Control programming problems must be carefully formalized. A definition of the language before this is done is just guesswork, and the result may be of little value in the areas where there is the greatest need.

In examining the problem oriented languages which have been of most practical value one finds two common characteristics. A) They are simple in syntactic structure. B) They are easy to learn and remember. Such languages are uninteresting to the theorist; a blessing to the technician, but they are actually being used rather than just studied by programmers. The language we are seeking will be judged on the basis of dollars and programming time saved, not on the basis of academic or research value.

The three requirements stated above are certainly not independent. The state of the art in compiler building indicates that efficient compilers and operating systems can be constructed for a language which is unambiguously defined and satisfies requirements 1 and 2. The real question is the cost of the software. Compiler builders will not be allowed to adjust the two parameters of object program efficiency and implementation cost as freely as they have in compilers for scientific and business data processing. In the latter cases, the data being processed is normally by machine time rather than real-time. Object program efficiency cannot be sacrificed in many Command and Control programs. Loss of object program efficiency may mean failure to meet mission requirements and objectives rather than just increased processing costs. On the other side of the fence, system designers must give more consideration to programming characteristics of the various components assembled into the Command and Control system. They are too often satisfied by the fact that two devices fit together electrically without worrying about the languages they speak. The compiler builder's job is not made any easier by the existence of "almost identical" equipment in supposedly identical installations.

Efficient compilers and operating systems will be extremely expensive if the proliferation of equipment programming characteristics continues at the present rate. First and foremost is the need for standards in the control of input/output devices. This problem is not going to be defined away in a language. It requires standards for the logical design of hardware.

Assuming reasonable standards in the programming characteristics of equipment, the costs of constructing compilers for a standard Command and Control language will be minor compared to the costs of documentation, maintenance, and programmer training. Compiler construction is basically a one shot affair for a given machine, whereas the latter activities must continue for the useful life of the language. Programming training in particular must be given the most careful and serious consideration in choosing a language. The virtues of simplicity in a language are only too well known to those who have faced this problem.

The optimum approach for rapid development and acceptance of an adequate Command and Control language with efficient compilers and operating systems is to work from the bottom up – from the specific to the general, not vice versa. Tactical programming requirements are the most difficult to meet. It is here that the real effort must be expended. Strategic programming requirements are much closer to scientific and business data processing requirements, and a great deal of experience is available in these areas. The greatest contributions can be made by those with experience in tactical programs who are willing to formalize their solutions and develop an effective language for the tactical problems, as well as point out the aspects of hardware which create the most difficulty in developing programs. All major hardware and software contractors must be asked to participate in the solution of the Command and Control programming problem. Unless this is done it is very probable that major portions of the problem will remain unsolved. Standards are needed in both the hardware and software. A forced separation of hardware and software development will only result in unnecessary costs and delays in producing operational Command and Control systems.

Some ill-fated compiler projects have started from the top and attempted to work down to the programmer and the problem by a series of compromises and changes in the language and compiler. By the time acceptable systems were developed, either the machines were obsolete or the problems had been solved. In this case the danger lies in the appearance of a multiplicity of languages and temporary solutions while the proper solution is being found. Contractors and programmers are not going to stop their work in the solution of immediate problems on the strength of promises of better things to come. ■

COMPUTER PLOTTING FOR ENGINEERING DESIGN

Meissner Engineers, Inc., Chicago, has developed a computer-plotter system which is capable of designing a wide range of engineering and architectural products, directly from prerequisite information, and producing fully dimensioned working drawings. The system employs an IBM 1620, 1401, General Dynamics/Electronics S-C 4020, plus a microfilm processor and reproduction equipment.

All software for the system was designed by Meissner personnel, and utilizes the 4K memory of the 1401, and the 1620's 40K digit memory, which can be expanded to 100K digits.

According to Robert C. Meissner, president of the engineering-construction management firm, the MEISENG system can design anything that can be mathematically described. Current efforts have been concentrated on developing computer-plotter program and sub-routines in the broad fields of structural, civil, mechanical and electrical engineering, in addition to the production of business routines.

In operation, mathematical design data, such as dimensional and loading details for structural steel products and terrain elevation and width for highway routing, is prepared for processing by conversion to punched cards, which are input for the 1620. The output, incorporating the basic design program which is stored in memory, is expressed in plotting instructions on cards.

The 1401 translates this information from digital to binary instructions on mag tape, along with positioning instructions, which were stored in memory. The plotting and positioning instructions determine the type, length, and direction of the drawing line to be placed by the electron beam within the cathode ray tube of the S-C 4020.

The proper drawing details are symbolically traced, and all calculated dimensions and instructions for the particular structural design segment are inserted. A form projection, such as company symbol, logotype, etc., is simultaneously superimposed over the design. The entire presentation is recorded on 35 mm microfilm by a camera in the S-C 4020. After processing, the film is prepared in strip form on mounted aperture cards. Using an electrostatic printer, dimensioned drawings up to 24x36" are made. ■

The physical support of a major computer installation is provided by means of a unique architectural system, especially designed and custom-tailored to fit the needs of individual data processing centers. The advantages of a raised flooring system are numerous, outweighing by far the hazards that might be encountered if exposed cables were allowed to snake to, from, around, and behind peripheral equipment, main frame, console, cabinets, etc. The systems described in the following article represent a sampling of the many types of computer floors currently available, and should not be viewed as an all-inclusive catalog.

THE FLOOR BELOW

for heavy machines and overweight operators

The components of elevated, or free access flooring systems for computer installations consist of individual, removable sections, providing access to electrical connecting cables, air-conditioning and heating ducts. Each panel is a "sandwich" of aluminum, steel, plywood, hardboard, or specially-formed rigid material, topped with a bonded surface of vinyl or rubber tile or carpeting. The panels are maintained either by a framework of aluminum or steel stringers, or are self-supporting. In former design, the basic support is furnished by adjustable pedestals or jacks.

Functionally, there is no difference between one flooring system and the next, as all provide a utility area between the sub-floor and raised floor, contain a built-in safety factor to support heavy data processing equipment, and the elements are fire resistant or retardant.

The physical properties and component design of each system will vary, however, as the following descriptions of representative manufacturers' products point out:

COMPUTER FLOORS, INC., Hackensack, N. J.: Panels, measuring 18¼ x 18¼″ are made of die cast aluminum plates, and covered with vinyl tile ⅛″ thick. A plastic lip the height of the tile makes the flooring modules non-conductive. Steel supporting structural hardware is plated for rust prevention. Finished floor heights are available from 5⅝″ to 14″ with under-floor free access areas from 4⅜″ to 12¾″. Load capacity is 275 lbs. per sq. ft.

CIRCLE 119 ON READER CARD

CONSTRUCTION SYSTEMS, INC., Los Angeles: Three types of systems are available, incorporating aluminum, steel, and steel and plywood. The all-aluminum design consists of extruded aluminum planks of 6063 alloy, with interlocking edges of a concave-convex configuration for matching between adjacent modules. The panels, measuring 9 x 27″, are covered with vinyl tile ⅛″ thick. Lateral beams, of slotted, roll-formed 12 ga. steel and supported by pedestals, form the supporting structure. Load capacity is 250 lbs. per sq. ft. The module incorporating steel and plywood is made of 24 ga. steel, laminated top and bottom to a plywood core. For extreme load conditions, the all-steel panel, of non-modular design, is available.

CIRCLE 120 ON READER CARD

FLOATING FLOORS, INC., New York City: Stringers are not used in this system, as each 18¼ x 18¼″ die cast aluminum module interlocks with the adjacent module, supported by a pedestal at the juncture. An electrically non-conductive plastic lip surrounds the 18 x 18″, ⅛″ thick vinyl covering. Positive contacts are provided in the structure to give electrical continuity for grounding all of the metal of the floor. The area beneath the raised floor can be utilized as part of a low pressure heating and ventilating air-conditioning system. Two modules are available, rated at 250 lbs. capacity per sq. ft. and 100 lbs. per sq. ft.

CIRCLE 121 ON READER CARD

HARFORD METAL PRODUCTS, INC., Aberdeen, Md.: Panels are constructed of an aluminum honeycomb core, with a 16 ga. steel sheet bonded to the top surface, and a 24 ga. steel sheet bonded to the bottom. Sizes of modules are 3 x 3′ and 2 x 4′. The supporting framework is a fabricated steel channel 2 x 1¼″. Load capacity is in excess of 250 lbs. per sq. ft.

CIRCLE 122 ON READER CARD

HASKELITE MANUFACTURING DIVISION EVANS PRODUCTS CO., Grand Rapids, Mich.: Floor panels consist of 24 ga. zinc-coated steel, structurally bonded to both surfaces of exterior grade fir plywood. Standard panel sizes are 3 x 3′ and 2 x 2′, one inch thick, covered with ⅛″ vinyl tile. A vinyl edge banding surrounds each panel, making installation grounding unnnecessary. Panels are interlocking, with support provided by a pedestal at each intersection. Load capacity is 200 lbs. per sq. ft.

CIRCLE 123 ON READER CARD

LISKEY ALUMINUM, INC., Glen Burnie, Md.: Two types of panels are offered: Steel-Core, consisting of a 1″ phenolic-bonded core material faced on both surfaces with 24 ga. zinc-coated sheet steel, with panel edges slotted and sealed with an aluminum extrusion bonded to the plywood; and Elafloor, fabricated of extruded tongue-and-groove aluminum planks welded to extruded end bars. Steel-Core panels have three edge trim options: 3/16″ vinyl, aluminum, or no visible edge trim. A 3/16″ vinyl edge trim is optional with Elaflor. The substructure for Steel-Core is stringers made of rolled-steel channel with a vinyl rib on top. Elaflor stringers are extruded aluminum channel, also featuring a vinyl rib. The purpose of the rib is to prevent lateral movement of panels whenever adjacent panels are removed. Both systems support 250 lbs. per sq. ft. Size of modules is 2 x 2′.

CIRCLE 124 ON READER CARD

STRATO-FLOOR, INC., Cleveland, Ohio: This system incorporates a triangular jack, rather than a single-pillar pedestal. Two points of the jack are bolted to the stringer framework, while the apex is bolted to the sub-floor support. Panels are made of non-combustible fiberglass, molded around a wood core. Stringers and cross braces are ⅛″ gauge steel channel, 2½ x 1½″. A rubber seal is applied across the cross brace spacers, at right angles to stringers, and in short sections in the direction of the stringers, to form an air, water, and dust-tight seal. Panels, which measure 24 x 24 x ⅞″, do not require floor tiles. Support load is 250 lbs. per sq. ft.

CIRCLE 125 ON READER CARD

UNISTRUT PRODUCTS CO., Chicago, Ill.: An automatic self-locking device secures the jack to the channel gridwork, eliminating the need for nuts, bolts, or spring locks except at terminating locations, such as walls and columns. 2 x 2′ panels are of the pan formed type with .018 steel skins, bonded around exterior grade plywood; 3 x 3′ panels, also pan formed type, are made of .024 steel skins. Both sizes are furnished with or without extruded grey vinyl plastic edging. Framework grid members are 1⅝″ wide, 12 ga. steel channels with pyramid-shaped inturned edges. Total uniform load is 250 lbs. per sq. ft. Jacks provide adjustability from 4″ to a standard maximum height of 14″.

CIRCLE 126 ON READER CARD

WASHINGTON ALUMINUM CO., INC., Baltimore, Md.: Panels are constructed of a welded assembly of formed steel plates, and have periphery contact with frame for positive electrical grounding. The grid framing is fabricated of zinc-coated rolled steel. Vinyl, rubber, carpeting, and wood parquetry are optional floor coverings. Standard 2 x 2′ x 1″ panels support a minimum of 250 lbs. per sq. ft. ■

CIRCLE 127 ON READER CARD

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people IN DATAMATION

■ Frank Wagner, Group Leader, Numerical Sciences, North American Aviation, Los Angeles, resigned his position last month to join Informatics, Inc., Culver City-based consultant firm, as Director of Plans and Programs. Wagner who had been with NAA for 18 years, was founder of the NAA computing facility. He is a member of the executive council of the Association for Computing Machinery, and is a past SHARE president. At press time, no successor has been appointed.

■ John McCarthy has returned to Stanford University and will serve as professor of computer science. He had been on the MIT faculty since 1958, where he was professor of communication sciences, and at Dartmouth College, 1955-58. He was an acting assistant professor of mathematics at Stanford during 1953-55. McCarthy has been active in the fields of multiprogramming, artificial intelligence, and remote-control computer operations.

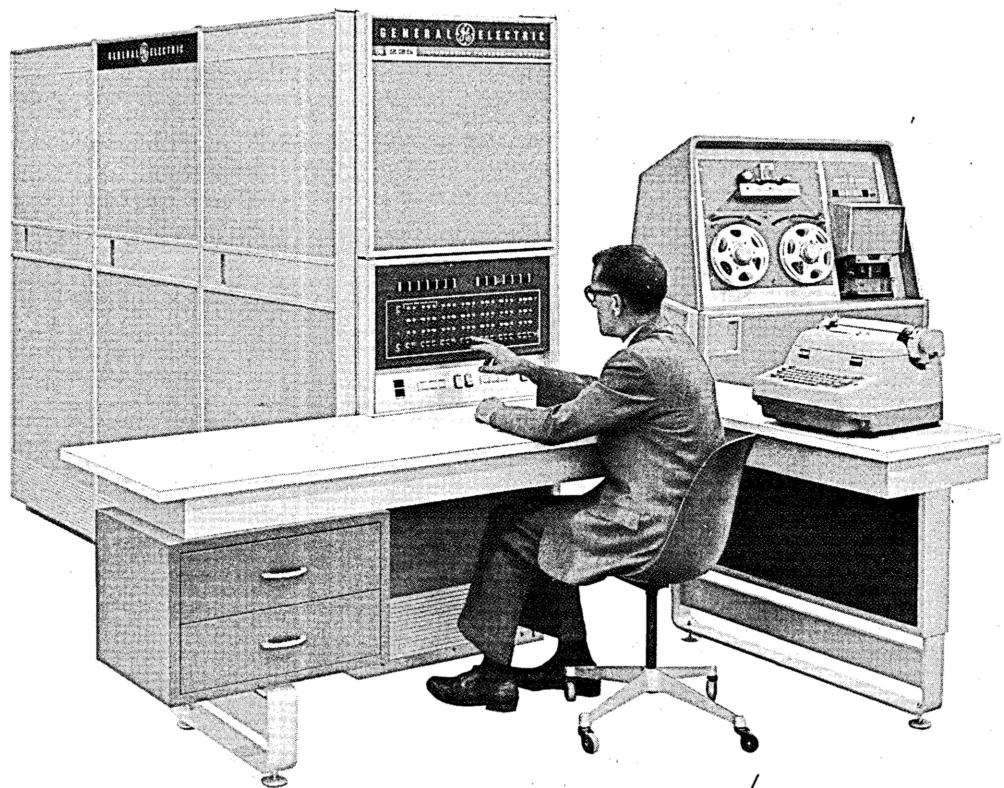
■ Richard E. Utman has been appointed director of standards of the Business Equipment Manufacturers Association's Data Processing Group, and will coordinate the standardization program sponsored by BEMA/DPG under the American Standards Association. His duties will also include the international aspects of this effort. Utman's most recent position was at UNIVAC, where he was director of systems standards. He replaces Herb Bright who is now with Philco Computer.

■ The election of Cuthbert C. Hurd to the position of board chairman of Computer Usage Co., Inc., has been announced by Elmer C. Kubie, president. In his new position, Hurd will be concerned primarily with long-range planning. Kubie remains as the company's chief executive officer. Hurd had been with IBM since 1949, and his most recent post there was special assistant to the vice president of research and engineering.

■ Eldred C. Nelson has been appointed director of the Programming and Applied Mathematics Laboratory at STL's Computation and Data Reduction Center, Redondo Beach, Calif. Associated with Ramo-Wooldridge since 1954, Nelson joined STL, a TRW subsidiary, last January. He had been senior staff engineer in the Systems Research and Analysis Division prior to his appointment. He replaces Edward K. Blum, who resigned to direct computing activities at Wesleyan University.

■ Fred W. Bauer has joined UNIVAC as manager of product planning. Previously, he was with Bendix in a sales and marketing capacity. Bauer has also been associated with Burroughs and IBM.

■ Digital Electronics, Westbury, L.I., N.Y., has named Samuel Lubkin as chairman of the board. The firm, Lubkin stated, will concentrate in the field of custom designed data conversion equipment, educational training devices, and a proprietary line of pulse and digital test equipment. Dr. Lubkin was associated with the ENIAC and EDVAC projects, and was responsible for the logic design of the SEAC computer at the National Bureau of Standards. He was founder and president of the Electronic Computer Corp. (ELECOM) in 1947, before it became a division of the Underwood Corporation.



it's true For $2,390 per month, you could have a complete GE-225 computer installation, ideal for scientific computation. The price includes the central processor with 4096 words of 18μs memory, paper tape input and output, electric typewriter and console. We really mean it when we say "complete." You won't find out later that things like multiply and divide hardware are "extra." They are standard on the GE-225.

The pricing structure on the GE-225 has been simplified to tell you exactly what you need and what you get. Pick the size of memory and the input/output equipment you want. You can't be misled, because there are only 10 other options in the entire GE-225 line (and none are normally required with the $2,390 system to obtain results). The prices are clear and to the point.

But don't get the idea that the system described above is the only GE-225 system available. This small system will do a wide range of scientific problems, but it will obviously have limitations in problem size with 4096 words of memory and no magnetic tape. Input/output will be in the form of paper tape. That's enough to meet many requirements, but if it is too small for you, or you figure you might outgrow it, look what you could add:

- Memory up to a total of 16,384 words.
  Note: By adding 4096 words, you can use WIZ, the algebraic compiler.
- Card reader...400 or 1000 cards/minute.
- Card punch...100 cards/minute.
  Note: The basic scientific system with a card reader (400 card/min.) and punch, in place of paper tape is $2,675/mo.
- Magnetic Tape...15 KC, 41.6 KC or 66.6 KC.
- High speed printers...900 line/minute on-line or on/off line.
- Magnetic Random Access Data Storage...18.8 million characters per unit.
- Document Handler...Reads and sorts 1200 documents/minute.

- o Provision for up to 10 read/write operations simultaneous with computing.
- o Floating point and double-word fixed point hardware.
- o BCD package...3-way compare, added index words, decimal add-subtract.
- o Automatic interrupt.
- o Real-time Clock

Somewhere along the way in your expansion, you will probably have added data processing applications to the work load. Good. The GE-225 is ideal for this combined use, with its full peripheral line and its binary arithmetic, backed up by BCD capability. The addition of management planning, control and decision applications won't throw it either.

A very large GE-225 system has approximately ten times the capacity of the small system designed only for scientific applications. So start with whatever meets your immediate needs. Forget the idea that you will have to replace your GE-225 if your problem load becomes bigger and more sophisticated.

* * * * *

The support behind every GE-225 matches fully the proven performance of the system itself. Take software. GECOM, the general compiler, combines a business oriented language, an algebraic language, a tabular language (TABSOL) for decision making problems, and an unusually capable report writer.

WIZ offers simplified scientific programming and fast compiling speeds. GE-225/CPM brings control of time and cost in project management. ZOOM allows machine language programs to be written in "shorthand." All of these program systems, plus many industry oriented programs are available to the GE-225 user.

* * * * *

Reliability of the GE-225 is becoming legend. Its conservative design produced exceptional reliability to start with. The thorough training of General Electric's service engineers makes it a certainty that this kind of performance will continue.

* * * * *

Right down the line, General Electric provides the services needed to see you through the transition from manual methods (or from an obsolete computer, for that matter) to efficient, effective computer operation.

Now you know perhaps half the story. There are many important features of the GE-225 which have only been touched on here, or not mentioned at all. Get the <u>whole</u> story and you will find the GE-225 to be far and away the biggest buy in its price range.

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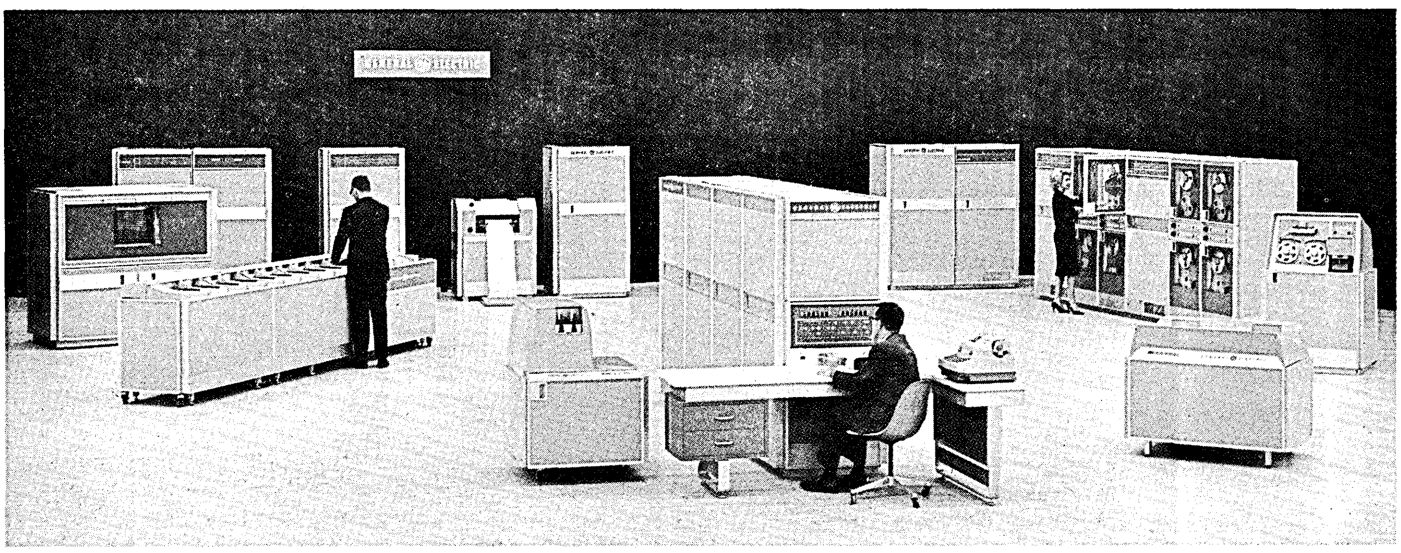
In Canada: Canadian General Electric Company, Limited, Electronic Equipment and Tube Dept., 214 King Street West, Toronto, Ontario, Canada

In Europe: International General Electric S. A. Data Automation Department 81 Route del'Aire Geneva, Switzerland



A large GE 225 system

Progress Is Our Most Important Product

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LITHO IN U.S.A.

DATAMATION SEP 62

WHY MULTI-COMPUTERS?

by WALTER F. BAUER, President, Informatics, Inc., Culver City, Calif.

The era of the multi-computer system is apparently upon us. The computing field is now beset with multi-processing, satellite and polymorphic systems with promises of many new and varied types to come. Meanwhile there seems to be little evidence of a firm understanding of multi-computer systems and a cursory investigation shows that there is much fiction mixed with the fact. It is the purpose of this article to review some of the fact and cut away some of the fiction.

There are two unmistakable trends in digital computer systems: parallel processing, and modularity. The first step in the trend toward parallel processing (or multiple computing) probably took place when the 60-word buffers for tape operations were announced as part of the UNIVAC I system; here was the first step of an operation, although a simple one at that time, provided outside the main frame. The temporary storage of quantities and synchronizing of signals between the electronics of the main frame and the electromechanical devices to which it is connected came to be standard items with computers like the Remington Rand 1103A and the IBM 705. With the advent of the IBM 709/7090 an important step was taken: the decentralization of part of the control from the main frame and its evolvement to data synchronizing channels to allow transfers independent of the main frame. In this same period the LARC computer with its completely independent processors came into being and Bull's GAMMA 60 computer with its independent arithmetic-logic units was announced. Since then, nearly all computers have a parallel processing capability in varying degrees. Multi-computers as discussed here, is simply another step in this apparently inexorable march toward decentralization of functions.

The other trend in computer systems, modularity, probably first appeared in the UNIVAC I when the customer was allowed to buy any number of tape units up to 10. Since then, the customer has had the option of buying the number or amount of memory, printers, punches and other output devices, and more recently data synchronizing channels which provide a control capability. With the LARC computer, modularity took a very big step forward when an entire processor could be added to the system. Again, multi-computers are simply an extension of these ideas.

Among more modern computers which have a multi-computer capability are the Burroughs B-5000 and the Bendix G-20. All of the most recently announced computers seem to have a multi-computer aspect. The IBM 7040-7094 systems have multi-computer provisions, the CDC 3600 can be a multi-computer system, and the Bendix G-21 is a complex of G-20s.

It should be noted that the ability to process in parallel or simultaneously is quite a different characteristic than modularity which has not proceeded nearly as far as parallel processing.

definitions and classifications

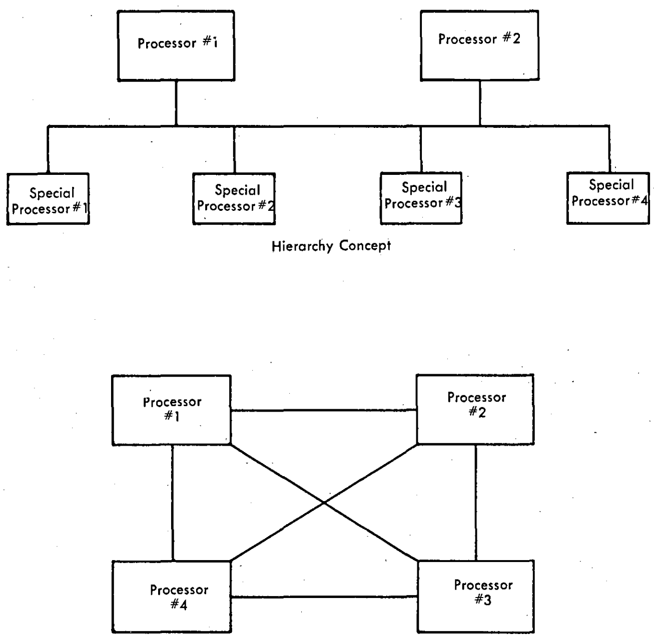
The definition of multi-computer system is in itself interesting and challenging if not contentious and controversial. A reasonable definition is one which satisfies the following four criteria:

1. There are two or more separate arithmetic control units capable of operating simultaneously and with special

hardware facility for operating two or more programs simultaneously.
2. There are two or more independently operating primary random access memories.
3. Communications among major elements of the system is of the memory-to-memory type at memory access speeds.
4. All major components of the system are in use during normal operations.

The first criterion is probably satisfied by most of the computers which in some sense claim parallel processing. However, there may be some question of interpretation in the case of the GAMMA 60, STRETCH, and Honeywell 800. Also, there is a continuous spectrum on how this criterion is met by the different computers. A CDC 1604-160 or IBM 7044-1410 configuration certainly fits this requirement as does the LARC or the RW-400. Computers such as the GAMMA 60, STRETCH or the 800 meet it to a lesser degree. In the case of the 800, for example, the arithmetic unit is time-shared by the various operation programs although up to eight problems can run simultaneously. In the case of STRETCH, there is no special provision for operating totally independent computer programs although the logic processor operates simultaneously with the arithmetic processor.

Some of the systems which satisfy the first criterion fall by the wayside in consideration of the second. Independently operating random access memories implies that the selection and switch circuitry is such that two or more quantities can be accessed simultaneously. Thus the GAMMA 60 without this capability does not satisfy the requirement. Of course, the use of a hierarchal memory system such as one using core and disc file memory would not satisfy the criterion unless the primary memory was capable of multiple access.



Hierarchy Concept

Distributed Concept

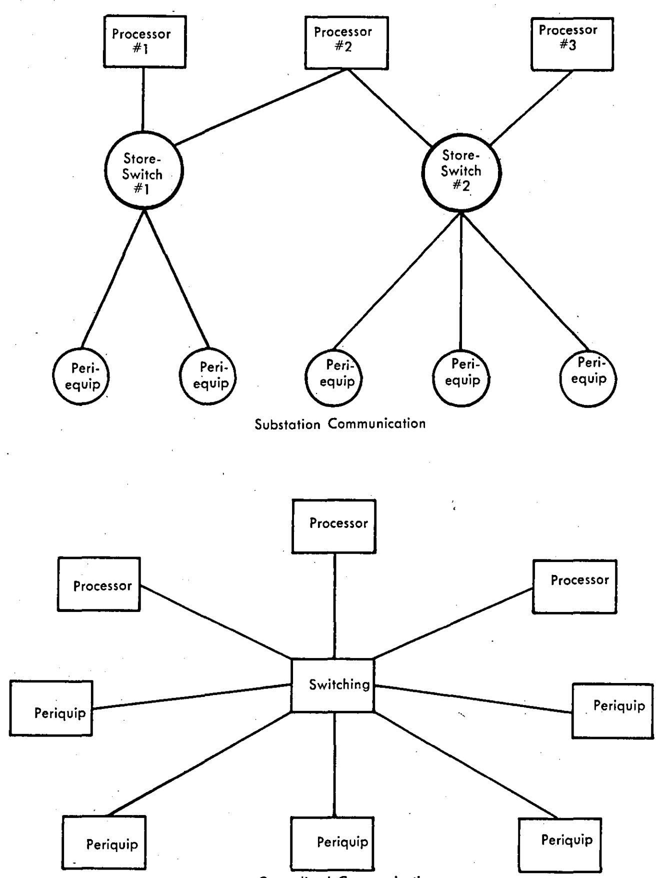
ASSIGNMENT OF FUNCTIONS

figure I

Criterion three means that most computer-to-computer communication schemes which use magnetic tape as an interim medium (or cards, or paper tape) do not qualify as multicomputer systems. This would be true of systems connected by communication systems as well as those in close proximity which communicate by means which require manual operation such as the transfer of tape reels or the manual setting of a switch.

The fourth criterion referring to all major components being in use during normal operations is included to rule out systems such as SAGE where one computer is simply a reliability backup for the primary one. This "duplexing" for reliability is in common use in the military in systems like BMEWS and in some commercial systems like SABRE. Based on the preceding definition, none of these systems should be classified as multi-computer.

The classification of multi-computer systems deserves some attention. First there is a question of the *assignment of functions.* Figure I shows two major concepts possible. The first, the hierarchy concept, is one where one or more central processors carry out the main processing load and a number of special processors carry out subordinate tasks. The case of a Philco S-2000 – 2400 system is a single thread special case of this hierarchy concept. The distributed concept is the other way of assigning functions and it refers to having two or more processors each with approximately equal power and each with roughly the same level of responsibility in the system. This is the approach used in the RW-400. Note that in the hierarchy concept, the problem is "torn apart" according to the functions to be performed, while in the other concept it is "torn apart" by the size of the problem.



Substation Communication

Centralized Communication

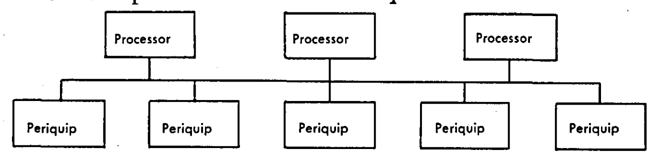
TOPOLOGY OF COMMUNICATION

figure II

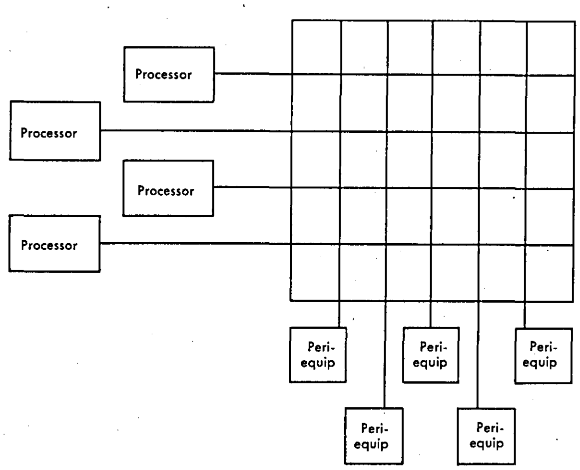
Once having considered the assignment of functions, the *topology of communications* comes under discussion. There seem to be two major approaches: the substation communication approach and the centralized communication approach. They are shown in Figure II. In the substation approach there is a level of principal processing and there is a level of communication and switching such that all communication with peripheral units (drums, tapes, displays, etc.) is handled through communication with the substation. This approach is used in the Bendix G-20 and to some extent in the IBM 7090. It has advantages of requiring no highly specialized or unusual devices to accomplish the switching processes since this is handled by smaller computer-like devices which could include smaller satellite computers like the CDC 160 or the H-400. It has the disadvantage that if the switching requirements become high, the computers used at the substation become expensive and awkward switching devices.

The centralized communication approach has the advantage of flexibility in the assignment of functions to the various modules since very few of the modules are dedicated to a particular task. Also, since no modules are critical to the operation of the system except the switching equipment itself, certain system reliability and flexibility advantages accrue.

Perhaps it is clear that in the centralized communication concept the switching function can be centralized as with a switch of the crossbar type, or it can be decentralized as with the information bus arrangement. In Figure III there are depicted these two techniques for communication



information bus



Central Switch

COMMUNICATION AND SWITCHING
figure III

and switching between elements. In the information bus technique, one module communicates with another either by specifying and decoding and addressing, or by using the dedicated time slot technique. The information bus is, of course, time-shared. The advantages of the information bus type switch is that the techniques are by and large conventional and it is inexpensive if the number of modules remains small.

The other kind of switching approach is that of the central switch as shown in Figure III. In this approach, pairs of modules are in communication and many pairs communicate simultaneously. This is the cross bar type switch similar to that used in the telephone central. The advantage of this switch is the low cost if the number of modules is high. Also, the communication rates through the switch can be very high since each of the communication paths is independent of any of the others. Another advantage is that certain functions associated with switching can be included with the switching equipment; assignment tables which allow communication only between modules in a subset of the system, thereby reducing the inadvertent destruction of information; and symbolic addressing can be used, under programmer control, for assignment of names to the various "spigots" of the switch. The disadvantage is the fact that few electromechanical or electronic switches of this type suitable for computer use have been made, and for system ultra-reliability such as in military applications, need to be duplexed. Ramo-Wooldridge has made three such devices for use with the RW-400.

present systems

At present there are only a few truly multi-computer systems (or multi-computer systems truly used as such) in operation anywhere in the world. This is especially true if one ignores specialized military systems. Despite the fact that the CDC 160 was introduced as a satellite computer fully able to communicate with the 1604 there is only one system in such use to this writer's knowledge. This undoubtedly reflects the lack of developed use technology of multi-computer systems and the lack of sophistication of the user community rather than the efficacy of multi-computer systems or the particular design of the 1604-160 tie-in. It should be noted that a number of 1604-160 installations plan extensive multi-computer uses.

An IBM 1401-1620 installation is in operation in Portland, Oregon, for the purpose of processing highway engineering data. The system is considered to be in balance since the 1401 is able to perform the input function efficiently, whereas the 1620 can be used efficiently for the arithmetic operations required after input. An informal survey indicated that there are few IBM computers used in a multi-computer configuration. LARC computers which are multi-computer processors, are in operation at the David Taylor Model Basin in the Washington, D. C. area and at the University of California Lawrence Radiation Labo. Last year at Ramo-Wooldridge a three-computer RW-400 system was tied to a CDC-1604 for a very large scale system.

A very interesting discussion of the LARC multi-computer programming aspects is contained in a paper by Tonik and Schmitt[1]. Another such paper is the one by Perkins and McGee[2] reporting experience on the RW-400 – CDC-1604 system.

There are a number of military systems in which computers are used in a multi-computer configuration. Two Remington Rand 1103As are used in classified command and control application for the Navy. Two 1103As at Holloman Air Force Base have been used for data reduction. The HARVEST system made by IBM is a multi-computer operation with certain specified processing capability and the Naval Tactical Data System using the Remington Rand M480 computer is another such military example. In only a few of these cases are full descriptions of the systems available in open literature. It is uncertain whether these systems meet the above criteria for multi-computer systems.

motivations for multi-computers

There are a number of motivations which are claimed for multi-computers. Some have basis in fact and analysis. Others are only apparent on the surface and do not hold up under close scrutiny. In the following paragraphs, some of these motivations are discussed in increasing order of their merit.

To ease the Central Computing Load. This is the reason most frequently heard for a multi-computer system. It is also the reason which has the least merit. In very few cases does it pay to have the total capacity of the system increased by 5 – 15% with a satellite or an input/output processor in the case where that associated processor is small and relatively incapable; usually the central computer can do the job faster and more economically than the smaller computer. The only true merit to this argument occurs when the problem is simply too big for the computer and there is a sizeable input/output processor or sizeable satellite computer which can be used in the system to reduce the demand on the main computer.

Lower Equipment Cost. Usually the smaller computer has a lower capability/cost ratio than the larger. If cost of equipment is the only consideration, then there is seldom a good argument. However, the economics of the system can sometimes be improved by a decentralized computer system. Consider, for example, the case of an extremely high duty cycle on the memory unit of the main computer where there is the desire to add more high-speed input data. Multi-computer systems can result in lower equipment costs but a careful analysis is required which depends on the many use factors of the system.

Reliability. Here is certainly a good reason for multi-computers. For on-line military systems, the reliability which one gets from one central computer in consideration of the 24-hour, seven-day week required uptime of the computer is simply not high enough. For one thing, the computer must undergo periods of preventive maintenance. If one divides the total problem in half and applies a two computer system to perform the task, a single computer can carry on the high priority half of the problem while the other computer is down for preventive maintenance or malfunction. (Note that this is quite different from the duplexing referred to earlier, where one computer is not normally used and provides backup only.) It is quite clear that in a highly decentralized, modular system a few extra modules give the system a reliability that is equal to the duplexing of a larger computer. In a system where a large computer is used for central processing and a smaller computer is used for input and output, if either computer goes down, the system probably does not lose all its capability; and if the down period is not great, there is probably little time lost in the total operation.

Expansibility and Flexibility. Multi-computer systems are clearly expansible and flexible. In the case of a modular multi-computer system, additional modules can be added conveniently. In most cases, flexibility is gained by using the various larger elements in different ways at different times. Even in a multi-computer system which is not modular, it is still possible to easily expand the system capability by replacing one of the computers with a more capable computer, provided that the interface between the computers was such that the programming problem is not unduly complicated by this replacement.

The Establishment of Control Hierarchy. From strictly a programming point of view multi-computers allow a more natural division of the problem into levels of control. The control of a large scale multi-computer on-line system is a complex matter. It requires various levels of control such as the control of the overall environment and its response to the people using it, the assignment of the various modules such as printers, buffers, tape units, etc. and the detailed control on a subroutine level of various information transfers.

Programming Organization. The clearest advantage of multi-computers lies in the naturalness with which the programming job can be organized. Natural interfaces in programming can be developed between the various large program components such as input, output, analysis, information retrieval, and the like. This is of great advantage in large programming jobs, especially where pieces of the programming might be subcontracted. In the event of independent programming in independent computers with simple communication interface between the two systems, programming of the two computers can be relatively independent. In the case of executive programs alone, for example, the separation from the executive control program of the input/output executive program greatly simplifies synchronization and memory allocation problems.

It should be emphasized that the above paragraph refers to the programming problem where there is some "naturalness" to the division of the effort and where the multi-computer system allows the natural division. The programming of a complex trajectory analysis program would probably be a difficult job on a multi-computer system. On the other hand a system requiring extensive real-time input-output or servicing of display-interrogation units as well as a central processing function can be programmed more easily in a multi-computer system where the satellite system handles the former functions and the main computer the central processing functions.

A common myth in multi-computer systems is that the complexity of the overall master control program (in an n-computer system) must be so overwhelming as to render the whole plan infeasible. This is not true. A usable and quite comprehensive master control program for the RW-400 – CDC-1604 system mentiond above (three computers, six buffers, three drums, eight tapes, and one 1604) was less than 5000 words in length.

problem analysis

In discussing the possible reasons for a multi-computer system, lower equipment cost was advanced as a motivation. However, the question of equipment cost is a complex one and requires careful analysis on a case-by-case basis. In the following discussion it is assumed that the general question is raised as to whether a satellite type computer should be added to the central computer to provide a rudimentary multi-computer configuration. Certain specialized cases are discussed. No general policies or philosophies are generated and the cases are only meant to be illustrative of the type of analysis which should be undertaken.

A Tape Limited Problem Where More Input is Desired. In this first case, it is assumed that the machine is tape limited – the main frame has to wait on tape input – and more input from a different source such as a data link is desired. This case is simple and it is quite obvious that the main frame and communication channels in all likelihood can handle the additional input and no satellite system would improve the economics of the system.

A Tape Limited Problem – and There is an Urgent Need to Speed up the Total Processing. Consider, for example, an application where inputing the N + 1st record takes 30 milliseconds, then processing requires 15 milliseconds but can proceed simultaneously with input and output, and outputting of the N – 1st record, 30 milliseconds. The total processing can obviously be speeded up by performing tape input simultaneously from two sources. This can be accomplished by reading tapes simultaneously into the machine through two or more channels and out of the machine by two or more channels, or by utilizing satellite computers to read the tapes and predigest the information for the central processor. The addition of four satellites, for example, in this case, would approximately double the total computing speed and might have other advantages over simply adding channels and tapes.

A Certain Amount of the Computing is of a Specialized Processing Nature. Consider, for example, a case where 20% of the main computer is used for a specialized process, say, the formatting of input data. The normalized cost figures for the main inputting plus the input processing is $0.8 + 0.2 = 1.0$. If a specialized satellite processor were available to perform the input formatting job at half the cost, the 20% could be "deleted" from the main processor and the cost formulae for the main plus input processing could then be $0.8 + 0.1 = 0.9$, or a cost saving of 10%. This assumes that the 20% deleted from the main frame represents a cost saving on equipment or, equivalently, a time saving on the use of the equipment. Specialized processors to perform certain restricted jobs at low cost are coming closer to reality as the data processing industry burgeons and the cost savings such as these are becoming more likely.

The Magnetic Core of the Main Processor is Saturated and it is Required to Input Data from High Speed Data Links. Assume in this case that sufficient input/outputting is being done in the computer so that the magnetic core of the machine is saturated; that is, there are insufficient memory cycles available to provide the processing of the data. In this case, if a high-speed data link were to be attached to the computer to be read in through a synchronizing channel, the computer would be idle (no processing) according to the number of memory cycles which were being used to read in the data from the high-speed link. In this case a satellite computer could act as a buffer for the high-speed data link and provide predigestion of the input data to reduce the amount of input to the central computer.

the future

The future is seeing a steady decentralizing of the functions which have been in the past accomplished by the main frame. The spectrum between the main frame and the peripheral devices such as tapes, drums, etc. is gradually being filled. A first step in this direction was data synchronizing channels. Steps now being taken are computers with an independent capability. Along with this, specialized processors such as message handlers are coming more and more into use and will provide a greater impetus toward multi-computer systems. We are seeing some evidence of these trends with the short word length in computers which now exist (CDC-160, SDS-910, DDP-19, Remington Rand 1218, PDP-1, GE-225, RW-AN/UYK-1, etc.) many of which do not have 36-48 bit built-in multiplication and division. These are the precursors of the many specialized processors which will be built in the future.

The increasing use of on-line computer systems will provide the climate for increasing use of multi-computer systems. On-line systems tend to emphasize the segmentation of the problem into input, central processing and output. They also tend to emphasize the need for reliability, expansibility and flexibility all of which are advantages to be gained by multi-computer systems.

Whereas large centralized processors will continue to have an important place in the spectrum it appears certain that multi-computers as defined here will command more attention and will represent an increasing percentage of the total computing systems in existence. ■

NOTES

1. W. F. Schmitt and A. B. Tonik, "Sympathetically Programmed Computers," Proceedings of the International Conference of Information Processing, UNESCO, Paris, 15-20 June 1959
2. R. Perkins and W. McGee, "Programmed Control of Multi-Computer Systems," Proceeding of International Federation of Information Processing Congress-62, Munich, August 27 to September 1, 1962

High-Speed, Disc-Storage Option Gives Honeywell 400 Random Access Capability

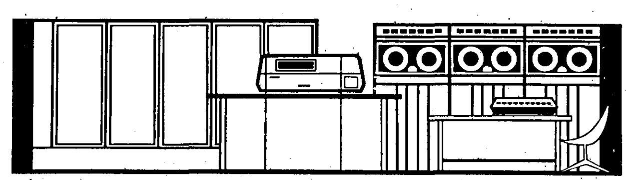
Honeywell 400 with its choice of fast, faster or still faster tape units, expandable core memory, and peripheral overlap capabilities is considered one of the most versatile, flexible and efficient computers in the small to medium category.
The option of an expandable magnetic disc storage file adds still another dimension to the multiple talents of this popular computer: the ability to take on applications that require extremely fast access to any item in a large volume of data without regard to file or transaction sequence.

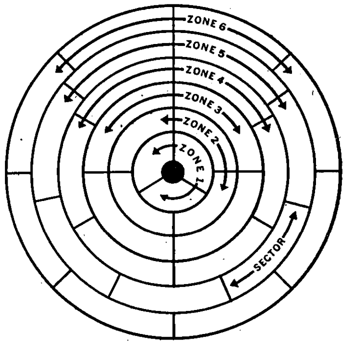
Four Sizes to Pick From

The Honeywell 460 Random Access Storage and Control Unit is available in four models containing 6, 12, 18 or 24 information discs. The capacities of the four models are: 37,500,000, 75,000,000, 112,500,000 and 150,000,000 decimal digits respectively.
One of the features of Honeywell random access is the fact that the smaller models can be expanded up to 24 discs in the field with no interruption in service. There is no increase in physical size of the unit, and existing programs can utilize the added storage area with a simple modification of limit checks on the disc-face portion of the data address.

How to Read a Disc Without a Label

A disc surface is divided into six concentric zones.
Each zone contains 128 data tracks, providing a total of 768 concentric data tracks per disc face.
The zones are sub-divided into sectors each of which may contain up to 64 50-bit words (48 information and 2 parity bits). These 64-word groups are considered records.
There are 32 sectors (records) on each disc face in varying numbers per zone as the following diagram shows.
Note that the inner zone has 3 records, the next two have four each and zones 4, 5 and 6 have 6, 7 and 8 records, respectively. Each disc face has an access arm associated with it, and this arm contains six read-write heads (one for each zone), any one of which may be activated at a time for reading or writing.





A continuous address range is defined as that group of records lying on the same track throughout all zones on all disc faces. (For programming purposes, the disc file may be regarded as composed of 128 small tapes.) No more than 128 track-to-track head positionings are needed, therefore, to go from the lowest to the highest address in the file. The number of records available per tape is a function of the number of discs in the file. Since incrementation of the Control Unit address counter is automatic over the sector, face, and disc, up to 1536 records can be read or written consecutively with each Search instruction. Furthermore, these records can be read or written without intervening delays due to head positioning or disc latency.

Here's How Fast You Can Find it.

The access time of a random access file includes head positioning time and disc rotation delay (latency).
The average time required to position the head system in preparation for reading or writing is approximately 80 milliseconds. Disc latency will vary between 0 and 67 milliseconds.

Here's How Fast You Can Move it.

The rate of transmission of information depends upon the zone involved. The outermost zone will send or receive information at a rate of 112,500 decimal digits per second. The inner zone rate is 41,250 digits per second. The middle zones have transmission rates between these two limits, averaging 73,850 decimal digits per second, or 10.4 milliseconds per record transfer. The programmer need not concern himself with which zone is involved, nor with the rate of transmission, since these matters are taken care of automatically by the H-460 control unit.

While You're Waiting

Searching is initiated in the random access storage unit by means of a peripheral instruction issued in the H-400 central processor. After searching is initiated, control reverts to the main program in the H-400 central processor and other work may proceed until such time as the searching operation is complete. Completion of the search operation is indicated by an interrupt signal approximately two milliseconds prior to the time at which reading or writing may actually take place on the selected track.
The interrupt signal causes a transfer of control to a location in memory which normally contains an instruction to perform the reading or writing process. All searching time may, therefore, be overlapped fully with other programs in the central processor.

With Honeywell You Know It's Correct

Honeywell's exclusive error-correction technique, Orthotronic Control, may be implemented in the disc file. When this technique is used, errors that are detected by the read parity check can be automatically corrected through use of an Orthocorrection routine. Though many competitive systems can detect parity errors, only Honeywell provides for automatic correction.

In addition, the track position of the arm is automatically verified, eliminating the necessity for a programmed checking routine. A write tracking check will indicate any loss of track address verification that might occur during a write operation.

The Hard Work is Done by the Software

Features which simplify the programming required for random access applications are being incorporated into the automatic programming aids provided with the H-400 system. Some of the features of this software include:

Loading Routines which provide for loading and maintaining disc storage data records. The incorporation of a randomizing technique enables a user to distribute master files on the disc in a true random sequence.

Sort Routines designed specifically to optimize the use of the disc storage. The most important consideration in this respect is minimizing the search or access time. Although the search time may be overlapped with processing, the objective is to maximize internal buffer areas. Thus several records can be read or written at a time as the result of one search order.

Utility Routines such as disc-to-tape programs that unload a file of records onto magnetic tape or into a high-speed printer; and tape-to-disc programs that provide the means for reloading tape records produced by the disc-to-tape program or prepared in a similar format.

Checkout Routines are being implemented in the Honeywell 400 EASY Assembly System to assemble disc search, read, and write instructions. The EASY Monitor will also be implemented to dump selected disc records as part of the Program Test System.

So Much For a Starter

If you would like more information on Honeywell 400 and the H-460 Random Access option, write to Honeywell EDP, Wellesley Hills 81, Massachusetts.

Honeywell

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"Why we chose the NCR Computer." —S and W Fine Foods, Inc., *San Francisco*

"With the many items in our product line, we have urgent need for a data processing system which permits fast random access to data stored in our billing, accounts receivable, and inventory files. After a thorough investigation, we chose the NCR 315 Computer which features CRAM . . . Card Random Access Memory . . . as the one best suited to our particular data processing requirements.

"CRAM will enable us to store all the required billing, accounts receivable, and inventory data on-line with the computer. Then as sales data is introduced, the computer will make all the necessary billing extensions, post the accounts receivable, and reduce the separate inventories—all on an extremely fast random access basis.

"Being in a business where QUALITY is of paramount importance, we were very impressed with the quality built into the machines which make up the NCR 315 System. Similarly, we were impressed with the quality built into NCR's software—in both the standard programs and backup support offered.

"In summary, we are certain the NCR 315 CRAM Computer System will be a highly profitable investment."

J. Koregelos

Controller
S and W Fine Foods, Inc.

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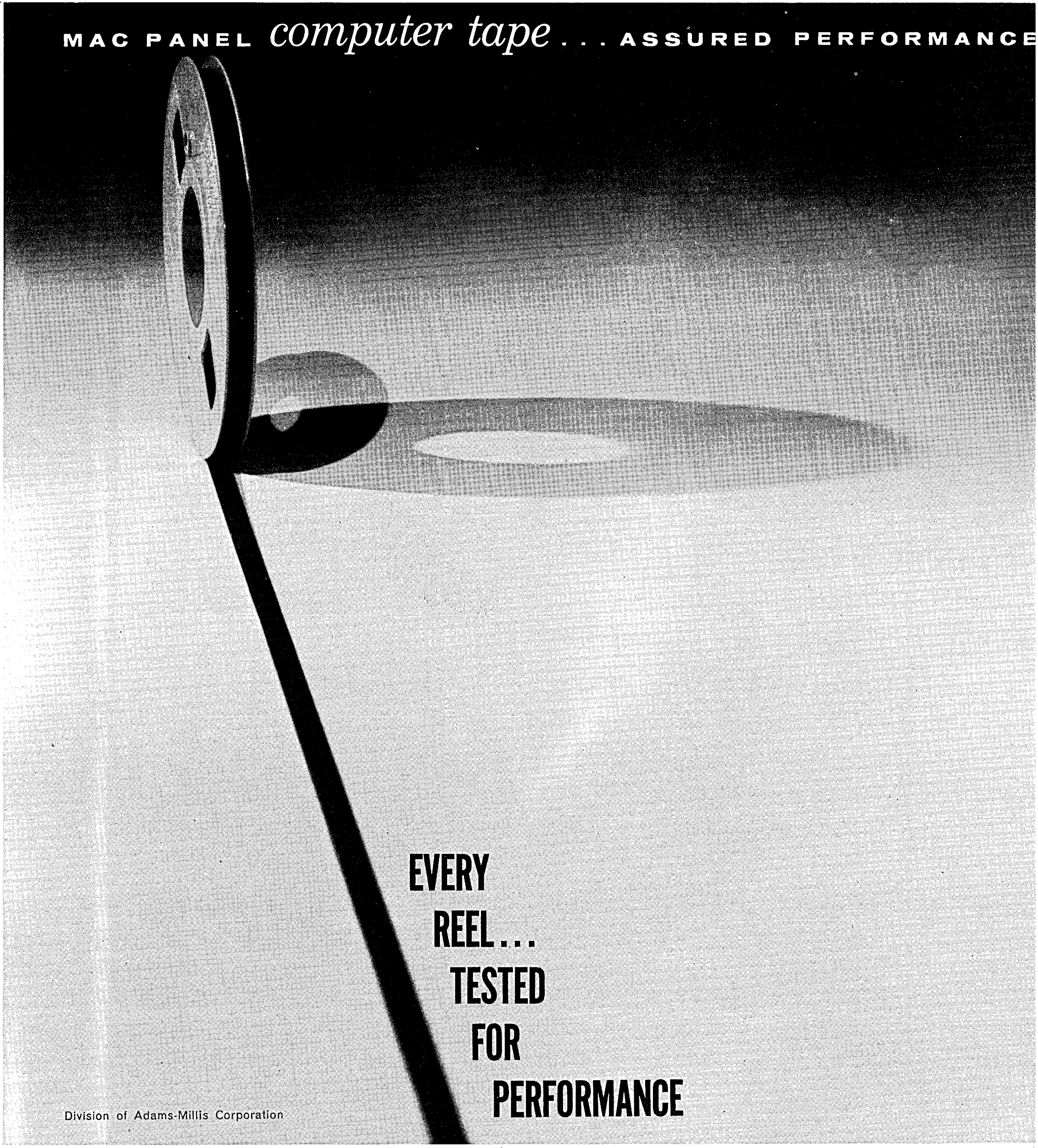
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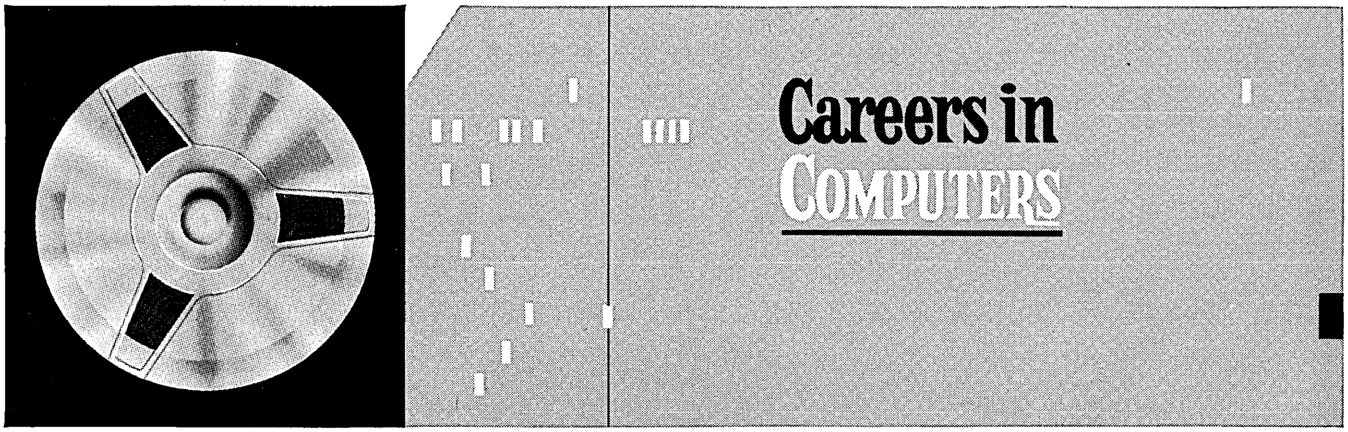

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*DATA MANAGEMENT . . . *Recruiting Specialists for Data Processing and Computer Personnel Exclusively.*

NEW FIRMS & mergers in DP

Data Systems Corporation, a new firm which will specialize in the development of custom-engineered peripheral systems and computer modification, has been formed by E. I. Blumenthal and F. B. Hannon, both formerly with UNIVAC. Dr. John W. Mauchly, president of Mauchly Associates, Inc., was elected to the board of directors. The firm is located in Valley Forge Industrial Park, Pa.
CIRCLE 111 ON READER CARD

Computer Applications: Software-Hardware, a Corp., is a new consulting firm in Los Angeles, headed by Bob Kerr. Seymour A. Lesonsky, formerly chief of data processing for Los Angeles County, is director of programming.
CIRCLE 112 ON READER CARD

Business Supplies Corporation of America, Princeton, N. J., is a new firm which includes six companies in its organization: Tabulating Card Co., Data Processing Accessories Co., Whiting Stationery Co., Data Processing Supplies Co., American Business Machines Co., and Data Processing Service Co. The principals in the company are Clement V. Conole and L. Stanley Crandall. The latter was president of Royal Precision Corp. until his resignation in April.
CIRCLE 113 ON READER CARD

Computer Accounting Corp., has been established in Massapequa, New York, to provide data processing services to banks and business firms in the Long Island area. Arnold B. Schacknow, formerly manager of the Computational Laboratory at the Arma Div. of American Bosch Arma Corp., is president.
CIRCLE 114 ON READER CARD

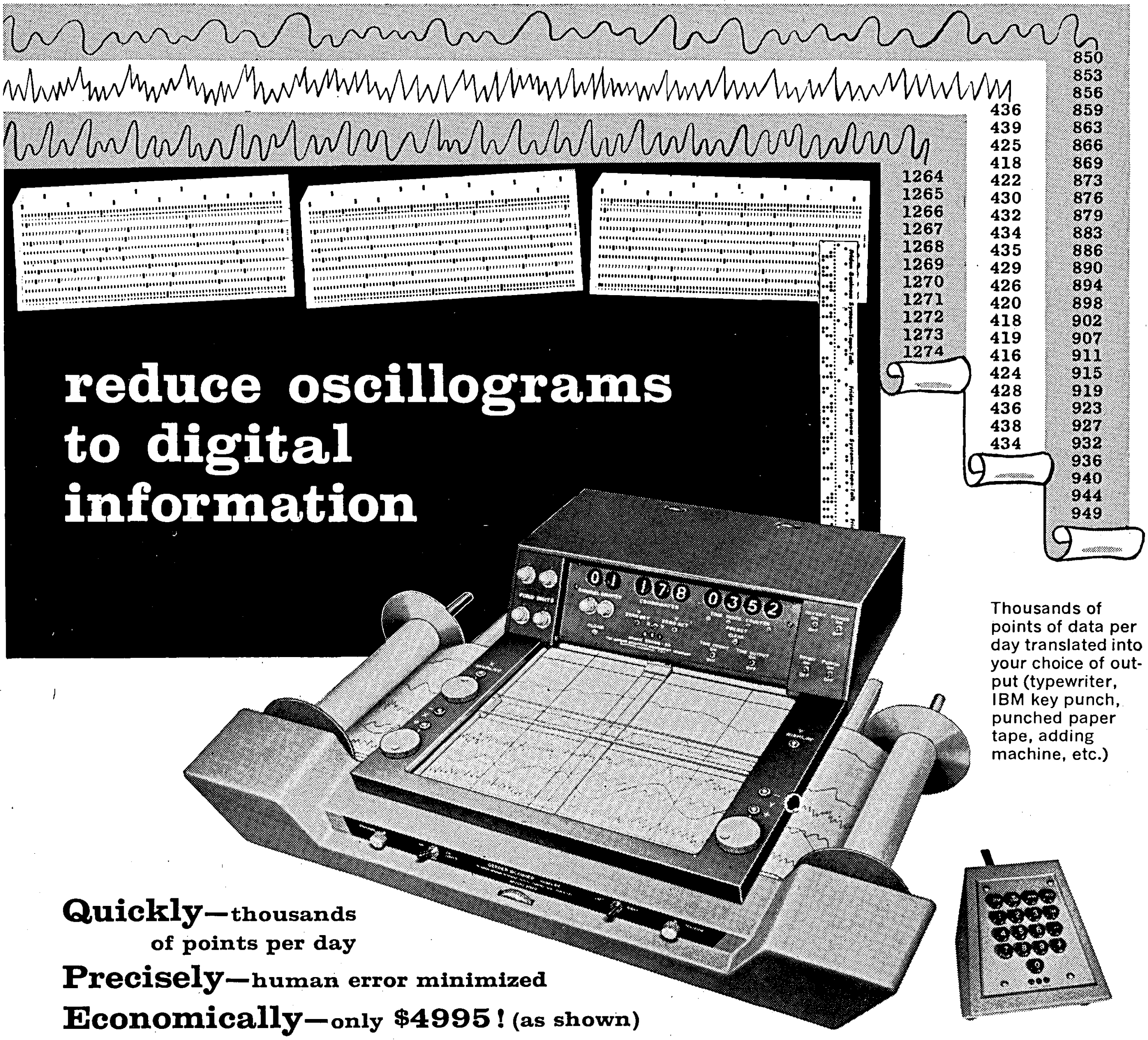
Ampex Corporation has purchased International Computer, Inc., Los Angeles manufacturer of memory components. ICI, formed last year by Witold Modlinski, ICI president, and several others previously associated with Ampex, reported annual sales of approximately $400,000. Modlinski and seven key technical and production personnl have assumed new posts with Ampex.
CIRCLE 115 ON READER CARD

Electro-Mechanical Research, Inc., Sarasota, Florida, has acquired Solartron, Inc., Anaheim, California, which will continue operation as a separate corporation under EMR corporate guidance. Solartron manufactures transfer function analyzers, used in laboratory and field checkout of servo systems. EMR is engaged in the design and manufacture of telemetry and dp equipment for missle and spacecraft testing.
CIRCLE 116 ON READER CARD

Boothe Leasing Corporation, San Francisco, has established a Computer Leasing Division, to be located in New York City. The division will offer guidance and assistance in equipment selection. Services and maintenance will be provided through separate contracts with equipment manufacturers.
CIRCLE 117 ON READER CARD

Codamite Corporation, a new firm located in Anaheim, California, has been announced by R. W. Johnson, president. The organization will specialize in the field of subminiature digital communications equipment. Initial production will involve electronic, keyboard-operated subminiature code generators, while future plans call for subminiature automatic receivers and printers, tape equipment, and desk-top units suitable for remote communication with central computers. CIRCLE 118 ON READER CARD

reduce oscillograms to digital information



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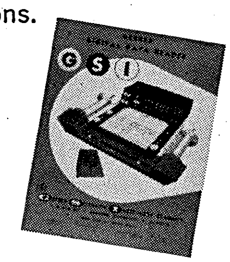
Low-cost Gerber Digital Data Reader saves valuable engineering manhours on essential applications like these:

√ Measuring amplitudes of single or multiple channels having either linear or non-linear calibrations.

√ Measuring at random along the X axis to find the elapsed time from the origin.

√ Measuring amplitudes with a fixed number of counts per inch from a given origin, or with scale factors and offset zero locations.



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CIRCLE 29 ON READER CARD

NEWS BRIEFS

NCR's COMPUTER SALES OVER 100 MEGABUCKS

National Cash Register Co. has reported that it has installed or has on order more than 500 computer systems. The sales value of this equipment is said to be more than 100 megabucks. In its last semi-annual report, NCR pointed to the significance of its sales in edp as an impressive contribution to the overall growth of the company.

The NCR 390, according to the report, has been installed in approximately 150 companies in the U. S. and Canada and 40 firms in 23 overseas countries.

M-H, NIPPON ELECTRIC SIGN COMPUTER TRADE PACT

Nippon Electric Co., Japan's leading manufacturer of dp equipment, will manufacture and market in Japan a full line of Honeywell's computing systems. In return, Honeywell will have access to Nippon Electric's technical data and specifications for its own use.

Under the "Technical Know-How and Patent License Agreement," Honeywell will provide the Japanese firm with technical information and specifications to produce and sell in Japan the 400, 800, 1800, and 290 computers. Also included in the agreement were specifications on I/O devices and software.

1401 COBOL NOW AVAILABLE

The availability of COBOL for 1401 systems with 12 to 16K memories has been announced by IBM. In November, COBOL for 1401s with 4 to 8K memories is scheduled for release.

Previously, IBM had released COBOL for the 1410, 7070-74, 705, and 7080. IBM pointed out that while "several hundred copies of the 1410 COBOL processor are now in the hands of users, a few are doing all their programming with COBOL, but many are experimenting." 1410 COBOL, like all other processors, IBM added, "is not completely error-free." Modifications and improvements are being made "in the light of user experience," and as experience dictates, modifications and new versions are released.

COBOL processors for the 7090/94 and 7040/44 (16 to 32K work storage) are expected to be available during 1962 and third quarter, 1963, respectively.

CIRCLE 100 ON READER CARD

AN ANALOG COMPUTER WITHOUT MOVING PARTS

Using a recently developed electroluminescent-photoconductive combination, a device of smaller size and requiring less power than circuits previously available can be made to obtain rate generation of a modulating voltage. Electronic or electromechanical equipment was needed in the past to perform the same task.

The circuit, developed by William H. Lohneiss and Rubin Boxer, senior systems engineers at Servomechanisms /Inc., Goleta, Calif., is part of an R & D program in which optics and electronics are combined to replace motors, gear trains and potentiometers to obtain a solid state analog computer, which would function without moving parts.

A patent has been granted for the circuit design.

CIRCLE 101 ON READER CARD

C-E-I-R WINS SUIT VS. COMPUTER DYNAMICS

A lower court's ruling against C-E-I-R, Inc., who sought to prevent a rival firm, Computer Dynamics, established by former C-E-I-R employees, from seeking to do business with C-E-I-R's prospective or former clients, has been reversed by the Maryland Court of Appeals.

The court ruled that the former employees, who had been engaged in a 90-day study contract while still with C-E-I-R, were placed in a unique position to compete against the corporation by establishing their own organization while still employed by C-E-I-R and to bid against their employer for the subsequent contract. Further, the court said the former employees should be barred from making such a bid and testimony should be taken in the lower court on the amount of damages due to C-E-I-R.

Among the general principles stated by the court in handing down its decision were: "It is an elementary principle that fundamental duties of an agent are loyalty to the interest of his principal and the need to avoid any conflict between that and his own self-interest . . . an agent is under a duty to disclose to his employer any information concerning the agency which the employer would be likely to want to know. The employee may not before the termination of his employment, solicit his employer's customers for such . . . business."

NAA ORDERS CCC's DDP-19

North American Aviation, Columbus, Ohio, has awarded a $235,000 contract to Computer Control Co. for a DDP-19. The computer will be used for real-time control techniques and navigation simulation. The system is to include a computer satellite digital function generator for on-line solution of trigonometric and hyperbolic functions.

CIRCLE 102 ON READER CARD

● A UNIVAC 1107 is scheduled to be installed in November at the Department of Defense's Electromagnetic Compatibility Analysis Center at Annapolis, Md. The Armour Research Foundation, which has an Air Force contract to study the effects of radio frequency interference upon military radars and communication equipment, will use the 1107 for spectrum signatures analysis.

CIRCLE 103 ON READER CARD

● An ASI 210 W system has been delivered to Argonne National Laboratory, Argonne, Ill., by Advanced Scientific Instruments, Inc., Minneapolis. The system, sold at a reported price of slightly more than $117K, is a modified ASI 210.

CIRCLE 104 ON READER CARD

● Thompson Ramo Wooldridge, Inc., will build 29 computers and associated dp equipment under a 4.5 megabuck contract awarded by Sperry Gyroscope Co. The units will be part of an operational high-accuracy

DISCfILE is a trademark of *data products corporation*

Meet the DISCfILE:™ newest mass random access memory — now on the job in customer systems

At work on-line: latest and most effective solution to a wide variety of problems demanding fast, random access to large masses of stored data—the DISCfILE by *data products corporation.* Applied to any digital data system, the DISCfILE multiplies capacity by orders of magnitude, while simultaneously shrinking space requirements.

Reliable, readily-integrated dp/f-5020 DISCfILE systems are being delivered in capacities from 35 to 155 million bits, at costs-per-bit of 1/15 to 1/7 cent. With average access speed of 225 msec., these systems deliver: high density, 400-bits-per-inch recording; individually addressable, linear head positioners for each disc; exceptional programming flexibility; successive records accessed without interrupt; fixed heads for 26 msec. average data access; and easy, on-site maintenance.

This is the DISCfILE: first in a new and unified line of technologically advanced data input/output/storage equipments from *data products corporation.* For technical data and the DISCfILE Game, newest and most sophisticated form of an ancient numerical diversion, write on your letterhead to: *data products corporation*/Room 812
8535 Warner Drive
Culver City, California
Phone: 837-4491

navigation set for the Navy's Fleet Ballistic Missile Weapon System. Deliveries will start this month, and continue through late 1963. System components consist of the CP-677/BRN-3 Digital Processing Computer, CV-1296/BRN-3 Digital Data Processor, computer writer adapter, and paper tape reader and punch.

● A Honeywell 800 and two 400s will be used for manufacturing and inventory control applications in connection with NASA's Project Apollo. The two megabuck contract calls for the systems to be operative by October 1, 1962, in the Data Computing Center at Slidell, La.

CIRCLE 105 ON READER CARD

● Data Products Corporation, Culver City, Calif., has received a contract in excess of $300,000 for an unspecified number of DISCfile systems to be used in conjunction with the U. S. Army's project ACSI-MATIC.

● A computer-oriented war gaming model will be produced by the Datatrol Corp., Silver Spring, Md., under the terms of a $66,000 contract awarded by the Department of Defense Damage Assessment Center. The model will simulate pre-war and post-attack operations of offensive nuclear forces according to pre-planned strategies.

● Electronic Associates, Inc., Long Branch, N. J., has been awarded a $679,000 Air Force contract to build a large-scale analog computer system for simulating various aspects of the X-20 (Dynasoar) space program. The system, to be installed at the Air Force Flight Test Center at Edwards Air Force Base, Calif., will consist of three PACE 231R gp analog computers, each capable of being programmed independently.

CIRCLE 106 ON READER CARD

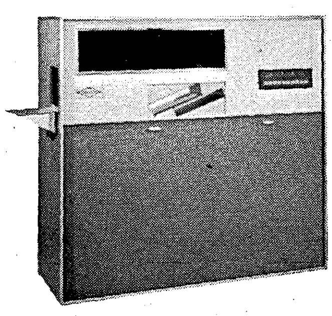
● An IBM 7090-1401 system has been ordered by the University of Maryland for its new Computer Science Center. Delivery is scheduled for early 1963. Dr. Werner C. Reinboldt has been named director of the center.

● Control Corporation, subsidiary of CDC, has received a contract to double the size of its 8000 Series Digital Control System installation, cur-

Send me a machine that can read!

A machine that can read source documents and be on the job everyday. The pile of documents mounts higher and all have to be read and translated into computer language. **PROBLEM:** How to eliminate the input bottleneck and tell the computer *quickly, most economically,* and *100% accurately,* what it must know?

SOLUTION: The Farrington Optical Scanner, such as the Model 1P below, the machine that reads pages, up to legal size and translates the data *fast* into computer language: punched cards, punched tape, or magnetic tape. Farrington Optical Scanners are now solving this everyday problem every day for TIME INC., U. S. AIR FORCE, and others.



for further information, write Farrington Electronics Inc.

7019 Edsall Road, Alexandria, Virginia

16 out of every 17 reading machines in use today are by FARRINGTON®

CIRCLE 30 ON READER CARD

rently used to control the flow of natural gas in a major pipeline complex. The addition of three satellite stations is part of a proposed system for an ultimate 128 remote stations, including a computer at the master station.

CIRCLE 107 ON READER CARD

● A mobile process control center, containing a TRW-330 computer, has been leased by Phillips Petroleum Co. The firm plans to use the system for special measurements, data logging, analysis, and process control functions, and can be connected directly to equipment in its plants.

CIRCLE 108 ON READER CARD

● Dr. Harry W. Mergler, associate professor of engineering at Case Institute of Technology, has demonstrated a new technique which transforms human speech into numbers or digits that can be input to a computer. These numbers in turn can be reconstructed to form the original sound or word signal. Further work will be aimed at transforming alpha-numeric sound signals into digital signals in a form suitable for machine recognition.

● A Honeywell 400 will be installed at the University of Southern California's Computing Sciences Laboratory, replacing a UNIVAC SS 80. The Laboratory also has an H-800 in operation.

● Harvard University will establish a new Computing Center this Fall and will utilize an IBM 7090, currently in operation at the Smithsonian Astrophysical Observatory. Named to direct the Center was Frank Engel, Jr. who has been with Westinghouse as an advisory engineer with the Advanced Systems Engineering and Analytical Department.

● Honeywell's first Computer Service Bureau in Canada was opened in Ottawa recently, with a second center scheduled to be opened in Toronto in late summer. The Ottawa bureau is equipped with an H–800.

● CUBE (Cooperating Users of Burroughs Equipment) is expected to be the new name of the organization formed by the merger of two existing Burroughs users groups, DUO and CUE. The merger meeting will be held October 24-26 at the Statler Hilton Hotel, Los Angeles. The new

On Thursday, June 21, 1962, your machine accounting equipment became obsolete.

What happened?

We came up with the world's first self-contained reader-printer-processor with magnetic-core memory.

The UNIVAC® 1004 Card Processor.

The first major advance in punched-card accounting in over ten years.

Not just *our* first major advance.

The only one in the entire industry.

The UNIVAC 1004 Card Processor is the missing link between conventional punched-card equipment and electronic computers.

What does it do?

To begin with, the UNIVAC 1004 System will do everything conventional machine accounting equipment will do —*as much as four times faster*.

It will read, print and compute in one card pass.

It reads up to 400 cards a minute.

80 *and* 90 column cards.

It prints up to 400 lines a minute.

It will perform as many as nine operations in one program step.

A full line of 132 characters can be edited, spaced and punctuated in the same step that transfers data to print storage.

Punctuation includes such symbols as dollar signs, decimal points, asterisks, total and sub-total signs.

The Chairman could read a report from the 1004.

But the most important development in the UNIVAC 1004 is its processing ability.

Its magnetic-core memory is actually faster than that of many medium and large-scale computers. Access time: 8 microseconds.

Now if you bear in mind that when the 1004 is reading for all it's worth, it still leaves itself 35,000 microseconds of compute time after each card read —enough for, say, 200 six-digit additions—you'll get some idea of its potential.

It adds, subtracts, multiplies and divides far faster than any punched-card calculator.

Its totalling capacity is more than three times that of the largest conventional card-accounting machine.

The magnetic-core memory has 961 storage locations. These are never occupied by program instructions. They're always available for computations.

(Up to 75% of the memory space of many computers is taken up by the program.)

What doesn't it do?

It doesn't take up a lot of space, for one thing.

Its vital statistics are 67″—55″—63″.

If you run a tape measure around the equipment you have now, you'll get a rough idea of the space you'll save.

(Don't forget to include the space *between* your present equipment.)

Another thing.

The UNIVAC 1004 Card Processor is *not* a stripped-down computer.

It was designed from scratch to be exactly what it is.

A card processor.

The way it's programmed is an excellent example of this.

The UNIVAC 1004 is programmed on an *external* plugboard.

The sort your present operators are used to.

So they'll need only a smidgen of instruction before they can get to work.

Who needs it?

Any business that's using (or thinking of using) punched-card equipment should find out about our UNIVAC 1004.

The chances are that it will save you a barrel of space, time and money. And do a lot of jobs your old machines couldn't.

Maybe yours is one of the 25,000 businesses whose punched-card machines just aren't up to scratch.

How can you increase capacity *and* efficiency?

You've got it.

With the UNIVAC 1004 Card Processor.

And if you're renting a stripped-down EDP system (or even a medium-scale one), you might well find that one little 1004 will do the same job.

How much does it cost?

It comes in three models.

They cost from $46,000 to $60,000 (plus tax), if you'd like to own one.

Monthly rentals range from $1,150 to $1,500 (plus tax).

A good deal less than you'd pay for the machines you'd need to do a similar amount of work.

How soon can you get one?

Since we already have a stack of orders to fulfill, delivery may take a little while.

Instead of pacing up and down till then, sit down and read a few brochures about the UNIVAC 1004.

Write or call your local Univac Office and we'll gladly send them.

organization will be open to users of B200 and B5000 series systems as well as 205 and 220 computers.

● Applied Data Research, Inc., Princeton, N. J., has issued a call for papers for a Sort Symposium the firm is sponsoring, to be held in late November. Papers may be directed toward, but not limited to, the following areas: the influence of sorting on hardware design; new sorting techniques; the relationship between sorting techniques and equipment. Date and place of the symposium will be announced later. Papers should be addressed to Martin A. Goetz, Sort Symposium, Applied Data Research, Inc., 759 State Rd., Princeton, N. J.

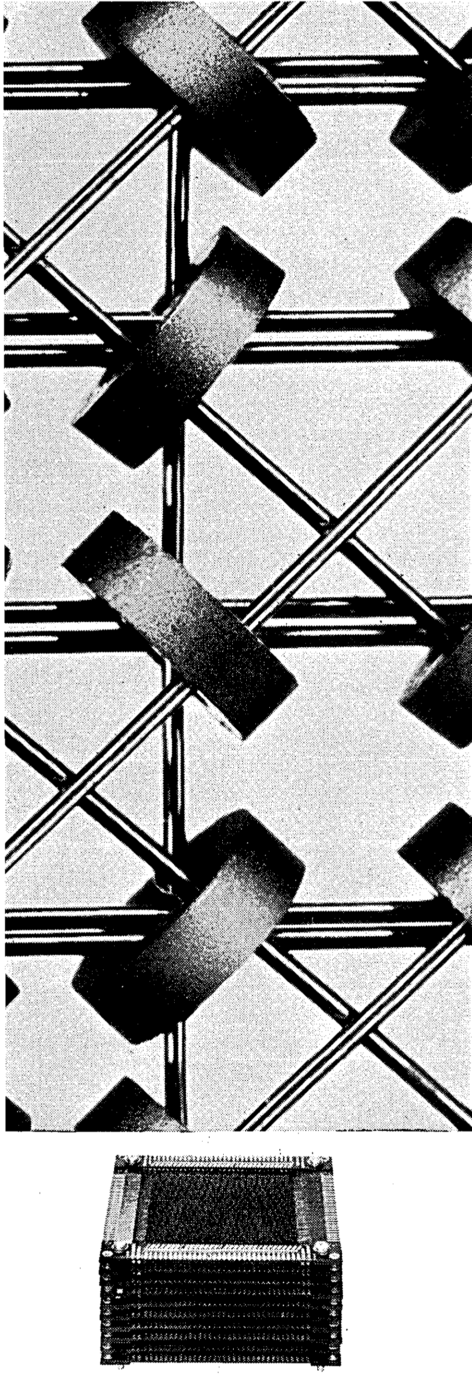
● Corporate headquarters for IBM will be moved to a permanent location in Armonk, N. Y., during the second quarter of 1963. About 200 headquarters personnel, presently at the research center in Yorktown, and 800 employees now located in the IBM building in Manhattan will be included in the move.

● What is described as a complete automatic programming system for computer control of industrial processes has been announced by Honeywell's Special Systems Division. The new technique, termed CLEAR (Compiler, Executive Program, Assembler Routines), was devised specifically for the Honeywell 290. Included in the system is a compiler, called FAST (formula and statement translator) and an assembler. The compiler accepts most FORTRAN written programs without conversion, and the assembler accepts a mixture of computer languages, merges them into one main program, and produces a perforated tape in machine language.

CIRCLE 109 ON READER CARD

● A UNIVAC 1107 is scheduled to be installed in Case Institute of Technology's Computing Center early in 1963. The 1107 will replace a UNIVAC I, which has been in use since 1958. The machine will be made available to Case through the RemRand educational program, which offers edp equipment at a substantial discount to selected educational institutions.

● A five-year study recently concluded at Harvard presents new ways to design and coordinate the financing, engineering and govermental plan-



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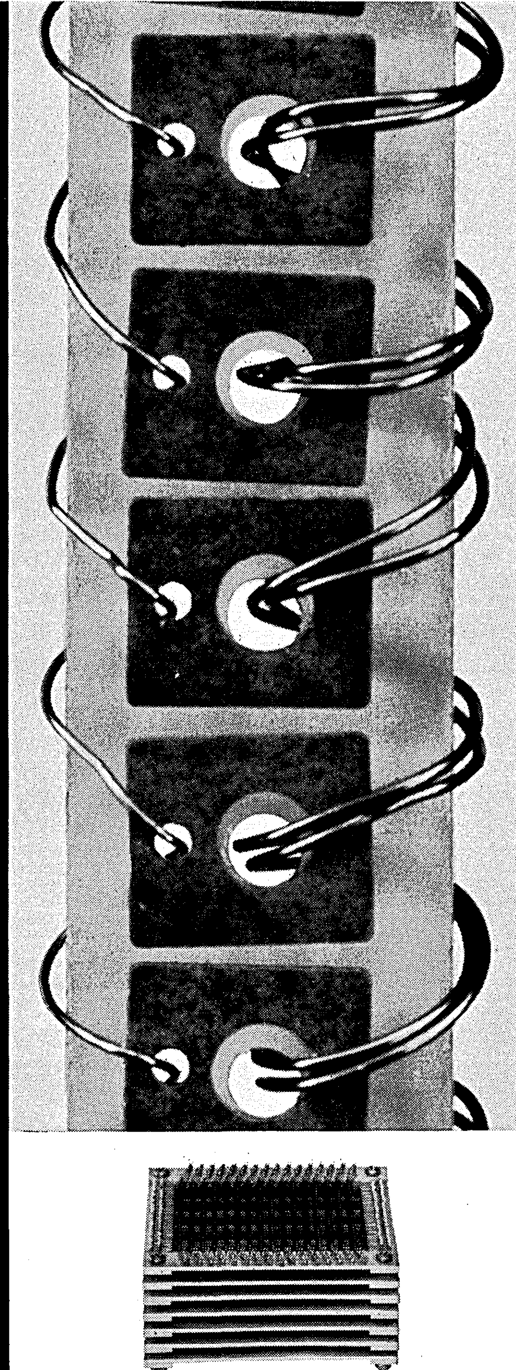

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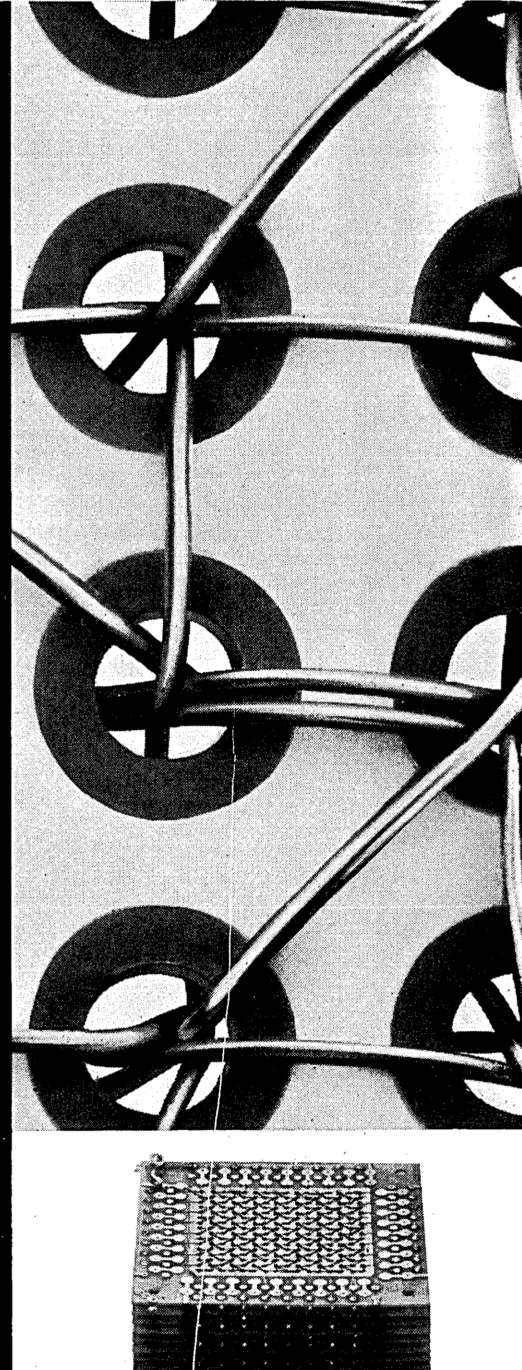


3.

PRODUCTS PHOTOMACROGRAPHED APPROXIMATELY 30 TIMES ACTUAL SIZE

close-up of maximum reliability

Lockheed Electronics' in-house capability produces ferrite cores, multi-aperture devices, printed circuit boards, memory planes and stacks, plug-in circuit modules, and fabricated metal casings. Every step from design through test is under one management to assure maximum quality control and minimum cost.

The enlarged photos above show three of the many types of memory plane assemblies produced by Lockheed Electronics.

1. Standard commercial open frame ferrite core memory plane utilizing either coincident current or linear select wiring.

2. Lockheed designed memory array using multi-aperture cores to provide non-destructive readout. This unique method of mounting and wiring provides the necessary rigidity for severe environmental applications.

3. Memory plane with conventional ferrite cores using imbedded assembly and wiring techniques to meet exceptionally high environmental shock and vibration requirements of military specifications.

For further information on Lockheed cores, memory planes and stacks, or printed circuitry to fill your particular requirements, write: Lockheed Electronics Company, 6201 East Randolph Street, Los Angeles 22, California.

LOCKHEED ELECTRONICS COMPANY

A DIVISION OF THE LOCKHEED AIRCRAFT CORPORATION

CIRCLE 33 ON READER CARD

ning of river works. During the project, researchers used an IBM 704 to alter the flow of a hypothetical river to create a design that would yield the greatest net benefit to a community or nation. The river system included dams, reservoirs, flood control works, power stations and irrigation canals.

● An information updating and retrieval system called Tellertron has been put into operation at the Provident Institution for Savings, Boston. Developed by Stone Laboratories, Inc., Boston, the system presents visually the condition and balance of accounts. A memory connected to teller posting machines by a series of control units operates the system, and contains account number, status, stop payments, unposted interest and balance.

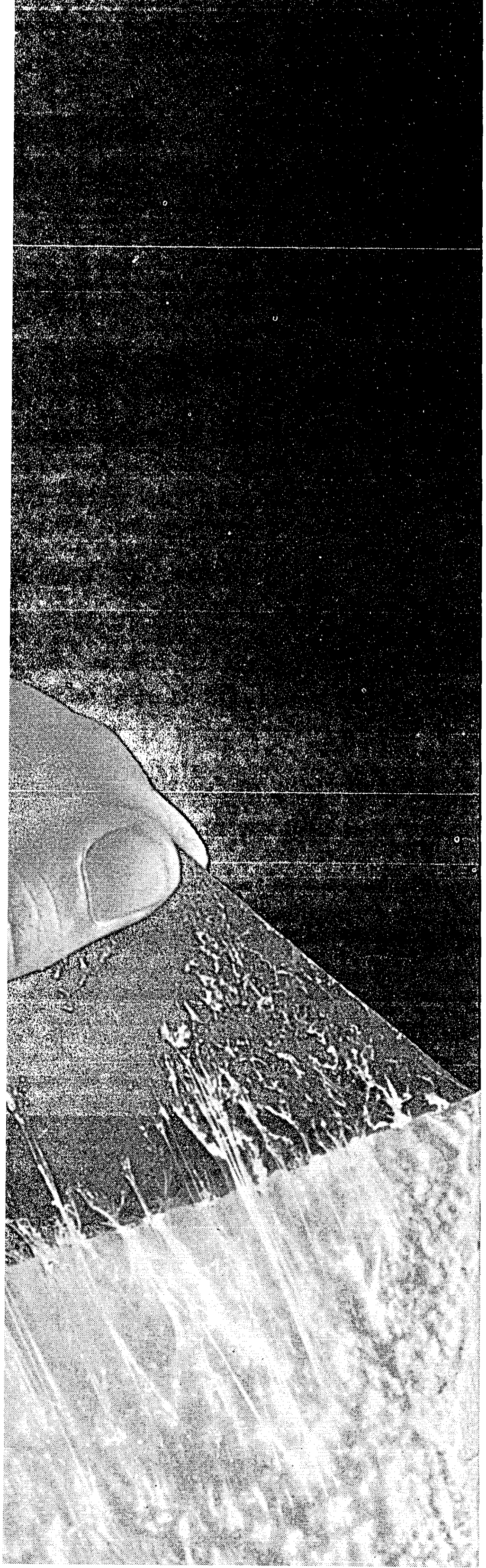
CIRCLE 110 ON READER CARD

● A discount supermarket in Nice, France, distributes IBM punched cards with each purchase which shows the discount price, standard price and description of the merchandise. When the shopper reaches the checkout counter, an IBM tabulating machine receives the punched cards and prints an itemized invoice, giving the total discount price and compares it with the total standard price.

● The first dp system in the garment industry will be installed by the H. D. Lee Co., manufacturer of work, utility, and play clothing. The system will be built around an NCR 315.

● The EDP Newsletter, published by Chicago Teachers College—North, is a new entry in the dp publishing field. Published six times yearly, the Newsletter covers the use of dp in education. Price of the publication is $5.00 for six issues. The publication office is located at Chicago Teachers College—North, 5500 N. St. Louis Ave., Chicago 25, Ill.

● Experimental programs for mechanized information retrieval on pulp and paper problems have been initiated by The Institute of Paper Chemistry, Appleton, Wisc., and the Pulp and Paper Research Institute of Canada, Montreal. The two groups will be conducting separate but coordinated experiments with various system configurations. The experiment is expected to result in a suggested sys-



One of a series briefly describing GM's research in depth

Adhesion: describing an elephant of science

Adhesion has certain similarities to the elephant the blind men were asked to describe. This interdisciplinary subject has occupied the talents of the physicist, chemist, mathematician, metallurgist, and polymer scientist. But still, what adhesion is—its mechanisms and principles—seems to have eluded an overall scientific theory. Perhaps not for long.

Food for inductive thought is being gathered from fundamental research studies around the world. At the General Motors Research Laboratories, for example, recent experimental work by our polymer scientists has supported the idea that adhesion is dependent on:

(1) specific chemical groups in the adhesive film

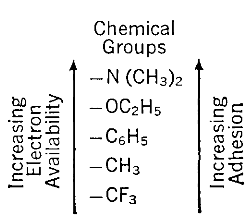
(2) surface roughness of the metal substrate to which the polymeric film adheres.

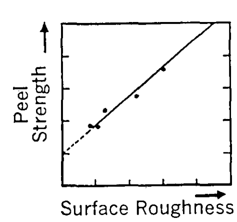
Particularly, through a range of polymers synthesized in the lab, they have found that the more available the electrons in the chemical groups, the stronger the adhesion. Similarly, the rougher the metal surface, the more force required to break the adhesive bonds between the polymeric coating and the substrate.

This experimental approach is enriching our understanding of some of the fundamentals affecting adhesion. It is also finding practical use in General Motors, helping in improving the adhesion of paint, rubber, plastics, and metals to each other. It's another example of GM's continual quest for—A BETTER WAY.

General Motors Research Laboratories

Warren, Michigan





NEWS BRIEFS . . .

tem for paper manufacturers, regardless of the firm's size. For small collections, manual use of index cards will suffice. Larger firms may want to duplicate the mechanized systems of IPC and PPRI which will center around the IBM 1620.

● RemRand UNIVAC has formed a Systems Programming Department which will prepare programming packages for all new UNIVAC systems, make major additions to existing packages, and organize and write programming manuals for direct field distribution. Dr. Werner W. Leutert is director of the new department, reporting to Jay W. Schnackel, vice president and general manager of RemRand UNIVAC.

● Two IBM 1401 RAMACs will be used at the 1964 Olympic Winter Games at Innsbruck, Austria, to keep a running account of the scoring at the various sporting events which will be taking place simultaneously. The computers will be linked by direct lines to remote input terminals at each of the various event sites, so that times or judges' points can be relayed directly for processing.

● Thirteen district sales offices of the National Tube Div. of U S. Steel Corp., will be linked to GE 225 computers at Ellwood City, Pa., and Gary, Ind. to provide greater efficiency for quoting customer inquiries. The computers will be combined with an information-accumulation and transmission system hooked into a teletype network connecting the sales offices.

● The Telefile Savings Account System, made by the Teleregister Corp., Stamford, Conn., was recently put in operation at the Howard Savings Institution, Newark, N. J. The service allows tellers at all branch offices immediate access to 290K savings accounts stored in drum memory. The sorting and master report production control programs for the system were developed by National Computer Analysts, Inc., Princeton, N. J.

● A. J. Whitmore, Westinghouse Corp., has been named chairman of a subcommittee of the maintenance committee of CODASYL (Conference on Data Systems Language) which will be responsible for developing specifications for table handling and mass storage functions in COBOL. When the specifications are approved by the maintenance committee, they will be added to the existing COBOL language.

● A contract to produce a single interpretive system for the ASI-210 computer which will accept computer programs written in any of three source languages — Intercom 1000-S, Intercom 1000-D and 500-X, originally implemented on the Bendix G-15—has been awarded to the Datrol Corp., Silver Spring, Md., by Advanced Scientific Instruments, Inc., Minneapolis.

clarification

Listed as involved with Midwest Tech in a news report appearing in the June issue of DATAMATION was Kauke & Co. While the report is correct since Kauke & Co. received considerable financial assistance from Midwest Tech, the impression may have been conveyed that Kauke & Co. was named in the SEC suit. This is incorrect and no such impression should be drawn since no employee or director of Midwest Tech has ever purchased, held or sold a share of stock in Kauke & Co.

NEXT MONTH IN DATAMATION

Rated as one of the more widely discussed, annual gatherings of industry leaders, the 1962 RAND Symposium will receive DATAMATION's principle editorial spotlight in October. The subject: Programming Languages.

Also on tap is a stimulating commentary on "Benchmarks in Artificial Intelligence;" a report on IFIP, and some on-the-scene observations and photographs of Russian computers. For the hardware oriented, DATAMATION will offer "Computer Memories" — with remarks on possible future developments by Jan A. Rajchman, a fitting accompaniment to the concluding part of the Burks, Goldstine and von Neumann paper.

Finally, for the foolish and disheartened, the final segment of our Kludge series is scheduled on a user's view of KKK.

EAST
VS.
WEST

DIAGRAMS
VS.
EQUATIONS

THE COMPUTER'S ANSWER TO A LONG-STANDING COMPUTER ISSUE.

For a decade East Coast and West Coast computer designers have been using different methods of representing computer logic—the Easterners with diagrams, the Westerners with equations.

LBSMI=
(LXA1)(LXA2*)(LFCA*)
+(LXA1*)(LXA2)(LFCA*)
+(LXA1*)(LXA2*)(LFCA)
+(LXA1)(LXA2)(LFCA)
LFCAJ =
(LXA1)(LXA2)
LFCAK =
(LXA1*)(LXA2*)

In the example illustrated here, the diagram and the equation tell us exactly the same thing. Either represents a serial full adder where the sequence of pulses at the output, LBSM, will represent a serial binary number that is the sum of two serial binary input numbers occurring at LXA1 and LXA2. (The asterisks indicate binary complements; for example, whenever LXA1 is energized LXA1* is not, and vice versa. LFCA is a carry flip-flop.)

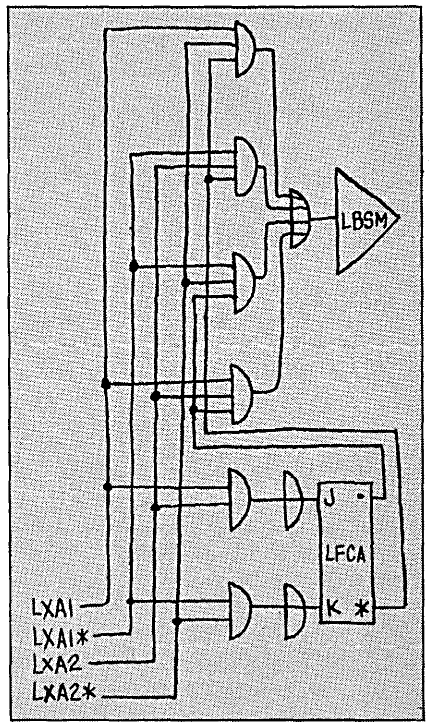
There are persuasive arguments on both sides. Eastern proponents of diagrams point out that the logical interconnections can be seen at a glance and followed through any number of stages by eye. The logical structure of an entire system can be understood from a diagram more directly and intuitively, they maintain, than from a set of equations.

The Western argument for equations goes like this. It's not true that diagrams communicate better to the viewer's intuition, except at first exposure. The human mind is highly adaptive. After working analytically with the equations for a while, the mind begins to operate intuitively in that symbology. Then the intrinsic superiority of equations over diagrams begins to make itself evident. One advantage, say the Westerners, is that equations can represent the same information more compactly and efficiently, as our illustration shows. Another is that equations lend themselves better to computer manipulation of logical design information.

As evidence of the latter advantage Westerners point to a recent achievement of some Litton Systems people: a completely mechanized procedure for translating logical designs into wiring lists, including operational simulation of the design to verify its accuracy. A procedure enormously facilitated by the computerizability of logical equations. It's easy to picture the benefits in cost, delivery schedules, reliability, price. Using only a partial development of this method Litton Systems recently brought a major computer system from concept to operation in less than a year.

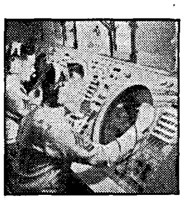
Now under consideration at Litton: a machine that will accept as inputs a supply of standard computer components and a set of coded specifications defining the logical functions desired, and will crank out completely fabricated systems.

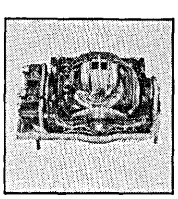
Maybe you think we've loaded the argument in favor of equations. You're right. But we're ready to listen to arguments on either side. Drop us a card. Or better still, drop in in person. You'll like the



imagination-stretching atmosphere generated by Litton management's appreciation of the rewards of creative controversy. We have a few excellent opportunities for computer design people. Ask for Harry Laur at Litton Systems, Inc., Data Systems Division, 6700 Eton Ave., Canoga Park, California.

An equal opportunity employer





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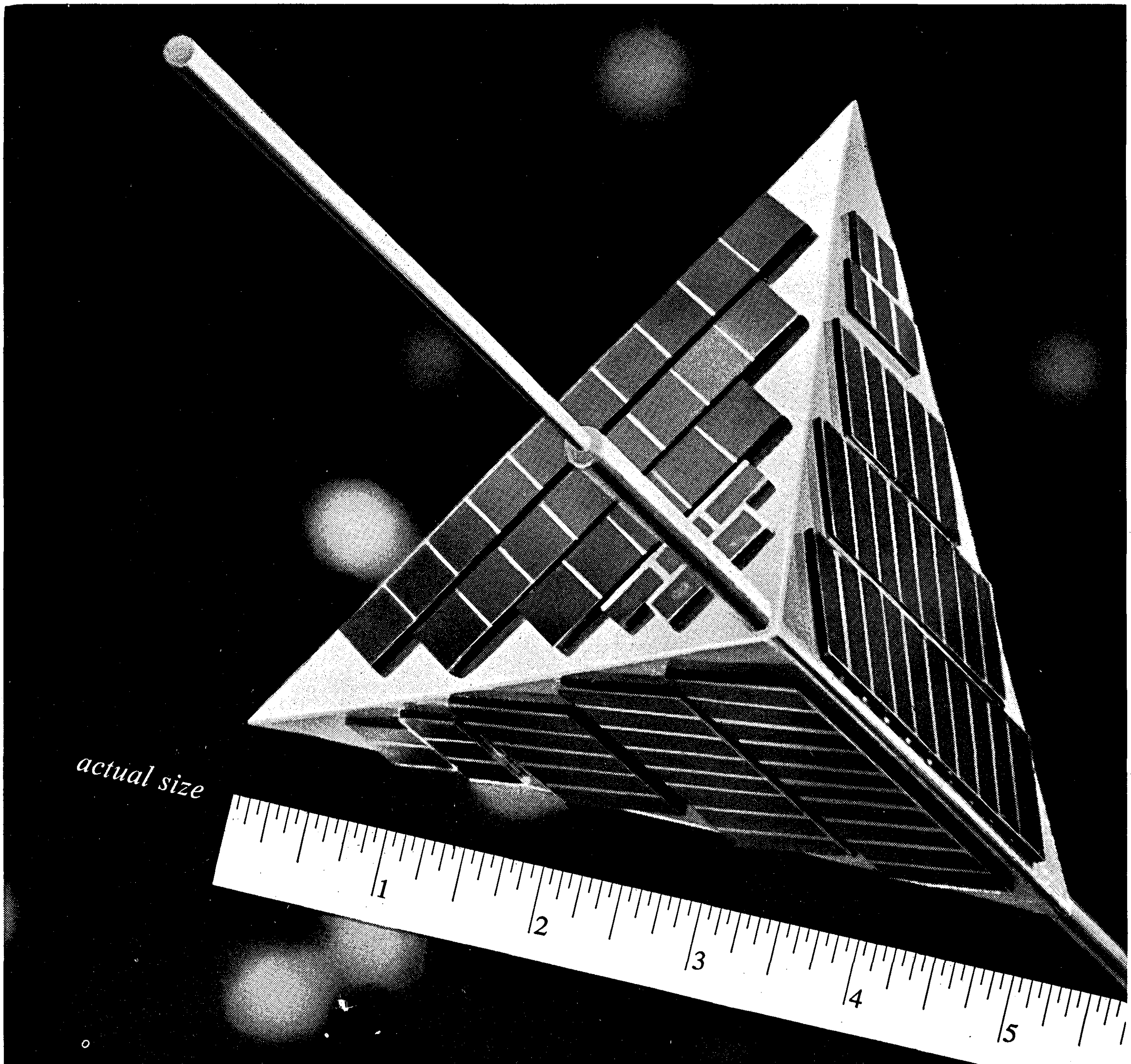
DATA HANDLING & DISPLAY SYSTEMS · GUIDANCE & CONTROL SYSTEMS · COMPUTER SYSTEMS · SPACE SCIENCE · BIOELECTRONICS · ADVANCED COMMUNICATIONS TECHNOLOGY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NEW LITERATURE

INFORMATION PROCESSING GLOSSARY: This 110-page reference manual contains lists of both general and special terms, definitions for over 1,000 terms, definitions of over 500 acronyms and other abbreviations, 35 groups of inverted terms, and a bibliography of glossaries for information processing. IBM CORPORATION, DP DIV., 112 E. Post Rd., White Plains, N. Y. For copy:

CIRCLE 130 ON READER CARD

MICRO: An illustrated bulletin describes this miniaturized digital computer for aerospace, defense and industrial applications, and presents packaging, production and component techniques. Specifications, performance parameters and applications are included. AMERICAN BOSCH ARMA CORP., Roosevelt Field, Garden City, N. Y. For copy:

CIRCLE 131 ON READER CARD

SPEDAC: This brochure presents the applications, advantages, theory of computation and operation of this digital differential analyzer. HAZELTINE CORP., TECHNICAL DEVELOPMENT CENTER, Weir Cook Municipal Airport, Indianapolis 41, Indiana. For copy:

CIRCLE 132 ON READER CARD

G-21 COMPUTING SYSTEM: This illustrated, 16-page brochure contains discussions on command and control systems, macro system, system equipment, information flow, programming, command complement, execution times, internal characteristics and internal checking. THE BENDIX CORP., COMPUTER DIV., 5630 Arbor Vitae St., Los Angeles 45, Calif. For copy:

CIRCLE 133 ON READER CARD

PLOTTING NEWSLETTER: This bi-monthly bulletin is devoted to information on computer-controlled digital graph plotting techniques and applications. CALIFORNIA COMPUTER PRODUCTS, INC., 8714 E. Cleta St., Downey, Calif. For copy:

CIRCLE 134 ON READER CARD

DIGITAL DATA RECORDER: This leaflet highlights the model 1, high-speed data system to be utilized in the reduction of analytical data to a suitable form for computer input. Use, performance and specifications are included. PERKIN-ELMER CORP., Norwalk, Conn. For copy:

CIRCLE 135 ON READER CARD

LINE PRINTER: This 12-page brochure includes general information and specifications of the H-207. The printer's speed ranges from 150 lines per minute (64 character format) to 685 lines per minute (ten character format). HOLLEY COMPUTER PRODUCTS CO., 11955 E. Nine Mile Rd., Warren, Michigan. For copy:

CIRCLE 136 ON READER CARD

P. S. Computape doesn't really talk, of course. But in a computer, Computape *reliability* will deliver its own message. New COMPUTAPE, the premium quality computer and instrumentation tape, is the product of the only company devoted exclusively to the manufacture of quality tapes for data processing and instrumentation. *Investigate new Computape today. Better still, immediately.*

Send today for your free magnetic tape booklet.

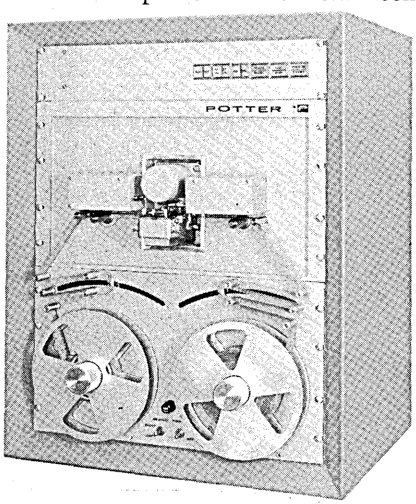
COMPUTRON INC.
122 Calvary Street, Waltham, Massachusetts

CIRCLE 40 ON READER CARD

NEW PRODUCTS

tape reader and spooler

The PTR-500 perforated tape reader and the PTS-500 perforated tape spooler features the new MONO-BRAKE tape stop system which, it is claimed, eliminates tape buckling and bounce at the tape read station. Also featured is photo-electric solar cell



sensing for bi-directional reading, dual speed combinations, and optical end-of-tape sensing circuits. At a tape speed of 50 inches per second, start time is eight milliseconds. Cost of the unit is approximately $2,930. POTTER INSTRUMENT CO., INC., 151 Sunnyside Blvd., Plainview, L. I., N. Y. For information:

CIRCLE 200 ON READER CARD

mag tape drives

These new drives, developed for use with the H800, read and write at the rate of 48K decimal digits or 32K alphanumeric characters per second. Monthly rental is $550 and sale price is $26,400. HONEYWELL EDP, 60 Walnut St., Wellesley Hills 81, Mass. For information:

CIRCLE 201 ON READER CARD

magnetic tape system

This system has been designed for use with the 130 "Stored Logic" digital computer. A single magnetic tape set consists of a 192 magnetic tape controller and one to four 170 tape units. Controls on the 192 permit selection of tape recording densities of either 200 and 556 bit rows per inch. Each bit row carries six information bits and a lateral parity bit. Speed of tapes past the heads is 75 inches per second, with a transfer rate of 90,000 bits per second at low density, and 250,000 bits per second at high density. THOMPSON RAMO WOOLDRIDGE, INC., 8433 Fallbrook Ave., Canoga Park, Calif. For information:

CIRCLE 202 ON READER CARD

punched tape and reader

The 570 punched paper tape reader and the 520 punched tape perforator are housed with drive motors, shaft position indication, electrical connectors, tension and tape feed switches and are furnished with solid state logic modules. The 570, reading five to eight channel tape, in either direction, can operate at a speed of 50 characters per second. Price for either model is approx. $600. INDUSTRIAL PRODUCTS DEPT., ROYAL McBEE CORP., 850 3rd Ave., New York 22, N. Y. For information:

CIRCLE 203 ON READER CARD

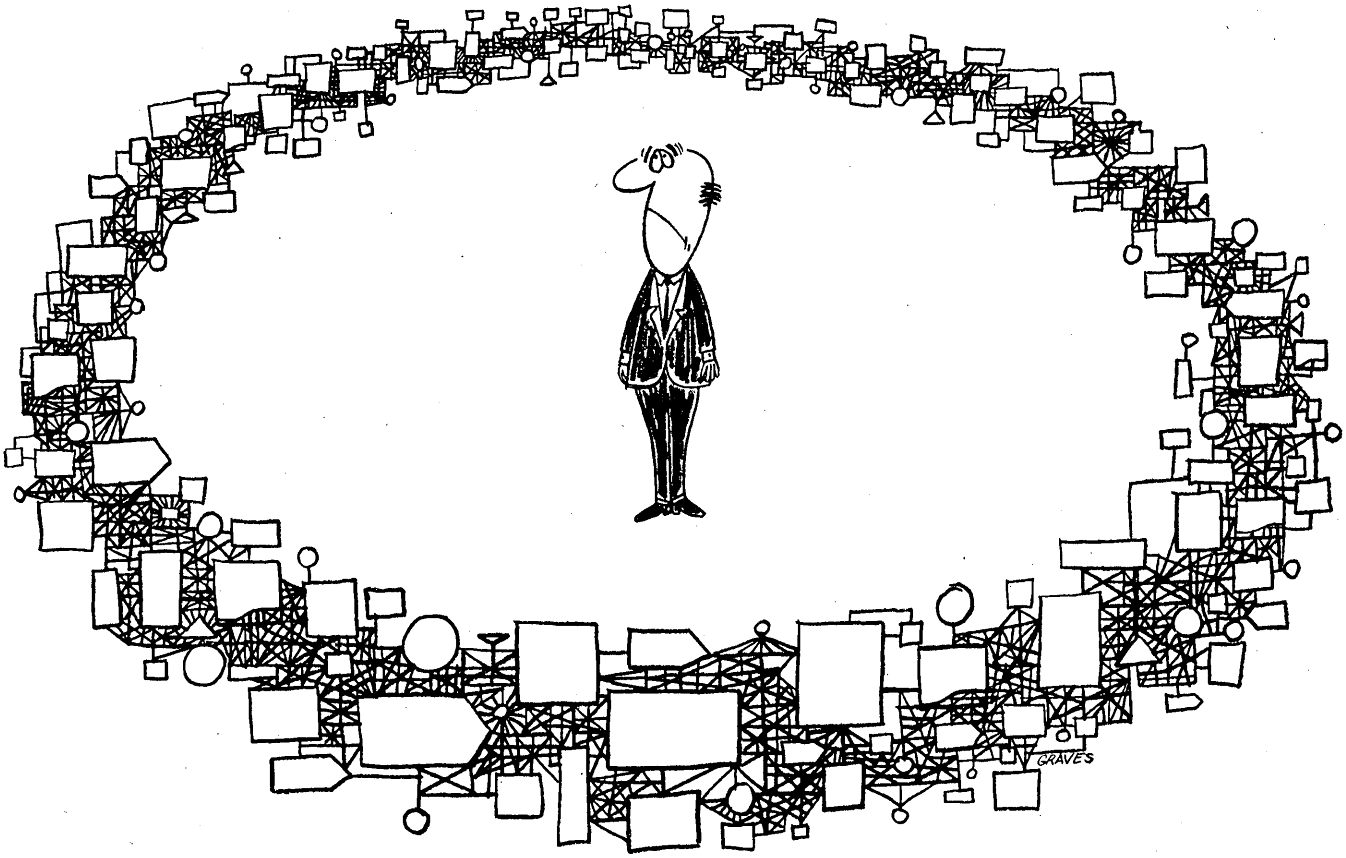
tape package unit

Model 180 consists of punch, reader, tape handling, power supply and printed circuit modules. The reader can be used in any combination with I/O typewriters and can operate either the typewriter or the punch or it can feed directly into the computer. The punch can operate from the typewriter, reader or computer, or from any suitable source. INVAC CORP., 26 Fox Road, Waltham 54, Mass. For information:

CIRCLE 204 ON READER CARD

electrostatic strip printer

This alphanumeric printer, the Omni-Data, model ATR-7, records characters serially on ¼″ paper tape at a rate of 600 cps. Up to four parallel lines may be multiplexed and printed simultaneously on one inch tape. Utilizing a 5 x 7 matrix, semiconductor diodes are sequenced in AND and OR gates to feed information to seven amplifiers



is your programming career in a closed loop?

Have you programmed your career into a corner? Create a loop exit for yourself . . . apply for one of many openings in the area of **AUTOMATIC PROGRAMMING SYSTEMS, MONITORS** and **EXECUTIVE SYSTEMS, SCIENTIFIC APPLICATIONS** and **WRITERS** at Bendix Computer Division.

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CIRCLE 83 ON READER CARD

NEW PRODUCTS . . .

and then on to the seven recording heads which print the appropriate number of dots in each of five columns making up any given character. OMNITRONICS, INC., 511 N. Broad St., Philadelphia 23, Pa. For information:

CIRCLE 205 ON READER CARD

military printer system

Model E 2000 features "hypocycloidal" printing action accomplished by a compound motion of the type drum as it rotates at constant speed of six to 10 lines per second in 12 to 21 columns. Each column displays 12 characters. The system, which operates directly from binary-coded decimal data sources, is priced from $12,500, to $14,900. CLARY CORP., San Gabriel, Calif. For information.

CIRCLE 206 ON READER CARD

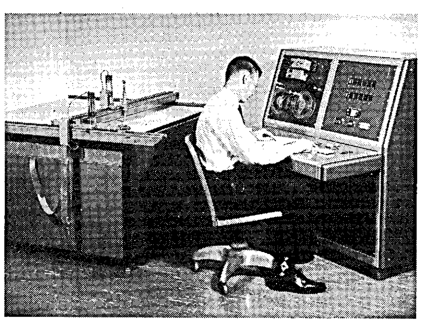
memory system

The SEMA 2000 has been designed to add high speed dp capabilities to accounting machine equipment. Depending on specific requirements, any number of memory drums can be used with the 2000, each drum having a capacitv of 20,000 digits. Price is $22,500. HRB-SINGER, INC., 396 5th Ave., New York, N. Y. For information:

CIRCLE 207 ON READER CARD

Digitork

This solid state plotting and measuring instrument is capable of point-to-point or continuous line plotting. Utilizing Digitork stepping motors as mechanical actuators for the plotting table mechanism programmed plotting over



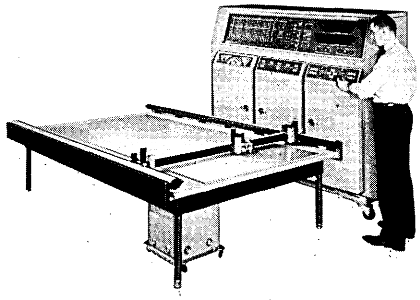
a 47½" x 47¼" surface to ±.0025 of an inch may be accomplished. AERO SERVICE CORP., 210 E. Courtland St., Philadelphia 20, Pa. For information:

CIRCLE 208 ON READER CARD

drafting machine

The Orthomat, a numerically controlled engineering drafting machine can automatically translate complex mathematical formula defined on punched or magnetic tape into engineering drawings at speeds up to 200 inches per minute. It can operate in-

NEW PRODUCTS . . .



dependently or as an integral part of total computer engineering systems, correlating with other numerically controlled data, production and inspection machines. UNIVERSAL DRAFTING MACHINE CORP., 1825 E. 18th St., Cleveland 15, Ohio. For information:

CIRCLE 209 ON READER CARD

stimuli generator

This generator consists of two 3550A 2 mc pulse generators with a built-in sine square wave generator and a 22 kc crystal-controlled oscillator. Outputs include: two independent pulse trains, with pulse repetition rate from 200 cycles to 2 mc; a 10-volt sine wave, with frequency range of 18 cycles to 1 mc; a 22 kc sine wave output, available at two jacks, one a reference, the other variable in phase a full 360° with respect to the reference. SERVO CORP. OF AMERICA, Hicksville, L. I., N. Y. For information:

CIRCLE 210 ON READER CARD

digital indicator

Model 170 provides digital readout on tape or punched cards when operating as a calibration standard for weight, force and thrust measuring systems. GILMORE INDUSTRIES, INC., 3355 Richmond Rd., Cleveland 22, Ohio. For information:

CIRCLE 211 ON READER CARD

single arm plotting board

Model 3305 has been designed for both analog and digital computer applications. Features include isolation of x and y inputs from each other and ground, a plotting area of 30″ x 30″, static accuracy of ±0.05% and dynamic accuracy of ±0.05% to 20 inches per second. It has a maximum slewing speed of 40″ per second and a maximum writing speed of 25″ per second. COMPUTER SYSTEMS, INC., Monmouth Junction, N. J. For information:

CIRCLE 212 ON READER CARD

solid state converter

This four-bit converter, display module, type DC-1, features parallel preset, variable radix counter, and

shift register. Each module consists of a minimum of four parallel read-in gates, four single bit storage stages, a decoding matrix and 10 output drivers. The unit price is $95. HYPERION INDUSTRIES, INC., 127 Coolidge Hill Rd., Watertown, Mass. For information:
CIRCLE 213 ON READER CARD

100 optical reader

Answer sheets may be fed into this machine and scanned at 2500 sheets per hour which utilizes photoelectric scanning and digital computer logic. In addition to scoring, the 100 may be used to perform information-search functions. DIGITEK CORP., 147 Lincoln Highway, Fairless Hills, Pa. For information:
CIRCLE 214 ON READER CARD

single unit power supply

The Chal-Multi-Pak unit is a computer grade multi-output supply which offers from one to five individually regulated outputs and a selection of voltages and currents ranging from 0-50 volts and 0-10 amperes with a total output power capacity of one kilowatt. Each power supply has transistorized regulators with the same short-circuit protection as single-unit power supplies. CHALCO ENGINEERING CORP., 15126 S. Broadway, Gardena, Calif. For information:
CIRCLE 215 ON READER CARD

counter-timer

A transistor dc to two megacycle universal counter-timer, model 726B, combines the functions of a counter, time interval meter and frequency/period meter. Output information from each DUC will operate digital printers, punches, in-line readouts and other dp equipment. COMPUTER MEASUREMENTS CO., 12970 Bradley Avenue, San Fernando, Calif. For information:
CIRCLE 216 ON READER CARD

differential amplifier

The P65 differential operational amplifier has been designed for computing, instrumentation and control. The miniaturized plug-in amplifier has a direct-coupled input with a differential input range of ± 10 volts and common mode rejection of about 10,000 to one. Input current is about 10^{-7} amperes and can be balanced out to 10^{-8} amperes with external circuitry. PHILBRICK RESEARCHERS, INC., 127 Clarendon St., Boston, Mass. For information:
CIRCLE 217 ON READER CARD

electromechanical dp system

A self-contained electromechanical dp system records sales orders via a keyboard or a pushbutton input, automatically retrieves stored data from punched-tape-memory reels, performs price calculations and selectively prints a variety of documents needed for manufacture, delivery and invoicing at multiple local or remote locations. The system does not require highly skilled operating personnel, and features compactness, low power consumption, and expandability. CREED & COMPANY LTD., Telegraph House, Croydon, England. For information:

CIRCLE 218 ON READER CARD

606 magnetic tape transport

The 606 features the selection of both high and low recording densities of 556 or 200 bits of digital information per inch, with a maximum data transfer rate of 83,400 characters per sec. The transport uses one-half inch tape and records information on seven channels. CONTROL DATA CORP., 8100 34th Ave., South, Minneapolis 20, Minn. For information:

CIRCLE 219 ON READER CARD

digital stepping recorder

The DSR 1250 offers asynchronous operation commonly associated with paper tape and card punches. The recorder has a stepping rate of 150 discrete steps per second and 300 discrete steps per second on special order. Features include dual voltage transistorized circuitry, two position pressure roller and input gates for record amplifiers. DIGI-DATA CORP. 4908 46th Ave., Hyattsville, Md. For information:

CIRCLE 220 ON READER CARD

punched tape reader

The model RR-301 photocell punched tape reader is a 300 character per second unit with completely transistorized circuits and photovoltaic sensing cells. The RR-301 is priced at $845.00. RHEEM MANUFACTURING CO., ELECTRONICS DIV., 5200 W. 104th St., Los Angeles, Calif. For information:

CIRCLE 221 ON READER CARD

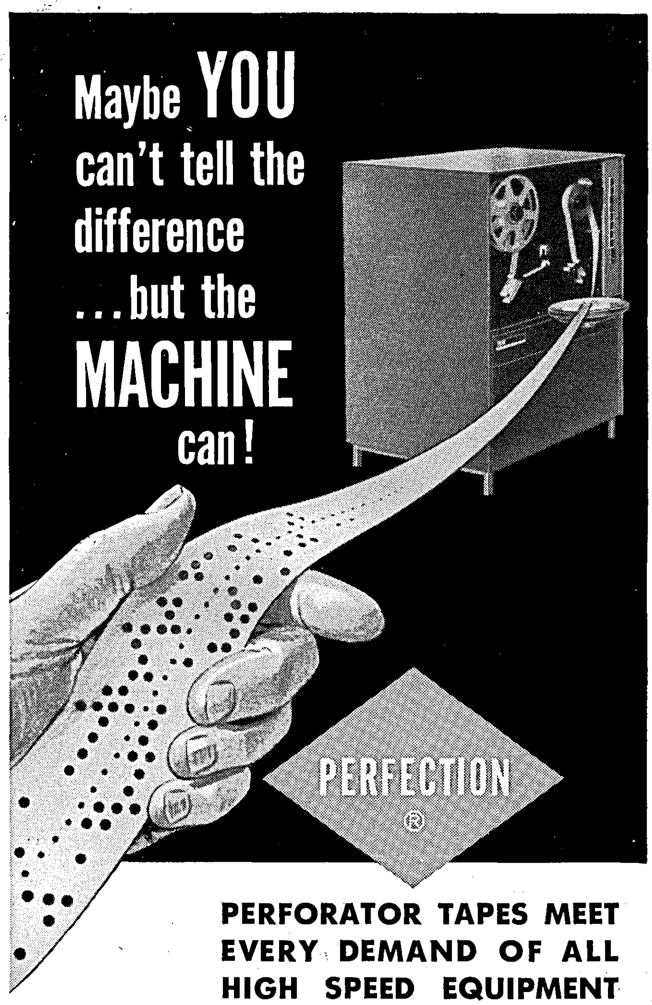
dual flip-flop module

The FF-521 is comprised of two independent transistor flip-flops which operate from dc to 250 kc. Each circuit has ac coupled "set" and "reset" inputs and a dc reset input. CONTROL EQUIPMENT CORP., 19 Kearney Rd., Needham Heights 94, Mass. For information:

CIRCLE 222 ON READER CARD

self-programming scanner

The SQ series of standard crossbar scanners can perform selective scan-



PERFORATOR TAPES MEET EVERY DEMAND OF ALL HIGH SPEED EQUIPMENT

The difference becomes very apparent in actual usage . . . particularly in today's high speed data processing systems. Perfection® tapes are made to the very highest standards of quality . . . quality that is superior to most others and second to none! Punches are clean and sharp, avoiding the danger of garbled or distorted readings. And Perfection® Tapes won't tear or break under the terrific speeds of modern equipment, frequently as fast as 10 million perforations an hour! You can *expect* and *get* the maximum number of reruns and folds with Perfection.®

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CIRCLE 46 ON READER CARD

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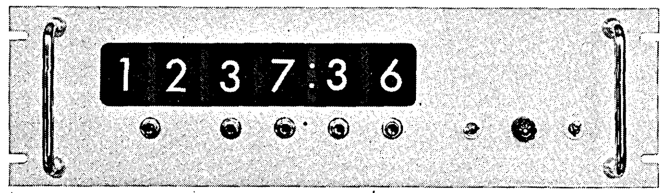
Time in increments of minutes, tenth minutes, or seconds. Time of day (12 hour or 24 hour) — Count Down or Elapsed Time configurations.

Easy to read, single or multiple displays. Output compatible with printers, typewriters, card punches, etc. Special models. For details write:



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CIRCLE 27 ON READER CARD

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CIRCLE 78 ON READER CARD

ning operations at rates up to 30 per second. The scanner crossbar is rated at 20,000,000 operations per crosspoint; insulation of an open point is not less than 10k megohms, and the resistance of the longest closed-circuit path is not more than 0.2 ohms. JAMES CUNNINGHAM, SON & CO., INC., Honeoye Falls, N. Y. For information:

CIRCLE 223 ON READER CARD

symbol generators

A new series of Universal Symbol Generators is able to convert digital codes into readable alpha-numeric characters at rates up to 32,000 per second. Up to 64 characters can be provided in 16-character groups. INFORMATION PRODUCTS CORP., 156 6th St., Cambridge, Mass. For information:

CIRCLE 224 ON READER CARD

serial memories

Models SM-30 and SM-32 employ magnetostrictive delay lines as the basic storage medium. Continuous storage is achieved by feeding the serial memory PAC output back to its input and recirculating the stored data. Maximum storage capacity of the SM-30 and the SM-32 are 1500 bits @ 1 mc and 1200 bits @ 2 mc, respectively. COMPUTER CONTROL CO., 983 Concord St., Framingham, Mass. For information:

CIRCLE 225 ON READER CARD

miniature core memory

This unit with sequential-access addressing modes has a selection of storage capacities from 72 to 4096 characters and character loading and unloading rates of up to 100 KC. The unit is able to retain information in the memory when the power is shut off. DI/AN CONTROLS, INC., 944 Dorchester Ave., Boston 25, Mass. For information:

CIRCLE 226 ON READER CARD

staggered finger dissipator

The configuration and continuous surface area of the new LP dissipator maximizes efficiency in natural convection and forced air environments, due to the staggered finger design. INTERNATIONAL ELECTRONIC RESEARCH CORP., 135 W. Magnolia Boulevard, Burbank, Calif. For information:

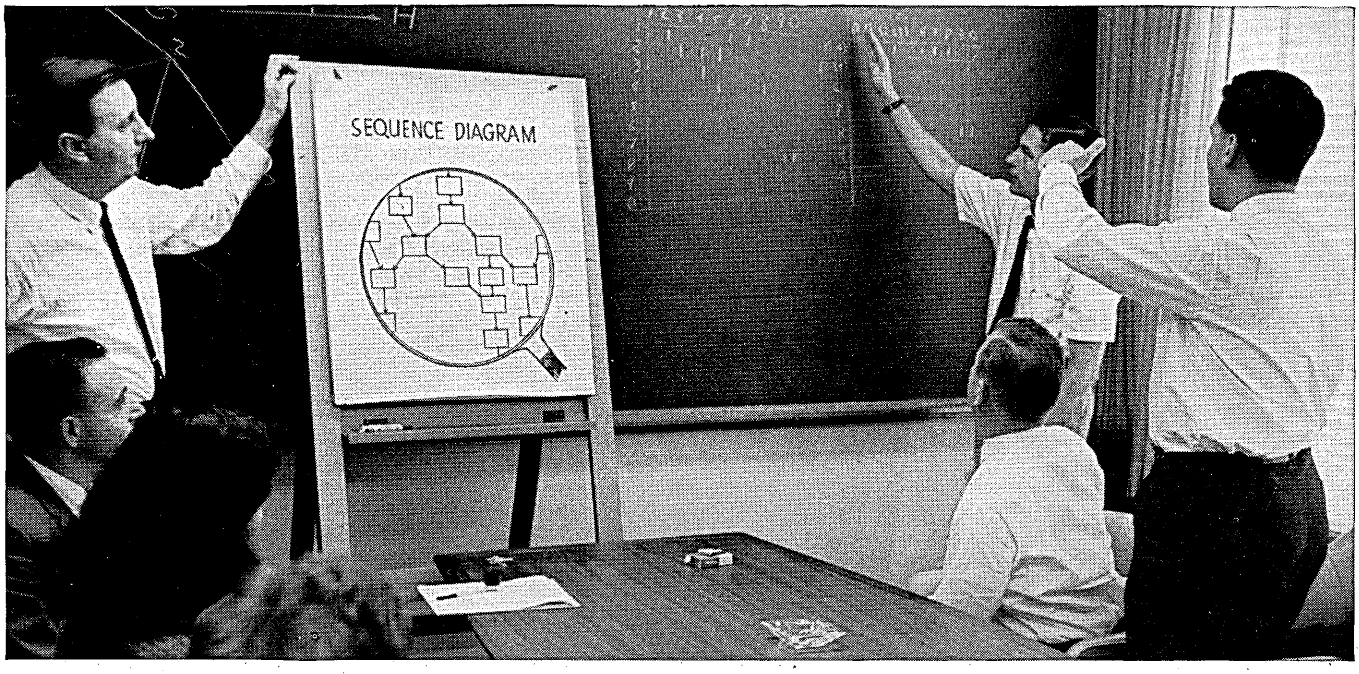
CIRCLE 227 ON READER CARD

precision clock

The MV-4 has four frequency rates available and is designed for applications which require clock pulse trains of moderate frequency tolerences. TECH SERV, INC., 4911 College Ave., College Park, Md., For information:

CIRCLE 228 ON READER CARD

at IBM



PROGRAMMERS shape the future of a new technology

IBM programmers, working with professional associates in research, development and manufacturing, are contributing expert knowledge and ideas in the creation of future computing systems.

This teamwork represents a striking advance in the role of the programmer and dramatizes the important part being played by this young but rapidly growing profession. At IBM, programmers are creating new concepts in software, and contributing to the design of new systems for virtually every phase of business, science and industry.

In response to the vastly increasing versatility of computers and their widespread applications, IBM programmers at all levels of endeavor are establishing new standards of achievement. They are designing programs that will simulate business and industrial operations. They are developing systems for government projects in space, defense and communications, where their data processing skills will help produce significant advances in tomorrow's computer technology. They are also studying the complex programs for . . . information-handling systems . . . scheduling methodology . . . information-retrieval studies.

IBM programmers also face challenging tasks in developing new programming systems. For example, they are devising programs that in turn use machine capability for formulating new programs. They are creating programs that enable computers to diagnose their own faults through self-checking. And they are helping to design the systems that will let scientists and engineers "talk" to machines in the everyday language of science and engineering.

Programmers at IBM take pride in their professional status and enjoy the unusual opportunities offered by a leader of the computer industry. In an atmosphere so receptive to new ideas, their concepts flourish. They find that their keen interest in exploring the capabilities of electronic computing is supported by IBM's full resources. This combination results in significant accomplishments recognized throughout the field.

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ADVERTISERS' INDEX

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The PB250 offers solid state reliability, a full complement of peripheral equipment, and software in abundance. It is backed by the resources of Packard Bell Computer Corporation (Subsidiary of Packard Bell Electronics).

SPECIFICATIONS: PB250 gp digital computer

Memory—expandable by plug-in from 2320 to 15,888 words

Word Length—21 bits plus sign

Command Structure—Single address with index register and next instruction location tag

Operation Times—Add/subtract—12 microseconds
Multiply—276 microseconds
Divide—252 microseconds
Maximum operation rate—41,666 instructions per second

Power Requirements—115 volts, 60 cps, 110 watts

Peripheral Equipment (connected by plug-in):
- Magnetic tape units (up to six)
- High speed paper tape punch and reader
- Card reader
- Line printers
- Analog/digital converters
- Multiplexers and commutators

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CIRCLE 2 ON READER CARD

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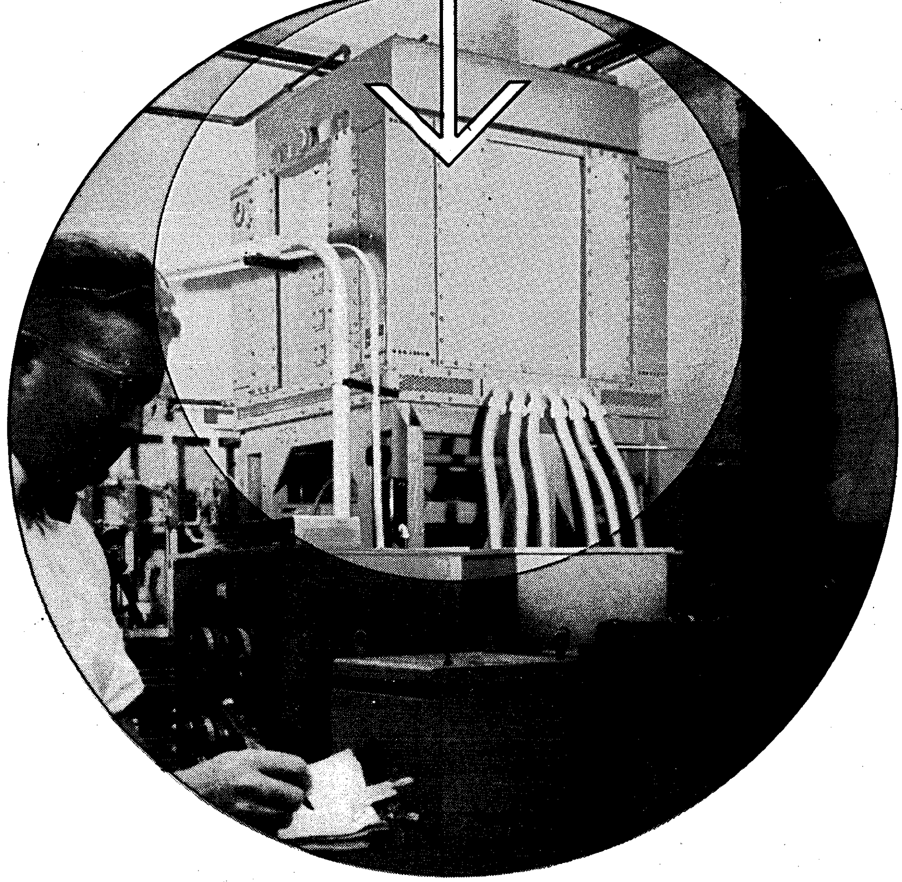

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