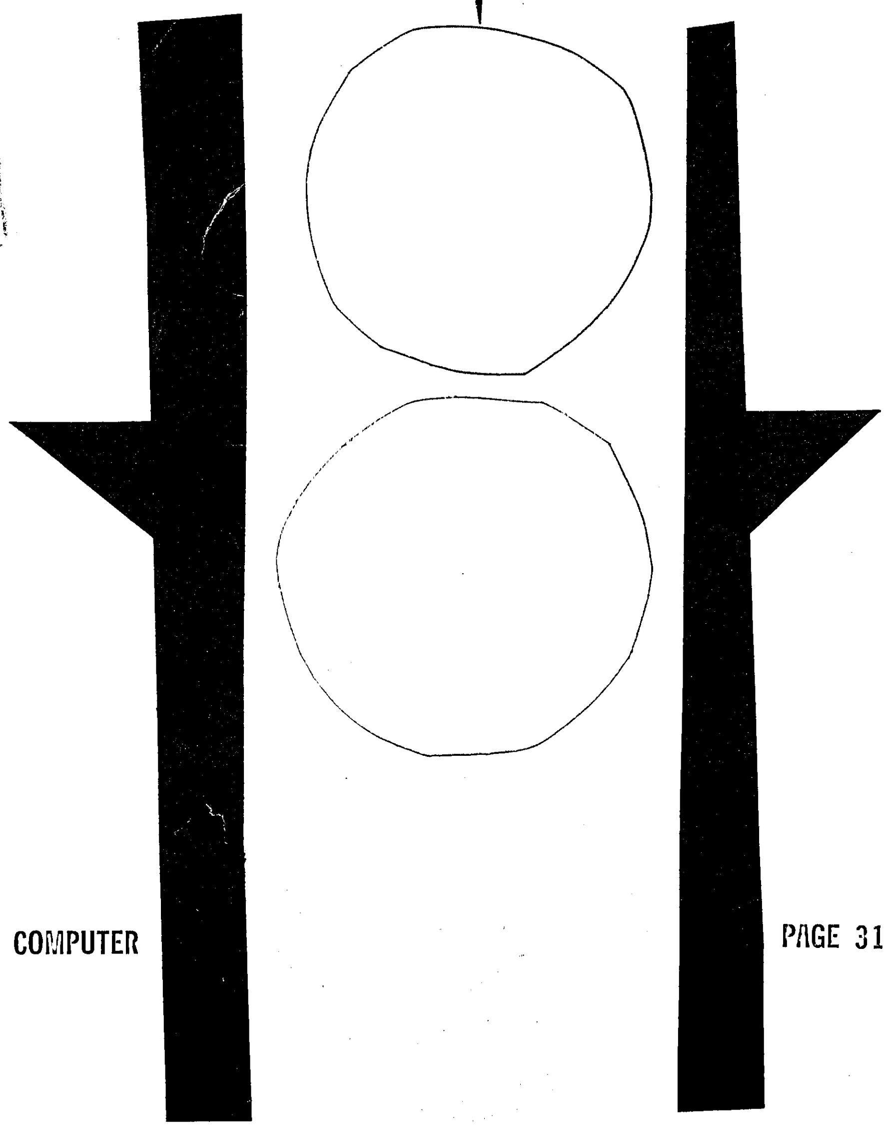
DATAMATION 62

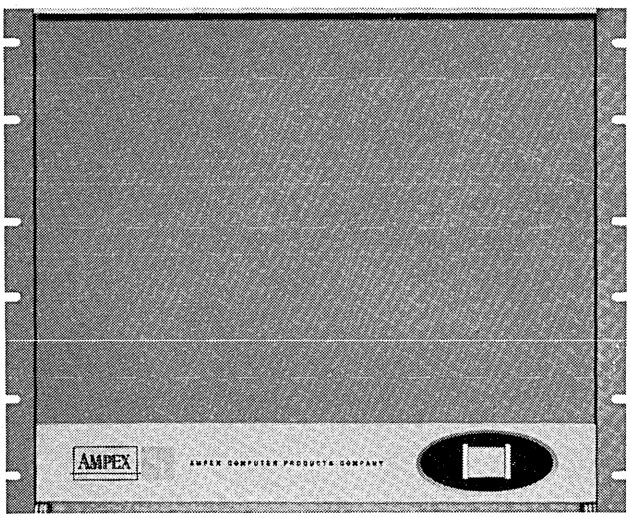
MAY

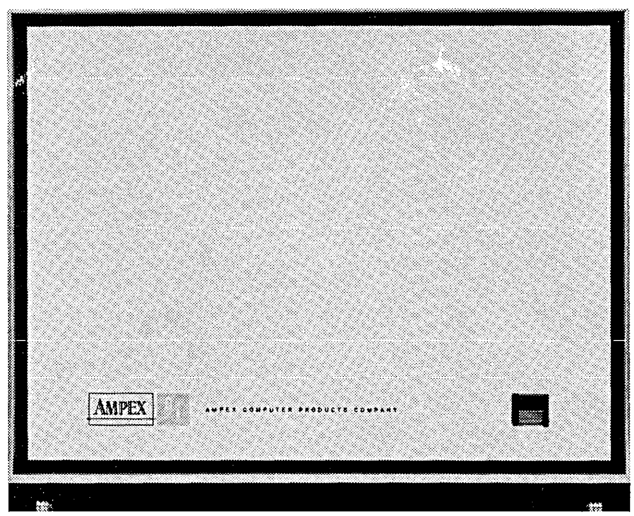


TRAFFIC CONTROL BY COMPUTER

PAGE 31

Richard Darnell, Sys Engr
I B M Corp
377~~Long Beach Blvd~~
~~Long Beach 7 Calif~~
Forward
13-16
Wilshire Blvd, LA





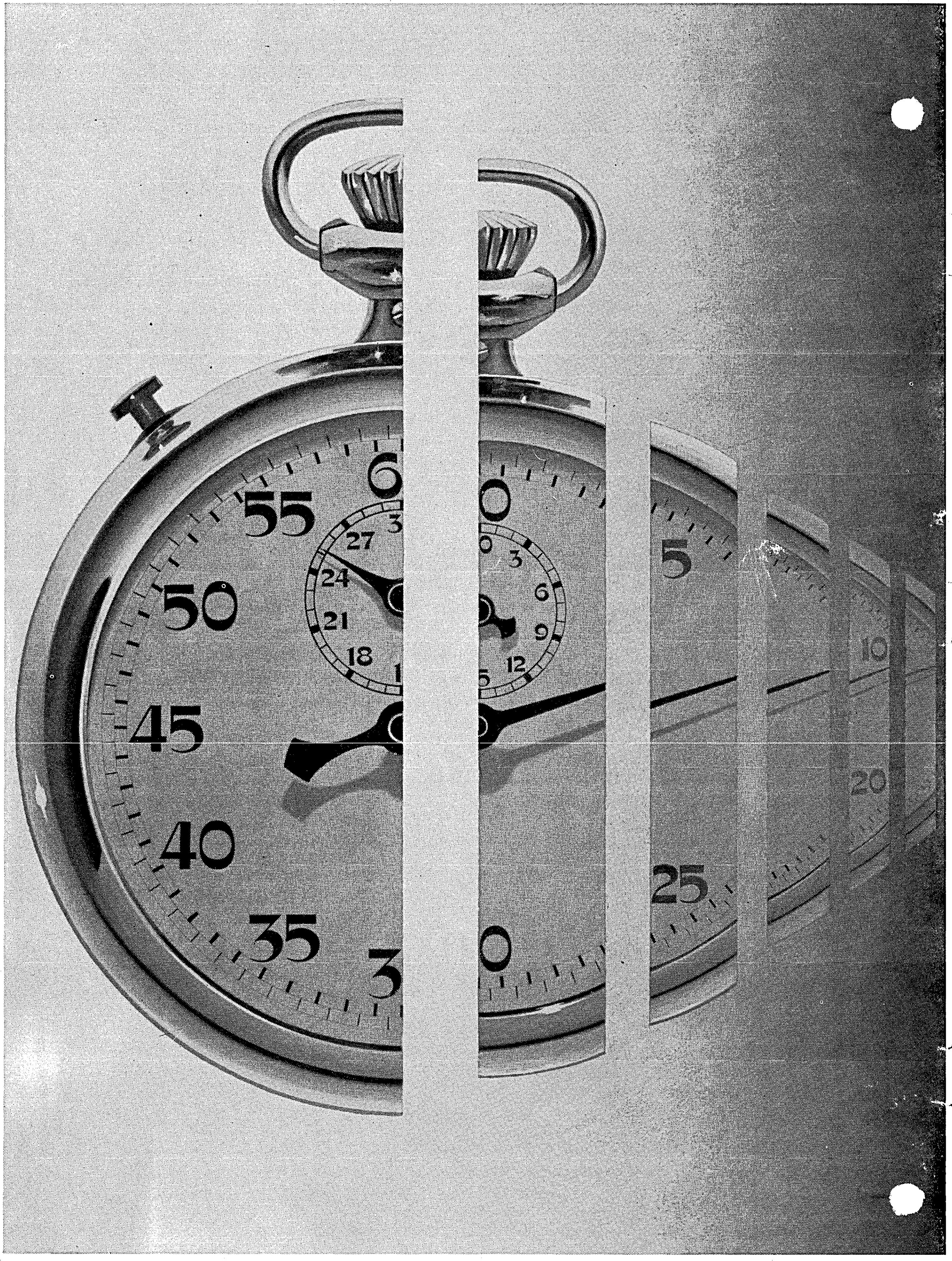
Yesterday Ampex introduced the RB for data systems that need a small memory. (1024 words.)

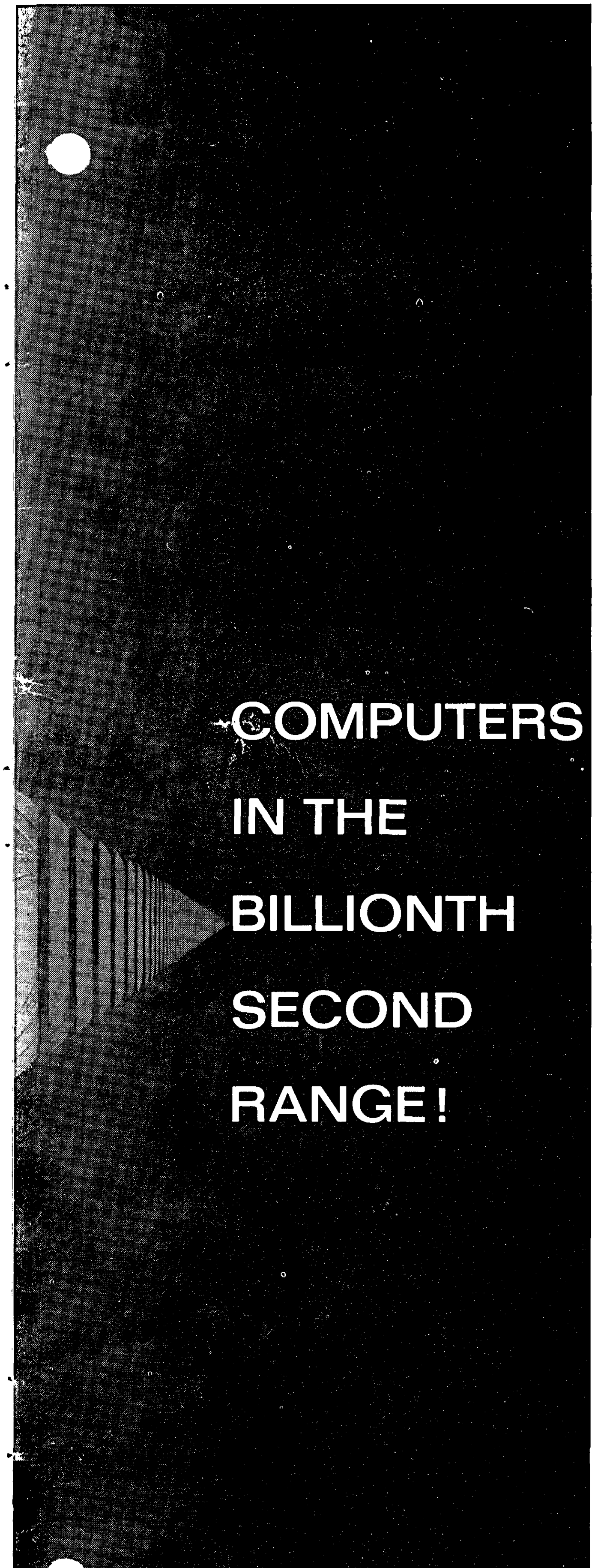
Today we bring you the RVQ for systems that need to think a bit bigger. (4096 words.)

The Ampex RVQ core memory unit is ideal for data systems that need small-to-medium storage capacities. At the same time, it has the flexibility for random access applications or high speed sequential or buffer operations. It's designed for rack mounting—a 36 bit word RVQ occupies only 15¾″ of rack space. It loads or unloads in 4 microseconds. Has a complete memory cycle of 6 microseconds. Remembers words 8 to 36 bits long. And operates on conventional unfiltered and unregulated AC power. You can tell it's an Ampex model by its reliable, simple operation. And its ease of maintenance—just flip the front panel down. The RB and RVQ are two of more than 40 solid state memories made by Ampex. Cycle times range from 24 to 1 microseconds with capacities up to a million bits or more. For data write: Ampex Corporation, 934 Charter Street, Redwood City, California.

AMPEX

CIRCLE 1 ON READER CARD





What's new at RCA
is news in EDP

Opening the Way to a New Generation of Data Processing Equipments

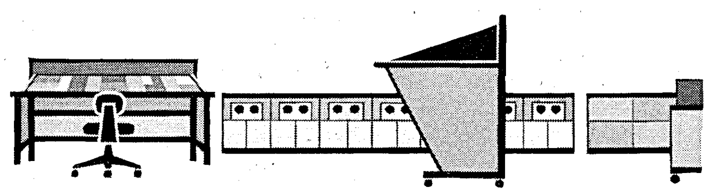
A future computer up to 100 times faster than today's computer . . . is now within the range of reality.

What makes possible such incredibly fast computers for tomorrow? It is the achievement of new, super-fast computer circuits based on RCA's tiny *tunnel diode* . . . an ultra-small decision element, simple in construction, economical to operate.

This advance was born of a far-reaching development program in which RCA was assigned the task of producing computer circuitry that would operate at speeds hardly imagined five years ago. Today, RCA has a variety of major circuit groups working in the nanosecond* (billionth of a second) range! In accomplishing this, RCA has surmounted many obstacles in miniaturization and high-frequency wiring techniques.

Here is another example of RCA's engineering progress in EDP . . . another step toward a new revolution in data processing, with important implications for business, industry, government and sciences. It's news in EDP, it's from RCA Electronic Data Processing, Cherry Hill, Camden 8, N. J.

**A nanosecond is to a second what a second is to 30 years!*



COMPLETE 301 SYSTEM NOW AVAILABLE FOR AS LITTLE AS $3,315 PER MONTH! Expansible to accommodate increased workloads . . . with high-speed magnetic tapes, millisecond random access processing, large capacity core memory, simultaneous operations, dual line printers and punched card readers. And more!

The Most Trusted Name in Electronics
RADIO CORPORATION OF AMERICA

CIRCLE 5 ON READER CARD

"Why we chose the NCR Computer."—AMERICAN GREETINGS CORPORATION, Cleveland, Ohio

"We chose the NCR Computer because, after thorough investigation, we became convinced it had the most advanced combination of features to meet our specific needs. And, looking to the future, we were convinced that it had the flexibility to adapt to the changing conditions that occur in a growing business such as ours.

"Because of its many unique features, our NCR Computer will become a vital electronic nerve-center, enabling us to keep a steady finger on the pulse of our business. For example, it will penetrate right to greeting card racks on more than 45,000 dealers' sales floors. We will be able to quickly measure sales activity by dealer and by card number. As a result, we will be able to stock each rack scientifically according to the needs of each dealer.

"Our NCR Computer will give us a tighter control over merchandise assignment. It will give us a sharper gauge of stock control and stock turnover. It will improve customer relations. And, while we will use the computer for all phases of our data processing, our investment will be justified on the Order Processing application alone."

Irving I. Stone

President
American Greetings Corporation

NCR PROVIDES TOTAL SYSTEMS—FROM ORIGINAL ENTRY TO FINAL REPORT—
THROUGH ACCOUNTING MACHINES, CASH REGISTERS OR ADDING MACHINES, AND DATA PROCESSING
The National Cash Register Co.•1,039 offices in 121 countries•78 years of helping business save money

NCR

CIRCLE 6 ON READER CARD

DATAMATION 62

the automatic handling of information

volume 8, number 5

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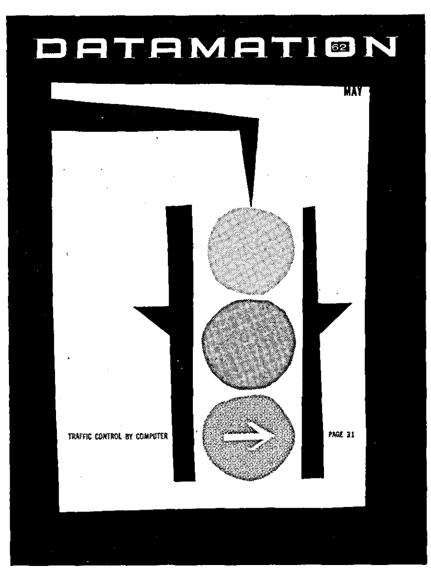

Cover

More important than the accuracy and speed of a computer in traffic control, and integrally related to the movement of vehicles is the often forgotten stoplight which *Datamation* art director Cleve Boutell has colorfully illustrated for this month's cover design. A report on an NBS traffic study in Washington, D.C. begins on page 31.

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WHY

■ *does one computer system take maximum advantage of its computing speed, peripheral equipment and storage capacity at all times and under all conditions—whereas others do not (and cannot)?*

■ *do three jobs that each take an hour to do on other systems take only 1¼ hours all told on this system?*

■ *do interrupt conditions that make other systems bog down have no effect on this system?*

■ *do you get more throughput per dollar with this system than with any other?*

■ *can this equipment lay claim to a totally new concept in computer system operation?*

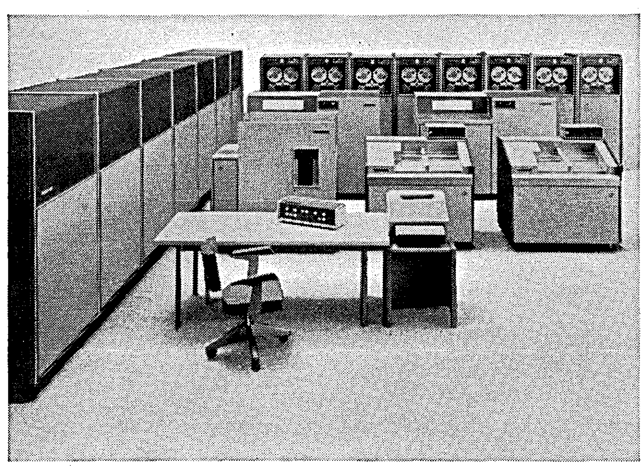
The Master Control Program (MCP) of a Burroughs B 5000 Information Processing System is the answer. It's one of the primary answers to all the questions above, and it's also the solution to just about every operational drawback that's ever drained away a computer user's time, money and patience.

Take the question of interrupts, for example. Conventional systems employ programed interrupt detection. In the B 5000, interrupt detection is built right into the hardware. The hardware then switches electronically to the appropriate portion of the MCP for automatic handling of that specific interrupt condition. Meanwhile, the current program is processed further or another program is run instead, if preferred. In either event, the B 5000's MCP assures that an interrupt *condition* does not mean an interruption of the system itself or the work in progress.

Or consider the paradox of how three jobs that each take one hour to do on other systems can be completed in less than half that time by the B 5000. It's easy—the way the MCP does it. Since some jobs need a lot of processor time but little input-output time, whereas some jobs need just the opposite, the MCP cuts the total processing time of each by running them *concurrently*. The programer needs to write only the basic program and the MCP takes over from there, scheduling and assigning different components when free. This ability to time-share unused processor and input-output capacities is one of the main reasons the B 5000 can give you more throughput per dollar.

Versatile as it is, however, the MCP doesn't fully account for the fact that the B 5000 is a totally new concept in system operation. There's the B 5000's ability to incorporate a second central processor, for instance—without reprograming. And there's the fact that the B 5000's basic design concept provides effective and productive use of the higher level languages of ALGOL and COBOL. Plus enough other reasons to fill a whole booklet—which we'll be glad to send to you. It's called *The B 5000 Concept* and is available from our main office at Detroit 32, Michigan.

Burroughs—TM



Burroughs Corporation Burroughs

CIRCLE 7 ON READER CARD

important DATES

• "Electronic Information Display Systems" is the subject of an institute to be held May 21-25 at the American University, Wash., D.C.

• A conference on Self-Organizing Systems will be held on May 22-24 at the Museum of Science and Industry, Chicago. It is co-sponsored by the Information Systems Branch, Office of Naval Research, and the Armour Research Foundation.

• A Symposium on Mathematical Programming sponsored by the Graduate School of Business of the University of Chicago, the ACM, and USAF Project RAND, will be held June 18-22 at the University of Chicago, Chicago, Ill.

• The Ninth Annual Symposium on Computers and Data Processing sponsored by the Denver Research Institute of the University of Denver is scheduled for June 27-28 at the Elkhorn Lodge, Estes Park, Colorado.

• The 1962 Rochester Conference on Data Acquisition and Processing in Medicine and Biology is set for July 17 and 18 for the Whipple Auditorium, Strong Memorial Hospital, Rochester, N.Y.

• The Northwest Computing Assoc. will hold its fifth annual conference Aug. 9-11 in Seattle, Washington. The conference is being held in conjunction with the Century 21 exhibit.

• The 1962 WESCON will be held Aug. 21-24 in the California Memorial Sports Arena and Statler-Hilton Hotel, Los Angeles.

• The 1962 IFIP Congress is set for Aug. 27-Sept. 1 in Munich, Germany.

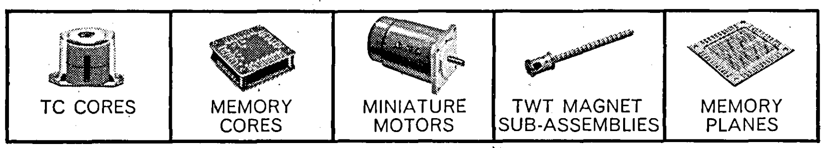
• The ACM National Conference will be held Sept. 4-7 at the Onondaga County War Memorial Auditorium and Hotel Syracuse, Syracuse, N.Y.

• The 3rd annual Symposium on Switching Circuit Theory and Logical Design will be held Oct. 7-12 in Chicago, Ill. under the sponsorship of the AIEE Computing Devices Committee.

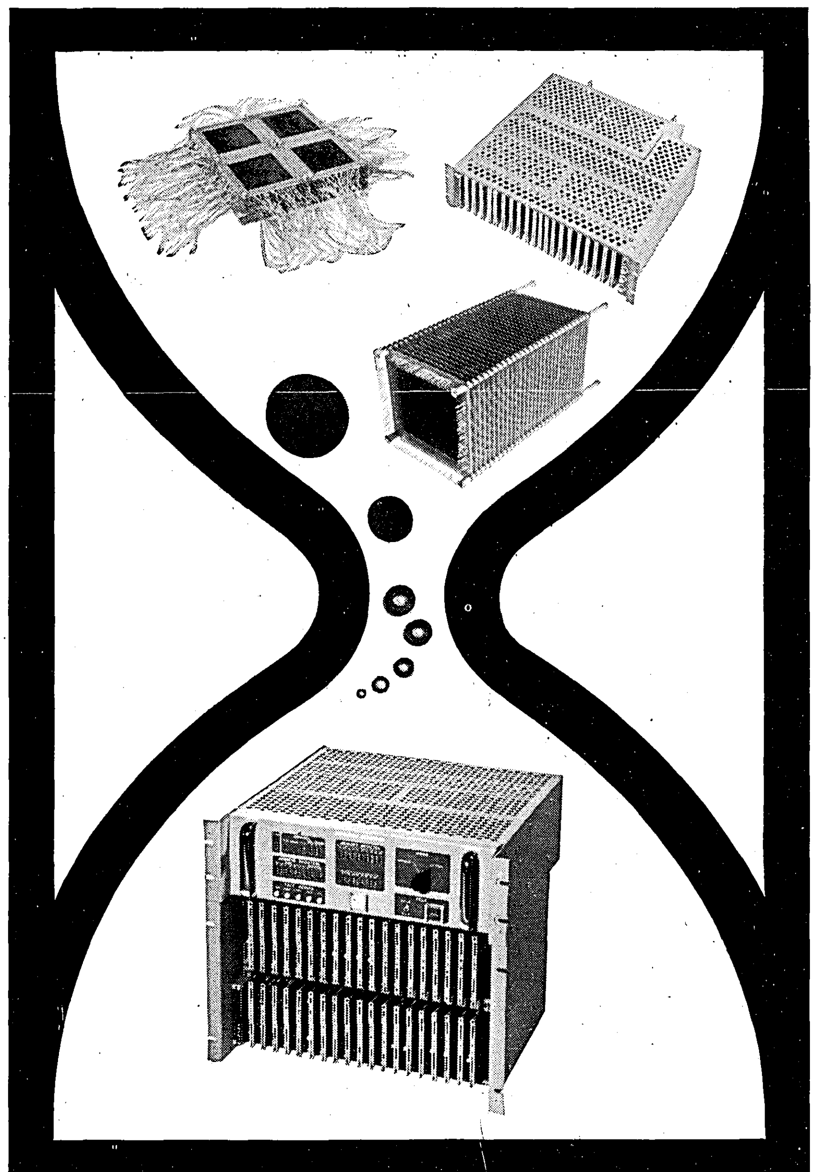
• The 1962 Fall Joint Computer Conference will be held Dec. 14-17 at the Bellevue Stratford Hotel, Philadelphia, Penna.

Storage Systems are our business — We can build a memory system to fit your needs from in-stock standard parts — memory stacks, printed circuit cards, power supply unit, 19″ standard racks — and deliver it complete in 45 days. These are available in each of three basic internal logic types — random access, sequential non-interlaced, sequential interlaced — with cycle times as fast as 1.5 μs. In addition to fast delivery, we offer you much more — a highly competent team of research, development and application engineers, backed by the finest production facilities in the industry. ■ **For new data file on memory products, write to** Indiana General Corporation, Electronics Division, Keasbey, New Jersey.

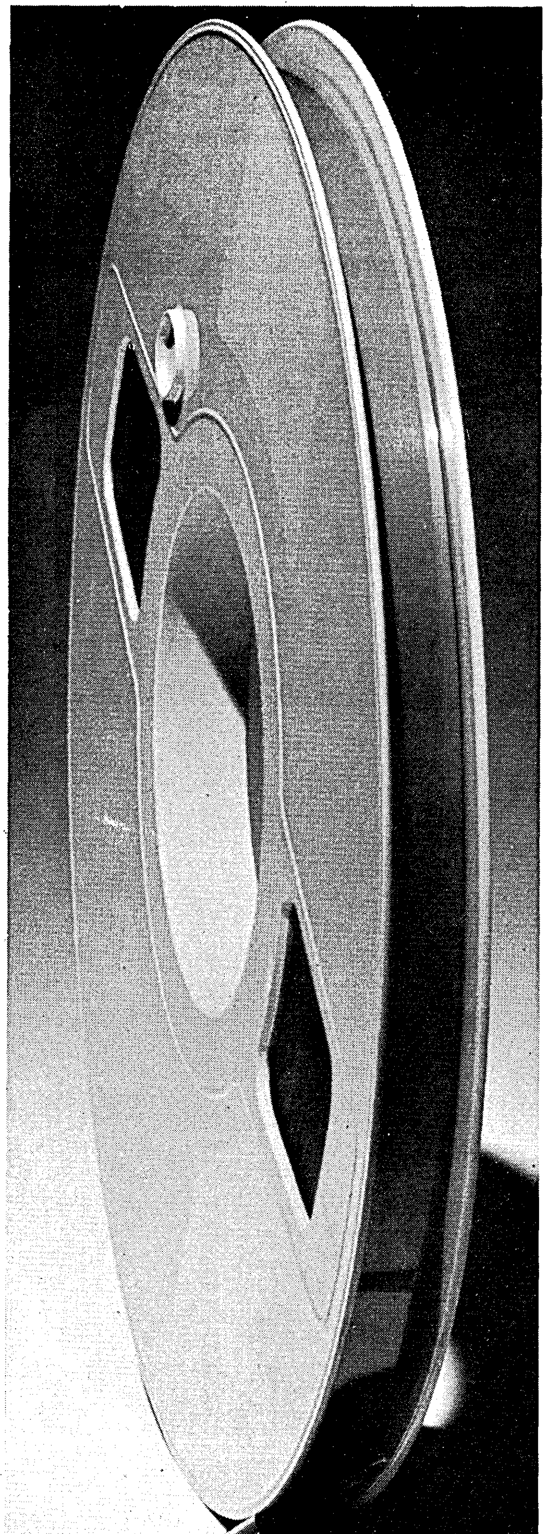
INDIANA GENERAL



in-stock modules
45-day memory delivery...



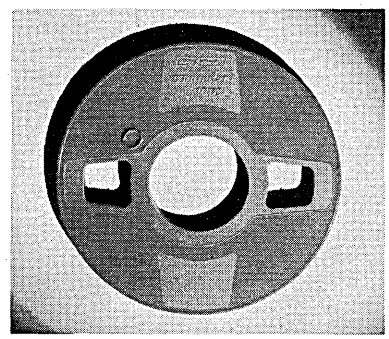
CIRCLE 9 ON READER CARD



MAC / PANEL

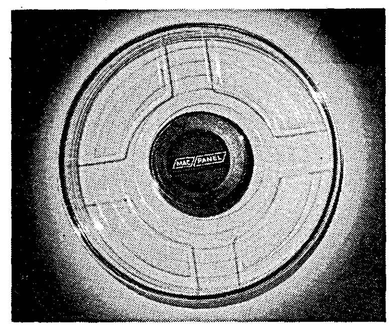
computer tape ACCESSORIES

In addition to providing you with a complete line of quality control panels and wires, MAC Panel is also a dependable source for your computer tape accessory needs. Same MAC Panel quality, of course . . . and all shipments made the same day orders are received.



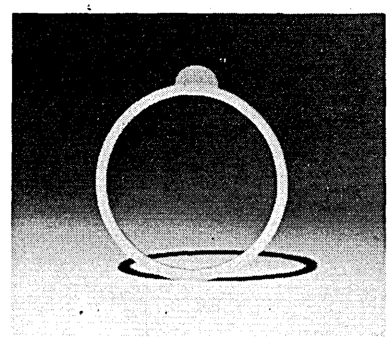
PLASTIC REELS

Attractive and easy to use reels of high impact plastic to insure proper alignment on magnetic tape units. Holds 2400 feet of magnetic tape for 727, 729 and 7330 tape units. Colors available: Gray, Blue, Red and Yellow.
Weight: 8 ounces per reel.



PLASTIC CONTAINERS

Holds plastic reel above. Clear plastic container is equipped with "positive lock" hub device that prevents motion thereby reducing plastic dust and particles caused by friction.
Weight: 1 pound, 6 ounces per container.



READ OUT RINGS

The read out ring is a device which upon removal from the reel prevents accidental loss of master information and only allows data to be read. When the ring is in place on the reel, reading, writing or erasing can be done by the tape unit as called for during processing.
Polyethylene Plastic: 3 ounces per dozen.

MAIL TODAY

USE THIS HANDY ORDER FORM OR WRITE

MAC Panel Company • P.O. Box 5027 • High Point, North Carolina

☐ Please have a representative call for an appointment.

☐ Please ship the following immediately: TERMS: F.O.B. High Point, N. C.

_____Plastic Reels @ $2.65 per reel. (Specify Colors):_____

_____Plastic Containers @ $3.15 per container.

_____Reels and Containers at the combination rate of $5.75. (Specify Reel Colors):_____

_____Dozen Read Out Rings @ $1.80 per dozen.

NAME_____ COMPANY_____

ADDRESS_____ CITY_____ STATE_____

CIRCLE 10 ON READER CARD

letters

nano or nona?

Dear Sir:

With the advent of faster machines and thin film memories, technical articles refer to very small time units as "*nano*seconds." In some instances the term "*nona*second" is used.

According to Webster, NANO is a combining form from the Greek "nanos," meaning dwarf. A nanosecond would then be defined as an abnormally small second.

On the other hand, the term nonasecond seems appropriate to describe a billionth of a second: a billionth of a second is 1×10^{-9} seconds and the Latin root "nona" means nine.

Are the terms nanosecond and nonasecond synonymous and do they both define one-billionth of a second?

J. M. GILLY
C-E-I-R, Inc.
Arlington, Virginia

(Editor's Note: To the best of our knowledge there has been no standardization on either nonasecond or nanosecond although the latter is more commonly used. As a third alternative, try "gigacycle" which has been accepted as an international standard for one kilomegacycle, or one billion cycles.)

an open letter to CODASYL

Hon. Thos. D. Morris
Asst. Secty. of Defense
Pentagon, Wash. D. C.

In a relatively new field such as computer software for business use there are wide ranges of opinion and hence it was to be expected that COBOL would be criticized. Unfortunately, however, the issues are clouded by the fact that many persons involved represent companies which may have financial interests in decisions reached. Since the Department of Defense (DOD) has adopted policies which have elevated COBOL to a unique position, I believe that the DOD has an obligation to all concerned to put COBOL on a firm basis. My suggestion would be that the DOD ask a group of the best qualified persons to take short leaves of absence from their present work and to prepare an unbiased report on COBOL, supported solely by the DOD in this effort.

In particular, I suggest such a group be composed of five persons chosen with the advice of the Joint Users Group or the National Council of the ACM preferably from among computer users. I would like to see them prepare a report on:

1) Compatibility in specific detail of presently specified COBOL Processors.
2) Current acceptance of COBOL in competition with other languages —facts regarding manufacturer efforts and user efforts.
3) Technical comparison of COBOL with other languages in both basic principles and major details.
4) Technical criticism of the specifications of COBOL with regard to internal consistency and completeness.

In order to ensure that the members act without any pressure, it should be previously understood that only one final joint report will be issued.

CHARLES J. SWIFT,
Los Angeles, Calif.

credit and apologies

Dear Sir,

The article "BALGOL At Stanford" in the December, 1961 issue of *Datamation* generated considerable interest at Lockheed since the computer program and comparisons reported appear to have originated here and no credit was given to LMSC in the article.

L. H. AMAYA,
Manager,
Lockheed Missiles & Space Co.
Sunnyvale, Calif.

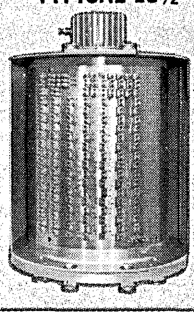
(**Editor's Note:** *Sincere apologies are tendered to Mr. Amaya by* **Datamation** *and from Professor George Forsythe at Stanford who furnished us your report as part of the Stanford article under the erroneous assumption that it was available for public consumption sans credit. Also see Business & Science, page 19*).

NEXT MONTH IN DATAMATION

Three state-of-the-art surveys on air line reservation systems, computing in the medical sciences and the pros and cons of equipment leasing will share the heated editorial glow in our June issue. Another Grosch exclusive and a helpful treatment by Bob Patrick titled, "Let's Measure Our Own Performance," will also be featured. On the lighter side will be Part III in our series on the Maintenance, Care and Coddling of sick Kludge machines.

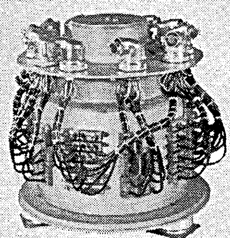
HERE'S PROOF YOU STILL CAN'T BEAT A BRYANT DRUM

TYPICAL 18½" DRUM APPLICATIONS

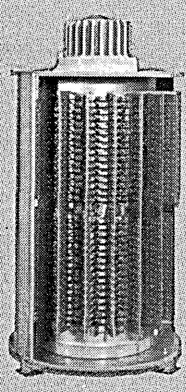


Teleregister Corporation
Airlines Reservation System
Banking Systems
Melpar, Incorporated
Military System

TYPICAL 7½" DRUM APPLICATIONS



Bailey Meter Company
Bailey 700 Systems
General Precision, Inc.
RPC 4000 Computer

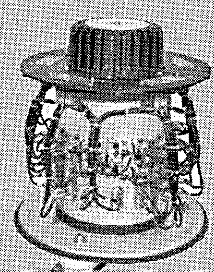


TYPICAL 10" DRUM APPLICATIONS

Rabinow Engineering Company, Inc.
Post Office Sorter
Consolidated Avionics Corporation
Security System

No other manufacturer offers you Bryant's proven experience in the design and production of magnetic data storage drums. Since 1953, Bryant has produced more than 1,500 memory drums for over 100 customers . . . a few of which are shown here. Included are drums for commercial data processing computers . . . for industrial process control systems . . . for rugged airborne and military applications. Some represent drums only, others are complete data storage systems. Some have fixed heads, some flying. In sum, they are your assurance that you still can't beat a Bryant drum.

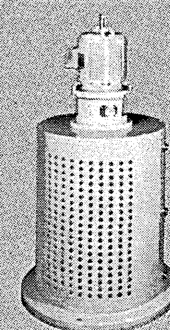
For additional proof, see your Bryant Representative, or write direct to: 850 Ladd Road, Walled Lake, Michigan, MArket 4-4571.



TYPICAL 5" DRUM APPLICATIONS

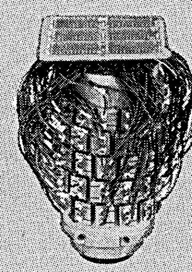
The Martin Company
BIRDiE Computer
Sandia Corporation
Check-out System

TYPICAL CUSTOM UNIT APPLICATIONS



Philco Corporation
20" Drum (Philco 2000 Electronic Data Processing Systems)
Radio Corporation of America
18,000 RPM Disc

TYPICAL 3" DRUM APPLICATIONS

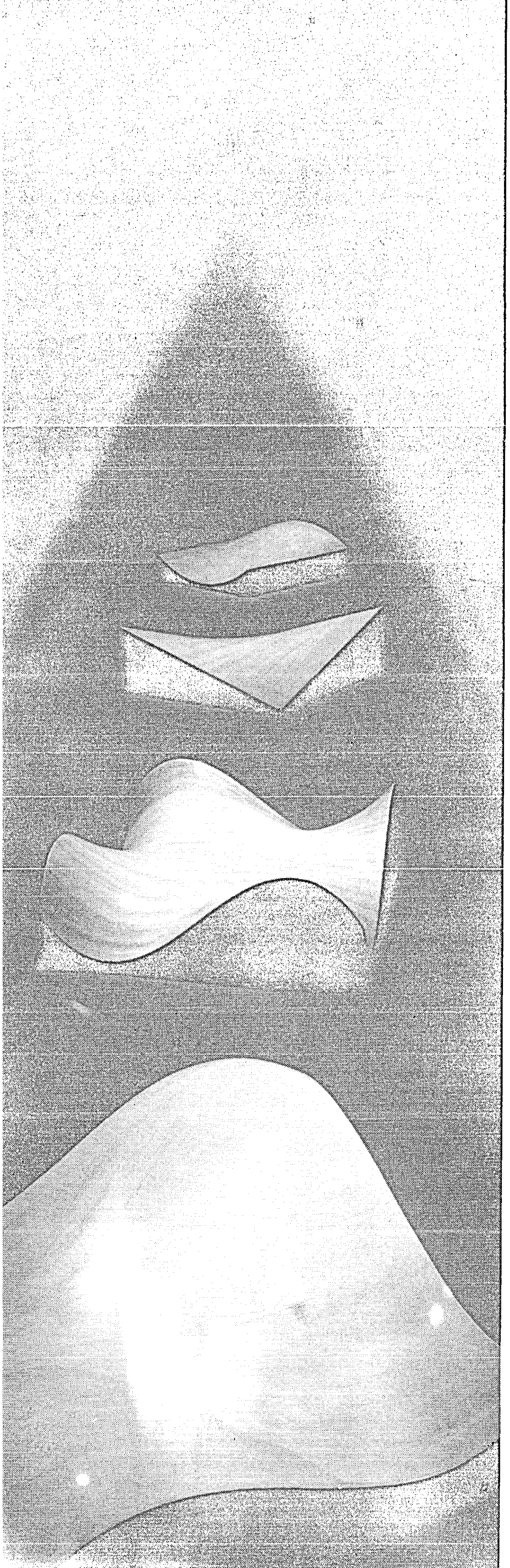


ITT Kellogg
Telephone Switching System
Burroughs Corporation
Airborne Computer

62-43 CP

BRYANT **COMPUTER PRODUCTS**
Disc File and Magnetic Drum Memories for Every Storage Application
A DIVISION OF EX-CELL-O CORPORATION XLO

CIRCLE 24 ON READER CARD



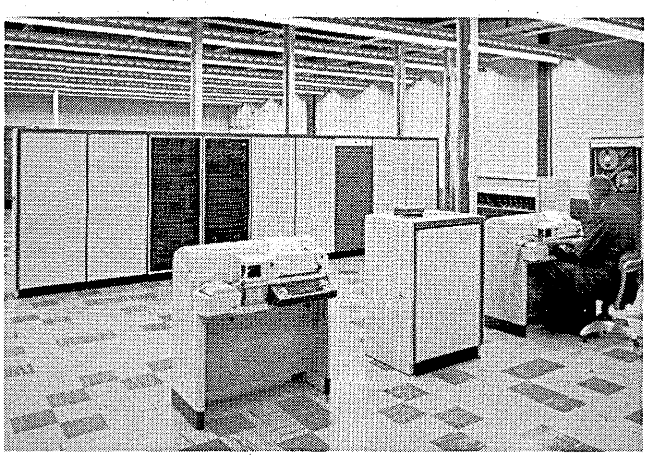
Announcing:

Collins Data Central

A fast, flexible electronic switching center for your company's communication network

Data Central offers you new advantages and economies because it is designed specifically as a communication processing system. Its direct TTY connections save you the cost of line conversion equipment. It gives you micro-second speed in switching messages from incoming to outgoing lines. It can be organized, as no other system can, to meet your own *specific* TTY requirements, and it accommodates any change in your requirements.

A unique, solid-state processor gives Data Central its flexibility. This processor has two memories — a conventional computer memory, and a *Programmed Logic Unit.* This unit performs functions handled by fixed wiring in other processors. By removing fixed wire restrictions, Data Central gives you the freedom you need to organize an automatic switching center to meet your specific communication needs . . . and to change the operation of your center as your requirements vary. All that's required are simple changes in the Programmed Logic.



Here are other features of this versatile switching system:

Conventional TTY operation — Serial, mixed speed on full or half duplex lines.

Store and forward — Messages awaiting free circuits are held in temporary storage.

Multiple priority — Immediate interrupt for no-delay priority messages.

Multiple address — From a two-station to all-station broadcast as each circuit becomes available.

Automatic conversion — Code, speed and format, concurrent with switching.

No lost messages — Automatic message accounting, queuing and check-off.

Accuracy — Internal parity check. System check optional.

Traffic analysis — Historical files permit message retrieval for analysis, logging and retransmission.

High-speed trunking — Collins Kineplex® high-speed data transmission systems operate under stored program control of the Data Central processor.

System balance — Handles peak loads efficiently.

Expandability — Processor memories, storage and input-output devices, and TTY circuits are expandable to meet changes.

Complete customer service — Includes installation, maintenance, programming and training.

Data processing, too. The Data Central processor is also capable of handling both scientific and business data processing assignments. This system is the first to be made commercially available from Collins' new C-8000 Series of communication and data systems. Find out why leading companies are turning to Data Central . . . how it can advance your own communication capabilities. Write:

COMMUNICATION AND DATA SYSTEMS DIVISION, COLLINS RADIO COMPANY, DALLAS, TEXAS.

FOR THE BEST COMMUNICATION OF BUSINESS INFORMATION . . . CALL COLLINS

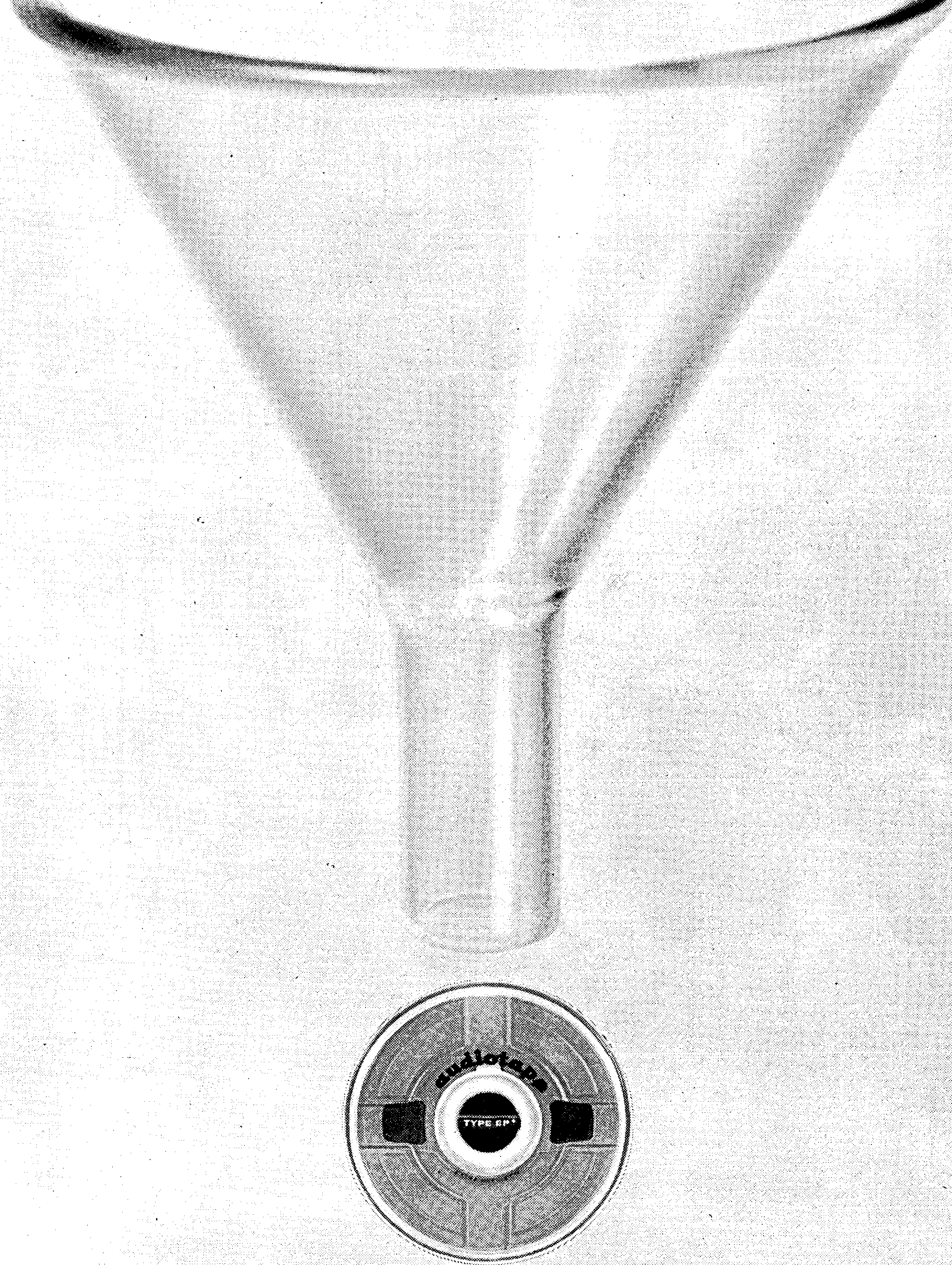
COLLINS

CIRCLE 15 ON READER CARD

WHAT GOES INTO A SUPERIOR COMPUTER TAPE?

Many things, tangible and intangible, go into the making of EP Computer Audiotape. On the tangible side, only the finest materials and equipment—meticulously selected and constantly tested—are used in producing this extra precision computer tape. In addition, every reel is 100% checked on specially-designed Automatic Certifiers to insure that each of the 112 million test pulses (161 million on high density tapes) reproduce properly . . . Less tangible but just as important are our years of experience in this exacting field. Experience that tells you Extra Precision Computer Audiotape consistently lives up to its name. Once you try this superior computer tape, we're certain that you'll agree.

EP COMPUTER AUDIOTAPE / AUDIO DEVICES INC., 444 MADISON AVE., N. Y.



BUSINESS & SCIENCE

1ST 6600 SET FOR LIVERMORE

A firm order for Control Data's first super-scale 6600 will soon be placed by the Atomic Energy Commission for installation in Livermore, California. Delivery will be scheduled for August, 1963 at a price tag of approximately 5.8-megabucks.

Bids for this equipment were initiated during the summer of '61 although the restriction of a general purpose machine in Livermore's RFD letter whittled the field down to only a few competitors.

Presently operative at Livermore is RemRand's LARC, IBM's STRETCH, three 7090s, one 1401 and one 650. The 6600 will add another 256K of core storage to the facility with its 20 megacycle circuitry approximately 15 times faster than the 1604. Word size is 60 bits divided into 48 bits for fractional use and 12 for exponent.

C-E-I-R SCRATCHES STRETCHES: "AN AGONIZING REAPPRAISAL"

Long publicized as its bid for the major segment of time sales in business data processing, C-E-I-R has finally been confronted with the economic realities of acquiring STRETCH, the world's biggest, fastest and most aggravating computer. Last month, C-E-I-R president, Dr. Herbert Robinson, announced cancellation of both orders for his Los Angeles and Boston offices.

Untangling oneself from a $14-megabuck contract is not always the most pleasant of chores but according to Dr. Robinson, "Under the terms of the cancellation, C-E-I-R is not required to make any payments to IBM. In exchange for an alleged one megabuck penalty, C-E-I-R has agreed to furnish its own software "for certain new lines of IBM equipment on order by C-E-I-R and which will be made freely available to IBM." (At press time Datamation has been unable to determine whether a $500,000 deposit per STRETCH will be returned to C-E-I-R.)

Primary emphasis will now be placed on the 7094 which C-E-I-R will soon have available in each of its centers.

For certain classes of scientific problems for which there is largely all computing and virtually no I/O, STRETCH offers a significant advantage over any other announced equipment. However, for popular job mixes the throughput per buck for a STRETCH system is not competitive with a 7094.

Whereas STRETCH time would have sold from $1,500-$1,800 per hour, the 7094 will be available from $400-$632 per hour.

The contract for two STRETCH machines was signed by Dr. Robinson on Aug. 2, 1960. On Oct. 19, 1960,

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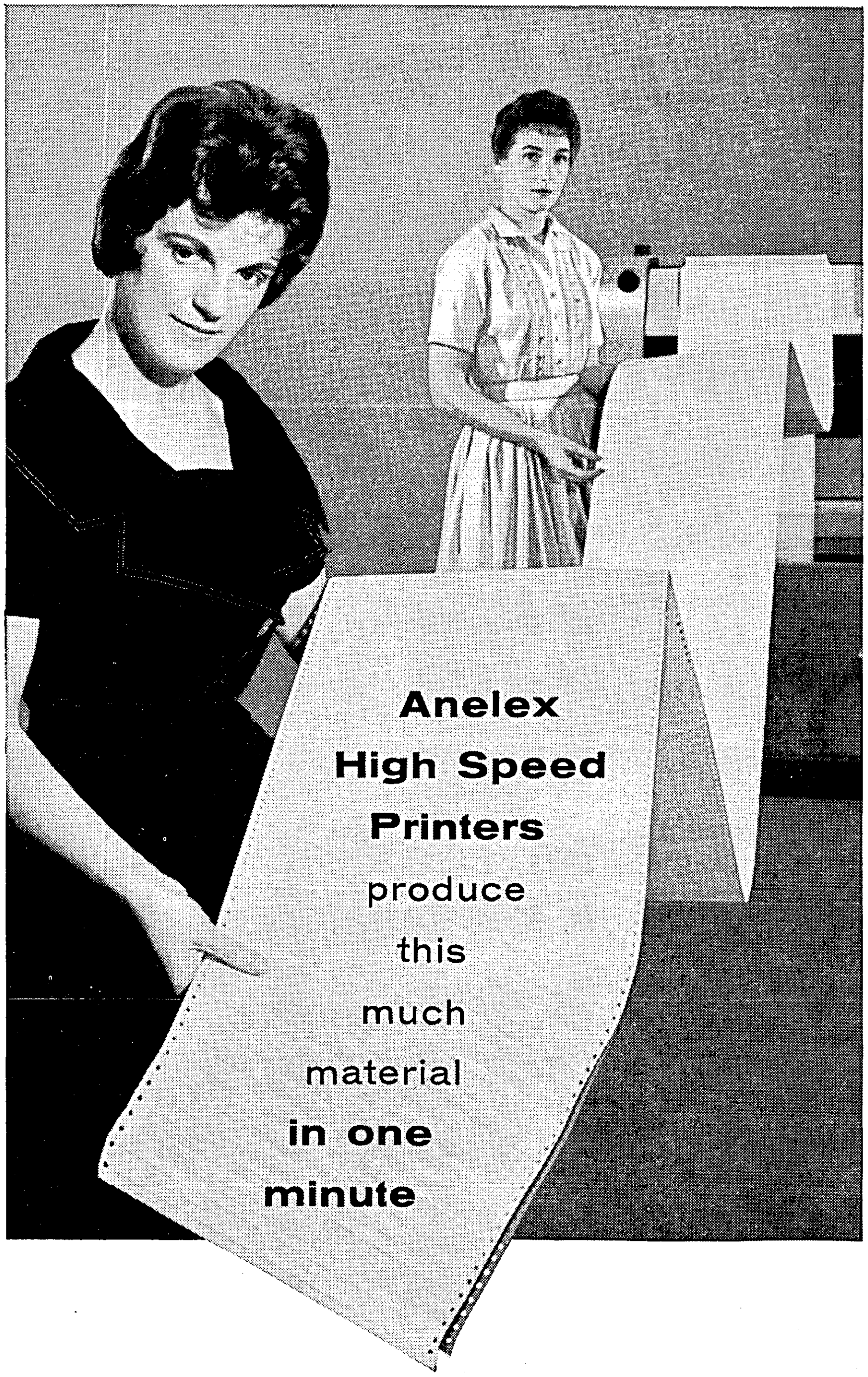

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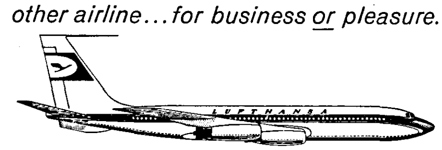

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IBM's technical rep Ken Poovey, addressed himself to this subject at a one day technical symposium of the ACM held appropriately at Disneyland in Los Angeles (across the highway from Frontierland and Fantasyland).

Poovey discussed circumstances in which the high speed and storage of STRETCH is not always required particularly for numerous, small problems and explained that the throughput would be limited by I/O speed which is similar on large computers such as STRETCH and the 7090.

"We conclude immediately," Poovey added, "that without multi-programming, the acquisition of a STRETCH computer in these circumstances would be a blunder."

He said, "Multi-programming on STRETCH is then not only desirable but necessary if it is to be considered at all. It is difficult to present tactfully my doubts of our ability to realize in a practical length of time or outlay of money, an efficient, workable multi-programming system for STRETCH."

While several studies were obviously made to determine the economic feasibility of STRETCH for C-E-I-R, it would appear that once a major position is firmly taken, it becomes close to impossible to affect an early retreat. In this case, insufficient attention was paid to a competent extrapolation of the state of the art and when sufficient time was not sold in advance of the installation, a hasty withdrawal became a financial necessity as well as a public embarrassment.

It is expected that the two STRETCHES which C-E-I-R has cancelled will not be made commercially available by IBM at any price. Although no official statement has been received as yet from White Plains, the pre-Christmas clearance of STRETCH machines announced by T. J. Watson in May of last year is finally over.

A COMPILER COMPARISON

A time test comparison study of compilers was recently completed by Lockheed Missiles & Space Co. in Sunnyvale, Calif. Initial figures were released in Nov., 1960 and have since been updated. With the propensity of users to worship the latest surveys of compile speeds, the following may prove of more than passing interest:

Machine	Language	Time (seconds) Compile	Execute	Remarks
IBM 7090	FORTRAN	28	9	*
IBM 7090	FORTRAN	27	28	
CDC 1604	FORTRAN	12	54	
H 800	FORTRAN	77	264	
GE 225	WIZ	156	26.5 min.	Line printer O/P
IBM 1620	FORTRAN	260	38 min.	Card O/P*
IBM 1620	FORTRAN	260	38 min.	Card O/P*
RPC 4000	FORTRAN	38 min.	10.5 hrs.	Typewriter O/P

* These runs were made with a revised source program, which performs approximately 70% of the computation and gives 50% of the output, as compared to the original source program.

EDITOR'S READOUT

A LONG VIEW OF A MYOPIC PROBLEM

First on anyone's checklist of professional problems is the manpower shortage of both trained and even untrained programmers, operators, logical designers and engineers in a variety of flavors.

While both recruiting and training are obviously priority budget items and costly ones at that, there are several other negative and expensive side effects to this problem.

In an employees' market predominated by inexperience, wages have become inflated, discontent with one's job and working conditions is increasingly evident, a general lowering of overall capability has occurred and the quality of individual productivity has suffered proportionately.

For an industry just emerging from the embryo state, the gravity of these symptoms are of major consequence and before the slightest improvement may be evident, the basic problem will undoubtedly grow far worse.

While the number of programmers per computer may tend to decrease, the population of machines will substantially outdistance automatic programming methods. For example, while there has been only slight improvement in the race to meet software deadlines, there is an alleged 7,000 orders in the IBM household for the 1401 alone and within one year, it may be reasonably assumed that today's population of computers will be doubled and so will the problem.

And since there is virtually nothing which *can* be done on an individual corporate basis to improve this condition, the profession has boldly faced the reality of its problem and aside from occasional collective mutterings, virtually nothing *has* been done.

Solutions however, can be found to most problems and the warm body shortage is no exception. Once again, application of the solution or in another sense, its practicality, requires a measure of careful thought.

It has been suggested for example, that the training of high school students in computer technology might provide the industry with a major segment of relief from its personnel problem but of course, the investment is substantial and the gains to be reaped are very long range, indeed. One dubiously incisive school of thought quite prominent in the industry, suggests that high schools should not be a haven for teaching even the fundamentals of programming. It is argued that carefully selected groups of college students enrolled in an advanced technical school, learn much more quickly than younger people. It is also argued that high schools should improve their courses in English and basic mathematics to better prepare young minds for the rigors of advanced technical training.

Both arguments are somewhat ludicrous since the current and projected outpourings of our finer technical colleges and universities will hardly prove of sufficient quantity (with no judgment as to quality) to relieve the personnel problem. Secondly, high school educators have shown little motivation to revise their triple R curriculum and no matter how lofty is the prestige of our elder statesmen, computing people can do little to affect a change.

More important perhaps is the fact that computing will ultimately exercise a substantial effect on almost every functional aspect of our lives and the gross lack of information and preponderance of misconception throughout the country remains unchanged. What better a method of shifting this tide and influencing an increasing number of youngsters toward a career in computing than to teach some semblance of the subject in their early years of education?

Of the very sparse number of efforts in this area (one of the more extensive experiments is reported on the following pages) most have indicated considerable success and all have reported surprising interest from the student body.

Directly pertinent to the personnel problem however, is the persistent report from teachers of high school computing and from a recent career guidance center at which the ACM was represented, that students as well as their career counsellors, are grossly misinformed concerning the requirements of entering this field or for that matter, about what a computer is, does, and even looks like.

It has been suggested by several professional observers, that most students have never seen a photograph of a gp, digital computer nor could many recognize it from previously implanted images recalled from the grotesque representations of popular cartoonists.

Many students are surprised to learn that one does not require a Ph.D. in mathematics from Carnegie or MIT to become a programmer. Others firmly believe that an advanced degree in electronic engineering is a prerequisite to operating edp equipment.

Finally, many of the young ladies attending senior classes in high school have been told that programmers are restricted to the male sex, and their consideration of this profession should be heartily discouraged.

The response to published material in this field has been overwhelming. Whenever a specific individual or firm is mentioned, literally hundreds of requests for additional information are received from students and their schools. Last year the Reader's Digest described the background of IBM's Bob Bemer as having included set designing in Hollywood and programming for the RAND Corp. Both IBM and RAND received a considerable influx of inquiries, some of which asked what specific substitutes for a set designer's background might be useful for programming. Others asked for recommendations on where set designing could be studied with the assumption that one could always learn computer programming, if necessary.

Assuming that there may be some merit in supporting a program of high school education in computing, the method of implementation becomes of principal importance.

Since no pattern of standardization has been developed for internal training programs or at the college level, there would be serious difficulty in establishing a firm, widely accepted high school curriculum at this time. The goal is certainly a worthy one but nevertheless, far too impractical for the moment.

Within more immediate reason is the prospect of colleges offering evening and summer sessions in computing fundamentals for selected groups of high school instructors. Manufacturers could contribute in a similar fashion at minimum expense and users such as RAND, SDC, MITRE and many of the larger business and scientific institutions might also initiate similar instruction.

To introduce school districts and boards of education to the prospects and advantages of a computing curriculum, several of the professional societies under the support and perhaps guidance of AFIPS might initiate contact and serve as missionary bodies.

In an industry well noted for its frequent sojourns into high speed tomorrows, there must be an attraction in the simple necessity of planning for personnel who can apply next generation hardware if and when it becomes available. Without a substantial inventory of well-trained, career-minded computerites, there is certainly little value in sustaining more adventuresome dreams. ■

INFORMATION SOURCES

For students seeking professional guidance on computing as a career, it may be suggested that they contact their local ACM, IRE or AIEE chapter or write to: American Federation of Information Processing Societies, P.O. Box 1196, Santa Monica, California; Association for Computing Machinery, 14 East 79th Street, N.Y. 21, N.Y.; IRE, Professional Group on Electronic Computers, 1 East 79 St., N.Y. 21, N.Y.; AIEE, Computing Devices Committee, 345 East 47th St., N.Y. 17, N.Y., or the National Machine Accountants Assoc., 524 Busse Highway, Park Ridge, Illinois.

Encouragement may also be given to contacting major computer manufacturers such as IBM, RemRand UNIVAC, Burroughs, RCA, Minneapolis Honeywell, etc., who may be able to provide literature on their equipment and perhaps an occasional machine manual.

Worthwhile literature which students may be referred to include: *Digital Computer Programming,* by D. D. McCracken, published by John Wiley & Sons, N.Y.; an article on salary ranges in computing published in the March, 1961 issue of *Transactions of the IRE* Professional Group on Electronic Computers; two booklets from RemRand titled *Programming, A New Profession For You* (#155.2) and *How The Computer System Works For You* (#UT1555.1A). Also meriting attention is a series of institutional ads from IBM titled *Mathematics Serving Man* (#520-0937). Another excellent orientation may be found in a booklet by Saul Gorn and Wallace Manheimer, *The Electronic Brain and What It Can Do,* published by Science Research Assoc., Chicago, Illinois.

While a Bachelor's Degree in mathematics is certainly desirable, it should be clearly stated to prospective computerites that it is not a requirement for entrance to the field. Certainly an interest in solving problems, working puzzles, playing chess or bridge, etc., might indicate an aptitude for this work. Undergraduate courses in finite differences, numerical analysis, computer programming, etc. in addition to some contact with actual machines would be helpful. For business data processing, emphasis on business education is obviously preferable.

A COMPUTER CURRICULUM FOR THE HIGH SCHOOL

report of a large-scale experiment

by GEORGE C. HELLER,* National Education Chairman, ACM, and Education Chairman, Computing Devices Committee, AIEE

Although many colleges and universities have extensive computer oriented curricula on the graduate level and many offer courses for undergraduates, only sporadic knowledge exists about the ability of pre-college students to understand and use computers. A large-scale educational experiment initiated during the Fall of 1960 by the Washington, D.C. Chapter of the Association for Computing Machinery (ACM) was intended to explore this uncharted territory.

During the last two years a computer-oriented program evolved as a direct result of the chapter's extracurricular courses. Currently this program consists of an elementary and an advanced sequence, and includes five separate courses. The elementary sequence, "Introduction to High Speed Digital Computation" offers three programming courses: an introductory course, an advanced course, and a course in programming a second computer. The advanced sequence, "Introduction to Computer Science," includes a course in computer design and a course on artificial intelligence and heuristic programming.

Each of these courses has now been taught to a class of high school students. In addition, the introductory programming course has been repeated several times using essentially the same syllabus.

Machines utilized during the course of instruction included the IBM 709, 7090, 1620, RemRand UNIVAC SS 80, RPC 9000 and CDC 160.

Representatives from various institutions contributing their time included American Research Bureau, American University, C-E-I-R, IBM Federal Systems, Melpar and the U. S. Air Force.

A direct result of the interest of high school teachers in this program was the introduction of a computer oriented mathematics unit in the 12th grade mathematics curriculum in the high schools of Montgomery County, Maryland.

the large-scale experiment

In early January, 1960, the Washington, D. C. Chapter of ACM approached the Superintendent of Schools of Montgomery County, Maryland, offering to conduct a digital computer course. By September, the ground rules were set and the course was organized.

Students volunteering for this extracurricular course, added three additional class hours per week and an average of four to five additional hours of homework a week to their schedule. Entrance requirements for the course included: grades of A or B in all regular class work; two

***In addition to his by-lined activities, George Heller is employed full time for IBM Federal Systems, Bethesda, Maryland. The following description of his education activities represents part one in a two part series. Next month, an *outlook* for computing education in high schools will be offered.**

years of algebra, one year of geometry, one year of physics or enrollment in one of the latter two courses; and a high degree of interest in mathematics and science.

The topics in this initial course covered the history of computers, binary and octal number systems, analysis of typical problems, fundamentals of programming and computer applications. Students first learned to program a simple, hypothetical computer. They then progressed to writing programs for the IBM 709 using actual machine manuals as class material. To treat additional topics in computer programming and computer technology, films were used extensively. The syllabus for this course appears in figure 1. To enhance the educational breadth of the course, several leading authorities on scientific and business applications were invited as guest lecturers.

In response to the tremendous interest generated among both students and local educators by this course, "Introduction to High Speed Digital Computation I" the Chapter enlarged the experiment several fold during the next term. During the Spring term of 1961 a total enrollment of 368 students attended courses in five of the school districts in the greater Washington, D. C. area. Thirteen new classes had been organized, consisting of eight full term courses all using essentially the syllabus in figure 1, and five abbreviated courses using the syllabus shown in figure 2. One hundred and thirty nine students in Maryland and Virginia took the short courses, instructed by their own school teachers who were concurrently attending the full term courses.

The second course in the sequence "Introduction to High Speed Digital Computation II" was given at Bethesda-Chevy Chase High School during the Spring of 1961. This class began with advanced applications, including the application of linear programming in determining maximum profits in making ice cream sodas. A discussion of automatic programming touched briefly on FORTRAN, ALGOL, COBOL, SLANG, COMIT and LISP. Working in small groups, the class spent most of the term writing and testing an assembly program and a 709 simulator of the "Simple Computer" introduced during the first term. The course ended with a brief discussion of computer design and Boolean algebra. The syllabus for this course is shown in figure 4.

In June of 1961 the 209 students completing one or both full term courses received diplomas from the Washington, D. C. Chapter of ACM. The four school districts in which the program was most successful had a total

Figure 1.

15 Lesson Syllabus For
INTRODUCTION TO HIGH SPEED DIGITAL COMPUTATION
(High School Course on Computers)

1. *Introduction.* Background on history of computers, need for computers. What is a computer, analog and digital computers, use of computers in scientific and business areas.
2. *Number Systems.* Decimal, binary, octal and their use. Conversion from one system to another.
3. *Basic Concepts of a Computer.* General description of a computer, specific discussion on computer components: input, output, arithmetic unit, storage, control. Exhibit of such devices, use of desk calculators and card punch equipment, if available.

4.-5. *Analysis of Problems.* Logical and flow chart analysis of typical problems, needs for such analysis.

6.-13. *Programming a Computer.* The language of a computer, instructing a computer to solve a problem, demonstration and use of a computer.

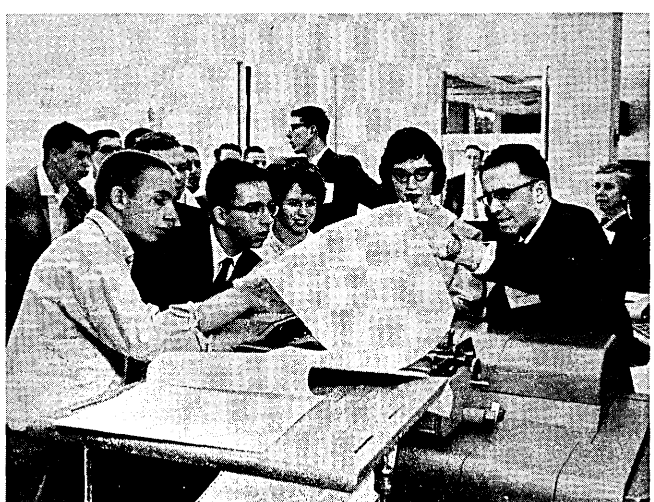
14.-15. *Applications of Computers.* Data Processing — use of computers in business applications.
Scientific Computing. Satellite tracking, design of missiles, war gaming, language translation, automatic programming.
Other applications and future developments in the computer area.

Figure 2.

5 Lesson Syllabus for
INTRODUCTION TO HIGH SPEED DIGITAL COMPUTATION
(Short High School Course on Computers)

1. *Introduction.* Background on history of computers, need for computers. What is a computer, analog and digial computers, use of computers in scientific and business areas.
2. *Basic Concepts of a Computer.* General description of a computer, specific discussion on computer components: input, output, arithmetic unit, storage, control.
   Movie: Memory Devices. 28 min., black & white, 16 mm.
3. *Introduction of the Simple Computer.* Logical and flow chart analysis of typical problems, need for such analysis. The language of a computer, instructing a computer to solve a problem.
   Movie: Computer Programming. 33 min., black & white, 16 mm.
4. *Review of the Simple Computer.* Introduction to symbolic programming and to assembly programs. Detailed discussions of the homework set.
5. *Class Demonstration* of a game that teaches the fundamentals of computer operation. Counters, shift registers and adders will be organized and operated by members of the class who will be acting as "components" of the computer.

The output of the rocket problem is observed by the students taking part in the education program. George Heller (right) explains the printed results.



Peter Loffan (center) debugs his chess problem on the 709 at the IBM Space Center in Washington. Aiding him are students Tommy Price and Elaine Ross.

enrollment of 316 students of whom 303, or 96%, completed their courses. Among those 177 students enrolled for a full term's work; 164 or 93% completed it successfully.

summer courses

In the summer of 1961, the experiment was carried forward into advanced training for superior students. One group explored symbol string manipulation, symbolic logic, Boolean function operations, and the experimental IBM 709 programming of "Qubic," using FORTRAN to develop an acceptable game program for three dimensional tic-tac-toe.

Eight juniors and four seniors from four Montgomery County, Maryland high schools participated in another course, "Introduction to High Speed Digital Computation III." This advanced high school course attempted to determine whether a group of high school students experienced in the use of one computer could be introduced to a conceptually different computer on an accelerated schedule. The class learned the new computer, the IBM 1620, in eight hours composed of four weekly sessions of two hours each. During the remainder of the term the students pursued special projects. Of particular interest among these were a partial chess game, a tic-tac-toe game, a musical transposition program, the simulation of a roulette wheel and a solution of the rocket firing simulation. The University of Maryland cooperated in this experiment by making class room facilities and its IBM 1620 computer available.

The students received their first programming assignment during the first meeting of the class. They prepared their program and that same evening debugged it on the 1620. The next three meetings covered additional classroom instruction and practice on the computer. In the fifth meeting the class reviewed special machine features and FORTRAN, and in the last five classes each student devoted his efforts to solving individual term problems using the 1620. Total instruction time in this course was 20 hours.

1961-'62 school year

The large scale experiment picked up added momentum during the Fall of 1961. Six courses with well over a hundred students were organized in Washington and in the suburban communities of Maryland and Virginia. "Introduction to Computer Science I," the first of the advanced sequence of computer courses, was offered at Bethesda-Chevy Chase High School to 15 seniors from four Montgomery County High Schools. The class learned computer design, using E. M. McCormick's *Digital Computer Primer* (McGraw-Hill, 1959) as their text. The syllabus of the course appears in figure 5, and one of the final examination questions is shown in figure 6. The students were selected from among the juniors who had participated in the 1960-61 large scale experiment. Among the original contributions made by students, one young lady of 17 designed a small computer. Another student simulated a minus two base computer on the 1620, and a third worked on neural network simulation. So significant was the latter work, that a paper was submitted for evaluation to the Program Committee of the 1961 Eastern Joint Computer Conference. The paper, CONTRANS, (Conceptual Thought, Random-Net Simulation) was referred via regular channels and accepted for and presented at the 1961 EJCC.

Concurrently with the computer design course, several of the beginner's programming courses were offered in 1961-62. The classes oriented toward the 709 used as a text Leeds and Weinbers's *"Computer Programming Fundamentals"* (McGraw-Hill, 1961.) As in the previous year, movies proved quite valuable in presenting many

Figure 3.

ACM COMPUTER COURSE
FIRST SEMESTER — FINAL EXAM
(EXTRACT)

True or False — 3 points each — 5/26/61

1. The octal equivalent of 32767 is 777777.
2. The stored program concept allows data and instructions to be treated interchangeably.
3. Indexing allows a program to select sequential items of data thru modification of the instruction address in - - - machine registers.
4. Decimal data can be handled directly in a binary digital computer.
5. A program that is coded 'straight-line' operates faster than one that uses index loop control.

Multiple Choice — 5 points each — Choose best answer.

6. The instruction CLA TABLE+10, 4 will
   A — Place the C(TABLE) into the AC.
   B — Add the C(TABLE) to the AC.
   C — Place the C(TABLE)+10)—C(XR4) into the AC.
   D — Place the C(TABLE+10—C(XR4) into the AC.
   E — Place the C(TABLE+10+C(XR4)) into the AC.

Figure 4.

12 Lesson Syllabus for
INTRODUCTION TO HIGH SPEED DIGITAL COMPUTATION II
(Advanced High School Course on Computers)

1-4 *Applications of Computers.* Advanced applications in science and business.
Linear programming, mathematical models, war gaming, information retrieval, language translation, logistics, management science, applications in medicine.

5-10 *Automatic Programming.* Simulators, Assemblers, Compilers. Brief descriptions of the programming languages of FORTRAN, ALGOL, COBOL, and SLANG. Introduction to the specialized programming languages of COMIT and LISP. Outline of the SOS system.
The class will work in small groups toward the solution of a simple, yet unsolved problem of writing an assembly program for the "Theoretical Computer" introduced in the first half of the course.

11-12 *Elements of Computer Design.* Basic problems of designing a computer. Boolean Algebra.

Figure 5.

10 Lesson Syllabus for
INTRODUCTION TO COMPUTER SCIENCE I
(High School Course on Design of Digital Computers)

1-2. *Review of programming* and other topics covered in the sequence of courses "Introduction to High Speed Digital Computation."

3. *Review of the methods of representing numbers* with an emphasis on factors important to computer design. Complements.

4-6. *Application of logic to computer design* and operation. Basic logical connectives and their relation to the normal non-mathematical expressions of logic. Logical representation and manipulation by means of Boolean Algebra. Simplification techniques. The logic of basic control and storage devices of computers. Fundamental computer control functions.

7. *Serial Adders.* Equivalence of 2-input binary addition and logical operation of inequivalence (exclusive OR). Half adders. The "minimization" problem. Full serial binary adders. Linkage of serial adder to a register of flip-flops. Simulation of serial adders using human logic elements.

8. *Parallel adders;* the carry problem. Simulation of parallel adder stages. Review of timing considerations; connection of combinational circuits to flip-flops; "clocking;" depth of logic. Decimal adders. Subtraction in decimal adders.

9. *Multiplication.* Storage principles. The square loop magnetic core. Coincident current selection. Word organized core stores. Human simulation of storage access. Drum, disk, tape, and core compared. Future store systems.

10. Review and Final Examination.
TEXTBOOK: *Digital Computer Primer by E. M. McCormick,* McGraw-Hill Book Company, Inc., 1959

of the broader aspects of programming and computer technology. It is particularly significant and indicative of the effort of both students and instructors that in 1960-61, and again in 1961-62, beginning courses appeared in the regular curriculum of several local high schools as part of senior mathematics courses. In these classes the mathematics teacher provided the instruction and the students received credit toward graduation for the courses.

Encouraged by the excellent results of the computer design course, the topic selected by the ACM Education Committee for the Spring of 1962 was artificial intelligence and heuristic programming. Under the title of "Introduction to Computer Science II" the course is currently under way. The 15 lesson syllabus is shown in figure 7. The class has completed the study of IPL V using the manual edited by Allen Newell (Prentice Hall, 1961.) Symbolic logic is currently on the agenda. A sample homework set is shown in figure 8. Fourteen seniors and two juniors are enrolled representing four high schools in the Montgomery County School system. A new introductory course this term brings the total courses this year to seven.

Members of the Education Committee who contributed their time and effort to this year's program as instructors came from the American Research Bureau, Control Data Corporation, Datatrol, General Kinetics, IBM, James Madison High School (Vienna, Va.), National Institute of Health, and the National Science Foundation. The IBM 1620 and 709 and the CDC 160 were used for program checkout.

contributions from industry

In cooperation with the Education Program of the Washington, D. C. Chapter of ACM, several thousand books, booklets and pamphlets on computers were contributed by several industrial companies. These were given to students or donated to libraries of the schools. Among them was a bookshelf of thirty books presented to Walter Johnson High School by *Datamation* as part of the Junior Achievement Award of the 1961 EJCC. Another part of this award, a movie entitled "Computer Programming" was given, jointly, by *Datamation* and the System Devolpment Corporation to the Montgomery County School System. Many posters and library exhibits are used in the schools to publicize computer courses.

Approximately thirty ACM members participated in making a major contribution to full term courses during the last two years. Many more pitched in with individual lectures, seminars, debugging sessions, and project assistance.

plans for the future

The approach presented here is one that worked well in the Washington, D. C. area. The extra-curricular program developed by the Washington, D. C. Chapter of ACM is now being considered as the basis for a four year high school course in computer technology. Current plans call for the development of additional courses and the standardization and detailed documentation of the courses conducted in this large-scale experiment.

Thus far this exploration has attracted the enthusiastic attention of many able and gifted young people and it aroused the interest of the cooperating members of the teaching profession. ■

Figure 6.

WASHINGTON, D.C. CHAPTER OF ACM
INTRODUCTION TO COMPUTER SCIENCE I
(Introduction to Logic Design)

Fall Semester at Bethesda-Chevy Chase High School
H. E. Tompkins

Saturday January 6, 1962
EXTRACT FROM FINAL EXAMINATION
2 Hrs - Closed Book

2. (30 minutes) In a recent homework problem you desiged an excess-3 decimal adder. Now design the logic for a checking circuit to insure that the 4-bit output of the adder is one of 10 allowed excess-3 digits. Your circuit should fit into the system sketched below and should operate as follows: When the clock pulse occurs the output of the adder should be transmitted to the output of the check circuit if and only if that adder ouput is one of the 10 valid combinations of four bits that are in the excess-3 code. If the adder output is not a valid excess-3 digit, a pulse should appear on the *alarm* line, and no signal should appear on the check-circuit outputs.

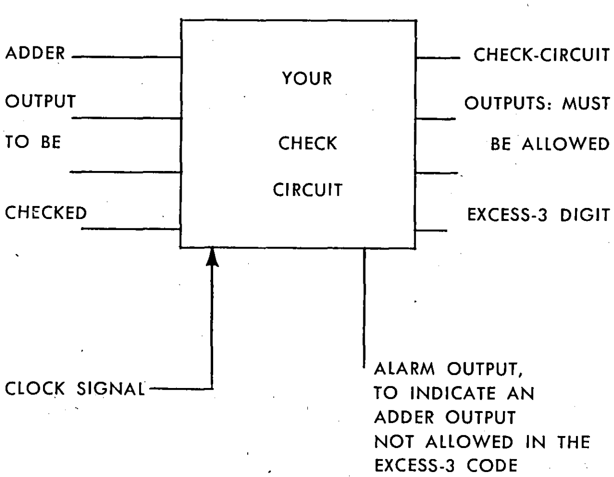


Figure 7.

15 Lesson Syllabus for
INTRODUCTION TO COMPUTER SCIENCE II
(High School Course on Artificial Intelligence and Heuristic Programming)

1. *Introduction*. What is heuristic programming? Preliminary considerations. Information Processing Language IPL V, its relationship to FORTRAN, COMIT, LISP, SAP. The elements of the IPL Computer, and IPL Programming.

2-4. *IPL V*. A detailed description of the language. Programming examples.

5. *Experimental Programs Underway*. Mechanical Translation, Artificial Intelligence, Character Recognition, etc. Heuristic Programming and Computer Design.

6-9. *Symbolic Logic*. An introduction. Sentential Connectives, Sentential Theory of Inference, Theory of Definition, Symbolizing Languages, Theory of Inference, Elementary Set Theory, The Axiomatic Method, the Concept of Formalization of Language, Logic, Mathematics. Some useful theorems.

10-12. *Heuristics*. Computability vs. Unsolvability, Turing Machines, Simulation of Thought Processes, Critique of Current Efforts.

13-15. Individual term projects.

Figure 8.

INTRODUCTION TO COMPUTER SCIENCE II
Session 3
Homework Assignment

A. Read: IPL-V Manual, pp. 44-83, 163-168, 179-206

B. Problems: Consider the function E, defined for non-negative integers as follows:

(1) $E(I, J) = E(I-1, J) + E(I-1, J-1)$
(2) $E(I, 0) = 1$
(3) $E(0, J + 1) = 0$

Write a program in IPL-V
(a) to evaluate E(I, J) for all I, J. Store E(I, J) in a form suitable for subsequent table lookup.
(b) to find the sum for all J for any given I, i.e. $E(I, 0) + E(1, 1) + \ldots + E(1, N)$

Statistical surveys concerning the employment of edp equipment in institutes of higher learning were compiled recently by Clarence B. Lindquist, Division of Higher Education, U.S. Office of Education, for the American Mathematical Society, and by Dr. Roy F. Reeves, Director, Numerical Computation Laboratory, the Ohio State Research Center, Columbus, Ohio.

In 1961, AMS queried more than 1,000 colleges and universities who grant bachelor and higher degrees in mathematics, asking for the make and model number of each digital computer on the campus of the institution, and the year of installation of each. A total of 164 computer centers responded. The accompanying breakdown of installations is the result of the two surveys.

In publishing this compilation, DATAMATION hastens to point out that it is hardly definitive in its scope but merely reflects the findings of two competent surveys of the field. Additions, comments or corrections which would update this report should be addressed to Editor, Datamation, 10373 W. Pico Blvd. Los Angeles 64, California.

COMPUTING IN THE UNIVERSITY

two surveys report on $115-million of hardware installations

An imposing array of hardware valued at more than $115-million is currently in use in American colleges and universities, from 15-year-old configurations such as MANIAC I at the University of New Mexico and UNIVAC I at the University of Chicago to New York University's IBM 7090 and CDC 1604.

Ten large-scale solid-state systems are reported in operation, divided largely between Control Data Corporation's 1604 and IBM's 7090. Among first-generation computers, large-scale installations show eight IBM 709's, five 704's, two UNIVAC 1103's, and one UNIVAC 1105.

Four major trends in the university computing field are apparent: 1. Many universities which have been in the computing field since 1945 are replacing first generation models with solid-state hardware; 2. Others who have never used edp equipment have recently acquired their first computers; 3. Some institutions are retaining their tube equipment and adding solid-state systems, and 4. Schools with limited budgets are using first generation machines in increasing numbers.

The country's largest universities, U. C. (Berkeley), UCLA, and N.Y.U., with enrollments ranging from 14-25K, are equally prominent in the acquisition of computing equipment.

However, size of student body does not appear to play a leading roll as far as computer usage or acquisition is concerned. Some of the comparatively smaller schools also show considerable activity in computer sciences: Scripps Institute of Oceanography has installed a CDC 1604; the University of Rochester (N.Y.) an IBM 7090; and the University of Southern California has a Honeywell 800 and RemRand SS 80.

For sheer numerical weight of hardware concentrated on one campus, MIT weighs in with no less than ten

Manufacturers of university-operated computers.

Bendix	30
Burroughs	21
Control Data	7
General Electric	2
Honeywell	1
IBM	138
National Cash Register	1
RemRand	12
Royal McBee	32
Special Makes	15
	275
On Order:	
Burroughs	1
Control Data	5
IBM	16
RemRand	2
	24

installations: IBM 704; 2 650s; 4 LPC-30s; Bendix G-15; TX-O; and IBM 709. (This does not include computers in use at the Lincoln and Mitre Laboratories.)

Large-scale systems reported on order include a UNIVAC 1107 for the University of Notre Dame and for Case Institute. Expecting deliveries in the medium-to-large scale range are Stanford University, Burroughs B-5000, and Washington University, St. Louis, an IBM 7072.

UNIVERSITY HARDWARE

State-by-state breakdown of university-operated edp equipment, as compiled by the American Mathematical Society and the Ohio State Research Center. Figures in brackets show reported date of installation.

ALABAMA:

Auburn University	IBM 650 (1959)
University of Alabama	RemRand SS/80 (1961)

ARIZONA:

Arizona State Univ.	G.E. 304 (1960)
Univ. of Arizona	IBM 650 (1957)

ARKANSAS:

Univ. of Arkansas	IBM 650 (1960); Bendix G-15

CALIFORNIA:

Calif. Institute of Technology	Burroughs 220; Bendix G-15
Calif. State Poly. College	Bendix G-15 (1960)
Chico State College	IBM 1620 (del. 1962)
Claremont Men's College	Bendix G-15 (1960)
Harvey Mudd College	IBM 1620
Los Angeles City College	Bendix G-15
Los Angeles State College	IBM 650 (1961)
Pacific Union College	Bendix G-15 (1961)
Pomona College	2 Bendix G-15s (1958)
Sacramento State College	Royal McBee LGP-30
San Diego State College	IBM 650
San Jose State College	IBM 650
Scripps Institute	CDC 1604; Bendix G-15
Stanford University	IBM 650 (1957); Burroughs 220 (1960); IBM 1401; IBM 7090; (on order: Burroughs B-5000.)
University of Calif. at Davis	IBM 1620 (1961)
Univ. of Calif. at Berkeley (does not include computers at Lawrence Radiation Lab. and other AEC projects.)	IBM 701 (1956); 2 Bendix G15's (1959); IBM 704 (1959); IBM 1620 (1961); (on order: IBM 1620.)
Univ. of Calif. at Los Angeles	SWAC; IBM 7090 (1961); IBM 1401 (1961); Bendix G-15; (on order: IBM 1401; variable logic computer under construction.)
Univ. of Calif. at Riverside	IBM 1620
Univ. of Calif at San Diego	CDC 1604 (1961); CDC 160A (1962)
Univ. of Southern California	RemRand SS/80 (1961); Honeywell 800 (1961)

COLORADO:

Colorado State University	IBM 1620 (1961)
Univ. of Colorado	Bendix G-15 (1958)
University of Denver	Burroughs 205 (1955)

CONNECTICUT:

Wesleyan University	Royal McBee LGP-30
Yale University	IBM 610; 650; 1401; 709; 1620

DELAWARE:

University of Delaware	Bendix G-15 (1958)

DISTRICT OF COLUMBIA:

American University	3 Royal McBee CPCs
George Washington Univ.	The Logistics Computer (1951); Abel (1951)
Georgetown Univ.	2 Burroughs E-101

FLORIDA:

Florida State Univ.	IBM 650
Univ. of Florida	IBM 650 (on order: IBM 1620)

GEORGIA:

Georgia Institute of Tech.	UNIVAC 1101; Burroughs 220; IBM 650
Georgia State College	IBM 305 RAMAC; IBM 1620
Univ. of Georgia	IBM 650 (1960)

HAWAII:

University of Hawaii	IBM 650 (1959)

ILLINOIS:

Illinois Inst. of Technology	IBM 650
Northwestern Univ.	IBM 650 (1958); IBM 709
Southern Illinois Univ.	IBM 650 (1959)
Univ. of Illinois	ILLIAC; IBM 650
Univ. of Chicago	UNIVAC I; MANIAC III; 2 IBM 1620s; Royal McBee LGP-30

INDIANA:

Indiana University	IBM 650 (1956); Bendix G-15; (on order: IBM 709)
Purdue University	Burroughs 205; RemRand SS/80; IBM 1620; LGP-30; 2 RPC-4000s
Rose Polytechnic Inst.	Bendix G-15 (1960)
Univ. of Notre Dame	IBM 610 (on order: UNIVAC 1107
Valparaiso Univ.	IBM 610

IOWA:

Iowa State Univ.	IBM 650 (1957); CYCLONE (1959)
State University of Iowa	IBM 7070 (1961); IBM 1401 (1959)

KANSAS:

Kansas State University	IBM 650 (1958)
University of Kansas	IBM 650; (on order: IBM 1620)
University of Wichita	IBM 1620 (1961)

KENTUCKY:

University of Kentucky	IBM 650; 1620
University of Louisville	IBM 1620 (1960)

LOUISIANA:

Louisiana Polytechnic Inst.	Royal McBee LGP-30
Louisiana State University	IBM 650; 1620
Tulane University	IBM 650 (1958)
Univ. of Southwestern Louisiana	IBM 1620

MARYLAND:	
Johns Hopkins University	Royal McBee LGP-30; IBM 1620; 7090; (on order: IBM 1401)
Univeristy of Maryland	IBM 1620; LGP-30; (on order: IBM 1401)
MASSACHUSETTS:	
Boston University	IBM 650
Harvard University	UNIVAC I; IBM 650; IBM 7090; 2 Bendix G-15s
Lowell Technological Inst.	On order: Royal McBee RPC 4000
Massachusetts Inst. of Tech. (excluding computers at Lincoln and Mitre Labs.)	IBM 704; 2 650s; 4 LPG-30s; Bendix G-15; TX-O; IBM 709
Northeastern Univ.	IBM 650 (1959)
Univ. of Massachusetts	On order: IBM 1620
Worcester Polytechnic Inst.	IBM 610 (1959)
MICHIGAN:	
General Motors Institute	IBM 1620
Lawrence Institute of Tech.	Burroughs E-101
Michigan College of Mining	Bendix G-15
Michigan State University	MISTIC (1956) (on order: CDC 160; 1604)
University of Detroit	Burroughs E-102 (1956); IBM 1620 (1961)
University of Michigan	IBM 704 (1959); 709 (1960)
Wayne State University	IBM 650 RAMAC
MINNESOTA:	
Carleton College	IBM 610 (1959)
St. Olaf College	IBM 610 (jointly with Carleton College)
University of Minnesota	UNIVAC 1103 (1958) (on order: CDC 160; 1604)
MISSISSIPPI:	
Mississippi Southern College	On order: RPC 4000
Mississippi State University	IBM 650 (1958)
University of Mississippi	IBM 650 (1958); IBM 1620
MISSOURI:	
Drury College	LGP-30 (1959)
Lincoln University	IBM 1620 (1961)
Missouri School of Mines	LGP-30; IBM 1620 (1961)
St. Louis University	IBM 610; 1620 (1961)
University of Missouri	Burroughs 205 (1960)
Washington University	IBM 650; (on order: IBM 7072)
MONTANA:	
Montana State College	IBM 650; IBM 1620 (1961)
NEBRASKA:	
University of Nebraska	Burroughs 205 (1960)
NEW HAMPSHIRE:	
Dartmouth College	LGP-30 (1956)
University of New Hampshire	IBM 1620 (1961)
NEW JERSEY:	
Newark College of Engineering	On order: IBM 1620
Princeton University	IBM 650; (on order: IBM 7090)
Rutgers, The State University	IBM 650 (1957)
Stevens Institute of Tech.	IBM 1620 (1961)
NEW MEXICO:	
New Mexico State University	Burroughs 220; Bendix G-15
University of New Mexico	CRC 102-A (1957); MANIAC I
NEW YORK:	
City College of New York	LGP-30 (1960)
Clarkson Institute of Tech.	IBM 1620 (1961)
Columbia University	IBM 650 (1954); IBM 650 (1958); 1620 (1961)
Cornell University	Burroughs 220 (1959); 2 Bendix G-15s (on order: CDC 160A; 1604)
Fordham University	Bendix G-15 (1959)
New York University	IBM 704; 650 (1961); 7090 (1961); CDC 1604 (1961)
Polytechnic Inst. of Brooklyn	IBM 650; Bendix G-15
Pratt Institute	IBM 1620 (1961)
Rensselaer Polytechnic Inst.	IBM 650 (1958)
Syracuse University	IBM 650 (1959)
University of Rochester	IBM 650; 7090
NORTH CAROLINA:	
Duke University	IBM 7070
Univ. of North Carolina (Raleigh)	IBM 650 (1956)
Univ. of North Carolina (Chapel Hill)	UNIVAC 1105 (1959); LGP-30
OHIO:	
Case Institute of Technology	UNIVAC I (1958); Burroughs 220 (1960); (On order: UNIVAC 1107)
Fenn College	Burroughs 205 (1960)
John Carroll University	LGP 30-66 (1960)
Miami University	IBM 650
Ohio University	LGP-30
Ohio State University	IBM 704 (1958); IBM 709; 1620
University of Cincinnati	IBM 650 (1958) Burroughs E-102
University of Dayton	NCR 304; Burroughs 205; Burroughs 220
Western Reserve Univ.	G. E. 225
OKLAHOMA:	
Oklahoma State Univ.	IBM 650
University of Oklahoma	IBM 650; 1410; OSAGE
OREGON:	
Oregon State University	ALWAC III E (1957); IBM 1620 (1961)
University of Oregon	IBM 1620
PENNSYLVANIA:	
Bucknell University	Burroughs E-101 (1959); IBM 1620 (1961)
Carnegie Inst. of Technology	IBM 650 (1957); Bendix G-20
Drexel Institute of Technology	IBM 650; 1620
Lafayette College	IBM 607
Lehigh University	LGP-30 (1957)
Pennsylvania State Univ.	IBM 650 RAMAC (1959) 7070 (1962)

Temple University	IBM 650
Univ. of Pennsylvania	UNIVAC I; LGP-30; RPC 4000
Univ. of Pittsburgh	IBM 7070
Villanova University	IBM 1620 (1961)
PUERTO RICO:	
University of Puerto Rico	IBM 650 (1958)
RHODE ISLAND:	
Brown University	IBM 7070 (1960)
University of Rhode Island	IBM 610
SOUTH CAROLINA:	
Clemson College	RPC 4000
Univ. of South Carolina	LGP-30
TENNESSEE:	
Christian Brothers College	On order: IBM 1620
Tennessee Polytechnic Inst.	IBM 1620
Univ. of Tennessee	IBM 1620 (1961)
Vanderbilt University	IBM 650 (1959)
TEXAS:	
Howard Payne College	LGP-30 (1960)
Lamar State College of Technology	LGP-30 (1958)
Rice University	Computer built by Rice and similar to MANIAC II; LGP-30
Southern Methodist Univ.	UNIVAC 1103; SS/90; UNIVAC 120
Texas A & M	IBM 650 (1956) 709 (1961)
Texas Technological College	CRC 102-A (1959); Litton 20-40 (1960); (tentative: IBM 1620)
Texas Western College	Bendix G-15
Trinity College	LGP-30
University of Houston	IBM 650
University of St. Thomas	Bendix G-15
University of Texas	CDC 160 (1961); CDC 1604 (1961)
UTAH:	
Bringham Young Univ.	IBM 650 (1958)
University of Utah	Burroughs 205
Utah State University	IBM 1620
VERMONT:	
University of Vermont	IBM 1620 (1961)
VIRGINIA:	
University of Virginia	Burroughs 205 (1960)
Virginia Polytechnic Inst.	IBM 650 (1958)
WASHINGTON:	
Univ. of Washington	IBM 709 (1960); IBM 650
Washington State Univ.	IBM 650 (1956); (on order: IBM 709)
WEST VIRGINIA:	
West Virginia University	IBM 610 (1958); 650 (1960)
WISCONSIN:	
Marquette University	IBM 650 (1958); (on order: IBM 1620)
University of Wisconsin	CDC 1604 (1961); 3 IBM 1620s (1961; Bendix G-15
WYOMING:	
University of Wyoming	Bendix G-15 ■

U.S. PAPERS SET FOR IFIP CONGRESS

The IFIP Program Committee has released the titles of American papers—both submitted and invited—which will be read at the IFIP Congress 62, to be held in Munich, August 27-September 1. In addition, the organizers of symposia and panels were also announced.

Included in the list of submitted papers are: *Toward Inductive Inference Automata,* L. J. Fogel, Bell Telephone Laboratories; *Mathematical Analysis of Merge-Sorting Techniques,* W. C. Carter, IBM; *Extending Management Capability by Electronic Computers,* A. Vazsonyi, Thompson Ramo Wooldridge; *Generalization of an Elementary Perceiving and Memorizing Machine,* E. A. Feigenbaum, Univ. of Cal., and H. A. Simon, Carnegie Tech; *An Experimental System for Logic Design—Data Accumulation and Retrieval,* R. J. Preiss, IBM; *The Multi-List System for Real-Time Storage and Retrieval,* N. S. Prywes and H. J. Gray, Univ. of Pa.; *An Algorithm for the Translation of ALGOL Statements,* W. M. Keese and H. D. Huskey, Univ. of Cal.; *Computer to Computer Communication at 2.5 Megabits/Sec.,* N. Clark and A. C. Gannet, Control Data Corp.

Invited papers include: *Automata Theory,* A. W. Burks, Univ. of Mich.; *Standardized Comparisons of Computer Performance,* R. L. Sisson and J. A. Gosden, *Auerbach Electronics; Pulse Mode and Fundamental Mode Operations of Sequential Circuits,* E. J. McCluskey, Princeton Univ.; *Problem Solving, Learning and Generality,* A. Newell, Rand Corp.; *Information Retrieval—Review and Prospectus,* A. Kent, Western Reserve Univ.; *High-Speed Memories,* W. E. Proebster.

Other invited papers will be read by Grace M. Hopper and J. P. Eckert, RemRand, and J. McCarthy, M.I.T.

Among the panel and symposia organizers are: J. Rajchman, RCA, *Symposium on Fast Memory Technology;* A. L. Samuel, IBM, *Symposium on Pattern Recognition;* M. Minsky, M.I.T., *Symposium on Artificial Intelligence;* R. W. Bemer, IBM, *Symposium on Programming Languages;* L. Fein, consultant, Palo Alto, Calif., *Panel on University Education in Information Processing;* M. L. Juncosa, Rand Corp., *Symposium on Optimum Routing in Large Networks;* A. S. Householder, Oak Ridge National Lab., *Symposium on Matrix Computations.*

Sixteen American firms will exhibit at IFIP Interdata: Ampex International Operations; Beckman Instruments; Bureau of National Affairs; CDC; DATAMATION; Electronic Engineers International; Friden; Hewlett-Packard; Honeywell; IBM; IT & T; NCR; Potter Instrument; UNIVAC; and Telex Inc., Data Systems Div.

Dr. Werner Buchholz, in charge of travel arrangements, has announced that reduced fares to Europe will be available to qualified groups of 25 or more persons. Complete information can be obtained by writing to Dr. Buchholz at IBM Corp., Development Laboratories, P. O. Box 390, Poughkeepsie, N. Y.

The U. S. members of IFIP, the American Federation of Information Processing Societies (AFIPS), is headed by Dr. E. L. Harder, vice president of AIEE. ■

TRAFFIC FLOW SIMULATION

NBS models Washington artery on 704

A three-year program utilizing data processing and display equipment to simulate traffic flow over a nine-block length of a principal traffic artery in downtown Washington, D. C., has been completed by the National Bureau of Standards.

The program, conducted by M. C. Stark of the NBS data processing systems laboratory for the Bureau of Public Roads, was to determine the results of proposed changes in traffic control measures without actually disrupting traffic. The test course selected was 13th Street, N. W., from Euclid Street to Monroe Street, and the computer used was an IBM 704.

Each lane of each street was divided into 12-foot sections called Unit Blocks (UB). A place for information on each UB was reserved in computer memory; if there was a car in a UB, full information on its exact location and its physical characteristics was stored. Another portion of the stored word furnished any necessary information about the road at that point.

The UBs were numbered consecutively wherever possible, facilitating a systematic search of successive UBs for cars to be processed, as well an orderly movement of each car from one UB to the next higher numbered UB. One quarter-second of simulated real time was the cycle for searching all UBs for cars, moving the cars, generating new cars and preparing outputs.

Traffic inputs were generated (using random numbers) to represent assumed input volumes. Every quarter-second, the 704 moved the cars according to "rules of the road" built into the program. The coordinates of the car positions and the traffic signal settings were written on mag tape output. The tape was later fed into SEAC (a specialized NBS computer) which was equipped with facilities for projecting the coordinates onto an oscilloscope and actuating the trigger of a camera to produce a series of photos capable of being processed into a real-time motion picture film.

The 704 program also printed out detailed data which described the generated cars, counted and clocked them as they passed an intermediate check point along the course, and finally checked out the cars as they finished the course. The film provided an overall view of the general performance of the vehicular fleet, while the read out provided quantitative material which measured and judged the performance.

The basic program, including the working constants and input parameters, contained about 6K words. In addition, the "A" layout (two words for each of about 1.8K UBs) used about 3.6K words and the "B" layout another 3.6K. A table look-up of the coordinates of each UB and traffic signal for presentation by SEAC on the oscilloscope used about 3.7K words. The total requirement was about 16K words. The 704 installation at NBS has 32K words of primary core storage so that no effort was made to conserve space. The program was assembled using the SAP assembly system.

(The final production run representing four minutes of real time required 60 minutes of 704 time, a ratio of computer time to real time of 15 to 1.)

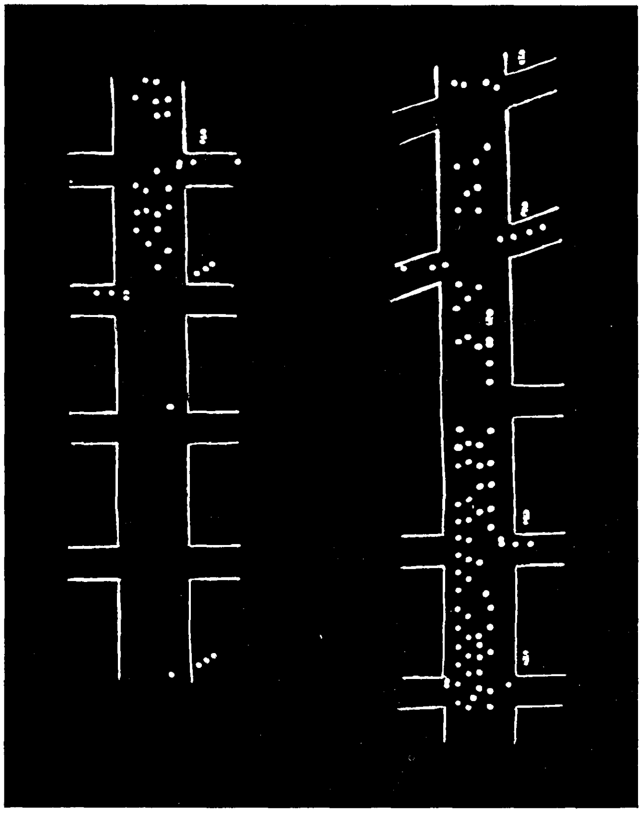
In operation, the program searched for cars to be processed, starting at UB-O, the first UB in Lane 1, then through Lanes 1, 2, 3, and 4 of 13th St., the lanes of all cross streets, and finally the diagonal UBs (for turns).

The cars found were on the "A" layout, and as each car was processed, it was moved to a new position on the "B" layout. (This was done since it was impossible to process all the cars simultaneously.) For the remainder of the review cycle, the car continued to appear on the "A" layout in its old position. When all cars found in the "A" layout were moved to new positions in the "B" layout, the scanning was completed. The "A" layout was erased and the "B" layout became the starting point for the next scan.

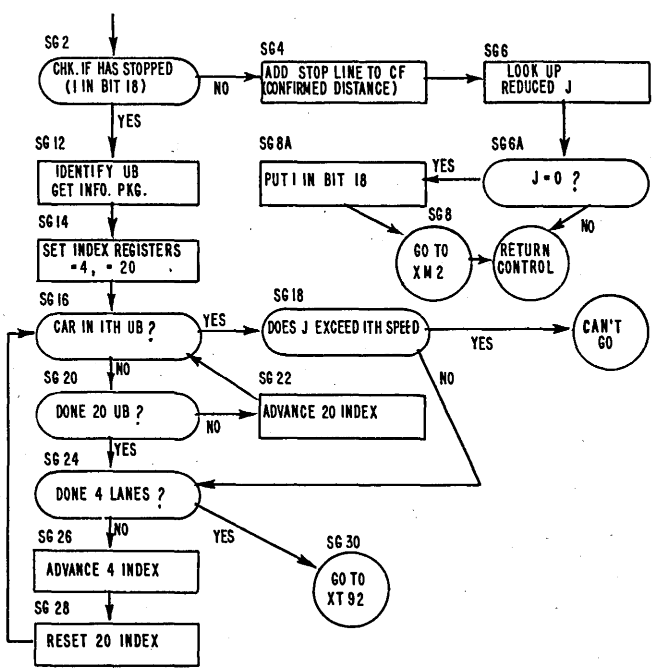
The car generation routine was performed at the end of each cycle. A newly generated car would be launched only if it could be done safely. Otherwise, it was retained on a backlog for the particular generation point in question until it could be launched safely.

The vehicles generated at each entrance were described by two words of 35 bits each. The first word and the first part of the second word described the car characteristics (if there happened to be a car in the UB), and the last part of the second word described the roadway at that point by noting the presence of one or more irregularities, if any existed. When a significant irregularity was noted, the program went to a table stored in memory where the

NBS traffic researchers prepare to make motion pictures of oscilloscope presentation of computer-simulated city traffic. In background, project director M. C. Stark, readies the Bureau's SEAC computer, while Leonard Cahn adjusts the oscilloscope on which the simulation is presented.



Single frame of motion picture produced from oscillograph. The course is photographed in two segments, beginning at lower right, ending at upper right. Traffic lights are shown as a bar of three lights: vertical configuration indicates green for 13th St. traffic, horizontal red, and diagonal amber. Single dots represent cars, double dots small trucks, and triple dots large trucks.



Flow chart of Stop Sign Routine. Before the car can proceed across the intersection, 20 approaching Unit Blocks are checked in each of the four lanes. If another car is present or moving, the car cannot proceed. Should an opposing car be farther away but moving at a critical speed, the stopped car cannot proceed.

necessary information was located for the particular UB. (During processing, the program was on the alert to comply with the requirements of any roadway "irregularity:" if a UB is responsive to a traffic signal, the program must check the signal indication; if there is a turn ahead, the program must test whether the car is intending to turn, etc.)

Characteristics included: time of departure in quarter-second intervals; type of vehicle—automobile, small truck, or large truck; exit point to be used (determining the route); and desired speed category—15, 20, 25, 30 or 35 m.p.h.

The edit routine noted the positions of the cars and the settings of the traffic signals, looked up the coordinates and wrote the information on the output tape to be used later for the SEAC display. The clocks were advanced one quarter-second and the program was ready to repeat the cycle.

Additional information was added within the vehicle two-word format as the entire course was surveyed at quarter-second intervals. Computations determined the length of each vehicle "jump," or distance traversed during an interval, and assigned to each its new actual speed and position, given by its unit block number and the hundredth's of the block length to which vehicle's nose had penetrated.

Vehicles approaching stopped vehicles in the same lane (where lane changing was not possible), a stop sign, or a red light were decelerated gradually, in the form of a quarter-second jump of decreasing size. A stopped vehicle was identified by its two-word description showing a zero jump and indicating the same position at successive intervals.

When the distance between any two vehicles in the same lane became less than the allowable net clear sight distance determined by both vehicles' speeds, the net clear sight distances for the overtaking vehicle in the two neighboring lanes were determined as part of the computations of each quarter-second interval.

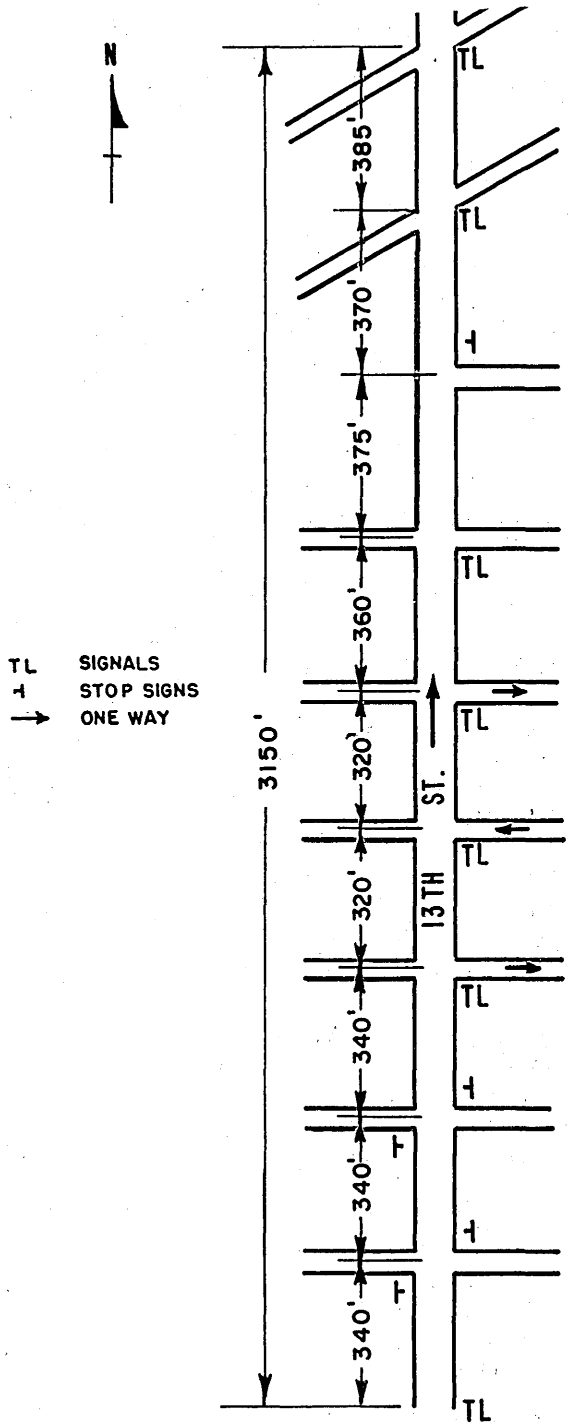
The three alternatives—stay in lane, switch to right, or switch to left—were evaluated at each interval and one was chosen which best permitted the desired speed to be attained. The overtaking car was switched to the lane selected by being moved through progressive straddle positions during the time required to make the change. Vehicles obliged to stay in the same lane were gradually decelerated to the speed of the leading vehicle.

The routes assigned to vehicles at the time of generation determined their behavior in complex intersection situations. Westbound vehicles were not permitted to turn left (13th St. was one-way northbound) and could always proceed through or turn right in the lane determined by route or lane preference assigned at time of generation.

Eastbound vehicles assigned a turn onto 13th St. were obliged to wait for a gap in westbound traffic. Those requiring a near or far lane because of a later turn waited to enter 13th St. on the appropriate lane. Those not assigned a later turn entered on the preferred lane (1 or 4), except for vehicles having a Lane 4 preference, which if blocked by oncoming traffic went on to enter at Lane 1, waiting there to turn if necessary.

Vehicles assigned to turn off 13th St. were "coaxed" into the appropriate lanes when within 1200 feet (100 UBs of the turn). A definite pattern of "last chance" unit blocks for each lane shift approaching each intersection was programmed. The cars made the necessary shifts in as rapid succession as possible when approaching the turning point, following the lane-switching rules.

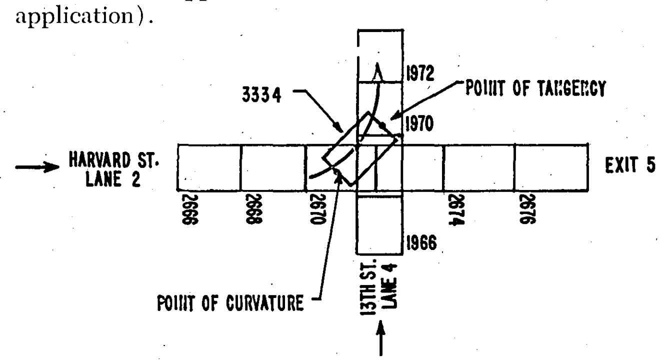
Four tabular printouts were obtained after every run. The Vehicle Generation Table gave the launch time, exit, type of vehicle, generating point, desired speed and lane preference for each vehicle. The Station B Check tabulated vehicles passing the maximum-load point of the course for comparison with empirical data. The Vehicle Retirement Table tabulated the individual running times and actual speed of vehicles completing the course in each lane, and for comparison with empirical data. The Marked Car Chronological Printout gave the location of each marked car every quarter-second for progress analysis. ("Marked cars" were used for sampling car performance and recording detailed movements of specific cars as an aid in debugging or analyzing a special situation.)



Layout of 13th Street. TL indicates location of traffic lights; arrows show direction of one-way streets. Stop signs are located at Fairmont, Girard and Lamont Street intersections with 13th.

While the simulation technique was said to have produced a model which apparently was made to correspond with actual field conditions, further applications are contemplated. These fall into three categories: those that can be done almost immediately; those that will require some changes and rewriting of the program; and those of longer-range nature that may require fairly extensive program changes.

Some of the future research tasks are: change volumes, turn ratios, lane distributions, traffic signal settings, desired speed for the specific course; plant a stalled car and see what happens; set up a solid line of cars to study the wave action; set up a conflicting turn action (immediate application); prepare an editing routine that will summarize output data at several levels of detail; substitute a yield sign for a stop sign; change any cross street from one-way to two-way (or vice versa); provide for buses which would stop at prescribed locations (intermediate application); make 13th St. two-way; study the problem of generalizing the computer model so that by merely "plugging in" proper data regarding physical layout, it can be made applicable to another set of streets (future application).



When making a simple turn, the car progresses through Unit Blocks 2666-2668-2670-3334-1970-1972. All information for making the turn is contained in UB 2670, such as if the car will turn, direction of turn, which lane car will enter after turning, and exit if car will not turn.

S.T.C. MODELS S.F. BRIDGE TRAFFIC

An analysis of the traffic flow pattern across the six bridges spanning San Francisco Bay is being conducted by Statistical Tabulating Corp. to determine whether the proposed Tiburon Bridge from San Francisco to Marin County would be instrumental in alleviating bay area traffic congestion.

Input to STC's recently-installed IBM 1401 will consist of 500K prepunched cards, distributed to motorists crossing the bridges, and returned for processing. Information on the card will indicate which bridge each motorist was crossing, direction of travel, date and hour of crossing, and whether the vehicle was private or commercial. The motorist added his point of origin and destination for the trip for which the card was issued.

In addition to measuring the economic feasibility of the proposed San Francisco-Marin bridge (which would be the longest suspension bridge in the world) the analysis will also determine the need for and desirability of a proposed southern bay crossing.

The over-all traffic movement will be projected on the basis of hundreds of simulated bridges, tunnels, causeways, and alternative approaches on both sides of the bay.

The information will be used by Coverdale and Colpitts, traffic engineers, in the firm's recommendations to the California Department of Public Works. ■

THE LANGUAGE PROLIFERATION

an unwholesome profile

by CHRISTOPHER J. SHAW, Sr. Programming Analyst,
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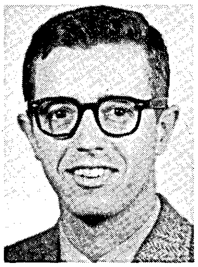


If there's just one thing in the computing field that almost every reasonable person agrees with — with the possible exception of professional compiler writers—it's the fact that there are too many programming languages in use these days. Not just machine-oriented programming languages (it's too late at this stage of the game to do anything about these except build interpreters) but too many problem- and/or procedure-oriented programming languages — languages that are supposedly machine independent.

This proliferation of "machine-independent" programming languages has two well-known and pernicious effects: it inhibits the communication of information processing procedures between people and computers both, and what's worse, it distracts attention and effort from that which is to be communicated — namely, procedures for solving real, worthwhile problems. Interestingly enough, these two effects are exactly those which each individual language is supposed to ameliorate. In conjunction, therefore, these languages tend to defeat their own purposes, with the result that the computing industry is, today, suffering from too much of a good thing.

By and large, the industry realizes this unwholesome situation and seems willing to expend considerable amounts of money and effort to rectify it. Two well-meaning attempts have already been made to bring some order out of the chaos, by the ALGOL folks and by CODASYL, and now the ASA X3.4 sub-committee has taken up the struggle. Measured by their ability to replace, or to inhibit the development of, competing languages, both ALGOL and COBOL have been only partially successful; it remains to be seen what X3.4 will accomplish.

why so many languages?

There's some excuse for the hundreds of different computers on the market — manufacturers like to make money — even if this excuse is not always justified by practice. But what's the excuse for all these different programming languages? *Nobody* makes money on them, except indirectly.

Many programming languages have been designed to fulfill their implementers' desire to break-in to the compiler-writing game. And once you've gone to the not inconsiderable trouble of writing a compiler, it does seem a shame not to use it. And since the language that such a home-made compiler accepts is not demonstrably any worse, usually, than the programming language used by the boys in the next county, these languages do get used. "Besides," the argument often goes, "our language has some built-in features that facilitate the kind of work we do in our shop, or will do, after we get the compiler checked-out."

Another reason for the existence of an overwhelming variety of programming languages is the fact that most of these languages are not machine independent. Even the ones that claim to be are not really. Thus, the motivation toward a standard notation for those areas that could be machine independent is considerably weakened by the argument, "If the language is going to be different anyway, why not make it lots different?"

Most problem- or procedure-oriented languages are excellent programming languages. Much better in many respects, in fact, than the assembly languages they've replaced. But excellent as they each are, not one of them is excellent enough to replace any of the others in the affections of its adherents. Neither are they excellent enough to greatly inhibit the development of new languages or the refurbishing of old, worn-out ones. And this, of course, is the main reason for the existence of so many different languages. All of them are inadequate in one way or another, and thus breed others by their very inadequacies.

do we need them all?

Many people have complained that the computing industry is too preoccupied with its tools, and that it should forget about new tools and get to work applying those it has. This would be a worthy sentiment except that the tasks facing the industry have outgrown the capabilities of the available tools, so that new and better ones are urgently needed. Thus, developing a new programming language isn't bad in itself but, when you consider the wild variety of notations available for expressing even a simple task, it is apparent that developing *six* new languages is. The computing industry doesn't need six different but equivalent and equally good ways of expressing a procedure any more than a machine-language programmer needs six different mnemonics for expressing the operation: load accumulator.

Many of the available problem- or procedure-oriented programming languages are very similar in scope, or at least have large areas of overlapping scope. This, of course, is part of the case for language standardization, and to convince yourself of the need for such standardization, you need only code the same short routine in half-a-dozen different languages, as below, and observe the unnecessary and occasionally mystifying notational differences that arise.

ALGOL

```
integer array NUMBER[0:99];
integer I, J, TEMP;
comment A routine that sorts a list of 100 unsigned
integer numbers into numeric order, using the
shuttle exchange method;
begin SORT:
for I := 0 step 1 until 98 do
    begin
    if NUMBER[I] > NUMBER[I+1] then
         begin
         TEMP := NUMBER[I];
         NUMBER[I] := NUMBER[I+1];
         NUMBER[I+1] := TEMP;
         J := I+1;
         for J := J—1 while
         J > 0 ∧ NUMBER[J] < NUMBER[J—1] then
              begin
              TEMP := NUMBER[J];
              NUMBER[J] := NUMBER[J—1];
              NUMBER[J—1] := TEMP;
end  end  end  end
```

MAD

```
              INTEGER NUMBER, I, J, TEMP
              DIMENSION NUMBER (99)
          R   A ROUTINE THAT SORTS A LIST OF 100
          R   UNSIGNED INTEGER NUMBERS INTO NUM-
          R   ERIC ORDER, USING THE SHUTTLE EX-
          R   CHANGE METHOD.
SORT          THROUGH XX FOR I = 0, 1, I .G. 98
              WHENEVER NUMBER(I) .LE. NUMBER
          1   (I+1), TRANSFER TO XX
              TEMP = NUMBER(I)
              NUMBER(I) = NUMBER(I+1)
              NUMBER(I+1) = TEMP
              THROUGH YY FOR J = I,—1, J .E. 0
          1   .OR. NUMBER(J) .GE. NUMBER(J—1)
              TEMP = NUMBER(J)
              NUMBER(J) = NUMBER(J—1)
              NUMBER(J—1) = TEMP
YY            CONTINUE
XX            CONTINUE
```

JOVIAL

```
ARRAY NUMBER 100 A 15 U $
BEGIN SORT.
"A ROUTINE THAT SORTS A LIST OF 100 UNSIGNED
INTEGER NUMBERS INTO NUMERIC ORDER, USING THE
SHUTTLE EXCHANGE METHOD."
FOR I = 0,1,98 $
    BEGIN
    IF NUMBER($I$) GR NUMBER ($I+1$) $
        BEGIN
        NUMBER($I$) == NUMBER($I+1$) $
        FOR J = I,—1 $
            BEGIN
            IF J EQ 0 OR NUMBER($J$) GQ
            NUMBER($J—1$) $
                TEST I $
            NUMBER($J$) == NUMBER($J—1$) $
END   END   END   END
```

FORTRAN

```
      DIMENSION NUMBER(100)
C     SORT, A ROUTINE THAT SORTS A LIST OF 100
C     UNSIGNED INTEGER NUMBERS INTO NUMERIC
C     ORDER, USING THE SHUTTLE EXCHANGE METHOD.
      DO   10   I = 1,99
      IF (NUMBER(I) — NUMBER(I+1))   10,10,20
   20 K = NUMBER(I)
      NUMBER(I) = NUMBER(I+1)
      NUMBER(I+1) = K
      J = I
   24 IF (J — 1)   10,10,25
   25 IF (NUMBER(J) — NUMBER(J—1))   10,10,26
   26 K = NUMBER(J)
      NUMBER(J) = NUMBER(J—1)
      NUMBER(J—1) = K
      J = J —1
      GO TO 24
   10 CONTINUATION
```

COBOL

```
001000 WORKING—STORAGE SECTION.
001100 02   NUMBER; SIZE IS 5 DIGITS; CLASS IS
001200      NUMERIC; OCCURS 100 TIMES.
001300 77   TEMP; SIZE IS 5 DIGITS; CLASS IS
001400      NUMERIC.
001500 77   I; SIZE IS 2 DIGITS; USAGE IS
001600      COMPUTATIONAL.
001700 77   J; SIZE IS 3 DIGITS; USAGE IS
001800      COMPUTATIONAL.
001900 77   K; SIZE IS 2 DIGITS; SIGNED; USAGE IS
002000      COMPUTATIONAL.
002100 PROCEDURE DIVISION.
002200 SORT SECTION. GO TO SORTING LOOP.
002300      NOTE   A ROUTINE THAT SORTS A LIST OF
002400      100 UNSIGNED INTEGER NUMBERS INTO
002500      NUMERIC ORDER, USING THE SHUTTLE
002600      EXCHANGE METHOD.
002700 EXCHANGES.
002800      COMPUTE   K = K + 1;
002900      IF NUMBER(I) IS GREATER THAN NUMBER
003000      (K) THEN MOVE NUMBER(I) TO TEMP;
003100      MOVE NUMBER(K) TO NUMBER(I);
003200      MOVE TEMP TO NUMBER(K);
003300      MOVE I TO J;
003400      PERFORM SUBSEQUENT-EXCHANGES.
003500 SUBSEQUENT—EXCHANGES.
003600      COMPUTE K = J—1;
003700      IF J IS GREATER THAN 1 AND NUMBER(J)
003800      IS LESS THAN NUMBER(K) THEN
003900      MOVE NUMBER(J) TO TEMP;
004000      MOVE NUMBER(K) TO NUMBER(J);
004100      MOVE TEMP TO NUMBER(K);
004200      MOVE K TO J;
004300      GO TO SUBSEQUENT — EXCHANGES.
004400 SORTING-LOOP.
004500      PERFORM EXCHANGES VARYING
004600      I FROM 1 BY 1
004700      UNTIL I IS GREATER THAN 99.
```

NELIAC

```
TEMP, NUMBER (100);
SORT:
(COMMENT: A ROUTINE THAT SORTS A LIST OF 100 UN-
SIGNED INTEGER NUMBERS INTO NUMERIC ORDER,
USING THE SHUTTLE EXCHANGE METHOD.)
FOR I = 0(1)98 DO
    {IF NUMBER [I] > NUMBER [I + 1]:
        {NUMBER [I] → TEMP,
        NUMBER [I + 1] → NUMBER [I],
        TEMP → NUMBER [I + 1],
        I → J,
XX:     IF J > 0 AND NUMBER [J] < NUMBER [J—1]:
            {NUMBER [J] → TEMP,
            NUMBER [J—1] → NUMBER [J],
            TEMP → NUMBER [J—1],
            J—1 → J,
            GO TO XX. }; }; }
```

is one language enough?

If we don't need all the programming languages we have, how many do we need?

A feeling is growing in the computing industry that perhaps a single, general-purpose, procedure-oriented programming language could be devised and adapted to suit everybody's needs. This is technically feasible, although there are many arguments (and arguers) against it.

One such argument is that no single language could satisfy those who want mathematical brevity and those who want English-like verbosity. This disparity is more apparent than real, however, for it is not impossible to combine readability with brevity, and have mathematical notation too.

A more serious argument is that a powerful, universal programming language could not be made completely machine independent. These is no doubt, however, that the basic information processing procedures, data and processing rules both, can be described in machine independent terms — even though machine characteristics may heavily influence the relative efficiency of programs compiled from such descriptions. This is true even of current, less powerful and less universal languages. COBOL, however, has incorporated an acceptable, partial solution to this problem in separating the machine dependent and independent portions of the program, and perhaps even greater stratification would be desirable. The ultimate solution, though, lies in improved compilation techniques, and in machine languages oriented toward these techniques.

Another, related argument is that a powerful, universal programming language might not be compilable on all computers that would be using it. This is true enough, but one or two nested subsets of such a language could be designated for this purpose, without sacrificing upward compatibility, and probably with little sacrifice in applicability. Character set incompatibility could also be handled on a language-subset basis. By designing the language around a maximum character set and providing an English-word synonym for each special symbol, a language implementer could include all the synonyms, and all the special symbols his hardware could handle, thus minimizing the problem. Programs for many computers would then be written mainly with English, and if a few two- and three-letter "noise" words were also available, readability could be attainable, as a by-product.

Still another argument is that no single language could have a broad enough range of expression and that many special purpose languages are necessary to express the many different types of problems that people use computers to solve. But though there've been murmurings from here and there, we're a long way from a general ability to describe a problem to a computer and get back a solution. Meanwhile, we are reduced to describing information processing procedures (as we have been doing all along) and, basically, these differ very little from application to application — even when disguised with a gloss of technical jargon.

The range of expression of a universal programming language need therefore not be excessive, just so long as it includes all basic information processing procedures (each of which consists of an operation and the data it involves.) And since the number of basic operations (those that can't be *conveniently* expressed as combinations of other operations) and the number of data types and structures that need be considered are not unlimited, the basic information processing procedures *can* be enumerated. After all, there's only half-a-dozen or so different data types, as many different data structures, and perhaps two or three dozen different operations that such a language must deal with. And given a programming language with a more or less complete range of expression that also allows the user to modify its structure (e.g., with free-format, syntax-sensitive, conditional macro definitions,) problem orientation could easily be imposed on top of the basic language structure without violating the "common language" concept — any more than does the current ability to define and name subroutines.

can we standardize?

The need for language standardization is widely apparent. A mechanism for language standardization exists in the ASA X3 committee. A single, general purpose, standard programming language is technically feasible. What, then are the prospects for effective language standardization in the near future? My guess is that prospects are pretty poor!

For one thing, both ALGOL and COBOL, or updated versions of them, will probably be around for some time. They seem likely to be accepted as twin standards by the ASA, which will probably lack the temerity to purpose a new standard to replace them. ALGOL and COBOL are each inadequate as *the* standard because neither of them have a complete range of expression — even taken together. And even if they were complete, taken together, they would still be inadequate as standards because problems would exist requiring language features that each lacked and for which neither would be suitable. Thus, a nonstandard language would be required. (The critical point is, of course, that applications for which neither ALGOL nor COBOL are particularly well suited constitute a minor but very significant and growing part of the total information processing spectrum. Examples are: software program systems, and real-time, management or command control systems.)

What seems most likely is that extensions will be made to both ALGOL and COBOL to broaden their range of expression, and that they will continue as standards for scientific and business computing. In the meantime, another standard programming language, suitable for both software systems and for real-time management or command control systems, might be developed, incorporating most of the capabilities of both ALGOL and COBOL and additional capabilities as well. (Such a language would be the most likely prototype for a general standard.) The computing industry would then have a triple standard which, while not the ideal situation, would be far better than the current one. However, the inertia to be overcome in scuttling all the other, surplus programming languages could well delay the complete acceptance of these standards until they, too, were outmoded.

are there too many languages?

The preceding sections have asked and, to some extent, answered a series of questions concerning programming languages and the standardization problem.

Are there too many languages? Yes, the present language plague is widely recognized as being unnecessary, unwholesome, and much too costly.

Why so many languages? Besides the fact that everybody wants to get into the act, the main reason is that none of the presently available languages is adequate as a general purpose standard. Because of the inadequacy of available languages, new ones are designed and implemented — without, however, solving the overall problem of language standardization.

Do we need all these languages? No! Most currently available programming languages have similar ranges of expression and there is a broad, overlapping area common to all of them. Different ways of expressing the exact same concept are only needed in poetry, not in programming.

Is one language enough? Almost. It is technically feasible to develop a single, procedure-oriented programming language with a range of expression complete enough to handle, with reasonable ease, just about any production application imaginable. And a language with the capability for self-defined growth could handle most non-production applications as well.

Can we standardize? Not completely, and not in the foreseeable future. The best that can soon be expected is a triple standard: ALGOL, COBOL, and a language suitable for systems programming. And developments in hardware and programming techniques could make these standards less than optimum before they are fully accepted.

THE CDC 3600

large-scale modularity from 32-262 k

The Control Data 3600 is the latest in a line of advanced large-scale computers offered by Control Data Corporation. The basic 3600 Computer is large by any industry standards, yet its modular design provides options for adding functional modules tailored to satisfy specific computing and data processing requirements as they arise.

The Control Data 3600 has the following machine characteristics:

- 48-bit word length plus 3 bits for parity checking.
- Storage Module of 32,768 48-bit words—expansible in 32,768-word modules up to 262,144 48-bit words:
  1.5 microseconds—memory cycle time
  .7 microseconds—effective cycle time
- Communication Module with 4 bi-directional data channels—expansible up to 8 bi-directional data channels. (Up to eight control and/or peripheral devices can be attached to each bi-directional data channel.)
- Up to 3 additional Communication Modules may be added, with from 1 to 8 bi-directional data channels each.
- Execution times, including access:
  4 microseconds—Floating Point Add
  1-6 microseconds—Floating Point Multiply
  1-14 microseconds—Floating Point Divide
  2-26 microseconds—Double Precision Floating Point Multiply
- Code compatibile with the Control Data 1604 except for three 1604 I/O instructions.
- Byte-scan operation in which: 1) data of variable length within a word can be operated on by one operation or 2) high-speed scanning can be performed on computer storage in byte-size pieces.
- Special computing functions easily added to system via special channel in the Compute Module, e.g., trigonometric and exponential functions, etc.
- Double precision floating point commands—with mantissa of 84 bits plus sign.
- Results of all arithmetic operations normalized or unnormalized, rounded or unrounded . . . at programmer's option.
- Inter-register instructions.
- Two-way search instructions.
- Data transmission control performed by high-speed register located in Communication Module —permitting I/O activity to proceed independent and asychronous of main computer program.
- Universal bit-sensing instructions.
- Shifting time constant—regardless of number of positions shifted.
- Sophisticated interrupt capability.
- Auto-load buttons for card and magnetic tape equipment.
- Direct card reader entry into Arithmetic Register.
- Parity check on all I/O data transmission.
- Registers for memory lockout—under program control.
- Various special, high-speed circuits operating at 4 nanoseconds per stage.

Characteristic of the 3600 is a high degree of modularity. Smooth expansion of the basic system is affected by the addition of functional modules. These are designed so as to eliminate the necessity of installing specialized interconnecting black boxes.

The basic 3600 Computer consists of three functional modules: the high-speed 3604 Compute Module, the high-speed 3603 Storage Module, and the high-speed 3602 Communications Module. Also included with the basic computer are the 3601 Console (with its electric typewriter and display panel) and a 250 card-per-minute card reader. Figure 1 shows a diagram of the basic 3600 Computer.

3604 compute module

The 3604 Compute Module performs all the computing and logical operations. In addition, it contains the control for initiating I/O operations. Having direct access to the core storage module (s), the 3604 operates in the parallel binary mode in one of two programmable moduli: $2^{48}-1$ for single precision fixed point and $2^{84}-1$ for double-precision floating-point operations.

The 3604 instruction repertoire consists of both half-word and full-word instructions. A subset of half-word instructions is identical to the Control Data 1604 instruction repertoire, except for three I/O instructions in the 1604.

Several new categories of instructions have been included in the 3600 instruction repertoire, as follows:

- Commands which facilitate manipulating portions of a data word. For example, bytes of 48 bits or

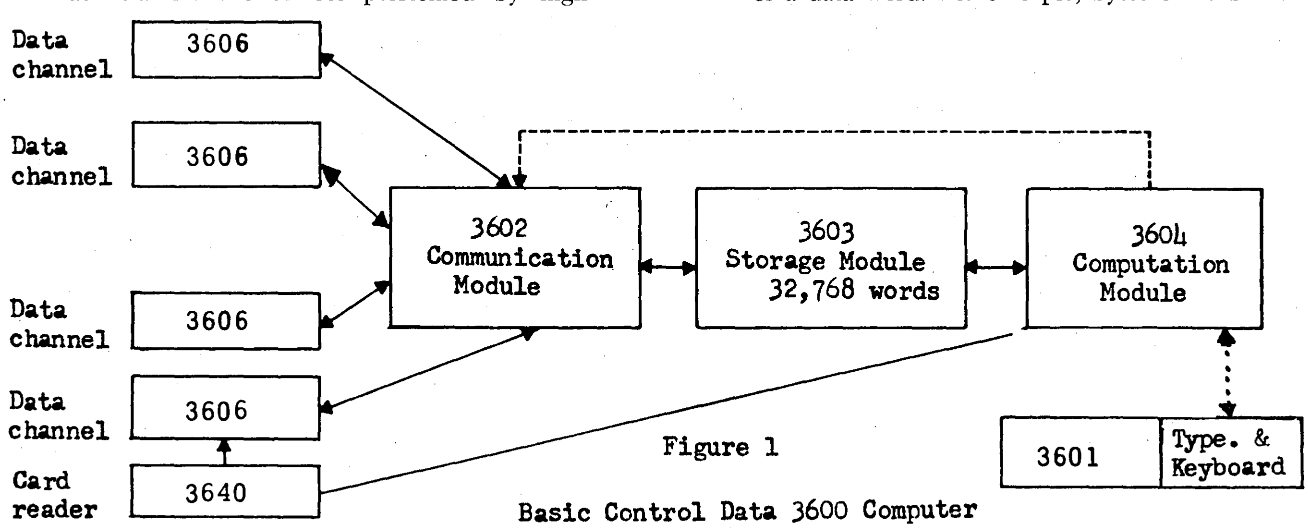


Figure 1

Basic Control Data 3600 Computer

less may be transmitted to any portion of a register or storage word in a single operation. Provision is made for indexing through bytes in a word (horizontally) and through a list of such words (vertically) in the same operation.

- Double-precision floating-point commands include add, subtract, multiply, divide, fetch, and store. A 10-bit plus sign exponent is used with an 84-bit plus sign fraction.
- Two-address transmissive and repeated transmissive instructions are included with provision for any size address increment to be used in the repeated operations—independent of the number of words in the list.
- A special instruction for list processing, as well as several new indexing operations.
- A universal bit-sensing instruction which permits any bit in any register to be tested and branched upon. In addition, the bit sensed may then be complemented, set, cleared, or left unchanged.
- A powerful, extremely fast interrupt facility is provided, as well as instructions for processing interrupts.
- Indexing instructions which may, under program option, be performed in either one's or two's complement arithmetic.
- Six sense switches are included on the console and can be program sensed. These are in addition to three selective jump and three selective stop switches.
- A 48-bit sense light register is included. Each position in the register may be set or cleared under program or manual control. Provision is made for sensing the status of each position and branching upon the condition or its complement.
- Two "bounds registers" of 18 bits each used for memory lockout. Information is not written into the region of the core storage specified by the addresses within the "bounds register."

The 3604 Compute Module employs special circuitry to speed up the basic arithmetic processes. Thus, the basic cycle time of the adder network is 250 nanoseconds. The shift time is a constant 250 nanoseconds regardless of the number of places shifted. These times do not include storage references. Some typical average execution times including all storage references are listed in the table below:

	Fixed Point	Single Precision Floating Point	Double Precision Floating Point
Multiply	1-6	1-6	2-26
Divide	1-14	1-14	2-26
Fetch/Store	1.5-2.2	1.5-2.2	3
Add/Sub	1.5-2.2	4	5

Table 1. Typical Average* Execution Times.

*Average time of multiply and divide instructions is the same as the maximum time; the lower figure of the range permits abortion of the sequence for zero values of one or both operands.

3603 storage module

The 3603 Storage Module provides high-speed, random-access magnetic core storage of 32,768 48-bit words. A storage word may be two 24-bit instructions, a single

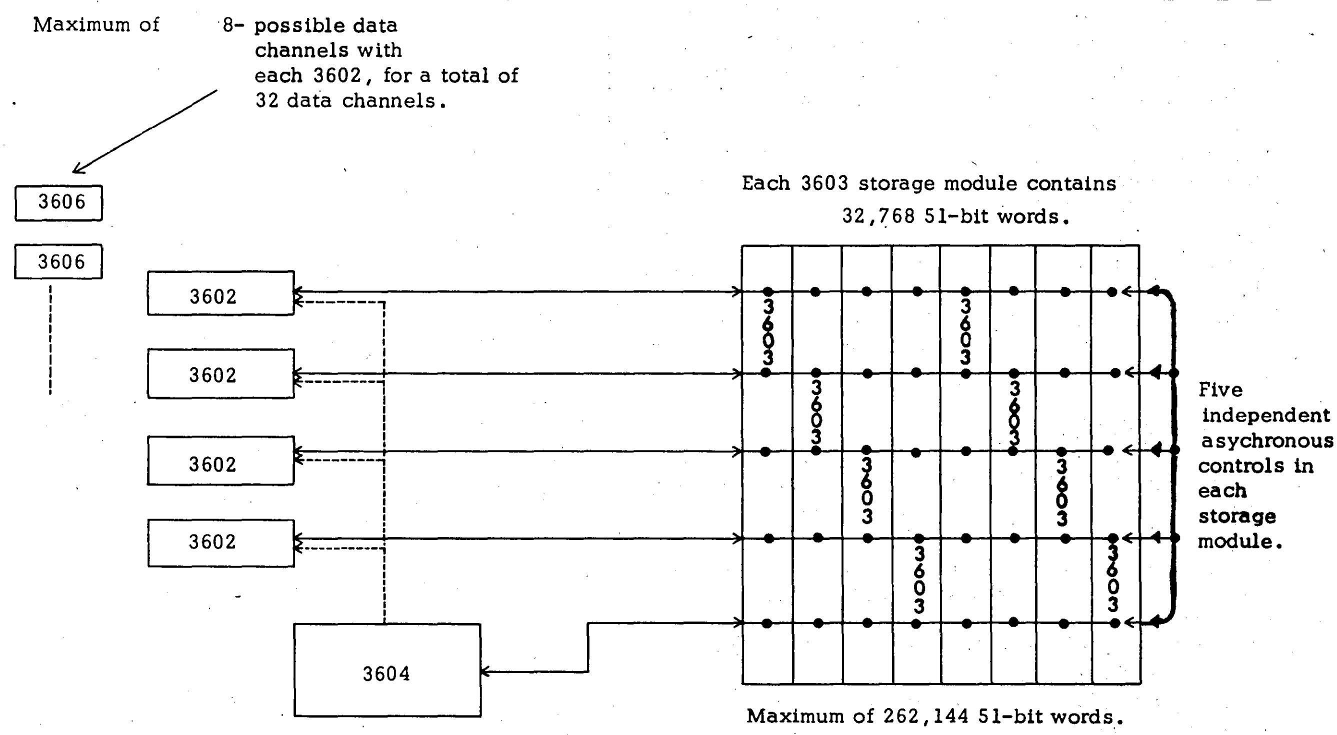


Figure 2.

A fully expanded 3600 Computer System.

48-bit instruction, a 48-bit data word, or half of a 96-bit data word. Three parity bits are generated for each storage word; thus, a storage word is 51 bits in length.

The parity bits are generated each time a word is read from or written into storage. One of the three parity bits is assigned to each of the two 15-bit addresses; the third parity bit is assigned to the remainder of the word.

The storage cycle time, i.e., time for a complete storage reference, is 1.5 microseconds. Since the storage cycles of the two independent 16,384-word storage sections may overlap one another in the execution of a program, the average effective cycle time for random accesses is approximately .7 microseconds.

3602 communications module

Input-output operations are initiated by the compute module and controlled by the 3602 Communications Module. The basic 3602 contains a storage access control section, an arithmetic and control section, and four bi-directional data channels. Included are provisions for attaching up to a total of 8 bi-direction I/O data channels to each 3602.

Input-output operations may occur independently asychronously with operations in the compute module. Input or output data is transmitted to or from storage directly, and *does not pass through the compute module.*

The arithmetic and control portion of the 3602 supervises all I/O functions once operating conditions have been initiated. The compute module directs the selection of a specific external equipment and the channel in which I/O activity is to take place, as follows: a 48-bit control word is read from storage and entered into a 48-bit control register. The control word specifies a starting address, i.e., the storage address from which the first output word will be read . . . or where the first input word will be stored —along with a 15-bit word count. Once these initial operating conditions have been generated, the channel control supervises all I/O activity.

Each data channel is bi-directional, i.e., it may be used for both input and output communication. Each 48-bit data word is transmitted in 12-bit bytes and is assembled/dissassembled in a 48-bit assembly/disassembly register. Assembly/disassembly time is less than one storage cycle, permitting the storage module to be used at its maximum rate and allowing full utilization of a parity bit for each 12-bit byte transmitted.

Upon completion of the assembly/disassembly of the 48-bit word, it is transmitted to the appropriate storage module via the access control section. The parity bits accompanying the output transmission are checked by the external equipment; parity bits accompanying input transmissions are checked by the 3602.

3600 expansibility

The basic 3600 Computer can be expanded to include up to eight 3603 Storage Modules, each with a capacity of 32,768 48-bit words. The fully expanded 3600 Computer is shown in Fig. 2.

If a 3600 employs more than one storage module, its compute module references each storage module in either one of two ways, or a combination thereof as follows:

1) One type of instruction where the full 18-bit address is specified and/or
2) By means of two 3-bit bank address registers:
   a) an operand bank register
   b) a program address bank register

These two registers are *directly addressable* by the main computer program and can be changed at will.

All 24-bit instructions implicitly refer to these two registers; all other instructions explicitly contain an operand bank address together with one bit . . . indicating whether the implicit operand register address or the explicit instruction operand address is to be used in the instruction.

The stored program may thus be located in one storage module, while the operands, i.e., data, constants, etc., may be located in a different storage module . . . thus, significantly increasing the speed of the 3600 Computer.

Any of the four possible 3602 Communications Modules can *directly reference* any of the eight possible storage modules . . . once I/O operations have been initiated by the 3604 Compute Module. For example, the 3604 Compute Module may use storage module #3 for operands and storage module #2 for stored programs. At the same time, communication module #1 may be transmitting data to storage module #5. Concurrently and asychronously, communication module #2 may be transmitting data to storage module #4. While communication module #3 is transmitting data to storage module #6, communications module #4 is transmitting data to storage module #7.

Thus, six storage modules may be operating simultaneously at peak rates . . . completely asychronous.

multiple computer system

Up to five 3600 Computers can be linked together in a common system, as shown in Figure 3. This may be accomplished by employing one of two basic operating modes, or a combination of each.

In one mode, the compute module of each 3600 Computer can address eight storage modules. In a common system, the compute modules of each 3600 would address a fixed number of storage modules which the remaining compute modules could not address. In other words, the eight addressable storage modules are considered an integral part of each 3600 Computer in the common system.

However, each compute module in the common system can address a common pool of storage modules. The total number of storage modules in this common pool and the number of modules connected to a given 3600 Computer, cannot exceed eight. Five such 3600 Computers can address the common pool of storage modules independently and asychronously.

In the second operating mode, each 3602 Communications Module may contain up to eight 48-bit inter-computer, bi-directional data channels. Each of these eight channels has provision for communication directly with identical channels in other 3600 Computers in the common system.

These 48-bit data channels exchange control and computer-identity information. They also permit one 3600 Computer to interrupt any other 3600 Computer in the common system . . . under program option.

Should they occur, machine malfunctions, e.g., a parity error, are instantly transmitted via 48-bit channels to any other 3600 Computer in the common system.

3600 circuitry

The computer circuits have been under development at Control Data for over two years, and are the result of an extensive development effort expended toward producing the 3600.

The basic building block is a bi-level amplifier-inverter which operates at an equivalent phase rate of 16 megacycles. Several levels of logic can be performed in one phase time of 62.5 nanoseconds. In addition, various special high-speed circuits employing tunnel diodes are used (4 nanoseconds per stage).

Printed-circuit cards similar to those found in the 1604 are used in the 3600. The dimensions have been changed slightly, and the component packing density has been increased. The voltage levels are −5.5 volts and −1.5 volts. All cards are pluggable and have eyelet test points for attaching oscilloscopes.

3600 software

In parallel with the development of the 3600, Control Data is developing a complete and integrated software system to be delivered with the first computer. This software system will be oriented around a Master Control System.

The Master Control System (MCS) will act as a common communication link among all programming systems and I/O devices, interrupt, and memory allocation functions. Thus, the MCS will allow programming systems to be independent of particular machine configurations . . . as well as of types and numbers of I/O media. In addition, the MCS will provide:

- A library common to all systems such as FORTRAN and COBOL which will operate within the MCS.
- An open-ended ability to incorporate new compilers and operating systems as they are developed.
- A linking loader that will permit joining together in one program several sub-programs that may have been separately and independently compiled or assembled.
- A system easy to modify and adapt when necessary to the needs peculiar to a given installation.

Some of the important programming systems operating under control of the MCS will be:

- *MONITER SYSTEM*—a complete operations supervisory system for automatic control of all jobs. It will allow stacking of jobs with arbitrary intermixing of different job types, such as assembly, compilation, and execution.
- *COMPASS*—a comprehensive assembly system with versatile language features for representing the extensive instruction repertoire in a simple symbolic notation, employing advanced assembly techniques.
- *FORTRAN*—An algebraic compiler with extensions to, and generalizations of, the basic FORTRAN language using advanced compiler techniques for producing optimum object programs.
- *COBOL*—a complete compiling system for business-oriented applications.
- *1604 COMPATIBILITY PACKAGE*—a software package which will execute interpretively all trapped I/O and interrupt instructions of a 1604 program running in the 1604 compatibility mode.

optional peripheral items

A variety of optional on/off-line peripheral items may be used with the 3600 Computer. These include 12-, 24-, and 48-bit bi-directional data channels; a 48-bit intercomputer data channel; special function generators; magnetic tape handlers and tape synchronizers; medium- and high-speed card readers, card punches; low- and high-speed line printers; paper tape I/O equipment; keyboard entry devices and typewriters; and disc files. ■

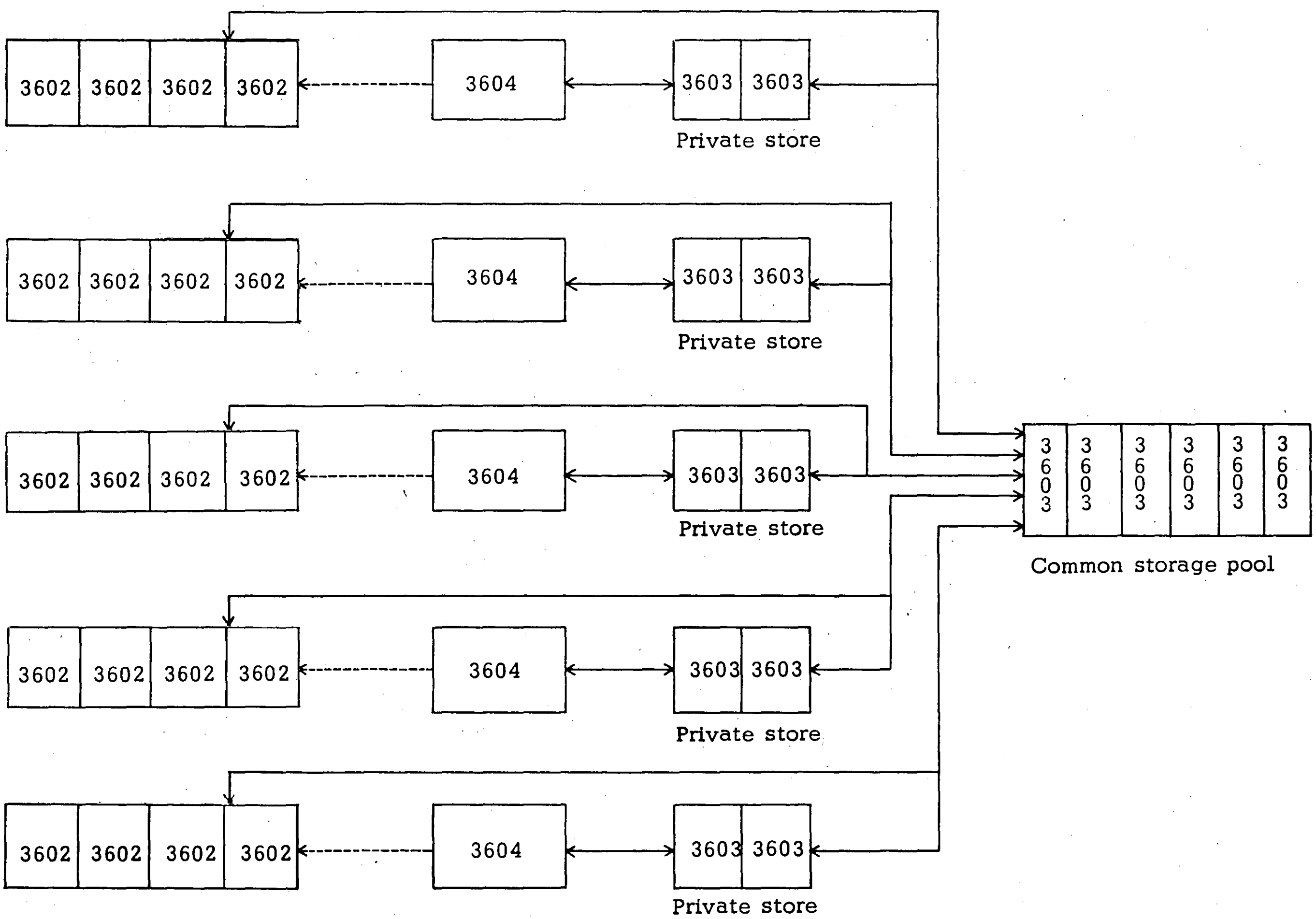
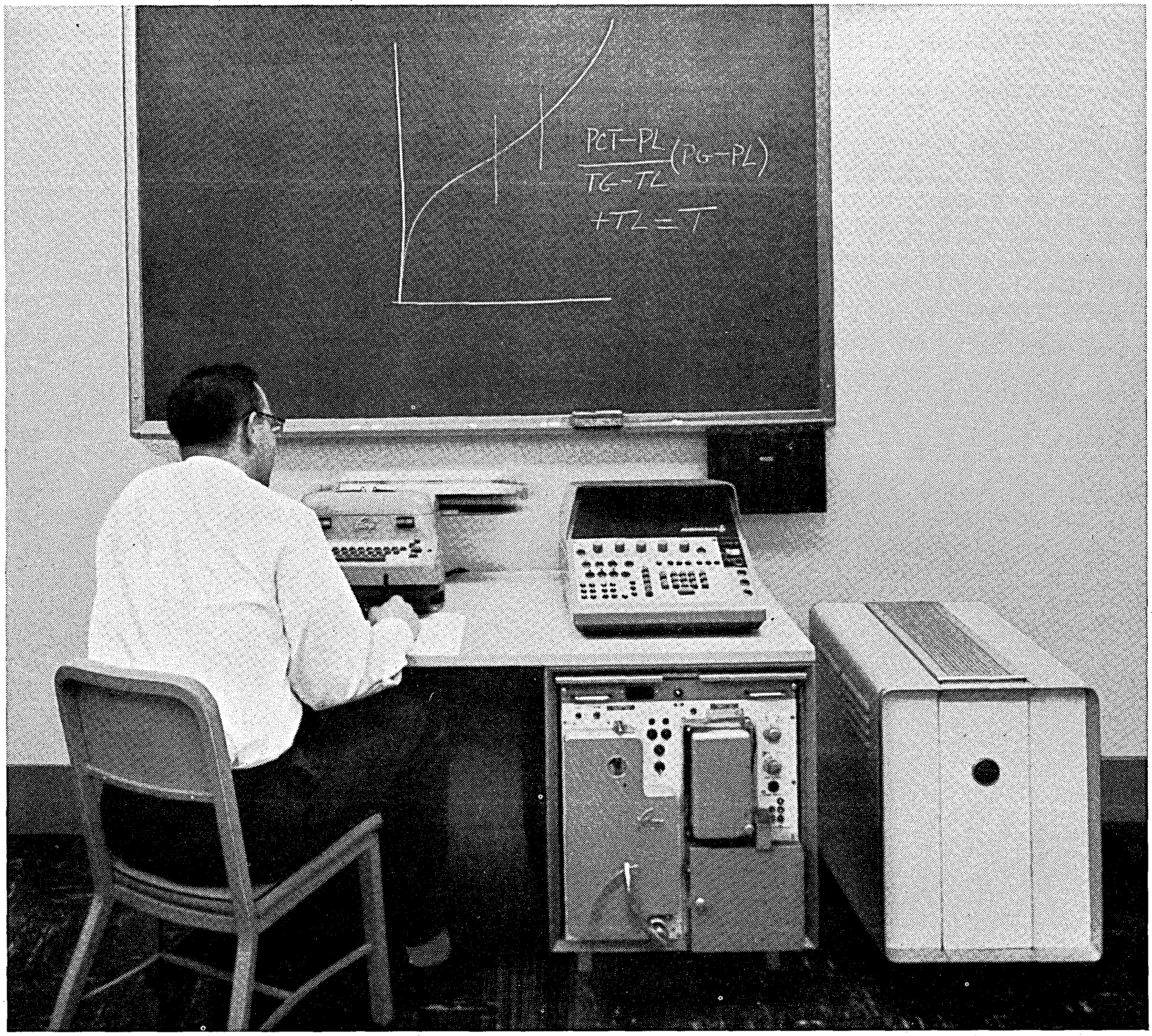


Figure 3

A multiple computer complex



Standard Oil Company of California uses Recomp II in overall operations planning for its Richmond Refinery.

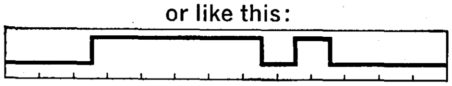
This computer speaks English.

Some computers act as though they're trying to hide the facts. Not Recomp.®

Recomp II has a built-in direct numerical display of any memory word. When it wants to show you a number like 1000., it shows just that: 1000. And it can carry it out to 12 digits. To show you 1000., other computers may display something like this:

●●○○○○○●○●●●

or like this:



Recomp II automatically checks every program, bit by bit, against the original tape. And built-in echo checking of typewriter or punch output assures accuracy.

Recomp II abounds in other built-ins (floating-point, square root command, and conversion from decimal to binary, to name a few). It has two high speed memory loops (each containing 16 instructions). It has a large word length (40 bits). And a large memory (8160 instructions).

Recomp II is ideal for medium-scale needs; Recomp III is perfect for small-scale needs. You can lease a Recomp III for $1,495 (complete with no accessories required), or a Recomp II (with a complete line of peripheral equipment) for up to $4,500 a month.

There are many small and medium scale computers on the market today. Only a few are really outstanding. Recomp is one of them.* For the full Recomp story, write:

AUTONETICS Industrial Products
Department 65, 3400 E. 70th Street, Long Beach, California.
Autonetics is a Division of North American Aviation.

Recomp

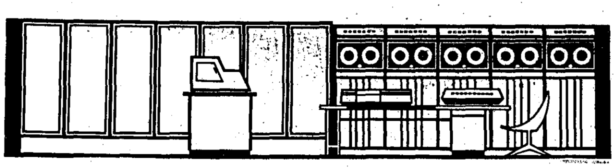
*No computer feasibility study is complete without Recomp.

CIRCLE 19 ON READER CARD

Honeywell's newest magnetic tape units may be just your speed

Now there are four models of magnetic tape systems to choose from in Honeywell's line-up of high-speed computers. The newest addition is called the Super Density system. It might also be called Super Speed, with its transfer rate of 186,000 decimal digits per second. Other models in the line include the High Density system which has a transfer rate of 133,000 digits per second, the Standard system at 96,000 digits per second, and the Economy system at 48,000. With a speed for every need, you can select the combination of computer and magnetic tape system that will assure maximum efficiency and economy for the job you have at hand.

With the compatibility of this line of magnetic tape systems, you also have added flexibility when it comes time to expand. You can move up to higher speed units without need for reprogramming or other costly changeover operations. Tapes written at one speed can be read at other speeds on other units.



Super Density gives higher speed, takes less tape

The new Super Density magnetic tape units achieve their high data transfer rate by packing information more compactly on tape. The 777 bits-per-channel-inch density of the Super Density unit compares, for example, to the 397 bits-per-inch of the Standard unit. In addition to higher speeds, this also means that more data is recorded on a reel of tape which, in turn, means fewer reels, less tape changing.

Table talk

	Economy Tape Unit	Standard Tape Unit	High Density Tape Unit	Super Density Tape Unit
DENSITY OF DATA ON TAPE				
Decimal digits per inch of tape	794	794	1,111	1,554
Pulses (bits) per channel inch	397	397	555	777
TRANSFER RATES				
Decimal digits per second	48,000	96,000	133,000	186,000
Alphanumeric characters per second	32,000	64,000	89,000	124,000
MEAN TRANSFER RATE				
Characters per second	40,000	80,000	111,000	155,000
SYSTEM APPLICABILITY	H400	H400 H800	H400 H800 H1800	H800 H1800

Automatic error correction across the board

All Honeywell magnetic tape units feature Orthotronic Control, a unique method of automatically detecting and correcting errors. This technique, developed and perfected by Honeywell, minimizes the cost of maintaining accuracy and saves time otherwise required by human intervention or rerunning of programs.

Transports that treat their tape tenderly

All Honeywell tape units utilize vacuum capstans to produce and control the motion of tape past the read/write head. Vacuum is used to grip the tape to one of two counter-rotating capstans, depending on the direction of motion called for. Air pressure serves as a low-friction bearing to float the tape over the surface of the opposite capstan. The course of tape travel from reel to reel is designed in such a way that the oxide surface of the tape is untouched by any portion of the unit except the read/write head. Also, there are no pinch rollers to imbed dirt or dust into the tape or cause excessive wear. No other tape units treat their tape so gently or transport it so precisely.

Even a novice can change Honeywell tapes in seconds

Honeywell tape units and tape reels are designed for fast, safe changing. Reels are locked in place and the tape leader is threaded with the aid of vacuum. There are no openings in the reel flanges to catch fingers or foul the tape. Tapes can be changed in less than 25 seconds with a minimum of practice.

Write for more information

If you would like more information, write to Honeywell EDP Division, Wellesley Hills 81, Mass. In Canada, Honeywell Controls Limited, Vanderhoof Avenue, Toronto 17, Ontario.

Honeywell

H HONEYWELL *Electronic Data Processing*

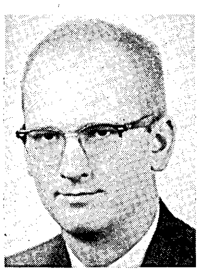
CIRCLE 20 ON READER CARD

At *Datamation's* request, editorial adviser Dan McCracken interrupted a vacation in Italy last March to attend most of a meeting in Rome at the International Computation Centre. Here is his report, consisting of important news about ALGOL, some impressions of European computer conferences and a brief sketch of the Computation Centre.

a report on the Rome symposium on symbolic languages

A NEW HOME FOR ALGOL

by DANIEL D. McCRACKEN, Ossining, N.Y.



The beautiful new EUR Zone in Rome was the setting March 26-31 for a Symposium on Symbolic Languages in Data Processing. The meeting was sponsored by the International Computation Centre, an important organization that is not as well known in the United States as it deserves to be.

This will not be a complete technical report on the conference; too much was presented, in too many different areas of research, to permit a casual summary by a person not closely familiar with the fields. The detailed technical content may be examined in the Proceedings when they are published in a few months. Here we shall have to be content with some essentially non-technical highlights.

ALGOL has a home

Probably the most important news to come out of the conference has to do with ALGOL, although not all of the action took place at the meeting.

At a meeting in Geneva the week before the Symposium, the International Federation of Information Processing Societies established a Working Group on ALGOL as part of Technical Committee #2, Programming Languages. The chairman of the ALGOL Working Group is Dr. W. L. van der Poel of the Netherlands, who has long been active in the ALGOL effort and who has implemented ALGOL on the ZEBRA computer.

This is indeed important news to anyone interested in the acceptance of ALGOL, since one of the main obstacles to its adoption has been its homelessness. Until now, no one could really speak for ALGOL with complete authority except the 13 authors of the original Report and they were not in the language-maintenance business. Now, there will be an official body to which questions, suggestions, and complaints can be directed, with assurance that a response will be forthcoming and that it will be official policy.

The Working Group will have some 30 members, who have not yet been chosen. All of the 13 authors of the ALGOL report will be invited to become members, and indications are that most of them will accept. (This last is quite significant, since reluctance by the authors to go along with IFIPS sponsorship of ALGOL could easily undermine the Working Group.)

Most of the 13 authors were at the Symposium. They held a two-day meeting the following week, to try to clean up some minor errors and some ambiguities in the Report. A summary of their recommendations for changes in the Report will be published in the ALGOL Bulletin and presumably in the ACM *Communications*, these being in the nature of suggestions to the Working Group. From now on, all such matters will be the responsibility of the Working Group.

There is no intention of making substantial modifications or extensions to ALGOL at the present time, and there definitely will not be an ALGOL 62. Modifications and extensions are of course very much in the wind and will be a major concern of the Working Group, but implementors should have no problems with official changes this year. In fact, the problems of implementors in making changes will probably not be too great even when the Report is eventually extended, since the general attitude seems to be that extensions should not involve changes in the present Report. Thus, any processors now under development would not be made obsolete, but would merely need to be extended if desired.

It was quite in keeping with the tenor of the Symposium that big news on ALGOL should emerge from it. There were nearly a dozen papers more or less directly on the subject, ranging from basic ideas and generalizations to the construction of compilers. Two panel discussions were rather specifically about ALGOL, and most of the others drifted toward it.

In one of the panel discussions that was to have been on general aspects of compilers but turned into an ALGOL free-for-all, there was an exchange that pretty well sums up the attitudes toward this subject about which no one seems to be neutral. G. Seegmuller of Germany stood up and made an impassioned speech advocating a *practical* approach to computing. Condensed to essentials, the argument ran: "We've got a lot of customers who need *answers*, not speculation. We would be happy to use ALGOL, since it seems to have many good features, but we can't do much with a compiler that is loaded down with these miserable recursive procedures and which produces horribly inefficient object programs. We want to *work* with ALGOL, not *play* with it." There was loud, sustained applause.

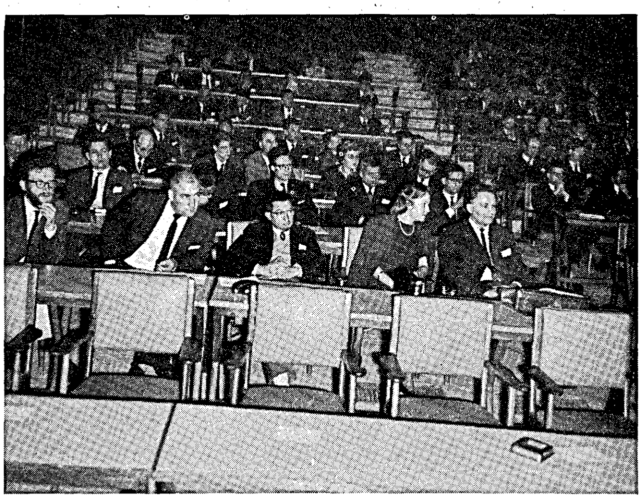
Four viewpoints could be identified in the ensuing discussion. Some one said, "But I've got a compiler that isn't slowed down by recursiveness, and the object programs are pretty good. You've just got to learn how to write compilers." Somebody else said, "Maybe recursiveness does cost time in some cases, but it costs *not* to use it when it is the best solution. You've just got to learn how to use this new tool we've provided." Another said, "Even if

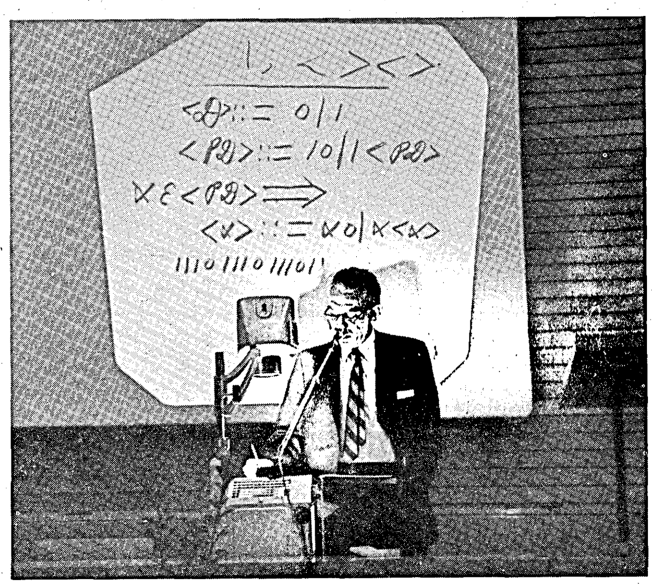
INTERNATIONAL COMPUTATION CENTRE

Centre International de Calcul

Palazzo dei Congressi EUR
Rome, 26 - 31 March, 1962

SCENES FROM THE SYMPOSIUM ON SYMBOLIC LANGUAGES





recursiveness is difficult and often not useful, the idea of ALGOL for standardization is so important that some compilers should be constructed without recursiveness, if necessary. You've got to provide us with more than one version of ALGOL." Finally, some one said, "ALGOL is such a large advance in the computing art that we never should have expected immediate acceptance. We've got a lot of things to learn before ALGOL is widely accepted, as it surely will be in time, and one of these is patience."

Reflection shows that there are large elements of truth in both the impassioned speech and in the responses. To the extent that wide acceptance is the goal, the advocates clearly need to respond to some of the complaints. The detractors, on the other hand, need to realize that a new tool cannot always be used in the same ways as old ones. A jet liner should not be gold plated, but neither can it be flown or maintained like a DC-3.

reflections on computer meetings

Without intending to suggest that all American conferences are uniformly bad, or to infer from a sample of one that all European meetings are great, it may nevertheless be interesting to note some features of this symposium that are not always typical of what we have here.

Of the 300 or so people in attendance, at least 80% would appear to have been professional workers in the field. Conspicuous by their absence, with a few exceptions, were salesmen, out-of-contact managers, promoters of assorted hues, and people being rewarded with a trip instead of a raise. The bulk of the attendees were there to give papers, participate intelligently in discussions, and learn. The general atmosphere was that of work, not holiday.

This could be seen in several ways. One striking example was attendance at the sessions. In the first place, the hall was generally filled when the first paper started very shortly after the announced hour of nine. Papers and discussions ran from then until a little after noon, and very few people wandered in and out. Although there was a coffee break in the afternoon, there was none in the morning. I'm not advocating the abolition of coffee breaks; the point is that most of the 300 people thought enough of the speakers and of their own responsibilities to sit in one place for three straight hours.

After the traditional long lunch hour, sessions and panel discussions ran again from three until seven. Most of the audience was still there at seven.

Virtually all of the papers represented many months of hard work, and largely discussed accomplishment. Not heard, in the main: pitches from manufacturers, airy speculation, broad rambling generalizations with no content, vague discourses on why the speaker chose to adapt some one else's work to his own small goals, and papers designed primarily to get the speaker a trip to Rome.

The very fact that most of the speakers did have so much to say raised once again the old problem of what to do with half an hour. Quite a number of the papers represented research that could easily fill a 40 hour seminar; what can you hope to get across in 30 minutes? Too many of the speakers apparently decided in frustration simply to say what they would have said in the first 30 minutes of the seminar: a brief introduction, followed by the beginning of the detailed presentation of the technical content—and stop when the bell rings. Judging from the admittedly small sample of this one symposium, it would appear that the Americans, with some exceptions, had thought more about how to present their material. They tended to start with a general discussion to set the stage, continue with a sketch of the important results and perhaps some of the details to indicate the flavor of the subject, and close with a summary of the highlights.

This was an important meeting. The speakers and the International Computation Centre deserve applause, and it might be hoped that some of the best features could be incorporated into meetings in the United States.

the international computation centre

The ICC grew out of a UNESCO Convention set up in 1951. Ratification by the required number of countries was slow in coming, so in late 1957 a Provisional International Computation Centre was established. The PICC operated for about four years, until the formal establishment of the ICC in January of this year. The present organization will carry on the work started by the provisional group, as well as moving into high gear on activities that were not feasible until formal status had been achieved.

The ICC has headquarters in space supplied by the Italian government in the Palazzo degli Uffici, in the EUR Zone, Rome. It is supported by contributions from the member governments; the budget for 1962 is approximately $200,000. There are at present ten countries participating: France, Belgium, Italy, Mexico, Japan, Egypt, Libya, Ceylon, Argentina, and Germany. One or two others are expected to join shortly. It may be noted that the United States is not included in the list. There is apparently some interest in this country in joining, but so far nothing has come of it. Joining would require formal action by some branch of the Federal Government, such as perhaps the National Science Foundation.

The Centre presently has a quite small staff and no hardware, but there are plans for considerable expansion in the next year or two. The Director is Professor Stig Comet who was previously director of the Swedish Board of Computing Machines. He is assisted by Mr. Jean Besse; publications are handled by Miss Pamela Campbell; secretariat functions are under the direction of Miss A. Seggiaro. The hope is to build toward a staff of 50 to 100 people fairly soon, to carry out the three main functions of the Centre.

The first function is that of research into matters related to computing: numerical analysis, applications, etc. There will eventually be full-time professional staff members working in various areas.

The second function is that of education, which is carried out in several ways. The present meeting is one such way, and there have been several previous meetings, primarily devoted to various aspects of numerical mathematics. Another way is through fellowships, of which some have been granted already. Another is through promoting exchanges of personnel.

The education function also includes a number of publications. There is the Bulletin, published quarterly, which ranges from semi-technical progress reports and equipment surveys to news notices, book reviews, and bibliographies. Most articles are in English; some are in French; a few important items printed are in both languages. The Bulletin is currently distributed free to some 2000 people; starting next year there will be a modest charge. The Centre also publishes a Repertory of Computation Laboratories, which currently lists the important facts about some 400 computing centers around the world, and is updated in the Bulletin. Finally, there are the proceedings of the various conferences.

The third function of the ICC is consultation and computing services. In carrying out this responsibility there will be a computer by the end of this year, with the possibility of a second next year. A decision was to have been made before publication of this report as to which computer to obtain.

All in all, the International Computation Centre impresses one as an important element of the computing society, with an influence that will surely grow. ■

NMAA'S '62 INTERNATIONAL DP CONFERENCE & EXHIBIT

new york's Statler to host 4,000 delegates june 19-22

The Statler Hilton Hotel, New York City, will be the scene of the 1962 International Data Processing Conference and Business Exposition, to be held June 19-22. "Key to Efficiency" has been selected as the Conference's theme by the sponsoring group, the National Machine Accountants Association.

Registration for the conference, which is expected to attract over 4,000 persons, will be in the Grand Ballroom Rotunda of the Statler Hilton on Monday, June 18, from noon to 10 p.m., and 8 a.m. to 10 p.m. on June 19 and 20.

The Business Exposition, which will show the products of more than 80 manufacturers, will be open during all four days of the conference, during these hours: 1 p.m. to 8 p.m. on June 19; 9 a.m. to 6 p.m., June 20 and 21; and 9 a.m. to noon, June 22.

The conference's General Assembly will be convened at 9:30 a.m. on June 20, in the Grand Ballroom. John J. Wilk, international vice president, 1962 International Conference, and Alfonso G. Pia, International president, NMAA, will address the attendees; Governor Nelson Rockefeller will deliver the welcoming address. Keynote speaker will be Dr. Kenneth McFarland, educational consultant, General Motors Corp.

Two closed circuit TV programs are scheduled. On June 19, from 2 p.m. to midnight, a ten-hour Datathon, originating from the Grand Ballroom will be telecast live over channel 6 on all receivers in hotel rooms and throughout the hotel. The program will include a panel of dp experts from management and personnel, scheduling, converting, information systems, optical scanning, MICR, information retrieval, etc.

The Datathon will also present interviews with persons prominent in data processing, seminar speakers, exhibitors, international officers, and conference attendees.

The second closed circuit telecast will be on the following evening, from 10 p.m. to midnight, and will feature discussions with seminar speakers who will offer a synopsis of the seminars. Also included will be evaluation interviews with persons attending the seminars.

Thirty seminars will be held during the conference, and have been scheduled so that each seminar will be presented twice, to allow for possible conflict of subject matter presented simultaneously. The seminar times are from 9 a.m. to 11:30 a.m. and 2 p.m. to 4:30 p.m., on Wednesday, Thursday and Friday.

Six subject areas of discussion have been selected, and are subdivided as follows:

Management: selecting and training staff; managing the data processing department; organizing the data processing department; efficient punched card department administration and operation; planning management development.

Machines: computer comparisons; machine communications; input devices; new concepts in data processing.

Systems Development: the accountant's role in data processing; the systems team; real time computer systems; scheduling.

Other Subjects: what you can expect from the service bureau; punched card installations for the small firm;

FOR HOTEL REGISTRATION CARD SEE PAGE 60

management decision games; automatic coding and programming; review of first year experience with a small computer; information retrieval; programmer and computer utilization measurement; operations research; a new approach to computer conversion.

Industry Sessions: banking; stock brokerage; use of management operating systems in manufacturing applications; retailing.

Applications: improving inventory management controls; general ledger; payroll and taxes; accounts payable.

Ten business tours are scheduled during the conference, eight on Tuesday and two repeated on Thursday: IBM, Poughkeepsie, N. Y.; RCA, Princeton, N. J.; RemRand Univac, Whitpain, Pa.; New York Stock Exchange (morning only); RCA Electronics Systems Center, NYC (afternoon only; repeated Thursday morning); IBM-NCR Data Centers, NYC (afternoon only; repeated Thursday morning); Autographic Business Forms, Hackensack, N. J. (afternoon only).

The conference banquet is scheduled for June 21, at 7 p.m., while the farewell luncheon will be held at 12:30 p.m. on June 22. Guest speaker will be Warren Hume, president, Data Processing Division, IBM.

A full ladies' program is planned, including a cruise around Manhattan Island, luncheon at Leone's restaurant, and a selection of sightseeing tours. ■

THE EXHIBITORS

The following manufacturers will exhibit their products at the International Data Processing Conference's Business Exhibition:

Addressograph-Multigraph
Administrative Management
Allied/Egry Business Systems
American Business Systems
American Data Machines
American Data Processing
American Lithofold
AT & T
Ansell-Simplex Corp.
Applied Dynamics
Autographic Business Forms
Automation Institute of America
Bankers Box Co.
Bensen Business Equipment
Business Automation
Business Efficiency Aids
Burroughs
Clarkson Press
Columbia Ribbon & Carbon
Computron
Conecticut Tab Card Bindery
Curtis 1000
Dashew Business Machines
Data-American Equipment
Datamation
Data Processing Accessories
Datex
Diebold
Dresser Products
Electronic Accounting Card Corp.
Electronic Associates
Engler Instrument Corp.
Farrington Electronics
Friden
Futronics
Gates Acoustinet
GE
General Fireproofing
HRB-Singer
Allen Hollander
IBM
International Sound Control
ITEECO
Jersey Tab Card
Kee Lox Mfg. Co.
Mac Panel Co.
Manpower
Middle States Mfg. Co.
Monarch Metal Products
Monitor Service Corp.
Monroe Calculating Machine
Moore Business Forms
National Blank Book Co.
NCR
John W. Nelson, Inc.
Normandie Dataforms
OA Business Publications
Edward Ochman Systems
Office Equipment Mfg. Co.
Office Publications
Office Temporaries
Oxford Filing Supply Co.
Prentice Hall
Programming and Systems
PWI Co.
RCA EDP
Ramsey Co.
RemRand UNIVAC
The Service Bureau Corp.
The Shelby Salesbook Co.
Snapout Forms Co.
Standard Instrument Corp.
Standard Register
Statistical Tabulating Corp.
Steelcase, Inc.
Systems Magazine
Systems Sales Co.
Tab Accounting Card Co.
Tab Products Co.
Tabulating Accessory Co.
The Tabulating Card Co.
Tech Panel Co.
Teletype Corp.
UARCO Inc.
Varifab, Inc.
Virginia Panel Corp.
Alfred Allen Watts
Weber Marking Systems
Western Union
Wheeldex & Simpla Products
Wilson Jones
Wright Line

NMAA CERTIFICATION

The 1962 examination for a Certificate in Data Processing (see Datamation, March, p. 25) will be held at New York University on Wednesday, June 20, at 2 p.m. Handling the arrangements for the examination are the NMAA's Advisory Committee and the Department of Education.

Complete details regarding the examination are available at local NMAA Chapters and NMAA International Headquarters, 524 Busse Highway, Park Ridge, Illinois. ■

THE PRESIDENTS' FORUM

A feature of the Conference will be the President's Forum, which will be held at the Grand Ballroom of the Statler Hilton on June 20, from 8 p.m. to 10 p.m. The panel members, representing top level management of leading computer manufacturers, will discuss "The Direction of Data Processing and its Relationship to Automation." The speakers will be:

K. T. Bement
Vice President, Marketing
Burroughs

R. E. Pfenning
Comptroller
GE

O. M. Scott
VP and Data Processing
Group Executive, IBM

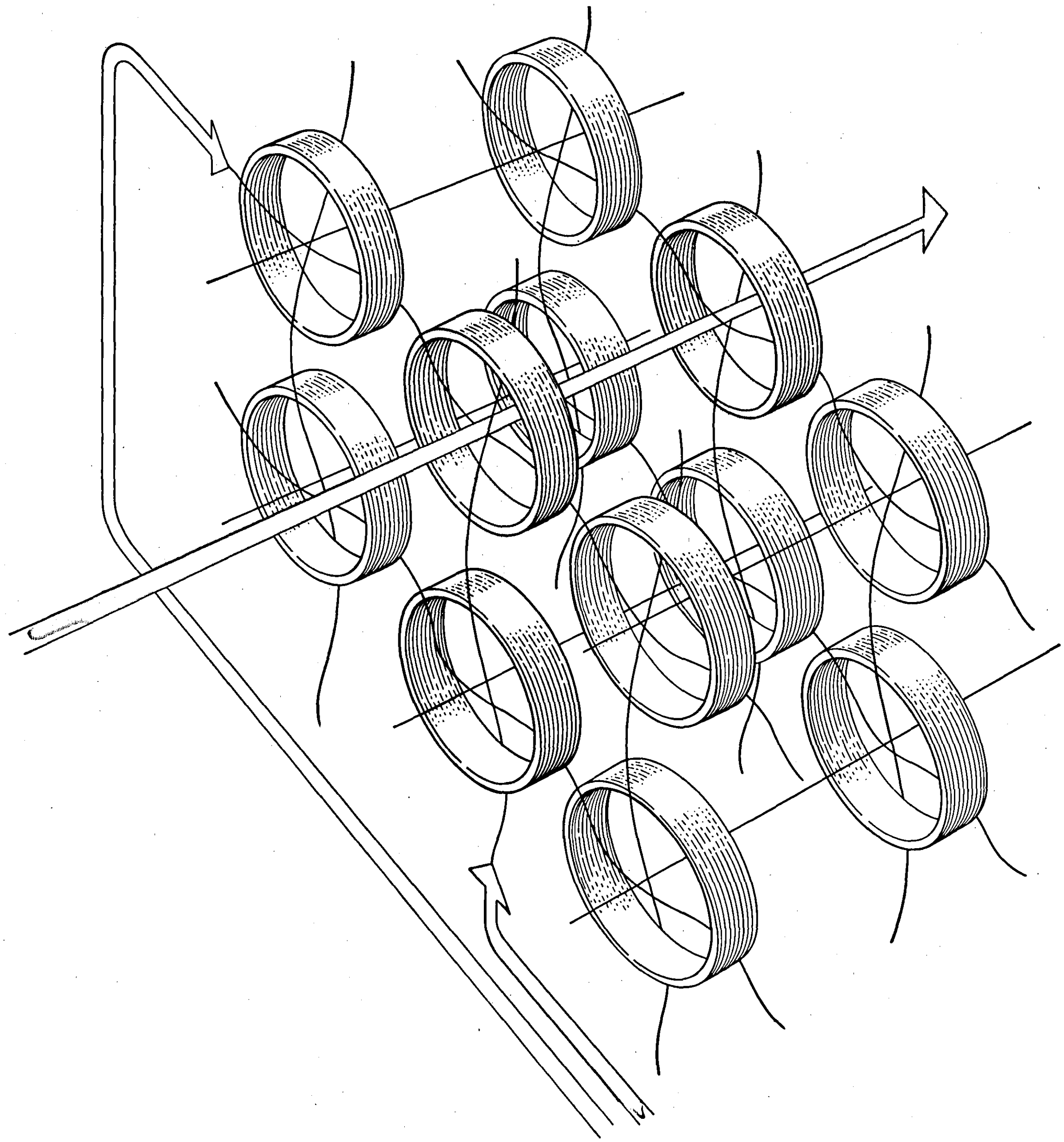
W. W. Finke
President, EDP Div.
Minneapolis-Honeywell

R. G. Chollar
VP Engineering & Research, NCR

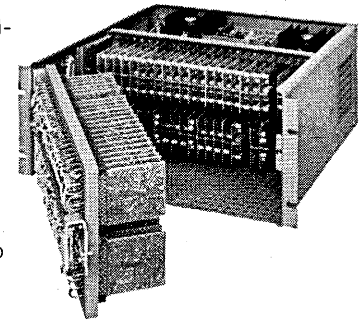
T. A. Smith
Executive VP, Data Processing, RCA

D. L. Bibby
President, RemRand Div.
Sperry Rand Corp.

Walter Cronkite
CBS
Moderator



STANDARDIZED COMMERCIAL COINCIDENT CURRENT MEMORY SYSTEMS



Daystrom Military Electronics Division is now making available a series of new standardized coincident current memory "packages". Designed for commercial data processing systems, the CCM memories present features as: highly reliable all-solid-state circuitry; high component density which results in sizes up to 30% smaller than presently available units; and cycle times as fast as 3.5 μsec. These commercially-priced CCM's provide the data systems engineer with a variety of packaged, modular core storage memories flexible enough to fit a vast number of design needs. Daystrom's CCM's are available as random access, sequential/interlaced, or sequential/non-interlaced. Word lengths of 8, 16, and on up to 64 bits, and capacities up to 4096 words are offered. The construction of these memories is modular, and many special features may be incorporated without major design change. Daystrom CCM systems reflect our extensive experience in the design of military digital machines such as the Navy's NORC memory and memories for the 465L global command and control network for SAC, in addition to our commercial one μsec memory series. They represent a considerable advance in the field of commercial memories. Send for technical data.

DAYSTROM, INCORPORATED

MILITARY ELECTRONICS DIVISION

ARCHBALD, PENNSYLVANIA

CIRCLE 21 ON READER CARD

FOR GENERAL ELECTRIC CIRCLE 22 ON READER CARD →

Not untypical as a heavy investor in computing hardware and software, the present posture of Minneapolis Honeywell's EDP division can offer no better spokesman than its president, Walter Finke. To clear away whatever haze may exist, *Datamation* fired a number of pointed inquiries at Mr. Finke during one of his recent visits to the West Coast. While several of his replies may not satisfy all well-heated iconoclasts, they should serve as interesting between-the-lines reading and as a reference for tomorrow's balance sheet of accomplishments and embarrassments.

FINKE, FACT & THE CHANGING FACE OF HONEYWELL

based on a taped interview with the president of the edp division

by HAROLD BERGSTEIN, Editor

Q: Mr. Finke, what is Honeywell's position with regard to the FACT compiler?

A: This matter of compilers is of serious concern to all manufacturers and it certainly has been to Honeywell, because we undertook what now in retrospect appears to have been a gigantic task in developing a compiler substantially ahead of the software art. We certainly have thrown a tremendous amount of effort into the venture, exceeding our original expectations.

The timing on FACT has stretched out because when we started the project two or three years ago no one could foresee the extent of the interplay between the preparation of the various segments of a compiler, and the tying down of all of these various factors in relation to its proper utilization.

The FACT compiler is now operating in the field at a number of our installations. Many of our users are now writing in FACT. We have released a succession of many hundreds of FACT compiler tapes each with improvements over its predecessor.

At our home office we have, of course, run a vast number of FACT programs and many of these are operating in first rate shape.

When one says that a compiler is complete, I think one raises a very interesting question. We have concluded that software engineering, and we call it that, is exactly the same as hardware engineering. It is going to involve a continuous improvement as feedback comes in from the field and we find better ways to do things. It will involve research and creative thinking about further additions to be made to the compiler.

As you know, there is an endless number of areas in which once you have a working compiler you can expand its use. And there remains the whole question of the measurement of efficiency of compilers which will eventually be the proving point on how valuable these instruments are.

My position, and I'm not a technician or a scientist, is that FACT, as a compiler is, indeed, complete and is achieving broader and broader use in the hands of our customers. The individual difficulties that arose in the early months after the compiler was released for preliminary use, have proven to be situations that can be solved. Areas in which the resulting speeds of object programs have been fairly high have shown themselves susceptible to improvement with intelligent application of manpower. In summary, I might say that FACT is rounding into a very, very fine instrument.

Q: With this very substantial investment in the development of FACT, what are your plans for COBOL, particularly, since given a choice, most users would probably elect to use FACT if compatibility is not a requirement?

A: I believe that this will be the case. Nevertheless, we are well along with our COBOL compilers for the Honeywell 400 and 800. With respect to the Honeywell 800 it appears that when our COBOL is completed, which is scheduled for the end of this year, the user will have an option in the business side of his operations to choose either COBOL or FACT.

There will come by the end of this year more sophistication and knowledge on the part of users, as well as producers, as to how you measure software and some means of comparing software both in terms of its efficiency, which is a matter of running time on object programs, and more importantly in terms of the spread of subjects that it covers. I think that it will inevitably be the case that the FACT compiler will cover a broader spread and range of subject matter than the COBOL compiler.

Of course, this is understandable and is no criticism of COBOL compilers. But in seeking commonness among various producers, there obviously were some limitations as to the rate at which coverage could be expanded. In our COBOL compiler, we will implement a very substantial number of optional features to make it a more effective compiler. However, we will also have put a couple of years of additional work into FACT.

These software implements don't fade away—they grow and improve. I think it reasonable to state that a user having a free choice and not concerned with compatibility with other systems, will have a means of measuring FACT against COBOL and, if he has no other considerations, will probably take the one which provides the most utility and better coverage for his particular application.

Q: Have some of the problems you have experienced in the completion of FACT changed your attitude toward software development?

A: Yes, it has had a very marked result in terms of our experience with that situation. It has led us to the conclusion that software, or the applications of software to EDP systems, is as important as hardware, and that it, therefore, must be assumed to be a part of the cost of doing business in this industry. It has also convinced us that there is as great a need for integrating organizationally the responsibilities in the areas of software as there has been historically in what all of us used to call engineering.

And that means an existing organization in the establishment of a computer manufacturer that carries the total responsibility for the planning, production, improvement, repair and the releasing of software products. Unless you centralize this authority, you create conflicts that you can't possibly integrate in a big organization. We have taken necessary steps. We have faced up to it.

At one time, I must say, we thought with many others that this was a simple addition to our products which could be procured here and there on the basis of contracts without creating a continuing overhead. This we no longer believe to be true.

As you know, we have created a Programming Systems Division that has the same level and authority in our organizational structure as our Engineering Division, or our Operations Division. It will itself be subdivided, like our engineering division, into R&D, production and maintenance. This is the way we are now heading in our organization. This is not to speak against the very fine consulting organizations in this field. We still use them from time to time. The difference is that we will always keep the responsibility for the form of our software, for its functioning and for its customer acceptance in our own organization, using outside people where they can be of assistance on specifically defined projects.

Q: How many Honeywell 800s and Honeywell 400s have currently been installed?

A: As of the end of March, approximately 40 Honeywell 800s, 10 Honeywell 400s and, of course, the seven D-1000s are still operating. There also are some six or eight Honeywell 290s in the field in process control applications. We are therefore now well past the 50-mark, which is significant in terms of operating revenue and in terms of installations requiring customer maintenance and support. This seems to me to mark the point when you reasonably come of age. As of January, we had delivered approximately $46,000,000 worth of solid state EDP systems and our backlog exceeded the shipments that we had made.

Q: Would you estimate where Honeywell might rank among the computer manufacturers?

A: This is a rather difficult question to answer and I think my answer must be a highly personal one rather than an attempt to judge any of our able competitors. First, we really ought to define what it is that we are comparing. In the case of some large companies in this field there are equipments that are included in total figures that relate to non-tape installations. This makes a comparison with our figures incomplete. In other companies, there are inter-mixtures with military shipments which has some bearing on the comparisons.

Let me say, and I admit my bias toward my own company, that it is my feeling that in terms of the value of our 50 major installations which we have in operation, Honeywell certainly would rank in the first three or four companies in the field, and perhaps second in the classes of equipment in which we are competing.

Q: In earlier conversations, you had expressed the feeling that Honeywell would not be bidding for a position in the super-computer class. Is this still the case?

A: Yes, and I think our position has clarified itself with some recent announcements. We now have a product line that stars at $4,900 per month for the Honeywell 400. With its various augmentations and some of the added options that we expect to announce in the next month or two, it will probably approach $17,000 to $18,000 as a maximum monthly rental. The Honeywell 800 system with some of the options we expect to announce for it picks up at about $18,000 a month and we think will run to as high as $45,000. The recently announced Honeywell 1800 Series will run from roughly $30,000 to $60,000 a month. So we are now talking about our area of the market in terms of monthly rentals ranging from $5,000 to 60,000. This is maximum. We do not intend to get into the giant computer class which, as you know, runs far higher than that.

The options I mentioned which will give our line even greater flexibility, relate to choices between three tape densities and, therefore, three transfer rates, and between two tape drive speeds. We have, as you know, high speed and economy magnetic tape systems.

Q: Would you care to make a projection as to when Honeywell's EDP division will reach a breakeven point or go into the black?

A: As we have stated that our EDP operation represented a substantial investment on the part of the company and that it was thought to be worthwhile because of the great opportunities in this field about which, as you know, I am extremely bullish. This burden is expected to continue in 1962, but hopefully, 1963 might well see the turn in this venture. This, however, is not a prediction. It is a hope based on the situation as it presently appears in terms of the growing acceptance of the product line.

Q: In the near future, do you feel that there will be a number of companies leaving the field, or will there be more companies competing for the same slice of the market?

A: In my own judgment we are approaching a period where there will be a reduction in the number of companies in this field, rather than an increase. As you recall, none of us three or four years ago could estimate how large the field might become in terms of manufacturers, except that it was the general feeling that the entry fee was so high that the number would not get too large. It has reached a fairly substantial number, but my own view is that this number will shrink. Let me say that it may not shrink simply by companies dropping out of the field completely, but it may become smaller in the broad sense in that certain manufacturers will concentrate on a specific area of the market, thereby reducing the number of firms covering the whole, broad spectrum of data processing equipment.

Q: If a comparatively small newcomer such as Control Data, for example, can produce an annual profit in their sale of computers, why has this proven so difficult for the majority of other companies, including Honeywell?

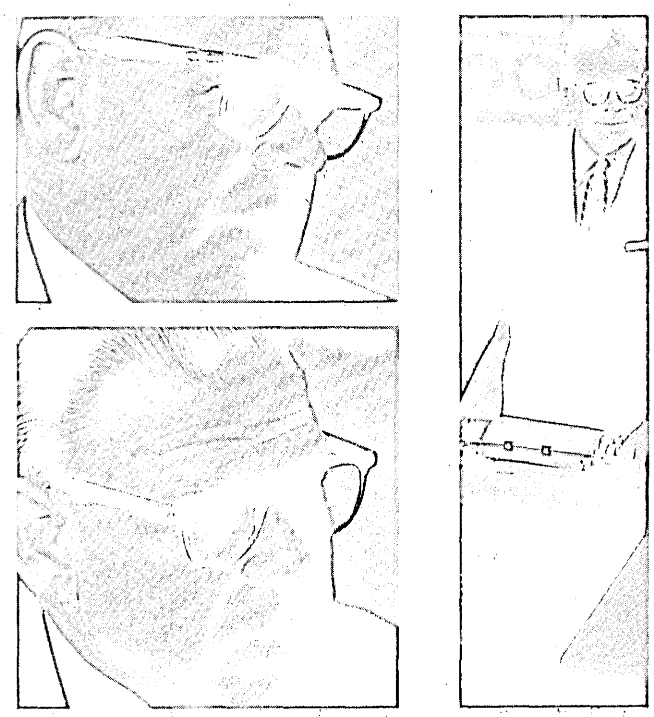
A: I am inclined to think that this problem might relate to the fact that when one limits the extent of penetration to less than the total market, say a small segment of it, it is possible to operate successfully in the early stages. I think that soon thereafter, if one is to continue in the broad field of EDP equipment, one must face up to the need to do many things today and pay for them in the form of current cost overheads which change the profit picture, yet these are investments which we feel are absolutely essential.

Q: What are your feelings about the approaching third generation of computers including, perhaps, thin film technology?

A: I do not believe that it will be a change in kind. I think it will be a change in degree and that the day of rapid and complete technological displacement of EDP is past, unless, of course, some development occurs which none of us can presently predict.

When you talk about change from a 100 microsecond cycle, you can have a number of steps which are really changes in kind because they are so big, but when you get down to a two microsecond cycle, the changes in degree are apt to be not nearly as impressive.

Therefore, I feel that changes will come in the areas of increased flexibility of systems, in reduction of production costs, which is very important to the manufacturer and the user. The question of thin film is, therefore, one in which any company must remain interested as they must in several other avenues that seem to open themselves up as possibilities, but their importance must be weighed in terms of economics as well as engineering or technical improvement. This is so because their significance to the users is simply a question of whether he can get more work done at less cost. I don't believe that



the coming of thin film memories in large sizes would have any devastating impact on the industry. I think that a much more devastating impact would occur if someone found a way to make a memory that costs practically nothing.

Q: You have recently announced the large-scale Honeywell 1800 with virtually none of the customary fanfare. Why?

A: It has been the practice over the past several years in the industry, and I must say that we have been a party to it, to hail and proclaim every new system as a great achievement. I think this was probably true in the earlier days as we were advancing very rapidly in terms of technology and there were not very many systems in the field. Each announcement did have significance. These were usually characterized by the press conference, by fanfare, as you say, by the full-page ad, and by all of the steps familiar to the industry.

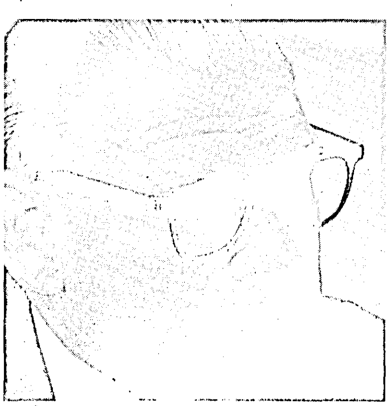
We debated this at great length and felt that with growing maturity in the business, and since we would be making numerous additions to and improvements in our product line, we should take these more in stride and that the sophisticated users would understand these new implements without the necessity of great pageantry.

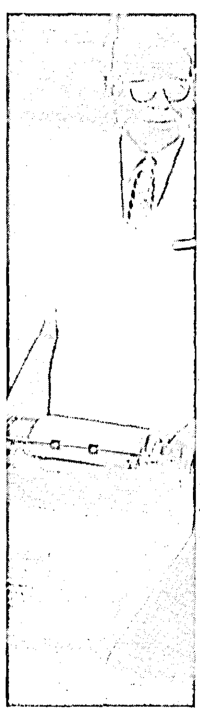
A second important factor, of course, is that the Honeywell 1800 is intended to be integrated into a product line and not a replacement or a new, great accomplishment that overshadows existing pieces of equipment, except in terms of its applicability. Finally, perhaps the whole industry has matured to a point where people are tired of the old, somewhat flamboyant approach.

Q: What is the chief competition for the Honeywell 1800?

A: We think that the Honeywell 1800 is a very hard running and able competitor to such systems as the 7090, 7094, 7044 of IBM and certainly the 1107 and related equipments of Sperry Rand. It is not intended to compete with LARC and STRETCH. It has definite upper limits in the top level class.

Q: A point of view recently expressed is that if hardware development were frozen for several years, it would provide us with an opportunity to more effectively apply current technology. Would you care to comment?





A: I think the statement taken simply as you have given it is correct. If you could stop the advance of technology on the hardware side, we would have an opportunity to close the gap in terms of improving our ability to apply and use these systems. However, I think that the question assumes something that cannot be accomplished. I think that there is no way to place a restraint on the ability of a new technology to find ways of improving itself.

I do feel that this technological improvement will continue at a much reduced pace as compared to the period from 1955 to 1961. Acceleration of the pace of change will come in our ability to better apply these systems.

There is one point I have neglected to mention which I think is significant to our discussion of software. It is apparent to me that as an overall policy in terms of the long run success and profitability of this business, we must do our best to relate existing software tools to new variations or improvements of the systems in the product line.

This is not easy to accomplish, because there are many who conceive new approaches to hardware configurations and feel that the optimum should always be obtained, even at the expense of obsoleting software. I think this is not in the interest of the customer or manufacturer and certainly not in the interest of achieving applications know-how.

Q: What do you consider the most serious professional problem which the industry today faces?

A: I think that the obtaining and training of people with the new skills required in the application of EDP systems is the greatest professional problem facing the industry. Also, we must continue to have available engineering and scientific personnel in sufficient numbers to carry the tasks involved in hardware improvement. I think we have a great problem in finding and training people to man the manufacturers' software departments, but largely we face the problem of obtaining enough able, bright people to understand the problems of applying these systems to provide customer support, to respond to increased training needs and to act as instructors in all of these classes of activities.

I believe there is a whole, vast area in which literally the obtaining of trained manpower is just as pressing a problem as preparing and delivering hardware.

Q: How would you evaluate progress in the field of data processing standards?

A: I certainly believe there has been a slowness of accomplishment in the field of standardizations. However, I think this is inevitable in a new technology. I think we are making progress, although very slowly, toward the solution of some of these problems. You have pointed out that as yet we have no glossary in the field. This is indicative of the fact that we aren't able to define our problems in this new technology. You and I have trouble with words here and it will take quite a while to arrive at some definitions so that we will begin to have a basis on which to advance a standardization effort.

With further regard to this problem, I frequently think of the fellow whose house was on fire. He ran out with an atomizer in his hand which he proceeded to squirt on the blaze. When questioned, he justified his action by saying that it was a step in the right direction.

Of course, I am being facetious, but the fact is that the work on standards is certainly, at this moment, far from final adoption of a series of EDP standards. Nevertheless, the work must go on. It must have the support of all groups, not only manufacturers, but users as well, so that we can eventually underpin this technology with some definable framework. All of this will come in the future, but it will take long years of hard work.

Q: Can you predict any future trend as far as centralized vs. decentralized facilities are concerned?

A: I think the new EDP systems will have a profound effect on management practices. It is becoming more evident every day that management has a willingness to explore new approaches to integration of management processes. I think we must have the vision to see that the end of EDP is not simply to seal in existing inefficient practices, but rather to open thoughtful minds to new approaches to the problems of procedures in business and industry.

My own feeling is that these systems coupled to the increasing efficiency of communication links, will tend to lead in the direction of centralization, particularly on procedural matters. This may not affect the centralization of ultimate policy decisions, but certainly it will result in a pulling together, rather than a continuing pursuit of the trend which, as you know, up to the early '50s was to push out all procedural matters on as decentralized a basis as possible.

Q: For the near future, what geographical region do you feel is the most lucrative for Honeywell EDP equipment?

A: I believe the West represents a tremendous market for EDP systems—one in which relatively speaking we have not progressed as rapidly as we have in the East. This is natural. The East is close at hand, but it is our hope that our product line will expand in installations on the West Coast at an increasing rate.

Q: As for marketing directions, are there any specific fields aside from the military, in which you feel Honeywell will be concentrating its sales efforts?

A: Our interest will probably now turn to some of these areas that involve what might be called special systems, (although I don't like this word particularly), that are digital-computer-oriented and based on existing hardware. I believe the government is coming more and more to a position in which they no longer need to build a special and separate computer for every purpose, and that the interest of the whole country, as well as of the government, is served best by using existing computers, with special interfaces or special conversion gear.

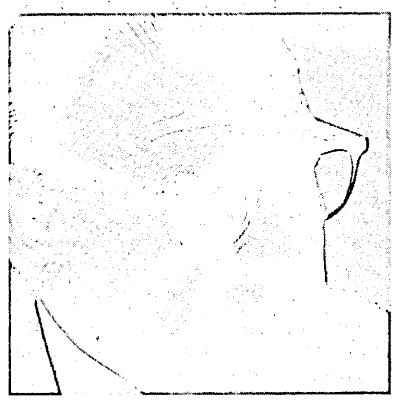
With the Honeywell 1800 system we are interested in certain scientific areas in conjunction with space explorations and, of course, in data reduction. In private industries, we are interested in the integration of existing computer systems into larger systems that may be oriented around a total business complex. The increasing flexibility of communication links makes it possible to meet these special needs.

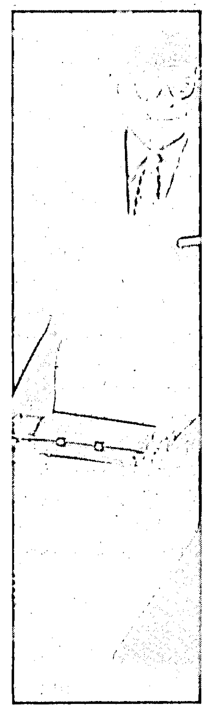
As we find new uses for EDP systems, and I'm sure we will continue to find them in great number, we may also need in conjunction with each application, some special interface or piece of gear not too complex in itself, but necessary in order to bridge the gap between the function of the new application and the system itself. We are interested, for example, in the use of existing computer abilities in vehicular traffic control.

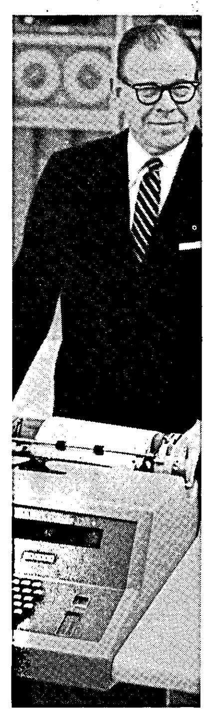
As another example, I am interested in the educational area in which there is a growing need for the power of these systems to facilitate the educational process, whether it be for the local community board of education or state programs of education. I am sure there will be a great surge of activity in these areas in the next five years, and I'm sure that EDP systems will play significant roles in them.

Q: One final question. Do you feel that your computers are displacing workers or creating serious unemployment problems?

A: At this time, I don't think that EDP systems are displacing workers. We have found no areas of actual displacement of people. I think that computers are minimizing the need for bringing in additional workers, but I believe that the procedural problems of business and government are so vast that without the power of digital computers, literally we would be unable to keep pace with the daily requirements of this growing nation of ours without the increasing use of this new and powerful tool of office automation. ■





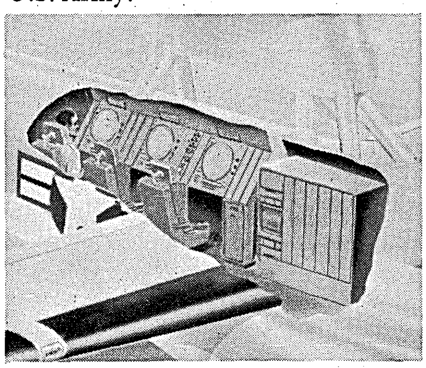


ADVANCED AIR DEFENSE SYSTEMS WITH FIRST-DAY CAPABILITY

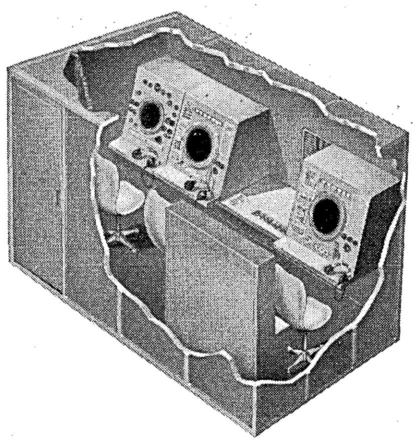
The needs of today's air defense systems pose a problem that would have seemed insoluble ten short years ago. The problem of furnishing mixed-weapons command and control, with first-day capability, in a system that is portable to any place in the world.

Here is how that problem has been solved through creative engineering utilizing a decade of industry progress in tactical data systems.

Systems already delivered by Litton to the military, or in the advanced state of development and production, include: Airborne Tactical Data Systems (AN/ASQ-54, AN/ASA-27) for the U.S. Navy, the Marine Corps Tactical Data System (AN/TYQ-1, AN/TYQ-2) for the U.S. Marine Corps, and the AN/FSG-1 Retrofit Improvement System (OA-3063/FSG-1 (V)) for the U.S. Army.



The first of these, the Airborne Tactical Data Systems, provides a capability for the mission of Airborne Early Warning and Control (AEW & C) in defense of large land masses, attack carrier task groups and other naval units. Both the AN/ASQ-54, installed in a land-based AEW & C aircraft, and the AN/ASA-27, installed in a carrier-based AEW & C aircraft, furnish early warning data on enemy raids to surface elements of an air defense network and provide airborne control of interceptors.



The second of these systems, the Marine Corps Tactical Data System (MTDS), features capabilities for continuous and effective control of Combat Air Operations during an amphibious assault. Facilities are available for control of aircraft on missions such as close air support, reconnaissance, and interdiction and for air defense with mixed weapons, both ship-based and shore-based surface-to-air missiles and interceptors. An integral air traffic control system assists in initial and continuous identification of friendly aircraft.

The third, the AN/FSG-1 Retrofit Improvement System, significantly increases the counter-countermeasures capability of the AN/FSG-1 Missile Master System deployed within the Continental United

States to furnish surface-to-air missile battery coordination in the defense of large cities and industrial areas.

Through the successful design, development and manufacture of systems for air defense missions, Litton has demonstrated its capability to proceed with even further advanced data systems. Such systems are now under conception and development at Litton.

Air defense systems that not only fulfill today's defense requirements but also defy obsolescence for years to come require engineering that is versatile, inventive, aggressive, and adaptable. This is the kind of engineering Litton expects from its people. If you are qualified to perform engineering at this level, you are invited to write: H. D. Laur, Litton Systems, Inc., Data Systems Division, 6700 Eton Avenue, Canoga Park, California; or telephone DIamond 6-4040.

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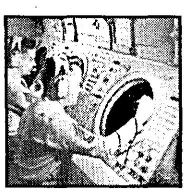
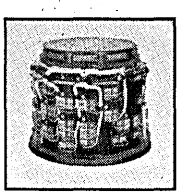
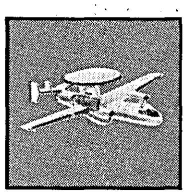






DATA SYSTEMS DIVISION

LITTON SYSTEMS, INC.

A DIVISION OF LITTON INDUSTRIES

DATA HANDLING & DISPLAY SYSTEMS • COMPUTER SYSTEMS • MODULAR DISPERSED CONTROL SYSTEMS

The gratifying response received after publication of "How To Design A Kludge," by J. W. Granholm (*Datamation*, February, 1962), has prompted a full-blown series of seven Kludge reports. "How To Market A Kludge" is second in the series. Others will reflect on programming, maintenance, management, installation, and intellectual implications of Kludges.

Solicitation of authors for this series has proven no problem whatsoever; in fact, a screening process has been initiated to insure competence and a venerable backlog of experience in some aspect of Kludge creativity. The sole requirement which many prospective authors have insisted upon is anonymity for fear of being chucked out of a paying job. And since unemployment compensation is not one of the rewards for *Datamation* authorship, the editors have concurred in establishing an absolution of responsibility via the cowardly route of a pseudonym.

shrewdly

HOW TO MARKET A KLUDGE

by OSWALD I. ORTHMUTT, Vice President, Marketing, Kludge Komputer Korporation

With deference to previous and future authors of this series, it should be emphatically understood that to market a kludge is somewhat more difficult than to design and manufacture one. For proof of this congealed pudding, merely reflect on our record. The 650th design of the Kludge Komputer Korp. uses bi-quinary, BCD, and binary for arithmetic, the Dandy-1000 uses binary internally, but cannot read or punch it; and among the lower production versions is the HOT-FLASH X2E which was born an orphan and has remained parentless for want of massive sales support from our Korporate headquarters in Peachfuzz, Alabama.

To compete or not to compete is the primary marketing question! To answer it properly, money from Peachfuzz must be encouraged. All other factors are incidental and largely unnecessary. To obtain backing, a report of some sort is certainly nice to think about. Typing it up is quite another matter.

To accomplish this, one must analyze with polished shrewdness, the characteristics of the market, the potential reception of unwashed users and ultimately, the performance of KLUDGEVAC 990B.

One method of being certain to obtain the most favorable report is to seek the counsel of a management or marketing consultant with an active curiosity about the Komputer field. Experience is undesirable. And since consultants are generally seated in a strikingly unbiased position, their input may be gently colored so that only correct conclusions are drawn.

After a report has been received, it will be couched in such general terms that it must be interpreted to management, orally and over cocktails. This fact alone guarantees that the budget and staff befitting such an endeavor will be obtained from the Korporate headquarters without curious visitations to the manufacturing facility.

It is best if the above market survey can be completed before the hardware manual is finalized and documented. If a manual on the equipment exists, one runs the risk of having it read and subsequently losing control of the report. If a manual exists before the market survey is in, there is a serious risk of being stuck with a definitive survey report which will never do.

setting the price

After the firm decision to produce is made, the price must be established. In this regard it is best to price as vaguely as possible so that one may compete with entrenched machines *now* in the field. Prices on existing, operable equipment are generally higher than those to be delivered at the same time as the 990B and hence the markup on the 990B will appear to be greater. For added pricing flexibility, offer quotations with a profusion of peripheral gear. Never quote on the main frame alone!

After the greatest possible markup is obtained, hold out for impressive commissions when the letter of intent is signed. That way you get yours. It's best not to enter the discussions on manufacturing volume at this time. Let manufacturing and engineering bother their heads with this small problem. Later when the costs soar out of believable proportions, produce the marketing report which will most certainly show the expected volume even higher than anticipated. Thus, one protects a high commission scale with infallible evidence perfectly timed.

the gimmick

Now that the market has been surveyed, the volume established, and the price determined, all that remains is the advertising. Before one can produce news releases, ads, give papers, etc., a gimmick is needed. The days are gone when arithmetic speed, flexible in-output, compatibility, or throughput per dollar will sell machines. We need a thing! The thing can be a simple come-on or it can camouflage some glitch in the kludge.

For instance, the KLUDGEVAC 990B has an incurable cross coupling between the load button and the tape write circuits. Every time the load button is depressed, the character under the read-write head is erased. While this might be unhandy for some applications, it could be called "Auto Message Protection" (AMP) and sold to a variety of government agencies.

Another unique feature of the 990B is Recent Rollback Record (R^3). If the master power switch is thrown unintentionally or if the power supply fails, transients cause the B to reference memory at the current instruction counter and to reset that cell by destructive readout. This may be heralded as Recent Rollback Record. The restart program has to merely determine which cells won't hold ones, compare this with the previous cumulative-to-date list of R^3(s) and the first difference is the contents of the instruction counter at the instant of power failure.

In addition to emphasizing these unique features on the 990B, it is always advisable to contribute to the glossary of the field. This is preferably done by taking some familiar, prevalent concept and establishing a synonym for it. The competition is already entrenched in the input/output area with such terms as block, record, item, unit, and message. There is even some disagreement over such terms as index register and B-box. This obviously is bigger than the marketing division, and hence a Management Policy is called for.

This is a particularly fertile area for management participation as they probably can't define the accepted terms in the first place. From such a series of meetings you will have the opportunity to meet the new members of management council: the Razor Head Auditor, the Kiddy Games Planner, and a Ball Point Pen Comptroller. From such a collection of advisors, the sales plan will gradually emerge. The device which contains all of the operator buttons, switches, lights, and panels shall be known as the Associated Display Device of Elementary Registers (ADDER). The device connected between the mainframe and the individual input-output units from which source data is read from or punched on 80 column unit record shall be known as a Complete Assembled Record Distributor (CARD). The device which places symbols on a sheet of paper in a line by line fashion shall be known as a Writer Of Record Data (WORD). We now have a full product line!

announcement

Timing an announcement for a major press conference is most important. Do not plan it for a Sunday. Late Saturday afternoon is best. Invite the secretaries. Invite the salesmen. Invite the president of your company to sing the Star Spangled Banner. At KKK the vice president for marketing is always on hand to explain the wonders of software systems.

Most important, an announcement should be bold and decked with the prickly rose bushes of tomorrow's world as directly influenced by the 990. Applications such as simulating rattlesnake brain envolvements, varying the parameters in sausage recipes, and pipe organ effects uplift the interest factor among news beagles and other hounds.

Equally most important, don't invite questions. If the salesmen attend, plant a few questions such as, "Will this machine truly stop the Commies?" and "What does the magic brain think about capital punishment?"

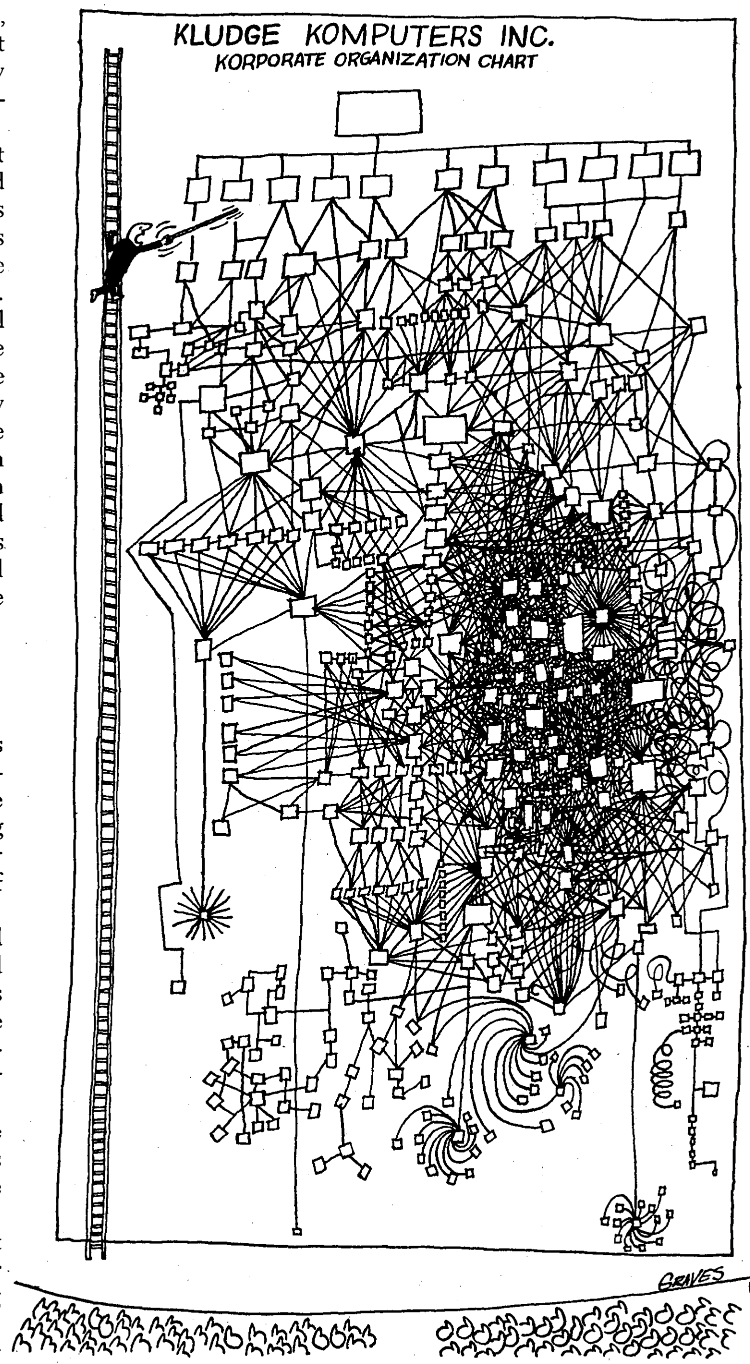
When demonstration time rolls around, explain that the machine is battery operated and ask for volunteer batteries. Show movies and keep the secretaries wandering around the room with bottles of good cheer.

Laugh it up in a cynical fashion. Press people are very cynical.

the sales staff

Now that the announcement is completed and press clippings collected, the selection of a sales force must receive immediate attention. The first task in this regard is to clean house. Move the timid ones back out into the field. Let them rejoin your competitors. Since you now have a budget you may choose a few good men with contacts or many neophytes and let the customers train them. A compromise that is often tried is to hire the Disgruntleds back from the competition. This plan saves all those travel and training dollars. You can fill in the weak spots with recent college graduates or engineering throwbacks.

If you insist on daily call reports, they won't loiter in the office learning the product line. By getting them out of the office and on calls, they start making contacts from the day they come on the payroll. The present users are the most obvious first calls to make. They just may be unhappy enough to re-program. In addition, they are the



most knowledgeable and hence the new men can learn the vocabulary "on the job."

appeal inducers

Also responsible to the Vice-President-Marketing are certain projects classed as appeal inducers. Our Sign and Slogan Group came up with the startling - -

The Gimcracks and Googaws Section is working on a client's office mobile which depicts the balance of time and space over a cascade of buffered input-output units. The Social Impact and Math (SIAM) Department is working on a new user language which offers some astounding breakthroughs. It is an amalgam of Machine language, Algol, Generators, Interpreters, and Cobol.* It takes in absolute code in binary, hates formulas, puts out 400 cycle 220 VAC, and recognizes French and Russian verbs. It has also transposed the Washington Post March into a minor key and output as Cobol narrative a piece known as Phillips Forever, or BEMA Valentine. All in all we are very proud of it.

Early reports indicate that it slows down the KLUDGEVAC 990 so much that our net income will double for this fiscal year from increased second shift rentals alone. We at KKK are very excited about the few minutes which were spent with the programmers, metalinguisians, and associated hangers-on. These sessions have done more to mask out the glitches in the basic kludge than we could have obtained with next year's engineering budget. Of course, the customer pays a slight performance penalty, but one can't have everything.

Since we don't propose to furnish machine manuals, training, or a one-for-one assembly, we feel that all of our customers will use MAGIC exclusively. So sure are we of our ability to meet our committments that we have a standing offer of double your money back (plus a dead chicken) if we fail to compete throughput-wise with machines half our size.

This particular department is backlogged pretty bad right now, as the impact of our software is tremendous. Not only is our own MAGIC language gaining popularity but our sales force has committed us to integrate PACT, BACKACHE, CAGE, FORTRAN, SURGE, SPEEDCODE, COMTRAN, JOVIAL, UNICODE, FLOWMATIC, MAD, MATHMATIC, AND NELTAC into one grand system similar to S.O.S. This meld will be known as PBCFSSCJUFMMN. Once this is put on the system tape, our crew will be free to work on a higher level POL as PBCFSSCJUFMMN will be coded in its own language and hence is selfmaintainable by customers without ancillary documentation.

the outlook

I must admit that we of KKK have not been too elated over our penetration with the KLUDGEVAC 990A. Since we have had 990A's around for 7 years, and our only sales have been to Federal Agencies (NASA, USDA, IRS, CIA, and DTMB), we are somewhat at a loss to explain our lack of commercial civilian sales. We hope that the 990 series and in particular the subminiature, petrified state, thin film, 994 (which is orderwise compatible with the 990) will raise our penetration to .003%. This is our classical share of the market and we hope that our model 994 (with the disposable mainframe) will allow us to retain it in the face of severe competition.

***We know this spells MAGIC, but we prefer to call it STUPENDOUS.**

ANNOUNCING

Control Data Corporation is proud to announce the new Control Data 606 high performance magnetic tape transport for the storage and manipulation of digital information. The 606 features pneumatic control of tape movement that provides smooth, uniform tape acceleration with minimum stress and stretch to the tapes.

The head assembly consists of individual read/write heads, an erase head, pressure pad, and vacuum-operated tape cleaners—designed to maintain precise head-to-tape contact pressure and reduce head and tape wear. The dual-gap 7-channel head construction provides read-while-write capabilities . . . as well as format compatibility with most major existing tape systems.

Designed for full computer control with no programming restrictions, the 606 was developed by Control Data computer engineers who know the value and importance of reliable, trouble-free operation in high performance equipment. Electrical and mechanical adjustments in the 606 have been minimized. The inherent reliability of all solid-state components is safe-guarded by direct-blast cooling.

Ease of maintenance is facilitated by provisions which permit quick replacement of major components through the use of pluggable modules and sub-assemblies. In multiple-unit systems, each 606 can be individually serviced for testing and maintenance without effecting the operation of other units.

The Control Data 1615 Tape Control Unit is used to connect the 606 Tape Transport to Control Data's large-scale computers. Up to eight 606 Transports can be controlled from a single 1615. As a standard feature, electronic circuitry is included in the 1615 to operate Control Data computers in the Satellite Computer System.

DETAILED SPECIFICATIONS

RECORDING FORMAT
- Method—NRZ (non-return to zero—change on ones)
- Seven-Track Recording: Data—6 bits; Parity—1 bit
- Inter-Record Gap—¾ inch
- Tape Markers
  End-of-Tape & Load Point reflective spot
- Compatible with IBM 727 and 729, I, II, III and IV Tape Units

TAPE
- Width—½ inch
- Length—2400 feet with 1½ mil base Mylar tape
- Reels—10½ inch NARTB hub with file-protect ring

TAPE SPEED
- Read/Write—150 inches/sec.
- Reverse Movement—150 inches/sec.
- Rewind & Unload—225 inches/sec.
- Start Time—4 millisec. max.
- Stop Time—4 millisec. max.

RECORDING DENSITY—Selectable
- Low—200 frames per inch
- High—556 frames per inch

CHARACTER RATE
- 83,400 per sec. @ High Density & 150 inches/sec.
- 30,000 per sec. @ Low Density & 150 inches/sec.

HEADS
- Physical Spacings (forward direction):
  Erase gap-to-write gap—7/16 inches
  Write gap-to-read gap—0.300 inches

PANEL
- Operator Controls with Indicators:
  Power/Load Point/Forward/Hi-Lo Density/
  Reverse/Ready/Unload/Clear/
  Unit No. Selector
- Operation Indicators Only
  Read/Fault/Write/File Protect

PHYSICAL CHARACTERISTICS
- Size: Height—72 inches
  Depth—33 inches
  Width—28 inches
- Weight: 800 pounds
- Power—115v, 60 cycle, 3 KW

PITFALLS & SAFEGUARDS IN REAL-TIME DIGITAL SYSTEMS

part two, emphasis on programming

by W. A. HOSIER*, Systems Engineering, Sylvania Electric Products, Waltham, Mass.

An underlying purpose of the original article was to remind the managers of real-time digital systems what few DATAMATION readers need to be told—*viz.*, that the computer program is an integral and vital part of such systems, which can not be casually written at the tail end of the development like an instruction manual. The first half of the article, published here last month, suggested the influence which programming considerations should exert on equipment selection and design. This half desribes the process (and hazards) of creating a working system program, with less regard to the equipment involved.

People have been writing programs for computers for more than a decade now—to compute tables of Bessel functions, to figure payrolls, to simulate performance of jet engines and nuclear reactors, etc. One may legitimately ask, is real-time system programming significantly different from these? The answer is yes. One word epitomizes the difference: constaint.

peculiarities of real-time programming

The following six characteristics, present in varying degrees in different systems, serve to set real-time programming apart from its more relaxed non-real-time counterparts:

1) Input-output and internal control decisions are intimately allied to system hardware and to specific timing requirements of the environment.
2) There are absolute limits on running time.
3) The time constraint imposes what amounts to absolute limits on storage.
4) The consequences of errors are likely to be serious, at least if not promptly detected.
5) The program must adapt itself to overload conditions and other significant changes of the system environment, automatically.
6) As an enduring product of team effort subject to modification by persons unknown, the program requires systematic documentation and rigid control of assembly and testing.

One might add the frequent requirement for uninterrupted operation, but this is primarily an equipment problem in spite of probable involvement with the program. Insofar as program operation resembles thought, one might consider a non-real-time program as thought in a book, or at a desk, or in conversation, but a real-time program as thought under pressure in the midst of action.

The main observation on the first point is that each programmer must see clearly his role in the system and understand all the rules. General system education, desirable in some degree for all participants, pays particular dividends for programmers, since their task touches most others. If they are to understand the rules—*i.e.*, the specifications and interface documents—these must be clear, and available when needed.

The second and third points are so closely allied as to amount to one. It has already been suggested that cost-accounting procedures be applied to time; the same is true, and easier, for storage. Budgeting is also useful. A large program will have 20 or more sections constructed by different people. If they are given carte blanche on time and storage, they will only have to do the job over. Naturally, the allotments neither can nor should be very precise at first; but if the budget is refined as pieces take shape, better warning can be had of potential overruns in time to take corrective action. Ingenious programmers now and then will overdo compression to the point of making their work hard to understand and hard to change. Straightforwardness is preferable as long as there is room for it.

There is one important corollary to these two points: they restrict the use of compilers.

As a matter of fact, any constraint is apt to qualify the use of a compiler. The compiler will produce programs that have one family of constraints inherent in its own design; the more other constraints the program has to satisfy, the less likely are the two sets to be consistent. Time and storage are likely areas of conflict, for the good reason that the conservation of time and storage in the produced or "object" program is usually a compromise peculiar to the individual system and difficult to provide for in compiler design. It is extremely difficult to tell, without trying, whether a given compiler is adequate for a given real-time system program. Nothing in this author's limited experience can be recommended without qualification. The System Development Corporation (SDC) has constructed one compiler language, known as JOVIAL, for a particular real-time system purpose (the Military Computer in the Air Force's 465 program), and it is undoubtedly versatile enough for other applications.

According to a report, "Computers in Command and Control," issued in November 1961 by the Institute for Defense Analysis, Jovial compilers now exist for most large machines, and two other languages, "Nelliac" and "CL-2", are applicable. This IDA report is well worth reading for several aspects of real-time digital system design.

In general, time and storage restrictions make it essential in real-time programming to pay close attention to layout of all stored items, the reduction of waste motion, and the pooling of everything that can be used in common. This often takes trial and study and implies that such a program is seldom dashed off in a hurry.

A single-instruction symbolic assembler, old enough to be reasonably free of "bugs," is a somewhat primitive tool, but it is the only tool which at this date can be guaranteed to work in all cases.

The foregoing admonitions regarding compilers should not be construed as indicating bias against their use. Indeed, system programs of a large size (say, somewhat arbitrarily, over 50,000 instructions) may be virtually impossible to produce, much less to modify, without the

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*W. A. Hosier was first associated with digital computing at M.I.T.'s Lincoln Laboratory from 1952-1957 where he participated in the design, programming and testing of the prototype SAGE system, and supervised the first computer (MTC) which used a coincident current ferrite memory. Since 1957 he has been at Sylvania with responsibilities for the design of the Plato anti-missile system, and the selection and configuration of computer equipment for BMEWS.

The following article is the conclusion of a two part series; the first part appeared in April. In a different format, it was first published in IRE Transactions, June 1961, but has been substantially revised by the author to better suit the specific interests of *Datamation* readers.

help of a compiler; and a *suitable* compiler will greatly lessen the amount of trial and error and detail in any program development. But choosing a compiler, like choosing a wife, is hard to undo after getting involved, and is not to be taken lightly.

Point 4) means, first, that the testing of a real-time system program must be very thorough indeed, and second, that as many internal checks of consistency and reasonableness as possible should be built by each programmer into his own contributions. Programmers should be imbued with the doctrine of anticipating possible troubles and detecting or correcting them. Unfortunately, there will have to be a compromise between 100 per cent checking and the limitations of time and storage, so that it will be necessary to pick out critical items and processes.

Point 5) is not always present. Some systems (*e.g.*, missile guidance) will have a reasonably constant and predictable load. But when it is, as, say, in the case of air-traffic control, then the program's design has to be carefully considered in the light of the origins, nature, and frequency of overload, and the system consequences of alternate courses of action taken by the program. Sampling is a possibility (not for air traffic!). Action to reduce the load (if possible) is another. Partial postponement is a third. Reduced accuracy is a fourth. It might be added from a programmer's viewpoint that system managers seldom make up their minds on the handling of this problem soon enough to assure its being worked into the original design of the program. Sometimes it is a costly feature to add at the eleventh hour.

Item 6) is not absent in all non-real-time programming. Many such programs—utility programs in particular—have to be thoroughly documented and tested; but the circumstances are seldom as stringent as in the real-time case. For one thing, system programs are more apt to be written in pieces by several programmers and usually have more interdependence among pieces. For another, a system program will usually have more exact specifications, and questions of contractual compliance arise that seldom occur in non-real-time programming. Urgent changes may have to be made, far removed in space or time from the source. So program documentation, no less than that for the rest of the system, must be systematic, adequately circulated, explicit, well-supervised, and up to date. Program testing, already brought up under point 4), is so large an issue that it will receive an entire subsection below.

organizing attack on the program

Most of the generalities cited previously under "System Genesis" have considerable force also in program genesis. The common difficulty is vagueness of command, or even total lack of it. Little groups will be told to study this and simulate that; each one will proceed as it sees fit; and they will still be studying and simulating two years later unless a structure is imposed on them which reflects the whole task, and completion targets are set for the main parts of it. It may be hard to foresee the structure entirely at first, but if it is not too wildly Procrustean, it will get things moving; and it can always be changed.

Initial thought and discussion will have to occur to sketch out this structure—perhaps even some detailed study and simulation. The old proverb about too many cooks was never more appropriate than here, nor is this the place for inexperience. Quantity is in no sense a substitute for quality; it will only make matters worse. If one man could handle the whole job, it were best left to one man (prudently, with an understudy); for a system program is essentially a thought process made graphic, and is not easy to transfer intact from one mind to another.

Not uncommonly, this design period will coincide with augmentation of the programming staff by numbers of junior personnel. The designers should not be saddled with the distracting burden of keeping subordinates profitably occupied. Junior personnel will need system orientation and can assist with simulations and auxiliary programs; but their supervisors should not have major design responsibilities during this early formative period, or what should be planning will degenerate into improvisation.

The primary design effort must proceed along two separate but converging lines, which finally unite in coding. These are the familiar lines of form and content.

A secondary design effort on tools and procedures for program production and testing is essential to carrying out the primary design. In many respects, it has to precede the primary design; therefore, no time should be lost in setting it up. The flow chart of typical real-time program development, Fig. 2, shows the main stages of the process which this paper is describing; and it is apparent how necessary to each stage are the corresponding test procedures. The standard utility-program part of these tools will be in some degree ready at the start. However, many special-purpose tools will have to be designed: simulated-input generators, test control and recording, and data-reduction routines to analyze test recording. Special hardware may also be needed as an adjunct to testing, to simulate external system signals and responses. Routines like these will not have to be as painstakingly built as the system program itself (compilers should be used to construct them wherever possible); but their total bulk is likely to exceed that of the system program, and they will themselves require testing; so they must be started early. Input simulation is a good place to start, since it depends less on internal details of the system program.

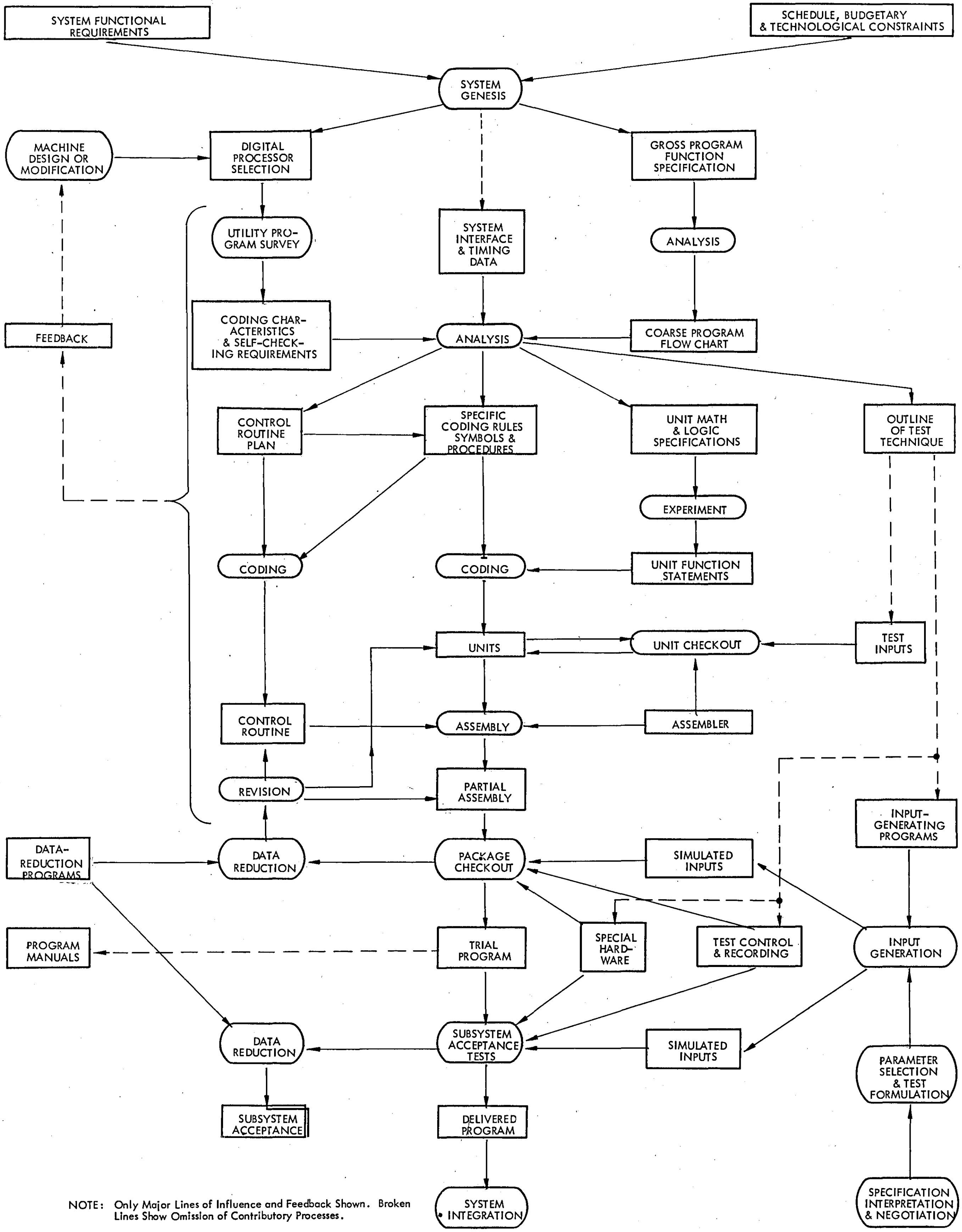
form and content of the system program

Form, in a small-scale linguistic sense, has to do with the symbols and conventions imposed on the programmer by one's choice of compiler or assembler. Assemblers, being general-purpose and versatile, purposely give programmers wide choice of symbols. Since system program units must communicate with each other, the symbols they use cannot be left to chance or caprice. This means that an orderly corpus of symbology, conventions, and procedures must be set up to cover all items of common usage. It must be kept up to date and readily accessible to all programmers. Like general system documentation on a smaller scale, program documentation can usually profit from a "librarian" and an indexing system. In most systems, the symbology is extensive enough to justify recording it in a punch-card file.

There is another, more difficult, aspect of form. This is the "paragraphing" of the whole program, its organization and transitions, constituting the control linkage that holds it together. It is difficult because it must be appropriate to content and "audience"—*i.e.*, the rest of the system. To arrive at it, an over-all flow chart has to be sketched out and the precise manner of attaching members to the framework defined. The structure must anticipate somewhat the techniques of assembly and testing, in allowing for temporary bypassing of missing units, ubiquitous insertion of test recording, and addition of units to a partial assembly without complete reassembly. Something should also be postulated as to how overload response, if required, will affect the structure, even though system specifications for this are lacking.

Content begins with the functional requirements of the system; but these have to be worked out to a painful level of detail and their implications at least partially digested before they can serve as a basis for coding the units of the system program. Initially, a small analysis group will have to categorize the data-processing tasks and their intermediate inputs and outputs.

But gradually, production teams will become more self-sufficient as the initial form of the set of program unit function-statements emerges, and the analysts can turn their attention to other aspects of the problem. Initial func-



NOTE: Only Major Lines of Influence and Feedback Shown. Broken Lines Show Omission of Contributory Processes.

tion-statements will undergo change in the course of checkout and testing; they probably will not be considered final until the program is delivered.

Some details of content, such as those that depend on system interfaces, may be a long time appearing. At some established schedule point, they will have to be explicitly stated, but considerable program progress can be made on general descriptions and assumptions, provided that outside limits are stated and that programmers understand how much is specification and how much is assumption.

assembly

When a large program is composed of several units, each programmer will check out his own as best he can, using methods appropriate to the unit. Having done this, one must decide how many units to combine at once and in what sequence. Experience has shown one negative answer: putting all units together at once is the worst possible method. Too many malfunctions occur, and they conceal each other. A gradual, functionally-expanding build-up usually works best, each partial assembly being shaken down before a new unit or related group of units is added. However, units will not all be ready simultaneously. Depending on their complexity, the availability of specifications, manpower, priorities, etc., some will appear early and some late, and the build-up sequence will be a compromise between this and some logical ideal. Nevertheless, it should be approximately foreseen, have its major phases marked as schedule milestones, and have auxiliaries scheduled in parallel to be ready when needed.

A common error in planning production of a system program is to underestimate the time needed to combine units after they have been coded, allowing excess time for their prior refinement.

As a rule of thumb, of the time between appearance of the first unit function-statements and the beginning of program acceptance tests, at least two thirds should be alloted to build-up and checkout of successive "packages" culminating in the entire program. Therefore, a reasonably complete control or "executive" routine, including control of test inputs and recording, should be ready, together with the first nucleus of program units, no later than the end of the first third of this interval.

testing

The checkout of individual program units can usually proceed with a minimum of auxiliaries, largely provided by the unit programmer himself, but once the combination of units has begun, more elaborate tools will be found necessary. Since these take time to make ready, test requirements, as mentioned earlier, must be anticipated. One of these is storage space: test control, test recording, and perhaps some simulation of external system elements must in some degree occupy high-speed storage alongside the program being tested. If the complete program comes too near to filling this storage, thorough and convenient testing will be difficult.

Special Hardware: A system will frequently include certain signals and responses to its central-control device which cannot be simulated with sufficient realism either within the computer or by tape or card inputs. In such cases, special auxiliary hardware containing timing and logical circuits may be essential, at least to the later stages of program testing. External events of a random nature relative to the program cycle, which can cause trapping or changes of program sequence, are likely sources of such a requirement. For early checkout, this additional complication is neither necessary nor desirable; but if it is omitted altogether, system integration will probably uncover embarrassing program faults that could thus have been corrected earlier. Like any other hardware item, this sort of device must be specified early enough for the complete sequence of design, procurement, construction, bench testing, and integrated testing with the computer to be fulfilled before applying it to the system program. Otherwise, there will be needless confusion as to whether program or hardware is misbehaving.

Testing of a real-time program is bound to include recording and other auxiliary functions which are irrelevant to true real-time system operation. Full test realism in a time sense may therefore require an external clock that can be started and stopped by the program test-control routine, so that "time out" can be called to perform non-real-time functions. It is desirable that the computer system clock have this facility.

Input Simulation: Test inputs will undoubtedly be mainly on magnetic tapes. The programs which make these tapes must be versatile enough to vary, conveniently, all significant system parameters. The mechanics of reading the tapes must present their content to the program in a manner as near to system behavior as possible. Since input tapes will be processed separately along with their associated test output by a data-reduction program, they must also carry control and identification for this purpose, distributed through the input items but not fed to the real-time program. Questions of format on these tapes (and in the program) should be kept separable as much as possible. By this means, some testing can be done, if necessary, before all computer interface formats are frozen. Then, when final formats are specified, both the input tapes and the program's interpretation of them can be altered with minimum ramifications. Obviously, it is best to start with the right formats, but one seldom can. Input tapes will have to be verified; special reduction and print-out routines will be needed to do this.

It is fairly obvious that the first input tapes to which a new assembly is subjected should be as simple as is consistent with yielding useful test data. As the more glaring mistakes in the assembly are corrected, input complexity should be stepped up to uncover the more subtle ones. High-load simulations will probably serve little purpose until the last quarter or so of the build-up process.

Test Control and Recording: If a system program were simple enough for all of its internal operation to be inferred from inspection of its normal system output, little test control and no test recording would be necessary. But this is almost never the case. Just as oscilloscopes and probes are necessary to look inside complex circuits, so is it necessary, in order to understand and correct internal details of program operation, to record selected intermediate data at selected times. Unless one can be highly selective about such recording, the volume of it will be overwhelming. To accomplish such selection, a versatile test recording routine is an essential tool. It must permit the test operator to control, as by card input, where he puts the "probe," *i.e.,* what locations are to be recorded, and what is to be used for a "synch pulse," *i.e.,* what conditions must be met in the program to cause recording. It is quite likely that the system data processor, for adequate program testing, may have to be equipped with more magnetic tape units, tape-control channels, or buffering equipment, than it would need for actual system operation. Such input and recording needs must be anticipated as items of test hardware.

Data Reduction: The preceding paragraph points out that selectivity in test recording is essential to avoid being overwhelmed by sheer volume of test output. But it does not guarantee such avoidance. Even a highly-selected record, if simply printed out verbatim, will be staggering; and the task of tediously analyzing it will drag like an anchor on program check-out progress. Condensation, abstraction, and interpretation of this test output by machine are thus indispensable. Programs will be required for the purpose, and they will not be simple. At the least, they must take desired data off the output tape and print it out in easily-legible format. More useful routines will have a degree of built-in "judgment;" they will ignore the routine items on the output tape and print out only what seems significant—*i.e.*, usually, what is wrong. To do this, such a routine must operate not only on the output of a test, but also on the input or some summary thereof. If it is desired to assess program performance on randomized inputs in a monte carlo fashion, a special routine will be needed to generate the resultant statistics.

Acceptance tests: As soon as specifications for a system program are definitive, both system and programming contractors should begin to consider how they will verify the program's meeting of the specifications. In fact, they should have had this in mind to some extent in writing the specifications; for it is easy to write specifications in such terms that conformance is impossible to demonstrate. For example: "The program shall satisfactorily process all input traffic presented to it."

Needless to say, once agreed on, such tests should be fully rehearsed well before their official performance. The unexpected can always happen, and usually does.

administrative monitoring

One of the first administrative measures in developing a real-time system program will be to lay out a schedule with appropriate milestones.

In general, the fewer subtasks set out in the official schedule and the more carefully they are chosen, the less guesswork, fiction, and annoying justification will be called for. Internal schedules for self-monitoring are a different matter; they should have enough detail to be compared with week-to-week progress. Some milestones which must be included in any official schedule are 1) the freezing of specifications, probably in two or three stages of detail, 2) the start of "package" assembly (*i.e.*, the combining of units by the control routine), 3) one or two significant stages of package build-up, 4) start of checkout of the whole program, and 5) performance of acceptance tests. The typical program-development flow chart, Fig. 2, may help to visualize the process and its significant stages.

Budgets of time and storage, as mentioned earlier, should be set up, and monthly or more frequent reports are advisable on how well they are being adhered to.

Programmers differ little from engineers, in general, in their reluctance to stop tinkering with and improving their creations. This is a laudable trait; but as delivery dates approach and time grows short, it has to be restrained. Definitive test versions of the program must be established, and tight control exercised over changes so that all effort can be directed at those which are really necessary to meet specifications.

a few contractual aspects

In developing electronic equipment, managers accept the fact that design changes are expensive after construction has begun. But a computer program, even a real-time system program, is plausibly regarded as little more than a list of instructions written on paper, easy to erase and change. It is certainly true that the program can usually be changed more easily than a piece of equipment can be rebuilt (though even this is not always true). However, it is more accurate to think of the program as resembling a set of interdependent drawings and parts lists, or even as a piece of breadboard equipment; it is, in general, easier to change than production hardware, but late changes can have severe repercussions. If management takes the casual list-on-paper attitude toward a system program, the consequence will be procrastination of complete program specifications, followed by disbelief and consternation when lack of a proper program delays the whole system.

The meeting of program-production schedules, and the holding of costs, must be predicated on not having to make last-minute changes. In other words, specifications must be written unambiguously and all necessary interface data must be spelled out by some conservatively set date. Lacking adequate definition on that date, all parties must be clearly apprised of the potential slippage of end dates.

In any technical development project, it is a commonplace that all changes of specification must be in writing and through channels, with the required number of authorized signatures. This applies no less in system programming, but is harder to enforce, mainly because of the ease with which minor or early changes can be made, and, once made, forgotten. In early stages, while things are fluid, many exceptions can be made; but unless control gets progressively more stringent as time goes on, acrimony is certain to ensue.

The program of a real-time system is of precious little use without an explanatory manual. Normally it will not be operated by the people who wrote it, and circumstances will frequently require trouble shooting and minor changes. Therefore, an accompanying manual (loose-leaf, by all means) must give sufficient explanation of the program's organization and of techniques of modification to enable changes to be made as needed. To contain the requisite technical competence and detail, the writing of such a manual plainly cannot be left to non-programming technical writers. If possible, it should grow with the program. Any uninitiated editor who tries to put such a manual together after the program is complete and its several designers have been scattered among other projects will find the task just about hopeless.

The author is only too well aware that to a number of people experienced in real-time digital systems, many of the foregoing observations will be platitudes. But perhaps even to such old hands, a few of the points will provoke further thought; and a summary of this sort can serve as a broad check list.

If the discussion has given pause to a few intrepid souls about to embark on a real-time system with more enthusiasm than *savoir faire,* its intent will not have been mistaken. Future voyages across these waters are sure to be stimulating and challenging; but mariners will be well advised to know what lies in wait for them and to be equipped for it. ■

ACKNOWLEDGMENT

The observations in this brief paper have been drawn in part from the author's own experience, but even more, indirectly, from many predecessors and colleagues. Names are too numerous to list, but in the first rank are members and former members of the M.I.T. Lincoln Laboratory staff (in part transferred to the MITRE Corp.), who forged an impressive body of tools and doctrine for the SAGE system. It is on their foundation that the rest of us have built. For almost an equal number of technical and administrative lessons, I must thank my associates in Sylvania Electronic Systems, who have made a timely success (moon echoes notwithstanding!) of digital equipment and program in the Ballistic Missile Early Warning System.

NEWS BRIEFS

AIEE-IRE BOARDS O.K. MERGER PRINCIPLES

Merger of the Institute of Radio Engineers and the American Institute of Electrical Engineers moved a step closer recently when the Boards of Directors of the two groups approved the principles of the proposed consolidation.

Constitution, agreement of merger, and principles of consolidation will be submitted to the combined membership of both organizations for approval. If approved by a mail vote this summer, it is expected that the new society will be operating by January 1, 1963.

At a meeting held earlier this year, it was proposed that the merged society might be known as the Institute of Electrical and Electronics Engineers. Presently, the IRE's membership is 97K and AIEE's 70K. Combined assets of the two societies total about 6.5 megabucks.

LEAS NAMED CHAIRMAN OF FALL COMPUTER CONFERENCE

J. Wesley Leas has been named general chairman of the Fall Joint Computer Conference, to be held December 4-6 at the Sheraton Hotel, Philadelphia. Announcement was made by Dr. Willis H. Ware, chairman of the governing board of AFIPS.

Leas is chief engineer, EDP, for Radio Corporation of America, a position he has held since December, 1961. He also acts as an advisor to a Department of Defense agency. In 1955 he served on the Four Member Advisory Group on Computers for the Assistant Secretary of Defense, R & D.

STRETCH AIRLIFTED TO U.K. ATOMIC AGENCY

Two CL 44 cargo planes were used to airlift an IBM 7030 STRETCH to Great Britain, where the system will be delivered to the United Kingdom Atomic Energy Authority. Two other STRETCH systems are used for atomic research: The U.S. AEC operates 7030 systems in laboratories at Los Alamos, N. M., and Livermore, Calif.

MICH. STATE TO INSTALL CDC 3600 NEXT YEAR

Michigan State University will install a CDC 3600 system, with a delivery date set for March, 1963. The system, which was announced at the SJCC, will cost the university $1,387,800. Without educational discount, the CDC 3600 lists for $2,298,000.

Prior to delivery, CDC will install a "smaller" system within two months, on an interim basis. Additionally, 200 hours will be made available by CDC to the university on a larger computer at CDC's Minneapolis headquarters. (For complete CDC 3600 specifications, see page 37.)

REAL-TIME PROCESSOR FROM ITT FEDERAL LABS

The ITT-025 Real-Time Data Processor, a solid-state, parallel, binary computer, has been announced by ITT Federal Laboratories, Nutley, N. J. Although originally designed for message switching, it was stated that the system can be utilized for industrial process control, communications, automatic check-out, reservations, and traffic control.

Main storage contains from one to four modules each with 16K locations of 33 bits each. Magnetic drum storage contains 262K words of 33 bits. Read-write cycle time for main storage is 6 microseconds. Add instruction time is 16 microseconds, and addition time is 3 microseconds.

The ITT-025 can accomodate 32 two-way high-speed data lines (4800 bits per second maximum) and 86 two-way, low-speed data lines (2400 bits per second maximum). While serving real-time demands, the system can continue normal computer problem-solving functions.

Software for the ITT-025 includes a simulator and an assembly system. Price for a configuration including console, central processor, 16K memory, card reader and punch, is reported to be under 1.5 megabucks. Delivery time is from nine to twelve months.

CIRCLE 100 ON READER CARD

UNIVAC NOW A DIVISION OF SPERRY RAND

Announcement of the establishment of Univac as an independent division of the Sperry Rand Corporation was made recently. Previously, Univac was a segment of the Remington Rand Division.

Named to head the Univac Division was Dr. Louis T. Rader. He will report directly to D. L. Bibby, president of the RemRand Group and a Sperry Rand board member. Jay W. Schnackel, general manager of Univac, will become vice president and executive assistant to Bibby.

ARMED FORCES SYMPOSIUM WILL REVIEW MILITARY DP

A joint Symposium on Armed Forces Data Processing will be held on June 5-7, at the Sheraton-Palace Hotel, San Francisco. Representatives of the three services and several major manufacturers have joined in organization and sponsorship.

Purpose of the Symposium is to evaluate the use and benefits of electronic dp in military commands and installations on the West Coast; exchange knowledge on problematic and successful applications; review present availabilities in soft and hardwares; and to develop guidelines for military management in dealing with the processing of management information.

Activities scheduled for the three-day meeting include panel discussions and field trips to military dp installations and manufacturers' showrooms and service centers.

TYPESETTING FROM COMPUTER TRANSLATOR

The output of an experimental Russian translating computer is now being automatically converted into a reproducible English text by use of the Linofilm photocomposition system. Use of Linofilm results in a book quality printout on film or paper suitable for reproduction by offset or letterpress printing.

The language translator computer system produces the necessary signals to control the Linofilm unit through the tape which contains

DERIVING
majority logic
NETWORKS

FUND THM:

$f(X,Y,Z) \equiv (X\#Y\#f_{x\bar{y}})\#(\bar{X}\#\bar{Y}\#f_{x\bar{y}})\#f_{xy}$

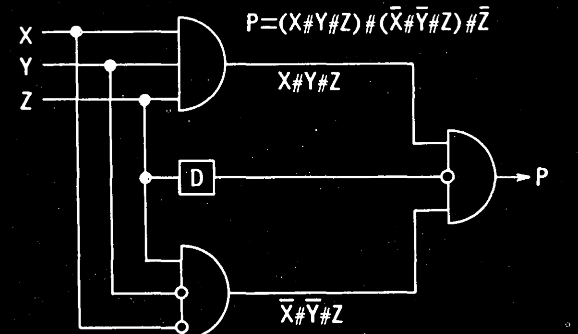
DEFINITIONS:

$X\#Y\#Z \equiv \mathrm{Maj}(X,Y,Z)$; $f_{xy} \equiv f(X,X,Z)$; $f_{x\bar{y}} \equiv f(X,\bar{X},Z)$

DERIVATION:

Let $f(X,Y,Z)$ be even-parity function P.
Then $f_{xy} \equiv \bar{Z}$ and $f_{x\bar{y}} \equiv Z$, so

$P = (X\#Y\#Z)\#(\bar{X}\#\bar{Y}\#Z)\#\bar{Z}$



The fundamental theorem of majority-decision logic, a typical product of Univac's Mathematics and Logic Research Department, has practical as well as theoretical interest. The even-parity checker derived above from the fundamental theorem can be treed to determine the parity of 3^n bits in $2n$ logic levels using only $\frac{3}{2}(3^n - 1)$ three-input majority gates.

Qualified applicants will find at Remington Rand Univac a scientific climate tuned to the intellectual curiosity of the professional man. The opportunity and the incentive for advancement are waiting for you in highly significant positions at Univac. You are invited to investigate them immediately.

■ SYSTEMS ANALYSTS ■ APPLICATIONS ANALYSTS ■ ENGINEER WRITERS ■ LOGICAL DESIGNERS ■ PROGRAMMERS

Contact the office of your choice:

R. K. PATTERSON	**WILLIAM LOWE**
REMINGTON RAND UNIVAC	REMINGTON RAND UNIVAC
Univac Park	P.O. Box 6068
St. Paul 16, Minnesota	San Diego 6, California

R E M I N G T O N R A N D

UNIVAC

DIVISION OF SPERRY RAND CORPORATION

There are also immediate openings in all areas of digital computer development at our other laboratories. Inquiries should be addressed to:

T. M. McCABE	**D. CLAVELOUX**
Rem. Rand Univac	Rem. Rand Univac
P.O. Box 500	Wilson Avenue
Blue Bell, Penn.	So. Norwalk, Conn.

(An equal opportunities employer)

COMPUTER PROGRAMMERS
(with B.S. plus experience)

DOUGLAS Missile and Space Systems Division

offers you outstanding career opportunities in the following fields:

Engineering Analysis
Systems Analysis
Programming Research
Standards

Please forward resume to F. V. Edmonds, Chief, Engineering Personnel Section

DOUGLAS AIRCRAFT COMPANY

3000 Ocean Park Boulevard
Santa Monica, California

CIRCLE 75 ON READER CARD

COMPUTER ENGINEERS
LOGIC DESIGNERS
CORE MEMORY SPECIALISTS

Collins Radio Company has immediate openings for experienced digital computer design engineers at its plant in Cedar Rapids, Iowa. New programs in digital data systems offer outstanding opportunities for growth and development with a leader in the electronics field.

Recently announced development plans call for graduate engineers experienced in

Computer Systems	Memory Systems
Logic Design	Magnetic Tape Handlers

Qualified applicants interested in a career with a future, send your resume to:

L. R. Nuss, Manager
Professional Employment

COLLINS RADIO COMPANY
Cedar Rapids, Iowa

COLLINS

An equal opportunity employer

CIRCLE 76 ON READER CARD

coding specifying case, character width, type face and size, line length and punctuation.

NEW TRW-340 FEATURES MEMORY EXPANDABILITY

Thompson Ramo Wooldridge recently announced the TRW-340 which features core memory expandable from 4K to 16K words and drum memory expandable from 8K to more than 112K words. Speed was stated to be 20K ops/sec. Reduction of operating time is said to be achieved through parallel operation and special off-line commands.

The TRW-340 is compatible with all optional equipment, including software, which is available with the TRW-330. The latter can be field-modified to a 340 system by adding the core processor.

Almost unlimited expansion of the number of digital and analog I/Os is said to be possible with the 340.

CIRCLE 101 ON READER CARD

DATA TRANSMISSION OVER THE MOUNTAIN

Low-power microwave transmission of data over the horizon at high speeds without using relay stations has been reported by IBM, San Jose, Calif. In recent experiments, computer data was transmitted over a mountain at speeds of 500K bits/second, with power as low as 16 watts, using small antennas.

The experiments, being conducted by IBM's Advanced Systems Division, are based on a technique called "knife-edge diffraction," which uses the narrow ridges of a mountain range to deflect radio signals. The experimental link is operating between a Monterey transmitter and a San Jose receiver, 45 miles away, both aimed directly at the 3,800 ft. Loma Prieta Ridge in the Santa Cruz Mountains.

CIRCLE 102 ON READER CARD

● The Ordnance Tank-Automotive Command, Detroit, will install an RCA 501/301 configuration which will replace its RCA Bizmac 1 system, in operation since 1951. The system will control inventory and distribution of automotive repair parts at 10 depots. Rental of the equipment will average about one megabuck yearly.

CIRCLE 103 ON READER CARD

● A SPEDAC 220 Digital Differential Analyzer (DDA) Computer has been ordered by the U. S. Army's White Sands Missile Range Flight Simulation Laboratory. The system, made by the Hazeltine Corp., Little Neck, N. Y., will be used to determine flight reactions of various missiles.

CIRCLE 104 ON READER CARD

● The Daystrom memory which replaced the original CRT unit in the Naval Ordnance Research Computer (NORC) in March, 1960, has been instrumental in establishing a down time to total operating time ratio of better than 0.1% during the past six months. A recent report states that for a total operating time of 12,407 hours for the period March 1960 to August 1961, mean time between failures attributed to memory was better than 1770 hours. During the same period, a ratio of 0.3% was recorded.

CIRCLE 105 ON READER CARD

● The first Collins C-8000 Communications Switching System, made by Collins Radio Co., Dallas, Texas, has been ordered by Aeronautical Radio, Inc. (ARINC) Cost of the system was reported to be more than 2 megabucks.

CIRCLE 106 ON READER CARD

● Honeywell's EDP Division has established its first overseas Service Bureau in London. A Honeywell 800, recently shipped by air from Boston, will be available for British customers in the London center. The Service Bureau will also function as an education and demonstration center.

● State Farm Mutual will soon put into operation a decentralized dp system, involving a total of 38 IBM 1401-1410s. The system, with both disk and tape storage, will be installed in each of the auto insurance company's regional offices. A 1410 has also been ordered for the home office in Chicago.

● Battelle Memorial Institute, Columbus, Ohio, has installed a Bendix G-20. A special 650 simulator, developed by Battelle for Bendix, made it possible for Battelle scientists to transfer computing problems from other equipment to the G-20 in one day.

CIRCLE 107 ON READER CARD

● The newest computer users' group, SWAP, held its first meeting recently. Composed of users of the Control Data 160 and 160A, 38 delegates representing 25 separate installations attended the meeting, held at the U S. Naval Postgraduate School, Monterey, Calif. Keith Johnson, Data Management, Inc., Minneapolis, was elected president of the group.

NEW LITERATURE

PERT PORTFOLIO: An information kit called PERTFOLIO highlights the PERT System which provides data regarding time, costs, performance/reliability of military and industrial programs. OPERATIONS RESEARCH INC., 225 Santa Monica Blvd., Santa Monica, Calif. For copy:
CIRCLE 130 ON READER CARD

G-20 COBOL: A new programming support bulletin outlines the general features of the COBOL offered with the G-20. BENDIX CORP., COMPUTER DIV., 5630 Arbor Vitae St., Los Angeles 45, Calif., For copy:
CIRCLE 131 ON READER CARD

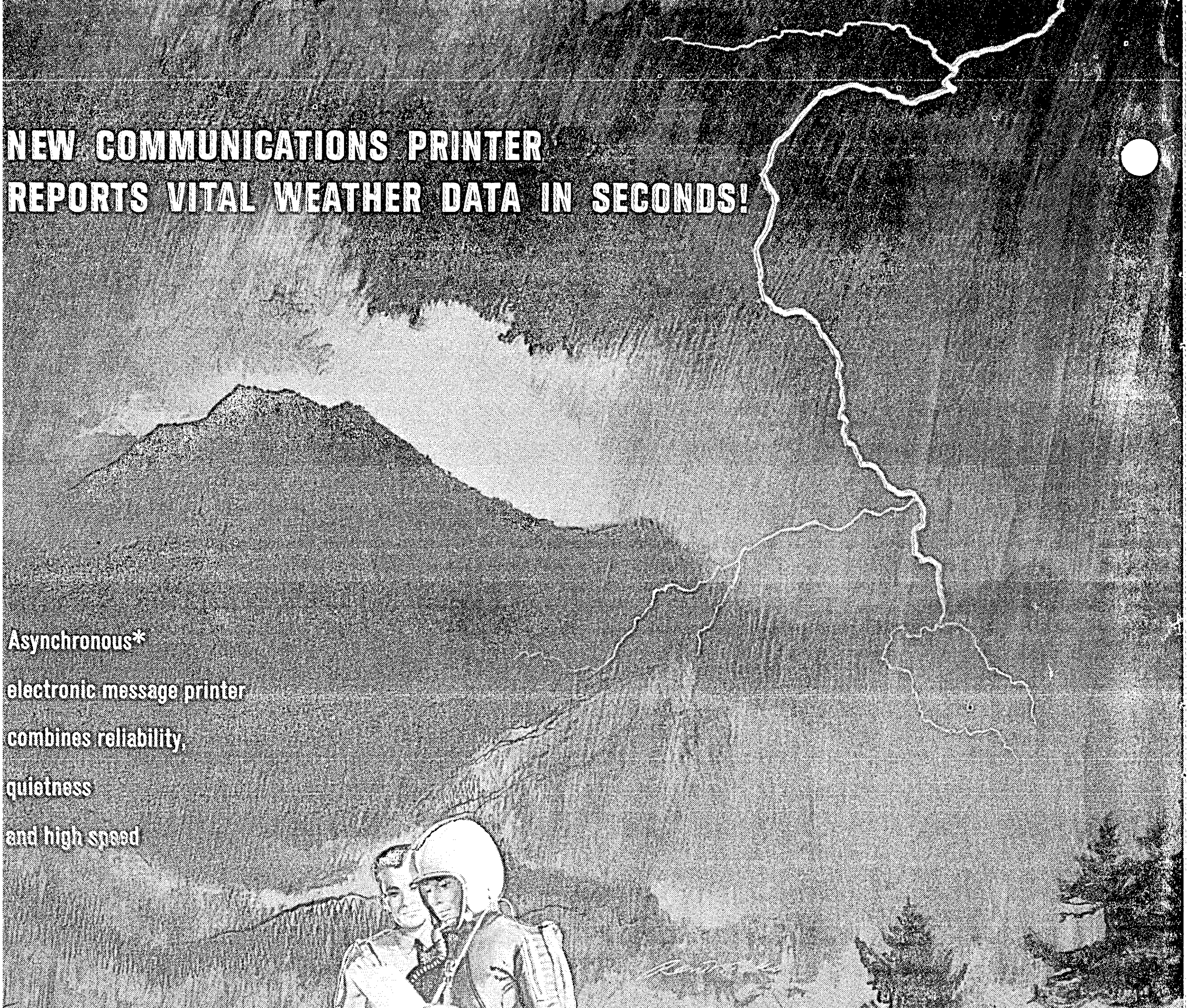
DIGITAL DATA PROCESSOR: This booklet highlights the DDP-19, designed for real time engineering applications, data acquisition and reduction, and scientific problem solving. Features, operational characteristics, options and a command list are included. COMPUTER CONTROL CO., INC., 983 Concord St., Framingham, Mass., For copy:
CIRCLE 132 ON READER CARD

BANK AUTOMATION: This 18 page booklet lists management services offered, features of automation and a step by step description of the automation process. MCDONNELL AUTOMATION CENTER, Lambert-St. Louis Municipal Airport, Box 516, St. Louis, Mo. For copy:
CIRCLE 133 ON READER CARD

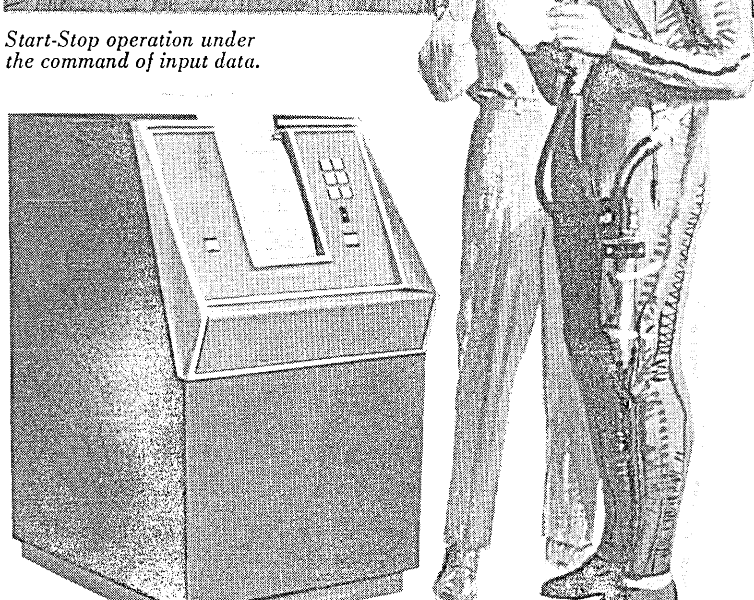
A THIRD SURVEY OF DOMESTIC ELECTRONIC COMPUTER SYSTEMS: This report presents information on 16 engineering and programming characteristics of 222 computing systems. Also included are comparative charts, analysis of the survey data, discussion of trends, bibliography and glossary. For a copy of this survey send $10 to U. S. GOVERNMENT PRINTING OFFICE, Superintendent of Documents, Washington 25, D. C.

DIGITAL COMPUTER SYSTEM: Information on the memory, speed, instruction system and commands, automatic priority interrupt, console, operation and peripheral equipment of the AD/ECS-37 is presented in this pamphlet. Systems applications are also included. GENERAL MILLS, ELECTRONICS GROUP, 1620 Central Ave., Minneapolis, Minn. For copy:
CIRCLE 134 ON READER CARD

DATA TRANSMISSION SYSTEMS: This



Start-Stop operation under the command of input data.



The S-C 3070 puts current preflight weather data in the hands of pilots faster than ever before! The printer utilizes an electrostatic process to produce highly legible, permanent copy. The S-C 3070 is designed to operate at speeds up to 3,000 words per minute using standard computer or communications codes over telephone, telegraph and microwave links. ■ Compact dimensions and quiet operation make the S-C 3070 ideal for communications or command centers. Multiple copies of S-C 3070 output can be easily obtained by using the original as a litho offset master or by standard office copying methods. ■ Reliable, unattended operation in the S-C 3070 results from the unit's non-impact printing concept and field-proven electronic circuitry. Replacement paper rolls can be loaded into the S-C 3070 without interfering with message transmission. ■ For additional information on the S-C 3070, write to Dept. C-39 General Dynamics | Electronics, P. O. Box 2449, San Diego 12, Calif.

GENERAL DYNAMICS | ELECTRONICS GD SAN DIEGO

CIRCLE 28 ON READER CARD

brochure gives information on tape punch consoles for receivers, recorders and computer outputs as well as tape reader consoles for transmitters, inputs and instrumentation sequencers. A price list is also included. SOROBAN ENGINEERING, INC., P. O. Box 1717, Melbourne, Fla. For copy:
CIRCLE 135 ON READER CARD

INFORMATION SYSTEM: This 16-page booklet describes the 750 which is a process-oriented data system of solid state design. System functions consist of data gathering, alarm monitoring, trend records and displays, logging, measuring arithmetic computations, and digital readout. Information on how the system works, features and function selection is given. BAILEY METER CO., 1050 Ivanhoe Rd., Cleveland, Ohio, For copy:
CIRCLE 136 ON READER CARD

RECOMP: This illustrated booklet gives information on card equipment capability, x-y graph plotter, programs, the RECOMP II and III, FACITAPE, VERSATAPE and the magnetic tape memory. Features and performance are highlighted. AUTONETICS INDUSTRIAL PRODUCTS, 3400 E. 70th St., Long Beach, Calif. For copy:
CIRCLE 137 ON READER CARD

SERVICES AND FACILITIES: A 12-page booklet highlights this computer center which rents the 704 and necessary peripheral and auxiliary equipment. The center also provides personnel assistance. Prices are included. LITTON COMPUTER CENTER, 5500 Canoga Ave., Woodland Hills, Calif., For copy:
CIRCLE 138 ON READER CARD

SELECTED DATA PAGE SCANNER: This pamphlet highlights an optical scanning machine which can select and read specified data from a business document and convert the information into business machine language for computer processing. FARRINGTON ELECTRONICS INC., 7019 Edsall Rd., Alexandria, Va., For copy:
CIRCLE 139 ON READER CARD

DIGITAL SERVOS: This illustrated booklet surveys the application of digital techniques to a 400-cycle carrier analog servo system, and includes topics in stability, analysis, operation, error considerations of a digital position servo and applications. DIGITAL SERVO CORP., 13425 Wyandotte Ave., N. Hollywood, Calif., For copy:
CIRCLE 140 ON READER CARD

AT THE DROP OF A DECK...

$$f=3wb^2/4t^2(1+1.61b^3/a^3)$$

WIZ and the GE-225 computer solve this problem less than six milliseconds after data is read in.

The program reads WIZ language statement cards and data cards once and immediately and continuously produces a completed GE-225 program. It compiles 500 to 800 machine instructions per minute in one pass, requires no magnetic tape and as little as 8000 words of memory.

No professional programming is needed, since the WIZ language consists of familiar algebraic terminology. Between breakfast and lunch, any engineer or mathematician can learn to write his own programs.

A GE-225, on which you can use WIZ, leases for as little as $3,275 per month. For this low cost, you can have at your fingertips a versatile information processing system with an 18 microsecond memory, and an algebraic compiler that is fast, accurate, and truly easy to use.

To see WIZ in action, contact your nearest General Electric Computer Department office. Or write for Bulletin CPB 217, General Electric Computer Department, Section 12-15, Phoenix, Arizona.

Progress Is Our Most Important Product

GENERAL ELECTRIC

A New Generation of Low Cost Computers

SDS 900 Series of high-speed, solid state, general-purpose digital computers are in production. First deliveries will be made in autumn. Designed with the user in mind, they are single address, random access core memory machines, intended for general-purpose scientific computation and special-purpose systems integration. Programming is simplified. Input/output is buffered and high speed. Computation rates are comparable to that of large-scale computers. SDS 900 Series computers are *symbolically homogeneous*—the programs from either machine can be run on the other. They are unusually reliable, with ferrite core memories, all-silicon semiconductors, and circuitry based on worst case analysis. Compare the following characteristics:

$89,000—Model 920

The 920 is an extremely fast, general purpose computer for scientific use. Its command structure includes built-in Floating Point and Multi-Precision instructions. In speed, characteristics, and working flexibility, it surpasses larger, more costly first generation solid state machines. When carefully compared on all of its operating parameters, the 920 clearly offers more general purpose scientific computing-per-dollar than currently available machines.

Memory & Speed The 920's basic core memory of 4,096 words is expandable to 16,384 words. Typical execution times for 24-bit operands, *including both memory access and indexing,* are: Add . . . 16 μsec. Multiply . . . 32 μsec. Floating point operations (24-bit mantissa plus 9-bit exponent) —Add . . . 192 μsec., Multiply . . . 184 μsec.; (39-bit mantissa plus 9-bit exponent)—Add . . . 368 μsec., Multiply . . . 272 μsec.

Standard Equipment All SDS 920 computers are delivered complete with 300 character/second paper tape reader, 60 character/second paper tape punch, input/output typewriter, and manual control and display of all registers. SDS magnetic tape units, converters, and other I/O devices are available as optional equipment.

Common Characteristics

Memory Characteristics

SDS 900 Series computer words contain 24 binary bits. An additional parity bit allows parity checking of all memory and input/output operations. Special logic makes memory non-volatile with power failure.

Input/Output Characteristics

SDS computers incorporate five separate input/output systems. One of these, a buffered input/output, allows data transfer at rates in excess of 120,000 characters/second. A priority interrupt system provides two standard plus 1024 optional channels. In addition to standard input/output devices, all SDS computers communicate directly with: IBM-compatible magnetic tape units, A-D converters, IBM 7090 computers, other SDS machines, and an unlimited range of additional input/output devices.

Programming Characteristics

SDS single address instructions include both an Index Register and an Indirect Address bit. *Programmed Operator* instructions, an exclusive SDS feature, permit complete interchangeability of 910 and 920 programs. FORTRAN II with magnetic tape statements and a symbolic assembler are included in a complete SDS 900 series software package.

Write today for new SDS 900 Series Brochure

SDS

SCIENTIFIC DATA SYSTEMS

1542 FIFTEENTH ST., SANTA MONICA, CALIF.

$41,000—Model 910

The 910 is the first random access, buffered input/output digital computer to be priced below $90,000. Although designed primarily for systems use, its high speed, working flexibility, and excellent performance allow it to be used as an extremely low cost general purpose machine. The 910 operates directly, without special coupling, with all types of input/output devices, including magnetic tape units, A-D converters, automatic typewriters and line printers.

Memory & Speed The 910's basic core memory of 2,048 words is expandable to 16,384 words. Typical execution times for 24-bit operands, *including both memory access and indexing,* are: Add . . . 16 μsec. Multiply . . . 248 μsec. Floating Point operations (24-bit mantissa plus 9-bit exponent) Add . . . 640 μsec., Multiply . . . 656 μsec.; (39-bit mantissa plus 9-bit exponent)—Add . . . 1,984 μsec., Multiply . . . 2,040 μsec.

Standard Equipment All SDS 910 computers are delivered complete with a 300 character/second paper tape reader and manual control and display of all registers. SDS magnetic tape units, converters, 60 character/second paper tape punch, automatic typewriter, and other I/O devices are available as optional equipment.

P. S. Computape doesn't really talk, of course. But in a computer, Computape *reliability* will deliver its own message. New COMPUTAPE, the premium quality computer and instrumentation tape, is the product of the only company devoted exclusively to the manufacture of quality tapes for data processing and instrumentation. *Investigate new Computape today. Better still, immediately.*

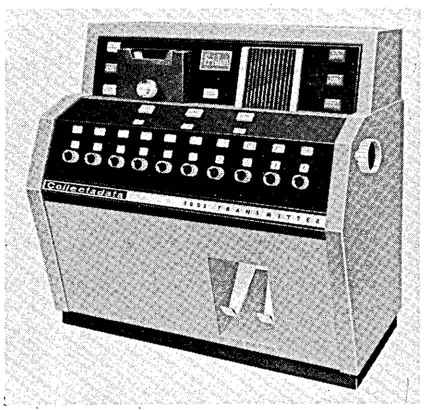
COMPUTRON INC.
122 Calvary Street, Waltham, Massachusetts

CIRCLE 31 ON READER CARD

NEW PRODUCTS

collectadata 30

This data collection system of transmitters and receivers automatically channels data on work transactions to a central location where it is converted into usable information. The system features several controls and checks which, in addition to preventing malfunctions, also indicates where



the malfunction, if any, has occurred so that corrections may be made.

The Collectadata 30 also performs such functions as recording employee attendance and on-job time and is able to distribute line transmission time among transmitters in proportion to their individual traffic leads. FRIDEN, INC., PROMOTION PLANNING DEPT., 97 Humboldt St., Rochester 2, N. Y. For information:

CIRCLE 200 ON READER CARD

data logging

The DDL-101 data logging system can automatically print data from up to 15 sources. Inputs are scanned and printed at a maximum rate of three each second with provision for either internal or external control. Each input accepts up to 10 bits of binary information and the systems can be modified so that it will be able to log up to 255 input quantities. DIGINAMICS CORP., 2525 East Franklin Ave., Minneapolis 6, Minn. For information:

CIRCLE 201 ON READER CARD

analog to digital converter

This solid state analog to digital converter contains no moving parts and will operate from three wire or four wire synchro data, converting the represented shaft position into subdivisions of a circle in binary form. Units at the 10 bit level are presently being tested. DAYSTROM, INC., TRANSICOL DIV., Worcester, Pa. For information:

CIRCLE 202 ON READER CARD

document sorter

The 403 is able to read and sort 1,620 checks per minute and can handle intermixed documents of varying sizes, thicknesses and weights. The sorter will incorporate a new, high-speed transport and a new reading mechanism which will make it possible for a bank to sort checks over 30 times faster than by manual methods. The machine costs $90,000. THE NATIONAL CASH REGISTER CO., Public Relations Office, Dayton 9, Ohio For information:

CIRCLE 203 ON READER CARD

30 inch plotter

The 563 x-y plotter provides for computer-controlled plots up to 29½ inches wide on 30 inch paper, and of any length from usual flat-bed size up to 120 feet on continuous-feed from the standard paper roll supplied for use with the plotter. The 563 can perform 2000 steps per second operation in step increments of 1/100 inch. CALIFORNIA COMPUTER PRODUCTS, INC., 8714 E. Cleta St., Downey, Calif. For information:

CIRCLE 204 ON READER CARD

data conversion system

This new system utilizes a computer-printer tied in with a spectrograph and teletype equipment to permit close analytical control on heats of carbon and alloy steels. The system makes it possible to prevent heats being held overlong in the furnaces or from being downgraded because of incorrect analysis. BETHLEHEM STEEL CO., Bethlehem, Pa. For information:

CIRCLE 205 ON READER CARD

decade decoder

The decade decoder board may be used to convert from binary coded decimal to decimal information and may be driven by a decade counter or decade storage register. The outputs from the 10 AND inverters are logical "O's" (-6 volt level) when the corresponding decimal digit (0-9) is reached. Dual OR inverters may also be provided when logical "1's" are desired as outputs. ELECTRONICS MODULES CORP., 1949 Greenspring Drive, Timonium, Md. For information:

CIRCLE 206 ON READER CARD

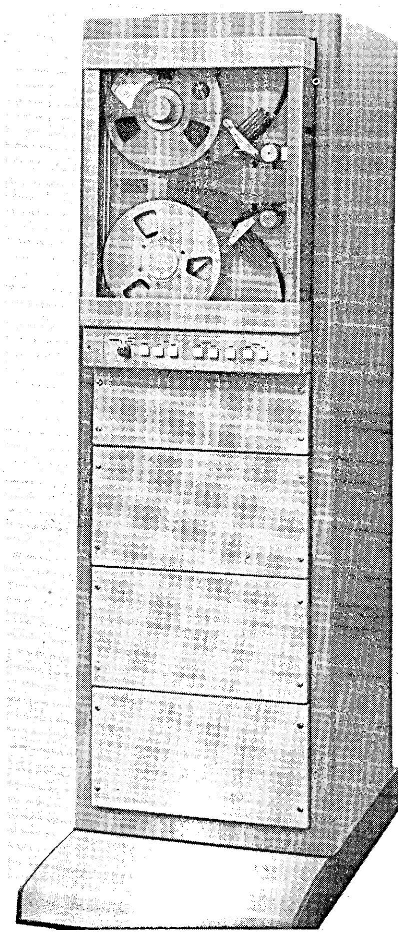
microplanar transistors

The 2N 2368 and 2N 2369 combine the Planar process with epitaxial deposition in an interdigitated geometry with metalized contacts over the oxide surface for ultra-high speed, high current switching for computer logic, applications. FAIRCHILD SEMICONDUCTOR, 545 Whisman Rd., Mountain View, Calif. For information:

CIRCLE 207 ON READER CARD

digital tape handler

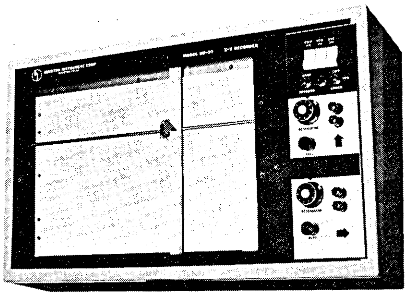
The TM-4 is a modernized version of the FR-400 which features the addition of a vacuum chamber high speed buffer storage. The TM-4 is compatible with all commonly used



recording systems and can be utilized for both high and low density recording. AMPEX CORP., 934 Charter Street, Redwood City, Calif. For information:
CIRCLE 208 ON READER CARD

x-y plotter

This new plotter, model HR-97, offers vacuum paper hold-down, zener references, and over 600 in./sec.^{2} acceleration. Maximum sensitivity of 1



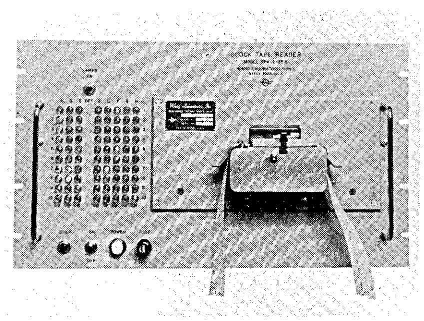
mv/in. can be readjusted with a continuously variable attenuator full scale calibration. HOUSTON INSTRUMENT CORP., P. O. 22234, Houston 27, Texas. For information:
CIRCLE 209 ON READER CARD

paper tape recorder/reader

A high-speed paper tape recorder/reader, model 5903A, records at a rate of 300 characters per second and reads out at a rate of 10 characters per second. The Tele-Buffer, as it is called, uses an electrostatic charge-deposition technique to record the coded data as permanent visible dots. TELE-DYNAMICS DIV., AMERICAN BOSCH ARMA CORP., 5000 Parkside Ave., Philadelphia 31, Pa. For information:
CIRCLE 210 ON READER CARD

punched tape block reader

This reader is now being offered in a form for mounting in a standard 19" panel with verifying lamps designed to read all the holes of the



particular block size of the reader. Standard block sizes from six to 32 lines are available. WANG LABORATORIES, INC., 12 Huron Dr., Natick, Mass. For information:
CIRCLE 211 ON READER CARD

memory plane

Type BIP 1001 is a new high density thin film memory plane which has a 3072 bit capacity. This five mc thin film plane has a cycle time of .2 microseconds and can be driven by single polarity pulses for information entry and readout. BURROUGHS CORP., ELECTRONIC COMPONENTS DIV., Plainfield, N. J. For information:
CIRCLE 212 ON READER CARD

data generator

This general purpose digital test instrument, model 200, provides simulated serial data, serial words, or pulse programs in one or two channels, at clock rates to two mc. The basic instrument controls timing and coding of output signals, operating as a single channel generator with any selected cycle length up to 100 bits or as a two channel unit with coding provided for any cycle length up to 50 bits. DATA-PULSE, INC., 509 Hindry Ave., Inglewood 1, Calif. For information:
CIRCLE 213 ON READER CARD

plotting boards

A new line of plotting boards, series MEC 4000, consists of 10 configurations capable of plotting analog or digital data up to 50 ips with an accuracy of .05% on a 30" x 30" plotting surface. The MEC 4000 series x-y recorders can accept either parallel or serial data directly from punched tape, keyboard, digital computer, punched cards or may be remotely

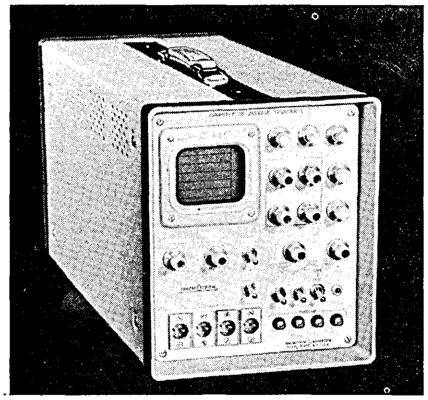
operated by means of a voice channel. MILGO ELECTRONIC CORP., 7620 N. W. 36th Ave., Miami, Fla. For information:
CIRCLE 214 ON READER CARD

programming device
The Drexamatic card reader is a static memory in which all information on a punched card is presented simultaneously in the form of switch closures. Specifications include standard Rem-Rand card, 540 holes, matrix 12 x 45. DREXEL DYNAMICS, Maple Ave., Horsham, Pa. For information:
CIRCLE 215 ON READER CARD

business form
A special form, the "Computer Time Log," has been developed for recording every operation performed on a computer. The form may also be used to schedule machine time or job routing. These forms may be obtained free by writing to AUTOGRAPHIC BUSINESS FORMS, INC., 45 E. Wesley St., So. Hackensack, N. J. For Copy:
CIRCLE 216 ON READER CARD

computer multiplier
Based on the quarter square principal, this analog multiplier, model 500A, can handle over 100,000 products per second. The device accepts two input voltages and produces a single output voltage. It employs direct, coupled, low drift chopper stabilized amplifiers and has a solution time of about eight microseconds. INTECTRON, INC., 2300 Washington St., Newton Lower Falls, Mass. For information:
CIRCLE 217 ON READER CARD

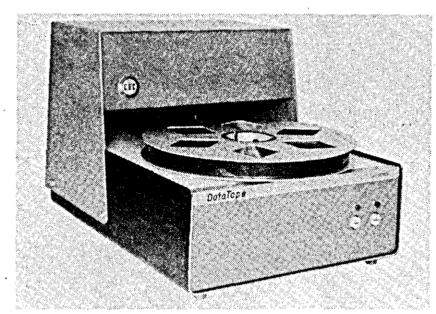
portable computer
This portable, multi-purpose digital computer, the CAT 400 (Computer of Average Transients), is able to average four different variables simultaneously and can perform such func-



tions as analog to digital conversion, recording fast wave forms, plotting of digital data, statistical distribution of analog and events and function generation. MNEMOTRON CORP., 45 S. Mail St., Pearl River, N. Y. For information:
CIRCLE 218 ON READER CARD

data processor
The 025 solid state data processor can receive and transmit at speeds from 75 to 4800 bits per second over telephone circuits. The 025 can simultaneously receive, process and transmit messages from a large number of communication lines. These rates range from the 100-word-per-minute standard teletype to 6000-word-per-minute data transmission. INTERNATIONAL TELEPHONE AND TELEGRAPH CORP., 320 Park Ave., New York 22, N. Y. For information:
CIRCLE 219 ON READER CARD

tape degausser
This automatic tape degausser can erase audio, video and instrumentation tape on reels from three to 14 inches in diameter. A one inch reel of tape



can be erased to a nominal 90 db below saturation level. CONSOLIDATED ELECTRODYNAMICS CORP., 360 Sierra Madre Villa, Pasadena, Calif. For information:
CIRCLE 220 ON READER CARD

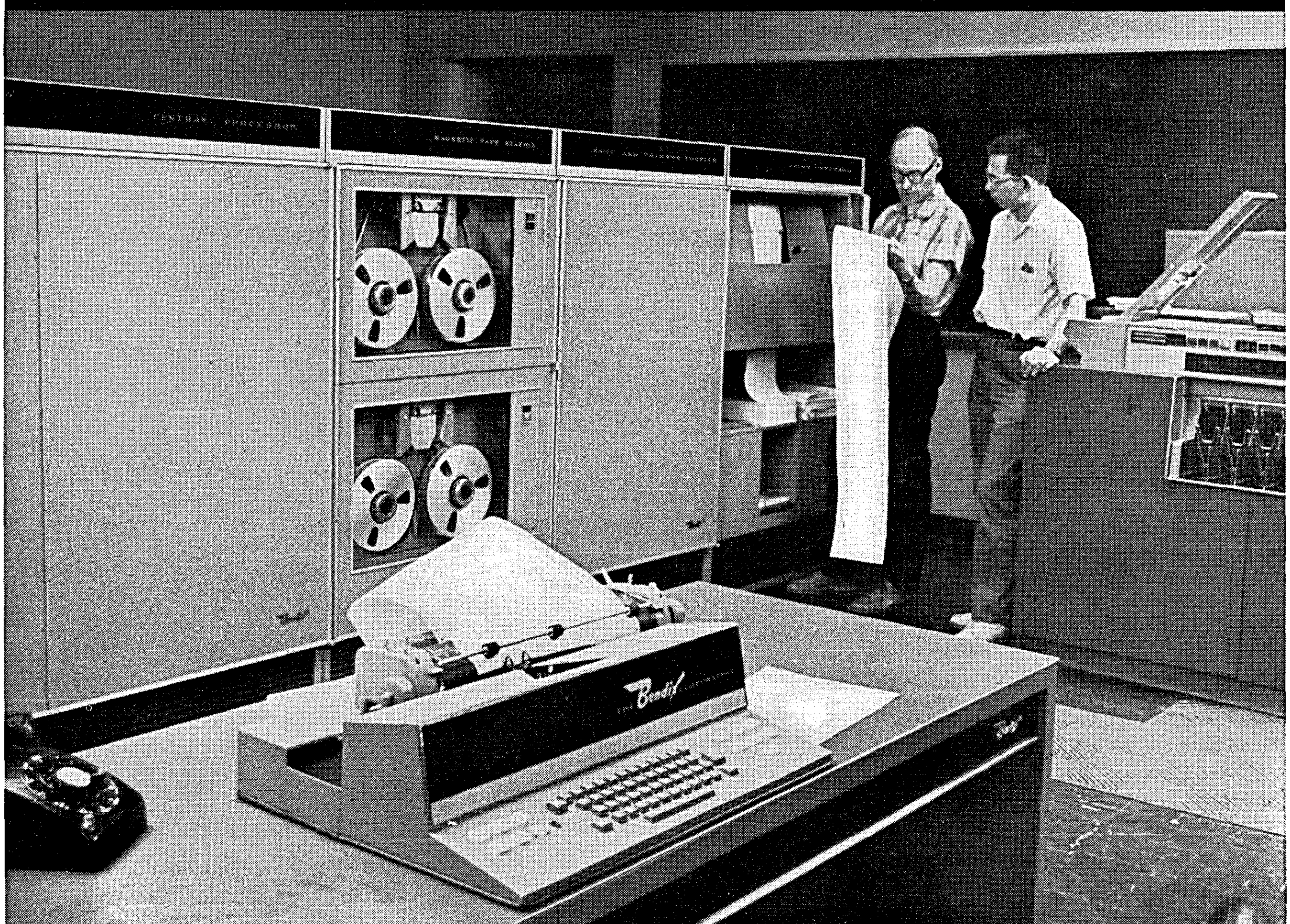
SYSTEMS ENGINEERED

Blending a powerful, high-speed central processor with a uniquely flexible communications system, the Bendix G-20 is systems engineered for more scientific management control...maximum productivity per dollar invested. ■ The self-organizing, self-monitoring capabilities of the G-20—achieved under executive programmed control—permit dynamic re-scheduling to meet the swift-paced demands of modern management decision making. Multiprocessing—the concurrent handling of business and scientific programs—becomes a practical reality with the Bendix G-20 computer system. ■ Thanks to complete automatic control of memory allocation and designation of multiple communications channels and input-output accessories, the G-20 represents the most effective operational configuration for every kind of computational workload. The result: the elimination of piecemeal data processing...a truly balanced system, without sacrificing speed, as reflected in the G-20's magnetic tape transfer rate of 240,000 digits per second. ■ And don't overlook the nationwide support provided by Bendix—systems support in depth...from preliminary evaluation through systems analysis, automatic programming and installation to maximum "uptime" performance. Your nearby Bendix Computer representative will be glad to introduce you to the cost reducing capabilities of the proven, systems engineered Bendix G-20. Or write, Bendix Computer Division, 5630 Arbor Vitae Street, Los Angeles 45, California. Dept. E-40.

Bendix Computer Division

THE Bendix CORPORATION

THE BENDIX G-20 COMPUTING SYSTEM



NOW IN OPERATION—Carnegie Institute of Technology, Pittsburgh, Pennsylvania

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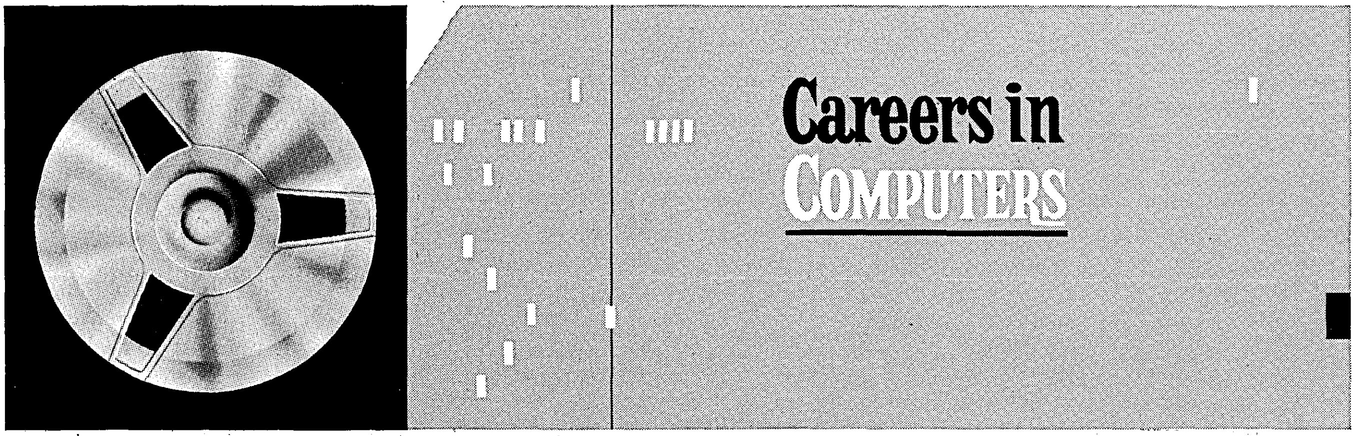
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What is your program for professional growth?

To the programmer in IBM's Systems Development Department, total systems development offers unique opportunities to grow with the programming field. Systems Programmers participate in the development of new techniques and explore new applications of information processing. They have opportunities to progress into broader areas of analysis and design required to provide advanced systems for challenging new projects.

IBM's Systems Development Department is in the forefront of the development of new systems for government applications in military, civil agency and space programs. In the field of programming, this advanced professional staff has excellent assignments open in:

Analysis of Systems Programming Requirements
Programming Techniques Development
Real-Time Operational Programming
Simulation Programming and Evaluation

Among the immediate programming assignments are such tasks as:

Data Reduction	**Numerical Analysis**
Decision Programming	**Problem-Oriented Language Processors**
Information Retrieval	**Sound Recognition**
Logistic Simulation	**Trajectory Prediction**
Message Switching	**Other Related Projects**

These are opportunities for both personal and professional growth. In addition to educational and benefit programs, IBM salaries are commensurate with ability and merit. Relocation expenses are paid. Locations are in Washington, D. C., and Omaha, Nebraska.

The qualifications desired are dependent on assignment and range from one to two or more years' experience in programming large-scale computer systems. IBM is an Equal Opportunity Employer. Qualified applicants are invited to send resumes to: **John V. Croker, Dept. 701R, IBM Systems Development Department, 7220 Wisconsin Ave., Bethesda 14, Maryland.**

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INTERNATIONAL BUSINESS MACHINES CORPORATION

In addition to Washington, D.C., and Omaha, Nebraska, programming facilities are located in San Jose, California; Lexington, Kentucky; Rochester, Minnesota; and New York City, Endicott, Kingston, Owego, Poughkeepsie and Yorktown Heights, N. Y.

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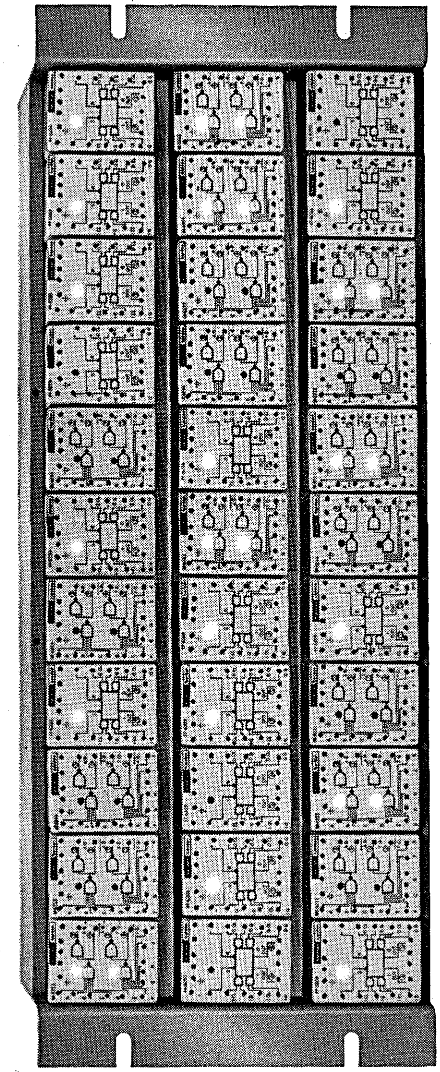

NEW! FACILOGIC BY H-K
FOR DIGITAL SYSTEMS BREADBOARDING

Facilog modules provide a new simplified system for breadboarding, building specialized test equipment and training personnel...easily, sensibly and economically.
Facilog offers: BUILT-IN INDICATOR LIGHTS show "logical state of circuit" ■ FRONT AND BACK PLUG CONNECTIONS Use front for breadboard and checkout...rear for semi-permanent wiring ■ "NO-MAZE" WIRING with modular construction ■ MIL SPEC SYMBOLS and simplified loading rules on front of each module. And 14 more exclusive features. Breadboard and checkout with FACILOG. Specify your system with H-K Encapsulated Logic Modules on FLEXI-CARD Assemblies.

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CIRCLE 39 ON READER CARD

NEW FIRMS
mergers in DP

A new firm, Data Systems Devices of Boston, Inc., has been formed to produce high-speed printing devices and other peripheral equipment. The firm's initial product, reports Michael L. Robins, chairman of the company, will be a printer capable of speeds up to 1K per minute with a skip rate of no less than 50 inches per second.

CIRCLE 108 ON READER CARD

A Teleproducts Group has been formed by Atlantic Research Corp., Alexandria, Va., which will develop and produce Atlantic's telegraph and data communications equipment. Heading the group will be George C. Pierce. Frank D. Baxter was named chief of production and production engineering.

CIRCLE 109 ON READER CARD

The Adcom Corp., Chatsworth, Calif., has started manufacturing operations. The firm, headed by Joseph M. Looney, Jr., will specialize in analog-to-digital conversion and digital communications techniques, as well as high density digital data transmission and recording devices.

CIRCLE 110 ON READER CARD

Decision Systems, Inc., is a new firm in Silver Springs, Md. The company will provide services in the areas of system analysis, programming, and special digital equipment development. President of the firm is Richard R. Martin, formerly with IBM.

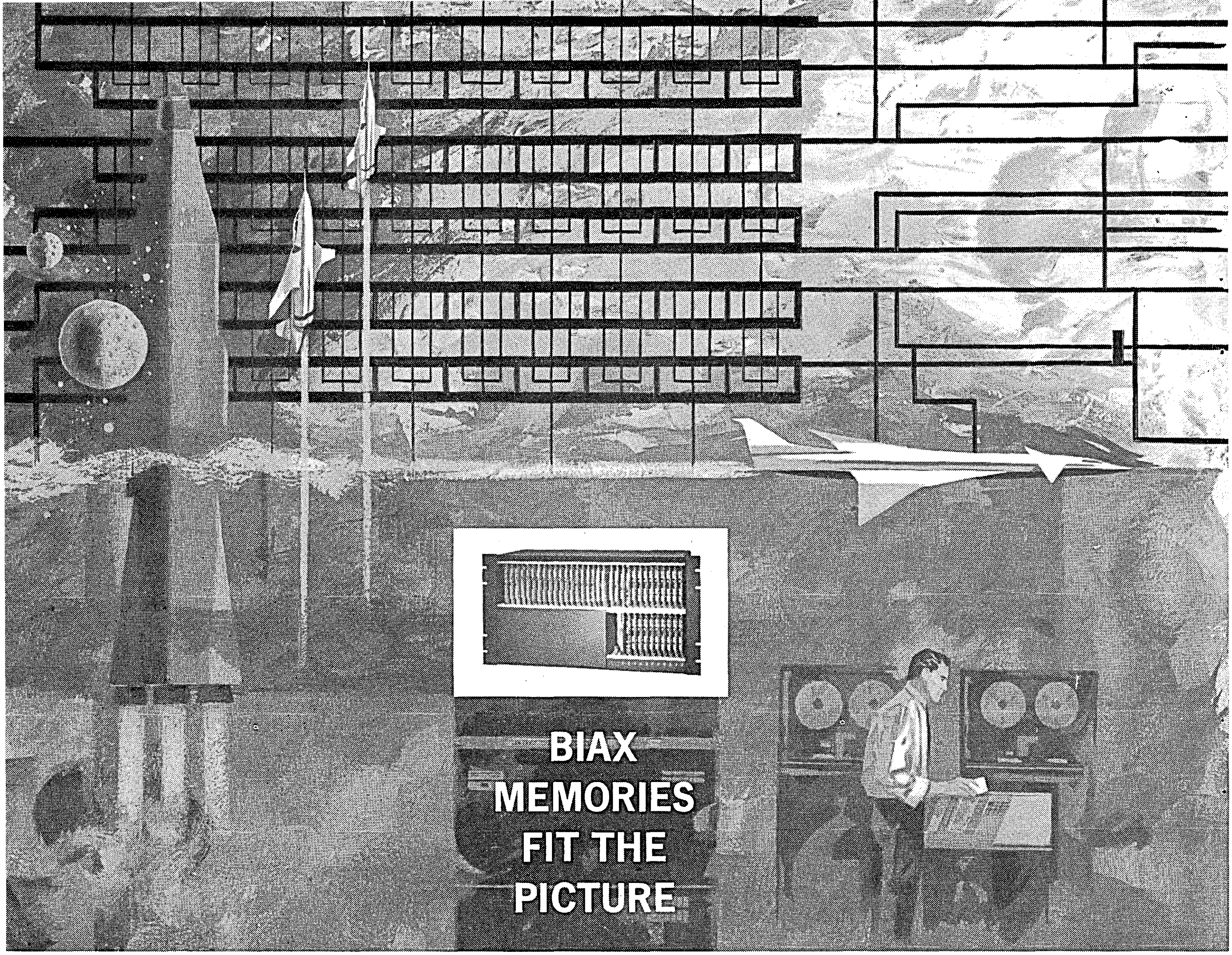
CIRCLE 111 ON READER CARD

Linder C. Hobbs has formed his own consulting firm, to be known as Hobbs Associates, of Corona del Mar, Calif. Formerly with Aeronutronic, div. of Ford Motor Co., the new firm will develop and design digital systems and aid in proposal writing, systems review and design evaluation.

CIRCLE 112 ON READER CARD

M.K.S. Data is a new electronic firm in El Cajon, Calif., and will repackage, reduce in size, and produce special circuits in standard printed circuits or welded construction. According to William R. Miller, the firm's president, a complete line of compatible logic modules in the one, five, and ten megacycle ranges is also available.

CIRCLE 113 ON READER CARD



Aeronutronic is now delivering the highest speed instruction memories for general use. Proved systems are available in standard line, built to special requirements or packaged for larger memories or aerospace installations.

BIAX memories improve the performance of ground-based and aerospace data systems that must operate reliably at very fast repetitive read cycling rates. BIAX memories also enhance reliability in applications in which non-destructive readout, low power level, and operation over extended temperature ranges are significant design factors.

BIAX memories find ready usage in—• Program, instruction, and statistics storage • Micro-programming techniques • Associative memories • Automatic check-out equipment • Digital simulators and training devices • Display and character generators.

The standard line of BIAX instruction memories offers modules ranging in size from 128 up to 1024 words for ground equipment. BIAX memories can also be customized to fit individual system design requirements not only in the area of speed performance but in capacity and packaging concepts as well.

Miniaturized aerospace BIAX memories are designed to withstand extreme shock, vibration and temperature environments. In this field, non-destructive readout, guaranteed security of stored data and low operating power levels are vital characteristics BIAX memories can add to your system. *For technical brochure, specific application information, or for price and delivery details contact: BIAX Memories Department MX.*

Typical Specifications for Standard BIAX memories

- Up to 1024 words
- Up to 36 bits per word
- Random Access — Non-destructive Readout
- Read Cycle time — 1 μsec
- Access Time — 0.3 to 0.4 μsec
- Operating Temperature — 0°C to 50°C
- Loading — from manual entry to on-line operation up to 200 KC
- Power — less than 50 watts

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CIRCLE 41 ON READER CARD

people IN DATAMATION

■ H. W. Thue has been promoted to vice president, manufacturing, of IBM's General Products Division. Formerly assistant general manager for manufacturing, he joined IBM in August, 1957, as a member of the IBM corporate staff in N.Y.C. Previously, he held the positions of director of manufacturing planning on the corporate staff, and general manager of the division's Endicott, N. Y., manufacturing facility.

■ The appointment of Harold A. Timken, Jr., as government liason manager of C-E-I-R's Washington Center has been announced. Timken's previous position was assistant to the president and director of marketing of Washington Technological Associates, Inc., Rockville, Md.

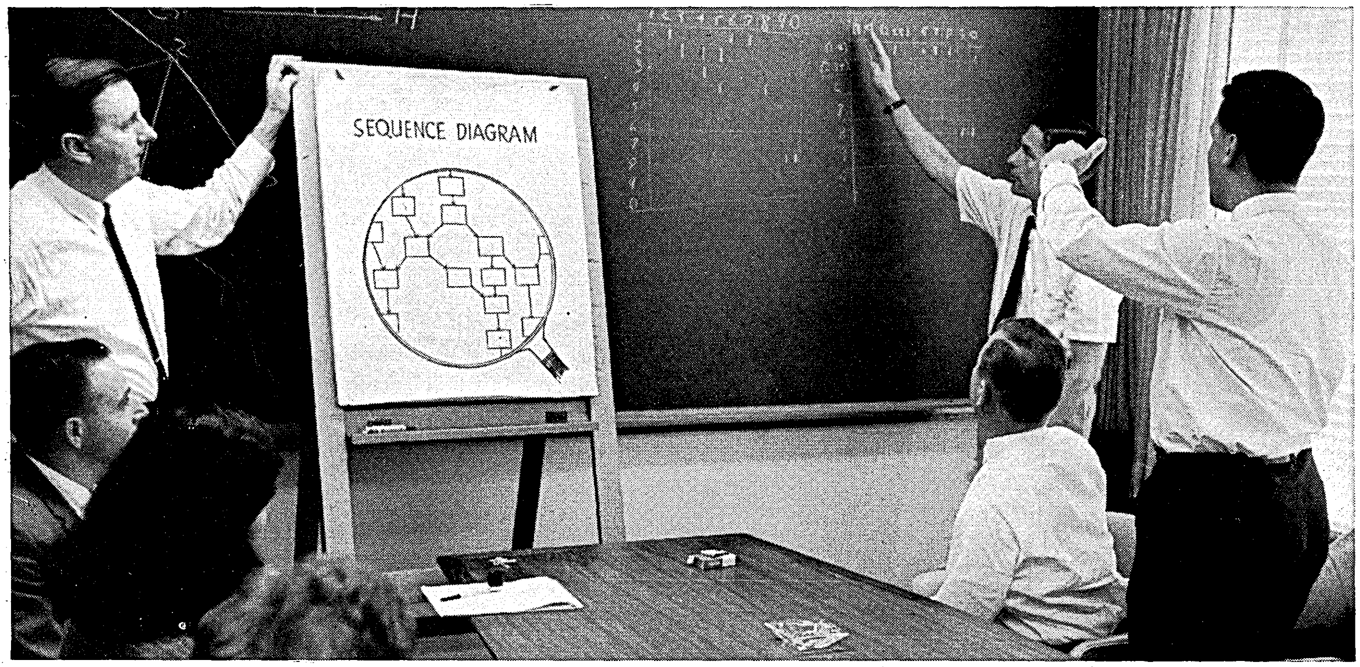
■ Princeton University has announced the appointment of Prof. Edward J. McCluskey, Jr., as director of the School's Computer Center. Hale F. Trotter, visiting associate professor of mathematics, was named associate director, and Dr. Irving Rabinovitz, formerly in charge of computing services for the Plasma Physics Laboratory, was appointed associate director for operations.

■ Filling the newly-created position of associate manager of project engineering at TRW Computers Co. is H. J. Ridinger, Jr., formerly manager of the division's marketing services. In his new position, he will be responsible for the application of TRW computers to the control of industrial processes.

■ Advanced Data Systems Corp. has announced the election of John J. Bonness to vice president. Previously, Bonness was manager of integrated data systems at the Los Angeles division of North American Aviation.

■ Dr. Stewart E. Fliege has been appointed manager of the SAGE Computer Programming Development department at System Development Corp.

at IBM



PROGRAMMERS shape the future of a new technology

IBM programmers, working with professional associates in research, development and manufacturing, are contributing expert knowledge and ideas in the creation of future computing systems.

This teamwork represents a striking advance in the role of the programmer and dramatizes the important part being played by this young but rapidly growing profession. At IBM, programmers are creating new concepts in software, and contributing to the design of new systems for virtually every phase of business, science and industry.

In response to the vastly increasing versatility of computers and their widespread applications, IBM programmers at all levels of endeavor are establishing new standards of achievement. They are designing programs that will simulate business and industrial operations. They are developing systems for government projects in space, defense and communications, where their data processing skills will help produce significant advances in tomorrow's computer technology. They are also studying the complex programs for . . . information-handling systems . . . scheduling methodology . . . information-retrieval studies.

IBM programmers also face challenging tasks in developing new programming systems. For example, they are devising programs that in turn use machine capability for formulating new programs. They are creating programs that enable computers to diagnose their own faults through self-checking. And they are helping to design the systems that will let scientists and engineers "talk" to machines in the everyday language of science and engineering.

Programmers at IBM take pride in their professional status and enjoy the unusual opportunities offered by a leader of the computer industry. In an atmosphere so receptive to new ideas, their concepts flourish. They find that their keen interest in exploring the capabilities of electronic computing is supported by IBM's full resources. This combination results in significant accomplishments recognized throughout the field.

Openings for programmers exist in all IBM facilities, including: San Jose, California; the Washington, D. C., area; Lexington, Kentucky; Rochester, Minnesota; Omaha, Nebraska; and New York City, Endicott, Kingston, Owego, Poughkeepsie and Yorktown Heights, New York. In addition to its extensive benefits programs, the IBM Educational Program is one of the most extensive in the country today. IBM is an Equal Opportunity Employer.

If you have experience in computer programming and would like to have more information about careers with IBM, we'd like to hear from you. Please write to:

Manager of Professional Employment
IBM, Dept. 701R
590 Madison Avenue
New York 22, New York

CIRCLE 83 ON READER CARD

CIRCLE 84 ON READER CARD

CIRCLE 85 ON READER CARD

CIRCLE 90 ON READER CARD

Why we believe the Tally Mark 50 introduces the Second Generation in Data Communications

Briefly, this is why: Tally's Mark 50 series is the only complete equipment ready now for *parallel* Bell System DATA-PHONE Service.

A little backtracking here may be enlightening before we tell you about the Mark 50.

During the past year, a number of perforated tape communications systems designed to operate computers and other data handling equipment in combination with Bell DATA-PHONE Service have been introduced. All of them, including our own, suffered from the basic disadvantages inherent in the serial mode of operation.

The serial system has two major weaknesses. One, the equipment is highly susceptible to bit dropout and bit insertion caused by switching transient generated noise. Two, high equipment requirements for serializing, character indexing, character recognition, and character reassembly.

New *parallel* DATA-PHONE Service completely eliminates all of these problems. In the parallel system, character condition is present for several cycles because of the 13 millisecond time interval between characters. Consequently, high network noise rejection. Parallel operation also means lowered business machine hardware requirements coupled with a modest increase in telephone company equipment. The result: A major cost reduction with a simultaneous increase in accuracy, and—a second dimension in communications.

About the Mark 50 Series

The Tally Mark 50 series is a complete perforated tape preparation and bi-directional communications center which combines a Tally perforator and reader, Tally transmit, receive, and error detection equipment, the new IBM Selectric typewriter, and the Bell System Parallel DATA-PHONE, 402A Transmitter and 402B Receiver.

In one compact console, the user can prepare data tape as a by-product of a useful typing operation and then, at any convenient time, he can transmit the data at 750 words per minute over the dial-up telephone network. On mating Tally equipment, the data is received at 750 words per minute and recorded on perforated tape, followed by printout at 155 words per minute using the IBM Selectric typewriter. The new Selectric prints out 25% faster than the IBM model B or other equivalent automated typing equipment.

Unique Code Structure

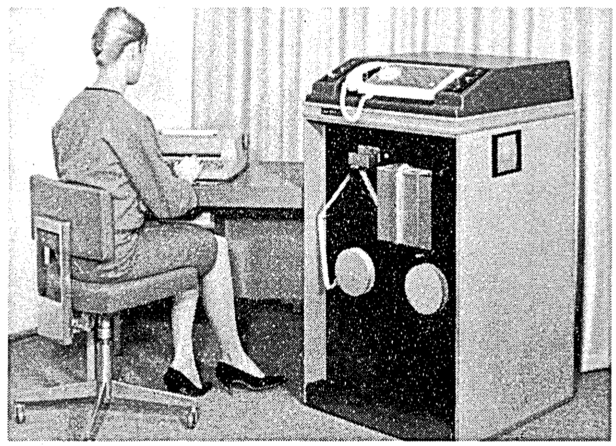
The Mark 50 Series is offered with the Tally 1501 code structure, an 8 level code on a 1″ wide perforated tape. Whenever one Selectric is preparing information for another Selectric, code variations are of no importance. Where code translation is required, note that the Tally 1501 code corresponds generally with character assignment in IBM and other codes minimizing the code conversion problem. Where the tape is used for computer input, the program can be written to perform the translation.

About Mark 50 Series Readers and Perforators

Tally produces its own perforators and readers which have been proven in hundreds of customer installations from coast to coast. By manufacturing all of the equipment in data communications systems except the DATA-PHONE, Tally maintains *complete* system control.

Automatic Error Detection

Error detection and correction is important in data transmission equipment simply because of inherent switching transients in the automatic dial-up telephone network. Indeed, the telephone people themselves recommend that business machines be equipped to recognize and re-transmit those data portions necessary to provide error-free data. Tally Mark 52 and 53 systems carry a "forward skip" feature so that data prepared on source machines, such as billing typewriters, can be block error coded and transmitted in reverse. The data block in error is recognized because of the error code and transmission is suspended while the reader passes over the block in error. This same feature facilitates tape clean-up and off-line error-free tape duplication. In summary, Tally Mark 52 and 53 systems can check errors prior to sending, during the receiving process, or as a re-read operation after receiving.



Mark 51 Data Communications Center using IBM Selectric typewriter.

More Information

Further information on the powerful new Mark 50 series can be obtained by calling your nearest Tally engineering representative (sales and service in more than 30 cities), or writing directly to our Marketing Manager, Tally Register Corporation, 1310 Mercer Street, Seattle 9, Washington. Phone: MAin 4-0760, TWX SE 551.

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PROGRAMMERS: SCIENTIFIC and BUSINESS

INVESTIGATE NEW OPPORTUNITIES in our COMPUTER CENTER at the Lockheed-Georgia Company, located near Atlanta, a city of flowering beauty and ideal climate.

SPECIFIC OPPORTUNITIES IN:

SCIENTIFIC PROGRAMMING utilizing the 7090 computer in areas of: Monitor Systems; Numerical Control Systems—APT I, II, III; Information Retrieval; Flow Field Investigation; System Analysis; Statistical Analysis; Dynamic Systems Analysis; Simulation Systems; Flight Data Reduction; Analogue-To-Digital Conversion; Trajectory Computation; and Operations Research. Also openings for Analogue Computer Engineers for application, programming and operation of Direct Analogy Electric Analogue Computers.

Requirements include a Bachelor's degree in Mathematics or related field and experience in programming scientific problems on the 7090, 709 and 704 computers.

BUSINESS PROGRAMMING utilizing the 7080, 1410 (Random Access) and 1401 computers in areas of: Design of a total Management System; Research on projects such as Management Information Systems, Communications Media, Portrayal of Logical Concepts, Advanced Programming Languages; and Man-Machine Relationships.

Requirements include a Bachelor's deree in Scientific or Business fields and experience in programming business problems on the 7080, 1410, and 1401 computers.

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SENIOR COMPUTER PROGRAMMERS and SENIOR SYSTEMS ENGINEERS are invited to discuss immediate opportunities available in Philadelphia and Washington. To discuss these professional positions in confidence, please contact – William S. Walker.

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■ In continuous operation since 1955, this high-quality team of computer experts has solved complex problems through sophisticated programming . . . for a variety of computer systems.

■ A current assignment for a leading computer manufacturer requires GKI to develop a formula translator/compiler for two computer languages, ALGOL 60 and FORTRAN II. Other recent GKI accomplishments . . . Analysis and Program for Calculation of Optimum Propellant Performance for Liquid and Solid Rocket Fuels; Rapid Item Processor to Facilitate Complex Operations on Magnetic Tape Files.

■ For more information, including other examples of recent work, please write or phone.

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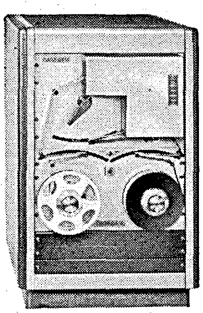
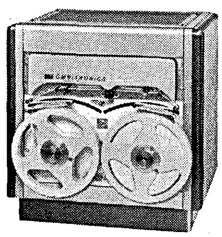
operating at 600 CHARACTERS A SECOND
...and doing it reliably!

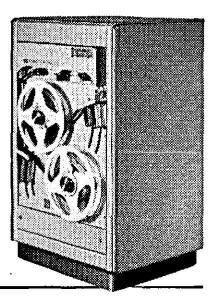
The new OMNI-DATA electrostatic recorders, reflected-light readers, and high-speed reelers comprise the first complete systems for presentation, reading, and reeling of paper tape at speeds up to 600 characters a second.
Options and modifications available. Write for complete information.



omni-data electrostatic recorder with reeler, Model ETR-70250. Eliminates mechanical tape punches through high-speed recording of visible data on paper tape. Shown here with 8-in. reels.



omni-data photoelectric reader with reeler, Model PTR-70250A. Reads any type of tape—punched or recorded, opaque or transparent—with chopped reflected light. Offers start-and-stop asynchronous action up to 60 steps per second. Unidirectional, with rewind and no tape breakage.



omni-data bidirectional reader with reeler, Model PTR-71400. Same 600-characters-per-second speed as other OMNI-DATA equipment, plus advantage of bi-directional operation. Reeler accommodates any diameter NAB reel up to 10½ in.

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NCR

ADVANCED PROGRAMMING RESEARCH

The expanding utilization of NCR's computer systems has created new opportunities for experienced programmers familiar with automatic programming techniques. College education, plus 2-5 years experience with large scale magnetic tape systems can qualify you for a rewarding career with NCR, one of the world's leading business machine manufacturers. Recognized and respected wherever men trade, NCR stands alone for its creative and flexible approach to business system development.

Aside from the opportunities present in Programming Research, other openings in our expanding operation include:

- Installation Representative: experience required, covers magnetic tape system programming, knowledge of complete business systems, and ability to work effectively as a representative of NCR.
- Programmer: for small systems work which requires good background in data processing as related to normal business functions and some knowledge of programming of magnetic tape systems. Intermittent customer contact.
- Instructor: experience and education should be such that the person employed can effectively train program personnel. Familiarity with math and business systems is desirable. Programming of magnetic tape systems necessary.

Other opportunities may more nearly meet your particular experience and aspirations. To investigate, you need only write, sending complete resume to:

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The National Cash Register Company, Main & K Streets, Dayton 9, Ohio

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COMPUTER TAPE CONVERSION CENTER

Now you can let your computers talk to each other fast and at low cost through a brand new mail order service. Your magnetic tapes, paper tapes, and IBM cards will reach us overnight via air mail and air express from anywhere in the country. Accepted and generated at our new center are magnetic tape formats for IBM, Burroughs, RCA, and Remington Rand computers, 5 to 8-level paper tape formats for Friden-Flexowriter, Teletype, NCR, and IBM 1620, IBM 80-column card Hollerith coding. For the first time, obtain rapid, economical direct data format conversion without leasing or purchasing costly conversion equipment.

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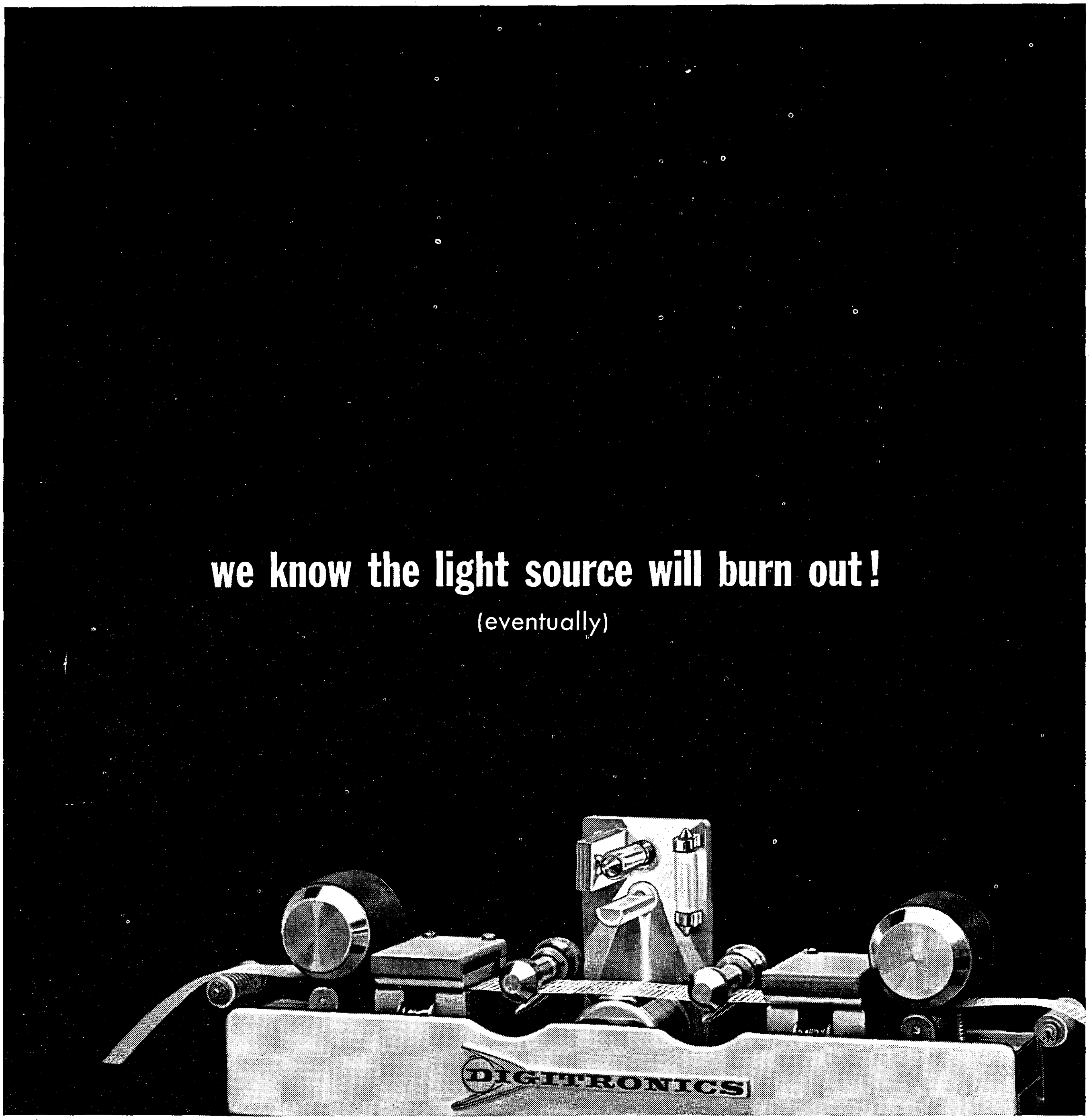
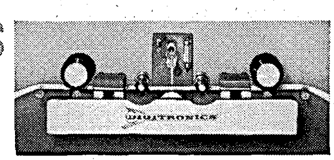

we know the light source will burn out!
(eventually)
DIGITRONICS



ADVERTISERS' INDEX

TRI

TRICE: The world's most advanced hybrid gp/dda computing system; shortens engineering schedules by months, saves thousands in programming costs. If TRICE is applicable to your projects, you're already paying for it.

TRICE is a major advance in computing technique offering dramatically increased efficiency for your operation. Many problems that may now be putting excessive demands on your large digital computer and its programming staff can be more effectively handled by TRICE... at a fraction of the cost and without dislocation of your other work. TRICE pays for itself in less than a year.

This powerful hybrid gp/dda computing system for real time solution of differential equations can be applied to problems found in simulation studies ... axis transformations... open loop integrations. TRICE provides the accuracy and repeatability of the digital computer combined with the speed and programming ease of the analog computer.

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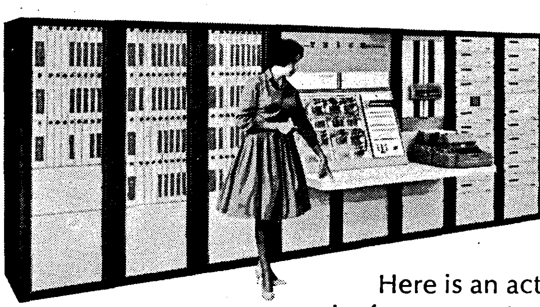

Here is an actual example, from many in our files, of the spectacular savings possible with TRICE. A certain transformation problem required two months of programming for solution by a large scale computer; the same problem was programmed and solved on TRICE in just three days. That problem, like many others, cannot be solved satisfactorily on obsolete analog computers. Space age technologies demand accuracy and repeatability beyond analog capability plus the computing sophistication offered by TRICE.

TRICE is simple to use. One customer's engineering staff learned to program TRICE in only one morning—from a sales brochure. Such a sales brochure would probably be of interest to you. Why don't you write for your copy?

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