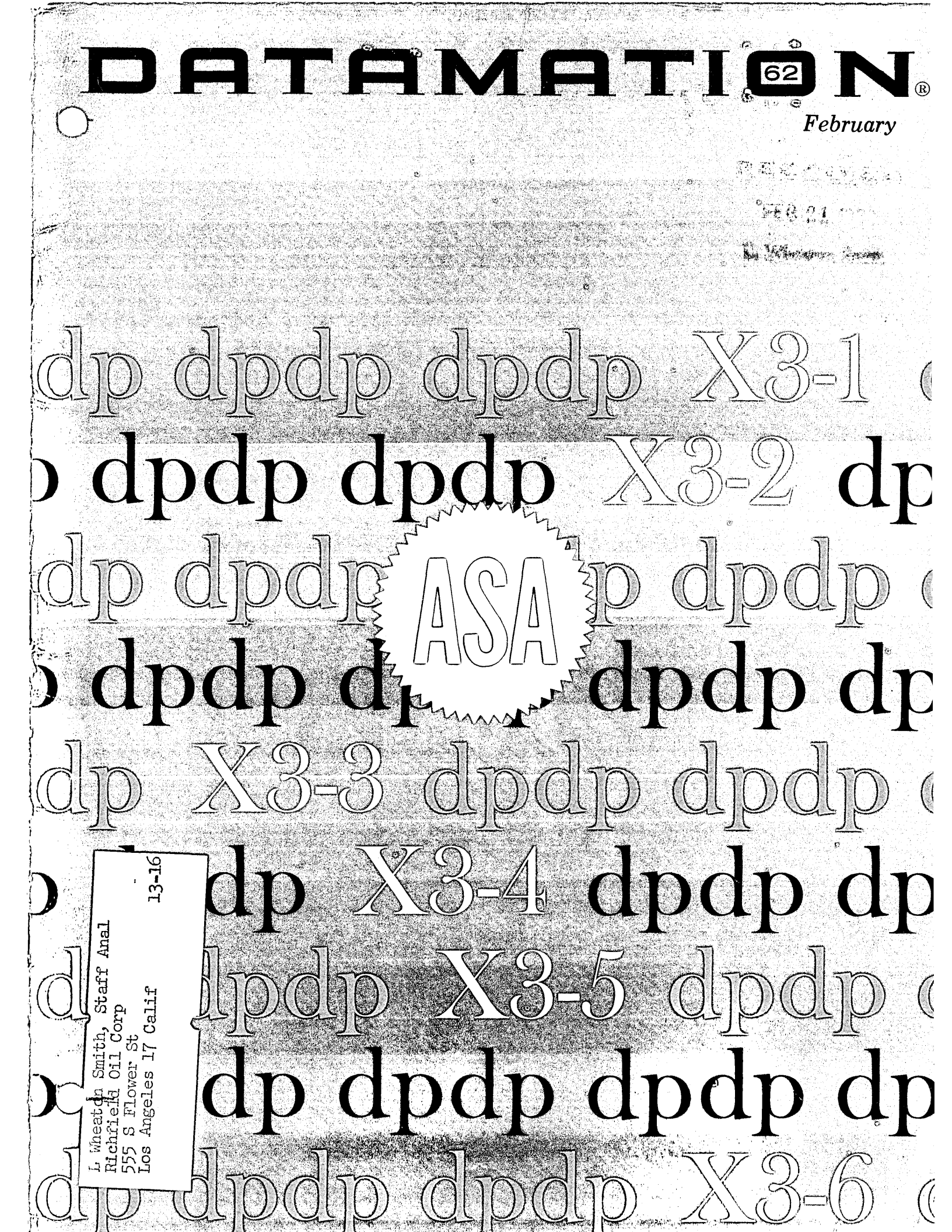
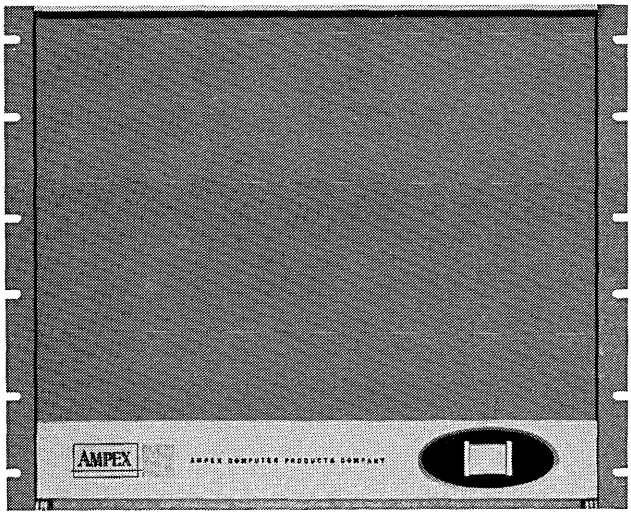
DATAMATION®

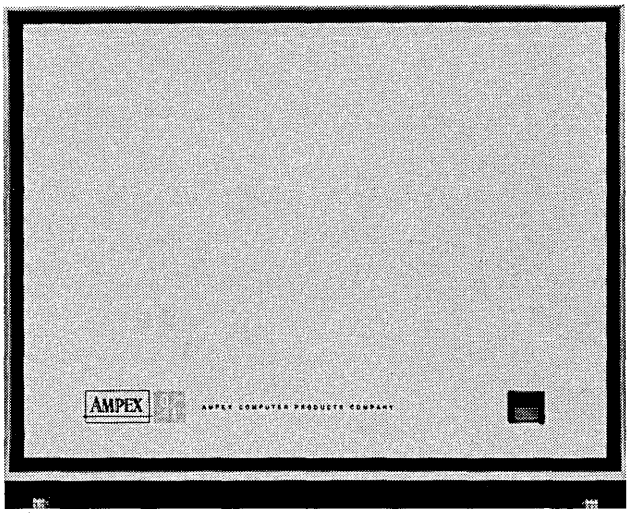
62

February





Yesterday Ampex introduced the RB for data systems that need a small memory. (1024 words.)

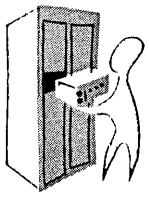


Today we bring you the RVQ for systems that need to think a bit bigger. (4096 words.)

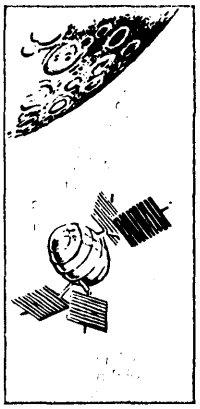
The Ampex RVQ core memory unit is ideal for data systems that need small-to-medium storage capacities. At the same time, it has the flexibility for random access applications or high speed sequential or buffer operations. It's designed for rack mounting—a 36 bit word RVQ occupies only 15¾" of rack space. It loads or unloads in 4 microseconds. Has a complete memory cycle of 6 microseconds. Remembers words 8 to 36 bits long. And operates on conventional unfiltered and unregulated AC power. You can tell it's an Ampex model by its reliable, simple operation. And its ease of maintenance—just flip the front panel down. The RB and RVQ are two of more than 40 solid state memories made by Ampex. Cycle times range from 24 to 1 microseconds with capacities up to a million bits or more. For data write: Ampex Corporation, 934 Charter Street, Redwood City, California.

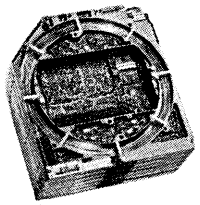
AMPEX

CIRCLE 1 ON READER CARD



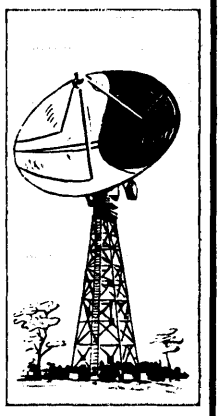
continuing its leadership in digital electronics!

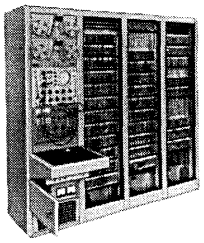




SPACE

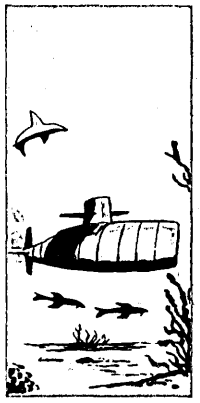
Ultra-reliable, high density, low-power consumption, data acquisition and storage systems for deep space probes.

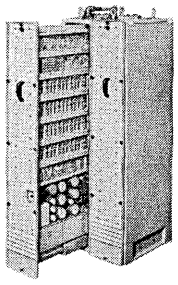




GSE

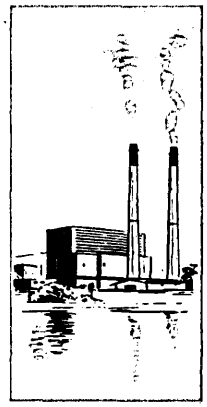
Real-time target acquisition and tracking computers for military and space applications.

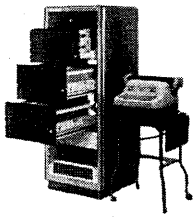




ASW

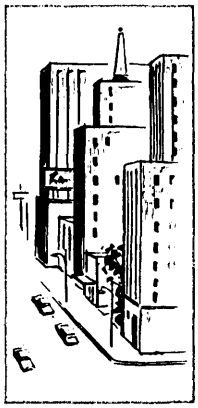
Information processing systems for surface and undersea sonar and communications applications.

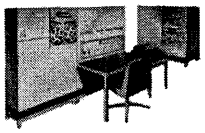




INDUSTRIAL

Digital scanning, positioning, and read-out systems for process control and other industrial applications.





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General and special purpose computers, data conversion systems, and information retrieval systems for commercial and industrial applications.

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With a minimum of fanfare, the Systems Division of Computer Control Company, Inc. successfully and continuously designs and produces many types of computing and control systems for Government, industrial, and commercial applications. Only a few of these devices and their respective areas of application are illustrated above.

This quiet but continuing proficiency is another aspect of the methodical determination of the Systems Division of 3C to maintain its leadership in complete systems capabilities. We are very proud of the customer respect we have earned.

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COMPUTER CONTROL COMPANY, INC.

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CIRCLE 4 ON READER CARD

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Whatever your immediate or long-range computer requirements, Bryant is equipped to provide "right now" response to your needs for prompt delivery of custom-designed memory drums, standard storage units, read/record heads, and other precision memory system components.

Remember—Bryant Magnetic Memory Drums offer these special features:

- Time-proven reliability
- Super-precise ball bearing suspension
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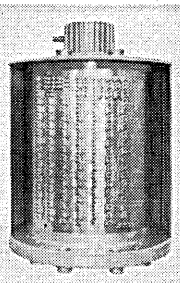
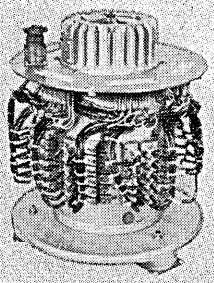
- Precision integral-drive induction motors
- Exclusive tapered drum design

For more detailed information, or if you'd like to discuss your particular storage drum application problems, contact your Bryant Representative, or write direct: 852 Ladd Road, Walled Lake, Mich., MArket 4-4571.



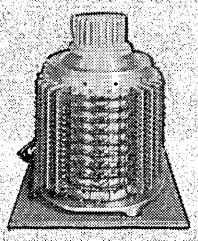
MASS DRUM MEMORY

Capacity—Up to 6,210,500 bits with fixed heads—25,000,000 bits with movable heads . . . **Tracks**—Up to 825 . . . **Speed**—900, 1800 or 3600 rpm . . . **Size**—18.5″ dia. x up to 34″ long . . . **Access time**—As low as 16.6 ms (one head per track).



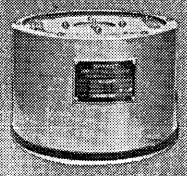
BUFFER APPLICATIONS

Capacity—Up to 225,000 bits . . . **Tracks**—Up to 150 . . . **Speed**—Up to 60,000 rpm . . . **Size**—3″ to 5″ dia. x 1″ to 8″ long . . . **Access time**—As low as 0.25 ms (4 heads per track @ 60,000 rpm).



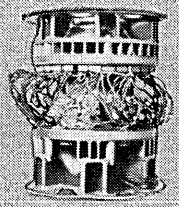
GENERAL MEMORY

Capacity—20,000 to 2,500,000 bits @ 130 bits per inch . . . **Tracks**—40 to 420 . . . **Speed**—600 to 24,000 rpm . . . **Size**—5″ dia. x 2″ long to 10″ dia. x 19″ long . . . **Access time**—As low as 2.5 ms (one head per track) . . . Aerodynamic heads optional.



SPECIAL PURPOSE MEMORIES

Analog recording . . . Multispeed operation . . . Speed—As low as 2.5 rpm . . . **Aerodynamic heads** for high density, high frequency recording . . . **Flux-sensitive heads** for low-speed playback . . . **Air bearing drums . . . Magnetic Disc Files** for mass storage up to 720,000,000 bits.



AIRBORNE SYSTEMS

Capacity—Up to 250,000 bits . . . **Tracks**—Up to 150 . . . **Speed**—Up to 18,000 rpm . . . **Size**—As small as 6″ dia. x 6″ long . . . Weight—As light as 7 lbs . . . **Access time**—As low as 3.3 ms (one head per track). Designed to meet MIL-E-5400.

62-41-CP

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XLO

DATAMATION 62

the automatic handling of information

volume 8, number **2**

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THIS ISSUE — 41,125 COPIES

Cover

As the centralizing body for the U.S. standards effort in data processing, the American Standards Association's X3 committees are attractively represented on this month's cover designed by Art Director Cleve Boutell. While there is a logical pattern evident in the arrangement of the committees, it is equally apparent that unity has not been entirely achieved. An editorial analysis of progress in dp standards begins on page 19.

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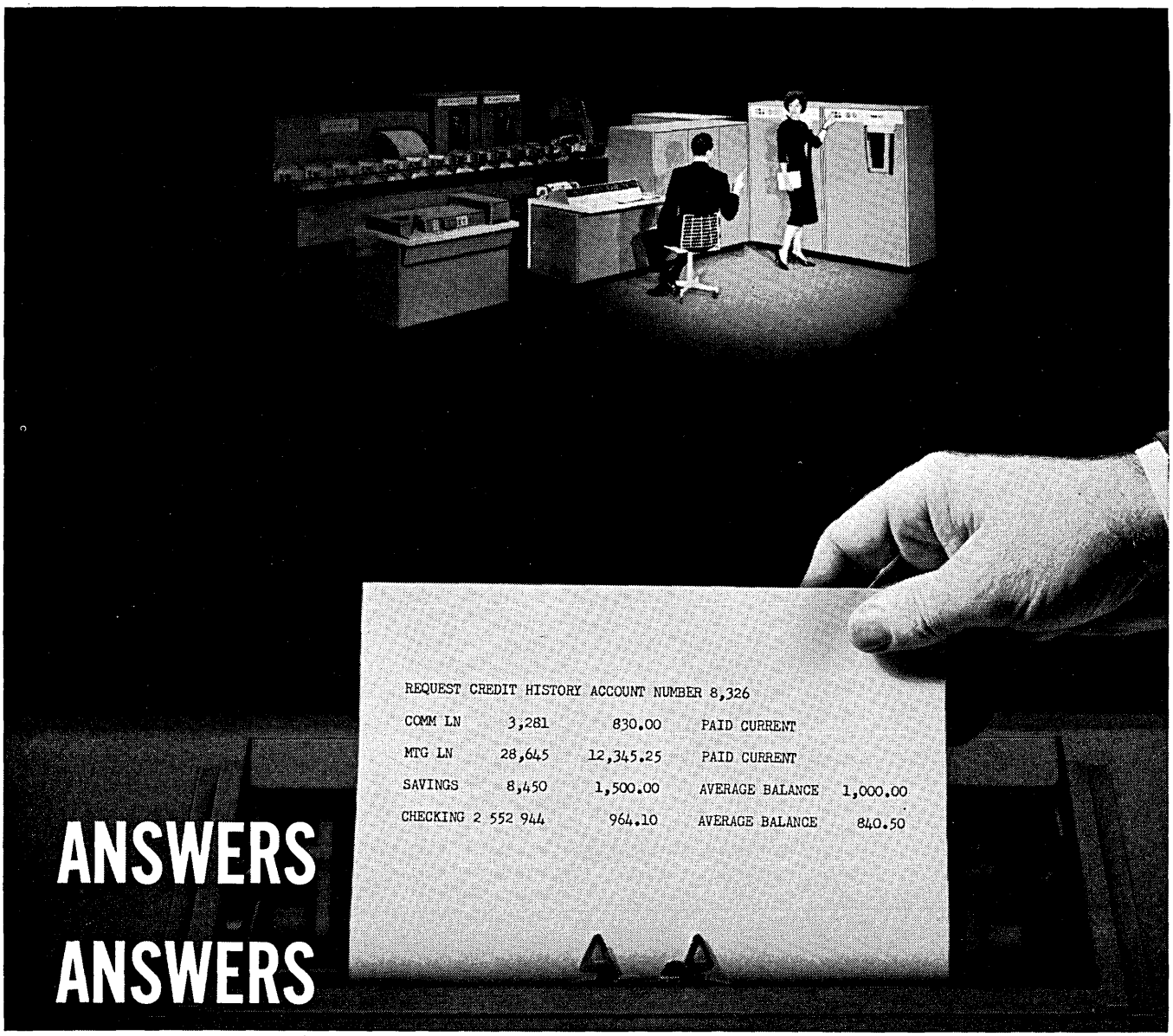

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provided by the NCR 315 Computer System

The NCR 315 CRAM (Card Random Access Memory) Computer System is more than just another back-office electronic accounting machine . . . it is a vital electronic tool which contributes to a higher-quality of management and personnel effectiveness.

For example: in a bank, Inquiry Units placed in the various departments enable authorized personnel to interrogate the computer files at will . . . to promptly answer requests for balances . . . to quickly obtain valuable credit information . . . to obtain current, up-to-the-minute reports on investments, trusts, loans, and other essential data.

In Industry, Inquiry Units can be located at dozens of remote locations, enabling people to communicate with the computer files . . . even from hundreds of miles away. With the NCR 315 you will be able to keep a "current-finger" on the pulse of your business . . . to get immediate answers to questions about inventories, production, sales . . . and a host of other timely facts people must have to effectively manage . . . and to act while the "iron is hot."

The NCR 315 CRAM System provides many exclusive advantages for Remote Inquiry, Data Processing, On-Line Accounting, Operations Research, Engineering and Scientific Applications . . . for more information, call your nearby NCR representative or write to Data Processing Systems and Sales, Dayton 9, Ohio.

NCR PROVIDES TOTAL SYSTEMS—FROM ORIGINAL ENTRY TO FINAL REPORT—
through Accounting Machines, Cash Registers or Adding Machines, and Data Processing
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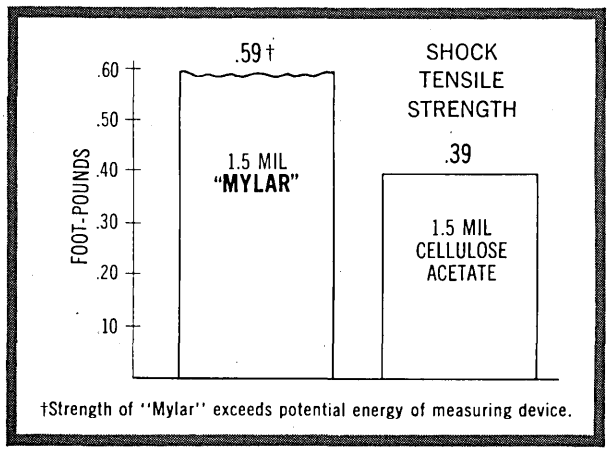
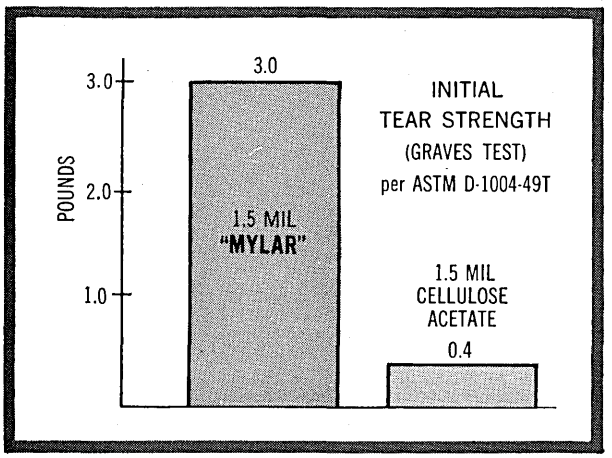
NCR®

CIRCLE 6 ON READER CARD

GUARD AGAINST DOWNTIME WITH RELIABLE TAPES OF MYLAR®





Every minute of downtime costs you dollars. That's why the reliability of your magnetic tape is so important. Tapes of Mylar*, resist breaking from sudden starts and stops since they have high shock-tensile strength . . . and they have 7 times the initial tear strength of acetate tapes.

"Mylar" adds to the reliability of playback. It resists the cupping, swelling and shrinking which can reduce intimate head contact and cause read/write errors. Age, storage conditions and repeated playbacks won't affect "Mylar" either.

The cost of the data . . . the cost of the equipment . . . the cost of time *all* demand reliability. Get it with tapes of "Mylar". Send coupon for free booklet of comparative test data and judge for yourself. Du Pont Company, Film Department, Wilmington 98, Delaware.

*Du Pont's registered trademark for its polyester film.

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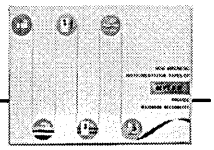


E. I. du Pont de Nemours & Co. (Inc.)
Film Department, Room #12, Wilmington 98, Delaware

Please send free, 12-page booklet of comparative test data to help me evaluate magnetic-tape reliability.

Name_____ Position_____

Company_____

Address_____

City_____ Zone____ State_____

CIRCLE 7 ON READER CARD

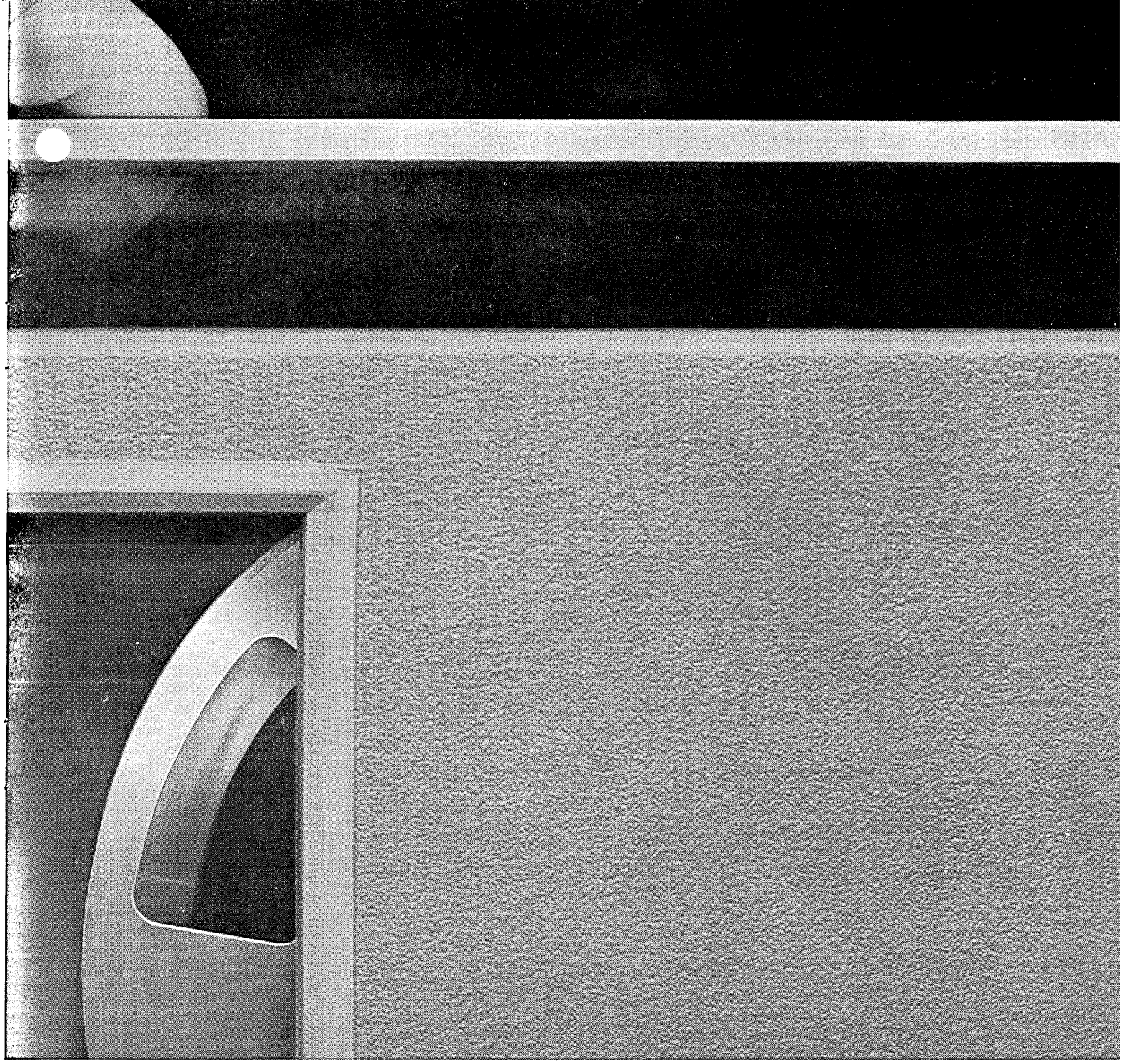
New Hypertape Drive gives your IBM

Here's a new input/output device that will let you get more information into your computer to take even greater advantage of the tremendous electronic speed with which it processes information internally.

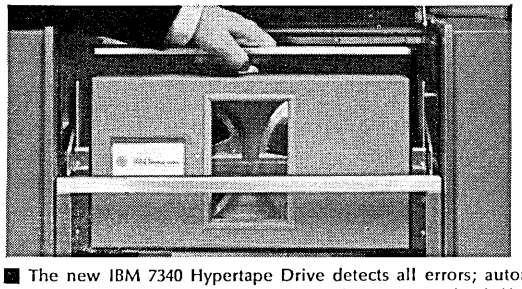
This new Hypertape stores two to four times as much information and delivers the information to your computer two to four times faster than your present tape system.

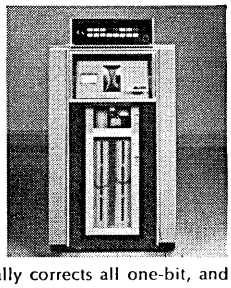
The magnetic tape is kept in a sealed, dust-proof cartridge. All you do is place the cartridge in the tape drive... the rest is automatic. No more manual threading and unthreading. It takes only 20 seconds or about one-quarter the time it takes with conventional reels.

Ask your local IBM Representative for details.



computer information twice as fast





The new IBM 7340 Hypertape Drive detects all errors; automatically corrects all one-bit, and most two-bit errors; and, depending on the system with which it is used, processes up to 340,000 numeric or 170,000 alphabetic characters per second.

IBM®
DATA PROCESSING

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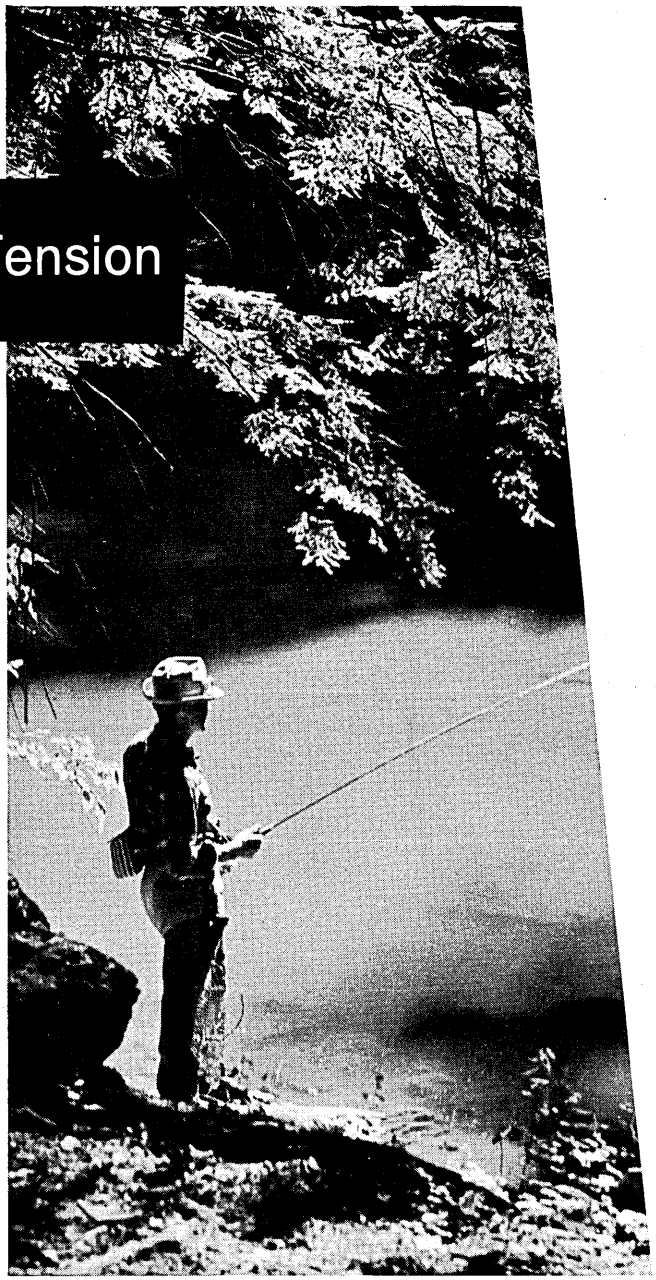

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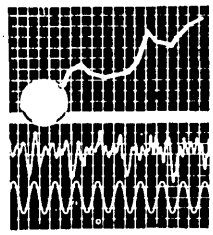


BUSINESS &

SDS TO ANNOUNCE TRIPLETS IN MARCH

A new line of small-scale, gp computers designated the 910, 920 and 930 will be formally announced by Max Palevsky's Scientific Data Systems next month. Hardware delivery is planned for the autumn and software (FORTRAN and a symbolic assembler) will be completed early next year.

The new machines will feature silicon transistors (the first non-military use) and will be priced from $40-100,000. They will be marketed largely for the scientific and control fields and feature a basic core memory of 2K in the 910 and 4K in the 920 and 930. All memories will be expandable to 16K. The word size is 24 bits plus one bit for parity. Add time in each machine is 16 microseconds.

Built-in features of the line include I/O devices such as indirect and relative addressing. Palevsky will also announce a scheme known as "programmed operator" which he refers to as compatibility of the equipment permitting users to go down in power and size as well as in the more customary upward direction.

A 300-line-per-minute printer will be offered as peripheral gear with paper tape readers and optional mag tape units.

Palevsky feels that the chief competitors for the SDS line are Digital Equipment Corp.'s PDP-1 and Control Data's 160A.

PB RALLIES FOR PROFIT IN '62

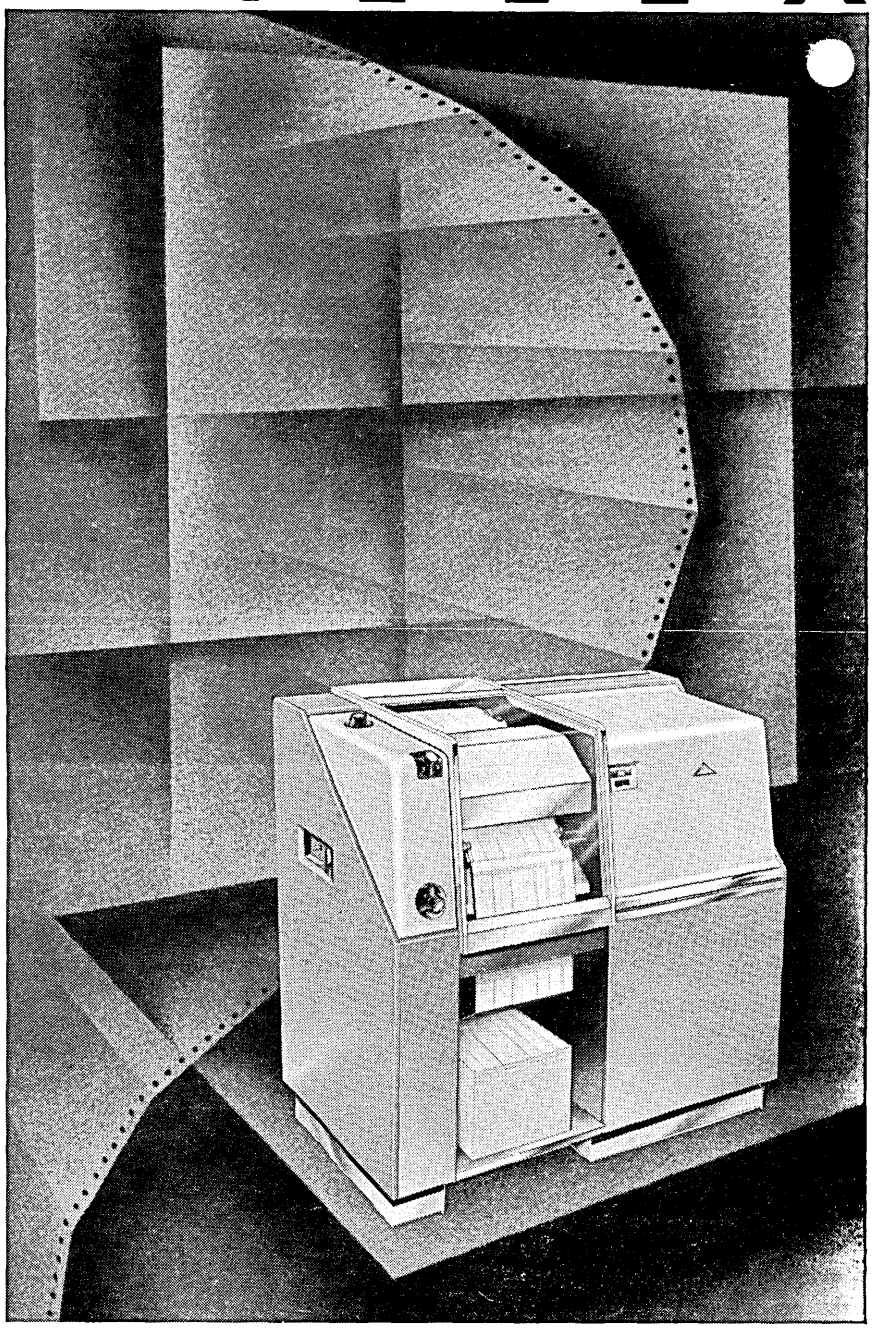
Packard Bell Computer is gradually revitalizing its posture in the computer field following last year's heavy financial setbacks and the resignation of top level personnel. Under the generalmanship of S. Dean Wanlass (founder of Aeronutronic), it is expected that 1962 will be the first profitable year for the corporation with a doubling of last year's sales of $5.9-million.

Still the mainstay of PB, 40 250s have been installed and about 25 are on order. Production expectations are for 7 250s per month.

A new computer somewhat above the 250 in power and size, will be announced early this year in the less than $100,000 price range. The earlier designation 350 has been dropped and internally, the new hardware is known as "Phoebe."

There will be no delay lines in the new machine and it will not be third generation. Expectations are for

ANELEX®



To the expanding line of Anelex High Speed Printer Systems has been added the new Model 300 . . . especially designed for those installations which need high capability and low cost . . . but with output requirements well satisfied by a printing rate of 300 lines per minute.

With all the reliability, versatility and operating convenience of faster, more expensive Anelex Printer Systems, the Model 300 will print 120 columns on forms up to 19″ wide and 22″ deep. The complete System is housed in a compact, modern, soundproofed cabinet and can be installed almost anywhere for on-line or off-line use.

ANELEX
SYMBOL OF QUALITY

Further information available on request

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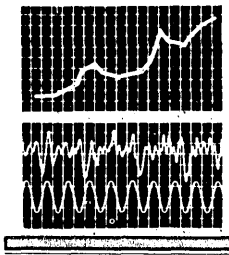
CIRCLE 9 ON READER CARD



BUSINESS & SCIENCE

a basic 4K core memory expandable to 16K. Chief competition will be the IBM 1620. A third machine smaller than the 250, may be introduced in '63.

In components, Wanlass feels that PB has been "delinquent in new product development" and the depth of the line will be increased this year. Finally, PB's $750,000 digital differential analyzer, TRICE, which appeared over-priced for the market 1½ years ago, is expected to experience wider sales in '62. Three orders are in the house.

OPTIMISM OUTPUT FROM PHILCO & RCA

Despite a considerable shuffling of top-level brass (see People in Datamation, page 23), both Philco and RCA have disseminated a heavy output of "we're-really-behind-our-computer-division" optimism during the past two months. And while their statements have been promising, there has been no formal pronouncements as to changes in specific direction or general attitude. Waiting and professional speculation continues.

At Philco, president Charles E. Beck was quoted in a local Philadelphia paper as stating, "Electronic computers offer a tremendous opportunity, and we intend to get our share of the market." Also serving as director of Ford's business planning office, Beck said that Philco's new management has no plans to discontinue any of the company's present operations. In a later interview for a national trade paper, Beck was somewhat less optimistic and felt that Philco "is not going clear across the board" in marketing computers and would place less effort in sales for commercial applications. He added that a concentrated effort would be made on the area in which Philco believes it has superior capabilities (i.e., 7090 users).

With the financial backing of Ford (one of the few companies in the U.S. that can probably buy IBM), Beck's statements appear cautious and somewhat in conflict with the general expectation that "IF" Ford does decide to back its new computer division, all holds previously in operation would be generously lifted.

At RCA, Board Chairman David Sarnoff in a year-end statement, emphasized the company's "firm determination to assure for RCA an important position in this vital and expanding field" of data processing. He added that RCA's costs in dp were believed to have reached a peak in 1961 and "we expect that our 1962 edp losses...will be approximately half of what they were in 1961."

And while thought is obviously being given to encourage this healthy posture, the only activity widely publicized has been a severe personnel shake-

up following the Burns resignation. Retrenchment is widely suspected throughout RCA's edp division with cutbacks in the 601 and 604 program and less emphasis on the 501. Aside from special purpose military contracts, the only hardware still in active competition is the 301 which is hardly as significant a contribution to the industry as RCA's financial resources and Sarnoff's public statements imply. The most likely route is a commercial version of RCA's Project Lightening work in nanosecond hardware. However, in view of the implied cutbacks in financial support and the large appropriations necessary for applications and product development, the outlook for this alternative also appears dim.

"SELLING" THE UNIVERSITY

A prime target for large scale computer manufacturers is a prestige installation at one of the major U.S. universities. New hardware as well as the more venerable giants are being offered on literal silver platters with not-too-subtle disguises for slicing the purchase price down to a token payment or none at all.

Several manufacturers have refrained from bidding in this area on grounds that it is increasingly difficult to compete against a free machine and even rougher to turn a fair profit. The university (like many a prospective customer) is anxious for the best possible price regardless of thinly veiled shenanigans.

Major university installations include: RemRand's 1107 at Notre Dame; B5000 at Stanford; H-800 at USC; IBM 7090s at CalTech, Stanford and UCLA, Bendix G20 at Carnegie Tech, and a CDC 1604 at the University of Texas.

The sales tactic most frequently used in installations such as these (and not always by the winner) is a benevolent educational discount up to 60% off rental, which is often accompanied or replaced by one of the following: a) a large, overt donation to the school; b) a generous scholarship program initiated by the manufacturer; c) substantial prepayments for third shift rental; d) a liberal purchase of time by the manufacturer for service and training; e) not relinquishing ownership of the hardware but installing it at the school and reserving one shift of free time, and finally f) donating the machine with no contractual frills except the promised cooperation and facilities of the university.

While the result is frequently to the general advancement of computer education, the means to this pious end have forced some manufacturers to drop what they considered a fair educational discount, and others less able to compete have stopped production on a line which they could not give away.

Occasionally, the "sale" may backfire such as when one manufacturer offered a large prepayment on third shift rental to keep a competitor's machine off the ivy covered premises. In this case the school did accept the machine and the prepayment but used the newly acquired capital to buy the competitor's hardware as well.

letters

FORTRAN diagnostic

Dear Editor,

Here is another letter in what I suspect is a large stack of mail informing you of the error appearing in the FORTRAN "DO" statement on the cover of your December issue. The statement:

DO 21 I = 1,1,N

should have read

DO 21 I = 1,N,1

or

DO 21 I = 1,N

These last two are equivalent, if the increment by which "I" is to be increased each time the instruction is executed is not specified, it is taken to be "1".

J. W. SCHOENBORN
IBM, Federal Systems Division
Bethesda, Maryland

Dear Editor,

One of my colleagues has pointed out to me that the best argument one could give for switching from FORTRAN to MAD, ALGOL or BALGOL is the cover of the December issue. The simple iteration pictured in all four languages is correct in MAD, ALGOL and BALGOL, but in FORTRAN we find not only a mixed expression, but incorrect formation of the "DO" statement (for the iteration desired).

BERNARD A. GALLER
The University of Michigan
Ann Arbor, Michigan

Editor's correspondence to and from *Datamation* advisor Dan McCracken:

Dear Dan,

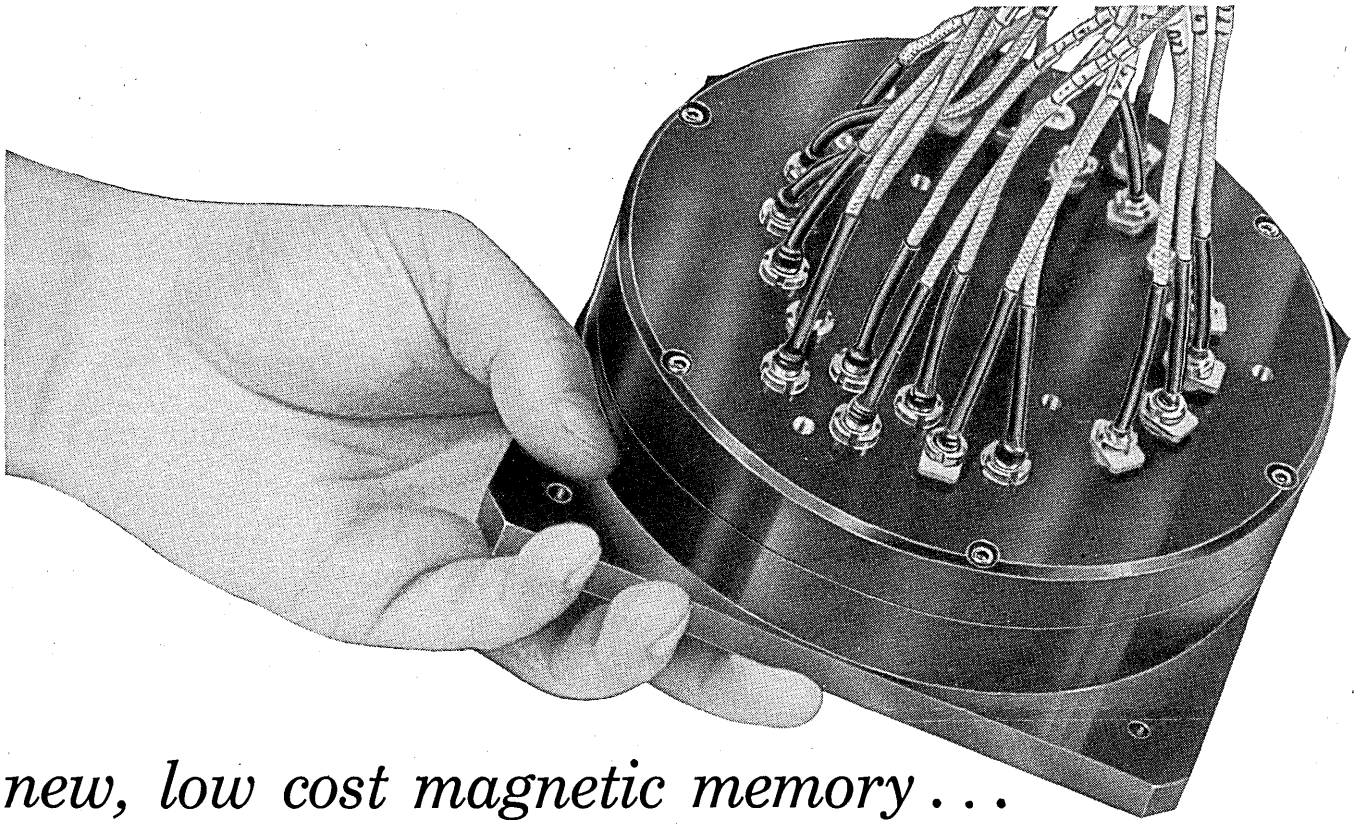
Thanks a lot for preparing the statements for our December cover. Maybe I can write something for your next book. *Merry Christmas, Hal*

Dear Hal,

What can I say? I wish I could claim printer's error, but that is a bit difficult since you have so considerately supplied me with my original copy, which shows the statements exactly as they appeared on the cover. Should I quote from my book on FORTRAN? "Care must be taken to observe the rule for distinguishing between fixed and floating point variables, but one learns fairly readily to avoid this pitfall."

I think I should give up, after noting that this wouldn't have happened in ALGOL. (If you hear of any other errors, don't bother to tell me.)

Happy New Year, Dan



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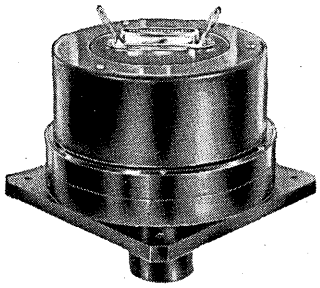

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Storage Capacity (max.) Bits	25,000
Disk Diameter (max.) Inches	4
Bits per Track (max.) @ 1½" radius	2,300
Bit Rate — kc	10-500
Track Layout As Required	
Typical:	
Total Tracks:	12
Data Storage Tracks	*
Spare Tracks	*
Clock and Timing Tracks	*
Register Tracks	*
Number of Registers	*
Register Length — Bits (minimum @ 2,300 B/T)	32
Register Adjustment — Bits	±3
Disk Speed — RPM Induction or Synchronous Motors Available	6,000-12,000
Power Source — cps	400
Magnetic Heads (Compatible with solid state circuits)	
Standard Heads	
Inductance (Per Leg. — C.T. Coil) uh	40, 55, 90
Write Current (O/P Manchester) ma (nominal)	125
Read Out (Min. P/P Full Coil) — mv (nominal)	20
Size — Inches	5¾ x 5¾ x 5
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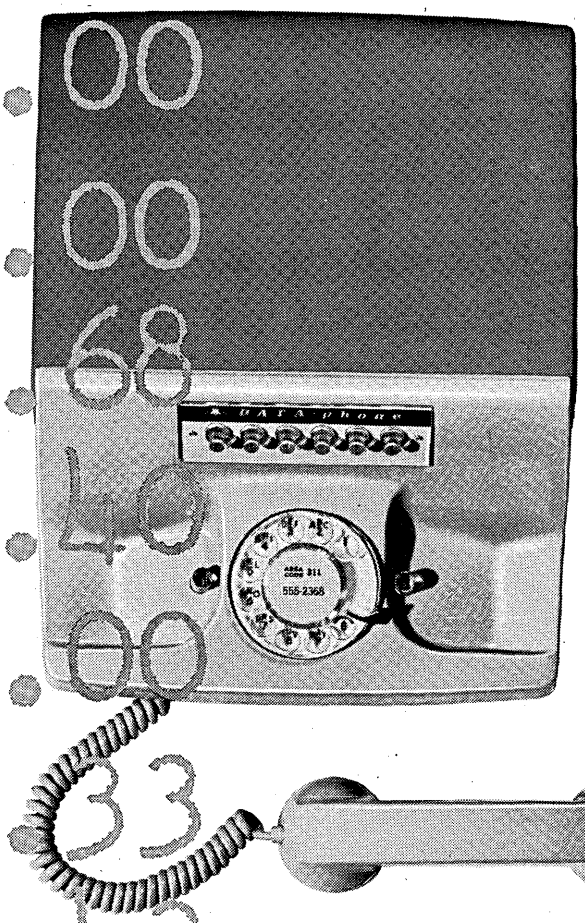
CIRCLE 12 ON READER CARD

important DATES

- The American Management Association's Eighth Annual Conference & Exhibit will be held Feb. 26-28 at the Statler-Hilton Hotel, N.Y.C.
- The IRE National Convention is scheduled for March 26-29 at the Waldorf Astoria and Coliseum, N.Y.C.
- The 15th annual Southern California Business Show will be held March 20-23 at the Ambassador Hotel, Los Angeles.
- A symposium on Interactions Between Mathematical Research and High Speed Computing will be held April 16-18 at the Chalfone-Haddon Hotel, Atlantic City, N.J.
- "Information Retrieval in Action" is the subject of a conference scheduled for April 18-20 at the Center for Documentation and Communication Research, Western Reserve University, Cleveland, Ohio.
- The 1962 Spring Joint Computer Conference, sponsored by the American Federation of Information Processing Societies, will be held May 1-3 at the Fairmont Hotel, S.F.
- "Electronic Information Display Systems" is the subject on an institute to be held May 21-25 at the American University, Wash., D.C.
- A conference on Self-Organizing Systems will be held on May 22-24 at the Museum of Science and Industry, Chicago. It is co-sponsored by the Information Systems Branch, Office of Naval Research, and the Armour Research Foundation.
- The Ninth Annual Symposium on Computers and Data Processing sponsored by the Denver Research Institute of the University of Denver is scheduled for June 27-28 at the Elkhorn Lodge, Estes Park, Colorado.
- The 1962 WESCON will be held Aug. 21-24 in the California Memorial Sports Arena and Statler-Hilton Hotel, Los Angeles.
- The 1962 IFIPS Congress is set for Aug. 27-Sept. 1 in Munich, Germany.
- The ACM National Conference will be held Sept. 4-7 at the Onondaga Country War Memorial Auditorium and Hotel Syracuse, Syracuse, N. Y.



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CIRCLE 14 ON READER CARD

EDITOR'S READOUT

THE CORPORATE IMAGES

Whether by judicious strategy or an injudicious lack of it, all corporations present a public face. Sometimes it is masked; often it appears heavy with mascara, rouge and similar accouterments of battle. Always it seems to smile with a noble, deistic expression, occasionally winking a fetching eye at the computing professional.

And since the public and professionals' view of the computing industry is based largely on a composite impression of individual corporate faces, it is important to consider the present appearance of these images even if a close, bright light may cast some unglamorous shadows.

Because several computer manufacturers quite unintentionally convey dual images while others may fit a single description, specific corporate identities for the following categories have been omitted. It is also felt that the game of matching a company to a description may prove an interesting sport of its own although for the majority of *Datamation's* readers, this obstacle will be of minor importance.

1. *The Virginal Goliath.* It is indeed difficult to provide an air of Godliness to a biblical villain. Nevertheless, the computer manufacturer with the largest single stake in the market focuses on purity as an image. While the company is well known for possessing highly capable personnel, good hardware and dependable backup, it is also the most common butt of all "in" humor. A substantial dichotomy exists between its public appearance and the professionals' view. Within the industry, it is looked upon as the roughest of competitors and some green-eyed partisans have fancifully suggested that Goliath "permits" other firms to market their wares seemingly as a benevolent concession to the watchful eye of the government. To the public, its highly varnished surface reflects a deep, golden hue untarnished except for occasional flecks of dust.

2. *The Unassuming David.* In contrast to Goliath, a pint-sized but money-making competitor has successfully played the role of gentle humility in the face of manly odds. Coupling its posture to a respectable line of hardware, its corporate image has continued to improve among sophisticated users while its public face has been comparatively unknown. The fact that it really is in business to wrench out a profit has become increasingly apparent during recent months detracting somewhat from its early virtue which prompted sideline viewers to root with much logical exhuberance.

3. *The Ethereal Spirit.* High atop a snow-covered mountain, research adorned with professorial labels, is as pure and sometimes as thin as the surrounding air, and while the sale of a product line is vaguely encouraged, the image conveyed is that a profit orientation is for the small folk residing in the crowded valley below. Inspiration and government money come only from above and propaganda to the contrary may be tainted with commercialism. The effect of this image has been substantial on the public and to a limited

extent, encouraged by several respected, non-drinking professionals.

4. *The Mighty Snoozer.* When the potential of an industrial giant far exceeds the present contribution of its computing division, its image becomes one of unflexed muscle to the public, nervous conservatism to competitors, and critical perplexity to professional observers. While sustaining the life span of a current line of equipment, sales are impeded by the prospective user's uncertainty of the corporation's future posture. Certainly, the image portrayed is not a desirable one. It *appears* favorable only in view of the enormous bank account accessible to and instrumental in rousing the snoozer.

5. *The Happy Loser.* The effect of a public declaration that one plans to lose substantial amounts of capital in gaining admission to the computing field, prompts onlookers to keep a close tally on how well the corporation is doing in this regard. The latest returns indicate all expectations are being satisfactorily fulfilled: machine sales are well below the breakeven point; r&d expenditures continue at a dandy pace, and the loser should be overjoyed at being able to predict his loss with such keen precision.

6. *The Unhappy Loser.* As distinguished from the happy loser, this corporation's management is anxiously concerned over unquestionably heavy losses particularly since its public image conveys all the classic ingredients for success: historic and technological leadership; a reasonably complete line of hardware; a healthy number of installations, and a fair share of capable personnel. Despite these niceties, the division continues to depress the profits of the corporation and computing professionals are well aware of its loss statements which strangely overshadow the firm's more classic virtue.

7. *The Brinksman.* Consistently on the verge of either leaving the computer field or getting into it, the public image is non-controversial and largely non-existent. To the professional, this firm has all the earmarks of a successful, early failure: rapidly shifting management, little if any capital, no prospect of expansion, and few customers. If for no other reason than sheer obstinacy, the brinksman has refused to close his doors and probably can't open them too widely. However, while onlookers may smile, there is no hearty laughter echoing from the galleries.

8. *The Immodest Newcomer.* Optimism abounds as the first flush of a seemingly fat pursestring prompts the most generous of promises and the most colorful of brochures. The public image is a rosy one at least within the confines of the city in which the corporation has been founded. The professional is skeptical but willing to wait patiently, at least for the first operating prototype.

This present grouping of corporate faces in the computing industry may be compared to a panoramic photograph of a junior high school graduating class. The general impression is certainly one of innocence, excitement and impatience with the photographer. A closer inspection of the print would reveal some freckled faces, a few smiles with well-braced teeth, and spotted throughout the group, an advanced sign or two of approaching maturity.

With the passage of time, virtually all of the faces will show marked changes although some will retain their freckles and others will remove their braces only to find that their teeth have not been straightened. For the majority however, it will be possible to reflect on the early photograph with an adult smile and only an occasional wince. ■

Because of the serious formative problems which ASA's X3 has experienced, its function as well as organization had undoubtedly become somewhat muddled to many *Datamation* readers. The following commentary may provide some stimulating clarification on this significant industry activity.

ASA's X3

a perspective

In the two years since the U.S. standards program for data processing was first conceived, not a single standard has been born.

Conception first took place in January, 1960, when a general conference was held to initiate an American standards effort for the data processing field. Following this meeting, the American Standards Association (ASA) established X3 as the committee to lead the U.S. effort with the Business Equipment Manufacturers Association (BEMA, formerly OEMI) designated as the project's sponsoring parent.

Despite the outward virtue of this arrangement and the apparent need for edp standards, X3's efforts have been generally hindered by both complex and highly sensitive machinations, resulting in an obvious void of specific accomplishment. Blocking progress have been the problems of controlling political in-fighting, personality clashes, resignations by key executives, duplicity of effort by numerous groups outside and inside the framework of ASA, and the delaying tactics of companies represented on X3 and faced with the unsavory realization that certain edp standards might injure their competitive position.

Throughout its stormy formation, X3 representatives have been fully cognizant of the fact that "voluntary" standards hastily derived would be useless if unacceptable by the majority of the industry. The formative problems had to be overcome before constructive efforts could be undertaken.

The present feeling of the group is that many of these "organizational" problems have been partially solved and a few have been eliminated. Initial progress in the formation of specific standards is very definitely underway. (see *Datamation*, pgs. 25-28, November, and pgs. 35-37, January) Today, the X3 committee comprised of six subcommittees, stands on the verge of performing a major contribution to the data processing industry and may be appropriately classed as the single, most important committee activity presently active in the field.

Despite its publicized function, X3 is considerably more than a group aiming at the construction of a set of voluntary standards. Its efforts represent a general unifying factor in the industry. Competitive manufacturers, business and scientific users, and various special interest groups are able to air their differences and evaluate the application of significant technical advances. For example, a realistic program for the compatibility of compiling languages is a function of X3.4, and the elimination of needless duplication in some r and d efforts is a result of the work in X3.1 which will standardize on type fonts for optical character recognition (OCR).

X3 also serves as a controlling factor in establishing the equality of manufacturers by rule of reason and contribution as opposed to economic weight. It has the pressing responsibility for the well-ordered maturing of the computing industry as opposed to present buckshot progress.

It is expected that the efforts of X3 will prove of a continuing nature hardly expiring after the first group of acceptable standards are introduced. Maintenance of standards will become an important function, and the spawning of new groups within ASA's basic organizational structure will encourage exploration of advanced areas for eventual standardization (i.e., the current work on problem description and analysis).

It is not expected that X3 will replace the function of such groups as the government's Committee on Data Systems Languages (CODASYL), the Data Transmission

Study Group, ACM's ALGOL committee, or the data processing studies of the Electrical Industries Association (EIA), but rather, it will serve as a top-level evaluative and action body surveying and encouraging implementation of the activities of others.

Since ASA is also the U.S. member of the International Organization for Standardization (ISO), standards approved by American member groups can be submitted for international consideration and vice versa. Recently, ISO Technical Committee 97 on dp standards was designated and the Secretariat assigned to the U.S.

Within BEMA, a Data Processing Group is composed of 20 member firms involved in manufacturing dp equipment. The DPG provides administrative and technical assistance for the standards program, with the aid of the DPG Engineering Committee.

In some areas of edp, standards will gain rapid ground such as in defining the physical measurements (ie., width and thickness) of a punched card. A second grouping is where the real accomplishments and progress of the committee may be measured such as in character sets, type fonts and electrical engineering specifications. It is here that the bias of manufacturers will become most apparent and some obstacles may prove impenetrable. Finally, in areas such as operating systems, the standards effort will find little usefulness since individual shops will decide on those characteristics most suitable for their own operation.

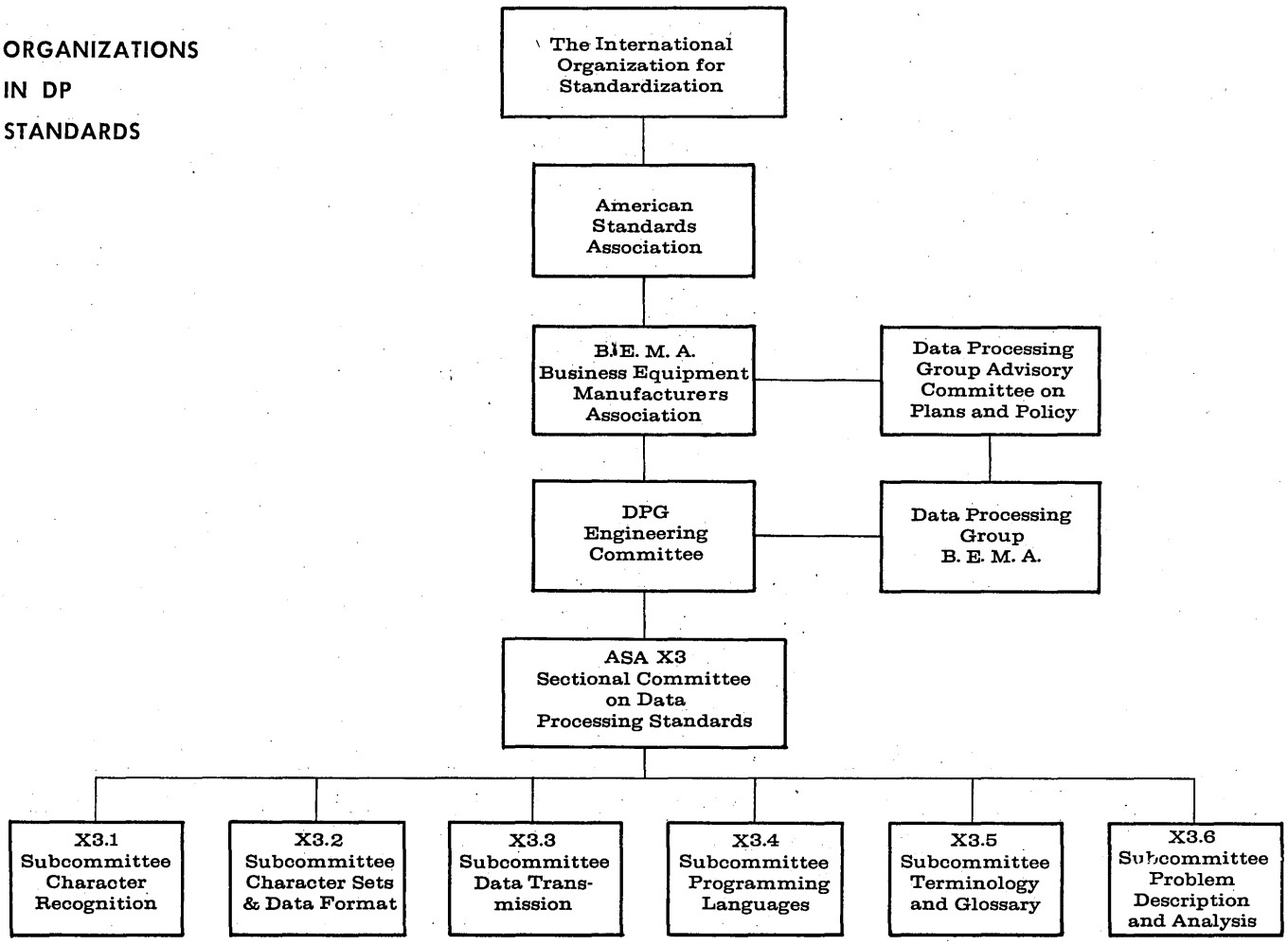
Since most committee members in X3 offer their time on a voluntary basis and are senior citizens in the computing community, they are also well aware of the source of their paychecks, the financial commitments of that source as well as the current direction of its r and d efforts.

Despite the nobility of their intentions, it is sometimes difficult to bite the proverbial feeding hand and committee arguments may therefore be based largely on a realistic concern for a corporation's financial investment as opposed to more technically sound, objective viewpoints.

It is unfortunate perhaps that an effort as important to the industry as standards could not be funded privately and subsequently obtain the talents of the industry's most capable professionals permitting them to deliberate in a less biased environment. While this suggestion would violate ASA's traditional operating procedures, it should be pointed out that in previous considerations, the general problem of setting a standard for an industry has not been confronted with the highly complicated involvements common to edp (ie., specifications for a screw thread are hardly comparable to standardizing on ALGOL).

Because the growth of the computing industry has been a dynamic one, many of X3's critics feel that the standards effort should be equally dynamic in its accomplishments and impatience with procedural considerations may prompt sharper criticism than justified. A more realistic point of view is that standards activities are by their very nature, methodical, plodding and subsequently, quite permanent in their effect. It should be clearly understood that the biases, politics and frictions which come to play and may seem to impede the effort, are in fact, expressions of legitimate interests which comprise one of the most important aspects of the deliberations involved in setting and maintaining a standard. ■

ORGANIZATIONS IN DP STANDARDS



CONTRACTING FOR COMPUTER SERVICES

some critical cautions for the prudent customer

by ROBERT L. PATRICK, Computer Specialist, Northridge, California

Commercial Service Houses (CSH) are springing up like weeds. They are endeavoring to fill a need in our technical society. Just what is this need and how do they fill it? A commercial computer service house draws customers from that section of industry which has requirements for computer science and technology but not in sufficient volume to justify an installation of their own. A commercial house also appeals to the military, who seem ready to admit that they can't cope with their expanding programming load. A service house also draws customers from other users who have an occasional overwhelming peak load which gluts their installed capacity. It is to the first two categories that this note is directed. Those in the latter category should know their own costs and hence have a comparison for negotiation.

Since those in the first two categories are not yet "in the swim," a note or two of explanation is in order. Although we in the programming field put our best foot forward and pretend to be able to solve the ills of the great unwashed, we have some problems of our own. If the customer is aware of those problems when he is negotiating with a vendor, then he is negotiating from a position of strength: both he and the vendor are aware of their mutual problems.

It is my belief that the most difficult unsolved problem in the field of computer programming is that of estimating requirements for programming services. Where a vendor has done a similar (or identical) job in the recent past, he can estimate his programming requirements accurately. With accurate estimates a vendor can feel assured that he can fulfill his commitments within the time and money allowed. If there has been a significant change in crew since the job was last done, or if the programming effort is ill defined and has never been done before, the CSH is completely without yardsticks to measure the task at hand or, in some cases, to measure their enroute performance after the contract is awarded. A customer should be wary! Just because a CSH has scheduled a manufacturing facility in the past, a *new* contract brings problems: data preparations, editing, scheduling, management review, and output formats are probably sufficiently different so that a reprogramming effort is required.

running time guesstimates

At one extreme of the spectrum, there are tasks which merely require that data is transcribed for an existing program and one or more computer runs are made. These *can* be estimated accurately. At the other extreme is the customer who has heard the audacious stories of the vendors and has the gleam of an application in his eye. Under these conditions, even a very experienced man can do little better than to guess that the task is small, medium, or large. To request that a computer programmer hazard a guess as to the running time on an application before the program is nearly written and checked out is to ask that he amplify his uncertainty about the program. Running time estimates on unspecified programs require some occult means usually awarded only to priests in good standing. In many cases the important facts are so befogged by an inexact or unclear statement of application that one cannot even determine whether the task at hand is computer limited or input/output limited.

The above is fact. One other fact should be acknowledged before we interpret any of them. The proper management of computer programmers is an unknown art! Every programming shop in existence somehow gets the task done. The programming shops which are buried within corporations are successful as long as they provide a service within the time constraints impressed upon them by the parent organization. They probably don't know what their costs are. In the field of contract programming the situation is woefully different. Once a contract is signed, the service house is obligated to strive and meet that contract within the committed bounds of time and money. Unfortunately the turnover and growth in commercial houses is severe (one CSH has accidently begotten three competing firms). Furthermore, the search for new

business is a millstone about the necks of the management of these houses. In addition, there is slight opportunity for programmers to specialize and really become efficient in a given area since they are required to be "expert" overnight in whatever contractural area they have been assigned. (Even John Von Neumann would have difficulty going from a program which determines optimum lunch meat mixtures to a real-time control task overnight!) When we consider this kaleidoscopic changing panorama, it is no wonder that the manager of a computer service house has difficulty meeting schedules and time commitments.

inside the house

Before we really inspect the posture of the manager of a commercial service house, we should know one or two more facts about his life. With one notable exception, commercial service houses are classically underfinanced. Consequently, the manager of a commercial service house is under heavy pressure from his own superiors to at least break even on each job. In addition, commercial service houses are undergoing a rapid maturity. With this maturity comes a rather rapid expansion. The profits of jobs are being poured into expanded facilities and sales forces in an effort to try and optimize fixed expenses for facilities, salesmen, management, and machines. The man who is actually doing the task in such an environment is quite often not truly an INsider, even within his own house. He is concerned about such mundane matters as tardiness, schedules, turnover (on a job basis), machine time schedules for checkout, and the changing nature of the problem. On the other hand, his management is concerned with potential mergers, corporate financing, public issues, contracts not yet signed, and the corporate image. Although a line supervisor may be sincerely interested in fulfilling the contract and its provisions, he may have difficulty in communicating his problems to his own management.

Having noted several salient facts about commercial service houses, let us now see how they effect YOU, the potential client. As in the Federal Income Tax, wherever a gray area exists in the problem statement, the service house man will interpret the problem statement in his favor. This is a ploy known as "baiting the hook." If the problem statement is not complete and accurate, the service house will interpret it such that it appears to be a smaller problem than it actually is, knowing full well that once the face amount of the contract is expended, additional monies will come from some reserve fund so that the work can be completed.

personnel checks

While many customers direct adequate attention to the rates charged for a given level of personnel (coder, programmer, or analyst), they fail to direct adequate attention as to how many analysts of a given class passed through the assigned staff during the course of the task (you shouldn't have to pay to train them all). Furthermore, it is questionable whether the men assigned during the latter portions of the contract have as good backgrounds, resumes, and customer acumen as the men who originally clinched the contract. It is merely good management on the part of the customer to request from the service house their standard job titles and salary rates for the various classes of personnel. Furthermore, a review of the resumes and an informal interview of those people assigned or to be assigned the contract will assure a customer that he actually gets a senior programmer if he pays for one. In addition, an astute customer should insist on parallel documentation for his own protection. From time to time, a programmer will take sick or undergo some other extenuating circumstances and will be relieved immediately.

In addition, due to normal attrition, turnover, and promotions within the crew, the staff will change. As a mere formality, a customer should request that changes in the membership of an assigned staff should be approved by him *in advance*. Furthermore, he should refuse to approve changes without an interview and the accompanying resume for the man to be assigned. While some commercial service houses will look upon this as prying into *their* business, a reputable firm should be delighted to comply. The time spent in such an interview is surely billable to the contract. A well written contract should stipulate that the replacement must be approved before the previous man can be transferred. A customer *should* be willing to undergo double billing for the same service and hence be somewhat in control of the overlap between two men. While the situation in a commercial programming house can and does change, excessive turnover is expensive to the contract. Judicious planning, so that expansion occurs when it does not appreciably damage an in-house contract, is merely responsible business.

planning requirements

Although the technical part of the programming itself may be a research or development endeavor, the management of the effort is not. After an adequate problem statement exists, it should be possible to devise a programming plan which states specific goals. A plan should also contain estimates of programming and machine time required to achieve those goals. It is possible to compare the invoices for programming services with these schedules. Furthermore, good management practice on a developmental item indicates that the programming plan should be reviewed and rescheduled when 50% of the calendar time has elapsed, and when 80% of the money has been spent. An astute customer will also require the vendor to notify him 10 days in advance of such a review meeting. This will cause the vendor either to stick to the plan, or amend it. In either case, the customer will be assured that the status of the work is being watched and that the overall time and money will be contained.

Occasionally investigations into new or unique areas will be accompanied by major revisions to the programming between early system test and first production. Every once in a while, something unanticipated crops up and the program just doesn't work. It must be revised. While this *does* happen, its incidence can be minimized by adequate management followup. A plan, laid out before the work actually starts, will cause the management of the service house to think through their manpower scheduling and not over-commit one or two key individuals. Jobs which were bid assuming unique talents applied at full efficiency will run over on both time and budget when these key personnel are doubly or triply committed within the same time period. As a further protection against this situation, the original contract can stipulate a level of effort for the talented individual and the invoicing for payment can be on a name basis. Consequently, the customer himself can follow up and determine whether the talented individual is actually being applied where and when his abilities were planned.

the fixed price contract

In a very few cases, the answer to the problems of turnover, training, and expanding environment is a fixed price contract. The customer should be careful, however, that he is sure of his problem statement before he enters into

a fixed price contract. If by chance one or the other or both parties fail to recognize a developmental effort, and make the mistake of contracting fixed price for such an effort, the quality of the product usually suffers. If the job were properly estimated (pure luck) and the contract was properly administered (darn good management) then the vendor can perform on a fixed price contract and still turn a reasonable profit. The customer should always remember, though, THE UNDERFINANCED COMMERCIAL HOUSE CANNOT STAND A LOSS. The quality or the extent of the work is pared to fit within the fixed price bounds.

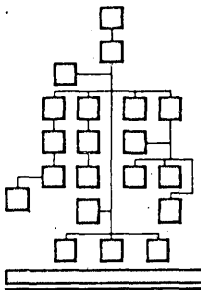
For their mutual protection, the contracting parties should discuss and agree on partial payments, acceptance, and final completion. Since the negotiator for the service house probably has more experience in these matters than the customer, the customer is usually at a disadvantage. If partial payments are to be paid, then some of the money should be held back until the acceptance tests have been met. If prompt or early delivery is desirable, then a bonus should he paid for early delivery. A portion of the held funds should be retained for tardy delivery.

If the service house needs the work, they are highly motivated toward delivering an interim product, partially documented, and replete with possibilities for improvement. On the other hand, if the customer is preparing to build his own in-house staff in parallel with *this* contract, then he should plan to pick up the maintenance of the procedure. He should willingly expect to pay for self-explanatory documentation and some overlap period so that his own staff can pick up the code from the vendor. Here is where a goal oriented contract is required. If the customer plans to let follow-on contracts with the service house for maintenance and improvements, then he should make this goal known during contract negotiations. The documentation requirements can be reduced somewhat, with resulting savings in his behalf.

the rate picture

I would be remiss if I did not just touch on rates for commercial computer time. In some service houses, the main frame rate covers some reasonable amount of off-line equipment usage at no additional charge. In other cases, the machine time rate covers the main frame only and the off-line equipment is an extra charge item. It behooves the customer to get these facts straight in his mind, and to know enough about his own job so that he can decide which type of machine time invoicing is to his advantage. Furthermore, he must expect to pay for priority, convenience, and first shift time. The actual dollar figure for machine time should be competitive with time sold on identical configurations or similar machines elsewhere. The cost of operating a large computer does not vary appreciably from locale to locale.

Last but not least, a customer who enters into a machine time contract at "cost" is obligated to carefully review the definitions of direct and indirect charges. Furthermore, a customer is being overly trusting if he does not upper bound the allowable contract "cost" by the highest standard commercial rate for similar equipment. To do less is to give the manager of the service house more control over his destiny than he deserves. ■



people IN DATAMATION

■ Charles A. Phillips, Director of the Data Systems Review Division of the Office of the Assistant Secretary of Defense, has resigned from this position as of Feb. 15 to assume the duties of Director of the Data Processing Group for the Business Equipment Manufacturers Association (BEMA, formerly OEMI), a post vacated last year by John Howard.

Phillips, a key figure in government data processing since 1952, is also chairman of the Committee on Data Systems Languages (CODASYL) and has been instrumental in the COBOL effort. He has been associated with the Department of Defense since 1948 and has been in the government's employ for 28 years.

■ Theodore Smith, former executive vice president of RCA's Industrial Electronic Products Group, is now in charge of the EDP division. Recent resignations at RCA include Donald H. Hunsman, division vice president and general manager of the EDP division; John J. Graham, division vice president-operations of the EDP division, and Francis J. Dunleavy, general manager of the Communications and Controls divisions.

■ Dr. H. R. J. Grosch, formerly with GE, CEIR and IBM, has established offices in Monte Carlo, Monaco, as a computer consultant.

■ Edward F. Canfield has joined Philco's Government Planning and Marketing Group, a newly created staff function. Canfield replaces Joseph M. Hertzberg who had been vice president of marketing for the former Government and Industrial Group. Hertzberg is now with RCA as vice president of defense marketing.

■ TRW Computers Co. has promoted John B. Neblett to the position of programming department manager and Margaret E. Brooks to assistant manager of the programming department. Neblett, who was formerly assistant manager in charge of the department's real-time programming group, will head the development of computer programs for use in industrial control systems and for the preparation and checkout of programs for specific customer applications. Mrs. Brooks was formerly in charge of the programming department's services group.

■ H. A. Shepard has replaced Dean W. Wooldridge as president of TRW on Feb. 1st. Wooldridge will continue to serve the company as a board member of both TRW and STL. He was president of the parent organization since 1958 when it merged with the former Ramo-Wooldridge Corp. Shepard was Vice President and General Manager prior to his recent appointment to the presidency.

■ Harold D. Ross has been appointed manager of the IBM Data Systems Division Development Laboratory in Poughkeepsie, N. Y. Ross, who has been associated with the company since 1949, was formerly director of Engineering Plans, IBM Corporate Staff.

■ Borge Hansen-Moller and Louis M. Ballard have been elected vice presidents of American Systems, Inc. Hansen-Moller will be responsible for planning and organization in the areas of finance and corporate growth, while Ballard will direct manufacturing operations.

HOW TO MAKE A COMPUTER APPEAR INTELLIGENT

"Five-in-a-Row" offers no guarantees

by JOSEPH WEIZENBAUM, Computer Laboratory, General Electric Co., Mountain View, Calif.

There exists a continuum of opinions on what constitutes intelligence, hence on what constitutes artificial intelligence. Perhaps most workers in the fields of heuristic programming, artificial intelligence, et al, now agree that the pursuit of a definition in this area is, at least for the time being, a sterile activity. No operationally significant contributions can be expected from the abstract contemplation of this particular semantic navel. Minsky has suggested in a number of talks that an activity which produces results in a way which does not appear understandable to a particular observer will appear *to that observer* to be somehow intelligent, or at least intelligently motivated. When that observer finally begins to understand what has been going on, he often has a feeling of having been fooled a little. He then pronounces the heretofore "intelligent" behavior he has been observing as being "merely mechanical" or "algorithmic."

The author of an "artificially intelligent" program is, by the above reasoning, clearly setting out to fool some observers for some time. His success can be measured by the percentage of the exposed observers who have been fooled multiplied by the length of time they have failed to catch on. Programs which become so complex (either by themselves, e.g. learning programs, or by virtue of the author's poor documentation and debugging habits) that the author himself loses track, obviously have the highest IQ's.

The program described in this article plays the game Five-in-a-Row, also known as Go-MOKU. This game is, to the author's knowledge, undetermined in the sense that no strategy other than exhaustive look ahead is known for guaranteeing a win or even a tie. In this respect it differs from Nim and Tic-Tac-Toe for which guaranteed winning strategies are known and have been programmed. On the basis of the criterion given above, the program certainly appears (to many observers) to make the computer behave intelligently. The fact that it permits its opponent to develop a position while paying close attention to its own development for a time and only occasionally becomes obviously defensive in its play helps to create and maintain a wonderful illusion of spontaneity. In fact, however, the program represents a simple algorithm as is shown below.

It is perhaps ironic that the author has never succeeded in beating the program and also that the program is being used as an automatic opponent (i.e. teacher) to certain learning programs trying to master its game.

The game can be looked upon as a generalization of Tic-Tac-Toe which, from this perspective, should be called Three-in-a-Row. An additional generalization is that whereas Tic-Tac-Toe is played on a 3 x 3 board, Five-in-a-Row is traditionally played on a Go board of size 19 x 19. The game is won by that player who first succeeds in placing five of his symbols adjacently and in a straight row (in any direction) on this board.

The fundamental strategy is that after a certain value is assigned to every potential move both from the point of

the player (P) and that of the machine (M), the machine chooses its next move by a technique based on these values which has for its aim the invalidation to the greatest extent possible of the planning of the player while optimizing its own advantage. The trick is in coming up with good evaluation functions and optimizing techniques appropriate to these functions. Once this has been done, refinements suggest themselves rather easily. Obviously, a prior problem is that of determining a terminology and a notation within which evaluation functions and strategies can be unambiguously described.

definitions

A *chain* is defined to be any set of five consecutive squares in either the horizontal, vertical, or diagonal direction. Every point is said to *anchor* four chains. For the point (i, j)* these are:

$$(1)\quad \begin{aligned} W(i,j) &\equiv (i-s,\ j) \\ NW(i,j) &\equiv (i-s,\ j+s) \quad (s=0,1,\ldots,4) \\ N(i,j) &\equiv (i,\ j+s) \\ NE(i,j) &\equiv (i+s,\ j+s) \end{aligned}$$

Thus every possible chain has a unique name. Every chain has two *values*, a P value (PV) and a M value (MV). The chain value is simply the number of P or M marks respectively which are to be found in the chain. A chain which has a P value is said to be *uninteresting* from the M point of view and vice versa. Clearly some chains are uninteresting from both the P and M point of view. Chains which are not uninteresting are *interesting*.

Every point (i, j) is said to *belong* to twenty chains. These are the chains whose values are affected if a mark were to be made at that particular point. The names of these chains for the point (i,j) are:

$$(2)\quad \begin{aligned} &W(i+s,\ j) \\ &NW(i+s,\ j-s) \quad (s=0,1,\ldots,4) \\ &N(i,\ j-s) \\ &NE(i-s,\ j-s) \end{aligned}$$

In addition, every point (i, j) is said to be *associated with* 32 points, namely those points different from the point (i, j) which form the union of all points which make up the twenty chains to which the reference point belongs. For the point (i, j) this set consists of the points

$$(3)\quad \begin{aligned} &(i \pm t,\ j) \\ &(i,\ j \pm t) \quad (t=1,2,3,4) \\ &(i \pm t,\ j \pm t) \\ &(i \pm t,\ j \pm t) \end{aligned}$$

position values

It is now possible to define position values for both P and M. These will be called P position value (PPV) and M position values (MPV) respectively. Judgment enters into the determination of algorithms suitable for their computation. Before describing a specific algorithm, however, the general manner in which position values enter into the strategy is discussed.

The P position value of an unoccupied position (i, j), i.e. PPV(i, j) is supposed to be a numerical measure of the utility of that particular position to the developing plan of the player of P. It must therefore reflect the extent to which P-interesting chains would be enriched were that move to be made by P. The way this is done is to assign a specific weight w(PV) to the four non-trivial possible chain values, and then to compute PPV(i, j) by simply summing the weights of all P-interesting chains to which the position (i, j) belongs. The computation of PPV(i, j) is therefore given by

$$(4)\quad PPV = \sum_{s=1}^{r} w(PV)_s$$

where s ranges over the r P-interesting chains involved. Similarly for MPV(i, j).

The function (4) is still quite general in that the weight assignment procedure has not been specified. Indeed, experiments show that quality of machine play is strongly dependent on weight assignment rules. Such rules are easy to state in tabular form. The table given below is that used in the game exhibited in this paper.

Chain Weight Table

Chain Value	Weight
1	5
2	25
3	80
4	1000

the basic strategy

Assuming a specific chain weight table, machine strategy is now quite straightforward. When P makes his move all relevant chains are updated. New PPV's and MPV's for the 32 points associated with the chosen point are computed and stored. Every empty point associated with any point which has a mark in it is considered a candidate for the next machine move. For each candidate point the number

$$(6)\quad N = K_1 PPV + RK_2 MPV$$

is computed. K_1 and K_2 (small integers) are parameters within the strategy. R is computed as described below. Thus the strategy has essentially five free parameters, K_1/K_2, and four weights which determine the chain weight table. It may be seen that the ratio K_1/K_2 constitutes an aggression coefficient. That is, its value determines how offensive or defensive a game the machine will play. Observation reveals, however, that human players vary the aggressiveness with which they play from move to move. They make this determination on the basis of an evaluation of the danger they feel themselves to be in versus the strength of their own position. This evaluation is approximated in this strategy by having the machine (when it is its turn to move) compute the ratio

$$(7)\quad R = \max(MPV) \,/\, \max(PPV)$$

and then multiplying K_2 by R for each of its moves. This means that if the machine's strongest move is much stronger than that of the player's next possible one, the machine will play proportionately more aggressively, and vice versa.

The point for which N(i, j) is a maximum (if there is one) is the machine move. If several N's have the maximum value, then the final choice of the move is made from among the maximum candidates on the basis of a random number generator. After proper updating of the appropriate MVs, PPV's and MPV's the player may make his next move.

Experience has led to the conclusion that an initial aggressiveness coefficient of approximately 1 is proper. Obviously, if the machine game is too defensive, then the machine follows the player's moves like a puppy dog, permitting the observant player to lead the machine play into traps. Too offensive a coefficient, on the other hand, permits the player to build combinations which remain unchallenged until it is too late.

The weight table exhibited above can be justified on the basis of the judgments that

a) An interesting chain of value two should have a greater weight than two crossing chains of value one, and

b) An interesting chain of value three should have a

*For definiteness, it can be assumed that the first mark made determines the origin of the coordinate system.

greater weight than two crossing chains of value two each.

These lead to the inequalities

$$8\,w(1) < 2\,[3\,w(2) + w(1)]$$

(8) and

$$2\,w(3) > 5\,w(2) + w(1)$$

which are satisfied by the table.

The weight w(4) is really irrelevant in the sense that a simple test can be made to determine whether the machine or the player has a chain of value four. If the machine has such a chain, then it completes it and wins the game. Any player chain of value four must be stopped under all other conditions. The weight table could take care of these matters. But when the machine is playing defensively and it and the player have an interesting four chain each, the machine will block rather than win. A "four test" fixes this difficulty simply.

The program displays an initial aggressiveness which is a manifestation of an overly naive goal directed behavior. The job is to make five-in-a-row and the program proceeds right to the task. In the beginning game, the player has, of course, not yet developed any position against which a defense appears necessary. This form of initial behavior on the part of the program gives the player an important advantage. A way to avoid this is to give the machine a stack of starting patterns to develop. Two or three moves would probably be sufficient to overcome the difficulty under discussion. Similarly, a number of "pattern detectors" could easily be built in. These would catch certain patterns which are known to result in winning combinations if completed.

A program implementing the strategy here outlined has been written by R. C. Shepardson of the General Electric Computer Laboratory (Mountain View, California). This program has been matched against players of various strengths. In general it has beaten novices even when it plays second.

An interesting sidelight on the apparent intelligence of the strategy described, is that novices seem to play according to the same algorithm as that on which the program is based. They continue to do so in many cases for some time. After many games, the novice suddenly makes moves in an entirely different way. He then begins to beat the system rather regularly. Evidence for these assertions is gained from analysis of the print-out of games played. Among other data, the move the machine would have made had it been in the player's position is printed out together with its position value. In many instances, the novice player chooses exactly that move as his own. To some extent the machine win can therefore be attributed to the machine's infallible bookkeeping. The player is finally confused by the mass of data generated by a long game.

The above comment lends to a possible modification of the strategy which should improve machine play. The program can be made to notice whenever the player departs from orthodox (i.e. programmed) strategy. This condition can be detected on the basis of the fact that unorthodox moves have low position values. Whenever this takes place, the machine should switch its play to the purely defensive and furthermore consider only points associated with the player's unorthodox move as candidates for its own response. ■

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WARSAW CONFERENCE ADOPTS ALGOL-60

Automatic Programming Committee established

From The Institute of Applied Mathematics, Polish Academy of Science, Warsaw

A working meeting on Automatic Programming Methods was held in Warsaw last Fall. About 60 participants took part in the Conference representing the Soviet Union, Czechoslovakia, East Germany, Hungary and Rumania.

The aim of the Conference was to consider theoretical and practical problems in the field of automatic programming, to get acquainted with progress in countries represented at the Conference, and to trace a common future action for this group.

Fourteen reports were presented and two panel discussions were held; one of which was concerned with problems connected with the international ALGOL language, and the other with address-free computers.

A demonstration of the SAKO automatic programming system which is similar to FORTRAN II, was organized at the Institute of Mathematical Machines in Warsaw. The demonstration was performed on the XYZ computer. Two mathematical problems were formulated by Conference participants during this demonstration. The first problem consisted in finding the root of a third degree polynomial. The second problem was to provide a tabulation of 100 values of a certain function in a given editorial format. Programs for solving these problems were written in SAKO, perforated on tape, translated into the resulting program and operated on by the XYZ computer. In both cases the performance time for all of these operations was under 45 minutes.

In the course of the discussion on ALGOL-60, many of its limitations were emphasized, as well as the complexity of its notations which suppress the popularization of the language among engineers, biologists, etc. In addition, numerous difficulties were indicated in producing an effective translator of the full ALGOL version. In spite of this, it was decided to accept ALGOL-60 as the basis for a standard mathematical language. Further development of this language was acknowledged as being necessary. It was pointed out that some work in this field has already been accomplished in Moscow and Nowosibirsk.

Besides the work connected with the realization of a possible full version of ALGOL, the application and propagation of simpler languages, already in use (for instance, the autocode used in Kiev, or the autocode SAKO) was also encouraged. The necessity of close cooperation of different scientific centers in countries represented at the Conference was emphasized.

For this purpose, a Committee of Automatic Programming was established, the members of which represent the various countries attending the Conference. The main task of this Committee will be to organize a mutual exchange of information and to establish contacts in the field of autocodes with other international institutions such as the International ALGOL Committee.

Finally, it was decided to arrange an annual Conference similar to the one held in Warsaw. It was suggested that the next Conference be held in the Soviet Union in autumn, 1962. ■

PROGRAM EVALUATION and REPORTING TECHNIQUE

a functional explanation of PERT

by HERBERT L. GROSS
National Cash Register Co., Dayton, Ohio

The PERT concept was originated in 1958 by a team whose members were drawn from U.S. Navy Bureau of Weapons, Booz Allen & Hamilton, and Lockheed Aircraft Corp. The technique had such outstanding success in achieving early delivery of the Polaris missile that industry at large has adopted it for many types of development and production problems.

Use of PERT requires an extensive analysis of an overall project, in order to list all the individual *activities,* or jobs, which must be performed in order to meet the total objective. These activities are then arranged in a network which displays the sequential relationships among them. This analysis must be extremely thorough and detailed if it is to be realistic, and it will require application of all the talents and experience available to the organization.

A highly simplified example of such a network is illustrated on the following page, showing the activities required for a specific project, and their relationships. The intersections between activities, which are assigned unique identifications, are called *connectors.** Each activity may then be identified by naming its front and back connectors.

Time estimates are made for each activity, and recorded on the network along with actual dates for scheduled start and completion of the project, as well as any intermediate target dates which may have been specified.

The entire network is then reduced to coded form, keypunched, and presented to the PERT program in the processor. The program summarizes elapsed time through all paths of the network, and identifies the *critical path*—the one with the greatest total elapsed time. The program also determines the probability of meeting each scheduled date, and of course indicates any dates which are impossible to meet.

The program also computes the probable date on which each activity will be completed, as well as the latest date to which its completion might be delayed without endangering overall completion of the project. The difference between these two dates is the *slack* in that activity. Those activities with the least slack are the most critical; they require close adherence to schedule, and it may be worth additional expense to expedite them. An activity with *Negative slack* is one which cannot be completed on schedule in this network.

If the critical path is unduly critical, the situation can

*The circles which mark the completion of one activity and the beginning of another are sometimes called "events." This appears to be a misnomer, since a connector like 2 in the example (marking the completion of two activities and the start of three others) actually represents five different *events,* not all of which need occur simultaneously.

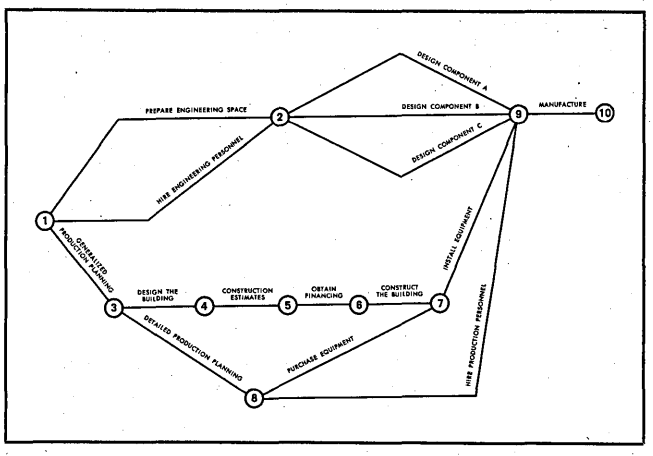
sometimes be corrected by reorganizing the network. If even a single activity can be removed from that particular path, and placed elsewhere, additional slack will appear in that path. Of course, there is always the possibility that the change will use up all the slack in some other path, and perhaps make matters worse, but that will be evident from the results when the processor runs the reorganized network.

An activity with substantial slack offers several courses to management:

> Alternative means of accomplishing the same activity more slowly, at lower cost, can be explored.
>
> Start of the activity might be postponed. If the activity, for example, is the hiring of personnel, there is no point in having a work force on hand before there is work for them to do.
>
> The slack in this activity might reveal that, by starting and finishing it promptly, a substantial (and perhaps unexpected) amount of facilities and personnel will become available to expedite some other activity which has little or no slack.

The use of PERT facilitates analyzing several alternative approaches to a project, obtaining realistic comparisons between costs and payoffs. As a result of initial analysis of a network, changes will be made and the problem recomputed, until an optimum schedule is obtained. As a project progresses, and some of the activities have been completed, the network may be rerun using the actual completion dates, yielding a revised projection each time.

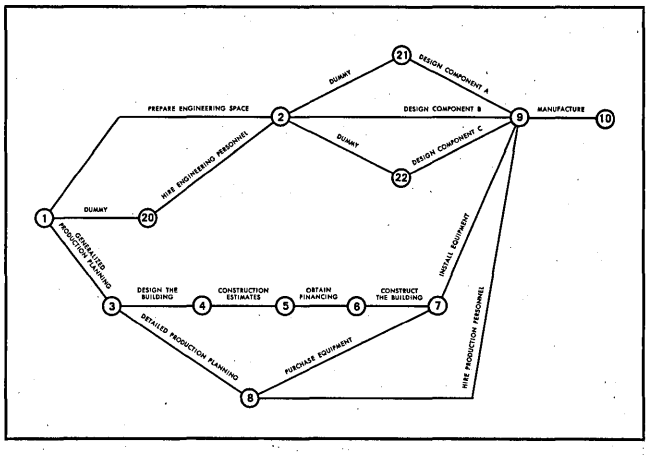
As an example of an activity network, consider the problem of designing and manufacturing a new product. Presently existing space can be made available for engineering and design, but a new building will be required for production.



This highly over-simplified network might actually be the first attempt at recording a real situation, but it requires a great deal of additional detail, and there are some obvious errors apparent in the network. It is impossible to begin *"generalized production planning"* until at least a certain amount of design work on the product has been completed; the design work on the three components will undoubtedly involve many activities not listed, and they are certain to be interlocked with each other and with other parts of the network; there is no mention of such a fundamental matter as procurement of raw materials; in fact, *"design–manufacture"* would represent an extremely naive conception of the production process.

However, any short example of an activity network must be over-simplified, and it is felt that this example will be more instructive than one which (although equally unrealistic) is superficially more plausible. Therefore we will use this network, as it stands, to illustrate our discussion.

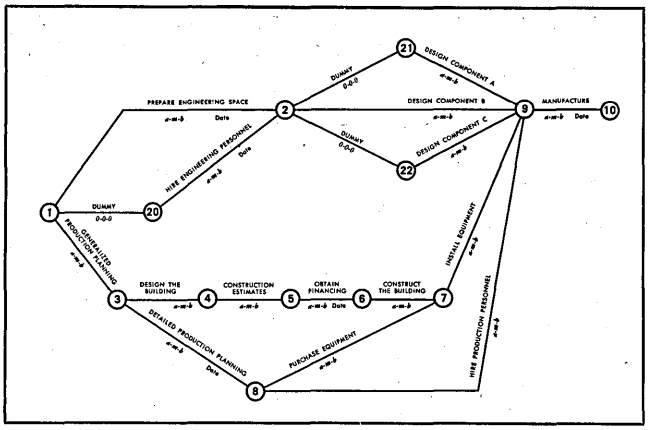
The first problem would arise from the fact that the network shows two paths from 1 to 2, and three paths from 2 to 9. When the network is coded for keypunching, each activity is identified by noting its front and back connectors, and this notation would furnish no way of distinguishing the parallel paths. In a realistic network (with hundreds of activities) the amount of detail, and the number of inter-dependencies, would make such parallel paths extremely rare, but they might occur. Such an ambiguity can be eliminated by combining the parallel activities, so that 1-2 would be a single path entitled *"Prepare . . . and Hire . . ."* but this is probably less desirable than inserting dummy activities (whose time estimates will be zero):



The next step is to add the estimates, and scheduled dates, to the network. Three different estimates are made for each activity:

(a) optimistic (if all goes well),
(m) most likely (expected time),
(b) pessimistic (if there is a run of bad luck).

Psychologically, the requirement that (a) and (b) must be estimated reduces the likelihood that (m) will be biased toward one or the other by the more or less sanguine temperaments of the estimators. And in the program, bias is further reduced by combining the three estimates into a weighted average. In addition, (a) and (b) also express the degree of uncertainty in the estimates. These estimates are expressed in weeks and (if desired) tenths of weeks, with fractions of a week expressed to the nearest tenth, according to the length of the work week.

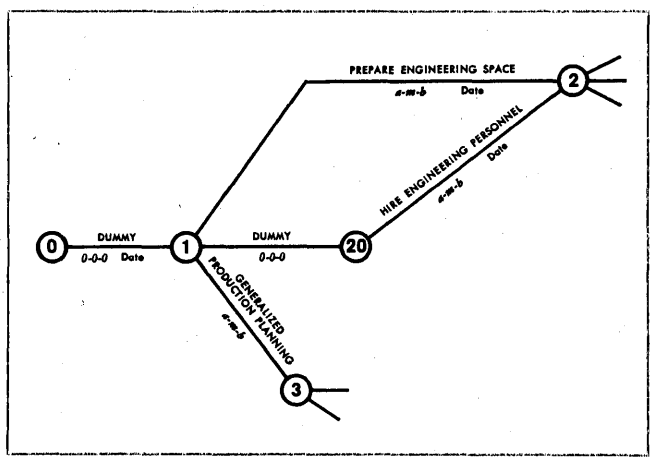


The symbols a-m-b have been shown on the diagram, representing the three actual time estimates which would be made for each activity. Three zeros have been entered for each dummy activity.

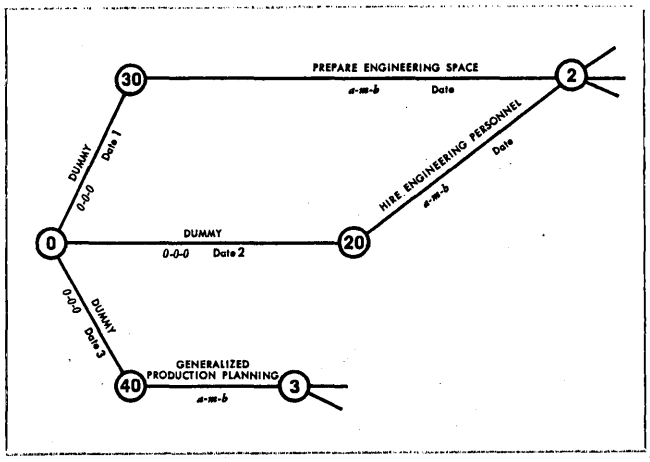
Although a scheduled date may often be specified for the beginning of some activity, in NCR PERT it is formally associated with the *completion* of an activity. Thus activity 2-9 may be scheduled to begin on a certain date; this date is entered for *each* of the activities 1-2 and 20-2 preceding 2-9, since the schedule *actually* requires that they both be completed by that date.

Although a network might have several end-points, it may have only a single beginning, which must be represented by connector zero. The initial activities may be represented in two different ways, depending on circumstances.

There may be a single scheduled starting date, which may be thought of as the date of approval of the project, and all the initial activities are free to start at that time:



Or there may be individual starting dates scheduled for each of the initial activities:



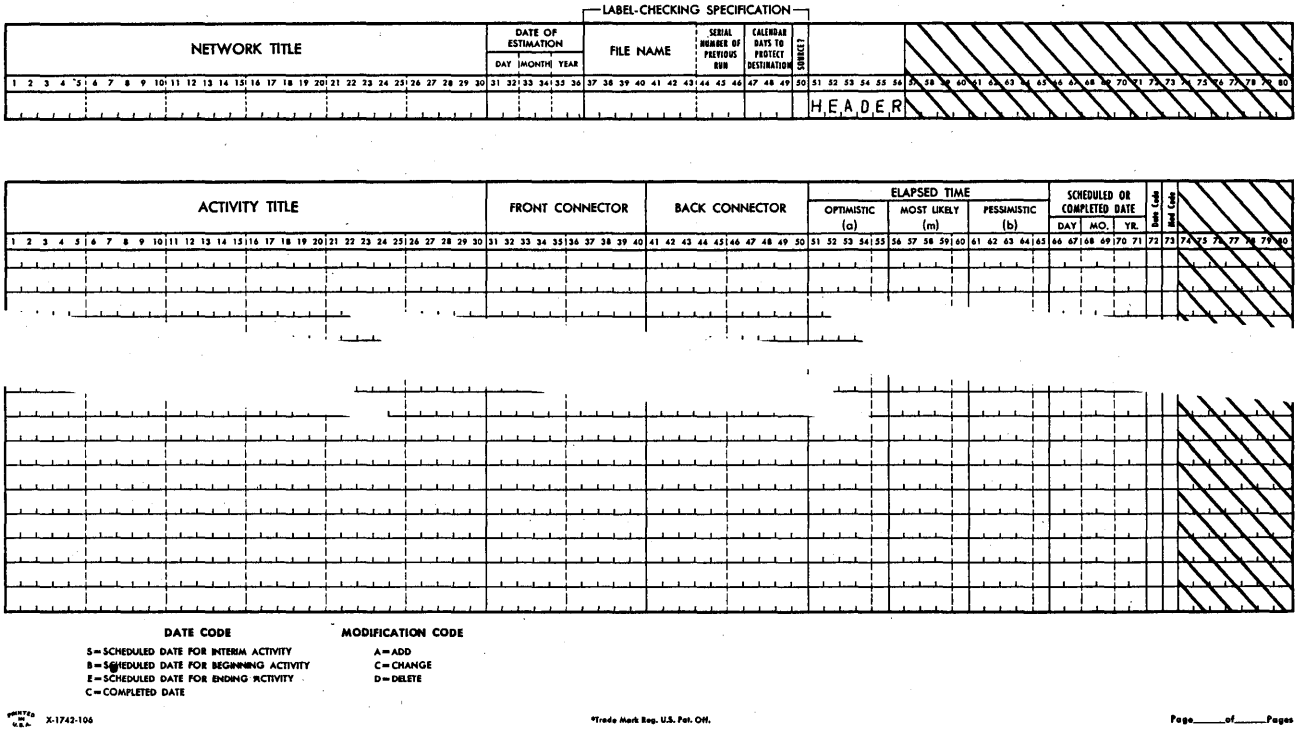
These additional dummy activities are required by the fact that, in the conventions of PERT, every scheduled date corresponds to the *completion* of some activity.

Once the network is complete, and all parties are satisfied that it is accurate, the activities are recorded on the PERT Input Sheet. Then the information is keypunched into either punched cards or paper tape, and input to the PERT program in the computer.

For subsequent runs, the user may add the changes and corrections to the original paper tape or card deck, or he may have preferred to discard the original medium and to have kept the magnetic tape transcription which the program provides. In the latter case, the program uses this transcription as primary input, and reads paper tape or cards only for the changes and corrections.

The output consists of a listing of the activities, in sequence by increasing slack. The activities on the critical path will head the list since they all have minimum, and equal slack. Also listed for each activity are scheduled date, expected time and date, latest allowable time and date, probability of completing the activity on or before scheduled date, etc. ■

PERT INPUT



DATE CODE

S = SCHEDULED DATE FOR INTERIM ACTIVITY
B = SCHEDULED DATE FOR BEGINNING ACTIVITY
E = SCHEDULED DATE FOR ENDING ACTIVITY
C = COMPLETED DATE

MODIFICATION CODE

A = ADD
C = CHANGE
D = DELETE

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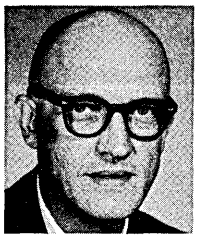
Page____ of ____ Pages

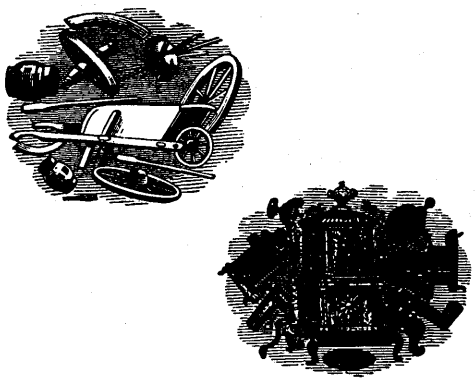
HOW TO DESIGN A KLUDGE

by JACKSON W. GRANHOLM,
Thousand Oaks, California



A phone call to Phineas Burling can be revealing. Phineas Burling is the Chief calligrapher with the Fink and Wiggles Publishing Company, Inc. Fink and Wiggles are, of course, the well-known publishers of the NEW MULTILINGUAL DICTIONARY. According to Burling, the word "kludge" first appeared in the English language in the early fifteen-hundreds. It was imported into the geographic region of the lowlands between King's Lynn (then Bishop's Lynn) and the Isle of Ely by Dutch settlers arriving there to reclaim tidelands of the Wash as rutabaga fields. These Dutch Settlers had been driven from their homelands by a great storm in the North Sea which swept inland over The Netherlands, greatly enlarging the Yssel Meer.

The word "kludge" is, according to Burling, derived from the same root as the German *Kluge* (Dutch *Kloog*, Swedish *Klag*, Danish Klφgg. Gothic *Klaugen*, Lettish *Kladnis*, and Sanskrit *Veklaunna)*, originally meaning "smart" or "witty." In the typical machinations of language in evolutionary growth, the word "Kludge" eventually came to mean "not so smart" or "pretty ridiculous." Today the leading definition given by the NEW MULTILINGUAL



is, "An ill-assorted collection of poorly-matching parts, forming a distressing whole."

It is in this latter sense that "kludge" is used by computer hardwaremen. Today "kludge" forms one of the most beloved words in design terminology, and it stands ready for handy application to the work of anyone who gins up 110-volt circuitry to plug into the 220 VAC source.

The building of a Kludge, however, is not work for amateurs. There is a certain, indefinable, masochistic finesse that must go into true Kludge building. The professional can spot it instantly. The amateur may readily presume that "that's the way computers are."

As an aid to young computer designers, then, it may be helpful, and a social service, to write down carefully, as Campylos[1] has done, some of the elementary rules for "kludgemanship" or "Designasininity," as Winchell has named it.

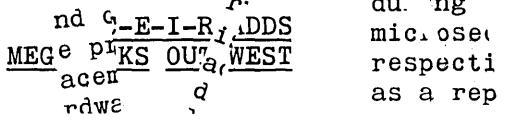
A word of caution is in order. One should *not* lash up an arithmetic unit, for example, which does not work. It must actually do arithmetic. The expert Kludge constructor will design his arithmetic unit to perform 2^{512} distinct kinds of addition, each called forth by opcodes six words long. None of these should, of course, be fixed point addition with sign and overflow indication. Overflow, in no instance, should be allowed to merely indicate something. It should generate a three-stage interrupt, preferably interrupting the computer in the next room, or, better yet, in the next plant.

The expert kludge builder will find ways to require three accesses to each of nine index registers in an instruction to query the real-time clock. With a little thought, he can cause automatic clearing of the upper third of memory in the event of an attempt to take square root of a negative number.

But it is in the lashing together of whole modules of equipment that the opportunity for applied kludgemanship présents itself to the hilt. Here, in what is often laughably called "interface resolution" there is an outstanding chance to glitch the user *without his even realizing it.*

Beginning with the most rudimentary of the I/O devices, the console keyput, the correct design approach is to use one of the standard, well-known electric typewriters, but to *alter the character set.* Of course, one chooses an internal machine character set different from that of any other manufacturer (after all, theirs are no good either)

and this internal character set must, at all costs, be *different from the one on the console keyput.*



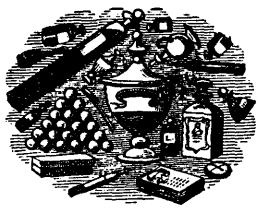
Moving on a step to cards, the field widens. Here one has a choice of card styles. It is *not* good taste to mix these. Do not go round-hole on input and square-hole on output. Stick to one or the other all the way. Use some more subtle device, such as formatting all card input in card-image and all output in Hollerith, or vice versa.

With magnetic tape the paths are well-charted. Use both odd and even parity, and as many widths as one can find reels for. Some special circuitry must, by all means, be designed into the tape connectors in order to make it, if not impossible, at least fabulously expensive to connect the tape machines of any other, second-rate manufacturer to your kludge.

Punched paper tape, in spite of its venerability and antiquity, is the latest hot diggety these days. Here is a great chance to go ape, for if the formats of cards are manifold, those of paper tape are megafold. The proper approach is to select a different one for each use, say four-channel on the input photoreader, nine-channel at the output punch, and six-channel as an auxiliary to the console keyboard. Give the user free a 28 foot-per-hour paper tape rewinder (set up for seven-channel).

Where drum and disc file function as auxiliary stores, there is room for application of some of the magnetic tape technique. But for a full discussion of kludgemanship applied to these and similar devices the reader is referred to the complete and comprehensive work, "Minimum Latencycraft and Random Accessmanship Applied in the Field" by Otis Remack.

The newer devices such as air-film floating cryogenic heads and tunnel diode delay lines are too much in the laboratory or R&D stage to be susceptible to concrete rules of use.



From the foregoing, though, the beginner should begin to form a picture of proper kludge building.[2] The essence of it is the designer who is so clever he outsmarts himself. The method lies as much in character set land and mishapen softwaresville as in techniques of solder and scope. The proper approach lies in producing a machine with maximum unforgivability. To go too far in one direction is to produce a completely impossible machine. To err the other way is to come out with just another ordinary computer.

Enoch Mote suggests the inclusion of a translation function in every hardware data transmission. By Mote's method, information standing punched in Hollerith hexadecimal will read into core in three's compliment form with bit order reversed.

Cicero Beam suggests a random hardware permuter built into every machine to add the contents of a random number table into all instruction regions in memory every 500 milliseconds on the even millisecond. But then, no one pays much attention to what Beam says.

The pricing structure of a machine is often a clue to its status as a kludge or quasi-kludge. Exemplary of the kind of thing one may expect to find is the following for a "basic" machine (Kludgevac 990B):

Central Processor	**$ 6200.00**	(month)
Console	**$ 500.00**	
Magnetic Tapes (8)	**$ 4400.00**	
Card Reader (1050 cards/min)	**$ 211.50**	
Card Punch (10 cards/min)	**$ 987.01**	
Data Channel (to connect all of the above together)	**$56800.00**	

Outstanding in this case is the exhorbitant money asked for the card reader.

The actions of management turn out to be quite important in kludge design, as, indeed, they sometimes are in other matters. It is sad, but true, that a kludge cannot be designed under just any old organizational structure. One of the most helpful of atmospheres in which a kludge may arrive at full flower is that of complete, massive, and iron-bound departmentalization. It is a good idea if the I/O men, say, not only are not allowed to speak to the main frame designers, but also that they have, in fact, never met them.

Interface crosstalk should, by all means be done by edict and directive (Beam says "ukase"), and not by memo and design note. After all, someone has to hew to the line on design philosophy, or people will go off in all directions. The "Project Manager," if there be one, should preferably be chosen from among the junior-ranking personnel of the Marketing Research Department.

Finally, and this is advice of the most sound sort, if it looks like, in spite of all efforts, your kludge will begin to resemble an ordinary computing machine, it is time to put more men on the job.

Whatever weird shape your final product may assume, after a year or so of careful kludgecraft, there is one thing to keep always in mind: Don't apologize for it! ■

NOTES:

1. Lucy Campylos, Secretary to Dr. Rupert B. Pooble.
2. The Author is indebted to Mr. Norman G. R. Sanders for permission to use his notes on "design glitches in the FRED Project."

A GAME TO COUNTER COMPILERITIS

the Compilogram from Burroughs

Compilation, that sane sounding link between problem-oriented language statement and internal computer jargon, may have to forfeit some of its mystery. The industry has produced many different breeds of compilers from the multiplicity problem statement languages developed to meet varying needs of individual computers.

The user, who must understand something of the basic compilation process if he is to appreciate its benefits, has been quietly pleading for someone to explain the generic cat.

Burroughs Corporaton has arrived at a means of graphically illustrating at least the basic process necessary for compilation. The company has developed a gimmick, yes, but a useful one, which employs a game format to take the interested party through sample ALGOL and COBOL problems to final creation of a machine language object program. Labeled Compilogram, the game materials consist of a playing board, about the size of a checkerboard, four decks of cards, an instruction manual and an answer sheet.

The game assumes the use of either ALGOL or COBOL as the source language. The reason is obvious – the Burroughs B5000 computer, due for first deliveries late this year, is advanced as one of the only systems that predicates its design and function on the use of problem-oriented languages. Since ALGOL and COBOL are the most commonly accepted in this classification, they naturally are the ones being tailored for use initially with the B5000.

Compilogram originally was contrived as part of the sales technical support package for the B5000 and, hence, the game specifically outlines the process of compilation in that computer. But because the game is merely a simulation of the B5000 compiling processes and since ALGOL and COBOL aren't the private property of Burroughs, the game does a wider service than stump for this company's computer.

People actually are discovering that a run through the game – it takes from 10 to 30 minutes to "compile" an object program from one of the problem card decks – gives them an appreciation of the process. The game can accomplish this basic understanding because it deals with the common objectives and function of compiling.

Compilogram takes the common elements of compiler function and rivets them to particular, visual examples. Although these are greatly oversimplified, the process which must be common to all compilers if they are to be effective, is quickly laid before the player.

Compilation or translation, of an object program from a source language program is fairly simple in concept. What the Compilogram reveals is that nothing reveals simplicity like an example.

The impediment to understanding of compilers is in the detailed job they are burdened with when the source language – ALGOL, COBOL, or whatever – is vastly different from the machine language of the computer. Burroughs claims that its B5000 machine language closely resembles the source program statement, hence a more natural working climate for the compiler.

Compilogram illustrates that, regardless of its application, the compilation process can and is being understood. This approximates a beatific blessing for those wandering in the noxious netherland of compileritis. To find the common or universal elements in compiling object programs automatically is just a part of the blessing. Actually being able to illustrate the concept is by far the greater benefit for the user.

The game begins with a stack of cards piled in a designated spot on the playing board. The player works his way through the deck, following the game regulations as outlined in the manual, moving each card through its logical path as indicated on the algorithm displayed on the opposite page. Sections of the playing board are set apart to hold cards during the compilation just as the computer would temporarily hold data and transfer it from one location to another.

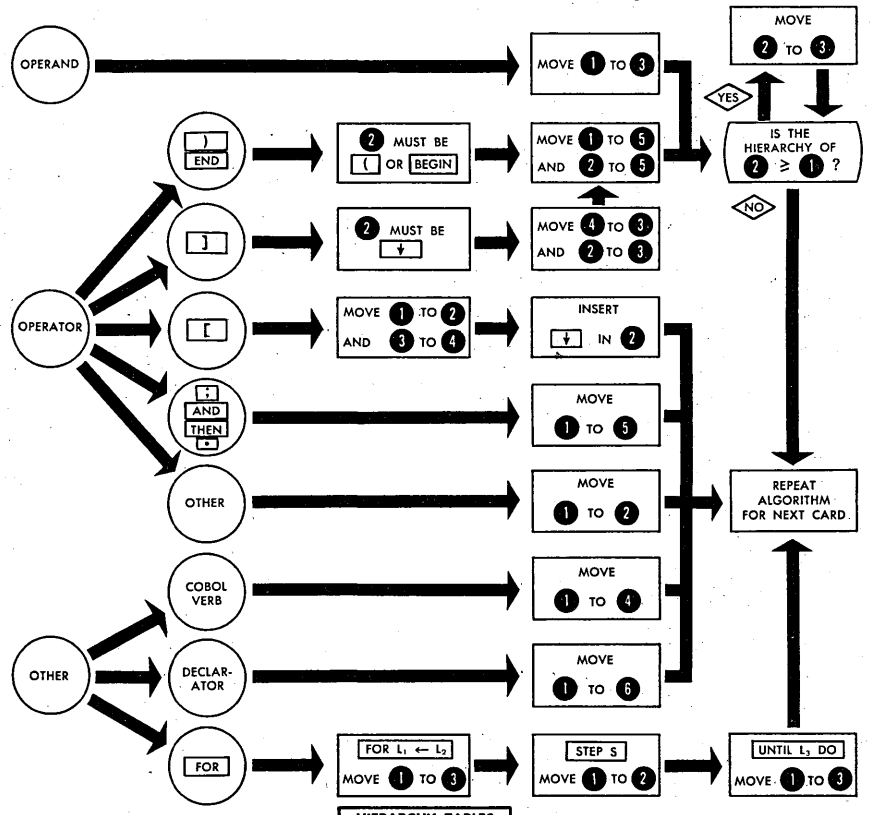
The final result is that cards containing information to be included in the compiled object program are arranged in sequence and non-essential cards are "stored" in their proper places.

Hardly the subject for pure fun for the family, Compilogram is nonetheless ideal for the serious student of compiling who likes a speck of sport with his education.

Persons whose business or professional responsibility necessitates an appreciation of compiling principles may write for the Compilogram package. Address requests on a corporate letterhead to: Sales Manager—Data Processing, Burroughs Corporation, 6071 Section Avenue, Detroit 32, Michigan.

Burroughs COMPILOGRAM™

COMPILATION ALGORITHM



HIERARCHY TABLES

	0	1	2	3	4	5	6	7	8	9	10
ALGOL OPERATORS	(BEGIN ↓	; END) STEP	IF ELSE	∨ THEN GO TO	∧	¬	≡ ≠ < ≤ > ≥ ←	,]	− +	× ÷ /	[

	0	1	2	3	4
COBOL OPERATORS	(	) ; IF . OTHERWISE	GIVING = GO TO EXCEEDS AND EQUALS (MOVE) TO IS GREATER THAN IS LESS THAN	(ADD) TO (SUBTRACT) FROM (ADD), + −	* (MULTIPLY) BY / (DIVIDE) INTO

	2
COBOL VERBS	ADD MULTIPLY DIVIDE SUBTRACT MOVE COMPUTE

SOURCE STRING

1 — B16 — A — OPERAND

OPERATOR STACK

2 — D44 — + — OPERATOR 3

POLISH STRING OBJECT PROGRAM

3 — B22 — > — OPERATOR 6

HOLD

4 — B29 — [— OPERATOR 10

DISCARD

5 — B1 — BEGIN — OPERATOR 0

PROGRAM REFERENCE TABLE (P R T)

6

- B2 — REAL ARRAY A [,] ; — DECLARATOR
- B3 — REAL Y ; — DECLARATOR
- B4 — INTEGER I, J, K, L M , N ; — DECLARATOR
- A2 — REAL ARRAY Y [ ] , — DECLARATOR
- A3 — (ARRAY) A [ ] ; — DECLARATOR
- A4 — REAL B , — DECLARATOR
- A5 — (REAL) C , — DECLARATOR

Since the preparation of the following commentary, the latest issue of the ACM's *Computing Reviews* has been received and features several highly favorable criticisms of DATAMATION articles. While we are duly appreciative of this fact, it does not mitigate the negative criticism voiced at some length by Sander Rubin in the September/October issue to which Dr. Grosch refers. And while we realize the possibility that Rubin may not speak for all ACM members, the inclusion of his volleys in an official ACM journal does imply an open invitation for fair game hunter Grosch's occasionally barbed delicacies. It is DATAMATION's belief that all expressions from our editorial contributors which appear well-written, relevant to the computing profession and in this instance, entertaining as well, merit publication and the critical consideration of our readers — *The Editor.*

WHO'S

by DR. H. R. J. GROSCH,
Contributing Editor

Well, well—here we go again! I must admit I welcome the chance to take a few long range swings at ACM (long range, because I'm writing this on a rainy Sunday afternoon in Paris). But I really had thought that the battle between the Reform Party and the Die-hards—between dollars and scholars, as it were—was subsiding. You know: the tumult and the shouting dies; the captains and the Carrs depart!

But in the September/October *Computing Reviews,* hidden away in an unlikely corner on optical scanners, one Sander Rubin calls lovely old *Datamation* the "yellow press" of technology! I can just imagine Hal Bergstein and the other Thompson Publications people crooning "Big Bad John," and crossing their fingers when they come to the place where the roof caves in. Perhaps they plan to take a position on Rubin's attack themselves; in any event, a few ripostes will add to the excitement.

Rubin begins with a critique of the controlled circulation magazine concept. Because most copies go free of charge to people who "might" patronize its advertisers – I would prefer to say, to people who *claim* to be able to do so – the editor of such a periodical, he says, has to consider advertisers first and readers "secondarily." On the contrary, my abrasive friend! It's ACM that has the captive audience; every member gets the *Reviews* whether he wants it or not, and he pays for it whether he wants it or not – by an increase in dues! If *Datamation* readers don't have enough interest to fill out the "I'm qualified" renewal form, or to fork out cold cash, the carefully

audited circulation drops, and so does the advertising rate. *Datamation* prints what it thinks its readers want; the ACM prints what its editors and referees want. And dry fare it is!

Datamation often misses the mark, I'm sure, although Sandy, and now Hal, try hard. But their aim is to build reader interest and participation. Many of us contributors, and all of the commercial outfits that send in material, are looking for monetary returns. But that is out in the open, clearly understood by every reader. No whited sepulchers, we. The publisher and the editor are hungry types, but their incomes depend on the mailing list. That's what brings in the advertising!

Rubin concedes that the Yellow Peril serves a useful purpose by keeping readers "superficially and relatively painlessly informed" although its articles are "quite inadequate to the needs of the specialist." I note the rather condescending tone, but nevertheless this is a fairly accurate statement. We are not offered articles on the convergence rate of Lafayette's method of inverting a matrix of quaternions. But with typical Diehard perversity this criticism omits a much more important aspect: ACM is supposed to do this itself; it's an officially approved function, and the vehicle is the *Communications*. *Datamation* and its trade competitors flourish because Al Perlis is not permitted by Editorial Board policy and by ACM finances to run a really competitive journal. Remember the big howl two years ago when *Datamation* published the second Rand invitational discussion? That discussion claimed, among many other disparagements, that ACM was dead from the ankles up. Could it have been published in the *Communications*? I doubt it; Al says yes, but I doubt it. Yet with all its rigidities, the *Communications* is the best read and the only eagerly awaited ACM publication.

I take particular exception to the claim that *Datamation's* articles need no "originality or aptness of thought." On the contrary, the articles need them and the editor solicits them. And I'm sure Al Perlis would claim that the *Communications* also strives for such. There are more kinds of originality and aptness, Sander, than are dreamed of in your philosophy! Indeed, if a dreary reworking of ancient technical furrows and an avoidance of "over-colorful language" (see Review 1050) are the marks of the professional, Rubin himself fails the test. Welcome to our ranks, dear boy – you have wiped the ACM's collective eye by sneaking a *Datamation*-type article into their most austere columbarium! I wish I could think you did it on purpose.

In several of his reviews Rubin complains of articles lacking solid new factual substance. But in an adjacent review, 1067, written by an inmate of what one might describe as that hotbed of purity, Chapel Hill, we read two-thirds of a column on AMOS IV without discovering who designed or built it! Here, though, the critic does have a point. The issue he censures in such detail had an awful lot of undigested press release material in it. Besides, three nearby reviews by others (1061, 1062, 1065) make the same complaint about EJCC papers. Even the professions nod, it seems.

In Review 1052 Rubin points out the article under consideration could be read more meaningfully if the author's job title were given. How true—and how much *more* true of the reviews themselves, which by a slavish copying of *Mathematical Reviews* identify the reviewers only by their (home?) residence. This is the same kind of reverse snobbery that leads Harvard professors always to refer to themselves as "Mr."! I probably know who Sander Rubin is, but sitting here in a hotel room thousands of miles away from my reference material, I would value something more than "East Orange." OK, so he has beautiful sunrises—but what does he *do*?

Kidding aside, though, he sure does at least one thing: he criticizes clearly, vigorously, and colorfully. However, the magazine doesn't look to *me* as though it is a catspaw of the manufacturers and other advertisers; if it looks so to others, or if they want something changed, they should let the editor know. They can write privately if they choose, or by all means for the letter columns.

I now pass from the defensive to the offensive (yes, I know one usually says "defense" and "offense," but let it stand.) The great unwashed may be interested in how a really "professional" journal operates, and what goes on behind the scenes at the ACM Kremlin. By "great unwashed" I mean all those who, lacking Ph.D's, move their lips as they read ALGOL (I have the union card, and I move *my* lips—but only because I can't keep a straight face!)

In a recent issue of the *ACM Journal* a nice article appeared on automatic indexing. It was padded out with some entirely irrelevant probability equations, left over from an earlier article perhaps, but basically it described a valuable and interesting experiment in information retrieval. I enjoyed it very much—one of the better things in a pretty good issue, I thought. Then I noticed something curious, something disquieting. The article was a reasonably formal one; it carried the usual scholarly apparatus of footnotes and references and bibliography. But nowhere, in the body of the article or in the academic artifacts, did it mention the automatic abstracting work of H. P. Luhn of IBM. Now Pete Luhn is the daddy of this whole field, but more than that, this particular experiment simply applied the original Luhn technique to an adjacent problem area.

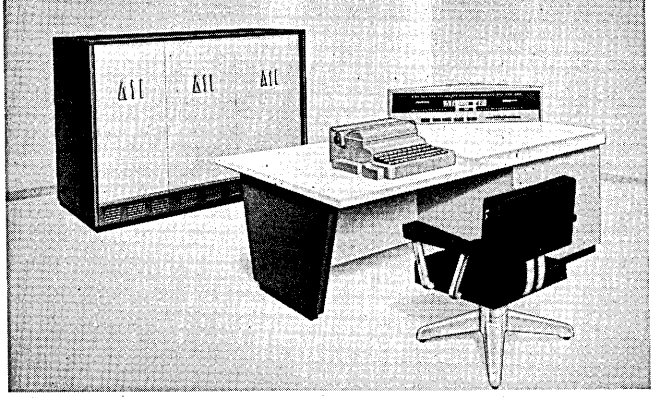
So for once I followed Diehard protocol—much good that it did me! I wrote the editor, Mario Juncosa, and asked him to put in the letters column of the *Journal* a good loud protest from me on the matter. The protest not only called attention to the solecism, but expressed surprise and annoyance that the editor and his referees had not corrected it. And I sent a copy of the material to George Forsythe, who is chairman of the ACM Editorial Committee.

Mario refused point blank to publish my letter. He didn't like its heckling tone, he said. Moreover, he had discussed the substance of my protest with the author, who rather conveniently happened to have an office just down the hall, and had been assured that he—the author—was just a little wooly lamb, and could he—the author—please have the reference to this man Luhn's work so he could check further. Aggh!

So I wrote again, again with copy to George, saying essentially: "Put my letter in, and a reply from the author if he cares to make one. I'm serious!" And this time I got the treatment. I musn't quote the whole reply, of course, but it ended: "We are still awaiting the appropriate relevant reference which you may wish to supply in support of your position . . . Awaiting your cooperation in supplying us with this desired information which will terminate this trivial exchange . . . Mario." I got the message—from Mario, that is. George didn't even bother to answer.

Well, that's how the "real professionals" operate. Personally, I prefer the *Datamation* approach. None of this cloak-and-dagger bit; no pharisaical pulling aside of the garments; no little cliques passing the goodies from hand to hand.

Maybe we have to operate this way—criticize *Datamation* in ACM publications, and ACM in the trade press. But it would be far more logical to appeal to the pertinent reader group, and not criss-cross. I think *Datamation* would have published Rubin's comments: I *know* the ACM woldn't print mine! ■



THE 210 & 420

new hardware from ASI

One of the newer entrants in general purpose computer competition is Advanced Scientific Instruments, Inc., Minneapolis. ASI is currently in production on two solid state models, the 210 and 420. A third computer, the Advanced II, is in the development stage.

Basic cost of an ASI 210 is $94,000 (4K core memory expandable to 8K at a cost of $116,000), and for an ASI 420, the basic cost is $324,000 (8K memory expandable to 32K). Applications are in the scientific and engineering fields as well as in data reduction and real time process control.

Word length of the 210 is 21 bits with the arithmetic system in fixed point binary. Add time is 10 microseconds, divide and multiply times are 56 microseconds, including time for indexing, memory access and I/O channel memory reference. The 210 has one index and one operand address. Total memory cycle time is two microseconds, and there are 32 instructions including multiply and divide.

Computation and data transfer can be simultaneous because of I/O channel buffering. Minimum transfer rate is 30KC. With the machine halted, the transfer rate is in the 160 KC range.

The 420 features include stored program, parallel operation and a 42-bit word length (seven characters). It has two buffered I/O channels with a minimum total transfer rate of 125,000 words per second. I/O channels are expandable to six and may be used for off-line operation.

In indexing, every memory location may be used as an index register, and successive indirect addressing is possible with indexing at each step.

A number of the instructions to the ASI 420 are automatically repeatable using operands from consecutive memory locations until a specified limit is reached.

A checking feature is built-in trapped program interrupt. Logic circuits which sense interrupt events can be armed or disarmed under program control to "jump" the program into various subroutines.

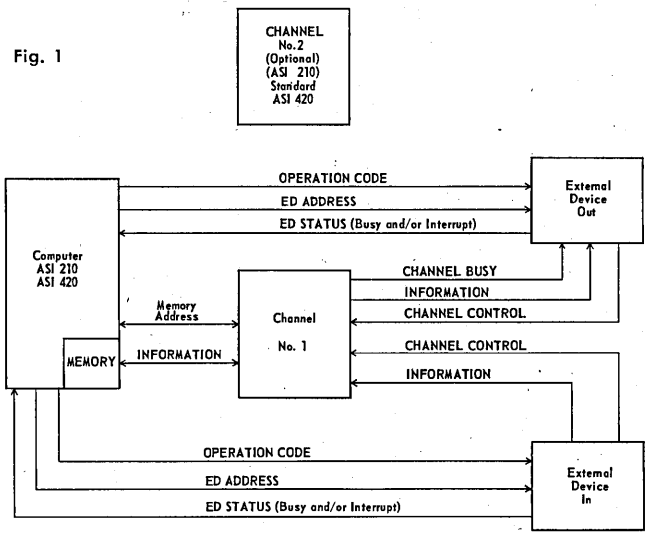
Memory cycle time in the 420 is two microseconds; add time is six microseconds (10 microseconds, including memory access time, indexing and I/O channel memory reference); multiply and divide times are 98 microseconds, including memory access, indexing and I/O channel memory reference.

Transfer of data to or from the computers is conducted via I/O channels which communicate directly with the memory of the 210 and 420. The I/O channels are buffered and have an average transfer rate of more than 30,000, 21-bit words per second in the 210, and 125,000, 42-bit words per second in the 420. There is one buffered channel in the 210, with an additional channel optional. The 420 features two buffered channels with four additional channels optional. In both units, access to the memory time is shared between the operating program and the I/O data transfer.

In the 210, a typical situation allows approximately 15 per cent of the memory time for I/O data transfer. In the 420, about 33 per cent of the memory time is available. Since the arithmetic and control function of the operating program do not require access to the memory during every computer cycle, both computers may proceed simultaneously in I/O data transfer with little or no loss of speed. Both computers can accomodate up to 64 on-line external devices, and the I/O systems are provided with program interrupt features.

In the simplified block diagram of ASI's control system (Fig. 1), the external device (ED) always senses the external device address lines to determine when it is being addressed. Except for this, no external device loads an I/O line unless it is addressed.

Fig. 1



The EXTERNAL DEVICE CONTROL WORD (ED-CW) is present only during the ED instruction in the computer and when the address and operand are transmitted back to the device which if not "busy," sends a "start" signal to begin operation.

In general, the amount of data transferred and memory locations employed are determined by a computer assembly instruction. Once an external device is placed in action, the information transfer is irrevocably under the control of the ED until the operation is completed. At this time, the ED may cause an interrupt, i.e., COMPLETED OK, COMPLETED FAIL.

In each standard I/O channel, there are a word length assembly register, assembly register in-out gates, and timing and control logic.

The external device start signal is received and the

channel I/O line is placed in the "in" condition, the "clear" line is pulsed to insure normalization of the I/O channel logic and the first data character is placed on data "in" or information lines. The channel timing and control logic operates the assembly register I/O gates, initiates the required communication with memory and provides control communication with an active external device. The last word will be stored in memory at the end of transmission.

The control lines of the external device "OUT" line are similar to the "IN" device or ED.

If a previously specified operation of an external device or I/O channel is not complete at the time it receives its next instruction, a "busy interrupt" will occur. This results in a "jump" to a fixed location which may lead to a busy routine. If the channel is free the I/O line is placed in the "OUT" condition and the "clear" line is pulsed to insure normalization of the I/O channel logic. The channel timing and control logic keep the external device line open while data is being sought from the memory and then it is fed to the external device which takes over until the instruction is completed, at which time an "external device interrupt" or "stop" occurs.

Both input and output have "verify" signals which essentially define the period during which the actual data transfer to or from the assembly register and memory occur. These make possible closed loop data transmission systems.

The standard mode of I/O data flow in the 210 is by sequentially transmitted six-bit octal or alphanumeric characters. These characters are assembled into 21-bit computer words by an I/O assembly register (B), one of which is employed for each I/O channel. In addition, each I/O channel is provided with two 13-bit address registers. The address register (BM) defines the beginning location, and the limit address register (BL) defines the limit location in the core memory into or from which a block of data is to be transferred via the particular I/O channels.

The address register (BM) always contains the address of the memory location involved in the data transfer operation. BM may be loaded or stored by the computer program through the use of an assembly register (B) instruction. Each time a word is transferred by an I/O channel, the content of BM is automatically increased by one. Thus an external device will communicate with memory locations in numerical sequence starting with the location specified by BM at the beginning of the external device operation. (See Fig. 3)

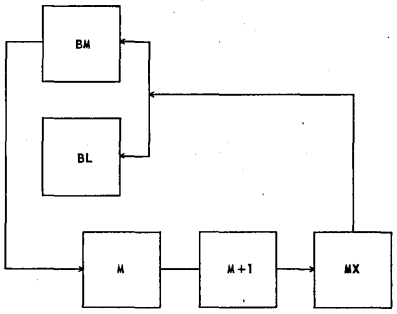


Fig. 3

The Limit Address Register (BL) contains an address which is always one greater than that of the last memory location intended for a particular block data transfer by the respective I/O channel. BL may be loaded by the computer program through the use of the assembly register (B) instruction. BL cannot be stored.

In typical usage, the computer will load BM with the address of the first location in a sequential block of data and load BL with the address of the location next in sequence, *after* the sequential block of data. This is accomplished by two applications of the assembly register (B) instruction. The program may then instruct an external device on the particular I/O channel to perform the desired data transfer. The external device is commanded by the use of the external device instruction.

If the external device is capable of transferring any specified number of words, it will begin with the memory location specified by (BM) and continue through location (BL)-1. Since BM is augmented after each word transfer, (BL) will not be involved. If the next block of data is intended to involve the memory locations next in immediate sequence, BM need not be loaded because it will be at the appropriate starting address; however BL must again be loaded with the new limit address. Only one use of an assembly register (B) instruction is required in this case.

In the ASI 420, the I/O data flow is basically the same as in the 210. Assembly Register (B) is 42 bits in length, and the BM and BL registers are 15 bits each.

In the EXTERNAL DEVICE CONTROL WORD (EDCW), the appropriate channel number must be specified. Thus, it becomes part of the external device address. In this sense, the most significant three octals in the EDCW will become the external device address. The channel number is also necessary to the computer logic for the proper manipulation of the "short format" provision of the EDCW. By this provision, the "start address" (operand address portion of the EDCW) may be loaded in BM at the same time the external device is commanded. When applicable, this provision obviates loading BM with an assembly register instruction. The "short format" mode is specified when bit 32 in the EDCW is a "one."

The two I/O channels may transfer data simultaneously, and access to the main memory and the arithmetic unit is on a time-sharing basis.

Every external device in the 210 and 420 has a unique memory location for program interrupt. The interrupt sequence is as follows: the address portion of the EDCW is fed from the memory address register and the operand is fed from the assembly register (commutating in/out gates) W (see Fig. 2). to register C to form the EDCW for external device operation. The external device address is transmitted through the interrupt control to the external device control logic. The external device operand also is fed to the external device.

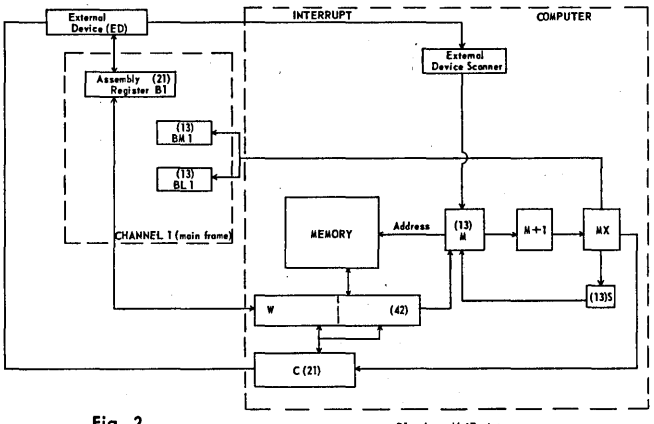


Fig. 2

( ) = No. of Bits
Channel 1 located in main frame of computer
Channel 2 optional in ASI 210 - Std ASI 420
BM = Address Register

B1 = Assembly Register
W = Double Length Assembly Register
BL = Limit Address Register
C = Arithmetic Register
M = Memory Address Register (console)
S = Program Sequence Register (console)

With the exception of the time during which the external device instruction is being transmitted, the interrupt control causes the external device scanner to be transmitted

on the 6-bit external device address lines. The scanner counts through all external device addresses in sequence. Each time the scanner addresses an external device, it constitutes an interrupt interrogation. If the particular external device desires an interrupt, it responds on an interrupt response line. The computer logic determines the following events when an external device is addressed by an instruction or by an interrupt:

1) Instruction:
   (a) ED not busy. Send "start" to ED. Continue program.
   (b) ED busy. "B" interrupt" if trap is set.
2) Interrupt Interrogation:
   (a) No response on interrupt response line. Continue scanning to next ED in sequence.
   (b) Response on interrupt response line. ED interrupt with jump to location specified by scan counter (ED address) if trap is set.

The trapped program interrupt is a special feature of both computers. Some of the events which can cause the program to be interrupted are: Busy, Add Overflow, Fault, Operator, External Device and Index Overflow.

An interrupt trap associated with each event may be set under program control to either respond when the event occurs or to ignore the event. Bits 11 and 10 in the operand address designate whether the traps will be armed or disarmed and bits nine through one of the operand address specify which traps are to be armed (set) or disarmed (cleared). If bit 12 of the operand address is present, the condition of each of the traps will be stored in the operand address portion of the register A (Accumulator) in the bit position that corresponds to the designating bit for that particular trap in the trap instruction. This stores the original trap position and is useful in subroutines that require use of traps but which must return these traps to their previous conditions at the end of the subroutine.

By specifying bit 13 in the trap instruction, the contents of Add Overflow and Index Overflow in the 210 plus Exponent Overflow in the 420 may be stored in the bits of A (Accumulator) corresponding to their trap designators.

If a particular trap is set to respond to the occurrence of an event, an interrupt is initiated when the event occurs. The current instruction will be completed and the address of the following instruction will be stored in the interrupt fixed address. Control is then transferred to the fixed address of the event causing interrupt. This will usually be a "jump" instruction to a subroutine that is usually an established subroutine; this means that no decoding need be written by the programmer. At the end of each subroutine a "jump" to the interrupt fixed address occurs and the program continues.

Only a priority external device may interrupt an interrupt subroutine. (If a priority external device has interrupted an interrupt subroutine, the clearing of the interrupt routine flip-flop will be inhibited at the end of the priority external device interrupt subroutine.)

The ability to selectively arm and disarm traps gives the programmer complete program control over either initiating an interrupt when a particular condition occurs or ignoring its occurrence.

Figure 4 is the flow diagram of an I/O routine with a single external device instruction. A busy interrupt will occur if an external device is instructed to do something which it can't do either because the device or its assembly register are busy. This interrupt may also occur if an assembly register instruction addresses a busy channel.

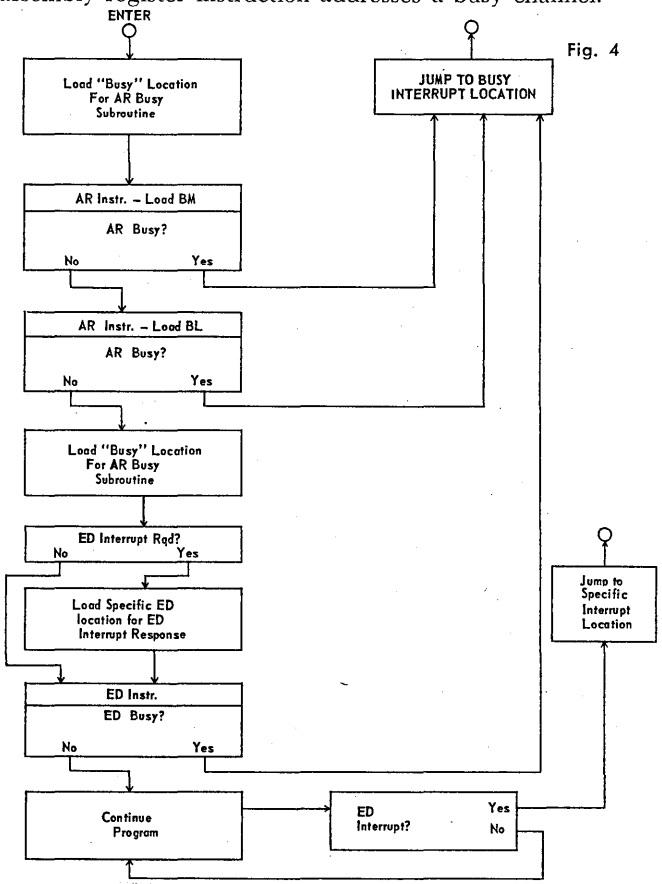


Fig. 4

An external device interrupt will occur when an external device sends a signal to the central computer that it has completed its assignment. There are also provisions for two interrupt routines associated with a particular external device: one for normal interrupt and one for failure. ■

American Management Association

Eighth Annual Data Processing Conference And Exhibit

FEBRUARY 26, 27, 28, STATLER-HILTON HOTEL, NEW YORK CITY

MONDAY MORNING — SESSION ONE — GRAND BALLROOM

9:30- 9:45	Conference Opening
9:45-10:00	Introduction
10:00-noon	Keynote Panel:
	Increasing Corporate Profits — Using management information systems for integrated planning, decision-making and control.
10:00-10:15	Richard Neuschel, Director, McKinsey & Co., New York City
10:15-10:30	Marshall Evans, Vice President, Management Services, Westinghouse, Pittsburgh, Pa.
10:30-10:45	Arthur W. Lucas, Vice President, Director of Corporate Planning and Evaluation, Monsanto Chemical Co., St. Louis, Mo.
10:45-11:00	William Hogan, Executive Vice President, American Airlines, New York City
11:00-noon	Panel Discussion

SESSION TWO
MONDAY 2 pm-5 pm

GRAND BALLROOM

General Management Information Systems

2 pm-3 pm

Organizing and Operating a Centralized Management Information Service Center

Robert Cheek, Director of Westinghouse Tele-Computer Center, Pittsburgh, Pa.

3 pm-4 pm

A Totally Integrated Management Information System

Al Apgar, Manager, Methods & DP, Clark Equipment Co., Buchanan, Mich.

4 pm-5 pm

Development & Installation of a Master Plan for Overall Management Planning, Decision-Making & Control.

John Roe, Supervisor, DP, Chance-Vought, Dallas.

SESSION THREE
MONDAY 2 pm-5 pm

GEORGIAN ROOM

Manufacturing Management Control Systems

2 pm-4:15 pm

A totally integrated computer production line at Western Electric Co.

Robert N. Marshall, Supt., Hdqtrs. Engineering, Western Electric, Winston Salem, N.C.

J. D. Schiller, Asst. Supt., Mfg. Engineering, Western Electric, Winston Salem, N.C.

H. H. Arnold, Dept. Chief, Development Engineering, Western Electric, Winston Salem, N.C.

4:15 pm-5 pm

A Manufacturing & Information Control Center at the Norge Corp.

TUESDAY 9 am-noon

GRAND BALLROOM

Advances in Management, Planning, Decision-Making & Control Systems Applications

9 am-10 am

A Marketing & Sales Planning, Decision-Making, & Control Information Service

Lionel E. Griffith, Asst. Controller, International Latex Corp., Dover, Del.

10 am-11 am

A Research & Engineering Planning, Decision-Making, & Control Information Service

Martin J. Crean, Dir., DP, Sperry Gyroscope Co., Great Neck, N.Y.

11 am-noon

A Financial Planning, Decision-Making, & Control Information Service

Neal Dean, Dir., E. D. P., Booz, Allen & Hamilton, Chicago, Ill.

TUESDAY 9 am-noon

GEORGIAN ROOM

Advances in E. D. P. Hardware & Software

9 am-9:45 am

Advances in E. D. P. Peripheral Hardware

Norman J. Ream, Dir., Systems Planning, Lockheed Aircraft Corp., Burbank, Calif.

9:45 am-10:30 am

Advances in Computer Hardware

Charles Adams, Pres., C. W. Adams Assoc., Boston, Mass.

10:30 am-11:15 am

Advances in E. D. P. Software

Milton M. Stone, Dir. Management Information Systems, Arthur D. Little, Inc., Cambridge, Mass.

11:15 am-noon

Exhibitor's Equipment Announcements

noon-2 pm

Annual Get-Together Luncheon Exhibition of Advances in E. D. P. Equipment & Systems

TUESDAY 2 pm-6 pm

EXHIBITION HALL

WEDNESDAY 9 am-noon

GRAND BALLROOM

Advances in Management Information Systems Concepts

9 am-11 am

Advanced Management Information Systems & Industrial Dynamics in Practice

J. Pettit, Dir., Industrial Dynamics Research, Hughes Aircraft Co., Culver City, Calif.

Dr. Alan Rowe, Manager, Industrial Dynamics Research, Hughes Aircraft Co., Culver City, Calif.

11 am-noon

Integration of Management Planning, Decision-Making & Control with Information Systems

Dr. Alex Rathe, A. M. A. Fellow & Assoc. Prof. of Management, Columbia University, New York City

WEDNESDAY 9 am-noon

GEORGIAN ROOM

Advances in E. D. P. Operations & Practices

9 am-9:45 am

E. D. P . Systems Reliability, Control & Internal Auditing

Felix Kaufman, Principal, Lybrand, Ross Bros. & Montgomery, New York City

9:45 am-11 am

E. D. P. Systems Production Planning, Scheduling, Control

James Gibbons, Sr. Dir., EDP Systems, Price Waterhouse Co., New York City

11 am-noon

Use of PERT for the Planning & Control of Management Information Systems Design & Installation

Russell L. Robinson, Manager, Administration & Programming, General Electric Co., Cincinnati, Ohio

noon-2:30 pm

Luncheon Speech
TERRACE ROOM

The Relationship of Management Information Systems to Executive Practices and Corporate Profits

Dudley E. Browne, Group Vice President, Finance & Administration, Lockheed Aircraft, Burbank, Calif.

2:30 pm-5 pm

GRAND BALLROOM

Advances in Management Information Systems Techniques

2:30 pm-3:30 pm

Use of Systems Modules in Systems Design

Frank J. Carr, Dir., Business Systems Research & Development, Westinghouse, Pittsburgh, Pennsylvania

3:30 pm-4:15 pm

Use of Decision Tables in Systems Design

Burton Grad, Manager, Systems Engineering, IBM Corp., White Plains, N.Y.

4:15 pm-5 pm

Use of Systems Generators in Systems Design

Mel Grosz, Division Head, Systems Coordination Div., Standard Oil of N.J., New York, N.Y.

2:30 pm-5 pm

GEORGIAN ROOM

Advances in MIS Research and Development

2:30 pm-3:15 pm

A Report on AMA's Management Information Systems

James Gallagher, Socony-Mobil, New York City

3:15 pm-4:15 pm

A Report on SDC's Model for Management Information Systems

Jay B. Heyne, Director, System Development Corp., Santa Monica, Calif.

4:15 pm-5 pm

A Report on Management Information Systems Techniques

John W. Field, Vice President, Omega Management Inc., New York, N.Y.

THE 7094

IBM announces 90 successor

The 7094, IBM's fastest commercially available system, was announced last month as the newest, large scale entry in the scientific field.

Featuring a 2 microsecond memory as compared to 7090's 2.18 microseconds, the 7094 sells for $3,134,500 and rents for $70,000 per month. Installation will begin in the fourth quarter of 1962.

7090 users may not consider the 7094 a "new" machine however, since their 90s may be converted within 72 hours at a user's present site including installation of additional circuitry and system testing, according to IBM.

Other 7094 specifications include an add time of 4 microseconds (4.4 in the 90); multiply time ranging from 4-10 microseconds; divide time from 4-16 microseconds, and a basic core storage of 32K, 32 bit words. There is a full complement of 7090 op codes plus 20 additional instructions.

The 7094 has 7 index registers as standard equipment (3 in the 90), as well as a look ahead feature. Operations may be performed in automatic single and double precision floating point arithmetic.

In single precision, addition or subtraction averages at 166K ops per second; multiply at 100K ops per second and divide at 55K ops per second. In double precision, average ops per second are 125K for add or substract; 454K for multiply, and 26.3K for divide.

Programming support will include FORTRAN, COBOL, I/0 Control System, Sort, 9PAC, Basic Monitor (IBSYS), and Commercial Translator.

The 7094 completes IBM's present range of medium to large scale hardware which includes the 704 and 709 (12 microsecond memory); 7040 (8 microseconds); 7044 (2.5 microseconds), the 7090 and 94. ■

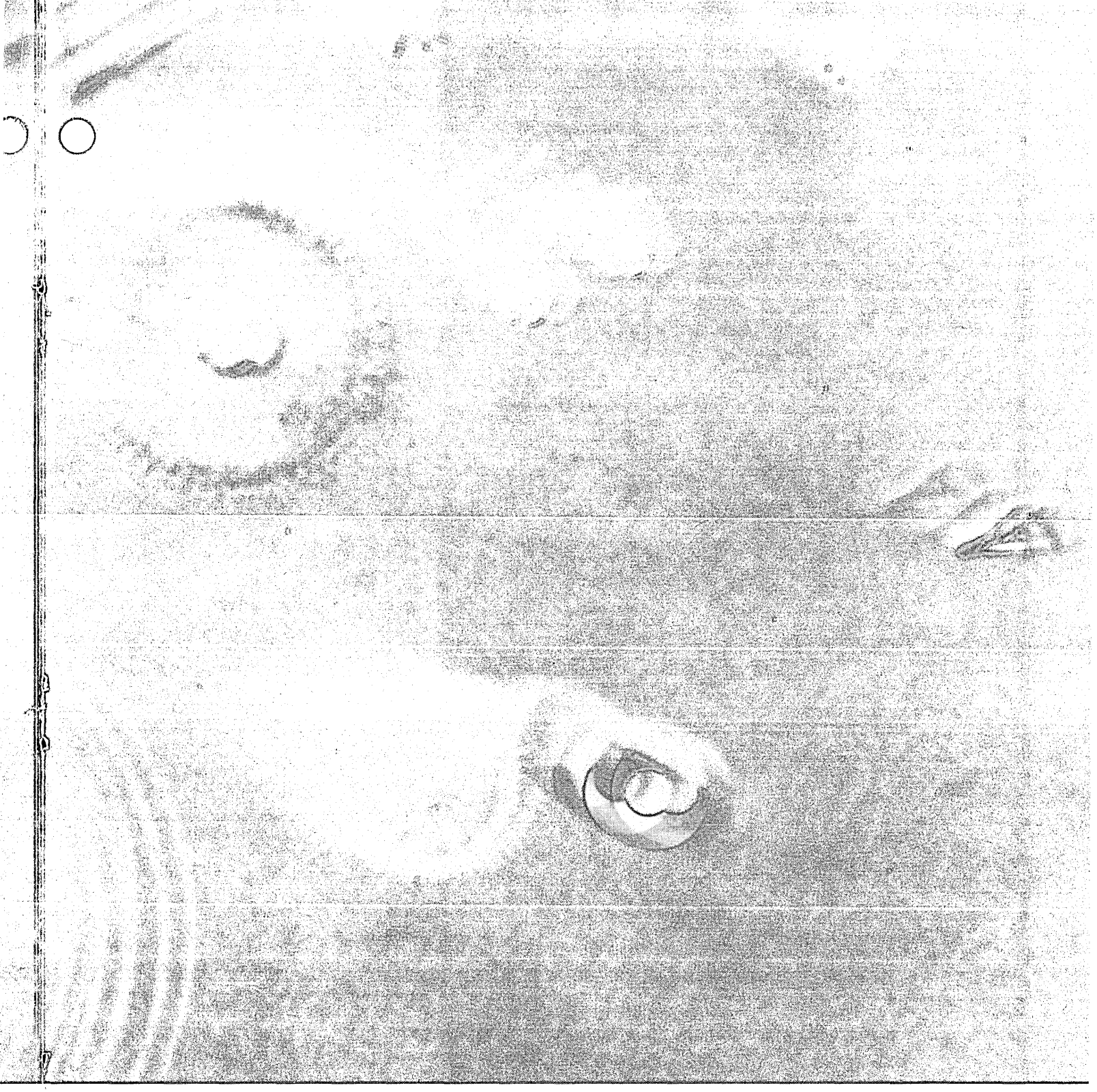
CIRCLE 106 ON READER CARD

Old concepts of time . . . shattered!

Now a computer that operates in billionths of a second—the new UNIVAC® 1107 Thin-Film Memory Computer.

The first Thin-Film Memory Computer available for business and scientific applications, UNIVAC 1107 opens the way to a new generation of computers operating in nanoseconds (billionths of a second). And it combines this amazing speed with unprecedented versatility.

The UNIVAC 1107 has the capacity—16 pairs of input-output channels, 6-million word drum storage per channel, and exclusive interrupt features—to handle a multitude of processing jobs simultaneously. It will



analyze employee records, compute your payrolls, update your inventory or solve matrix problems faster than you thought possible.

Cost? Surprisingly low. In fact, it costs considerably less than many computer installations today while it gives you more speed and broader applications.

What's more, the 1107 talks in many computer languages—Algol, Cobol, Fortran II, to mention a few.

UNIVAC 1107 breaks through traditional computer technology to establish a new standard of performance. You'll want to learn more—so call your Univac representative for complete details.

UNIVAC

DIVISION OF SPERRY RAND CORPORATION

NEW FIRMS & mergers in DP

Advanced Data Systems Corp. was organized late last year to offer edp counsel on such management science applications as capital investment and financial simulation. Offices are in Los Angeles and Robert C. Wigger is president. Edward Coughran is executive vice president. Both officials are former employees of IBM.

CIRCLE 107 ON READER CARD

Recognition Equipment Inc., a new manufacturer of optical character equipment, is staffed by individuals who previously occupied key technical and managerial positions in National Data Processing Corp., which was recently acquired by RemRand.

Herman L. Philipson, Jr., president of the new Dallas firm, stated that in addition to making advanced types of optical reading machines, the company will also engage in military and commercial contracts for the development of electronic, mechanical, electromechanical and optical apparatus.

CIRCLE 108 ON READER CARD

A new firm, Adtrol Electronics, Inc., Philadelphia, will specialize in peripheral input-output devices for digital data processing application. Andrew E. Trolio is president, and Boyce M. Adams is vice president of the company. Trolio was formerly associated with Burroughs and Omnitronics. Adams was recently sales manager for Omnitronics.

CIRCLE 109 ON READER CARD

The Character Recognition Corp., Tarrytown, N. Y., has been formed to sponsor r&d in optical and magnetic reading devices. James W. Murray, chairman of the board of General Precision Equipment Corp., will also serve as president for the new company. The corporation owns all rights to a number of character recognition devices invented by Harold S. Hemstreet who was formerly a member of Link Aviation, Inc.

CIRCLE 110 ON READER CARD

A. O. Smith Corp. has formed a new data systems division with Donald H. Bein as manager. The new division combines the technical computing department of the r&d division with systems and computer programming at the Milwaukee works.

CIRCLE 111 ON READER CARD

International Telephone and Telegraph Corp. has formed an advanced record communication and digital systems group, the ITT Information Systems Division. Alfred di Scipio has been named president and chief executive officer. Function of the new division will be "to utilize ITT's worldwide resources in providing modern, electronic systems . . . for management information and control problems," according to di Scipio.

CIRCLE 112 ON READER CARD

NEXT MONTH IN DATAMATION

Data Transmission — its problems, costs and potential, will receive major feature treatment in DATAMATION's March issue. In cooperation with the Data Transmission Study Group, the first fruits of DTSG's three-year labors will include a comprehensive hardware catalog, a glossary of terminology and a problematic approach to solving specific D.T. headaches. Chairman of the Study Group Jack Strong (C-E-I-R) will introduce this special issue with an exclusive state-of-the-art report.

HOW PRECISE IS EP COMPUTER AUDIOTAPE Extra precise. An unscientific term but an accurate one. We know EP Computer Audiotape is extra precise (which is what EP stands for) because every step in its production is directed toward that end. From raw material to sealed container, this computer tape is measured, checked, controlled, inspected, tested. Automatic Certifiers record and play back every inch of every reel and if just one test pulse out of 40 million doesn't reproduce properly out goes the entire reel. On high density tapes, it takes 112 million perfect pulses to qualify. Is it unreasonable to call this extra precision? Try EP Computer Audiotape.

AUDIO DEVICES INC., 444 MADISON AVENUE, NEW YORK 22, NEW YORK

CIRCLE 19 ON READER CARD

DATA TRANSMISSION AT 3,000,000 BITS PER SECOND

ITT announces 7300 ADX system

The ITT 7300 Automatic Data Exchange System (ADX) is a new, commercially available system which is able to process and switch telegraphic messages and data at speeds up to 3,000,000 bits per second. The system is a solid-state, stored-program, record-communications switching center which can be incorporated in any existing record communications network to handle simultaneously information from high speed computers, as well as relatively slow, 60-word-a-minute teleprinter machines.

The heart of the ADX system is the Multiplexed Message Processor (MMP) which is a stored program, fixed word length, single address, sequential message processor containing the operator console, control circuits, and magnetic core memory. The basic machine is equipped with 4K words of core storage, expandable to a maximum of 32 K. Each MMP word consists of 18 binary bits, which can be retrieved within five microseconds.

The instructions that inform the switching center of where and how to route a received message bearing a specific address are in the form of a stored program which includes "a list of all possible addresses for received messages; the instructions as to the steps to be taken with regard to messages having each of these addresses; instructions as to priority ranks for special messages; and code- and speed-conversion information." It is not necessary to rewire or change plugs or patch-cords for changing the mode of operation since this may be accomplished by merely reading revisions of the stored program into the machine.

Components of the system include the MMP control console equipped with a paper tape reader which can read 400 lines of five, six, seven and eight hole tape per second; a paper tape punch which operates at a speed of 20 characters per second and an electric typewriter for I/O. Additional components generally included are

magnetic tape units, cabinets containing line termination units, level converters and line switches.

The first 7300 ADX system has been ordered by the U.S. State Department. The system has been designed and developed by the ITT Information Systems Division of International Telephone and Telegraph Corp. It is scheduled to be installed in the Paris (France) Embassy early this year. ■

CIRCLE 104 ON READER CARD

THE PACE TR-48

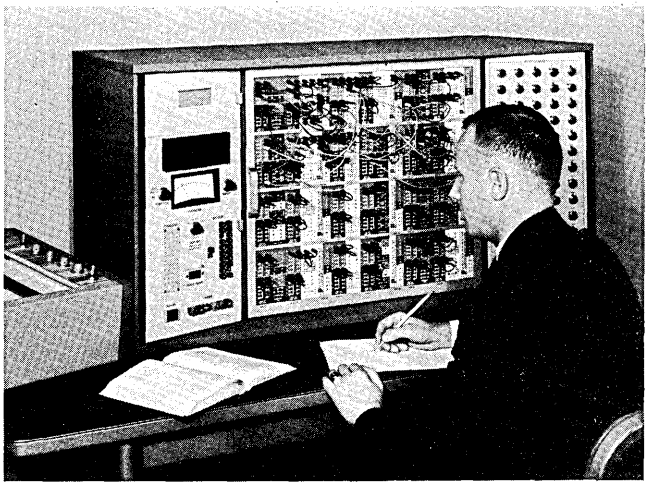
a desk-top analog computer from EA

Electronic Associates, Inc., Long Branch, N. J., have recently introduced a new, transistorized, desk-top analog computer, the PACE TR-48, which can be powered by any ordinary electrical outlet.

The TR-48 contains up to 48 operational amplifiers, 60 coefficient potentiometers and 23 other components including multipliers and function generators. Features of the TR-48 include a built-in digital voltmeter which provides a four-digit plus polarity reading of voltages; push-button readout; interchangeable non-linear components; prewiring of the basic computer to accept the maximum complements of components, high speed repetitive operation accessory which permits the TR-48 to be operated alternately as a real time or repetitive computing device; and color-coded removable patch panel.

Two or more TR-48s can be slaved together to solve larger problems but can be easily disconnected to permit the solution of individual problems simultaneously.

The mechanism is housed in a single cabinet, 47″ long x 20″ deep x 25″ high, and weighs approximately 275 pounds.



The TR-48 is priced between the TR-10 which sells for under $10,000, and the large scale 231R units which cost upwards of $40,000.

CIRCLE 105 ON READER CARD

HOW

■ *can multi-processing make all components of your computer system work full time for you?*

■ *can your jobs run simultaneously in any combination even though your programs are written to run by themselves?*

■ *can you feed new jobs into the system any time without interfering with programs in process?*

■ *can you add a second central processor to the system and thus get true parallel processing without reprogramming?*

■ *can you have automatic scheduling, memory allocation, error checking, and routine control functions without the inefficiencies of conventional operating systems?*

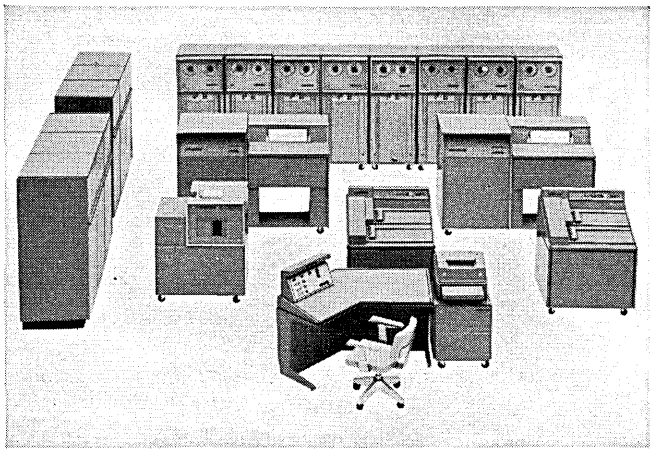
A Burroughs B 5000 is your answer to all these questions. Take multiple processing. We define it as "priority processing on a time-sharing basis." This is the way the B 5000 is normally used. When you want to feed in another job, the B 5000 does not need additional instructions for sequencing and scheduling. It has its own master control program that does scheduling automatically. The programmer doesn't even have to specify the components to be used. He just feeds in the new program. Any time. Usually while other jobs are processing. The master control will integrate it into the work load and see that the components operate at maximum efficiency. The human error factor in scheduling is virtually eliminated.

And your work load can't outgrow the B 5000. It's the only computer on the market that can accommodate a second central processor. A new processor can be linked in any time—*without* costly reprogramming. Thus equipped, the B 5000 can solve several problems absolutely simultaneously; this is *true* parallel processing.

You see our master control program wasn't patched up to fit the computer. We designed the computer to fit a carefully thought-out master control. This is the secret of the built-in operating system's unmatched flexibility and efficiency. It does all the things we mentioned in our 5th question and also permits the addition of new equipment and programs.

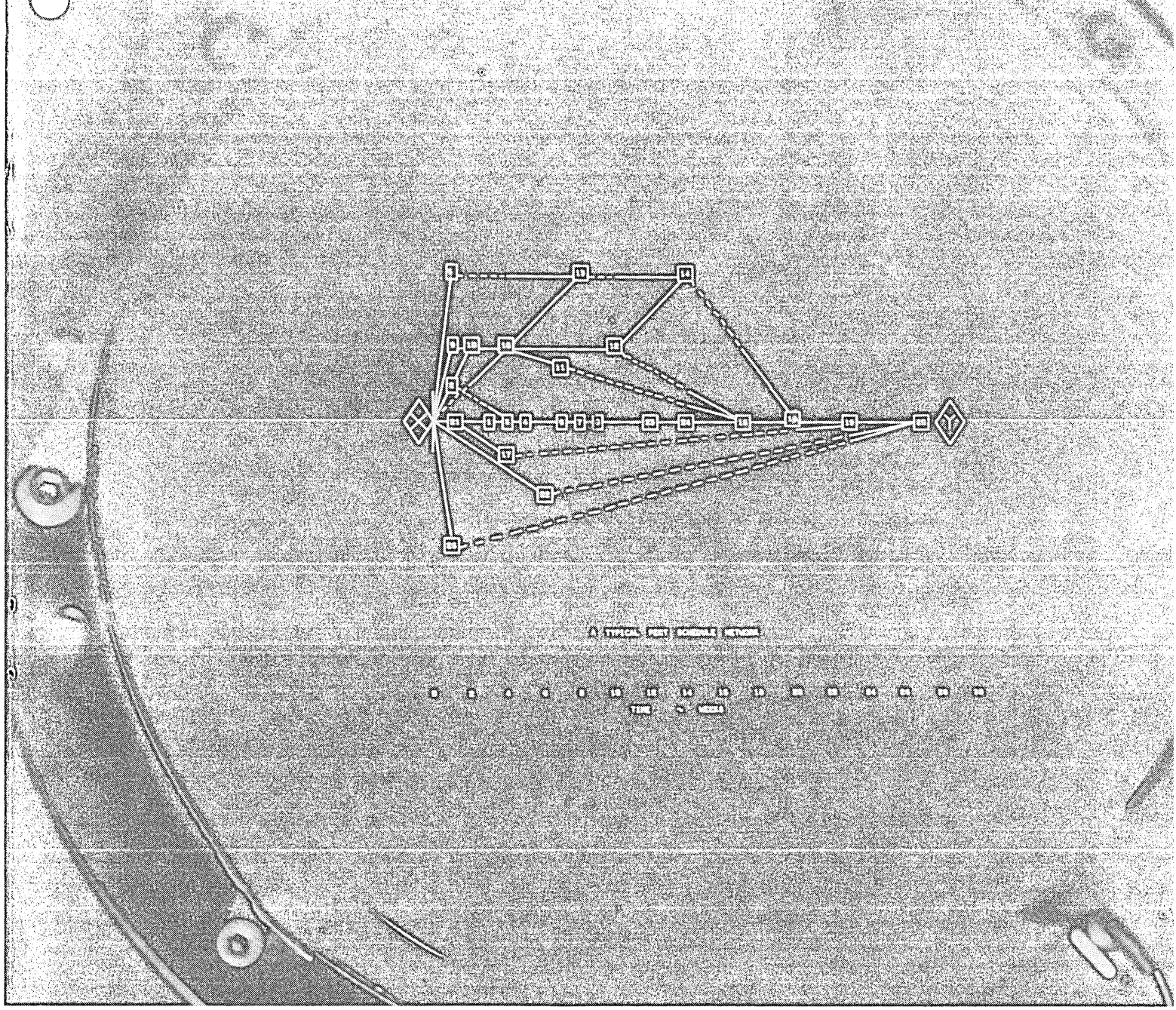
Another thing: The B 5000 can process programs written in COBOL or ALGOL—but that's a story in itself. If you would like the details on *all* the advantages of this remarkable computer, just write Burroughs and ask for a copy of *The B 5000 Concept,* Burroughs Corporation, Detroit 32, Mich.

Burroughs—TM



Burroughs Corporation

Critical path programs drawn in milliseconds!



Typical critical path scheduling network on face of CHARACTRON® Shaped-Beam Tube, heart of the SC-4020.

General Dynamics|Electronics' versatile S-C 4020 Computer Recorder draws complete critical path schedule charts in less than a second. It is the fastest, most economical method available today to translate digital computer language into usable graphs, tabular data, or drawings. Information is recorded on 35mm microfilm which can be enlarged to wall-size viewing charts, or directly on page-size photorecording paper. Write today to Department C-17, General Dynamics|Electronics, Post Office Box 2449, San Diego, California.

GENERAL DYNAMICS | ELECTRONICS GD SAN DIEGO

CIRCLE 23 ON READER CARD

JB ELECTRONIC TRANSFORMERS, INC.

TECHNICAL SPECIFICATIONS

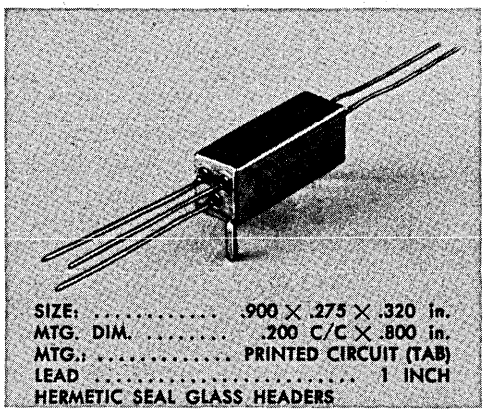
"RUGGED RUNT"
MICRO-MINIATURE RELAY
S.P.D.T. 26.5V.,
1 AMP., 130°C OPERATION
TYPE: RR100 * (PAT. PEND)

MICRO-MINIATURE RELAY

S.P.D.T. (CONTINUOUS DUTY)

REVOLUTIONARY NEW DESIGN; * MEETS AND EXCEEDS, MIL-R-5757, featuring —

- ★ TEMPERATURE RANGE, —65°C TO +130°C
- ★ FAST OPERATING TIME
- ★ FAST RELEASE TIME
- ★ HIGH RELIABILITY
- ★ EXTENDED LIFE
- ★ SMALL SIZE



ELECTRICAL

CONTACT ARRANGEMENT	S.P.D.T.
COIL VOLTAGE	26.5 VDC NOMINAL
COIL RESISTANCE	725 Ω ±10% @ 25°C
CONTACT RATING	LOW LEVEL: 8 MICROAMPS @ 16 MILLIVOLTS: AC OR DC POWER LEVEL: 1 AMP. @ 28 VDC RESISTIVE LOAD
PICK UP VOLTAGE	50% OF OPERATING VOLTAGE
DROP OUT VOLTAGE	7 V. MAX.; 1.5 V. MIN.
OPERATING TIME	1.0 MILLISECONDS MAX. @ 26.5 V.D.C. — COIL VOLTAGE
RELEASE TIME	2 MILLISECONDS MAX. @ 26.5 V.D.C. — COIL VOLTAGE
CONTACT BOUNCE	1 MILLISECOND MAX. (N.O. CONTACT) 2 MILLISECOND MAX. (N.C. CONTACT)
CONTACT RESISTANCE	LOW LEVEL: 500 Ω MAX. POWER LEVEL: .050 Ω MAX. (INITIAL) 0.100 Ω (AFTER LIFE)
DIELECTRIC STRENGTH	500 V. RMS (SEA LEVEL) 300 V. RMS (70,000 FT.)
INSULATION RESISTANCE	10,000 MEGOHMS MIN. 100 V. DC POTENTIAL
OVERVOLTAGE (CONTINUOUS)	30 V. MAX. @ 130°C FOR 10 HRS. MIN. WITH CONTACT CARRYING FULL RATED LOAD
LIFE	100,000 OPERATIONS MIN. (WITH RATED LOAD) CONTACT RESISTANCE LESS THAN 0.1 Ω AFTER MIN. OPERATION AT MAX. AMBIENT OF 130°C
LIFE EXPECTANCY	1,000,000 OPERATIONS (LOW LEVEL)

MECHANICAL

MILITARY SPEC.	EXCEEDS MIL-R-5757
TEMPERATURE RANGE	—65° TO +130°C
VIBRATION	30 G'S, 34-2000 CPS 0.4" EXCURSION, 5-34 CPS
SHOCK	35 G'S @ 11 MILLISECONDS
WEIGHT	.175 oz.

APPLICATIONS

WHEREVER MINIATURIZED HIGH SPEED OPERATIONS ARE MANDATORY FOR HIGH RELIABILITY, PLUS EXTENDED LIFE.

e.g. MISSILES, AIRCRAFT, CONTROLS PRINTED CIRCUITS, COMPUTERS, LOGIC CIRCUITS, ETC.

"RUGGED RUNT" • MICRO-MINIATURE RELAY TYPE RR-100 * (PAT. PEND)

RELAY DIVISION

JB ELECTRONIC TRANSFORMERS, INC.

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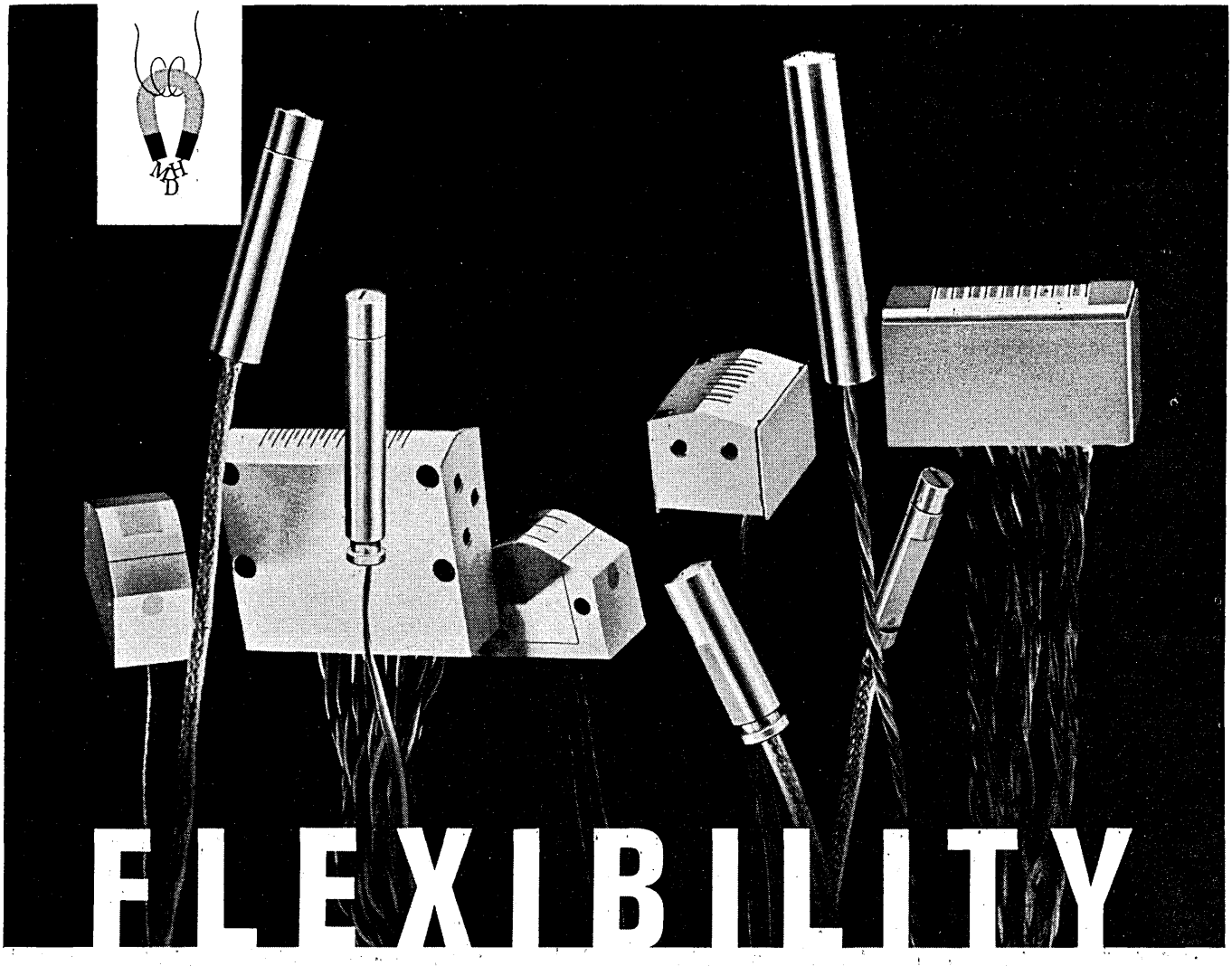


FLEXIBILITY MEANS MAGNE-HEAD... engineered especially for your applications, Magne-Head tapes and drum heads meet both military and commercial specifications. Flexibility of application has been a byword of Magne-Head in the many years the company has pioneered in the development of drums, tape heads, and drum heads. Recently Magne-Head has introduced a full line of drums.

TAPE HEAD SPECIFICATIONS:

Tailored electrical parameters.
Single or multichannel.
Digital or analog.
No limit on number of in-line channels.
Digital bit densities to 5500 per inch manchester.
Analog bit densities to 9000 cycles per inch.
Typical in-line track densities to 20 per inch.
Magnetic card reader track densities to 80 per inch in line.
Gap length as short as 20 micro inches.

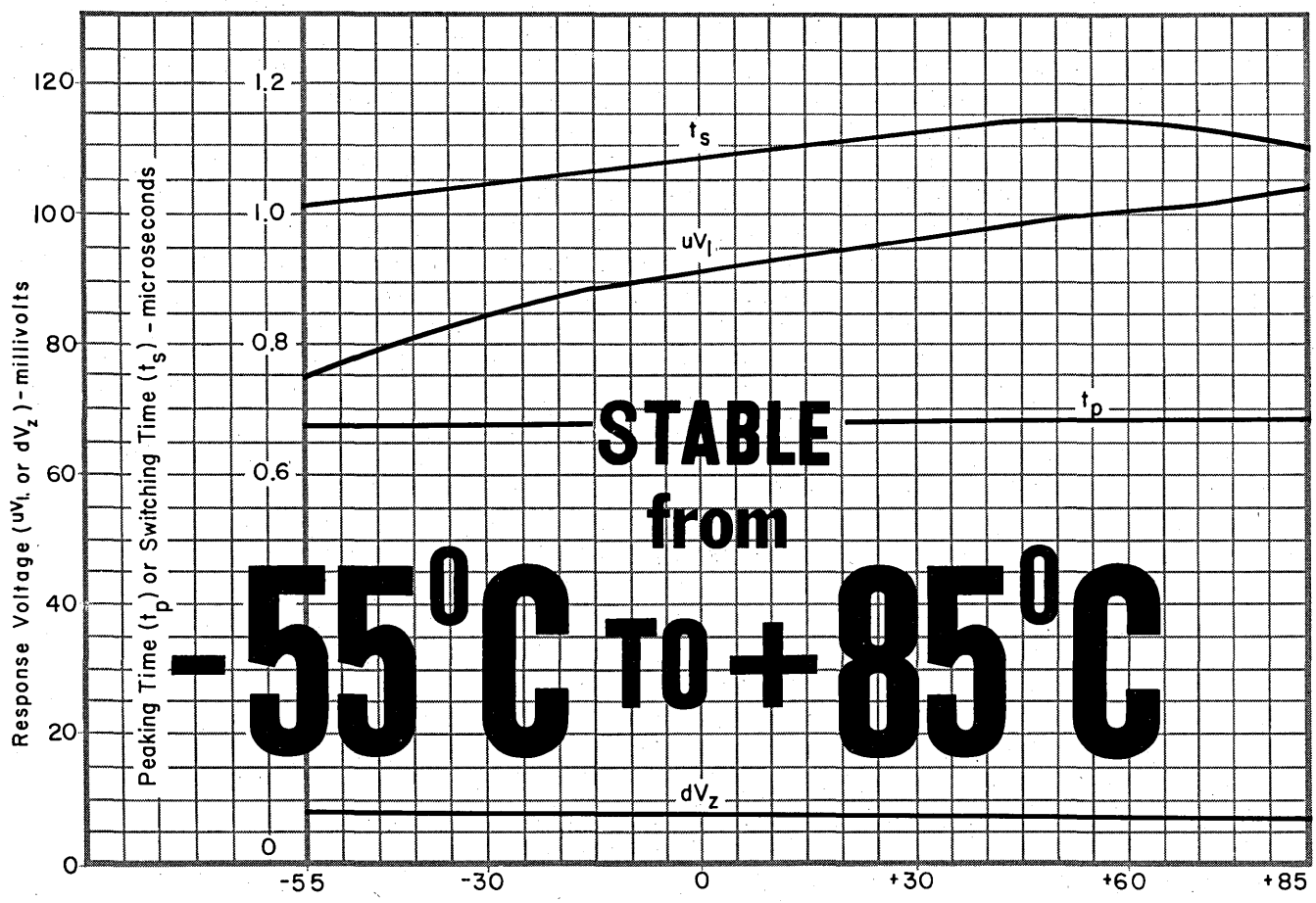
DRUM HEAD SPECIFICATIONS:

Contact or non-contact.
Tailored electrical parameters.
Digital or analog.
Multi-channel heads available.
Manchester bit densities to 350 per inch.
Inductances as low as 40 μh.
Gap lengths as short as 100 micro inches.

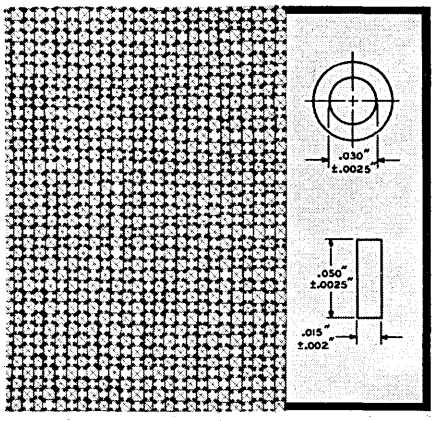
ADAPTABILITY + FLEXIBILITY + CAPABILITY = MAGNE-HEAD

Magne-Head Division of General Instrument Corporation
3216 West El Segundo Boulevard, Hawthorne, California

CIRCLE 25 ON READER CARD



NEW RCA MEMORY CORE MAINTAINS STABILITY WITHOUT CURRENT COMPENSATION OR TEMPERATURE CONTROL



Through new developments in ferrite technology, RCA announces the 233M1, a new ferrite memory core that operates without current compensation over a temperature range four times greater than that permissible for conventional cores.

RCA introduces a new high-temperature ferrite memory core, type 233M1, having an output variation less than 0.25 millivolt per °C from −55°C to +85°C. This operating stability eliminates the need for much of the peripheral temperature control and conditioning equipment now necessary in many computer designs. This new high level of stability opens the way to greater design freedom in applications where space and weight are prime considerations.

The new RCA 233M1 is especially useful in coincident-current magnetic memory devices. At a full driving current of 900 ma, it has a switching time of 1.1 μsec, making it suitable for use in magnetic memories having operating cycles in the 5 μsec region.

RCA now offers one of the industry's most comprehensive lines of memory cores. For your custom requirements, RCA ferrite-core specialists are ready to design virtually any core you require.

Call your RCA Semiconductor and Materials Division Field Representative for a completely coordinated applications service covering transistors, tunnel diodes, multiple semiconductor switching diodes, ferrite components, and memory systems. For further technical information, write RCA Semiconductor and Materials Division, Commercial Engineering, Section B-109-NF, Somerville, N.J.

TYPICAL CHARACTERISTICS OF TYPE 233M1
DRIVING CURRENT CONDITIONS

Full Driving Current (I_m)	900 ma
Partial Write Current (I_{pw})	450 ma
Pulse Rise Time (t_r)	0.5 μsec.
Pulse Duration (t_d)	4.0 μsecs.
Core Size: .050" x .030" x .015"	

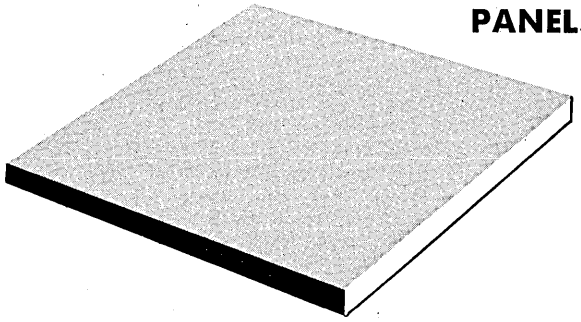
RCA The Most Trusted Name in Electronics

RCA SEMICONDUCTOR & MATERIALS DIVISION FIELD OFFICES... EAST: Newark, N. J., 744 Broad St., HU 5-3900 • (Camden-Philadelphia Area) Erlton, N. J., 605 Marlton Pike, HA 8-4802 • Syracuse, N. Y., 731 James St., Rm. 402, GR 4-5591 • Baltimore, Md., EN 9-1850 • **NORTHEAST:** Needham Heights 94, Mass., 64 "A" St., HI 4-7200 • **SOUTHEAST:** Orlando, Fla., 1520 Edgewater Dr., Suite #1, GA 4-4768 • **EAST CENTRAL:** Detroit 2, Mich., 714 New Center Bldg., TR 5-5600 • **CENTRAL:** Chicago, Ill., Suite 1154, Merchandise Mart Plaza, WH 4-2900 • Indianapolis 5, Ind., 2132 East 52nd St., CL 1-1405 • Minneapolis 16, Minn., 5805 Excelsior Blvd., WE 9-0676 • **WEST:** Los Angeles 22, Cal., 6801 E. Washington Blvd., RA 3-8361 • (San Francisco area) Burlingame, Cal., 1838 El Camino Real, OX 7-1620 • Seattle 4, Washington, 2250 First Ave. S., MA 2-8350 • **SOUTHWEST:** Dallas 7, Tex., 7905 Carpenter Freeway, ME 1-9720 • **GOV'T:** Dayton, O., 224 N. Wilkinson St., BA 6-2366 • Washington, D. C., 1725 "K" St., N.W., FE 7-8500.

CIRCLE 26 ON READER CARD

BEFORE YOU CONTRACT FOR ELEVATED FLOORING

IT PAYS TO TAKE A SECOND LOOK!

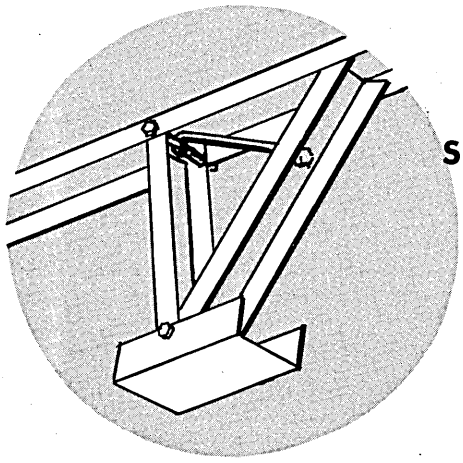


PANELS

Panels available from elevated flooring manufacturers vary considerably in terms of abrasion and indentation resistance.

Sample panels of A, B, and C might look alike. But what does the Taber Abraser (standard test for abrasion) show about elevated flooring panels? It proves the STRATO-FLOOR molded fiberglass panel to be *20 to 30% more mar-and-abrasion resistant and totally free of indentation!* Indentation tests, with compression pressures of up to 5000 lbs. through an individual caster wheel, show that all panels tested, *except STRATO-FLOOR,* had permanent indentation.

STRATO-FLOOR panels, of course, are non-conductive and light-weight.



SUB-STRUCTURE

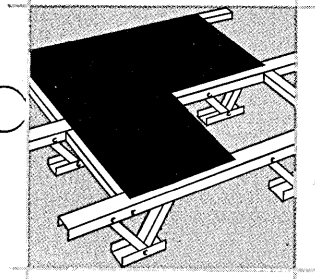
For maximum strength, minimum deflection, the STRATO-FLOOR sub-structure features the patented STRATO-TRI-JACK, which utilizes the strength of the triangle in its design.

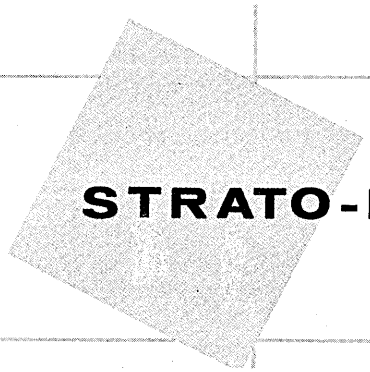
Conventional types of jacks in other elevated flooring systems support the stringer and floor at one concentrated point. The STRATO-TRI-JACK distributes support of the stringer over a larger area, increases the load-bearing capacity and provides greater strength and rigidity. Supports a live load of 250 lbs. per square foot and a point load of 1000 lbs.

CONTRACTOR-RELIABILITY

STRATO-FLOOR elevated flooring is sold and installed by licensed STRATO-FLOOR distributors. They are NOT manufacturer's representatives or commission salesmen. They are reputable flooring contractors, carefully selected by STRATO-FLOOR and known for reliable and conscientious work in the communities they service.

This is important. Before you contract for elevated flooring—get full details about STRATO-FLOOR. Write us for further information and the name of your STRATO-FLOOR distributor.





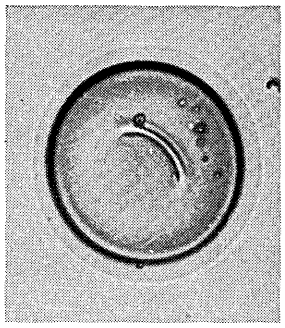
STRATO-FLOOR, INCORPORATED

795 East 152nd Street • Cleveland 10, Ohio

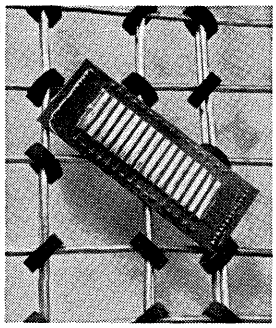
CIRCLE 27 ON READER CARD

Phone: Liberty 1-4200

NCR ...Research

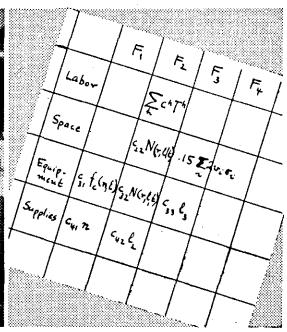


MICRO-ENCAPSULATION



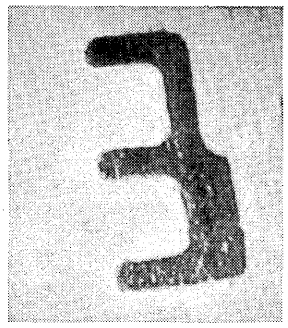
MAGNETICS

THIN FILMS

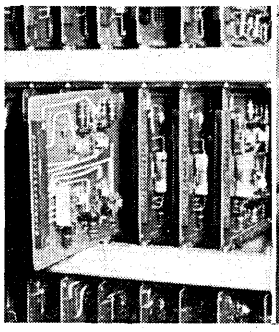


OPERATIONS

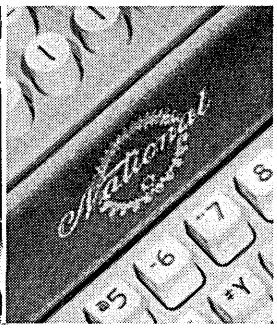
...Development



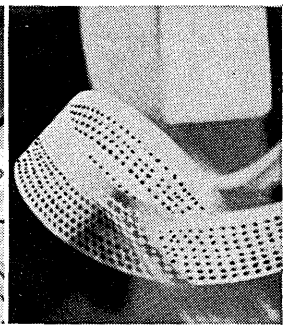
OPTICS



LOGIC & CIRCUITRY

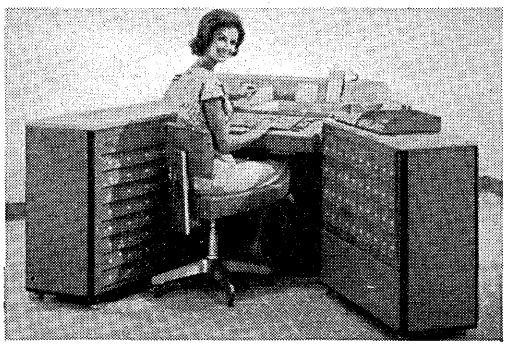


MECHANICS

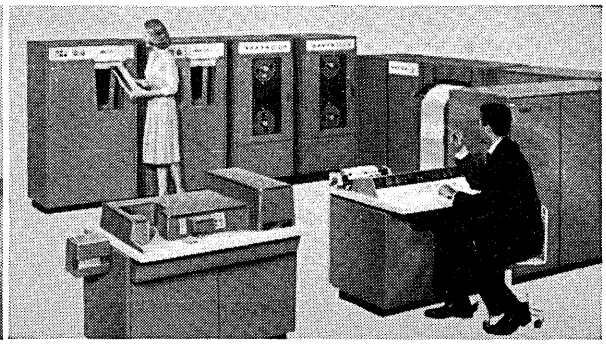


DIGITAL SYSTEMS

...New Products



THE NCR 450 CONTROL AND PROOF MACHINE



THE NCR 315 COMPUTER

NCR offers a wide range of opportunities for experienced scientists and engineers interested in commercially oriented projects or advanced military electronic development. Current work encompasses a broad field of activity including semi conductor research, low temperature physics, micro-electronics, photochromics, advanced electronic systems development, high frequency communications, and operations research studies related to complex business and financial systems. Previous efforts of NCR research and development have resulted in new products such as: NCR (no carbon required) Paper, the highly successful Electronic Data Processing Systems, and other items for the electronic and business machine industries. Rapid growth has caused openings at all levels of experience and education and provide opportunity for technical or administrative growth.

Send letter of application and résumé to: T. F. Wade, Technical Placement, G 14, The National Cash Register Company, Dayton 9, Ohio.

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ONE OF THE WORLD'S MOST SUCCESSFUL CORPORATIONS

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ACCOUNTING MACHINES
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CIRCLE 93 ON READER CARD

NEWS BRIEFS

EXHIBITS OVERSUBSCRIBED FOR SPRING JCC

Exhibit space for the 1962 Spring Joint Computer Conference to be held in San Francisco from May 1-3, has been oversubscribed.

According to exhibits chairman John W. Ball, 56 national firms have applied for the 112 booth spaces. An additional ten booths have been requested and an effort is being made to accommodate them.

Ball and his committee have made space assignments this month for the 8,866 square feet of displays to be installed in the Grand Ballroom of the Fairmont Hotel for the run of the annual conference sponsored by the American Federation of Information Processing Societies.

Exhibits are being limited to approximately half the space available in the new hall, Ball explained, in order to ensure an orderly and equitable flow of visitor traffic. He is being assisted by Arthur Scholar and John L. Whitlock. D. C. Lincicome heads another committee arranging special exhibits in connection with the conference.

NOTRE DAME ORDERS 1107 THIN FILM COMPUTER

Plans for a $3,000,000 computing center to be constructed around a RemRand 1107 thin film memory system, have been announced by the University of Notre Dame. The project, scheduled for completion this fall, has been accelerated by a gift of $1,000,000 from the Sperry-Rand Corp.

The 1107 will be used both for education and research by the colleges of Science, Engineering, Liberal Arts and Business Administration. The computer center is also expected to contribute to the school's Radiation Laboratory which is currently studying the effects of radiation on chemical, physical and biological systems.

CIRCLE 100 ON READER CARD

COLLINS ANNOUNCES TWO COMPUTER ENTRIES

A new line of general purpose computers designated the C-8000 series has been announced by Collins Radio, Dallas, Texas, with the first production models to be available late this year.

Reportedly an extension of its present efforts in integrating data communication and processing, the first system, C-8400, will feature medium-scale computer capability with a main memory expandable to 65K. A smaller model, C-8200, will also be introduced this year.

The C-8400 will be used for automatic message and data operations, with switching, selecting, converting and transmission under stored program control. The C-8200 will be used for tape and card data transmission and communication switching functions.

Prices and further specifications have not been released as yet. Tests on initial models are in progress at Collins' Information Science Center in Newport Beach, Calif.

CIRCLE 101 ON READER CARD

IFIPS PROGRAM FEATURES 123 PAPERS

The technical program for the 1962 Congress of the International Federation for Information Processing Societies (IFIPS) will feature 88 general papers, a survey session of 20 invited papers, 28 symposia, and three hardware sessions of five papers each, on techniques, computers and peripheral equipment.

The conference will be held at the Technische Hochschule, Munich, Germany, from August 27th to September 1st.

Dr. Alwin Walther of the Technische Hochschule in Darmstadt, has been designated general chairman of the '62 conference and Dr. Hans J. Piloty of the Technische Hochschule in Munich, has been named vice general chairman. Dr. Edward L. Harder of Westinghouse Electric Corp., is chairman of the committee for U. S. participation.

A global exhibit of computers and related equipment will be held in Exhibition Park Theresienhoehe, Munich, at the same time as the Congress, and four tours of European information processing activities will be offered during and after IFIPS-62. Thomas Cook and Son is the official transportation agent.

WILEY TO PUBLISH ALGOL TEXTBOOK

The first expository textbook for beginners in ALGOL has been written by Daniel D. McCracken and will be published by John Wiley & Sons in July. Similar in format to McCracken's "A Guide To FORTRAN Programming," published last September, the ALGOL text will be a paperbound edition of approximately 120 pages.

In addition to introducing the

STANFORD ORDERS BURROUGHS B5000 & IBM 7090/1401

A 50-fold increase in computing power will be experienced by Stanford University's Computation Center with the acquisition of a Burroughs B5000 and IBM 7090/1401. Installation of this large-scale hardware in a new 34,000 sq. ft. building will be completed by the spring of 1963.

According to the Director of the Computation Center, George E. Forsythe, a special advantage of having two contrasting computing systems is that "we can learn from intimate knowledge of both which factors are most important for which jobs." The B5000 will utilize ALGOL while the 7090 will run FORTRAN.

At present, a Burroughs 220 and an IBM 650 are being used at the Center. Stanford now has 43 courses concerned with or utilizing computing power, with an enrollment of close to 1,600 students. Other users will be Stanford's linear accelerator project, Stanford Research Institute, and various graduate schools and departments.

It is Professor Forsythe's feeling that "no technical or professional course should now be taught as it was in the pre-computer era. Textbooks need much revision to provide techniques and exercises appropriate to computers."

NEWS BRIEFS . . .

various features of ALGOL, the textbook cites numerous examples in terms of the reference language. An appendix summarizes the transliteration rules for present and planned processors for about 10 general purpose computers.

CIRCLE 102 ON READER CARD

PROBLEM DESCRIPTION & ANALYSIS SURVEYED

The American Standards Association's X3.6 subcommittee on data processing problem description and analysis is presently conducting an industry survey on procedures and problem languages which may be ready for general acceptance as a standard for performing dp problem studies.

Data is being gathered on current practices in methodology; input/output/file description; transformation, and terminology including glossary and flow chart symbols. Present studies have indicated that 60 to 85 per cent of dp preparation can involve problem description, and such steps as programming, testing, installation, conversion, and the initial phases of operation may consume less than half of the total effort.

Interested contributors to the subcommittee's work should contact Robert Green, Chairman, X3-6 subcommittee, Engineering and Research Division, Standard Register Co., Dayton 1, Ohio, or John Pfaff, Chairman, X3-6.1 Task Group, Burroughs Corp., P.O. Box 843, Paoli, Penna.

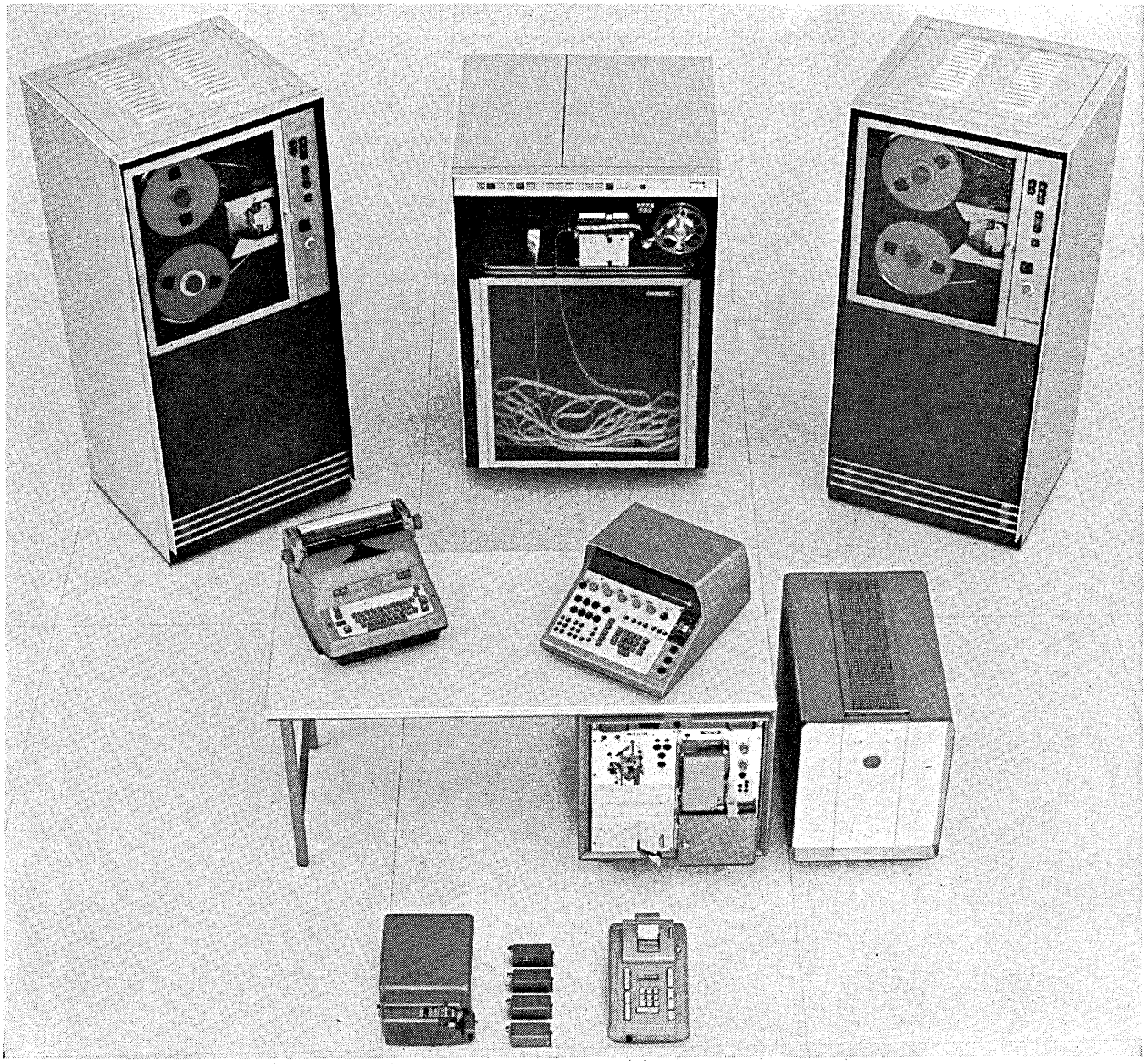
CANCER STUDIES UTILIZE G-15

A Bendix G-15 is being programmed by scientists at New York City's Memorial Hospital for Cancer and Allied Diseases for use in applying data processing techniques to the study of radiation in diagnosing and treating cancer patients. The G-15 will be initially used to determine the amount of radiation from external sources delivered to cancer tissues and surrounding normal tissues, and distribution of radiation by radioactive needles and seed implants. The hospital's G-15 system includes two magnetic tape units and a PA-3 graph plotter.

CIRCLE 103 ON READER CARD

● The Interface model 73 is a small, self-contained, special purpose tape translator which has been developed by the McDonnell Automation Center, St. Louis, Mo., for connecting a variety of digital tape transports to IBM 7000 series computers.

CIRCLE 113 ON READER CARD



Recomp II and accessory equipment.

This machine makes money.

It's a computer.

Like all computers it makes money by solving problems, saving time.

But that's where the similarity between the computer shown and all others ends.

For this is a Recomp® computer. And while Recomp computers are competitively priced—you can lease one from $1,495 to $4,500 a month—they have some distinct money-making advantages over others.

In the medium scale computer field, Recomp II is the only one with built-in floating point. In the small scale field, Recomp III offers the largest word size and largest memory. Recomp's accessory line and software advantages are the most up-to-date in the computer industry. And an extensive programming library is available without charge.

How do we know of Recomp's money-making ability? A feasibility study done by a prospective customer (now a satisfied user) showed that Recomp could save — or make — almost $70,000 more than its nearest competitor on a given project.

There are a number of small and medium scale computers on the market today. Only a few are really outstanding. Recomp is one of them.* For the full story, write:

AUTONETICS Industrial Products
Department 62, 3400 E. 70th Street, Long Beach, California.
Autonetics is a Division of North American Aviation.

Recomp

*No computer feasibility study is complete without Recomp.

CIRCLE 30 ON READER CARD

EDP EVENTS . . .

● A magnetic tape retesting service has been established by IBM to provide for detection and removal of flaws in existing customer tapes. According to the company, this service may reduce the cost of maintaining tape inventories by as much as 30 per cent.

CIRCLE 114 ON READER CARD

● Auerbach Corporation's COBOL-61 Self-Teacher has been designed for training edp users and manufacturers in this common language compiler. The course requires from 25-30 hours of study, at the end of which time the student is prepared to write computer source programs in COBOL, according to the company.

CIRCLE 115 ON READER CARD

● The Burroughs Finance Corporation has been established as another step in the parent company's marketing program for edp systems. The finance company will be used on the leasing phase of Burroughs computer sales.

CIRCLE 116 ON READER CARD

● Computer Sciences, Inc., Westbury, N. Y., has established a data processing center built around an IBM 1620 for processing scientific and business problems.

CIRCLE 117 ON READER CARD

● A computer center has been established by the Instrument Corporation of Florida both for use by the company and the public. The center will make time available on an IBM 1620.

CIRCLE 118 ON READER CARD

● A Seminar in Search Strategy is being offered by the Graduate School of Library Science of Drexel Institute, in Philadelphia, from April 30th through June 8th.

CIRCLE 119 ON READER CARD

● A Univac solid-state will provide an electronic "Syntopicon" at the Seattle World's Fair in an American Library Association exhibit. The memory of the computer will contain data taken from "Great Books of the Western World" for the purpose of demonstrating the potentials of the computer-based library of the future.

CIRCLE 120 ON READER CARD

● Addressograph-Multigraph's Series 900 edp system including card readers, model 943 file processor, model 950 serial printer, model 960 high speed line printer and tape transport units, has been installed at the Salvatorian Center in New Holstein, Wisconsin.

CIRCLE 121 ON READER CARD

● EDGE, a new data gathering system, has been announced by RCA and Lockheed. The system features include speeding the flow of information within plants, eliminating delays in paperwork, and reducing the time and error factor in various production reporting operations.

CIRCLE 122 ON READER CARD

● Autonetics has recently completed the final assembly and checkout of its 1,000th military, transistorized digital computer. Current production at Autonetics' Computers and Data Systems Division in Anaheim, Calif., is on the Verdan D-17 series.

● The New Hampshire Insurance Group, Manchester, N. H., is the recipient of the first commercial model of the Honeywell 400.

CIRCLE 123 ON READER CARD

● A Stored Reference Check Sorter from Ferranti-Packard Electric Ltd., Toronto, Canada, has been installed in the Federal Reserve Bank of New York. The system has been designed to simultaneously control three 18 pocket document sorters, together with three magnetic ink character readers and line printers, for sorting up to 135,000 checks per hour.

CIRCLE 124 ON READER CARD

● The first Bendix G-20 to be installed in Europe has been put into operation at the University of Naples, Italy. The G-20 will provide teaching and research support to the university's engineering school and will be used by both students and faculty for studies in civil engineering, electronics, naval engineering, chemistry, and aeronautical engineering.

CIRCLE 125 ON READER CARD

● Owens-Corning Fiberglass Corp. has installed an RCA 501 to calculate building construction and operating cost economies. Data from a 12,850-mile teletypewriter network between the company's eight plants and 36 offices is fed to the 501 in Toledo.

CIRCLE 126 ON READER CARD

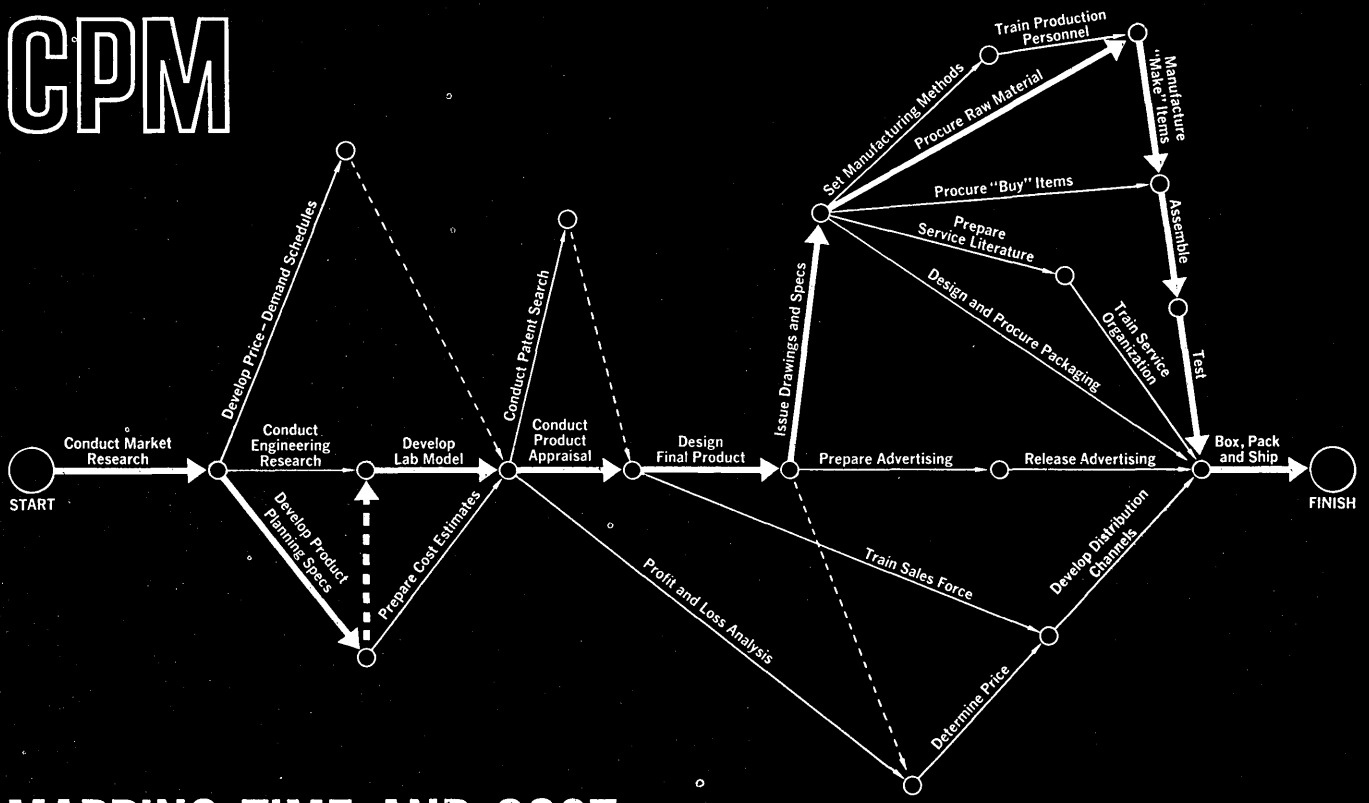
● A Burroughs 270 has been installed in the Community National Bank of Pontiac for the conversion of record processing, payroll and accounts payable work.

CIRCLE 127 ON READER CARD

● The first Burroughs B251 Visible Record computer has been installed in the First National Bank of Miami. First National intends to use the B251 for processing special checking accounts, personal and business checking accounts, cost accounting and savings accounts and general ledger applications.

CIRCLE 128 ON READER CARD

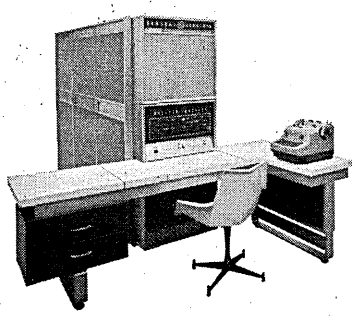
CPM



MAPPING TIME AND COST

A new and powerful project-planning tool from General Electric

You are looking at a dramatic new idea in project planning and control... the Critical Path Method*. General Electric's CPM program can be applied with equal benefit to the set-up of distribution channels, the planning of a missile program, the building of a skyscraper, or as in this case, to the development of a new product. The object is to select the optimum time-cost relationship. To find the answer, the job sequence is first defined in the form of an arrow diagram (above). Then a word description of each activity is added, plus estimates of "normal" and "crash" time and cost, and a job priority weighting factor. Feed this information to the GE-225 Information Processing System and within minutes you have a printed table of the project duration time and least total investment for a complete selection of alternative work schedules, ranging from all normal to all crash programs. You are made aware of those jobs that are critical ... when they must be completed... how to plan for labor and materials and to avoid bottlenecks. You know the status of the project at all times in relation to the scheduled completion date, and what effect a delay in one activity will have on the entire project. CPM and the GE-225 give you the facts for decision-making without guesswork, and can be applied wherever there is a need for timely and cost oriented selection from alternate courses of action. Write today for Bulletin CPB-185, General Electric Company, Computer Department, Section 2J2, Phoenix, Arizona.



GE's CPM PROGRAM PROVIDES: *1 or 3 types of time-estimate options • Non-linear cost approximation • Fixed milestone capability • Automatic renumbering • Optional time-cost summary • Detailed schedule selection*

* *Developed by Mauchly Associates, Inc.*

CIRCLE 44 ON READER CARD

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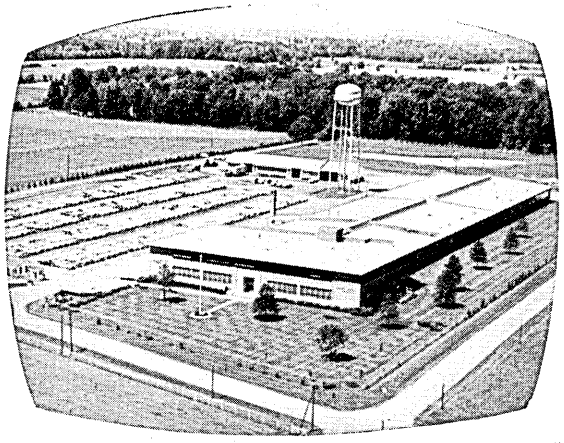
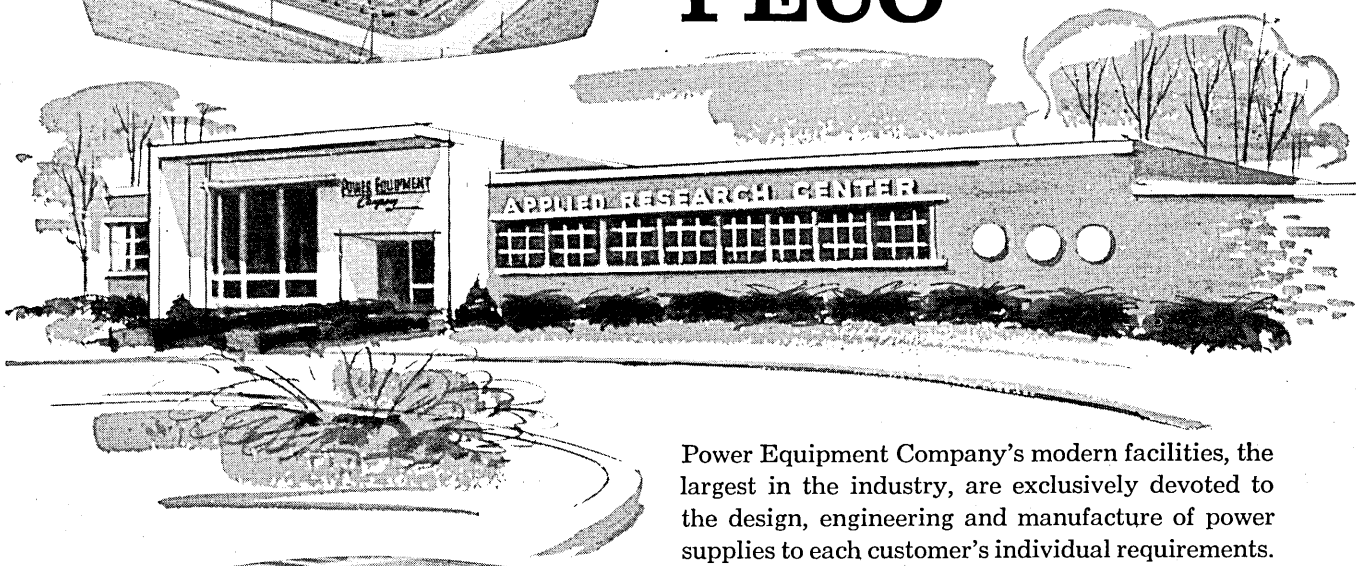
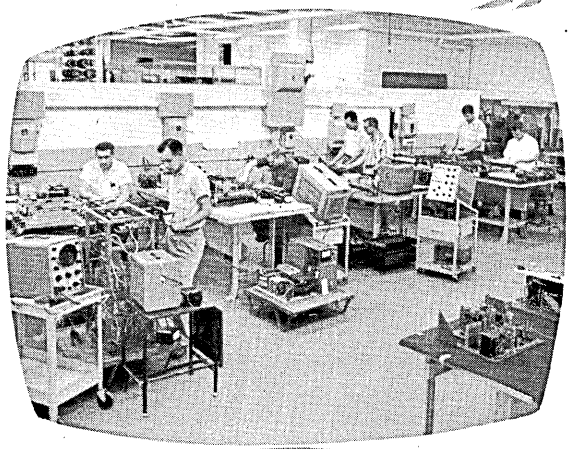


Power supplies are **everything** we make at **PECO**





Power Equipment Company's modern facilities, the largest in the industry, are exclusively devoted to the design, engineering and manufacture of power supplies to each customer's individual requirements.

PECO *Engineering* will custom design a power supply equal in reliability to your own equipment.

PECO *Laboratory and Prototype Service* will place a custom built prototype in your hands in the shortest possible time.

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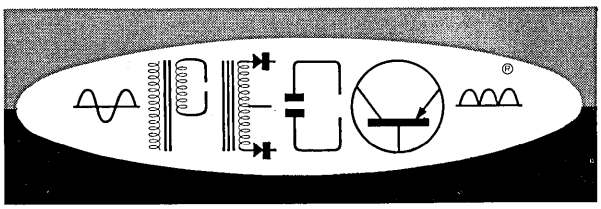
AND PECO power supplies are competitively priced.

PECO custom-engineered power devices, from low power miniaturized and transistorized power supplies to unusually high current capacity battery chargers, range from unregulated AC & DC to highly-regulated AC & DC for commercial, industrial and military computer, communications and automatic control systems.

The PECO capability, recognized since 1935, is at your service. We welcome your inquiry. Write for brochure "Custom Engineered Systems."



POWER EQUIPMENT COMPANY

A DIVISION OF NORTH ELECTRIC COMPANY
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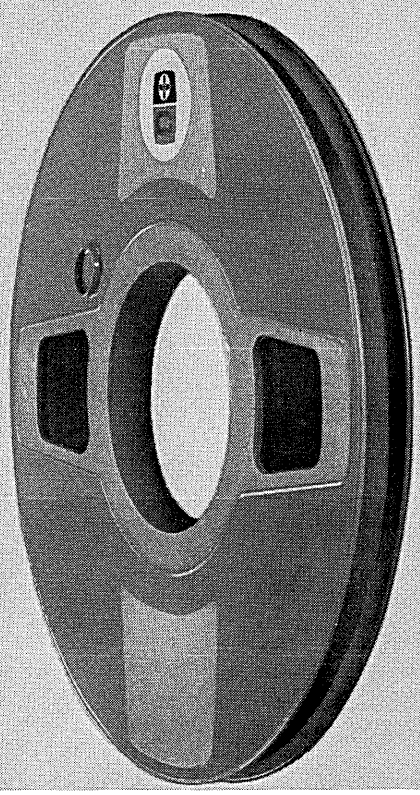
Computape, you never change a bit.

Penelope, you're exactly right. One can't change a bit if one expects to run around with computers all day. That's why I'm guaranteed to deliver *556 or* 800 bits per inch with no dropouts in severest computer applications.



P. S. Computape doesn't really talk, of course. But in a computer, Computape *reliability* will deliver its own message. New COMPUTAPE, the premium quality computer and instrumentation tape, is the product of the only company devoted exclusively to the manufacture of quality tapes for data processing and instrumentation. *Investigate new Computape today. Better still, immediately.*

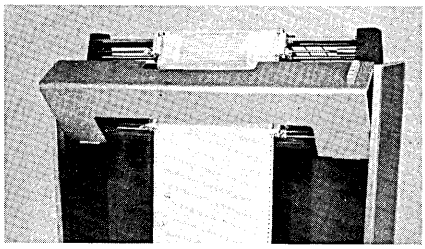
COMPUTRON INC.
122 Calvary Street, Waltham, Massachusetts

CIRCLE 34 ON READER CARD

NEW PRODUCTS

line printer

The T-3300 provides 300-lines-per-minute speed and has a 10 character/inch density, 64 character types, 132 standard print positions, program controlled line spacing and character

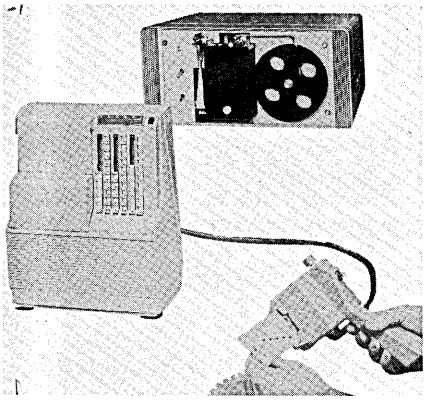


synchronization through a mechanically linked photo diode/code wheel system. TELEX, INC., DATA SYSTEMS DIV., Telex Park, St. Paul 1, Minn. For information:

CIRCLE 200 ON READER CARD

recorder system

The DASHArecorder system features a new kinetic reading head concept and provides a method of reading data from identification plates with transmission to central computing via wire or Dataphones. The unit also transmits simultaneously variable data entered on a specially designed keyboard.



The system may be used for inventory control, production flow control, shipment and receiving control and labor distribution. DASHEW BUSINESS MACHINES, INC., 3655 Lenawee Ave., Los Angeles 16, Calif. For information:

CIRCLE 201 ON READER CARD

magnetic storage drum

Magnetic storage drum model 4-20 has a capacity of up to 50 tracks with individually adjustable heads. The 15 lb. 4-20 may be used in data reduction applications. Bit density is up to 300 pulses per inch with NRZ rec, and capacity is 150,000 bits. It has a pulley and belt drive which permits selected drum speeds up to 25,000 rpm. The unit measures 8½x8½x10¼". A normal playback signal of 40mv is obtained at 2400 ips. COGNITRONICS CO., Briarcliff Manor, N.Y. For information:

CIRCLE 202 ON READER CARD

micro diode

The ultra-fast 1N3206 silicon micro diode is rated at four nanoseconds recovery and four picofarads capacitance. The diode is said to eliminate 90 per cent of common semiconductor failure mechanisms through use of crystal surface passivation. Body size is .030x.075". Operating temperature range is −65°C to +150°C. MICROSEMICONDUCTOR CORP., 11250 Playa Court, Culver City, Calif. For information:

CIRCLE 203 ON READER CARD

decade counting units

A new line of solid state decade counting units covers ranges from dc

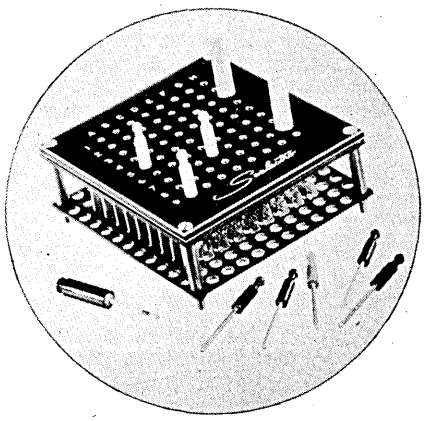
NEW PRODUCTS . . .

to 35 mc and has five basic plug-in units which cover ranges from dc to 300kc, 2 mc, 12 mc, 20 mc, and 35 mc. COMPUTER MEASUREMENTS CO., 12970 Bradley Ave., San Fernando, Calif. For information:

CIRCLE 204 ON READER CARD

programming kit

The Sealectroboard Proto-Kit consists of a program board, shorting pins and component holders. The kit permits multi-point switching and component

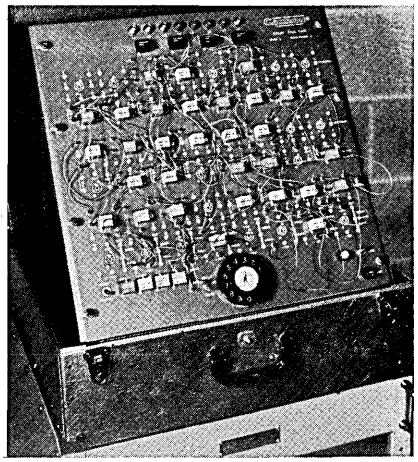


insertion and may be used for troubleshooting, breadboarding, decading of components, paralleling or series operations. SEALECTRO CORP., 610 Fayette Ave., Mamaroneck, N.Y. For information:

CIRCLE 205 ON READER CARD

circuit experimenter

The Circuit Trial Case is a portable, digital panel which permits arrangement of 48 seven-pin miniature computer modules. The instrument enables system engineers to experiment



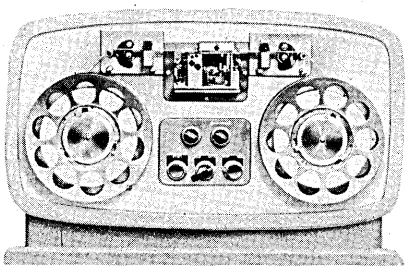
with computer modules to set up logic circuits, change load, frequency and to vary voltages in the generation of a static logic system. CAMBRIDGE THERMIONIC CORP., 445 Concord Ave., Cambridge 38, Mass. For information:

CIRCLE 206 ON READER CARD

NEW PRODUCTS . . .

tape storage unit

Tape storage unit model 2000 provides retrieval and read-out of prepunched tape on reels which revolve at 60 miles per hour. The unit has a capacity of



240,000 alphanumeric characters per reel. CREED & CO., LTD., ITT CORP., 320 Park Avenue, N. Y. 22, N. Y. For information.

CIRCLE 207 ON READER CARD

tape speed detection, correction & apologies

In the November issue of *Datamation*, a new product report was published in which Honeywell "claimed" that their high-density magnetic tapes operate "40 per cent faster than any other tapes in current commercial operation . . . transferring data at 133,000 decimal digits per second . . . "

While there may be some dispute as to whether Honeywell's use of the word "commercial" implies "business dp" as opposed to "scientific and engineering," the argument is a purely semantic one and their claim is invalid since the tape system on the Bendix G20 has been in operation since April, 1961, at 240,000 decimal digits per second, which appears considerably faster regardless of the application.

binary counter

The BC-501 digital module consists of four standard flip-flop circuits connected as a binary counter, which counts from zero through 15 in a standard binary code at frequencies from zero to 250 kc. CONTROL EQUIPMENT CORP., 19 Kearney Needham Heights 94, Mass. For information:

CIRCLE 208 ON READER CARD

zener diodes

The line of 250mW zener diodes has been expanded to include EIA types 1N708 through 1N725, 1N761 through 1N769, and 1N129 through 1N1937. A 4.3-30v voltage range is available and all diodes may be stored and operated at temperatures between −65°C and +150°C. COMPUTER DIODE CORP., 250 Garibaldi Ave., Lodi, N. J. For information:

CIRCLE 209 ON READER CARD

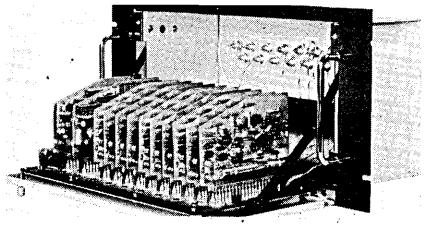
NEW PRODUCTS . . .

analog-digital converters

Series 2500 analog-digital converters claim a basic accuracy of ± .01% for six months. The converter features the electrical isolation of digital input and output lines from conversion circuits during decision making intervals. Speed of the 2500 is 14,000 per second with a max. drift of .0025% of full scale (9999). Digital codes available include binary, 14 bits plus sign; binary coded decimal, coded either 8421 or 4221; or any restricted range of the two basic codes. Display is in four columns of binary coded decimal digits plus sign. BECKMAN INSTRUMENTS, INC., SYSTEMS DIV., 2400 Harbor Blvd., Fullerton, Calif. For information:

CIRCLE 210 ON READER CARD

A new high speed analog-to-digital converter, model AD-10A, operates at up to 500,000 complete 10-bit conversions per second. The AD-10A has a serial output of 5 million bits per



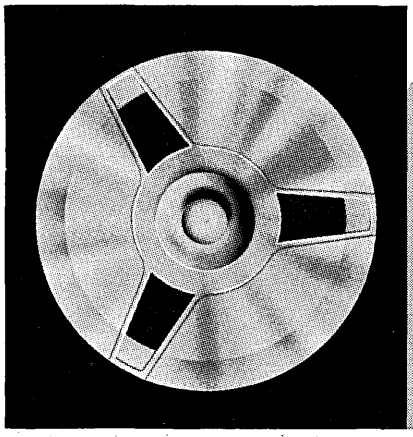
second while its parallel output is up to 500,000 words per second. RAYTHEON CO., COMMUNICATIONS AND DP OPERATION, 1415 Providence Highway, Norwood, Mass. For information:

CIRCLE 211 ON READER CARD

Model 7409R4N is a four-digit, transistorized, analog-to-digital converter which accomplishes all switching by use of a semiconductor device operating on the principle of "successive approximations." Signal polarity is determined automatically and displayed

along with the digital value of the input voltage and the decimal point location on a three-position tilting readout. ELECTRO INSTRUMENTS, INC., 8611 Balboa Ave., San Diego 11, Calif. For information:

CIRCLE 212 ON READER CARD



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Professionals who wish to participate in advancing the state of the art, with experience or training in:

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concepts studies of system availability from the viewpoint of on line data processing systems; knowledge of systems engineering or probability theory necessary.

development of new analysis techniques required in the design of programming large real time computer systems; broad technical background required with specialization in Statistics or Modern Applied Mathematics.

exploration of new techniques in fault location on systems including new logic, diagnostic programming techniques and applied programming techniques.

planning and execution of a full line of computer systems, plan programming systems to accompany the new machines, or the logic design and engineering of one or more of the new systems.

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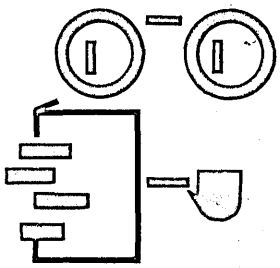


NEW LITERATURE

EDP SALES ANALYSIS: This six-page brochure presents information on sales analysis through computer service. Illustrations of reports on pricing, purchasing, product profitability and other sales management data are given. A typical flow chart is included. STATISTICAL TABULATING CORP., 104 S. Michigan Ave., Chicago 3, Ill. For copy:

CIRCLE 130 ON READER CARD

AUDITING DP SYSTEMS: This new publication, "Guide for Auditing Automatic Data Processing Systems," has been designed to provide the auditor with a general compilation of applicable principles. The book includes topics on modern accounting machines, dp systems, the auditors and ADPS, internal control in ADPS, and machine utilization. A glossary of terms is also included. DEPT. OF THE AIR FORCE, HQ U. S. AIR FORCE, Washington 25, D. C. For copy:

CIRCLE 131 ON READER CARD

PATTERN RECOGNITION: A 59-page report describes the results of a Navy study on recent developments in automatic recognition of two-dimensional visible patterns. Also included are a number of possible industrial applications. Military devices are directed at automatic recognition of enemy aircraft, ships and vehicles. For a copy of this report titled, "Automatic Devices for Recogntion of Visible Two-Dimensional Patterns. A Survey of the Field," send $1.50 to OTS, U. S. Department of Commerce, Washington 25, D. C.

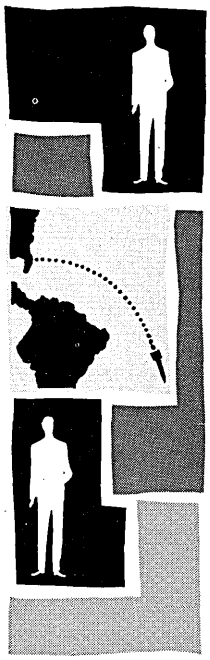
OPTICAL SCANNERS: These two brochures highlight the 1D page scanner and the 1D document scanner. Capabilities of the scanners are given as well as their specifications. FARRINGTON ELECTRONICS INC., 7019 Edsall Rd., Alexandria, Va. For copy:

CIRCLE 132 ON READER CARD

PERIPHERAL EQUIPMENT: An 8-page reference brochure describes a line of record readers, digital plotters, language converters and photo instruments. Bulletin QRC is available from BENSON-LEHNER CORP., 1860 Franklin St., Santa Monica, Calif. For copy:

CIRCLE 133 ON READER CARD

GLOSSARY OF COMPUTER TERMS: A 27-page, illustrated glossary gives definitions of computer terminology used



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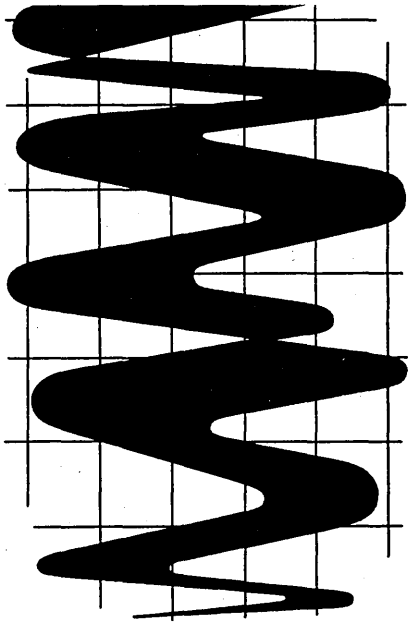

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both in scientific and business data processing. GENERAL ELECTRIC CO., COMPUTER DEPT., 13430 N. Black Canyon Highway, Phoenix, Arizona. For copy:
CIRCLE 134 ON READER CARD

315 EDP SYSTEM: This 44-page booklet includes information on the 315 data processor, control console, punched paper tape reader, high-speed card reader, magnetic character sorter and the interconnecting device. A description of terms, conditions, policies, customer services and programming is also included. NATIONAL CASH REGISTER CO., 1401 E. El Segundo Blvd., Hawthorne, Calif. For copy:
CIRCLE 135 ON READER CARD

800 EDP SYSTEM: This booklet highlights the H-800 and includes topics on parallel processing, orthotronic control, general design, service policies and systems specifications. MINNEAPOLIS-HONEYWELL, EDP DIV., 60 Walnut St., Wellesley Hills 81, Mass. For copy:
CIRCLE 136 ON READER CARD

G-20 PROGRAMMING SYSTEMS: This 24-page brochure outlines the utilization of various automatic languages in the G-20 including COBOL, SPAR, ALCOM, EXECUTIVE and SNAP. BENDIX COMPUTER DIV., 5630 Arbor Vitae St., Los Angeles 45, Calif. For copy:
CIRCLE 137 ON READER CARD

7300 ADX SYSTEM: This illustrated manual on an automatic data exchange system includes topics on ADX system concept, operating features, description of system components, applications, reliability and mnemonic operations codes. ITT INFORMATION SYSTEMS DIV., 320 Park Ave., New York, N. Y. For copy:
CIRCLE 138 ON READER CARD

PROGRAM SIMULATOR: A two-page data sheet describes the PS-425 program simulator which combines manual programming and automatic punch control. The PS-425 is available in 80–, 96– and 120-bit configurations. ELECTRONIC ENGINEERING CO. OF CALIF., 1601 E. Chestnut Ave., Santa Ana, Calif. For copy:
CIRCLE 139 ON READER CARD

PROCESS CONTROL SURVEY: This report surveys the status of computer control in the fields of power, petroleum, chemicals, steel and ceramics. A list of present computer control installations and a chart of process control computer characteristics are given. Machine specifications, compu-

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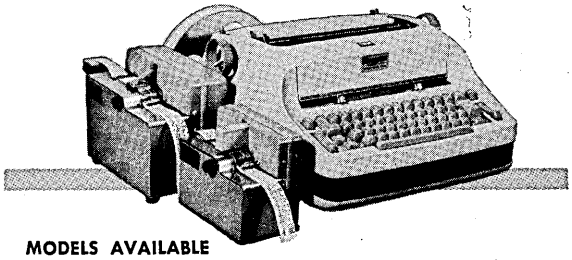
  Computer receives ready signals to permit true closed loop operation . . . keyboard lock control . . . remote tab set and clear . . . print head position indicated in binary code . . . carriage return and index independently controlled for format application.



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TT-200 transmits signals while typing, TR-200 receives signals and prints. TTR-200 transmits or receives signals, TM-200 TT unit with paper punch, TMP-200 TTR unit with paper punch and reader.

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NEW LITERATURE . . .

tation speeds, size and cost of 20 computers are included. CHRONOLOG CORP., 2583 West Chester Pike, Broomall, Pa. For copy:
CIRCLE 140 ON READER CARD

TAPE EQUIPMENT: Four illustrated brochures provide specifications, general data and features of the model 33600 magnetic recorder/reproducer system, model 84 punched tape reader, model 59 digital magnetic tape transport and the model 90 perforated tape reader. DATA-STOR, 8100 Monticello Ave., Skokie, Ill. For copy:
CIRCLE 141 ON READER CARD

T-3300 LINE PRINTER: This brochure includes general information, specifications, system operation, and a description of components. The 3300 can print 300 lines per minute and has a 64 character array. TELEX, DATA SYSTEMS DIV., Telex Park, St. Paul 1, Minn. For copy:
CIRCLE 142 ON READER CARD

HARDWARE/SOFTWARE CATALOG: "Catalog of Printed Material" contains more than 35 publications on the company's current line of hardware and software. Some of the materials included in the library of programs are DIM, FREG, XSUPP and ENDJB. PHILCO CORP., 3900 Welsh Rd. Willow Grove, Pa., For copy:
CIRCLE 143 ON READER CARD

MAGNETIC TAPE CERTIFIER: Bulletin 61-CA provides information on an automatic inspection system that locates defects which might cause loss of information in tapes for instrumentation, telemetering and control systems and explains the principle of operation and method of use. CYBETRONICS, INC., 132 Calvary St., Waltham, Mass. For copy:
CIRCLE 144 ON READER CARD

PRODUCTIVITY METERING: This booklet serves as an introduction to productivity metering in edp. Subjects include a typical example of system monitoring and description of the series TJ time totalizer and also provides a price list for this equipment. STANDARD INSTRUMENT CORP., 657 Broadway, New York 12, N. Y.
CIRCLE 145 ON READER CARD

RESEARCH AND DEVELOPMENT: A 20-page brochure outlines the research and development capabilities of this firm in regard to its Videograph EDP Systems. Personnel, facilities and products are described. A. B. DICK CO., 5700 W. Touhy, Chicago 48, Ill. For copy:
CIRCLE 146 ON READER CARD

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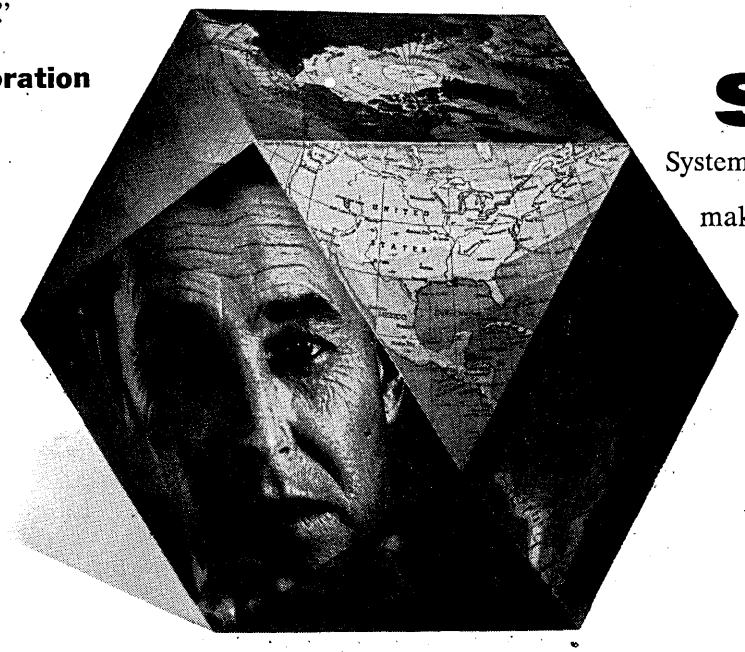

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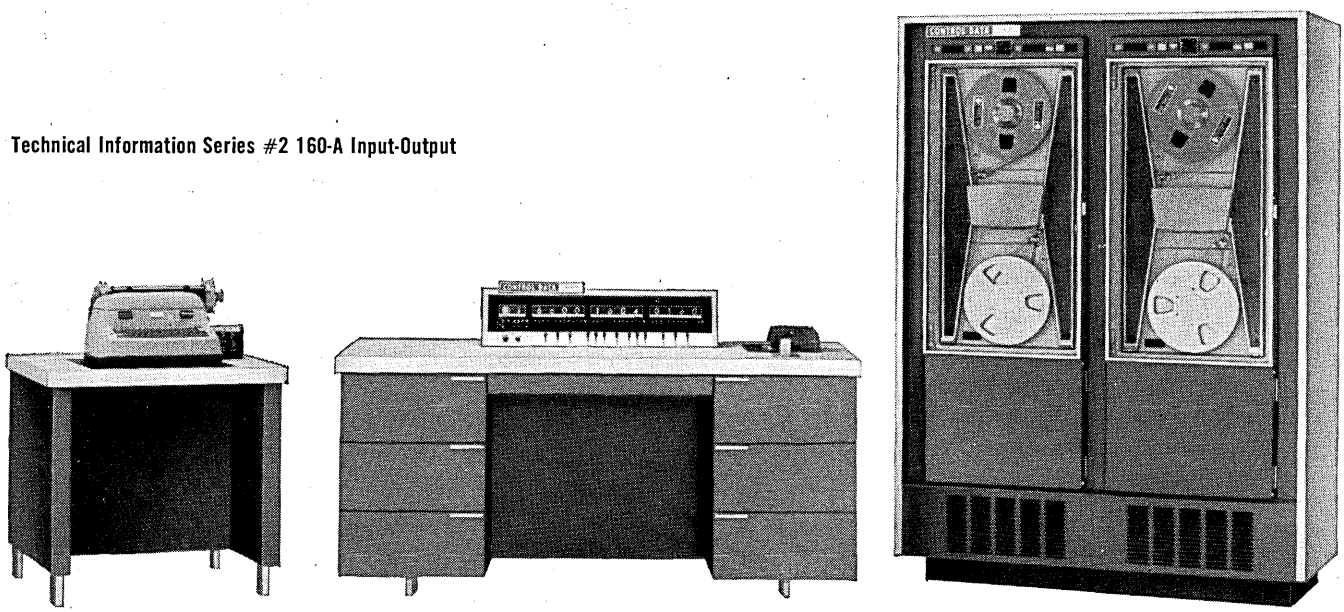
Technical Information Series #2 160-A Input-Output



NEW CONTROL DATA 160-A COMPUTER

Desk Size Computer with Large Computer Capabilities

In most computer evaluations, the flexibility and capability of the computer to handle input-output operations is of special importance. No other small scale computer on the market today has the input-output features that are standard on the Control Data 160-A Computer.

For example, the 160-A exchanges data with input-output devices at any rate up to 70,000 12-bit words per second. The 160-A also has the capability of buffering data while computing... or while the operator manually enters data (whether the computer program is running or stopped). This input-output flexibility is combined with the following 160-A features:

- **Internal and external INTERRUPT**
- **8192 words of magnetic core storage (expansible to 16,384; 24,576; or 32,768 words)**
  6.4 microseconds..... memory cycle time
  12.8 microseconds..... basic add time
  15.0 microseconds..... average execution time
- **Flexible repertoire of 130 instructions**
- **External multiply-divide unit (optional)**
- **Completely solid state**
- **Low power requirements: 16 amps, 110 volt, 60 cycles**

There are two input-output channels in the 160-A: a *buffer channel* and a non-buffer channel called the *normal channel.* Both can be used simultaneously for any combination of input-output operations.

During an input-output operation via the *normal channel,* computation is halted temporarily while the operation is carried out. However, once an input-output operation is initiated on the *buffer channel,* the 160-A either continues computation or performs some other I/O operation on the normal channel.

The Control Data 350 Paper Tape Reader and the BRPE-11 Teletype Paper Tape Punch—standard equipment on the 160-A—are connected to the normal channel and are not buffered. Other peripheral devices can be connected either to the normal channel or buffer channel.

When a peripheral device is connected to the normal channel, data is transmitted between the 160-A and the peripheral device via the normal channel only. However, when it is connected to the buffer channel, data can be transmitted between the 160-A and the peripheral device via *either* the buffer or normal channels. In this case, the normal channel is utilized at any time the buffer channel is not engaged.

A desk-size computer, the Control Data 160-A has the speed, capability, and flexibility of many large-scale computers. For more detailed information write for Publication No. B12-61.

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COMPUTER DIVISION
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EAST VS. WEST DIAGRAMS VS. EQUATIONS

THE COMPUTER'S ANSWER TO A LONG-STANDING COMPUTER ISSUE.

For a decade East Coast and West Coast computer designers have been using different methods of representing computer logic—the Easterners with diagrams, the Westerners with equations.

```
LBSMI=
      (LXA1)(LXA2*)(LFCA*)
     +(LXA1*)(LXA2)(LFCA*)
     +(LXA1*)(LXA2*)(LFCA)
     +(LXA1)(LXA2)(LFCA)
LFCAJ =
      (LXA1)(LXA2)
LFCAK =
      (LXA1*)(LXA2*)
```

In the example illustrated here, the diagram and the equation tell us exactly the same thing. Either represents a serial full adder where the sequence of pulses at the output, LBSM, will represent a serial binary number that is the sum of two serial binary input numbers occurring at LXA1 and LXA2. (The asterisks indicate binary complements; for example, whenever LXA1 is energized LXA1* is not, and vice versa. LFCA is a carry flip-flop.)

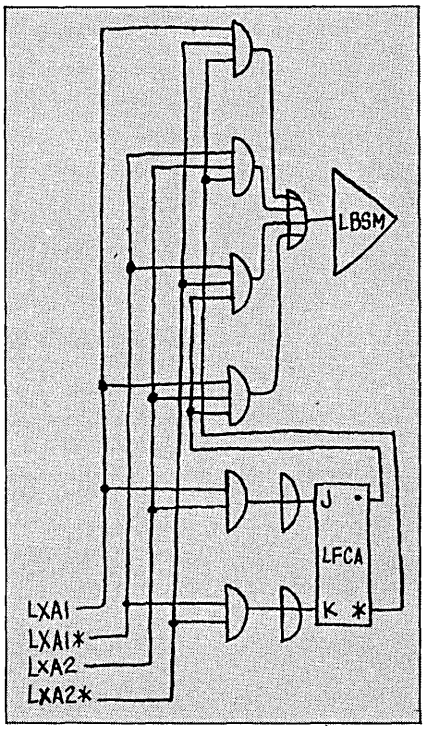
There are persuasive arguments on both sides. Eastern proponents of diagrams point out that the logical interconnections can be seen at a glance and followed through any number of stages by eye. The logical structure of an entire system can be understood from a diagram more directly and intuitively, they maintain, than from a set of equations.

The Western argument for equations goes like this. It's not true that diagrams communicate better to the viewer's intuition, except at first exposure. The human mind is highly adaptive. After working analytically with the equations for a while, the mind begins to operate intuitively in that symbology. Then the intrinsic superiority of equations over diagrams begins to make itself evident. One advantage, say the Westerners, is that equations can represent the same information more compactly and efficiently, as our illustration shows. Another is that equations lend themselves better to computer manipulation of logical design information.

As evidence of the latter advantage Westerners point to a recent achievement of some Litton Systems people: a completely mechanized procedure for translating logical designs into wiring lists, including operational simulation of the design to verify its accuracy. A procedure enormously facilitated by the computerizability of logical equations. It's easy to picture the benefits in cost, delivery schedules, reliability, price. Using only a partial development of this method Litton Systems recently brought a major computer system from concept to operation in less than a year.

Now under consideration at Litton: a machine that will accept as inputs a supply of standard computer components and a set of coded specifications defining the logical functions desired, and will crank out completely fabricated systems.

Maybe you think we've loaded the argument in favor of equations. You're right. But we're ready to listen to arguments on either side. Drop us a card. Or better still, drop in in person. You'll like the



imagination-stretching atmosphere generated by Litton management's appreciation of the rewards of creative controversy. We have a few excellent opportunities for computer design people. Ask for Harry Laur at Litton Systems, Inc., Data Systems Division, 6700 Eton Ave., Canoga Park, California.

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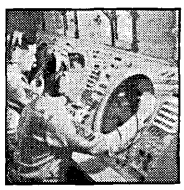
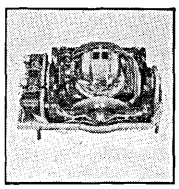


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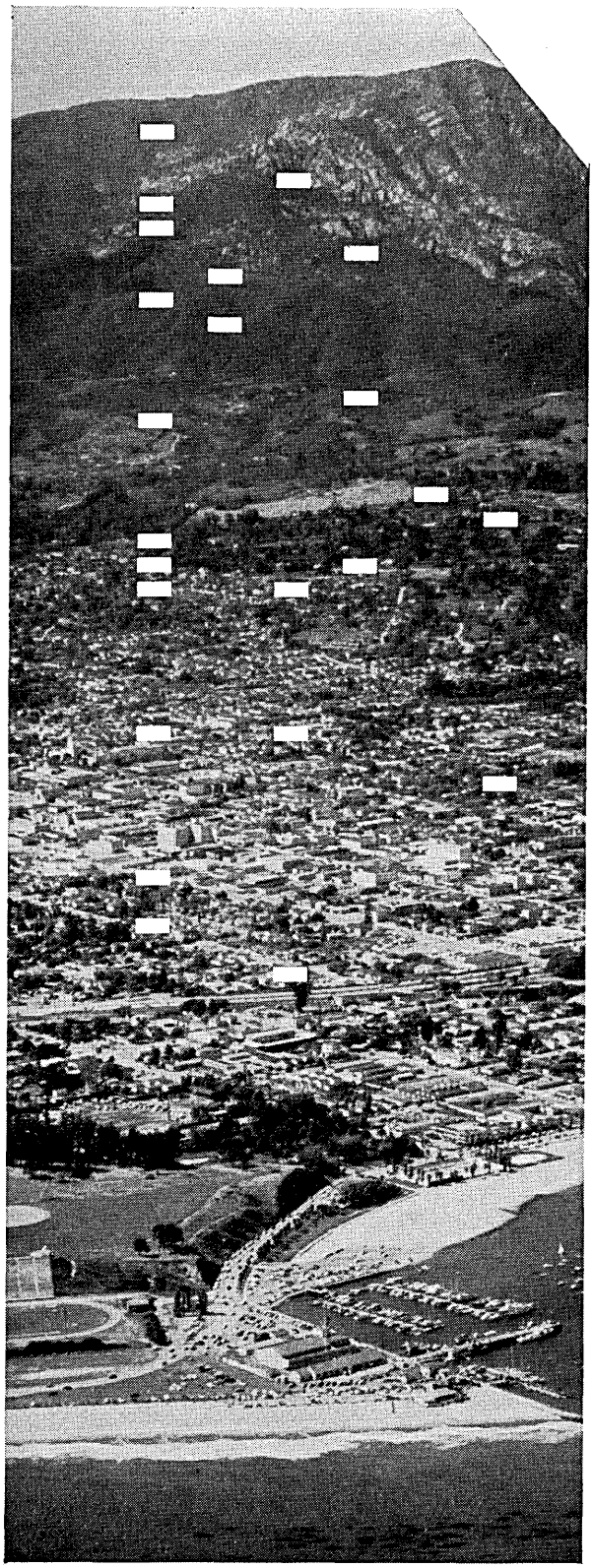

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Installation is under way of a 704 computer to be followed by a G.E. 225 computer, both for use as research tools at *TEMPO*, General Electric's center for the long-range study, synthesis and evaluation of future military weapon and electronic systems.

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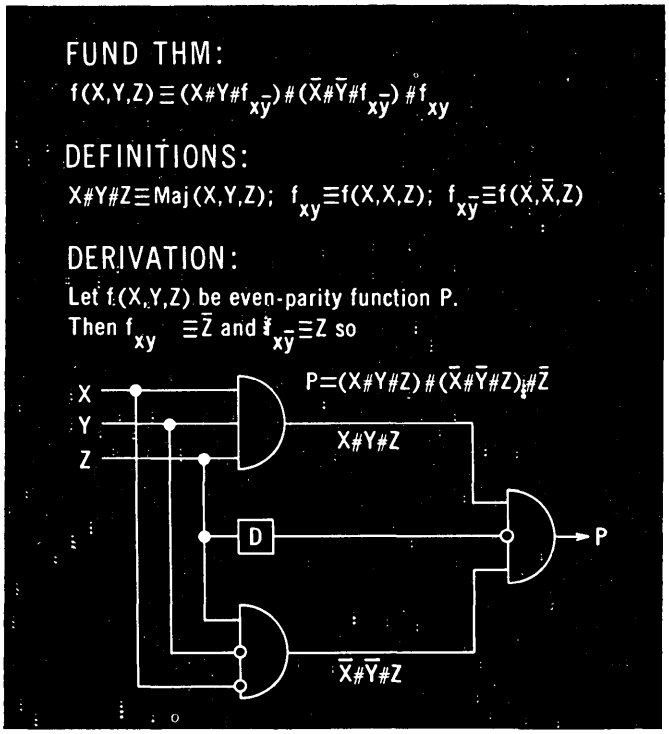
DERIVING majority logic NETWORKS



The fundamental theorem of majority-decision logic, a typical product of Univac's Mathematics and Logic Research Department, has practical as well as theoretical interest. The even-parity checker derived above from the fundamental theorem can be treed to determine the parity of 3^n bits in $2n$ logic levels using only $\frac{3}{2}(3^n - 1)$ three-input majority gates.

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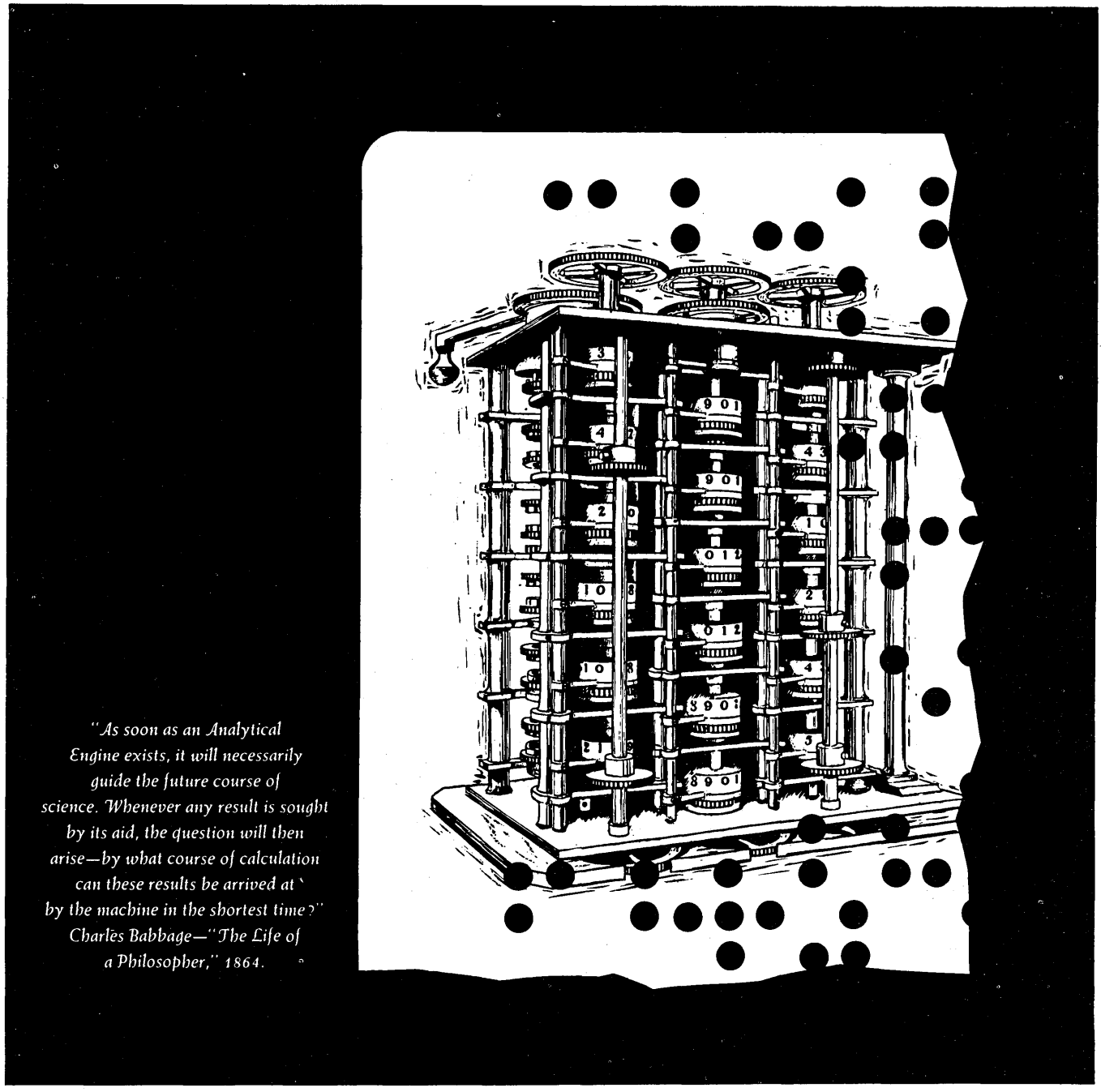

"As soon as an Analytical Engine exists, it will necessarily guide the future course of science. Whenever any result is sought by its aid, the question will then arise—by what course of calculation can these results be arrived at by the machine in the shortest time?" Charles Babbage—"The Life of a Philosopher," 1864.

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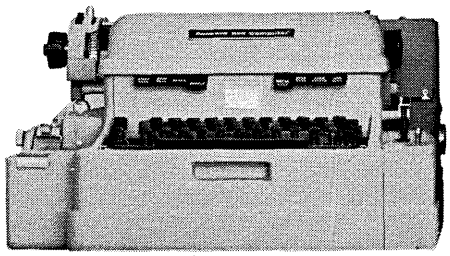

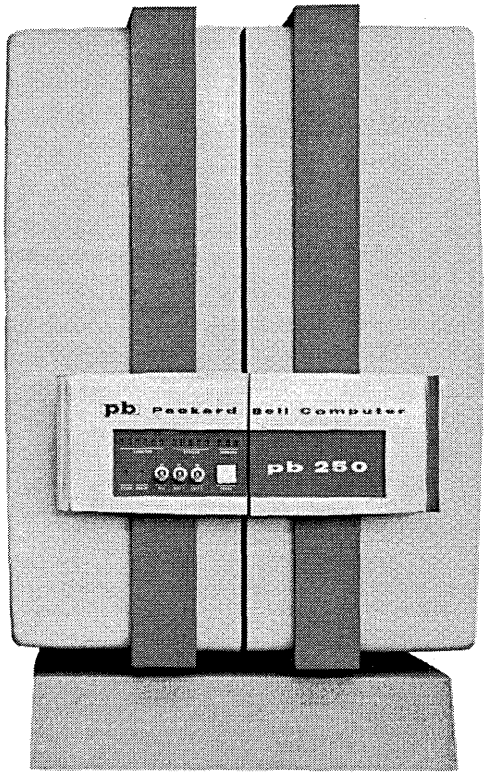

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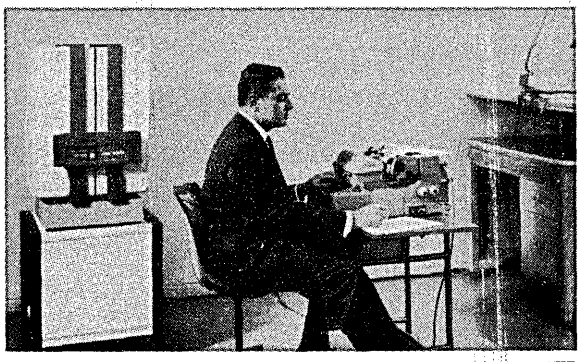

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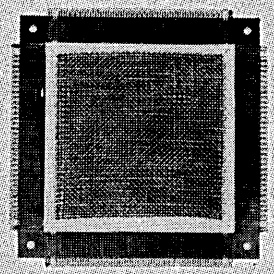

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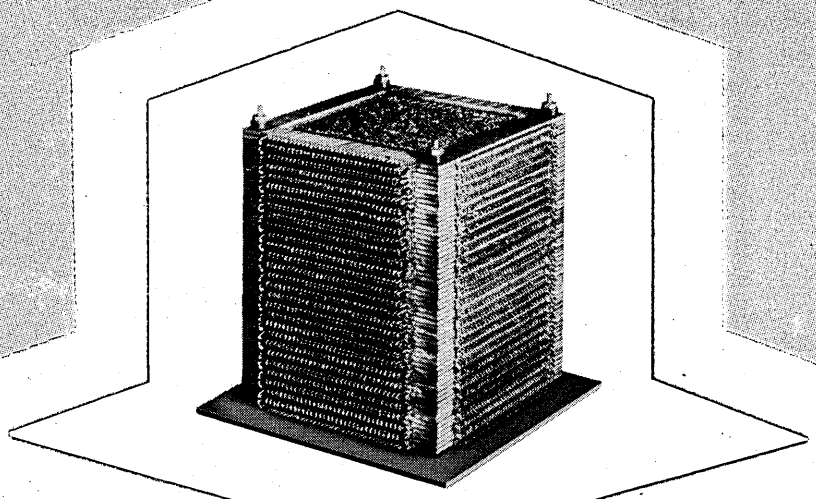

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