COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

MARCH 1969

IN THIS ISSUE ● DESIGN CONSIDERATIONS FOR COMPUTER-DRIVEN CRT DISPLAYS

AN ALGORITHM FOR THE SYNTHESIS OF COMPLEX SEQUENTIAL NETWORKS

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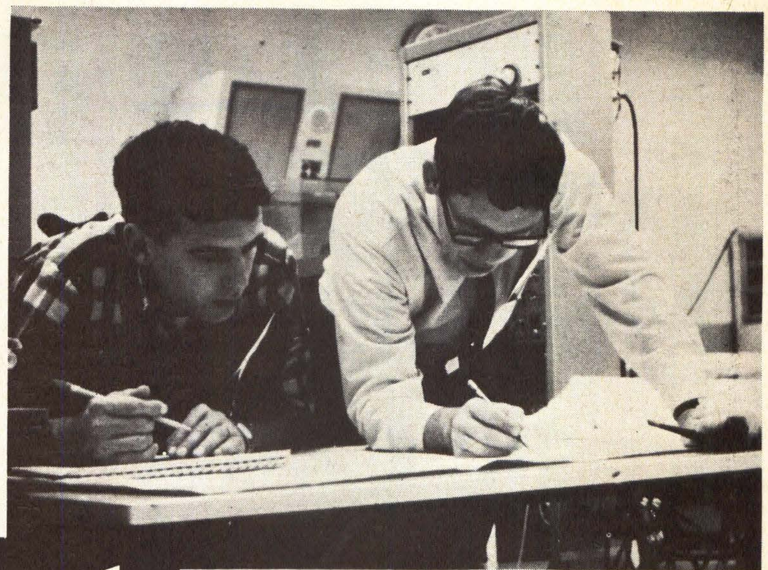

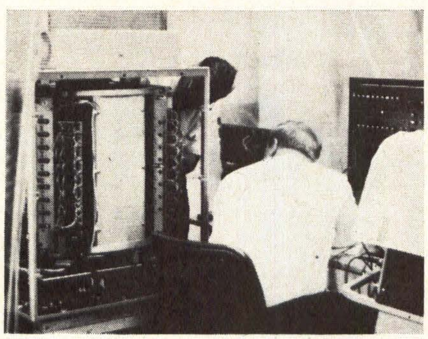

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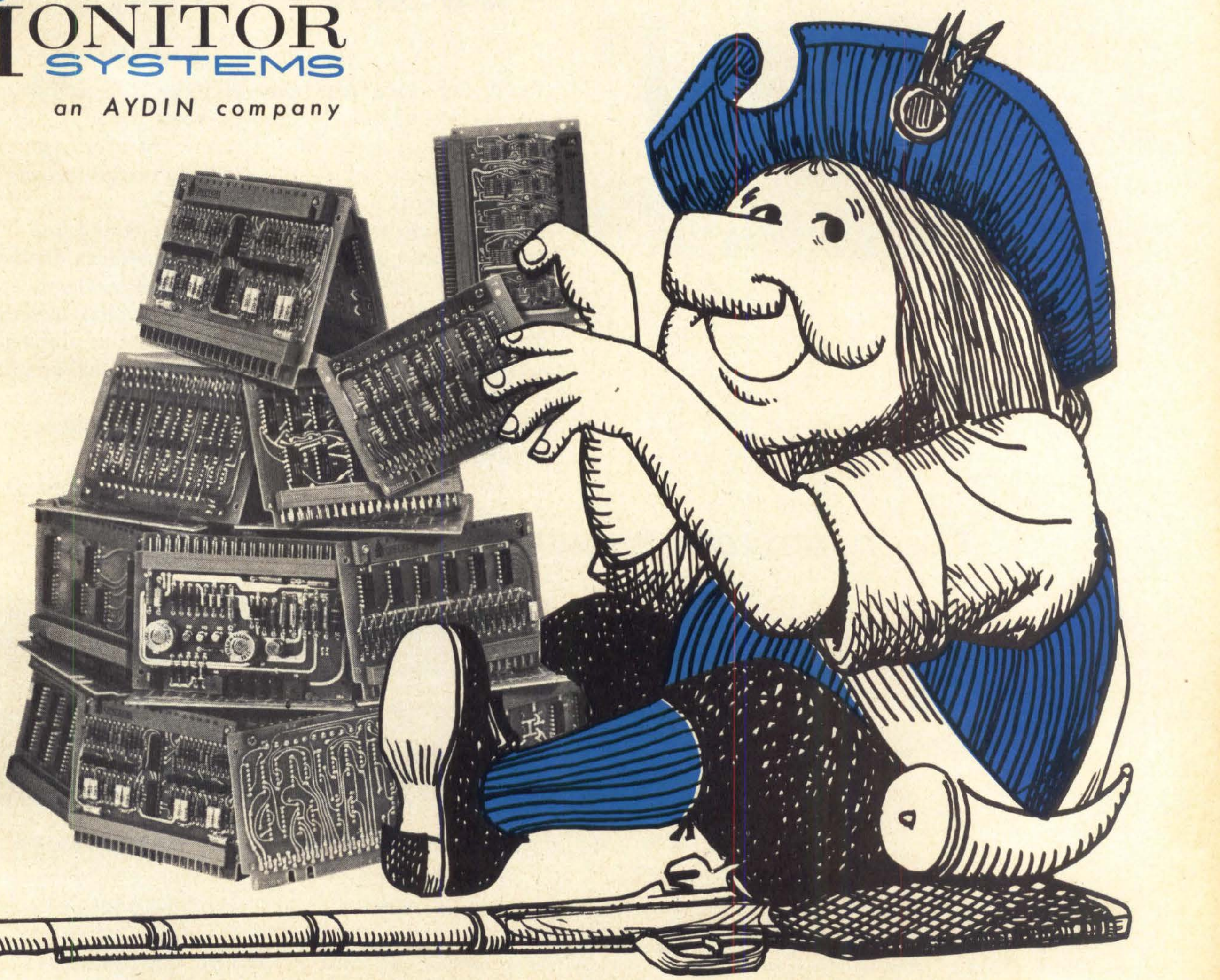

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Editorial & Executive Offices
Prof. Bldg., Baker Ave.,
W. Concord, Mass. 01781
Tel. 369-6660

Computer Design is published monthly.

Controlled circulation postage paid at Bristol, Conn.

Postmaster: CHANGE OF ADDRESS—FORM 3579 to be sent to Computer Design, Circulation Dept., P. O. Box A, Winchester, Mass. 01890. Subscription rate to nonqualified subscribers is \$15.00 per year; \$1.50 per issue. Subscription rate to all foreign subscribers is \$25.00 per year; \$2.50 per copy.

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COMPUTER DESIGN

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DEPARTMENTS

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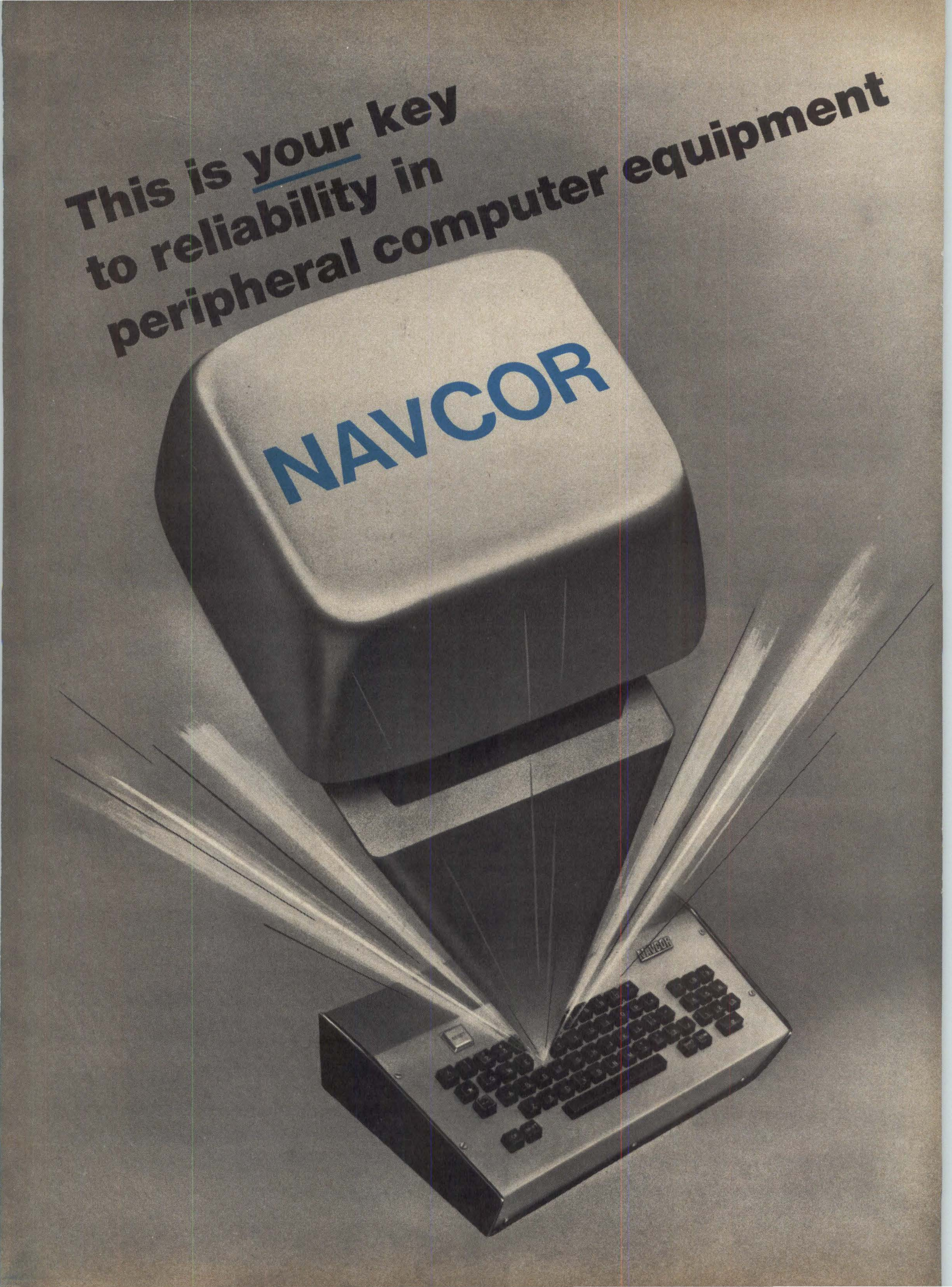
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READER FEEDBACK

To the Editor:

I find the article "The Synthesis of Sequential Circuits" by M. A. Ettinger in the December, 1968 issue of *Computer Design* quite readable and interesting. However I think his Definition 4 of the least upper bound (l.u.b.) of a pair of partitions is not given properly. He defines $\pi_1 + \pi_2$ as the set union of all blocks of π_1 and π_2. This is not sufficient in general. A "transitivity closure" property should be added to the definition. The reason is that, while it is true that the intersection of blocks from two partitions forms a new partition, it is not so for set union of blocks from the two partitions.

The "transitivity closure" property can be explained as follows: Let $\pi_1 = [B_1; B_2; --; Bn]$ $\pi_2 = [C_1; C_2; --; Cm]$ where B_i is a block of π_1 and C_i is a block of π_2. We say B_i and C_j are connected if and only if $B_i \cap C_j \neq \emptyset$. We say B_i and C_j are chain connected if there exists a sequence of blocks A_1, A_2, -- A_k where $B_i = A_1$, $A_k = C_j$ and A_l are blocks from π_1 and π_2 such that A_l is connected to A_{l+1} for $l = 1,2,..k\text{-}1$. Then the block in $\pi_3 = \pi_1 + \pi_2$ that contains B_i of π_1 is formed from the set union of all the blocks of π_1 and π_2 that are chain connected to B_i. For formal definition see Hartmanis & Stearn's "Algebraic Structure Theory of Sequential Machine" pp. 4-5. The author seems to understand this property implicitly. However, his misprinted example that follows the definition makes it harder to see the difference.

There is also a misprint in Fig. 3. X should have a pulse at the fourth clock pulse.

K. M. Yeh
Engineer
Advanced Computing Systems
Burroughs Corporation

To the Editor:

With reference to Mr. K. M. Yeh's letter of January 7, 1969, concerning my article entitled "The Synthesis of Sequential Circuits" in the December, 1968 issue of your magazine, I should like to state the following:

1) With regard to Definition 4 of the least upper bound (l.u.b.), Mr. J. Hartmanis in his paper "On the State Assignment Problem for Sequential Machines I" published in the *IRE*

Transactions on Electronic Computers, Volume EC-10, No. 2, pp. 156-165, June 1962 (my reference 4) states:

". . . for some π_1 and π_2 we have that $\pi_1 \not\leq \pi_2$ and $\pi_2 \not\leq \pi_1$. In such cases, it is useful to be able to construct the least upper bound and greatest lower bound. The least upper bound (l.u.b.) of any two partitions π_1 and π_2, is a partition π_3 such that $\pi_1 \leq \pi_3$, $\pi_2 \leq \pi_3$ and if $\pi_1 \leq \pi_4$, $\pi_2 \leq \pi_4$, then $\pi_3 \leq \pi_4$. Dually the g.l.b. is defined for π_1 and π_2. We shall denote the l.u.b. of π_1 and π_2 by $\pi_1 + \pi_2$ and the g.l.b. by $\pi_1 \cdot \pi_2$. . . .

If two partitions π_1 and π_2 are given and A is a block of π_1, then in the partition $\pi_1 + \pi_2$ the block which contains A is the set union of all blocks of π_1 and π_2 which are chain connected to A in the family of subsets consisting of the blocks of π_1 and π_2."

It is the above that I used to formulate my definition. I agree with Mr. Yeh in that the misprinted example makes it harder to see the difference.

2) The example which follows Definition 4 should have been:

for Example 2

$\pi_1 = \overline{1,2,3}\ ;\ \overline{4,5,6}$

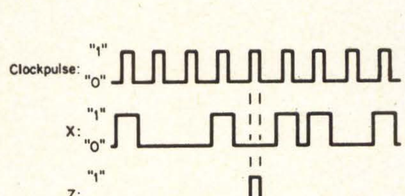
$\pi_2 = \overline{1,6}\ ;\ \overline{3,4}\ ;\ \overline{2,5}$

and therefore

$\pi_3 = \pi_1 + \pi_2 = \overline{1,2,3,4,5,6}$

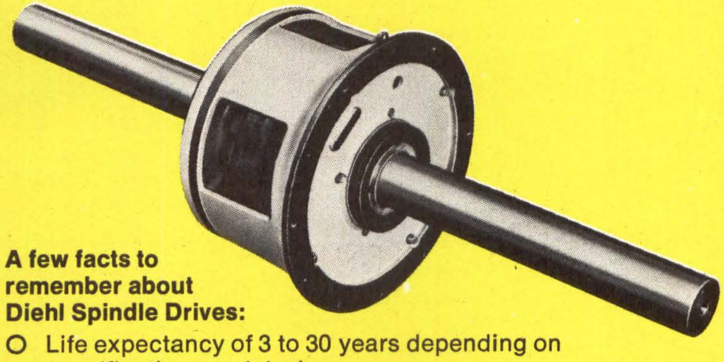
It is unfortunate that π_1 was "misprinted." However, the correct π_1 was referenced some five times throughout the article. With the corrected example I feel that the "modified" definition of least upper bound is sufficient to allow one to generate the l.u.b. partition. After all, the importance of the above mentioned operations in the study of sequential machines is the fact that this partition preserves the substitution property and possibly facilitates solution to the secondary assignment problem for "optimum" realization.

3) The fact that there is a misprint in Figure 3 is correct. The X waveform should have been identical as that of the X waveform in Figure 6 and is shown below:

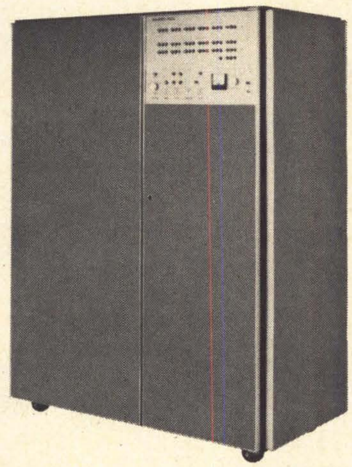


I should like to thank Mr. Yeh for comments and for his care and time in which he spent in reading this article. If he has any further comments concerning the definition, kindly have him contact me.

M. A. Ettinger
Mark Computer Systems, Inc.
Plainview, N.Y.



Reliability is a four-letter word: mtbf



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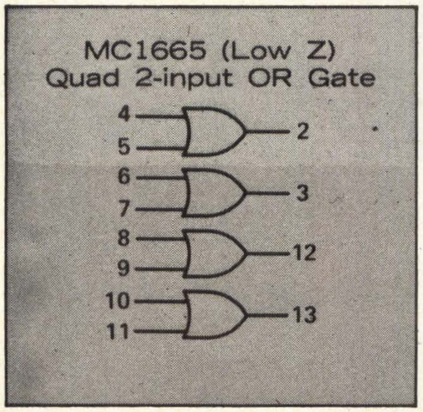

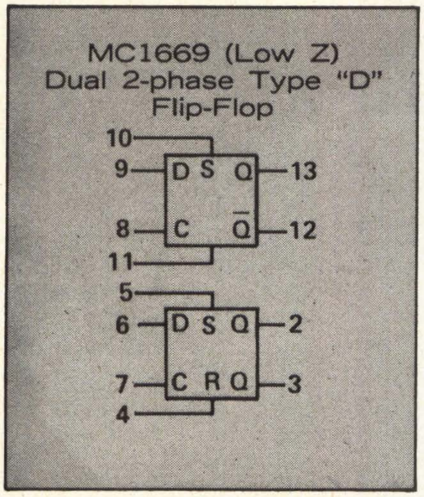

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- MC1667S (Low Z) Dual, 2-phase R-S Flip-Flop
- MC1669S (Low Z) Dual, 2-phase, Type "D" Flip-Flop
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Watch for the introduction of these additional 2 nS MECL II Circuits!

- MC1062 Quad 2-Input NOR Gate
- MC1064 Quad 2-Input OR Gate
- MC1061 Quad Twisted Pair Line Receiver.
- MC1063 Quad Twisted Pair Line Driver. (OR/NOR outputs)
- MC1066 Triple 2-Input Gate With OR/NOR outputs.

All MECL III types (MC1600 series) are currently available from distributor stock in the 14-pin flat pack with stud (for heat sinking).

The MECL II types (MC1000 series) are in the 14 and 16 pin dual in-line ceramic packages. For complete specification data and applications information, circle the reader service number or write to the address below.

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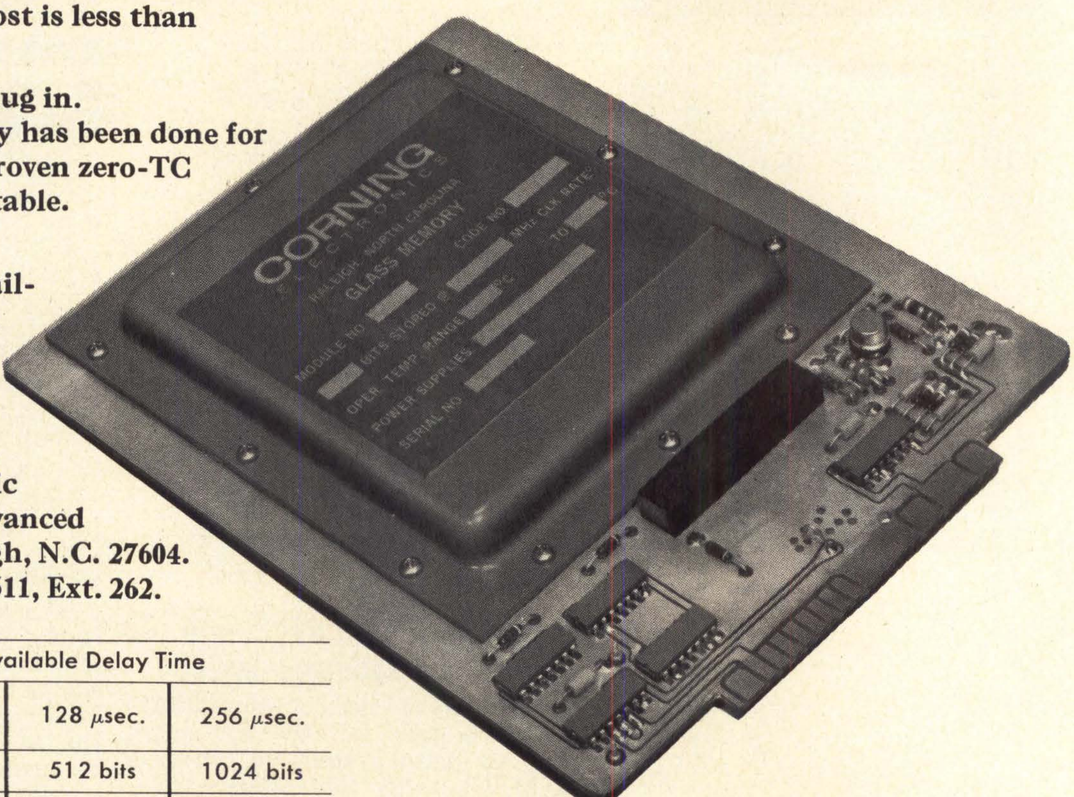

Available Frequencies	Available Delay Time		
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4 MHz	256 bits	512 bits	1024 bits
8 MHz	512 bits	1024 bits	2048 bits
16 MHz	1024 bits	2048 bits	4096 bits

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CIRCLE NO. 12 ON INQUIRY CARD →

CALL FOR PAPERS

The Tenth Annual Symposium on Switching and Automata Theory, sponsored by the Switching and Automata Theory Committee of the IEEE Computer Group and the Department of Applied Analysis and Computer Science of the University of Waterloo will be held in Waterloo, Ontario, Canada, on October 15, 16, 17, 1969. Papers describing original research results in the general areas of switching theory, automata theory, formal languages, theory of computation, theory of programming, and theoretical aspects of logical design are being sought. Typical (but not exclusive) topics of interest include: Abstract Languages, Adaptive Logic, Algebraic Formulations of Automata, Asynchronous Circuits, Automata Theory, Cellular Theory, Computational Complexity, Iterative Circuits, Minimization Techniques, Reliability and Fault Diagnosis, Sequential Machines, Theory of Parallel Computation, Theory of Programming Languages, Threshold Logic, Probablistic Sequential Machines and Automata.

Authors are requested to send six copies of detailed abstracts (no word limit) by May 16 to: Professor John E. Hopcroft, Department of Computer Science, Cornell University, Upson Hall, Ithaca, N. Y. 14850.

Authors will be notified of acceptance or rejection by June 27. For inclusion in the Conference Record, a copy of each accepted paper typed on special forms, will be due at the above address by August 15.

The Third Annual Solid State Devices Conference will be held from 16th to 19th September 1969 at the University of Exeter, Exeter, Devon, England. The Conference will be sponsored by The Institute of Physics and The Physical Society, The Institution of Electrical Engineers, The Institution of Electronic and Radio Engineers, and The Institute of Electrical and Electronics Engineers (United Kingdom and Republic of Ireland Section).

The Conference aims to provide a forum for the presentation of applied research in the physics and characterization of solid state devices, together with associated technologies.
(cont. on p. 18)

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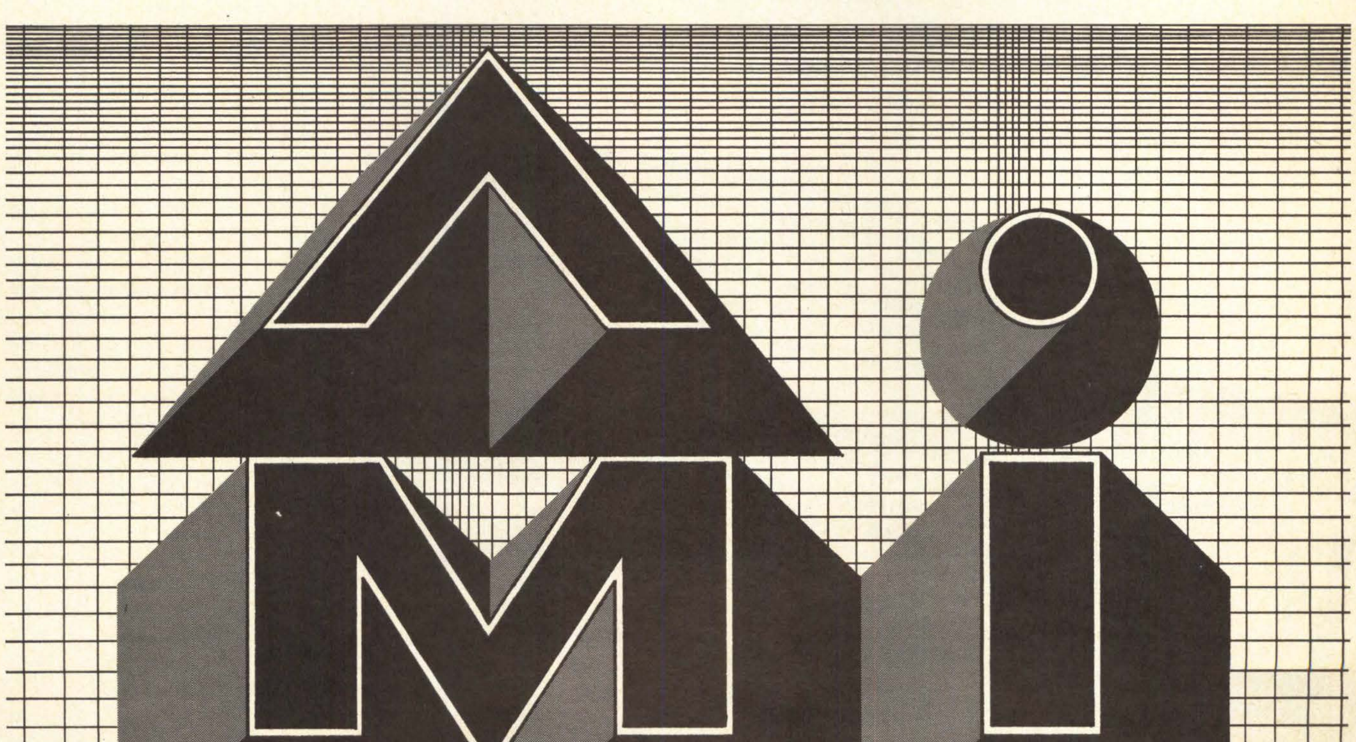


CIRCLE NO. 13 ON INQUIRY CARD

Papers are being invited on the following topics: New devices that are needed, Large Scale integration—two approaches, Semiconducting ferromagnetics, Semiconducting ferroelectrics, Physics of Schottky barriers, the physics of silicon—silicon dioxide interface, Novel circuit elements used in S. I. C. design, and Semiconductor detectors of visible and I. R. radiation and modern microwave techniques.

Contributions on these topics and on new device concepts, device physics, device modelling, device characterization, reliability physics and silicon technology, of about 15 minutes' presentation time will be welcome. Synopses in duplicate of approximately 350/400 words, typed on one side of one sheet, double line spacing, not including figures and capable of being photo-copied, should be sent by June 27th, 1969 to: Dr. P. C. Newman, Conference Programme Secretary, Allen Clark Research Center, Caswell, Towcester, Northamptonshire, England.

Late papers may be considered up to August 29th, 1969.

A symposium of parallel processor systems, technologies and applications will be held at the Navy Postgraduate School, Monterey, California, June 25, 26, 27, 1969. Sponsored by the office of Naval Research, Naval Weapons Center Navy Postgraduate School, and Hobbs Associates, Inc., the symposium is planned to bring together active workers and interested participants from system, device, and application disciplines. Papers will be solicited from a number of people in all three disciplines who are known to be actively working in this area. In addition, this call for papers requests the submission of systems, hardware, and applications papers from other workers in these fields.

Three typed (double-spaced) copies of complete papers and 500 word abstracts should be submitted by March 16, 1969 to: L. C. Hobbs Associates, Inc., P. O. Box 686, Corona Del Mar, Calif. 92625.

All papers submitted in response to this call for papers will be carefully reviewed by at least three reviewers and authors will be notified of acceptance or rejection of their papers and any changes requested by approximately April 1, 1969.

INDUSTRY NEWS

HONEYWELL ANNOUNCES DEDICATED TIME-SHARING SYSTEM —Honeywell's Computer Control Division has announced a dedicated time-sharing system for problem solving which will handle up to 48 simultaneous users for $12 per terminal per day. Unlike conventional time-sharing systems, the H-1648 interconnects three computers to form one multiprocessor. Thus, interactive (conversational) tasks are separated from computational tasks, interactive response time is not increased by heavy computational loads on the system, and a simple, user-oriented command language such as BASIC can be employed.

The three processors used are a communications processor (DDP-416), a control processor (DDP-516), and a job processor (DDP-516). The communications processor acts as a line handler. It receives information from the terminals and formats it for input to the other processors. Conversely, it transmits responses from these processors to the terminals. The control processor acts as a monitor for all activity within the system. It controls the sequence in which requests are serviced, monitors the flow of input and output data, and logs information on services provided for each user.

The job processor performs job requests. It compiles programs and executes jobs under the direction of the control processor. Average response time at a terminal is three to five seconds.

GREAT PROGRESS MADE IN DIGITAL COMMUNICATIONS— The digital communications market, already one of the fastest-growing areas in the computer industry, holds even greater promise over the next few years due to advancing technology, according to Mr. Richard P. Rifenburgh, Executive Vice President of Mohawk Data Sciences Corp.

Speaking before the Second Institutional Analysts Conference at The New York Hilton, Mr. Rifenburgh outlined the present difference between the message communication market and the data communication market. "Today," he said, "the digital message communication market is primarily limited by low-speed terminal devices that we familiarly think of as being used in private wire, TWX, and telex terminals.

"Although there has been some progress in message terminal devices, particularly in inquiry/response devices such as CRT terminals," he continued, "the majority of the technological advances to date have been in equipment used to switch, store, and distribute the information to these older and slower terminal units. On the other hand, great progress has been made in digital communications, especially in equipment for batch transmitting large blocks of information transcribed prior to transmission on auxiliary equipment at the terminal location.

"The future of the communication industry lies in the gradual merging of higher performance terminals used in data communication with the highly sophisticated concentrating, switching and storing units now used in the message communications market. A major corporation's entire flow of message and data information could be handled by large networks of such terminals attached for both message and digital communication functions," he said.

TI SIMPLIFIES DISCRETE SEMICONDUCTOR SELECTON — A unique approach to discrete semiconductor selection has been developed by Texas Instruments, Dallas, Texas. One of the major problems semiconductor users face is choosing the best semiconductor devices—with respect to performance, cost and availability —for their applications. In an effort to ease this condition, TI has preselected the most popular device types out of nearly 15,000 standard and special discrete devices which satisfy the majority of semiconductor requirements.

Robert Pierson, assistant V.P. for TI's Electronic Devices Div., told why the program was developed. "There has been a great proliferation of 'Standard' device types over the years —D.A.T.A. now lists over 65,000 from which to choose. Not only is the choice difficult, but a wrong selection could mean higher equipment costs, or result in availability problems so often associated with special devices. We have conducted extensive computerized analyses to determine basic specification requirements and demand-analysis curves. This year-long program resulted in the selection of 285 small signal and power transistors—both germanium and silicon—diodes, thyristors, rectifiers, regulators, light sensors and resistors which are now designated as 'preferred semiconductors'."

In order to be classified a preferred product, each discrete device in TI's complete standard line was subject to four tests:

1. The product must be in wide use today, known by the majority of design engineers and be proven in numerous applications;

2. The device must be in volume production;

3. It must be readily available from distributor and factory stocks; and

4. The device must be recommended for either present or new design.

"We are encouraging our customers to consider these preferred semiconductors first," Mr. Pierson continued. "If a preferred product does not appear to fit the requirements of a specific design, the choice can still be made from our 15,000 standard and special devices."

A new Preferred Semiconductors and Components catalog is available to design and standards engineers by writing on their company letterhead to: Texas Instruments Inc., Technical Information Services, MS 308, P.O. Box 5012, Dallas, Texas 75222.

INDUSTRY NEWS

CONTRACT TO ELIMINATE TAPE FLUTTER EFFECTS AWARDED—The Office of Naval Research of the Department of the Navy, Washington, D.C., has awarded a $84,384 contract to Technology, Inc., Dayton, O., to develop a system that will automatically eliminate flutter in data reproduced on magnetic tape recorders.

William S. Arnold of Technology Inc.'s Information Systems Div. will serve as project engineer for this program.

Arnold is the inventor of a prototype system that uses electronically-controlled and continuously-variable delay lines to remove flutter from the analog data recorded by magnetic tape transports. The system utilizes the delay lines to alter the time base of the reproduced signals by means of a signal derived from the flutter itself, resulting in a self-correcting servo system.

R&D FORCASTED FOR 1969—Total 1969 expenditures for research and development in the United States are expected to reach $25.9 billion, according to the annual R & D forecast by the Columbus Laboratories of Battelle Memorial Institute.

This is an increase of 3.6 percent over estimated 1968 expenditures of $25.0 billion, but represents a distinctly slower rate of growth than in any year since 1953 when expenditure figures were first compiled. The growth rate from 1967 to 1968, for example, was an estimated 5 percent, and from 1966 to 1967, it was 7.1 percent.

The modest increase predicted in total 1969 expenditures, as Battelle sees it, will result largely from additional funds provided by industry and by colleges, universities, and other not-for-profit institutions. Federal support of R & D in 1969 is expected to remain at about the same level as in 1968.

This year's forecast, prepared by Battelle-Columbus economists Dr. W. Halder Fisher and Leonard L. Lederman, points out that, in terms of purchasing power, the projected increase in R & D spending is not likely to cover the higher cost of doing the same amount of R & D. Current rates of inflation in R & D are frequently estimated at between 5 and 8 percent per year.

The declining growth rate of Federal expenditures represents the continuation of a trend. Over the past ten years, Federal expenditures on R & D grew at a compound rate of 9 percent per year. However, the Battelle forecast points out that the growth rate over the last four years has slowed to about 6 percent per year.

In the near future, fiscal pressures on the Federal Government will tend to hold down appropriations for R & D, according to the Battelle economists. It is unlikely, they observe, that Federal R & D expenditures during 1969 would be much affected by peace in Vietnam. Reductions in total military outlays will not be rapid, even if a cease-fire is negotiated within the next few months.

AUTOMATED FLOWCHARTING SYSTEM OFFERS MORE LOGIC THAN CONVENTIONAL SYSTEMS—An automated flowcharting system for computer program documentation has been created by Applications Programming Company, Moorestown, N. J. Dynachart is written in COBAL format and is especially applicable for computers such as the RCA Spectra 70 and the IBM 360 Series machines.

A major advantage of the Dynachart is the ability to put as much as 100% more logic per page than conventional flowcharting systems such as Autoflow. This is made possible by creating parallel logic chart flow in much the same manner as an analyst would define his own logic, using vertical rather than horizontal paths. In addition to improving clarity of information flow, this approach eliminates much wasted page space and economizes on the physical size of the documentation. Dynachart can generate charts at the rate of from 100 to 200 statements per minute.

All cross references are provided in-line eliminating the need for searching back and forth for reference points. References to a name are included at the point where the name is defined in the program. References to source statements are included above each logical block.

MOTOROLA EXPANDS MHTL™ INDUSTRIAL LOGIC LINE—Motorola Semiconductor Products Inc. has announced a major expansion of its line of high-threshold logic (MHTL), a digital integrated circuit family capable of operating in the high electrical noise encountered in industrial environments. MHTL finds application in numerical control, supervisory equipment, computer peripheral equipment and other logic systems used in industry. It is also compatible with discrete components.

The high-threshold logic was developed for applications requiring higher inherent electrical noise immunity than is available with other standard logic families. The basic MHTL gate is similar to the MDTL gate, but uses a zener diode rather than a forward-biased diode in the input circuit. This results in a typical 7.5 V input threshold instead of the 1.5 V threshold of MDTL.

A loose-leaf brochure covering the MHTL family is available from Motorola. It gives general MHTL information and data sheets on each member of the family. It can be updated to include planned future additions to the line. For a copy of this brochure, write on company letterhead to Technical Information Center, Motorola Semiconductor Products Inc., Box 20912, Phoenix, Arizona 85036.

SCC RECEIVES FIRST ORDER FOR NEW TIME SHARE COMPUTER—Scientific Control Corp., Dallas, Texas, has received the first contract for its new Model 6700 time-share computer. The contract calls for Information Industries, Inc., of Los Angeles to purchase the time-share computer for in excess of $2,000,000.

The 6700 system has a central memory system capable of sustaining transfer rates in excess of 16 million words per second.

The complete system is to be installed by late 1969. Information Industries plans to utilize seven more of the Model 6700 over a 2-year period.

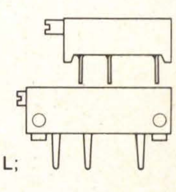
SCC has been conducting research and development on the 6700 for more than a year. It is a large-scale general purpose computer specifically designed for time-sharing applications, and will provide the remote terminal user with a completely versatile computer facility. It will have the capacity to serve simultaneously 265 users at a rate of 5,000 instructions per second. An extremely high instruction execution speed is achieved through the use of parallel processing throughout the system. Increased memory performance is achieved by minimizing memory conflicts through the use of eight independent memory modules, each of which is accessed by four independent communication buses.

Can a low-cost trimmer succeed in a high-class job like this?

Mohawk Data-Recorders speed input preparation by transferring data direct from source document to computer-compatible magnetic tape. Dale Econo-Trims are used here to control gain in a number of amplifier circuits.

Dale Econo-Trims do!

Specify Dale Econo-Trims for handling important circuit adjustments at a budget price. They combine dependability with prices that start under a dollar. Mohawk Data Sciences uses the 2317 Econo-Trim to control gain in vital tape readback amplifiers. Sealed to withstand automatic soldering, fluxing and total immersion, this ½-watt wirewound is noted for its good setting stability. It's just one of 12 Econo-Trim models now available. You can select from ½, ¾ or 1 watt models...film or wirewound elements...sealed or unsealed. Count on good delivery, too—less than 2 weeks in 1,000 piece quantities. Give Econo-Trims the chance to succeed in your circuits. They can help you get ahead, too!



SPECIFICATIONS

2300-2400 Series/Wirewound
8300-8400 Series/Film

Dimensions: 2300 & 8300 = .36″ H x .28″ W x 1.00″ L; 2400 & 8400 = .31″ H x .16″ W x .75″ L

Standard Resistance: Wirewound models = 10 ohms to 50K ohms; film models = 10 ohms to 2 Meg.

Resistance Tolerance: Wirewound models = ±10%; film models = ±10% 100 ohms thru 500K ohms, ±20% all other values

Power Rating: 2300 = 0.5 watt at 25° C; 2400 = 1 watt at 40° C; 8300 & 8400 = .75 watt at 25° C

Operating Temperature Range: 2300 & 8300 = −55° C to 105° C; 2400 & 8400 = −55° C to 125° C

Mechanical Adjustment: 2300 & 8300 = 15 turns; 2400 & 8400 = 20 turns

Mechanical Stops: None. Clutch permits overtravel without damage

Models: Sealed or unsealed. Gold-plated PC terminals or gold-plated hook type solder lugs (2300/8300 only).

Get samples and a quote quick—
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SEE OUR SPECIFICATIONS IN VSMF THE MICROFILM CATALOG FILE

CIRCLE NO. 17 ON INQUIRY CARD

INDUSTRY NEWS

PRICE REDUCTION RESULTS IN 2¢ PER BIT CORE MEMORY SYSTEM—Standard Memories, Inc., a subsidiary of Applied Magnetics Corp., has announced, effective immediately, new pricing for the entire ECOM 2.5 line of Core Memory Systems. Unit pricing has been slashed from $3,579 to $2,469 for a completely packaged 4K x 16 memory system.

According to W. B. Barnes, Vice President of Marketing, this price reduction amounts to 30-33⅓%. In moderate production quantities, the cost will approach 2¢ per bit. He further stated that this price is less than many users are presently paying for the core stack alone. Due to the scope of the reduction, Standard Memories is currently re-quoting all customers on a crash basis.

The basic design concept of the ECOM System allows the user to buy the completely assembled core memory system or the magnetics assembly and the PC board assemblies, minus the card cage and connectors.

IEEE COMPUTER GROUP ELECTS NEW OFFICERS—The Computer Group of IEEE has elected its executive officers and administrative committee members for 1969.

Named as chairman of the Group for a second term is L. C. Hobbs, president and senior consultant for Hobbs Associates, Corona del Mar, California. Elected as vice chairmen are Dr. Robert A. Kudlich, a program director at A. C. Electronics, General Motors Corporation, Milwaukee, Wisconsin and Dr. Edward J. McCluskey, Professor at Stanford University's Electronics Laboratory. Dr. Kudlich is also serving his second term as one of the Group's executive officers.

The Group's Administrative Committee, which elects half of its twenty total members each year, named the following Computer Group members to serve during 1969; David R. Brown, Stanford Research Institute; Dr. Curt F. Fey, Texas Instrument; Dr. A. S. Hoagland, IBM; Thomas E. Lindsay, Bell Telephone Labs; Milton A. Lipton, U. S. Army Electronics Command; Sam Nissim, Electronics Arrays, Inc.; Ralph J. Preiss, IBM; Rex Rice, Fairchild Semiconductor; Sei Shohara, Scientific Data Systems; John W. Worthington, IBM.

MAG DISC MANUFACTURER FORMED—Data Memory, Inc., has been formed in Mt. View, Calif., and has acquired MVR Corporation, as its first step in producing and marketing a full line of magnetic disc recording systems.

According to the Data Memory president, Ray Stewart, "The acquisition of MVR Corp.—pioneer developer of the now popular stop action and slow motion instant replay for TV sports broadcasting—will provide a solid technological base on which to expand magnetic disc recording into numerous visual and data information retrieval systems.

"It is our opinion," Stewart continued, "that disc recording is at the same threshold of potential that magnetic tape recording was 10 or 15 years ago.

"To capitalize on this potential, we will develop and build new recording devices and also manufacture in high volume recording discs for use with Data Memory systems and for sale to computer memory producers and other customers. The discs will employ a new nickel-cobalt plating which is regarded as superior to the presently used iron-oxide discs in many applications."

SINGLE SOURCE FOR IC PACKAGE WIRE-WRAPPING—Raytheon Co. and Augat Inc. are offering a single source for the production of high density, wire wrapped packaging panels and boards for dual in-line integrated circuitry.

Under an agreement announced by the two companies, Augat Inc. of Attleboro, Mass., is offering its full line of standard and custom assemblies with automatic wire wrapping services to be performed at Raytheon's wire wrap facilities in Waltham, Mass.

The plan offers a total package concept in which a single order placed with Augat covers both the panel and wire wrap service.

The agreement also makes available to customers the design and production capabilities of both companies to deliver a total package from panel design and production through wire wrap programming, wire specification, automatic wrapping, and final test and checkout.

When an order is placed, Augat Inc. produces the panels and boards for shipment in re-usable containers to Raytheon to be wire wrapped with prompt shipment by Raytheon to the customer.

CONFERENCE CALENDAR

A summer program at MIT, Monday, August 4, through Friday, August 29, 1969, will present an integrated treatment of the theoretical and practical aspects of digital systems with primary emphasis on the development of ability to design and construct moderately complex digital systems. It is intended for participants with an engineering or scientific background, but no specific experience with either integrated circuits or digital systems is required.

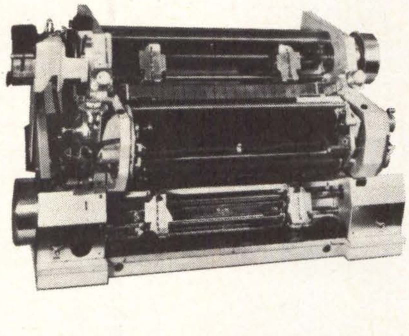
Topics to be covered include: review of semiconductor physics, fabrication of integrated circuits; analysis and characteristics of logic circuits; combinational logic design; synchronous and asynchronous sequential circuit design; computer interfacing; and the design of medium scale digital systems. Mornings will be devoted to lectures; afternoons to tutorials, laboratory experiments, and laboratory projects. The Program is planned for participants from industry and government and for faculty from academic institutions. The Program will be under the direction of Professor Donald E. Troxel and Mr. Charles L. Seitz of the MIT Electrical Engineering Department. Tuition is $1,000.

For further information, contact: Center for Advanced Engineering Study, Room 9-257, Massachusetts Inst. of Technology, Cambridge, Mass. 02139.

IEEE has constituted a special "Ad Hoc" Committee to explore interest in the technology of manufacturing, as distinguished from the product itself.

The first committee sponsored technical session entitled "Computerized Testing for Electronic Manufacturing" was held during NEREM '68 in Boston, Massachusetts. The response was so great that another session on the "Manufacturing Technology for Microelectronics" is scheduled for March 27, 1969, 10:00 A.M., at the New York Hilton Hotel during the March 24-27, IEEE International Convention and Exhibition. The session will present information relative to the impact that microelectronics has had on the manufacture of electronic equipment.

HIGH-SPEED LINE PRINTERS... WITH THE "WORK-HORSE-OF-THE-INDUSTRY" REPUTATION



MDS 5013 HIGH-SPEED PRINTER MECHANISM

MDS 5320 HIGH-SPEED BUFFERED LINE PRINTER

Line Printers in the MDS Series 5000 are designed to meet your maximum requirements. They offer you three choices: *the 5013 Printer Mechanism only for integration into your own equipment; the 5320 Buffered Line Printer (Console); and the 5300 Line Printer (Console, unbuffered). Console models are complete with MDS electronics and DC power supplies.*

All models provide extra performance factors that insure clean, crisp copy on forms 4" to 20" wide, including sprocket strip, 22" long (maximum), and up to 6 parts. Print speed is 1000 lines per minute with 64-character set... up to 1250 lines per minute with reduced character set. Line length is 120 columns (132/136, 160 optional).

MDS 5013, the high-speed rotating drum, on-the-fly Printer Mechanism, is the vital center of every Series 5000 unit. It contains the critical components that have won the "work-horse-of-the-industry" reputation for Series 5000.

Ask for full details about: Dual Tractor Paper Feed; Improved Clutch/Brake Mechanism with vacuum clean-out system; Tape Control Vertical Format with standard 8 channels (12 channels optional); Improved Ribbon Tracking Mechanism; New Fibre Optics System with only 3 light sources... plus many other MDS features.

Phone or write for folder-file on the MDS Series 5000 Line Printers.

FOR MORE — MEET YOUR MAN FROM MDS

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DIGITAL STRIP PRINTERS • BUFFERED TAPE UNITS
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CARD PUNCHES AND READERS
PAPER TAPE PUNCHES AND READERS

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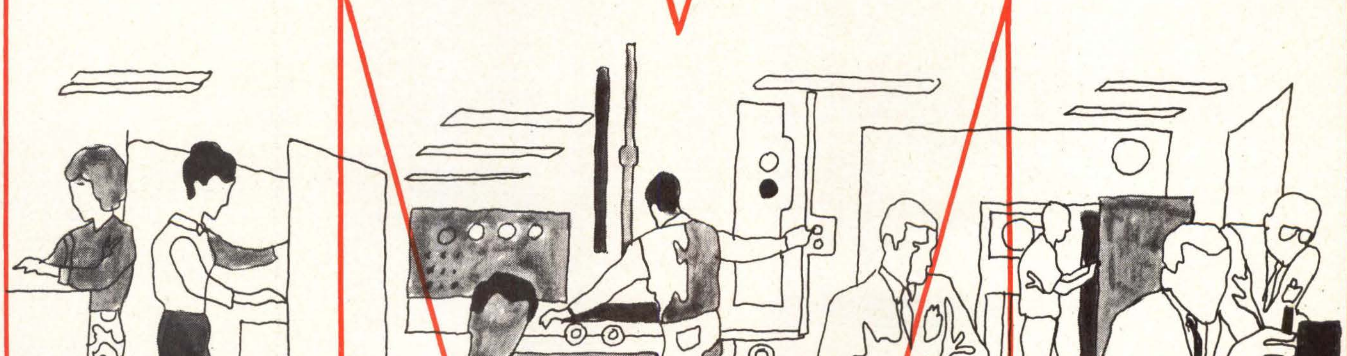


CIRCLE NO. 18 ON INQUIRY CARD

30-gage wire needs Kynar®. If you've ever tried to locate a short in thousands of feet of small-gage computer wire, you'll appreciate the toughness found in insulation of Kynar.

With twice the cut-through resistance of totally fluorinated plastics, Kynar eliminates the worry over physical damage to the wire. You can bend it, loop it and pull it over knife-sharp edges without harm. It's compatible with automatic wiring machines or hand tools. And it cuts and strips fast and smoothly.

But Kynar's toughness isn't all mechanical. It resists cleaning solvents, won't degrade with age and operates at temperatures of from −80° to +300°F.

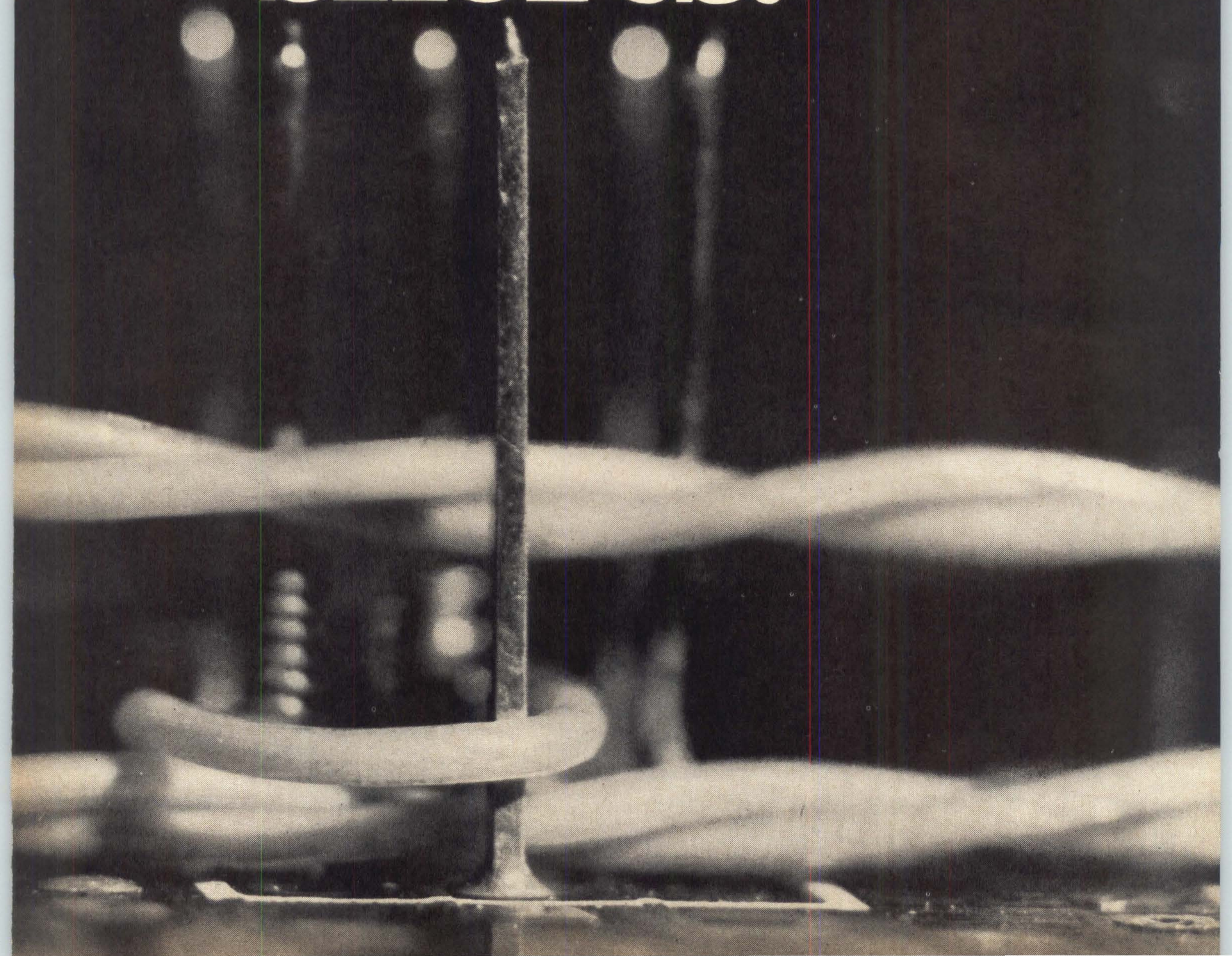
For samples and information, write: Plastics Department, Pennsalt Chemicals Corporation, 3 Penn Center, Philadelphia, Pa. 19102.

®Kynar is Pennsalt's registered trademark for its vinylidene fluoride resin

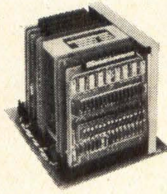
Kynar® . . . the fluoroplastic that's tough!

PENNSALT®

down with shorts.



The case for our micromemory.



There is none.

Most memories available today come in nice packages. Totally-enclosed, well-protected, and looking like they still belong to the original manufacturer.

We've got one that doesn't look like it belongs to anyone. Our newest system for industrial/commercial applications, the MICROMEMORY™ 1000, provides up to 32K bits of storage with a cycle time of 2.5 u sec for less than 7 cents/bit. And it's just as economical with space (400 cubic inches) and power (35 watts maximum).

But it has no case. The system consists of a stack and five cards of electronics that plug into an unenclosed mother board, with a single connector providing the I/O interface for integration into your system. Maintainability is enhanced by this configuration even though you'll probably never have to take advantage of it. The same advanced 3D drive technique that gives you the lower price because of a lower component count also yields a correspondingly higher MTBF.

The MICROMEMORY 1000 will fit almost anyplace in your system. Its open construction leaves access unhampered, while its low power dissipation eliminates the need for additional cooling. Mount it upside down or sideways, show it off or hide it. It looks like it belongs in your system because it does.

Price and delivery, true random access and ease of electrical interface all strengthen the case for the MICROMEMORY 1000. Write us for the full story.

EM electronic memories

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CIRCLE NO. 20 ON INQUIRY CARD

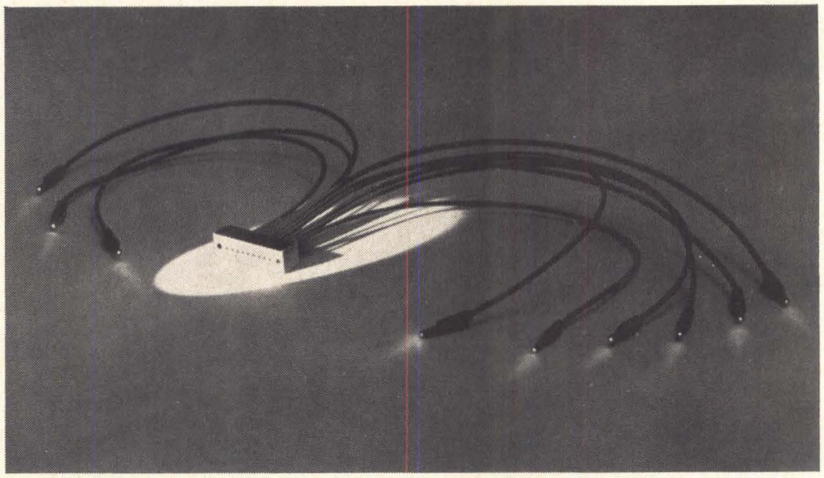
← CIRCLE NO. 19 ON INQUIRY CARD

DEVELOPMENTS

Glass Fibers Used In Versatile Read-Head

The Bendix Corporation has recently developed a universal fiber optic read-head device utilizing flexible optical quality glass fiber bundles for use with paper tape reader arrays.

The new read-head developed by the Mosaic Fabrications Div., Sturbridge, Mass., can be used with any currently available tape reader array such as the Fairchild FPA 700. This fiber optic device commands greater versatility than any other device on the market for high speed reading of information from paper tape. One reason for this significant state-of-the-art advance is the device's adaptability for modulation of each light channel so that coded information can be received at each tape hole. As a result, anyone experimenting with paper tape and photosensors, particularly design/or development engineers, will find that this fiber optic read-head assembly will provide a great deal of design freedom.



The Mosaic Fabrications Div. of the Bendix Corp. has developed this fiber optic read-head device using flexible optical glass fiber bundles.

The device consists of a machined aluminum case, or head, approximately $1\frac{5}{16}'' \times \frac{3}{8}'' \times \frac{3}{8}''$, into which individual fiber bundles are potted and sealed with high-temperature epoxy. The individual fiber bundles are ground and polished on both ends, with the free, external ends protected and sealed by an injection molded end tip. Each lightguide is 12″ long and covered with tough, but flexible, pvc jacketing.

For further information, contact: Mr. George R. Batchelder, Director of Marketing, Mosaic Fabrications Div., The Bendix Corp., Galileo Park, Sturbridge, Mass. 01518.

Australian Break-Through In Computer Design

A significant computer design breakthrough has been achieved by a research team at the University of New South Wales in Sydney, Australia. And with this achievement has come the establishment of Australia's first computer manufacturing industry.

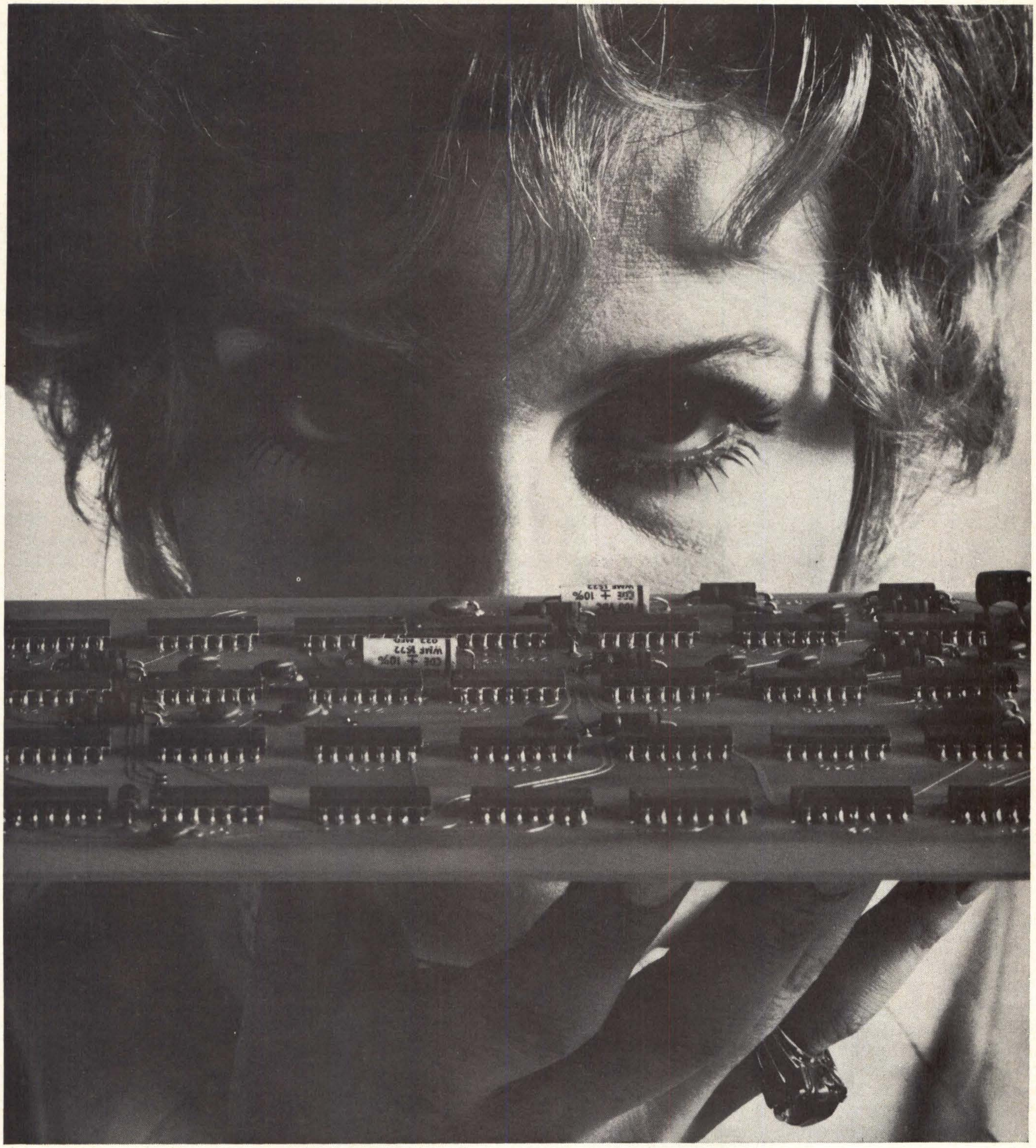
The breakthrough came with the perfection of the "Intergraphic" computer in the University's Department of Computation. It is an intermediate machine, serving as a buffer between the University's IBM System 360 Model 50 with a large storage capacity and other equipment required to link with the terminal units, and is designed to link a large number of television display units in an information utility network.

The purpose of the University project has been to provide economical graphical communication through techniques which eliminate many costly inefficiencies in other networks. The Intergraphic computer will enable man-machine communication in graphics at electronic speeds in a network of terminals which can be operated simultaneously. With other computer-driven displays equipped with electronic light pens, only one or two have been connected to a central computer at a time.

The system initially will link eight terminals and has the capacity to expand this number to 50.

Each terminal user equipped with an electronic typewriter keyboard and a light pen is able to obtain screen graphical representation from computer storage, and if so desired, to operate on these with the light pen.

The Intergraphic's design provides a network of flexible electronic terminals at no greater cost than a network of electro-mechanical teletype-writer terminals. Mass production of this Australian-designed computer is planned by a newly-formed company, Information Electronics Ltd., Canberra, Australia.



DEVELOPMENTS

Servo Drive Units Developed For Automation Equipment

Three compact, integrated servo drive units, each designed as a complete, self-contained, velocity controlled, bi-directional, electric drive in one housing, will soon be marketed by Pollak and Skan, Inc., Chicago, Ill.

The servo drive units were primarily developed for mechanical positioning applications on automation equipment in the textile, metalworking, woodworking, electronics, materials handling, computer aided graphic arts, and a wide variety of process control applications.

The system eliminates the need for costly custom assembly of components into a servo system for a particular application and allows direct computer control.

Six standard internal components are included in the basic unit: gear reducer, dc servo motor, dc servo power amplifier, velocity control amplifier, digital tachometer, and power supply. Other configurations consist of the basic unit plus additional electronic circuitry permitting the digital tachometer to serve also as a bi-directional, shaft position encoder or a precision shaft position encoder mounted directly on the output shaft. Resolutions of up to 1/10000th of a revolution of the output shaft are obtainable.

Maximum torque output of the dc servo motor ranges from 50 through 500 in-lbs. at speeds of from 400 through 40 rpm. This output torque is electronically limited with provision for pre-setting the limit.

The digital velocity command input option accepts two digit, binary coded decimal, velocity command inputs in a serial format, and, therefore, its input register is a shift register. Pollak and Skan's engineers selected a serial format to minimize the number of interconnections to the source to maximize reliability.

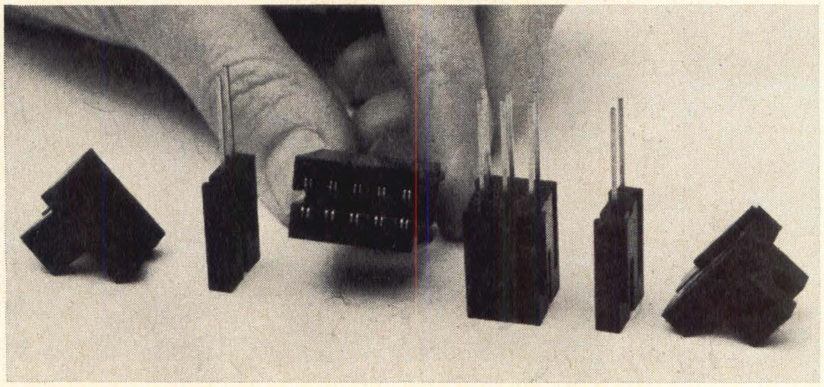
The acceleration - deceleration limit option permits the acceleration and deceleration of the load on the output shaft to be limited, if required; this limit can be either pre-set or remotely controlled. This acceleration-deceleration limit feature can be particularly useful in point-to-point positioning applications when combined with step changes in velocity commands.

Segmented Connector Permits Building-Block Approach

A four-part segmented connector which permits design engineers to use a building block approach in the fabrication of breadboard and prototype circuits for the computer and communication applications has been developed by the Parts Division of Sylvania Electric Products Inc., Warren, Pa.

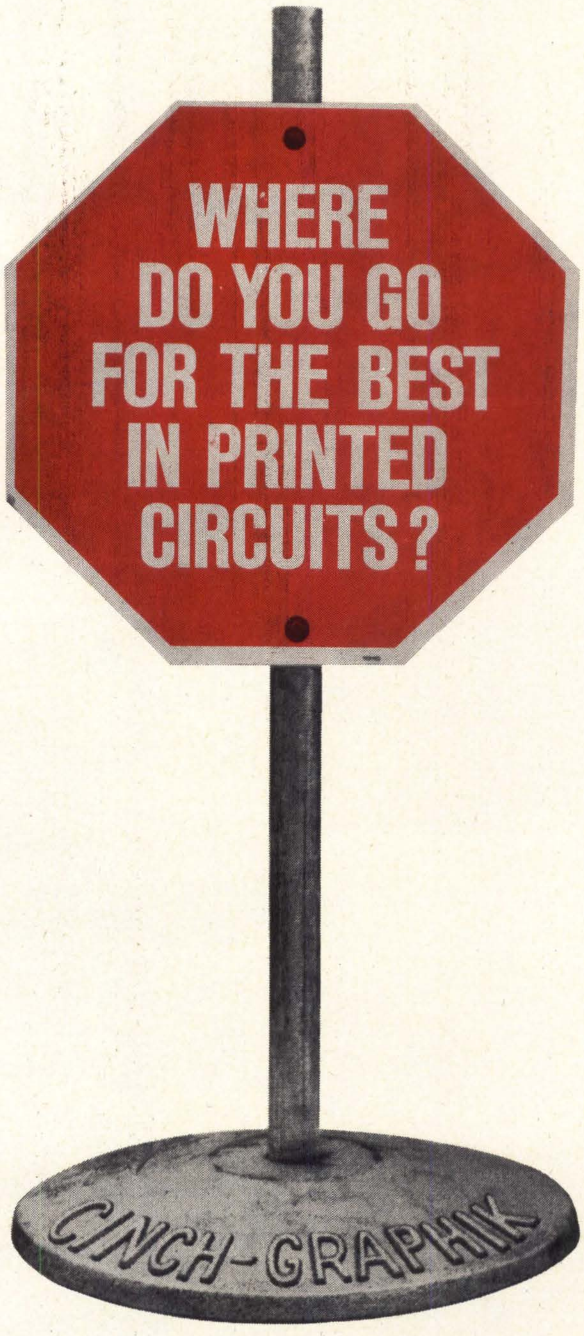
A single position connector can be assembled to any desired length up to 50 contact positions and used for circuit wiring and mechanical layout purposes. After the length of the connector is determined, the segments can be assembled by bonding the attached adhesive film.

The connector has four basic segments: end-block, single-position, three-position, and five-position. Castings are molded from a glass-filled phenolic and the contacts are spaced on a .150-inch square grid to allow hand wire wrapping. The connector will withstand 500 insertions and withdrawals of a printed circuit board with no appreciable loss of performance.



A segmented connector which can be assembled to any desired length up to 50 contact positions has been developed by the Parts Division of Sylvania Electric Products Inc. Sylvania is a subsidiary of General Telephone & Electronics Corporation.

The preloaded bifurcated phosphor/bronze contact springs provide constant pressure and added protection against vibration, corrosion, and repeated insertions of printed circuit boards .055 to .072-inches thick. The one-piece contact spring has a .630-long rectangular tail of .020 x .030-inches. Use of 18-karat gold/silver dots extends contact life and eliminates porosity problems which may occur in gold-plated contacts. A technical information bulletin may be secured by writing on letterhead stationery to Sylvania Electric Products Inc., 12 Second Avenue, Warren, Pa. 16365.



C D DEVELOPMENTS

Unique Digital Data Transmission Cable

Dynatronic Cable Engineering Corp., a division of National Wire and Cable, has developed a new series of multi-pair, digital pulse transmission cables. Designed for connecting computers with their peripheral equipment, the D-200 series cables provide up to 50 simultaneous channels for transmission of digital pulse signals with fast risetime and extremely low crosstalk. The D-200 cables are designed for use in both balanced and single-ended systems without necessitating individual shields on each pair. Thus, by eliminating these shields, surge impedance can be kept high, allowing direct integrated circuit drive, and cable dimensions can be kept small, allowing convenient connector installation. The cables are particularly well suited for use with differential line receivers, permitting 1000 ft. runs at data rates to 1 MHz.

Software Allows Simultaneous Laser Beam Plotting and Calculation

McDonnell Automation Company, St. Louis, Mo., has developed computer software that makes it possible for a computer to do millions of calculations while simultaneously driving a laser beam plotter over photographic film faster than a mile-a-minute.

The plotter uses a laser optics system to produce contour maps, engineering drawings, geophysical cross sections and various other types of graphic presentations.

Completely computer controlled, the plotter uses information from a core memory to plot one line while the next line is being computed. Scans are produced across a 40-inch film at the rate of 200 scans per inch to a depth of 10 inches per minute. A weather map 40 inches square can be produced in black, white and various shades of gray in four minutes.

Essentially, the plotter creates a picture by drawing many thin lines, each of which consists of a string of tiny dots. While the computer is driving the plotter to draw a line, the computer is also determining the placement and intensity of dots on the next line.

micro-pak™

Short on size, but long on life. The dot on the "I" is a life-sized picture of our newest transistor package, the Fairchild Micro-Pak. Just 80mils on a side, our Micro-Pak is the only plastic transistor in this size that passes rigid military reliability tests. Plastic, but with all the reliability of a metal can.

The high degree of shock resistance inherent in its inert single-block construction makes it ideal for warhead fuzes or missiles. Small, light and reliable, the Micro-Pak is the best way to go for applications from missiles to computers, submarines to satellites. And anything in-between.

Listed on the right are 26 popular transistor types available in the Micro-Pak. Electrical characteristics are similar to those of metal can equivalents. The transistors can operate with junction temperatures up to 175°C and dissipate up to 300mW doing it. Three radial ribbon leads make it easy to incorporate into PC board layouts, hybrid modules and other high density configurations. Write for full specifications.

Or, if you already know what you want, see your Fairchild distributor. He's got them in stock, in quantity.

FAIRCHILD
SEMICONDUCTOR

PART NUMBER	PRICE (100-999)	PART NUMBER	PRICE (100-999)
FX3299	1.60	FX2894A	3.00
FX3300	2.00	FX4960	6.00
FX3962	2.40	FX918	2.20
FX3963	3.20	FX2483	2.00
FX3964	3.20	FX2484	2.40
FX3965	3.70	FX709	2.00
FX3724	4.00	FX2368	1.20
FX3725	5.00	FX914	1.20
FX4046	3.00	FX2894	2.00
FX4047	4.00	FX4034	1.60
FX3013	5.00	FX4207	3.00
FX3014	3.00	FX3502	3.00
FX2369A	1.30	FX3503	5.00

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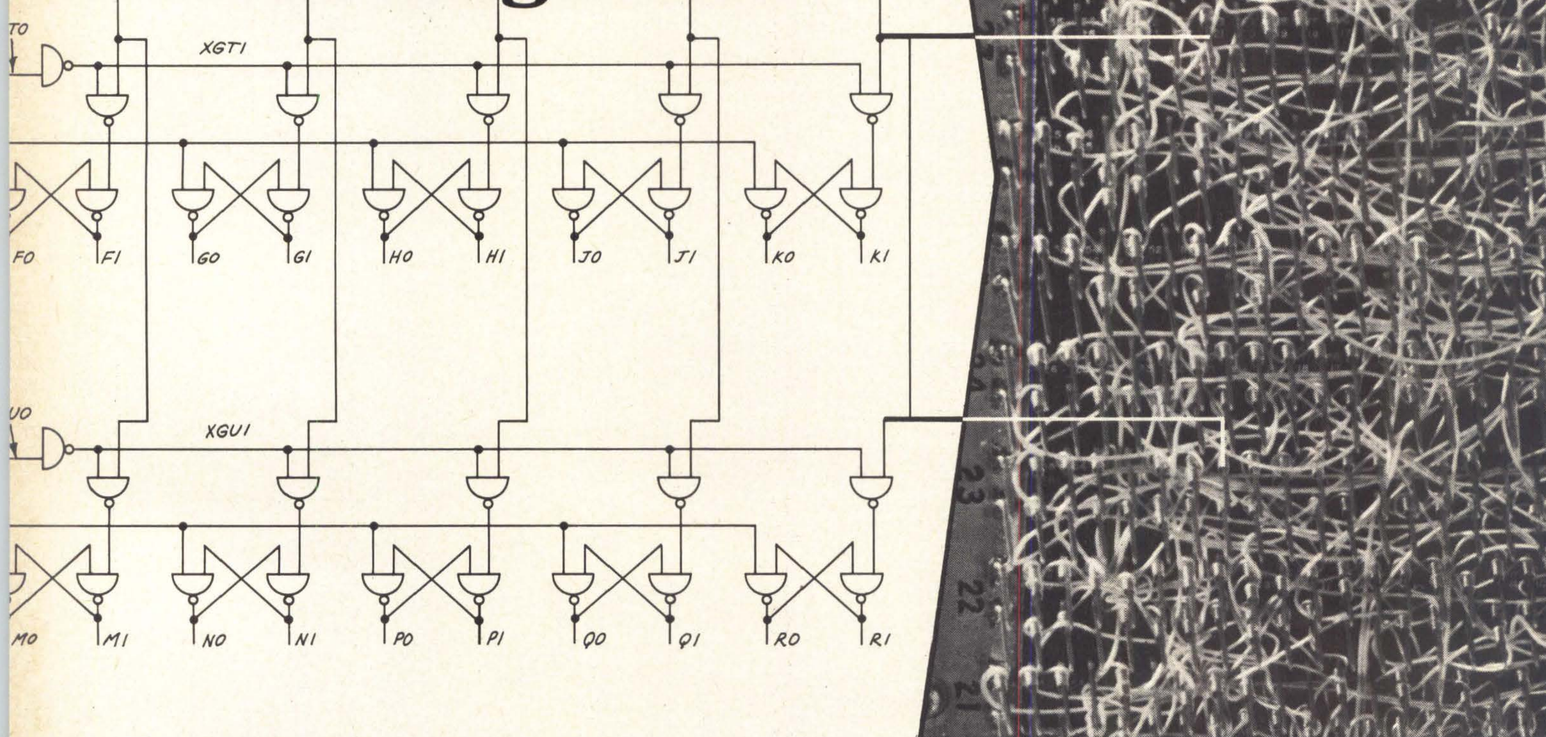
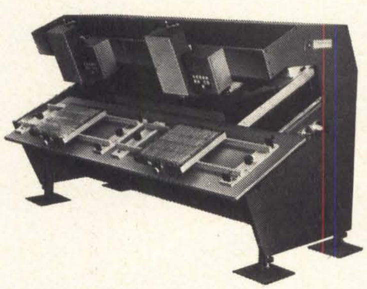
CIRCLE NO. 68 ON INQUIRY CARD

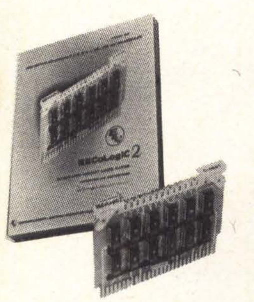
New Computer-Automated wiring service for EECoLogIC® 2...



converts lines on paper to wires on hardware



SAVES YOU TIME & MONEY – You supply a simple PIN LOGIC LIST* (not a costly and time-consuming wire list). Making a Pin Logic list for 1000 wires takes but 1 working day to complete.



EECO's entire EECoLogIC·2 line of digital logic cards is designed with automatic machine wiring capability. Send for catalog.

FLEXIBLE – We will provide wired EECoLogIC·2 hardware using Termi-Point® or Wire-Wrap® techniques...or you can do the wiring on your machine ...or use any qualified vendor.

LOW COST – Typical costs .... for prototype: 20 cents per wire
for production: 15 cents per wire

Send for an illustrated brochure today.

*You simply choose the module and write the signal name by each pin number. You *don't* worry where the wires go or the order of listing.

COMPONENTS DIVISION

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*

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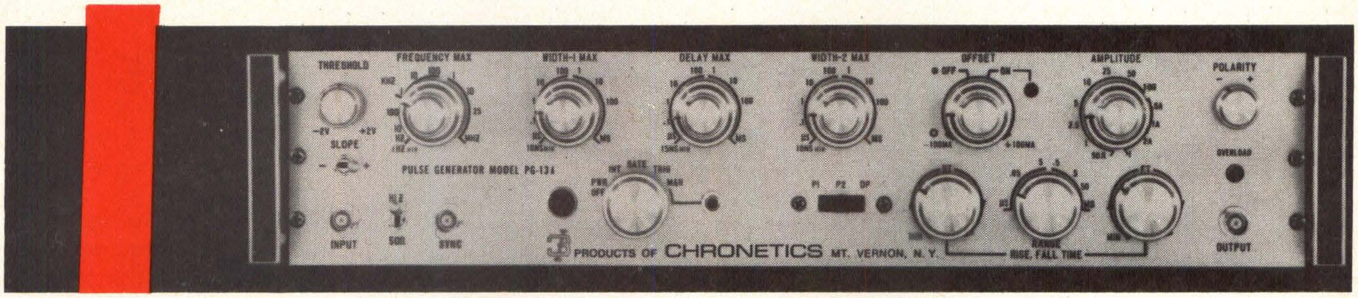

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A display should match the characteristics of a computer to the visual system of man. Important relationships, together with some of the practical limitations of a CRT display and its ancillary equipment, are reviewed in this article, concluding with a short review of design trends.

DESIGN CONSIDERATIONS FOR COMPUTER DRIVEN CRT DISPLAYS

Joseph E. Bryden

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Cathode ray tube displays have become a very important interface between visual communication channels or computers and the human observer. This article reviews constraints within this interface and discusses some of the more important inter-relationships between parameters.

The information to be displayed may have many different characteristics, and these are generally identifiable by the function which has to be performed. For example, page print and tabular data are assemblages of predefined symbols in lines and columns. The data is changed relatively slowly at the typing and reading speeds of an operator.

Graphics introduces an additional degree of freedom because lines may be written anywhere on the screen and the writing may have no predetermined form. In the simplest application black-and-white graphs and other line diagrams are generated, but sophisticated displays are able to present elaborate diagrams in multi-color, and may be given dynamic characteristics to show changes with time. Graphic displays may have information refresh rates ranging from a change every few seconds to thirty per second to give an optical impression of continuity of motion.

Television displays are really a special case of the graphics display in which every elemental area of the screen contains useful information. Consequently, the total screen area must be scanned, and this is most conveniently achieved with a raster.

Perhaps, the first question to which a display designer addresses himself is how much information can, or must, be displayed. An observer's eye sharply resolves detail within a central area encompassed by a conic angle of two or three degrees; as the angle increases the detail which can be resolved is greatly reduced. Therefore, it becomes a question of ground rules as to whether the eye is allowed to select the required information by directing the center of vision to a part of a large screen, or whether a smaller screen should be used with facilities to electronically zoom or filter by class of information; such arrangements would make use of a very large field of stored data of which only a small part would be displayed at any instant.

At the operator-screen interface, there is the problem of relating the efficiency and comfort of an operator to physical parameters that are meaningful to engineers. We may assume that the ideal display would convey the maximum amount of information in the shortest time with the maximum accuracy. To test, or investigate such displays, implies a requirement for an "average" operator. There can be no such individual; the best our human engineering colleagues can do is to develop a statistical relationship between rapid, accurate reading and various combinations of measurable display parameters such as size, resolution, brightness, contrast and refresh rate. The engineering problem is one of optimizing the environment and realistically relating trade-off between the measurable display parameters, cost and reliability.

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OPERATOR-SCREEN INTERFACE

The size of the screen is primarily determined by the required viewing distance, which is usually settled by knowing the number of viewers that have to be accommodated.

The field of vision and minimum resolvable element are characterized by conic angles at the eye. When an object is being examined, the eye will sharply focus the field within a conic angle of about three degrees; this field of vision is sometimes referred to as foveal vision. With less appreciation of detail, the eye recognizes patterns over a conic angle of at least 120 degrees. From a system point of view, it is wasteful to generate information beyond the requirements of the foveal field. However, the eye usually scans up and down and sideways, and a larger field gives the eye the opportunity to select the information of interest.

A guide for suitable viewing angles can be obtained by considering the dimensions of newspapers and books which are typically read at a distance of about 16 inches. The page of a book is covered by alphanumerics or diagrams over an area of 4 inches by 7 inches; this gives a horizontal viewing angle of ± 7.1 degrees and a vertical angle of ± 12.3 degrees. Although the printed area of a newspaper is much larger (14 inches by 21 inches), it has been found necessary to introduce columns to facilitate reading, and diagrams or photographs are seldom larger than the page of a book. Other examples are the typical typewritten page and the printed area of a page of this magazine. If we apply these guide lines to a console for two operators with a viewing distance of 30 inches, a generous screen area would be 16 inches by 20 inches. For a display console which is designed for a single operator, a comfortable distance between the eye and the screen is about sixteen inches and a screen area of 8 inches by 10 inches would be adequate. Consoles designed for one or two operators are often equipped with a keyboard and control buttons which must also be considered in terms of user comfort.

Resolution (visual angle) is a function of contrast ratio, brightness, the form of test object, color and time. Figure 1 shows some curves expressed in the commonly used parameters for displays with values obtained from Reference 1. The tests were conducted with a black test pattern (Landolt "C") on a white background. It will be observed that:

1. The maximum resolution (smallest angle) is approached when the contrast ratio exceeds 2.
2. Resolution is much less dependent upon brightness than upon contrast, at least for foveal vision.

However, at very low brightness levels, and well below the levels of interest for almost all displays, the central part of the retina becomes inoperative. The result is colorless vision of very poor resolution.

Yellows and greens give better resolution than reds and blues and parallel lines may be discriminated more easily than point sources. Under optimum conditions, the threshold of resolution for most people is about 30 seconds of arc and resolution of a display system could be required to introduce negligible degradation compared to that of the eye.

Changing the deflection sensitivity of a CRT dis-

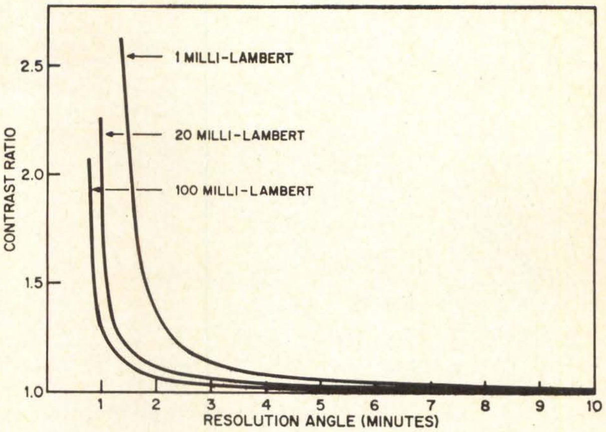

Fig. 1 Visual-angle contrast.

CONTRAST RATIO

A few comments on contrast ratio are necessary to avoid ambiguity. In most optical experiments (such as Reference 1) involving resolution and contrast ratio, the test pattern, such as the "Landolt Test Object," is black against a relatively large white background. It is, therefore, conventional and appropriate to express contrast ratio as:

$$C_o = \frac{B_s - B_o}{B_s} \tag{A1}$$

where,
B_s is the screen, or background, brightness
B_o is the brightness of the object

With a cathode ray tube display the writing is usually brighter than the background, and the most frequently used form to express contrast is:

$$C_t = \frac{B'_s + B_w}{B'_s} \tag{A2}$$

where,
B'_s is the brightness of the screen from ambient light
B_w is the brightness of the written line when ambient light is excluded

Legibility is not highly dependent upon whether symbols are written dark on a light background, or light on a dark background.[10] When measurements have been made with a light background the results are converted to the conventional form for CRT contrast by:

$$C_t = \frac{1}{(1 - C_o)} \tag{A3}$$

This conversion does not account for any effect that the difference in average brightness of the field may have on the eye. In Equation A1 the average brightness is high and approaches B_s, whereas in Equation A2 the average brightness is low and approaches B'_s. It will be seen from Fig. 1 that brightness does not have too much effect; the curves of that figure were obtained with a bright screen, and the brightnesses stated are essentially the averages for the fields.

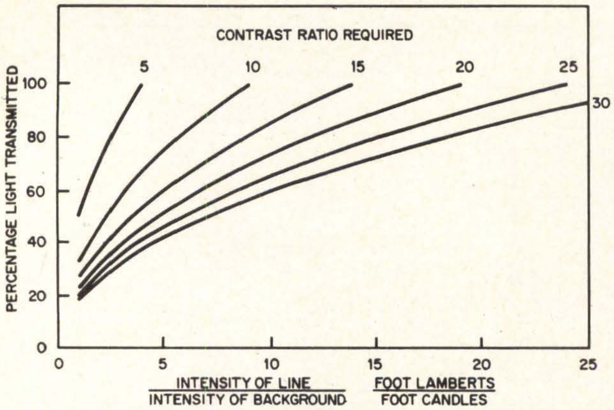

Fig. 2 Loss of light-energy by contrast-filter.

play is equivalent to simultaneously changing the magnification and aperture in an optical system. It allows the operator to examine a large field in coarse detail, or a smaller area in finer detail. With this possibility, we can reconsider the required resolution in terms of the detail required in a relatively small viewing area; the operator would be provided with a "zoom" control. For example, he could start with a map of the United States showing state lines and capital cities. He could zoom to, say, a full screen display of part of Boston showing street names. Such a zooming capability usually implies filtering the data in discrete steps as the magnification is changed.

At this point, we will consider the range of writing intensities which will be displayed; that is, the grey scale.

The difference in brightness (δB) between two areas, that can be detected is a function of the average brightness (B) of the field; our range of interest is between about one and a hundred foot-lamberts. In this range, a difference ($\delta B/B$) of 2 or 3 percent may be observable, especially if the boundary is sharply defined and the two areas are abutting.[2] If the areas are well separated, estimates of relative brightness become quite erratic.

Although the range of luminance over which the eye adapts is very large, a television picture seems to have an acceptable range if the black to highlight ratio in any scene is between 50:1 and 150:1. The illusion of a change of scene from bright sunlight to dim moonlight may be achieved with a change of average brightness of less than 10:1; some loss of detail in the dark parts of the dim scene seems to enhance the illusion. A satisfactory total range of brightness is probably about 200:1.

A graphic display must have a minimum contrast ratio in excess of two (Fig. 1). A few levels of line brightness may be required to aid the operator in identifying different classes of data, and intensity ratios for successive steps of 2:1 would seem to meet both the resolution and widely separated data requirements. Therefore, the maximum contrast ratio (brightness of line to background) would have to exceed 2^n, where n is the number of intensity levels. If the operator is allowed to adjust the maximum brightness over a range of A:1, the maximum contrast ratio would have to exceed $A2^n$:1.

Upper limits of brightness in written areas and contrast would be set by the discomfort caused by glare; in Reference[2], a simple formula is used to define the threshold of discomfort:

$$B_g^{1.6} \cdot \omega^{0.8}/B_F \geqslant 150 \qquad (1)$$

where,

B_g is the luminance of the glare area, foot lamberts
B_F is the general luminance of the field, foot lamberts
ω is the angular area of the source of glare, steradians

In displays, the discomfort threshold from glare is not likely to be reached unless brightness levels of several hundred foot lamberts are used. However, the ability to differentiate between two brightness levels may be seriously reduced by the close proximity of other brighter sources; it is doubtful whether more than four brightness levels can be successfully used in a display to distinguish classes of data.

The peak brightness level is usually chosen to equal, or slightly exceed, the peak brightness of objects and panels that are within the field of vision of the operator. A sheet of white paper with normal office illumination may be expected to reflect light with an intensity of about 70 foot lamberts. However, direct illumination should be shielded from the surface of a display console and a line brightness of 50 foot lamberts produces good results in most office areas. In rooms of very low ambient light level, line intensities may be as low as two foot lamberts.

Loss of contrast is particularly disturbing when it is caused by specular reflection, usually from the glass-air boundary of the faceplate. Common practices for minimizing specular reflection are:

1. Etching the surface of the glass; this technique tends to loose resolution by scatter.
2. Depositing an anti-reflective coating on the surface of the glass; fabrication is relatively expensive for the replaceable CRT.
3. Placing a directional filter on the surface of the glass; the viewing angle is restricted and there is some loss of resolution.
4. Placing a circularly polarized light filter over the surface of the glass. Usually, the polarizer incorporates an anti-reflective coating.

In rooms with high levels of illumination, a contrast filter will be required because contrast is lost by reflection of diffused light from the phosphor. Such a filter is usually a wide spectrum attenuator to provide twice the loss for the ambient light, which must pass through it twice, as for the light emitted by the phosphor. The improvement in contrast is obtained at the expense of a necessary increase in writing intensity (see Fig. 2). Sometimes, a circularly polarized filter is used to attenuate (typically, about 3.5:1) the non-specularly reflected light from the phosphor; the advantage is that it will also effectively eliminate the specularly reflected light from the glass.

Light rays from a point on the phosphor surface are radiated in all directions and travel through the glass faceplate of the CRT. When these rays reach the boundary of the faceplate, they will pass through it if the angle to the normal is less than the critical angle. If the angle is greater than critical, the light will be internally reflected and escape through some other part of the faceplate. Typically, internally reflected light may be fifteen percent of the directly radiated light and may cause light to be radiated from an unenergized area of the screen with a consequent reduction in contrast. Several techniques have been used to minimize this effect:

1. Thin layers of phosphor without a reflective backing will allow the reflected light to escape through the phosphor. These screens give good resolution, but poor efficiency.
2. Fiber optic faceplates to channel the radiation. Such faceplates are very expensive, even for medium sized screens.
3. Faceplate using lossy glass to give attenuation; although this technique is inefficient, it also reduces loss of contrast from ambient light.

For a television picture, there is no doubt that color conveys mood and increased information. With data on a computer driven display, it can be used to identify different classes of information; flagging urgent, or unusual data is an important application. When the amount of displayed data is large the judicious use of color may avoid the loss of critical lines by over-write. However, using color must be treated with caution unless operators are carefully screened for color blindness. A limited number of colors may be used with fair safety.[3]

Some of the dynamic factors will now be discussed. The most fundamental consideration is the frequency of updating the displayed information. For a truly dynamic display, such as television, or "live" diagrams, the eye requires at least twenty pictures per second to avoid an impression of jerking. If the display shows data which are being read, or controlled by an operator, his reaction time usually determines the speed of updating; it is typically about a tenth of a second. In some cases, the display shows the output of a sensing system which takes samples at well spaced intervals; for example, a radar system in an area search mode may renew information every five seconds.

The sensation of flicker is determined by the persistence of the eye. The threshold of flicker perception, also known as the critical frequency, for any particular observer, is a function of:

Refresh Rate	Surrounding Surface
Brightness	Persistence of Phosphor
Color	Angle of Vision
Size of Illuminated Area	Movement of displayed data
Ambient Light	

Most observers find that the critical frequency associated with small angle (foveal) vision is more repeatable than that obtained from wide angle fields and peripheral vision. Figure 3 shows the minimum refresh rate to avoid flicker with small angle vision, as a function of screen phosphor and brightness. If a short persistence phosphor is used, the critical frequency which satisfies 90 percent of all observers is about 38 Hz at 50 foot lamberts. It is estimated that 99 percent would be satisfied with about 42 Hz. The critical frequency which satisfies wide angle vision is often about 5 Hz higher than that for foveal vision. Therefore, a flicker free display would be expected to have a refresh rate greater than 47 Hz.

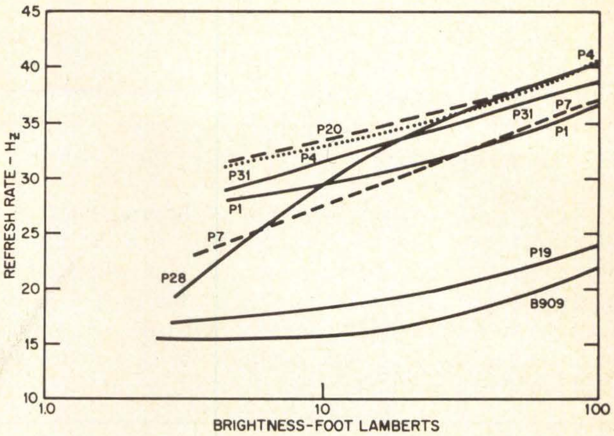

Fig. 3 Lowest refresh rate which will give freedom of flicker for 90 per cent of observers.

A cathode ray tube is a device in which the light produced by the spot is time shared between all the possible writing addresses. To avoid flicker, each element of writing must be refreshed at a high enough frequency. The stability of the refresh frequency is fairly critical, because the eye can detect an instantaneous change of about 2 percent in the number of energy exposures per second.

TABLE 1

Phosphor	Persistence (seconds). Time for brightness to fall to 10% of initial value
P4	60×10^{-6}
P20	50×10^{-6} to 1.8×10^{-3}
P31	38×10^{-6}
P28	600×10^{-3}
P7	25×10^{-6} to 75×10^{-6} 400×10^{-3}
P1	24.5×10^{-6}
P19	200×10^{-3}
B909	10

It is interesting to compare the results of subjective flicker tests with published curves of persistence for the phosphors. From Table 1 and the curves in Fig. 3, it is implied that the critical frequency is only slightly affected by the persistence of the phosphor, unless it is long compared to the persistence of the eye and is free from a primary flash. Long persistence phosphors are unattractive for computer driven displays because they produce smears and ghosts from previously written information.

Another phenomenon which is disturbing to an operator is the apparent "jump" which may occur when a short persistence phosphor is used. If the observer moves his eye fairly rapidly, he retains the impression of the positions of light on the screen produced by the last exposure; new data appears in a new position on his retina and he momentarily sees two pictures which is interpreted as a position jump. A long persistence phosphor avoids this effect; alternatively some relief may be obtained from a fairly bright frame surrounding the screen.

The flicker phenomena associated with peripheral vision do not seem to be well understood. The peripheral flicker effect is particularly annoying when several displays are in a row, and an observer sees the screen of an adjacent display out of the corner of his eye. Not only does the critical frequency appear to be higher for peripheral vision, but it seems that an impression of flicker is produced by movement of the eye. This movement effect may have a similar mechanism to the illusion of jump previously discussed.

The legibility of symbols and alpha-numerics is a subject worthy of more consideration than it is usually given by equipment designers. The objective is to have characters which are unambiguously recognized by an observer. Dr. Kinney and colleagues have conducted a series of tests to find the causes of confusion with the most common alpha-numeric formats.[4]

Mutual	One-Way
O and Q	C called G
T and Y	D called B
S and 5	H called M or N
I and L	J, T called I
X and K	K called R
I and 1	2 called Z
	B called R, S, or 8

Confusion associated with X, K, I, 1, 2 and B has accounted for more than half of the errors in some tests.

Character styles may range from crude, utilitarian forms to classical printer's fonts. These variations should more properly raise questions of aesthetics, rather than functional efficiency. A guide line for good readability is that the line width should be between a tenth and a sixth of the character height and the relative accuracy of the line positions should be within half a line width.

Other features of characters which determine their packing density on the screen are: character spacing, line spacing and character aspect ratio. When high density is required, the spatial interval allowed for a character may be varied according to the width of the character.

It has been shown that words written in lower-case characters tend to have a lower legibility than those written in upper-case; furthermore, the observer appears to have a slightly quicker response time when identifying an upper-case word.[5] These results imply that displays used in applications where accuracy is of the utmost importance may well take advantage of an improvement in reliability by restricting the character repertoire to upper case symbols.

THE CATHODE RAY TUBE

The luminous energy conversion characteristics of a CRT may be analyzed, with sufficient accuracy, in terms of beam current density, beam acceleration voltage, spot diameter, writing speed and phosphor characteristics. Usually the performance of the phosphor includes the thin aluminized backing which eliminates ion burn and increases the forward light output.

For any choice of phosphor and beam acceleration voltage, the brightness increases with the current density at the screen. The maximum current density is a function of spot size and allowable cathode loading. The convergence of electrons in a beam bundle to a point on the screen is limited by space charge effects. Space charge forces are shown to be a more important limitation than cathode loading[6], and an equation is developed, based on earlier work by Schwartz which defines the maximum current density which can be obtained in a focused spot.[7] An approximation of that equation within the range of r_s/r_1 between .03 and 3, may be rewritten as,

$$\rho_s \approx k\, V^{3/2} \Big/ \left(\frac{r_s}{r_i}\right)^{1.15} \cdot Z^2 \text{ amps/cm}^2 \qquad (2)$$

where

r_s radius of beam, or spot, at screen
r_i radius of beam at exit of gun
k 5.75×10^{-5}
V beam acceleration voltage
Z distance from exit of gun to screen (cms)

Since brightness is almost proportional to current density, Equation 2 shows that a CRT with a short beam throw distance will have a higher brightness capability than one with a long throw; furthermore, the maximum brightness is almost proportional to the beam bundle radius at the gun.

When the beam is deflected, the spot is defocused; however, magnetic and electrostatic deflection fields have distinctly different mechanisms. With magnetic deflection, the speeds of the electrons after passing through the deflection field are unchanged. With electrostatic deflection, electrons in different parts of the beam bundle have their speeds affected by different amounts. Relative changes in electron speeds cause defocusing. The increases in spot radius as a function of deflection angle (λ) are,

Magnetic Deflection:

$$\delta S \approx r_i (\sec \lambda - 1) \qquad (3)$$

Electrostatic Deflection, with deflection plates of length l:

$$\delta S \approx \frac{Z}{l} \cdot r_i (\sec^2 \lambda - 1) \qquad (4)$$

These equations assume an ideal field which is sharply bounded by parallel planes, and is uniform within those bounds. Figure 4 makes a comparison of the defocusing caused by electrostatic and magnetic deflection. It clearly shows why cathode ray tubes using electrostatic deflection have small maximum deflection angles (usually less than ±20 degrees) and use astigmatic focusing correction. Magnetic deflection is superior to electrostatic deflection when high brightness levels are required; if the size of the screen is fixed, Equation 3 shows that the defocusing is reduced by keeping the maximum deflection angle small, that is by using a long beam throw distance (Z). Equation 2 shows that the highest brightness for a given resolution is obtained by making Z as short as possible. In practice, the conflicting requirements for throw distance (Z) are resolved by making the beam bundle radius (r_i) sufficiently small and the beam acceleration voltage (V) sufficiently large for the brightness and resolution required.

Usually, the phosphor is chosen for color and persistence. It is convenient to combine the photopic spectral luminous efficiency with the phosphor efficiency to assess the effective brightness of the screen as seen by an observer. There are internationally adopted standards for Relative Luminous Efficiency, often loosely referred to as the visual response of a "standard observer." These standards are a useful guide, but many users are not convinced that they are truly representative.

Table 2 lists a few of the hundred, or so, phosphor variations that are manufactured. It will be seen that there is a considerable range of visual efficiencies.

TABLE 2

(1) Screen	(2) Color	(3) Composition	(4) Foot Lamberts	(5) Foot Lamberts Per Hz Refresh K (Ave.)	(6) α
P31	Green	ZnS; Cu	12.0	0.2000	0.917
P32	Purplish Blue Yellowish Green	CaO • MgO • SiO_2; Ti	9.5	0.158	0.790
P20	Yellow Green	Zn/CdS; Ag	9.2	0.153	0.915
P2	Yellowish Green	ZnS; Cu	9.1	0.151	0.780
P28	Yellow Green	Zn/CdS; Cu	5.2	0.087	0.888
P7	White Yellowish Green	ZnS; Ag	5.2	0.087	0.888
P4	White	ZnS; Ag; Zn/Cd. S; Ag	5.2	0.087	0.888
P1	Yellowish Green	Zn_2SiO_4; Mn	3.8	0.064	0.945
B909	Orange	Mg.F_2; Mn	3.6	0.060	0.850
P14	Purplish Blue Yellowish Orange	Zn/CdS; Cu	3.2	0.053	0.914
P19	Orange	Zn. F_2; Mn	3.0	0.050	0.856
B908	Orange	Mg. F_2; Mn	1.4	0.023	0.822
P11	Blue	Zn. S; Ag	1.2	0.020	0.883

Luminous output of typical phosphors measured under the following conditions:

Writing Speed:	1 inch/microsecond
Refresh Rate:	Column 4—60 Hz
	Column 5— 1 Hz
Aperture Size of Photometer:	12 mils
Spot Size (half brightness diameter):	18 mils
Beam Acceleration Voltage:	14 KV
Beam Current	25 microamps

NOTES: *(1) α in column 6 is an approximation for the range in writing speed between 10^4 and 10^6 inches per microsecond.*
(2) All phosphors have aluminized backing.
(3) Measurements are made in a typical CRT and include glass losses.

An empirical formula has been derived which defines the average-brightness of a line within the normal range of parameters for a practical display with final anode potential of the CRT between 10 KV and 18 KV:[8]

$$B_T = K \cdot R \cdot \left(\frac{0.72\, I}{S \cdot D}\right)^{\alpha} \cdot \left(\frac{V}{14}\right)^{\beta} \text{ foot lamberts} \qquad (5)$$

where K, and α define the screen characteristics and

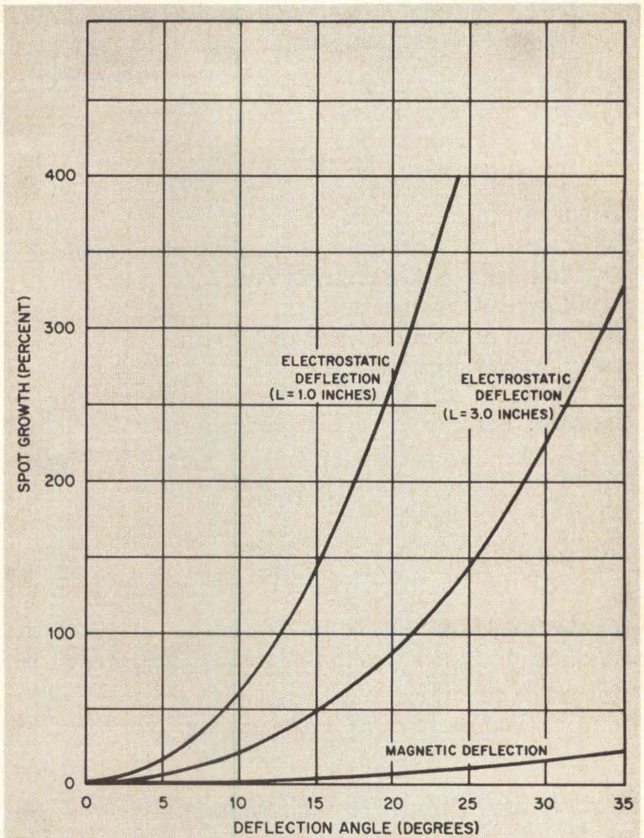

Fig. 4 Defocusing caused by an ideal deflection field.

Beam throw distance: 20 inches
Length of deflection plates: L inches
Spot diameter: 20 mils
Beam bundle diameter in deflection field: 20 mils

are given in Table 2, columns 5 and 6.

- R is the refresh rate in Hz
- S is the writing speed in inches per microsecond
- D is the half-brightness diameter of the spot
- I is the beam current in microamps for a spot having a half brightness diameter D
- V is the accelerating voltage in kilovolts
- β has a range of values probably between 1.3 and 2. (As the rate of energy conversion is increased, the color centers of the phosphor will become saturated and β will become less than unity.)

It is now possible to discuss the effect of the choice of operating parameters on the design of the supporting electronics. Consider the total frame time ($T = 1/R$) to compromise two parts. The active writing time when the beam is unblanked, and the positioning time when the beam is blanked. Positioning will be accomplished as quickly as possible with due regard to the size and cost of the deflection amplifiers, and it will be assumed that the positioning time is fixed at T_p per frame.

Brightness is proportional to

$$RS^{-\alpha} = R\left(\frac{1}{R} - T_p\right)^{\alpha} \Big/ W^{\alpha} \qquad (6)$$

Where, W is the total written line length.

The maximum brightness will be obtained with the lowest refresh rate (R). Furthermore, the bandwidth of the video circuits will increase with refresh rate. Therefore, it is good economics to use a refresh rate close to the critical frequency of flicker. Very low rates which require long persistence screens are not attractive because of smearing when information is updated.

With a magnetic field, the deflection angle

$$\lambda = \sin^{-1}\left(\frac{\kappa \cdot L^{\frac{1}{2}} \cdot I}{V^{\frac{1}{2}}}\right) \text{ radians} \qquad (7)$$

κ Constant dependent upon yoke dimensions
L Inductance of deflection coil
I Current through coil
V Beam acceleration voltage

The maximum back EMF across the deflection coil will be equal to L di/dt. The maximum rate of change of current for a full deflection angle change of $+\lambda_m$ to $-\lambda_m$, occurring in time T_r will be $2I_m/T_r$. Therefore, the maximum back EMF will be,

$$V_m = L\frac{2 \cdot I_m}{T_r} \qquad (8)$$

and the peak dissipation of the output stage of the deflection amplifier (excluding circuit losses) will be,

$$P = V_m \cdot I_m = \frac{2 \cdot L \cdot I_m^2}{T_r} \qquad (9)$$

which is proportional to the beam acceleration voltage, V.

Therefore, when resolution and brightness requirements are met by increasing the beam acceleration voltage, larger deflection amplifiers will be required. The limitation of performance is mainly determined by the availability of fairly high-speed, high-power transistors for the output stage of the amplifier, because the maximum brightness tends to increase at about $V^{3.5}$ for a direct view CRT in the normal range of operation (see Eq. 2 and 5).

If more data has to be displayed, the writing and the deflection speeds will have to be increased. To maintain the same brightness with increased writing speed, the beam acceleration voltage will also have to be increased. In practice, with full screen deflection times of less than 10 microseconds, the finite response time of the deflection coil field becomes important, and small gains in time are only obtained with a large improvement of the amplifier; that is, its current changing capability must increase by a greater ratio than the increase in data loads. Thus, an increase in data display capability of a high capability display is obtained with a disproportionately large increase in deflection amplified dissipation.

At this point, it is enlightening to consider the beam-on to beam-off duty cycles for different display modes. A television picture is generated by a dot pattern, ranging from all resolution areas white to all black. Allowing for flyback intervals, an all white display will achieve about a 90 percent duty cycle. However, the average scene will have a very much lower duty cycle.

The duty cycle characteristics of a computer driven alphanumeric and graphics display are very different from those of a television display; Table 3 summarizes the performance of a typical high-grade computer driven display for mixed alphanumerics and graphics.

It will be seen that only 7.0 ms is used for writing in each frame period of 16.7 ms. The remainder of the period is used for beam positioning, set-up and safety margins.

If the spot were to be used to write all lines at the maximum speed for which the display was designed, all the writing would be accomplished in 3.2 ms. The difference between the actual time taken (7.0 ms) and the ideal is attributable to a nonconstant writing speed.

TABLE 3

	Number of	Average total line length in display diameters	Total time required (μ secs)
Characters	1709	41.5	4106
Lines	832	75.0	2880
Dots	721	0.45	13
Positioning (Random)	3262	--	7487
Set-up	--	--	1044
		116.95	15530 μ secs

Maximum Writing Speed:	1/27 screen diameter per microsecond
Refresh Period:	16.7 milliseconds
Screen Diameter:	20 inches
Resolution:	12 mils (half-brightness spot diameter)
Character Size:	0.187 inches by 0.140 inches

With high data loads, constancy of writing speed eases the demands for peak-brightness imposed on the CRT. In turn, this reduces the acceleration voltage and allows faster positioning for a given dissipation of the deflection amplifiers.

One method of decreasing the amount of time used for major positioning is to reduce the average magnitude of a position change. This may be accomplished by sorting the addresses into 'boxes' defined by X_1, X_2 and Y_1, Y_2 addresses; the positions would then be sequentially taken from one 'box' at a time.

It is interesting to compare the performance of the random-positioning display, which has just been discussed, with one using a television raster to present the same displayed data. The raster resolution would have to be 12 mils and 1660 lines would be required to fill the 20 inch diameter screen. To maintain the same refresh rate a line would have to be written in about 7 μs, that is the writing speed would be about 3 inches per microsecond; this is about four times the peak writing speed used with random deflection, and four times the beam current would be required.

DISPLAY MEMORY

The displayed data are generated piece by piece, and the beam of the CRT is time shared when writing this data on the screen.

The update of data may consist of a complete replacement at regular intervals, regardless of the extensiveness of changes; or, only those elements of data which have been changed may be replaced.

There are three general techniques which provide a steady picture for the operator:

1. Refreshing the displayed information at a rate high enough to avoid the sensation of flicker. The

output load on the computer is high (50, or more, complete sets of data per second) and is usually only justified in small systems, or if the update rate is also high.

2. Storing the displayed data on the screen of the CRT. If selective erase is used it is only necessary to process changes of data. Writing speeds, computer loading, and display generation rates are all minimized with this approach. However, there are difficulties in achieving high resolution/brightness combinations, and selective erase.
3. Refreshing the displayed information from a separate refresh memory which is periodically updated by the computer.

A separate refresh memory is most frequently used, because it provides a convenient way of allowing the computer and display to operate on independent time systems. The refresh memory may store information in real display time; such memories use delay lines, drums or disks and may have from 8,000 to 50,000 cell spaces. Alternatively, the refresh memory may use core storage, with words demanded sequentially by the display when it is ready to accept new commands.

CHARACTER AND LINE GENERATION TECHNIQUES

The techniques used to generate characters fall into three general classes:

1. Beam Shaping. In the CRT, the object plane (cathode, or stencil) provides electron sources shaped as characters, which are selectable for focusing onto the screen of the tube.
2. Fixed Format. The deflection of the CRT beam (which is added to the major deflection) follows the same pattern for all characters. The required character is selected by appropriate unblanking of the beam. There are two important sub-classes:
   a. Raster scan of a single symbol area.
   b. Fixed pattern (all component lines of all required characters).
3. Cursive or Stroke Writing. An approximation to a written character is obtained by steering the beam by X and Y waveforms. The beam is blanked and unblanked, as required.

Figure 5 shows typical dwell times for each of the basic techniques. For a specific brightness of a written line, the "spot" current density is inversely proportional to the dwell time. The shaped beam has the advantage of simultaneously energizing a much larger area than that of an elemental spot. However, with a shaped-beam the beam current density is limited by the difficulties of focusing a complex bundle of rays, and is considerably less than the limit imposed by space charge forces at the screen.

Fixed format scanning is very inefficient; the example used in Fig. 5 is a 16 line per character raster. In terms of the unblanking duty cycle a complex line structure with all lines drawn in ideal positions is worse than a raster. However, some simple structures which would produce crude characters, may approach the duty cycle efficiency of the raster.

The fixed raster character generator requires two control channels (synchronizing and video). When a raster is used the horizontal scan is provided by the

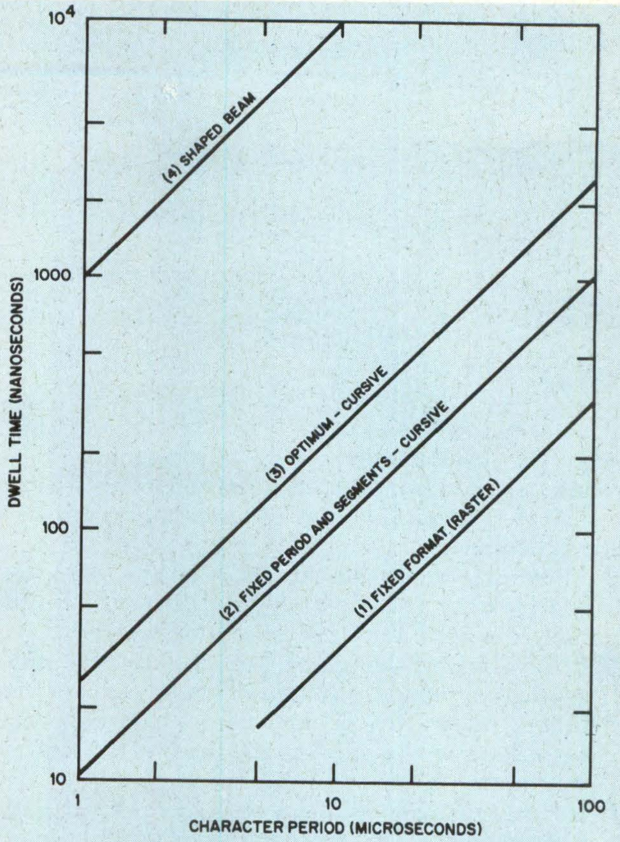

Fig. 5 Dwell time of CRT beam as a function of method of generating characters and character period.

Spot Size: 12.5 mils
(1) Monoscope—16 lines per character width 20 percent overscan
(2) Cursive—16 segments constant period per segment
(3) Cursive—Variable number of segments variable period per segment
(4) Shaped Beam

major deflection system and the vertical scan by an auxiliary deflection system. One subtle advantage of the fixed format generator is that it can write with constant speed.

In low data density systems the resolution/brightness requirements are easily met by standard CRT's with raster scan of the symbols. The monoscope is one successful method which is used to scan a selected character with high quality and low cost.

Cursively written characters may have excellent unblank duty cycles if the number of segments varies with the character complexity. The peak beam current may be minimized by eliminating variations in writing speed by making the segment period proportional to the length of the segment. In practical terms, the present state of the art tends to favor cursively written characters for high data density displays; about the same line writing speed is chosen for vectors and characters.

A cursively written character requires three contol channels (X, Y, and unblank); consequently the character generator is fairly complex. High speed characters require a wide bandwidth, and this is often obtained by using an auxiliary deflection system.

Line generation has most frequently been relatively crude. Start and end points are joined by straight lines generated by X and Y deflection ramps of appropriate slopes. In terms of display resolution/brightness capa-

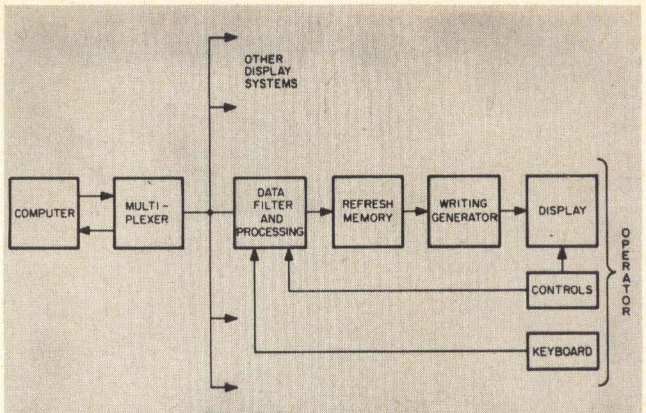

Fig. 6 Display system.

bility, the reasons for writing at a constant speed are equally applicable to separate lines as to lines within a character. Typical causes of speed variations by a line generator are:

1. Allowance is not made for the resultant line length generated by the ΔX and ΔY deflections; this results in a $\sqrt{2}$:1 variation in writing speed.
2. If the slopes of the X and Y ramps are determined by digital signals, an approximate normalization process by shifting is often used which only takes cognizance of the most significant bit; this may result in a 2:1 error in writing speed.
3. If lines must start and end at fixed clock times, the multiple of discrete periods within which a line is written will introduce writing speed errors.

The limitation of having to construct all figures from straight lines imposes a heavy load on a generator when curves have to be drawn. There will be idle periods if the time for writing a segment is less than the set-up time for the next small segment. For aesthetic reasons of writing precision and for display efficiency, it can be expected that in the future more line generators will include arc drawing capability and there will be constant-writing-speed generators which will eliminate the need for intensity correction.

GENERAL REVIEW

Figure 6 shows the essential parts of the display interface in block schematic form.

The screen and controls are the immediate interface with the operator and some improvements over current practices are possible. In particular, it is feasible to have linear resolution of better than 2^{11} elements and brightness levels in excess of 50 foot lamberts with a data load in excess of that given in Table 3. With increased data loads it becomes important to ease the task of the operator. Special attention must be paid to legibility of characters, and it would seem to be worthwhile developing a new unambiguous repertoire of alpha-numerics for international standardization. Good contrast and distinctive levels of brightness are also important factors. The use of a few well chosen colors may help the operator to quickly recognize classes of information and minimize the loss of information by over-writing.

It would appear that zooming coupled with data filtering can do much to alleviate the load on the display and the operator. The zoom control can most economically select the data which is transferred from the computer to the display refresh memory. The most successful devices for selecting the address center, around which the field is to be expanded, have been the track-ball and light pen.

The speed and dissipation of the deflection amplifiers tend to be critical in advancing the loading capability of displays. Much effort has already been applied to this problem and ingenious circuits have been developed. To minimize acceleration voltage and deflection amplifier size it is important that the beam should have a high duty cycle and that the writing speed should be substantially constant.

Character generators having variable periods should be used to minimize time lost with the beam blanked. Sophisticated line generators which will provide continuous steering of the beam, or arcs as well as straight lines will improve the appearance of graphics and reduce time losses.

Random positioning is generally more efficient than a sequentially scanned raster for presenting the output data of a computer. However, random positioning is wasteful in terms of average screen distances separating consecutive groups of data. A considerable reduction in positioning time may be obtained by sorting the output addresses from the computer to minimize distances between data groups.

A refresh memory dedicated to a display reduces the speed and capacity of the interface with the computer. It also reduces loading of the data filter and allows the operator to write information on his display without access to the computer.

Cathode ray tubes are likely to use higher acceleration voltages, and post-deflection acceleration, to achieve improved brightness and resolution; a recent survey of radiation hazards indicates that display designers have tended to be over cautious in limiting high voltages to CRT's.[9] Shorter tubes and almost flat screens are in demand and will create the need for improved linearity correction and dynamic focusing with astigmatic correction.

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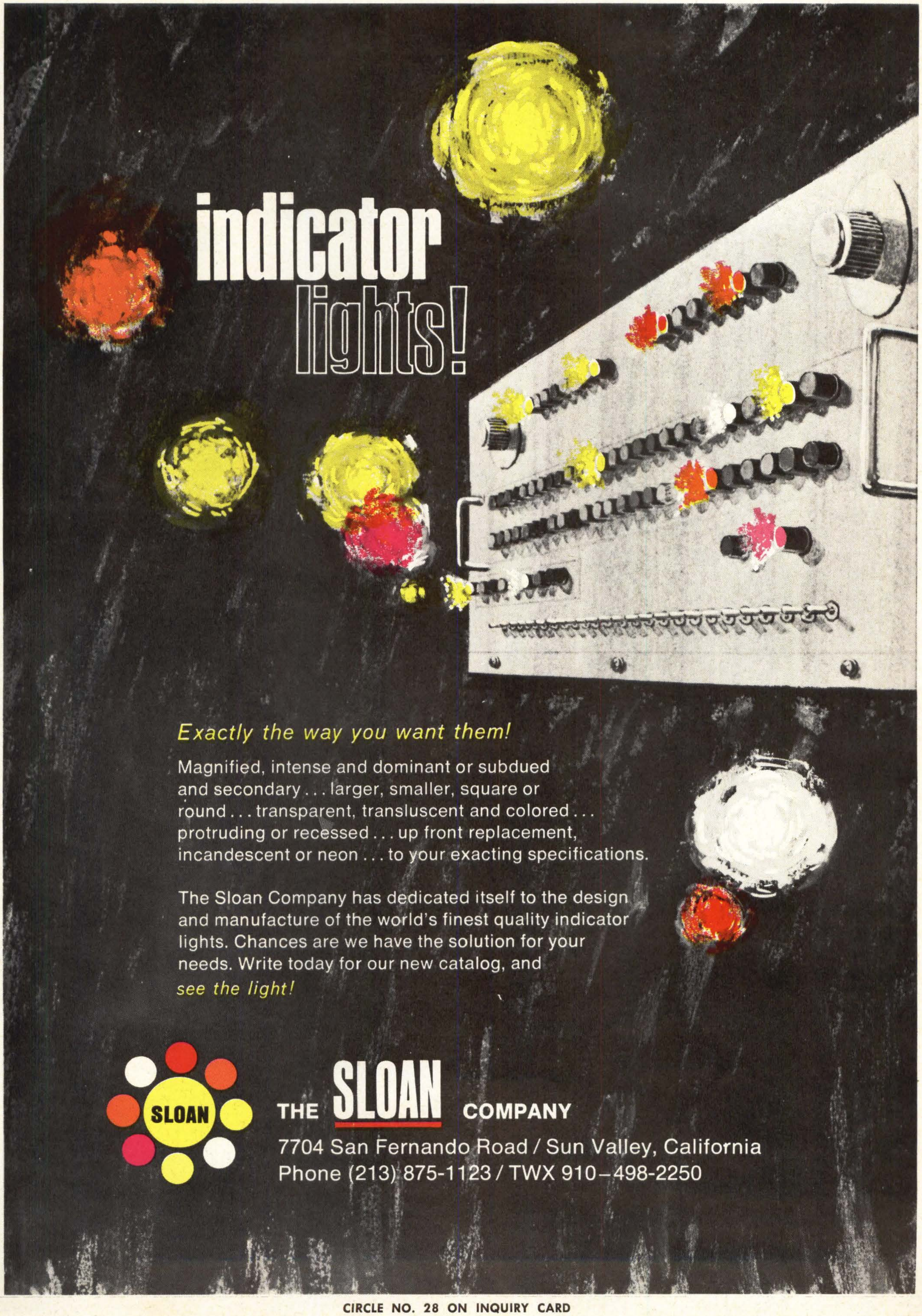
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A powerful, but simple step-by-step procedure is described that reduces the complexity of the sequential network design process by essentially reducing the number of Boolean variables. This algorithm provides the most direct route to a solution and is developed for use with the RS, JK, T and D flip-flops.

AN ALGORITHM FOR THE SYNTHESIS OF COMPLEX SEQUENTIAL NETWORKS

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The problem of designing complex sequential logic networks is typically solved by classical techniques involving the use of state diagrams, truth tables and Karnaugh maps.[1,2,3] The designer generally finds these techniques difficult and tedious to apply when the number of variables is greater than five. Unfortunately, only "classroom" problems involve less than five variables. Design problems often require four or five "frequent" variables to code state assignments and any number of additional "infrequent variables" to control sequence direction at state diagram nodes. Computer-aided design programs aimed at performing this task have found little usage because they are not widely available, not written in a universal language, and in many cases do not find acceptance to the solution of particular problems.

The algorithm presented here is a simple step by step procedure which reduces the complication of the sequential network design process by making full utilization of the designer's understanding of the problem, and allowing primary consideration to frequent variables. At the same time it takes advantage of the designer's specific choice of memory element (i.e., JK F/F, RS F/F, etc.) and its related excitation requirements to reduce the number of steps needed to develop the final input equations.

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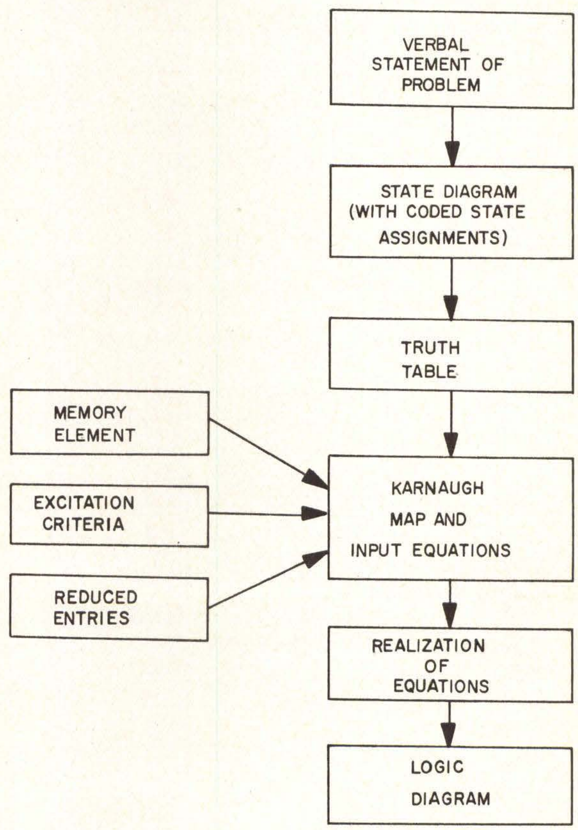


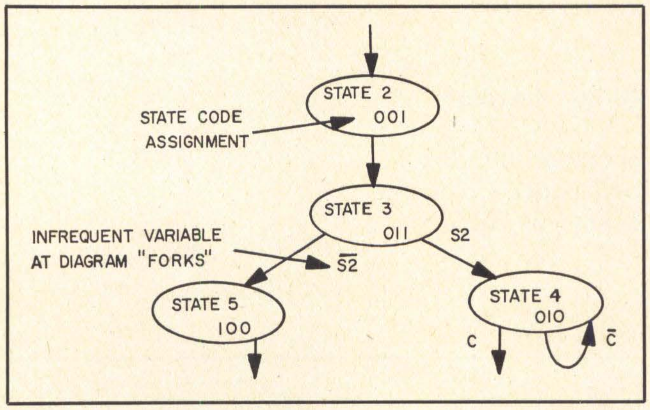
Fig. 1 Sequential circuit synthesis algorithm

SEQUENTIAL CIRCUIT SYNTHESIS ALGORITHM

The sequential circuit design process presented in Fig. 1 is in many ways representative of the classical approach.

The primary differences are in the details of the development of the Karnaugh maps and the derivation of the flip-flop input equations from the maps. This sequential network synthesis algorithm utilizes the following steps:

1. Translate the verbal problem into a reduced state diagram. Code assignments are added to each state on the diagram and infrequently used variables which do not relate to all states are assigned to establish control at each fork of the diagram. Typically, a portion of the diagram may appear as follows:



2. Develop a truth table depicting the state diagram and showing "present state", "next state", and "infrequent variables". A "remarks" column may be added to further document and clarify entries as shown here:

PRESENT STATE	INFREQUENT VARIABLE	NEXT STATE	REMARKS
001	—	011	State 2 ⟶ State 3
011	S2	010	State 3 ⟶ State 4
011	$\overline{S2}$	100	State 3 ⟶ State 5

3. Develop the Karnaugh maps by combining (ANDING) the excitation requirements of the particular memory element chosen with any infrequently used variables to formulate either reduced Boolean expression, or "1", or "0" entries. The memory element input equations are derived from the map by the following additional rules:

a. Mentally set all infrequent variables to 0's and write combinational expressions for all 1's; then mentally set all 1's to "don't care's" and write expressions for the infrequent variables.

b. One infrequent variable entry cannot be combined with another unless it is known that the one being used as a don't care is a 1 at all times when the one being circled is a 1.

4. Realize the input equations by choosing specific gate elements (i.e., 3 input AND, 2 input OR etc.) and using the memory elements chosen in step 3. The equations derived in step 3 apply for a specific memory element type and may be directly realized. Most design processes first lead to generalized equations which are then converted to specific equations. In practice the "generalized" equation form is of little use and only adds steps to the design process.

EXCITATION CRITERIA

In order to properly make entries into the Karnaugh map the designer must first take into account the representation of the truth table and transform it into entries which are in accordance with present state to next state input requirements of the particular memory element selected. For example, if we are working with JK flip-flops and wish to cause the element to go from a 1 to a 0 state we must have a 1 on the K input and we don't care whether there is a 1 or a 0 on the J input when the next clock pulse occurs. By this type of reasoning the excitation criteria shown in Table I can easily be derived and memorized. As another example, if we are working with RS flip-flops and deriving the set input Karnaugh map entry for a transition of 1⟶1 (remain set), we derive an X (do not care) from Table I.

Table I Flip-Flop Excitation Criteria

F/F STATE TRANSITION	JK FLIP FLOP		RS FLIP FLOP		D FLIP FLOP	T FLIP FLOP
PRESENT NEXT	J INPUT	K INPUT	R INPUT	S INPUT	D INPUT	T INPUT
0 ⟶ 0	0	X	X	0	0	0
0 ⟶ 1	1	X	0	1	1	1
1 ⟶ 0	X	1	1	0	0	1
1 ⟶ 1	X	0	0	X	1	0

INFREQUENT VARIABLES

Consider the state diagram shown in Fig. 2. The sequential network may progress from state 1 to either state 2 or state 3 depending on the 1 or 0 condition of a control line labled S1. Similarly, state 4 may proceed to either state 2 or state 1 as a function of control S2. In this example S1 and S2 are not of importance at any other times and thus may be considered as infrequent variables. Any variable which is not required for the definition of every state may be considered as an infrequent variable. The truth table for this example generated by step 2 of the algorithm is shown in Fig. 3. Flip-flops F1 and F2 have been assigned to define the four possible states represented by the state diagram.

The next step is to combine the excitation criteria derived from Table I with infrequent variables and place the results on the Karnaugh map. For example, consider the first two lines of the truth table of Fig. 3, and assume the JK flip-flop is the chosen memory element.

Present State F2	Present State F1	Infrequent Variables	Next State F2	Next State F1	Remarks
0	0	S1	0	1	State 1 ⟶ State 2
0	0	$\overline{S1}$	1	0	State 1 ⟶ State 3

The J input excitation for F1 from the first line is a 1 and for the second line is a 0. Step 3 of the algorithm requires these excitation entries to be $\overline{S1}$ to form the F1 F2 Karnaugh map entry: $1 \cdot S1 + 0 \cdot \overline{S1}$. "anded" with the related infrequent variables S1 and This example is easily reduced by the rules of Boolean algebra:

$$1 \cdot S1 + 0 \cdot \overline{S1} = 1 \cdot S1 = S1$$

However, if all of the possible combinations of excitation criteria (1, 0, X) and the variable (S) are taken, only five of them can be directly reduced by Boolean rules as shown below:

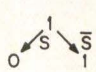
$$\left.\begin{array}{l} 1.\ S \cdot 0 + \bar{S} \cdot 0 = 0 \\ 2.\ S \cdot 0 + \bar{S} \cdot 1 = \bar{S} \\ 3.\ S \cdot 1 + \bar{S} \cdot 0 = S \\ 4.\ S \cdot 1 + \bar{S} \cdot 1 = 1 \\ 5.\ S \cdot X + \bar{S} \cdot X = X \end{array}\right\} \text{Reduced by rules of Boolean algebra}$$

$$\begin{array}{l} 6.\ S \cdot 1 + \bar{S} \cdot X \\ 7.\ S \cdot X + \bar{S} \cdot 1 \\ 8.\ S \cdot 0 + \bar{S} \cdot X \\ 9.\ S \cdot X + \bar{S} \cdot 0 \end{array}$$

In examining the last four expressions it is immediately known that these forms could only occur with JK and RS flip-flops because T and D flip-flops do not produce "don't care", (X), excitation criteria. Furthermore, if these four forms are examined with respect to the JK flip-flop it is determined that they do not apply. For example consider the form, $S \cdot 1 + \bar{S} \cdot X$: If the J input is being derived, then the $S \cdot 1$ term implies a $0 \rightarrow 1$ transition. However, there is no possible transition from 0 that could at the same time produce a (X) don't care, excitation criteria to be anded with $\bar{S}$ (see Table I). Similar reasoning applies to the K input. If these forms are analyzed with respect to the RS flip-flop it is found that only the last two apply:

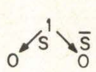
8. $S \bullet 0 + \bar{S} \bullet X$

(Applies for R or S input)



9. $S \bullet X + \bar{S} \bullet 0$

(Applies for R or S input)



By examining the state diagram conditions which would imply these forms it is shown that the correct excitation input for these two expressions is a 0. Thus the proper Karnaugh map entry reduced form is 0.

The result of this analysis is a simple table, Table II, which depicts all of the possible forms which can occur with T, D, RS and JK flip-flops. These expressions and their reduced forms apply to both inputs of the RS and JK flip-flop.

Thus far the analysis has considered only two-way branches. Although this case predominately occurs it is certainly not the only possibility. In examining other cases more entries will be generated for Table II and it would be desirable to derive some simple rules for reducing these expressions independent of memory element type and number of directions of branching so that Table II would not be required.

Consider a case of two control variables. The situation presented below appears when the variable (S)

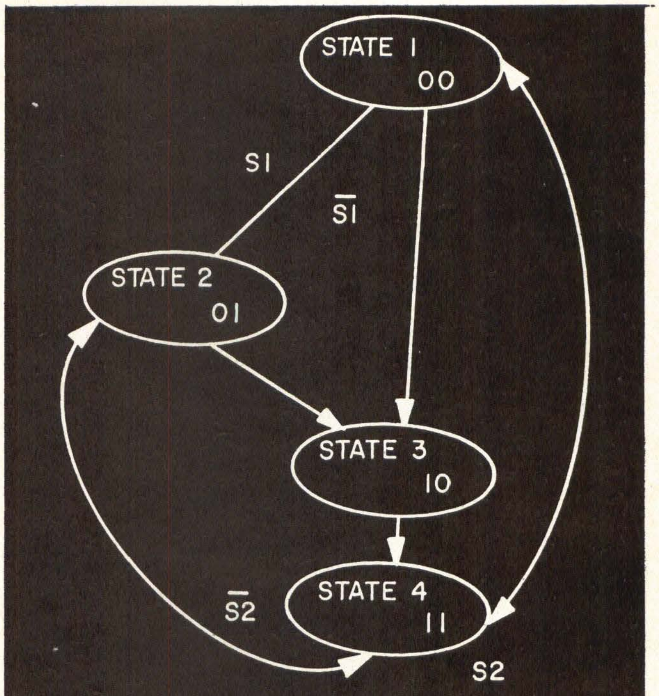


Fig. 2 Simple state diagram; 4 variables

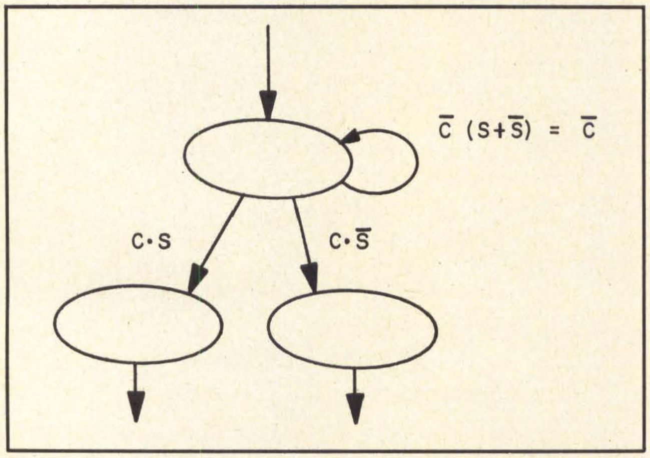
Binary Count	Present State F2	Present State F1	Infrequent Variables	Next State F2	Next State F1	Remarks
0	0	0	S1	0	1	State 1 → State 2
0	0	0	$\overline{S1}$	1	0	State 1 → State 3
1	0	1		1	0	State 2 → State 3
2	1	0		1	1	State 3 → State 4
3	1	1	S2	0	0	State 4 → State 1
3	1	1	$\overline{S2}$	0	1	State 4 → State 2

Fig. 3 Truth table for Fig. 2 state diagram

Table II Possible Karnaugh Map Entries Involving Infrequent Variables

Excitation Criteria Combined with Infrequent Variable	Reduced Form (Karnaugh Map Entry)
1. $S \cdot 1 + \bar{S} \cdot 0$	S
2. $S \cdot 0 + \bar{S} \cdot 1$	$\bar{S}$
3. $S \cdot 0 + \bar{S} \cdot 0$	0
4. $S \cdot 1 + \bar{S} \cdot 1$	1
5. $S \cdot X + \bar{S} \cdot X$	X (don't care)
6. $S \cdot 0 + \bar{S} \cdot X$	0 } occur only with RS F/F
7. $S \cdot X + \bar{S} \cdot 0$	0 } occur only with RS F/F

controls the direction of transfer and the variable (C) determines if the circuit should maintain its present state or proceed when consecutive clock pulses occur.



If all the possible expressions for this case are examined in the same manner as above; the only ones which apply are shown below:

Expression	Reduced Form	Remark
$X\cdot C\cdot S + X\cdot C\cdot\overline{S} + X\cdot C \longrightarrow$	X	JK and RS F/F
$O\cdot C\cdot S + O\cdot C\cdot\overline{S} + X\cdot C \longrightarrow$	0	RS F/F only
$O\cdot C\cdot S + X\cdot C\cdot\overline{S} + X\cdot C \longrightarrow$	0	RS F/F only

These resultant expressions have a form similar to the last three entries of Table II. By examining these forms and considering the results derived from other multiple control variable examples, two general rules may be derived:

RULE 1:

When the Boolean expression consists of minterms, all of which combine a variable with a don't care excitation criteria, the reduced form Karnaugh map entry is a "X" (don't care).

Example:

$A\cdot X + B\cdot X + C\cdot D\cdot X + J\cdot X \longrightarrow X$

RULE 2:

When the Boolean expression consists of minterms which are a combination of X (don't care) and a variable summed with minterms which are a combination of 1 or 0 and a variable; then ignore the minterms containing don't care conditions and reduce the remaining portions of the expression by Boolean rules.

Example:

$$\overset{\text{ignore}}{\cancel{A\cdot X}} + \overset{B}{\cancel{B\cdot 1}} + \overset{0}{\cancel{C\cdot 0}} + \overset{\text{ignore}}{\cancel{D\cdot E\cdot X}} \longrightarrow B$$

$$\overset{0}{\cancel{S\cdot 0}} + \overset{\text{ignore}}{\cancel{\bar{S}\cdot X}} \longrightarrow 0$$

Rule 1 is useful for JK and RS flip-flops. Rule 2 is useful only for RS flip-flops because the expression forms that it applies to are generated only when working with this type of flip-flop. These two rules in conjunction with normal Boolean rules can be used to reduce all Karnaugh map entries regardless of memory element type or number of variables involved.

KARNAUGH MAP CONSIDERATIONS

If the truth table state assignments are arranged in an increasing binary count order as shown in Fig. 3 and the Karnaugh map is arranged in the same manner as shown below (Fig. 4), then entries can be made more easily in a sequential fashion. The Karnaugh map representations for the truth table discussed above (Fig. 2, 3) are shown in Fig. 5.

From step 3 of the algorithm the 1's are first circled, then treated as don't cares while infrequent variables are circled. The resulting equations (Fig. 5) shown below each memory element input map may be applied to step 4 of the algorithm to produce the final mechanized logic diagram.

SAMPLE DESIGN PROBLEMS

The sample problem 1 represented by the state diagram in Fig. 6 requires a 3 variable Karnaugh

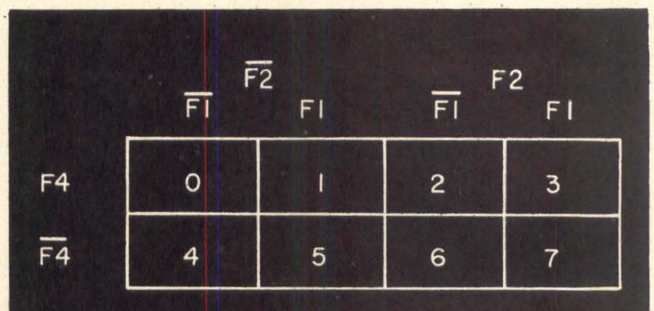


Fig. 4 3-variable Karnaugh map arranged in increasing binary count order.

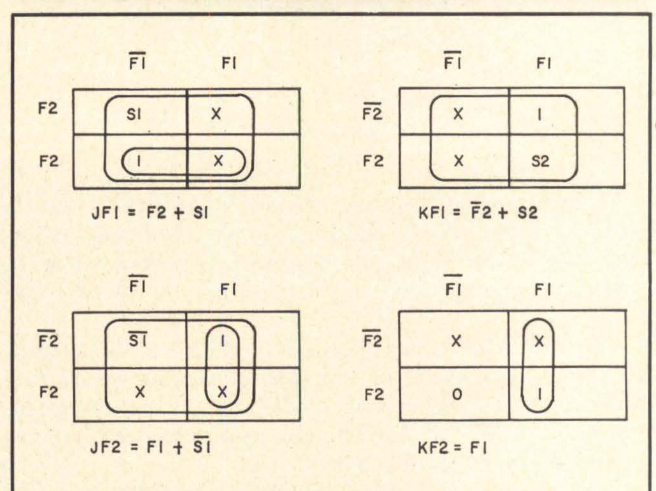


Fig. 5 Karnaugh maps for Fig. 3 truth table

map even though six variables (F1, F2, F4, S1, S2, S3) are involved in the definition of the problem. This typical situation would normally require a 6 variable map even though the designer's feeling for the complexity of the problem is more closely aligned with the three variables F1, F2, F4.

Figure 7 presents the truth table representation of the problem. JK flip-flops are chosen to implement the design and from Tables I and II the excitation criteria is combined with infrequent variables where applicable and the reduced form is entered on the Karnaugh map (Fig. 8). In learning this process it may be easier for the designer to first

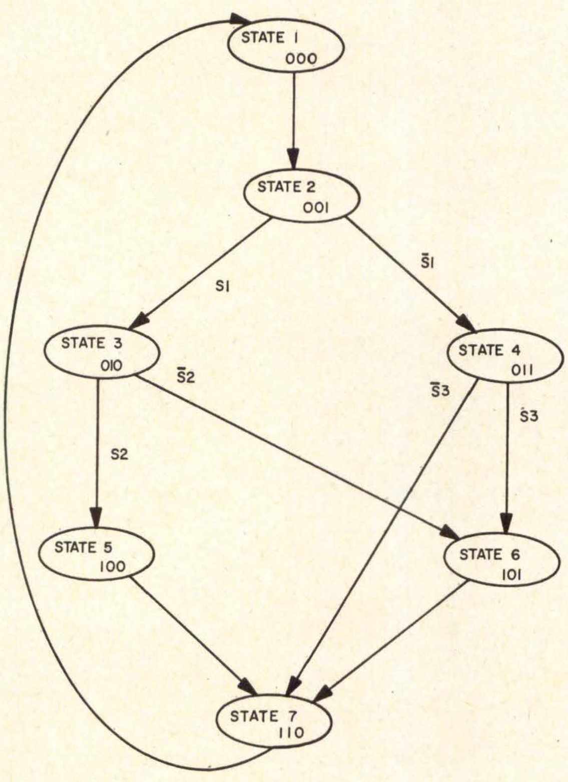


Fig. 6 Sample problem 1 state diagram

PRESENT STATE				INFREQUENT VARIABLE	NEXT STATE		
Count	F4	F2	F1		F4	F2	F1
0	0	0	0		0	0	1
1	0	0	1	S1	0	1	0
1	0	0	1	$\overline{S1}$	0	1	1
2	0	1	0	S2	1	0	0
2	0	1	0	$\overline{S2}$	1	0	1
3	0	1	1	S3	1	0	1
3	0	1	1	$\overline{S3}$	1	1	0
4	1	0	0		1	1	0
5	1	0	1		1	1	0
6	1	1	0		0	0	0
7	1	1	1	Don't Care	X	X	X

Fig. 7 Sample problem 1 truth table

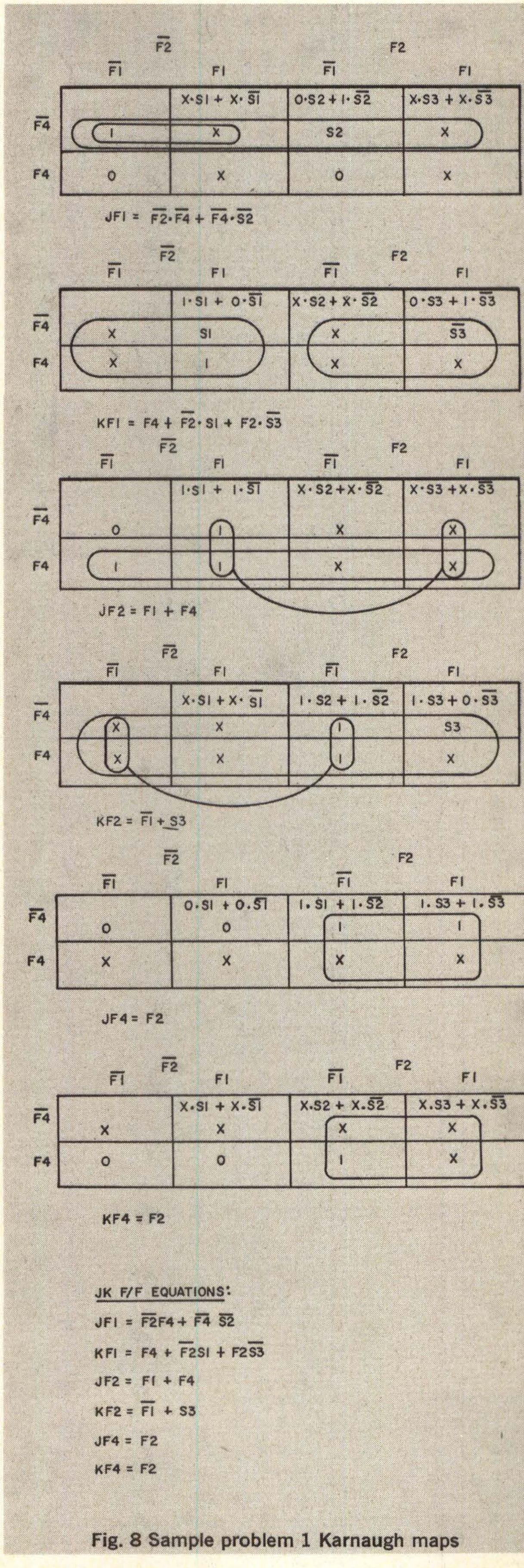


Fig. 8 Sample problem 1 Karnaugh maps

enter the unreduced form as shown in Fig. 8 and then consult Table II for the reduced form if it is not immediately obvious.

The state diagram for sample problem 2 is shown in Fig. 9. This example introduces an additional capability of being able to remain at a particular state for consecutive clock times until a complete signal appears. For example, the network for problem 2, Fig. 9, will remain at state 2 until a sign C2 appears, at which time it will proceed to state 5 if S2 or state 4 if $\overline{S2}$. States 4 and 5 would occur for only one clock time and would advance to state 1 in an unrestricted manner. When two variables, a complete

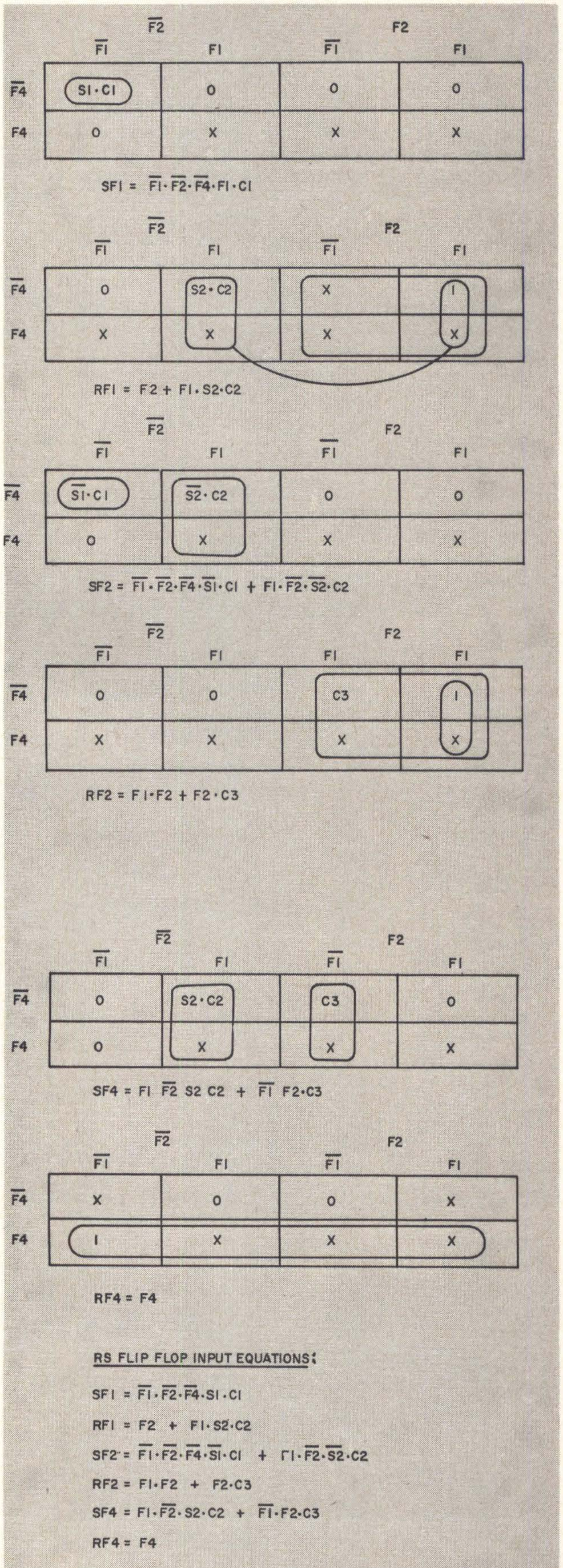


Fig. 11 Sample problem 2 Karnaugh maps

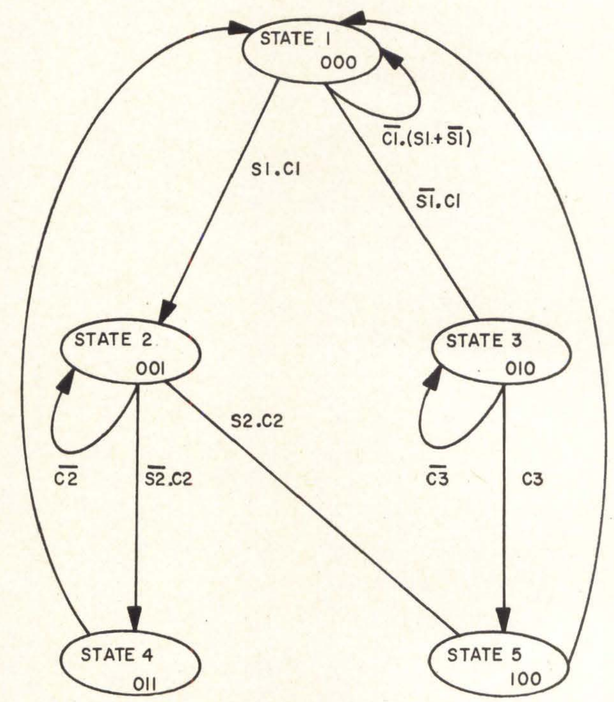


Fig. 9 Sample problem 2 state diagram

	Present			Remark	Next		
	F4	F2	F1		F4	F2	F1
	0	0	0	$\overline{C1}$	0	0	0
0	0	0	0	S1•C1	0	0	1
	0	0	0	$\overline{S1}$•C1	0	1	0
	0	0	1	$\overline{C2}$	0	0	1
1	0	0	1	S2•C2	1	0	0
	0	0	1	$\overline{S2}$•C2	0	1	1
2	0	1	0	$\overline{C3}$	0	1	0
	0	1	0	C3	1	0	0
3	0	1	1	——	0	0	0
4	1	0	0	——	0	0	0
5	1	0	1	Don't Care	X	X	X
6	1	1	0	Don't Care	X	X	X
7	1	1	1	Don't Care	X	X	X

Fig. 10 Sample problem 2 truth table

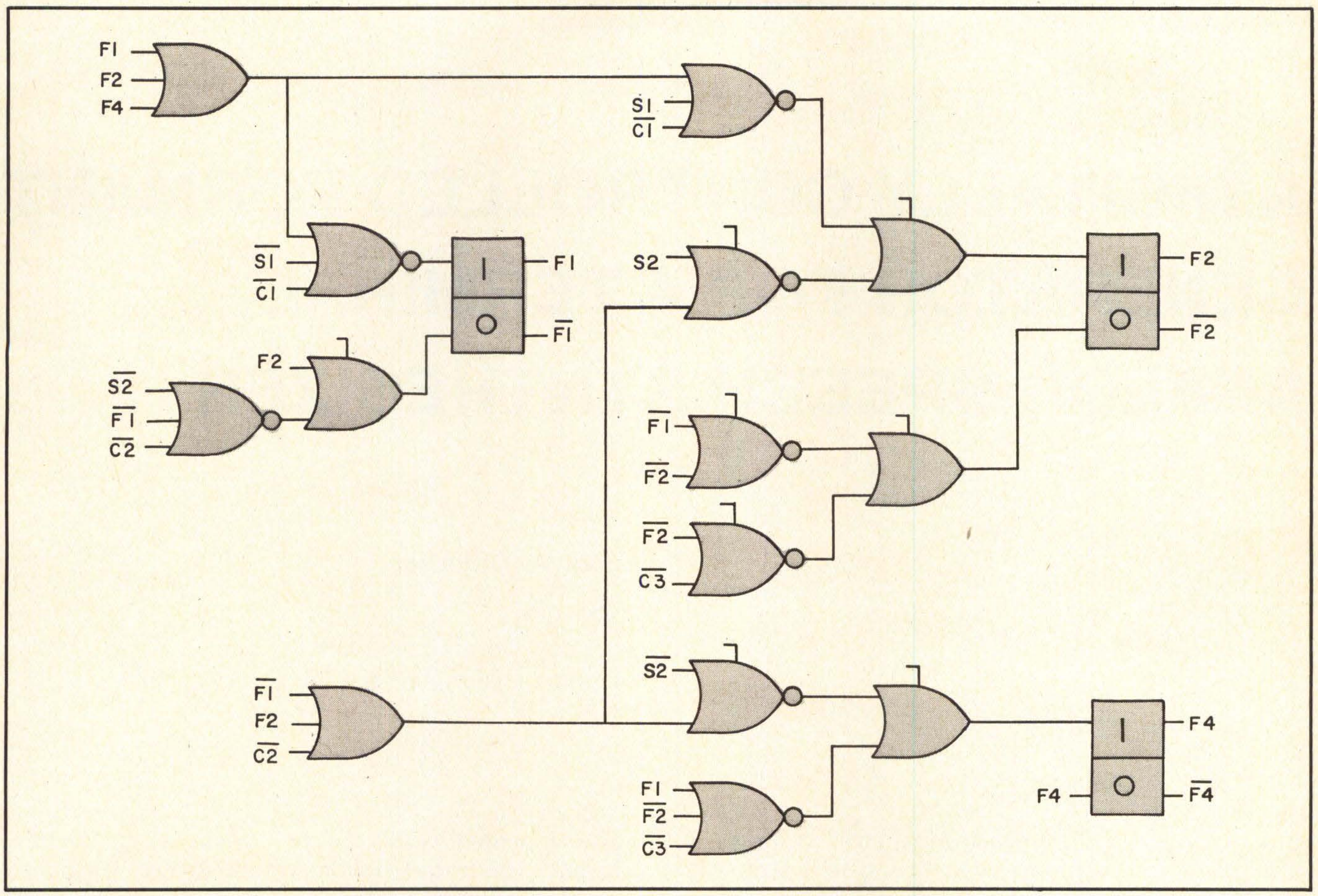


Fig. 12 Logic diagram for Fig. 11 state diagram

(C) signal as well as a steering signal (S), appear at the fork of a state diagram four directions are implied.

Two of the directions ($\overline{C \cdot S}$ and $\overline{C} \cdot S$) cause the network to maintain the present state. Thus, actually this condition can be reduced to three directions, $S \cdot \overline{C}$, $\overline{S} \cdot C$, $\overline{C}$. The solution is performed in exactly the same manner as presented above. The truth table for this example is shown in Fig. 10. Note that three entries are made for state's 1 and 2 as explained above.

This problem, if treated in the classical manner, would require an eight variable Karnaugh map (F1, F2, F4, C1, C2, C3, S1, S2). By utilizing this technique it is treated in terms of only three frequent variables. The Karnaugh maps shown in Fig. 11 assume the use of RS flip-flops. Step 4 has been completed in Fig. 12 to show the desired logic configuration. This diagram assumes a particular choice of logic gate elements.

CONCLUSION

The solutions posed by these examples are not necessarily optimal because optimal state assignment techniques[4,5] were not applied during the construction of the state diagram. This is treated as a separate problem. Similarly, the choice of memory elements can have an effect on optimization of the final result. This is less of a problem because the JK flip-flop is by far the most popular offering by integrated circuit manufacturers and is usually chosen because of its universality.

Aside from these two considerations the method presented here will always yield an optimal solution and in so doing it will significantly reduce the complexity of this process. It has immediate applicability to the logic design of complex sequential networks and may be a desirable inclusion for a computer aided design program.

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A formant generator for a terminal anaylog speech synthesizer has been designed which accomplishes direct digital control, bypassing the inherent disadvantages of maintaining the accuracy of analog control voltages.

A DIGITALLY CONTROLLED FORMANT GENERATOR FOR A TERMINAL ANALOG SPEECH SYNTHESIZER

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There are presently two major types of synthesizers being used for computer-controlled speech synthesis. The first, and most basic, is a synthesizer which models the human vocal tract. This type of synthesizer achieves intelligible sounds by electronic simulation of the physiological operations which occur in human speech. The second category of speech synthesizer is the terminal analog synthesizer which simulates the sounds of human speech, but not the vocal mechanisms which produce them. This article describes a key component of the latter type of synthesizer—the formant generator.

The IBM Laboratory at Research Triangle Park, N. C., has built and used such formant generators, continuing development work begun at the IBM Research Laboratory in San Jose, California, several years ago. The operation of the formant generators is crucial in any speech synthesizer since they shape the spectrum of the voice source in order to simulate human voice sounds. Each generator creates a peak in the spectrum envelope. These peaks or formants are those bands which, collectively, determine the phonetic identity of spoken vowels. These variable formant generators simulate the first three resonances of the human vocal tract.

IBM's experimental work in speech synthesis has extended over several years. Although considerable progress has been made in the development of vocabulary, control signals, synthesizer hardware, and programming, one element of the system underwent little change—the type of control signal used to tune the formant generator. This has traditionally been accomplished by analog voltages. However, these impose limitations in accuracy and stability. As speech synthesis has been made more sophisticated and accurate, it has become more difficult for the synthesizer hardware to adequately respond to the refined control signals. We have overcome the shortcomings of analog control by using digital controls. The approach of using digital control of loop gain to establish filter tuning should also be applicable to other tunable-filter designs.

Figure 1 shows a basic block diagram of an analog speech synthesizer. The formant generators are the three filters—F1, F2 and F3—shown in the lower-right corner of the diagram. Although I will discuss primarily the formant generator, similar filters are used in the fricative and nasal filters. The nasal filter differs from the formant filters only in that it has a fixed digital address, resulting in a filter frequency of approximately 250 Hz with a bandwidth of 100 Hz. The fricative filter is composed of two formant-type filters in addition to a tunable anti-resonance created by connecting a formant filter in a feedback loop of an operational amplifier, yielding two poles

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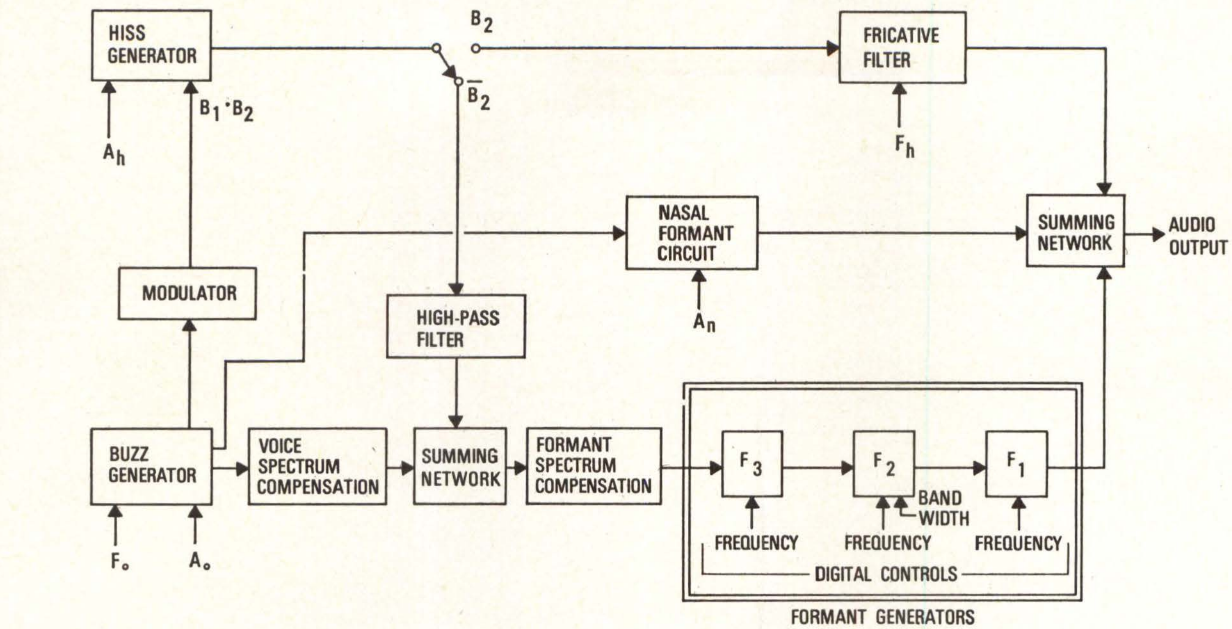

Fig. 1 Terminal analog speech synthesizer.

(maximum resonant frequency) and one zero (minimum resonant frequency).

As described by Flanagan,[1] the transfer function of a formant resonance is characterized by a pair of complex conjugate poles. It is the resonant frequency of this transfer function which must be varied under computer control, while maintaining a relatively constant bandwidth.

The original formant filters[2] were built using an LC resonance and a feedback amplifier with variable-gain characteristics. An amplifier was needed whose overall gain could be rapidly changed and accurately set between ten and one hundred. Three approaches were considered for obtaining variable gain characteristics:

- Photo-sensitve resistors
- Resistors switched by reed relays
- Pulse-width modulation

Initially, the third approach offered the best solution to the problem. Briefly, the technique was to modulate or switch an amplifier (in the filter loop) on and off at a variable- repetition rate. Gain through the amplifier (after suitable filtering) was proportioned to the duty cycle of the modulating signal. A programmable, analog-control voltage obtained from a digital-analog (D/A) converter was used to establish the duty cycle of the modulating signal.

As speech synthesis changed from an art to a science, it became evident that the speech synthesizer had limitations. Among these were lack of formant stability (with time and temperature) and a poor signal-to-noise ratio. For these reasons it was desirable to eliminate all analog control. The new formant generators consist of a digital attenuator between two amplifier-type integrators (Fig. 2).

DIGITAL ATTENUATOR

The digital attenuator circuit (Fig. 3) resembles a conventional, digital-to-analog converter (D/A) where a reference voltage is supplied to E_{in}. In general, high speed and accuracy of conversion are prime considerations when selecting a D/A converter for a particular job. A typical application might be the generation of an accurate, digitally controlled, saw-tooth-deflection voltage required for beam deflection on a cathode ray tube. However, for use in a speech synthesizer, 7-bit resolution (127 discrete-pole positions) was considered adequate.

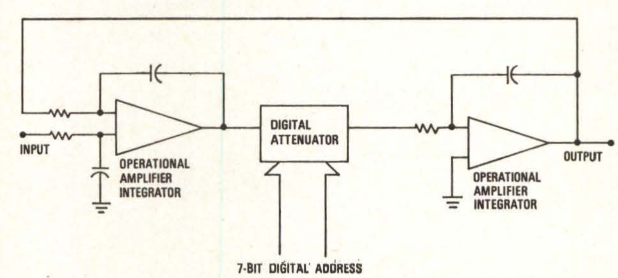

Fig. 2 Simplified diagram of formant generator.

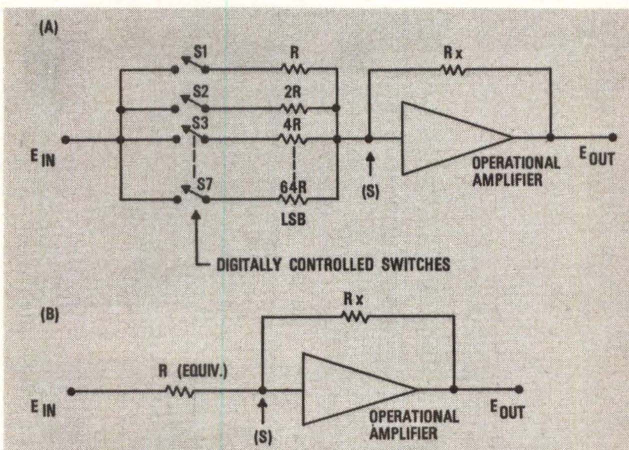

Fig. 3 Digital attenuator and equivalent circuit.

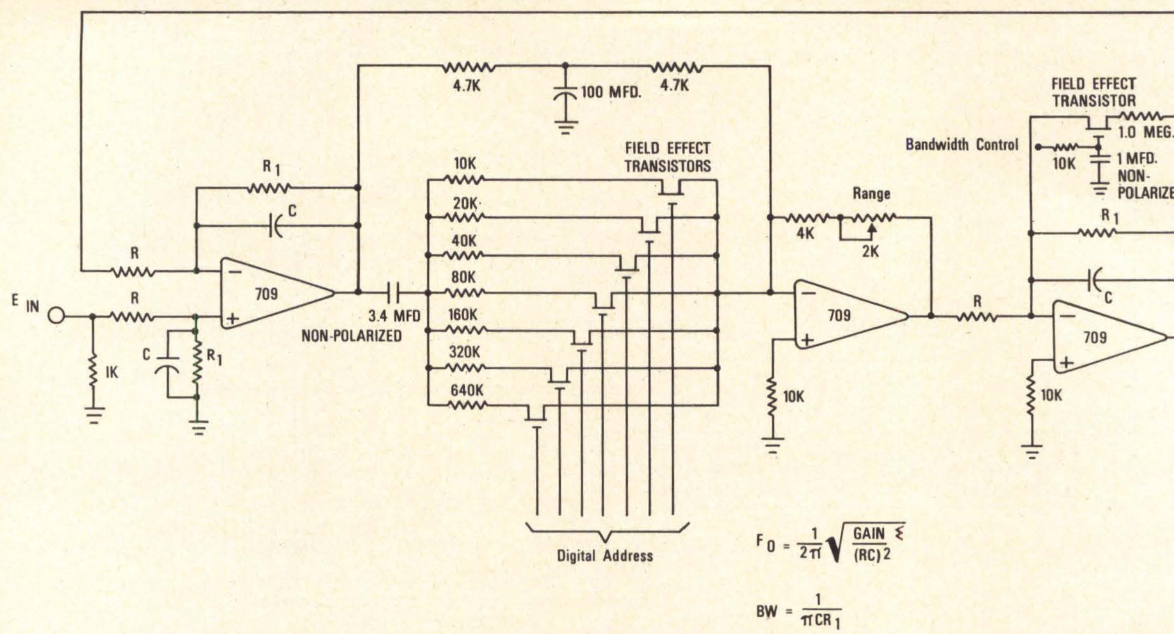

Fig. 4 Formant generator circuit.

The attenuator consists of two parts: a summing amplifier and a resistive-decoding network. The weighted-resistor network in Fig. 3A (resistor values ascending by powers of two and currents inversely proportional) was used in the formant generator. The 1%-2% accuracies which can be obtained are adequate for speech synthesis. Figure 3B is an equivalent circuit of the summing amplifier and resistive network.

The weighted resistor network consists of seven, binary-related resistors: R, 2R, 4R, 8R, 16R, 32R, 64R, with associated single-pole switches. (For this part of the discussion the switches are considered connected to a voltage reference supply.) Each current input from the reference-supply/switched-resistor combination is summed at point S.

For an equivalent resistance, R_{eq}, formed by any combination of resistors switched (in or out), attenuator gain can be calculated by:

$$A = \frac{R_x}{R_{\text{equivalent}}}$$

Field-effect transistors have some definite advantages compared to junction transistors when used in analog switching circuits:

- Better on-off ratio;
- Greater temperature stability;
- No inherent offset voltage between input and output terminals;
- No floating-drive circuit (transformer) required.

A major problem in this use of a field-effect transistor as a switch is the small amount of drive signal that is fed through to the output (because of gate-to-drain capacitance). This condition is most noticeable when switching low-level signals at high frequency. Fortunately, in our application, the integrators used with the attenuator have a filtering effect on these noise spikes.

Drain-to-source resistance (r_{ds}) when the field-effect transistor is turned on is an important characteristic in an analog-switching application. For our attenuator we chose to use a P-channel type of insulated-gate field effect transistor because of its availability, although the N-type is generally preferred for chopper and analog-switching applications. The particular P-type which we chose to use is normally off with zero-gate voltage, and has a drain-to-source resistance (on) of approximately 250 ohms. When in the off condition, this value increased to 10^{11} ohms.

The on resistance was the primary concern in the design of the resistive decoding/switching network, since it was this resistance (r_{ds}) which is in series with the decoding resistor. Hence the value chosen for the most significant bit (MSB) was made large (10K for the decoder vs. 250Ω for the on resistance of the field-effect transistor).

One point that was originally overlooked was the possibility of large incoming signals turning the field-effect transistor on. Thus, maximum input voltage (±) is a function of the biasing voltage. A level-conversion card was designed to convert our standard logic levels to those compatible with the field-effect transistors.

The attenuator is also used within the synthesizer (Fig. 1) to control the amplitude of the following:

A_H—digital-amplitude control of the hiss generator (white noise source) which excites either the fricative or format filters;

A_N—digital-amplitude control of the buzz generator, also referred to as the voice source. These variable-amplitude pulses shock-excite the nasal-formant filter;

A_O—digital-amplitude control of the buzz generator (used in establishing the loudness of voiced sounds).

FORMANT GENERATOR DESIGN

The digitally controlled formant generator is a hybrid computing device for solving second-order differential equations with time-varying coefficients.

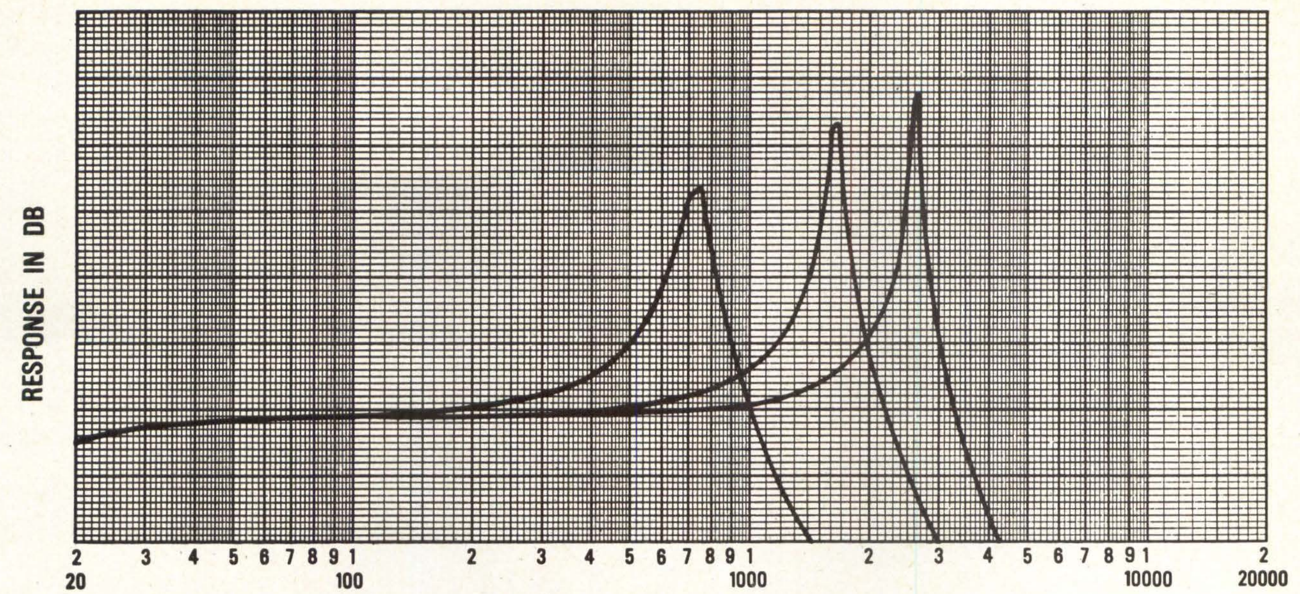

Fig. 5 Frequency response of a formant filter for three different digital addresses.

The transient response to a step-function input is an exponentially-damped output wave.

Two operational-amplifier integrators (Fig. 2) are used with the digital attenuator (between them) in a loop configuration to form the generator. Pole location (formant frequency) is controlled by regulating attenuator gain.

An equation for calculating the center frequency (pole location) is:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{\frac{\text{Digital Count}}{127}}{(RC)^2}}$$

This gives the maximum tuning frequency when all bits are turned "on" (minimum attenuation in the digital attenuator). Thus, for increasing amounts of attenuation, pole frequency decreases.

For some speech sounds, the bandwidth of the second formant had to be broadened. This was accomplished by shunting the second integrating capacitor with a fixed resistor. Here again, a field-effect transistor was used for switching. The bandwidth of the filter is program selectable.

Those of you who have worked with speech synthesizers are aware of the gremlin-type noises generated within formant filters. One type of noise often referred to as "thump", consists of step excitation of the filter which is generated whenever a small dc voltage finds its way into the filter loop. It is most noticeable during periods of "silence" when a new pole location is being obtained. This dc base-line shift is caused by an unbalance in the modulator diodes if a pulse-width modulator is used by the emitter-base potential when transistors are used for switching, or by feed-through capacitance with field-effect switches. By designing the attenuator around field-effect transistors, this source of disturbance has been reduced. The instantaneous, signal-to-noise (thump) ratio for this filter is better than 40 dB.

Typical specifications for a filter circuit shown in Fig. 4 are:

Formant range for F_2 .... 250-2,500 Hz

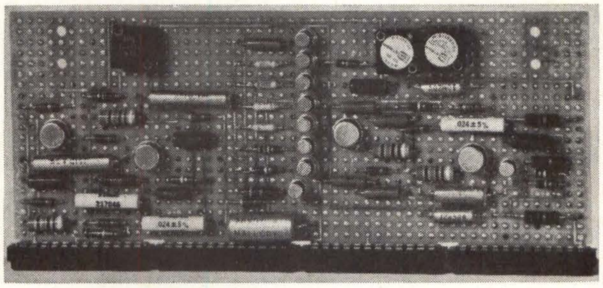

Fig. 6 Formant generator (packaged with input-signal-conditioning amplifier).

Bandwidth at 2,500 Hz .... 98 Hz

Q control at 2,500 Hz ....17 dB

Temperature drift, 10°-40°C .... Frequency & amplitude$\pm$0.5%

Power supply changes $\pm$10% ...... Less than 0.5%

Figure 5 shows a graphic plot of the frequency response of a formant filter for three digital addresses. Figure 6 is a photo of our packaged formant filter. The card contains an additional operational amplifier for input-signal conditioning and two potentiometers for input and output level setting.

ACKNOWLEDGMENT

I wish to thank Mr. H. D. Maxey of the Speech Processing Laboratory at Research Triangle Park for establishing the performance criteria of the digitally controlled formant generator, and for other valuable suggestions.

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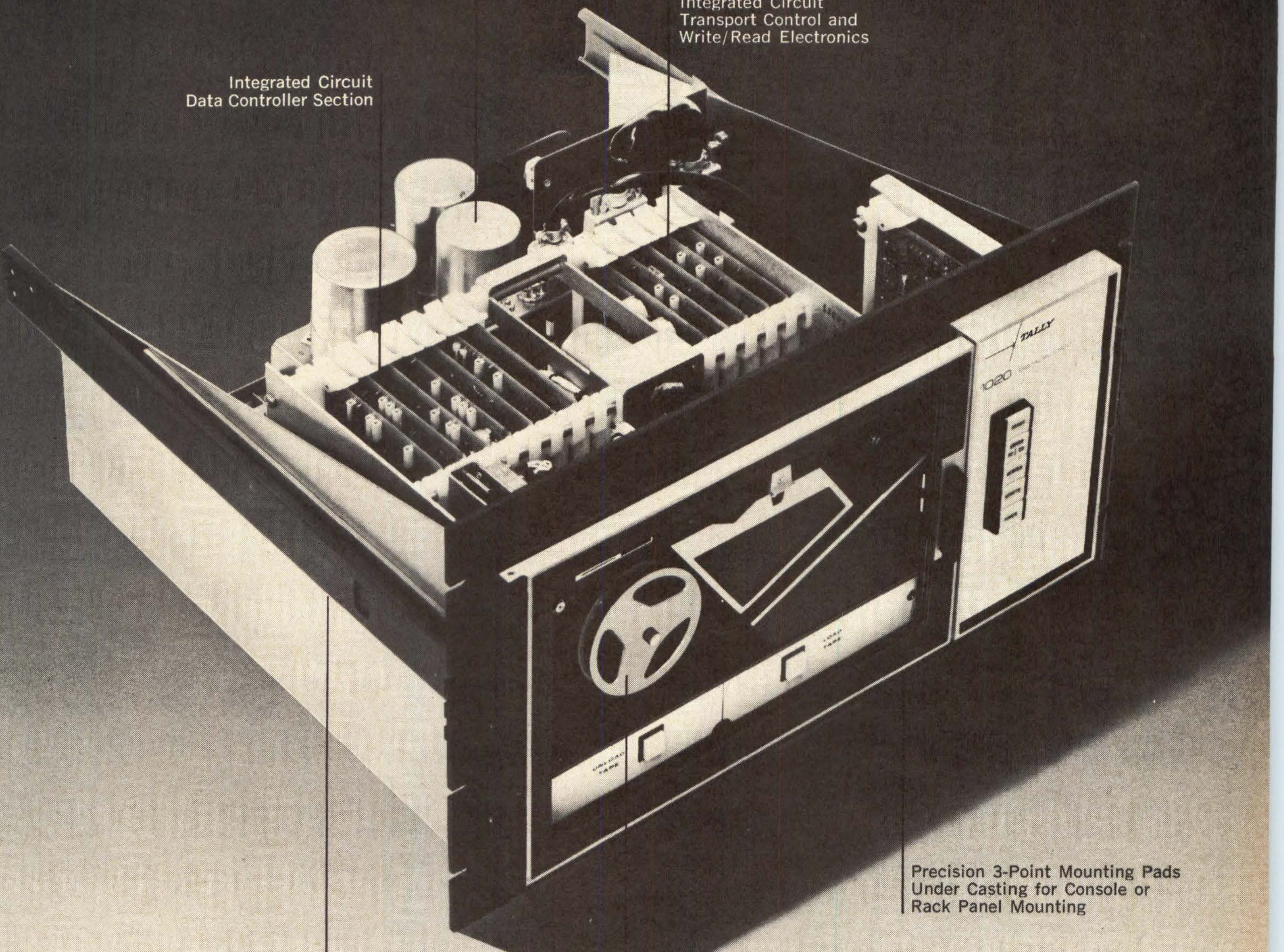

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TECHNICAL NOTE

RECENT DEVELOPMENTS IN AUTOMATED CORE TESTING

S. Zuccaro and D. H. Flaningam

E-H Research Laboratories, Inc.
Oakland, California

Present-day high-volume core handlers and measurement systems were conceived back in the days of 50-mil cores and 100-ns drive pulses. In the natural course of events cores got smaller and faster and specifications got tighter, until the industry was faced with the fact that measurement technology had fallen behind device technology. Principal evidence of this deficiency has been poor correlation between detailed scope analysis and test results from available sorting systems, and consequent poor yields. This situation has inevitably called forth a new generation of automated core-test equipment whose prime objective is to take advantage of recent advances in instrument technology to improve correlation between AQL test bench and system measurements. This article is a discussion of the design factors involved and how they have been resolved in the development of one particular family of the new generation, the E-H 8321/8350 Series.

CONCEPTS

Correlation With Scope Analysis

The primary problem in relating automated system results to the manual analysis of the AQL test bench has been the fundamental disparity of the two measurement techniques involved. Systems designers heretofore have been forced by the single-shot nature of the sense analysis problem to rely on voltage-threshold discriminators, making it necessary to "close in" on actual core output levels. The analog comparator can only affirm that a core's output is above or below a pre-set voltage level, plus or minus the grey area defined by the comparator's basic sensitivity and noise characteristics. In the typical design the uncertainty due to charge-sensitivity (i.e. the millivolt-nanosecond product) swamps out the noise error, so that we are far from achieving the ideal noise-limited measurement.

By contrast, the technique used to check system performance is some form of oscilloscope analysis, where the instrument makes a direct measurement of voltage as a function of time. The grey area of the measurement is reduced nearly to the theoretical limit, the uncertainty due to noise.

Recent developments in high-speed sample-and-hold techniques have made it possible to do away with analog discriminators in sense analysis. The systems described here are built around strobing voltmeter sense analysis, a radical departure from previous concepts. In this technique a wideband voltmeter is operated in single-shot sample-and-hold mode to make an actual voltage measurement at programmed time after sync. It was immediately obvious that this approach offered a fundamental advantage in the attempt to achieve better correlation, in that it does away with the basic disparity between system approach and AQL scope approach. Voltmeter sense analysis effectively puts an automated scope into the system itself.

The Ω Index and Multiplexing

From the outset it is obvious that the ability to multiplex handlers is a highly-desirable feature of any new system designed to make the most of advances in high-speed pulse technology. Fast-pulse machinery is expensive, and if we define an investment index

$$\Omega = \frac{\text{Yield, Cores/Sec}}{\text{Capital Equipment Expenditure}}$$

then one fundamental and overriding consideration (hence Ω, or the final argument) in developing a new system is to make the numerator YIELD keep pace with the inevitable enlargement of the denominator. That is, we want to keep Ω constant and competitive with existing systems. The first step in increasing YIELD is to improve the measurement accuracy and thereby the correlation with AQL batch-sampling; the second step is to increase throughput rates. The obvious way to increase the number of cores handled per second is to recognize that handlers handle for about 60 to 80% of the time, and test for 20 to 40%.

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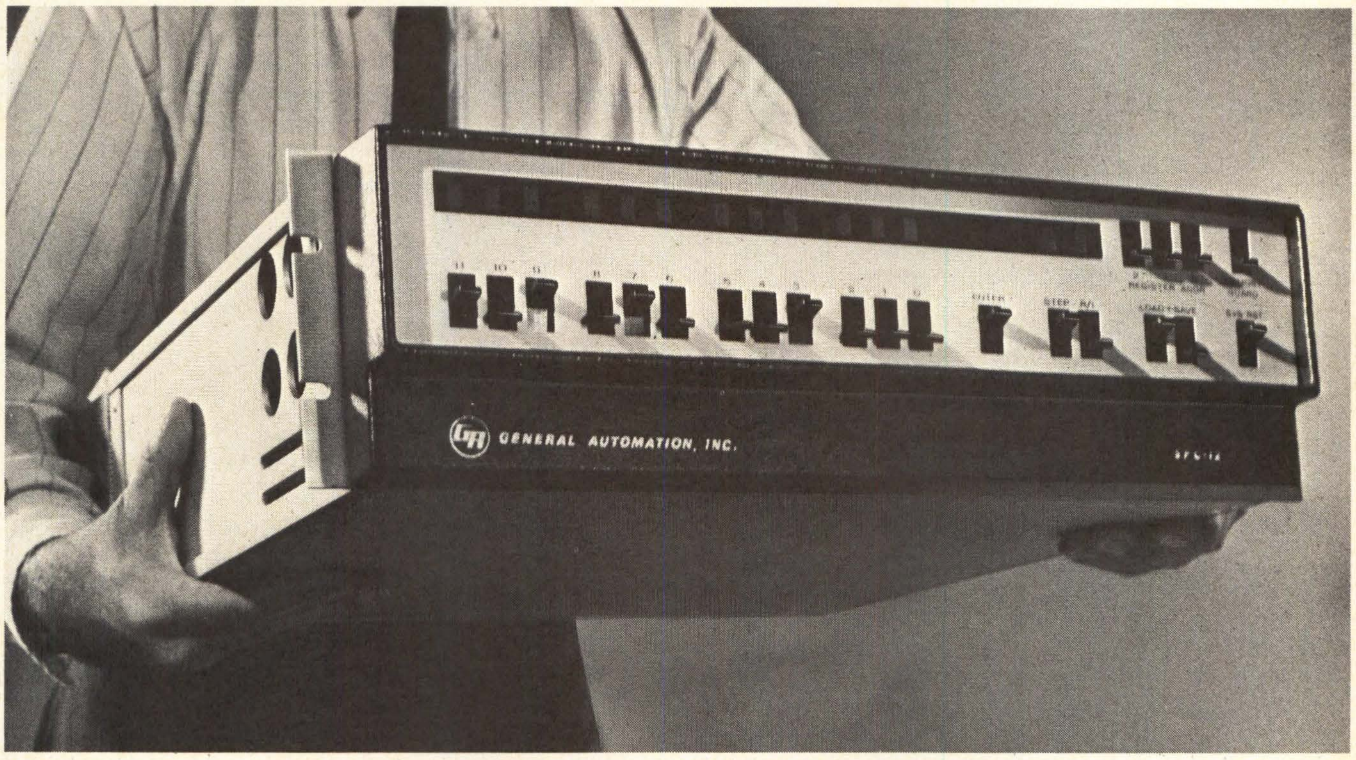

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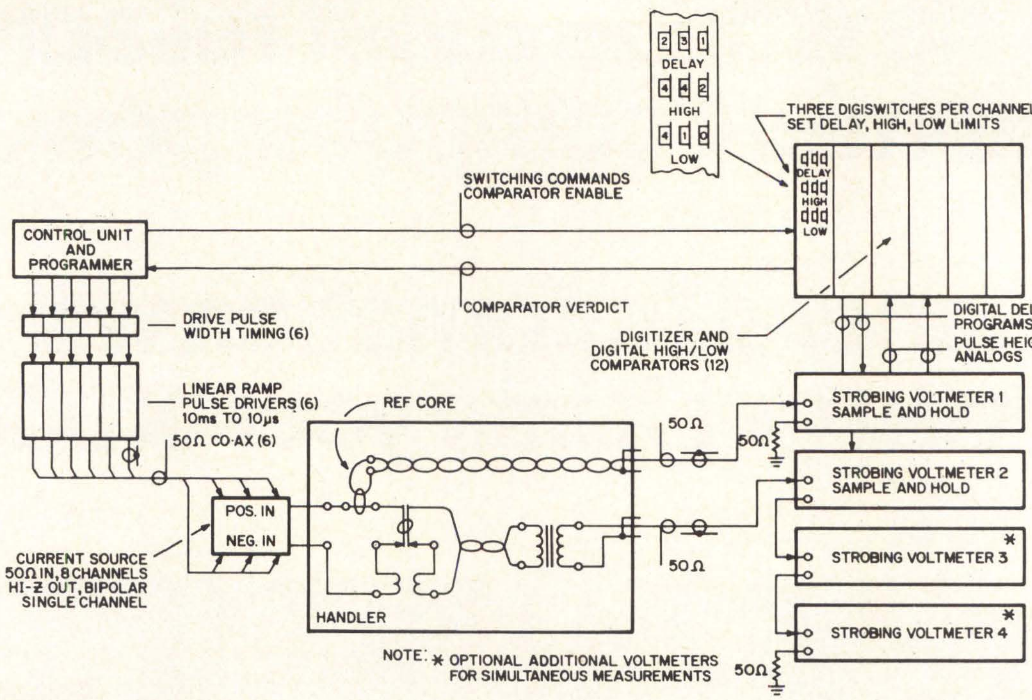


Fig. 1 Basic system elements.

Efficient synchronous multiplexing of two handlers will considerably improve the use-factor of an expensive rack of equipment which would otherwise be standing idle for as much as 80% of the time, even when running at full bore.

The Digital Revolution

It is hardly necessary now to point out the multiple advantages of digital techniques in terms of simplicity of calibration, long-term stability, simplification of system set-up, logic, and data-handling functions. It is an oddity in itself that the older generation of test equipment used in the production of the prime element of the digital revolution, the core-bit, is itself based on analog concepts; it was a certainty that the inexorable pressure of cost-per-bit would force digital techniques into the revolution's own production test equipment.

In the systems described the existence of actual measurement information in BCD form makes it possible to use digital high low comparators in every analysis channel. Instead of laborious channel-by-channel calibration of analog comparators, calibration is reduced to a single operation on the inherently stable voltmeter/digitizer unit. With the voltmeter designed to accept BCD strobe-positioning information, it is possible to make set-up of any number of analysis channels a matter of dialing in delay, high, and low settings on thumbwheel switches. The existence of an accurate pulse voltmeter already mounted in the system, complete with digital readout, also makes it possible to calibrate drive pulse amplitude without scope or other auxiliary equipment. Another bit of serendipity: with accurate BCD measurement information available, it is possible to build histogram capability right into the system simply by adding the necessary accumulators and decision logic to the basic system.

REALIZATION

With the design concepts and objectives established, we can now turn to a detailed description on the systems as realized.

Handling

The heart of a high-performance core-test system, on which its performance ultimately depends, is the handler itself and its integral signal line and probe arrangements. This is immediately apparent in considering:

• *Drive pulse risetime,* where the limiting factor is the inductance of the driveline/probe configuration inside the handler. Six inches of open wire lead corresponds to about 300 nanohenries of inductance, i.e. the excess inductance of 6″ of ≅600Ω line at 50nh/in. Driven from a 50-ohm line this represents a time constant of

$$\tau = \frac{L}{R} = \frac{300 \times 10^{-9}}{50} = 6 \text{ ns}$$

and a risetime $T_R = 2.2\,\tau = 13.2$ ms meaning that with a perfect zero-risetime step propagated down a 50-ohm cable and directly into a handler with 6″ of open wire drive line, current through the core can never rise faster than about 13 ns. Attainable risetime is seen to be directly related to physical length of the drive line of the handler. At 50 ns a 6″ line is reasonable. If the designer wants to achieve 15 ns he must reduce the drive line to several centimeters. This was one of the prime considerations in developing the signal-handling portion of the handler used: to reduce signal lines and dimensions to a minimum so that the physical plant would not be a factor in achieving speed to 15 ns. The actual drive line length inside the handler is about 4 inches. This can be driven easily to 15 ns, as shown in Fig. 1.

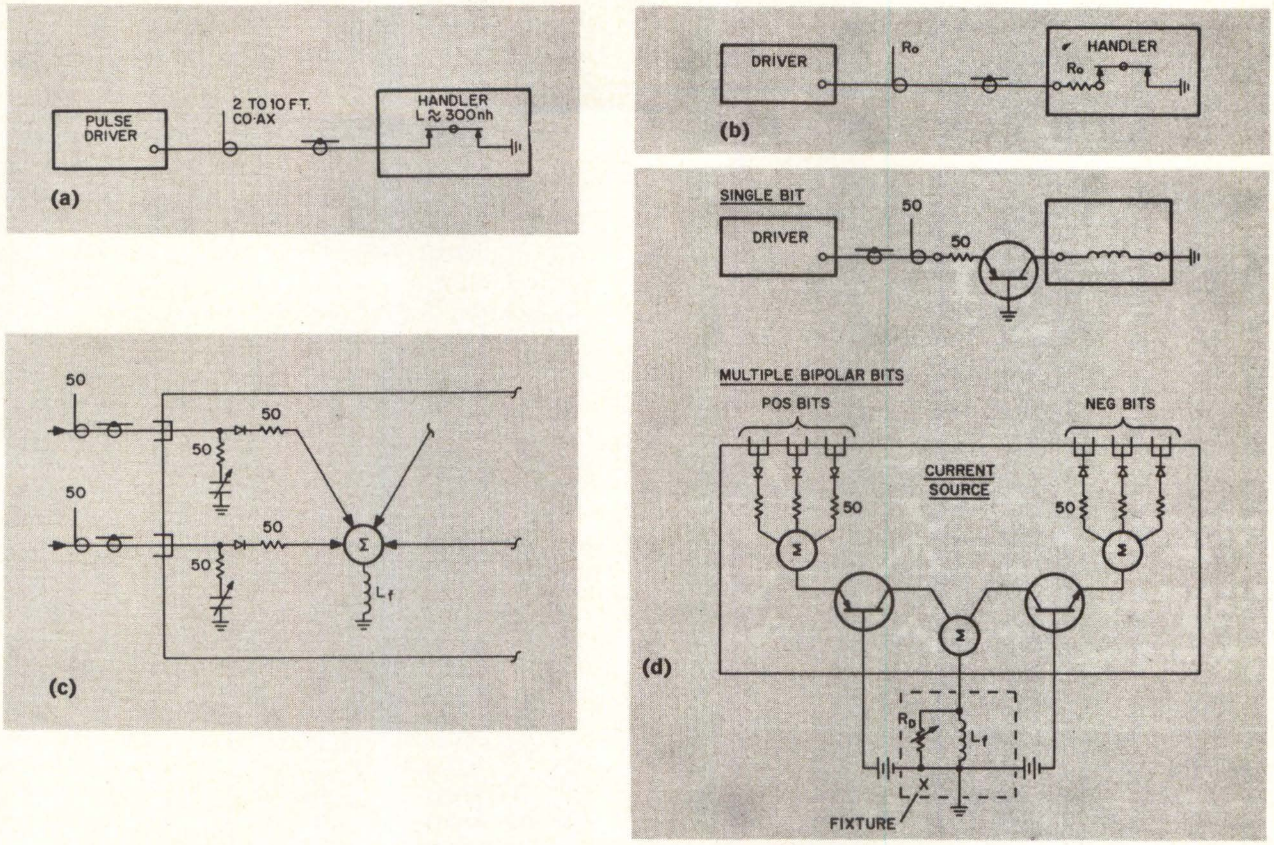
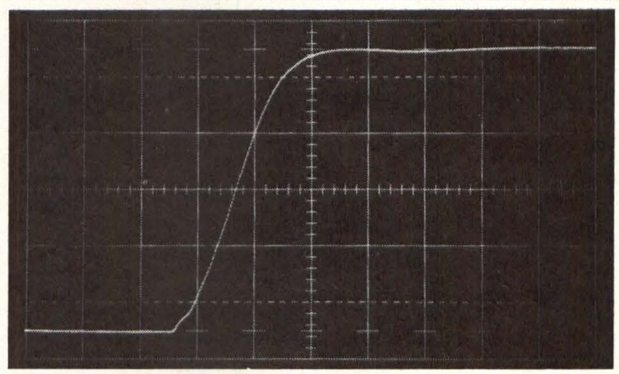


Fig. 2 Evolution of core-test fixture driving. (a) "Simultaneous" network: where transit time is a small fraction of drive pulse risetime, the L, C **constants** of the connecting line and shunt C of the driven one lumped together with the fixture inductance. (b) Faster drive causes intolerable reflections series resistor R_o makes the line see an R, L termination. If the connecting is "long" with respect to drive pulse risetime, the drive is effectively isolated from the L, R network of the fixture (c) Bit-summing from several drive lines using resistor diode networks. RC shunt legs cancel reactive component of the RL leg, i.e. give conjugate matching. (d) Using complementary transistors as an active current source mounted directly at the fixture inport: Drive-transmission is effectively isolated from fixture inductance. Fixture is driven directly from a high-impedance source.



15ms ramp from the current source above into the handler described. At 10ns & 200ma/cm.

• *Drive pulse residual on sense line.* Closely allied to the problem of reducing dimensions for faster speeds is the problem of reducing unwanted voltage coupled from drive line into sense line. Coupling is inevitable, regardless of probe arrangement, and since it is reactive, is always worse at higher speeds. Methods of cancelation which are suitable for 50 ns drive are entirely inadequate for 15 ns. A solid-probe system using minimum-length leads and air-core cancellation is described below.

• *Multiplexing.* What is required for efficient multiplexing is fully-synchronous, controlled operation in which both handlers are properly phase-related to each other. This is all but impossible to achieve with pneumatic actuation, and suggests synchronous-motor drive. The ideal multiplexed handlers would be mechanically-linked, possibly using a single motor, with disengaging mechanism to allow shutdown of one handler without affecting the other. This is the method used here: the single handler is driven by an electric motor at speeds to 18 cores per second, or 64,800 per hour. The duplexed pair may be driven from a single motor or independently as desired.

Driving

Back in the old days of 100 ns drive, it was common to see several feet of coax taking the driver output to the handler input, with no attempt at termination or making the network into a reflectionless transmission system. Transit time of three feet of line is about 5 ns, a small part of the risetime of the pulse involved; in fact the whole system could be taken as a lumped or simultaneous network. It was important that the driver be a high-impedance or current source with low shunt capacity. Since then the technique of delivering a good current ramp into several inches of open line located several feet from the rack-mounted driver has progressed through several stages of evolution as illustrated in Fig. 2.

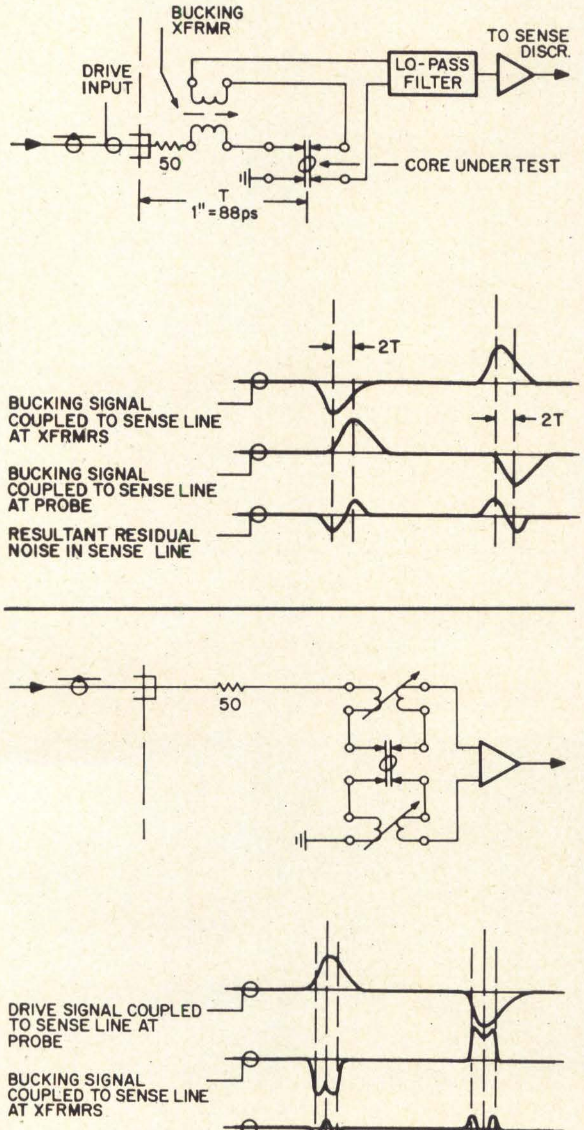


Fig. 3 Single-ended and symmetrical sense-line noise bucking.

When drive pulses got down to 50 ns and faster, the transit time of several feet of cable became noticeable in the shape of serious reflection problems, and it became necessary to start thinking in terms of lines-and-reflections rather than in terms of lumps-and-conductors. The objective became to make the transmission line see a flat termination; if this was achieved, the old definition of a good "core driver" (i.e. it should have high impedance and low shunt capacity) became obsolete. It was necessary only that the driver deliver a good clean step to the line, i.e. that it should be an essentially resistive source. And in fact, since it is all but impossible to remove all reflections from the line with passive networks, the ideal driver for flat-line systems should be neither current-source nor voltage-source, but should match the line perfectly to absorb all reflections.

Passive-network terminations with diode isolators and conjugate-matching RC networks solved all the problems of 20 ns driving but one, the summing of bipolar bits. At faster speeds the distributed nature of the long drive lines of fixtures and handlers began to make it difficult to get good conjugate matching using lumped R&C.

The need for better isolation of drive line from opposite-polarity feedthrough, and from the inductance of the load itself, led to the active-network termination of Fig. 2d. Resistor-diode summing of like-polarity bits is done in the emitter circuits of a pair of complementary grounded-base stages. Opposite-polarity summing is done in the collector circuits directly at the fixture inport. Drive lines are isolated from opposite-polarity feedthrough and from the load reactance by collector-base junctions. The drive lines see a near-perfect resistive termination; the reactive load is driven directly from a high-impedance low-capacity source. This arrangement makes it possible to deliver a clean 15 ns ramp to the minimum-lead-length handler, as shown in the scope shot of Fig. 2.

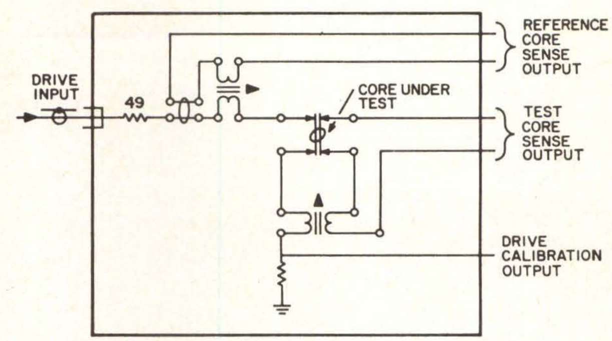
Probing, Sense-Bucking

The single element which gives the most trouble in core handlers is naturally the probe. Many manufacturers change probes every shift, and order them in thousand lots. All other things being equal, it would be a significant advance to eliminate the fragile two-piece split probe in favor of a single-piece solid probe as we might expect a significant gain in life expectancy.

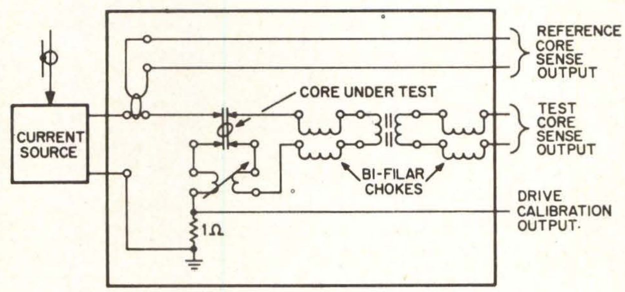
The first step in solving the problems inherent in going to faster drive is to analyze the sense-line bucking arrangements of existing systems. Figure 3 shows typical waveforms associated with single-ended systems, which use a variable-coupling cancellation transformer at the distance T from the probe. This transformer has its primary in the drive line, and its secondary in the sense line. It is supposed to supply an equal and opposite signal to the sense line to buck out the unavoidable signal coupled from the drive-line half of the probe into the sense-line half during the drive pulse. But note that the distance T represents a time-shift of the bucked signal with respect to the bucking signal. This phase shift is always twice the one-way transit time, or 2T. Therefore, if the cancellation transformer is located several inches away from the probe, for a large part of a nanosecond after the drive pulse reaches the transformer and begins to inject a signal into the sense line, there is no probe-coupled signal at all. The first rule in getting residual noise down is therefore: get the bucking signal extracted from the drive line and injected into the sense line as closely as possible to the probe.

It was thought that a second major improvement in reducing residual noise level might be to split the cancellation transformer in half and derive bucking signals both before and after the probe. While it would never be possible to reduce the time shift to zero, it is possible to bracket the probe-coupled signal in time by splitting the transformer, as in Fig. 3 b. This results in a second-order cancellation as shown. The price paid is in a small increase in drive-line length and inductance. It was found that a single loop at the low end of the probe resulted in satisfactory noise levels on the order of 1 or 2 millivolts. There seemed to be little advantage in going to a more complex split-transformer configuration. Some systems use a screw-mounted ferrite core as the method for varying the coupling of the bucking transformer. Ferrite is notoriously non-linear and it has proven much more satisfactory to oppose two half-loops of bare wire in midair, and tune out by positioning. The results are as shown in the scope shot of Fig. 4, which gives residual noise patterns for three speeds of incident pulse.

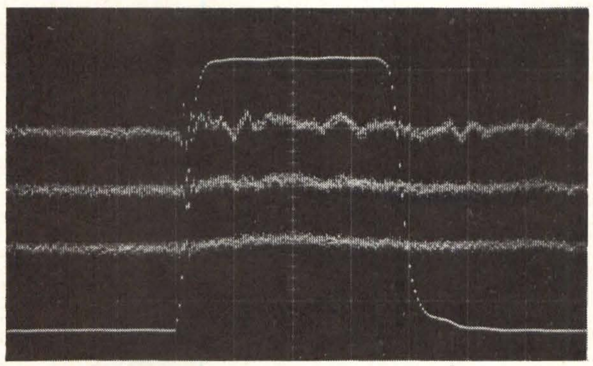
Figure 4 also compares typical split-probe and solid-probe signal-handling configurations. At first glance it might be thought that the split-probe idea is fundamentally superior in terms of isolation of sense line from drive line. A closer analysis shows that the choice is between distributed LC coupling as in a length of transmission line, and common-impedance coupling where the impedance in question is the series LR of the probe itself and its contractors. The sense-bucking problem is exactly the same except for the different mode of coupling. The dc isolation inherent in the split probe is easily achieved by a wideband bifilar transformer. Further common-mode rejection is provided by bifilar chokes on both sides of the transformer. The performance of the single-probe system of Fig. 4b is more than comparable to previous split-probe designs, to say the least: in the prototype a drive pulse developing 4 volts peak across the probe produced 4 millivolts peak-to-peak disturbance in the sense line, 1000:1 or 60 dB isolation.



(a) Typical split-probe configuration.



(b) Solid-probe configuration for use with adjacent current source.



Drive pulse and sense-line residual noise for 1-amp drive in the solid-probe fixture above.
Sense line outputs at 2mV/cm for 15ns, 30ns, and 50ns ramps.

Fig. 4 Split Probe and solid probe configuration.

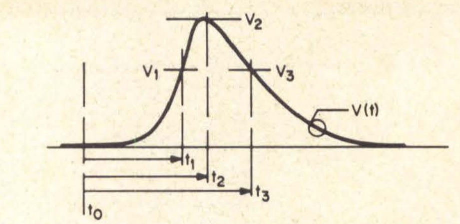
Sensing

The technique of sense analysis developed for use in this system departs radically from the established concepts of analysis employing biased discriminators. It was felt that significant improvement in performance might be gained by applying recent developments in high-speed sampling and digitizing techniques.

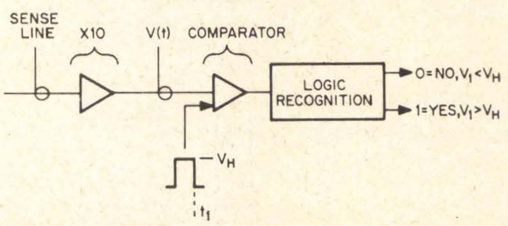
The fundamental problem in sense analysis is to determine instantaneous voltage as a function of time, i.e. on a rapidly-changing waveform whose whole duration is of the order of tens of nanoseconds, we want to establish enough voltage points $V_1, V_2, V_3, \ldots V_n$ to define the performance of the core. Regardless of the particular waveform or its position in the test pattern, whether it is uV_1, dV_1, dV_z or whatever, the basic problem is to determine whether V_1 at some time t_1 is above or below a known value, designated here v_H.

The first technique developed to solve this problem used voltage-sensitive discriminators following an amplifier. The discriminators can be peak-reading, in which case no fast timing is involved, but merely an enabling signal to pick out a particular response from the test sequence; or they can be strobed so that their time-aperture is narrowed down to several nanoseconds. Whether the circuitry is biased tunnel-diode or long-tail-pair comparator, the logic decision is made by comparing the signal waveform with an analog standard at the front end of the discriminator.

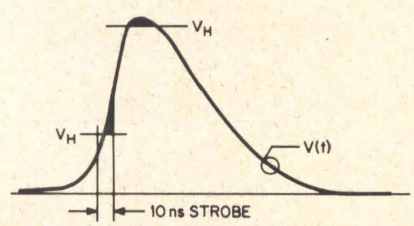
The sensitivity of a comparator of this kind is determined by the amount of charge which must be delivered from the signal source to the comparator to make it change state. In terms of the normal voltage-vs-time plot of a sense-line waveform, sensitivity corresponds to an area or a millivolt-nanosecond product. Figure 5c shows the relationship of the mV-ns product to accuracy. In the strobed measurement shown, the decision as to whether v(t) has exceeded the threshold V_h during the strobe time is entirely dependent on whether the shaded area, which is proportional to the charge being delivered into the



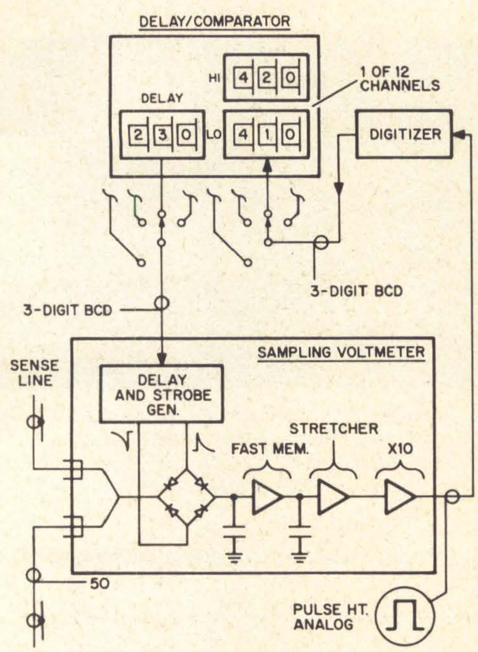
(a) Basic problem: determining V (t)



(b) Using a strobed voltage comparator



(c) Sensitivity as area, mV x ns



(d) Analysis using strobing voltmeter with digital comparators.

Fig. 5 Sense analysis

comparator, is larger than the mV-ns threshold characteristic of the discriminator. Similarly the decision as to whether V_{peak} is above the threshold V_h is dependent on the shaded area compared to the mV-ns product. Statements about "accuracy" in terms of so many millivolts plus or minus are seen to be meaningless in the dynamic test situation. A good analog comparator may make 20 mV-ns; a typical one is more like 50 mV-ns.

The design objective then becomes to lower the millivolt-nanosecond product to the point where accuracy becomes effectively noise-limited. The system of Fig. 5 d uses sampling-digital techniques to reduce the mV-ns index by about one order of magnitude, 2 mV-ns. The sense line is effectively isolated by a diode sampling gate until the 6 ns strobe is applied at the delay time set up by thumbwheels on the comparator panel. The charge required from the signal line is only what is required to load up a FET fast memory input having a time constant of about 0.5 ns. The measurement pulse is stretched and amplified and delivered as a pulse height analog to a fast digitizer which converts it to BCD. At this point measurement information of v_1 at time t_1 exists in 3-digit BCD. This is compared to limits set in by thumbwheels. Note that the voltmeter and digitizer are the only elements of the system which have to be calibrated. Any number of delay/comparator channels may be programmed to work with one or several voltmeters. The feed-through configuration of the voltmeter input makes it easy to strap several voltmeters in series off the 50-ohm sense output.

In the basic system which has two voltmeters and twelve comparator channels, core analysis might be organized on the basis of assigning one voltmeter and three comparators to the reference core, one voltmeter and nine comparators to the core under test. Then each test pass would allow one measurement on uV_1, dV_1, and dV_z for up to three passes with unique delay, high, and low settings for each measurement. Note that the simultaneous presence of actual voltage measurement information in digital form from both cores makes differential measurements as simple as adding a digital adder block to the system.

Duplexing

At a full speed of 18 cores per second, the total test cycle for the handler, is 55 ms. The probe is in position 27 ms, of which about 20 ms is actual test time. Therefore, the electronics in a single-handler system is working for about 20% of the time at best. This duty factor can be improved considerably, if not doubled, by duplexing two handlers. Two modes of operation are possible:

Asynchronous, in which no attempt is made to phase the two handlers or time relate their operating sequence to each other. Systems control switches the electronics to whichever handler is first to signal "ready". This method is practical providing the length of the test program is less than half the available test time or 10 ms. Worst case would occur when both handlers indexed simultaneously. A 10 ms program could still be run if this occurred. One advantage in asynchronous operation is the ability to shutdown one handler without disturbing the companion unit.

Synchronous, in which the two handlers are mechanically phased 180° opposed so that one is handling while the other is testing. The electronics is still switched by handler command; however, each now has full availability of 20 ms test time.

Switching. Reference to Fig. 1 shows that multiplexing handlers involves switching three signal lines. Two of these are 50-ohm coax to the voltmeters, the third is the drive line from current source to handler inport.

Switching coaxial lines is easily done using form C magnetically-operated reeds. It is immediately obvious, however, that attempting to switch the single drive line at the current source output is going to defeat one of our prime design objectives, and add several inches of length to the drive line which we have spent some time in trimming down to centimeters. To maintain the desired performance level we will have to use two current sources and switch in the 4- (or 6) bit lines between drivers and current sources, in 50 ohm geometry. This requires one form C reed per bit line, and the multiplexer becomes a block housing 6 or 8 form C reeds, three BNC connectors per reed, all actuated by a single magnet.

SUMMARY

To establish some norms for the older generation of core-test equipment, here are some typical performance-index numbers:

- Handling: Rates to 40,000/hour with single handler. To 60 or 70,000/hour with asynchronous duplexing.
- Driving: Linear-ramp low-distortion edges to 50 ns. Some handlers are difficult to drive much faster than 100 ns.
- Sensing: Sensitivities to about 20 mV-ns. Sense-line noise bucked to about 25 mV typically, to half that in well-adjusted systems. Bandwidths typically 25 MHz, corresponding to risetime capability of 14 ns.

Summarizing the performance of the systems described in this article:

- Handling: Rates to 65,000/hour with single handler, to 130,000 with synchronous duplexing.
- Driving: Linear-ramp low-distortion edges to 15 nanoseconds. This is in current waveform delivered to probe, not basic driver capability which is not a true index of driver/handler system performance.
- Sensing: Sensitivity to about 2 mV-ns. Sense-line residual noise bucked to 2 mV. Bandwidth of the sensing system equivalent to more than 100 MHz.

Performance numbers, however gratifying to the design engineer, mean little to the system user until they are translated into his language.

What precise waveform control and voltmeter sense analysis mean to the user is higher yield. The driving/sensing techniques described result in measurement accuracy approaching that of the QC test bench analysis. The result has been a striking improvement in correlation.

What all-digital sense-channel set-up means to the user is less downtime for set-up and calibration, and inherently better calibration accuracy and uniformity with single-unit calibration.

What voltmeter sensing means to the user is self-calibration of drive pulse amplitude; simultaneous high low comparisons on every measurement for cookie-cutter style bracketing of the go window; it means accurate measurement information for data analysis purposes such as the histogram generator which is a feature of the more sophisticated systems.

REFERENCES

1. Dreher, Thad, "Why Single-Shot Measurements In The Time Domain," EDN, August 1968.

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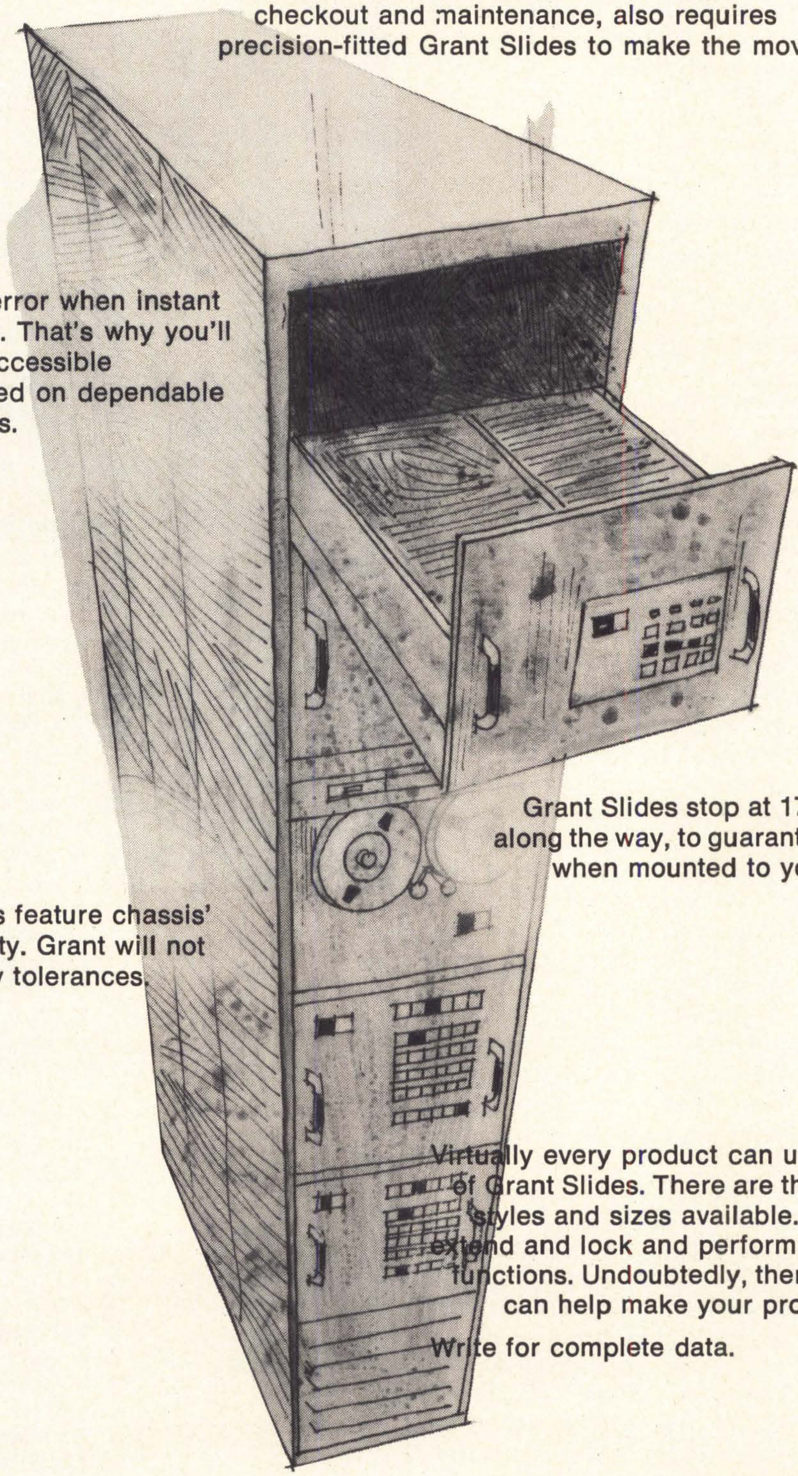

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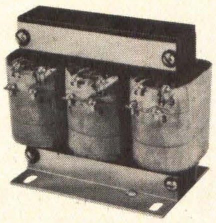

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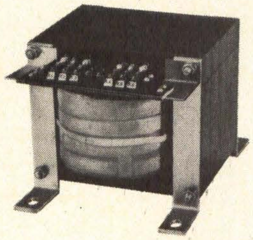

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APPLICATION NOTE

A Four Decade Numerical Display For Instrument and System Applications

EDWARD BRADY
INDUSTRIAL ELECTRONIC
ENGINEERS, INC.
Van Nuys, Calif.

The cost of information display has become increasingly more significant as larger blocks of logic are integrated and time sharing techniques are more widely practiced. As functional units are compressed in size through integration, the volume available for information display components is also proportionately reduced. As a result, appearance and, more important, legibility are often compromised to reduce volume and cost. This application note describes a four decade display system utilizing the Model SA "nimo" cathode ray display tube in conjunction with Model 770004 display logic.

The CRT as a Display Element

The cathode ray display tube used in this system employs a unique concept which combines the display characteristics of the CRT with the character generation techniques of the rear projection readout. Fundamentally, the device is a 10-gun cathode ray vacuum tube. As shown in Fig. 1, each gun is provided with a control grid cup (1). The voltage applied to this grid cup determines the aperture of an electric lens (2) in the gun structure.

Electrons are emitted from the common directly heated cathode (3). When any control grid is positive with reference to the cathode, the associated aperture is open and electrons are accelerated from the gun structure through the aperture (2). At point (4) the electron beam is a solid stream of low energy electrons. The cross section and focus at point (4) are controlled by the electro-optical characteristics of the gun structure. When the grid potential is sufficiently positive with respect to the cathode, the lens aperture is fully open and the grid has no further effect. Under this condition the character focus and position is determined only by the mechanical configuration of the gun structure. The beam, as produced by the gun structure, is picked up by the electrostatic field of the anode (5), and accelerated. A metal mask (6) with etched openings shaped in the

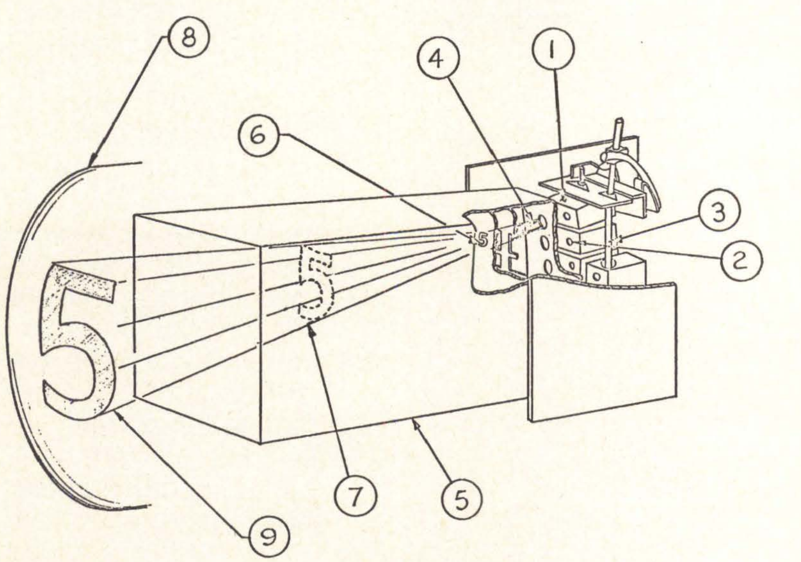

Fig. 1 Pictorial diagram IEE CRT display.

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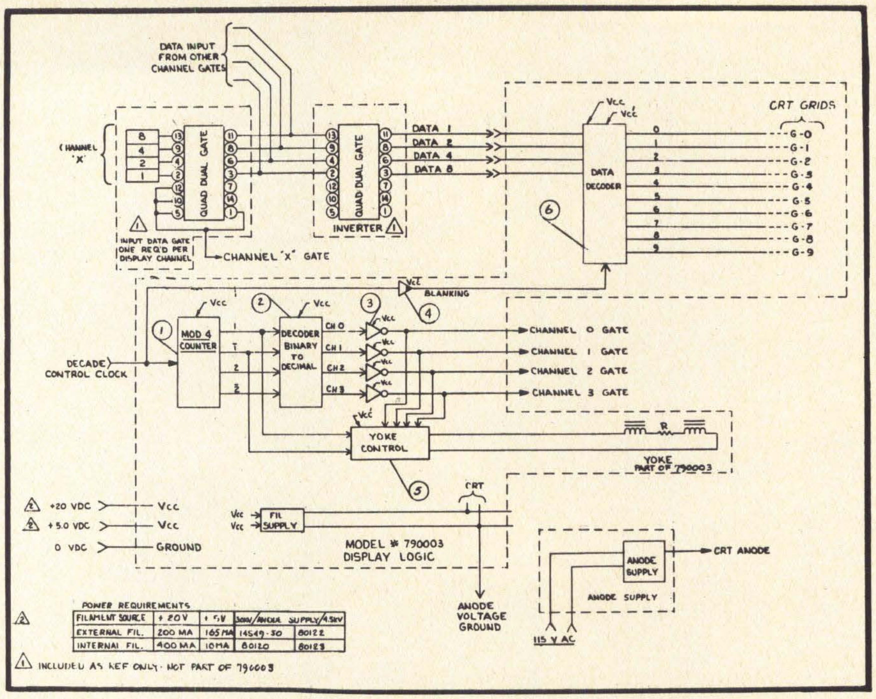

Fig. 2 Four decade display system.

form of the desired characters is situated within the anode structure such that it interrupts the electron beam. This mask is maintained at anode potential and collects electrons which collide with solid mask areas, which results in forming the cross section of the electron beam in the shape of the selected character (7).

The electron beam, thus shaped, is further accelerated by the anode field and finally collides with the phosphor screen (8), at the viewing end of the glass envelope. The phosphor reacts to the high energy impact and a phosphorescent character is displayed (9). Since each gun is independent and mechanically aimed at the screen, the only requirement for character selection and generation is the application of proper control grid potential.

Controlling the Model SA CRT Display

As noted by the preceding characteristics, the Model SA nimo is voltage operated. It requires a total grid voltage swing of 10.5 V from cut-off to fully-on for any selected character with nominal anode potential. Since the control grid voltage is referred to the cathode, it is desirable to bias the cathode positive to obtain an effective negative grid bias for cut-off conditions when the grid voltage is at ground. This is accomplished by introducing a positive 6.5 Vdc bias potential to the center tap of the filament transformer, thus producing a negative 6.5 Vdc grid potential (relative to the cathode) when the grid is at ground potential.

This bias must be bucked-out in addition to the required 4 V forward bias to fully open the character lens aperture. Thus, a total grid voltage swing of 10.5 V with respect to ground is required. Under these conditions a grounded grid results in no character display; a grid at + 10.5 V results in a displayed character.

Since the SA tube is voltage controlled, the grid current is zero except for leakage. This leakage is nominally 40 milli-microamps. The cathode potential represents a negative bias and leakage current is immeasurable for cut-off conditions.

Multiple Decade Presentation

The SA nimo has been developed to display four decades of data while the Model BA nimo is intended for single decade presentation.

The two devices are structurally identical except for an abbreviated anode in the SA nimo. This foreshortened anode structure coupled with the smaller characters (0.625″—BA; 0.35″—SA) allows the shaped beam of the SA nimo to be electromagnetically deflected from its normal center-screen target thereby displaying multiple decades. With the 0.35″ high characters, four decades are easily displayed on the face of the nimo. In special applications, 2, 3, or 5 decades may be obtained.

In practice, the standard P-31 phosphor has a decay time of 10 ms measured to a point where the loss of intensity is noticeable (35% of original brilliance). The response time is less than 100 μs, thus, a duty cycle of 10% or less is sufficient to maintain a display with adequate brilliance. If a character position is actuated with a pulse, the character will remain on the screen for a period of time after the control signal is removed. This is exactly the same phenomena used to develop as oscilloscope or television picture. Retention time, once the character is activated, is independent of control grid bias or filament voltage.

Beam deflection, decade channel selection, blanking, filament power and BCD to decimal decoding are provided by the Model 770004 display logic.

Functional Discussion Four Decade Display

A complete four decade display system using the SA nimo is schematically shown in Fig. 2. The display is comprised of:

1. Model SA nimo (1 required)
2. Model 770004 display logic (1 required)
3. Model 790003 assembly

The display logic module (770004) includes the beam deflection and data decoding circuitry. The logic module is intended to mount remotely.

The display logic is divided into three independent functional blocks:

a. Sequence control
b. Yoke control
c. Data decoding

The sequence control accepts a decade control clock in the format detailed by Fig. 3. This clock steps a four bit counter (1 in Fig. 2), the output of which is decoded (2) and inverted (3) to produce channel control gates 0 through 3. These gates are used to select the decade (or channel) to be displayed as well as position the character via the yoke control (5). The decade control clock is also used to generate the blanking pulse (4). This pulse provides Z-axis modulation to interrupt the nimo beam while the decade control clock is low by driving all control grids to ground while the cathode is held at + 6.5 Vdc, thereby biasing all grids to cutoff. When the decade control clock is high (+5V) the blanking pulse is removed and the control grid voltage levels are determined by the data decoder (6).

The yoke control combines the first two outputs of the mod-4 counter with the 4 channel gates to control the magnitude and direction of the current through the yoke. The profile of the yoke drive current is as detailed by Fig. 3. As shown, the current changes in four steps from a positive 130 mA to a negative 130 mA causing the beam to be magnetically deflected from left to right across the face of the nimo.

The data decoding section (6, Fig. 2) accepts 4-line BCD data (true terms) and decodes to decical, inverts and drives the nimo control grids. Since only a single set of ten grids is used (allowing the decoder to be time shared), all four common lines as shown by Fig. 2. The channel gate signals are used to select the channel or decade to be displayed.

The time relationship between control signals is detailed by Fig. 3. A single sweep and display cycle is as follows:

a. At the trailing edge of the decade control clock, the counter steps to channel 0.

b. Channel 0 gate is presented to the appropriate gate circuit in the data multiplexer, channel 0 is decoded and one of the 10 grids is selected.

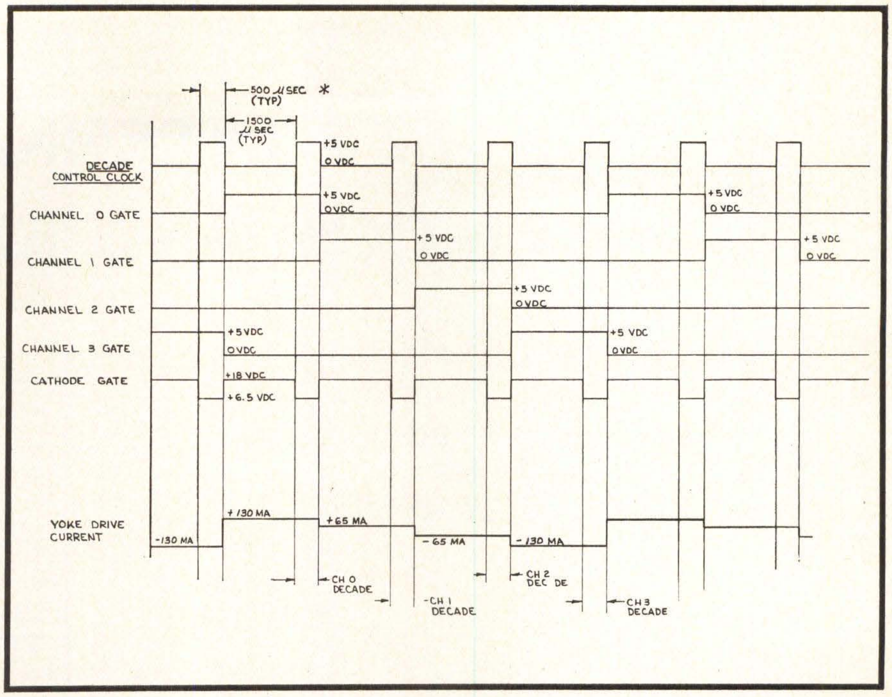

Fig. 3 Time relationship between control signals.

c. Channel 0 gate causes the yoke control to apply full positive current to the yoke.

d. The system remains static for approximately 1500 μsec (with the clock rate shown) while the yoke current stabilizes. The beam deflection is now conditioned for the full left-hand decade.

e. The decade control clock goes positive and the blanking pulse is removed allowing the character selected in "b" above to print. The selected character is displayed as long as the decade control gate is high.

f. At the falling edge of the decade control gate, the counter steps to channel 1 and a similar cycle occurs except that the yoke control modifies the yoke current to position the second decade.

g. Each character, in turn, is selected, decoded, and printed until all four decades have been displayed. Each recurrence of channel 0 initiates a new cycle.

Since the theoretical life of a nimo is a function of total charge applied to the phosphor screen, time sharing of the type discussed here has a beneficial effect on total life. Brilliance is controlled by duty cycle and anode voltage. As either is reduced the average beam current is also reduced; the charge (per unit time) applied to the screen is directly proportional to average beam current and inversely proportional to projected nimo life. Thus, at 100 foot lamberts and 3.0 KV anode voltage a duty cycle of 7.5% per character will provide an average beam current equivalent to 7.5% of the 20,000 hour beam current and a theoretical life equal to 1/0.075 x 20,000 hours or 256,000 hours.

Conclusion

This approach to data display provides the design engineer with a display element which minimizes volume and cost while providing appearance and legibility characteristics heretofore attainable only with elaborate and expensive display systems. For the first time, the instrument designer as well as the systems designer may utilize modern display techniques without sacrificing size, cost or legibility.

In keeping with the trend towards integrating larger blocks of logic, the concepts presented here allow the designer to treat the display as a component, relieving him from the task of devising special circuits.

For additional information circle No. 198 on inquiry card.

1969 IEEE INTERNATIONAL CONVENTION AND EXHIBITION

New York Coliseum and
New York Hilton Hotel
March 24, 25, 26, 27, 1969

"Unlocking the Future in Electrical/Electronic Engineering" is the theme of this year's major electronics convention. Fifty-two regular technical sessions make up the technical program, with all sessions but one to be held at the Hilton. The one exception is Monday evening's session on "Lunar Exploration in the 1970s" which will be held at the Hayden Planetarium.

Regular session hours are scheduled from 10:00 AM to 12:30 PM and from 2:00 PM to 4:30 PM. The Monday evening session at the Hayden Planetarium will be held at 8:00 PM, and the Highlight Session on Tuesday evening is scheduled for 8:00 PM.

The IEEE Exhibition at the Coliseum will be open from 10:00 AM to 8:00 PM daily, Monday through Thursday. The first floor has been set aside for production equipment and service organizations such as publishers and consultants. The second floor will be restricted to systems and instruments. The third and fourth floors will be devoted to components with all microwave components included in the third floor exhibits. There will be a free shuttle bus service between the Coliseum and the Hilton.

You may register at either the New York Hilton or the New York Coliseum. Registration hours at the Hilton are from 2:00 to 8:00 PM on Sunday, March 23, and from 9:00 AM to 5:00 PM daily during the convention, except for Tuesday when the registration period is extended to 8:00 PM because of the Highlight session that evening. Registration hours at the Coliseum are from 9:00 AM to 8:00 PM, Monday through Thursday. Registration fees are $3.00 for all IEEE members and Group Affiliates and members of the military services including civilian employees of Government establishments. Non-members may register for $6.00 and women accompanied by a registered guest for $1.00.

A Convention Digest will be available at special booths at both the Coliseum and the Hilton. During the convention, one copy of the digest will be available to IEEE members at $3; additional copies will be $5 per copy. Nonmembers may purchase copies at $5 each at the convention. After the convention, prices for members will be $5 each, and for nonmembers, $7 per copy.

TECHNICAL PROGRAM EXCERPTS

Monday Afternoon, March 24

Session 2A — Trianon Ballroom

The Role of the Citizen Engineer in Technological Decision Making

Chairman and Organizer: B. H. Manheimer, Member, Professional Staff, Center for Naval Analyses, Arlington, Va.

Panelists: Hon. J. H. Scheuer, Member of Congress, U.S. House of Representatives, Washington, D.C; Seymour Melman, Professor, Dept of Industrial and Management Engineering, Columbia University, New York, N. Y.; C. W. Fotis, Director, Employee Training and Career Development, Dept. of Defense, Washington, D.C., Visiting Professor, University of Oklahoma, also Adjunct Professor at the American University.

Session 2E — Nassau Suite

Twenty Years of Information Theory

Chairman and Organizer: J. L. Massey, Professor, Dept. of Electrical Engineering, University of Notre Dame, Ind.

INFORMATION THEORY: THE FIRST TEN YEARS, Peter Elias, Professor, Dept. of Electrical Engineering, M.I.T., Cambridge, Mass.

INFORMATION THEORY: THE SECOND TEN YEARS, R. G. Gallager, Professor, Dept. of Electrical Engineering, M.I.T., Cambridge, Mass.

THE INFLUENCE OF INFORMATION THEORY ON DIGITAL COMMUNICATION SYSTEMS, A. J. Viterbi, Associate Professor, Dept. of Engineering, U.C.L.A., Los Angeles, Calif.

SOME APPLICATIONS OF INFORMATION THEORY TO OTHER DISCIPLINES, Myron Tribus, Dean of Engineering, Thayer School of Engineering, Dartmouth College, Hanover, N.H.

Tuesday Morning, March 25

Session 3B — Mercury Ballroom

Today's Choice of Digital Computers—What's the Difference?

Chairman and Organizer: S. Fernbach, Lawrence Radiation Lab., University of California, Livermore, Calif.

Only one man in a thousand needs this kind of performance in a digital-to-synchro converter...

(the other 999 heave a sigh of relief knowing it's there)

Exclusive-design solid-state switching circuits, high-precision trigonometric transformers provide high-speed conversion from digital input of within 8.5μsec.

High-speed conversion of parallel binary-angle data to synchro and/or resolver data with 1-minute accuracy, 14 to 17-bit resolution.

Data-ready strobe eliminates effects of noise on digital-input lines, can be addressed for use in multiplex operation.

Full protection against overload, power-line transients, frequency changes or improper reference frequency, or short circuit of output terminals.

The North Atlantic Series 538/10 Digital-to-Resolver/Synchro Converter is available in many configurations with many optional features, including higher accuracy, to provide the digital-to-analog interface required by the user. It is another example of the versatile and elegant instrumentation and control systems available from North Atlantic Industries. For additional rewarding information, call our field-engineering representative (see EEM), use the reply card, or write or call North Atlantic Industries, Inc., Terminal Drive, Plainview, Long Island, N.Y. 11803. (516) 681-8600

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COMPUTER WORKLOAD EVALUATION AS A GUIDE FOR FUTURE REQUIREMENTS, H. R. Bruijnes, Lawrence Radiation Lab., University of California, Livermore, Richard Brown, Professor, Physics Dept., University of Illinois, Urbana

APPLICATION OF COST-EFFECTIVENESS ANALYSIS TO EDP SYSTEM SELECTION, Jack Porter, The Mitre Corp., Bedford, Mass.

SELECTION OF COMPUTERS FOR ADMINISTRATIVE PURPOSES, Tom Patterson, Electronics Officer, Continental Illinois National Bank and Trust Co. of Chicago.

Session 3E Nassau Suite

Modern Technology for Signal Handling

Chairman and Organizer: J. J. Stiffler, Principal Engineer, Raytheon Co., Sudbury, Mass.

TIME DIVISION MULTIPLE ACCESS FOR LARGE USERS AND SMALL, W. G. Schmidt, Branch Manager, COMSAT Labs., Communication Satellite Corp., Washington, D.C.

DATA MODEMS WITH INTEGRATED DIGITAL FILTERS AND MODULATORS, P. G. van Gerwen, P. van der Wurf, Phillips Research Lab., Eindhoven, The Netherlands.

SAME FREQUENCY REPEATER TECHNIQUES, Morton Parker, Principal Engineer, Communications Systems, David Trask, Principal Engineer, Communications Systems, Thomas Gluszccak, Engineer, Communications Systems, Space Information Div., Raytheon Co., Sudbury, Mass.

ADAPTIVE EQUALIZATION—OPTIMUM AND PRACTICAL DESIGN, W. E. Coffrin, Sr. Engineer, Applied Communications Research Dept., Raytheon Co., Norwood, Mass.

THE EVALUATION OF PLANETARY COMMUNICATION TECHNOLOGY, R. C. Tausworthe, Member, Technical Staff, Telecommunications, Jet Propulsion Lab., Pasadena, Calif.

Session 3G Gramercy Suite

Thin Films or Thick

Chairman: R. E. Thun, Technical Director, Industrial Components Div., Raytheon Co., Bedford, Mass.

Organizer: D. A. McLean, Director, Components Lab., Bell Telephone Labs., Inc., Allentown, Pa.

INTRODUCTION TO THE SUBJECTS, R. E. Thun, Technical Director, Industrial Components Div., Raytheon Co., Bedford, Mass.

MATERIALS AND COMPONENT CAPABILITIES OF THICK FILMS, Darnall Burks, Sprague Electric Co., North Adams, Mass.

MATERIALS AND COMPONENT CAPABILITIES OF THIN FILMS, Leon Maissel, Manager, Basic Studies, Thin Films, IBM Corp., East Fishkill, N. Y.

APPLICATION OF THICK FILMS TO MICROELECTRONICS, Morton Topfer, Leader, Hybrid Circuit Subsystem, Defense Microelectronics Div., Bell Telephone Labs., Inc., Murray Hill, N. J.

APPLICATION OF THIN FILMS TO MICROELECTRONICS, David Feldman, Dept. Head, Film Circuits and Component Development, Bell Telephone Labs., Inc., Murray Hill, N. J.

Discussion and Summary Led by R. E. Thun.

Tuesday Afternoon, March 25

Session 4A Trianon Ballroom

Where is the Electrical Engineering Profession Headed?

Chairman and Organizer: W. D. Rowe, Sub-Dept. Head, Special Studies, Systems Development, The Mitre Corp., McLean, Va.

Moderator: W. D. Rowe, Sub-Dept. Head, Special Studies, Systems Development, The Mitre Corp., McLean, Va.

Panelists: S. W. Herwald, Junior Past President, IEEE, Vice President, Electrical Engineering, Westinghouse Electric Corp., Pittsburgh, Pa.; J. L. McLucas, President, The Mitre Corp., McLean, Va.; W. K. Linville, Executive Head, Dept. of Engineering-Economic Systems. Stanford University, Calif.; T. F. Rogers. Director, Office of Urban Technology and Research, U. S. Dept. of Housing and Urban Development, Washington, D.C.; E. A. Walker, President, National Academy of Engineering, Washington, D.C. and President, Pennsylvania State University, University Park.

Session 4E Nassau Suite

Computer Languages for Process Control

Chairman and Organizer: E. A. Weiss, Coordinator, Corporate Computer Planning, Sun Oil Co., Philadelphia, Pa.

The invited panel members will introduce the subject and the tabulation and will make brief comments on the possible nature of a common language. The audience will be expected to comment and contribute.

Tuesday Evening, March 25

8:00-10:00 P.M.

Highlight Session Grand Ballroom

Electronically Expanding the Citizen's World

Moderator: The Honorable James D. O'Connell, Director, Telecommunications Management, Special Assistant to the President, Washington, D.C.

Organizer: K. H. Fischbeck, RCA, David Sarnoff Research Center, Princeton, N. J.

The Honorable James O. O'Connell will moderate a panel discussion with the following panelists:
J. H. Hollomon, President, University of Oklahoma, Norman, and former Assistant Secretary of Commerce for Science and Technology.
E. G. Fubini, Vice President and Group Executive, IBM Corp., Armonk, N. Y.
K. G. McKay, Vice President, Engineering AT&T, New York, N. Y.
J. Hillier, Vice President, Research and Engineering, RCA Princeton, N. J.

Session 5E Nassau Suite

Trends in Instrument-Computer Systems

Chairman and Organizer: B. O. Weinschel, President, Weinschel Engineering, Inc., Gaithersburg Md.

ENHANCEMENT OF DC AND AF PRECISION MEASUREMENTS BY COMPUTER, J. C. Riley, Member, Technical Staff, Electro Scientific Industries, Inc., Beaverton, Ore.

A 3700-4200 MHZ COMPUTER CONTROLLED MEASUREMENT SYSTEM FOR LOSS, PHASE, ENVELOPE DELAY AND REFLECTION, D. Leeds, Supervisor, Microwave Measurements, Bell Telephone Labs., Inc., Holmdel, N. J.

EXPERIENCE AND STATUS OF COMPUTER TEST EQUIPMENT SYSTEMS IN DOD/NASA, D. M. Goodman, Director, Project SETE School of Engineering and Science, New York University, N. Y.

USE OF COMPUTERS WITH FACTORY TEST EQUIPMENT, S. N. Levy, Administrator, Automatic Test and Measurement Systems, RCA, Camden, N. J.

Session 5G Gramercy Suite

Semiconductor Memory

Chairman and Organizer: J. M. Goldey, Director, Materials and Process Technology Lab., Bell Telephone Labs., Inc., Allentown, Pa.

SEMICONDUCTOR MEMORIES—DEVICE ASPECTS, G. E. Moore, Vice President, Intel Corp., Mountain View, Calif.

MONOLITHIC MEMORY—PROGRESS AND POTENTIAL, J. A. Ayling, Manager, Memory Product Design, IBM Components Div., Poughkeepsie, N. Y.; Benjamin Agusta, Sub-Dept. Head, Special Studies Systems Development, IBM Components Div., Essex Junction, Vt.

P-CHANNEL IGFET MEMORIES, E. J. Alexander, Head, Semiconductor Memories Div., Bell Telephone Labs., Inc., Allentown, Pa.

COMPLEMENTARY MOSFET MEMORIES, G. B. Herzog, Director, Data Processing, Applied Research Lab., RCA, Princeton, N. J.

Wednesday Afternoon, March 26

Session 6A — Trianon Ballroom

LSI in Use

Chairman and Organizer: C. G. Thornton, Director, Research and Development, Philco-Ford Corp., Blue Bell, Pa.

OPERATIONAL COMPUTER-AIDED SYSTEM AND MOS LSI DESIGN PROCEDURES, J. Orson Field, Assistant Manager, Materials and Design Services of Engineering, National Cash Register Co., Dayton, Ohio.

ARRAY PROCESSING AND LARGE SCALE INTEGRATION, J. O. Campeau, Member, Technical Staff, Litton Systems, Guidance & Control Div., Woodland Hills, Calif.

THE LIMAC—AN LSI DEMONSTRATION VEHICLE, G. B. Herzog, Director, Data Processing, Applied Science Research Lab., RCA Labs., Princeton, N. J.

LSI IN USE—THE PRACTICAL APPROACH, W. E. Wickes, Manager, Advanced Integration Programs, Texas Instruments, Inc., Dallas.

Session 6B — Mercury Ballroom

Computer Peripherals

Chairman and Organizer: Eugene Shapiro, Sr., Corporate Technical Communications, IBM Corp., Armonk, N. Y.

THE SYSTEMS APPROACH TO THE DESIGN OF MAGNETIC TAPE EQUIPMENT, W. B. Phillips, Sr. Engineer and Assistant, Development Div., IBM Corp., Boulder, Colo.

ELECTROMECHANICAL ACTUATORS FOR COMPUTER PERIPHERALS, G. C. Newton, Associate Director, Electronic Systems Lab., Professor, Dept. of Electrical Engineering, M.I.T., Cambridge, Mass.

COMMUNICATIONS AND DISPLAYS, H. S. MacDonald, Assistant Director, Communications Principles Research Lab., Bell Telephone Labs., Inc., Murray Hill, N. J.

Thursday Morning, March 27

Session 7B — Mercury Ballroom

Communications and the Computers

Chairman: D. C. Evans, Director, Computer Science Dept., University of Utah, Salt Lake City.

Organizer: J. A. Young, Director, Communication Principles Research Lab., Bell Telephone Labs., Inc., Holmdel, N. J.

COMPUTERS AND COMMUNICATIONS—WHAT'S THE PROBLEM?, D. C. Evans, Director, Computer Science Dept., University of Utah, Salt Lake City.

RESEARCH SHARING COMPUTER NETWORK, L. G. Roberts, Special Assistant for Information Sciences, ARPA, Dept. of Defense, Washington, D.C.

COMMUNICATIONS FOR INTERACTIVE ON-LINE COMPUTER SYSTEMS, Gerald Estrin, Professor, Electrical Engineering, U.C.L.A., Los Angeles, Calif.

DATA COMMUNICATION REQUIREMENTS OF COMPUTER SYSTEMS, R. Kerby, Manager, Advance Technology, IBM Corp., Research Triangle Park, N. C.

COMPUTERS FROM THE COMMUNICATIONS VIEWPOINT, E. E. David, Jr., Executive Director, Research, Communications Systems Div., Bell Telephone Labs., Inc., Murray Hill, N. J.

Session 7E — Nassau Suite

The Interdisciplinary Nature of Design

Chairman and Organizer: M. M. Tall, Manager, Defense Products, RCA, Moorestown, N. J.

SYSTEMS ANALYSIS, George Luchak, Professor, Systems Engineering in Civil and Geological Engineering Dept., Princeton University, N. J.

SYSTEMS ENGINEERING MANAGEMENT PLANNING, Keith Sargent, Western Div., Arinc Corp., Santa Ana, Calif.

CONTRIBUTIONS OF MECHANICS AND CHEMISTRY TO ELECTRONIC DESIGN, G. Reethof, Alcoa Professor of Mechanical Engineering, Pennsylvania State University, State College

THE IMPACT OF NEW TECHNOLOGY, James Vollmer, Manager, Advanced Technology, Defense Electronics Products, RCA, Camden, N. J.

Thursday Afternoon, March 27

Session 8A — Trianon Ballroom

The Electronic Package What—Why—How Much?

Chairman: Leon Podolsky, Consultant, Pittsfield, Mass.

Organizer: A. P. Kromer, Varian Associates, Palo Alto, Calif.

Moderator: Leon Podolsky, Consultant, Pittsfield, Mass.

Panelists: C. J. Dietrich, Manager, Product Design, Electronic Systems Div., TRW Systems, Redondo Beach, Calif.; J. J. Clement, President, Clement Labs., Mountain View, Calif.; E. D. Stoeckert, Group Engineer, R & D Div., Lockheed Missile & Space Co., Sunnyvale, Calif.; Joseph St. Amour, Chief Mechanical Engineer, Digital Equipment Corp., Maynard, Mass.; Robert Hansen, Manager, Color TV Development, Consumer Products Div., Motorola Inc., Franklin Park, Ill.

Session 8B — Mercury Ballroom

Graphics and Computer-Aided Design

Chairman and Organizer: G. L. Baldwin, Head, Computer Graphics Development Dept., Bell Telephone Labs., Inc., Murray Hill, N. J.

MAN-MACHINE TEST PATTERN GENERATOR, R. G. Carpenter, Sr., Associate Engineer; L. K. Lange, Staff Engineer, Components Div., IBM Corp., East Fishkill, N. Y.

ULTRA PRECISION ARTWORK GENERATED WITH A CRT DISPLAY, Wayne Huelskoetter, Manager, Computer Graphics Marketing Support; Joseph Kimlinger, Engineering Manager, UNIVAC, Roseville, Minn.

INTERACTIVE GRAPHICS FOR INTEGRATED CIRCUIT LAYOUT DESIGN, Philip Hudson, Member, Technical Staff, Texas Instruments, Inc., Dallas.

INTERACTIVE COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS, J. A. Narud, Motorola Inc., Phoenix, Ariz.

Session 8E — Nassau Suite

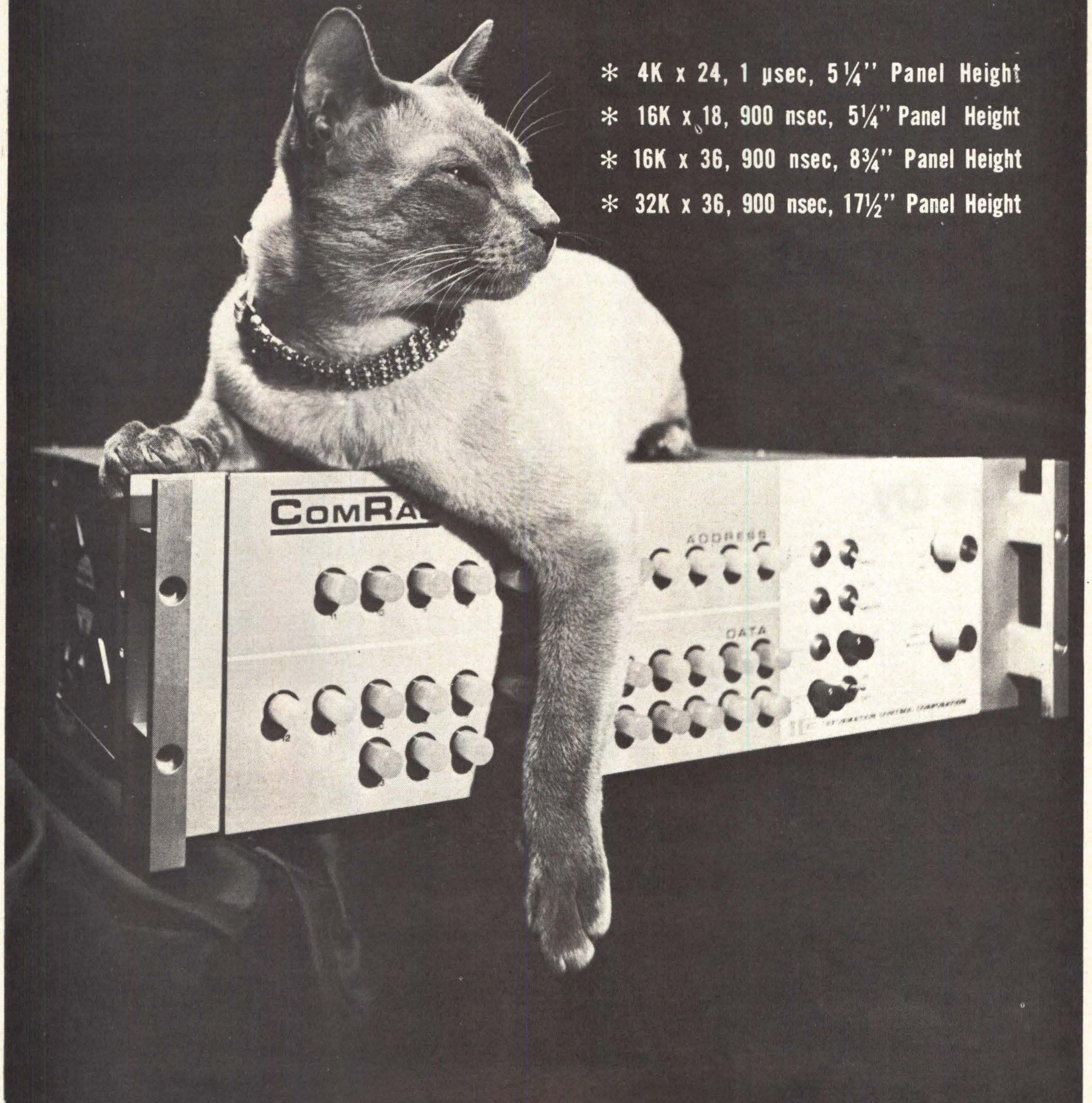
An International Language for Electronics?

Chairman and Organizer: Edward Keonjian, Grumman Aircraft Engineering Corp., Bethpage, N. Y.

Moderator: Edward Keonjian, Gruman Aircraft Engineering Corp., Bethpage, N. Y.

The international panel of prominent leaders in various areas of electronics will discuss the means and methods of developing a better mutual understanding in their respective fields. Special attention will be given to the works of the International Electrotechnical Commission (IEC) which is devoted to the promotion of world-wide standards and to the development of mutual cooperation in intellectual scientific and technological activities.

CAT ON A HOT CORE MEMORY



* 4K x 24, 1 μsec, 5¼" Panel Height
* 16K x 18, 900 nsec, 5¼" Panel Height
* 16K x 36, 900 nsec, 8¾" Panel Height
* 32K x 36, 900 nsec, 17½" Panel Height

INFORMATION CONTROL CORPORATION

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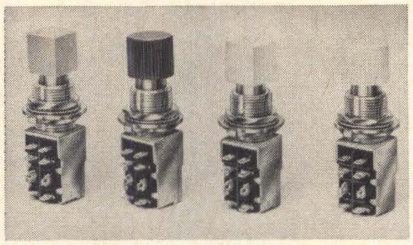
CIRCLE NO. 40 ON INQUIRY CARD

IEEE PRODUCTS

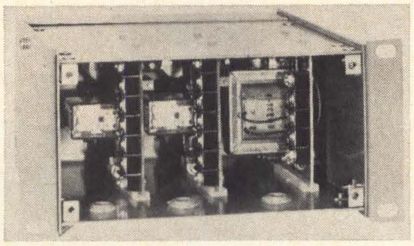


ILLUMINATED PUSH BUTTON

MSPN series switches have a current rating of 6 A @ 125 Vac. Standard T-1 3/4 grooved lamps are employed which are easily replaceable from the front without the use of special tools. Side terminals are incorporated for printed circuits or wired installations.

The switches feature a metal construction, phenolic case, and solid silver contacts. Each switch mounts in a standard 15/32" diameter hole and comes equipped with two hex nuts, locating ring, and lock washer. A wide choice of plastic buttons are supplied optionally in three basic sizes (1/2", 5/8", 3/4"), either round or square shapes, each in a choice of nine color shades. Alco Electronic Products, Inc., Lawrence, Mass. See at IEEE Booth 4G23.

Circle No. 255 on Inquiry Card.



CURRENT/VOLTAGE ALARMS

Single and dual current and voltage alarms produce alarms by means of a relay contact actuated when the input voltage or current signal reaches the value of the internal set point. The set point is adjustable to give an alarm at any value desired.

The alarms feature all solid state components and provide 0.1% accuracy, excellent temperature stability, and are immune to line fluctuations. Units maintain their calibration for a full year. Ease and accessibility are provided by front connected field wiring. Deltron, Inc., Control Div., North Wales, Pa. See at IEEE Show Booth 2J35.

Circle No. 205 on Inquiry Card.

DC SERVOMOTORS

Two dc servomotors, the HSM30 and HSM100, feature hollow rotors which exhibit low inertia and low inductance.

The HSM30 has an armature inertia of 0.00039 oz-in-sec^2, a mechanical time constant of 1.55 ms, acceleration of 370,000 rads/sec^2 and a power rate of 376 kw/sec (initial at 24V). The HSM30 weighs 4.5 pounds. The HSM100 features: armature inertia of .0037 oz-in-sec^2, a 2 ms time constant, acceleration of 149,000 rads/sec^2, and power rate of 580 kw/sec (initial at 24V). Honeywell Inc., Manchester, N.H. See at IEEE Booth 2G49.

Circle No. 266 on Inquiry Card.

INTERACTIVE MICROFILM FILE

The AIM System II (Automated Information Management) provides for the subscriber who needs information that is not contained in the file due to obsolescence or limited use. When the subscriber has a problem, he picks up the handset on the side of the reader/printer and the "Libraphone" places him in immediate voice communication with AIM Central Information Center. He can search the central files, have special material given to him verbally or request the inclusion of new material in the file.

AIM System II contains over 1,000,000 pages of material representing over 7,000 complete vendor catalogs, a complete set of MLS, MS, AND and AN specifications, standards, QPLs and descriptive patterns, and the complete D.A.T.A. Transistor Information File of over 20,000 pages covering 5,000 type numbers. Specialized Business Services, Inc., Jericho, N.Y. See at IEEE Booth 1K13.

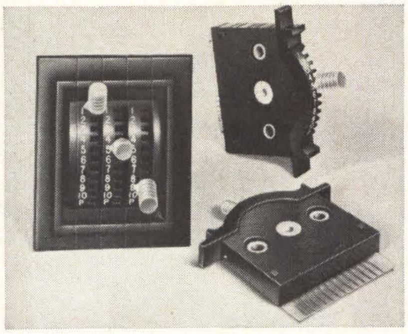
Circle No. 258 on Inquiry Card.

HIGH VOLTAGE SOURCE

Model 1579 power source for high voltage CRT display systems furnishes highly stable, low noise corona-free voltages between 10 KV and 30 KV. The unit features a series of completely encapsulated modular high voltage blocks which nest into each other mechanically and electrically.

Specifications include: Maximum output current of 1 mA; 0.0025% regulation for line or load variations; less than 250 mV ripple p-p; output voltage drift less than 100 ppm per hour and 300 ppm per 24 hours; and repeatability of 100 ppm. Power Designs, Inc., Westbury, N.Y. See at IEEE Booths 2G10-2G11.

Circle No. 253 on Inquiry Card.



PROGRAMMING CIRCUIT SELECTOR

The Slide 'n Switch programming circuit selector is a modular switch featuring the ability to go from any one of a total of eleven positions to any other position without contacting intermediate switch steps enroute. It features printed-circuit construction with gold-plated contacts for minimum contact resistance over many operations. The units may be stacked horizontally for higher programming capability and mounted in a variety of ways to suit specific user requirements. Output terminations fit conventional PC edge mount connectors, while knobs and cases can be supplied in a variety of colors. Contacts are rated to carry 3 A static, 250 mA during switching for a minimum of 250,000 operations. Sealectro Corp., Mamaroneck, N.Y. See at IEEE Booths 4E03-4E07.

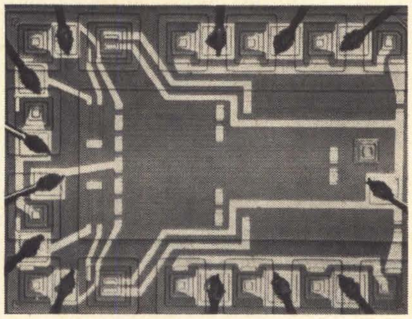
Circle No. 269 on Inquiry Card.

IEEE PRODUCTS

RIBBON CABLE

A flexible woven ribbon cable, designated as FRC Controlled Impedance Cable, is a circuit which may be folded, rolled, twisted, or even tied in knots with no tendency to delaminate or change impedance. A controlled impedance of 80 ohms with less than ±10% deviation has been maintained, and cross-talk reduced below 10%. In some applications it has replaced four different lengths of flexible printed circuits, as only one length for all interconnect levels is needed simply by following a folding procedure. Zippertubing Co., Los Angeles, Calif. See at IEEE Show Booth 1B28.

Circle No. 238 on Inquiry Card.



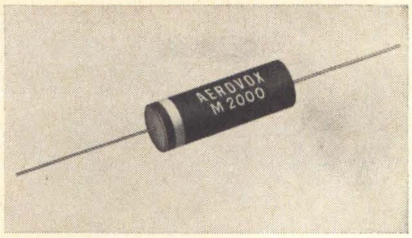
HARDENED ICs

A family of 930 DTL devices consists of a Dual 4 Gate (RD-930R), a Dual 4 Buffer (RD-932R), a Dual 4 Power Gate (RD-944R), a Clocked Flip-Flop (RD-945R), and a Triple 3 Gate (RD-962R). All of the circuits, with the exception of the dual level shifter and the dual line driver, are plug-in replacements for the 930 DTL non-hardened series and operate over the full military temperature range of −55°C to +125°C.

The RD-980R dual level shifter operates from +5V and −15V or −22V power supplies and interfaces with standard logic circuits such as DTL and TTL. It is suitable for driving either MOS or junction-FET gates.

The RD-981R dual line driver has a post neutron output current capability of 50mA over the full temperature range of −55°C to +125°C and exhibits excellent overall hardened properties. Radiation Inc., Melbourne, Fla. See at IEEE Booths 4H19-4H21.

Circle No. 259 on Inquiry Card.

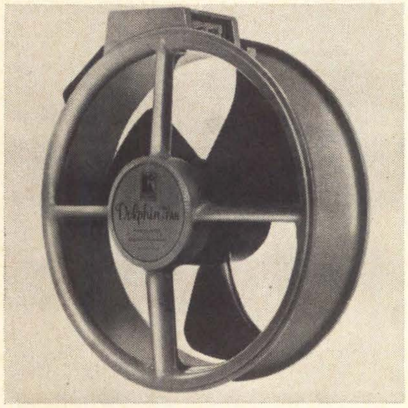


MINIATURE TUBULAR MICAS

A series of plastic-cased miniature tubular micas feature small size and a unique construction that permits micas to achieve a tubular configuration. They meet the electrical and environmental test requirements of MIL-C-5C and EIA RS-153A, and are presently being produced in both bulk and reel form.

The tubular mica units are available in a capacitance range of 1 pF to 1,000 pF and working voltages of 500, 300 and 100 Vdc. All units measure 0.312" dia x 0.515" long, regardless of value. Standard capacitance tolerance of the tubular mica line is ±5%. Units are also available to ±1%. Aerovox Corp., New Bedford, Mass. See at IEEE Booths 4E04-4E06.

Circle No. 263 on Inquiry Card.



AIR MOVER

The Dolphin^{R} Fan is an economical unit which provides up to 265 CFM from a $2\frac{7}{16}$" deep axial package for as long as five years of continuous operation. This highly reliable fan features oil-impregnated sleeve bearings and mounts easily with clips on integral clamping rims. It is airflow reversible by mounting on either face and can be used continuously in ambient temperatures up to 65°C.

Motors are available in both 115 and 230 Vac, 60 Hz, 1 Phase. The unit produces minimum acoustical disturbance and has characteristics below NC-55. Rotron Inc., Woodstock, N.Y. See at IEEE Booths 4B05-4B09.

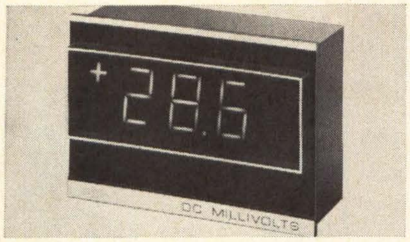
Circle No. 250 on Inquiry Card.

METAL OXIDE GLAZE RESISTORS

MOX resistors range in maximum voltage from 1000V for the MOX-400 unit up to 5000V for MOX-1125. Wattage ratings are from 0.25 to 1.0. The larger MOX resistors go from MOX-1 with 7500V maximum voltage and 2.5W rating at 70°C up to MOX-5 of 37,500V maximum voltage and 12.5W rating at 70°C. Larger and smaller units can be produced on special order. Maximum hotspot temperature is 220°C.

Available tolerances are given as ±2% and ±5% over the entire range of resistances to 2500 megohms, with ±1% to 1000 megohms, and ±½% up to 100 megohms. High stability of less than 1% full-load drift in 2000 hours, and shelf drift less than 0.1% per year are also features. Victoreen Instrument Div., Cleveland, Ohio. See at IEEE Booth 3B08.

Circle No. 265 on Inquiry Card.

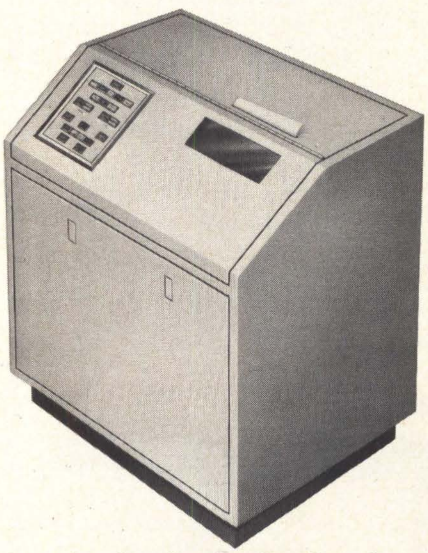


DIGITAL PANEL METER

A 3-digit digital panel meter, Model 4301, with a display readable from 40 feet and a depth of only 1½ inches, has a removable power supply that may be remotely mounted within three feet. Overall size of the instrument with attached power supply is 4½" w x 3" h x 4½" d. It may be mounted from either the front or rear of a panel. It has an accuracy of ±1 digit, 30% overrange, autopolarity and a TTL/DTL compatible BCD output.

The display uses ⅞"-high seven-bar segmented digits to provide a non-blinking display for readability over angles of ±70° at distances of 40 feet. The digits are presented in a single plane at the front of the display area. Other standard features include print command, display hold, polarity, and overrange output. Voltage ranges are 0-99.9 mV to 0-999 V and current ranges of 0-9.99 μA to 0-99.9 mA. Input impedance is 1000 megohms. API Instruments Co., Chesterland, Ohio. See at IEEE Booth 2G34.

Circle No. 251 on Inquiry Card.



IEEE PRODUCTS

N/C ASSEMBLY CENTER

A numerically-controlled assembly center, Model PCP-300, is the first of a series of systems utilizing the ARAT system (Automatic Random Access Transport). A self-sufficient assembly center, it makes possible insertion rates many times higher than those achieved by conventional assembly methods, virtually eliminating assembly errors in the process.

The PCP-300's solid-state circuitry is programmed to deliver the correct component tray from any of 300 trays in the console's storage magazine. An articulated overhead projector then flashes an image onto the assembly to show the operator the correct positioning and polarity for each component. Ragen Precision Industries, Inc., N. Arlington, N.J. See at IEEE Booths 1A07-1A09.

Circle No. 257 on Inquiry Card.

SEMICONDUCTOR ANALYZER

PM 6509 Meter measures leakage current down to 3 pA, breakdown voltage up to 1000 V, and resistance up to 100 Tera-ohms without auxiliary equipment. Previously available instruments permitted measurements in the pico and nano-amp regions only by employing special assemblies; including switching facilities, a highly sensitive dc micrometer, a stable leakage-free power supply, auxiliary power supplies for third and fourth connections, resistance blocks, etc. Measurements are made with the PM 6509 by connecting the semiconductor to the meter, adjusting voltage and current limits, and reading off the quantities.

The PM 6509 is ideally suited for lot sample testing as well as detailed analysis of diodes, transistors and other semiconductors, including silicon devices. Philips Electronic Instruments, Mt. Vernon, N.Y. See at IEEE Booths 2B15-2B21.

Circle No. 262 on Inquiry Card.

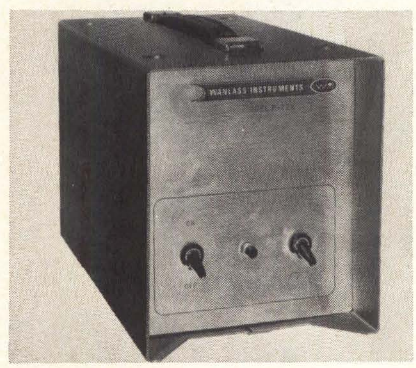
RIBBON CABLE

Ribbon cable made with XL PVC insulation won't melt, smoke or shrink back if hit by a hot soldering iron. It's more solvent-resistant than ordinary PVC and several times tougher than TFE against cutting, crushing and abrasion.

Using XL PVC, the bonded round conductor flat ribbon cable, harnesses and cable assemblies are rated for continuous service at 115°C, intermittent operation at 150°C and momentary exposure to 350°C.

Also shown will be flat ribbon cable and cable assemblies made of individual round conductors insulated with silicone rubber. Flat ribbon cable made with silicone rubber insulation retains its flexibilty from −60°C to +260°C and provides uniform insulation wall thickness with predictable, stable dielectric properties. Silicone rubber cable and cable assemblies meet the requirements of MIL-W-16878D, Type F. Spectra-Strip Corp., Garden Grove, Calif. See at IEEE Booth 1A11.

Circle No. 267 on Inquiry Card.



SCOPE PACK

A scope pack (called "SCOPAC") provides 50 dB filtering to 1 MHz and 0.25% regulation for oscilloscopes and CRT devices. Problems normally experienced in scope use such as pre-triggering, jumping off scale, false signals, jitter, zero level stabilization, and erroneous readings that are caused by line disturbances are virtually eliminated. This parametric device was specifically designed to operate Tektronix, Hewlett Packard, Dumont, and other oscilloscope and CRT devices.

Designated Model P-TEK, the unit is attractively packaged and is compatible with all scope usage. Wanlass Instruments, Santa Ana, Calif. See at IEEE Booths 4D11 and 4D13.

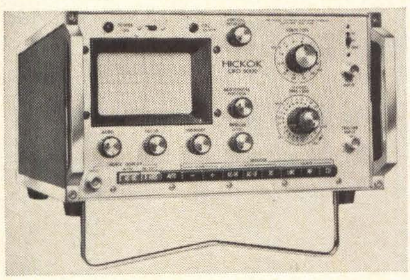
Circle No. 254 on Inquiry Card.

ANALOG/HYBRID COMPUTER

The 380 Analog/Hybrid Computing System is a ten-volt computing system with the capability of expanding from 10 to 50 amplifiers. Parallel logic may be added as well as a data interface to a digital computer. It is ideally suited to undergraduate instruction. In expanded configuration, the 380 can be used to teach or implement modern hydrid techniques necessary to study the dynamics of physical systems too complex for simplified analytical models. Very importantly, the 380 offers the advantage of direct interaction between the investigator and the system.

Also on display will be the EAI 1125, 1131 and 1140 VARIPLOTTERS®, a high speed repetitive operation display unit, and the EAI 8870 two-channel strip chart recorder. Electronic Associates, Inc., W. Long Branch, N.J. See at IEEE Booths 2D32-2D36.

Circle No. 268 on Inquiry Card.



ALL SOLID-STATE OSCILLOSCOPE

Model CRO 5000 25 MHz oscilloscope features an all-solid-state design and bandwidth of dc to 25 MHz to 3 dB down point. Response above 25 MHz is essentially Gaussian for optimum pulse reproduction and it is usable to 50 MHz.

A built-in vertical delay line permits viewing of the leading edge of pulse displays when triggered internally, providing nearly 50 ns of baseline prior to start of the pulse display. Vertical sensitivity is 10 mV per division with 12 calibrated sensitivity steps, from 10 mV per division to 50 V per division.

Twenty-four calibrated sweep ranges are provided, from 50 ns per division to 2 sec per division, with continuously variable sweep speeds between ranges. Accuracy is 3.0%. Horizontal amplifier response is dc to over 5 MHz. The instrument measures 11¼" w x 6⅞" h x 19" d and weighs 24 pounds. Hickok Electrical Instrument Co., Cleveland, Ohio. See at IEEE Booths 2C18-2C20, 2C25-2C27.

Circle No. 260 on Inquiry Card.

IEEE PRODUCTS

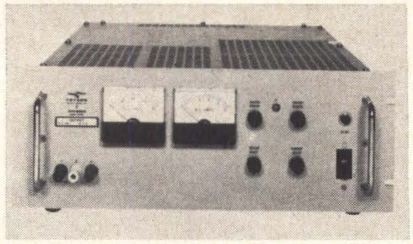
DATA SET

A data modem capable of transmitting and receiving serialized digital data at 2000 bits per second over the switched direct distance dialing (DDD) network is electrically and functionally identical to the Western Electric 201A and can be readily incorporated into communication facilities containing the WE equipment. No modifications are required.

The T201A interfaces with Western Electric 804A data sets in installations requiring alternate voice/data communications. This arrangement also provides automatic answer and control functions, and compatibility with Western Electric 801A and 801C automatic call units.

Two versions of the T201A are available. The T201A3 has an internal crystal-controlled clock for controlling the data flow. The T201A4 is used in applications where the timing signal is provided by a business machine. Sangamo Electric Co., Springfield, Ill. See at IEEE Booths 2C26-2C28.

Circle No. 237 on Inquiry Card.

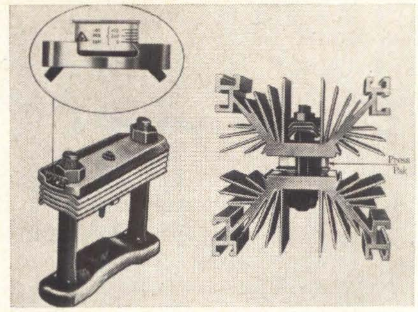


WIDE RANGE POWER SUPPLY

Model M7C160-15 is a 0-160 Vdc, 0-15 A, highly regulated power supply in a 7-inch panel height. This power supply, as do all models of the Super-Mercury series, features all-silicon design, full-programmable, constant voltage/constant current and precision performance. Other Super-Mercury units are available up to 100 A in panel heights from $3\frac{1}{2}''$ to 7" with provisions for slide rack mounting.

Other features include: 0.005% regulation, 0.015% stability; full power to 60°C without derating; ripple less than 1 mVrms; automatic load share paralleling; master slave tracking; mil spec performance to vibration, shock, line voltage, EMI. Trygon Electronics, Inc., Roosevelt, N.Y. See at IEEE Booths 2H47-2H49.

Circle No. 264 on Inquiry Card.

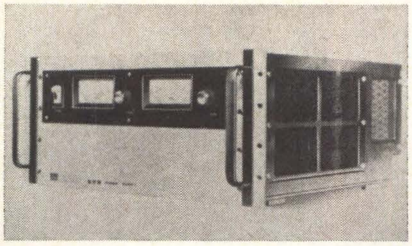


HEAT SINK/CLAMP

A line of heat sink clamps for press-pak SCRs will handle SCRs up to 2.25" in diameter. Uniform contact pressure is provided for needed parallelism and centering accuracy. An optional force indicator reads in "lbs./leaf," and the clamp assembly may be ordered with 2, 3, 4 or 5 leaves for maximum clamping forces of 800, 1200, 1600, or 2000 lbs. respectively. U-clamp insulation rated at 5000V ac.

Five styles of extruded heat sinks are available. These include standard bolt size T-slots for mechanical and electrical mounting of busswork or supports. Wakefield Engineering Inc., Wakefield, Mass. See at IEEE Booth 4B06.

Circle No. 256 on Inquiry Card.

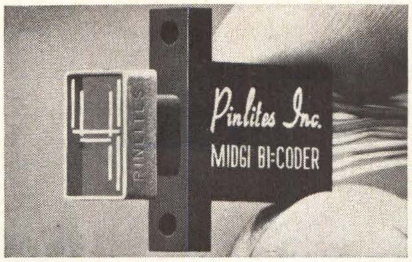


POWER SUPPLIES

Three 10,000 watt constant-current, constant-voltage power supplies, each measuring 12½" high by 20" deep by 19" wide, include Model SCR 40-250, rated 250 A at 40 V adjustable to zero volts; Model SCR50-200, 200 A at 0-50 V; and Model SCR100-100, 100 A at 0-100 V. Inputs for all three are 208, 220 or 480 V, delta or wye connected, 60 Hz. Efficiency is 75%.

Voltage regulation is 0.1% against line-to-line input voltage variations of ±10% and full-load to no-load or no-load to full-load step changes anywhere within the current range. In the constant current mode, regulation is 0.1% against input voltage variations of ±10% and step changes in load. Electronic Measurements, Div. of Rowan Industries, Oceanport, N.J. See at IEEE Booth 2D44.

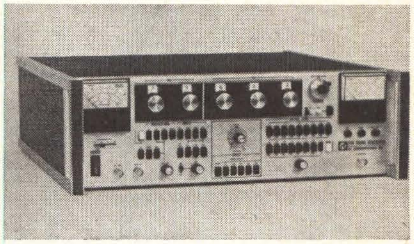
Circle No. 261 on Inquiry Card.



DIGITAL READOUT DISPLAYS

Midgi-Lite, a direct viewing, seven segment, digital readout, has displayed characters formed by incandescent tungsten filaments or light bars, and is voltage controllable over a wide range of brightness. The design life of the filaments is 100,000 hours. Within one display head, two electrically/mechanically separate sets of seven light bars, are concentrically arranged for two character sizes: primary size 5/16", secondary size ¼". Both sets of filaments are uniplane for maximum viewing angle, and parallel filaments are sufficiently separated for immediate indication of mode failure. The display head is an all hermetic, ceramic, metal, glass package. Pinlites Inc., Fairfield, N.J. See at IEEE Show Booths 3B22-3B23.

Circle No. 213 on Inquiry Card.



SIGNAL GENERATOR

The RF-808 Signal Generator is a synthesizer and a sweeper in addition to a standard signal generator which covers the frequency range of .05 to 80 MHz. The unit features full remote programmability, high signal power output, FM, AM, automatic sweep, and manual sweep.

The generator covers its frequency range in synthesized 1-kilohertz steps and a vernier may be calibrated to 1 Hz accuracy to obtain frequencies between the 1 kHz steps. Output amplitude is adjustable from 0.1 μV to 10 V rms into 50 ohms. RF output is automatically leveled over the entire frequency range. Stability is 5 parts in 10^{-9} per day or 1.25 parts in 10^{-7} per month. R F Communications Inc., Rochester, N.Y. See at IEEE Booth 2C01.

Circle No. 252 on Inquiry Card.

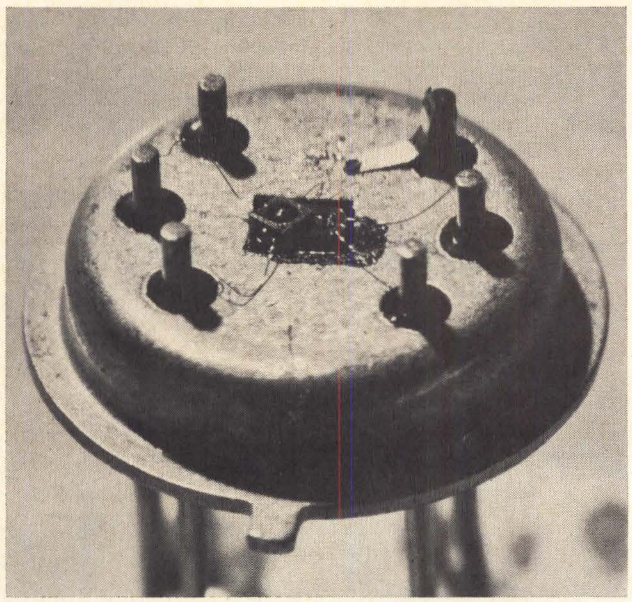
Solid-State Isolators for Low-Power Relay and Transformer Replacement

TEXAS INSTRUMENTS, INC.
Dallas, Texas

Two high-gain, optically coupled isolators capable of replacing low-power relays and transformers have been announced by Texas Instruments Inc., Dallas, Texas. These solid-state optoelectronic coupling devices have no moving parts or fragile wiring, and offer operating speeds three orders of magnitude faster than their mechanical counterparts.

Designated TIXL102 and TIXL103, the devices provide electrical isolation of ± 100V, internal resistance greater than 10^{12} ohms, and a capacitance of 4pF, all resulting in excellent signal-to-noise performance.

High, typical overall current gains are 0.6 for the TIXL102 and 1.4 for the TIXL103. Both devices are packaged in 6-lead TO-5 metal cans.



Isolator Characteristics

Functionally, optically coupled isolators are similar to relays and transformers in that they offer a pair of input and output terminals having a high degree of electrical isolation. Instead of using a magnetic field for signal transfer, however, these devices operate through internal light coupling.

An important advantage of optically coupled isolators over transformer counterparts is their lower frequency response which extends to dc. This feature makes isolators practical for operation as dc relays or isolation switches. The linearity of response to input cur-

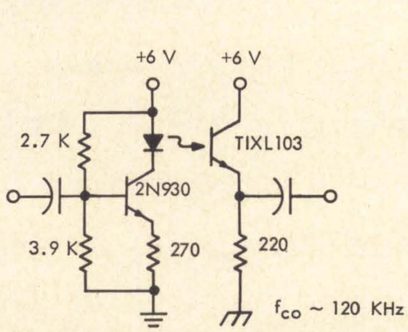


Fig. 1 Isolation amplifier.

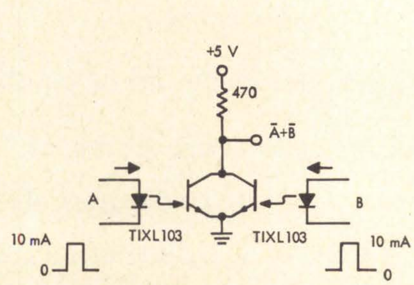


Fig. 2 Isolators in a NOR gate.

rent also makes these devices applicable to linear circuits. Besides the ordinary applications as replacements for relays and transformers, optically coupled isolators benefit new designs as subsystem coupling elements to avoid noise generation with common ground connections.

Applications

Usually the advantages of optically coupled isolators represent more than the replacement of a relay or transformer, since considerable other circuity is often eliminated. This is the case for TIXL102 and TIXL103 high-gain isolators when used in applications such as high-performance voltage regulators, sub-system couplers and actuator switches, and in various logic arrangements.

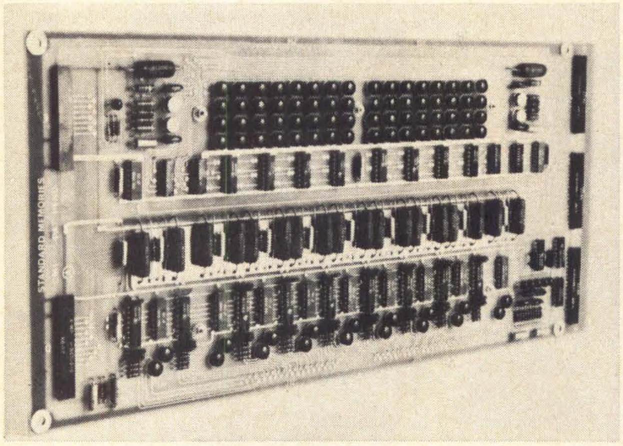
The circuit in Fig. 1 is an example of a 120 KHz amplifier. With this circuit, a complex voltage-level shifting circuit is not needed in coupling two circuits having a varying difference in ground potentials. An additional benefit of using the isolator is a significant reduction in the spurious noise resulting from the floating ground arrangement. Previously, a large, bulky transformer was required for coupling low frequencies between the two sub-systems while maintaining voltage isolation. Even then, the lower frequency response was limited to a value in the range of tens of Hertz. The response of the isolator in Fig. 1 is dc; thus the lower limit is restricted only by the capacitors. Actually, even dc coupling could be obtained, if desired.

An example of optically coupled isolator use where logic gates must receive their inputs from several different subsystems of peripheral equipment is shown in Fig. 2. Connection of the signal grounds from two sub-systems, which could result in ground loop noise, is avoided in this arrangement. Inputs A and B have separate, isolated input tie-points.

The devices are available in evaluation quantities and are priced at $40.00 for the TIXL102 and $75.00 for the TIXL103 in 100-piece quantities. See at IEEE Booths 2F08-2F20.

For additional information, circle no. 199 on inquiry card

NEW PRODUCTS



SINGLE PC BOARD MEMORY SYSTEM

A low-cost, random access core memory system, ECOM-S, fully contained on a single pc board, offers capacities from 128 words x 9-bits to 256 words x 18 bits and operates in either the read-only/write-only mode at 2.0 μs or in the read-restore/clear-write mode at 4.0 μs. Access time is 0.9 μs max.

Addressing is in 8-bit binary level (dual rail) format. Specified input levels are: Logic 1, +2.5 V to +5.5 V; Logic 0, −0.5 V to +1.0 V; Loading, 2 DTL or TTL loads max. Output levels are: Logic 1, +4.5 V nominal; Logic 0, 0 V nominal; Loading, 6 DTL or TTL loads max. The operating temperature range of the memory is from 0° C to +50° C. Standard Memories, Inc., Sherman Oaks, Calif.

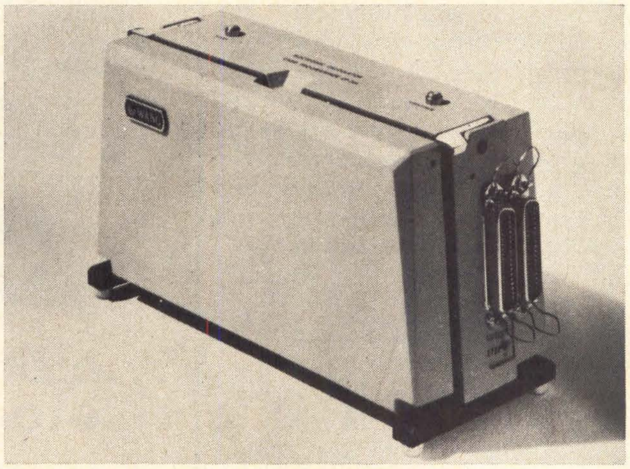
Circle No. 200 on Inquiry Card.

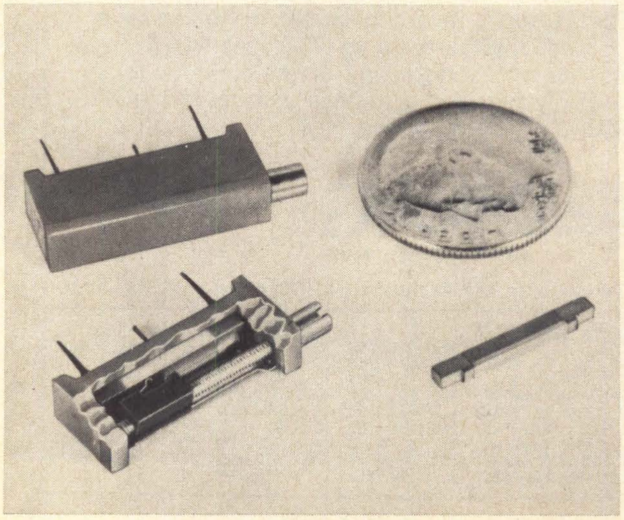
CARD PROGRAMMER

A card programmer, Model CP-2, has been offered as a plug-in accessory for all Wang calculators. The new device makes use of pre-scored IBM tab cards, which can be punched by hand with a pencil or paper clip. To prepare his own unique programs, the user performs the desired calculations on his keyboard and writes down the sequence of keystrokes. He then looks up the punched card code corresponding to a keystroke, marks the card, and repeats this for each key operation required.

The programmer handles programs of up to 80 steps. Program codes are provided to allow the calculator to test itself for the desired answer. Based on the test results, the program jumps to the desired new sequence of steps on the same tab card, or in a card in another reader. Wang Laboratories, Inc., Tewksbury, Mass. See at IEEE Show Booths 2B16-2B20.

Circle No. 203 on Inquiry Card.





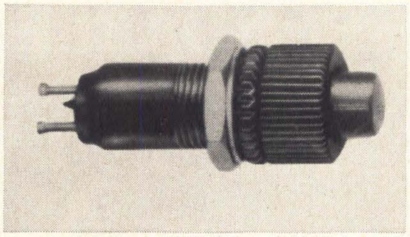
RECTANGULAR FILM-MET TRIMMER

A 3/4" rectangular "Film-Met"(TM) trimming potentiometer, offering infinite resolution and superior electrical performance over trimming ranges of from 10 ohms through 20K, features Amphenol's patented Film-Met resistance element, a metal film deposited on a dimensionally stable ceramic substrate. Characteristics of Film-Met result in infinite resolution as well as low CRV—two percent of RT or 20 ohms, whichever is greater.

The 3811 will operate over an ambient temperature range of −55° C through +125° C (−85° F to +257° F) and is humidity-proof. It has a rotational life of 200 cycles minimum. The temperature co-efficient is a low 100 ppm/degree C maximum with 50 ppm/degree C available upon request. Amphenol Controls Div. The Bunker-Ramo Corp., Janesville, Wisc.

Circle No. 201 on Inquiry Card.

NEW PRODUCTS



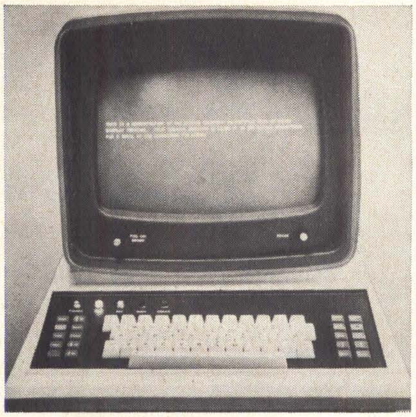
CARTRIDGE LAMPS

To meet a variety of commercial and military applications involving both incandescent and neon type lighting, Eldema is offering a series of C-Lite cartridge lamps and mating D-holders, designed to suit a variety of applications, including those meeting specifications of MIL-L3661.

Built to be relamped from the front of the panel, D-holders feature anodized housing and nickel plated hardware, and are available in RFI/EMI-shielded configurations.

Designed to fit the appropriate D-holders, the C-lite lamp cartridges are constructed with aluminum cases, stainless steel pins, and plastic lens caps. C-lite units are available with built-in resistors for applications utilizing neon lighting. Voltages for incandescent C-lites range from 1.35 to 120 V. Eldema, Compton, Calif.

Circle No. 214 on Inquiry Card.



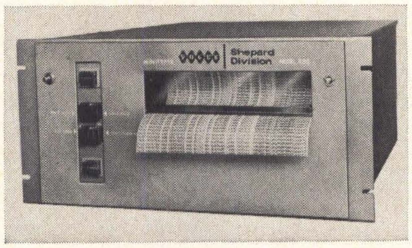
KEYBOARD DISPLAY

A keyboard display terminal, the VT03, operates similarly to a conventional teleprinter and incorporates "carriage return" and "line feed" characters for position control. It is virtually noiseless and accepts data at the rate of 1200 baud.

The full-duplex console features a local memory for display refreshing thus eliminating the demand on processor time usually required for this function. The VT03 displays up to 960 characters arranged in 12 rows of 80 characters each.

Among others, the display unit features an alphanumeric keyboard, editing capability from the keyboard or computer, audible end-of-line and incoming message tones and plug-in boards for easy maintenance. Digital Equipment Corp., Maynard, Mass.

Circle No. 211 on Inquiry Card.

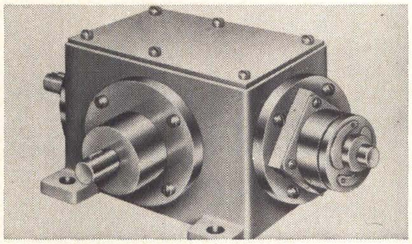


HIGH SPEED MINITYPER

A high speed printer, Model 880, has a 64 character font, and is capable of 20 L.P.S. alphanumerics, 40 L.P.S. numerics with up to 80 columns, completely buffered. It consists of 2 drawers, each 8¾"h x 19"w x 22"d whose combined weight is 135 lbs.

The printing mechanism, paper feed, and paper supply assemblies are constructed on a front opening drawer chassis. Shepard Div., Vogue Instrument Corp., Summit, N.J.

Circle No. 202 on Inquiry Card.



HIGH SPEED REVERSING DRIVE

Electromagnetic actuated reversing drive units for positive control of rotary motion allow for positive positioning and holding, clutching and braking, indexing, jogging, searching and random access. Units are available in various physical configurations of input and output shafts, have totally enclosed housing with precision sealed ballbearings and come in the following voltages; 3,6,12 and 24/28 Vdc. Electroid Co., Union, N.J.

Circle No. 204 on Inquiry Card.

You probably aren't our kind of engineer.

No offense intended. We just know what we want.

We're computer memory specialists. If you know our products, you know we're good.

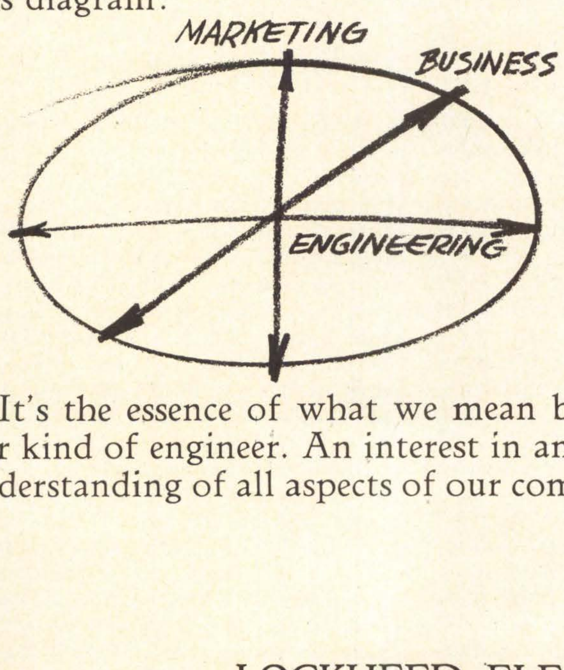
Not surprisingly, we're growing fast.

So we need engineers. Good minds. Good technical backgrounds. But that's not all.

You see, back when we were small we learned an important lesson. Each of our engineers had to get involved in everything: research, design, costing, marketing, production – you name it. Being involved, they became committed. And worked better for it.

That's how we got our reputation for doing what we do better than anyone else. We intend to keep it.

That's why we take such a close look at all applicants for our engineering positions. We'll talk to you about interests and aspirations and experience. And, at some point along the line, we'll draw this diagram:



It's the essence of what we mean by our kind of engineer. An interest in and understanding of all aspects of our company's activities. You could call it balance. Whatever it is, it works for us.

* * *

What can we offer you?

First, a good salary. (We want the best and we're willing to pay for it.) Second, the opportunity to advance rapidly along either engineering or administrative lines. (Lots of outfits will tell you this, then stick you in an isolation ward. We mean what we say.) Third, the opportunity to grow with the best engineering staff in the industry. Fourth, the satisfaction and pride of seeing the products you work on produced and sold.

* * *

We make memory systems and stacks and planes and printed circuits. We're looking to the future with research in plated wire and films. And we're in the process of introducing a brand new product: MAC 16, a compact, inexpensive Multi-Application Computer. Our division is going to keep right on growing. And we'll need even more of our kind of engineers.

If we sound like your kind of company and if you have an M.E. or E.E. degree and computer-related experience, let's get together.

Write me a letter: Mr. E. B. Gage, 6201 E. Randolph Street, Los Angeles, California 90022. Or, call me collect at (213) 722-6810.

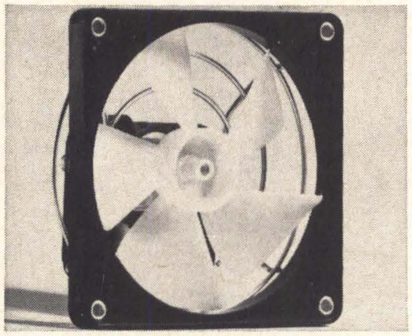
Naturally, we're an equal opportunity employer.

LOCKHEED ELECTRONICS COMPANY

Data Products Division • Lockheed Aircraft Corporation

CIRCLE NO. 901 ON INQUIRY CARD

NEW PRODUCTS

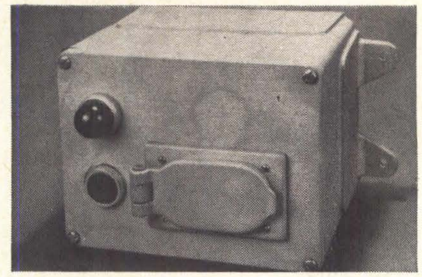


AXIAL FAN

A key feature of the SK4251 miniature axial fan is the efficient fan blade design coupled with a superior impedance protected motor. The fan blades are molded of Celcon, a high strength acetal resin. With a free air delivery of 115 cfm, this unit can be expected to run continuously for a minimum of 5 years without maintenance, when operated at maximum ambient temperatures of 125° F in clean atmosphere.

Designed for 115 V, 50/60 Hz, single phase operation, the motor design provides excellent low voltage starting characteristics, quieter operation and a smoother static pressure versus cfm curve. Ripley Co., Inc, Middletown, Conn.

Circle No. 219 on Inquiry Card.



ALL-WEATHER CARD READER

A card reader, protected by a rugged cast-aluminum housing with provisions for air purging, has a spring-loaded door that protects the card-entry slot against water entry during rain or conditions of forced spray.

The mechanism is solenoid operated with electrical and mechanical interlocks to ensure correct card positioning and read head closure. After the card has been fully inserted, the read head mechanism automatically operates to provide output data within 100 ms. The unit has a push-button card release for local operation, or may be remotely or automatically controlled.

Sensing up to 264 data bits, the reader accepts several types of plastic credit or badge type cards. The sensing contacts exhibit less than 100 mΩ resistance and feature a double wiping action. Contact rating is 250 mA with a dc resistive load. Pin-to-pin capacitance is less than 5 pF and the insulation resistance is greater than 10,000 MΩ. AMP Inc., Harrisburg, Penn.

Circle No. 208 on Inquiry Card.

HYBRID ICS

Type LDS210, packaged in a LID case, is designed primarily for use as a medium current switch and core driver. It is an extremely versatile device, functionally replacing JEDEC types 2N2476, 2N2477, 2N3252, 2N2554, 2N3724, 2N4013 and 2N5188. Primary electrical characteristics include: Polarity, NPN; I_C range, 100-500mA; V_{CEO}, 30V; h_{FE}, 30 (minimum); I_c, 300 mA; f_t, 200 mHz; t_{on}, 15ns; t_{off}, 50 ns.

Type LDS207 is basically designed for use as a low on-resistance switch in digital to analog circuits. Primary electrical characteristics include: Polarity, NPN; V_{CEO}, 5V; h_{FE}, 50 (minimum); I_C for h_{FE}, .03mA; R_{ec} (on), 4 ohms (maximum); I_B for R_{ec} (on), 1mA. Amperex Electronic Corp., Semiconductor and Microcircuits Div., Slatersville, R. I.

Circle No. 230 on Inquiry Card.

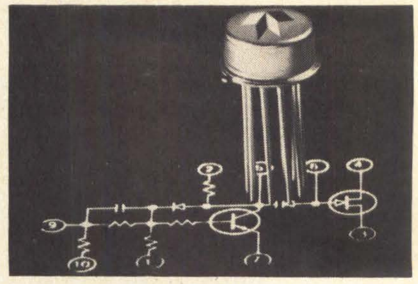
OPERATIONAL AMPLIFIER

The LM107 offers the same input current specification advantages of the recently introduced LM101A, but with the necessary frequency compensation built into the chip. The LM107, like the LM101A, has a guaranteed bias current of 100nA and offset current of 20nA over the full military temperature range. These advantages have been accomplished with no sacrifice in drift or offset voltage. Offset voltages of 3mV, offset voltage drifts of 15uV/°C are also guaranteed over the military temperature range.

The LM107 is a plug in replacement for the 709, LM101, LM101A and the 741. The low input currents make it well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform generators. National Semiconductor Corp., Santa Clara, Calif.

Circle No. 231 on Inquiry Card.

NEW PRODUCTS

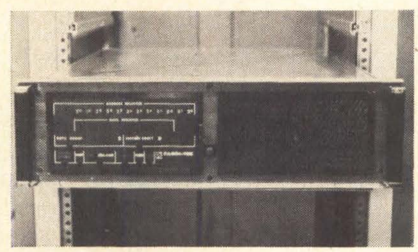


FET ANALOG GATES

CAGIO SPST FET switch hybrid ICs, designed for analog gating, feature turn-on and turn-off times of 50 nanoseconds maximum. Other performance features include 30 ohms maximum on-resistance, zero offset voltage, and direct operation from DTL or TTL logic. The package is a low profile TO-5.

This hybrid microcircuit uses all military grade semiconductors. All active semiconductors are preconditioned in chip form to ensure reliable operation over full military temperature ranges. Crystalonics, a Teledyne Company, Cambridge, Mass.

Circle No. 215 on Inquiry Card.

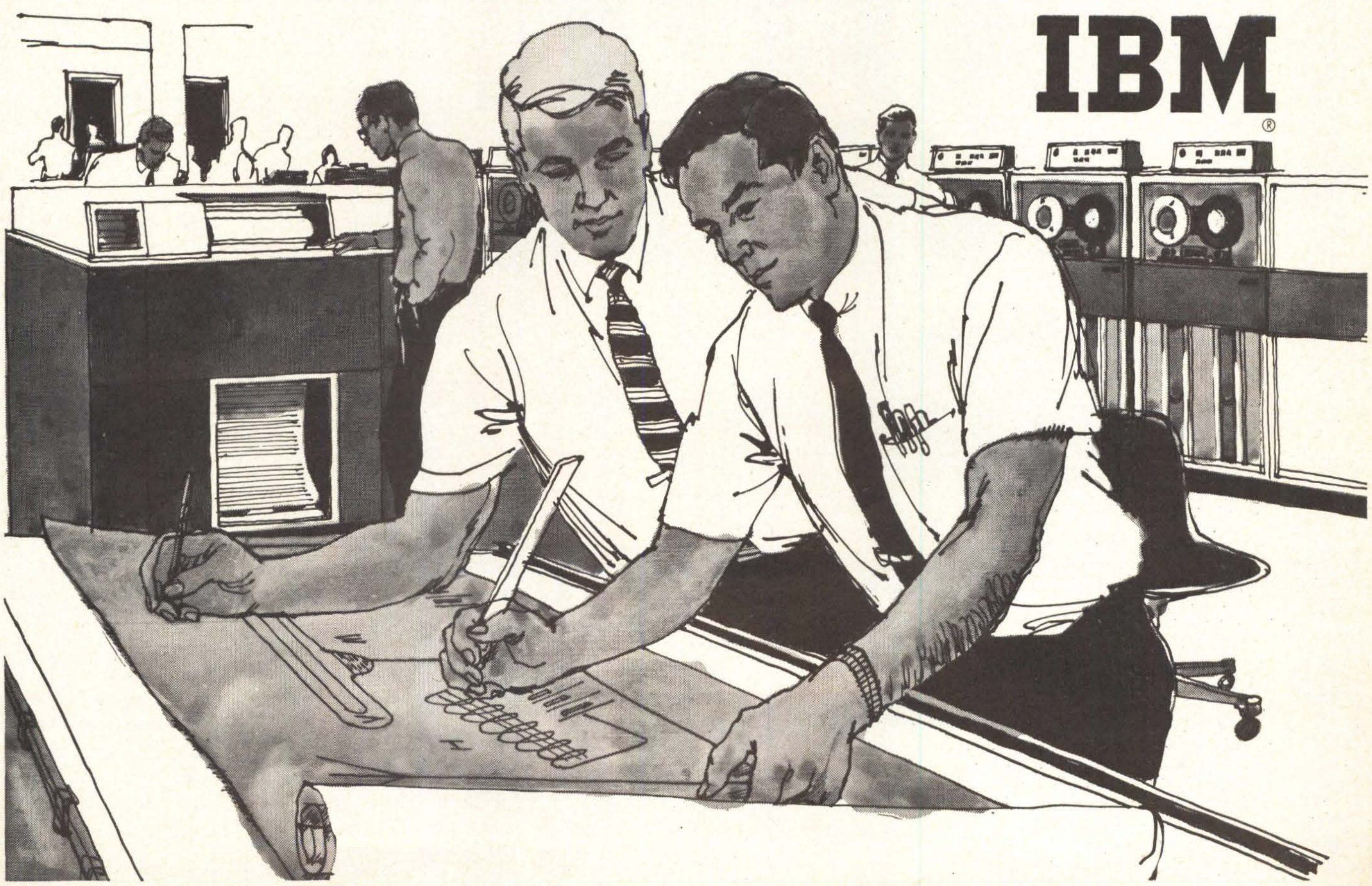


CORE MEMORY SYSTEM

The 370 Memory offers high speed with modularly expandable storage capacity. Basic module sizes are 1K to 4K by 40 bits, with expandable capacities of up to 655,360 bits. The 370 System offers three full-cycle memory speeds of 750 ns, 1 μs and 1.5 μs. Access times are 325 ns, 350 ns and 400 ns, respectively. The unit offers the following modes as standard: full cycle, half cycle, and split cycle. All sub-assemblies, including stacks, are pluggable. Inter-face circuits are compatible with a wide range of interface logic levels.

The 370 measures 5¼″ high by 20″ deep with power supply and mounts in a standard RETMA relay rack. Fabri-Tek Inc., Minneapolis, Minn.

Circle No. 210 on Inquiry Card.



NEW PRODUCTS

ACOUSTICAL COUPLER LINE

A line of acoustic/magnetic couplers, designated Telemate 300, connects a conventional telephone to a remote input/output terminal device.

Telemate 300 measures 3½ x 10 x 10½ inches and weighs 5½ pounds. Other specifications include: 300 Baud data rate; Carrier and power on/off signal indicator lights; Highly selective tuned oscillator circuitry; Half & full duplex switch; Triple tune circuitry; AGC circuitry; Acoustic isolation—minimum of 20 dB; Teletype on EIA interface.

Other options include a carrying case, originate/answer capability, a loudspeaker, RS232B capability and several different cable interface connections. Direct Access Computing Corp., Southfield, Mich.

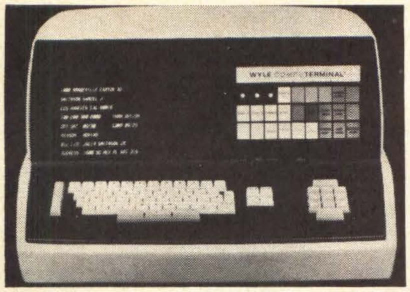
Circle No. 216 on Inquiry Card.

CAPACITORS

Type WFH, tantalum capacitors feature an etched tantalum foil anode with a neutral electrolyte and a glass-to-tantalum hermetic end seal. They are manufactured in ratings and sizes equal to MIL type CLR65, but have the electrical characteristics of MIL type CLR 25 units. The result is one line of capacitors with considerably higher voltage (up to 200 Vdc at 85°C) and capacitance ratings (up to 5600 μF than CLR65 or CSR 13 capacitors, They also have reverse voltage capability, contain a noncorrosive electrolyte, and are lighter in weight than CLR65 capacitors.

Eight case sizes are available. Type WFH capacitors have a corrosion-resistant metal case and operate efficiently over the full temperature range of −55°C to +85°C (or −55°C to +125°C at higher voltages). Tansitor Electronics, Inc., Bennington, Vermont.

Circle No. 236 on Inquiry Card.



DATA TERMINALS

The Model 600 Computerminal offers a unique combination of features, including large CRT character size total capacity of 1,024 displayable characters, and a special feature which permits the operator to concentrate on any 32-character by 8-line segment of the total display by rolling the display up and down like paper in a typewriter. Another important feature is direct natural conversation communications between the operator and the computer.

The Computerminal incorporates a complete core-type memory and hardwired controller instruction set to allow independent multi-terminal operation on a common dedicated line, a multi-element display with flicker-free operation, and a standard typewriter configuration keyboard plus special-function keys for input of information. Wyle Laboratories, El Segundo, Calif.

Circle No. 209 on Inquiry Card.

COMMUNICATIONS TERMINAL

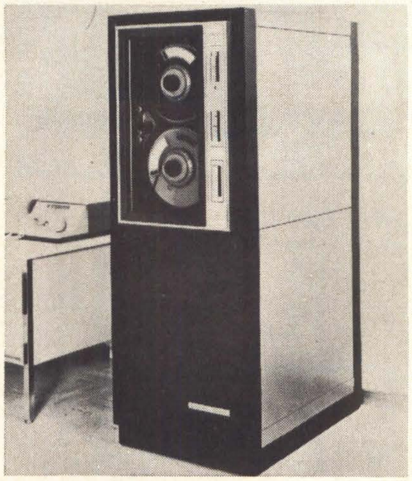
The new terminal, the DCT-132 data communications terminal is capable of interfacing with a dial-up switched network, or with a dedicated line, sending and receiving data at 2000 to 4800 bits per second.

When the DCT-132 is configured as a communication line concentrator, the capability of the unit is limited only by the quantity and speed of the communication lines connected. Up to 32 low speed (110 bits per second or less) asynchronous communication lines can be concentrated into one 4800-bit-per-second synchronous communication line.

Medium speed (up to 1200 bits per second) asynchronous communication lines as well as high speed (up to 2400 bits per second) synchronous communication lines can also be concentrated to significantly reduce communication line costs in most communication systems. Scientific Control Corp., Dallas, Texas.

Circle No. 229 on Inquiry Card.

NEW PRODUCTS



COMMUNICATIONS TERMINAL

Computer compatible System 4031 magnetic tape terminal provides point-to-point data communications at speeds of 1200 words per minute serially or 600/720 words per minute in a parallel format over ordinary telephone lines. It is completely compatable with all other Tally send and receive terminals in any given transmission network. Recording densities of 200, 556, or 800 characters per inch in 7 track format or 800 characters per inch in 9 track format are offered.

Features include automatic error detection and retransmission and unattended answering capability. Tally Corp., Seattle, Wash.

Circle No. 212 on Inquiry Card.

DC POWER SUPPLIES

QSA Series dc power supplies provide voltage regulation of ±0.005% for line and load changes combined, low ripple of 300 μV rms, (3 μV p-p), and maximum drift of 0.025% for an eight hour period. Output voltages cover the range from 0 to 330 Vdc at power levels to 300 watts. Ten μs crowbar overvoltage protection is available for all models.

The units are thermally protected with an operating temperature range of −20° C to +71° C and are short circuit proof. Remote sensing and remote programming by resistance and voltage are possible. Raytheon Co., Sorensen Operation, Norwalk, Conn.

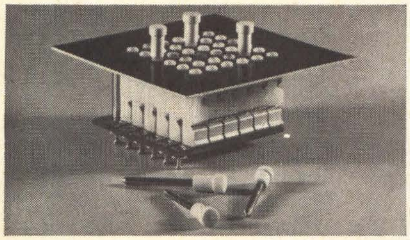
Circle No. 239 on Inquiry Card.

RESISTOR KIT

A kit of chip resistors prepackaged with a selection of forty resistance values contains a total of 400 resistors, ten chips of each of the forty values which range from 56 ohms to 100 kilohms.

The kit concept permits prototyping of microcircuits within the dimensions of the completed system and eliminates the need for using discrete resistors. Mepco, Inc., Morristown, N.J.

Circle No. 233 on Inquiry Card.



CROSSPOINT PROGRAMMER

A modular crosspoint programming system allows almost any X-Y size with its standard two-layer construction. In addition, as many as ten decks can be utilized with up to three circuit paths for each contact position. The design insures that the contact springs only conduct electrical current since the pins are guided by the precision-molded module.

Color coding can be provided as an aid in programming. The modules themselves are individually color coded in your choice of eight colors, arranged to your specifications. MAC Panel Co., High Point, N.C.

Circle No. 218 on Inquiry Card.

DC TACHOMETER GENERATOR

The E-590, a dc tachometer-generator is housed in a size 20 frame and weighs one pound. Windings are available to provide outputs of 7, 15, and 21 V per 1000 rpm. Nominal linearity is 0.2% maximum divergence from true velocity/voltage proportionality. When properly terminated, a thermal compensation network provides an overall temperature coefficient of less than .05% per °C. The peak-to-peak ac ripple component in the generator output is better than 4%, unfiltered. When observed on an rms meter, total ac ripple is less than 1% at any speed from 100 rpm to 5000 rpm. Electro-Craft Corp., Hopkins, Minn.

Circle No. 234 on Inquiry Card.

NEW PRODUCTS

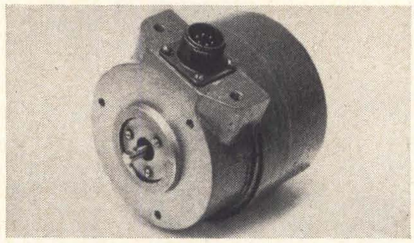
MAG TAPE RECORDER

A portable cartridge-loaded incremental recorder, Model 12-358, incorporates a unique new concept in cartridge load performance which maintains tension in the unloaded condition and advanced design techniques to produce high performance recording.

The seven or nine track unit weighs less than 40 lbs. and measures $10\frac{1}{2}$ x $7\frac{1}{2}$ x 22 inches. The cartridge accommodates standard IBM $8\frac{1}{2}$ inch reels with 1200 feet of $1\frac{1}{2}$ mil computer tape.

Other features include: Format, IBM Compatible NRZI; packing density, 200 or 556 bpi (write only) $\pm 5\%$; write speed, 0 to 500 steps per second; Slew Rate, 10.0 ips @ 200 bpi, 3.6 ips @ 556 bpi. Data Div., Genisco Technology Corp., Compton, Calif.

Circle No. 232 on Inquiry Card.



PULSE GENERATOR

Model 8609 pulse generator features a heavy duty base and housing along with seals on the shaft and housing to afford maximum protection where oil mist, dirt and other contaminates normally are present.

The 8609 is available with any standard pulse rate up to 1000 ppr single channel or with quadrature output for direction sensing. It may be obtained with or without shaping electronics. Typical applications would be as a measuring device to determine shaft speed, length controllers, on lead screws for x-y measurement and other similar applications. W. & L. E. Gurley, A Teledyne Company, Troy, N.Y.

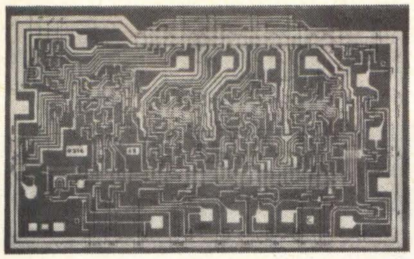
Circle No. 207 on Inquiry Card.

PHOTO-SCR

A series of low-cost photo-SCR's (RTPCO501) specified for operation over the military temperature range of $-55°C$ to $+125°C$ features very high light sensitivity of 20 fc typical without the need for a focusing lens. The flat lens permits wide angular response and lends itself more readily to fiber-optic light coupling schemes.

Five types are available with peak off-state voltages ranging from 15 to 200V. All types handle up to 300 mA of dc current. The series features silicon-planar die construction and typical dv/dt of 50V per microsecond. Transitron Electronic Corp., Wakefield, Mass.

Circle No. 220 on Inquiry Card.

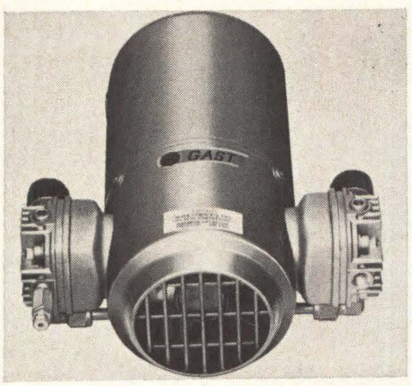


CCSI MSI COUNTERS

Two 4-bit counters, the 9310 BCD decade counter and the 9316 binary hexidecimal counter, can be used in multistage operations without external logic or degradation in speed over a single stage. They feature synchronous gated parallel entry and built-in look ahead logic to allow expansion to seven stages. An asynchronous master reset is available to reset all stages, over-riding all other inputs.

Operation of the 9316 is identical to the 9310 except that the 9310 reaches terminal count and starts counting over again after ten clock pulses. Fairchild Semiconductor, Mt. View, Calif.

Circle No. 206 on Inquiry Card.



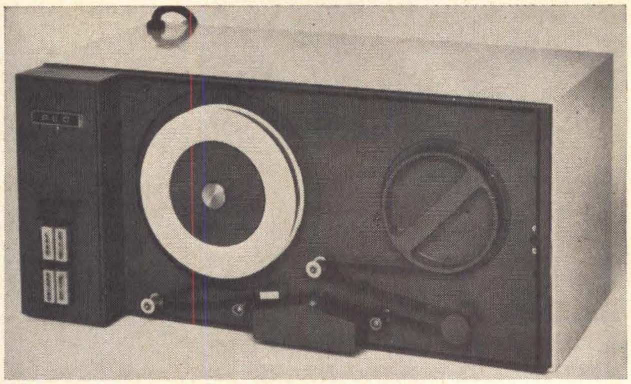
PISTON COMPRESSORS

A series of oil-less piston air compressors will deliver oil-free air at 100 psig for OEM and plant use. Five models range up to 4.65 cfm air flow. All units are motor-mounted and fan cooled. Sizes include single cylinder 1/6 hp and twin cylinder 1/4, 1/3, 1/2 and 3/4 hp motors.

Teflon® piston rings with lap joints maintain long-lived efficiency and Teflon rider rings on pistons eliminate metallic contact with cylinders. Corrosion resistant materials are used for all parts in contact with compressed air. Large ball bearings in connecting rod are greased for life and equipped with Teflon seals. Gast Manufacturing Corp., Benton Harbor, Mich.

Circle No. 217 on Inquiry Card.

NEW PRODUCTS

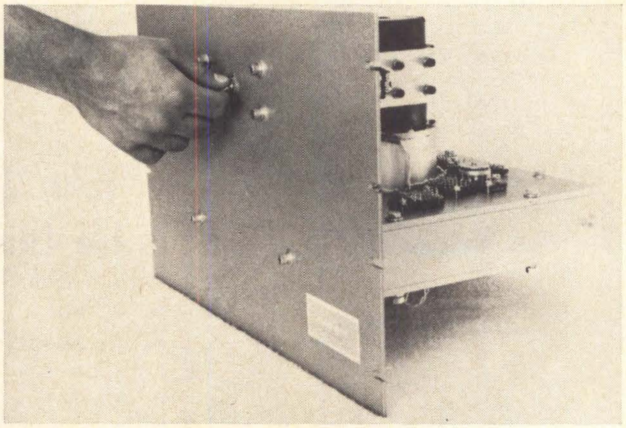


SMALL MAG TAPE TRANSPORT

A low-cost digital magnetic tape transport, model 7820, especially designed for small digital computer and data communication terminal applications, is an IBM compatible, 9 track, 12.5 ips, 800 bpi write/read transport, which provides data transfer rates of 10 kHz. Seven track operation and an erase head are available options.

The Model 7820 employs a single capstan velocity servo system which eliminates the pinch roller, a major source of skew and tape wear. The 7820 also saves on space, requiring only 8¾ inches of standard 19" rack height. It uses 7-inch reels, capable of storing 600 feet of magnetic tape. Peripheral Equipment Corp., Chatsworth, Calif.

Circle No. 225 on Inquiry Card.



DISC MEMORY SYSTEM

Model 10128 is a 128 track, 4 million bit disc memory that has an average access time of 8.4 ms. The 128 data heads are mounted in 16 independent 8-track head bars thus allowing 16 tracks to be read simultaneously. This results in a potential data transfer rate of up to 30 million bits per second. Typical values of write current and readback voltages are 125 mA and 20 mV, respectively. Mechanical features include a spindle-mounted plated disc, flexibly coupled to the drive motor. The read-write heads, actuated by an electro-mechanical head lifter, are located inside a sealed aluminum housing. The head lifter places into operating position—or retracts—all data, clock, and spare heads solely as a function of motor speed. Alpha Data, Inc., Tarzana, Calif.

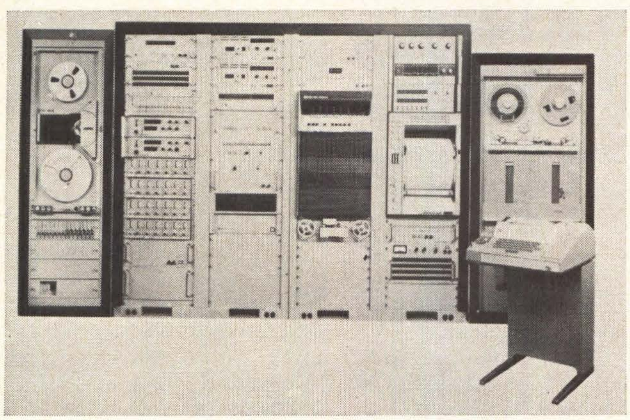
Circle No. 222 on Inquiry Card.

PORTABLE DATA COUPLER

The model 327 data coupler offers the ability to connect a data terminal via any convenient telephone handset to a time-sharing computer. Data terminals compatible with the coupler are various models of Teletypes, and terminals with an EIA communications interface, e.g., key-board printer terminals, card readers, plotters, CRT displays, etc.

The coupler features a high impact Royalite plastic alloy case and cover. Special electronic filtering and acoustic engineering have been incorporated to reject unwanted noise for error free operation. The Model 327 is available for originate only mode of operation. Standard features are half and full duplex operation, and a carrier-on indicating light. An optional circuit monitor speaker is also available. Data Communications Systems, Inc., Minneapolis, Minn.

Circle No. 226 on Inquiry Card.



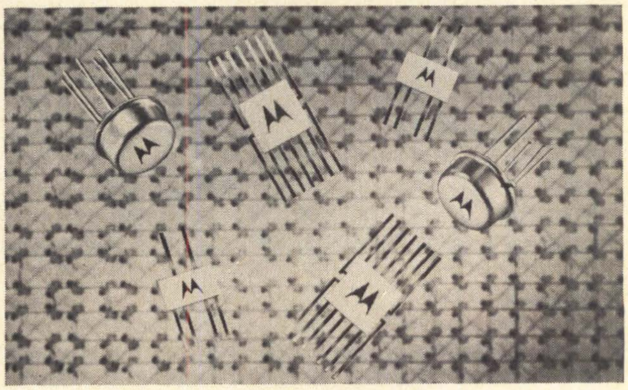
TELEMETRY PROCESSOR

The OMEGA IV, one of the Series 4024 telemetry systems, operates simultaneously on several frequency modulated and time-division-multiplexed inputs, with frequency responses totaling 100kHz. Synchronization and processing are accomplished with 100 kHz PAM inputs. Under complete program control for all functional parameters, including routing, subcarries discrimination, PAM/PDM synchronization, tape search and control, multiplexed sequencing, data compression, D-A addressing and oscillograph control, the system throughputs processed and identified data to magnetic tape and oscillograph recorders.

The system is completely automatic in operation and can be programmed using punched tape, magnetic tape, or input typewriter. Stellarmetrics, an Aydin Co., El Segundo, Calif.

Circle No. 228 on Inquiry Card.

NEW PRODUCTS



IC-COMPATIBLE PNP CORE DRIVERS

Six multiple core-driver transistors are multiple versions of the popular 2N3762 and 2N3467 fast, high-current PNP switches. Like the single transistors, the new devices have high current capability, low saturation voltage, low capacitance (11 pF C_{cb}) and extremely fast switching time (22 ns typical turn-on time, 46 ns turn-off time, at rated current). They are rated at 40 V V_{CEO}.

The MD3467 dual transistor, which is packaged in a TO-5 type case, the MD3467F dual, in a small 6-pin ceramic flat pack, and the MQ3467 quad in a standard 14-pin ceramic flat pack, are ½ A transistors. The TO-5 type cases can dissipate a total of 600 mW (500 mW maximum per transistor) at 25°C ambient temperature. The small flat-pack duals are rated at 350 mW total, 250 mW per transistor, and the 14-pin flat packs containing four transistors 500 mW total, 400 mW per transistor. Motorola Semiconductor Products Inc., Phoenix, Ariz.

Circle No. 227 on Inquiry Card.

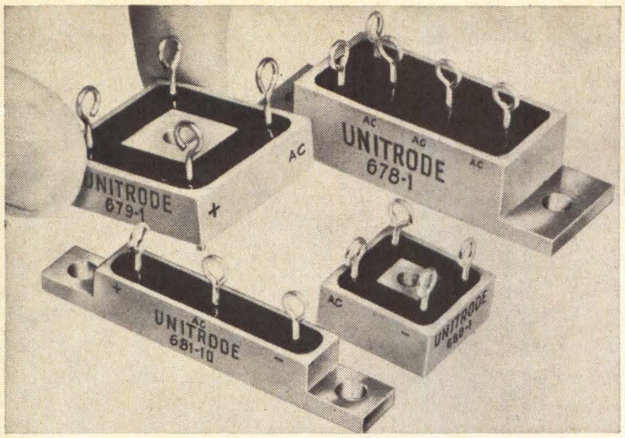
X-Y RECORDER ACCESSORY

A point plotter, Model 17012B, fits in place of the pen on the HP Model 7004A X-Y recorder (equipped with a Model 17173A null detector plug-in), and imprints up to 50 points per second. It prints a dot whenever the null detector senses that the X-Y recorder has moved the plotter to the next coordinate position specified by external equipment.

Point plotting is controlled by the null detector, which, when commanded by a seek pulse from external equipment, monitors the servo drive signals in the recorder and when these indicate that the plotter has reached the new data point (servo null reached) it activates the plotter. It then sends a plot completed signal to the external equipment, indicating that the recorder is ready for new instructions.

If the data point is off scale, in which case the servo drive signals do not reach a null, the Null Detector waits one second then plots a point anyway at the edge of the paper. This "forced" plot prevents the system from becoming stalled on off-scale data. Hewlett Packard Co., Palo Alto, Calif. See at IEEE Show Booths 2F25-2F26.

Circle No. 223 on Inquiry Card.

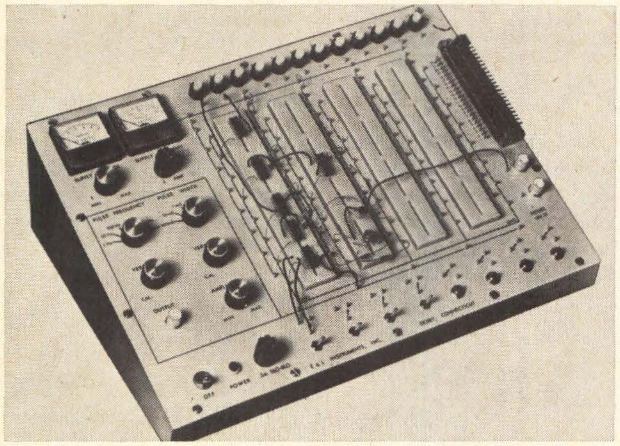


HIGH CURRENT RECTIFIER ASSEMBLIES

The MAGNUM series of miniature high-current controlled-avalanche rectifier assemblies has a PIV range of 100 to 600 V and includes 25 A single and three-phase bridges, 10 A single-phase bridges, and 15 A doublers and center-tap-rectifiers. The aluminum case is electrically insulated.

As in all Unitrode assemblies, only individually sealed, fused-in-glass, void-free diodes are used. The line is offered in two square and two rectangular configurations. Their max dimensions are: 2.25" x .350" x .375"; .750" x .750" x .240"; 1.125" x 1.125" x .328"; and 2.250" x .750" x .505". Unitrode Corp., Watertown, Mass. See at IEEE Show Booths 4H11-4H17.

Circle No. 224 on Inquiry Card.



DYNAMIC LOGIC BREADBOARD

Model LLB-32 contains in one compact, portable unit, everything needed to assemble and test experimental logic designs. The breadboard is completely self-contained, including a power supply, a pulse generator, indicator lights, switches and all necessary connectors (BNC, PC board, DIP).

The power supply is variable from 2 to 10 Vdc, has a maximum current capacity of 2 A, and offers a ripple of less than 50 mV. The pulse generator operates from 1 Hz to 1 MHz with a max amplitude of 6 V; pulse width is variable from 1 μs to 100 ms; rise and fall time is less than 100 ns; output impedance is 100 ohms. Twelve indicator lamps are provided (drivers included) and present an input impedance of 4.7 Kohms. The breadboard can accommodate 14, 16, or 24 pin dual-in-line modules as well as TO-5 packages. E&L Instruments, Inc., Derby, Conn.

Circle No. 221 on Inquiry Card.

LITERATURE

IC Single Point Annunciators

The single point system of integrated circuit annunciators is the subject of a two page bulletin. Deltron, Inc., Control Div., North Wales, Pa.

Circle No. 313 on Inquiry Card

Advanced Computer Software

A 4 page brochure describes the features and applications of the AUTOSCAN/LOG Software Package. Information General Corp., Woodland Hills, Calif.

Circle No. 324 on Inquiry Card

Power Supplies

A comprehensive 56-page catalog provides detailed specifications, prices and complete ordering information for over 300 models of power supplies. Lambda Electronics Corp., Melville, N. Y.

Circle No. 323 on Inquiry Card

Subminiature Pushbutton Switches

This data sheet lists all electrical and mechanical specifications for four subminiature monetary snap action pushbutton switches and includes outline drawings, recommended panel layouts and current price information. C&K Components, Inc., Watertown, Mass.

Circle No. 306 on Inquiry Card

Decode/Display Assemblies

Model D-103 decode display assemblies is the subject of a data sheet which includes applications, logic states, interfacing, mounting information and complete electrical specifications. Integrated Circuit Electronics, Inc., Waltham, Mass.

Circle No. 332 on Inquiry Card

Lab Data Processing Systems

A 20-page illustrated booklet describing the SpectroSystem 100/200 family of laboratory data processing systems provides a clear, concise description of computer-based systems that chemists can use to automate research and analytical laboratories. Varian Data Systems, Palo Alto, Calif.

Circle No. 314 on Inquiry Card

Serial Character Printer

This illustrated literature gives full information on the serial character printer, Model SCP-6A. Adtrol Electronics, Inc., Philadelphia, Pa.

Circle No. 317 on Inquiry Card

Motor-Generator Sets

Complete specifications and features of a motor-generator set with gearbox are provided in Brochure 4000-PDL-868, Kato Engineering Co., Mankato, Minn.

Circle No. 325 on Inquiry Card

Drum Memory System

A four-page brochure describes the CLC-1, a compact, low-cost ten-inch, rotating drum memory system with read/write and select electronics. Bryant Computer Products, Walled Lake, Mich.

Circle No. 327 on Inquiry Card

Poly Chip Transistors

A four-page folder provides complete specifications on a line of differential amplifiers, dual amplifiers, NPN/PNP complementary duals, and Darlington amplifiers. Raytheon Company, Semiconductor Operation, Mountain View, Calif.

Circle No. 315 on Inquiry Card

Transistors & Dice

A transistor and dice specification guide contains electrical specs, dice geometrics, substitution recommendations and carrier information on a line of silicon, planar, epitaxial unencapsulated transistors. National Semiconductor, Santa Clara, Calif.

Circle No. 326 on Inquiry Card

Digital/Analog Instruments

This six-page brochure gives examples of three system applications utilizing digital/analog instruments. Applications include a multichannel automatic scanner, jet engine test instrumentation and an automatic programmer. Anadex Instruments Inc., Van Nuys, Calif.

Circle No. 312 on Inquiry Card

Indicator Lights

Series 2900 GLO-DOT one-piece lens/body type indicator lights are described in this bulletin. Industrial Devices, Inc., Edgewater, N. J.

Circle No. 302 on Inquiry Card

Reed Switch Keyboards

Product Sheet 51RW lists the features, specifications, code assignments and ordering information for the 51RW2-1 reed keyboard. Micro Switch, a division of Honeywell, Freeport, Ill.

Circle No. 329 on Inquiry Card

MOS/LSI Integrated Circuits

A 44-page reference describes MOS/LSI integrated circuits and other recent MOS IC products. Illustrative charts and diagrams are included. Fairchild Semiconductor, Mountain View, Calif.

Circle No. 319 on Inquiry Card

Data Communications Systems

Two eight-page brochures detail actual situations of how data communication solves business problems by speeding order processing and invoicing, tightening inventory control, and making credit checking more accurate. Teletype Corp., Skokie, Ill.

Circle No. 308 on Inquiry Card

Designing Hybrid Microcircuits

A 12-page guide book "Designing Hybrid Microcircuits" describes circuit design philosophy, component compatibility, circuit characterization and test methods, packaging, and reliability. Circuit Technology Inc., Farmingdale, N. Y.

Circle No. 321 on Inquiry Card

Incremental Shaft Encoders

Modular design of Rotaswitch photoelectric and mercury-wetted type encoders are described in a two-page bulletin. Included are specifications and schematics of encoder components, prices, and typical mounting configurations. Disc Instruments, Inc., Santa Ana, Calif.

Circle No. 331 on Inquiry Card

IC Testing Techniques

This illustrated 8-page booklet discusses the economics of IC testing, the needs for logical and parametric testing, and the use of an analogical circuit test instrument. Teradyne, Inc., Boston, Mass.

Circle No. 316 on Inquiry Card

General Purpose Computer

This brochure features a discussion of small computers and describes the hardware, input, output, facilities, instruction set, and software for the NOVA general purpose computer. Data General Corp., Hudson, Mass.

Circle No. 307 on Inquiry Card

Remote Data Terminal

A six-page brochure describes the features and capabilities of the Computerminal,™ a remote data terminal, as well as the peripheral devices which have been designed to operate with it. Wyle Laboratories, El Segundo, Calif.

Circle No. 310 on Inquiry Card

Multiplexing Terminals

A 4 page bulletin describes the Model TDX time division multiplexing terminals and illustrates typical time-division multiplexing system configurations. Rixon Electronics, Inc., Silver Spring, Md.

Circle No. 303 on Inquiry Card

SCR Regulated Power Supplies

This bulletin gives complete and specific details on the technical features of silicon-controlled rectifier regulated dc (SCRDC) power supplies, and also presents performance characteristics and output voltage/current selection options. Sola Electric Div., Sola Industries, Elk Grove Village, Ill.

Circle No. 304 on Inquiry Card

Precision Potentiometers

This 4-page nonlinear function catalog sheet featuring a wide selection of single and multi-turn wirewound precision potentiometers in servo and bushing mount styles, provides a complete description of standard function capabilities, resistance ranges and conformity tolerances. Bourns, Inc., Trimpot Products Div., Riverside, Calif.

Circle No. 305 on Inquiry Card

High Speed TTL IC's

A comprehensive application guide to Series 5400/7400 high-speed TTL integrated circuits features various standard gate and flip-flop circuits and explains their basic operation. Sprague Electric Co., North Adams, Mass.

Circle No. 322 on Inquiry Card

Printed Circuit Connections

Catalog M400 shows a variety of printed circuit board "problem solvers"—versatile components that speed production and assembly of printed circuits. Molex Products Company, Downers Grove, Ill.

Circle No. 320 on Inquiry Card

Diced Chip Capacitors

Technical data and physical specifications on general purpose, temperature stable and by-pass and filtering ceramic chip capacitors are listed in Bulletin No. 689. American Lava Corp., Chattanooga, Tenn.

Circle No. 311 on Inquiry Card

Tubeaxial Fans

An illustrated 4-page catalog ET10 presents electrical and mechanical specifications, performance curves, dimensions, and wiring data for a full line of slim-profile tubeaxial fans. IMC Magnetics Corp., Westburg, N. Y.

Circle No. 300 on Inquiry Card

Gated Digitizer

This technical data sheet offers a comprehensive description of the LRS Model 143B Gated Digitizer, a high-speed, high-resolution instrument which converts the amplitudes or areas of nanosecond pulses to digital form for entry into scales or counter. LeCroy Research Systems Corp., West Nyack, N. Y.

Circle No. 328 on Inquiry Card

Data Set Application Manual

Technical Information Manual ECD-52 provides specifications, interfaces and application information on the Digi-Net TDM-211 switched telephone network data set for binary digital data transmission over typical voice channel up to 1200 bps. General Electric Communication Products Department, Lynchburg, Va.

Circle No. 301 on Inquiry Card

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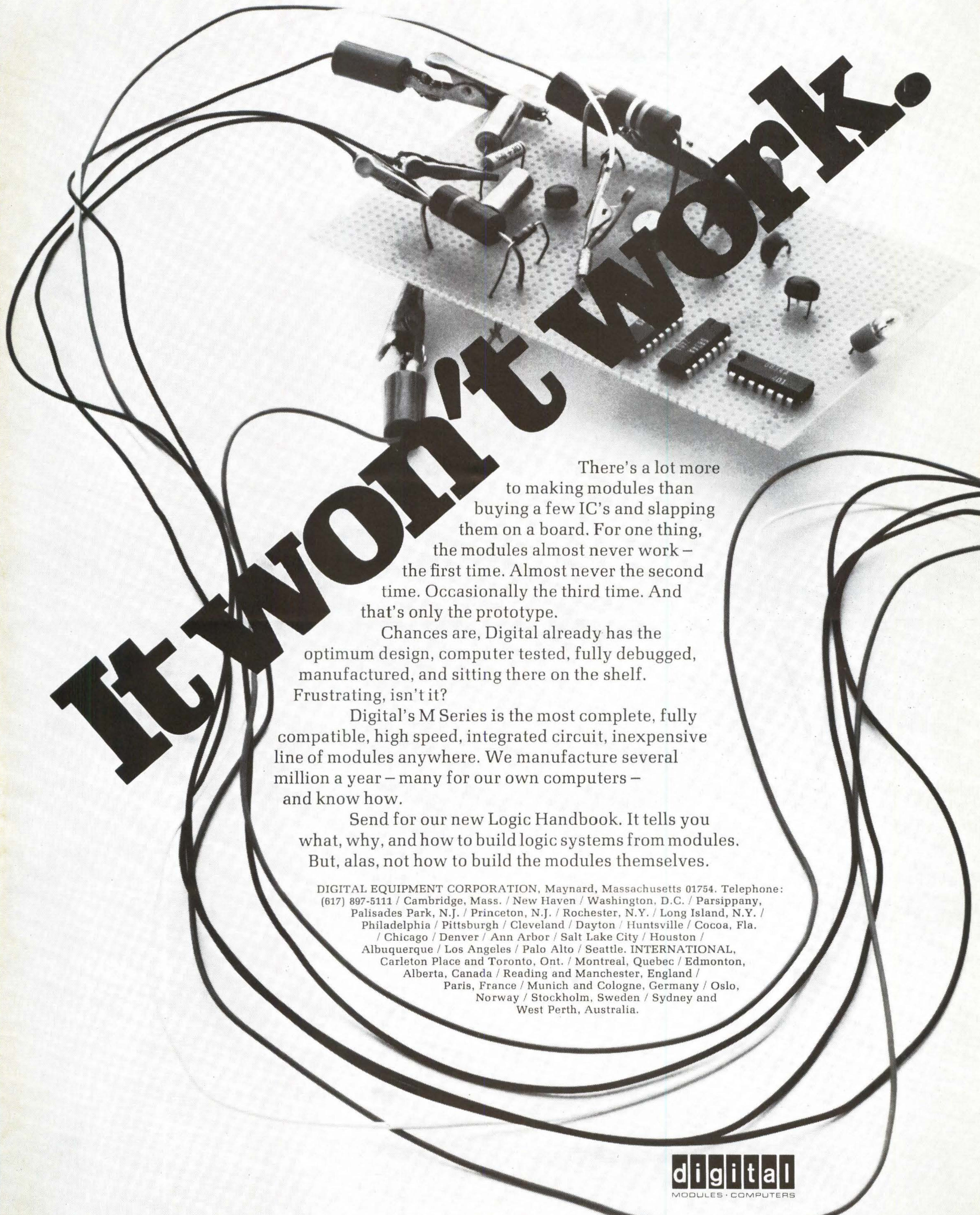
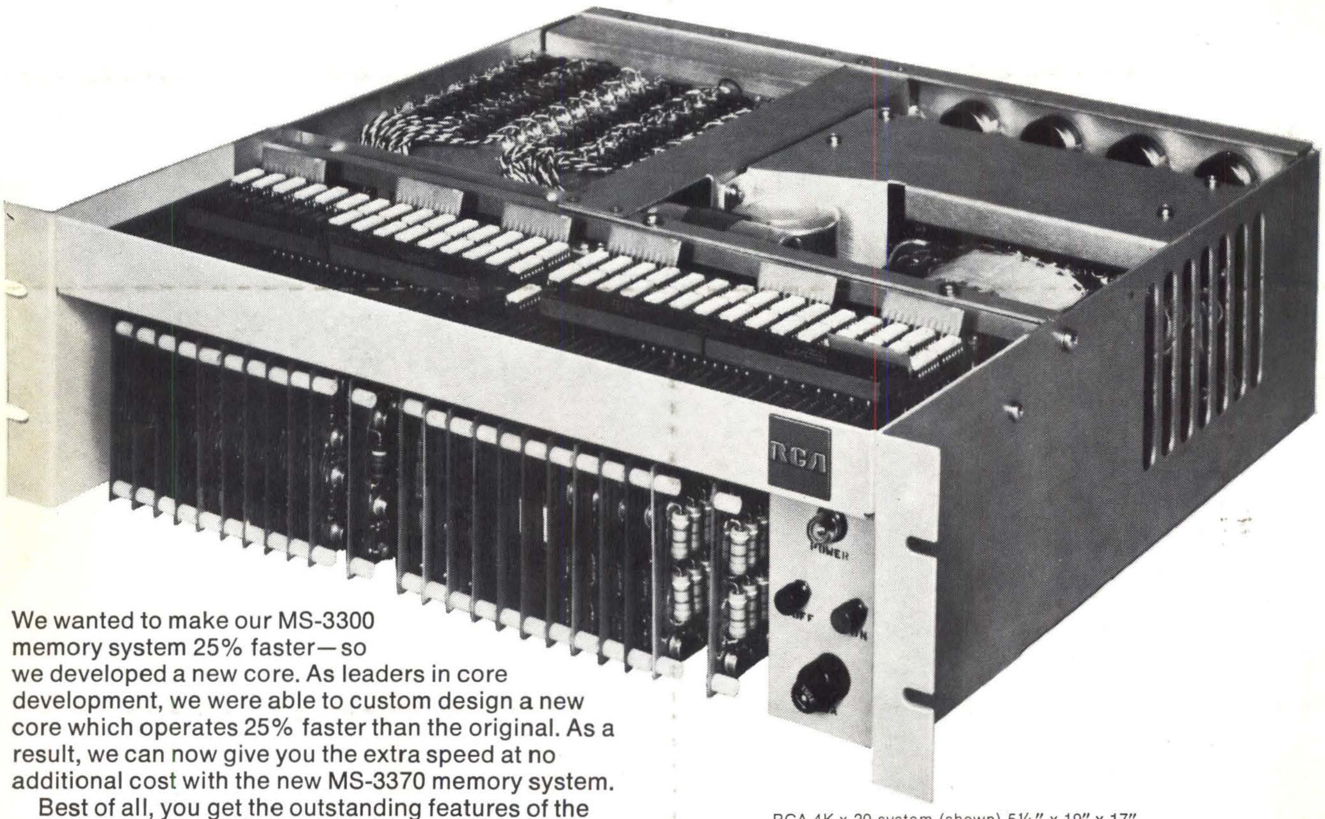


CIRCLE NO. 66 ON INQUIRY CARD

See us at the IEEE Show, Booth #2G02-2G09.

Announcing the new MS-3370 memory system full cycle time--750 ns access time--290 ns



We wanted to make our MS-3300 memory system 25% faster—so we developed a new core. As leaders in core development, we were able to custom design a new core which operates 25% faster than the original. As a result, we can now give you the extra speed at no additional cost with the new MS-3370 memory system.

Best of all, you get the outstanding features of the MS-3300 Series "3-wire 3-D" coincident current memory system using solid-state integrated circuits, and other features such as: temperature stability from 0°C to 50°C; exceptional reliability, low power requirements, and full range of options. And we continue to offer these systems as close to "off-the-shelf" as this industry can provide.

Take advantage of RCA leadership in memory core technology and system design. Find out all about our MS-3370 memory systems. For complete details, contact your RCA Field Representative. Or call Marketing Department (617-444-7200), RCA Memory Products Division, Needham Heights, Massachusetts 02194. For Data Sheet and Application Note, write Commercial Engineering, Section No. PZB-3, RCA Electronic Components, Harrison, N.J. 07029.

RCA 4K x 20 system (shown) 5¼" x 19" x 17"
Full cycle time ≤ 750 ns, access time ≤ 290 ns

RCA 16K x 40 21" x 19" x 20"
Full cycle time ≤ 750 ns, access time ≤ 350 ns

RCA

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