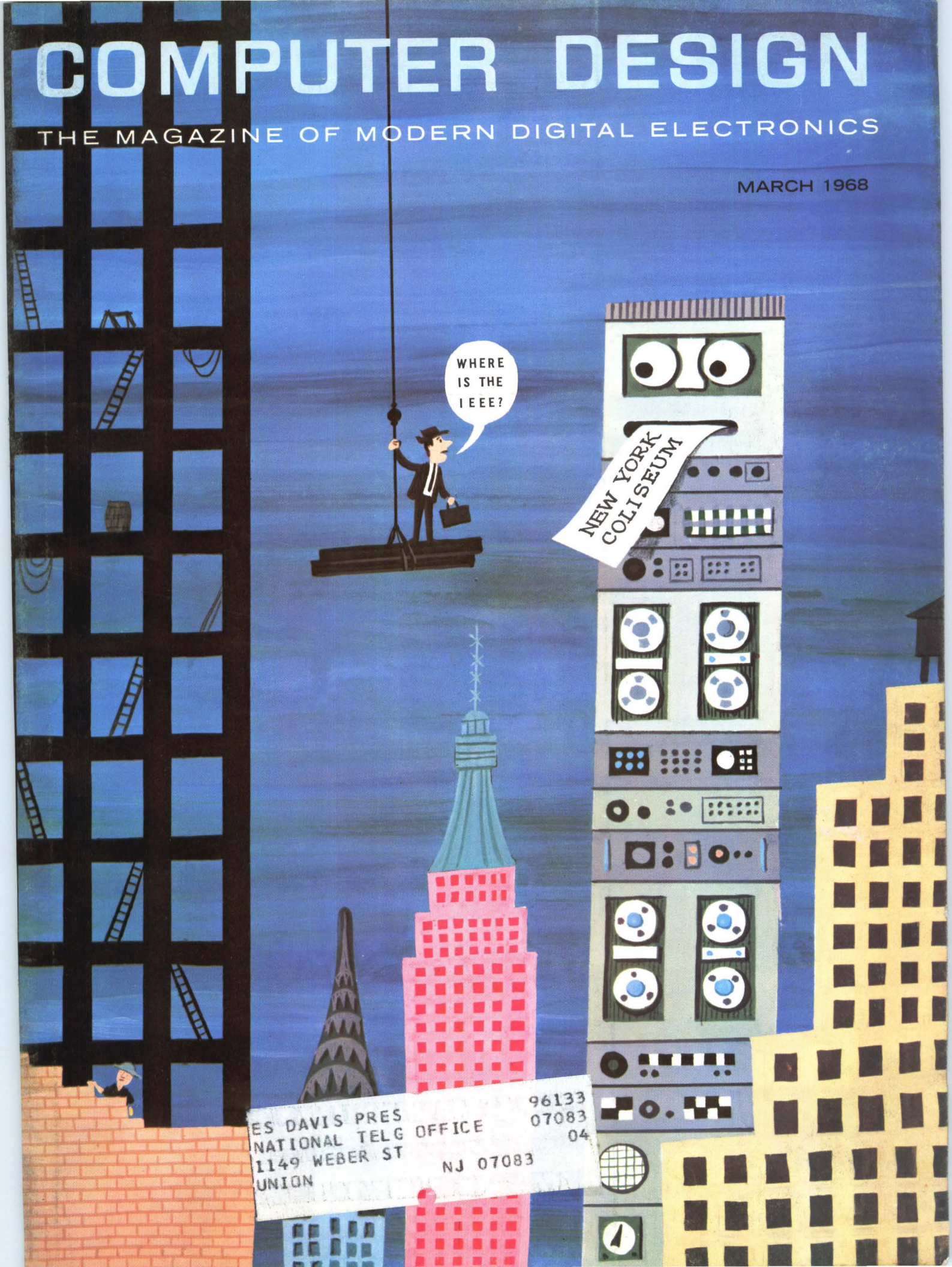
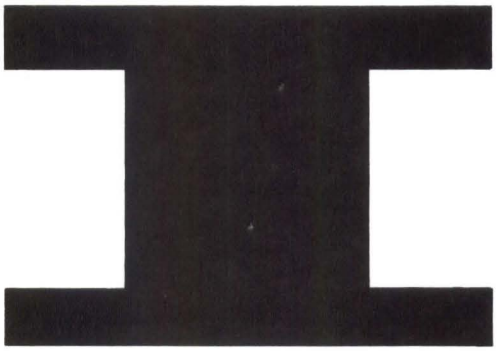
COMPUTER DESIGN

THE MAGAZINE OF MODERN DIGITAL ELECTRONICS

MARCH 1968





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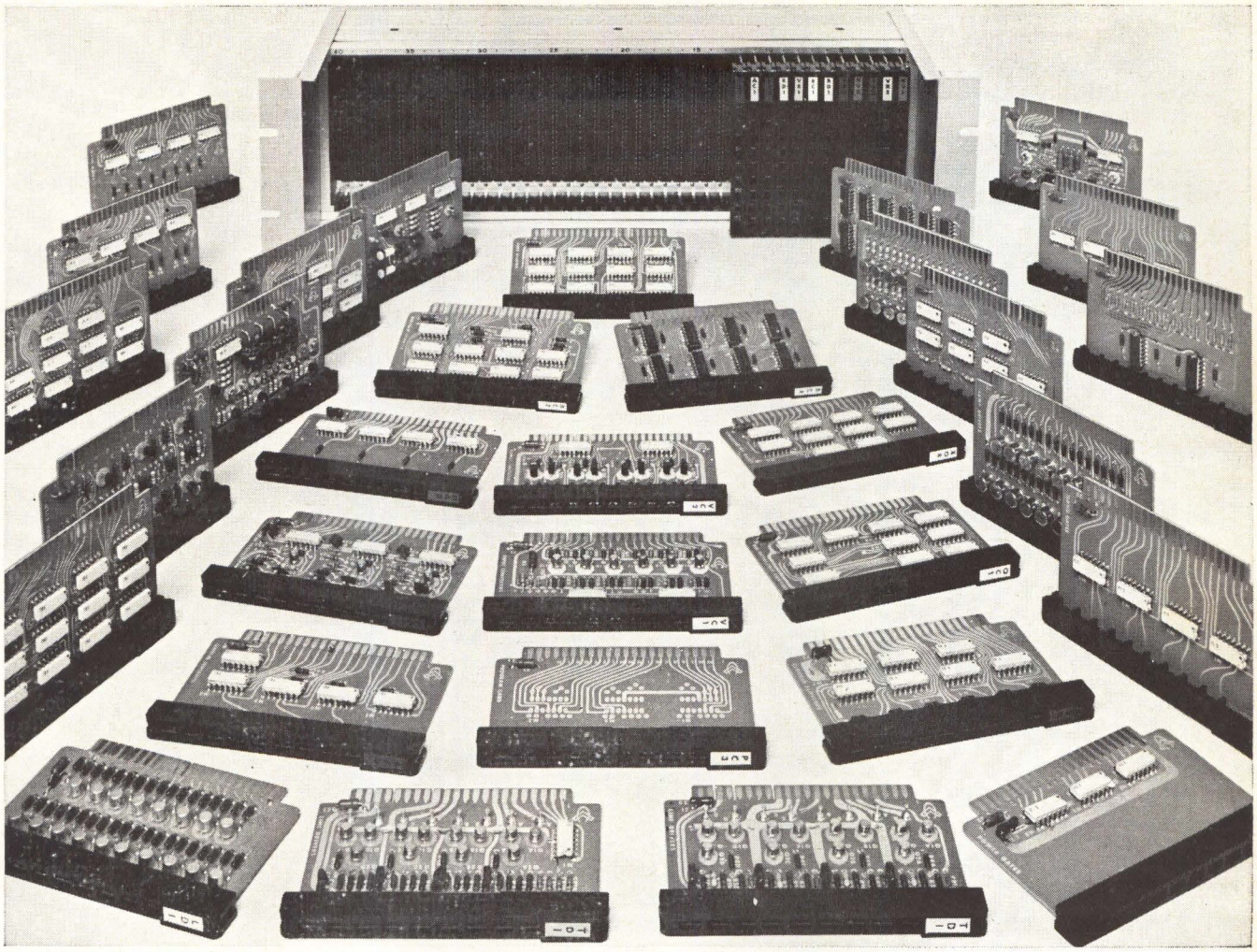

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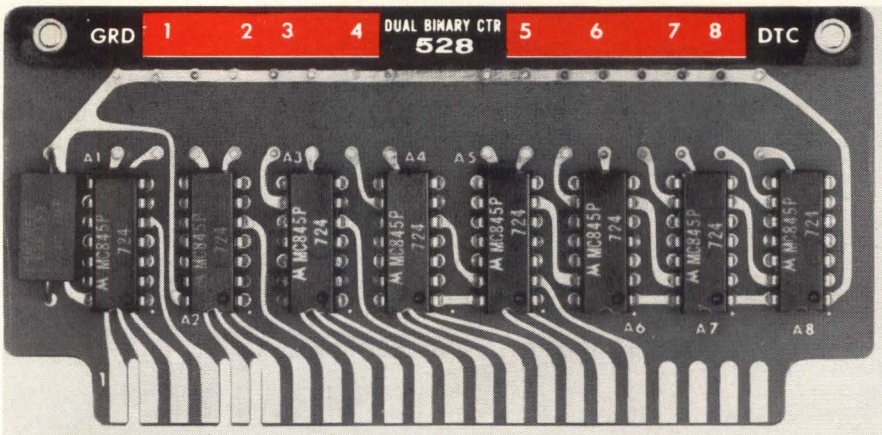
CIRCLE NO. 1 ON INQUIRY CARD



FREE FROM DATA TECHNOLOGY. A 387 PAGE I.C. LOGIC MODULE APPLICATIONS AND DESIGN MANUAL.

Only Data Technology . . . the company that has shipped more integrated circuit logic cards to system manufacturers than any other supplier could make such an offer.* ■

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*Data Technology's application and design manual . . . the most complete of this type ever printed . . . is free to all users. Ask our representative, listed below, to show you **his** copy. To get a copy for evaluation contact us or circle the appropriate reader service card number. For general catalog information circle the companion number. ■

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FEATURES

28 **FUNDAMENTALS OF TIME SHARED COMPUTERS (Continued)**

"Time Sharing" is presented in its most general sense as any application of a computer system that involves simultaneous users. Concepts and equipment of time-shared systems are defined and described and criteria for system configurations are given in terms of application requirements.

48 **SOLID-STATE SYNCHRO-TO-DIGITAL CONVERTER**

Placing the accuracy and speed burden for S-D conversion on the digital equipment minimizes the analog equipment and enhances system performance.

54 **A ONE MAP METHOD FOR OBTAINING FLIP FLOP INPUT EXPRESSIONS**

Most methods for obtaining flip flop input expressions require a Karnaugh map for each type of flip flop considered. This article presents a method that requires only one map, regardless of the number of different types of flip flops to be investigated.

60 **A PROPOSED ASSOCIATIVE PUSH DOWN MEMORY**

Small, high-speed semiconductor memories designed to store the most recently-used information contained in the main memory can increase the effective speed of computing systems.

68 **THE ANTRAM INPUT-OUTPUT TERMINAL**

Operating simplicity, minimum cost, sophisticated programming and graphical display capability are achieved in the design of an input-output terminal.

DEPARTMENTS

20 **INDUSTRY NEWS**

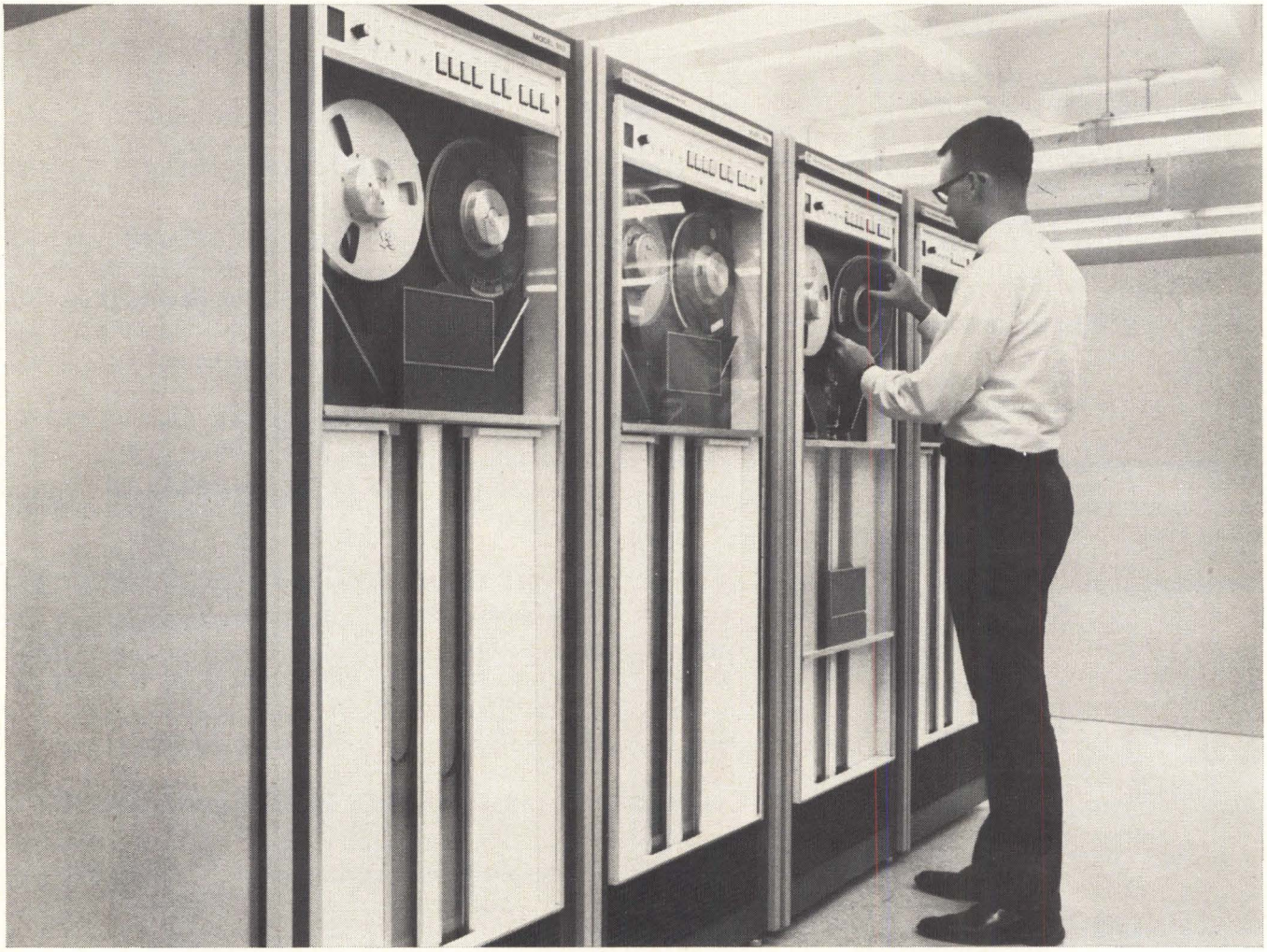
76 **NEW PRODUCTS**

86 **NEW LITERATURE**

Reader subscription card ..... *opposite page 1*

Reader service card ..... *opposite page 88*

NEW! Designed for the Computer O.E.M.



A simple, reliable and economical computer tape transport that meets the critical requirements of the original equipment manufacturer. It's called the Model 959 Computer Tape Transport, and it's made by Texas Instruments.

Advanced design is the reason why. You get a machine that handles from 200 to 800 bpi at 60 to 120 ips, yet has remarkable simplicity. Permanent magnet reel motors and a printed circuit capstan motor eliminate gears, belts, pulleys, clutches, and other cumbersome mechanical systems. No pinch rollers are used, and tape is automatically loaded without moving the read/write head.

The size and complexity of electronic circuitry has been reduced through the use of the latest linear and digital integrated circuits with advanced silicon power transistors.

Improve your price/performance ratio with the new TI Model 959 Computer Tape Transport. Lower maintenance costs improve system quality with a transport designed for the original equipment manufacturer. For more information, contact your TI representative or Texas Instruments, Industrial Products Division, P. O. Box 66027, Houston, Texas 77006 (713-227-3611).

See the Model 959 Computer Tape Transport at the IEEE — Booths 2F08-20

TEXAS INSTRUMENTS
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CIRCLE NO. 2 ON INQUIRY CARD

Computers are big, expensive components. Bit for bit, ounce for ounce, some are a bargain.

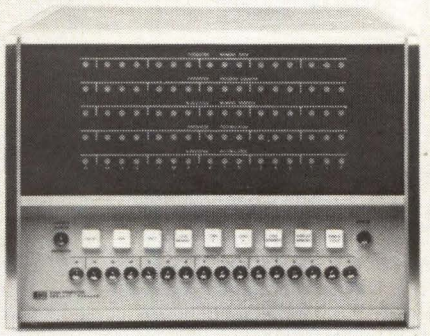
When you tie another man's computer into your product, you're staking your reputation on his equipment. Your reputation is worth shopping for. Naturally you want the most for your dollar. Like reliability at 130° F. Hewlett-Packard computers are designed for rugged dependability—as well as high performance. All things considered, they're something of a bargain.

We've been selling quality instruments to original equipment manufacturers for years. We know the problems. So we back our computers with excellent training, complete service and our traditional warranty. We'll train your people or your customer's people in maintaining the computer and in using the software.

We supply plug-in I/O interfaces and the software drivers for peripheral devices. You buy only the equipment you need for interfacing your system. And you tie it in with minimum engineering time because both hardware and software are operational and fully documented.

The 2115A pictured here measures 16¾"x 12"x 24⅜" (its power supply is a bit smaller). It uses 16-bit words, operates with 4K or 8K memory, and has a two microsecond cycle time. Price: $14,500.

For more information about a computer that will live up to your reputation, call your local HP field engineer. Or write Hewlett-Packard, Palo Alto, California 94304; Europe: 54 Route des Acacias, Geneva.



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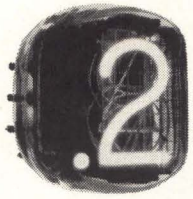
06807

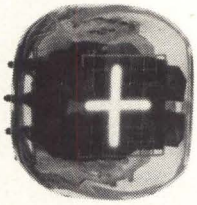
CIRCLE NO. 3 ON INQUIRY CARD

Here's why you should now be using Datavue* Indicator Tubes

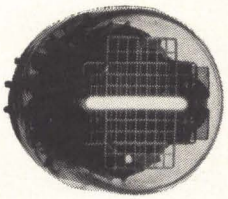


CK1904—Interchangeable with B59956 and NL809.

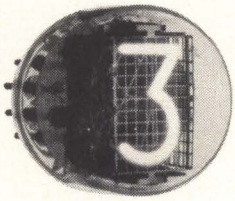
8422—Interchangeable with B5991 and NL8422.



CK1903—Interchangeable with B5992 and NL5992.



CK1901—Interchangeable with B5016 and NL5016; CK1902—Interchangeable with B5032, NL5032, B50911 and NL50911.

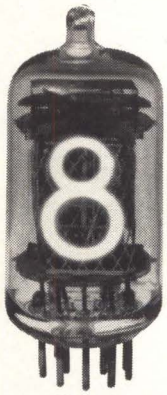


8421—Interchangeable with B5092 and NL8421; 8037—Interchangeable with B5031 and NL8037. Also available: 6844A.

CK1900 (used with CK8650, CK1905, CK1906); CK1907 (used with 8754)—Interchangeable with NL843.

8754—Also available with right- and/or left-hand decimal points; Interchangeable with NL840/8754. Decimal-point types interchangeable with NL841, 842, 848.

CK1905; CK1906 (right-hand decimal point).



CK8650

These indicator tubes—just a few of Raytheon's wide selection—offer you advantages in design, economy and performance. For example:

You don't need to revise designs. Raytheon's Datavue round and rectangular end-view tubes conform to EIA ratings—interchange with other brands. And Raytheon also offers you a selection of side-view types—and "specials" with up to 12 characters, ± signs, symbols, etc., to your specifications.

You can buy them at low cost. All Datavue Indicator Tubes are priced competitively—or lower. Most side-view types, for example, cost less than $5 each in lots of 500 or more.

Reliably trouble-free readouts. All Datavue characters are fully formed—not segmented. The fully formed characters are brightly displayed and easy to read—at distances up to 30 feet.

They last for years. They're made better because of Raytheon's experience—40 years of producing more than 100,000,000 cold cathode gas-filled tubes with carefully controlled electrical performance. Ultra-long-life types, for example, have dynamic life expectances of 200,000 hours or more.

They're readily available—in sample and production quantities. For samples, prices, or technical information, call your Raytheon regional sales office or distributor. Or write: *Raytheon Company, Industrial Components Operation, Quincy, Mass. 02169.*

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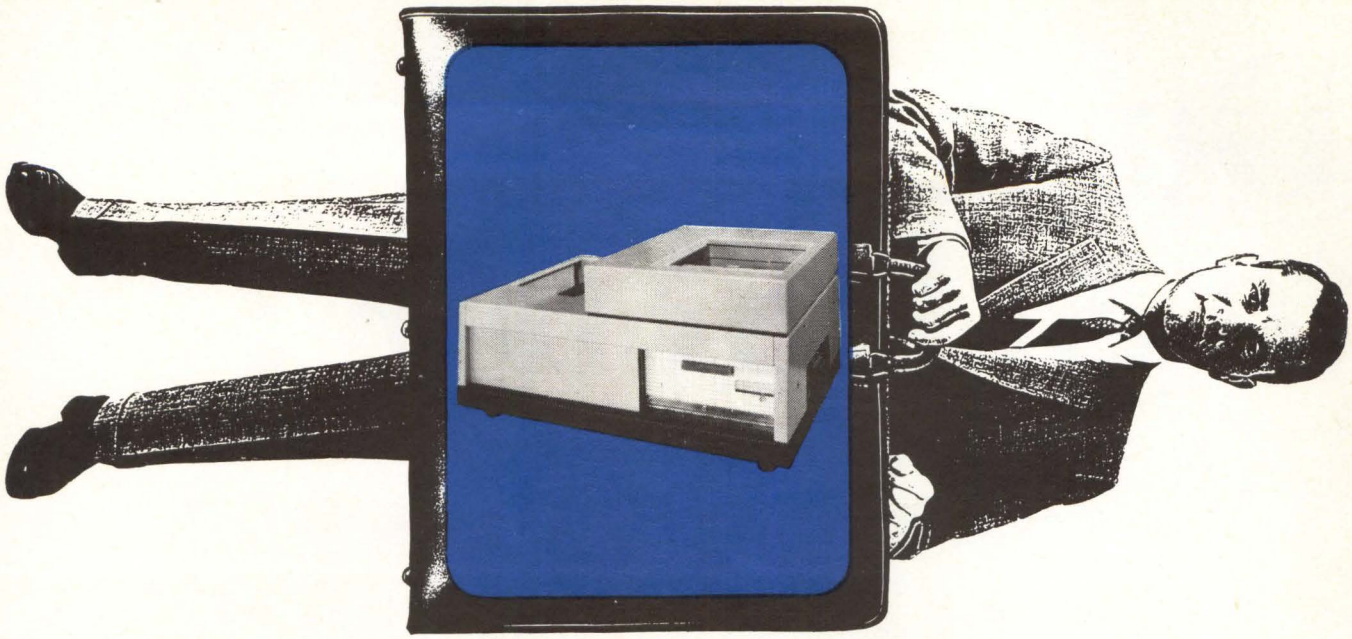
CIRCLE NO. 4 ON INQUIRY CARD



The Peripheral People announce the ultimate in reading reliability– the D4 punched card reader. It's great for companies that hate the sight of a maintenance man.

NCR knows more about electro-mechanics than anyone. That's why the economical D4 300 cpm reader keeps up the good work longer, with minimal maintenance. Still we know that sooner or later a card will stick, so we made the card track fully accessible—an operator can free a jam in seconds. If you should ever need service (after an earthquake, fire or office party), the D4's modular construction makes it fast and easy. For information on speedy delivery, contact the Peripheral People today.

NCR®

THE PERIPHERAL PEOPLE

Card Readers, Tape Punches, Tape Readers, Printers, MICR Readers, CRAM (Card Random Access Memory)

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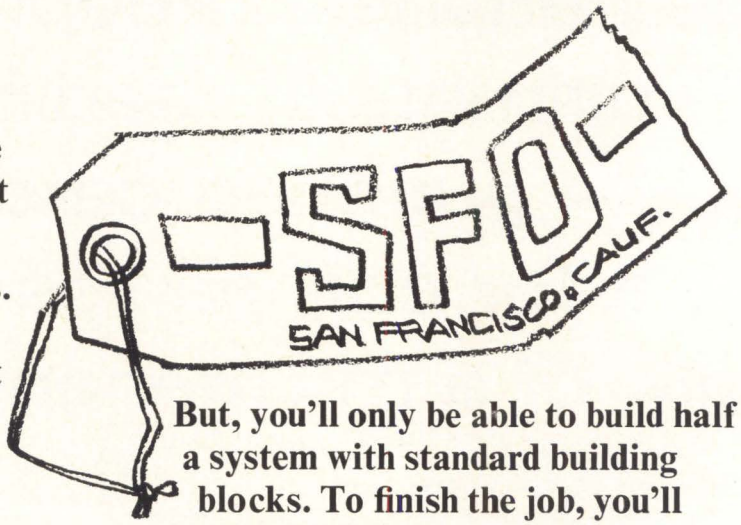
CIRCLE NO. 5 ON INQUIRY CARD

Do you want to go LSI now?

If you really want LSI now, grab the next plane to Mountain View. (It lands in San Francisco.) It's the quickest, least expensive way to get LSI into your system.

Plan to bring along your blueprints. And be ready to answer a lot of questions. We'll need to know what you have in mind for sub-systems, functions and specs. And, don't be surprised when we ask "why" a couple of times. It's all part of Fairchild's systems approach to complex circuitry.

We'll take your requirements and match them against our family of fundamental building blocks. We've got LSIs (and MSIs) that work in any digital logic system. The most advanced circuitry on the market. Offspring of computer-aided design and double-layer metal technology. And, they're all so versatile, we can probably give you a counter that has a dozen other applications in your system.

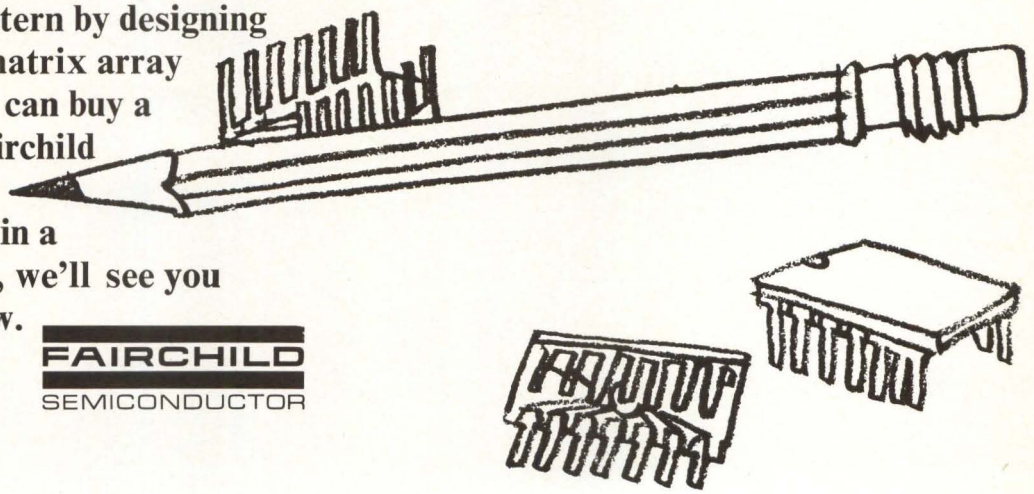


But, you'll only be able to build half a system with standard building blocks. To finish the job, you'll need interface devices to tie the whole thing together. And, here's where Fairchild can really save you time and money. We don't have to custom design each LSI interface circuit. We use Micromatrix™–a unique cellular array that's completed when we add your specific interconnection pattern. Your specs customize the entire array for your system.

Of course, there's a lot more to the story. But, you ought to hear it in person. Just call your Fairchild salesman. He knows the flight schedule to San Francisco.

Or do you want to think about it?

We've got an LSI design kit. It's based on our new 4500 Bipolar Micromatrix Array—the first device in a highly versatile LSI family. The 4500 is an eight-cell array that can be customized for virtually any function. All it needs is your interconnection pattern. You can determine the pattern by designing your own Micromatrix array with our kit. You can buy a kit from your Fairchild distributor for about $100. And, in a couple of months, we'll see you in Mountain View.



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CIRCLE NO. 6 ON INQUIRY CARD

Cheap mass storage for small computers and how to get the most out of it

For some people the only limitation of the small computer is the price of the extra memory. What's needed is low-cost mass storage, and lots of it. For filing data. For quick and convenient program manipulation.

DIGITAL, the leader in small computers, has a low-cost disc and unique magnetic tape unit tailored for the small computer. Now, new software is available to take even better advantage of this low-cost memory.

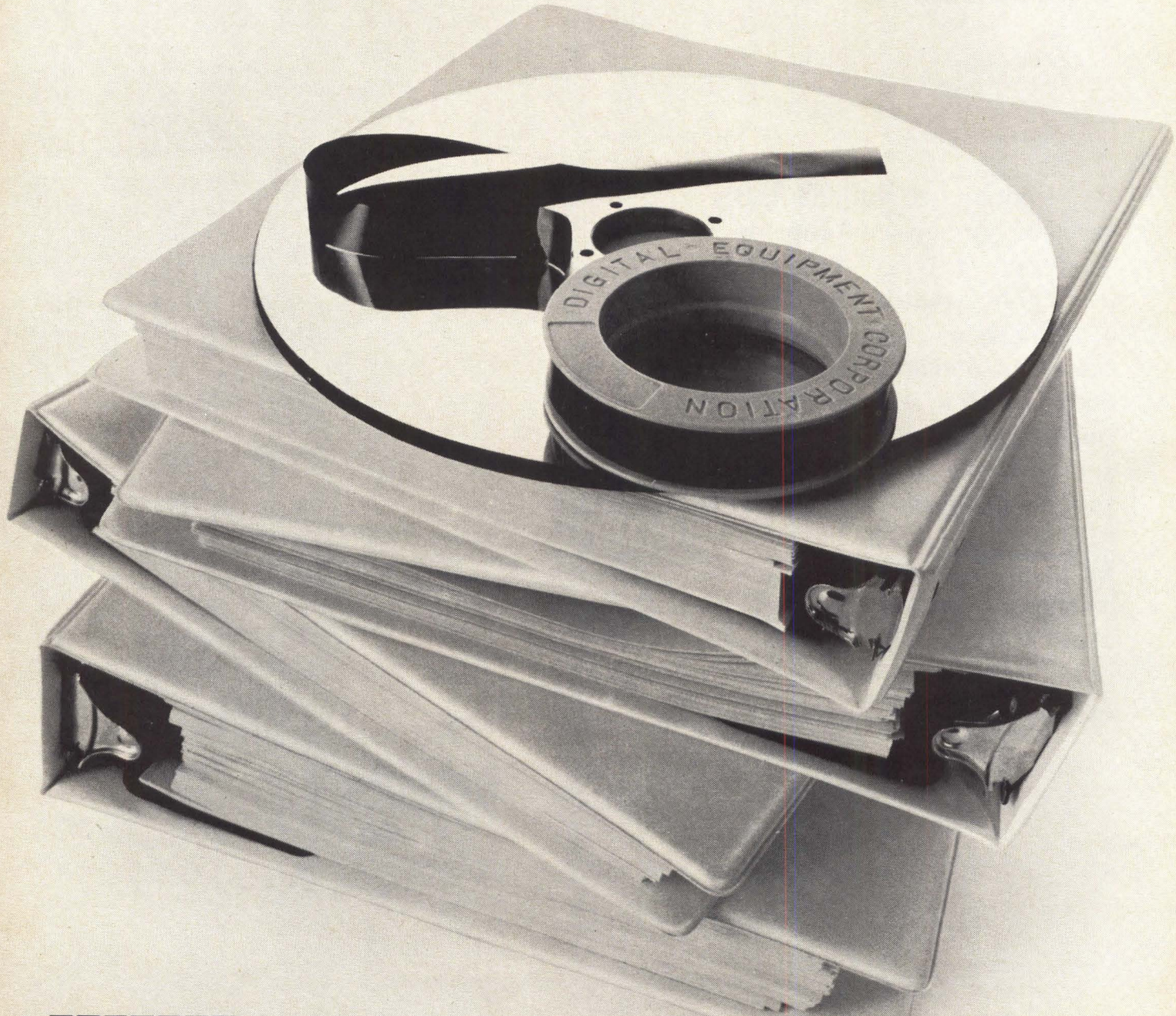
DECdisc adds 32,768 words of memory for $6,000. Additional expander discs (up to 3) can be added at $3,000 each. That means a total of 131,072 words of disc memory for $15,000.

A full scale PDP-8/S computer with 36,864 twelve bit words of memory, for example (4k core plus disc), costs $18,500.

DECtape, Digital's unique fixed address magnetic tape system, provides over 200,000 words of storage on a 3½-inch reel. It's the lowest cost mass storage available anywhere. You can edit and debug programs on line. Then you can put your programs in your pocket and take them away until you want them again.

New keyboard monitor software all but eliminates the laborious use of paper tape and cards. You edit from the keyboard, compile from the keyboard, assemble, load, store, debug all from the keyboard. What might have been hours or days in getting the computer ready for use, is now just minutes.

Available now. PDP-8/S off-the-shelf. PDP-8 in one month. PDP-8/I in the spring. DECdisc and DECtape immediately available. Send for our new Small Computer Handbook. It's free.



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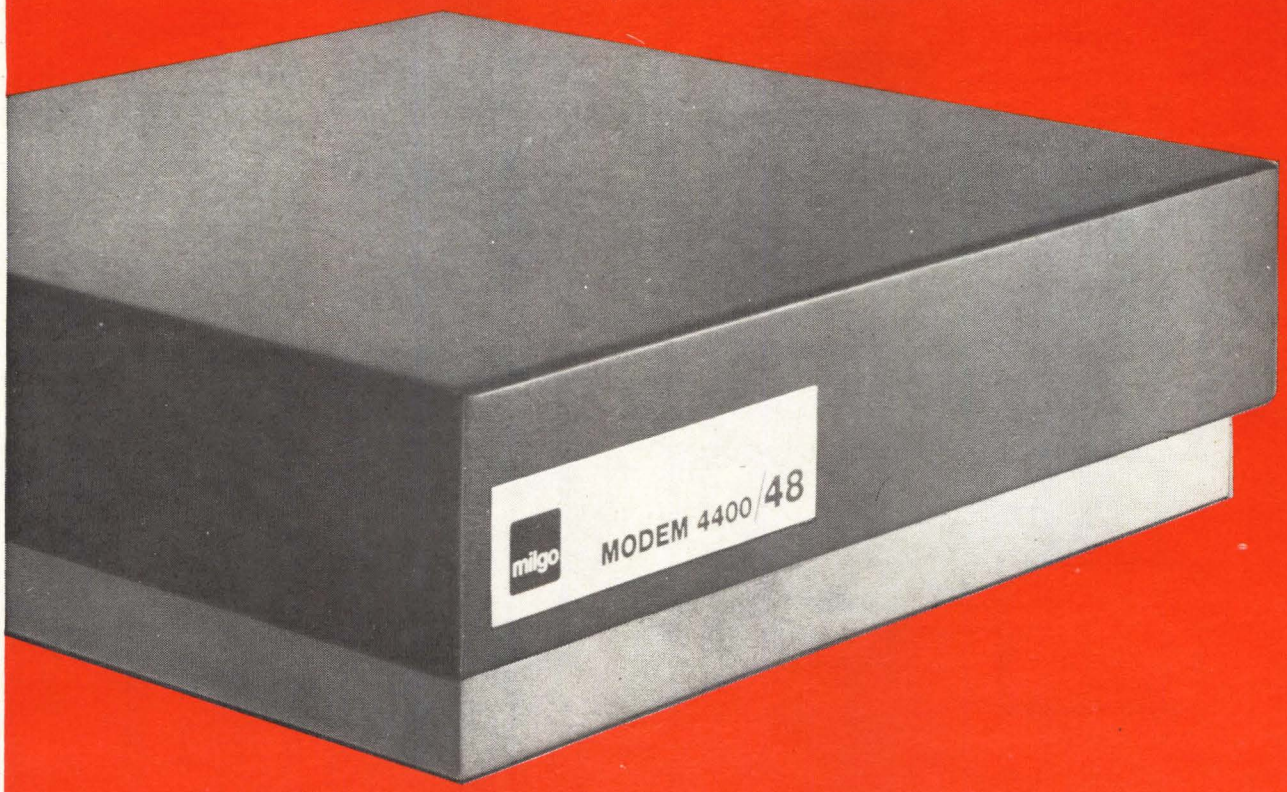
4800 bps has grown up!



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a data set with:
quick, simple installation
dependable operation
maximum throughput
lower costs

MODEM 4400/48

No more costly delays in acquiring and operating over highly conditioned transmission lines. MODEM 4400/48 by-passes the troublesome bandwidth on any line, conditioned or not, just like our 2400 bps modem. Milgo's unique* narrow-band concept allows transmission on unequalized voice grade Type 3002 lines, the lowest cost lines available. The cost per unit — much less than other 4800 bps data sets!

Let us show you how 4800 bps has grown up. Send for data sheets and information on nearby users.

milgo

Milgo Electronic Corporation
7620 N. W. 36th Avenue, Miami, Florida 33147
*patent applied for

← CIRCLE NO. 7 ON INQUIRY CARD

CIRCLE NO. 8 ON INQUIRY CARD

RECAP:

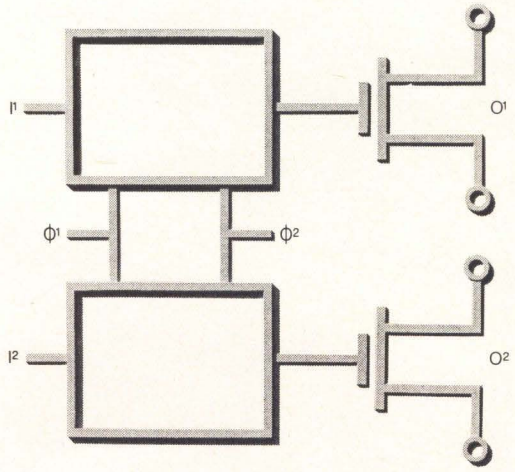
Starting October 9, 1967, Fairchild promised to introduce a new integrated circuit each week for 52 weeks. This is number **15.**

3303 DUAL 25-BIT DYNAMIC SHIFT REGISTER

The 3303 is a product of Planar II*, P-channel enhancement mode MOS technology. It contains two 25-bit shift register strings with two common clock lines. Output stages can be connected as either inverters or as source followers. It is applicable for digital delay lines in computers and radar systems (both ground and airborne). It can also be used as a serial memory in telemetry systems.

The 3303 comes in a TO-5 can and will operate over the entire temperature range from −55°C to +85°C. It operates at 1 MHz (typical). Power dissipation is typically less than 2mW per bit. Volume quantities of the 3303 are now available. Your Fairchild distributor has it in stock. Write for complete specs and applications information. Ask about our other new products, too.

*Planar is a patented Fairchild process.



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CIRCLE READER SERVICE NUMBER 115

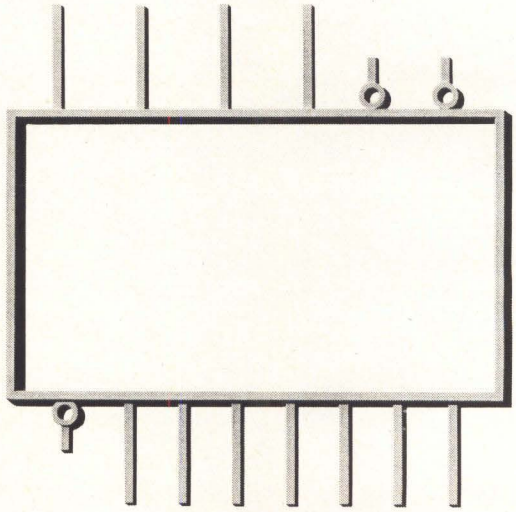
Starting October 9, 1967, Fairchild promised to introduce a new integrated circuit each week for 52 weeks. This is number **16.**

9307 BCD TO SEVEN-SEGMENT DECODER

The Fairchild 9307 is designed to be used in any numeric display system which requires seven-segment information. This includes incandescent, electroluminescent, seven-segment neon, or CRT numeric displays. It is an MSI device. It accepts an input in 8421 BCD code and produces individual outputs to drive the seven-segment display system. It has an active low input lamp test which overrides all other input combinations and verifies overall lamp operation. It also has active high outputs (1.3mA minimum). In addition, it has ripple blanking inputs and outputs to provide leading edge zero suppression. It also has intensity modulation capability.

The 9307 is a CCSL device in a 16-pin hermetic DIP. It operates from a single 5-volt power supply. It comes in both military and industrial temperature ranges (−55°C to +125°C and 0°C to +70°C). The 9307 is available in volume quantities. Your Fairchild distributor has it in stock now.

Write for complete specs and applications information. Ask about our other new products, too.



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CIRCLE READER SERVICE NUMBER 116

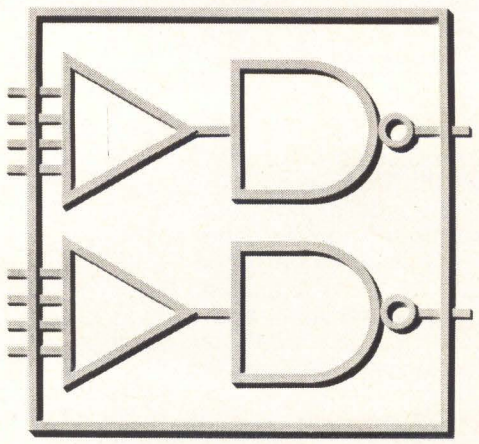
Starting October 9, 1967, Fairchild promised to introduce a new integrated circuit each week for 52 weeks. This is number **17.**

9620 DUAL DIFFERENTIAL LINE RECEIVER

The 9620 is designed to take differential logic from transmission lines and convert it to CCSL levels. It also has the capability for conversion to higher levels. It is ideal for use in data net collectors, or in data processing applications where the central processor and data source are in separate locations. The 9620 can also be used as a CCSL-compatible differential comparator.

Each section of the dual IC consists of a differential amplifier driving a saturating inverting DTL gate with uncommitted collector. Maximum differential threshold voltage is ±500mV in the presence of ± 15 volts common mode. Typical power dissipation is 55mW per receiver. Propagation delay is 30ns maximum at 25°C. High common mode rejection is also provided.

The 9620 comes in a 14-pin hermetic DIP and will operate in both military and industrial temperature ranges (−55°C to 125°C and 0°C to +70°C.) It's available in volume quantities. Your Fairchild distributor has it in stock now. Write for complete specs and applications information. Ask about our other new products, too.



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CIRCLE READER SERVICE NUMBER 117

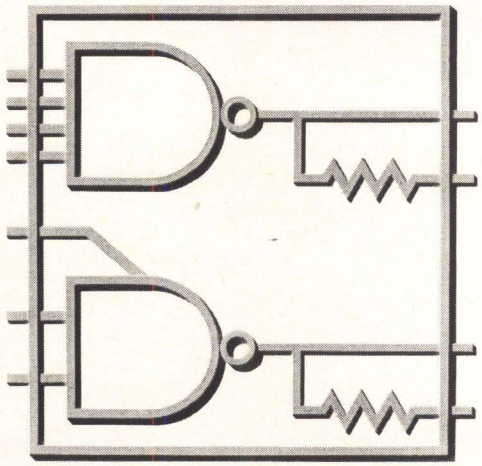
Starting October 9, 1967, Fairchild promised to introduce a new integrated circuit each week for 52 weeks. This is number **18.**

9621 DUAL LINE DRIVER

Fairchild's 9621 is used to transmit CCSL-level logic down transmission lines. It can also be used to drive high capacity loads. It consists of a 4-input inverting DTL gate and a 2-input inverting DTL gate. There is a termination resistor available on each stage which permits you to backmatch 130-Ohm lines, either directly or differentially. An extender is available on the 2-input gate which allows you to add additional external diodes, and thus obtain more inputs. The 9621 can also be used as a low output impedance device. Each driver provides minimum output current of 20mA at 0.4V. Diode clamps are provided to damp reflections on the output.

Maximum power dissipation for the new IC is 210mW. Propagation delay is 25ns maximum into a 30pF load. It comes in a 14-pin hermetic DIP and will operate in both military and industrial temperature ranges (−55°C to +125°C and 0°C to +70°C).

Applications for the 9621 include data processing and computer peripheral equipment. It is designed specifically to operate in conjunction with our 9620 dual differential line receiver (New Product No. 17). Both devices are available in volume quantities. Fairchild distributors have them in stock now. Write for complete specs and applications information. Ask about our other new products, too.



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CIRCLE READER SERVICE NUMBER 118

Fairchild is introducing a new integrated circuit every week. The last two months look like this.

FAIRCHILD
SEMICONDUCTOR

Starting October 9, 1967, Fairchild promised to introduce a new integrated circuit each week for 52 weeks. This is number **19.**

3300 25-BIT MOS STATIC SHIFT REGISTER

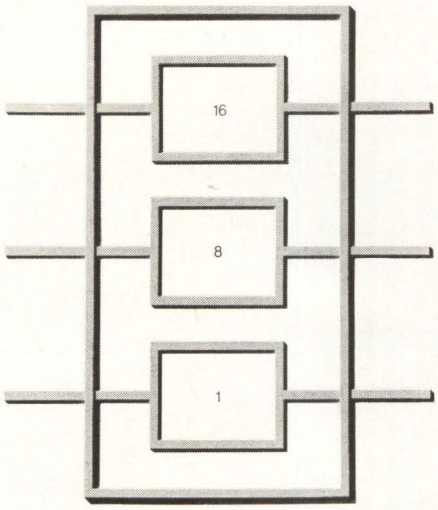
The 3300 is the fifth MOS device we've introduced since December 11, 1967. (The first four were the 3701 six-channel multiplex switch; 3102 three-input gate; 3700 four-channel multiplex switch; and the 3303 dual 25-bit dynamic shift register.)

The 3300 is a monolithic IC utilizing Planar II*, P-channel enhancement mode MOS technology. It is designed to be used for digital delay lines and long serial memory storage in radar systems and computers. It is also applicable for data storage in telemetry systems.

The 25-bit device comes in a TO-5 can and will operate over the entire temperature range from −55°C to +85°C. There are independent 16-, 8- and 1-bit data strings within the package. Power dissipation is typically 2mW per bit. Speed is typically 500KHz. The clock drive circuit is simplified by a single-phase clock input. The output is buffered to improve drive capability.

Volume quantities of the 3300 are now available. Fairchild distributors have it in stock. Write for complete specs and applications information. Ask about our other new products, too.

*Planar is a patented Fairchild process



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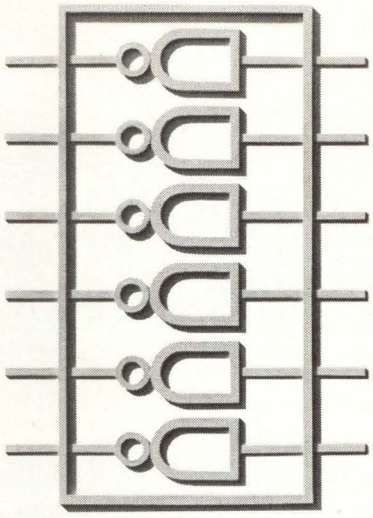
CIRCLE READER SERVICE NUMBER 119

Starting October 9, 1967, Fairchild promised to introduce a new integrated circuit each week for 52 weeks. This is number **20.**

9110 HIGH LEVEL LOGIC HEX INVERTER

The 9110 is the fundamental element of our new high noise immunity family. It features worst case DC noise immunity of 5.5 volts. And, AC noise immunity is even better (it can reject pulses of 100 nanoseconds duration and 20 volts amplitude minimum). Other members of the family provide interfacing capability to make the 9110 compatible with CCSL levels.

The 9110 consists of six high-level DTL gates without input diodes. It can be expanded with external diodes on the input. There is active pull-up on the output for good drawing capability. Propagation delay is typically as slow as 170 nanoseconds to reduce sensitivity to high-level noise pulses. Output voltage swing is typically 0.5 to 15 volts. The 9110 operates over the entire range of 12 to 20 volts at temperatures of 0°C to +70°C. It comes in an hermetic DIP and is available in volume quantities. It's in stock at your Fairchild distributor now. Write for complete specs and applications information. Ask about our other new products, too.



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CIRCLE READER SERVICE NUMBER 120

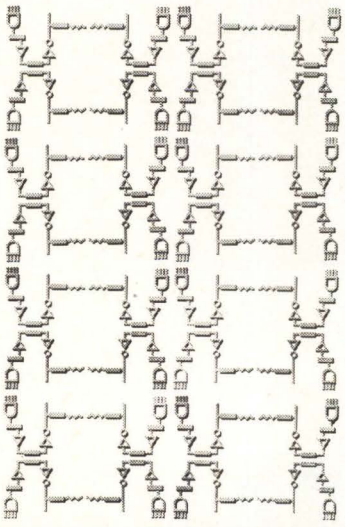
Starting October 9, 1967, Fairchild promised to introduce a new integrated circuit each week for 52 weeks. This is number **21.**

4500 BIPOLAR MICROMATRIX™ ARRAY

Fairchild's 4500 is the first device in a new, highly versatile LSI family of fundamental elements. It can be used in any digital logic system. And, it can be customized for virtually any function. Fairchild's unique LSI capability is the result of two major achievements: double-layer metal processing and computer-aided design.

The 4500 is a monolithic CCSL device consisting of eight cells. Each cell is made up of four 4-input DTL gates. The entire array is capable of custom interconnection between cells and portions of cells to produce any logic function. The primary application for the 4500 is in circuits used to interconnect basic system building blocks. However, it can also be used as a fundamental building block, itself. The new LSI array comes in an hermetic DIP as well as in flatpack.

Since the 4500 cannot be completed without your specific requirements, we've prepared a kit to help you design your own custom circuits. It's at your Fairchild distributor now. Write for detailed specs and applications information.



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CIRCLE READER SERVICE NUMBER 121

Starting October 9, 1967, Fairchild promised to introduce a new integrated circuit each week for 52 weeks. This is number **22.**

3320 MOS 64-BIT, 4-PHASE SHIFT REGISTER

The 3320 is a shift-register/accumulator. Its input logic can be used to control the loading of new information, or the recirculating of existing information, in the device. Its primary applications include digital data accumulation in telemetry systems, long-serial memories for computers, long delay lines in radar equipment and industrial serial system control.

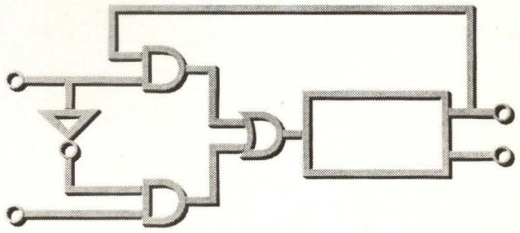
No DC power supplies are required for 3320 operation. It comes in a TO-5 can and will operate over the entire temperature range from −55°C to +85°C. Both data and data-complement output are provided. Power dissipation is approximately 200μW per bit at 2MHz.

The 3320 is a product of Planar II* P-channel enhancement mode technology. It's the sixth monolithic MOS IC we've introduced since December 11, 1967. (The others are the 3701 six-channel multiplex switch; 3102 three-input gate; 3700 four-channel multiplex switch; 3303 dual 25-bit dynamic shift register; and the 3300 25-bit static shift register.)

Volume quantities of all six devices are available. Your Fairchild distributor has them in stock. Write for complete specs and applications information.

*Planar is a patented Fairchild process

To order the 3320, ask for Part No. 43F3320 1X
Price: $25.00 (1-24)
20.00 (25-99)
23.50 (100-999)



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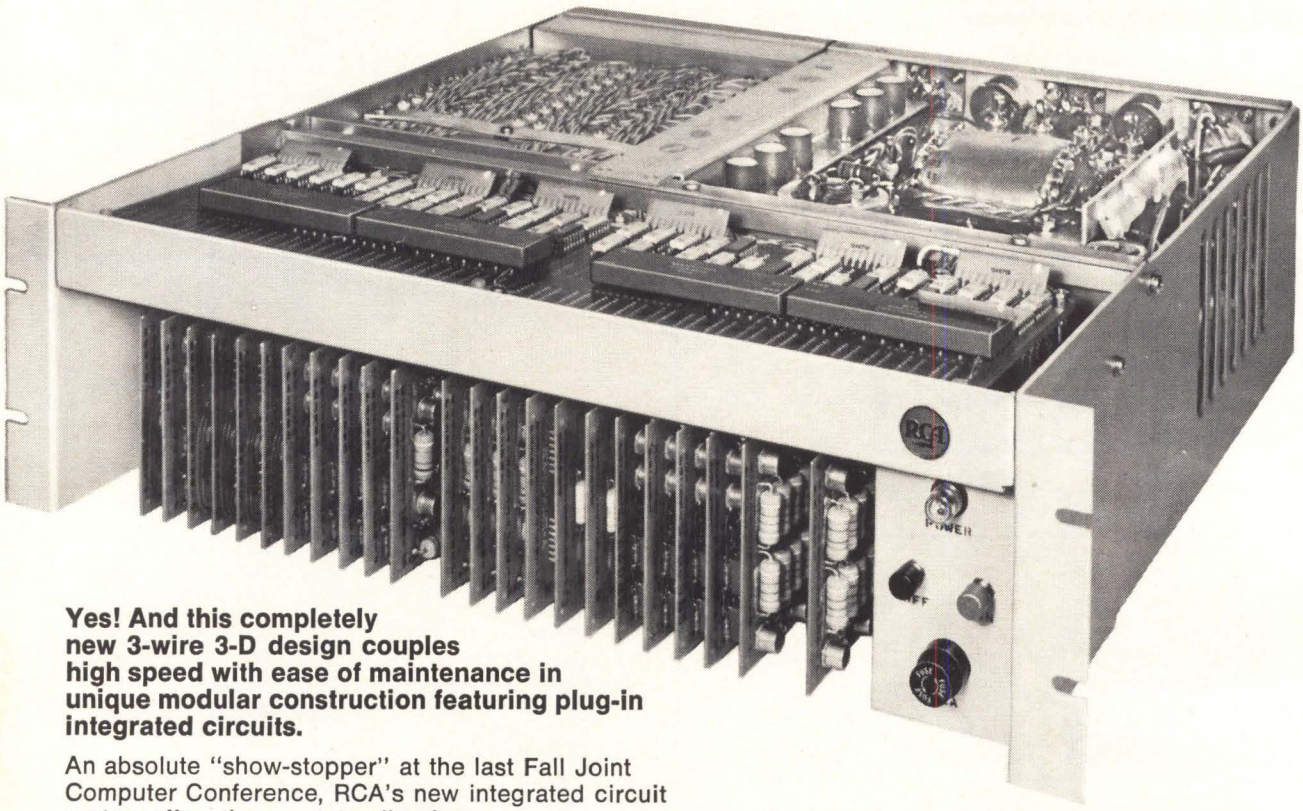
CIRCLE READER SERVICE NUMBER 122

Can a coincident-current memory system cycle faster than 1 microsecond?



RCA 4K x 20 system with integral power supply measures: 5¼"H, 19"W, 20"D.

Yes! And this completely new 3-wire 3-D design couples high speed with ease of maintenance in unique modular construction featuring plug-in integrated circuits.

An absolute "show-stopper" at the last Fall Joint Computer Conference, RCA's new integrated circuit system offers these outstanding features:

Temperature stable; 0°C to 50°C.

High Level TTL logic—excellent noise immunity, exceptional reliability, low power requirements.

Full range of options for wide flexibility: parity check circuit—sequential address register—memory retention—read, modify, write mode-voltage margin switch—special interfacing for most requirements—exerciser for self checking.

Available with short delivery schedules, RCA's new 3-wire 3-D coincident current core memory systems are designed with capacities of 4K x 8 to 32K x 72.

For complete details, contact your RCA Field Representative. Or call Marketing Department (617-444-7200), RCA Memory Products Division, Needham Heights, Mass. 02194. For Data Sheet and Application Note, write Commercial Engineering Section 0000. RCA Electronic Components and Devices, Harrison, N.J. 07029.

RCA

Printed in U.S.A.

CIRCLE NO. 9 ON INQUIRY CARD

How do you gruntle the buyer of memory stacks?

(Take a powder and control it all the way).

The man who buys memory stacks (or planes or just cores) knows that a myriad of tiny variables which affect performance can pass right through the tightest spec. It's nobody's fault, but still it leaves the buyer disgruntled.

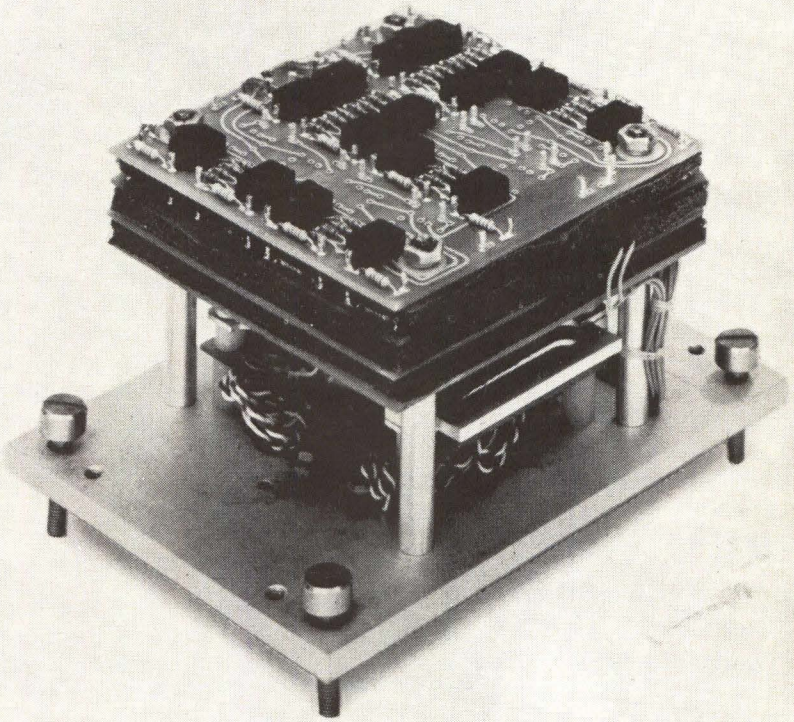
How to gruntle him? Well, this is what we do at Ferroxcube. We control the entire process from formulation of the powder for the cores to the planes or stacks that go out the door. To the naked eye much of this looks like textbook QC procedure. But some of it goes deeper. It's the kind of control you associate with a veteran airline pilot whose experience amounts almost to intuition. As pioneers in ferrites and core memory components, we have people like that in control at every vital stage of manufacture.

This is one reason why Ferroxcube can design and build to exacting requirements (example: military stacks that exceed the environmental requirements of MIL-E-16400 and MIL-E-5400). And it's the main reason why every production unit performs like the prototype you approved.

If you specify cores, planes or stacks, talk with the people who pioneered ferrite technology. As a conversation piece, a sheaf of technical literature awaits you. Write for it today.

Ferroxcube

Saugerties, New York



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CIRCLE NO. 10 ON INQUIRY CARD

1,000 Steps per second/800 bits per inch! and this elegant Incremental Recorder is SYSTEM/360 compatible too.

Born to Win

This new incremental/continuous tape recorder was born to be a winner. While last year's tired entrees are busily being "hyped" up to meet the 9 channel 800 bpi requirement, this simple new model from PERIPHERAL EQUIPMENT CORPORATION breezes along in preconceived IBM SYSTEM/360 compatibility.

You see, PEC offers a single capstan velocity D.C. servo drive system with optical accuracy. This unusually wide bandwidth, low inertia drive employs printed circuit motors and single shaft coupling. That's how the truly incremental rates of 350, 500, and 700 steps/second are easily met, with 1,000 steps/second an available option.

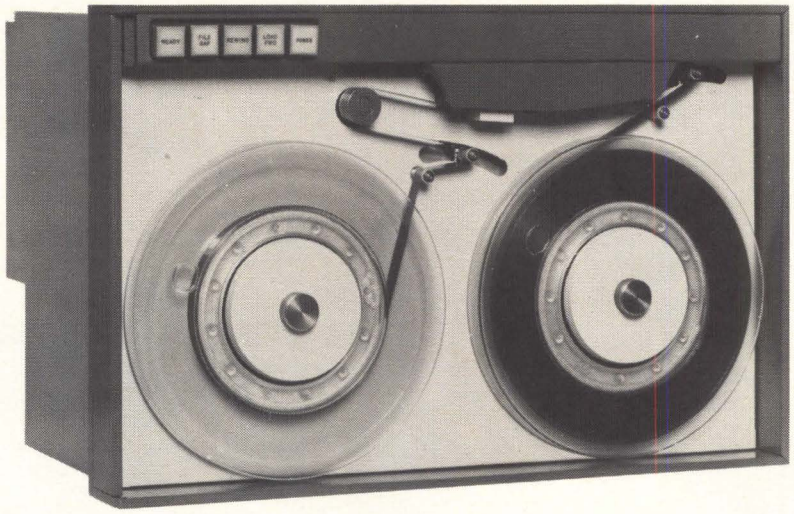
You can say goodbye to those obsolete tired old stepping motor types of incremental recorders that are self-limiting in speed and accuracy.

The Taming of the Skew

This elegant PEC recorder has conquered skew exactly like the *very expensive* computer tape transports.

Do you benefit? You bet you do because you are guaranteed that a magnetic tape written on an inexpensive PEC recorder will read perfectly into your computer transport.

PEC tames the skew in three important ways. With a single capstan drive that eliminates pinch rollers (and skew) . . . with



an optical capstan position encoder which precisely positions data bits . . . and with electronic deskewing at 800 bpi (just like the big boys). A feature which is possible because PEC writes on the fly! And we even guide tape with IBM configuration and tape tension.

Racing Through the Gap

Another time saving advantage. You can race through the inter-block gap in 60 ms (50 ms for SYSTEM/360 compatibility). The gap time is independent of data density and doesn't cost you a penny more . . . compliments of our wideband servo drive.

Elegance in Emptyness

It's the little things that PEC has left out that count. (Those troublesome little things like gear trains, pinch rollers, and other mechanical linkages.) Using IC logic, we have figured out how to design "expensive" circuitry inexpensively. You are the winner. Both on initial cost and continuing maintenance.

Continuous, Too

Not only can this revolutionary recorder prepare SYSTEM/360 compatible tapes at packing densities of 200, 556, and 800 bits per inch *incrementally,* but it can also operate as a continuous recorder or reproducer at any speed up to 25 inches per second. The price saving over the big machines is considerable . . . the performance is even better.

Design PEC in

Data acquisition . . . computer peripheral . . . integrated circuit testers . . . digital plotters . . . pulse height analyzers. If you are designing any of these systems the new PEC incremental/continuous recorder will make your job easier. Phone or write us today.

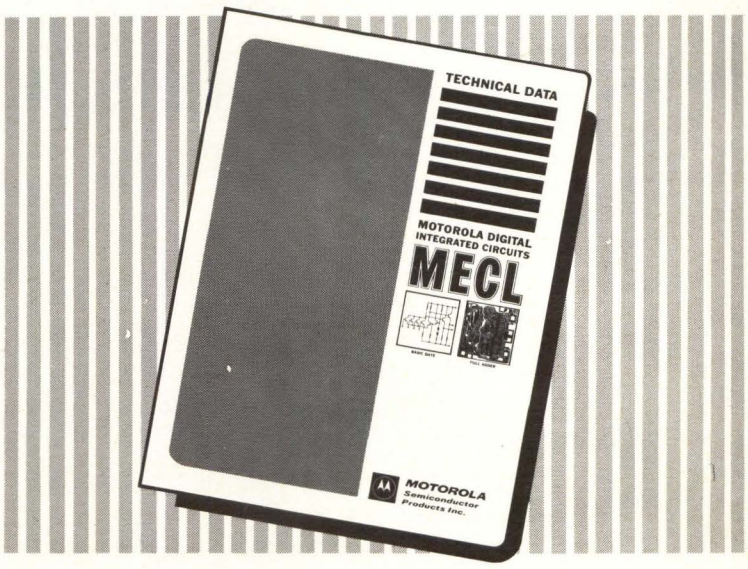
PEC

PERIPHERAL EQUIPMENT CORPORATION

9551 Irondale Avenue ■ Chatsworth, California 91311 ■ (213) 882-0030

CIRCLE NO. 11 ON INQUIRY CARD

THIS BOOKLET CONTAINS COMPLETE DATA, PLUS "HOW-TO-USE" IDEAS FOR THE WORLD'S MOST ADVANCED I/C LOGIC FAMILY!



IT'S YOURS FOR THE ASKING!

Most data brochures contain specification sheets for all of the devices in the line. So does this one — for 56 MECL* II integrated circuits (29 different circuit designs). But, it also includes applications information, right on the data sheet, for each circuit. And, that's not all . . . there's 10-pages devoted solely to the unique and interesting design philosophy of emitter-coupled logic. Then, to make it the highly-practical design tool that it is, this new MECL Data Brochure is designed for perpetual updating . . . New circuit information can be added easily; and, there's room for the MECL 300/350 series brochures that are currently in use.

Yes, the MECL Data Brochure is Extraordinary in many ways . . . but then, so is the MECL line of integrated logic circuits. We felt that the world's fastest, most-advanced full complement line of digital integrated circuits deserved more than just ordinary technical data treatment . . . so, we prepared this special approach for you.

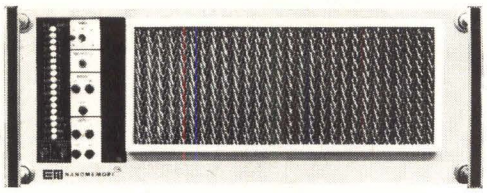
It's Yours for the Asking! Just drop us a line on your company letterhead, at P.O. Box 955, Phoenix, Arizona 85001.

*Trademark of Motorola Inc.

-where the priceless ingredient is care!

MOTOROLA
Semiconductors

This new memory may not do everything better. But it does everything. And it takes up less space doing it.



All together, the specs on our medium capacity memory systems are unsurpassed. Some systems may have slightly faster cycle times, but they don't offer speeds of 650 nanoseconds in a unit that's so small you'll be surprised to find a power supply and tester also included—just like the I.C. electronics and 2½ D magnetics. All are contained in only 2⅝ cubic feet (7"x19"x21.5").

Capacities range up to 295,000 bits per unit. Multiple module capability is available for larger capacity requirements.

Compact as it is, the design doesn't get in the way of maintenance. The systems are extremely easy to repair. Stacks, electronics and tester are on plug-in modules—all are accessible and slip in and out easily.

Information on both the Nanomemory 2650 (650 nsecs cycle time) and Nanomemory 2900 (900 nsecs) are in our compact (8½x11") brochure. Write for Litpak 200.

electronic memories

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(213) 772-5201

CIRCLE NO. 13 ON INQUIRY CARD

If you're interested in working five years ahead of the times, learn about IBM in Washington, D.C. area.

We're working at state-of-the-art levels—and we need programmers and analysts now.

Our Federal Systems Division is involved in a series of real-time projects for the Government that are about as advanced as anything in the field of computer technology today: trajectory analysis, orbit prediction, multi-programming, multiple-access concepts, acoustic instrumentation. And most of this work is being done using the latest computers and peripheral equipment available.

Our positions are located in and around Washington, D.C.—from the convenient downtown area to the gracious countryside near Gaithersburg, Maryland, 15 miles northwest of the nation's capital. Housing and recreational facilities are plentiful. And IBM's generous benefits program is company paid.

Are you one of these people?

We need programmers and analysts with experience in one of two basic areas: information-handling systems and scientific-engineering programming.

Ideally, you should have a Bachelor's degree in Mathematics, Physics, Engineering, Economics, or Statistics. (Equivalent experience in some instances is acceptable.) You should have at least one year's experience.

Contact IBM today

If you're interested in one of the hottest careers going in computer technology, we want to talk to you. Send a brief resume to: Mr. J.F. Ryan, IBM Corporation, Department SC6-M, 18100 Frederick Pike, Gaithersburg, Md. 20760.

It could be the most important resume you've ever written.

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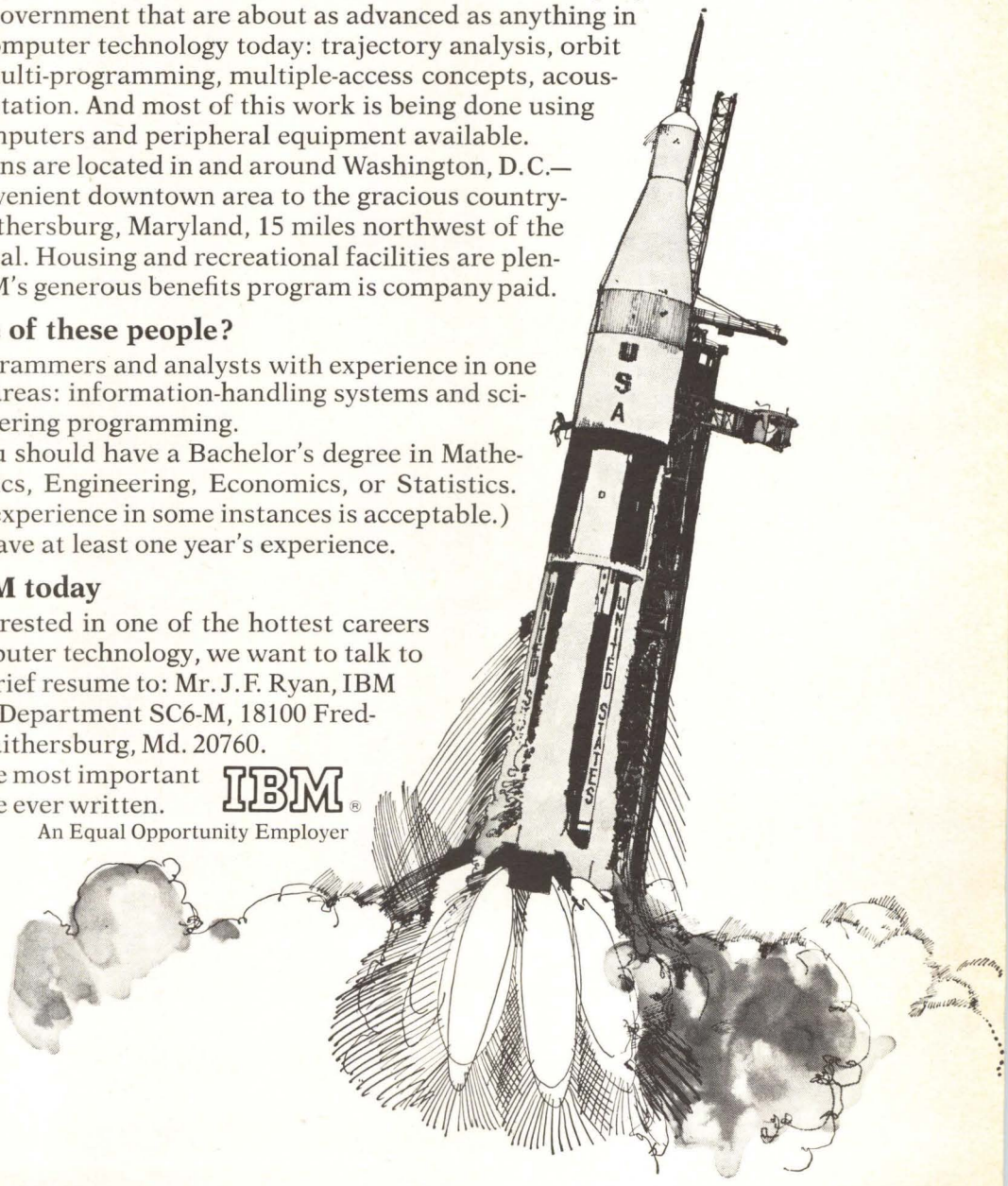
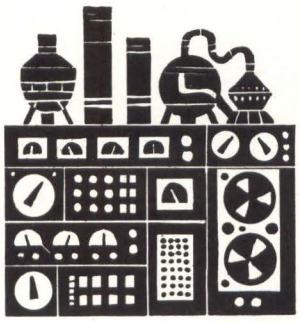




INDUSTRY NEWS

NEWSPAPER TYPESETTING 95% COMPUTER CONTROLLED — The Boston Globe has completed installation of a million dollar computer system to automate hot metal typesetting and photocomposition.

The newspaper installed its second Honeywell 1200 computer, making up the nucleus of what is said to be "the most advanced EDP system in the newspaper field." Both computers have been connected to 20 photo-electric keyboards and two teletypewriters to control printing functions, while other applications are being directed toward financial management, according to Robert J. Heyd, Globe EPD manager.

The keyboards are in the newspaper's composing room and are used to transmit advertising copy and news stories to the computers for automatic formatting and justification. The computers, following the typists' instructions, select the proper type style, size and column width, and handle hyphenation. The copy is then immediately transmitted on a coded perforated paper tape to any of 17 linecasting and photocomposition machines that set the type.

The teletype units, used exclusively for program control, indicate whether the copy was processed and which linecasting machine received it. They also can be used for sending messages from the composing room to the computer.

The most important feature of the Globe's system is that it eliminates the need for entering information into the computers via punched paper tape. Other newspapers using computers must generate a paper tape before the computer can select the type style and font.

Right now, about half the keyboards are running full time. At peak operation, Mr. Heyd said, the paper expects to average 4,000 lines an hour, or about 95 per cent of the total typesetting and photocomposition done by the Globe.

1968 DATA PROCESSING SERVICES — "It is estimated that in 1968 the data processing service center industry in the United States will serve more than 100,000 customers resulting in revenues approaching $800,000,000, while providing jobs for approximately 30,000 people."

These projections, made by Jerome L. Dreyer, executive vice president of the Association of Data Processing Service Organizations, (ADAPSO), are based on a recently prepared economic study of the service center industry which was submitted to the FCC inquiry into the interdependence of the computer-common-communication carrier industries as background information.

"The figures cited," Mr. Dreyer said, "represent an estimated 20% increase in revenue and customers over 1967."

"The development of time-sharing communication-computer systems has opened many new markets. Although no definite information is available, it has been estimated that time-shared systems are presently the most rapidly growing segment of the data-processing service industry," he concluded.

1967 COMPUTER SHIPMENTS ZOOM TO ALMOST $6 BILLION — The value of new computers and related peripheral equipment shipped by American manufacturers to customer locations, both in the United States and overseas, was approximately $5.9 billion in calendar 1967. This represents an impressive 61.2% increase over the $3.66 billion shipped in 1966.

When the value of special-purpose machines, peripherals, supporting services, and supplies are included, the total size of the computer industry comes to more than $9 billion for 1967. For 1968, computer shipments are predicted to be about $6.5 billion, according to the results of a study just completed by the International Data Corp.

"The huge increase in shipments last year reflects the second of the two key step-up years in the seven-year cycle of a computer generation," explains a company official.

"During the next three or four years" he claims, "we can expect a plateauing in the level of computer shipments. Manufacturers will smooth out their present product lines and introduce less expensive equipment that will give them a downward expansion of the marketplace. There was a similar period, naturally at much lower shipment levels, during the period of second-generation computer shipments.

IDC estimates that the $5.9 billion in computer shipments represents 18,700 computers shipped during 1967, and brings the worldwide population of installed computers, made by American-based companies, to 57,600, up 41.9% over the 40,600 machines installed at the end of 1966.

As of December 31, 1967, the company estimates that the value of computers installed in the United States was $13.6 billion, consisting of some 40,100 general-purpose computer systems. Outside the U. S., the value of computers manufactured by American companies — either at plants in the U. S. or at foreign-operated plants, was $5.3 billion, with 17,500 computers installed.

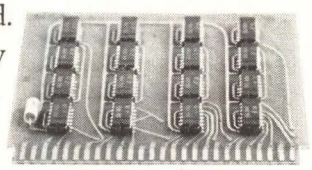
CIRCLE NO. 14 ON INQUIRY CARD

A word to the do-it-yourself module builder:

Don't.

Buy our J Series modules instead.

The J Series is our new family of general purpose, all integrated circuit logic modules. Their performance almost matches that of our famous T Series modules, but they cost about 25% less. They're made to the same dimensions as the T Series, with the same 52 pin connectors, so they're physically interchangeable. We make them for our own seismic recorder systems, so they're rugged and reliable. Now, as of January, you can buy them (complete with mounting hardware, racks and power supplies, if you wish) in any of 25 different functions.



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QUICK...

WE MEAN

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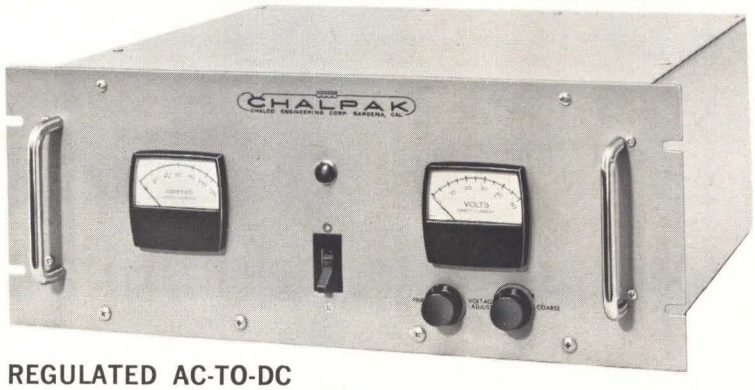

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CIRCLE NO. 15 ON INQUIRY CARD

PLANS FOR EXPANDED SERVICE ACTIVITY — Sperry Rand Corporation's Univac Division plans a major expansion in computing services through a nationwide network of data processing facilities, according to a recent announcement.

Univac has formed a new Information Services Division, headquartered in Philadelphia, that will utilize an integrated system of nationally deployed computers, communication lines, and terminals. The new division is a restructuring of Univac's Data Processing Centers Division, established in 1964, and represents a major expansion of its charter and service activities.

HIGH-SPEED MAGNETIC TAPE DATA TRANSMISSION SYSTEM — Communitype corporation has introduced a 6,000-character-per-minute magnetic tape transmission system designed to provide economical off-line data receiving and sending facilities for a computer operation, and to enable economical, high-speed computer magnetic tape-to-tape data communication over telephone lines.

The system will receive and batch magnetic tape data and translate it to computer-compatible codes recorded on computer-compatible magnetic tape. It also will send computer-prepared data at 1,200 bits per second to magnetic tape systems located at branch office data processing centers anywhere in the world.

Batching of data at the computer location not only permits more efficent use of the computer but also helps keep the data communication lines open throughout the working day, thus providing a real time environment with batch-processing economy.

The device reads and writes on computer-compatible, 7-channel tapes at 556 bits per inch density. Its ½-inch, IBM-type reels have a capacity of 14 million characters at 556 bpi. A 9-channel, 800 bpi version, designed for use with the new IBM-360 computer series, is presently under development by the company and will soon be made available.

NEW GOLD CROSSOVERS INTERCONNECT INTEGRATED CIRCUITS — A reliable new structure for interconnecting integrated circuits — an air-insulated, beam-lead crossover— has been invented by Bell Telephone Laboratories. The crossover is said to have a higher

breakdown voltage, greater reliability, and lower capacitance than conventional interconnection structures.

The new structure has been used successfull both in experimental integrated circuit chips and in larger, more complex substrates. Such circuits and substrates are expected to be used broadly, in electronic switching systems, telephone sets, and many other types of telephone equipment.

Where two conductors must cross, a gold beam lead is formed into a 10-micron-high "microbridge" over the lower conductor. The two conducting paths are separated by a thin layer of zirconium oxide and an air gap. This dual dielectric insulation can withstand over 200 volts, is immune to "pinhole shorts" through the dielectric, and has very low capacitance.

In conventional interconnection structures, the top conductor is deposited directly on a dielectric (usually silicon dioxide) that separates the crossing conductors. Because the top conductor is formed in intimate contact with the dielectric, any pinholes in the dielectric can cause short circuits between the two conducting paths.

In the new structure, however, any pinholes in the zirconium layer are harmless, because the top conductor is plated on top of a spacer that is later etched away. The resulting air gap insulates the top conductor from the zirconium layer, which is heated to form zirconium oxide, the other half of the dual insulation.

The new crossover will not fail even if the top conductor is pushed down to the bottom level, because the zirconium oxide alone can withstand 100 volts. The top beam lead will spring back to its original position as soon as the extenral force is removed.

The crossover is formed by depositing layers of zirconium and copper over the bottom conductor, and then plating the gold beam lead on top of the copper. Next the copper is etched away to form the air gap, and the whole structure is heated to 350° centigrade to convert the zirconium layer into zirconium oxide. The last step does not affect the rest of the integrated circuit, because silicon does not oxidize at this temperature.

The new crossovers have been fabricated on experimental integrated circuits with high initial yields. Hundreds of the crossovers have been aged in room air at 350° centigrade for over 1000 hours with no apparent change.

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WE MEAN

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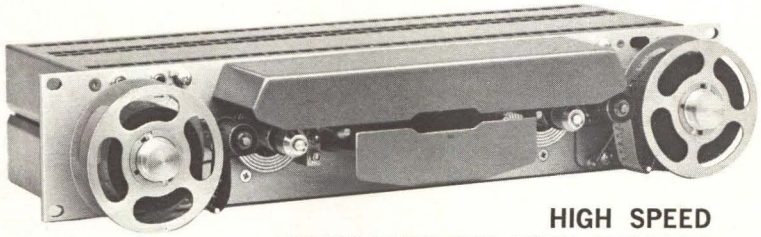

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Occupies only 3½" of panel space ☐ Spoolers for 200 to 1,000 feet of tape ☐ Operates asynchronously at any rate between 0 and 150 cps ☐ Slews at 600 cps and stops "on character" ☐ Lamp is unconditionally guaranteed for 1 year.

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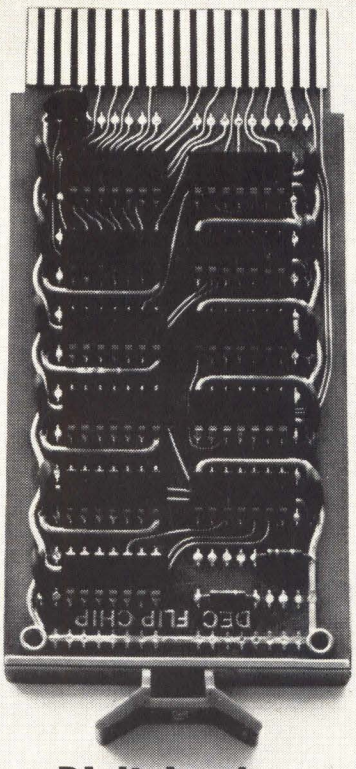

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CIRCLE NO. 17 ON INQUIRY CARD

READER FOR PUNCHED OR MARK-SENSE DATA — Motorola Instrumentation and Control Inc., Phoenix, Ariz., a subsidiary of Motorola Inc., will display a new, inexpensive desk-top reader for acquiring data from mark-sense documents, mark-sense cards, punched cards, or combined mark-sense/punched cards, at its booth, No. AA, at the Spring Joint Computer Conference, April 30 - May 2, Convention Hall, Atlantic City, N. J.

The new MDR-1000 reader provides a simple means of entering into a data processing system, in computer language, data marked or punched on cards or marked on standard 8½" x 11" documents. Cards can be fed into the new device singly or automatically in batches of up to 500 with an optional automatic hopper. It thus offers systems designers a new, low-cost method of getting raw data, right from the source, without need for skilled data processing equipment operators. In addition, the unit is small enough (16¾" wide by 16¼" deep by 9¾" high) to fit almost anywhere.

The reader produces a standard USASCII output that is compatible with standard telephone transmission interfaces for long-distance transmission or directly with standard data processing equipment, such as teletypewriters, tape recorders, or computers.

TRADITIONAL? SURREALISM? AVANT GARDE? — For lack of a better word, it's called computer/plotter art, a little known but increasingly important art form which was demonstrated at an informal showing held at the New York room of the Statler Hilton, Los Angeles, (2/29/68).

Around the walls were hung approximately a dozen framed drawings in color, and black and white, both original drawings and reproductions of masterpieces, the products of a collaboration between computers, a California Computer Products, Inc., Plotter, and, of course, human beings.

The showing was held in conjunction with the announcement by Calcomp that it is sponsoring an international "computer/plotter art" competition by offering scholarships of $5000, $3000 and $2000 to accredited colleges or universities named by the winners, plus cash awards of $500, $300, and $200 with additional awards of $50 each to 50 runners-up.

Judging the contest, which will end on November 1, are Anthony La Rotonda, art director of Parade Magazine, Arnold C. Holywell, acting art director of Time-Life Books, and Peter Fingesten, editor of the Pace College (New York City) art department. Winning entries will be exhibited at leading art galleries and museums throughout the country.

Computer/plotter art has been hitherto little known except within the technical world. Increasing refinements, however, have produced beautiful pictures, so much so that the drawings, both originals and reproductions, are now being sought by collectors.

The CalComp Plotter, of course, is engaged in more materialistic pursuits such as generating garment patterns of various sizes from the designer's original pattern at a fraction of the time formerly required, producing contour maps for oil exploration, and a variety of other uses applicable to industry. Information on the awards contest and entries can be obtained by writing to California Computer Products, Inc., 305 North Muller Street, Anaheim, California.

WESCON TO PRESENT 'HYBRIDS' SYMPOSIUM — A two-day lecture program on designing with hybrid microelectronics has been confirmed as a special feature of WESCON week in Los Angeles next August.

It is the second of the concurrent symposia announced for WESCON. The 1968 International Electronic Circuit Packaging Symposium has been set for August 19 and 20 at the Statler Hilton Hotel, and the "hybrids" series will follow at the Statler on August 21 and 22. WESCON's own four-day technical program of 25 sessions will be held at the nearby Biltmore Hotel.

The 20 lectures on designing with hybrids are being organized under sponsorship of the IEEE Parts, Materials and Packaging Group. Wayne Martin, Radio Corp. of America (Aerospace System Division) is co-chairman of the series with S. M. Stuhlbarg (Raytheon), who was chairman of the 1967 WESCON symposium titled "Microelctronics Comes of Age." Like that program, the hybrids series will be a compact, follow-on version of an eight-week lecture program currently in presentation at MIT.

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70% to 90% efficiency? ?	Instant fault repair by plug-in module replacement? ?	Add-on power capability by using more modules? ?	Ability to handle full load steps while maintaining out put in regulation band? ?

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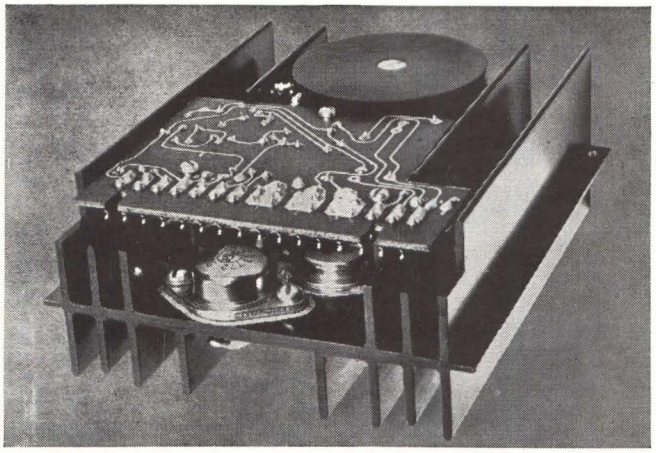
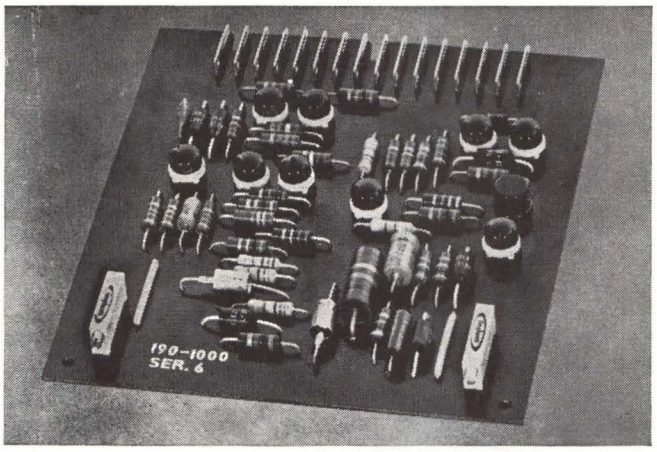


Omnimod power control module.



Omnimod control amplifier.

OMNIMOD gives you all these features—*and* more—*and* at a lower price! Want to know more?

OMNIMOD is a dc to dc converter using transistors in a CONSTANT PULSE WIDTH, variable repetition rate switching mode to regulate output voltage or current. Two small plug-in units make-up the OMNIMOD concept—a power control module and a control amplifier.

Output can be regulated between ± 2 and ± 60 dc at up to 20 amperes using the OMNIMOD family of modules WITHOUT MODIFICATION OR ADJUSTMENT. Higher current ratings are obtained by paralleling power control modules.

Any number of power controller modules can be controlled by one amplifier. OMNIMOD has a current limiting parameter, over voltage protection, voltage sequencing, and remote sensing.

To design a custom power supply, one must simply

1. design one input power converter to change unregulated line ac power to unregulated dc power

2. select the number of plug-in OMNIMOD power control modules to supply the power needed for each output

3. package these elements with filter capacitors and a plug-in amplifier module for each output

All the power used by every element in a typical data processing system could be supplied by custom power supplies constructed with interchangeable OMNIMOD modules.

Isn't this enough to consider OMNIMOD for your custom requirement? We will design an OMNIMOD custom power supply to your specs, or will help you design your own system using our plug-in OMNIMOD modules.

Write for the complete story. We'll have it to you within 48 hours.

CONTEMPORARY ELECTRONICS

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CIRCLE NO. 18 ON INQUIRY CARD

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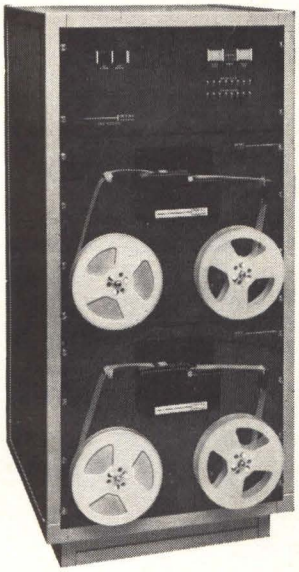
DUPLICATORS, VERIFIERS, and CODE-CONVERTERS



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INDUSTRY'S FIRST BI-POLAR LSI ARRAY WITH 2-LAYER METAL — The industry's first bi-polar large scale monolithic array incorporating two-layer metalization is now available from Fairchild Semiconductor. Termed the 4500, this unit is the first of a full line of bi-polar and MOS arrays planned for introduction by the firm during 1968. Because of the custom interconnection between cells and parts of cells inherent in the Micromatrix technique, the 4500 is capable of producing a wide variety of CCSL compatible logic functions.

The 80 x 110-mil chip used in this unit is a 2 x 4 array containing eight distinct cells. A cell is subdivided into quarter cells, each of which is a four-input DTL NAND logic gate. For additional logic flexibility, each quarter cell has three further logic options: input AND expansion, internal OR expansion, or output open-collector.

Fairchild's Micromatrix approach uses a complex array of two-dimensional multi-gate building blocks or cells. Each cell contains a set of components that may be individually specialized by cell intraconnects to become one of a variety of fundamental logic building blocks (NOR, NAND, flip-flop, latch, etc.). By means of the two-layer metalization process, the cells may be interconnected to form a complex subsystem logic function analogous to the interconnection of conventional integrated circuits on a dual-sided printed circuit board.

IMPATT DIODES CONNECTED IN SERIES FOR INCREASED POWER — IMPATT diodes have been connected in series to provide a power output which is the sum of the individual diode outputs. These diodes produce negative resistance at microwave frequencies based on a combination of avalanche current multiplication and transit time delay. While parellel connection has been used in the past, this is the first time the diodes have been connected in series. Although the power output is theoretically the same in both cases, the series connection offers the advantage that the combined structure works at a higher impedance level.

The result of these experiments was reported by F. M. Magalhaes and W. O. Schlosser of Bell Telephone Laboratories in a paper presented at the 1968 International Solid-State Circuits Conference in Philadelphia, Pa. To demonstrate that IMPATT (IMPatt Avalance and Transit Time) diodes can be operated in series, three packaged 4.5 GHz diodes were placed in a coaxial cavity and biased in series. With approximately 250 milliwatts output each, the diodes provided 750 milliwatts of continuous wave output. This indicates that medium power millimeter-wave IMPATT oscillators with reasonable impedance levels are now foreseeable.

Virtually no significant drop in the power output was observed even when the spacings between the diodes were varied considerably. This consistency of output is due to variations in negative resistance with respect to rf current through the diodes. Also, since the spacing can be made relatively large, it becomes easier to extract heat from the operating diodes.

From the experiments, it was concluded that it is possible to operate IMPATT diodes in series. Also, because spacing between the diodes is not critical, it is possible that similar series connections are applicable to millimeter wave oscillators.

DATA COMMUNICATIONS SUBSYSTEM — Multi-line communication between the UNIVAC 9200 and 9300 computers and remote terminals is the function of the new DSC-4 Data Communications Subsystem announced recently by Sperry Rand Corporation's UNIVAC Division.

The DCS-4 can be employed with wideband (Telpak) service at speeds up to 230,400 bits per second (9200 communication is limited to 50,000 bits per second), telephone lines at up to 2400 bits per second, and telegraph lines at up to 150 bits per second.

With one DCS-4, concurrent communication is possible over up to four lines. With two DCS-4's, communication can be established over up to eight lines (telephone and telegraph line combinations only).

A UNIVAC 9000 series computer equipped with DCS-4 can communicate with the following UNIVAC systems — 418, 494, 1107, 1108, DCT 2000, 1004, 1005, Uniscope 300, as well as with Teletype remote devices.

A feature of the DCS-4 is that processor functions, including magnetic tape reading and writing, can be overlapped with communication at voice-grade and telegraph rates. Deliveries of the DCS-4 are scheduled to begin in the Fall of 1968. The price for a DCS-4 configuration serving four telegraph lines will be $522 per month or $19,155 purchase.

LOGICALLY THERE IS NO OTHER CHOICE THAN THE MODEL PDC 808

- Available off the shelf for $6,600
- 4,096-word core memory, expandable
- Parallel processing
- Fifty-eight basic instructions
- 24-μs ADD
- Two priority interrupt lines
- 8-bit word length
- Extremely powerful and flexible I/O system, easily interfaced

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CIRCLE NO. 20 ON INQUIRY CARD

"Time Sharing" is presented in its most general sense as any application of a computer system that involves simultaneous users. Concepts and equipment of time-shared systems are defined and described and criteria for system configurations are given in terms of application requirements.

FUNDAMENTALS OF TIME-

This is the second and concluding section of the article by C. Gordon Bell which appeared on pages 44 through 59 of the February issue of Computer Design. The first section discussed the hardware of time-shared computers and suggested advantages of time sharing. This section discusses operating system software and user components and includes an extensive bibliography on time sharing.

OPERATING SYSTEM SOFTWARE

Operating system, monitor, supervisor, and *executive* are names given to those processes that supervise and control the operation of the system for all users.

Unlike conventional operating systems that are static, a Time Sharing Operating system is growing and dynamic. New procedures may be added continuously.

The additional languages and facilities have a structure that may have a rather complex operating system as a major part of the language. For example, consider the administration of a teaching program. The program would undoubtedly schedule its users (pupils), and the hierarchy of the whole system would be: the operating system for the entire computer managing a central teaching program to manage all courses managing a course teaching program which would manage all individual users taking the particular course.

The objectives of the system software are:

1. Provide many user functions or facilities with easy-to-use processes.
2. Effective or efficient hardware utilization. Perhaps allow users to utilize the hardware directly. Provide special user services which utilize special hardware.

The criteria for the design might:

1. Meet the requirements for Time-Sharing (computer time and memory space) per user.
2. Provide for flexibility in the operating system using modular construction. Individual components can be independently designed, tested, and modified (or improved). If possible, the system components should be written as user processes.

In general, all systems are constrained by cost considerations. A special system may concentrate on a single objective, while a general system is forced to find a balance between many objectives.

The system software contains:

1. System data base, or information necessary for system management, and management procedures.
2. Resource allocation, control, and management procedures.
3. Common procedures or processes for the users, the library.
4. Miscellaneous elements: System initialization and shut-down; error recovery; file backup; creation of new system; and system debugging.

OPERATING SYSTEM DATA BASE

The operating system requires a large data base that is retained in primary memory and in files. Back-up files (copies of files) must be regularly written so that the system can be restarted in a correct state in the event of system failure.

The data for a user include: his memory map or process location, generally found in primary memory while running or active; the processor status (the location counter, processor flags, accumulators, index registers, etc.); identity information (name, number, project numbers, etc.); the time used, allotted, last run, etc.; the run state (e.g., presently running, waiting to run, requiring special service, waiting for file transaction, terminal action, additional memory, etc.); permanent user data to allow the assignment of terminals and file space; accounting information; system temporary storage to enact user requested procedures; and active terminal and file buffering storage.

SHARED COMPUTERS

by
C. GORDON BELL

Associate Professor of Computer Science and
Electrical Engineering, Carnegie Institute of Technology.
Formerly manager of Computer Design, Digital Equipment
Corporation, Maynard, Massachusetts.

In addition to the data base associated with each user there are inherent data associated with system components and resources. These include: hardware status and availability information; terminal names; file directories including descriptors of abilities, modes, etc.; primary memory free space; and file memory free space.

Historical, statistical, and accounting information are also kept, and historical or activity data provide tools for system improvement. They especially aid scheduling and memory allocation as well as indicate the system balance and load.

RESOURCE ALLOCATION, CONTROL AND MANAGEMENT

This responsibility includes: processor time or scheduling; process space (primary memory allocation) and assignment of a process to secondary memory or files; file space; and terminal/process/user allocation and assignment.

The two extreme philosophies that determine the number of users a system can have are "denied access" and "degraded service." "Denied access" provides for a fixed number of users, each of which will obtain a known or worse case response. "Degraded service" provides for more users and the service is at least inversely proportional to the number of active users.

Scheduling

The assignment of processors to processes is *scheduling*. The scheduling algorithms that compute the time a process is to run usually use the following input parameters: previous time used; memory space occupied; status of terminal or file data transmission; expected response time for the user; user information; and number of users.

The priority information available includes the user, his urgency, and willingness to pay. As economically realistic systems that charge for their actual uses come into existence, users will be able to get a broader range of service.

The round robin algorithm runs each user, in turn, for a fixed quanta of time, and when all users have been served, the process is repeated. If any user cannot run because he is waiting for input or output, or halted, he misses a turn. On completion of input or output the user is put at the head of the queue and run (subject to his allotted time).

The scheduling algorithm is a most subjective system component, and, therefore, might be written in a form that can be easily modified. How, when, and which components call the scheduler is also important.

Memory Allocation

Primary/secondary memory allocation occurs as users make demands for more space the system activates user processes. The hardware memory allocation scheme of Table 2 constrains the user map organization, and the process organization. This hardware constrains the user procedure with restrictions ranging from writing in interpretive languages; writing at particular addresses or using a convention determined index register as a base register; writing with no restrictions (over the basic machine); and finally providing a two-dimensional addressing space.

The memory paging-memory segmentation hardware will drastically influence future program structure and design. With two-dimensional addressing, the user is not required to manage primary memory, and is free to address data by two logical numbers rather than by physical numbers. (With such freedom, and ability one might expect a proportional cost.)

File Allocation and Control

File allocation and control are generally subject to extra-system constraints on the basis of user-size-restriction tables.

File allocation cannot easily be separated from detailed file management. The management includes the service of detailed user requests for data, while allocation

is concerned with broader control of all file space.

Hardware's View of Files. The hardware parameters that affect file organization are: the hardware access time for words or sectors of the file; the word or record transfer time; the size of the records transferred; the total file size; and the file failure rate.

Operating System's View of Files. The apparent file parameters are: the size of files; the number of users and number of files per user; the access time to segments of a file; the nature of addressing the file information (sequential or random accessing); the file index; and the file data buffering.

File activities can be divided into operations: naming, or declarations, inter-file manipulation, intra-file utilization, and file closing.

User's View of Files. Parameters associated with the directory or index of files for users provide a means of controlling a file's activity, flexibility, general usage, name, users, record of its activity, and actual location of the file components. File accessibility control for the user is on the basis of the originator (owner), group, and public. The modes of file activity include read/write, read only, execute only (a procedure), and denied access. Other information about file access includes creation date, number of times used, last time used, times modified, etc. The user requests of functions for utilization include: reading, writing, naming, re-naming, deleting, appending, inserting, providing access restrictions, obtaining statistical information, or in general, any operation that can be done with the data in or about a file.

Terminal Allocation

Terminal allocation in general systems is either on a first-come-first-served basis or on a completely reserved basis. Requests for terminal reservations are via a control terminal, and as a job is initiated, the terminals required for job completion are requested. The terminal is the means by which a process is

TABLE 2. MEMORY ALLOCATION METHODS

Hardware Designation	Method of Memory Allocation Among Multiple Users	Limits of Particular Method
Conventional computer — no memory allocation hardware	No special hardware. Completely done by interpretive programming.	Completely interpretive programming required. (Very high cost in time is paid for generality.)
1 + 1 users. Protection for each memory cell	A protection bit is added to each memory cell. The bit specifies whether the cell can be written or accessed.	Only 1 special user + 1 other user is allowed. User programs must be written at special locations or with special conventions, or loaded or assembled into place. The time to change bits if a user job is changed makes the method nearly useless. No memory allocation by hardware.
1 + 1 users. Protection bit for each memory page.	A protection bit is added for each page. (See above scheme.)	No memory allocation by hardware.
Page locked memory	Each block of memory has a user number which must coincide with the currently active user number.	Not general. Expensive. Memory relocation must be done by conventions or by relocation software. A fixed, small number of users are permitted by the hardware. No memory allocation by hardware.
One set of protection and relocation registers (base address and limit registers). Bounds register.	All programs written as though their origin were location 0. The relocation register specifies the actual location of the user, and the protection register specifies the number of words allowed. (See Fig. 7.)	As users enter and leave, primary memory holes form requiring the moving of users. Pure procedures can only be implemented by moving impure part adjacent to pure part.
Two sets of protection and relocation registers, 2 pairs of bounds register.	Similar to above. Two discontiguous physical areas of memory can be mapped into a homogeneous virtual memory.	Similar to above. Simple, pure procedures with one data array area can be implemented.
Memory page mapping*	For each page (2^6-2^{12} words) in a user's virtual memory, corresponding information is kept concerning the actual physical location in primary or secondary memory. *If the map is in primary memory, it may be desirable to have "associative registers" at the processor-memory interface to remember previous reference to virtual pages, and their actual locations. Alternatively, a hardware map may be placed between the processor and memory to transform processor virtual addresses into physical addresses. (See Fig. 8.)	Relatively expensive. Not as general as following method for implementing pure procedures.
Memory page/segmentation mapping	Additional address space is provided beyond a virtual memory above by providing a segment number. This segment number addresses or selects the page tables. This allows a user an almost unlimited set of addresses. Both segmentation and page map lookup is provided in hardware. (See Fig. 9.) May be thought of as two dimensional addressing.	Expensive. No experience to judge effectiveness.

intiated and requests for additional terminals, primary memory, time, etc., are made through it. It is the medium for job control.

Resource management deals with servicing user demands after resource allocation has occurred. It is imperative to provide users with a system that requires little or no knowledge of particular device or terminal idiosyncrasies. Even though terminals have differing characteristics it is desirable for the system to provide users with a single basic set of characteristics. More flexible terminals would, of course, leave abilities in access of the common characteristics which could be utilized. On the other hand, it is important to allow users the freedom to control special terminal activity directly. This is particularly necessary in mixed experimental-production systems involving terminals that differ widely. For example, in flight simulation systems, the usage may range from program debugging, new terminal hardware-software debugging, and simulation.

The terminal characteristics are: speed or data rate of the terminal; amount of primary memory used for buffering and the location of the buffers; system overhead time for data requests, including processing time required for the data; and device data acquisition modes, and terminal data usage. Detailed terminal management includes the process that buffers data from the terminal and synchronizer user demands with terminal performance.

SYSTEM-PROVIDED PROCEDURES AND PROCESSES

In addition to providing the software framework within which users operate the hardware, the system also supplies many of the processes for a user. That is, the system includes a library of procedures for arithmetic function evaluation, special and procedure oriented language translations, computer aided instruction, file data conversion, text editing, program debugging, fact retrieval, simulation, etc. In fact, the difference between a user and a system process is that a user process can be altered.

The method of calling these procedures (or job setup) and the ability to have a hierarchy of procedure calls is important. A system-supplied procedure can be considered an extension of the system and called with the same mechanism with which a user would request file or terminal activity. In fact, the hardware instructions that provide communication between the system and the user should also be used for procedure calls. In this fashion, the system can conserve memory space by not providing duplicate copies of routines that are in use by multiple users. The data or temporary storage required by the system while enacting a procedure on behalf of a user is part of the user's memory. This structure conserves space both for users of small subroutines (e.g., arithmetic, data conversion, etc.) and large programs (translators, text editors, etc.).

A set of commands might include programmed floating point arithmetic (for a small system), common arithmetic functions, complex arithmetic, string processing, data conversion and operating libraries for the language translators, translators, editors, loaders, etc. Also desirable is the facility for a user to define and call his own functions in the same hierarchy and framework.

MISCELLANEOUS SYSTEM FUNCTIONS

These processes include record keeping, the periodic recording of the system state for backup, error detection, error recovery, error handling for a device, and communication with the user terminals for system requests.

The system clock is a part of the operating system that provides the actual time base and is used by the scheduler and the accountant, for example, to carry out their functions.

System start-up and shut-down procedures are necessary for initialization of system and the recording of history. Parts of the system can be written as pseudo users. This allows functions like data gathering and system analysis to go on by watching the system rather than being embedded in it. This operation is obtained by defining monitor instructions that allow a user to obtain behavioral characteristics on demand.

A debugging system for the operating system might have the following features: ability to examine or alter; ability to dump or save the complete system in the event of a "crash"; ability to control the substitution of a "new" system for the present one, etc. These features are extensions of a normal on line debugging program.

EXAMPLE OF TIME SHARING SYSTEM FOR THE DEC PDP-6

Figure 10 first presents a simplified view of the system in terms of the memory map of the user and operating system, together with terminals and files. The system runs either as a multi-programming or multi-programming/swapping system depending on whether a secondary memory device is available for program swapping.

A job for a user can be viewed as an area of memory which it occupies while running and I/O

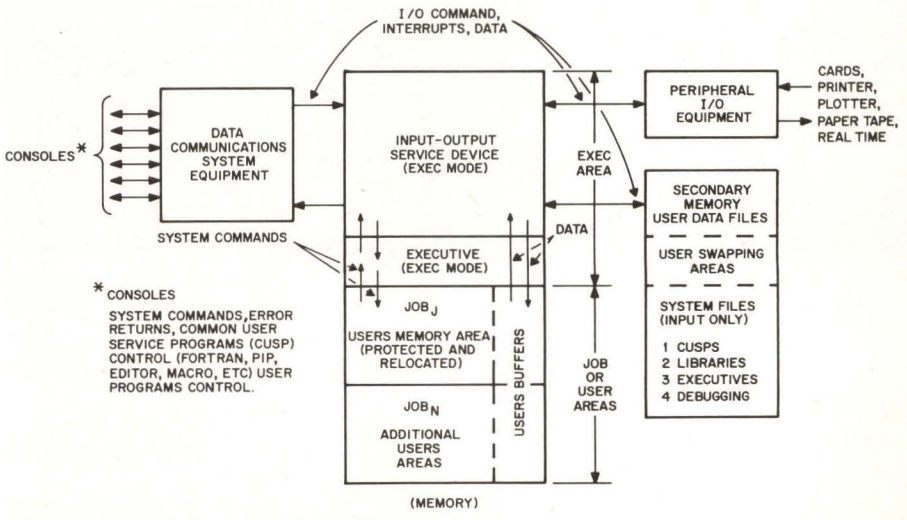


Fig. 10 PDP-6 Multiprogramming System Diagram. (Courtesy of Digital Equipment Corporation.)

equipment assigned to the job, including the user's files and terminals. The operating system software has four main modules: the system files (e.g. FORTRAN, assembler, language translators); terminal control; file control; and the main body of the executive.

Figure 11 gives a more detailed view of what a user program looks like. The user program (e.g., a common user program such as a Fortran Compiler) has its own executive system which communicates with the operating system. The user executive translates user commands from a console into operating system commands for file and terminal activity, while the actual Fortran compiler only accepts input data and produces output data. The user executive is responsible for making it possible for the compiler to read and write files.

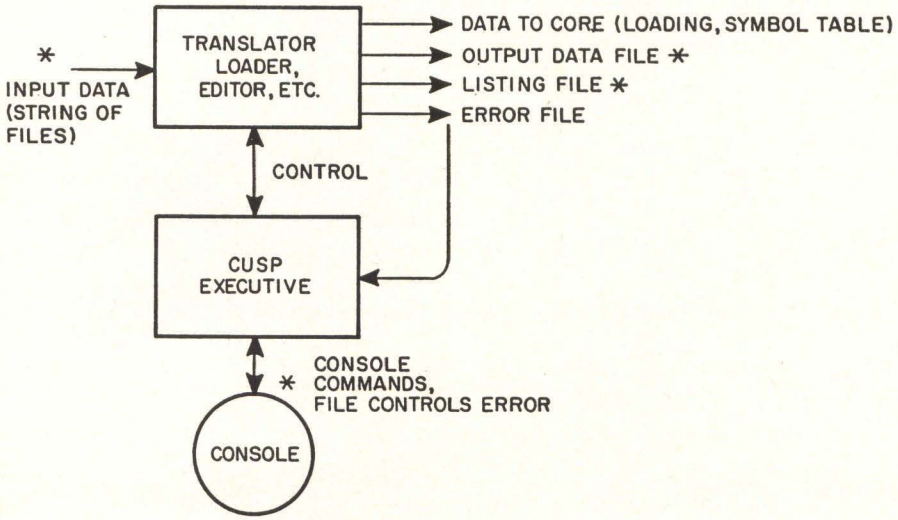


Fig. 11 General structure of common user service program (CUSP) for PDP-6. (Courtesty of Digital Equipment Corporation.)

Figure 12 shows a memory map of a user's program. The space can grow (and contract) as the program is running, since a user program may make requests to the operating system for space. The first main area, that reserved for operating system parameters, is 140_8 long and is available to both the user and the operating system, although special commands must be given to the operating system to change it. The other areas are a function of what programs are being run.

The system's part of the user's job area contains temporary registers which store the processor state while the job is not running. These include:

1. Two groups of 20_8 registers to store the accumulators or general registers (AC's).
2. The Program Counter (PC) and processor flags.
3. The program's location or boundaries.

The registers that hold the organization to a particular program include:

1. Starting address of the program.
2. Starting address of the debugging program, DDT.
3. Location of various blocks in the user's area, i.e., the symbol table, free storage space, etc.
4. Assignment of I/O device names to numbers, so that a device can be referred to by name rather than on an absolute basis ($2 \times 20_8$ locations).

The registers used as working storage for the system include:

1. The STACK, a pushdown area of temporary storage, and stack pointer.
2. Input-Output data Buffers.
3. Job number.

User requests to the monitor are handled via a defined set of instructions which are called the un-used operation codes, or Programmed Operators, or UUO's. Any time the user program makes a call to the system for service it is via these instructions.

The loader is a system routine that is placed in the user area initially and loads the various subprograms required into the user area. The loader links all symbolic references together and fetches needed library programs.

Figure 13 presents a memory map of the operating system which shows the kinds of program modules in it, together with some of the communication paths. The modules perform the following functions:

Job Status Table holds the state of each job in the system, whether a job is in core or residing within a secondary memory prior to running. The state is defined by several words and includes its condition for running, the time it is used, and the location of the job (which includes more status information).

IO Device Service exists for each peripheral device, and the module manages the transmission of data between primary memory and the device, the initiation of the device, and the processing of error or unusual conditions associated with the device (e.g., re-read trys for magnetic tape).

File Directory and File Free Storage Control is used with devices that have named files and directories. It provides the ability to enter new file names and delete files, and it manages the file's free storage.

Error Handling is a common routine that may be called whenever a job (or the monitor) detects an error. A notice of the error is passed on to the user at his console (or to his program), and the job status may be altered.

Run Control is called by other programs and is just concerned with starting and stopping a particular job.

Core Allocation is a common routine responsible for knowing the location of free core in the system and when told, it reserves core blocks.

Clock and Clock Queue are common routines that accept requests for future notification from other parts of the monitor. The clock (more correctly, a timer) notifies the caller at a specified future time.

(For example, the timer is called by the scheduling program so that the scheduler can be activated to schedule the next job.)

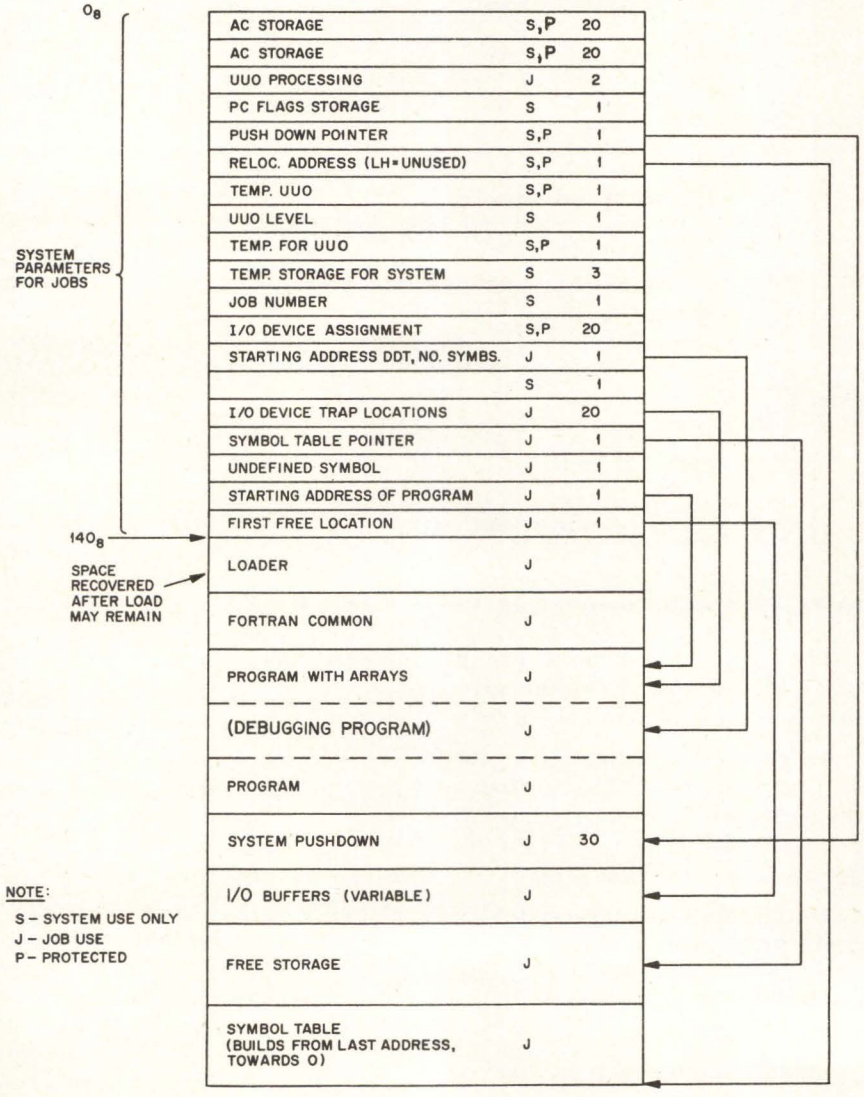
Scheduler makes a decision about the number of the next job to run, based on the variables associated with the system's state (each job status, time, core, etc.).

Programmed Operator Dispatcher processes the instructions that are given by the user program to the executive system. The dispatcher looks up the instruction in a directory, does common pre-processing, and passes control to the appropriate part of the monitor. Some of the instructions are defined by a mnemonic call name. A Call table is hash coded with the name, and corresponding monitor address for the processing.

Command Decoder processes console requests and decides the system routine to call.

Console Command Processors include the programs for actually processing the user console requests (or a user program request). These include programs for log in, save job, start, stop, assign a device, etc. Some programs may not be resident, in which case they are loaded and run in a fashion similar to that of a user program.

System Initialization starts the system just after it is loaded, and includes the freeing of devices and the initialization of all variables.



PDP-6 USER
JOB AREA STORAGE
(COURTESY OF DIGITAL EQUIP. CORP.)

Fig. 12 PDP-6 user job area storage. (Courtesy of Digital Equipment Corporation.)

System Debugging Program is a version of the debugging program, DDT, and may be loaded with the system. It can be used in the event of system failure, to interrogate the state of the system, and includes facilities for preserving the system for future examination.

System Maker allows a complete new monitor to be made as a user program, and when called will copy the new monitor into the area occupied by the old monitor and transfers control to the new monitor.

USER COMPONENTS

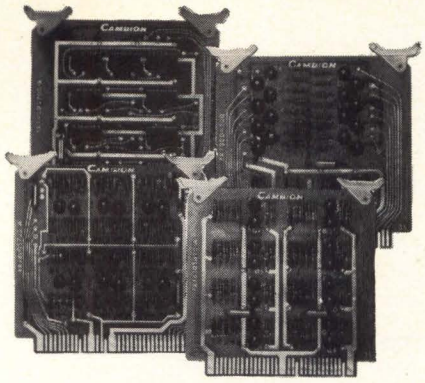
TERMINALS

Communication among the terminal, system software, and user process is very important because of process time, memory space, ease of use, and design modularity considerations. "Human engineering" design aspects include those that affect a user's apparent or actual response.

Although there are many aspects of terminals and their design, the following terminal unit groups will be used:

1. Typewriters.
2. Text—Keyboard Displays. (Text cathode ray tube displays with keyboard inputs)
3. General Graphic Displays or Consoles.
4. Direct Terminals.
5. Indirect Terminals.
6. Specialized Terminals.
7. Machine Links.
8. Peripheral Computers.
9. Other time-sharing systems or computer networks.

The parameters that are common to all terminals and that present the user with certain apparent characteristics have been discussed in the hardware section. The physical data transmission modes, character sets, speed, etc., and general appearance differ among terminals, but the "apparent" characteristics to a user program can be nearly constant, so that user programs can be written independent of their environment or terminals they use. The operating system software is responsible for translating basic user requests into common commands that operate the hardware.



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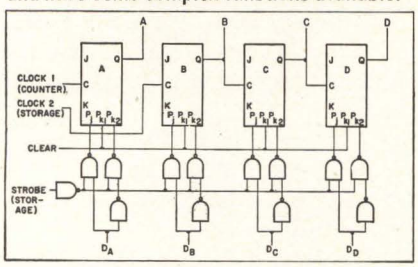

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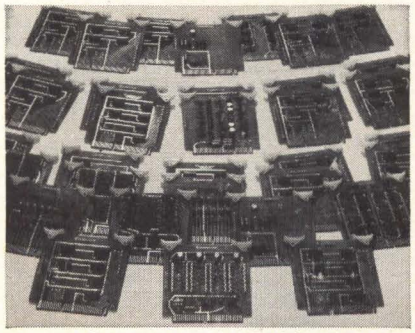

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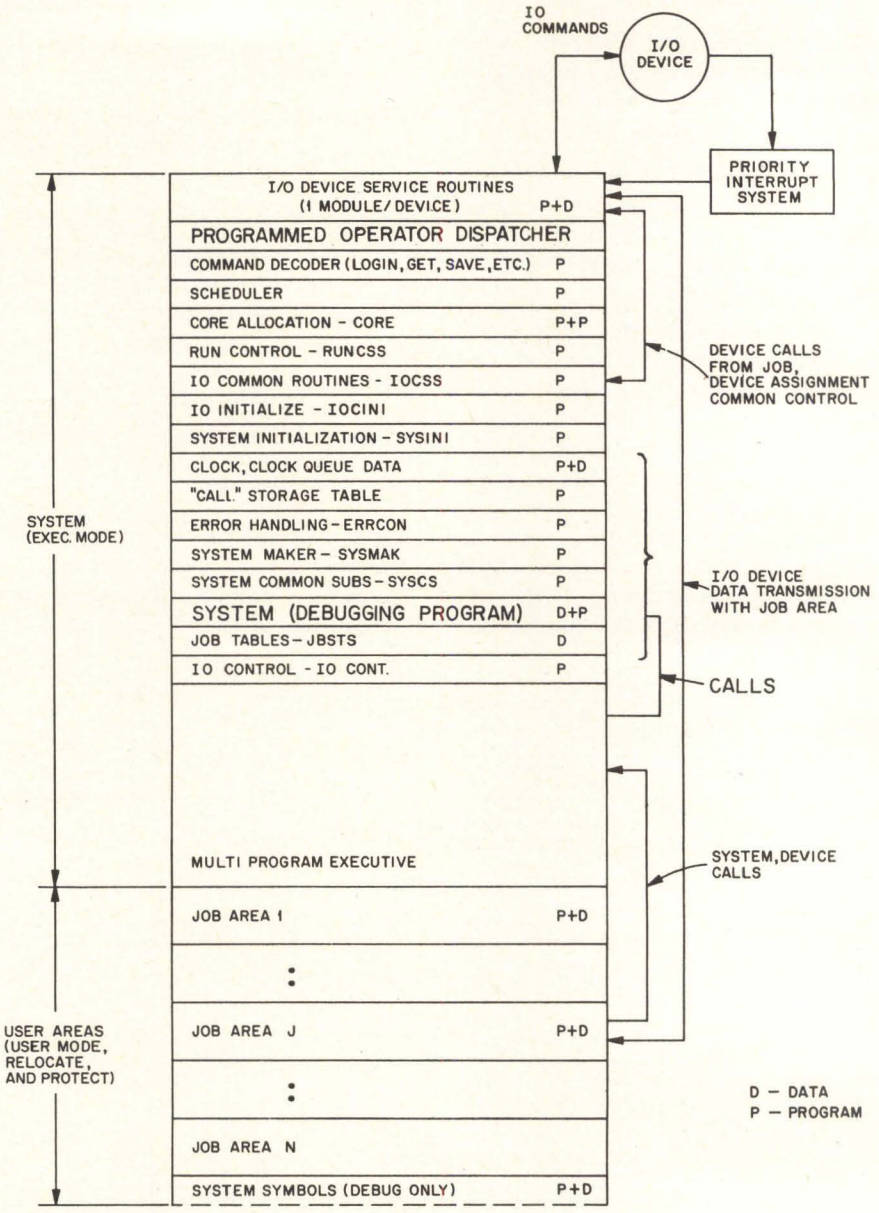


Fig. 13 PDP-6 Multiprogramming System Storage. (Courtesy of Digital Equipment Corporation.)

The typical commands or instructions a user program gives that deal with a terminal include:

1. Assignment of terminal to a process (including the ability to change the name of a terminal, so that programs do not have to address terminals in an absolute sense).

2. Initialization of the terminal to begin transmission, including the declaration of data buffering (number and size), specification of transmission modes, etc.

3. Actual transmission of data (a character, word, buffer, etc., at a time).

4. Termination of transmission, and relinquishing terminal.

Typewriters

Typewriters include both typewriters and Teletypes. The typewriter is the most important because people have been trained to use them. Although harder to use, Teletypes are a common system terminal because they can be used remotely (low bandwidth communication lines), hard copy oriented, low cost, and are available.

Although they are inherently character oriented, it is sometimes desirable to buffer terminal data on a page text line at a time basis or until a special data delimiting key has been struck by the user. (This requires less overhead time from the system to process the

characters, since processing is done for each separate line of text rather than for each character of the text.)

It is necessary to allow some form of simultaneous input and output in order that a user can communicate with the system while it is printing, so that a user can stop or change the process. Full duplex Teletypes easily provide this; half duplex Teletypes can accomplish this by a form of "echo checking" during output. Most typewriter consoles must be supplied with special switches or keys to "break" the information output flow so that the user can stop runaway programs, for example.

Keyboard-Text Displays

These devices are similar to the typewriter in principle. The keyboard-text display does not have the hard copy provided by the typewriter (unless the terminal or console also has a printer), but it does provide the viewing of almost a full page of text, together with the ability to "point" anywhere on the page. These displays also require a higher output data rate from a computer in the form of "page turning" requests. This is the principal terminal for systems requiring simple graphical results or rapid scanning of text.

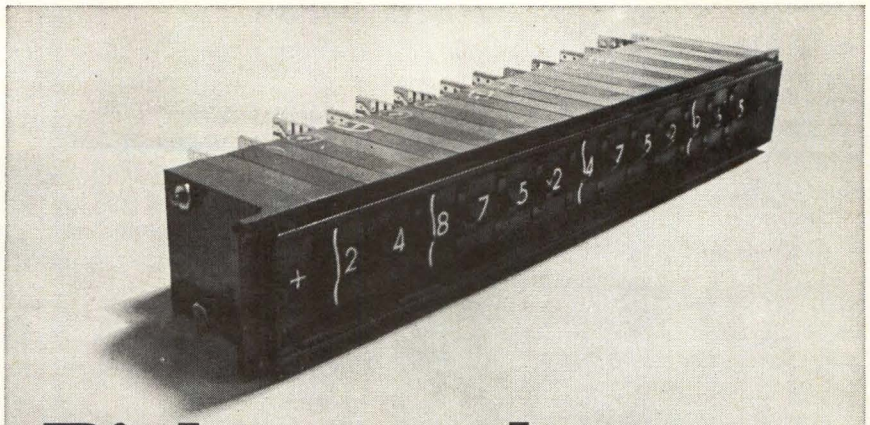
A small cursor, which is controlled by the terminal allows the user to "point" to any character on the page. The data associated with a single page of text is associated with the display.

The control of text displays requires more information processing than other terminals, since data can be randomly addressed by blocks both for input and output, rather than on a strictly sequential basis.

General Graphical Displays

These displays are similar to the text display, but have the added ability to display data by points, characters, lines, circles, etc., and in general have better resolution and are faster.

The information forming the picture may exist in primary memory (as a process or as data for a process) or within the display's own storage. The human eye requires a complete refresh or regenerate cycle about every 30 milliseconds, in



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which the data forming the picture must be sent to the display. This may impose a high data transmission rate on the memory system, interfering with processing, unless the display has an independent data memory to hold the picture.

For graphical input, a light pen is used to "point" to displayed information. The light pen can be used to "draw" on the scope face. The control and data structure problems of the text display are present to a much higher degree in general graphical displays.

The RAND Tablet is a very simple graphical input device. It allows one to draw on a 10″ × 10″ tablet with a stylus, and it can allow free hand drawing, printed character input, or curve tracing (through paper). It may be used independently or in conjunction with a graphical display. The resolution or number of electronically independent points over the 10″ × 10″ area corresponds to 1024 × 1024 points.

Plotters

These devices provide hard copies of general graphical data. Typically, a plotter operates on an incremental or discrete basis (0.01 inches/increment) at a rate of 300 points/second over a plotting area of 12-30 inches by several hundred feet.

Direct Terminals

The above terminals are special cases of direct terminals, but in them most of the problems of terminal hardware and software design can be seen. Namely, problems of providing continuous two-way dialogue, response time, and the other human engineering problems.

Indirect Terminals

These terminals include most terminals used by other systems, i.e., peripheral card readers and line printers. The interface from a user's viewpoint can be identical to the above terminals. The logical difference, for example, between a line printer and a typewriter printer may just be the number of allowable characters on a line; thus, a page output on a line printer would appear identical to that of a typewriter (but not vice versa).

Specialized Terminals

These terminals are used for special time-sharing systems such as airlines reservations, etc. They include: banking teller windows, airline reservation stations, stock quotation inquiry keyboards, production line data acquisition terminals, etc. They provide the best possible coupling between the user and his system and are designed to minimize the number of errors and the time required as data is entered and extracted from the terminal by restricting the format and by encoding the information.

Inter-Machine Links

The link to specialized "non-human user" devices imposes the highest performance requirements on the design because the data transmission rate is high and is determined by the device characteristics, rather than the system. That is, these devices have to be served in real time, at the demands of the device. Devices of this type include those used in process control applications, simulation equipment (aircraft or aerospace cockpits), film reading devices or scanners, hybrid linkages, etc.

By providing for this equipment in a system, hardware protection may also be required. A very complete interrupt or trap system may also be necessary in the hardware so that a job can be rescheduled rapidly to serve the device.

Peripheral Computers

These form a most necessary class of terminals by distributing terminal data transmission or loading to the system periphery. The peripheral computer provides the ability to lower the data rate for a larger system by providing local storage and processing capability. For example, display computers with the ability to detect light pen position and track the pen, and perform

TABLE 3. TERMINAL INPUT REQUESTS TO SYSTEM SOFTWARE

MESSAGES TO THE OPERATING SYSTEM:

1. Log in and log out. (Includes presentation of name, number, password, data, etc.)
2. Resource requests (assignment of terminals, primary memory, file space).
3. Setup of the job, or process.
4. Start, stop, and continuation of a process.
5. Examination and modification of elements of the primary memory process. (Presentation of a storage or memory map.)
6. Information requests:
   a. Run time, time of day
   b. Files used or space available
   c. Facts about system use.
7. Communication with other users or human operators.
8. Saving and restoring the complete state of a process.
9. Transmission of a job to a queue for batch processing.

MESSAGES TO EDITORS:

1. File name declarations including specification of access restrictions, formats, etc.
2. Transmission of data among files and/or terminals.
3. General file editing including creating, appending, inserting, modifying, deleting, etc.

MESSAGES TO TRANSLATORS:

1. File specifications including:
   a. Control statements.
   b. Source language inputs.
   c. Object output.
   d. Object listing.
   e. Object linkage information (if separated from output).
   f. Errors and diagnostics.
2. Control switches (e.g., what to do in case of errors).

MESSAGES FOR PROGRAM DEBUGGING:

Command messages to system debugging routines are similar to the system commands, except that they are in terms of the source language program. They include:

1. Start, stop, and continuation of the process.
2. Examination and modification of the process in terms of the source language. Insertion of program patches. Display of data in any format.
3. Data set searching.
4. Program tracing.
5. Conditional tracing via breakpoints which are executed only if program reaches a specific state.

MESSAGES TO SYSTEM OPERATORS (HUMAN) AND MANAGEMENT (HUMAN)

1. Equipment availability or status information.
2. Configuration specification.
3. Accounting and system status requests.
4. Appending user availability, cost, facility, priority lists.
5. Message broadcasts.
6. Manual instructions for tape mounting, card removal, etc.
7. System diagnostic reports.
8. Control of back-up or archival storage.

MESSAGES TO CONVERSATIONAL LANGUAGES

1. Language or Text Edit commands. Creation, modification, and deletion of programs is provided.
2. Direct Statement Commands Execution. For languages which allow arithmetic statements to be written, the ability to have a statement executed immediately (e.g., 2 + 2 = ?) is provided.
3. Commands for Control of the Programs.
4. Data entry and data output from the program.

some coordinate transformations on the display data may be desirable.

In process control applications, data sampling, limit checking, and data logging can be done by peripheral computers, on a more economical basis, since they do not require the generality of a large machine. Also, since the overhead time to switch to another program may be high, the high data rates associated with these processes would degrade the large machine.

External Time-Sharing Systems

These terminals form the link with other time-sharing systems. This form of intercommunication is new, but may be significant in total problem solving systems by allowing programs in one system to call on other systems.

Message switching centers with some local file storage might form the immediate link with users. As users require more advanced services, the switching centers would likely call either large, general systems or systems specializing in a particular service. Because of our geographical time zones, inter-system load sharing is possible in a fashion similar to that in which utilities share electrical generation capacity.

TERMINAL COMMUNICATION WITH THE OPERATING SYSTEM

In addition to the terminal connection with the process, a terminal must connect with the operating system software for the control of the job. All of the programs (translators, editors, loaders, etc.) that form the system also require control words or statements. Table 3 lists the information required from the user to specify tasks for the system.

Communication Dialogue

The format used for control information is an important design consideration, and it is important to have a "forgiving system," or one which does not affect a user too adversely when a wrong command is given.

It may be important that the user react (type in, observe output, etc.) as little as possible to specify a given situation. Abbreviated commands might be permitted in place of longer words (e.g., LOGIN = LI),

Chapter III. *The Word from GENISCO.*

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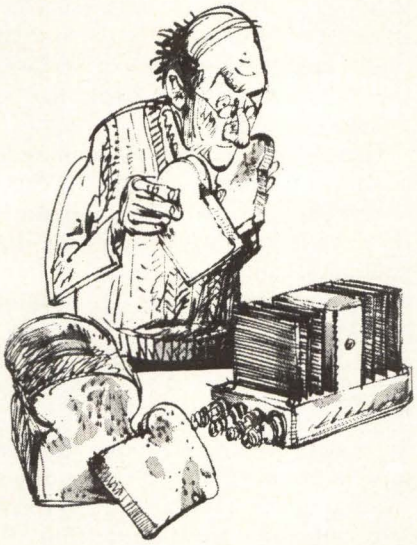

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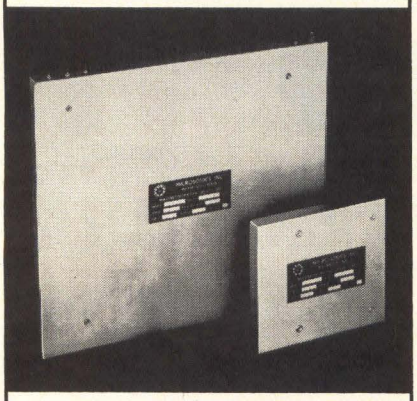

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although longer commands would also work. For example, two interesting possibilities are: a user types a command that has enough information to make the command unambiguous, and, the user types enough information to make the command unambiguous, followed by the system typing the rest of the command in a "ghost-like" fashion. When commands are given that irrecoverably affect files, the system might require some sort of verification that the command specified is actually desired.

User defined macro commands compose the most general method to provide users with the commands they want, and what they call the commands, because users define, name, and write them in terms of standard sets of system commands.

FILES

It is desirable to consider the file and terminal structure in a similar fashion from both a user and system software viewpoint; that is, the access, method of transmitting data, and data formats may be nearly identical for both files and terminals.

The file characteristics have been previously discussed as part of the operating system software in terms of what the hardware is, what the operating system provides, and what the file looks like to a user.

USER PROCESS

The user process or procedure includes: a memory map locating the process, the actual process, and user status information (terminal and file assignments).

Occasionally, a guaranteed service must be made available to a user both for specialized devices, and processing. For example, a user may have a particular terminal that requires service at regular intervals. A protected, assignable command subset to control the particular device may be required. Alternatively, control can sometimes be provided by incorporating the device in the normal system peripheral or input-output service programs. Scheduling of users now becomes more complex, since the device anomalies constrain the scheduling algorithm.

Guaranteed processing capabilities are provided by treating the total processing capacity as a resource. Thus, a guaranteed capacity at a guaranteed time can be scheduled according to request. Users of systems may get degraded service rather than be denied access because of poor service. With a supply of unattended jobs to process in a batch queue, or compute-bound problems to run as background, a combination denied/degraded service may be provided which balances the system's capacity.

The methods of communication with the system through a hierarchy of higher level operating systems pose the questions: "What is the user process?" and "What is the system?" A user's procedure may be appended to the system and become a system function or common user service procedure. This ever expanding set of program segments which form the system present the problems of segment naming, file location within the system, and protection while they are being run. Nevertheless, the ability to run normally while creating and testing other parts of a system, or to have a portion of the system removed and another one substituted gives rise to very powerful tools in the graceful creation of the system. As a minimum, a new system should be able to be created on a general purpose system, with the substitu-

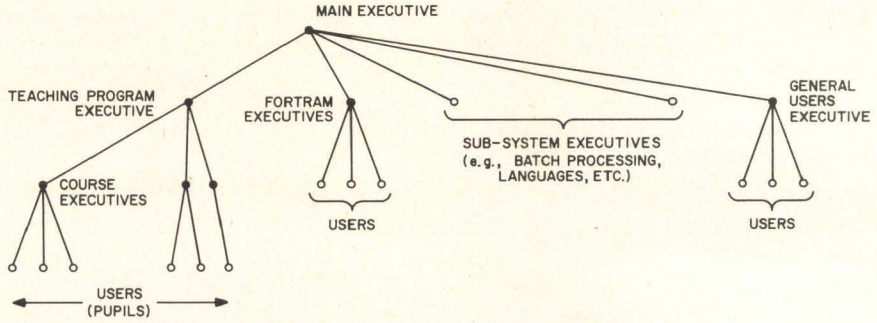

Fig. 14 Hierarchy of executives with a general purpose time-sharing system.

tion for the existing system occurring at a time when the system is inoperative. We can look forward to complete systems that allow subsystems that do their own scheduling of time, etc., and allocate some resources. Thus, a completely general purpose system might allow complete freedom to incorporate any of the systems described in Table 1 in an efficient manner. Figure 14 shows the relationship processes might have to one another in a general purpose system.

CONVENTIONAL VERSUS CONVERSATIONAL LANGUAGE PROCESSING

Conventional processing or translation of a language occurs in the sequence:

1. Creation of a text format source file (cards or system file) which describes the process.
2. Translation of source files into object files with linkage, relocation, subroutine, listing, and error information.
3. Loading the object file together with library files to form the process.
4. Process execution.

In contrast, conversational language processing provides nearly simultaneous creation and execution of procedures. The input language can be checked at the time of entry at the terminal and is translated, being immediately available for execution.

The data may be transformed into an interpretive form with all sub-routines, linkages, etc., occurring directly on input with no intermediate files. The insertion of additional statements or program steps is done directly, and debugging is through the run time diagnostics and user abilities to examine variables directly and execute statements conditionally. The conversational system may require a slightly longer execution time, but is most effective because of its combined editor, translator, loader, library and debugging system. Clearly, for problems involving little computation, the turn-around time is very short for solving problems in this fashion. The main structure of programs is such that this interactive approach may be the common method in a few years.

Batch Processing

This is one of the most efficient methods of controlling the execution of a large number of programs, since jobs are always run to completion. In a time-sharing system which is principally serving on-line users, the batch process can be used as a background job or to absorb spare capacity. A fixed or guaranteed amount of processing can be allocated to batch processing. The batch must be able to be loaded by either external users with card decks or users who defer jobs that can be done anytime (or at batch convenience).

The handling of a batch need not be incorporated within the system, but rather a batch process can

TABLE 1. CAPACITY REQUIREMENTS FOR TIME-SHARING SYSTEM APPLICATIONS

Specialized System Service, or Application	Primary Memory for Process (in bits)	Primary Memory for User Data (in bits)	Processing Capacity/ User (in operations*/ interaction†)	File Organization and Size (10^6-10^9 bits)	Direct Terminals
Desk calculator	very small	very small ($<10^3$)	very small ($>10^4$)	none	typewriter, input keyboard, strip printer, scopes, audio output, or special console.
Stock quotation	small	small ($<10^4$)	very small ($>10^4$)	one (small-medium)	see above, stock ticker tape or transactions input, telephone.
Airline reservations	medium	small ($>10^4$)	small ($>10^5$)	approx. 6 (medium-large)	special consoles, typewriters, scopes.
On line banking	medium	small ($>10^4$)	small ($>10^5$)	approx. 10 (medium-large)	see above, special bank teller consoles.
General conversational computational languages (JOSS, CULLER-FRIED System)	medium	small-very large (10^3-10^5)	small-large unbounded (10^4-$>10^8$)	multiple files per user, with few file types (medium-large)	typewriter, printer, scope, plotter. (Culler-Fried consists of scope, keyboard, and tablet.)
Specialized computer aided design, engineering, problem solving languages (COGO, etc.)	medium-large	small-very large (10^3-10^5)	small-very large (10^4-$>10^8$)	see above	see above
Process control	medium-large	medium ($>10^5$)	small-very large (10^4-$>10^8$)	few (small)	physical quantity transducers, general user terminals.
Text editing (Administrative Terminal Service)	medium	small ($>10^4$)	small (10^4-10^5)	multiple single purpose files/user. (medium)	typewriter, printer, scope.
On line information retrieval of periodical headings, bibliographies, keywords, abstracts	medium-large	medium ($>10^5$)	medium (10^5-10^7)	one (very large)	see above. telephone (dial in, audio out)

*assumes a fairly sophisticated processor and instruction set
†maximum interaction intervals for user requests are $\simeq$ 10 sec.

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be regarded as a special user. Thus, a common service program (the batch manager) would permit any user to "batch process."

CONCLUSIONS

PRESENT PROBLEMS

Before widespread time-sharing systems and system networks can be formed, standardization of data and file format descriptions will have to occur. Simple conventions must be established to control the actual format of the bits transmitted between computers. This will enable the transmission of problems, data, and procedures between systems. Present intersystem communication experiments should provide a framework for the standardization of information interchange formats, and detailed data representation.

Once a data representation for higher speed lines is established, it will be possible to remove the terminals we presently associate with the computer outside the computer's periphery. This will enable the cross-use of terminals among computers. It will also allow software that is more independent of the peripheral and computer to be written.

Current data transmission costs for the remote typewriter user (with an average input rate of ten bits per second) do not reflect the true cost-capacity (2400 bits per second for a voice grade line) or use of the line.

Although good, low cost computers (processor, memory, and minimum peripheral equipment) are available, the higher costs associated with file storage for smaller systems do not permit the design of low cost time-shared computers.

Present time-sharing structures for computers are extension organizations of the basic computer. Present systems were not initially designed for time-sharing, but were modified slightly to accommodate potential users. Hence, these systems create almost as many problems as they solve. A more reasonable approach for a system's design is an initial specification that includes Time-Sharing as a goal. A solution might take on the form of a network. For example, the very large computing machines that are built by computer manufacturers have: taken a long time to build (and technology has changed, invalidating industry's extrapolations before the computers were operational); required longer than expected to become operational; failed to meet initial design goals, have been uneconomical from a production standpoint; and only a few systems have been built. The current large, very general systems also suffer from the same kind of design thinking.

Each component of a general purpose time sharing system is constrained to supply such general service that the system as a whole may be so inefficient (and expensive) as to make the system impractical. The issue is similar to an organization consisting of either highly trained specialists or generalists. An organization of generalists is very flexible; but, on the other hand, it may not be economical to have people who are capable of being the president doing all the tasks within an organization. The general purpose systems just now becoming operational are constructed in such a flexible fashion as to probably be uneconomical. Each system component is so general (for example, the filing system) that, although it can perform any task (given enough time), the act of doing very trivial operations requires a great deal of time. Perhaps a better approach is to divide the systems's resources by allowing several independent operating systems to care for them (e.g., editing, assembling, filing, translating, and running).

FUTURE SYSTEMS

Future computers will be equipped with hardware to allow some form of time-sharing. For smaller com-

puters, the additional hardware greatly enhances a system's utility, especially when being used in process control and in research requiring the direct links with other machines or to experimental equipment.

The form of Time-Sharing Computers will be:

1. The system with a single general user or batch process, *plus* one fixed job or a fixed multi-terminal community of special users (1+1, or 1+n special users). Process control and on-line special business data processing systems take this form.
2. Dedicated special systems which service a particular user community. These provide little or no communication with other systems. (E.g., library, airlines reservations, etc.)
3. Dedicated systems with switching ability so that a problem that requires other aids can be referred to other systems. More general systems may refer problems to them.
4. Message switching for other systems. These may have file processing, editing, and limited calculation capability, or message buffering; such a system would communicate with other systems for most demands from users.
5. Peripheral computers that service special terminals and control small local processes. Processing capacity for general purpose problem solving, file storage, program translation, and diagnostics for the peripheral system would be derived from a higher level system.
6. The totally general system with a large community of users. The general system would undoubtedly communicate with other systems.

Although the author has attempted to be objective, it is felt that the technique of computer Time-Sharing is a significant advance toward an effective use of computers. Time-Sharing removes one more restriction in computer usage — that of allowing only a single use of a machine. As such, the additional generality creates opportunities, as well as countless problems.

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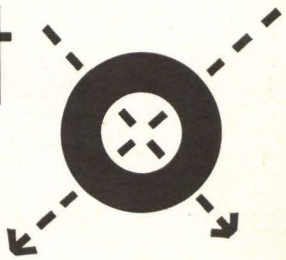

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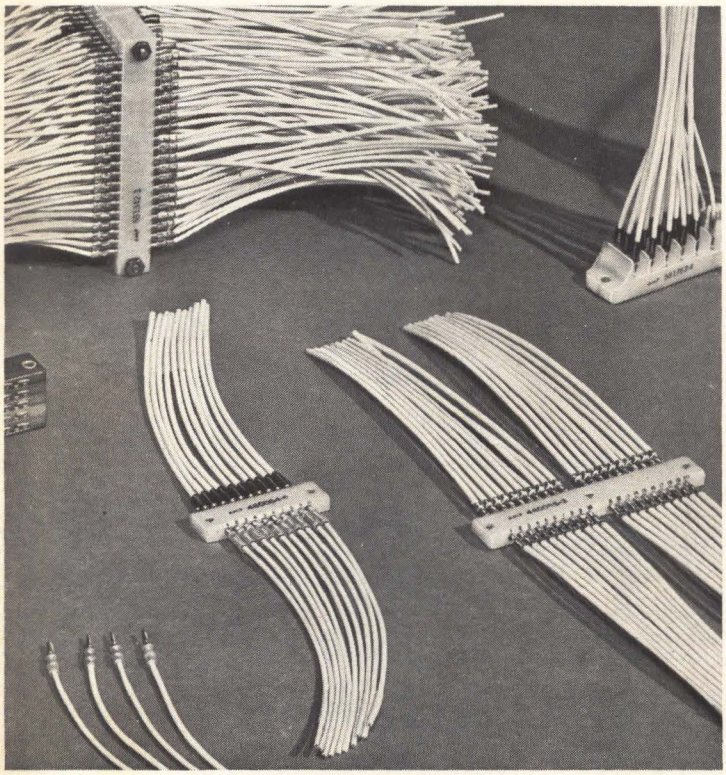

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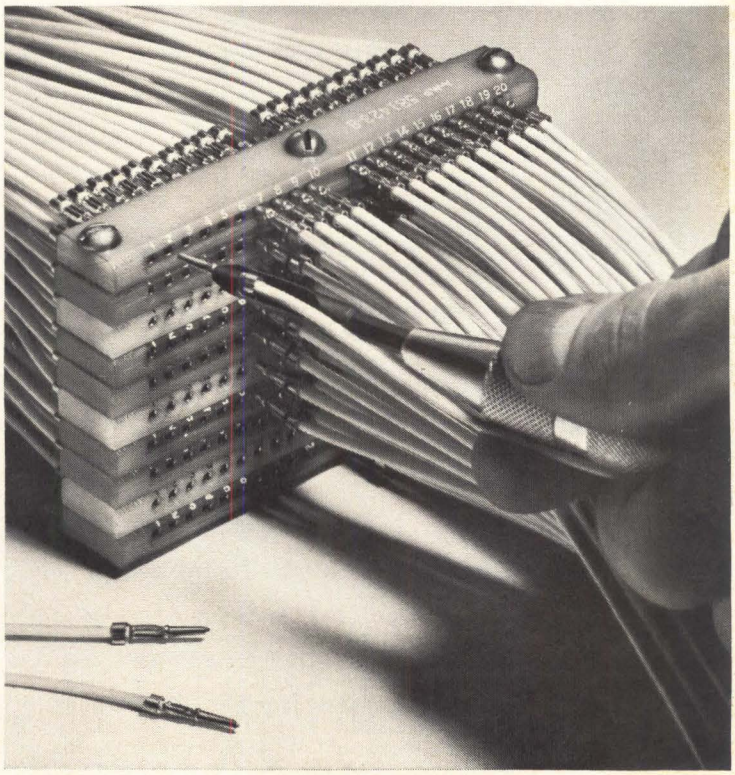

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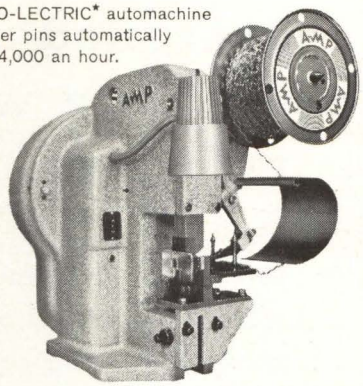

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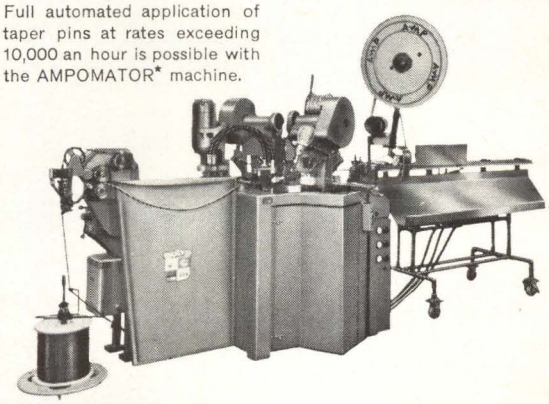

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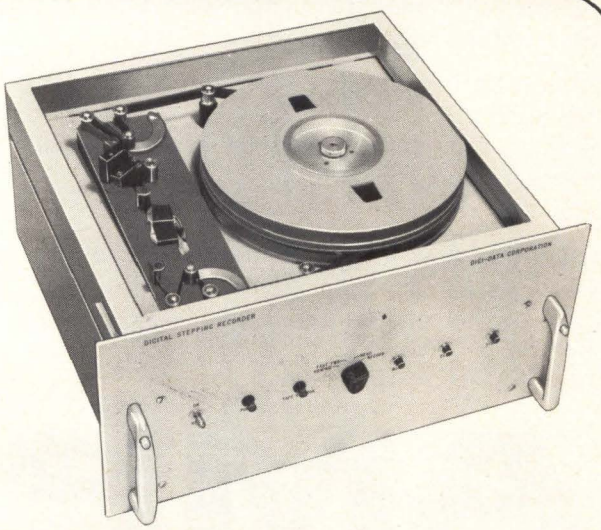

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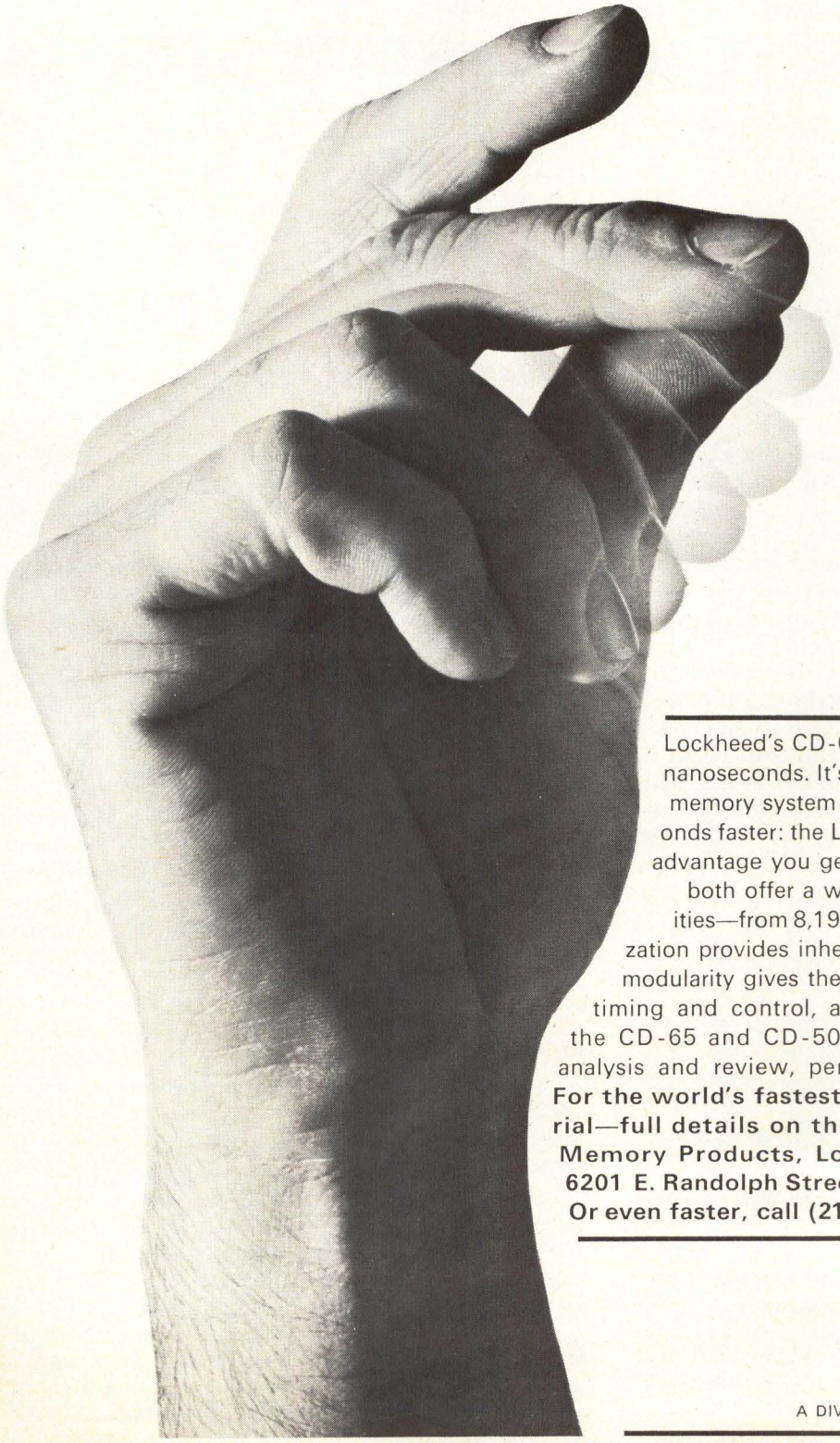

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Placing the accuracy and speed burden for S-D conversion on the digital equipment minimizes the analog equipment and enhances system performance.

SOLID-STATE SYNCHRO-

The application of digital computers has been severely limited in systems that must interface with analog computer equipment. This limitation is particularly prevalent in aerospace systems where the lack of the appropriate interface equipment often precludes the use of a digital computer. Although digital computers are highly miniaturized and economical, the interface equipment often offsets these advantages with mechanizations that can exceed that computer size and cost. In order to enhance the applicability of digital computers for aerospace applications, Teledyne has expended considerable effort in the development of hybrid interface equipment. This hybrid equipment is mechanized with the latest solid state components and advanced packaging techniques to implement a universal interface that is miniaturized, modular, and economical. The interface unit is compatible in performance and packaging with the Teledyne family of digital computers.

The basic guidelines for the development of the hybrid interface equipment were to:

1. place the burden of the conversion on the digital equipment
2. minimize the performance requirement placed on the analog equipment
3. eliminate electromagnetic and electromechanical equipment.

The most complex part of the hybrid interface equipment is the synchro-to-digital (S/D) converter because of the three wire (120° coordinate system) AC analog form of the synchro signals. The Solid State S/D Converter accepts these three wire AC waveforms, performs a minimum of signal processing in the analog domain, then efficiently converts the data to a digital form for processing in the digital domain. The analog equipment converts the AC analog 120° coordinate signal forms to incremental digital orthogonal coordinate data. The digital data is processed with a digital "follow-up servo" implemented with digital differential analyzer (DDA) computer modules. The DDA will insure scale factor and phase angle precision and automatically compensate for many errors introduced in the analog domain. The digital output of the S/D converter will contain the sine and cosine functions in addition to the angle. This is a significant advantage over converters that only generate the angle, because the trigonometric functions of the angle are often the parameters that are required.

Contemporary S/D converters perform the conversion with electromechanical follow-up servos driving digital shaft encoders or with switching of taps on transformer type electromagnetic equipment. These techniques require large, heavy, and expensive electromechanical or electromagnetic hardware used in a servo loop to null the input signal. The size, weight, performance, and cost considerations preclude the use of these converters for many aerospace applications.

A description of the Solid State S/D Converter mechanization will be presented following an analysis of the pertinent characteristics of the synchro waveforms.

Synchro Signal Forms

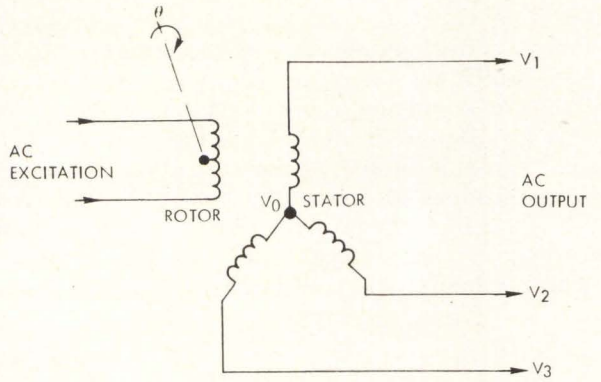
A synchro is an analog angular position transducer, where the output signal is an AC voltage with the amplitude indicative of the angular position of the rotor.

A schematic representation of a synchro is presented in Figure 1. The rotor is excited with an AC voltage that couples to the Y windings of the stator through transformer action. Angular position of the rotor, with respect to the stator, will determine the electromagnetic coupling between the rotor and each of the stator windings, thereby defining the amplitudes of the signals in the three windings. The stator output voltages are either in-phase or 180° out-of-phase with

TO-DIGITAL CONVERTER

by
GILBERT P. HYATT
Teledyne Systems Company

the reference excitation. Amplitude and phase (in/out) of the output voltages are indicative of the angular displacement. The output signals are in time phase with the excitation signal, with the amplitude of the output signals conveying the trigonometric information. Phase shifts between the reference and the output waveforms do not convey angular information, but are potential sources of error in interpreting the output signals.



(A) Synchro

Fig. 1 Shematic representation of a synchro.

The excitation signal, shown in equation (1), is electromagnetically coupled to the output windings of the synchro, generating the output signals shown in equations (2) through (4).

$$V_{excitation} = E \sin wt \quad \text{eq (1)}$$
$$V_{0-1} = K_1 E \sin wt \sin \theta \quad \text{eq(2)}$$
$$V_{0-2} = K_1 E \sin wt \sin (\theta\text{-}120°) \quad \text{eq (3)}$$
$$V_{0-3} = K_1 E \sin wt \sin (\theta\text{-}240°) \quad \text{eq(4)}$$

The time dependent term, sin wt, is common to all signals and is not a function of rotor position. The other terms of the synchro output equations are amplitude defining qualities, independent of the time varying portion of the waveform. It can be seen that the output signals are all in time phase with the excitation signal, and the amplitude is a trigonometric function of the angular position of the rotor. Equations (2) through (4) define the voltage induced in the winding from the common point of the three coil Y-connection to the output terminal. The common point of the three windings is usually not available for synchro follow-up operation. Therefore, it is necessary to operate on the voltages across the three output winding legs. The output signals of the synchro are listed in equations (5), (6) and (7). The subscripts define the terminals across which the voltages are measured.

$$V_{1-2} = K_2 E \sin wt \sin (\theta - 150°) \quad \text{eq (5)}$$
$$V_{2-3} = K_2 E \sin wt \sin (\theta + 90°) \quad \text{eq (6)}$$
$$V_{3-1} = K_2 E \sin wt \sin (\theta - 30°) \quad \text{eq(7)}$$

The signals defined in equations (5), (6) and (7) represent those signals which are available at the interface. Equations (5) and (7) contain sufficient information to completely define the synchro position, while equation (6) is redundant. The information contained in equations (5) and (7) can be organized in a more intuitive form with the use of the trigonometric identities, illustrated as equations (8) and (9).

$$\sin (\theta - 150°) = \sin \theta \cos 150° - \cos \theta \sin 150° \quad \text{eq(8a)}$$
$$= -\sqrt{3/2} \sin \theta - 1/2 \cos \theta \quad \text{eq(8b)}$$
$$\sin (\theta - 30°) = \sin \theta \cos 30° - \cos \theta \sin 30° \quad \text{eq(9a)}$$
$$= \sqrt{3/2} \sin \theta - 1/2 \cos \theta \quad \text{eq(9b)}$$

Substituting equations (8b) and (9b) into equations (5) and (7) yields equations (10) and (11), respectively.

$$V_{2-1} = (K_2 E/2) \sin wt (\sqrt{3} \sin \theta + \cos \theta) \quad \text{eq(10)}$$
$$V_{3-1} = (K_2 E/2) \sin wt (\sqrt{3} \sin \theta - \cos \theta) \quad \text{eq(11)}$$

From equations (10) and (11), it can be seen that

the voltages measured from synchro outputs 2 and 3, using synchro output 1 as a reference, is composed of sine and cosine components of the angular displacement of the synchro rotor. The coefficients of the corresponding trigonometric functions of θ from equations (10) and (11) are equal. Therefore, algebraic manipulation of equations (10) and (11) can be used to isolate the components of the interface signals that define the sine and the cosine of the synchro angular position. Addition and subtraction of equations (10) and (11) yield equations (12) and (13), respectively.

$$V_{2-1} + V_{3-1} = K_2\sqrt{3}\,E \sin wt \sin \theta \qquad \text{eq(12)}$$
$$V_{2-1} - V_{3-1} = K_2\,E \sin wt\,\theta \qquad \text{eq(13)}$$

The time varying term, sin wt, is removed with a phase sensitive demodulator. This term is removed from the signals represented by equations (10) and (11) before they are added to form the signals represented by equations (12) and (13).

Equations (12) and (13) completely define the angular position of the synchro. It should be noted that the trigonometric functions of θ contribute only to the amplitude of the respective signals, introducing no inherent time or phase sensitive terms. The two signals defined in equations (12) and (13) are time coincident with the excitation to the synchro, excluding error mechanisms.

Synchro-to-Digital Converter

A representative mechanization of the Solid State S/D Converter is illustrated in Figure 2. It is basically a succession of conversions from each signal form to a more convenient signal form that permits appropriate processing. This approach permits many variations of the conversion concept, depending upon interface considerations and tradeoffs. In a typical application, the synchro transmitter is excited from a reference AC voltage supply. The excitation is coupled to the output windings as a function of the mechanical angular displacement of the synchro rotor. This angular displacement is illustrated as the θ_I input angular displacement. Three output lines are presented to the interface with signals that are indicative of the angular position of the synchro. These interface signals are in AC analog form, with an AC carrier frequency that is amplitude modulated as a trigonometric function of the angular displacement of the synchro. The time varying components of these signals are either in-phase or 180° out-of-phase with the reference excitation. A phase sensitive demodulator (PSD) is used as an AC analog to DC analog converter. The demodulator is a synchronous chopper, switching the input signals onto the output line in synchronism with the reference signal waveform. The output of the phase sensitive demodulator is a DC signal with a high ripple content, similar to a full wave or half wave rectified waveform, whichever is applicable.

In typical application of a phase sensitive demodulator, the output signals are filtered to remove the large ripple content. In the mechanization illustrated in Figure 2, the output of the phase sensitive demodulator is operated on by a reset integrator (RI), which provides a filtering function superior to that of a passive filter. In addition, the ripple does not propagate into system errors due to the inherent error compensation characteristics of this converter.

The reset integrator provides the primary function of a DC analog to pulse rate converter. In the mechanization shown, the reset integrator also provides the secondary function of algabraic summation of the synchro information, described analytically in equations (12) and (13). This summation function effectively converts from three phase synchro type information to two phase resolver type information. Therefore, the output of the reset integrator is in orthogonal coordinate trigonometric functions.

The reset integrator primary function of DC analog to pulse rate conversion is accomplished by implementing an analog integrator which integrates the DC voltages applied at the input. When the integrator output exceeds a voltage threshold, a precise reset pulse is generated to reset the integrator a calibrated amount by discharging the feedback capacitor. The rate at which the integrator continues to exceed the threshold is a function of the input voltage levels. The resetting pulse rate is also used as the reset integrator output and is indicative of the rate at which the integrator continues to exceed the output voltage threshold. Therefore, the output pulse rate is directly proportional to the average input voltage magnitude.

The mechanization illustrated in Figure 2 makes

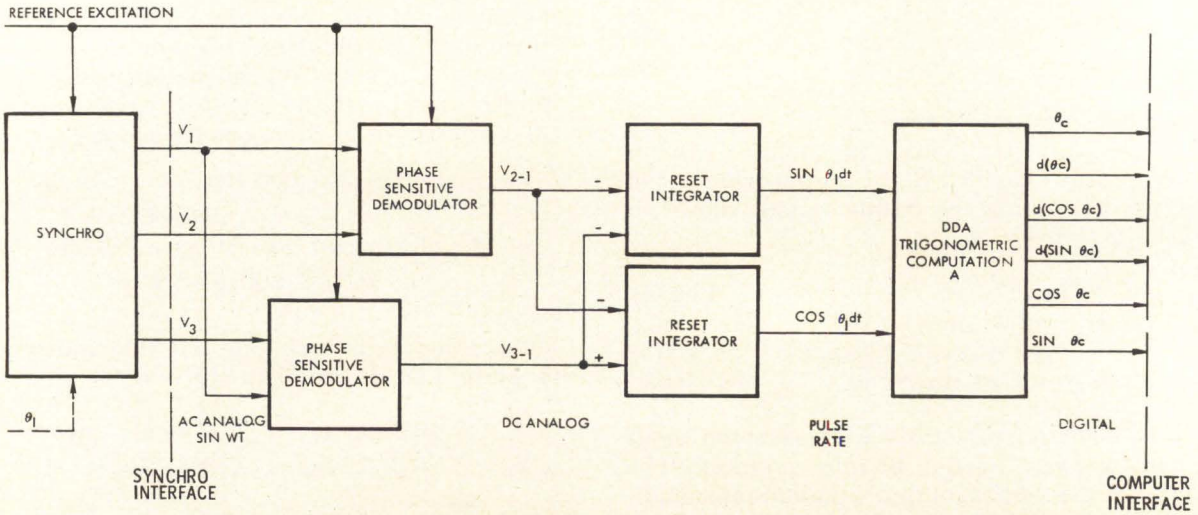


Fig. 2 Representative mechanization of the solid-state synchro to digital converter.

multiple use of the reset integrator functional block, where it is used to:

1. Perform the DC voltage to pulse rate conversion.
2. Perform the three phase synchro to two phase resolver type signal conversion.
3. Perform the filtering function for the DC signals from the Phase Sensitive Demodulator.

Ease with which the multiple functions are implemented in the analog domain significantly reduces hardware and improves accuracy of this mechanization. For example, the three phase synchro to two phase resolver type signal conversion is accomplished by the addition of one resistor to each reset integrator summing junction. These two resistors are used to replace the Scott-T transformer-type three-phase-to-two-phase signal converter. Therefore, the advantages of this technique are quite significant.

The reset integrator outputs are pulse trains, the rate of which is proportional to the trigonometric functions of the synchro angular displacement. These two pulse trains are significantly amplitude sensitive; where synchro excitation variations, synchro transformation ratios, and other mechanisms that affect the scale factor of the signals will affect the amplitude of the reset integrator output. Direct use of this pulse rate information in the computation results in amplitude or scale factor errors, but which appear as angular displacement errors. These scale factor errors can be conveniently eliminated by using the ratio of the two pulse trains instead of each pulse train by itself to determine the angular displacement of the synchro.

A digital differential analyzer (DDA) trigonometric computational block is implemented to eliminate the scale factor sensitivity of the synchro signals. This computation is described in the corresponding section of this article. Effectively, equation (17) is implemented with a DDA computational block.

$$\sin(\theta_I - \theta_C) = \sin\theta_I \cos\theta_C - \cos\theta_I \sin\theta_C \qquad \text{eq(17)}$$

A DDA sin-cos generator, used as a "digital resolver", is rotated computationally to balance the input pulse rates. Solution of equation (17) using DDA techniques assures availability of the synchro trigonometric functions that are completely independent of any scale factor type errors from the input. Outputs of the computation block are whole number serial trigonometric (sine and cosine) functions, whole number serial angular information, incremental trigonometric functions, and incremental angular information. This DDA computation is a necessary part of this synchro-to-digital converter concept, because the scale factor sensitivity of the synchro information would not permit sufficient accuracy, in most applications, without this compensation. As a contrast, the insensitivity of the converter outputs to the input scale-factor parameter significantly decreases the cost of the analog equipment and provides a very significant amount of automatic compensation of scale factor type errors in the analog hardware. The predominating error mechanisms in the analog equipment are of a scale factor nature. Therefore, the elimination of the scale-factor sensitivity consideration permits extremely accurate analog mechanizations with only moderate consideration to many of the predominating error mechanisms. In addition, this DDA computation generates the trigonometric functions of the angle in addition to the angular information. Other types of S/D converters typically generate the angular information only, requiring additional computation to generate the trigonometric functions of the angle. Therefore, cost and equipment comparison between this mechanization and other converters should be made on a comparable basis, where the DDA computation is included in the comparison only if the alternate converter will present the trigonometric functions of θ at the computer interface. If the other converter will generate only the angular information, a functional block equivalent to the DDA computation must be added to generate the trigonometric functions of the synchro angle. An alternate trade-off would be to draw the computer interface at the input to the DDA computational block for a realistic comparison with the alternate type of converter. That is not to indicate that this converter can operate independent of the DDA computational block, but only to compare the alternates on an equivalent basis. These considerations are contingent upon the

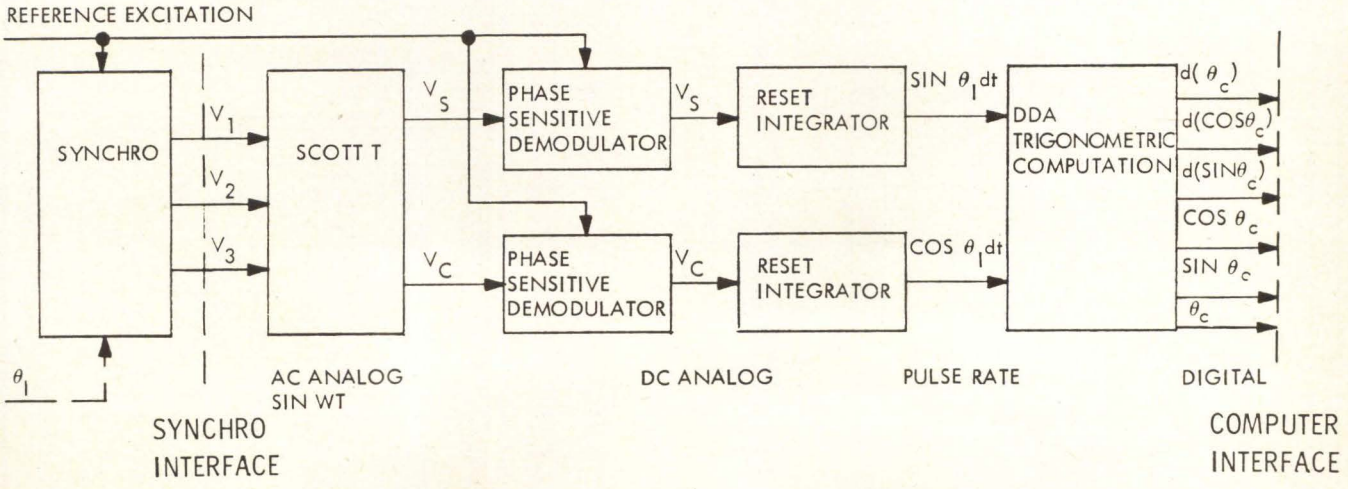


Fig. 3 Alternative mechanization of the solid-state synchro to digital converter.

requirement for trigonometric functions of the angle in the computation. Experience has shown that, in general, the trigonometric functions of the angle are required and not the angle explicitly.

An alternate mechanization of the synchro-to-digital converter is illustrated in Figure 3. This mechanization accepts the three phase synchro type information and converts it to two phase resolver type information with a Scott-T transformer. The two channels operate virtually independently, without the need for cross summing DC analog signals. The outputs of the Scott-T transformer are AC waveforms with amplitudes indicative of the trigonometric functions of the synchro angular position. The phase sensitive demodulators will act as AC analog to DC analog converters, with the reset integrators acting as DC analog to pulse rate converters. The DDA computation is identical to that used in the previously described mechanization. Considerations for this alternate mechanization are identical to those for the first mechanization, with the exception of the added cost and weight factors introduced by the Scott-T transformer.

DDA Trigonometric Computation

The DDA trigonometric computation functional block is a requirement for this synchro-to-digital converter mechanization in order to eliminate the scale-factor sensitivity of the converter. It is conceivable that, in certain types of applications, the synchro scale-factor parameters could be controlled within the requirements of the conversion. In the general case, tolerances are an order of magnitude greater than the required conversion accuracy, necessitating this computation. For high-accuracy type converters, the DDA equipment that is required will be offset by the simplification of the analog equipment due to the reduction of the scale-factor sensitivity of the converter.

The converter implicit servo is implemented in the digital domain with digital differential analyzer (DDA) computational elements. This DDA is a parallel-computation serial-word computer, where all computations are performed simultaneously in a bit-by-bit serial fashion. The DDA performs computations by successive additions accomplished at the rate of 32,000 iterations/second to approximate integration or multiplication. A detailed description of DDA operation is contained in Reference 1. The DDA computation is illustrated functionally in Figure 4. This functional diagram implements equation (17), which is the trigonometric identity for the sine of the difference of two angles. The input angle, θ_I is defined by the synchro rotor displacement with respect to the stator. The computed angle, θ_c, is contained in the DDA sin-cos generator. For the condition that θ_I is equal to θ_c, equation (17) will be nulled. Implementation of equation (17) with a DDA in an implicit servo type function causes the DDA sin-cos generator to be driven to a condition equivalent to the angular displacement of the synchro. As the synchro is rotated, the DDA sin-cos generator is servoed to the corresponding angular position. Effectively, the DDA computation block performs the function of a digital "follow-up servo."

The functional diagram, illustrated in Figure 4A, implements an implicit servo to solve equation (17). DDA computational elements 1 and 2 are used as pulse rate multipliers, where the input trigonometric function pulse-rate information is multiplied by orthogonal trigonometric functions from the "digital resolver". The symbolism used for DDA computational elements 1 and 2 indicates that the R register and R logic functions are utilized, but the Y register word is fanned-in from other DDA computational elements. For example, the Y register number for computational element 1 is obtained from the Y register of computational element 4. This Y register number is fanned-out to the two R logic functions, one in computational element 4 and the other in computational element 1. This fan-out is illustrated more graphically in Figure 4B, the sub-functional block diagram. Computational elements 3 and 4 implement a DDA sin-cos generator.

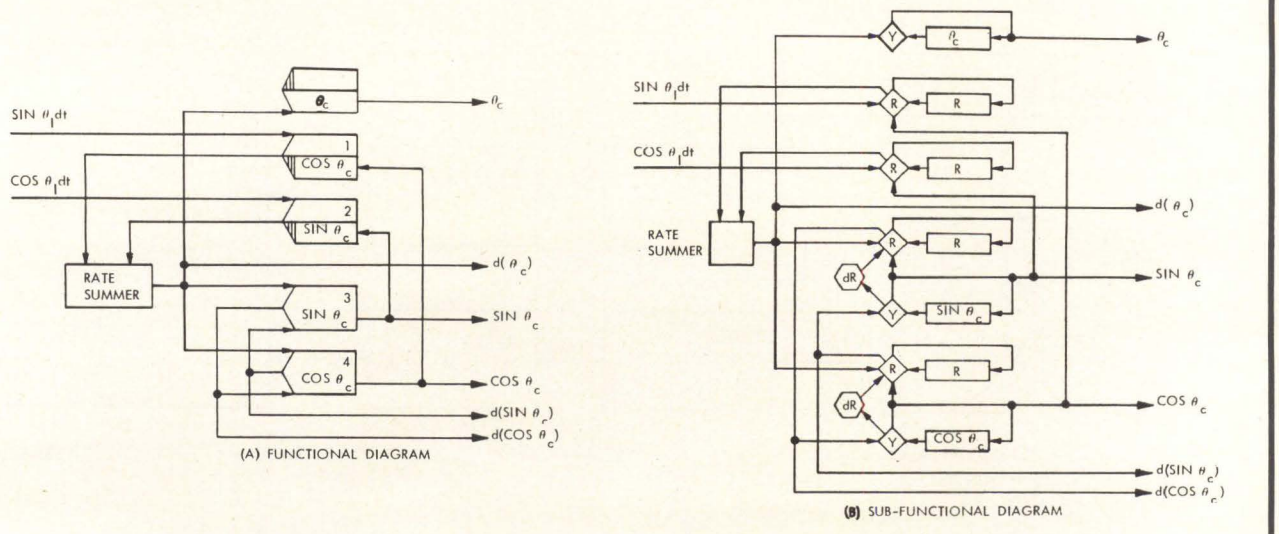


Fig. 4 Functional representation of a digital differential anasyzer trigonometric computation.

The two pulse-rate products from computational elements 1 and 2 are subtracted in the rate summer to generate an error rate which is a solution to equation (17). If this error rate is zero, indicative of the two trigonometric products being equal, the "digital resolver" is at the equivalent angular position of the synchro. If the error rate is not at null, the incremental pulses will be used as the $d\theta$ inputs to the DDA sin-cos generator, resulting in this "digital resolver" being rotated to null the error rate.

The sub-functional block diagram, illustrated in Figure 4B, implements rectangular integration for the pulse rate multipliers and trapezoidal integration for the sin-cos generators. The trapezoidal integration algorithm will reduce the error buildup in the "digital resolver" to an extremely small level.

It can be seen that scale-factor coefficients of the trigonometric functions will not affect the computation at the "digital servo" summing junction, which is the rate summer. A true scale factor coefficient is common to each of the trigonometric sub-products of equation (17), thereby affecting the gain of the "digital servo" but not the null. The DDA computation that implements equation (17) is nulled independent of the scale factor of the respective angular functions.

Output scale factor of the "digital servo" is dependent on the initial conditions loaded into the sin-cos generator. The vector sum of initial conditions for the sin-cos generator defines the scale factor of the output trigonometric functions. These initial conditions are simple to generate, permitting a zero to be loaded into the sin θ_c register and a nominal scale factor, typically unity, to be loaded into the cos θ_c register. These initial conditions are representative of an initial 0° angular position with a unity scale factor. After the initial conditions are loaded, the "digital servo" loop will be closed; thereby permitting the "digital resolver" to be driven to the corresponding angular position of the synchro. Therefore, only constant initial conditions need be loaded, since the "digital resolver" automatically generates the proper parameters after the "digital servo" loop has been closed.

Conclusion

The Solid State S/D Converter permits the mechanization of a low cost accurate, versatile, and miniature interface that can accommodate synchro input signals. This converter will increase the feasibility of using digital computers in conjunction with electromechanical analog computers, which are common in aerospace applications. In addition, a more optimum mix of analog and digital techniques will be practical for hybrid computers.

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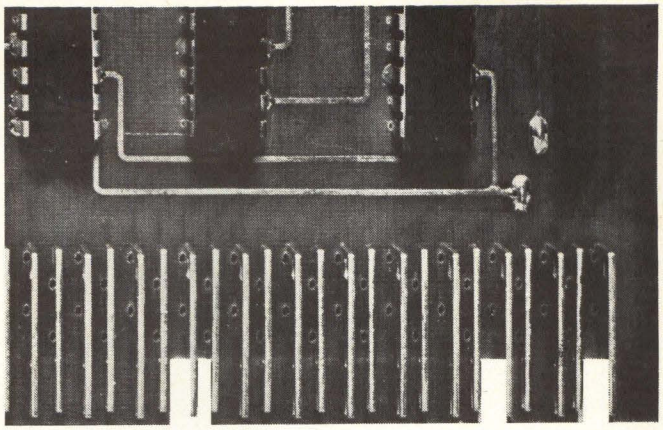

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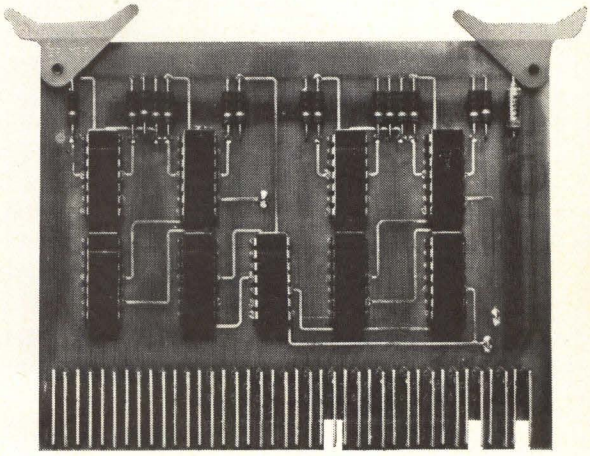

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CIRCLE NO. 33 ON INQUIRY CARD

Most methods for obtaining flip flop input expressions require a Karnaugh map for each type of flip flop considered. This article presents a method that requires only one map, regardless of the number of different types of flip flops to be investigated.

A ONE-MAP METHOD FLIP-FLOP INPUT

by
MITCHELL P. MARCUS

In the synthesis of pulse-input sequential circuits, in which flip flops furnish the memory and delay properties, the design procedure is basically as follows:

1. the word statement of the problem is transformed into a flow table;

2. a secondary assignment is made for the flow table, i.e., a combination of flip flop states is assigned to each circuit state;

3. the flip flop input (excitation) expressions are obtained; and

4. the output expressions are obtained.

This article is concerned with step 3. There are various methods for implementing this step, most of which utilize Karnaugh maps. All methods except the one presented here require a map for each type of flip flop considered. In these approaches, (e.g., References 1, 2 and 3) each type of flip flop has a specific set of rules for going from the flow table to the maps.

The method presented here requires only only one map, regardless of the number of different types of flip flops to be investigated. The map is drawn from the flow table without regard to any type of flip flop. A set of rules for each type of flip flop is used in reading the map, the input expressions for all types of flip flops being read from this one map. This method is described in detail in Reference 4, a book on switching circuits, now in its second edition, which emphasizes the practical rather than the abstract.

To illustrate the method, the example from Reference 3 will be used — that of designing a BCD counter. The BCD counter sequence is shown in Table 1.

Each row, in turn, can be considered an initial circuit state, that is, a combination of flip-flop states at time n. The following row, in each case, represents the next circuit state that will be reached, at time (n + 1), upon receipt of the input, clock, or synchronizing pulse. The sequence is repetitive.

Map entries are made as shown in Fig. 1.

TABLE 1

BCD COUNTER SEQUENCE

A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1

Initial flip flop state	Next flip flop state	Map entry
0	1	1
1	0	0
1	1	1
0	0	0
Optional		—

Figure 1. Map entries.

A 1 map entry thus represents the condition of a flip flop turning on; a 0 represents a flip flop turning off; a "1" represents a flip flop staying on; and a "0" represents a flip flop staying off. The maps for the four flip flops are shown in Fig. 2.

These are the only maps that need be drawn; input expressions for any type of flip flop can now be read from these maps. The rules for reading a map for some typical types of flip flops — T, S-R, S-R-T, J-K (or S-R-SR), and D — will now be discussed.

FOR OBTAINING EXPRESSIONS

CD \ AB	00	01	11	10
00	0	0	—	1
01	0	0	—	0
11	0	1	—	—
10	0	0	—	—

A Map

CD \ AB	00	01	11	10
00	0	1	—	0
00	0	1	—	0
11	1	0	—	—
10	0	1	—	—

B Map

CD \ AB	00	01	11	10
00	0	0	—	0
01	1	1	—	0
11	0	0	—	—
10	1	1	—	—

C Map

CD \ AB	00	01	11	10
00	1	1	—	1
01	0	0	—	0
11	0	0	—	—
10	1	1	—	—

D Map

Figure 2. Maps for the four flip flops.

T Flip Flop

The T flip flop has one input, T. When this input is pulsed, the flip flop changes state. The operating characteristics of the T flip flop are shown in Fig. 3.

T	Initial State = 0	Initial State = 1
0	0	1
1	1	0

Figure 3. Operating characteristics of T flip flop.

The input pulse requirements for the T flip flop (Fig. 4) can now be read from Fig. 3.

Map entry	T
1	1
0	1
1	0
0	0
—	—

Figure 4. Input pulse requirements for T flip flop.

The rules for reading a map for the T flip flop are thus:

- Every 1 and 0 must be accounted for in the T input expression.
- Any — may be used optionally in the T input expression.

From the map in Fig. 2, the input expressions for the T flip flop are read:

$$T_A = BCD + AD$$
$$T_B = CD$$
$$T_C = \bar{A}D$$
$$T_D = 1$$

S-R Flip Flop

The S-R flip flop has two inputs, S and R. When the S input is pulsed, the next state of the flip flop is "on," regardless of the initial state. When the R input is pulsed, the next state of the flip flop is "off." The S and R inputs of this flip flop must never be pulsed simultaneously, since the resulting circuit action is indeterminate. These operating characteristics are shown in Fig. 5.

S	R	Initial State = 0	Initial State = 1
0	0	0	1
1	0	**1**	1
0	1	0	**0**
1	1		

Figure 5. Operating characteristics of S-R flip flop.

The input pulse requirements for the S-R flip flop (Fig. 6) are now read from Fig. 5.

Map entry	S	R
1	1	0
0	0	1
1	—	0
0	0	—
—	—	—

Figure 6. Input pulse requirements for S-R flip flop.

The rules for reading a map for the S-R flip flop can thus be stated as:

- Every **1** must be accounted for in the S input expression.
- Every **0** must be accounted for in the R input expression.
- Any 1 or — may be used optionally in the S input expression.
- Any 0 or — may be used optionally in the R input expression.

From the map in Fig. 2, the input expressions for the S-R flip flop are read:

$$S_A = BCD$$
$$R_A = AD \text{ or } \overline{B}D \text{ or } \overline{C}D$$
$$S_B = \overline{B}CD$$
$$R_B = BCD$$
$$S_C = \overline{A}\overline{C}D$$
$$R_C = CD$$
$$S_D = \overline{D}$$
$$R_D = D$$

S-R-T Flip Flop

The S-R-T flip flop has three inputs, S, R and T. It has the combined characteristics of the S-R flip flop and the T flip flop. The S and T inputs of this flip flop must never be pulsed simultaneously when the flip flop is on, and the R and T inputs must never be pulsed simultaneously when the flip flop is off, since the resulting circuit actions in both cases are indeterminate. Operating characteristics of the S-R-T flip flop are shown in Fig. 7.

S	R	T	Initial State = 0	Initial State = 1
0	0	0	0	1
1	0	0	**1**	1
0	1	0	0	**0**
0	0	1	**1**	**0**
1	0	1	**1**	
0	1	1		**0**
1	1	0		
1	1	1		

Figure 7. Operating characteristics of S-R-T flip flop.

Input pulse requirements for the S-R-T flip flop (Fig. 8) are read from Fig. 7.

Map entry	S	R	T
1	1	0	—
	—	0	1
0	0	1	—
	0	—	1
1	—	0	0
0	0	—	0
—	—	—	—

Figure 8. Input pulse requirements for S-R-T flip flop.

The rules for reading a map for the S-R-T flip flop can thus be described as:

- Every **1** must be accounted for either in the S or T input expression.
- Every **0** must be accounted for either in the R or T input expression.
- Any **1** accounted for in the T input expression, or any 1 or — may be used optionally in the S input expression.

• Any **0** accounted for in the T input expression, or any 0 or — may be used optionally in the R input expression.

• Any **1** accounted for in the S input expression, any **0** accounted for in the R input expression, or any — may be used optionally in the T input expression.

In this particular example, the S-R-T flip flop offers no economical advantage over the S-R or T flip flops.

J-K (or S-R-SR) Flip Flop

This flip flop has two inputs, J and K (or S and R). It has the same operating characteristics as the S-R flip flop with one exception: both inputs may be pulsed simultaneously, in which case the flip flop changes state. These characteristics are shown in Fig. 9.

J	K	Initial State = 0	Initial State = 1
0	0	0	1
1	0	**1**	1
0	1	0	**0**
1	1	**1**	**0**

Figure 9. Operating characteristics of J-K flip flop.

The input pulse requirements for the J-K flip flop (Fig. 10) can be read from Fig. 9.

Map entry	J	K
1	1	—
0	—	1
1	—	0
0	0	—
—	—	—

Figure 10. Input pulse requirements for J-K flip flop.

The rules for reading a map for the J-K flip flop can thus be stated as:

• Every **1** must be accounted for in the J input expression.

• Every **0** must be accounted for in the K input expression.

• Any **0**, 1 or — may be used optionally in the J input expression.

• Any **1**, 0, or — may be used optionally in the K input expression.

From the map in Fig. 2, the input expressions for the J-K flip flop are read:

$$J_A = BCD$$
$$K_A = D$$
$$J_B = CD$$
$$K_B = CD$$
$$J_C = \overline{A}D$$
$$K_C = D$$
$$J_D = 1$$
$$K_D = 1$$

D Flip Flop

This flip flop has one input, D. The output at time $(\underline{n} + 1)$ is the same as the input at time $\underline{n}$; i.e., the flip flop is a one-bit time delay. The operating characteristics are shown in Fig. 11.

D	Initial State = 0	Initial State = 1
0	0	**0**
1	**1**	1

Figure 11. Operating characteristics of D flip flop.

The input pulse requirements for the D flip flop (Fig. 12) are read from Fig. 11.

Map entry	D
1	1
0	0
1	1
0	0
—	—

Figure 12. Input pulse requirements for D flip flop.

The rules for reading a map for the D flip flop are thus:

• Every **1** and 1 must be accounted for in the D input expression.

• Any — may be used optionally in the D input expression.

From the map in Fig. 2, the input expressions for the flip flop are read:

$$D_A = BCD + A\overline{D}$$
$$D_B = \overline{B}CD + B\overline{C} + B\overline{D}$$
$$D_C = \overline{A}\overline{C}D + C\overline{D}$$
$$D_D = \overline{D}$$

The input pulse requirements for the five flip flops discussed are summarized in Fig. 13.

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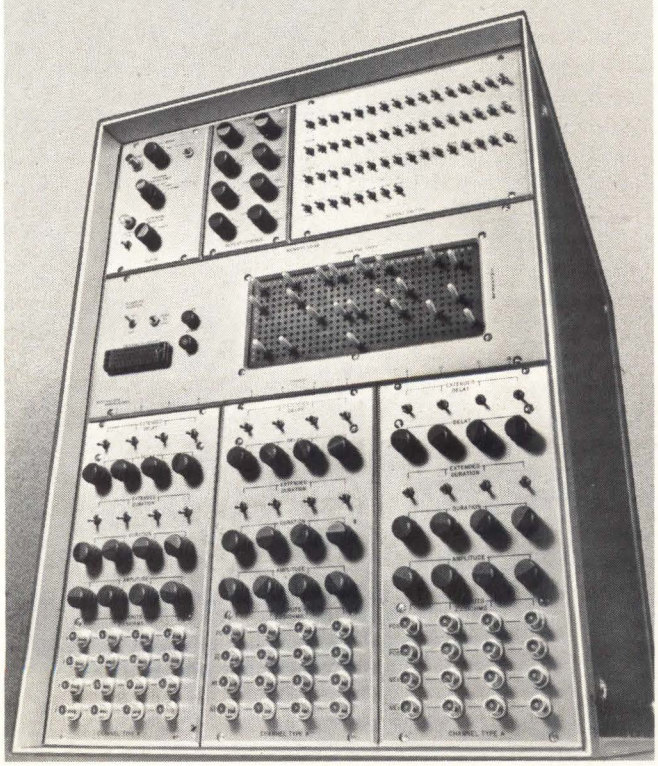

CIRCLE NO. 34 ON INQUIRY CARD

Map entry	T	S	R	S	R	T	J	K	D
1	1	1	0	1/—	0	—/1	1	—	1
0	1	0	1	0	1/—	—/1	—	1	0
1	0	—	0	—	0	0	—	0	1
0	0	0	—	0	—	0	0	—	0
—	—	—	—	—	—	—	—	—	—

Figure 13. Summary of input pulse requirements for the five flip flops discussed.

It has been shown how the single map is obtained from the flow table, how the map-reading rules are generated, and how the map is read for different types of flip flops. (The same procedure can, of course, also be extended to any other type of flip flop.) While the rules have here been formally derived, they can also be easily realized intuitively by simply considering the operating characteristics of each particular flip flop.

Inspection of the various input expressions derived in this example might lead to the circuit in Fig. 14. (The clock pulse is not shown.)

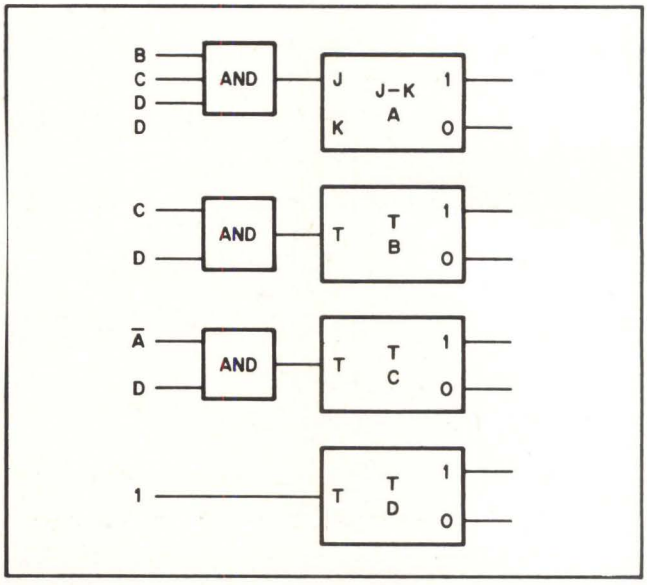

Figure 14. BCD Counter Circuit

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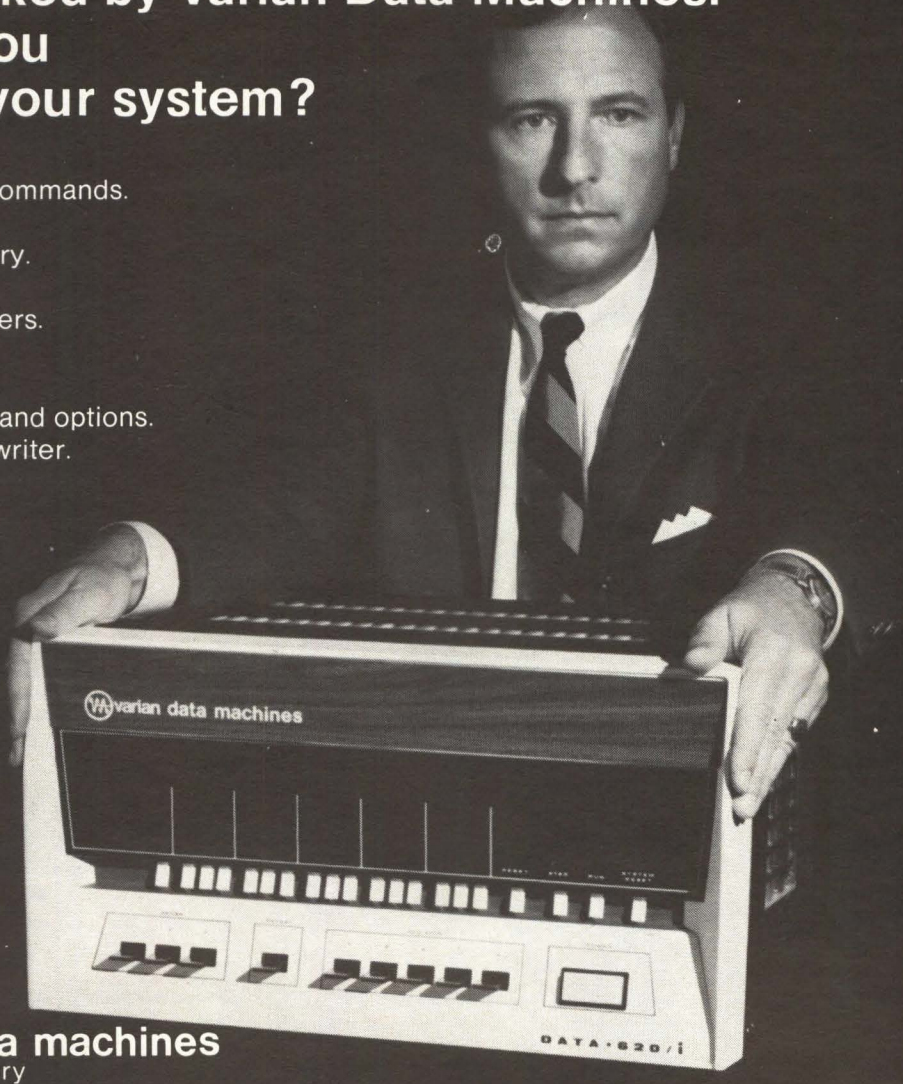

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Small, high-speed semiconductor memories designed to store the most recently-used information contained in the main memory can increase the effective speed of computing systems.

A PROPOSED ASSOCIATIVE

With the cost of semiconductor logic functions going down and the relatively slow speed of magnetic memories, there is a trend toward using small high-speed semiconductor memories to increase the effective speed of computing systems. Presented here is a logical design of a semiconductor memory capable of increasing the speed of such a system.

The function of the proposed memory is to store the most recently-used information contained in the main memory for immediate access to the processor. Instead of the processor having to access the main memory for every instruction and data word, it can first search the Associative Push Down Memory (APDM) for the word. If the word is present in the APDM, it can be accessed in a fraction of the main memory access time. If the word is not present in the APDM, it is fetched from the main memory and also written into the APDM. The APDM is limited in size and, therefore, each time a new word is written, a word must be discarded. The word discarded will have been in the APDM the longest time without having been accessed.

The memory is not restricted to this function, but may be used as a more "conventional" associative memory. If the physical capacity of the memory is exceeded, the oldest word is discarded. Multiple matches are not permitted and the address field is fixed.

Functional Description

The APDM is divided into three basic parts: **associative array, data array,** and **control logic.** (Figure 1)

The **associative array** consists of the address field and compares logic associated with each word location. In the APDM described, the address field is 16 bits. With 16 address bits, this memory may operate with 64K words of main memory. The associative array, therefore, comprises 16 memory cells/word, match compare logic with each cell, and one flag cell/word. Match compare logic is always active and compares the address field of each word to the incoming address lines. If each bit of the address field of a word matches each bit of the incoming address lines, a match signal is generated, except under special conditions to be described. The flag cell will also be described.

The **data array** consists of the data field and gated outputs associated with each word location. The data word length is also 16 bits. For each bit there is an output data bus that is activated by the word (if any) that has a match in its address field.

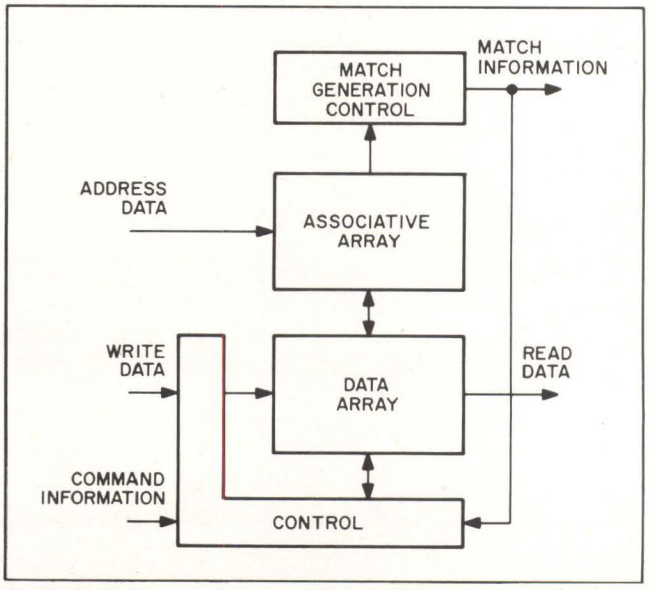


Fig. 1 Block diagram of the Associated Push Down Memory.

PUSH DOWN MEMORY

by
R. B. DERICKSON
Senior Systems Engineer
Fairchild Semiconductor

The **control logic** presets the APDM upon command. It controls writing, updating, discarding and the physical transfer of words, where a word consists of the address field and data field.

Theory of Operation

The APDM physically arranges its contents so that the most recently addressed word is at the top and the least recently addressed, or the oldest word is at the bottom. If a word in the memory is addressed, it is physically removed from its location and inserted at the top. This occurs on both read and write commands. In the case of a write command, the data field is changed to the incoming data. When a new word whose address is not already contained in the APDM is to be added, there is no room for the oldest word. This word must be discarded by transferring the next to bottom word into the bottom word location, followed by the word above that to the next to bottom word location, etc., until the top word has been transferred to the location below it. Now there is room to write the new word at the top.

It would seem that this transfer operation would be slow because 16 serial word transfers must be effected before the new word can be written. This problem may be circumvented by placing a buffer word location at the top, which is always ready to accept a new word. Now a word may be written in the buffer location at the same time the oldest word is discarded at the bottom. Before the next access to the APDM, the word transfer bubble has propagated from the bottom to the top and the buffer word location has transferred its contents to the next lower location so that the top location is again ready to receive a word.

There is an inherent cycle time limitation in the method just described. The cycle time of the APDM is limited by the bubble propagation delay (T_{bp}) from the bottom word to the top word. Of course, if the minimum time between accesses (T_a) is greater than T_{bp} there is no problem, but if T_a is less than T_{bp} then additional buffering is required at the top of the APDM. (More than one bubble is allowed to exist at one time.) The number of bubbles required equals the number of buffer words and is a function of T_a and T_{bp}. (See Figure 2)

The APDM described for illustrative purpose has a 16-word storage capacity and two buffer word locations ($T_{bp} < 2\,T_a$). By the time the third command arrives at the APDM, the bubble created by the first command has had time to propagate to the top.

$$\text{Bubbles} = \left[\frac{T_{bp}}{T_a}\right]^{*} + 1$$

*Where $[x]$ = integral part of x.

Number of Bubbles	T_a	T_{bp}
1	1	< 1
2	1	< 2
3	1	< 3
4	1	< 4

Fig. 2 The cycle time of the APDM is limited by the bubble propagation delay (T_{bp}) from the bottom word to the top word. If the minimum time between accesses (T_a) is greater than T_{bp} there is no problem, but if T_a is less than T_{bp} then additional buffering is required at the top of the APDM. The number of bubbles required equals the number of buffer words and is a function of T_a and T_{bp}.

As will be explained in the command section the discarded word need not be the bottom word, but may be any word in the APDM except the top buffer word. However, words are always written at the top.

The design of this system as shown is not dependent on any particular logic family, but for illustration a family was chosen having decision elements with the following characteristics: If all inputs are at a high logic level, the output assumes a low logic level; if the outputs of two or more decision elements are tied together, the outputs will assume a low logic level if all the inputs to any one of the decision elements are at a high logic level.

Commands

Preset Command:

The preset command is executed by a low logic level on the preset line and it has two purposes. The first is to establish the number of bubbles. This is accomplished by presetting all the word transfer control bistables (control cells) associated with storage word locations to the reset state, and all the control cells associated with buffer word locations to the set state. The control cells gate the inputs to the word cells from the next high word location. Their operation will be covered later in more detail. The number of control cells in the set state indicates the number of bubbles. Once the APDM is preset with the proper number of bubbles, this number will be preserved. Each time the top control cell is reset, a control cell is simultaneously set somewhere else in the memory. When the memory is not being exercised the bubbles accumulate toward the top, but cannot merge into one another.

The second purpose of the preset command is to empty the memory. This is achieved by resetting all the flag cells. If the flag cell for a given word location is in the reset state, no match may occur at that word location even if the address data agrees with the data field of that word. Each time a new word is written into the APDM the flag bit is set and it propagates down through the memory with the word.

This feature ensures that any random or not yet used portion of the APDM will not give a false response to a command, and also provides complete freedom for all 16 address bits.

Before discussing read or write commands it should be noted that the APDM must be in a stable condition in order to read or write. This means bubble propagation must be arrested during the command. Between commands, a bubble can always propagate at least halfway through the APDM. ($T_{bp} < 2\,T_a$) Thus if propagation is stopped as it reaches the middle word location, the APDM will always be in a stable state prior to the initiation of a read or write command.

Write Command:

This command is executed by a low logic level on the write command line and is divided into two categories: No-Match and Match. If a no-match exists by the trailing edge of the command, the word is transferred into the top of the APDM, the top control cell is reset and the bottom control cell is set. This bubble immediately starts propagating toward the top, transferring data downward as it goes.

If a match exists by the trailing edge of the command, the word is updated and transferred into the top of the memory, the top control cell is reset and a control cell is set at the location where the match existed. Writing in this fashion prevents multiple matches and updates the data with its associated address.

Read Command:

The read command is executed by a low logic level on the read command line and is divided into two categories: No-Match and Match. If a no-match exists by the trailing edge of the command no action is taken. (See logic diagram of center control cell, Figure 7. If this cell is set at the trailing edge of the command, bubble propagation will continue following the command.) If a match exists by the trailing edge of the command, the address data is transferred into the address field at the top of the APDM and the data outputs are transferred into the data field at the top of the APDM. The top control cell is reset and a control cell is set at the location where the match existed. The effect of this operation (similar to write) is to remove physically the addressed word from the APDM, move each word above one location downward, and reinsert the original word at the top.

Functional Description of Components

There are five basic functional blocks in the APDM: associative cell, data cell, flag cells, control cell, and write data control. Their quantities are shown in the table below.

Associative Cell	(16/Word $\times$ 18 Words)	288 Cells
Data Cell	(16/Word $\times$ 18 Words)	288 Cells
Flag Cell	(1/Word $\times$ 18 Words)	18 Cells
Control Cell	(1/Word $\times$ 18 Words)	18 Cells
Write Data Control	(1/Data Bit $\times$ 16 Bits)	16 Cells

Associative Cell:

An associative cell is a latch with a gated input and match gating to compare the content against the incoming address bit. The input is the content of the next higher associative cell in the same bit position. The input to a top cell is the incoming address data. The signal that allows the associative cell to assume the state of the input is present when a bubble is present in that word location (control cell is set). The match gating compares the double rail incoming address bit with the double rail content. The match output is tied to the match outputs of all the associative cells at that word location and is true only if all the associative cells of the word match their respective incoming address bits. Figure 3 shows the logic of an associative cell.

Data Cell:

A data cell is a latch with a gated input and output to a data bus. The input is the content of the next higher data cell in the same bit position. The input

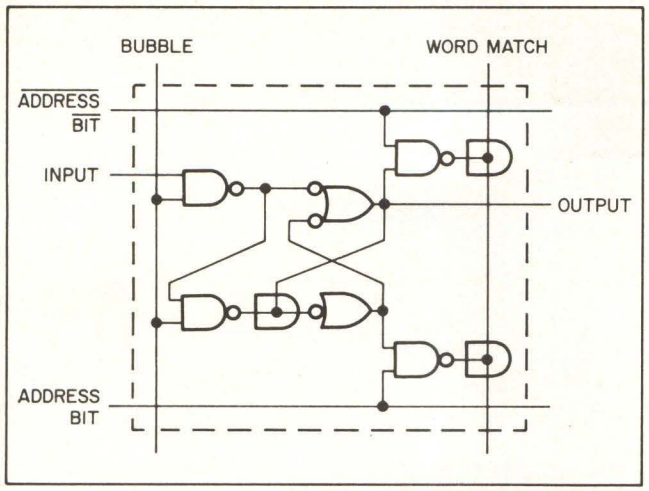


Fig. 3 Associative cell. As drawn, a columb of these cells constitute the bits of a word location. The higher words are to the left, the lower words are to the right.

to a top data cell is either the data bus or incoming write data. The signal that allows the data cell to assume the state of the input is present when a bubble is present in that word location. The signal that allows the content of the data cell to be transferred to the data bus is the presence of the match signal generated by the associative field of the word. (Figure 4 shows the logic of a data cell.)

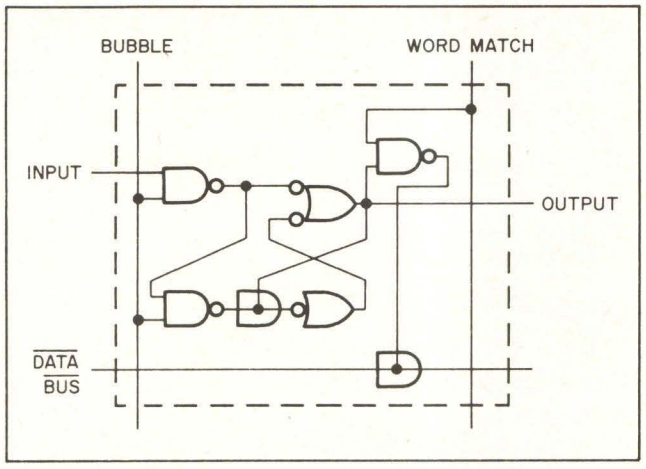


Fig. 4 Data cell. Drawn in same orientation as associative cell.

Flag Cell:

A flag cell is considered part of the associative array. When it is set it indicates that a word has been written at the word location. When it is reset it inhibits a match at the word location. The input to the top flag cell is a high logic level. Included in the flag cell is a gate preventing a match if a bubble is present. This is to prevent matches where bubbles have accumulated and to prevent multiple matches that would induce extra bubbles. (Figure 5 shows the logic of a flag cell.)

Control Cell:

A control cell is a word transfer control bistable that controls information transfer from the above word location to its controlled location. When a control cell is set, the corresponding word location assumes the

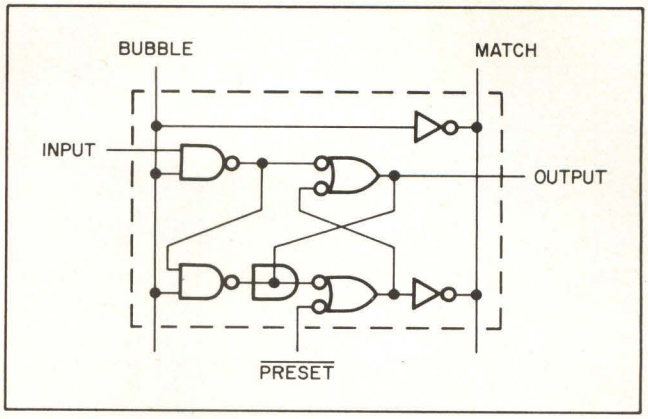


Fig. 5 Flag cell. As drawn, the higher words are to the left, the lower words are to the right.

state of the above word location. This word transfer includes the address field, data field and flag bit. During the time a given control cell is set a bubble exists at that word location. Although all the control cells are similar, four configurations are necessary: The top, center, and bottom cells are each unique; the remainder of the cells are typical.

Two stable states may exist after bubble propagation has ceased following a command:

(1) The top two control cells are set, all other control cells are reset.

(2) The top and middle control cells are set, all other control cells are reset.

Preset command presets the control cells to state (1). The APDM arrives at one of these states following each command and prior to the next read or write command.

Table 1 shows the control functions that set and reset the four configurations of control cells (excluding preset). The logic of the four configurations is shown in Figures 6, 7, 8 and 9. The following explains some signals that appear on these figures:

- $\overline{\text{Bubble}}$ (next higher) is true if the next higher control cell is reset.
- $\overline{\text{Bubble}}$ (next lower) is true if the next lower control cell is reset.
- $\overline{\text{Command}}$ is a signal to eliminate a race condition at the trailing edge of a read or write command. It is generated as shown in Figure 10.
- $\overline{\text{Data Bus}}$ (2^i) is one of the 16 data outputs.
- Match is the inversion of no-match where no-match is shown in Figure 12.

Write Data Control:

The input to each top data cell is controlled by the write data control logic. Its function is to gate either the data busses or the write data into the top data cells during a read or write command. The logic of one data control line is shown in Figure 11.

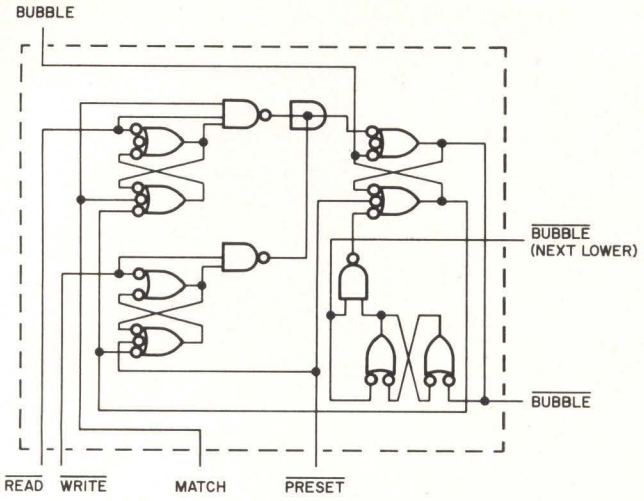


Fig. 6 Top control cell.

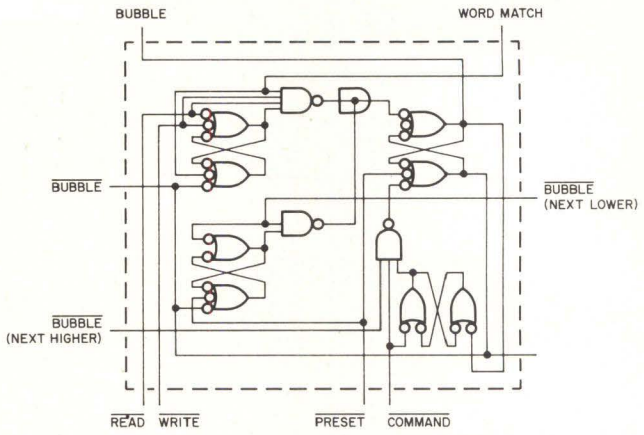


Fig. 7 Center control cell.

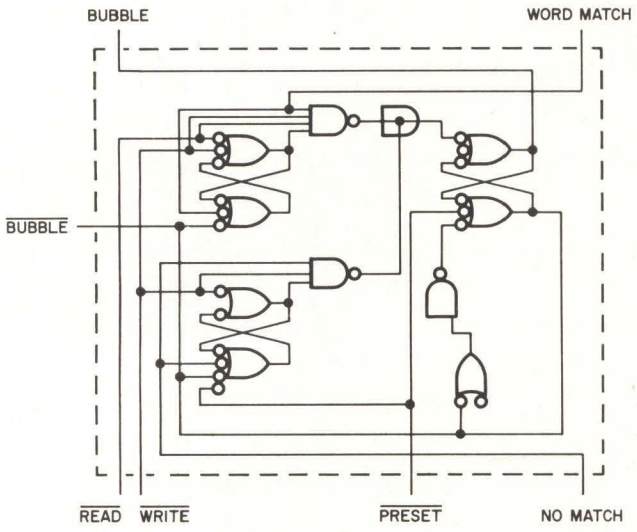


Fig. 8 Bottom control cell.

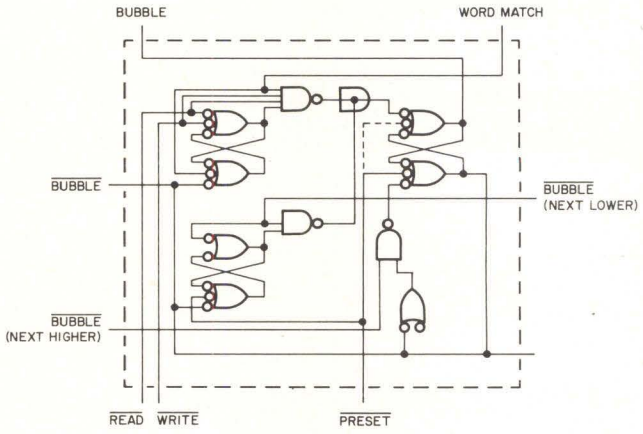


Fig. 9 Typical control cell. Note preset may set the control cell indicated by dashed line. The dashed-line configuration is used on the cell below the top cell.

Component Configuration:

The diagram in Figure 13 shows the organization of the APDM. All cells are oriented as shown in their logic diagrams.

Special Considerations

Considerations that are mentioned here briefly but will not be covered in detail are fan-out and loading. These factors have significant effect on the amount of circuitry and speed. Since the system has not been committed to a logic family, arbitrary rules have been assumed. Each gate presents a unit load. The number of gates in a single "or-tie" may be no more than 40. This presents no problem since the maximum number in this system is 34. Gates may fan out to no more than 10 loads. Drivers may fan out to no more than 50 loads. The following signals have an effective fan-out of >10 and <50, requiring drivers: address data (32 signals), preset, and word match (17 signals). write, read, and bubble (18 signals) each have an effective fan-out of >50. Two drivers are required for each of these signals. The total number of drivers under the above assumptions is 90. These drivers do not appear in the block diagrams.

Timing:

Figure 14 shows the bubble propagation time from a control cell to the next higher control cell. Since the system has not been committed to a logic family, the unit of time is one gate propagation delay. The control cell is held set for five propagation delays to ensure transfer through associative and data cells (3 delays required, two delays if no tolerance is considered between gate delays in assocative and data cells). The five delays through the control cell is accomplished by inverting the bubble output instead of merely using the bubble output to reset the cell. The bubble propagation rate is 1/6 times the gate delay time since the setting of one bubble cell to the setting of the next is six delays.

command goes low two propagation delays after read or write go low, but command does not go high until read and write have been high for six propagation delays. This is to allow the next higher bubble to be set at the trailing edge of a command before command goes high. The signal is used only with the middle bubble cell and prevents two bubbles from merging.

The total time required from the initiation of a command until the match output may be sampled is

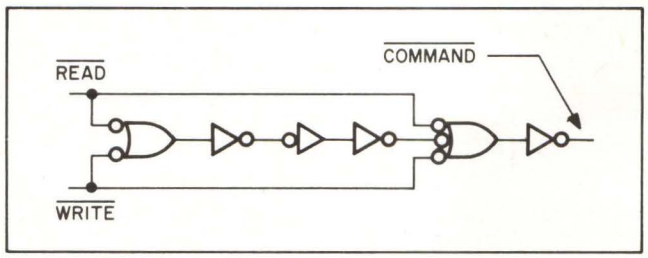


Fig. 10 Generation of command.

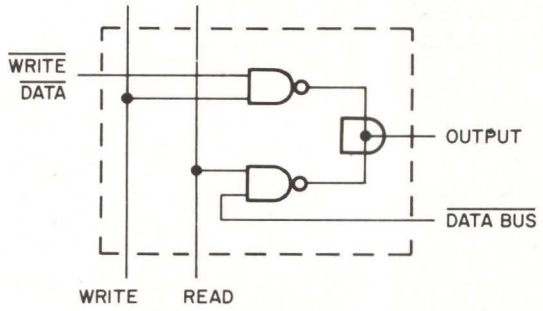


Fig. 11 Write data control where write and read are logical inversions of write and read.

four gate propagation delays; this includes two levels of drivers (match and address). The output $\overline{\text{data}}$ may be sampled at the same time as $\overline{\text{match}}$. This assumes that address data and a command occur at the same time. Actually, $\overline{\text{match}}$ and output $\overline{\text{data}}$ may be sampled after three gate propagation delays from change of address data, *without* the presence of a command,

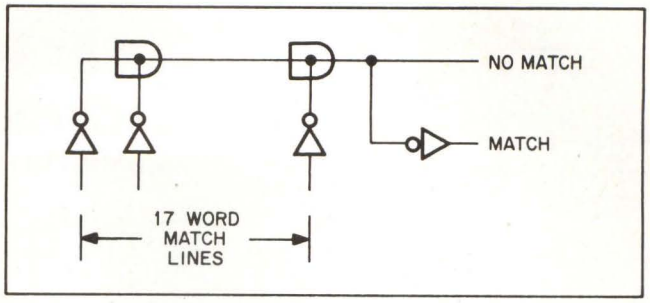


Fig. 12 Generation of no match and match.

and the APDM is in a stable state. The command need only be present for two delays. If the system using the APDM has a command repetition rate that is slower than T_{bp} then the APDM control cells may be simplified to always reset after five propagation delays (excepting the top cell). No center cell configurations would be required and *command* would not be generated.

The worst case recovery time for this APDM is 56 gate delays. The time is measured from the trailing edge of a command that causes the bottom control cell to be set until the center control cell is set and settled. Time from trailing edge of a command until trailing edge of bottom bubble is seven gate delays plus one driver delay. Time for bubble propagation from next to bottom cell to center cell is seven cells times six gate delays. Time for center cell to set and its data to settle is six gate delays. Slightly less recovery time is required from the center cell to the top cell. The aforementioned times do not account for any toler-

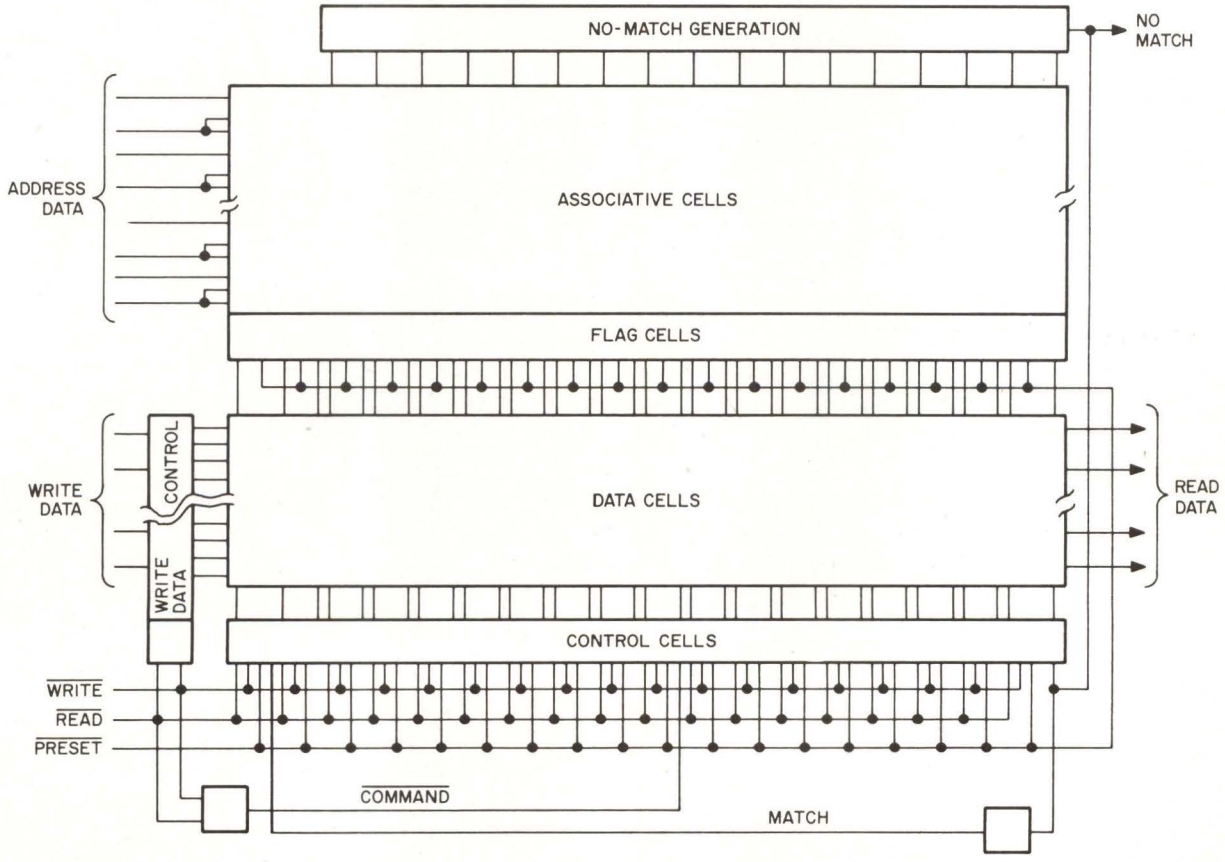
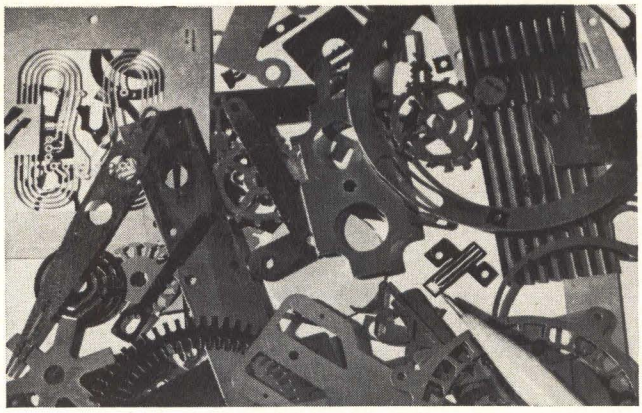


Fig. 13 Organization of APMD. All elements are oriented as shown in previous figures.



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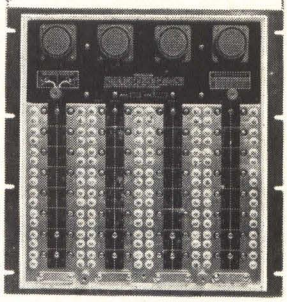

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ances, therefore worst case unit gate delays must be assumed.

If 56 gate delays (T_a) is not tolerable, then control cells that are in the configuration of the center control cell (hold configuration) must be more closely spaced and the number of bubbles must be increased. An example will illustrate: Maintaining the same storage capacity of 16 words and allowing four bubbles rather than two, the spacing between hold configuration cells becomes five rather than nine. Two buffer words must be added at the top. T_a now becomes 32 gate delays. It should be noted that for a given T_a, as the capacity of this type APDM is varied, the required number of bubbles is a fixed proportion of the capacity.

Conclusions

The technique of transferring data through simple dc latches reduces the cost of an APDM by avoiding more complex edge-triggered storage cells. Although there is significant control, it becomes a smaller proportion of the system as the memory size increases. Even though transfer of information is not a one clock synchronous step, but a ripple similar to that of an adder, it can be made to operate at fast access and cycle times.

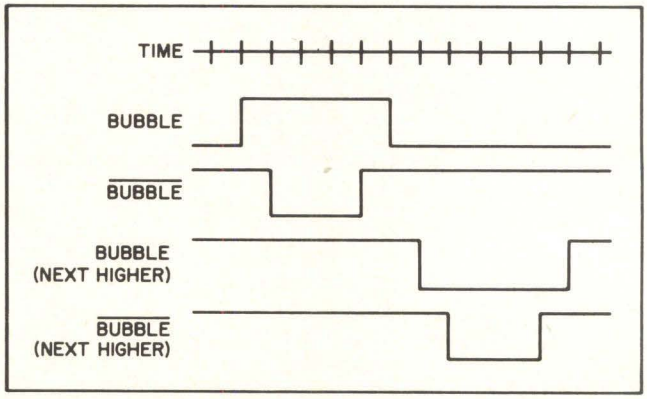

Fig. 14. Bubble propagation in units of gate propagation delays.

With a number of identical cells in an APDM, there is a potential for numerous identical LSI packages. This reduces the potential price further. For very high speed circuit families, however, (i.e., CML, CTL) the scale of integration on a chip is limited due to power dissipation. To increase the scale of integration a hybrid approach may be used (at some sacrifice of speed). For example, the memory array may be TTL which may directly interface with CML or CTL. Using the highest speed logic throughout, a single chip in a 16-pin DIP could accommodate six associative cells, 3 words $\times$ 2 bits. The system would then require 48 such chips. Assuming the associative cells comprise about one-third of the APDM electronics, the system could be included in about 150 packages. Of course, as the scale of integration is increased the number of packages would decrease along with cost and speed.

This type of memory may have other applications where the address field is fixed and multiple matches are not desired. If the application has no high speed requirements, the APDM could be realized using other technologies such as MOS.

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Operating simplicity, minimum cost, sophisticated programming and graphical display capability are achieved in the design of an input-output terminal.

THE AMTRAM INPUT-

The evolution of interactive conversational mode computer systems heralds an era in which scientists and engineers will employ digital computers with the ease and facility presently possible only with slide rules and desk calculators.[1,2] Flexible access and rapid response to problems is a particularly timely computer development in view of the increasing magnitude and complexity of scientific and engineering problems. Significant impetus to the actual development of "on-line" computing systems has been provided by scientists and engineers, frustrated by long "turn-around" times and inflexible computational arrangements. Fundamental to all interactive computer systems are the sophisticated software packages being developed to implement the conversational mode; however, conversational flexibility has been enhanced considerably by special input-output terminals. One of the more advanced interactive systems is the AMTRAN (Automatic Mathematical TRANslation) system, the development of which was begun in late 1964.[3,4,5] A description of the input-output terminals developed for the AMTRAN system follows.

The AMTRAN system was first implemented on the IBM 1620 computer. Availability was the principal motivation for selecting the 1620; nevertheless, its small size and low cost permitted adequate access for development of the basic AMTRAN system. The latest version of the input-output terminal for the 1620 system is shown in Figure 1; the major elements are two storage oscilloscopes, a large function keyboard, and a typewriter printer. A terminal connected to a Burroughs B5000 computer via a voice-grade telephone line has been in operation for several months, and a prototype terminal for the IBM 1130 computer (Figure 2) is nearly operational. An additional capability is being introduced on the 1130 system — multiterminal operation. Three terminals will be interfaced to an 1130 for the initial multi-terminal configuration.

Development of the 1620 AMTRAN terminal began shortly after software development, and close coordination between hardware and software has been continuously maintained. This has contributed immensely to the over-all efficiency of the system. For example, considerable terminal simplification was realized through a decision made early in the development of the system that construction of alphanumeric characters on a storage scope would be performed by software rather than by the more conventional hardware character generation techniques. This is economically attractive with storage scopes, because it is unnecessary for the computer to continuously regenerate display information.

General Considerations

Experience with the development and operation of the AMTRAN system has pinpointed a number of desirable input-output terminal characteristics, principally the following:

Figure 1 Input output terminal for 1620 system.

(1) convenient location
(2) simplicity of operation
(3) sophisticated programming and graphical display capability
(4) low cost

Although these characteristics are not absolutely compatible, acceptable compromises are possible.

The most convenient location for the average user would probably be on or near his desk. Unfortunately, this would require a very large number of terminals which would lead to a prohibitive over-all cost. A more realistic arrangement would entail the emplacement of a few terminals in a centrally located room. These terminals could then be connected di-

OUTPUT TERMINAL

L. H. WOOD, C. A. ELY,
H. GLANZER, and V. RADICE

rectly to a large central computer, or to a smaller satellite processor and thence to a large computer. The advantages and disadvantages of these alternate modes of connection will be discussed later.

Simplicity of operation involves the language employed to communicate with the computer and the operation of the terminal. The AMTRAN language has been the subject of other papers[3,5] and will not be discussed here except to state that it is well suited for conversational-mode problem solving. The simplicity of terminal operation implies a minimum of effort necessary to enter and extract information. Also, the amount of instruction necessary to use the terminal should be minimized. All these considerations led to

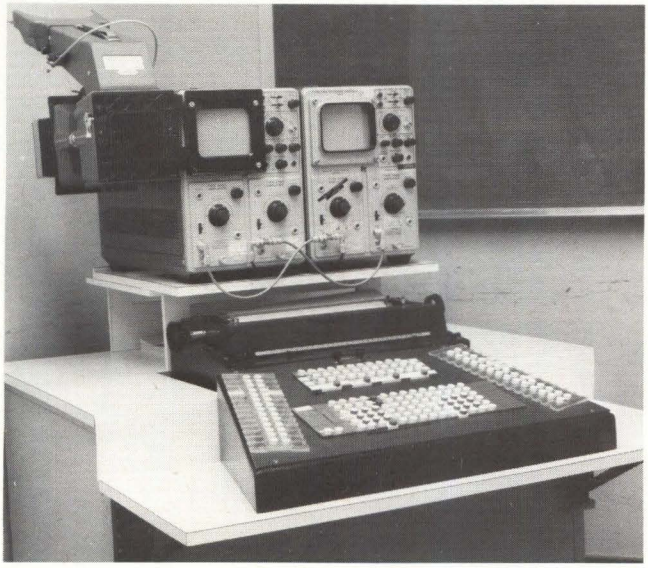


Figure 2 Prototype terminal for 1130 computer.

the choice of the large keyboard which permits input of information with a single button push. Output information is displayed on two storage oscilloscopes and a typewriter printer.

The sophisticated programming capability of the AMTRAN system is realized primarily through the system software; however, the input/output terminal greatly facilitates programming by relieving the user of many details and allowing him to concentrate upon the problem. Advanced graphic display is provided by two storage scopes: an alphanumeric scope and a graphical scope.

Programming via the terminal is initiated with the keyboard. Typical keyboard layouts are shown in Figure 3. Individual buttons on the keyboard are used to enter instructions or data into the computer. Immediately after accepting information generated by a

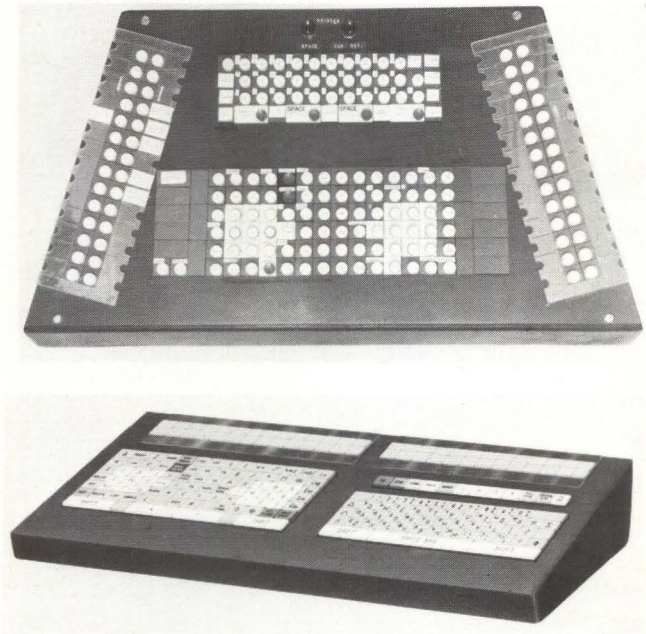
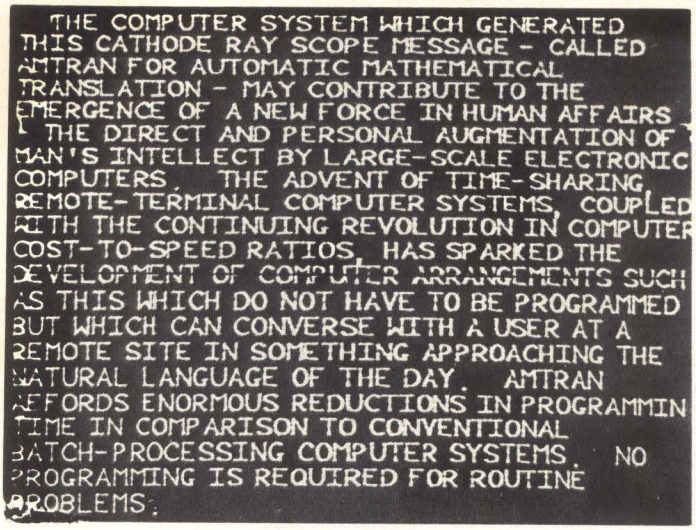


Figure 3 Typical keyboard layouts

button push, the computer displays the label corresponding to the instruction or data associated with the button upon the alphanumeric scope. For example, if the COS button is pressed, COS is printed on the storage scope. Typical alphanumeric displays are shown in Figure 4. Input of information with a single button push and the automatic formating and display of labels corresponding to each button push are key features of input-output terminal programming which are responsible for a decrease in errors and much faster programming. Instructions and data are constructed by the user and processed by the computer a line at a time. If, during the development of a statement, any



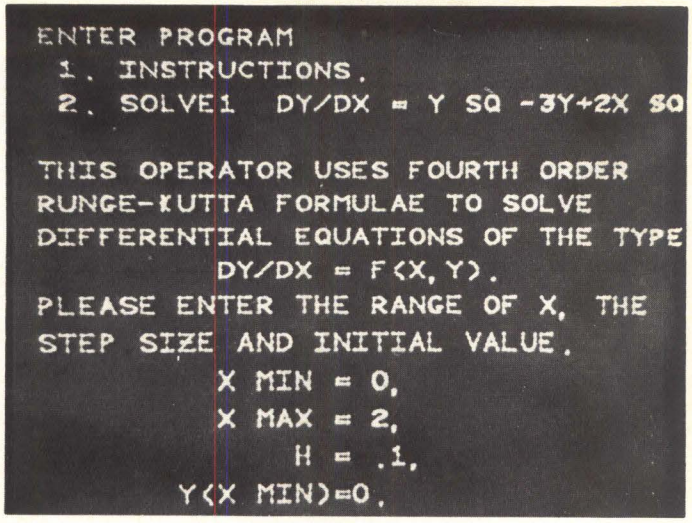


Figure 4 Typical alphanumeric display

change, such as deletion or addition of information, is desired, a backspace and erase capability is provided. Once the user is satisfied with a particular statement, he presses a "terminate" button; the computer then records the statement on the typewriter printer. A graphical display of any particular calculation can be exhibited upon the graphical display scope with the appropriate instruction button on the keyboard. The variety of graphical displays which are possible are shown in Figure 5.

The cost of the AMTRAN terminal has been kept to a minimum through the coordination of software and hardware development and by modularization. Approximate component cost for the IBM 1620 AMTRAN terminal is:

Typewriter/printer (IBM Model B)	$1600
Storage Scopes (Tektronix 564) (2 ea.)	2600
Keyboard	1300
Electronics (discreet component PC Boards)	4000

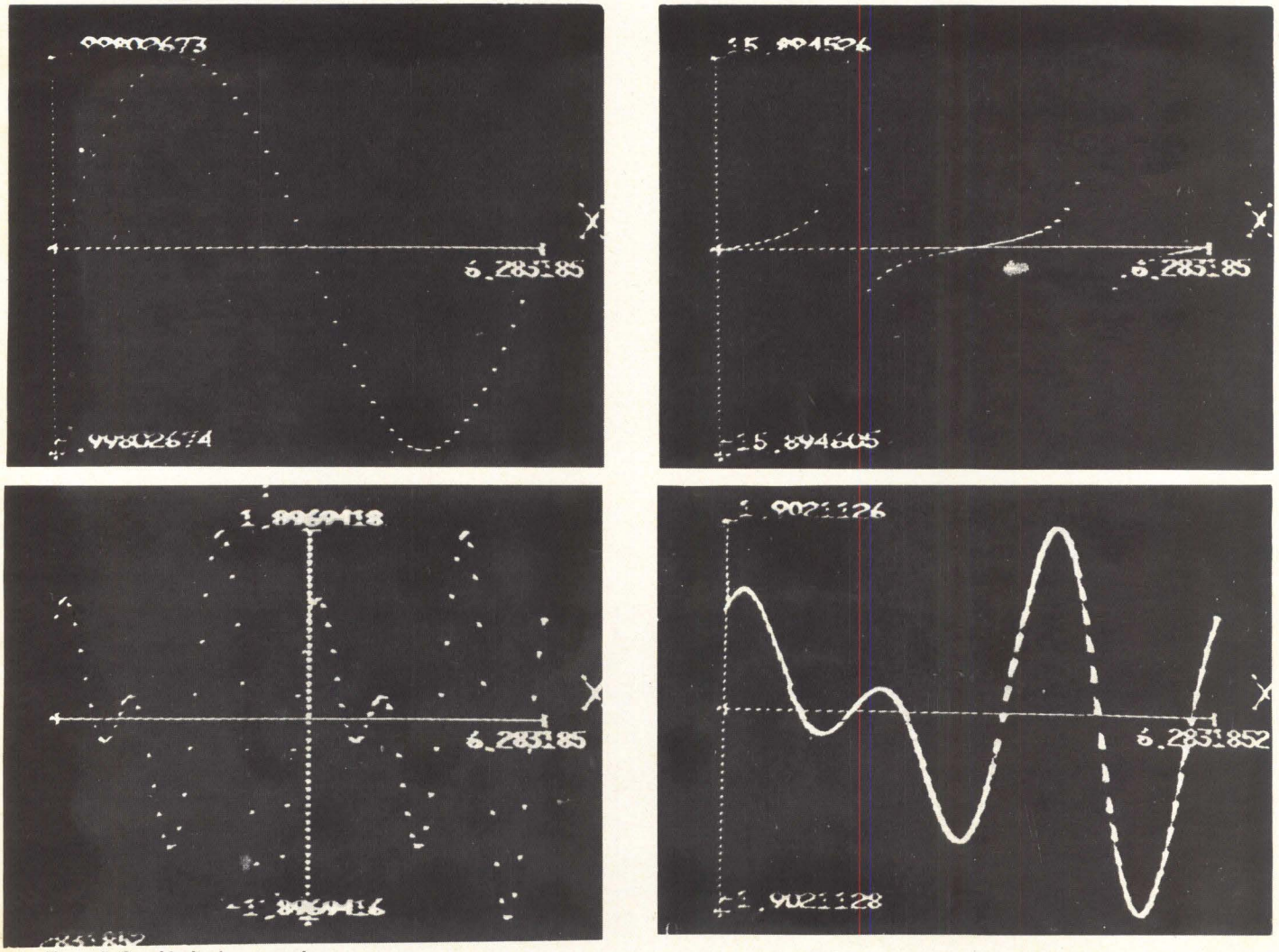


Figure 5 Graphic display examples

If $3000 is added for fabrication and miscellaneous expenses, terminal hardware cost is only $12,600.

No attempt was made during the early terminal development to arrive at a particularly sophisticated design. Hence, discrete components and "AND-OR" logic were employed in the initial electronics design. At present, integrated circuits and other refinements are being incorporated in the terminals which should reduce terminal cost even more. Also, reduced versions of the terminals are possible (e.g., one oscilloscope or a smaller keyboard) which should permit terminal costs approaching $5000.

The Amtran Graphics Terminal

A block diagram illustrating the basic AMTRAN terminal is shown in Figure 6 in which the basic electronic interface elements are delineated. The input/output register accomplishes voltage and logic level interfacing, and the control functions are modularized so that the basic terminal design can be adapted to a variety of needs. Historically, the development of the oscilloscope portion of the terminal was begun first; then came the keyboard and printer, and the rapid data-input device was added last. The rapid data-input device, which operates somewhat like a "stylus," is needed because the AMTRAN system operates on functions rather than discrete data. Therefore, the ability to input a large amount of data, such as an initial function, is highly desirable. Two available possibilities, light pens and analog-to-digital devices, have been considered for AMTRAN and will be discussed in detail below. The physical arrangement of the input-output elements has evolved considerably during the development of the AMTRAN terminal, as can be seen by comparing the 1130 and 1620 terminals.

During the initial AMTRAN system development, it quickly became apparent that there was insufficient core storage available in the 1620 to permit continuous regeneration of data for graphical display. However, it did appear possible to generate the data for one-time display; hence, came suggestions of using storage scopes to retain the data. While storage scopes are more expensive than TV monitors, they are less expensive than the necessary character-generation hardware located in terminals using TV monitors. Furthermore, the storage scopes are definitely less expensive than the core storage necessary for continuous generation of display data. The storage scopes initially available were too small and were not designed for high resolution making high-quality graphical display difficult to achieve. However, as seen in Figures 4 and 5, the displays are adequate; furthermore, increasing interest in the application of storage scopes to low-cost terminals has prompted the development of a new high-resolution 11-inch (diagonal) storage scope by the Tektronix Corporation.[6] This new storage oscilloscope, designated the 611, will cost approximately $2500, and is designed specifically for high-quality visual display.

It should be noted that the storage oscilloscope not only eliminates the need for auxiliary buffer storage containing a million bits of information, but it also

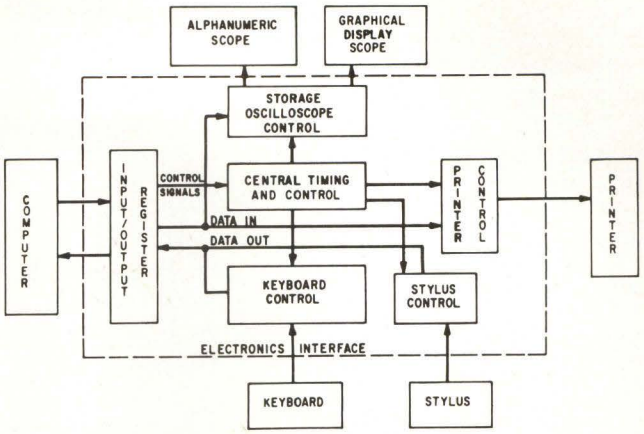


Figure 6 Basic Amtran terminal block diagram

permits a more leisurely flow of information from the computer to the display device. The raster of a typical television monitor must be repeated approximately 30 times a second for flicker-free display; whereas, the storage oscilloscope display, which is only drawn once, can be built up as slowly as necessary. For example, the display of 2,000 characters upon a conventional alphanumeric display scope requires a writing rate of 60,000 characters per second. This permits only 16 microseconds per character to draw and position it on the scope face. Consequently, special high-speed character generation hardware is necessary. On the other hand, with storage scopes writing texts at 600 characters per second, the characters may be drawn slowly by the software as a series of short-line segments. Slow writing rate is particularly useful when operating over a phone-line which may be limited to 2400 bits per second. Typical experience with the AMTRAN system has indicated that a single item of data may be retained for several minutes before being erased (e.g., a user may have to check an equation or look up some data); therefore, a storage scope tends to eliminate highly repetitious data regeneration.

It thus appears that the storage scope is destined to play an important role in introducing true graphics terminal capabilities in the $5,000 to $15,000 price range within the next few years. For example, these considerations have led MIT's Electronic Systems Laboratory to invest some effort in the development of a low-cost graphics terminal based upon the new 11-inch storage scope.[7] The estimated production price of such a terminal, with typewriter keyboard and a graphic input device interfaced to a voice-grade telephone line, is believed by the developers to be approximately $5,000 to $10,000.

We hasten to point out that the use of a storage scope terminal places greater demands upon a central computer than the continuously refreshed terminals with their own buffer storage and line and character generation hardware. Also, the storage scopes are not well suited for dynamic motion picture displays. Finally, revision of any portion of the stored image requires that at least half of the scope face be erased and rewritten.

A block diagram of the oscilloscope control section

of the electronics interface is shown in Figure 7. Standard digit/alanalog deflection drive circuits have been employed. Some consideration has been given to dc analog amplifiers; however, the amplifiers present stability problems, and do not appear to offer any advantage over the more prosaic D/A converters. The two storage scopes utilize a common deflection circuit with the blanking circuit controlling the scope face upon which information is displayed. Although direct axis control is not standard on the Tektronix 564 oscilloscope, this capability can be added through a simple modification. This operational mode eliminates the need for dual deflection circuits or analog switching.

Alphanumeric characters are drawn on the oscilloscope face by first representing each character by a dot pattern. The computer presents the X and Y coordinates of each dot to the electronic interface in a predetermined sequence. The dots are then smoothed into a solid pattern for each character by attaching an R-C integrating network to the oscilloscope deflection circuit terminals. In essence, the R-C network converts each dot pair into a short vector. The R-C network can be switched on and off under software control thereby providing increased flexibility for both alphanumeric and graphical display. Finally, a remote erase capability under computer control is provided.

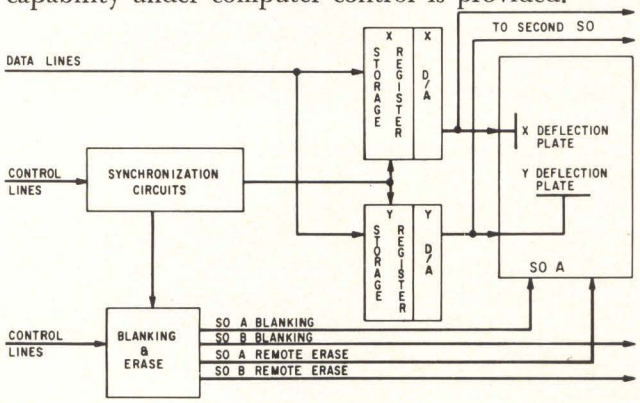


Figure 7 Storage oscilloscope (SO) control

One of the more controversial elements of the AMTRAN terminals is the large keyboard. The necessity and desirability of the large number of buttons (Figure 3) has often been questioned. After all, it is argued, does it not require a long time to become familiar with these buttons; furthermore, why not use the standard typewriter keyboard with which people are more or less familiar? The answers to these questions have become quite clear during the development of the AMTRAN system. The earlier versions of AMTRAN employed the typewriter associated with the 1620 computer for input and output of data. Mnemonic codes such as SIN, TAN, EXP, and DISPLAY were used to expand the capabilities of the 44 keys on the typewriter. In principle, this procedure should be quite straightforward; unfortunately, in an actual problem solving situation, the necessity to type in mnemonic labels leads to many errors. If one is concentrating upon the development of a particular mathematical expression, there is a tendency to misspell. Also, the software is greatly simplified, if spaces are placed between certain operations. For example, ABC is interpreted by AMTRAN as a program label, while A B C is interpreted as a product of A, B, and C. This tends to result in formating errors; therefore, automatic formating by the computer is very helpful. It has become clear that the number of steps necessary to enter information into the computer should be reduced to an absolute minimum, and for the input of mathematical statements, instructions, or data, the minimum is one button push. One of the distinct advantages of on-line programming with a keyboard terminal is that the user is freed from a great deal of the drudgery and routine associated with more conventional programming arrangements. Users of both keyboard and typewriter versions of AMTRAN have unanimously concluded that the keyboard is preferable. Keyboard familiarization generally requires some time; however, as seen in Figure 3, the AMTRAN keyboard is arranged in a logical manner, and the famaliarization period is usually short. It should be noted that the use of multiple levels (assigning more than one function to a button) to reduce the number of buttons has been omitted on AMTRAN. Again, simplicity of operation dictated this choice, since it is difficult to keep track of the level on which a particular item is located.

In Figure 3, note that there are basically two types of buttons on the keyboard: (1) pre-programmed buttons which call mathematical operators such as the arithmetic operations, the trigonometric functions and instructions such as SCOPE, ARRAY, and PRINT and (2) blank (unprogrammed) buttons. The preprogrammed buttons form the basic instruction set of the AMTRAN system, while the two rows of blank buttons on the left and right sides of the keyboard are available to the user who may assign a program he has prepared, to one of the buttons. Moreover, the programs assigned to the programmable buttons can be considered as subroutines and combined into more complicated programs. This concatenation can be continued almost indefinitely and thus permit the development of extremely powerful and complex programs. Two plastic overlays, provided for the programmable buttons, have slots in which a user can place the program labels after assigning a program to the button. The plastic plate is held in place with two quick-disconnect screws designed for quick removal. Label arrangements are shown in Figure 3.

In the block diagram of the keyboard control electronics section (Figure 8), it may be seen that each button push is stored in a flip-flop buffer register. The storage of the button push is necessary since the user and computer operate asynchronously to each other. After many design iterations, it was decided that the simplest and most reliable method of storing a button push would be to "clamp" the flip-flop collector lead. Each time the keyboard is "read" by the computer, the buffer is reset to zero in preparation for the next button push.

"Single-throw" buttons employed on the first keyboards were connected to the keyboard buffer through a complex diode matrix. The keyboard shown in Figures 2 and 3 uses the new microswitch KB buttons. Each button has eight contacts which can be preset for any binary number from 0-255, thus eliminating the need for a large diode matrix. Furthermore, the

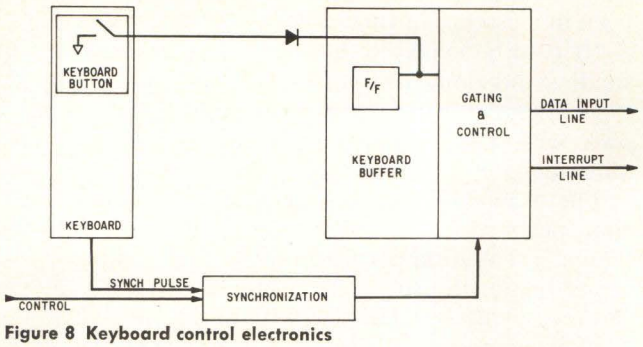


Figure 8 Keyboard control electronics

use of KB buttons, in contrast with earlier types, results in a much more compact keyboard. For a comparison, refer to Figures 1 and 2.

The keyboard can input data to the computer either passively or actively. A passive mode is employed with the 1620 system in which the computer automatically samples the keyboard every 100 milliseconds whether or not a button has been pressed. After data is entered into the buffer, the terminal waits until the computer performs the next read operation. The active system employs an interrupt line, such as is available with the 1130 and most other late model computers, to signal the computer that the keyboard buffer contains data. The latter is a more efficient method; however, the user is unaware of the difference.

Upon receipt of a number from the keyboard, the computer stores the number along with any previous numbers forming a string of button codes. When the "terminate" button is pressed, the computer compares each number with a scan table and executes the operation or series of operations indicated by each number code. In this manner each button elicits a distinct response from the computer.

In Figure 3, note that within the AMTRAN keyboard is incorporated a standard typewriter keyboard; consequently, the keyboard on a standard input-output typewriter is unnecessary. INVAC printers have been used on the latest versions of the AMTRAN system. These are modified IBM selectric typewriters; the character set available is shown in Figure 9 together with an equation typed with one of the printers. The equation was typed using the unique forward and reverse indexing capability of the INVAC printer. One of the difficulties in standard programming is the required linear format for mathematical equations. If the equation is at all involved, linear formating requires many parentheses the placement of which becomes somewhat tedious and leads to errors. Therefore, one of the early requirements for AMTRAN printers was the capability for forward and reverse indexing which would permit more natural formating of equations.

] 2 3 4 5 6 7 8 9 0 - = 0 1 2 3 4 5 6 7 8 9)

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Figure 9 Character sets available and sample equation

A block diagram of the printer control electronics is shown in Figure 10. A "one-shot" multivibrator is employed to provide timing for the electromechanical actuation of the printer functions, while a flip-flop controls the machine functions. The particular data input arrangement corresponds to the INVAC printer which has a built-in decoder, but a similar arrangement would apply to other printers.

Rapid data input from the AMTRAN terminal is accomplished by an Analog-to-Digital "stylus." This input mode was selected on the basis of the following data-input device requirements:

1. Mounting of stylus on the oscilloscope face to assure ease of operation

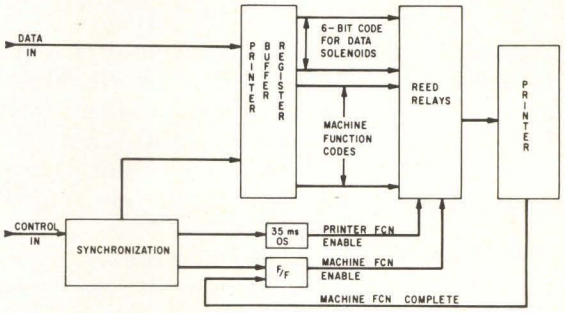

Figure 10 Printer electronics

2. Minimization of hardware cost
3. Suppression of redundant data at the terminal rather than in the computer
4. Resolution: approximately 250 points/inch

These considerations eliminated the use of the more conventional light-pen devices, principally, because the light-pen requires the continuous generation of a raster which would substantially increase terminal cost and complexity.

The prototype stylus is composed of two arms with potentiometers installed at the extremities of the central arm (Figure 11). A microswitch connected to the Teflon stylus tip activates the data-input circuits.

The stylus data-input control circuit employs Analog-to-Digital Converters (ADC) and a digital comparator (Figure 12). The ADC channels convert the analog input from the potentiometers to digital form by the successive approximation method. When both channels have reached analog comparison, the contents of the ADC flip-flop registers are digitally compared with the last data sent to the computer which is stored in the storage registers. If digital comparison exists, a reset pulse is sent to the ADC registers and the cycle is reinitiated, thereby preventing input of redundant data. If comparison does not exist, the new data are transferred to the storage registers and transmitted to the computer by the output gating circuit. A reset pulse is then sent to the ADC registers and the sequence is recycled.

As mentioned above, the 1130 AMTRAN system will be established on a multi-terminal basis. A block diagram illustrating the terminal arrangement is presented in Figure 13. The input register performs logic and voltage level conversions while the output register

Figure 11 Phototype stylus

has the added function of multiplexing data from the three terminals. The three terminals are identical. They are arranged as shown in Figure 6, except that the central timing and control circuits are combined into a single interface control circuit, which also provides control signals (e.g., gating and timing pulses) to the 1130.

In principle, a large number of terminals could be accommodated on the 1130; however, the practical number depends upon the over-all mode of operation of the 1130. If the 1130 is to "stand alone," then core storage and computing speed will probably limit the number of terminals to between three and five. However, if the 1130 is connected to a larger computer, either by a direct interface or over a telephone line, then it may be possible to attach as many as ten terminals. The latter arrangement has much in its favor. From the brief description of AMTRAN programming given above, it is clear that a large number of very routine tasks are performed by the computer during

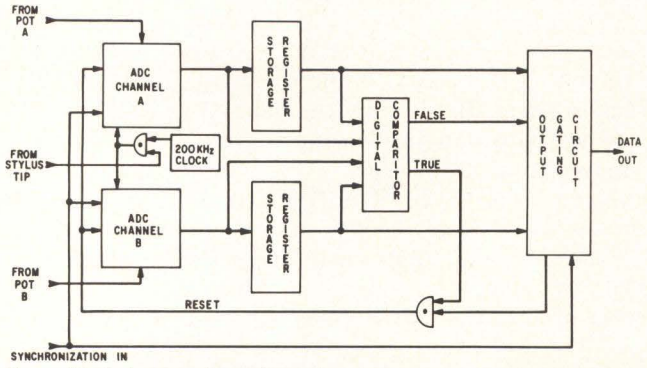

Figure 12 Stylus data-Input Control

the development of a program. Such activities as label formating and editing, while of considerable value to the human operator, do not require the services of a multi-million-dollar, third-generation computer. On the other hand, after a program has been established, rapid response to the more involved calculations will necessitate a large computer. Hence, an arrangement such as suggested in Figure 14 appears highly desirable. Multiterminal operation for banks, airlines, and similar groups are now becoming commonplace and multiterminal operations for scientists and engineers have been in existence in various forms for many years.[8]

"It is to be expected, however, that in the long run small stand-alone computers will be replaced by remote consoles with some processing ability of their own, with a large computer in the background available when needed."[2]

The exact dividing line between a "small" calculation performed by the satellite processor and the "large" calculation performed by a large computer will depend upon the user. It is hoped that some of the answers to these questions will be known when the 1130 is connected to the Univac 1108 now being installed at Marshall Space Flight Center.

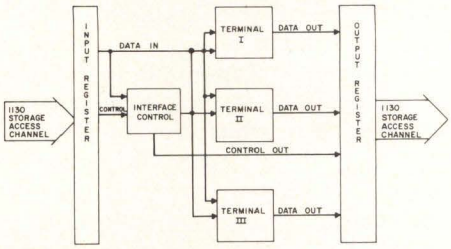

Figure 13 Amstran IBM 1120 Multiterminal Arrangement

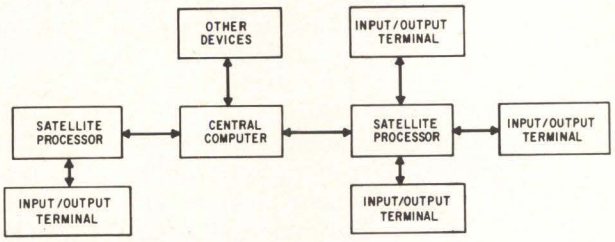

Figure 14 Possible Amstram – terminal satellite – processor central – computer arrangement

Summary

The principal design goals of the AMTRAN input-output terminal have been simplicity of operation and minimum cost while providing sophisticated programming and graphical display capability. These goals have been achieved through the use of a large function keyboard, two storage oscilloscopes, a typewriter printer, and a rapid data input stylus. The first terminal was interfaced to an IBM 1620 computer and has operated reliably for over a year. Development of a terminal interfaced to an IBM 1130 is almost completed, and an experimental voice-grade phone line interface is operational.

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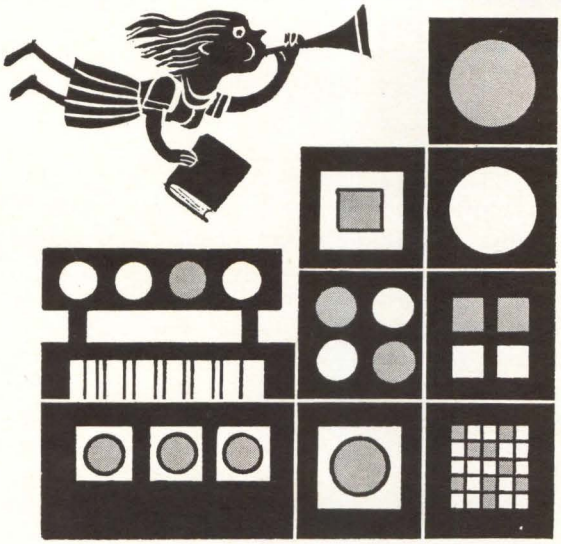

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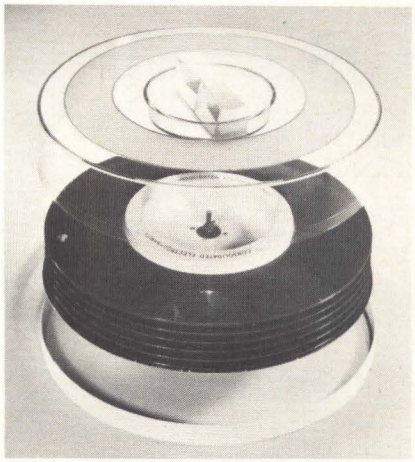

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QUAD-PACK PULSE TRANSFORMER

Said to be one of the smallest configurations of its type, this Quad-Pack unit consists of four encapsulated transformers designed to drive a transistorized switch on memory cores employed in computers and related equipment.

Only 7/8 in. x 1/4 in. x 3/16 in., the device contains miniature ferrite toroids designed to meet Mil-T-21038 and gold plated leads of nickel-iron-cobalt alloy (KOVAR, Type K) per Mil-Std-1276. Unit features a primary sine wave inductance of 400 microhenries, min. Rise time: 8 nanoseconds, max. Primary to secondary leakage inductance: 1.5 microhenries, max. PCA Electronics, Inc., Sepulveda, California.

Circle No. 212 on Inquiry Card

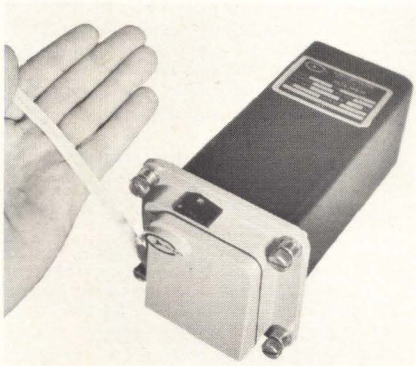
ELECTRONIC COMPOSITION SYSTEM

Videocomp typesetter combines computer and television techniques to set text in sizes from microimage to letters over an inch high at rates of up to 6,000 characters per second. The all-electronic typesetter can set the complete text for a magazine page in less than four seconds or write information for microfilm storage at computer speeds.

Videocomp stores typefonts in electronic memory where they can be used instantly. This internal storage reduces the load on computer memory and permits use of the equipment off-line with any computer.

Because the entire operation is electronic, every letter can be altered electronically to form roman, oblique, extended, condensed and superior and inferior versions of the basic face. Every face, in every variation, can be mixed at will — on the same line, in the same word — with every other face. RCA Graphic Systems Division, Dayton, N. J.

Circle No. 232 on Inquiry Card

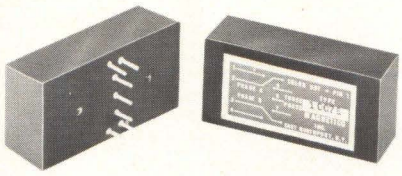


MIN-STRIP PRINTER

A miniaturized strip printer with only 6 moving parts has been designed to meet applicable sections of MIL-E-5400, MIL-E-16400 and MIL-E-5272 with a 5,000-hour M. T. B. F. in military airborne and mobile applications.

Printer height and width is 3" x 3" with a depth requirement of 6 1/4", including the control electronics. Total weight is less than 4 lbs. The printer has full 64-character alpha-numeric (ASC11 code) selection and a printing speed of up to 1500 characters per minute. The AN-16 is designed for front cartridge loading to allow for rapid paper change. Standard input power is 28VDC plus DC logic voltages, options permit 115V, 400 cycle AC. Clary Corp., San Gabriel, Calif.

Circle No. 211 on Inquiry Card



MATCHED TRANSFORMERS

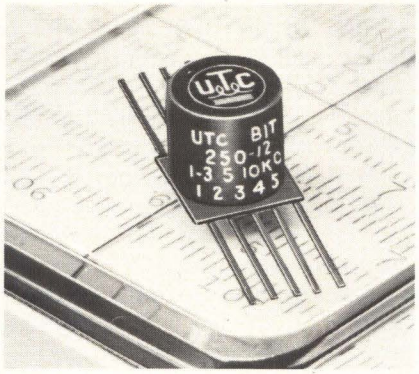
A series of matched transformer pairs, which isolate resolver outputs with 2 seconds of arc accuracy, are precision miniature toroidal units designed to fit on PC boards. They are designed to handle virtually any application requiring resolver to digital and digital to resolver conversion, including multiplexed systems. The transformers will meet the requirements of MIL-T-27B, and weigh 5 ounces each. Magnetico Inc., East Northport, N. Y.

Circle No. 225 on Inquiry Card

MAG TAPE REEL GAUGE

Mechanical gauge for field-checking magnetic tape reels checks the most common source of reel failure, bent and distorted flanges. The gauge consists of a precision base plate, a manually rotatable spindle, and three gauge posts. The three posts are accurately machined to test a wide variety of instrumentation, video, computer, and sound recording reels. General Kinetics, Reston, Virginia.

Circle No. 207 on Inquiry Card

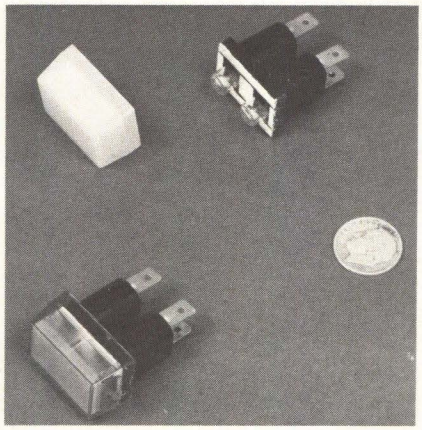


TRANSISTOR TRANSFORMERS AND INDUCTORS

New line of ultraminiature transistor transformers and inductors, called the BIT-250, is said to achieve outstanding reliability in a size compatible with flat pack transistors and integrated circuits, while maintaining response and power levels found only in large units. A substantial size reduction (profile height .250") without sacrifice in reliability is obtained through cylindrical winding techniques.

All units are manufactured to MIL-T-27B, Grade 4, assuring ruggedized construction. The line contains 17 stock units available for immediate delivery. United Transformer, New York, N. Y.

Circle No. 208 on Inquiry Card



TWIN-LIGHT CIRCUIT INDICATORS

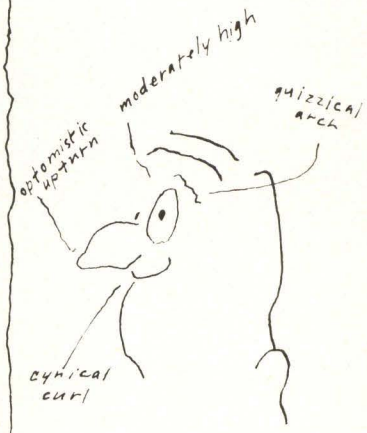
Three dual lamp, long-life circuit indicators, called "Twin-Lights", are available in three versions for 4 to 48-volt operation. The units measure approximately one inch in overall length, including their 1 x ½-inch lens covers. The lights are available in three standard configurations: the first has two quick-connect terminals for two light indication of a single circuit for fail-safe applications; a second includes three terminals for indication of two circuits with a common ground; the third, with four terminals, allows for two completely separate circuits. Sylvania Electric Products, New York, N. Y.

Circle No. 223 on Inquiry Card

LENSLESS LAMP CARTRIDGES

Miniature lamp cartridges, constructed without lenses, are intended for use in computers, display panels, etc. The lens is part of the matching lampholder and can be replaced or maintained separately from the lamp cartridge. Industrial Devices, Edgewater, N. J.

Circle No. 204 on Inquiry Card



The guy we're looking for was born between 1934 and 1943. He's spent the rest of his life wondering why, and wondering about all sorts of cosmic things as well. Between musings, he graduated with an E.E. or M.E. degree, probably has a Master's Degree tagged on, and by now has been recognized by his peers for some major (or minor) achievement in computer-related diggings around—man-versus-machine, etc.

If you are this guy and have digital experience in engineering, production, marketing or management, contact John Link, Personnel Director, Electronic Memories, Inc., 12621 Chadron Ave., Hawthorne, California 90250. (213) 772-5201.

CIRCLE NO. 39 ON INQUIRY CARD

Any day now you computer people will make an incredible discovery:

Nobody has made custom power supplies longer than Varo.

Or with a better performance record.

Or to tougher mil specs.

Funny we haven't crossed paths with you folks.

Funny?

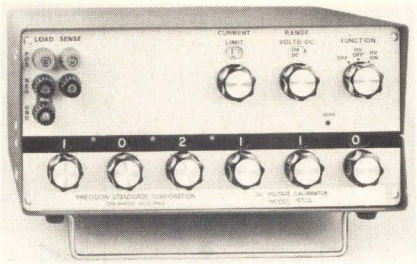
It's incredible!

Let's discover each other.

Write Rex Carter, Varo, Inc., Static Power Division, 1600 Dallas North Parkway, Plano, Texas 75074.
TWX 9108605640
TELEX 73-2713

VARO

CIRCLE NO. 40 ON INQUIRY CARD



DC VOLTAGE CALIBRATOR

Model 470A calibrator, with a voltage range of 0 to 1111.10 volts DC, provides a voltage accuracy (11 volt range) of ± 0.005% or 25 microvolts and resolution of 1 microvolt. Additional features include stability of 10 PPM + 10 microvolts per hour, 20 PPM + 20 microvolts per 200 hours, ripple and noise (.1 Hz to 1K Hz) of 100 microvolts RMS and output resistance of 0.001 ohm or 0.000 2E out at DC. Precision Standards Corp., Pasadena, California.

Circle No. 200 on Inquiry Card

250 MHz PULSE GENERATOR

Model 113, a 250 MHz pulse generator with built-in wide-range burst capability, offers both synchronous and asynchronous gating, + 2V to − 2V baseline offset (after the attenuator), simultaneous positive and negative 5V outputs and complementary outputs. Delays and widths are variable from 10 ns to 1000μs. Rise and fall times are 1.3 ns. Separate baseline controls, independent of amplitude controls, are provided for positive and negative outputs. The unit may be triggered externally. Datapulse, Culver City, Calif.

Circle No. 201 on Inquiry Card

BCD PRINTER

With a printing rate of one line per second, the Model 4500 BCD parallel entry printer is available with up to five decades print-out.

Using all integrated-circuit logic, the printer accepts inputs in a 1-2-4-8 BCD code. Input data are printed upon receipt of an external print command in the EXTERNAL mode; at the maximum printing rate in the AUTO mode; and when the front-panel push button is pressed in the MANUAL mode. When a line has been printed, a print-completed pulse is generated, indicating the printer is ready for another input. Price $695. AIC Instruments, Houston, Texas.

Circle No. 202 on Inquiry Card

LOW PROFILE RELAY

DPDT relay designed especially for the high-density packaging and severe environmental requirements of military logic circuits has a profile height of only 0.25″. Other dimensions are 0.4″ x 0.5″, and terminals are spaced 0.1″.

The DPDT contacts are rated (for 28 VDC) at 2.0 amps resistive, 0.2 amp inductive. Operate and release times are 6 milliseconds or less. Allied Control, New York, N. Y.

Circle No. 203 on Inquiry Card

MINIATURE RESISTOR

A molded precision metal film resistor, 0.065″ diameter by 0.150″ long, featuring rugged end cap construction, is now available for miniature circuit assembly applications.

Designated ACI Type EE-1/20, the resistor conforms in all respects to Type RN50 of MIL-R-10509F and RNR50 of MIL-R-55182C. Range coverage is from 10 ohms to 110K, and higher values to 500K are available at reduced specifications. Wattage rating is 1/20 at 125°C. Leads may be specified as tinned copper, goldflashed dumet, or bare nickel "A." Temperature coefficients of 0 ± 25 ppm/°C are available, as well as special tracking requirements to 0 ± 3 ppm/°C over specified temperature spans.

Prices range from $0.19 to $2.07. American Components, Conshohocken, Pennsylvania.

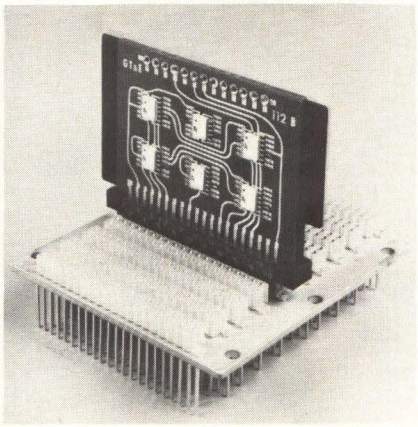
Circle No. 231 on Inquiry Card

TTL HEX INVERTER

A TTL hex inverter with high-speed operation, high-output drive capability, and a compatibility with the DTL and LPDTL families has been designed primarily for high-speed inverter applications in military, computer and industrial systems, but can be also used as a line driver. A high-capacitive drive is achieved by means of an active pull-up in the hex inverter's output.

Designated TTμL 9016, the device features input clamping diodes to prevent ringing. Each of its six gates performs a single inversion operation, making it extremely useful where a number of complementary signals are required simultaneously. The six-gate feature is said to make possible a reduced package count in system assemblies. Fairchild Semiconductor, Mountain View, Calif.

Circle No. 229 on Inquiry Card



2-SIDED PC MODULES

A series of double-sided, multi-layer printed circuit modules, designed to accommodate high-speed logic functions utilizing integrated circuit assemblies, also can accommodate discrete components and film-hybrid microcircuits. The circuit modules are available in 78 basic circuit configurations. Primary application of the modules will be in computer logic control systems, telemetered data reduction, and data processing systems.

Versatility Stressed

The modules are 1.8 inches high by 2.84 inches wide by .281 inches deep. They utilize a standard 40-pin NAFI connector.

The printed circuit board is of multi-layer construction containing two printed circuit cards with a backbone of black anodized aluminum for heat conduction and card pulling. Each card consists of a double-sided etched signal panel with two signal layers interconnected as needed by plated through holes, and a double-sided power/ground panel. Sylvania, New York, N. Y.

Circle No. 230 on Inquiry Card

1½¢/BIT MASS MEMORY

A new mass memory, Model CM-300, available in storage capacities up to 32 million bits (1,024,000 words of 32 bits), has a cycle time of less than 4 microseconds. Dependent upon quantity and capacity, the price will be as low as 1½ cents per bit.

The Model CM-300 is said to offer true random access at speeds and capacities not previously available in static storage devices.

A 2 wire 2½D magnetics organization and field proven circuitry are utilized in the mass memory to assure high reliability and wide operating margins. All circuits in the system have been subjected to verifiable worst case design. Lockheed Electronics, Los Angeles, California.

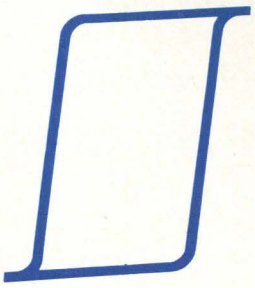
Circle No. 228 on Inquiry Card

PRECISION FILM CAPACITORS

Ceramic-cased capacitors, type PK and PKH, are constructed with a dual paper and film dielectric that is oil impregnated and filled to offer outstanding characteristics in reliability and performance. Extended foil electrodes are employed to offer the lowest possible inductance and dissipation factor enabling these capacitors to be used safely in pulse forming networks and energy storage applications.

The capacitor roll assembly is rigidly secured in a ceramic case and hermetically sealed. Utilization of a ceramic case provides long leakage paths which enable these capacitors to be used in humid or dust laden atmosphere. The inherent strength of the ceramic case allows the units to be potted or subjected to high pressure environments. Del Electronics Corp., Mt. Vernon, N. Y.

Circle No. 222 on Inquiry Card



- ***Customer Satisfaction***
- ***Reliability***
- ***Speed***

That's what Datacraft Corporation engineers into each memory, whether it's an off-the-shelf 512 x 8 unit or a custom designed 65536 x 32 system.

The model DC-31 for example, is a high speed, linear select, coincident-current, magnetic core memory especially suited for systems requiring small high speed units. It comes with a full complement of field proven options that enable the customer to select a custom system at minimum expense.

The basic DC-31 features include: less than one microsecond full cycle time; 450 nanosecond access time; capacities up to 1024 x 12 in one bit per word increments; 30 days delivery. Prices start at $1210.

For detailed specifications on the DC-31 and information on other models, call (305) 565-9441 now, or write

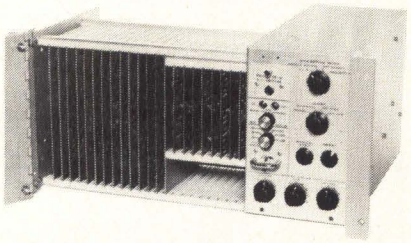
Datacraft Corporation,
776 N.E. 40th Court,
Fort Lauderdale, Florida 33307.

DATACRAFT CORPORATION

CIRCLE NO. 41 ON INQUIRY CARD

Need to sample low-level transducers?

cut your per-channel cost with IEC's new MX 500 Series Low Level Analog Multiplexer.



The MX 500 benefits both designers and users of Data Acquisition Systems:

- Eliminates data amplifiers in each channel
- Reduces system costs sharply
- Simplifies system interface
- Reduces system size, power, and cooling
- Increases system reliability
- Simplifies system checkout and operation
- Reduces system maintenance and spares

Outstanding features include:

- ±5 mv to ±500 mv full scale inputs (±10 v full scale output)
- Up to 50 kHz sample rate
- Easily expandable up to 1000 differential, guarded channels
- 120 db common mode rejection
- Sequential or random address channel selection
- Automatic and programmable gain selection
- Overload protected
- Solid state–FET switches–IC logic
- Available with or without AD converter

The new MX 500 interfaces easily with any Data Acquisition System. Need more information on how you can use the MX 500 in your system? Simply call or write, today.

IEC

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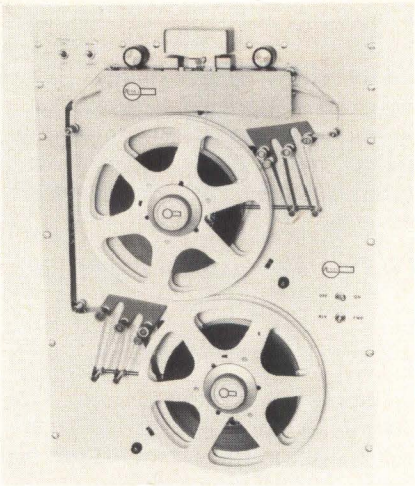
CIRCLE NO. 42 ON INQUIRY CARD



PUNCHED TAPE READER AND SPOOLER

Ultra high-speed, photoelectric punched-tape reader, model RR-1002, and matching tape spooler, model RS-1000, operate at a reading speed of 1000 characters per second and rewind or search at 2000 characters per second.

The units are available in unidirectional and bidirectional models with 10½ inch diameter reels having tape storage capacities of up to 2040 feet. The reader is available with several output and drive modes including integrated circuit compatible modes.

Prices for the units total from $3,610.00 to $3,780.00 depending upon configuration. Delivery is eight (8) weeks after receipt of order. Remex Electronics, Hawthorne, Calif.

Circle No. 217 on Inquiry Card

RUN-TIME METER

Model RTM-1 is a non-reset miniature running time meter 7/8" in diameter with a 4-digit readout in less than a 1" square. Height of digits is 1/8". Synchronous motor is 3/4" diameter by less than 1" long. Power consumption is 2 watts. Solder terminal lugs are provided with an insulated barrier. An adjustable mounting flange is included to allow for any thickness of panel from 1/64" to 2".

The standard voltage is 110 Volts 60 Hertz; other voltages and frequencies are available on order. Present delivery on quantities up to 1,000 pieces is 2 to 3 weeks. Middlebury Mfg., Inc., Waterbury, Conn.

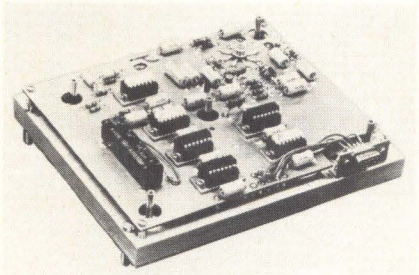
Circle No. 221 on Inquiry Card

HI-V FAST SWITCHING DIODES

As many as six individual, matched silicon junctions are stacked and packaged in a micro epoxy form for switching applications up to 6,000 working volts in the Micro-Codistor II line of diodes. It is claimed that switching speeds range as low as 50 nanseconds for conditions of 10 milliamps, 100 ohms. Applications of these diodes can be extended into the megaHertz range.

Measuring only 0.075" in diameter and 0.125" long, these diodes are available in five separate models ranging from working inverse voltage (WIV) ratings of 2000 volts to 6000 volts in 1000 volt steps. Maximum reverse leakage at working voltage is 1.0 μA. Computer Diode, Fair Lawn, N. J.

Circle No. 215 on Inquiry Card



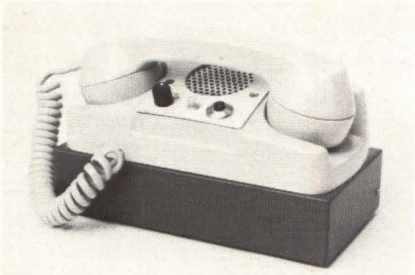
DELAY-LINE PRODUCTS

High storage and bit rate memory module series, available from Andersen Laboratories in Bloomfield, Connecticut, are suitable for a broad range of applications in computer terminal equipment of all types.

A glass delay line is used for high-density storage, compactness and high reliability. The memory measures 7.0 x 5.82 x 1.56 in., and includes both input and output electronics. Delay time and data rate are factory adjustable over a wide range from 10 to 300 microseconds and 2 to 10 MHz.

As extensive use is made of integrated circuitry, power consumption is low. Only an NRZ input is required, and both NRZ and NRZ outputs will drive up to 30 logic units. The memories may be stacked readily to achieve increased delay lengths and storage. Weight is less than 32 ounces. Andersen Laboratories, Bloomfield, Conn.

Circle No. 227 on Inquiry Card



VOICE/DATA ACCESSORY

Milgo Electronic Corporation will introduce a new accessory to their line of narrow-band data sets at the Spring Joint Computer Conference, April 30-May 2, in Atlantic City.

The Model 10 Voice Adapter allows users of Milgo's Modem 4400/24PB data sets to transmit voice or Teletype simultaneously with 2400 bps data over a single unconditioned telephone line.

The telephone-size unit plugs directly into a Modem 4400/24PB data set and requires no outside power. It allows selection of voice/data, teletype/data, and full voice and has its own ringing circuit which does not interfere with the high-speed data. Milgo Electronic Corp., Miami, Fla.

Circle No. 205 on Inquiry Card

MOS BREADBOARD GATE

A MOS 3-input gate has been announced for use in breadboarding complex custom integrated circuit subsystems, as a vehicle in gaining familiarity with MOS integrated circuit techniques, or as a test device in life test programs.

The new product is the 3102, a monolithic P-channel enhancement mode device that performs three basic logic functions: NAND, NOR and gated NAND. This logic versatility results from the bilateral nature of an MOS device.

Using one or more 3102 packages, an enginer can build full adders, RS flip-flops, RST flip-flops, type flip-flops, inverting and noninverting buffers, exclusive NOR and OR gates, monostable multivibrators, free-running multivibrators, and many more static and dynamic MOS functions.

The gate utilizes Planar II, a patented process, for superior stability and provides input protection on all gate inputs. It operates over a temperature range of −55°C to + 85°C. 1000-hour operating life test data is available on this device. $6.00 each for orders of 1-99 and $4.00 each for orders of 100-999. Fairchild Semiconductor, Mountain View, Calif.

Circle No. 218 on Inquiry Card

PERFORATING TAPES

A new extra-thin extra-length cross-linked cellulose perforating tape that fits nearly twice as much tape in the same space as conventional paper tapes is said to permit twice as much unattended machine time in communication, computer, numerical control and data processing applications without changing rolls, and to provide a saving in handling and storage space. It comes in 1,800 and 5,500 foot lengths, three standard widths: 1″, 7/8″ and 11/16″, and four colors: buff, red, green and blue. The core is 2″ I.D. Robins Industries, Flushing, N. Y.

Circle No. 206 on Inquiry Card

MODULAR POWER SUPPLY

Power supply series FR features remote sensing and provision for remote programming in a wide range module. Voltage ranges are 0 to 15 and 0 to 30 volts DC with current capabilities of 0.5 or 1.0 Ampere. The units are designed for general applications where ripple and regulation requirements are stringent. The producer claims these laboratory quality modules may be locked at any voltage and are protected against short circuits and overloads. Prices begin at $75 each in small quantity. Elasco, Boston, Mass.

Circle No. 209 on Inquiry Card

VARIABLE OSCILLATOR

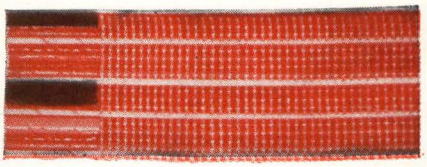
Model 4200, a 10 Hz to 10 MHz, all solid-state oscillator with calibrated pushbutton/vernier output attenuator, has an open circuit output of 10 volts, and delivers 1/2-watt power (5 volts across 50 ohms) with less than 0.1% distortion. The flat frequency response (0.025 db) eliminates the need to reset amplitude when making response measurements. Krohn-Hite, Cambridge, Mass.

Circle No. 224 on Inquiry Card

IT'S FLAT

IT'S FLEXIBLE

IT'S VERSATILE



IT'S TEMPBRAID

...the solution to packaging problems.

HITEMP BRAIDED RIBBON CABLE IS:

- Flat — as the insulated conductor
- Flexible — much more flexible than bonded and laminated cables
- Saves Space — up to 60% over round cables
- Light Weight — no jackets or fillers
- Easily Terminated — uses commercially available connectors
- Versatile — any combination of insulated conductors — any width

For more information and literature, contact:

1200 Shames Drive
Westbury, New York 11590
Tel: 516-333-4600

Hitemp DIVISION
Simplex
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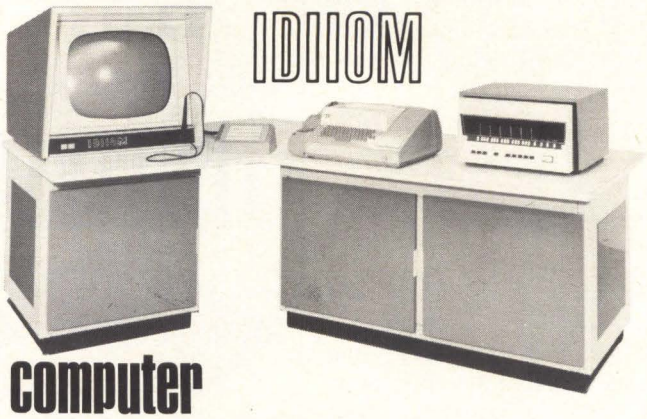


computer

ENGINEERS & AIDES INTERESTED IN GROWTH

Here's a chance to be a big fish in a small pond that's getting big rapidly.

Information Displays Inc. has facilitated rapid man-computer dialog with its new **IDIIOM** multi-media, freestanding terminal.

Now we need Engineers and Aides to take on broad-scale responsibility for new projects. Men who want to see the results of their work; men who want more than "just a job."

Growth Potential? Well, we're still small enough to call our president "Ken" but we've doubled our staff in six months. And here's a point to consider: almost everyone at IDI has invested in the company's stock.

Salaries: good. Location: northern Westchester — nice country, outstanding schools. Contact: Mr. Henrichs.

INFORMATION DISPLAYS INC.
333 N. Bedford Rd., Mt. Kisco, N. Y. 10549 • (914) 666-2936

CIRCLE NO. 46 ON INQUIRY CARD

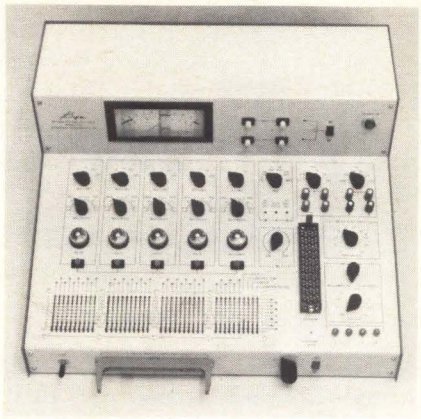
NEW! low cost direct viewing filament readout

A major advance in production techniques is responsible for this low cost, micro-miniature numeric readout — Model M6-30. ☐ High in reliability, low on power, small in size and long on life, it withstands extreme shock and vibration conditions, uses only 8ma/segment at 3 volts, is only 1/2" high x 5/16" wide x 3/16" deep with a character height of 5/16" and lasts 100,000 hours/segment. ☐ By viewing the filament directly, excellent readability is provided even in direct sunlight. It can be plugged into a connector or wired directly into printed circuit logic. ☐ Commercial unit, in large quantities, only $12.95.

SEE A DEMONSTRATION AT THE IEEE EXHIBITION, MARCH 18-21, BOOTHS 4J26-4J28

Pinlites Inc. 1275 Bloomfield Ave., Fairfield, N. J. 07006
201-226-7724

CIRCLE NO. 55 ON INQUIRY CARD



INTEGRATED CIRCUIT ANALYZER

An integrated circuit analyzer, offering a high degree of flexibility for circuit testing, provides two test modes: manual operational via the 10 x 40 cross-point matrix or as a rapid change; and programmed functional tester via the pre-wired program patch plug. All DC parameters of micrologic circuits and most microlinear circuits may be tested.

Designated model 715, the analyzer tests linear or digital circuits in 30 seconds. Price: $1695. Microdyne Instruments, Waltham, Mass.

Circle No. 216 on Inquiry Card

15-BIT SYNCHRO/RESOLVER TO DIGITAL CONVERTER

High-reliability, all-electronic 15-bit synchro/resolver to digital converter with an accuracy of 40 seconds of arc at high tracking speeds is suitable for applications in servo system testing, machine tool readout, antenna position indicators or any other application where a precise indication of angle is required.

The new converter accepts either 3 wire synchro or 4 wire resolver inputs at 11.8 or 90 volts and converts to a 15 bit parallel binary output without the use of rotating components. Models are available for 60 cps or 400 cps operation. Both a visual display and an electric output are provided. Standard

logic level outputs are compatible with DTL or TTL microcircuits. Astrosystems, New Hyde Park, N.Y.

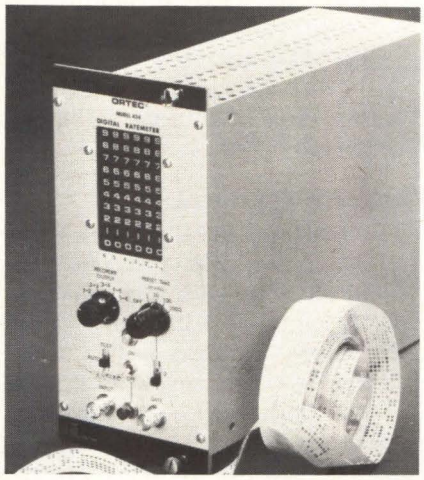
Circle No. 220 on Inquiry Card

FET VOLTOHMETER

Compact voltohmeter, designed with an advanced field-effect transistor circuit, measures voltages as low as one-tenth of a volt d-c full scale and one/one-hundredth of a volt a-c full scale. Claimed to be more sensitive than a VTVM, the model 870 Millivolt Commander as it is called, provides a full-scale indication of low voltage with a sensitivity range from 100 mv full scale to 1000 v full scale in nine increments.

Also, the new voltohmeter measures a-c voltages from one/one-hundredth of a volt full scale to 300 v full scale in ten steps. Most voltmeters are sensitive down to only 3 v a-c. The model 870 makes possible a-c voltage measurements where before the electronic technician had to use an oscilloscope. Amphenol Corp., Broadview, Ill.

Circle No. 219 on Inquiry Card



BUFFERED DIGITAL RATEMETER

Modular buffered scaler/timer that performs as a digital ratemeter includes a self-contained six-decade 2-MHz scaler, timing system, buffer memory, and serial printout capability and analog output. Data are transferred to the buffer memory for recording on computer-compatible punched tape and/or a printer while the scaler begins collecting new data. Dead time between data collecting intervals is less than 50 usec in continuous operation. Ortec, Oak Ridge, Tenn.

Circle No. 210 on Inquiry Card

be sure to see
DIALIGHT READOUTS
before you specify!
WHY?

- **Operate on:**
  - **6V AC-DC**
  - **10V AC-DC**
  - **14-16V AC-DC**
  - **24-28V AC-DC**
  - **150-160V DC**
  - **110-125V AC**
- **Bright always-easy-to-read numerals.**
- **Non-glare viewing windows with choice of colors**
- **Available with RFI-EMI suppression screen.**
- **Universal BCD to 7 line translator driver**
- **10 line to 7 line converters for decimal input**
- **Custom translators on application.**

Because **we can prove to you that they are superior** . . . that they will improve the readout qualities needed in your application . . . and will enhance the sale of your equipment.

What's more . . . Dialco readouts cost as little as

$3.99

each (less lamps)
in 1000 lot quantities

How can we prove this superiority to you? **See the readouts for yourself.** We're confident that's all the proof you'll need. Let us demonstrate the product in your office, at your convenience. To do so, circle Reader #47.

For current catalog with 9 data sheets, circle reader number noted below.

DIALCO®

Foremost Manufacturer of Indicator Lights

DIALIGHT CORPORATION

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CIRCLE NO. 48 ON INQUIRY CARD

SNAP-ACTION SWITCHES

Snap-action, toggle-rocker push-button and special-use switches feature 3 to 30 amp capacity range, and a wide choice of actuator types, circuitry, and operational characteristics.

Called the 2600 series, the 20-ampere snap-action switches provide high-precision in a medium-priced switch with differential travel loss less than 0.005". The 4600 Series, 15 amp. miniature snap-action switches are compact without sacrificing switch capacity or life. McGill Manufacturing, Valparaiso, Ind.

Circle No. 226 on Inquiry Card

DECODER WITH MSI COMPLEXITY

A 28-gate circuit which features four inputs in standard 8421 binary coded decimal code and provides active high outputs for a seven-segment numerical display has been added to Fairchild Semiconductor's family of medium scale integrated products (MSI)

The 9307 decoder, fourth in the fast-growing complexity family, has capabilities for display intensity modulation, ripple blanking and lamp testing. Like other MSI products, the 9307 interfaces with all CCSL elements (Compatible Current Sinking Logic) and can be coupled directly to CCSL logic.

The 9307 is ideal for driving numerical displays involving high-current, high-voltage incandescent lamps, neon and electroluminescent devices, or cathode ray tubes in military, computer or industrial systems.

Fairchild's device will automatically suppress leading and/or trailing edge zeroes, thus displaying only the most significant digits. A low-input lamp testing facility provides the advantage of being able to check the legitimate operation of the display segments, including the lamps.

The 9307 chip is hermetically sealed in all-ceramic, 16-pin Dual In-Line package, with the 16 leads optimally arranged for printed circuit layouts. Maximum package size is 0.200 by 0.375 by 0.785 inches. Fairchild Semiconductor, Mountain View, Cal.

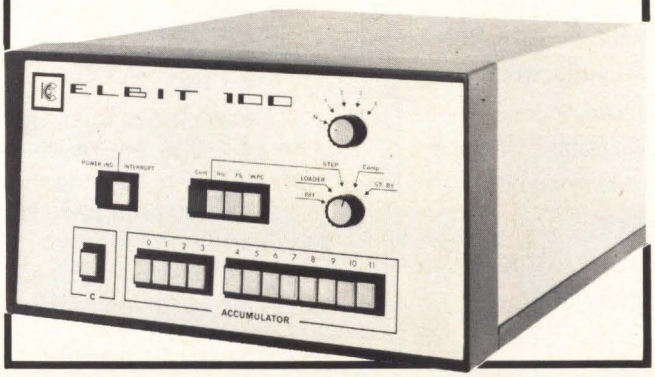
Circle No. 250 on Inquiry Card

ELBIT 100

FOR PEOPLE WHO THOUGHT THEY COULDN'T AFFORD A DIGITAL COMPUTER

A $4900 DIGITAL COMPUTER

* 2 MICROSECOND CORE STORE.
* 400 NANOSECOND READ ONLY STORE.
* 6 μ SEC FULL WORD ADD TIME.
* MICROPROGRAMMABLE.
* UP TO 256 I/O DEVICES.
* ALL DTL INTEGRATED CIRCUIT CONSTRUCTION.



ELBIT COMPUTERS LTD.

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CIRCLE NO. 49 ON INQUIRY CARD

NEW N/C SYSTEM

Designed primarily for N/C control on lathes and milling machines, a new machine control system can easily be fitted to new or used equipment. It utilizes punched tape inputs and electro-hydraulic servo controls to direct a table in two axes with ±° .0005" accuracy. Table speeds of 300"/min. and greater are attained with minimum hydraulic power requirements. A special shifting feature on the hydraulic motor drive provides rapid traverse at 5 to 10 times maximum feed rates up to 1000"/min. Available options for miller applications include a "Z" axis drive and/or automatic spindle control.

An advantage claimed by the manufacturer is that its system computes actual table or tool position, therefore no compensation for wear in aging machine tools is necessary. Performance can be upgraded without the added cost of rebuilding the tool.

The electronics section utilizes integrated circuits for long-term reliability and economies. A unique feature to insure minimum downtime is a kit of printed circuit cards duplicating those in the system. In the event of electronic malfunction, the machine operator (or other non-technical personnel) simply replaces cards with like units from the kit until a "GO" condition is restored.

Circle No. 256 on Inquiry Card

DISPLAY TERMINAL

The DATA-SCREEN Display Terminal, a new input/output CRT display system, with a character capacity of up to 512 stroke-written characters, combines a CRT screen with a display system permitting display of both fixed and variable information. The display terminal can be interfaced with most computer systems and standard communication links; it accepts and transmits codes such as ASCII, IBM, BCD, or EBCDIC. Integral core refresher memory permits flicker-free image projection. The complete unit, which measures 20" x 13¼" x 25", fits on a desk top or mounts in a 19-inch rack panel. Optional electronic keyboard console of the terminal is closely similar to a conventional electric typewriter making it easy to operate. Transistor Electronics Corp., Minneapolis, Minn.

Circle No. 258 on Inquiry Card

LOW-COST INCREMENTAL TAPE RECORDER

Compact, write only, magnetic incremental tape recorder, for recording data in industry-compatible format for immediate data processing, can be connected to typewriters, keyboards, adding machines, accounting machines, cash registers, etc. Recorded data can be computer-processed without intermediate conversion. Applications include data logging, data transmission, and office machine output.

This new recorder, complete with drive/record electronics, sells for $1400 in production quantities, said to be substantially below comparative industry prices; and offers — for the first time — IBM compatible magnetic tape recording at paper tape equipment prices.

The ME-4210 records data in one-character increments on magnetic tape. Asynchronous data transfers from 0 to 60 characters-per-second can be accepted. Recording accuracy is better than 1 in 10^7. Data is recorded in NRZ-I format on ½", 7-channel tape at a packing density of 200 bpi. The 5½" diameter reels hold 140' of tape.

The ME-4210 automatically generates inter-record and file gaps, upon command. Parity generation and immediate check-read-after-write are available.

Potter Instrument Company, Inc., Plainview, New York.

Circle No. 251 on Inquiry Card

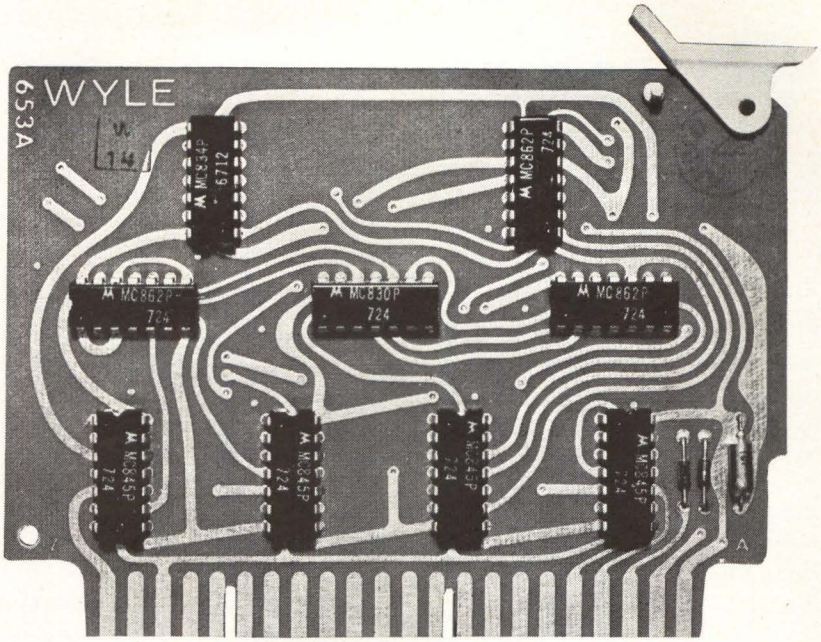
POWER SOURCE FOR OP AMPS

A regulated power source for operational amplifiers and comparators complete with transformer, in a small package and at a reasonable price has been designed on the basis of a thorough survey of popular op amps, both discrete and monolithic types. The regulation and ripple of the new power source are a factor of two better than the amplifiers require for negligible influence on the amplifiers' voltage and current noise and drifts. Outputs are completely protected against overloads and short circuits.

Available with or without mounting ears, the power source can be mounted directly on a printed circuit card. Dimensions are 2 inches square by 1¾ inches high.

The 2330 power source is priced at $49.50 each in 1 - 9 quantities and is available from stock to 30 days. Solatron Enterprises, Venice, California.

Circle No. 255 on Inquiry Card



WYLE LOGIC MODULES

FAST DELIVERY

TECHNICAL ASSISTANCE

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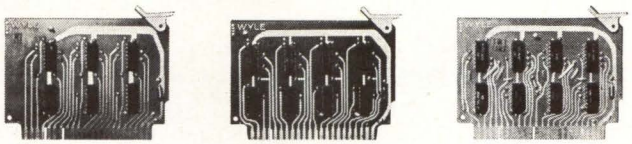
BROAD SELECTION

TEN-YEAR WARRANTY

STATE-OF-THE-ART DESIGN



The above are some of the subheads in the Wyle Integrated Circuit Logic Modules short-form catalog. They are seven of the twelve reasons Wyle logic cards may be your best buy. If you want to discuss the other five reasons (or get more detail on the Big Seven), drop us a line on your company letterhead, and we'll send you the catalog. Or better still, call Don Tothe, our product manager, and let him fill you in on what Wyle can contribute specifically to your system. Systems Division, Wyle Laboratories, 128 Maryland Street, El Segundo, California. (213) 678-4251.

WYLE

CIRCLE NO. 50 ON INQUIRY CARD

LITERATURE

Digital Readouts

Twelve-page booklet discusses three major developments said to have significantly improved the total performance of illuminated bar readout: 1. The molecular bonded filter which provides greater contrast enhancement. 2. The 16-segment digit configuration, for greater display capacity, and 3. low-power incandescent lamps which reduce heat problems and which can be driven directly from IC circuits. The booklet also contains a description of the system characteristics of the manufacturers readouts along with a discussion of pertinent reliability considerations. Tung-Sol Div., Wagner Electric Corp., Newark, New Jersey.

Circle No. 305 on Inquiry Card

Overseas Telegraph Equipment

Equipment for international telegraphic communications is described in a 16-page catalog providing communications managers and businessmen who have overseas correspondents with an illustrated, up-to-date listing of equipment available for use on ITT circuits for telegram, telex, high-speed data and private leased channels. ITT World Communications, New York, N. Y.

Circle No. 306 on Inquiry Card

Thin-Film Microcircuits

Custom microcircuits, which combine Nichrome thin-film passive resistor networks with silicon integrated circuits and other semiconductor dice, are described in a new brochure containing a summary of features, performance data, packaging information and check list of information required for translating your custom design into a thin-film microcircuit. Halex, Inc., El Segundo, Calif.

Circle No. 307 on Inquiry Card

New Multiplier Catalog

Six-page catalog lists a line of solid state analog multipliers, covering a range from DC to 4 Megahertz in four models.

The flat-pack units all operate in four quadrants, do not require external amplifiers and are compatible with operational amplifier circuitry.

Applications data, connection diagrams and mechanical drawings are included in the literature. Transmagnetics, Inc., Flushing, New York.

Circle No. 308 on Inquiry Card

Business Communication System

Illustrated catalog describes data communication systems used to move data over ordinary telephone lines at up to 1200 words per minute. Both one and two way communication systems using perforated and magnetic tape, and punched card input/output are covered. Tally Corporation, Seattle, Washington.

Circle No. 309 on Inquiry Card

Ultra-Min Indicator Lights

A complete line of ultra-miniature indicator lights, for rear mounting in $\frac{3}{8}$" clearance hole is presented in Catalog L-203.

The light source in this series is a T-2 type neon lamp designated as NE-2H for high brightness and the NE-2E for standard brightness operation. The former is used on AC circuits of 110-125 volts, the latter on DC circuits of 105-125 volts. With appropriate current-limiting resistor, approximate lamp life is 25,000 hours.

Also described is the 915 Series. This ultra-miniature series has three terminals. A pair of terminals, common to the hot side of the power supply, permit extending the circuit by jumpers to all lights in multiple arrangements.

Specifications, drawings, lamp data and ordering information is included to aid in the selection of the desired indicator lights. Dialight Corporation, Brooklyn, New York.

Circle No. 310 on Inquiry Card

Power Supply Catalog

Eight-page catalog describes all power supplies manufactured by the firm including the new CS 7-3, CS 18-2, and CS 30-1 Card Supplies. The line will service a total of 79 inductance low-voltage DC requirements. The new catalog carries both price and delivery information. Valor Instruments, Inc., Gardena, California.

Circle No. 300 on Inquiry Card

Computer Measuring System

A brochure recently released describes a measuring system said to provide all the versatility and flexibility of a general-purpose digital computer. The system, equipped with a random access magnetic core memory unit, has the capability of calculating dimensional deviations, generation of N/C tapes, pattern duplication, "accept-reject" determination, alignment correction and scaling with all operations performed automatically.

Output of the computer is simultaneously printed and punched into a tape by an ASR-33 teletypewriter. The printed copy becomes a permanent record of the complete operation. The punched tape copy is available for future processing, such as statistical analysis or further evaluation. Output of the computer can be in any N/C or computer format desired — on punched tape or magnetic tape — and different programs can be run on the same system. Potter Instrument, Plainview, N. Y.

Circle No. 301 on Inquiry Card

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Los Angeles 57, California
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Ceramic Packages

Eight-page, three-color booklet, covering a line of high-performance ceramic flat packs for packaging microcircuits presents the material, mechanical, electrical and environmental specifications of the packages. Titled "Microcircuits Packages," the booklet also contains a description of the package structure which employs a ceramic-to-glass-to-metal seal and discusses its advantages over the conventional sintering technique, higher reliability and simplicity of modification. Tung-Sol Div., Wagner Electric Corp., Newark, N. J.

Circle No. 302 on Inquiry Card

Ultra-High Surge 10-Watt Stud Zener

Two-page data sheet describes new 350 Watt surge power, 10 Watt continuous power stud-mounted zener diodes — said to be the highest surge rating in the industry. Included are all the important zener parameters as well as information not often available to the designer, such as leakage current and temperature coefficient. Graphs are provided on surge duration vs surge power, zener impedance vs zener current, as well as on de-rating. Included also are outline drawings and application and ordering information. Unitrode Corporation, Watertown, Mass.

Circle No. 303 on Inquiry Card

Magnetic Tape Rehabilitation

A technically updated "Systematic Guide to Magnetic Tape Rehabilitation" encompasses 6 basic areas relating to the use and maintenance of magnetic tape. Among the areas covered are causes for tape failure, rehabilitation concepts and cost concepts.

A section on techniques and procedures describes processes such as tape cleaning, testing, the hypercritical testing concept, certification and repair, 7 to 9 channel tape conversion and management reporting. A section is devoted to helping the data processing executive choose the proper equipment to suit his operation. Cybertonics, Waltham, Mass.

Circle No. 304 on Inquiry Card

SLASH DIGITAL DATA HANDLING COSTS!

DIGI-STORE® DS-2

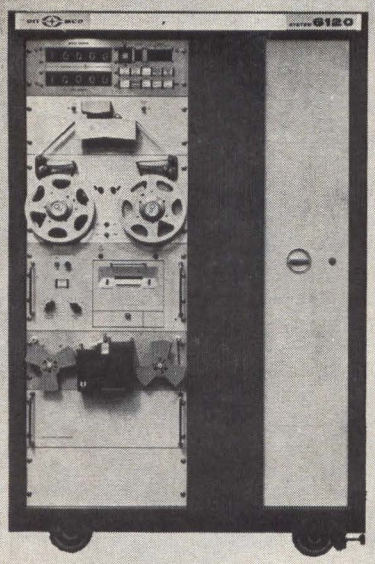
DIGI-STORE® DS-2 is a **bidirectional, incremental** magnetic tape unit offering these advantages . . .

- Speeds up to 333 characters per second.
- Operates in either read or write mode—can replace both tape punch and reader.
- High reliability — all-solid-state circuitry — only one moving part during operation.
- Handles any code up to 8 levels.
- Eight times more packing density than paper tape — less tape bulk—no chad.
- Less tape handling cost — DS-2 tape can be reused thousands of times.
- Compatible with conventional paper tape data handling systems.
- Interface logic available to suit individual requirements.
- Two DS-2 units — one operating in the read mode, the other in write — team up to make the Wiltek Buffer-Store for use whenever a device of variable data storage capability of 1000 ch/ft. is needed.

WRITE FOR COMPLETE DS-2 DATA

WILTEK, INC.
formerly Trak Electronics Co., Inc.
59 DANBURY ROAD • WILTON, CONN.

CIRCLE NO. 12 ON INQUIRY CARD



FASTEST WIRING SYSTEM ANALYZER IN THE WEST AND EAST AND NORTH AND SOUTH.

The DIT-MCO System 6120 walks tall in the world of wiring system analyzers. It's a tough, versatile and highly adaptable testing unit that's ready, willing and able to meet today's demand for speed, accuracy and flexibility. Works on the latest fully automatic taped program and printout concept.

INSULATION TEST CAPACITY: 2010 PER MINUTE!

CONTINUITY TEST CAPACITY: 2963 PER MINUTE!

The DIT-MCO System 6120 has been thoroughly lab and field tested.

Switching Console contains terminal selector and high speed 500-termination Reed relay switching modules that give you a total system capacity of up to 50,000 terminations. Save time, save manpower, save dollars — and — improve both the testing function and the tested product with the DIT-MCO System 6120.

Write for Detailed Specs and Full Information.

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CIRCLE NO. 51 ON INQUIRY CARD

ADVERTISERS' INDEX

ADAR ASSOCIATES, INC.	58
AMP, INC.	44, 45
BURROUGHS CORPORATION	Cover 3
CAMBRIDGE THERMIONTIC CORPORATION	34
CHALCO ENGINEERING CORPORATION	22, 23
COMPUTER AUTOMATION, INC.	27
CONTEMPORARY ELECTRONICS	25
CONTROL LOGIC, INC.	1
DATA TECHNOLOGY	2
DATACRAFT CORPORATION	79
DIALIGHT CORPORATION	83
DIGI-DATA CORP.	46
DIGITAL EQUIPMENT CORP.	10, 23
DIGITRAN CO.	35
DT-MCO INTERNATIONAL	88
ELBIT COMPUTERS LTD.	84
ELECTRONICS MEMORIES	18. 77
ETCHIT, INC.	66
FAIRCHILD SEMICODUCTOR	8, 9, 12, 13
FERRANTI-PACKARD ELECTRIC LIMITED	35
FERROXCUBE CORP.	15
GENISCO TECHNOLOGY CORP. Components Div.	37
HEWLETT-PACKARD	5
HITEMP WIRES COMPANY	81
IBM	19
INFORMATION DISFLAYS, INC.	82
INTERDATA	Cover 2
INTERSTATE ELECTRONICS CORP. (Data Products)	80
INVAC CORP.	26
JOSEPH KAYE & COMPANY	66
LOCKHEED ELECTRONICS	37, 47
MICROSONICS	38
MILGO ELECTRONICS	11
MOTOROLA SEMICONDUCTOR PRODUCTS, INC.	17
NATIONAL CASH REGISTER CO	7
PATWIN ELECTRONICS	41
PERIPHERAL EQUIPMENT CORP.	16
PINLIGHTS, INC.	82
RAYTHEON Computer Div.	6
RAYTHEON COMPUTER	41
RCA ELECTRONIC COMPONENTS & DEVICES	14
SCIENTIFIC DATA SYSTEMS	21
TALLY CORP.	Cover 4
TEXAS INSTRUMENTS, INC.	4
TRANSISTOR ELECTRONICS CORP.	40
VARIAN DATA MACHINES	53, 59, 67
VARO, INC.	78
WILTEK, INC.	37
WYLE LABBORATORIES SYSTEMS DIVISION	85

4 breakthroughs: new NIXIE® tube

size

.530" dia. x 1.5" for IC compatibility — largest numeral height provides best readability.

anode strobing

new design permits all like-numerals to be driven in parallel for time sharing operation with improved brightness.

pin spacer

simplifies both PC board layout and tube insertion.

price

in quantities of 1,000 — only **$3.95** each.

ACTUAL SIZE

This new tube, type B-5750, has been engineered to achieve all these outstanding breakthroughs in a single design. The new slim-line tube not only has two internal decimal points but also has an "in-line" lead arrangement which is compatible with dual in-line IC's. In addition, the numeral aspect ratio has been designed to provide the optimum in readability and viewing distance.

The movable pin spacer – standoff, which is used to align the tube pins for ease of PC layout and insertion, is part of the tube assembly. The anode strobing/time sharing operation permits substantial reduction in driver costs for many multi-digit display applications. For more information on these and other features contact your nearest Burroughs representative or sales engineer, or write: *Burroughs Corporation, Electronic Components Division, P.O. Box 1226, Department N6, Plainfield, New Jersey 07061 TEL: (201) 757-5000.*

Burroughs

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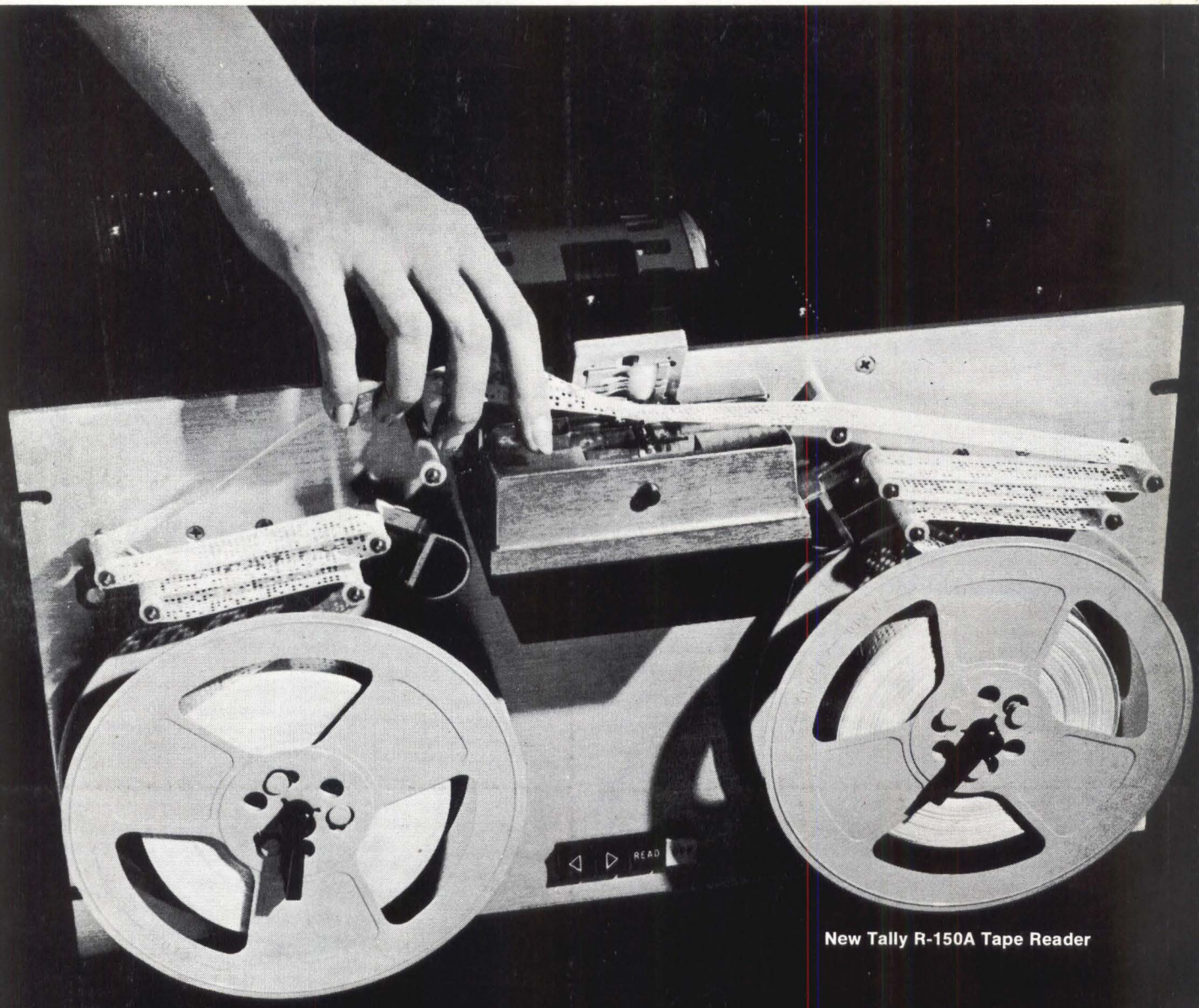
easy to interface...easy to use



New Tally R-150A Tape Reader

☐ Whether you're involved in system design or system usage, the new Tally R-150A Tape Reader will fill the bill. ☐ From the user point of view, the big, new feature is "top load" design for convenient, fast "straight line" tape loading. The "free" tape path and front panel control switches add up to a fast and simple rewind operation. Dependable starwheel sensing from the bottom of the tape allows high speed reading of chadless tape. Bidirectional and asynchronous. the R-150A operates at speeds up to 150 characters per second. Newly developed servo motors for reeling are featured. Reliability of the R-150A has been proven through extensive use in high traffic military communications networks. ☐ Write us on your letterhead and we'll send you interface specs on this oustanding new reader. ☐ Please address Tom Tracy, Tally Corporation, 1310 Mercer Street, Seattle, Washington 98109. Phone: (206) MA 4-0760. In Europe and the U.K., address Tally/APT, Ltd., 6a George Street, Croydon, Surrey, England. Phone: MUN 6838.

TALLY

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