XCELL

Issue 20
First Quarter 1996

THE QUARTERLY JOURNAL FOR XILINX PROGRAMMABLE LOGIC USERS

XILINX®

The Programmable Logic Company℠

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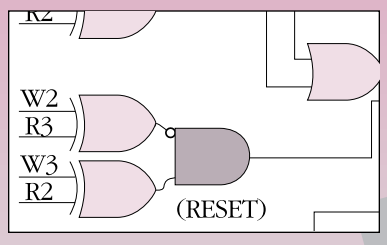

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PLDs, Pins and PCBs

By BRADLY FAWCETT ◆ Editor

Change is inevitable. The best system designers recognize this axiom and incorporate tolerance for change into their schedules, design methodologies, and even the physical realizations of their designs.

Changes can occur during all stages of a product's life cycle. Surveys suggest that as much as 50% of the typical product's development time is spent in the debug/modify/re-implement cycle that occurs after the first prototype is created. Even if the designer is skilled (and lucky) enough to create a working prototype on the first try, the product specification can change in the meantime in response to changing market conditions. In some cases, products that already have been produced and sold for months or even years have been modified to extend the product's life (or, heaven forbid, to correct some previously undetected flaw).

Tolerance of change is one of the prime attractions of programmable logic devices. With PLDs, design changes can be implemented quickly and easily, especially as compared to custom and semicustom IC technology. However, when it comes to tolerating changes, printed circuit boards (PCBs) are more like custom ICs than PLDs. To modify a PCB, new drawings (masks) must be created, and new prototypes must be manufactured, with all the associated expenses and delays.

> *"Tolerance of change is one of the prime attractions of programmable logic devices."*

Thus, to garner the true benefits of the adaptability of programmable logic, programmable logic device architectures should isolate the PCB design from logic changes that occur within the device. As a result, two concepts that should be of primary concern to PLD users are pin-locking and footprint compatibility.

Pin-locking refers to the ability to establish a fixed pin location for all the signals entering and leaving a PLD so that the PCB layout, in turn, can be fixed. Since PCB design and production is often a critical path in product development, most designers would prefer to lock PLD pin locations early in the design cycle. However, with some PLDs, this can be a risky proposition; the chosen pinout may prove to be less than optimal after the implementation of the inevitable design changes, leading to decreased performance, or, in the worse case, a design that cannot be implemented at all due to routing limitations within the PLD. Designers that used the earliest generations of CPLDs and FPGAs may recall that PLD manufacturers routinely warned their users not to begin their PCB design until the PLD design was completed and debugged. This reputation, established in the early days of high-density PLDs — that is, that design changes can be difficult or impossible to implement without changing the device pinout — lingers on today (and deservedly so, for some of our competitors' offerings!).

However, those days have long passed for Xilinx FPGA and CPLD devices.

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GUEST EDITORIAL

In-System Programming and Flash Technology for CPLDs

By NICK KUCHAREWSKI ◆ Vice President, EPLD Division

The latest wave of complex programmable logic devices (CPLDs) has been targeted at an emerging applications area: **In-System Programmability (ISP).** In-system programmable CPLDs allow the user to mount an unprogrammed device on the PC board, then program the device as part of the manufacturing flow. This greatly eases the handling problems associated with fine pitch packages such as the popular plastic quad flat pack (PQFP). But this is far from the only advantage of ISP CPLDs.

Designers can use ISP devices to meet a wide range of needs — from facilitating an integrated design, program, and test environment that allows easy prototyping and system debug, all the way to providing the ability to upgrade a design in the field through CPLD reconfiguration. Of course, manufacturing support must be provided for integrated device programming and board-level test. We refer to supporting this range of user requirements as "supporting the total product life cycle" with in-system programmable CPLDs. As more and more users begin to take full advantage of ISP capabilities during all stages of a product's life, the use of ISP CPLDs will continue to increase. In turn, CPLD manufacturers will need to offer device architectures and development tools that support this full range of user needs in order to remain competitive.

Introducing the FastFLASH™ XC9500™ Family

The XC9500 family is the first CPLD family specifically developed to meet all the typical user requirements for in-system programmability. Xilinx used those requirements to drive the XC9500 development process, including basic device architecture decisions and process technology choices. Let's take a closer look at some of these requirements, and their impact on the CPLD.

"The XC9500 family is the first CPLD family specifically developed to meet all the typical user requirements for in-system programmability."

As mentioned in Brad Fawcett's editorial *(see page 2)*, the flexibility of ISP is enhanced by the ability to fix the chip pinouts ("lock the pins") while continuing to implement design changes. Obviously, the reconfiguration of CPLDs already in the field requires maintaining fixed pinouts to be successful. The approach we have taken to solving this challenge is quite complex and involves several architectural innovations as well as improvements to the optimization and fitter software. The result is the industry's best pin-locking CPLD.

Many users require complete support of industry-standard IEEE 1149.1 JTAG boundary scan test capabilities. By including the in-system programming control within the JTAG controller, both board test and device programming are accomplished with a single interface, and in an integrated environment. This greatly simplifies the manufacturing engineering requirements. The XC9500 is the only CPLD to include support for JTAG instructions such as INTEST and USERCODE. The INTEST instruction is used to test internal logic after device programming on the PC board,

Continued on the next page

XILINX®

Xilinx Enters Into Joint Venture for Foundry Capacity

In a joint venture with United Microelectronics Corporation (UMC) and others, Xilinx has invested a 25% equity stake in a semiconductor manufacturing facility in Hsin Chu City, Taiwan.

Xilinx is one of more than 100 semiconductor companies that use independent silicon "foundries" rather than their own wafer fabrication facilities. Being "fabless" allows the company to focus on what Xilinx does best — the design and marketing of programmable logic devices. Xilinx transcends the scope of traditional customer-supplier relationships by employing its own process experts, who work closely with our foundry partners in the development and implementation of process technology improvements.

The Taiwan facility will ensure a steady and reliable supply of product as the demand for programmable logic devices continues to grow. Starting its two-year ramp up cycle in early 1996, the factory will produce eight-inch wafers using submicron CMOS processes. In the meantime, UMC will provide Xilinx with interim capacity at its other facilities in Taiwan.

Xilinx will maintain its existing foundry partnerships with Seiko Epson, Yamaha, Taiwan Semiconductor Manufacturing Company (TSMC) and IC Works. While the UMC investment marks the first time Xilinx has taken an equity position in a foundry, it is not the first Xilinx investment involving its foundry partners. For example, in early 1994, Xilinx helped fund Seiko Epson's expansion of an IC facility in Sakata, Japan.

"This new venture ensures foundry capacity of leading-edge process technologies to meet the rising demand for FPGAs," noted Xilinx CEO Bernie Vonderschmitt. "This agreement, combined with our other foundry partnerships, favorably positions the company to meet customer demand to the end of the decade." ◆

GUEST EDITORIAL

Continued from the previous page

while the USERCODE function allows the user to "program in" information such as version numbers, assembly locations, or dates as part of the manufacturing process.

Flash Process Technology

An easy-to-use, integrated design and programming environment allows designers to implement multiple design iterations per day. This can translate into a need to support hundreds, and perhaps thousands, of program-erase cycles. Flash process technology provides this capability, with margin to spare. The Xilinx proprietary FastFLASH Technology is the industry's first 5-volt flash technology developed specifically for CPLD applications. It is an extension of industry-standard flash memory technology, and offers the proven reliability of 10,000 program-erase cycles — a factor of up to 100 times more than competing ISP CPLDs.

The benefits of flash technology extend beyond program-erase endurance. The flash memory cell provides the basic programmable "switch" in the XC9500 CPLDs. The size of the flash memory cell is about 1/3 that of other non-volatile technologies, allowing the implementation of many more "switches" in the same chip area. These added resources lead to improved routability and pin-locking capability.

In-system programmability is an increasingly important requirement for CPLDs. The needs of ISP CPLD users extend beyond easier handling of PQFP packages to more complete support of "the total product life cycle." The architecture, process technology and development tools of the XC9500 FastFLASH family meet these needs, allowing users to take full advantage of the flexibility of ISP technology. ◆

Continued from page 2

Pin-locking is not an issue with Xilinx CPLDs. The XC7300 and XC9500 CPLD families offer the ultimate in pin-locking capability, with 100% connectivity through the CPLD's internal switch matrix. Thus, any I/O pin can be connected to any function block input or output, regardless of utilization levels. Design changes internal to the CPLD will seldom force pinout changes.

While the Xilinx FPGA families cannot provide the same guarantee of full connectivity offered by the Xilinx CPLDs, the latest generations do provide a high degree of flexibility in their I/O connections. All recent Xilinx FPGA architectures, including the XC5200, XC4000E, XC4000EX, XC6200, and XC8100 families, embrace the VersaRing™ concept introduced in the XC5200 family. Simply put, these FPGAs include an extra layer of routing resources along the perimeter of the logic array to increase routing flexibility between the internal array and the I/O blocks. User feedback is confirming that these devices deliver on the promise of allowing last-minute design changes without changes to the I/O pin locations.

Actually, this capability also is present to a large degree in the "older" XC4000 series FPGAs. The popular XC4000 family was the subject of the only independent research study (that I know of) that examined pin-locking in FPGA architectures. As reported at the 3rd Canadian Workshop on Field-Programmable Devices last May, researchers at the University of Toronto implemented sixteen different designs in XC4000 devices. The designs were first routed with no placement constraints, then with "bad" pin constraints (wherein signals that were assigned to adjacent pins in the unconstrained design were now assigned to opposite ends of the device), and, lastly, with a randomly-generated pin placement. In every case, the designs routed to completion, albeit with a slight performance impact; the average signal delay increase was less than 5% for the "bad" constraints and 3% for the random constraints. Significantly, the researchers concluded that "Fixed pin assignment does impact routability significantly, because the amount of routing resources used was increased, but the Xilinx XC4000 series architecture provided sufficient resources to handle the increased demand". Incidentally, a major competitor's FPGA family — the only other device included in the study — did not fare nearly as well; several designs were unroutable with bad or random pin constraints, and the researchers recommended that users of that FPGA "should leave about 20% of the logic elements and I/O pins free to avoid routability problems due to pin constraints."

In conclusion, while "intelligent" placement of I/O pins is still recommended, Xilinx FPGA and CPLD devices are quite tolerant of design changes without forcing the redesign of the PCB layout. This facilitates an early release of the PCB design and eases the debugging process, thereby accelerating time-to-market, and accommodates the inevitable changes that occur throughout a product's total life cycle.

In the next issue, part 2 of this article will examine the benefits of footprint compatibility both within and across Xilinx PLD product families. ◆

"These FPGAs include an extra layer of routing resources along the perimeter of the logic array to increase routing flexibility between the internal array and the I/O blocks. User feedback is confirming that these devices deliver on the promise of allowing last-minute design changes without changes to the I/O pin locations."

Wim Roelandts New Xilinx CEO

New Xilinx CEO Wim Roelandts

In late January, Bernie Vonderschmitt retired as Chief Executive Officer of Xilinx. His successor is Willem "Wim" Roelandts, a 28-year veteran of Hewlett-Packard. Vonderschmitt, 72, who co-founded Xilinx in 1984, remains with the company as chairman of the board of directors, and continues to be active in the business affairs of the company.

Roelandts joined HP in 1967 as a service engineer in his native Belgium and most recently served as a senior vice president in Hewlett-Packard's Computer Systems Organization. He was responsible for all aspects of the computer systems business worldwide, including research and development, manufacturing, marketing and sales.

"Wim Roelandts is a seasoned veteran who possesses the right mix of leadership and management skills to guide Xilinx through its next period of growth," Vonderschmitt stated. "Employees, customers, and shareholders can be confident he is the right man to take the helm at Xilinx." ◆

Xilinx Ireland Earns ISO 9002 Certification

Xilinx Ireland, the new manufacturing facility in Dublin, was awarded ISO 9002 certification in November. The Xilinx manufacturing facility in San Jose, California, obtained ISO 9002 certification last October. The ISO quality standards were developed by the International Organization for Standardization, a Geneva-based organization with representatives from 91 countries.

As noted by Derek Kernan, quality manager at Xilinx Ireland, "The ISO standard is widely-recognized in Europe and is a very good means of measuring the quality of our processes and the extent to which the development of the company is keeping pace with our overall strategy. Acquiring ISO certification has made us look at all our processes and all our customers' requirements and understand what we can do better. For us, it represented a good external measure of the value and quality of our systems."

Xilinx Ireland, the company's first wholly-owned manufacturing facility outside of the United States, produces and distributes component products for Europe and other international markets. More than one million FPGA devices were shipped from Xilinx Ireland within the first six months of operation. The facility will eventually replicate all the activities of the company headquarters in San Jose, with the exception of field sales and marketing.

The first group of Xilinx Ireland's software engineers has returned from training in California and has begun development work in Ireland. More than 80 staff members are now employed in Dublin. ◆

The team of Xilinx Ireland

30-Day Design Cycle With XC8100 FPGA Family

SIXNET®

Design engineers at SIXNET (Clifton Park, NY), a manufacturer of industrial control equipment, faced a daunting challenge: to build a new I/O module (from concept to installation at a customer's site) within eight weeks.

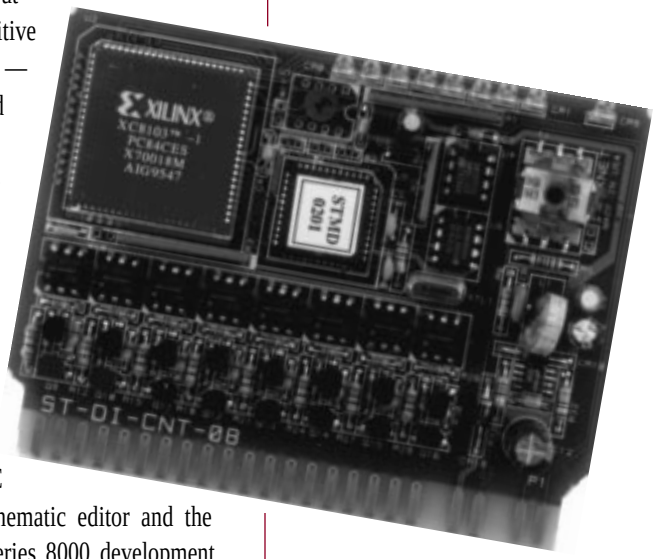
The device, a digital counter board, was required to provide position and/or velocity information for eight independent incoming signals. The digital count signals can be used singly to provide total count or velocity information, or in pairs to provide quadrature-decoded position information. Typical applications are flow metering (where a small turbine pulses at a rate proportional to the flow of a liquid) and position measurement (where a quadrature decoder tracks the motion of precision machinery).

All previous designs at SIXNET had employed 22V10 (or smaller) PLDs, using equation-based design entry as the primary development tool. While time restrictions dictated the use of programmable logic, severe space limitations drove the need for a more highly-integrated, single-chip solution. The SIXNET design team quickly narrowed its choices to a competitor's SRAM-based FPGA or the Xilinx XC8100 FPGA family.

The main elements of the design include registers to capture and synchronize incoming data, state machines for quadrature decoding, and eight 16-bit counters and latches used for position and velocity measurement. The outputs of the counters and state machines are multiplexed and output on an 8-bit bus. The clock frequency is a modest 4 MHz.

SIXNET engineers quickly discovered that it would be difficult to fit the design using the relatively large logic blocks of the SRAM-based FPGA. The counter logic is register-intensive, requiring very little logic between flip-flops, resulting in substantial "wasted" logic in each logic block. Similarly, the wide multiplexers were not a "good fit," requiring the use of many blocks, but with relatively low utilization of the logic in each block. (These problems would have been even more prevalent in the combinatorial-intensive architecture of a CPLD device.)

The same design was easily implemented in a less-expensive XC8103 FPGA. In the XC8100 FPGA architecture, each fine-grained logic cell can implement either combinatorial or sequential logic, allowing high utilization regardless of the unequal mix of combinatorial functions and flip-flops. The counters were implemented as ripple counters, both to minimize area and avoid switching noise; the flexible clocking structure of the XC8100 architecture enabled this approach. An internal quad latch with output enable — a primitive in the XC8100 library — was used to latch and multiplex the eight counters onto a common bus, eliminating the multiplexing logic needed with the competitor's product.



The design was entered and implemented on a PC using a Viewlogic schematic editor and the Xilinx XACT*step*™ Series 8000 development system, respectively. "The transition from equation entry to Viewlogic schematics was easy, " claims Dave Ellis, vice president of Engineering at SIXNET. "It was just like doing the schematic for a printed circuit board. The XC8100 tools were very easy and intuitive to use. We were able to complete the design phase from concept to a working board in less than four weeks, including learning the Viewlogic and XC8100 design tools." The controller fits on a compact 3.3"x4.3" circuit board.

In conclusion, Mr. Ellis noted, "The Xilinx XC8103 was by far the most cost-effective solution for our needs." ◆

New Product Literature

Learn about the newest Xilinx products and services through our extensive library of product literature. The most recent pieces are listed below. To order or to obtain a complete list of all available literature, please contact your local Xilinx sales representative. ◆

TITLE	DESCRIPTION	NUMBER
FPGAs		
XC4000EX Overview	Features & Benefits	#0010284-01
XC4000 Data Sheet	Technical Data	#0010278-01
XC4000E Data Sheet	Technical Data	#0010274-01
Xilinx XC5200 vs. Altera FLEX 8000A FPGAs White Paper	Technical Data	#0010270-01
LogiCore PCI Target Interface for 4000E FPGA Data Sheet	Technical Data	#0010288-01
XC3100L Data Sheet	Technical Data	#0010285-01
Design Migration from XC3000/XC3000A to XC5200	Technical Data	#0010275-01
EPLDs		
XABEL-CPLD Overview	Features & Benefits	#0010277-01
XABEL-CPLD Evaluation Software	CD-ROM	#500354
XC9500 Data Sheet	Technical Data	#0010280-01
XC9500 Applications Guide	Technical Data	#0010286-01
Development Systems		
XACT*step* Advanced Development System Overview	Features & Benefits	#0010271-01
XACT*step* 5.2 Overview	Features & Benefits	#0010289-01

FINANCIAL RESULTS

Revenue Grows by 58%

Sales revenue up 58% over same quarter in 1995!

Fast XC5200 FPGA family production ramp up!

Xilinx sales revenues achieved a record $144.1 million for the third quarter of fiscal year 1996 (ended December 31, 1995). This is 58% larger than the same quarter in fiscal year 1995. It shows a 2% increase from the second quarter of fiscal year 1996. This quarter's performance was affected by a slowdown in bookings, particularly in the early portion of the quarter.

Growth was particularly strong for the new XC5200 FPGA family. Revenues from this family have "ramped up" faster than any other new product family in Xilinx history.

Sales revenues for the first nine months of fiscal 1996 totaled $411.1 million, an increase of 67% from the comparable period last year.

Looking ahead to the next quarter, CEO Bernie Vonderschmitt stated that, "We are encouraged by recent indications of a return to more normal bookings. Customer inventory corrections that we witnessed this past quarter appear to be mostly completed. Most importantly, we are encouraged by the new products that we have recently introduced, which will begin to contribute meaningful reveunes in calendar 1996."

Founded in 1984, Xilinx is the world's largest supplier of programmable logic devices. Xilinx stock is traded on the NASDAQ exchange under stock symbol XLNX. ◆

Xilinx and XC8100 Receive Excellence Awards in Japan

Hitachi, Ltd. bestowed the prestigious "Hitachi Award for Excellence" on Xilinx in December. Eiji Aoki, deputy general manager of Hitachi's Telecommunications Division, presented the award to representatives of Xilinx KK in Japan.

The XC8100 FPGA was a finalist in the "ASIC of the Year" competition sponsored by Sanyo Times Ltd., publisher of *The Semiconductor Industry News*, a weekly journal. The prize is awarded for products or technologies developed using EDA/ESDA technology. The XC8100 FPGA family was awarded third place in a field of more than 110 entries. ◆

UPCOMING EVENTS

Look for Xilinx technical papers and/or product exhibits at these upcoming industry forums. For further information about any of these conferences, please contact Kathleen Pizzo (Tel: 408-879-5377 FAX: 408-879-4676). ◆

International IC Conference
Mar. 27-29
Shanghai, China

PCI '96
Apr. 14-18
San Jose, California

Digitronics
Apr. 17-18
Birmingham, UK

IEEE Symposium on FPGAs for Custom Computing Machines (FCCM)
Apr. 17-19
Napa, California

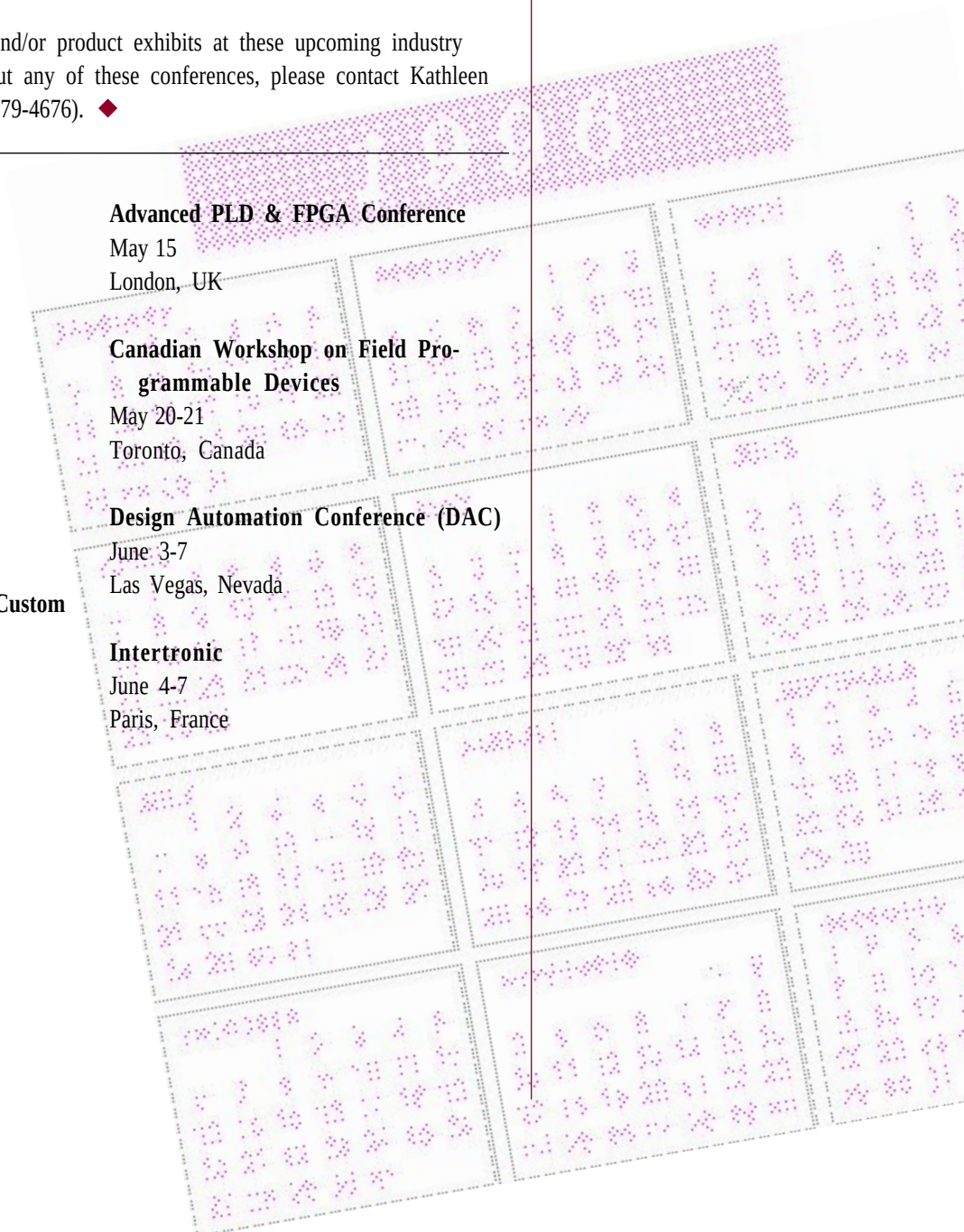
Custom IC Conference (CICC)
May 5-8
San Diego, California

Advanced PLD & FPGA Conference
May 15
London, UK

Canadian Workshop on Field Programmable Devices
May 20-21
Toronto, Canada

Design Automation Conference (DAC)
June 3-7
Las Vegas, Nevada

Intertronic
June 4-7
Paris, France



Xilinx Alliance Goes On-Line

Wallace Westfeldt is the manager of the Xilinx Alliance Program. He can be reached by telephone at 303-413-3280 or by E-mail at wallace.westfeldt@xilinx.com.

Alliance Program Vendors and Contacts

See pages 14-16

Alliance Program E-Mail:

alliance@xilinx.com

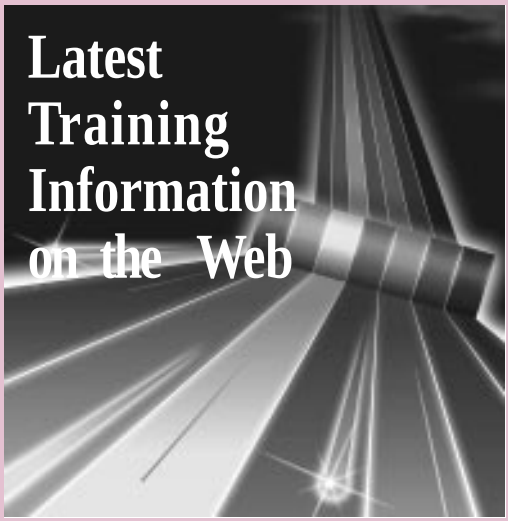
The Xilinx Alliance has been going strong for six years, and 1996 promises to be the most exciting year ever. In addition to bringing you more world-class tools for your world-class products, we will provide easier and innovative ways to find out about the wide variety of high-quality, third-party design tools available through the Alliance.

One example is WebLINX, the Xilinx site on the World Wide Web. In March, the Xilinx Alliance will go on-line. An initial listing of our Alliance partners will allow you to easily search our web pages (and our partners' pages) for product and contact information. The Xilinx *Smart*Search and *Smart*Search Agents utilities *(see related article at right)* will allow you to quickly find the information you need — whether it be product functionality, updates, or compatibility data.

As of February, the Xilinx Alliance includes more than 80 partners who have been selected for their contribution to Xilinx development systems and their ability to provide the widest variety and highest qualiity of design/programming tools for Xilinx programmable logic. These vendors offer well over 100 products, including schematic editors, logic synthesis tools, simulators, third party cores, reconfigurable computing products and device programmers. *(See Alliance Program EDA tool vendor and product list on pages 14-16.)*

The breadth and depth of the Xilinx Alliance is not accidental. Today's programmable logic users are required to complete ever more complex and dense designs more quickly than ever before. Xilinx has recognized those needs by adopting an open systems approach to enable engineers to select the best tools for the task at hand.

So come visit Xilinx and our Alliance partners on the World Wide Web**. E-mail your comments to alliance@xilinx.com.** Tell us about what products you are building, what tools you are using and what tools you need — we will continue to offer you the best programmable logic development solution anywhere. The Xilinx Alliance is dedicated to your success by bringing together complete development solutions for your needs. With Xilinx programmable logic and the Xilinx Alliance, the possibilities are limitless. ◆



Xilinx is adding new training courses and scheduling additional locations in 1996! To get the latest information on available classes, use the Xilinx site on the World Wide Web (http//www.xilinx.com). From the home page, select Customer Support and then Training Classes. You can even register for classes on-line.

Both schematic-based and synthesis-based three-day introductory classes are offered. In January, Xilinx began offering a series of one-day update classes on XACT*step*™ v6, targeted at customers familiar with XACT® 5.0. Watch the web site for new training class support as new products are introduced. ◆

Introducing WebLINX *Smart*Search

The Best Programmable Logic Related Web Searching

From WebLINX, the Xilinx site on the World Wide Web, you can now search and monitor the Web like never before. WebLINX *Smart*Search is the most effective web search engine for finding information related to programmable logic. WebLINX *Smart*Search Agents will proactively inform you when new Web information becomes available that meets your specific interests.

_Smart_Search provides:

- **Selective Multi-site Indexing**
  WebLINX *Smart*Search spans multiple sites, not just the Xilinx site. You get "one-stop" searching of leading industry magazines such as *EE Times* and *Electronic News*, all the major EDA companies, and programmable logic-related organizations, universities and distributors. Unlike generic search engines, WebLINX *Smart*Search yields better results by only searching known content-rich sites.

  For example, if you enter "PCI" in the search engine Lycos, you get pages on Berkeley UNIX pci structs and the PCI home page for geographic management software. With WebLINX *Smart*Search, you'll get more pertinent results like Synopsys' PCI Design Kit, NuHorizons' Technical Forum, the PCI SIG Group, and more.

- **User-selectable Search Domain**
  WebLINX *Smart*Search allows greater control by letting users search by specific site location, such as Xilinx or Cadence. For example, you can search for "Power Dissipation" at only the EDN and Cadence web sites by entering the keywords and selecting the EDN and Cadence checkboxes before starting your search.

- **Intra-site Searching**
  You can even search specific sources within a site. For example, you can search for "counters" and "XC3000A" within Xilinx Application Notes only. Simply type in "counters, XC3000A" and select the Application Notes checkbox.

- ***Smart*Search Topics**
  When you select topics such as "CPLD" by selecting one of the listed check-boxes, WebLINX *Smart*Search will automatically search for all related keywords and phrases like "Programmable Logic Device" and "EPLD," so that you don't miss results you might want. Alternatively, you can also specify literal keywords and phrases that must match precisely to make the results list.

- **Proactive User Notification**
  Say you're interested in the new Xilinx XC9500 family, for example. WebLINX *Smart*Search Agents will monitor the Web for XC9500 information and notify you automatically when new or modified documents become available. You can train WebLINX *Smart*Search Agents to watch for specific information at specific sites or at all of them!

  *Smart*Search and *Smart*Search Agents are the first web information retrieval tools of their kind in any industry. Check them out by visiting our home page at http://www.xilinx.com and selecting the Search button. ◆

Xilinx Web Site:
http://www.xilinx.com

> *"SmartSearch and SmartSearch Agents are the first web information retrieval tools of their kind in any industry. Check them out by visiting our home page at http://www.xilinx.com."*

We're counting on you to keep our search engine useful — if there's a good web site that we're not indexing or a new topic-specific search form you'd like to see, let us know by sending e-mail to webmaster@xilinx.com.

COMPONENT AVAILABILITY CHART

PINS	TYPE	CODE	XC3020A	XC3030A	XC3042A	XC3064A	XC3090A	XC3020L	XC3030L	XC3042L	XC3064L	XC3090L	XC3142L	XC3190L	XC3120A	XC3130A	XC3142A	XC3164A	XC3190A	XC3195A	XC4003E	XC4005E	XC4006E	XC4008E	XC4010E	XC4013E	XC4020E	XC4025E	XC4028EX	XC4036EX	XC4044EX	XC4052EX	XC4062EX	XC4085EX	XC40125EX
44	PLASTIC LCC	PC44		◆												◆																			
	PLASTIC QFP	PQ44																																	
	PLASTIC VQFP	VQ44																																	
	CERAMIC LCC	WC44																																	
48	PLASTIC DIP	PD48																																	
64	PLASTIC VQFP	VQ64		◆					◆							◆																			
68	PLASTIC LCC	PC68	◆	◆											◆	◆																			
	CERAMIC LCC	WC68																																	
	CERAMIC PGA	PG68																																	
84	PLASTIC LCC	PC84	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆										
	CERAMIC LCC	WC84																																	
	CERAMIC PGA	PG84	◆	◆	◆										◆	◆	◆																		
100	CERAMIC QFP	CQ100																																	
	PLASTIC PQFP	PQ100	◆	◆	◆										◆	◆	◆				◆	◆													
	PLASTICTQFP	TQ100														◆	◆																		
	PLASTIC VQFP	VQ100		◆	◆				◆	◆						◆	◆				◆														
	TOP BRZ. CQFP	CB100	◆		◆										◆	◆																			
120	CERAMIC PGA	PG120																			◆														
132	PLASTIC PGA	PP132			◆	◆											◆	◆																	
	CERAMIC PGA	PG132			◆	◆											◆	◆																	
144	PLASTICTQFP	TQ144			◆	◆				◆	◆		◆	◆			◆	◆				◆	◆												
	CERAMIC PGA	PG144																																	
156	CERAMIC PGA	PG156																				◆	◆												
160	PLASTIC PQFP	PQ160				◆	◆											◆	◆	◆		◆	◆	◆	◆	◆								
164	CERAMIC QFP	CQ164																																	
	TOP BRZ. CQFP	CB164					◆												◆	◆															
175	PLASTIC PGA	PP175					◆												◆	◆															
	CERAMIC PGA	PG175					◆												◆	◆															
176	PLASTICTQFP	TQ176					◆					◆		◆					◆																
184	CERAMIC PGA	PG184																																	
191	CERAMIC PGA	PG191																																	
196	TOP BRZ. CQFP	CB196																																	
208	PLASTIC PQFP	PQ208					◆												◆	◆		◆	◆	◆	◆	◆								
	METAL MQFP	MQ208																																	
	HI-PERF QFP	HQ208																								◆	◆		❖						
223	CERAMIC PGA	PG223																		◆						◆	◆	◆							
225	PLASTIC BGA	BG225																							◆	◆									
	WINDOWED BGA	WB225																																	
228	TOP BRZ. CQFP	CB228																																	
240	PLASTIC PQFP	PQ240																								◆	◆	◆							
	METAL MQFP	MQ240																																	
	HI-PERF QFP	HQ240																								◆	◆		❖						
299	CERAMIC PGA	PG299																										◆	❖						
304	HI-PERF QFP	HQ304																										◆	❖	❖					
352	PLASTIC BGA	BG352																											❖						
411	CERAMIC PGA	PG411																												❖	❖				
432	PLASTIC BGA	BG432																												❖	❖	❖			
499	CERAMIC PGA	PG499																														❖	❖	❖	
596	PLASTIC BGA	BG596																														❖	❖	❖	❖

◆ = Product currently shipping or planned

❖ = New since last issue of XCELL

FEBRUARY 1996

PINS	TYPE	CODE	XC4005L	XC4010L	XC4013L	XC5202	XC5204	XC5206	XC5210	XC5215	XC7236A	XC7272A	XC7318	XC7336	XC7336Q	XC7354	XC7372	XC73108	XC73144	XC8100	XC8101	XC8103	XC8106	XC8109	XC95108	XC95216	XC9536
	PLASTIC LCC	PC44									◆		◆	◆	◆	◆				❖							❖
	PLASTIC QFP	PQ44											◆	◆	◆												
44	PLASTIC VQFP	VQ44													◆												
	CERAMIC LCC	WC44									◆			◆	◆	◆											❖
48	PLASTIC DIP	PD48																									
64	PLASTIC VQFP	VQ64																									
	PLASTIC LCC	PC68										◆				◆	◆										
68	CERAMIC LCC	WC68										◆				◆	◆										
	CERAMIC PGA	PG68																									
	PLASTIC LCC	PC84	◆	◆		◆	◆	◆	◆			◆					◆	◆			◆	◆	◆	❖	◆		
84	CERAMIC LCC	WC84										◆					◆	◆									
	CERAMIC PGA	PG84																									
	CERAMIC QFP	CQ100																									
	PLASTIC PQFP	PQ100				◆	◆	◆									◆	◆			◆	◆	◆		◆		
100	PLASTIC TQFP	TQ100																							❖		
	PLASTIC VQFP	VQ100																									
	TOP BRZ. CQFP	CB100																									
120	CERAMIC PGA	PG120																									
132	PLASTIC PGA	PP132																									
	CERAMIC PGA	PG132																									
144	PLASTIC TQFP	TQ144				◆	◆	◆	◆																		
	CERAMIC PGA	PG144																◆									
156	CERAMIC PGA	PG156				◆	◆																				
160	PLASTIC PQFP	PQ160					◆	◆	◆									◆	◆						◆	❖	
164	CERAMIC QFP	CQ164																									
	TOP BRZ. CQFP	CB164																									
175	PLASTIC PGA	PP175																									
	CERAMIC PGA	PG175																									
176	PLASTIC TQFP	TQ176		◆																							
184	CERAMIC PGA	PG184																									
191	CERAMIC PGA	PG191						◆																			
196	TOP BRZ. CQFP	CB196																									
	PLASTIC PQFP	PQ208	◆	◆	❖			◆	◆	◆																❖	
208	METAL MQFP	MQ208																									
	HI-PERF QFP	HQ208								◆																❖	
223	CERAMIC PGA	PG223							◆																		
225	PLASTIC BGA	BG225			❖					◆								◆	◆					❖			
	WINDOWED BGA	WB225																	◆								
228	TOP BRZ. CQFP	CB228																									
240	PLASTIC PQFP	PQ240			❖				◆																		
	METAL MQFP	MQ240																									
	HI-PERF QFP	HQ240								◆																	
299	CERAMIC PGA	PG299								◆																	
304	HI-PERF. QFP	HQ304								◆																	
352	PLASTIC BGA	BG352																									
411	CERAMIC PGA	PG411																									
432	PLASTIC BGA	BG432																									
499	CERAMIC PGA	PG499																									
596	PLASTIC BGA	BG596																									

ALLIANCE PROGRAM - EDA COMPANIES & PRODUCTS - FEBRUARY 1996 - 1 OF 2

CompName	ProdName	Version	Function	DesignKit	2k3k4k	XC5200	CPLD7k9k	UniLib	6200	8100
ACEO Technology	Softwire	3.3	Multi-FPGA Partitioning	Included	✓	✓		✓		
	Gatran	3.3	ASIC to FPGA Netlist Mapping	Included	✓	✓		✓		
	Asyn	3.3	Synthesis	Included	✓	✓		✓		
Acugen Software	ATGEN	2.60	Automatic Test Generation	AALCA interface	✓	✓	7k			
	Sharpeye	2.60	Testability Analysis	AALCA interface	✓	✓	7k			
Aldec	Active-CAD	2.2	Schematic Entry & Simulation & HDL Editor	Included	✓	✓	7k	✓		
ALPS LSI Technologies	Edway Design Systems		Synthesis/Simlulation		✓		✓			
Aptix Corporation	System Explorer	2.1	System Emulation	Axess 2.1	✓	✓		✓	✓	✓
	ASIC Explorer	2.3	ASIC Emulation	Explorer 2.3	4K	✓		✓		
Aster Ingenierie S.A.	XILLAS	4.1	LASAR model generation	Worst Case Simulation	✓		7k			
Cadence	Concept	2.1	Schematic Entry	Xilinx Front End	✓		7k	✓	TBD	Q2
	Composer	4.3.4/4.4	Schematic Entry	Xilinx Front End	✓		7k	✓	TBD	TBD
	Verilog	2.3.2	Simulation	Xilinx Front End	✓	✓	7k	✓	Q2	Q2
	FPGA Designer	9504	Topdown FPGA Synthesis	Call Xilinx	✓	✓	7k	✓	Q2	Q2
	Synergy	2.3	FPGA Synthesis	Call Xilinx	✓	✓	7k	✓	Q2	Q2
Capilano Computing	Design Works	3.1	Schematic Entry/Sim	XD-1	✓			✓		
Chronology Corporation	TimingDesigner									
CINA - Computer Integrated Network Analysis	SmartViewer	1.0c	Schematic Generator	XNF Interface	✓	✓	7k	✓		
Compass Design Automation	QSim		Simulation		3k,4k					
	ASIC Synthesizer		Synthesis		3k,4k					
	Logic Assistant		Design Capture	Xilinx Des. Kit	3k,4k					
	QTV		Timing Analysis		3k,4k					
Escalade	DesignBook		Design Entry		✓			✓		
Exemplar Logic	Galileo	3.2	Synthesis/Timing Analysis Simulation	Included	3k,4k	✓	7k			✓
Flynn Systems	FS-ATG	3.0	Test Vector Generation	Xilinx Kit	✓	✓	7k			
	Probe	3.0	Testability Analysis	Xilinx Kit	✓	✓	7k			
	CKTSIM	3.0	Logic Analysis	Xilinx Kit	✓	✓	7k			
	FS-SIM	3.0	Simulation	Xilinx Kit	✓	✓	7k			
Fujitsu LSI	PROVERD		Top-Down Design System	Included	3k,4k					
Harmonix Corporation	PARTHENON	2.3	Synthesis		4k		7k			
IBM-EDA	Boole-Dozer		Synthesis		✓					
IK Technology Co.	ISHIZUEPROFESSIONALS	1.05.02	Schematic Entry/Simulation	Xilinx Design Kit	✓					
IKOS Systems	Voyager	2.2	Simulation	Xilinx Tool Kit	✓					
	Gemini	1.1	Mixed Level Verilog Simulation	Xilinx Tool Kit	✓					
INCASES Engineering	Theda	4.0	Schematic Entry	Xilinx Kit	✓					
ISDATA	LOG/iC2	4.2	Synthesis Simulation	Xilinx Mapper	✓	✓	7k	✓		
	LOG/iC Classic	4.2	Synthesis	LCA-PP	✓		7k	✓		
ITS	XNF2LAS	1a	Lasar model gen.	XNF2LAS	✓					
Logic Modeling Corp. (Synopsis Division)	Smart Model		Simulation Models	In Smart Model Libary	✓	✓	7k,9k			
	Hardware Models (LM fAMILY & ModelSource Series)		Simulation Models	Xilinx Logic Module	✓		7k,9k			
Logical Devices	CUPL Total Designer	4.7	Synthesis	Xilinx Fitter	✓	✓	7k			
Mentor Graphics	QuickSim II	A.x_F	Simulation	Call Xilinx	✓	✓	7k	✓		✓
	Design Architect	A.x_F	Schematic Entry	Call Xilinx	✓	✓	7k	✓		✓
	Autologic	A.x_F	Synthesis	Xilinx Synthesis Library	✓	✓	7k	✓		✓

ALLIANCE PROGRAM - EDA COMPANIES & PRODUCTS - FEBRUARY 1996 - 2 OF 2

CompName	ProdName	Version	Function	DesignKit	2k3k4k	XC5200	CPLD7k9k	UniLib	6200	8100
MINC	PLDesigner-XL	3.3	Synthesis	Xilinx Design Module	✓					
MINC - IST	ASYL+	3.2.1	Synthesis, Partitioning	XNF interface	✓	✓	7k	✓		
Minelec	Ulticap	1.32	Schematic Entry	Xilinx Interface	2k,3k					
OrCAD	SDT386+ (DOS)	1.2	Schematic Entry	Call Xilinx	✓		7k	✓		
	Capture (Win)	6.1.1	Schematic Entry	Call Xilinx	✓	✓	7k	✓		
	VST 386+ (DOS)	1.2	Simulation	Call Xilinx	✓		7k	✓		
	Simulate (Win)	6.0.1	Simulation	Call Xilinx						
	PLD 386+ (DOS)	2.0	Synthesis	Call OrCAD	✓		7k			
Protel Technology	Advanced Schematic	3.1	Schematic Entry/Client Server	Xilinx Interface	✓		7k			
Quad Design Technology	Motive	4.3	Timing Analysis	Call Xilinx	✓					✓
SimuCad	Silos III	95.100	Simulation	Included	✓			✓		✓
Sophia Sys & Tech	Vanguard	5.31	Schematic Entry	Xilinx I/F Kit	✓		✓			
Summit Design	Visual HDL	3.0	Graphical Entry/Simulation/Debug	EDIF Interface	✓	✓	✓	✓	✓	✓
Synario Design Automation	ABEL	6.2	Synthesis, Simulation	XEPLD Fitter			7k,9k	✓		
	Synario	2.2	Schematic Entry, Synthesis & Simulation	SYN-LCA	✓	✓	7k,9k	✓		
Synopsys	FPGA Compiler	3.4a	Synthesis	Call Xilinx	3K, 4K	✓	7k	✓		✓
	Design Compiler	3.4a	Synthesis	Call Xilinx	✓	✓	7k	✓		✓
	VSS	3.4a	Simulation	Call Xilinx	✓	✓	7k	✓		✓
Synplicity	Synplify	2.5c	Synthesis	Included	3K, 4K	✓		✓		
	Synplify-Lite	2.5c	Synthesis	Xilinx Mapper	3K, 4K	✓		✓		
Teradyne	Lasar	6	Simulation	Xilinx I/F Kit	✓					
The Rockland Group	State Machine Library		Graphic Design for One-Hot State Machines	Xilinx Kit	✓	✓		✓	✓	
Tokyo Electron Limited	ViewCAD	1.2	FLDL to XNF translator	XNFGEN	✓					
TopDown Design Solutions	V-BAK\Vital	2.1	XNF to VHDL translator	XNFinterface	✓	✓		✓		
Trans EDA Limited	TransPRO	1.2	Synthesis	Xilinx Library	✓					
VEDA Design Automation	Vulcan	4.5	Simulation	XILINX Tool Kit	✓					
VeriBest	AdvanSIM-1076	12.0	Simulation	Xilinx FPGA Design Kit	3k,4k			✓		
	VeriBest Simulator	14.0	Simulation	Xilinx FPGA Design Kit	3k,4k	✓		✓		✓
	DMM	14.0	Design Management	Xilinx FPGA Design Kit	3k,4k	✓		✓		
	VeriBest Synthesis	14.0	Synthesis	Xilinx FPGA Design Kit	3k,4k	✓		✓		
	Synovation	12.2	Synthesis	Xilinx FPGA Design Kit	3k,4k			✓		
	PLDSyn	12.0	Design Entry Synthesis		✓		7k			
	VeriBest Design Capture	14.0	Design Capture	Xilinx FPGA Design Kit	3k,4k	✓		✓		
	ACE Plus	12.2	Schematic Entry	Xilinx FPGA Design Kit	3k,4k			✓		
Viewlogic	WorkView Office	7.0	Schem/Sim	Call Xilinx	✓	XACT6	7k	✓	✓	✓
	Pro Series	6.1	Schem/Sim/Synth	call Xilinx	✓	XACT6	7k	✓	✓	✓
	PowerView	5.3.2	Schem/Synth	call Xilinx	✓	XACT6	7k	✓	✓	✓
	ViewSynthesis	6.0	Synthesis	call Xilinx	✓	XACT6	7k	✓	✓	✓
Visual Software Solutions, Inc.	StateCAD	2.1	State Diagram	Xilinx fitter	✓					
Zuken	Tsutsuji		Synthesis/Simulation	XNFInterface	3k,4k					
Zycad	Paradigm XP		Gate-level Sim		✓					
	Paradigm RP		Rapid Prototyping		✓					

ALLIANCE PROGRAM - PLATFORMS & CONTACTS - FEBRUARY 1996

Company Name	Contact Name	Contact (Telephone or E-mail)	PC	Sun	RS6000	HP7
ACEO Technology, Inc.	Ray Wei	510-656-2189	✓	✓	✓	✓
Acugen Software, Inc.	Nancy Hudson		✓	✓		✓
Aldec	David Rinehart		✓			
Aptix Corporation	Robert Sarkaisian	408-428-6209				
Aster Ingenierie S.A.	Christopher Lotz	339-953-7171	✓	✓		✓
Cadence	Itzhak Shapira Jr.	408-428-5793		✓	✓	✓
Capilano Computing	Chris Dewhurst	604-522-6200	✓			
Chronology Corporation	Mike McClure	sales@chronology.com				
CINA - Computer Integrated Network Analysis	Brad Ashmore	info@cina.com	✓			
Compass Design Automation	Terry Strickland	408-434-7493		✓		✓
Escalade	Mark Miller	408-481-1300	✓	✓		
Exemplar Logic	Mary Murphy	510-337-3700	✓	✓		
Flynn Systems	Mike Jingozian	603-598-4444	✓			
Fujitsu LSI	Masato Tsuru	+81-4-4812-8043	✓			
Harmonix Corporation	Shigeaki Hakusui	617-935-8335	✓	✓		
IBM - EDA	George Doerre	914-433-9086			✓	
IK Technology Co.	Tsutomu Someyu	+81-3-3839-0606	✓	✓		✓
IKOS Systems	Larry Melling	408-255-4567		✓		✓
INCASES Engineering	Christian Kerscher	+49-89-839910				✓
ISDATA	Ralph Remme	+49-721-751087	✓	✓		✓
ITS	Frank Meunier	508-897-0028		✓		✓
Logic Modeling	Marnie McCollow	503-531-2412	✓	✓	✓	✓
Logical Devices	David Mot	303-279-6868	✓			
Mentor Graphics	SamPicken	503-685-1298		✓	✓	✓
MINC	Kevin Bush	719-590-1155	✓	✓		✓
Minelec	Marketing Department	+32-02-4603175	✓			
OrCAD	Troy Scott	503-671-9500	✓			
Protel Technology	Matthew Schwaiger	408-243-8143	✓			
Quad Design Technology	Britta Sullivan	805-988-8250	✓	✓	✓	✓
SimuCad	Richard Jones	510-487-9700	✓			
Sophia Sys & Tech	Bobby Alvarez	408-232-4764	✓	✓		✓
Summit Design Corporation	Ed Sinclari	503-643-9281	✓	✓	✓	✓
Synario Design Automation	Jacquelin Taylor	206-867-6257	✓			
Synopsys	Lynn Fiance	415-694-4289		✓	✓	✓
Synplicity	Alisa Yaffa	415-961-4962	✓	✓		
Teradyne	Mike Jew	617-422—3753		✓		✓
The Rockland Group	Rocky Awalt	916-622-7935	✓	✓	✓	✓
TopDown Design Solutions	ArtPisani	603-888-8811	✓	✓	✓	
Trans EDA Limited	James Douglas	+44-1703-255118		✓		✓
VEDA Design Automation	Kathie O'Toole	408-496-4515		✓		✓
VeriBest	Will Wong	415-961-9680	✓	✓		✓
Viewlogic	Preet Virk	508-480-0881	✓	✓	✓	✓
Visual Software Solutions	Andy Bloom	305-423-8448				
Zuken	Makato Ikeda	+81-4-5942-7787		✓	✓	✓
Zycad	Mike Hannig	201-989-2900		✓		✓

Inquiries about the Xilinx Alliance Program can be E-mailed to alliance@xilinx.com.

PROGRAMMER SUPPORT FOR XILINX XC1700 SERIAL PROMS — FEBRUARY 1996

MANUFACTURER	MODEL	1736A 1765	17128	1718D 1736D 1765D	1718L 1765L	17128D 17256D
ADVANTECH	PC-UPROG		V2.1	V2.0	V2.0	V2.1
	LABTOOL-48		V1.0	V1.0	V1.0	V1.0
ADVIN	PILOT-U24	10.83	10.83	10.83	10.83	10.83
	PILOT-U28	10.83	10.83	10.83	10.83	10.83
	PILOT-U32	10.83	10.83	10.83	10.83	10.83
	PILOT-U40	10.83	10.83	10.83	10.83	10.83
	PILOT-U84	10.83	10.83	10.83	10.83	10.83
	PILOT-142	10.83	10.83	10.83	10.83	10.83
	PILOT-143	10.83	10.83	10.83	10.83	10.83
	PILOT-144	10.83	10.83	10.83	10.83	10.83
	PILOT-145	10.83	10.83	10.83	10.83	10.83
B&C MICROSYSTEMS	Proteus-UP40	V3.4e	V3.4e	V3.5f	V3.7f	V3.7l
BP MICROSYSTEMS	CP-1128	C	V2.17	V2.21c	V2.34	V3.06
	EP-1140	C	V2.17	V2.21c	V2.34	V3.06
	BP-1200	V3.12	V3.12	V3.12	V3.12	V3.12
	BP-2100	V3.12	V3.12	V3.12	V3.12	V3.12
BYTEK	135H-FT/U	V42	V51	V51	V51	
	MTK-1000	V42	V51	V51	V51	
	MTK-2000	V42	V51	V51	V51	
	MTK-4000	V42	V51	V51	V51	
DATA I/O	UniSite	V4.0	V4.1	V4.1	V4.6	V4.8
	2900	V2.1	V2.2	V2.2	V3.4	V3.6
	3900	V1.5	V1.6	V1.6	V2.4	V2.6
	AutoSite	V1.5	V1.6	V1.6	V2.4	V2.6
	ChipLab	V1.1	V1.0	V1.0	V1.1	V3.0
	2700	V3.0	V3.0	V3.0	V3.0	V3.0
DEUS EX MACHINA	XPGM		V1.40	V1.40	V1.40	V1.40
ELECTRONIC ENGINEERING TOOLS	ALLMAX/ALLMAX+	V1.3	V1.5	V1.5	V1.5	V2.3e
	PROMAX	V2.34	V2.34	V2.34	V2.34	V2.34
ELAN DIGITAL SYSTEMS	3000-145	C	C			
	5000-145	C	C			
	6000 APS	K2.01	K2.02	K2.01	K2.10	K2.14
HI-LO SYSTEMS RESEARCH	All-03A	V3.30	V3.30	V3.30	V3.30	V3.50
	All-07	V3.30	V3.30	V3.30	V3.30	V3.47
ICE TECHNOLOGY LTD	Micromaster 1000/1000E	V1.1	V3.00	V3.00	V3.07	V3.00
	Speedmaster 1000/1000E	V1.1	V3.00	V3.00	V3.07	V3.00
	Micromaster LV	V3.003	V3.00	V3.00	V3.00	V3.00
	LV40 Portable					
	Speedmaster LV		V3.00	V3.00	V3.00	V3.00
LEAP ELECTRONICS	LEAPER-10					
	LEAP-SU1					
	LEAP-U1					

MANUFACTURER	MODEL	1736A 1765	17128	1718D 1736D 1765D	1718L 1765L	17128D 17256D	17128L 17256L
LINK COMPUTER GRAPHICS	CLK-3100	V5.08	V5.08	V5.08			
LOGICAL DEVICES	ALLPRO-40	V2.2					
	ALLPRO-88	V2.2	V2.3	V2.3		V2.5	
	ALLPRO-88XR	V1.1	V2.3	V1.3		V2.3	
	CHIPMASTER 3000	V2.0	V2.1	V2.0	V2.3		
	CHIPMASTER 6000	V1.15					
	XPRO-1	V1.01	V1.01	V1.01	V1.01	V3.04	
MQP ELECTRONICS	MODEL 200	C	6.45	6.45	6.45	6.46	
	SYSTEM 2600						
	PINMASTER 48						
MICROPROSS	ROM 5000 B	C	V1.70	V1.70	V1.89	V1.89	
	ROM 3000 U	C	V3.60	V3.60	V3.79	V3.79	
	ROM9000				V1.5	V1.5	
NEEDHAM'S ELECTRONICS	EMP20	V1.5	V1.5	V2.92	V2.92	V2.92	
RED SQUARE	IQ-180	C	V9.2	V8.2	V9.2	V9.2	
	IQ-280	C	V9.2	V8.2	V9.2	V9.2	
	Uniwriter 40	C	V9.2	V8.2	V9.2	V9.2	
	Chipmaster 5000	C	V9.2	V8.2	V9.2	V9.2	
SMS	Expert	B/93	A/94	A/94	A1/94	Cx/94	
	Optima	B/93	A/94	A/94	A1/94	Cx/94	
	Multisyte			A/94		Cx/94	
	Sprint Plus 48	B/93	A/94	A/94	A1/94	A/95	
STAG	Eclipse		4.4	V2.2	V4.3	V4.10.31	
	Quasar	10.76C	10.76C	V10.76C	V10.76C	V10.78B	
SUNRISE	T-10 UDP	V3.31	V3.31	V3.31	V3.31	V3.31	
	T-10 ULC	V3.31	V3.31	V3.31	V3.31	V3.31	
SUNSHINE	POWER-100	V8.18	V8.18	V8.18	V8.18	V8.18	
	EXPRO-60/80	V8.18	V8.18	V8.18	V8.18	V8.18	
SYSTEMGENERAL	TURPRO-1	V2.21F	V2.21F	V2.21F	V2.21F	V2.21F	
	TURPRO-1 FIX	V2.21F	V2.21F	V2.21F	V2.21F	V2.21F	
	APRO	C	V2.14	V2.01	V2.12		
	MULTI-APRO	V1.13E	V1.13E	V1.13E	V1.13E	V1.13E	
TRIBAL MICROSYSTEMS	TUP-300	C	V3.31	V3.31	V3.37C	V3.47	
	TUP-400	C	V3.31	V3.31	V3.37C	V3.50	
	FLEX-700	C	V3.31	V3.31	V3.37C	V3.47	
XELTEK	SuperPRO	1.5B	1.7C	1.7D	1.8	2.2A	
	SuperPRO II	1.5B	1.7C	1.7D	1.8	2.2A	
XILINX	HW-112	4.02	4.06	5.00	5.00	5.00	
	HW-120	2.03	2.03	2.03	2.03	3.01	
	HW-130		1.11	2.01	2.01	2.01	1.00

PROGRAMMER SUPPORT FOR XILINX XC7200 EPLDS — FEBRUARY 1996

MANUFACTURER	MODEL	7236	7236A	7272	7272A
ADVANTECH	PC-UPROG	V2.4	V2.4	V2.4	V2.4
	LabTool-48	V1.0	V1.0	V1.0	V1.0
ADVIN SYSTEMS	Pilot-U40	10.77E	10.77E		
	Pilot-U84	10.77E	10.77E	10.77E	10.77E
B&C MICROSYSTEMS INC.	Proteus	V3.6j	V3.6j	V3.7h	V3.7h
BP MICROSYSTEMS	BP-1200	3.12	3.12	3.12	3.12
	BP-2100	3.12	3.12	3.12	3.12
DATA I/O	UniSite	4.9	4.9	V4.5	V4.5
	2900	4.9	4.9		
	3900	4.9	4.9	V2.3	V2.3
	AutoSite	4.9	4.9	V2.3	V2.3
DEUS EX MACHINA ENGINEERING	XPGM	V1.40	V1.40	V1.40	V1.40
ELECTRONIC ENGINEERING TOOLS	ALLMAX/ALLMAX+	V2.1	V2.1	V2.1	V2.1
	PROMAX	V2.34	V2.34	V2.5	V2.5
ELAN DIGITAL SYSTEMS	6000 APS	K2.04	K2.04	K2.06	K2.06
HI-LO SYSTEMS RESEARCH	All-03A	V3.01	V3.01	V3.00	V3.00
	All-07	V3.01	V3.01	V3.00	V3.00
ICE TECHNOLOGY LTD	Micromaster 1000/E	VX1.00	VX1.00	VX1.00	VX1.00
	Speedmaster 1000/E	VX1.00	VX1.00	VX1.00	VX1.00
	Micromaster LV	VX1.00	VX1.00	VX1.00	VX1.00
	Speedmaster LV	VX1.00	VX1.00	VX1.00	VX1.00
LEAP ELECTRONICS	LEAPER-10				
	LEAP-SU1				
	LEAP-U1				
LOGICAL DEVICES	ALLPRO-88	2.2	V2.4	2.2	V2.4
	ALLPRO-88XR	1.35	V2.4	1.35	V2.4
	XPRO-1	3.3	3.3	1.01	1.01
MICROPROSS	ROM9000				
MQP ELECTRONICS	SYSTEM 2000				
	PINMASTER 48				
NEEDHAM'S ELECTRONICS	EMP20	V2.92	V2.92	V2.92	V2.92
STAG	Eclipse	V5.7.3	V5.7.3	V5.7.3	V5.7.3
SMS	Expert	A1/94	A1/94	A1/94	A1/94
	Optima	A1/94	A1/94	A1/94	A1/94
	Multisyte	A1/94	A1/94	A1/94	A1/94
SUNRISE ELECTRONICS	T-10 UDP	V3.31	V3.31	V3.31	V3.31
	T-10 ULC	V3.31	V3.31	V3.31	V3.31
SUNSHINE ELECTRONICS	POWER-100	V8.16	V8.16		
	EXPRO-60/80	V8.16	V8.16		
SYSTEMGENERAL	TURPRO-1/FX	V2.12	V2.12	V2.12	V2.12
	MULTI-APRO	V1.13E	V1.13E	V1.13E	V1.13E
TRIBAL MICROSYSTEMS	TUP-300	V3.0	V3.0	V3.0	V3.0
	TUP-400	V3.0	V3.0	V3.0	V3.0
	FLEX-700	V3.0	V3.0	V3.0	V3.0
XELTEK	SUPERPRO	1.7C	2.2	2.1	2.1
	SUPERPRO II	1.7C	2.2	2.1	2.1
XILINX	HW-120	2.02	2.02	2.02	2.02
	HW-130	1.14	1.14	1.04	1.04

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PROGRAMMER SUPPORT FOR XILINX XC7300 EPLDS — FEBRUARY 1996

MANUFACTURER	MODEL	7318	7336	7336Q	7354	7372	73108	73144
ADVANTECH	PC-UPROG LABTOOL-48	V2.4 V1.0	V2.6 V2.6	V2.6 V1.2	V2.4 V1.0	NS V1.04	NS V1.04	
ADVIN SYSTEMS	PILOT-U40 PILOT-U84	10.78N 10.78B	10.78N 10.78B	10.8 10.8	10.78N 10.78B	10.78B	10.79	
B&C MICROSYSTEMS	Proteus	3.7k	3.7k		3.7k	3.71	3.7k	
BP MICROSYSTEMS	BP-1200 BP-2100	V3.12 V3.12	V3.12 V3.12	V3.12 V3.12	V3.12 V3.12	V3.12 V3.12	V3.13 V3.13	
DATA I/O	2900 3900/AutoSite UniSite	4.9 4.9 4.9	4.9 4.9 4.9	4.9 4.9 4.9	4.9 4.9 4.9	4.9 4.9	4.9 4.9	
DEUS EX MACHINA	XPGM	V1.40	V1.40	V1.40	V1.40	V1.40	V1.40	
ELECTRONIC ENGINEERING TOOLS	ALLMAX/ALLMAX+ PROMAX	V2.1 V2.34	V2.1 V2.34	 V2.88	V2.1 V2.34	V2.1 V2.57		
ELAN	6000 APS	k2.13	k2.13		k2.13	k2.13	k2.13	
HI-LO SYSTEMS RESEARCH	All-03A All-07	V3.04 V3.02	V3.04 V3.02	V3.08 V3.08	V3.04 V3.02	V3.05 V3.01	V3.01 V3.00	
ICE TECHNOLOGY LTD	Micromaster 1000/E Speedmaster 1000/E Micromaster LV Speedmaster LV	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	 V1.2 V1.2	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	
LOGICAL DEVICES	ALLPRO-88 ALLPRO-88XR XPRO-1	V2.5 V2.5 3.3	V2.5 V2.5 3.3		V2.5 V2.5 1.01	V2.5 V2.5 1.01	V2.5 V2.5 1.01	
MICROPROSS	ROM9000							
MQP ELECTRONICS	SYSTEM 2000 PINMASTER 48							
NEEDHAM'S ELECTRONICS	EMP20	V2.92	V2.92	V2.92	V2.92	V2.92	V2.92	
SMS	EXPERT OPTIMA	C/94 C/94	C/94 C/94		C/94 C/94			
STAG	ECLIPSE	V4.10.31	V4.10.31	5.8.24	V4.10.31	V4.10.31	V4.10.31	
SUNRISE	T-10 UDP T-10 ULC	V3.31 V3.31	V3.31 V3.31		V3.31 V3.31	V3.31 V3.31	V3.31 V3.31	
SUNSHINE	POWER-100 EXPRO-60/80	V8.18	V8.18	V8.18	V8.18	V8.18	V8.18	
SYSTEMGENERAL	TURPRO-1/FX MULTI-APRO	V2.2 1.13E	V2.2 1.13E	V2.22I 1.13E	V2.2 1.13E	V2.2 1.13E	V2.2 1.13E	
TRIBAL MICROSYSTEMS	Flex-700 TUP-300 TUP-400	V3.02 V3.03 V3.03	V3.02 V3.03 V3.03	V3.08 V3.08 V3.08	V3.02 V3.03 V3.03	V3.01 V3.03 V3.03	V3.00	
XELTEK	SUPERPRO SUPERPRO II	2.1 2.1	2.2A 2.2A		2.1 2.1	2.2B 2.2B		
XILINX	HW-120 HW-130	3.13 1.15	3.13 1.15	1.00 1.06	3.00 1.16	1.01 1.05	3.01 1.07	 1.02

WHITE=changed since last issue

XILINX RELEASED SOFTWARE STATUS - MARCH 1996

	Key	Product Category	Product Description	Product Function	Xilinx Part Reference Number	Current Version by Platform PC1 6.2	SN2 4.1.x	HP7 9.01	Last Updt Comp	Previous Version Release	Comments Features
XILINX INDIVIDUAL PRODUCTS		CORE EPLD	XC7K Support	Core Implementation	DS-550-xxx	6.00	5.20	5.20	11/95	5.10	PC update by request only
		XABEL-CPLD	XC7K Support	Entry/Simulation/Core	DS-571-PC1	6.01			2/96	6.00	Keyless version - update not required
		Mentor	8.4(A.3-F)	I/Fand Libraries	DS-344-xxx		5.20	5.20	11/95	5.11	No AP1update
		OrCAD		I/Fand Libraries	DS-35-PC1	5.20			11/95	5.10	Support for SDT+, VST+ v1.2
		Synopsys		I/Fand Libraries	DS-401-xxx		5.20	5.20	11/95	3.30	Includes XC5200 X-BLOX Support
		Viewlogic	PROcapture	I/Fand Libraries	DS-390-PC1	6.00			11/95	5.11	Includes PRO Series 6.1
		Viewlogic	PROsim	I/Fand Libraries	DS-290-PC1	6.00			11/95	5.11	Includes PRO Series 6.1
		Viewlogic		I/F and Libraries	DS-391-xxx	6.00	5.20	5.20	11/95	5.11	
		XABEL		Entry,Simulation,Lib, Optimizer	DS-371-xxx	5.20	5.20	5.20	11/95	5.10	Nowavailable on HP7
		XBLOX		Module Generator & Optimizer	DS-380-xxx	5.20	5.20	5.20	11/95	5.10	
	PR	CORE EPLD	XC9K Support	Core Implementation	PR-9500-PC1	1.00			na	na	Product Marketing approval required
	E	Verilog	2K,3K,4K,7K Libraries	Models & XNF Translator	ES-VERILOG-xxx		1.00	1.00	na	na	Sun and HP
	N	LogiCore	4KE Support	PCIInterface	LC-DI-PCIM-C	1.00	1.00	1.00	na	na	Requires signed license agreement
	N	Evaluation	Evaluation Kit		EV-PCI-C	6.0					6.0, Foundation, 8000, XABEL-CPLD support
	N	Evaluation	Evaluation Kit		EV-WS-C		5.2	5.2			5.2, 8000 support
XILINX PACKAGES		Cadence	Standard		DS-CDN-STD-xxx		5.20	5.20	11/95	5.11	
		XC8000	Standard	8kCore+Schematic Libraries	DS-8000-STD-xxx	1.10	1.10	1.10	na	na	w/schematic and simulation libraries
		XC8000	Extended	8kCore+Synthesis Libraries	DS-8000-EXT-xxx	1.10	1.10	1.10	08/95	1.00	w/schematic, simulation, synthesis libraries
		Mentor	Standard		DS-MN8-STD-xxx		5.20	5.20	11/95	5.11	No AP1update
		Mentor	Advanced		DS-MN8-ADV-xxx		7.00	7.00	na	na	
	U	OrCAD	Base		DS-OR-BAS-PC1	6.00			11/95	5.11	Update by request only
		OrCAD	Standard		DS-OR-STD-PC1	6.00			11/95	5.11	
		Synopsys	Standard		DS-SY-STD-xxx		5.20	5.20	11/95	5.12	Includes DS-401 v5.2
		Synopsys	Advanced		DS-SY-ADV-xxx		7.00	7.00	na	na	Includes DS-401 v5.2
	U	Viewlogic	Base		DS-VL-BAS-PC1	6.00			11/95	5.11	Update by request only
		Viewlogic	Standard		DS-VL-STD-xxx	6.00	6.00	6.00	11/95	5.11	
		Viewlogic	Advanced		DS-VL-ADV-xxx	7.00	7.00	7.00	na	na	
		Viewlogic/S	Base		DS-VLS-BAS-PC1	6.00			11/95	5.11	Includes PROSeries 6.1
		Viewlogic/S	Standard		DS-VLS-STD-PC1	6.00			11/95	5.11	Includes PROSeries 6.1
		Viewlogic/S	Extended		DS-VLS-EXT-PC1	6.00			11/95	5.11	Incl PROSeries 6.1/PROsynth 5.02X
		Viewllogic/S	Advanced		DS-VLS-ADV-PC1	7.00			na	na	
	U	3rd Party Alliance	Base		DS-3PA-BAS-xxx	6.00			na	na	
		3rd Party Alliance	Standard	FPGA/EPLD Core	DS-3PA-STD-xxx	6.00	5.20	5.20	na	5.10	Includes 502/550/380
		3rd Party Alliance	Advanced		DS-3PA-ADV-xxx	7.00	7.00	7.00	na	na	
	N	Foundation	Standard		DS-FND-STD-PC1	6.00			na	na	NewAldec software pkg v2.0
	N	Foundation	Standard VHDL		DS-FND-STV-PC1	6.00			na	na	NewAldec software pkg v2.0
	N	Foundation	Base		DS-FND-BAS-PC1	6.00			na	na	NewAldec software pkg v2.0
	N	Foundation	Base VHDL		DS-FND-BSV-PC1	6.00			na	na	NewAldec software pkg v2.0
	PR	XC4000E	Standard	XACT 5.2 Core + Synthesis	PR-MN8-STD- xxx-4E		1.00	1.00	na	na	By request only; Req In-wnty prod
	PR	XC4000E	Standard	XACT 5.2 Core + Synthesis	PR-OR-STD-xxx-4E	1.00			na	na	By request only; Req In-wnty prod
	PR	XC4000E	Standard	XACT 5.2 Core + Synthesis	PR-SY-STD-xxx-4E		1.00	1.00	na	na	By request only; Req In-wnty prod
	PR	XC4000E	Standard	XACT 5.2 Core + Synthesis	PR-VL-STD-xxx-4E	1.00	1.00	1.00	na	na	By request only; Req In-wnty prod
	N/PR	XC4000E	Standard	XACT 5.2 Core + Synthesis	PR-3PA-STD-xxx-4E	1.00	1.00	1.00	na	na	By request only; Req In-wnty prod
3RD PARTY PRODUCTION SOFTWARE VERSIONS		Aldec	Active-CAD	Entry & Simulation	na	2.00			na		
		Cadence	Composer	Schematic Entry	na		4.3.3	4.3.3	na	4.2.2	Design Kit V 5.1.1
		Cadence	Verilog	Simulation	na		2.1.2	2.1.2	na	2.0.5	Design Kit V 5.1.1
		Cadence (Valid)	Concept	Schematic Entry	na		1.7-P4	1.7-P4	na	1.6	Design Kit V 5.1.1
		Cadence (Valid)	Rapidsim	Simulation	na		4.2	4.2	na	4.1	Design Kit V 5.1.1
		Mentor	Design Architect	Schematic Entry	na		8.4	8.4	na	8.2_5	8.4 = A.4
		Mentor	QuickSim II	Simulation	na		8.4	8.4	na	8.2_5	8.4 = A.4
		OrCad	SDT 386+	Sche Entry	na	1.20			na		Capture support w/App Note
		OrCad	VST 386+	Simulation	na	1.20			na		VST 386+ only
		Synopsys	Dsgn/FPGA Comp.	Synthesis	na		3.3b	3.3b	na	3.3a	
		Viewlogic	ViewSynthesis	Synthesis	na	5.00	2.3	2.3	na	5.02X	
		Viewlogic	PROcapture	Schematic Entry	na	6.10	5.3	5.3	na		
		Viewlogic	PROsim	Simulation	na	6.10	5.3	5.3	na		
		Data I/O	ABEL Compiler	Entry & Simulation	na	6.1	6.0		na		
		Data I/O	Synario	Entry & Simulation	na	2.1			na		

KEY: *N=New Product, E= Engineering Software for in-warranty users by Request Only, U= Update by request only, PR = Pre-release requiring in-warranty status or Product Marketing apporval*

Introducing the XC4000EX FPGA Family

125,000 GATES

Xilinx Builds on the XC4000 Series to Extend FPGAs up to a Quarter of a Million Gates.

The XC4000 series, including the original XC4000, the XC4000E and now the XC4000EX family, is the ideal solution for high-density, high-performance FPGA needs. First introduced in 1991, the XC4000 series has become the world's most-popular FPGA family; in fact, if it were a free-standing entity, the XC4000 series would be the third largest programmable logic company in the world.

The new XC4000EX family extends the density and performance leadership of the XC4000 series to new levels. With devices up to 125,000 usable gates, the XC4000 series density range will overlap with the majority of gate array design starts. In addition to increased density, the XC4000EX family features architectural improvements that increase design ease, utilization and performance.

The XC4000EX family

The XC4000EX family will include seven members ranging from 28,000 to 125,000 logic gates. In a typical system application using on-chip memory, the maximum density rises to 250,000 gates *(see table 1)*. These devices are available in a variety of packages that are footprint compatible with the other members of the XC4000EX and XC4000E families. The XC4028EX is available now. The XC4036EX will be available in the first half of this year, with the XC4044EX, XC4052EX and XC4062EX following in the second half. The two largest devices, the XC4085 and XC40125, will be offered in 1997.

Continued on the next page

Table 1 - The XC4000EX family

	4028EX	4036EX	4044EX	4052EX	4062EX	4085EX	40125EX
Typical Logic Gates	28,000	36,000	44,000	52,000	62,000	85,000	125,000
Typical System Gates* (Logic + Select-RAM)	56K	72K	90K	110K	130K	175K	250K
Available RAM bits	32,768	41,472	51,200	61,952	73,728	100,352	157,968
CLB Array	32x32	36x36	40x40	44x44	48x48	56x56	68x68
CLBs	1,024	1,296	1,600	1,936	2,304	3,136	4,624
Flip-Flops	2,560	3,168	3,840	4,576	5,376	7,168	10,336
I/O	256	288	320	352	384	448	544
Packages:	HQ208 HQ240 PG299 HQ304 BG352	HQ304			*100% Footprint Compatible*		
		BG432 PG411	BG432 PG411	BG432 PG411 BG596	PG499 BG596	PG499 BG596	BG596

**30% of CLBs as RAM*

XILINX®

Continued from previous page

The XC4000E family is manufactured on a 0.6 micron (drawn) triple layer metal (TLM) process. The XC4000EX FPGAs are based on an advanced 0.5µ (drawn) TLM process. This new process enables both increased density and increased performance. The two primary determinants of silicon speed are feature size and interconnect delay. The 0.5µ gate length speeds transistor performance, while the silicon size decrease resulting from the smaller geometry dramatically reduces the size of the die, which, in turn, reduces interconnection delays.

The 0.5µ technology used for the XC4000EX devices will be replaced by a more advanced 0.35µ quad layer metal technology, planned for early 1997. This new technology will allow the manufacture of the two largest members of the XC4000EX family — the XC4085EX and XC40125EX. In addition, all family members will be redesigned in 1997 to leverage the 0.35µ technology, resulting in cost reductions and speed improvements.

Additional Routing Resources

Programmable logic is successful because it allows designers to achieve a faster time-to-volume than conventional approaches. For high density FPGA designs, device routability is a key factor; better routability enables faster design compilation times and boosts silicon utilization. As device densities increase, both the number of interconnections and the average length of interconnections increase. In order to effectively route designs of more than 100,000 gates, breakthroughs in interconnect topology were necessary.

The XC4000EX family features an enhanced interconnect scheme. As shown in **Figure 1**, the number of interconnect resources has increased substantially compared to the XC4000E and XC4000 architectures. Twelve "quad lines" are added both horizontally and vertically. The quad lines are interconnected by a buffered switch matrix that is spaced every four CLBs. Each buffered switch matrix contains both buffers and pass transistors. The place and route software will use the timing requirements of the design to determine whether it is optimal to use a buffer or pass transistor for each interconnect switch. Because of the buffered switch matrices, quad lines provide the fastest means for routing heavily loaded signals over long distances.

In addition to the quad lines, the number of vertical long lines has increased from six to 10. Buffered programmable splitters are added to these long lines at positions 1/4, 1/2 and 3/4 of the way across the chip. Due to the buffering, XC4000EX long line performance does not deteriorate with larger array sizes. If a long line is split, the resulting partial long lines are independent. The number of global lines also was doubled from four to eight, as described below.

The XC4000EX architecture also offers direct connects that allow efficient and fast connections between adjacent CLBs. These nets allow high-speed data flow from CLB to CLB. Signals routed on the direct connects exhibit minimum interconnect propagation delay and use no general routing resources. Direct connects are ideal for creating sophisticated, high-speed macros.

The XC4000EX devices have additional VersaRing™ routing around the perimeter

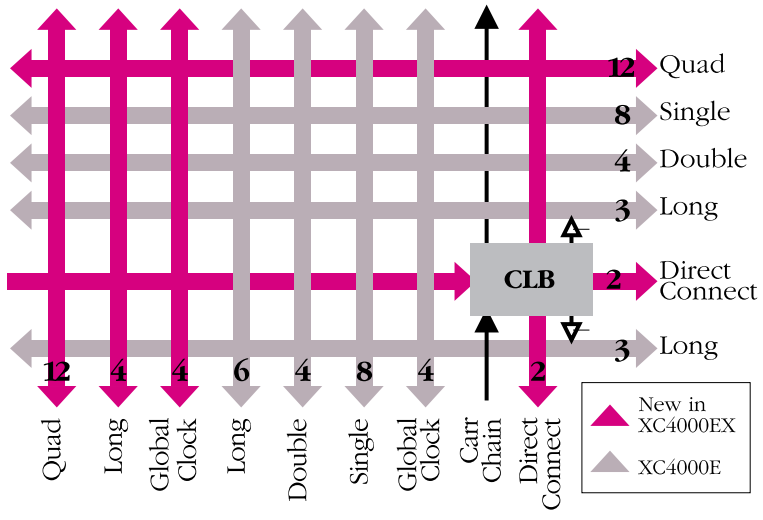


Figure 1 - XC4000EX Interconnect

of the CLB array. The VersaRing feature, first introduced with the XC5000 series, facilitates pin-swapping and redesign without affecting board layout. It avoids the trade-off of high utilization versus pin assignment flexibility by allowing both.

Global Nets and Buffers

Global nets and buffers are the primary mechanism for distributing clocks and other high fanout control signals throughout a device. The buffers accept signals that are generated on-chip or externally and drive them onto the global nets. The XC4000EX device has three types of global buffers.

- **Global Low-Skew Buffers** - similar to those found on the XC4000, XC4000E and many other devices. The buffers are designed to deliver a low-skew clock signal to the entire chip, and are used for most internal clocking. They must be used when a single clock needs to drive the entire chip. Each XC4000EX device contains eight Global Low-Skew Buffers.
- **Global Early Buffers** - provide faster clock access than Global Low-Skew Buffers, but have a limited distribution capability. Each buffer can only supply a clock signal to 1/4 of the CLBs and 1/4 or 3/8 of the IOBs. Each XC4000EX device contains eight Global Early Buffers.
- **FastCLK™ Buffers** - specifically designed to provide the fastest possible I/O clocks. The only access they have to CLBs is through local interconnect. Using the FastCLK buffers enables near 100 MHz chip-to-chip communication. Each XC4000EX device contains four FastCLK Buffers.

Figure 2 shows the portion of a device that can be driven in a typical application by the three buffer types. Global Low-Skew and Global Early Buffers can drive any of eight vertical long lines in each column. These long lines are separate from the vertical long lines used for standard interconnect.

Development System Support

Software is the key enabling technology for maximizing the power, flexibility, and performance capabilities of the XC4000EX. Xilinx and its Alliance Partners are fully-prepared to support the XC4000EX with the industry's most powerful and versatile suite of design tools. Support for HDL-based, ASIC-like design methodologies is a key part of this strategy.

The recent merger of Xilinx and NeoCad provided a unique opportunity to combine the best software elements from the two companies. The merger took place during the development of the XC4000EX. A software tool, the FPGA Architect, developed by NeoCad, was used to evaluate design trade-offs and maximize the ultimate performance and routability of the devices.

In summary, the new XC4000EX family extends the capacity, performance and system-integration capabilities of the popular XC4000 FPGA series to unprecedented levels. Both advanced processing technology and architectural enhancements have contributed to these dramatic improvements. The XC4000EX FPGA is the ideal logic device for high-density, high-performance applications. ◆

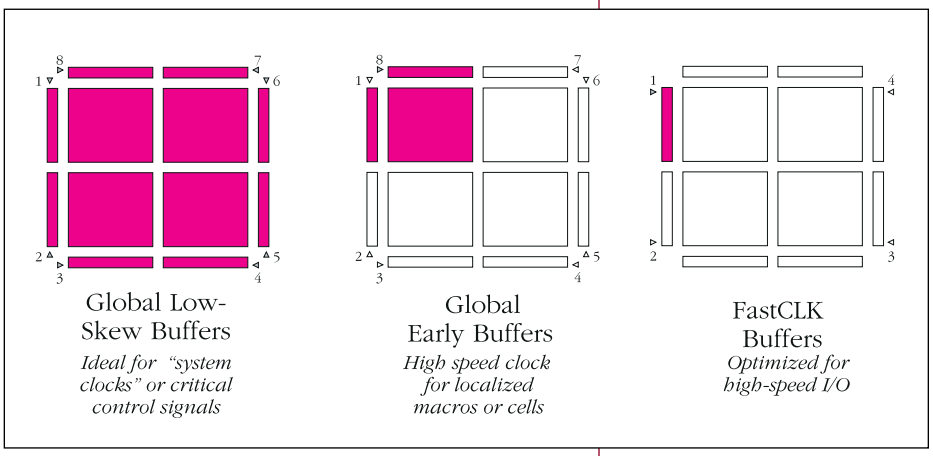


Figure 2 - XC4000EX Clocking options (shaded area indicates reach of a typical single buffer)

Designing with XC9500 CPLDs — *First In-System*

XC9500 CPLDs are the first in-system programmable (ISP) devices based on 5 V flash technology. The XC9500 architectural features enhance ISP by permitting design changes without altering pin assignments.

The powerful XC9500 architecture supports a wide variety of design methodologies. Each function block and macrocell is identical. This assists the designer when using HDLs, synthesis and/or schematic capture tools by allowing the software to fit and route the design quickly and efficiently.

The XC9500 family allows easy migration across multiple density options in a given package footprint. Designs initially targeted at a small part can be migrated into a larger part. This capability helps designs maintain their pin assignments if additional logic capacity is needed in a socket already committed to a printed circuit board.

The design software also incorporates a number of strategies permitting future edits without altering pinouts. The *XC9500 Application Guide* outlines many of these architectural features and software strategies.

Macrocells

Understanding the macrocell and interconnect capability is key to designing with XC9500 CPLDs. Detailed knowledge is not required, but general facts are helpful.

The XC9500 macrocell performs most logic functions at the bit level in a single macrocell. Counters, shifters, multiplexers and decoders require a single macrocell to perform one bit of corresponding function. Adding and subtracting functions generally require two macrocells per bit. Parity can be calculated over four bits in one macrocell. The design software automatically implements appropriate mapping and optimization.

Product terms are automatically distributed among macrocells. Any macrocell easily receives up to 15 product terms with additional product terms delivered from local neighboring macrocells. There are few logic functions needing more than 25 product terms. However, up to 90 product terms can be assigned to a

Low Voltage Product Line Expands

Xilinx Announces First 3 V PCI and CardBus Compliant Devices

Xilinx has significantly expanded its product offerings for 3.3 V systems with the introduction of the XC3100L and XC4000L FPGA families. These new product offerings include more than 30 combinations of device, speed, and package, tripling the size of the Xilinx 3 V FPGA product line. Engineering samples are available now, with full production scheduled for the second quarter of this year.

XC3100L FPGAs, the highest-performance 3 V FPGAs available today, are architecturally and functionally identical to the XC3100A family. Family members include the XC3142L and XC3190L. The -2 speed grade of the XC3100L is the first 3 V PCI *and* CardBus compliant programmable logic device. The XC3100L family is targeted towards speed-sensitive, low-voltage applications such as PC-Card modems and video peripherals.

The XC4000L family offers the broadest density range of any 3 V FPGA product family, ranging from 5,000 gates to an industry-leading 13,000 gates. Family members include the XC4005L, XC4010L and XC4013L devices. The XC4000L FPGAs have all the

n Programmable Devices Based on 5-V Flash Technology

macrocell within a particular function block. The XACT*step*™ design software handles the details of product term assignment.

In-System Programming

XC9500 devices are programmed in-system via an IEEE 1149.1 standard 4-pin JTAG protocol. Multiple XC9500 CPLDs as well as other JTAG-compatible devices (such as XC4000E and XC5200 FPGAs) can be linked together in the same JTAG chain. In-system programming offers quick and efficient design iterations and eliminates package handling. Once designs are compiled, their configuration patterns are downloaded automatically using the EZTAG download software. Users need only provide the JTAG chain ordering sequence to the software that targets the specific CPLD being programmed.

All XC9500 CPLDs are in-system programmable for at least 10,000 program/erase cycles. In addition, the JTAG downloading and programming circuitry is the most comprehensive and advanced available today. Each XC9500 device supports EXTEST, SAMPLE/PRELOAD, BYPASS, USERCODE, INTEST, IDCODE, and HIGHZ instructions. All in-system programming, erase and verify instructions fully comply with extensions of the IEEE 1149.1 boundary-scan.

The XC9500 family supports **mixed voltage systems** combining both 3.3 V and 5 V components. XC9500 CPLDs can implement both logic and level shifting functions in a single programmable device. This eliminates the need for discrete level translation buffers.

The XC9500 family also includes **User Programmable Ground** for internal signal management. User Programmable Ground allows the device I/O pins to be configured as additional ground pins. Tying programmable ground pins to the external ground connection reduces system noise.

"The XC9500 family offers a superior high-performance, general-purpose logic integration solution."

Superior Performance

These additional features enhance the overall electrical capabilities of this new family, relieving designers of many critical signal management responsibilities.

In summary, the XC9500 family offers a superior high-performance, general-purpose logic integration solution. The powerful CPLD architecture expands in-system programming capabilities with the industry's most comprehensive JTAG support. The architecture also permits design changes without altering pin assignments. ◆

architectural features of the XC4000E family, including Select-RAM™ memory.

These low-voltage FPGA products are bitstream compatible with their 5 V counterparts; designers can use the current XACT*step* v6 and XACT 5.2 development systems to design with these new devices.

While in the past 3 V designs have been limited mostly to laptop computer and cellular telephone applications, there now is a significant increase in design activity in the mainstream telecommunications, data communications and instrumentation markets The expansion of the 3 V FPGA product line addresses this growing market. *Please contact your local Xilinx representative for the latest availability information.* ◆

Device	Speed Grades	Eng. Samples	Limited Production	Volume Production	Package Availability
XC3142L	-2/-3	Now	March	2Q 96	PC84, VQ100, TQ144
XC3190L	-2/-3	Now	March	2Q 96	PC84, TQ144, TQ176
XC4005L	-5/-6	Now	March	2Q 96	PC84, PQ208
XC4010L	-5/-6	Now	March	2Q 96	PC84, TQ176, PQ208
XC4013L	-5/-6	Now	March	2Q 96	PQ208, PQ240, BG225

XC4000E in Volume Production

New -2 Speed Grades Sampling! Software Shipping Today!

The XC4000E family has entered full-volume production. Xilinx is now able to satisfy the rapidly growing demand for the industry's highest-performance, full-featured FPGA.

Production volumes of the -5, -4, and -3 speed grades are available, and sampling has begun for the fastest speed grade, the -2. The new -2 speed grade propels the XC4000E to a higher than 60 MHz typical system speed and, like the -3 speed grade, is fully PCI compliant.

The XC4000E software began shipping in January. This XACT-Development™ software update provides access to all the advanced features of the XC4000E architecture, including the Select-RAM™ memory and the I/O clock enables. It will be shipped free of charge to current in-warranty customers upon request. Contact your local Xilinx sale representative or call Customer Service at 408-559-7778.

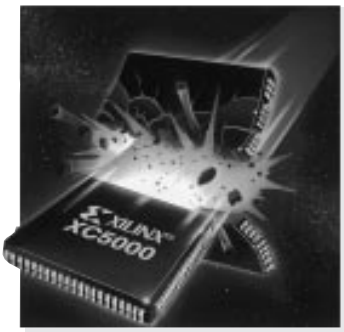
XC4000E users can take full advantage of this advanced FPGA architecture to accelerate their time-to-market through the use of the new Xilinx LogiCore™ modules. The inaugural LogiCore module is a fully verified PCI interface based on the XC4000E architecture. *(See page 27.)* ◆

DSP Application Design Contest!

Would you like to see your name in print? Would you like to win a Xilinx XC4000E t-shirt *and* either a CD-ROM drive with the lastest Xilinx Development Software Package, a multimedia board (and speakers) for your PC, or one of several other prizes? Xilinx is looking for the five most innovative XC4000E-based DSP designs using XC4000E/XC4000EX Select-RAM™ memory. Xilinx will judge all entries received by May 30. The winning design ideas will be featured in the 3Q96 edition of *XCELL*. So what's the catch? You must be willing to allow Xilinx to print and share your design idea with other designers, and promise to wear your Xilinx t-shirt with pride.

If you need some ideas to get started, check out our DSP application notes on our World Wide Web site (http:/www.xilinx.com).

Send your schematic drawings, a diskette with your XC4000E/EX design files, and any other relevant documentation to: **Xilinx DSP Designer Challenge,** Xilinx Product Marketing, 2100 Logic Drive, San Jose, CA 95124 USA For more information, email inquiries to dsp@xilinx.com or fax them to 408-879-4442, ATTN: DSP Design Challenge. ◆



XC5200 Family on Record Pace

XC5200 FPGA family revenue for the third fiscal quarter (ended December 30, 1995) increased by more than 150% from the previous quarter — the fastest ramp up of any new product in Xilinx history. The XC5200 family already is being used in hundreds of high-volume applications, including communications, data processing, networking and industrial systems.

The XC5200 family's unprecedented success results from a cost-optimized design that takes full advantage of a 0.6µ three-layer-metal SRAM process technology and architectural innovations such as the VersaRing™ I/O interface. The XC5200 family includes five members, ranging from 2,000 to 18,000 usable gates. The devices are offered in 15 different packages, with more than 100 different device/package/speed combinations. ◆

PCI Interface is First New LogiCore™ Module

MEMBER PCI LOCAL BUS SPECIAL INTEREST GROUP

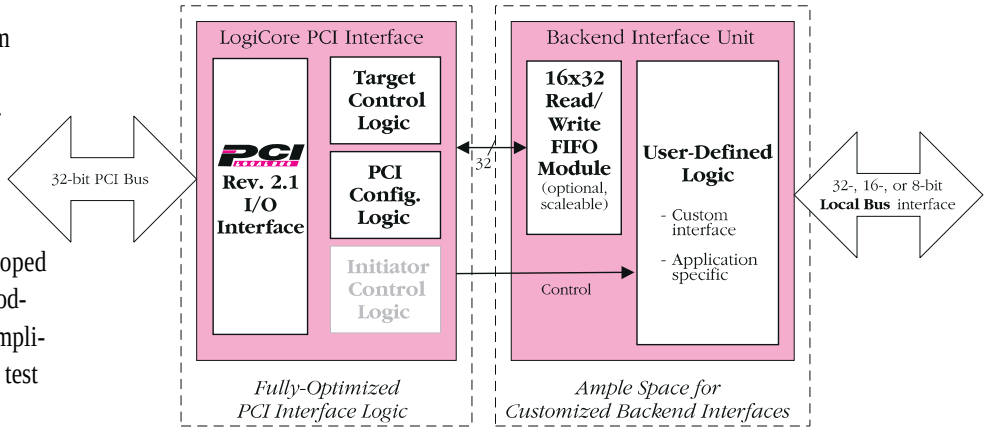
To date, integrating a PCI interface into an FPGA or ASIC device has been a difficult challenge, often requiring months to learn the PCI specification and to optimize and verify the design. With LogiCore modules, Xilinx is doing the tough work for you (now for PCI, to be followed soon by several other applications).

The LogiCore program supplies pre-implemented "drop-in modules" for Xilinx FPGA designs. As a result, users can slash development time, reduce design risk, and obtain optimal performance for their FPGA designs. Since LogiCore modules have predefined implementations and are already fully-verified, designers can focus their time and energy on their unique system functions.

The first LogiCore module is a fully-compliant, 32-bit PCI interface for the XC4000E FPGA family. It has predefined mapping, relative placement and timing specifications. Jointly developed by Xilinx and HighGate Design, the module has been verified using the PCI-compliant test bench from Virtual Chips. This test bench is approved by the PCI Special Interest Group (PCISIG) and simulates all possible signaling on a PCI bus. Furthermore, 30 designers have beta tested the module, and 17 PCI board designs have been completed using the beta version.

"We chose Xilinx modules because they're fully verified," noted Brian Warren, senior design engineer at Delco Electronics. "The module we used worked the first time, saved us more than six months in development time, and allowed us to focus our resources on our system design." Warren, one of the beta-site users of the module, has designed a Digital Audio Broadcast (DAB) transceiver that includes a RISC processor and Xilinx XC6200 and XC4013 FPGA devices.

As shown in the diagram, the LogiCore PCI module is partitioned into five major blocks. In addition to the PCI interface, configuration and control logic, the module includes a FIFO buffer and a simple, general-purpose interface to the user's back-end logic. The FIFO buffer uses the Select-RAM™ memory feature of the XC4000E to support burst transfers at the maximum bus speed. The schematic-based module can be easily customized to meet the user's needs. When implemented in an XC4013E FPGA, more than 7,000 programmable gates remain free for integration of the unique, back-end functions of the application. This is a high-performance, one-chip solution.



LogiCore PCI module block diagram

The LogiCore PCI interface is available with target functionality today, and will be updated with full initiator/target functionality in March. *(Contact your local Xilinx representative for ordering information.)*

Coming Attractions

The LogiCore PCI interface is just the first of a planned series of vertical solu-

See LOGICORE, page 32

XILINX®

XABEL-CPLD Software Available NOW!

XABEL-CPLD software is available **now** for immediate ordering and delivery!

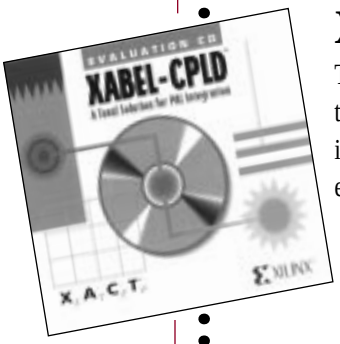
XABEL-CPLD is the new Xilinx development system designed for PAL and CPLD users. With this completely self-contained system, PC-based customers can quickly and easily integrate their logic into Xilinx CPLDs using the industry-standard ABEL hardware description language.

This new design software combines the well-known, windows-based Data I/O ABEL6 front-end with the new Xilinx XACT*step*™ v6 core software; the result is an extremely easy-to-use, industry-standard user interface capable of targeting Xilinx CPLDs.

Designed for the PC and priced at only $495, XABEL-CPLD is the perfect software solution for users familiar with ABEL, PALASM, CUPL and MACHXL who design with PALs and CPLDs.

Features

- Familiar Data I/O ABEL, Windows-based environment for design entry, simulation and fitting.
- Industry-standard ABEL-HDL supports state machines, high level logic descriptions, truth tables and equation entry.
- Hierarchical design entry and JEDEC file conversion for integration of existing PALs into Xilinx CPLDs.
- Functional simulation with graphical waveform viewer and static timing reports
- Advanced XACT*step* v6 fitter with fully automatic device selection, multiple pass optimization, partitioning and mapping, and timing-driven fitting.
- On-line tutorial and on-line help reduces learning curve. ◆



XABEL-CPLD Evaluation CD-ROM Available

The XABEL-CPLD software offers a truly accurate method for evaluating the performance, power, board real estate and cost savings gained by integrating multiple PALs into a single Xilinx XC7000 CPLD device. Simply enter the design and the evaluation software does the rest.

To obtain an evaluation CD, contact your local Xilinx sales representative or distributor. You also can request a CD from the Xilinx WebLINX web page (www.xilinx.com). ◆

XC8100 Family Adds Schematic Support

XSACETP

Production version 1.1 of XACT*step* Series 8000 is now available. This release adds support for the PC platform and the use of Viewlogic's ProCapture and Mentor's Design Architect schematic editors for XC8100 FPGA design.

As a result, schematic-based designs can now access the advanced features of the XC8100 FPGA family:

- Extremely high design security
- Near 100% utilization regardless of logic type
- Abundant routing resources
- Internal 3-state buffers
- Pin-locking tolerance
- Footprint compatibility with XC4000 and XC5200 FPGAs

New XC7000 Core Software in XACT*step* v6

The Xilinx XC7000 core software delivered in XACT*step* v6 contains new features and enhancements of existing features that address user productivity and design performance for Xilinx CPLD designs.

Productivity Improvements

Automatic Device Selection - The software automatically implements the design in the smallest device possible using device type, package type and speed constraints entered by the designer

XACT-Performance™ - Timing-driven optimization collapses logic to meet user-specified critical timing requirements.

Static Timing Analyzer - Provides a complete pin-to-pin timing report of the design, including detailed internal path analysis

Performance Improvements

New Design Optimization Algorithms - New design optimization and partitioning algorithms better utilize the XC7300 architecture *without user intervention*. Designs fit in smaller devices, take about 10% fewer macrocells and run about 10% faster than before.

Multiple-Pass Optimization, Partitioning and Mapping - The software will try a different optimization and partitioning strategy if necessary to achieve a first-time fit, *without user intervention.*

Schematic and VHDL Design Entry

Xilinx provides an open design environment that allows designers to choose from a variety of schematic entry, VHDL synthesizer and simulation tools, such as those from OrCAD, Viewlogic, Mentor Graphics, Exemplar and Synopsys. When combined with the appropriate library and interface software, XACT*step* v6 provides a complete environment for the processing of Xilinx XC7000 CPLD designs

ABEL-HDL Entry

XABEL owners can continue to embed macros in their schematics or enter complete chip designs for the XC7000 family and use XACT*step* v6 to complete the design implementation. This core software is included in the new Xilinx XABEL-CPLD package, a complete ABEL-HDL based tool designed specifically for PAL users who want to use Xilinx XC7000 CPLDs.

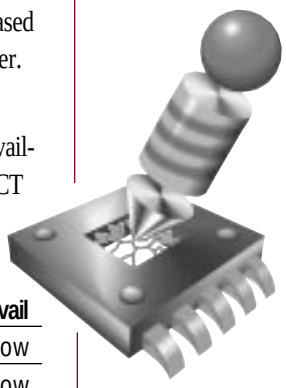
Embedded Third Party Compilers

Xilinx licenses its fitter technology to third-party development tool vendors, giving you the flexibility and versatility of industry-standard design software environments with the speed, density and routability of Xilinx CPLDs. The Xilinx CPLD fitter is fully integrated into the Data-I/O Synario, Logical Devices CUPL and IsDATA LOGiC environments. For price and availability of the XACT*step* v6 based fitter, contact the development tool manufacturer.

Product Availability and Pricing

The XC7000 XACT*step* v6 core software is available on the PC for immediate delivery. The XACT 5.2 core software is available for workstation platforms. ◆

Part Number	Version	Platform	Pricing	Avail
DS-550-PC1-C	6.0	PC	$89.95	Now
DS-550-SN2-C	5.2	Sun	$995	Now
DS-550-HP7-C	5.2	HP	$995	Now



The table summarizes the supported CAE interfaces. Many other third-party CAE vendors are working on XC8100 solutions that will be released in the first half of 1996.

Now Runs on PC — Version 1.1 adds PC support (DS-8000-STD-PC1-C or DS-8000-EXT-PC1-C). It runs under Windows 3.1, Windows 95 and Windows NT. The CAE interfaces available on the PC include Viewlogic and Exemplar. Workstation versions are available for SunOS, Solaris, HPPA, and RS6000 platforms. ◆

CAE Tools Supporting XC8100 FPGA Design

Schematic	Synthesis	Simulation	Timing Analysis
Viewlogic ProCapture	Synopsys Design Compiler	Synopsys VSS	Synopsys
Mentor Design Architect	Synopsys FPGA Compiler	Cadence Verilog	Motive
	Viewlogic ViewSynthesis	Viewlogic ViewSim	Mentor QuickPath
	Mentor Autologic I, II	Mentor QuickSim	Cadence Veritime
	Exemplar	Mentor QuickVHDL	
		Model Tech	
		VITAL VHDL	

PowerGuide™

Innovative Approach to Incremental Design for the XC8100 Family

Incremental design support (also known as "re-entrant design") is a key feature of today's FPGA implementation tools. Often, minor changes are required near the end of a design cycle to fix last-minute bugs or respond to a change in specifications. The design of large, complex systems can be simplified by first implementing a small portion of the design and then iteratively adding other modules to it. Both these situations require tools that support incremental design techniques.

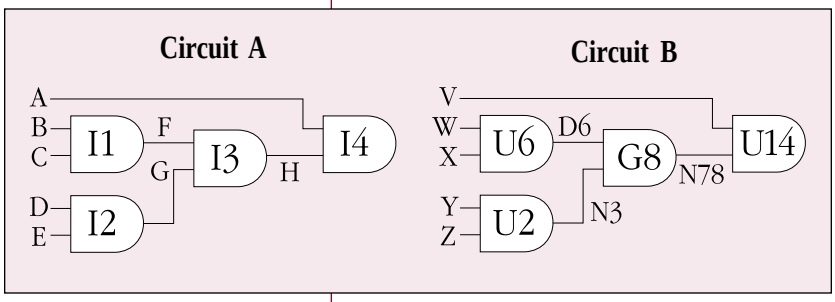


Figure 1

Incremental design techniques involve using a previous implementation of a design as a guide to the placement and routing of a new version of that design. Where the two designs match, the newer design mimics the old one exactly, preserving its placement and routing, and, therefore, its timing characteristics. For example, suppose a large design has been successfully implemented and tested. A small change is then required. By using the "guide" option, the majority of the placement and routing will remain unchanged, so only the relatively small, altered portion of the design needs to be re-implemented and re-tested. With this technique, minor changes can be implemented and verified in a matter of a few minutes. This capability has been a valued feature of the XACT*step* tools supporting the Xilinx FPGA families.

The XACT*step* Series 8000 development system for the XC8100 FPGA family further advances the state-of-the-art for incremental design support. Conventional FPGA guided placement and routing algorithms match cells and nets using the cell instance and net names. This approach breaks down when used with logic synthesis tools, as synthesis tools assign instance and net names arbitrarily during the synthesis process. A small change in a design's source code can result in different symbolic names for the majority of cells and nets in the final design netlist. XACT*step* Series 8000 PowerGuide feature is the first and only FPGA guide option that enables incremental and iterative design for HDL-based designs. PowerGuide accomplishes this by using a nameless correlation algorithm.

Instead of using instance and net names, PowerGuide uses the design's topology to perform guide matching. Compare the two circuits above (Circuit A and Circuit B). A conventional guide algorithm does not match any cells or nets between the two circuits, since the instance and net names are different between the two circuits. The PowerGuide algorithm matches all cells and nets between the two circuits, since the two circuits have identical topology.

For example, suppose a 3,000 gate VHDL design is synthesized with the Synopsys FPGA Compiler. All synthesis options are set to their default values. An area constraint of zero is applied to the design. (This constraint produces minimum area in Synopsys.) A portion of the VHDL gate-level netlist is shown at the top of the next page, and the circuit is diagrammed in **Figure 1**, left.

Continued from the previous page

```
U3053:        BUFGP port map( O => n10123, I => OSC);
byteptr_reg:  FDC port map( Q => byteptr, D => n10802, C =>
              n10123, CLR => n9602);
U3571 :       M2_1B1B port map( O => n10802, D1 => byteptr, D0 =>
              n10651, S0 => n10251);
```

The VHDL design is then modified to add an inverter to an input port named DACK7_N. The port is renamed DACK7 to show the change in signal sense from active low to active high. This modified VHDL design is also synthesized with Synopsys FPGA Compiler. The same options and constraints are used with this modified design as was used with the original design. A portion of the new VHDL netlist is shown below; this netlist shows the same gates and nets as the previous code, but changes in the synthesized code are highlighted. The circuit is shown in **Figure 2.**

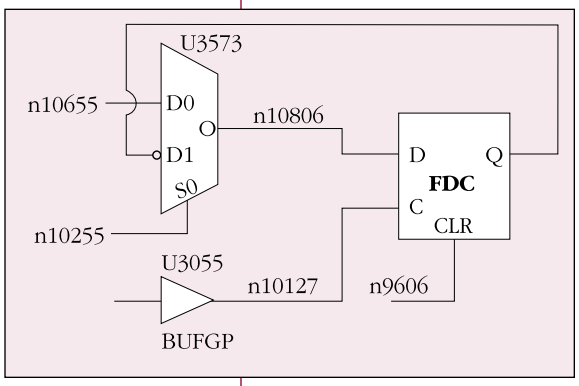


Figure 2

```
U3055:        BUFGP port map( O => n10127, I => OSC);
byteptr_reg:  FDC port map( Q => byteptr, D => n10806,
              C => n10127, CLR => n9606);
U3573:        M2_1B1B port map( O => n10806, D1 => byteptr,
              D0 => n10655, S0 => n10255);
```

The instance names for all combinational cells have changed from the guide netlist to the modified netlist. The names of all nets except the flip-flop output nets have also changed. If the guide algorithm relied on instance names and net names to match these cells, then the guide algorithm would not match any of these cells.

Shown below is the PowerGuide correlation report for this modified design. This report is generated when the guide design is read into the Series 8000 software. (To read a guide design into XACT8000, select “Guide” from the Place/Route menu.)

```
Reading guide design from file “guide.xb”
Comparing net-lists ...
                    :     Nets       CLCs       Pads       Misc
-------------------------------------------------------------------
design              :      861       1029         70          0
guide               :      861       1029         70          0
-------------------------------------------------------------------
correlation         :     861(100%) 1026(99%)     70(100%)     0
```

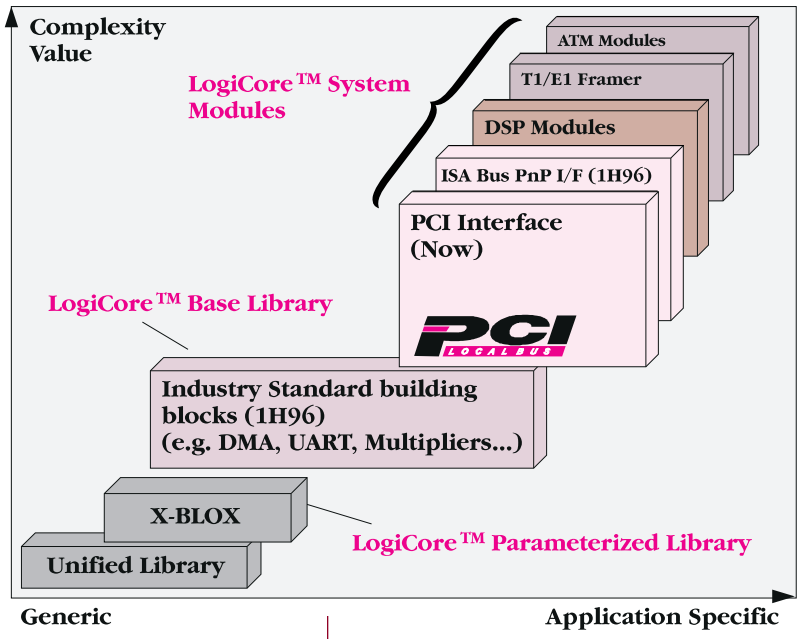
In the report above, all but three CLCs match. These three CLCs comprise a two-input multiplexer cell (1 CLC) and a six-input sum-of-products cell (2 CLCs). The inverter that was added to the DACK7 input pin in the modified VHDL source file is optimized to a bubble on an input pin on both the multiplexer and the sum-of-products. All nets are correlated between the guide design and the modified design. All I/O pads are also matched between the guide design and the modified design, including the input pin with the changed name (DACK7). Again, this result is obtained because the PowerGuide feature does not use instance or net names for the guide matching.

In summary, Series 8000 PowerGuide uses the topology of the design to match instances and cells, enabling users to fully utilize incremental and iterative design methodologies for HDL-based designs. The PowerGuide feature allows the user to make design changes without having to re-verify timing on the entire design, as well as providing fast place and route times on successive iterations — features previously available only to schematic designers. ◆

LogiCore

Continued from page 27

tions from Xilinx. Several LogiCore system modules are in development, including an ISA bus plug and play interface, DSP building blocks, and ATM modules. In addition to these high-complexity system modules, a collection of medium-sized, industry-standard building blocks will be available in the LogiCore base library. When released this spring, this library will include functions such as DMA controllers, UARTs, multipliers and FIFOs. All the modules are pre-defined, drop-in solutions that maximize utilization and performance, and accelerate time-to-market.



Along with the LogiCore products created and distributed by Xilinx, we will work with third-party intellectual property providers. In order to grow the number of available modules rapidly, Xilinx has initiated the **LogiCore Partners Program**. This program will access existing industry expertise to encourage the creation of a wide range of high-quality FPGA building blocks from third-party vendors. Xilinx will work closely with the LogiCore partners to verify the quality of LogiCore modules. The table below lists the intial members of the program.

Xilinx is the first FPGA vendor to provide pre-designed, fully-verified drop-in modules. By allowing you to focus your time and effort on your system design, these modules can help you save months in development time for your high-performance, high-density systems.

For further information about the LogiCore PCI interface or other modules in the program, please contact your local Xilinx representative or visit the LogiCore section of WebLINX, Xilinx's World Wide Web site (http://www.xilinx.com). ◆

LOGICORE PARTNERS

Company	Application areas of expertise
3Soft Corporation (CA)	Industry standard functions
Comit Systems (CA)	Communication, DSP
CoreEl MicroSystems (CA)	ATM, Sonet
Logic Innovations (CA)	PCI Bus Models, Set Top Box Technologies
Rice Electronics (MO)	Digital Signal Processing (DSP), Image Processing
SAND Electronics (CA)	Bus Interfaces (PCI, ISA, PCMCIA, CardBus)
Sierra Research and Technology (CA)	ATM, 100MB Ethernet, CPU Cores
Toucan Technology (Ireland)	Bus Interfaces including PCI, Telecom
VAutomation (NH)	Micro Processors, Embedded Systems, Communications
Virtual Chips (CA)	PCI, PCMCIA/CardBus, USB, ATM

Selecting a Xilinx Product Family

Programmable logic users enjoy a wealth of choices when selecting CPLD and FPGA devices from Xilinx. A quick guide to the broadest line of product offerings in the industry follows.

Type of Logic Functions

All Xilinx devices are general-purpose in nature. Any family can implement any type of logic. There are, however, some features that make certain families more applicable than others for certain logic functions. These eight items should be interpreted as 'soft' suggestions, not as absolute, unequivocal choices.

- *For shortest pin-to-pin delays and fastest flip-flops:* Use XC7300, XC9500 or, if fan-in is sufficient, XC3100A, XC4000E/EX
- *For fastest state machines:* For encoded state machines, use XC7300, XC9500. For "one-hot" state machines, use XC3100A, XC4000E/EX, XC5200, XC8100
- *For fast counters/adders/subtractors/accumulators/comparators:* Use XC4000E/EX, XC5200 or XC7300. Use XC3100A for very fast, but short or simple counters.
- *For I/O -intensive applications with a high ratio of I/O to gates:* Use XC5200
- *For shortest design compilation time:* Use XC7300, XC9500, or XC8100
- *For lowest cost per gate, when on-chip RAM is not required:* Use XC5200, XC3100A
- *For pin-out compatibility within and between families, allowing easy migration to different device sizes in the same package (sometimes even between families), thus maintaining an existing pc-board layout:* Use XC4000E/EX, XC5200, XC8100, XC9500
- *For Digital Signal Processing (multiply-accumulate) applications:* Use XC4000E/EX

Specific Functions and Characteristics

Specific features/characteristics available only in the listed families. These are "hard" selection criteria.

1. *For on-chip RAM:* Use XC4000E, XC4000EX, or XC6200.
2. *For on-chip bidirectional bussing:* Use XC3000A, XC4000, XC5200, XC7300, XC9500, XC8100 (i.e. use any Xilinx family except XC2000). XC3000, XC4000 and XC5000 FPGA families have horizontal long lines that can be driven by internal 3-state drivers; XC8100 FPGAs use internal 3-state drivers on arbitrarily defined interconnects; XC7300 and XC9500 CPLD devices implement busses indirectly using their Universal Interconnect Matrix™.
3. *For on-chip crystal oscillator circuitry:* Use XC3000A, XC3100A.
4. *For very fast or partial reconfiguration, and for a dedicated microprocessor interface:* Use XC6200.
5. *For non-volatile single-chip solutions:* Use XC7300, XC9500, XC8100 or any HardWire™ device.
6. *For lowest possible static power consumption at 5 V:* Use XC3000A, XC8100 and, to a lesser extent, XC5200, XC4000E, XC4000EX.
7. *For JTAG boundary scan test support:* Use XC4000E, XC4000EX, XC5200, XC8100, XC9500 .
8. *For rail-to-rail output voltage swing at 5 V V_{CC}:* Use XC3000A, XC3100A, XC4000E, XC4000EX, XC5200, XC6200, XC8100 (in XC4000E/EX, rail-to-rail is a user-option).
9. *For 3.3-V operation:* Use XC3000L, XC4000L, XC4000XL, XC8100.
10. *For 5-V operation interfacing with 3.3 V devices:* Use XC7300, XC9500 or XC4000E/EX. (Any XC4000E/EX 'totem-pole' output drives 3.3 V inputs safely, and the TTL-like input threshold can be driven from 3.3 V logic.)
11. *For in-system programmability:* Use all Xilinx families except XC7300 and XC8100.
12. *For PCI-compatibility:* Use XC4000E/EX, XC3100A, XC3100L, XC7300, XC9500
13. *For hi-rel, military or mil temperature-range applications:* Use XC3100A, XC4003, XC4005, XC4010, XC4013.
14. *For battery-operated applications requiring low stand-by current:* Use XC3000A, XC4000E/EX, XC8100.
15. *For best protection against illegal copying of a design (design security):* Use XC8100, XC7300, XC9500 with security bit activated. *For powerdown battery-backed-up configuration:* Use XC3000A, XC3000L.

XILINX®

JTAG Support in the XC9500 CPLD Family

The new XC9500 family of CPLDs can mitigate the effects of rapidly rising testing costs for loaded PC boards by simplifying the manufacturing process. Caused by the increasing complexity of IC's and the use of packaging technologies that restrict access to interconnections, along with the handling requirements of most complex programmable logic devices, increased testing costs have been a significant challenge to manufacturers.

The XC9500 family allows you to automatically program and test multiple devices and PC boards in-system, using the industry standard JTAG interface. This greatly simplifies the production, test, and maintenance of complex systems. With this capability you can even make engineering changes to CPLDs on your production boards in the field, and those changes can be fully verified.

The XC9500 CPLD family simplifies testing because you can use software to verify the functionality of devices and their interconnections; complex and expensive PC board test/probing systems are no longer required. Device handling problems are also minimized since XC9500 devices are programmed in-system, alleviating the lead integrity problems associated with external programming methods. The XC9500 family includes seven devices that range from 800 to 6,400 equivalent gates, with pin-to-pin delays as fast as 5 ns.

JTAG Overview

JTAG, also known as IEEE Standard 1149.1, uses a simple 4-wire interface known as the Test Access Port (TAP) to access a boundary scan serial shift register and control logic embedded within a device. Each XC9500 I/O pin is connected to one stage of the boundary scan shift register, allowing the pin to be stimulated and sampled. Output sampling can even occur during normal device operation. By shifting in a test stimulus and instructions,

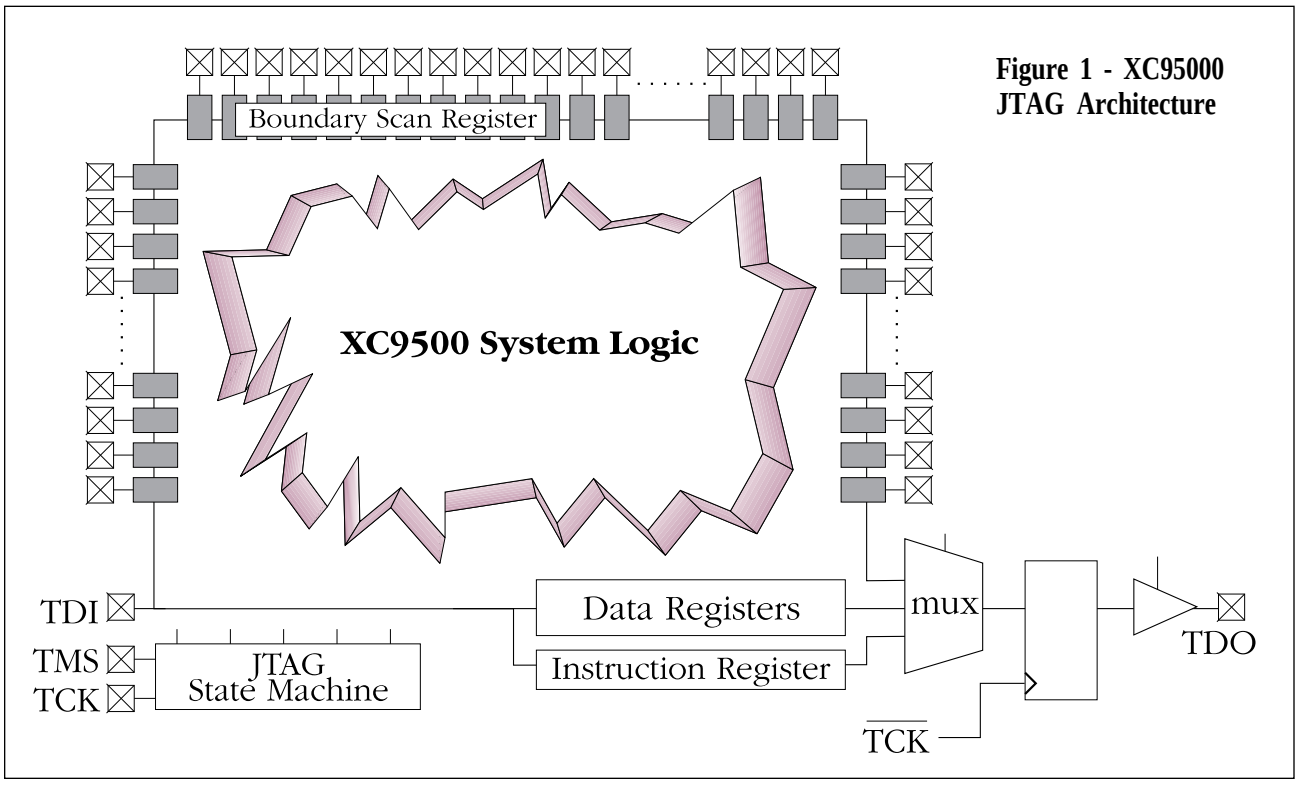


Figure 1 - XC95000 JTAG Architecture

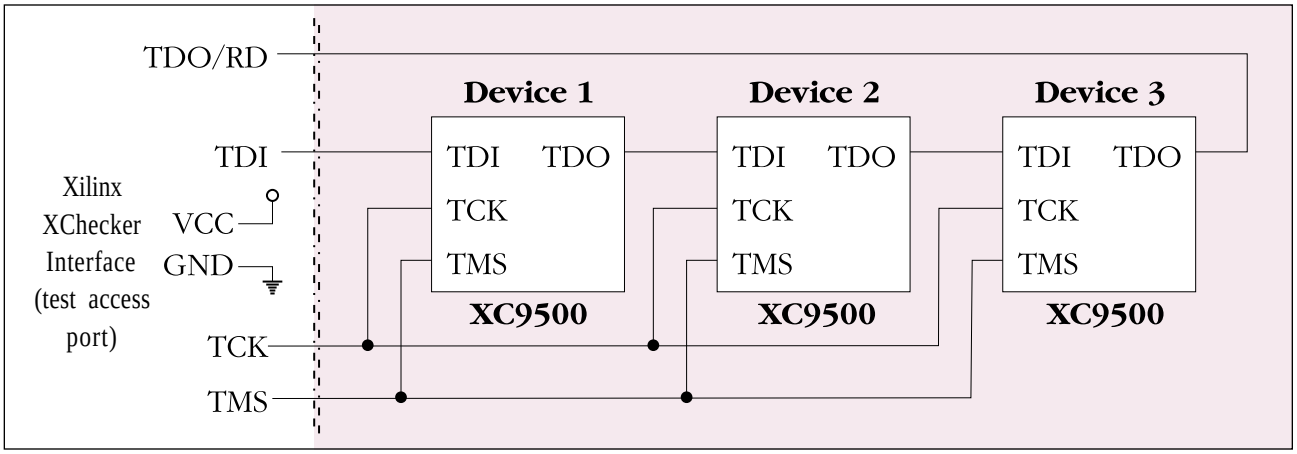


Figure 2 - Daisy Chain Operation

and then shifting out the result, you can effectively and automatically test devices and their interconnections on a PC board.

Figure 1 shows the XC9500 JTAG architecture. JTAG allows multiple devices to be daisy-chained and accessed via the TAP. This simplifies board layout, minimizes hardware overhead and reduces test software requirements. **Figure 2** illustrates a typical daisy-chain arrangement.

Xilinx has extended the TAP to include in-system programming capabilities. Just four dedicated pins are needed for both programming and testing any number of devices.

JTAG Operations

The XC9500 devices support standard and optional JTAG operations, including:

- **SAMPLE/PRELOAD** - Allows output sampling and input stimulus preloading while the device is fully operational.
- **EXTEST** - Allows testing of device interconnections, independent of internal device operations.
- **BYPASS** - Bypasses a device by effectively connecting TDI to TDO.
- **IDCODE** - Used to identify the system, to verify that a system is "alive," and to select specific test sequences. It can be used for system debug, manufacturing test, field diagnostics, and upgrades.
- **USERCODE** - Used to identify the contents and version of a system. This is essential for on-line diagnostics, field upgrades and the specification of test sequences or programs to be used during manufacturing. Also used during prototyping and manufacturing for version control.
- **INTEST** - Facilitates functional verification, independent of system interconnections. This is essential for prototyping and for low-cost manufacturing test because it can immediately identify functional errors in your design.
- **HIGHZ** - Facilitates interconnect test in systems with busses. It allows unique enabling and disabling of drivers on bussed lines and can also be used to isolate and diagnose interconnect failures.

These operations are fully-compatible with the IEEE 1149.1 JTAG standard and all third party JTAG test systems.

Xilinx provides everything you need for developing, programming and automatically testing XC9500 devices. This support is available for SUN, HP 9000 and IBM-compatible PC platforms.

In summary, the XC9500 CPLD family is the first to feature full in-system programming and test capabilities. This family of high-speed, high-density devices will help you produce complex designs more efficiently, and those designs will be easier to program and verify. Circuit board manufacturing and maintenance costs are reduced since production designs can be modified and tested without retooling or using expensive board testers. ◆

FIFO Buffer Designs in The XC4000E/EX FPGA Families

Many XC4000 designs use the distributed RAM feature to implement First-In-First-Out (FIFO) elastic buffers to form a bridge between subsystems with different clock rates and access requirements. However, the non-synchronous nature of the single-port RAM in the original XC4000 architecture leaves the designer with several challenges. Addresses must be multiplexed, independent read and write clocks must be synchronized, and access requests must be arbitrated.

The synchronous dual-port option RAM in the new XC4000E and XC4000EX FPGAs eliminates most of these problems.

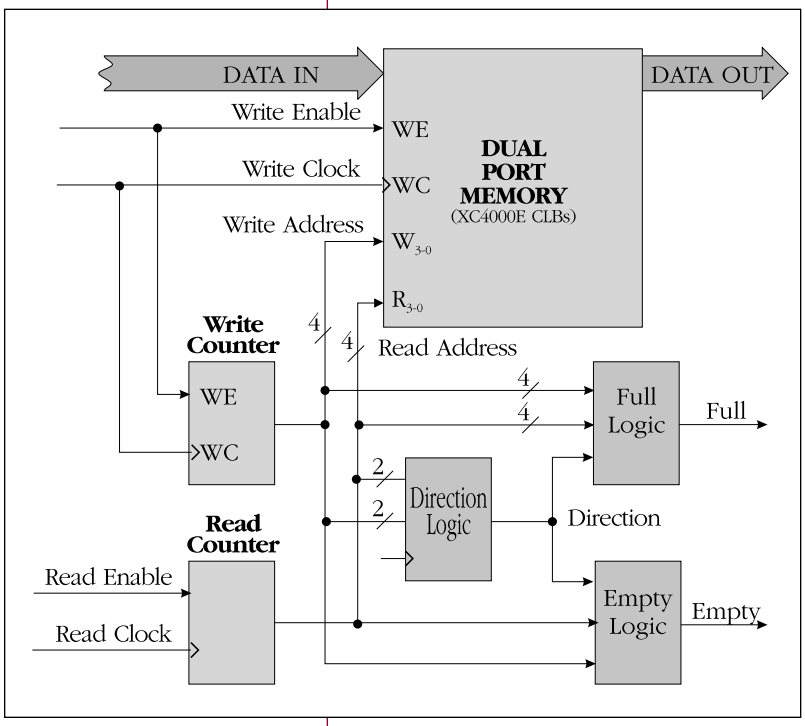


Figure 1 - 16x16 FIFO Block Diagram

Since the dual-port RAM in each CLB has independent write and read addresses, there is no need to multiplex addresses and arbitrate their selection. The synchronous write mechanism simplifies write timing and contributes to much faster operation. The FIFO design effort can now be concentrated on achieving high throughput and low cost, and on solving the fundamental timing problems created by asynchronous read and write clocks.

Synchronous and Asynchronous FIFOs is an application note now available on the Xilinx WebLINX World Wide Web site (http://www.xilinx.com). This application note describes six complete design examples of RAM-based FIFO designs using the dual-port RAM feature of the XC4000E and XC4000EX FPGAs. Three synchronous designs with a common read/write clock are described, as well as the corresponding three asynchronous designs with independent read and write clocks. Emphasis is on the fast, efficient and reliable generation of the handshake signals FULL and EMPTY that determine design performance.

The first design is a synchronous 16x16 FIFO buffer, where the depth of the basic CLB-RAM is sufficient. This leads to a very fast and efficient implementation that can run at, or close to, the maximum write speed of 70 MHz (-3 speed grade), even for simultaneous read and write operations. This is the simplest and fastest design because it avoids the more challenging issues of asynchronous clocking. The design occupies 23 CLBs.

Figure 1 shows the basic block diagram of the 16x16 FIFO buffer. In the synchronous version of this design, read and write clocks are identical. The 4-bit read counter and the 4-bit write counter (**Figure 2**) are implemented as two cascaded 2-bit Grey or Johnson counters. In a fully synchronous design, this choice is not mandatory, but it has advantages in the non-synchronous implementation. It is, however, mandatory that the upper two bits always stay constant for four consecutive counts. Therefore, Linear-Feedback-Shift-Register (LFSR) counters cannot be used.

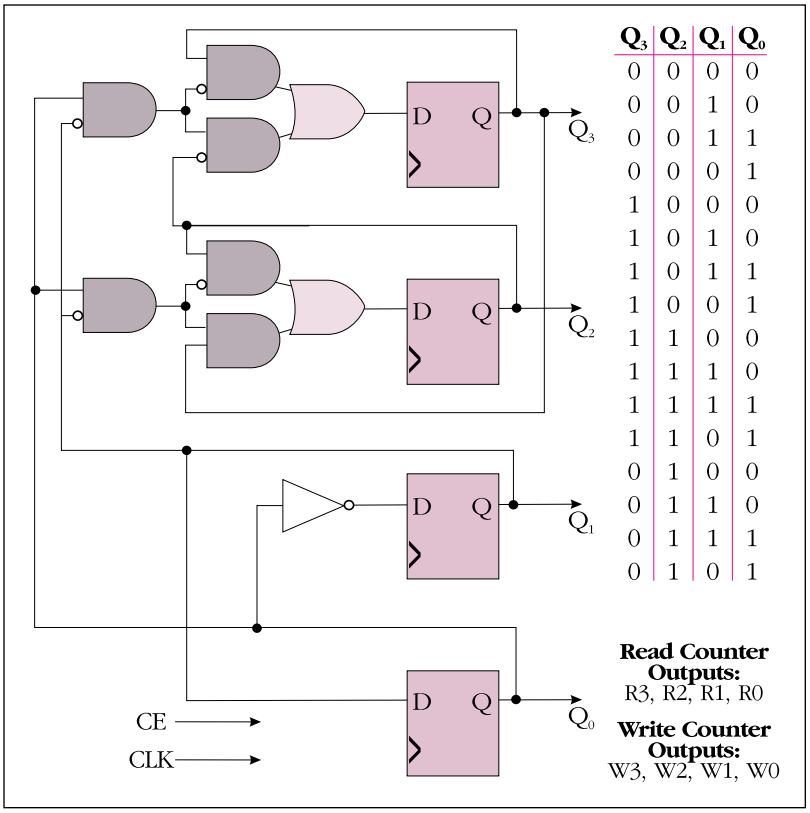
The two 4-bit counters address the RAM in the conventional way. Seen as a “black

box," the FIFO buffer behaves like an elastic shift register: input data is latched by an active edge on the Write Clock, and output data is always available at the output port. FULL and EMPTY signals must be interpreted by external logic to prevent a Write operation during FULL, or a Read operation during EMPTY.

Most of the design effort is spent on the control logic (**Figure 3**) that detects the FULL and EMPTY conditions. Since the easily decoded signal for these two abnormal conditions is the same — read address is identical with write address — an additional signal must be created that distinguishes between the the two very different conditions of FULL and EMPTY. For this purpose, an auxiliary signal, called DIRECTION is created to indicate whether the Write counter is about to catch up with the Read counter, or whether the Read counter is about to catch up with the Write counter. The two most significant bits of both counters are compared, since they indicate in which quadrant of the 16-position circular address space the present address resides. These two most significant bits of both address counters together are used to address two 4-input look-up tables in parallel. The look-up tables (LUTs) decode the relative quadrant position of the two counters.

The 4-bit LUT address describes one of 16 possible conditions:

- Four addresses describe the situation where the write counter is in the quadrant immediately behind the read counter. This is decoded as a "possibly going full" condition, and sets the DIRECTION latch or flip-flop.
- Another four addresses describe the situation where the write counter is in the quadrant immediately ahead of the read counter. This is decoded as a "possibly going empty" condition, and it resets the DIRECTION latch or flip-flop.
- Four other addresses indicate that the two counters are in the same quadrant, and another four addresses indicate that the two counters are in opposite quadrants. These eight addresses provide no useful information about the relative address position, and thus do not affect DIRECTION. Note that DIREC-



Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	1	0
0	0	1	1
0	0	0	1
1	0	0	0
1	0	1	0
1	0	1	1
1	0	0	1
1	1	0	0
1	1	1	0
1	1	1	1
1	1	0	1
0	1	0	0
0	1	1	0
0	1	1	1
0	1	0	1

Figure 2 - Read Counter or Write Counter

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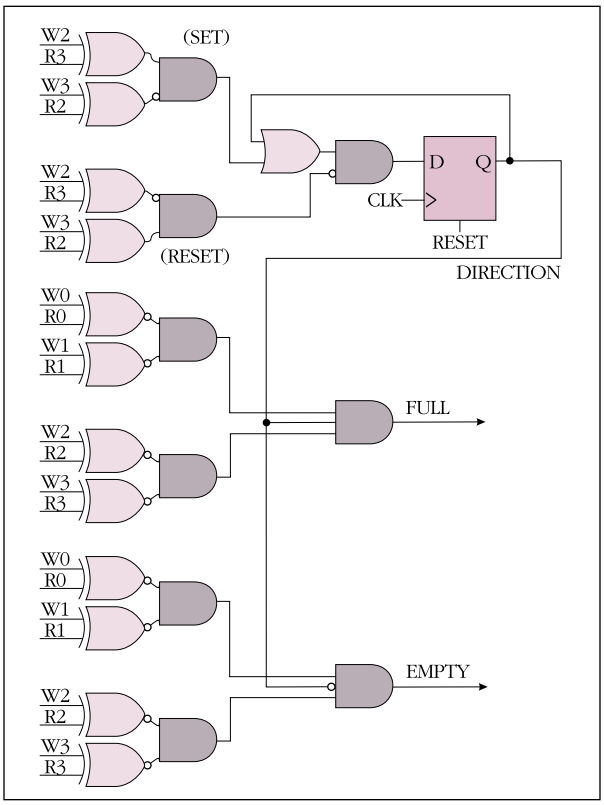


Figure 3 - 16x16 FIFO Synchronous Control

Distributed Arithmetic Laplacian Filter

A common practice in image processing involves convolving an image with a Laplacian operator. **Figure 1** shows a typical Laplacian operator that might be used for edge enhancement. To convolve it with an image, the operator is moved over the image, and centered over each pixel in turn. In each position, the 25 weights in the matrix are multiplied and accumulated with the 25 pixels that the matrix covers. This operation yields one pixel in the resulting image.

-16	-7	-13	-7	-16
-7	-1	12	-1	-7
-13	12	160	12	-13
-7	-1	12	-1	-7
-16	-7	-13	-7	-16

Figure 1 - Example Laplacian operator for edge enhancement in an image processing system.

This is an ideal application for "distributed arithmetic" techniques that exploit the lookup-table (LUT) architecture of the XC4000E™ FPGA family. **Figure 2** shows the basic approach. Four external line buffers plus the incoming video data provide simultaneous access to five lines of the image. Inside the FPGA, each of the video streams is serialized and passed through four 1-bit-wide shift registers, each of which delay the data by one pixel. This provides simultaneous bit-serial access to five adjacent pixels from five adjacent lines — the region covered by the Laplacian filter. The shift registers can be implemented very efficiently using the CLB RAM feature of the XC4000E FPGA architecture.

In the most basic distributed arithmetic approach, the 25 signals address a 2^{25}-word LUT which, in turn, feeds a shifting accumulator. This is obviously impractical. A typical cost-reduction measure would be to partition the problem, segmenting the addresses into multiple smaller LUTs. The outputs of these smaller LUTs would be combined in an adder tree to provide the input to the accumulator.

In this particular case, however, the weighting values involved permit the use of more efficient techniques. Except for the values 160 and -7, each of the coefficients is used in four places.

FIFO Buffer

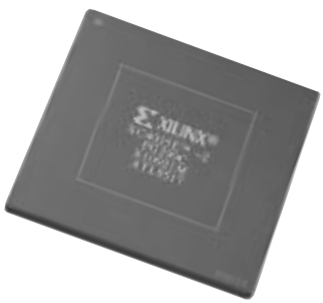
Continued from previous page

TION must start in the reset state when the FIFO is initiated with both counters at zero.

DIRECTION is thus established well before the actual FULL or EMPTY condition can occur. There will be at least four, and usually many more, consecutive set or reset inputs to the DIRECTION latch or flip-flop before it is being used to discriminate between FULL or EMPTY.

FULL goes active as a result of the write clock edge that writes data into the last available location. FULL goes inactive as a result of the first read clock that reads one word out of the previously full FIFO buffer. EMPTY goes active as a result of the read clock edge that reads the last available data from the FIFO buffer. EMPTY goes inactive as a result of the first write clock that writes one word into the previously empty FIFO buffer. In a synchronous design, FULL and EMPTY are synchronous control signals, to be used appropriately by the logic external to the FIFO buffer.

The application note goes on to describe an asynchronous version of the 16x16 FIFO buffer, and 32x8 and 64x8 FIFO buffers with both synchronous and asynchronous read and write clocks. The larger FIFO buffer designs include input and output data multiplexing between multiple RAM banks. The asynchronous 32x8 FIFO buffer requires 28 CLBs and the 64x8 FIFO buffer needs 48 CLBs; both can perform simultaneous read and write operations at 40 MHz. ◆



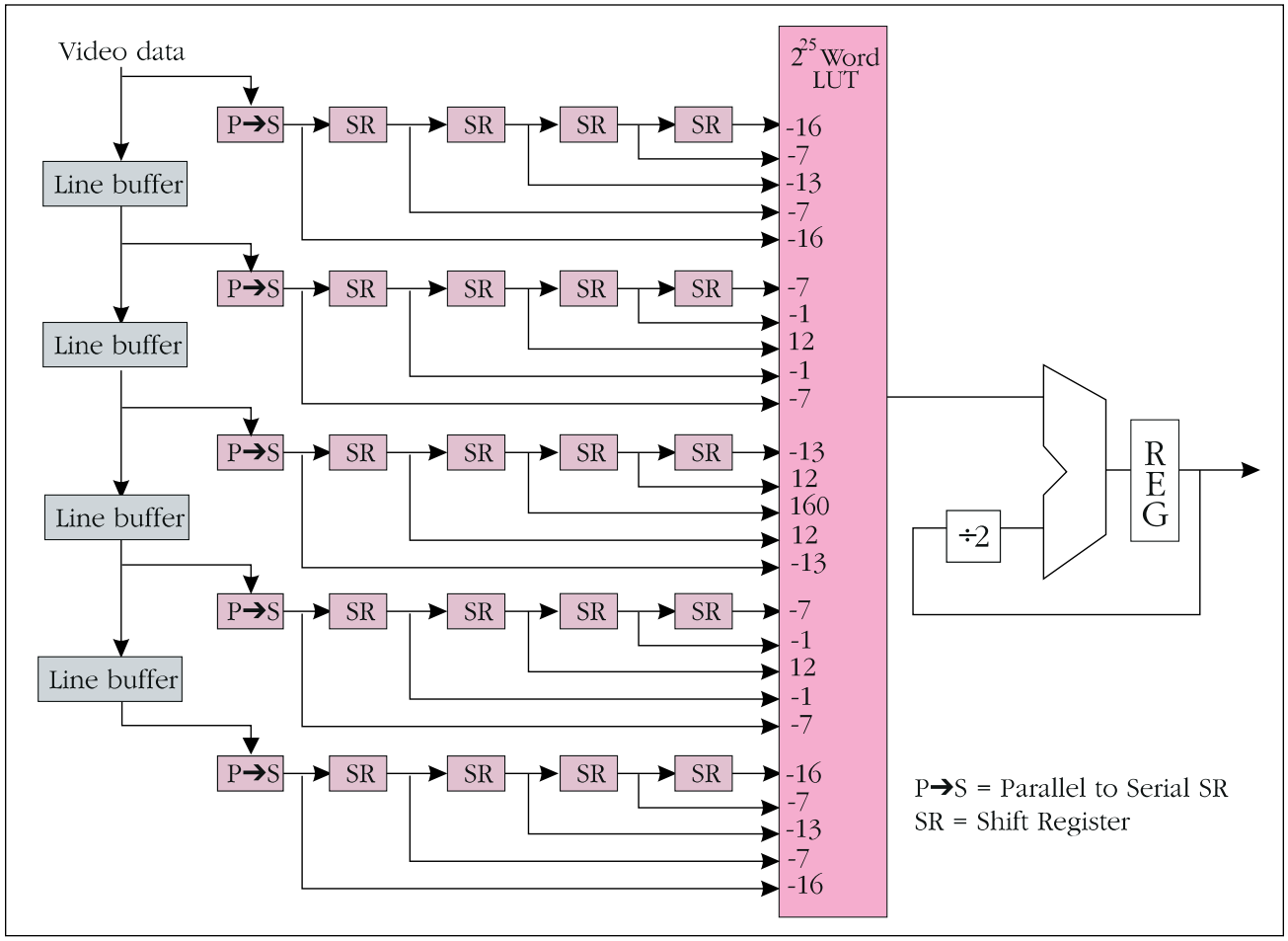


Figure 2 - Basic approach to implementing the Laplacian operator.

Consequently, serial adders can be used to combine four serial bit streams into one before addressing the multiplying LUT (**Figure 3**). Effectively, this adds, and then weights, data that would otherwise be weighted and added afterwards. A tree of three serial adders is needed in each case, and each serial adder can be implemented in a single CLB.

The value -7 is used eight times. The eight inputs could be combined into one, but here it is only necessary to reduce them to two lines. The value 160 is used once, and the data only needs to be delayed to match the delay introduced into the other paths by the serial adders.

These modifications reduce the size of the LUT from 2^{25} words to 2^{7} words. This is a large reduction gained from a small amount of logic, but the LUT still is so large that it would have to be split. However, further techniques can be applied.

The -13, -16 and the two -7 values need to be combined into a LUT (**Figure 4**). The values 12 and 160, however, have no non-zero bit locations in common. Consequently, all possible sums of the two values can be achieved by simply wiring the input signals to appropriate bits of the adder.

All that remains is to handle the -1 value. This value uses the carry input of the adder, but requires some trivial modification to the LUT. Instead of containing all of the possible sums of -13, -16, -7 and -7, it is loaded with all the sums of 13, 16, 7 and 7. The minus signs are accommodated by subtracting in the "adder."

The output of the LUT is inverted as part of a conventional invert-and-add-one method of subtraction. The -1 value can then be accommodated by simply omitting the "add-one" when necessary.

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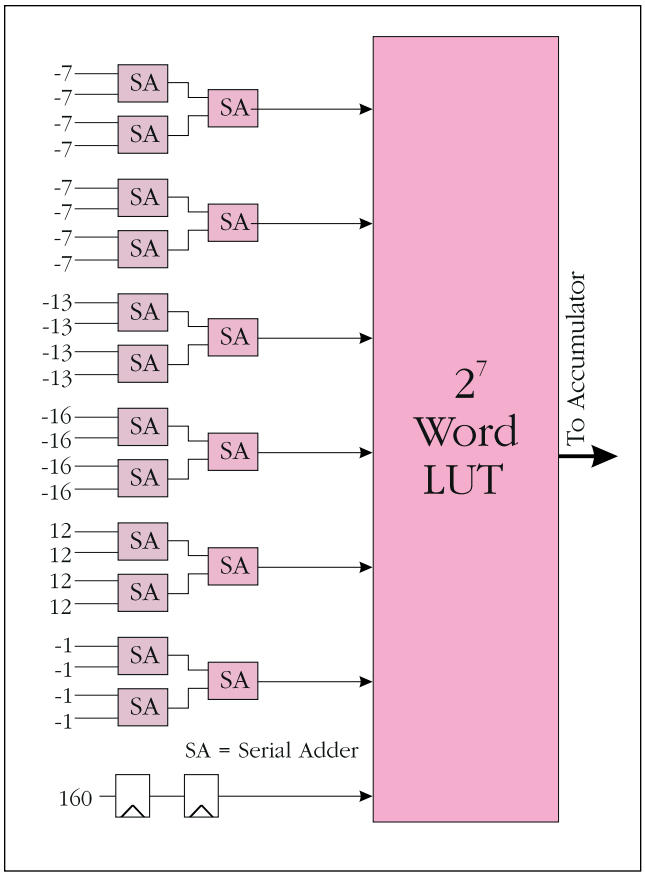
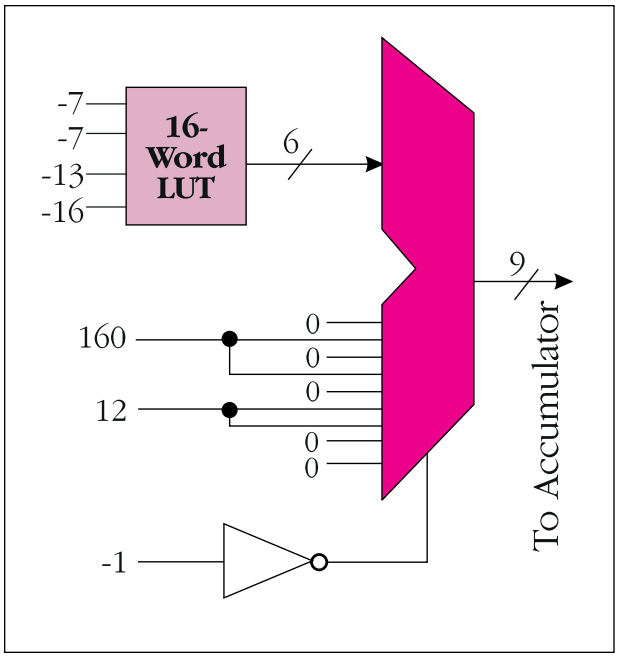


Figure 3 - Serial bit streams can be combined before entering the LUT.



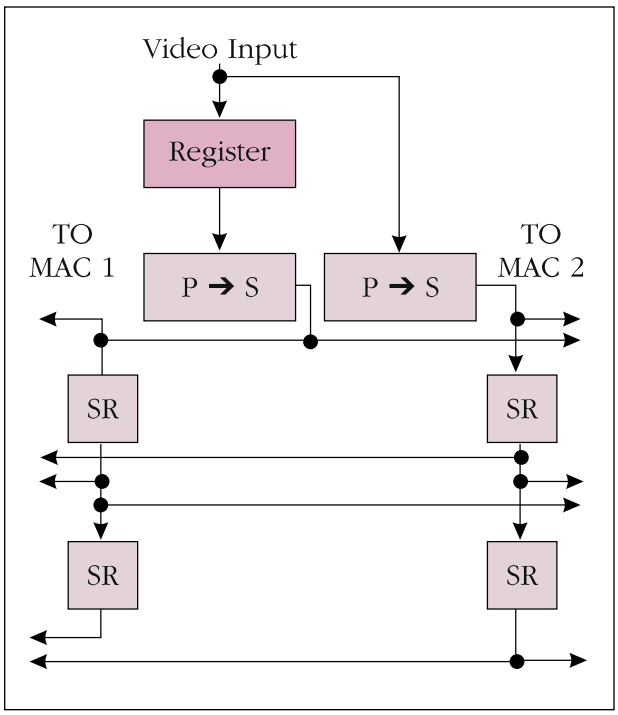


Figure 4 - (top) Final implementation of Laplacian operator.

Figure 5 - (right) Sharing input shift registeres between parallel MACs.

Laplacian

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That means the inverted -1 input is used as the carry input to the adder.

In this way, the 2^{25}-word LUT is reduced to a 16-word LUT plus 18 serial adders and one 9-bit parallel adder.

Bit-serial arithmetic inherently involves multiple cycles per pixel. With the multiplier-accumulator reduced to such a small size, however, two or more of them could be used in parallel to regain throughput.

Figure 5 shows how input shift registers can be shared between two MACs.

For each MAC operation, two pixels are brought in, and loaded simultaneously into two parallel-to-serial converters. This requires an additional register to temporarily hold one of the pixels. Six serial outputs are formed, and these are used as two overlapping sets of five each. ◆

Retargeting Designs in Mentor Graphics Design Architect

A new utility in Design Architect (DA) from Mentor Graphics can be used to retarget schematic-based designs between Xilinx FPGA families. Although the *Mentor Graphics Interface/Tutorial Guide* recommends using the Change References utility in Mentor's Design Manager to accomplish this, the latest version of the Mentor interface (5.2) includes **Convert Design**, a more thorough and robust utility for retargeting a Xilinx schematic.

◆ ◆ ◆

Invoke PLD_DA (it is not necessary to open the schematic). On DA's desktop background (that is, outside of any schematic or symbol windows), call up the session pop-up menu with the mouse button on the right and select Convert Design. Of the fields in the resulting dialog box these are the most relevant:

Select a group of designs from a list file? Whether you answer "yes" or "no" to this question affects the following field.

Enter Design name (List file = no). The name of the design to retarget. Convert Design does *not* traverse the hierarchy of a schematic.

Enter list file name (List file = yes). A file which lists designs, one per line, to retarget. This is useful if your design has many lower-level schematics.

TIP: You can easily create a list file with the following command:

```
ls *.mgc_component.attr | sed s/.mgc_component.attr//g > listfile
```

The **ls** command lists all MGC components within a single directory; the **sed** command strips off the .mgc_component.attr trailer. The result is redirected to **listfile**.

Schematic name. The name of the schematic model (the default is "schematic").

Check & Save switch. Because all schematic sheets in Convert Design are literally redrawn in Design Architect, you must apply Check & Save to each sheet. This switch controls whether to do this automatically. By default, this switch is set for manual checking because it allows you to spot Xilinx components that did not convert properly. Use the manual setting until you are comfortable with how Convert Design works and you are certain that all Xilinx components will convert properly.

From Technology. The device family from which you are converting (e.g., XC3000, XC4000, XC4000E, XC5200, etc.). This and the next field are case insensitive.

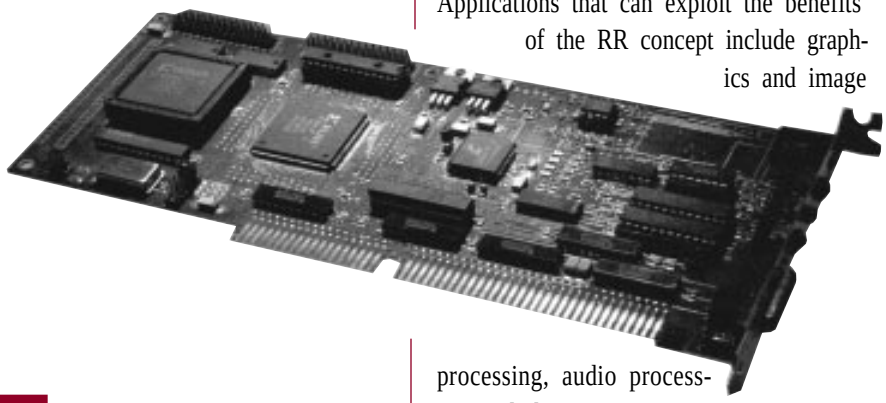
To Technology. The device family to which you are converting.

After filling out the fields in the dialog box and selecting "OK," you will see Convert Design doing its job directly in Design Architect. ◆

Note: The first few times you use Convert Design, you may want to make a copy of the schematic(s) you wish to retarget, to make sure you have a feel for what this utility does before modifying your design permanently.

Metalithic Systems Exploits Real-Time

The Xilinx Reconfigurable Computing Developer's Program is promoting the commercial use of FPGAs in Rapid Reconfiguration (RR, also known as reconfigurable computing) applications. These systems add significant value by dynamically changing FPGA designs, in real-time, while the system is operating. Applications that can exploit the benefits of the RR concept include graphics and image processing, audio processing and data communications.



In recognition of the unique achievements of Metalithic System Inc. (Sausalito, California), Xilinx presented the company with its inaugural "RR Company of the Quarter" award. Metalithic Systems (MSI) was one of the first companies to realize the potential of RR, and has released a commercial product that has RR benefits which vastly improve the music industry's state-of-the-art.

MSI's *Digital Wings* audio processing system uses FPGAs in one of its first mass-market commercial applications. *Digital Wings* is a complete audio authoring system that operates in the Windows environment on a PC. It delivers 128 tracks, allowing a random access edit environment with a programmable algorithmic synthesizer that supports pan, level, fade, parametric EQ, echo, chorus, reverb and stereo effects.

The *Digital Wings for Audio* product — a system consisting of a single add-in board for the PC and related software — was announced and demonstrated at the NAMM (National Association of Music Marketers) convention in Anaheim this January. (NAMM is the "COMDEX" of the music industry.) Their closest competitor was displaying a 48-track, 9-board system costing more than 50 times as much. Enthusiastic editorial interest in MSI and *Digital Wings* has resulted in feature articles planned for upcoming editions of

Using Decoupling Capacitors

As CMOS devices have become faster and as the number of outputs increases, good decoupling is vital to reliable circuit operation. Current pulses with a 1 ns rise or fall-time must be treated like GHz signals. In fact, digital printed circuit board designers could learn something from looking inside a UHF-TV tuner.

The standard "rule of thumb" for decoupling-modern CMOS ICs is to mount one low-inductance, decoupling capacitor of 0.01 to 0.1 µF very close to each V_{CC} pin. This provides the fast changing dynamic supply current, especially when capacitively-loaded outputs are switching.

The big power-supply capacitor, and even the 100 µF board-decoupling capacitor, cannot perform this function. First, big capacitors have an unavoidable internal series-inductance that makes them incapable of supplying fast-changing current pulses with nanosecond rise and fall-times. Second, those capacitors are typically positioned too far away from the devices that need access to an instant current reservoir. Even a good power/ground distribution network has unacceptable inductance over distances of several inches.

For example, assume a device has 40 outputs switching simultaneously (or within a few nanoseconds of each other), with each output

Reconfigurability for Audio Processing

The staff of Metalithic Systems.

Pro Sound News, EQ, Electronic Musician and *Mix*. MSI left the convention with commitments for tens of thousands of systems. *Digital Wings* will be distributed through retail stores later this spring.

MSI's proprietary "nanoprocessor technology" uses Xilinx XC3090 and XC4005 FPGAs to reconfigure the system's hardware on-the-fly. Hardware changes with the needs of the system. In one instant it handles a specific communication function, in the next it is configured as a multi-processor to do complex pattern recognition, and in the next it's a microcontroller handling a specialized peripheral. Reconfigurable FPGAs perform all these functions, significantly reducing system cost while accelerating system performance.

Congratulations are due to the whole MSI development team. For more information on the *Digital Wings* product, contact Metalithic Systems at 415-332-2690. ◆

For more on the Xilinx Developer's Program and our RR efforts, please see our web site at http://www.xilinx.com or call John Watson at 408-879-6584.

driving a 100 pF load. With an output swing of 4 V and all outputs switching in the same direction, each such transition consumes 0.016 µCoulomb. If four decoupling capacitors of 0.01 µF have to supply this charge, they will drop their voltage by 0.016/0.04 = 0.4 V. That is barely acceptable. Four 0.1 µF decoupling capacitors would be preferred, since they reduce this drop by an order of magnitude. Capacitors larger than 0.1µF tend to have more series-inductance, and are actually inferior for this application.

Another way to look at dynamic current requirements is to start with power dissipation. A 3-watt device clocked at 40 MHz does not consume a steady 600 mA, but might consume 3 A for 5 ns, and very little for the rest of the time. As explained above, to provide the 0.015 µCoulombs (3 A x 5 ns) requires at least four 0.01 µF decoupling capacitors, and 0.1µF would be better.

The need for V_{CC} decoupling varies with the amount of internal logic, the number of outputs that switch simultaneously and their capacitive load. The rule of one low-inductance 0.01 to 0.1 µF capacitor at each V_{CC} pin is still a good guideline. ◆

INSTALL

Q Can I use XACT*step* v6 with Windows 95?

Windows 95 is not officially supported by the XACT*step* v6 release, but many users have been successfully working with this combination. You will, however, run into this problem: when exiting the Design Manager, the error message "This program has performed an illegal operation and will be shut down." will appear. Simply choose Close; this message is benign.

The Viewlogic PROseries tools are not supported in Windows 95. Windows NT is not supported by XACT*step* or PROseries.

Q How can I find out more information about my Windows Configuration?

There are two Windows utilities on the XACT*step* CD-ROM (the following instructions assume that C:\ is the hard drive and D:\ is the CD drive). Choose File➡Run from the Program Manager and select D:\XBBS\UTILS\XINFO\XINFO.EXE to run XINFO. XINFO will analyze the current configuration of your PC, and report DOS and Windows environment settings, amount of memory available, and a list of hints and recommendations. The other program, XMEM, is run by selecting D:\XBBS\UTILS\XMEM\XMEM.EXE from File➡Run. This dynamic program will keep you updated with the status of RAM, memory below 1 Meg, and USER and GDI percentages. These tools are designed to help you debug memory or configuration issues you may come across.

Q I followed the instructions from the article "Executing from the XACT*step* CD-ROM" from the last issue of XCELL (#19, 4Q95) but I still get errors. What am I doing wrong?

The article assumed that the XACT*step* SETUP program had been previously run. In other words, it assumed that some Windows environment settings had already been configured. Here's what you'll need to do:

1. Install the correct version of Win32s, which is 1.25.142.0. You can verify this by looking at the file: C:\WINDOWS\SYSTEM\WIN32S.INI or by checking XMEM or XINFO. If you do not have this version, exit Windows and run the batch file from the XACT*step* CD-ROM: D:\XBBS\UTILS\RMWIN32S.BAT. Then re-enter Windows and choose File ➡Run and select D:\WIN32S\DISK1\SETUP.EXE to install the proper version of Win32s.
2. Install the necessary Windows drivers. If you are only using the XACT*step* tools, do the following:

```
copy D:\XACT\WINDOWS\SYSTEM\*.* C:\WINDOWS\SYSTEM
mkdir C:\WINDOWS\ASYM
mkdir C:\WINDOWS\ASYM\RUNTIME
copy D:\XACT\WINDOWS\ASYM\RUNTIME\*.*
C:\WINDOWS\ASYM\RUNTIME
  If you are using the PROseries tools, you will also need
to do the following:
copy D:\PROSER\WINDOWS\*.* C:\WINDOWS
copy D:\PROSER\WINDOWS\SYSTEM\*.* C:\WINDOWS\SYSTEM
```

3. Install the DAIKON.386 device driver. You have already copied this driver in Step 2, but now you need to edit the C:\WINDOWS\SYSTEM.INI file. Open this file and add the line:

```
DEVICE=DAIKON.386
```

after the [386Enh] header. After you quit and re-enter Windows, you'll be all set.

Design Manager/Flow Engine

Q When using Viewlogic schematics, what can I do to avoid problems in the translation phase of the Design Manager?

There are several problems that can stop the design from translating. The .WIR files must be present for the translation process to complete. If they are missing, the design can be brought up to date by running check -p <design>from a DOS prompt or selecting Tools ➡check ➡project from PROcapture. The parttype must be specified either in the design or in the Translate Options dialog box; WIR2XNF requires a parttype to be specified. The path to the design must not contain a period, other than in the name of the design file.

Continued on the next page

Q How do I change options that aren't listed in the Options dialogs?

Select Utilities ➡ Template Manager from the Design Manager's menu. Select the desired template and click on the Customize... button. In the Custom Template Dialog, type in the program name and the desired option. For example, to force XNFPREP to ignore xnf locations in the interior of the chip, the following line would be used:

```
xnfprep ignore_xnf_locs=true
```

When any custom options are used, an asterisk will appear next to that template.

Q I am running the Flow Engine from the Design Manager and it hangs. My PC is still working (I can move my mouse), but the Flow Engine seems to have stopped. What has happened?

The problem is that the DOS process underneath the Windows application has become disconnected. The Flow Engine is still running in Windows, but there is nothing running in DOS to tell it when it is done. Try the following suggestions one at a time:

1. Disable 32-bit File Access and reduce the cache size by using the Control Panel ➡386Enhanced ➡Virtual Memory ➡Change. (Windows 3.1.1 only)
2. Disable SmartDrive write caching by using the /X option.
3. Disable 32-bit Disk Access, also found in the Virtual Memory settings.

If these changes do not fix the problem, call the Technical Support Hotline at 800-255-7778.

Q Selecting Design ➡Implement seems to give one Flow Engine while the Tools ➡Flow Engine gives a different one. What's the difference?

The one under Design ➡Implement is an automatic version of the Tools ➡Flow Engine. Use the first to perform automatic runs; use the latter to set advanced options or stop the flow at a certain point.

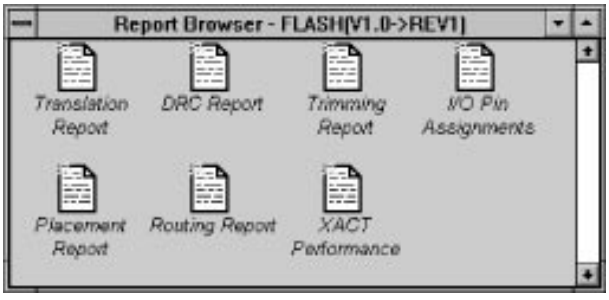
Q The Flow Engine appeared to hang in bitstream phase. How do I get it to finish?

This is a problem we have traced to 32-bit file access in Windows for Workgroups v3.1.1. In the Windows control panel under Enhanced ➡ Virtual Memory... ➡ Change>>there is a "Use 32 Bit File Access" checkbox. Turn this off, restart Windows, and the Flow Engine should complete successfully.

Q What's the difference between the report browser and browse revision?

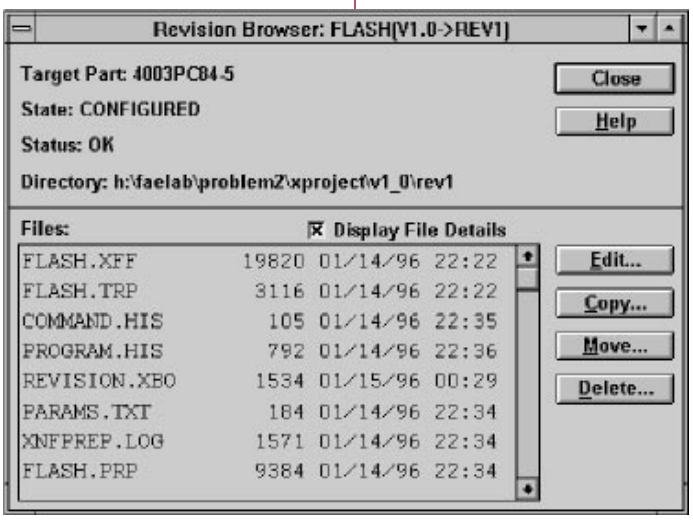
The report browser is a graphic interface that allows access to the most commonly needed report files, such as I/O pin locations, trimming report, etc. Design ➡ Browse Revision allows access to all the files in a selected revision through a listing of the files. (See figures.)

Technical Questions and Answers continued on the next page



Report Browser

Revision Browser



Mentor Graphics

NOTE: A more elegant solution was in development at press time. For further information, send an e-mail to xdocs@xilinx.com with "send 692" as the subject line.

Q I have several external signals connected to PAD symbols that I merge into or bus-rip out of a single bus connected to a bussed I/O buffer symbol (*e.g.*, IBUF8, OBUF8, *etc.*). I have done this so that I can place LOC properties on the individual PAD symbols (since they cannot be placed on IPAD8s, OPAD8s, *etc.*). However, when I compile the design, I discover that the LOC constraints have not been followed, and no warning has been issued by any programs. In fact, these LOC properties do not exist in any of the XNF files output by Men2XNF8! What's happening?

The Mentor translation process involves two programs, ENWrite and EDIF2XNF. ENWrite (a Mentor program) generates an EDIF netlist which EDIF2XNF translates to a set of XNF files. When signals are bussed in a Mentor schematic, ENWrite creates a construct called a "net bundle" in the EDIF file. Although all the information about the associated LOC properties is included as part of the net bundle, EDIF2XNF expects to see a separate, independent construct for each of these nets when it looks for associated properties. Therefore, when EDIF2XNF translates these net bundles from the EDIF file, it leaves off the pin-location constraints that were placed on the input and output signals. This problem is solved by simply bus-ripping the signal path internally (*i.e.*, after the IBUFs or before the OBUFs).

Q Some LOC properties on the pads in my design are not passed to subsequent stages in the design compilation. I've noticed that these LOC properties are displayed as purple text in Design Architect, instead of the normal gold color. What does this mean?

A purple property in Design Architect means that the property is attached to the *pin* on the PAD symbol, whereas a gold property means that it is attached to the *net* attached to the pin. Because the PAD symbols in the Mentor libraries are defined as ports, any properties attached to these symbols (*i.e.*, shown in purple) will not be passed to the EDIF file during Men2XNF8, and thus will not be passed to subsequent stages of the compilation.

Usually, LOC properties on Xilinx PAD symbols will transfer to the attached net and will therefore appear gold; however, sometimes the property gets stuck on the PAD pin. The workaround is to select the *net vertex* connected to the offending pin, then add the LOC property to the net vertex. This new property should show up in gold, and thus will be passed to the compilation tools. In any case, beware of purple LOC properties!

Q When running the Check function in Design Architect, I get these warnings:

```
Warning: Unable to evaluate property "model" on I$30
   Unable to resolve expression symbol lca_technology
Warning: Unable to evaluate property "__qp_prim" on I$30
   Bad Triplet CASE Control Expression
Unable to resolve expression symbol lca_technology
```

What do these warnings mean and how can I fix them?

All Xilinx simulation models in Mentor have a variable associated with them called "lca_technology." Normally, this parameter is set whenever a library component is instantiated, but a number of situations can cause Design Architect to lose this parameter. If this happens, Check will not be able to evaluate any properties that use this parameter; however, the lca_technology parameter does not need to be set until the design is simulated or translated to an XNF netlist, at which point the lca_technology parameter is filled in appropriately. Therefore, these warnings can be safely ignored.

You can recover the value of lca_technology and unclutter the Check report of these warnings by selecting Check → Parameters → Set. In the dialog box, enter **lca_technology** as the parameter name, and set the value to the appropriate device family (e.g., **xc3000** or **xc4000**). After doing this, re-execute Check Sheet.

Synopsys

Q Can Input and Output flip-flops be inferred in XC4000E designs?

Synopsys can infer input and output flip flops in an XC4000E design. However, if a flip flop has its clock enable (or reset pin) connected, then Synopsys cannot infer it as an IOB flip-flop, and it will be implemented as an XC4000E CLB flip-flop. For a flip-flop to be inferred as an IOB flip flop by Synopsys, its clock enable (and reset pin) must not be connected to anything. You must, therefore, instantiate IOB flip-flops that have their clock enable pin connected.

Q Can Synopsys infer an input flip-flop with the "NODELAY" attribute?

The Synopsys (XSI) For FPGAs manual states on page B-9 and B-10 that input latches and flip flops with the NODELAY attribute may be inferred. This is not true. All Input flip flops and input latches with a NODELAY attribute must be instantiated.

Input Flip-Flops:

For the XC4000/A/H/D family, the "fast" input flip-flops are IFD_F and IFDI_F

For the XC4000E family, the "fast" input flip-flops are IFDX_F, IFDXI_F, and IFDXI_U

Input Latches:

For the XC4000/A/H/D family, the "fast" input latches are ILD_1F and ILDI_1F

For the XC4000E family, the "fast" input latches are ILDX_1F and ILDXI_1F

Q Do I require any additional settings for XC3000 or XC5200 designs in Synopsys?

There is one additional setting that you should include into your .synopsys_dc.setup file, if you are using the FPGA Compiler to synthesize XC3000 or XC5200 designs. Include the following line in your .synopsys_dc.setup file:

```
fpga_improved_delay_mapping = 1
```

◆

Technical Support Resources

In addition to field application engineers (FAEs) and technical support engineers (TSEs) located all over the world to provide direct support, Xilinx has several automated services to provide answers to your queries: an e-mail server, an automated FAX system, a bulletin board system, and special interest e-mail groups.

The **XDOCS** e-mail system provides 24-hour-a-day, 7-day-a-week access to the same database that the TSEs use. It is updated daily with bugs, workarounds, and helpful hints. Via e-mail, users can search for a specific record, or use keywords to trigger a search of the database; XDOCS will send the requested information by return e-mail. Users can receive periodic updates regarding new additions to the system.

To subscribe to XDOCS, send an e-mail to xdocs@xilinx.com with "help" as the only word in the subject header.

The **XFACTS** automated FAX system (408-879-4400) provides the same information as XDOCS, but uses a phone/FAX interface instead of e-mail. Using a touch-tone telephone, users can request documents that are sent to their FAX machine.

The **technical support group** also has an e-mail alias: hotline@xilinx.com, and a bulletin board that is updated with utilities such as new package files as they become available.

Due to the growth in interest in specific application areas, Xilinx has established a set of e-mail addresses to provide support for questions related to these topics *(see margin at right).*

If you have any questions or comments regarding these systems, or if there are other support methods that you would like to see implemented, give us a call or send a FAX; the numbers are given in the margin at right. ◆

Synopsys (con't)

HOTLINE SUPPORT

United States

Customer Support Hotline:
800-255-7778
Hrs: 8:00 a.m.-5:00 p.m. Pacific

Customer Support Fax Number:
408-879-4442
Avail: 24 hrs/day-7 days/week

E-mail Address:
hotline@xilinx.com

Electronic Tech. Bulletin Board:
408-559-9327
Avail: 24 hrs/day-7 days/week

Customer Service*:
408-559-7778
ask for customer service
**Call for software updates, authorization codes, documentation updates, etc.*

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AUTOMATED SUPPORT

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http://www.xilinx.com.

XDOCS e-mail document server
for instructions, send an e-mail to xdocs@xilinx.com with "help" as only item in the subject header.

XFACTS fax document server -
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To: Brad Fawcett, *XCELL* Editor **Xilinx Inc. FAX**: 408-879-4676

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