Product Brief
December 2006
Revision 1.0

WPCN381U
Legacy-Reduced SuperI/O with Fast Infrared Port, Two Serial Ports and GPIOs

General Description

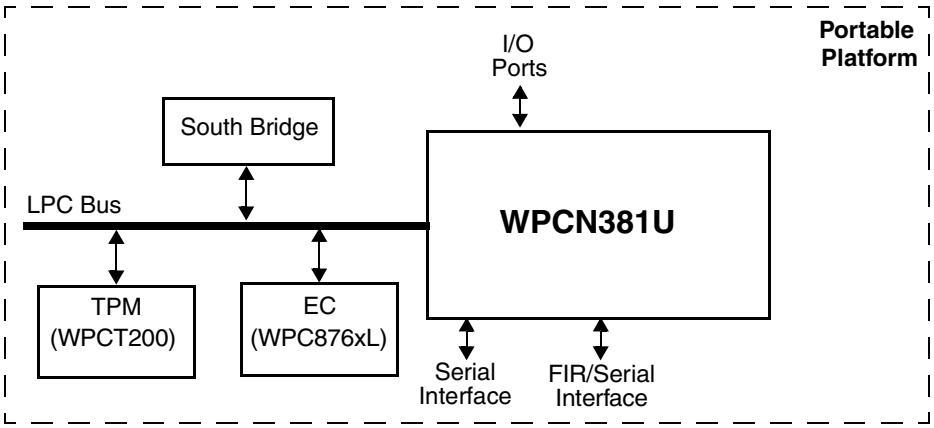
The WPCN381U, a member of the Winbond LPC SuperI/O family, is targeted for legacy-reduced ultra-light portable applications. The WPCN381U is PC2001 and ACPI compliant, and features a Fast Infrared port (FIR, IrDA 1.1 compliant), two Serial Ports and General-Purpose Input/Output (GPIO) support for a total of 11 ports.

The WPCN381U is a "no-frills" solution for the new generation of notebook systems, providing just the essential functions.

Outstanding Features

- Pin and software compatible with the Winbond 87381
- Fast Infrared Port (FIR)
- Two Serial Ports
- LPC bus interface, based on Intel's *LPC Interface Specification* Revision 1.1, August 2002 (supports $\overline{\text{CLKRUN}}$ and $\overline{\text{LPCPD}}$ signals)
- PC2001 and ACPI Revision 3.0 compliant
- 11 GPIO ports, including 6 with IRQ assertion capability
- Two testability modes (XOR Tree and TRI-STATE® device pins).
- 5V tolerant and back-drive protected pins (except LPC bus pins)
- 48-pin LQFP package

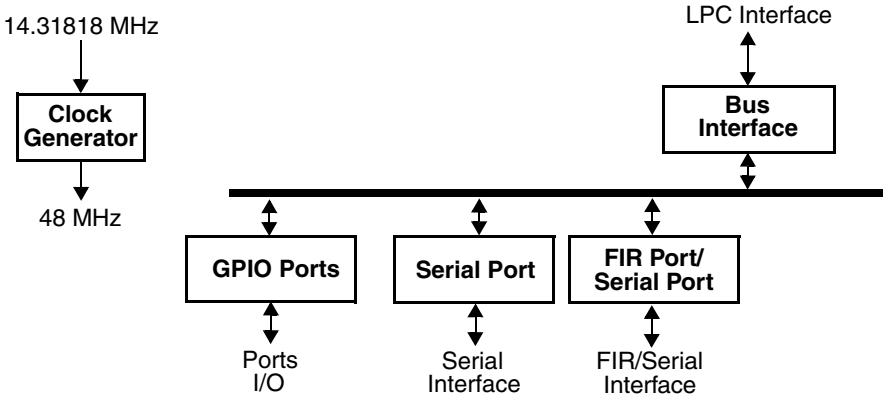
System Block Diagram



Features

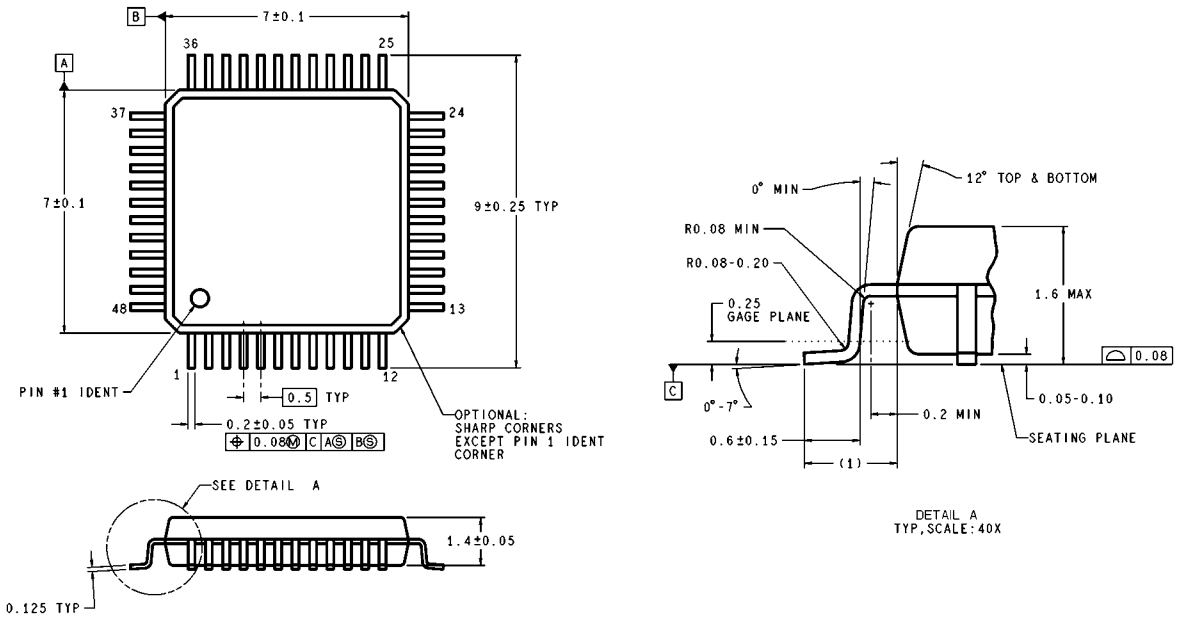
- Fast Infrared Port (FIR)
  - — Software compatible with the 16550A and the 16450
  - — Shadow register support for write-only bit monitoring
  - — FIR IrDA 1.1 compliant
  - — HP-SIR
  - — ASK-IR option of SHARP-IR
  - — DASK-IR option of SHARP-IR
  - — Consumer Remote Control supports RC-5, RC-6, NEC, RCA and RECS 80
  - — DMA support: one or two channels
- Two Serial Ports (SP1 and SP2)
  - — SP2 can be used only when FIR is not needed
  - — Software compatible with the 16550A and the 16450
  - — Shadow register support for write-only bit monitoring
  - — UART data rates up to 1.5 Mbaud
- 11 General-Purpose I/O (GPIO) Ports
  - — Supports IRQ assertion
  - — Programmable drive type for each output pin (open-drain, push-pull or output disable)
  - — Programmable option for internal pull-up resistor on each input pin
  - — Output lock option
  - — Input debounce mechanism
- LPC System Interface
  - — 8-bit I/O cycles
  - — $\overline{\text{LPCPD}}$ and $\overline{\text{CLKRUN}}$ support
  - — Implements PCI mobile design guide recommendation (*PCI Mobile Design Guide 1.1, Dec. 18, 1998)*
- PC2001 and ACPI 3.0 Compliant
  - — PnP Configuration Register structure
  - — Flexible resource allocation for all logical devices
    - ❑ Relocatable base address
    - ❑ 15 IRQ routing options
    - ❑ Optional 8-bit DMA channels (where applicable) selected from four possible DMA channels
- Clock Sources
  - — 14.318 MHz or 48 MHz clock input
  - — LPC clock, 0 or 30 MHz to 33 MHz
- Strap Configuration
  - — Base Address (BADDR) strap to determine the base address of the Index-Data register pair
  - — Strap Inputs to select testability mode
- Power Supply
  - — 3.3V supply operation
  - — All pins are 5V tolerant, except LPC bus pins
  - — All pins are back-drive protected, except LPC bus pins
- Testability
  - — XOR Tree
  - — TRI-STATE device pins

Internal Block Diagram



Physical Dimensions

All dimensions are in millimeters



DIMENSIONS ARE IN MILLIMETERS

VBH48A (Rev D)

48-Pin Low-Profile Plastic Quad Flatpack (LQFP)
Order Number WPCN381U_0DG
(Replace "_" with chip revision: A, B, and so on)

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