Advance Information

FE3600B
Chip Set Overview

- ❑ Four-chip core logic implementation for 80286-based IBM * AT * compatible computers
- ❑ Operates at high performance 16 MHz, .7 wait state, interleaved, page mode
- ❑ Programmable CPU, DMA, and system clock generator
- ❑ LIM EMS 4.0 support
- ❑ AT compatible Bus timing
- ❑ PLCC packaging
- ❑ Programmable wait state generator
- ❑ Memory control for up to 4 banks of DRAM (up to 8 Mbytes) programmable on 128K boundaries
- ❑ Provides data buffering for 16-bit local memory Bus
- ❑ Page mode access with 2 way or 4 way interleaved memory banks
- ❑ On-chip DRAM address multiplexing
- ❑ Provides data buffering for 8-bit local I/O Bus
- ❑ Zero wait state and other standard DRAM control modes available
- ❑ On-chip parity generation and checking
- ❑ CMOS technology

The Western Digital ® 3600B chip set is a four chip VLSI implementation of most of the system logic required to implement a high performance IBM PC AT. The chip set is designed to offer a 100% PC AT compatible solution using only 27 components in addition to memory.

This document details how the four chips work together to provide 100% PC AT compatible solutions. It also provides an overview of the four chips: FE3001, FE3010B, FE3021, and FE3031. Clock generation, clock programming, bus programming, and control registers information is also provided.

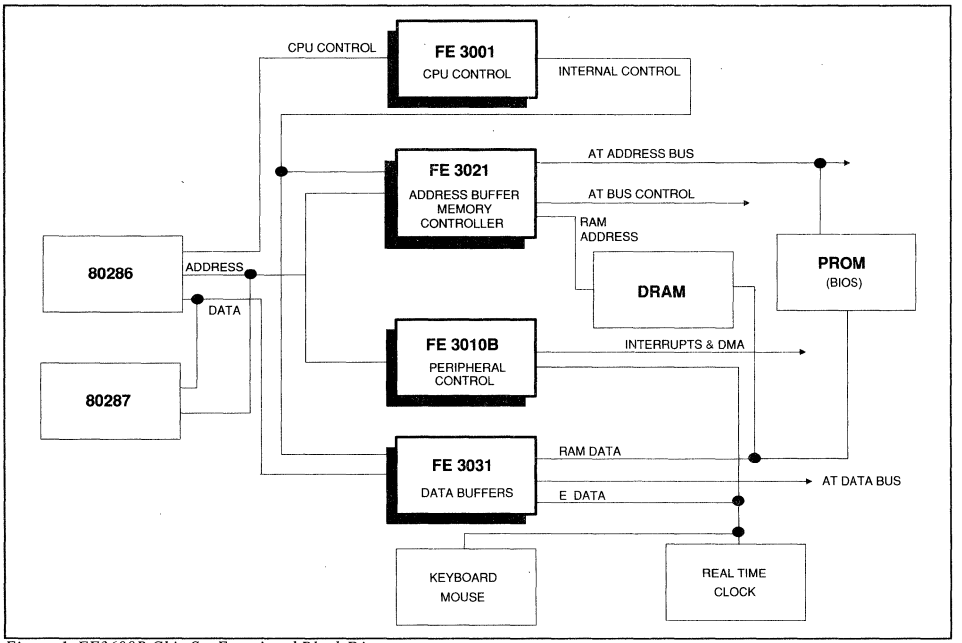

Figure 1. FE3600B Chip Set Functional Block Diagram

Additional References

IBM AT Technical Reference Manual
Intel Microprocessor and Peripheral Handbook*

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1.0 OVERVIEW

The FE3600B chip set provides all necessary core logic to build a totally integrated IBM AT compatible motherboard using the 16-bit Intel 80286 Central Processing Unit (CPU). The FE3600B chip set is 100% hardware (register level) and software compatible with the IBM PC/AT.

The FE3600B chip set consists of four devices:

- **FE3001 AT CPU Control Logic**
- **FE3010B AT Peripheral Control Logic**
- **FE3021 AT Address Bus Buffer**
- **FE3031 AT Data Bus Buffer**

Each of the four chips are covered in detail in separate Data Sheets.

2.0 REQUIRED COMPONENTS

The major components of an IBM PC AT compatible system using the FE3001, FE3010B, FE3021, and FE3031 are:

- **Intel 80286 CPU**
- **Intel 80287 Math Coprocessor**
- **W.D. CPU Control Logic (FE3001)**
- **W.D. AT Peripheral Logic (FE3010B)**
- **W.D. Address Buffer & Memory Controller (FE3021)**
- **W.D. Data Buffer (FE3031)**
- **Keyboard Controller (Intel 8042)**
- **Real Time Clock**

The design presented is fully compatible with the IBM PC AT system. The CPU Bus, the Expansion Bus, the Memory Bus, and I/O Bus are implemented in the same manner as in the IBM PC AT systems. All the peripherals and memories are decoded to match an IBM PC AT.

3.0 APPLICATIONS

The FE3600B is a highly-integrated chip set that allows designers to reduce chip count, increase flexibility, and provide improved operating speed and functionality for a 16 MHz IBM PC/AT compatible system board. The FE3600B chip set is extremely cost effective because it replaces approximately 60% of the components on a typical IBM AT motherboard and results in decreased size and power consumption. In addition, the FE3600B chip set devices are manufactured in surface-mountable packages which allows for a higher level of logic integration resulting in an extremely reliable device that occupies much less space.

4.0 FE3001 AT CONTROL LOGIC IC

The FE3001 contains all of the clock generation and cycle control logic necessary to implement an AT compatible computer. The salient features of the FE3001 are:

- **Programmable CPU, DMA, and system clock generation**
- **Programmable bus timing**
- **Programmable wait state generator**
- **Refresh and DMA controls**
- **Bus arbitration logic**
- **NMI generator and Parity error logic**
- **Reset/shutdown control**
- **Sleep mode**
- **80286 interface logic**

The FE3001 is also detailed in Section 8.0.

5.0 FE3010B AT PERIPHERAL CONTROL LOGIC

The Western Digital FE3010B AT and peripheral controller is a highly integrated chip with various control and peripheral functions. The FE3010B contains the functional equivalent of two 8237 DMA Controllers in cascade mode. This block improves the performance of the system by allowing external devices to transfer data directly from the system's memory.

The FE3010B also contains the functional equivalent of two 8259A Interrupt Controllers in cascade mode. A

total of 15 interrupts are supported including one from the time block. In addition, the FE3010B includes a functional equivalent of an 8254 timer. One channel is used to generate refresh request, one to generate sound for the speaker, and the other is tied to interrupt 0.

The FE3010B also contains a page register. It is used to generate address bits 16 to 23 for 8-bit DMA transfers and address bits 17 to 23 for 16-bit DMA transfers and refresh cycles.

6.0 FE3021 ADDRESS BUFFER & MEMORY CONTROLLER

The FE3021 is designed to reduce chip count, increase flexibility, and provide improved operating speed and functionality when used with the FE3001, FE3010B, and FE3031 to implement a low cost, high performance AT compatible computer. Chip count is reduced by integrating the memory controller, AT bus address buffers and I/O manager functions into one chip.

The memory controller is a high performance design with programmable modes of operation. It generates RAS and CAS signals for DRAM chips. It also provides control signals for Page Mode DRAM operation.

The Memory Controller portion has the capability to control page interleaved memory systems. It controls up to 4 banks of DRAM (up to 8 Mbytes) of memory. The DRAM bank locations are programmable on 128K boundaries. One memory bank allows split addressing so that one portion may be placed in real memory with the remainder in extended memory.

An additional major function of the FE3021 is to generate chip select decodes for peripheral chips on the system board; the floppy controller, hard disk controller, serial and parallel port chips. System operating speed may be optimized by tailoring the number of process wait states to each individual peripheral device.

Separate blocks of ROM may be mapped into a single physical ROM. The EGA BIOS and standard BIOS may be placed into a single 16-bit wide ROM. In addition to reduction of chip count, EGA operating speed will be increased since the EGA BIOS will be accessed at 16-bits at a time.

To reduce cost and board space, the video and system BIOS may be placed in a single 8-bit ROM. For highest operating speed, the video and system BIOS may be "shadowed" in RAM.

7.0 FE3031 AT DATA BUFFER

The FE3031 AT Data Buffer contains all of the data buffers necessary to implement an AT compatible computer. Its features include:

- **100 Pin PLCC design**
- **PC/AT Data Bus Buffers**
- **Peripheral Data Bus Buffer**
- **Memory Data Bus Buffers**
- **Parity Generator/Checker**
- **1.25 Micron CMOS Technology**

8.0 PROGRAMMING OF THE IBM PC/AT BUS

CLOCK GENERATION:

The FE3001 generates clock signals for the 80286, 80287 numeric processor, DMA, FE3010B, and the 8042 keyboard controller. There are three clock inputs to the FE3001: CLK16, CLKHS, and CLK14. The CLK16 is for 16 MHz oscillators, CLKHS is for 32 MHz or 40 MHz oscillators, and CLK14 is for 14.31 MHz oscillator inputs. The FE3001 generates six different clock signals: CPUCLK, DMACLK, PCLK, SYSCLK, TMRCLK, and 287CLK.

The user may select (with software) either CLK16 or CLKHS. As a result, CPUCLK and SYSCLK will change. The remaining four clocks will not change.

The CLK16 and CLKHS are provided to enable the 80286 to operate at up to 20 MHz while plug-in boards to the PC AT bus run up to 10 MHz. In essence, a motherboard designed with the FE3600B chipset (FE3001, FE3010B, FE3021 and FE3031) may be used with slower peripheral boards.

Although the FE3001 has two clock inputs, two oscillators are not necessary. The CLK16 is tied high with a pull-up resistor and the oscillator is connected to CLKHS. In this case, CLKHS ÷ 2 will be used for the CLK16 input (done internally). It is not possible to connect CLKHS high and connect CLK16 to an oscillator. The frequency of CPUCLK is either CLK16 or CLKHS depending on whether CLK16 or CLKHS is chosen.

The SYSCLK clock is used on the motherboard and is available on a PC AT Bus (B-20). The frequency of SYSCLK clock is either CLK16 ÷ 2 or CLKHS ÷ 4 depending on whether CLK16 or CLKHS is selected.

When CLKHS is selected, the phase of SYSCLK is dependent on ALE. When ALE is low, SYSCLK is equal to CPUCLK ÷ 4. When ALE is high, SYSCLK goes low when CPUCLK makes the high to low transition. When CLK16 is selected, SYSCLK is equal to CPUCLK ÷ 2, and does not depend on ALE. This scheme is used to insure that SYSCLK is synchronous to the command strobes and other bus signals.

The clock input CLK14 is a 14.31818 MHz input used to derive clock signals for the 8042 and FE3010B timer. The 8042 clock (PCLK and $\overline{\text{PCLK}}$) is fixed at 7.15 MHz and the timer clock is fixed at 1.19 MHz.

The DMA clock is programmable and is derived from CLKHS and CLK16. By writing in a register, the DMA clock can be set to either low or high speed. When CLKHS is selected for the CPU, the DMA CLK is CLKHS ÷ 8 or CLKHS ÷ 4. The user can choose between CLKHS ÷ 8 and CLKHSS ÷ 4 by writing in a register. When CLK16 is selected for the CPU, DMACLK is CLK16 ÷ 4 and CLK16 ÷ 2. The user can choose between CLK16 ÷ 4 and CLK16 ÷ 2 by writing in a register.

The clock for the 80287 (CLK287) is also generated by the FE3001. If CLKHS is chosen for CPU operation and CLK16 is tied to 5 V through a pull up resistor, then CLK = CLKHS ÷ 2. If CLK16 is not connected to 5 V and is selected, then CLK287 = CLK16. For example, if CLKHS = 32 MHz and CLK16 = 16 MHz, and CLK16 is selected, then CLK287 = 16 MHz. However, the 80287 does not function beyond 10 MHz so a divide-by-three method must be used resulting in roughly 5 MHz 80287 operation.

To use the 80287 at 10 MHz, the CPUCLK from the FE3001 may be more suitable than CLK287 as it can be divided down to 8 or 10 MHz. For power consumption when the system is temporarily not in use, the FE3001 can be put in a sleep mode (bit 6 of port 063H high). In this mode, all clocks will be off except the 8042 and FE3010B timer clocks. These clocks are used for refresh timing and keyboard interface logic. Sleep mode is exited by pulsing the CPURES input of the FE3001.

9.0 PROGRAMMING CLOCKS

The speed select register controls the speed of the CPU and DMA clocks. This speed select register resides in I/O space and is an 8-bit with address 063H. It is a write-only register and can be written with an I/O command. The address 063H is defined to accomplish this task. Bits 0, 1, 4, and 5 are not used. When bit 2 is low, CLK16 is selected; otherwise CLKHS is selected. When bit 3 is low, the DMA clock is at 4 MHz, otherwise it is 8 MHz. The speed selector register is used to initiate the sleep mode. When bit 6 is at logic high, all of the clocks (except the timer clock) are stopped, allowing refresh to continue. Bit 7 is used to unlock and write other registers in the FE3000A. The speed select register is cleared by a system reset. To exit the sleep mode, the pulsing of the CPURES input of the FE3001 (by external hardware) is required.

10.0 BUS PROGRAMMING

PC AT Bus programming is required due to the CPU 80286 running at up to 16 MHz and the fact that the PC AT Bus is designed for up to 8 MHz operations. The control/command signals from the motherboard should be delayed to conform up to 8 MHz specifications.

The programmed signals are BALE, IOW, IOR, MEWR, and the number of wait states. All programming is handled through registers in the FE3001.

11.0 PROGRAMMABLE REGISTERS

Table 1 contains registers, functions, waveforms, and default parameters. There are 13 registers (R0 to R12) which handle the programming of various bus signals. These registers are controlled through two registers; point register, address 072H, and data register, address 073H. Both are write-only registers, located in I/O space .

The pointer register contains the address of one of 14 registers. Not all 8 bits in the pointer are used (bit 0, 1, 4, and 5 are unused). The remaining four bits (bit 2, 3, 6, and 7) form the address with bit 7 as MSB and bit 2 as LSB.

EXAMPLE: If bits 2, 3, 6, and 7 are 0, 1, 0, and 1 respectively, the address is 10 (decimal). It is pointing to register R (see Table 1). If all four bits are zero, R is being pointed at 0.

The data register, address 073H, contains data to be written into one of Ro-12 register. Not all eight bits of the data registers are used (bits 0, 1, 4, and 5 are not used). Bits 2, 3, 6, and 7 form 4-bit data with bit 2 as LSB and bit 7 as MSB.

REG	FUNCTION	DEFAULT
R_0	BALE delay from ALE leading edge	0
R_1	BALE width	1
R_2	NOT USED	
R_3	8-bit memory, 8/16-bit I/O - cmd delay	1
R_4	8-bit operation - wait states	4
R_5	16-bit I/O operation - wait states	1
R_6	16-bit memory operation - command delay	0
R_7	16-bit memory operation - wait states	1
R_8	16-bit memory operation - wait states	0
R_9	Local DRAM read operation - wait states	0
R_{10}	Local DRAM write operation - wait states	1
R_{11}	Local DRAM write operation - cmd delay	0
R_{12}	On-board I/O operation - command delay	1

Table 1. Summary of Command Timing Reference