

*WD16C451, WD16C551*

*Enhanced Asynchronous*

*Communications Element (ACE)*

*with Parallel Port*



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## 1.0 INTRODUCTION

### 1.1 DESCRIPTION

The low-power CMOS WD16C451/WD16C551 is a single-device solution for serving one serial I/O port and one bidirectional parallel port on the IBM PC, PC XT, PC AT, PS/2, and compatible systems. The WD16C451/WD16C551 is an enhanced ACE with a bidirectional parallel port. The ACE performs parallel-to-serial conversion on output and serial-to-parallel conversion on input. It is programmable, independent, and has a maximum recommended data rate of 512K baud.

The WD16C451 family (WD16C451, WD16C451A, WD16C451B) is a WD16C450 ACE plus a bidirectional parallel data port.

The WD16C451 and WD16C451A parallel port supports a Centronics-compatible printer interface. The parallel port, together with the serial port, provides IBM PC XT, PC AT and compatibles with a single-device solution for serving both ports. The WD16C451A is further enhanced by its crystal input capability.

The WD16C451B, also enhanced by its crystal input capability, supports a PS/2-compatible printer port interface. The parallel port, together with the serial port, provides IBM PS/2 and compatibles with a single-device solution for serving both ports.

The WD16C551 is a WD16C550 Enhanced ACE plus a compatible PS/2 bidirectional parallel port. After power-up and hardware reset, the ACE is functionally compatible with WD16C450 (Character Mode). The ACE in the WD16C551 has been enhanced with 16-byte FIFO buffers on both the receive and transmit lines, allowing an additional mode of operation called FIFO Mode. The FIFO Mode, only available in WD16C551, can be activated through software, relieving CPU of interrupt overhead. Buffering of data also allows greater latency time in interrupt servicing, which is vital in multitasking environments. The WD16C551 also has DMA signaling between the FIFO buffers and host CPU allowing single-character or multicharacter transfers. The recommended maximum data rate is 512 Kbaud with an 8.0 MHz clock rate. The PS/2 parallel port, together with the serial port, provides IBM PS/2 and compatibles with a single-device solution for servicing both ports.

### 1.2 FEATURES

- Fully programmable serial interface characteristics including:
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no parity bit generation/detection
  - 1, 1-1/2, or 2 stop-bit generation
  - DC to 512 Kbaud rate generation
- Tri-state TTL drive capabilities for bidirectional data bus and control bus
- Loopback controls for communications link fault isolation
- Line break generation and detection
- False start-bit detection

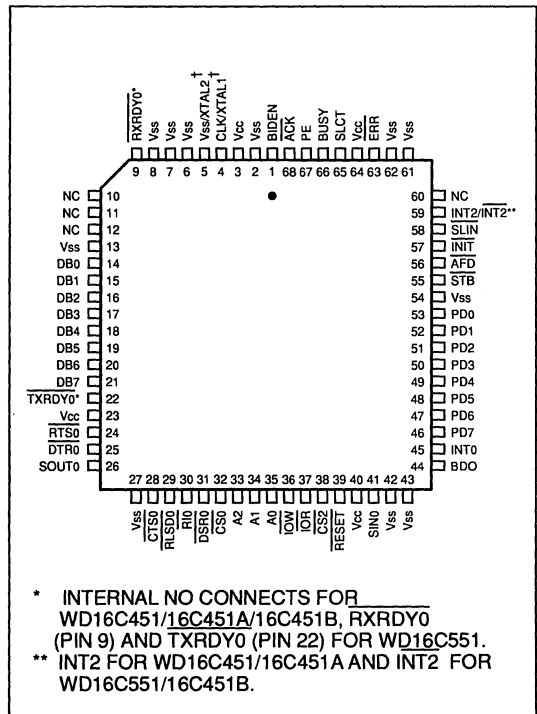


FIGURE 1-1. 68-PIN QUAD



- Complete status reporting capabilities
- Generation and stripping of serial asynchronous data control bits (start, stop, parity)
- Programmable baud rate generator and MODEM control signals
- Fully prioritized independent interrupt system controls
- CMOS implementation for high-speed, low-power requirements
- 68-pin QUAD package

**AVAILABLE VERSIONS****WD16C451 with:**

- Centronics (PC/AT) compatible bidirectional parallel port for direct printer interface

**WD16C451A with:**

- Centronics (PC/AT) compatible bidirectional parallel port for direct printer interface
- Crystal-controlled external clock input

**WD16C451B with:**

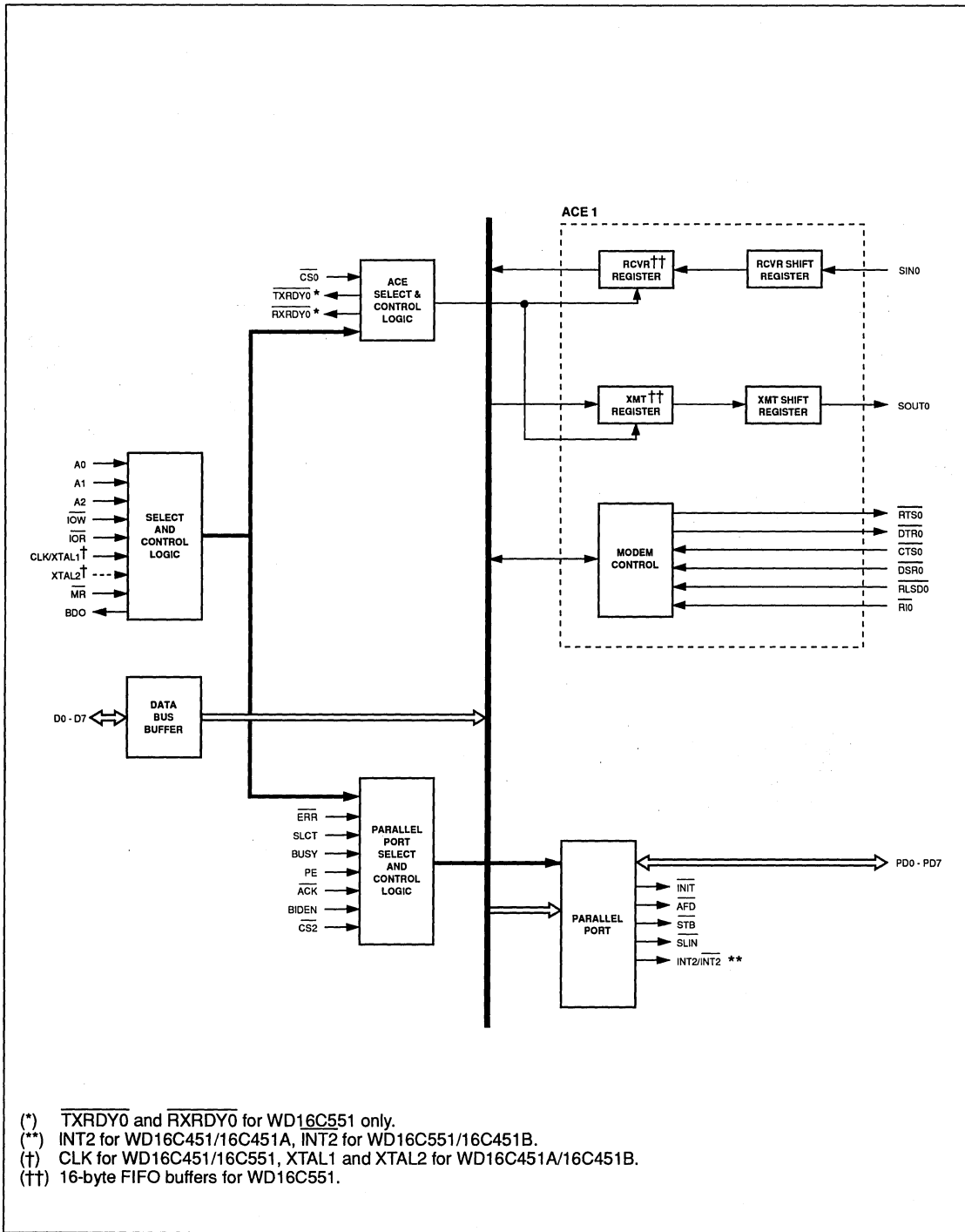
- PS/2-compatible bidirectional parallel port
- Crystal-controlled external clock input

**WD16C551 with:**

- PS/2-compatible bidirectional parallel port
- 16-byte transmit and receive FIFO buffers for CPU relief during high-speed data transfer
- Programmable 1-, 4-, 8-, or 14-byte FIFO threshold levels on each receive channel
- Two modes of DMA signaling for transfer of data characters to and from FIFO buffers







(\*) TXRDY0 and RXRDY0 for WD16C551 only.  
 (\*\*) INT2 for WD16C451/16C451A, INT2 for WD16C551/16C451B.  
 (†) CLK for WD16C451/16C551, XTAL1 and XTAL2 for WD16C451A/16C451B.  
 (††) 16-byte FIFO buffers for WD16C551.

FIGURE 1-2. WD16C451/WD16C551A BLOCK DIAGRAM



## 2.0 SIGNAL DESCRIPTIONS

Figure 2-1 illustrates the 68-Pin QUAD assembly. Table 2-1 lists all signal descriptions.

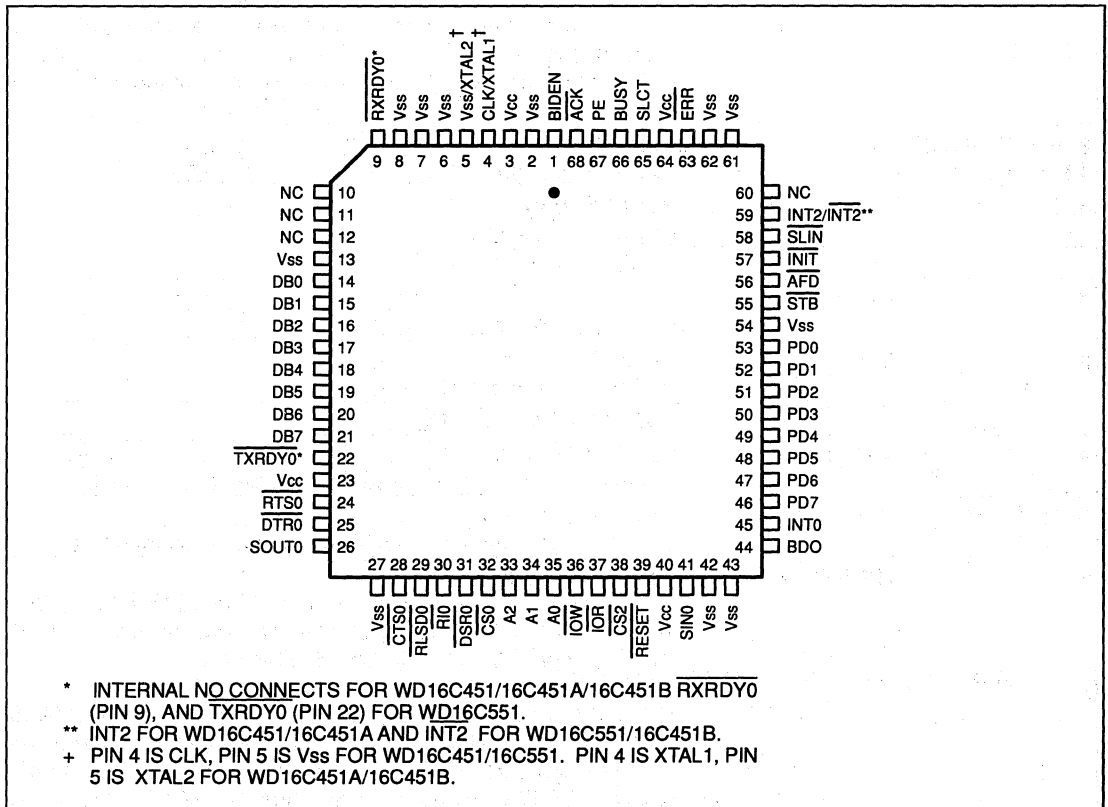


FIGURE 2-1. WD16C451/WD16C551 68-PIN QUAD ASSEMBLY PIN DESIGNATIONS



PIN	MNEMONIC	DESCRIPTIONS
1	BIDEN	<b>Bidirectional Enable</b> Input signal in WD16C451/16C451A when low enables the parallel port data lines as outputs. When high, the WD16C451/16C451A will hold the parallel port data pins in a high-impedance state, allowing these pins to be driven with data. The BIDEN input signal on the WD16C551/16C451B works in conjunction with the DIR bit (see Table 6-3) to control the direction of the parallel port data bit.
2, 6-8, 13, 42, 27, 43, 54, 61, 62	Vss	<b>Ground</b> System signal ground.
3, 23, 40, 64	Vcc	<b>Power Supply</b> +5V power supply.
<i>WD16C451/16C551</i>		
4	CLK (Times 1)	<b>Clock Input</b> External clock input.
5	Vss	<b>Ground</b> System signal ground.
<i>WD16C451A/16C551B</i>		
4	XTAL1	<b>External Clock In</b> Connects the crystal to the ACE baud rate divisor circuit.
5	XTAL2	<b>External Clock Out</b> Connects the crystal to the ACE baud rate divisor circuit.
9	RXRDY0 ♦	<b>Receiver Ready</b> Receiver ready output is used to signal DMA transfer to the CPU from the ACE. Two modes of operation are available in FIFO Mode, and one (Mode 0) in Character Mode.  Mode 0: When in Character Mode (FCR0=0), or in the FIFO Mode (FCR0=1) with FCR3=0, RXRDY will be active (low) if there is at least one character in the RCVR holding register or RCVR FIFO register. RXRDY will go inactive when the RCVR FIFO buffer (FIFO Mode), or holding register (Character Mode) is empty.  Mode 1: In FIFO Mode (FCR0=1) with FCR3=1, $\overline{\text{RXRDY}}$ will go active (low) when the trigger level or time out has been reached. RXRDY goes inactive (high) when the FIFO buffer is empty.
(♦) These pins are internal no-connects on the WD16C451.		

TABLE 2-1. SIGNAL DESCRIPTIONS



PIN	MNEMONIC	DESCRIPTION
10-12	NC	<b>No connection</b> Internally not connected.
14-21	DB0-DB7	<b>Data Bits</b> Tri-state, bidirectional communication lines between the internal registers and Data Bus. D0 is the LSB and the first serial transmitted or received bit.
22	TXRDY <sup>♦</sup>	<b>Transmitter Ready FIFO Control</b> Transmit ready output is used to signal DMA transfer to the CPU from the ACE. Two modes of operation are available when using FIFO Mode, and one (Mode 0) when using Character Mode.  Mode 0: In Character Mode (FCR0=0) or in FIFO Mode (FCR0=1) with FCR3=0, TXRDY will be active (low) if there are no characters in the Xmit FIFO buffer (FIFO Mode) or Xmit holding register (Character Mode). TXRDY will go inactive after the first character is loaded.  Mode 1: In FIFO Mode (FCR0=1) with FCR3=1, if there is one or more <u>unfilled</u> position in the Xmit FIFO TXRDY0 will be active (low). TXRDY0 goes inactive when the FIFO buffer is completely full.
24	RTS0	<b>Request to Send</b> Output when low informs the MODEM or data set that the ACE is ready to transmit data. This value is reflected in bit 1 of the MODEM Control Register.
25	DTR0	<b>Data Terminal Ready</b> Output when low informs the MODEM or data set that the ACE is ready to receive. This value is reflected in bit 0 of the MODEM Control Register.
26	SOUT0	<b>Serial Data Output</b> Transmitted Serial Data Out to the communication link from the ACE. SOUT is set to a marking condition (logical 1) on a Master Reset.
28	CTS0	<b>Clear to Send</b> Input from DCE to the ACE indicating remote device is ready to transmit. This value is reflected in bit 4 of the MODEM Status Register.

(♦) These pins are internal no-connects on the WD16C451.

TABLE 2-1. SIGNAL DESCRIPTIONS (Continued)



PIN	MNEMONIC	DESCRIPTION
29	RLSD0	<b>Received Line Signal Detect</b> Input from the DCE indicating that the ACE is receiving a signal that meets its signal quality conditions. Bit 3 of the MODEM Status Register reflects this value.
30	RIO	<b>Ring Indicator</b> Input when low indicates a ringing signal being received by the MODEM or data set. This logical value is reflected in bit 6 of the MODEM status Register.
31	DSR0	<b>Data Set Ready</b> When low, this input signal from the communication link indicates that it is ready to exchange data with the ACE. Bit 5 of the associated MODEM Status Register reflects the DSR logical state.
32	CS0	<b>Chip Select 0</b> Chip Select input when active (low) selects serial channel 0.
33 thru 35	A2, A1, A0	<b>Address lines A2-A0</b> These three inputs are used to select an internal register of the ACE, or parallel port.
36	IOW	<b>Input/Output Write Strobe</b> Input when active (low), causes data from the data bus (DB0-DB7) to be input to the selected port's addressed register. The data will be written to the register chosen by A0-A2 and the port is chosen by CS0 or CS2 to be ACE parallel port, respectively.
37	IOR	<b>Input/Output Read Strobe</b> Input active (low) will display data from the selected internal register on the data bus DB0-DB7. The chip select line determines within which port the register being accessed resides, and A0-A2 choose the internal register to be read.
38	CS2	<b>Chip Select 2</b> Chip Select input when active (low), enables the line printer port.
39	Reset	<b>Reset</b> Input when active (low), will force the device into an idle mode where all serial data activity is suspended. The device will remain in an idle state until programmed to begin data activities.
41	SIN0	<b>Serial Data Inputs</b> Received Serial Data Input from the communication link to the ACE. Data on the serial data inputs are disabled when exercising loopback mode, and internally connected to their respective SIN lines.

TABLE 2-1. SIGNAL DESCRIPTIONS (Continued)



PIN	MNEMONIC	DESCRIPTION
44	BDO	<b>Bus Buffer Output</b> Output goes active when either the serial channel or the parallel port is serial channel or the parallel port is selected as an output. BDO is used to control the system bus driver device (74LS245).
45	INT0	<b>Serial Channel Interrupt</b> Tri-state output (enabled by bit 3 of MCR) goes high whenever an enabled interrupt is pending. INT is reset when the pending interrupt(s) are serviced, or a Master Reset is performed.
46-53	PD7-PD0	<b>Parallel Data Bits</b> Bidirectional data port which provides parallel input and output to the system. The 8 lines are held in a high impedance state when BIDEN is high.
55	STB†	<b>Line Printer Strobe</b> Output line, when active, provides the line printer with a signal to latch the data currently on the parallel port.
56	AFD†	<b>Line Printer Autofeed</b> Output line, when active, provides a signal for the line printer to autofeed continuous form paper.
57	INIT†	<b>Line Printer Initialize</b> Output line to printer, when active (low), signals the line printer to begin an initialization routine.
58	SLIN†	<b>Line Printer Select</b> Output line, when active (low), selects the printer.
59	INT2/INT2††	<b>Interrupt Printer Port</b> Tri-state output enabled by bit 4 of WCR. For the WD16C451/16C451A, INT2 goes active high on the rising transition of ACK and reset (low) on the falling transition of ACK. For the WD16C551/16C451B, INT2 goes active low on the rising edge of ACK. INT 2 is reset (high) on the rising edge of IOR, when reading the parallel port status register.
60	NC	<b>No connection</b> Internally not connected.
63	ERR	<b>Line Printer Error</b> Input line from the line printer, informs the parallel port of an error by inputting an active low signal. Set low by the printer upon a deselect condition, PE, or other error condition.
(†) These outputs are open drain with internal pull-ups. (††) This pin is INT2 fro WD16C451/16C451A and INT2 for WD16C551/16C451B.		

TABLE 2-1. SIGNAL DESCRIPTIONS (Continued)



PIN	MNEMONIC	DESCRIPTION
65	SLCT	<b>Line Printer Select</b> Input from the line printer that goes high when the line printer has been selected.
66	BUSY	<b>Line Printer Busy</b> Input from the line printer that goes high when the line printer has an operation in progress.
67	PE	<b>Line Printer Paper Empty</b> Input from the line printer goes high when the printer is out of paper.
68	ACK	<b>Line Printer Acknowledge</b> Input from the line printer that goes low to confirm the data transfer from the WD16C451/16C551 to the printer was successful.

TABLE 2-1. SIGNAL DESCRIPTIONS (Continued)



### 3.0 SERIAL CHANNEL REGISTERS

#### 3.1 SERIAL PORT REGISTER ADDRESSING

Chip Select ( $\overline{CS0}$ ): When  $\overline{CS0}$  is low, registers for the serial channel can be accessed.

##### Master Reset:

A low level input on this pin causes the ACE to reset to the condition listed in Table 3-1.

##### Software Reset:

A software reset is performed by writing to the Divisor Latches, forcing the transmitter and receiver to an Idle Mode. (Registers are not reset by this operation.) Prior to enabling interrupts, the LSR and RBR registers should be read to clear out any data. This is used to

return to a known state without resetting the system.

Chip Select ( $\overline{CS0}$ ) and register select (A0, A1, A2) signals must be stable for the duration of a read or write operation.

Register Select (A0, A1, A2): To select a register for read or write operation, see table 2-1

##### NOTE:

Divisor Latch Access Bit (DLAB) is the MSB of the Line Control Register. DLAB must be programmed high (logic 1) by the system software to access the Baud Rate Generator Divisor Latches.

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer Register (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable Register
X	0	1	0	Interrupt Identification Register (read only)
X	0	1	0	FIFO Control Register (write only)
X	0	1	1	Line Control Register
X	1	0	0	MODEM Control Register
X	1	0	1	Line Status Register (read only)
X	1	1	0	MODEM Status Register
X	1	1	1	Scratch Pad Register
1	0	0	0	Divisor Latch Register (least significant byte)
1	0	0	1	Divisor Latch Register (most significant byte)

TABLE 3-1. REGISTER ADDRESSING





## 4.0 ACE OPERATIONAL DESCRIPTION

### 4.1 MASTER RESET

A low-level input on this pin causes the ACE to reset to the condition listed in Table 4-1.

### 4.2 ACE ACCESSIBLE REGISTERS

The system programmer has access to any of the registers as summarized in Table 4-2. For individual register descriptions, refer to the following pages under register heading.

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High and Bits 1-3; 6 and 7 are forced Low. Bits 4 and 5 are permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, except Bits 5 and 6 are High
MODEM Status Register	Master Reset	Bits 0-3 Low, Bits 4-7 at Input Signal
Divisor Latch (low order byte)	Writing into the Latch	Data
Divisor Latch (high order byte)	Writing into the Latch	Data
SOUT	Master Reset	High
BDO	$BDO = RCLK \cdot IOR$ (At Master Reset, the CPU sets RCLK and IOR = Low when device is selected.)	High
INT0 (RCVR ERRS)	Master Reset/Read LSR	Low
INT0 (RCVR DATA READY)	Master Reset/Read RBR	Low
INT2 (WD16C451/WD16C451A)	Master Reset/ACK (High)	Low
INT2 (WD16C551/WD16C451B)	Master Reset/Read PPSR	High
RTS	Master Reset	High
DTR	Master Reset	High
RCVR FIFO Counter (WD16C551 Only)	MR or FCR1 • FCR0 or $\Delta FCR0$	All Bits Low
XMIT FIFO Counter (WD16C551 only)	MR or FCR1 • FCR0 or $\Delta FCR0$	All Bits Low
FIFO CONTROL (WD16C551 only)	Master Reset	All Bits Low
D7 - D0 Data Bus Lines	In Tri-state Mode, Unless IOR = Low or IOW = Low when Device is Selected	Tri-state Data (ACE to CPU) Data (CPU to ACE)

TABLE 4-1. RESET CONTROL OF REGISTERS AND PINOUT SIGNALS



REGISTER ADDRESS						
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	2	3
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register
0	Data Bit 0	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending (IP)	FIFO Enable (Write Only) (FEWO)	Word Length Select Bit 0 (WLS0)
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 0 (IIDB0)	Rcvr FIFO Reset (RFR)	Word Length Select Bit 1 (WLS1)
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ERLSI)	Interrupt ID Bit 2 (IIDB2)	Transmitter FIFO Reset (TFR)	Number of Stop Bits (STB)
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	Interrupt ID Bit 3 (IIDB3) *	DMA Mode Select (DMS)	Parity Enable (PEN)
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity (STP)
6	Data Bit 6	Data Bit 6	0	FIFO Enabled* (READ ONLY) (FERO)	Rcvr FIFO Trigger Level (LSB)(RTLBSB)	Set Break Control (SBR)
7	Data Bit 7	Data Bit 7	0	FIFO Enabled* (READ ONLY) (FERO)	Rcvr FIFO Trigger Level (MSB) (RTMSB)	Divisor Latch Access Bit (DLAB)

( \* ) These bits are 0 in Character Mode.

TABLE 4-2. ACCESSIBLE WD16C451/WD16C551 REGISTERS



REGISTER ADDRESS						
	4	5	6	7	0 DLAB=1	1 DLAB=1
Bit No.	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Pad Register	Divisor Latch (LSB)	Divisor Latch (MSB)
0	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Not Connected (NC)	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Interrupt (Int)	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 3	Bit 11
4	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	0	Error in RCVR FIFO (EIRF)	Received Line Signal Detect (RLSD)	Bit 7	Bit 7	Bit 15

(♦) These bits are 0 in Character Mode.

TABLE 4-2. ACCESSIBLE WD16C451/WD16C551 REGISTERS (Contd)



### 4.3 LINE CONTROL REGISTER

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 are as follows:

Bit 1	Bit 0	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Bit 2: This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1-1/2 Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (Transmit data) or checked (Receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1's when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced

to the Spacing (logic 0) state and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

### 4.4 ACE PROGRAMMABLE BAUD RATE GENERATOR

The ACE contains a programmable Baud Rate Generator capable of taking any clock input (dc to 8.0 MHz) and dividing it by any divisor from 1 to ( $2^{16} - 1$ ). The output frequency of the Baud Generator is 16X the baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 4-3, 4-4, and 4-5 illustrate the use of the Baud Generator with three different driving frequencies. One is referenced to a 1.8432 MHz clock. Another is a 3.072 MHz clock. The third is an 8.0 MHz clock.

#### NOTE:

The maximum operating frequency of the Baud Generator is 8.0 MHz.

In no case should the data rate be greater than 512K baud.



Desired Baud Rate	Divisor Used to Generate 16 Times Clock	Percent Error Difference Between Desired and Actual
50	2304	--
75	1536	--
110	1047	0.026
134.5	857	0.058
150	768	--
300	384	--
600	192	--
1200	96	--
1800	64	--
2000	58	0.690
2400	48	--
3600	32	--
4800	24	--
7200	16	--
9600	12	--
19200	6	--
38400	3	--
56000	2	2.860

TABLE 4-3. BAUD RATES USING 1.8432 MHz CLOCK

Desired Baud Rate	Divisor Used to Generate 16 Times Clock	Percent Error Difference Between Desired and Actual
50	3840	--
75	2560	--
110	1745	0.026
134.5	1428	0.034
150	1280	--
300	640	--
600	320	--
1200	160	--
1800	107	--
2000	96	--
2400	80	--
3600	53	0.628
4800	40	--
7200	27	1.230
9600	20	--
19200	10	--
38400	5	--
56000	3	14.285

TABLE 4-4. BAUD RATES USING 3.072 MHz CLOCK



Desired Baud Rate	Divisor Used to Generate 16 Times Clock	Percent Error Difference Between Desired and Actual
50	10000	--
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	--
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.344

TABLE 4-5. BAUD RATES USING 80.0 MHz CLOCK



#### 4.5 LINE STATUS REGISTER

This 8-bit read only register provides status information to the CPU concerning the data transfer. Its contents are indicated in Table 4-2 and are described below.

**Bit 0:** This bit is the Receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register, or to the RCVR FIFO (when in FIFO Mode). Bit 0 will be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register (for Character Mode) or by writing a logic 0 into it from the CPU.

In FIFO Mode Receiver Data Ready is set when the receiver shift register is loaded into the FIFO and reset when the receiver FIFO is empty.

**Bit 1:** This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

When in FIFO Mode an OE occurs after the RCVR FIFO is full and the receiver shift register has completely received the next character. An OE is indicated to the CPU as soon as it happens. The character in the shift register will be written over, but nothing will be transferred to the FIFO.

**Bit 2:** This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to logic 0 whenever the CPU reads the contents of the Line Status Register.

When in FIFO Mode a parity error is associated with a particular character in the FIFO buffer, and revealed to the CPU when the associated character is in the top of the FIFO buffer.

**Bit 3:** This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop Bit. Bit 3 is set to a logic 1 whenever the Stop Bit following the last data bit or parity bit is detected as a zero bit (Spacing Level). When in FIFO Mode, an FE is associated with a

particular character in the FIFO buffer, and revealed to the CPU when the associated character is in the top of the FIFO buffer.

**Bit 4:** This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time (that is, the total time of Start Bit + data bits + Parity + Stop Bits). Bit 4 is reset to logic 0 whenever the CPU reads the contents of the Line Status Register. Restarting after a break is received requires the SIN pin be high for at least one-half bit time.

When in FIFO Mode BI is associated to the particular character in the FIFO buffer, and this bit is set when the associated character is in the top of the FIFO buffer.

#### NOTE:

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and Receiver Line Status interrupt is enabled. All bits except bit 7 of the Status Register can be set or reset by writing to the register.

**Bit 5:** This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the ACE is ready to accept a new character for transmission. This bit also causes the ACE to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

When in the FIFO Mode this bit will be set when the XMIT FIFO is empty, and cleared after at least one character is written into the XMIT FIFO buffer. The Transmitter FIFO Empty indications will be delayed one character time minus the last Stop bit time whenever the following occurs: the Transmitter FIFO buffer is empty and there have not been at least two characters in the Transmitter FIFO buffer at the same time since the last time that Transmitter FIFO buffer was empty. The first transmitter interrupt after changing the first bit of the FIFO Control Register will be immediate if it is enabled.

**Bit 6:** This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 when both transmitter registers (Transmitter Holding Register and



Transmitter Shift Register) are idle (empty). It is reset to a logic 0 upon loading of data into the Transmitter Holding Register.

In FIFO Mode this bit is set when the XMIT FIFO buffer and SMIT Shift Register are both empty. It is cleared when at least one byte is written into the XMIT FIFO.

Bit 7: This bit (LSR7) is 0 when in Character Mode. When in FIFO Mode, this bit is a one if there is at least one parity error, framing error or break indication in the FIFO buffer. LSR7 is cleared when this register is read as long as there are no addition errors in the FIFO buffer.

#### 4.6 INTERRUPT IDENTIFICATION REGISTER

The ACE has an interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the ACE prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and source of that interrupt is stored in the Interrupt Identification Register (refer to Table 3-2)

This register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. Its contents are indicated in Table 3-6 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 through 3: These three bits are used to identify the highest priority interrupt pending (see Table 3-6).

Bits 4 and 5: These bits are always logic 0.

Bits 6 and 7: These bits, when set, indicate that the device is in FIFO Mode (FCR0 = 1).





INTERRUPT IDENTIFICATION REGISTER				INTERRUPT SET AND RESET FUNCTIONS			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	0	1	--	None	None	--
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
1	1	0	0	Second	Character Timeout Identification	No Characters have been input or removed from RCVR FIFO buffer during the last four character times, and at least one character occupies it during this time.	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

TABLE 4-6. INTERRUPT CONTROL FUNCTIONS



#### 4.7 INTERRUPT ENABLE REGISTER

This 8-bit register enables the four interrupt sources of the ACE to separately activate the device Interrupt (INT) output signal, when bit 3 of MCR is a logic 1. Its contents are indicated in Table 3-2 and are described below. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INT output from the device. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

#### 4.8 SCRATCH PAD REGISTER

This 8-bit register does not control or report status on any part of the ACE. It is a read/write register that can be used by the programmer to as a general purpose register.

#### 4.9 FIFO CONTROL REGISTER

This write only register is located at the same address as the IIR (read only). This register is used to enable FIFO Mode, clear FIFO buffers, set the RCVR FIFO trigger levels, and select the mode of DMA signaling.

Bit 0: Writing a one to this bit enables the XMIT and RCVR FIFO buffers. When changing from Character Mode to FIFO Mode and vice versa, data in the FIFO buffers does not automatically clear. Resetting FCR0 will clear all characters from RCVR Error FIFO. The FIFOs should be cleared immediately after changing to FIFO mode. This bit must be a 1 before writing to other FCR bits or they will not be programmed.

Bit 1: Writing a 1 to FCR1 will clear all bytes from RCVR Error FIFO and reset its counters to 0, and then self clear this bit to 0. The shift register and RCVR FIFO are not cleared.

Bit 2: Functions the same as bit 1, but for XMIT FIFO.

Bit 3: If FCR0 = 1, setting FCR3 to a 1 will cause the RXRDY and TXRDY pins to change from Mode 0 to Mode 1 (See pin description of RXRDY and TXRDY).

Bits 4 and 5: Reserved for future use.

Bits 6 and 7: These bits control the trigger level of the RCVR FIFO interrupt.

7	6	RCVR FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14



## 5.0 MODEM CONTROL REGISTER

This 8-bit register controls the interface either with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table 4.2

**Bit 0:** This bit controls the Data Terminal Ready (DTR) output. When bit 0 is set to a logic 1, the DTR output is forced to a logic 0. When bit 0 is reset to a logic 0, the DTR output is forced to a logic 1.

### NOTE:

The DTR output of the ACE may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

**Bit 1:** This bit controls the Request to Send (RTS) output. Bit 1 affects the RTS output in a manner identical to that described above for bit 0.

**Bit 2:** No connect. In loopback mode this bit is connected to the MODEM Status Register bit 6.

**Bit 3:** This bit enables the INT output pin. When this bit is a logic 0 the INT output pin is tri-stated. In loopback mode this bit is connected to bit 7 of the MODEM Status Register.

**Bit 4:** This bit provides a loopback feature for diagnostic testing of the ACE. When bit 4 is set to logic 1, the following occurs: the transmitter Serial Output (SOUT) is set to a logic 1 (high) state; the receiver Serial Input (SIN) is disconnected; the

output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control Inputs (CTS, DSR, RLSD, and RI) are disconnected; and the four MODEM Control outputs (0-3) are internally connected to the four MODEM Control inputs. The INT output pin is tri-stated when in loopback mode. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the ACE.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The ACE MODEM interrupt system can be tested by writing into the lower four bits of the MODEM Status Register. The resetting of these interrupts is the same as in normal ACE operation. To return to this operation, the registers must be reprogrammed for normal operation and then bit 4 must be reset to a logic 0.

**Bits 5 through 7:** These bits are permanently set to a logic 0

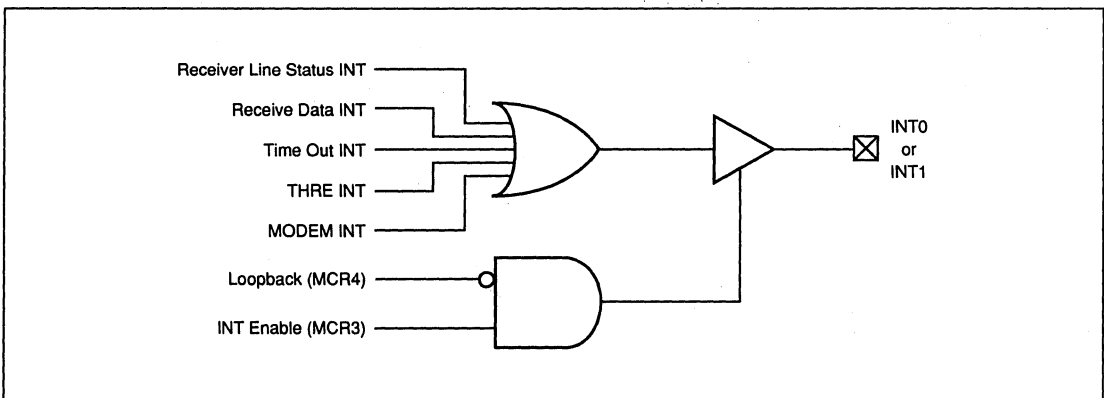


FIGURE 5-1. INTERRUPT SIGNAL LOGIC

## 6.0 MODEM STATUS REGISTER

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. Besides this information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 3.2 and are described below.

**Bit 0:** This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the CTS input to the device has changed state since the last time it was read by the CPU.

**Bit 1:** This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the DSR input to the device has changed since the last time it was read by the CPU.

**Bit 2:** This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the RI input to the device has changed from an On (logic 1) to an Off (logic 0) condition.

**Bit 3:** This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the RLSD input to the chip has changed state.

**NOTE:** Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

**Bit 4:** This bit is the complement of the Clear to Send (CTS) input. This bit becomes equivalent to RTS of the MODEM control register, if Bit 4 of the MODEM control register is set to 1.

**Bit 5:** This bit is the complement of the Data Set Ready (DSR) input. This bit becomes equivalent to DTR of the MODEM control register, if Bit 4 of the MODEM control register is set to 1.

**Bit 6:** This bit is the complement of the Ring Indicator (RI) input. This bit becomes equivalent to Bit 2 of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

**Bit 7:** This bit is the complement of the Received Line Signal Detect (RLSD) input. This bit becomes equivalent to Bit 3 of the MODEM Control Register, if Bit 4 of the MODEM Control Register is set to 1.

### 6.1 FIFO INTERRUPT MODE OPERATION NOTES

When FCR0=1 and IER0=1 the following RCVR interrupts will occur:

1. A FIFO timeout interrupt occurs when:
  - a. There is at least one byte in the RCVR FIFO buffer
  - b. No character has been received in 4 continuous character times (if 2 stop bits are being used the second one is included in this time delay).
  - c. The most recent CPU read from the FIFO buffer has exceeded 4 continuous character times.

The timeout counter is proportional to the baud rate. After a timeout interrupt, the interrupt is cleared and the timer is reset when the CPU reads a character from the RCVR FIFO.

2. When the RCVR FIFO buffer reaches its programmed trigger level the receive data interrupt is set. This interrupt is cleared as soon as the FIFO buffer level falls below the trigger level.

### 6.2 FIFO POINTER NOTES

The RCVR FIFO has an internal pointer that automatically points to the RCVR Data byte to be read and the associated Status byte. Reading the RCVR Data byte will increment the internal counter, whereas reading the Status byte will not. The Status byte should always be read prior to the Data byte associated with it.



### 6.3 FIFO POLLING MODE OPERATION NOTES

This mode is initialized when FCR0=1 and IER0, IER1, IER2, and IER3 are all 0. In polling mode the user must poll the LSR to check the transmitter and receiver status. Since the receiver and transmitter

are controlled separately either one or both can be in polling mode.

There is no trigger level reached or timeout condition indicated in the FIFO Polling Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.



### 7.0 PARALLEL PORT DESCRIPTION

The parallel port supports Centronics-type printers. When CS2 is low, the parallel port is selected allowing access to all parallel port control and status registers. (Refer to Tables 7-1 and 7-2.)

**Register Descriptions:**

**Read Port Register**

Bits 0 through 7: These bits correspond to the data on the parallel bus. This register is used to read the data from the parallel bus.

**Read Status Register**

Bits 0 through 1: These bits are set to a logic one.

Bits 2: This bit represents the status of the

$\overline{\text{INT}}$  pin. This bit is only available in the WD16C551/ WD16C451B.

Bits 3 through 7: These bits represent the status of the corresponding pins. Refer to Table 7-2.

**Read Control Register**

Bits 0 through 3: These bits show the status of the corresponding pins. Refer to Table 7-2.

Note: These values reflect the signal on the open drain outputs, not necessarily the value in the write control register.

A1	A0	$\overline{\text{IOR}}$	$\overline{\text{IOW}}$	REGISTER
0	0	0	1	Read Data
0	1	0	1	Read Status
1	0	0	1	Read Control
1	1	0	1	Invalid
0	0	1	0	Write Data
0	1	1	0	Invalid
1	0	1	0	Write Data
1	1	1	0	Invalid

TABLE 7-1. PARALLEL PORT (CS2=0) REGISTER ADDRESSES

BIT NO.	READ PORT 0	READ STATUS 1	READ CONTROL 2	WRITE CONTROL 2	WRITE DATA 0
0	Data Bit 0	1	Strobe	Strobe	Data Bit 0
1	Data Bit 1	1	Autofd	Autofd	Data Bit 1
2	Data Bit 2	$\overline{\text{INT}} \blacklozenge$	Init	Init	Data Bit 2
3	Data Bit 3	Error	Slin	Slin	Data Bit 3
4	Data Bit 4	Sict	Irq Enb	Irq Enb	Data Bit 4
5	Data Bit 5	PE	1	DIR $\blacklozenge$	Data Bit 5
6	Data Bit 6	Ack	1	1	Data Bit 6
7	Data Bit 7	Busy	1	1	Data Bit 7

( $\blacklozenge$ ) These bits are 0 in Character Mode.

TABLE 7-2. ACCESSIBLE PARALLEL PORT REGISTERS



Bit 4: This bit represents the status of INT2 being enabled. INT2 is enabled when this bit is set to one.

Bits 5 through 7: These bits always return to a logic one.

#### Write Port Register

Bits 0 through 7: These bits correspond to the data to be placed on the parallel bus. This register is used to write data to the parallel bus based on Table 7-3.

#### Write Control Register

Bits 0 through 4: Writing to these bits will set the output of the corresponding pins.

Bit 5: The Direction bit works in conjunction with the BIDEN pin to determine the direction of the parallel port data bus in extended mode, as described in the table below. This bit is only available in the WD16C551/WD16C451B, and is a write-only bit.

PORT MODE	PORT DIRECTION	PIN 1 BIDEN	DIRECTION BIT
Extended	Write	1	0
Extended	Write	0	X
Extended	Read	1	1
Compatible	Write	0	N/A
Compatible	Read	1	N/A

TABLE 7-3. PARALLEL PORT OPERATION MODES

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Control	Master Reset	All bits low.
Data (Write)	Master Reset	All bits low.
Data (Read)	Master Reset	Data
Status	Master Reset	Bits 0-2 are high, Bits 3-7 are ERR, SLCT, PE, ACK and Busy inputs.
INT2	Master Reset	High Impedance
SLIN	Master Reset	High
INIT	Master Reset	Low
AFD	Master Reset	High
STB	Master Reset	High

TABLE 7-4. REGISTERS/SIGNALS PARALLEL PORT RESET CONTROL



### 8.0 TYPICAL APPLICATIONS

Figures 8-1 and 8-2 show how to use the ACE devices in a 80286 system and in a microcomputer system with a high-capacity data bus.

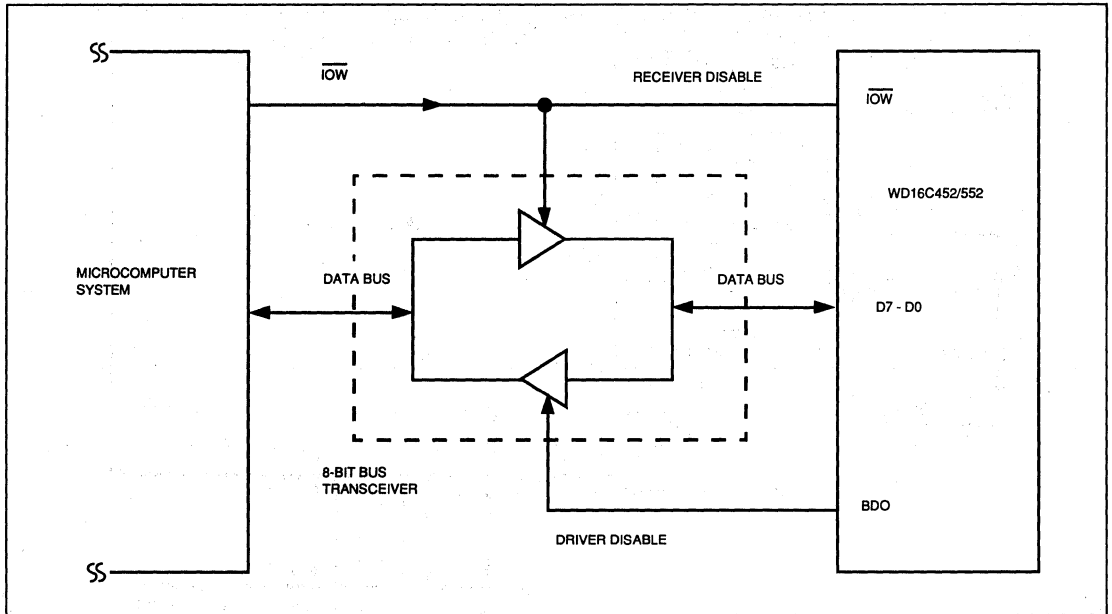


FIGURE 8-1. TYPICAL INTERFACE FOR A HIGH-CAPACITY DATA BUS





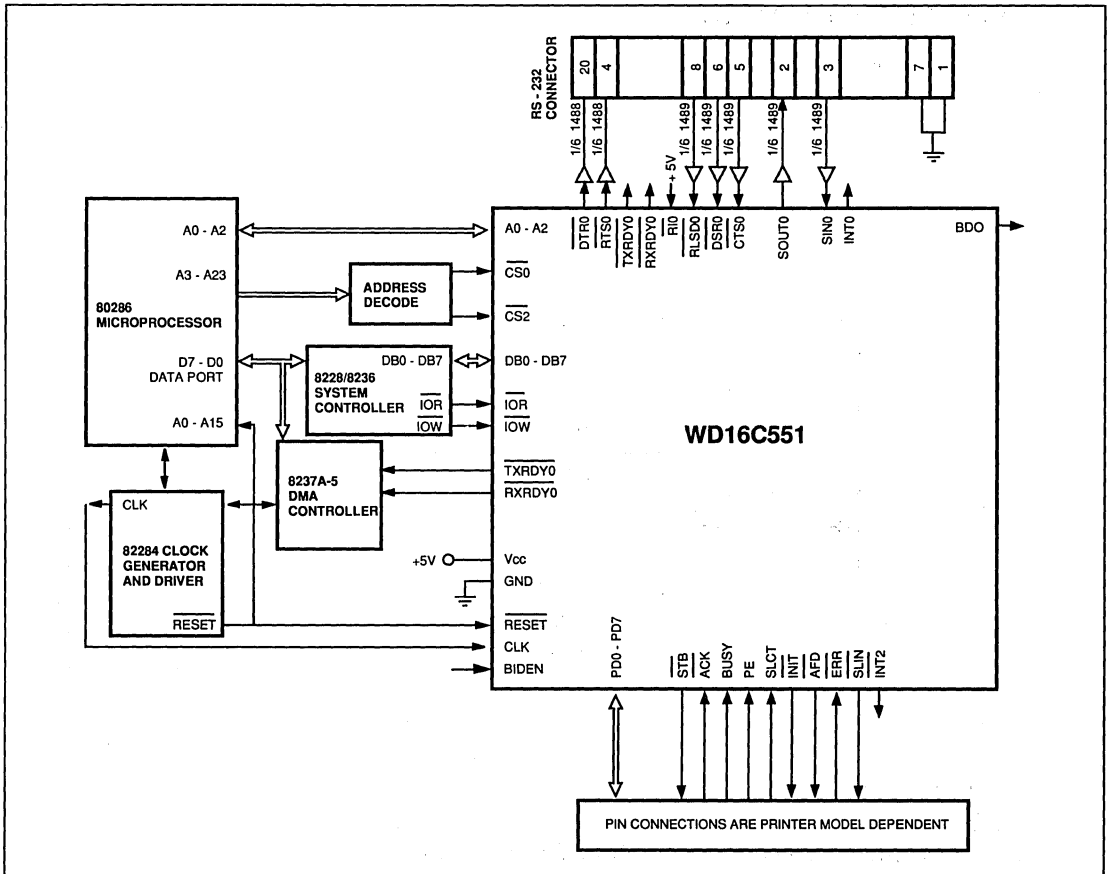


FIGURE 8-2. TYPICAL 16-BIT MICROPROCESSOR/RS-232 TERMINAL INTERFACE USING THE WD16C551



### 9.0 CRYSTAL MANUFACTURERS (Partial List)

American Time Products Division  
 Frequency Control Products Inc  
 Woodside, NY 11337

Bliley Electric Company  
 Erie, PA 16508

Cryster Crystals  
 Whitby, Ontario

Erie Frequency Control  
 Carlisle, PA 17013

Q-Matic Corporation  
 Costa Mesa, CA 92626

#### CRYSTAL SPECIFICATIONS

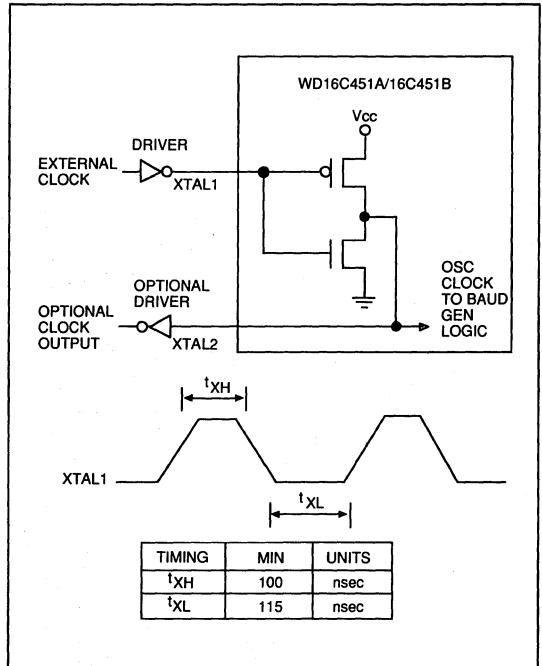
Frequency: 1.8432 MHz, 3.072 MHz, and 8.0 MHz

Type: Microprocessor Crystal

Temp. Range: 0°C (32°F) to +70°C (158°F)

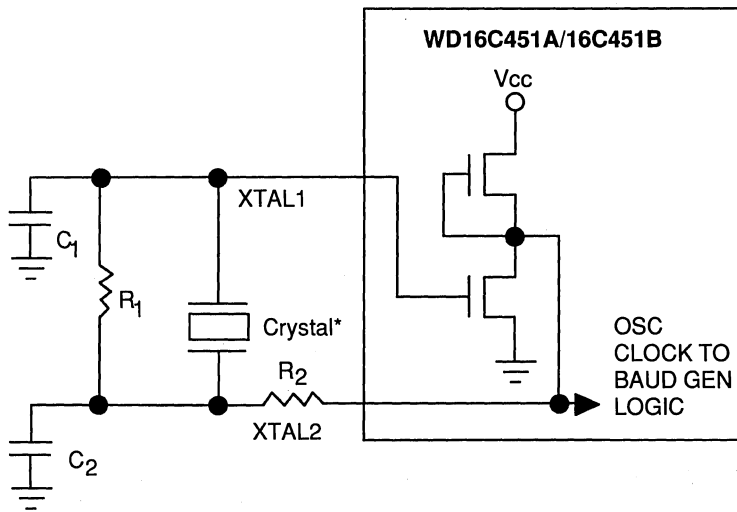
Series Resistance:  
 200-500 Ohms at 1.8432 MHz  
 100-200 Ohms at 3.072 MHz  
 20-40 Ohms at 8.0 MHz

Series Resonant  
 Overall Tolerance: ± 0.01%



**FIGURE 9-1. EXTERNAL CLOCK INPUT (8.0 MHz MAXIMUM)**





Crystal	R <sub>1</sub>	R <sub>2</sub>	C <sub>1</sub>	C <sub>2</sub>
8.0 MHz	1M Ohm	0-100 Ohm	5-10 pF	20-40 pF
3.1 MHz	1M Ohm	0-100 Ohm	10-20 pF	100-200 pF
1.8 MHz	1M Ohm	0-100 Ohm	10-20 pF	100-200 pF

EXAMPLE

FIGURE 9-2. TYPICAL CRYSTAL OSCILLATOR NETWORK

## APPENDIX A

### A.0 DC OPERATING CHARACTERISTICS

#### ABSOLUTE MAXIMUM RATINGS

Temperature

Under Bias ..... 0°C (32°F) to 70°C (158°F)

Storage Temperature ..... -65°C (-85°F) to +150°C (302°F)

All Input or Output Voltages

With respect to Vss ..... -0.5V to +7.0V

Power Dissipation WD16C451/WD16C551 ..... 300 mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Operating Characteristics



WD16C451/WD16C551					
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
Vilx	Clock Input Low Voltage	-0.5	0.8	V	
Vihx	Clock Input High Voltage	2.0	V <sub>CC</sub>	V	
Vil	Input Low Voltage	-0.5	0.8	V	
Vih	Input High Voltage	2.0	V <sub>CC</sub>	V	
Vol	Output Low Voltage		0.4	V	I <sub>OL</sub> = 4.0 mA on DB0-DB7. I <sub>OL</sub> = 24 mA on PD0-PD7. I <sub>OL</sub> = 20 mA on INIT, STB, SLIN, AFD (NOTE). I <sub>OL</sub> = 2.0 mA on other outputs.
Voh	Output High Voltage	2.4		V	I <sub>OH</sub> = 4.0 mA on DB0-DB7. I <sub>OH</sub> = 15.0 mA on PD0-PD7. I <sub>OH</sub> = 0.55 mA on INIT, AFD, STB, SLIN. I <sub>OH</sub> = 0.2 mA on other outputs.
I <sub>CC</sub>	Power Supply Current		60	mA	V <sub>CC</sub> = 5.25V, no loads on outputs: SIN0, SIN1, DSR0, DSR1, RLSD0, RLSD1, CTS0, CTS1, RI0, RI1 = 2.0V. Other inputs = 0.8V. Baud Rate = 512K. BRG = 8 MHz.
I <sub>IL</sub>	Input Leakage		±10	µA	V <sub>CC</sub> = 5.25V, V <sub>SS</sub> = 0.0V. All other pins float.
I <sub>CL</sub>	Clock Leakage		±10	µA	V <sub>IN</sub> = 0.0V, 5.25V.
I <sub>DL</sub>	Data Bus Leakage		±10	µA	V <sub>OUT</sub> = 0.4V, V <sub>OUT</sub> = 4.6V Data Bus in High Impedance State.
I <sub>OZ</sub>	Tri-state Leakage		±20	µA	V <sub>CC</sub> = 5.25V, GND = 0V, V <sub>OUT</sub> = 0.0V, 5.25V.
Vil (RES)	Reset Schmitt Vil		0.8	V	
Vih (RES)	Reset Schmitt Vih	2.0		V	

NOTE: The SLIN, AFD, STB and INIT outputs are all open collector with 2.5K to 3.5K Ohms internal pull-up resistors. When in Vol state, each input will sink a minimum of 20 mA. The internal pull-ups generate 2.0 mA of internal I<sub>OL</sub>.

T<sub>a</sub> = 0°C (32°F) to = 70°C (158°F), V<sub>CC</sub> = +5V±5%, V<sub>SS</sub> = 0V, unless otherwise specified.

TABLE A-1. DC OPERATING CHARACTERISTICS



WD16C451/WD16C551					
SYMBOL	CHARACTERISTIC	TYP	MAX	UNITS	TEST CONDITIONS
Cxin	Clock Input Capacitance	15	20	pF	fc = 1 MHz
Cxout	Clock Output Capacitance	20	30	pF	
Cin	Input Capacitance	6	10	pF	Unmeasured Pins Returned to Vss
Cout	Output Capacitance	10	20	pF	Unmeasured Pins Returned to Vss

Ta = 25°C (77°F), f = 1.0 MHz, Vcc = Vss = 0V

**TABLE A-2. CAPACITANCE**



## APPENDIX B

## B.0 AC OPERATING CHARACTERISTICS AND TIMING DIAGRAMS

Ta = 0°C (32°F) to + 70°C (158°F), Vss = +5V ±5%

## TIMING DIAGRAMS

FIGURE NUMBER	TITLE
B-1	Receiver Timing
B-2	Transmitter Timing
B-3	MODEM Control Timing
B-4	Read Cycle Timing
B-5	Write Cycle Timing
B-6	RCVR FIFO Signaling Timing for First Byte
B-7	RCVR FIFO Signaling Timing after First Byte (RBR already set)
B-8	Receiver DMA Mode 0 Timing (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)
B-9	Receiver DMA Mode 1 Timing (FCR0 = 1 and FCR3 = 1)
B-10	Transmitter DMA Mode 0 Timing (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)
B-11	Transmitter DMA Mode 1 (FCR3 = 1)
B-12	Parallel Port Timing
B-13	WD16C451/WD16C451A Parallel Port Input Timing
B-14	WD16C551/WD16C451B Parallel Port Input Timing

TABLE B-1. WD16C451/WD16C551 TIMING DIAGRAMS

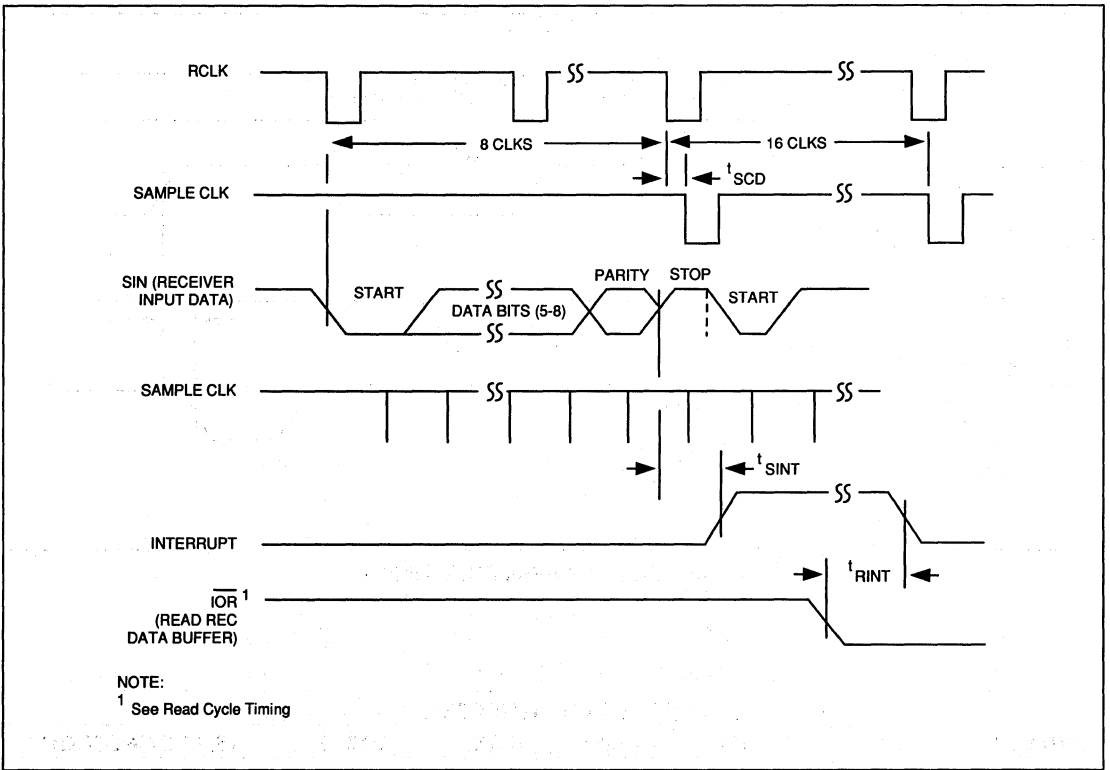


FIGURE B-1. RECEIVER TIMING

WD16C451/WD16C551					
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
$t_{SCD}$	Delay from RCLK† to Sample Time		2	$\mu$ s	
$t_{SINT}$	Delay from Stop to Set Interrupt		17*	RCLK† Cycles	100 pF Load
$t_{RINT}$	Delay from IOR (RD RBR) Reset Interrupt		1	$\mu$ s	100 pF Load

(♦) When receiving the first byte in FIFO Mode,  $t_{SINT}$  (only for timeout or trigger level interrupt) will be delayed 19 RCLK cycles, except for a timeout interrupt where  $t_{SINT}$  will be delayed 24 RCLK cycles.

(†) RCLK is an internal clock used for sampling serial in data. RCLK is equivalent to 16 times the baud rate clock.

TABLE B-2. RECEIVER TIMING





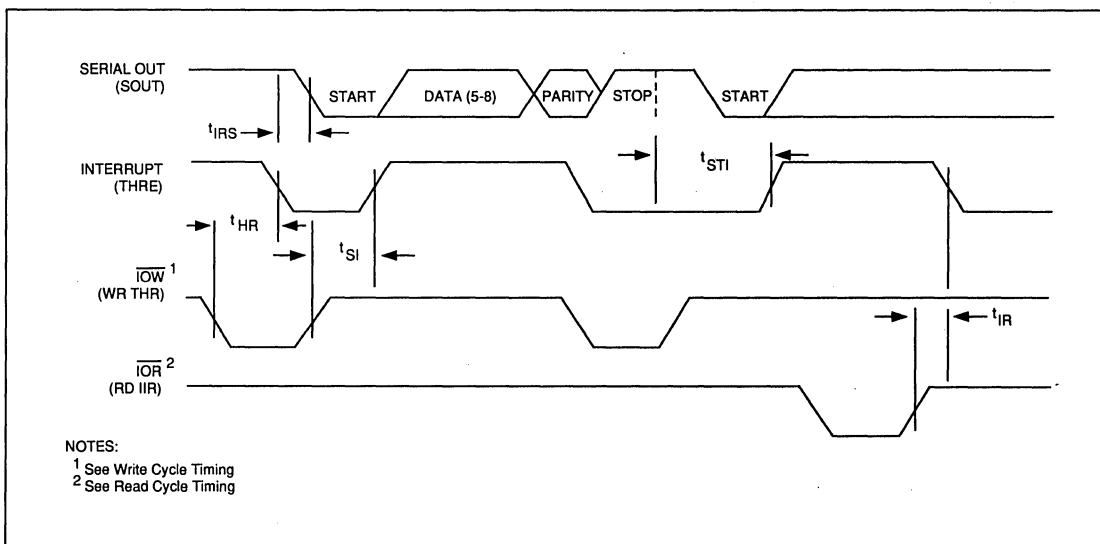


FIGURE B-2. TRANSMITTER TIMING

WD16C451/WD16C551					
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
t <sub>HR</sub>	Delay from IOW (WR THR) to Reset Interrupt		175	ns	100 pF Load
t <sub>IRS</sub>	Delay from Initial INTR Reset to Transmit Start	8	24	TCLK† Clock Cycles	
t <sub>SI*</sub>	Delay from Initial Write to Interrupt	16	24	TCLK† Clock Cycles	
t <sub>STI</sub>	Delay from Stop to Interrupt (THRE)	8	8	TCLK† Clock Cycles	
t <sub>IR</sub>	Delay from IOR (RD IIR to Reset Interrupt (THRE)		250	ns	100 pF Load
t <sub>SXA</sub>	Delay from Start to TXRDY Active	0	8	TCLK† Clock Cycles	
t <sub>WXI</sub>	Delay from Write to TXRDY Inactive	0	300	ns	

(†) TCLK is an internal clock used for sending serial out data. TCLK is equivalent to 16 times the baud rate clock.  
 (\*) In FIFO Mode, t<sub>SI</sub> might extend to beginning of Stop bit. See Line Status Register for details.

TABLE B-3. TRANSMITTER TIMING

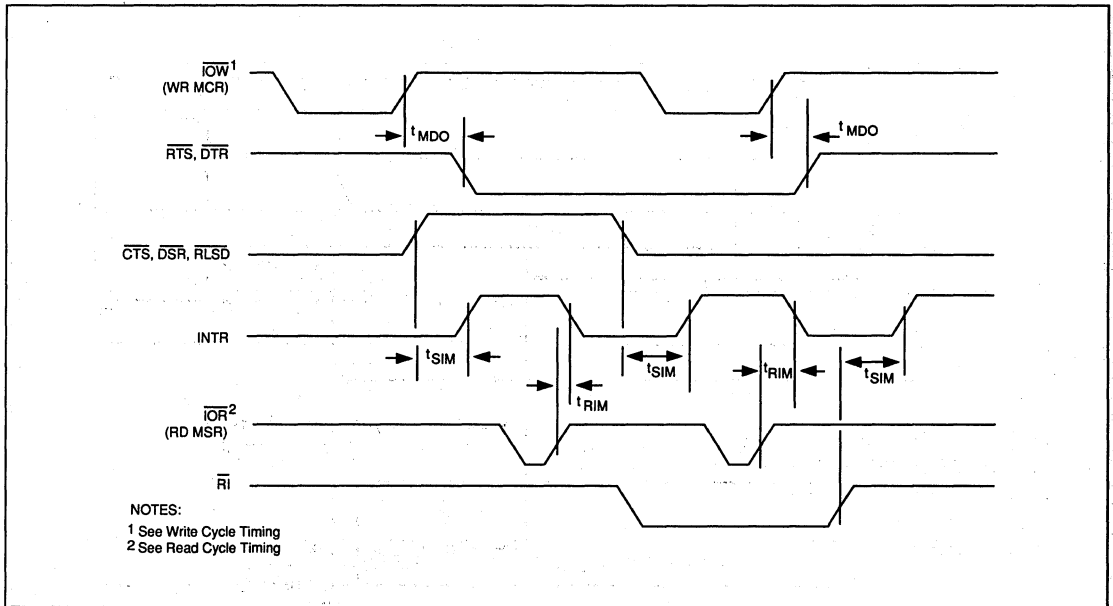


FIGURE B-3. MODEM CONTROL TIMING

WD16C451/WD16C551					
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
$t_{MDO}$	Delay from $\overline{IOW}$ (WR MCR) to Output		200	ns	100 pF Load
$t_{SIM}$	Delay to Set Interrupt from MODEM Input		250	ns	100 pF Load
$t_{RIM}$	Delay to Reset Interrupt from $\overline{IOR}$ (RD MSR)		250	ns	100 pF Load

TABLE B-4. MODEM CONTROL TIMING



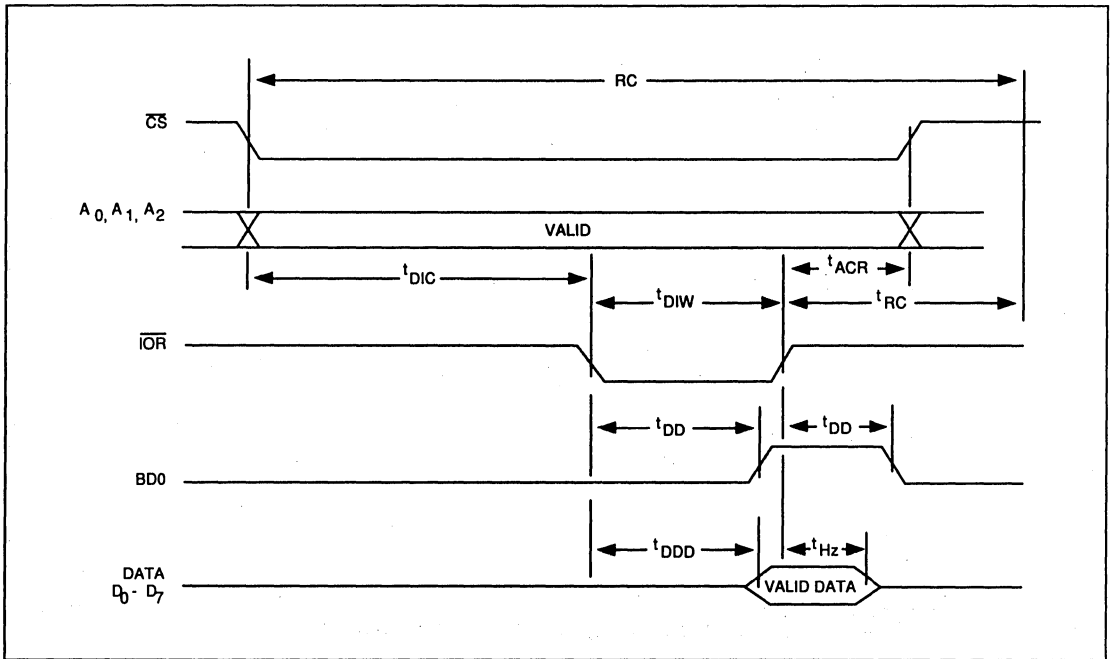


FIGURE B-4. READ CYCLE TIMING

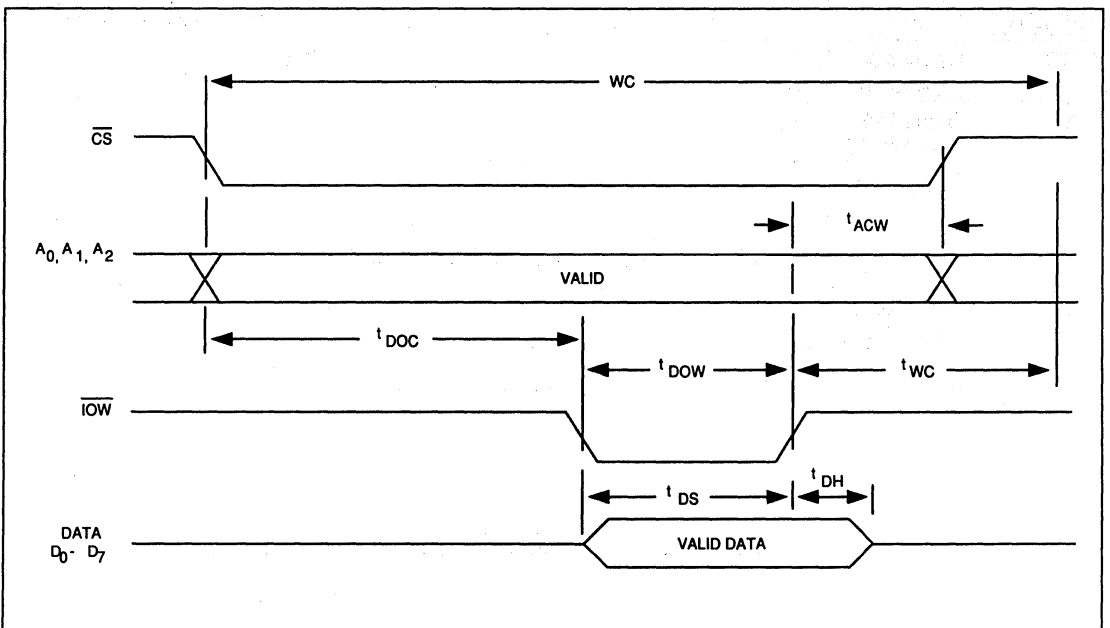


FIGURE B-5. WRITE CYCLE TIMING

WD16C451/WD16C551					
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
tDIW	IOR Strobe Width	125		ns	1TTL Load
tRC	Read Cycle Delay	125		ns	1TTL Load
RC	Read Cycle = tDIC + tDIW + tRC + 20 nsec	280		ns	1TTL Load
tDD	IOR to Driver Enable (BDO) Delay		60	ns	1TTL Load
tDDD	Delay from IOR to Data		100	ns	1TTL Load
tHZ	IOR to Floating Data Delay	0	100	ns	1TTL Load
tDOW	IOW Strobe Width	100		ns	1TTL Load
tWC	Write Cycle Delay	150		ns	1TTL Load
WC	Write Cycle = + tDOC + tDOW + tWC + 20 nsec	280		ns	1TTL Load
tDS	Data Setup Time	30		ns	1TTL Load
tDH	Data Hold Time	30		ns	1TTL Load
tDIC	IOR DELAY from Select or Address	30		ns	1TTL Load
tDOC	IOW Delay from Select or Address	30		ns	1TTL Load
tACR	Address and Chip Select Hold Time from IOR	20		ns	1TTL Load
tACW	Address and Chip Select Hold Time from IOR	20		ns	1TTL Load
tMR	Master Reset Pulse Width	5.0		μs	1TTL Load
tXH	Duration of Clock HIGH Pulse	55		ns	1TTL Load
tXL	Duration of Clock LOW Pulse	55		ns	External Clock (8.0 MHz Max.)

TABLE B-5. READ/WRITE CYCLE TIMING



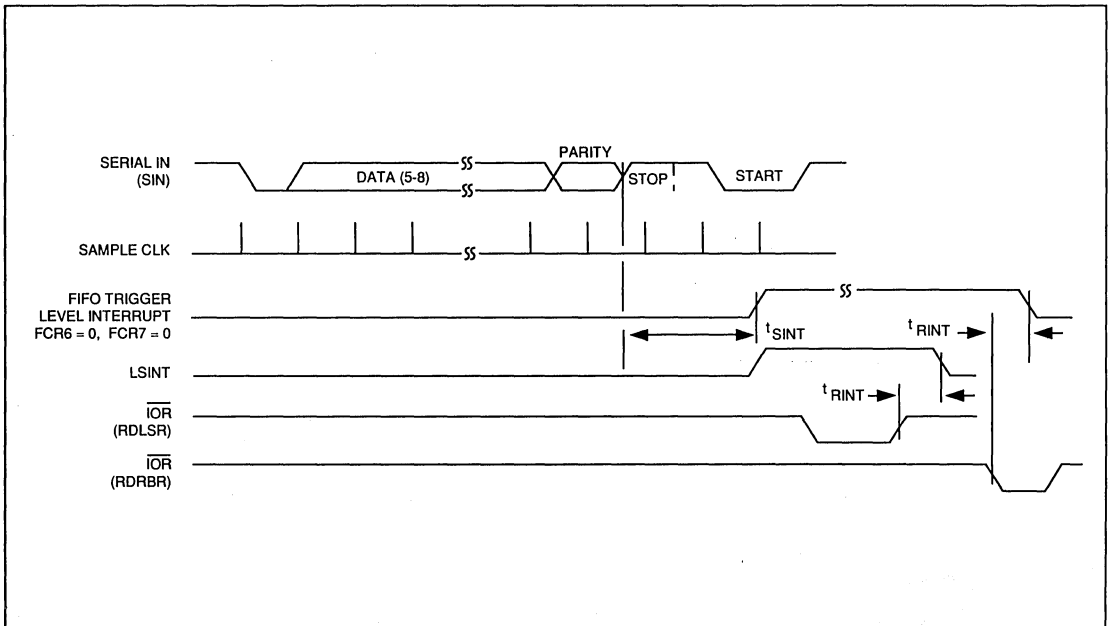


FIGURE B-6. RCVR FIFO SIGNALING TIMING FOR FIRST BYTE

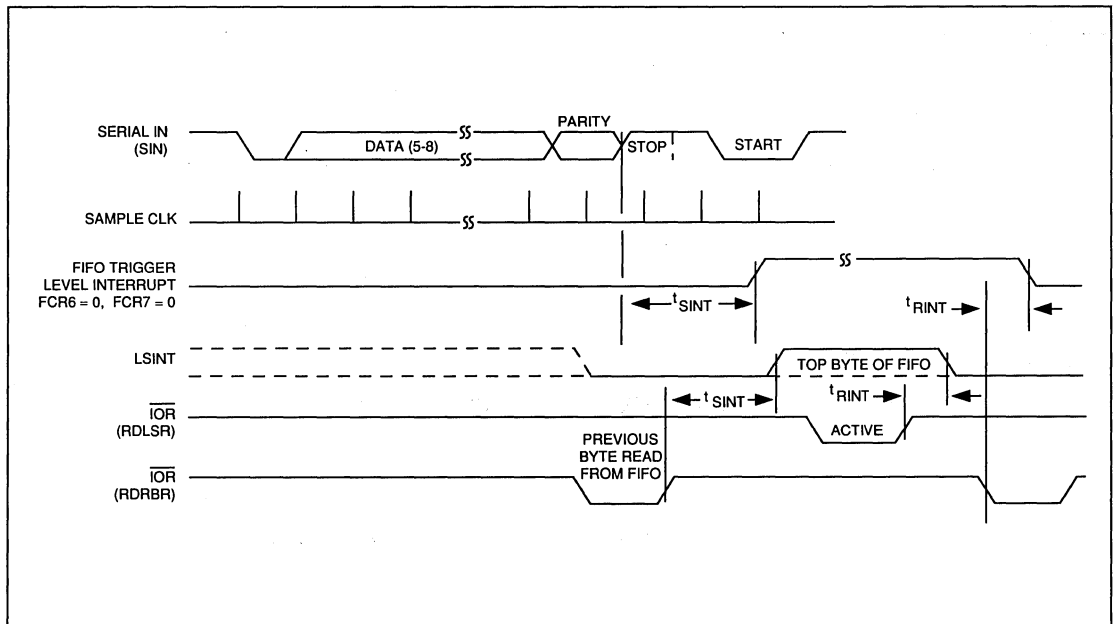
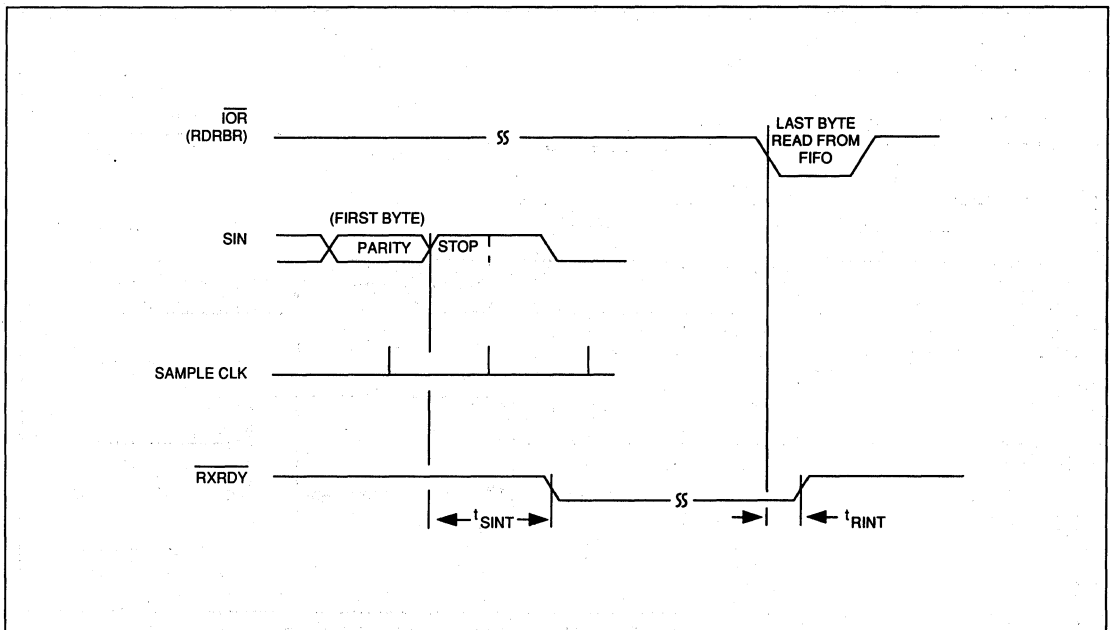
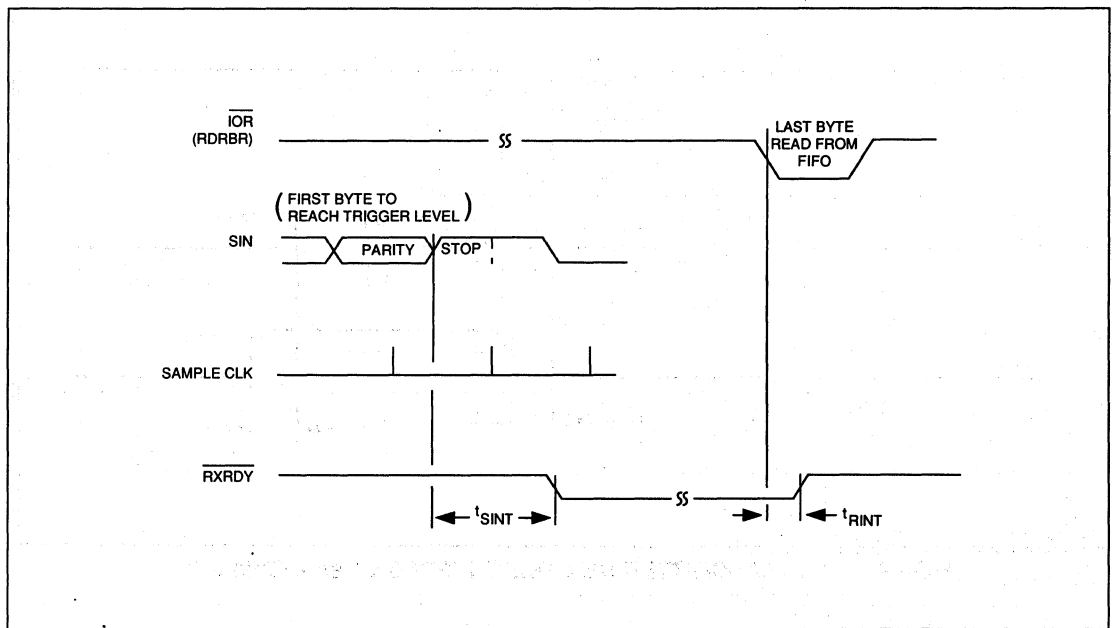


FIGURE B-7. RCVR FIFO SIGNALING TIMING AFTER FIRST BYTE  
(RBR Already Set)

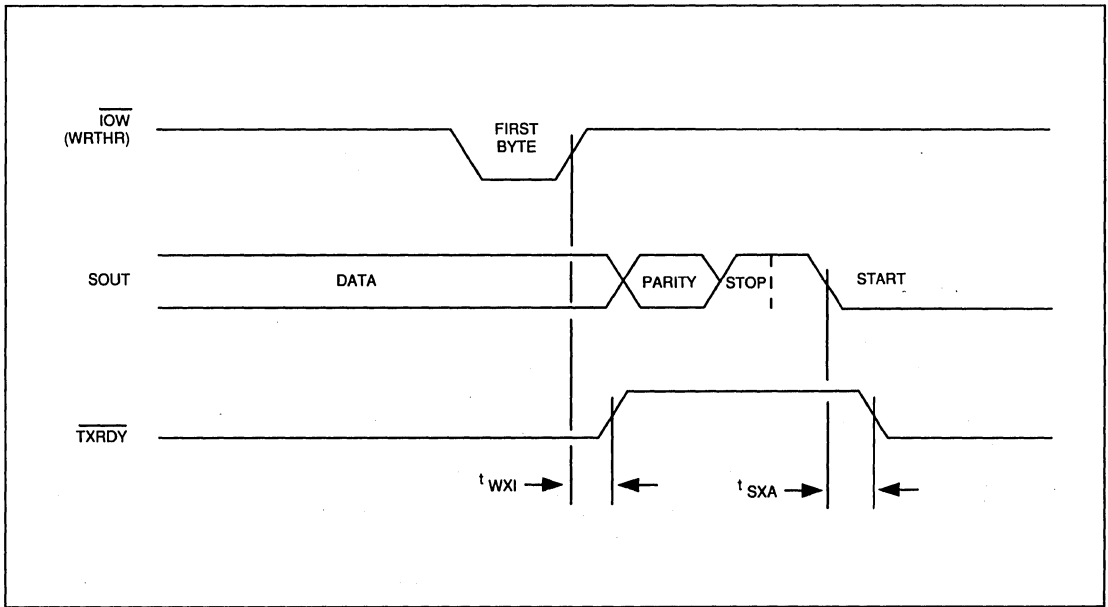


**FIGURE B-8. RECEIVER DMA MODE 0 TIMING (FCR0 = 0 or FCR0 = 1 and FCR3 = 0)**

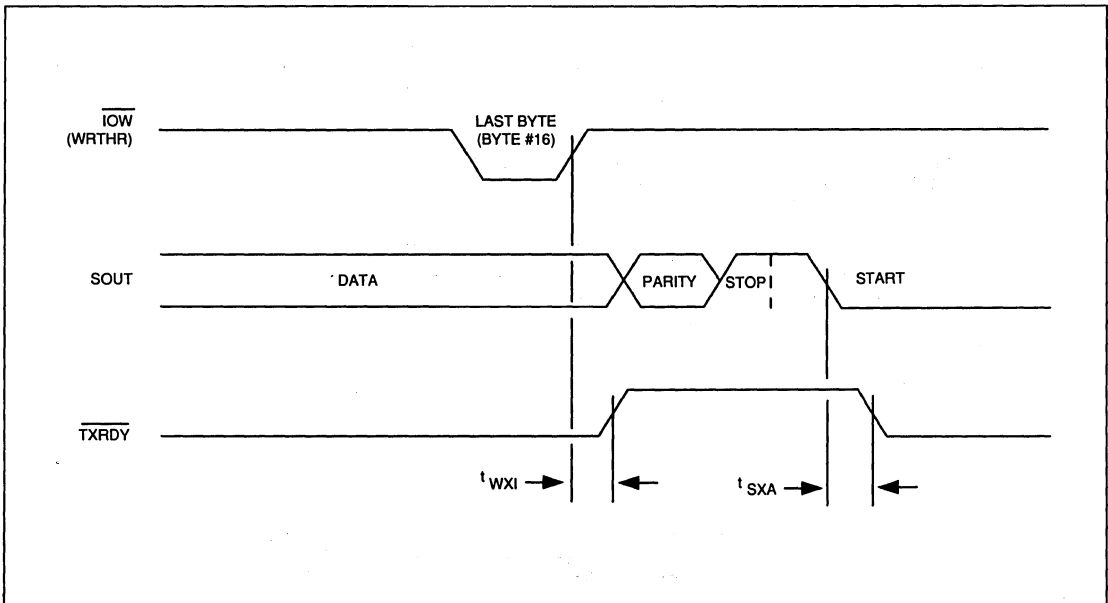


**FIGURE B-9. RECEIVER DMA MODE 1 TIMING (FCR0=1 and FCR3=1)**





**FIGURE B-10. TRANSMITTER DMA MODE 0 TIMING**  
**(FCR0 = 0 or FCR0 = 1 and FCR3 = 0)**



**FIGURE B-11. TRANSMITTER DMA MODE 1 (FCR0 = 1 and FCR3 = 1)**



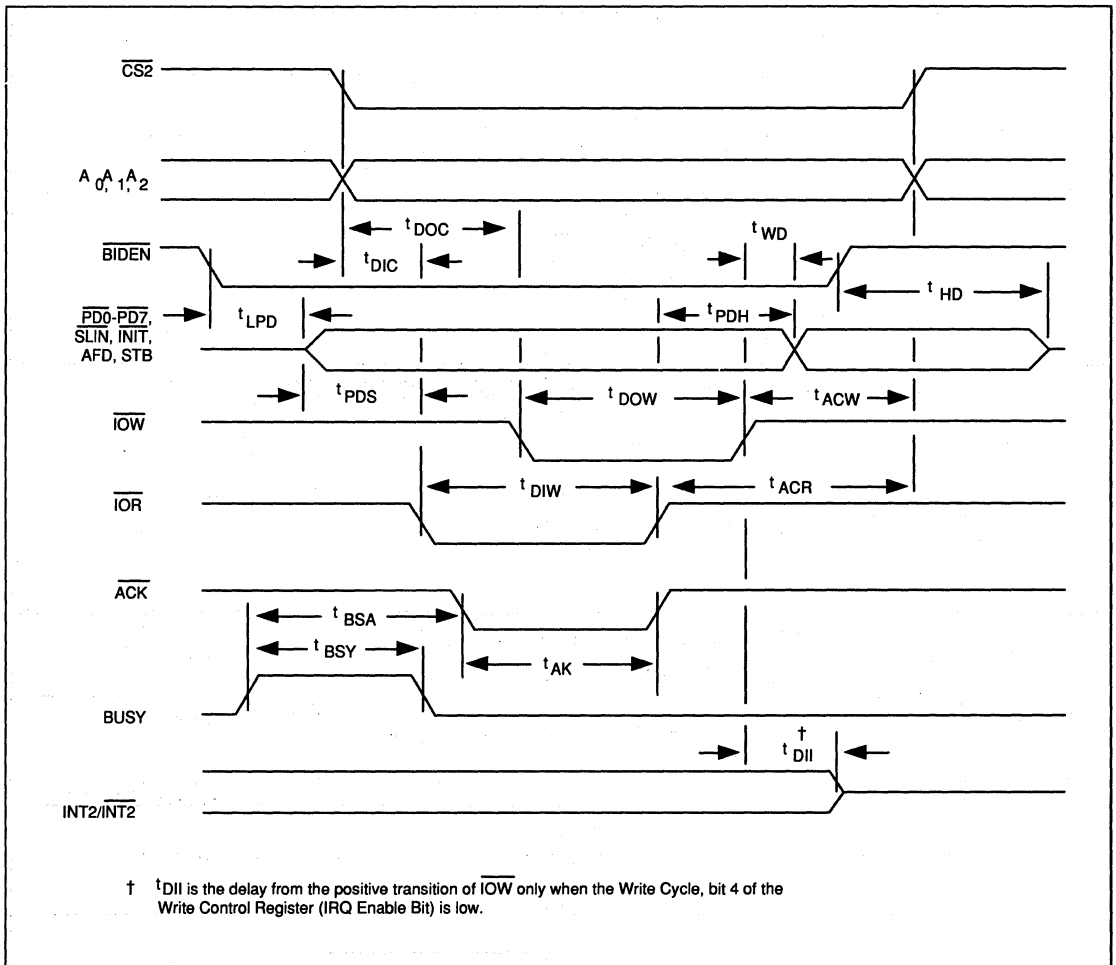


FIGURE B-12. PARALLEL PORT TIMING





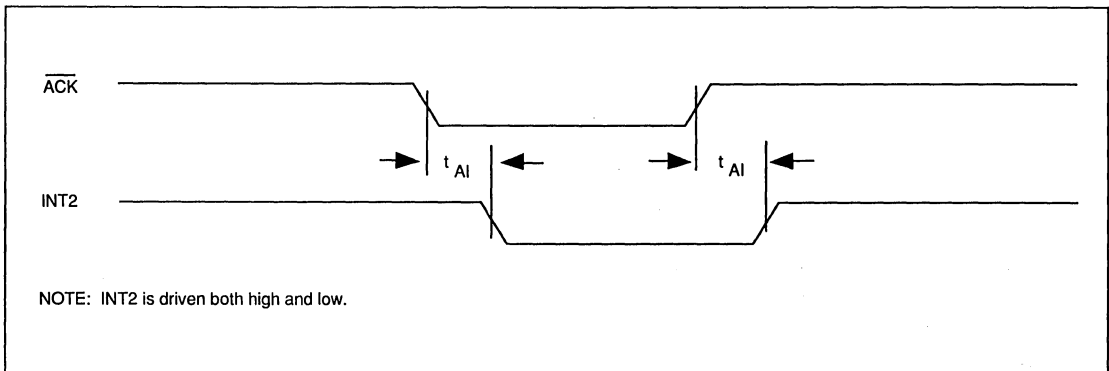


FIG. B-13. WD16C451/WD16C451A PARALLEL PORT INTERRUPT TIMING

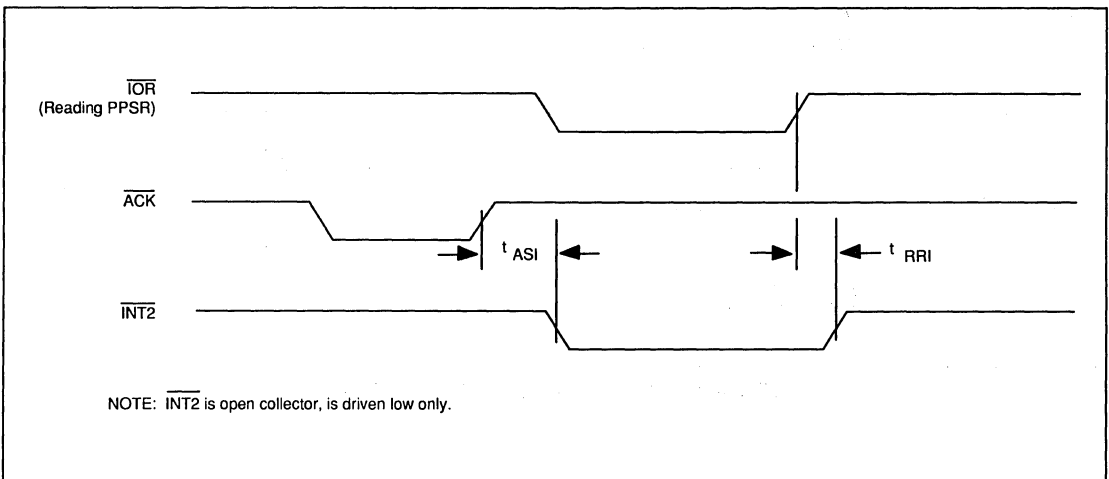


FIG. B-14. WD16C551/WD16C451B PARALLEL PORT INTERRUPT TIMING

WD16C451/WD16C551					
SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
t <sub>DOC</sub>	$\overline{\text{IOW}}$ Delay from Chip Select and Address	30		ns	
t <sub>DIC</sub>	$\overline{\text{IOR}}$ Delay from Chip Select and Address	30		ns	
t <sub>WD</sub>	$\overline{\text{IOW}}$ High to PD0-PD7, SLIN, INIT, AFD, STB		1	$\mu\text{s}$	No External Pull-up Resistor and 50 pF load
t <sub>HD</sub>	BIDEN High to PD0-PD7 Tri-State		120	ns	
t <sub>LPD</sub>	BIDEN Low to PD0-PD7 Delay		100	ns	
t <sub>PDH</sub>	PD0-PD7 Hold Time from IOR	100		ns	
t <sub>PDS</sub>	PD0-PD7 Set-up Time from IOR	100		ns	
t <sub>DOW</sub>	$\overline{\text{IOW}}$ Strobe Width	100		ns	
t <sub>DIW</sub>	$\overline{\text{IOR}}$ Strobe Width	125		ns	
t <sub>ACW</sub>	Chip Select and Address Hold Time from IOW	20		ns	
t <sub>ACR</sub>	Chip Select and Address Hold Time from IOR	20		ns	
t <sub>BSA</sub>	BUSY Start to $\overline{\text{ACK}}$			ms	Printer Dependent
t <sub>BSY</sub>	BUSY Width			$\mu\text{s}$	Printer Dependent
t <sub>AK</sub>	$\overline{\text{ACK}}$ Width			$\mu\text{s}$	Printer Dependent
t <sub>AI</sub>	INT2 Delay from $\overline{\text{ACK}}$ (WD16C451)		60	ns	1 TTL Load
t <sub>ASI</sub>	$\overline{\text{ACK}}$ to set interrupt (WD16C551)		60	ns	1 TTL Load
t <sub>RRI</sub>	Read Parallel Port Status Register (PPSR) to reset INT2		60	ns	1 TTL Load
t <sub>DII</sub>	$\overline{\text{IOW}}$ high to INT2/ $\overline{\text{INT2}}$ Tri-state	0	100	ns	1 TTL Load

TABLE B-6. PARALLEL PORT TIMING



APPENDIX C

C.O PACKAGE DIAGRAM

Figure C-1 illustrates the 68-Pin QUAD plastic package showing dimensions in inches.

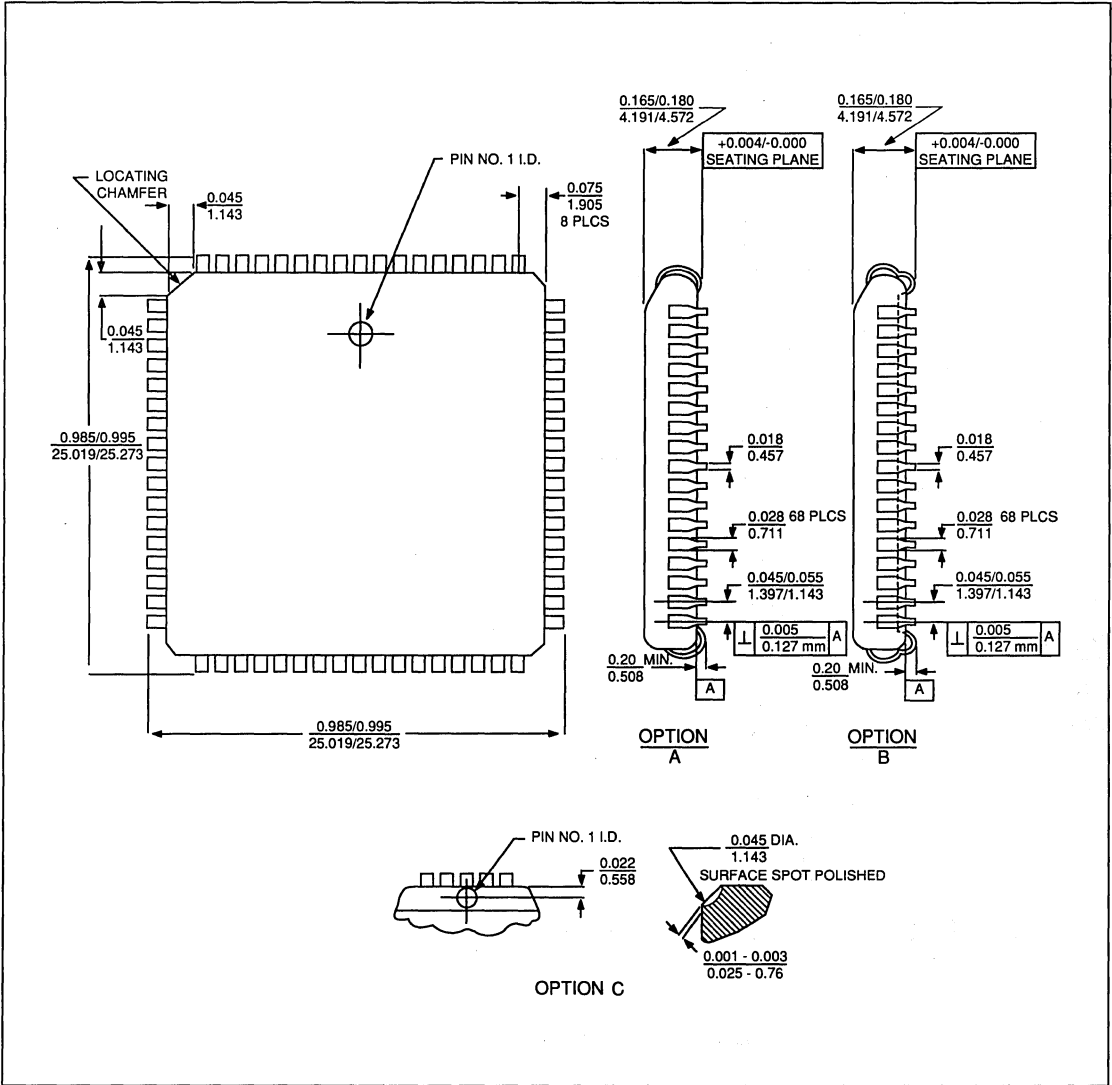


FIGURE C-1. 68-PIN QUAD PLASTIC PACKAGE

