WD90C61

(PCLK2) Video

Graphics Array Clock

WESTERN DIGITAL

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1.0 INTRODUCTION

The Western Digital® Imaging WD90C61 is a dual clock generator for VGA applications. It simultaneously generates two clocks. One clock is for the video memory, the other is the video dot clock.

The WD90C61 Video Graphics Array clock generator is capable of producing different output frequencies under firmware control. The video output frequency is derived from a 14.318 MHz system clock available in IBM PC/XT/AT and Personal System/2 computers. It is designed to work with every Western Digital Imaging Video Graphics Array device to optimize video subsystem performance.

The video dot clock output may be one of six internally generated frequencies or one of two external inputs. The selection of the video dot clock frequency is done through four inputs: VSEL0, VSEL1, VGA/TTL, and FCLKSEL. The video clock selection is latched by the SELEN signal. See Table 1 below.

The inputs and truth table have been designed to allow a direct connection to one of the many Western Digital Imaging VGA controllers. When a Western Digital Imaging controller is used with a WD90C61, two of the VGA's video clock inputs become outputs and directly drive the SELEN and VGA/TTL inputs.

The WD90C61 generates the VCLK output as shown in Table 1. The VSEL0 and VSEL1 inputs are latched with SELEN. VGA/TTL is an additional select input that selects frequencies for VGA modes when left high and frequencies for TTL modes when pulled low. Select input FCLKSEL overrides internal clock generation and passes through the FCLKIN clock input.

The MCLK output is generated as shown in Table 2. The various VCLK and MCLK frequencies are achieved by multiplying the 14.318 MHz input frequency by a factor of N/32 (e.g., 44.74 is obtained with N = 100).

The VCLKEN and MCLKEN inputs can tri-state the VCLK and MCLK outputs to facilitate board level testing. External filter components are attached to the MCAP and VCAP pins for the internal phase lock loops.

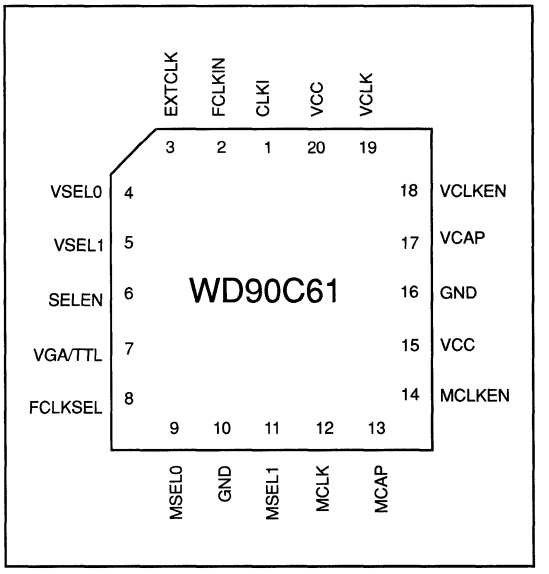

FIGURE 1. WD90C61 PIN DIAGRAM

This data book supplies sales order information, a functional overview, signal pin details, a block diagram, AC/DC characteristics, timing diagrams, and package mechanical information.

1.1 FEATURES

- Clock generator for the IBM compatible Western Digital Imaging Video Graphics Array (VGA) chips.
- Generates six video clock frequencies (25.057, 28.189, 36.242, 16.108, 32.216 and 44.744 MHz) derived from a 14.318 MHz system clock reference frequency.
- On-chip generation of four (36.242, 41.612, 37.586 and 44.744 MHz) memory clock frequencies.
- Video clock is selectable among the six internally generated clocks and two external clocks.
- CMOS technology.
- Available in a 20-pin PLCC package.

VCLKEN	FCLKSEL	VGA/TTL	VSEL0	VSEL1	SELEN†	VCLK FREQUENCY
Open	1 or Open	1 or Open	0	0	↑	25.057 MHz
Open	1 or Open	1 or Open	0	1	↑	28.189 MHz
Open	1 or Open	1 or Open	1	0	↑	EXTCLK pass-through
Open	1 or Open	1 or Open	1	1	↑	36. 242 MHz
Open	1 or Open	0	0	0	↑	14.318 MHz
Open	1 or Open	0	0	1	↑	16.108 MHz
Open	1 or Open	0	1	0	↑	32.216 MHz
Open	1 or Open	0	1	1	x	44.744 MHz
Open	0	x	x	x	x	FCLKIN pass-through

TABLE 1. VCLK SELECTION

† rising edge for SELEN (↑)

MCLKEN	MSEL0	MSEL1	MCLK FREQUENCY
Open	1 or Open	1 or Open	44.744 MHz
Open	1 or Open	0	37.585 MHz
Open	0	1 or Open	36.242 MHz
Open	0	0	41.612 MHz
0	x	x	DISABLED

TABLE 2. MCLK SELECTION

2.0 WD90C61 INTERFACE

The WD90C61 has three system interfaces: System Bus, Feature Connector and VGA Controller, as well as analog filters and four user programmed inputs. Figure 2 shows how the Western Digital Imaging VGA Clock WD90C61 is connected to a VGA controller. Western Digital Imaging VGA controllers normally have a status bit that indicates to the VGA controller that it is working with a clock chip. When working with a clock chip the VGA controller changes two of its clock inputs VCLK1 and VCLK2 to outputs. These outputs are used to select the required video clock frequency.

2.1 SYSTEM BUS INPUTS

The system bus inputs are listed below:

- CLKI
- VSEL0
- VSEL1

The WD90C61 uses the 14 MHz system bus clock as a reference to generate all its frequencies for both video and memory clocks. Address lines D2 and D3 are also commonly used as inputs to VSEL0 and VSEL1 for video frequency selection.

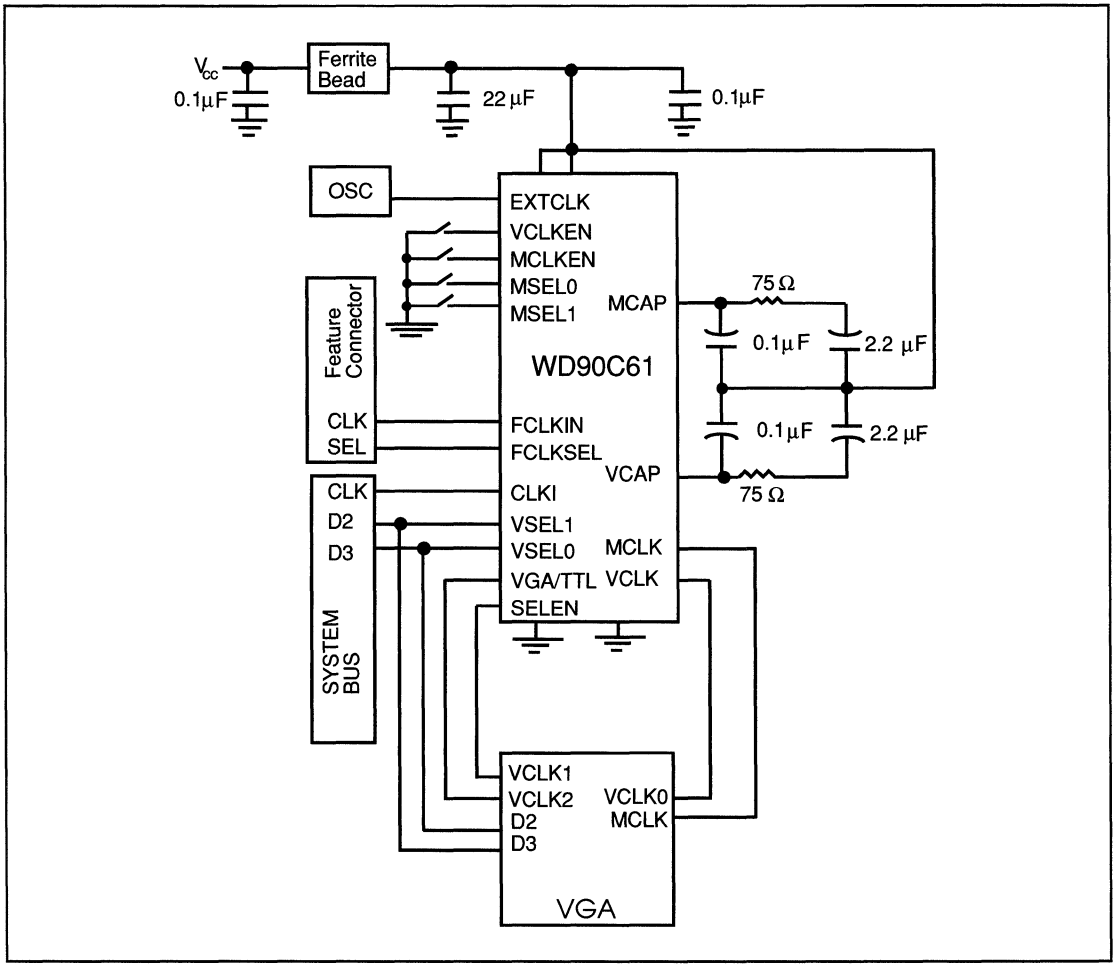

FIGURE 2. WD90C61 INTERFACE

2.2 SYSTEM BUS OUTPUTS

None

2.3 VGA CONTROLLER INPUTS

The VGA controller inputs are listed below:

- VGA/TTL
- SELEN

The WD90C61 is programmed to generate different video clock frequencies using the inputs of VSEL0, VSEL1, and VGA/TTL. The signal VGA/TTL may be supplied by the VGA controller as is the case in Western Digital Imaging VGA controllers. The inputs VGA/TTL, VSEL0, and VSEL1 are latched with the signal SELEN. The SELEN input should be an active low pulse. This active low pulse is generated in Western Digital Imaging VGA controllers during I/O writes to 3C2H.

2.4 VGA CONTROLLER OUTPUTS

The VGA controller outputs are listed below:

- MCLK
- VCLK

MCLK and VCLK are the two clock outputs to the VGA controller.

2.5 FEATURE CONNECTOR INPUTS

The feature connector inputs are listed below:

- FCLKIN
- FCLKSEL

There are two inputs from the feature connector: FCLKIN and FCLKSEL. FCLKIN may be used as an alternate video clock. FCLKIN becomes the selected video clock if FCLKSEL goes low.

2.6 FEATURE CONNECTOR OUTPUTS

None

2.7 ANALOG FILTERS

The analog filters are lsited below:

- MCAP
- VCAP

These connections are for the analog filters. The component values of the filters are critical. Care must be taken to ensure proper values over the entire operating range desired for the final product. Figure 2 shows the filter circuit. The capacitator tolerances are ± 20%. The resistor tolerance is 2%.

2.8 USER DEFINEABLE INPUTS

The user defineable inputs are listed below:

- EXTCLK
- VCLKEN
- MCLKEN
- MSEL0
- MSEL1

EXTCLK is an additional input that may be routed to the VCLK0 output. This additional input is useful for supporting modes that require frequencies not provided by the WD90C61. VCLKEN and MCLKEN are the output enable signals for VCLK and MCLK.

MSEL0 and MSEL1 are the memory clock (MCLK) select lines. Table 2 shows how MCLK frequencies are selected. All signals in this group have internal pullup resistors.

3.0 WD90C61 FUNCTIONAL BLOCK DIAGRAM

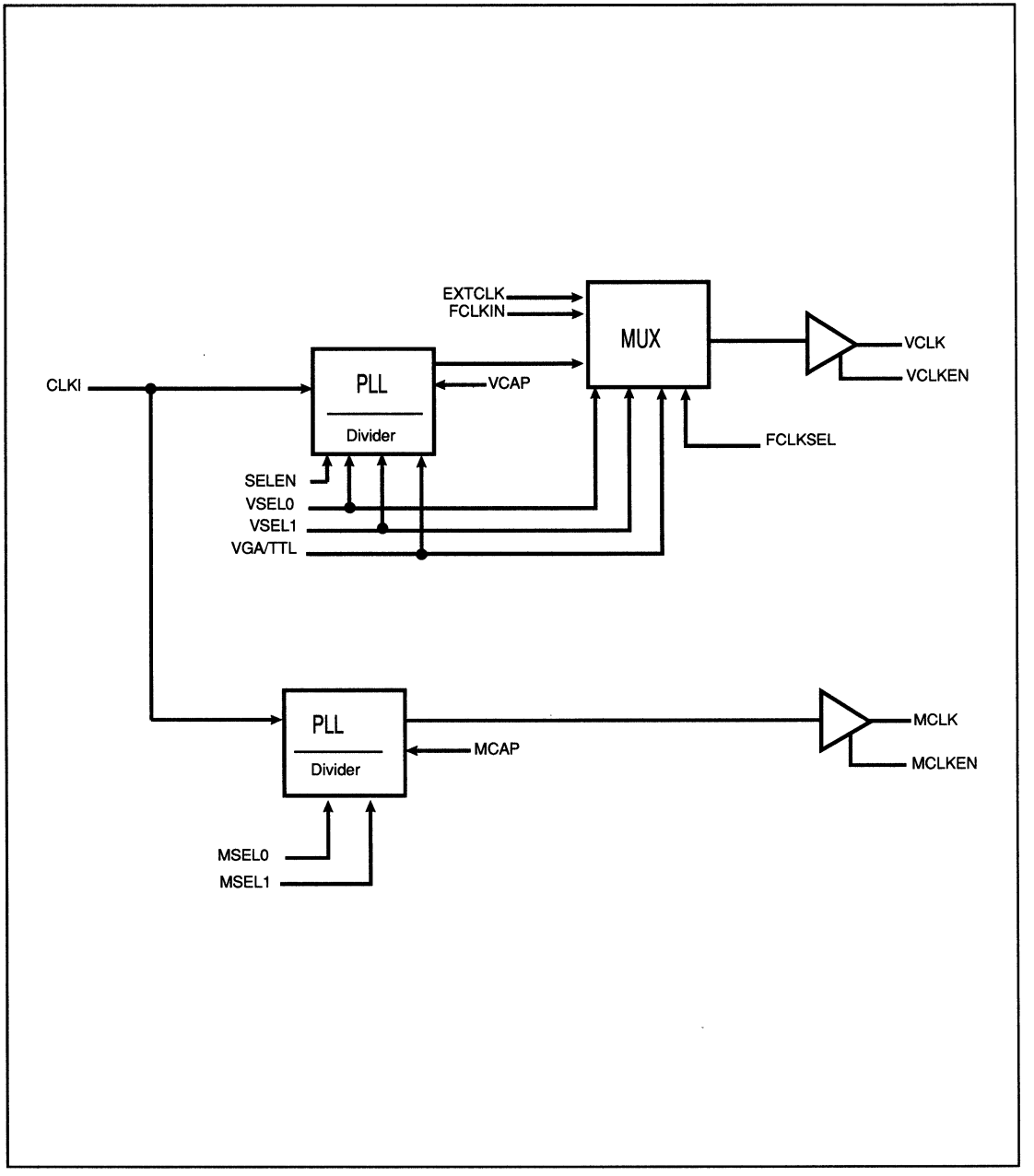

FIGURE 3. WD90C61 FUNCTIONAL BLOCK DIAGRAM

4.0 PIN DESCRIPTION

The following table provides the pin definitions for the 20-pin WD90C61 package.

PIN NO.	PIN SYMBOL	TYPE	DESCRIPTION
1	CLKI	IN	Reference Input Clock from system (14.318MHz)
2	FCLKIN	IN	Clock input from Feature Connector
3	EXTCLK	IN	External Clock input for an additional frequency
4	VSEL0	IN	Control Input for VCLK selection
5	VSEL1	IN	Control Input for VCLK selection
6	SELEN	IN	Strobe for latching SEL0 and SEL1
7	VGA/TTL	IN	Select input for VCLK selection
8	FCLKSEL	IN	Select input for VCLK. When pulled low, passes through FCLKIN
9	MSEL0	IN	Select input for MCLK selection
10	GND	---	Ground for digital circuit
11	MSEL1	IN	Select input for MCLK selection
12	MCLK	OUT	Memory Clock (MCLK) output
13	MCAP	IN	External filter connection for MCLK generation
14	MCLKEN	IN	Enable input for MCLK output. When pulled low, tri-states MCLK
15	VCC	---	Power supply for analog circuit
16	GND	---	Ground for analog circuit
17	VCAP	IN	External filter connection for VCLK generation
18	VCLKEN	IN	Enable input for VCLK output. When pulled low, tri-states VCLK
19	VCLK	OUT	Video Clock (VCLK) output
20	VCC	---	Power supply for digital circuit

TABLE 3. PIN DESCRIPTIONS

NOTE
CLKI, FCLKIN, EXTCLK, VSEL0, VSEL1, SELEN, VGA/TTL, FCLKSEL, MSEL0, MSEL1, MCLKEN, VCLKEN input pins have internal pull-up resistance.

5.0 ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	0°C to 70°C
Storage temperature	-40° C to 125° C
Voltage on all inputs and outputs with respect to V_{SS}	0.5 to 7 Volts

NOTE
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

5.1 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (0V Ground). Positive current flows into the referenced pin.

Operating temperature range	0° to 70° C
Power supply voltage	4.75 to 5.25 Volts

5.2 D.C . CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage	V_{SS}	0.8	V	VCC = 5V
V_{IH}	Input High Voltage	2.0	VCC	V	VCC = 5V
I_{IH}	Input Leakage Current	---	20	µA	$V_{IN} = V_{CC}$
V_{OL}	Output Low Voltage	---	0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output High Voltage	2.4	---	V	I_{OH} = 4.0 mA
I_{CC}	Supply Current	---	30	mA	V_{CC} = 5V
R_{UP}	Internal Pullup Resistors	25	---	KOhm	VCC = 5V
Cin	Input Pin Capacitance	---	8	pF	Fc = 1 MHz
Cout	Output Pin Capacitance	---	12	pF	Fc = 1 MHz

TABLE 4. DC CHARACTERISTICS

NOTE:
CLKI, FCLKIN, EXTCLK, VSEL0, VSEL1, SELEN, VGA/TTL, FCLKSEL, MSEL0, MSEL1, MCLKEN, VCLKEN input pins have internal pullup resistance.

6.0 AC TIMING CHARACTERISTICS

The following notes apply to all of the parameters presented in this section:

1. REFCLK = 14.318 MHz
2. $t_c = 1/f_c$
3. All units are in nanoseconds (ns)
4. Maximum jitter within a range of 30 µs after triggering on a 400 MHz scope.
5. Rise and fall time between 0.8 and 2.0 VDC.
6. Output pin loading = 25 pF.
7. Duty cycle measured at 1.4 V

SYMBOL	PARAMETER	MIN	MAX	NOTES
	SELEN TIMING			
t_{pwen}	Enable Pulse Width	20	---	
t_{suen}	Setup Time Data to Enable	20	---	
t_{hden}	Hold Time Data to Enable	10	---	
	Reference Input Clock			
t_r	Rise Time	---	10	Phase Jitter 1 ns max
t_f	Fall Time	---	10	Duty Cycle 42.5% min to 57.5% max
	MCLK & VCLK TIMINGS			
t_r	Rise time	---	3	Phase Jitter 5 ns max
t_f	Fall time	---	3	Duty Cycle 40% min to 60% max
---	Frequency Error		1	%
---	Pass through Frequency		56	MHz
---	Propogation Delay for Pass through frequency	---	20	
---	Output Enable to tri-state (into and out of) time	---	15	

TABLE 5. AC TIMING CHARACTERISTICS

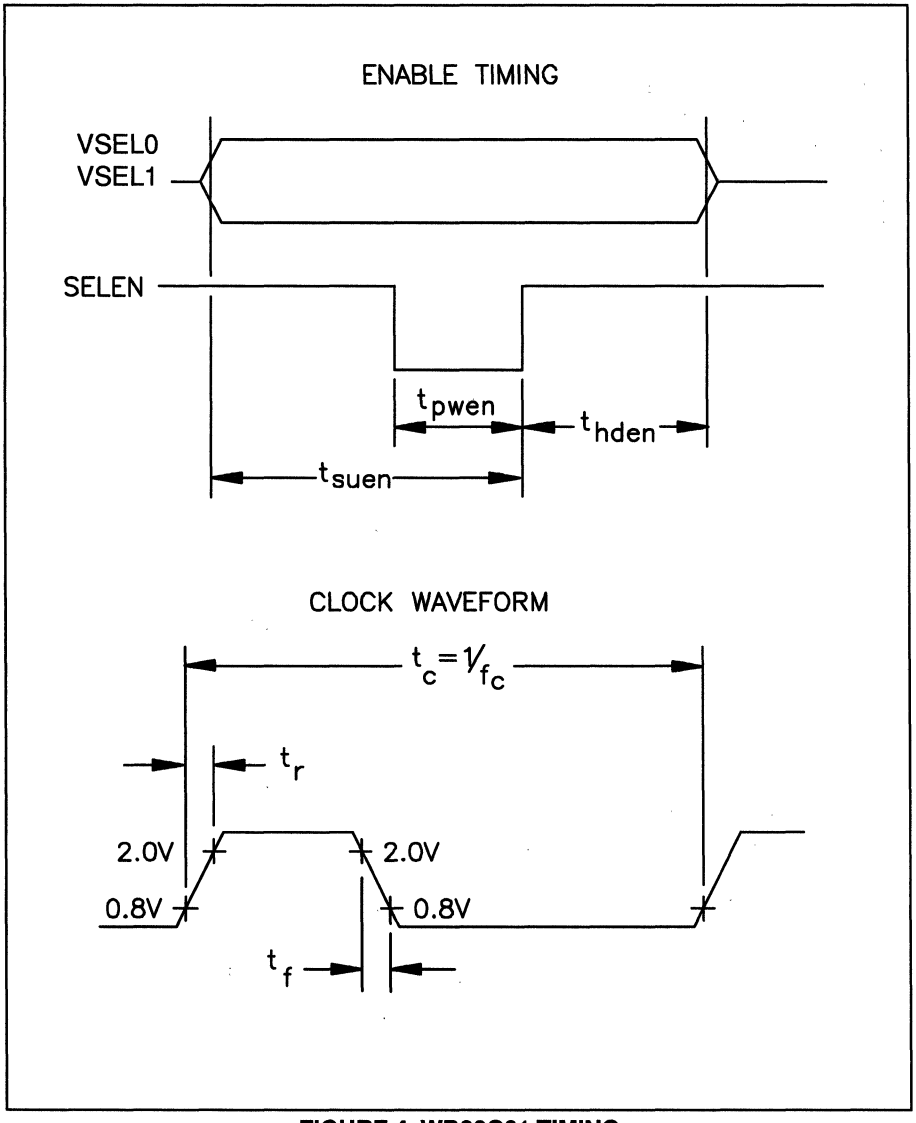

FIGURE 4. WD90C61 TIMING

7.0 ORDERING INFORMATION

Package Type: 20-Pin PLCC

Part Number: WD90C61JE00 02

7.1 PACKAGE DIMENSIONS

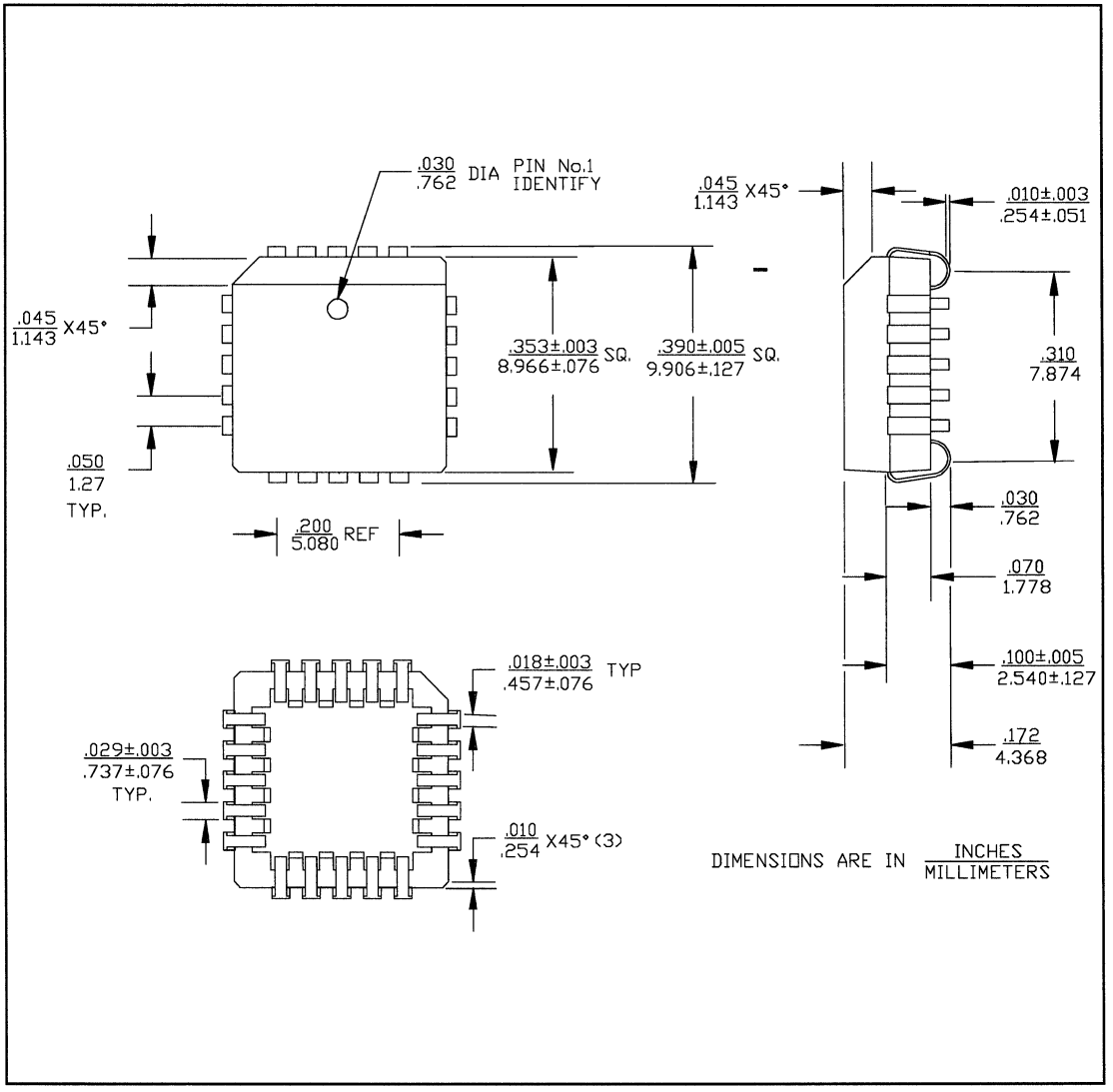

FIGURE 5. WD90C61 20-PIN PLCC PACKAGE DIMENSIONS