VLSI TECHNOLOGY, INC.

SCAMP II 5 VOLT CHIP SET FOR POWER-MANAGED PORTABLE APPLICATIONS

VL82C316
VL82C323
DATA MANUAL

Portable Systems
Division
October 1992

ADVANCE INFORMATION

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PREFACE

This manual provides the reader with a preliminary technical reference for VLSI Technology, Inc.'s VL82C316 SCAMP System Controller device for use in PC/AT-compatible applications. If you should require performance or functions not included in this manual, please contact your local VLSI Technology Design Center or Sales Office. The addresses are listed on the last page of this manual.

Since computer technology is extremely fast-moving, it is planned that VLSI's Personal Computer Products Division will revise, update, and publish this manual often. This will allow timely publication of data on new products, as well as improvements on existing ones. The most current information may also be obtained from your local VLSI Technology, Inc. Sales Office, Representative, or the Personal Computer Division in Tempe, Arizona.

Readers are encouraged to send their comments, corrections, or suggestions to:

Director, Marketing Communications
VLSI Technology, Inc.
8375 South River Parkway
Tempe, AZ 85284

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LIST OF FIGURES

VLSI TECHNOLOGY, INC.

ADVANCE INFORMATION

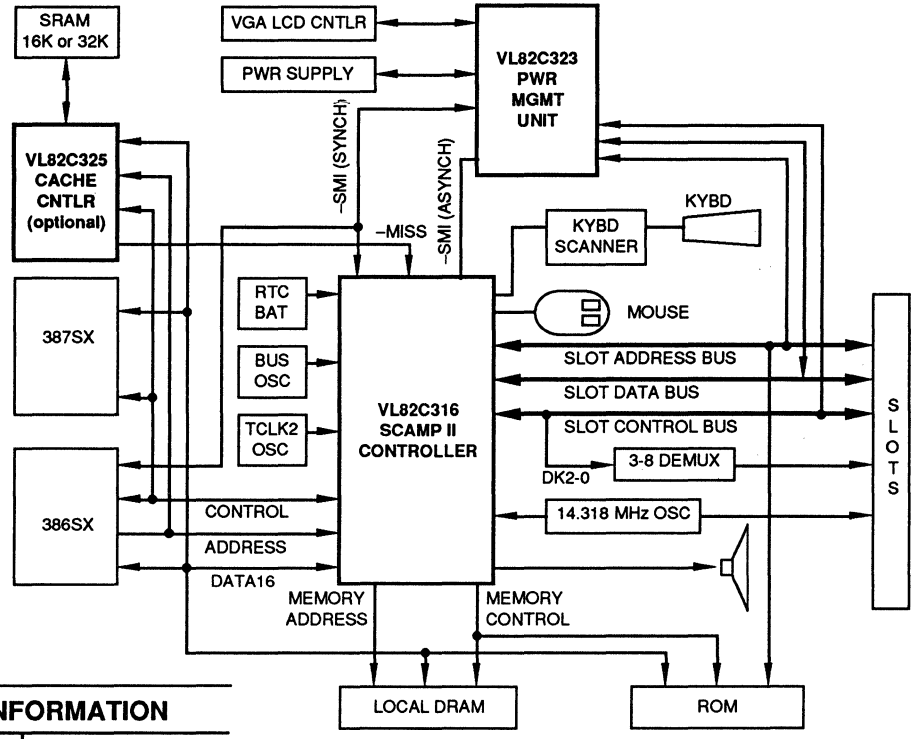
VL82C316

SCAMP™ II SYSTEM CONTROLLER

FEATURES

- Compatible with 386SX-based PC/AT compatible systems
- Up to 33 MHz system clock
- Replaces 11 peripheral devices on the motherboard:
  - Two 82C37A DMA controllers
  - 74LS612 memory mapper
  - Two 82C59A interrupt controllers
  - 82C54 timer
  - 82284 clock generator and ready interface
  - 82288 bus controller
  - Keyboard controller
  - Real-time clock
- Includes:
  - Memory/refresh controller
  - Port B and NMI logic
  - Bus steering logic
  - Parity generation checking logic
  - Turbo Mode control logic
  - Staggered refresh to minimize power supply load variations
  - Three-state control pin for board level testability
- Supports:
  - Up to 16 MB system memory
  - PCMCIA 1.0 IC Memory Card mapping logic
  - VL82C325 (SX) Cache Controller compatibility
  - Four 16- or 18-bit wide banks of 256K, 1M, or 4M DRAM or eight 16-bit wide banks of 512K x 8 DRAM
  - Shadow RAM in 640K to 1M range
  - 387SX numeric coprocessors
  - 8- or 16-bit wide BIOS ROMs
  - Synchronous or asynchronous slot bus operation up to 16 MHz
  - Relocation of video and slot ROMs
- Power saving features include:
  - Sleep and Suspend Modes
  - Slow DRAM refresh
  - CAS-before-RAS and Self-Refresh DRAM
  - Sleep Mode refresh switch to 32 kHz clock
  - Leakage Control in Stop Clock or Suspend Mode
  - CPU on or off option in Suspend Mode

VL82C316/386SX-BASED NOTEBOOK SYSTEM DIAGRAM



ORDER INFORMATION

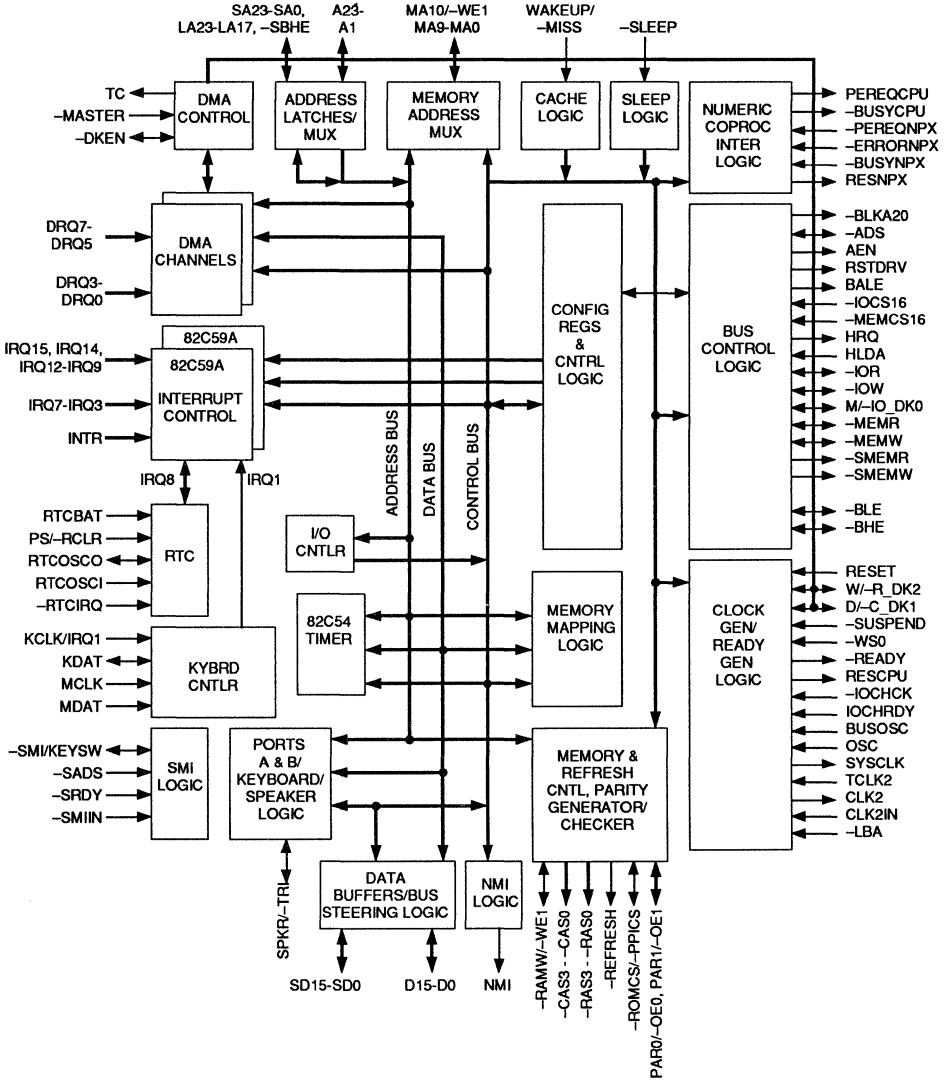
Part Number	Package
VL82C316-FC	Metric Quad Flat Pack

Note: Operating temperature range is 0°C to +70°C.

Features (Cont.)

- Low-power page interleave memory mode
- Fully static operation
- DMA power management mode
- Full SMM (System Management Mode) and I/O break support
- Supports standard Sleep Mode for interface to the VL82C323 Power Management Unit (PMU) or other third party PMUs
- Programmable, extendable peripheral cycle
- Disable software coprocessor reset option
- Option for automatic bus speed-up on video or PCMCIA accesses
- Full support for local bus peripherals
- Separate power pins for ISA bus signals allows ISA to be powered down independently of other interfaces
- Other advanced features
  - Programmable I/O decode for 10- or 16-bit addresses
  - Hardware configurable setup to minimize custom BIOS requirements
  - Programmable drive current to reduce ringing on DRAM
- 0.8-micron CMOS technology
- 208-lead metric quad flat pack (MQFP)

VL82C316 BLOCK DIAGRAM



OVERVIEW

The VL82C316 is a true single chip AT high-performance controller for 386SX-based PC/AT systems. The VL82C316 is intended primarily for low-power applications requiring a high degree of integration (e.g., notebooks). However, the VL82C316 is also an excellent choice for high integration, low-cost desktop systems running up to 33 MHz.

The VL82C316 includes the dual 82C37A DMA controllers, dual 82C59A programmable interrupt controllers, 82C54 programmable interval timer, 82284 clock and ready generator, 82288 bus controller, 8042 keyboard controller, and 146818A-compatible real-time clock. Also included is the logic for SMM (System Management Mode) control, address/data bus control, memory control, shutdown, refresh generation and refresh/DMA arbitration.

The controller also includes the following:

- AMD and Cyrix compatible SMM and I/O Break interface
- Complete ISA bus interface logic
- Integrated power management features
- Supports slow and self-refresh DRAM
- Memory/refresh controller
- Port B and NMI logic
- Bus steering logic
- Turbo Mode control logic
- Optional parity checking logic
- Optional parity generation logic

The VL82C316 supports 387SX-compatible numeric coprocessors including versions that support slow and stop clock operation.

The memory controller logic is capable of accessing up to 16 MB. There can be up to four banks of 256K, 1M, or 4M attached in the system or eight banks of 512K x 8 DRAMs. The VL82C316 can drive the full compliment of DRAM banks without external buffering. It features Built-in Page Mode operation. This, along with two-way interleaving, allows the PC designer to maximize system performance using low-cost DRAMs. Support is also included for zero, one, or two wait state operation of system DRAM.

Shadowing features are supported on 16K boundaries between C0000h and DFFFFh, and on 32K boundaries between A0000h and BFFFFh, and between E0000h and FFFFFh. Simultaneous shadowed ROM, and direct system board access is possible in a non-overlapping fashion throughout this memory space. Control over four access options is provided. The options are:

1. Access ROM or slot bus for reads and writes.
2. Access system board DRAM for reads and writes.
3. Access system board DRAM for reads and slot bus for writes.
4. Shadow setup mode. Read ROM or slot bus, write system board DRAM.

The VL82C316 handles system board refresh directly and also controls the timing of slot bus refresh. Refresh is performed in the standard PC/AT-compatible Mode where on- and off-board refreshes are performed synchronousiy. Refreshes are staggered to minimize power supply loading and attenuate noise on the VDD and ground pins. In the VL82C316, refresh can be programmed to support CAS-before-RAS refresh operation, standard RAS-only refresh operation, self-refresh, or no refresh. The VL82C316 supports the PC/AT standard refresh period of 15.625 µs plus 125 µs or 250 µs slow refresh options. When the Suspend Mode is active, the real-time clock's 32 kHz oscillator is used as the timing reference for absolute minimum power dissipation. Self-refresh is possible only in the Suspend Mode. DRAM accesses are not possible in this mode of operation. When self-refresh is active, it is only enabled when the Suspend Mode is also active. Otherwise, CAS-before-RAS refresh is used.

A 146818A-compatible real-time clock (RTC) is provided that supports battery voltages down to 2.4 volt standard. It also includes 128 extra battery-backed RAM locations (178 total) for operating system and power-management support. The base address of the RTC is programmable, but defaults to the PC standard address. The hardware supports an external RTC. It may be used with the internal RTC or by itself by disabling the internal RTC.

An internal keyboard controller replaces the standard 8042 required in a standard PC environment. It provides a keyboard and PS/2® mouse interface. As an option, the internal keyboard controller can be disabled allowing use of an external controller.

The 387SX is supported. A software coprocessor reset does not leave a 387SX in the same state as does the reset of a 287. The VL82C316 can be programmed to disable these software resets if problems arise.

The interrupt controller logic consists of two 82C59A megacells with eight interrupt request lines each for a total of 16 interrupts. The two megacells are cascaded internally and two of the interrupt request inputs are connected to internal circuitry allowing a total of 13 external interrupt requests. There is a special programmable logic included in the VL82C316 which allows glitch-free inputs on all the interrupt request pins.

The interval timer includes one 82C54 counter/timer megacell. The counter/timer has three independent 16-bit counters and six programmable counter modes.

The DMA controllers are 82C37A compatible. The DMAs control data transfers between an I/O channel and on- or off-board memory. DMA can transfer data over the full 16 MB range available. There are internal latches provided for latching the middle address bits output by the 82C37A megacells on the data bus, and 74LS612 memory mappers are provided to generate the upper address bits. An optional low-power DMA mode is available. In this mode, the DMA clocks are stopped except when DMA accesses are in progress.

The VL82C316 can be programmed for asynchronous or synchronous operation of the AT® bus.

The VL82C316 also performs all of the data buffer control functions required. Under the control of the CPU, the VL82C316 chip routes data to and from the CPU's D bus and slots (SD bus). The parity is checked for D bus DRAM read operations. The data is latched for synchronization with the CPU. Parity is generated for all data written to the D bus. The parity function may be optionally disabled except when 512K x 8 DRAM memory maps are used. In this case, parity is not an available option.

The VL82C316 generates control signals for external buffers to perform high-to-low and low-to-high byte swaps on the SD bus. For transfers between two peripherals on the slot bus, the flow control outputs of the VL82C316 disable the external data buffers. The VL82C316 also provides the feature of a single input, –TRI, to disable all of its outputs for board level testability.

The VL82C316 SCAMP II Controller's functions are programmable via a set of internal Configuration Registers. The state of the memory address bus, parity pins, DKEN, –BLKA20, –RAMW/–WE0, and –ROMCS/–PPICS pins on reset is used to determine the default configuration. A dip switch can be used to establish the initial configuration.

Separated power buses are provided for:

A. ISA bus signal I/O pads

B. DRAM interface I/O pads

C. Real-time clock

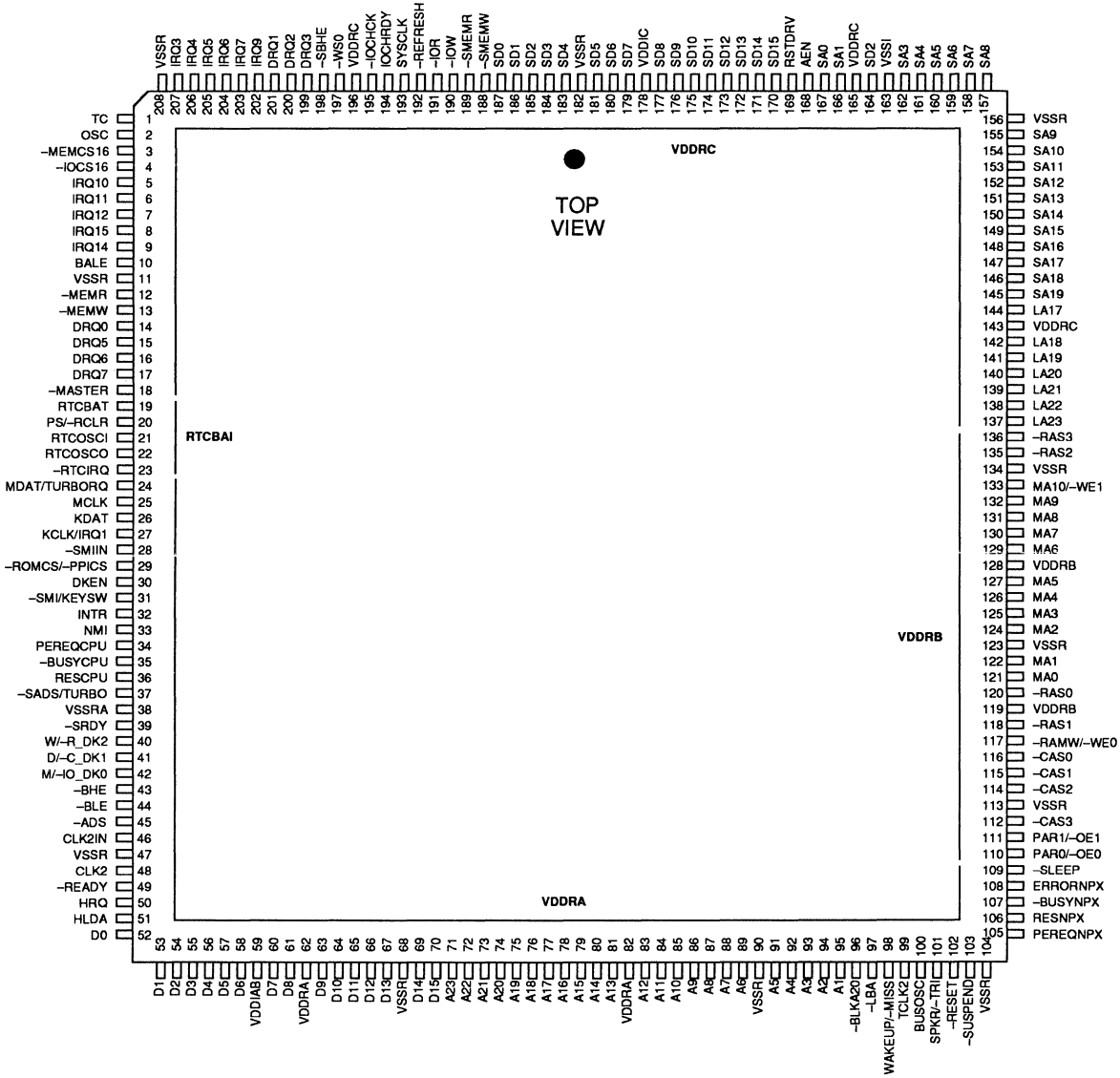
D. CPU interface I/O pads

E. Internal core logic

This break-out allows the following options:

1. The CPU can be shut down while the remainder of the system continues powered.
2. The DRAM interface can remain powered during the Suspend Mode in order to provide refresh while other circuitry is powered down.

PIN DIAGRAM


TOP
VIEW
VDDRC
RTCBAI
VDDRB
VDDRA
1 TC
2 OSC
3 -MEMCS16
4 -IOCS16
5 IRQ10
6 IRQ11
7 IRQ12
8 IRQ15
9 IRQ14
10 BALE
11 VSSR
12 -MEMR
13 -MEMW
14 DRQ0
15 DRQ5
16 DRQ6
17 DRQ7
18 -MASTER
19 RTCBAT
20 PS/-RCLR
21 RTCOSCI
22 RTCOSCO
23 -RTCIRQ
24 MDAT/TURBORQ
25 MCLK
26 KDAT
27 KCLK/IRQ1
28 -SMIIN
29 -ROMCS/-PPICS
30 DKEN
31 -SMI/KEYSW
32 INTR
33 NMI
34 PEREQCPU
35 -BUSYCPU
36 RESCPU
37 -SADS/TURBO
38 VSSRA
39 -SRDY
40 W/-R_DK2
41 D/-C_DK1
42 M/-IO_DK0
43 -BHE
44 -BLE
45 -ADS
46 CLK2IN
47 VSSR
48 CLK2
49 -READY
50 HRQ
51 HLDA
52 D0
53 D1
54 D2
55 D3
56 D4
57 D5
58 D6
59 VDDIAB
60 D7
61 D8
62 VDDRA
63 D9
64 D10
65 D11
66 D12
67 D13
68 VSSR
69 D14
70 D15
71 A23
72 A22
73 A21
74 A20
75 A19
76 A18
77 A17
78 A16
79 A15
80 A14
81 A13
82 VDDRA
83 A12
84 A11
85 A10
86 A9
87 A8
88 A7
89 A6
90 VSSR
91 A5
92 A4
93 A3
94 A2
95 A1
96 -BLKA20
97 -LBA
98 WAKEUP/-MISS
99 TCLK2
100 BUSOSC
101 SPKR/-TRI
102 -RESET
103 -SUSPEND
104 VSSR
105 PEREQNPX
106 RESNPX
107 -BUSYNPX
108 ERRORNPX
109 -SLEEP
110 PAR0/-OE0
111 PAR1/-OE1
112 -CAS3
113 VSSR
114 -CAS2
115 -CAS1
116 -CAS0
117 -RAMW/-WE0
118 -RAS1
119 VDDRB
120 -RAS0
121 MA0
122 MA1
123 VSSR
124 MA2
125 MA3
126 MA4
127 MA5
128 VDDRB
129 MA6
130 MA7
131 MA8
132 MA9
133 MA10/-WE1
134 VSSR
135 -RAS2
136 -RAS3
137 LA23
138 LA22
139 LA21
140 LA20
141 LA19
142 LA18
143 VDDRC
144 LA17
145 SA19
146 SA18
147 SA17
148 SA16
149 SA15
150 SA14
151 SA13
152 SA12
153 SA11
154 SA10
155 SA9
156 VSSR
157 SA8
158 SA7
159 SA6
160 SA5
161 SA4
162 SA3
163 VSSI
164 SD2
165 VDDRC
166 SA1
167 SA0
168 AEN
169 RSTDRV
170 SD15
171 SD14
172 SD13
173 SD12
174 SD11
175 SD10
176 SD9
177 SD8
178 VDDIC
179 SD7
180 SD6
181 SD5
182 VSSR
183 SD4
184 SD3
185 SD2
186 SD1
187 SD0
188 -SMEMW
189 -SMEMR
190 -IOW
191 -IOR
192 -REFRESH
193 SYSCLK
194 IOCHRDY
195 -IOCHCK
196 VDDRC
197 -WS0
198 -SBHE
199 DRQ3
200 DRQ2
201 DRQ1
202 IRQ9
203 IRQ7
204 IRQ6
205 IRQ5
206 IRQ4
207 IRQ3
208 VSSR

PIN TYPE BY OPERATIONAL STATE

Pin Name	Pin No.	Pin Type	Input Type	Drive mA	Power Rail	Suspend Mode CPU On (Note 9)	Suspend Mode CPU Off (Note 9)
TC	1	O-TS		12	C	PD - Note 8	PD - Note 8
OSC	2	I	TTL (Notes 7 & 10)		C	HI-Z	HI-Z
–MEMCS16	3	I (Note 1)	CMOS (Note 10)		C	HI-Z	HI-Z
–IOCS16	4	I (Note 1)	TTL		C	HI-Z	HI-Z
IRQ10	5	I	TTL		C	PD	PD
IRQ11	6	I	TTL		C	PD	PD
IRQ12	7	I	TTL		C	PD	PD
IRQ15	8	I	TTL		C	PD	PD
IRQ14	9	I	TTL		C	PD	PD
BALE	10	O-TS		12	C	PD	PD
VSSR	11	GND			Ring Gnd		
–MEMR	12	IO (Note 2)	TTL (Note 10)	12	C	HI-Z	HI-Z
–MEMW	13	IO (Note 2)	TTL (Note 10)	12	C	HI-Z	HI-Z
DRQ0	14	I	TTL		C	PD	PD
DRQ5	15	I	TTL		C	PD	PD
DRQ6	16	I	TTL		C	PD	PD
DRQ7	17	I	TTL		C	PD	PD
–MASTER	18	I	TTL		C	PD	PD
RTCBAT	19	PWR			RTC PWR		
PS/–RCLR	20	I-PU	CMOS-S		RTC BAT	Unchanged	Unchanged
RTCOSCI	21	I	CMOS		RTC BAT	Unchanged	Unchanged
RTCOSCO	22	O			RTC BAT	Unchanged	Unchanged
–RTCIRQ	23	IO-PU	TTL-S	4	RTC BAT	Unchanged	Unchanged
MDAT/TURBORQ	24	IO (Note 1)	TTL-S	12	A	HI-Z	HI-Z
MCLK	25	IO (Note 1)	TTL-S	12	A	HI-Z	HI-Z
KDAT	26	IO (Note 1)	TTL-S	12	A	HI-Z	HI-Z
KCLK/IRQ1	27	IO (Note 1)	TTL-S	12	A	HI-Z	HI-Z
–SMIIN	28	I	TTL		A	HI-Z	HI-Z
–ROMCS/–PPICS	29	IO	TTL	4	A	High	PD
DKEN	30	IO	TTL	4	A	Low	PD
–SMI/KEYSW	31	IO (Note 1)	TTL-S	4	A	HI-Z	HI-Z
INTR	32	O-TS		4	A	Unchanged	PD
NMI	33	O-TS		4	A	Unchanged	PD
PEREQCPU	34	O-TS (Note 3)		4	A	Unchanged	PD

PIN TYPE BY OPERATIONAL STATE (Cont.)

Pin Name	Pin No.	Pin Type	Input Type	Drive mA	Power Rail	Suspend Mode CPU On (Note 9)	Suspend Mode CPU Off (Note 9)
–BUSYCPU	35	O-TS (Note 4)		4	A	Unchanged	PD
RESCPU	36	IO	TTL	4	A	Low	PD
–SADS/TURBO	37	I	TTL (Note 10)		A	HI-Z	PD
VDDRA	38	PWR			A Supply		
–SRDY	39	O-TS (Note 4)		4	A	High	PD
W/–R_DK2	40	IO	TTL	4	A	PD	PD
D/–C_DK1	41	IO	TTL	4	A	PD	PD
M/–IO_DK0	42	IO	TTL	4	A	PD	PD
–BHE	43	IO	TTL	4	A	PD	PD
–BLE	44	IO	TTL	4	A	PD	PD
–ADS	45	IO	TTL (Note 10)	4	A	HI-Z	PD
CLK2IN	46	I	CMOS		A	HI-Z	HI-Z
VSSR	47	GND			Ring Gnd		
CLK2	48	IO	TTL	8	A	Low	Low
–READY	49	IO	TTL	4	A	High	PD
HRQ	50	IO	TTL	4	A	High	PD
HLDA	51	I	TTL		A	HI-Z	PD
D0	52	IO	TTL	4	A	PD	PD
D1	53	IO	TTL	4	A	PD	PD
D2	54	IO	TTL	4	A	PD	PD
D3	55	IO	TTL	4	A	PD	PD
D4	56	IO	TTL	4	A	PD	PD
D5	57	IO	TTL	4	A	PD	PD
D6	58	IO	TTL	4	A	PD	PD
VDDIAB	59	PWR			A & B Core		
D7	60	IO	TTL	4	A	PD	PD
D8	61	IO	TTL	4	A	PD	PD
VDDRA	62	PWR			A Supply		
D9	63	IO	TTL	4	A	PD	PD
D10	64	IO	TTL	4	A	PD	PD
D11	65	IO	TTL	4	A	PD	PD
D12	66	IO	TTL	4	A	PD	PD
D13	67	IO	TTL	4	A	PD	PD
VSSR	68	GND			Ring Gnd		

PIN TYPE BY OPERATIONAL STATE (Cont.)

Pin Name	Pin No.	Pin Type	Input Type	Drive mA	Power Rail	Suspend Mode CPU On (Note 9)	Suspend Mode CPU Off (Note 9)
D14	69	IO	TTL	4	A	PD	PD
D15	70	IO	TTL	4	A	PD	PD
A23	71	IO	TTL	4	A	PD	PD
A22	72	IO	TTL	4	A	PD	PD
A21	73	IO	TTL	4	A	PD	PD
A20	74	IO	TTL	4	A	PD	PD
A19	75	IO	TTL	4	A	PD	PD
A18	76	IO	TTL	4	A	PD	PD
A17	77	IO	TTL	4	A	PD	PD
A16	78	IO	TTL	4	A	PD	PD
A15	79	IO	TTL	4	A	PD	PD
A14	80	IO	TTL	4	A	PD	PD
A13	81	IO	TTL	4	A	PD	PD
VDDRA	82	PWR			A Supply		
A12	83	IO	TTL	4	A	PD	PD
A11	84	IO	TTL	4	A	PD	PD
A10	85	IO	TTL	4	A	PD	PD
A9	86	IO	TTL	4	A	PD	PD
A8	87	IO	TTL	4	A	PD	PD
A7	88	IO	TTL	4	A	PD	PD
A6	89	IO	TTL	4	A	PD	PD
VSSR	90	GND			Ring Gnd		
A5	91	IO	TTL	4	A	PD	PD
A4	92	IO	TTL	4	A	PD	PD
A3	93	IO	TTL	4	A	PD	PD
A2	94	IO	TTL	4	A	PD	PD
A1	95	IO	TTL	4	A	PD	PD
–BLKA20	96	IO	TTL	4	A	PD	PD
–LBA	97	I	TTL		A	HI-Z	PD
WAKEUP/–MISS	98	IO	TTL	4	A	HI-Z	PD
TCLK2	99	I	CMOS (Note 10)		A	HI-Z	HI-Z
BUSOSC	100	I	CMOS (Note 10)		A	HI-Z	HI-Z
SPKR/–TRI	101	IO-PU	TTL	8	A	PU	PU
–RESET	102	I	TTL-S		A	HI-Z	HI-Z

PIN TYPE BY OPERATIONAL STATE (Cont.)

Pin Name	Pin No.	Pin Type	Input Type	Drive mA	Power Rail	Suspend Mode CPU On (Note 9)	Suspend Mode CPU Off (Note 9)
–SUSPEND	103	I	TTL		A	HI-Z	HI-Z
VSSR	104	GND			Ring Gnd		
PEREQNPX	105	I	TTL (Note 10)		A	HI-Z	PD
RESNPX	106	IO	TTL	4	A	Low	PD
–BUSYNPX	107	I	TTL (Note 10)		A	HI-Z	PD
–ERRORNPX	108	I	TTL (Note 10)		A	HI-Z	PD
–SLEEP	109	I	TTL		A	HI-Z	HI-Z
PAR0/–OE0	110	IO	TTL	12/24	B	(Note 6)	(Note 6)
PAR1/–OE1	111	IO	TTL	12/24	B	(Note 6)	(Note 6)
–CAS3	112	IO	TTL	12/24	B	(Note 5)	(Note 5)
VSSR	113	GND			Ring Gnd		
–CAS2	114	IO	TTL	12/24	B	(Note 5)	(Note 5)
–CAS1	115	IO	TTL	12/24	B	(Note 5)	(Note 5)
–CAS0	116	IO	TTL	12/24	B	(Note 5)	(Note 5)
–RAMW/–WE0	117	IO	TTL	12/24	B	(Note 6)	(Note 6)
–RAS1	118	IO	TTL	12/24	B	(Note 5)	(Note 5)
VDDRB	119	PWR			B Supply		
–RAS0	120	IO	TTL	12/24	B	(Note 5)	(Note 5)
MA0	121	IO	TTL	12/24	B	(Note 6)	(Note 6)
MA1	122	IO	TTL	12/24	B	(Note 6)	(Note 6)
VSSR	123	GND			Ring Gnd		
MA2	124	IO	TTL	12/24	B	(Note 6)	(Note 6)
MA3	125	IO	TTL	12/24	B	(Note 6)	(Note 6)
MA4	126	IO	TTL	12/24	B	(Note 6)	(Note 6)
MA5	127	IO	TTL	12/24	B	(Note 6)	(Note 6)
VDDRB	128	PWR			B Supply		
MA6	129	IO	TTL	12/24	B	(Note 6)	(Note 6)
MA7	130	IO	TTL	12/24	B	(Note 6)	(Note 6)
MA8	131	IO	TTL	12/24	B	(Note 6)	(Note 6)
MA9	132	IO	TTL	12/24	B	(Note 6)	(Note 6)
MA10/–WE1	133	IO	TTL	12/24	B	(Note 6)	(Note 6)
VSSR	134	GND			Ring Gnd		
–RAS2	135	IO	TTL	12/24	B	(Note 5)	(Note 5)
–RAS3	136	IO	TTL	12/24	B	(Note 5)	(Note 5)

PIN TYPE BY OPERATIONAL STATE (Cont.)

Pin Name	Pin No.	Pin Type	Input Type	Drive mA	Power Rail	Suspend Mode CPU On (Note 9)	Suspend Mode CPU Off (Note 9)
LA23	137	IO	TTL	12	C	PD	PD
LA22	138	IO	TTL	12	C	PD	PD
LA21	139	IO	TTL	12	C	PD	PD
LA20	140	IO	TTL	12	C	PD	PD
LA19	141	IO	TTL	12	C	PD	PD
LA18	142	IO	TTL	12	C	PD	PD
VDDRC	143	PWR			C Supply		
LA17	144	IO	TTL	12	C	PD	PD
SA19	145	O-TS		12	C	PD	PD
SA18	146	O-TS		12	C	PD	PD
SA17	147	O-TS		12	C	PD	PD
SA16	148	IO	TTL	12	C	PD	PD
SA15	149	IO	TTL	12	C	PD	PD
SA14	150	IO	TTL	12	C	PD	PD
SA13	151	IO	TTL	12	C	PD	PD
SA12	152	IO	TTL	12	C	PD	PD
SA11	153	IO	TTL	12	C	PD	PD
SA10	154	IO	TTL	12	C	PD	PD
SA9	155	IO	TTL	12	C	PD	PD
VSSR	156	GND			Ring Gnd		
SA8	157	IO	TTL	12	C	PD	PD
SA7	158	IO	TTL	12	C	PD	PD
SA6	159	IO	TTL	12	C	PD	PD
SA5	160	IO	TTL	12	C	PD	PD
SA4	161	IO	TTL	12	C	PD	PD
SA3	162	IO	TTL	12	C	PD	PD
VSSI	163	GND			Core Gnd		
SA2	164	IO	TTL	12	C	PD	PD
VDDRC	165	PWR			C Supply		
SA1	166	IO	TTL	12	C	PD	PD
SA0	167	IO	TTL	12	C	PD	PD
AEN	168	O-TS		12	C	PD	PD
RSTDRV	169	O-TS		12	C	PD	PD
SD15	170	IO	TTL	12	C	PD	PD

PIN TYPE BY OPERATIONAL STATE (Cont.)

Pin Name	Pin No.	Pin Type	Input Type	Drive mA	Power Rail	Suspend Mode CPU On (Note 9)	Suspend Mode CPU Off (Note 9)
SD14	171	IO	TTL	12	C	PD	PD
SD13	172	IO	TTL	12	C	PD	PD
SD12	173	IO	TTL	12	C	PD	PD
SD11	174	IO	TTL	12	C	PD	PD
SD10	175	IO	TTL	12	C	PD	PD
SD9	176	IO	TTL	12	C	PD	PD
SD8	177	IO	TTL	12	C	PD	PD
VDDIC	178	PWR			C Core		
SD7	179	IO	TTL	12	C	PD	PD
SD6	180	IO	TTL	12	C	PD	PD
SD5	181	IO	TTL	12	C	PD	PD
VSSR	182	GND			Ring Gnd		
SD4	183	IO	TTL	12	C	PD	PD
SD3	184	IO	TTL	12	C	PD	PD
SD2	185	IO	TTL	12	C	PD	PD
SD1	186	IO	TTL	12	C	PD	PD
SD0	187	IO	TTL	12	C	PD	PD
–SMEMW	188	O-TS (Note 2)		12	C	HI-Z	HI-Z
–SMEMR	189	O-TS (Note 2)		12	C	HI-Z	HI-Z
–IOW	190	IO (Note 2)	TTL (Note 10)	12	C	HI-Z	HI-Z
–IOR	191	IO (Note 2)	TTL (Note 10)	12	C	HI-Z	HI-Z
–REFRESH	192	IO-OD (Note 1)	TTL-S (Note 10)	12	C	HI-Z	HI-Z
SYSCLK	193	O-TS		12	C	PD	PD
IOCHRDY	194	IO	TTL (Note 10)	12	C	PD	PD
–IOCHCK	195	I	TTL (Note 10)		C	PD	PD
VDDRC	196	PWR			C Supply		
–WS0	197	I	TTL (Note 10)		C	PD	PD
–SBHE	198	IO	TTL	12	C	PD	PD
DRQ3	199	I	TTL		C	PD	PD
DRQ2	200	I	TTL		C	PD	PD
DRQ1	201	I	TTL		C	PD	PD
IRQ9	202	I	TTL		C	PD	PD
IRQ7	203	I	TTL		C	PD	PD
IRQ6	204	I	TTL		C	PD	PD

PIN TYPE BY OPERATIONAL STATE (Cont.)

Pin Name	Pin No.	Pin Type	Input Type	Drive mA	Power Rail	Suspend Mode CPU On (Note 9)	Suspend Mode CPU Off (Note 9)
IRQ5	205	I	TTL		C	PD	PD
IRQ4	206	I	TTL		C	PD	PD
IRQ3	207	I	TTL		C	PD	PD
VSSR	208	GND			Ring Gnd		

Notes:
1. These pins are normally open-collector signals and require an external pull-up resistor.
2. These pins require an external pull-up resistor (10 kΩ is recommended).
3. These pins are pulled down externally at the processor.
4. These pins are pulled up externally at the processor.
5. These pins operate during the Suspend Mode. If the VL82C316's core is powered off, they become three-state.
6. These pins are normally driven during the Suspend Mode. If the VL82C316's core is powered off, they become three-state.
7. PD indicates a high-impedance state with approximately 20 kΩ minimumresistance to VSS. A programmable pull-down cell is used on these lines.
8. Depending on the state of configuration bit, CPU (local bus interface) can remain powered in the Suspend Mode.
9. These pads have an input that is gated inactive during the Suspend Mode.

Legend:

CMOS	CMOS-compatible input
GND	Ground pin
HI-Z	A very high-impedance condition.
I	Input-only pin
IO	Bidirectional pin
PWR	Power supply pin
TTL	TTL-compatible input
-PD	Indicates a high-impedance with approximately 10 kΩ minimum resistance to VSS.
-PU	Indicates a high-impedance with approximately 10 kΩ minimum resistance to VDD.
-TS	Three-state pin
-S	Indicates a Schmitt-trigger input with hystersis for noise immunity.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
CPU INTERFACE SIGNALS		
A23-A1	71-81, 83-89 90-95	Address bus bits 23 through 1 - These pins are inputs during any CPU cycle. They become outputs during any HLDA cycle and are driven by the DMA controller, refresh counter or the SA or LA bus in the Master Mode. These bits allow direct access for up to 16 MB of memory.
–ADS	45	Address Strobe - Driven by the CPU as an indication that the address and control signals currently supplied by the CPU are valid. –ADS is driven by the VL82C316 when HLDA is active and goes low for one CPU clock cycle at the beginning of DMA or Master Mode cycles when a local bus region is selected by the PMR Registers.
–BHE	34	Byte High Enable - An active low signal that is driven by the CPU. It is used to select the upper byte of a 16-bit wide memory location. –BHE is driven by the VL82C316 when HLDA is active and indicates the upper byte contains valid data in a 16-bit DMA or Master Mode transfer between slot I/O and a local bus peripheral.
–BLE	44	Byte Low Enable - When in 386SX Mode, this active low signal is driven by the CPU. It is used to select the lower byte of a 16-bit wide memory location. –BLE is an input during CPU cycles and an output during HLDA cycles. –BLE is driven by the VL82C316 when HLDA is active. It indicates the lower byte contains valid data in a 8- or 16-bit DMA or Master Mode transfer between slot I/O and a local bus peripheral.
–BUSYCPU	35	Busy CPU - An active low output sent to the CPU that is generated from three sources. It always occurs in response to the –BUSYNPX input. It is also derived from –ERRORNPX and at system reset. –BUSYCPU toggles every refresh period when a coprocessor access is made when a cache controller is present and the coprocessor is absent in the system. This is to prevent system hang-up. –BUSYCPU is set low at power-up reset. It is set high at any software reset.
CLK2	48	Clock - This output signal is a CMOS level signal which is the frequency of, and in phase with, the TCLK2 signal. It is output to the CPU and other on-board logic for synchronization.
CLK2IN	46	Clock - This is the main clock input to the VL82C316 state machine and is connected to the CLK2 signal that is output by the VL82C316.
D/–C_DK1	41	Data or Code Enable or Decode bit 1 - This pin has three functions depending on the operating mode. It is Data or (active low) Code enable driven by the CPU. This signal is decoded with the remaining CPU control signals to indicate the type of bus cycle requested. See W/–R_DK2 definition for bus cycle types. During DMA acknowledge cycles, this is an output signal which along with DK0 and DK2 represents the encoded channel number being serviced. When the VL82C316 makes –ADS active during DMA or Master Mode cycles for local bus accesses, this signal is forced high.
D15-D0	70, 69, 67-63 61, 60, 58-52	CPU Data bus bits 15 through 0 - This is the data bus directly connected to the CPU. It is also referred to as the local data bus. D15-D8 require pull-up resistors for AT compatibility.
DKEN	30	Decoder Enable - An active high signal which enables an external 3-to-8 decoder for the generation of the DMA acknowledge signals from DK2-DK0. This pin, along with the pin –RAMW/–WE0, is used at power-on reset to select the frequency of the bus clock (SYSCLK) for normal operation. Refer to the section titled "System Configuration" for more details.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
HLDA	51	Hold Acknowledge - This active high signal is issued by the CPU in response to the HRQ driven by the VL82C316. It indicates that the CPU is floating its outputs to the high impedance state so that another master may take control of the bus.
HRQ	50	Hold Request - This active high output signal is driven by the VL82C316 to the CPU. It indicates that a bus master, such as a DMA or refresh controller, is requesting control of the bus. It is synchronized to CLK2.
INTR	32	Interrupt Request - This signal is used to interrupt the CPU and is generated by the 82C59A megacells any time a valid interrupt request input is received.
M/–IO_DK0	42	Memory or (active low) I/O enable - This signal is driven by the CPU. M/–IO is decoded with the remaining CPU control signals to indicate the type of bus cycle requested. See W/–R definition for bus cycle types. During DMA acknowledge cycles, this is an output signal which along with DK1 and DK2 represents the encoded channel number being serviced. When the VL82C316 makes –ADS active during DMA or Master Mode cycles for local bus accesses, this signal is driven by the VL82C316 to indicate whether a memory or I/O access is required.
NMI	33	Non-Maskable Interrupt - An output used to drive the NMI input to the CPU. It is asserted by either a parity error or an I/O channel error. The NMI output is enabled by writing a 0 to bit D7 of I/O port 70h. NMI is disabled on reset.
PEREQCPU	34	Processor Extension Request - An active high signal sent to the CPU in response to a PEREQNPX which is issued by the coprocessor to the VL82C316. It indicates to the CPU that the coprocessor is requesting a data operand to be sent to or from memory by the CPU. For PC/AT compatibility, PEREQCPU is returned active on occurrence of an –ERRORNPX after –BUSYNPX has gone inactive. A write to F0h by the interrupt 13 handler returns control of the PEREQCPU signal to directly follow the PEREQNPX input.
–READY	49	Ready - This active low signal is driven by the VL82C316 as an indication that the current memory or I/O bus cycle is complete. –READY is the synchronized version of IOCHRDY during slot bus accesses. An external pull-up resistor is required. When the SMM Mode is enabled (SMMEN, bit 7 of the SMMCTL Register is set to 1), and the Composite Ready Mode is active (SMMRDY, bit 4 of the MISCSET Register is set to 0), –READY is also generated to complete cycles started with –SADS. This is used for compatibility with Cyrix CPUs. The VL82C316 enables the –READY three-state output only when it needs to drive it low and leaves it enabled for two CLK2 cycles after it has driven it high again. When HLDA is active, –READY is an input to the VL82C316 and is driven by local bus devices to terminate DMA and Master Mode cycles.
RESCPU	36	Reset CPU - An active high signal sent to the CPU by the VL82C316. It is issued in response to the control bit for software reset located in the Port A Register or a dummy read from I/O port EFh. It is also issued in response to the –RESET input and in response to detection of a shutdown command. In all cases it is synchronized to CLK2.
TCLK2	99	Clock - This input is connected to a crystal oscillator whose frequency is twice the system frequency. The CMOS level oscillator output is internally buffered and sent to the CLK2 output.
W/–R_DK2	40	Write or (active low) Read or Decode bit 2 - This pin has three functions depending on the operating mode. It is write or active low read enable input driven by the CPU. This signal is decoded with M/–IO_DK0 and D/–C_DK1 to indicate the type of bus cycle requested. The bus cycle types include interrupt acknowledge, halt, shutdown, I/O reads and writes, memory data reads and writes, and memory code reads. During DMA acknowledge cycles, this is an output signal which along with DK0 and DK1 represents the encoded channel number being serviced.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
		When the VL82C316 makes –ADS active during DMA or Master Mode cycles for local bus accesses, this signal is driven by the VL82C316 to indicate whether a read or write cycle is required.
ON-BOARD MEMORY SYSTEM INTERFACE SIGNALS		
–CAS3 - –CAS1	112, 114-116	Column Address Strobe bits 3 through 0 - These signals are sent to their respective RAM banks to strobe in the column address during on-board memory bus cycles. There is a –CAS signal for upper and lower bytes of each of the two 16-bit DRAM memory banks. The active period for this signal is determined by the number of wait states and Page Mode configuration. When –RESET is low, these pins are three-stated until the fourth –ADS. Therefore, external pull-ups are required.
MA10/–WE1, MA9-MA1	133-129, 127-124, 122, 121	Memory Addresses 10 through 0 or Write Enable bit 1 - These address bits are the row and column addresses sent to the on-board memory. They are buffered and multiplexed versions of the CPU bus addresses. They allow addressing of up to 16 MB of memory. The MA10-MA0 pins are used at power-on reset (–RESET) for configuration purposes. Refer to the section titled "System Configuration" for details. With 512Kx8 DRAMs installed (bit 7, MAP512K, of the RAMMAP Register set to 1), MA10 becomes a Write Enable output (–WE1) to control Banks 2 and 3 to provide up to 8 MB capability.
–RAMW/–WE0	117	RAM Write or Write Enable bit 0 - This active low signal is output to the DRAM memory to control the direction of data flow of the on-board memory. It is a result of the address and bus control decode. It is active during on-board memory write cycles and high at all other times. –RAMW is used at power-on reset (–RESET) for configuration purposes. When –RESET is low this pin is three-stated. Refer to the section titled "System Configuration" for details. With 512Kx8 DRAMs installed (bit 7, MAP512K, of the RAMMAP Register set to 1), –RAMW becomes a Write Enable output –WE0 to control Banks 0 and 1 to provide up to 8 MB capability.
–RAS3 - –RAS0	136, 135 120, 118	Row Address Strobe bits 3 through 0 - These active low signals are sent to their respective RAM banks to strobe in the row address during on-board memory bus cycles.
COPROCESSOR SIGNALS		
–BUSYNPX	107	Coprocessor Busy - An active low input signal driven by the coprocessor to indicate that it is currently executing a previous instruction and is not ready to accept another. This signal is decoded internally to produce IRQ13 and to control PEREQCPU.
–ERRORNPX	108	Coprocessor Error - An active low signal from the coprocessor to indicate that an error has occurred in the previous instruction. This signal is internally gated and latched with –BUSYNPX to produce IRQ13.
PEREQNPX	105	Coprocessor Extension Request - An active high input signal driven by the coprocessor to indicate that it needs transfer of data operands to or from memory. For PC/AT compatibility, this signal is also gated with the internal ERROR/BUSY control logic before being output to the CPU as PEREQCPU during NPX interrupts.
RESNPX	106	Coprocessor Reset - This output is connected to the coprocessor reset input. It is triggered through an internally generated system reset or via a write to port F1h. In the case of a system reset, the RESCPU signal is also activated. A write to port F1h resets only the coprocessor. The coprocessor instruction FINIT should be executed after an F1h generated reset in a 386SX-based system. Otherwise the 387SX is not initialized to the same state that a 287 is placed in by a hardware reset alone. For compatibility, the F1h reset may be disabled by setting bit 6 (F1CTL) of the MISCSET Register.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
SD, SA, AND LA SYSTEM BUSES		
SD15-SD0	170-177, 179-181, 183-187	System Data bus bits 15 through 0 - This bus connects directly to the slots. It is used to transfer data to and from the low byte of local and system devices.
LA23-LA17	137-142, 144	Latchable Address bus bits 23 through 17 - This bus is an output during all CPU and DMA cycles. It becomes an input during external Bus Master cycles and is driven low during refresh cycles.
SA19-SA17	145-147	System Address bus bits 19 through 17 - This bus is always an output, but is driven low during refresh cycles.
SA16-SA9	148-155	System Address bus bits 16 through 5 - This bus is always an output during CPU and DMA cycles. It becomes an input during external Bus Master cycles. These pins are three-stated during refresh cycles.
SA8-SA0	157-162, 164, 166, 167	System Address bus bits 8 through 0 - This bus is always an output during CPU and DMA cycles. It becomes an input during external Bus Master cycles and contains the refresh counter address during refresh cycles.
PERIPHERAL INTERFACE SIGNALS		
–LBA	97	Local Bus Access - This input signal must be driven low by a local bus peripheral before half-way through the first T2 or T1P cycle of any CPU bus cycle. It causes the VL82C316 to ignore the current command, allowing the peripheral to complete the cycle. Local bus accesses to memory devices may also be internally triggered based on programmable decodes. See the section titled "Local Bus Peripheral Support" for full details. When –LBA is active, the VL82C316 does not generate –READY. Instead, the –READY pin is monitored by the VL82C316 for the –READY signal generated by local bus peripheral. Until bit 4 (LBAEN) of the BUSCTL1 Register is changed from the default value of 0 to 1, –LBA is ignored.
–ROMCS/ –PPICS	29	ROM Chip Select and Peripherial Chip Select - The –ROMCS output is active only in the CPU Mode (HLDA is low). It is active any time the address on the A bus selects the address range between FE0000h and FFFFFFh or 0E0000h and 0FFFFFh during a memory read or write cycle except in regions for which shadow RAM is enabled. –PPICS can be used for real-time clock and/or keyboard controller chip selects if external devices are used instead of the built-in components. Activation of –PPICS occurs during I/O reads or writes per the following table: **–PPICS** — **INT KBC** 70h, 71h — Enabled 60h, 64h, 70h, 71h — Disabled In the later case, external circuitry is required to generate separate chip selects from the composite chip select. Note that –PPICS always decodes 70h and 71h regardless of whether the internal real-time clock is enabled via RENA (bit 0 of the RTCLSB Register). This simplifies the design for systems wishing to use both the internal and an external real-time clocks simultaneously. However, –PPICS decodes keyboard controller accesses only if the internal keyboard is disabled via the hardware or software methods described in this document. –PPICS is never activated during HOLD cycles, but it may be activated during Master Mode accesses; i.e., –PPICS is blocked when AEN is active. This pin is used for used for system configuration purposes at power-on reset. Refer to the section titled "System Configuration" for details.
–SLEEP	109	Sleep - This active low input signal enables the system controller's Sleep Mode features.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
SPKR/–TRI	101		Speaker or Three-State - This output drives an externally buffered speaker. It is created by gating the output of Timer 2. Bit 1 of port B, 61h, is used to enable the speaker output and bit 0 is used to gate the output of the timer. This signal is an input when the –RESET input is low. If this input is sampled low, it forces the VL82C316 into the Three-State Mode where all outputs and bidirectional pins are driven to a high impedance state.
WAKEUP/ –MISS	98		Wakeup or Cache Miss - In systems using the VL82C325 (SX) Cache Controller or a discrete cache implementation, the internal CACHEN configuration bit (bit 3 of the MISCSET Register) is set in order to configure pin 98 as the –MISS input from the cache controller. In the default state (CACHEN reset 0), the state of this pin is ignored. In 32-bit systems where the VL82C3216 Cache Controller and Interface Unit is used with the VL82C316 rather than the VL82C325, this pin must be configured as WAKEUP. This is done by setting bit 3 (CACHEN) of the MISCSET Register to 0 and bit 7 (WAKEUP) of the RAMSET Register to 1. In this mode, WAKEUP is an output signal driven low during DMA or Master Mode cycles. WAKEUP must be externally ORed with the –SLEEP signal. The ORed output is then connected to the VL82C3216's –SLEEP input.

MISCSET, Bit 3	RAMSET, Bit 7	Description
0	0	Inactive Input Mode (Default)
0	1	WAKEUP Output Active
1	X	–MISS Input Active

BUS INTERFACE SIGNALS

AEN	168		Address Enable - This output goes high any time the inputs HLDA and –MASTER are both high.
BALE	10		Buffered Address Latch Enable - An active high pulse which is generated at the beginning of any bus cycle initiated from the CPU which is not directed to on-board DRAM. BALE is forced high anytime HLDA is high.
–BLKA20	96		Block A20 - The logic OR of the internal A20GATE signal and Port A bit 1. On reset, the state of this pin determines whether to use the internal register defaults or the external jumper settings. This pin requires an external pull up or pull down resistor. Refer to section titled "System Configuration" for details.
BUSOSC	100		Bus Oscillator - This signal is supplied from an external oscillator. It is used for AT bus operations and for non-Turbo processor cycles. If SYSCLK is to be derived from TCLK2, the BUSOSC input is used to determine the clock divisor to be used. During normal operation, the BUSOSC pin can be used in conjunction with an internal register to select SYSCLK to be TCLK2 +2, +4, +6, or +8. If an oscillator is connected to this pin, SYSCLK can be programmed to be BUSOSC +2, +4, +6, or +8. In some applications an external pull-up or pull-down is required on this pin. Refer to the section titled "Clock Generation" for details.
DRQ7-DRQ5 DRQ3-DRQ0	17-15, 199-201, 14		Request - These asynchronous DMA request inputs are used by external devices to indicate when they need service from the internal DMA controllers. DRQ3-DRQ0 are used for transfers between 8-bit I/O adapters and system memory. DRQ7-DRQ5 are used for transfers between 16-bit I/O adapters and system memory. DRQ4 is not available externally as it is used to cascade the two DMA controllers together.
–IOCHCK	195		I/O Channel Check - An active low input signal used to indicate that an error has taken place on the I/O bus. If I/O checking is enabled, an –IOCHCK assertion by a peripheral device generates an NMI to the processor.
IOCHRDY	194		I/O Channel Ready - This input is pulled low in order to extend the read or write cycles of any bus access when required. The cycle can be initiated by the CPU, DMA controllers, Masters, or refresh controller. The default number of wait states for cycles initiated by the CPU are four wait states for 8-bit peripherals, one wait state for 16-bit peripherals and three wait states for ROM cycles. Any peripheral that can not present read data or strobe in write data in this amount of time must use IOCHRDY to extend these cycles.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
		If HLDA is active, IOCHRDY will be driven low for a valid DMA or Master Mode cycle access to a local bus peripheral (defined by the PMR Registers) to allow for local bus latency. IOCHRDY is driven high for one clock cycle after –READY is sampled low (driven by a local bus device), then three-stated.
–IOCS16	4	16-bit I/O Chip Select - This input is used to determine when a 16-to-8 bit conversion is needed for CPU accesses. A 16-to-8 bit conversion is done any time the VL82C316 requests a 16-bit I/O cycle and –IOCS16 is sampled high.
–IOR	191	I/O Read - This signal is an input when HLDA is high and –MASTER is low. It is an output at all other times. When HLDA is low, –IOR is driven from the 82288 bus controller megacell. When HLDA is high and –MASTER is high, –IOR is driven by the 82C37A DMA controller megacells. This pin requires an external pull-up resistor.
–IOW	190	I/O Write - This signal is an input when HLDA is high and –MASTER is low. It is an output at all other times. When HLDA is low, –IOW is driven from the 82288 bus controller megacell. When HLDA is high and –MASTER is high, –IOW is driven by the 82C37A DMA controller megacells. This pin requires an external pull-up resistor.
IRQ15, IRQ14 IRQ12-IRQ9, IRQ7-IRQ3	8, 9, 7-5, 202, 203-207,	Interrupt Request bits 15, 14, 12 through 9, and 7 through 3- These inputs are the asynchronous interrupt request inputs for the 82C59A megacells. IRQ0, IRQ2 and IRQ13 are not available as external inputs to the chip, but are used internally. IRQ0 is connected to the output of the 82C54A Counter 0. IRQ2 is used to cascade the two 82C59A megacells together. IRQ13 is used for numeric coprocessor error. IRQ1 and IRQ8 are internally generated signals. See the section titled "Interrupt Controller Subsection" for their definitions. Also, all IRQ pins have a special programmable logic to reduce noise sensitivity. The logic is controlled by bit 0 (IRQIN) of the MISCSET Register. When IRQIN is set, the input to these pins must be stable for at least 105 ns to generate an interrupt.
–MASTER	18	Master - An active low input which is used by an external device to disable the internal DMA controllers and get access to the system bus. When asserted, it indicates that an external Bus Master has control of the bus.
–MEMCS16	3	Memory Chip Select 16-bit - This input is used to determine when a 16-to-8 bit conversion is needed for CPU accesses. A 16-to-8 bit conversion is done anytime the VL82C316 requests a 16-bit memory cycle and –MEMCS16 is sampled high.
–MEMR	12	Memory Read - When HLDA is high and –MASTER is low this signal is an input. It is an output at all other times. When HLDA is low, –MEMR is driven from the 82288 bus controller megacell. When HLDA is high and –MASTER is high, –MEMR is driven by the 82C37A DMA controller megacells. This pin requires an external pull-up resistor.
–MEMW	13	Memory Write - When HLDA is high and –MASTER is low this signal is an input. It is an output at all other times. When HLDA is low, –MEMW is driven from the 82288 bus controller megacell. When HLDA is high and –MASTER is high, –MEMW is driven by the 82C37A DMA controller megacells. This pin requires an external pull-up resistor.
OSC	2	Oscillator - This is the buffered input of the external 14.318 MHz oscillator.
PAR1/–OE1 PAR0/–OE0	111, 110	Parity bits 1 and 0 or Output Enable bits 1 and 0 - These bits are generated by the parity generation circuitry. They are written to memory along with their corresponding bytes during memory write operations. During memory read operations, these bits become inputs and are used along with their respective data bytes to determine if a parity error has occurred. PAR1 and PAR0 are used at power-on reset to program ROM wait states. Refer to the section titled "System Configuration" for details. These pins must be pulled up or down externally. With 512Kx8 DRAMs installed (bit 7, MAP512K, of the RAMMAP Register set to 1), these pins are tied to the DRAM Output Enable inputs to provide up to 8 MB capability. –OE1 controls Banks 2 and 3, while –OE0 controls Banks 0 and 1.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–RESET	102		System Power-on Reset - A low signal generates RESCPU, RESNPX, and RSTDRV and resets the values of the internal registers. In non-power managed systems, this input is usually connected to the PWRGD output of the system power supply. In power managed systems, an external RC reset circuit is used.
–SUSPEND	103		Suspend - If the Suspend Mode has been enabled (bit 7, SUSPACT, of the REFCTL Register is set to 1) and the –SUSPEND input is low, the 32 kHz Suspend Mode refresh is activated and all non-essential internal clocks are stopped. This pin should be tied high in systems not utilizing the Suspend Mode. In systems using the VL82C323 Power Management Unit (PMU) this pin is connected to the PWGOUT signal. The Suspend Mode has two possible states of operation: 1) Suspend Mode - CPU Off; 2) Suspend Mode - CPU On. These states of operation are based on the setting of bit 6 (CPUOFF-SUS) in the REFCTL Register. Refer to the REFCTL Register table for details.
–REFRESH	192		Refresh - This active low I/O signal is pulled low whenever a refresh cycle is initiated. It is used as an input to sense refresh requests from external sources such as Bus Masters. It is used internally to clock the refresh address counter and select a location in the memory mapper which drives A23-A17. –REFRESH is an open drain output capable of sinking 24 mA and requires an external pull-up resistor.
RSTDRV	169		Reset Drive - This active high output is a system reset generated from the –RESET input. RSTDRV is synchronized to the BUSOSC input.
–SMEMR	189		Memory Read - This signal is active during refresh cycles and memory read cycles to addresses below 1 MB. It requires an external pull-up resistor.
–SMEMW	188		Memory Write - This signal is active during memory write cycles to addresses below 1 MB. It requires an external pull-up resistor.
–SBHE	198		System Byte High Enable - This signal is controlled the same way as the SA bus. It is generated form a decode of the –BLE and –BHE inputs in the CPU Mode. –SBHE is forced low for 16-bit DMA cycles and forced to the opposite value of SA0 for 8-bit DMA cycles.
SYSCLK	193		System Clock - This output is 1/2, 1/4, 1/6, or 1/8 of the frequency of TCLK2 or BUSOSC depending on the BUSOSC pin status and the four lower bits in the CLKCTL Register. The bus control signals BALE, –IOR, –IOW, –MEMR, and –MEMW are synchronized to SYSCLK.
TC	1		Terminal Count - This output indicates that one of the DMA channels terminal count has been reached. It directly drives the system bus.
–WS0	197		Wait State 0 (terminate) - This input is pulled low by a peripheral on the S bus to terminate a CPU controlled bus cycle earlier than the default values defined internally on the chip.
KEYBOARD INTERFACE SIGNALS			
KCLK/IRQ1	27		Keyboard Clock or Interrupt Request bit 1 - When bit 4 (KBDEN) of the KBDCTL Register is set to 1, the internal keyboard controller is enabled and this pin is configured as T0/-P26 keyboard clock (AT and PS/2 Modes). If bit 4 is 0, the internal keyboard controller is disabled and its IRQ pin is logically disconnected from the 82C59A megacell. The interrupt output from an external keyboard controller is connected to this pin.
KDAT	26		Keyboard Data - When bit 4 (KBDEN) of the KBDCTL Register is set to 1, the internal keyboard controller is enabled and this pin is configured as T1/P27 keyboard data (AT Mode) or P10/-P27 keyboard data (PS/2 Mode). If bit 4 is 0, the internal keyboard controller is disabled and the KDAT pin becomes a three-stated output.
MCLK	25		Mouse Clock - When bit 4 (KBDEN) of the KBDCTL Register is set to 1, the internal keyboard controller is enabled and this pin is configured as mouse clock (PS/2 Mode). If bit 4 is 0, the internal keyboard controller is disabled and the MCLK pin becomes a three-stated output.
MDAT/ TURBORQ	24		Mouse Data or Turbo Request - When bit 4 (KBDEN) of the KBDCTL Register is set to 1, the internal keyboard controller is enabled and this pin is configured as mouse data (PS/2 Mode).

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
		If bit 4 is 0, the internal keyboard controller is disabled and the MDAT pin is logically disconnected from the internal keyboard controller. This pin then becomes a Turbo Request input and is internally combined with other Turbo Requests in order to generate a composite request signal.
REAL-TIME CLOCK (RTC) INTERFACE SIGNALS		
RTCBAT	19	Real-Time Clock Battery - Connected to the RTC hold-up battery between 2.4 and 5 volts.
–RTCIRQ	23	Real-Time Clock Interrupt Request - This pin is a bidirectional open drain RTC interrupt line at all times and requires an external pull-up. This allows the internal RTC to drive the output for compatibility with external power management units (PMUs) such as the VL82C323. It also allows an external RTC to drive –RTCIRQ. The –RTCIRQ signal is internally inverted before application to the 82C59A's IRQ8 input. By programming the internal RTC to an alternate address both the internal and an external RTC may be used.
RTCOSCI	21	Real-Time Clock Internal Oscillator - An input for the real-time clock crystal. It requires a 32.768 kHz external crystal or stand-alone oscillator.
RTCOSCO	22	Real-Time Clock Internal Oscillator - An input for real-time clock crystal. (See the description for RTCOSCI.) This pin is a no connect when an external oscillator is used.
PS/–RCLR	20	Power Sense or RTC Clear - The (active high) PS input signal is used to reset the status of the Valid RAM and Time (VRT) bit. This bit is used to indicate that the power has failed and that the contents of the RTC may not be valid. This pin is connected to an external RC network. Pulling PS/–RCLR low for at least 100 µs sets all bits in the internal RTC RAM.
SYSTEM MANAGEMENT MODE (SMM) INTERFACE SIGNALS		
–SMI/KEYSW	31	System Management Interrupt or Keyswitch - When the SMM is enabled (bit 7, SMMEN, of the SMMCTL Register is set to 1) this pin is defined as an I/O. The normal state of this pin is the input mode. It is possible for internal sources to cause the VL82C316 to generate an –SMI. When this occurs, the –SMI pin is driven low until the falling edge of –SADS. The –SMI pin then returns immediately to the input mode and continues monitoring the state of the –SMI input. –SMI is also driven out in response to an active low signal on the –SMIIN input (see below). In this case, –SMI follows –SMIIN and is not terminated by the VL82C316 at the falling edge of –SADS. As an output, this signal is always synchronized to CLK2. When the SMM is not enabled (bit 7 is 0), this pin is configured as an input and is connected to the P17 input of the keyboard controller. This allows use of an external PC/AT-compatible keyswitch circuit.
–SMIIN	28	Asynchronous System Management Interrupt Input - This input is connected to –SMIOUT from the VL82C323 or any asynchronous system –SMI source. This signal is synchronized to CLK2 and driven out on –SMI. The state of –SMIIN is ignored when the SMM is disabled (bit 7, SMMEN, of the SMMCTL Register is 0).
–SADS/ TURBOSW	37	SMM Address Strobe or Turbo Software Request - This signal is used to latch CPU addresses during accesses to SMM address space when –SMI is active. When the SMM is not enabled (bit 7, SMMEN, of the SMMCTL Register is 0), this pin is configured as an input and is internally combined with the output of the keyboard controller's P22 signal and internal software generated TURBO request sources in order to generate a composite TURBO request signal.
–SRDY	39	SMM Ready - This output is generated with the same timing as the standard –READY output, but only in response to cycles that start with activation of –SADS when the SMM is enabled (bit 7, SMMEN, of the SMMCTL Register is 1). When the SMM Ready Mode is active (RDYSMM, bit 4, of the MISCSET Register is 0), Ready for SMM cycles is also generated on the –READY pin.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
POWER AND GROUND PINS		
VDDRA	38, 62, 82	Pad-ring power connection for CPU and system interface signals.
VDDRB	119, 128	Pad-ring power connection to MA10/–WE1, MA9-MA0, –CAS3 - –CAS0, –RAS3 - –RAS0, –RAMW/–WE0, PAR1/–OE1, and PAR0/–OE0 pins.
VDDIAB	59	Core-logic power connection for VDDRA and VDDRB.
VDDRC	143, 165, 196	Pad-ring power connection for all ISA bus interface pins.
VDDIC	178	Core-logic power connection for VDDRC.
VSSR	11, 47, 68, 90, 104, 113, 123, 134, 156 182, 208	Pad-ring ground connection.
VSSI	163	Core-logic ground connection.

FUNCTIONAL DESCRIPTION

The VL82C316 can broadly be divided into two blocks - the System Controller Block and the ISA Bus Controller Block.

- System Controller Block - Includes the 82284 clock generator, ready generator, and the logic for address/ data bus control, memory control, and shutdown.
- ISA Bus Controller Block - Includes the dual 82C37A DMA controllers, dual 82C59A programmable interrupt controllers, 82C54A programmable interval timer, and the logic for refresh generation and refresh/DMA arbitration.

The following sections cover detailed operational information for the various logical groupings of VL82C316's subsystems. In most of these sections, the effect of configureable elements that can be controlled via I/O registers is discussed at length.

CPU INTERFACE

The VL82C316 handles the top level control interface between the synchronous local and memory data bus and the asynchronous slot data bus. It intercepts the CPU's bus status and address signals, then decodes the bus access. The interface of a 386SX with the VL82C316 is shown in Figure 1.

LOCAL BUS ACCESSES

Upon receiving the CPU's bus status signals and address, the VL82C316 latches these signals with –ADS. If the decoded address and M/–IO point to on-board memory, a bank request is issued to the on-chip DRAM controller. The DRAM controller then delivers the appropriate signals to the on-board memory. It senses when the data has been transferred and returns a –READY signal. –READY is externally gated with ready signals from the coprocessor or other external devices on the D bus to form the final –READY signal driven to the CPU. This –READY signal is synchronized properly with the CPU's CLK2 signal.

SLOT BUS ACCESSES

The CPU makes ISA bus accesses when the VL82C316 decodes the CPU's control signals as either an I/O cycle or an off-board memory access (the latter includes ROM accesses). In this case, the VL82C316 latches and decodes the CPU's control signals and handles control of the ISA transfer. The CPU is prevented from executing another ISA cycle until the previous slot cycle is completed. During an ISA cycle, the –READY signal returned to the CPU from the VL82C316 is delayed until the data transfer is over.

BUS ARBITRATION

DMAHRQ, DMAHLDA, and OUT1 are internal signals related to bus arbitration. The related external signals are HRQ and HLDA. When DMAHRQ (DMA Hold Request) is generated by the internal DMA controllers, the Hold Request signal (HRQ) is synchronized with the CPU clock and relayed to the CPU. The CPU responds with HLDA (Hold Acknowledge) to the VL82C316. In response, the internal signal DMAHLDA, which is an input to the DMA controllers, is generated and the bus control is transferred to either an internal DMA controller or an external master.

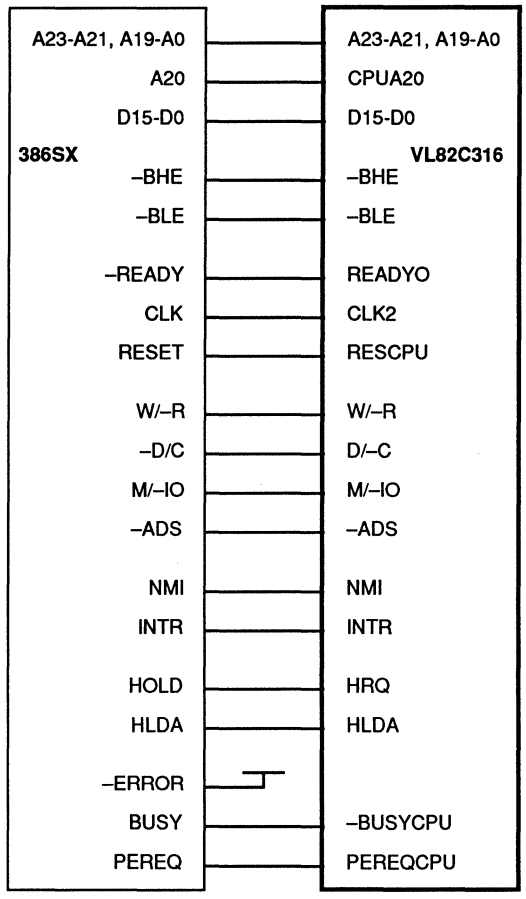
During a refresh cycle, OUT1 is generated internally from a timer. HRQ is sent to the CPU and HLDA is returned to indicate the CPU has given up the bus for refresh cycles.

SYSTEM RESET

System reset occurs in response to the –RESET signal.

There are three reset signals, RESCPU, RESNPX, and RSTDRV generated from the VL82C316. The

FIGURE 1. CPU INTERFACE



INTERFACE WITH 386SX

CPU reset signal, RESCPU, and the coprocessor reset signal, RESNPX, can be generated individually as described in the later sections or as a result of a system reset when RSTDRV is also generated.

When -RESET goes low, RSTDRV is driven high on the next rising edge of BUSOSC, which in turn three-states the -RAS and -CAS outputs. When -RESET goes high, RSTDRV goes low. The -RAS and -CAS outputs are then activated on the fourth high-to-low transition of the -ADS input. This is depicted in Figure 2.

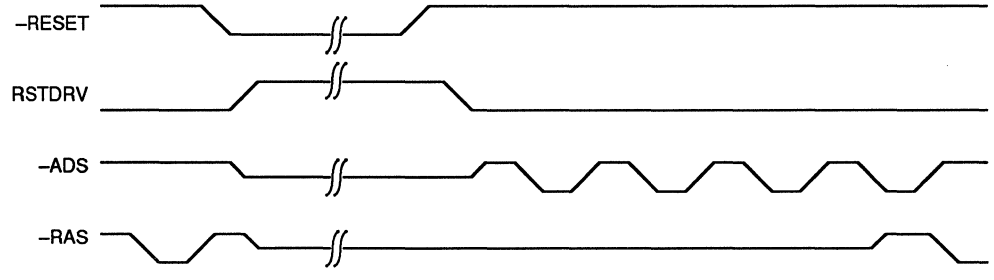
CPU-ONLY RESET

A CPU reset without a coprocessor reset can occur for one of three reasons. Two of the ways are usually used for switching from the Protected Mode to the Real Mode. One way of achieving this is by setting bit 0 of I/O port 92h to a 1 or by a dummy read of I/O port EFh. There is a 6.72 µs delay between the occurrence of either of the first two events and activation of the RESCPU signal. The second way is to generate the internal -RC signal by writing FCh or FEh to I/O port 64h. The RESCPU signal is generated after either 6.72 µs or approximately a 50 µs delay depending on the value of the FASTRC bit (bit 5) in the MISCSET Register.

Internal detection of a shutdown command from the CPU also triggers a CPU-only reset. Shutdown commands are properly decoded for 386SX/DX- and 486-based systems.

In all the above cases, reset is also synchronized to CLK2 and lasts for 16 CLK2 cycles.

FIGURE 2. RESET SEQUENCE



CPU SELF-TEST REQUEST
The CPU self-test request is generated only at system reset. This is achieved by activating the –BUSYCPU signal at least eight CLK2 cycles before the falling edge of RESCPU and disabling it at least eight CLK2 cycles after that edge of RESCPU.

The Self-Test Mode adds 21 ms (at 25 MHz) to the CPU reset time. At the end of the self-test, if desired, the BIOS can read the CPU Self-Test Result Register and perform whatever function is desired on failure.

Note that there is no self-test performed when a CPU-only reset is invoked. This results in the faster execution of a "Hot Reset."

NUMERIC COPROCESSOR INTERFACE

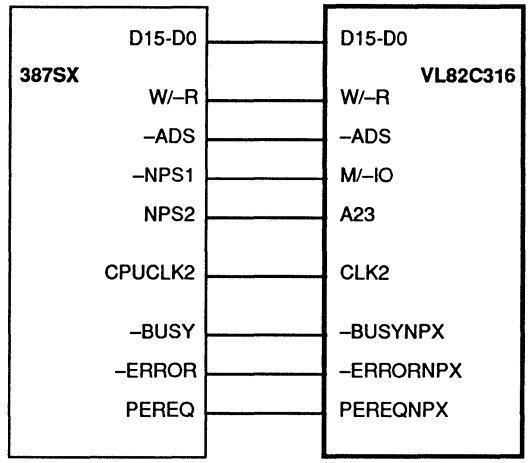
The VL82C316 supports the Intel i387™SX and compatible numeric coprocessors for use in high performance floating point math applications.

If the system contains a coprocessor, the interface signals –ERRORNPX, –BUSYNPX, and PEREQNPX are sent from the coprocessor to the VL82C316 and decoded to produce the proper interface signals for the CPU. The same decode determines activation of the RESNPX output to the coprocessor. This interface provides PC/AT compatibility for use with the 387SX.

The VL82C316 contains several dedicated pins in order to provide the interface between the coprocessor and the CPU. Figure 3 shows the interface between the VL82C316 and the coprocessor.

COPROCESSOR-ONLY RESET LOGIC
For PC/AT compatibility, logic for a coprocessor-only reset is provided via a dummy I/O write to F1h. This action provides a reset to the coprocessor synchronized to CLK2 of an 80 CLK2 cycle duration. –READY goes active 50 CLK2 cycles after the falling edge of RESNPX once a dummy write to F1h is performed. There may be incompatibility with some software due to the fact that a hardware reset does not put a 387SX into the same internal state as does the reset of a 287. For this reason, the F1h reset function may be disabled by setting bit 6 (F1CTL) of the MISCSET Register to 1.

FIGURE 3. NUMERIC COPROCESSOR INTERFACE



ERROR/INTERRUPT LOGIC
–ERRORNPX, when active, generates IRQ13 for PC/AT compatibility. It also latches –BUSYCPU. This is done in order to prevent the CPU from attempting to use the coprocessor until the error handling interrupt routine is executed. The interrupt handler inactivates the latched –BUSYCPU by performing a dummy write to I/O port F0h.

BUSY LOGIC
There are three sources that can generate the –BUSYCPU signal:

- It is always activated in response to the –BUSYNPX input.
- It is also generated by latching the –ERRORNPX signal (as described above).
- At system reset.

The state of –BUSYNPX is always passed through to –BUSYCPU indicating that the coprocessor is processing a command. On occurrence of an –ERRORNPX signal, it is latched and held active until occurrence of a write to ports F0h, F1h, or RESNPX. The former case is the normal mechanism used to reset the active latched signal. The latter two are resets. Since –ERRORNPX generates IRQ13 for PC/AT compatibility, –BUSYCPU is held active to prevent software access of the coprocessor until the interrupt service routine writes F0h.

Toggle Busy
The VL82C316 determines the presence of a coprocessor at reset. (–ERRORNPX is sampled immediately after RESET). If there is no coprocessor present, any attempts to access the coprocessor
(–IOR or –IOW with A23 high) will cause the –BUSYCPU signal to generate an active low pulse. This prevents system hang-up. (In some cached systems, this logic must be provided externally.)

PEREQ LOGIC
–BUSYNPX is latched in at the falling edge of the –ERRORNPX signal and ORed with the PEREQNPX signal to generate the PEREQCPU signal.

The PEREQCPU signal reflects only the PEREQNPX signal after a dummy write to the Coprocessor Busy Clear Register (I/O port F0h).

–READY LOGIC
The READY pin is asserted by the VL82C316 after 1 wait state for all coprocessor cycles. The coprocessor's –READY out should not be connected.

DRAM CONTROLLER

There can be up to four 16-bit banks used with the VL82C316. Each 16-bit bank of memory is further divided into two 8-bit banks. Each byte contains its own parity bit for a total of 18 bits per bank.

A single bank can consist of the following DRAM types:

QTY	DRAM Types Useable
18	256Kx1
18	1Mx1
18	4Mx1
6	four 256Kx4 + two 256Kx1
6	four 1Mx4 + two 1Mx1
4	512Kx8 (less parity)

The parts used in multiple banks can consist of all one DRAM type or mixtures of two types. It is not possible to use all three types in a single system simultaneously and not all combinations of any two types are supported.

The VL82C316 provides four –RAS and four –CAS signals. They can be used directly to drive two banks as shown in Figure 4.

When the VL82C316 is used in a system to support four banks of DRAM, –CAS0 and –CAS1 are used to drive the lower and upper byte, respectively, of Banks 0 and 2, while –CAS2 and –CAS3 are used to drive those of Banks 1 and 3. This connection is shown in Figure 5.

The drive of pins MA10/–WE1, MA9-MA0, and –RAMW/–WE0 is determined at power-on reset by the state of the MA9 pin. If pulled low, 150 pF drive is selected. The drive is 300 pF if MA9 is pulled up. MA9 must be either high or low at power-on reset. The drive of these pins can also be programmed by the RAMDRV bit (bit 2) of the MISCSET Register. RAMDRV is a read/write bit and reflects the state of MA9 at power-on reset.

512Kx8 DRAM SUPPORT

The VL82C316 supports up to 8 MB of DRAM using 512Kx8 DRAM chips. If this option is selected (bit 7 of the RAMMAP Register is set to 1), DRAM types cannot be mixed, only 512Kx8 DRAMs can be used for system memory. In this case, a bank consists of four chips or 2 MB per bank arranged as shown in Figure 6. The two parity pins (PAR1 and PAR0) become DRAM output enables (–OE1 and –OE0) and

FIGURE 4. TWO BANK DRAM SYSTEM

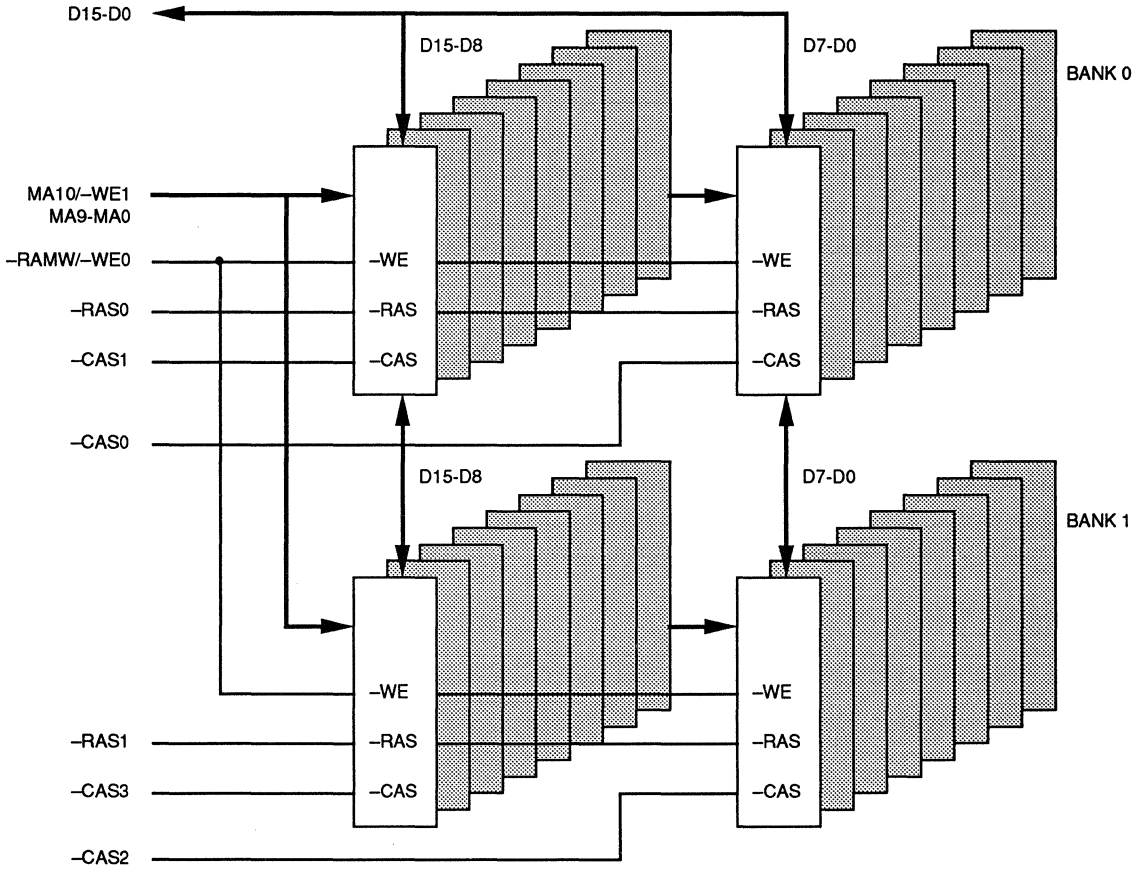


FIGURE 5. FOUR BANK DRAM SYSTEM

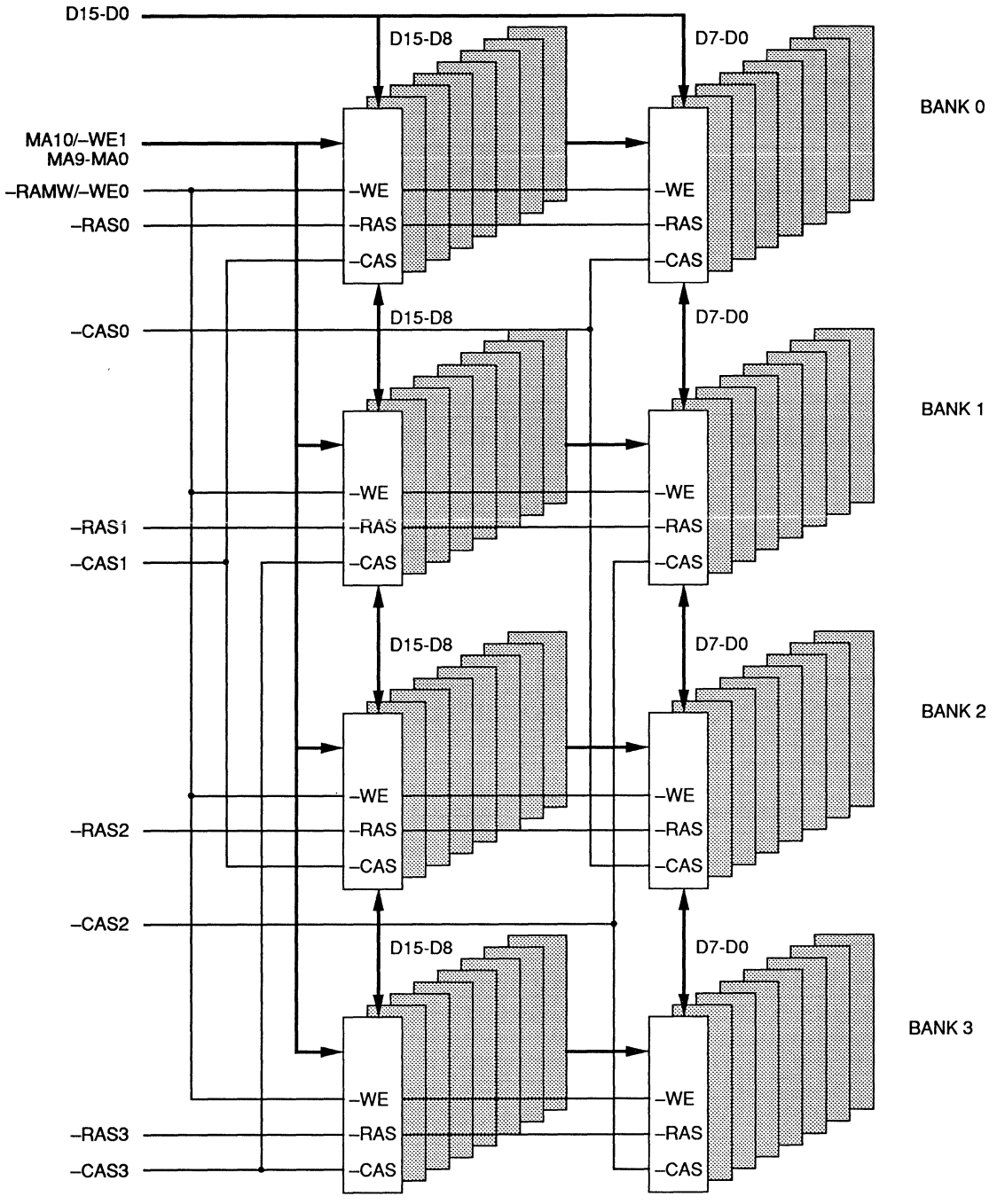
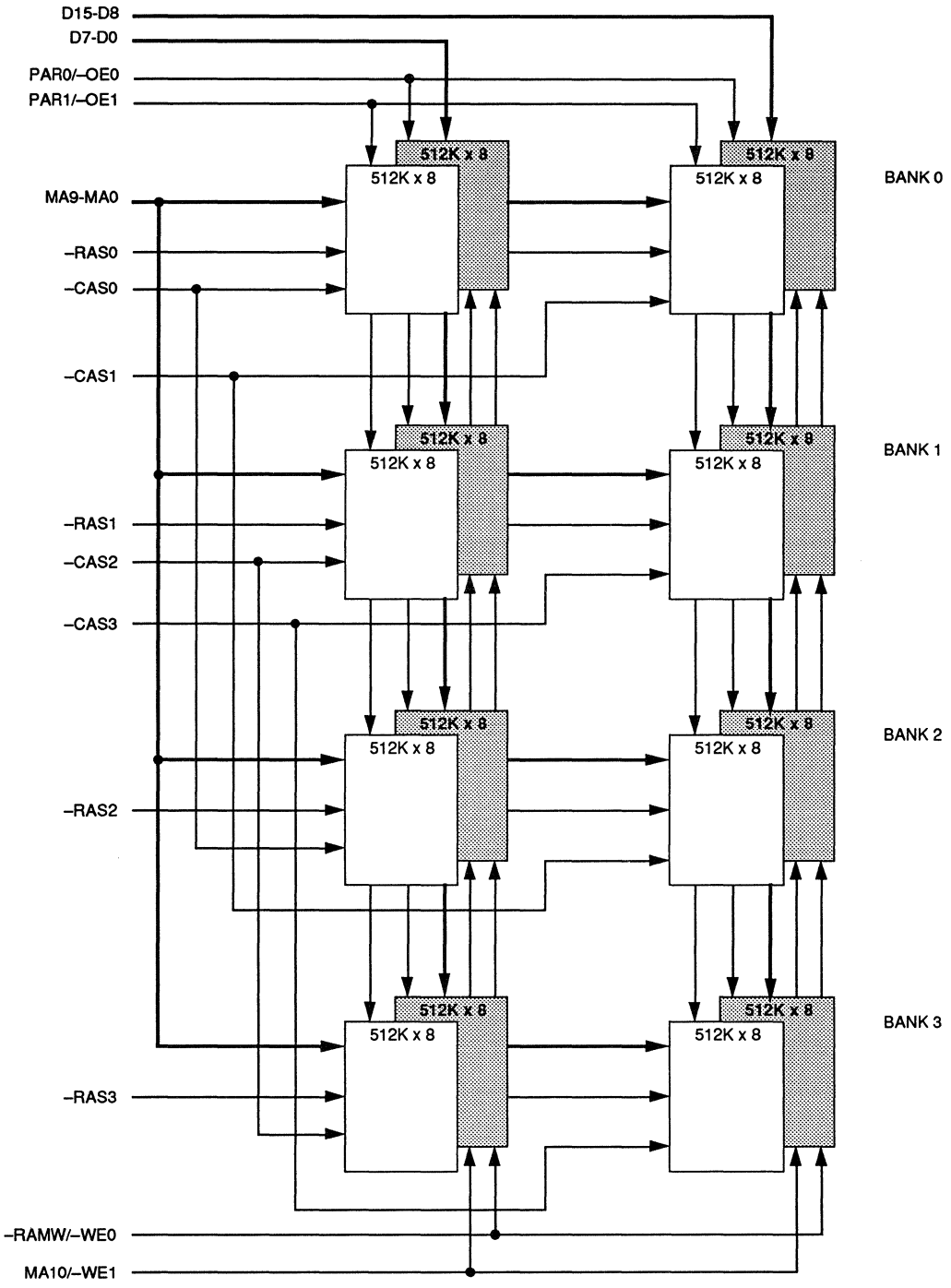


FIGURE 6. DRAM CONFIGURATION FOR 512K x 8: 2, 4, 6, AND 8 MB



MA10 becomes a second write enable (–WE1). Two-way interleaving is supported on 2 MB boundaries between Banks 0 and 1 or between Banks 2 and 3. The signals –OE0 and –WE0 control the enables for Banks 0 and 1 (Bank A) while signals –OE1 and –WE1 are connected to Banks 2 and 3 (Bank B). Figure 6 shows the 512Kx8 DRAM configuration.

MEMORY MAPS

The memory maps are selected by the RAMMAP Index Configuration Register via bits 3-0 (MEMAP3-MEMAP0). The VL82C316 supports 13 memory maps and two special cases. These maps are shown in Tables 1 and 2. The tables show the DRAM combinations that are addressable in each of four 16-bit memory banks. The MEMAP3-MEMAP0 column indicates the binary values written in bits 3-0 of the RAMMAP Register in order to select each map.

MEMAP1 and MEMAP0 indicate the number of populated banks when all the banks have similar DRAM types. MEMAP3 and MEMAP2 select DRAM type as follows.

MEMAP3, MEMAP2 = 00 => 256K
01 => 1M
10 => 4M
11 => Mixed DRAMS

MEMAP1, MEMAP0 = 00 => 1 Bank
01 => 2 Banks
10 => 3 Banks
11 => 4 Banks

When MEMAP3 and MEMAP2 = 11, MEMAP1 and MEMAP0 do not indicate the number of populated DRAM banks.

Note: Setting bit 7 (MAP512K) to a 1 selects 512Kx8 DRAM mapping regardless of the state of MEMAP3-MEMAP0. The value of MEMAP3-MEMAP0 should be set according to Tables 1 and 2 to select one of the 1M memory maps for 2, 4, 6, or 8 MB of total memory.

A memory map of Banks 0 and 1 populated with 256K DRAM allows EMS and shadowing, but no extended memory. A memory map with 0.5M total DRAM is the only case where there is no DRAM available for shadow, extended, or expanded memory. All other memory maps support shadow, expanded, and extended memory.

TABLE 1. DRAM MEMORY MAPS

Bank 3	Bank 2	Bank 1	Bank 0	Total Memory (MB)	384K Remap?	MEMAP3-MEMAP0
			256K	0.5	No	0000
		256K	256K	1.0	Yes	0001
	256K	256K	256K	1.5	No	0010
256K	256K	256K	256K	2.0	Yes	0011
			1M	2.0	Yes	0100
		1M	1M	4.0	Yes	0101
	1M	1M	1M	6.0	No	0110
1M	1M	1M	1M	8.0	No	0111
			4M	8.0	No	1000
		4M	4M	16.0	No	1001
	4M	0 or 256K	256K	8.0	No	1010 (Note 1)
4M	4M	0 or 256K	256K	16.0	No	1011 (Note 1)
	1M	256K	256K	3.0	Yes	1100
1M	1M	256K	256K	5.0	No	1101
	4M	1M	1M	12.0	No	1110

Note: 1. It is common for OEMs to directly solder in two banks of DRAM. Sockets are then provided for the other two banks as an end user upgrade. The VL82C316 has two special MEMAP options. They provide a way for the end user to obtain up to the maximum 16 MB of supported DRAM even when he has purchased a board with 512K or 1M of DRAM soldered in. For this option, 4M DRAM modules are plugged in Bank 2 and, optionally, Bank 3. The 256K DRAMs are disabled and the 4M DRAMs logically appear in the lower Banks, when either of the two special MEMAP codes are used (1010 or 1011).

2. If 512Kx8 DRAMs are used, MEMAP3-MEMAP0 should be set to one of the available 1M DRAM memory maps to select 2, 4, 6, or 8 MB of total memory. Two-way interleaving occurs on 2 MB boundaries.

TABLE 2. LOGICALLY REMAPPED DRAM MEMORY - SPECIAL CASES

Bank 3	Bank 2	Bank 1	Bank 0	Total Memory (MB)	384K Remap?	MEMAP3-MEMAP0
	Remapped		4M	8.0	No	1010
Remapped	Remapped	4M	4M	16.0	No	1011

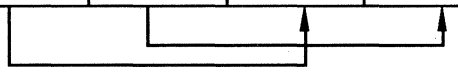


TABLE 3. PAGE/INTERLEAVE VERSUS MEMORY MAP

16-Bit DRAM Banks				Page/Interleave				Total Memory
B		A		Page Mode On		Page Mode Off		
Bank 3	Bank 2	Bank 1	Bank 0	B	A	B	A	
			256K		Page		Linear	0.5M
		256K	256K		2/P*		2/NP	1.0M
	256K	256K	256K	Page	2/P	Linear	2/NP	1.5M
256K	256K	256K	256K	2/P	2/P	2/NP	2/NP	2.0M
	1M	256K	256K	Page	2/P	Linear	2/NP	3.0M
1M	1M	256K	256K	2/P	2/P	2/NP	2/NP	5.0M
			1M		Page		Linear	2.0M
		1M	1M		2/P		2/NP	4.0M
	1M	1M	1M	Page	2/P	Linear	2/NP	6.0M
1M	1M	1M	1M	2/P	2/P	2/NP	2/NP	8.0M
	4M	1M	1M	Page	2/P	Linear	2/NP	12.0M
			4M		Page		Linear	8.0M
		4M	4M		2/P		2/NP	16.0M

* Two-way interleaving on page boundary of 1K.

PAGE MODE AND INTERLEAVE MODE OPERATIONS

Both Page Mode and Interleave Mode operations are available on system board DRAM in order to raise performance and decrease system cost. Table 3 shows the Page Mode and Interleave Mode options available for each possible memory map. These options are selected by programming the RAMSET and RAMMAP Configuration Registers. When bit –PGMD is set to 0, paging is active on all memory maps for the enabled bank pairs. The Page Mode can also be activated by pulling MA6 low at power-on reset. Interleaving requires pairs of banks. Detailed operation of each mode is given next.

Interleave Mode Operation
If both banks of a pair are populated with like DRAM types, two-way block interleaving occurs on a 1K boundary. If the four banks are not populated with like DRAMS, two-way interleaving occurs on pairs that are of the same type. In a system with three banks populated, the first two banks interleave but the third does not. Table 4 shows the interleaving options that occur versus the number of populated banks.

All combinations not shown are unsupported. There is no Configuration Register programmability for enabling the Interleave Mode. All interleaving options (none, or two-way) occur automatically as the result of the memory map programmed into the RAMMAP Register.

Tables 5, 6, and 7 show how the CPU address lines are used to accomplish the Interleave Mode options possible with the three supported DRAM types.

The top portion of each table shows the CPU address lines that are strobed onto MA10-MA0 by –CAS, the column address strobe. The middle portion of each table shows the CPU address lines strobed onto MA10-MA0 by –RAS, the row address strobe. The bank select box shows the CPU address bit(s) used for interleaving. The bank enable decodes further qualify whether the CPU address is in the range of current memory map.

TABLE 4. AUTOMATIC INTERLEAVE VERSUS POPULATED BANKS

Populated?		Bank B Address Mode	Populated?		Bank A Address Mode
Bank 3	Bank 2		Bank 1	Bank 0	
No	No	N/A	No	Yes	Linear
No	No	N/A	Yes	Yes	2-Way Interleave
No	Yes	Linear	Yes	Yes	2-Way Interleave
Yes	Yes	2-Way Interleave	Yes	Yes	2-Way Interleave

TABLE 5. 256K DRAM PAGE/ INTERLEAVE MAPPING

	No Interleave	2-Way Block Interleave	Memory Address
Column Address	3	3	0
	4	4	1
	5	5	2
	6	6	3
	7	7	4
	8	8	5
	9	9	6
	1	1	7
	2	2	8
			9
			10
Row Address	18	18	0
	17	17	1
	16	16	2
	15	15	3
	14	14	4
	13	13	5
	12	12	6
	11	11	7
	10	19	8
			9
			10
Bank Selects	19	10	
Bank Enable Decode	20	20	

TABLE 6. 1M DRAM PAGE/ INTERLEAVE MAPPING

	No Interleave	2-Way Block Interleave	Memory Address
Column Address	3	3	0
	4	4	1
	5	5	2
	6	6	3
	7	7	4
	8	8	5
	9	9	6
	1	1	7
	2	2	8
	10	11	9
			10
Row Address	18	18	0
	17	17	1
	16	16	2
	15	15	3
	14	14	4
	13	13	5
	12	12	6
	11	20	7
	19	19	8
	20	21	9
			10
Bank Selects	21	10	
Bank Enable Decode	22	22	

TABLE 7. 4M DRAM PAGE/ INTERLEAVE MAPPING

	No Interleave	2-Way Block Interleave	Memory Address
Column Address	3	3	0
	4	4	1
	5	5	2
	6	6	3
	7	7	4
	8	8	5
	9	9	6
	1	1	7
	2	2	8
	10	11	9
	11	12	10
Row Address	18	18	0
	17	17	1
	16	16	2
	15	15	3
	14	14	4
	13	13	5
	12	12	6
	20	20	7
	19	19	8
	21	21	9
	22	23	10
Bank Selects	23	10	
Bank Enable Decode			

Page Mode Operation
Page Mode is controlled by the –PGMD bit in the Configuration Register RAMSET. When low, this bit enables the Page Mode operation on all DRAM banks. The Page Mode can also be enabled at power-on reset by pulling MA6 low. When activated for a bank pair, Page Mode is active whether one bank or both are populated.

The Page Mode operation results in no additional wait state penalty for either reads or writes which immediately follow reads to the same DRAM page. A page-miss causes a two wait state penalty if a bank-hit, and a one wait state penalty if a bank-miss.

When pairs of banks are installed, interleaving is automatically enabled. The combination of Page Mode with Interleave Mode results in the best possible combination of fast system memory operation using the most cost-effective DRAMs. When accesses between interleaved banks occur, CAS precharging of the next bank to be accessed occurs while –CAS is active on the current bank. This has the effect of multiplying the effective page size by the number of banks being interleaved, thus increasing the odds of page-hit cycles.

Wait states by cycle type are shown below.

Cycle Type	0WS	1WS	2WS
Page-hit	0	1	1
Page-miss/ bank switch	1	1	2
Page-miss/ bank-hit	2*	3	4+
Non-Page Mode	0	1	2

* When the –FASTSX bit (bit 3) in the RAMSET Register is set, this option becomes three wait states.

\+ When the –FASTSX bit (bit 3) in the RAMSET Register is set, this option becomes five wait states.

DRAM Speed Versus Wait State Configuration
Refer to the VLSI application note "Interfacing System DRAM to SCAMP II Controller" (document #295312-001) for complete information on this topic.

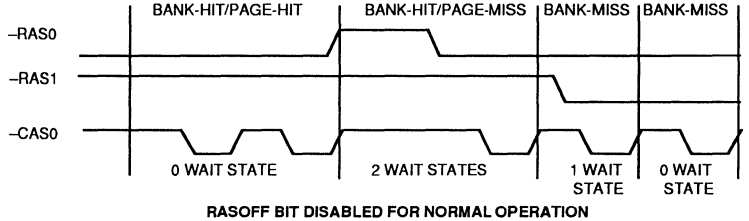
RAS SHUT-OFF
In a DRAM system, the row addresses are put on the memory address lines first. One of the –RAS signals is then used to latch in this address. The column address appears after it and is latched in with a –CAS signal. In a bank-hit/page-hit cycle, only a new column address is required because the successive memory accesses are in the same page. A new –CAS edge needs to be generated for this purpose but there is no need for a new –RAS edge as shown in Figure 7.

However, a new –RAS edge is required when the successive memory accesses are in different pages or different banks. If the accesses are in the same bank (page-miss cycle), the same –RAS (–RAS0 in Figure 7) signal requires a new edge. If a bank-switch occurs, a new edge should be on the other –RAS line (–RAS1 in Figure 7). The –RAS line has to be negated before a new edge can occur. The time from which it is negated to the time when a low going edge occurs is called RAS precharge time, which typically is a considerable portion of the DRAM access time.

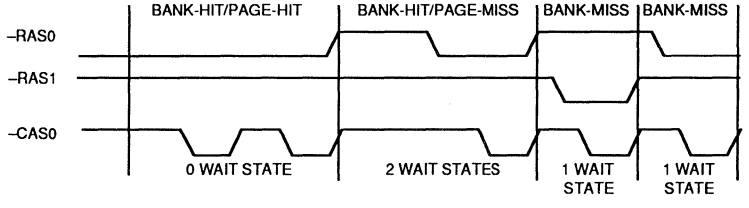
The bank-miss cycles are faster than the page-miss/bank-hit cycles because a different –RAS line can be activated as soon as a miss occurs. In the page-miss/bank-hit cycles, the same –RAS line must be precharged and then pulled low which is slower. In the VL82C316, a bank-miss cycle has one wait state while a page-miss/bank-hit cycle has a two wait state penalty.

In a normal Page Mode operation, both the –RAS lines are kept active when a bank-miss occurs. This expedites the memory accesses because there is no RAS precharge penalty. However, there is a price to be paid in higher power consumption. A DRAM bank consumes more power when –RAS is active. This can be a disadvantage in the Power Saving Mode. The power consumption is reduced by enabling the RASOFF bit (bit 0) in the RAMSET Register. This activates only one –RAS line, hence power is consumed in only one DRAM bank. The saving in power consumption is achieved at the expense of a slight loss in overall memory system performance.

FIGURE 7. RAS SHUT-OFF



RASOFF BIT DISABLED FOR NORMAL OPERATION



RASOFF BIT ENABLED FOR POWER SAVING

DRAM REFRESH

The VL82C316 supports the PC/AT-Compatible Refresh Mode with a refresh period of 15.625 µs and the Slow Refresh Mode with a refresh period that can be set to 125 or 250 µs. In the Slow Refresh Mode, the time to refresh the entire DRAM is 64 or 128 ms instead of the standard 4 ms. It performs the on-board DRAM refresh and controls both on- and off-board refresh timing. Refresh timing for both the system board and slot bus refreshes is performed in a synchronous manner. The REFCTL Register (Refresh Control Register) is provided to select the refresh period.

System Board Refresh

The entire system board DRAM is refreshed every 4, 64, or 128 ms as programmed by the bits REFSPD1 and REFSPD0 (bits 1 and 0) in the REFCTL Register. The refresh cycle can be a RAS-only refresh or a CAS-before-RAS refresh as selected by the REFMODE1 and REFMODE0 bits (bits 3 and 2) in the REFCTL Register. A special mode of CAS-before-RAS that switches to self-refresh during the Suspend Mode is also available. As a fourth alternative, refresh may be completely shut-off while leaving Timer 0 running. The type of refresh cycle should be programmed at power-on and the REFMODE1 and REFMODE0 bits should not be altered during normal operation.

Off-Board DRAM Refresh

The VL82C316 contains all the control circuitry necessary to generate a refresh cycle for the off-board DRAMs. The –MEMR signal will go low a minimum of one SYSCLK cycle after –REFRESH goes low. –MEMR will stay low for two SYSCLK cycles unless extended by IOCHRDY. A low on IOCHRDY will extend the –MEMR and –REFRESH pulse until IOCHRDY is returned high.

A 12-bit refresh address counter is included in the VL82C316. The address is driven onto the address lines A11-A0. Signals A16-A12 are driven to a logic 1 while the contents of the Page Register 74LS612 are driven on the lines A23-A17. The low-order eight bits of the address counter are also driven on to the slot bus SA7-SA0. At the end of the refresh cycle, when –REFRESH goes high, the counter is incremented to the next refresh address.

Self-Refresh Mode

The VL82C316 supports four different refresh options as described in the section titled "DRAM Registers." In three of the four options, the selected refresh option is active both in the Normal Operating Mode and in the Sleep Mode. However, self-refresh is a special case. When selected, CAS-before-RAS cycles are actually performed except while in the Suspend Mode. See below for more details.

Suspend Mode Refresh

An option is provided for a very low-power refresh during the Suspend Mode. In order to use this option, bit 7 (SUSPACT) of the REFCTL Register must be set to a logic 1. When set and a falling edge on the –SUSPEND signal is sensed and HLDA becomes active, refresh switches from using the OUT1 Timer pulse for refresh to using the real-time clock's 32 kHz oscillator as the time base. When a rising edge on the –SUSPEND signal occurs and HLDA is deactived, the time base switches back to use of the OUT1 Timer. The options programmed into REFSPD bits (bits 1 and 0 in the REFCTL Register) for the refresh rate and into the REFMODE bits (bits 3 and 2 in the REFCTL Register) for the type of refresh mode are applicable both when the OUT1 or the 32 kHz oscillator time base is used to trigger refresh cycles.

Note: The Suspend Mode is completely independent from the Sleep Mode. In order to use the Suspend Mode Refresh, the –SUSPEND pin must be pulled low with bit 7 (SUSPACT) in the REFCTL Register set to 1.

RAS-Only and CAS-before-RAS Refresh

When either of these modes are used, operation continues uninterrupted when switching to the Suspend Mode. The only change is in the refresh clock source from the OUT1 pulse to the 32 kHz oscillator when the –SUSPEND signal goes low. The clock source is switched back when the –SUSPEND signal returns high. For lowest power consumption, if –CAS before –RAS refresh is selected, the pull-ups on the CAS lines should be connected to a supply that collapses in Suspend Mode.

Self-Refresh Mode

This is the lowest power option if DRAMs are chosen that support this mode of operation. Operation is similar to the CAS-before-RAS operation, however, after the last CAS-before-RAS refresh upon entering the Suspend Mode, both –RAS and –CAS remain low. The DRAMs then begin to self-refresh within 16 ms. The –SUSPEND signal going inactive causes this mode to cease and normal CAS-before-RAS refresh, based on OUT1 timing, is begun. For lowest power consumption, the source for the pull-up resistors on the CAS lines or unused RAS lines should collapse in Suspend Mode.

DRAM REGISTERS

DRAM Map Register (RAMMAP)
The RAMMAP Index Configuration Register is used to select a memory map and remap a portion of the memory to the top of the existing memory. Its format is given in Table 8.

DRAM Control Register (RAMSET)
The RAMSET Index Configuration Register is used to select the Page or Non-Page Mode operation, to enable parity checking, and select the drive current on the memory address lines, (pins MA10/–WE1 and MA9-MA0) and –RAMW/–WE0 pin. Its format is given in Table 9.

Refresh Control Register (REFCTL)
The Refresh Control Register is used for programming the Refresh Mode, selecting the refresh period, and allows the BIOS to check for the Suspend Mode refresh option selected. The REFCTL Register format is given in Table 10.

TABLE 8. RAMMAP CONFIGURATION REGISTER (READ/WRITE)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
RAMMAP (03h)	MAP512K	ROMMOV1	ROMMOV0	REMP384	MEMAP3	MEMAP2	MEMAP1	MEMAP0
POR Value	0	MA8	MA7	MA4	MA3	MA2	MA1	MA0

Bit	Name	Function
7	MAP512K	512Kx8 DRAM Option: This bit defines whether 512Kx8 DRAMs are implemented in the system according to the following: MAP512K = 0: 512Kx8 DRAMs are not implemented. (Default) MAP512K = 1: 512Kx8 DRAMs are implemented up to 8 MB (four banks).
6, 5	ROMMOV1, ROMMOV0	System and Slot ROM Move Bits 1 and 0: These bits relocate video ROM and fixed disk ROM (address range C0000h to CFFFFh) to the system board and move the on-board ROM space E0000h to EFFFFh to the slot address range. The initial power-on reset value of these bits are set the same as pins MA8 and MA7 at the end of the reset period. Refer to the section titled "Relocating System and Slot ROM" for more details.
4	REMP384	Remap 384K Memory: This bit, when set, remaps 384K memory to the top of the current memory map. The remapping option is available only if the total memory is 1M, 2M, 3M, or 4M. The initial power-on reset value of this bit is set the same as pin MA4 at the end of the reset period. This bit is disabled if the total memory is not 1M, 2M, 3M, or 4M. Remapping is explained in the section titled "Remapping of Memory Range A0000h-FFFFh."
3-0	MEMAP3-MEMAP0	DRAM Memory Map bits 3-0: These bits specify one of the valid memory maps shown in Tables 1 and 2. The initial power-on reset value of these bits are set the same as pins MA3-MA0 at the end of the reset period.

TABLE 9. RAMSET CONFIGURATION REGISTER (READ/WRITE)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
RAMSET (05h)	WAKEUP	DELAY	DRAMWS1	DRAMWS0	–FASTSX	–PGMD	–ENPAR	RASOFF
POR Value	0	0	MA5	0	0	MA6	0	0

Bit	Name	Function
7	WAKEUP	Wakeup: The state of this bit and bit 3 (CACHEN) in the MISCSET Register determines whether the WAKEUP/–MISS pin is configured as the WAKEUP output or –MISS input. For use with the VL82C3216 Cache Controller and Interface Unit, the WAKEUP pin function must be enabled. This is done by setting this bit to 1 and bit 3 in the MISCSET Register to 0. In this mode, the WAKEUP pin output is driven low during DMA and Master Mode cycles. (WAKEUP must be externally ORed with –SLEEP. The ORed output is then connected to the VL82C3216's –SLEEP input.) Note: Setting bit 3 of the MISCSET Register clears this bit (WAKEUP). **MISCSET, Bit 3** / **RAMSET, Bit 7** / **Description** 0 / 0 / Inactive Input Mode (Default) 0 / 1 / WAKEUP Output Active 1 / X / –MISS Input Active
6	DELAY	Delay: This bit causes the internal cycle start to delay two CLK2 cycles after the rising edge of –ADS. It is only required for use with the VL82C325 Cache Controller in 33 MHz systems. This provides the VL82C325's –MISS signal the required propagation time before sampling by the VL82C316. This delay only occurs during memory read cache-miss cycles. 0 = No start delay (default). 1 = Start delay active.
5, 4	DRAMWS1, DRAMWS0	DRAM Wait States bits 1 and 0: These bits control the number of wait states to be inserted in each DRAM access. A wait state is defined as two CLK2 periods. **DRAMWS1** / **DRAMWS0** / **# of Wait States** 0 / 0 / 0 0 / 1 / 1 1 / X / 2 The initial power-on reset value of DRAMWS1 = 1 and DRAMWS0 = 0 indicating two wait state operation. Using a configuration jumper on the pin MA5, it is possible to select zero wait state operation at power-up (refer to section titled "System Configuration").
3	–FASTSX	Fast Page-Miss/Bank-Hit Cycles for 386SX: This bit, in conjunction with the DRAMWS1 and DRAMWS0 bits, decides the number of wait states to be introduced in page-miss/bank-hit DRAM access cycles in a 386SX-based system as follows (the default value of this bit is 0): **DRAMWS1** / **DRAMWS0** / **–FASTSX** / **# of Wait States** 0 / 0 / 0 / 2 0 / 0 / 1 / 3 0 / 1 / X / 3 1 / X / 0 / 4 1 / X / 1 / 5
2	–PGMD	Page Mode Banks A and B: This bit indicates whether Page Mode is active on Bank A (0 and 1) and Bank B (2 and 3). The Page Mode is disabled when –PGMD is set to 1. Resetting this bit to 0 enables the Page Mode. The initial power-on reset value of this bit is set the same as the MA6 pin at the end of the reset period.
1	–ENPAR	Enable Parity: Parity generation and checking is enabled when set to a 0 and disabled when set to a 1. The power-on reset default of this bit is 0.
0	RASOFF	RAS Shut-Off: This bit, when set to 1, enables only one –RAS line and disables all the other unused –RAS lines when a bank-miss occurs. When 0, it allows two –RAS lines to be active when a bank-miss occurs. The power-on reset default value of this bit is 0.

TABLE 10. REFCTL CONFIGURATION REGISTER (READ/WRITE)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
REFCTL (06h)	SUSPACT	CPUOFF-SUS	RSTREQ	HLTACT	REFMODE1	REFMODE0	REFSPD1	REFSPD0
POR Value	0	0	0	0	0	0	0	0

Bit	Name	Function
7	SUSPACT	Suspend Mode Active: When high and the –SUSPEND pin is pulled low, the Suspend Mode is enabled. In this mode, the 32 kHz time based refresh is begun and the self-refresh option is available. All non-essential internal clocks are stopped and leakage control is enabled. When SUSPACT is 0, all Suspend Mode features are disabled and the state of the –SUSPEND pin is ignored. The default value of this bit is 0.
6	CPUOFF-SUS	Suspend Mode: There are two options available. When set to 1, the VL82C316's pin state is set according to the "Suspend State - CPU Off" column in the "Pin Type by Operational State" table on page 6. The assumption is that the CPU, coprocessor, and any other local bus devices are powered down in this mode. When the Suspend Mode is exited, the VL82C316 generates RESCPU and RESNPX. When reset to 0, the VL82C316's pin state is set according to the "Suspend State - CPU On" column of the same table. The assumption is that the CPU, coprocessor, and any other local bus devices remain powered in this mode. When the Suspend Mode is exited, the VL82C316 does not generate RESCPU and RESNPX. The default value of this bit is 0.
5	RSTREQ	Reset Request: Set whenever a software induced CPU Reset request is active. There are three possible causes of CPU Reset that are reflected in this bit. 1) Keyboard controller 2) Port A 3) VLSI Special Feature (VSF) The occurrence of any one of these events causes RSTREQ to go high. It remains high until the occurence of the CPU Reset event. The rising edge of RESCPU clears RSTREQ unconditionally. Default = 0.
4	HLTACT	Halt Active: Set when the VL82C316 decodes a halt condition from the CPU. This bit is reset when –RESET is active low, RESCPU is active high, rising edge of NMI, or on detection of an interrupt acknowledge cycle. Default = 0.
3, 2	REFMODE1, REFMODE0	Set Refresh Mode: These bits when set 01 enables CAS-before-RAS refresh. RAS-only refresh is selected if they are set to 00. A value of 10 selects CAS-before-RAS in Normal Operating Mode and self-refresh when the Suspend Mode is selected. For Static RAM-based systems, code 11 may be used to completely disable refresh while still leaving Timer 0 running. The default value for these bits is 00.
1, 0	REFSPD1, REFSPD0	Refresh Period: These bits determine the refresh period. If set to 01, they enable the Slow Refresh Mode in which a refresh cycle occurs every 125 µs. When set to 10, 250 µs refresh occurs. When 00, PC/AT Standard Mode is selected and the refresh period is 15.625 µs. This code is applicable to Normal, Sleep, and Suspend Modes Refresh. The default of these bits is 00. Code 11 is reserved.

ADDRESS MAPPER/DECODER

The VL82C316 offers several address mapping and decoding options for better system performance and flexibility. The available options include a slot pointer, ROM/EPROM shadowing, mapping of 384K memory to the top of the available physical memory, and PCMCIA IC Memory Card support.

SLOT POINTER (SLTPTR)

The slot pointer sets the 64K boundary between 256K and 16M above which CPU addresses are directed to the AT slot bus. Eight bits are required to specify this range (See Table 11). They are compared with the address lines A23-A16. Any system board memory from 1 MB up to SLTPTR is accessible as on-board extended memory. The slot bus DRAM extended memory resides from SLTPTR up to 16 MB in VL82C316.

SLTPTR can also be set below 1 MB. The minimum valid value for SLTPTR is 00h to facilitate the use of SRAM. The bank select signals internal to the device are disabled resulting in inactive –RAS and –CAS lines when SLTPTR is 00h. SLTPTR can not have values 01h, 02h, and 03h. For this reason, at least one bank of 256K RAM must be on the system board on reset for a physical memory size of 512 KB. The next valid value for SLTPTR is 04h to allow slot memory cards, especially EEMS capable boards, to backfill down to 256K. Any value between 04h and 09h makes the portion of system board DRAM from that address to A0000h inaccessible. The useable values for SLTPTR are 04h-FDh. A value of FEh or FFh results in no off-board accesses since CPU accesses in the FE0000h and FF0000h segments always result in ROM chip selects. Any out of range value is treated the same as FFh.

Table 12 and Figure 8 show the effects of the slot pointer.

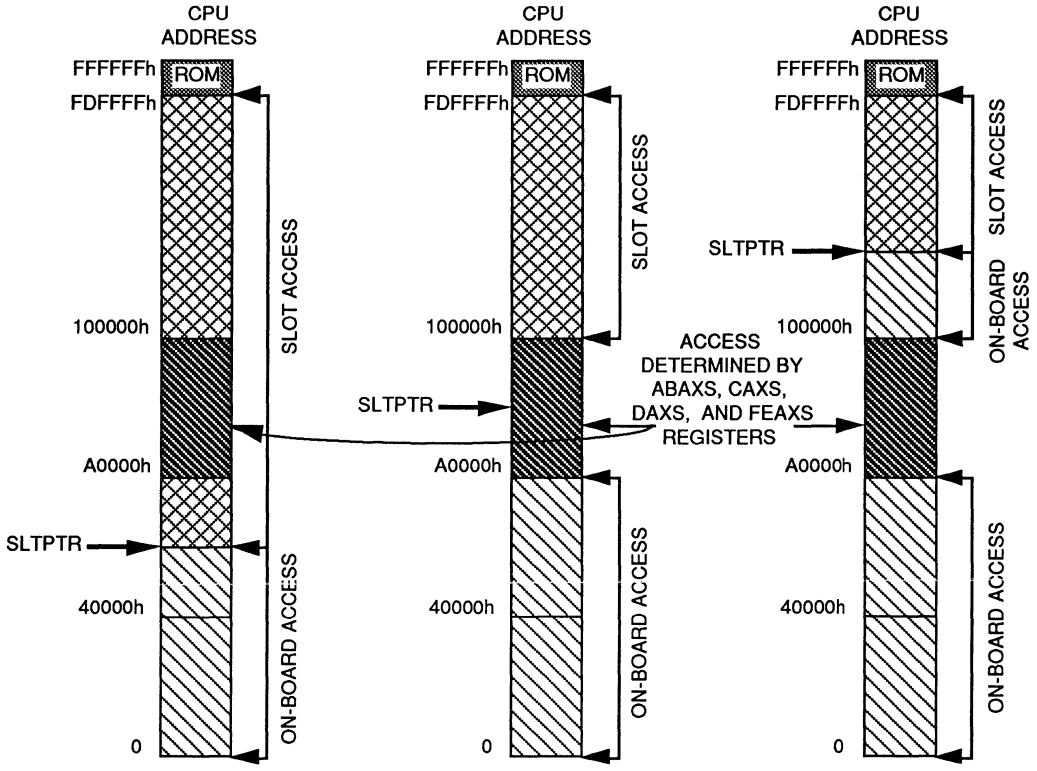
TABLE 11. SLTPTR CONFIGURATION REGISTER (READ/WRITE)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
SLTPTR (02h)	A23	A22	A21	A20	A19	A18	A17	A16
POR Value	1	1	1	1	1	1	1	1

TABLE 12. EFFECT OF SLOT POINTER

Slot Pointer Value	Slot Pointer Location	Effect
00h		No DRAM cycles initiated. This is to support the use of SRAM.
0004h-0009h	256K-640K	CPU addr 0h to SLTPTR = > system board access, CPU addr SLTPTR to 640K and 1M to 16M = > slot bus, CPU addr 640K to 1M = > determined by ABAXS, CAXS, DAXS, FEAXS Registers, CPU addr > 16M = > no accesses.
000Ah-000Fh	640K-1M	Respond as if SLTPTR = 0010h (see next case).
0010h-00FFh	1M-16M	CPU addr 0 to 640K = > system board accesses, CPU addr 640K to 1M = > determined by ABAXS, CAXS, DAXS, FEAXS Registers, CPU addr 1M to SLTPTR = > system board accesses. CPU addr SLTPTR to 16M = > if value 10h-FDh then slot bus else ROM. CPU addr > 16M = > no access.

FIGURE 8. EFFECT OF SLOT POINTER



REMAPPING OF MEMORY RANGE A0000H-FFFFFH

DOS utilizes 640K of memory from address locations 00000h to 9FFFFh. The memory range from A0000h to FFFFFh is used for video RAM, BIOS ROM, video BIOS, etc. If a system has more than 640K DRAM, the DRAM between A0000h and FFFFFh can be accessed directly by enabling read and/or write shadow RAM. This 384K of DRAM may be remapped to another memory range to also be utilized.

Remapping the memory range between A0000h and FFFFFh is performed via the REMP384 bit (bit 4) in the RAMMAP Register. The VL82C316 allows remapping of this memory only if the total system DRAM memory is 1M, 2M, 3M, or 4M. The 384K of memory is then remapped to the top of the system memory as shown Figure 9. Shadow RAM is unavailable in this mode.

RELOCATING SYSTEM AND SLOT ROM

A PC/AT motherboard normally includes 640K DRAM located in the address range 00000h to 9FFFFh, and 128K ROM residing from E0000h to FFFFFh. The memory accesses from A0000h to DFFFFh are directed towards the slots. The video buffers occupy memory space A0000h to BFFFFh while C0000h to DFFFFh is available for installable ROM (e.g. video ROM, fixed disk ROM). In a PC/AT, BIOS ROM is located from F0000h to FFFFFh. The ROM locations E0000h to EFFFFh are available for other purposes. The VL82C316 offers flexibility of having video ROM and fixed disk ROM either on the system board or on the slot bus.

The video ROM and the fixed disk ROM, memory range C0000h to CFFFFh, can be relocated to the on-board ROM range with the ROMMOV1 and ROMMOV0 bits (bits 6 and 5) in the RAMMAP Register. Similarly, the on-board memory range E0000h to EFFFFh can be moved to the slots by the same bits. This is done at power-on reset by configuring the ROMMOV bits with the pins MA8 and MA7. The two bits can also be controlled by software. Refer to Table 13.

Note: The DRAM mapping is not affected by these bits.

On-Board ROM Width and Location
System ROM can be located on either the local bus (D bus) or the slot bus (SD bus) via a jumper option on the –ROMCS/–PPICS pin sampled during power-up (refer to the section titled "System Configuration" for jumper configuration options). A second jumper on the MA10/–WE1 pin determines whether an 8- or 16-bit BIOS ROM is present in the system. If an 8-bit ROM is used, it must be placed on D15-D8 (if ROM is on the D bus) or SD7-SD0 (if ROM is on the SD bus). In either case, any access to on-board ROM means that the –ROMCS/–PPICS signal is generated.

Using Flash Memory for On-board ROM
Special programming considerations must occur if an 8-bit flash memory is used on the D bus. If an 8-bit flash device is located on D15-D8, the software must place the data onto the upper byte since the VL82C316 will not steer the data from low- to high-order bytes in this case. For even byte addresses, the data to be written should be on the high byte and a 16-bit even address write should be performed. Odd byte addresses are written by performing a byte write to the odd address. There is no similar restriction if the flash device is on the SD bus as the data steering inherent in ISA bus operation is in effect.

Flash memory requries the system to poll the flash memory following a write operation to detect that programming is complete. In order to accommodate this requirement, the VL82C316 does not perform the expected 16-to-8 bit conversion on ROM write cycles. In other words, a 16-bit ROM write to an 8-bit BIOS results in a single 16-bit access.

FIGURE 9. REMAPPING OF 384K DRAM

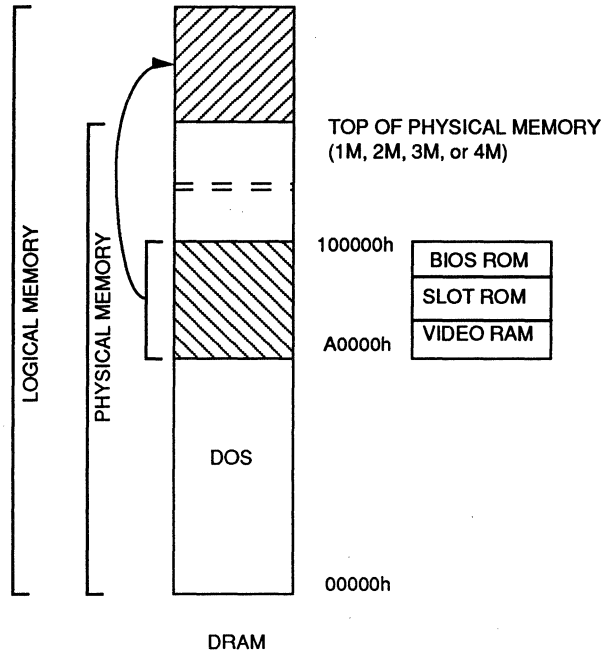


TABLE 13. RELOCATION OF SYSTEM AND SLOT ROM

ROMMOV1, ROMMOV0	00	01	10	11
E8000-EFFFFh	ROM	Slots	ROM	Slots
E0000-E7FFFh	ROM	Slots	Slots	Slots
C8000-CFFFFh (fixed disk ROM)	Slots	Slots	Slots	ROM
C0000-C7FFFh (video ROM)	Slots	Slots	ROM	ROM

SHADOWING

For better performance data from slow memory devices, like ROM, is copied into RAM to speed up memory accesses. This is called shadowing. The VL82C316 supports shadowing of the BIOS ROM and the installable slot ROM (also called adapter ROM). See Figure 10.

Four Indexed Configuration Registers are provided to give complete control over each of the 64K memory segments between A0000h and FFFFFh. The registers are called ABAXS, CAXS, DAXS, and FEAXS, see Table 14. Registers CAXS and DAXS contain two bits for each 16K segment in the memory address range C0000h and DFFFFh while ABAXS and FEAXS contain two bits for each 32K segment in the memory ranges A0000h-BFFFFh and E0000h-FFFFFh, respectively.

Shadowing can be enabled by writing a 1 and 0 in the two bits provided for each segment. Each segment can be enabled independent of the other segment. The ROM contents should be copied to the DRAM before shadowing is enabled. The two bits should be set to 0 and 1 for this purpose.

Shadowing is disabled when remapping of 384K memory (A0000h-FFFFFh) is selected.

FIGURE 10. SHADOW RAM CONTROL

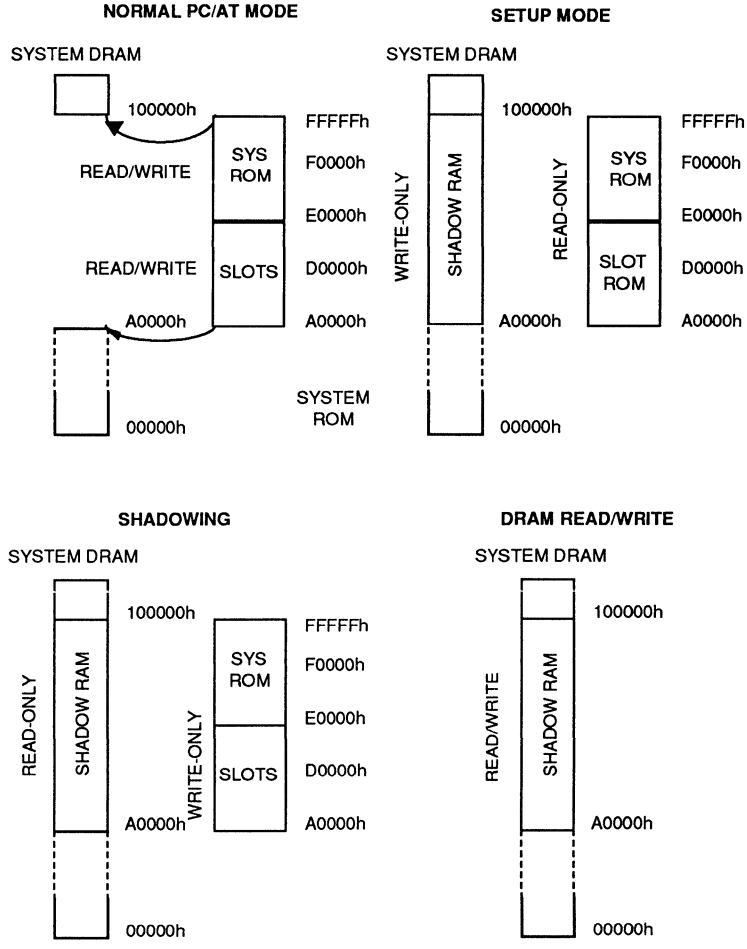


TABLE 14. SHADOWING CONFIGURATION REGISTERS (READ/WRITE)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
ABAXS (0Eh)	B8000 Access		B0000 Access		A8000 Access		A0000 Access	
CAXS (0Fh)	CC000 Access		C8000 Access		C4000 Access		C0000 Access	
DAXS (10h)	DC000 Access		D8000 Access		D4000 Access		D0000 Access	
FEAXS (11h)	F8000 Access		F0000 Access		E8000 Access		E0000 Access	
POR Values	0	0	0	0	0	0	0	0

The two bits for each segment select four modes as follows:

1. *00* *Read/Write Slot Bus (Default)*
   Normal PC/AT-compatible operation. This may be R/W slot bus or ROM chip select depending on the memory space.

2. *01* *Setup Mode: Read Slot Bus/ Write System Board*
   Shadow setup mode. In the E0000 and F0000 segments reads cause on-board ROM chip selects and writes to the same address are to system board DRAM. In the segments C0000 to D0000 reads are from the slot bus and writes are to system board DRAM. This allows shadowing of system board ROM as well as the ROMs on a slot card.

3. *10* *Read System Board/Write Slot Bus*
   Read-only DRAM. This is the normal shadow operational mode though it could be used to protect data previously written to a memory area while configured for Mode 2 (above). In this mode, writes are directed to the slot bus.

4. *11* *Read/Write System Board*
   R/W system board DRAM. This allows complete access to DRAM in the given 16K or 32K region.

PCMCIA 1.0 IC MEMORY CARD SUPPORT

The VL82C316 supports PCMCIA 1.0 IC Memory Card of up to 32 MB for use in laptop and notebook computers.

Note: This is not a complete interface. External logic is required.

The 32 MB of memory on the memory card can be divided into 2048 pages, each 16 KB long. There are four Mapping Registers provided in the VL82C316 to map four of these pages to the CPU address space between A0000h and FFFFFh. These four registers hold pointers to the IC memory card space. There are four more Mapping Registers provided which contain pointers to the CPU address space as shown in Figure 11.

There is a correlation existing between the Mapping Registers for IC memory card and those for the CPU address space. When the CPU accesses a 16K page pointed to by one of the CPU Address Mapping Registers, the CPU address is translated to access the 16K page pointed to by the associated IC Memory Mapping Register.

The Mapping Registers are accessed via the Index Register at I/O address E8h. The lower six bits of this register are used to access one of the eight Mapping Registers. The Mapping Registers for CPU address space are accessed if the Index Register data is 30h, 32h, 34h, or 36h, while the Mapping Registers for IC memory card are selected if the lower six bits are 31h, 33h, 35h, or 37h.

The port addresses EAh and EBh are used for byte accesses to the Mapping Registers. The instructions for writing a byte to the Page 0 Mapping Register for IC memory card are:

```
MOV   AL,31    ; Page 0 Mapping
                 Register for
                 memory card
OUT   E8,AL
MOV   AL,data  ;
OUT   EA,AL    ; Write low byte
or
OUT   EB,AL    ; Write high byte
```

The Mapping Registers are word accessible at port address EAh. The Mapping Registers for CPU address space return FFh in the upper byte when a word read is performed.

TABLE 15. PCMCIA 1.0 IC MEMORY CARD INDEX REGISTER AND DATA PORT MAP

E8h Index Port	D7	D6	D5	D4	D3	D2	D1	D0
			A5	A4	A3	A2	A1	A0

Index Port (E8h)	Page Segment	Data Port (EBh) D15	D14	D13	D12	D11	D10	D9	D8	Data Port (EAh) D7	D6	D5	D4	D3	D2	D1	D0
30	0	1	1	1	1	1	1	1	1	1	1	SA19	SA18	SA17	SA16	SA15	SA14
31	0	1	1	1	1	1	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
32	1	1	1	1	1	1	1	1	1	1	1	SA19	SA18	SA17	SA16	SA15	SA14
33	1	1	1	1	1	1	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
34	2	1	1	1	1	1	1	1	1	1	1	SA19	SA18	SA17	SA16	SA15	SA14
35	2	1	1	1	1	1	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
36	3	1	1	1	1	1	1	1	1	1	1	SA19	SA18	SA17	SA16	SA15	SA14
37	3	1	1	1	1	1	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0

The lower six bits of port EAh allow access to SA19-SA14 during CPU memory cycles. The memory address lines (MA10-MA0) are accessed by the lower three bits of port EBh and all eight bits of port EAh. The MA10-MA0 pins are connected to the address lines 24-14 of the IC memory card allowing access to 32 MB memory.

The four pages can be independently enabled using the Configuration Register MCDCTL. The MCDCTL Register has four bits available, one for each page.

It should be noted that the auto-increment feature is not available in this mode. Also, when an invalid memory access is made for a disabled page, zeros are driven out on the address lines used for IC memory card support.

The IC memory card pages share the same CPU address space with shadowed memory. The IC memory card pages having the lowest priority makes it imperative for the software to ensure that shadowing is not enabled in the CPU address space where an IC memory card page is assigned.

FIGURE 11. MEMORY MAPPING FOR PCMCIA 1.0 MEMORY CARD

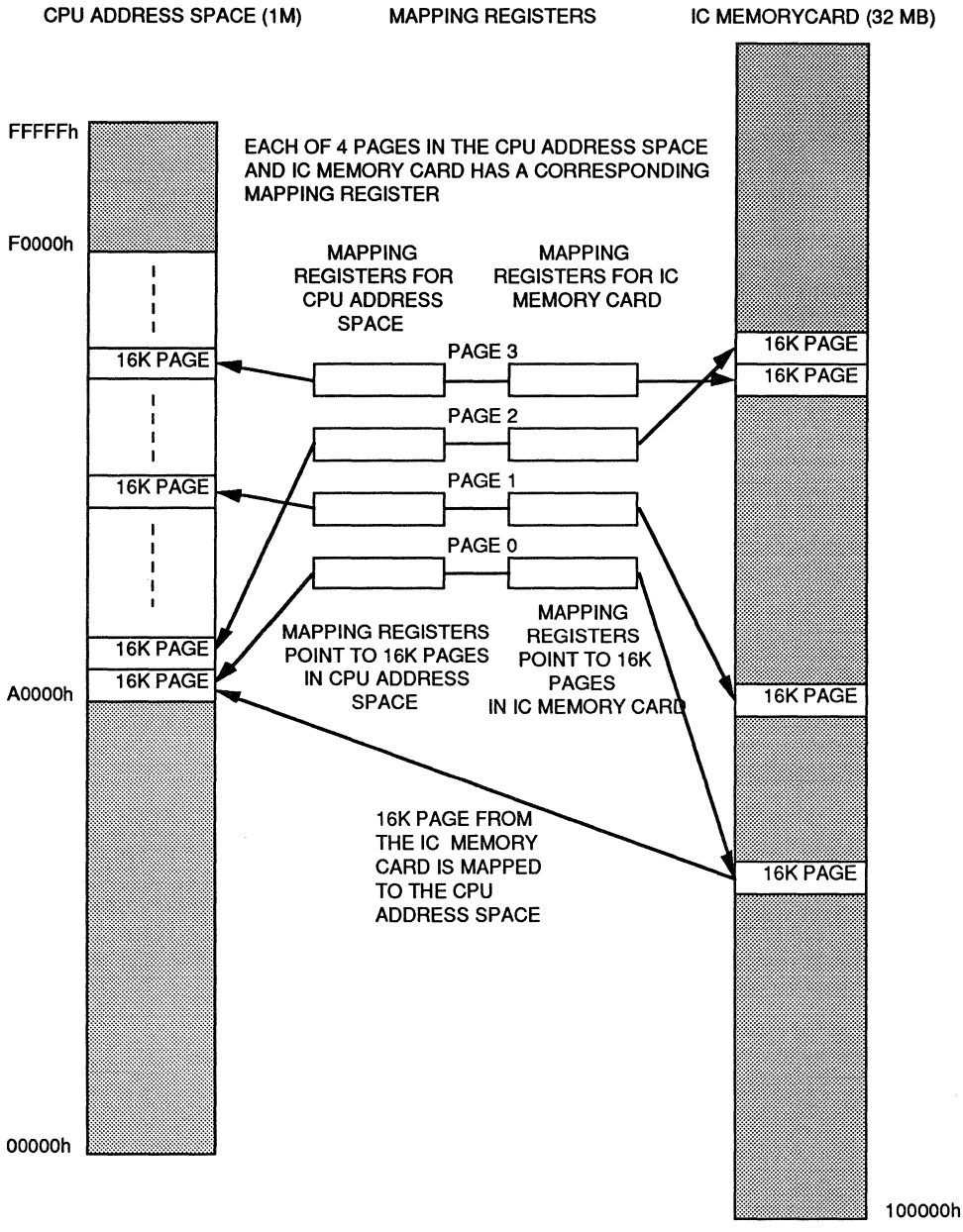


TABLE 16. MCDCTL CONFIGURATION REGISTER (READ/WRITE)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
MCDCTL (0Ah)	–ENMCSPD	R	R	R	MCPGEN3	MCPGEN2	MCPGEN1	MCPGEN0
POR Value	1	X	X	X	0	0	0	0

Bit	Name	Function
7	–ENMCSPD	Enable Memory Card Space Decode: When 0, accesses to the memory card space as internally decoded and based on the values programmed into registers 30h-37h in the E8h index port I/O space, result in use of the fast BUSCLK divider as configured in the CLKCTL Register. The bit is totally independent of the ENVDSPD bit of the CLKCTL Register. It is possible to enable speed-up to either, neither, or both of these areas simultaneously. Default value is 1, speed-up disabled.
6-4	R	Reserved: These bits are currently undefined. For compatibility with future versions of this product, this register should always be written such that the value of these bits are not altered.
3-0	MCPGEN3-MCPGEN0	Memory Card Page Enable: These bits are used to enable the Mapping Registers for the CPU address space and IC memory card. Each bit controls a pair of Mapping Registers associated with one page. The bits, when high, enable the Mapping Registers and allow access to four 16 KB pages. MCPGEN0 enables the Mapping Registers at address 30h and 31h, MCPGEN1 controls those at 32h and 33h, MCPGEN2 allows access to 34h and 35h, while the registers at 36h and 37h are controlled by MCPGEN3. At power-on all four bits are disabled.

Memory Card Control Register
The Memory Card Control Register, MCDCTL, is available for enabling the Mapping Registers. Four bits of this register control a pair of Mapping Registers associated with a page. A pair of Mapping Registers consists of one for the CPU address space and one for the IC memory card. See Table 16 for the MCDCTL Register format.

DIRECT MEMORY ACCESS (DMA)

The DMA controllers are 82C37A compatible, have internal latches provided for latching the middle address bits output by the 82C37A megacells on the data bus, and have 74LS612 memory mappers provided to generate the upper address bits.

The DMA logic controls transfers between an I/O channel and on- or off-board memory. It generates a hold request to the CPU when an I/O channel requests a DMA operation. Once the hold has been acknowledged, the DMA controller drives the CPU address bus and the slot address bus. DMAs can occur over the full 16 MB range available.

The seven DMA acknowledge signals are encoded within the VL82C316 to generate external signals DK2-DK0. They must be decoded externally using a 3-to-8 demultiplexer (74HC138). An enable signal, DKEN, is generated by VL82C316 for use by the demultiplexer.

DMA CONTROLLER REGISTERS
The 82C37A megacells can be programmed any time HLDA is inactive, i.e., when DMA controllers are not in operation. Table 17 lists the addresses of all registers which can be read or written in the 82C37A megacells. In Table 17 addresses under the column DMA2 are for the 16-bit DMA channels and DMA1 corresponds to the 8-bit channels. When writing to a channel's Address or Word Count Register, the data is written into both the base register and current register simultaneously. When reading a Channel Address or Word Count Register only the current address or word count can be read. The base address and base word count are not accessible for reading.

The Address and Word Count Registers for each channel are 16-bit registers. The value on the data bus is written into the upper byte or lower byte depending on the state of the internal addressing flip-flop. This flip-flop can be cleared by the "clear byte pointer flip-flop" command. After this command, the first read/write to an Address or Word Count Register will read/write to the low byte of the 16-bit register and the byte pointer flip-flop will toggle to a one. The next read/write to an Address or Word Count Register will read/write to the high byte of the 16-bit register and the byte pointer flip-flop will toggle back to a zero. Refer to the 82C37A data sheet for more information on programming the 82C37A megacell.

The 82C37A DMA controller megacells allow the user to program the active level (low or high) of the DREQ and DACK signals. Since the two megacells are cascaded together internally on the chip, these signals should always be programmed with the DREQ signals active high and the DACK signals active low.

When programming the 16-bit channels (channels 5, 6, and 7) the address which is written to the base Address Register must be the real address divided by two. Also, the base word

count for the 16-bit channels is the number of 16-bit words to be transferred, not the number of bytes as is the case for the 8-bit channels.

It is recommended that all internal locations, especially the Mode Registers, in the 82C37A megacells be loaded with some valid value. This should be done even if the channels are not used.

MIDDLE ADDRESS BIT LATCHES

The middle DMA address bits are held in an internal 8-bit register. The DMA controller will drive the value to be loaded onto the internal data bus and then issue an address strobe signal to latch the data bus value into this register. An address strobe is issued at the beginning of a DMA cycle and any time the lower 8-bit address increments across the 8-bit subpage boundary during block transfers. This register cannot be written to or read externally. It is loaded only from the address strobe signals from the megacells and the outputs go only to the A16-A8 pins.

PAGE REGISTERS

A 74LS612 cell is used in the VL82C316 to generate the Page Registers for each DMA channel. The Page Registers provide the upper address bits during a DMA cycle. DMA addresses do not increment or decrement across page boundaries. Page boundaries for the 8-bit channels (channels 0 through 3) are every 64 KB and page boundaries for the 16-bit channels (channels 5, 6, and 7) are every 128 KB. There are a total of 16 8-bit registers in the 612 megacell.

These registers must be written to select the correct page for each DMA channel before any DMA operations are performed. The other address locations between 80h and 8Fh not shown in the table below are not used by the DMA channels but can be read or written to by the CPU.

A23-A16	DMA Channel
87h	0
83h	1
81h	2
82h	3
8Bh	5
89h	6
8Ah	7
8Fh	Refresh

ADDRESS GENERATION

The DMA addresses are setup such that there is an upper address portion used to select a specific page, a middle address portion used to select a block within the page, and a lower address portion.

The upper address portion is generated by the Page Registers in the 74LS612 equivalent megacell. The Page Registers for each channel must be setup by the CPU before a DMA operation. DMA addresses do not increment or decrement across page boundaries. Page sizes are 64 KB for 8-bit channels (channels 0 through 3) and 128 KB for 16-bit channels (channels 5, 6, and 7). The DMA Page Register values are output on A23-A16 for the 8-bit channels and A23-A17 for the 16-bit channels.

The middle address portion, used to select a block within the page, is generated by the 82C37A megacells at the beginning of a DMA operation and any time the DMA address increments or decrements through a block boundary. Block sizes are 256 bytes for the 8-bit channels (channels 0 through 3) and 512 bytes for the 16-bit channels (channels 5, 6, and 7). This middle address portion is output by the 82C37A megacells onto the internal data bus during state S1. The internal middle address bit latches will latch this value in. The middle address bit latches are output on A15-A8 for the 8-bit channels and A16-A9 for the 16-bit channels.

The lower address portion is generated directly by the 82C37A megacells during DMA operations. The lower address bits are output on A7-A0 for 8-bit channels and A8-A1 for 16-bit channels. A0 and –SBHE are forced low during 16-bit DMA operations. –SBHE is forced to the opposite value of A0 for 8-bit DMA.

–SBHE is configured as an output during all DMA operations and will be driven as the inversion of A0 during 8-bit DMA cycles and forced low for all 16-bit DMA cycles.

Table 18 shows the mapping from the DMA subsystem signals to slot bus signals. Table 19 shows the mapping of the DMA subsystem signals to local address bus signals.

TABLE 17. DMA CONTROLLER REGISTERS

Hex Address		
DMA2	DMA1	Register Function
0C0	000	Ch 0 Base and Current Address Register
0C2	001	Ch 0 Base and Current Word Count Register
0C4	002	Ch 1 Base and Current Address Register
0C6	003	Ch 1 Base and Current Word Count Register
0C8	004	Ch 2 Base and Current Address Register
0CA	005	Ch 2 Base and Current Word Count Register
0CC	006	Ch 3 Base and Current Address Register
0CE	007	Ch 3 Base and Current Word Count Register
0D0	008	Read Status Register/ Write Command Register
0D2	009	Write Request Register
0D4	00A	Write Single Mask Register Bit
0D6	00B	Write Mode Register
0D8	00C	Clear Byte Pointer Flip-Flop
0DA	00D	Read Temp Register/ Write Master Clear
0DC	00E	Clear Mask Register
0DE	00F	Write All Mask Register Bits

TABLE 18. DMA ADDRESSING FOR SLOT BUS ACCESSES

Outputs from 74LS612 Page Registers	Outputs from Middle Address Latches	Address Outputs from 82C37	8-Bit DMA Address Bits	16-Bit DMA Address Bits
M9				
M8				
M7			LA23	LA23
M6			LA22	LA22
M5			LA21	LA21
M4			S/LA20	S/LA20
M3			S/LA19	S/LA19
M2			S/LA18	S/LA18
M1			S/LA17	S/LA17
M0			SA16	
	D7		SA15	SA16
	D6		SA14	SA15
	D5		SA13	SA14
	D4		SA12	SA13
	D3		SA11	SA12
	D2		SA10	SA11
	D1		SA9	SA10
	D0		SA8	SA9
		A7	SA7	SA8
		A6	SA6	SA7
		A5	SA5	SA6
		A4	SA4	SA5
		A3	SA3	SA4
		A2	SA2	SA3
		A1	SA1	SA2
		A0	SA0	SA1
		VSS		SA0
		–A0	–SBHE	
		VSS		–SBHE

TABLE 19. DMA ADDRESSING FOR SYSTEM BOARD MEMORY

Outputs from 74LS612 Page Registers	Outputs from Middle Address Latches	Address Outputs from 82C37	8-Bit DMA Address Bits	16-Bit DMA Address Bits
M9				
M8				
M7			A23	A23
M6			A22	A22
M5			A21	A21
M4			A20	A20
M3			A19	A19
M2			A18	A18
M1			A17	A17
M0			A16	
	D7		A15	A16
	D6		A14	A15
	D5		A13	A14
	D4		A12	A13
	D3		A11	A12
	D2		A10	A11
	D1		A9	A10
	D0		A8	A9
		A7	A7	A8
		A6	A6	A7
		A5	A5	A6
		A4	A4	A5
		A3	A3	A4
		A2	A2	A3
		A1	A1	A2
		A0	–BLE	A1
		VSS		–BLE
		–A0	–BHE	
		VSS		–BHE

TABLE 20. ROMDMA CONFIGURATION REGISTER (READ/WRITE)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
ROMDMA (15h)	ROMWS1	ROMWS0	DRAMWS8 (1 & 0)		DRAMWS16 (1 & 0)		DMACLK	MEMTM
POR Value	PAR1	PAR0	1	0	1	0	0	0

Bit	Name	Function
7, 6	ROMWS1, ROMWS0	ROM Wait States: Bits 7 and 6 indicate the number of ROM wait states. These wait states are timed in slot bus cycles. The valid range is 1-3: **Bit 7** **Bit 6** **# of WS** 0 0 3 0 1 1 1 0 2 1 1 3 The initial power-on reset value of ROMWS1 is set the same as PAR1 and of ROMWS0 is set the same as PAR0 at the end of the reset period.
5, 4	DMAWS8(1) DMAWSA(0)	8-Bit DMA Wait States: Bits 5 and 4 specify the number of clocks the command is active for 8-bit DMA cycles: **Bit 5** **Bit 4** **DMA Clocks** 0 0 2 0 1 4 1 0 3 1 1 3
3, 2	DMAWS16(1) DMAWS16(0)	16-Bit DMA Wait States: Bits 3 and 2 specify the number of clocks the command is active for 16-bit DMA cycles: **Bit 3** **Bit 2** **DMA Clocks** 0 0 2 0 1 4 1 0 3 1 1 3
1	DMACLK	DMA Clock: When set, this bit selects SYSCLK as an input clock for the DMA. When 0, the input clock to the DMA is SYSCLK/2. At power-on, SYSCLK/2 is selected as DMA clock.
0	MEMTM	–MEMR Signal Delay: This specifies the delay for the –MEMR signal. When 0, –MEMR is active at the same time as in the original PC/AT design. This is the default case. When 1, falling edge of –MEMR occurs one DMACLK earlier. In this latter case, the –MEMR timing during a memory to I/O DMA cycle is the same as that of the –XIOR signal during an I/O to memory DMA cycle.

ROMDMA REGISTER

The ROMDMA Indexed Configuration Register is used to program the extended DMA features. Table 20 gives the ROMDMA Register format.

DMA POWER MANAGEMENT OPTION

Bit 6 (DMAPWR) of the BUSCTL2 Configuration Register controls automatic DMA clock management. Control is independent for each DMA controller. This feature is activated when DMAPWR is reset to 0. (The default is disabled.) In this mode, when any of the DRQs to an individual DMA controller are active, the DMA clock to that controller is enabled. The clock remains active until all DRQs and –DACKs to that DMA controller are inactive. At that time the clock is shut off. The DMA controller's internal registers may be read or written when the clocks are stopped.

CLOCK GENERATOR

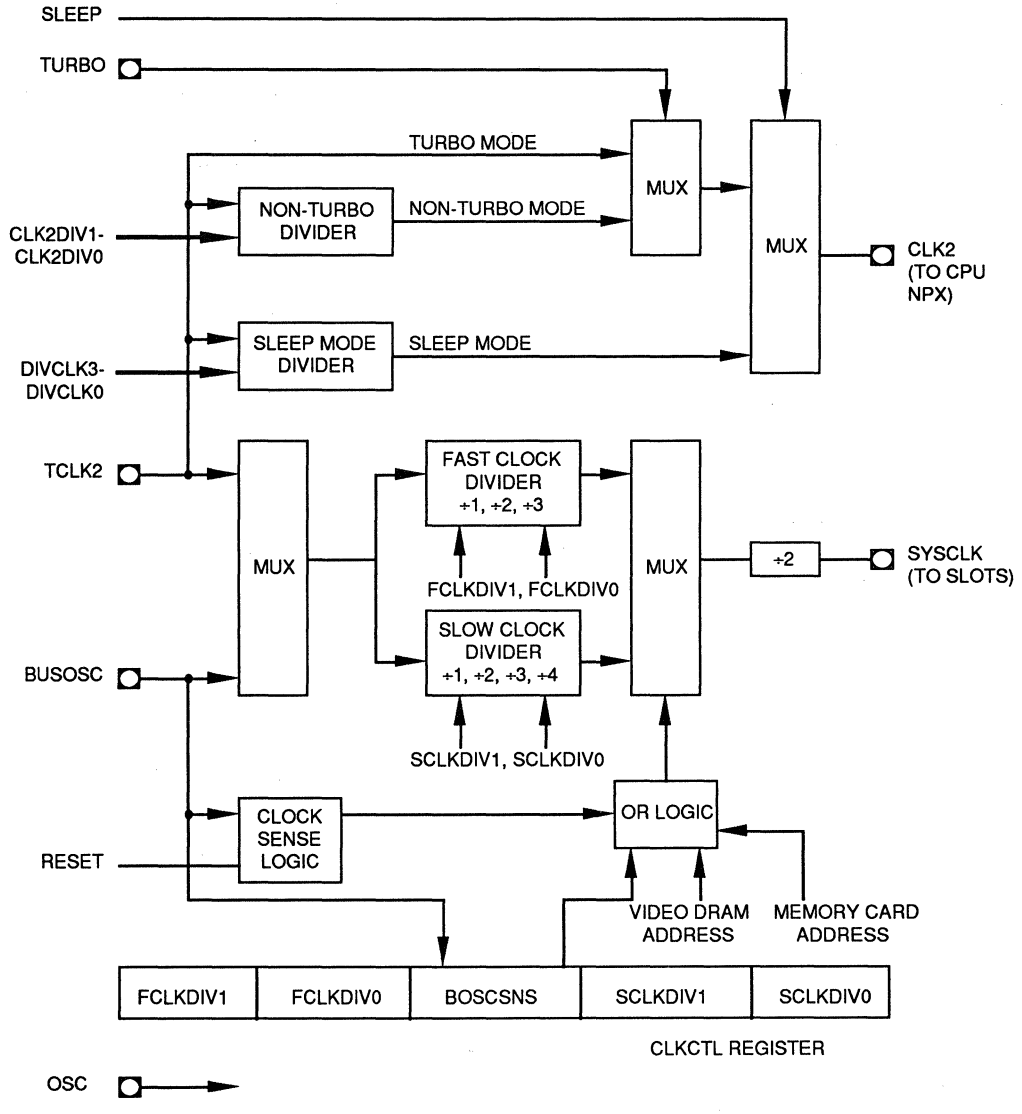
The clock generator logic generates programmable frequency clock signals. The VL82C316 has a unique expanded clock feature by which the clock is automatically increased when the video DRAM address range, A0000h to BFFFFh, is accessed. The logic diagram of the clock generator is shown in Figure 12.

The external input pins related to the clock generation are TCLK2, OSC, and BUSOSC. The output pins are CLK2 and SYSCLK.

CLOCK SIGNALS

The VL82C316 supports systems with operating frequencies up to 33 MHz. The processor clock (CLK2) is connected to the CPU, the coprocessor, and other on-board logic for synchronization. It is derived from the TCLK2 input signal which is connected to a crystal oscillator with a of frequency twice the operating frequency. The frequency of CLK2 is programmable. The CLK2DIV1 and CLK2DIV0 bits in the Clock Control Register (CLKCTL) select CLK2 to be TCLK2, TCLK2 ÷2, ÷3, or ÷4.

FIGURE 12. CLOCK GENERATOR LOGIC



OSC is the buffered input of the external 14.318 MHz oscillator. The bus clock, BUSOSC, is supplied from an external oscillator and is used for asynchronous AT bus operations.

The system clock output, SYSCLK, is a programmable clock. It is generated from either TCLK2 or BUSOSC as explained in the section titled "Programmable AT Bus Clock." The bus control outputs BALE, –IOR, –IOW, –MEMR, and –MEMW are synchronized to SYSCLK.

PROGRAMMABLE AT BUS CLOCK

The VL82C316 provides a special feature of programming the AT bus clock, SYSCLK, for optimum performance. The synchronous SYSCLK frequency can be varied from 5 to 16 MHz using the BUSOSC pin and CLKCTL Register. Thus, different SYSCLK frequencies can be used for different peripheral accesses. The logic diagram of the circuit that generates SYSCLK is shown in Figure 12.

The BUSOSC pin is sensed by the clock sense logic at power-on reset. If there is no external oscillator connected to BUSOSC, it can be used to select the frequency of SYSCLK. At power-on reset, the values of pins DKEN and –RAMW/–WE0 are latched into the SCLKDIV1 and SCLKDIV0 bits (bits 1 and 0) in the CLKCTL Register. TCLK2 is divided by a factor of 2, 4, 6, or 8 depending on the values of the SCLKDIV bits to generate SYSCLK. Refer to Table 21.

The frequency of SYSCLK for faster operation is programmable using the FCLKDIV1 and FCLKDIV0 bits (bits 4 and 3) in the CLKCTL Register. TCLK2 is divided by 2, 4, or 6. When there is no external oscillator connected to BUSOSC, it can be toggled to switch between the two dividers. When reset 0, the slow clock divider is active. If BUSOSC is held high, the fast clock divider is used for generating SYSCLK. The switching between the two dividers also occurs automatically in the VL82C316 when the ENVDSP bit (bit 7) in the CLKCTL Register is enabled and the video DRAM address space (A0000h to BFFFFh) is accessed.

The BOSCSNS bit (bit 2) in the CLKCTL Register reflects the status of BUSOSC pin and is read-only bit when there is no oscillator connected to the BUSOSC pin. If BUSOSC does have an oscillator connected, SYSCLK is derived from TCLK2 instead of BUSOSC. The frequency of SYSCLK can then be varied by using the BOSCSNS bit which now is a read/write bit. At power-on reset, the Slow Clock Divider is enabled, dividing BUSOSC by a factor dependent on the value of the SCLKDIV bits. These two bits (SCLKDIV1 and SCLKDIV0) are configured at power-on by the DKEN and –RAMW/–WE0 pins, respectively. The Fast Clock Divider is activated if the BOSCSNS bit is set to 1, or a valid video DRAM address space is accessed with the ENVDSP bit enabled, or a valid memory card address space is accessed with the –ENMCSPD bit enabled. The division factor is determined by the values of the FCLKDIV bits.

TABLE 21. AT BUS CLOCK FREQUENCIES

BUSOSC	BOSCSNS/ Video DRAM	FCLKDIV1, FCLKDIV0	SCLKDIV1, SCLKDIV0	SYSCLK
BUSOSC	0	XX	00	BUSOSC ÷2
	0	XX	01	BUSOSC ÷4
	0	XX	10	BUSOSC ÷6
	0	XX	11	BUSOSC ÷8
	1	00	XX	BUSOSC ÷2
	1	01	XX	BUSOSC ÷4
	1	10	XX	BUSOSC ÷6
	1	11	XX	
0	0	XX	00	TCLK2 ÷2
0	0	XX	01	TCLK2 ÷4
0	0	XX	10	TCLK2 ÷6
0	0	XX	11	TCLK2 ÷8
1	1	00	XX	TCLK2 ÷2
1	1	01	XX	TCLK2 ÷4
1	1	10	XX	TCLK2 ÷6
1	1	11	XX	

CLOCK CONTROL REGISTER (CLKCTL)
The CLKCTL Register is used for determining SYSCLK frequency (as described in the section titled "Programmable AT Bus Clock"), setting CLK2 frequency, and enabling SYSCLK frequency switching in the video DRAM address range. Table 22 gives the CLKCTL Register format.

TABLE 22. CLKCTL CONFIGURATION REGISTER (READ/WRITE)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
CLKCTL (07h)	ENVDSP	CLK2DIV1	CLK2DIV0	FCLKDIV1	FCLKDIV0	BOSCSNS	SCLKDIV1	SCLKDIV0
POR Value	0	0	0	1	0	See Descrip.	DKEN	–RAMW/ –WE0

Bit	Name	Function
7	ENVDSP	Enable SYSCLK Frequency Switching in Video DRAM Address Range: This bit selects a different SYSCLK frequency when a memory access is made in the the video DRAM address range of A000h-BFFFFh. When set to 0, ENVDSP disables the automatic frequency change in SYSCLK and enables that feature if set to 1. The default value of this bit is 0.
6, 5	CLK2DIV1, CLK2DIV0	CLK2 Divider in Non-Turbo Mode: These bits specify the CLK2 divider value to be used when the TURBO pin is low or when a write to port F4h is performed. **Bit 6 / Bit 5 / CLK2** 0 / 0 / TCLK2 ÷ 1 0 / 1 / TCLK2 ÷ 2 1 / 0 / TCLK2÷ 3 1 / 1 / TCLK2 ÷ 4 The power-on reset default value of these bits is 00, selecting TCLK2 as the frequency of CLK2.
4, 3	FCLKDIV1, FCLKDIV0	Fast Clock Divider: These bits determine the frequency of SYSCLK when an access is made to the video DRAM address space with ENVDSP of this register set to 1, or when BOSCNS bit is 1. **Bit 4 / Bit 3 / SYSCLK** 0 / 0 / CLOCK ÷ 1 0 / 1 / CLOCK ÷ 2 1 / 0 / CLOCK ÷ 3 1 / 1 / Reserved CLOCK is BUSOSC if an asynchronous bus clock or TCLK2 if synchronous. The default value of these bits is 10.
2	BOSCSNS	BUSOSC Status: This bit reflects the state of the BUSOSC pin when there is no external oscillator connected to it. In this case, BOSCSNS is a read-only bit. If an oscillator is connected to the BUSOSC pin, BOSCSNS becomes a read/write bit selecting SYSCLK frequency (as explained in the section "Programmable AT Bus Clock"). The power-on reset default value of BOSCSNS is 0 if an external oscillator is present. If not, it is the status of the BUSOSC pin.
1, 0	SCLKDIV1 SCLKDIV0	Slow Clock Divider: These bits are used for selecting the frequency of SYSCLK and when BOSCSNS bit is 0. **Bit 1 / Bit 0 / SYSCLK** 0 / 0 / CLOCK ÷ 2 0 / 1 / CLOCK ÷ 4 1 / 0 / CLOCK ÷ 6 1 / 1 / CLOCK ÷ 8 CLOCK is BUSOSC if connected externally or TCLK2 if not. The default values are determined by the status of pins DKEN and –RAMW at power-on reset.

CLOCK CONTROL ENHANCEMENTS

The VL82C316's architecture expands on the capabilities of the original VL82C310 SCAMP I Controller's clock control. In addition to controlling video cycle speed-up, the VL82C316 also provides for the option of PCMCIA IC memory card cycle speed-up. Both speed-up address spaces can be individually enabled or disabled for standard ISA bus timed cycles. However, they use the same clock divider as programmed using the BUSOSC pin and CLKCTL Register. If standard ISA bus cycles are programmed for 8 MHz accesses and fast cycles are programmed for 16 MHz cycles, both areas, if enabled, will result in 16 MHz cycles.

Refer to Table 16 for the MCDCTL Register format. If the memory card option is not used, the speed-up feature is still accessible. Each of the four memory card bits may be programmed with a memory space range for which speed-up is desired. This might be used to speed-up accesses when third party PCMCIA 2.0 chips are incorporated, for example.

POWER MANAGEMENT MODE CONTROL LOGIC

Sleep Mode operation is provided for battery operated microcomputer support. The REFCTL, SLPCTL, and MISCSET Indexed Configuration Registers are provided to control this function. Operation of the Suspend Mode is provided if use of the VL82C316 is desired to provide on-board refresh. Since the VL82C316 is powered when used in this mode, other power savings features are also activated. Use of this feature is optional when the VL82C323 Power Management Unit (PMU) is used with the VL82C316 since the VL82C323 provides a Suspend Mode refresh. However, for designers who may already have developed alternate Power Management Subsystems (based on a CMOS microcontroller, for example) that do not support the Suspend Mode refresh, the Suspend Mode refresh capability may be required.

SLEEP MODE OPERATION

The Sleep Mode can be activated by software as well as by hardware. The external –SLEEP pin is used to enable the Sleep Mode by hardware. A 1-to-0 transition on this pin puts the VL82C316 into the Sleep Mode when set for –SLEEP input mode. Activation of the Sleep Mode via software is accomplished by setting the SLP bit (bit 7) in the SLPCTL Register high.

When the VL82C316 is in the Sleep Mode, the CLK2 divider and refresh dividers are activated and BUSOSC is shut-off from non-essential internal circuitry. The clocks going to the interrupt controllers and refresh logic are not shut-off. The DMA clock is independently controllable. Refer to the section titled "BUSCTL Register" for further information.

For maximum power savings, it is recommended that a "Halt" instruction be executed immediately after setting the SLP bit. Power saving can also be accomplished by operating the CPU at the minimum allowable frequency. There are four bits (DIVCLK3-DIVCLK0) available in the SLPCTL Register to select the clock frequency for the CPU. It should be noted that the Turbo or Non-Turbo Mode of operation has no effect on this frequency when the Sleep Mode is activated.

The VL82C316 can be brought out of the Sleep Mode in one of four ways:

1) Clearing of the SLP bit in the SLPCTL Register to 0 by software.
2) Driving a 0-to-1 input on the –SLEEP pin with the SLP bit set to 0.
3) Interrupting the device. (IRQs not NMI or SMI.)
4) Resetting the device.

Normal BUSOSC routing and clock speed are resumed when the VL82C316 exits the Sleep Mode.

The Sleep Mode is suspended during refresh, DMA, or Master Mode cycles by automatically deactivating the sleep clock divider in response to the hold request. Upon completion of the cycle, the system re-enters the Sleep Mode unless the SLP bit has been cleared.

The exception to this is if the VL82C316 is programmed for Static Sleep Mode Operation (CLK2OFF, BUSCTL2, bit 7 = 0). In this case, the VL82C316 waits for the end of a hold acknowledge cycle before entering Sleep Mode and stopping the CPU clock. DMA, refresh and master cycles can occur without restarting the CPU clock since the logic operates from the fixed 14.518 MHz clock (OSC).

During the Static Sleep Mode, leakage control is enabled to prevent floating lines. This leakage control is active as long as the VL82C316 remains in the Static Sleep Mode and idle (e.g., no DMA, refresh, or master cycle activity).

Sleep Mode Configuration Register (SLPCTL)

The SLPCTL Register controls the functionality of the Sleep Mode. Bits 0, 1, and 4-6 should be set with the desired values by the BIOS during POST. Only bit 7 needs to be toggled to get in and out of the Sleep Mode during operation. Table 23 gives the format of the SLPCTL Register.

TABLE 23. SLPCTL CONFIGURATION REGISTER (READ/WRITE)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
SLPCTL (13h)	SLP	DIVCLK3	DIVCLK2	DIVCLK1	DIVCLK0	SLPSTS	R	ENSYSCK
POR Value	0	0	0	0	0	–SLEEP	X	1

Bit	Name	Function
7	SLP	Sleep Mode: This bit is set to 1 to invoke the Sleep Mode function via software. When set, CLK2 is divided by the value coded in bits 6-4 of this register. Default = Sleep Mode disabled.
6-3	DIVCLK3-DIVCLK0	Power-Down TCLK2 Divider: These bits provide a code used to divide the TCLK2 down for the Sleep Mode. Division from 1-1024 is programmable as specified below. (See the section titled "BUSCTL Register" for activation of the stop clock option.) **Bit 6 / Bit 5 / Bit 4 / Bit 3 / Clock** 0 0 0 0 ÷1 (Default) 0 0 0 1 ÷4 0 0 1 0 ÷8 0 0 1 1 ÷12 0 1 0 0 ÷16 0 1 0 1 ÷64 0 1 1 0 ÷128 0 1 1 1 ÷256 1 0 0 0 ÷1024 All the other combinations not mentioned here are reserved.
2	SLPSTS	–SLEEP Pin Status: This bit reflects the status of the –SLEEP pin. It is used by the software to check whether –SLEEP is active or not. The VL82C316 enters the Sleep Mode when –SLEEP is pulled low. If an interrupt occurs, the device comes out of the Sleep Mode but the pin still might be pulled low. The interrupt service routine can check this bit and activate the Sleep Mode by enabling the SLP bit (bit 7 of this register).
1	R	Reserved: This bit is currently undefined. For compatibility with future versions of this product, this register should always be written such that the value of this bit is not altered.
0	ENSYSCK	System Clock Enable: Resetting this bit to 0 disables the SYSCLK oscillator (BUSCLK ÷2) if bit 7 (SLP) is set to 1. Returning bit 7 to 0 re-enables the oscillator signal. If bit 0 is 1, the oscillator is always enabled even in the Sleep Mode. In operation, bit 0 is set for the desired operational mode by the BIOS on power-up. Bit 7 is then controlled as required to jump in and out of the Sleep Mode during operation. Default = SYSCLK enabled.

SUSPEND MODE OPERATION

The VL82C316 supports an additional low-power mode defined as "Suspend". The basic assumption of the Suspend Mode is that the on-board DRAM refresh and video DRAM are active. Power is shutdown to non-essential components or put into a Static Mode. The following activities occur when the VL82C316 is in the Suspend Mode:

- All clocks are synchronously stopped except for the 32 kHz oscillator. CLK2 and SYSCLK are forced low.
- DRAM continues to be refreshed by using the 32 kHz ocsillator in either the CAS-before-RAS or Self-Refresh Mode depending on the state of the REFCTL (Refresh Control) Register.
- Control signal inputs, such as –IOR or –IOW, etc., are gated inactive internal to the VL82C316 so that inadvertent register corruption is prevented.
- Leakage control is enabled so that minimum power dissipation occurs in the Suspend Mode (refer to the "Pin Type by Operational State" table on starting on page 6 for further details).
- The local bus (CPU) interface may remain powered or may be powered off in the Suspend Mode, according to bit 6 (CPUOFF-SUS) in the REFCTL Register. If powered off, a local bus reset occurs during a resume from the Suspend Mode (RESCPU and RESNPX driven high).
- The internal state and register values of the VL82C316 are maintained during the Suspend Mode.

Entering the Suspend Mode

The Suspend Mode is activated by asserting the –SUSPEND input to the VL82C316. In designs where the companion VL82C323 Power Management Unit (PMU) is used, –SUSPEND is connected to the PWGOUT output from the VL82C323. Upon completion of the next refresh cycle (Hold Acknowledge state), the VL82C316's suspend state machine is engaged to stop all non-essential clocks and gate control inputs to an inactive state. Leakage control is enabled to eliminate power dissipation due to floating lines. The Suspend Mode refresh controller begins operation immediately upon entering the Suspend Mode to minimize the time delay between refresh cycles. Only on-board DRAM is refreshed using either CAS-before-RAS or self-refresh, depending upon the state of the REFCTL Register during the Suspend Mode. Since no refresh burst is performed when entering or exiting the Suspend Mode, RAS-only refresh should not be used since the internal DRAM address counter state may not be known.

An option is included in the VL82C316 to power the CPU/local bus interface off during the Suspend Mode (REFCTL Register bit 6, CPUOFF-SUS). If SUSMODE is set to 0 (default), the CPU interface remains powered up and the CPU local bus remains in a hold state during the Suspend Mode. If CPUOFF-SUS is set to 1, the CPU interface is powered off during the Suspend Mode. Most pins are three-stated and pull-downs are enabled to prevent leakage from floating lines. Refer to the "Pin Type by Operational State" table starting on page 6 for further details.

The amount of time required to complete the transition varies depending on the time between the –SUSPEND signal going low and the next refresh cycle. It should never exceed 1 ms. Once in the Suspend Mode, external peripherals (including oscillators) may be safely powered off without affecting the internal state of the VL82C316. The VL82C323 PMU delays a minimum 500 ms before power is removed once the PWGOUT (–SUSPEND) signal is activated.

Exiting the Suspend Mode (Resume)

A minimum Suspend Mode time is not specified, however, some self-refresh DRAMs require several milliseconds to transition to and from the Self-Refresh Mode. The Suspend Mode is exited by raising the –SUSPEND line high to the VL82C316. It is assumed that once –SUSPEND is de-asserted, all oscillators and other peripheral elements are powered and stabilized. The VL82C323 delays a minimum 500 ms from the start of a Resume and the de-assertion of PWGOUT (–SUSPEND). Once –SUSPEND is sampled high using the 32 kHz clock, all clocks are re-started. The suspend state machine re-enables outputs and forces a system reset (RSTDRV active) for a minimum of 2 ms. If the CPU interface is powered off (bit 6, CPUOFF-SUS, in the REFCTL Register is 1), a local bus reset also occurs (RESCPU and RESNPX driven high). At the end Resume, the suspend refresh controller stops operation and refresh is allowed to continue using the standard mechanism (based on the 14.318 MHz clock).

Powering the VL82C316 Off During Suspend Mode

For even lower power dissipation while in the Suspend Mode, the VL82C316 may be powered off with the companion VL82C323 PMU performing refresh of the system DRAM. In this case, the internal registers and machine state of the VL82C316 must be saved to backup memory or to disk prior to entering the Suspend Mode so they be restored later. Using the IO Break mechanism (described in the section titled "SMM IO Break Functions") and the AMD Am386SXLV CPU, a simple, low-cost method is available to accurately shadow the machine state of the internal VL82C316 peripherals (e.g., 82C37A, 82C59A, 892C54, etc.) with minimal performance impact. This leads to a reliable, robust Suspend-Resume Mode sequence even if power is removed to the VL82C316.

In this situation, all power to the VL82C316 is removed except for the DRAM interface (VDDB). The –RAS and –CAS outputs from the VL82C323 PMU are wire-ORed to those from the VL82C316 and enabled during the Suspend Mode for either CAS-before-RAS or Self-Refresh Modes. Refer to the VL82C323 data sheet for further information.

Applications Note:

When a standard software reset command is issued, the BIOS must first be sure A20GATE is enabled. Otherwise, A20 is forced low by the system and the reset jump address is fetched from the wrong memory location. This same consideration is required in the Power Off Suspend Mode.

ISA BUS INTERFACE

The ISA bus is accessed in the CPU Mode, DMA Mode, Refresh Mode, and Bus Master Mode.

In the CPU Mode, the 82288 megacell is responsible for generating the command signals –IOR, –IOW, –MEMR, –MEMW, –SMEMR, –SMEMW, and BALE. The VL82C316 samples the inputs –MEMCS16, –IOCS16, and IOCHRDY. The signal –WS0 determines the length in wait states of each bus cycle.

During refresh, the VL82C316 drives the –REFRESH signal, a refresh address, and –MEMR command onto the bus to implement the refresh cycle. The refresh circuit samples IOCHRDY to determine if the –MEMR and –REFRESH pulses need to be extended. The output BALE is driven high during the refresh cycles.

In DMA Mode, the DMA controllers generate the command and address signals. BALE is forced high for all DMA cycles. The VL82C316 asserts the AEN signal to indicate that the current address on the bus is for memory only and is not to be decoded as an I/O address. The DMA section samples IOCHRDY to extend bus cycles longer than the internally defined cycle length.

The Bus Master Mode is an extension of the DMA Mode. A bus master can get control of the bus by requesting a DMA operation. Once the DMA is acknowledged, the –MASTER signal is pulled active and the VL82C316 relinquishes control of the bus to the master.

BUS CONTROL REGISTERS (BUSCTL)

Three bus control options are provided and are programmable via the indexed BUSCTL Register. It controls the number of wait states to be inserted in the 8-bit and 16-bit slot cycles and determines the width of the BIOS ROM. Tables 24 and 25 give the formats of the BUSCTL1 and BUSCTL2 Registers.

TABLE 24. BUSCTL1 CONFIGURATION REGISTER (READ/WRITE)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
BUSCTL1 (16h)	ROMWID	R	DSKTMG	LBAEN	R	CMDLY2	R	CMDLY1
POR Value	MA10/–WE1	X	1	0	X	0	X	0

Bit	Name	Function
7	ROMWID	ROM Width: This bit determines the width of the BIOS ROM. When set, the BIOS ROM is assumed to be 16 bits wide and connected to D15-D0. When 0, 8-bit BIOS ROM is assumed to be on D15-D8 (8-bit ROM resides on the upper byte of the D bus). The initial power-on reset value of this bit is set the same as MA10 at the end of the reset period.
6	R	Reserved: This bit is currently undefined. For compatibility with future versions of this product, this register should always be written such that value of this bit is not altered.
5	DSKTMG	Disk Timing: When set to 1, the first memory cycle after an I/O cycle is run at the programmed Non-Turbo frequency for compatibility with older programmed I/O devices. When set to 0, the first memory cycle after an I/O cycle is run at full speed. The default value of this bit is 1.
4	LBAEN	Local Bus Access Enable: When set to 1, the –LBA pin is active and local bus peripherals may drive –LBA low to cause the VL82C316 to ignore the current cycle. When set to 0, the state of the –LBA pin has no effect. The default value of this bit is 0.
3	R	Reserved: This bit is currently undefined. For compatibility with future versions of this product, this register should always be written such that value of this bit is not altered.
2	CMDLY2	Command Delay 2: This bit allows the addition of one extra command delay for 8-bit and 16-bit I/O cycles and for 8-bit memory cycles. When set to 0, there is no added command delay. The default value of this bit is 0.
1	R	Reserved: This bit is currently undefined. For compatibility with future versions of this product, this register should always be written such that value of this bit is not altered.
0	CMDLY1	Command Delay 1: This bit allows the addition of one extra command delay for 16-bit memory cycles. When set to 0, there is no added command delay. A value of 1 adds one command delay. The default value of this bit is 0.

TABLE 25. BUSCTL2 CONFIGURATION REGISTER (READ/WRITE)

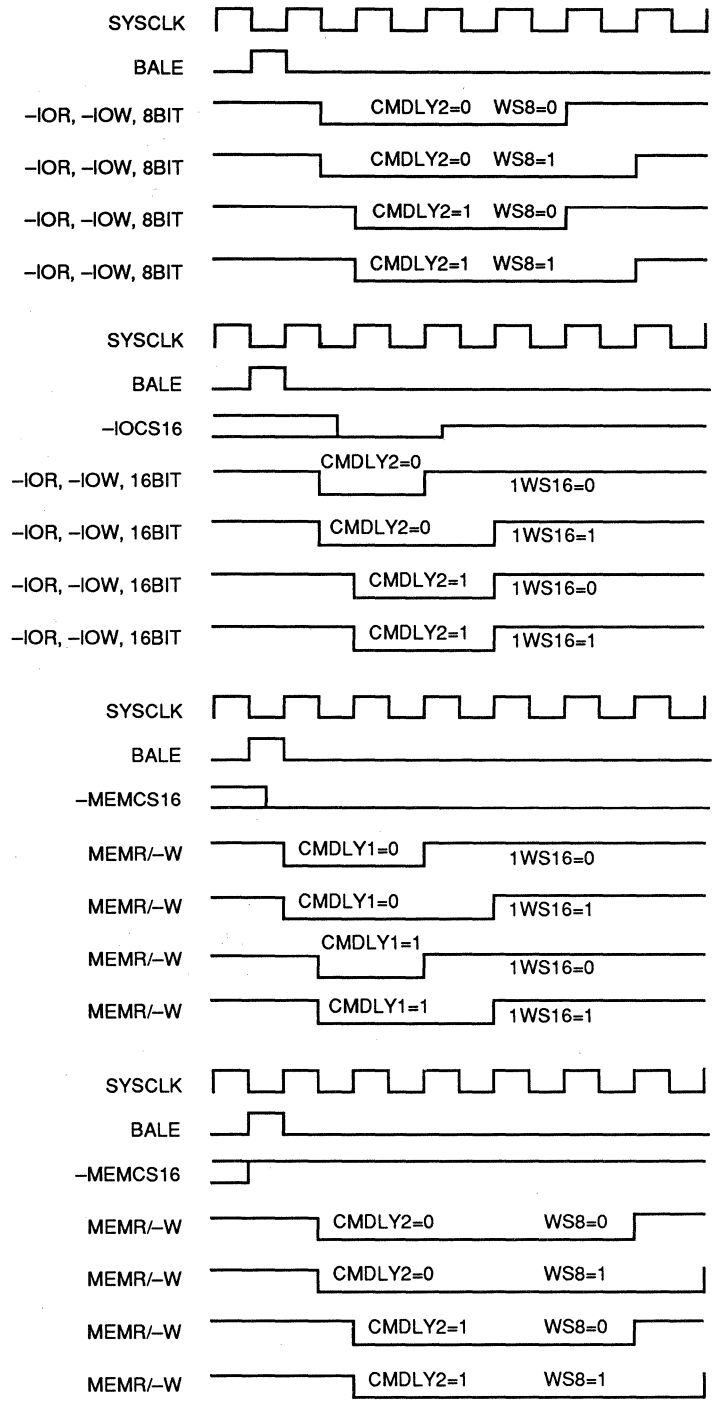
Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
BUSCTL2 (17h)	–CLK2OFF	–DMAPWR	R	R	R	1WS16	R	WS8
POR Value	1	1	X	X	X	0	X	0

Bit	Name	Function
7	–CLKOFF	Clock 2 Off: When 0, CLK2 will be gated low when the Sleep Mode is entered. CLK2 automatically resumes at the preprogrammed frequency when the Sleep Mode is permanently or temporarily exited by any of the previously documented means. When 1, the clock divider programmed into bits 6-3 (DIVCLK3-DIVCLK0) of the SLPCTL Register is active when the Sleep Mode is entered. The default value of this bit is 1.
6	–DMAPWR	DMA Power Managed: When 0, the DMA automatically enables its DMA clocks when a DRQ signal is sensed. The clock is turned off when all external DRQ and internal DACK signals are inactive. Separate circuitry controls both DMA controllers; i.e, activation of a specific DRQ signal only enables the DMA clock for its DMA controller. When 1, the DMACLK is always enabled. In either case, the DMA clock frequency is determined by the value programmed into bit 1 (DMACLK) of the ROMDMA Register. The default value of this bit is 1.
5-3	R	Reserved: These bits are currently undefined. For compatibility with future versions of this product, this register should always be written such that value of this bit is not altered.
2	1WS16	16-Bit Wait States: This bit determines the number of wait states for 16-bit slot bus accesses. The extended range of wait states may be required for hardware board compatibility if faster BUSCLK frequencies are used. When set to 0, zero wait state operation is enabled. 0 = 0WS, 1 = 1WS. The default value of this bit is 0.
1	R	Reserved: This bit is currently undefined. For compatibility with future versions of this product, this register should always be written such that value of this bit is not altered.
0	WS8	8-Bit Wait States: This bit determines the number of wait states for 8-bit slot bus accesses. The provided range allows for faster or slower than normal 8-bit bus operation in order to optimize compatibility and performance for a wide variety of add-in cards. 0 = 4WS, 1 = 5 WS. The default value of this bit is 0.

Zero wait state operation is possible on extremely fast boards that can pull the –WS0 line fast enough and more than five wait states are possible if IOCHRDY is pulled low before the last normal wait state. However, –MEMCS16 or –IOCS16 must be pulled low before the last normal wait state even if IOCHRDY has previously been activated.

Figure 13, Default ISA and Memory Cycles, shows the effect of IWS16 and WS8 in the BUSCTL2 and CMDLY1 and CMDLY2 in BUSCTL1 on default cycles, (0WS and IOCHRDY not asserted).

FIGURE 13. DEFAULT ISA AND MEMORY CYCLES



KEYBOARD CONTROLLER

The VL82C316 contains an integral PC/AT or PS/2 compatible keyboard controller. When PS/2 Mode is programmed under software control, the mouse data and clocks pins are activated. Note that there are no A20GATE or –RC pins on the VL82C316. These two signals are generated internally in the VL82C316. The data lines are checked for a particular data sequence when the keyboard controller is selected to generate A20GATE and –RC.

For the hardware compatibility, the generation of –RC is delayed by about 50 µs from the issuance of the command to generate a 6 µs pulse. A delay timer is used in the internal circuit for this purpose. This timer can be disabled by the bit FASTRC (bit 5) in the MISCSET Register. When FASTRC is 1, –RC is generated with only a 6.72 µs delay. This provides an alternative for "Fast CPU Reset."

The keyboard controller is accessed via internally decoded port 60h (read/write data) and port 64h (read status/write command).

PC/AT or PS/2 compatibility is controlled via bit 1 (MODE) of the KBDCTL Register.

KEYBOARD CONTROLLER FUNCTIONAL DESCRIPTION

The VL82C316 keyboard controller's microcontroller unit (MCU) offers a subset of the instruction set of the 8042, with 8042-like instructions. Enhancements have been made to conditional jumps (jumps may be made between pages). The on-chip ROM is loaded with the code that is required to support the PC/AT and PS/2 command sets and 128 bytes of conversion code. A small amount of scratch-pad RAM is provided as an extension of the MCU register set for the purpose of keyboard to host interfacing.

Keyboard serial I/O is handled with hardware implementations of the receiver and transmitter. Both functions depend on an 8-bit timer for time-out detection. Enhanced status reporting is provided in hardware to simplify error handling in software. This logic is duplicated for the mouse interface.

User RAM support is provided. The program writes the 5-bit address (32 byte range) to a register, and then reads or writes the data through accesses to another register, port 60h DBB.

Parallel ports 1 and 2 are provided, but are restricted to inputs only for P1 and outputs only to P2.

Support for port 60h DBB (reads and writes) and Status Register (reads and writes) is provided in hardware for interface to the PC host.

Common PC/AT uses for the parallel I/O bits are shown below.

- P16 - Color/Monochrome input:
  Not used, BIOS determines monitor type automatically.
- P17 - Key switch input:
  When the SMI Mode is not enabled (SMICTL bit 7 = 0), pin 31 (–SMI/KEYSW) is configured as an input and is connected to the P17 input of the keyboard controller. When the SMI Mode is enabled (SMICTL bit 7 = 1), this input is held high.
- P20 - Reset CPU output:
  Used internally and not brought to an output pin on the VL82C316.
- P21 - A20 Gate output:
  Used internally and not brought to an output pin on the VL82C316.
- P22 - Speed Select output:
  Used internally and not brought to an output pin on the VL82C316.
  This signal is internally combined with other hardware and software selectable Turbo request sources in order to generate a composite Turbo request signal.

KEYBOARD CONTROLLER INTERFACE TO PC/AT

The interface to the PC/AT consists of one register pair (60h/64h) for the keyboard and mouse. Access to the registers is determined by the state of A2 and the chip select. For host control signals involved, the Command, Status, and Data Registers are accessed as shown in Table 26.

The port 60h DBB read operations output the contents of the Output Buffer to D7-D0 (host bidirectional, three-statable data bus), and clears the status of the Output Buffer Full (OBF/Status Register bit 0) bit.

Status read operations output the contents of the Status Register to D7-D0. No status is changed as a result of the read operation.

The port 60h DBB write operations cause the Input Buffer DBB to be changed. The state of the C/D bit is cleared (Status Register bit 3, a 0 indicates data) and the Input Buffer Full (IBF/Status Register bit 1) bit is set (1).

Command write operations are the same as DBB writes, except that the address is 64h. The C/D bit will be set (1) when a command has been written to address 64h.

TABLE 26. ACCESSING THE COMMAND, STATUS, AND DATA REGISTERS

–CS	–IOR	–IOW	A2	Register
0	0	1	0	Read - Data DBB Output Buffer
0	0	1	1	Read - Status
0	1	0	0	Write - Data DBB Input Buffer
0	1	0	1	Write - Command
1	X	X	X	Not Valid

KEYBOARD CONTROLLER INTERFACE PROTOCOL

Data transmission between the controller and the keyboard or mouse consist of a synchronous bit stream over the data and clock lines. The bits are defined as follows:

Bit	Function
1	Start bit (always 0)
2	Data bit 0 (LSB)
3-8	Data bits 1-6
9	Data bit 7 (MSB)
10	Parity bit (odd)
11	Stop bit (always 1)

Figures 14 and 15 show the states that are implemented for receive and transmit operations from the controller to the keyboard, respectively.

FIGURE 14. CONTROLLER RECEIVES FROM KEYBOARD

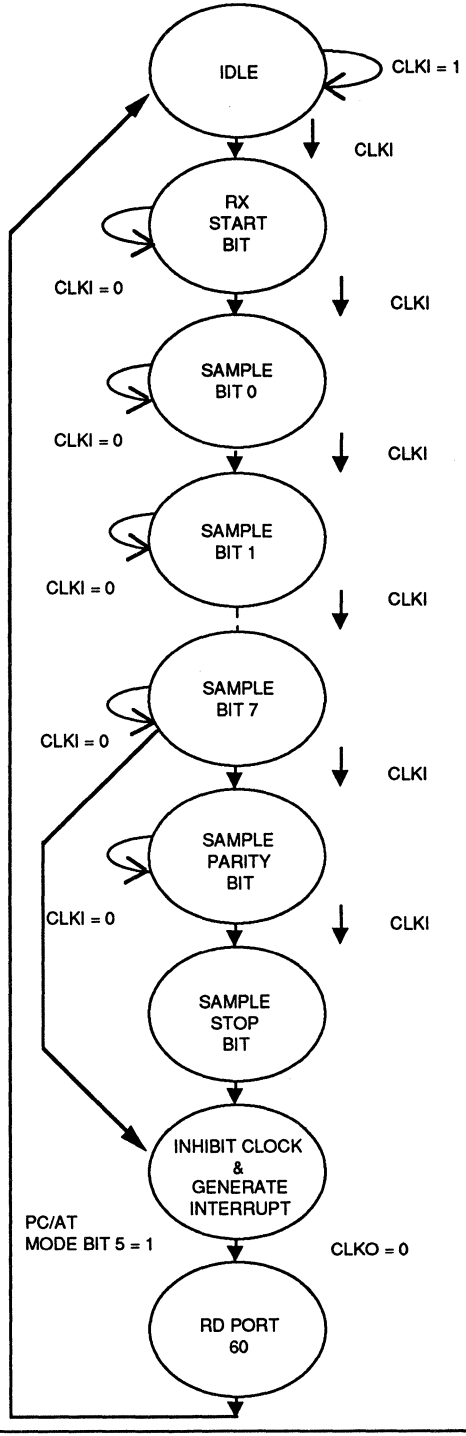
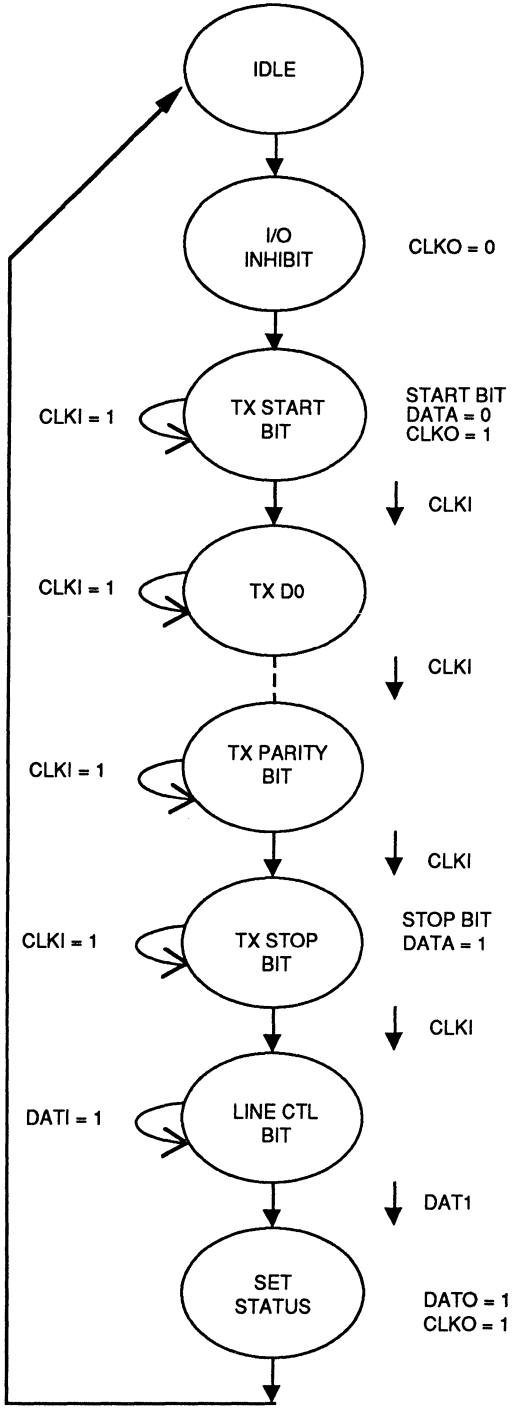


FIGURE 15. CONTROLLER TRANSMITS TO KEYBOARD



PROGRAMMER INTERFACE

The programmer interface to the keyboard controller is quite simple. It consists of four registers:

Register	R/W	I/O
Status	R	64h
Command	W	64h
Output Buffer	R	60h
Input Buffer	W	60h

The behavior of these registers differ according to the mode of operation (PC/AT or PS/2). There exists only one Status Register with different bit definitions for PC/AT Mode and PS/2 Mode. The bit definitions for the Status Register in each mode are listed in Tables 27 and 28.

TABLE 27. PC/AT STATUS REGISTER (READ-ONLY)

PCATSTAT	D7	D6	D5	D4	D3	D2	D1	D0
(64h)	PERR	RTIM	TTIM	KBEN	C/D	SYS	IBF	OBF
POR Value	0	0	0	1	0	0	0	0

Bit	Name	Function
7	PERR	Parity Error: When 1, it indicates that a parity error (even parity = error) occurred during the last transmission (received scan code) from the keyboard. When a parity error is detected, the output buffer is loaded with FFh, the OBF status bit is set, and the KIRQ pin is set (1 if the EKI bit/Mode Register bit 0 is set (1)).
6	RTIM	Receive Time-Out: When 1, it indicates that a transmission from the keyboard was not completed before the controller's internal timer timed out. 0 = normal, 1 = time-out occurred.
5	TTIM	Transmit Time-Out: When 1, it indicates that a transmission to the keyboard was not completed before the controller's internal timer timed-out. 0 = normal, 1 = time-out occurred.
4	KBEN	Keyboard Enable: When 1, this bit indicates that the keyboard is currently enabled. When reset, it indicates that the keyboard is inhibited.
3	C/D	Command/Data: When 1, this bit indicates that a command has been placed into the input data buffer of the controller. A 0 indicates data. The controller uses this bit to determine if the byte written is a command to be executed. This bit is updated when the next byte is written to the input data buffer.
2	SYS	System Flag: When this bit is set (1), it indicates that the CPU has changed from Virtual to Real Mode.
1	IBF	Input Buffer Full: This flag is set on a write to port 60h or 64h. It is cleared when the microcontroller reads the DBBIN contents into the accumulator. A 0 indicates the input buffer is empty and a 1 that it is full.
0	OBF	Output Buffer Full: This flag is automatically set when the microcontroller loads DBBOUT. It is cleared on a read to port 60h. A 0 indicates the output buffer is empty and a 1 that it is full.

TABLE 28. PS/2 STATUS REGISTER (READ-ONLY)

PS2STAT	D7	D6	D5	D4	D3	D2	D1	D0
(64h)	PERR	GTO	ODS	KBEN	C/D	SYS	IBF	OBF
POR Value	0	0	0	1	0	0	0	0

Bit	Name	Function
7	PERR	Parity Error: When 1, it indicates that a parity error (even parity = error) occurred during the last transmission (received scan code) from the keyboard. When a parity error is detected, the output buffer is loaded with FFh, the OBF status bit is set, and the KIRQ pin is set (1 if the EKI bit/Mode Register bit 0 is set (1)).
6	GTO	General Time-Out Error: When 1, it indicates that a transmission was started and that it did not complete within the normald time taken (approximately 11 KCLK cycles). If the transmission originated from the controller, a FEh is placed in the output buffer. If the transmission originated from the keyboard, a FFh is placed in the output buffer.
5	ODS	Output Buffer Data Source: When 1, it indicates that the data in the output buffer is mouse data. When reset, it indicates the data is from the keyboard.
4	KBEN	Keyboard Enable: When 1 , this bit indicates that the keyboard is currently enabled. When reset, it indicates that the keyboard is inhibited.
3	C/D	Command/Data: When 1, this bit indicates that a command has been placed into the input data buffer of the controller. A 0 indicates data. The controller uses this bit to determine if the byte written is a command to be executed. This bit is updated when the next byte is written to the input data buffer.
2	SYS	System Flag: When this bit is 1, it indicates that the CPU has changed from the Virtual to Real Mode.
1	IBF	Input Buffer Full: This flag is set on a write to port 60h or 64h. It is cleared when the microcontroller reads the DBBIN contents into the accumulator. A 0 indicates the input buffer is empty and a 1 that it is full.
0	OBF	Output Buffer Full: This flag is automatically set when the microcontroller loads DBBOUT. It is cleared on a read to port 60h. A 0 indicates the output buffer is empty and a 1 that it is full.

KEYBOARD CONTROLLER COMMAND SET

The command set described below is supported by PC Keyboard Code Version Rev. B which must be downloaded from the host into the keyboard controller. It supports two modes of operation and a set of extensions to the AT command set for the PS/2 Mode. In both modes, the command is implemented by writing the command byte to 64h. Any subsequent data is read from 60h (see description for Command 20 in Table 16) or written to 60h (see description of Command 60, also in Table 16). The commands for each mode are shown in Tables 29 and 30.

Command Descriptions

The keyboard controller will support the following command set, which is described as the hex command code, followed by a description:

20 Read keyboard controller's Mode Register (PC/AT and PS/2). The keyboard controller sends its current mode byte to the output buffer (accessed by a read of port 60h).

60 Write keyboard controller's Mode Register (PC/AT and PS/2). The next byte of data written to the keyboard data port (60h) is placed in the controller's Mode Register.

The bit definitions of the Mode Register for each mode (PC/AT or PS/2) are described in Tables 31 and 32.

TABLE 29. PC/AT & PS/2 COMMANDS

Command	Description
20	Read Mode Register
60	Write Mode Register
21-3F	Read Keyboard Controller RAM (Byte 1-31)
61-7F	Write Keyboard Controller RAM (Byte 1-31)
AA	Self-Test
AB	Keyboard Interface Test
AC	Diagnostic Dump
AD	Disable Keyboard
AE	Enable Keyboard
C0	Read Input Port (P10-P17)
D0	Read Output Port (P20-P27)
D1	Write Output Port (P20-P27)
E0	Read Test Inputs (T0, T1)
F0-FF	Pulse Output Port (P20-P27)

TABLE 30. ADDED PS/2 COMMANDS

Command	Description
A4	Test Password
A5	Load Password
A6	Enable Password
A7	Disable Mouse
A8	Enable Mouse
A9	Mouse Interface Test
C1	Poll Input Port Low (P10-P13 = S4-S7)
C2	Poll Input Port High (P14-P17 = S4-S7)
D2	Write Keyboard Output Buffer
D3	Write Mouse Output Buffer
D4	Write to Mouse

TABLE 31. PC/AT MODE REGISTER (READ/WRITE - COMMAND 20H/60H)

PCATMODE	D7	D6	D5	D4	D3	D2	D1	D0
(60h)	R	KCC	KBD	DKB	INH	SYS	R	EKI
POR Value	0	0	0	1	0	0	0	0

Bit	Name	Function
7	R	Reserved: This bit should be written as 0.
6	KCC	Keycode Conversion: When 1, it causes the controller to convert the scan codes to PC format. When reset, the codes are passed along unconverted.
5	KBD	Keyboard Type: When 1, it allows for compatibility with PC-style keyboards. In this mode, parity is not checked and scan codes are not converted.
4	DKB	Disable Keyboard: When 1, it disables the keyboard by holding the KCLK line high.
3	INH	Inhibit Override: When 1, it disables the keyboard inhibit function (P17 switch).
2	SYS	System Flag: When 1, it writes the system flag bit 2 of the Status Register to 1. This bit is used to indicate a switch from Virtual to Real Mode when set.
1	R	Reserved: This bit should be written as 0.
0	EKI	Enable Keyboard Interrupt: When 1, it allows the controller to generate a keyboard interrupt whenever data (keyboard or controller) is written into the output buffer.

TABLE 32. PS/2 MODE REGISTER (READ/WRITE - COMMAND 20H/60H)

PS2MODE	D7	D6	D5	D4	D3	D2	D1	D0
(60h)	R	KCC	DMS	DKB	R	SYS	EMI	EKI
POR Value	0	0	0	1	0	0	0	0

Bit	Name	Function
7	R	Reserved: This bit should be written as 0.
6	KCC	Keycode Conversion: When 1, it causes the controller to convert the scan codes to PC format. When reset, the codes are passed along unconverted.
5	DMS	Disable Mouse: When 1, it disables the mouse by holding the KSRE output high in the PS/2 Mode.
4	DKB	Disable Keyboard: When 1, it disables the keyboard by holding the MCLK line high.
3	R	Reserved: This bit should be written as 0.
2	SYS	System Flag: When 1, it writes the system flag bit 2 of the Status Register to 1. This bit is used to indicate a switch from the Virtual to Real Mode when set.
1	EMI	Enable Mouse Interrupt: When 1, it allows the controller to generate a mouse interrupt when mouse data is available in the output buffer.
0	EKI	Enable Keyboard Interrupt: When 1, it allows the controller to generate a keyboard interrupt whenever data (keyboard or controller) is written into the output buffer.

Command Descriptions (Cont.)

21-3F Read Keyboard Controller RAM (PC/AT and PS/2): Bits D4-D0 specify the address.

61-7F Write the Keyboard Controller RAM (PC/AT and PS/2): This command writes to the keyboard controller RAM with the address specified in bits D4-D0.

A4 Test Password Installed (PS/2 only): This command checks if there is currently a password installed in the controller. The test result is placed in the output buffer (the OBF bit is set) and KIRQ is asserted (if the EKI bit is set). Test result - FAh means that the password is installed, and F1h means that the password is not installed.

A5 Load Password (PS/2 only): This command initiates the password load procedure. Following this command, the controller will take data from the input buffer port (60h) until a 00h is detected or a full 8-byte password, including a delimiter (e.g. <cr>), is loaded into the password latches.

Note: This means that during password validation, the password can be a maximum of seven bytes plus a delimiter such as <cr>.

A6 Enable Password (PS/2 only): This command enables the security feature. The command is valid only when a password pattern is written into the controller (see A5 command). No other commands will be "honored" until the security sequence is completed and command A6 is cleared.

A7 Disable Mouse (PS/2 only): This command sets bit 5 of the Mode Register which disables the mouse by driving the KSRE line (mouse clock) high.

A8 Enable Mouse (PS/2 only): This command resets bit 5 of the Mode Register, thus enabling the mouse again.

A9 Mouse Interface Test (PS/2 only): This command causes the controller to test the mouse clock and data lines. The results are placed in the output buffer (the OBF bit is set) and the KIRQ line is asserted (if the EKI bit is set). The results are as follows:

Data	Meaning
00	No Error
01	Mouse Clock Line Stuck Low
02	Mouse Clock Line Stuck High
03	Mouse Data Line Stuck Low
04	Mouse Data Line Stuck High

AA Self-Test (PC/AT and PS/2): This commands the controller to perform internal diagnostic tests. A 55h is placed in the output buffer if no errors were detected. The OBF bit is set and KIRQ is asserted (if the EKI bit is set).

AB Keyboard Interface Test (PC/AT and PS/2): This command causes the controller to test the keyboard clock and data lines. The test result is placed in the output buffer (the OBF bit is set) and the KIRQ line is asserted (if the EKI bit is set). The results are as follows:

Data	Meaning
00	No Error
01	Keyboard Clock Line Stuck Low
02	Keyboard Clock Line Stuck High
03	Keyboard Data Line Stuck Low
04	Keyboard Data Line Stuck High

AC Diagnostic Dump (PC/AT only, reserved on PS/2): Sends 16 bytes of the controller's RAM, the current state of the input port, and the current state of the output port to the system.

AD Disable Keyboard (PC/AT and PS/2): This command sets bit 4 of the Mode Register to a 1. This disables the keyboard by driving the clock line (KCLK) high. Data will not be received. The keyboard will be enabled after the system sends data to be transmitted to the keyboard.

AE Enable Keyboard (PC/AT and PS/2): This command resets bit 4 of the Mode Register to a 0. This enables the keyboard again by allowing the keyboard clock to free-run.

C0 Read P1 Input Port (PC/AT and PS/2): This command reads the keyboard input port and places it in the output buffer. This command overwrites the data in the buffer.

C1 Poll Input Port Low (PS/2 only): P1 bits 0-3 are written into Status Register bits 4-7. The bits are restored to their original status upon a write to port 64h.

C2 Poll Input Port High (PS/2 only): P1 bits 4-7 are written into Status Register bits 4-7. The bits are restored to their original status upon a write to port 64h.

D0 Read Output Port (PC/AT and PS/2): This command causes the controller to read the P2 output port and place the data in its output buffer. The definitions of the bits are as follows:

Bit	Pin	PC/AT Mode	PS/2 Mode
0	P20*	–RC	–RC
1	P21*	A20 Gate	A20 Gate
2	P22	Speed Select (Turbo)	Mouse Data
3	P23		Mouse Clk
4	P24	KIRQ	KIRQ
5	P25		MIRQ
6	P26	–KCKOUT	–KCKOUT
7	P27	KDOUT	–KDOUT

* These signals are not used either from the internal keyboard controller or when connected to an external keyboard controller. Internal logic is used to emulate this function (See the section "Emulation of A20GATE and –RC" for more details

D1 Write Output Port (PC/AT and PS/2): The next byte of data written to the keyboard data port (60h) will be written to the controller's output port. The definitions of the bits are defined as previously stated. In PC/AT Mode, P26 and P27 will not be altered. In PS/2 Mode, P22, P23, P26, and P27 cannot be altered.

D2 Write Keyboard Output Buffer (PS/2 only): The next byte written to the data buffer (60h) is written by the output buffer (60h) as if initiated by the keyboard (the OBF bit is set (1) and KIRQ will be set if the EKI bit is set (1)).

D3 Write Mouse Output Buffer (PS/2 only): The next byte written to the data buffer (60h) is written to the output buffer as if initiated by the mouse (the OBF bit is set (1), and MIRQ will be set if the EMI bit is set (1)).

D4 Write to Mouse (PS/2 only): The next byte written to the data buffer (60h) is transmitted to the mouse.

Note: If data is written to the data buffer (60h) and the command preceding it did not expect data from the port (60h), the data will be transmitted to the keyboard.

E0 Read Test Inputs (PC/AT and PS/2): This command causes the controller to read the T0 and T1 input bits. The data is placed in the output buffer with the following meanings:

Bit	PC/AT Mode	PS/2 Mode
0	Keyboard Clk	Keyboard Clk
1	Keyboard Data	Mouse Clk
3-7	Read as 0s	Read as 0s

F0-FF Pulse Output Port (PC/AT and PS/2): Bits 0 through 3 of the controller's output port may be pulsed low for approximately 6 µs. Bits 0 through 3 of the command specify which bit will be pulsed. A 0 indicates that the bit should be pulsed, a 1 indicates that the bit should not be modified. FF is treated as a special case (Pulse Null Port).

Note: In PS/2 Mode, bits P22 and P23 will not be pulsed.

EMULATION OF A20GATE AND –RC

When an external keyboard controller (8042) is used with the VL82C316, it is connected as shown in Figure 16. Note that there are no A20GATE or –RC pins on the VL82C316. The port pins P20 and P21 of an external (or internal) keyboard controller are not connected. These two signals are generated internally in the VL82C316. The data lines are internally monitored for a particular data sequence when the keyboard controller is selected to generate A20GATE or –RC and the VL82C316 emulates these keyboard functions.

For the hardware compatibility, the internal generation of –RC is delayed by about 50 µs from the issuance of the command to generate a 6 µs pulse. A delay timer is used in the internal ciruit for the purpose. This timer can be disabled by the bit FASTRC (bit 5) in the MISCSET Register. When this bit is 1, –RC is generated with only a 6.72 µs delay. This provides an alternative method for "Fast CPU Reset".

The keyboard controller interface signals A20GATE and –RC are emulated internal to the VL82C316. These signals are generated in two ways in a PC/AT-compatible keyboard controller (8042) as described next.

1) Data D1h is written to I/O address 64h. This is a "Write Output Port" command from CPU to the keyboard controller. The next byte written to I/O address 60h then enables or disables A20GATE and –RC. The LSB of this byte is reflected on –RC and bit 1 gets propagated to A20GATE. It should be noted that the I/O address 60h does not have to be written immediately after writing D1h to the address 64h.

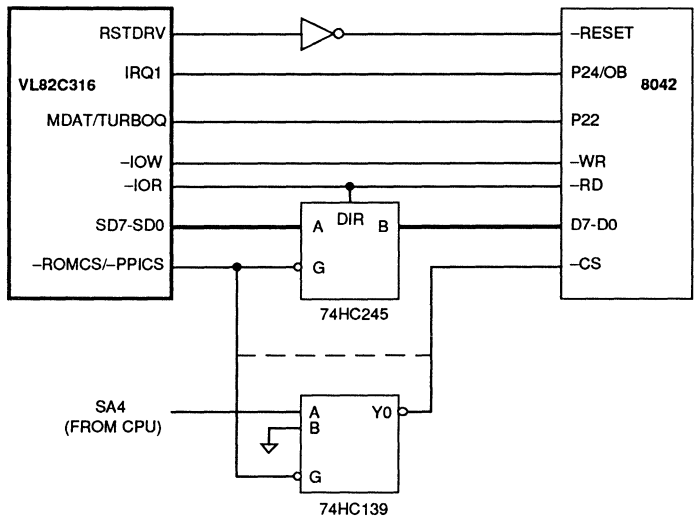
   Only A20GATE is generated in this way in VL82C316 because generation of –RC by this method can hang-up the system. There is no delay involved in the generation of A20GATE .

2) If I/O address 64h is written with F0h-FFh, A20GATE or –RC are pulsed depending on the lower two bits of the data. If bit 0 is low, –RC is pulsed and A20GATE is pulsed if bit 1 is low. The pulse duration is approximately 6 µs.

   The VL82C316 generates a pulsed –RC this way but there is no effect on A20GATE.

To summarize, the VL82C316 allows the use of Method 1 only to generate A20GATE. Method 2 is only allowed to generate –RC.

FIGURE 16. EXTERNAL KEYBOARD CONTROLLER INTERFACE (WHEN INTERNAL KEYBOARD CONTROLLER DISABLED)



KEYBOARD POWER MANAGEMENT

The VL82C316's keyboard controller can be put into a low-power mode of operation in which the high frequency internal clock to the keyboard controller is stopped and resumed in a controlled manner, thereby lowering the power dissipation of the device considerably. Entry into this mode can be controlled by two methods, either automatically under internal hardware control or by a by a software settable control bit. The –HSLP bit (bit 6) in the KBDCTL Register enables either mode of operation.

In the software controlled mode, (–HSLP = 1), the keyboard clock is disabled by clearing the –SLP bit (bit 0) in the KBDCTL Register. The clock remains disabled until either an I/O read or write operation to addresses 60h or 64h occurs or until a falling edge occurs on the keyboard clock input (KCLK) or the mouse input KSRE (MCLK), if the PS/2 Mode has been enabled. The Sleep Mode's status can be determined by reading bit 7 (–KISLP) of the KBDCTL Register. Note that the software Sleep Mode is a one time event. –SLP automatically resets to 1 on keyboard wake-up and must be rewritten to 0 in order to reneable software Sleep Mode after each wake-up event.

In automatic hardware controlled mode (–HSLP = 0), the clock to the keyboard controller is disabled after KCLK (and MCLK if the PS/2 Mode is enabled) remain inactive for approximatley 750 µs or 100 ms depending on the setting of the SLPCTL bit (bit 3) in the KBDCTL Register. When either a KCLK (or MCLK if PS/2 Mode) falling edge is sensed, an I/O read or write to 60h or 64h, or a rising edge on the –SLEEP pin occurs, the keyboard controller's clock is restarted. (This mode approximates the function of the VL82C312 or VL82C323 PMU's –KBSLOWCK signal used in a VL82C310/VL82C107-based notebook system, but with a much finer degree of control.) The Sleep Mode's status can be determined by reading bit 7 of the KBDCTL Register. The KBDCTL Register format is given in Table 33.

To summarize:

–HSLP	–SLP	System Response
0	X	Hardware Sleep Mode is active. Automatic keyboard clock control occurs. This is the power-on reset default case (01).
1	0	Software Sleep Mode control is active. The keyboard controller clock is stopped.
1	1	Software Sleep Mode is enabled, but not active. The keyboard controller clock always remains active.

TABLE 33. KBDCTL CONFIGURATION REGISTER (READ/WRITE)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
KBDCTL (1Dh)	–KISLP	–HSLP	RAMEN	KBDEN	SLPCTL	PRV	MODE	–SLP
POR Value	1	1	0	1	0	0	1	1

Bit	Name	Function
7	–KISLP	Keyboard In Sleep (active low): Reflects the state of the keyboard controller's Sleep Mode. If high, the keyboard is operating in normal mode. If low, the keyboard is in the Sleep Mode. Meaning is the same for hardware or software Sleep Modes. –KISLP is a read-only bit. Default = 1.
6	–HSLP	Hardware Sleep Enable (active low): When set to 1, the automatic hardware keyboard Sleep Mode function is disabled. Control of the keyboard's Sleep Mode can still be accomplished under software control using the –SLP bit. When set to 0, the automatic hardware Sleep Mode is enabled. Default = 0.
5	RAMEN	PMU RAM Enable: This bit enables accesses to the alternate set of 64 bytes of battery-backed RAM in the RTC. If set (1), accesses to the RTC's addresses from 64h to 127h access the second page of battery-back RAM. Default = 0.
4	KBDEN	Keyboard Enable: When 1, the internal keyboard controller is enabled. When 0, the internal keyboard controller is disabled. In the latter case, an external keyboard controller is required. The VL82C316's –ROMCS/–PPICS signal then includes 60h and 64h in its decode range and the IRQ1 pin is active. The BIOS will automatically determine whether the internal or external keyboard is present and sets this bit accordingly. Default = 1.
3	SLPCTL	Sleep Control: Only active when –HSLP = 0. This bit controls the keyboard or mouse inactivity time-out before turning off the keyboard controller clock. 1 = 500 to 1000 µs, 0 = 62.5 to 125 ms. Default = 0. **Application Note:** Program to a value of 0 for the lowest power operation. When a write to the keyboard scanner is made (60h), the keyboard controller implements a 28 ms time-out for a response in case the scanner is inoperative. In order for this to properly function when SLPCTL = 1, the keyboard sleep time automatically extends to the 62.5 to 125 ms interval after each write to port 60h. After that one longer time-out period, the keyboard sleep time-out reverts to the 500 to 1000 µs interval.
2	PRV	Private Controls Enable: If 1, this bit prevents the KHSE, KSRE, and MIRQ pins from changing their current state. If 0, normal operation of these pins result. Default = 0.
1	MODE	PC/AT or PS/2 Mode: If 1, the keyboard operates in the PC/AT-compatible Mode. If 0, the keyboard operates in the PS/2 keyboard and mouse Mode. Default = 0.
0	–SLP	Sleep (active low): If the –HSLP bit is set and –SLP is cleared, the clock to the keyboard controller is disabled. The clock is resumed if an I/O read or write operation to 60h or 64h occurs on the falling edge of the keyboard clock, or on the falling edge of the mouse clock input (if in PS/2 Mode). Resumption of the keyboard clock in the software Sleep Mode also resets the value of the –SLP bit to 1. –SLP must be rewritten to 0 before the software Sleep Mode is activated again. If both the –HSLP and –SLP bits are set, power management of the keyboard controller clock is deactivated. Default = 1.

KEYBOARD CONFIGURATION IN DIFFERENT MODES

Five basic keyboard configuration options exist as shown in Figures 17 through 21. They are as follows:

Option 1 Internal Keyboard Active, PC/AT Mode Active, SMM Mode Inactive:

With this option, the key switch and turbo switch options are available. These signals are muxed with the –SMI/KEYSW and –SADS/TURBOSW pins, respectively. The –SMI/KEYSW input is connected to the keyboard controller's input port bit P17 and is pulled up via an external resistor when the external key switch is open. When the key switch is closed, the KEYSW input is grounded. P22 of the internal keyboard controller is gated with the external –SADS/TURBOSW signal and the VSF Turbo control, if enabled, to generate a composite TURBO signal.

Option 2 Internal Keyboard Active, PS/2 Mode Active, SMM Mode Inactive:

In a standard PS/2 system, front panel turbo and keyswitch options are not supported. However, it is easy to configure the VL82C316's internal keyboard controller for PS/2 keyboard Mode and still support the turbo and keyswitch for use in PC/AT-compatible systems. The main advantage of this mode is the ability to access the PS/2 mouse feature of the keyboard controller in a PC/AT-compatible system. This saves either a slot (as required for PC/AT bus mice) or a serial port (as required by serial mice). The PS/2 mouse uses IRQ12. This requires that the keyboard controller's mouse interrupt signal be gated with the external IRQ12 input.

The –SMI/KEYSW input is connected to the keyboard controller's input port bit P17 and pulled up via an external resistor when the external key switch is open. When the key switch is closed, the KEYSW input is grounded. There is no available output pin from the keyboard controller to drive a keyboard controller controlled Turbo signal. However, the external turbo switch (–SADS/TURBOSW) and VSF Turbo, if internally enabled, are gated to generate a composite TURBO signal.

FIGURE 17. OPTION 1: INTERNAL KEYBOARD ACTIVE, PC/AT MODE ACTIVE, SMM MODE INACTIVE

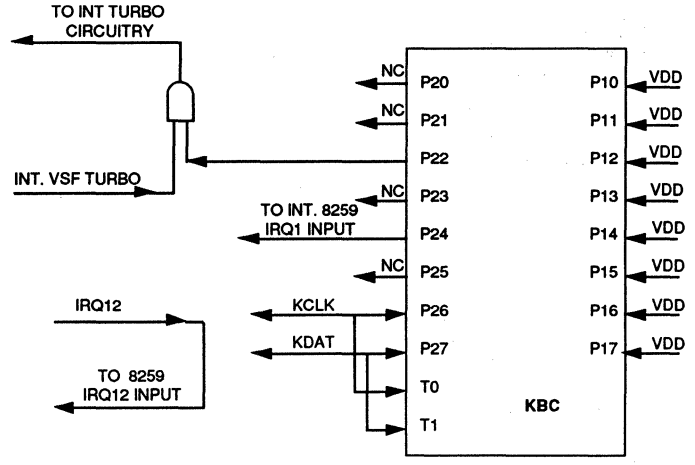
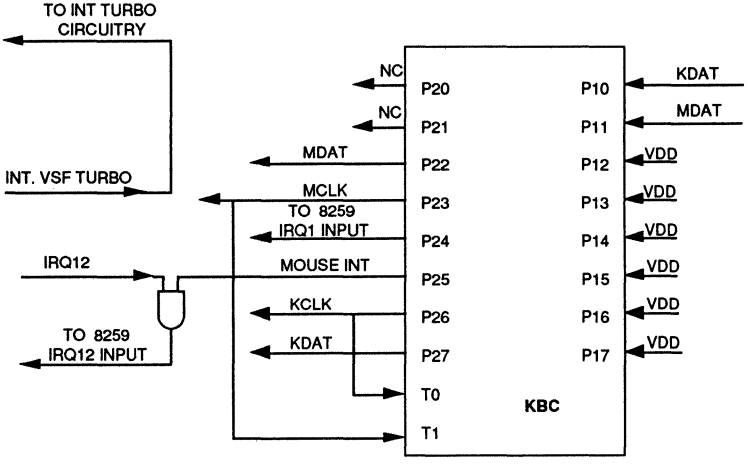


FIGURE 18. OPTION 2: INTERNAL KEYBOARD ACTIVE, PS/2 MODE ACTIVE, SMM MODE INACTIVE



Option 3 Internal Keyboard Active, PC/AT Mode Active, SMM Mode Active:

This option differs from Option 1 only in the fact that the external KEYSW and TURBOSW signals are not available. While the key switch option is totally unavailable in this mode, two of the three turbo options remain. The VSF Turbo Mode, if internally enabled, and P22 of the internal keyboard controller are used to generate a composite TURBO signal.

Option 4 Internal Keyboard Active, PS/2 Mode Active, SMM Mode Active:

The external KEYSW and TURBOSW signals are not available in this mode and only one of the three turbo options remain. The VSF Turbo Mode, if internally enabled, is the only available way to generate a TURBO signal.

As in Option 2, the keyboard controller's mouse interrupt signal is internally combined with the external IRQ12 input.

FIGURE 19. OPTION 3: INTERNAL KEYBOARD ACTIVE, PC/AT MODE ACTIVE, SMM MODE ACTIVE

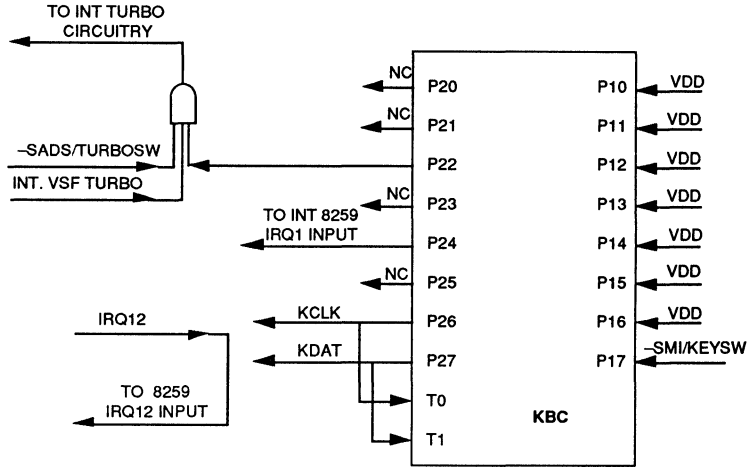
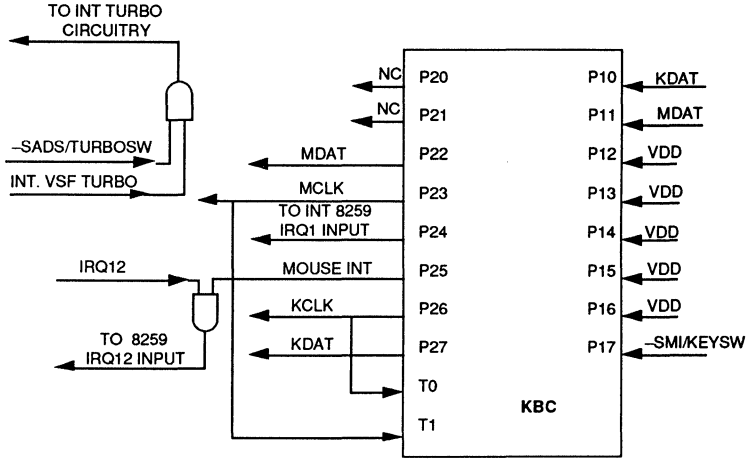


FIGURE 20. OPTION 4: INTERNAL KEYBOARD ACTIVE, PS/2 MODE ACTIVE, SMM MODE ACTIVE



Option 5 External Keyboard Active, SMM Mode Active or Inactive: In this mode, the internal keyboard controller is completely inactive. The turbo function consists of the external MDAT/TURBORQ input gated with the internal VSF Turbo signal, if enabled. The signal driving the MDAT/TURBORQ input may itself be a composite signal consisting of the external keyboard controller's TURBO output (P22) gated with a turbo switch signal.

Table 34 shows in tabluar form the same information as Figures 17 through 21. There are four possible turbo request sources. Table 28 shows which are active in each possible keyboard configuration mode. The active turbo sources are internally ANDed in order to generate the final system turbo request. All active sources must be logically high in order to trigger the Turbo Mode. If any active source goes low, the programmable non-turbo clock divider is activated.

FIGURE 21. OPTION 5: EXTERNAL KEYBOARD ACTIVE, SMM MODE ACTIVE OR INACTIVE

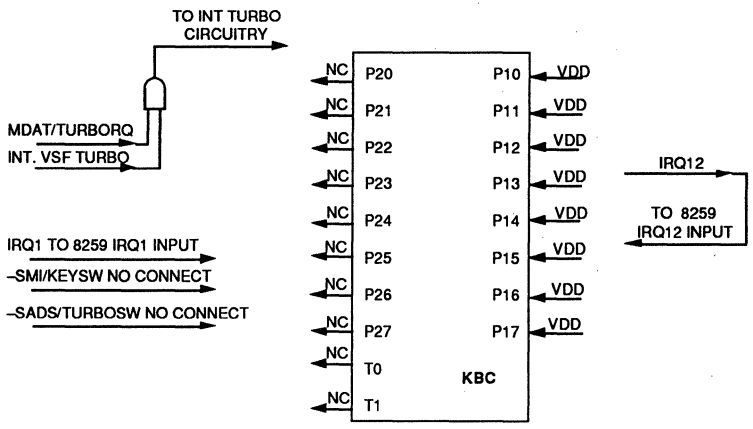


TABLE 34. ACTIVE TURBO OPTIONS BY KEYBOARD MODE

Int KBC Enable	Mode	SMI Enabled	Internal KBC P22	-SADS/TURBOSW	MDAT/TURBORQ	VSF Turbo
Yes	PC/AT	Yes	Yes	No	No	Yes
Yes	PC/AT	No	Yes	Yes	No	Yes
Yes	PS/2	Yes	No	No	No	Yes
Yes	PS/2	No	No	Yes	No	Yes
No	NA	Yes	No	No	Yes	Yes
No	NA	No	No	No	Yes	Yes

REAL-TIME CLOCK

The VL82C316 contains an integral 146818A-compatible real-time clock (RTC). The RTC drives its interrupt out to an external pin. This –RTCIRQ signal allows for interface to external power management subsystems that can take advantage of a pre-programmed RTC interrupt to wakeup the system. It is open drain and only driven when active. This allows the use of an external RTC as an alternate or second device.

The RTC performs the following functions:

- Time of day clock
- Alarm function
- 100 year calendar function
- Programmable periodic interrupt output
- 178 bytes of user RAM
- User RAM preset feature

The RTC contains a patented write-protect circuit to prevent loss of data during power-cycling.

The RTC memory consists of ten RAM bytes which contain the time, calendar and alarm data, four control and status bytes, and 178 general purpose RAM bytes. The address map of the real-time clock is shown as follows:

Addr	Function	Range
0	Seconds (time)	0-59
1	Seconds (alarm)	0-59
2	Minutes (time)	0-59
3	Minutes (alarm)	0-59
4	Hours (time)	0-11, 12 Hr Mode
4	Hours (time)	0-23, 24 Hr Mode
5	Hours (alarm)	0-23
6	Day of Week	1-7
7	Date of Month	1-31
8	Month	1-12
9	Year	0-99
10	RTC Register A	(R/W)
11	RTC Register B	(R/W)
12	RTC Register C	(R-O)
13	RTC Register D	(R-O)
14-127	User RAM (standby)	

All 192 bytes are directly readable and writeable by the processor program except for the following:

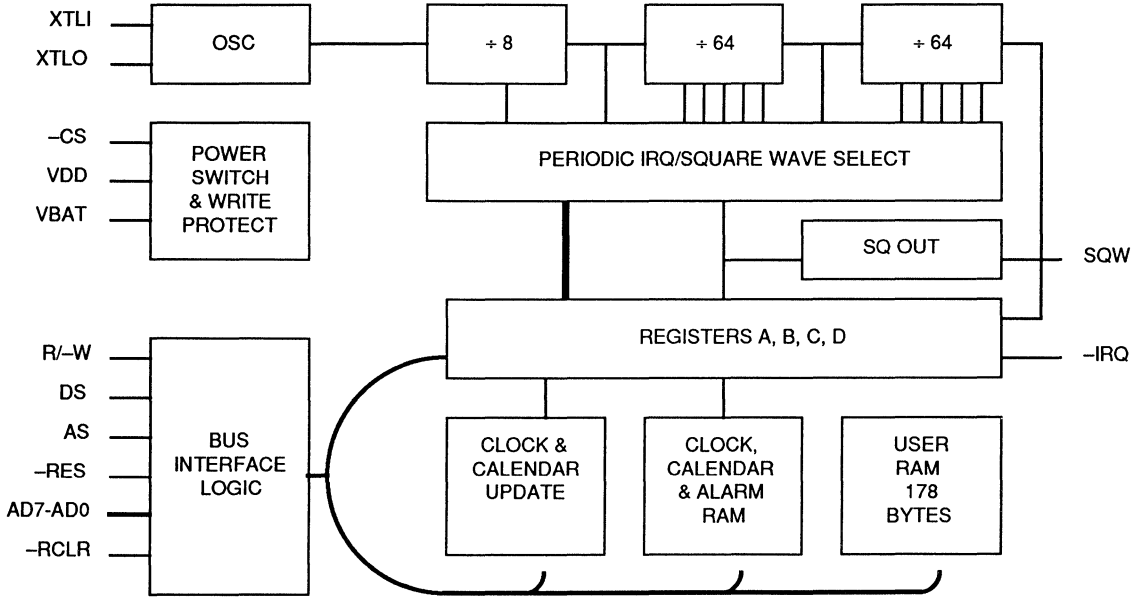
1) Registers C and D are read-only.

The RTC address map also includes additional standby RAM. The bottom 64 bytes of the address space are devoted to the RTC function. Two banks of additional standby RAM is mapped into this space in the index address range of 64-127. Control of which bank is accessed is provided by the RAMEN bit of the KBDCTL Register. The total address map is shown below:

Addr	Function
0-13	Time portion
14-63	Scratch-pad RAM portion
64-127	Dual-mapped additional scratch-pad RAM

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these RAM locations. The contents of the ten time, calendar, and alarm bytes may be either binary or binary-coded decimal (BCD).

FIGURE 22. REAL-TIME CLOCK BLOCK DIAGRAM



TIME OF DAY REGISTER DESCRIPTIONS

The contents of the Time of Day Registers can be either in binary or binary-coded decimal (BCD) format. The address map of these registers is shown below:

Addr	Function	Range
0	Seconds (time)	0-59
1	Seconds (alarm)	0-59
2	Minutes (time)	0-59
3	Minutes (alarm)	0-59
4	Hours (time)	0-11, 12 Hr Mode
4	Hours (time)	0-23, 24 Hr Mode
5	Hours (alarm)	0-23
6	Day of Week	1-7
7	Date of Month	1-31
8	Month	1-12
9	Year	0-99

Address 0 - Seconds:
The range of this register is 0-59 in BCD Mode and 0-3Bh in Binary Mode.

Address 1 - Seconds Alarm:
The range of this register is 0-59 in BCD Mode and 0-3Bh in Binary Mode.

Address 2 - Minutes:
The range of this register is 0-59 in BCD Mode and 0-3Bh in Binary Mode.

Address 3 - Minutes Alarm:
The range of this register is 0-59 in BCD Mode and 0-3Bh in Binary Mode.

Address 4 - Hours:
The range of this register is:

Range	Mode	Time
1-12	BCD	AM
81-92	BCD	PM
01h-0Ch	Binary	AM
81h-8Ch	Binary	PM

Address 5 - Hours Alarm:
The range of this register is:

Range	Mode	Time
1-12	BCD	AM
81-92	BCD	PM
01h-0Ch	Binary	AM
81h-8Ch	Binary	PM

Address 6 - Day of Week:
The range of this register is 1-7 in BCD Mode and 1-7h in Binary Mode.

Address 7 - Date:
The range of this register is 1-31 in BCD Mode and 1-1Fh in Binary Mode.

Address 8 - Month:
The range of this register is 1-12 in BCD Mode and 1-0Ch in Binary Mode.

Address 9 - Year:
The range of this register is 0-99 in BCD Mode and 0-63h in Binary Mode.

RTC CONTROL REGISTER DESCRIPTIONS

The RTC has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle.

Addr	Function	Type
10	RTC Register A	(R/W)
11	RTC Register B	(R/W)
12	RTC Register C	(R-O)
13	RTC Register D	(R-O)
14-63	User RAM (Standby)	(R/W)

Register A Description

This register contains control bits for the selection of the periodic interrupt, input divisor, and update-in-progress (UIP) status bit. The bits in the register are defined as follows:

Bit	Description	Abbr
0	Rate Select bit 0	RS0
1	Rate Select bit 1	RS1
2	Rate Select bit 2	RS2
3	Rate Select bit 3	RS3
4	Divisor bit 0	DV0
5	Divisor bit 1	DV1
6	Divisor bit 2	DV2
7	Update-in-progress	UIP

Bits 0-3 RS0-RS3 - Rate Select: These four rate selection bits select one of 15 taps on the 22-stage divider, or disable the divider output. The tap selected may be used to generate a periodic interrupt. These four bits are read/write bits which are not affected by reset. The periodic interrupt rate that results from the selection of various tap values is as follows:

RS Value	Periodic Interrupt Rate	
0	None	
1	3.90625	ms
2	7.8125	ms
3	122.070	µs
4	244.141	µs
5	488.281	µs
6	976.562	µs
7	1.953125	ms
8	3.90625	ms
9	7.8125	ms
0Ah	15.625	ms
0Bh	31.25	ms
0Ch	62.5	ms
0Dh	125	ms
0Eh	250	ms
0Fh	500	ms

Bits 4-6 DV0-DV2 - Divisor: The three divisor selection bits are fixed to provide for only a five-state divider chain, which would be used with a 32 kHz external crystal. Only bit 6 of this register can be changed allowing control of the reset for the divisor chain. When the divider reset is removed the first update cycle begins one-half second later. These bits are not affected by power-on reset (external pin).

DV Value	Condition
2	Operation Mode, divider running
6	Reset Mode, divider in reset state

Bit 7 UIP - Update-In-Progress: This bit is a status flag that may be monitored by the program. When a 1, the update cycle is in progress or will soon begin. When a 0, the update cycle is not in progress and will not be for at least 244 µs. The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is 0. The UIP bit is a read-only bit, and is not affected by reset. Writing the SET bit in Register B to a 1 will inhibit any update cycle and then clear the UIP status bit.

Register B Description
Register B contains command bits to control various modes of operations and interrupt enables for the RTC. The bits in this register are defined as follows:

Bit	Description	Abbr
0	Daylight Savings Enable	DSE
1	24/12-Hour Mode	24/12
2	Data Mode (Binary or BCD)	DM
3	Reserved	
4	Update-End Interrupt Enable	UIE
5	Alarm Interrupt Enable	AIE
6	Periodic Interrupt Enable	PIE
7	Set Command	SET

Bit 0 DSE - Daylight Savings Enable: A read/write bit which allows the program to enable two special updates (when DSE is 1). On the last Sunday in April, the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October, when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a 0. DSE is not changed by any internal operations or reset.

Bit 1 24/12 - 24/12-Hour Mode: This control bit establishes the format of the hours bytes as either the 24-Hour Mode (1) or the 12-Hour Mode (0). This is a read/write bit, which is affected only by software.

Bit 2 DM - Data Mode: This bit indicates whether time and calendar updates are to use a binary or a BCD format. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or reset. A 1 in DM specifies binary data, while a 0 specifies BCD data.

Bit 3 Reserved: This bit is unused in this version of the RTC.

Bit 4 UIE - Update-End Interrupt Enable: A read/write bit which enables the update-end flag (UF) bit in Register C to assert an -RTCIRQ. The RSTDRV pin being asserted or the SET bit going high clears the UIE bit.

Bit 5 AIE - Alarm Interrupt Enable: A read/write bit which, when set to a 1, permits the alarm flag (AF) bit in Register C to assert an -RTCIRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code of 11XXXXXXb). When the AIE bit is a 0, the AF bit does not initiate an –RTCIRQ signal. The RSTDRV pin clears AIE to 0. The internal functions do not affect the AIE bit.

Bit 6 PIE - Periodic Interrupt Enable: A read/write bit which allows the periodic interrupt flag (PF) bit in Register C to cause the -RTCIRQ pin to be driven low. A program writes a 1 to the PIE bit in order to receive periodic interrupts at the rate specified by RS3-RS0 in Register A. A 0 in PIE blocks –RTCIRQ from being initiated by a periodic interrupt, but the periodic flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal functions but is cleared to 0 by a reset.

Bit 7 SET - Set Command: When the SET bit is a 0, the update cycle functions normally by advancing the counts once-per-second. When the SET bit is written to a 1, any update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. SET is a read/write bit which is not modified by reset or internal functions.

Register C Description
Register C contains status information about interrupts and internal operation of the real-time clock. The bits in this register are defined as follows:

Bit	Description	Abbr
0	Reserved, Read as 0	
1	Reserved, Read as 0	
2	Reserved, Read as 0	
3	Reserved, Read as 0	
4	Update-Ended Flag	UF
5	Alarm Interrupt Flag	AF
6	Periodic Interrupt Flag	PF
7	–RTCIRQ Pending Flag	IRQF

Bits 0-3 Reserved: These bits are read as 0s and cannot be written.

Bit 4 UF - Update-Ended Interrupt Flag: This bit is set after each update cycle. When the UIE bit is a 1, the 1 in UF causes the IRQF bit to be a 1, asserting -RTCIRQ. UF is cleared by a Register C read or a reset.

Bit 5 AF - Alarm Interrupt Flag: A 1 indicates that the current time has matched the alarm time. A 1 also causes the -RTCIRQ pin to go low, and a 1 to appear in the IRQF bit when the AIE bit also is a 1. A reset or a read of Register C clears AF.

Bit 6 PF - Periodic Interrupt Flag: This is a read-only bit which is set to a 1 when a particular edge is detected on the selected tap of the divider chain. The RS3-RS0 bits establish the periodic rate. PF is set to a 1 independent of the state of the PIE bit. PF being a 1 initiates an -RTCIRQ signal and sets the IRQF bit when PIE is also a 1. The PF bit is cleared by a reset or a software read of Register C.

Bit 7 IRQF - Interrupt Request Flag: This bit is set to a 1 when one or more of the following are true:

PF = PIE = 1
AF = AIE = 1
UF = UIE = 1
The logic can be expressed in equation form as:

IRQF = PF • PIE + AF • AIE + UF • UIE

Any time the IRQF bit is a 1, the -RTCIRQ pin is asserted. All flag bits are cleared after Register C is read by the program or when the RSTDRV pin is asserted.

Register D Description
Register D contains a bit that indicates the status of the on-chip standby RAM. The contents of the registers are described as the following:

Bit	Description	Abbr
0	Not Used, Read as 0	
1	Not Used, Read as 0	
2	Not Used, Read as 0	
3	Not Used, Read as 0	
4	Not Used, Read as 0	
5	Not Used, Read as 0	
6	Not Used, Read as 0	
7	Valid RAM Data and Time	VRT

Bits 0-6 Reserved: These bits cannot be written and are always read as 0s.

Bit 7 VRT - Valid RAM Data and Time: It indicates the condition of the contents of the RAM, provided the power-sense (PS) pin is satisfactorily connected. A 0 appears in the VRT bit when the PS pin is low. The processor program can set the VRT bit when the time and calendar are initialized to indicate that the RAM and time are valid. The VRT is a read-only bit which is not modified by the RSTDRV pin. The VRT bit can only be set by reading Register D.

RTC CMOS STANDBY RAM DESCRIPTION
In addition to the 50 dedicated general purpose RAM bytes, the RTC provides an additional 128 bytes of battery-backed RAM for general purpose uses. They can be used by the system BIOS or user program, and are available during the RTC update cycle. They are mapped as two banks of 64 bytes each residing in the 64-127 index address range. Access to these banks is controlled by setting the bit 5, RAMEN, in the KBDCTL Register.

GENERAL OPERATIONAL NOTES
Set Operation
Before initializing the internal registers, the SET bit in Register B should be set to a 1 to prevent time/calendar updates from occurring. The program initializes the ten locations in the selected format (binary or BCD), then indicates the format in the Data Mode (DM) bit of Register B. All ten time, calendar, and alarm bytes must use the same Data Mode, either binary or BCD. The SET bit may now be cleared to allow updates. Once initialized, the real-time clock makes all updates in the selected Data Mode. The Data Mode cannot be changed without re-initializing the ten data bytes.

24/12-Hour Mode
The 24/12 bit in Register B establishes whether the hour locations represent 0-11 or 0-23. The 24/12 bit cannot be changed without re-initializing the hour locations. When the 12-Hour Mode is selected, the high-order bit of the hours byte represents PM when it is a 1.

Update Operation
The time, calendar, and alarm bytes are not always accessible by the processor program. Once-per-second the ten bytes are switched to the update logic to be advanced by one second and to check for an alarm condition. If any of the ten bytes are read at this time, the data outputs are undefined. The update lockout time is 1948 µs for the 32.768 kHz time base. The update cycle section shows how to accommodate the update cycle in the processor program.

Alarm Operation
The three alarm bytes may be used in two ways. First, when the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second usage is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any byte from 0C0h-0FFh. An alarm interrupt each hour is created with a "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

Interrupts
The RTC plus RAM includes three separate, fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at rates from one-per-second to one-a-day. The periodic interrupt may be selected for rates from one-half second to 30.517 µs. The update-ended interrupt may be used to indicate to the program that an update cycle is completed.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in Register B enable the three interrupts. Writing a 1 to a interrupt enable bit permits that interrupt to be initiated when the event occurs. A 0 in the interrupt enable bit prohibits the –RTCIRQ pin from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enabled, the –RTCIRQ pin is immediately activated, though the interrupt initiating the event may have occurred much earlier. Thus, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts. The flags are cleared by a read of Register C.

When an interrupt event occurs, a flag bit is set to a 1 in Register C. Each of the three interrupt sources have separate flag bits in Register C, which are set independently of the state of the corresponding enable bits in Register B. The flag bit may be used with or without enabling the corresponding enable bits.

Divider Control
The divider control bits are fixed for only 32.768 kHz operation. The divider chain may be held reset, which allows precision setting of the time. When the divider is changed from reset to an operating time base, the first update cycle is one-half second later. The divider control bits are also used to facilitate testing the VL82C316.

Periodic Interrupt Selection
The periodic interrupt allows the –RTCIRQ pin to be triggered from once every 500 ms to once every 30.517 µs. The periodic interrupt is separate from the alarm interrupt which may be output from once-per-second to once-per-day.

Update Cycle
The RTC executes an update cycle one-per-second, assuming one of the proper time bases is in place, the DV2-DV0 divider is not clear, and the SET bit in Register B is clear. The SET bit in the 1 state permits the program to initialize the time and calendar bytes by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the seconds byte, check for overflow, increment the minutes byte when appropriate and so

forth through to the year of the century byte. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code (11XXXXXX) is present in all three positions.

With a 32.768 kHz time base, the update cycle takes 1984 µs, during which the time, calendar, and alarm bytes are not accessible by the processor program. The VL82C316 protects the program from reading transitional data. This protection is provided by switching the time, calendar, and alarm portion of the RAM off the microprocessor bus during the entire update cycle. If the processor reads these RAM locations before the update is complete, the output will be undefined. The update-in-progress (UIP) status bit is set during the interval.

A program which randomly accesses the time and date information finds data unavailable statistically once every 4032 attempts. Three methods of accommodating non-availability during an update cycle are useable by the program. In discussing the three methods, it is assumed that at random points user programs are able to call a subroutine to obtain the time of day.

The first method of avoiding the update cycle uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999 ms are available to read valid time and date information. Before leaving the interrupt service routine, the IRQF bit in Register C should be cleared.

The second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress or not. The UIP bit will pulse once-per-second. Statistically, the UIP bit will indicate that time and date information is unavailable once every 2032 attempts. After the UIP bit goes high, the update cycle begins 244 µs later. Therefore, if a low is read on the UIP bit, the user has at least 244 µs before the time/calendar data will be changed. If a 1 is read in the UIP bit, the time/calendar data may not be valid. The user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C.

To properly setup the internal counters for daylight savings time operation, the user must set the time at least two seconds before the roll-over will occur. Likewise, the time must be set at least two seconds before the end of the 29th or 30th day of the month.

POWER-DOWN MODE

The passive components that are critical for low-power operation are shown in Figure 23.

The –RESET input is used to control the Power-Down Mode of the VL82C316.

When –RESET is pulled low, the RTC enters the Power-Down Mode. In this mode, all outputs are three-stated and read or write operations are inhibited. Any operation in progress (address entered but data not yet accessed) will be terminated and must restart from the beginning of the bus cycle for proper operation. A write operation in progress will be completed if the write strobe has been low for a specificed minimum time. Any write operation stopped prior to the minimum write strobe setup time will not have guaranteed results, since the data path is not double-buffered.

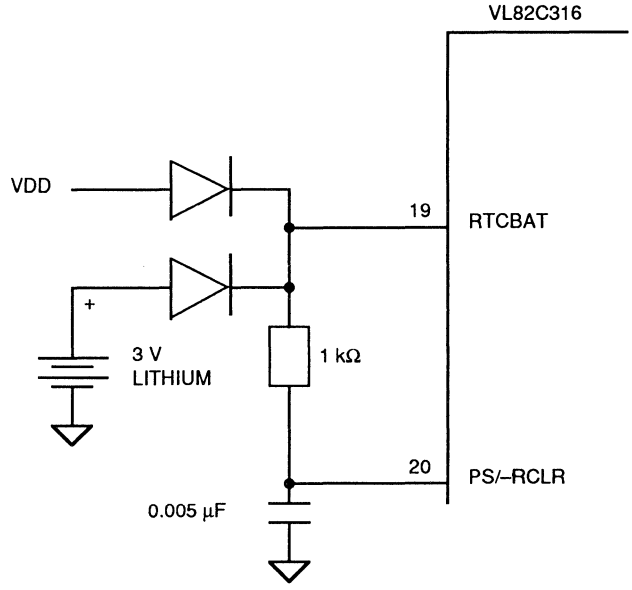
Figure 24 is the bus controller state-diagram that will be implemented in the RTC.

The Power Sense (PS) signal is used to reset the state of the valid RAM and time (VRT) bit. This input must be asserted after power is applied to the RTC to set the state of the VRT bit properly.

RTC ADDRESS SPACE CONTROL

The default I/O address space for the real time clock is 70h and 71h. Some system designers may prefer to use a different real-time clock module or a second one in a system. The register pair, described in Tables 35 and 36, allows the VL82C316's RTC to be remapped anywhere in the standard 64K I/O space.

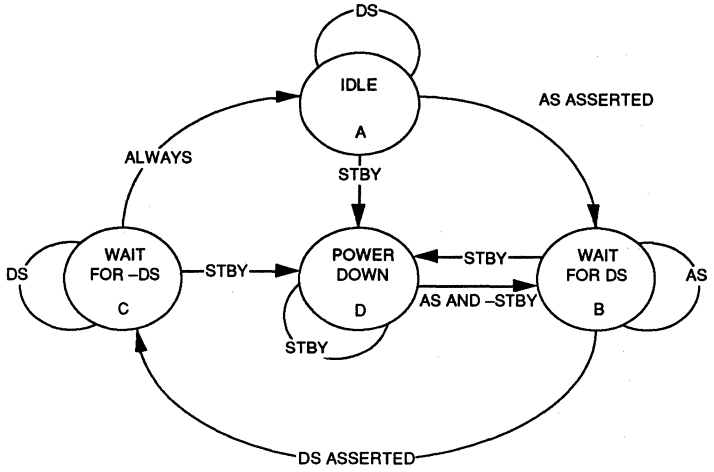
FIGURE 23. RTC BATTERY CONNECTION



–RTCIRQ OPERATION

The –RTCIRQ pin provides compatible internal RTC operation, external RTC operation, or both. –RTCIRQ is an open drain I/O pin requiring an external pull-up. When the internal RTC is enabled via the RENA bit in the RTCLSB Register, the internal RTC interrupt signal drives the –RTCIRQ pin low. Internally this signal is inverted to produce the required active high input to the IRQ8 pin of the internal 83C59A interrupt controller. When not being driven active, –RTCIRQ is three-stated. This allows connection of an external RTC for simultaneous operation with the internal RTC. The interrupt signals are effectively wire ORed by connecting the external RTC's interrupt signal to the –RTCIRQ pin. The –RTCIRQ logic is powered from the RTCBAT supply.

FIGURE 24. REAL-TIME CLOCK STATES



Notes: 1. STBY is defined as –STBY or –RESET.

2. Once a write operation is started, it will not be interrupted until completed. Read operations are immediately terminated by Standby Mode.

TABLE 35. RTCLSB CONFIGURATION REGISTER (READ/WRITE)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
RTCLSB (1Bh)	A7	A6	A5	A4	A3	A2	A1	RENA
POR Value	0	1	1	1	0	0	0	0

Bit	Name	Function
7-1	A7-A1	Combined with RTCMSB, these bits determine the address at which the RTC is accessed. Default is 70h.
0	RENA	RTC Enable: If set, when SA15-SA1 match the 15-bit compare value in RTCLSB and RTCMSB, an access to the RTC is generated. If cleared, all accesses to the internal RTC are disabled. Default is 1.

TABLE 36. RTCMSB CONFIGURATION REGISTER (READ/WRITE)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
RTCMSB (1Ch)	A15	A14	A13	A12	A11	A10	A9	A8
POR Value	0	0	0	0	0	0	0	0

Bit	Name	Function
7-0	A15-A8	Combined with RTCLSB, this determines the address at which the RTC is accessed. Default is 00h.

INTERRUPT CONTROLLER

The interrupt controller subsection is made up of two 82C59A megacells with eight interrupt request lines each for a total of 16 interrupts. The two megacells are cascaded internally and four (or two) of the interrupt request inputs are connected to internal circuitry. This allows a total of 11 (or 13) external interrupt requests.

All external interrupt request signals have an internal pull-up resistor to eliminate noise on unconnected request pins.

The following interrupt request signals are different from the standard interrupt request in some way.

IRQ0 This interrupt is connected to the OUT0 of the 82C54 megacell and is not available as an external input.

IRQ1 By default, this interrupt controller megacell input is connected to the interrupt output of the internal keyboard controller megacell. If the external keyboard controller option is used, the external IRQ1 pin is connected to the internal interrupt controller megacell.

IRQ2 IRQ2 is used to cascade the two 82C59 megacells together and is not available as an external input.

IRQ8 Real-Time Clock megacell's interrupt pin drives the IRQ8 input of the interrupt controller and also the –RTCIRQ pin of the VL82C316 in normal operation. An external RTC may be used without requiring that the internal RTC be disabled. An external RTC's interrupt connects to the –RTCIRQ pin effectively wire ORing the internal and external interrupt sources.

A typical interrupt sequence would be as follows. Any unmasked interrupt generates the INTR signal to the CPU. The interrupt controller megacells then respond to the –INTA pulses from the CPU. On the first –INTA cycle, the cascading priority is resolved to determine which of the two 82C59A megacells outputs the interrupt vector onto the data bus. On the second –INTA cycle, the appropriate 82C59A megacell drives the data bus with the correct interrupt vector for the highest priority interrupt.

Because the two megacells are cascaded internally on the VL82C316, they should never be programmed to operate in the Buffered Mode.

INTERRUPT CONTROLLER REGISTERS

The internal registers of the 82C59A megacells are written to in the same way as in the standard part. Table 37 shows the correct addressing for each of the 82C59A registers.

Before normal operation can begin, each 82C59A megacell must follow an initialization sequence. The sequence is started by writing the Initialization Command Word 1 (ICW1). After ICW1 has been written, the 82C59A megacell expects the next writes to follow in the sequence ICW2, ICW3 and ICW4 if it is needed. The Operation Control Words (OCW) can be written at any time after initialization.

In the standard 82C59A megacell ICW3 is optional. But since the two 82C59A's in this chip are cascaded together, they should always be programmed in Cascade Mode and ICW3 will always be needed. Refer to the 82C59A data sheet for more information on programming the 82C59A megacell. Table 38 shows the read operations of the 82C59 registers

When reading at address 20 or A0 hex, the register read will depend on how Operation Control Word 3 was setup prior to the read.

TABLE 37. 82C59A REGISTERS: WRITE OPERATIONS

INT1	INT2	XD4	XD3	Register Function
20h	A0h	1	X	Write ICW1
21h	A1h	X	X	Write ICW2
21h	A1h	X	X	Write ICW3
21h	A1h	X	X	Write ICW4 (if needed)
21h	A1h	X	X	Write OCW1
20h	A0h	0	0	Write OCW2
20h	A0h	0	1	Write OCW3

TABLE 38. 82C59A REGISTERS: READ OPERATIONS

INT1	INT2	Register Function
20h	A0h	Interrupt Req Register, In-Svc Register, or Poll Command
21h	A1h	Interrupt Mask Register

COUNTER/TIMER

The timer subsection consists of one 82C54 counter/timer megacell configured as shown Figure 25. The clocks for each of the three internal counters are tied to the 14.318 MHz oscillator through a divide by 12 counter. The gate inputs of Counters 0 and 1 are tied high to enable those counters at all times. The gate input of Counter 2 is tied to bit 0 of the Port B Register inside the VL82C316.

One of the 82C54 megacell counter outputs is directly available at an external pin. Counter 0's output is connected to the IRQ0 input of Interrupt Controller 1. Counter 1's output goes to the pin OUT1. Finally, Counter 2's output goes to an AND gate which drives the output pin SPKR. The other input on this AND gate is connected to bit 1 of the Port B Register.

COUNTER/TIMER REGISTERS

The internal registers of the 82C54 counter/timer megacell are written to in the same way as in the standard part. Table 39 shows the correct addressing for each of the 82C54 registers.

The write control word at address 43 hex could also be the counter latch command or read back command depending on the values on the data bus. Refer to the 82C54 data sheet for more information on programming the 82C54 megacell.

SYSTEM MANAGEMENT MODE (SMM)

The VL82C316 fully supports the AMD SMM 2.0 Specification while using the latitude allowed in that specification to make the task of writing system BIOS-based power management software much easier than competing solutions. System designers should obtain and reference that specification and the Am386SXLV data sheet, publication #16305, from Advanced Micro Devices. In Am386DXLV implementations via the VL82C3216 Cache Controller and Interface Unit reference the Am386DXLV data sheet, publication #16306.

Note: Cyrix SMM capable 386SX-compatible CPUs are also fully hardware compatible with the VL82C316. A slight BIOS change is required.

FIGURE 25. COUNTER/TIMER BLOCK DIAGRAM

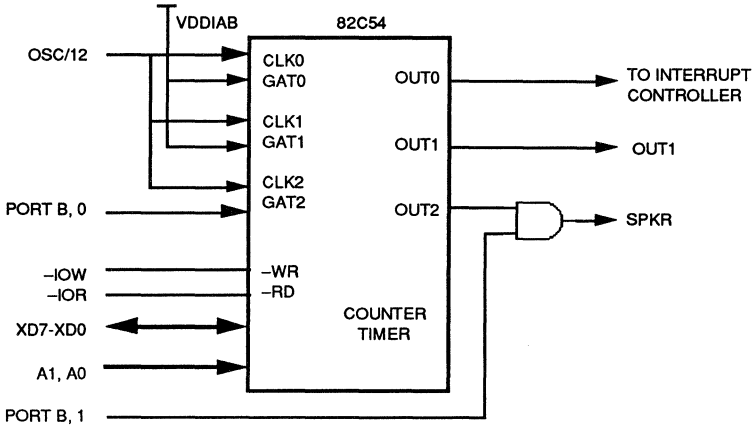


TABLE 39. COUNTER/TIMER REGISTERS

Addr	–IOR	–IOW	Register Function
40h	1	0	Write Initial Count to Counter
40h	0	1	Read Count/Status from Counter 0
41h	1	0	Write Initial Count to Counter 1
41h	0	1	Read Count/Status from Counter 1
42h	1	0	Write Initial Count to Counter 2
42h	0	1	Read Count/Status from Counter 2
43h	1	0	Write Control Word
43h	0	1	No Operation

Via Configuration Register SMMCTL (17h), either 32K, 64K, or 128K of protected memory space may be accessed. SMM space is only available in on-board DRAM. However, ROM-based SMM code may be shadowed. (This feature makes it possible to have SMM code either in BIOS ROM or other ROM at lower addresses as specified in the BASIZ bits, then shadow it for performance.)

TABLE 40. SMMCTL REGISTER - READ ALWAYS/WRITE SPECIAL

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
SMICTL (18h)	SMMEN	SMMBRK	SMMOPT	SMMLOK	SMMACT	BASIZ2	BASIZ1	BASIZ0
POR Value	0	0	1	0	0	0	0	0

Bit	Name	Function
7	SMMEN	SMM Enable: When set to 1, the protected SMM memory space features, as programmed into the other bits of this register, are enabled. SMMEN also affects the definition of pins 31 and 37. When set to 1, pin 31 becomes the –SMI input pin and pin 37 becomes the –SADS input pin. When SMMEN is set to 0, pin 31 becomes the KEYSW input and pin 37 becomes the TURBO input for compatibility with desktop systems. Default = 0, SMM Mode is disabled. **Note:** Never change this bit from 1 to 0 with the SMMLOK bit set and do not allow execution of SMI Cycles before SMMEN is set.
6	SMMBRK	SMM Break: When set to 1, an SMM I/O Break has occurred. If set to 0, a normal SMM has occurred. This bit is the logical OR of the defined bits of registers SMSTSA, SMSTSB, and the SMM bit of the five timer registers. When an I/O Break –SMI occurs, the SMM Handler must read those registers to determine the cause of the break. Reading those registers clears them and the SMMBRK bit in order that it will accurately reflect the status for the next System Management Interrupt.
5	SMMOPT	SMM Memory Options: When SMMOPT is 1, SMMEN is 1, and SMMACT is 1, the normal SMM translation mode is active. In this mode, accesses to protected SMM address space, starting at address 60000h, are translated to the actual on-board memory space set in the BASIZ bits. When set to 0, this translation mode is temporarily suspended. To access the actual DOS memory at 60XXX, either use the new UMOU instruction of the AMD processor or change this bit to a 0 to make the desired access. Make sure this bit is in the same state when exiting the SMI handler as it was when entering the SMI handler. Addresses to the protected SMM space access the actual memory at that space; i.e., accesses in the 60XXX range retrieve the contents of DOS memory and not SMM memory. In this mode, the contents of the SMM space can be directly accessed in the address space programmed into the BASIZ bits. In either case, accesses with the remainder of DOS space below 1MB are never translated. **Note:** This mode must never be used while SMM code is running out of the protected SMM space, otherwise, the system will crash. Also, SMMOPT must be reset to 0 before attempting to exit the SMM, otherwise the CPU restore state function will fail. Default = 1.
4	SMMLOK	SMM Lock: When set to 1, the SMMCTL Register and all read/write I/O Break Control and Status Registers can only be written when –SMI is active. (They are still readable when –SMI is inactive.) When set to 0, the SMMCTL and the I/O Break Registers can be read and written without regard to the state of –SMI. After initial setup, this feature prevents non-SMM code from changing the register settings. Default = 0.
3	SMMACT	SMM Active (read-only): This bit can be accessed to determine if the SMM is active. It indicates the inverted state of the –SMI pin. When the SMM is active, –SMI is low and SMMACT is high. Since an SMM access jumps to the standard reset address, the reset service routine uses this bit to determine if a reset or –SMI has occurred.
2-1	BASIZ2-BASIZ0	SMM Memory Base Size: These bits set the translated physical base address and range for the SMM space as follows (see "Shadow Control Effects During SMM" for additional details): 000 - 32K space from E8000h-EFFFFh (Default) 001 - 32K space from A0000h-A7FFFh 010 - 32K space from B0000h-B7FFFh 011 - 32K space from C8000h-CFFFFh 100 - 64K space from A0000h-AFFFFh 101 - 64K space from B0000h-BFFFFh 110 - 64K space from E0000h-EFFFFh 111 - 128K space from A0000h-BFFFFh

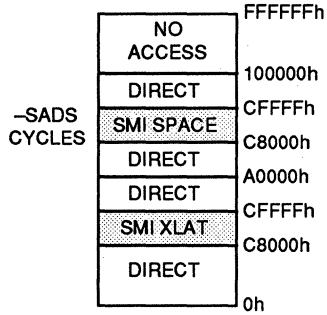
SHADOW CONTROL EFFECTS DURING SMI

During SMM and Normal Mode accesses, the Shadow RAM Control Registers continue to operate normally outside the protected memory space defined by BASIZ2-BASIZ0.

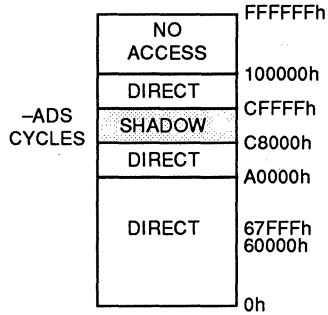
Shadow control acts normally within the the SMM space. In general, the shadow controls that overlap the SMM space should be set to 00b. This results in reads and writes directly to the address range specified in BASIZ2-BASIZ0 to the slot bus. When SMMOPT is 1, the SMM Translation Mode is enabled. Accesses to 60000h (with –SADS active) are directed to the on-board DRAM in the address range programmed into BASIZ2-BASIZ0. Direct accesses to the BASIZ2-BASIZ0 address range are under shadow control. If the shadow bits for the affected address are set to 11, the actual SMM space is accessed. Setting the shadow bits to 00h protects the SMM space from direct accesses while allowing slot bus peripherals at the the same addresses to be accessed via –SADS or –ADS cycles.

When –ADS cycles are active, accesses to the area 60000h are to the standard DOS area. Accesses to the SMM space programmed in BASIZ2-BASIZ0 are under shadow control. The shadow bits should not be set to 11h in order to protect this area. When SMMOPT is 0, –SADS cycle accesses are the same as –ADS cycles as described previously in this section.

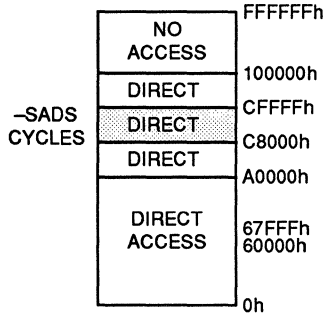
FIGURE 26. EXAMPLES OF SHADOW CONTROL EFFECTS DURING SMI



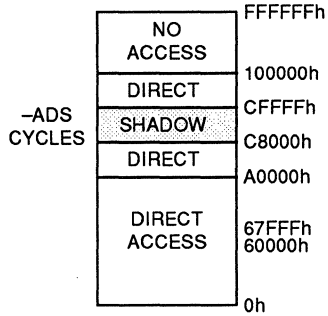
- Accesses from 60000h to 67FFFh are translated to the SMI space in the 640K-1M range as specified in BASIZ (C8000h-CFFFFh).
- Direct R/W accesses to SMI space are allowed without regard to Shadow Registers.



- Accesses from 60000h to 67FFFh are not translated. DOS space in that range is accessed.
- Accesses to the SMI space specified in BASIZ (C8000h-CFFFFh) are directed as programmed in Shadow Register CAXS7-CAXS4. In order to protect SMI space, do not program those Shadow Register bits to 1111 or 0101.



- Accesses from 60000h to 67FFFh are not translated. DOS space in that range is accessed. This mode allows the SMI software to access the DOS space in this region if required. Don't set bit 5 of the SMICTL Register to 0 if running code from protected SMM space.
- Direct R/W accesses to SMI space are allowed without regard to Shadow Registers.



- Accesses from 60000h to 67FFFh are not translated. DOS space in that range is accessed.
- Accesses to the SMI space specified in BASIZ (C8000h-CFFFFh) are directed as programmed in Shadow Register CAXS7-CAXS4. In order to protect SMI space, do not program those Shadow Register bits to 1111 or 0101.

SMM IO BREAK FUNCTIONS

Please reference Advanced Micro Devices document "Am386DXLV and Am386SXLV Technical Reference Manual". Also reference the Am386SXLV data sheet, publication #16305.

In order to use this function, the –IIBEN pin on the Am386SXLV or Am386DXLV must be grounded. Also the SMMCTL Register of the VL82C316 must be configured. Bit 7 must be set to a 1, otherwise the settings of the registers described in this section will have no effect.

The VL82C316 can detect accesses to a variety of pre-set and programmable I/O ranges and generate an SMM in response. Some of these ranges are provided to allow firmware to detect attempts to access powered down peripherals. The SMM code can then power up the peripheral, perform any required initialization sequences, then restart code execution with the instruction that originally generated the SMM IO Break.

Other I/O Break ranges are also included such as for keyboard controller accesses, 82C37A DMA controllers writes, 82C59A interrupt controller writes, or 82C54 counter/timer writes. These options provide the BIOS power management software the flexibility to monitor accesses to these internal system resources, if required.

Five timers are also provided to allow periods of inactivity to be detected. These allow the power management firmware to power down peripherals not currently in use.

Several sets of registers are provided. The first set provides individual enables for each IO Break range or ranges. These are described in the "IO Break Mask Register" descriptions. Note that whether 10- or 16-bit decodes are performed on the hardwired or programmable ranges specified in the IO Break Mask Registers depends on the setting of the 10/16IO bit (bit 1) in the MISCSET Register.

Note: IO Break handler firmware must not allow the instruction that generated the Break to re-execute on exiting the handler unless its respective mask bit has been reset.

IO Break Mask Registers

All IO Break decodes specified in the IO Break Mask Register descriptions (Tables 41 and 42) may be 10- or 16-bit. This is determined by the setting of bit 1 (10/16IO) in the MISCSET Register. SMMSKA and SMMSKB are always read/write when the SMM is active. However, they are read-only when the SMM is inactive if the bit SMMLOK is set to 1 in SMMCTL Register.

TABLE 41. SMMSKA CONFIGURATION REGISTER (READ/WRITE SPECIAL)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
SMMSKA (80h)	R	PIO2MSK	PIO1MSK	HDCMSK	FDCMSK	LPT1MSK	COM2MSK	COM1MSK
POR Value	X	0	0	0	0	0	0	0

Bit	Name	Function
7	R	Reserved: This bit is currently undefined. For compatibility with future versions of this product, this register should always be written such that the value of this is bit is not altered.
6	PIO2MSK	Programmable IO space #2: When set to a 1, I/O reads and writes to the Programmable I/O space #2 base address and range programmed in the PIO2HI and PIO2LO Registers generates an –SMI. **Note:** Be sure to program the desired values into PIO2HI AND PIO2LO before setting this bit to a 1.
5	PIO1MSK	Programmable IO space #1: When set to a 1, I/O reads and writes to the Programmable IO space #1 base address and range programmed in the PIO1HI and PIO1LO Registers generates an –SMI. **Note:** Be sure to program the desired values into PIO1HI AND PIO1LO before setting this bit to a 1.
4	HDCMSK	Hard Disk: When set to a 1, I/O reads and writes to the primary hard disk controller range 1F0h to 1F7h and 3F6h generates an –SMI.
3	FDCMSK	Floppy Disk: When set to a 1, I/O reads and writes to the primary floppy disk controller range 3F0h to 3F5h generates an –SMI.
2	LPT1MSK	Line Printer Port #1: When set to a 1, I/O reads and writes to the the line printer port #1 range 378h to 37Ah generates an –SMI.
1	COM2MSK	COM 2 Port: When set to a 1, I/O reads and writes to the COM 2 Port range 2F8h to 2FFh generates an –SMI.
0	COM1MSK	COM 1 Port: When set to a 1, I/O reads and writes to the COM 1 Port range 3F8h to 3FFh generates an –SMI.

TABLE 42. SMMSKB CONFIGURATION REGISTER (READ/WRITE SPECIAL)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
SMMSKB (81h)	KBRMSK	KBWMSK	CMSMSK	DMA2MSK	DMA1MSK	INT2MSK	INT1MSK	CTMMSK
POR Value	0	0	0	0	0	0	0	0

Bit	Name	Function
7	KBRMSK	Keyboard Controller Reads: When set to a 1, I/O reads to the keyboard controller addresses 60h, 61h, and 64h generates an –SMI.
6	KBWMSK	Keyboard Controller Writes: When set to a 1, I/O writes to the keyboard controller addresses 60h, 61h, and 64h generates an –SMI.
5	CMSMSK	CMOS Index Registers: When set to a 1, I/O writes to the CMOS Index Registers at address 70h generates an –SMI.
4	DMA2MSK	DMA Controller #2: When set to a 1, I/O writes to the 82C37A DMA Controller #2 Registers at even addresses in the range C0h to DEh generates an –SMI.
3	DMA1MSK	DMA Controller #1: When set to a 1, I/O writes to the 82C37A DMA Controller #1 Registers range 00h to 0Fh generates an –SMI.
2	INT2MSK	Interrupt Controller #2: When set to a 1, I/O writes to the 82C59A Interrupt Controller #2 Registers range 20h to 21h generates an –SMI.
1	INT1MSK	Interrupt Controller #1: When set to a 1, I/O writes to the 82C59A Interrupt Controller #1 Registers range A0h to A1h generates an –SMI.
0	CTMMSK	Counter/Timer: When set to a 1, I/O writes to the 82C54 Counter/Timer Registers range 40h to 43h generates an –SMI.

SMI IO Break Status Registers
The following set of registers is used to determine the cause of an –SMI due to the IO Breaks which have been enabled via the IO Break Mask Registers. By polling bit 6 (SMMBRK) in the SMMCTL Register it is possible to tell in advance that at least one of the bits in the SMSTSx Register or the SMM Status bit in one of the five Timer Registers is set. All register bits are set back to 0 by a read of these registers. A read of both Status Registers and the five Timer Registers assures that the SMMBRK bit is cleared.

TABLE 43. SMISTSA CONFIGURATION REGISTER (READ-ONLY)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
SMSTSA (82h)	R	PIO2STS	PIO1STS	HDSTS	FDSTS	LPT1STS	COM2STS	COM1STS
POR Value	X	0	0	0	0	0	0	0

Bit	Name	Function
7	R	Reserved: This bit is currently undefined. For compatibility with future versions of this product, this register should always be written such that the value of this is bit is not altered.
6	PIO2STS	Programmable IO space #2: When set to a 1, an –SMI is due to an enabled IO Break to the Programmable I/O space #2 base address and range programmed in the PIO2HI and PIO2LO Registers.
5	PIO1STS	Programmable IO space #1: When set to a 1, an –SMI is due to an enabled IO Break to the Programmable I/O space #1 base address and range programmed in the PIO2HI and PIO2LO Registers.
4	HDSTS	Hard Disk: When set to a 1, an –SMI is due to an enabled IO Break to the primary hard disk controller range 1F0h to 1F7h and 3F6h.
3	FDSTS	Floppy Disk: When set to a 1, an –SMI is due to an enabled IO Break to the primary floppy disk controller range 3F0h to 3F5h.
2	LPT1STS	Line Printer Port #1: When set to a 1, an –SMI is due to an enabled IO Break to the line printer port #1 range 378h to 37Ah.
1	COM2STS	COM 2 Port: When set to a 1, an –SMI is due to an enabled IO Break to the COM 2 Port range from 2F8h to 2FFh.
0	COM1STS	COM 1 Port: When set to a 1, an –SMI is due to an enabled IO Break to the COM 1 Port range from 3F8h to 3FFh.

Note: In the hard disk and floppy disk (bits 4 and 3) controller decodes there is an I/O address common to both per the PC/AT architecture. An access to this common address will set two bits in the Status Register if both are unmasked.

TABLE 44. SMSTSB CONFIGURATION REGISTER (READ-ONLY)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
SMSTSB (83h)	KBRSTS	KBWSTS	CMSSTS	DMA2STS	DMA1STS	INT2STS	INT1STS	CTMSTS
POR Value	0	0	0	0	0	0	0	0

Bit	Name	Function
7	KBRSTS	Keyboard Controller Reads: When set to a 1, an –SMI is due to an enabled Read IO Break to the keyboard controller range 60h, 61h, and 64h.
6	KBWSTS	Keyboard Controller Writes: When set to a 1, an –SMI is due to an enabled Write IO Break to the keyboard controller range 60h, 61h, and 64h.
5	CMSSTS	CMOS Index Registers: When set to a 1, an –SMI has been generated due to the enabled Write IO Break to the CMOS Index Registers at address 70h.
4	DMA2STS	DMA Controller #2: When set to a 1, an –SMI has been generated due to the enabled Write IO Break to the 82C37A DMA Controller #2 Registers at even addresses in the range from C0h to DEh.
3	DMA1STS	DMA Controller #1: When set to a 1, an –SMI has been generated due to the enabled Write IO Break to the 82C37A DMA Controller #1 Registers in the range from 00h to 0Fh.
2	INT2STS	Interrupt Controller #2: When set to a 1, an –SMI has been generated due to the enabled Write IO Break to the 82C59A Interrupt Controller #2 Registers in the range from 20h to 21h.
1	INT1STS	Interrupt Controller #1: When set to a 1, an –SMI has been generated due to the enabled Write IO Break to the 82C59A Interrupt Controller #1 Registers in the range from A0h to A1h.
0	CTMSTS	Counter/Timer: When set to a 1, an SMI has been generated due to the enabled Write IO Break to the 82C54 Counter/Timer Registers in the range from 40h to 43h.

Programmable IO Break Registers

TABLE 45. PIO2HI CONFIGURATION REGISTER (READ/WRITE SPECIAL)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
PIO2HI (84h)	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8
POR Value	X	X	X	X	X	X	X	X

Bit	Name	Function
7-2	SA15-SA10	Programmed to the SA15-SA10 values for the base address. If the 10/16IO configuration bit (bit 1 of the MISCSET Register) is set to 1, these bits are ignored in the decode process.
1	SA9	Programmed to the SA9 value for the base address.
0	SA8	Programmed to the SA8 value for the base address.

TABLE 46. PIO2LO CONFIGURATION REGISTER (READ/WRITE SPECIAL)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
PIO2LO (85h)	SA7	SA6	SA5	SA4	SA3	SA2	RANGE1	RANGE0
POR Value	X	X	X	X	X	X	X	X

Bit	Name	Function
7-5	SA7-SA5	Programmed to the SA7-SA5 values for the base address.
4	SA4	Programmed to the SA4 value for the base address. It is ignored when the RANGE bits are set for 32 bytes.
3	SA3	Programmed to the SA3 value for the base address. It is ignored when the RANGE bits are set for 16 or 32 bytes.
2	SA2	Programmed to the SA2 value for the base address. It is ignored when the RANGE bits are set for 8, 16, or 32 bytes.
1, 0	RANGE1, RANGE0	The RANGE bits can be coded to provide a 4, 8, 16, or 32 byte space starting at the base address as programmed into the remaining bits of the PIO2HI and PIO2LO Registers. The encoding is as follows: 00 = 4 bytes 01 = 8 bytes and the value of SA2 is a "don't care" 10 = 16 bytes and SA3 and SA2 both beomce "don't cares" 11 = 32 bytes and SA4-SA2 are "don't cares"

TABLE 47. PIO1HI CONFIGURATION REGISTER (READ/WRITE SPECIAL)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
PIO1HI (86h)	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8
POR Value	X	X	X	X	X	X	X	X

Bit	Name	Function
7-2	SA15-SA10	Programmed to the SA15-SA10 values for the base address. If the 10/16IO configuration bit (bit 1 of the MISCSET Register) is set to 1, these bits are ignored in the decode process.
1	SA9	Programmed to the SA9 value for the base address.
0	SA8	Programmed to the SA8 value for the base address.

TABLE 48. PIO1LO CONFIGURATION REGISTER (READ/WRITE SPECIAL)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
PIO1LO (87h)	SA7	SA6	SA5	SA4	SA3	SA2	RANGE1	RANGE0
POR Value	X	X	X	X	X	X	X	X

Bit	Name	Function
7-5	SA7-SA5	Programmed to the SA7-SA5 values for the base address.
4	SA4	Programmed to the SA4 value for the base address. It is ignored when the RANGE bits are set for 32 bytes.
3	SA3	Programmed to the SA3 value for the base address. It is ignored when the RANGE bits are set for 16 or 32 bytes.
2	SA2	Programmed to the SA2 value for the base address. It is ignored when the RANGE bits are set for 8, 16, or 32 bytes.
1, 0	RANGE1, RANGE0	The RANGE bits can be coded to provide a 4, 8, 16, or 32 byte space starting at the base address as programmed into the remaining bits of PIO1HI and PIO1LO. The encoding is as follows: 00 = 4 bytes 01 = 8 bytes and the value of SA2 is a "don't care" 10 = 16 bytes and SA3 and SA2 both become "don't cares" 11 = 32 bytes and SA4-SA2 are "don't cares"

PROGRAMMABLE TIMER BASED –SMI GENERATION

In addition to the SMM IO Breaks listed in Tables 46 and 48 that are based on I/O address range decodes, five programmable timers are also available for –SMI generation. The timers are each four bits in length. A FINE/–COURSE bit selects a range from ~4 sec to ~1 min (FINE/–COURSE = 1) or from ~64 sec to ~16 min (FINE/–COURSE = 0). The 32 kHz RTC oscillator is the clock source for these Timer Registers.

The timer is enabled as soon as the ENABLE bit is set to 1. The 4-bit count is loaded into an internal down counter whose timing is controlled by the state of the FINE/–COURSE bit. Any I/O access to the range covered by the timer will reload the 4-bit timer count and the down count restarts. If the timer reaches terminal count in the absence of I/O for that time period, an –SMI is generated and the –SMI STATUS bit is set. This event automatically disables the timer by resetting the ENABLE bit to 0. A read of the register resets the –SMI STATUS bit to 0. The ENABLE bit must be reset by firmware to continue a new count down sequence.

Note: The count programmed into the TIMER3-TIMER0 bits represents the maximum time-out count. This value never changes unless rewritten with a new value. The actual timer count at any given moment is not externally accessible.

Do not set the ENABLE bits of any timers before the SMMCTL Register is programmed and the SMMEN bit is set.

The IO Break feature described previously is used to prevent accesses to peripherals that are powered off. The timer based –SMI generation feature described in this section provides an indication to the system that a pre-programmed period of inactivity to a powered on peripheral has occurred. In this case, the peripheral might be powered off by the power management firmware after saving critical state information and the associated Break bit for that feature is enabled in the registers previously described.

A typical operational scenario for power management of peripherals using the IO Break feature might be as follows:

Example: Floppy Disk Controller

The power management BIOS firmware initializes the IO Break feature by setting the timer count and the FINE/–COURSE bit in the FDTMR Register. The ENABLE bit is then set to 1 and the timer begins to count down. When no accesses to the floppy disk have occurred for the time programmed, an –SMI is generated and the ENABLE bit is reset to prevent further time-outs.

The SMM handler then enables the floppy disk IO Break by setting the FDCMSK bit in the SMMSKA Register. It can then power down the floppy disk drive and, optionally the floppy disk controller depending on the specific system design. As soon as an I/O access to the primary floppy disk I/O range occurs, an IO Break –SMI occurs. The SMM interrupt handler repowers the floppy disk interface, reinitializes the floppy disk interface, re-enables the Floppy Disk Timer (FDTMR), then exits the SMM. On exit, the CPU reruns the I/O instruction that caused the Break. At this point we have completed a cycle and are back to the same state that started this example. However, this time the firmware has only to set the ENABLE bit of the FDTMR Register since the FINE/–COURSE and TIMER3-TIMER0 bits settings remain correct.

Timer Registers

The IOTMR Register is retriggered by any access to the COM1, COM2, or LPT1 I/O ranges. Since these devices are normally included in a single package they will be powered down together. In systems which have only a single COM port, setting COM2 DISABLE to 1 causes the timer (when enabled) to only retrigger on accesses to COM1 and LPT1.

The other four Timer Registers are retriggered only by single peripheral decodes at the same I/O port address ranges as defined in the I/O Break Mask Registers.

Table 49 gives the format for the five Timer Registers.

TABLE 49. IO BREAK PROGRAMMABLE TIMER REGISTERS (READ/WRITE)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
IOTMR (8Ah)	ENABLE	–SMI STATUS	FINE/ –COARSE	COM2 DISABLE	TIMER3	TIMER2	TIMER1	TIMER0
POR Value	0	0	0	0	1	1	1	1

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
FDTMR (8Bh)	ENABLE	–SMI STATUS	FINE/ –COARSE	R	TIMER3	TIMER2	TIMER1	TIMER0
POR Value	0	0	0	X	1	1	1	1

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
HDTMR (8Ch)	ENABLE	–SMI STATUS	FINE/ –COARSE	R	TIMER3	TIMER2	TIMER1	TIMER0
POR Value	0	0	0	X	1	1	1	1

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
PIO1TMR (8Dh)	ENABLE	–SMI STATUS	FINE/ –COARSE	R	TIMER3	TIMER2	TIMER1	TIMER0
POR Value	0	0	0	X	1	1	1	1

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
PIO2TMR (8Eh)	ENABLE	–SMI STATUS	FINE/ –COARSE	R	TIMER3	TIMER2	TIMER1	TIMER0
POR Value	0	0	0	X	1	1	1	1

SMM SYSTEM ROBUSTNESS FEATURES

For backward compatibility with 286-based systems, a switch from the Protected Mode to the Real Mode is often performed by issuing a CPU Reset command and then executing a Halt instruction. In the 6.72 µs interval between these two events it is possible that a System Management Interrupt (–SMI) may occur. If a CPU Reset is allowed to occur randomly during the execution of the System Management Mode (SMM) code, a system failure is possible. The SMM code is often involved in changing the system's hardware configuration in a variety of ways for the purpose of power managmement. It might be very harmful to the system to allow power-up or -down sequences to be interrupted by a system reset.

Two configuration bits are available to the SMM software to indicated if a CPU Reset is pending, but has not yet occurred and to indicate if the system is currently in a Halt state.

CPU Reset Request Indicator

Bit 5 (RSTREQ) in the REFCTL Register is set whenever a software induced CPU Reset request is active. There are three possible causes of a CPU Reset that are reflected in this bit:

1. Keyboard Controller:
   Write of Reset command to the keyboard controller initiates a CPU Reset sequence. (Note: The VL82C316 emulates the Reset and A20 commands of the keyboard controller internally. therefore, Keyboard Controller CPU Reset cause is correctly trapped regardless of whether the internal or an external keyboard controller is used.
2. Port A:
   Setting bit 0 of IO port 92 initiates a CPU Reset sequence.
3. VLSI Special Feature (VSF):
   A dummy read EFh initiates a CPU Reset sequence.

The occurence of any one of these events causes the RSTREQ bit to go high. It remains high until the occurrence of the CPU Reset event. RSTREQ is cleared by the rising edge of the VL82C316's RESCPU signal. The rising edge of RESCPU clears RSTREQ unconditionally.

A Shutdown detection by the VL82C316 also results in a CPU Reset. However, this reset occurs immediately on Shutdown detection, not after the 6.72 µs delay. It is not reflected in RSTREQ.

Halt Indicator

When the VL82C316 dcodes a Halt condition from the CPU, bit 4 (HLTACT) in the REFCTL Register is set. HLTACT is reset when –RESET is active low, RESCPU is active high, rising edge of NMI, or on detection of an interrupt acknowledge cycle.

Interaction of RSTREQ and SMM

On the falling edge of –SMI, when the SMMEN bit (bit 7) in the SMMCTL Register is set to 1, the VL82C316 checks the state of RSTREQ. If it is high, a CPU Reset event is pending. This event is immediately blocked. On the rising edge of –SMI the VL82C316 regenerates the CPU Reset event from the start. RESCPU will occur 6.72 µs after the rising edge of –SMI. The rising edge of RESCPU clears RSTREQ.

Interaction of HLTACT and SMM

The typical case of a pending CPU Reset is that the last instruction before the occurrence of –SMI was a Halt. –SMI brings the CPU out of the Halt condition. In these cases the SMM routine must return the system to the Halt state after it exits. HLTACT simplifies the SMM code's task of determining that a Halt instruction was the last instruction executed before the –SMI. It is up to the SMM code to ensure that the first instruction executed is a Halt instruction after exiting from the SMM .

TURBO/SLOW CPU CONTROL

It has become standard for fast PC/AT compatibles to provide means to slow operation for older speed sensitive software. This is especially true for graphics intensive entertainment software which may otherwise operate much too fast on a high speed machine. One way this mode may be toggled on and off is by external control of the TURBO input pin. The Slow Mode is activated and the CLK2 divider is in effect when TURBO is low. When TURBO is high, CLK2 runs at the same speed as TCLK2 (only if the VLSI Special Feature TURBO request is also active). This range provides the capability to operate at 8 MHz or under for any actual CPU speed from 12 to 33 MHz.

The TURBO pin is normally connected to the keyboard controller and triggered by the BIOS via detection of a key combination such as Ctrl Alt + / Ctrl Alt -. This input is often externally ANDed with a mechanical TURBO switch on the front panel.

The VL82C316 offers a way to control the CPU speed by software also. A dummy write to F5h returns to full speed operation if the TURBO pin is high. The –VSF bit (bit 7) in the MISCSET Register must be enabled for the software control. The slow operation can be enabled by either pulling the TURBO pin low or by performing a dummy write to I/O port F4h. When the –VSF bit is disabled, CPU speed control is solely under control of the TURBO pin.

Note: The state of TURBO has no impact on the synchronous slot clock frequency. While selection of the Slow Mode does affect the frequency of CLK2, it has no effect on the slot clock. The synchronous slot clock is derived from TCLK2 which is always constant.

PORT B AND NMI LOGIC

The VL82C316 generates the Non-Maskable Interrupt (NMI) output pin for the CPU. NMI is enabled by a write to I/O address 70h with Data Bit 7 low. Once enabled, an NMI can be generated by the –IOCHCK input going low or a parity error. Each of these NMI sources has an enable bit in the Port B Register to allow these inputs to cause an NMI when set high, or ignore the input if the bit is low.

The Port B Register at I/O address 61h is included in the VL82C316 chip. It contains bits to control the speaker output and NMI circuitry. Bits 3-0 are read/write bits and are set low by a reset, while bits 7-4 are read-only. Each bit of the register is defined in Table 50.

TABLE 50. PORT B REGISTER (READ/WRITE)

Port B	D7	D6	D5	D4	D3	D2	D1	D0
61h	PCK	CHAN_CHK	OUT2	REFDET	ENA_IO_CHK	ENA_RAM_PCK	SPK_DAT	TIM2GAT_SPK
POR Value	X	X	X	X	0	0	0	0

Bit	Name	Function
7	PCK	Parity Check: This bit indicates that an on-board RAM parity error has occurred. It can only be set if ENA_RAM_PCK is set 0. PCK should be cleared by writing a 1 to ENA_RAM_PCK.
6	CHAN_CHK	Channel Check: This bit indicates that a peripheral device is reporting an error. It can only be set if ENA_IO_CK is set low. CHAN_CHK should be cleared by writing a 1 to ENA_IO_CK.
5	OUT2	Timer Output bit 2: This bit indicates the current state of the OUT2 signal from the 82C54 megacell.
4	REFDET	Refresh Detect: This bit is tied to a toggle flip-flop which is clocked by REFRESH. It toggles to the opposite state every time a refresh cycle occurs.
3	ENA_IO_CHK	Enable I/O Check: When this bit is set low, it allows an NMI to be generated if the –IOCHCK input is pulled low. Otherwise, the –IOCHCK input is ignored and can not generate an NMI.
2	ENA_RAM_PCK	Enable RAM Parity Check: When this bit is set low, it allows parity errors from on-board RAM memory to cause an NMI. When high, on-board RAM parity errors will not cause an NMI.
1	SPK_DAT	Speaker Data: This bit is gated with the output of Counter 2 from the 82C54 megacell. When this bit is high, it allows the OUT2 frequency to be passed out on the SPKR pin. When low, the SPKR output is forced low.
0	TM2GAT_SPK	Speaker Timer 2 Gate: This bit goes to the Gate 2 input on the 82C54 megacell to enable Counter 2 to produce a speaker frequency.

VLSI SPECIAL FEATURES

The port addresses F8h-FFh are reserved for coprocessor use in an IBM PC/AT. However, only F8h, FAh, FCh, and FEh are actually used. The VLSI Special Feature (VSF) allows the use of unused port addresses in this range as well as special registers in the address range EEh-F7h.

The special registers provided for VLSI Special Feature are Fast A20 (EEh), Fast Reset (EFh), Slow CPU (F4h), Fast CPU (F5h), Configuration Disable (F9h), and Configuration Enable (EBh).

This feature is controlled by MISCSET Register. It is possible to disable the VSF functions mapped in the address range EEh-FFh if they conflict with a specific design implementation.

MISCELLANEOUS CONFIGURATION REGISTER (MISCSET)

The MISCSET Register is used for controlling the VLSI Special Feature (VSF), enabling internal –RC generation with less delay, selecting cache controller speed, and configuring the interrupt pins for glitch-free operation. The bits in the MISCSET Register are described in Table 51.

TABLE 51. MISCSET CONFIGURATION REGISTER (READ/WRITE)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
MISCSET (14h)	–VSF	F1CTL	FASTRC	RDYSMM	CACHEN	RAMDRV	10/16IO	IRQIN
POR Value	0	0	0	1	0	MA9	0	1

Bit	Name	Function
7	–VSF	Enable I/O Space F0h-FFh: This bit is used to enable or disable the VSF options mapped into the coprocessor I/O space between F0h and FFh. When 1, VSF options are disabled. When 0, options are enabled. Default = 0.
6	F1CTL	Coprocessor Software Reset: When 0, a write to I/O port F1h causes generation of an RESNPX signal. When 1, no RESNPX signal is generated by a write to F1h. Default = 0.
5	FASTRC	Fast –RC: For hardware compatibility, the internally generated –RC has delay of 50 µs from the issuance of the command to write data FCh or FEh to port 64h (which generates a low going 6 µs pulse on –RC). This delay can be removed by using the FASTRC bit. If 1, there is no delay introduced. Default = 0.
4	RDYSMM	Ready SMM: When 0 and the SMI Mode is enabled, –READY is active for both –ADS and –SADS initiated cycles. When set to 1 and the SMI Mode is enabled, –READY is only active in response to –ADS cycles. When the SMI Mode is enabled, –SRDY is generated in response to –SADS initiated cycles regardless of the setting of RDYSMI. Default = 1.
3	CACHEN	Cache Enable: When set to 1, the VL82C316 is configured for compatiblity with the VL82C325 Cache Controller. In this mode, the –MISS input is active. When set to 0, the state of the –MISS input has no effect. Default = 0.
2	RAMDRV	DRAM Interface Signal Drive: This bit determines the capacitive load on the MA10-MA0 and –RAMW pins. If 0, the capacitive load limit is 150 pF. The limit is 300 pF if this bit is 1. This bit is software programmable and the value of it is the same as the state of MA9 at power-on reset.
1	10/16IO	10/16 bit I/O Address Decode: When set to 0, full 16-bit address decode is performed. When set to 1, 10-bit I/O decode is performed. Default = 0.
0	IRQIN	Glitch-free Interrupt Request Pin Input: This bit, when set to 1, allows glitch-free input on the IRQ pins. The input to these pins then should be stable for at least 105 ns to generate an interrupt. Default = 1.

DEDICATED INTERNAL CONTROL REGISTERS

The registers and features described next are a fully compatible superset of the VLSI Special Features (VSF). All port decodes are between E8h and FFh as shown in Table 52.

All the internal control registers are accessible in the Master Mode also.

TABLE 52. DEDICATED I/O CONTROL REGISTERS

Port Addr	Function	Port Addr	Function
E8h	PCMCIA Index Register	F4h+	Slow CPU
EBh	PCMCIA Data Port High Byte	F5h+	Fast CPU
EAh	PCMCIA Data Port Low Byte	F8h	Coprocessor
ECh	Config Index Register	F9h+	Config Disable
EDh	Config Data Port	FAh	Coprocessor
EEh*†	Fast A20	FBh+	Config Enable
EFh*†	Fast Reset	FCh	Coprocessor
F0h	Coprocessor Busy Clear	FEh	Coprocessor
F1h	Coprocessor Reset		

* Also can be activated through port 92h for PS/2 compatibility.

† These decodes can be disabled in case of a conflict.

TABLE 53. CONFIGURATION INDEX REGISTER (READ/WRITE)

ECh	D7	D6	D5	D4	D3	D2	D1	D0
Config Index	X	X	X	X	X	X	X	X

The value written to this register is the 8-bit address of the data port which is accessed through the Data Port Register at I/O address EDh. All subsequent Data Port reads and writes access the register at this address until the Index Register is written with a new address. This register is readable. It always returns the last value written to it.

TABLE 54. CONFIGURATION DATA PORT REGISTER (READ/WRITE)

EDh	D7	D6	D5	D4	D3	D2	D1	D0
Config Data	X	X	X	X	X	X	X	X

The registers accessible through I/O address EDh are summarized in the section "Register Summary." They are accessed by writing their addresses to the Index Register at I/O address ECh, then by accessing the Data Port at I/O address EDh.

TABLE 55. FAST A20 REGISTER (READ/WRITE)

EEh (PC/AT)	D7	D6	D5	D4	D3	D2	D1	D0
Fast A20	1	1	1	1	1	1	1	1

92h (PS/2)	D7	D6	D5	D4	D3	D2	D1	D0
Port A	1	1	1	1	1	1	A20	RESET

A dummy read enables A20 and returns a value of FFh. A dummy write disables A20. This method provides a fast, parallel alternative to the standard PC/AT-compatible method of using the keyboard controller to control A20. This signal and the keyboard controller's A20 enable are ORed so that either event controls the A20 address line.

Default on reset is internal A20 control disabled. While disabled, A20 is solely controlled by the keyboard controller for strict PC/AT compatibility.

This register is also controlled via bit 1 of I/O Register 92h (Port A) for PS/2 compatibility. When bit 1 is high, A20 is active. When bit 1 is low, A20 is always 0. This feature is fully integrated with the Fast A20 control achieved through EEh; i.e., a dummy read of EEh followed by a read of bit 1 of port 92h returns a logic 1.

The register at EEh is controlled by bit 7 (–VSF) of the MISCSET Register. –VSF should be 0 to access this register.

TABLE 56. FAST CPU RESET REGISTER (READ-ONLY)

EFh (PC/AT)	D7	D6	D5	D4	D3	D2	D1	D0
Fast Reset	1	1	1	1	1	1	1	1

92h (PS/2)	D7	D6	D5	D4	D3	D2	D1	D0
Port A	1	1	1	1	1	1	A20	RESET

This register provides a fast alternative to the keyboard controller for resetting the CPU. A dummy read of EFh resets the processor and returns a value of FFh. This reset signal is internally ORed with the keyboard controller's reset signal, internal –RC, so that either event invokes a reset. This provides a much faster way for the system to jump between the Real and Protected Modes thus speeding up operation for OS/2. Reset timing is the same as described below for the Port A reset.

A Fast CPU Reset can also be controlled via bit 0 of the I/O Register 92h (Port A) for PS/2 compatibility. When RESET (bit 0) is set to 1, a reset operation is triggered after a minimum 6.72 µs delay. Reset pulses are high for 16 CLK2s. This latch remains set until written again or until the VL82C315 is externally reset.

If the –VSF bit (bit 7) of the MISCSET Register is set to 1, the Fast CPU Reset feature at EFh is disabled. The Fast Reset at 92h is always available as is the reset activated by the BIOS through the keyboard controller.

Note: In order to successfully reset a PC/AT-compatible system, A20 must be gated through and not held low. Otherwise, the reset vector is not fetched and the system hangs. In some existing systems a hot reset without controlling A20 seems to work. However, this is because an error trap occurs which eventually supplies the reset vector to the sys-

TABLE 57. COPROCESSOR CONTROL REGISTERS (WRITE-ONLY)

F0h	D7	D6	D5	D4	D3	D2	D1	D0
Fast Reset	X	X	X	X	X	X	X	X

F1h	D7	D6	D5	D4	D3	D2	D1	D0
Reset Coproc	X	X	X	X	X	X	X	X

A dummy write to I/O port F0h clears the D-Flop which holds –BUSYCPU and PEREQCPU active after an –ERRORNPX signal occurs. This write is normally performed by the interrupt 13 service routine.

A dummy write to I/O port F1h resets the coprocessor. This write results in a positive pulse 40 CLK2 cycles wide and synchronized to CLK2. –READY is held inactive for an additional 50 CLK2 cycles following the falling edge of RESNPX. Bit 6 (F1CTL) of the MISCSET Register must be set to 0, otherwise a write to F1h does not cause a reset. This feature is provided for 387SX compatibility concerns. The 387SX is not put into the same state by reset as is a 286. An FNINT software instruction is also required for initializing the coprocessor.

TABLE 58. CPU SPEED CONTROL REGISTERS (WRITE-ONLY)

F4h	D7	D6	D5	D4	D3	D2	D1	D0
Slow CPU	X	X	X	X	X	X	X	X

F5h	D7	D6	D5	D4	D3	D2	D1	D0
Fast CPU	X	X	X	X	X	X	X	X

A dummy write to port 0F5h causes the CPU to run at normal "fast"speed. A dummy write to port 0F4h invokes the CLK2 divider circuit. This is selected by writing the appropriate code to the MISCSET Register. The programmable range provided allows for 12 to 33 MHz systems to run at or below 8 MHz . Default on reset is "fast" speed.

CPU Speed Control Registers are controlled by the –VSF bit (bit 7) in the MISCSET Register. –VSF should be set to 0 to enable these registers. However, if –VSF is disabled, it is still possible to control the CPU speed with the keyboard controller if allowed by the BIOS.

An I/O read operation on these two addresses returns undefined data.

TABLE 59. CONFIGURATION ENABLE/DISABLE REGISTERS (WRITE-ONLY)

FBh	D7	D6	D5	D4	D3	D2	D1	D0
Config Enable	X	X	X	X	X	X	X	X

F9h	D7	D6	D5	D4	D3	D2	D1	D0
Config Disable	X	X	X	X	X	X	X	X

When enabled and used as described below, the Configuration Registers are protected from unauthorized accesses that might garble the system configuration and either crash the system or change its operational characteristics in an unwanted manner. A dummy write to FBh enables the Configuration Registers. A dummy write to F9h disables the Configuration Registers.

When disabled, the system is locked out from write access to the configuration and control ports from address ECh through EFh. This includes the Dedicated Internal Control Registers, the Memory Card Registers, and the Configuration Indexed Registers.

If the –VSF bit in the MISCSET Register is disabled, the CONFIG ENABLE/DISABLE feature is also disabled. An I/O read operation from these two addresses returns undefined data.

Ports F9h and FBh control access to the Configuration Registers. A dummy write to FBh enables access. A dummy write to F9h disables access.

PARITY GENERATION AND DETECTION CIRCUIT

Parity generation and detection is completely PC/AT compatible. System board memory write cycles generate two parity bits, one for each byte of the 16-bit word bank. These bits are written out coincident with the data write. On a CPU read both system board DRAM bytes feed the parity generator. The resulting two parity bits are compared to the two stored parity bits. In case of a match failure, the NMI interrupt is sent to the CPU. This latter event only occurs after the NMI interrupt is enabled via a write to its enable bit in Port B. On power-on reset the NMI is disabled. This allows the BIOS POST to initialize memory prior to NMI activation. False parity error detection is avoided.

LOCAL BUS PERIPHERAL SUPPORT

The VL82C316 supports peripherals on the local bus, such as VGA controllers for higher performance operation. Such peripherals must generate an –LBA signal input to the VL82C316 as defined below for CPU Mode accesses.

A local device may force the VL82C316 to not respond to any CPU memory or I/O request by making the –LBA signal low before the middle of the first T2/T1P state if enabled (bit 4, LBAEN, in the BUSCTL Register is 1). The local device intercepts the CPU request and completes the cycle as required by the 386SX. When –LBA is driven low with the proper timing, the VL82C316 does not generate –READY. Rather the state of the –READY is monitored by the VL82C316 for a externally generated Ready signal.

CPU ACCESS TO LOCAL BUS DEVICES

CPU access to local bus devices is supported through programmable address regions at which the VL82C316 is deselected during memory accesses, and by the –LBA pin which forcibly deselects the VL82C316 during memory and I/O accesses.

Local Bus Access Input (–LBA)

If the –LBA input is asserted low during any memory or I/O access, the VL82C316 is deselected. To guarantee deselection of the VL82C316, the –LBA input must meet the setup time to the middle of T2 or T1P (pipeline mode). When –LBA is driven low with the proper timing, the VL82C316 does not generate –READY. Rather the –READY output is three-stated and the state of the –READY pin is monitored by the VL82C316 for an externally generated –READY signal.

Programmable Local Bus Memory Regions

One or two regions of the first 16 MB of memory space may be programmed as being local bus address space by the PMR Registers. Each region may be as small as 2 KB or as large as 512 KB. When the VL82C316 detects an access to a programmed local bus memory region it treats the cycle as if the external –LBA pin was asserted, allowing the external local bus device to handle the cycle.

TABLE 60. PMRA1, PMRR1, PMRA2, PMRR2 CONFIGURATION REGISTERS (READ/WRITE)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
PMRA1 (19h)	R	R	AX5	AX4	AX3	AX2	AX1	AX0
PMRR1 (1Ah)	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0
PMRA2 (08h)	R	R	AX5	AX4	AX3	AX2	AX1	AX0
PMRR2 (09h)	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0

PMRAx Bit Definitions

Bit	Name	Function
7, 6	R	Reserved: Always read as 1.
5-0	AX5-AX0	Select the start address and size of the memory region as follows:

AX5	AX4	AX3	AX2	AX1	AX0
0	A23	A22	A21	A20	A19

A23-A19 selects a 512 KB region in the first 16 MB of memory, aligned on a 512 KB boundary.

AX5	AX4	AX3	AX2	AX1	AX0
1	X	A17	A16	A15	A14

A17-A14 selects a 16 MB region in the address range C0000h to FFFFh (768K - 1M) aligned on a 16 MB boundary.

Default: AX5-AX0 = 0
AX7 and AX6 are always read as 1

PMRRx Bit Definitions

7-0	RE7-RE0	Sub Region Enables: These bits enable the region selected by PMRAx for remapping into a local bus peripheral space. The region selected by PMRAx is divided inot eight equally sized continuous sub-regions, each with its own enable, RE7-RE0. RE0 controls the sub-region with the lowest address. Thus for 512 KB regions the sub-region size is 64 KB and for 16 KB regions the sub-region size is 2 KB. Any combination of RE7-RE0 may be set. Operation is as follows: REx = 0: Default mapping is selected (cycle handled by VL82C316 for addresses in this space). REx = 1: Local bus peripheral sub-region mapping is enabled as defined by PMRAx. Programming all 0s for the PMRRx register disables the effect of the corresponding PMRAx Register. Default: RE7-RE0 = 0

DMA and MASTER Mode Local Bus Memory Transfers

The VL82C316 supports DMA and Master Mode cycles between ISA slot bus I/O devices and local bus memory devices. The mechanism is programmed via the PMR Registers. To support DMA transfers between a slot bus device and a local bus device, a PMR Register must be programmed to select a local bus device for the address range in which such transfers are to occur.

Whenever the HLDA input of the VL82C316 is high, –ADS, M/–IO_DK0, W/–R_DK2, D/–C_DK1, –BLE, and –BHE are three-stated (pulled up). The –READY pin is configured as an input.

Then on detection of an active –MEMR or –MEMW signal during a DMA or Master Mode transfer cycle that falls within the range selected by a PMR for local bus accesses, the VL82C316:

- Drives IOCHRDY inactive (low) on the next negative or positive edge of SYSCLK.

- Sets W/–R_DK2 high on memory writes or low on memory reads, sets D/–C_DK1 high, sets M/–IO_DK0 high on memory cycles and low on I/O cycles, and sets –BLE and –BHE according to the decode of SA0 and –SBHE.
- After synchronization with the CPU clock, –ADS is asserted for one T-state. On memory writes, the contents of the SD bus is driven onto the selected portion of the D bus.
- Waits for –READY to be returned by the local bus device. For memory reads, –READY is used to strobe the data returned by the local bus device into a synchronous data register; the output of the data register is placed on the selected portion of the SD bus.
- After synchronization with SYSCLK, IOCHRDY is re-asserted (high) to terminate the cycle, then three-stated on the next SYSCLK edge (either positive or negative).

When the local bus access mechanism is used in DMA transfers, the DMA acknowledge (–DACK) signals, decoded from the M/–IO_DK0, D/–C_DK1, and W/–R_DK2, must be latched externally and enabled when DKEN is active, since these signals hold a valid DMA acknowledge code only for a short time after DKEN goes active, before being multiplexed to select the local bus cycle definition.

If the local bus feature is disabled (bit 4, LBAEN, of the BUSCTL1 Register is cleared), the sequence of events for local bus accesses defined above does not occur. The signals involved retain their normal (non-local bus cycle) function and timing.

Local Bus Watchdog Timer

When the VL82C316 detects an access to a local bus device via the PMR Registers, an internal watchdog timer is activated. If no –READY from the peripheral is detected within 14 to 28 µs from the time-out start, then a time-out occurs, and the VL82C316 generates an internal –READY to terminate the cycle. Note that the watchdog timer does not operate if the –LBA pin is sampled low at the end of T2/T1P (for either CPU or hold acknowledge cycles.)

IN-CIRCUIT TEST LOGIC

The VL82C316 is designed to make system board testing as easy as possible. The –TRI input causes all pins on the VL82C316 go to a high impedance state. This can be used to isolate the VL82C316 so other components in the system can be tested.

The –TRI input can also be used to put the VL82C316 into a special test mode called In-Circuit Test (ICT). The purpose of the ICT Mode is not to test the VL82C316 functionally while it is inserted in a circuit board, but to test that the part that is connected correctly and all the pins can be toggled high and low in a predictable pattern. It uses a multiplexing scheme between inputs and outputs to allow easy access and testing of each pin.

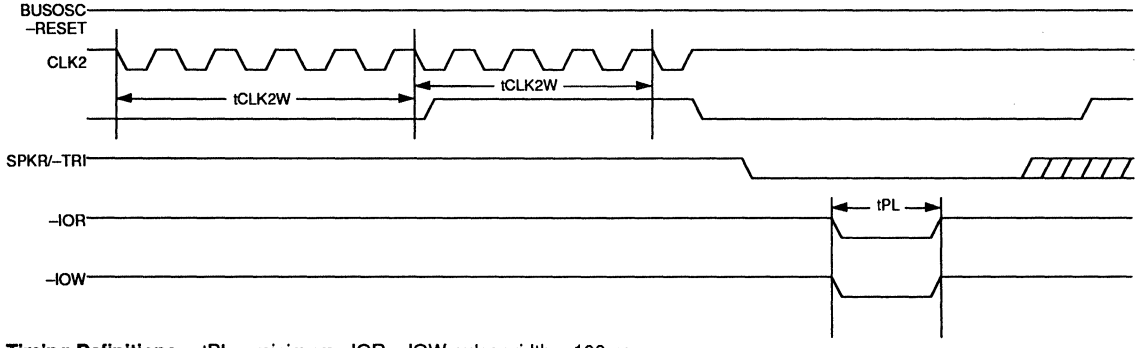
The VL82C316 has a number of internal test modes in order to completely test the functionality of the circuit. The test modes are disabled upon reset. In order to activate the ICT Mode, refer to the test mode timing diagram Figure 27. If –RESET is held low, the SPKR/–TRI pin becomes an input. (Normally, this pin is pulled up by the internal pull-up resistor.) If driven low while –RESET is low, all outputs and I/Os are three-stated. This can be used to isolate the VL82C316 from other board components for debugging. The ICT Mode can then be invoked by toggling –IOR and –IOW together. The SPKR/–TRI pin should then be released (allowed to float) and the –RESET input returned high. The test mode will remain in effect until a reset is performed (–RESET driven low). Note that the BUSOSC and CLK2 input should be left inactive during the test register access, otherwise a reset will occur.

To enter the ICT Mode:

1. Drive –RESET low.
2. Drive SPKR/–TRI low.
3. Invoke ICT Mode by pulsing –IOR and –IOW simultaneously.
4. Release SPKR/–TRI (allow to float).
5. Return –RESET high.

Note: CLK2 must initially be allowed to operate in conjunction with –RESET. This is required in order to initialize internal logic. Once in the ICT Mode, CLK2 and BUSOSC must not be allowed to operate as this will cause a system reset.

FIGURE 27. ICT TEST MODE TIMING WAVEFORM



Timing Definitions: tPL = minimum –IOR, –IOW pulse width = 100 ns
tCLK2W = minimum 25 CLK2s

TABLE 61. PIN ASSIGNMENT FOR IN-CIRCUIT TEST MODE

ICT Input		ICT Output		ICT Input		ICT Output		ICT Input		ICT Output	
Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
OSC	2	T/C	1	DRQ3	199	SYSCLK	193	IRQ7	203	SD2	185
–MEMCS16	3	D0	52	IRQ4	206	–SMEMW	188	IRQ6	204	SD1	186
–IOCS16	4	D1	53	IRQ3	207	AEN	168	IRQ5	205	SD0	187
IRQ10	5	D2	54	–CAS1	115	A5	91	–SMI/KEYSW	31	BUSYCPU	35
IRQ11	6	D3	55	–CAS0	116	A6	89	SA1	166	SD8	177
IRQ12	7	D4	56	–RAMW/–WE0	117	–SRDY	39	PS/–RCLR	20	SD10	175
IRQ15	8	D5	57	–RAS1	118	A3	93	SA0	167	SD11	174
IRQ14	9	D6	58	–RAS0	120	A21	73	–SBHE	198	SD12	173
–MEMR	12	INTR	32	MA0	121	A19	75	SA2	164	SD13	172
–MEMW	13	BALE	10	MA1	122	A18	76	SA3	162	SD14	171
DRQ0	14	PEREQCPU	34	MA2	124	A17	77	SA4	161	SD15	170
DRQ5	15	D7	60	MA3	125	A16	78	SA15	149	PAR0/–OE0*	110
DRQ6	16	D8	61	MA4	126	A15	79	–LBA	97	PAR0/–OE0*	110
DRQ7	17	D9	63	MA5	127	A14	80	SA14	150	LA23	137
–MASTER	18	D10	64	MA6	129	A13	81	SA13	151	LA22	138
PEREQNPX	105	W/–R_DK2	40	MA7	130	A12	83	SA12	152	LA21	139
RESNPX	106	D/–C_DK1	41	MA8	131	A11	84	SA11	153	LA20	140
BUSYNPX	107	D11	65	MA9	132	A10	85	SA10	154	LA19	141
–ERRORNPX	108	D12	66	MA10/–WE1	133	A9	86	SA9	155	LA18	142
CLK2IN	46	M/–IO_DK0	42	–RAS2	135	A8	87	SA8	157	LA17	144
–BLE	44	–BHE	43	–RAS3	136	A7	88	SA7	158	SA19	145
CLK2	48	–ADS	45	–BLKA20	96	PAR1/–OE1*	111	SA6	159	SA18	146
–READY	49	–A23	71	TCLK2	99	PAR1/–OE1*	111	SA5	160	SA17	147
CPUHRQ	50	A1	95	BUSOSC	48	SD9	176	SA16	148	A4	92
CPUHLDA	51	A22	72	–IOCHCK	195	SD7	179	MDAT/TURBORQ	24	NMI	33
–SUSPEND	103	A20	74	IRQ9	202	SD6	180	MCLK	25	–SADS/TURBO	37
RESCPU	36	D14	69	DRQ2	200	SD5	181	KDAT	26	D13	67
–CAS3	112	D15	70	–WS0	197	SD4	183	KCLK/IRQ1	27	–MISS	98
–CAS2	114	A2	94	IOCHRDY	194	RSTDRV	169	SPKR/–TRI	101	DKEN*	30
–IOW	190	–SMEMR	189	DRQ1	201	SD3	184	–SMIIN	26	DKEN*	30
–IOR	191	–REF	192					–SLEEP	109	–ROMCS/–PPICS	29

* These outputs are the OR of two inputs.

SPECIAL VL82C316 CYCLES AND RESET OPTIONS

HALT/SHUTDOWN CYCLES

The VL82C316 detects and responds as described below to Halt and Shutdown operations from 386SX processors. This is also compatible with use in 486-based systems.

The VL82C316 detects a Halt condition from the CPU, bit 4 (HLTACT) in the REFCTL Register is set. HLTACT is reset whend –RESET is active low, RESCPU is active high, rising edge of NMI, or on detection of an interrupt acknowledge cycle. No further action is taken in respone to Halt except to acknowledge it by asserting –READY.

Note: See the section titled "SMM System Robustness Features" on page 90 for information on how the SMM code must use the HLTACT bit.

Shutdown is handled differently. This bus cycle is executed by the CPU in response to a critical internal processing error. The VL82C316 responds by issuing a CPU-only reset for 16 CLK2 cycles. More detail on the CPU-only reset sequence is discussed previously in this document in the section "CPU-Only Reset" on page 22.

Detection of a Halt or Shutdown cycle causes the VL82C316 to activate its –READY signal after a one wait state delay. See Table 62 for Halt/Shutdown detection codes.

ISA CYCLES

When in the CPU Mode, the 82288 megacell is responsible for generating the command (–IOR, –IOW, –MEMR, –MEMW, –SMEMR and –SMEMW) signals, BALE and the timing for when the SA bus will be valid. The VL82C316 samples the inputs –MEMCS16, –IOCS16, –IOCHRDY and –WS0 and determines the length in wait states of each bus cycle.

COPROCESSOR CYCLES

The VL82C316 automatically generates a –READY signal in one wait state during coprocessor read and write cycles.

TABLE 62. HALT/SHUTDOWN DETECTION

D/–C_DK1	W/–R_DK2	–BHE/A1	Mode
0	1	1	Halt
0	1	0	Shutdown

SYSTEM RESET OPTIONS

This section describes all Reset Modes of the VL82C316 based on their activating signal. They have been discussed in other applicable sections of this document and are summarized in one place as an aid to the reader.

–RESET This signal causes all internal state machines to be reset. The Internal Configuration Registers are reset to their default values shown in Table 66. A reset is issued to the CPU and the coprocessor via the RESCPU and RESNPX signals. RSTDRV is generated from –RESET and is synchronized with BUSOSC. The –BUSYCPU signal is active for eight CLK2 cycles before and after the falling edge of the RESCPU signal. This invokes the Self-Test Mode of the 386SX. Systems that desire to use this feature can then read the result of this test in the 386SX's EAX Register and decide what to do based on the result. Otherwise, it can be ignored.

REG_{92} Setting bit 0 of I/O port 92h causes a CPU-only reset after a 6.72 µs delay. RESCPU is activated for 16 CLK2 cycles. See the section "Fast CPU Reset Register" for more details.

REG_{EF} A dummy read of I/O port EFh causes a CPU-only reset after a 6.72 µs delay. RESCPU is activated for 16 CLK2 cycles. VLSI Special Feature must be enabled for this feature to function.

OUT_64 The CPU is reset when I/O port 64h is loaded with the value FCh or FEh. This generates an internal reset signal equivalent to –RC from a keyboard controller. The internal –RC is active after 6.72 µs or about 50 µs delay depending on the value of the FASTRC bit in MISCSET Register. The pulse width of this signal is 16 CLK2 cycles. It generates RESCPU.

OUT_F1 A dummy write to I/O port F1h causes a coprocessor-only reset. RESNPX is activated for 40 CLK2 cycles. Assertion of –READY is delayed for 50 CLK2 cycles after RESNPX is deactivated.

SHUTDOWN Detection of the Shutdown condition causes a CPU-only reset for 16 CLK2 cycles.

REGISTER SUMMARY

SYSTEM CONFIGURATION

The VL82C316 offers hardware configurable options so that a generic BIOS can be used for a system designed with the VL82C316. Table 21 details the mapping. When using the high strap options, be sure to pull-up to the VL82C316 power rail associated with that pin. The correct power rail is noted in parenthesis under the "Pin" column in Table 63.

TABLE 63. CONFIGURATION REGISTER

Pin	Register Name	Register Bit	Bit Name	Functional Description	Default
MA3-MA0 (VDDRB)	RAMMAP	3-0	MEMAP3-MEMAP0	Memory Map Code 3-0 (Refer to Tables 1 and 2)	0000
MA4 (VDDRB)	RAMMAP	4	REMP384	Remap 384K DRAM (A0000-FFFFFh) 0 = Disabled 1 = Enabled	0
MA5 (VDDRB)	RAMSET	5	DRAMWS1	DRAM Wait States 0 = 0 Wait State 1 = 2 Wait State	1
MA6 (VDDRB)	RAMSET	2	–PGMD	Page Mode Enable 0 = Enabled 1 = Disabled	1
MA7, MA8 (VDDRB)	RAMMAP	5, 6	ROMMOV0, ROMMOV1	System and Slot ROM Move (Refer to Table 13)	00
MA9 (VDDRB)	MISCSET	2	RAMDRV	MA10/–WE1, MA9-MA0, –RAMW/–WE0, –RAS3 - –RAS0, –CAS3 - –CAS0, PAR1/–OE1, and PAR0/–OE1 Drive 0 = 150 pF 1 = 300 pF	1
MA10 (VDDRB)	BUSCTL1	7	ROMWID	ROM Width 0 = 8-Bit 1 = 16-Bit	*
PAR0, PAR1 (VDDRB)	ROMDMA	7, 6	ROMWS1, ROMWS0	BIOS ROM Wait State Bits 1 and 0 Determine ROM Wait States: 00 = 3 Wait States 01 = 1 Wait State 10 = 2 Wait States 11 = 3 Wait States	00
DKEN (VDDRA) –RAMW (VDDRB)	CLKCTL	1, 0	SCLKDIV1, SCLKDIV0	Slow Clock Divider Bits 1 and 0 Selects the SYSCLK Frequency: 00 = Clock +2 01 = Clock +4 10 = Clock +6 11 = Clock +8 where Clock is BUSOSC or TCLK2	01
–ROMCS /–PPICS (VDDRA)				ROM Location 0 = ROM on SD Bus 1 = ROM on D Bus	*
–BLKA20 (VDDRA)				System Configuration 0 = Externally Configured 1 = Internal Default	

* ROMWID and ROMLOC must still be externally configured for the desired modes even when –BLKA20 is strapped to select the internal default options.

POWER ON CONFIGURATION NOTES:

1. SCAMP II power-on configuration is set by pull-up/pull-down resistors on 17 pins. Most of these pins are only used for configuration when external configuration is used. Even when internal configuration is used, functions that are setup prior to use may not need configuration resistors. For instance, if the BIOS ROM sets up the RAMMAP, RAMSET, and MISCSET registers prior to making any DRAM accesses, then no resistors will be required on MA0-MA9.
2. The following pins must always have a pull-up or pull-down: –BLKA20, –ROHCS.–PPICS, MA10.
3. The PAR0 and PAR1 pins are also configuration pins. These pins cannot be left floating. If party is used and internal configuration is used, (BLKA20 pulled high), then no resistors are required. If parity is not used pull ups or pull downs are required even if internal configuration if used.

SUMMARY OF CONFIGURATION REGISTERS

Version (00h)

D7-D0 contains a read-only code which indicates that this part is a VLSI Technology, Inc. VL82C316. D7 and D6 contains the code 01. D5-D3 contains the code 101. D2-D0 contains the version number of this chip. D2-D0 will be the only bits in this register that will ever change value. By using this byte, a smart BIOS can compensate for "feature" differences based on the version number. The first version of this chip contains the code 6Ah. Breaking the code pieces reveals it to be "316", Rev 2.

Index Register

The value written to this register is the 8-bit address of the data port which is accessed through the Data Port Register at I/O address EDh. All subsequent data port reads and writes access the register at this address until the Index Register is written with a new address. This register is readable. It always returns the last value written to it. The Index Register is a read/write register.

Data Port Register

Each register accessible through I/O address EDh is functionally described in Table 22. It is accessed first by writing its address to the Index Register at I/O address ECh, then by accessing the Data Port Register at I/O address EDh.

TABLE 64. INDEXED CONFIGURATION REGISTERS MAP

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
ECh (R/W)	Index Port	A7	A6	A5	A4	A3	A2	A1	A0
EDh (R/W)	Data Port	D7	D6	D5	D4	D3	D2	D1	D0
00h (R-O)	VER	0	1	1	0	1	0	1	0
02h (R/W)	SLTPTR	A23	A22	A21	A20	A19	A18	A17	A16
03h (R/W)	RAMMAP	MAP512K	ROMMOV (1 & 0)		REMP384	MEMAP (3-0)			
05h (R/W)	RAMSET	WAKEUP	DELAY	DRAMWS (1 & 0)		–FASTSX	–PGMD	–ENPAR	RASOFF
06h (R/W)	REFCTL	SUSPACT	CPUOFF-SUS	RSTREQ	HLTACT	REFMODE (1 & 0)		REFSPD (1 & 0)	
07h (R/W)	CLKCTL	ENVDSP	CLK2DIV (1 & 0)		FCLKDIV (1 & 0)		BOSCSNS	SCLKDIV (1 & 0)	
08h (R/W)	PMRA1	R	R	AX5	AX4	AX3	AX2	AX1	AX0
09h (R/W)	PMRR1	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0
0Ah (R/W)	MCDCTL	–ENMCSPD	R	R	R	MCPGEN (3-0)			
0Eh (R/W)	ABAXS	B8000 Access		B0000 Access		A8000 Access		A0000 Access	
0Fh (R/W)	CAXS	CC000 Access		C8000 Access		C4000 Access		C0000 Access	
10h (R/W)	DAXS	DC000 Access		D8000 Access		D4000 Access		D0000 Access	
11h (R/W)	FEAXS	F8000 Access		F0000 Access		E8000 Access		E0000 Access	
13h (R/W)	SLPCTL	SLP	DIVCLK (3-0)				SLPSTS	R	ENSYCK
14h (R/W)	MISCSET	–VSF	F1CTL	FASTRC	RDYSMM	CACHEN	RAMDRV	10/16IO	IRQIN
15h (R/W)	ROMDMA	ROMWS (1 & 0)		DMAWS8 (1 & 0)		DMAWS16 (1 & 0)		DMACLK	MEMTM
16h (R/W)++	BUSCTL1	ROMWID	R	DSKTMG	LBAEN	R	CMDLY2	R	CMDLY1
17h (R/W)++	BUSCTL2	–CLK2OFF	–DMAPWR	R	R	R	16WS	R	8WS
18h (R/WS)	SMICTL	SMMEN	SMMBRK	SMMOPT	SMMLOK	SMMACT	BASIZ (2-0)		
19h (R/W)	PMRA2	R	R	AX5	AX4	AX3	AX2	AX1	AX0
1Ah (R/W)	PMRR2	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0
1Bh (R/W)	RTCLSB	A7	A6	A5	A4	A3	A2	A1	RENA
1Ch (R/W)	RTCMSB	A15	A14	A13	A12	A11	A10	A9	A8
1Dh (R/W)	KBDCTL	–KISLP	–HSLP	RAMEN	KBDEN	SLPCTL	PRV	MODE	–SLP
80h (R/WS)	SMMSKA	R	PIO2MSK	PIO1MSK	HDMSK	FDMSK	LPT1MSK	CM2MSK	CM1MSK
81h (R/WS)	SMMSKB	KBMSK	KBWMSK	CMSMSK	DMA2MSK	DMA1MSK	INT2MSK	INT1MSK	CTMMSK
82h (R-O)	SMSTSA	R	PIO2STS	PIO1STS	HDSTS	FDSTS	LPT1STS	CM2STS	CM1STS
83h (R-O)	SMSTSB	KBSTS	KBWSTS	CMSSTS	DMA2STS	DMA1STS	INT2STS	INT1STS	CTMSTS
84h (R/WS)	PIO2HI	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8
85h (R/WS)	PIO2LO	SA7	SA6	SA5	SA4	SA3	SA2	RANGE (1 & 0)	
86h (R/WS)	PIO1HI	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8
87h (R/WS)	PIO1LO	SA7	SA6	SA5	SA4	SA3	SA2	RANGE (1 & 0)	
8Ah (R/W)	IOTMR	ENABLE	SMI STAT	F/–C	C2 DISBL	TIMER (3-0)			
8Bh (R/W)	FDTMR	ENABLE	SMI STAT	F/–C	R	TIMER (3-0)			
8Ch (R/W)	HDTMR	ENABLE	SMI STAT	F/–C	R	TIMER (3-0)			
8Dh (R/W)	PIO1TMR	ENABLE	SMI STAT	F/–C	R	TIMER (3-0)			
8Eh (R/W)	PIO2TMR	ENABLE	SMI STAT	F/–C	R	TIMER (3-0)			

Notes: R Indicates reserved bits. These bits are currently undefined. For compatibility with future versions of this product, registers should always be written such that the value of these bits is not altered.

R/WS Indicates read any mode, write special in SMM Mode.

++ ROMWID is a read-only bit. This is set by jumper on power-up. Refer to Table 63.

TABLE 65. INDEXED CONFIGURATION REGISTERS RESET VALUES

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
ECh (R/W)	Index Port	A7	A6	A5	A4	A3	A2	A1	A0
EDh (R/W)	Data Port	D7	D6	D5	D4	D3	D2	D1	D0
00h (R-O)	VER	0	1	1	0	1	0	1	0
02h (R/W)	SLTPTR	1	1	1	1	1	1	1	1
03h (R/W)	RAMMAP	0	MA8	MA7	MA4	MA3	MA2	MA1	MA0
05h (R/W)	RAMSET	0	0	MA5	0	0	MA6	0	0
06h (R/W)	REFCTL	0	0	0	0	0	0	0	0
07h (R/W)	CLKCTL	0	0	0	1	0	Note 1	DKEN	–RAMW
08h (R/W)	PMRA1			0	0	0	0	0	0
09h (R/W)	PMRR1	0	0	0	0	0	0	0	0
0Ah (R/W)	MCDCTL	1	X	X	X	0	0	0	0
0Eh (R/W)	ABAXS	0	0	0	0	0	0	0	0
0Fh (R/W)	CAXS	0	0	0	0	0	0	0	0
10h (R/W)	DAXS	0	0	0	0	0	0	0	0
11h (R/W)	FEAXS	0	0	0	0	0	0	0	0
13h (R/W)	SLPCTL	0	0	0	0	0	–SLEEP	X	1
14h (R/W)	MISCSET	0	0	0	1	0	MA9	0	1
15h (R/W)	ROMDMA	PAR1	PAR0	1	0	1	0	0	0
16h (R/W)++	BUSCTL1	MA10		1	0		0		0
17h (R/W)++	BUSCTL2	1	1	X	X		0		0
18h (R/WS)	SMICTL	0	0	1	0	Note 2	0	0	0
19h (R/W)	PMRA2			0	0	0	0	0	0
1Ah (R/W)	PMRR2	0	0	1	0	0	0	0	0
1Bh (R/W)	RTCLSB	0	1	1	1	0	0	0	0
1Ch (R/W)	RTCMSB	0	0	1	0	0	0	0	0
1Dh (R/W)	KBDCTL	1	0	0	1	0	0	1	1
80h (R/WS)	SMIMSKA	X	0	0	0	0	0	0	0
81h (R/WS)	SMIMSKB	0	0	0	0	0	0	0	0
82h (R-O)	SMISTSA	X	0	0	0	0	0	0	0
83h (R-O)	SMISTSB	0	0	0	0	0	0	0	0
84h (R/WS)	PIO2HI	X	X	X	X	X	X	X	X
85h (R/WS)	PIO2LO	X	X	X	X	X	X	X	X
86h (R/WS)	PIO1HI	X	X	X	X	X	X	X	X
87h (R/WS)	PIO1LO	X	X	X	X	X	X	X	X
8Ah (R/W)	IOTMR	0	0	0	0	1	1	1	1
8Bh (R/W)	FDTMR	0	0	0		1	1	1	1
8Ch (R/W)	HDTMR	0	0	0		1	1	1	1
8Dh (R/W)	PIO1TMR	0	0	0		1	1	1	1
8Eh (R/W)	PIO2TMR	0	0	0		1	1	1	1

Notes: 1. The default value of this bit is dependent on the external clock BUSOSC. If there is an external clock connected to BUSOSC pin, the reset value is 0, otherwise the status of BUSOSC pin is reflected in this bit.

2. This bit reflects the state of the –SMI pin.

3. In general, its indicated by "X" have no currently defined function and no guaranteed value. For compatibility with future versions of this product, registers should always be written such that the value of these bits is not altered. Registers 84h-87h are an exception relative to the others in this category. They have a defined function but no power-on reset default. They must be programmed to valid values before use.

TABLE 66. DEDICATED I/O CONTROL REGISTERS

Port Address	Name	Access	Function
E8h	PCMCIA Index Register	R/W	Contains the address of one of the PCMCIA 1.0 Memory Card Mapping Registers.
EAh	PCMCIA Upper Data Port	R/W	Contains the upper byte of data written to the PCMCIA Data Port selected by the PCMCIA Index Register.
EBh	PCMCIA Lower Data Port	R/W	Contains the lower byte of data written to the PCMCIA Data Port selected by the PCMCIA Index Register.
ECh	Configuration Index Register	R/W	Contains the address of one of the Configuration Registers mentioned in Table 22.
EDh	Configuration Data Port	R/W	Contains the data written to the Configuration Register selected by the Configuration Index Register.
EEh*+	Fast A20 Register	R/W	A read enables Fast A20 and a write disables Fast A20.
EFh*+	Fast CPU Reset Register	R	A read resets the CPU.
F0h	Coprocessor Busy Register	W	A write clears –BUSYCPU and PEREQCPU signals.
F1h	Coprocessor Reset Register	W	A write resets the coprocessor.
F4h+	Slow CPU Register	W	A write enables slow clock for the CPU.
F5h+	Fast CPU Register	W	A write enables fast clock for the CPU.
F9h+	Configuration Disable Register	W	A write disables access to the Configuration Registers.
FBh+	Configuration Enable Register	W	A write enables access to the Configuration Registers.

* Also can be activated through port 92h for PS/2 compatibility.

+ These decodes can be disabled by setting the MSB of the MISCSET Register in case of conflict.

AC CHARACTERISTICS: TA = 0°C to 70°C, VDD = 5 V ±10%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Comments/Conditions
Clock Timings					
t1	TCLK2 Period	15.0		ns	Processor Clock
t2	TCLK2 High	6.5		ns	VIH=0.7 x VDD, 60/40% Duty Cycle
t3	TCLK2 Low	6.5		ns	VIL=0.2 x VDD, 60/40% Duty Cycle
t4	BUSOSC Period	31.0		ns	16 MHz AT Bus Clock
t5	BUSOSC High	12.0		ns	VIL=0.8 V, VIH=2.0 V, 60/40% Duty Cycle
t6	BUSOSC Low	12.0		ns	VIL=0.8 V, VIH=2.0 V, 60/40% Duty Cycle
t7	CLK2IN High	6.5		ns	
t8	CLK2IN Low	6.5		ns	
t9	CLK2 Fall		4.0	ns	CL=50 pF, 3.6 V to 1.0 V
t10	CLK2 Rise		4.0	ns	CL=50 pF, 1.0 V to 3.6 V
tD11	TCLK2 to CLK2	4.0	25.0	ns	CL=50 pF
t12	SYSCLK Fall		10.0	ns	CL=200 pF, tested at VOL=0.8 V, VOH = 2.0 V
t13	SYSCLK Rise		10.0	ns	CL=200 pF, tested at VOL=0.8 V, VOH = 2.0 V
tD14	TCLK2 to SYSCLK	5.0	40.0	ns	CL=200 pF
tD14a	BUSOSC to SYSCLK	5.0	40.0	ns	CL=200 pF
t15	OSC High	20.0		ns	VIL=0.8 V, VIH=2.0 V, 60/40% duty cycle
t16	OSC Low	20.0		ns	VIL=0.8 V, VIH=2.0 V, 60/40% duty cycle
CPU Mode Timings					
tD17	CLK2IN to RESCPU	3.0	10.0	ns	CL=30 pF
tD18	CLK2IN to RESNPX	3.0	10.0	ns	CL=30 pF

AC CHARACTERISTICS (Cont): TA = 0°C to 70°C, VDD = 5 V ±10%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Comments/Conditions
CPU Mode Timings (Cont.)					
tD19	CLK2IN to –READY, –SRDY	4.0	16.0	ns	CL=30 pF
tD21	CLK2IN to –ROMCS/–PPICS	4.0	20.0	ns	CL=50 pF (ROM cycles)
tD22	CLK2IN to –BUSYCPU	4.0	25.0	ns	CL=50 pF
tD23	CLK2IN to MA10-MA0	4.0	21.0	ns	CL=150 pF (Row -> Column Address)
tD24	A23-A1 to MA10-MA0	4.0	30.0	ns	CL=150 pF (Row Address)
tD25	CLK2IN to –RAS3 - –RAS0	4.0	10.0	ns	CL=75 pF
tD26	CLK2IN to –CAS3 - –CAS0	4.0	10.0	ns	CL=75 pF
tD27	CLK2IN to –RAMW/–WE0, MA1O/–WE1	4.0	20.0	ns	CL=150 pF
tD28	CLK2IN to D15-D0 Active (Re-drive)	4.0		ns	CL=100 pF, from –READY Active
tD29	CLK2IN to D15-D0 Valid (Re-drive)		25.0	ns	CL=100 pF
tD30	CLK2IN to D15-D0 Float (Re-drive)	4.0	20.0	ns	CL=100 pF
tD31	CLK2IN to PAR1, PAR0 Active	4.0	20.0	ns	CL=50 pF, from –RAMW Active
tD32	D15-D0 to PAR1, PAR0	3.0	14.0	ns	CL=50 pF
tD33	CLK2IN to PAR1, PAR0 Float	4.0	20.0	ns	CL=50 pF, from –RAMW Inactive
tD33a	CLK2IN to –OE0, –OE1	4.0	20.0	ns	CL=150 pF, 512KX8 option
tD34	PEREQNPX to PEREQCPU	3.0	25.0	ns	CL=50 pF
tD35	–BUSYNPX High to PEREQCPU High	3.0	25.0	ns	CL=50 pF
tD36	–BUSYNPX to –BUSYCPU	3.0	25.0	ns	CL=50 pF
tD37	SYSCLK to BALE	–6.0	10.0	ns	CL=200 pF
tD38	SYSCLK to –CMD	–6.0	15.0	ns	CL=200 pF, Note 6
tD39	SYSCLK to –SCMD Valid	–6.0	15.0	ns	CL=200 pF, Note 7

AC CHARACTERISTICS (Cont): TA = 0°C to 70°C, VDD = 5 V ±10%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Comments/Conditions
CPU Timings (Cont.)					
tD40	SYSCLK to –SCMD Active	–5.0	25.0	ns	CL=200 pF, Note 7
tD41	SYSCLK to –SCMD Float	–5.0	25.0	ns	CL=200 pF, Note 7
tD42	CLK2IN to –ROMCS/–PPICS	4.0	40.0	ns	CL=50 pF (Keyboard or RTC Access)
tD43	CLK2IN to SA19-SA0, –SBHE	4.0	30.0	ns	CL=200 pF
tD43a	A23-A17 to LA23-17	4.0	25.0	ns	CL=200 pF
tD44	SYSCLK to SA0 (Conversion Cycle)	–5.0	16.0	ns	CL=200 pF
tD45	SYSCLK to SD15-SD0 Active	–1.0		ns	CL=200 pF, Slot Write Cycles
tD46	SYSCLK to SD15-SD0 Valid		35.0	ns	CL=200 pF, Slot Write Cycles
tD47	SYSCLK to SD15-SD0 Float	–2.0	30.0	ns	CL=200 pF, Slot Write Cycles
tD51	CLK2IN to NMI	4.0	50.0	ns	CL=50 pF, Parity Error
tD53	CLK2IN to MA10-MA0	4.0	40.0	ns	CL=300 pF, PCMCIA Accesses Only
tD54	–IOW Low to PEREQCPU, –BUSYCPU	4.0	50.0	ns	CL=50 pF, during Port F0h Write
tD55	–IOW Inactive to BLKA20	4.0	50.0	ns	CL=50 pF, following Write Strobe to Port 64h
tD56	–IOW Inactive to NMI, SPKR	4.0	50.0	ns	CL=50 pF, following Port 61h Write
tD57	–IOW, –IOR Low to BLKA20	4.0	50.0	ns	CL=50 pF, during Port 92h Write or Port EEh Read
tSU60	–ADS, –SADS to CLK2IN Setup	15.0		ns	End T1/T2P
tH61	–ADS, –SADS from CLK2IN Hold	4.0		ns	End T1/T2P
tSU62	W/–R, M/–IO, D/–C to CLK2IN Setup	15.0		ns	End T1/T2P
tH63	W/–R, M/–IO, D/–C to CLK2IN Hold	4.0		ns	End T1/T2P
tSU64	A23-A1 from CLK2IN Hold	15.0		ns	End T1/T2P

AC CHARACTERISTICS (Cont): TA = 0°C to 70°C, VDD = 5 V ±10%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Comments/Conditions
CPU Mode Timings (Cont.)					
tH65	A23-A1 to CLK2IN Hold	4.0		ns	End T2/T1P
tSU66	–BLE, –BHE to CLK2IN Setup	15.0		ns	End T1/T2P
tSU66a	–BLE, –BHE to CLK2IN Setup	15.0		ns	Cache Enabled, Mid T2/T1P
tH67	–BLE, –BHE from CLK2IN Hold	4.0		ns	End T2/T1P
tH67a	–BLE, –BHE from CLK2IN Hold	4.0		ns	Cache Enabled, End T2/T1P
tSU68	–MISS Setup to CLK2IN	10.0		ns	Cache Enabled, Mid T2/T1P
tH69	–MISS Hold from CLK2IN	4.0		ns	Cache Enabled, End T2/T1P
tSU70	D15-D0, PAR1, PAR0 to CLK2IN Setup	4.0		ns	To latch for Parity Checking, On-board Memory Reads
tH71	D15-D0, PAR1, PAR0 to CLK2IN Hold	13.0		ns	To latch for Parity Checking, On-board Memory Reads
tSU72	–MEMCS16 to SYSCLK Setup	30.0		ns	
tH73	–MEMCS16 from SYSCLK Hold	–2.0		ns	
tSU74	–WS0 to SYSCLK Setup	30.0		ns	
tH75	–WS0 from SYSCLK Hold	–2.0		ns	
tSU76	IOCHRDY to SYSCLK Setup	30.0		ns	
tH77	IOCHRDY from SYSCLK Hold	–2.0		ns	
tSU78	–IOCS16 to SYSCLK Setup	30.0		ns	
tH79	–IOCS16 from SYSCLK Hold	–2.0		ns	
tSU80	D15-D0 to SYSCLK Setup	30.0		ns	To latch Data during CPU Off-board Read Cycles
tH81	D15-D0 from SYSCLK Hold	6.0		ns	To latch Data during CPU Off-board Read Cycles
tSU82	SD15-SD0 to SYSCLK Setup	30.0		ns	To latch Data during CPU Off-board Read Cycles

AC CHARACTERISTICS (Cont): TA = 0°C to 70°C, VDD = 5 V ±10%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Comments/Conditions
CPU Timings (Cont.)					
tH83	SD15-SD0 from SYSCLK Hold	6.0		ns	To latch Data during CPU Off-board Read Cycles
tSU84	SD15-SD0 to SYSCLK Setup	75.0		ns	Internal Register Accesses, CPU Write Cycles
tH85	SD15-SD0 to SYSCLK Setup	30.0		ns	Internal Register Accesses, CPU Write Cycles
Bus Arbitration Timings					
tD101	CLK2IN to HRQ	4.0	25.0	ns	CL=50 pF
tSU102	HLDA to CLK2IN Setup	15.0		ns	
tH103	HLDA from CLK2IN Hold	4.0		ns	
tD104	–MASTER to AEN	3.0	35.0	ns	CL=200 pF
tD105	HLDA to AEN	3.0	35.0	ns	CL=200 pF
tD106	HLDA to BALE	3.0	35.0	ns	CL=200 pF
tD107	–REFRESH to SA16-SA0, –MEMR, –SMEMR Active	3.0	30.0	ns	CL=200 pF, Start of External Master Refresh Cycle
tD108	–REFRESH to SA16-SA0, –MEMR, –SMEMR Float	3.0	30.0	ns	CL=200 pF, Start of External Master Refresh Cycle
tD109	–REFRESH to A23-A1, –BLE, –BHE Active	3.0	30.0	ns	CL=50 pF
tD110	–REFRESH to A23-A1, –BLE, –BHE Float	3.0	30.0	ns	CL=50 pF
tD111	–MASTER Low to SA, LA, –SBHE, –CMD float	3.0	30.0	ns	CL=200 pF
tD112	–MASTER High to SA, LA, –SBHE, –CMD Active	3.0	30.0	ns	CL=200 pF
tD113	HLDA High to A23-A1, –BHE, –BLE Active	3.0	25.0	ns	CL=50 pF

AC CHARACTERISTICS (Cont): TA = 0°C to 70°C, VDD = 5 V ±10%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Comments/Conditions
Bus Arbitration Timings (Cont.)					
tD114	CLK2 Rising Edge that drives HLDA low to A23-A1, –BHE, –BLE Float	3.0	25.0	ns	CL=50 pF
Interrupt Timings					
tPW117	External Interrupt Request Pulse Width Active	105.0		ns	Glitch-free Circuit is On
tD118	External IRQ to INTR High	5.0	130.0	ns	CL=50 pF, Glitch-free Circuit is Off
tD120	OSC to INTR High	5.0	130.0	ns	CL=50 pF, Glitch-free Circuit is On
tD120a	OSC to INTR	35.0	200.0	ns	CL=50 pF, when Source is from Internal IRQ0
tSU121	External Interrupt to OSC Setup		15.0	ns	Glitch-free Circuit is On
tH122	External Interrupt to OSC Hold		10.0	ns	Glitch-free Circuit is On
tD123	–IOCHCK to NMI	3.0	40.0	ns	CL=50 pF
tD124	–ERRORNPX Low to INTR	5.0	150.0	ns	CL=50 pF
Miscellaneous Timings					
tPW126	–IOCHCK Pulse Width	15.0		ns	
tSU127	–RESET to OSC Setup	15.0		ns	
tH128	–RESET from OSC Hold	10.0		ns	
tD129	SYSCLK to RSTDRV	–10.0	20.0	ns	CL=200 pF
tD130	OSC to SPKR	5.0	120.0	ns	CL=50 pF
tD131	CLK2IN to DRAM Interface Active	4.0	50.0	ns	Following 4th –ADS after Power-On Reset

AC CHARACTERISTICS (Cont): TA = 0°C to 70°C, VDD = 5 V ±10%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Comments/Conditions
DRAM Controller Timings (HLDA/Refresh Cycles)					
tD132	–MEMW to –RAMW	3.0	30.0	ns	CL=300 pF
tD133	–MEMW/–MEMR to –RAS3 - –RAS0	4.0	25.0	ns	CL=150 pF
tD134	OSC to –CAS3 - –CAS0 Low	4.0	25.0	ns	CL=150 pF, either High or Low OSC Edge
tD135	–MEMW/–MEMR to –CAS3 - –CAS0 High	4.0	25.0	ns	CL=150 pF
tD136	OSC to MA10-MA0 (Row to Column Address)	5.0	35.0	ns	CL=300 pF, either High or Low OSC Edge
tD137a	LA23-LA17, SA16-SA0 to MA10-MA0	5.0	40.0	ns	CL=300 pF, Row Address
tD138	LA23-LA17, SA16-SA14 to MA10-MA0	5.0	50.0	ns	CL=300 pF, Memory Card Access
tD139	–MEMW Low to PAR1, PAR0 Active	4.0	25.0	ns	CL=50 pF, On-board Memory Write Cycles
tD140	–MEMW High to PAR1, PAR0 Float	4.0	25.0	ns	CL=50 pF, On-board Memory Write Cycles
tD141	SD15-SD0 to PAR1, PAR0	5.0	45.0	ns	CL=50 pF, On-board Memory Write Cycles
Data Steering Timings					
tD143	SD7-SD0 to D15-D8	4.0	30.0	ns	CL=200 pF. On-board –MEMW/–IOR odd byte (8-bit DMA). CL=100 pF. Swap odd byte read from 8-bit Master.
tD144	SD7-SD0 to D7-D0	4.0	30.0	ns	CL=200 pF. On-board –MEMW/–IOR even byte (8/16-bit DMA). CL=200pF. On-board –MEMW cycles (external Bus Master).
tD145	D7-D0 to SD7-SD0	4.0	25.0	ns	On-board –MEMR/–IOW even byte (8/16-bit DMA). On-board –MEMR cycles (external Bus Master).
tD146	D15-D8 to SD7-SD0	4.0	25.0	ns	On-board –MEMR/–IOW odd byte (8-bit DMA). Data swap odd byte write to an 8-bit slot card.

AC CHARACTERISTICS (Cont): TA = 0°C to 70°C, VDD = 5 V ±10%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Comments/Conditions
Data Steering Timings (Cont.)					
tSU147	–IOCS16 to –IOR, –IOW Setup	15.0		ns	In order to meet data steering requirements.
tH148	–IOCS16 from –IOR, –IOW Hold	5.0		ns	In order to meet data steering requirements.
tSU149	–MEMCS16 to –MEMR, –MEMW Setup	15.0		ns	In order to meet data steering requirements.
tH150	–MEMCS16 from –MEMR, –MEMW Hold	5.0		ns	In order to meet data steering requirements.
tSU149	–MEMCS16 to –MEMR, –MEMW Setup	15.0		ns	In order to meet data steering requirements.
Master Mode Timings					
tD153	SA15-SA0 to –PPICS	3.0	40.0	ns	CL=50pF
tD154	–MEMW, –MEMR to –SCMD	3.0	30.0	ns	CL=200pF, Note 7
tD155	LA23-LA20 to –SCMD Active	3.0	25.0	ns	CL=200pF
tD156	LA23-LA20 to –SCMD Float	3.0	25.0	ns	CL=200pF
tSU157	LA23-LA17, SA16-SA0, –BHE from –CMD Setup	35.0		ns	
tH158	LA23-LA17, SA16-SA0, –BHE from –CMD Hold	20.0		ns	Note 6
tD159	LA23-LA0, SA23-SA0, –SBHE to A23-A1, –BHE, –BLE	3.0	16.0	ns	CL=50pF
tSU161	SD15-SD0 to –IOW Setup	55.0		ns	Internal register accesses, even bytes.
tH162	SD15-SD0 to –IOW Hold	20.0		ns	Internal register accesses, even bytes.
tD165	–IOR Low to SD15-SD0	5.0	120.0	ns	CL=200pF. Internal register accesses.
tD165a	–IOR High to SD15-SD0 Float	4.0	30.0	ns	CL=200pF. Internal register accesses.

AC CHARACTERISTICS (Cont): TA = 0°C to 70°C, VDD = 5 V ±10%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Comments/Conditions
Master Mode Timings (Cont.)					
tD170	–CMD Low to SD15-SD8 Float	4.0	35.0	ns	CL=200 pF
tD171	–CMD High to SD15-SD0 Active	4.0	35.0	ns	CL=200 pF
tD172	–CMD Low to SD15-SD0 Active	4.0	35.0	ns	CL=200 pF. On-board –MEMR odd byte write to 8-bit ISA bus.
tD173	–CMD High to SD15-SD0 Float	4.0	35.0	ns	CL=200 pF. On-board –MEMR odd byte write to 8-bit ISA bus.
tD174	–CMD Low to D15-D0 Float	4.0	35.0	ns	CL=200 pF. On-board –MEMR odd byte write to 8-bit ISA bus.
tD175	–CMD High to D15-D0 Active	4.0	35.0	ns	CL=100 pF. On-board –MEMR odd byte write to 8-bit ISA bus.
Refresh Mode Timings					
tD182	SYSCLK to –REFRESH Low	–8.0	13.0	ns	CL=200 pF. Waiting for arbiter switch (std. ref. cycle).
tD183	SYSCLK to –REFRESH Float	–7.0	18.0	ns	CL=200 pF
tD184	SYSCLK to SA16-SA0	–4.0	40.0	ns	CL=200 pF
tD185	SYSCLK to A16-A1, –BLE	–4.0	40.0	ns	CL=50 pF
tD186	SYSCLK to MA10-MA0	–2.0	70.0	ns	CL=300 pF. RAS-only Refresh
tD188	SYSCLK to –MEMR	–5.0	30.0	ns	CL=200 pF
tSU189	–REFRESH to SYSCLK Setup	30.0		ns	External Bus Master refresh cycle.
tH189a	–REFRESH from SYSCLK Hold	5.0		ns	External Bus Master refresh cycle.
tD190	SYSCLK to –SMEMR	–5.0	30.0	ns	CL=200 pF
tD191	–REFRESH to –SMEMR Active	4.0	40.0	ns	CL=200 pF. External Bus Master refresh cycle.
tD192	–REFRESH to –SMEMR Float	–5.0	30.0	ns	CL=200 pF. External Bus Master refresh cycle.

AC CHARACTERISTICS (Cont): TA = 0°C to 70°C, VDD = 5 V ±10%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Comments/Conditions
Refresh Mode Timings (Cont.)					
tSU193	IOCHRDY to SYSCLK Setup	4.0		ns	
tH194	IOCHRDY from SYSCLK Hold	0.0	35.0	ns	
DMA Mode Timings					
tSU195	DRQ to SYSCLK Setup	20.0		ns	
tD197	SYSCLK to DK2-DK0 Active			ns	Waiting for arbiter switch.
tD198	SYSCLK to DK2-DK0	–2.0	70.0	ns	CL=50 pF
tD199	SYSCLK to DK2-DK0 Float	–2.0	70.0	ns	CL=50 pF. Internal DMAHRQ changes from 1 to 0.
tD200	SYSCLK to DKEN	–2.0	70.0	ns	CL=50 pF
tD201	SYSCLK to –CMD Valid	–5.0	60.0	ns	CL=200 pF. Note 6
tD202	SYSCLK to A23-A1, –BLE, –BHE Valid	0.0	90.0	ns	CL=50 pF
tD203	SYSCLK to A23-A1, –BLE, –BHE Active			ns	CL=50 pF
tD204	SYSCLK to A23-A1, –BLE, –BHE Float			ns	CL=50 pF
tD205	SYSCLK to SA0 Valid	0.0	95.0	ns	CL=200 pF
tD206	SYSCLK to T/C	–5.0	60.0	ns	CL=100 pF
tSU207	IOCHRDY to SYSCLK Setup	25.0		ns	
tH208	IOCHRDY from SYSCLK Hold	15.0		ns	
tD209	SYSCLK to –SCMD Valid	–5.0	60.0	ns	CL=200 pF. Note 7
tD210	–SCMD Active from –SYSCLK			ns	CL=200 pF
tD211	–SCMD Float from SYSCLK			ns	CL=200 pF

AC CHARACTERISTICS (Cont): TA = 0°C to 70°C, VDD = 5 V ±10%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Comments/Conditions
RTC Mode Timings					
tD213	VBAT good to PS high	2.0		µs	
tPW214	–RCLR Pulse Width	2.0		µs	
tD215	–RCLR low to VRT bit low		2.0	µs	
Keyboard Mode Timings					
tSU216	KDAT/MDAT Receive Data Setup	0		ns	
tH217	KDAT/MDAT Receive Data Hold		52.0	cycle	Periods of OSC
tH218	KDAT/MDAT Transmit Data Hold	18.0	52.0	cycle	Periods of OSC
SMI Mode Timings					
t219	–SMI Pulse Width	4.0		cycle	Periods of CLK2
t219a	CLK2IN to –SMI	3.0	15.0	ns	
Local Bus Timings					
tSU220	–LBA Falling to Mid-cycle CLK2IN Rising		10.0	ns	
tH221	–LBA from CLK2IN Hold	3.0		ns	
tD222	CLK2IN to –ADS, M/–IO, W/–R, D/–C, A23-A1, –BLE, –BHE	4.0	16.0	ns	CL = 50 pF (HLDA Cycles) T1 of local bus cycles
tH223	–READY to CLK2IN Setup	8.0		ns	Local bus cycles

Notes:
1. Specification is characterized and guaranteed, not 100% tested.
2. Asynchronous input for test purposes only to assure recognition at a particular clock edge.
3. Measurement point is when the pin is no longer driving.
4. This timing only indicates that the data steering logic will be settled to the correct path. A data swap will occur if –MEMCS16 or –IOCS16 are inactive during some cycle types. Actual performance and operation are determined by the system.
5. Specified minimums are characterized and guaranteed, not 100% tested.
6. –CMD refers to the signals –MEMR, –MEMW, –IOR, –IOW.
7. –SCMD refers to the signals –SMEMR and –SMEMW.

FIGURE 28. CLOCK TIMING

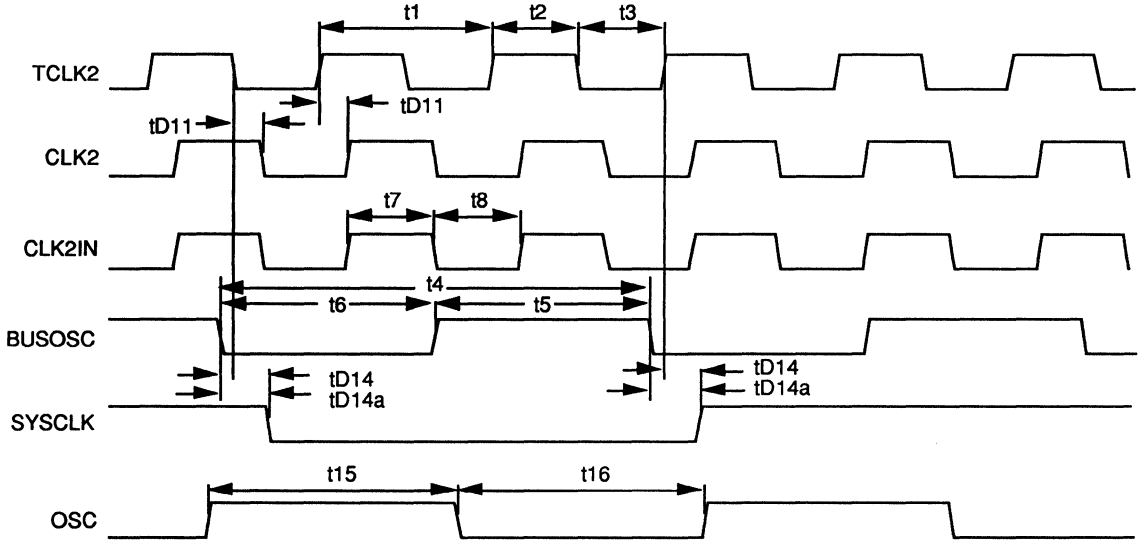


FIGURE 29. RESET TIMING

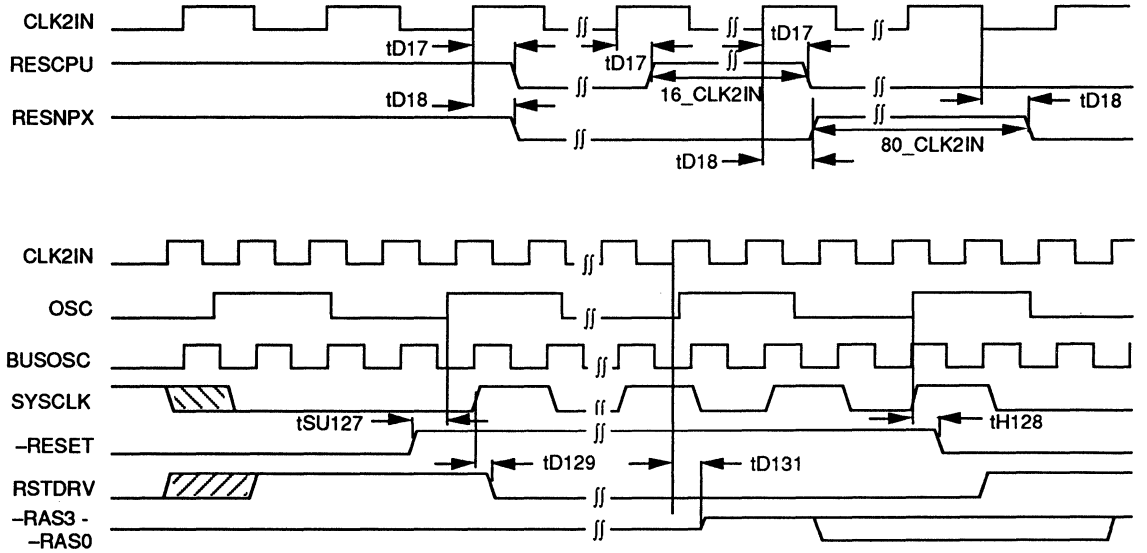
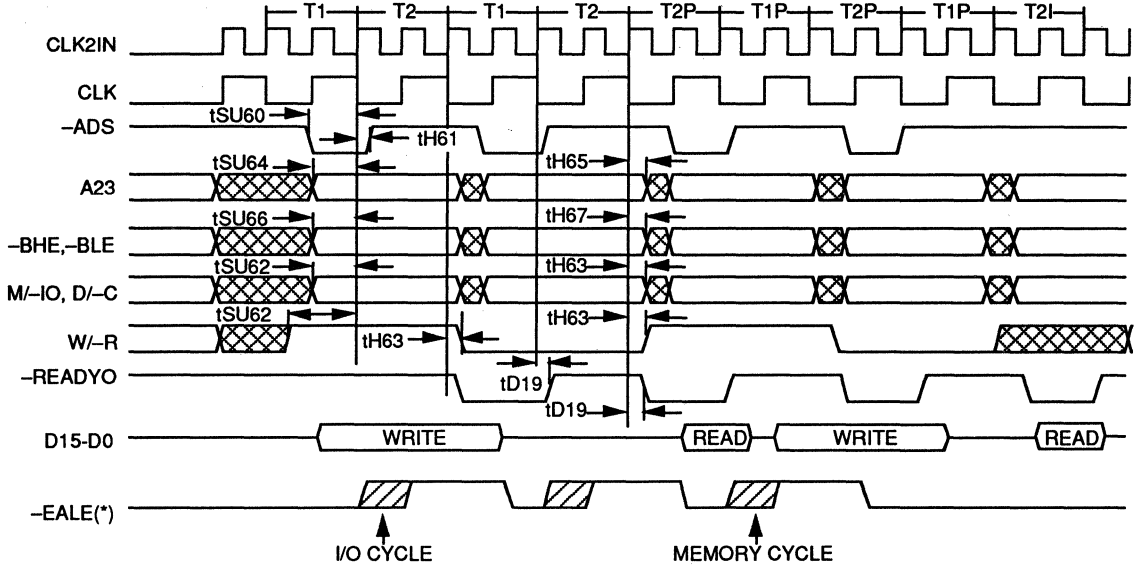


FIGURE 30. CPU INTERFACE TIMING



Notes: (*) Internal signal.

FIGURE 31. NUMERIC PROCESSOR EXTENSION INTERFACE TIMING

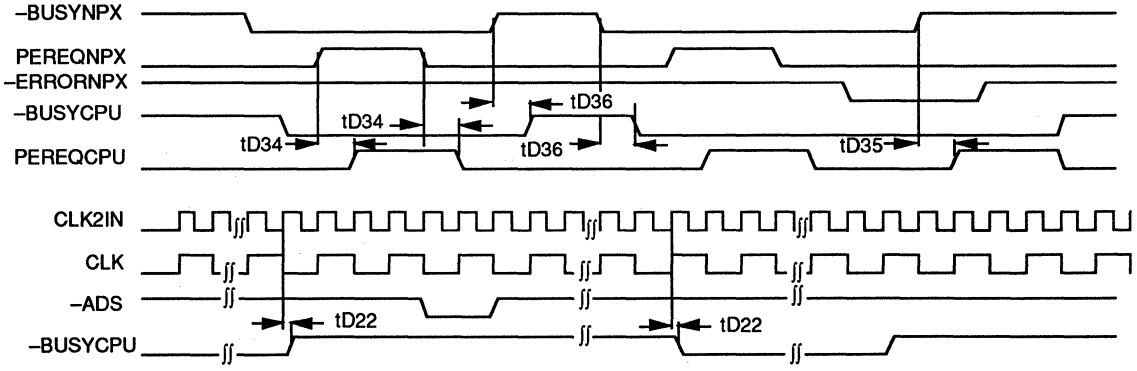


FIGURE 32. CPU MODE DRAM TIMING

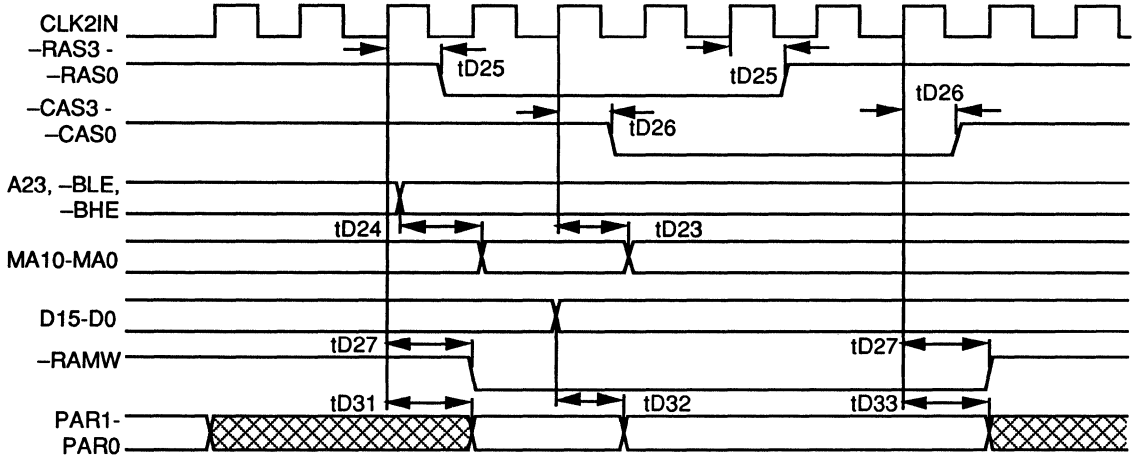


FIGURE 33. HLDA MODE DRAM TIMING

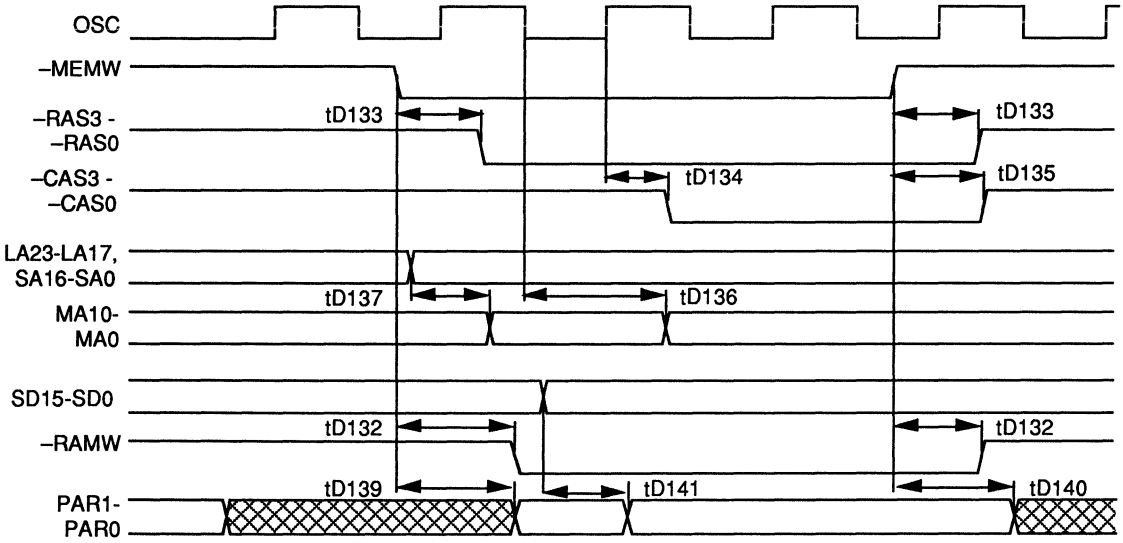
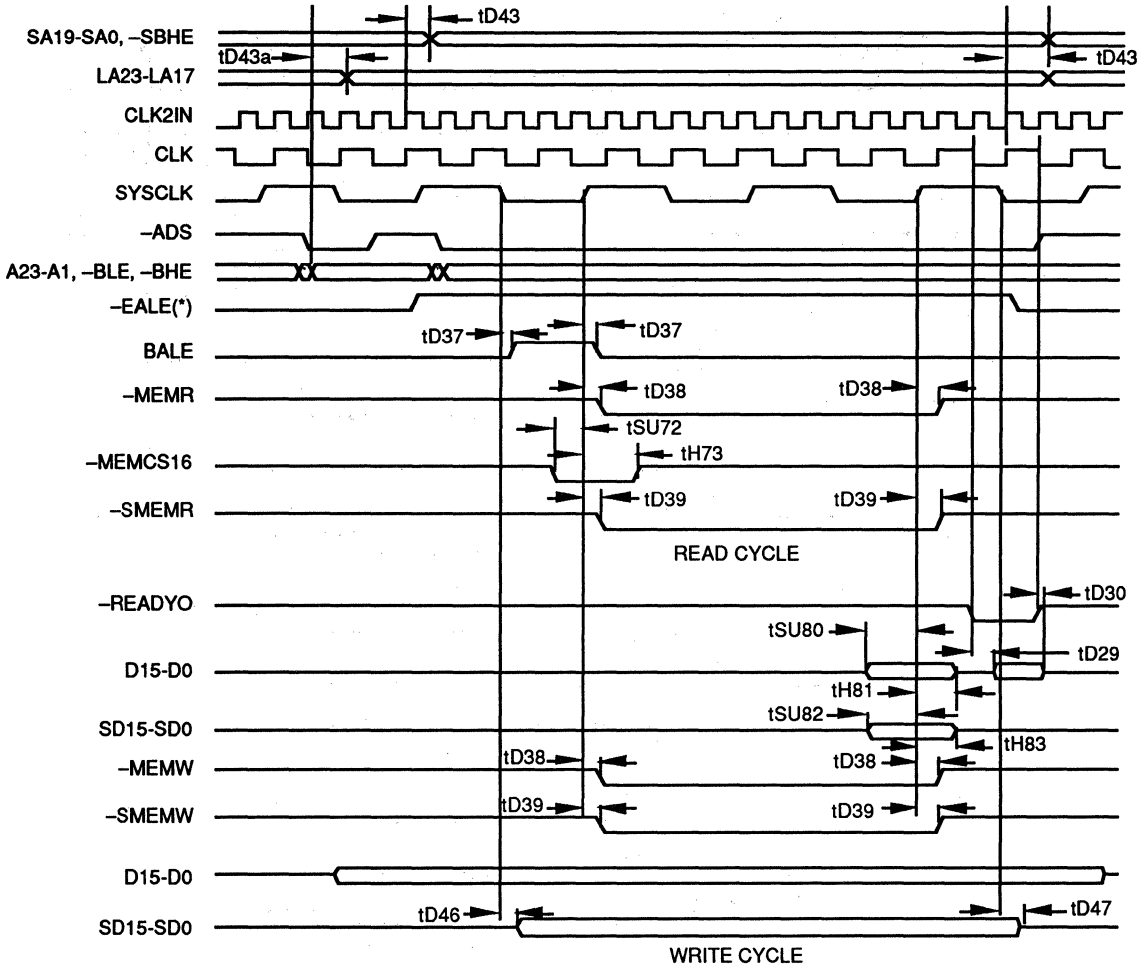


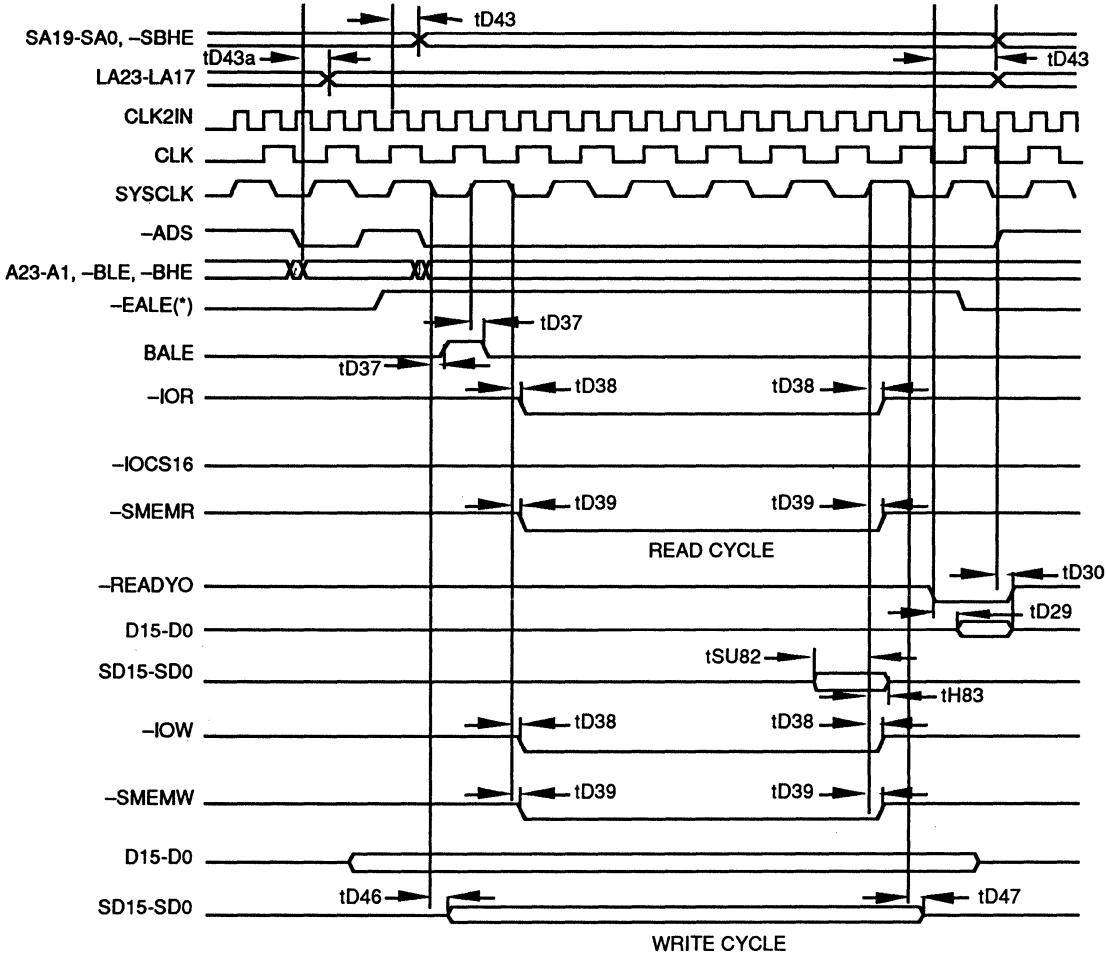
FIGURE 34. OFF-BOARD MEMORY CYCLE: 16-BIT



Notes: (*) Internal signal.

–SMEMR and –SMEMW are three-state for addresses above 1M.

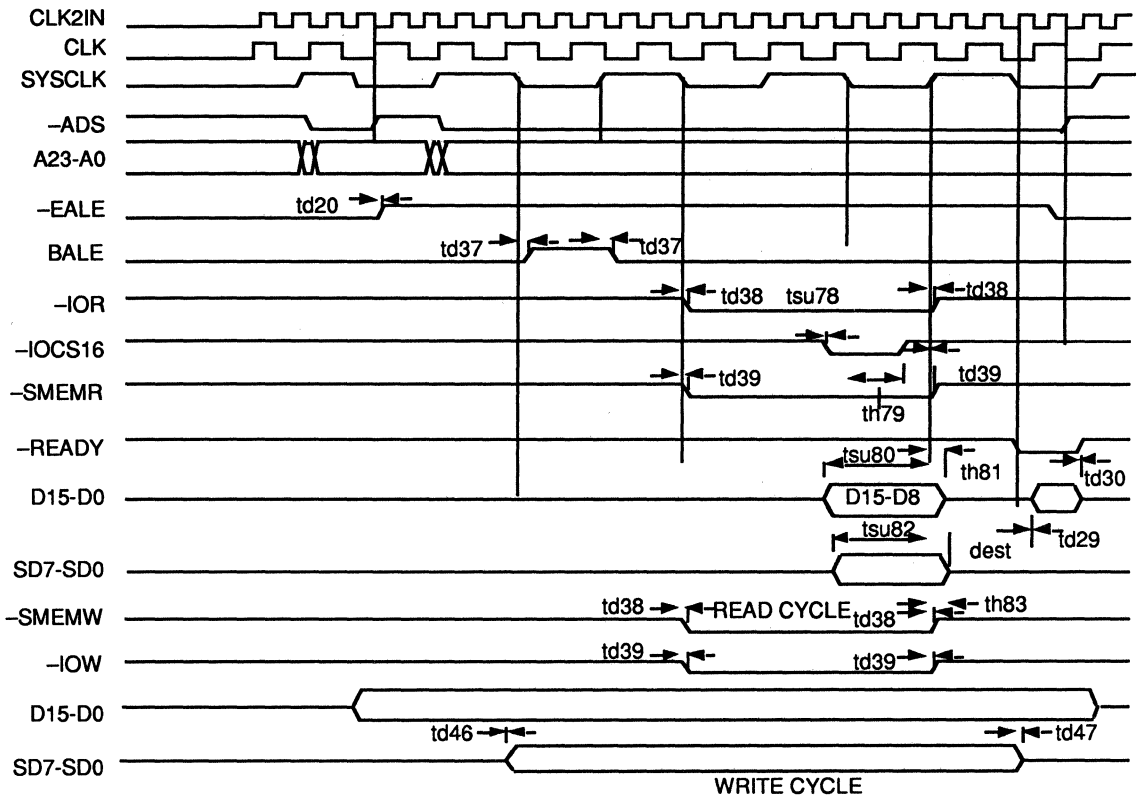
FIGURE 35. OFF-BOARD MEMORY CYCLE: 8-BIT



Notes: (*) Internal signal.

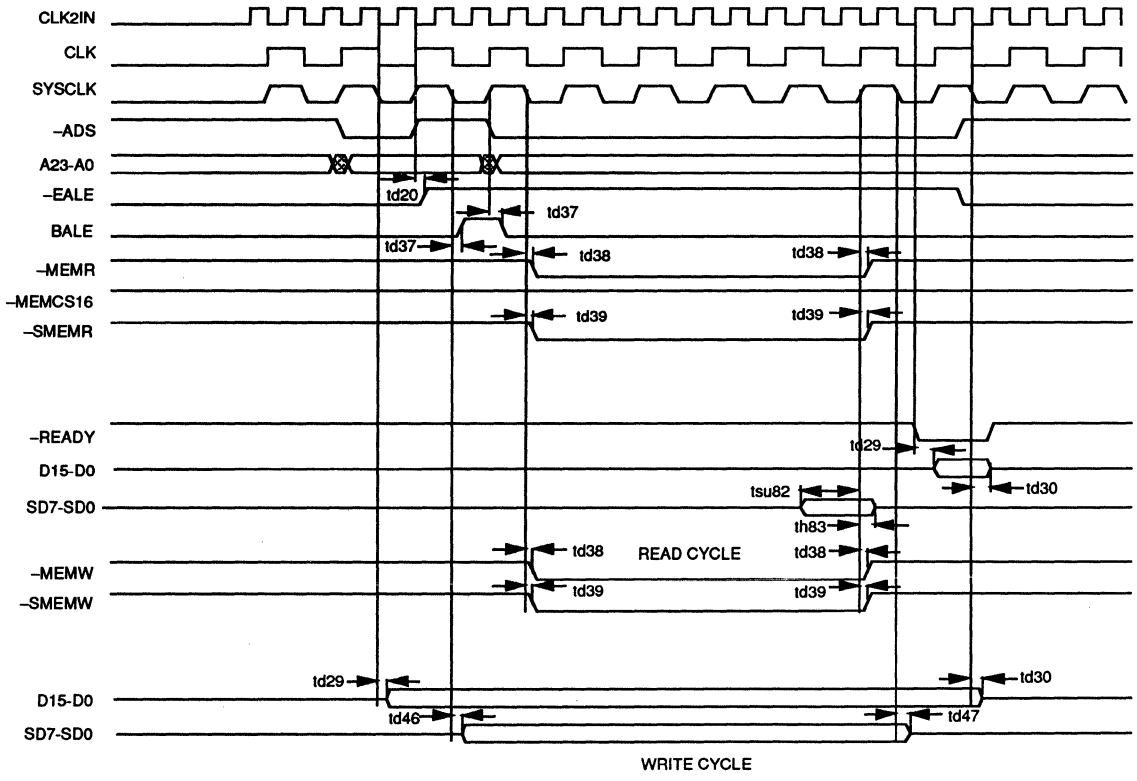
–SMEMR and –SMEMW are three-state for addresses above 1M.

FIGURE 36. OFF-BOARD IO CYCLE: 16-BIT



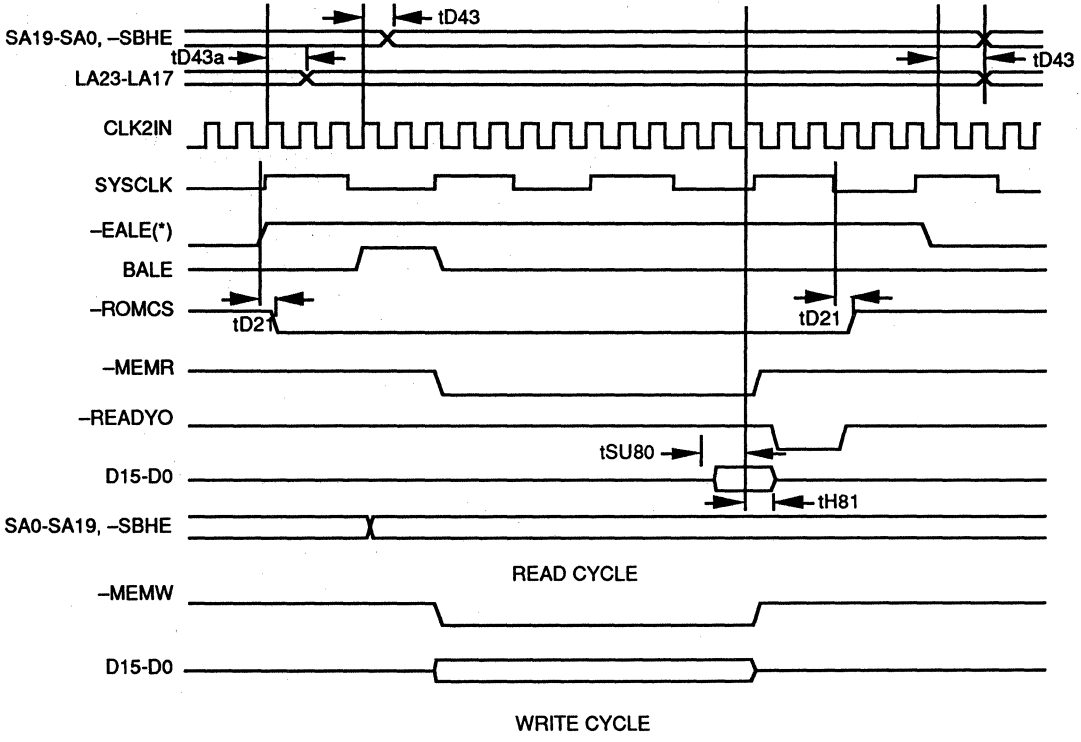
Note: -SMEMR and -SMEMW are three-state for addresses above 1M.

FIGURE 37. OFF-BOARD IO CYCLE: 8-BIT



Note: -SMEMR and -SMEMW are three-state for addresses above 1M.

FIGURE 38. D BUS ROM CYCLE



Notes: (*) Internal signal.

FIGURE 39. REFRESH CYCLE TIMING

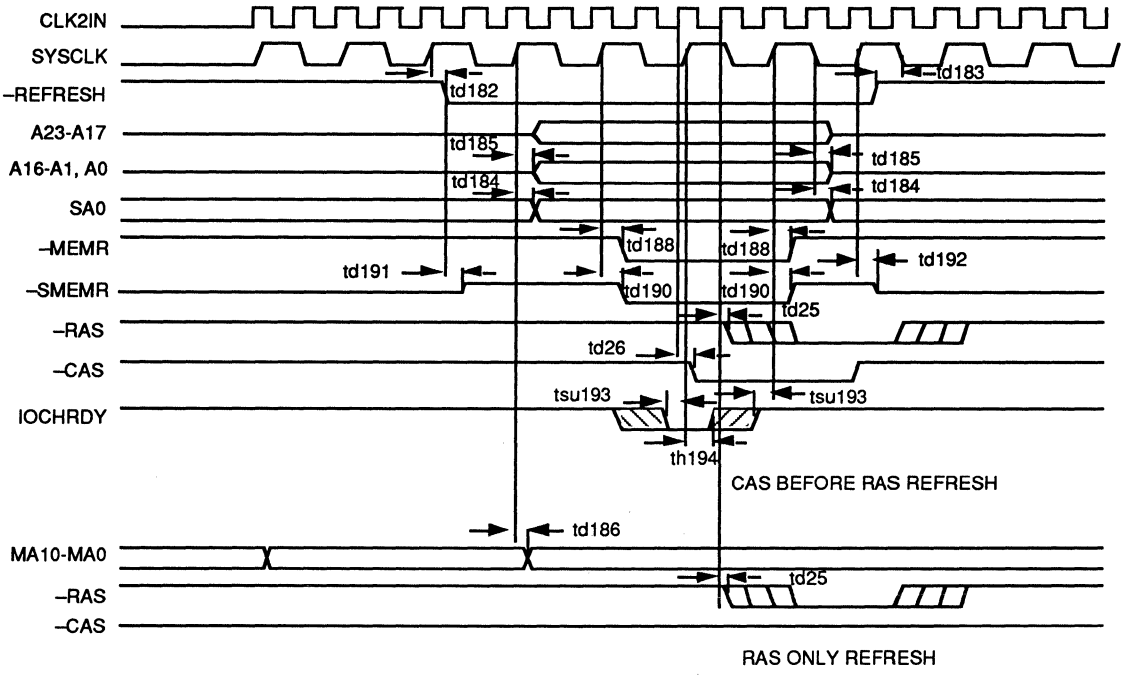


FIGURE 40. CPU MODE -WS0 AND IOCHRDY TIMING

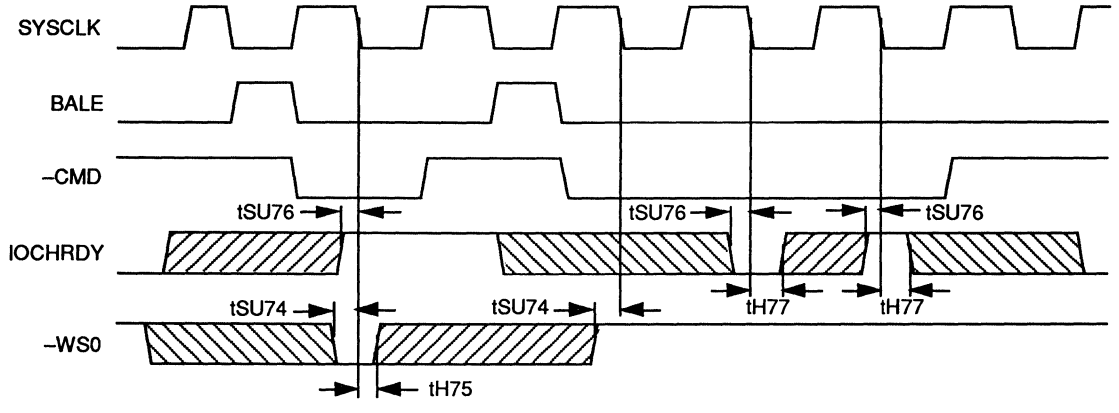
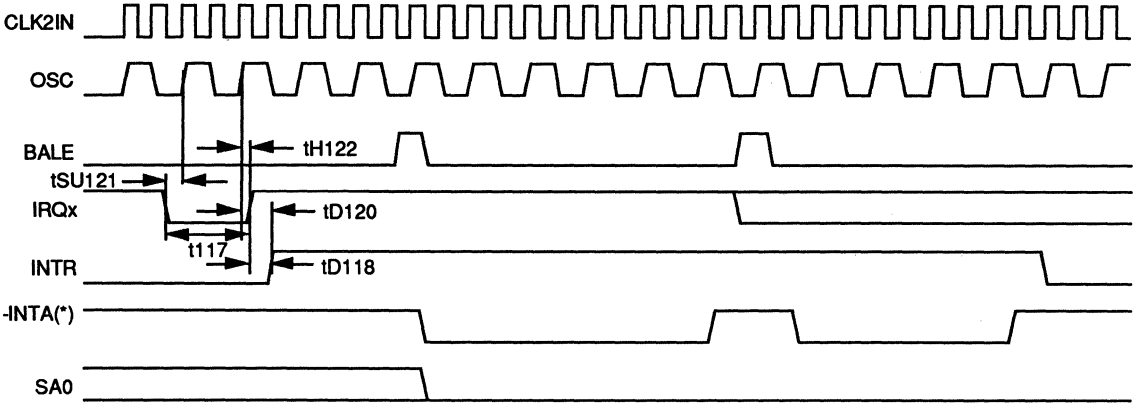


FIGURE 41. INTERRUPT ACKNOWLEDGE CYCLE



Notes: (*) Internal signal.

FIGURE 42. SPEAKER AND –IOCHK TIMING

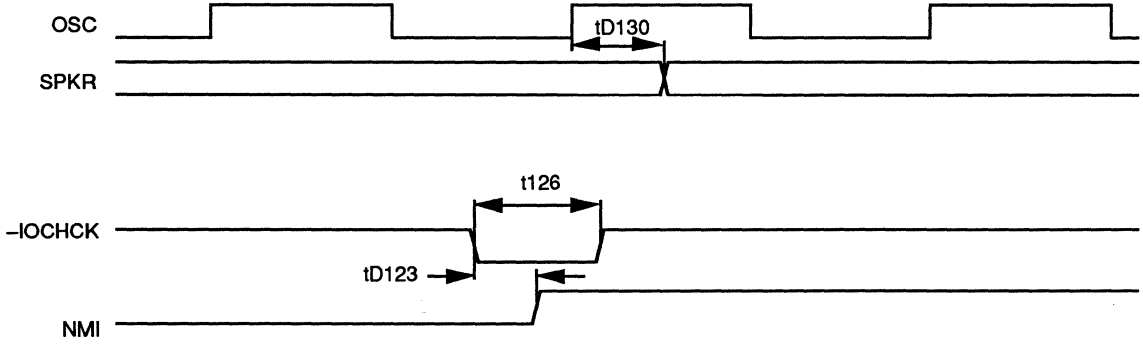
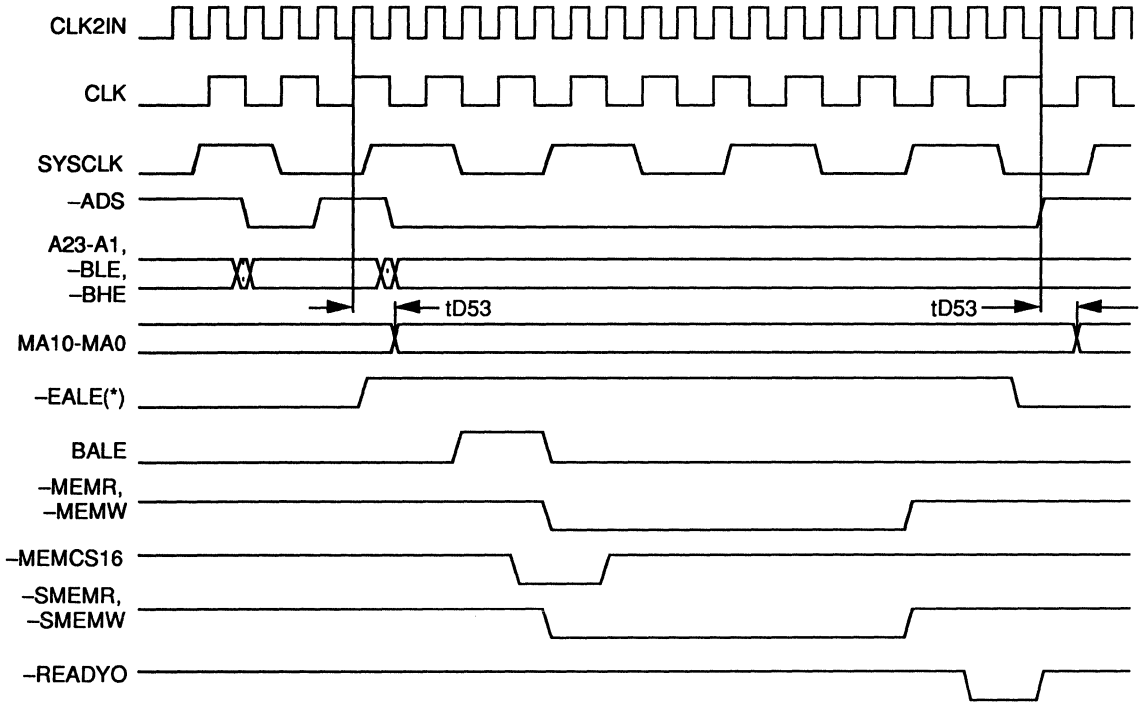


FIGURE 43. PCMCIA 1.0 MEMORY CARD TIMING



Notes: (*) Internal signal.

FIGURE 44. BUS ARBITRATION TIMING

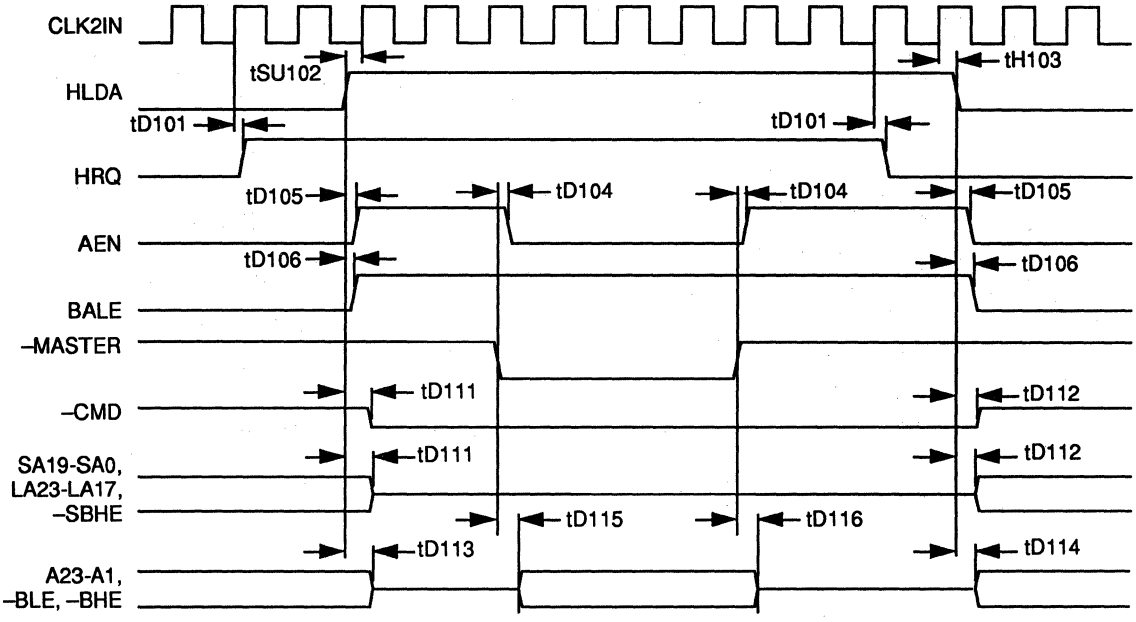


FIGURE 45. MASTER MODE CYCLE TIMING: ON-BOARD MEMORY ACCESSES

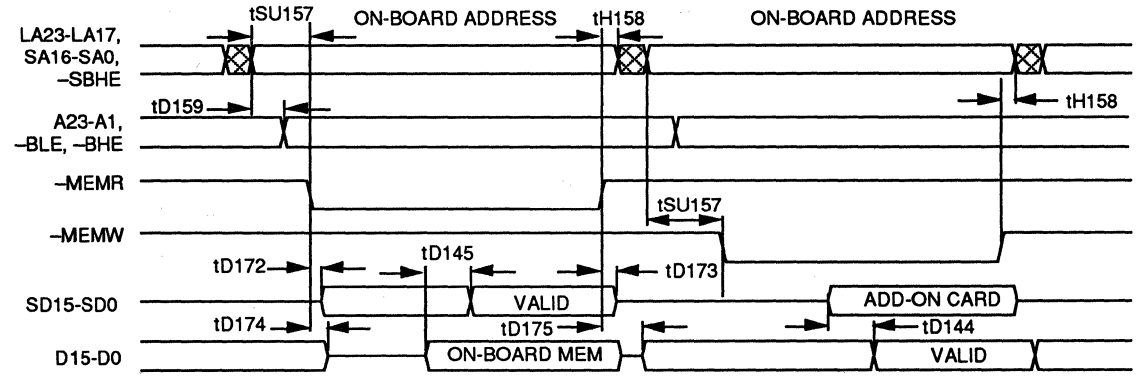
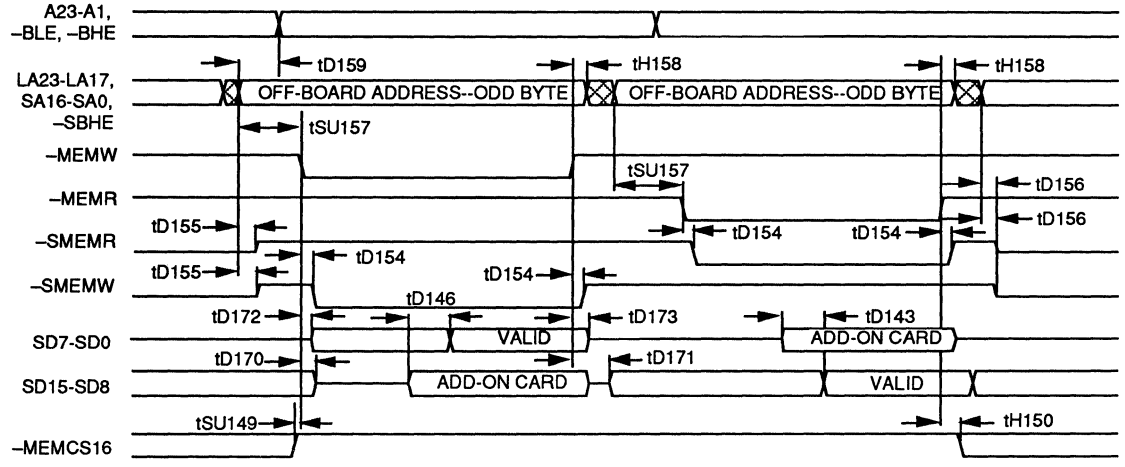


FIGURE 46. MASTER MODE CYCLE TIMING: OFF-BOARD MEMORY ACCESSES



Notes: -SMEMR and -SMEMW are three-state for addresses above 1M. They should be pulled up externally with a 10k resistor.

FIGURE 47. MASTER MODE CYCLE TIMING: I/O ACCESSES

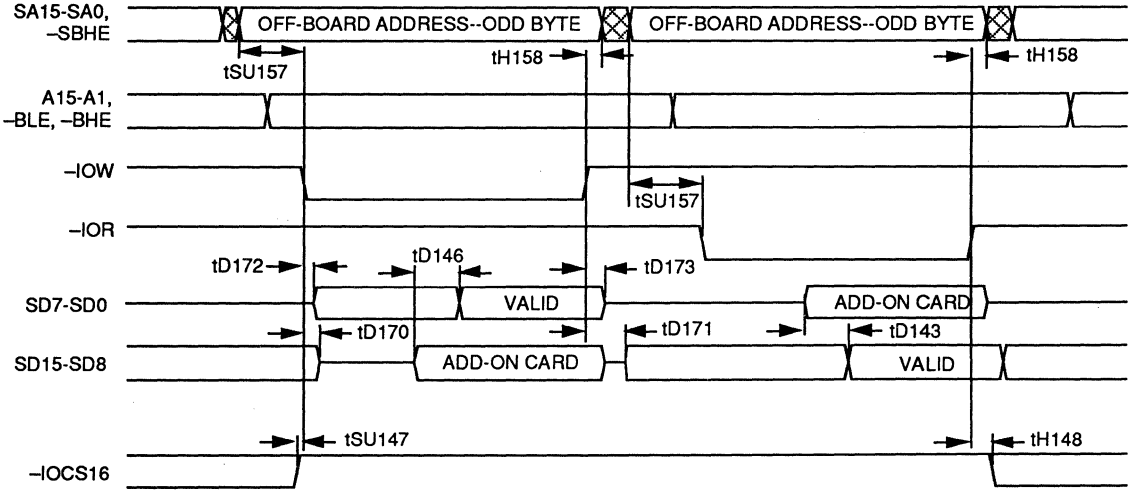


FIGURE 48. MASTER MODE CYCLE TIMING: INTERRUPT REGISTER ACCESSES

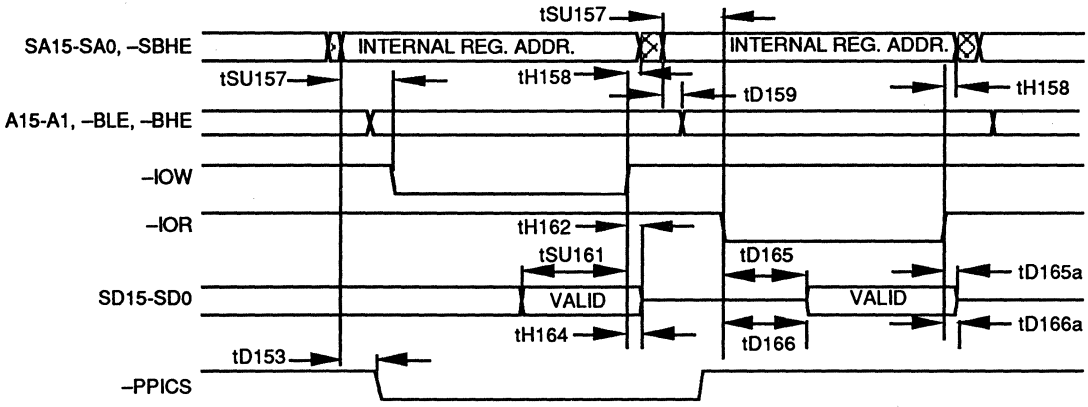


FIGURE 49. MASTER MODE REFRESH TIMING

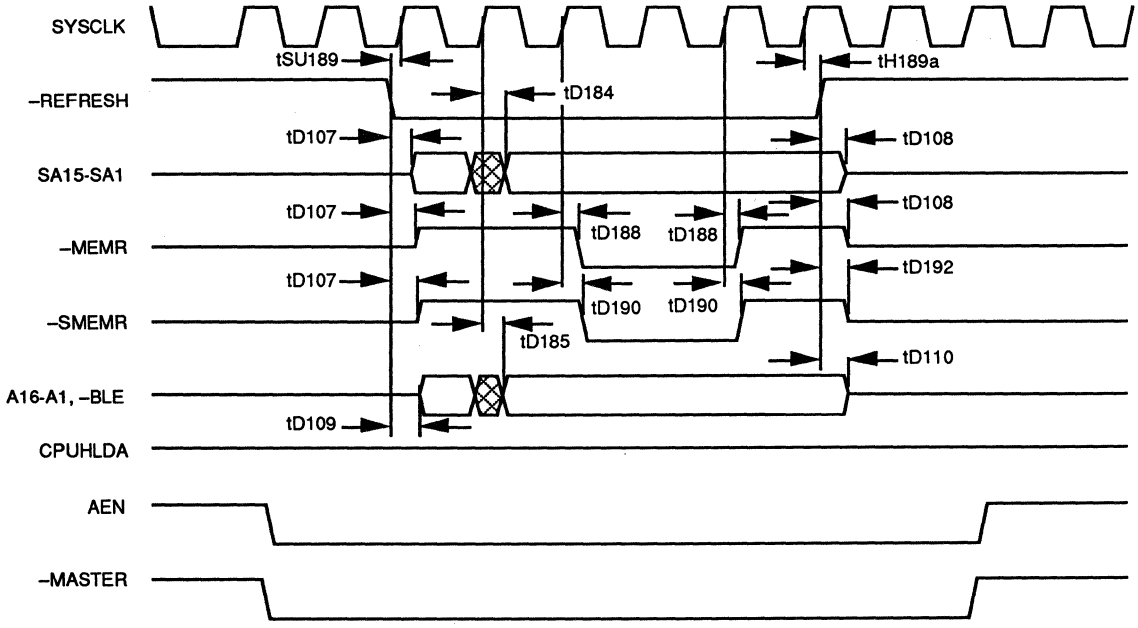
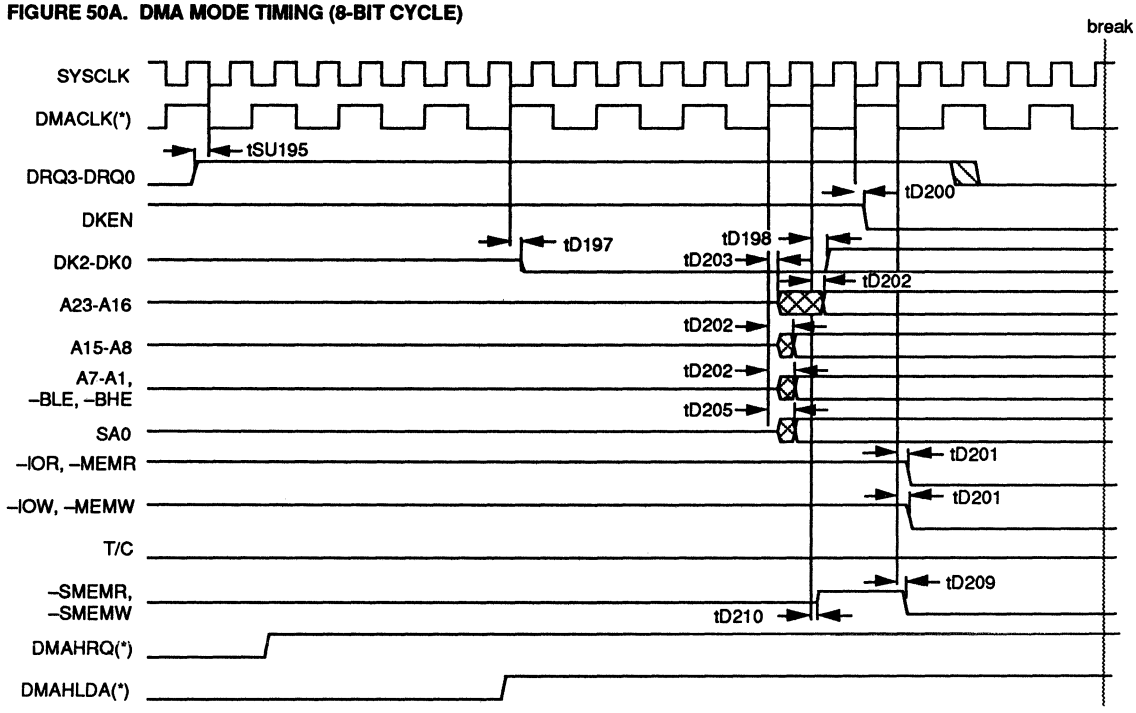


FIGURE 50A. DMA MODE TIMING (8-BIT CYCLE)

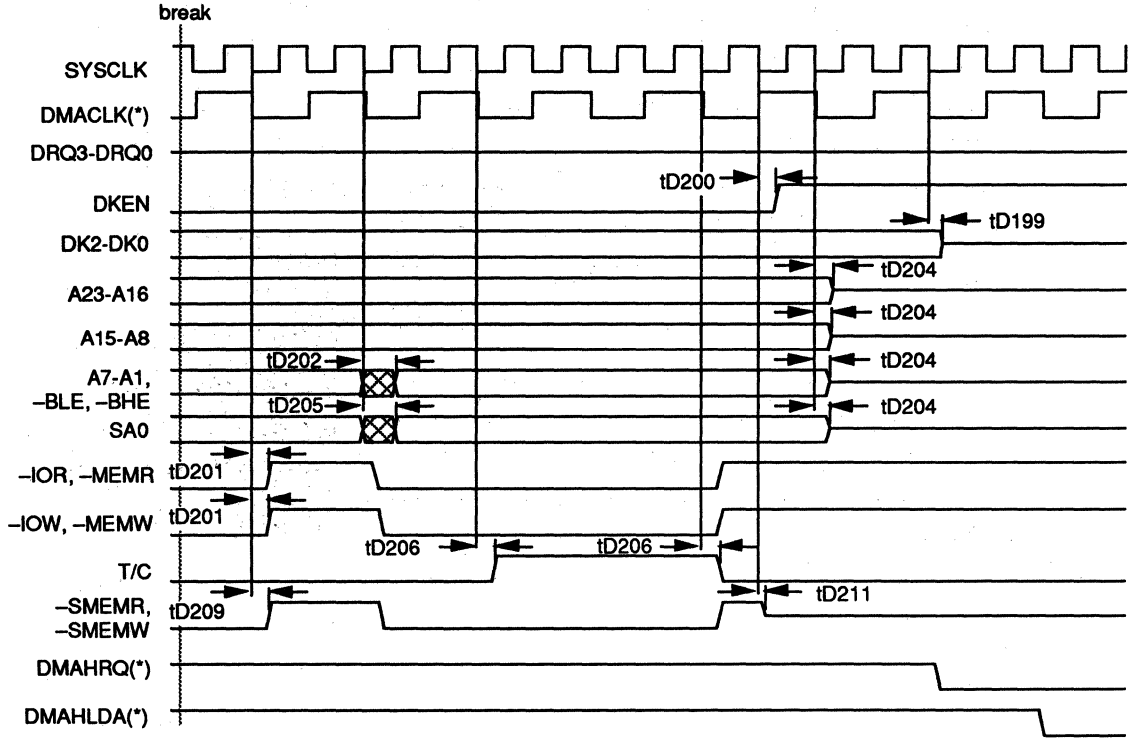


Notes: (*) Internal signal.

-SMEMR and -SMEMW are three-state for addresses above 1M.

-MEMR timing shown with ROMDMA Register bit 0 = 1. -IOW and -MEMW timing shown with DMA channels programmed for extended write mode.

FIGURE 50B. DMA MODE TIMING (8-BIT CYCLE)

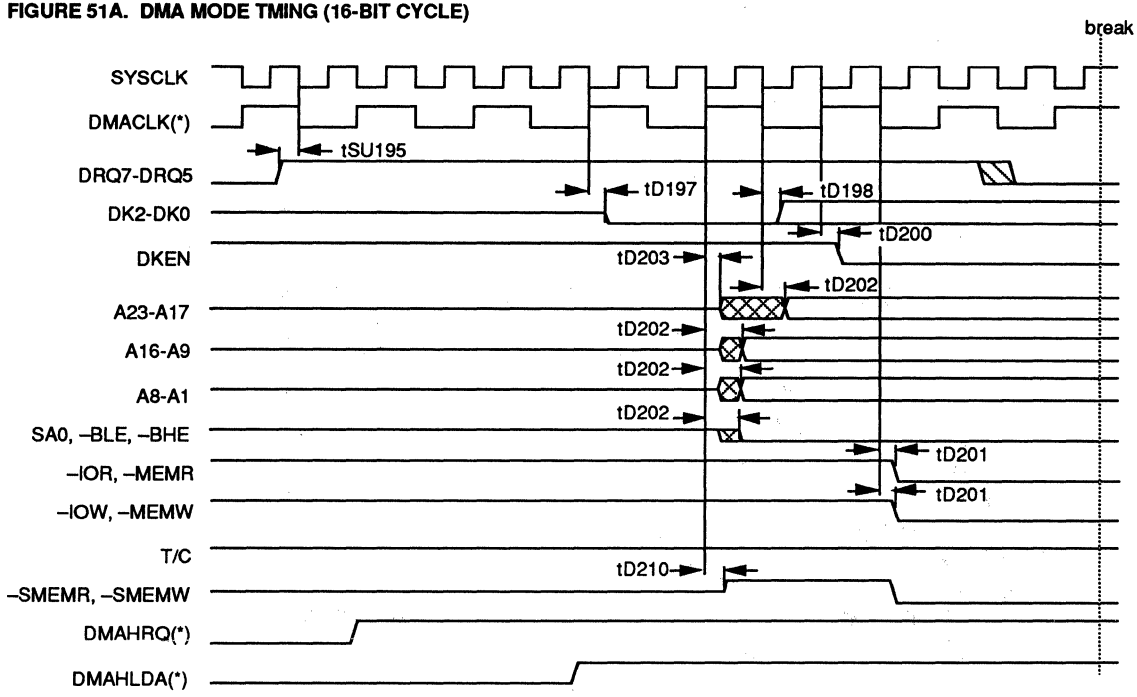


Notes: (*) Internal signal.

-SMEMR and -SMEMW are three-state for addresses above 1M.

-MEMR timing shown with ROMDMA Register bit 0 = 1. -IOW and -MEMW timing shown with DMA channels programmed for extended write mode.

FIGURE 51A. DMA MODE TMING (16-BIT CYCLE)

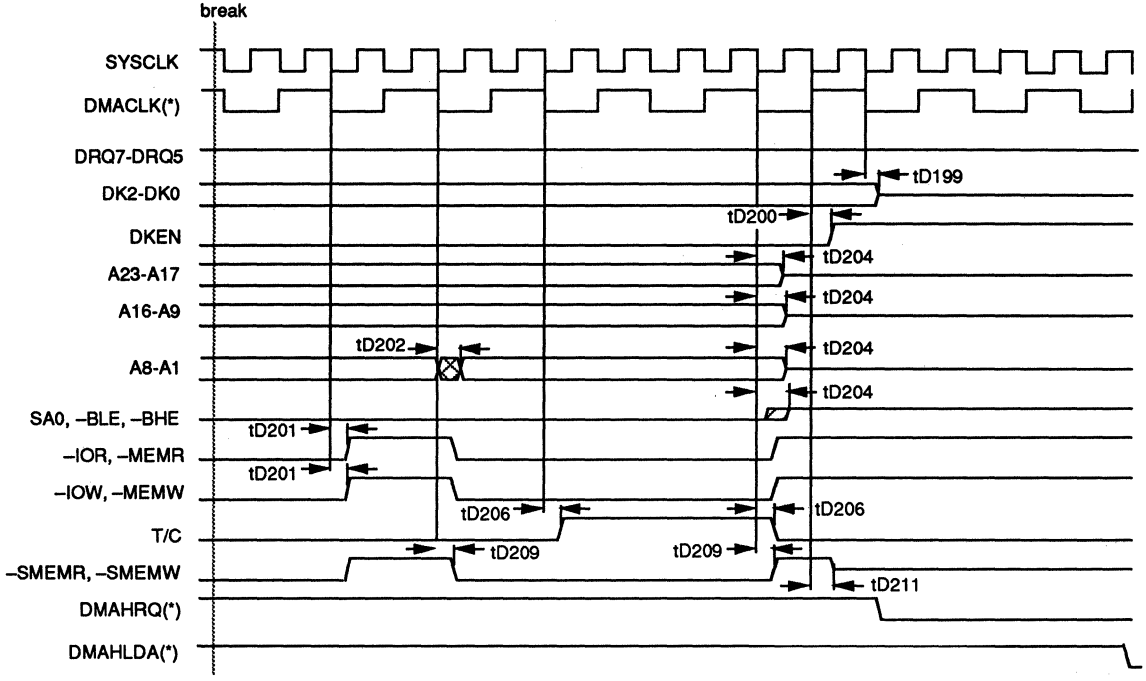


Notes: (*) Internal signal.

–SMEMR and –SMEMW are three-state for addresses above 1M.

–MEMR timing shown with ROMDMA Register bit 0 = 1. –IOW and –MEMW timing shown with DMA channels programmed in extended mode.

FIGURE 51B. DMA MODE TMING (16-BIT CYCLE)

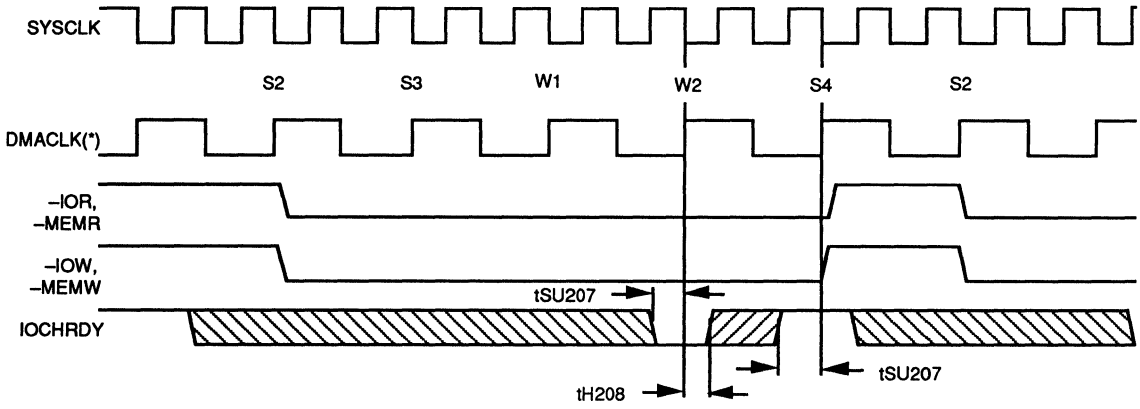


Notes: (*) Internal signal.

–SMEMR and –SMEMW are three-state for addresses above 1M.

–MEMR timing shown with ROMDMA Register bit 0 = 1. –IOW and –MEMW timing shown with DMA channels programmed in extended mode.

FIGURE 52. IOCHRDY TIMING: DMA CYCLES



Notes: (*) Internal signal.

The first wait state is automatically inserted by internal circuitry for all DMA cycles. Any additional wait states must be inserted using IOCHRDY.

FIGURE 53. DMA MODE DATA STEERING: ON-BOARD MEMORY ACCESSES

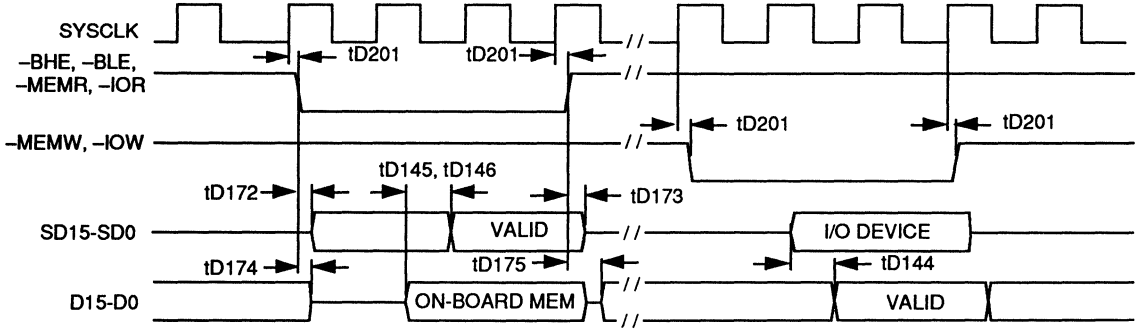


FIGURE 54. DMA MODE DATA STEERING: OFF-BOARD MEMORY ACCESSES

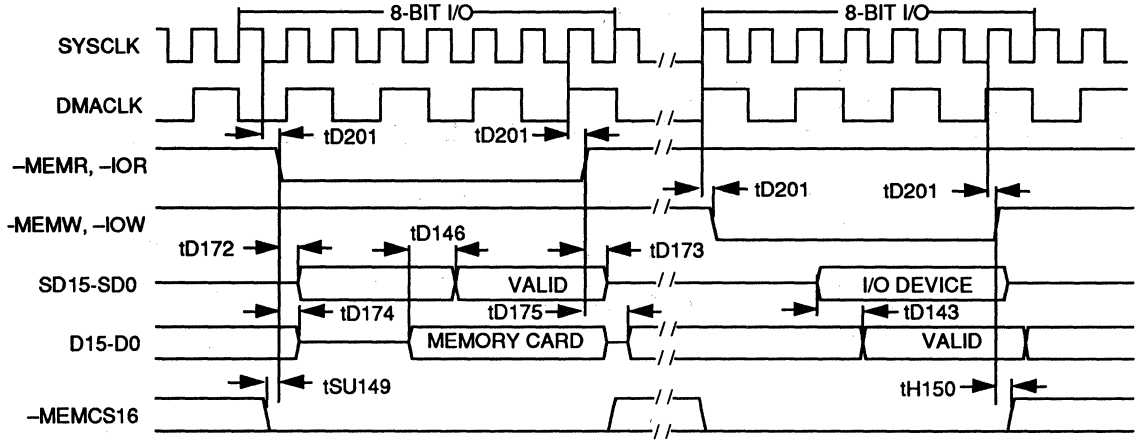
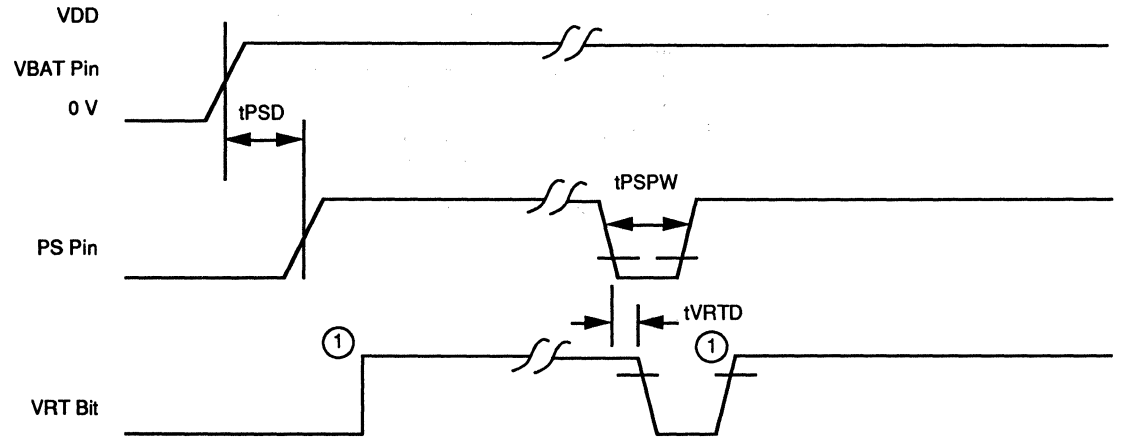


FIGURE 55. REAL-TIME CLOCK STANDBY MODE CONTROL



Notes: 1. The VRT bit is set to "1" by reading Register D. The VRT bit can only be cleared by pulling the PS pin low (see REGISTER D [$0D]).

FIGURE 56. KEYBOARD CONTROLLER INTERFACE TIMING (INTERNAL MODE)

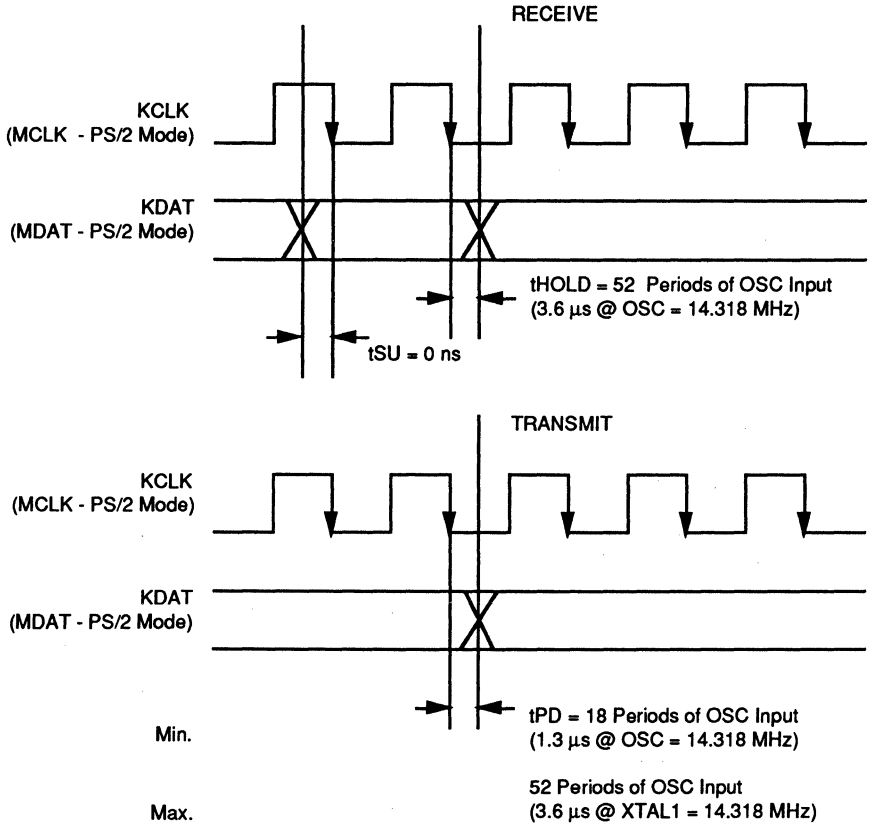


FIGURE 57. LOCAL BUS TIMING: NON-PIPELINE TO PIPELINE OPERATION

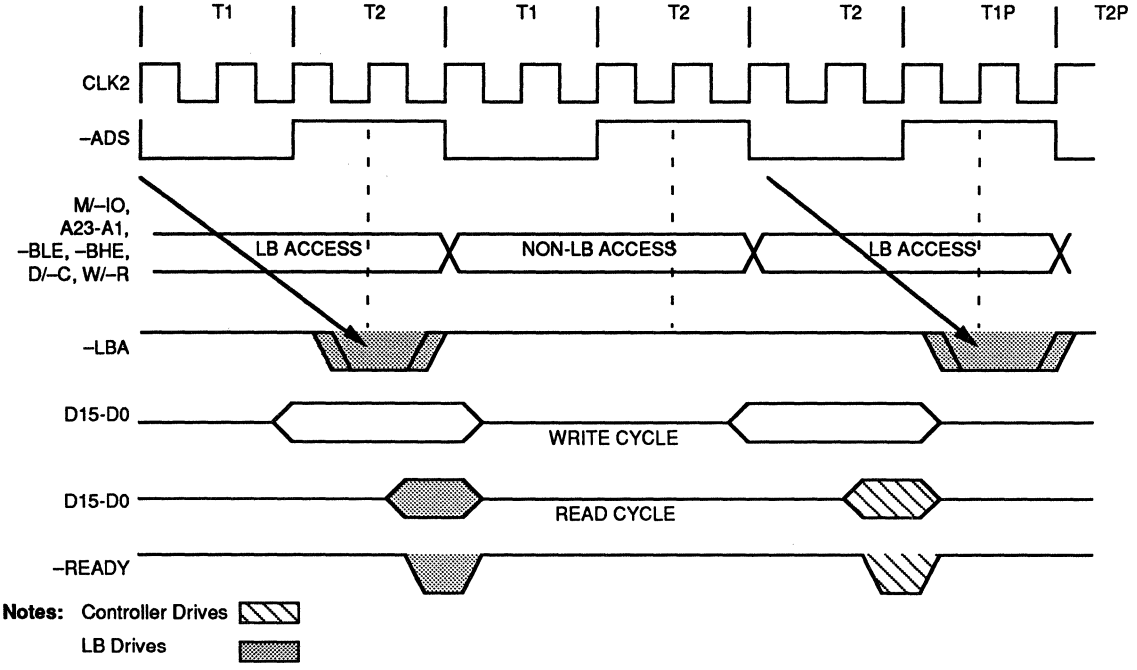


FIGURE 58. LOCAL BUS TIMING: PIPELINE TO NON-PIPELINE OPERATION

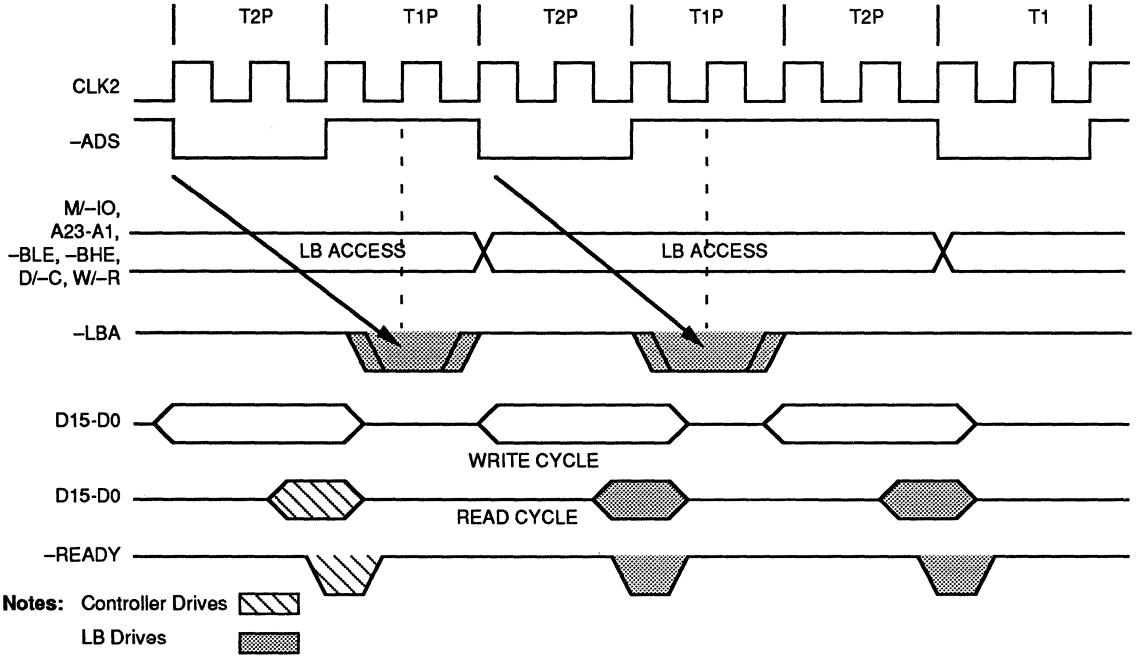
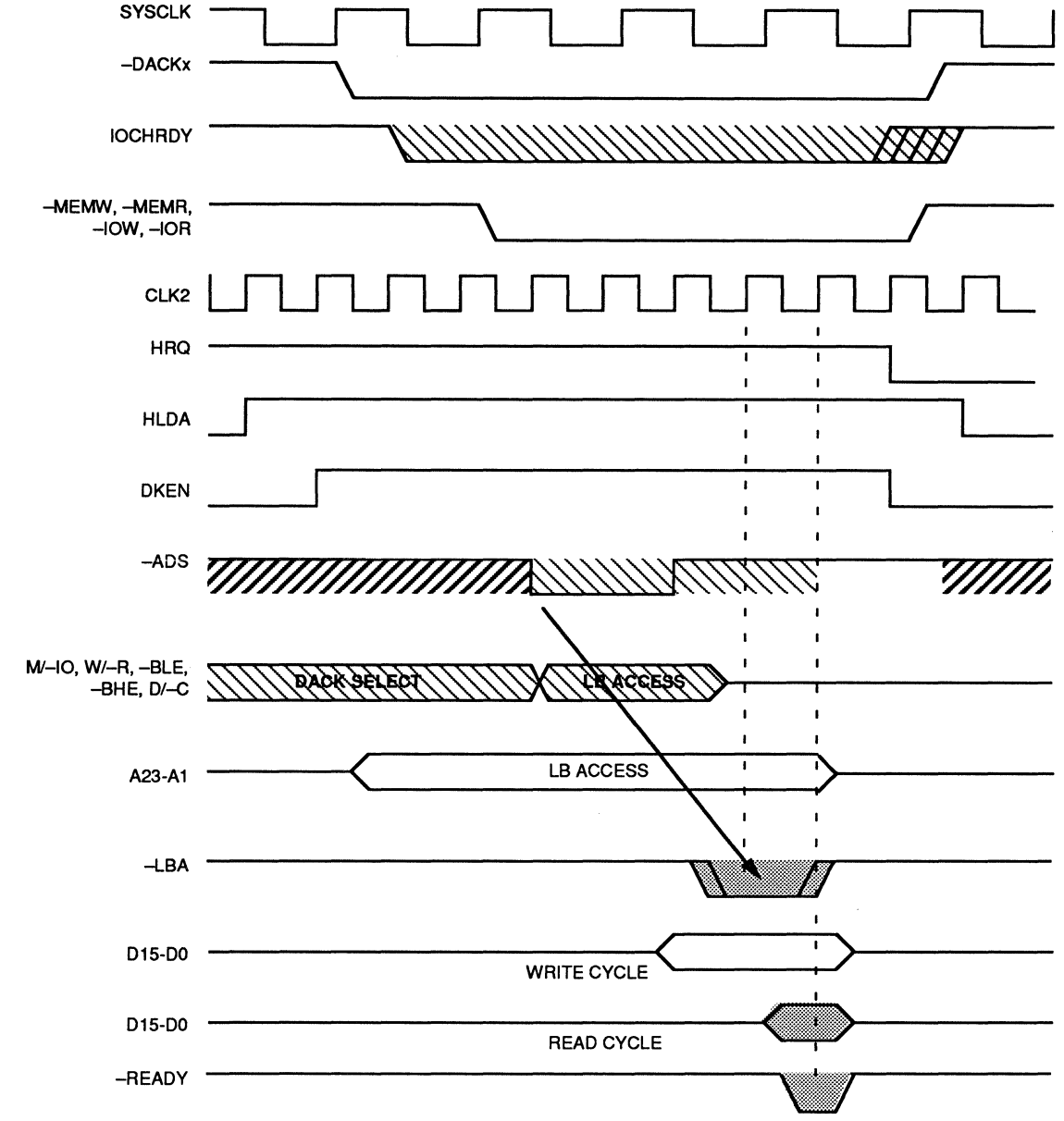


FIGURE 59. LOCAL BUS TIMING: DMA/MASTER OPERATION



Notes: Controller Drives

LB Drives

CPU Drives

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature –10°C to +70°C
Storage Temperature –65°C to +150°C
Supply Voltage to Ground –0.5 V to 7.0 V
Applied Output Voltage –0.5 V to VDD + 0.5 V
Applied Input Voltage –0.5 V to 7.0 V
Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to 70°C, VDD = 5 V ±10%, VSS = 0 V

Symbol	Parameter	Min	Max	Units	Conditions
VIL	Input Low Voltage	–0.3	0.8	V	TTL-compatible Inputs (Note 1)
VIH	Input High Voltage	2.0	VDD + 0.3	V	TTL-compatible Inputs (Note 1)
VILC	Input Low Voltage	–0.3	VDD + 0.3	V	CMOS-compatible Inputs (Note 1)
VIHC	Input High Voltage	VDD • 0.7	VDD + 0.3	V	CMOS-compatible Inputs (Note 1)
VOL1	Output Low Voltage		0.4	V	LOL = 4 mA ("4 mA" pads) (Note 1)
			0.2	V	LOL = 100 µA
VOL2	Output Low Voltage		0.4	V	LOL = 8 mA ("8 mA" pads) (Note 1)
			0.2	V	LOL = 100 µA
VOL3	Output Low Voltage		0.4	V	LOL = 12 mA ("12 mA" pads) (Note 1)
			0.2	V	LOL = 100 µA
VOL4	Output Low Voltage		0.4	V	LOL = 24 mA ("24 mA" pads) (Note 1)
			0.2	V	LOL = 100 µA
VOH1	Output High Voltage	2.4		V	LOH = –2 mA ("4 mA" pads) (Note 1)
		VDD – 0.2		V	LOL = –100 µA
VOH2	Output High Voltage	2.4		V	LOH = –4 mA ("8 mA" pads) (Note 1)
		VDD – 0.2		V	LOL = –100 µA
VOH3	Output High Voltage	2.4		V	LOH = –6 mA ("12/24 mA" pads) (Note 1)
		VDD – 0.2		V	LOL = –100 µA
ILLI	Input Leakage Current		±3	µA	0.1 V ≤ VIN ≤ VDD–0.1 V
ILO	Output Three-State Leakage Current		±5	µA	0.1 V ≤ VOUT ≤ VDD–0.1 V

DC CHARACTERISTICS: TA = 0°C to 70°C, VDD = 5 V ±10%, VSS = 0 V (CONT.)

Symbol	Parameter	Min	Max	Units	Conditions
IIPU	Input Current–Pads with Internal Pull-Up	–30.0	–500.0	µA	VIN = 0.1 V
IIPD	Input Current–Pads with Internal Pull-Down	30.0	500.0	µA	VIN = 5.5 V
IDDSB	Static Power Supply Current		225.0	µA	No DC Loads (Combined Total Measured with all Rails at VDD = 5.5 V)
IDDOP	Dynamic Power Supply Current		3.5	mA/MHz	No DC Loads-Outputs Open (Combined Total Measured with all Rails at VDD = 5.5 V)
IBAT	RTC Supply Current		4.0	µA	RTCBAT = 5.0 V at 32 kHz Oscillator Frequency
CIN	Input Capacitance		10.0	pF	FC = 1 MHz (Note 1)
			15.0	pF	CLK2IN
COUT	Output Capacitance		10.0	pF	FC = 1 MHz (Note 1)

Note 1: For pin input type, please refer to the table at the front of this document, "Pin Type by Operational State".

VDD CONNECTION OPTIONS

The VL82C316 has VDD inputs to four separately powered logic blocks. Valid VDD combinations for each of the four logic blocks are shown in the Table 67. These combinations provide the following operational modes:

- Entire chip at 5.0 V.
- ISA Bus at 5.0 V
- DRAM interface on, reset of logic off for low power Suspend Mode refresh via VL82C323 PMU.
- VL82C316 Suspend Mode refresh with CPU power on in Static Mode.
- VL82C316 Suspend Mode refresh with CPU power off.

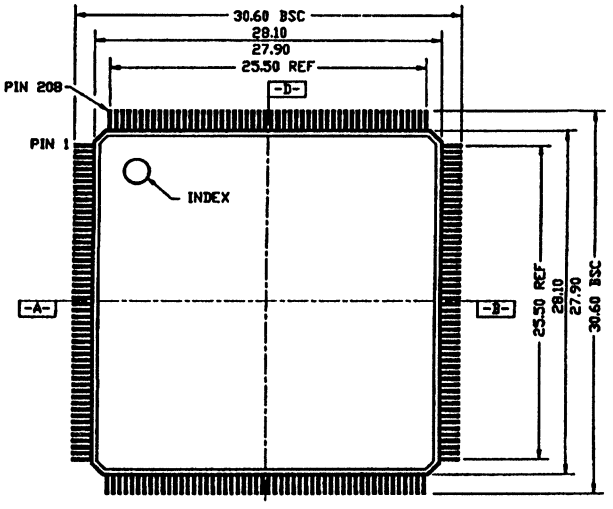
TABLE 67. VDD CONNECTIONS

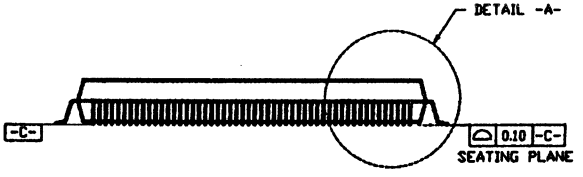
Options	Core Power (VDDIAB)	CPU Ring (VDDRA)	DRAM Ring (VDDRB)	ISA Ring & Core (VDDRC/VDDIC)	When Used
1	0	0	0	0	System Off
2	5.0	5.0	5.0	5.0	Normal On Mode or 33 MHz Static Mode
3	0	0	5.0	0	Suspend Mode, VL82C323 Refresh, 5.0 V System
4	5.0	5.0	5.0	0	VL82C316 Suspend

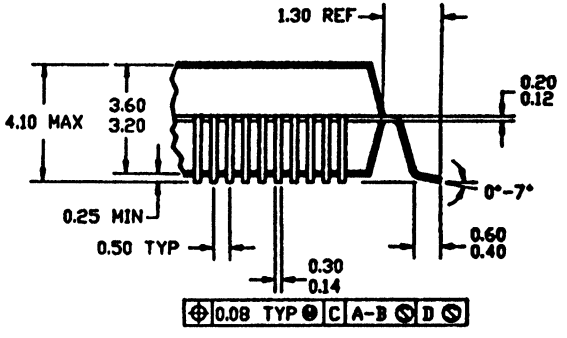
Note: When using the VL82C316's Suspend Mode, CPU/local bus On Mode, power buses remain powered per options 2 through 4. The only exception is in systems powering off ISA bus peripherals. In this case, turn off VDDRC and VDDIC.

PACKAGE OUTLINE

208-LEAD METRIC QUAD FLAT PACK (MQFP)







DETAIL -A-

Note: Dimensions are in millimeters.

NOTES:

VLSI TECHNOLOGY, INC.

VL82C323 SCAMP II 5 VOLT POWER MANAGEMENT UNIT

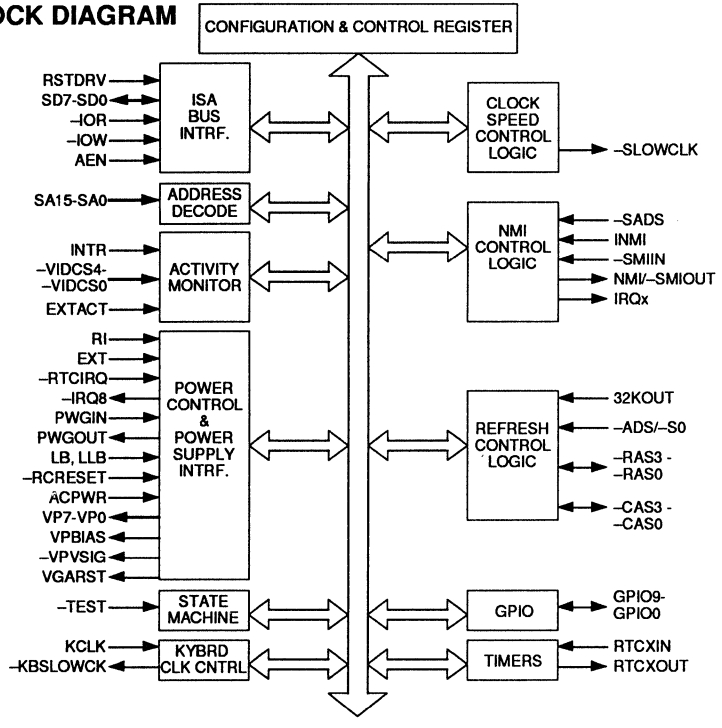
VL82C323

SCAMP™ II 5 VOLT POWER MANAGEMENT UNIT

FEATURES

- Supports X86-based PC/AT-compatible systems
- Provides system activity monitoring, peripheral control, power supply control, mode timers, and general purpose I/O for laptop/notebook power management
- Includes the logic to support X86 processors with the Systems Management Mode (SMM) feature
- Five operation modes:
  - On Mode
  - Doze Mode
  - Sleep Mode
  - Suspend Mode
  - Off Mode
- Independent programmable timers for power saving modes
- Independent programmable timers for LCD and backlight control
- Ten individual power control outputs:
  - Three for LCD power
  - Seven generai purpose for peripherals
- Two to four low battery warning monitors
- Multiple power-on sources from Suspend/Off Mode:
  - Push-button
  - Real-time clock alarm
  - Modem ring
- AC power monitoring to disable PMU function
- Suspend Mode refresh options: none, CAS-before-RAS, Self-Refresh
- Leakage control of outputs during Suspend Mode
- Wide range of LCD panel power-up/-down sequencing
- Ten general purpose I/O ports; eight with additional I/O features:
  - One programmable blinking I/O
  - Two optional low battery inputs
- Watchdog timer to turn-off system power if low battery NMI is not serviced
- Programmable interrupt generation on:
  - PMU power mode
  - Low battery warning
  - External input
  - LCD panel timer
  - Reschedule Suspend Mode Interrupt by BIOS
  - Activity detection
- Generated interrupt selectable as IRQx, NMI, or SMI
- Controls SCAMP™ I or SCAMP II (VL82C310 or VL82C316) –SLEEP pin
- Real-time clock alarm IRQ output pin for SCAMP I Controller
- 1.5-micron CMOS technology
- 100-lead (thin) metric quad flat pack (MQFP)

BLOCK DIAGRAM

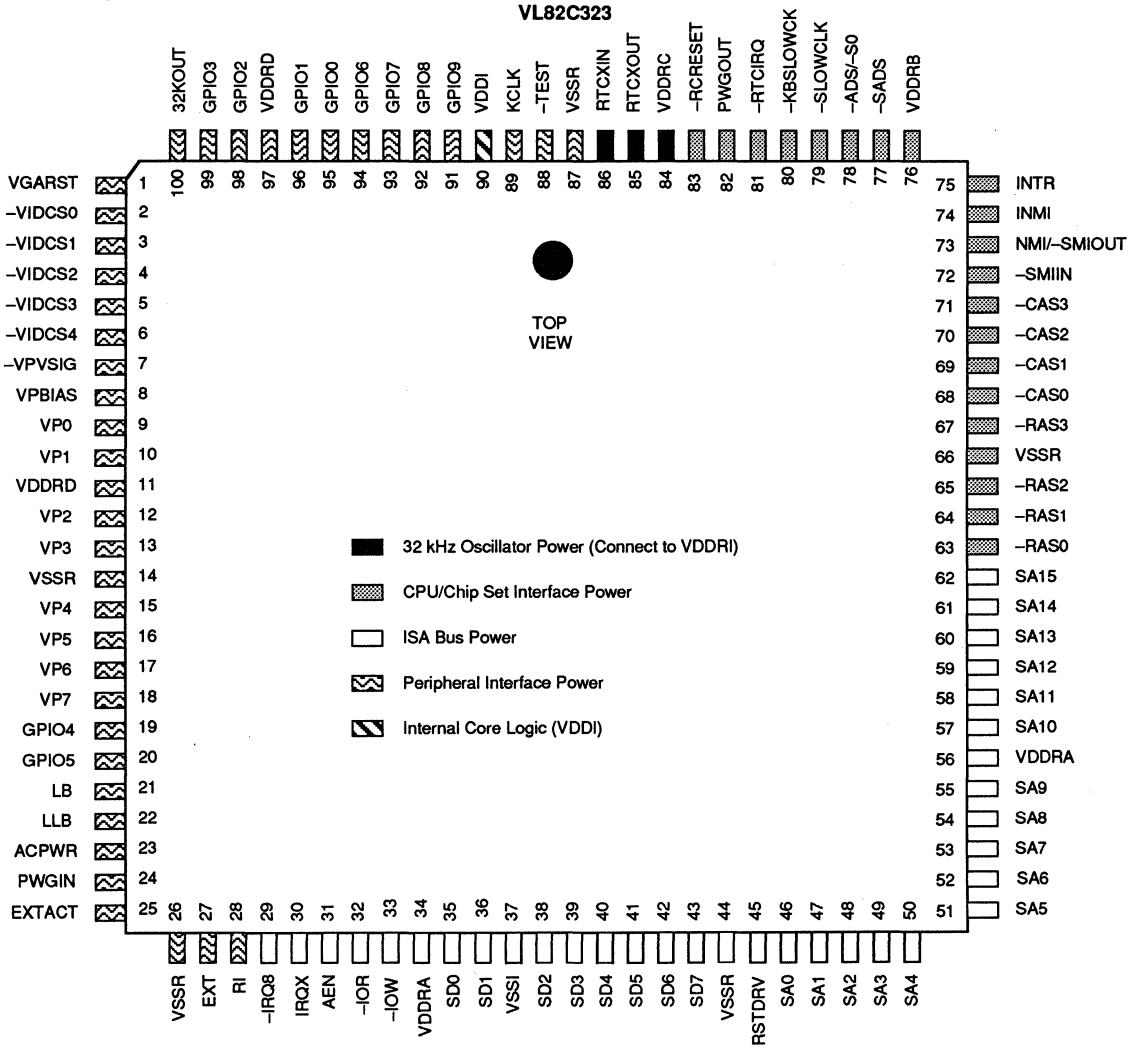


ORDER INFORMATION

Part Number	Package
VL82C323-FC	(Thin) Metric Quad Flat Pack

Note: Operating temperature range is 0°C to +70°C.

PIN DIAGRAM


VL82C323
TOP VIEW
1 VGARST
2 -VIDCS0
3 -VIDCS1
4 -VIDCS2
5 -VIDCS3
6 -VIDCS4
7 -VPVSIG
8 VPBIAS
9 VP0
10 VP1
11 VDDRD
12 VP2
13 VP3
14 VSSR
15 VP4
16 VP5
17 VP6
18 VP7
19 GPIO4
20 GPIO5
21 LB
22 LLB
23 ACPWR
24 PWGIN
25 EXTACT
26 VSSR
27 EXT
28 RI
29 -IRQ8
30 IRQX
31 AEN
32 -IOR
33 -IOW
34 VDDRA
35 SD0
36 SD1
37 VSSI
38 SD2
39 SD3
40 SD4
41 SD5
42 SD6
43 SD7
44 VSSR
45 RSTDRV
46 SA0
47 SA1
48 SA2
49 SA3
50 SA4
51 SA5
52 SA6
53 SA7
54 SA8
55 SA9
56 VDDRA
57 SA10
58 SA11
59 SA12
60 SA13
61 SA14
62 SA15
63 -RAS0
64 -RAS1
65 -RAS2
66 VSSR
67 -RAS3
68 -CAS0
69 -CAS1
70 -CAS2
71 -CAS3
72 -SMIIN
73 NMI/-SMIOUT
74 INMI
75 INTR
76 VDDRB
77 -SADS
78 -ADS/-S0
79 -SLOWCLK
80 -KBSLOWCK
81 -RTCIRQ
82 PWGOUT
83 -RCRESET
84 VDDRC
85 RTCXOUT
86 RTCXIN
87 VSSR
88 -TEST
89 KCLK
90 VDDI
91 GPIO9
92 GPIO8
93 GPIO7
94 GPIO6
95 GPIO0
96 GPIO1
97 VDDRD
98 GPIO2
99 GPIO3
100 32KOUT
32 kHz Oscillator Power (Connect to VDDRI)
CPU/Chip Set Interface Power
ISA Bus Power
Peripheral Interface Power
Internal Core Logic (VDDI)

PIN TYPE BY OPERATIONAL STATE

Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pwr Rail	Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pwr Rail
1	VGARST	O-1		8.0	D	34	VDDRA		PWR		
2	–VIDCS0	IO-3 (Note 1, 3)	TTL	12.0	D	35	SD0	IO-4	TTL	24.0	A
3	–VIDCS1	IO-3 (Note 1, 3)	TTL	12.0	D	36	SD1	IO-4	TTL	24.0	A
4	–VIDCS2	IO-3 (Note 1, 3)	TTL	12.0	D	37	VSSI		GND		
5	–VIDCS3	IO-3 (Note 1, 3)	TTL	12.0	D	38	SD2	IO-4	TTL	24.0	A
6	–VIDCS4	IO-3 (Note 1, 3)	TTL	12.0	D	39	SD3	IO-4	TTL	24.0	A
7	–VPVSIG	O-1		8.0	D	40	SD4	IO-4	TTL	24.0	A
8	VPBIAS	O-1		8.0	D	41	SD5	IO-4	TTL	24.0	A
9	VP0	O-1		8.0	D	42	SD6	IO-4	TTL	24.0	A
10	VP1	O-1		8.0	D	43	SD7	IO-4	TTL	24.0	A
11	VDDRD		PWR			44	VSSR		GND		
12	VP2	O-1		8.0	D	45	RSTDRV (Note 2)	IO-1	TTL	8.0	A
13	VP3	O-1		8.0	D	46	SA0 (Note 2)	IO-1	TTL	8.0	A
14	VSSR		GND			47	SA1 (Note 2)	IO-1	TTL	8.0	A
15	VP4	O-1		8.0	D	48	SA2 (Note 2)	IO-1	TTL	8.0	A
16	VP5	O-1		8.0	D	49	SA3 (Note 2)	IO-1	TTL	8.0	A
17	VP6	O-1		8.0	D	50	SA4 (Note 2)	IO-1	TTL	8.0	A
18	VP7	O-1		8.0	D	51	SA5 (Note 2)	IO-1	TTL	8.0	A
19	GPIO4	IO-3 (Note 1)	TTL	12.0	D	52	SA6 (Note 2)	IO-1	TTL	8.0	A
20	GPIO5	IO-3 (Note 1)	TTL	12.0	D	53	SA7 (Note 2)	IO-1	TTL	8.0	A
21	LB	I (Note 1)	TTL		D	54	SA8 (Note 2)	IO-1	TTL	8.0	A
22	LLB	I (Note 1)	TTL		D	55	SA9 (Note 2)	IO-1	TTL	8.0	A
23	ACPWR	I (Note 1)	TTL		D	56	VDDRA		PWR		
24	PWGIN	I (Note 1)	CMOS-S		D	57	SA10 (Note 2)	IO-1	TTL	8.0	A
25	EXTACT	I (Note 1)	TTL		D	58	SA11 (Note 2)	IO-1	TTL	8.0	A
26	VSSR		GND			59	SA12 (Note 2)	IO-1	TTL	8.0	A
27	EXT	I (Note 1)	TTL		D	60	SA13 (Note 2)	IO-1	TTL	8.0	
28	RI	I (Note 1)	CMOS-S		A	61	SA14 (Note 2)	IO-1	TTL	8.0	A
29	–IRQ8	O-1		8.0	A	62	SA15 (Note 2)	IO-1	TTL	8.0	A
30	IRQx	O-1		8.0	A	63	–RAS0	IO-2	TTL	12.0	B
31	AEN (Note 2)	IO-1	TTL	8.0	A	64	–RAS1	IO-2	TTL	12.0	B
32	–IOR (Note 2)	IO-1	TTL	8.0	A	65	–RAS2	IO-2	TTL	12.0	B
33	–IOW (Note 2)	IO-1	TTL	8.0	A	66	VSSR		GND		

PIN TYPE BY OPERATIONAL STATE (Cont.)

Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pwr Rail	Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pwr Rail
67	–RAS3	IO-2	TTL	12.0	B	84	VDDRC		PWR		
68	–CAS0	IO-2	TTL	12.0	B	85	RTCXOUT	O			C
69	–CAS1	IO-2	TTL	12.0	B	86	RTCXIN	I	CMOS		C
70	–CAS2	IO-2	TTL	12.0	B	87	VSSR		GND		
71	–CAS3	IO-2	TTL	12.0	B	88	–TEST	I-PU	TTL		D
72	–SMIIN	I	CMOS-S		B	89	KCLK	IO-3 (Note 1, 3)	CMOS	12.0	D
73	NMI/–SMIOUT	O-1		8.0	B	90	VDDI		PWR		
74	INMI (Note 2)	IO-1	TTL	8.0	B	91	GPIO9	IO-2	TTL	12.0	D
75	INTR (Note 2)	IO-1	TTL	8.0	B	92	GPIO8	IO-2	TTL	12.0	D
76	VDDRB		PWR			93	GPIO7	IO-3 (Note 1)	TTL	12.0	D
77	–SADS (Note 2)	IO-1	TTL	8.0	B	94	GPIO6	IO-3 (Note 1)	TTL	12.0	D
78	–ADS/–S0 (Note 2)	IO-1	TTL	8.0	B	95	GPIO0	IO-2	TTL	12.0	D
79	–SLOWCLK	O-1	TTL	8.0	B	96	GPIO1	IO-2	TTL	12.0	D
80	–KBSLOWCK	O-1		8.0	B	97	VDDRD		PWR		
81	–RTCIRQ	I	TTL		B	98	GPIO2	IO-2	TTL	12.0	D
82	PWGOUT	O-1		8.0	B	99	GPIO3	IO-2	TTL	12.0	D
83	–RCRESET	I	CMOS-S		B	100	32KOUT	O-1		8.0	D

Notes: 1. These inputs have no P-diodes.

2. These pins are outputs only when the VL82C323 is in the Suspend or Off Modes.

3. These pins are outputs only when the VL82C323 is in the Off Mode.

Legend:

CMOS	CMOS-compatible input
GND	A ground pin
I	Input-only pin
IO	Bidirectional pin
PU	Indicates a high-impedance with approximately 10 kΩ minimum resistance to VDD.
PWR	A power supply pin
TTL	TTL-compatible input
-S	Indicates a Schmitt-trigger input with hystersis for noise immunity.
-1	Pad type with 8.0 mA drive.
-2	Pad type with 12.0 mA drive.
-3	Pad type with 12.0 mA drive plus Note 1 above.
-4	Pad type with 24.0 mA drive.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
VGARST	1	VGA Reset - An output signal that is sent to the VGA controller's reset input.
–VIDCS4 - –VIDCS0	6-2	Video Controller Chip Select bits 4 through 0 - These are the VGA controller write enable signals. They lack P-diodes on the inputs and may be driven above the VDDRD power supply level.
–VPVSIG	7	Video Power Signal - An active low, open drain output signal used to control the LCD clock and data buffer.
VPBIAS	8	Video Power Bias - This power control output signal is used for controlling the LCD display's bias power. Its polarity is the same as VP0.
VP0	9	Video Power bit 0 - This power control output signal is used for controlling the LCD panel power. Its polarity is determined by the Polarity Register.
VP1	10	Video Power bit 1 - This power control signal is used for controlling the LCD backlight power. Its polarity is determined by the Polarity Register.
VP7-VP2	18-15, 13, 12	Video Power bits 7 through 2 - These power control signals are used for controlling user selected power. Their polarity is determined by the Polarity Register.
LB	21	Low Battery - An active high input signal from the power supply to the VL82C323 that indicates the battery level is low. It is the first low-level battery warning signal. This input has no P-diode and may be driven above the VDDRD power supply level.
LLB	22	Low Low Battery - An active high input signal from the power supply to the VL82C323 that indicates the battery level is low. It is the second low-level battery warning signal. This input has no P-diode and may be driven above the VDDRD power supply level.
ACPWR	23	AC Power - An input signal from the power supply that informs the VL82C323 that the system is running on AC power. When this signal is high, the VL82C323 disables Doze, Sleep, and LCD Timers which in turn disables the automatic hardware power saving features. This input has no P-diode and may be driven above the VDDRD power supply level.
PWGIN	24	Power Good - An input signal from the power supply to the VL82C323 that indicates that the power is stable. This input has no P-diode and may be driven above the VDDRD power supply level.
EXTACT	25	External Activity - On the rising edge of this input signal the VL82C323 will exit from the Doze or Sleep Mode, or generate an interrupt. It has no effect in the On Mode. This input has no P-diode and may be driven above the VDDRD power supply level.
EXT	27	External Wake-up - This active high input signal is intended for use with an external push-button switch. A rising edge on this input while the VL82C323 is not in the Suspend or Off Modes will generate an interrupt. This input has no P-diode and may be driven above the VDDRD power supply level.
RI	28	Ring Indicator - This active high input signal is intended for use with an external modem. The VL82C323 puts the system into the On Mode when it detects a pre-programmed number of transitions while in the Suspend or Off Modes. This input has no P-diode and may be driven above the VDDRD power supply level.
–IRQ8	29	RTC Interrupt Request - An output signal regenerated by the VL82C323 from the VL82C107 Combination I/O chip and sent to VL82C310. In systems using the VL82C316 SCAMP Controller, this signal is not connected; the RTC is built into the VL82C316.
IRQx	30	Interrupt Request output. This signal may be connected to any unused IRQ output. IRQ15 is a popular choice.
AEN	31	Address Enable - System bus address enable signal from the system bus. This pin is an output only when the VL82C323 is in the Suspend or Off Modes.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
–IOR	32	I/O Read - A command generated by the VL82C310 or VL82C316 SCAMP Controller and sent to the VL82C323. This pin is an output only when the VL82C323 is in the Suspend or Off Modes.
–IOW	33	I/O Write - A command generated by the VL82C310 or VL82C316 SCAMP Controller and sent to the VL82C323. This pin is an output only when the VL82C323 is in the Suspend or Off Modes.
SD7-SD0	43-38, 36, 35	System Data bus bits 7 through 0 - This bus connects directly to the VL82C310 or VL82C316 SCAMP Controller's system data bus and used to transfer data between the two.
RSTDRV	45	Reset Drive - The system reset input from the system bus. This pin is an output only when the VL82C323 is in the Suspend or Off Modes.
SA15-SA0	62-57, 55-46	System Address bus bits 15 through 0 - System address lines from the VL82C310 or VL82C316 SCAMP Controller. This pin is an output only when the VL82C323 is in the Suspend or Off Modes.
–RAS3 - –RAS0	67, 65-63	DRAM Row Address Strobe bits 3 through 0 - These signals are wired OR with the –RAS lines from the VL82C310 or VL82C316 SCAMP Controller. They are driven by the VL82C323 only in the Suspend Mode and three-state when they are not in the Suspend Mode. The SCAMP Controller three-states these signals in the Suspend Mode. If unconnected or not driven, these signals must be pulled up to VDDRB.
–CAS3 - –CAS0	71-68	DRAM Column Address Strobe bits 3 through 0 - These signals are wired OR with –CAS lines from the VL82C310 or VL82C316 SCAMP Controller. These signals are driven by the VL82C323 only in the Suspend Mode and three-state when they are not in the Suspend Mode. The SCAMP Controller three-states these signals in the Suspend Mode. If unconnected or not driven, these signals must be pulled up to a supply which collapses in the Suspend Mode.
–SMIIN	72	System Management Interrupt Input - An input to the VL82C323 from a connected shared –SMI line with the CPU and VL82C316 SCAMP II Controller.
NMI/–SMIOUT	73	Non-Maskable Interrupt or System Management Interrupt Output – This pin is a dual function pin. Depending upon the desired function, it can be either an NMI output to the CPU or an –SMI output to the VL82C316 SCAMP II Controller.
INMI	74	Input Non-Maskable Interrupt - An input from the from VL82C310 or VL82C316 SCAMP Controller to the VL82C323 that reports PC/AT standard NMIs. This pin is an output only when the VL82C323 is in the Suspend or Off Modes.
INTR	75	Interrupt Request - An active high input that is used to interrupt the CPU. It is generated by the VL82C310 or VL82C316 SCAMP Controller and sent to both the CPU and VL82C323. This pin is an output only when the VL82C323 is in the Suspend or Off Modes.
–SADS	77	SMI Address Strobe - A signal generated by the VL82C316 SCAMP Controller that is used to latch CPU addresses during accesses to SMI address space. A falling edge on this signal causes –SMIOUT to go high. This pin is an output only when the VL82C323 is in the Suspend or Off Modes.
–ADS/–S0	78	Address Strobe or S0 - Connect to the –ADS input if the CPU is a 386. Connect to –S0 input if the CPU is a 286. This pin is an output only when the VL82C323 is in the Suspend or Off Modes.
–SLOWCLK	79	Slow Clock - This input signal is the CPU clock speed control signal to VL82C310 or VL82C316 SCAMP Controller. When –SLOWCLK is low, the SCAMP Controller reduces the CPU clock speed to its the programmed divided clock speed.
–KBSLOWCK	80	Keyboard Slow Clock - An output signal that controls the keyboard clock. When low, the VL82C107 SCAMP Combination I/O chip stops the keyboard clock. When high, the VL82C107 starts the keyboard clock.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
–RTCIRQ	81	RTC Interrupt Request - A signal generated by the VL82C107 SCAMP Combination I/O chip and sent to the VL82C323. If the VL82C323 is in either the Suspend or Off Modes and detects any transition on this pin, it puts the system into the On Mode.
PWGOUT	82	Power Good Output - An output signal from the VL82C323 sent to the VL82C310 or VL82C316 SCAMP Controller informing the Controller that the power is good.
–RCRESET	83	RC Reset - External RC reset signal to reset the VL82C323 itself when its power is first applied.
RTCXOUT	85	32 kHz clock feedback.
RTCXIN	86	32 kHz input from the crystal.
–TEST	88	Reserved for testing the VL82C323 (internal pull-up).
KCLK	89	Keyboard Clock - Keyboard clock input from keyboard. When a transition is detected on this signal, the VL82C323 drives –KBSLOWCK high to enable the clock to the keyboard controller.
GPIO9-GPIO0	91-94, 20-19, 99, 98, 96-95	General Purpose Input/Output bits 9 through 0 - General purpose I/O low battery NMI warning option. Note that GPIO7-GPIO4 have no P-diodes and may be driven above the VDDRD power supply level when used as inputs. If used as outputs, an external pull-up resistor is required on GPIO7-GPIO4.
32KOUT	100	Refresh clock for VGA controller in the Suspend Mode.
VDDRA	34, 56	ISA bus interface power.
VDDRB	76	System interface power. Must be the same as VDDI.
VDDRC	84	32 kHz oscillator power. Connects to the same supply as VDDI, but should be separately filtered.
VDDRD	11, 97	Peripheral supply voltage. See the section titled "Operating Voltage Options" under DC Characteristics for additional information.
VDDRI	90	Core logic power.
VSSI	37	Core Logic ground reference.
VSSR	14, 26, 44 66, 87	Pad ring ground reference for VDDRA, VDDRB, VDDRC and VDDRD.

FUNCTIONAL DESCRIPTION

The VL82C323 SCAMP Power Management Unit (PMU) is intended to be used in conjunction with the VL82C310 SCAMP I System Controller or VL82C316 SCAMP II 5 Volt Power-Managed 386SX Controller and the VL82C107 SCAMP Combination I/O chip. The VL82C323 PMU dramatically reduces overall system power consumption and provides special features for laptop/notebook PC/AT-compatible computers. The power reduction is accomplished via an activity monitor which detects inactivity in the system, and reduces the CPU clock frequency and/or removes power from peripheral devices.

The VL82C323 has five operation modes:

- On Mode
- Doze Mode
- Sleep Mode
- Suspend Mode
- Off Mode

By monitoring the system activity, the VL82C323 switches between modes to achieve power saving without impacting system performance. The VL82C323 also provides an auto power-on feature to turn-on the system power via a push-button switch, modem ring indicator, or real-time clock time of day alarm.

The VL82C323 supports a suspend/resume function in conjunction with the BIOS to allow the user to turn the system power off and save the system information from the current application. When the system power is turned back on, the user is able to resume the application from the point where it was suspended.

PC/AT BUS INTERFACE

The VL82C323 resides on the ISA bus. The control signals –IOR, –IOW, and AEN are used to interface to the VL82C310 or VL82C316 SCAMP Controllers (here after referred to as SCAMP Controller unless specifying an individual device). The SCAMP Controller presents the address and data on the SA and SD buses and ISA bus control signals for all I/O cycles. The VL82C323 is tied to SA15-SA0 and SD7-SD0 buses. The VL82C323 constantly monitors SA15-SA0. If an access of the VL82C323's internal registers occur, the VL82C323 either places the data on SD7-SD0 while –IOR is asserted for an I/O read operation or it latches the data at the rising edge of the –IOW for an I/O write operation. The VL82C323 does not drive the –IOCHRDY signal so the SCAMP Controller uses its programmed number of I/O wait modes to terminate the bus cycle. The VL82C323 fully decodes SA15-SA0.

SCAMP CONTROLLER AND VL82C107 COMBINATION I/O INTERFACE

Clock Switching

The VL82C323 controls the CPU clock speed via the –SLOWCLK pin of the SCAMP Controller if the SCAMP Controller has its Sleep Mode enabled. When the VL82C323 is in the Doze or Sleep Mode, it drives the –SLOWCLK signal low. The SCAMP Controller slows down the clock when it detects a transition from high-to-low on its –SLOWCLK input pin. When it detects a transition from low-to-high, it speeds up to the maximum programmed CPU clock speed. The –SLOWCLK signal is a glitch-free signal and provides a 250 ns minimum pulse width. The frequency of the slow clock depends on the minimum speed of the CPU and can be set by the BIOS during system initialization in the Configuration Registers of the SCAMP Controller.

Please refer to the VL82C310 and VL82C316 SCAMP Controller data manuals for detailed information. Normally, the slow clock frequency is set to the minimum clock speed the CPU will support, i.e., 2 MHz for 386SX-LP and 4 MHz for 386DX.

The VL82C323 drives the –SLOWCLK pin high without exiting the Doze or Sleep Mode for an INTR. It pushes each interrupt occurrence on an internal Stack Register and an end-of-interrupt (EOI) instruction pops each interrupt occurrence from the stack to prevent multiple nested interrupts from slowing the CPU clock until the last EOI. The depth of the stack is 15 deep. When the last EOI is received, the VL82C323 waits for 15 to 30 µs before it drives the –SLOWCLK pin low. This forces the SCAMP Controller back into slow CPU clock operation. The VL82C323 flushes the stack if the AUTOFLUSH bit (bit 6) in the MISCSET Register is set and the VL82C323 enters the On Mode from the Doze or Sleep Mode. If the FLUSH bit (bit 5) in the MISCSET Register is set, the stack operation is disabled and the VL82C323 drives the –SLOWCLK pin low 15 to 30 µs after any EOI. The SCAMP Controller switches to maximum CPU clock speed for DMA or refresh operations automatically. If the –SLOWCLK pin is switched from high-to-low during a DMA operation, the SCAMP Controller waits for the completion of the DMA cycle and then slows down the CPU clock.

If the MSK_VIDM bit (bit 6) in the ACTMASK Register is set, any low transition on the –VIDCS inputs (–VIDCS4 - –VIDCS0) is not treated as an activity detection. The VL82C323 temporarily brings the –SLOWCLK pin high for 8 ms without exiting from the Doze or Sleep Mode. If the MSK_VIDM bit is reset, any low transition on the –VIDCS inputs causes an activity detection. Please refer to the section titled "System Activity Monitor" for more information.

At the end of any NMI service routine, the BIOS writes any data to the NMICAUSE-I Register. The VL82C323 then waits for 15 to 30 µs and drives the –SLOWCLK pin low, restoring slow CPU clock speed. If the BIOS fails to do so, eventually an EOI occurs in response to a Doze Timer interrupt and the VL82C323 brings the –SLOWCLK pin low at that time.

If the EN_HICLK bit (bit 0) in the MISCSET Register is set, the –SLOWCLK and –KBSLOWCK pins stay high but the VL82C323 enters the Doze and Sleep Modes. However, the CPU clock remains at high speed but some unused peripheral devices can still be turned off. This is for the calculation intensive application programs.

If the ACPWR signal is high, the Doze Timer is disabled and the power management function via the internal hardware timer scheme is disabled. However, the Doze or Sleep Modes are still available by a command to the Status Register.

VL82C323 Registers
The VL82C323's internal registers are accessed by an indexed address and data register scheme which is compatible with the SCAMP Controller. The index value is first written to the Index Register (ECh) and the data is read or written from the Data Register (EDh). The Index Register is a read/write register. When reading the Index Register, the SCAMP Controller returns the value to the CPU. The Index Register is a write-only register in the VL82C323.

The VL82C323's register range is from C0h to DFh. Write access to the Data Registers is locked out when entering the Suspend and Off Modes, and when power is first applied to the VL82C323. Bit 0 (LOCKOUT) in the Supply Register is set to indicate that a write access is not allowed. To unlock it for a write access, the CPU must first read the Supply Register. Once the write access is unlocked, the VL82C323 stays unlocked until it enters either the Suspend or Off Mode, or when –RCRESET is asserted.

RTC –IRQ8 Interrupt Handling in a VL82C310/VL82C107 System
The VL82C323 can be placed into the On Mode by the real-time clock's (RTC) time of day interrupt. The –RTCIRQ pin is an edge sensitive input from the VL82C107 SCAMP Combination I/O chip. In the Suspend Mode, the system power is off and the RTC logic in the VL82C107 and VL82C323 remains powered. In order to prevent leakage through the unpowered VL82C310, the –RTCIRQ signal from the VL82C107 is connected to the VL82C323. The VL82C323 will regenerate the –IRQ8 signal to the VL82C310 from the VL82C107 in normal operation. An external pull-up resistor is required on the –RTCIRQ input pin of the VL82C323 because the VL82C107 uses an open drain output buffer for –RTCIRQ.

Note: The above discussion only applies to use of the VL82C323 in a VL82C310/VL82C107-based system. The RTC is built into the VL82C316. In systems using the VL82C316, the VL82C323's –IRQ8 output signal is not connected to the VL82C316 and leakage control of this signal is not an issue. However, the –RTCIRQ output of the VL82C316 is connected to the VL82C323's –RTCIRQ input to support the time of day wake-up feature.

Keyboard Clock Control
To further reduce power consumption, the VL82C323 controls the keyboard clock in the VL82C107 through two control signals, –KBSLOWCK and KCLK. When the VL82C323 is in either the Doze or Sleep Mode, it drives the –KBSLOWCK signal low and the VL82C107 stops the clock to the keyboard controller. Only when the VL82C323 detects a high-to-low transition on the KCLK signal from the keyboard or an access to the port 60h or 64h occurs, does it drive –KBSLOWCK high for 0.5 to 1.0 seconds, activating the keyboard controller. Any activity other than a keyboard access does not cause the –KBSLOWCK signal to go high unless the VL82C323 returns to the On Mode. The –KBSLOWCK signal is a glitch-free signal and provides a 142 ns minimum width pulse.

Note: The VL82C316 does not have a –KBSLOWCK input. Rather it emulates the above feature internally and provides more advanced and programmable capabilities.

POWER SUPPLY INTERFACE
The VL82C323 controls the power to individual system devices to achieve maximum power savings. It is designed to interface to an intelligent power supply. To take full advantage of the VL82C323's features, the power supply should have the following features.

Power Control Signals
The LB and LLB input signals are used to report low battery conditions. The VL82C323 has ten power control output signals: VP7-VP0, VPBIAS, and –VPVSIG. VP7-VP2 are general purpose power control outputs. VP1 is used to control the LCD backlight power. VP0 is used to control the LCD panel power. VPBIAS is used to control the LCD bias power and –VPVSIG is used to control the LCD clock and data buffer. PWGIN is an input signal from the power supply indicating that the power is good. PWGOUT is an output signal to the SCAMP Controller. ACPWR is an input signal from the power supply to indicate the system is running on AC power. Figure 1 shows how the power supply interfaces to the VL82C323.

LCD Panel Power-Up/Down Sequencing
Most LCD panels have a +5 volt power supply and a bias power supply. These power sources, along with the clock and data lines to the LCD panel, are required to be sequenced correctly to prevent damage to the LCD panel. In addition, isolation must be provided between the LCD controller and the LCD panel to prevent destructive CMOS latch-up when power is applied. The VP0, VPBIAS, and –VPVSIG signals are provided to serve this purpose.

Warning: Improper LCD power sequencing may cause LCD panel damage.

The polarity of VPBIAS and VP0 are controlled by bit 0 in the Polarity Register. The polarity of –VPVSIG is defined to be active low for power-on, and is not programmable.

VP0 is active when bit 0 is set in the PWR Register for the currently active mode, and (in most cases) when the LCD Timer has not timed out.

When power is first applied to the VL82C323, –RCRESET clears the EN_LCDSEQ, LCDTMG0, and LCDTMG1 bits (bits 4-2) in the MISCSET Register, and sets the MSK_LCD bit (bit 1) in the NMIMASK-II Register. This selects the BIOS LCD power sequencing. VP0 and VPBIAS are active high, –VPVSIG is active low and all are inactive or in the Off Mode. From this point, LCD power sequencing may be done either by the BIOS directly manipulating these signals or automatically by the VL82C323 in the Automatic LCD Power Sequence Mode.

Automatic LCD Power Sequence Mode:
This is the simplest method and should be used when the panel timing requirements can be satisfied by the VL82C323.

The Automatic LCD Power Sequence Mode is enabled by setting the EN_LCDSEQ bit in the MISCSET

Register. When set, VP0, VPBIAS, and –VPVSIG become automatically sequenced outputs and can not be directly controlled by software. The LCDTMG1 and LCDTMG0 bits of the MISCSET Register specify a power sequencing delay time (see Table 16 for more information). VP0 must remain inactive while these bits are programmed, otherwise the VPBIAS and –VPVSIG outputs change state. The initial conditions must be:

1) EN_LCDSEQ, LCDTMG1, and LCDTMG0 are low,
2) the D0 bits in the PWRON and PWRDOZE Registers are low (automatic sequencing disabled, VP0, VPBIAS, and –VPVSIG off).

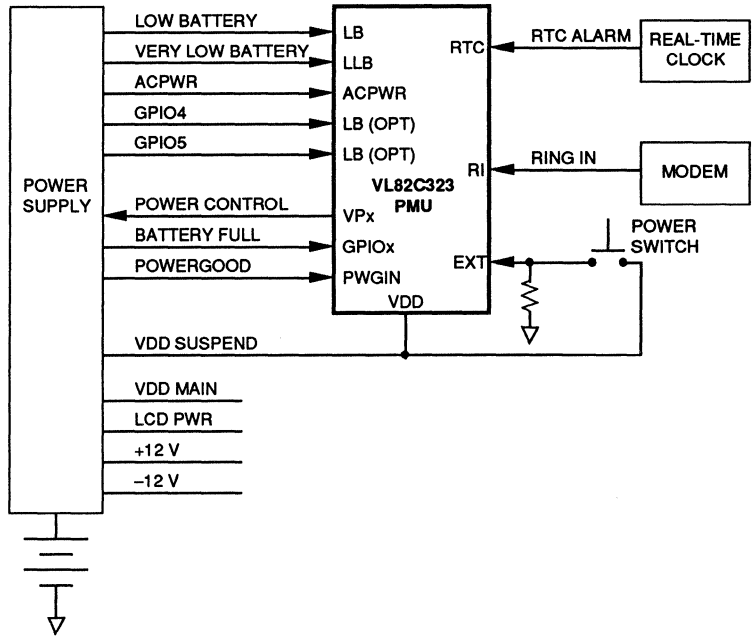
First, EN_LCDSEQ is set. Then LCDTMG1 and LCDTMG0 are set to the desired delay time. Finally, the D0 bits in the PWRON and PWRDOZE Registers are set to allow the display to turn-on in the On or Doze Modes while the LCD Timer has not timed out. Next, VP0 goes active, –VPVSIG goes active after the programmed delay and after another equal delay, VPBIAS goes active. When the display is to be powered down, VPBIAS goes inactive. Then after the delay, –VPVSIG goes inactive, and after another delay VP0 goes off. If the Automatic LCD Power Sequence Mode is enabled when the VL82C323 enters either the Suspend or Off Mode, the LCD sequentially turns off.

BIOS Controlled LCD Power Sequencing

This method is only for special displays that can not be handled with the Automatic Sequence Mode. The BIOS has direct control over the VP0, –VPVSIG, and VPBIAS signals. After –RCRESET, VP0 is controlled normally by the appropriate PWR Register's D0 bit. –VPVSIG and VPBIAS can be activated by setting the LCDTMG1 and LCDTMG0 bits in the MISCSET Register high. To make practical use of this hardware, the BIOS must enable some NMIs.

If the MSK_LCD bit (bit 1) in the NMIMASK-II Register is cleared, the LCD Timer no longer affects VP0. When it times out, it generates an NMI and the BIOS can then control VP0, –VPVSIG and VPBIAS in the proper order and timing. Of course, one or more activity detection NMIs should also be enabled so that the BIOS can turn the LCD back on again. If the EN_LCDSEQ bit is low, the LCDTMG1 and LCDTMG0 bits are cleared when the VL82C323 enters the Off Mode. Figure 2 shows the LCD power sequencing/isolation circuitry.

FIGURE 1. POWER SUPPLY INTERFACE



PMU Reset and Initialization

The VL82C323 requires the –RCRESET input signal to reset itself when power is first applied to it. This signal is generated from an external RC network so a Schmitt-trigger input is used. The resistor should be a 100 kΩ pull-up tied to the VL82C323's VDD, and the capacitor should be a 1.0 µF connected to VSS. The RC network must tie to the same power source as the VL82C323. The PWGIN signal does not affect the initialization of the VL82C323. After the internal registers are written by the CPU, the information remains the same regardless of assertion or deassertion of the PWGIN signal, until a low on the –RCRESET pin is detected or the registers are rewritten by the CPU.

AC Power Monitoring

The ACPWR input informs the VL82C323 that the system is running on AC power. If the ACPWR signal is high, the VL82C323 disables the Doze, Sleep, and LCD Timers which in turn, disables the automatic hardware power saving features. Since these timers are disabled, the system is running at maximum speed and peripheral devices are not turned off. Only the BL Timer is enabled for controlling the LCD backlight. Once the BL backlight is turned off, it is turned back on by any keyboard activity. However, all the power saving features may still be controlled by software when AC power is applied.

Low Battery Warning

The battery condition can be monitored by the power supply or by an external voltage comparison circuit. The VL82C323 has two dedicated pins, LB and LLB, to monitor the battery level. LB is the first-level low battery warning signal. LLB is a very low level battery warning. If a low battery input is high, and the corresponding NMI is unmasked, the VL82C323 will generate an NMI every 15 seconds. The BIOS can

flash a warning message on the screen, turn-on a low battery indicator, or save the current application and command the VL82C323 to enter the Suspend Mode. The VL82C323 also has two additional GPIO pins that can be programmed as low battery inputs for more levels of battery condition detection. The low battery inputs are debounced. To be recognized, these inputs must be high for two to four seconds if the FASTDB bit (bit 7) in the MISCSET Register is cleared, or 30 to 60 ms if the FASTDB bit is set. See the sections titled "LB, LLB NMI" and "GPI04 and GPIO5/LB1 and LB2 NMI" for more information.

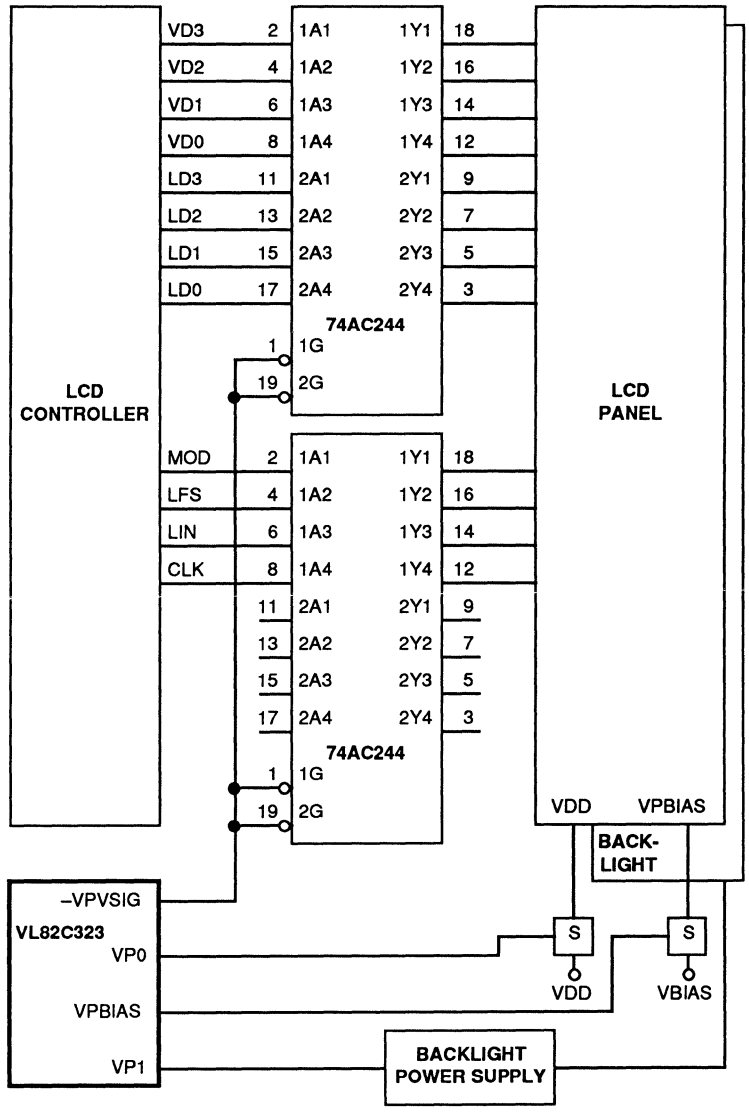
PWGIN and PWGOUT

The PWGIN input is an active high signal from the power supply. PWGIN does not reset the VL82C323 when it goes low. When a transition of PWGIN from low-to-high is detected and after a delay of 0.5 to 1.0 seconds, the VL82C323 asserts the PWGOUT signal high to the SCAMP Controller. If the PWGIN input goes low when the VL82C323 is not in the Suspend or Off Modes, the VL82C323 asserts the PWGOUT signal low immediately and places itself into the Off Mode. PWGOUT goes low before PWGIN goes low if the VL82C323 is commanded to enter either the Suspend or Off Mode.

INTERRUPT GENERATION AND HANDLING

There are 13 different sources for generation of a power management interrupt output logically ORed together by the VL82C323. These can be masked off independently by bits in the NMIMASK-I and II Registers. At power-on all NMIs are masked. When an internal NMI is generated, it generates a minimum 570 ns wide pulse. The cause of the NMI is latched and can be read from the NMICAUSE-I and II Registers. The NMICAUSE-I and II Registers are cleared when read. A read of the NMICAUSE-I Register also clears the NMI cause code in the Status Register. The NMI may also be read from the Status Register for an INMI, Sleep NMI, Activity NMI, Suspend NMI, EXT NMI, LB NMI, and LLB NMI. If any of the NMIs in the NMICAUSE-II Register are enabled, the BIOS should

FIGURE 2. LCD POWER SEQUENCING/ISOLATION CIRCUITRY



read the NMICAUSE-I and II Registers for NMI information and should not rely on the Status Register. Reading the NMIMASK-I Register does not affect the NMICAUSE-I and II Registers.

A timer is provided to automatically place the VL82C323 in the Off Mode if the LLB NMI is not serviced. See the section titled "Timers" for additional information

Although this specification refers to NMI throughout, the internally generated interrupt can be routed to –SMI or NMI, IRQx, both or neither.

NMI or IRQx Option:
If the MSK_NMI bit (bit 6) in the NMIMASK-I Register is cleared, the NMI pin is driven by the OR of all internally generated interrupts and by the INMI pin. If set, only the INMI drives the NMI output pin. If the MSK_IRQx bit (bit 7) in the NMIMASK-I Register is cleared, the IRQx output is active if any other bit besides the I_NMI bit, is set in either the NMICAUSE-I and II Registers. If set, IRQx remains inactive.

SMI (System Management Interrupt) Option:
(Applies only to X86 processors with the SMM, System Management Mode, feature.)

The programmable options described in the previous paragraph are only true if bit 4 (ALT_INT) of the MISCSET Register is 0 (default case). When ALT_INT is changed to 1, the IRQx output is disabled, the NMI pin definition changes to –SMIOUT, and the –SMIIN input is enabled. In this case, the –SMIOUT pin is driven low by the OR of all internally generated interrupts. It will remain low until the falling edge of the –SADS input pin. Reading the NMI_CAUSE Registers determines why the SMI was generated and re-enables SMI generation when –SMIIN returns inactive high. –SMIIN is also monitored for wake-up from the Doze and Sleep Modes.

Note: The VL82C310 SCAMP I Controller does not support the System Management Mode.

INMI
The INMI input comes from the SCAMP Controller for reporting PC/AT standard NMIs such as parity error or IOCHCHK. If the MSK_NMI bit in the NMIMASK-I Register is set, INMI still causes the NMI output to be active but internally generated interrupts do not.

Doze Timer NMI
When VL82C323 detects no activity and the Doze Timer times out, it generates an NMI if the MSK_DOZE bit (bit 0) is cleared in the NMIMASK-II Register. The VL82C323 remains in the On Mode.

Sleep Timer NMI
If the MSK_SLEEP bit (bit 4) in the NMIMASK-I Register is cleared, the VL82C323 generates an NMI when the Sleep Timer times out and remains in the Doze Mode.

Activity NMI and LCD Activity NMI
If the MSK_DOZE bit is cleared, activity detection occurring while the VL82C323 is in the Doze Mode generates an Activity NMI. The ACT_NMI bit (bit 6) in the NMICAUSE-I Register is set and the VL82C323 remains in the Doze Mode. If the MSK_SLEEP bit in the NMIMASK-I Register is cleared, the VL82C323 behaves the same way as in the Sleep Mode.

If MSK_LCD bit (bit 1) in the NMIMASK-II Register is cleared and the LCD Timer has previously timed out, activity that triggers the LCD Timer causes an LCD Activity NMI. The ACT_LCD_NMI bit (bit 7) in the NMICAUSE-I Register will be set. If EN_LCDSEQ is set, the LCD power is automatically sequenced on; otherwise, the BIOS must turn it on via the power control bits.

Suspend Timer NMI
If the MSK_SUSPEND bit (bit 5) in the NMIMASK-I Register is cleared, the VL82C323 generates an NMI when the Suspend Timer times out and it remains in the Sleep Mode. The BIOS saves the system status and commands the VL82C323 to enter the Suspend Mode. If the MSK_SUSPEND bit is set, the Suspend Timer is disabled. Refer to the section titled "Suspend Mode" for more information on entering Suspend.

Rescheduled Suspend NMI
When the Suspend Timer times out or the EXT pin goes high, the VL82C323 will generate an NMI to inform the BIOS to start the Suspend procedure. However, the application program may be in the middle of something that may cause the system to not be resumeable if entering the Suspend Mode at this moment. If so, a rescheduled Suspend NMI is provided to inform the BIOS to try to enter into the Suspend Mode whenever it is possible. When the MSK_RESCH bit (bit 2) in the NMIMASK-II Register is cleared, the VL82C323 will generate the rescheduled NMI every 60 ms. This feature can also be used to generate tick interrupts for the power management software. See the section titled "Suspend Reschedule Timer" also.

EXT NMI
EXT is a rising edge sensitive internally debounced input and is intended for use with an external push-button switch. A rising transition on this input while the VL82C323 is not in the Suspend or Off Mode will generate an NMI. Software can then save the status and the VL82C323 will enter either the Suspend or Off Mode.

LB NMI and LLB NMI
LB and LLB are active high inputs. The LB and LLB NMIs are masked by the MSK_LB and MSK_LLB bits, (bits 2 and 3) respectively, in the NMIMASK-I Register. If a low battery input is high and the corresponding NMI is unmasked, the PMU will generate an NMI every 15 seconds until it enters either the Suspend or Off Mode. (If the IRQx output is used, this is not the case. IRQx is latched active and remains active until the NMICAUSE-I Register is read.)

GPIO4 and GPIO5/LB1 and LB2 NMIs
When the MSK_GPLBx bits (bits 3 and 4) in the NMIMASK-II Register are unmasked, GPIO4 and GPIO5 can be used as LB1 and LB2 low battery warning inputs, respectively. These are active high inputs and are GPIO input pins at power-on reset.

LCD Timer NMI
If the MSK_LCD bit in the NMIMASK-II Register is cleared, the VL82C323 will generate an NMI when the LCD Timer times out. If the EN_LCDSEQ bit is set, the LCD power will be automatically sequenced off, otherwise the BIOS must turn it off.

SYSTEM ACTIVITY MONITOR

The System Activity Monitor is used to monitor I/O or video activity. If no activity is detected for a period of time (determined by one of several timers), the VL82C323 can generate an NMI or enter a power saving mode. If activity is detected, the VL82C323 can generate an NMI or enter the On Mode. There are eight system operations treated as a detection of activity and each of these can be masked independently in the ACTMASK Register. A bit will be set in the Activity Register for each unmasked activity that has occurred since the last time the register was read. The Activity Register is cleared when read.

Listed below are the eight different types of unmasked activities that are monitored by the System Activity Monitor and which mask bits they correspond to in the ACTMASK Register. However, the eighth activity listed (External Activity) has no corresponding mask bit.

Parallel I/O Ports	Bit 0 (MSK_PIO) Activity: Any read or write access to LPT1, LPT2, or LPT3. Their address ranges are: LPT1 - 378h to 37Fh LPT2 - 278h to 27Fh LPT3 - 3BCh to 3BFh
Keyboard Ports	Bit 1 (MSK_KBD) Activity: A read of the keyboard port 60h.
RTC Ports	Bit 2 (MSK_RTC) Activity: Any read or write access to the RTC ports 70h and 71h.
Serial Ports	Bit 3 (MSK_SIO) Activity: Any read or write access to the COM1-COM4 ports. Their address ranges are: COM1 is 3F8h to 3FFh COM2 is 2F8h to 2FFh COM3 is 3E8h to 3EFh COM4 is 2E8h to 2EFh
Floppy Disk Port	Bit 4 (MSK_FLP) Activity: A read or write to the floppy disk data port 3F5h.
Hard Disk Port	Bit 5 (MSK_HD) Activity: A read or write to the hard disk port, 1F0h to 1F7h.
Video Memory Writes	Bit 6 (MSK_VIDM) Activity: A high-to-low transition on –VIDCS4 - –VIDCS0. (A low on any of the –VIDCS inputs indicates a memory write is occurring. Typically, one of the –VIDCS inputs is connected to the video memory write signal of the VGA. The unused –VIDCS signals are pulled up with an external resistor or connected to VDDRD of the VL82C323.) Detection of the high-to-low transition is treated as an activity and the VL82C323 will exit from the Doze or Sleep Mode if bit 6 is not masked. If bit 6 is masked, the high-to-low transition causes the –SLOWCLK pin to go high for 8 ms without exiting from the Doze or Sleep Mode, temporarily speeding up the CPU clock.
Programmable I/O	Bit 7 (MSK_IORNG) Activity: A programmable I/O range to the Activity Monitor allows the designer to monitor a non-standard I/O device for activity. This I/O address is specified in the IORNG Register. The I/O range can be 8 or 16 bytes long. The default programmable I/O range is 16 bytes long.
External Activity	No Corresponding Mask Bit A rising edge on the EXTACT pin will be sensed as activity, however, there is no mask bit for this activity nor is it reported in the Activity Register.

OPERATION MODES

The VL82C323 has five operational modes:

- On Mode
- Doze Mode
- Sleep Mode
- Suspend Mode
- Off Mode

Each mode can be entered through a timer time-out or by a detection of activity. They also can be entered any time by writing bit 1 (MODE1, Mode MSB) and bit 0 (MODE0, Mode LSB) of the Status Register.

On Mode

When the VL82C323 is first powered up (from the Off Mode), an –RCRESET is generated and places the VL82C323 into the On Mode. In the On Mode, all power control outputs are controlled by the PWRON Register.

If the VL82C323 is in the Suspend or Off Mode, the On Mode is entered when either the EXT, RI or –RTCIRQ pins go high. Once this occurs, the Doze, BL, and LCD Timers are retriggered.

When in the Doze or Sleep Mode, the On Mode is entered when the Activity Monitor detects activity. The activity will also retrigger the Doze Timer.

If ACPWR is high, the Doze Timer is disabled and causes the hardware power saving features of the VL82C323 to be disabled except for the BL Timer. Unless commanded to change modes, the VL82C323 remains in the On Mode, with its –SLOWCLK output pin high.

Doze Mode

The Doze Mode may only be entered from the On Mode. If the MSK_DOZE bit (bit 0) in the NMIMASK-II Register is set, the Doze Mode is entered when the Activity Monitor has not detected activity within the specified amount of time set by the Doze Timer Register. Any unmasked activity causes an exit from the Doze Mode and into the On Mode. Alternatively, if the MSK_DOZE bit is cleared, the VL82C323 generates an NMI and remains in the On Mode until the BIOS commands it to enter the Doze or some other mode. Any unmasked activity causes an activity NMI. In the Doze Mode, the power control outputs are controlled by the PWRDOZE Register, the –SLOWCLK pin will go low and the SCAMP Controller may slow down the CPU clock. Interrupts, NMIs, or video memory writes temporarily forces the –SLOWCLK output pin high (as described in the section titled "SCAMP Controller and the VL82C107 Interface").

Sleep Mode

If the MSK_SLEEP bit (bit 4) in the NMIMASK-I Register is set, the Sleep Mode is automatically entered from the Doze Mode when the activity monitor has not detected activity within the time

specified by the Sleep Timer Register. Any unmasked activity causes an exit from the Sleep Mode and into the On Mode. Alternatively, if the MSK_SLEEP bit is cleared, the VL82C323 generates an NMI and remains in the Doze Mode until the CPU commands it to enter the Sleep Mode. Any unmasked activity causes an activity NMI. The –SLOWCLK pin's behavior is the same as when it is in the Doze Mode. The power control outputs are controlled by the PWRSLEEP Register.

Suspend Mode

If software support is provided for the Suspend Mode, the VL82C323 can be programmed to generate an NMI after the Suspend Timer times out, or in response to a low-to-high transition on the EXT input pin when the VL82C323 is not in the Suspend or Off Modes. After saving the system information, the BIOS can place the VL82C323 in the Suspend Mode via the Status Register. The BIOS may halt the CPU but it is not necessary. The BIOS must not read data or instructions from DRAM after issuing the Suspend command. The power control outputs are controlled by the PWRSUSPEND Register.

Refresh Control:

The –RAS and –CAS lines from the SCAMP Controller are bused to the VL82C323. The VL82C323 three-states its outputs connected to these lines during normal operation. There are three programmable options when the Suspend Mode is active.

1. VL82C323 Performs CAS-before-RAS Refresh: When the VL82C323 is commanded to enter the Suspend Mode and PWGOUT is driven low to the SCAMP Controller, the VL82C323 takes over refresh of on-board DRAM. It performs CAS-before-RAS refresh cycles at a rate determined by the SLWREF bit (bit 2) in the Control Register.
2. VL82C323 Enables DRAM's Self-Refresh Mode: When the VL82C323 is commanded to enter the Suspend Mode and PWGGD is driven low to the SCAMP Controller, the VL82C323 performs a 1024 cycle CAS-before-RAS refresh burst to DRAM. Self-Refresh Mode is then activated by holding the –RAS and –CAS lines low.
3. VL82C323 does not Perform Refresh: When the VL82C323 is commanded to enter the Suspend Mode and PWGGD is driven low to the SCAMP Controller, the VL82C323 enters the Suspend Mode and provides the usual leakage control functions but leaves the –RAS and –CAS lines three-stated. Use this mode if the VL82C316 SCAMP II Controller's Suspend Mode refresh option is desired.

Resume From Suspend:

Only activity on the EXT, RI, or –RTCIRQ input pins can cause an exit from the Suspend Mode and place the VL82C323 into the On Mode. The cause of the resume can be examined in the WU0 and WU1 bits (bits 5 and 6) in the Status Register. The BIOS must read the RESUME bit (bit 7) in the Status Register to determine if a cold boot or return from the Suspend Mode has occurred. If the RESUME bit is true, the BIOS restores all information and verifies the data in the main memory and video memory is still valid. The RESUME bit is reset when read.

When a wake-up event occurs, the VL82C323 enters the On Mode and turns VDD on 0.5 to 1.0 seconds later after PWGIN goes high. The digital signals that were three-stated or held low return to their normal levels. After PWGOUT is driven high, the VL82C323 discontinues the on-board DRAM refresh (if Refresh Control options 1 or 2 have been selected) and the SCAMP Controller takes over.

Off Mode

The VL82C323 enters the Off Mode after a falling edge on the PWGIN input or when the CPU writes the code for the Off Mode (FFh) to the Status Register. The Auto Power Off Timer described in the "Timers" section also causes the VL82C323 to enter the Off Mode.

The Off Mode is meaningful only when the VL82C323 is powered from a battery while the rest of the system is turned off. This type of connection is necessary only if the VL82C323 must wake-up the system from the Off Mode by activating the VP outputs in response to transitions on the EXT, RI or –RTCIRQ inputs. If this function is not implemented, the VL82C323 may be powered off along with the system power, as with a switch, and the Off Mode does not exist.

In the Off Mode, all devices except battery backed up devices in the computer are powered off. Only –RCRESET or activity on the EXT, RI, or –RTCIRQ inputs can cause an exit from the Off Mode and place it into the On Mode. When powered up from the Off Mode, burst refresh is not activated and if –RCRESET was not asserted, the contents of the VL82C323's internal registers are not changed after waking up from the Off Mode.

TIMERS

There are ten timers in the VL82C323. Some timers are associated with the activity monitors controlling mode transitions. Detailed description of the timers follows.

Doze Timer

The Doze Timer is programmable from 1/8 to 1 second with a resolution of 1/8 of a second, and from 2 to 14 seconds with a resolution of 2 seconds. Setting a zero value to the Doze Timer disables it and setting any non-zero value enables it. Any activity detected by the Activity Monitor retriggers the Doze Timer. The default value for the Doze Timer is 4 seconds.

Sleep Timer

The Sleep Timer is programmable from 1 to 15 minutes with a resolution of 1 minutes. Setting a zero value to the Sleep Timer disables it and setting any non-zero value enables it. Any activity detected by the Activity Monitor retriggers the Sleep Timer. The Sleep Timer is triggered when the Doze Mode is entered and is cleared when the Doze Mode is exited. The default value for the Sleep Timer is 2 minutes.

Suspend Timer

The Suspend Timer is programmable from 5 to 75 minutes with a resolution of 5 minutes. Setting a zero value to the Suspend Timer disables it and setting any non-zero value enables it. Any activity detected by the Activity Monitor retriggers the Suspend Timer. The Suspend Timer is triggered when the Sleep Mode is entered and is cleared when the Sleep Mode is exited. The default of the MSK_SUSPEND bit (bit 5) in the NMIMASK-I Register is

masked so it disables the Suspend Timer. The default value for the Suspend Timer is 5 minutes.

Backlight (BL) Timer
The BL Timer is programmable from 1 to 15 minutes with a resolution of 2 minutes. Setting a zero value to the BL Timer disables it and setting any non-zero value enables it. The BL Timer is always enabled and is retriggered when the Activity Monitor detects any keyboard activity. The default value for the BL Timer is 2 minutes.

LCD Timer
The LCD Timer is programmable from 1 to 15 minutes with a resolution of 1 minutes. Setting a zero value to the LCD Timer disables it and setting a non-zero value enables it. It is disabled if ACPWR is true and is triggered when the VL82C323 goes from the Off or Suspend Modes to the On Mode, and when keyboard activity occurs or when the –VIDCS inputs are asserted. The default value for the LCD Timer is 2 minutes.

Suspend Reschedule Timer
The Suspend Reschedule Timer is fixed at 60 ms. While the MSK_RESCH bit in the NMIMASK-II Register is cleared, the VL82C323 generates a Suspend Reschedule NMI every 60 ms. The Suspend Reschedule Timer can be retriggered by momentarily setting and clearing the MSK_RESCH bit (bit 2) in the NMIMASK-II Register. This feature can be used to generate reliable tick interrupts for the power management software if the System Clock Timer has been reprogrammed by the application or OS software. The Suspend Reschedule Timer is retriggered at each INT8, it never times out, but if other software takes over the System Clock Timer, it times out and repeatedly generates an NMI until masked.

Auto Power Off Timer
If an LLB NMI is unmasked and is not serviced within three minutes while LLB remains continuously true, the VL82C323 automatically enters the Off Mode.

VIDCS Timer
A fixed 8 ms timer is provided for the video memory write operations. If the MSK_VIDM bit (bit 6) in the ACTMASK Register is set, any low transitions on the –VIDCS inputs are not treated as an activity detection. The VL82C323 temporarily brings the –SLOWCLK pin high for 8 ms without exiting from the Doze or Sleep Modes. If the MSK_VIDM bit is cleared, the VIDCS Timer is disabled. Default is disabled.

Low Battery Timer
The Low Battery (LB) Timer is enabled in the On, Doze, and Sleep Modes. The LB Timer is fixed to 15 seconds. An NMI is generated by the LB Timer every 15 seconds until a timer period elapses during which all low battery inputs are continuously false. This is also true for LLB, LB1 (GPIO4), and LB2 (GPIO5).

Power-On Fault Timer
If PWGIN fails to go high within 1 to 2 seconds after a wake-up, the VL82C323 returns to the previous mode (either the Off or Suspend Mode).

Time Register
The Time Register is read-only register. It contains the value of a counter that counts cycles of the 32 kHz clock whenever it is running. Unlike the System Clock Timer, it can not be altered by the application software and can provide a reliable relative time reference for the power management software. It is cleared when –RCRESET is active.

POWER-ON
There are three power-on inputs to the VL82C323:
- –RTCIRQ
- RI
- EXT

These inputs can bring the VL82C323 out of the Suspend or Off Modes and into the On Mode. Since these inputs control the power on/off for the system, care must be taken to ensure these inputs never float. To ensure these inputs are always driven, tie any unused inputs low.

Real Time Clock Power-On
–RTCIRQ is an edge sensitive input, intended for use with the real-time clock's wake-up alarm from the VL82C107 SCAMP Combination I/O chip. Any transition on this input forces the VL82C323 into the On Mode. The VL82C323 generates an –IRQ8 output to the VL82C310 SCAMP I Controller to prevent leakage while in the Suspend Mode.

Note: The above discussion only applies when using the VL82C323 in a VL82C310/ VL82C107-based system. The RTC is built into the VL82C316. In systems using the VL82C316, the VL82C323's –IRQ8 output signal is not connected to the VL82C316 and leakage control of this signal is not an issue. However, the –RTCIRQ output of the VL82C316 is connected to the VL82C323's –RTCIRQ input to support the time of day wake-up feature.

Ring Indicator Power-On
RI is a rising edge sensitive input, intended for use with a modem ring indicator output. The number of rising edges required for this input to be recognized is specified in bits D6-D4 (RING2-RING0) of the Control Register. The default is one transition. If these bits are zero, the RI input is disabled. If enabled, the programmed number of edges forces the VL82C323 into the On Mode.

External Switch Power-On
EXT is a rising edge sensitive input, intended for use with an external source. A rising transition on this input while the VL82C323 is in either the Off or Suspend Mode forces it into the On Mode. A transition in the On, Doze, or Sleep Modes generates an NMI.

EXT is internally debounced. A rising edge immediately generates an NMI if EXT has been sampled low at least twice by a 32 Hz debounce clock prior to the rising edge. The VL82C323 does not respond to any activity on any other wake-up input until after the EXT input has been sampled low twice by the debounce clock.

LEAKAGE CONTROL DURING SUSPEND AND OFF MODES
Leakage control is active during the Suspend and Off Modes in order to provide absolute minimal current consumption. However, there is a set of signals for which the system designer must externally control leakage either because they must remain functional during the Off Mode or to prevent the design of the VL82C323 from placing restrictions on the user's circuits.

These signals are:
LB, LLB, RI, EXT, –RTCIRQ, ACPWR, PWGIN, –RCRESET, RTCXOUT, RTCXIN and GPIO9-GPIO0.

GPIO
The VL82C323 has ten general purpose pins that may be individually programmed as inputs or outputs. Some can be programmed as blinking outputs, low battery inputs, or AND/OR inputs or output. They default to general purpose inputs at power-on. If not used, they must be tied low to prevent leakage. Alternatively, they may be programmed as outputs to prevent leakage. For example, these could be used for monitoring the power supply status, EEPROM interface, or as software controlled VP outputs.

Blinking Option
The GPIO3 pin can be used as a programmable audio and/or blinking generator. The blinking option is enabled by setting the EN_BLK bit (bit 0) in the Blinking Register. Default is reset. The blink generator produces an audible output frequency which blinks on and off. The frequency, blink rate, and number of blinks are also programmed by the Blinking Register. When used to drive a LED rather than a speaker, the use of audio frequencies results in an LED that flashes at the blink rate but is unaffected by the audio frequency. This feature might be useful to drive an LED indicator, speaker, or both in response to a low battery indication or as an indicator that the Suspend Mode is active, for example.

Low Battery Option
The GPIO4 and GPIO5 pins may be used as an optional low battery warning inputs. Please refer to the section titled "GPIO4 and GPIO5/LB1 and LB2 NMI" for a detailed description.

TABLE 1. REGISTER DESCRIPTIONS

Register	Index		Register	Index
STATUS	C0h		LCD	CFh
SUPPLY	C1h		BL	D0h
CONTROL	C2h		NMIMASK-II	D1h
ACTMASK	C3h		NMICAUSE-I	D2h
NMIMASK-I	C4h		NMICAUSE-II	D3h
IORNG	C5h		MISCSET	D4h
PWRON	C6h		REVID	D5h
PWRDOZE	C7h		BLINKING	D6h
PWRSLEEP	C8h		GPDIR	D7h
PWRSUSPEND	C9h		GPEN	D8h
POLARITY	CAh		ANDOR	D9h
OUTPUT	CBh		Reserved	DAh
DOZE	CCh		ACTIVITY	DBh
SLEEP	CDh		TIME	DCh
SUSPEND	CEh			

TABLE 2. STATUS REGISTER (C0h)

Bit	Name	Function
D7	RESUME	Resuming from Suspend (Warm Start)
D6	WU1	Wake-up Code MSB
D5	WU0	Wake-up Code LSB
D4	NMI2	NMI Cause Code
D3	NMI1	NMI Cause Code
D2	NMI0	NMI Cause Code
D1	MODE1	Mode MSB
D0	MODE0	Mode LSB

–RCRESET clears all bits. D4-D2 are cleared when the NMICAUSE-I Register is read. D7 is cleared after the Status Register is read.

Only D0 and D1 are affected by a write. The CPU can write the mode code to this register to put the VL82C323 into another mode. Writing 0FFh puts it in the Off Mode. The NMI cause, mode, and wake-up codes are decoded in Table 3.

TABLE 3. NMI CAUSE, MODE, AND WAKE-UP CODES

NMI		Mode		Wake-up	
Code	Cause	Code	Cause	Code	Cause
000	None or INMI	00	On	00	
001	EXT Input	01	Doze	01	EXT Input
010	LB	10	Sleep	10	–RTCIRQ Input
011	LLB Time-out	11	Suspend	11	RI Input
100	Sleep Time-out				
101	Suspend Time-out				
110	Sleep to On (Activity)				

SUPPLY REGISTER (C1h)
This register has different functions for read and write. This GPIO2-GPIO0 pins are programmed as inputs or outputs by D2-D0 and are read and written on D6-D4. For read operations, D7-D4, D1, and D2 are driven directly by the input pins. D3 is set when system activity is detected and is cleared when the Supply Register is read.

TABLE 4. SUPPLY REGISTER - READ

Bit	Name	Function
D7	ACPWR	
D6	GPIN2	General Purpose Input
D5	GPIN1	
D4	GPIN0	
D3	ACTIVITY	System Activity Present
D2	LLB	Low Battery 2 (Second Warning)
D1	LB	Low Battery 1 (First Warning)
D0	LOCKOUT	PMU Registers Write-Protected

TABLE 5. SUPPLY REGISTER - WRITE

Bit	Name	Default	Function
D7	Reserved	0	
D6	GPOUT2	0	General Purpose Output
D5	GPOUT1	0	
D4	GPOUT0	0	
D3	Reserved	0	
D2	GPDIR2	0	General Purpose I/O Direction Control
D1	GPDIR1	0	
D0	GPDIR0	0	

TABLE 6. CONTROL REGISTER (C2h)

Bit	Name	Default	Function
D7	Reserved	0	
D6	RING2	0	RI Pulse Required for Turn-on
D5	RING1	0	
D4	RING0	1	
D3	Reserved	0	
D2	SLWREF	0	1 = Slow Refresh DRAM
D1	SUSPREF1	0	00 = CAS-before-RAS 01 = Self-Refresh 1X = Refresh Inactive
D0	SUSPREF0	0	

The RING2-RING0 bits are used to set the number of RI pulses required for turn-on. The default value of RING0 is 1 so that only one pulse is required for turn-on. If set to 0, RI is disabled.

TABLE 7. ACTMASK REGISTER (C3h)

Bit	Name	Default	Function
D7	MSK_IORNG	1	Mask Access to 16 Ports at IORNG5-IORNG0
D6	MSK_VIDM	0	Mask Access to Video Memory
D5	MSK_HD	0	Mask Hard Disk Activity
D4	MSK_FLP	0	Mask Access to Port 3F5
D3	MSK_SIO	0	Mask Access to COM1-COM4
D2	MSK_RTC	1	Mask Access to Port 70h, 71h
D1	MSK_KBD	0	Mask Keyboard Access to Port 60h Reads
D0	MSK_PIO	0	Mask Access to LPT1-LPT3

The activity monitor ACTIVITY output is the logical OR of all unmasked activity sources. This register affects only the ACTIVITY output.

TABLE 8. NMIMASK-I REGISTER (C4h)

Bit	Name	Default	Function
D7	MSK_IRQx	1	Mask IRQx Output
D6	MSK_NMI	0	Mask NMI Output
D5	MSK_SUSPEND	1	Mask Suspend Time-out
D4	MSK_SLEEP	1	Mask Sleep Time-out
D3	MSK_LLB	1	Mask LLB Input
D2	MSK_LB	1	Mask LB Input
D1	MSK_EXT	1	Mask EXT Input
D0	Reserved	0	

The register masks the various NMI sources. In the Default Mode, only the INMI input can generate NMI.

TABLE 9. IORNG REGISTER (C5h)

Bit	Name	Default	Function
D7	RNGSIZE	0	1 = 8 Bytes, 0 = 16 Bytes
D6	IORNG6	0	Maskable I/O Range Base Address
D5	IORNG5	0	
D4	IORNG4	0	
D3	IORNG3	0	
D2	IORNG2	0	
D1	IORNG1	0	
D0	IORNG0	0	

IORNG6-IORNG0 are the base address bits SA9-SA3 for the maskable I/O port range in the activity monitor. RNGSIZE is the size of the range. IORNG0 is ignored when RNGSIZE is low.

POWER REGISTERS (C6-C9h)
The bits in the Power Registers, D7-D0, correspond directly with the power control outputs VP7-VP0. In a particular mode, the corresponding PWR Register's outputs control the VP pins. The exception is VP0 and VP1 which are the LCD and BL power, respectively. These outputs are ANDed with the LCD and BL Timer outputs prior to driving the pins. All bits are then exclusive NORed with the Polarity Register and the result drives the pins. VPBIAS, –VPVSIG, and VP0 are controlled as described in the "Automatic LCD Power Sequencing" section. The default values for these registers are as shown in Table 10, where 1 indicates that the controlled device is on.

POLARITY REGISTER (CAh)
The Polarity Register controls the polarity of the VP outputs. If a logic low is required on any of the VP7-VP0 pins to turn the external device on, the corresponding bit in the Polarity Register must be low. If a high is required, set the bit high. The default value is 0FFh. The polarity of VPBIAS is the same as VP0. –VPVSIG is always low true.

OUTPUT REGISTER (CBh)
The Output Register is a read-only register. For each VP7-VP0 output that is on, the corresponding bit in the Output Register will be set.

TIMER REGISTERS (CC-D0h)
Loading a value into a Timer Register enables the timer and selects the time-out. All Timer Registers have four significant bits (bits 3-0). Data written to the upper bits has no effect. The upper bits are 0 when read back. Except for the Doze Timer, all Timer Registers can be set for a time-out from 1 to 15 time units, where a unit is the resolution of the timer. A zero disables the timer. Reading a Timer Register returns the value that was last written to it, not the actual time remaining. The default values are tabulated in Tables 11 and 12.

TABLE 10. POWER REGISTERS (C6-C9h)

Register	Default	Index
PWRON	FEh	C6h
PWRDOZE	FEh	C7h
PWRSLEEP	FCh	C8h
PWRSUSPEND	00h	C9h

TABLE 11. TIMER REGISTERS (CC-D0h)

Timer	Range	Default	Index
Doze	1/8-14 sec	4 sec	CCh
Sleep	1-15 min	2 min	CDh
Suspend	5-75 min	0 (disabled)	CEh
LCD	1-15 min	2 min	CFh
BL	1-15 min	2 min	D0h

TABLE 12. DOZE TIMER PROGRAMMING

D3-D0	Time	D3-D0	Time
0000	Disabled	1000	1 sec
0001	1/8 sec	1001	2 sec
0010	1/4 sec	1010	4 sec
0011	3/8 sec	1011	6 sec
0100	1/2 sec	1100	8 sec
0101	5/8 sec	1101	10 sec
0110	3/4 sec	1110	12 sec
0111	7/8 sec	1111	14 sec

TABLE 13. NMIMASK-II REGISTER (D1h)

Bit	Name	Default	Function
D7	Reserved		
D6	Reserved		
D5	Reserved		
D4	MSK_GPLB2	1	Mask off the LB2 NMI option from GPIO5. 1 = Mask. When this bit is low, the GPIO5 is used as LB2 input.
D3	MSK_GPLB1	1	Mask off the LB1 NMI option from GPIO4. 1 = Mask. When this bit is low, the GPIO4 is used as LB1 input.
D2	MSK_RESCH	1	Mask off the Suspend reschedule NMI. 1 = Mask.
D1	MSK_LCD	1	Mask off the NMI caused by the LCD Timer time-out. 1 = Mask.
D0	MSK_DOZE	1	Mask off the NMI caused by the Doze Timer time-out. 1 = Mask.

TABLE 14. NMICAUSE-I REGISTER (D2h)

Bit	Name	Default	Function
D7	ACT_LCD_NMI	0	LCD Timer Retrigger Activity
D6	ACT_NMI	0	Activity NMI from Doze or Sleep
D5	SUSPEND_NMI	0	Suspend NMI
D4	SLEEP_NMI	0	Sleep NMI
D3	LLB_NMI	0	LLB NMI
D2	LB_NMI	0	LB NMI
D1	EXT_NMI	0	EXT Input NMI
D0	I_NMI	0	PC/AT-compatible specified NMI generated by the SCAMP Controller.

The NMI cause can also be examined by reading the Status Register. Additional NMICAUSE Registers are provided to give more flexibility of using the VL82C323. Reading the NMICAUSE-I Register clears the NMICAUSE-I Register and the NMI cause codes in the Status Register. It also clears the IRQx output, if it is unmasked. The NMICAUSE-I Register is cleared at the trailing edge of the –IOR signal. A double buffer method is used to prevent loss of the NMI while it is cleared. Writing any data to it indicates the end of a VL82C323 NMI service routine but does not change the contents of the register.

TABLE 15. NMICAUSE-II REGISTER (D3h)

Bit	Name	Default	Function
D7	Reserved		
D6	Reserved		
D5	Reserved		
D4	GPLB2_NMI	0	GPLB2 NMI
D3	GPLB1_NMI	0	GPLB1 NMI
D2	RESCH_NMI	0	Rescheduled NMI
D1	LCD_NMI	0	LCD NMI
D0	DOZE_NMI	0	Doze NMI

The NMICAUSE-II Register is cleared by reading it. It is a read-only register.

TABLE 16. MISCSET REGISTER (D4h)

Bit	Name	Default	Function
D7	FASTDB	0	Low battery NMI debouce time. Low = 2-4 seconds and high = 30-60 ms.
D6	AUTOFLUSH	0	When set, it allows automatic stack flush when entering the On Mode.
D5	FLUSH	0	When set, it flushes and inhibits the INTR stack.
D4	EN_LCDSEQ	0	When the EN_LCDSEQ bit is set, the VL82C323 performs the LCD power-up/down sequencing.
D3	LCDTMG1	0	LCDTMG0 and LCDTMG1 are used to select the LCD power-up/down sequencing if the EN_LCDSEQ bit is set. If the EN_LCDSEQ is not set, LCDTMG0 controls –VPVSIG and LCDTMG1 controls the VPBIAS outputs individually.
D2	LCDTMG0	0	**1 0 Delay** 0 0 8 ms 0 1 15 ms 1 0 31 ms 1 1 125 ms
D1	ALT_INT	0	Enable –SMI generation and disable NMI and IRQx outputs.
D0	EN_HICLK	0	When high, forces –SLOWCLK pin to go high in the Doze or Sleep Mode.

TABLE 17. REVID REGISTER (D5h)

Bit	Name	Default	Function
D7	ID3	0	Used for the ID number of the VL82C323.
D6	ID2	0	
D5	ID1	0	
D4	ID0	0	
D3	Reserved	0	
D2	REV2	0	Used for revision number of the VL82C323.
D1	REV1	0	
D0	REV0	0	

TABLE 18. BLINKING REGISTER (D6h)

Bit	Name	Default	Function
D7	Reserved		
D6	BLKPERD1	0	**1 0 Period** 0 0 1 Hz 0 1 2 Hz 1 0 4 Hz 1 1 8 Hz
D5	BLKPERD0	0	
D4	BLKNBR1	0	**1 0 Number** 0 0 1 0 1 2 1 0 4 1 1 Continuous
D3	BLKNBR0	0	
D2	BLKFRQ1	0	**1 0 Frequency** 0 0 512 Hz 0 1 1024 Hz 1 0 1365 Hz 1 1 2048 Hz
D1	BLKFRQ0	0	
D0	EN_BLK	0	Used to enable the blinking option of the GPIO3. 1 = enable.

EXAMPLE OF BLINKING REGISTER

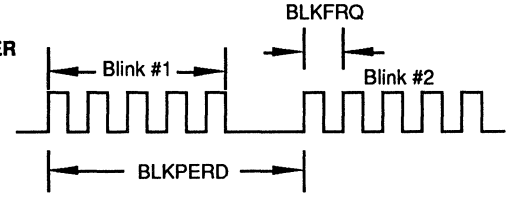


TABLE 19. GPDIR REGISTER (D7h)

Bit	Name	Default	Function
D7	Reserved		
D6	GPDIR9	0	GPDIR9-GPDI3 are used as general purpose I/O pins. The direction of GPIO can be programmed individually by setting this register. 1 = output and 0 = input. Default = input.
D5	GPDIR8	0	
D4	GPDIR7	0	
D3	GPDIR6	0	
D2	GPDIR5	0	
D1	GPDIR4	0	
D0	GPDIR3	0	

GPDATA REGISTER (D8h)
This register has different functions for read and write.

TABLE 20. GPDATA REGISTER - READ

Bit	Name	Default	Function
D7	Reserved		
D6	GPIN9	0	If the corresponding bit in the GPDIR Register is set to input, the value of the GPIO pin can be examined by this register. The register is cleared after reading.
D5	GPIN8	0	
D4	GPIN7	0	
D3	GPIN6	0	
D2	GPIN5	0	
D1	GPIN4	0	
D0	GPIN3	0	

TABLE 21. GPDATA REGISTER - WRITE

Bit	Name	Default	Function
D7	Reserved		
D6	GPOUT9	0	If the corresponding bit in the GPDIR Register is to output, the value of the GPIO pin can be set by this register.
D5	GPOUT8	0	
D4	GPOUT7	0	
D3	GPOUT6	0	
D2	GPOUT5	0	
D1	GPOUT4	0	
D0	GPOUT3	0	

TABLE 22. ANDOR REGISTER (D9h)

Bit	Name	Default	Function
D7	Reserved		
D6	Reserved		
D5	Reserved		
D4	Reserved		
D3	SEL_POL	1	If set, GPIO9 is the output of the AND/OR function. If cleared, GPIO9 is the output of the NAND/NOR function.
D2	SEL_AND	0	If EN_ANDOR is enabled, SEL_AND = 1 selects the AND function and SEL_AND = 0 selects the OR function.
D1	EN_AO8	0	Enable the AND/OR function for the GPIO8. When this bit and the EN_ANDOR bit are both set, GPIO8 becomes an input of the AND/OR function.
D0	EN_ANDOR	0	Enables the AND/OR function for GPIO9, GPIO7, and GPIO6. When set, GPIO7 and GPIO6 become the inputs of the AND/OR function and GPIO9 becomes the output.

TABLE 23. ACTIVITY REGISTER (DBh)

Bit	Name	Default	Function
D7	IORNG	0	I/O Range Activity
D6	VIDM	0	Video Memory Activity
D5	HD	0	Hard Disk Activity
D4	FLP	0	Floppy Disk Activity
D3	SIO	0	COM Port Activity
D2	RTC	0	Real-time Clock Access
D1	KBD	0	Keyboard Port 60h Read Activity
D0	PIO	0	LPT1-LPT3 Activity

TABLE 24. TIME REGISTER (DCh)

Bit	Significance
D7	1 s
D6	500 ms
D5	250 ms
D4	125 ms
D3	62.5 ms
D2	31.25 ms
D1	15.625 ms
D0	7.8125 ms

The Time Register contains the relative time in units of 1/128 second. It is a read-only register and is cleared only by –RCRESET.

FIGURE 3. POWER MANAGEMENT MODE FLOW

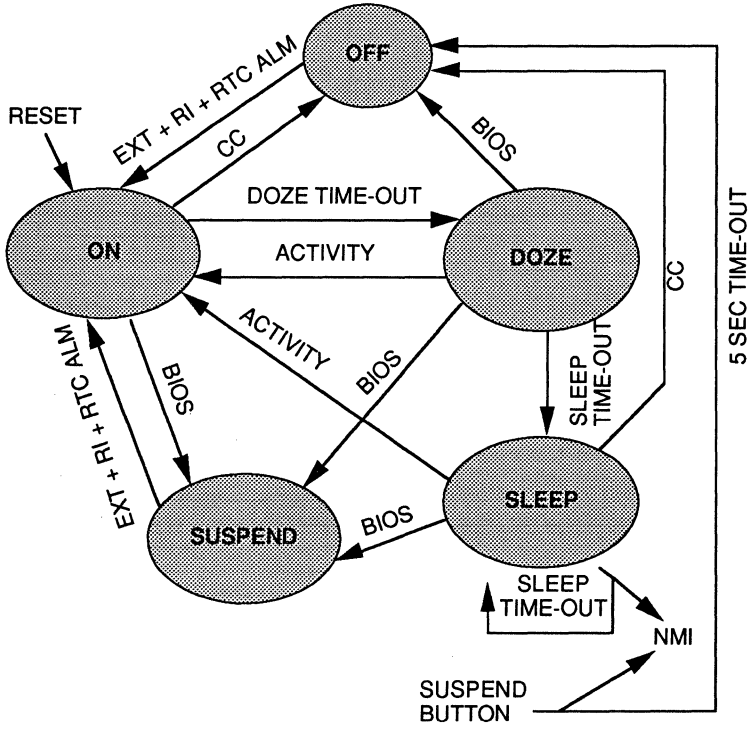


FIGURE 4. VL82C316 SCAMP II 5 VOLT CONTROLLER NOTEBOOK SYSTEM BLOCK DIAGRAM IN SMM SYSTEMS

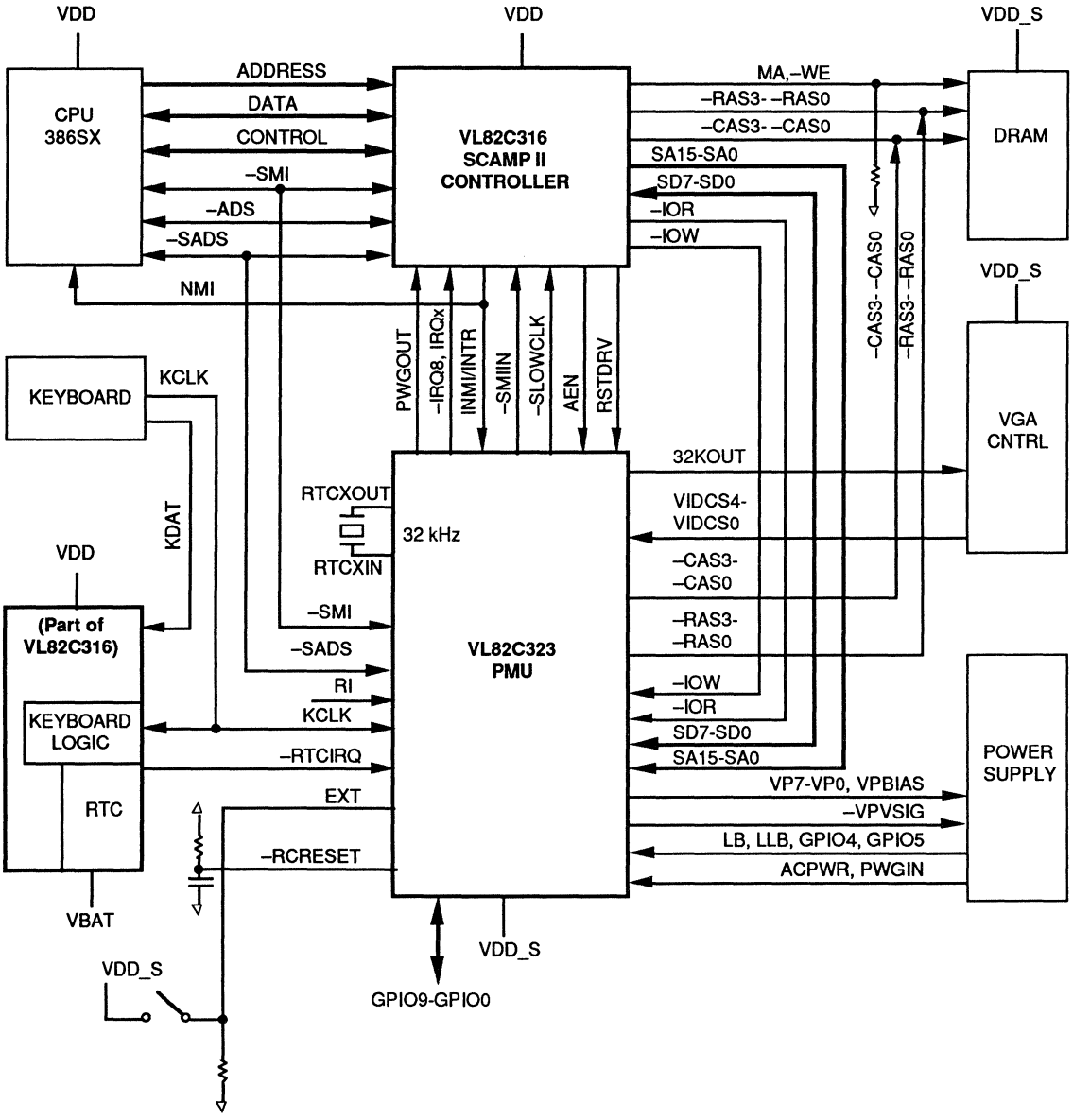
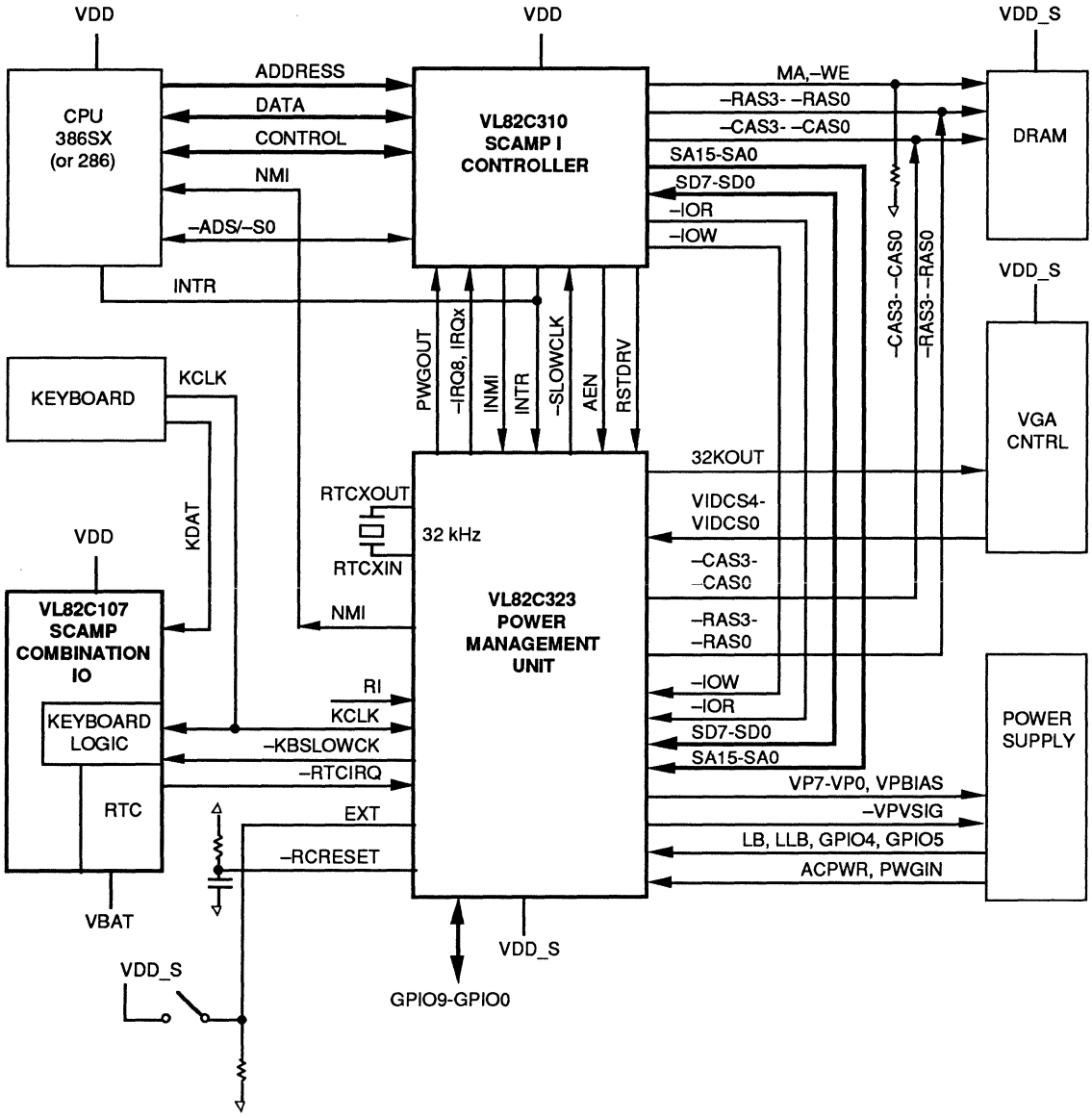


FIGURE 5. VL82C310 SCAMP I NOTEBOOK SYSTEM BLOCK DIAGRAM

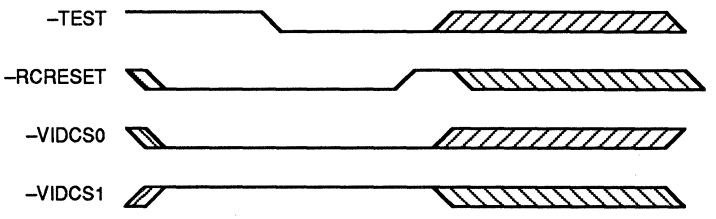


IN-CIRCUIT TEST MODE

During In-Circuit Test (ICT) Mode each output may be toggled by one or more of the inputs. This allows a board level tester to check the solder connection of each pin.

Table 25 shows the input to output mapping for each pin while the ICT Mode is active. The "Pin Name" column shows the first of the two signals in an I/O mapping pair. As an example, pin 3 (–VIDCS1), is used as an input while VP0 is used as the output.

The sequence for enabling ICT Mode:



To clear ICT Mode, –IOW and –IOR must be low and ACPWR high.

TABLE 25. PIN ASSIGNMENT FOR IN-CIRCUIT TEST

Pin #	Pin Name	ICT IO Mode	ICT Direction	ICT Connection	Pin #	Pin Name	ICT IO Mode	ICT Direction	ICT Connection
1	VGARST	Out	From	–VIDCS0	24	PWGIN	In	To	VP3
2	–VIDCS0	In	To	VGARST	25	EXTACT	In	To	GPIO5
3	–VIDCS1	In	To	VP0	26	VSSR			
4	–VIDCS2	In	To	–VPVSIG	27	EXT	In	To	U34*
5	–VIDCS3	In	To	VP1	28	RI	In	To	U34*
6	–VIDCS4	In	To	VPBIAS	29	–IRQ8	Out	From	AEN
7	–VPVSIG	Out	From	–VIDCS2	30	IRQx	Out	From	AEN
8	VPBIAS	Out	From	–VIDCS4	31	AEN	In	To	IRQX
9	VP0	Out	From	–VIDCS1	32	–IOR	In	To	U34*
10	VP1	Out	From	–VIDCS3	33	–IOW	In	To	U34*
11	VDDRD				34	VDDRA			
12	VP2	Out	From	LLB	35	SD0	In	To	U34*
13	VP3	Out	From	PWGIN	36	SD1	In	To	
14	VSSR				37	VSSI			
15	VP4	Out	From	LB	38	SD2	In	To	U34*
16	VP5	Out	From	ACPWR	39	SD3	In	To	U34*
17	VP6	Out	From	LB	40	SD4	In	To	U34*
18	VP7	Out	From	ACPWR	41	SD5	In	To	U34*
19	GPIO4	Out	From	U34*	42	SD6	In	To	U34*
20	GPIO5	Out	From	EXTACT	43	SD7	In	To	U34*
21	LB	In	To	VP4/VP6	44	VSSR			
22	LLB	In	To	VP2	45	RSTDRV	In	To	U34*
23	ACPWR	In	To	VP5/VP7	46	SA0	In	To	U34*

TABLE 25. PIN ASSIGNMENT FOR IN-CIRCUIT TEST (Cont.)

Pin #	Pin Name	ICT IO Mode	ICT Direction	ICT Connection	Pin #	Pin Name	ICT IO Mode	ICT Direction	ICT Connection
47	SA1	In	To	U34*	74	INMI	In	To	U34*
48	SA2	In	To	U34*	75	INTR	In	To	NMI/–SMIOUT
49	SA3	In	To	U34*	76	VDDRB			
50	SA4	In	To	U34*	77	–SADS	In	To	U34*
51	SA5	In	To	U34*	78	–ADS/–S0	Out	To	–SLOWCLK
52	SA6	In	To	U34*	79	–SLOWCLK	Out	To	–ADS
53	SA7	In	To	U34*	80	–KBSLOWCK	Out	To	–RTCIRQ
54	SA8	In	To	U34*	81	–RTCIRQ	In	To	–KBSLOWCK
55	SA9	In	To	U34*	82	PWGOUT	Out	From	–RTCIRQ
56	VDDRA				83	–RCRESET	In	To	U34*
57	SA10	In	To	U34*	84	VDDRC			
58	SA11	In	To	U34*	85	RTCXOUT			
59	SA12	In	To	U34*	86	RTCXIN			
60	SA13	In	To	U34*	87	VSSR			
61	SA14	In	To	U34*	88	–TEST	In	To	PWGOUT
62	SA15	In	To	U34*	89	KCLK	In	To	U34*
63	–RAS0	Out	From	SA15	90	VDDI			
64	–RAS1	Out	From	SA14	91	GPIO9	In	To	U34*
65	–RAS2	Out	From	SA13	92	GPIO8	In	To	U34*
66	VSSR				93	GPIO7	In	To	U34*
67	–RAS3	Out	From	SA12	94	GPIO6	In	To	U34*
68	–CAS0	Out	From	SA11	95	GPIO0	In	To	U34*
69	–CAS1	Out	From	SA10	96	GPIO1	In	To	U34*
70	–CAS2	Out	From	–CAS3	97	VDDRD			
71	–CAS3	In	To	–CAS2	98	GPIO2	In	To	U34*
72	–SMIIN	In	To	U34*	99	GPIO3	In	To	U34*
73	NMI/–SMIOUT	Out	From	INTR	100	32KOUT	Out	From	U34*

Notes: * U34 signals are tested differently. U34 is a large NAND gate and all signals listed at "To" are inputs to the NAND gate. The two signals listed as "From" are connected to the output of the NAND gate.

–IOR –> –IOW –> SA5 –> SA6 –> SA7 –> SA8 –> SA9 –>
–> SD0 –> SD1 –> SD2 –> SD3 –> SD4 –> SD5 –> SD6 –> SD7 –>
–> GPIO0 –> GPIO1 –> GPIO2 –> GPIO3 –> GPIO6 –> GPIO7 –> GPIO8 –> GPIO9 –>
–> SA0 –> SA1 –> SA2 –> SA3 –> SA4 –> RSTDRV –> –SADS –> KCLK –> INMI –>
–> EXT –> RI –> –SMIIN –> –RCRESET –>>>> To I/O Pads GPIO4/32KOUT

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5.0 V ±10%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
I/O Read/Write Timings					
tSU1	Address Setup Time	55		ns	
tH2	Address Hold Time	20		ns	
tSU3	AEN Setup Time	55		ns	
tH4	AEN Hold Time	20		ns	
tPW5	Command Pulse Width	125		ns	
tSU6	Write Data Setup	60		ns	
tH7	Write Data Hold	20		ns	
tD8	Read Data Delay	0	130	ns	CL = 200 pF
tH9	Read Data Hold	5	50	ns	CL = 50 pF
WC	Write Cycle	280		ns	
RC	Read Cycle	280		ns	
VL82C323 Pin Timing					
t10	–RAS Precharge Time (Burst Refresh)	125		ns	
t11	–RAS On Time (Burst Refresh)	250		ns	
tD12	Burst Refresh to Suspend Refresh Delay	15	31	µs	
t13	–RAS On Time Suspend Mode Refresh	170	610	ns	
t14	Suspend Refresh Cycle Time (Std. Ref.)	15		µs	
t15	Suspend Refresh Cycle Time (Slow Ref.)	124		µs	
tD16	PWGIN to PWGOUT Delay from –RCRESET	0.53	1.035	s	
tD17	–RCRESET to PWGOUT Delay	0.53	1.035	s	
tD18	–RCRESET to VP7-VP2 Delay	0	40	ns	

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5.0 V ±10%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
VL82C323 Pin Timing (Cont.)					
tD19	PWGOUT to VP1 Delay from –RCRESET				0.5 sec Typical
tD20	EXT to VP7-VP2 Delay	0	40	ns	
tD21	PWGIN to PWGOUT Delay from EXT	0.53	1.03	s	
tD22	PWGOUT to VP1 Delay from EXT				0.5 sec Typical
tD23	INMI to NMI Delay	0	40	ns	
tPW24	EXT Pulse Width Low	63		ms	
t25	–SLOWCLK or –KBSLOWCK Low	288		ns	
t26	–SLOWCLK or –KBSLOWCK High	288		ns	
tPW27	EXTACT Pulse Width High	60		ns	
tD28	Resume Command to PMU Refresh Burst Delay	0.53	1.03	s	
tD29	Suspend Command to Suspend Active Delay	0.53	1.03	s	
t30	PWGOUT Low to PMU Driving –CAS Low	560		ns	
t31	–CAS Low to Start of 1024 Refresh Burst	150		ns	
tPW32	NMI Pulse Width High	570		ns	
t33	–SADS to –NMI/–SMIOUT		40	ns	

FIGURE 6. WRITE CYCLE TIMING

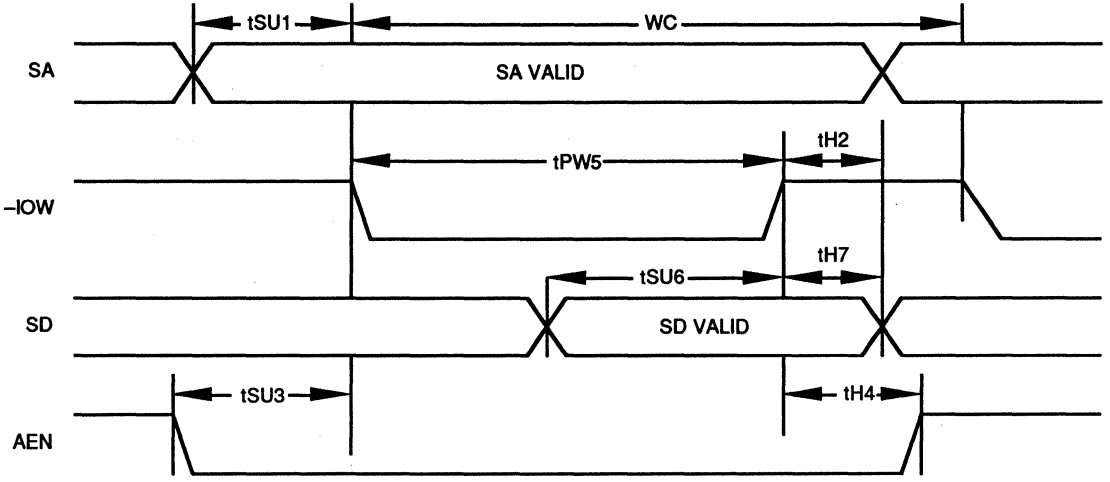


FIGURE 7. READ CYCLE TIMING

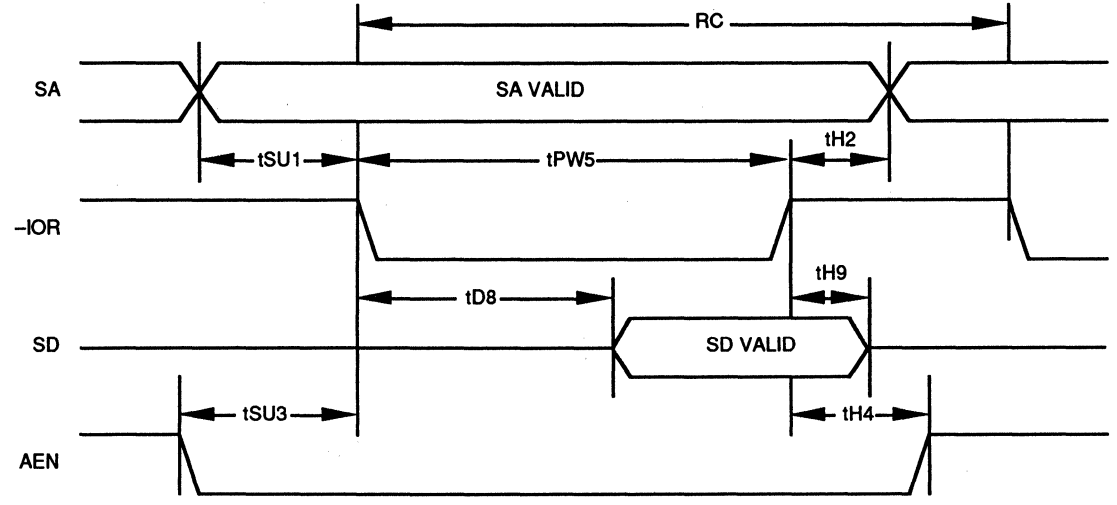


FIGURE 8. –RAS TIMING: ENTERING SUSPEND MODE WITH PMU DRIVEN REFRESH
(See Figure 23 for more system details)

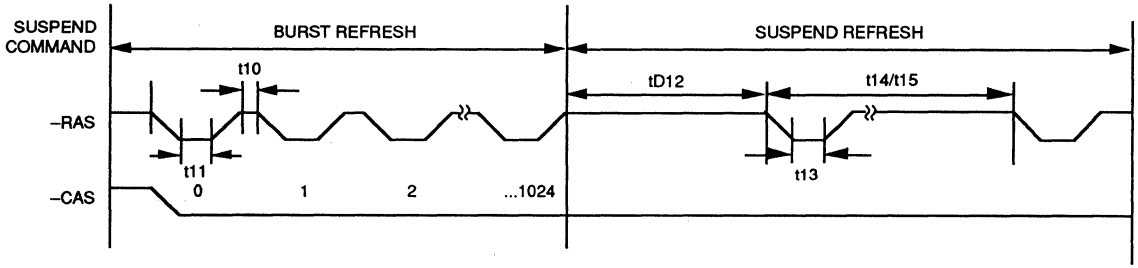


FIGURE 9. –RAS TIMING: LEAVING SUSPEND MODE WITH PMU DRIVEN REFRESH
(See Figure 23 for more system details)

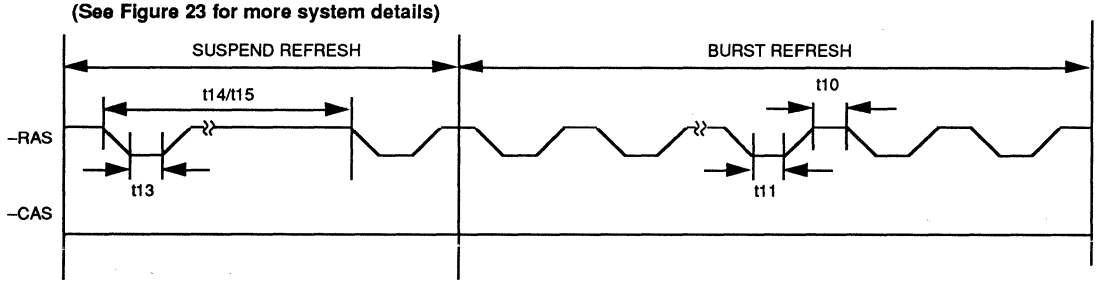


FIGURE 10.–RAS TIMING: ENTERING SELF-REFRESH MODE

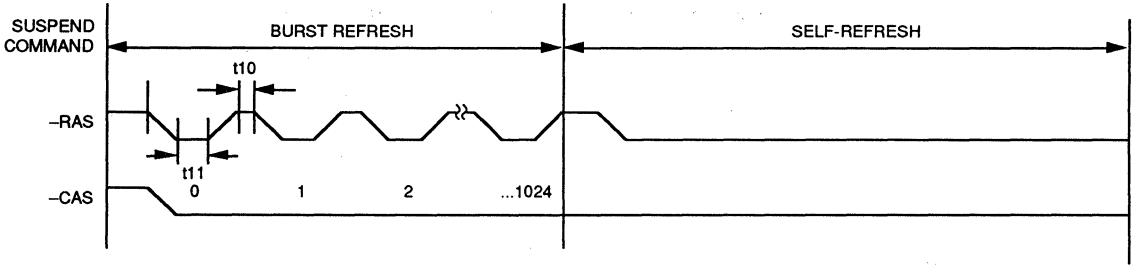


FIGURE 11.–RAS TIMING: LEAVING SELF-REFRESH MODE

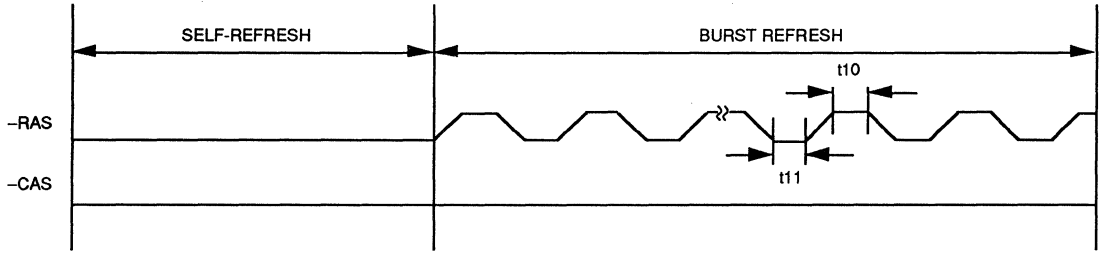
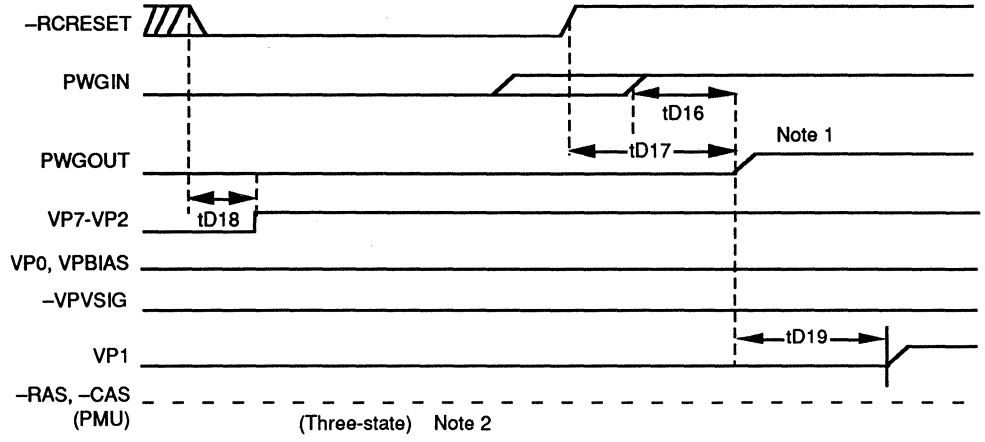


FIGURE 12. POWER-UP FROM –RCRESET TIMING (NO LCD AUTO-SEQUENCING)



Notes: 1. –RCRESET and PWGIN, whichever activates last 0.5 to 1.0 sec later, the VL82C323 drives PWGOUT high.

2. –RAS and –CAS from the VL82C323 are three-stated except when the VL82C323 enters the Suspend Mode. During the Suspend Mode the VL82C323 performs CAS-before-RAS refresh.

FIGURE 13. POWER-UP FROM EXT TIMING (NO LCD AUTO-SEQUENCING)

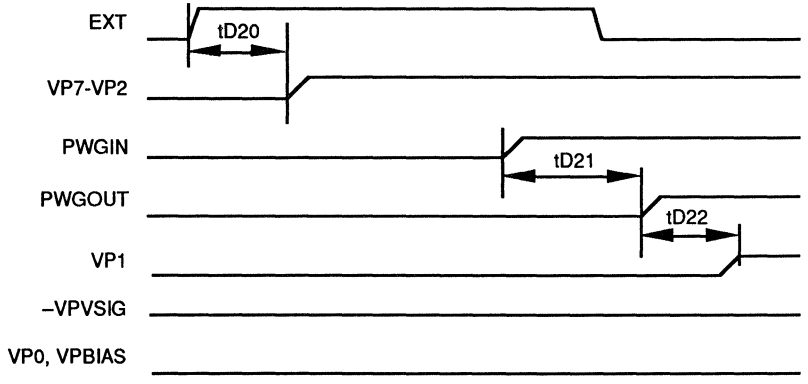
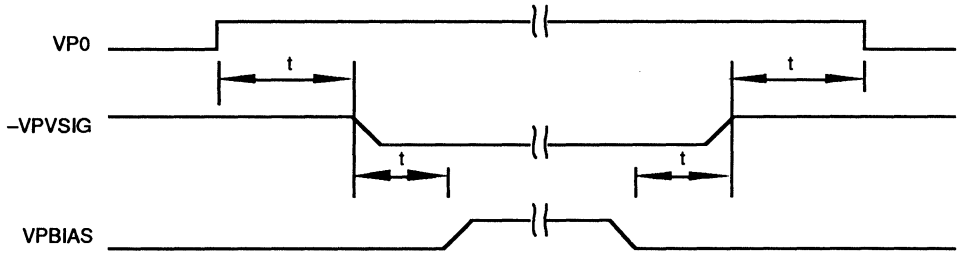


FIGURE 14. LCD AUTO-SEQUENCING TIMING



Note: t = the LCD sequencing time. t is based on the setup of D4 (data bit 4) of the MISCSET Register. The following table shows the requirements to enable LCD sequencing.

D4 = 1

D3	D2	t Delay
0	0	8 ms
0	1	15 ms
1	0	31 ms
1	1	125 ms

FIGURE 15. INMI TO NMI TIMING (NMI MODE)

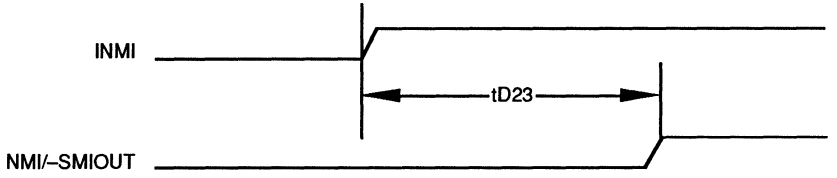
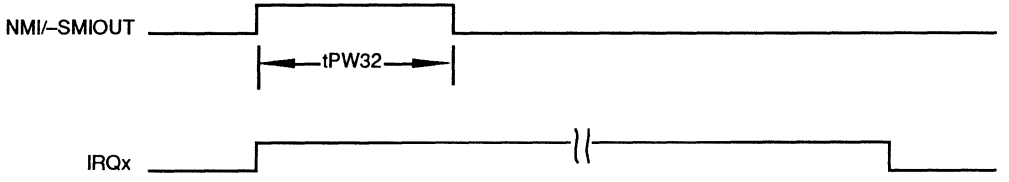


FIGURE 16. INTERNAL INTERRUPT GENERATION TIMING (NMI MODE)



Note: –SMI remains active until the falling edge of –SADS. IRQx remains active until the NMICAUSE Register is read.

FIGURE 17. –SADS TO –SMIOUT TIMING

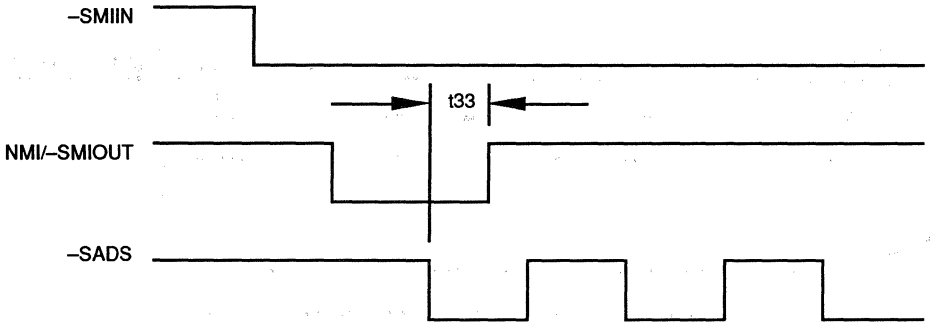
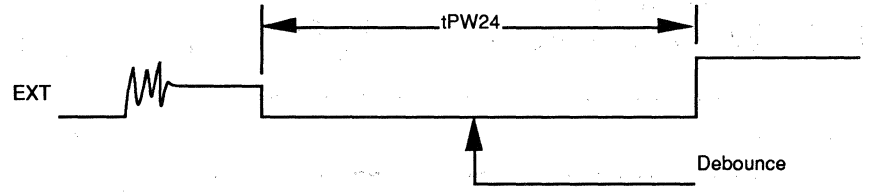


FIGURE 18. EXT TIMING (EXT CAUSES NMI FOR SUSPEND)



Note: EXT is internally debounced. It is required to go low for a minimum of 63 ms.

FIGURE 19. CLOCK CONTROL SWITCHING TIMING

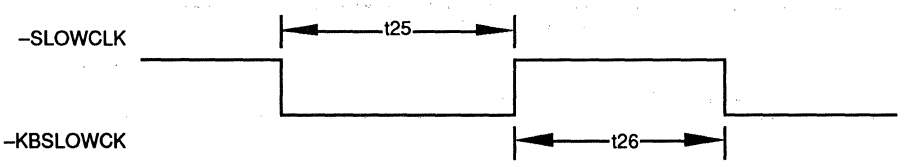
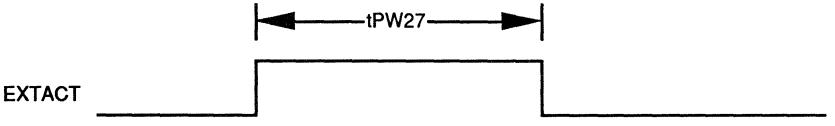


FIGURE 20. EXTACT TIMING



Note: EXTACT can remain high or low.

FIGURE 21. POWER MODE TIMING

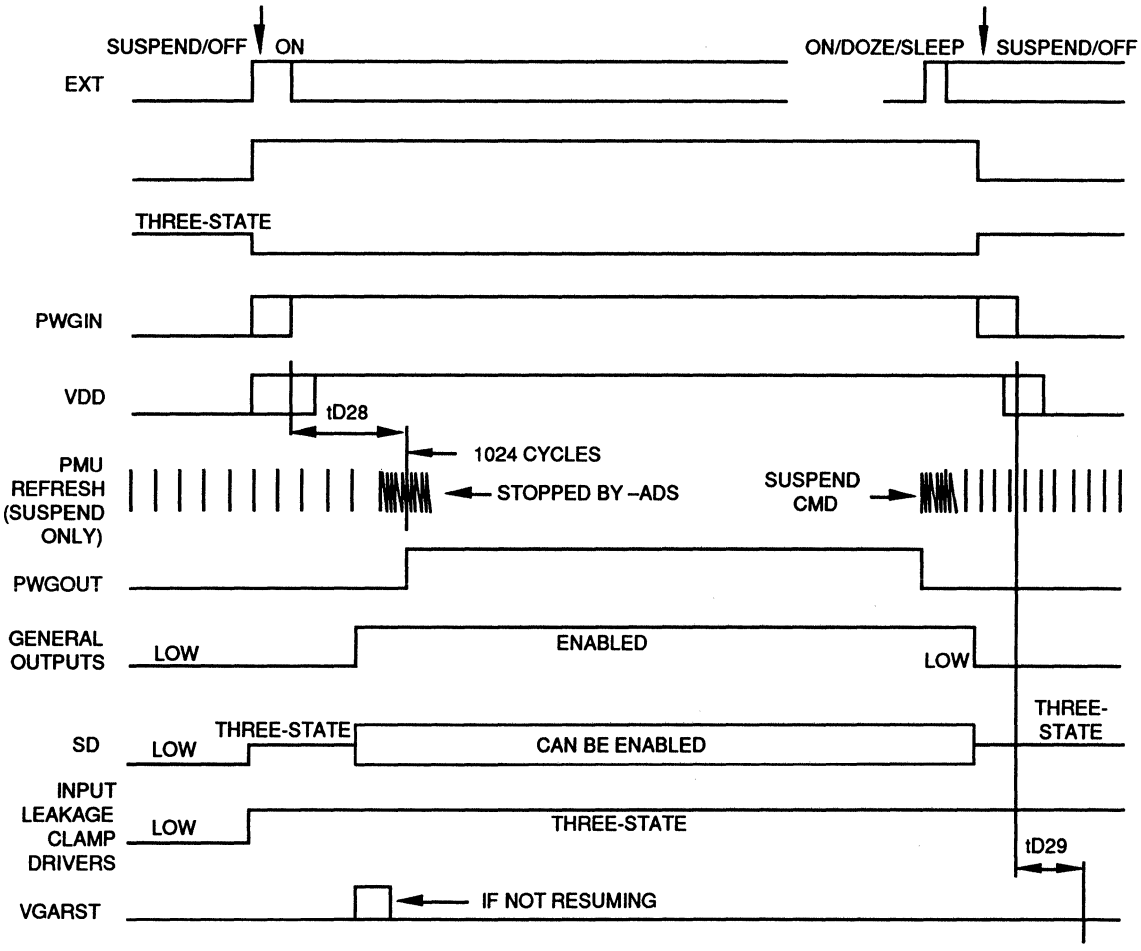
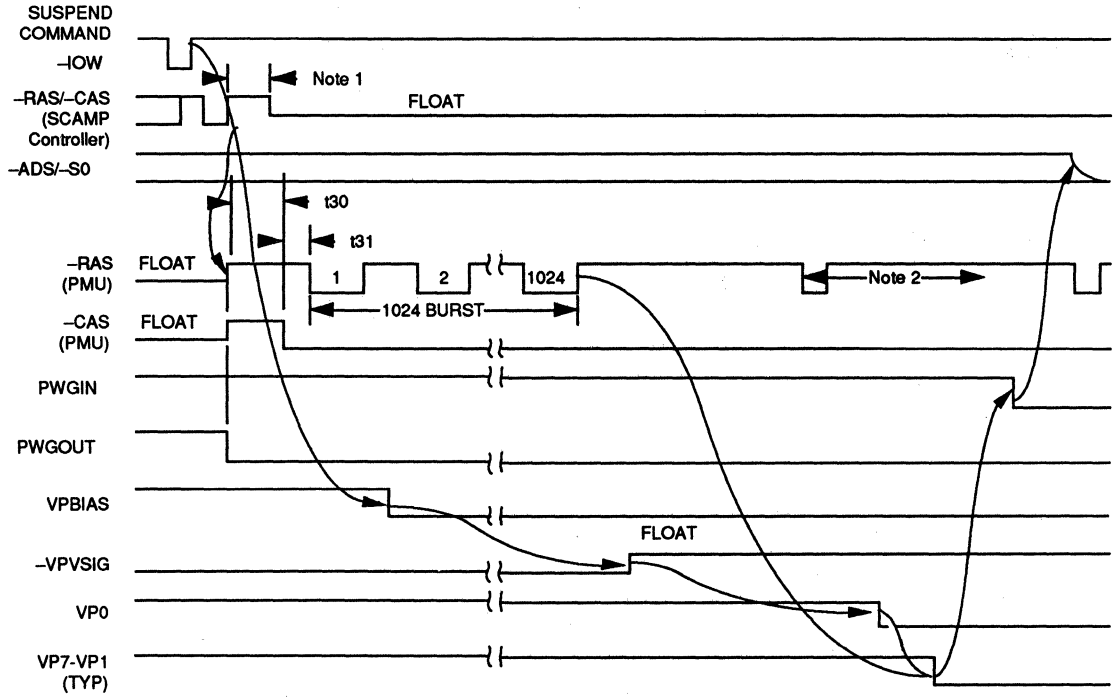


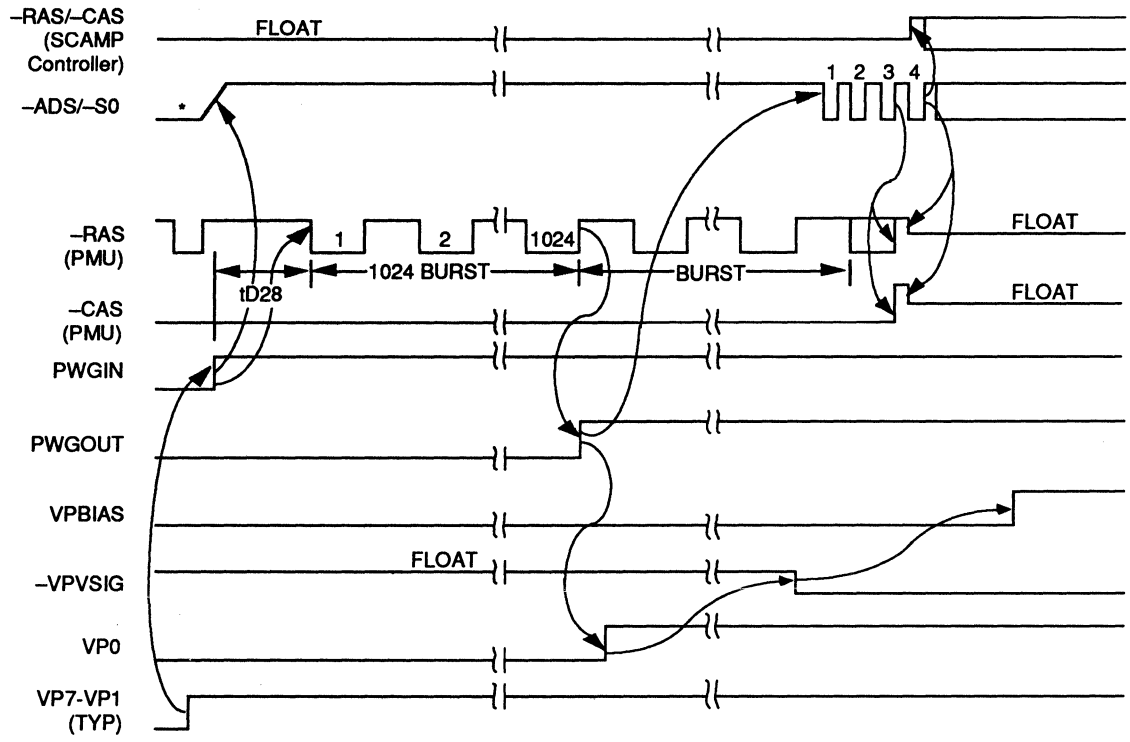
FIGURE 22. ON MODE TO SUSPEND MODE TIMING



Notes: 1. The SCAMP Controller floats RAS-before-CAS line within 400 ns after the falling edge of PWGOUT.

2. After completion of the 1024 cycle refresh burst, normal CAS-before-RAS refresh occurs at the programmed rate (15 or 122 µs).

FIGURE 23. SUSPEND MODE TO ON MODE TIMING



* Driven low by the VL82C323 during the Suspend Mode.

FIGURE 24. OFF MODE TO ON MODE TIMING WITH LCD SEQUENCING

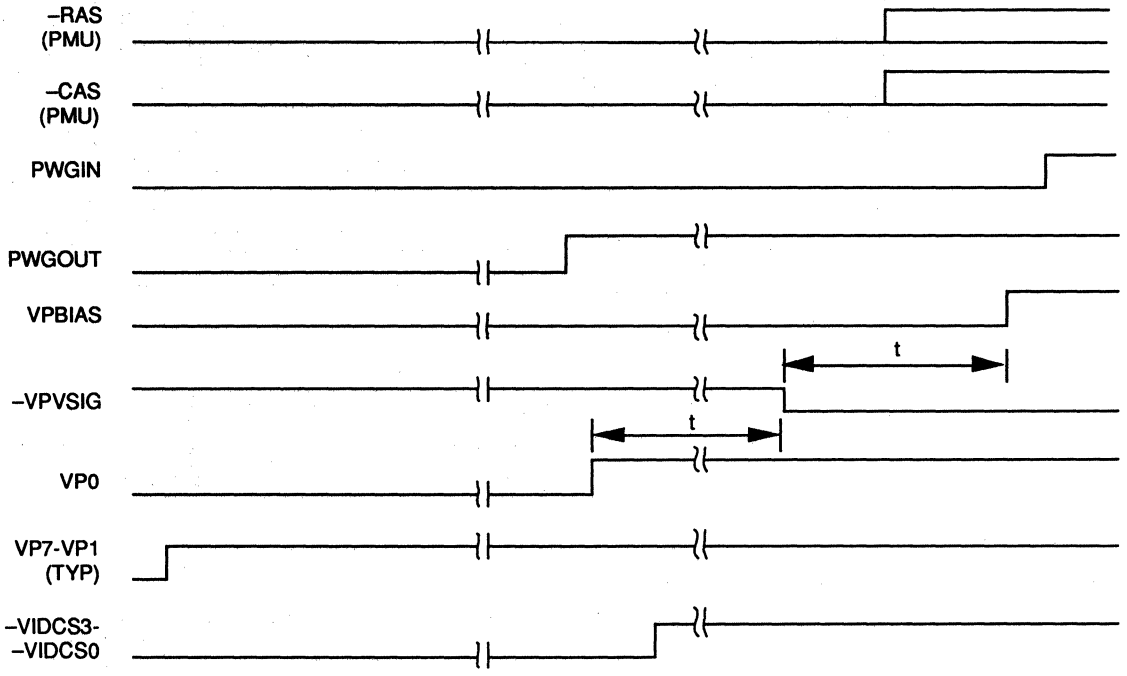
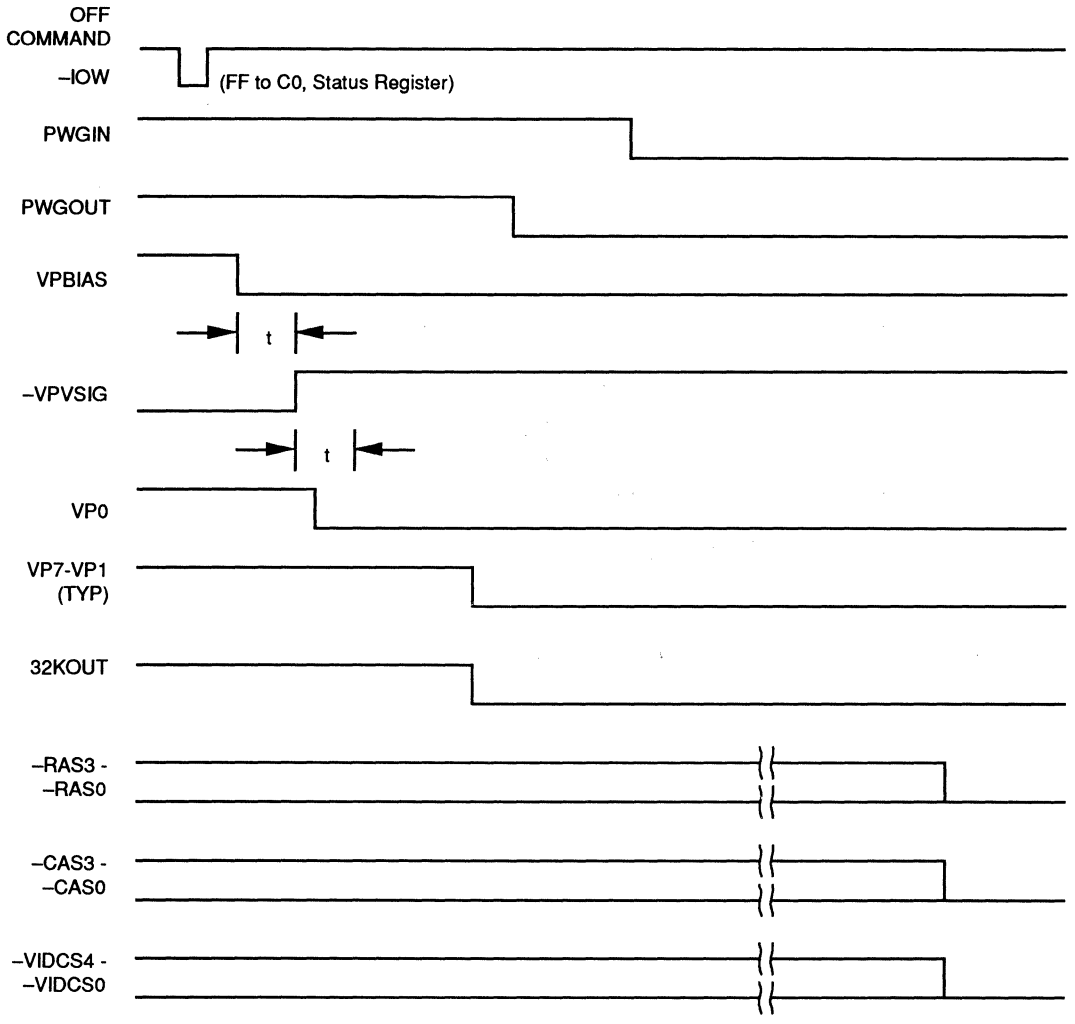
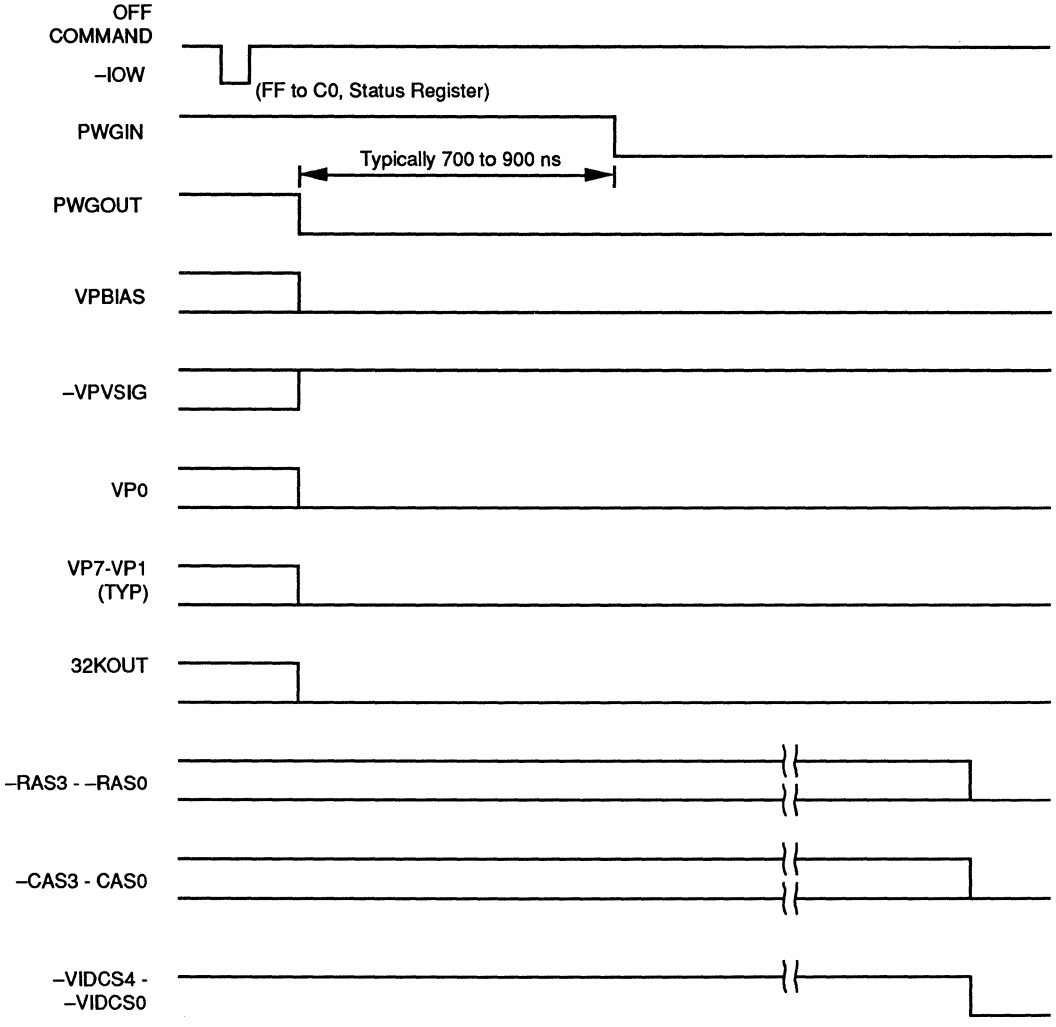


FIGURE 25. ON MODE TO OFF MODE TIMING WITH LCD SEQUENCING



Programmed by bits 2 and 3 (LCDTMG1, LCDTMG0) in the MISCSET Register with bit 4 (EN_LCDSEQ) high. 8 ms default.

FIGURE 26. ON MODE TO OFF MODE TIMING WITH NO LCD SEQUENCING



ABSOLUTE MAXIMUM RATINGS

Ambient Temperature –10°C to +70°C

Storage Temperature –65°C to +150°C

Supply Voltage to Ground Potential –0.5 V to 7.0 V

Applied Output Voltage –0.5 V to VDD + 0.5 V

Applied Input Voltage –0.5 V to VDD + 0.5 V

Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

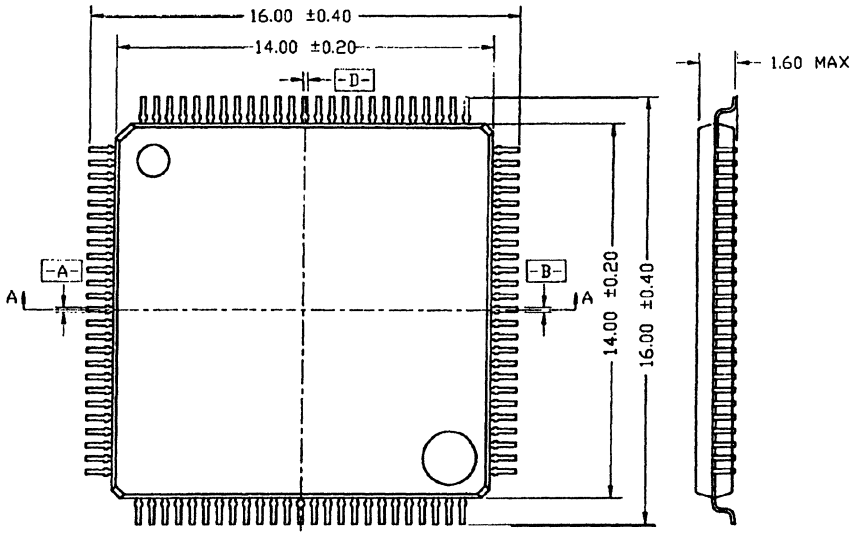
DC CHARACTERISTICS - 5.0 VOLT OPERATION: TA = 0°C to +70°C, VDD = 5.0 V ±10, VSS = 0 V

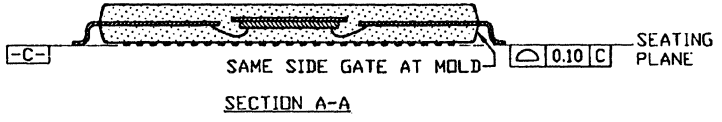
Symbol	Parameter	Min	Max	Unit	Condition
VIL	Input Low Voltage	–0.3	0.8	V	TTL-Compatible Inputs
VIH	Input High Voltage	2.4	VDD + 0.3	V	TTL-Compatible Inputs
VILC	Input Low Voltage	–0.3	VDD x 0.2	V	CMOS-Compatible Inputs
VIHC	Input High Voltage	VDD x 0.70	VDD + 0.3	V	CMOS-Compatible Inputs
VOL1	Output Low Voltage for Pins with -1 Pad Types*		0.45	V	IOL = 8 mA
			0.20	V	IOL = 100 µA
VOL2	Output Low Voltage for Pins with -2 Pad Types*		0.45	V	IOL = 12 mA
			0.20	V	IOL = 100 µA
VOL3	Output Low Voltage for Pins with -3 Pad Types*		0.45	V	IOL = 12 mA
			0.20	V	IOL = 100 µA
VOL4	Output Low Voltage for Pins with -4 Pad Types*		0.45	V	IOL = 24 mA
			0.20	V	IOL = 100 µA
VOH1	Output High Voltage for Pins with -1 Pad Types*	2.4	3	V	IOH = –4 mA
		VDD – 0.20		V	IOH = –100 µA
VOH2	Output High Voltage for Pins with -2 Pad Types*	2.4		V	IOH = –6 mA
		VDD – 0.20		V	IOH = –100 µA
VOH3	Output High Voltage for Pins with -3 Pad Types*	2.4		V	IOH = –6 mA
		3.5		V	IOH = –100 µA
VOH4	Output High Voltage for Pins with -4 Pad Types*	2.4		V	IOH = –6 mA
		VDD – 0.20		V	IOH = –100 µA
ILI	Input Leakage Current		±3	µA	0.1 V ≤ VIN ≤ VDD – 0.1 V
ILO	Output Three-State Leakage Current		±3	µA	0.1 V ≤ VOUT ≤ VDD – 0.1 V
LIPU	Input Current - Internal Pull-up	–30	–500	µA	VIN = 0.1 V
IDDSB	Static Power Supply Current		225	µA	No DC Loads. Outputs Open. VIL = 0.1 V, VIH = VDD – 0.1 V
IDDOP	Dynamic Power Supply Current		3.5	mA/MHz	No DC Loads. Outputs Open. VIL = 0.1 V, VIH = VDD – 0.1 V
CIN	Input or Output Capacitance		10	pF	
			15	pF	
COUT	Output Capacitance		10	pF	

* Refer to the table "Pin Type by Operational State" on pages 3 and 4 for pad type information.

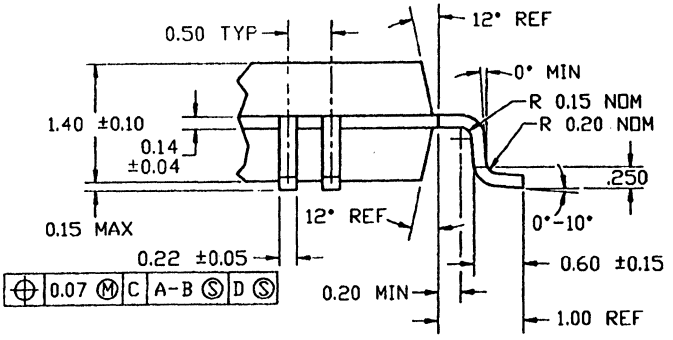
PACKAGE OUTLINE

100-LEAD THIN (PLASTIC) QUAD FLAT PACK





SECTION A-A



Notes: 1. All dimensions are in millimeters.
2. Leadframe material copper (OLIN 7025 or KLF125)
3. Mark of SG Indicates same side gate at mold.
4. To be molded cavity down (see section A-A).

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