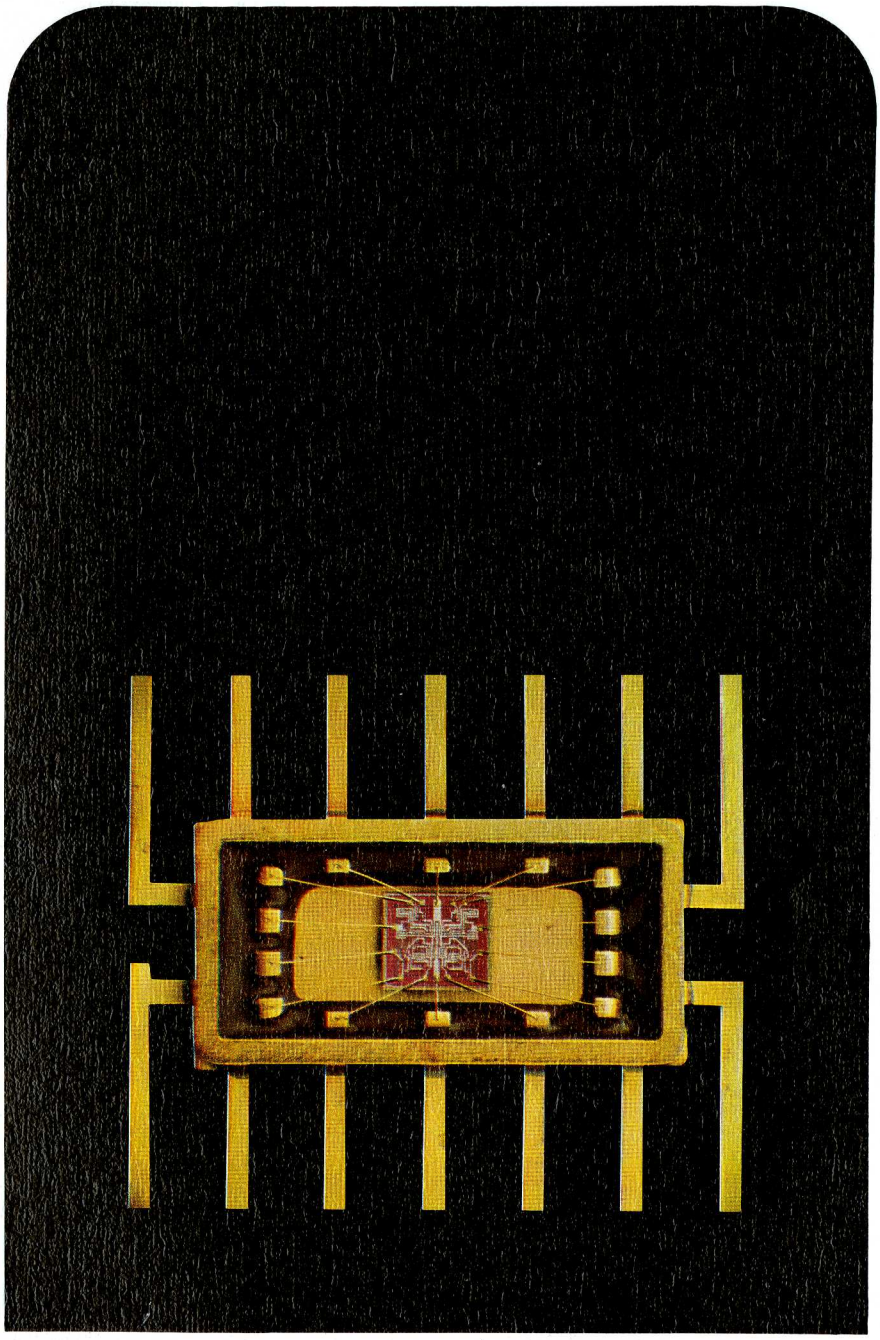

Semiconductor Integrated Circuits

TEXAS INSTRUMENTS INCORPORATED • SEMICONDUCTOR-COMPONENTS DIVISION

Applications Index

Digital Integrated Circuits

Typical Propagation Delay, nsec	Typical Power Dissipation per gate, mw	Typical Noise Immunity, mv	Temperature Range, °C	Logic Configuration	TI Logic Family	Page No.
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13	10	1000	−55° to +125°	TTL	Series 54	4-5
13	10	1000	0° to +70°	TTL	Series 74	4-5
25	8	750	−55° to +125°	DTL	Series 1500	14-15
25	8	750	0° to +70°	DTL	Series 1580	14-15
30	10	300	−55° to +125°	mod. DTL	Series 53	6-8
30	10	300	0° to +70°	mod. DTL	Series 73	6-8
35	4	150	−55° to +125°	RTL	Series 1700	16-17
130	2	200	−55° to +125°	RCTL	Series 51/51R	10-13
140	20-40	500	0° to +65°	DTL	Minuteman Series	18-19

Linear Integrated Circuits

Application	Series 52 (Pg 20-22)						Series 55 (Pg 23)		Minuteman Series (Pg 24-26)							Special Amplifiers (Pg 27)		
	SN 521A	SN 522A	SN 523A	SN 524A	SN 525A	SN 526A	SN 5500	SN 5510	SN 350A	SN 352A	SN 354A	SN 355A	SN 340A	SN 342A	SN 348A	SN 777	SNX 1303	SNX 1304
Audio preamplifier																●		
Buffer amplifier	●	●		●		●												
Comparator			●		●				●	●								
Demodulator chopper											●							
Differential amplifier			●		●	●		●	●	●								
Differentiator	●	●		●		●												
Driver switch												●						
Hearing-aid amplifier																●		
IF amplifier								●										
Integrator	●	●		●		●												
Level detector			●	●	●	●	●						●					
Low-level switch													●					
Matrix switch															●			
Multivibrator	●	●		●		●												
Oscillator	●	●			●			●								●		
Pulse amplifier																		●
Read preamplifier														●				
Sense amplifier							●	●										
Summing amplifier	●	●		●		●												
Video amplifier								●									●	
Voltage regulator			●	●	●	●			●	●								

Semiconductor Integrated Circuits

Semiconductor integrated circuits (SOLID CIRCUIT® semiconductor networks) are complete electronic circuits fabricated within monolithic bars of silicon, using diffusion techniques to form transistor, diode, resistor, and capacitor elements. Up to 82 such elements are available in a single network bar. The elements needed for a particular circuit are interconnected by depositing a metallic lead pattern over the oxide-protected surface of the bar, making contact only where "windows" are left in the oxide.

Advantages of using TI integrated circuits include lower system cost, improved system reliability, and reduced size, weight and power consumption. These benefits have been proved in hundreds of equipment applications ranging from the deep-space probe of NASA's IMP-A satellite to NAA/Autonetics' Minuteman II guidance system to Zenith's Micro-Lithic* hearing aid.

TI pioneered integrated-circuit technology, filing basic patents in the field as early as 1959. These patents were assigned to TI in 1964. Today, TI offers you the broadest line of semiconductor integrated circuits in the industry—more than 125 standard digital, linear, and memory networks.

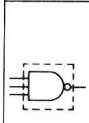
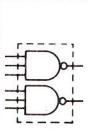
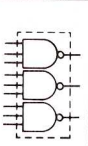
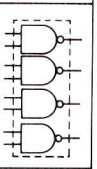
Special circuits for your particular application can be custom designed by TI's large and experienced engineering staff. In its digital line, TI has demonstrated competence in all the various logic configurations — TTL, DTL, RCTL, RTL, ECL, and DCTL — and presently uses several types of silicon planar structures.

Features of TI's linear circuits include wide frequency response, high gain, and high common-mode rejection ratios. The linear circuit bars have been designed to facilitate construction of special linear circuits by using the Master Slice technique.

With this broad technical capability, TI can provide the optimum combination of circuit structure and package to solve your design problem. Large, advanced manufacturing facilities are available to handle anything from prototype to high-volume requirements.

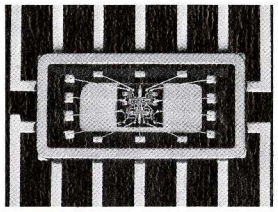
For additional information on any of the networks included in this bulletin, or for information on special circuits, contact your local TI Sales Engineer. His address and telephone number are listed on the back cover. Most networks are available off-the-shelf from your local TI distributor.

MULTI-FUNCTION APPROACH REDUCES SYSTEM COST, IMPROVES RELIABILITY

Network Package Content	Single Gate	Dual Gate	Triple Gate	Quad Gate
				
Value to User	$5	$10	$15	$20
Relative Network Manufacturing Cost	1.0	1.1	1.2	1.2
Cost per Circuit Function to User	$10	$5.50	**$4.00**	**$3.00**

TI's multi-function approach to network design and fabrication is extensively used. Since several circuits can now be built simultaneously in a single bar with only a nominal cost increase over that required to build one circuit, the cost-per-function can be reduced by a substantial percentage — up to 70 percent in some cases. Other multi-function advantages include fewer packages to handle, fewer external interconnections, fewer circuit boards, and less back-panel wiring — plus significantly improved system reliability.

**Zenith trademark*



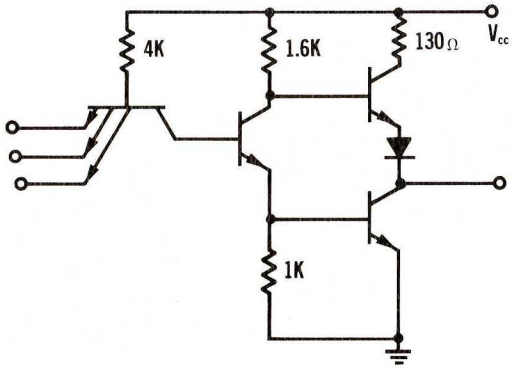
- High-speed saturated logic, low power dissipation
- High noise margin, high fan-out
- Excellent capacitance-driving capability
- Multiple circuit functions per package
- Two versions for application in military and industrial environments
- Standard TO-84 flat package (optional plug-in package for Series 74)

Series 54 and 74 TTL Digital Integrated Circuits

TYPICAL CHARACTERISTICS

Parameter	Basic Gate	Flip-flop
Propagation delay	13 nsec	40 nsec
Power dissipation	10 mw	60 mw
Fan-out	10	10
D-c noise margin	1 v	1 v
Supply voltage		
Series 54	4.5 to 5.5 v	4.5 to 5.5 v
Series 74	4.75 to 5.25 v	4.75 to 5.25 v
Temperature range		
Series 54	−55° to +125°C	−55° to +125°C
Series 74	0° to +70°C	0° to +70°C

Typical circuit diagram for Series 54/74 Positive NAND gate



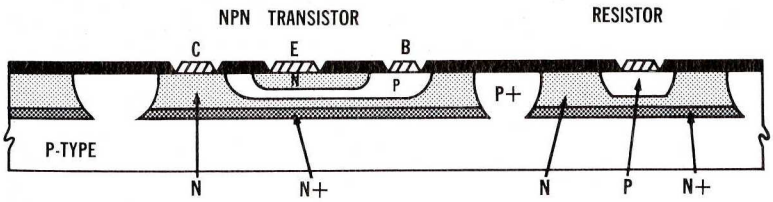
Transistor-Transistor Logic (TTL) fully exploits the inherent capabilities of integrated semiconductor structures, and the TI NAND gate circuit shown above is TTL at its best.

The multiple-emitter transistor input provides a faster turn-off time than other logic forms, thereby minimizing propagation delay. Because of unique circuit characteristics and exacting process control, propagation delays are almost independent of temperature and loading.

The output stage of the circuit provides low line-termination impedance in both logical "0" (12 ohms) and logical "1" (100 ohms) states. This contributes to low propagation delays and preserves undistorted waveforms even when driving large-capacitance loads.

Typical noise margin for Series 54/74 integrated circuits is one volt. Guaranteed worst-case noise margin is 400 millivolts for both logical "1" and logical "0" conditions. This wide margin for ground and signal-line noise is made possible by the strong overdrive to the output transistor and by the large V_{BE} drops inherent in the small transistor geometry.

Packages. TI's ¼" by ⅛" welded 14-lead flat pack, TO-84, is standard for both Series 54 and 74 versions. An optional package for Series 74 is TI's new 16-pin plug-in package featuring rigid pins for 100-mil grid spacings.

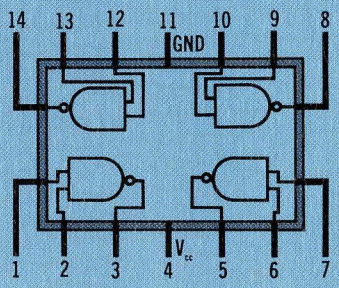


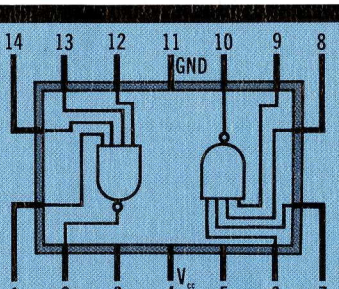
Diffused-planar, double-epitaxial structure used for Series 54/74 networks

SN5400/SN7400

Quadruple 2-input Positive NAND Gate

Propagation delay — 13 nsec
Fan-out — 10
Power dissipation — 10 mw per gate





Dual 4-input Positive NAND "Power" Gate

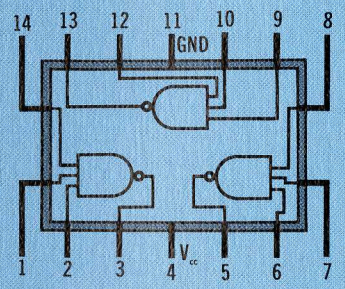
Propagation delay—18 nsec
Fan-out — 30
Power dissipation — 25 mw per gate

SN5440/SN7440

SN5410/SN7410

Triple 3-input Positive NAND Gate

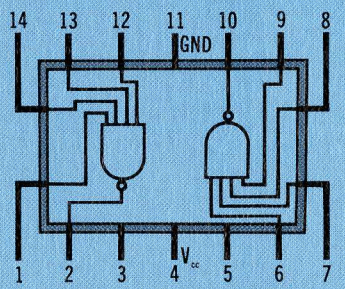
Propagation delay — 13 nsec
Fan-out — 10
Power dissipation — 10 mw per gate



SN5420/SN7420

Dual 4-input Positive NAND Gate

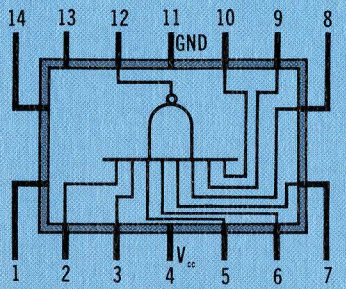
Propagation delay — 13 nsec
Fan-out — 10
Power dissipation — 10 mw per gate

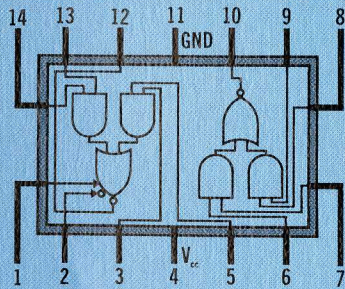


SN5430/SN7430

8-input Positive NAND Gate

Propagation delay — 15 nsec
Fan-out — 10
Power dissipation — 10 mw

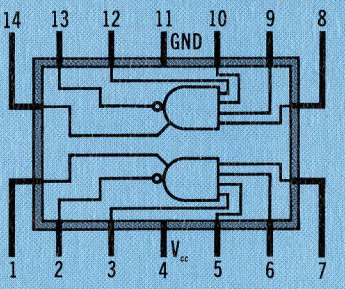




Dual EXCLUSIVE-OR Gate with Expander Inputs

Propagation delay — 15 nsec
Fan-out — 10
Power dissipation — 14 mw per gate

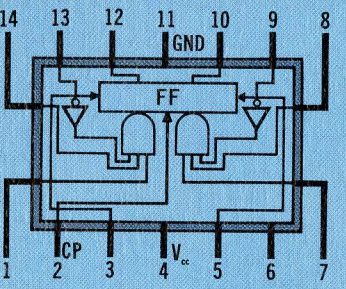
SN5450/SN7450



Dual 4-input Expander

Fan-out (max number of expanders connected to SN5450 or SN7450) — 4
Power dissipation — 5 mw per expander

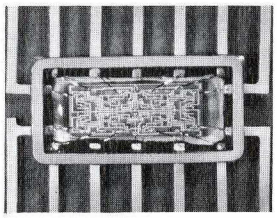
SN5460/SN7460



Single-phase J-K Flip-flop

Propagation delay — 40 nsec
Fan-out — 10
Power dissipation — 60 mw

SN5470/SN7470



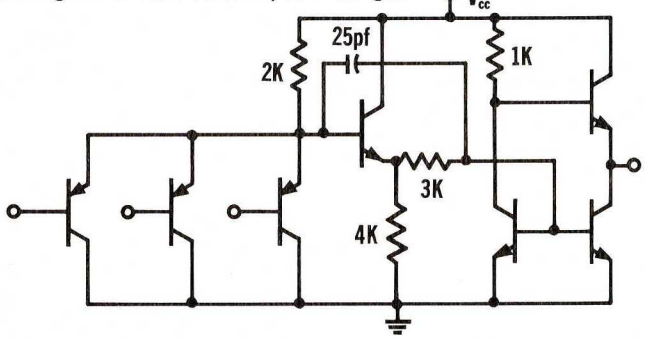
- Multiple circuit functions per package
- Full saturated NAND/NOR logic flexibility
- High fan-out
- Medium speed, medium power dissipation
- Two versions for application in military and industrial environments
- Standard TO-84 and TO-89 flat packages (optional plug-in package for Series 73)

Series 53 and 73 Modified-DTL Digital

TYPICAL CHARACTERISTICS

Parameter	Basic AND Gate	Basic NAND Gate	Flip-flop
Propagation delay	5 nsec	30 nsec	60 nsec
Power dissipation	10 mw	10 mw	27 mw
D-c noise margin	300 mv	300 mv	300 mv
Fan-out	4	10	10
Supply voltage	3 to 4 v	3 to 4 v	3 to 4 v
Temperature range			
Series 53	–55° to +125°C	–55° to +125°C	–55° to +125°C
Series 73	——	0° to +70°C	0° to +70°C

Circuit diagram for basic Series 53/73 NAND gate



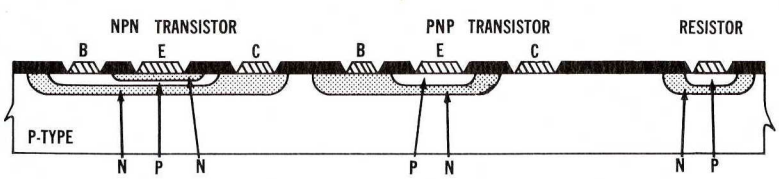
Multi-function networks. Each Series 53 and Series 73 bar contains between 50 and 80 elements — making it possible to provide quadruple gate and inverter networks, dual EXCLUSIVE-OR networks, or two complete J-K flip-flops in a single network package. This reduces the number of networks required per system — reducing cost and improving reliability. Each flip-flop can be used either as a counter or shift register.

Saturated NAND/NOR logic flexibility. An expandable gate, complementary inputs on the flip-flops, double-ended outputs, and a full family of networks make this the most flexible and powerful logic series in the industry.

Low noise susceptibility for capacitively coupled noise is provided by the low line-termination impedance in both the ON (50 ohms) and OFF (50 ohms) logic conditions.

Large-capacitance loads are easily driven at high speeds by the low-impedance output stage contained in each inverting network. Waveform integrity is preserved for capacitance loads of several hundred picofarads.

Two temperature ranges available. Series 53 is designed for operation over the full military temperature range of –55° to +125°C, and Series 73 is appropriate for limited-temperature applications (0° to 70°C) in industrial environments. TI's ¼" by ⅛" welded flat pack, TO-84 or TO-89, is standard for both versions. An optional package for most units in Series 73 is TI's new 16-pin plug-in package featuring pins for 100-mil grid spacings.

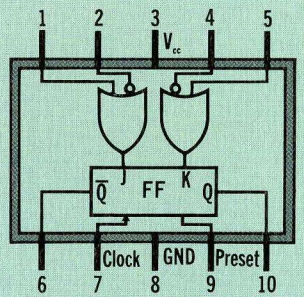


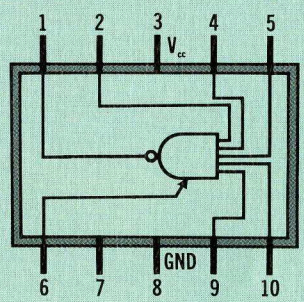
Triple-diffused structure used for Series 53/73 networks

SN530/SN7300*

Single-phase J-K Flip-flop with Preset

Propagation delay — 60 nsec
Fan-out — 10
Power dissipation — 27 mw





5-input Expandable NAND/NOR Gate

Propagation delay — 30 nsec
Fan-out — 10
Power dissipation — 10 mw

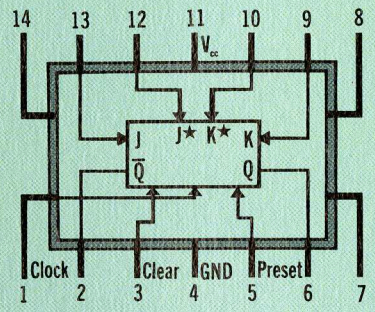
SN531/SN7310*

Integrated Circuits

SN5301/SN7301

J-K Flip-flop with Preset and Clear

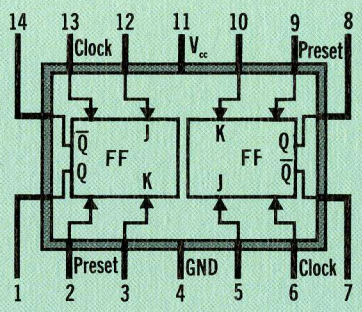
Propagation delay — 60 nsec
Fan-out — 10
Power dissipation — 27 mw



SN5302/SN7302

Dual J-K Flip-flop with Preset

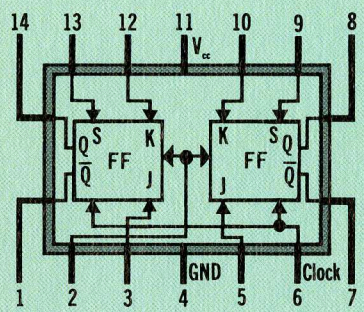
Propagation delay — 60 nsec
Fan-out — 10
Power dissipation — 27 mw per flip-flop

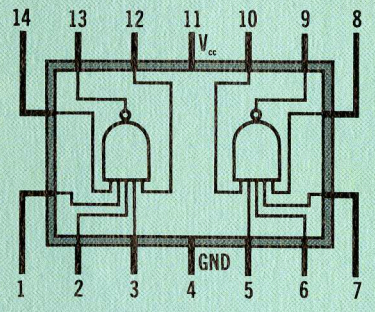


SN5304/SN7304

Dual J-K Flip-flop with Preset and Clear

Propagation delay — 60 nsec
Fan-out — 10
Power dissipation — 27 mw per flip-flop

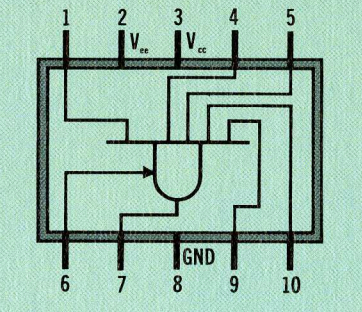




Dual 5-input NAND/NOR Gate

Propagation delay — 30 nsec
Fan-out — 10
Power dissipation — 10 mw per gate

SN5311/SN7311

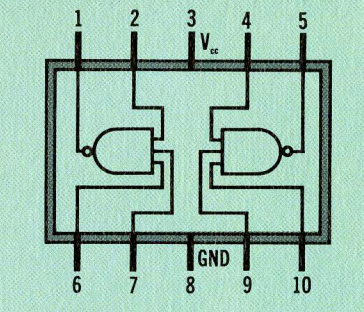


5-input AND/OR Gate or Expander†

Propagation delay — 5 nsec
Fan-out — 4
Power dissipation — 10 mw

†SN7320 is Expander only.

SN532/SN7320*



Dual 3-input NAND/NOR Gate

Propagation delay — 30 nsec
Fan-out — 10
Power dissipation — 10 mw per gate

SN533/SN7330*

*Pin numbers shown are for Series 53 10-lead networks. Series 73 networks follow the standard TO-89 numbering sequence as shown on page 29.

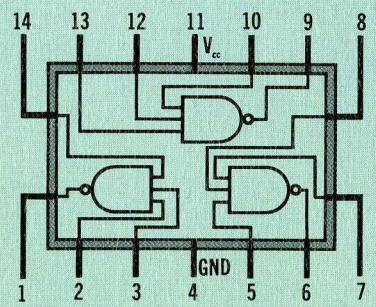
(Series 53/73 continued on next page)

(Series 53/73 continued)

SN5331/SN7331

Triple 3-input NAND/NOR Gate

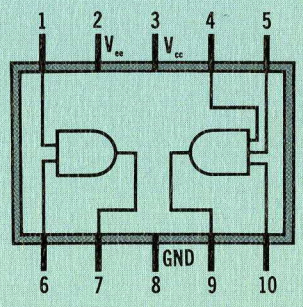
Propagation delay — 30 nsec
Fan-out — 10
Power dissipation — 10 mw per gate



SN534

Dual AND/OR Gate (2 and 3 Inputs)

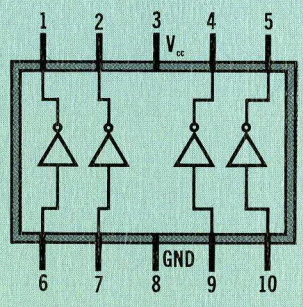
Propagation delay — 5 nsec
Fan-out — 4
Power dissipation — 10 mw per gate

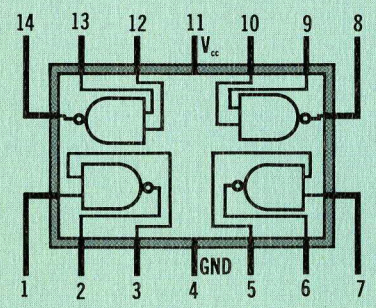


SN535/SN7350*

Quadruple Inverter/Driver

Propagation delay — 30 nsec
Fan-out — 10
Power dissipation — 9 mw per inverter

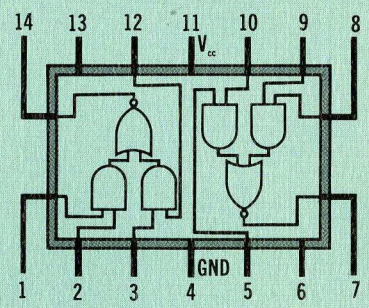




Quadruple 2-input NAND/NOR Gate

Propagation delay — 30 nsec
Fan-out — 10
Power dissipation — 10 mw per gate

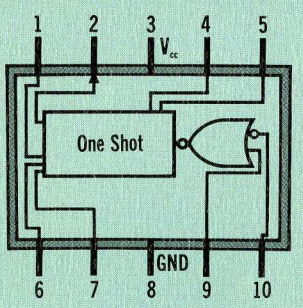
SN5360/SN7360



Dual EXCLUSIVE-OR Gate

Propagation delay — 90 nsec
Fan-out — 10
Power dissipation — 20 mw per gate

SN5370/SN7370

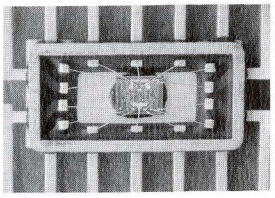


"One Shot" Monostable Multivibrator

Delay time — 100 nsec
Fan-out — 10
Power dissipation — 30 mw

SN5380/SN7380*

*Pin numbers shown are for Series 53 10-lead networks. Series 73 networks follow the standard TO-89 numbering sequence as shown on page 29.



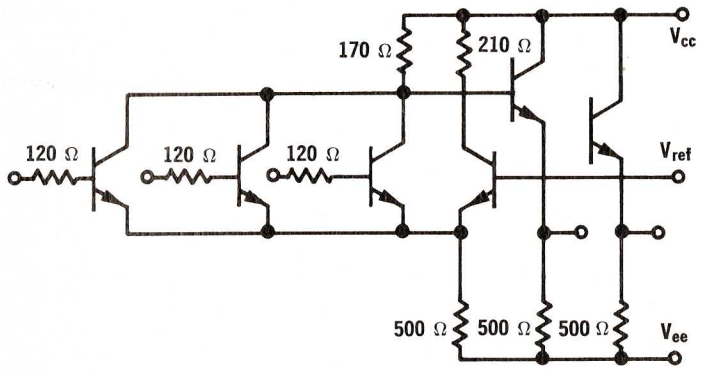
- Very high-speed unsaturated logic
- High degree of logic flexibility
- For application in large, high-speed computer systems
- Multi-function approach to system economy
- Standard TO-84 welded flat package or optional plug-in package

Series 70 ECL Digital Integrated Circuits

TYPICAL CHARACTERISTICS

Parameter	Basic Gate
Propagation delay	5 nsec
Power dissipation	40 mw+
Noise immunity	250 mv
Supply voltage	+1.25 v, −3.5 v
Temperature range	0° to +70°C

Typical circuit for basic Series 70 gate

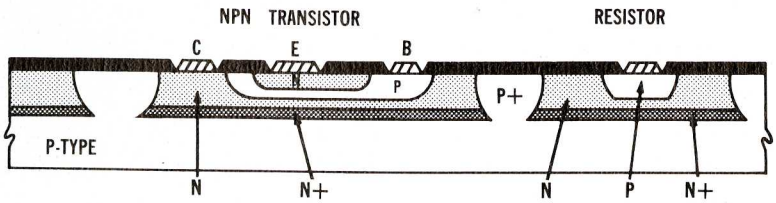


These unsaturated, emitter-coupled logic (ECL) gates feature high speed, moderate power dissipation, excellent logic flexibility, and the multi-function approach to system economy. The ECL gates were specifically designed for large high-speed, ground-based computer systems.

The SN7001 is a dual OR/NOR gate including two output resistors which may be connected to any of the four outputs. The SN7000 differs in having an additional pair of output resistors internally connected. Both units contain a 3-input and a 2-input gate.

Principal feature is a propagation delay of only 5 nsec. The gates have both inverting and non-inverting outputs, allowing considerable flexibility in system design. Also contributing to greater design flexibility is their capability of performing the "Dot-OR" function at the output with up to four gates simultaneously. This is made feasible because of the output resistors which may be left unconnected when not required. Using the resistors unconnected results in a reduction in power consumption.

The ECL gates are designed to operate effectively driving a 100-ohm transmission line. Symmetrical logical levels are +400 and −400 volts. Standard package is the ¼" by ⅛" flat pack (TO-84). An optional package is TI's new 16-pin plug-in package featuring pins for 100-mil grid spacings.

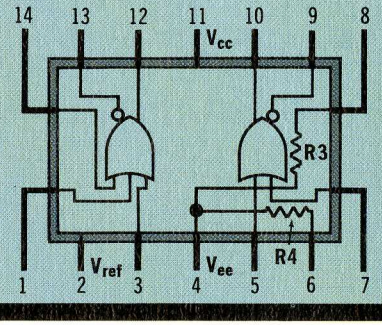


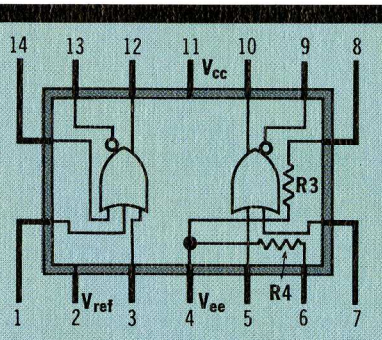
Planar diffused double-epitaxial structure used for Series 70 networks

SN7000
Dual OR/NOR Gate
(4 Load Resistors)

Propagation delay — 5 nsec
Power diss.—40 mw per gate,
(plus 25 mw per gate if internal output resistors are used)

Outputs 12 and 13 have resistors internally connected to Vee. Outputs 9 and 10 are open, and may be individually terminated or connected to Vee in a "Dot-OR" configuration at resistor R3 or R4.



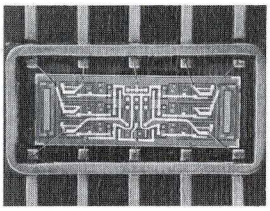


Dual OR/NOR Gate
(2 Load Resistors)

Propagation delay — 5 nsec
Power diss.—40 mw per gate,
(plus 25 mw per gate if internal output resistors are used)

Outputs 9, 10, 12, and 13 are open and may be individually terminated or connected to Vee in a "Dot-OR" configuration at resistor R3 or R4.

SN7001



- Very low power dissipation, high fan-out
- Proved reliability
- Master Slice capability
- Multiple circuit functions per package
- Familiar RCTL logic design
- Standard TO-84 and TO-89 welded flat packages

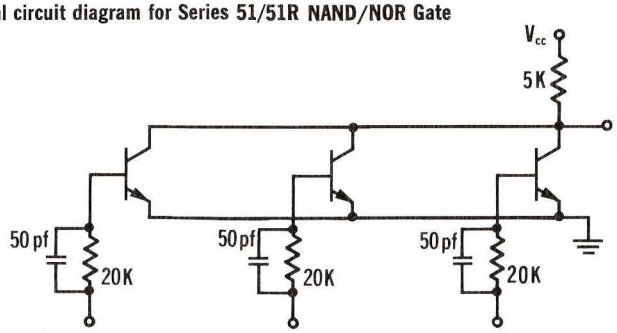
Series 51 and 51R RCTL Digital Integrated Circuits

TYPICAL CHARACTERISTICS

Parameter	Basic Gate	Flip-flop
Propagation delay	130 nsec @ 3 v 65 nsec @ 6 v	300 nsec
Power dissipation	2 mw @ 3 v	2 mw @ 3 v
Fan-out	5, 25*	4, 20*
D-c noise margin	200 mv	200 mv
Supply voltage	3 to 6 v	3 to 6 v
Temperature range	−55° to +125°C	−55° to +125°C

*with emitter-follower outputs

Typical circuit diagram for Series 51/51R NAND/NOR Gate



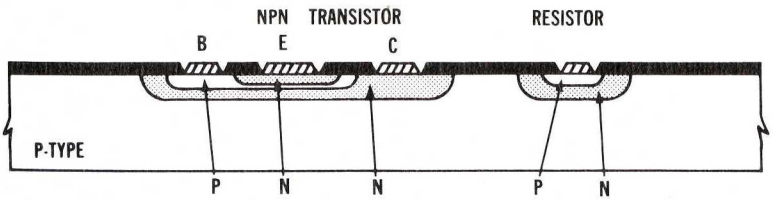
This compatible line of semiconductor integrated circuits features the lowest power drain in the industry . . . typically 2 mw at 3 v. For this reason, Series 51 networks are ideal for missile and space applications where power dissipation requirements are critical.

RCTL logic — familiar to designers — simplifies equipment design, as does the use of a single-phase clock. Series 51 networks have been used in systems employing clock rates well above 300 kc.

Proved reliability. More than five years of successful manufacturing experience, hundreds of equipment applications, and millions of hours of reliability testing stand behind every Series 51 network.

Series 51R for severe-environment applications. For these applications, you can now specify a standard line of semiconductor networks which parallels TI's standard Series 51 line. You get extra assurance of reliability through additional testing and processing. Each Series 51R network is subjected to:

- Centrifugal acceleration at 20,000 G in the Y_1 plane.
- Dynamic operation, burning-in each unit at 125°C for 168 hours.
- Radiographic inspection.

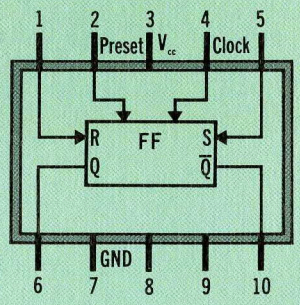


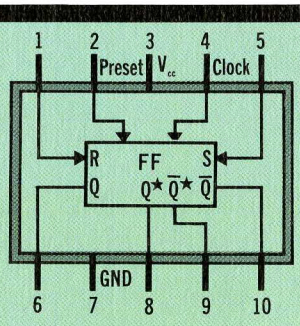
Triple-diffused planar structure employed in Series 51/51R networks

SN510A/SNR510

R-S Flip-flop/Counter

Fan-out — 4
Power diss.— 2 mw @ 3 v
Propagation delay — 300 nsec





Ripple-counter Flip-flop
(V_{CC} = 3 to 6 v)

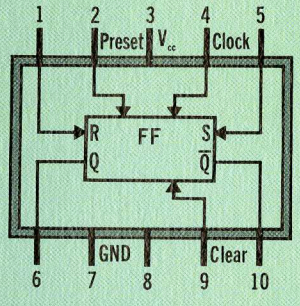
Fan-out
Collector output — 4
Emitter-follower — 16
Power diss.— 3 mw @ 3 v
Propagation delay — 300 nsec

SN5112/SNR5112

SN5101/SNR5101

R-S Flip-flop with Dual Preset

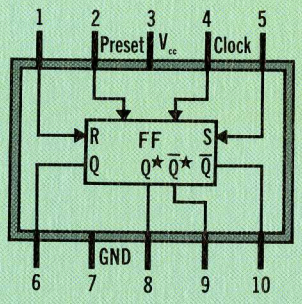
Fan-out — 4
Power diss.— 2 mw @ 3 v
Propagation delay — 300 nsec



SN511A/SNR511

R-S Flip-flop/Counter with Emitter-follower Outputs

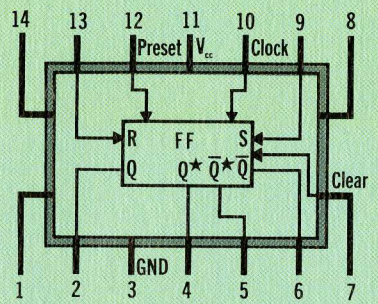
Fan-out
Collector output — 4
Emitter-follower — 20
Power diss.— 3 mw @ 3 v
Propagation delay — 300 nsec

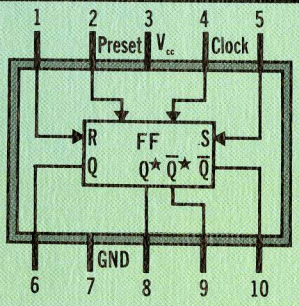


SN5111/SNR5111

R-S Flip-flop with Emitter-follower Outputs and Dual Preset

Fan-out
Collector output — 4
Emitter-follower — 20
Power diss.— 3 mw @ 3 v
Propagation delay — 300 nsec

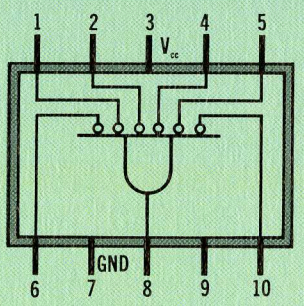




Ripple-counter Flip-flop (V_{CC} = 4 to 6 v)

Fan-out
Collector output — 4
Emitter-follower — 16
Power diss.— 4 mw @ 4 v
Propagation delay — 300 nsec

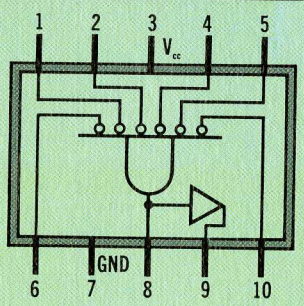
SN5113/SNR5113



6-input NAND/NOR Gate

Fan-out — 5
Power diss.— 2 mw @ 3 v
Propagation delay — 65 nsec @ 6 v

SN512A/SNR512



6-input NAND/NOR Gate with Emitter-follower Output

Fan-out
Collector output — 5
Emitter-follower — 25
Power diss.— 3 mw @ 3 v
Propagation delay — 65 nsec @ 6 v

SN513A/SNR513

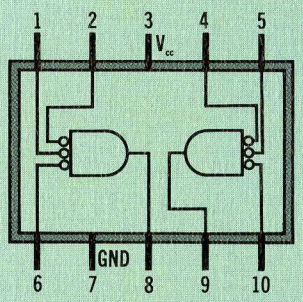
(Series 51/51R continued on next page)

(Series 51/51R continued)

SN514A/SNR514

Dual 3-input NAND/NOR Gate

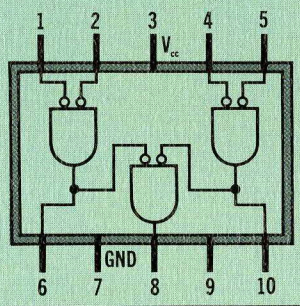
Fan-out — 5
Power diss.
2 mw/gate @ 3 v
Propagation delay — 65 nsec @ 6 v



SN515A/SNR515

EXCLUSIVE-OR Gate

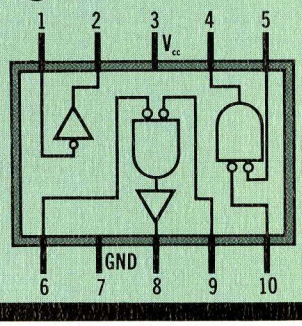
Fan-out
Auxiliary outputs — 4
Exclusive-OR output — 5
Power diss.— 3 mw @ 3 v
Propagation delay — 100 nsec @ 6 v

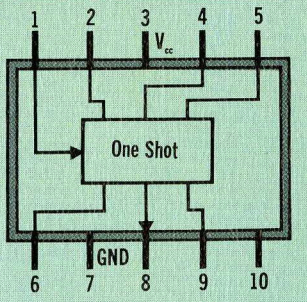


SN516A/SNR516

Dual 2-input NAND/NOR Gate and Inverter/Buffer

Fan-out
Collector output — 5
Emitter-follower output — 25
Power diss.
2 mw/gate @ 3 v
Propagation delay — 65 nsec @ 6 v

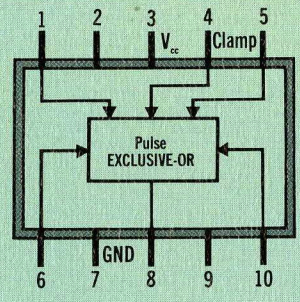




"One Shot" Monostable Multivibrator

Fan-out — 5
Power diss.— 2 mw @ 3 v
Pulse delay and pulse width adjustable by using internal and/or external R-C networks

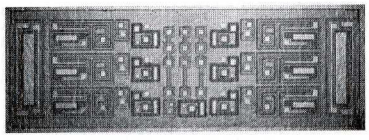
SN518A/SNR518



Pulse EXCLUSIVE-OR Gate

Fan-out — 5
Power diss.— 6 mw @ 3 v
Useful for up/down counter applications

SN5191/SNR5191



Master Slice capability. Circuit variations can be provided quickly and economically by changing the deposited lead pattern on the Series 51 Master Slice bar. Available are 31 circuit elements, including 7 npn transistors, 7 diodes, 3 resistors, 2 capacitors, and 6 R-C combinations which can be interconnected in scores of different configurations.

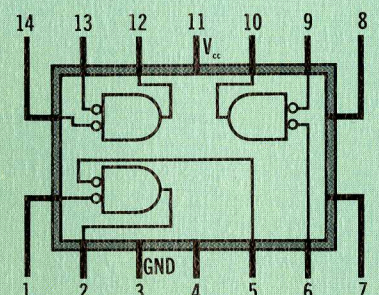
SN5161/SNR5161

Triple 2-input NAND/NOR Gate

Fan-out — 5

Power diss.
2 mw/gate @ 3 v

Propagation delay — 65 nsec @ 6 v



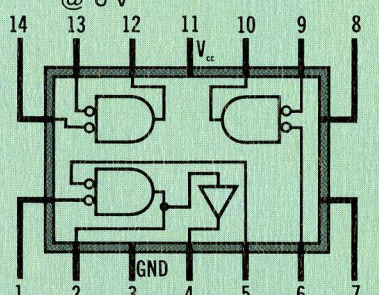
SN5162/SNR5162

Triple 2-input NAND/NOR Gate with Emitter-follower Output

Fan-out
Collector output — 5
Emitter-follower output — 25

Power diss.
2 mw/gate @ 3 v

Propagation delay — 65 nsec @ 6 v

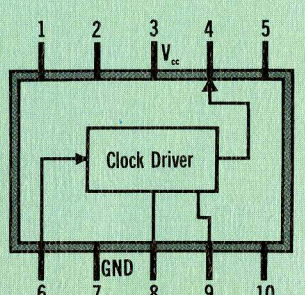


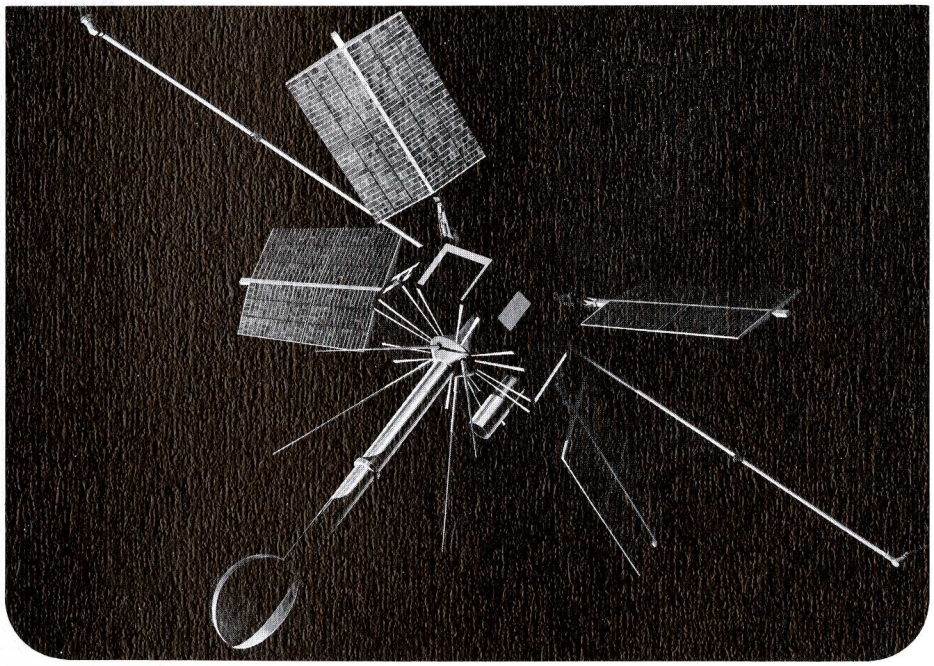
SN517A/SNR517

Clock Driver

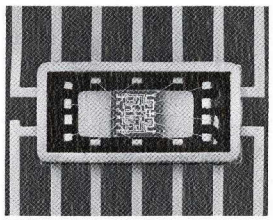
Fan-out, a-c — 20

Power diss.— 3 mw @ 3 v





Series 51 integrated circuits are used in the optical aspect computer of NASA's IMP satellites. These units have been operational in space since November, 1963.



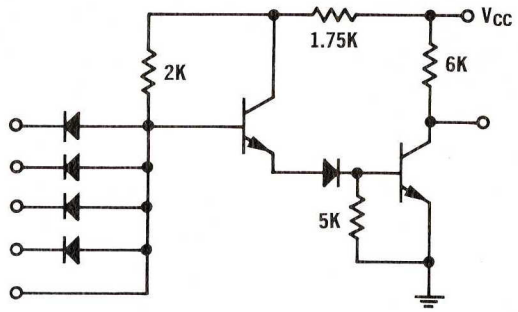
- High speed, low power dissipation
- High noise immunity
- Multiple circuit functions per package
- Single-ended outputs — "Dot-OR" capability
- Two versions for application in military and industrial environments
- Standard TO-84 welded flat package (Optional plug-in package for Series 1580)

Series 1500 and 1580 DTL Digital Integrated Circuits

TYPICAL CHARACTERISTICS

Parameter	Basic Gate	Flip-flop
Propagation delay	25 nsec	50 nsec
Power dissipation	5 mw	20 mw
Fan-out	8	7
D-c noise margin	750 mv	750 mv
Supply voltage	4.5 to 5.5 v	4.5 to 5.5 v
Temperature range		
Series 1500	–55° to +125°C	–55° to +125°C
Series 1580	0° to 70°C	0° to 70°C

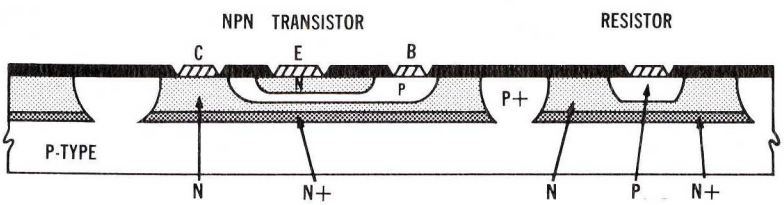
Typical circuit diagram for Series 1500/1580 NAND gate



This line of semiconductor integrated circuits provides a useful combination of speed, power dissipation, fan-out, and noise margin. Series 1500 is designed for operation over the full military temperature range of –55° to +125°C, and Series 1580 is appropriate for limited-temperature application (0° to +70°C) in industrial environments. The TO-84 ¼" by ⅛" flat pack, welded and hermetically sealed, is standard for both versions. An optional package for Series 1580 is TI's new 16-pin plug-in package featuring pins for 100-mil grid spacings.

The NAND/NOR gates can be cross-coupled to form an R-S flip-flop or can be connected in parallel to perform "Dot-OR" logic. The buffer has the ability to drive loads of large capacitance at high speeds because of its emitter-follower pull-up section which provides a low-impedance path during switching. The power gate, using the same circuit as the buffer minus the emitter-follower pull-up section, provides an open-collector output for use in high-fan-out, high-power-output applications.

The flip-flop is based on the "master-slave" concept. The master flip-flop stores information from its AND-gate inputs when the clock is in the high state, and transfers this information to the slave when the clock goes to the low state. The AND-gate inputs permit either R-S or J-K operation.

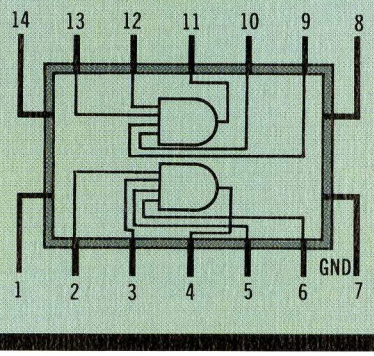


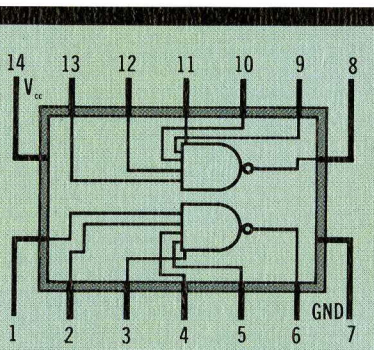
Planar diffused double-epitaxial structure for Series 1500/1580 networks

SN1500/SN1580

Dual 4-input Expander

Fan-out — (Max number of expanders connected to SN1501 or SN1581) — 4
Input capacitance — 2 pf





Dual 4-input Expandable NAND "Power" Gate

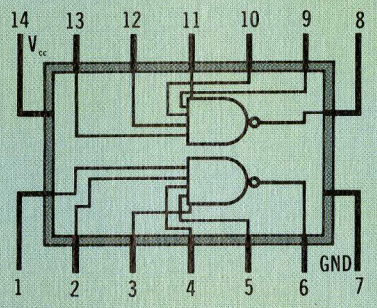
Propagation delay — 25 nsec
Fan-out — 20
Power diss. — 15 mw/gate

SN1504/SN1584

SN1501/SN1581

Dual 4-input Expandable NAND Gate

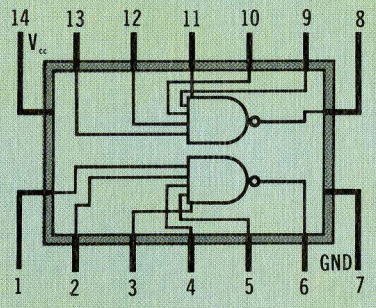
Propagation delay — 25 nsec
Fan-out — 8
Power diss.— 5 mw /gate



SN1502/SN1582

Dual 4-input Expandable Buffer

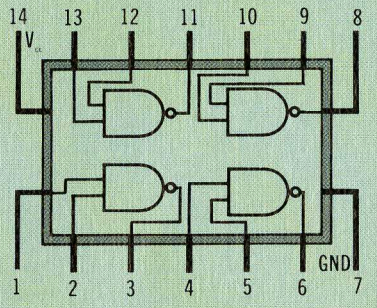
Propagation delay — 25 nsec
Fan-out — 20
Power diss.— 15 mw /gate

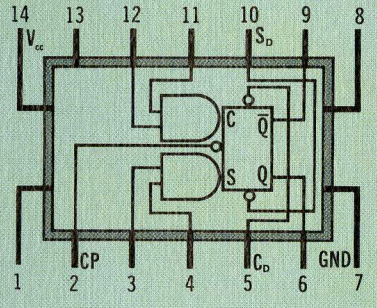


SN1503/SN1583

Quadruple 2-input NAND Gate

Propagation delay — 25 nsec
Fan-out — 8
Power diss.— 5 mw /gate

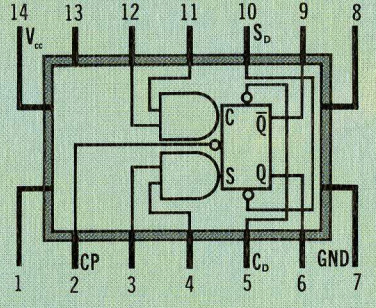




J-K/R-S Flip-flop

Propagation delay — 50 nsec
Fan-out — 7
Power dissipation — 20 mw

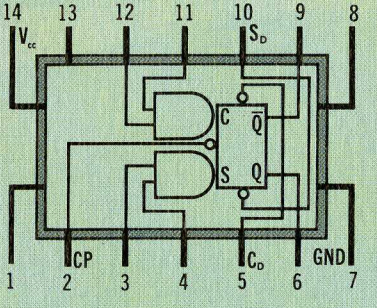
SN1510/SN1590



High-performance J-K/R-S Flip-flop

Propagation delay — 50 nsec
Fan-out — 10
Power dissipation — 30 mw

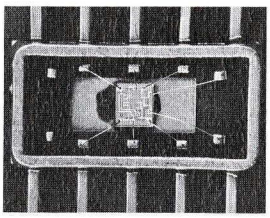
SN1511/SN1591



Fast-rise-time J-K/R-S Flip-flop

Propagation delay — 45 nsec
Fan-out — 9
Power dissipation — 35 mw

SN1513/SN1593



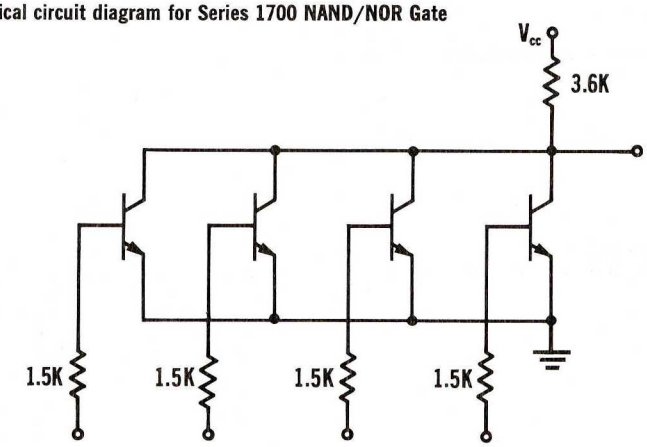
- Low power dissipation with moderate speed capability
- Simple RTL logic configuration
- Choice of TO-89 flat package or TO-78 (modified TO-5)

Series 1700 RTL Digital Integrated Circuits

TYPICAL CHARACTERISTICS

Parameter	Basic Gate	Register
Propagation delay	35 nsec	70 nsec
Power dissipation	4 mw	15 mw
D-c noise margin	150 mv	150 mv
Fan-out	4	3
Supply voltage	3 v	3 v
Temperature range	–55° to +125°C	–55° to +125°C

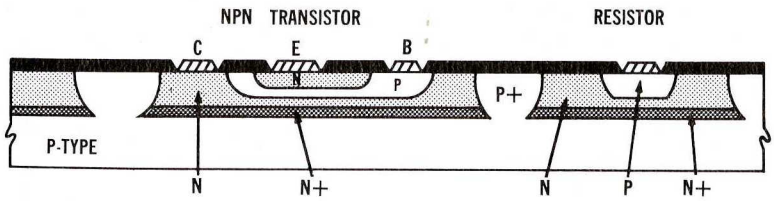
Typical circuit diagram for Series 1700 NAND/NOR Gate



This line of seven monolithic semiconductor integrated circuits combines low power dissipation with medium speed capabilities. The line is engineered and manufactured to the full-performance specifications of a sponsoring government agency. Compatibility is guaranteed through the full military temperature range of –55° to +125°C.

Choice of two packages. Equipment designers have a choice between the TO-89 flat package and a TO-78 (modified TO-5) package, with no price differential. The letter "A" after the type number designates units in TI flat packages. Type numbers without an alphabetical suffix indicate the 8-lead TO-78 package.

The register can be controlled either by a-c or d-c inputs. When the clocking input is high, control of the circuit is determined by d-c R and S inputs. For a-c operation, the register can be converted to a binary counter by simply connecting two leads externally.

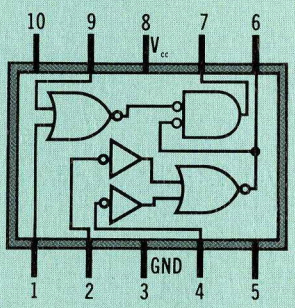


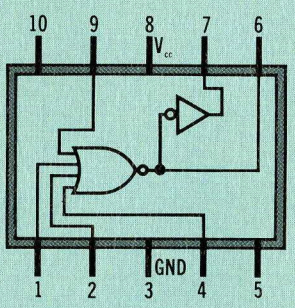
Planar diffused double-epitaxial structure used for Series 1700 networks

SN1729/SN1729A

Adder

Propagation delay — 70 or 105 nsec
Power dissipation — 10 mw
Fan-out — 3 or 4





4-input Gate

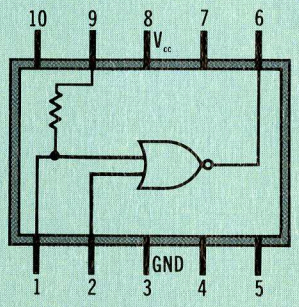
Propagation delay — 35 or 70 nsec
Power dissipation — 4 mw
Fan-out — 3 or 4

SN1733/SN1733A

SN1730/SN1730A

Buffer

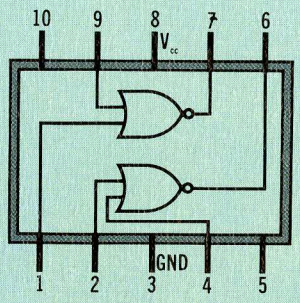
Propagation delay — 70 nsec
Power dissipation — 15 mw
Fan-out — 30



SN1731/SN1731A

Dual 2-input Gate

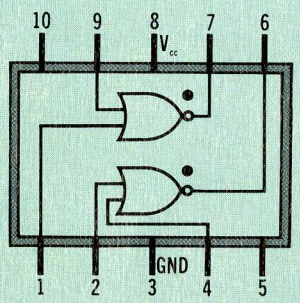
Propagation delay — 35 nsec
Power dissipation — 2.5 mw per gate
Fan-out — 4

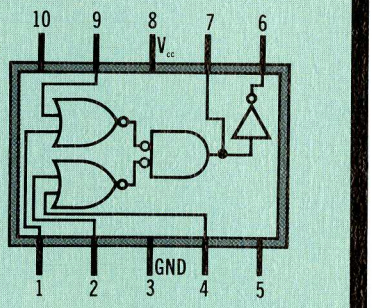


SN1732/SN1732A

Dual 2-input Expander Gate

Propagation delay — 35 nsec
Power dissipation — N/A
Fan-out — N/A

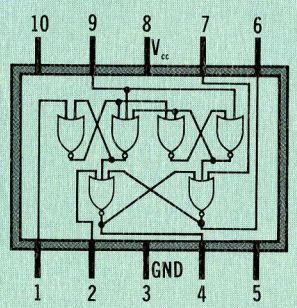




Half-adder

Propagation delay — 70 or 105 nsec
Power dissipation — 8 mw
Fan-out — 3 or 4

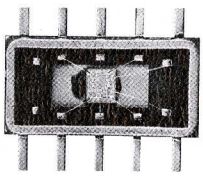
SN1734/SN1734A

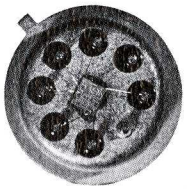


Register

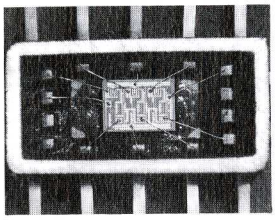
Propagation delay — 70 nsec
Power dissipation — 15 mw
Fan-out — 3

SN1735/SN1735A





RTL networks are available both in standard ¼" by ⅛" flat packages and in modified TO-5 cases.



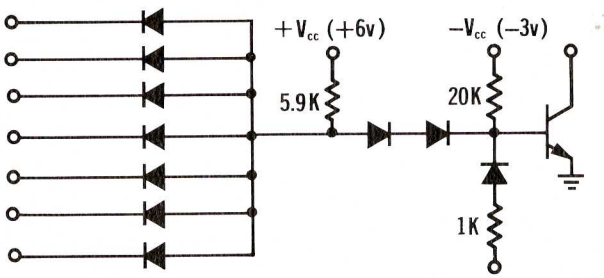
- Proved reliability in Minuteman II guidance and control-system applications
- Multiple circuit functions per package
- High noise immunity
- Linear and memory networks also available in Minuteman Series (page 24)
- Standard TO-84 welded flat package

Minuteman Series DTL Digital Integrated Circuits

TYPICAL CHARACTERISTICS

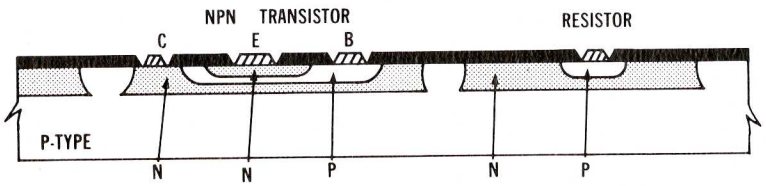
Parameters	Basic Gate	Flip-flop
Propagation delay	140 nsec	250 nsec
Power dissipation	20-40 mw	90 mw
Fan-out	12	12
D-c noise margin	500 mv	500 mv
Supply voltage	+6 v, —3 v	+6 v, —3 v
Temperature range	0° to +65°C	0° to +65°C

Circuit diagram for basic Minuteman Series NAND/NOR Gate

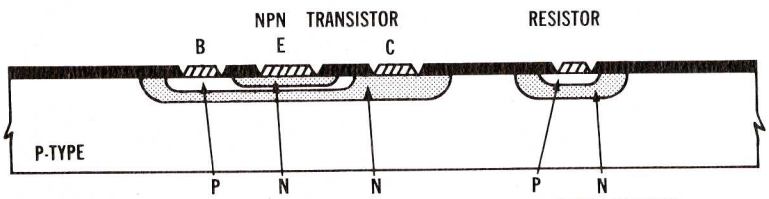


This compatible series of semiconductor integrated circuits was designed by Autonetics division of North American Aviation and TI. These digital units, along with linear units in the same series, perform more than 93 percent of the electronic functions in the guidance-computer section of the Minuteman II missile.

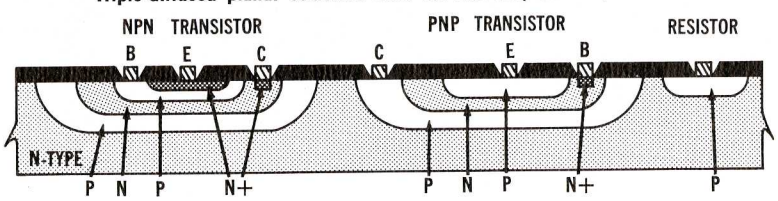
The NAND/NOR gates are conservatively designed for medium-speed operation with wide noise margins. A separate clock input is included in two of the gates — the SN341A and SN347A.



Diffused planar/epitaxial structure used for SN337A, SN344A



Triple-diffused planar structure used for SN341A, SN347A, SN359A



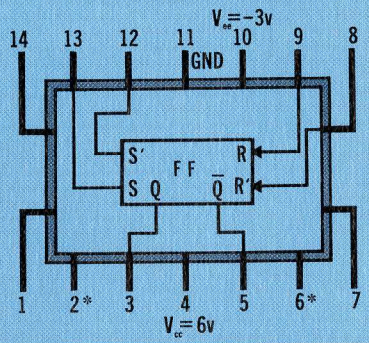
Quadruple-diffused planar structure used for SN343A, SN346A

SN337A

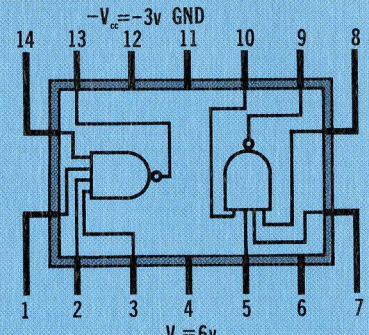
Flip-flop

Propagation delay — 250 nsec
Fan-out — 12
Power dissipation — 90 mw

*Connection of lead 2 to lead 3 and lead 5 to lead 6 provides collector pull-up resistors for the Q and $\bar{Q}$ outputs.



SN359A



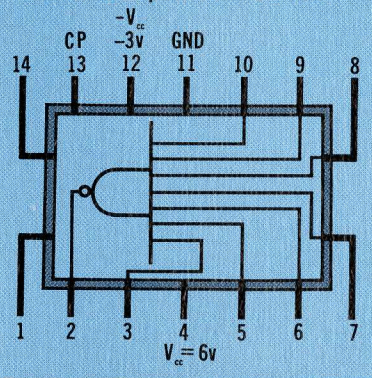
Dual 4-input, Low-level NAND/NOR Gate (Unclocked)

Propagation delay — 140 nsec
Fan-out — 6
Power dissipation — 22 mw per gate

SN341A

7-input NAND/NOR Gate (Clocked)

Propagation delay — 140 nsec
Fan-out — 6
Power dissipation — 12 mw

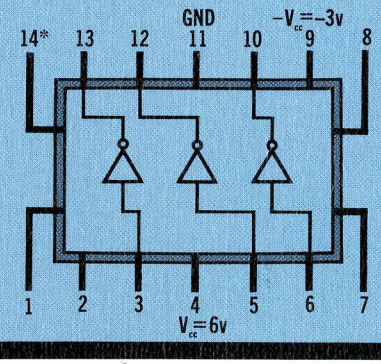


SN344A

Triple High-level Inverter

Propagation delay — 120 nsec
Fan-out — 12
Power diss. — 85 mw/inverter

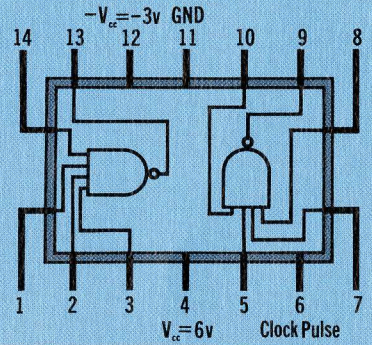
*Connection of lead 13 to lead 14 provides a collector pull-up resistor. Two other inverters have this collector resistor internally connected.

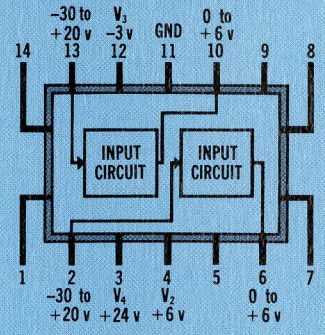


SN347A

Dual 4-input, Low-level NAND/NOR Gate (Clocked)

Propagation delay — 140 nsec
Fan-out — 6
Power dissipation — 22 mw per gate



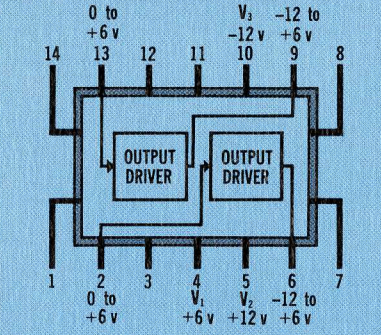


An inverting interface circuit that translates a large input voltage swing to a digital logic level.

Dual Input Network

Propagation delay — 500 nsec
Fan-out — 13
Power diss — 25 mw /circuit

SN343A

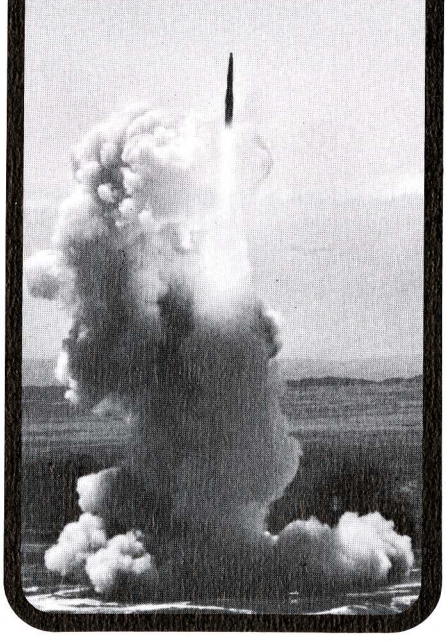


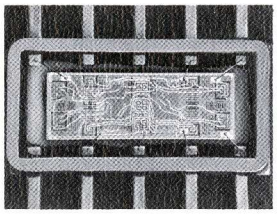
A non-inverting interface circuit that translates a digital logic level into a large output voltage swing.

Dual Output Driver

Propagation delay — 850 nsec
Fan-out — 11
Power diss — 160 mw /driver

SN346A





- High-performance operational amplifiers
- Very low input and output offset characteristics
- High common-mode input capability
- Excellent temperature drift characteristics
- Master slice flexibility
- Standard TO-84 and TO-89 welded flat package

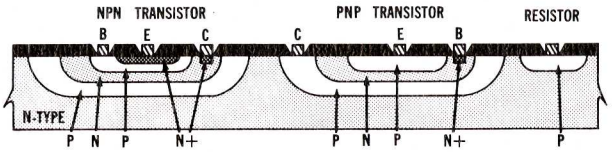
Series 52 Operational / Differential Amplifiers

The Series 52 family of six operational/differential amplifiers is fabricated in monolithic semiconductor structures. These general-purpose circuits find wide application in military and industrial control systems, analog-to-digital converters, and analog computers.

The circuit design of Series 52 permits a vast number of different linear circuit functions to be achieved by the addition of simple feedback networks. The very high gain and stable temperature characteristics greatly simplify circuit design and device interchangeability. Although characterized using supply voltages of ±12 volts, they can be used with single-polarity supplies and with supplies as low as ±3 volts. They have very high common-mode rejection and common-mode input-voltage capability, making them particularly suitable for voltage comparators, integrators, and low-gain buffers.

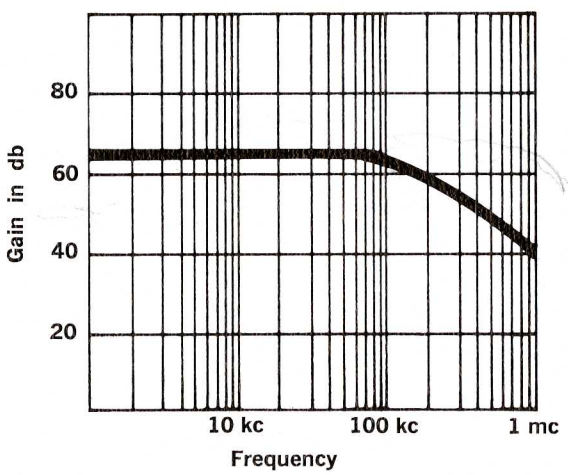
Master Slice Capability. Master slice variations from the standard amplifiers can be obtained quickly and economically simply by changing the metal interconnection pattern deposited on the face of the bar. This capability provides design flexibility for a wide variety of customized circuits. Two different bars are used for Series 52. The bar used for SN521A, SN522A, SN523A, and SN524A contains two pnp and eight npn transistors which can also be used as diodes.

The bar used for SN525A and SN526A features 10 npn and four pnp transistors. There are also 68 resistors totaling 300,000 ohms — making 82 component elements in all. Since the diffusion techniques create all transistors simultaneously in the single block of silicon material, transistor characteristics are closely matched over the full temperature range. Transistor pairs are closely spaced for improved differential-input voltage offsets and temperature-drift characteristics. Improved collector saturation resistance provides high output-current and high voltage capability.



Quadruple-diffused planar structure used for Series 52 networks

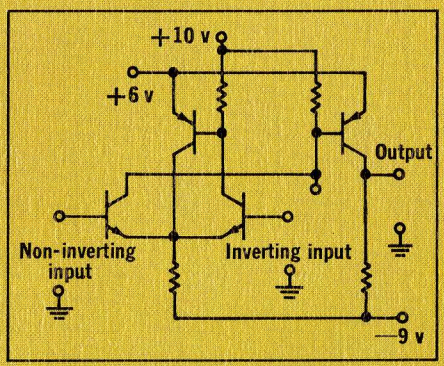
Typical response curve for Series 52 operational amplifiers



SN521A
Operational Amplifier

The SN521A, first announced in 1962, is an operational amplifier with inverting and non-inverting outputs. It features low power drain, typically 28 mw, and stable gain, ±1.5 db, over the full military temperature range. This network is useful in many applications such as summing amplifiers, integrators, differentiators, multivibrators, and buffer amplifiers.

TYPICAL CHARACTERISTICS	
Voltage gain	1200
Input impedance	12 k Ω
Output impedance	10 k Ω
D-c drift referred to input	8 μv/°C
Output signal swing	±4.7 v
Common-mode rejection	60 db
Temperature range	−55° to +125°C



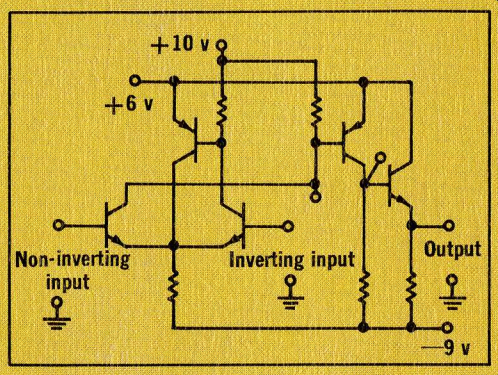
SN522A

Operational Amplifier with Emitter-follower Output

The SN522A is an operational amplifier similar to the SN521A, with the additional feature of an emitter-follower output for higher output current drive. Although this amplifier was originally designed to use three power supplies, stable operation is practical with two power supplies.

TYPICAL CHARACTERISTICS

Voltage gain	1200
Input impedance	12 k Ω
Output impedance	160 Ω
D-c drift referred to input	8 μv/°C
Output signal swing	±3.7 v
Common-mode rejection	60 db
Temperature range	−55° to +125°C



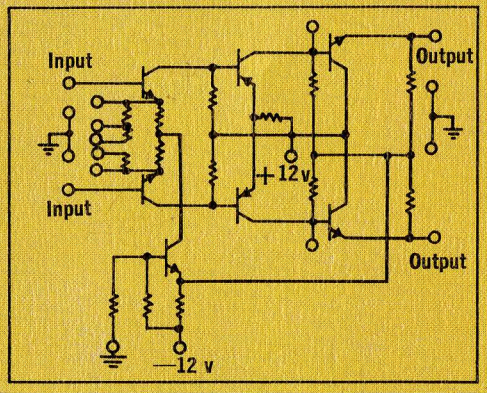
SN523A

General-purpose Differential Amplifier

The SN523A features both differential inputs and differential emitter-follower outputs, providing considerable design flexibility. The amplifier is designed with a resistance network in the emitters of the input stage, allowing gain to be adjusted over a wide range (40 to 70 db) simply by shorting various lead combinations. Frequency response is typically dc to 150 kc.

TYPICAL CHARACTERISTICS

Voltage gain (differential)	2500
Input impedance	10 k Ω
Input offset voltage	2 mv
D-c drift referred to input	5 μv/°C
Output signal swing, single-ended	±6.5 v
Common-mode rejection	90 db
Temperature range	−55° to +125°C



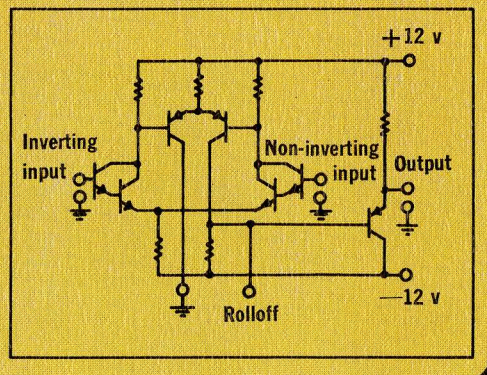
SN524A

General-purpose Operational Amplifier

The SN524A features an unusually high input impedance, resulting from the Darlington-type connection of the input transistors. It has a large dynamic output range providing an input common-mode voltage range of ±5 volts, which permits a high degree of flexibility in circuit design. Both SN523A and SN524A networks operate from ±12-volt power supplies.

TYPICAL CHARACTERISTICS

Voltage gain	1200
Input impedance	1 megohm
Input offset voltage	12 mv
D-c drift referred to input	20 μv/°C
Output signal swing, single ended	±7.5 v
Common-mode rejection	55 db
Temperature range	−55° to +125°C



(Series 52 continued on next page)

(Series 52 continued)

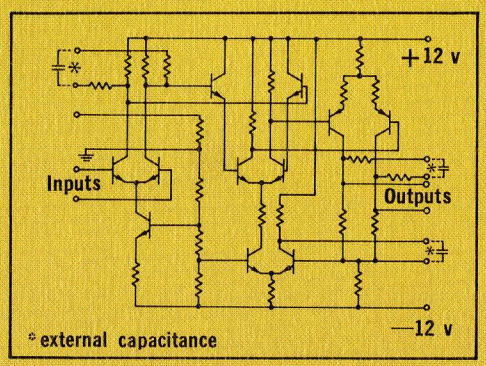
SN525A

High-performance Differential Amplifier

The SN525A is a high-performance amplifier featuring an open-loop gain of 88 db, yet it is unconditionally stable when used with two external capacitors in the frequency-response-shaping circuit. A feedback loop provides high common-mode rejection. Both differential input and output terminals are available.

TYPICAL CHARACTERISTICS

Voltage gain (differential)	50,000
Input impedance	100 k Ω
Input offset voltage	1 mv
D-c drift referred to input	5 μv/°C
Output signal swing, single-ended	±9 v
Common-mode rejection	100 db
Temperature range	−55° to +125°C



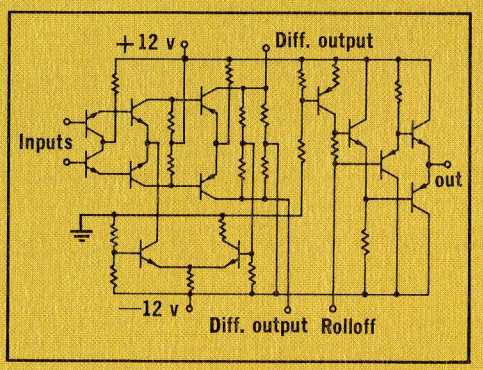
SN526A

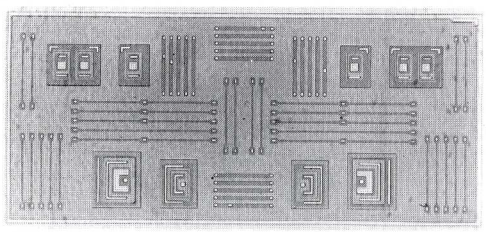
High-performance Operational Amplifier

The SN526A incorporates a class-B output stage formed by a complementary pair of npn and pnp transistors. The circuit is capable of a 10-volt signal swing with a 600-ohm load. Output-current peak is 10 ma. Transistor pairs are close together, providing a maximum differential input offset of 6 mv over the temperature range.

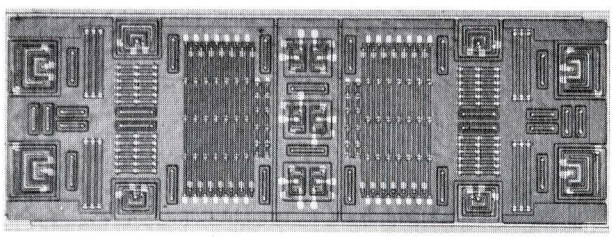
TYPICAL CHARACTERISTICS

Voltage gain	1200
Input impedance	2 megohm
Input offset voltage	3 mv
D-c drift referred to input	15 μv/°C
Output signal swing, single-ended	±6 v (R_L = 600 Ω)
Common-mode rejection	80 db
Temperature range	−55° to +125°C

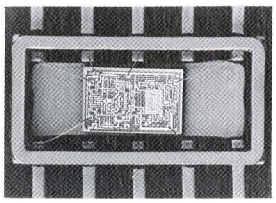




Master Slice bar used for SN521A, SN522A, SN523A, SN524A



Master Slice bar used for SN525A and SN526A



- High-frequency linear integrated circuits
- High level of complexity — up to seven stages per bar
- Master Slice flexibility
- Very low distributed capacitance
- Transistor f_T of over 1Gc.
- Standard TO-89 welded flat package

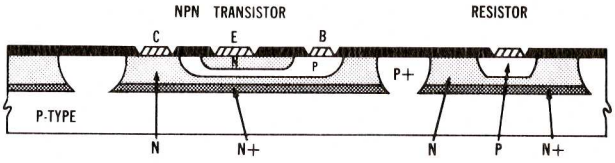
Series 55 High-frequency Amplifiers

This line of linear integrated circuits consists of the SN5500 magnetic-core sense amplifier and the SN5510 video differential amplifier. Featuring excellent high-frequency performance, low power dissipation, and low over-all cost, Series 55 circuits have wide applications as sense amplifiers, level detectors, IF amplifiers, and video amplifiers.

Series 55 amplifiers use transistors with f_T as high as 1.2 Gc under low-current and low-V_{ce} conditions. Circuit frequency response from dc to 300 mc is possible. The series 55 units can be operated with power-supply voltages of up to ±6 volts.

The large number of elements on the two Master Slice bars makes possible the fabrication of very complex circuits. Customized variations can be built economically simply by changing the metallic interconnection patterns. The SN5510 Master Slice bar has available 12 npn transistors and 70,000 ohms of resistance. The SN5500 Master Slice bar includes 23 npn transistors, 104,000 ohms of resistance, and diffused capacitance of 100 picofarads.

Standard package for all Series 55 networks is the ¼" by ⅛" TO-89 flat pack with 10 lateral leads. All external surfaces of the metal package are gold-plated. The lid is stitch-welded with 200 welds around the perimeter, hermetically sealing the package.



Planar diffused double-epitaxial structure used for Series 55 networks

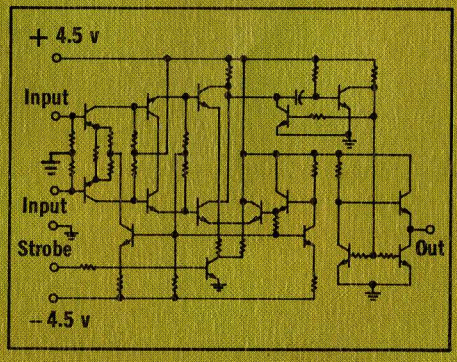
SN5500

Magnetic-core Sense Amplifier

The SN5500 is a complete sense amplifier, including strobe gate and pulse-shaping output circuits. It detects bi-polar differential input signals from a magnetic-core memory and provides a one-shot output interface between the memory and logic circuitry. It can be used for other applications requiring signal-level detection with an extremely sharp threshold.

TYPICAL CHARACTERISTICS

Input threshold voltage level	17 mv
"Off" output level	3.2 v
"On" output level	0.3 v
Common-mode rejection	2 v
Propagation delay	70 nsec
Temperature range	−55° to +125°C



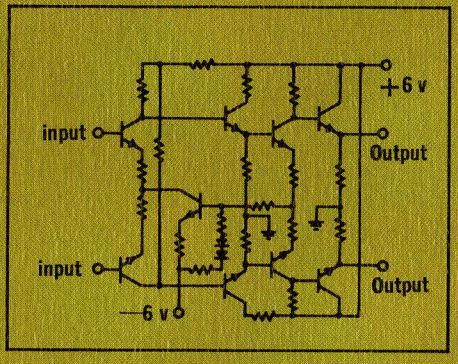
SN5510

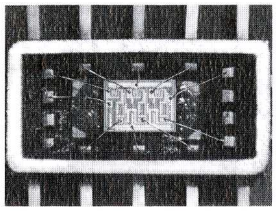
Video Differential Amplifier

The SN5510 video amplifier features flat frequency response and low phase-shift from dc to 40 mc. Differential inputs are provided which can be direct-coupled to ground. The differential outputs permit the unit to be used as a high-frequency differential amplifier or as an operational amplifier. Typical output impedance is less than 35 ohms.

TYPICAL CHARACTERISTICS

Voltage gain, open-loop, single-ended	40 db
Linear output, single-ended	4 v_{p-p}
Bandwidth, 3 db	40 mc
Common-mode rejection	60 db
Input impedance	3.5 k Ω
Temperature range	−55° to +125°C





- Proved in Minuteman II guidance system
- High reliability
- Wide range of circuits
- Digital networks also available in Minuteman Series (page 18)
- Applications include computer and control circuitry
- Standard TO-84 welded flat package

Minuteman Series Linear / Memory Integrated

TI's Minuteman Series was designed to minimize the variety of circuits required to fulfill the requirements of guidance and control systems. For example, the gates, switches, general-purpose amplifiers, and demodulator choppers are used in several different applications in the Minuteman II missile.

The circuits were designed by NAA's Autonetics Division and translated into integrated form by TI. These designs were so successful that integrated circuits perform more than 93.6 per cent of the electronic functions required in the computer portion of the missile.

This new Autonetics computer — which replaces a Minuteman system that set an industry standard for reliability — has two-and-one-half times the operational capacity of its predecessor . . . yet is about half its weight and size, uses less than 50 per cent as many parts, and operates on about 60 per cent of the power.

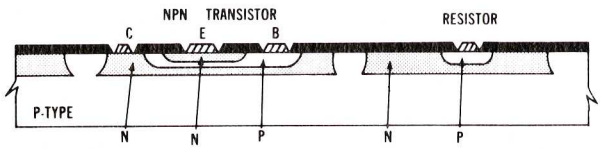
The complete Minuteman series is functionally compatible in the design of computer and control circuitry.

The operational amplifiers have double-ended outputs, small offset voltages, and large common-mode rejection ratios. These linear networks feature gains as high as 3000 with a 200-kc minimum cut-off frequency and 20-volt peak-to-peak differential output-signal swing.

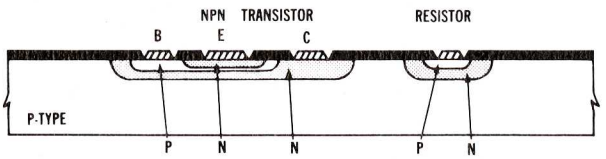
Minuteman Series memory networks include the SN340A low-level switch, the SN342A read preamplifier and the SN348A matrix switch. Information regarding these circuits is included on page 26.

Standard Package for all Minuteman Series networks is the TO-84 ¼" by ⅛" welded and hermetically sealed flat pack.

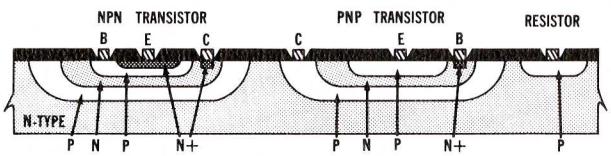
Operating temperature range for Minuteman Series networks is 0° to +65°C.



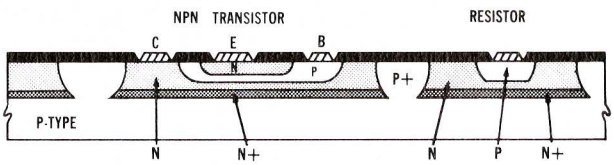
Diffused planar/epitaxial structure used for SN355A



Triple-diffused planar structure used for SN348A, SN350A, SN352A



Quadruple-diffused planar structure used for SN342A, SN354A



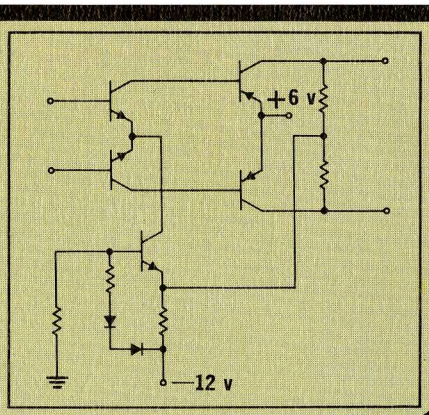
Diffused planar, double-epitaxial structure used for SN340A

SN350A

General-purpose Amplifier

This general-purpose amplifier offers differential inputs and outputs, low offset voltages, and high common-mode rejection ratios.

TYPICAL CHARACTERISTICS	
Differential d-c input offset	5 mv
A-c voltage gain	220
A-c signal swing	22 v_{P-P}
Upper cut-off frequency	220 kc
Input impedance	50 k Ω
Common-mode rejection	90 db



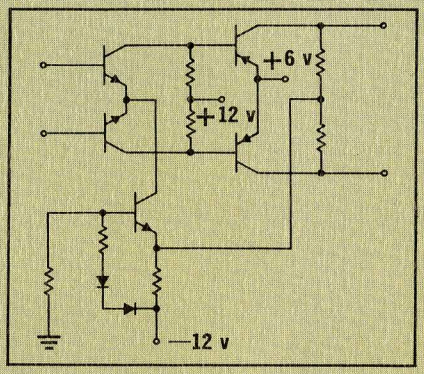
Circuits

SN352A
General-purpose Amplifier

The SN352A offers both differential inputs and outputs, plus a high voltage gain of 2000 minimum and an 80-db common-mode rejection ratio.

TYPICAL CHARACTERISTICS

Differential d-c input offset	8 mv
A-c voltage gain	6000
A-c signal swing	22 v_{p-p}
Upper cut-off frequency	220 kc
Input impedance	6 k Ω
Common-mode rejection	90 db

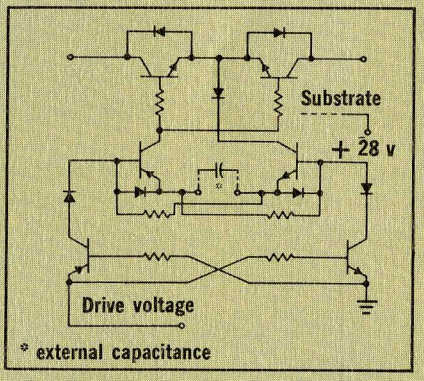


SN354A
Demodulator Chopper

The SN354A enables a d-c or low-frequency a-c signal to modulate a higher-frequency a-c signal — the drive voltage — producing a modulated a-c signal.

TYPICAL CHARACTERISTICS

Voltage offset, d-c component	4.6 mv
"On" condition low-current voltage drop	45 mv
"On" condition high-current voltage drop	950 mv
Output leakage current	40 μa
Static leakage current	1 μa
"On" condition leakage current	5 μa

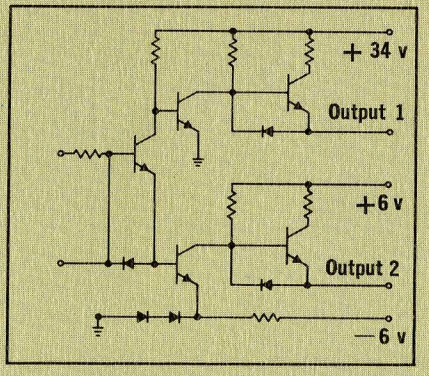


SN355A
Driver Switch

The SN355A performs as a power amplifier, separating the input signal into two output signals which are 180 degrees out of phase.

TYPICAL CHARACTERISTICS

D-c input resistance	11 k Ω
Output voltage No. 1	26.4 v
Output voltage No. 2	1.92 v
Output current	7.6 ma
Output leakage current	100 μa



(Minuteman Series memory networks on next page)

Minuteman Series Memory Integrated Circuits

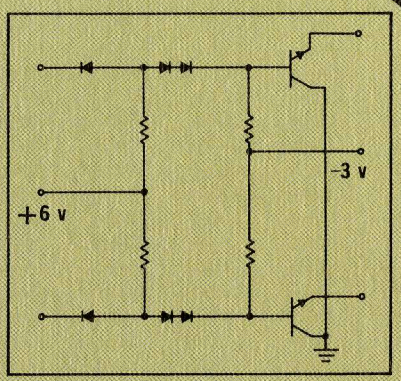
SN340A

Low-level Switch

This is a dual switching device utilizing diode inputs coupled to common-collector npn output transistors. An input level of plus 3.0 vdc causes the corresponding output to be in the conducting or "true" state; an input level of 0.35 vdc causes the corresponding output to be in the non-conducting or "false" state.

TYPICAL CHARACTERISTICS

Output breakdown voltage	2 v
Input breakdown voltage	7 v
Output current	1 ma
"True state" input leakage current	10 μa
"True state" output voltage	5 mv
A-c output impedance	20 Ω



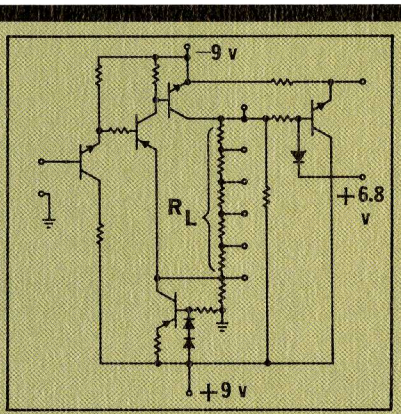
SN342A

Read Preamplifier

The SN342A is a voltage amplifier whose nominal gain can be varied by externally altering the value of an internal resistor with six taps.

TYPICAL CHARACTERISTICS

Input breakdown voltage	9 v
Output breakdown voltage	9 v
A-c input impedance	20 k Ω
A-c voltage gain	27 (R_L = max.)
Phase shift	0.35 μsec
A-c output impedance	180 Ω



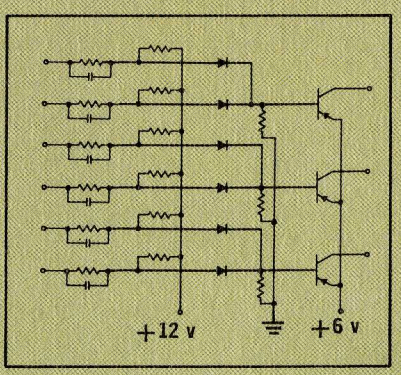
SN348A

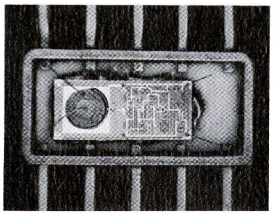
Matrix Switch

This is a matrix switch for application in digital computer systems, data-handling systems and control systems. It performs as a triple 2-input NOR gate, with differing logic levels on inputs and outputs.

TYPICAL CHARACTERISTICS

Output breakdown voltage	15 v
Output current	10 ma
Input current	1.9 ma
"True state" output voltage	5.6 v
Switching response, t_{on}	0.45 μsec
Switching response, t_{off}	0.45 μsec





SNX1304

Special Integrated-circuit Amplifiers

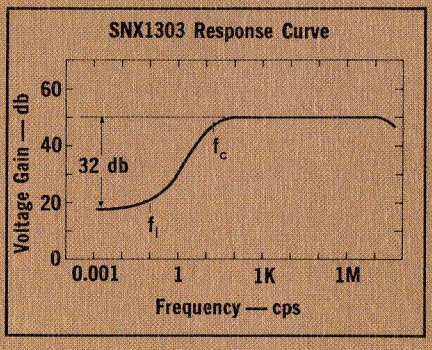
SNX1303

Thermal-feedback Video Amplifier

The SNX1303 consists of a thermal-feedback element and video differential amplifier. The video element uses direct-coupled stages in the signal path. The thermal feedback element acts as a regulator at low frequencies to maintain average output voltage constant and independent of d-c input or drift. Packaged in two TO-89 flat packs.

TYPICAL CHARACTERISTICS

Frequency response	50 cps to 10 mc
Voltage gain,	
Midband	48 db
D-c	16 db
Input signal before overloading,	
Midband	4 mv
D-c	150 mv
Dynamic output swing, no load	1.5 $v_{p\text{-}p}$



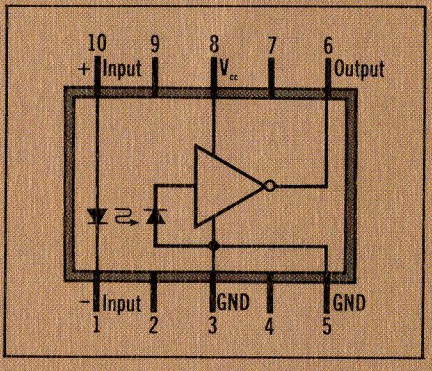
SNX1304

Optoelectronic Pulse Amplifier

The SNX1304 consists of a gallium-arsenide-junction light emitter that is optically coupled to an integrated silicon photodetector feedback-amplifier circuit. Applications include transmission of a-c or d-c signals across computer subsystem interfaces where circulating currents prevent interconnection of subsystem grounds. Package is 10-lead TO-89.

TYPICAL CHARACTERISTICS

Forward input threshold current	4 ma
Forward input voltage	1.2 v
"Off" output voltage	5 v
"On" output voltage	0.2 v
Rise time	250 nsec
Fall time	350 nsec



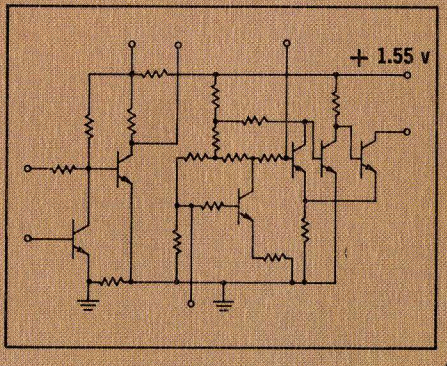
SN777

Low-level Audio Amplifier

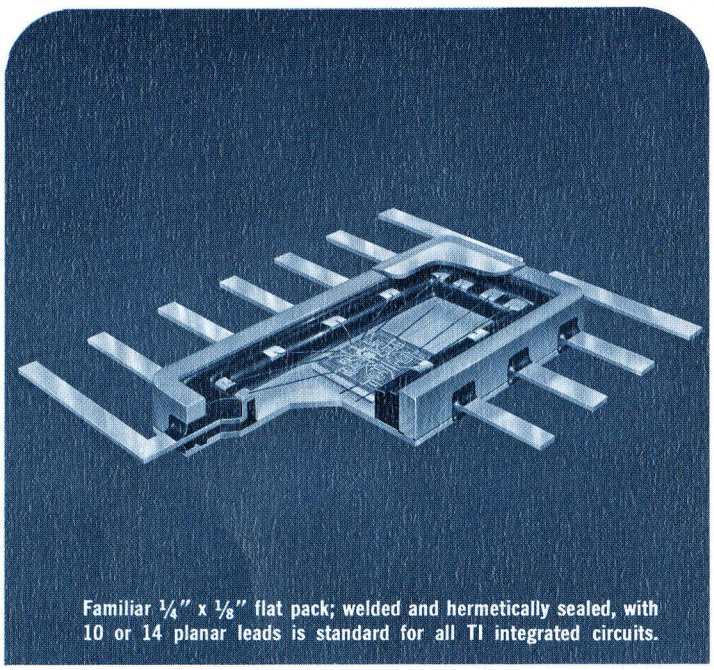
The SN777 is a low-level audio amplifier suitable for industrial and commercial applications. Examples are as a hearing-aid amplifier or as a microphone preamplifier. It is designed to operate from a supply voltage as low as 1.5 volts, greatly facilitating miniature-equipment design. Package is 10-lead TO-89.

TYPICAL CHARACTERISTICS

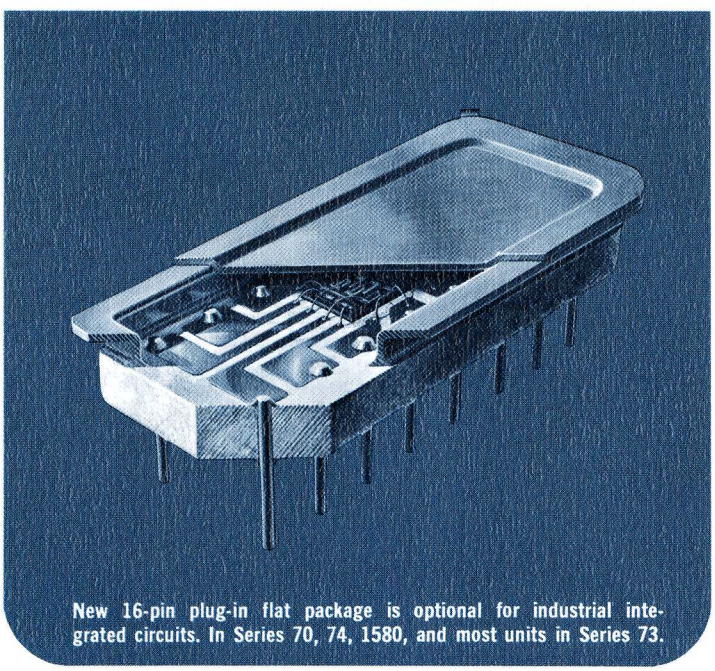
Frequency response (3db from 1 KC ref),	
Lower cut-off	20 cps
Upper cut-off	10 kc
Voltage gain at min volume attenuation	72 db
A-c signal swing across load,	
800 Ω a-c, 100 Ω d-c	±2.5 v
Power out	0.75 mw
Total harmonic distortion, 1 kc	2.1%



Integrated-circuit Packaging



Familiar ¼" x ⅛" flat pack; welded and hermetically sealed, with 10 or 14 planar leads is standard for all TI integrated circuits.



New 16-pin plug-in flat package is optional for industrial integrated circuits. In Series 70, 74, 1580, and most units in Series 73.

All TI networks are available in the standard 10-lead (TO-89) or 14-lead (TO-84) "flat-pack." The thin, rectangular configuration and lateral leads make this package suitable either for high-density equipment where size and weight are important or for mounted circuit-card assemblies where manufacturing cost and maintainability are major considerations.

The package — proved in field use over a five-year period — is all-welded construction, with a hermetic glass-to-metal seal. Leads are gold-plated F-15* alloy. The center-to-center lead spacing of 0.050 inches is a standard multiple of circuit-board interconnection spacings.

All external surfaces are metallic and are electrically insulated from leads and circuit. If requested, an insulator will be affixed to the bottom of the package. Thermal resistance (junction-to-case) of the package is 0.146°C per milliwatt (constant case temperature).

Other package configurations are available if required for your applications. These include the modified TO-5 type package with eight leads (TO-78) and ten leads, and TI's new 16-pin plug-in flat package.

Mech-Pak carrier. For your convenience, TI semiconductor networks are available in the Mech-Pak carrier — at no additional charge. This exclusive plastic carrier simplifies handling and reduces costs of incoming inspection, testing, breadboarding, storage, and assembly. The carrier is particularly appropriate for mechanized assembly operations, and will withstand temperatures of 125°C for extended periods.

Insulators. Where printed-circuit conductors pass under the package, insulators are available to prevent the metallic base of the package from shorting the conductors. Semiconductor networks can be ordered with high-temperature insulators permanently attached to the bottom of the package, at no additional charge. The insulator is 0.265 inches long, 0.140 inches wide and 0.0025 inches thick.

Formed leads. For mounting convenience, semiconductor networks can be ordered with formed leads, as shown at the right. If formed leads are not specifically ordered, units will be shipped with straight leads.

New Plug-in Package. A new family of integrated-circuit packages features plug-in pins on a 100-mil grid spacing, and is designed for high-volume industrial applications.

The modular family of plug-in flat packs includes units with 10, 16, 24, and 40 pins. The larger packages are designed to accommodate the more complex logic arrays that will be seen in coming months. First available is the 16-pin package, useful for today's multi-function logic networks of up to six circuits. The package has two rows of sturdy pins out the bottom, with the rows spaced 200 mils apart. The ceramic-to-metal, hermetically sealed version has dimensions of 390 by 890 mils. A lower-cost version in the same configuration, using other materials, will be available in the near future. A flange tab is provided as a means of indexing.

The new packages are adaptable to low-cost assembly techniques, including high-volume manual or automatic insertion,

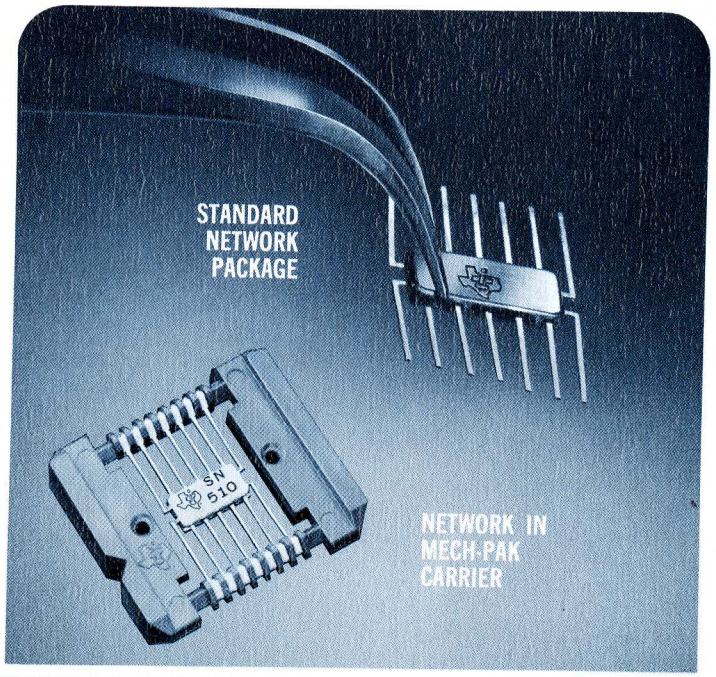
flow and wave soldering, and the use of less-expensive circuit boards with 100-mil grid spacings.

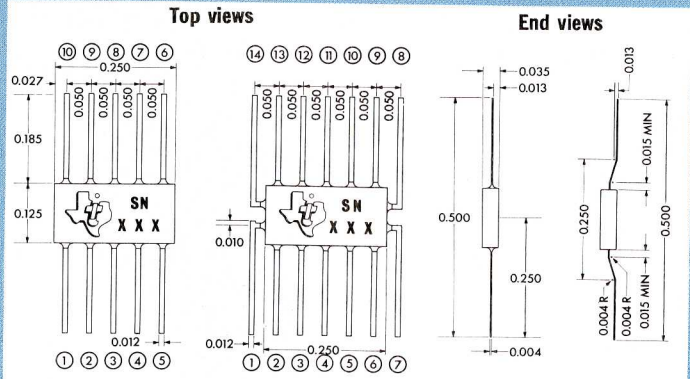
Ordering instructions. For detailed electrical and mechanical specifications, see data sheets. Semiconductor networks may be ordered with Mech-Pak carrier, formed leads, insulators, or any combination thereof. Simply select the appropriate ordering suffix from the table below and place it after the standard part number.

Example: To order SN510A with Mech-Pak carrier, formed leads and insulator, the network would be ordered as SN510A-5.

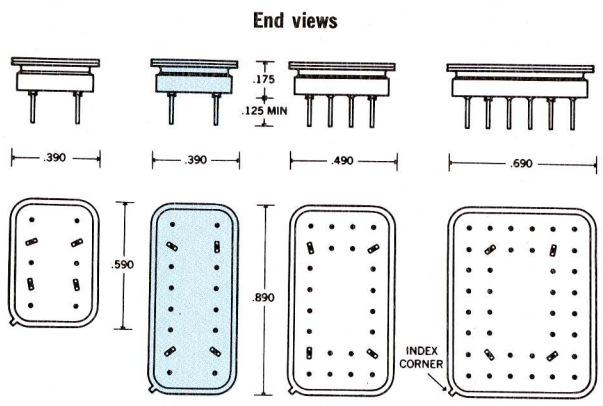
	Standard (No Mech-Pak Carrier)				Mech-Pak Carrier				Plug-in Package
Lead length	0.185 inch				Not Applicable				(Series 70, 73,‡74,1580 only)
Formed leads	No	No	Yes	Yes	No	No	Yes	Yes	
Insulators	No	Yes	No	Yes	No	Yes	No	Yes	
Ordering Suffix	None (Standard)	–6	–7	–1	–2	–3	–4	–5	P

**F-15 is the ASTM designation for a glass-sealing alloy containing nominally 29% nickel, 17% cobalt, and 53% iron.*





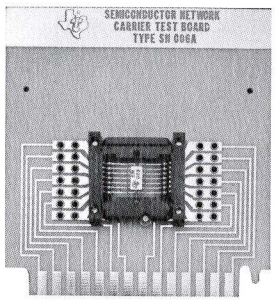
†10-lead networks in Series 51 and Series 53 use a different pin-numbering sequence. Refer to individual logic diagrams for position of lead #1.



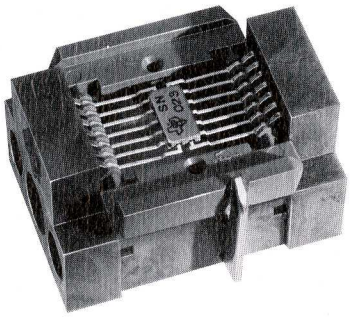
Family of industrial plug-in packages. 16-pin package now available.

‡For Series 73P, only the following networks are available as catalog products: SN7301, SN7302, SN7304, SN7311, SN7331, SN7350, SN7360, SN7370, SN7380.

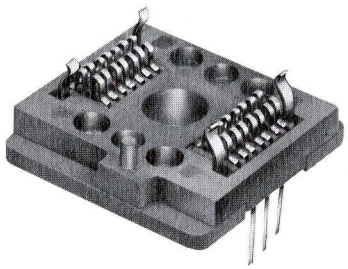
Accessory Equipment



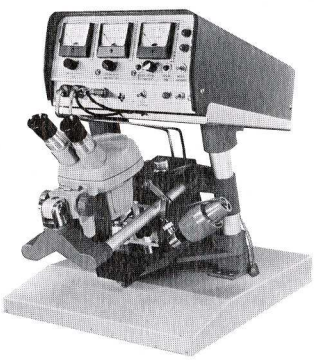
Test Board. SN006A is for incoming inspection and engineering breadboarding of networks in Mech-Pak carrier. Designed for extended use at 125°C. Uses Amphenol No. 143-015-01 printed-circuit connector or equivalent.



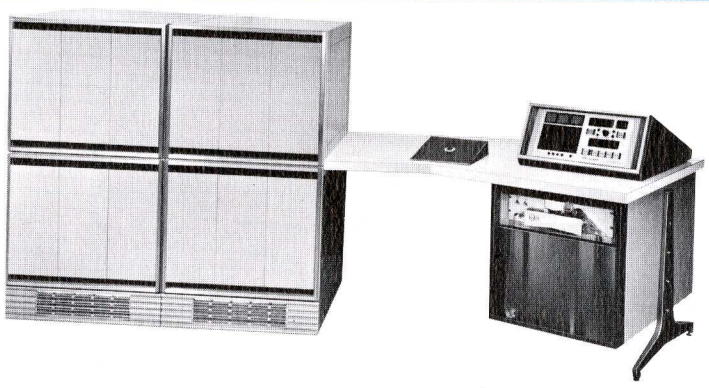
Test Socket. SN008 is designed for inspection and engineering breadboarding of networks in Mech-Pak carrier. Also, it is a convenient test fixture. Designed for extended use at 125°C.



Mech-Pak Connector. Spring-loaded connector permits plug-in operation of networks in Mech-Pak carrier. Suitable for testing, breadboarding, and production packaging. Contacts are gold-plated beryllium copper.



Parallel-gap Welder. New dynamically controlled welder is designed to weld ribbon leads of semiconductor networks to selected printed-circuit materials . . . reducing cost and improving reliability of network-to-PC-board connections.



The 553 Dynamic Test System. Designed to meet the needs of incoming inspection, reliability assurance, final test and quality assurance for integrated circuits, logic molules, thin films, printed-circuit cards, and other complex circuit elements.
The 553 system provides the capability for testing circuit elements under conditions simulating actual operating conditions. Testing of a wide variety of circuit elements under simulated operations is speedy and economical. Conducting both dynamic and d-c tests is possible in one operation without changing test sockets.

Reliability

The tables summarize reliability information for semiconductor networks manufactured during 1964. Based on this information, the present failure-rate estimate is 0.016% per 1000 hours at 55°C. This figure is the 60% upper confidence level (UCL) for one failure out of more than 12 million equivalent hours accrued on 1964 production.

Several customer programs using TI networks under field operating conditions have reported reliability data totalling 9,643,000 circuit hours. With two failures reported, the field-data failure rate is 0.021% per 1000 hours. Another customer program, including 30,000 TI networks, reports a mean-time-to-failure of 11,200,000 hours or a failure rate of 0.009% per 1000 hours.

Continued environmental testing demonstrates the ability of all semiconductor networks produced to substantially exceed the military requirements of MIL-S-19500.

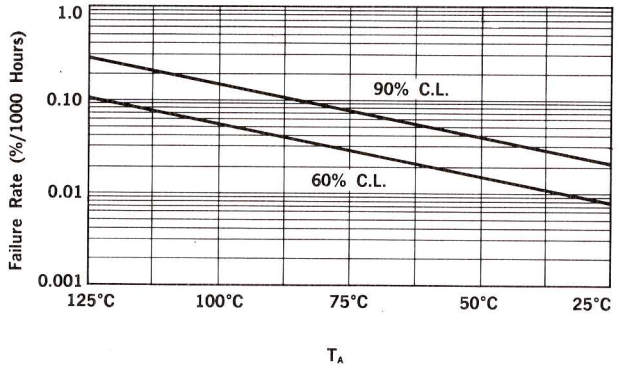
These data are only a small part of the total reliability information available. More than 33 million equivalent hours of circuit data have been accumulated on networks since early 1961. All reliability data is for networks mounted in the standard ¼" by ⅛" flat package.

In addition to reliability testing of the finished semiconductor networks, high reliability is assured by 100% processing of all semiconductor networks after final sealing through the following:

- **Temperature Cycle:**
  10 cycles minimum; +125° C to −55° C
- **High-temperature Bake:**
  48 hours minimum
- **Gross-leak Test:**
  Hot-liquid immersion
- **Helium Leak Test:**
  50 x 10^{-8} cc/sec maximum
- **Final 100% Electrical Test:**
  at temperature extremes
- **Centrifugal acceleration:**
  20,000 G in the Y_1 Plane

Summary of network reliability data accumulated during 1964.

Test Series	Stress Level	Number of Units on Test	Number of Failures	Longest Clock Hours	Actual Test Hours	Equivalent 55°C Test Hours
Weekly-add-to	125°C Operating	358	1	5000	632,000	4,300,000
Weekly-add-to	150°C Storage	200	0	2000	287,000	2,290,000
USAF Hi-Rel.	125°C Storage	48	0	5000	240,000	1,630,000
USAF Hi-Rel.	200°C Storage	44	0	5000	220,000	4,120,000
TOTALS		650	1		1,379,000	12,340,000



This chart enables you to determine a failure rate for the particular temperature and confidence level appropriate to your own applications.

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