Data Book

Programmable Logic

1988

TEXAS INSTRUMENTS

Programmable Logic

Data Book

1988

General Information 1

Data Sheets 2

Application Reports 3

Mechanical Data 4

The Programmable Logic Data Book

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INTRODUCTION

In this volume, Texas Instruments presents technical information on TI's broad line of programmable logic devices (PLDs), including 10-ns, 20-pin PAL® circuits.

TI's programmable logic products include high-speed leadership circuits, as well as standard 20- and 24-pin PAL devices in a variety of speed/power versions. This data book includes specifications on existing and future products, including:

- High-performance, low-power IMPACT™ and IMPACT-X™ 20- and 24-pin standard PAL circuits
- High-complexity Latched- and Registered-input PAL ICs and Exclusive-OR arrays
- Flexible, '22V10-architecture macrocell PAL ICs, including TI's enhanced, 20-ns version, the TIBPAL22VP10-20
- High-speed 6- and 3-ns, 10KH and 100K ECL IMPACT™ and ExCL™ PAL circuits
- Ultra-low-power UV-erasable and one-time programmable CMOS PAL ICs, including 20-pin, '22V10, and generic architectures
- Fast, 50-MHz programmable state machines, including enhanced versions of '82S105B/167B sequencers and the TIBPSG507 Programmable Sequence Generator

Texas Instruments high-speed programmable bipolar devices utilize TI's advanced IMPACT™ and new IMPACT-X™ technologies. IMPACT-X™ uses trench isolation and polysilicon emitters to increase performance and reduce power dissipation compared to traditional processes. IMPACT-X™ provides 1.5-μm feature sizes and 7-μm pitch.

Based on IMPACT-X™, TI's new ECL process, ExCL™, offers even greater speed and density for high-performance ECL circuits.

This volume contains design and specification data for 78 device types. Package dimensions are given in the Mechanical Data section in metric measurement (and parenthetically in inches).

Four programmable logic application reports have been incorporated into this data book as a reference tool. They are: *Designing with Texas Instruments Field Programmable Logic; Hard Array Logic; A Designer's Guide to the PSG507;* and *Systems Solutions for Static Column Decode.*

Complete technical data for any Texas Instruments semiconductor product is available from your nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at 1-800-232-3200.

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IMPACT and IMPACT-X are trademarks of Texas Instruments Incorporated.
ExCL is a trademark of Texas Instruments Incorporated.

General Information 1

Data Sheets 2

Application Reports 3

Mechanical Data 4

Contents

	Page
Alphanumeric Index	1-3
Glossary	1-5
Explanation of Function Tables	1-9
Parameter Measurement Information	1-11
Ordering Information	1-12
Hardware/Software Manufacturers	1-13
TI IMPACT™ Design and Service Centers	1-14

		Page
PAL16L8AC	PAL16L8AM	2-3
PAL16L8A-2C	PAL16L8A-2M	2-3
PAL16R4AC	PAL16R4AM	2-3
PAL16R4A-2C	PAL16R4A-2M	2-3
PAL16R6AC	PAL16R6AM	2-3
PAL16R6A-2C	PAL16R6A-2M	2-3
PAL16R8AC	PAL16R8AM	2-3
PAL16R8A-2C	PAL16R8A-2M	2-3
PAL20L8AC	PAL20L8AM	2-15
PAL20R4AC	PAL20R4AM	2-15
PAL20R6AC	PAL20R6AM	2-15
PAL20R8AC	PAL20R8AM	2-15
TIBPAD16N8-7C		2-27
TIBPAD18N8-6C		2-35
TIBPAL16L8-10C	TIBPAL16L8-12M	2-41
TIBPAL16L8-12C	TIBPAL16L8-15M	2-57
TIBPAL16L8-15C	TIBPAL16L8-20M	2-67
TIBPAL16L8-25C	TIBPAL16L8-30M	2-77
TIBPAL16R4-10C	TIBPAL16R4-12M	2-41
TIBPAL16R4-12C	TIBPAL16R4-15M	2-57
TIBPAL16R4-15C	TIBPAL16R4-20M	2-67
TIBPAL16R4-25C	TIBPAL16R4-30M	2-77
TIBPAL16R6-10C	TIBPAL16R6-12M	2-41
TIBPAL16R6-12C	TIBPAL16R6-15M	2-57
TIBPAL16R6-15C	TIBPAL16R6-20M	2-67
TIBPAL16R6-25C	TIBPAL16R6-30M	2-77
TIBPAL16R8-10C	TIBPAL16R8-12M	2-41
TIBPAL16R8-12C	TIBPAL16R8-15M	2-57
TIBPAL16R8-15C	TIBPAL16R8-20M	2-67
TIBPAL16R8-25C	TIBPAL16R8-30M	2-77
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TIBPAL20L8-25C	TIBPAL20L8-30M	2-101
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TIBPAL20X10-30C		2-127
TIBPAL22V10C	TIBPAL22V10M	2-145
TIBPAL22V10AC	TIBPAL22V10AM	2-145
TIBPAL22VP10-20C	TIBPAL22VP10-25M	2-157
TIBPALR19L8C	TIBPALR19L8M	2-169
TIBPALR19R4C	TIBPALR19R4M	2-169
TIBPALR19R6C	TIBPALR19R6M	2-169
TIBPALR19R8C	TIBPALR19R8M	2-169
TIBPALT19L8C	TIBPALT19L8M	2-181
TIBPALT19R4C	TIBPALT19R4M	2-181
TIBPALT19R6C	TIBPALT19R6M	2-181
TIBPALT19R8C	TIBPALT19R8M	2-181
TIBPLS506C	TIBPLS506M	2-193
TIBPSG507C	TIBPSG507M	2-201
TIB82S105BC	TIB82S105BM	2-209
TIB82S167BC	TIB82S167BM	2-219
TICHAL16L8-35C		2-229
TICHAL16R4-35C		2-229
TICHAL16R6-35C		2-229
TICHAL16R8-35C		2-229
TICPAL16L8-55C		2-243
TICPAL16R4-55C		2-243
TICPAL16R6-55C		2-243
TICPAL16R8-55C		2-243
TICPAL18V8-25C	TICPAL18V8-30M	2-257
TICPAL22V10C	TICPAL22V10M	2-271
TIEPAL10H16P8-3C		2-285
TIEPAL10H16P8-6C		2-291
TIEPAL10016P8-3C		2-297
TIEPAL10016P8-6C		2-303
TIFPLA839C	TIFPLA839M	2-309
TIFPLA840C	TIFPLA840M	2-309

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

PART 1 — GENERAL CONCEPTS AND CLASSIFICATIONS OF CIRCUIT COMPLEXITY

Chip-Enable Input

A control input that when active permits operation of the integrated circuit for input, internal transfer, manipulation, refreshing, and/or output of data and when inactive causes the integrated circuit to be in reduced-power standby mode.
NOTE: See "chip-select input."

Chip-Select Input

A gating input that when inactive prevents input or output of data to or from an integrated circuit.
NOTE: See "chip-enable input."

Field-Programmable Logic Array (FPLA)

A user-programmable integrated circuit whose basic logic structure consists of a programmable AND array and whose outputs feed a programmable OR array.

Gate Equivalent Circuit

A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

Large-Scale Integration (LSI)

A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether digital or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

Mask-Programmed Read-Only Memory

A read-only memory in which the data content of each cell is determined during manufacture by the use of a mask, the data content thereafter being unalterable.

Medium-Scale Integration (MSI)

A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

Memory Cell

The smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, and from which it can be retrieved.

Memory Integrated Circuit

An integrated circuit consisting of memory cells and usually including associated circuits such as those for address selection, amplifiers, etc.

Output-Enable Input

A gating input that when active permits the integrated circuit to output data and when inactive causes the integrated circuit output(s) to be at a high impedance (off).

Programmable Array Logic (PAL®)

A user-programmable integrated circuit which utilizes proven fuse link technology to implement logic functions. Implements sum of products logic by using a programmble AND array whose outputs feed a fixed OR array.

Programmable Read-Only Memory (PROM)

A read-only memory that after being manufactured can have the data content of each memory cell altered once only.

Random-Access Memory (RAM)

A memory that permits access to any of its address locations in any desired sequence with similar access time for each location.
NOTE: The term RAM, as commonly used, denotes a read/write memory.

Read/Write Memory

A memory in which each cell may be selected by applying appropriate electronic input signals and the stored data may be either (a) sensed at appropriate output terminals, or (b) changed in response to other similar electronic input signals.

Small-Scale Integration (SSI)

Integrated circuits of less complexity than medium-scale integration (MSI).

Typical (TYP)

A calculated value representative of the specified parameter at nominal operating conditions (V_{CC} = 5 V, T_A = 25°C), based on the measured value of devices processed, to emulate the process distribution.

Very-Large-Scale Integration (VLSI)

A concept whereby a complete system function is fabricated as a single microcircuit. In this context, a system, whether digital or linear, is considered to be one that contains 3000 or more gates or circuitry of similar complexity.

Volatile Memory

A memory the data content of which is lost when power is removed.

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PART 2 — OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} **Supply current**
The current into* the V_{CC} supply terminal of an integrated circuit.

I_{CCH} **Supply current, outputs high**
The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the high level.

I_{CCL} **Supply current, outputs low**
The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the low level.

I_{IH} **High-level input current**
The current into* an input when a high-level voltage is applied to that input.

I_{IL} **Low-level input current**
The current into* an input when a low-level voltage is applied to that input.

I_{OH} **High-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I_{OS} (I_O) **Short-circuit output current**
The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{OZH} **Off-state (high-impedance-state) output current (of a three-state output) with high-level voltage applied**
The current flowing into* an output having three-state capability with input conditions established that, according to the production specification, will establish the high-impedance state at the output and with a high-level voltage applied to the output.
NOTE: This parameter is measured with other input conditions established that would cause the output to be at a low level if it were enabled.

I_{OZL} **Off-state (high-impedance-state) output current (of a three-state output) with low-level voltage applied**
The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a low-level voltage applied to the output.
NOTE: This parameter is measured with other input conditions established that would cause the output to be at a high level if it were enabled.

*Current out of a terminal is given as a negative value.

V_{IH} **High-level input voltage**
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IK} **Input clamp voltage**
An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

V_{IL} **Low-level input voltage**
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} **High-level output voltage**
The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**
The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

t_a **Access time**
The time interval between the application of a specific input pulse and the availability of valid signals at an output.

t_{dis} **Disable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state. (t_{dis} = t_{PHZ} or t_{PLZ}).

t_{en} **Enable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low). (t_{en} = t_{PZH} or t_{PZL}).

t_h **Hold time**
The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.
NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

t_{pd} **Propagation delay time**
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. (t_{pd} = t_{PHL} or t_{PLH}).

t_{PHL} **Propagation delay time, high-to-low level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} **Disable time (of a three-state output) from high level**
The time interval between the specified reference points on the input and the output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} **Disable time (of a three-state output) from low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} **Enable time (of a three-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a three-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

t_{sr} **Sense recovery time**
The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.

t_{su} **Setup time**
The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w **Pulse duration (width)**
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets.

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
	=	value/level is reentered
X	=	irrelevant (any input, including transitions)
Z	=	off (high impedance) state of a 3-state output
a ... h	=	the level of steady-state inputs A through H respectively
Q_0	=	the level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
	=	one high-level pulse
	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each transition indicated by ↓ or ↑.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, or , the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

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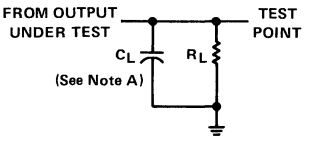
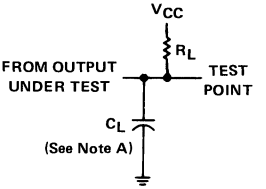
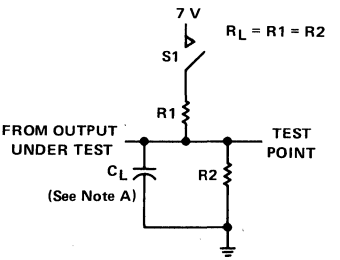
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS

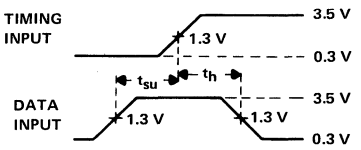


LOAD CIRCUIT FOR
OPEN-COLLECTOR OUTPUTS

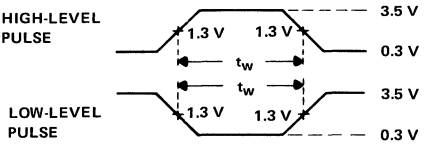


LOAD CIRCUIT FOR
THREE-STATE OUTPUTS

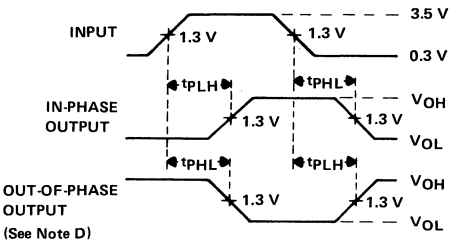
NOTE A: C_L includes probe and jig capacitance.



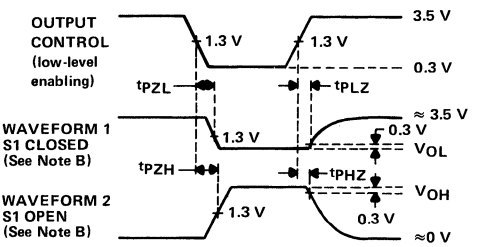
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE WIDTHS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

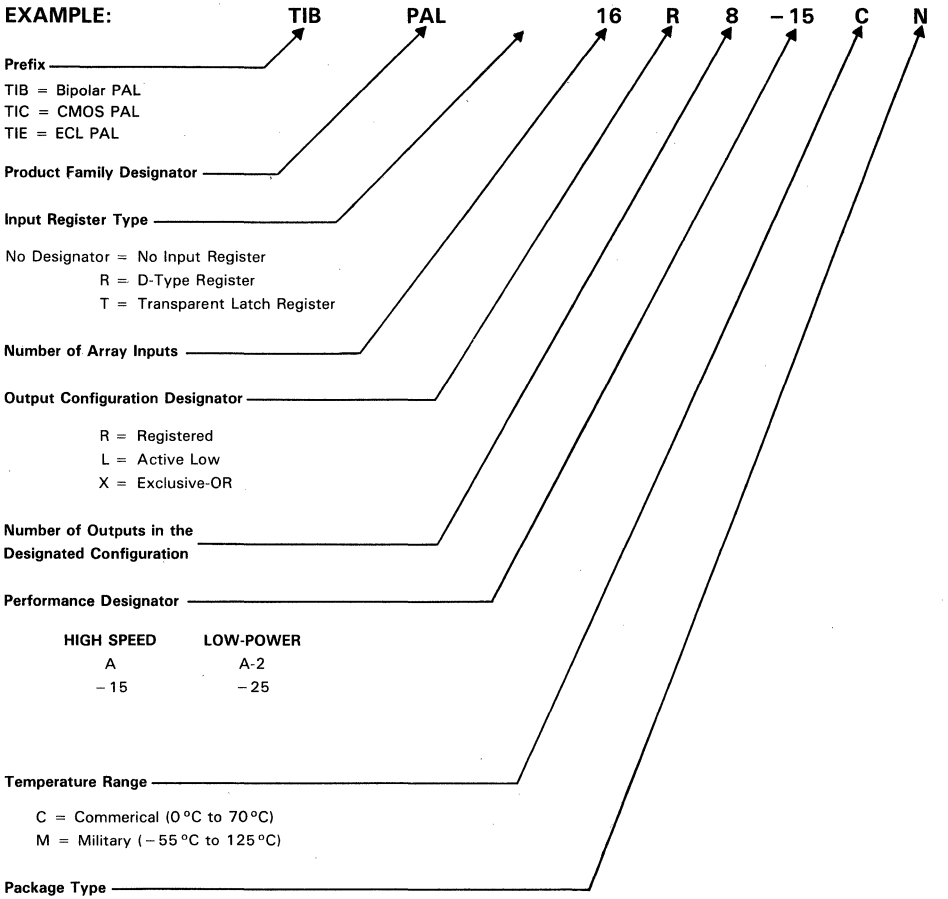


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

PAL® NUMBERING SYSTEM AND ORDERING INSTRUCTIONS

Factory orders for leadership PAL® circuits described in this catalog should include a nine-part type number as explained in the example below. Exclude the prefix when ordering standard PALs.



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ADDRESSES FOR PAL AND FPLA PROGRAMMING AND SOFTWARE MANUFACTURERS†

HARDWARE MANUFACTURERS

DATA I/O
10525 WILLOWS ROAD
REDMOND, WA 98073-9746
(800) 247-5700

DIGITAL MEDIA, INC
11770 WARNER AVE, UNIT 225
FOUNTAIN VALLEY, CA 92708
(714) 751-1373

STAG MICRO SYSTEMS
1600 WYATT DRIVE
SANTA CLARA, CA 95054
(800) 227-8836

SOFTWARE MANUFACTURERS

DATA I/O (ABEL)
10525 WILLOWS ROAD
REDMOND, WA 98073-9746
(800) 247-5700

PERSONAL CAD SYSTEMS (CUPL)
1290 PARKMOOR AVE
SAN JOSE, CA 95126
(408) 971-1300

†Texas Instruments does not endorse or warrant the suppliers referenced. Presently, Texas Instruments has certified DATA I/O, Sunrise, Structured Design and Digital Media. Other programmers are now in the certification process. For a current list of certified programmers, please contact your local TI sales representative.

TI *IMPACT*™ DESIGN AND SERVICE CENTERS

Design and programming assistance is offered by Texas Instruments IMPACT™ Design and Service Centers. The centers are equipped with the latest in software and hardware tools for design, debugging, prototyping, and production on a local basis. Supported by a professional engineering staff, the centers provide complete code development, device programming, symbolization, functional and DC parametric testing.

NORTHERN CALIFORNIA

MARSHALL IMPACT CENTER
336 LOS COCHES STREET
MILPITAS, CA 95035
(408) 942-4600

SOUTHERN CALIFORNIA

WYLE IMPACT CENTER
17872 COWAN AVENUE
IRVINE, CA 92714
(714) 863-9953

BOSTON

HALL-MARK IMPACT CENTER
6 COOK STREET, PINEHURST PARK
BILLERICA, MA 01821
(617) 935-9777

General Information 1

Data Sheets 2

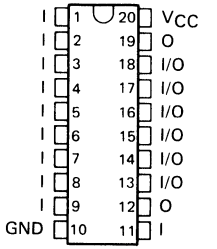
Application Reports 3

Mechanical Data 4

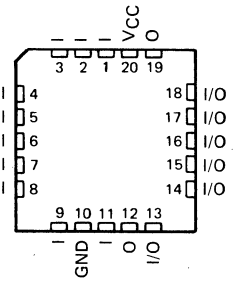
- **Standard High-Speed (25 ns) PAL Family**
- **Choice of Operating Speeds**
  HIGH SPEED, A Devices . . . 35 MHz
  HALF POWER, A-2 Devices . . . 18 MHz
- **Choice of Input/Output Configuration**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

DEVICE	INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state)	4
PAL16R6	8	0	6 (3-state)	2
PAL16R8	8	0	8 (3-state)	0

PAL16L8'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



PAL16L8'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



description

These programmable array logic devices feature high speed and a choice of either standard or half-power devices. They combine Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses. These devices will provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of "custom" functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

The Half-Power versions offer a choice of operating frequency, switching speeds, and power dissipation. In many cases, these Half-Power devices can result in significant power reduction from an overall system level.

The PAL16' M series is characterized for operation over the full military temperature range of −55°C to 125°C. The PAL16' C series is characterized for operation from 0°C to 70°C.

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

PAL is a registered trademark of Monolithic Memories Inc.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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PAL16R4'
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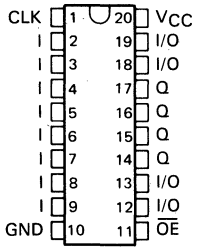
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



PAL16R4'
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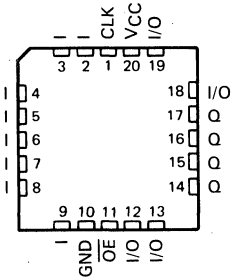
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



PAL16R6'
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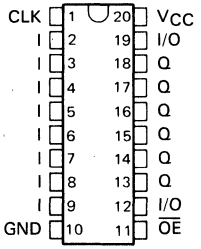
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



PAL16R6'
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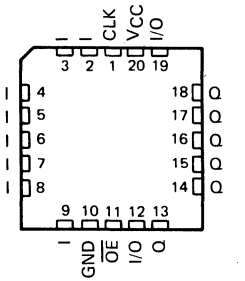
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



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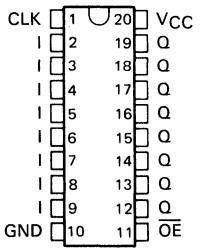
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



PAL16R8'
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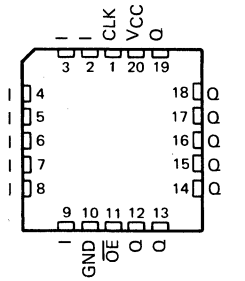
C SUFFIX FN PACKAGE
(TOP VIEW)



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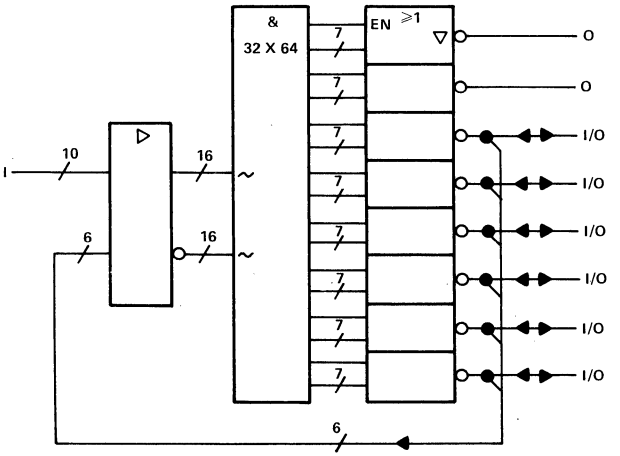
functional block diagrams (positive logic)

'PAL16L8A
'PAL16L8A-2



'PAL16R4A
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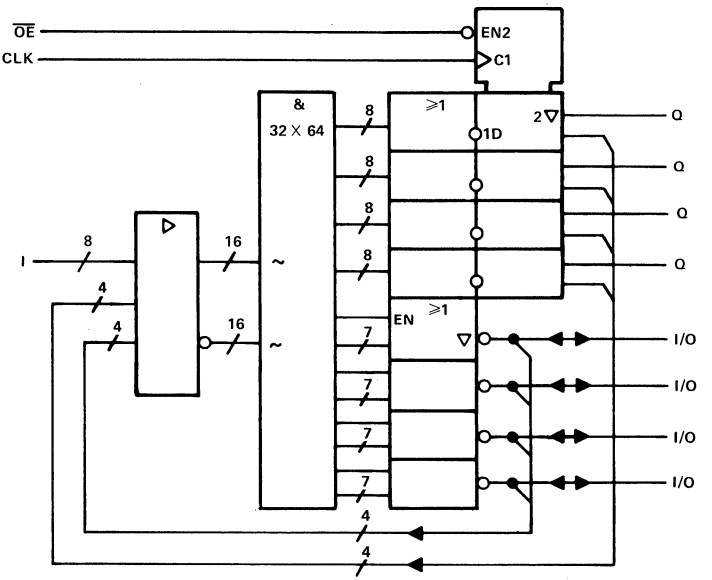

~ denotes fused inputs

functional block diagrams (positive logic)

'PAL16R6A
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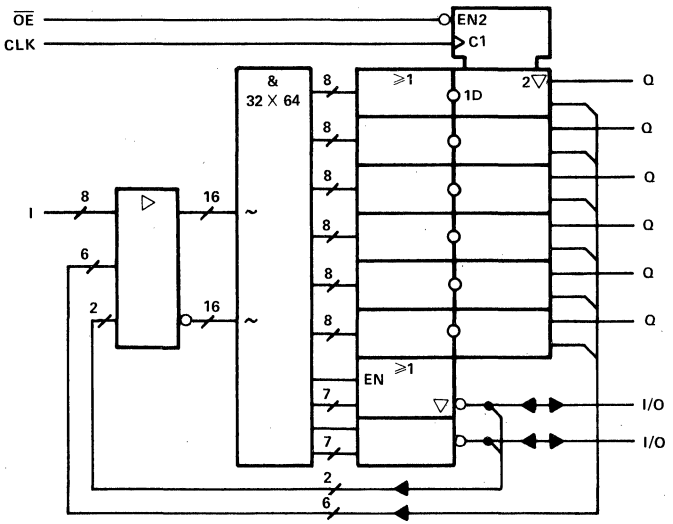
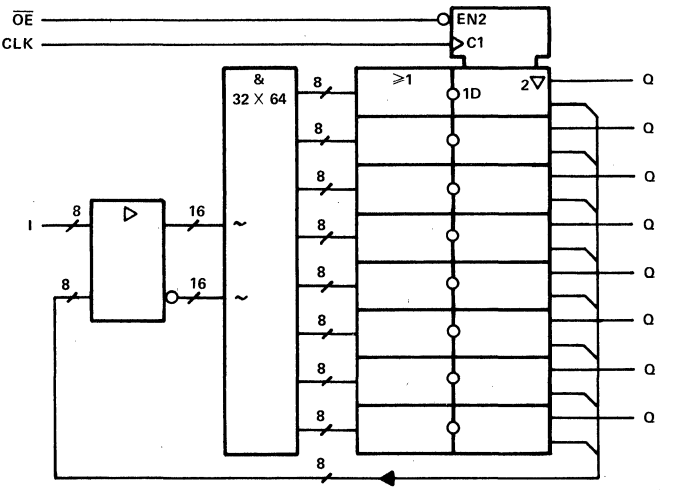
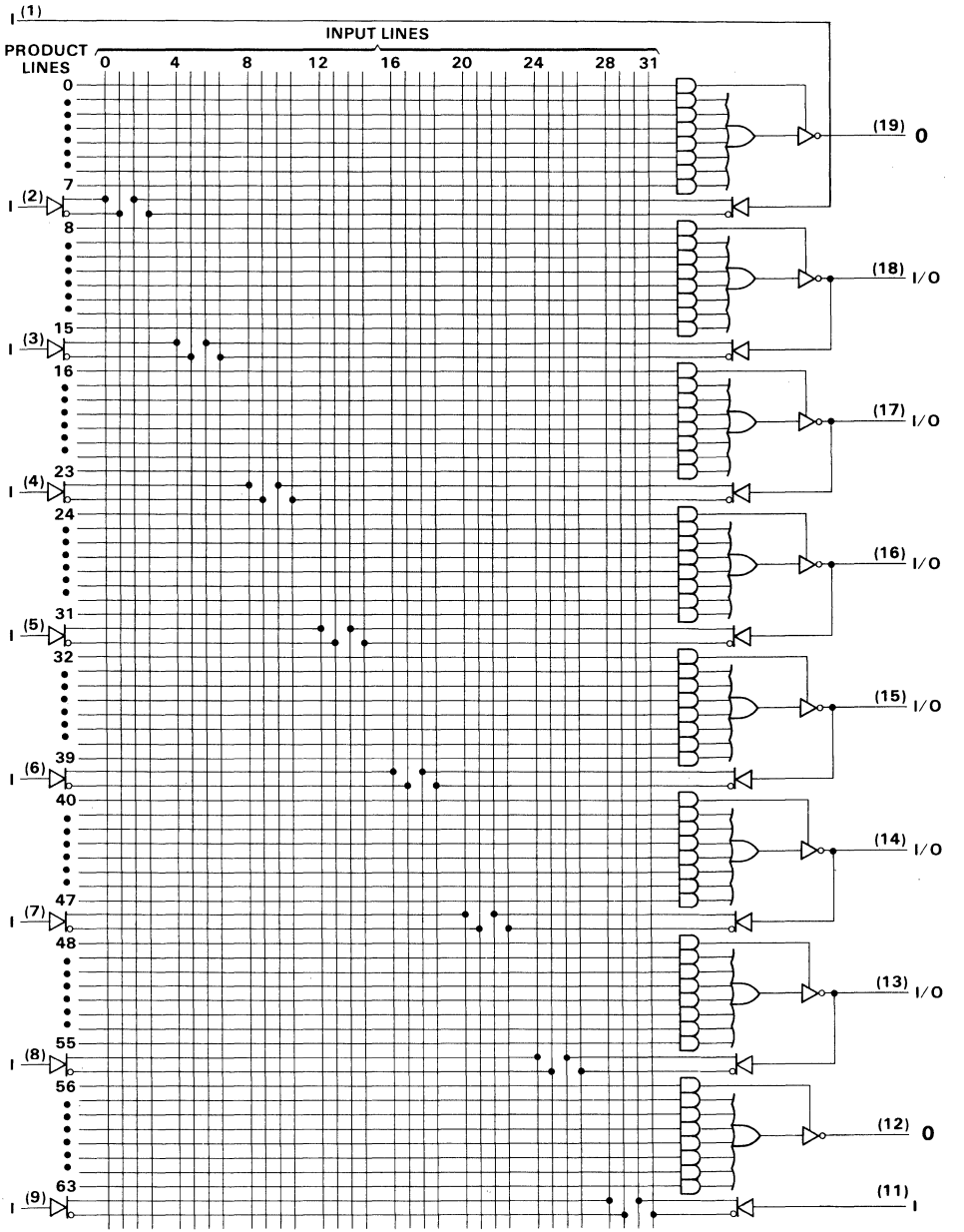


'PAL16R8A
'PAL16R8A-2

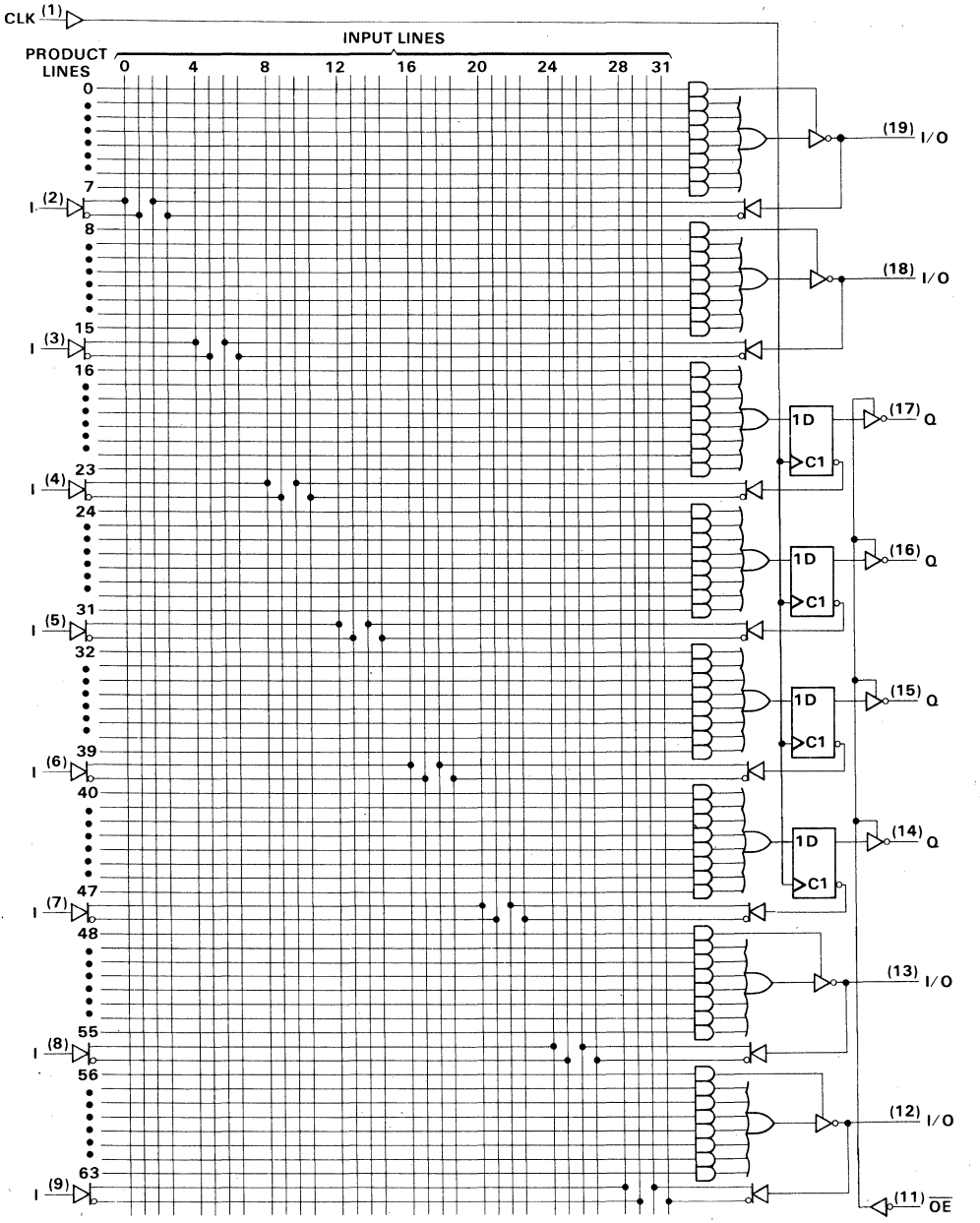


~ denotes fused inputs

logic diagram



logic diagram



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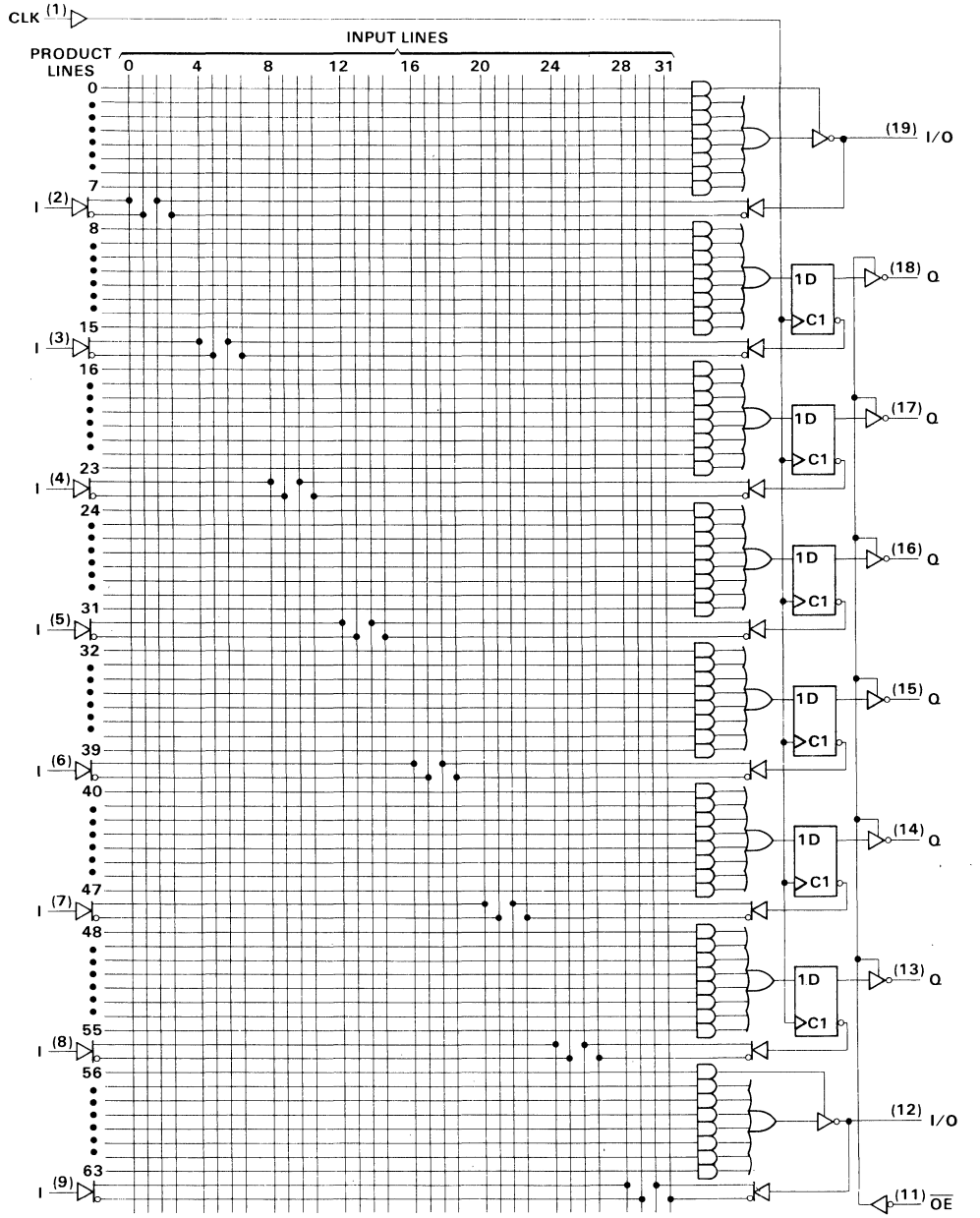
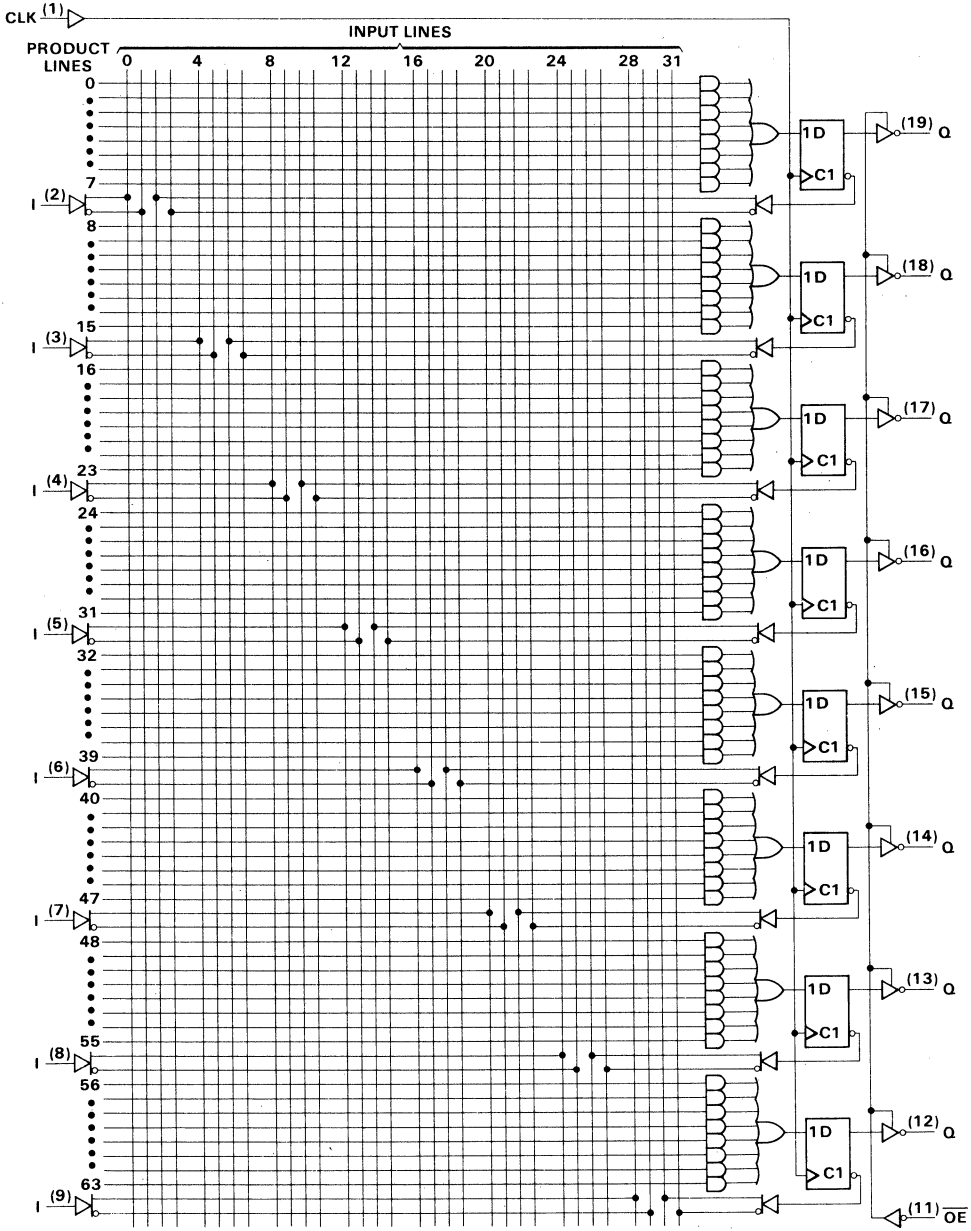
logic diagram



logic diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			M SUFFIX			C SUFFIX			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	$\overline{OE}$ input	2.4		5.5	2		5.5	V
		All others	2		5.5	2		5.5	
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			24	mA
T_A	Operating free-air temperature		−55		125	0		70	°C

programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5762.

recommended operating conditions

			M SUFFIX			C SUFFIX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{clock}	Clock frequency		0		25	0		35	MHz
t_w	Pulse duration, see Note 2	Clock high	15			12			ns
		Clock low	20			16			
t_{su}	Setup time, input or feedback before CLK↑		25			20			ns
t_h	Hold time, input or feedback after CLK↑		0			0			ns

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock}. The minimum pulse durations specified are only for clock high or clock low, but not for both simultaneously.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS†		M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = MAX		2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN, I_{OL} = MAX			0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX, V_O = 2.7 V				20			20	μA
	I/O ports					100			100	
I_{OZL}	Outputs	V_{CC} = MAX, V_O = 0.4 V				−20			−20	μA
	I/O ports					−250			−250	
I_I		V_{CC} = MAX, V_I = 5.5 V				0.2			0.1	mA
I_{IH}		V_{CC} = MAX, V_I = 2.7 V				25			20	μA
I_{IL}		V_{CC} = MAX, V_I = 0.4 V	$\overline{OE}$ INPUT			−0.25			−0.4	mA
			All others			−0.2			−0.2	
I_O§		V_{CC} = MAX, V_O = 2.25 V		−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, V_I = 0 V	Outputs Open		140	185		140	180	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely aproximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}				25	45		35	45		MHz
t_{pd}	I, I/O,	O, I/O			15	30		15	25	ns
t_{pd}	CLK↑	Q	R_L = 500 Ω,		10	20		10	15	ns
t_{en}	$\overline{OE}$↓	Q	C_L = 50 pF,		15	25		15	22	ns
t_{dis}	$\overline{OE}$↑	Q	See Note 3		10	25		10	15	ns
t_{en}	I, I/O	O, I/O			14	30		14	25	ns
t_{dis}	I, I/O	O, I/O			13	30		13	25	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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recommended operating conditions

			M SUFFIX			C SUFFIX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{clock}	Clock frequency		0		16	0		18	MHz
t_w	Pulse duration, see Note 2	Clock high	28			25			ns
		Clock low	28			25			
t_{su}	Setup time, input or feedback before CLK↑		35			28			ns
t_h	Hold time, input or feedback after CLK↑		0			0			ns

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock}. The minimum pulse durations specified are only for clock high or clock low, but not for both simultaneously.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS†			M SUFFIX			C SUFFIX			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX		2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX			0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX,	V_O = 2.7 V				20			20	μA
	I/O ports						100			100	
I_{OZL}	Outputs	V_{CC} = MAX,	V_O = 0.4 V				−20			−20	μA
	I/O ports						−250			−250	
I_I		V_{CC} = MAX,	V_I = 5.5 V				0.2			0.1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V				25			20	μA
I_{IL}		V_{CC} = MAX,	V_I = 0.4 V	$\overline{OE}$ INPUT			−0.2			−0.2	mA
				All others			−0.1			−0.1	
I_O§		V_{CC} = MAX,	V_O = 2.25 V		−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, V_I = 0 V	Outputs Open			75	95		70	90	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely aproximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}				16	25		18	25		MHz
t_{pd}	I, I/O,	O, I/O			25	40		25	35	ns
t_{pd}	CLK↑	Q	R_L = 500 Ω,		11	35		11	25	ns
t_{en}	$\overline{OE}$↓	Q	C_L = 50 pF,		20	35		20	25	ns
t_{dis}	$\overline{OE}$↑	Q	See Note 3		11	30		11	20	ns
t_{en}	I, I/O	O, I/O			25	40		25	35	ns
t_{dis}	I, I/O	O, I/O			25	35		25	30	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

D2706, DECEMBER 1982—REVISED DECEMBER 1987

- **Standard High Speed (25 ns) PAL Family**
- **Choice of Input/Output Configuration**
- **Preload Capability on Output Registers**
- **DIP Options Include Both 300-mil Plastic and 600-mil Ceramic**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PAL20L8A	14	2	0	6
'PAL20R4A	12	0	4 (3-state buffers)	4
'PAL20R6A	12	0	6 (3-state buffers)	2
'PAL20R8A	12	0	8 (3-state buffers)	0

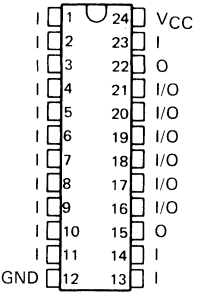
description

These programmable array logic devices feature high speed and a choice of either standard or half-power speeds. They combine Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses. These devices will provide reliable, high performance substitutes over conventional TTL logic. Their easy programmability allows for quick design of "custom" functions and typically result in a more compact circuit board. In addition, chip carriers are also available for further reduction in board space.

In addition, extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The PAL20' series is characterized for operation over the full military temperature range of −55°C to 125°C. The commercial range is characterized from 0°C to 70°C.

PAL20L8'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



PAL20L8'
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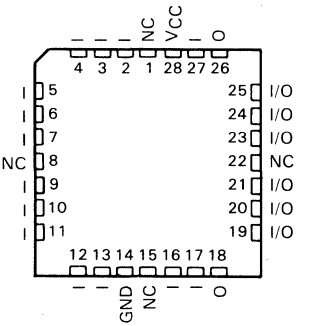
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



2 Data Sheets

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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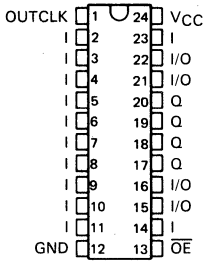
PAL20R4'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



PAL20R4'
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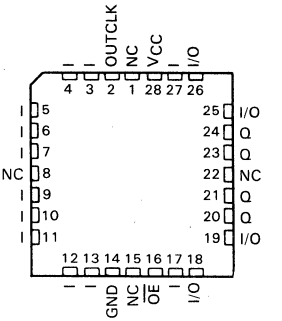

PAL20R6'
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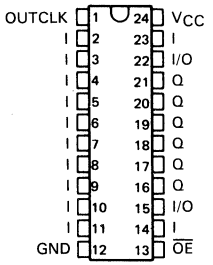
(TOP VIEW)



PAL20R6'
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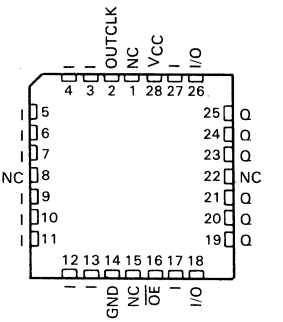
(TOP VIEW)



PAL20R8'
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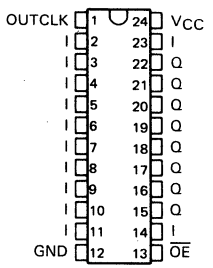
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



PAL20R8'
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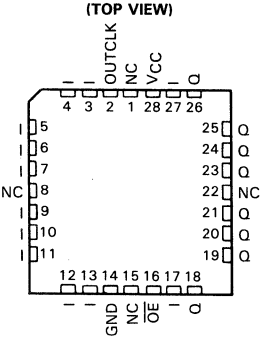
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



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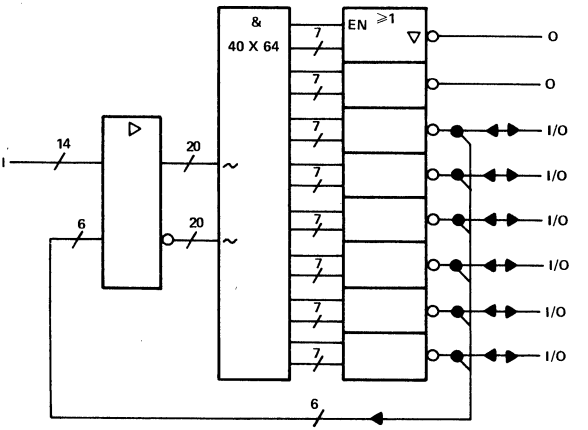
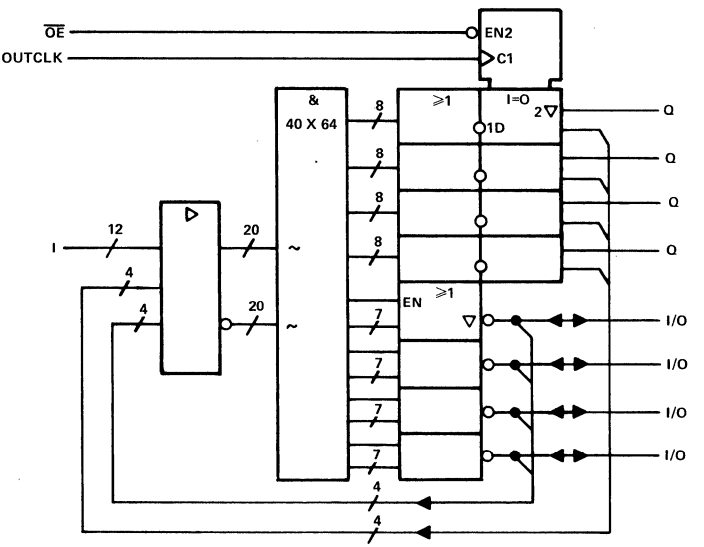
functional block diagrams (positive logic)

PAL20L8A
PAL20L8A-2

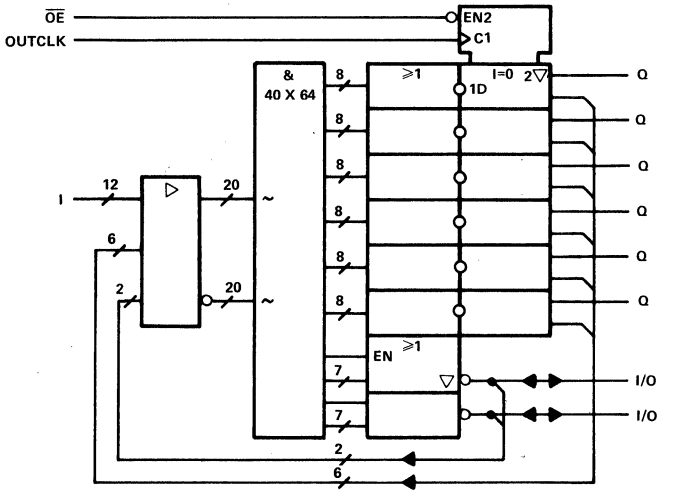


PAL20R4A
PAL20R4A-2



functional block diagrams (positive logic)

PAL20R6A
PAL20R6A-2



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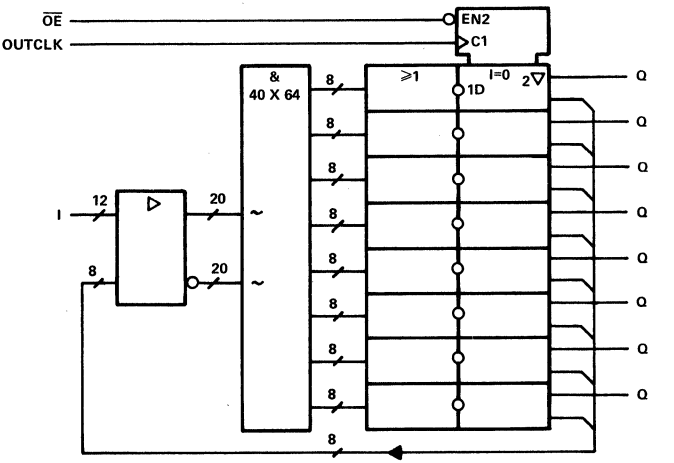

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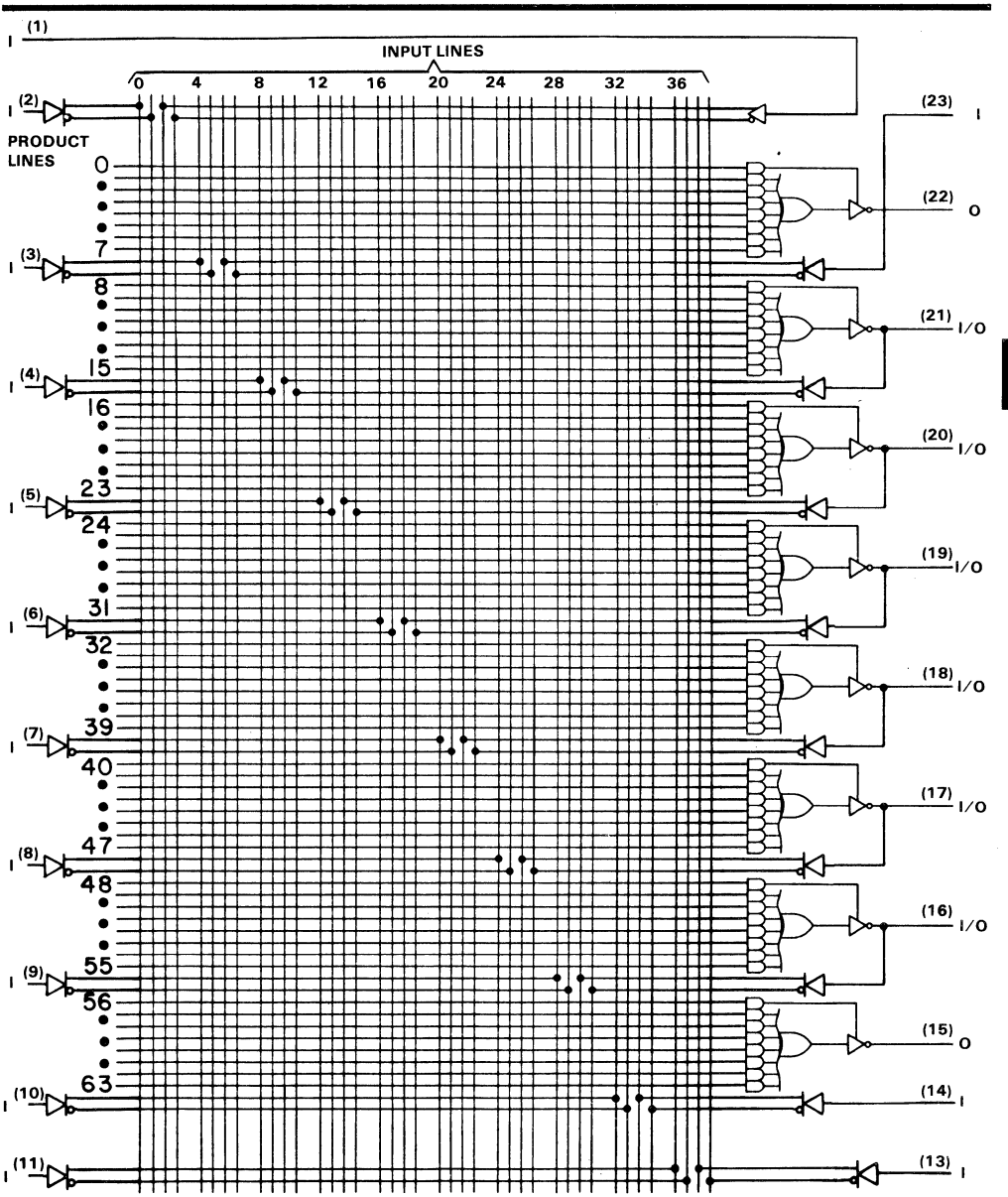
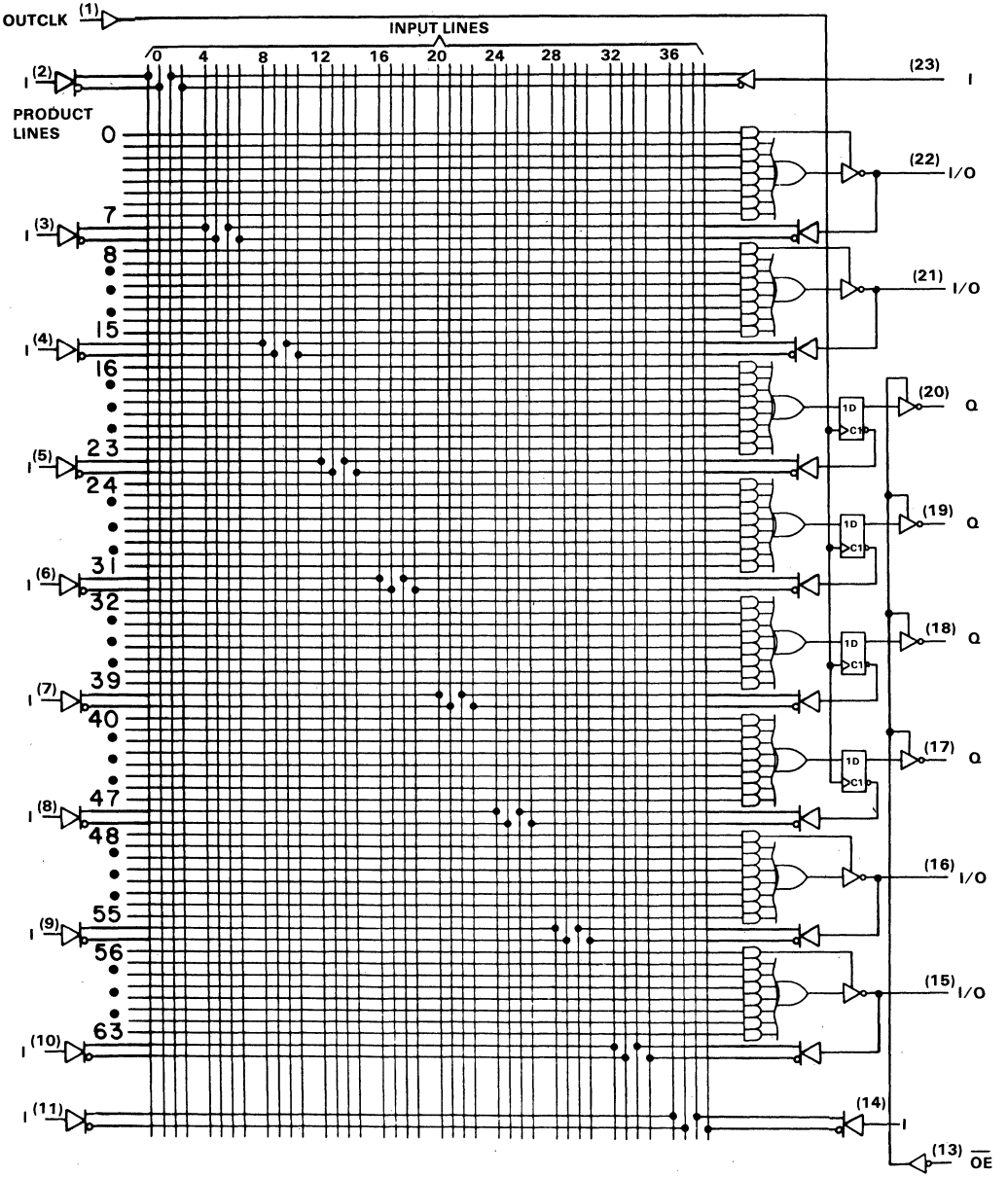

(1)
INPUT LINES
0 4 8 12 16 20 24 28 32 36
(2)
PRODUCT LINES
0
7
(3)
8
15
(4)
16
23
(5)
24
31
(6)
32
39
(7)
40
47
(8)
48
55
(9)
56
63
(10)
(11)
(23) I
(22) O
(21) I/O
(20) I/O
(19) I/O
(18) I/O
(17) I/O
(16) I/O
(15) O
(14) I
(13) I



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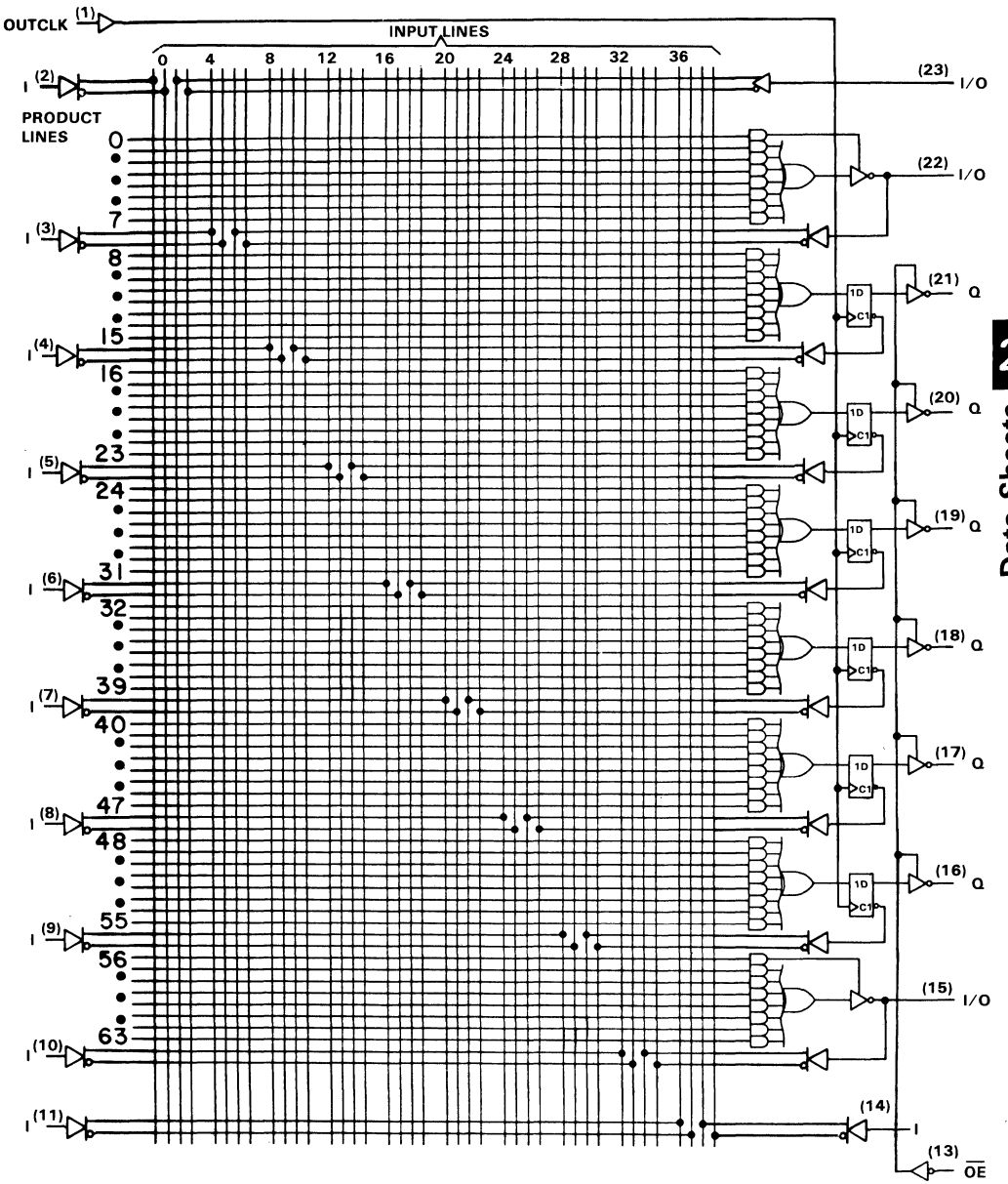
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INPUT LINES
0 4 8 12 16 20 24 28 32 36
I (2)
PRODUCT LINES
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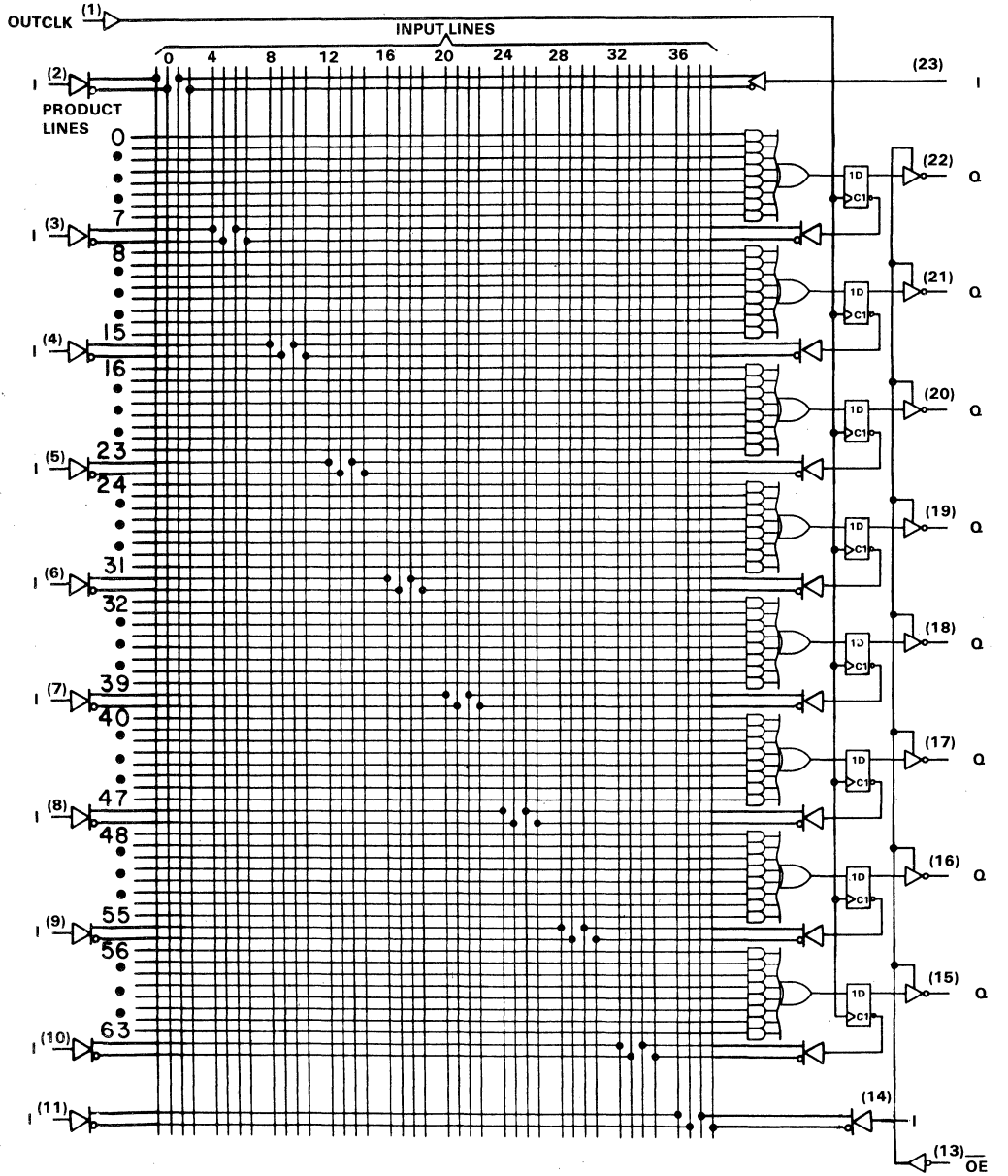
7
I (3)
8
15
I (4)
16
23
I (5)
24
31
I (6)
32
39
I (7)
40
47
I (8)
48
55
I (9)
56
63
I (10)
I (11)
(23) I/O
(22) I/O
(21) Q
(20) Q
(19) Q
(18) Q
(17) Q
(16) Q
(15) I/O
(14) I
(13) OE
1D
C1



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M SUFFIX . . . . . −55°C to 125°C
C SUFFIX . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			M SUFFIX			C SUFFIX			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		20	0		30	MHz
t_w	Pulse duration, clock	High	20			15			ns
		Low	20			15			ns
t_{su}	Setup time, input or feedback before OUTCLK↑		30			25			ns
t_h	Hold time, input or feedback after OUTCLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5762.

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†	M SUFFIX			C SUFFIX			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN, I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = MAX, V_{IH} = 2.7 V			20			20	μA
	I/O ports				100			100	
I_{OZL}	O, Q outputs	V_{CC} = MAX, V_{IH} = 0.4 V			−20			−20	μA
	I/O ports				−250			−250	
I_I	$\overline{OE}$ Input	V_{CC} = MAX, V_I = 5.5 V			0.2			0.2	mA
	All others				0.1			0.1	
I_{IH}	$\overline{OE}$ Input	V_{CC} = MAX, V_I = 2.7 V			40			40	μA
	All others				20			20	
I_{IL}	$\overline{OE}$ Input	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
	All others				−0.2			−0.2	
I_O§		V_{CC} = MAX, V_O = 2.25 V	−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, V_I = 0 V, Outputs open, $\overline{OE}$ at V_{IH}		150	210		150	210	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}				20			30			MHz
t_{pd}	I, I/O	O, I/O			15	30		15	25	ns
t_{pd}	OUTCLK↑	Q	R_L = 500 Ω,		10	20		10	15	ns
t_{en}	$\overline{OE}$	Q	C_L = 50 pF		10	25		10	20	ns
t_{dis}	$\overline{OE}$↑	Q	See Note 2		11	25		11	20	ns
t_{en}	I, I/O	O, I/O			14	30		14	25	ns
t_{dis}	I, I/O	O, I/O			12	30		12	25	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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PRELOAD PROCEDURES

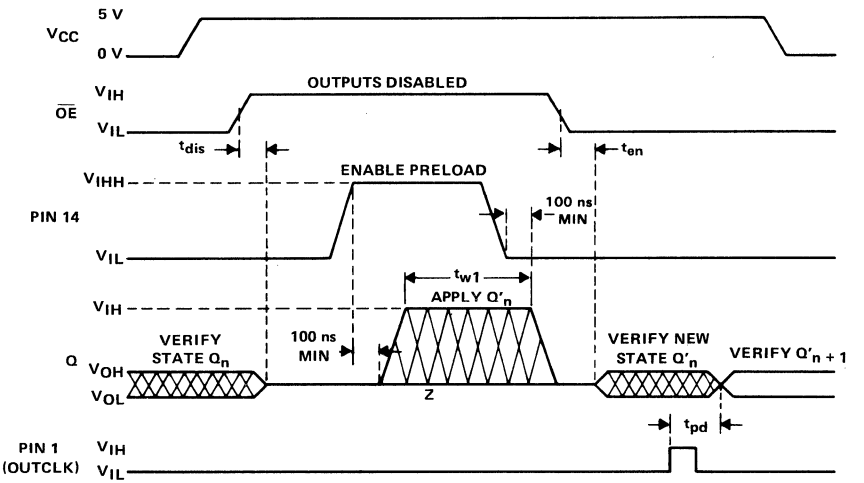


FIGURE 1. PRELOAD WAVEFORMS

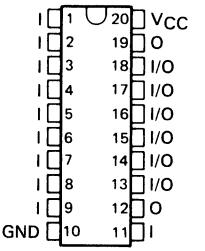
preload procedure for registered outputs

Step 1 Pin 13 to V_{IH}, Pin 1 to V_{IL}, and V_{CC} to 5 volts.
Step 2 Pin 14 to V_{IHH} for 10 to 50 microseconds.
Step 3 Apply V_{IL} for a low and V_{IH} for a high at the Q outputs.
Step 4 Pin 14 to V_{IL}.
Step 5 Remove the voltages applied to the outputs.
Step 6 Pin 13 to V_{IL}.
Step 7 Check the output states to verify preload.

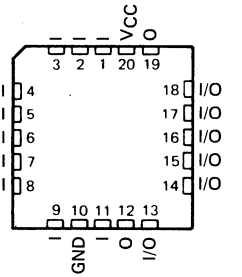
D3085, JANUARY 1988

- **Very-High-Speed Address Decoder (Ideal for Use with High Speed Processors)**
- **I/O Propagation Delay: 7 ns Max**
- **Field Programmable on Standard PLD Programmers**
- **Fully TTL Compatible**
- **Security Fuse Prevents Unauthorized Duplication**
- **Dependable Texas Instruments Quality and Reliability**
- **Potential Applications**
  - **Address Decoders**
  - **Code Detectors**
  - **Peripheral Selectors**
  - **Fault Monitors**
  - **Machine State Decoders**

J OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TIBPAD16N8 is a very-high-speed Programmable Address Decoder featuring 7 ns maximum propagation delay, the highest speed in the TTL programmable logic family. The TIBPAD16N8 utilizes the IMPACT-X™ process and proven titanium-tungsten fuse technology to provide reliable, high performance substitutes for conventional TTL logic.

The TIBPAD16N8 contains 10 dedicated inputs and 8 outputs. Each output has two product terms, one of which is used to enable the inverting buffer associated with the respective output. Six of the outputs are I/O ports, the remaining two are dedicated outputs. Each of the six I/O ports can be individually programmed as an input or an output; this allows the device to be used for functions requiring up to 16 inputs and and 2 outputs or 10 inputs and 8 outputs.

The TIBPAD16N8 is supplied with all six I/O ports in the input configuration (output buffers in the high-impedance state). If an I/O port is selected to be an output, it must be programmed accordingly. It is recommended that all unused outputs on this device remain in the three-state condition for better noise immunity.

The TIBPAD16N8-7C is characterized for operation from 0°C to 75°C.

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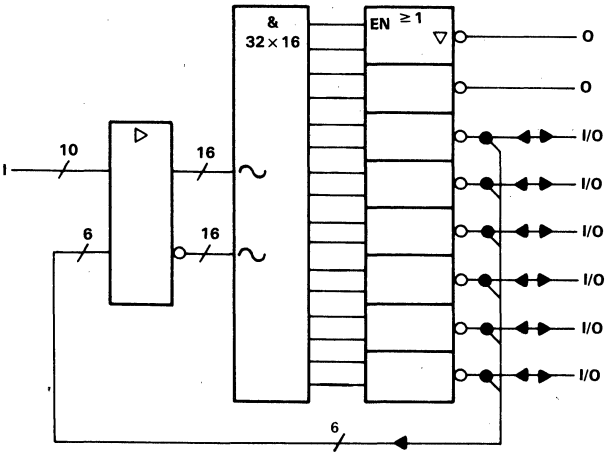
functional block diagram (positive logic)



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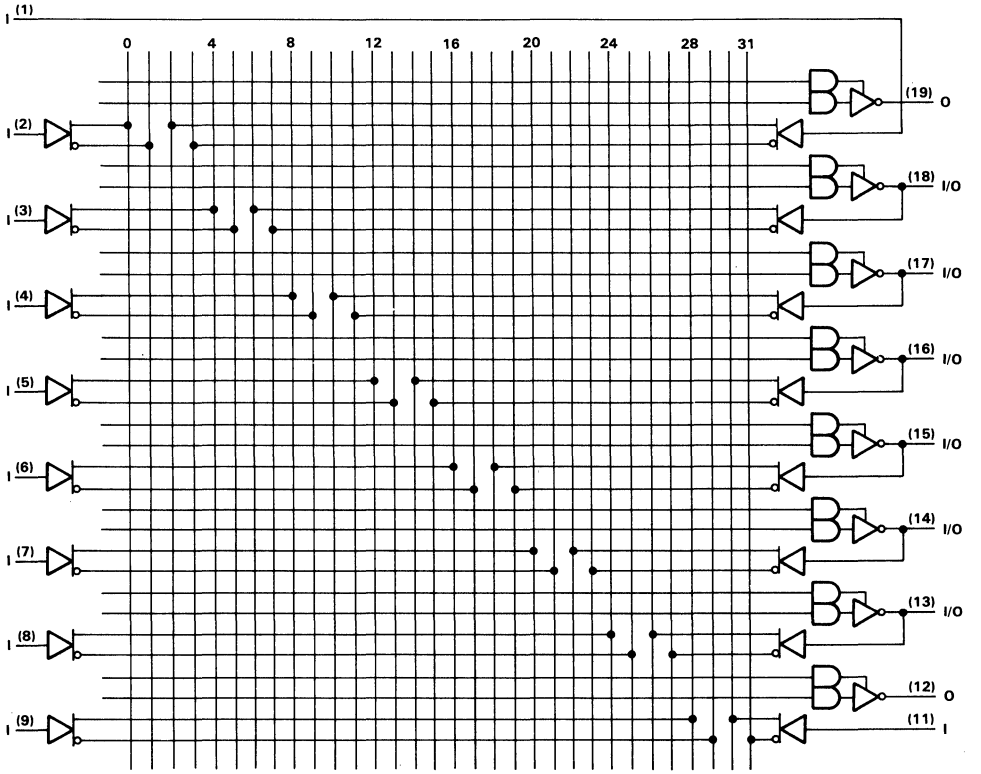
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during programming cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−3.2	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		75	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V, I_I = −18 mA			−1.5	V
V_{OH}	V_{CC} = 4.75 V, I_{OH} = −3.2 mA	2.4	3		V
V_{OL}	V_{CC} = 4.75 V, I_{OL} = 24 mA		0.3	0.5	V
I_I	V_{CC} = 5.25 V, V_I = 5.5 V			0.2	mA
I_{OZH}‡	V_{CC} = 5.25 V, V_O = 2.7 V			0.1	mA
I_{OZL}‡	V_{CC} = 5.25 V, V_O = 0.4 V			−0.1	mA
I_{IH}‡	V_{CC} = 5.25 V, V_I = 2.7 V			25	μA
I_{IL}‡	V_{CC} = 5.25 V, V_I = 0.4 V			−0.25	mA
I_O§	V_{CC} = 5 V, V_O = 0.5 V	−30	−70	−130	mA
I_{CC}	V_{CC} = 5.25 V, V_I = 0, Outputs open		120	180	mA
C_I	V_I = 2 V		5		pF
C_o	V_O = 2 V		6		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}.
§ This parameter approximates I_{OS}. The condition V_O = 0.5 V takes tester noise into account. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics with two outputs switching (typical PAD mode) over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd}	I, I/O	O, I/O 2 outputs switching	R1 = 200 Ω, R2 = 390 Ω	2	5	7	ns
t_{en}	I, I/O	O, I/O		3	8	10	ns
t_{dis}	I, I/O	O, I/O		3	8	10	ns

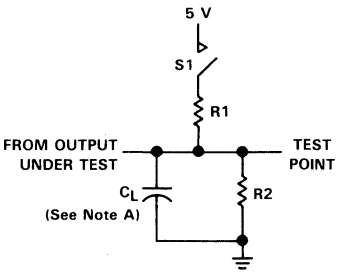
† All typical values are at V_{CC} = 5 V, T_A = 25°C

programming information

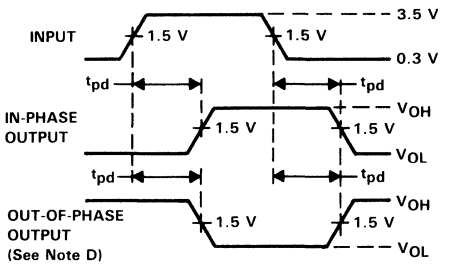
Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5762.

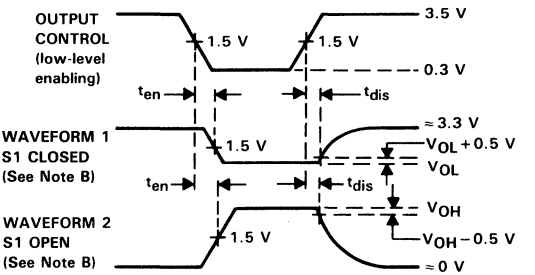
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR
THREE-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

FIGURE 1

WORST CASE MULTIPLE OUTPUT SWITCHING CHARACTERISTICS

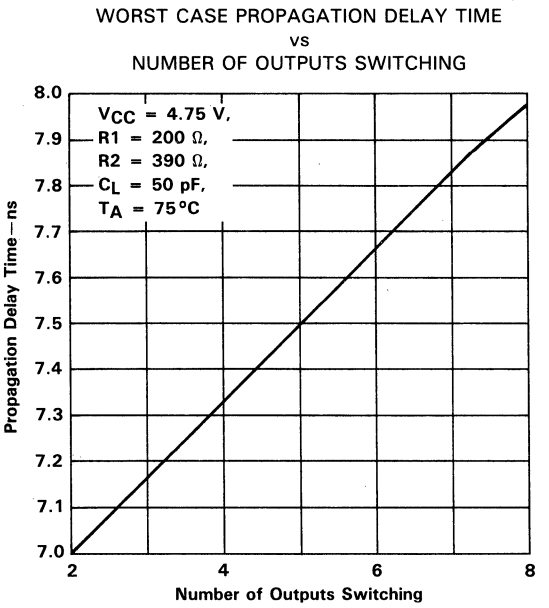


FIGURE 2

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TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

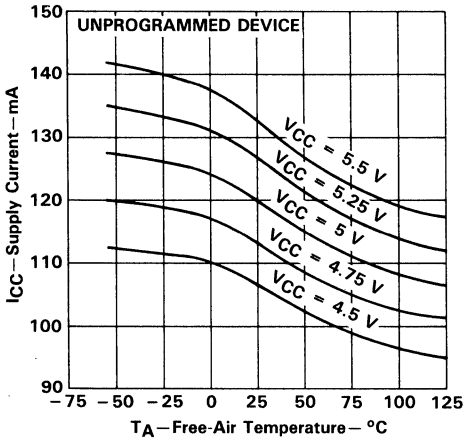


FIGURE 3

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

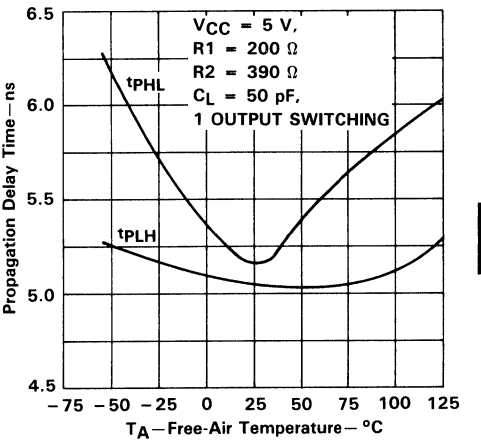


FIGURE 4

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

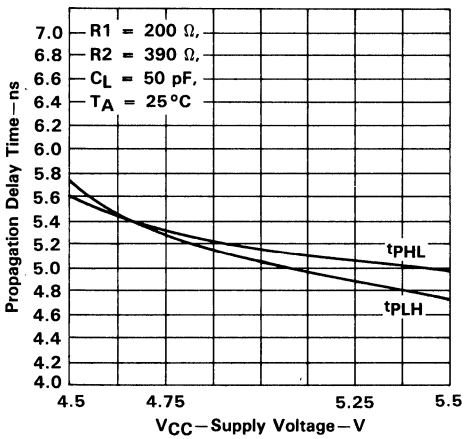


FIGURE 5

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

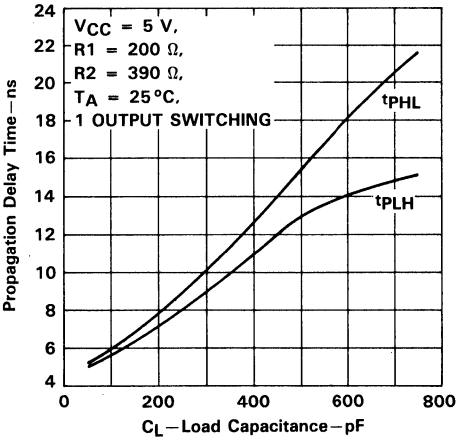
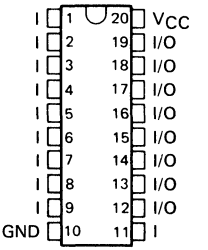


FIGURE 6

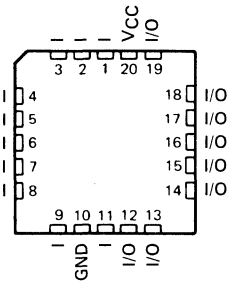
D3086, DECEMBER 1987

- Very High Speed Address Decoder (Ideal for Use with High Speed Processors)
- I/O Propagation Delay: 6 ns Max
- Suitable for High Speed NAND-NAND Logic Implementation
- Field Programmable on Standard PLD Programmers
- Fully TTL Compatible
- Security Fuse Prevents Unauthorized Duplication
- Dependable Texas Instruments Quality and Reliability
- Potential Applications
  - Address Decoders
  - Random Logic (NAND-NAND)
  - Code Detectors
  - Peripheral Selectors
  - Fault Monitors
  - Machine State Decoders

J OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TIBPAD18N8-6C is a very-high-speed Programmable Address Decoder featuring 6-ns maximum propagation delay, the highest speed in the TTL programmable logic family. The TIBPAD18N8 uses the IMPACT-X™ process and proven titanium-tungsten fuse technology to provide reliable, high-performance substitutes for conventional TTL logic.

The TIBPAD18N8-6C contains 10 dedicated inputs and 8 product terms, each followed by an inverting buffer leading to an I/O port. Each of the eight I/O ports can be individually programmed as an input or an output, depending on the state of the fuse controlling the output buffer, as indicated by Table 1. This allows the device to be used for functions ranging from 17 inputs and a single output to 10 inputs and 8 outputs.

A high-speed feedback path, which does not go through the output buffer, is provided to offer higher performance operation in designs where feedback is required. The architectural fuse on the I/O multiplexer is used for the selection of this path (see Table 2). This makes the TIBPAD18N8-6C ideal for the implementation of a very fast NAND-NAND logic.

The TIBPAD18N8 is supplied with all eight I/O ports in the input configuration (output buffers in the high-impedance state). If an I/O port is selected to be an output, it must be programmed accordingly. It is recommended that all unused outputs on this device remain in the high-impedance state for better noise immunity.

The TIBPAD18N8-6C is characterized for operation from 0°C to 75°C.

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PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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functional block diagram (positive logic)

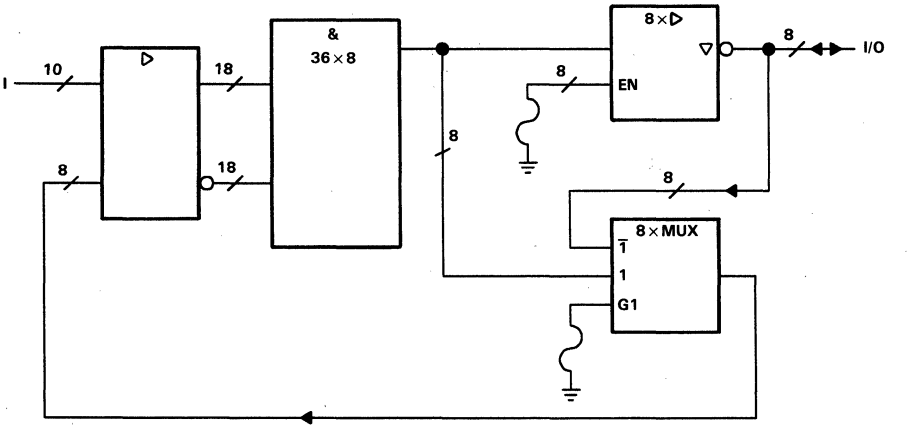


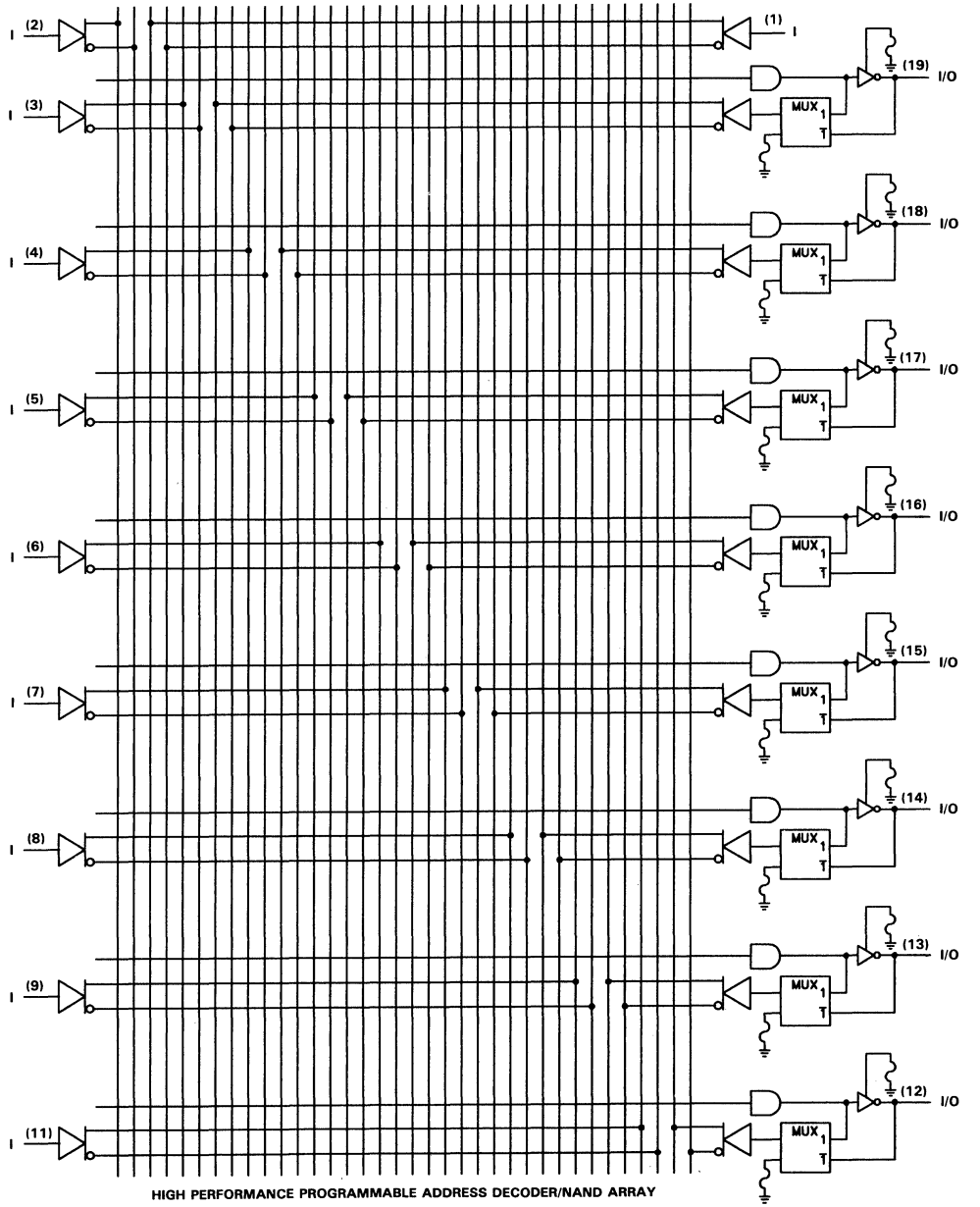
Table 1. Output Buffer Programming

ARCHITECTURAL FUSE	OPERATION
Intact	Input (Output Buffer in Hi-Z State)
Blown	Output

Table 2. I/O Multiplexer Programming

ARCHITECTURAL FUSE	OPERATION
Intact	I/O Feedback
Blown	High-Speed Feedback

logic diagram (positive logic)



HIGH PERFORMANCE PROGRAMMABLE ADDRESS DECODER/NAND ARRAY

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)	2			V
V_{IL}	Low-level input voltage (see Note 2)			0.8	V
I_{OH}	High-level output current			−3.2	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V, I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.75 V, I_{OH} = MAX	2.4	3		V
V_{OL}	V_{CC} = 4.75 V, I_{OL} = MAX		0.37	0.5	V
I_{OZH}	V_{CC} = 5.25 V, V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.25 V, V_O = 0.4 V			−20	μA
I_I	V_{CC} = 5.25 V, V_I = 5.5 V			0.2	μA
I_{IH}	V_{CC} = 5.25 V, V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.25 V, V_I = 0.4 V			−0.25	mA
I_{OS}	V_{CC} = 5.25 V, V_O = 0 V				mA
I_{CC}	V_{CC} = 5.25 V, V_I = 4.5 V		140	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd}	I	I/O (no feedback)	R1 = 200 Ω, R2 = 390 Ω, C_L = 50 pF		4	6	ns
		I/O (with 1 feedback path − I/O MUX fuse blown)			8	10	ns
		I/O (with 2 feedback paths − I/O MUX fuse blown)			12	14	ns
		I/O (with 3 feedback paths − I/O MUX fuse blown)			16	18	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

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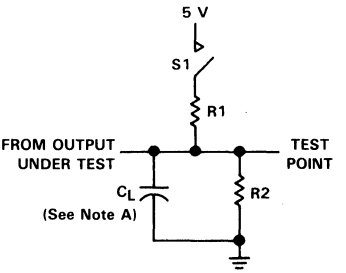
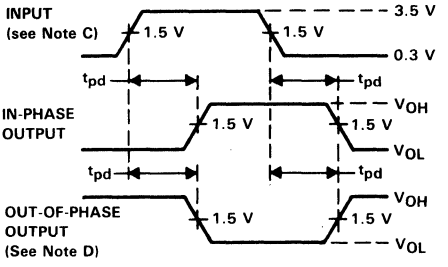
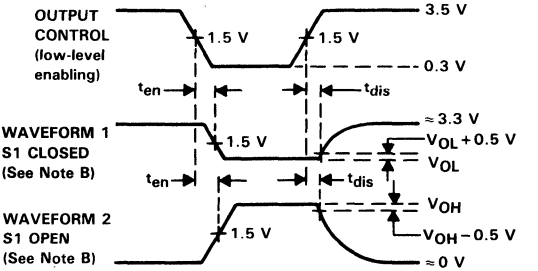
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR THREE-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

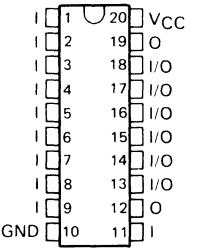
NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

FIGURE 1

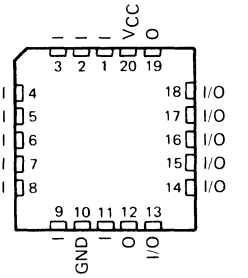
- **High-Performance Operation:**
  - **f_{max} (w/o feedback)**
    - **TIBPAL16R'-10C Series . . . 62.5 MHz**
    - **TIBPAL16R'-12M Series . . . 56 MHz**
  - **f_{max} (with feedback)**
    - **TIBPAL16R'-10C Series . . . 55.5 MHz**
    - **TIBPAL16R'-12M Series . . . 48 MHz**
  - **Propagation Delay**
    - **TIBPAL16L-10C . . . 10 ns Max**
    - **TIBPAL16L-12M . . . 12 ns Max**
- **Functionally Equivalent, but Faster than Existing 20-Pin PALs**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Remain High)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Security Fuse Prevents Duplication**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state)	4
PAL16R6	8	0	6 (3-state)	2
PAL16R8	8	0	8 (3-state)	0

TIBPAL16L8'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16L8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom-functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

All of the register outputs are set to a low level during power-up. Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL16' M series is characterized for operation over the full military temperature range of −55°C to 125°C. The TIBPAL16' C series is characterized for operation from 0°C to 75°C.

IMPACT™ is a trademark of Texas Instruments Incorporated.
PAL® is a registered trademark of Monolithic Memories Inc.
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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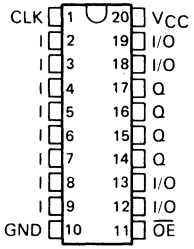
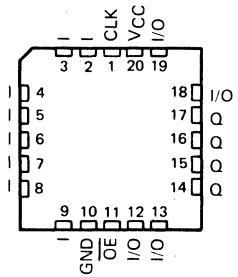
TIBPAL16R4'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16R4'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL16R6'
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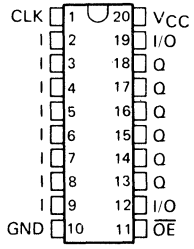
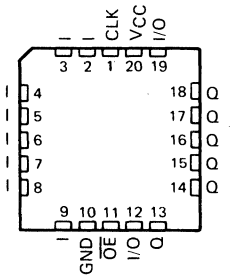
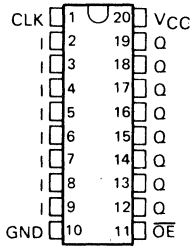
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



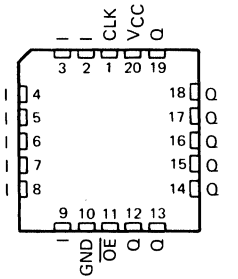
TIBPAL16R6'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL16R8'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16R8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode

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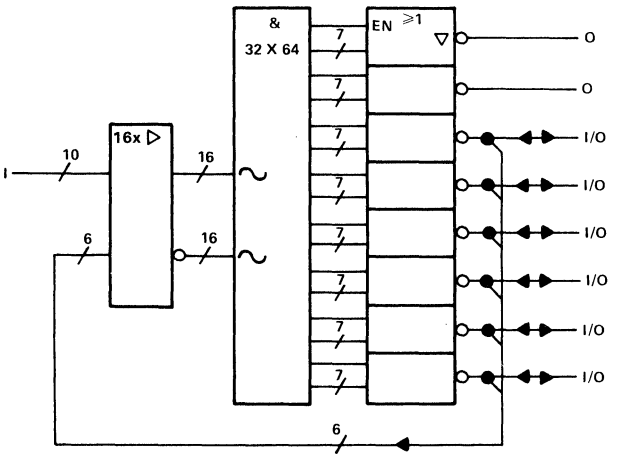
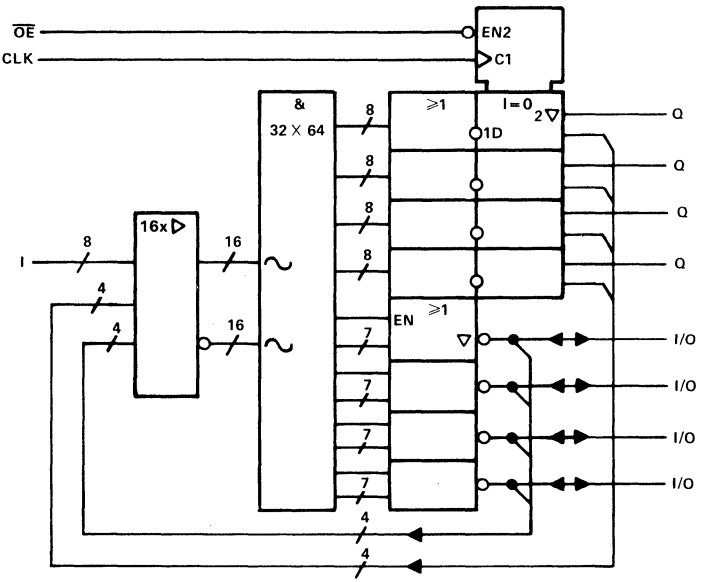
functional block diagrams (positive logic)

'PAL16L8



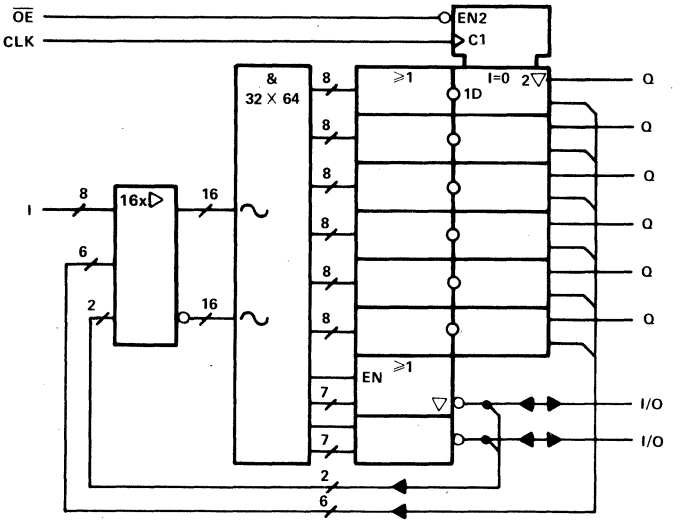
'PAL16R4



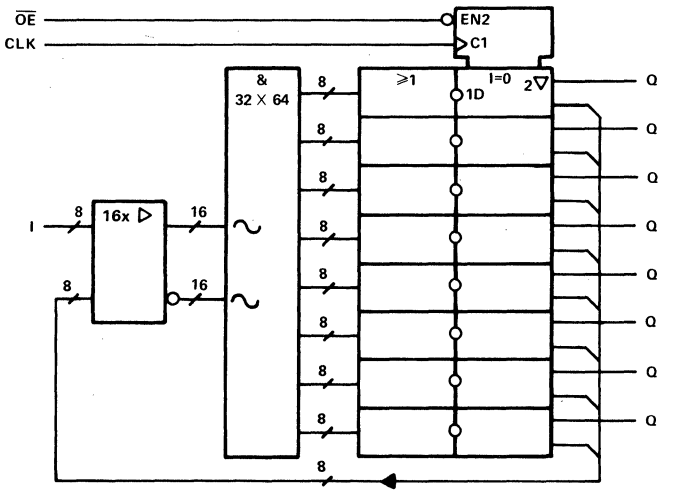
~ denotes fused inputs

functional block diagrams (positive logic)

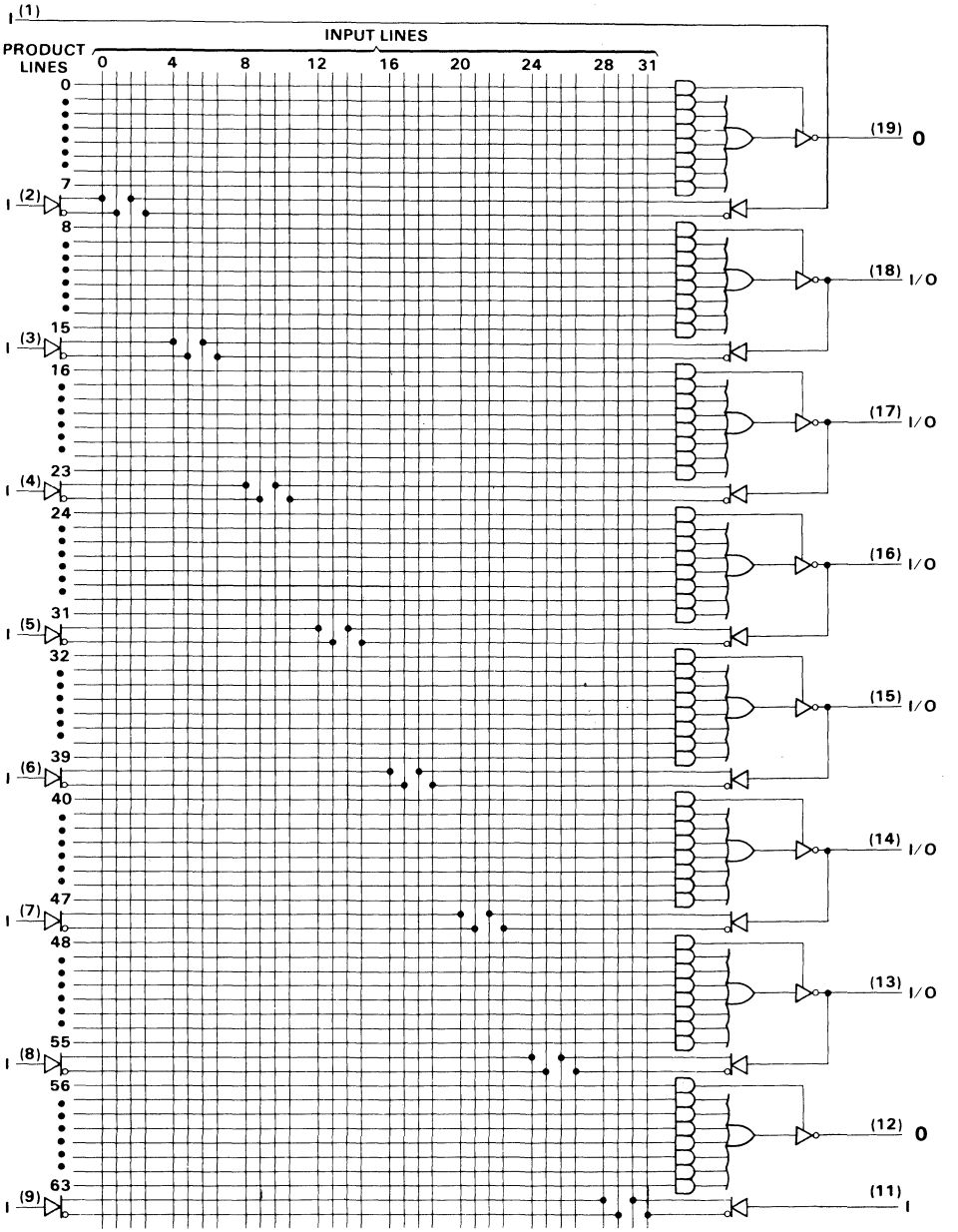
'PAL16R6

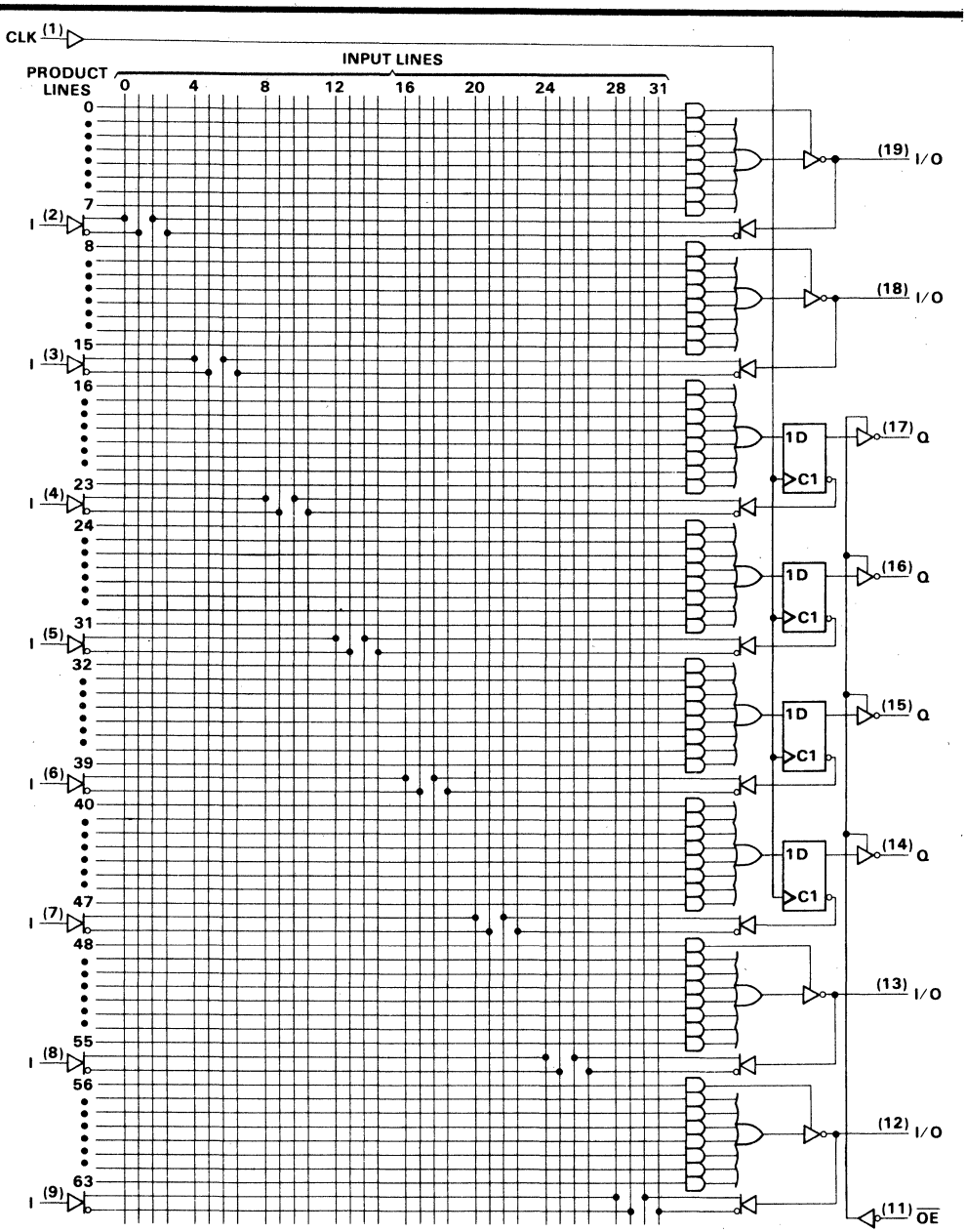


'PAL16R8



∼ denotes fused inputs


(1)
INPUT LINES
PRODUCT LINES
0
4
8
12
16
20
24
28
31
0
7
(2)
8
15
(3)
16
23
(4)
24
31
(5)
32
39
(6)
40
47
(7)
48
55
(8)
56
63
(9)
(19) 0
(18) I/O
(17) I/O
(16) I/O
(15) I/O
(14) I/O
(13) I/O
(12) 0
(11) I



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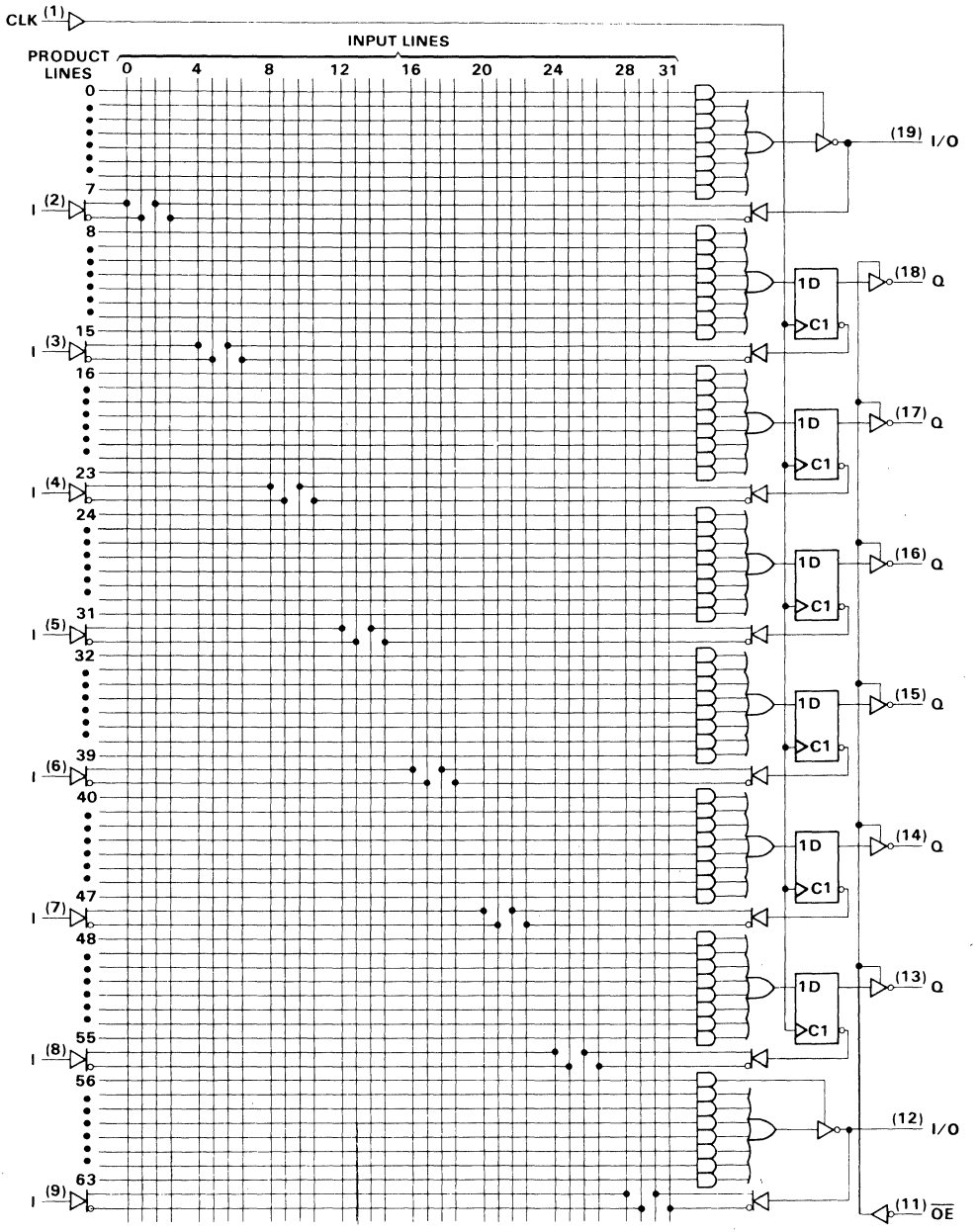
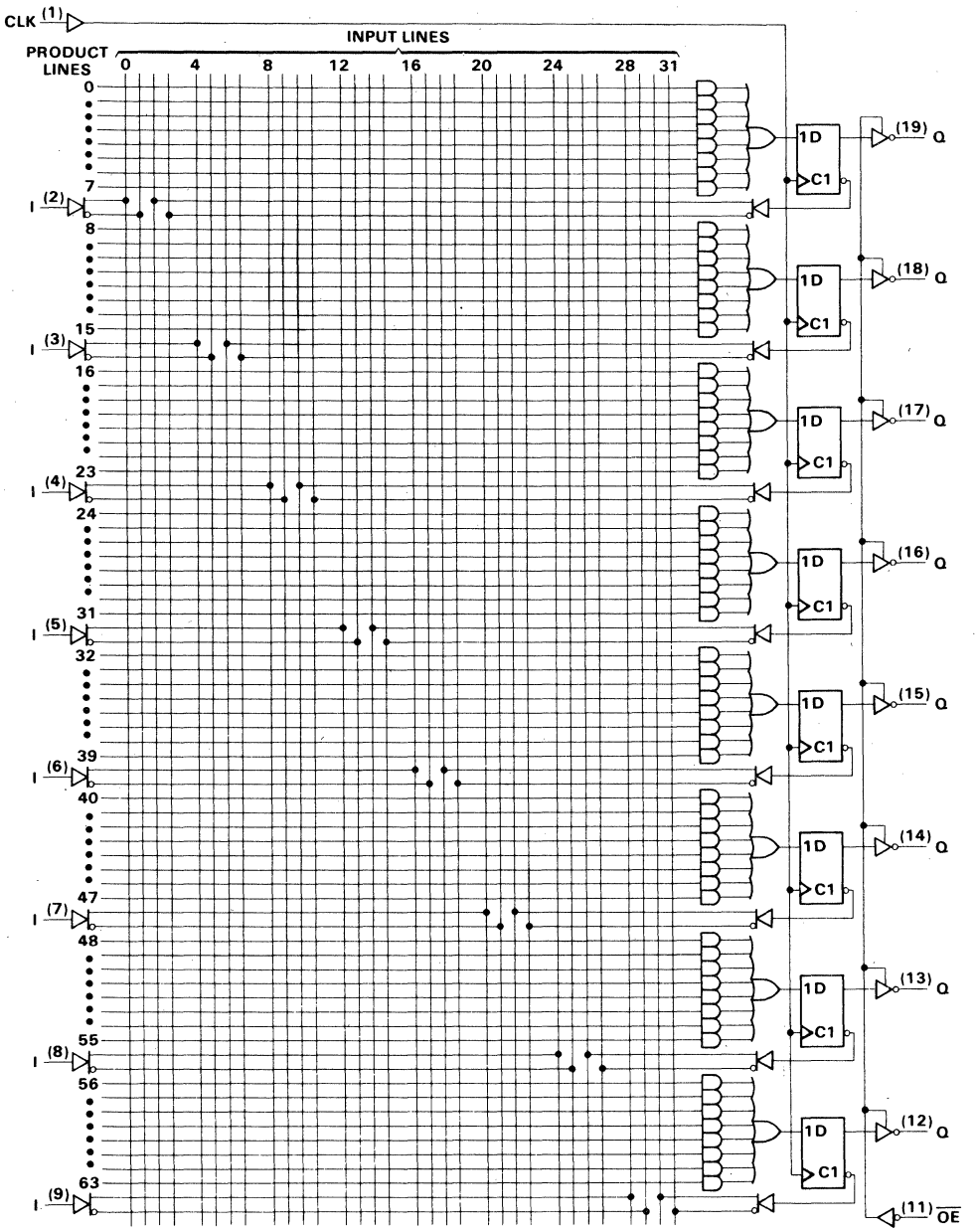

CLK (1)
INPUT LINES
PRODUCT LINES
0
4
8
12
16
20
24
28
31
0
7
8
15
16
23
24
31
32
39
40
47
48
55
56
63
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(19) I/O
(18) Q
(17) Q
(16) Q
(15) Q
(14) Q
(13) Q
(12) I/O
(11) OE
1D
C1


CLK (1)
INPUT LINES
PRODUCT LINES
0 4 8 12 16 20 24 28 31
0
7
(2)
8
15
(3)
16
23
(4)
24
31
(5)
32
39
(6)
40
47
(7)
48
55
(8)
56
63
(9)
1D
C1
(19) Q
(18) Q
(17) Q
(16) Q
(15) Q
(14) Q
(13) Q
(12) Q
(11) $\overline{OE}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			-12M			-10C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		56	0		62.5	MHz
t_w	Pulse duration, clock (see Note2)	High	9			8			ns
		Low	9			8			
t_{su}	Setup time, input or feedback before CLK↑		11			10			ns
t_h	Hold time, input or feedback after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55	25	125	0	25	75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics, over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS†		-12M			-10C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA		−0.8	−1.5		−0.8	−1.5	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3.2		V
V_{OL}	V_{CC} = MIN,	I_{OL} = MAX		0.3	0.5		0.3	0.5	V
I_{OZH}§	V_{CC} = MAX,	V_O = 2.4 V			100			100	μA
I_{OZL}§	V_{CC} = MAX,	V_O = 0.4 V			−100			−100	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			0.2			0.2	mA
I_{IH}§	V_{CC} = MAX,	V_I = 2.4 V			25			25	μA
I_{IL}§	V_{CC} = MAX,	V_I = 0.4 V		−0.08	−0.25		−0.08	−0.25	mA
I_{OS}¶	V_{CC} = 5 V,	V_O = 0	−30	−70	−130	−30	−70	−130	mA
I_{CC}	V_{CC} = MAX, V_I = 0 V,	Outputs Open		140	180		140	180	mA
C_{in}	f = 1 MHz,	V_I = 2 V		5			5		pF
C_{out}	f = 1 MHz,	V_O = 2 V		6			6		pF
C_{CLK}	f = 1 MHz,	V_{CLK} = 2 V		6			6		pF

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.
¶ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	-12M			-10C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}‡	With Feedback		R1 = 200 Ω, R_2 = 390 Ω, See Figure 1	48	80		55.5	80		MHz
	Without Feedback			56	85		62.5	85		
t_{pd}	I, I/O	O, I/O		3	7	12	3	7	10	ns
t_{pd}	CLK↑	Q		2	5	10	2	5	8	ns
t_{en}	OE↓	Q		1	4	10	1	4	10	ns
t_{dis}	OE↑	Q		1	4	10	1	4	10	ns
t_{en}	I, I/O	O, I/O		3	8	12	3	8	10	ns
t_{dis}	I, I/O	O, I/O		3	8	12	3	8	10	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ f_{max} (with feedback) = $\frac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, f_{max} (without feedback) = $\frac{1}{t_w\ \text{high} + t_w\ \text{low}}$.

programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5762.

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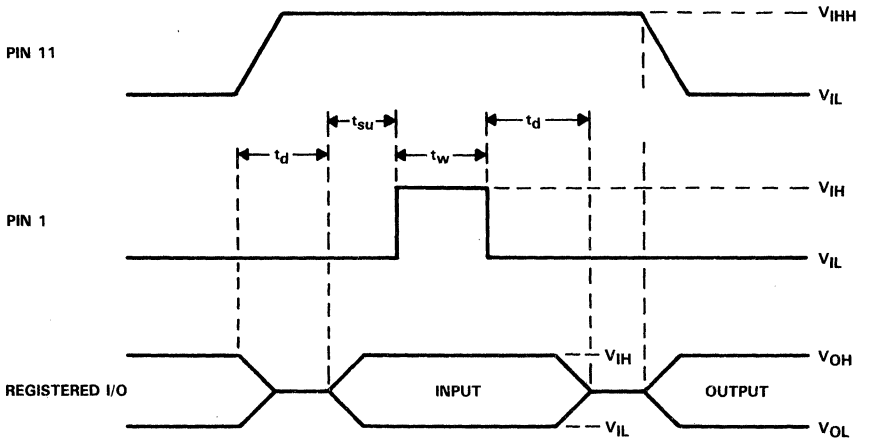
preload procedure for registered outputs (see Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

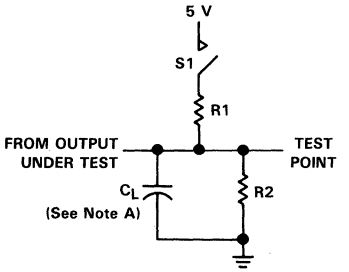
Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 11 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 11 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

preload waveforms (see Note 3)

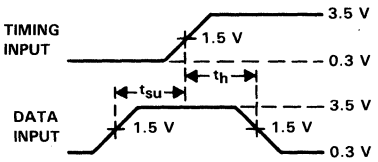


NOTE 3: $t_d = t_{su} = t_w$ = 100 ns to 1000 ns.
V_{IHH} = 10.25 V to 10.75 V.

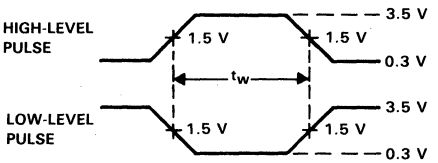
PARAMETER MEASUREMENT INFORMATION



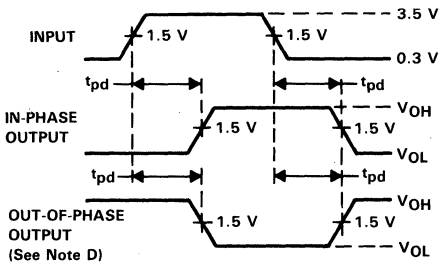
LOAD CIRCUIT FOR THREE-STATE OUTPUTS



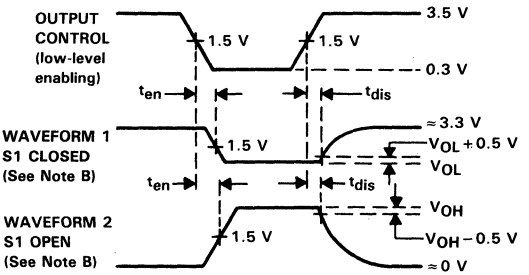
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

FIGURE 1

metastable characteristics for TIBPAL16R4-10C, TIBPAL16R6-10C, and TIBPAL16R8-10C

At some point in every system designer's career, he or she is faced with the problem of synchronizing two digital signals operating at two different frequencies. This problem is typically overcome by synchronizing one of the signals to the local clock through use of a flip-flop. However, this solution presents an awkward dilemna since the setup and hold time specifications associated with the flip-flop are sure to be violated. The metastable characteristics of the flip-flop can influence overall system reliability.

Whenever the setup and hold times of a flip-flop are violated, its output response becomes uncertain and is said to be in the metastable state if the output hangs up in the region between V_{IL} and V_{IH}. This metastable condition lasts until the flip-flop falls into one of its two stable states, which takes longer than the specified maximum propagation delay time (CLK to Q max).

From a system engineering standpoint, a designer cannot use the specified data sheet maximum for propagation delay time when using the flip-flop as a data synchronizer — how long to wait after the specified data sheet maximum must be known before using the data in order to guarantee reliable system operation.

The circuit shown in Figure 2 can be used to evaluate MTBF (Mean Time Between Failure) and Δt for a selected flip-flop. Whenever the Q output of the DUT is between 0.8 V and 2 V, the comparators are in opposite states. When the Q output of the DUT is higher than 2 V or lower than 0.8 V, the comparators are at the same logic level. The outputs of the two comparators are sampled a selected time (Δt) after SCLK. The exclusive OR gate detects the occurrence of a failure and increments the failure counter.

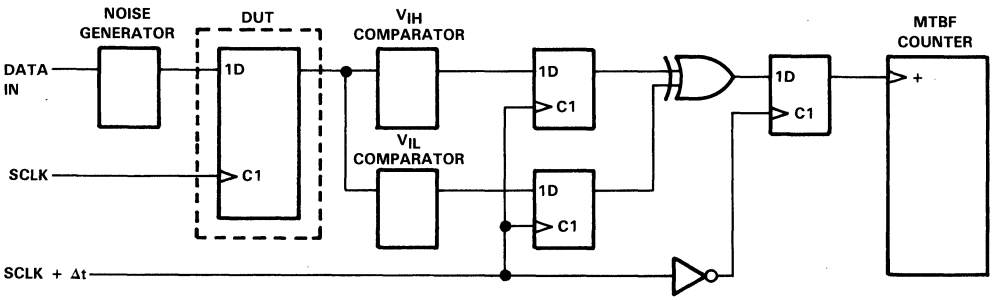
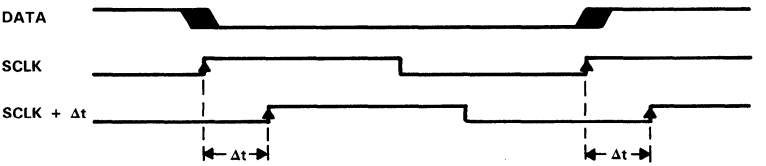


FIGURE 2. METASTABLE EVALUATION TEST CIRCUIT

In order to maximize the possibility of forcing the DUT into a metastable state, the input data signal is applied so that it always violates the setup and hold time. This condition is illustrated in the timing diagram in Figure 3. Any other relationship of SCLK to data will provide less chance for the device to enter into the metastable state.



$$MTBF = \frac{\text{TIME (SEC)}}{\text{\# FAILURES}}$$

t_{rec} = Δt − CLK TO Q (MAX)

FIGURE 3. TIMING DIAGRAM

By using the described test circuit, MTBF can be determined for several different values of Δt (see Figure 2). Plotting this information on semilog paper demonstrates the metastable characteristics of the selected flip-flop. Figure 4 shows the results for the TIBPAL16'-10 operating at 1 MHz.

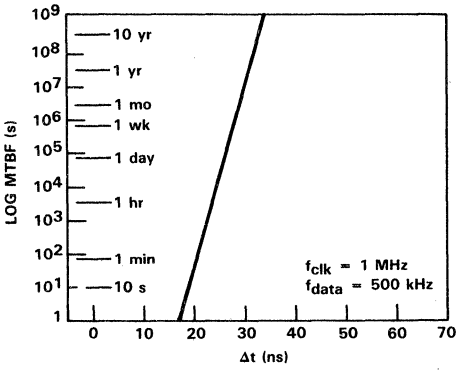


FIGURE 4. METASTABLE CHARACTERISTICS

From the data taken in the above experiment, an equation can be derived for the metastable characteristics at other clock frequencies.

The metastable equation: $\frac{1}{MTBF} = f_{SCLK} \times f_{data} \times C1\ e^{(-C2 \times \Delta t)}$

The constants C1 and C2 describe the metastable characteristics of the device. From the experimental data, these constants can be solved for: $C1 = 9.15 \times 10^{-7}$ and $C2 = 0.959$

Therefore

$$\frac{1}{MTBF} = f_{SCLK} \times f_{data} \times 9.159 \times 10^{-7}\ e^{(-0.959 \times \Delta t)}$$

definition of variables

DUT (Device Under Test): The DUT is a 10-ns registered PAL programmed with the equation Q := D.

MTBF (Mean Time Between Failures): The average time (s) between metastable occurrences that cause a violation of the device specifications.

f_{SCLK} (system clock frequency): Actual clock frequency for the DUT.

f_{data} (data frequency): Actual data frequency for a specified input to the DUT.

C1: Calculated constant that defines the magnitude of the curve.

C2: Calculated constant that defines the slope of the curve.

t_{rec} (metastability recovery time): Minimum time required to guarantee recovery from metastability, at a given MTBF failure rate. $t_{rec} = \Delta t - t_{pd}$ (CLK to Q, max)

Δt: The time difference (ns) from when the synchronizing flip-flop is clocked to when its output is sampled.

The test described above has shown the metastable characteristics of the TIBPAL16R4/R6/R8-10 series. For additional information on metastable characteristics of Texas Instruments logic circuits, please refer to TI Applications publication #SDAA004, "Metastable Characteristics, Design Considerations for ALS, AS, and LS Circuits."

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

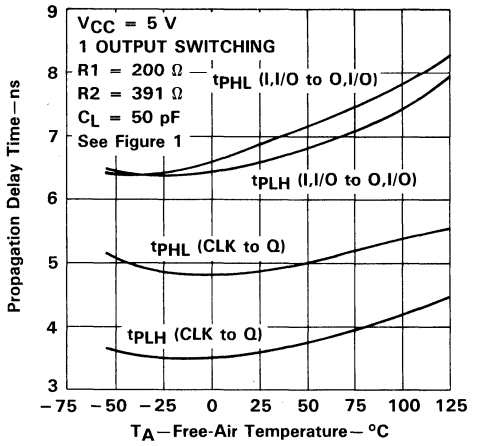


FIGURE 5

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

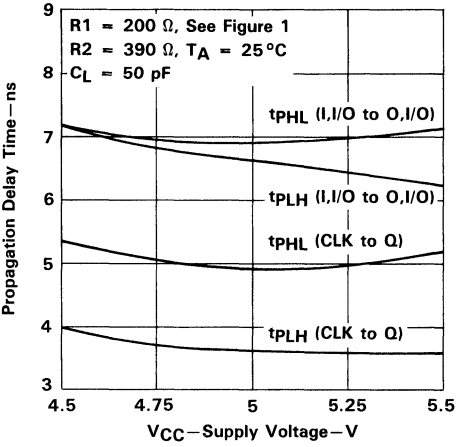


FIGURE 6

PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

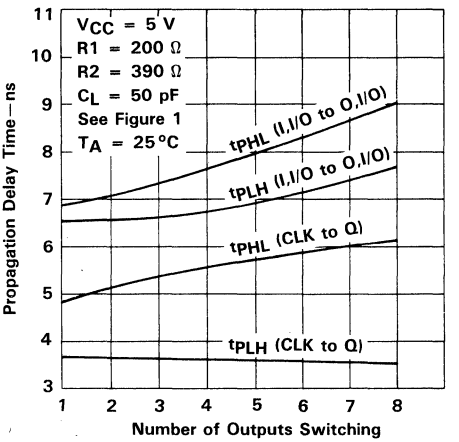


FIGURE 7

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

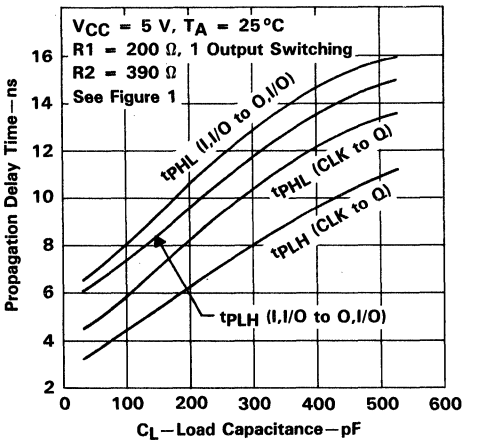


FIGURE 8

POWER DISSIPATION
vs
FREQUENCY
8-BIT COUNTER MODE

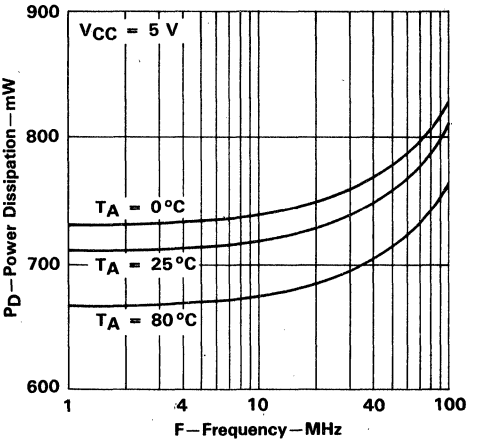


FIGURE 9

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

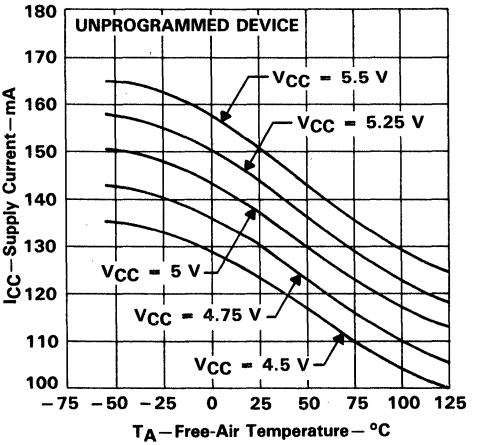


FIGURE 10

TEXAS INSTRUMENTS
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- **High-Performance Operation**
  Propagation Delay
  M Suffix . . . 12 ns Max
  C Suffix . . . 15 ns Max
- **Functionally Equivalent, but Faster than PAL16L8B, PAL16R4B, PAL16R6B, and PAL16R8B**
- **Power-Up Clear on Registered Devices (All Registered Outputs are Set Low)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

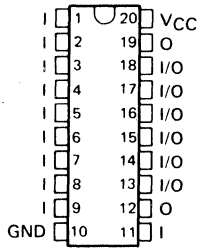
DEVICE	INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state)	4
PAL16R6	8	0	6 (3-state)	2
PAL16R8	8	0	8 (3-state)	0

description

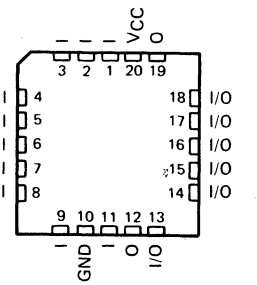
These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of "custom" functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

The TIBPAL16' M series is characterized for operation over the full military temperature range of −55°C to 125°C. The TIBPAL16' C series is characterized for operation from 0°C to 75°C.

TIBPAL16L8'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16L8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode

IMPACT™ is a trademark of Texas Instruments Incorporated.
PAL® is a registered trademark of Monolithic Memories Inc.
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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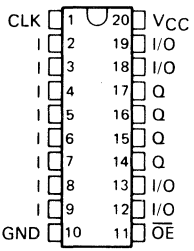
TIBPAL16R4'
M SUFFIX . . . J PACKAGE
C SUFFIX. . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16R4'
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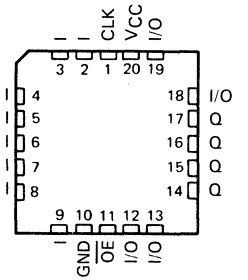
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



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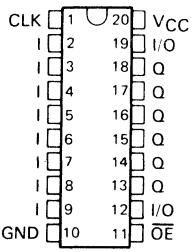
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



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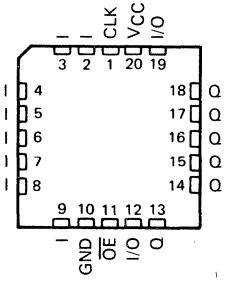
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



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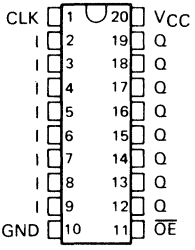
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16R8'
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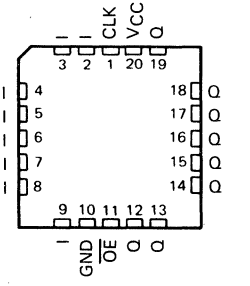
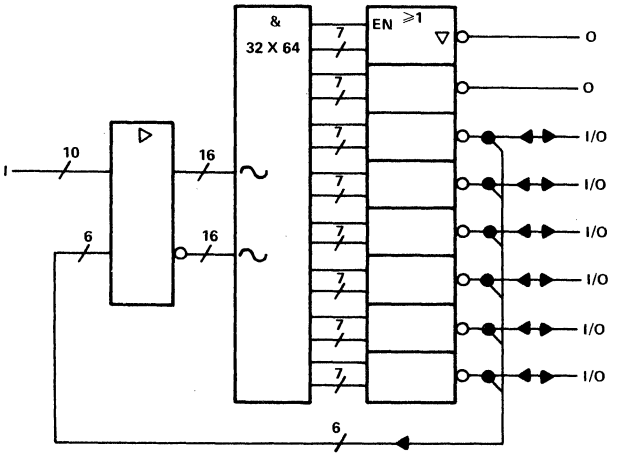
C SUFFIX. . . FN PACKAGE
(TOP VIEW)



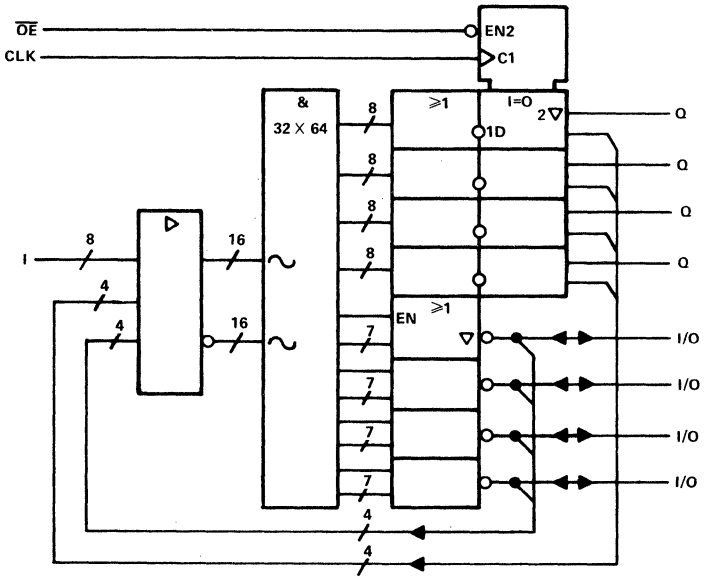
Pin assignments in operating mode

functional block diagrams (positive logic)

'PAL16L8



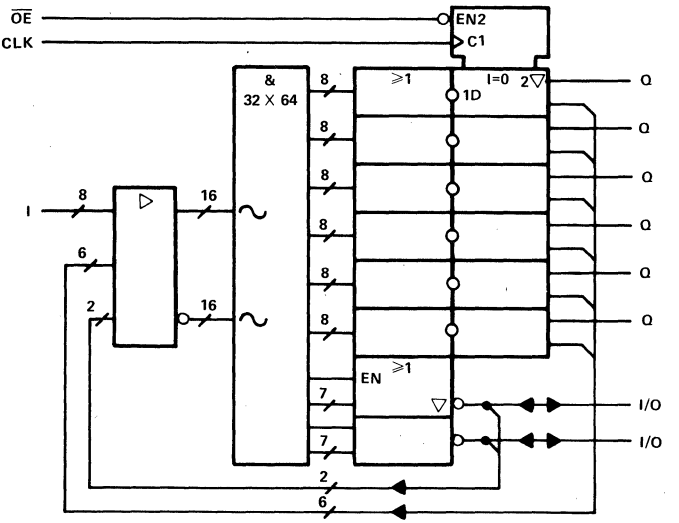
'PAL16R4



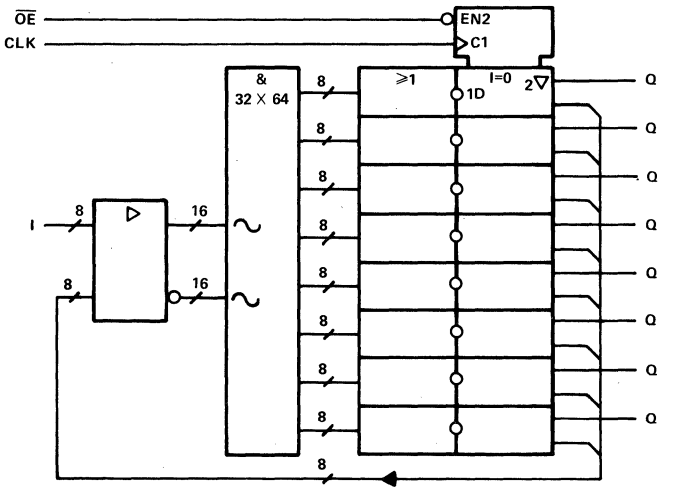
∼ denotes fused inputs

functional block diagrams (positive logic)

'PAL16R6



'PAL16R8



~ denotes fused inputs

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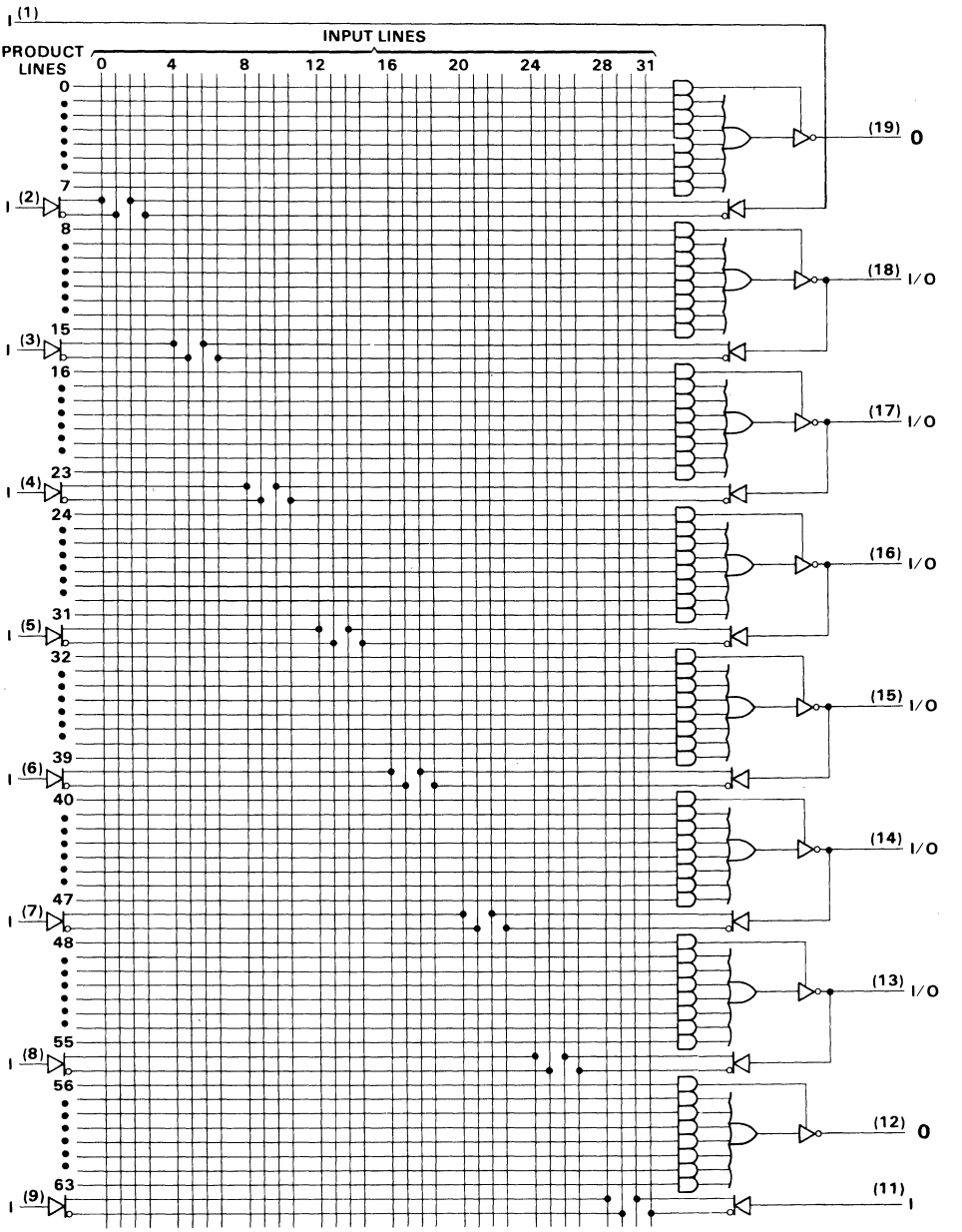
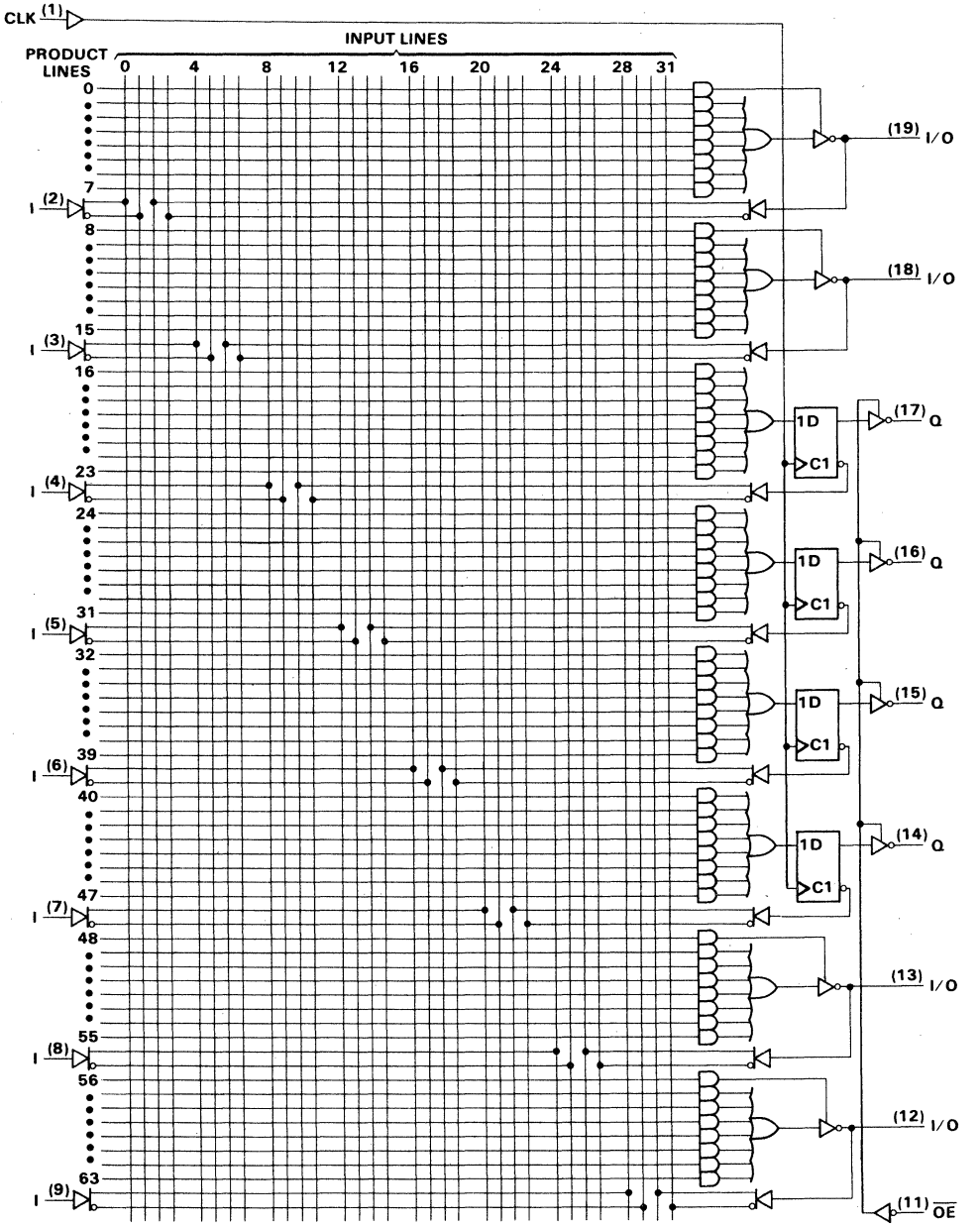

INPUT LINES
PRODUCT LINES
0
4
8
12
16
20
24
28
31
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(19) O
(18) I/O
(17) I/O
(16) I/O
(15) I/O
(14) I/O
(13) I/O
(12) O
(11) I



TEXAS INSTRUMENTS
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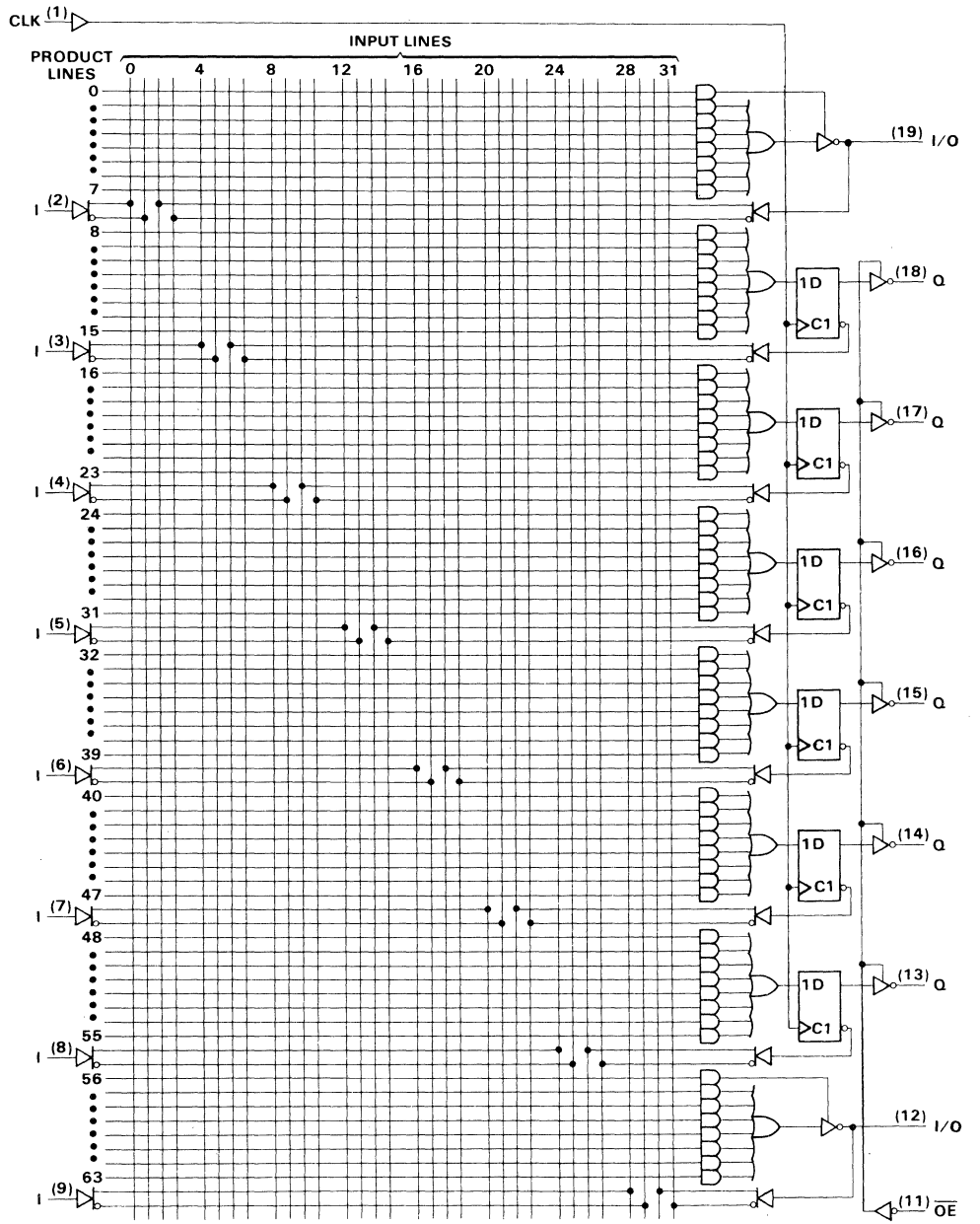
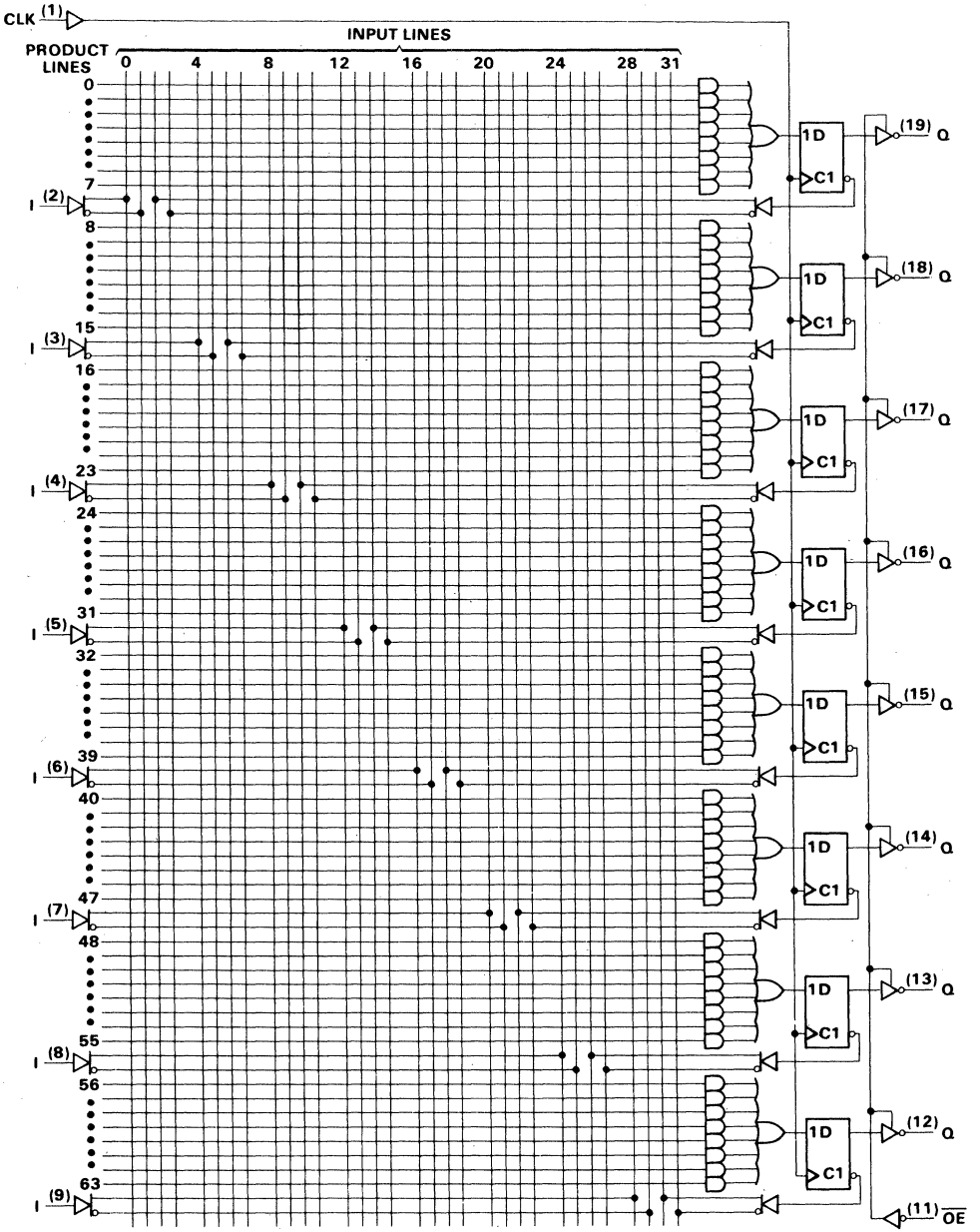

CLK (1)
INPUT LINES
PRODUCT LINES
0 4 8 12 16 20 24 28 31
0
7
8
15
16
23
24
31
32
39
40
47
48
55
56
63
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(19) I/O
(18) Q
(17) Q
(16) Q
(15) Q
(14) Q
(13) Q
(12) I/O
(11) OE
1D
C1


CLK (1)
INPUT LINES
PRODUCT LINES
0 4 8 12 16 20 24 28 31
0
7
8
15
16
23
24
31
32
39
40
47
48
55
56
63
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
1D
C1
(19) Q
(18) Q
(17) Q
(16) Q
(15) Q
(14) Q
(13) Q
(12) Q
(11) OE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions (see Note 2)

PARAMETER			−15M			−12C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		50	0		62	MHz
t_w	Pulse duration, clock (see Note2)	High	9			7			ns
		Low	10			8			
t_{su}	Setup time, input or feedback before CLK↑		15			10			ns
t_h	Hold time, input or feedback after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		75	°C

NOTE 2: The total clock period of CLK high and CLK low must not exceed clock frequency, f_{clock}. Minimum pulse durations specified are only for CLK high or CLK low, but not for both simultaneously.

electrical characteristics, over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS†			−15M			−12C			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX		2.4	3.3		2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX			0.35	0.5		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX,	V_O = 2.7 V				20			20	μA
	I/O ports						100			100	
I_{OZL}	Outputs	V_{CC} = MAX,	V_O = 0.4 V				−20			−20	μA
	I/O ports						−250			−250	
I_I		V_{CC} = MAX,	V_I = 5.5 V	Pin 1, 11			0.2			0.1	mA
				All others			0.1			0.1	
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V	Pin 1, 11			50			20	μA
				All others			20			20	
I_{IL}		V_{CC} = MAX,	V_I = 0.4 V				−0.2			−0.2	mA
I_O§		V_{CC} = MAX,	V_O = 2.25 V		−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, V_I = 0 V,	Outputs Open			170	220		170	200	mA

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	–15M			–12C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}‡			R_L = 500 Ω, C_L = 50 pF See Note 3	50			62			MHz
t_{pd}‡	I, I/O	O, I/O			8	15		8	12	ns
t_{pd}	CLK↑	Q			7	12		7	10	ns
t_{en}	OE↓	Q			8	12		8	10	ns
t_{dis}	OE↑	Q			7	12		7	10	ns
t_{en}	I, I/O	O, I/O			8	15		8	12	ns
t_{dis}	I, I/O	O, I/O			8	15		8	12	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Maximum operating frequency and propagation delay are specified for the basic building block. When using feedback, limits must be calculated accordingly.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

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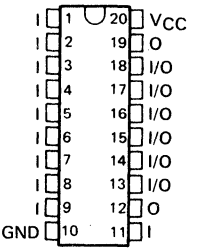
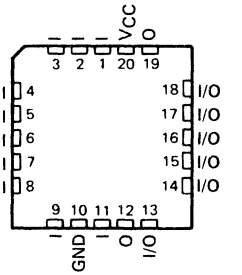
- **High-Performance Operation**
  Propagation Delay
  M Suffix . . . 20 ns Max
  C Suffix . . . 15 ns Max
- **Functionally Equivalent, but Faster than PAL16L8A, PAL16R4A, PAL16R6A, and PAL16R8A**
- **Power-Up Clear on Registered Devices (All Registered Outputs are Set Low)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

DEVICE	INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state)	4
PAL16R6	8	0	6 (3-state)	2
PAL16R8	8	0	8 (3-state)	0

TIBPAL16L8'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16L8'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



description

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The PAL16' M series is characterized for operation over the full military temperature range of −55°C to 125°C. The PAL16' C series is characterized for operation from 0°C to 70°C.

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.
IMPACT is a trademark of Texas Instruments Incorporated.

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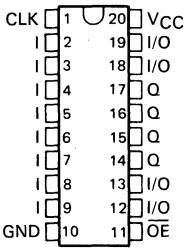
TIBPAL16R4'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16R4'
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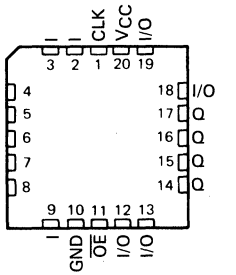
(TOP VIEW)



TIBPAL16R6'
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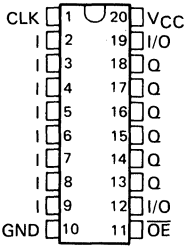
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16R4'
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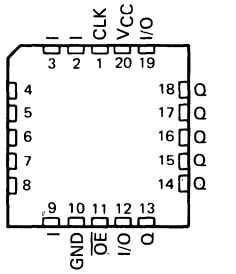
(TOP VIEW)



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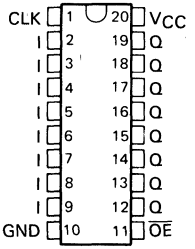
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16R8'
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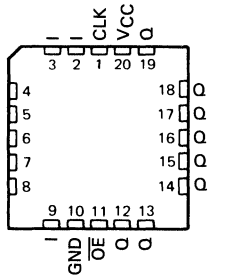
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



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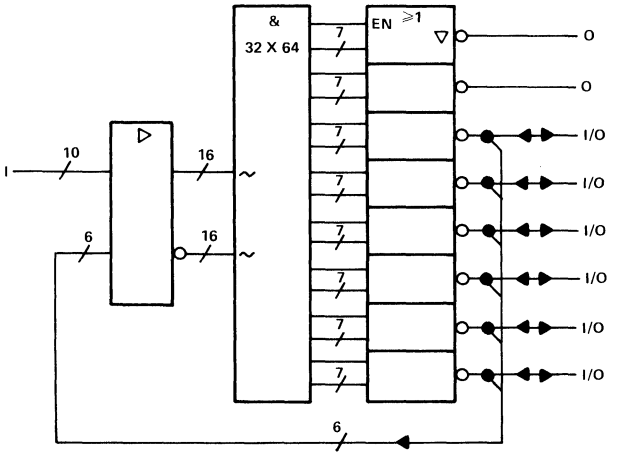
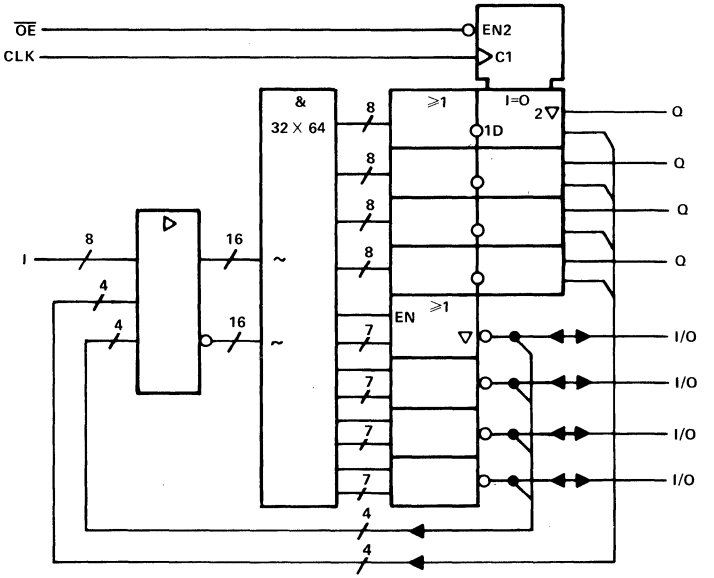
functional block diagrams (positive logic)

'PAL16L8



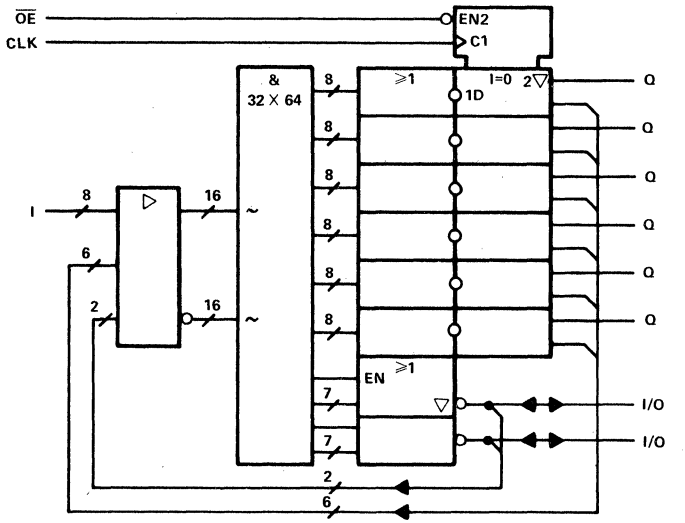
'PAL16R4



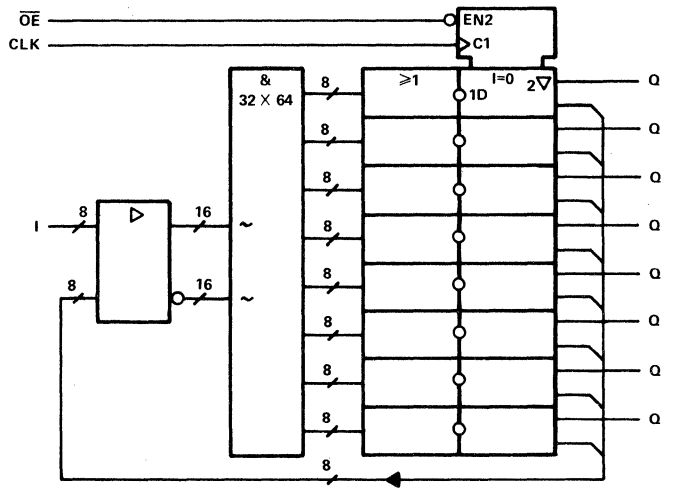
~ denotes fused inputs

functional block diagrams (positive logic)

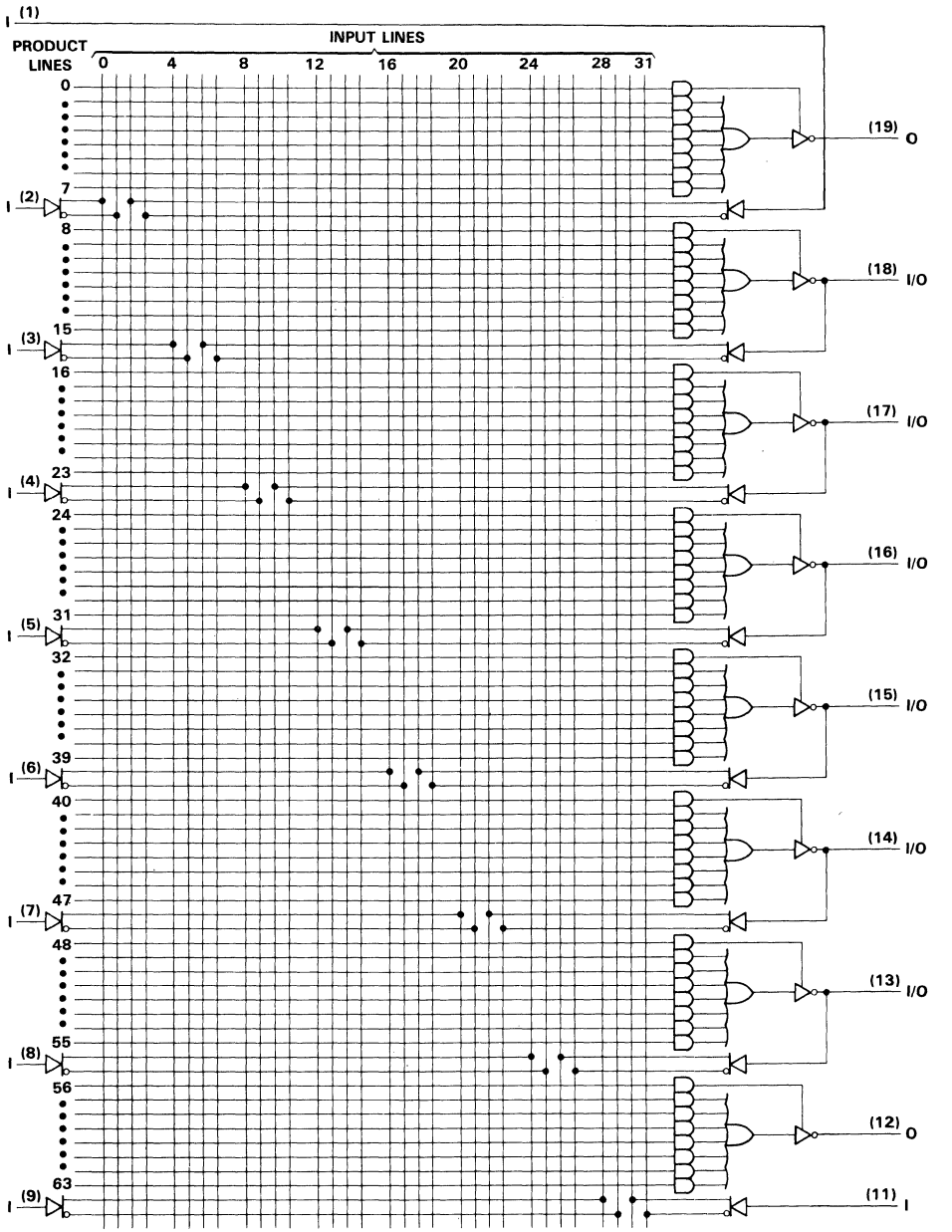
'PAL16R6

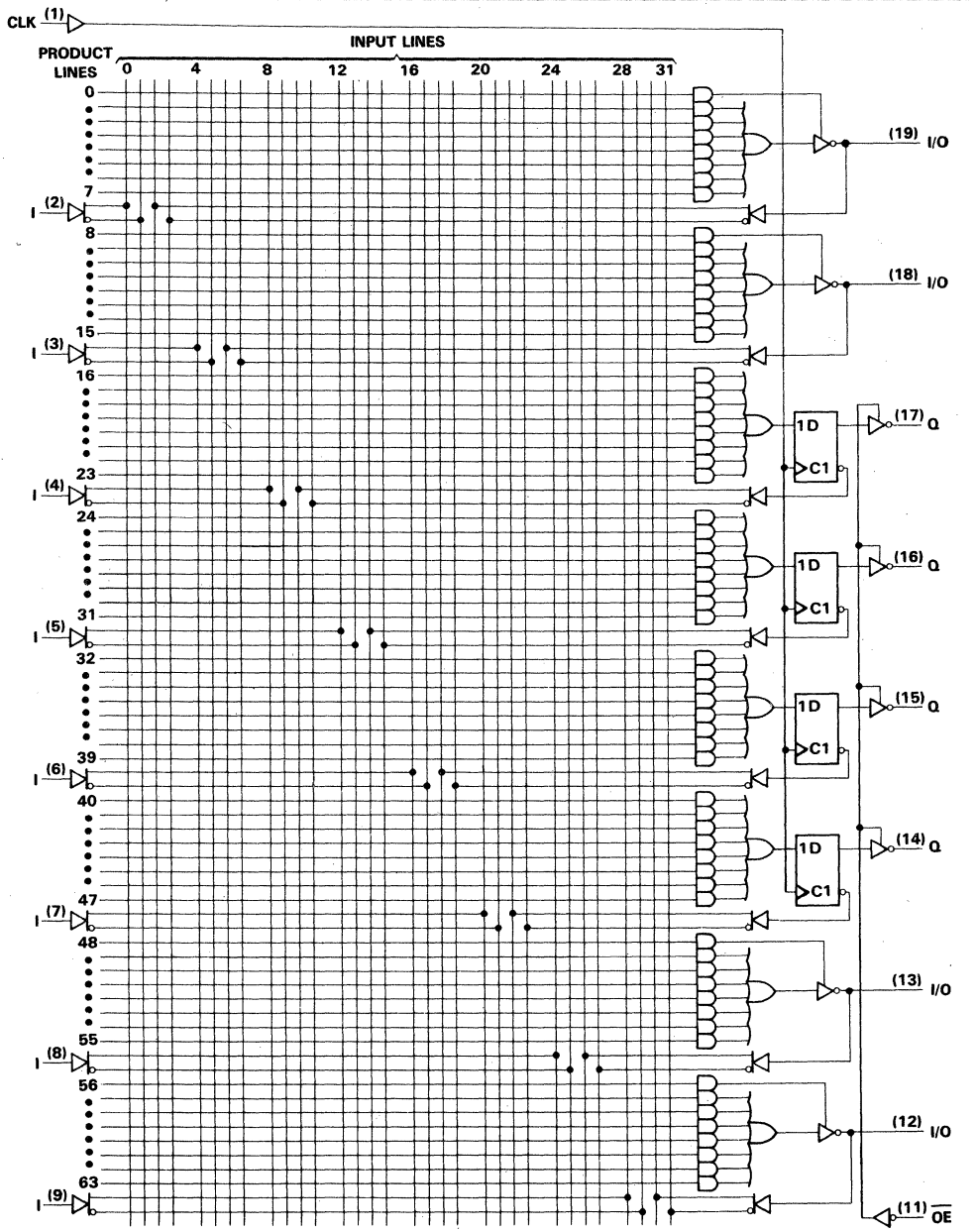


'PAL16R8



~ denotes fused inputs


INPUT LINES
0
4
8
12
16
20
24
28
31
PRODUCT LINES
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(19) O
(18) I/O
(17) I/O
(16) I/O
(15) I/O
(14) I/O
(13) I/O
(12) O
(11) I



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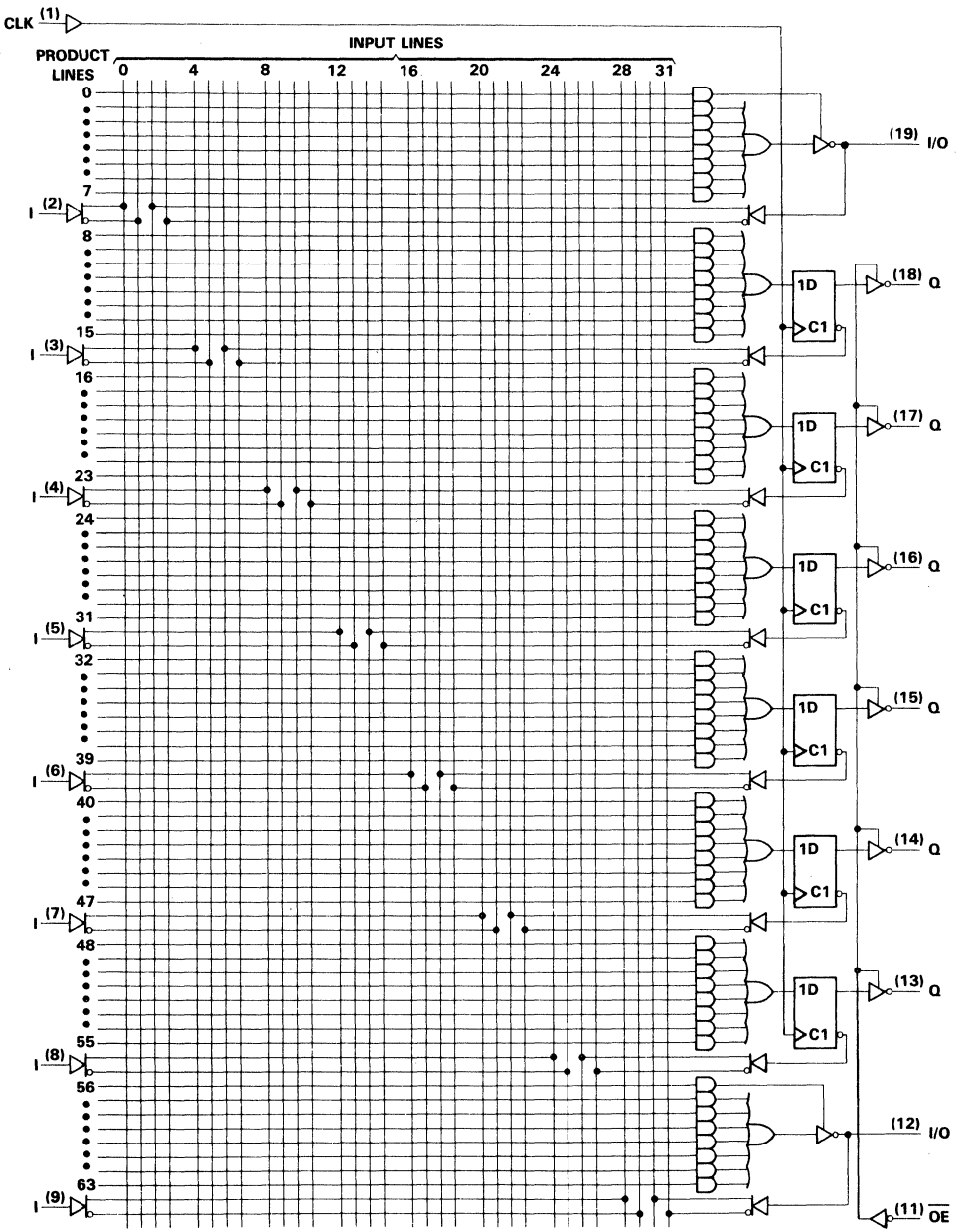
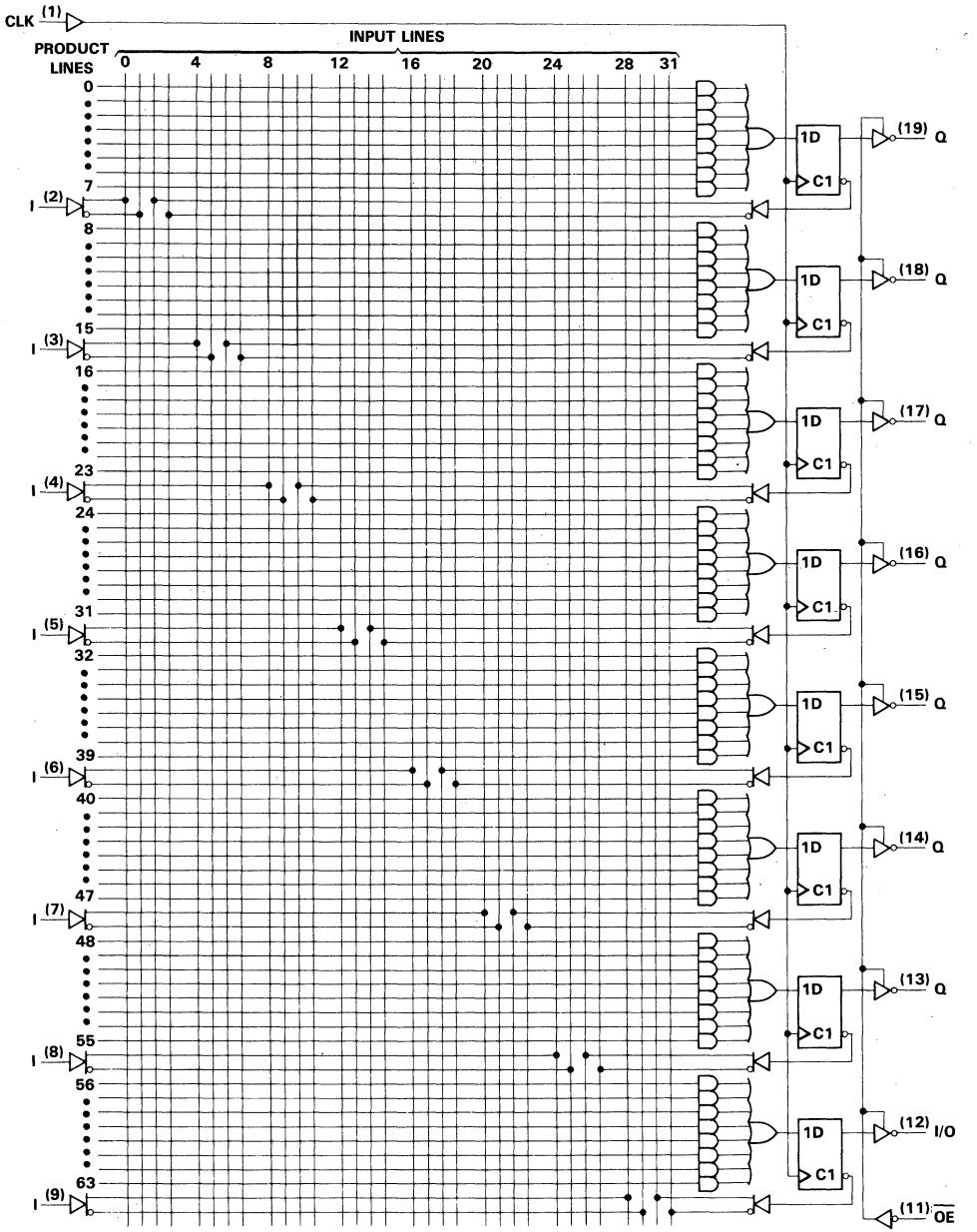

CLK (1)
INPUT LINES
PRODUCT LINES
0 4 8 12 16 20 24 28 31
0
7
I (2)
8
15
I (3)
16
23
I (4)
24
31
I (5)
32
39
I (6)
40
47
I (7)
48
55
I (8)
56
63
I (9)
(19) I/O
(18) Q
(17) Q
(16) Q
(15) Q
(14) Q
(13) Q
(12) I/O
(11) OE
1D
C1



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			20M			15C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		40	0		50	MHz
t_w	Pulse duration, clock (see Note 2)	High	10			8			ns
		Low	11			9			
t_{su}	Setup time, input or feedback before CLK↑		20			15			ns
t_h	Hold time, input or feedback after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTE: 2. The total clock period of CLK high and CLK low must not exceed clock frequency, f_{clock}. Minimum pulse durations specified are only for CLK high or CLK low, but not for both simultaneously.

programming information

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electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS†			20M			15C			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX		2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX			0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX,	V_O = 2.7 V				20			20	μA
	I/O ports						100			100	
I_{OZL}	Outputs	V_{CC} = MAX,	V_O = 0.4 V				−20			−20	μA
	I/O ports						−250			−250	
I_I		V_{CC} = MAX,	V_I = 5.5 V	Pin 1, 11			0.2			0.1	mA
				All others			0.1			0.1	
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V	Pin 1, 11			50			20	μA
				All others			20			20	
I_{IL}		V_{CC} = MAX,	V_I = 0.4 V				−0.2			−0.2	mA
I_O§		V_{CC} = MAX,	V_O = 2.25 V		−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, V_I = 0 V	Outputs Open			140	190		140	180	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	20M			15C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}				40			50			MHz
t_{pd}	I, I/O	O, I/O			10	20		10	15	ns
t_{pd}	CLK↑	Q	R_L = 500 Ω,		8	15		8	12	ns
t_{en}	OE↓	Q	C_L = 50 pF,		8	15		8	12	ns
t_{dis}	OE↑	Q	See Note 3		7	15		7	10	ns
t_{en}	I, I/O	O, I/O			10	20		10	15	ns
t_{dis}	I, I/O	O, I/O			10	20		10	15	ns

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- **High-Performance Operation**
  Propagation Delay
  M Suffix . . . 20 ns Max
  C Suffix . . . 15 ns Max
- **Functionally Equivalent, but Faster than PAL16L8A, PAL16R4A, PAL16R6A, and PAL16R8A**
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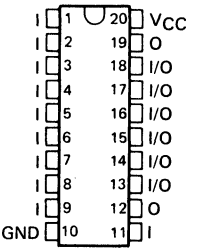
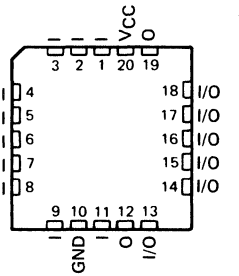
PAL16R6	8	0	6 (3-state)	2
PAL16R8	8	0	8 (3-state)	0

TIBPAL16L8'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16L8'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



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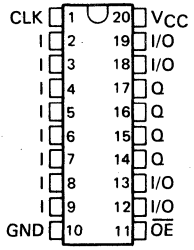
TIBPAL16R4'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16R4'
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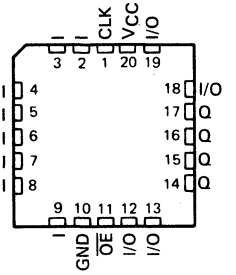
(TOP VIEW)



TIBPAL16R6'
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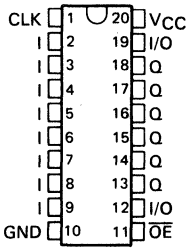
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16R4'
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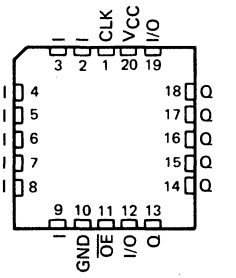
(TOP VIEW)



TIBPAL16R8'
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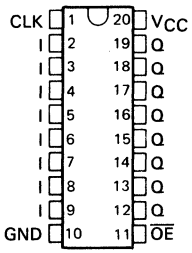
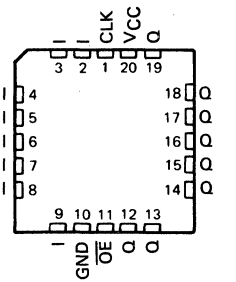
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16R8'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



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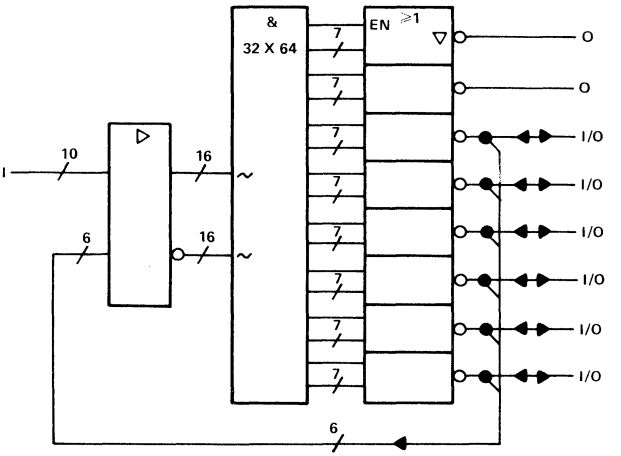
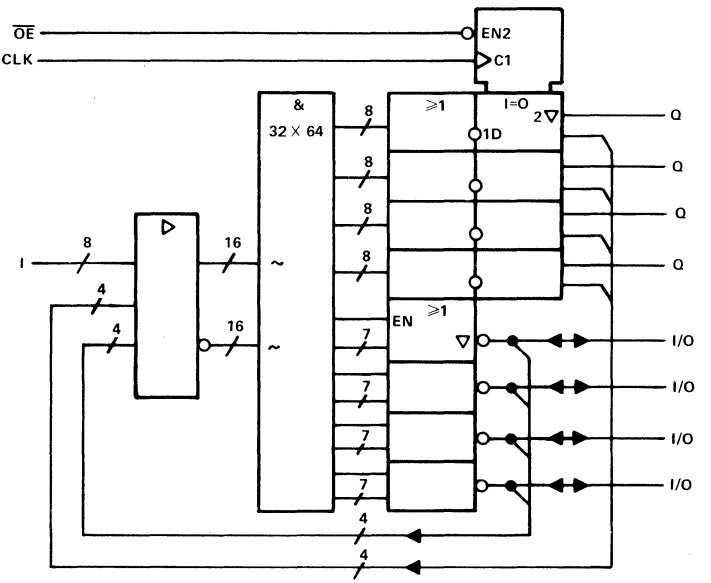
functional block diagrams (positive logic)

'PAL16L8



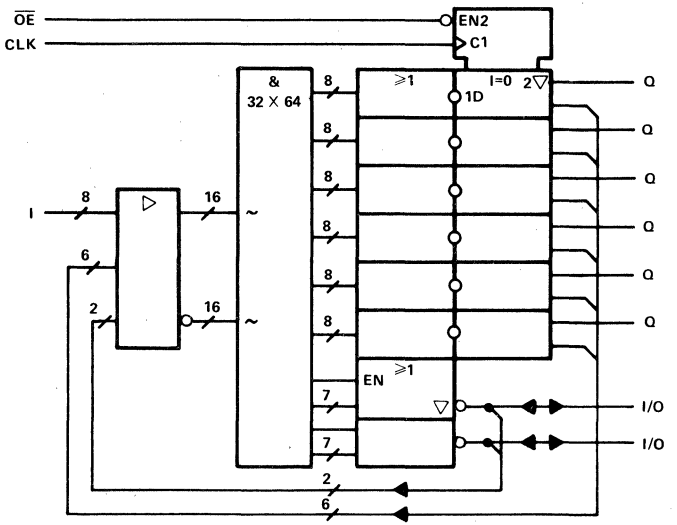
'PAL16R4



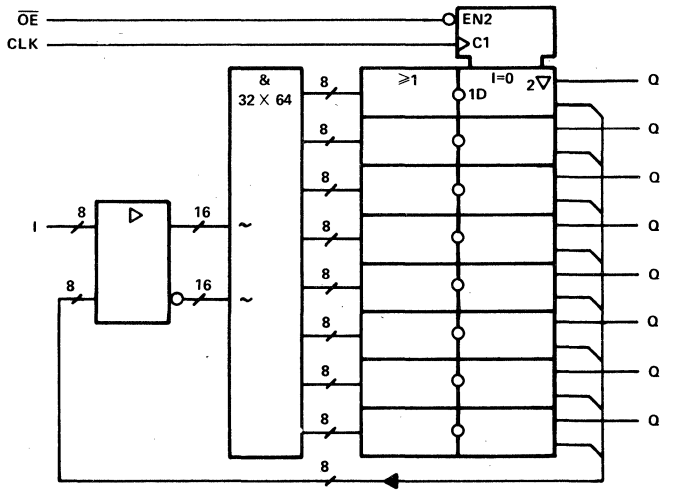
~ denotes fused inputs

functional block diagrams (positive logic)

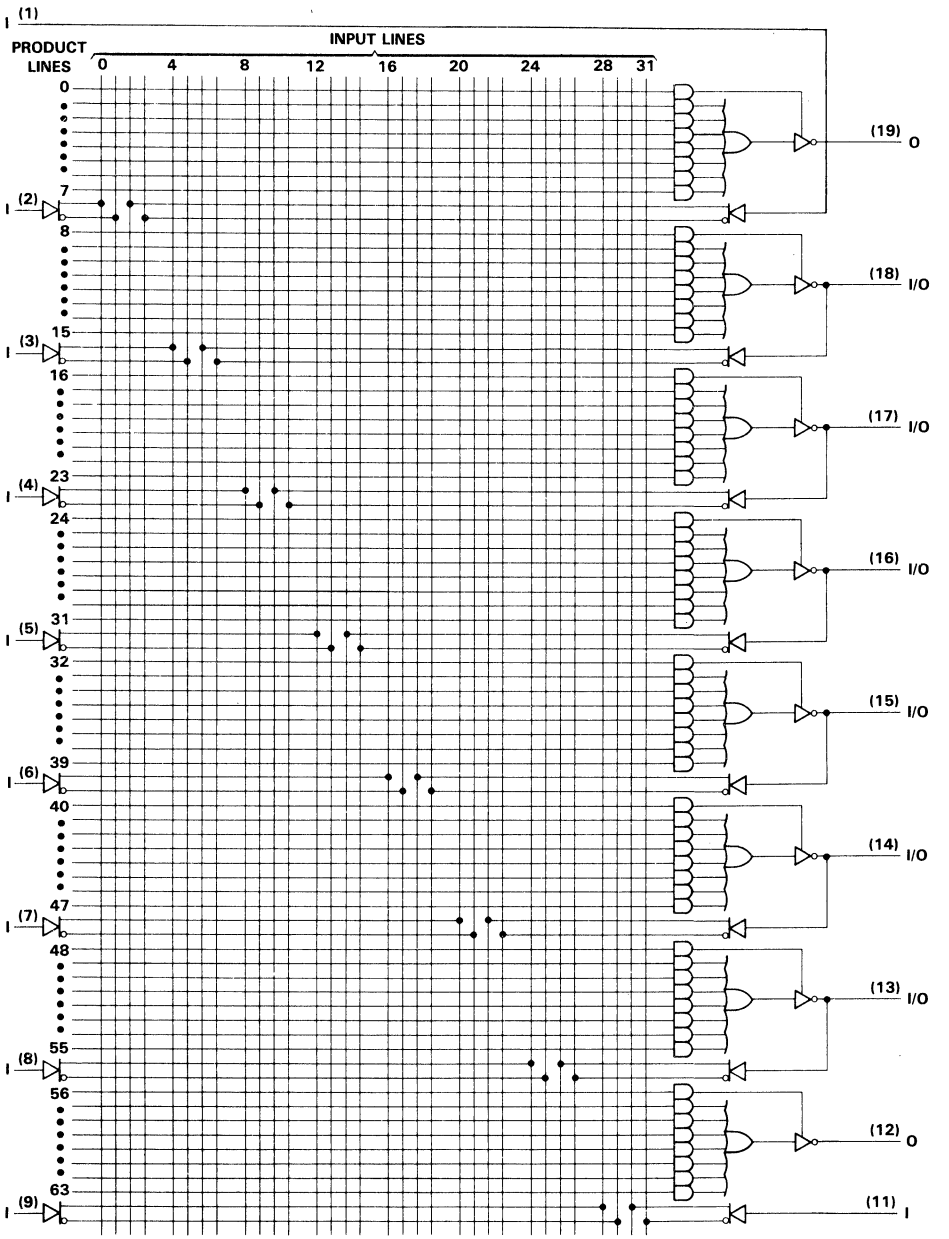
'PAL16R6

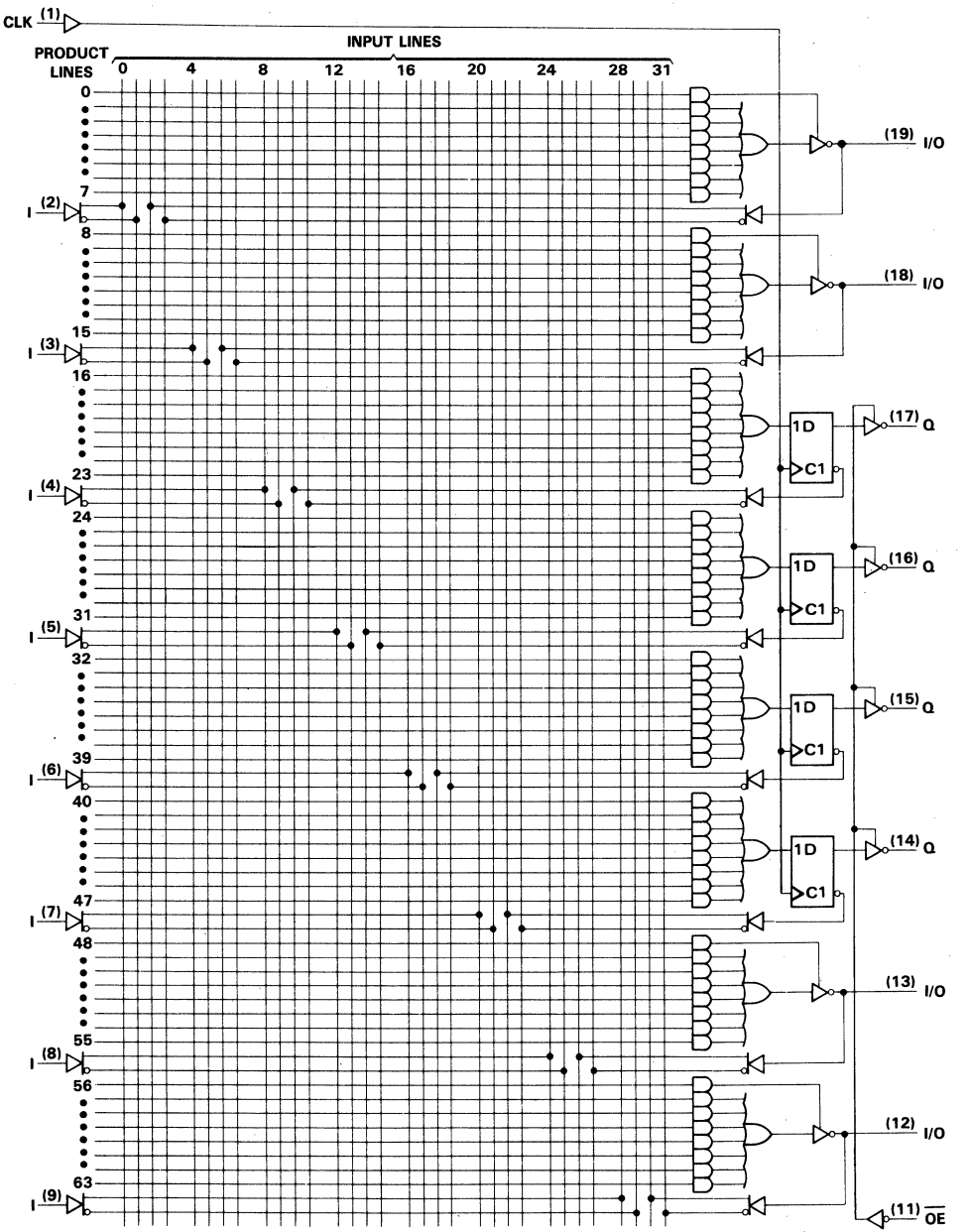


'PAL16R8



~ denotes fused inputs


(1)
INPUT LINES
PRODUCT LINES
0
4
8
12
16
20
24
28
31
0
7
8
15
16
23
24
31
32
39
40
47
48
55
56
63
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(19) O
(18) I/O
(17) I/O
(16) I/O
(15) I/O
(14) I/O
(13) I/O
(12) O
(11) I



TEXAS INSTRUMENTS
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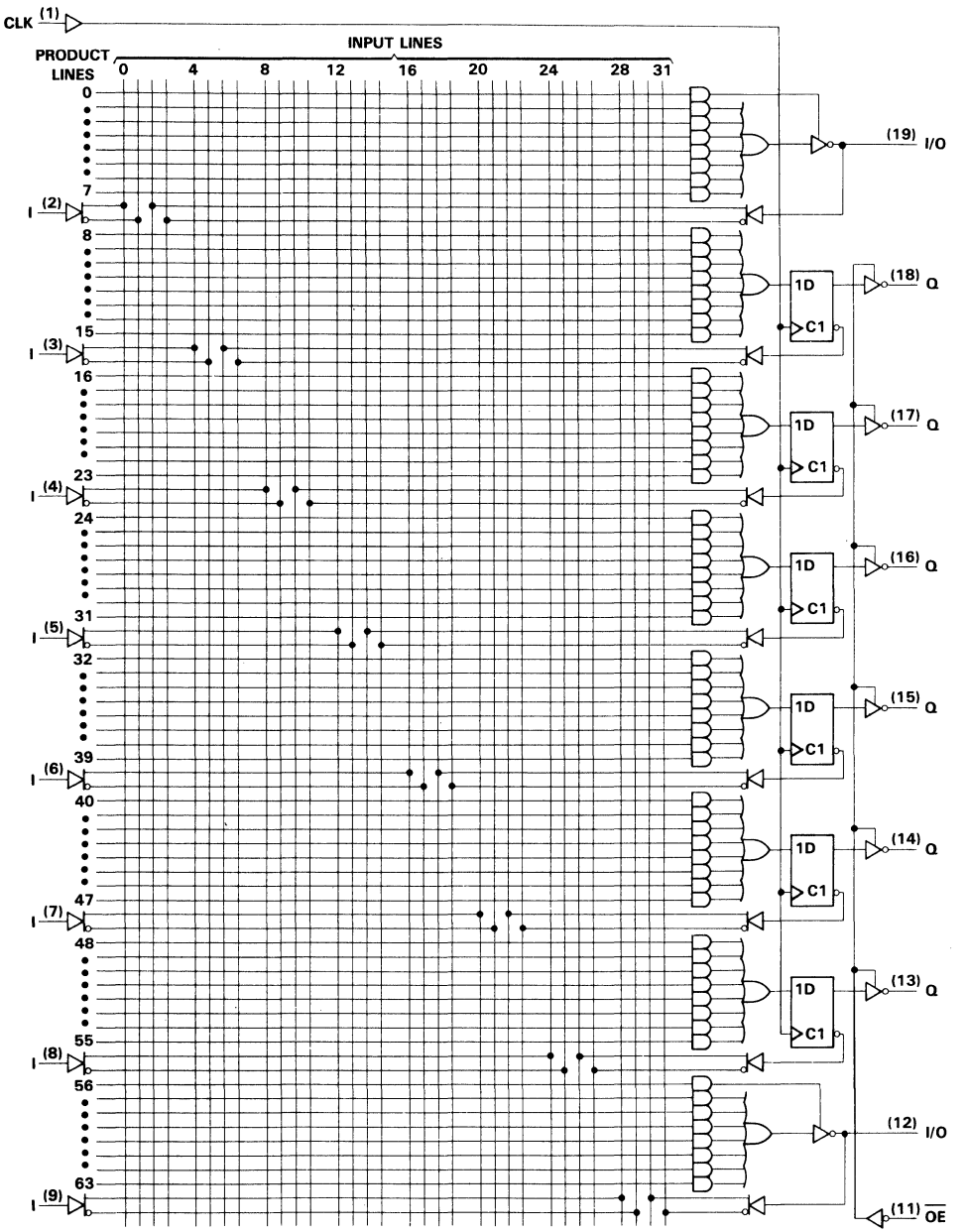
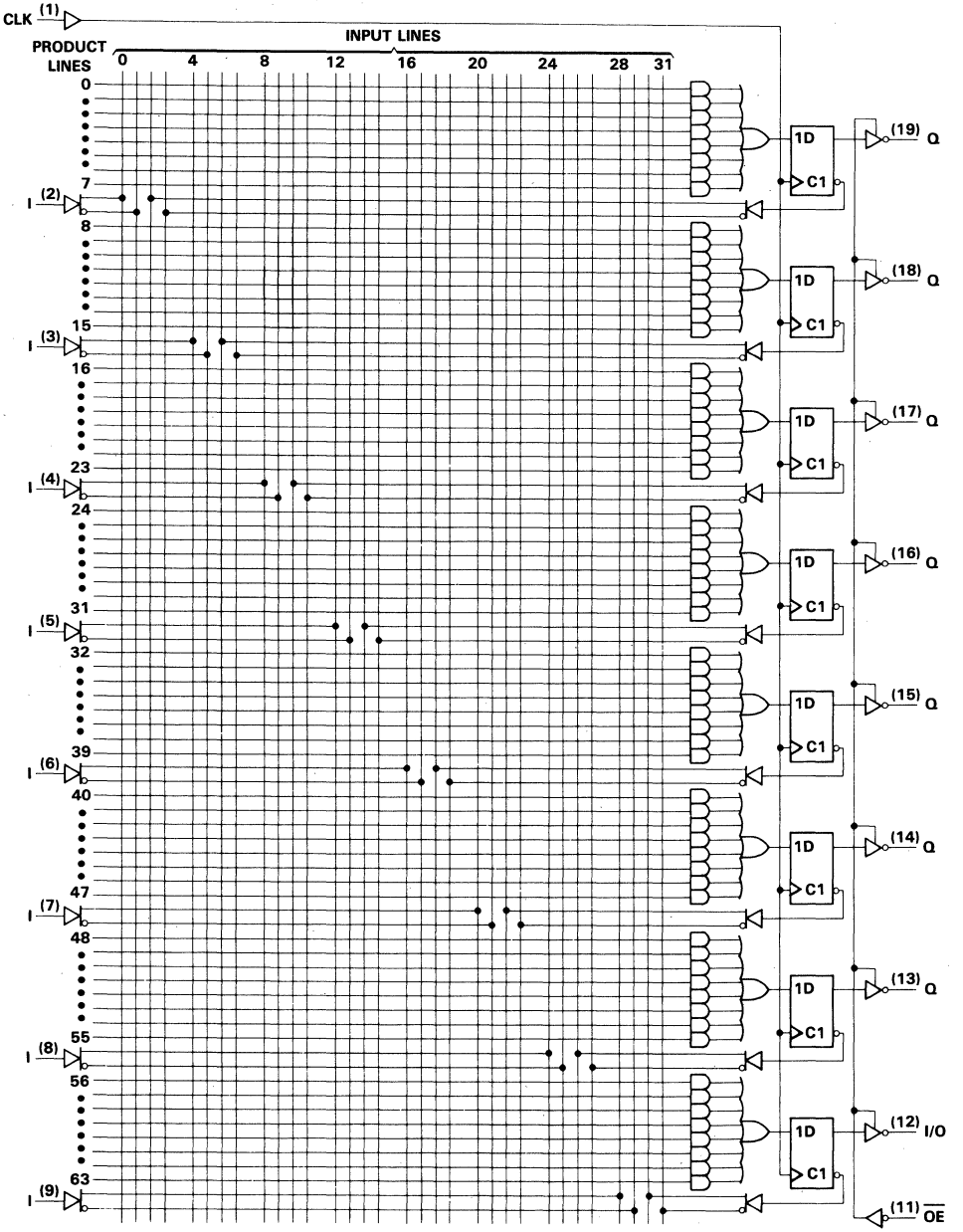

CLK (1)
INPUT LINES
PRODUCT LINES
0 4 8 12 16 20 24 28 31
0
7
I (2)
8
15
I (3)
16
23
I (4)
24
31
I (5)
32
39
I (6)
40
47
I (7)
48
55
I (8)
56
63
I (9)
(19) I/O
(18) Q
(17) Q
(16) Q
(15) Q
(14) Q
(13) Q
(12) I/O
(11) OE
1D
C1



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			30M			25C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		40	0		50	MHz
t_w	Pulse duration, clock (see Note 2)	High	10			8			ns
		Low	11			9			
t_{su}	Setup time, input or feedback before CLK↑		20			15			ns
t_h	Hold time, input or feedback after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTE: 2. The total clock period of CLK high and CLK low must not exceed clock frequency, f_{clock}. Minimum pulse durations specified are only for CLK high or CLK low, but not for both simultaneously.

programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 995-5762.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS†		-30M			-25C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = MAX		2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN, I_{OL} = MAX			0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX, V_O = 2.7 V				20			20	μA
	I/O ports					100			100	
I_{OZL}	Outputs	V_{CC} = MAX, V_O = 0.4 V				−20			−20	μA
	I/O ports					−250			−250	
I_I		V_{CC} = MAX, V_I = 5.5 V	Pin 1, 11			0.2			0.1	mA
			All others			0.1			0.1	
I_{IH}		V_{CC} = MAX, V_I = 2.7 V	Pin 1, 11			50			20	μA
			All others			20			20	
I_{IL}		V_{CC} = MAX, V_I = 0.4 V				−0.2			−0.2	mA
I_O§		V_{CC} = MAX, V_O = 2.25 V		−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, V_I = 0 V, Outputs Open			75	105		75	100	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	-30M			-25C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}			R_L = 500 Ω, C_L = 50 pF, See Note 3	25			30			MHz
t_{pd}	I, I/O	O, I/O			15	30		15	25	ns
t_{pd}	CLK↑	Q			10	20		10	15	ns
t_{en}	OE↓	Q			15	25		15	20	ns
t_{dis}	OE↑	Q			10	25		10	20	ns
t_{en}	I, I/O	O, I/O			14	30		14	25	ns
t_{dis}	I, I/O	O, I/O			13	30		13	25	ns

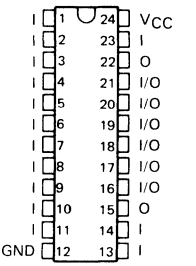
‡All typical values are at V_{CC} = 5 V, T_A 25°C.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

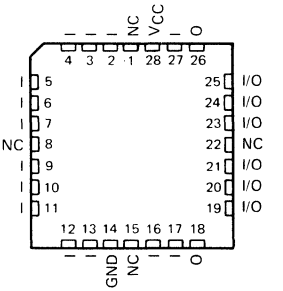
- **High Performance: f_{max} (w/o feedback)**
  TIBPAL20R' C series . . . 45 MHz
  TIBPAL20R' M series . . . 41.5 MHz
- **High Performance . . . 45 MHz Min**
- **Functionally Equivalent to, but Faster than, PAL20L8, PAL20R4, PAL20R6, PAL20R8**
- **Preload Capability on Output Registers Simplifies Testing**
- **Package Options Include Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Reduced I_{CC} of 180 mA Max**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PAL20L8	14	2	0	6
'PAL20R4	12	0	4 (3-state buffers)	4
'PAL20R6	12	0	6 (3-state buffers)	2
'PAL20R8	12	0	8 (3-state buffers)	0

TIBPAL20L8'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20L8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses to provide reliable, high performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are also available for further reduction in board space.

Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL20'M series is characterized for operation over the full military temperature range of −55°C to 125°C. The TIBPAL20'C is characterized from 0°C to 75°C.

IMPACT is a trademark of Texas Instruments Incorporated
PAL is a registered trademark of Monolithic Memories Inc.
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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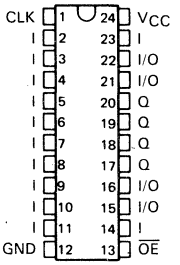
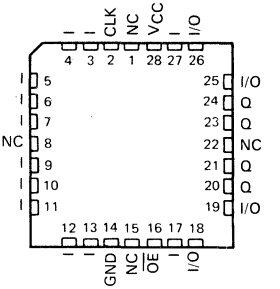
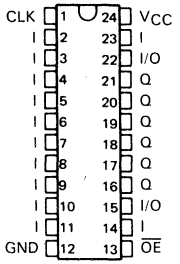
TIBPAL20R4'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



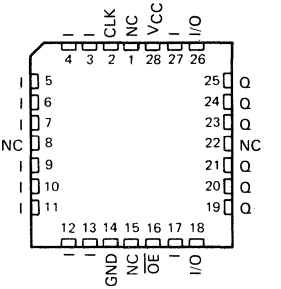
TIBPAL20R4'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



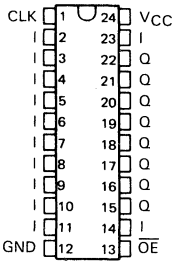
TIBPAL20R6'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



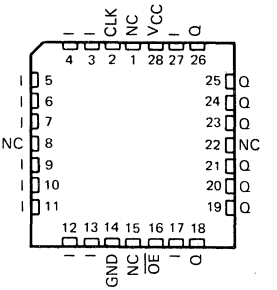
TIBPAL20R6'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL20R8'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20R8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)

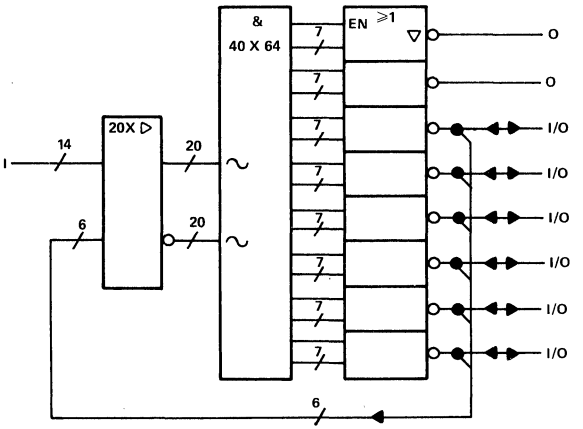


Pin assignments in operating mode

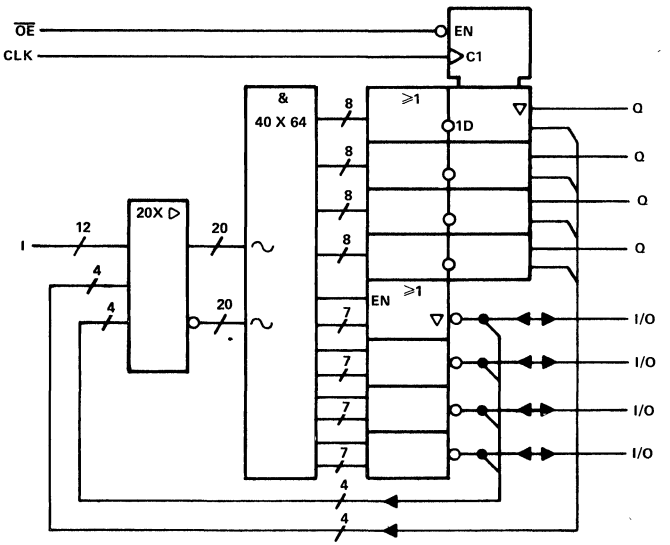
NC—No internal connection

functional block diagrams (positive logic)

TIBPAL20L8'



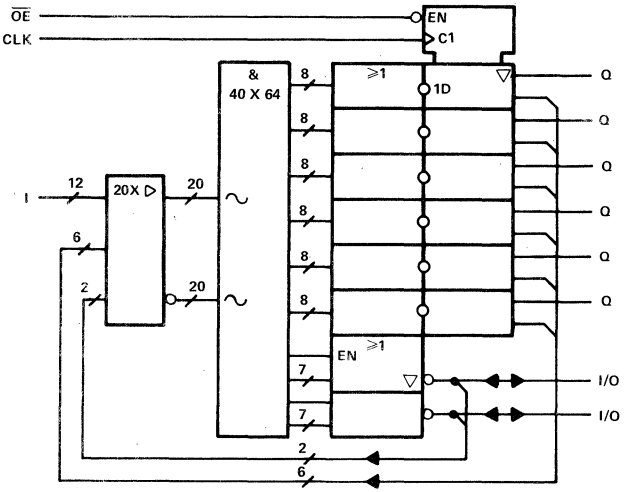
TIBPAL20R4'



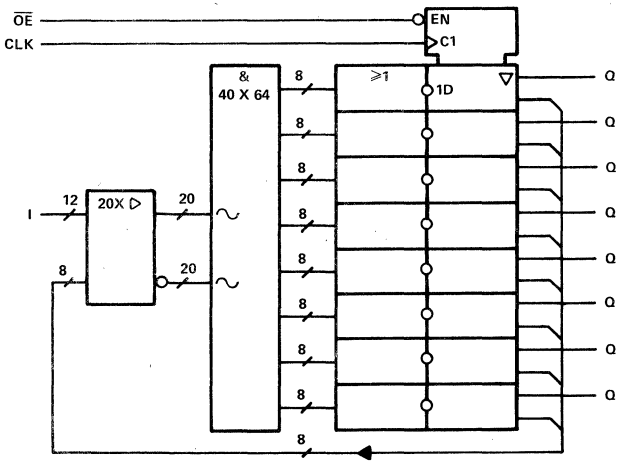
∼ denotes fused inputs

functional block diagrams (positive logic)

TIBPAL20R6'



TIBPAL20R8'



∿ denotes fused inputs

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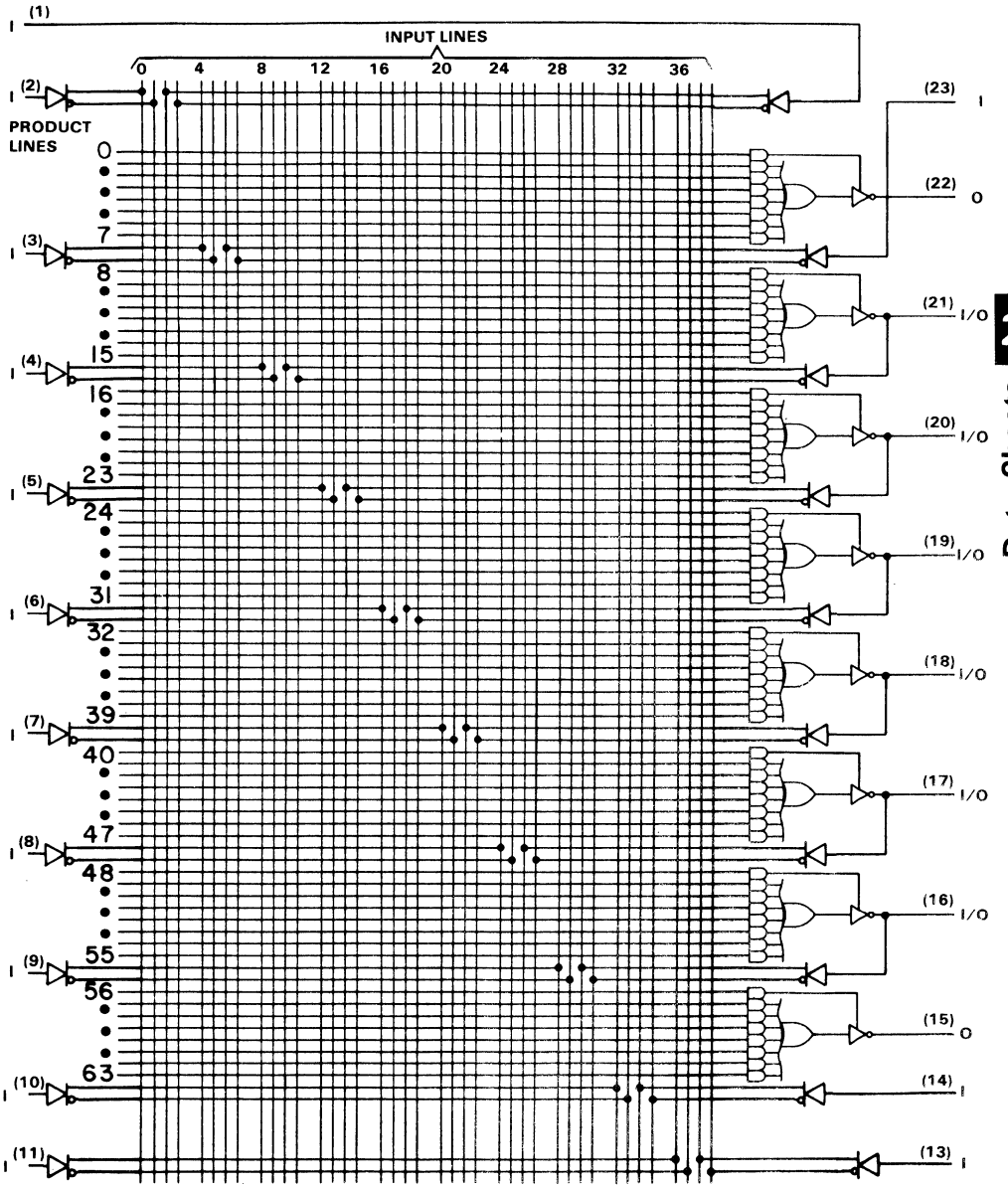
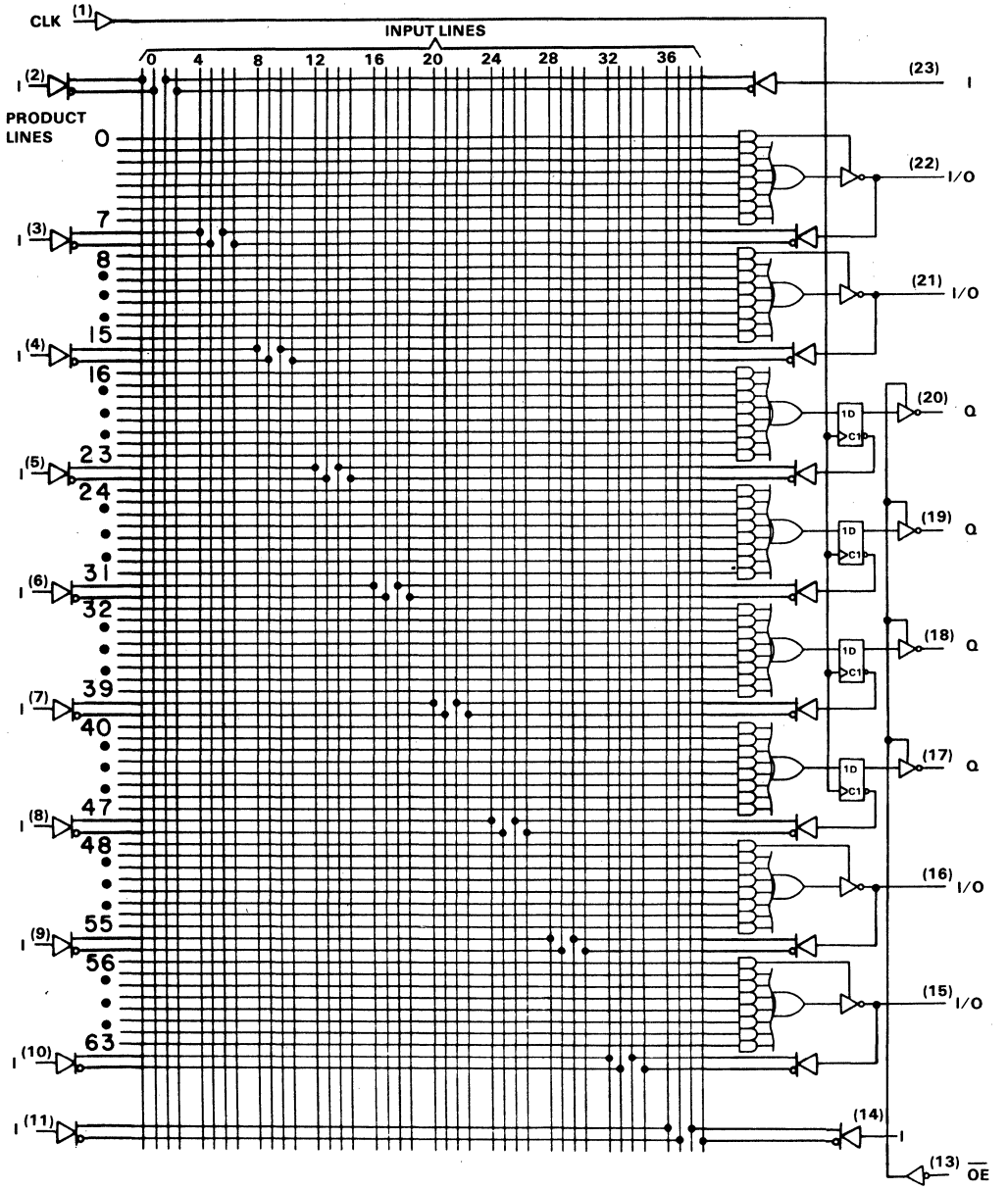
logic diagram (positive logic)



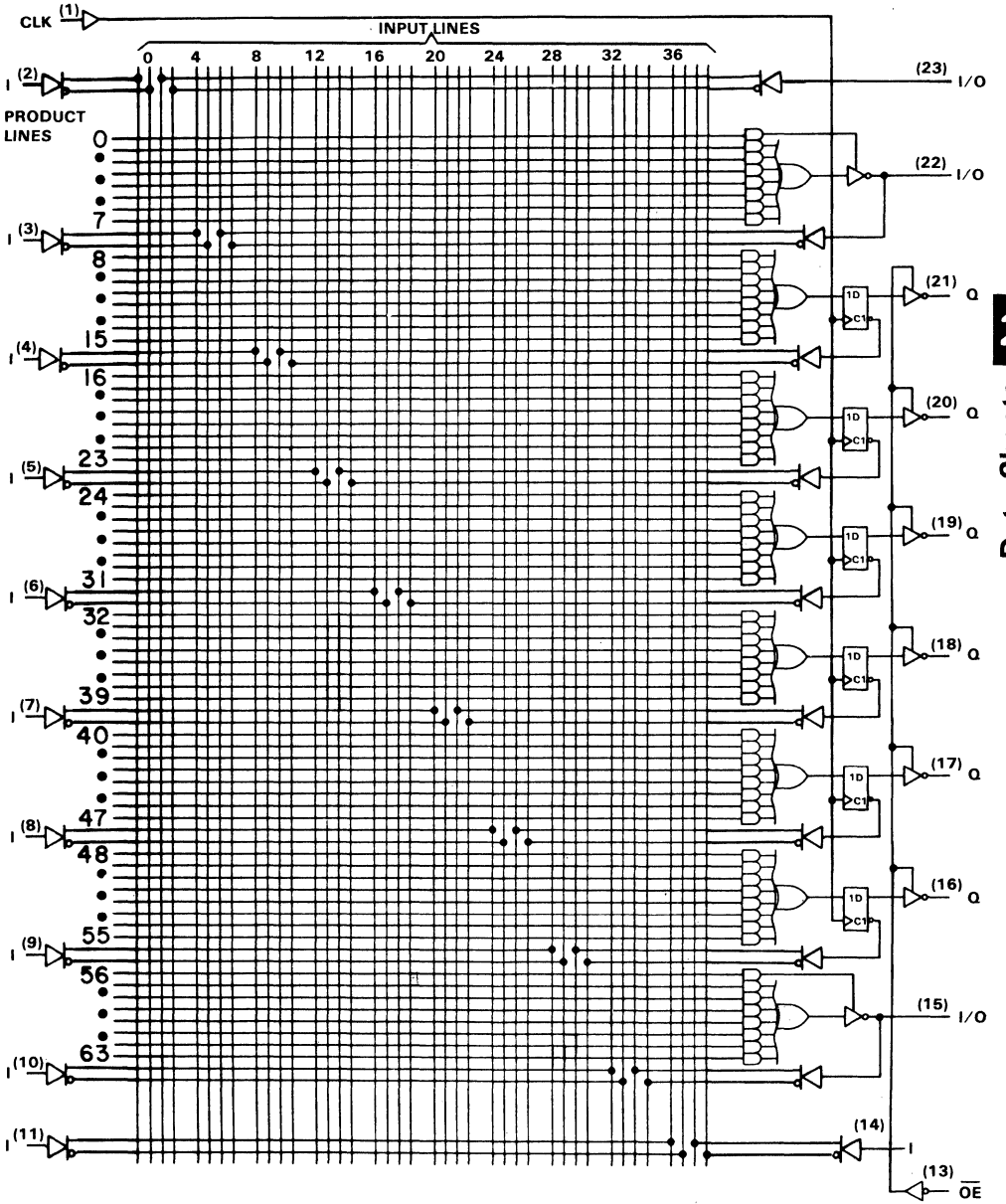
Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



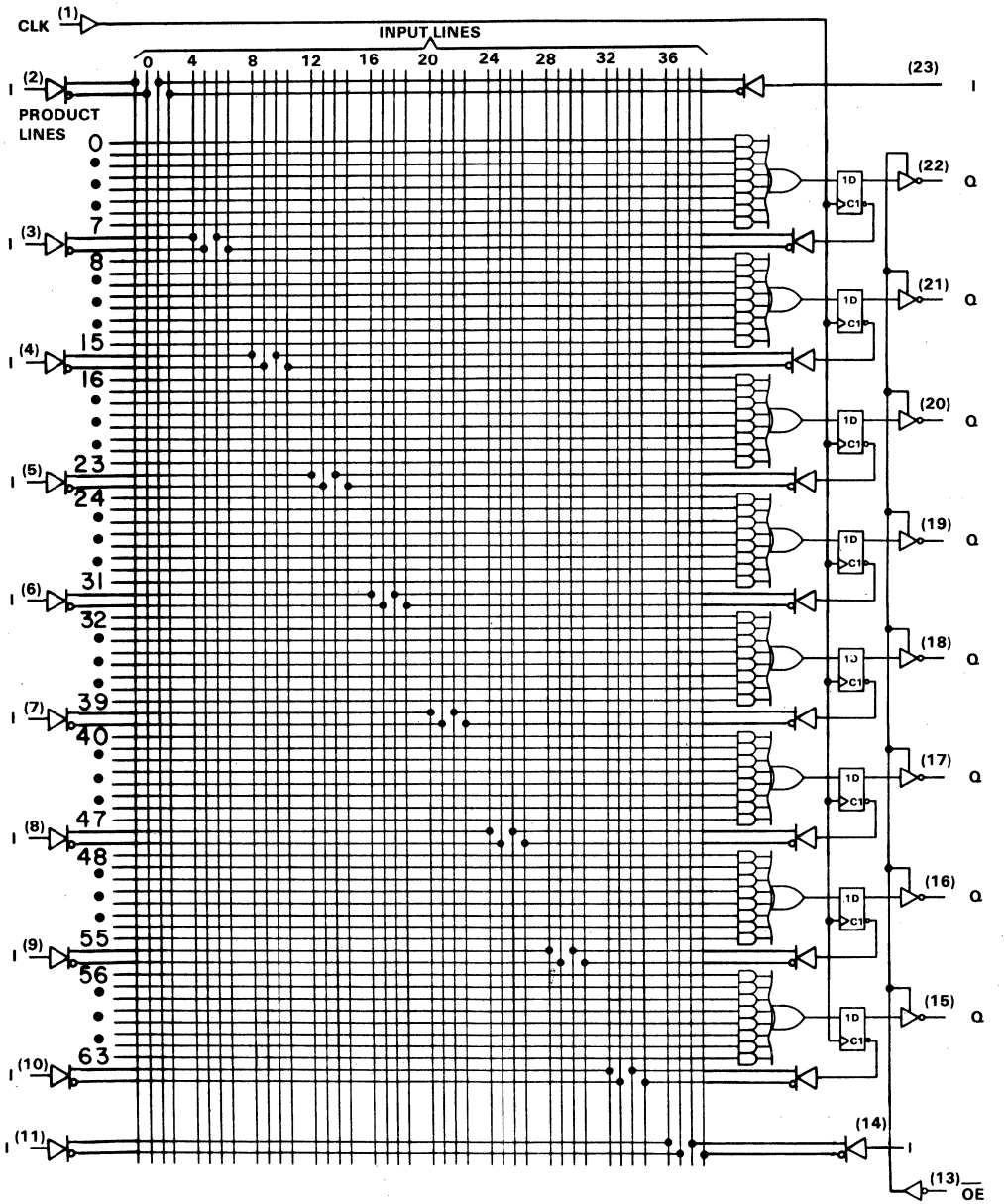
Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			−20M			−15C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		41.5	0		45	MHz
t_w	Pulse duration, clock	High	12			10			ns
		Low	12			12			ns
t_{su}	Setup time, input or feedback before CLK↑		20	10		15	10		ns
t_h	Hold time, input or feedback after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		75	°C

f_{clock}, t_w, t_{su}, and t_h do not apply for TIBPAL20L8'.

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS	−15C MIN	−15C TYP†	−15C MAX	UNIT
V_{IK}		V_{CC} = 4.75 V, I_I = −18 mA		−0.8	−1.5	V
V_{OH}		V_{CC} = 4.75 V, I_{OH} = −3.2 mA	2.4			V
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 24 mA		0.3	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = 5.25 V, V_O = 2.7 V			20	μA
	I/O ports				100	
I_{OZL}	O, Q outputs	V_{CC} = 5.25 V, V_O = 0.4 V			−20	μA
	I/O ports				−0.25	mA
I_I		V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}‡		V_{CC} = 5.25 V, V_I = 2.7 V			25	μA
I_{IL}‡		V_{CC} = 5.25 V, V_I = 0.4 V			−0.25	mA
I_{OS}§		V_{CC} = 5.25 V, V_O = 0	−30	−70	−130	mA
I_{CC}		V_{CC} = 5.25 V, Outputs open, V_I = 0, $\overline{OE}$ at V_{IH}		120	180	mA

† All typical values are V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	−15C MIN	−15C TYP†	−15C MAX	UNIT
f_{max}¶	with feedback		R_1 = 200 Ω, R2 = 390 Ω, C_L = 50 pF, See Figure 1	37	40		MHz
	without feedback			45	50		
t_{pd}	I, I/O	O, I/O			12	15	ns
t_{pd}	CLK↑	Q			8	12	ns
t_{en}	$\overline{OE}$	Q			10	15	ns
t_{dis}	$\overline{OE}$↑	Q			8	12	ns
t_{en}	I, I/O	O, I/O			12	18	ns
t_{dis}	I, I/O	O, I/O			12	15	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶ f_{max} (with feedback) = $\frac{1}{t_{su} + t_{pd}\text{ (CLK to Q)}}$, f_{max} (without feedback) = $\frac{1}{t_w\text{ high} + t_w\text{ low}}$

f_{max} does not apply for TIBPAL20L8'

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS	−20M			UNIT
			MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA		−0.8	−1.5	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −2 mA	2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 12 mA		0.25	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = 5.5 V, V_O = 2.7 V			20	μA
	I/O ports				100	
I_{OZL}	O, Q outputs	V_{CC} = 5.5 V, V_O = 0.4 V			−20	μA
	I/O ports				−0.25	mA
I_I		V_{CC} = 5.5 V, V_I = 5.5 V			1	mA
I_{IH}‡		V_{CC} = 5.5 V, V_I = 2.7 V			25	μA
I_{IL}‡		V_{CC} = 5.5 V, V_I = 0.4 V			−0.25	mA
I_{OS}§		V_{CC} = 5.5 V, V_O = 0	−30	−70	−130	mA
I_{CC}		V_{CC} = 5.5 V, Outputs open, V_I = 0, $\overline{OE}$ at V_{IH}		120	180	mA

† All typical values are V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	−20M			UNIT
				MIN	TYP†	MAX	
f_{max}¶	with feedback		R_1 = 390 Ω, R2 = 750 Ω, C_L = 50 pF, See Figure 1	28.5	40		MHz
	without feedback			41.5	50		
t_{pd}	I, I/O	O, I/O			12	20	ns
t_{pd}	CLK↑	Q			8	15	ns
t_{en}	$\overline{OE}$	Q			10	20	ns
t_{dis}	$\overline{OE}$↑	Q			8	20	ns
t_{en}	I, I/O	O, I/O			12	25	ns
t_{dis}	I, I/O	O, I/O			12	20	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶ f_{max} (with feedback) $= \frac{1}{t_{su} + t_{pd}\text{ (CLK to Q)}}$, f_{max} (without feedback) $= \frac{1}{t_w\text{ high} + t_w\text{ low}}$

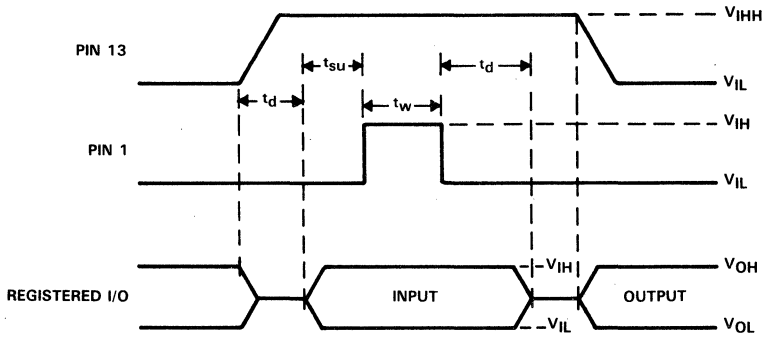
f_{max} does not apply for TIBPAL20L8'

preload procedure for registered outputs (see Note 2)

The output registers of the TIBPAL20R' can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 V and pin 1 at V_{IL}, raise pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

preload waveforms (see Notes 2 and 3)



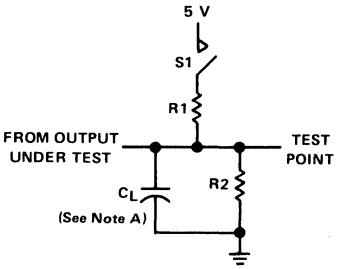
NOTES: 2. Pin numbers shown are for JT and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_w$ = 100 ns to 1000 ns.
V_{IHH} = 10.25 V to 10.75 V.

programming information

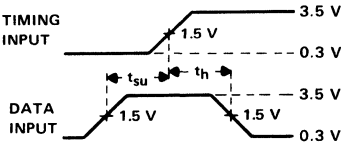
Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5762.

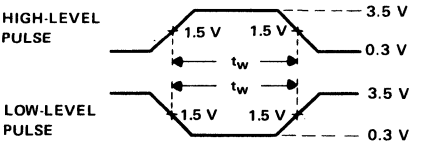
PARAMETER MEASUREMENT INFORMATION



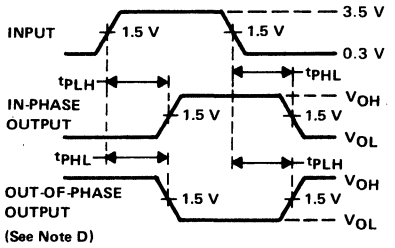
LOAD CIRCUIT FOR THREE-STATE OUTPUTS



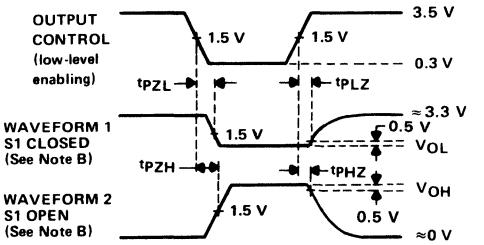
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

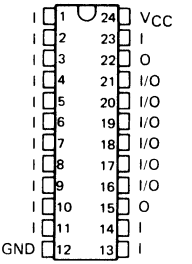
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

FIGURE 1

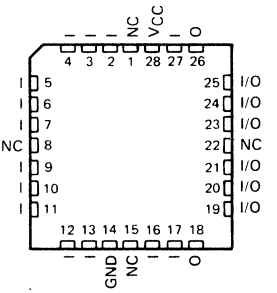
- **Low-Power, High Performance**
  Reduced I_{CC} of 105 mA Max
  f_{max} (TIBPAL20R'-25C Series):
  Without Feedback . . . 33 MHz Min
  With Feedback . . . 25 MHz Min
  t_{pd} (TIBPAL20'-25C Series) . . . 25 ns Max
- **Direct Replacement for PAL20L8A, PAL20R4A, PAL20R6A, and PAL20R8A with at Least 50% Reduction in Power**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices**
- **Package Options Include Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PAL20L8	14	2	0	6
'PAL20R4	12	0	4 (3-state buffers)	4
'PAL20R6	12	0	6 (3-state buffers)	2
'PAL20R8	12	0	8 (3-state buffers)	0

TIBPAL20L8'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20L8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are also available for further reduction in board space.

In many cases, these low-power devices are fast enough to be used where the high-speed or "A" devices are used. From an overall system level, this can amount to a significant reduction in power consumption, with no sacrifice in speed.

All of the output registers are set to a low level during power-up, but the voltage levels at the output pins stay high. Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL20'M series is characterized for operation over the full military temperature range of −55°C to 125°C. The TIBPAL20'C is characterized from 0°C to 75°C.

IMPACT is a trademark of Texas Instruments Incorporated
PAL is a registered trademark of Monolithic Memories Inc.
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

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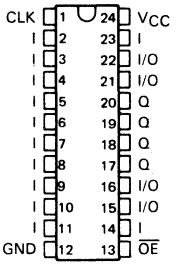
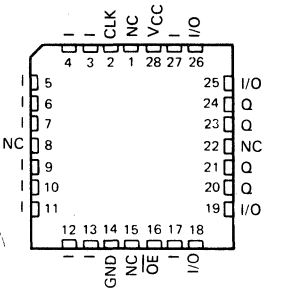
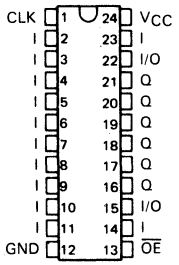
TIBPAL20R4'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



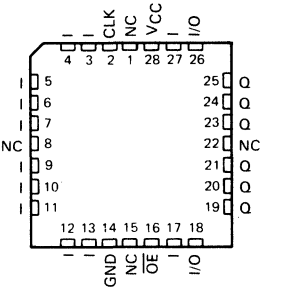
TIBPAL20R4'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



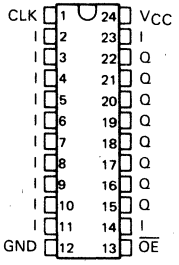
TIBPAL20R6'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



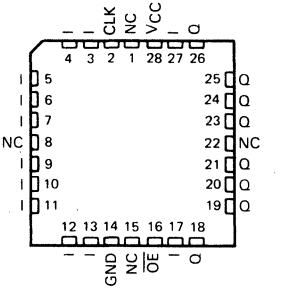
TIBPAL20R6'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL20R8'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20R8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode

NC—No internal connection

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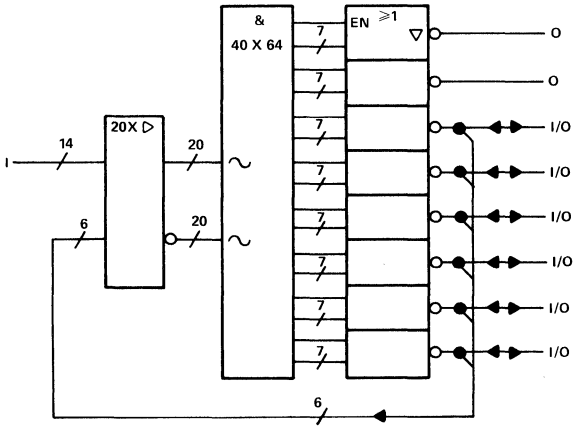
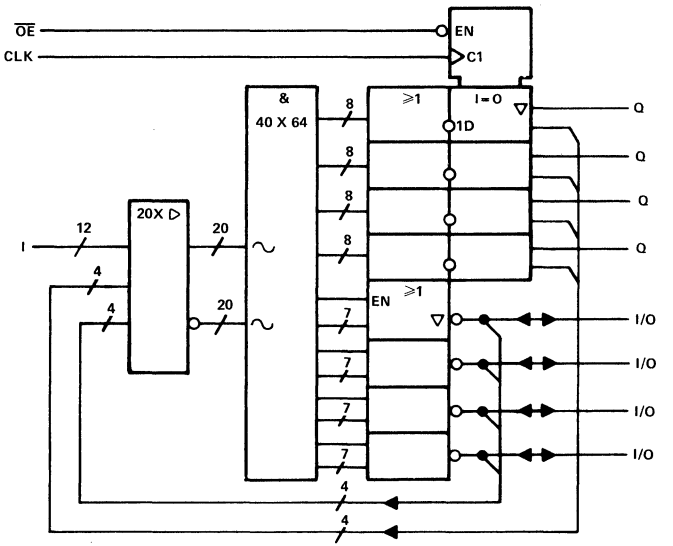
functional block diagrams (positive logic)

TIBPAL20L8'



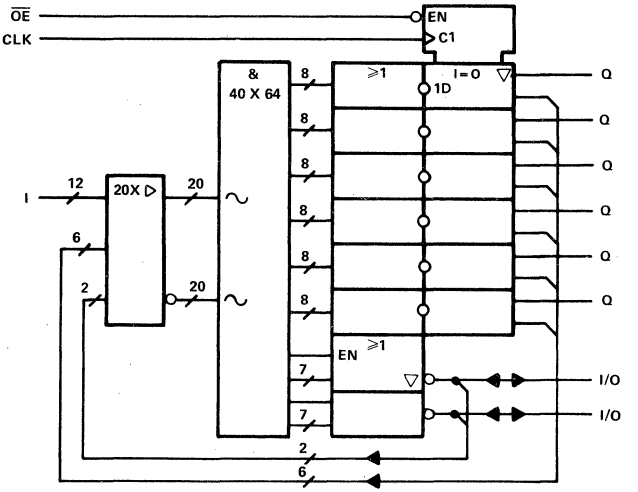
TIBPAL20R4'



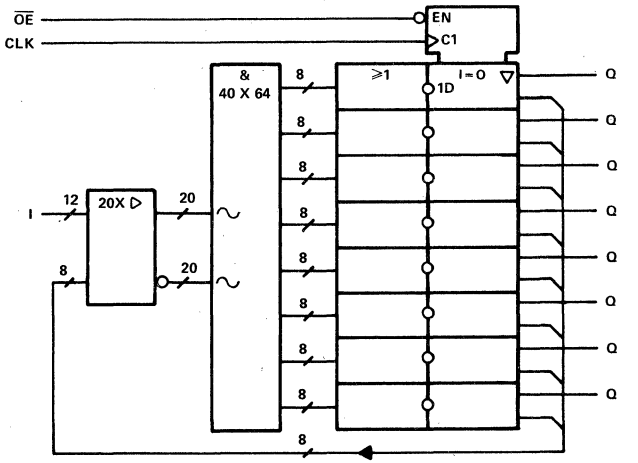
∼ denotes fused inputs

functional block diagrams (positive logic)

TIBPAL20R6'

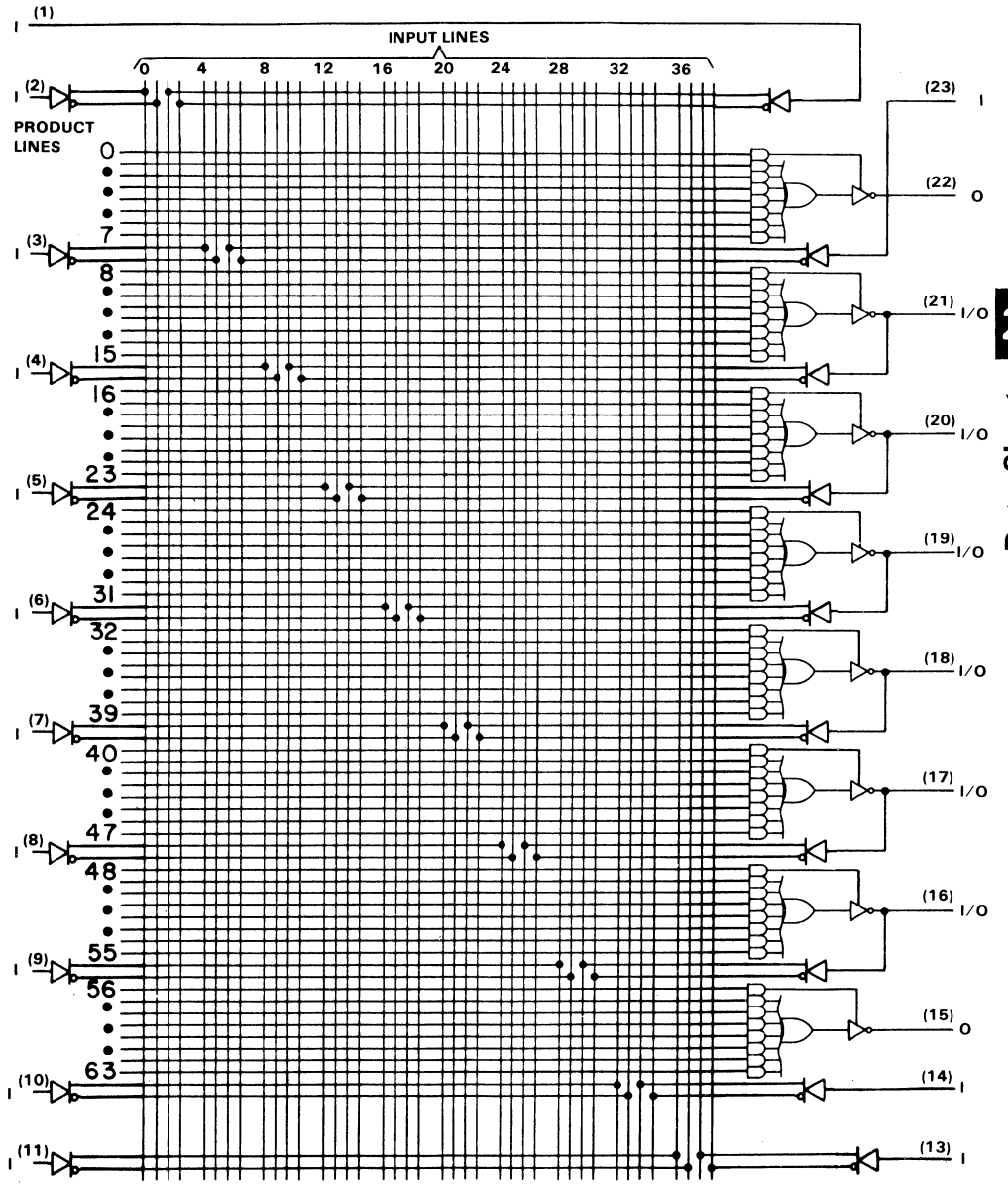


TIBPAL20R8'



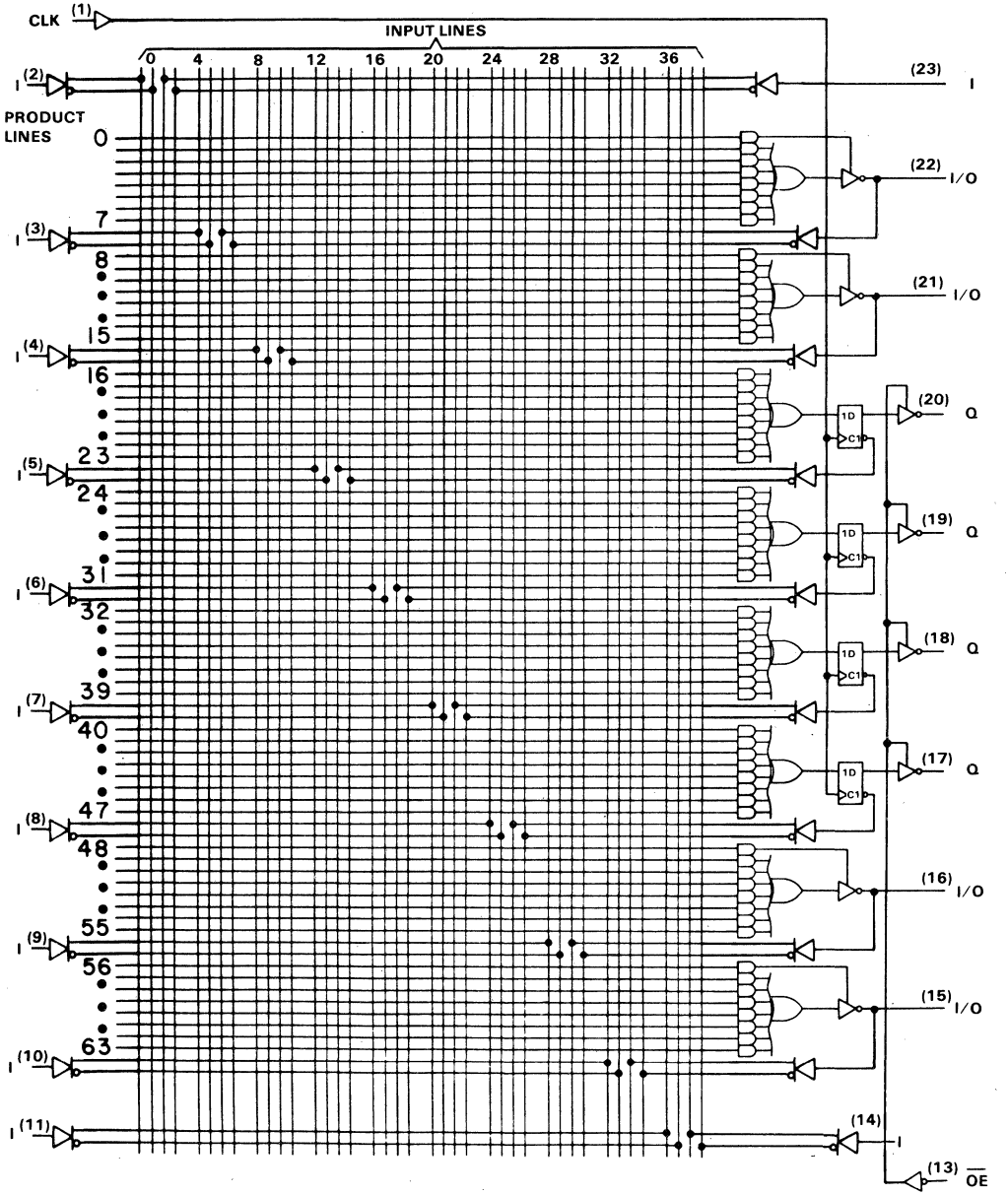
∼ denotes fused inputs

logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

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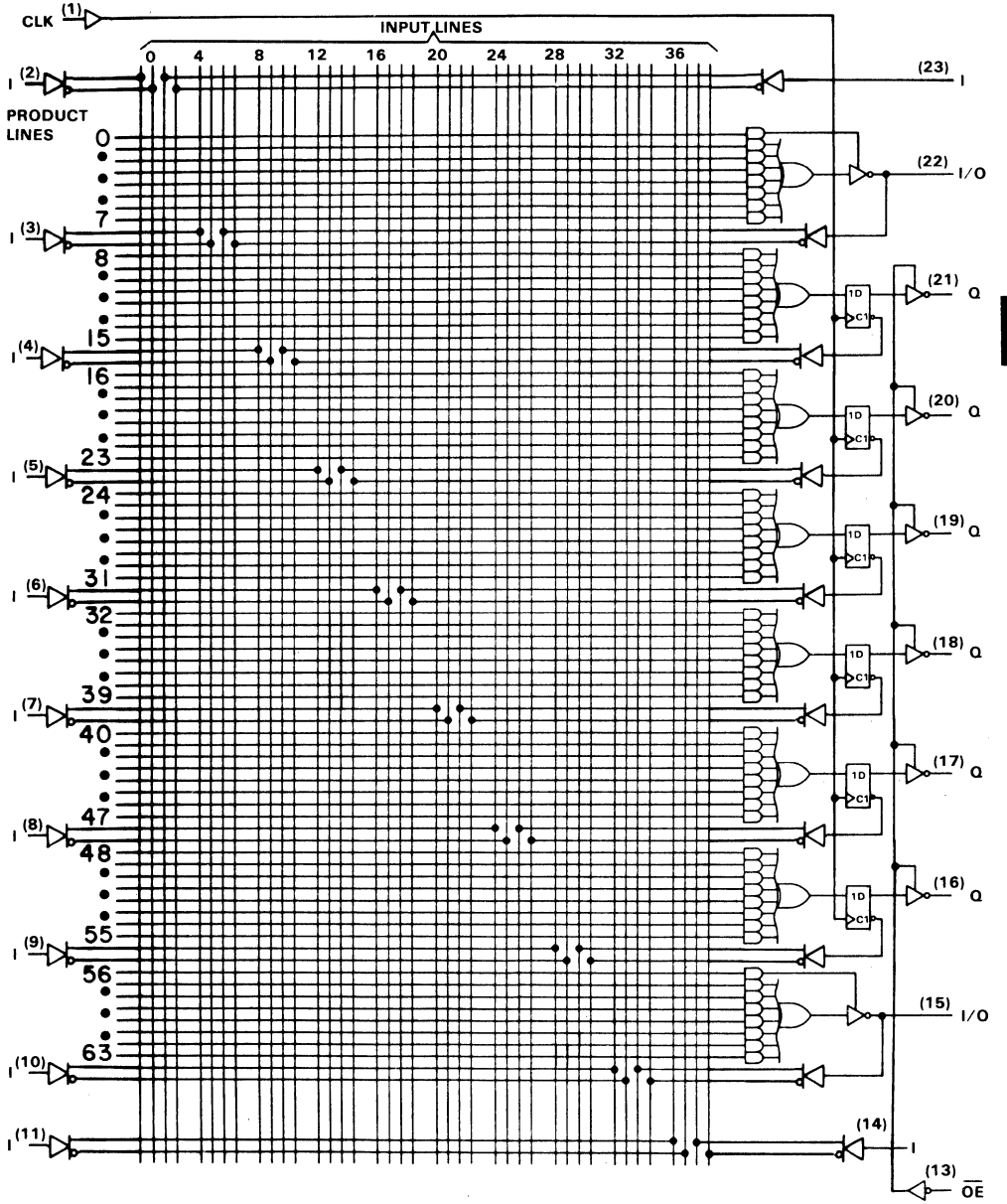
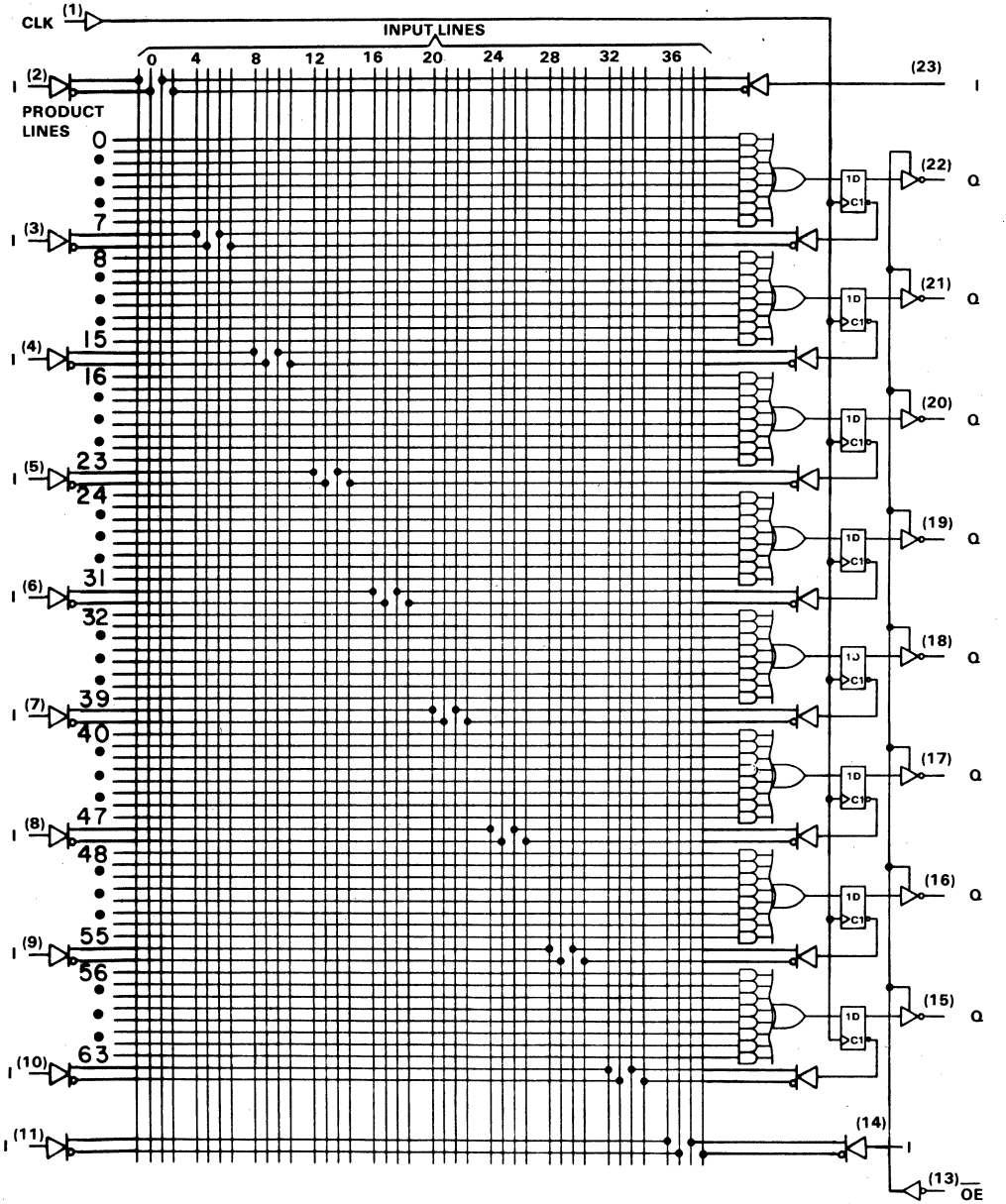
logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			-30M			-25C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		25	0		33	MHz
t_w	Pulse duration, clock	High				15			ns
		Low				15			ns
t_{su}	Setup time, input or feedback before CLK↑					25			ns
t_h	Hold time, input or feedback after CLK↑					0			ns
T_A	Operating free-air temperature		−55		125	0		75	°C

f_{clock}, t_w, t_{su}, and t_h do not apply for TIBPAL20L8'.

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS	-30M MIN	-30M TYP†	-30M MAX	UNIT
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA		−0.8	−1.5	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −2 mA	2.4	3.3		V
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 12 mA		0.25	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = 5.5 V, V_O = 2.7 V			20	μA
	I/O ports				100	
I_{OZL}	O, Q outputs	V_{CC} = 5.5 V, V_O = 0.4 V			−20	μA
	I/O ports				−0.25	mA
I_I		V_{CC} = 5.5 V, V_I = 5.5 V			0.1	mA
I_{IH}‡		V_{CC} = 5.5 V, V_I = 2.7 V			20	μA
I_{IL}‡		V_{CC} = 5.5 V, V_I = 0.4 V			−0.2	mA
I_{OS}§		V_{CC} = 5.5 V, V_O = 0	−30	−70	−130	mA
I_{CC}		V_{CC} = 5.5 V, V_I = 0, Outputs open, $\overline{OE}$ at V_{IH}		75		mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed 1 second.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	-30M MIN	-30M TYP†	-30M MAX	UNIT
f_{max}¶	with feedback		R_1 = 390 Ω, R2 = 750 Ω, C_L = 50 pF, See Figure 1				MHz
	without feedback			25			
t_{pd}	I, I/O	O, I/O				30	ns
t_{pd}	CLK↑	Q					ns
t_{en}	$\overline{OE}$	Q					ns
t_{dis}	$\overline{OE}$↑	Q					ns
t_{en}	I, I/O	O, I/O25					ns
t_{dis}	I, I/O	O, I/O					ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶ f_{max} (with feedback) = $\frac{1}{t_{su} + t_{pd}\ (CLK\ to\ Q)}$, f_{max} (without feedback) = $\frac{1}{t_W\ high + t_W\ low}$

f_{max} does not apply for TIBPAL20L8'

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS	-25C MIN	-25C TYP†	-25C MAX	UNIT
V_{IK}		V_{CC} = 4.75 V, I_I = −18 mA		−0.8	−1.5	V
V_{OH}		V_{CC} = 4.75 V, I_{OH} = −3.2 mA	2.4	3.3		V
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 24 mA		0.3	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = 5.25 V, V_O = 2.7 V			20	μA
	I/O ports				100	
I_{OZL}	O, Q outputs	V_{CC} = 5.25 V, V_O = 0.4 V			−20	μA
	I/O ports				−0.25	mA
I_I		V_{CC} = 5.25 V, V_I = 5.5 V			0.1	mA
I_{IH}‡		V_{CC} = 5.25 V, V_I = 2.7 V			20	μA
I_{IL}‡		V_{CC} = 5.25 V, V_I = 0.4 V			−0.2	mA
I_{OS}§		V_{CC} = 5.25 V, V_O = 0	−30	−70	−130	mA
I_{CC}		V_{CC} = 5.25 V, Outputs open, V_I = 0, $\overline{OE}$ at V_{IH}		75	105	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed 1 second.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	-25C MIN	-25C TYP†	-25C MAX	UNIT
f_{max}¶	with feedback		R_1 = 200 Ω, R2 = 390 Ω, C_L = 50 pF, See Figure 1	25	40		MHz
	without feedback			33	50		
t_{pd}	I, I/O	O, I/O		3	14	25	ns
t_{pd}	CLK↑	Q		2	10	15	ns
t_{en}	$\overline{OE}$	Q		2	8	15	ns
t_{dis}	$\overline{OE}$↑	Q		2	8	15	ns
t_{en}	I, I/O	O, I/O		3	15	25	ns
t_{dis}	I, I/O	O, I/O		3	15	25	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ f_{max} (with feedback) = $\frac{1}{t_{su} + t_{pd}\text{ (CLK to Q)}}$, f_{max} (without feedback) = $\frac{1}{t_w\text{ high} + t_w\text{ low}}$

f_{max} does not apply for TIBPAL20L8'

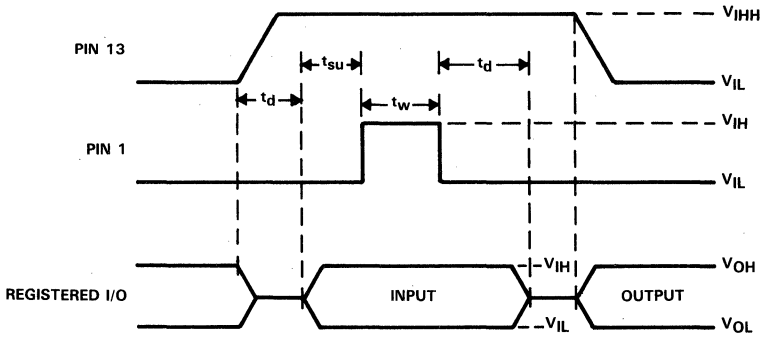
PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

preload procedure for registered outputs (see Note 2)

The output registers of the TIBPAL20R' can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 V and pin 1 at V_{IL}, raise pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

preload waveforms (see Notes 2 and 3)



NOTES: 2. Pin numbers shown are for JT and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_w$ = 100 ns to 1000 ns.
V_{IHH} = 10.25 V to 10.75 V.

programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

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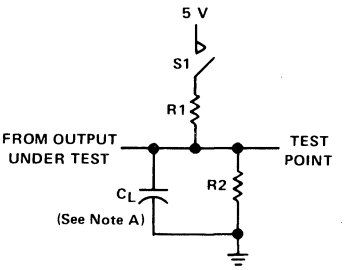
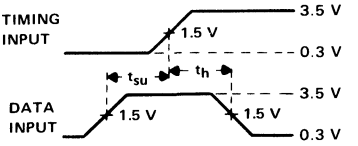
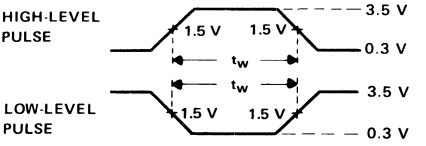
PARAMETER MEASUREMENT INFORMATION



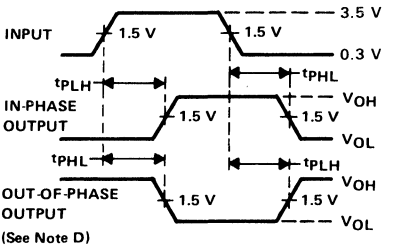
LOAD CIRCUIT FOR THREE-STATE OUTPUTS



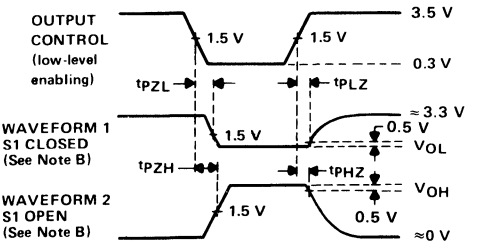
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

FIGURE 1

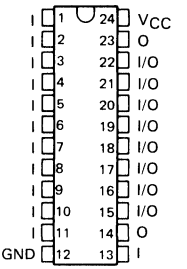
HIGH-PERFORMANCE EXCLUSIVE-OR *IMPACT*™ *PAL*® CIRCUITS

D2920, OCTOBER 1985—REVISED DECEMBER 1987

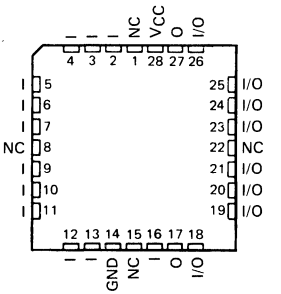
- **High Performance . . . 35 MHz Min**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PAL20L10	12	2	0	8
'PAL20X4	10	0	4 (3-state buffers)	6
'PAL20X8	10	0	8 (3-state buffers)	2
'PAL20X10	10	0	10 (3-state buffers)	0

TIBPAL20L10'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20L10'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

All of the registered outputs are set to a low level during power-up. In addition, extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The PAL20' M series is characterized for operation over the full military temperature range of −55°C to 125°C. The PAL20' C series is characterized for operation from 0°C to 75°C.

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PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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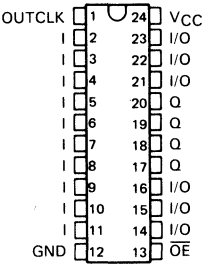
TIBPAL20X4'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



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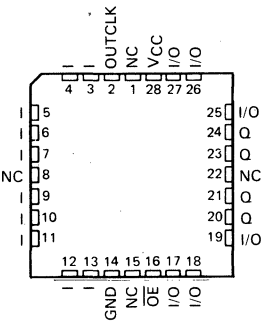

TIBPAL20X8'
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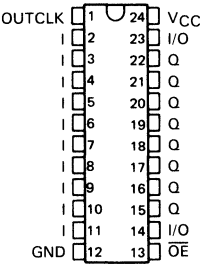
(TOP VIEW)



TIBPAL20X8'
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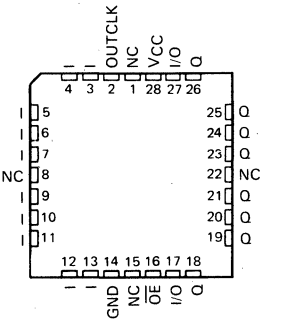
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL20X10'
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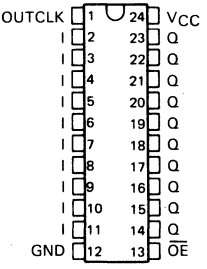

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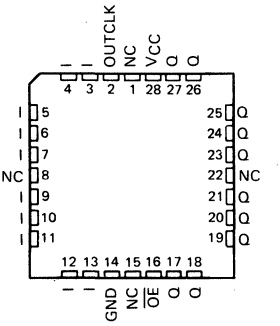


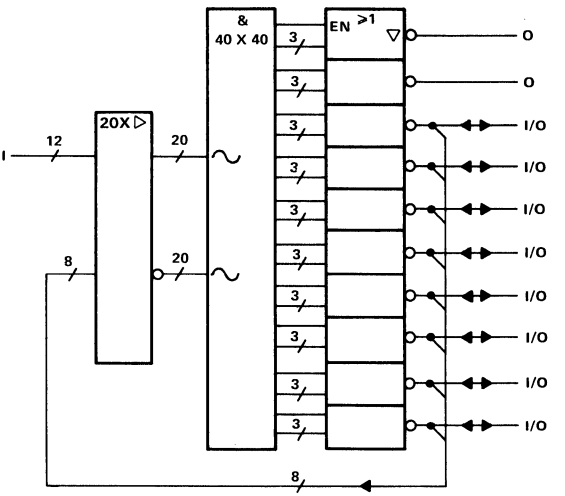
NC—No internal connection

Pin assignments in operating mode

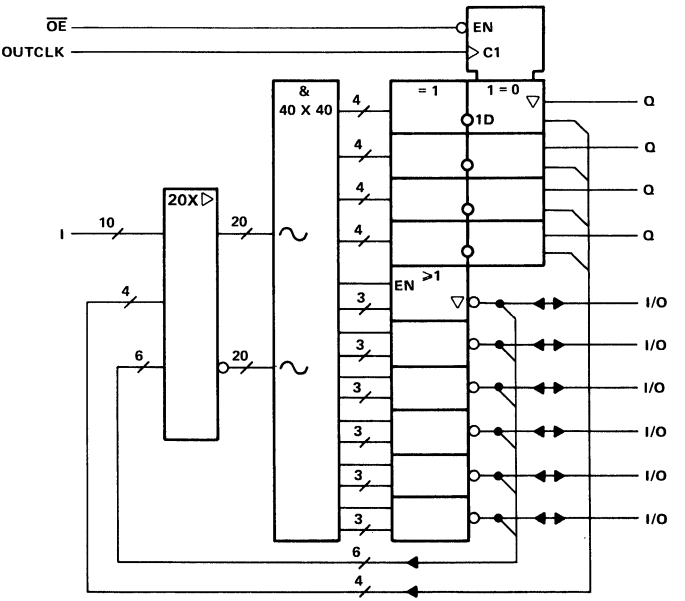
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

functional block diagrams (positive logic)

'PAL20L10



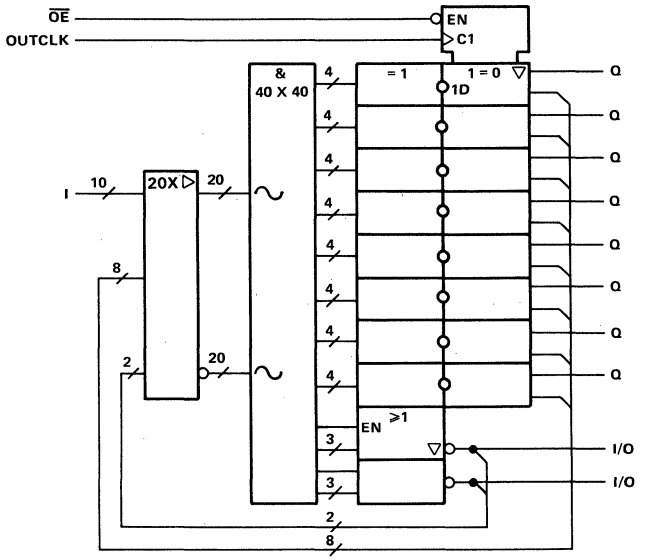
'PAL20X4



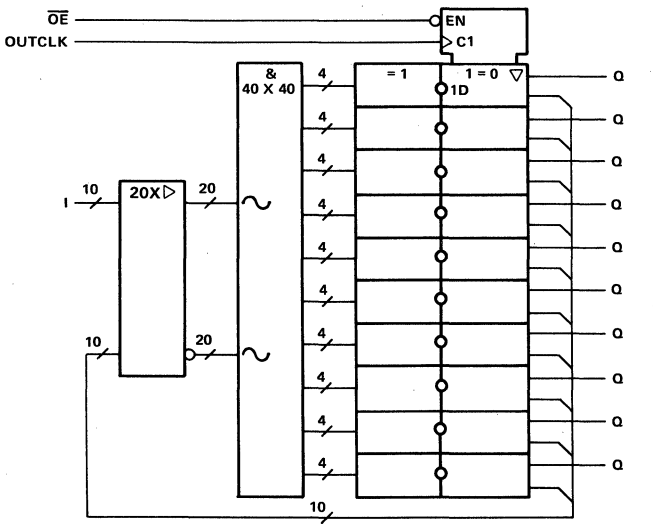
~ denotes fused inputs

functional block diagrams (positive logic)

'PAL20X8



'PAL20X10



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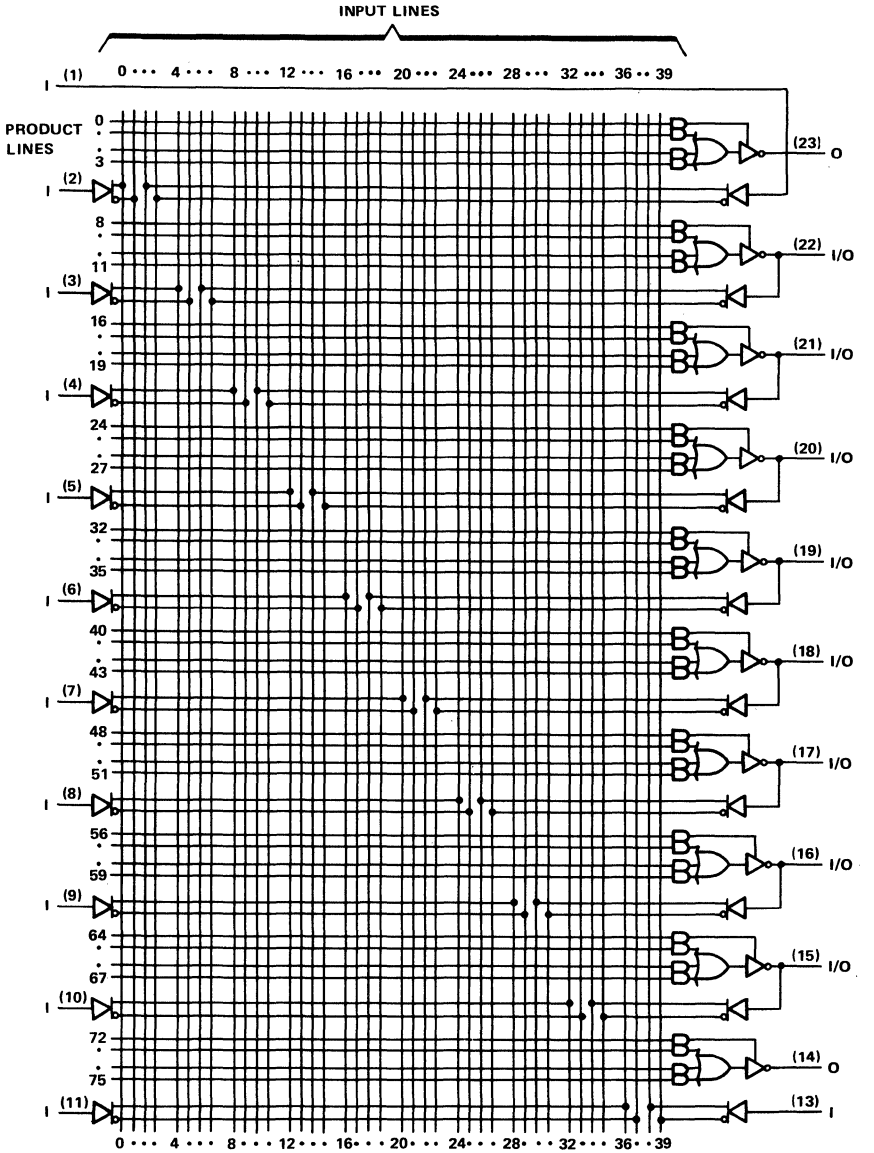
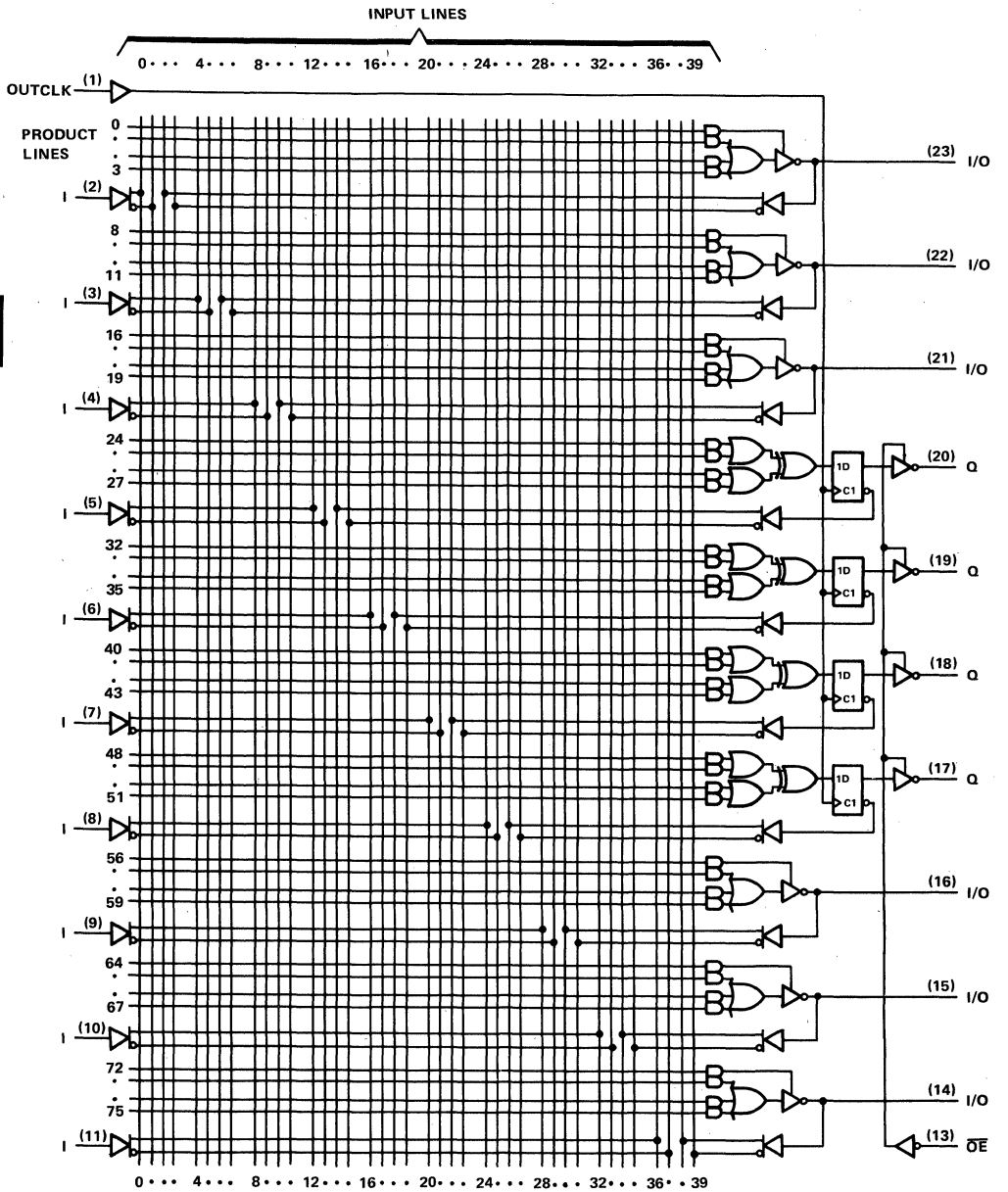
logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



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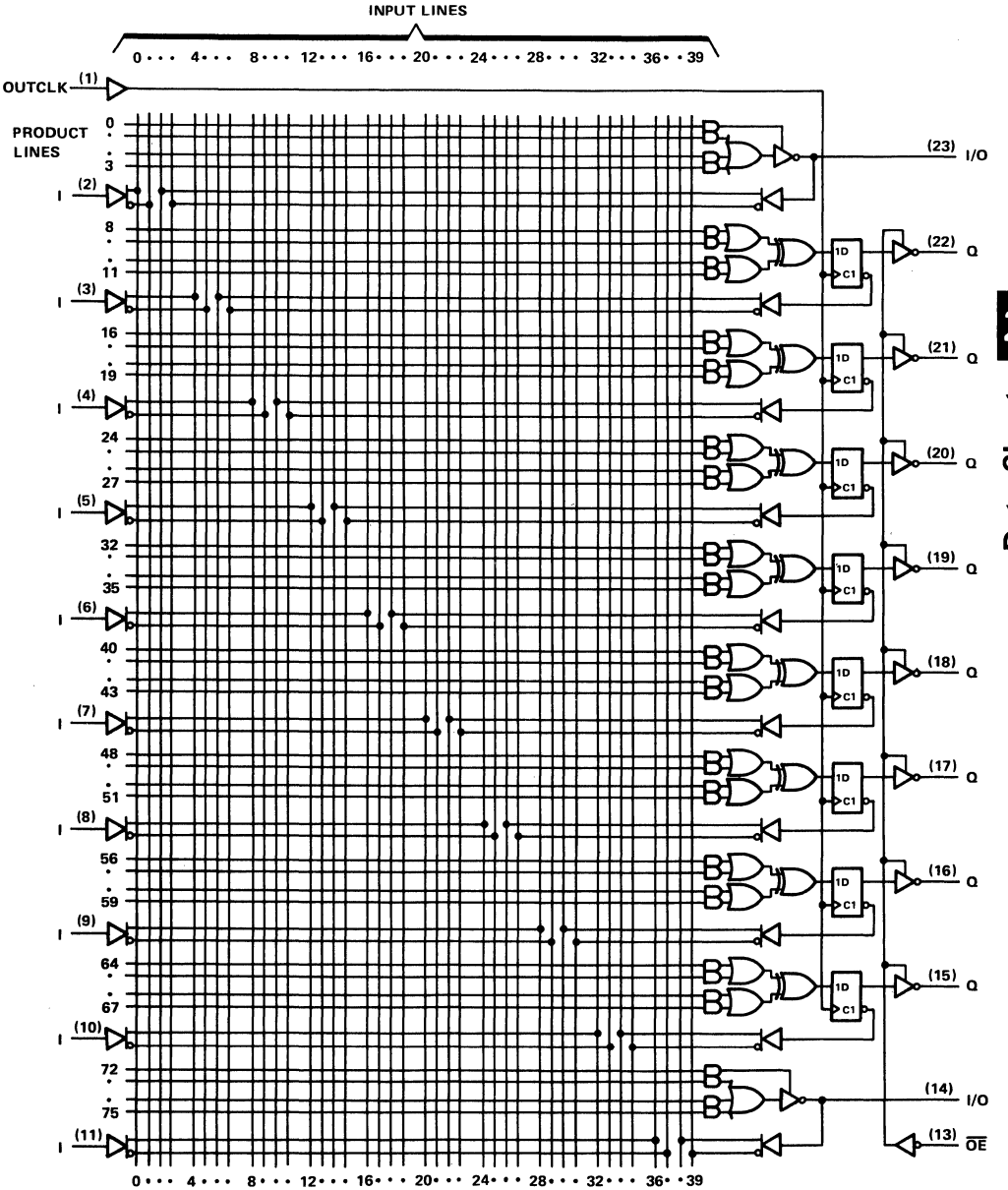

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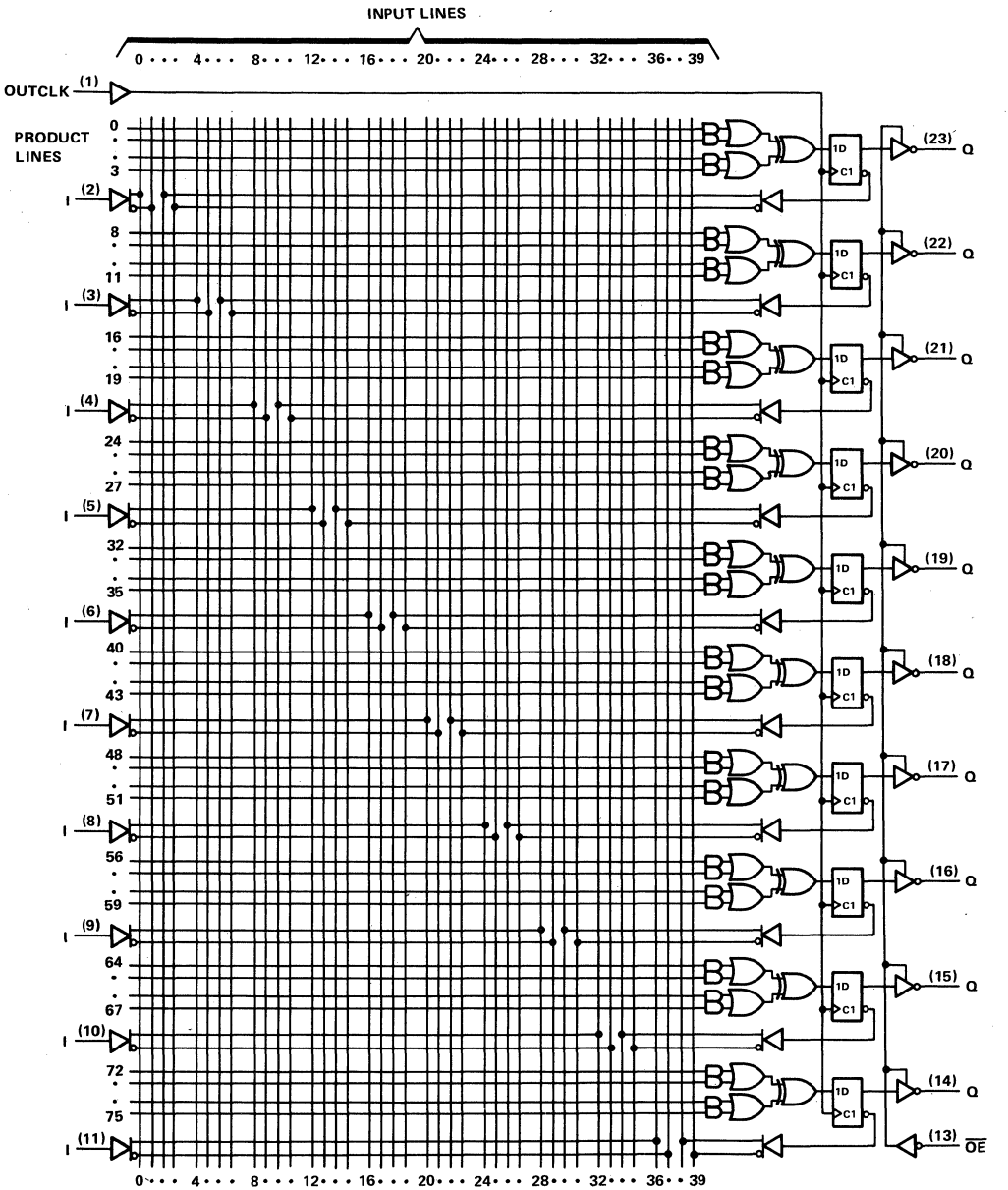

Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			−25M			−20C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		25	0		35	MHz
t_w	Pulse duration, clock, see Note 2	High	15			10			ns
		Low	20			14			ns
t_{su}	Setup time, input or feedback before OUTCLK↑		25			20			ns
t_h	Hold time, input or feedback after OUTCLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		75	°C

NOTE 2: The high and low clock pulse durations cannot both be at the minimum values specified. Their sum must be equal to or greater than the minimum clock period, which is the reciprocal of the maximum recommended clock frequency.

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†	−25M			−20C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = MIN, I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN, I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX, V_O = 2.7 V			20			20	μA
	I/O ports				100			100	
I_{OZL}	Outputs	V_{CC} = MAX, V_O = 0.4 V			−20			−20	μA
	I/O ports				−250			−250	
I_I		V_{CC} = MAX, V_I = 5.5 V			0.1			0.1	mA
I_{IH}		V_{CC} = MAX, V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = MAX, V_I = 0.4 V			−0.25			−0.25	mA
I_{OS}§		V_{CC} = 5 V, V_O = 0	−30		−130	−30		−130	mA
I_{CC}	'20X4, '20X8, '20X10	V_{CC} = MAX, V_I = 0		120	180		120	180	mA
	'20L10			120	165		120	165	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	−25M			−20C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}				25			35			MHz
t_{pd}	I, I/O	O, I/O			12	25		12	20	ns
t_{pd}	OUTCLK↑	Q	R1 = 200 Ω,		10	20		10	15	ns
t_{en}	$\overline{OE}$	Q	R2 = 390 Ω,		7	20		7	15	ns
t_{dis}	$\overline{OE}$↑	Q	C_L = 50 pF		7	20		7	15	ns
t_{en}	I, I/O	O, I/O			15	25		15	20	ns
t_{dis}	I, I/O	O, I/O			15	25		15	20	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

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TEXAS INSTRUMENTS
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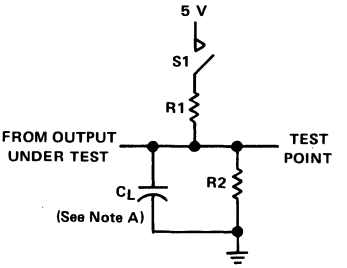

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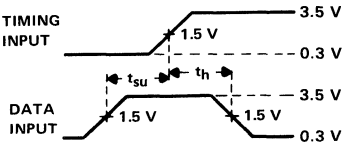
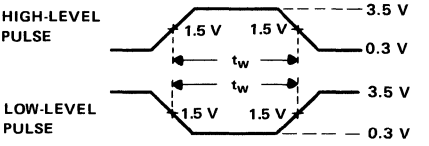
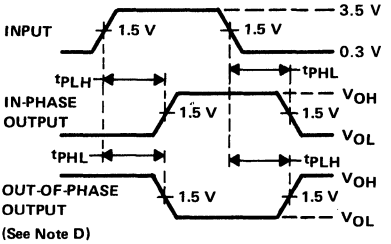
THREE-STATE OUTPUTS



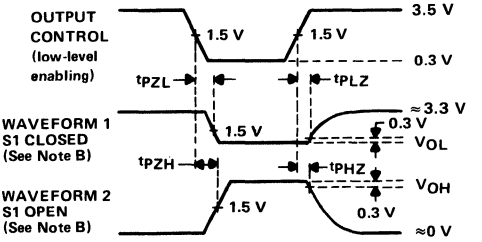
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

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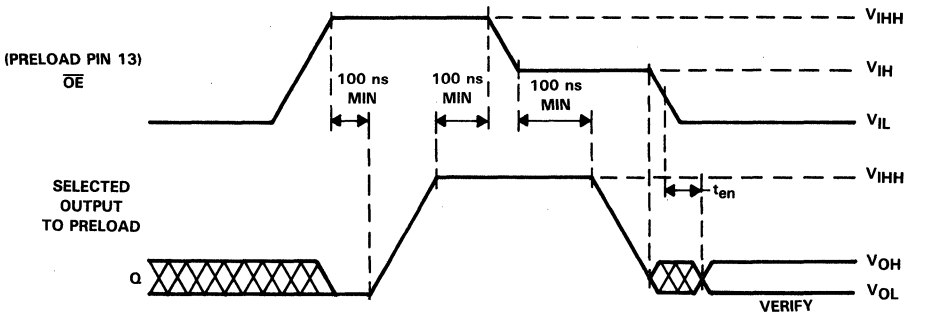
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, t_r = t_f = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

preload procedures

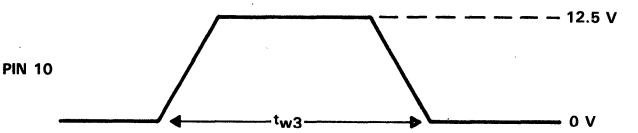
preload procedure for registered outputs

Step 1 With V_{CC} at 5 volts, raise Pin 13 ($\overline{OE}$) to V_{IHH} to disable the outputs and clear the registers (output goes low). Since the outputs are low, only high levels need be preloaded.
Step 2 Raise the selected output to be preloaded high to V_{IHH}.
Step 3 Lower Pin 13 to V_{IH}.
Step 4 Remove the voltages applied to the outputs. (At least a 100-ns wait is required between step 3 and step 4)
Step 5 Lower Pin 13 to V_{IL} to verify preload.



PRELOAD WAVEFORMS

security fuse programming



SECURITY FUSE PROGRAMMING WAVEFORMS

NOTE: Pin numbers shown apply only for the DIP package. If a chip carrier socket adaptor is not used, pin numbers must be changed accordingly.

D2920, DECEMBER 1987

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'PAL20X8	10	0	8 (3-state buffers)	2
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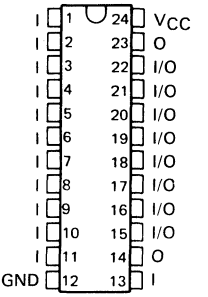
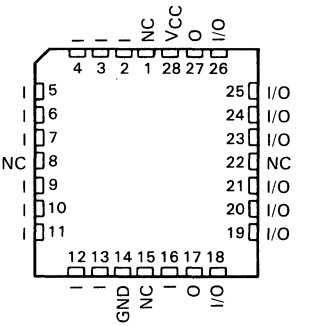
TIBPAL20L10'
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20L10'
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



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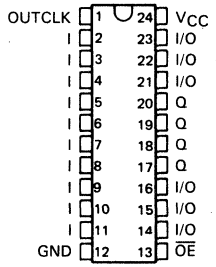
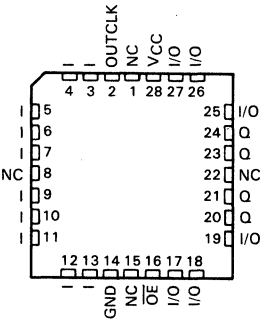
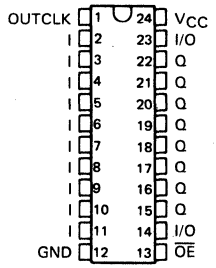
TIBPAL20X4'
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



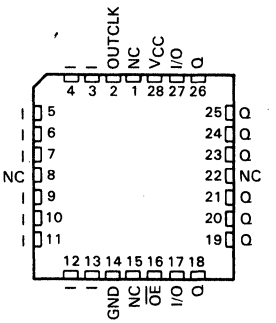
TIBPAL20X4'
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



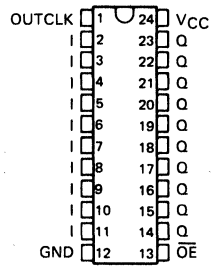
TIBPAL20X8'
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



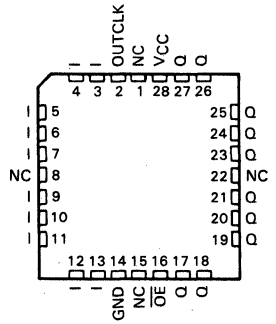
TIBPAL20X8'
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL20X10'
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20X10'
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



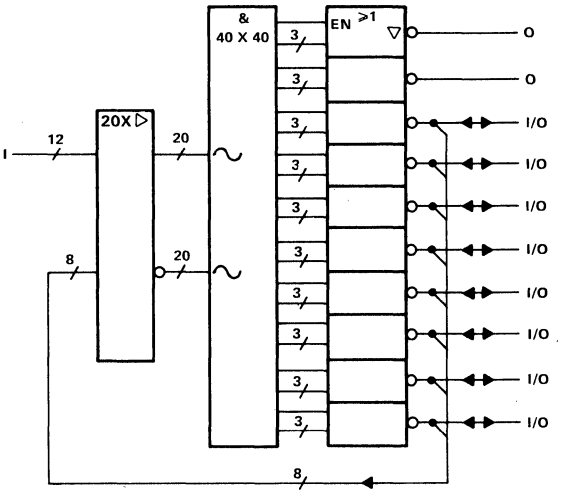
Pin assignments in operating mode

NC—No internal connection

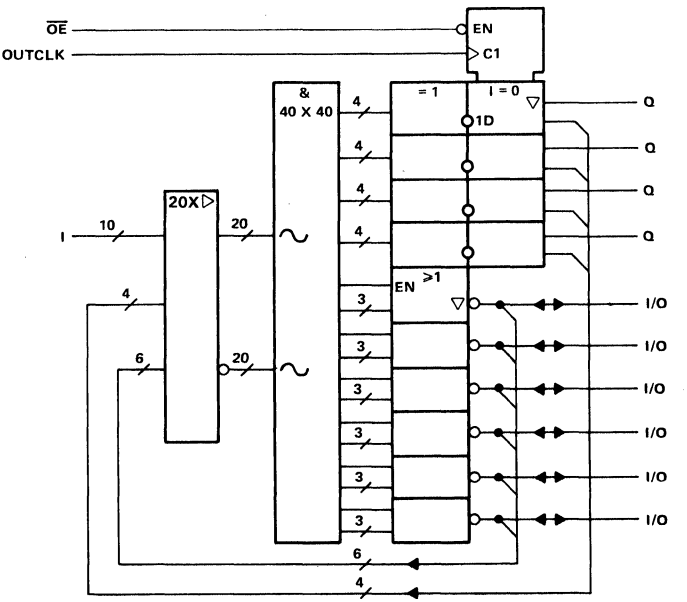
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

functional block diagrams (positive logic)

TIBPAL20L10'



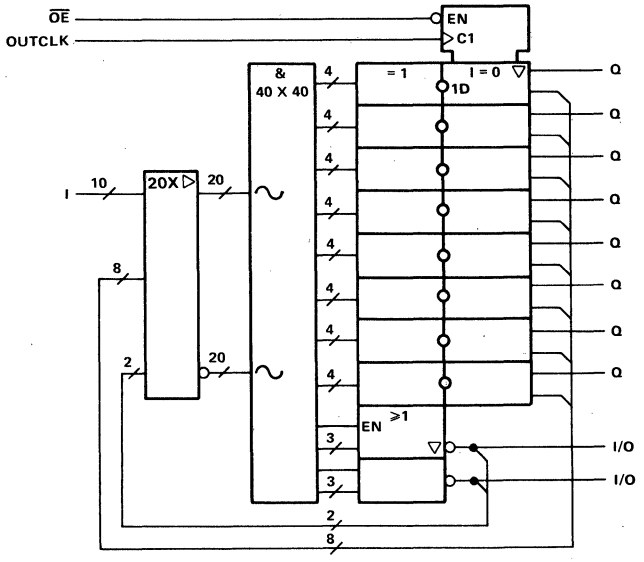
TIBPAL20X4'



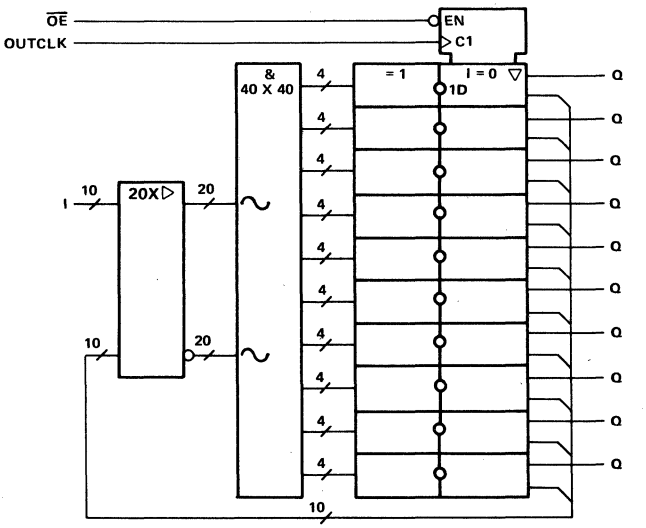
~ denotes fused inputs

functional block diagrams (positive logic)

TIBPAL20X8'

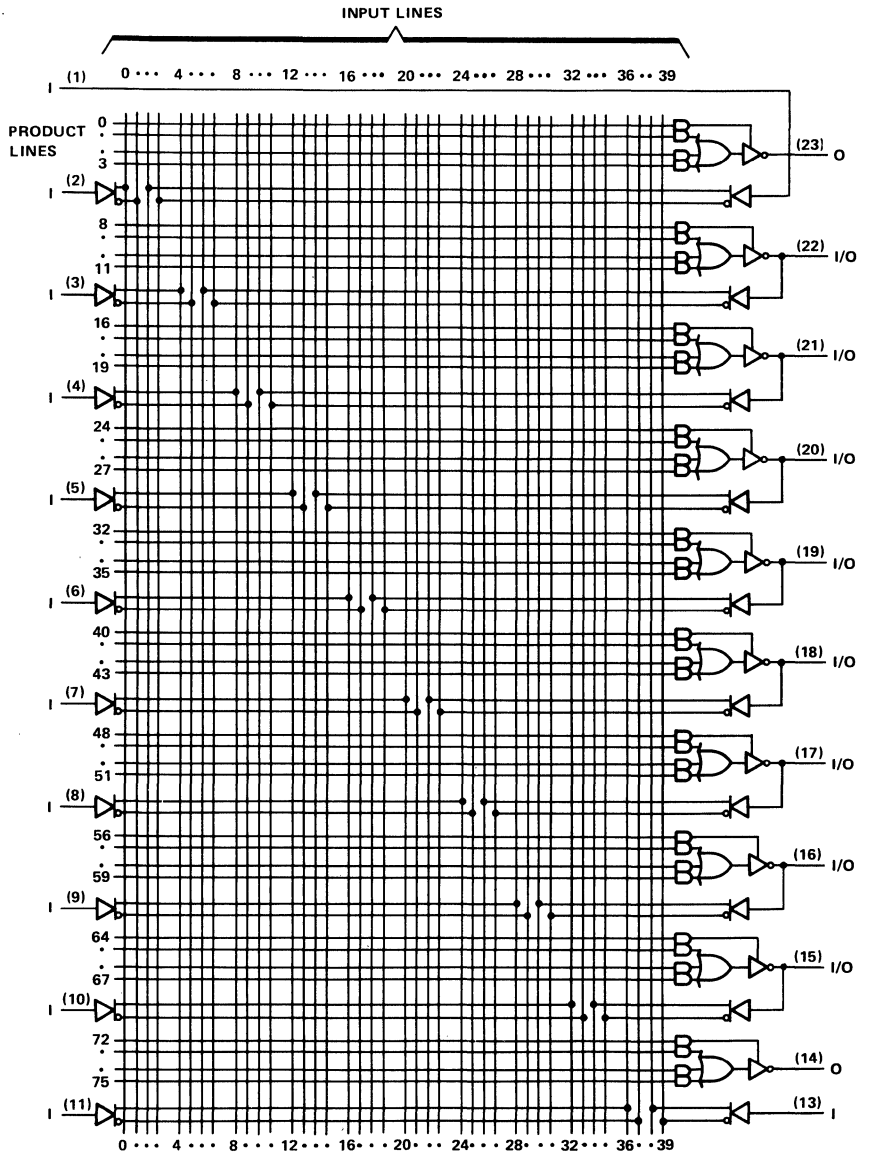


TIBPAL20X10'



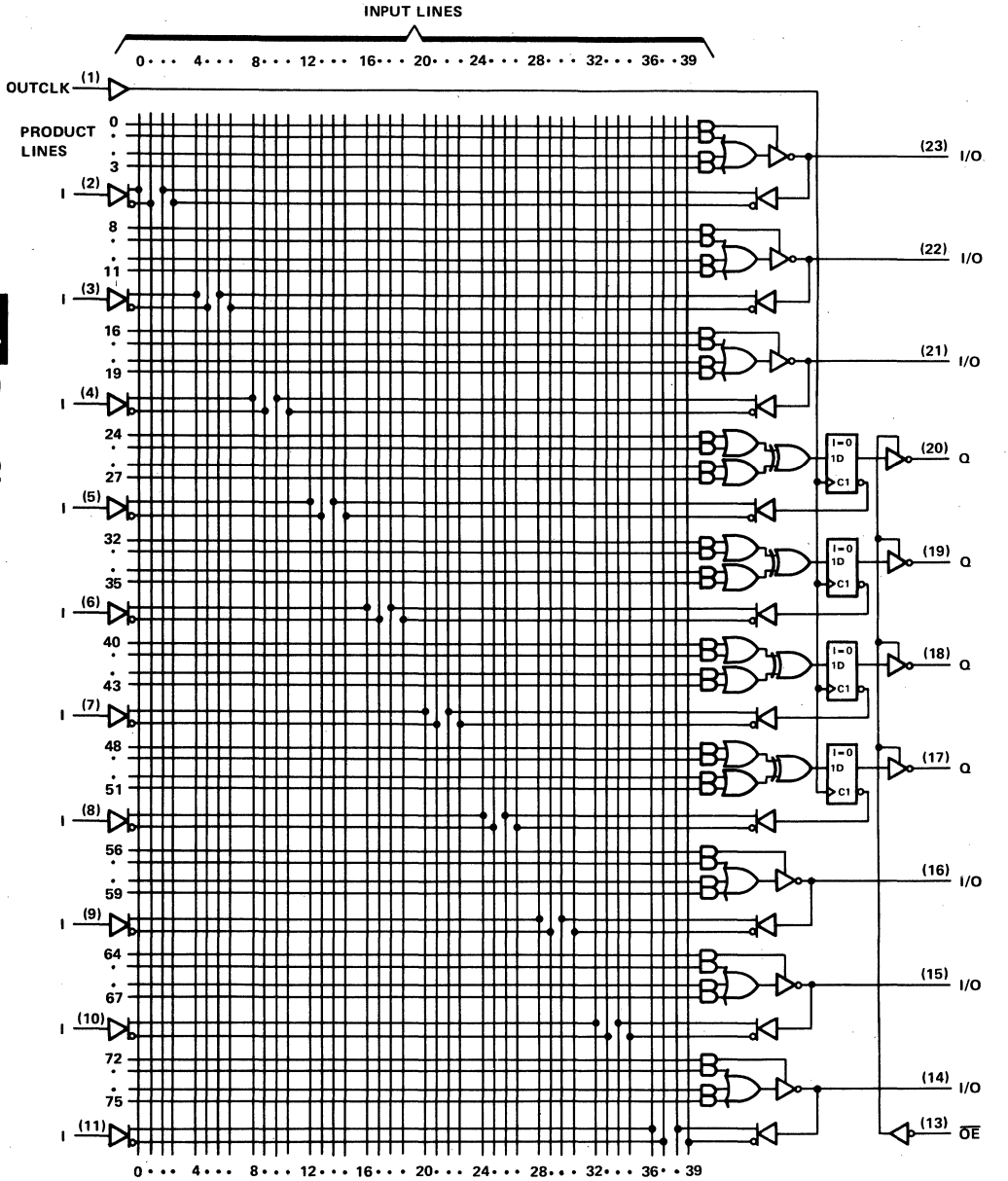
∼ denotes fused inputs

logic diagram (positive logic)



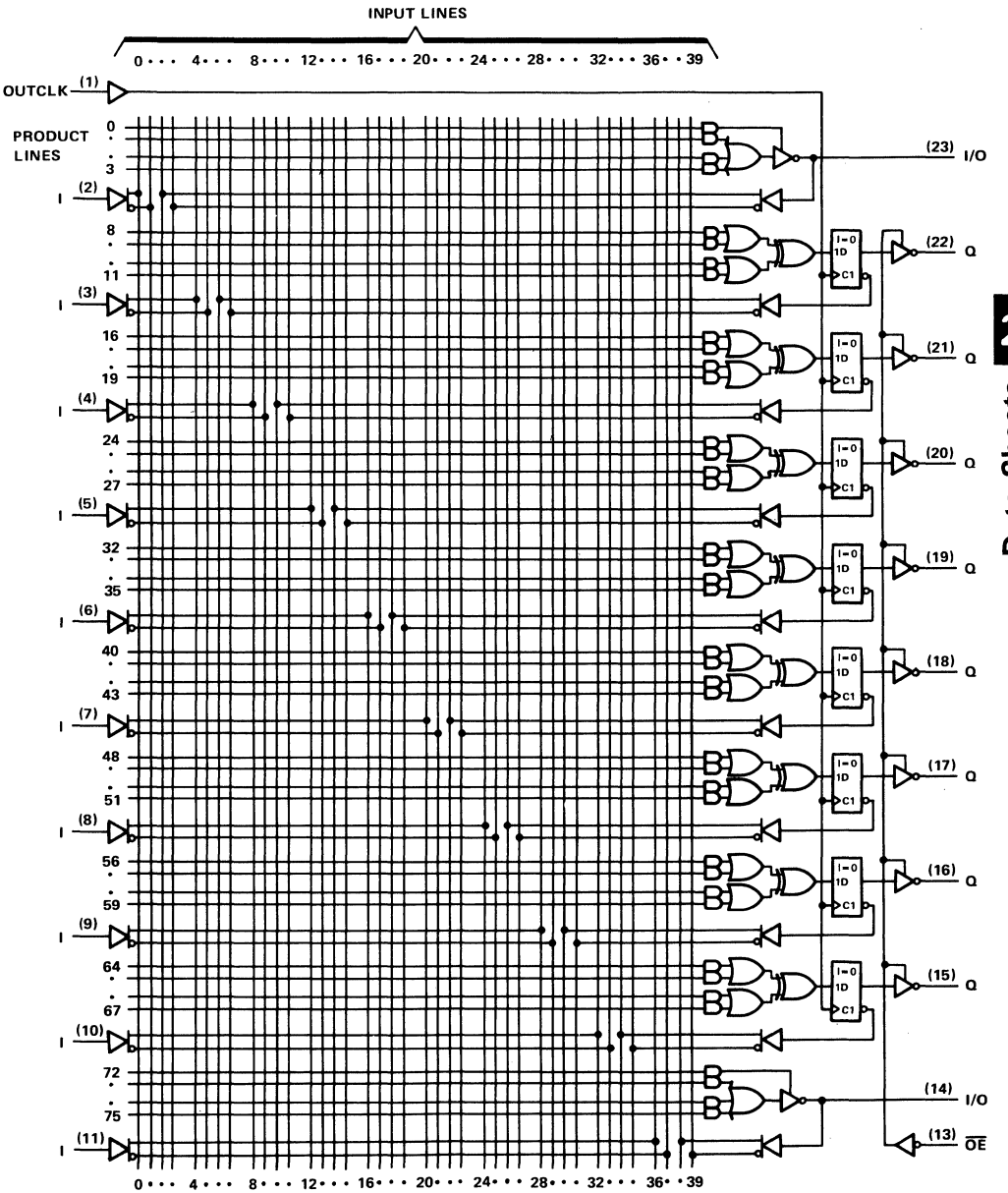
Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



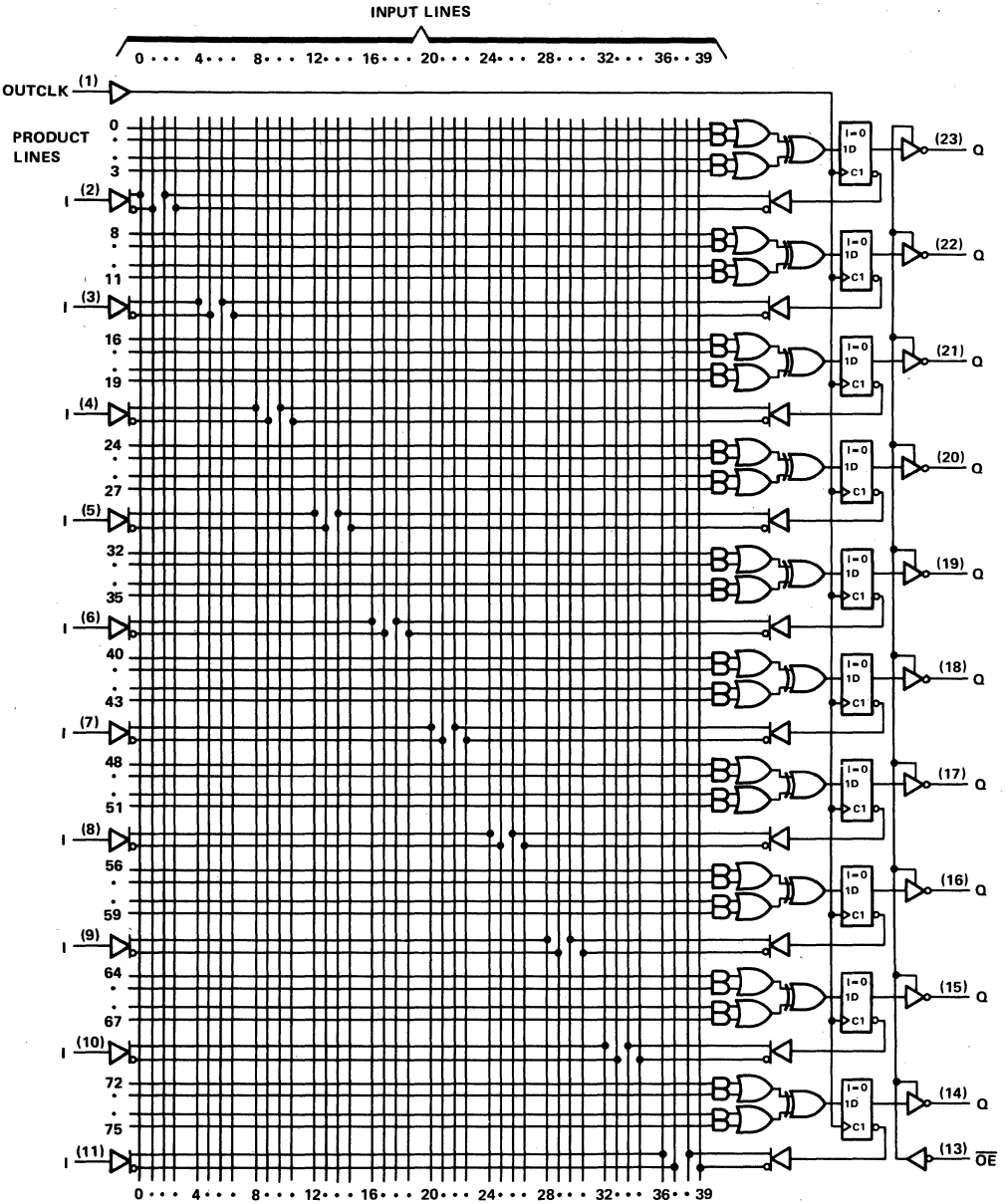
Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: C suffix . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			−30C MIN	−30C NOM	−30C MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		22.2	MHz
t_w	Pulse duration, clock, see Note 2	High	15			ns
		Low	25			
t_{su}	Setup time, input or feedback before OUTCLK↑		30			ns
t_h	Hold time, input or feedback after OUTCLK↑		0			ns
T_A	Operating free-air temperature		0		75	°C

NOTE 2: The high and low clock pulse durations cannot both be at the minimum values specified. Their sum must be equal to or greater than the minimum clock period, which is the reciprocal of the maximum recommended clock frequency.

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†		−30C MIN	−30C TYP‡	−30C MAX	UNIT
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX	2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX,	V_O = 2.7 V			20	μA
	I/O ports					100	
I_{OZL}	Outputs	V_{CC} = MAX,	V_O = 0.4 V			−20	μA
	I/O ports					−250	
I_I		V_{CC} = MAX,	V_I = 5.5 V			0.1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V			20	μA
I_{IL}		V_{CC} = MAX,	V_I = 0.4 V			−0.25	mA
I_{OS}§		V_{CC} = 5 V,	V_O = 0	−30		−130	mA
I_{CC}	'20X4, '20X8, '20X10	V_{CC} = MAX,	V_I = 0		120	180	mA
	'20L10				120	165	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	-30C			UNIT
				MIN	TYP†	MAX	
f_{max}‡	With Feedback			22.2			MHz
t_{pd}	I, I/O	O, I/O			23	30	ns
t_{pd}	OUTCLK↑	Q	R1 = 200 Ω,		10	15	ns
t_{en}	$\overline{OE}$	Q	R2 = 390 Ω,		11	20	ns
t_{dis}	$\overline{OE}$↑	Q	C_L = 50 pF		10	20	ns
t_{en}	I, I/O	O, I/O			19	30	ns
t_{dis}	I, I/O	O, I/O			15	30	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡f_{max} (with feedback) = $\frac{1}{t_{su} + t_{pd}(\text{CLK to Q})}$, f_{max} without feedback can be calculated as f_{max} (without feedback) = $\frac{1}{t_w\text{high} + t_w\text{low}}$

programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5762.

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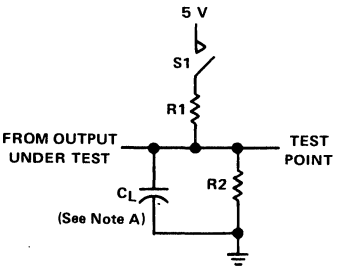
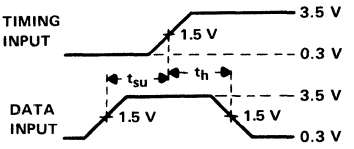
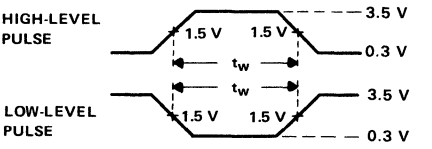
PARAMETER MEASUREMENT INFORMATION



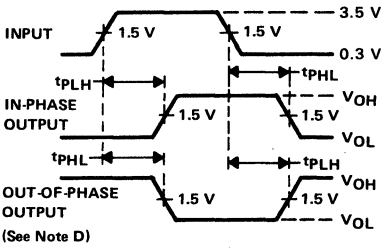
LOAD CIRCUIT FOR THREE-STATE OUTPUTS



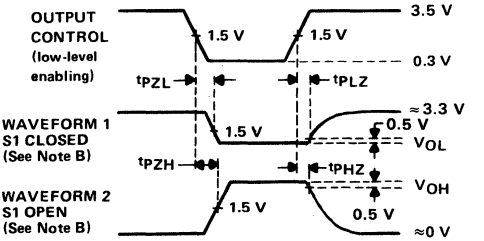
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

preload procedures

preload procedure for registered outputs

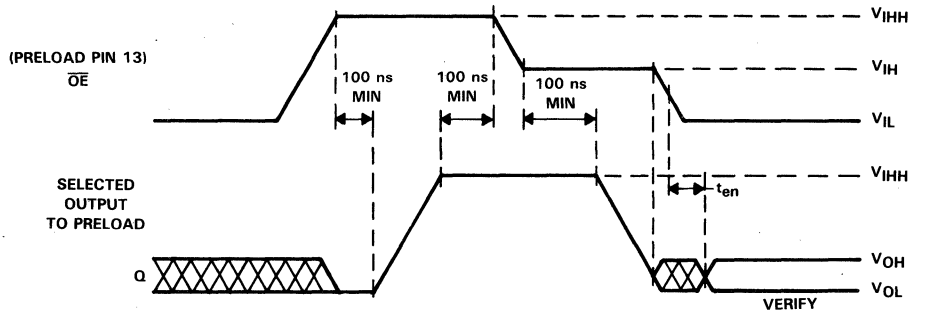
Step 1 With V_{CC} at 5 volts, raise Pin 13 ($\overline{OE}$) to V_{IHH} to disable the outputs and clear the registers (output goes low). Since the outputs are low, only high levels need be preloaded.

Step 2 Raise the selected output to be preloaded high to V_{IHH}.

Step 3 Lower Pin 13 to V_{IH}.

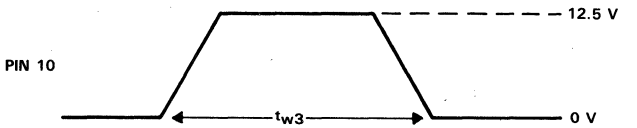
Step 4 Remove the voltages applied to the outputs. (At least a 100-ns wait is required between step 3 and step 4)

Step 5 Lower Pin 13 to V_{IL} to verify preload.



PRELOAD WAVEFORMS

security fuse programming



SECURITY FUSE PROGRAMMING WAVEFORMS

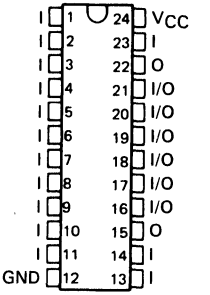
NOTE: Pin numbers shown apply only for the DIP package. If a chip carrier socket adaptor is not used, pin numbers must be changed accordingly.

D3088, DECEMBER 1987

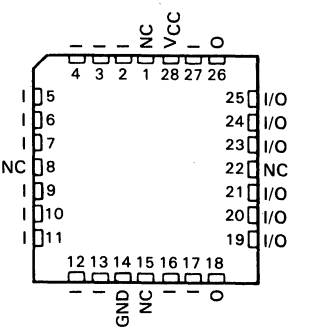
- **True Product-Term Sharing Option**
- **High-Performance Operation:**
  TIBPAL20SP8-20C tpd . . . 20 ns
  TIBPAL20SP8-30M tpd . . . 30 ns
- **Choice of Output Polarity**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	I INPUT	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PAL20SP8	14	2	0	6

TIBPAL20SP8
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20SP8
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

Pin assignments in operating mode

description

These programmable array logic devices feature high-speed product-term sharing. They combine the Advanced Low-Power Schottky technology with proven titanium-tungsten fuses. These devices will provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

Product-term sharing allows a choice of one or two outputs for any product term. The 56 product terms are grouped in multiples of 14 per output pair, not counting the 8 enable terms (1 per output). Any number of product terms (from 0 to 16) can be associated with one output. In addition, a product term may be common to two outputs. In addition to the product term sharing, these devices feature a polarity option for each output.

The TIBPAL20SP8-30M is characterized for operation over the full military temperature range of −55°C to 125°C. The TIBPAL20SP8-20C is characterized for operation from 0°C to 75°C.

IMPACT is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Monolithic Memories Inc.

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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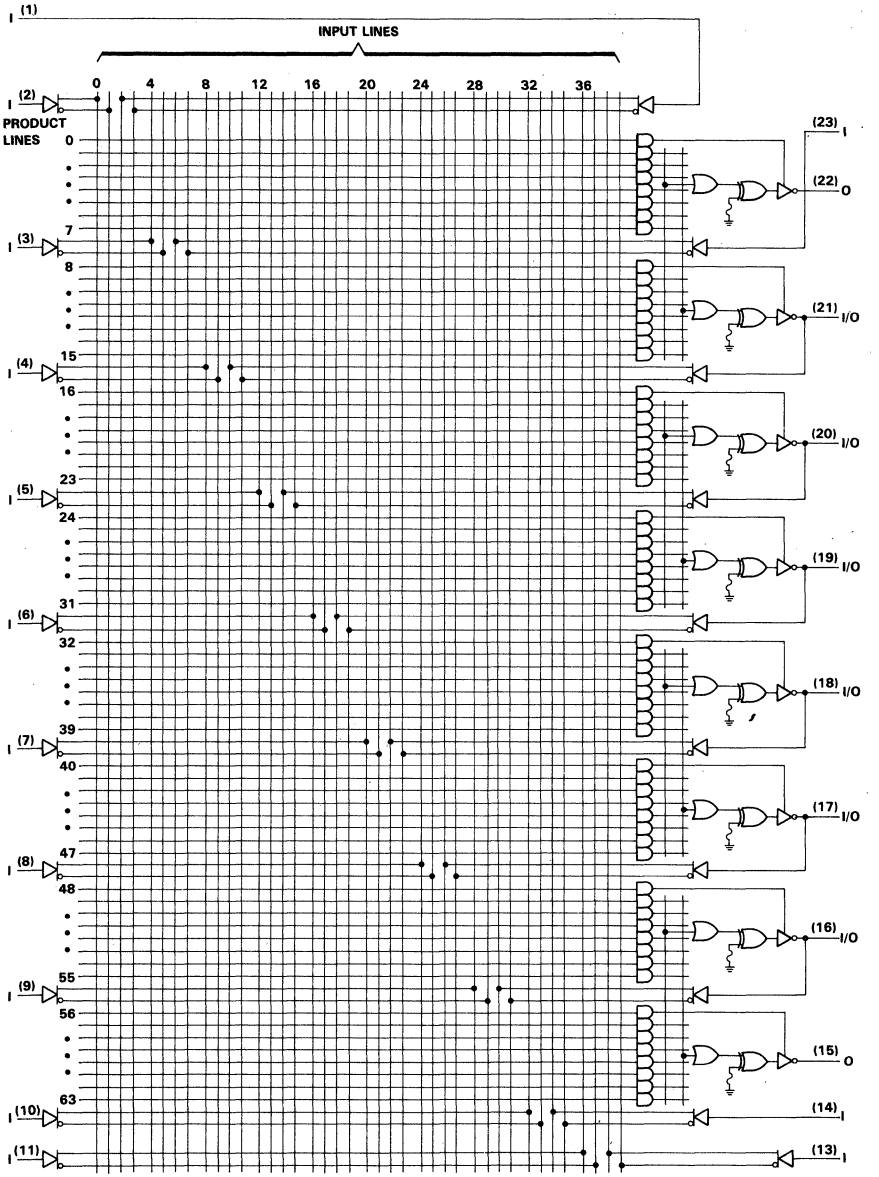
logic diagram (positive logic)



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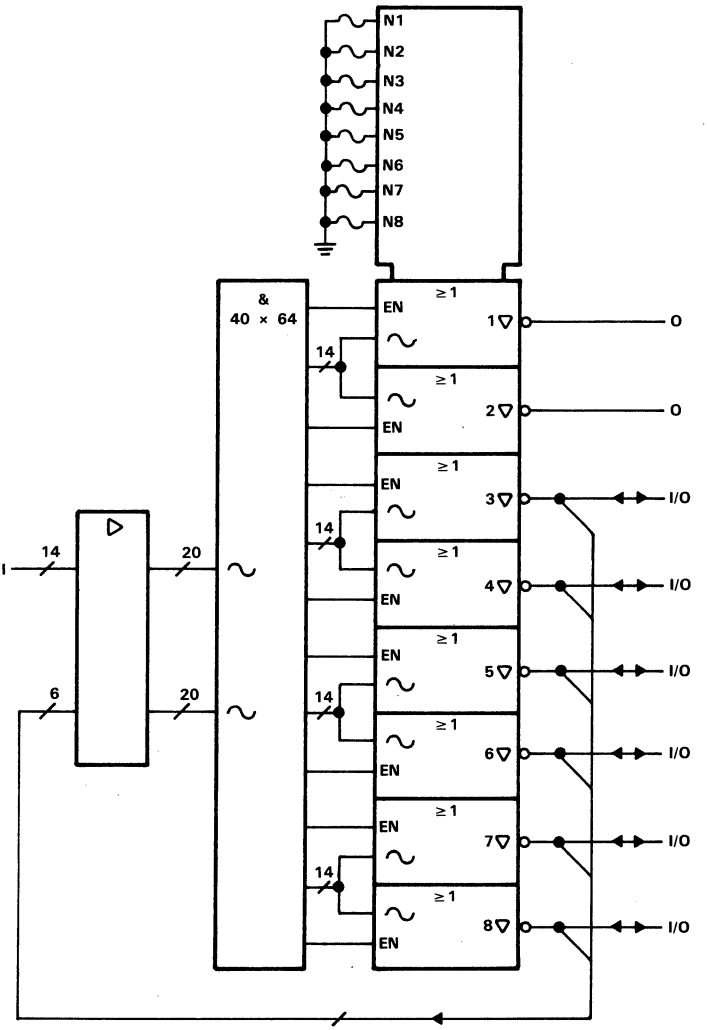
functional block diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: −30M suffix . . . . . −55°C to 125°C
−20C suffix . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating condtions

		−30M			−20C			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		75	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS†		−30M			−20C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA		−0.8	−1.5		−0.8	−1.5	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3.2		V
V_{OL}	V_{CC} = MIN,	I_{OL} = MAX		0.3	0.5		0.3	0.5	V
I_{OZH}§	V_{CC} = MAX,	V_O = 2.7 V			100			100	μA
I_{OZL}§	V_{CC} = MAX,	V_O = 0.4 V			−100			−100	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			0.2			0.2	mA
I_{IH}§	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}§	V_{CC} = MAX,	V_I = 0.4 V		−0.08	−0.25		−0.08	−0.25	mA
I_{OS}¶	V_{CC} = MAX,	V_O = 0	−30	−70	−130	−30	−70	−130	mA
I_{CC}	V_{CC} = MAX, V_I = 0	Outputs open,		140	180		140	180	mA
C_i	f = 1 MHz,	V_I = 2 V		5			5		pF
C_o	f = 1 MHz,	V_O = 2 V		6			6		pF

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.
¶Not more than one output should be shorted at at time and duration of the short-circuit should not exceed one second.

TEXAS INSTRUMENTS
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switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	−30M			−20C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	I, I/O	O, I/O	R1 = 200 Ω, R2 = 390 Ω, See Figure 1		15	30		15	20	ns
t_{en}	I, I/O	O, I/O			16	30		16	20	ns
t_{dis}	I, I/O	O, I/O			16	30		16	20	ns

programming information

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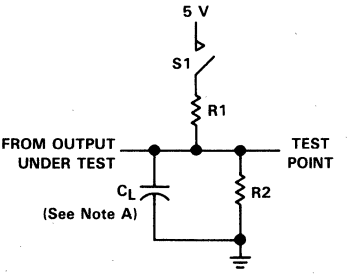
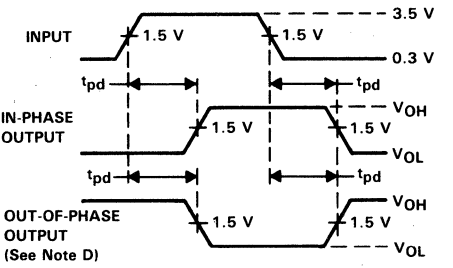
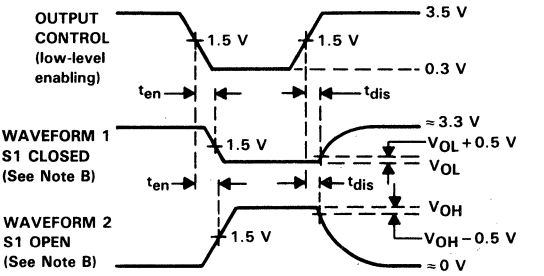
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR THREE-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

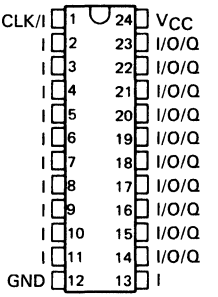
FIGURE 1

HIGH-PERFORMANCE *IMPACT™* PROGRAMMABLE ARRAY LOGIC

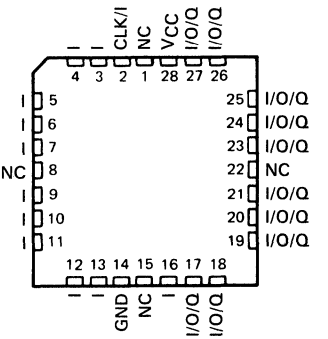
D2943, OCTOBER 1986—REVISED DECEMBER 1987

- Second Generation PAL Architecture
- Choice of Operating Speeds
  - TIBPAL22V10AC . . . 25 ns Max
  - TIBPAL22V10AM . . . 30 ns Max
  - TIBPAL22V10C . . . 35 ns Max
  - TIBPAL22V10M . . . 40 ns Max
- Increased Logic Power — Up to 22 Inputs and 10 Outputs
- Increased Product Terms — Average of 12 per Output
- Variable Product Term Distribution Allows More Complex Functions to be Implemented
- Each Output is User Programmable for Registered or Combinatorial Operation, Polarity, and Output Enable Control
- TTL-Level Preload for Improved Testability
- Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability
- Fast Programming, High Programming Yield, and Unsurpassed Reliability Ensured Using Ti-W Fuses
- AC and DC Testing Done at the Factory Utilizing Special Designed-In Test Features
- Dependable Texas Instruments Quality and Reliability
- Package Options Include Plastic and Ceramic Dual-In-Line Packages and Chip Carriers
- Functionally Equivalent to AMD AMPAL22V10 and AMPAL22V10A

M SUFFIX . . . JT PACKAGE
C SUFFIX . . . NT PACKAGE
(TOP VIEW)



M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection
Pin assignments in operating mode

description

The TIBPAL22V10 and TIPPAL22V10A are programmable array logic devices featuring high speed and functional equivalency when compared to presently available devices. They are implemented with the familiar sum-of-products (AND-OR) logic structure featuring the new concept "Programmable Output Logic Macrocell". These IMPACT™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable high-performance substitutes for conventional TTL logic.

These devices contain up to 22 inputs and 10 outputs. They incorporate the unique capability of defining and programming the architecture of each output on an individual basis. Outputs may be registered or nonregistered and inverting or noninverting as shown in the output logic macrocell diagram. The ten potential outputs are enabled through the use of individual product terms.

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PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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Further advantages can be seen in the introduction of variable product term distribution. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. This variable allocation of terms allows far more complex functions to be implemented than in previously available devices.

Circuit design is enhanced by the addition of a synchronous set and an asynchronous reset product term. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0. The output logic level after set or reset depends on the polarity selected during programming. Output registers can be preloaded to any desired state during testing. Preloading permits full logical verification during product testing.

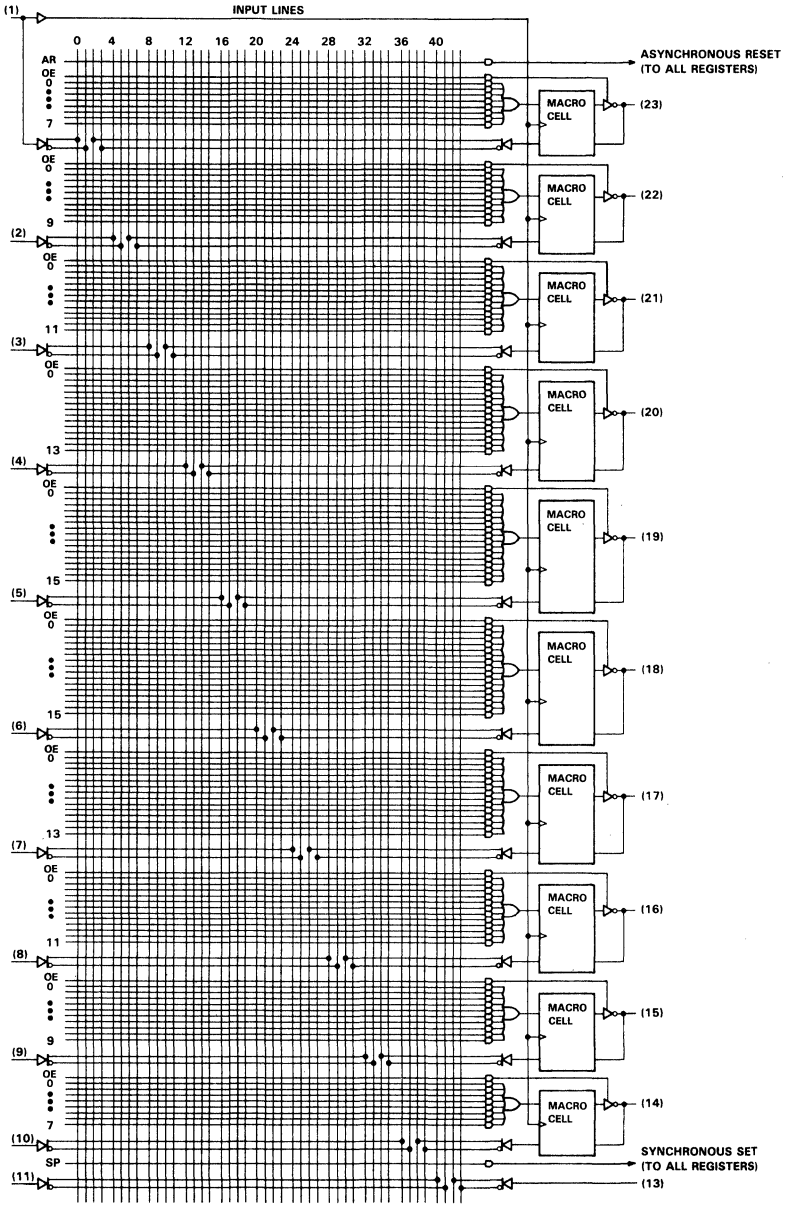
With features such as programmable output logic macrocells and variable product term distribution, the TIBPAL22V10 and TIBPAL22V10A offer quick design and development of custom LSI functions with complexities of 500 to 800 equivalent gates. Since each of the ten output pins may be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs are possible.

A power-up clear function is supplied that forces all registered outputs to a predetermined state after power is applied to the device. Registered outputs selected as active-low power-up with their outputs high. Registered outputs selected as active-high power-up with their outputs low.

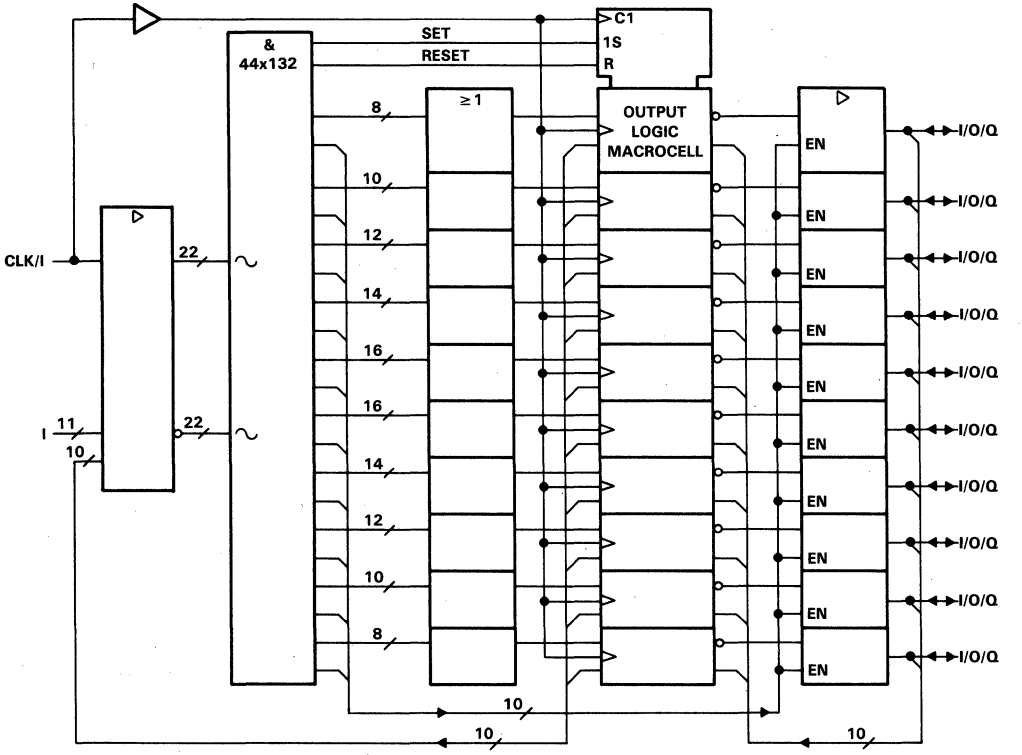
A single security fuse is provided on each device to discourage unauthorized copying of fuse patterns. Once blown, the verification circuitry is disabled and all other fuses will appear to be open.

The M suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The C suffix devices are characterized for operation from 0°C to 75°C.

logic diagram (positive logic)

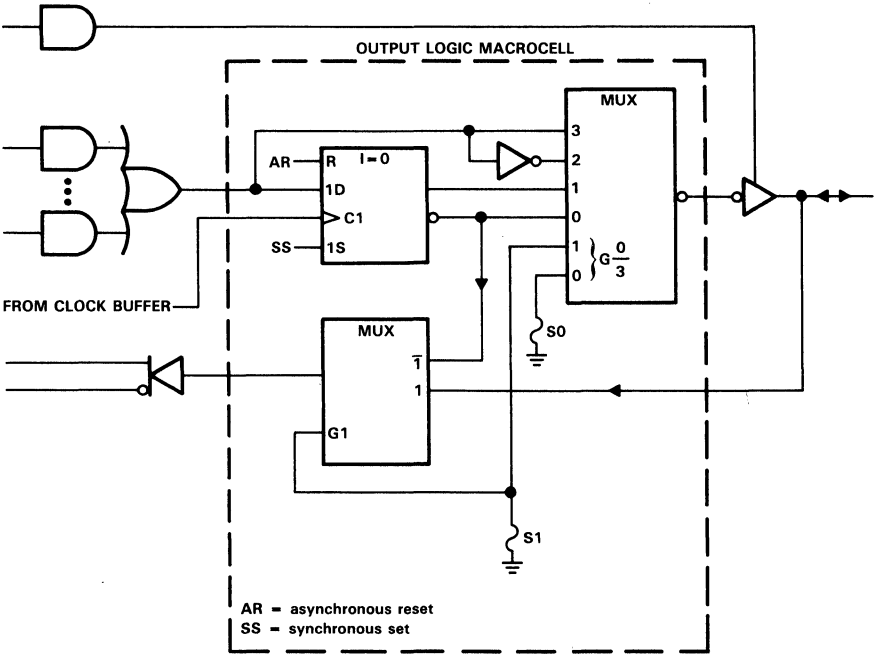


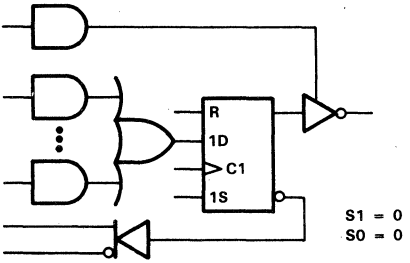
functional block diagram (positive logic)



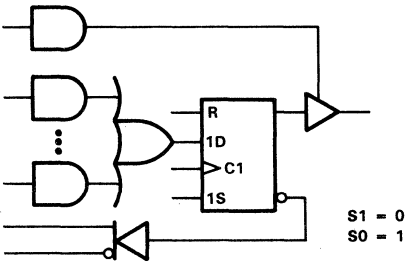
∼ denotes fused inputs

output logic macrocell diagram

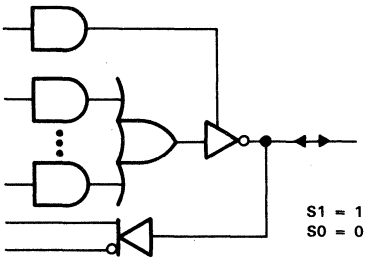




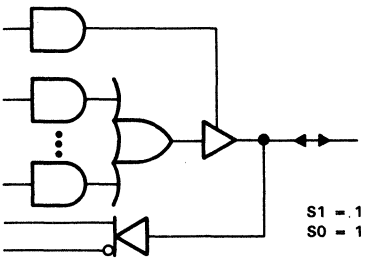
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

FUSE SELECT		FEEDBACK AND OUTPUT CONFIGURATION		
S1	S0			
0	0	Register feedback	Registered	Active low
0	1	Register feedback	Registered	Active high
1	0	I/O feedback	Combinational	Active low
1	1	I/O feedback	Combinational	Active high

0 = unblown fuse, 1 = blown fuse
S1 and S0 are select-function fuses as shown in the output logic macrocell diagram.

FIGURE 1. RESULTANT MACROCELL FEEDBACK AND OUTPUT LOGIC AFTER PROGRAMMING

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a pre-load cycle.

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recommended operating conditions

			TIBPAL22V10M			TIBPAL22V10C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			16	mA
f_{clock}	Clock frequency†				16.5			18	MHz
t_w	Pulse duration	Clock high or low	30			25			ns
		Asynchronous Reset high or low	40			35			
t_{su}	Setup time before clock↑	Input	35			30			ns
		Feedback	35			30			
		Synchronous Set	35			30			
		Asynchronous Reset low (inactive)	40			35			
t_h	Hold time, input, set, or feedback after clock↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		75	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS‡		TIBPAL22V10M			TIBPAL22V10C			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX	2.4	3.5		2.4	3.5		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX		0.25	0.5		0.35	0.5	V
I_{OZH}		V_{CC} = MAX,	V_O = 2.7 V			0.1			0.1	mA
I_{OZL}	Any output	V_{CC} = MAX,	V_O = 0.4 V			−100			−100	μA
	Any I/O					−250			−250	
I_I		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}		V_{CC} = MAX,	V_I = 0.4 V			−0.25			−0.25	mA
I_{OS}¶		V_{CC} = MAX,	V_O = 0.5 V	−30		−90	−30		−90	mA
I_{CC}		V_{CC} = MAX,	V_I = GND, Outputs open		120	180		120	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	TIBPAL22V10M			TIBPAL22V10C			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
f_{max}†	With feedback		C_L = 50 pF	16.5			18			MHz
t_{pd}	I, I/O	I/O	R1 = 300 Ω for C suffix,		15	40		15	35	ns
t_{pd}	I,I/O (reset)	Q	R1 = 390 Ω for M suffix,		15	45		15	40	ns
t_{pd}	Clock	Q	R2 = 390 Ω for C suffix,		10	25		10	25	ns
t_{en}	I, I/O	I/O, Q	R2 = 750 Ω for M suffix,		15	40		15	35	ns
t_{dis}	I, I/O	I/O, Q	See Figure 2		15	40		15	35	ns

† f_{max} and f_{clock} (with feedback) $= \frac{1}{t_{su} + t_{pd}\ (CLK\ to\ Q)}$. f_{max} and f_{clock} without feedback can be calculated as f_{max} and f_{clock} (without feedback) $= \frac{1}{t_w\ high + t_w\ low}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test problems caused by test equipment ground degradation.

recommended operating conditions

			TIBPAL22V10AM			TIBPAL22V10AC			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			16	mA
f_{clock}	Clock frequency†				22			28.5	MHz
t_w	Pulse duration	Clock high or low	20			15			ns
		Asynchronous Reset high or low	30			25			
t_{su}	Setup time before clock↑	Input	25			20			ns
		Feedback	25			20			
		Synchronous Set	25			20			
		Asynchronous Reset low (inactive)	30			25			
t_h	Hold time, input, set, or feedback after clock↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		75	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS‡		TIBPAL22V10AM			TIBPAL22V10AC			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX	2.4	3.5		2.4	3.5		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX		0.25	0.5		0.35	0.5	V
I_{OZH}		V_{CC} = MAX,	V_O = 2.7 V			0.1			0.1	mA
I_{OZL}	Any output	V_{CC} = MAX,	V_O = 0.4 V			−100			−100	μA
	Any I/O					−250			−250	
I_I		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}		V_{CC} = MAX,	V_I = 0.4 V			−0.25			−0.25	mA
I_{OS}§		V_{CC} = MAX,	V_O = 0.5 V	−30		−90	−30		−90	mA
I_{CC}		V_{CC} = MAX,	V_I = GND, Outputs open		120	180		120	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	TIBPAL22V10AM			TIBPAL22V10AC			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
f_{max}†	With feedback		C_L = 50 pF	22			28.5			MHz
t_{pd}	I, I/O	I/O	R1 = 300 Ω for C suffix,		15	30		15	25	ns
t_{pd}	I, I/O (reset)	Q	R1 = 390 Ω for M suffix,		15	35		15	30	ns
t_{pd}	Clock	Q	R2 = 390 Ω for C suffix,		10	20		10	15	ns
t_{en}	I, I/O	Q	R2 = 750 Ω for M suffix,		15	30		15	25	ns
t_{dis}	I, I/O	Q	See Figure 2		15	30		15	25	ns

† f_{max} and f_{clock} (with feedback) $= \frac{1}{t_{su} + t_{pd\ (CLK\ to\ Q)}}$. f_{max} and f_{clock} without feedback can be calculated as f_{max} and

$f_{clock}\ (without\ feedback) = \frac{1}{t_w\ high + t_w\ low}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test problems caused by test equipment ground degradation.

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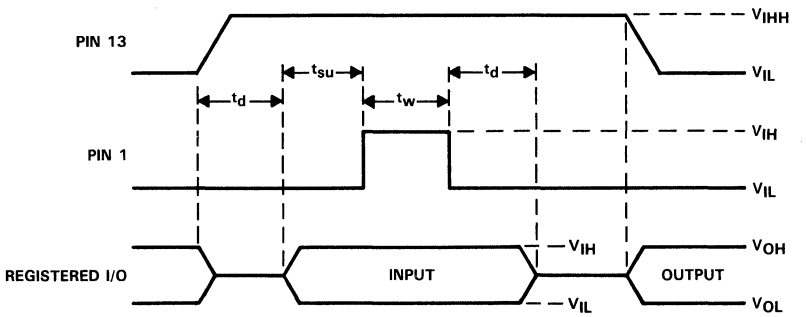
preload procedure for registered outputs (see Note 2)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and pin 1 at V_{IL}, raise pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

preload waveforms (see Notes 2 and 3)

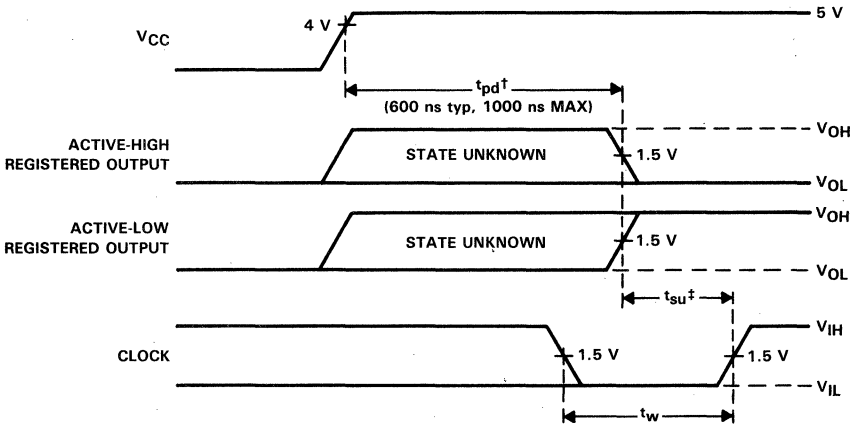


NOTES: 2. Pin numbers shown are for JT and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_w$ = 100 ns to 1000 ns. V_{IHH} = 10.25 V to 10.75 V.

power-up reset

Following power-up, all registers are reset to zero. The output level depends on the polarity selected during programming. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the V_{CC}'s rise be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.

power-up reset waveforms



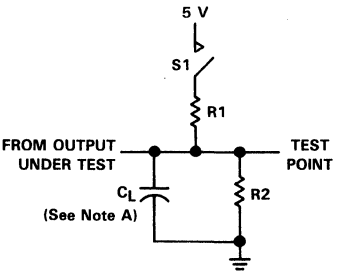
† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

programming information

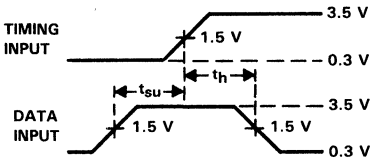
Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5762.

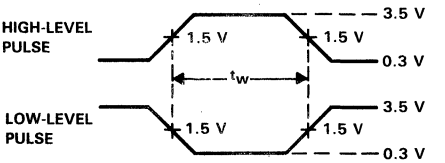
PARAMETER MEASUREMENT INFORMATION



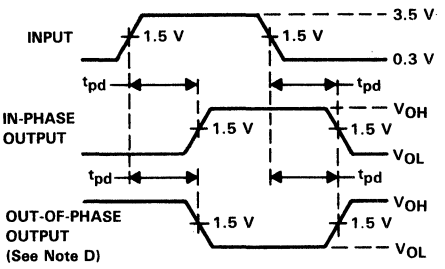
LOAD CIRCUIT FOR THREE-STATE OUTPUTS



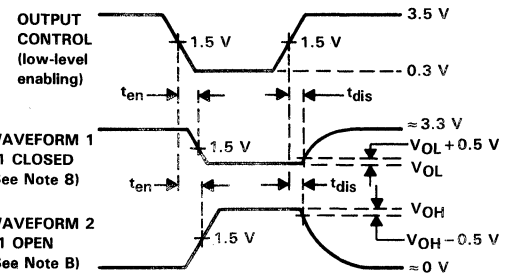
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 2

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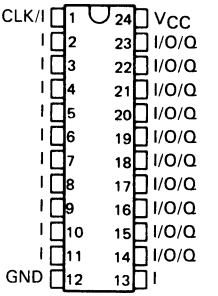
HIGH-PERFORMANCE *IMPACT*™ PROGRAMMABLE ARRAY LOGIC

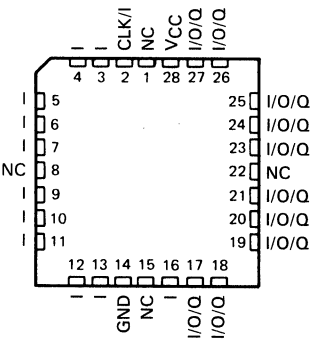
D2943, FEBRUARY 1987—REVISED DECEMBER 1987

- **Functionally Equivalent to the TIBPAL22V10/10A, with Additional Feedback Paths in the Output Logic Macrocell**
- **Choice of Operating Speeds:**
  TIBPAL22VP10-20C . . . 20 ns Max
  TIBPAL22VP10-25M . . . 25 ns Max
- **Variable Product Term Distribution Allows More Complex Functions to be Implemented**
- **Polarity of Each Output is Programmable**
- **TTL-Level Preload for Improved Testability**
- **Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability**
- **Fast Programming, High Programming Yield, and Unsurpassed Reliability Ensured Using Ti-W Fuses**
- **AC and DC Testing Done at the Factory Utilizing Special Designed-In Test Features**
- **Dependable Texas Instruments Quality and Reliability**
- **Package Options Include Plastic and Ceramic Dual-In-Line Packages and Chip Carriers**

M SUFFIX . . . JT PACKAGE
C SUFFIX . . . NT PACKAGE
(TOP VIEW)



M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection
Pin assignments in operating mode

description

The TIBPAL22VP10 is equivalent to the TIBPAL22V10A but offers additional flexibility in the output structure. The improved output macrocell uses the registered outputs as inputs when in a high-impedance condition. This provides two additional output configurations for a total of six possible macrocell configurations all of which are shown in Figure 1.

The device contains up to twenty-two inputs and ten outputs. It defines and programs the architecture of each output on an individual basis. Outputs may be registered or nonregistered and inverting or noninverting. In addition, the data may be fed back into the array from either the register or the I/O port. The ten potential outputs are enabled through the use of individual product terms.

Further advantages can be seen in the introduction of variable product term distribution. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. This variable allocation of terms allows far more complex functions to be implemented than in previously available devices.

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Circuit design is enhanced by the addition of a synchronous set and an asynchronous reset product term. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0. The output logic level after set or reset depends on the polarity selected during programming. Output registers can be preloaded to any desired state during testing. Preloading permits full logical verification during product testing.

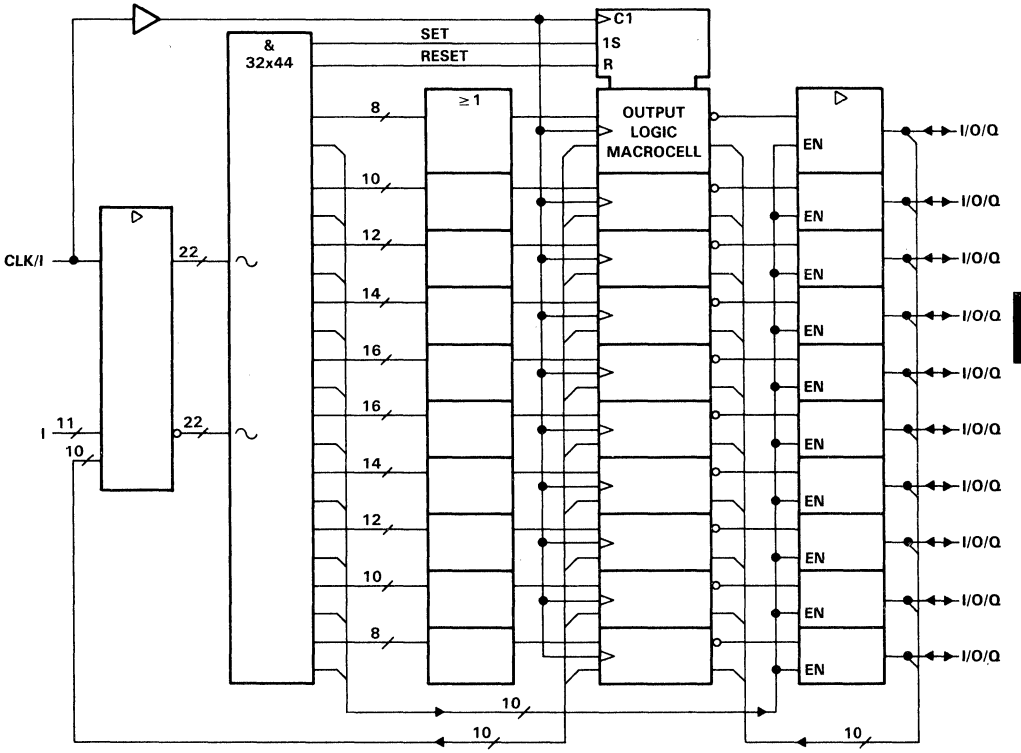
With features such as programmable output logic macrocells and variable product terms, the TIBPAL22VP10 offers quick design and development of custom LSI functions with complexities of 500 to 800 equivalent gates. Since each of the ten output pins may be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs are possible.

A power-up clear function is supplied that forces all registered outputs to a predetermined state after power is applied to the device. Registered outputs selected as active-low power-up with their outputs high. Registered outputs selected as active-high power-up with their outputs low.

A single security fuse is provided on each device to discourage unauthorized copying of fuse patterns. Once blown, the verification circuitry is disabled and all other fuses will appear to be open.

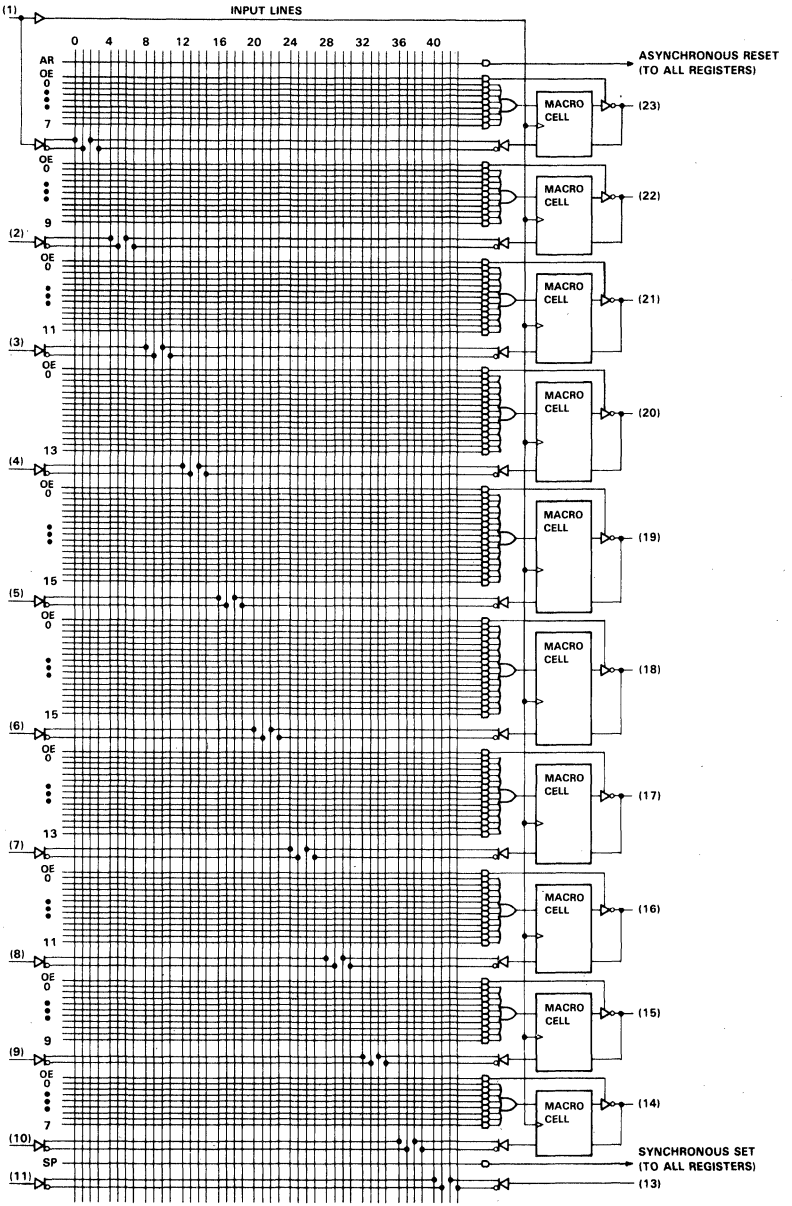
The TIBPAL22VP10-25M is characterized for operation over the full military temperature range of −55 °C to 125 °C. The TIBPAL22VP10-20C is characterized for operation from 0 °C to 75 °C.

functional block diagram (positive logic)



∿ denotes fused inputs

logic diagram (positive logic)



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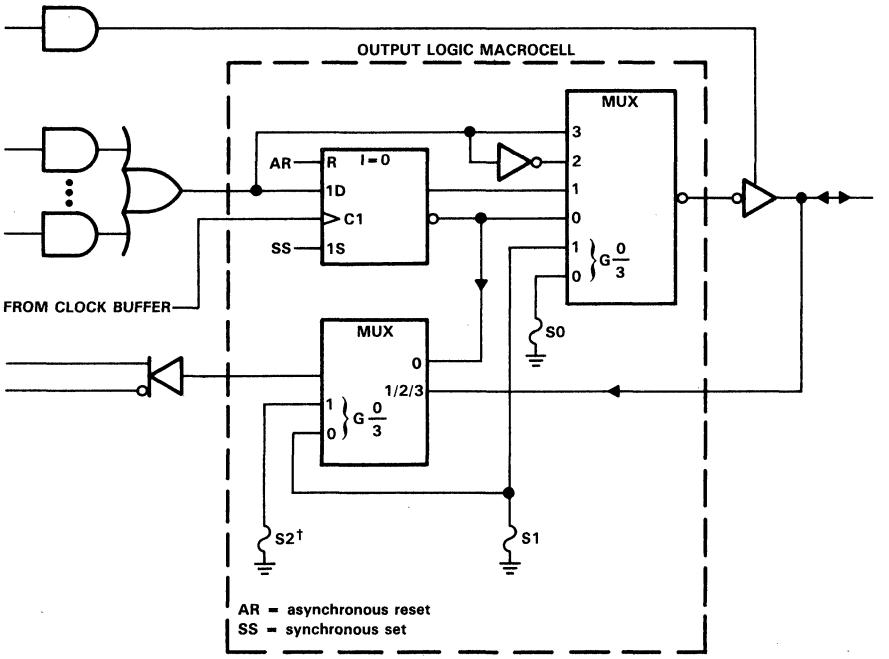
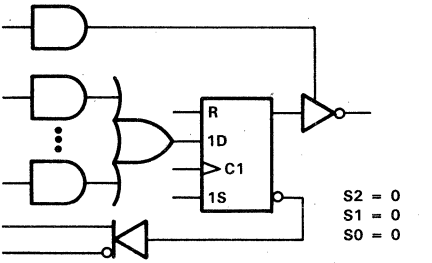
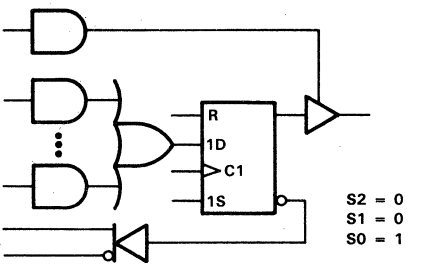
output logic macrocell diagram



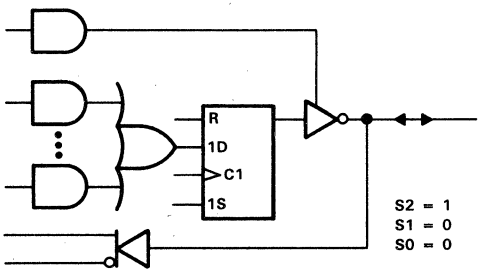
† This fuse is unique to the Texas Instruments TIBPAL22VP10. It allows feedback from the I/O port using registered outputs as shown in the macrocell fusing logic function table.



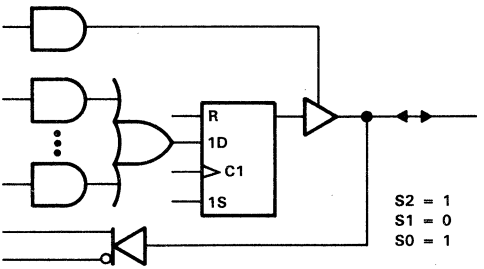
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



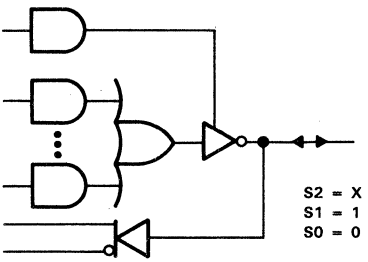
REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT



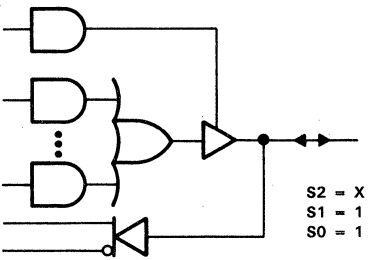
I/O FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT†



I/O FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT†



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

† These configurations are unique to the TIBPAL22VP10 and provide added flexibility when comparing it to the TIBPAL22V10 or TIBPAL22V10A.

FIGURE 1. RESULTANT MACROCELL FEEDBACK AND OUTPUT LOGIC AFTER PROGRAMMING

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MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

PROGRAM-FUSE SELECT			FEEDBACK AND OUTPUT CONFIGURATION		
S2	S1	S0			
0	0	0	Register feedback	Registered	Active low
0	0	1	Register feedback	Registered	Active high
1	0	0	I/O feedback	Registered	Active low
1	0	1	I/O feedback	Registered	Active high
X	1	0	I/O feedback	Combinational	Active low
X	1	1	I/O feedback	Combinational	Active high

0 = unblown fuse, 1 = blown fuse, X = unblown or blown fuse
S2, S1, and S0 are select-function fuses as shown in the output logic macrocell diagram.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: TIBPAL22VP10-25M . . . . . −55°C to 125°C
TIBPAL22VP10-20C . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a pre-load cycle.

recommended operating conditions

			TIBPAL22VP10-25M			TIBPAL22VP10-20C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			16	mA
f_{clock}	Clock frequency†				25			37	MHz
t_w	Pulse duration	Clock high or low	20			10			ns
		Reset high	30			20			
t_{su}	Setup time before clock↑	Input	25			15			ns
		Feedback	25			15			
		Preset	25			15			
		Reset low (inactive)	30			20			
t_h	Hold time, input, preset, or feedback after clock↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		75	°C

† f_{clock} (with feedback) $= \dfrac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, f_{clock} without feedback can be calculated as

f_{clock} (without feedback) $= \dfrac{1}{t_w \text{ high} + t_w \text{ low}}$.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS†		TIBPAL22VP10-25M			TIBPAL22VP10-20C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX	2.4	3.5		2.4	3.5		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX		0.25	0.5		0.35	0.5	V
I_{OZH}		V_{CC} = MAX,	V_O = 2.7 V			0.1			0.1	mA
I_{OZL}	Any output	V_{CC} = MAX,	V_O = 0.4 V			−100			−100	μA
	Any I/O					−250			−250	
I_I		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}		V_{CC} = MAX,	V_I = 0.4 V			−0.25			−0.25	mA
I_{OS}§		V_{CC} = MAX,	V_O = 0.5 V	−30		−90	−30		−90	mA
I_{CC}		V_{CC} = MAX,	V_I = GND, Outputs open		140	220		140	210	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)¶

PARAMETER	FROM	TO	TEST CONDITIONS	TIBPAL22VP10-25M			TIBPAL22VP10-20C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}¶			C_L = 50 pF,	25	50		37	50		MHz
t_{pd}	I, I/O	I/O	R1 = 300 Ω for C suffix,		12	25		12	20	ns
t_{pd}	I, I/O (reset)	Q	R1 = 390 Ω for M suffix,		12	25		12	20	ns
t_{pd}	Clock	Q	R2 = 390 Ω for C suffix,		8	15		8	12	ns
t_{en}	I, I/O	Q	R2 = 750 Ω for M suffix,		12	25		12	20	ns
t_{dis}	I, I/O	Q	See Figure 2		12	25		12	20	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test problems caused by test equipment ground degradation.

¶ f_{max} (with feedback) $= \dfrac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, f_{max} without feedback can be calculated as

f_{max} (without feedback) $= \dfrac{1}{t_w\ \text{high} + t_w\ \text{low}}$.

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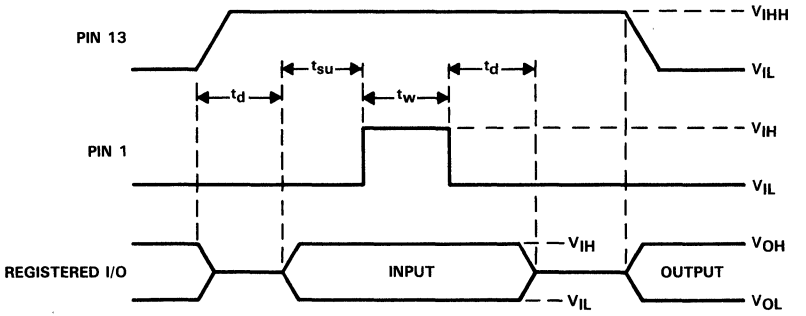
preload procedure for registered outputs (see Note 2)

The output registers of the TIBPAL22VP10 can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and pin 1 at V_{IL}, raise pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

preload waveforms (see Notes 2 and 3)

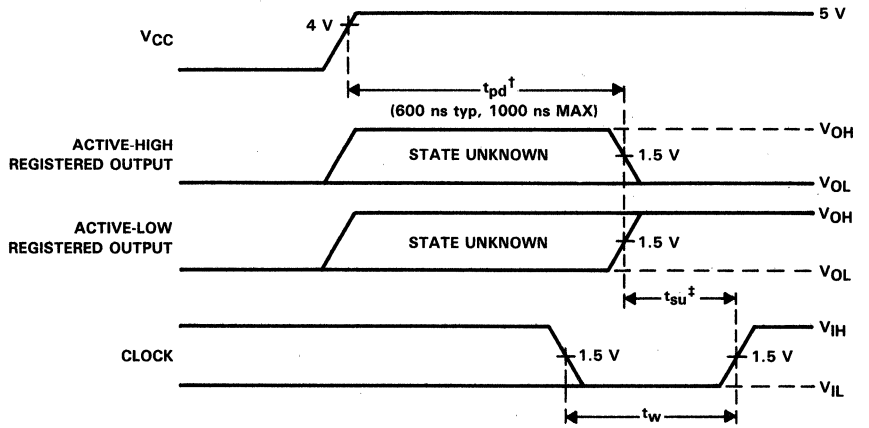


NOTES: 2. Pin numbers shown are for JT and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_w$ = 100 ns to 1000 ns. V_{IHH} = 10.25 V to 10.75 V.

power-up reset

Following power-up, all registers of the TIBPAL22VP10 are reset to zero. The output level depends on the polarity selected during programming. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the V_{CC}'s rise be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.

power-up reset waveforms



†This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡This is the setup time for input or feedback.

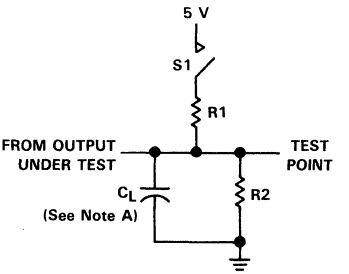
programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

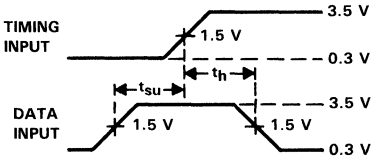
When the additional fuses are not being used, the TIBPAL22VP10 can be programmed using the TIBPAL22V10/10A programming algorithm. The fuse configuration data can either be from a JEDEC file (format per JEDEC Standard No. 3-A) or a TIBPAL22V10/10A master.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 995-5762.

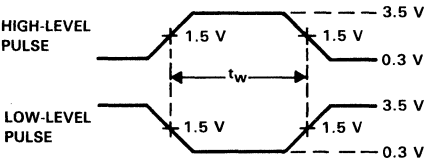
PARAMETER MEASUREMENT INFORMATION



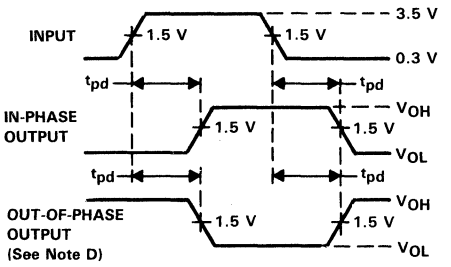
LOAD CIRCUIT FOR
THREE-STATE OUTPUTS



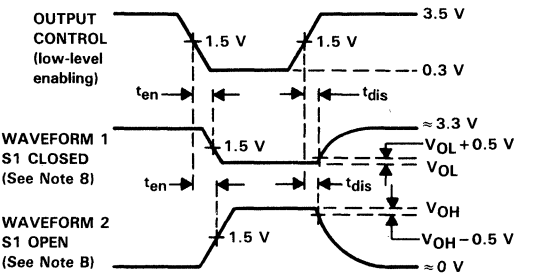
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

FIGURE 2

TIBPALR19L8M, TIBPALR19R4M, TIBPALR19R6M, TIBPALR19R8M
TIBPALR19L8C, TIBPALR19R4C, TIBPALR19R6C, TIBPALR19R8C
HIGH-PERFORMANCE LATCHED-INPUT *PAL*® CIRCUITS

D2709, DECEMBER 1982—REVISED DECEMBER 1987

- **High-Performance Operation . . . 30 MHz**
- **Preload Capability on Output Registers**
- **DIP Options Include Both 300-mil Plastic and 600-mil Ceramic**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	I/D INPUTS	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PALR19L8	11	2	2	0	6
'PALR19R4	11	0	0	4 (3-state buffers)	4
'PALR19R6	11	0	0	6 (3-state buffers)	2
'PALR19R8	11	0	0	8 (3-state buffers)	0

description

These programmable array logic devices feature high speed and functionality similar to the TIBPAL16L8, 16R4, 16R6, 16R8 series, but with the added advantage of D-type input registers. If any input register is not desired, it can be converted to an input buffer by simply programming the architectural fuse.

Combining Advanced Low-Power Schottky† technology, with proven titanium-tungsten fuses, these devices will provide reliable high performance substitutes over conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

An M suffix designates full-temperature circuits that are characterized for operation over the full military temperature range of −55°C to 125°C. A C suffix designates commercial-temperature circuits that are characterized for operation from 0°C to 70°C.

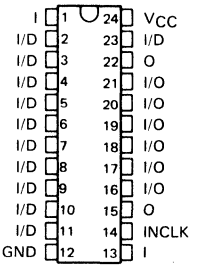
INPUT REGISTER FUNCTION TABLE

INPUT		OUTPUT OF
INCLK	D	INPUT REGISTER
↑	H	H
↑	L	L
L	X	Q_0

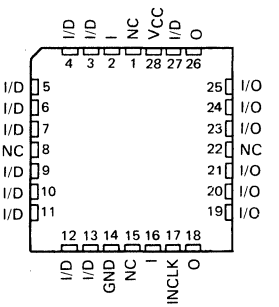
† Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

PAL is a registered trademark of Monolithic Memories Inc.

TIBPALR19L8'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



TIBPALR19L8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

Pin assignments in operating mode

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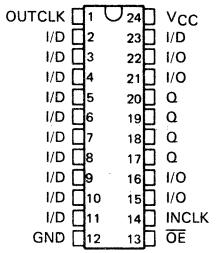
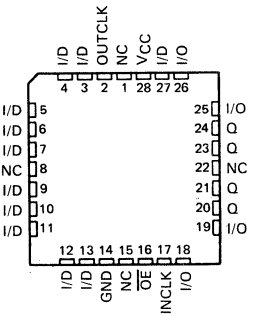
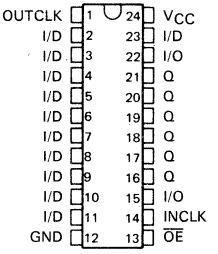
TIBPALR19R4'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



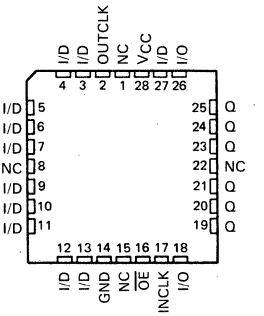
TIBPALR19R4'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



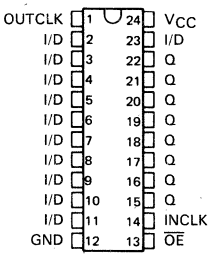
TIBPALR19R6'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



TIBPALR19R6'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)

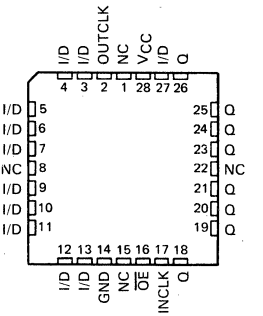


TIBPALR19R8'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



Pin assignments in operating mode

TIBPALR19R8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

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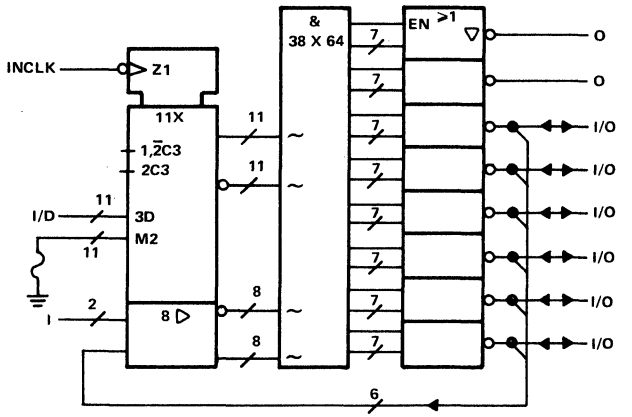
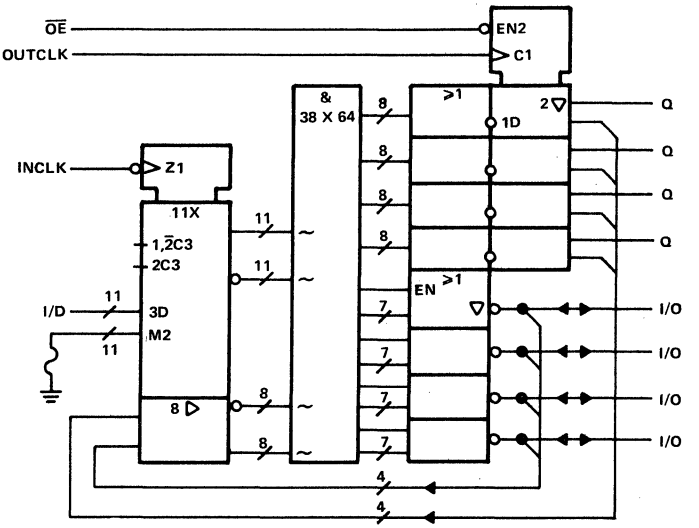
functional block diagrams (positive logic)

'PALR19L8

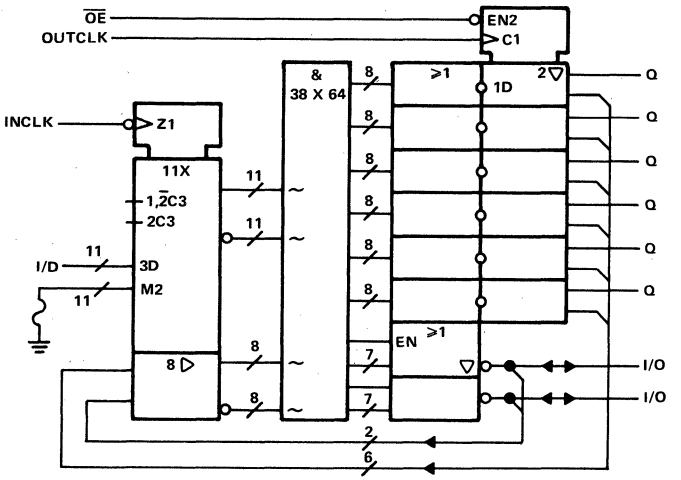


'PALR19R4

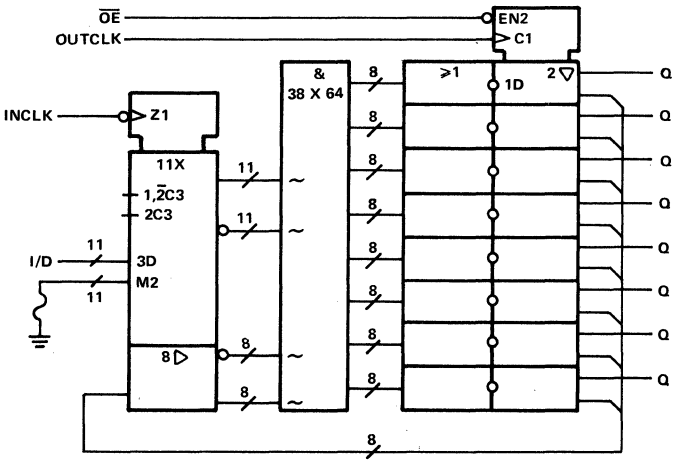


functional block diagrams (positive logic)

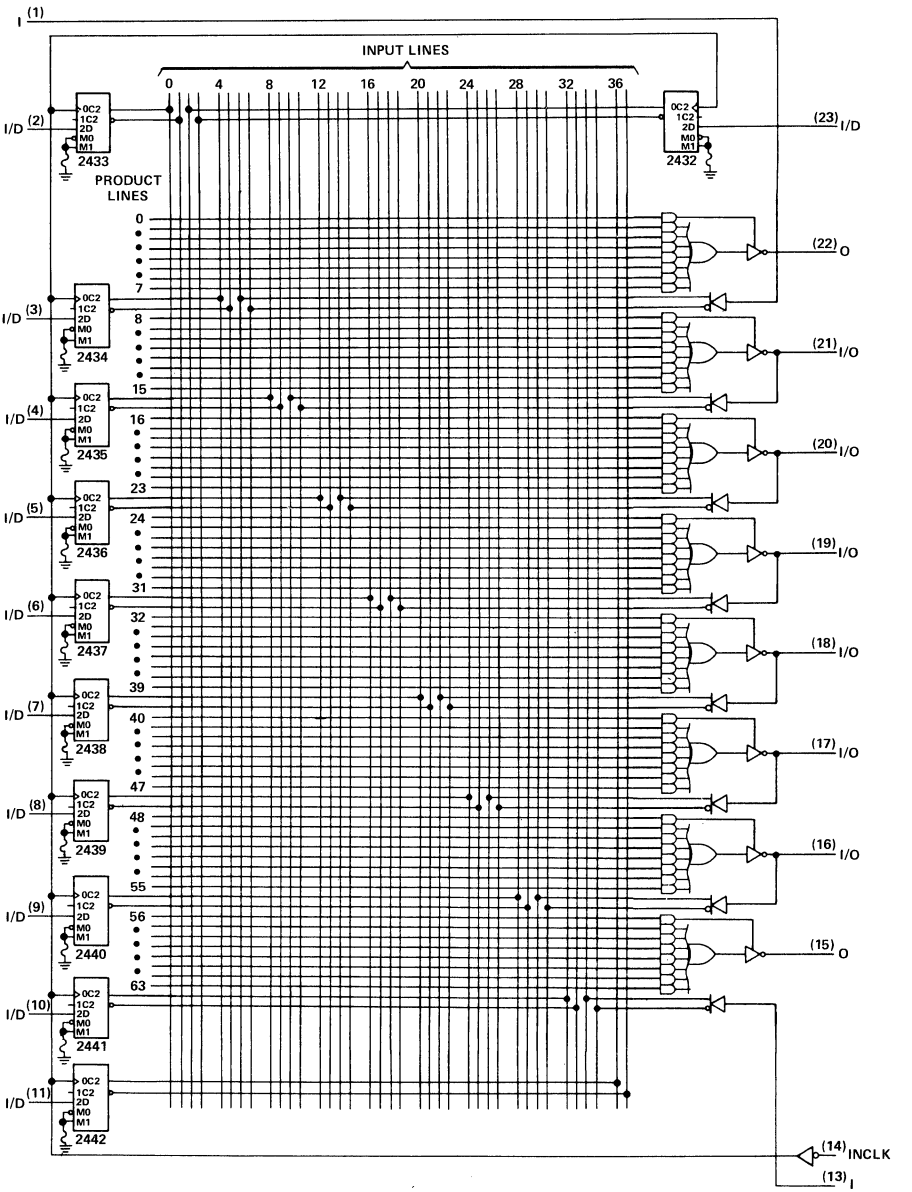
'PALR19R6



'PALR19R8

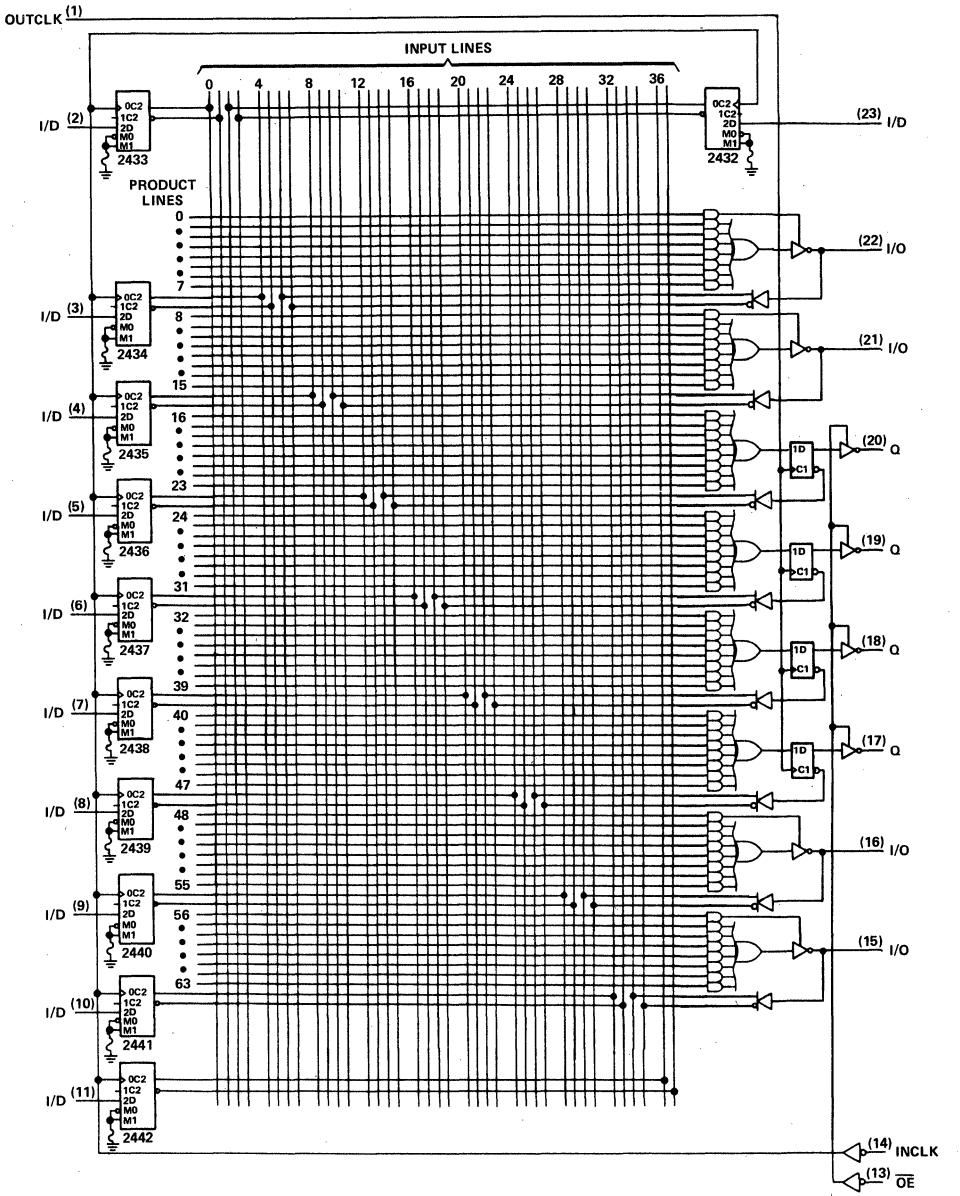


logic diagram (positive logic)



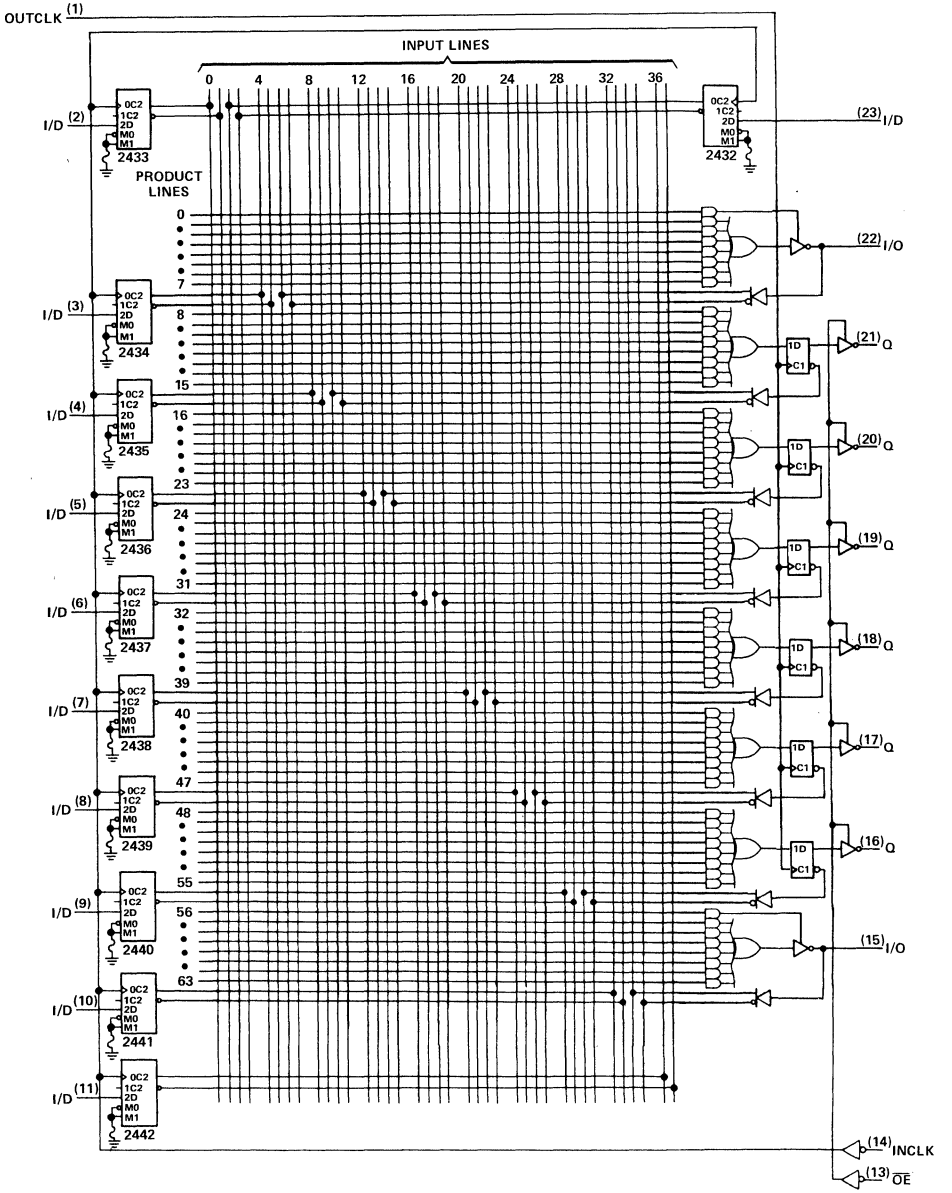
Pin numbers shown are for JW and NT packages.

logic diagram (positive logic)



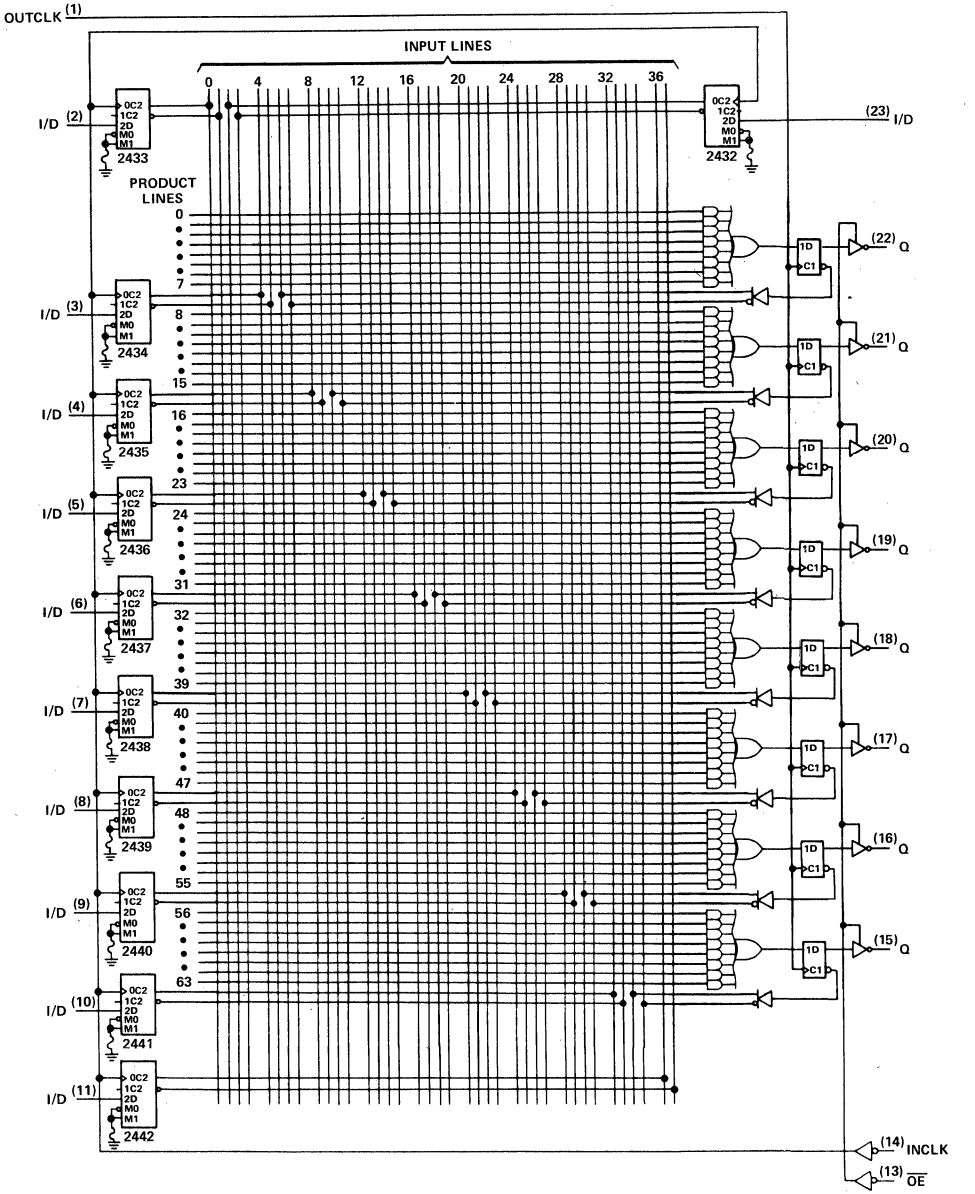
Pin numbers shown are for JW and NT packages.

logic diagram (positive logic)



Pin numbers shown are for JW and NT packages.

logic diagram (positive logic)



Pin numbers shown are for JW and NT packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during preload cycle.

recommended operating conditions

			M SUFFIX			C SUFFIX			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency	INCLK	0		20	0		30	MHz
		OUTCLK	0		20	0		30	
t_w	Pulse duration, clock	INCLK high	20			15			ns
		INCLK low	20			15			
		OUTCLK high	20			15			
		OUTCLK low	20			15			
t_{su}	Setup time	Data before INCLK↑	15			10			ns
		Data before OUTCLK↑	30			25			
		INCLK↑ before OUTCLK↑ (See Note 2)	30			25			
t_h	Hold time	Data after INCLK↑	5			5			ns
		Data after OUTCLK↑	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTE 2: This setup time ensures the output registers will see stable data from the input registers.

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†		M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	μA
	I/O ports					100			100	
I_{OZL}	Outputs	V_{CC} = MAX,	V_{IH} = 0.4 V			−20			−20	μA
	I/O ports					−250			−250	
I_I	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 5.5 V			0.2			0.2	mA
	I/D Inputs					0.1			0.1	
	All others					0.1			0.1	
I_{IH}	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
	I/D Inputs					20			20	
	All others					20			20	
I_{IL}	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
	I/D Inputs					−0.6			−0.6	
	All others					−0.2			−0.2	
I_O§		V_{CC} = MAX,	V_O = 2.25 V	−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, Outputs open	V_I = 0 V,		150	210		150	210	mA

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}	INCLK↑	I/O, O	R_L = 500 Ω, C_L = 50 pF, See Note 3	20			30			MHz
t_{pd}	I, I/O	I/O, O			15	30		15	25	ns
t_{pd}	I/D¶	I/O, O			20	40		20	35	ns
t_{pd}	INCLK↑	I/O, O			20	40		20	35	ns
t_{pd}	OUTCLK↑	Q			10	25		10	20	ns
t_{en}	$\overline{OE}$↓	Q			10	25		10	20	ns
t_{en}	I, I/O	I/O, O			14	30		14	25	ns
t_{en}	I/D¶	I/O, O			27	45		27	40	ns
t_{en}	INCLK↑	I/O, O			27	45		27	40	ns
t_{dis}	$\overline{OE}$↑	Q			11	25		11	20	ns
t_{dis}	I, I/O	I/O, O			12	30		12	25	ns
t_{dis}	I/D¶	I/O, O			13	30		13	30	ns
t_{dis}	INCLK↑	I/O, O			13	30		13	25	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.
¶ Input configured as an input buffer.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

programming information

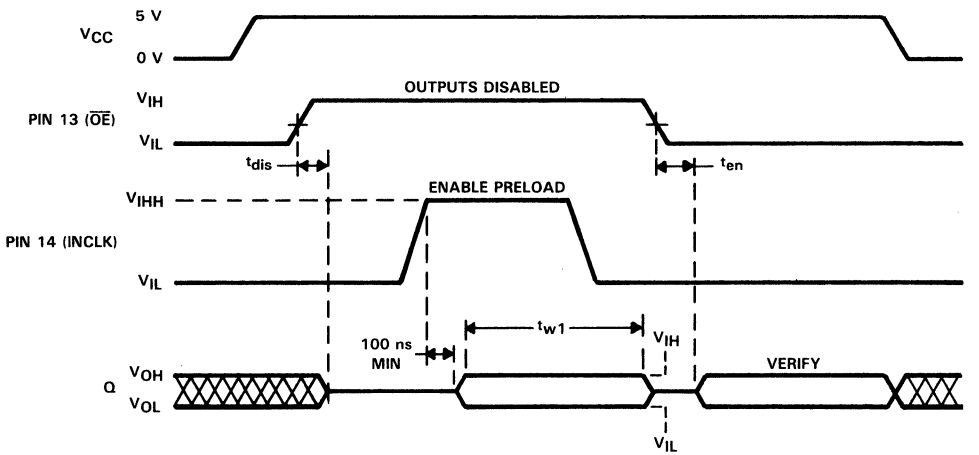
Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5762.

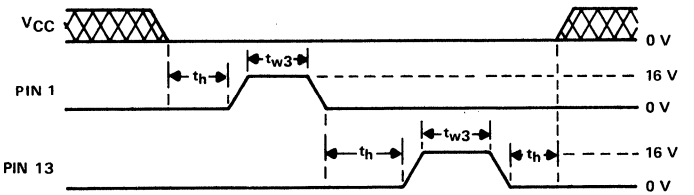
preload procedure for registered outputs (see Note 4)

Step 1 Pin 13 to V_{IH}, Pin 1 to V_{IL}, and V_{CC} to 5 volts.
Step 2 Pin 14 to V_{IHH}
Step 3 At Q outputs, apply V_{IL} to preload a low and V_{IH} to preload a high.
Step 4 Pin 14 to V_{IL}.
Step 5 Remove the voltages applied to the outputs.
Step 6 Pin 13 to V_{IL}
Step 7 Check the output states to verify preload.

preload waveforms (see Note 4)



security fuse programming (see Note 4)



NOTE 4: Pin numbers shown are for JW and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.

HIGH-PERFORMANCE REGISTERED-INPUT *PAL*® CIRCUITS

D2709, DECEMBER 1982—REVISED DECEMBER 1987

- High-Performance Operation . . . 30 MHz
- Preload Capability on Output Registers
- DIP Options Include Both 300-mil Plastic and 600-mil Ceramic
- Dependable Texas Instruments Quality and Reliability

DEVICE	I/D INPUTS	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PALT19L8	11	2	2	0	6
'PALT19R4	11	0	0	4 (3-state buffers)	4
'PALT19R6	11	0	0	6 (3-state buffers)	2
'PALT19R8	11	0	0	8 (3-state buffers)	0

description

These programmable array logic devices feature high speed and functionality similar to the TIBPAL16L8, 16R4, 16R6, 16R8 series, but with the added advantage of D-type transparent latches on the inputs. If any input register is not desired, it can be converted to an input buffer by simply programming the architectural fuse.

Combining Advanced Low-Power Schottky† technology, with proven titanium-tungsten fuses, these devices will provide reliable high performance substitutes over conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

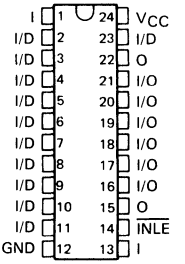
An M suffix designates full-temperature circuits that are characterized for operation over the full military temperature range of −55°C to 125°C. A C suffix designates commercial-temperature circuits that are characterized for operation from 0°C to 70°C.

INPUT LATCH FUNCTION TABLE

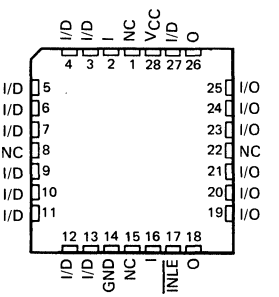
$\overline{INLE}$	D	LATCH OUTPUT
L	L	L
L	H	H
H	X	Q_0

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.
PAL is a trademark of Monolithic Memories Inc.

TIBPALT19L8'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



TIBPALT19L8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

Pin assignments in operating mode

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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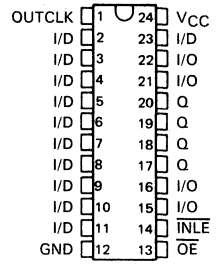
TIBPALT19R4'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



TIBPALT19R4'
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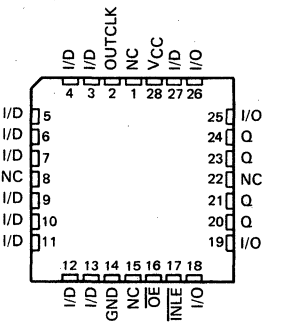
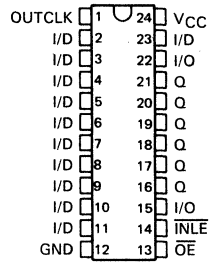
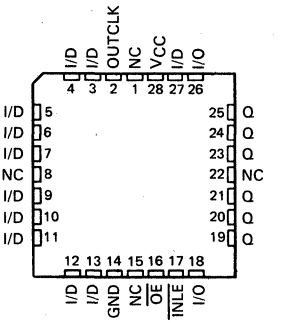
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



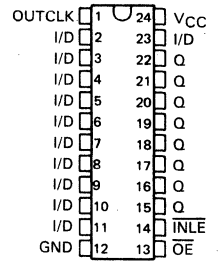
TIBPALT19R6'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



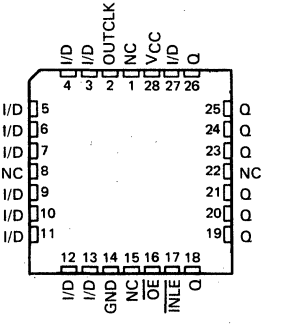
TIBPALT19R6'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPALT19R8'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



TIBPALT19R8'
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



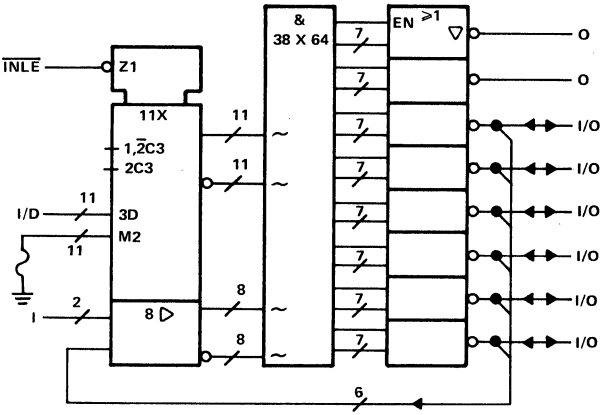
Pin assignments in operating mode

NC—No internal connection

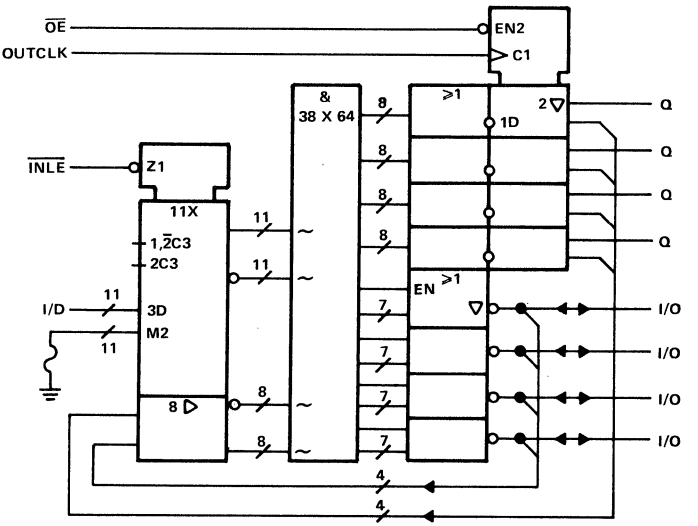
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

functional block diagrams (positive logic)

'PALT19L8

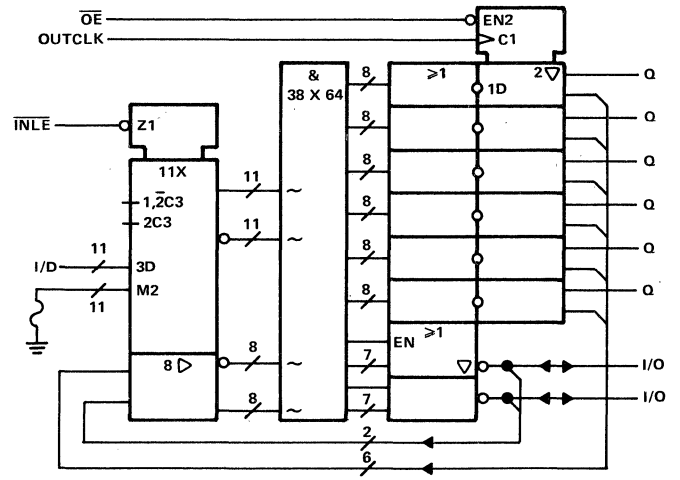


'PALT19R4

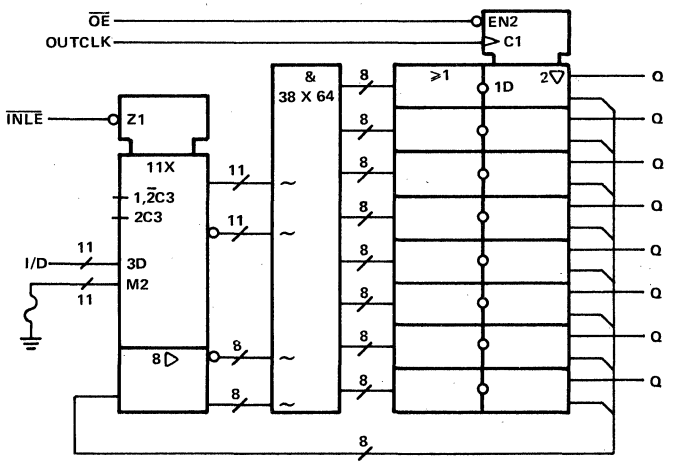


functional block diagrams (positive logic)

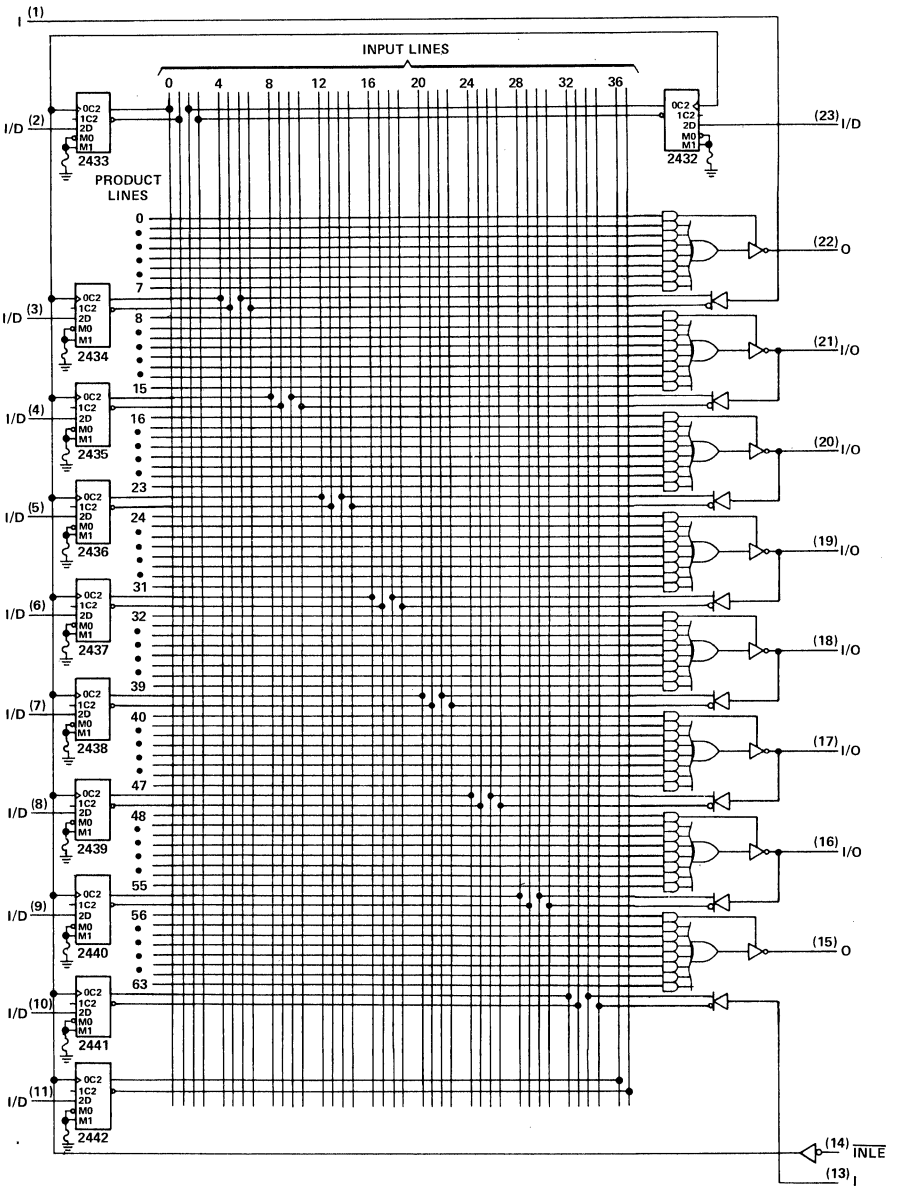
'PALT19R6



'PALT19R8

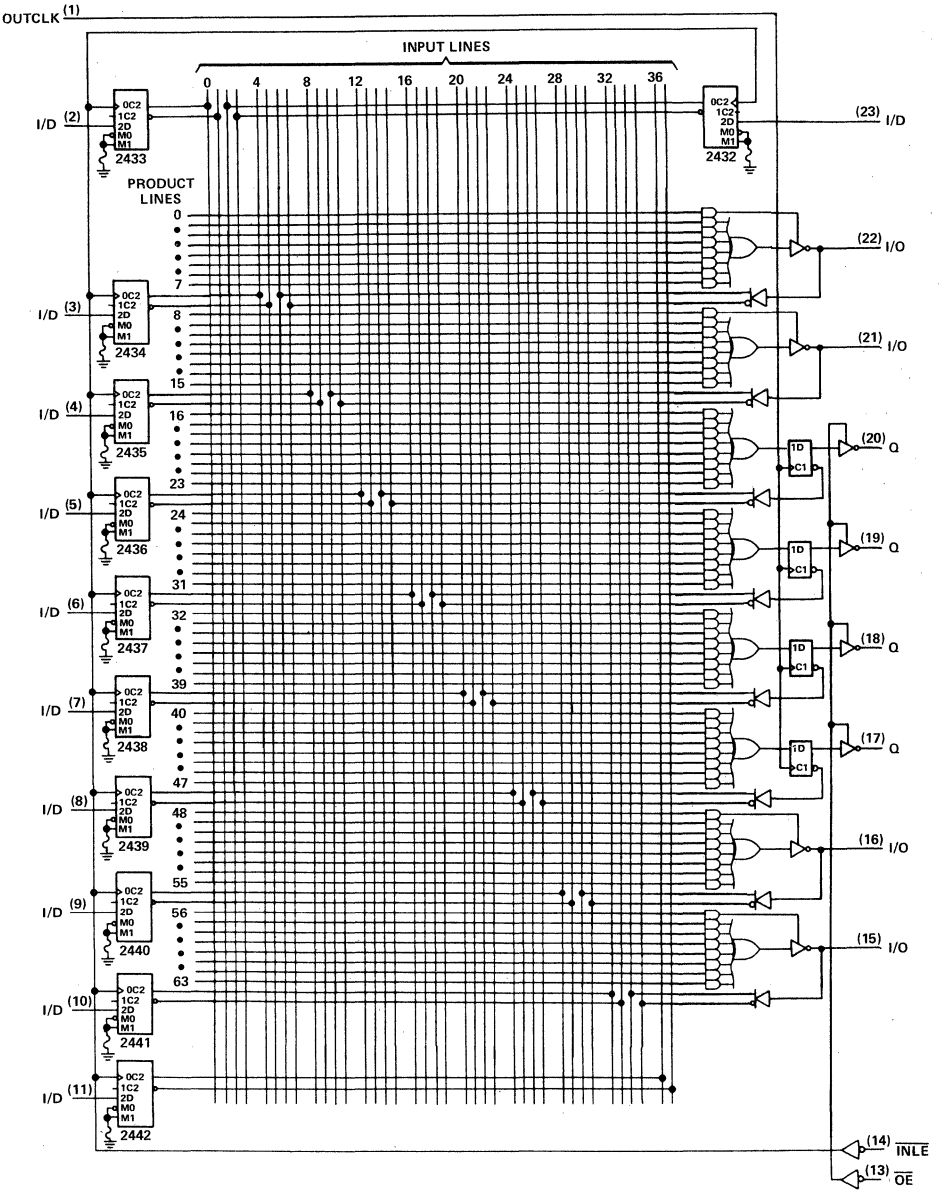


logic diagram (positive logic)



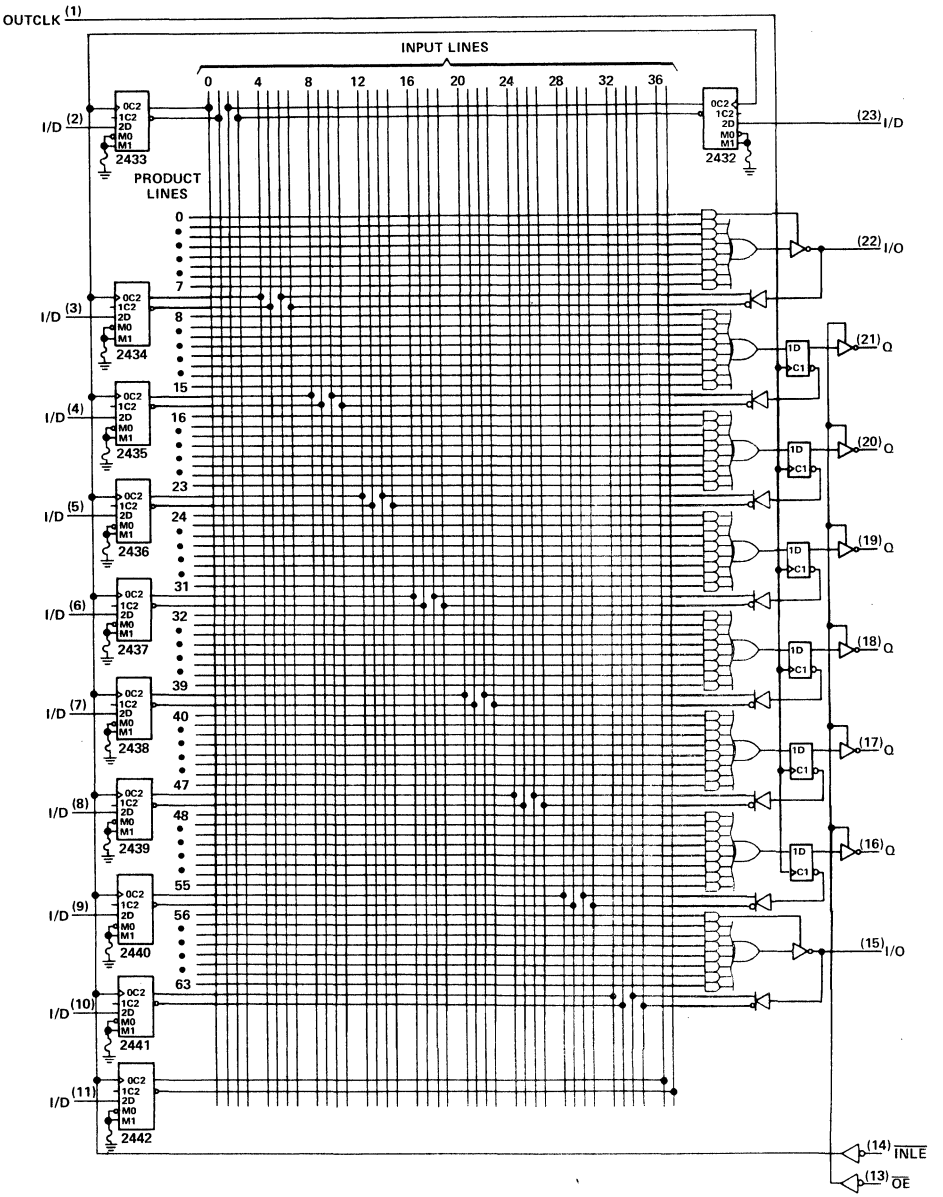
Pin numbers shown are for JW and NT packages.

logic diagram (positive logic)



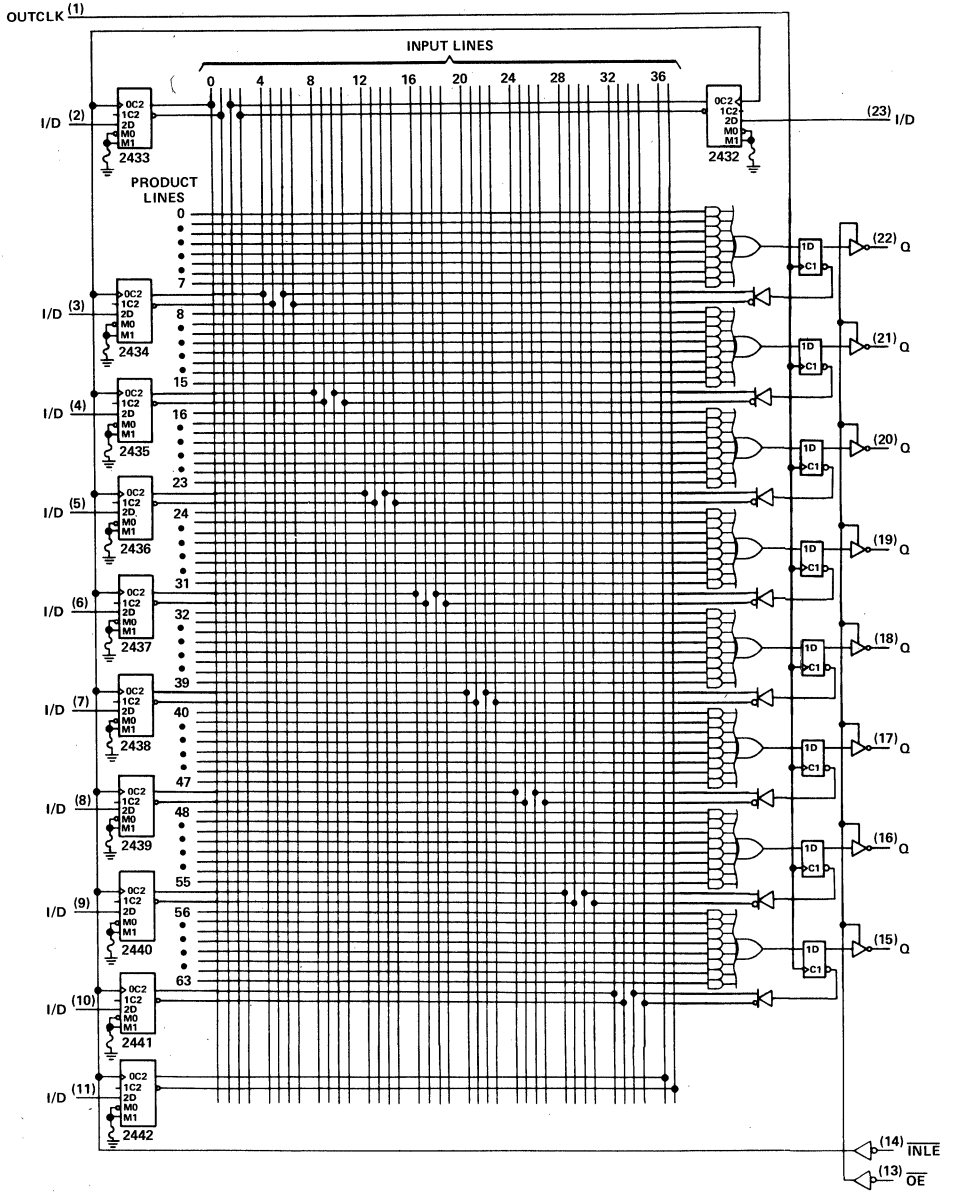
Pin numbers shown are for JW and NT packages.

logic diagram (positive logic)



Pin numbers shown are for JW and NT packages.

logic diagram (positive logic)



Pin numbers shown are for JW and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during preload cycle.

recommended operating conditions

			M SUFFIX			C SUFFIX			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency	OUTCLK	0		20	0		30	MHz
t_w	Pulse duration	$\overline{INLE}$ low	20			15			ns
		OUTCLK high	20			15			ns
		OUTCLK low	20			15			
t_{su}	Setup time	Data before $\overline{INLE}$ ↑	15			10			ns
		Data before OUTCLK↑	30			25			
		$\overline{INLE}$ low before OUTCLK↑ (See Note 2)	35			30			
t_h	Hold time	Data after $\overline{INLE}$ ↑	5			5			ns
		Data after OUTCLK↑	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTE 2: This setup time ensures the output registers will see stable data from the input latches.

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†		M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	μA
	I/O ports					100			100	
I_{OZL}	Outputs	V_{CC} = MAX,	V_{IH} = 0.4 V			−20			−20	μA
	I/O ports					−250			−250	
I_I	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 5.5 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
	All others					−0.2			−0.2	
I_O§		V_{CC} = MAX,	V_O = 2.25 V	−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, Outputs open	V_I = 0 V,		150	210		150	210	mA

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}	OUTCLK↑	Q		20			30			MHz
t_{pd}	I, I/O	I/O, O			15	30		15	25	ns
t_{pd}	I/D¶	I/O, O			25	45		25	40	ns
t_{pd}	$\overline{INLE}$↓	I/O, O			28	45		28	40	ns
t_{pd}	OUTCLK↑	Q			10	25		10	20	ns
t_{en}	$\overline{OE}$↓	Q	R_L = 500 Ω,		10	25		10	20	ns
t_{en}	I, I/O	I/O, O	C_L = 50 pF,		14	30		14	25	ns
t_{en}	I/D¶	I/O, O	See Note 3		30	45		30	40	ns
t_{en}	$\overline{INLE}$↓	I/O, O			30	45		30	40	ns
t_{dis}	$\overline{OE}$↑	Q			11	25		11	20	ns
t_{dis}	I, I/O	I/O, O			12	30		12	25	ns
t_{dis}	I/D¶	I/O, O			14	30		14	25	ns
t_{dis}	$\overline{INLE}$↓	I/O, O			14	30		14	25	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.
¶Input configured as an input buffer or $\overline{INLE}$ low.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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programming information

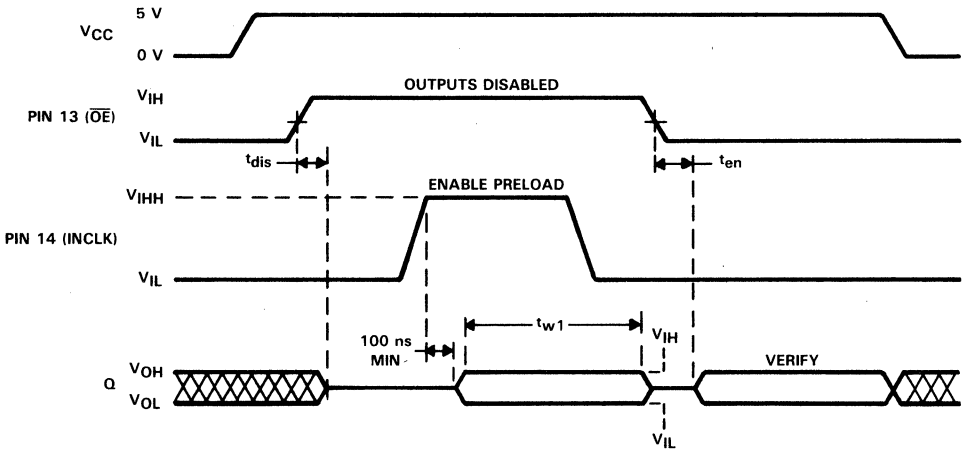
Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5762.

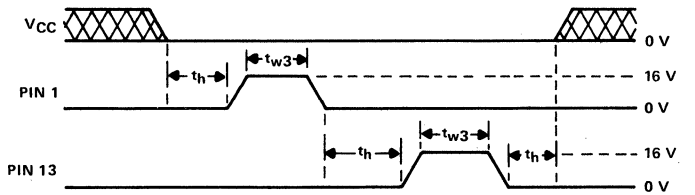
preload procedure for registered outputs (see Note 4)

Step 1 Pin 13 to V_{IH}, Pin 1 to V_{IL}, and V_{CC} to 5 volts.
Step 2 Pin 14 to V_{IHH}
Step 3 At Q outputs, apply V_{IL} to preload a low and V_{IH} to preload a high.
Step 4 Pin 14 to V_{IL}.
Step 5 Remove the voltages applied to the outputs.
Step 6 Pin 13 to V_{IL}
Step 7 Check the output states to verify preload.

preload waveforms (see Note 4)



secruity fuse programming (see Note 4)

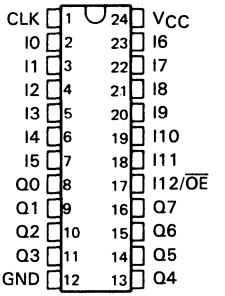


NOTE 4: Pin numbers shown are for JW and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.

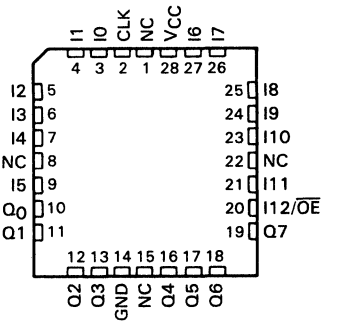
D3090, DECEMBER 1987

- **50-MHz Clock Rate**
- **Power-On Reset of All Registers**
- **16-Bit Internal State Registers**
- **8-Bit Output Registers**
- **Outputs Programmable for Registered or Combinational Operation**
- **Ideal for Waveform and State Machine Applications**

M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FK OR FN PACKAGE
(TOP VIEW)



NC—No Internal Connection

description

The TIBPLS506 is a TTL field-programmable state machine of the Mealy type. This state machine (logic sequencer) contains 97 product terms (AND terms) and 24 pairs of sum terms (OR terms). The product and sum terms are used to control the 16-bit internal state registers and the 8-bit output registers.

The outputs of the internal state registers (P0-P15) are fed back and combined with the 13 inputs (I0-I12) to form the AND array. In addition, two sum terms are complemented and fed back to the AND array, which allows any product terms to be summed, complemented, and used as inputs to the AND array.

The eight output cells can be individually programmed for registered or combinational operation. Nonregistered operation is selected by blowing the output multiplexer fuse. Each combinational output must also have all fuses blown from the reset term. Registered operation is selected by leaving the output multiplexer fuse intact.

Pin 17 can be programmed to function as an input and/or an output enable. Blowing the output enable fuse lets pin 17 function as an output enable but does not disconnect pin 17 from the input array. When the output enable fuse is intact, pin 17 functions only as an input with the outputs being permanently enabled.

The state and output registers are synchronously clocked by the fuse programmable clock input. The clock polarity fuse selects either positive- or negative-edge triggering. Negative-edge triggering is selected by blowing the clock polarity fuse. Leaving this fuse intact selects positive-edge triggering. The state and output registers are unconditionally reset low on power-up.

The eight outputs can be individually programmed for combinational operation by blowing the output multiplexer fuse. Each combinational output must also have all fuses blown from its associated reset term. When the output multiplexer fuse is left intact, registered operation is selected.

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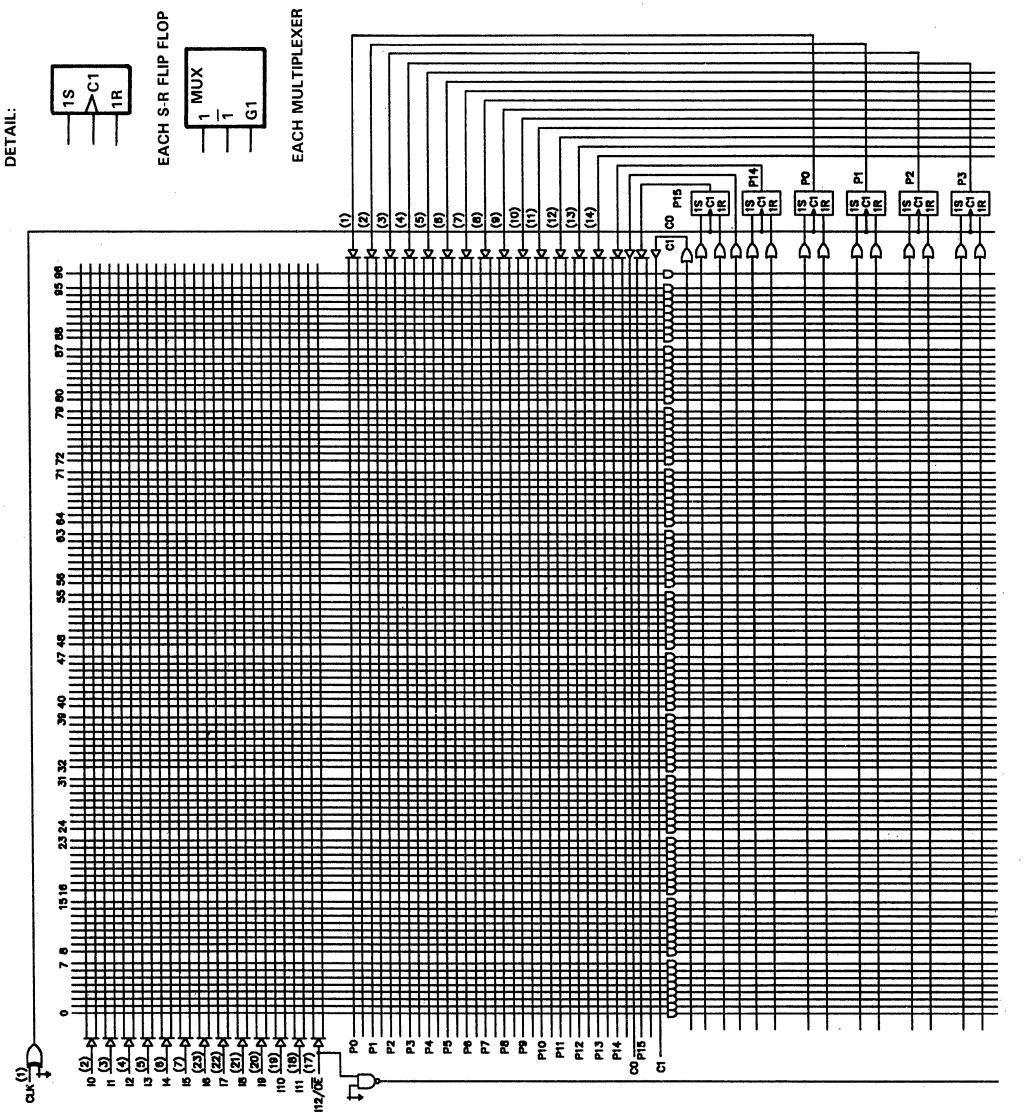
logic diagram (positive logic)



NOTES: A. All AND gate inputs with a blown link assume the logic-1 state
B. All OR gate inputs with a blown link assume the logic-0 state.

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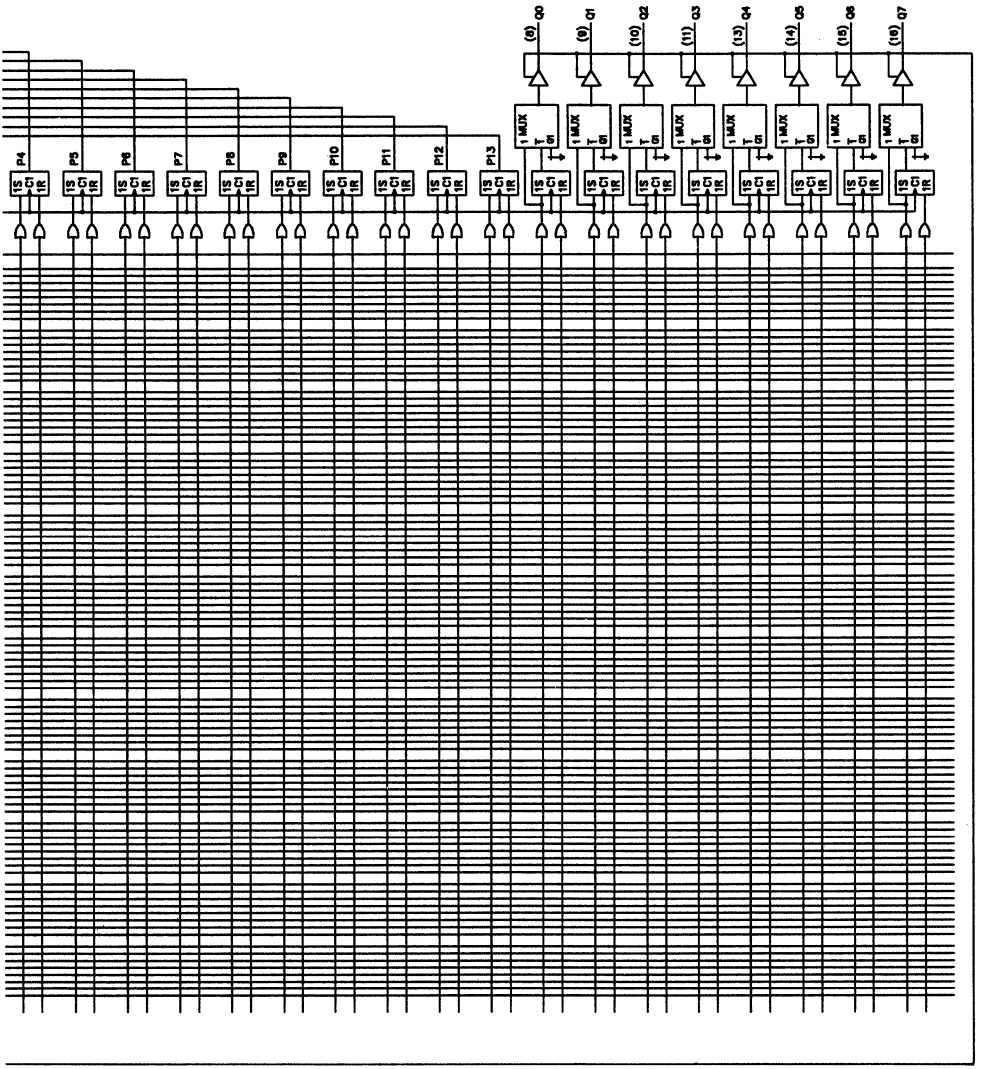
logic diagram (continued)

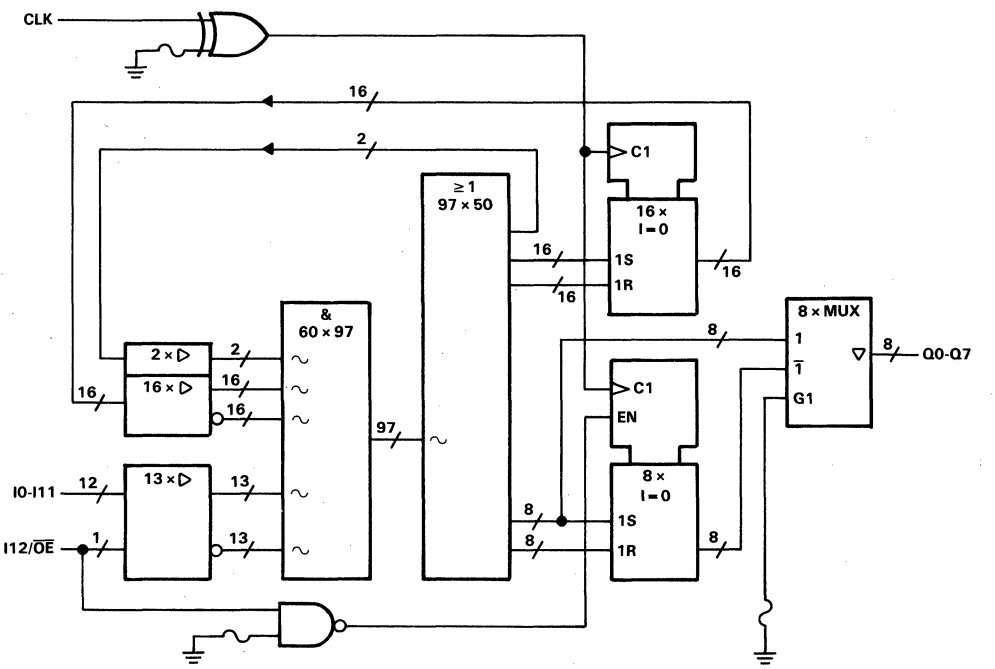


S-R FUNCTION TABLE (see Note 1)

CLK POLARITY FUSE	CLK	S	R	STATE REGISTER
INTACT	↑	L	L	Q_0
INTACT	↑	L	H	L
INTACT	↑	H	L	H
INTACT	↑	H	H	INDETERMINATE
BLOWN	↓	L	L	Q_0
BLOWN	↓	L	H	L
BLOWN	↓	H	L	H
BLOWN	↓	H	H	INDETERMINATE

NOTE 1: The S-R registers clear at power-up. Q_0 is the state of the S-R registers before the active clock edge.

functional block diagram (positive logic)



∼ denotes fused inputs

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 2) . . . . . 7 V
Input voltage (see Note 2) . . . . . 5.5 V
Voltage applied to disabled output (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: TIBPLS506M . . . . . 55°C to 125°C
TIBPLS506C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 2: These ratings apply except when programming pins during a programming cycle.

recommended operating conditions

			TIBPLS506M			TIBPLS506C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current							24	mA
t_w	Pulse duration	Clock high							ns
		Clock low							
t_{su}	Setup time before CLK† input or feedback to S-R inputs	Without C-array							ns
		With C-array							
t_h	Hold time after CLK	Input or feedback at S-R inputs							ns
T_A	Operating free-air temperature		−55		125	0		75	°C

†The active edge of CLK is determined by the programmed state of CLK polarity fuse.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		TIBPLS506M			TIBPLS506C			UNIT
			MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3		V
V_{OL}	V_{CC} = MIN,	I_{OL} = MAX		0.25	0.4		0.37	0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			25			25	μA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V			−0.25			−0.25	mA
I_{OS}	V_{CC} = MAX,	V_O = 2.25 V	−15		−65	−15		−65	mA
I_{OZH}	V_{CC} = MAX,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.4 V			−20			−20	μA
I_{CC}	V_{CC} = MAX, Outputs open	V_I = 4.5 V,		140			140		mA

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TIBPLS506M			TIBPLS506C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}‡	Without C-array		R_L = 500 Ω, C_L = 50 pF		60			60		MHz
	With C-Array				40			40		
t_{pd}	CLK§	Q (nonregistered)			20			20		ns
	CLK	Q (registered			9			9		
	I	Q (nonregistered)			15			15		
t_{en}	$\overline{OE}$↓	Q			6			6		ns
t_{dis}	$\overline{OE}$↑	Q			6			6		ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡f_{max} is independent of the internal programmed configuration and the number of product terms used.
§The active edge of CLK is determined by the programmed state of the CLK polarity fuse.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

diagnostics

A diagnostic mode is provided with these devices that allows the user to inspect the contents of the state registers. The step-by-step procedures required to use the diagnostics follow.

1. Disable all outputs by taking pin 17 ($\overline{OE}$) high (see Note 4).
2. Take pin 8 (Q0) double high to enable the diagnostics test sequence.
3. Apply appropriate levels of voltage to pins 11 (Q3), 13 (Q4), and 14 (Q5) to select the desired state register (see Table 1).

The voltage level monitored on pin 9 will indicate the state of the selected state register.

NOTE 4: If pin 17 is being used as an input to the array, then pin 7 (I5) must be taken double high before pin 17 is taken high.

diagnostics waveforms

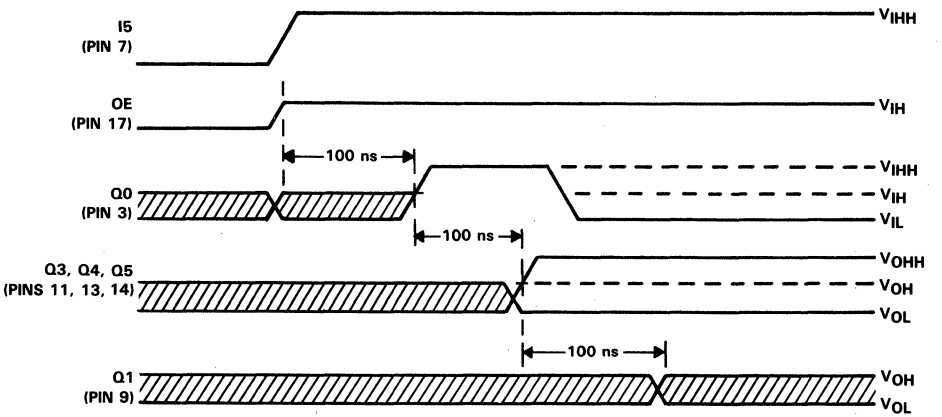

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TABLE 1. ADDRESSING STATE REGISTERS DURING DIAGNOSTICS

REGISTER BINARY ADDRESS			BURIED REGISTER
PIN 11	PIN 13	PIN 14	SELECTED
L	L	L	C1
L	L	H	P15
L	L	HH	C0
L	H	L	P14
L	H	H	P0
L	H	HH	P1
L	HH	L	P2
L	HH	H	P3
L	HH	HH	P4
H	L	L	P5
H	L	H	P6
H	L	HH	P7
H	H	L	P8
H	H	H	P9
H	H	HH	P10
H	HH	L	P11
H	HH	H	P12
H	HH	HH	P13

PROGRAMMING INFORMATION

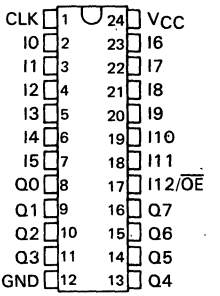
Texas Instruments programmable logic devices can be programmed using widely available software and reasonably priced device programmers.

Complete programming specifications, algorithms, and the latest information on firmware, software, and hardware updates are available upon request. Information on programmers that are capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI sales office, local authorized Texas Instruments distributor, or by calling Texas Instruments at (214) 997-5762.

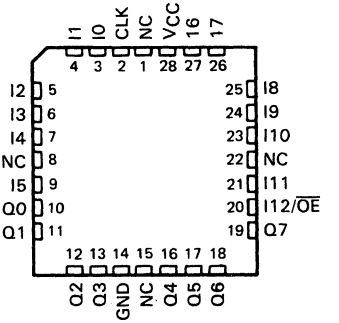
D3029, MAY 1987—REVISED DECEMBER 1987

- **50 MHz Clock Rate**
- **Ideal for Waveform and State Machine Applications**
- **6-Bit Internal Binary Counter**
- **8-Bit Internal State Register**
- **Programmable Clock Polarity**
- **Outputs Programmable for Registered or Combinatorial Operation**
- **6-Bit Counter Simplifies Logic Equation Development in State Machine Designs**
- **Dependable Texas Instruments Quality and Reliability**

M SUFFIX . . . . JT PACKAGE
C SUFFIX . . . . JT OR NT PACKAGE
(TOP VIEW)



M SUFFIX . . . . FK PACKAGE
C SUFFIX . . . . FK OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

The TIBPSG507 is a 13 × 80 × 8 Programmable Sequence Generator (PSG) that offers the system designer unprecedented flexibility in a high-performance field-programmable logic device. Applications such as waveform generators, state machines, dividers, timers, and simple logic reduction are all possible with a PSG. By utilizing the built-in binary counter, the PSG is capable of generating complex timing controllers. The binary counter also simplifies logic equation development in state machine and waveform generator applications.

The PSG507 contains 80 product (AND) terms, a 6-bit binary counter with control logic, eight S/R state holding registers, and eight outputs. The eight outputs can be individually programmed for either registered or combinatorial operation. The clock input is fuse programmable for either positive- or negative-edge operation.

The 6-bit binary counter is controlled by a synchronous-clear and a count/hold function. Each control function has a nonregistered and registered option. When either SCLR0 or SCLR1 is taken high, the counter resets to zero on the next active clock edge. When either $\overline{\text{CNT}}$/HLD0 or $\overline{\text{CNT}}$/HLD1 is taken high, the counter is held at the present count and is not allowed to advance on the active clock edge. The SCLR function overrides the $\overline{\text{CNT}}$/HLD feature when both lines are simultaneously high.

Clock polarity is programmable through the clock polarity fuse. Leaving this fuse intact selects positive-edge triggering. Negative-edge triggering is selected by blowing this fuse. Pin 17 functions as an input and/or an output enable. When the output enable fuse is intact, all outputs are always enabled allowing pin 17 to be used strictly as an input. Blowing the output enable fuse lets pin 17 function as an output enable and an input. In this mode, the outputs are enabled when pin 17 is low and are in a high-impedance state when pin 17 is high.

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description (continued)

The eight outputs can be individually programmed for combinational operation by blowing the output multiplexer fuse. Each combinational output must also have all fuses blown from its associated reset term. When the output multiplexer fuse is left intact, registered operation is selected.

The M suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The C suffix devices are characterized for operation from 0°C to 75°C.

6-BIT COUNTER CONTROL FUNCTION TABLE (see Note 1)

$\overline{CNT}$/HLD1	$\overline{CNT}$/HLD0	SCLR1	SCLR0	OPERATION
L	L	L	L	counter active
X	X	X	H	synchronous clear
X	X	H	X	synchronous clear
X	H	L	L	hold counter
H	X	L	L	hold counter

NOTE 1: The 6-Bit counter and the S/R control registers are clear upon power-up. Devices with the fuses intact will power-up in the counter-active mode. When all fuses are blown on a product line (AND), its output will be high. When all fuses are blown on a sum line (OR), its outputs will be low. All product and sum terms are low on devices with fuses intact.

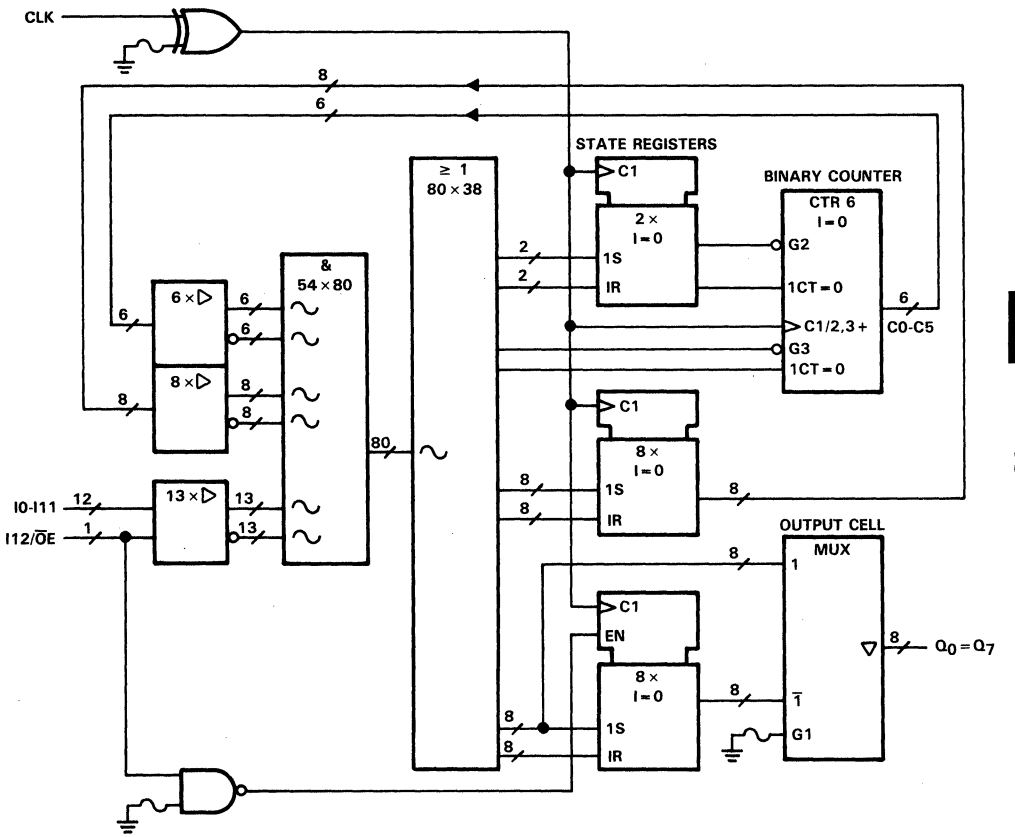
S/R FUNCTION TABLE (see Note 2)

CLK POLARITY FUSE	CLK	S	R	STATE REGISTER
INTACT	↑	L	L	Q_0
INTACT	↑	L	H	L
INTACT	↑	H	L	H
INTACT	↑	H	H	INDET†
BLOWN	↑	L	L	Q_0
BLOWN	↑	L	H	L
BLOWN	↑	H	L	H
BLOWN	↑	H	H	INDET†

†Output state is indeterminate

NOTE 2: S/R registers are clear upon power up. Q_0 is the state of the S/R register before the active clock edge.

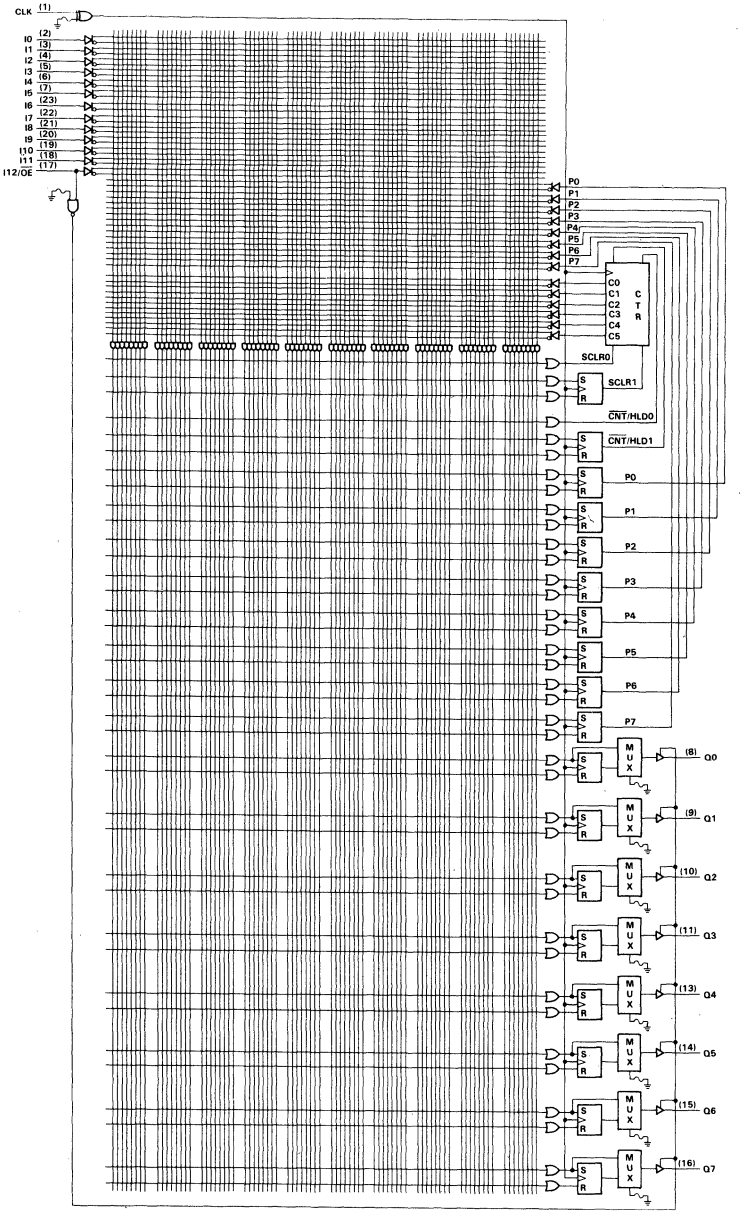
functional block diagram



~ denotes fused inputs

PRODUCT PREVIEW

logic diagram (positive logic)



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absolute maximum ratings

Supply voltage, V_{CC} (see Note 3) . . . . . 7 V
Input voltage, V_I (see Note 3) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 3) . . . . . 5.5 V
Operating free-air temperature range: TIBPGS507M . . . . . −55°C to 125°C
TIBPGS507C . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 3: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			M SUFFIX			C SUFFIX			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration	Clock high							ns
		Clock low							
t_{su}	Setup time† before CLK active transition	Input or feedback to S/R inputs				15			ns
		Input or feedback to SCLR0				25			ns
		Input or feedback to $\overline{CNT}$/HOLD0				25			ns
t_h	Hold time† after CLK active transition	Input or feedback at S/R inputs				0			ns
		Input or feedback at SCL0				0			
		Input or feedback at $\overline{CNT}$/HLD0				0			
T_A	Operating free-air temperature		−55		125	0		75	°C

†Internal setup and hold times, t_{su} feedback to SCLR1, feedback to $\overline{CNT}$/HLD1; t_h feedback at SCLR1 and feedback at $\overline{CNT}$/HLD1, are guaranteed by f_{max} specifications. The active transition of CLK is determined by the programmed state of the CLK polarity fuse.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		M SUFFIX			C SUFFIX			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3		V
V_{OL}	V_{CC} = MIN,	I_{OL} = MAX		0.25	0.4		0.37	0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			25			25	μA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V			−0.25			−0.25	mA
I_{OS}	V_{CC} = MAX,	V_O = 2.25 V	−15		−65	−15		−65	mA
I_{OZH}	V_{CC} = MAX,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.4 V			−20			−20	μA
I_{CC}	V_{CC} = MAX	V_I = 4.5 V, Outputs open		140			140		mA

switching characteristics over recommended supply voltage and operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}‡	6-Bit counter		R_L = 500 Ω, C_L = 50 pF							MHz
	6-Bit counter with SCLR1 or $\overline{CNT}$/HLD1						50			
	6-Bit counter with SCLR0 or $\overline{CNT}$/HLD0						35			
	S/R registers						50			
t_{pd}	CLK§	Q (non-registered)¶							20	ns
	CLK§	Q (registered)							12	ns
	I	Q (non-registered)							18	ns
t_{en}	$\overline{OE}$↓	Q							12	ns
t_{dis}	$\overline{OE}$↑	Q							12	ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1 of the TTL Data Book, Volume 4.
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡f_{max} is independent of the number of product terms used.
§The active edge of CLK is determined by the programmed state of the CLK polarity fuse.
¶t_{pd} CLK to Q (nonregistered) is the same for data clocked from the counter or state registers.

PRINCIPLES OF OPERATION

PSG DESIGN THEORY

Most state machine and waveform generator designs can be simplified with the PSG by referencing all or part of each sequence to a binary count. The internal state registers can then be used to keep track of which binary count sequence is in operation, to store input data and keep track of internally generated status bits, or as output registers when connected to a nonregistered output cell. State registers can also be used to expand the binary counter when a larger counter is needed.

Through the use of the binary counter, the number of product lines and state registers required for a design is usually reduced. In addition, the designer does not have to be concerned about generating wait states where the outputs are unaffected because these can be timed from the binary counter. For detailed information and examples using this design concept, see the "DESIGNER'S GUIDE TO THE PSG507" applications report (literature number SPDA003).

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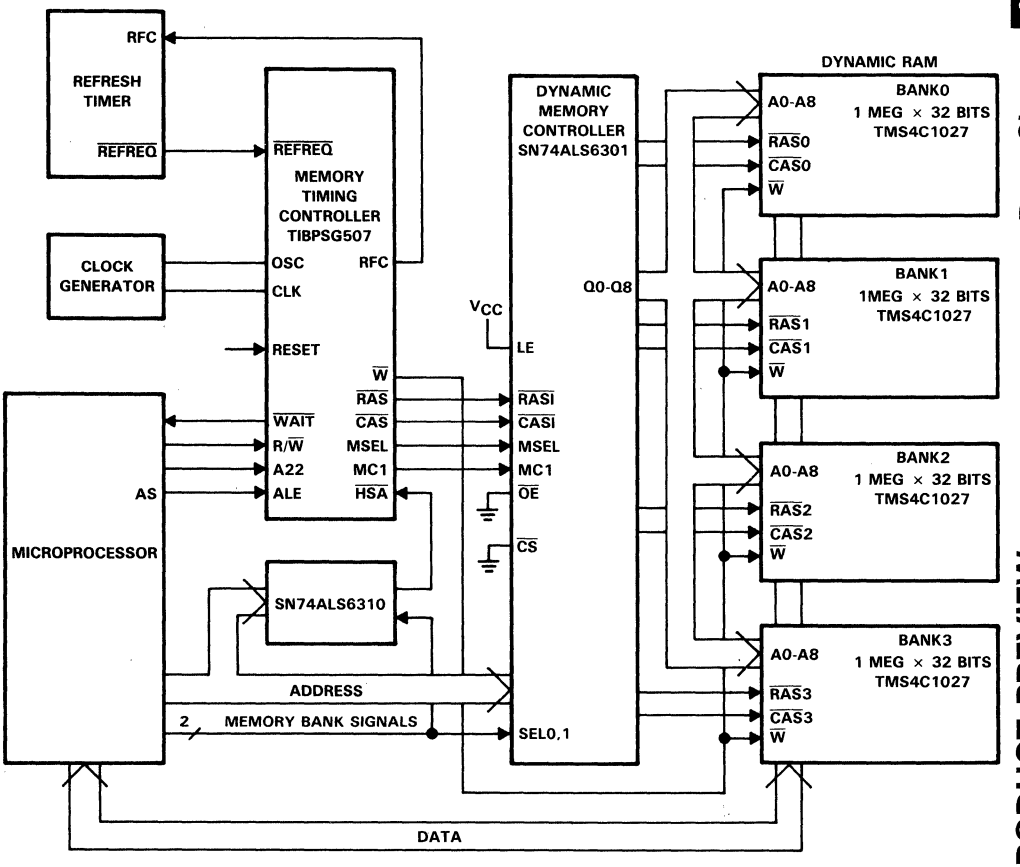
PRINCIPLES OF OPERATION

PROGRAMMING INFORMATION

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on firmware, software, and hardware updates are available upon request. Information on persons capable of programming Texas Instruments Programmable Logic is also available upon request from the nearest TI sales office or local authorized TI distributor; information may also be obtained by calling or writing Texas Instruments at (214) 997-5762, Texas Instruments, Post Office Box 655803, Dallas, Texas 75265.

TYPICAL APPLICATION



For detailed information, please see the "SYSTEMS SOLUTION FOR STATIC COLUME DECODE" Application Report.

diagnostics

A diagnostics mode is provided with these devices that allows the user to inspect the contents of the state registers. The following are the step-by-step procedures required for the diagnostics.

1. Disable all outputs by taking $\overline{OE}$ (pin 17) high. (Note: If pin 17 is being used as an input to the array, then pin I5 or pin 7 must be taken to double high first before pin 17 is taken high.)
2. Take Q0 (pin 8) double high to enable the diagnostics test sequence.
3. Apply appropriate levels of voltage to pins 11, 13 and 14 to select the desired state register, (see Table 1)
4. The voltage level monitored on pin 9 will indicate the state of the selected state register.

diagnostics waveforms

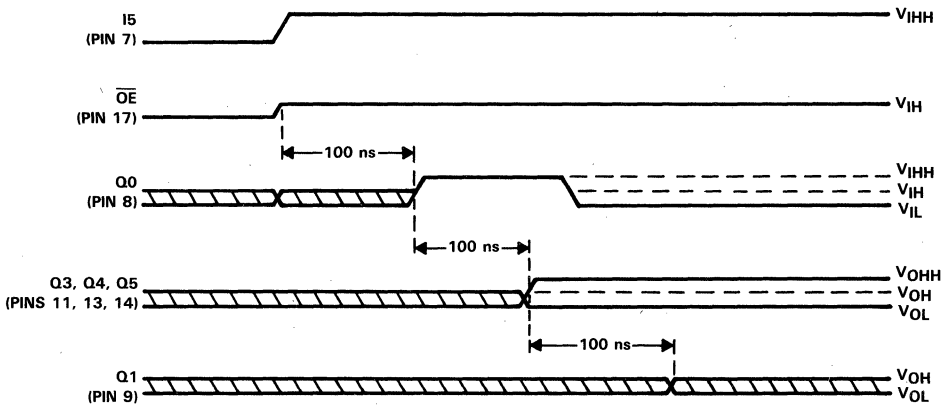


TABLE 1. ADDRESSING STATE REGISTERS DURING DIAGNOSTICS

REGISTER BINARY ADDRESS			BURRIED REGISTER SELECTED
PIN 11	PIN 13	PIN 14	
L	L	L	SCLR0
L	L	H	SCLR1
L	L	HH	$\overline{CNT}$/HLD0
L	H	L	$\overline{CNT}$/HLD1
L	H	H	P0
L	H	HH	P1
L	HH	L	P2
L	HH	H	P3
L	HH	HH	P4
H	L	L	P5
H	L	H	P6
H	L	HH	P7
H	H	L	C0
H	H	H	C1
H	H	HH	C2
H	HH	L	C3
H	HH	H	C4
H	HH	HH	C5

TEXAS INSTRUMENTS
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- **50-MHz Clock Rate**
- **Power-On Preset of All Flip-Flops**
- **6-Bit Internal State Register with 8-Bit Output Register**
- **Power Dissipation . . . 600 mW Typical**
- **Programmable Asynchronous Preset or Output Control**
- **Functionally Equivalent to, but Faster than 82S105A†**

description

The TIB82S105B is a TTL field-programmable state machine of the Mealy type. This state machine (logic sequencer) contains 48 product terms (AND terms) and 14 pairs of sum terms (OR terms). The product and sum terms are used to control the 6-bit internal state register and the 8-bit output register.

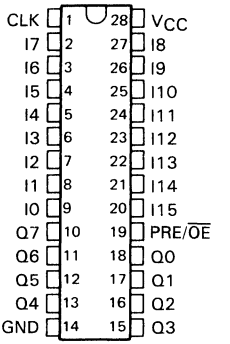
The outputs of the internal state register (P0—P5) are fed back and combined with the 16 inputs (I0—I15) to form the AND array. In addition a single sum term is complemented and fed back to the AND array, which allows any of the product terms to be summed, complemented, and used as an input to the AND array.

The state and output registers are positive-edge-triggered S/R flip-flops. These registers are unconditionally preset high on power-up. Pin 19 can be used to preset both registers or, by blowing the proper fuse, be converted to an output control function.

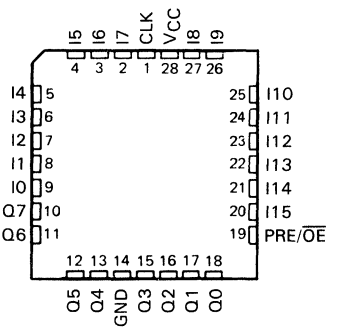
The TIB82S105BM is characterized for operation over the full military temperature range of −55°C to 125°C. The TIB82S105BC is characterized for operation from 0°C to 75°C.

† Power-up preset and asynchronous preset functions are not identical to 82S105A. See Recommended Operating Conditions.

M SUFFIX . . . JD PACKAGE
C SUFFIX . . . JD OR N PACKAGE
(TOP VIEW)



M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FK OR FN PACKAGE
(TOP VIEW)



2 Data Sheets

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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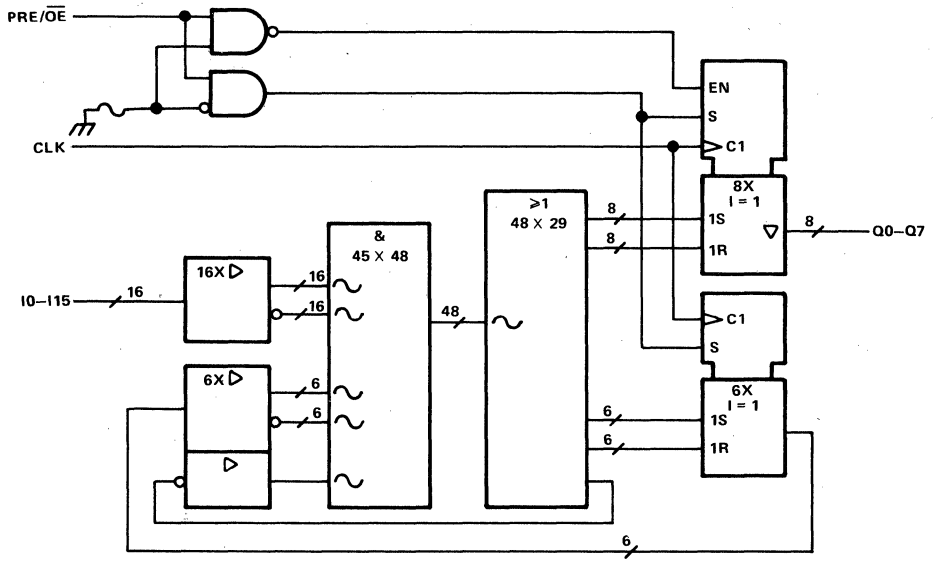
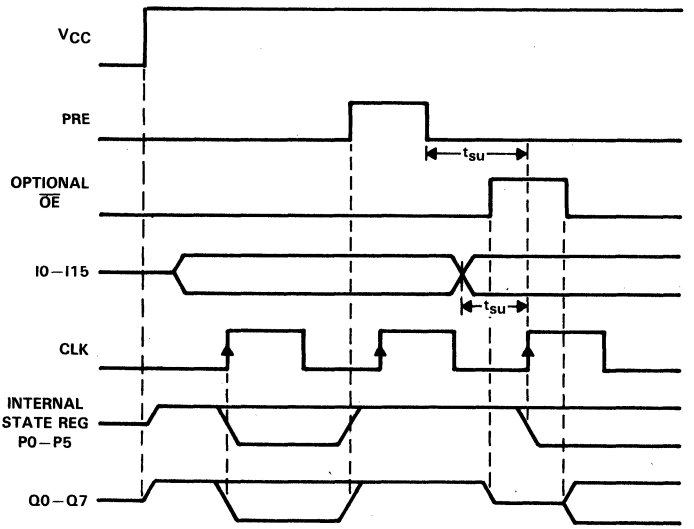
functional block diagram (positive logic)



∿ denotes fused inputs.

timing diagram



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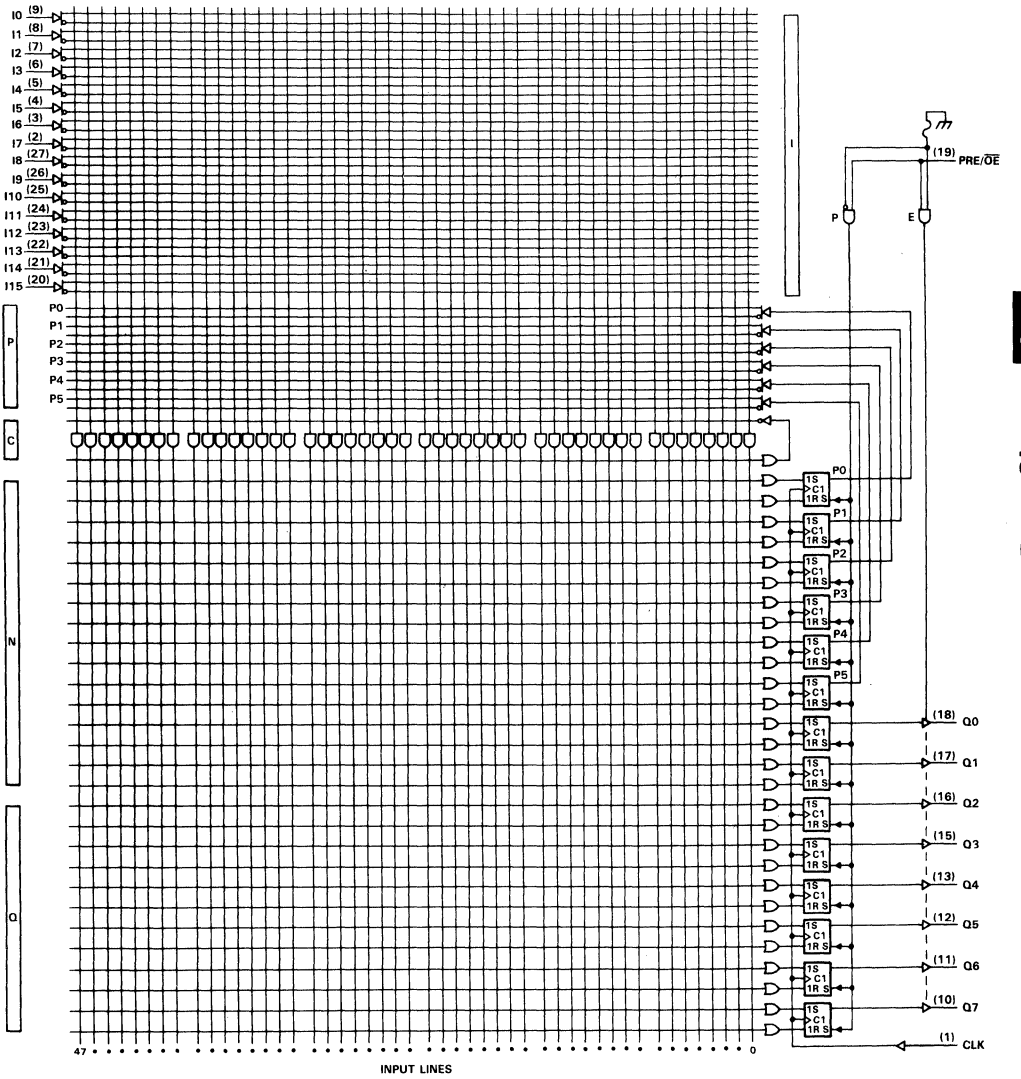
logic diagram (positive logic)



NOTES: 1. All AND gate inputs with a blown link float to a logic 1.
2. All OR gate inputs with a blown link float to a logic 0.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 3) . . . . . 7 V
Input voltage (see Note 3) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 3) . . . . . 5.5 V
Operating free-air temperature range: TIB82S105BM . . . . . −55°C to 125°C
TIB82S105BC . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 3: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			M SUFFIX			C SUFFIX			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency†	1 thru 48 product terms without C-array‡	0		40	0		50	MHz
		1 thru 48 product terms with C-array	0		25	0		30	
t_w	Pulse duration	Clock high or low	12			10			ns
		Preset	18			15			
t_{su}	Setup time before CLK↑, 1 thru 48 product terms	Without C-array	20			15			ns
		With C-array	35			30			
t_{su}	Setup time, Preset low (inactive) before CLK↑§		10			8			ns
t_h	Hold time, input after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		75	°C

† The maximum clock frequency is independent of the internal programmed configuration. If an output is fed back externally to an input, the maximum clock frequency must be calculated.
‡ The C-array is the single sum term that is complemented and fed back to the AND array.
§ After Preset goes inactive, normal clocking resumes on the first low-to-high clock transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		M SUFFIX			C SUFFIX			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3		V
V_{OL}	V_{CC} = MIN,	I_{OL} = MAX		0.25	0.4		0.37	0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			25			25	μA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V			−0.25			−0.25	mA
I_O§	V_{CC} = MAX,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{OZH}	V_{CC} = MAX,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.4 V			−20			−20	μA
I_{CC}	V_{CC} = MAX, PRE/$\overline{OE}$ input at GND,	V_I = 4.5 V, Outputs open		120	180		120	180	mA

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}¶	Without C-array			R_L = 500 Ω, C_L = 50 pF	40	70		50	70		MHz
	With C-array				25	45		30	45		
t_{pd}		CLK↑	Q			8	20		8	15	ns
t_{pd}		PRE↑	Q			12	25		12	20	ns
t_{pd}		V_{CC}↑	Q			0	10		0	10	ns
t_{en}		$\overline{OE}$↓	Q			10	25		10	20	ns
t_{dis}		$\overline{OE}$↑	Q			5	15		5	10	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}.
¶ f_{max} is independent of the internal programmed configuration and the number of product terms used.

programming information

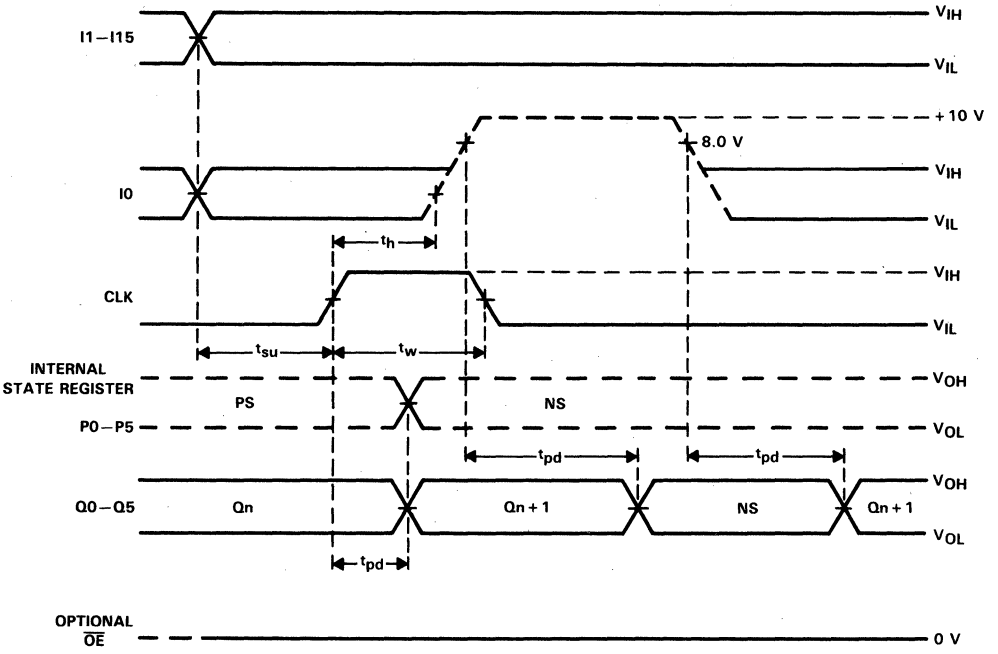
Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5762.

diagnostics

A diagnostics mode is provided with these devices that allows the user to inspect the contents of the state register. When I0 (pin 9) is held at 10 V, the state register bits P0—P5 will appear at the Q0—Q5 outputs and Q6—Q7 will be high. The contents of the output register will remain unchanged.

diagnostics waveforms



PS = Present state, NS = Next state

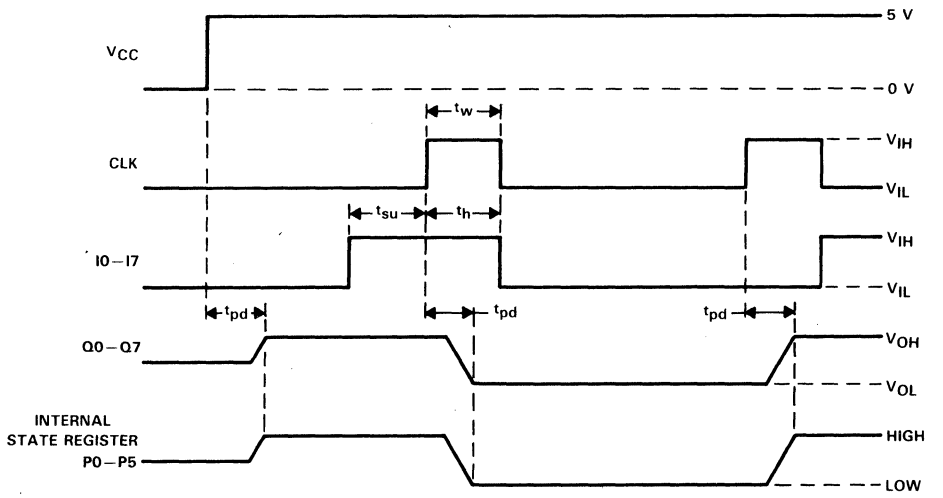
test array

A test array that consists of product lines 48 and 49 has been added to these devices to allow testing prior to programming. The test array is factory programmed as shown below. Testing is accomplished by connecting Q0–Q7 to I8–I15, PRE/$\overline{OE}$ to GND, and applying the proper input signals as shown in the timing diagram. Product lines 48 and 49 MUST be deleted during user programming to avoid interference with the programmed logic function.

TEST ARRAY PROGRAM

			OPTION PRE/$\overline{OE}$	H
	AND		OR	
PRODUCT LINE	C	$\overline{C}$	INPUT (In) 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	PRESENT STATE (PS) 5 4 3 2 1 0	NEXT STATE (NS) 5 4 3 2 1 0	OUT (Qn) 7 6 5 4 3 2 1 0
48	X	–	H H H H H H H H H H H H H H H H	H H H H H H	L L L L L L	L L L L L L L L
49	–	X	L L L L L L L L L L L L L L L L	L L L L L L	H H H H H H	H H H H H H H H

test array waveforms



TEST ARRAY DELETED

			OPTION PRE/$\overline{OE}$	H
	AND		OR	
PRODUCT LINE	C	$\overline{C}$	INPUT (In) 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	PRESENT STATE (PS) 5 4 3 2 1 0	NEXT STATE (NS) 5 4 3 2 1 0	OUT (Qn) 7 6 5 4 3 2 1 0
48	–	–	H H H H H H H H H H H H H H H H	H H H H H H	– – – – – –	– – – – – – – –
49	–	X	L L L L L L L L L L L L L L L L	L L L L L L	– – – – – –	– – – – – – – –

X = Fuse intact, – = Fuse blown

TIB82S105B, 82S105A COMPARISON

The Texas Instruments TIB82S105B is a 16 × 48 × 8 Field-Programmable Logic Sequencer that is functionally equivalent to the Signetics 82S105A. However, the TIB82S105B is designed for a maximum speed of 50 MHz with the preset function being made conventional. As a result the TIB82S105B differs from the 82S105A in speed and in the preset recovery function.

The TIB82S105B is a high-speed version of the original 82S105A. The TIB82S105B features increased switching speeds with no increase in power. The maximum operating frequency is increased from 20 MHz to 50 MHz and does not decrease as more product terms are connected to each sum (OR) line. For instance, if all 48 product tems were connected to a sum line on the original 82S105A, the f_{max} would be about 15 MHz. The f_{max} for the TIB82S105B remains at 50 MHz regardless of the programmed configuration. In addition, the preset recovery sequence was changed to a conventional recovery sequence, providing quicker clock recovery times. This is explained in the following paragraph.

The TIB82S105B and the 82S105A are equipped with power-up preset and asynchronous preset functions. The power-up preset causes the registers to go high during power-up. The asynchronous preset inhibits clocking and causes the registers to go high whenever the preset pin is taken high. After a power-up preset occurs, the minimum setup time from power-up to the first clock pulse must be met in order to assure that clocking is not inhibited. In a similar manner after an asynchronous preset, the preset input must return low (inactive) for a given time, t_{su}, before clocking.

The Signetics 82S105A was designed in such a way that after both power-up preset and asynchronous preset it requires that a high-to-low clock transition occur before a clocking transition (low-to-high) will be recognized. This is shown in Figure 1. The Texas Instruments TIB82S105B does not require a high-to-low clock transition before clocking can be resumed, it only requires that the preset be inactive 8 ns (preset inactive-state setup time) before the clock rising edge. See Figure 2.

The TIB82S105B, with an f_{max} of 50 MHz, is ideal for systems in which the state machine must run several times faster than the system clock. It is recommended that the TIB82S105B be used in new designs. ***However, if the TIB82S105B is used to replace the 82S105A, then the customer must understand that clocking will begin with the first clock rising edge after preset.***

TABLE 3. SPEED DIFFERENCES

PARAMETER	82S105A SIGNETICS	TIB82S105B TI ONLY
f_{max}	20 MHz	50 MHz
t_{pd}, CLK to Q	20 ns	15 ns

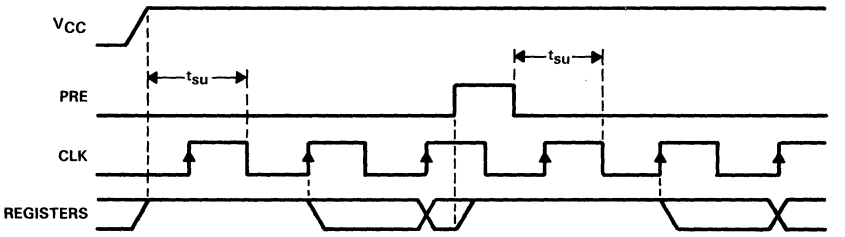


FIGURE 1. 82S105A PRESET RECOVERY OPERATION

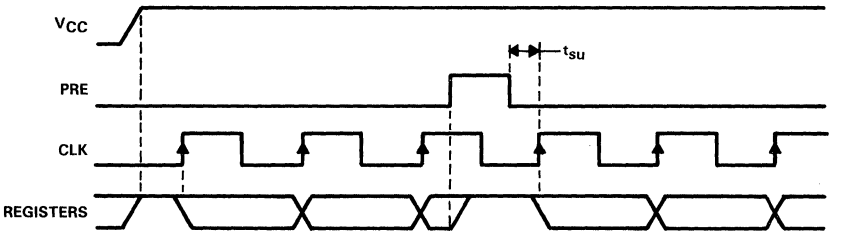


FIGURE 2. TIB82S105B PRESET RECOVERY OPERATION

D2896, JANUARY 1985—REVISED DECEMBER 1987

- **Programmable Asynchronous Preset or Output Control**
- **Power-On Preset of All Flip-Flops**
- **8-Bit Internal State Register with 4-Bit Output Register**
- **Power Dissipation . . . 600 mW Typical**
- **Functionally Equivalent to,† but Faster than 82S167A**

description

The TIB82S167B is a TTL field-programmable state machine of the Mealy type. This state machine (logic sequencer) contains 48 product terms (AND terms) and 12 pairs of sum terms (OR terms). The product and sum terms are used to control the 8-bit internal state register and the 4-bit output register.

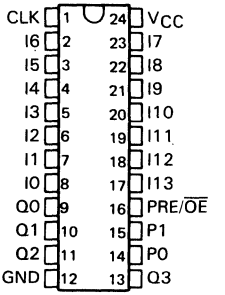
The outputs of the internal state register (P0-P7) are fed back and combined with the 14 inputs (I0-I13) to form the AND array. In addition the first two bits of the internal state register (P0-P1) are brought off-chip to allow the output register to be extended to 6 bits if desired. A single sum term is complemented and fed back to the AND array, which allows any of the product terms to be summed, complemented, and used as inputs to the AND array.

The state and output registers are positive-edge-triggered S/R flip-flops. These registers are unconditionally preset high on power-up. PRE/$\overline{OE}$ can be used as PRE to preset both registers or, by blowing the proper fuse, be converted to an output control function, $\overline{OE}$.

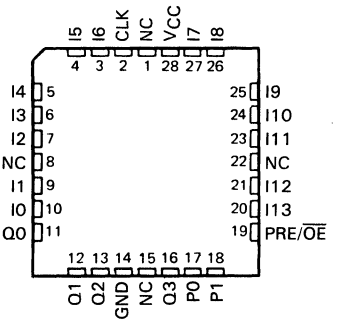
The TIB82S167BM is characterized for operation over the full military temperature range of −55°C to 125°C. The TIB82S167BC is characterized for operation from 0°C to 75°C.

† Power up preset and asynchronous preset functions are not identical to 82S167A.

M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FK OR FN PACKAGE
(TOP VIEW)



NC—No internal connection

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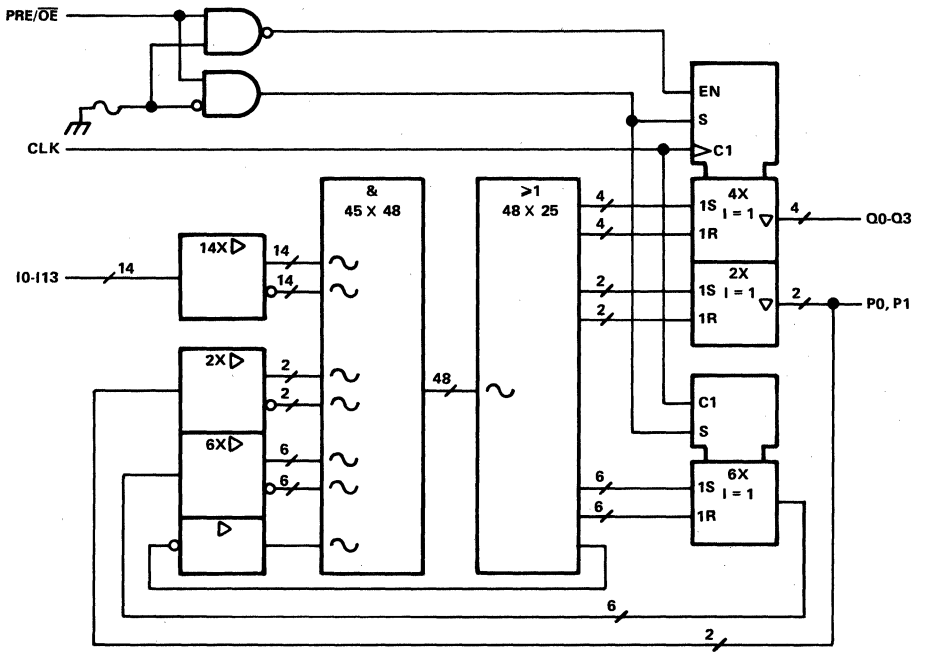
functional block diagram (positive logic)



∿ denotes fused inputs

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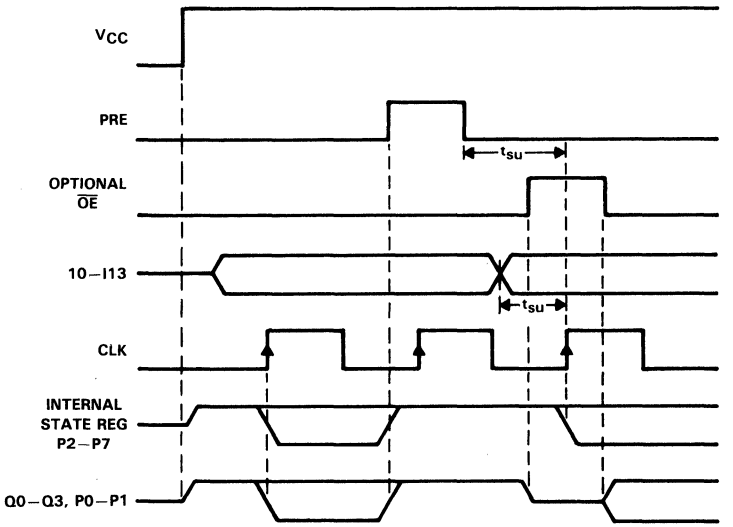
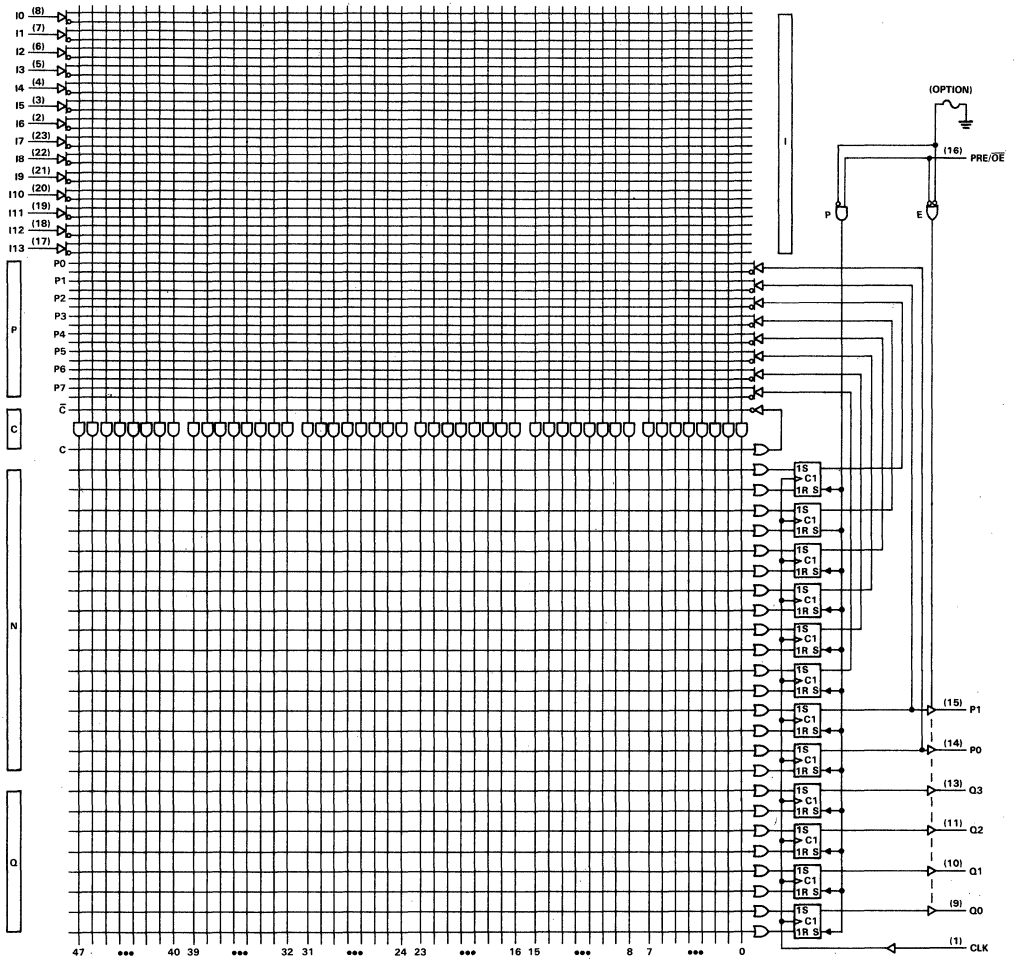
timing diagram



LOGIC DIAGRAM



NOTES: 1. All AND gate inputs with a blown link float to the high level.
2. All OR gate inputs with a blown link float to the low level.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 3) . . . . . 7 V
Input voltage (see Note 3) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 3) . . . . . 5.5 V
Operating free-air temperature range: TIB82S167BM . . . . . −55°C to 125°C
TIB82S167BC . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 3: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			M SUFFIX			C SUFFIX			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency†	1 thru 48 product terms without C-array‡	0		40	0		50	MHz
		1 thru 48 product terms with C-array	0		25	0		30	
t_w	Pulse duration	Clock high or low	12			10			ns
		Preset	18			15			
t_{su}	Setup time before CLK↑, 1 thru 48 product terms	Without C-array	20			15			ns
		With C-array	35			30			
t_{su}	Setup time, Preset low (inactive) before CLK↑§		10			8			ns
t_h	Hold time, input after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		75	°C

† The maximum clock frequency is independent of the internal programmed configuration. If an output is fed back externally to an input, the maximum clock frequency must be calculated.
‡ The C-array is the single sum term that is complemented and fed back to the AND array.
§ After Preset goes inactive, normal clocking resumes on the first low-to-high clock transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		M SUFFIX			C SUFFIX			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3		V
V_{OL}	V_{CC} = MIN,	I_{OL} = MAX		0.25	0.4		0.37	0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			25			25	μA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V			−0.25			−0.25	mA
I_O§	V_{CC} = MAX,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{OZH}	V_{CC} = MAX,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.4 V			−20			−20	μA
I_{CC}	V_{CC} = MAX, PRE/$\overline{OE}$ input at GND,	V_I = 4.5 V, Outputs open		90	160		90	160	mA

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}¶	Without C-array			R_L = 500 Ω, C_L = 50 pF	40	70		50	70		MHz
	With C-array				25	45		30	45		
t_{pd}		CLK↑	Q			10	20		10	15	ns
t_{pd}		PRE↑	Q			8	25		8	20	ns
t_{pd}		V_{CC}↑	Q			0	10		0	10	ns
t_{en}		$\overline{OE}$↓	Q			10	25		10	20	ns
t_{dis}		$\overline{OE}$↑	Q			5	15		5	10	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}.
¶ f_{max} is independent of the internal programmed configuration and the number of product terms used.

programming information

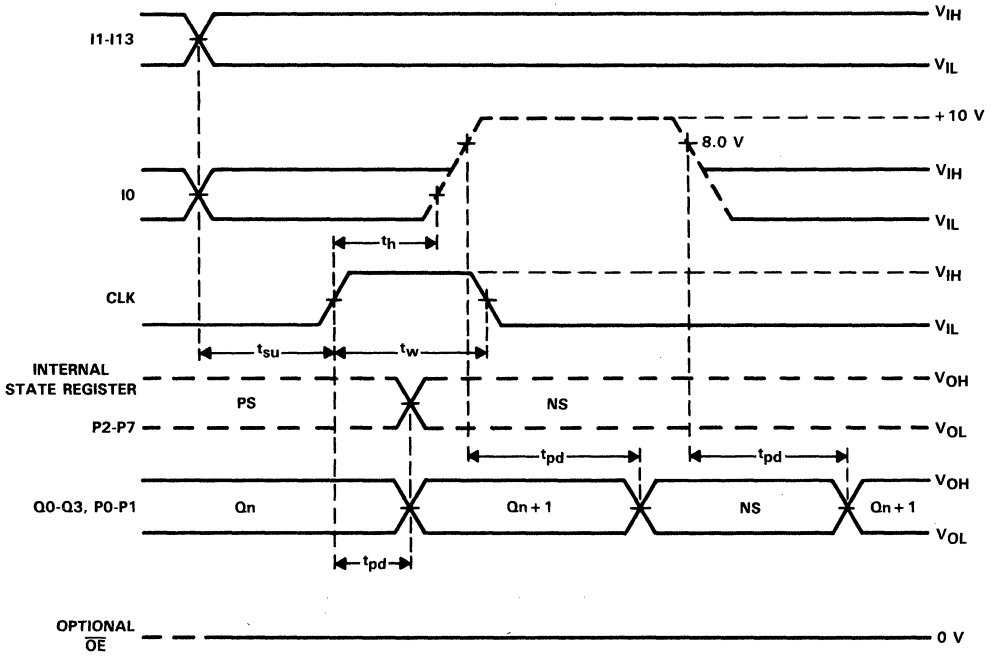
Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5762.

diagnostics

A diagnostics mode is provided with these devices that allows the user to inspect the contents of the state register. When I0 (pin 9) is held at 10 V, the state register bits P2-P7 will appear at the Q0-Q3 and P0-P1 outputs. The contents of the registers, Q0-Q3, and P0-P1 remain unchanged.

diagnostics waveforms



PS = Present State
NS = Next State

test array

A test array that consists of product lines 48 and 49 has been added to these devices to allow testing prior to programming. The test array is factory programmed as shown below. Testing is accomplished by connecting Q0-Q3 to I10-I13, PRE/$\overline{OE}$ to GND, and applying the proper input signals as shown in the timing diagram. Product lines 48 and 49 must be deleted during user programming to avoid interference with the programmed logic function.

test array program

| | | |

TIB82S167B, 82S167A COMPARISON

The Texas Instruments TIB82S167B is a 14 × 48 × 6 Field-Programmable Logic Sequencer that is functionally equivalent to the Signetics 82S167A. However, the TIB82S167B is designed for a maximum speed of 50 MHz with the preset function being made conventional. As a result the TIB82S167B differs from the 82S167A in speed and in the preset recovery function.

The TIB82S167B is a high-speed version of the original 82S167A. The TIB82S167B features increased switching speeds with no increase in power. The maximum operating frequency is increased from 20 MHz to 50 MHz and does not decrease as more product terms are connected to each sum (OR) line. For instance, if all 48 product tems were connected to a sum line on the original 82S167A, the f_{max} would be about 15 MHz. The f_{max} for the TIB82S167B remains at 50 MHz regardless of the programmed configuration. In addition, the preset recovery sequence was changed to a conventional recovery sequence, providing quicker clock recovery times. This is explained in the following paragraphs.

The TIB82S167B and the 82S167A are equipped with power-up preset and asynchronous preset functions. The power-up preset causes the registers to go high during power-up. The asynchronous preset inhibits clocking and causes the registers to go high whenever the preset pin is taken high. After a power-up preset occurs, the minimum setup time from power-up to the first clock pulse must be met in order to assure that clocking is not inhibited. In a similar manner after an asynchronous preset, the preset input must return low (inactive) for a given time, t_{su}, before clocking.

The Signetics 82S167A was designed in such a way that after both power-up preset and asynchronous preset it requires that a high-to-low clock transition occur before a clocking transition (low-to-high) will be recognized. This is shown in Figure 1. The Texas Instruments TIB82S167B does not require a high-to-low clock transition before clocking can be resumed, it only requires that the preset be inactive 8 ns (preset inactive-state setup time) before the clock rising edge. See Figure 2.

The TIB82S167B, with an f_{max} of 50 MHz, is ideal for systems in which the state machine must run several times faster than the system clock. It is recommended that the TIB82S167B be used in new designs. ***However, if the TIB82S167B is used to replace the 82S167A, then the customer must understand that clocking will begin with the first clock rising edge after preset.***

TABLE 3. SPEED DIFFERENCES

PARAMETER	82S167A SIGNETICS	TIB82S167B TI ONLY
f_{max}	20 MHz	50 MHz
t_{pd}, CLK to Q	20 ns	15 ns

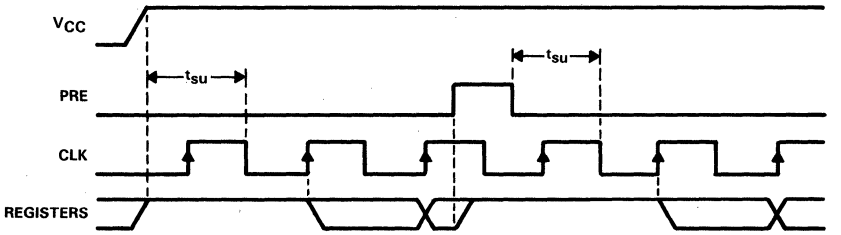


FIGURE 1. 82S167A PRESET RECOVERY OPERATION

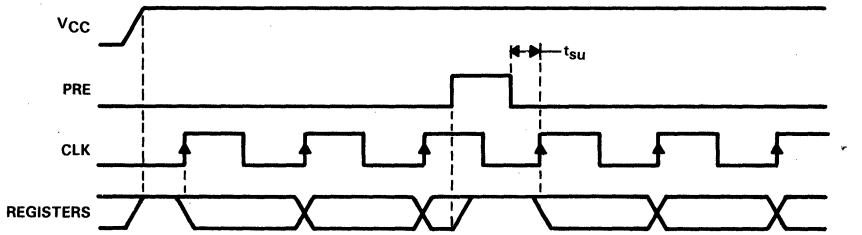


FIGURE 2. TIB82S167B PRESET RECOVERY OPERATION

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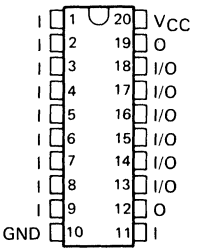
D2972, MARCH 1987—REVISED DECEMBER 1987

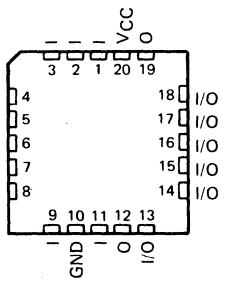
- **Mask-Programmed Version of 20-Pin PAL® Family**
- **Virtually Zero Standby Power**
- **35-ns Maximum Propagation Delay**
- **HC, HCT, and TTL Compatible**
- **Choice of 20-Pin DIP, 20-Pin SO (Small Outline) or 20-Pin PLCC Packages**
- **Low-Power Replacement for 20-Pin 'A' PAL® Devices**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	INPUTS	3-STATE Q OUTPUTS	REGISTERED OUTPUTS	I/O PORTS
'HAL16L8	10	2	0	6
'HAL16R4	8	0	4 (3-state)	4
'HAL16R6	8	0	6 (3-state)	2
'HAL16R8	8	0	8 (3-state)	0

TICHAL16L8
C SUFFIX . . . DW OR N PACKAGE
(TOP VIEW)



TICHAL16L8
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



description

These high-speed CMOS Hard Array Logic (HAL®) circuits are mask-programmed versions of the 20-pin PAL® devices. They provide reliable, high-speed, low-power substitutes for conventional TTL and HCT logic. They are also compatible with HC logic over V_{CC} range of 4.5 volts to 5.5 volts.

This family of CMOS HAL® circuits provide the flexibility of using integrated circuits with virtually zero standby power and lower operating power than those currently achieved by bipolar PALs. Prototyping can be done using standard PAL® devices before converting to CMOS HAL® circuits for production.

The TICHAL16' circuits have internal electrostatic discharge (ESD) protection circuits and have been classified with a 2000-volt ESD rating tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

The C suffix designates commercial-temperature circuits that are characterized for operation from 0°C to 75°C.

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PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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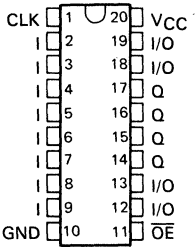
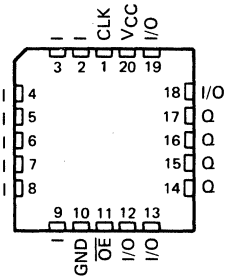
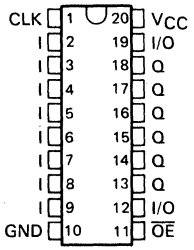
TICHAL16R4
C SUFFIX . . . DW OR N PACKAGE
(TOP VIEW)



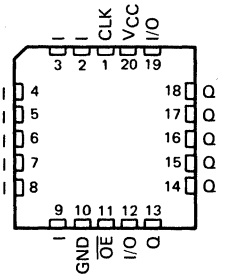
TICHAL16R4
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



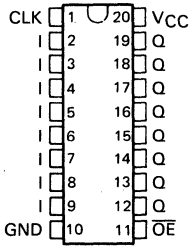
TICHAL16R6
C SUFFIX . . . DW OR N PACKAGE
(TOP VIEW)



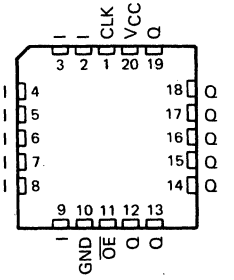
TICHAL16R6
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TICHAL16R8
C SUFFIX . . . DW OR N PACKAGE
(TOP VIEW)



TICHAL16R8
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



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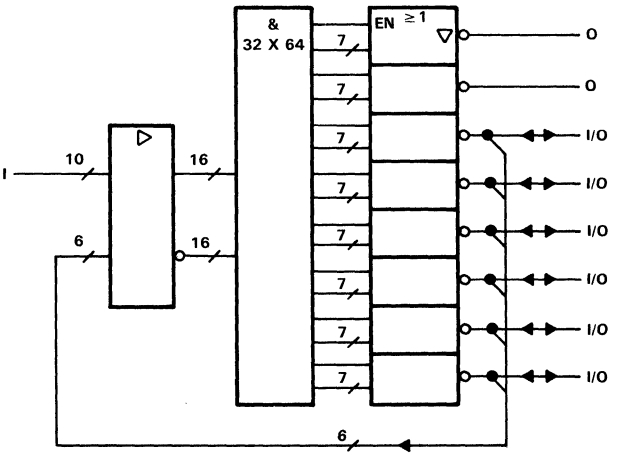
functional block diagrams (positive logic)

TICHAL16L8



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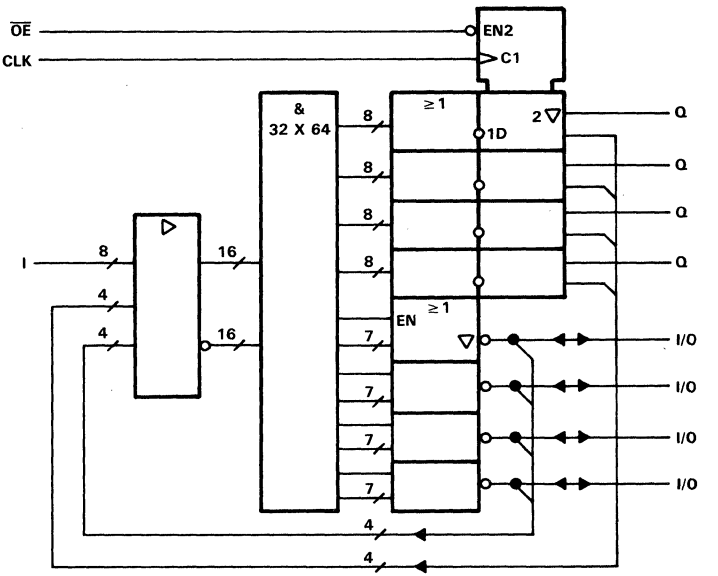
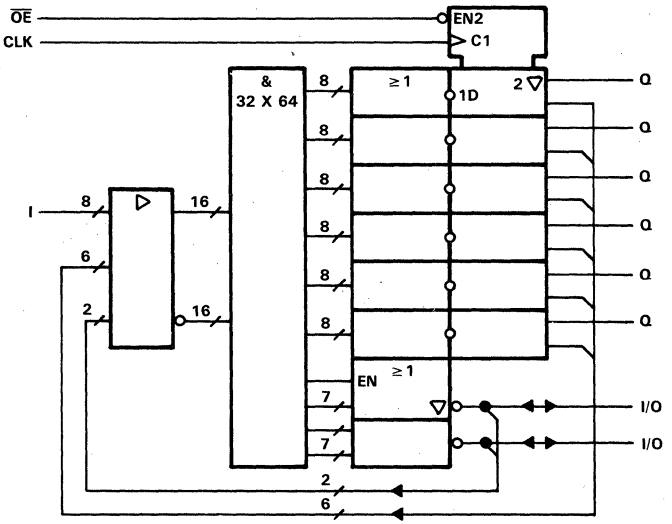


functional block diagrams (positive logic)

TICHAL16R6



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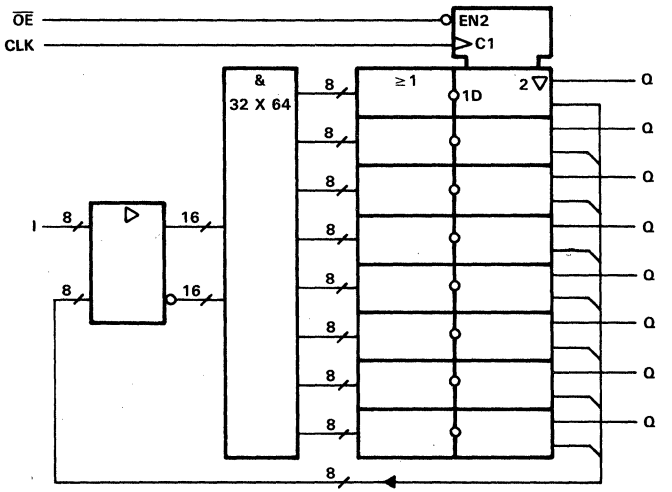

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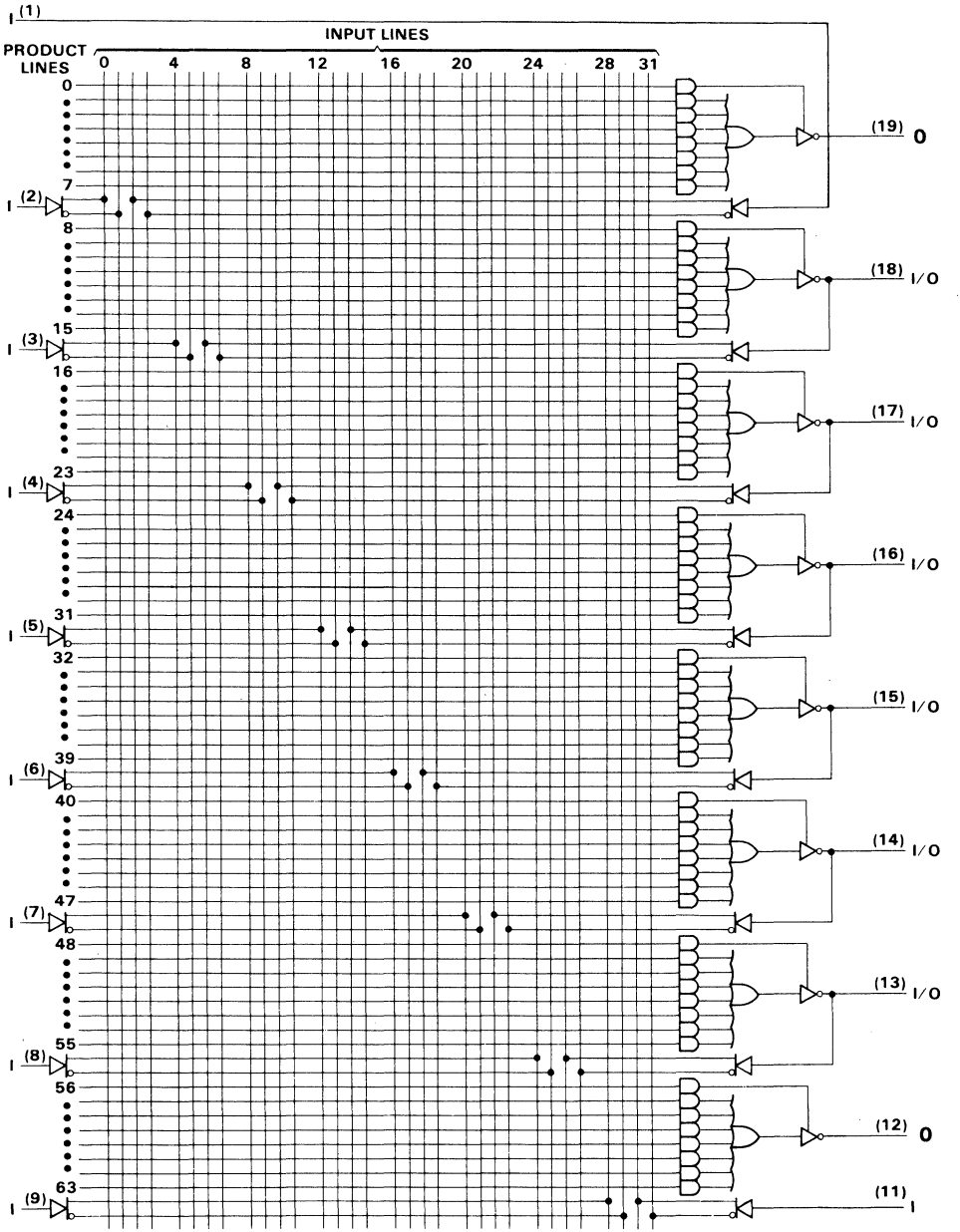
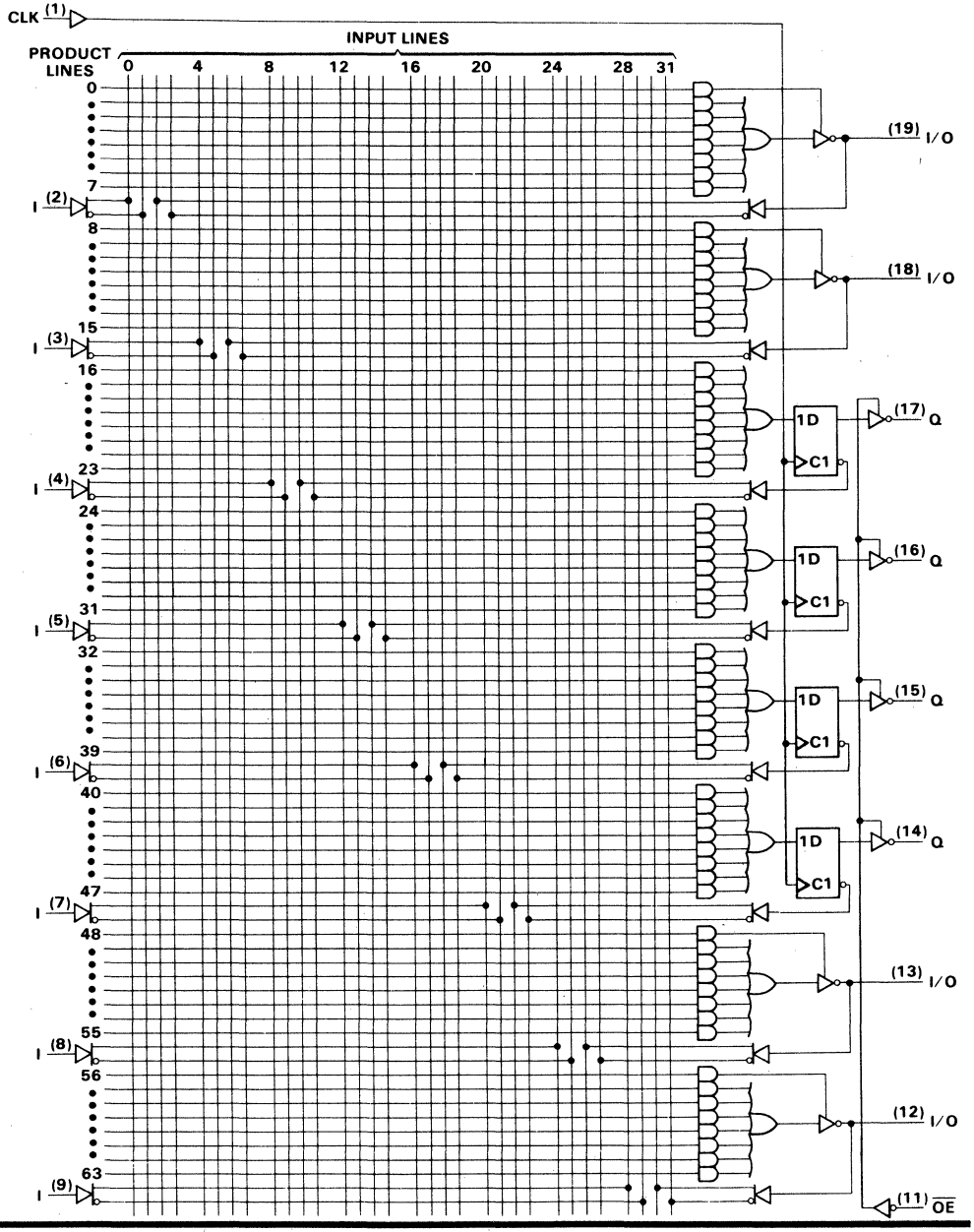
logic diagram (positive logic)



logic diagram (positive logic)



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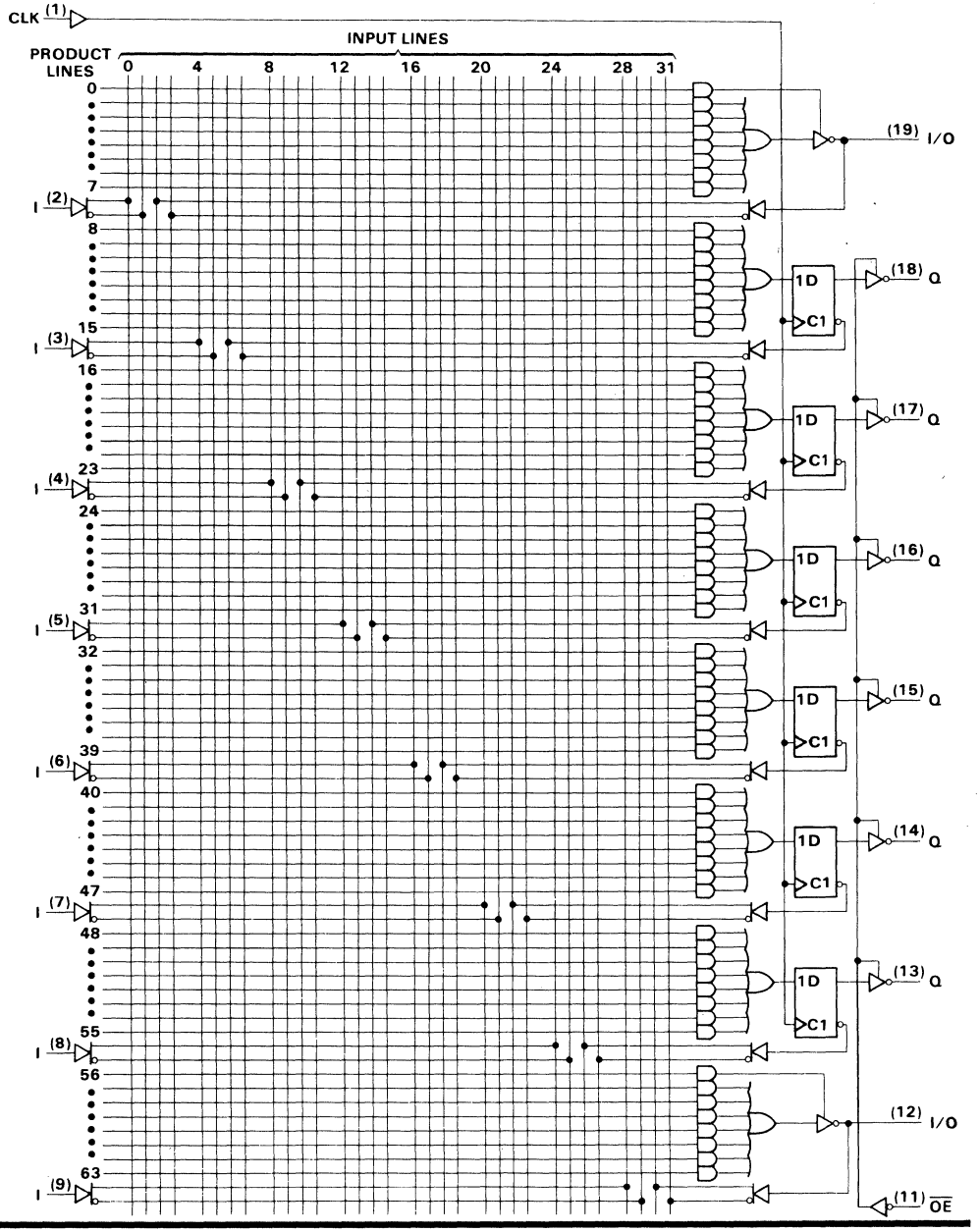
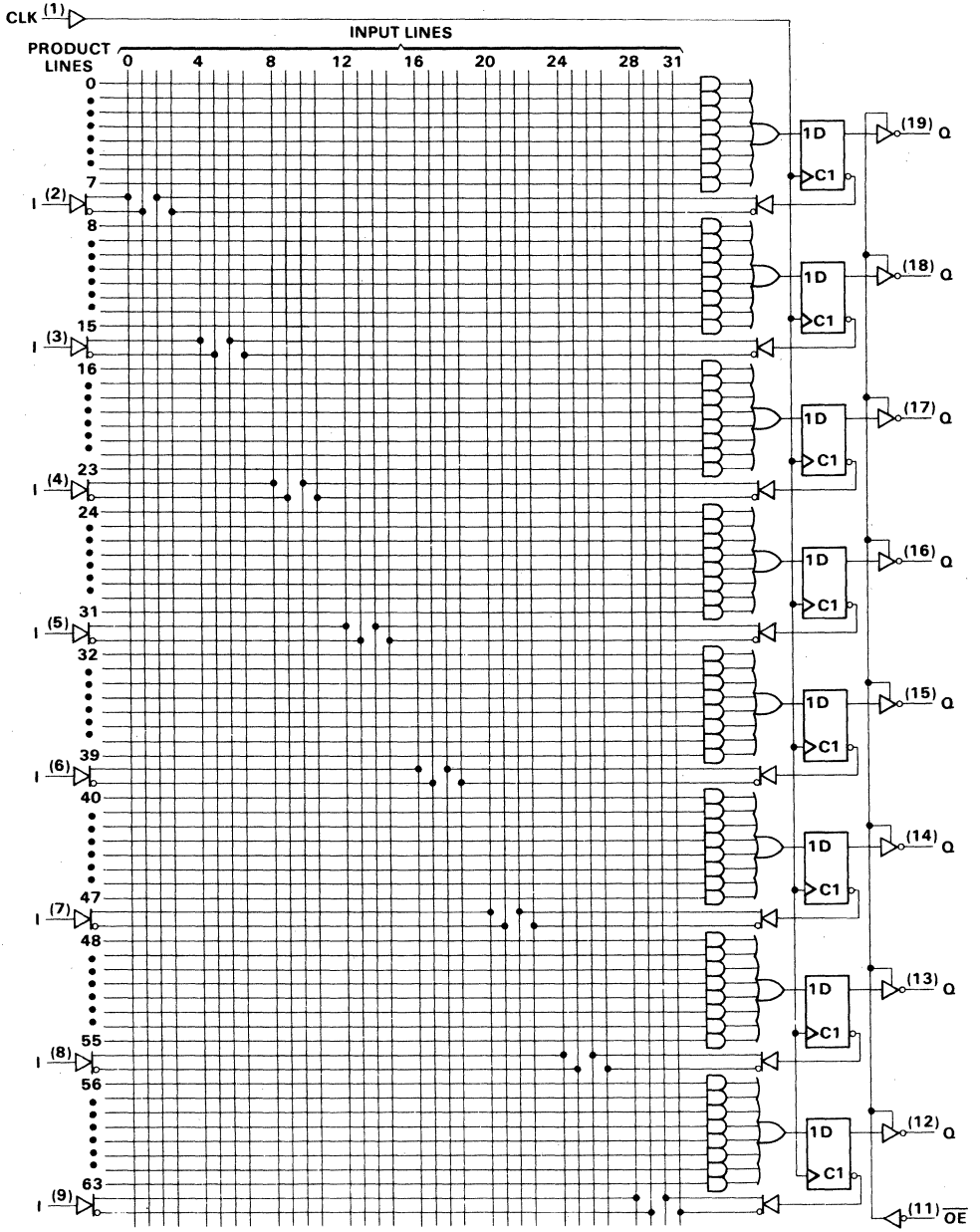
logic diagram (positive logic)



logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I . . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} pin . . . . . 70 mA
Continuous current through GND pin . . . . . −200 mA
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			C-SUFFIX			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5		5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
t_w	Pulse duration	Clock high	20			ns
		Clock low	20			
t_{su}	Setup time, input or feedback before CLK↑		30			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature range		0		75	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		C-SUFFIX MIN	C-SUFFIX TYP†	C-SUFFIX MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −6 mA	3.76			V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 24 mA			0.4	V
I_{OZH}	Off-state output current with high-level voltage applied	V_{CC} = 5.5 V,	V_O = V_{CC}			10	μA
I_{OZL}	Off-state output current with low-level voltage applied	V_{CC} = 5.5 V,	V_O = 0			−10	μA
I_{IH}	High-level input current	V_{CC} = 5.5 V,	V_I = V_{CC}			1	μA
I_{IL}	Low-level input current	V_{CC} = 5.5 V,	V_I = 0			−1	μA
I_{CC}	Standby supply current	V_{CC} = 5.5 V, I_O = 0	V_I = 0 or V_{CC},			100	μA
I_{CC}	Operating supply current	V_{CC} = 5.5 V, f ≥ 1 MHz,	V_I = 0 or V_{CC}, I_O = 0		2		mA/MHz
ΔI_{CC}‡	Change in supply current	V_{CC} = 5.5 V, Other inputs at 0 or V_{CC}	V_I = 0.5 V or 2.4 V,		1.4	3	mA
C_i	Input capacitance	T_A = 25°C,	f = 1 MHz			10	pF
C_o	Output capacitance	T_A = 25°C,	f = 1 MHz			10	pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	C-SUFFIX MIN	C-SUFFIX TYP†	C-SUFFIX MAX	UNIT
f_{max}§		with feedback	R_1 = 200 Ω, R_2 = 390 Ω, C_L = 50 pF	18			MHz
		without feedback		25			
t_{pd}	I, I/O, or feedback	O or I/O			18	35	ns
t_{pd}	CLK↑	Q			10	25	ns
t_{en}	$\overline{OE}$↓	Q			12	25	ns
t_{dis}	$\overline{OE}$↑	Q			12	25	ns
t_{en}	I or I/O	O or I/O			14	35	ns
t_{dis}	I or I/O	O or I/O			16	35	ns

† All typical values are V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 or V_{CC}.

§ f_{max} (with feedback) = $\frac{1}{t_{su} + t_{pd}\text{ (CLK to Q)}}$; f_{max} (without feedback) = $\frac{1}{t_w\text{(high)} + t_w\text{(low)}}$

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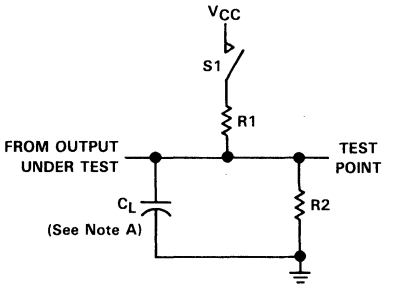
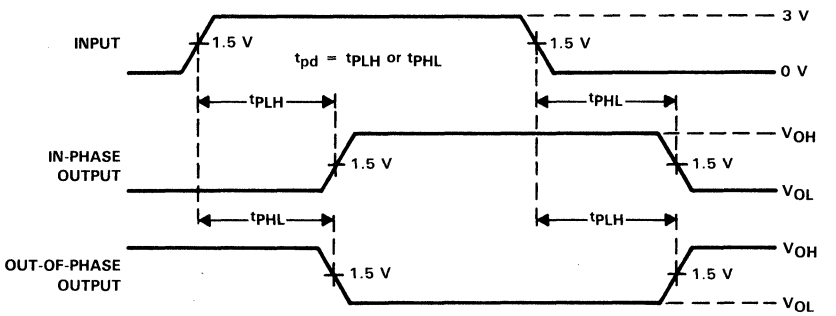
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L = includes probe and jig capacitance.
B. When measuring propagation times of 3-state outputs, S1 is closed.

FIGURE 1. LOAD CIRCUIT FOR THREE-STATE OUTPUTS

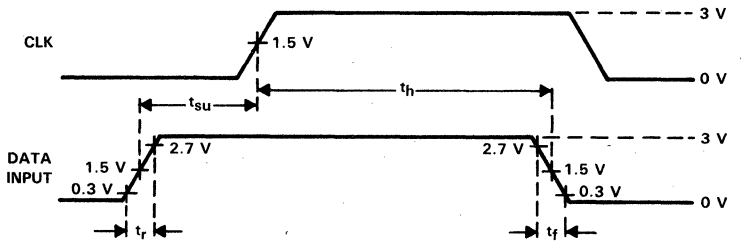


VOLTAGE WAVEFORMS

NOTES: A. When measuring propagation times of 3-state outputs, S1 is closed.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns.

FIGURE 2. PROPAGATION DELAY TIMES, OUTPUT RISE AND FALL TIMES

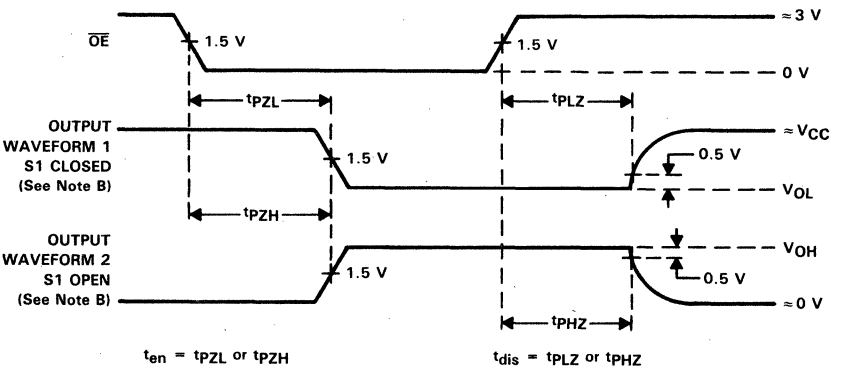
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTE: Phase relationship between waveforms was chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = t_r = 6 ns, t_f = 6 ns.

FIGURE 3. SETUP AND HOLD TIMES, AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 4. ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

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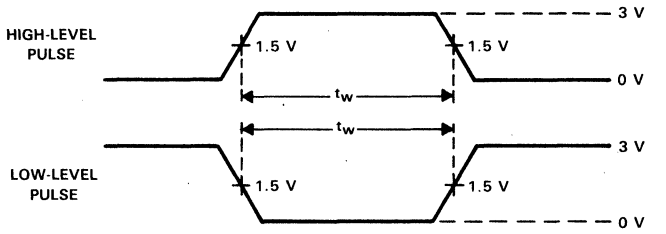
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns.
B. For clock inputs, f_{max} is measured with input duty cycle = 50%.

FIGURE 5. PULSE DURATIONS

- **Standard 20-Pin PAL Family**
- **Virtually Zero Standby Power**
- **Propagation Delay . . . 55 ns Max**
- **TTL- and HC-Compatible Inputs and Outputs**
- **Preload Capability to Aid Testing**
- **Fully Tested for High Programming Yield Before Packaging**
- **Greater than 2000-V Input Protection for Electrostatic Discharge**
- **Devices in the 'JL' Package Can Be Erased and Reprogrammed More Than Once**

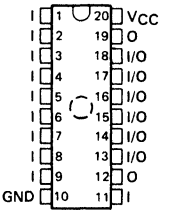
DEVICE	INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state)	4
PAL16R6	8	0	6 (3-state)	2
PAL16R8	8	0	8 (3-state)	0

description

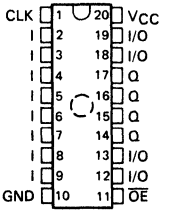
These PAL devices provide reliable, high-performance substitutes for conventional TTL and HCT logic. They are also compatible with HC logic over the V_{CC} range of 4.75 V to 5.25 V. Their easy programmability allows for quick design of "custom" functions and typically result in a more compact circuit board. Static power dissipation for these devices is negligible.

The output registers of these devices are D-type flip-flops that store data on the low-to-high transition of the clock input. The registered outputs may be disabled by taking $\overline{OE}$ high, whereas the nonregistered outputs may be disabled through the use of individual product terms. Unused inputs must always be connected to an appropriate logic level, preferably either V_{CC} or ground.

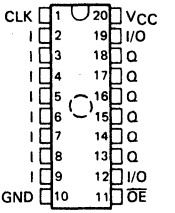
TICPAL16L8'
C SUFFIX . . . JL OR N PACKAGE
(TOP VIEW)



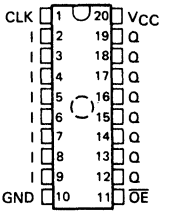
TICPAL16R4'
C SUFFIX . . . JL OR N PACKAGE
(TOP VIEW)



TICPAL16R6'
C SUFFIX . . . JL OR N PACKAGE
(TOP VIEW)



TICPAL16R8'
C SUFFIX . . . JL OR N PACKAGE
(TOP VIEW)



The dotted circles represent windows found only on the JL package.

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description (continued)

The programming cell consists of a floating-gate device like those used in EPROMs. All terms are initially connected. The unwanted terms are programmed out to provide the desired function. The output of a given AND gate is low if both the true and complement cells of a term are connected, and high if all related cells are programmed. Programming can be done manually but is usually achieved through the use of commercially available programming equipment.

This TICPAL16' series has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices, as exposure to ESD may result in a degradation of the device parametric performance.

The floating gate programmable cells allow these PALs to be fully programmed and tested before assembly to assure high field programming yield and functionality. They are then erased by ultraviolet light before packaging.

All devices in this series contain a security feature. Once the security cell is programmed, additional programming and verification cannot be performed. This prevents easy duplication of a design.

The TICPAL16'C series is characterized for operation from 0°C to 75°C.

erasure

The TICPAL16' (JL package) series can be erased after programming by exposure to ultraviolet light that has a wavelength of 253.7 nm (2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen $w \cdot s \cdot cm^{-2}$. The lamp should be located about 2.5 cm (1 inch) above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TICPAL16' series (JL package), the window should be covered with an opaque label.

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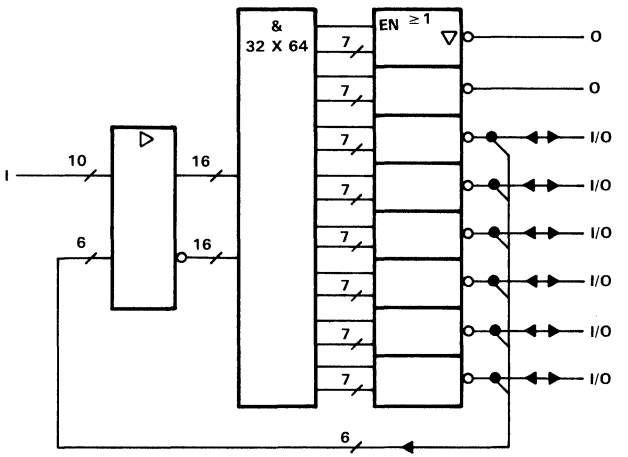
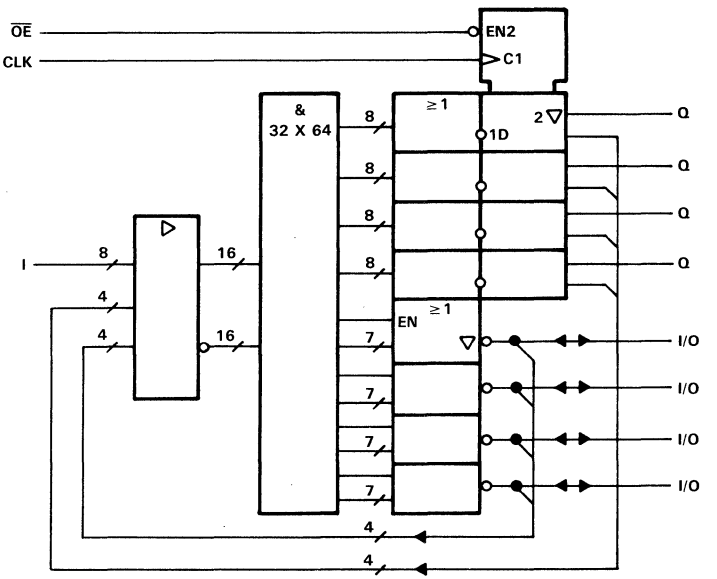
functional block diagrams (positive logic)

TICPAL16L8'

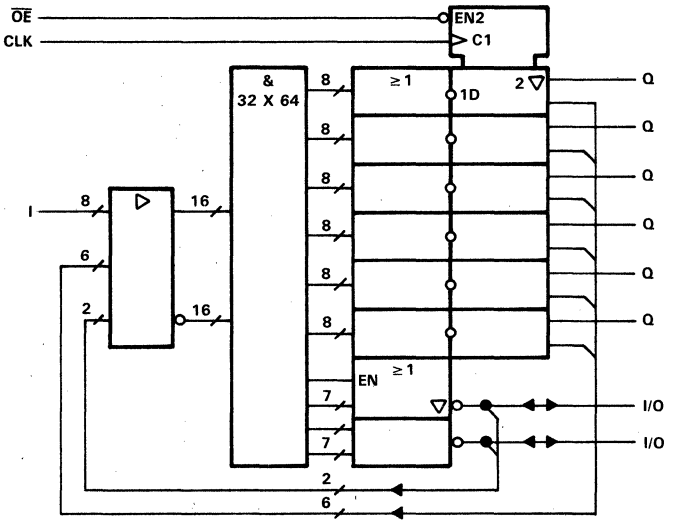


TICPAL16R4'

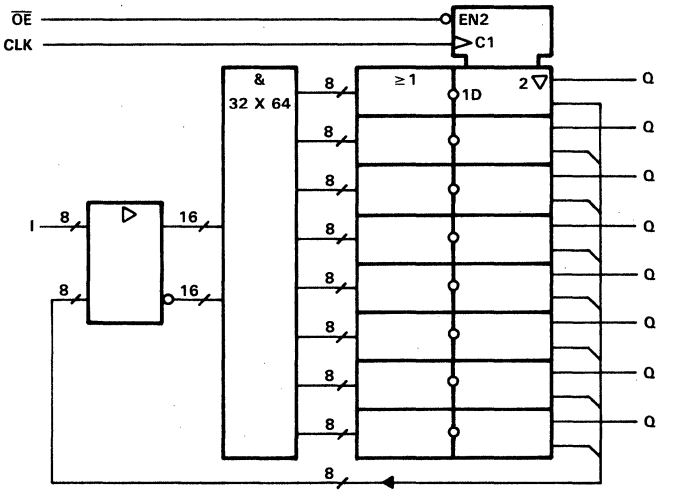


functional block diagrams (positive logic)

TICPAL16R6



TICPAL16R8



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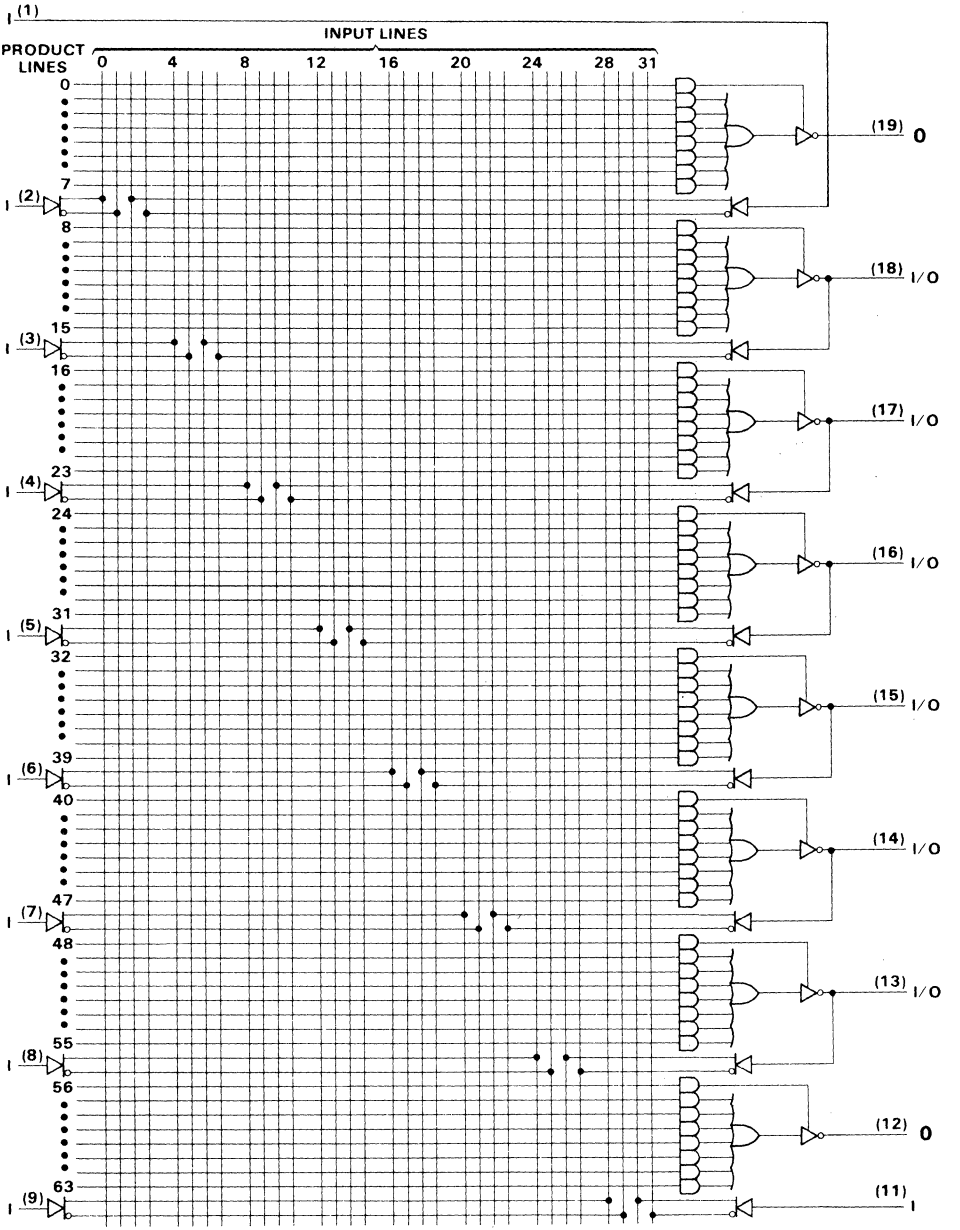
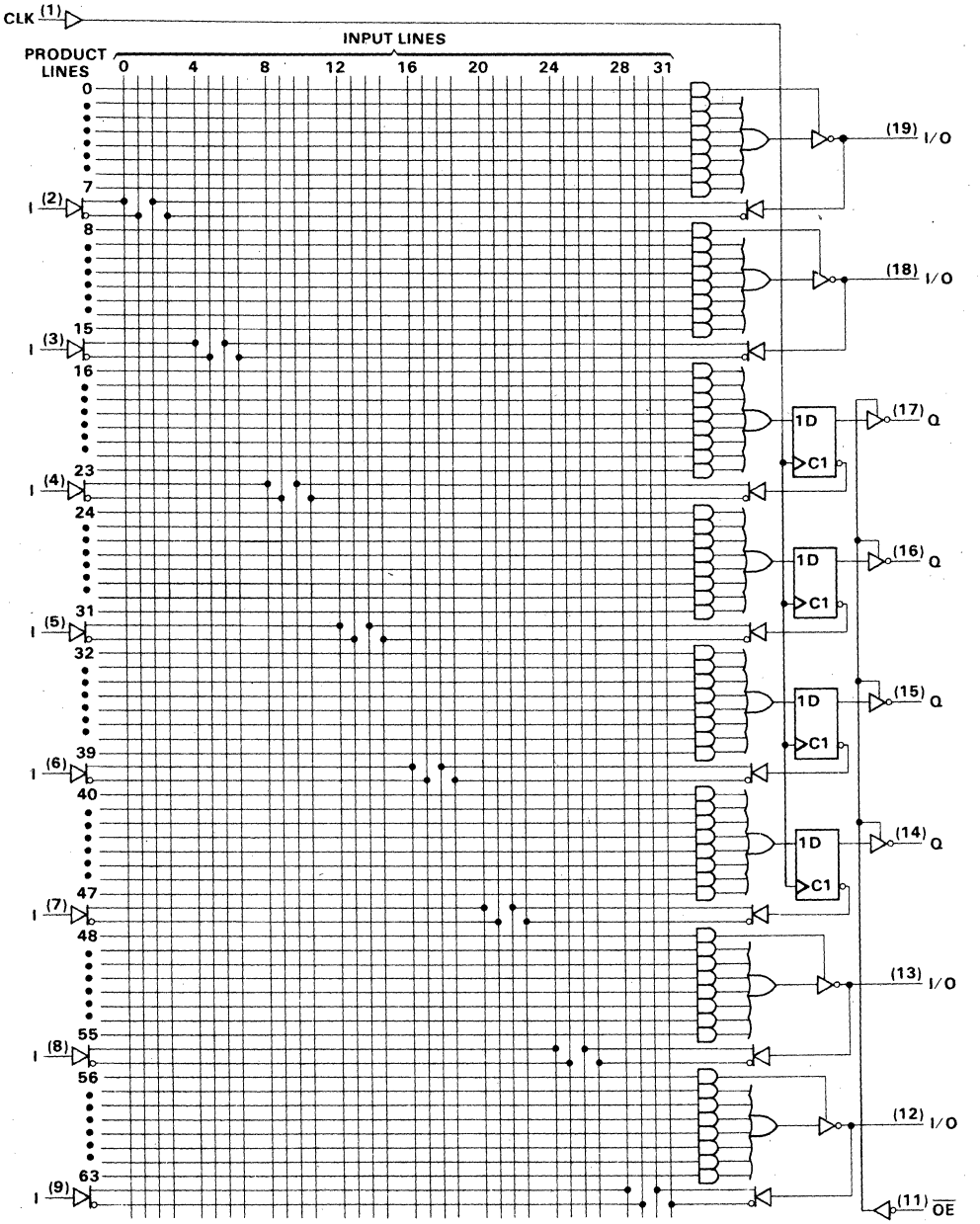
logic diagram (positive logic)



logic diagram (positive logic)



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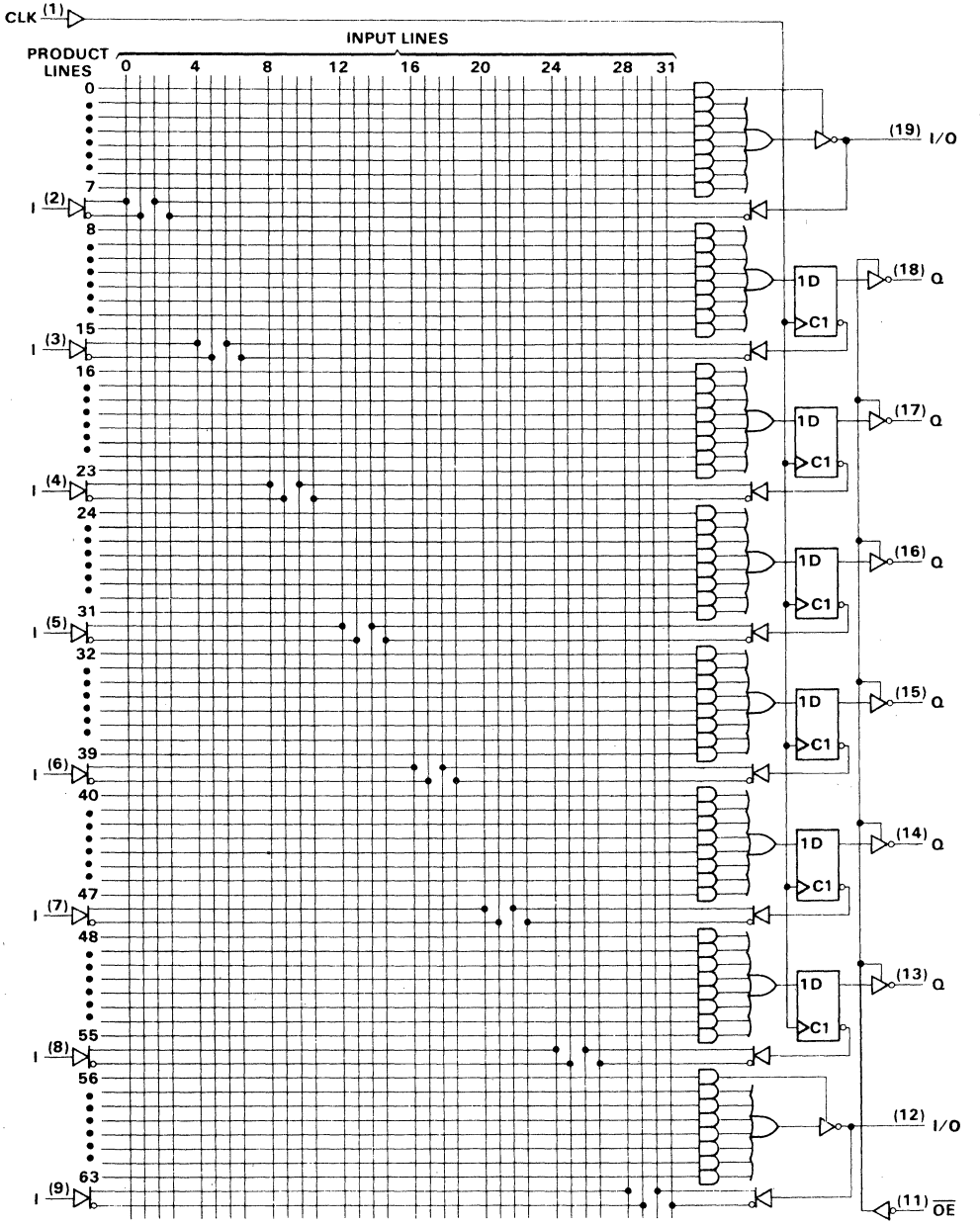
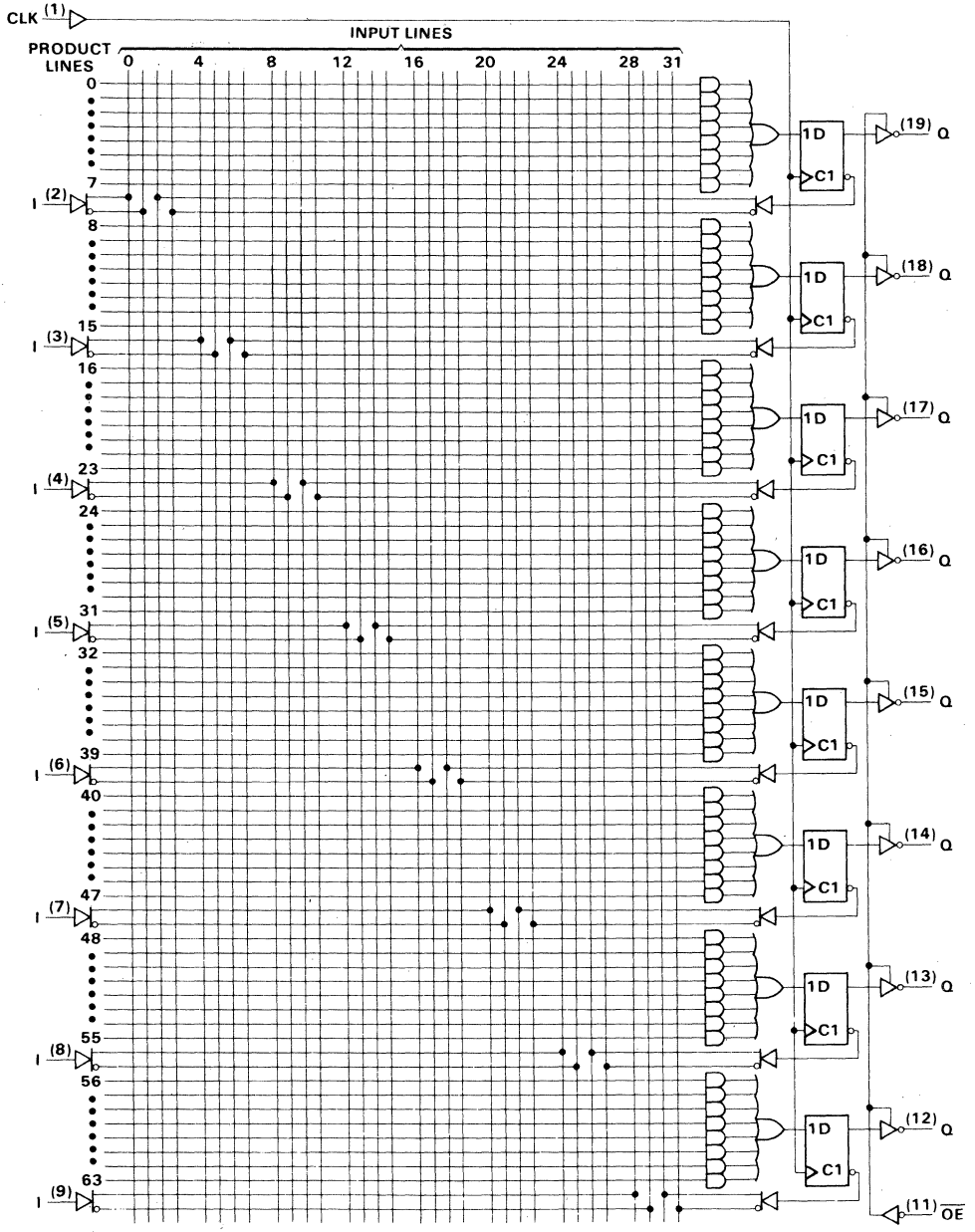
logic diagram (positive logic)



logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I . . . . . −0.5 V to V_{CC} +0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} pin . . . . . 70 mA
Continuous current through GND pin . . . . . −200 mA
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds (JL package) . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds (N package) . . . . . 260°C

recommended operating conditions

			C-SUFFIX			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75		5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
t_w	Pulse duration	Clock high	20			ns
		Clock low	20			
t_{su}	Setup time, input or feedback before CLK↑		40			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature range		0		75	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = 3.2 mA (for TTL)		4			V
	V_{CC} = 4.75 V,	I_{OH} = −4 mA (for CMOS)		3.86			
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA (for TTL)		0.5			V
	V_{CC} = 4.75 V,	I_{OL} = 4 mA (for CMOS)		0.4			
I_{OZH}	V_{CC} = 5.25 V,	V_O = 2.4 V				10	μA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.4 V				−10	μA
I_{IH}	V_{CC} = 5.25 V,	V_I = V_{CC}				10	μA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0				−10	μA
$I_{CC(standby)}$	V_{CC} = 5.25 V,	V_I = 0 or V_{CC},	I_O = 0			100	μA
$\frac{I_{CC(operating)}}{f}$	V_{CC} = 5.25 V, f = 1 MHz to 25 MHz	V_I = 0 to V_{CC},	I_O = 0,		2		$\frac{mA}{MHz}$
‡ΔI_{CC}	V_{CC} 5.25 V, Other inputs at 0 V or V_{CC}	V_I = 0.5 V or 2.4 V,			1.4	3	mA
C_i	T_A = 25°C,	f = 1 MHz			6		pf

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) R1 = 200 Ω, R2 = 390 Ω, C_L = 50 pf

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
f_{max}§		with feedback	16			MHz
		w/o feedback	25			
t_{pd}	I, I/O, or feedback	O or I/O		35	55	ns
t_{pd}	CLK↑	Q		15	22	ns
t_{en}	$\overline{OE}$↓	Q		15	25	ns
t_{dis}	$\overline{OE}$↑	Q		15	25	ns
t_{en}	I or I/O	Q or I/O		35	55	ns
t_{dis}	I or I/O	Q or I/O		35	55	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 or V_{CC}.
§$f_{max(with\ feedback)} = \frac{1}{t_{su} + t_{pd}\ (CLK\ to\ Q)}$; $f_{max(without\ feedback)} = \frac{1}{t_{su}}$

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preload procedure for registered outputs

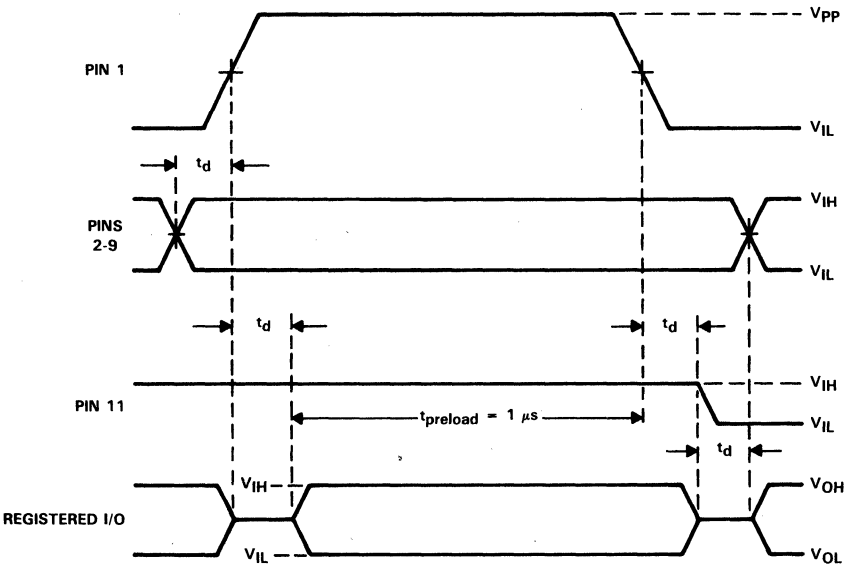
The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. All of the registers may be preloaded simultaneously by following the steps below.

Step 1. With V_{CC} at 5 V and Pin 11 at V_{IH}, raise Pin 1 to V_{IHH}.

Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.

Step 3. Lower Pin 1 to V_{IL}, then remove the output voltage. Preload can be verified by lowering Pin 11 to V_{IL} and observing the voltage level at the output pins.

preload waveforms

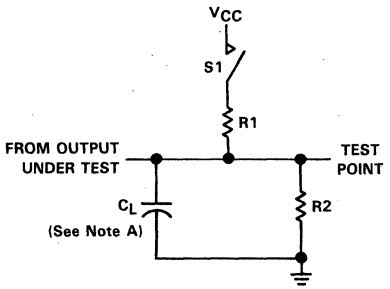


preload parameters, T_A = 25°C

PARAMETER†		MIN	NOM	MAX	UNIT
V_{IHH}	Preload voltage on pin 1	12.5	13	13.5	V
I_{IHH}	Preload input current at pin 1	3.2	4	4.8	mA
$\Delta v/\Delta t$	Voltage ramping (V_{IHH})	50			V/µs
t_d	Setup and hold times	2			µs

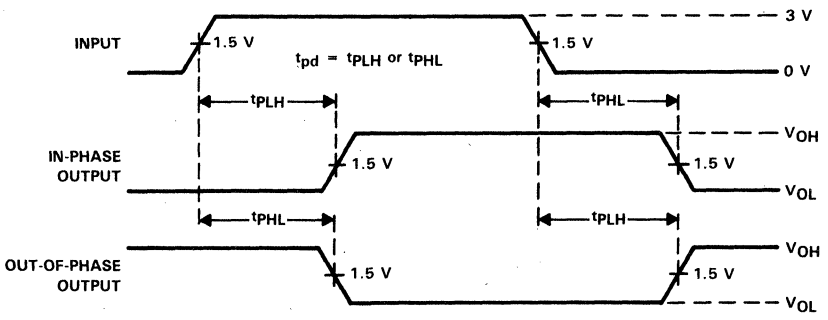
†Other test parameters and conditions are shown in recommended operating conditions and electrical characteristics tables.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L = includes probe and jig capacitance.
B. When measuring propagation times of 3-state outputs, S1 is closed.

FIGURE 1. LOAD CIRCUIT FOR THREE-STATE OUTPUTS



VOLTAGE WAVEFORMS

NOTES: A. When measuring propagation times of 3-state outputs, S1 is closed.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns.

FIGURE 2. PROPAGATION DELAY TIMES, OUTPUT RISE AND FALL TIMES

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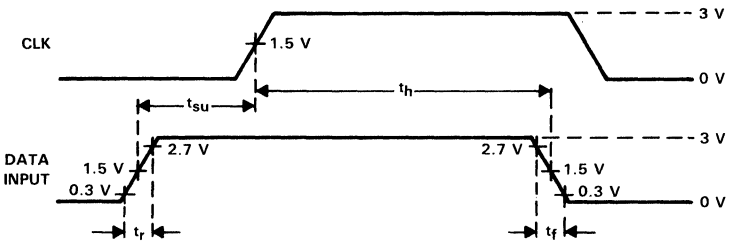
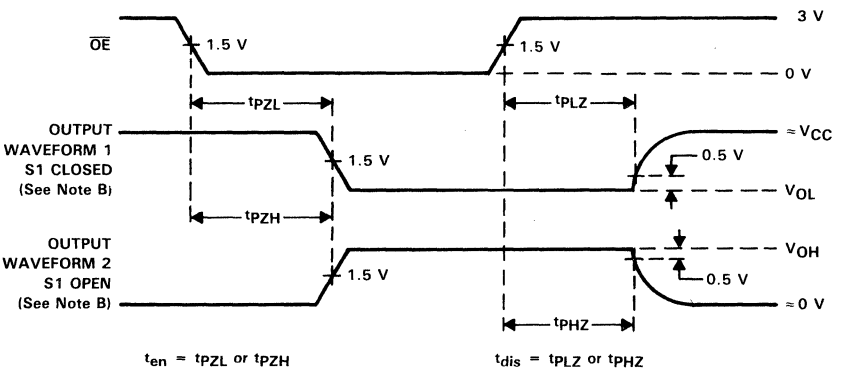
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTE: Phase relationship between waveforms was chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = t_r = 6 ns, t_f = 6 ns.

FIGURE 3. SETUP AND HOLD TIMES, AND INPUT RISE AND FALL TIMES

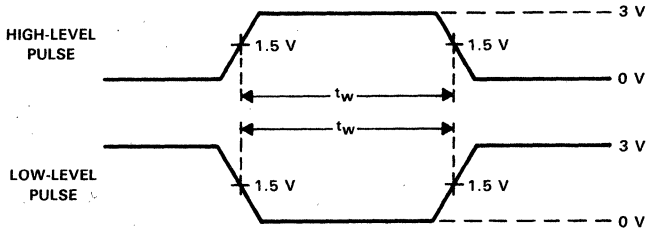


VOLTAGE WAVEFORMS

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 4. ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns.
B. For clock inputs, f_{max} is measured with input duty cycle = 50%.

FIGURE 5. PULSE DURATIONS

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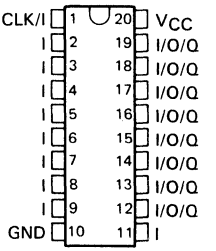
D3087, DECEMBER 1987

- 20-Pin Advanced CMOS Generic PAL
- Virtually Zero Standby Power
- 25-ns Maximum Propagation Delay
- Eight Output Logic Macrocells
  - Each OLM Is User-Programmable for Registered or Combinational Operation, Polarity, and Output Enable Control
- UV-Light-Erasable Cell Technology Allows for:
  - Reconfigurable Logic
  - Reprogrammable Cells
  - Full Factory Testing for Guaranteed 100% Yields
- Preload Capability on All Registered Outputs Allows for 100% Functional Testing
- Power-Up Clear
- Programmable Design Security Bit Prevents Copying of Logic Stored in Device
- The TICPAL18V8 Replaces the PAL Functions in Table 1

JL PACKAGE
(TOP VIEW)



Pin assignments in operating mode

description

This PAL device features advanced CMOS speed and virtually zero standby power. It combines TI's EPIC™ (Enhanced Processed Implanted CMOS) process with ultraviolet-light-erasable EPROM technology. Each output has an Output Logic Macrocell (OLM) configuration allowing for user definition of the output type. This PAL provides reliable, low-power substitutes for numerous high-performance TTL PALs.

TABLE 1. PAL FUNCTIONS

CLK/I –	–	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
I –	–	0	I	I	I	Q	I/O	I/O	0	0	I/O
I –	–	0	0	I	I	Q	Q	I/O	I/O	0	I/O
I –	–	0	0	0	I	Q	Q	Q	I/O	0	I/O
I –	–	0	0	0	0	Q	Q	Q	I/O	0	I/O
I –	–	0	0	0	0	Q	Q	Q	I/O	0	I/O
I –	–	0	0	0	I	Q	Q	Q	I/O	0	I/O
I –	–	0	0	I	I	Q	Q	I/O	I/O	0	I/O
I –	–	0	I	I	I	Q	I/O	I/O	0	0	I/O
GND –	–	I	I	I	I	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	I	I	I
		10L8	12L6	14L4	16L2	16R8	16R6	16R4	16L8	16LD8	18P8
		10H8	12H6	14H4	16H2	16RP8	16RP6	16RP4	16H8	16HD8	
		10P8	12P6	14P4	16P2				16P8		

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description (continued)

architecture

The 'PAL18V8 architecture is a generic version of the 20-pin family of PALs. This generic flexibility is achieved by the implementation of each output function with an Output Logic Macrocell (OLM). The OLM contains architectural options configured through programming. These options include the user selection of combinatorial or registered outputs with a choice of active-high or active-low logic.

The 'PAL18V8 has 74 product terms in the AND array, 64 of which are OR-function product terms, 8 product terms that are used as bidirectional output controls, and 1 product term each as asynchronous reset and synchronous set control, respectively. Each of the 8 outputs has 8 product terms per OR function and a dedicated product term for the bidirectional control of that output. The bidirectional control allows for individual outputs to be forced into the high-impedance state for bidirectional operations or for dedicated input usage.

The circuit design is enhanced by the addition of synchronous set and asynchronous reset product terms. These two functions are common to all the OLMs. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0 independently of the clock. The output logic level after set or reset depends on the polarity selected during programming. An asynchronous reset always overrides synchronous set.

A clock function is routed to all the OLMs. It is used with the registered macrocell options. The clock function shares a pin with an array input. The sharing provides an additional input pin when registered options are not exercised.

The registers in the '18V8 have been designed to reset after power-up. During power-up, all registers will reset to the 0-state following a transition of any input or any I/O. The output voltage level for any output will depend on the polarity selected for that output. This feature is especially valuable in simplifying state machine initialization.

All output registers can be preloaded to any desired state during testing. Preloading permits full logical verification during device testing.

The TICPAL18V8 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices, as exposure to ESD may result in a degradation of the device parametric performance.

The floating gate programmable cells allow these PALs to be fully programmed and tested before assembly to assure high field programming yield and functionality. They are then erased by ultraviolet light before packaging.

The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The C-suffix devices are characterized for operation from 0°C to 75°C.

design security

The 'PAL18V8 contains a programmable design security bit. Programming this bit will disable the read verify and programming circuitry, protecting the design from being copied. The security bit is usually programmed after the design is finalized and released to production. A secured device will verify as if every location in the device is programmed. Because programming is accomplished by storing an invisible charge instead of opening a metal link, the '18V8 cannot be copied by visual inspection. Once a secured device is fully erased, it can be reprogrammed to any desired configuration.

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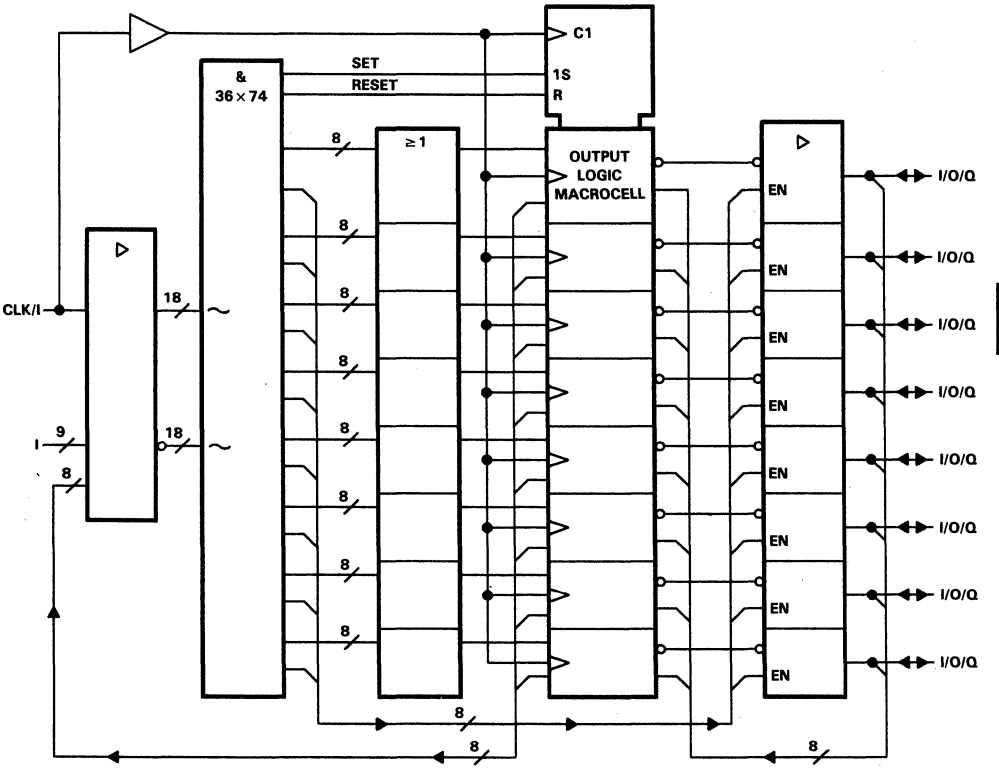
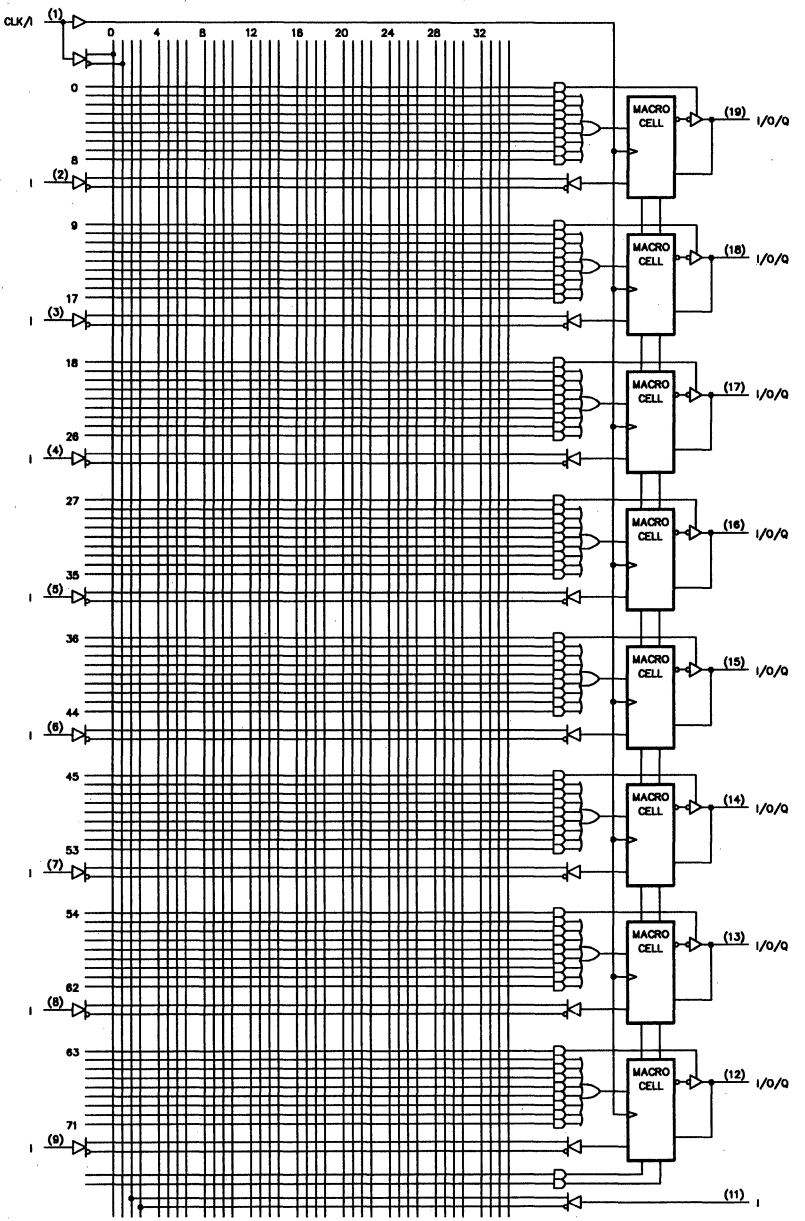
functional block diagram (positive logic)



~ denotes fused inputs

logic diagram (positive logic)

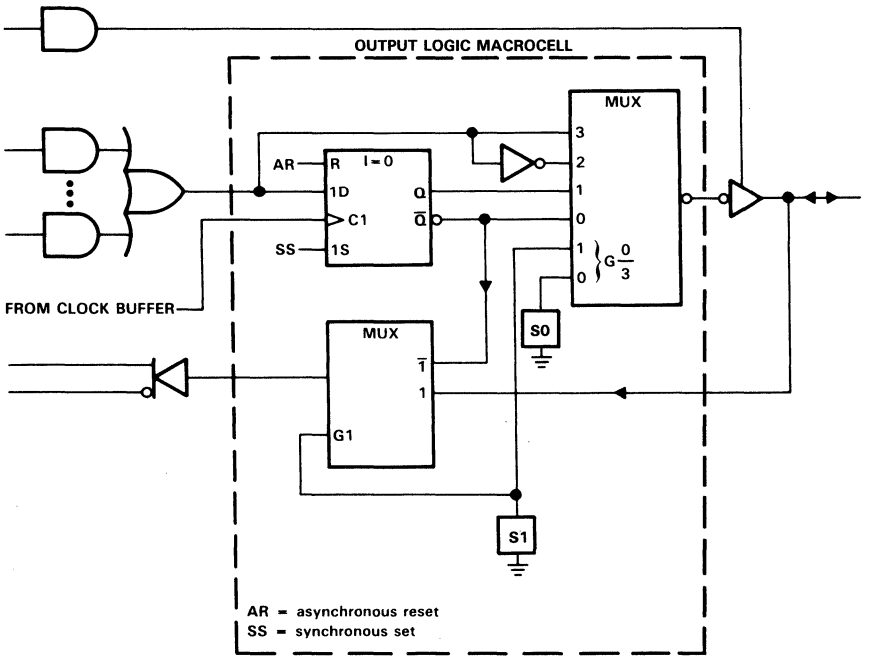


output logic macrocell (OLM) description

A great amount of architectural flexibility is provided by the user-configurable macrocell output options. The macrocell consists of a D-type flip-flop and two select multiplexers. The D-type flip-flop operates like a standard TTL D-type flip-flop. The input data is latched on the low-to-high transition of the clock input. The Q and $\overline{Q}$ outputs are made available to the output select multiplexer. The asynchronous reset and synchronous set controls are available in all flip-flops.

The select multiplexers are controlled by programmable bits. The combination of these programmable bits will determine which macrocell functions are implemented. It is this user control of the architectural structure that provides the generic flexibility of this device.

output logic macrocell diagram

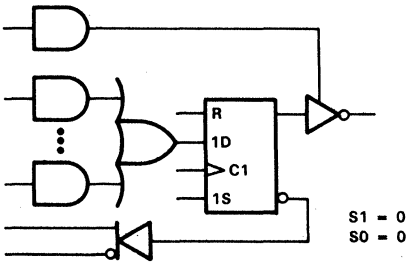


output logic macrocell options

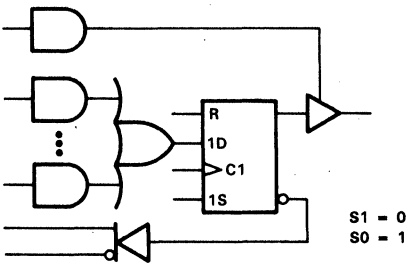
MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

CELL SELECT		FEEDBACK AND OUTPUT CONFIGURATION		
S1	S0			
0	0	Register feedback	Registered	Active low
0	1	Register feedback	Registered	Active high
1	0	I/O feedback	Combinational	Active low
1	1	I/O feedback	Combinational	Active high

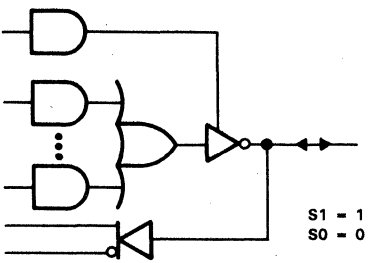
0 = erased cell, 1 = programmed cell
S1 and S0 are select-function cells as shown in the output logic macrocell diagram.



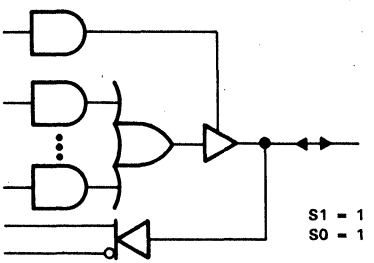
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage, V_I (see Note 1) . . . . . −0.5 V to V_{CC}+0.5 V
Input diode current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output diode current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±40 mA
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except during programming and preload cycles.
Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			−30M			−25C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		V_{CC}+0.5	2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Driving TTL			−2			−3.2	mA
		Driving CMOS			−2			−4	
I_{OL}	Low-level output current	Driving TTL			12			24	mA
		Driving CMOS			2			4	
f_{clk}	Clock frequency								MHz
t_w	Pulse duration	CLK high	10			8			ns
		CLK low	11			9			
		Asynchronous reset	30			25			ns
t_{su}	Setup time	Input or feedback	25			20			ns
		Reset inactive state	30			25			
t_h	Hold time	Input or feedback	0			0			ns
T_A	Operating free-air temperature		−55		125	0		75	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			−30M MIN	−30M TYP‡	−30M MAX	−25C MIN	−25C TYP‡	−25C MAX	UNIT
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	TTL	4			4			V
	V_{CC} = MIN,	I_{OH} = MAX	CMOS	3.86			3.86			V
V_{OL}	V_{CC} = MIN,	I_{OL} = MAX	TTL			0.5			0.5	V
	V_{CC} = MIN,	I_{OL} = MAX	CMOS			0.4			0.4	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.7 V							10	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V							−10	μA
I_{IH}	V_{CC} = MAX,	V_I = 5.25 V							10	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V							−10	μA
I_O§	V_{CC} = MAX,	V_O = 0.5 V		−30		−130	−30		−130	mA
I_{CC}	V_{CC} = MAX, Outputs open¶	V_I = 0 or V_{CC},				100			100	μA
$\frac{I_{CC}}{f}$	V_{CC} = MAX, f ≥ 1 MHz	v_i = 0 to 3 V,			2			2		mA/MHz
ΔI_{CC}#	V_{CC} = MAX, One input at 0.5 V or 2.4 V, Other inputs at 0 V or V_{CC}		Pin 1			4			4	mA/ Input
			Others			2			2	
C_i	V_I = 2 V, f = 1 MHz, T_A = 25°C	Pin 2			15			15		pF
		Clock Pin			12			12		
		All I/O Pins			15			15		
		Other inputs			10			10		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	−30M MIN	−30M TYP‡	−30M MAX	−25C MIN	−25C TYP‡	−25C MAX	UNIT
f_{max}‖	W/O feedback		C suffix:		50			50		MHz
	With feedback		R1 = 200 Ω, R2 = 390 Ω,		35			35		
t_{pd}	I, I/O	O, I/O	C_L = 50 pF		15	30		15	25	ns
t_{pd}	CLK↑	Q	M suffix:		12			12		ns
t_{pd}	Reset	Q	R1 = 390 Ω, R2 = 750 Ω,		20			10		ns
t_{en}	I, I/O	I,Q, I/O	C_L = 50 pF		15			15		ns
t_{dis}	I, I/O	I,Q, I/O	C_L = 5 pF, See Figure 4		15			15		ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§This parameter approximates I_{OS}. The condition V_O = 0.5 V takes tester noise into account.
¶Disabled outputs tied to GND or V_{CC}.
#This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than at 0 V or V_{CC}.
‖$f_{max(\text{with feedback})} = \frac{1}{t_{su} + t_{pd(\text{CLK to Q})}}$; $f_{max(\text{without feedback})} = \frac{1}{t_{w(\text{high})} + t_{w(\text{low})}}$

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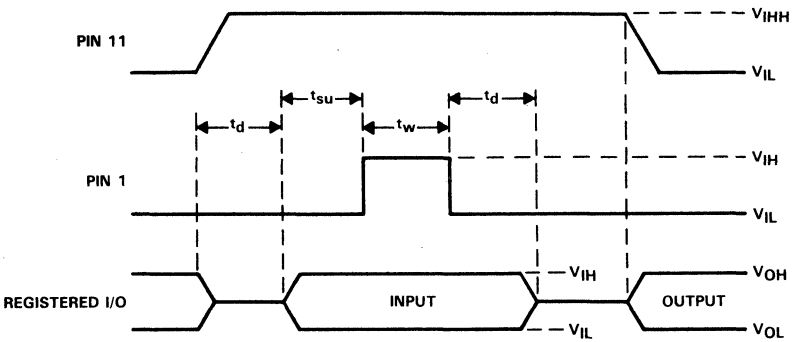
preload procedure for registered outputs

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below. The output level depends on the polarity selected during programming.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 11 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 11 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

preload waveforms (see Note 2)

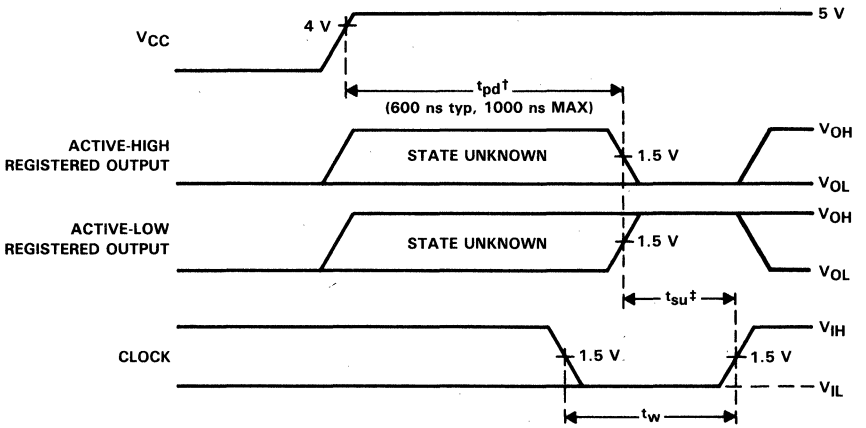


NOTE 2: $t_d = t_{su} = t_w$ = 100 ns to 1000 ns.
V_{IHH} = 10.25 V to 10.75 V.

power-up reset

Following power-up, all registers are reset to zero. The output level depends on the polarity selected during programming. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the V_{CC}'s rise be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.

power-up reset waveforms



†This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡This is the setup time for input or feedback.

programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Insruments at (214) 997-5762.

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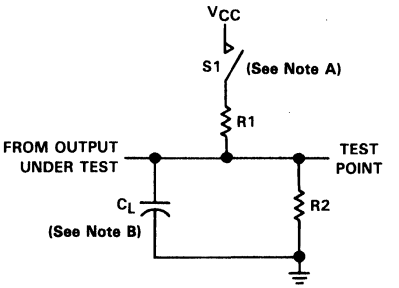
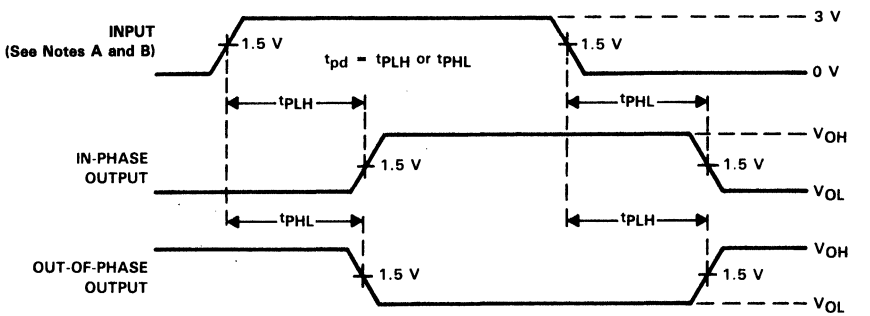
PARAMETER MEASUREMENT INFORMATION



NOTES: A. When measuring propagation times of 3-state outputs, S1 is closed.
B. C_L = includes probe and jig capacitance.

FIGURE 1. LOAD CIRCUIT FOR THREE-STATE OUTPUTS

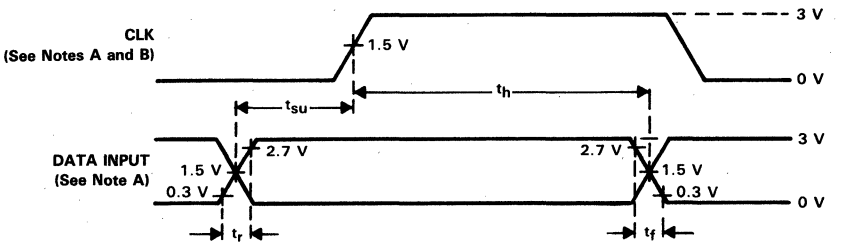


VOLTAGE WAVEFORMS

NOTES: A. When measuring propagation times of 3-state outputs. S1 is closed.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns.

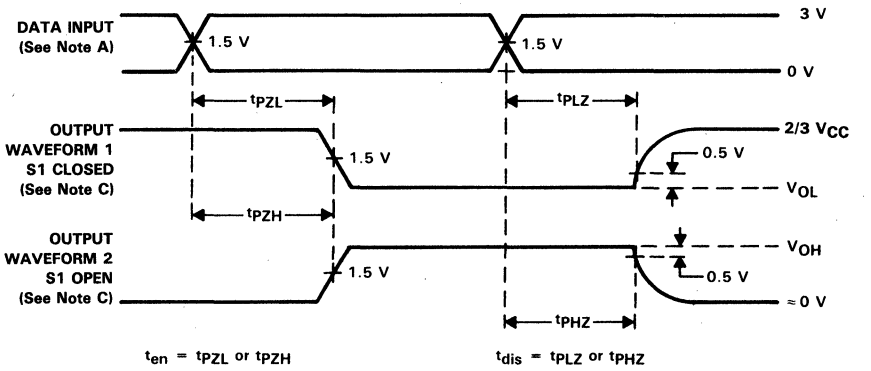
FIGURE 2. PROPAGATION DELAY TIMES, OUTPUT RISE AND FALL TIMES

PARAMETER MEASUREMENT INFORMATION



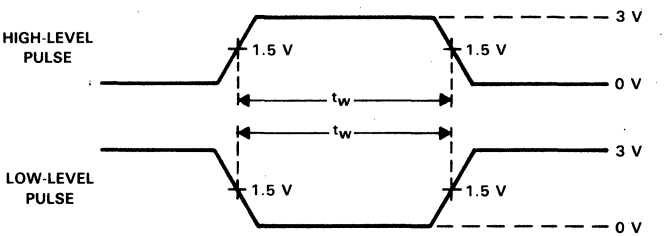
VOLTAGE WAVEFORMS

FIGURE 3. SETUP AND HOLD TIMES, AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS

FIGURE 4. ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS



VOLTAGE WAVEFORMS

FIGURE 5. PULSE DURATIONS

NOTES: A. All input pulses are supplied by generators having the followng characteristics: PRR ≤ 1 MHz, Z_o = 50 Ω, t_r = 3 ns.
B. For clock inputs, f_{max} is measured with input duty cycle = 50%.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

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special design features

True CMOS Outputs: Each '18V8 output is designed with a P-channel pull-up transistor and an N-channel pull-down transistor, a true CMOS output with rail-to-rail output switching. This provides direct interface to CMOS logic, memory, or ASIC devices without the need for a pull-up resistor. The CMOS output has 24-mA drive capability, which makes the '18V8 an ideal substitute for bipolar PALs. The electrical characteristics of this device show the output under both CMOS and TTL conditions.

Simultaneous Switching: High-performance CMOS devices often have output glitches on nonswitched outputs when a large number of outputs are switched simultaneously. This glitch is commonly referred to as "ground bounce" and is most noticeable on outputs held at V_{OL} (low-level output voltage). Ground bounce is caused by the voltage drop across the inductance in the package lead when current is switched ($dv \propto I \times di/dt$).

One solution is to restrict the number of outputs that can switch simultaneously. Another solution is to change the device pinout such that the ground is located on a low-inductance package pin. TI opted for a third option in order to maintain pinout compatibility and eliminate functional constraints. This option controls the output transistor turn-on characteristics and puts a limit on the instantaneous current available to the load, much like the I_{OS} resistor in a TTL circuit.

Wake-Up Features: The '18V8 employs input signal transition detection techniques to power-up the device from the standby-power mode. The transition detector monitors all inputs, I/Os, and feedback paths. Whenever a transition is sensed, the detector activates the power-up mode. The device will remain in the power-up mode until the detector senses that the inputs and outputs have been static for about 40 ns; thereafter, the device returns to the standby mode.

Electronic Signature Word: The '18V8 has a 72-bit word available for the user to store device information, such as ID codes, revision numbers, or inventory control. The signature cannot be programmed or altered once the device is secured.

Power Dissipation: Power dissipation of the '18V8 is defined by three contributing factors, and the total power dissipation is the sum of all three.

Standby Power: The product of V_{CC} and the standby I_{CC}. The standby current is the reverse current through the diodes that are reversed biased. This current is very small, and for circuits that remain in static condition for a long time, this low amount of current can become a major performance advantage.

Dynamic Power: The product of V_{CC} and the dynamic current. This current flows through the device only when the transistors are switching from one logic level to the other. The total dynamic current for the '18V8 is dependent upon the users' configuration of the PAL and the operating frequency. Output loading can be a source of additional power dissipation.

Interface Power: The product of ΔI_{CC} (operating) and V_{CC}. The total interface power is dependent on the number of inputs at the TTL V_{OH} level. The interface power can be eliminated by the addition of a pull-up resistor.

Even though power dissipation is a function of the user's device configuration and the operating frequency, the '18V8 is a lower-powered solution than either the quarter-powered or half-powered bipolar devices. The virtually zero standby power feature makes the '18V8 the device of choice for low duty cycle and battery-powered applications.

special design features (continued)

Programming and Eraseability: Programming of the '18V8 is achieved through floating-gate avalanche injection techniques. The charge trapped on the floating gate remains after power has been removed, allowing for the nonvolatility of the programmed data. The charge can be removed by exposure to light with wavelengths of less than 400 nm (4000 Å). The recommended erasure wavelength is 253.7 nm (2537 Å), with erasure time of 20 to 30 minutes, using a light source with a power rating of 12000 μW/cm placed within 2.5 cm (1 inch) from the device.

The '18V8 is designed for programming endurance of 1000 write/erase cycles with a data retention of ten years. A few precautions will guarantee maximum data retention. Continuous exposure to high-intensity UV light can cause permanent damage. The maximum exposure intensity is 7000 W•s/cm (The equivalent of leaving the unit in a UV eraser for a week). The window on the device should be covered by an opaque label, as the fluorescent light in a room can erase a unit in three years or, in the case of a direct sunlight, erasure can be complete in one week.

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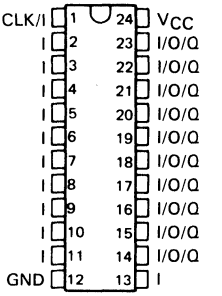
D3089, DECEMBER 1987

- 24-Pin Advanced CMOS PAL
- Virtually Zero Standby Power
- Propagation Delay Time . . . 20 ns Typ
- Variable Product Term Distribution Allows More Complex Functions to be Implemented
- Each Output is User-Programmable for Registered or Combinatorial Operation, Polarity, and Output Enable Control
- Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability
- Preload Capability on All Registered Outputs Allow for Improved Device Testing
- Power-Up Clear on Registered Outputs
- UV Light Erasable Cell Technology Allows for:
  - Reconfigurable Logic
  - Reprogrammable Cells
  - Full Factory Testing for Guaranteed 100% Yields
- Programmable Design Security Bit Prevents Copying of Logic Stored in Device
- Package Options Include Plastic and Ceramic Dual-In-Line Packages and Chip Carriers

JL PACKAGE
(TOP VIEW)



description

This PAL device features high-speed performance, increased and variable product terms, flexible outputs, and virtually zero standby power. It combines TI's EPIC ™ (Enhanced Processed Implanted CMOS) process with ultraviolet-light-erasable EPROM technology. Each output has an OLM (Output Logic Macrocell) configuration allowing for user definition of the output type. This PAL provides reliable, low-power substitutes for numerous high-performance TTL PALs with gate complexities between 300 and 800 gates.

The 'PAL22V10 has 12 dedicated inputs and ten user-definable outputs. Individual outputs can be programmed as registered or combinational and inverting or noninverting as shown in the Output Logic Macrocell (OLM) diagram. These ten outputs are enabled through the use of individual product terms.

The variable product-term distribution on this device removes rigid limitation to a maximum of eight product terms per output. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. The variable allocation of product terms allows for far more complex functions to be implemented in this device than in previously available devices.

With features such as the programmable OLMs and the variable product-term distribution, the TICPAL22V10-25 offers quick design and development of custom LSI functions. Since each of the ten output pins may be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs can be implemented with this device.

EPIC is a trademark of Texas Instruments Incorporated.

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description (continued)

Design complexity is enhanced by the addition of synchronous set and asynchronous reset product terms. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0 independently of the clock. The output logic level after set or reset will depend on the polarity selected during programming.

Output registers of this device can be preloaded to any desired state during testing, thus allowing for full logical verification during product testing.

The TICPAL22V10 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices, as exposure to ESD may result in a degradation of the device parametric performance.

The floating gate programmable cells allow these PALs to be fully programmed and tested before assembly to assure high field programming yield and functionality. They are then erased by ultraviolet light before packaging.

The TICPAL22V10-25 has a power-up clear function, which forces all registered outputs to a predetermined state after power is applied to the device. Registered outputs selected as active low will power up with their outputs high while registered outputs selected as active high power up with their outputs low.

The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The C-suffix devices are characterized for operation from 0°C to 75°C.

design security

The 'PAL22V10 contains a programmable design security bit. Programming this bit will disable the read verify and programming circuitry protecting the design from being copied. The security bit is usually programmed after the design is finalized and released to production. A secured device will verify as if every location in the device is programmed. Because programming is accomplished by storing an invisible charge instead of opening a metal link, the '22V10 cannot be copied by visual inspection. Once a secured device is fully erased, it can be reprogrammed to any desired configuration.

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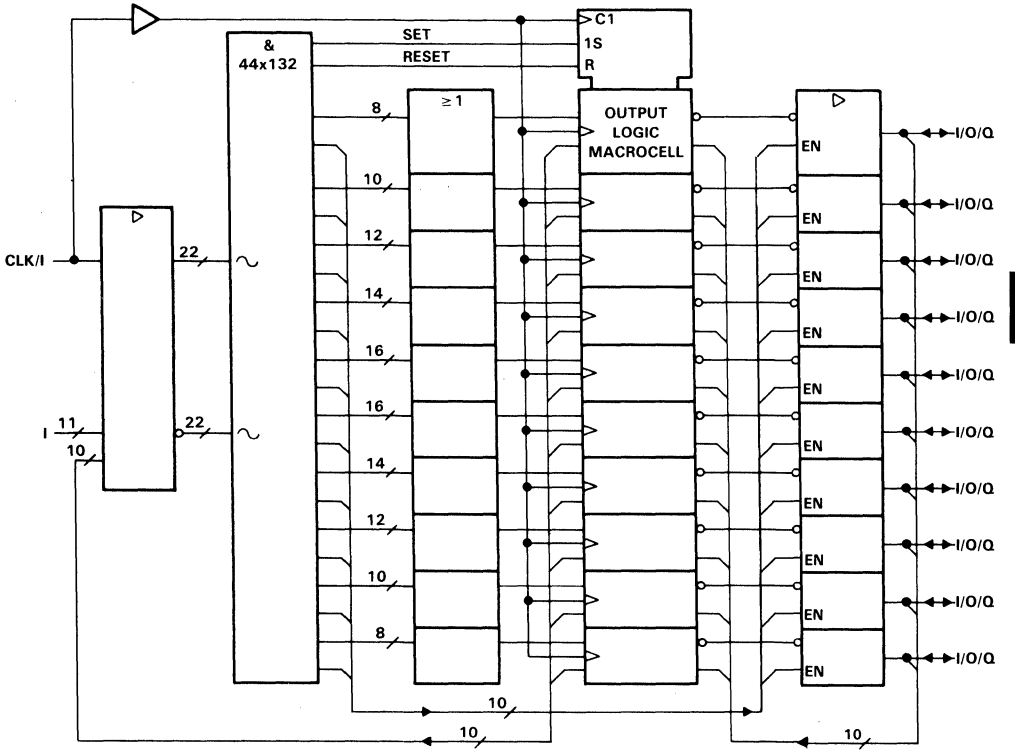
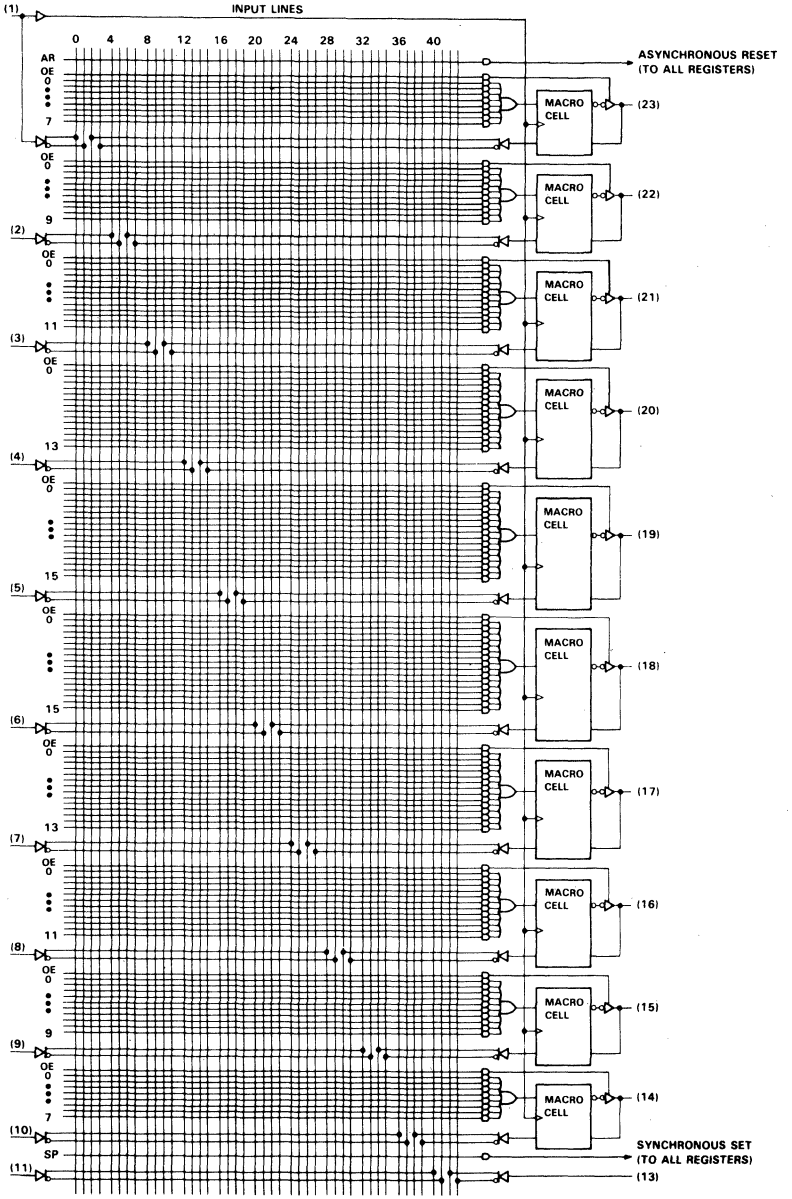
functional block diagram (positive logic)



∼ denotes fused inputs

logic diagram (positive logic)



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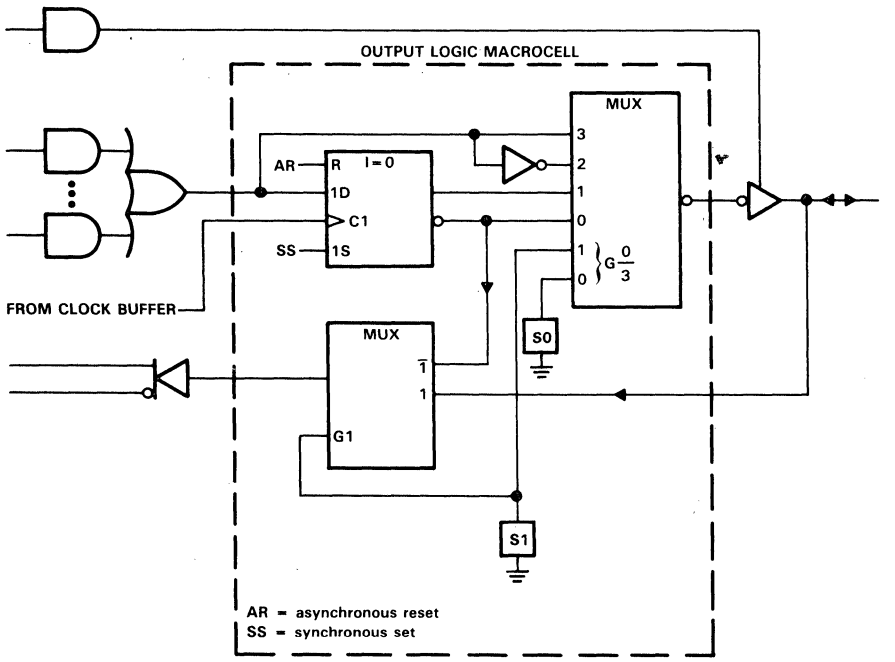
output logic macrocell (OLM) description

A great amount of architectural flexibility is provided by the user-configurable macrocell output options. The macrocell consists of a D-type flip-flop and two select multiplexers. The D-type flip-flop operates like a standard TTL D-type flip-flop. The input data is latched on the low-to-high transition of the clock input. The Q and $\overline{Q}$ outputs are made available to the output select multiplexer. The asynchronous reset and synchronous set controls are available in all flip-flops.

The select multiplexers are controlled by programmable bits. The combination of these programmable bits will determine which macrocell functions are implemented. It is this user control of the architectural structure that provides the generic flexibility of this device.

output logic macrocell diagram

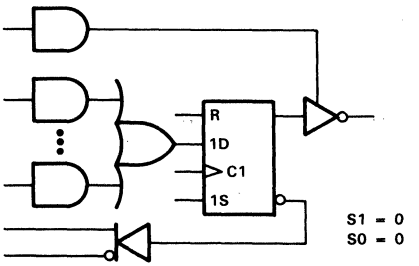


output logic macrocell options

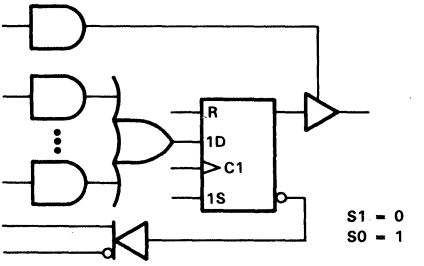
MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

CELL SELECT		FEEDBACK AND OUTPUT CONFIGURATION		
S1	S0			
0	0	Register feedback	Registered	Active low
0	1	Register feedback	Registered	Active high
1	0	I/O feedback	Combinational	Active low
1	1	I/O feedback	Combinational	Active high

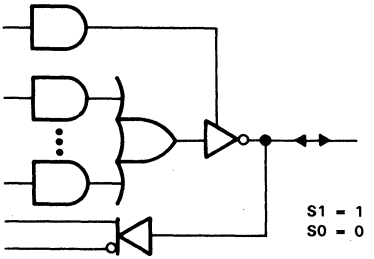
0 = erased cell 1 = programmed cell
S1 and S0 are select-function cells as shown in the output logic macrocell diagram.



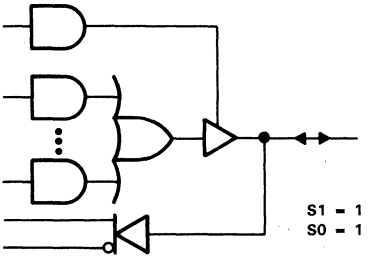
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 to V_{CC} + 0.5 V
Input diode current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output diode current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±40 mA
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: FN or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: FH or J package . . . . . 300°C
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

Note 1: This rating applies except during programming and preload cycles.

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			M SUFFIX			C SUFFIX			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		V_{CC}+0.5	2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Driving TTL			−2			−3.2	mA
		Driving CMOS			−2			−4	
I_{OL}	Low-level output current	Driving TTL			12			16	mA
		Driving CMOS			2			4	
f_{clock}	Clock frequency		0			0			MHz
t_w	Pulse duration	CLK high	10			8			ns
		CLK low	11			9			ns
		Asynchronous reset	30			25			ns
t_{su}	Setup time	Input or feedback	25			20			ns
		Reset inactive state	30			25			
t_h	Hold time	Input or feedback	0			0			ns
T_A	Operating free-air temperature		−55		125	0		75	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		M SUFFIX			C SUFFIX			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX for TTL	4			4			V
	V_{CC} = MIN,	I_{OH} = MAX for CMOS	3.86			3.86			V
V_{OL}	V_{CC} = MIN,	I_{OL} = MAX for TTL			0.5			0.5	V
	V_{CC} = MIN,	I_{OL} = MAX for CMOS			0.4			0.4	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.7 V						10	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V						−10	μA
I_{IH}	V_{CC} = MAX,	V_I = 5.25 V						10	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V						−10	μA
I_O§	V_{CC} = MAX,	V_O = 0.5 V	−30		−130	−30		−130	mA
I_{CC}	V_{CC} = MAX, Outputs open¶	V_I = 0 or V_{CC},			100			100	μA
$\frac{I_{CC}}{f}$	V_{CC} = MAX, f = 1 MHz	V_i = 0 to 3 V,		2			2		mA/MHz
ΔI_{CC}#	V_{CC} = MAX, One input at 0.5 V or 2.4 V, Other inputs at 0 V or V_{CC}	Pin 1			4			4	mA
		Others			2			2	
C_i	V_I = 2 V, f = 1 MHz, T_A = 25°C	Clock pin		12			12		pF
		All inputs		10			10		
		All I/O pins		15			15		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}‖	Without feedback		C suffix:		45			45		MHz
	With feedback		R1 = 200 Ω, R2 = 390 Ω,		30			30		
t_{pd}	I, I/O	O, I/O	C_L = 50 pF		20			20		ns
t_{pd}	CLK↑	Q	M suffix:		15			15		ns
t_{pd}	RESET	Q	R1 = 390 Ω, R2 = 750 Ω,		25			25		ns
t_{en}	I, I/O	I,Q, I/O	C_L = 50 pF		20			20		ns
t_{dis}	I, I/O	I,Q, I/O	C_L = 5 pF, See Figure 4		20			20		ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§This parameter approximates I_{OS}. The condition V_O = 0.5 V takes tester noise into account.

¶Disabled outputs are tied to GND or V_{CC}.

#This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than at 0 V or V_{CC}.

‖f_{max}(with feedback) = $\frac{1}{t_{su} + t_{pd}}$ (CLK to Q); f_{max}(without feedback) = $\frac{1}{t_{w(hi)} + t_{w(low)}}$

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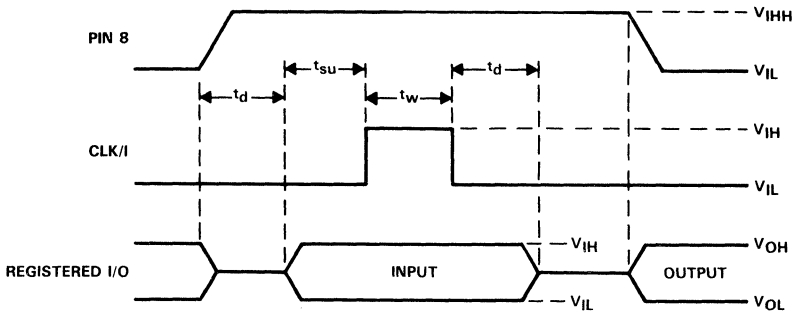
preload procedure for registered outputs

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below. The output level depends on the polarity selected during programming.

Step 1. With V_{CC} at 5 volts and pin 1 at V_{IL}, raise pin 8 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 8 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

preload waveforms (see Note 2)

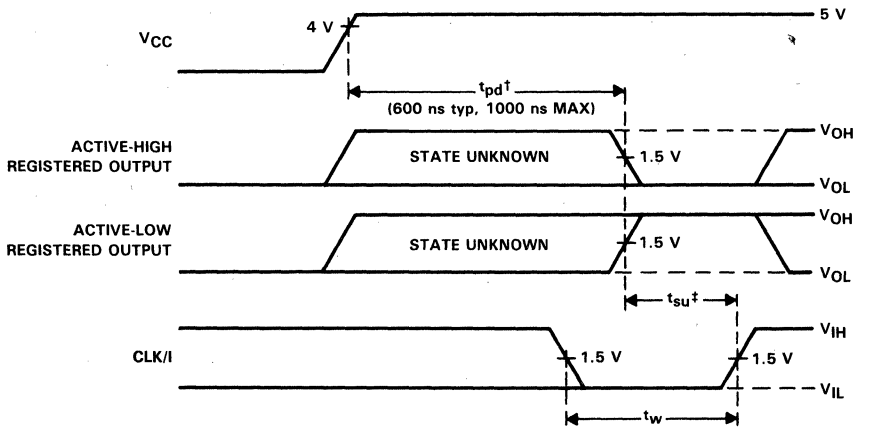


NOTE 2: $t_d = t_{su} = t_w$ = 100 ns to 1000 ns. V_{IHH} = 10.25 V to 10.75 V.

power-up reset

Following power-up, all registers are reset to zero. The output level depends on the polarity selected during programming. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the V_{CC}'s rise be monotonic. Following power-up, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.

power-up reset waveforms



†This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡This is the setup time for input or feedback.

programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specification, algorithms, and the lastest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5762.

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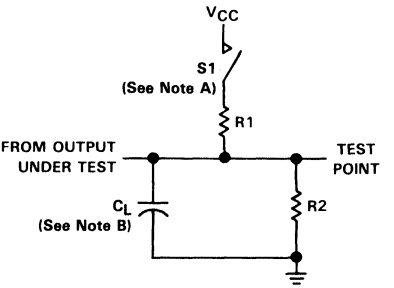
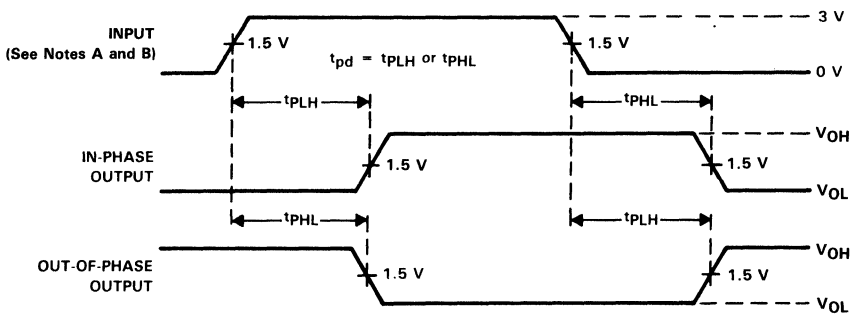
PARAMETER MEASUREMENT INFORMATION



NOTES: A. When measuring propagation times of 3-state outputs, S1 is closed.
B. C_L = includes probe and jig capacitance.

FIGURE 1. LOAD CIRCUIT FOR THREE-STATE OUTPUTS

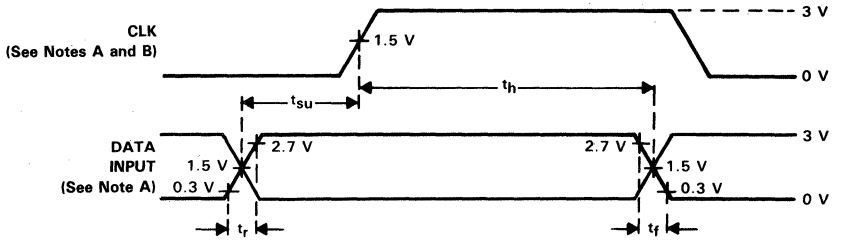


VOLTAGE WAVEFORMS

NOTES: A. When measuring propagation times of 3-state outputs, S1 is closed.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_o = 50 Ω, t_r = 3 ns.

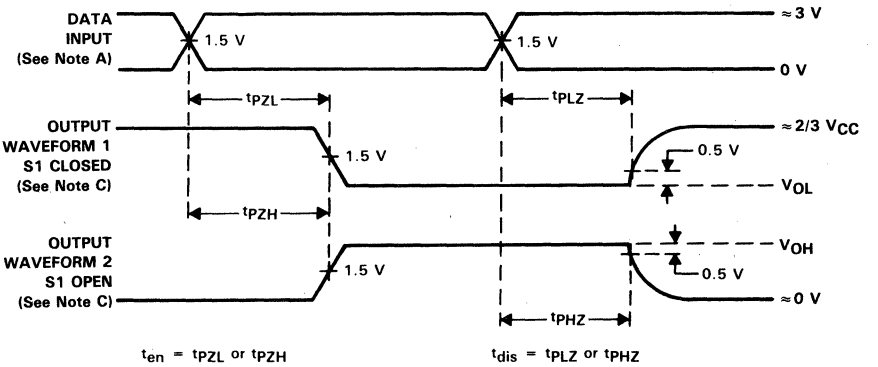
FIGURE 2. PROPAGATION DELAY TIMES, OUTPUT RISE AND FALL TIMES

PARAMETER MEASUREMENT INFORMATION



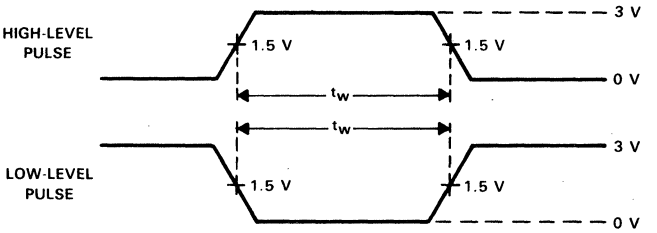
VOLTAGE WAVEFORMS

FIGURE 3. SETUP AND HOLD TIMES, AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS

FIGURE 4. ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS



VOLTAGE WAVEFORMS

FIGURE 5. PULSE DURATIONS

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_o = 50 Ω, t_r = 3 ns.
B. For clock inputs, f_{max} is measured with input duty cycle = 50%
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

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special design features

True CMOS Outputs: Each '22V10 output is designed with a P-channel pull-up transistor and an N-channel pull-down transistor, a true CMOS output with rail-to-rail output switching. This provides direct interface to CMOS logic, memory, or ASIC devices without the need for a pull-up resistor. The CMOS output has 16-mA drive capability, which makes the '22V10 an ideal substitute for bipolar PALs. The electrical characteristics of this device show the output under both CMOS and TTL conditions.

Simultaneous Switching: High-performance CMOS devices often have output glitches on nonswitched outputs when a large number of outputs are switched simultaneously. This glitch is commonly referred to as "ground bounce" and is most noticeable on outputs held at V_{OL} (low-level output voltage). Ground bounce is caused by the voltage drop across the inductance in the package lead when current is switched ($dv \propto I \times di/dt$).

One solution is to restrict the number of outputs that can switch simultaneously. Another solution is to change the device pinout such that the ground is located on a low-inductance package pin. TI opted for a third option in order to maintain pinout compatibility and eliminate functional constraints. This option controls the output transistor turn-on characteristics and puts a limit on the instantaneous current available to the load, much like the I_{OS} resistor in a TTL circuit.

Wake-Up Features: The '22V10 employs input signal transition detection techniques to power-up the device from the standby-power mode. The transition detector monitors all inputs, I/Os, and feedback paths. Whenever a transition is sensed, the detector activates the power-up mode. The device will remain in the power-up mode until the detector senses that the inputs and outputs have been static for about 40 ns; thereafter, the device returns to the standby mode.

Power Dissipation: Power dissipation of the '22V10 is defined by three contributing factors, and the total power dissipation is the sum of all three.

Standby Power: The product of V_{CC} and the standby I_{CC}. The standby current is the reverse current through the diodes that are reversed biased. This current is very small, and for circuits that remain in static condition for a long time, this low amount of current can become a major performance advantage.
Dynamic Power: The product of V_{CC} and the dynamic current. This dynamic current flows through the device only when the transistors are switching from one logic level to the other. The total dynamic current for the '22V10 is dependent upon the users' configuration of the PAL and the operating frequency. Output loading can be a source of additional power dissipation.
Interface Power: The product of I_{CC} (operating) and V_{CC}. The total interface power is dependent on the number of inputs at the TTL V_{OH} level. The interface power can be eliminated by the addition of a pull-up resistor.

Even though power dissipation is a function of the user's device configuration and the operating frequency, the '22V10 is a lower powered solution than either the quarter-powered or half-powered bipolar devices. The virtually zero standby power feature makes the '22V10 the device of choice for low-duty-cycle and battery-powered applications.

Programming and Eraseability

Programming of the '22V10 is achieved through floating-gate avalanche injection techniques. The charge trapped on the floating gate remains after power has been removed, allowing for the nonvolatility of the programmed data. The charge can be removed by exposure to light with wavelengths of less than 400 nm (4000 Å). The recommended erasure wavelength is 253.7 nm (2537 Å), with erasure time of 20 to 30 minutes, using a light source with a power rating of 12000 μW/cm placed within 2.5 cm (1 inch) of the device.

Programming and Eraseability (continued)

The '22V10 is designed for programming endurance of 1000 write/erase cycles with a data retention of ten years. A few precautions will guarantee maximum data retention. Continuous exposure to high-intensity UV light can cause permanent damage. The maximum exposure intensity is 7000 W•s/cm (The equivalent of leaving the unit in a UV eraser for a week). The window on the device should be covered by an opaque label, as the flourescent light in a room can erase a unit in three years or, in the case of a direct sunlight, erasure can be complete in one week.

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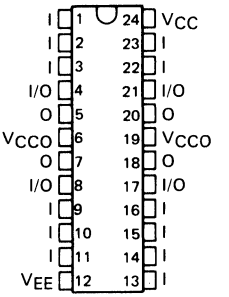
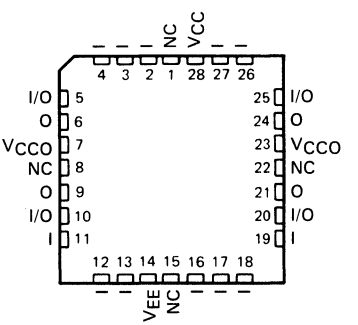
D3084, DECEMBER 1987

- **ECL 10KH PAL**
- **High-Performance Operation**
  Propagation Delay . . . 3 ns Max
- **Replacement for Conventional ECL Logic**
- **24-Pin, 300-Mil Package**
- **Reliable Titanium-Tungsten Fuses**

JT PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

This ECL PAL device combines the ExCL™ (Double Polysilicon Self-Aligned) process with the proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional ECL logic. Its easy programmability allows for quick design of "custom" functions and typically results in a more compact board. In addition, chip carriers are available for further reduction in board space.

The TIEPAL10H16P8-3 is provided with output polarity fuses. Each output remains active-high when the fuse is intact and is active-low when the fuse is blown.

The TIEPAL10H16P8-3 has 12 dedicated inputs, four standard outputs, and four I/O ports. It should be noted that with emitter-coupled outputs, a high level overrides a low level. Therefore, in order to use an I/O port as an input, the related output must be forced to a low level either through satisfying preprogrammed equations or permanently by programming.

The TIEPAL10H16P8-3 is equipped with a security fuse. Once the security fuse is blown, additional programming and verification cannot be performed. This prevents easy duplication of a design.

This device is characterized for operation from 0°C to 75°C; this temperature range is designated by a "C" suffix in the part number (TIEPAL10H16P8-3CJT).

PRODUCT PREVIEW

ExCL is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Monolithic Memories Inc.

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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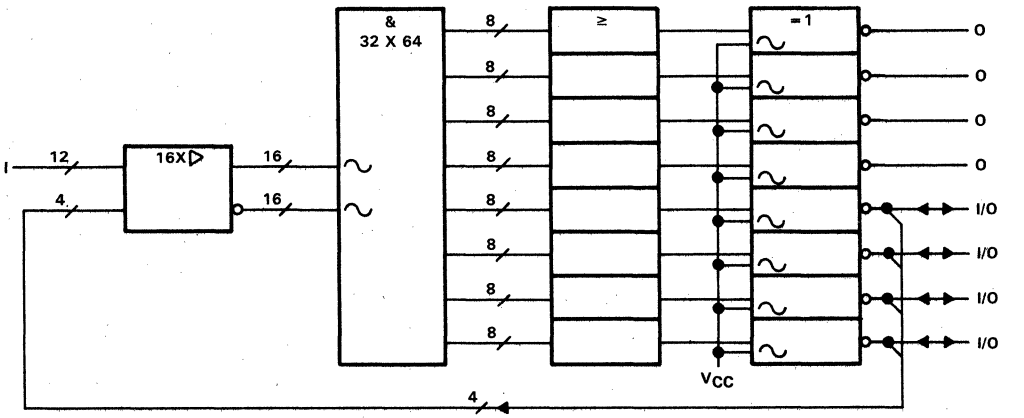
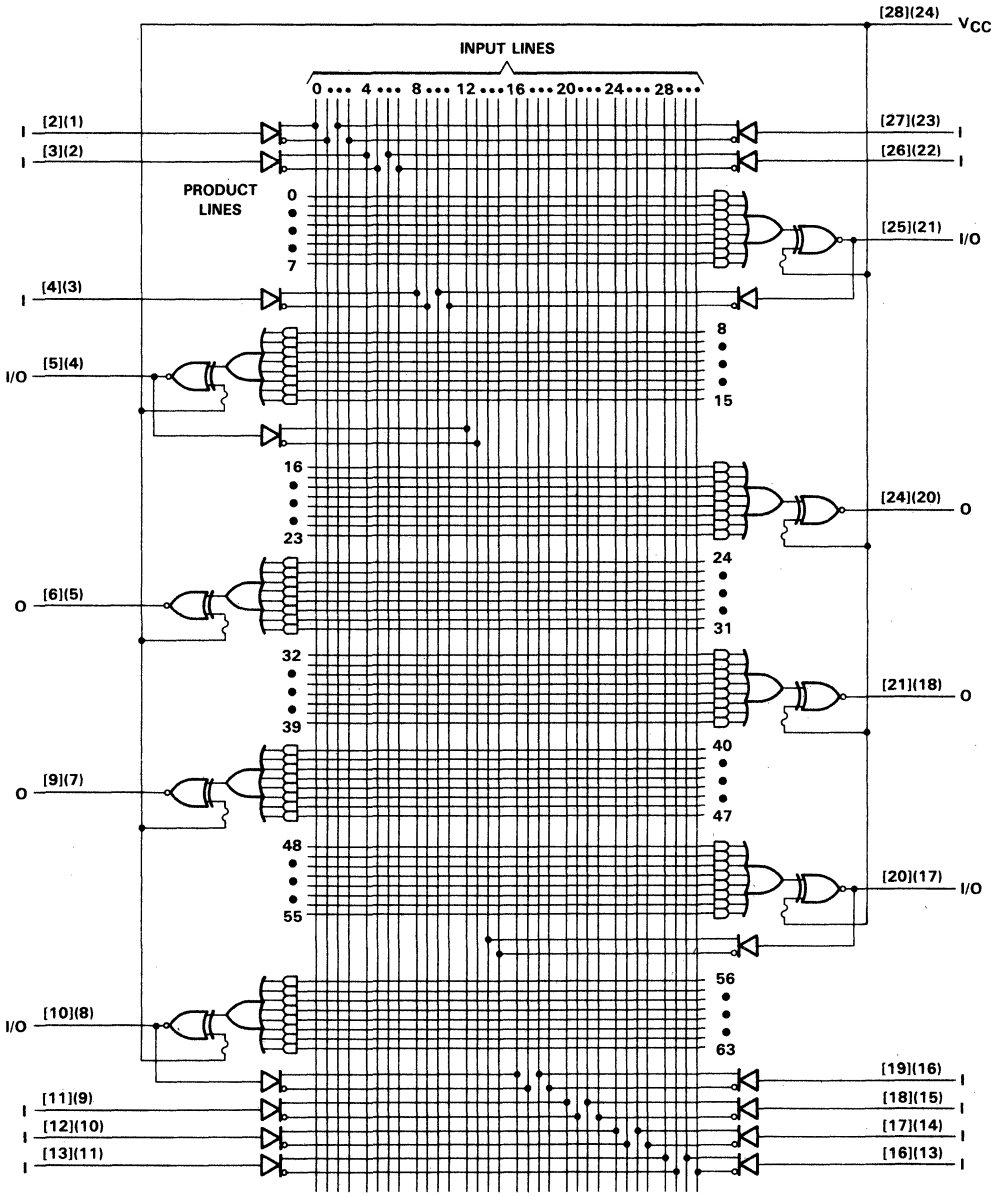
functional block diagram (positive logic)



logic diagram (positive logic)



NOTE: Pin numbers in [ ] are for the FK package; pin numbers in ( ) are for JT package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Note 1)

Supply voltage, V_{EE} (see Note 2) . . . . . 0 V to −6.5 V
Input voltage, V_I (see Note 3) . . . . . 0 V to V_{EE}
Output current . . . . . −50 mA
Operating free-air temperature range: C suffix . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. These ratings apply except for programming pins during a programming cycle.
2. All voltage values are with respect to V_{CC} and V_{CCO}, i.e., these pins are all assumed to be at 0 volts.
3. V_I should never be more negative than V_{EE}.

recommended operating conditions (see Note 4)

			C-SUFFIX			UNIT
			MIN	NOM	MAX	
V_{EE}	Supply voltage		−4.94	−5.2	−5.46	V
V_{IH}	High-level input voltage	T_A = 0°C	−1.17		−0.84	V
		T_A = 25°C	−1.13		−0.81	
		T_A = 75°C	−1.07		−0.735	
V_{IL}	Low-level input voltage	T_A = 0°C	−1.95		−1.48	V
		T_A = 25°C	−1.95		−1.48	
		T_A = 75°C	−1.95		−1.45	
T_A	Operating free-air temperature		0		75	°C

NOTE 4: The algebraic convention, in which the more negative limit is designated as minimum and the less negative limit is designated as maximum, is used in this data sheet for logic voltage levels only. For other quantities, e.g., supply voltages and currents, the normal magnitude convention is used.

electrical characteristics over recommended supply voltage range at specified free-air temperature (see Notes 4 and 5)

PARAMETER	TEST CONDITIONS		C-SUFFIX			UNIT
			MIN	TYP	MAX	
V_{OH}	V_I = V_{IH}min or V_{IL}max	0°C	−1.02		−0.84	V
		25°C	−0.98	−0.895	−0.81	
		75°C	−0.92		−0.735	
V_{OL}	V_I = V_{IH}min or V_{IL}max	0°C	−1.95		−1.63	V
		25°C	−1.95		−1.63	
		75°C	−1.95	−1.79	−1.60	
I_{IH}	V_I = V_{IH}max	0°C			220	μA
		25°C			220	
		75°C			220	
I_{IL}	V_I = V_{IL}min	0°C	0.5			μA
		25°C	0.5			
		75°C	0.3			
I_{EE}	All inputs open	0°C to 75°C			−220	mA

NOTES: 4. The algebraic convention, in which the more negative limit is designated as minimum and the less negative limit is designated as maximum, is used in this data sheet for logic voltage levels only. For other quantities, e.g., supply voltages and currents, the normal magnitude convention is used.
5. Each 10KH PAL has been designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 150 meters (500 feet) per minute is maintained. Outputs are terminated through a 50-ohm resistor to −2 V.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

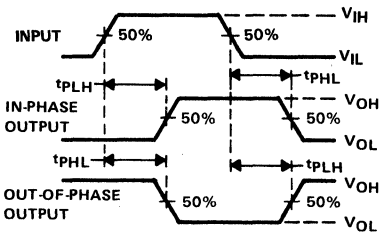
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	C-SUFFIX			UNIT
				MIN	TYP	MAX	
t_{pd}	I, I/O, or feedback	O, I/O	See Figures 1 and 2	1		3	ns
t_r				0.7		1.5	ns
t_f				0.7		1.5	ns

NOTE 5: Each 10KH PAL has been designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 150 meters (500 feet) per minute is maintained. Outputs are terminated through a 50-ohm resistor to −2 V.

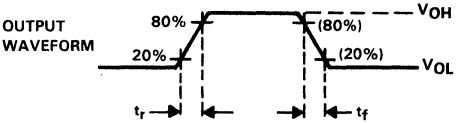
PROGRAMMING INFORMATION

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5762.

PARAMETER MEASUREMENT INFORMATION



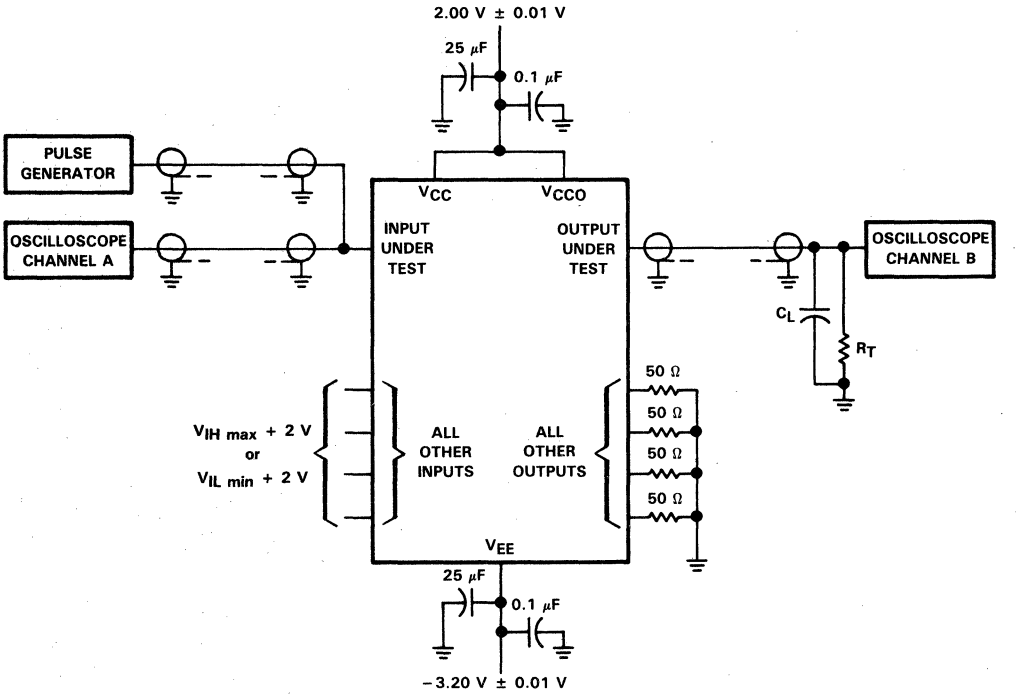
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
RISE TIME AND FALL TIME

FIGURE 1. VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The offset voltage generator has the following characteristics: Pulse amplitude = 800 mV P-P, PRR ≤ 1 MHz, t_w = 500 ns, $t_r = t_f$ = 1 ns.
B. R_T is a 50-Ω terminator internal to the oscilloscope.
C. C_L ≤ 3 pF, includes fixture and stray capacitance.
D. Coax has 50-Ω impedance and the coax to oscilloscope channel A and to channel B must be of equal lengths.
E. All unused outputs are loaded with 50-Ω ± 1% resistors to ground.
F. All unused inputs should be connected to either high or low levels consistent with the logic function required.
G. All fixture wire lengths or unterminated stubs should not exceed 6 mm (1/4 inch).

FIGURE 2. LOAD CIRCUIT

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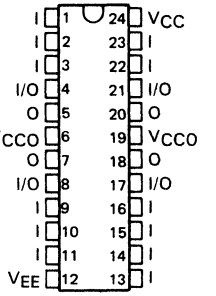
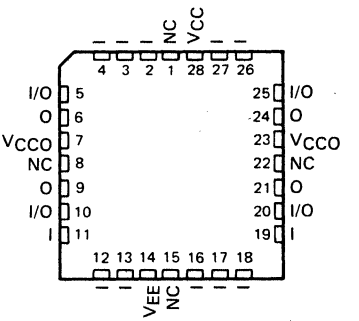
D2916, MAY 1987—REVISED DECEMBER 1987

- **ECL 10KH PAL**
- **High-Performance Operation**
  Propagation Delay . . . 6 ns Max
- **Replacement for Conventional ECL Logic**
- **24-Pin, 300-Mil Package**
- **Reliable Titanium-Tungsten Fuses**

TIEPAL10H16P8-6 . . . JT PACKAGE
(TOP VIEW)



TIEPAL10H16P8-6 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

This IMPACT™ ECL PAL device uses proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional ECL logic. Its easy programmability allows for quick design of "custom" functions and typically results in a more compact board. In addition, chip carriers are available for further reduction in board space.

The TIEPAL10H16P8-6 is provided with output polarity fuses. Each output remains active-high when the fuse is intact and is active-low when the fuse is blown.

The TIEPAL10H16P8-6 has 12 dedicated inputs, four standard outputs, and four I/O ports. It should be noted that with emitter-coupled outputs, a high level overrides a low level. Therefore, in order to use an I/O port as an input, the related output must be forced to a low level either through satisfying preprogrammed equations or permanently by programming.

The TIEPAL10H16P8-6 is equipped with a security fuse. Once the security fuse is blown, additional programming and verification cannot be performed. This prevents easy duplication of a design.

This device is characterized for operation from 0°C to 75°C; this temperature range is designated by a "C" suffix in the part number (TIEPAL10H16P8-6CJT).

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PAL is a registered trademark of Monolithic Memories Inc.

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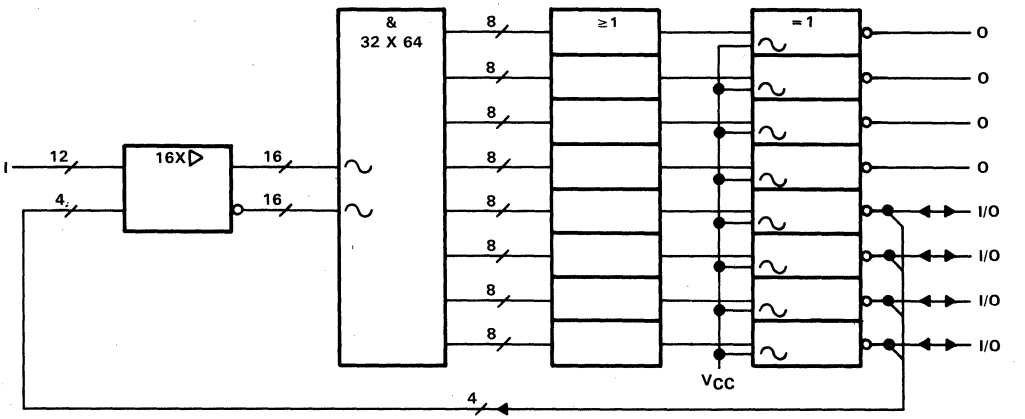
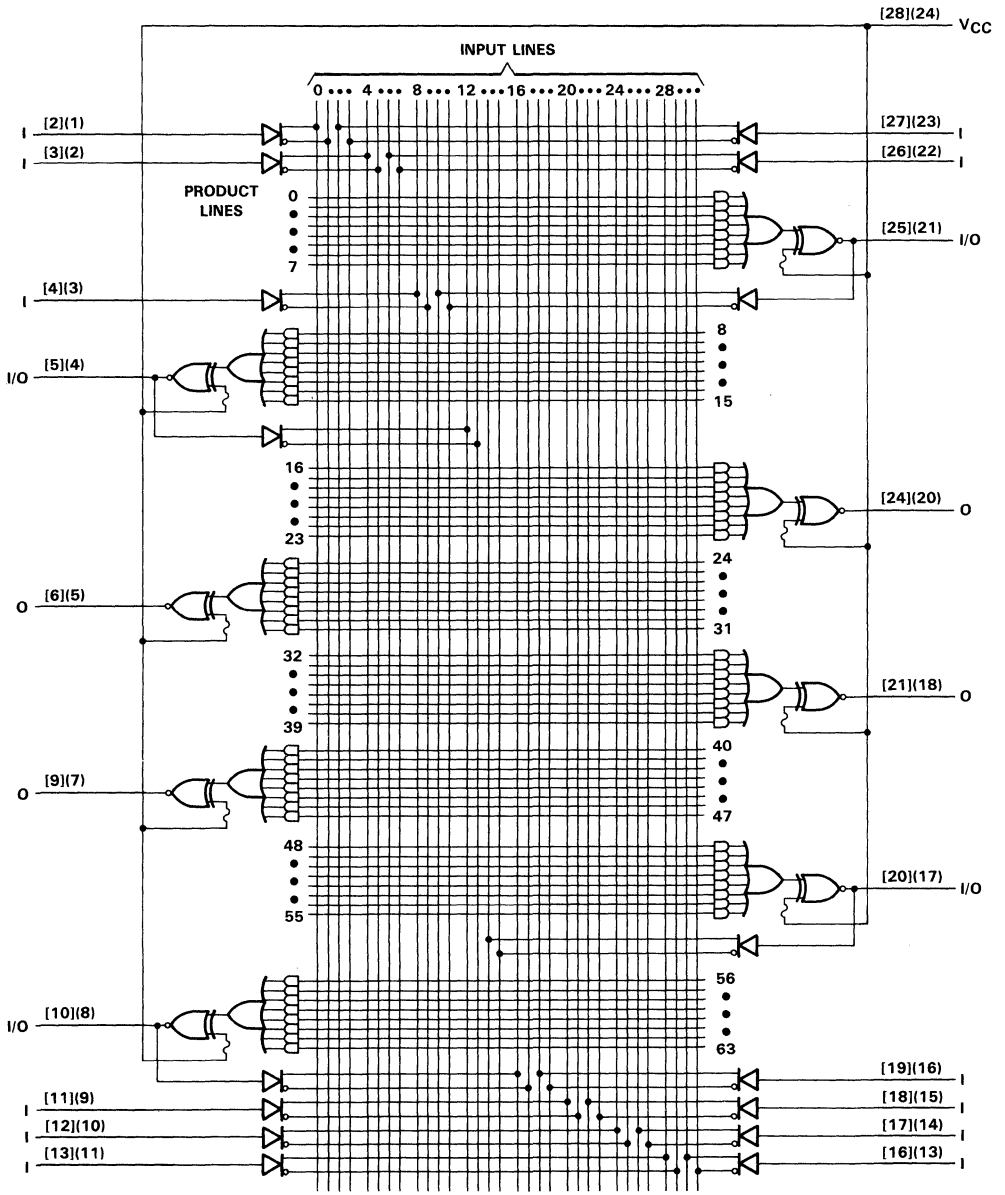
functional block diagram (positive logic)



logic diagram (positive logic)



NOTE: Pin numbers in [ ] are for the FK package; pin numbers in ( ) are for JT package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Note 1)

Supply voltage, V_{EE} (see Note 2) . . . . . 0 V to −6.5 V
Input voltage, V_I (see Notes 2 and 3) . . . . . 0 V to V_{EE}
Output current . . . . . −50 mA
Operating free-air temperature range: C suffix . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. These ratings apply except for programming pins during a programming cycle.
2. All voltage values are with respect to V_{CC} and V_{CCO}, i.e., these pins are all assumed to be at 0 volts.
3. V_I should never be more negative than V_{EE}.

recommended operating conditions (see Note 4)

			C-SUFFIX			UNIT
			MIN	NOM	MAX	
V_{EE}	Supply voltage		−4.94	−5.2	−5.46	V
V_{IH}	High-level input voltage	T_A = 0°C	−1.170		−0.840	V
		T_A = 25°C	−1.130		−0.810	
		T_A = 75°C	−1.070		−0.735	
V_{IL}	Low-level input voltage	T_A = 0°C	−1.950		−1.480	V
		T_A = 25°C	−1.950		−1.480	
		T_A = 75°C	−1.950		−1.450	
T_A	Operating free-air temperature		0		75	°C

NOTE 4: The algebraic convention, in which the more negative limit is designated as minimum and the less negative limit is designated as maximum, is used in this data sheet for logic voltage levels only. For other quantities, e.g., supply voltages and currents, the normal magnitude convention is used.

electrical characteristics over recommended supply voltage range at specified free-air temperature, V_{CC} = V_{CCO} = 0 (see Notes 4 and 5)

PARAMETER	TEST CONDITIONS	T_A	C-SUFFIX			UNIT
			MIN	TYP	MAX	
V_{OH}	V_I = V_{IH}min or V_{IL}max	0°C	−1.020		−0.840	V
		25°C	−0.980		−0.810	
		75°C	−0.920		−0.735	
V_{OL}	V_I = V_{IH}min or V_{IL}max	0°C	−1.950		−1.630	V
		25°C	−1.950		−1.630	
		75°C	−1.950		−1.600	
I_{IH}	V_I = V_{IH}max	0°C			220	μA
		25°C			220	
		75°C			220	
I_{IL}	V_I = V_{IL}min	0°C	0.5			μA
		25°C	0.5			
		75°C	0.3			
I_{EE}	All inputs open	0°C to 75°C			−240	mA

NOTES: 4. The algebraic convention, in which the more negative limit is designated as minimum and the less negative limit is designated as maximum, is used in this data sheet for logic voltage levels only. For other quantities, e.g., supply voltages and currents, the normal magnitude convention is used.
5. Each 10KH PAL® has been designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 150 meters (500 feet) per minute is maintained. Outputs are terminated through a 50-ohm resistor to −2 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Notes 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	C-SUFFIX			UNIT
				MIN	TYP	MAX	
t_{pd}	I, I/O, or feedback	Q	See Figures 1 and 2	2	4	6	ns
t_r				0.7	1	2.2	ns
t_f				0.7	1	2.2	ns

NOTES: 4. The algebraic convention, in which the more negative limit is designated as minimum and the less negative limit is designated as maximum, is used in this data sheet for logic voltage levels only. For other quantities, e.g., supply voltages and currents, the normal magnitude convention is used.

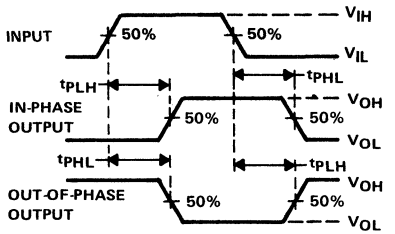
5. Each 10KH PAL® has been designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 150 meters (500 feet) per minute is maintained. Outputs are terminated through a 50-ohm resistor to −2 V.

programming information

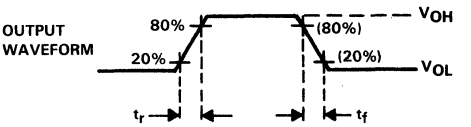
Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5762.

PARAMETER MEASUREMENT INFORMATION



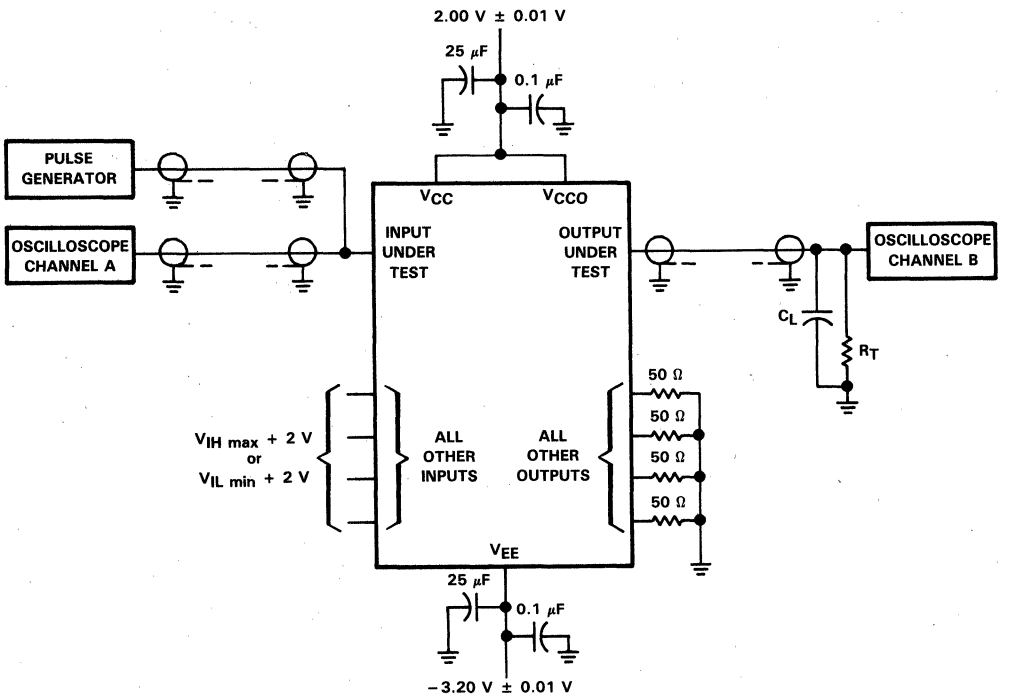
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
RISE TIME AND FALL TIME

FIGURE 1. VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



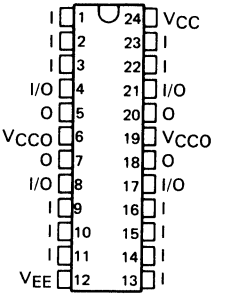
NOTES: A. The offset voltage generator has the following characteristics: Pulse amplitude = 800 mV P-P, PRR ≤ 1 MHz, t_w = 500 ns, $t_r = t_f$ = 1 ns.
B. R_T is a 50-Ω terminator internal to the oscilloscope.
C. $C_L \leq 3$ pF, includes fixture and stray capacitance.
D. Coax has 50-Ω impedance and the coax to oscilloscope channel A and to channel B must be of equal lengths.
E. All unused outputs are loaded with 50-Ω ±1% resistors to ground.
F. All unused inputs should be connected to either high or low levels consistent with the logic function required.
G. All fixture wire lengths or unterminated stubs should not exceed 6 mm (1/4 inch).

FIGURE 2. LOAD CIRCUIT

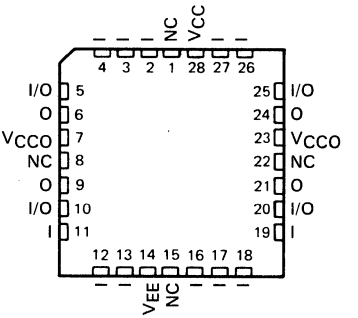
D3083, DECEMBER 1987

- **ECL 100K PAL**
- **High-Performance Operation**
  Propagation Delay . . . 3 ns Max
- **I_{EE} . . . −220 mA Max**
- **Replacement for 100K ECL Logic**
- **24-Pin, 300-Mil Package**
- **Reliable Titanium-Tungsten Fuses**

JT PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

This ECL PAL device combines the ExCL™ (Double Polysilicon Self-Aligned) process with the proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional ECL logic. Its easy programmability allows for quick design of "custom" functions with increased logic density. In addition, chip carriers are available for further reduction in board space.

The TIEPAL10016P8-3 is provided with output polarity fuses. Each output remains active-high when the fuse is intact and is active-low when the fuse is blown.

The TIEPAL10016P8-3 has 12 dedicated inputs, four standard outputs, and four I/O ports. It should be noted that with emitter-coupled outputs, a high level overrides a low level. Therefore, in order to use an I/O port as an input, the related output must be forced to a low level either through satisfying preprogrammed equations or permanently by programming.

The TIEPAL10016P8-3 is equipped with a security fuse. Once the security fuse is blown, additional programming and verification cannot be performed. This prevents easy duplication of a design.

This device is characterized for operation from 0°C to 85°C; this temperature range is designated by a "C" suffix in the part number (TIEPAL10016P8-3CJT).

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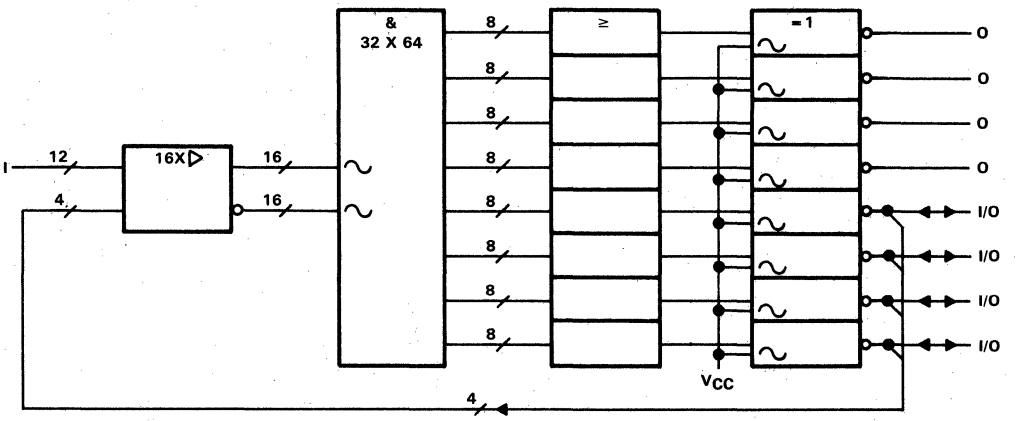
functional block diagram (positive logic)



PRODUCT PREVIEW

TEXAS INSTRUMENTS
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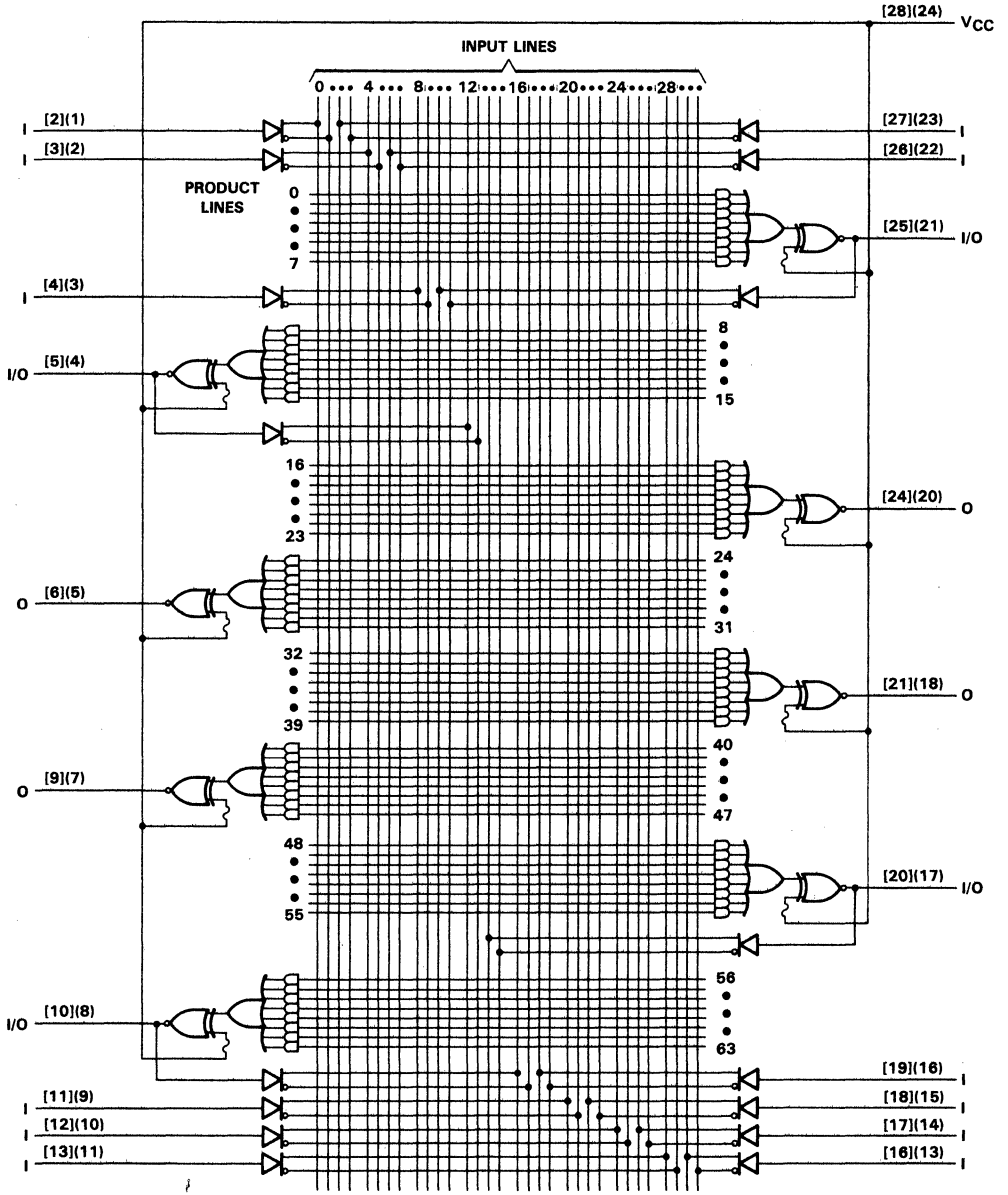
logic diagram (positive logic)



NOTE: Pin numbers in [ ] are for the FK package; pin numbers in ( ) are for JT package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Note 1)

Supply voltage, V_{EE} (see Note 2) . . . . . 0 V to −6.5 V
Input voltage, V_I (see Note 3) . . . . . 0 V to V_{EE}
Output current . . . . . −50 mA
Operating free-air temperature range . . . . . 0°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. These ratings apply except for programming pins during a programming cycle.
2. All voltage values are with respect to V_{CC} and V_{CCO}, i.e., these pins are all assumed to be at 0 volts.
3. V_I should never be more negative than V_{EE}.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{EE}	Supply voltage		−4.2	−4.5	−4.8	V
V_{IH}	High-level input voltage	V_{EE} = −4.2 V	−1.15		−0.88	V
		V_{EE} = −4.5 V	−1.165		−0.88	
		V_{EE} = −4.8 V	−1.165		−0.88	
V_{IL}	Low-level input voltage	V_{EE} = −4.2 V	−1.81		−1.475	V
		V_{EE} = −4.5 V	−1.81		−1.475	
		V_{EE} = −4.8 V	−1.81		−1.49	
T_A	Operating free-air temperature		0		85	°C

electrical characteristics over recommended supply voltage range, T_A = 0°C to 85°C (unless otherwise noted) (see Notes 4 and 5)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	V_I = V_{IH}min or V_{IL}max	V_{EE} = −4.2 V	−1.03		−0.87	V
		V_{EE} = −4.5 V	−1.035	−0.955	−0.88	
		V_{EE} = −4.8 V	−1.045		−0.88	
V_{OL}	V_I = V_{IH}min or V_{IL}max	V_{EE} = −4.2 V	−1.81		−1.595	V
		V_{EE} = −4.5 V	−1.81	−1.700	−1.61	
		V_{EE} = −4.8 V	−1.81		−1.61	
I_{IH}	V_I = V_{IH}max				220	μA
I_{IL}	V_I = V_{IL}min		0.5			μA
I_{EE}	All inputs open				−220	mA

†Typical values are at V_{CC} = 4.5 V, T_A = 25°C.

NOTES: 4. The algebraic convention, in which the more negative limit is designated as minimum and the less negative limit is designated as maximum, is used in this data sheet for logic voltage levels only. For other quantities, e.g., supply voltages and currents, the normal magnitude convention is used.
5. Each 100KH PAL has been designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 150 meters (500 feet) per minute is maintained. Outputs are terminated through a 50-ohm resistor to −2 V.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

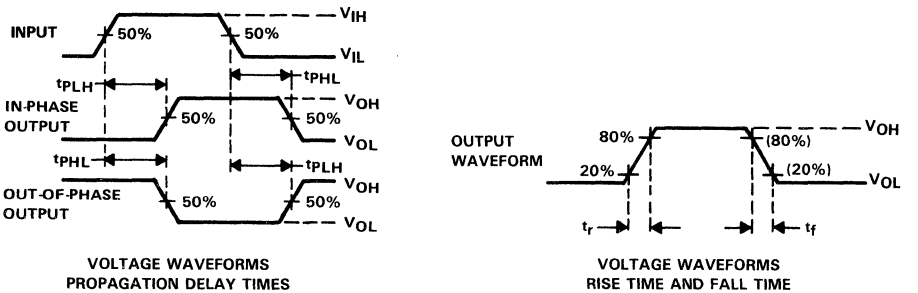
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd}	I, I/O, or feedback	O, I/O	See Figures 1 and 2	1	3	ns
t_r				0.7	1.5	ns
t_f				0.7	1.5	ns

NOTE 5: Each 100KH PAL has been designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 150 meters (500 feet) per minute is maintained. Outputs are terminated through a 50-ohm resistor to −2 V.

PROGRAMMING INFORMATION

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5762.

PARAMETER MEASUREMENT INFORMATION

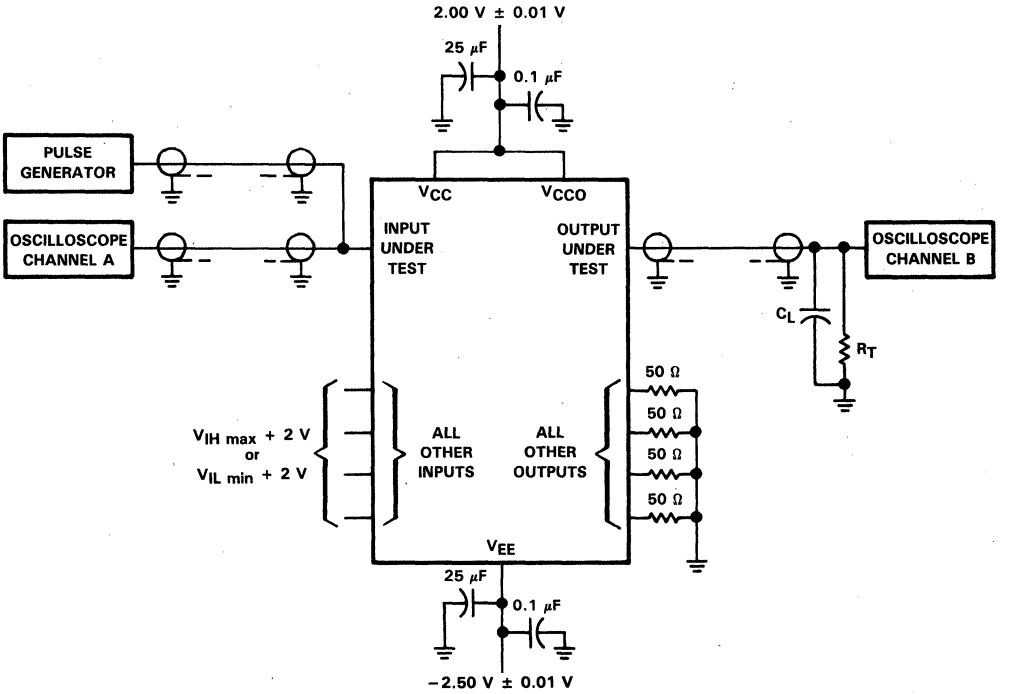


VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS RISE TIME AND FALL TIME

FIGURE 1. VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The offset voltage generator has the following characteristics: Pulse amplitude = 800 mV P-P, PRR ≤ 1 MHz, t_w = 500 ns, $t_r = t_f$ = 1 ns.
B. R_T is a 50-Ω terminator internal to the oscilloscope.
C. C_L ≤ 3 pF, includes fixture and stray capacitance.
D. Coax has 50-Ω impedance and the coax to oscilloscope channel A and to channel B must be of equal lengths.
E. All unused outputs are loaded with 50-Ω ± 1% resistors to ground.
F. All unused inputs should be connected to either high or low levels consistent with the logic function required.
G. All fixture wire lengths or unterminated stubs should not exceed 6 mm (1/4 inch).

FIGURE 2. LOAD CIRCUIT

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D3082, DECEMBER 1987

- **ECL 100K PAL**
- **High-Performance Operation**
  Propagation Delay . . . 6 ns Max
- **I_{EE} . . . −240 mA Max**
- **Replacement for 100K ECL Logic**
- **24-Pin, 300-Mil Package**
- **Reliable Titanium-Tungsten Fuses**

description

This IMPACT™ ECL PAL device uses proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional ECL logic. Its easy programmability allows for quick design of "custom" functions and typically results in a more compact board. Additionally, chip carriers are available for further reduction in board space.

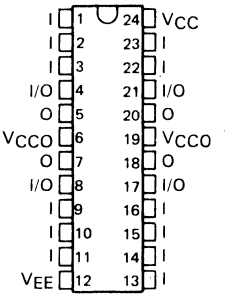
The TIEPAL10016P8-6 is provided with output polarity fuses. Each output remains active-high when the fuse is intact and is active-low when the fuse is blown.

The TIEPAL10016P8-6 has 12 dedicated inputs, four standard outputs, and four I/O ports. It should be noted that with emitter-coupled outputs, a high level overrides a low level. Therefore, to use an I/O port as an input, the related output must be forced to a low level either by satisfying preprogrammed equations or by permanent programming.

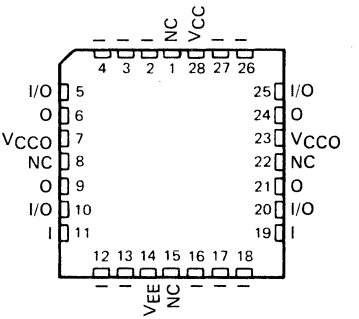
The TIEPAL10016P8-6 is equipped with a security fuse. Once the security fuse is blown, additional programming and verification cannot be performed. This prevents easy duplication of a design.

This device is characterized for operation from 0°C to 85°C.

JT PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC—No internal connection

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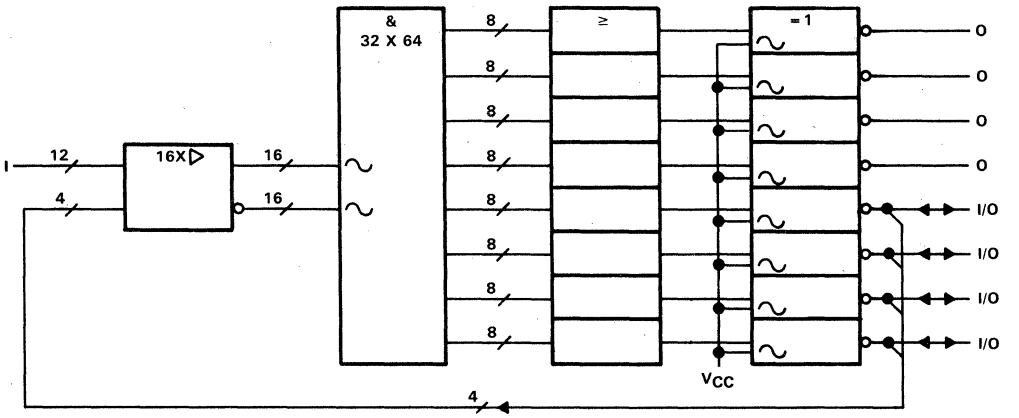
functional block diagram (positive logic)



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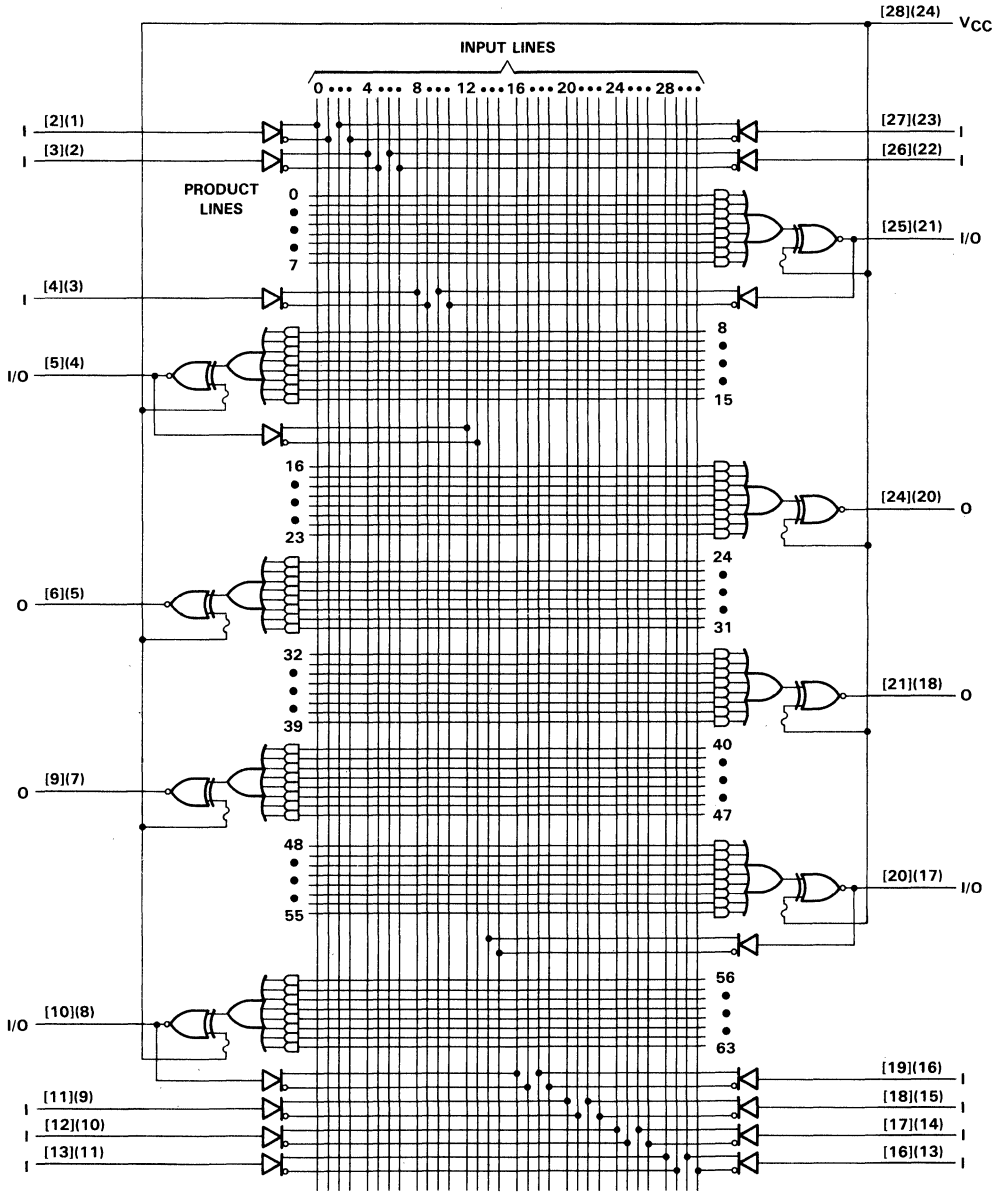
logic diagram (positive logic)



NOTE: Pin numbers in ( ) are for the FK package; pin numbers in ( ) are for JT package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Note 1)

Supply voltage, V_{EE} (see Note 2) . . . . . 0 V to −6.5 V
Input voltage, V_I (see Note 3) . . . . . 0 V to V_{EE}
Output current . . . . . −50 mA
Operating free-air temperature range . . . . . 0°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. These ratings apply except for programming pins during a programming cycle.
2. All voltage values are with respect to V_{CC} and V_{CCO}, i.e., these pins are all assumed to be at 0 volts.
3. V_I should never be more negative than V_{EE}.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{EE}	Supply voltage		−4.2	−4.5	−4.8	V
V_{IH}	High-level input voltage	V_{EE} = −4.2 V	−1.15		−0.88	V
		V_{EE} = −4.5 V	−1.165		−0.88	
		V_{EE} = −4.8 V	−1.165		−0.88	
V_{IL}	Low-level input voltage	V_{EE} = −4.2 V	−1.81		−1.475	V
		V_{EE} = −4.5 V	−1.81		−1.475	
		V_{EE} = −4.8 V	−1.81		−1.49	
T_A	Operating free-air temperature		0		85	°C

electrical characteristics over recommended supply voltage range at 0°C to 85°C (see Notes 4 and 5)

PARAMETER	TEST CONDITIONS	V_{EE}	MIN	TYP	MAX	UNIT
V_{OH}	V_I = V_{IH}min or V_{IL}max	−4.2 V	−1.03		−0.87	V
		−4.5 V	−1.035	−0.955	−0.88	
		−4.8 V	−1.045		−0.88	
V_{OL}	V_I = V_{IH}min or V_{IL}max	−4.2 V	−1.81		−1.595	V
		−4.5 V	−1.81	−1.700	−1.61	
		−4.8 V	−1.81		−1.61	
I_{IH}	V_I = V_{IH}max				220	μA
I_{IL}	V_I = V_{IL}min		0.5			μA
I_{EE}	All inputs open				−240	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	I, I/O, or feedback	O, I/O	See Figures 1 and 2	2	4	6	ns
t_r				0.7	1	1.5	ns
t_f				0.7	1	1.5	ns

NOTES: 4. The algebraic convention, in which the more negative limit is designated as minimum and the less negative limit is designated as maximum, is used in this data sheet for logic voltage levels only. For other quantities, e.g., supply voltages and currents, the normal magnitude convention is used.
5. Each 100KH PAL has been designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 150 meters (500 feet) per minute is maintained. Outputs are terminated through a 50-ohm resistor to −2 V.

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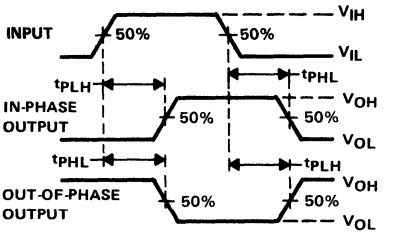
PROGRAMMING INFORMATION

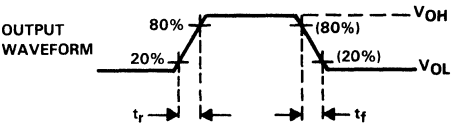
Texas Instruments Programmable Logic Devices can be programmed using widely available software and reasonably priced device programmers.

Complete programming specifications, algorithms and the latest information on firmware, software, and hardware updates are available upon request. Information on programmers that are capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI sales office, local authorized Texas Instruments distributor, or by calling Texas Instruments at (214) 997-5762.

PARAMETER MEASUREMENT INFORMATION



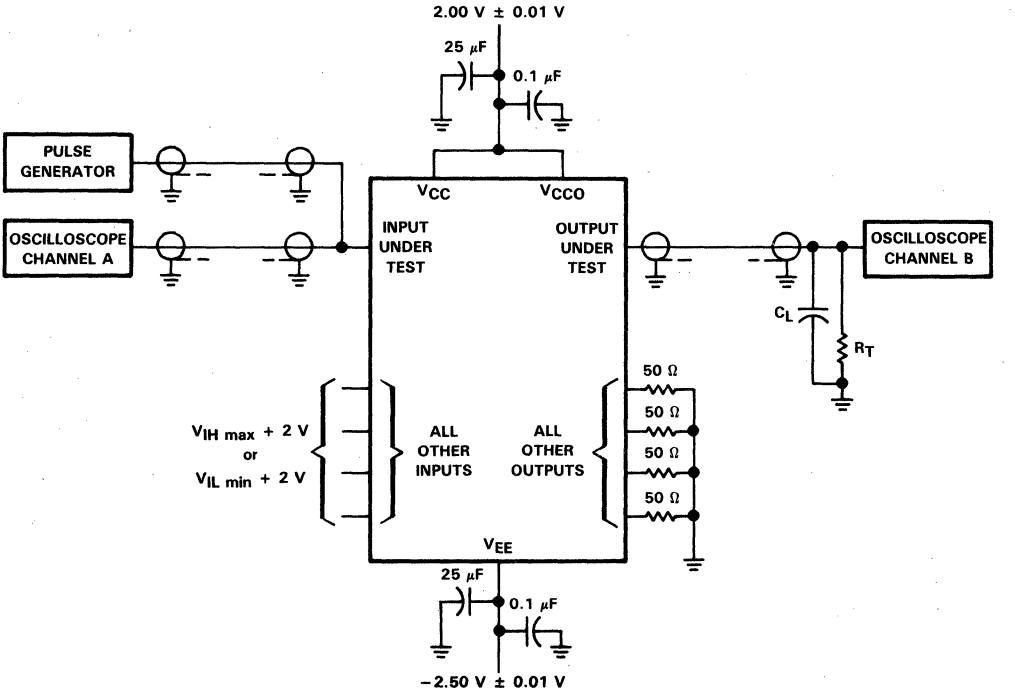
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
RISE TIME AND FALL TIME

FIGURE 1. VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The offset voltage generator has the following characteristics: Pulse amplitude = 800 mV P-P, PRR ≤ 1 MHz, t_w = 500 ns, $t_r = t_f$ = 1 ns.
B. R_T is a 50-Ω teminator internal to the oscilloscope.
C. $C_L \leq 3$ pF, includes fixture and stray capacitancea.
D. Coax has 50-Ω impedance and the coax to oscilloscope channel A and to channel B must be of equal lengths.
E. All unused outputs are loaded with 50-Ω ± 1% resistors to ground.
F. All unused input should be connected to either high or low levels consistent with the logic function required.
G. All fixture wire lengths or unterminated stubs should not exceed 6 mm (1/4 inch).

FIGURE 2. LOAD CIRCUIT

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14 × 32 × 6 FIELD-PROGRAMMABLE LOGIC ARRAYS

JUNE 1984—REVISED DECEMBER 1987

- **Input-to-Output Propagation Delay . . . 10 ns Typical**
- **24-Pin, 300-mil Slim Line Packages**
- **Power Dissipation . . . 650 mW Typical**
- **Programmable Output Polarity**

description

The 'FPLA839 (3-state outputs) and the 'FPLA840 (open-collector outputs) are TTL field-programmable logic arrays containing 32 product terms (AND terms) and six sum terms (OR terms). Each of the sum-of-products output functions can be programmed either high true or low true. The true condition of each output function is activated by the programmed logical minterms of 14 input variables. The outputs are controlled by two chip-enable pins to allow output inhibit and expansion of terms.

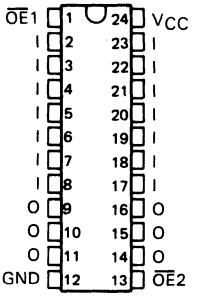
These devices provide high-speed data-path logic replacement where several conventional SSI functions can be designed into a single package.

The 'FPLA839M and 'FPLA840M are characterized for operation over the full military temperature range of −55 °C to 125 °C. The 'FPLA839C and 'FPLA840C are characterized for operation from 0 °C to 70 °C.

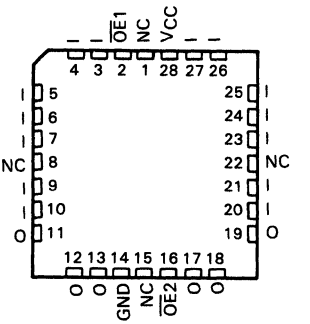
LOGIC FUNCTION

f(I) = P0 + P1 . . . P31 for polarity link intact
f(I) = $\overline{P0}$* $\overline{P1}$* . . . *$\overline{P31}$ for polarity link open
where P0 through P31 are product terms

TIFPLA839M, TIFPLA840M . . . JT PACKAGE
TIFPLA839C, TIFPLA840C . . . JT OR NT PACKAGE
(TOP VIEW)



TIFPLA839M, TIFPLA840M . . . FH OR FK PACKAGE
TIFPLA839C, TIFPLA840C . . . FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode (pin 1 is less positive than V_{IHH})

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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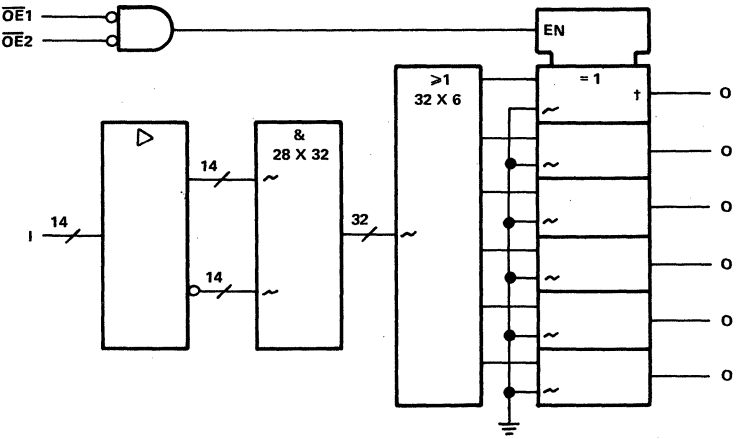
functional block diagram (positive logic)



~denotes fused inputs.
†FPLA839 has 3-state (▽) outputs; FPLA840 has open-collector (♢) outputs.

absolute maximum ratings

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Off-state output voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: 'FPLA839M, 'FPLA840M . . . . . −55°C to 125°C
'FPLA839C, 'FPLA840C . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

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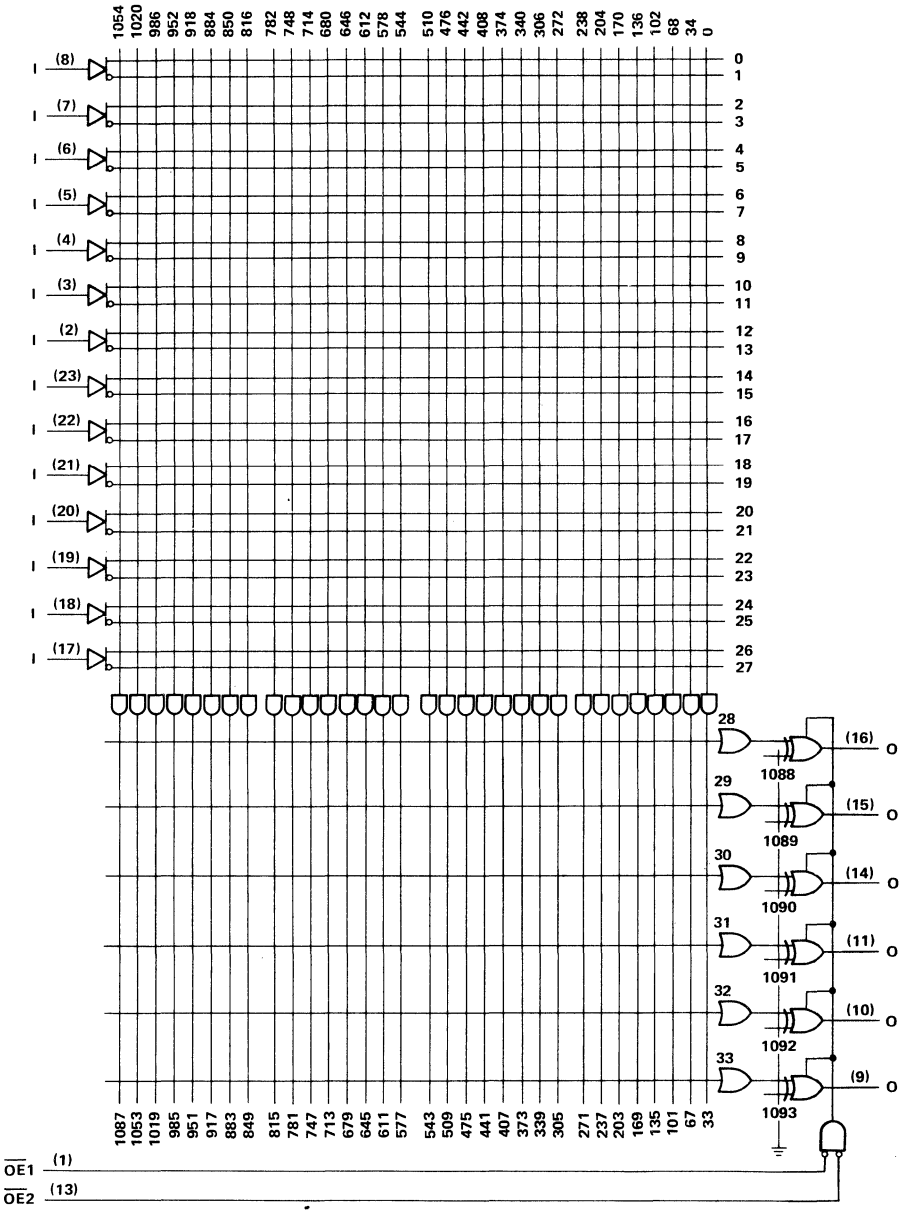
LOGIC DIAGRAM



recommended operating conditions

		M SUFFIX			C SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}		2			2			V
Low-level input voltage, V_{IL}				0.8			0.8	V
High-level output voltage, V_{OH}	'FPLA840			5.5			5.5	V
High-level output current, I_{OH}	'FPLA839			−2			−3.2	mA
Low-level output current, I_{OL}				12			24	mA
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		M SUFFIX			C SUFFIX			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
I_{OH} 'FPLA840	V_{CC} = MIN,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OH} 'FPLA839	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3		V
V_{OL}	V_{CC} = MIN,	I_{OL} = MAX		0.25	0.5		0.37	0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V			−0.5			−0.5	mA
I_O§	V_{CC} = MAX,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{OZH}	V_{CC} = MAX,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.4 V			−20			−20	μA
I_{CC}	V_{CC} = MAX, $\overline{OE}$ inputs at V_{IH}	V_I = 0 V,		130	190		130	180	mA

'FPLA839 switching characteristics

PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	Input	Output	R_L = 500 to GND, C_L = 50 pF to GND		10	25		10	20	ns
t_{en}	Pin 1 or Pin 13	Output	R_{L1} = 500 to 7 V, R_L = 500 to GND, C_L = 50 pF to GND		10	25		10	20	ns
t_{dis}					8	20		8	15	

'FPLA840 switching characteristics

PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	Input	Output	R_L = 500 to V_{CC}, C_L = 50 pF to GND		10	30		10	25	ns
t_{en}	Pin 1 or Pin 13	Output	R_{L1} = 500 to 7 V, R_L = 500 to GND, C_L = 50 pF to GND		10	25		10	20	ns
t_{dis}					8	20		8	15	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}.

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programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5762.

General Information 1

Data Sheets 2

Application Reports 3

Mechanical Data 4

Contents

	Page
Designing with TI Field-Programmable Logic	3-3
Hard Array Logic (HAL®)	3-25
A Designer's Guide to the TIBPSG507	3-31
System Solutions for Static Column Decode	3-81

Designing with Texas Instruments Field-Programmable Logic

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Contents

Title	*Page*
INTRODUCTION	3-7
FIELD-PROGRAMMABLE LOGIC ADVANTAGES	3-7
PAL® AND FPLA SYMBOLOGY	3-7
FAMILY ARCHITECTURES	3-8
PAL OPTIONS	3-9
Polarity Fuse	3-9
Input Registers	3-9
Input Latches	3-9
PROGRAMMING	3-12
DESIGN EXAMPLE	3-12
EXAMPLE REQUIREMENTS	3-13
PAL IMPLEMENTATION	3-13
PAL SELECTION	3-14
CLOCK SELECTOR DETAILS	3-14
4-BIT BINARY COUNTER DETAILS	3-16
BINARY/DECADE COUNT DETAILS	3-16
FUSE MAP DETAILS	3-17
ADVANCED SOFTWARE	3-21
PERFORMANCE	3-21
ADDRESSES FOR PROGRAMMING AND SOFTWARE MANUFACTURERS	6-24
Hardware Manufacturers	6-24
Software Manufacturers	6-24

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List of Illustrations

Figure	*Title*	*Page*
1	Basic Symbology	3-7
2	Basic Symbology Example	3-7
3	PROM Architecture	3-8
4	PAL Architecture	3-8
5	FPLA Architecture	3-9
6	TIBPLA16L8 Logic Diagram	3-10
7	TIBPAL16R8 Logic Diagram	3-11
8	Polarity Selection	3-12
9	Input Register Selection	3-12
10	Input Latch Selection	3-13
11	PAL Process Flow Diagram	3-13
12	Counter Implementation with Standard Logic	3-14
13	TIBPAL16R4 Logic Diagram	3-15
14	Karnaugh Map for $\overline{\text{CLKOUT}}$	3-16
15	Karnaugh Map for CLKOUT	3-16
16	Karnaugh Maps	3-17
17	Programmed TIBPAL16R4	3-18
18	Pin ID and Logic Equations	3-19
19	Fuse Map	3-20
20	Source File for ABEL	3-22
21	ABEL Output Documentation	3-23

List of Tables

Table	*Title*	*Page*
1	Clock Selection	3-13
2	Function Table	3-14
3	Truth Table	3-16
4	Truth Table	3-17

INTRODUCTION

The purpose of this application report is to provide the first time user of field-programmable logic with a basic understanding of this new and powerful technology. The term "Field-Programmable Logic" refers to any device supplied with an uncommitted logic array, which the user programs to his own specific function. The most common, and widely known field-programmable logic family is the PROM, or Programmable Read-Only Memory. Relatively new entries into this expanding family of devices are the PAL® and FPLA. This report will primarily concentrate on the PAL family of programmable logic.

FIELD-PROGRAMMABLE LOGIC ADVANTAGES

Field-programmable logic offers many advantages to the system designer who presently is using several standard catalog SSI and MSI functions. Listed below are just a few of the benefits which are achievable when using programmable logic.

1. Package Count Reduction: typically, 3 to 6 MSI/SSI functions can be replaced with one PAL or FPLA.
2. PC Board Area Reduced: Fewer devices consume less PC board space. This results in lower PC board cost.
3. Circuit Flexibility: Programmability allows for minor circuit changes without changing PC boards.
4. Improved Reliability: With fewer PC interconnects, overall system reliability increases.
5. Shorter Design Cycle: When compared with standard-cell or gate-array approaches, custom functions can be implemented much more quickly.

The PAL and FPLA, will fill the gap between standard logic and large scale integration. The versatility of these devices provide a very powerful tool for the system designer.

PAL AND FPLA SYMBOLOGY

In order to keep PAL and FPLA logic easy to understand and use, a special convention has been adopted. Figure 1 is the representation for a 3-input AND gate. Note that only one line is shown as the input to the AND gate. This line is commonly refered to as the product line. The inputs are shown as vertical lines, and at the intersection of these lines are the programmable fuses. An X represents an intact fuse. This makes that input, part of the product term. No X represents a blown fuse. This means that input will not be part of the product term (in Figure 1, input B is not part of the product term). A dot at the intersection of any line represents a hard wire connection.

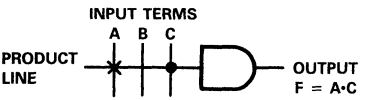

Figure 1. Basic Symbology

In Figure 2, we will extend the symbology to develop a simple 2-input programmable AND array feeding an OR gate. Notice that buffers have been added to the inputs, which provide both true and complement outputs to the product lines. The intersection of the input terms form a 4×3 programmable AND array. From the above symbology, we can see that the output of the OR gate is programmed to the following equation, $A\overline{B} + \overline{A}B$. Note that the bottom AND gate has an X marked inside the gate symbol. This means that all fuses are left intact, which results in that product line not having any effect on the sum term. In other words, the output of the AND gate will be a logic 0. **When all the fuses are blown on a product line, the output of the AND gate will always be a logic 1. This has the effect of locking up the output of the OR gate to a logic level 1.**

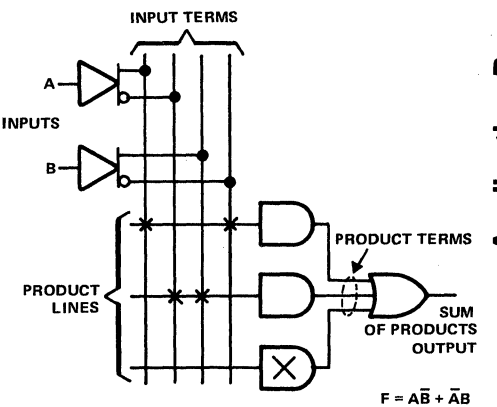

Figure 2. Basic Symbology Example

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FAMILY ARCHITECTURES

As stated before, the PROM was the first widely used programmable logic family. Its basic architecture is an input decoder configured from AND gates, combined with a programmable OR matrix on the outputs. As shown in Figure 3, this allows every output to be programmed individually from every possible input combination. In this example, a PROM with 4 inputs has 2^4, or 16 possible input combinations. With the output word width being 4 bits, each of the 16×4 bit words can be programmed individually. Applications such as data storage tables, character generators, and code converters, are just a few design examples which are ideally suited for the PROM. In general, any application which requires every input combination to be programmable, is a good candidate for a PROM. However, PROMs have difficulty accommodating large numbers of input variables. Eventually, the size of the fuse matrix will become prohibitive because for each input variable added, the size of the fuse matrix doubles. Currently, manufacturers are not producing PROMs with over 13 inputs.

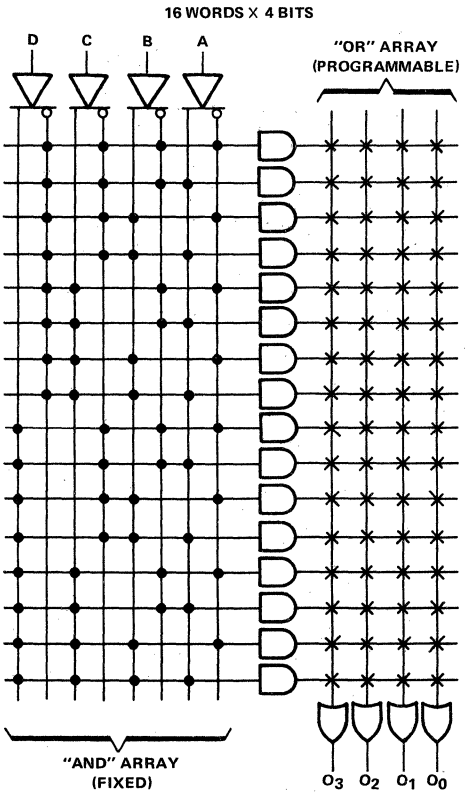


Figure 3. PROM Architecture

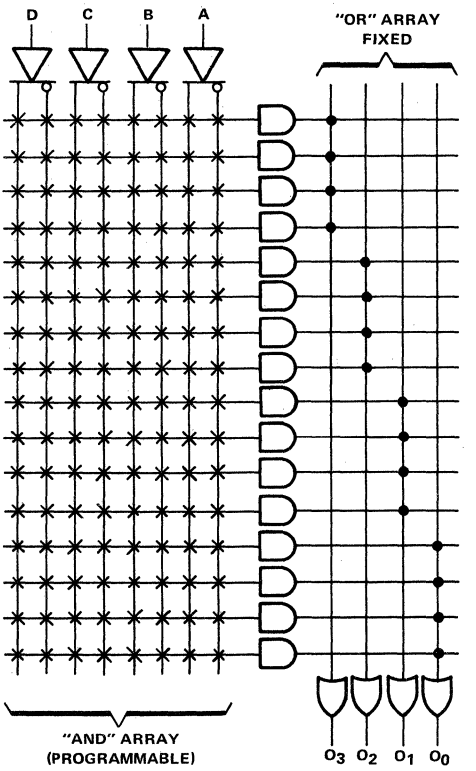


Figure 4. PAL Architecture

To overcome the limitation of a restricted number of inputs, the PAL utilizes a slightly different architecture as shown in Figure 4. The same AND-OR implementation is used as with PROMs, but now the input AND array is programmable instead of the output OR array. This has the effect of restricting the output OR array to a fixed number of input AND terms. The trade-off is that now, every output is not programmable from every input combination, but more inputs can be added without doubling the size of the fuse matrix. For example, If we were to expand the inputs on the PAL shown in Figure 4, to 10, and on the PROM in Figure 3, to 10. We would see that the fuse matrix required for the PAL would be 20×16 (320 fuses) vs 4×1024 (4096 fuses for the PROM). **It is important to realize that not every application requires every output be programmable from every input combination. This is what makes the PAL a viable product family.**

The FPLA goes one step further in offering both a programmable AND array, and a programmable OR array (Figure 5). This feature makes the FPLA the most versatile device of the three, but usually impractical in most low complexity applications.

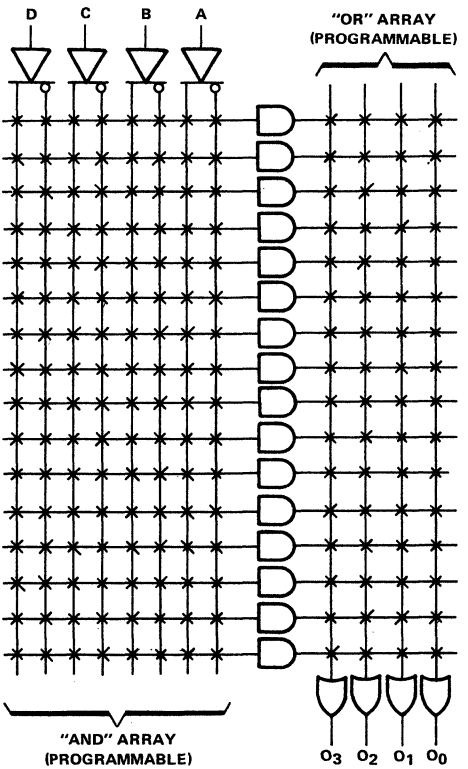


Figure 5. FPLA Architecture

All three field-programmable logic approaches discussed have their own unique advantages and limitations. The best choice depends on the complexity of the function being implemented and the current cost of the devices themselves. It is important to realize, that a circuit solution may exist from more than one of these logic families.

PAL OPTIONS

Figure 6 shows the logic diagram of the popular TIBPAL16L8. Its basic architecture is the same as discussed in the previous section, but with the addition of some special circuit features. First notice that the PAL has 10 simple inputs. In addition, 6 of the outputs operate as I/O ports. This allows feedback into the AND array. One AND gate in each product term controls each 3-state output. The architecture used in this PAL makes it very useful in generating all sorts of combinational logic.

Another important feature about the logic diagram, and all other block diagrams supplied from individual datasheets, are that there are no X's marked at every fuse location. From the previous convention, we stated that everywhere there was a intact fuse, there was an X. However, in order to make the logic diagram useful when generating specific functions, it is supplied with no X's. This allows the user to insert the X's wherever an intact fuse is desired.

The basic concept of the TIBPAL16L8 can be expanded further to include D-type flip-flops on the outputs. An example of this is shown in Figure 7 with the TIBPAL16R8. This added feature allows the device to be configured as a counter, simple storage register, or similar clocked function.

Circuit variations which are available on other members of the TI PAL and FPLA family are explained below.

Polarity Fuse

The polarity of the output can be selected via the fuse shown in Figure 8.

Input Registers

On PALs equipped with this special feature, the option of having D-type input registers is fuse programmable. Figure 9 shows an example of this type of input. If the fuse is left intact, data enters on a low-high transition of the clock. If the fuse is blown, the register becomes permanently transparent and is equivalent to a normal input buffer.

Input Latches

On PALs equipped with this special feature, the option of having input latches is fuse programmable.

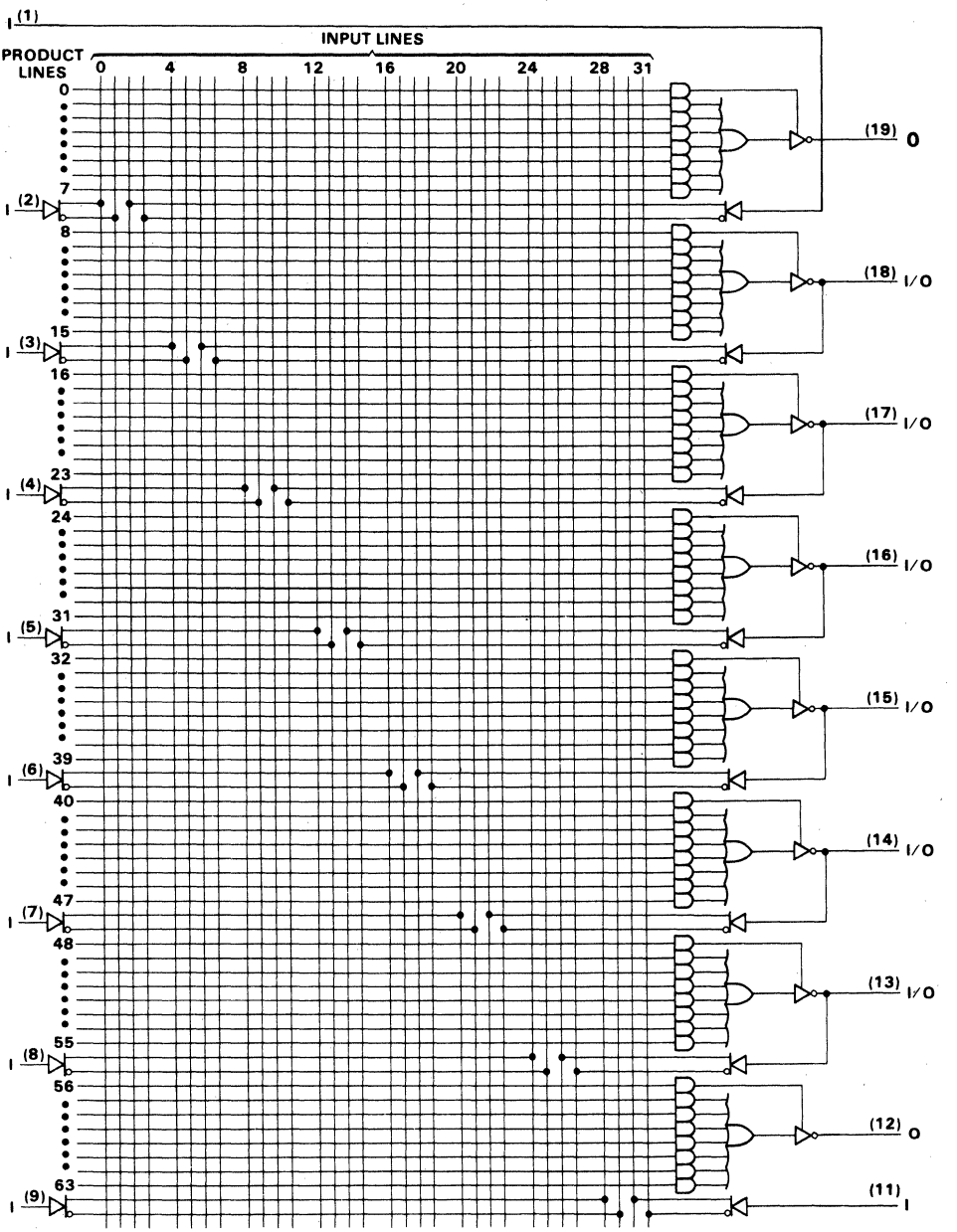


Figure 6. TIBPAL16L8 Logic Diagram

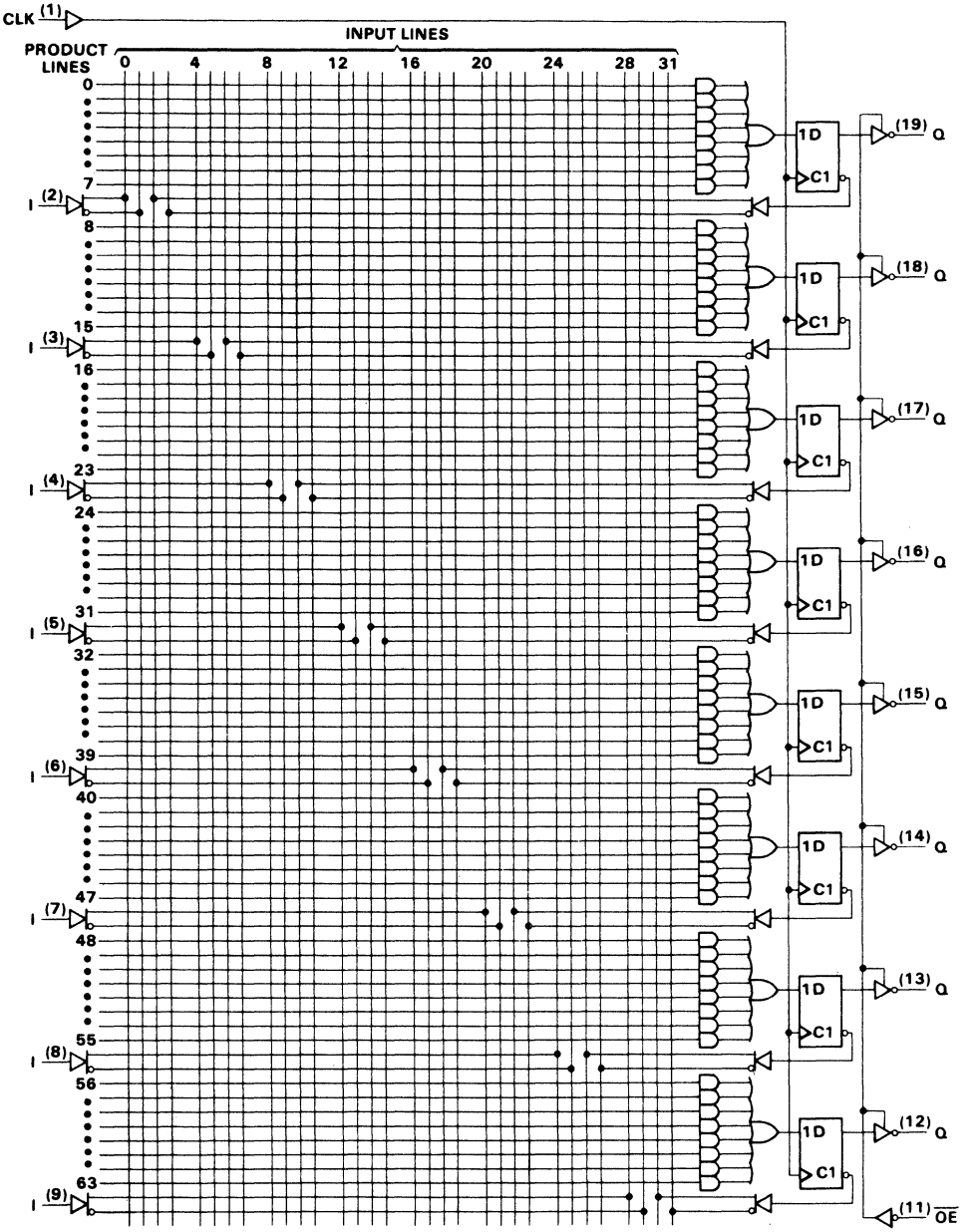
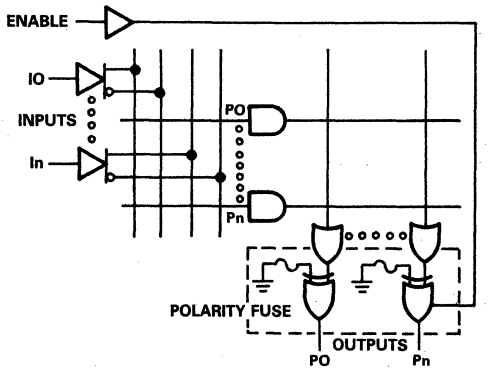


Figure 7. TIBPAL16R8 Logic Diagram



INTACT: OUTPUT = $\overline{PO} + \overline{P1} + \ldots + \overline{Pn}$
BLOWN: OUTPUT = $\overline{PO} \cdot \overline{P1} \cdot \ldots \cdot \overline{Pn}$

Figure 8. Polarity Selection

Figure 10 shows an example of this type of input. If the fuse is left intact, data enters while the control input is high. When the control input is low, the data that was present when the control input went low will be saved. If the fuse is blown, the latch becomes permanently transparent, and is equivalent to a normal input buffer.

PROGRAMMING

Notice in Figure 7, that the product and input lines are numbered. This allows any specific fuse to be located anywhere in the fuse matrix. When the device is in the programming mode (as defined in the device data sheet), the individual product and input lines can be selected. The fuse at the intersection of these lines, can then be blown (programmed) with the defined programming pulse. Fortunately, the user seldom has to get involved with these actual details of programming, because there exist several commercially available programmers which handle this function. Listed below are some of the manufacturers of this programming equipment.*

Citel	Storey Systems
DATA I/O	Structured Design
Digelec	Sunrise Electronics
Kontron	Valley Data Science
Wavetec	Varix
Stag Micro Systems	

At Texas Instruments, we have coordinated with DATA I/O using their Model 19 for device characterization. Currently, DATA I/O, Sunrise, and Structured Design have been certified by Texas Instruments. Other programmers are now in the certification process. For a current list of certified programmers, please contact your local TI sales representative.

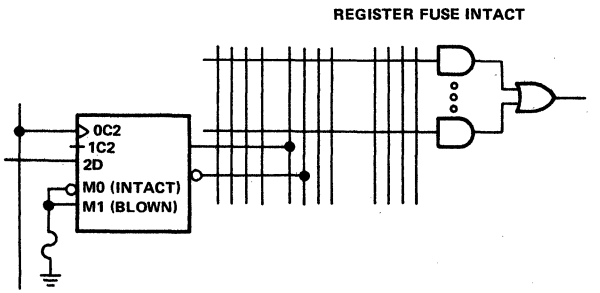
It should now be obvious to the reader, that the actual blowing of the fuses is not a problem. Instead, the real question is what fuses need to be blown to generate a particular function. Fortunately, this problem has also been greatly simplified by recent advances in computer software.

DATA I/O has developed a software package called ABEL™. Also available is CUPL™, from Assisted Technology. Both have been designed to be compatible with several different types of programmers. Both of these software packages greatly extend the capabilities of the original PALASM™ program, and both can be run on most professional computers.

Before proceeding to a design example, it would be instructive to look at the simplified process flow of a PAL (Figure 11). This should help give the reader a better understanding of the basic steps necessary to generate a working device.

DESIGN EXAMPLE

The easiest way to demonstrate the unique capabilities of the PAL is through a design example. It is



D-TYPE REGISTER FUNCTION TABLE

CLOCK	D	Q	$\overline{Q}$
↑	H	H	L
↑	L	L	H
L	X	Q_0	$\overline{Q}_0$

Q_0 = THE STATE OF Q BEFORE CLOCK ↑

Figure 9. Input Register Selection

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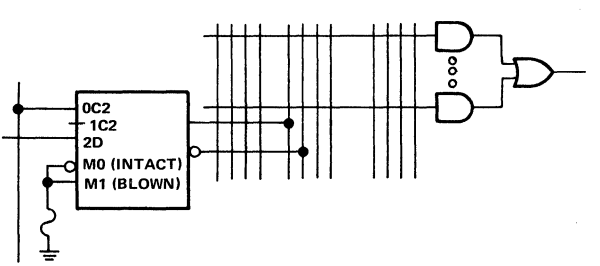
CUPL™ is a trademark of Assisted Technology, Inc.
PALASM™ is a trademark of Monolithic Memories Inc.



TRANSPARENT LATCH FUNCTION TABLE

ENABLE	D	O	$\overline{Q}$
H	L	L	H
H	H	H	L
L	X	Q_0	$\overline{Q}_0$

Q_0 = THE LEVEL OF Q BEFORE ENABLE ↓

Figure 10. Input Latch Selection

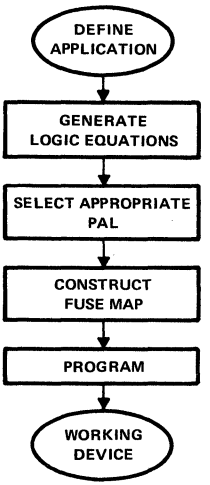


Figure 11. PAL Process Flow Diagram

hoped that through this example the reader will gain the basic understanding needed when applying the PAL in his own application. In some cases, this goal may only be to reduce existing logic, but the overall approach will be the same.

EXAMPLE REQUIREMENTS

It is desired to generate a 4-bit binary counter which is fed by one of four clocks. There are two lines available for selecting the clocks, SEL1 and SEL0. Table 1 shows the required input for the selection of the clocks. In addition, it is desired that the counter be able to switch from binary to decade count. This feature is controlled by an input called BD. When BD is high, the counter should count in binary. When low, the counter should count in decade.

Figure 12 shows how this example could be implemented if standard data book functions were used.

Table 1. Clock Selection

SEL1	SEL0	OUTPUT
0	0	CLKA
0	1	CLKB
1	0	CLKC
1	1	CLKD

As can be seen, three MSI functions are required. The 'LS162 is used to generate the 4-bit counter while the clock selection is handled by the 'LS253. The 'LS688 is an 8-bit comparator which is used for selecting either the binary or decade count. In this example, only five of the eight comparator inputs are used. Four are used for comparing the counter outputs, while the other is used for the BD input. The comparator is hard-wired to go low whenever the BD input is low and the counter output is "9". The $\overline{P=Q}$ output is then fed back to the synchronous clear input on the 'LS162. This will reset the counter to zero whenever this condition occurs.

PAL IMPLEMENTATION

As stated before, the problem in programming a PAL is not in blowing the fuses, but rather what fuses need to be blown to generate a particular function. Fortunately, this problem has been greatly simplified by computer software, but before we examine these techniques, it is beneficial to explore the methods used in generating the logic equations. This will help develop an understanding, and appreciation for these advanced software packages.

From digital logic theory, we know that most any type of logic can be implemented in either AND-OR-INVERT or AND-NOR form. This is the basic concept used in the PAL and FPLA. This allows classical techniques, such as Karnaugh Maps[1] to be used in generating specific logic functions. As with the separate component example above, it is easier to break it into separate functions. The first one that we will look at is the clock selector, but remember that the overall goal will be to reduce this design example into one PAL.

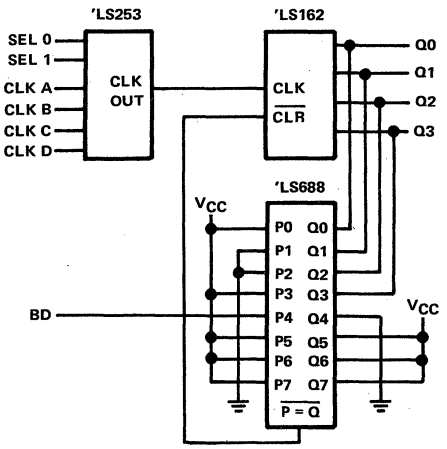


Figure 12. Counter Implementation with Standard Logic

PAL SELECTION

Before proceeding with the design for the clock selector, the first question which needs to be addressed is which PAL to use. As discussed earlier, there are several different types of output architectures. Looking at our example, we can see that four flip-flops with feedback will be required in the 4-bit counter, plus input clock and clear lines. In addition, seven inputs plus two simple outputs will be required in the clock selector and comparator. With this information in hand, we can see that the TIBPAL16R4 (Figure 13) will handle our application.

CLOCK SELECTOR DETAILS

The first step in determining the logic equation for the clock selector is to generate a function table with all the possible input combinations. This is shown in Table 2. From this table, the Karnaugh map can be generated and is shown in Figure 14. The minimized equation for CLKOUT comes directly from this.

Table 2. Function Table

SEL1	SEL0	CLKA	CLKB	CLKC	CLKD	CLKOUT	SEL1	SEL0	CLKA	CLKB	CLKC	CLKD	CLKOUT
0	0	0	0	0	0	0	1	0	0	0	0	0	0
0	0	0	0	0	1	0	1	0	0	0	0	1	0
0	0	0	0	1	0	0	1	0	0	0	1	0	1
0	0	0	0	1	1	0	1	0	0	0	1	1	1
0	0	0	1	0	0	0	1	0	0	1	0	0	0
0	0	0	1	0	1	0	1	0	0	1	0	1	0
0	0	0	1	1	0	0	1	0	0	1	1	0	1
0	0	0	1	1	1	0	1	0	0	1	1	1	1
0	0	1	0	0	0	1	1	0	1	0	0	0	0
0	0	1	0	0	1	1	1	0	1	0	0	1	0
0	0	1	0	1	0	1	1	0	1	0	1	0	1
0	0	1	0	1	1	1	1	0	1	0	1	1	1
0	0	1	1	0	0	1	1	0	1	1	0	0	0
0	0	1	1	0	1	1	1	0	1	1	0	1	0
0	0	1	1	1	0	1	1	0	1	1	1	0	1
0	0	1	1	1	1	1	1	0	1	1	1	1	1
0	1	0	0	0	0	0	1	1	0	0	0	0	0
0	1	0	0	0	1	0	1	1	0	0	0	1	1
0	1	0	0	1	0	0	1	1	0	0	1	0	0
0	1	0	0	1	1	0	1	1	0	0	1	1	1
0	1	0	1	0	0	1	1	1	0	1	0	0	0
0	1	0	1	0	1	1	1	1	0	1	0	1	1
0	1	0	1	1	0	1	1	1	0	1	1	0	0
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	0	0	0	1	1	1	0	0	0	0
0	1	1	0	0	1	0	1	1	1	0	0	1	1
0	1	1	0	1	0	0	1	1	1	0	1	0	0
0	1	1	0	1	1	0	1	1	1	0	1	1	1
0	1	1	1	0	0	1	1	1	1	1	0	0	0
0	1	1	1	0	1	1	1	1	1	1	0	1	1
0	1	1	1	1	0	1	1	1	1	1	1	0	0
0	1	1	1	1	1	1	1	1	1	1	1	1	1

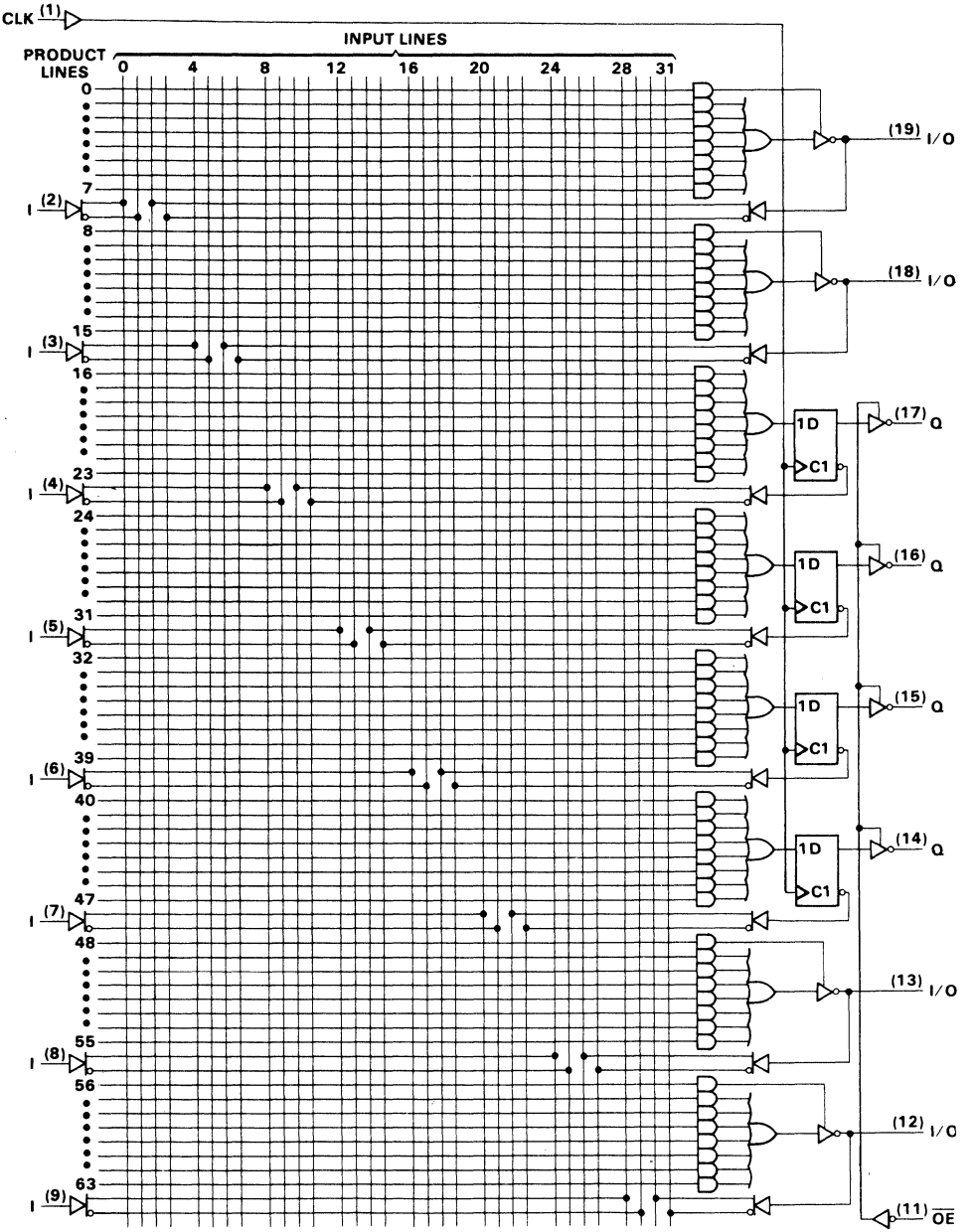
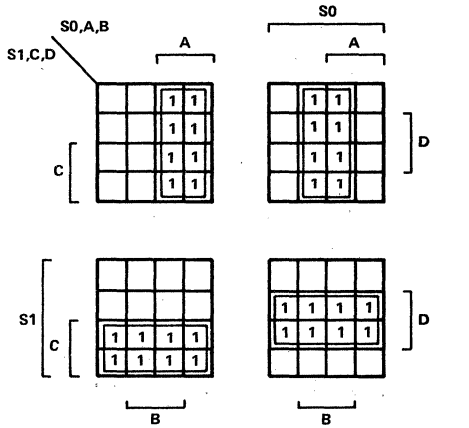


Figure 13. TIBPAL16R4 Logic Diagram

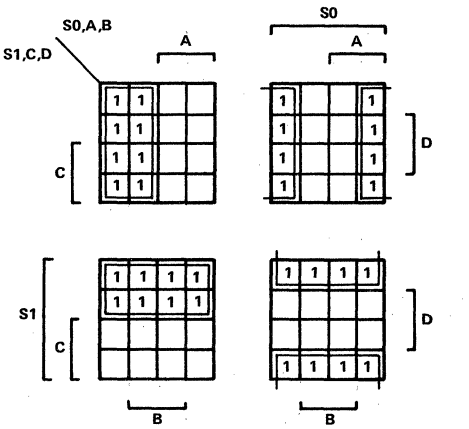
It is important to notice that the equation derived from the Karnaugh map is stated in AND-OR notation. The PAL that we have selected is implemented in AND-NOR logic. This means we either have to do DeMorgan's theorem on the equation, or solve the inverse of the Karnaugh map. Figure 15 shows the inverse of the Karnaugh map and the resulting equation. This equation can be easily implemented in the TIBPAL16R4.



$CLKOUT = \overline{S1}\,\overline{S0}A + \overline{S1}S0B + S1\overline{S0}C + S1S0D$

$CLKOUT = \overline{S1}\,\overline{S0}A + \overline{S1}S0B + S1\overline{S0}C + S1S0D$

Figure 14. Karnaugh Map for CLKOUT



$\overline{CLKOUT} = \overline{S1}\,\overline{S0}A + \overline{S1}S0B + S1\overline{S0}C + S1S0D$

$\overline{CLKOUT} = \overline{S1}\,\overline{S0}A + \overline{S1}S0B + S1\overline{S0}C + S1S0D$

Figure 15. Karnaugh Map for $\overline{CLKOUT}$

4-BIT BINARY COUNTER DETAILS

The same basic procedure used in determining the equations for the clock selector, is used in determining the equations for the 4-bit counter. The only difference is that now we are dealing with a present state, next state situation. This means a D-type flip-flop will be required in actual circuit implementation. As before, the truth table is generated first, and is shown in Table 3.

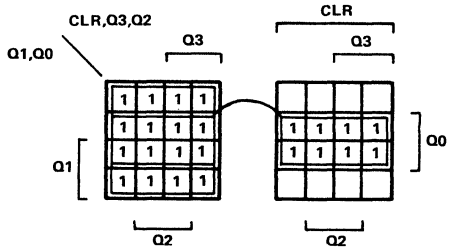
Table 3. Truth Table

	PRESENT STATE				NEXT STATE			
CLR	Q3	Q2	Q1	Q0	Q3	Q2	Q1	Q0
0	X	X	X	X	0	0	0	0
1	0	0	0	0	0	0	0	1
1	0	0	0	1	0	0	1	0
1	0	0	1	0	0	0	1	1
1	0	0	1	1	0	1	0	0
1	0	1	0	0	0	1	0	1
1	0	1	0	1	0	1	1	0
1	0	1	1	0	0	1	1	1
1	0	1	1	1	1	0	0	0
1	1	0	0	0	1	0	0	1
1	1	0	0	1	1	0	1	0
1	1	0	1	0	1	0	1	1
1	1	0	1	1	1	1	0	0
1	1	1	0	0	1	1	0	1
1	1	1	0	1	1	1	1	0
1	1	1	1	0	1	1	1	1
1	1	1	1	1	0	0	0	0

From the truth table, the equations for each output can be derived from the Karnaugh map. This is shown in Figure 16. Note that the inverse of the truth table is being solved so that the equation will come out in AND-NOR logic form.

BINARY/DECADE COUNT DETAILS

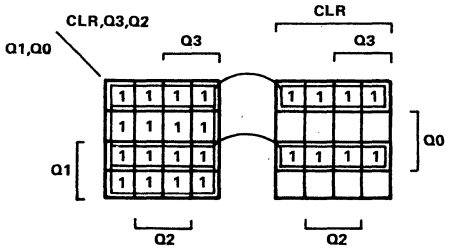
Recalling from the example requirements that the counter should count in decade whenever the BD input is low, we can again generate a truth table for this function (Table 4). Since the counter is already designed to count in binary, we can use this feature to simplify our design. What we desire is a circuit whose output goes low, whenever the BD input is equal to a logic level "0", and the counter output is equal to "9". This output can then be fed back to the CLR input of the counter so that it will reset whenever the BD input is low. Whenever the BD input is high, the output of the circuit should be a high since the counter will automatically count in binary. Notice that $\overline{Q}$ shown in the truth table is the function we desire.



$\overline{Q0} = \overline{CLR}\overline{Q3Q2Q1Q0} + \overline{CLR}\overline{Q3Q2Q1}Q0$

$\overline{Q0} = \overline{CLR} + Q0$

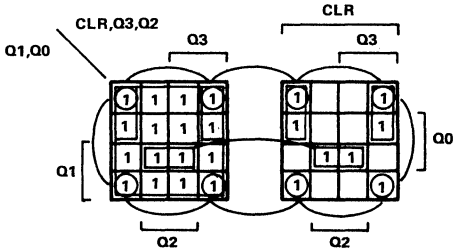
(a) KARNAUGH MAP FOR $\overline{Q0}$



$\overline{Q1} = \overline{CLR}\overline{Q3Q2Q1Q0} + \overline{CLR}\overline{Q3Q2}\overline{Q1}\overline{Q0} + \overline{CLR}\overline{Q3Q2}Q1Q0$

$\overline{Q1} = \overline{CLR} + \overline{Q1}\overline{Q0} + Q1Q0$

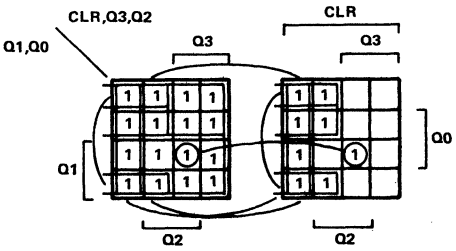
(b) KARNAUGH MAP FOR $\overline{Q1}$



$\overline{Q2} = \overline{CLR}\overline{Q3Q2Q1Q0} + \overline{CLR}\overline{Q3}\overline{Q2}\overline{Q1}\overline{Q0} + \overline{CLR}\overline{Q3}Q2Q1Q0$
$+ \overline{CLR}\overline{Q3}\overline{Q2}Q1\overline{Q0}$

$\overline{Q2} = \overline{CLR} + \overline{Q2}\overline{Q1} + Q2Q1Q0 + \overline{Q2}\overline{Q0}$

(c) KARNAUGH MAP FOR $\overline{Q2}$



$\overline{Q3} = \overline{CLR}\overline{Q3Q2Q1Q0} + \overline{CLR}\overline{Q3}Q2\overline{Q1}\overline{Q0} + \overline{CLR}\overline{Q3}Q2Q1Q0$
$+ \overline{CLR}\overline{Q3}\overline{Q2}\overline{Q1}\overline{Q0} + \overline{CLR}Q3Q2Q1Q0$

$\overline{Q3} = \overline{CLR} + \overline{Q3}\overline{Q2} + \overline{Q3}\overline{Q1} + \overline{Q3}\overline{Q0} + Q3Q2Q1Q0$

(d) KARNAUGH MAP FOR $\overline{Q3}$

Figure 16. Karnaugh Maps

In this particular example, a Karnaugh map is not required because the equation cannot be further simplified. The resulting equation is given below.

$$\overline{BD\ OUT} = \overline{BD}Q3\overline{Q2}\overline{Q1}Q0$$

Table 4. Truth Table

BD	Q3	Q2	Q1	Q0	Q	$\overline{Q}$	BD	Q3	Q2	Q1	Q0	Q	$\overline{Q}$
0	0	0	0	0	0	1	1	0	0	0	0	0	1
0	0	0	0	1	0	1	1	0	0	0	1	0	1
0	0	0	1	0	0	1	1	0	0	1	0	0	1
0	0	0	1	1	0	1	1	0	0	1	1	0	1
0	0	1	0	0	0	1	1	0	1	0	0	0	1
0	0	1	0	1	0	1	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1	0	1	1	0	0	1
0	0	1	1	1	0	1	1	0	1	1	1	0	1
0	1	0	0	0	0	1	1	1	0	0	0	0	1
0	1	0	0	1	1	0	1	1	0	0	1	0	1
0	1	0	1	0	0	1	1	1	0	1	0	0	1
0	1	0	1	1	0	1	1	1	0	1	1	0	1
0	1	1	0	0	0	1	1	1	1	0	0	0	1
0	1	1	0	1	0	1	1	1	1	0	1	0	1
0	1	1	1	0	0	1	1	1	1	1	0	0	1
0	1	1	1	1	0	1	1	1	1	1	1	0	1

FUSE MAP DETAILS

Now that the logic equations have been defined, the next step will be to specify which fuses need to be blown. Before we do this however, we first need to label the input and output pins on the TIBPAL16R4. By using Figure 12 as a guide, we can make the following pin assignments in Figure 17.

PIN			
1	CLK	20	VCC
2	SEL0	19	CLKOUT
3	SEL1	18	NC
4	CLKA	17	Q0
5	CLKB	16	Q1
6	CLKC	15	Q2
7	CLKD	14	Q3
8	CLR	13	NC
9	BD	12	BD OUT
10	GND	11	OE

With this information defined, we now need to insert the logic equations into the logic diagram as shown in Figure 17.

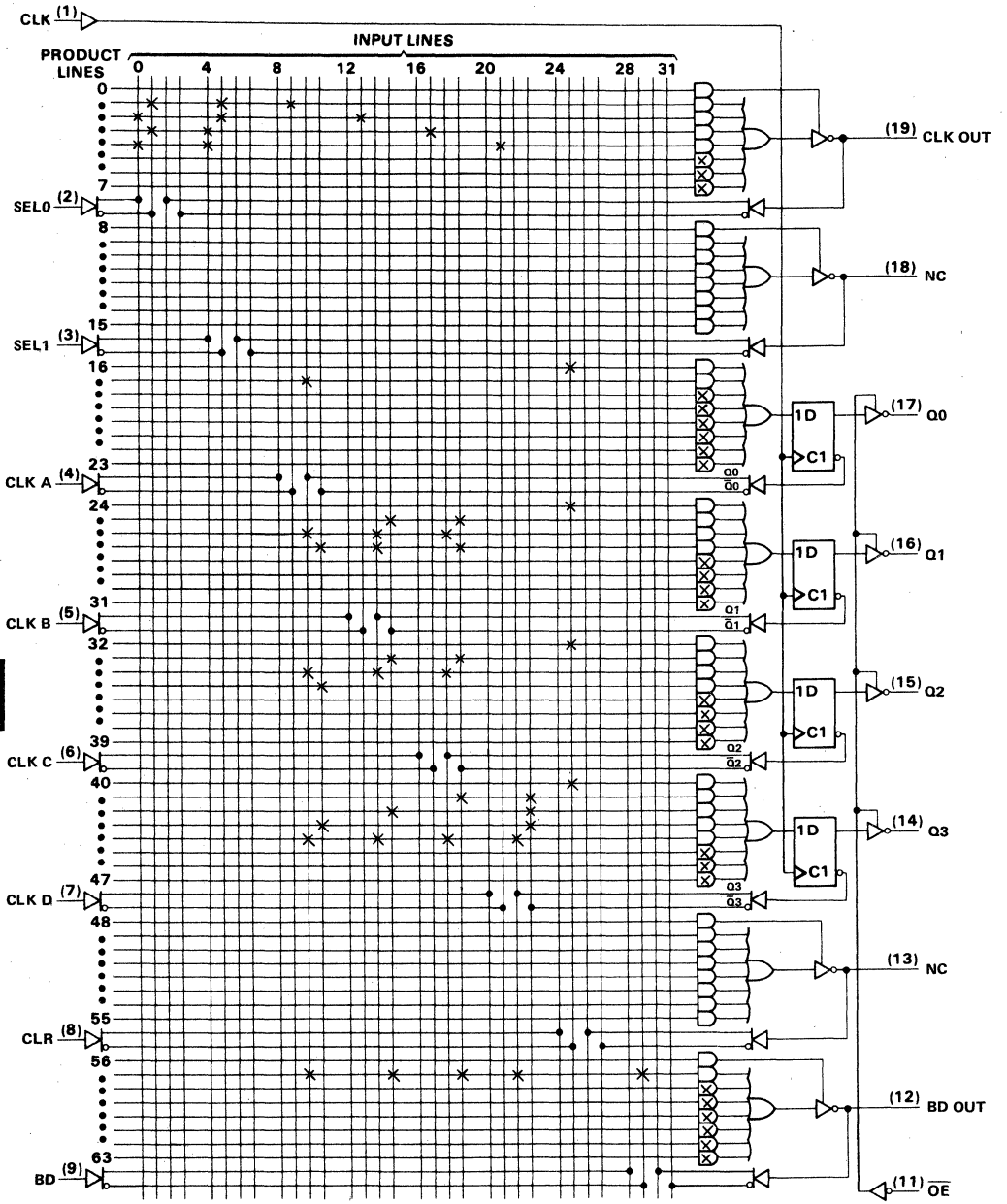


Figure 17. Programmed TIBPAL16R4

It is now probably obvious to the reader, that inserting the logic equations into the logic diagram is a tedious operation. Fortunately, a computer program called PALASM will perform this task automatically. All that is required is telling the program which device has been selected, and defining the input and output pins with their appropriate logic equations (Figure 18). The program will then generate a fuse map (Figure 19) for the device selected. Notice that the fuse map looks very similar to the block diagram (Figure 17) which we have just completed by hand. In addition, this information can now be down loaded into the selected device programmer.

```
DEVICE TYPE 16R4


PIN LIST NAMES =
PIN NUMBER =  1    PIN NAME = CLK
PIN NUMBER =  2    PIN NAME = SEL0
PIN NUMBER =  3    PIN NAME = SEL1
PIN NUMBER =  4    PIN NAME = CLKA
PIN NUMBER =  5    PIN NAME = CLKB
PIN NUMBER =  6    PIN NAME = CLKC
PIN NUMBER =  7    PIN NAME = CLKD
PIN NUMBER =  8    PIN NAME = CLR
PIN NUMBER =  9    PIN NAME = BD
PIN NUMBER = 10    PIN NAME = GND
PIN NUMBER = 11    PIN NAME = /OE
PIN NUMBER = 12    PIN NAME = BDOUT
PIN NUMBER = 13    PIN NAME = NC
PIN NUMBER = 14    PIN NAME = Q3
PIN NUMBER = 15    PIN NAME = Q2
PIN NUMBER = 16    PIN NAME = Q1
PIN NUMBER = 17    PIN NAME = Q0
PIN NUMBER = 18    PIN NAME = NC
PIN NUMBER = 19    PIN NAME = CLKOUT
PIN NUMBER = 20    PIN NAME = VCC


EXPRESSIONS  AND DESCRIPTION =
EXPRESSION[ 1] =
/CLKOUT=/SEL1*/SEL0*/CLKA +/SEL1*SEL0*/CLKB +SEL1*/SEL0*/CLKC +SEL1*SEL0*/CLKD


EXPRESSION[ 2] =
/Q0=/CLR +Q0


EXPRESSION[ 3] =
/Q1=/CLR +/Q1*/Q0 +Q1*Q0


EXPRESSION[ 4] =
/Q2=/CLR +/Q2*/Q1 +Q2*Q1*Q0 +/Q2*/Q0


EXPRESSION[ 5] =
/Q3=/CLR +/Q3*/Q2 +/Q3*/Q1 +/Q3*/Q0 +Q3*Q2*Q1*Q0


EXPRESSION[ 6] =
/BDOUT=/BD*Q3*/Q2*/Q1*Q0
```

Figure 18. Pin ID and Logic Equations

```
0000 0000 0011 1111 1111 2222 2222 2233
0123 4567 8901 2345 6789 0123 4567 8901
/CLKOUT  =
---- ---- ---- ---- ---- ---- ---- ----   0 -
-X-- -X-- -X-- ---- ---- ---- ---- ----   1 - /SEL1*/SEL0*/CLKA+
X--- -X-- ---- -X-- ---- ---- ---- ----   2 - /SEL1*SEL0*/CLKB+
-X-- X--- ---- ---- -X-- ---- ---- ----   3 - SEL1*/SEL0*/CLKC+
X--- X--- ---- ---- ---- -X-- ---- ----   4 - SEL1*SEL0*/CLKD
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX   5 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX   6 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX   7 -
        =
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX   8 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX   9 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  10 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  11 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  12 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  13 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  14 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  15 -
/Q0      =
---- ---- ---- ---- ---- ---- -X-- ----  16 - /CLR+
---- ---- --X- ---- ---- ---- ---- ----  17 - Q0
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  18 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  19 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  20 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  21 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  22 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  23 -
/Q1      =
---- ---- ---- ---- ---- ---- -X-- ----  24 - /CLR+
---- ---- ---X ---X ---- ---- ---- ----  25 - /Q1*/Q0+
---- ---- --X- --X- ---- ---- ---- ----  26 - Q1*Q0
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  27 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  28 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  29 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  30 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  31 -
/Q2      =
---- ---- ---- ---- ---- ---- -X-- ----  32 - /CLR+
---- ---- ---- ---X ---X ---- ---- ----  33 - /Q2*/Q1+
---- ---- --X- --X- --X- ---- ---- ----  34 - Q2*Q1*Q0+
---- ---- ---X ---- ---X ---- ---- ----  35 - /Q2*/Q0
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  36 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  37 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  38 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  39 -
/Q3      =
---- ---- ---- ---- ---- ---- -X-- ----  40 - /CLR+
---- ---- ---- ---- ---X ---X ---- ----  41 - /Q3*/Q2+
---- ---- ---- ---X ---- ---X ---- ----  42 - /Q3*/Q1+
---- ---- ---X ---- ---- ---X ---- ----  43 - /Q3*/Q0+
---- ---- --X- --X- --X- --X- ---- ----  44 - Q3*Q2*Q1*Q0
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  45 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  46 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  47 -
        =
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  48 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  49 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  50 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  51 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  52 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  53 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  54 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  55 -
/BDOUT   =
---- ---- ---- ---- ---- ---- ---- ----  56 -
---- ---- --X- ---X ---X --X- ---- -X--  57 - /BD*Q3*/Q2*/Q1*Q0
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  58 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  59 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  60 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  61 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  62 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  63 -
```

Figure 19. Fuse Map

ADVANCED SOFTWARE

PALASM, while extremely useful in generating the fuse map, does little to help formulate the logic equations. This is what the new software packages such as ABEL and CUPL address. They not only generate the fuse map, but they also help in developing the logic equations. In most cases, they can generate the logic equations from simply providing the program with either a truth table or state diagram. In addition, they can test the logic equations against a set of test vectors. This helps ensure the designer gets the desired function.

These are only a few of the features available on these new advanced software packages. We recommend that the reader contact the specific manufacturers themselves to obtain the latest information available. For your convenience, at the end of this application note we have included the addresses and phone numbers for many of these programming and software companies.

As an example, we will approach our previous design utilizing DATA I/O's ABEL package. The purpose here is not to teach the reader how to use ABEL, but rather to give them a basic overview of this powerful software package. Figure 20 shows the source file required by ABEL. Note that the 4-bit counter has been described with a state diagram table. When the ABEL program is complied, the logic equations will be generated from this. The equations for CLK OUT and BD OUT have been given in their final form to demonstrate how ABEL would handle these. Also notice that test vectors are included for checking the logic equations. This is especially important when only the logic equations has been given.

Figure 21 shows some of the output documentation generated by the program. Notice that the equations generated for the counter, match the the ones generated by the Karnaugh maps. A pinout for the device has also been generated and displayed. The fuse map for the device has not been shown, but looks very similar to the one in Figure 19. As with the PALASM program, this information can be down loaded into the device programmer.

PERFORMANCE

Up to this point, nothing has been said about the performance of these devices. The Standard High Speed PAL (indicated by an "A" after the device number) offered by TI has a maximum propagation of 25 ns from input to output, and 35 MHz f_{max}. Also available is a new, higher speed family of devices called TIBPALs. These devices are functionally equivalent with the current family and offer a maximum propagation delay of 15 ns from input to output. They are also rated at 50 MHz f_{max}. The higher speeds on these devices make them compatible with most high-speed logic families. This allows them to be designed into more critical speed path applications.

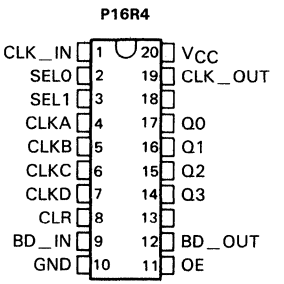
```
module BD_COUNT flag '-r2'
title '4-bit binary/decade counter

      IC1  device 'P16R4';

"  pin assignments and constant declarations
      CLK_IN,SEL0,SEL1,CLKA      pin  1,2,3,4;
      CLKB,CLKC,CLKD             pin  5,6,7;
      CLR,BD_IN,OE               pin  8,9,11;
      BD_OUT,CLK_OUT             pin  12,19;
      Q3,Q2,Q1,Q0                pin  14,15,16,17;
      CK, L, H, X, Z  =          .C. , 0 , 1 , .X. , .Z.;
      OUTPUT          =          [Q3,Q2,Q1,Q0];

"  counter states
      S0=^b0000;   S4=^b0100;   S8=^b1000;   S12=^b1100;
      S1=^b0001;   S5=^b0101;   S9=^b1001;   S13=^b1101;
      S2=^b0010;   S6=^b0110;  S10=^b1010;   S14=^b1110;
      S3=^b0011;   S7=^b0111;  S11=^b1011;   S15=^b1111;

equations
"  clock selector
      CLK_OUT = CLKA & !SEL0 & !SEL1 # CLKB & !SEL1 & SEL0
                # CLKC & SEL1 & !SEL0 # CLKD & SEL1 & SEL0;

"  count nine indicator for decade counting
      BD_OUT  = !(!BD_IN & Q3 & !Q2 & !Q1 & Q0);

state_diagram [Q3,Q2,Q1,Q0]
      State  S0:  IF CLR == 0 THEN S0 ELSE  S1;
      State  S1:  IF CLR == 0 THEN S0 ELSE  S2;
      State  S2:  IF CLR == 0 THEN S0 ELSE  S3;
      State  S3:  IF CLR == 0 THEN S0 ELSE  S4;
      State  S4:  IF CLR == 0 THEN S0 ELSE  S5;
      State  S5:  IF CLR == 0 THEN S0 ELSE  S6;
      State  S6:  IF CLR == 0 THEN S0 ELSE  S7;
      State  S7:  IF CLR == 0 THEN S0 ELSE  S8;
      State  S8:  IF CLR == 0 THEN S0 ELSE  S9;
      State  S9:  IF CLR == 0 THEN S0 ELSE S10;
      State S10:  IF CLR == 0 THEN S0 ELSE S11;
      State S11:  IF CLR == 0 THEN S0 ELSE S12;
      State S12:  IF CLR == 0 THEN S0 ELSE S13;
      State S13:  IF CLR == 0 THEN S0 ELSE S14;
      State S14:  IF CLR == 0 THEN S0 ELSE S15;
      State S15:  IF CLR == 0 THEN S0 ELSE  S0;

test_vectors   'clock selector'
     ([CLKA, CLKB, CLKC, CLKD, SEL1, SEL0] -> CLK_OUT)
      [ L  ,  X  ,  X  ,  X  ,   L,    L ] ->   L;
      [ H  ,  X  ,  X  ,  X  ,   L,    L ] ->   H;
      [ X  ,  L  ,  X  ,  X  ,   L,    H ] ->   L;
      [ X  ,  H  ,  X  ,  X  ,   L,    H ] ->   H;
      [ X  ,  X  ,  L  ,  X  ,   H,    L ] ->   L;
      [ X  ,  X  ,  H  ,  X  ,   H,    L ] ->   H;
      [ X  ,  X  ,  X  ,  L  ,   H,    H ] ->   L;
      [ X  ,  X  ,  X  ,  H  ,   H,    H ] ->   H;

test_vectors   'counter'
     ([CLK_IN, OE, CLR, BD_IN] -> [OUTPUT, BD_OUT])
      [  CK,   L ,  L,     X  ] -> [  S0,   H ];
      [  CK,   L ,  H,     X  ] -> [  S1,   H ];
      [  CK,   L ,  H,     X  ] -> [  S2,   H ];
      [  CK,   L ,  H,     X  ] -> [  S3,   H ];
      [  CK,   L ,  H,     X  ] -> [  S4,   H ];
      [  CK,   L ,  H,     X  ] -> [  S5,   H ];
      [  CK,   L ,  H,     X  ] -> [  S6,   H ];
      [  CK,   L ,  H,     X  ] -> [  S7,   H ];
      [  CK,   L ,  H,     X  ] -> [  S8,   H ];
      [  CK,   L ,  H,     L  ] -> [  S9,   L ];
      [  CK,   L ,  H,     X  ] -> [ S10,   H ];
      [  CK,   L ,  H,     X  ] -> [ S11,   H ];
      [  CK,   L ,  H,     X  ] -> [ S12,   H ];
      [  CK,   L ,  H,     X  ] -> [ S13,   H ];
      [  CK,   L ,  H,     X  ] -> [ S14,   H ];
      [  CK,   L ,  H,     H  ] -> [ S15,   H ];
      [  CK,   L ,  H,     X  ] -> [  S0,   H ];
      [   X,   H ,  X,     X  ] -> [   Z ,  H ];
end BD_COUNT
```

Figure 20. Source File for ABEL

```
ABEL(tm) Version  1.00  - Document Generator
4-bit binary/decade counter

Equations for Module BD_COUNT

Device IC1


     Reduced Equations:

       CLK_OUT = !((SEL1 & SEL0 & !CLKD
                  # (SEL1 & !SEL0 & !CLKC
                  # (!SEL1 & SEL0 & !CLKB
                  # !SEL1 & !SEL0 & !CLKA)));


       BD_OUT = !(Q3 & !Q2 & !Q1 & Q0 & !BD_IN);

       Q3 := !((Q3 & Q2 & Q1 & Q0
              # (!Q3 & !Q2
              # (!Q3 & !Q1
              # (!Q3 & !Q0
              # !CLR)))));


       Q2 := !((Q2 & Q1 & Q0 # (!Q2 & !Q1 # (!Q2 & !Q0 # !CLR))));

       Q1 := !((Q1 & Q0 # (!Q1 & !Q0 # !CLR)));

       Q0 := !((Q0 # !CLR));
```



```
ABEL(tm) Version  1.00  - Document Generator
4-bit binary/decade counter

Chip diagram for Module BD_COUNT

Device IC1
```




```
end of module BD_COUNT
```

Figure 21. ABEL Output Documentation

ADDRESSES FOR PROGRAMMING AND SOFTWARE MANUFACTURERS*

HARDWARE MANUFACTURERS

Citel
3060 Raymond St.
Santa Clara, CA 95050
(408) 727-6562

DATA I/O
10525 Willows Rd.
Redmond, WA 98052
(206) 881-6444

DIGITAL MEDIA
3178 Gibralter Ave.
Costa Mesa, CA 92626
(714) 751-1373

Kontron Electronics
630 Price Avenue
Redwood City, CA 94063
(415) 361-1012

Stag Micro Systems
528-5 Weddell Drive
Sunnyvale, CA 94086
(408) 745-1991

Storey Systems
3201 N. Hwy 67, Suite H
Mesquite, Tx 75150
(214) 270-4135

Structured Design
1700 Wyatt Dr., Suite 7
Santa Clara, CA 95054
(408) 988-0725

Sunrise Electronics
524 S. Vermont Avenue
Glendora, CA 91740
(213) 914-1926

Valley Data Sciences
2426 Charleston Rd.
Mountain View, CA 94043
(415) 968-2900

Varix
1210 Campbell Rd.
Richardson, TX 75081
(214) 437-0777

Wavetec/Digelec
586 Weddel Dr., Suite 1
Sunnyvale, CA 94089
(408) 745-0722

SOFTWARE MANUFACTURERS

Assisted Technologies (CUPL)
2381 Zanker Road, Suite 150
Santa Clara, CA 95050
(408) 942-8787

DATA I/O (ABEL)
10525 Willows Rd.
Redmond, WA 98052
(206) 881-6444

*Texas Instruments does not endorse or warrant the suppliers referenced.

Reference

1. H. Troy Nagle, Jr., B.D. Carroll, and David Irwin, *An Introduction to Computer Logic*. New Jersey: Prentice-Hall, Inc., 1975.

Hard Array Logic (HAL®)

TEXAS INSTRUMENTS

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INTRODUCTION

The purpose of this document is to provide the design and component engineer with a better understanding of Hard Array Logic (HAL®). [It details both the advantages and disadvantages of HAL and Programmable Array Logic (PAL®) designs as a means of aiding the design and component engineer in deciding whether to go to a HAL device or to remain with the (PAL) product.] More importantly, this document also defines the procedures to be used by the customer when ordering HALs from Texas Instruments.

PRODUCT DESCRIPTION

Programmable Array Logic (PAL) technology constitutes one of the fastest growing areas in the semiconductor industry today. This growth exists because PALs offer circuit flexibility and package count reduction, an advantage which design and component engineers find over standard catalog devices. Another advantage PALs offer is shorter design cycle times when compared to semicustom design approaches. However, once a PAL design has been proven and is to be phased into full production, the flexibility advantage inherently becomes costly since each PAL device must be individually programmed. Therefore, programming cost may be appreciable where a design requirement calls for a high total volume level. This is where a HAL design can become cost effective. HAL circuits are fixed and do not require individual programming.

PALs and HALs are fabricated in the same manner except for their final two metallization layers. In PALs the programmable titanium-tungsten fuse array is provided which gives the PAL its circuit flexibility. However, in a HAL, a custom metallization mask is used, which places solid metal links in the fuse locations to match the unblown fuse locations of the equivalent programmed PAL. The end result is a custom logic device that does not require programming by the customer.

HAL USER BENEFITS

Short Leadtime

HALs offer shorter leadtimes as compared with semicustom devices such as standard cell and gate array devices because the metallization photomasks are automatically generated from the equivalent PAL logic equations. This gives the design engineer an alternative approach through the use of the equivalent programmed PAL.

Lower Device Cost

HAL device cost can typically be 25% to 30% less on high volume levels when compared to an equivalent PAL.

Improved Testability

HALs allow TI to functionally test to a higher level and provide more specific ac testing because the device function is defined. Improved testability, means a HAL can be considered a true Ship-to-Stock component resulting in additional cost savings because incoming test is now optional for the customer.

Less Power Consumption

HALs consume less power than the equivalent PAL device because power consumption of the programming circuitry has been eliminated.

No Programming-Yield Losses

HALs do not have programming-yield losses because there is no individual programming.

HAL CONVERSION CONSIDERATIONS AND REQUIREMENTS

Remembering that a HAL's logic function is permanent and once fabricated cannot be altered, the following questions should be carefully considered by the design engineer before attempting to convert a PAL design into a HAL:

1. Is the PAL design code proven and not likely to change?
2. What is the total volume requirement?

As a general rule, Texas Instruments will accept orders on HALs if the total volume level for 1 year equals or exceeds 10,000 units per code. In addition, individual shipment quantities must be at least 2,000 units per code. Total volume levels of less than 10,000 units per code usually do not justify the tooling costs involved in generating the final two metallization photomasks. If your total volume level is marginal, please contact your local TI field sales representative for assistance.

HAL is a registered trademark of Monolithic Memories Inc.
PAL is a registered trademark of Monolithic Memories Inc.

INFORMATION REQUIRED BY TI TO START THE HAL DESIGN PROCESS

The information Texas Instruments needs to start a HAL design is fairly minimal and is a direct result of a PAL design. At the end of this document is a copy of the TI HAL Product Specification Form. For the customer's convenience, the HAL Product Specification Form may be removed. Additional copies of the HAL Product Specification Forms can be obtained from the local TI field sales representative. When completed, the form should be turned over to the local TI field sales representative for processing. This form will provide TI with all the information necessary to start the first phase of the HAL design process.

The HAL Product Specification Form is divided into two parts, Part A and Part B. When filled out and completed, Part A will contain general information and Part B will define the actual HAL design. For Part B, printouts of a PAL design generated by ABEL™, CUPL™, or PALASM™, with an equivalent diskette or 800/1600 BPI magnetic tape can be used as a satisfactory replacement for the required information. Additionally, a programmed PAL can also be used as a satisfactory replacement for the information required in Part B.

Once the completed HAL Product Specification Form is recieved, TI will assign a unique "SN" number to the request and then generate a design data base from the information. From this design data base, custom metallization photomasks can be generated. However, before TI actually generates the custom photomasks, an equivalent PAL is programmed from the design data base and returned to the customer for functional verification.

In addition to sending a programmed equivalent PAL, TI will also send a Print Evaluation and Acceptance Form which finalizes product specifications and testing procedures.

Once the signed Print Evaluation and Acceptance Form and the customer's guaranteed purchase order is returned, TI will then generate the custom metallization photomasks.

Texas Instruments will treat all information submitted by the customer as confidential and if required, enter into a Non-Disclosure Agreement.

SWITCHING HAZARD ANALYSIS REPORT

As a service to our customers, TI has a systematic computer simulation program that can analyze any sum-of-product design for potential switching hazards. This program is also capable of generating a hazard-free equivalent circuit if possible. Due to product term limitations, some hazards cannot be eliminated. In these cases, the analysis will identify the hazards and issue a warning.

ABEL is a trademark of Data I/O
CUPL Is a trademark of Assisted Technology, Incorporated
PALASM is a trademark of Monolithic Memories Incorporated

The hazard analysis report is automatically generated from the customer's design data base and a copy is sent to the customer along with the programmed equivalent PAL and Print Evaluation and Acceptance Form.

HAL PRODUCT TESTING

Due to similar architectures, HALs are tested to the same dc and ac test specifications as PALs. However, since the functionality of a HAL is known, a more specific functional and ac test is performed.

Functional test patterns are automatically generated from the customer's design data base. These patterns are then graded for completeness and incorporated in the final test program.

Since HALs are comparable to standard catalog devices, they are tested to the same rigorous process flows. This ensures that when ordering HALs, the customer will recieve the same high quality that they are accustom to when ordering standard catalog devices. Flows typically include 1) 100% functional and parametric dc testing at 25 °C and 80 °C, 2) 100% ac testing at 25 °C guardbanded for 80 °C, and 3) QA sampling for 1) and 2) above. Custom flow or PEP3/PEP4 flows may be accommodated.

TI SUPPORTED HALs

The following list of PALs is presently being supported by HALs. As new PALs are introduced by TI, such as the recently announced 15 ns IMPACT™ PAL, the HAL equivalent devices will be available shortly thereafter.

To obtain the latest list of TI supported HALs, please contact your local TI field sales representative.

SUPPORTED HAL	PAL EQUIVALENT	HAL AVAILABILITY
HAL16L8A	PAL16L8A	NOW
HAL16R4A	PAL16R4A	NOW
HAL16R6A	PAL16R6A	NOW
HAL16R8A	PAL16R8A	NOW
HAL16L8A-2	PAL16L8A-2	NOW
HAL16R4A-2	PAL16R4A-2	NOW
HAL16R6A-2	PAL16R6A-2	NOW
HAL16R8A-2	PAL16R8A-2	NOW
HAL16L8-15	TIBPAL16L8-15	NOW
HAL16R4-15	TIBPAL16R4-15	NOW
HAL16R6-15	TIBPAL16R6-15	NOW
HAL16R8-15	TIBPAL16R8-15	NOW
HAL16L8-25	TIBPAL16L8-25	NOW
HAL16R4-25	TIBPAL16R4-25	NOW
HAL16R6-25	TIBPAL16R6-25	NOW
HAL16R8-25	TIBPAL16R8-25	NOW

IMPACT is a trademark of Texas Instruments Incorporated

HAL PRODUCT SPECIFICATION FORM

Part A — General Information

Company Name: _____

Engineer's Name: _____

Title: _____

Company Address: _____

_____

Phone Number: ( ) _____

Local TI FSE:
(or TI sales office) _____

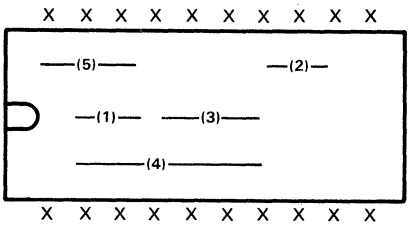
HAL Device Type:
(HAL16L8, HAL16R8, etc.): _____

Volume Level Reqd: _____

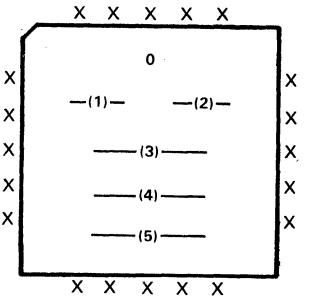
Package Type: ☐ Plastic DIP ☐ Plastic Chip Carrier
Glitch Analysis Reqd.: ☐ Yes ☐ No

HAL Symbolization Format

DIP PACKAGE



CHIP CARRIER PACKAGE



(1) = TI Logo
(2) = Manufacturing Data Code
(3) = TI Custom Part Number (SNXXXXX)
(4) = Customer Part Number (including any revisions)
Ten Characters maximum for DIP package
Eight characters maximum for chip carrier
(5) = Country of Origin

Customer Part Number
[Refer to item (4) above] _____

HAL PRODUCT SPECIFICATION FORM

Part B — HAL Design Requirements

The following information is required by TI to create the HAL design data base. The printouts of a PAL design generated by ABEL, CUPL, or PALASM with an equivalent diskette or 800/1600 BPI magnetic tape is satisfactory replacement for the information required in Part B. A programmed PAL is also a satisfactory replacement for the information required in Part B.

Pin Identification List

Pin 1:		Pin 15:	
Pin 2:		Pin 16:	
Pin 3:		Pin 17:	
Pin 4:		Pin 18:	
Pin 5:		Pin 19:	
Pin 6:		Pin 20:	
Pin 7:		Pin 21:	
Pin 8:		Pin 22:	
Pin 9:		Pin 23:	
Pin 10:		Pin 24:	
Pin 11:		Pin 25:	
Pin 12:		Pin 26:	
Pin 13:		Pin 27:	
Pin 14:		Pin 28:	

Programming Equations:

A Designer's Guide to the TIBPSG507

Robert K. Breuninger and Loren E. Schiele
with Contributions by
Joshua K. Peprah

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Contents

Title	*Page*
INTRODUCTION	3-37
FUNCTIONAL DESCRIPTION	3-37
THEORY OF OPERATION	3-37
Example 1: Waveform Generator	3-39
Example 2: Refresh Timer	3-42
Example 3: Dynamic Memory Timing Controller	3-45
DESIGNER NOTES	3-51
Obtaining Maximum Counter Performance	3-51
Expanding the 6-Bit Counter	3-51
Software Support	3-51

Appendixes

A	ABEL Files	3-57
B	CUPL Files	3-67
C	'PSG507 Fuse Numbers	3-79

List of Illustrations

Figure	*Title*	*Page*
1	PSG Architecture	3-38
2	Clock Generator Timing Requirements	3-39
3	SCLR at COUNT 11	3-40
4	Waveform Generator	3-41
5	Refresh Timer Requirements	3-42
6	Expanding to 7-Bit Binary Counter	3-43
7	Refresh Timer	3-44
8	Memory Timing Controller	3-45
9	Flow Chart: Dynamic Memory Timing Controller	3-46
10	Access Cycle	3-47
11	Refresh/Access Grant Cycle	3-48
12	Counter Control Logic	3-49
13	Memory Timing Controller	3-50
14	Registered SCLR Example	3-52
15	Expanding the 9-Bit Counter	3-53
16	Resetting after COUNT 383	3-54
17	Holding the 9-Bit Counter at COUNT 383	3-55

INTRODUCTION

The term PSG stands for Programmable Sequence Generator. The PSG is the newest member of the programmable logic family. It combines the powerful benefits of programmable array logic (PALs) with the specialized world of Field Programmable Logic Sequencers (FPLSs).

Applications such as waveform generators, state machines, timers, and simple logic reduction are all possible with a PSG. By utilizing the built-in binary counter, the PSG is capable of generating complex timing controllers. In short, the PSG offers the system designer an extremely powerful building block.

The purpose of this application report is to describe the functional operation of the PSG507 and demonstrate how it can be applied in real-world applications. Three design examples that highlight the features and flexibility of the PSG will be discussed.

FUNCTIONAL DESCRIPTION

Figure 1 shows the architecture of the PSG507. Major features include 13 inputs, eight programmable registered or nonregistered outputs, eight S/R state registers, and a 6-bit binary counter with control logic. The clock input is fuse-programmable for selection of positive or negative edge triggering.

The binary counter, state registers, and output cells are synchronously clocked by the fuse-programmable clock input. The clock polarity fuse selects either positive or negative edge triggering. Negative edge triggering is selected by blowing the clock polarity fuse. Leaving this fuse intact selects positive edge triggering.

Each output cell on the PSG can be configured for registered or nonregistered operation through the output multiplexer fuse. Nonregistered operation is selected by blowing the output multiplexer fuse. Leaving this fuse intact selects registered operation.

The PSG507 has 13 inputs, each providing a true and complement input to the AND array. Pin 17 functions as either an input and/or an output enable. Blowing the output enable fuse lets pin 17 function as an output enable but does not disconnect pin 17 from the input array. When the output enable fuse is intact, pin 17 functions only as an input with the outputs being permanently enabled.

The 6-bit binary counter is controlled by a synchronous clear and a count/hold function. Each control function has a nonregistered and registered option. When either SCLR0 or SCLR1 is taken active high, the counter resets to zero on the next active clock edge. When either $\overline{\text{CNT}}$/HLD0 or $\overline{\text{CNT}}$/HLD1 is taken active high, the counter is held at the present count and is not allowed to advance on each active clock edge. The SCLR feature overrides the $\overline{\text{CNT}}$/HLD feature when both functions are simultaneously active high. The functional benefit of both these features will be further clarified in the examples shown later in this appliction report.

The eight internal state registers feed back into the AND array. These registers can be used to store input data, to keep track of binary count sequences, or they can be used as output registers when connected to a nonregistered output cell. The state registers differ from the output registers in that they feed back into the input array. They can also be used to override an operating sequence such as demonstrated in the designer notes located at the end of this application report. By using extra state registers, the 6-bit counter can be expanded as shown in the second example. Other uses of the internal state registers will become apparent upon reading the examples shown.

THEORY OF OPERATION

The PSG architecture is capable of operating in many different modes. When comparing the operation of a PSG to a PAL, the outputs in both devices can be configured as an AND/OR function of the inputs. One major difference between a PSG and a PAL is that a programmable OR array is used in the PSG. This allows a selected number of AND terms to be connected to each output as compared to a fixed number of AND terms assigned to each output on a PAL. The programmable OR array is the more efficient in that it lets the user assign the exact number of AND terms to each output as required by the application.

Another major difference between the PAL architecture and that of a PSG is that the output cells on a PSG are not fed back into the input array. Typically, output feedback is used for building a counter or for holding state information. Since the architecture of the PSG already includes state registers and a binary counter, the requirement for output feedback is eliminated in most applications. This is a benefit to the user because valuable output cells and AND terms are not wasted when generating these functions.

When a Field Programmable Logic Sequencer is compared to a PSG, the most obvious difference is the addition of a binary counter. Most state machine designs can be simplified by referencing all or part of each sequence to a binary count. This technique is highlighted in the third example shown in this application note. A comparison will also reveal that the output cells on a PSG can be configured

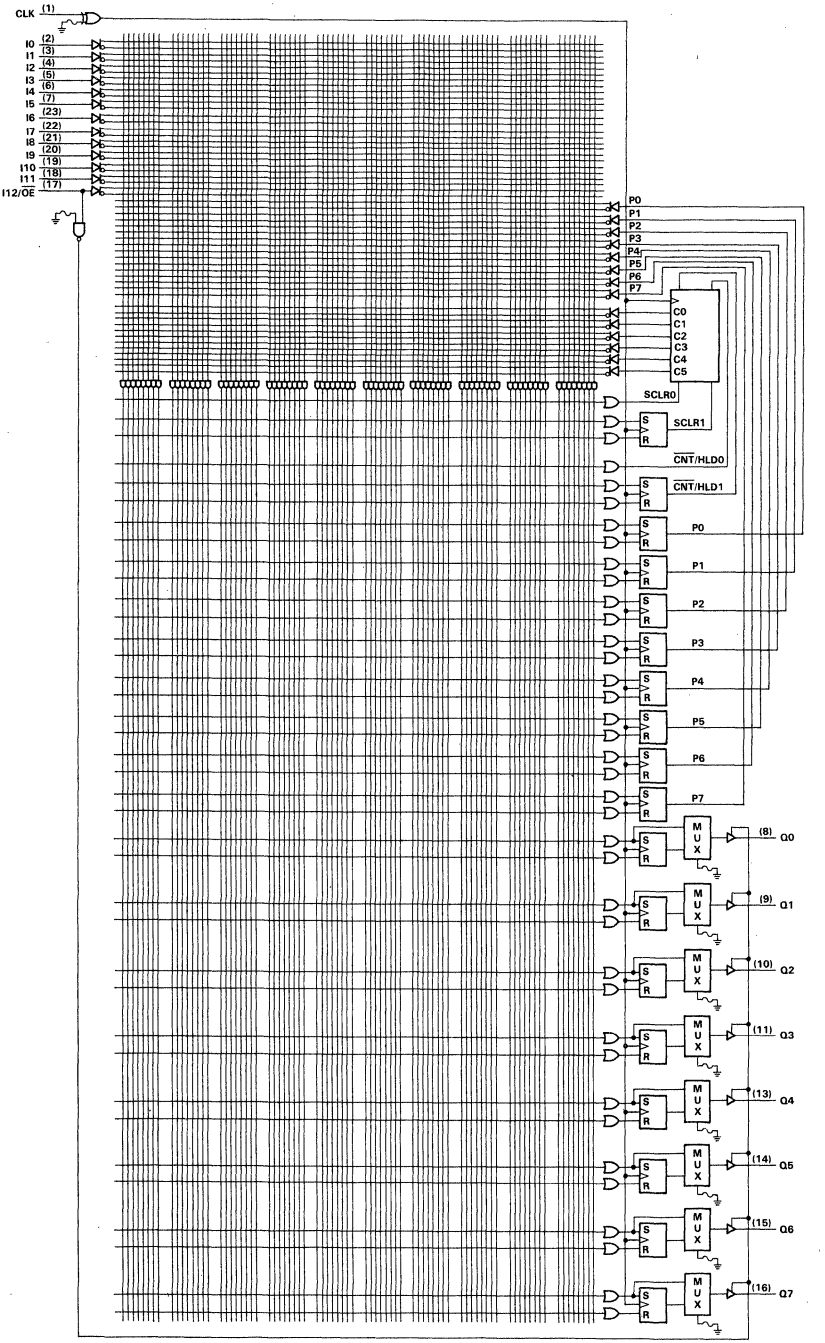


Figure 1. PSG507 Architecture

for nonregistered operation. This permits the outputs to be directly fed from the counter, AND/OR array, or state registers. Example 1 highlights this feature.

In short, the outputs of a PSG can be controlled by any or all of the following conditions:

- Present state of the inputs
- Present state of the binary counter
- Present state of the state holding registers

The key to understanding state machine design when using a PSG is to realize that different states can be assigned for each sequence. In other words, the assigned state determines which sequence is in operation. The length of each sequence is controlled by the SCLR function. Once the count sequence has been programmed to the desired length, each output can be easily decoded from the present state of the binary counter. The user will soon discover that complex state machines are easily developed when using this technique. This technique is demonstrated in Example 3.

Example 1: Waveform Generator

The first example demonstrates a design for a simple clock generator used for driving a microprocessor operating at 5 MHz (required duty cycle of 33.5% high, 66.5% low). In addition to the 5 MHz system clock (SYS CLK), a reference clock (REF CLK) operating at 15 MHz (50% duty cycle) and a peripheral clock (PCLK) operating at 2.5 MHz (50% duty cycle) are required for other timing controllers and peripherals throughout the system. Both clocks must be in close phase with the SYS CLK to guarantee synchronous operation within the system.

The above example demonstrates one of the many uses of the binary counter in the PSG. State registers are not used in this particular application, only the binary counter and three outputs. A 30 MHz clock, typically generated from a crystal, is used for driving the binary counter of the PSG. The three generated clock signals are decoded from the binary count. The unused inputs and outputs are still available for other sequential or combinational applications.

Figure 2 shows the timing diagram for the above application. For reference, a decimal count has been assigned to the master clock (PSG CLK) of the PSG. As shown in the timing diagram, at count 11 (1011_2) the sequence is repeated. By using the SCLR0 function, a logic equation can be defined to reset the counter at count 11. This concept is demonstrated in Figure 3.

With the binary counter programmed to clear at 11, it is a simple matter to decode the outputs from the binary count. With the REF CLK equal to the inverse of binary count zero (C0), REF CLK can be directly generated from the binary counter. A product term is required to connect C0 to the output cell. The output register is bypassed by blowing the output multiplexer fuse. Figure 4 shows how C0 can be connected.

SYS CLK and PCLK are decoded from the present state of the binary counter through the S/R outputs. Since the S/R register holds its present state until changed, product terms have to be used only during output transitions. For example, when the binary counter reaches one, a product term is used to reset the SYS CLK on the next clock transition. Below is a summary of the product terms required to control SYS CLK and PCLK. Note that the output transitions are set up in the previous clock cycle. Also note that only one product term is used regardless of how many output terms switch. This is demonstrated at count 5 and count 11. Figure 4 also shows how SYS CLK and PCLK are connected.

CNT 1:	Reset SYS CLK
CNT 5:	Set SYS CLK, reset PCLK
CNT 7:	Reset SYS CLK
CNT 11:	Set SYS CLK, set PCLK

This simple application demonstrates the basic concept of building a waveform generator using the PSG. This concept will be expanded further in Example 3 when a memory timing controller is developed. The basic rules for building a waveform generator are summarized below.

- Program the counter to reset to zero after the desired count length is reached.
- Generate the logic equations to control the outputs from the present state of the binary counter.

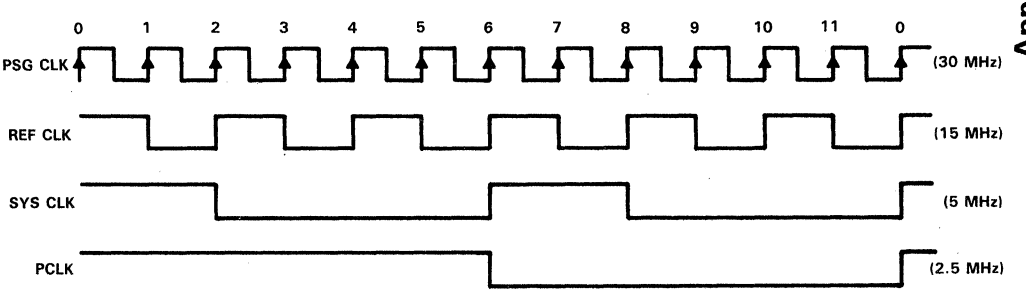


Figure 2. Clock Generator Timing Requirements (Example 1 — Waveform Generator)

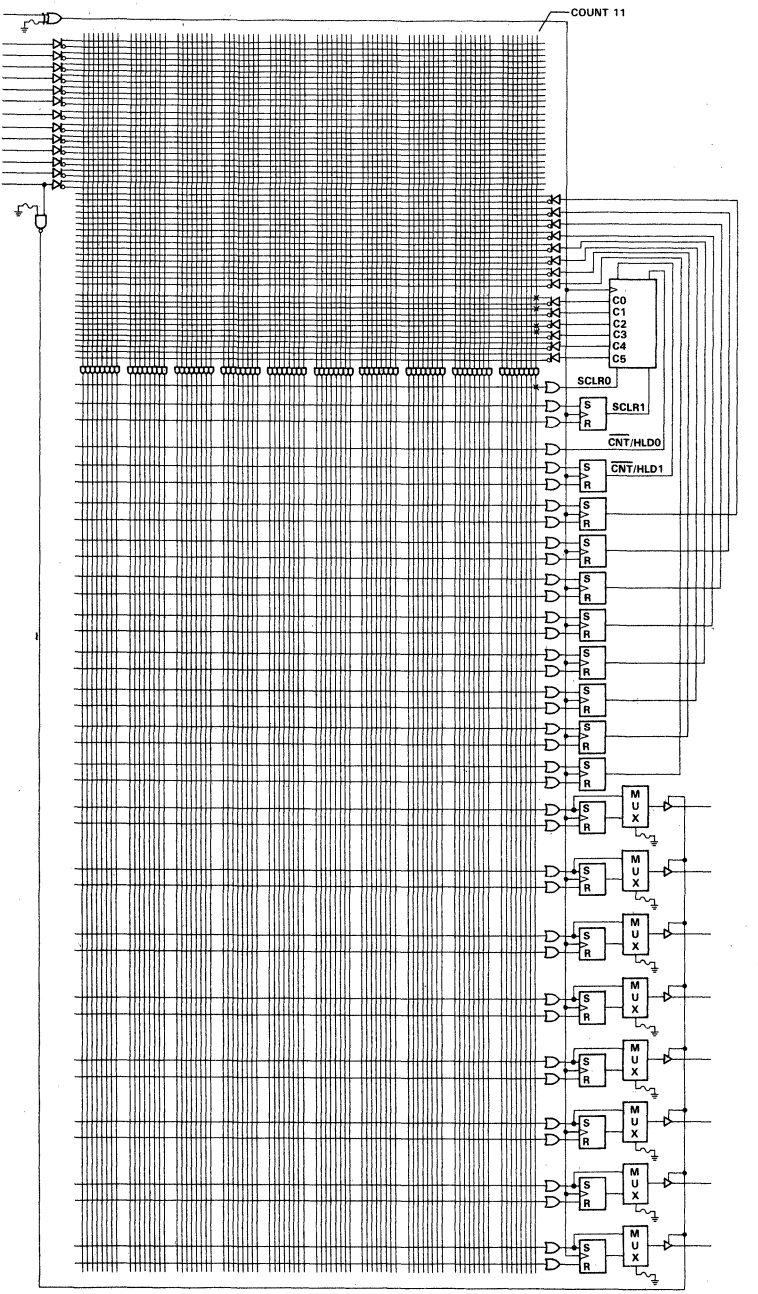


Figure 3. SCLR at COUNT 11
(Example 1 — Waveform Generator)

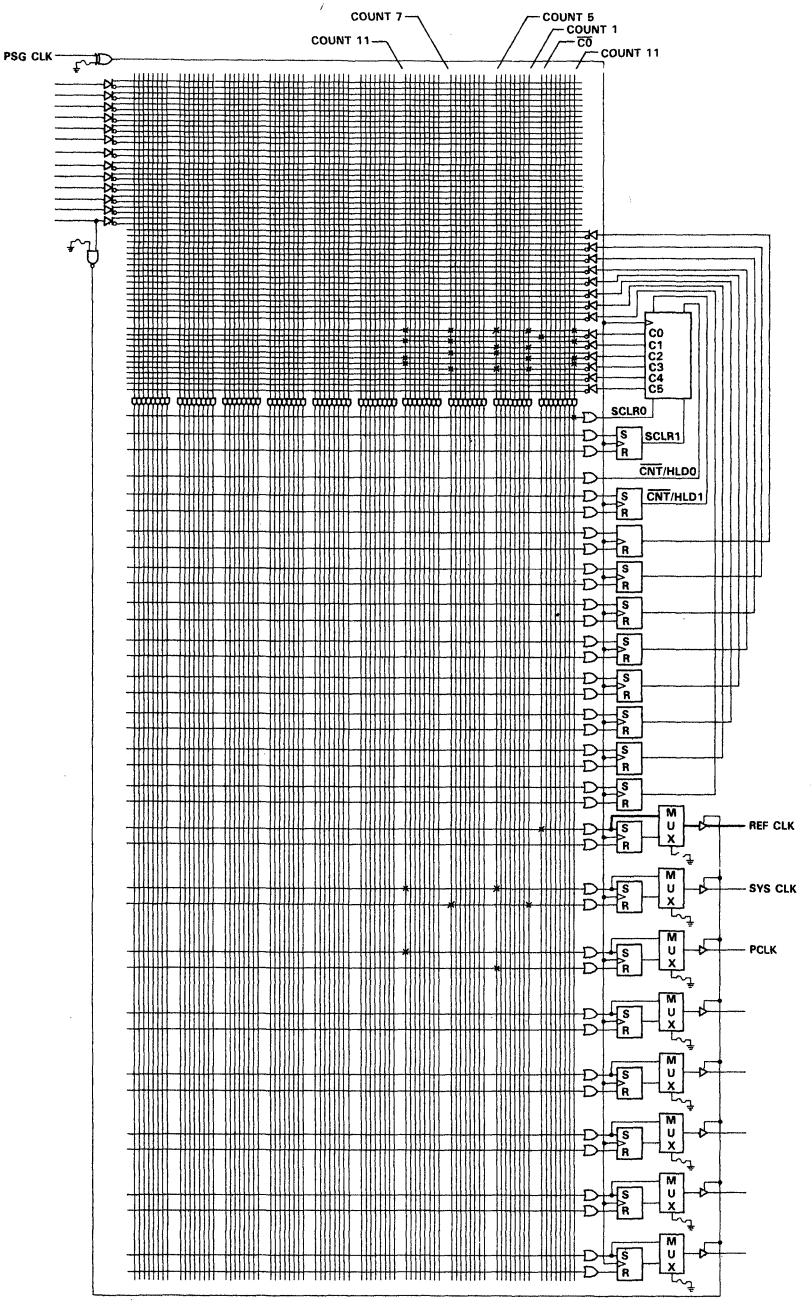


Figure 4. Waveform Generator (Example 1)

Example 2: Refresh Timer

The second example demonstrates a design for a refresh timer used for signaling to a memory controller that it should execute a refresh cycle. As required by the dynamic memory, every row (256 on TMS4256) must be addressed once every 4 ms. One method used to guarantee that this requirement is met is to refresh one row at least once every 15.6 μs. With a 5 MHz system clock, the timer should be set for a division rate of approximately 77 clock cycles. This condition will generate a refresh request every 15.4 μs.

The memory controller executes the refresh request ($\overline{\text{REFREQ}}$) immediately if it is not involved in an access cycle. If the memory controller is executing an access cycle, then the refresh request will not be honored until the access cycle is completed. A refresh complete input (RFC) is required on the refresh timer to acknowledge when the refresh cycle has been completed by the memory controller. It is important that the timer does not stop, even though a refresh complete signal has not been received. This guarantees the refresh requirement is not violated. This also assumes the memory controller will complete the refresh request sometime in the next 77 clock cycles.

Figure 5 shows the timing diagram for the above application. A decimal count has been assigned to the PSG's master clock (PSG CLK) for reference. The counter is held at zero until the reset input is taken inactive low. Once the counter reaches 76 (equal to 77 clock cycles) the $\overline{\text{REFREQ}}$ output is driven active (low). The $\overline{\text{REFREQ}}$ output returns inactive high on the first positive clock edge after RFC goes active high. RFC is the signal from the memory controller that tells the refresh timer when the refresh operation has been completed. The $\overline{\text{REFREQ}}$ output remains low until the RFC signal has been received.

In order to generate a refresh request every 77 clock cycles, a 7-bit counter is required. Since the internal counter of the PSG is 6 bits, one of the state holding registers is required to expand the counter to 7 bits. As shown in Figure 6, only two product terms are required to expand to 7 bits; one product term to set the register when the 6-bit counter reaches its full count (63), and one product term to reset the register after count 76. Since both the binary counter and the added register need to be reset after count 76, a single product line can be used for both. (For additional details on expanding the 6-bit counter of the PSG, see the designer notes at the end of this application report.)

Figure 7 shows the fuse map for the entire refresh timer. The refresh timer is initialized by taking the RESET input high. When RESET is taken high, a single product line is activated and all other product lines are disabled. On the next active clock edge, the binary counter and C6 are cleared and the $\overline{\text{REFREQ}}$ output is set high. The refresh timer will begin counting when RESET returns low. When the 7-bit counter reaches 76, a product line goes active (high) and on the next clock edge forces C6 and the 6-bit counter to zero. Note that the output register holding $\overline{\text{REFREQ}}$ is also reset to zero. The RFC input is connected to a product line which in turn is connected to the set input of the $\overline{\text{REFREQ}}$ output register. On the next active clock edge after RFC is taken high the $\overline{\text{REFREQ}}$ output will return high.

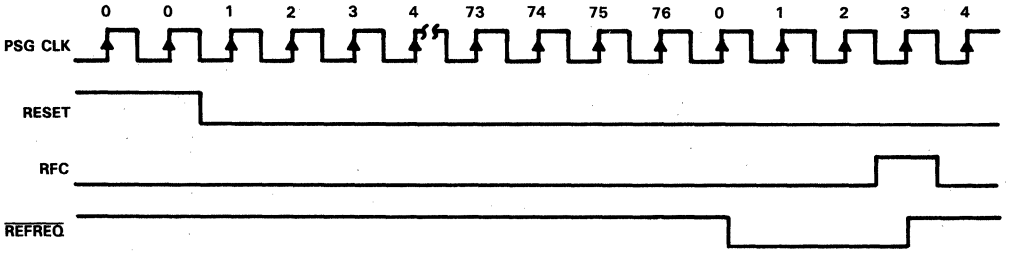


Figure 5. Refresh Timer Requirements (Example 2 — Refresh Timer)

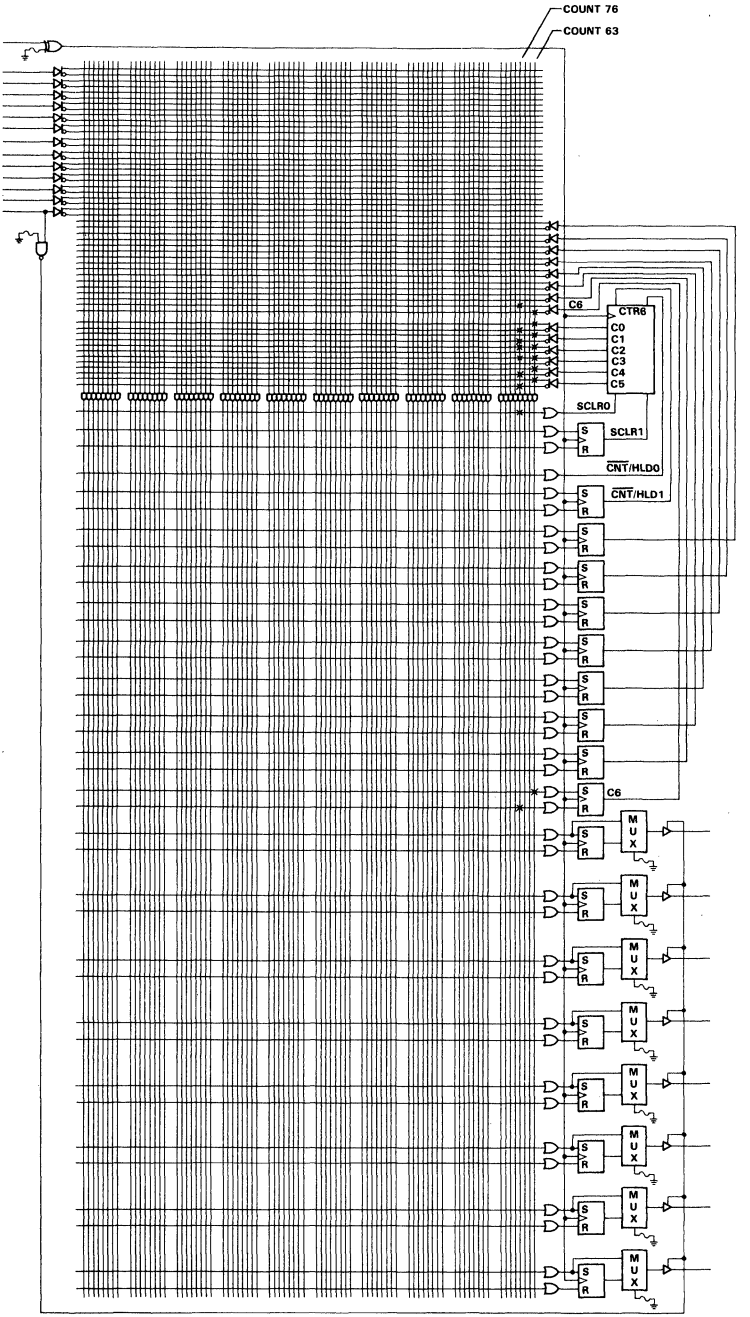


Figure 6. Expanding to 7-Bit Binary Counter (Example 2 — Refresh Timer)

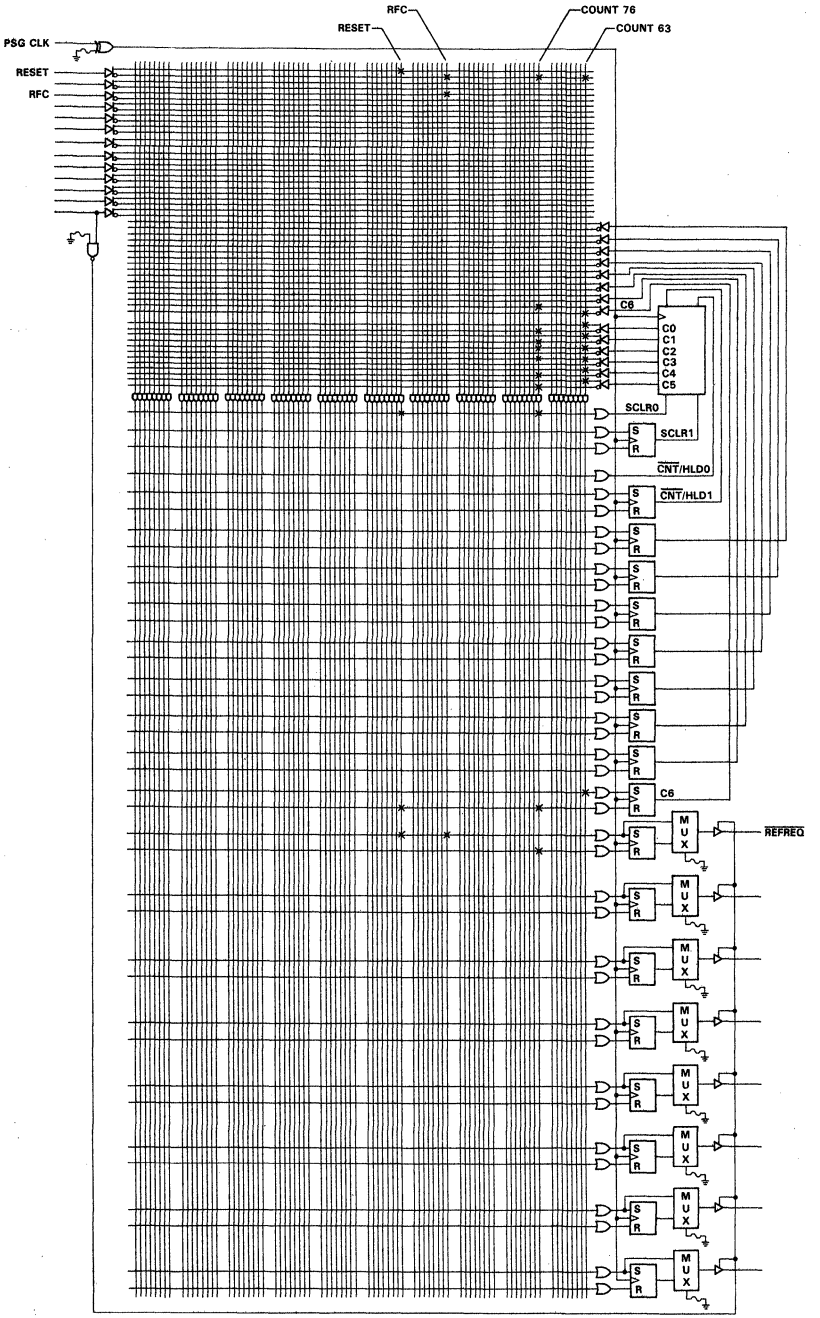


Figure 7. Refresh Timer (Example 2)

Example 3: Dynamic Memory Timing Controller

The third and last example will demonstrate a state machine design using the PSG507. Figure 8 shows the circuit requirement for a memory timing controller used for interfacing an Intel 8086 to an 'ALS2967 dynamic memory controller. Note that the clock generator and refresh timer, developed in Examples 1 and 2, can be used in this circuit.

The dynamic memory timing controller generates the control signals ($\overline{RAS}$, $\overline{CAS}$, MSEL, etc.) needed for accessing and refreshing the dynamic memory. The memory timing controller must also be capable of arbitrating between refresh and access cycles. In other words, if a refresh request ($\overline{REFREQ}$) occurs while the timing controller is performing an access cycle, the controller must finish the access cycle before granting the refresh request. Likewise, if an access cycle is requested during a refresh cycle, the controller must hold the processor while completing the refresh cycle. After the refresh cycle has been completed, the access cycle can be performed.

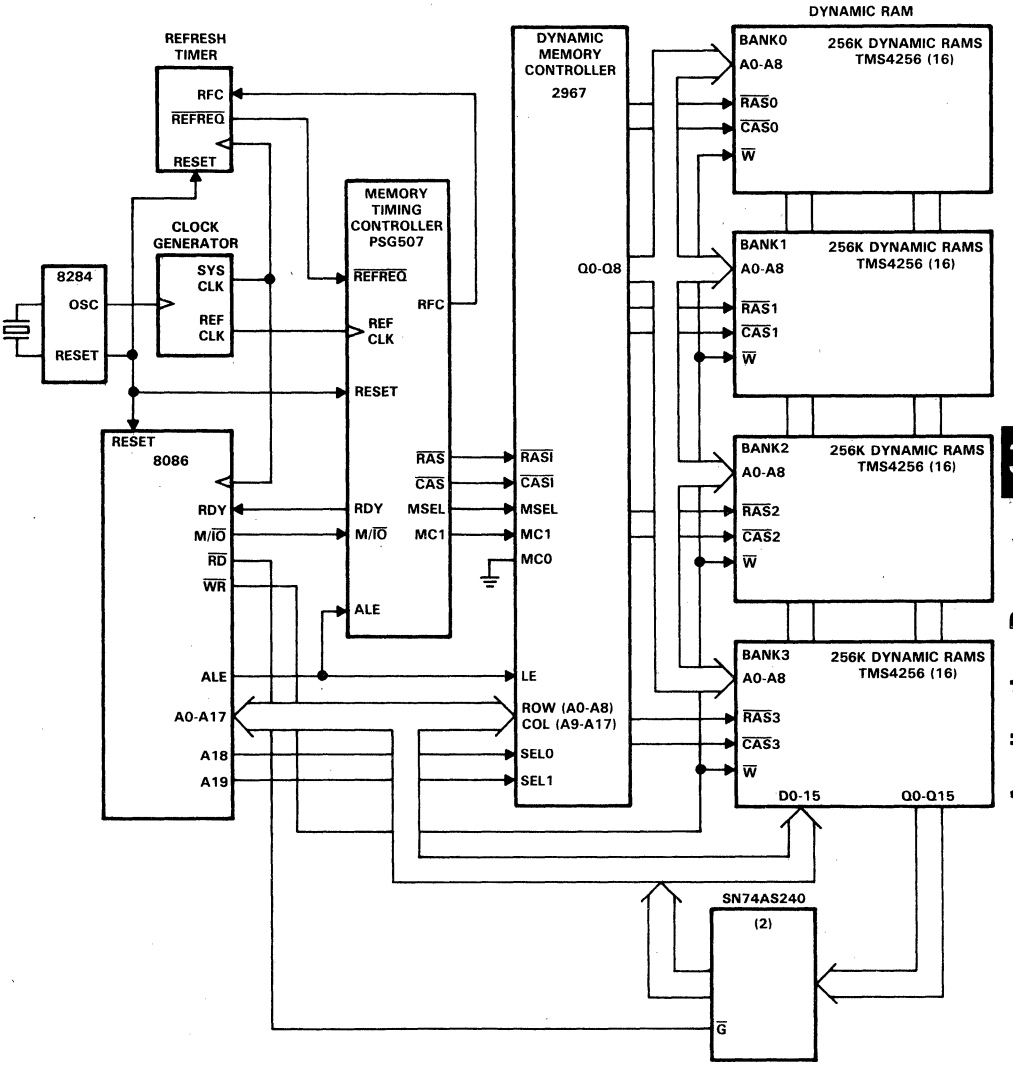


Figure 8. Memory Timing Controller (Example 3)

Figure 9 shows a detailed flow chart for the intended application. Note that two sequences are executed and three states are used. State 0 (ST0) provides an initalization and holding state, while state 1 (ST1) is assigned to the access sequence. The access sequence consists of 10 clock cycles as shown in Figure 10. State 2 (ST2) is assigned to the refresh/access grant sequence (Figure 11). This particular sequence takes 20 clock cycles, with a logical decision being made between count 9 and count 10. If at count 9 RDY is low, the counter will continue on and execute the access grant sequence. If RDY is high, the controller will clear the counter and return to state 0.

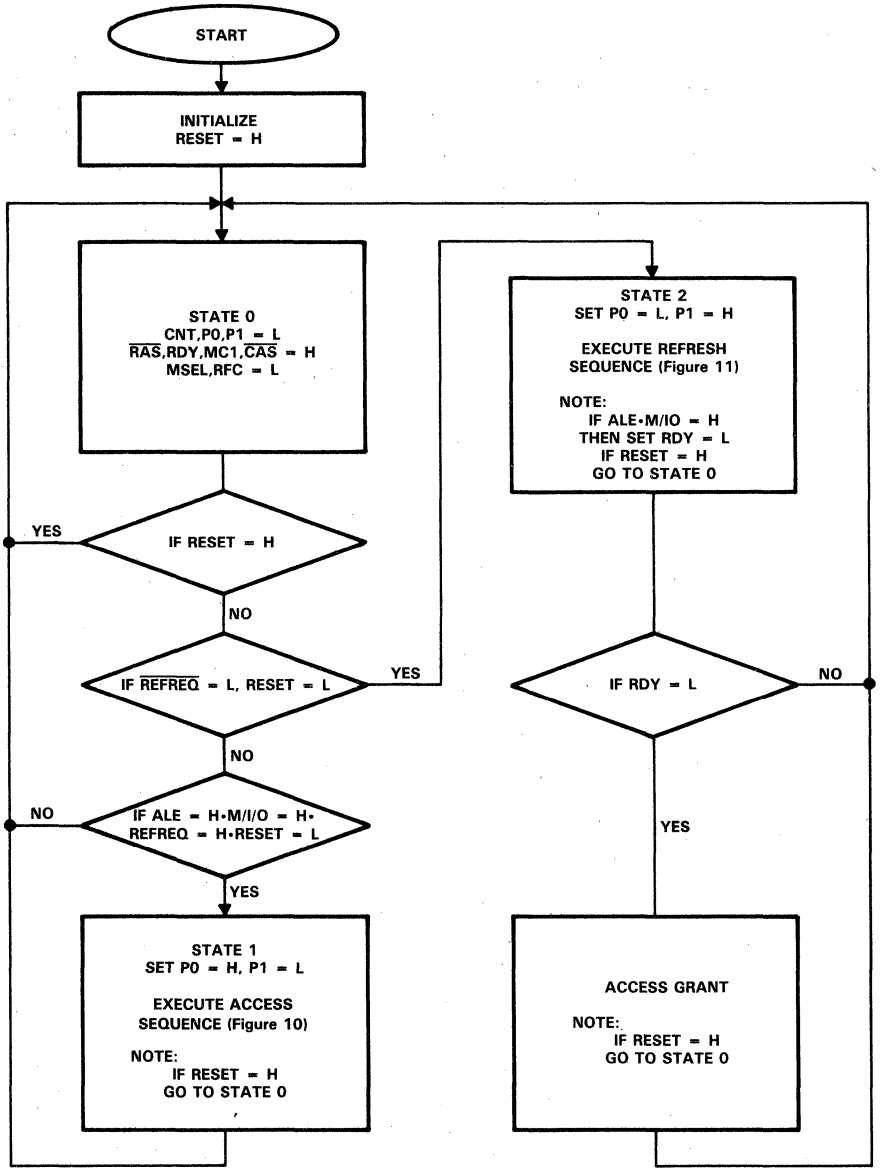


Figure 9. Flow Chart: Dynamic Memory Timing Controller

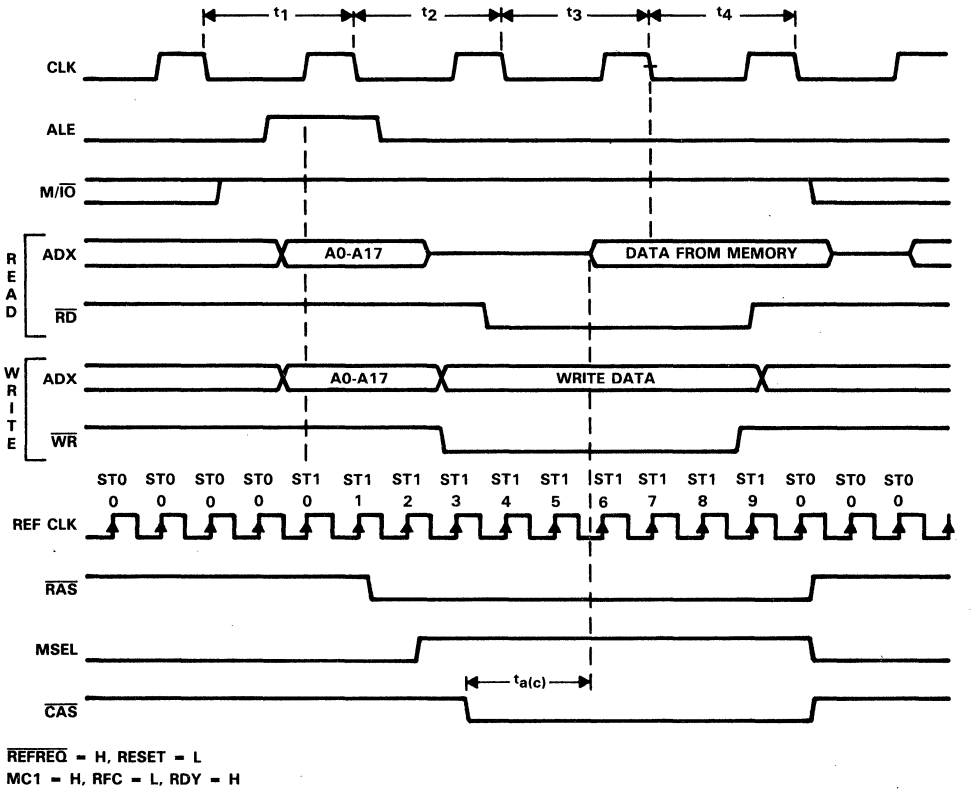


Figure 10. Access Cycle

Developing the logic equations for this application becomes a simple matter when referencing the sequences to a decimal count (Figures 10 and 11). It is important to realize that each sequence has been referenced to a state. This allows the same binary counter to be used for each sequence, even though each sequence is of a different length.

The first step in implementing the above application is to define the logic equations which will make the binary counter perform as described in the flow chart of Figure 9. As will become evident, these equations fall directly from the flow chart. After the counter has been made to perform as described, the outputs can be easily decoded from the binary count and the present state of the state holding registers.

Figure 12 shows a fuse map for step 1 as described above. Initalization is performed by taking the reset input high. When this condition occurs, all product lines except the reset product line are forced inactive. When the reset product line is active, the counter and state holding registers (P0 and P1) are reset to zero on the first active clock edge. The $\overline{CNT}$/HLD1 register is set high, which places the counter in the hold mode. The RDY, MC1, $\overline{RAS}$, and $\overline{CAS}$ outputs are driven high on the same active clock edge. Since the RDY output does not feed back to the AND array, a buried state register, BRDY, is used to monitor the RDY output and is also set high. MSEL and RFC are driven low.

Controlling the binary counter is a simple matter and normally takes only a couple of logic equations. For each sequence, a start and stop condition must be defined. In the case of ST1, when the condition RESET = L, ALE = H, M/$\overline{IO}$ = H, $\overline{REFREQ}$ = H, P0 = L, and P1 = L occurs, ST0 (P1 = L, P0 = L) changes to ST1 (P1 = L, P0 = H), and the $\overline{CNT}$/HLD1 register is driven low to let the counter advance on the next active clock edge. When the counter reaches nine, ST1 returns to ST0 and the counter is cleared and put back into the hold condition.

In the case of ST2, when the condition RESET = L, $\overline{REFREQ}$ = L, P0 = L, and P1 = L occurs, ST0 changes to ST2 (P1 = H, P0 = L) and the $\overline{CNT}$/HLD1 register is driven low to let the counter advance on the next active clock

edge. As shown in the flow chart, if M/IO and ALE go high while in state 2, RDY and BRDY will be reset low on the next active clock edge. When the counter reaches nine, if RDY (BRDY) is high the state registers are returned to ST0 and the counter is cleared and placed back into the hold condition. If RDY (BRDY) is low, the counter advances on until it reaches 19. ST2 then returns to ST0 with the counter being cleared and placed back into the hold condition.

With the binary counter programmed to execute the flow chart in Figure 9, it is now a simple matter of decoding the outputs to perform as required in Figures 10 and 11. This is the same technique used in Example 1, except now a state has been assigned to each sequence. Below is a summary of the switching requirements for both the access (ST1) and the refresh sequence (ST2).

Access Sequence		Refresh Sequence	
ST1 CNT 0:	Reset $\overline{RAS}$	ST2 CNT 0:	Reset MC1
ST1 CNT 1:	Set MSEL	ST2 CNT 1:	Set RFC, Reset $\overline{RAS}$
ST1 CNT 2:	Reset $\overline{CAS}$	ST2 CNT 5:	Reset RFC
ST1 CNT 9:	Set $\overline{RAS}$, Reset MSEL, Set $\overline{CAS}$	ST2 CNT 6:	Set $\overline{RAS}$
		ST2 CNT 7:	Set MC1
		ST2 CNT 10:	Reset $\overline{RAS}$
		ST2 CNT 11:	Set MSEL
		ST2 CNT 12:	Reset $\overline{CAS}$, Set RDY, Set BRDY
		ST2 CNT 19:	Set $\overline{RAS}$, Reset MSEL, Set $\overline{CAS}$

Note that the transition changes are set up in the previous clock cycle, just as in Example 1. Figure 13 shows a complete fuse map for the memory controller.

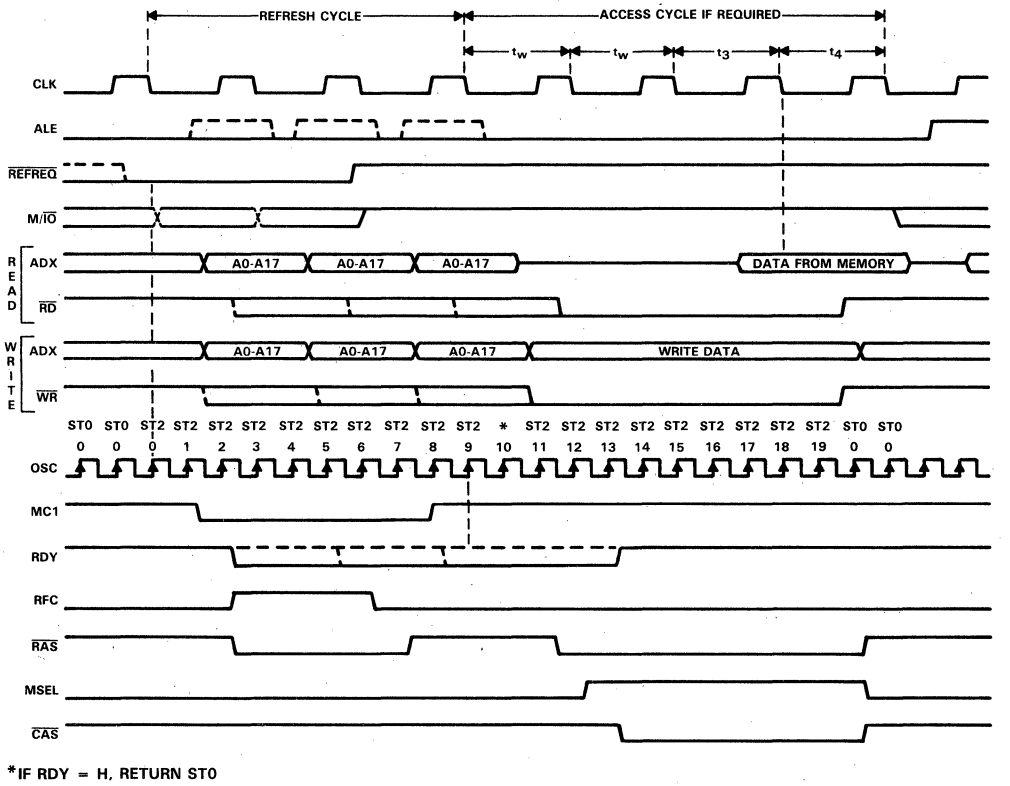


Figure 11. Refresh/Access Grant Cycle

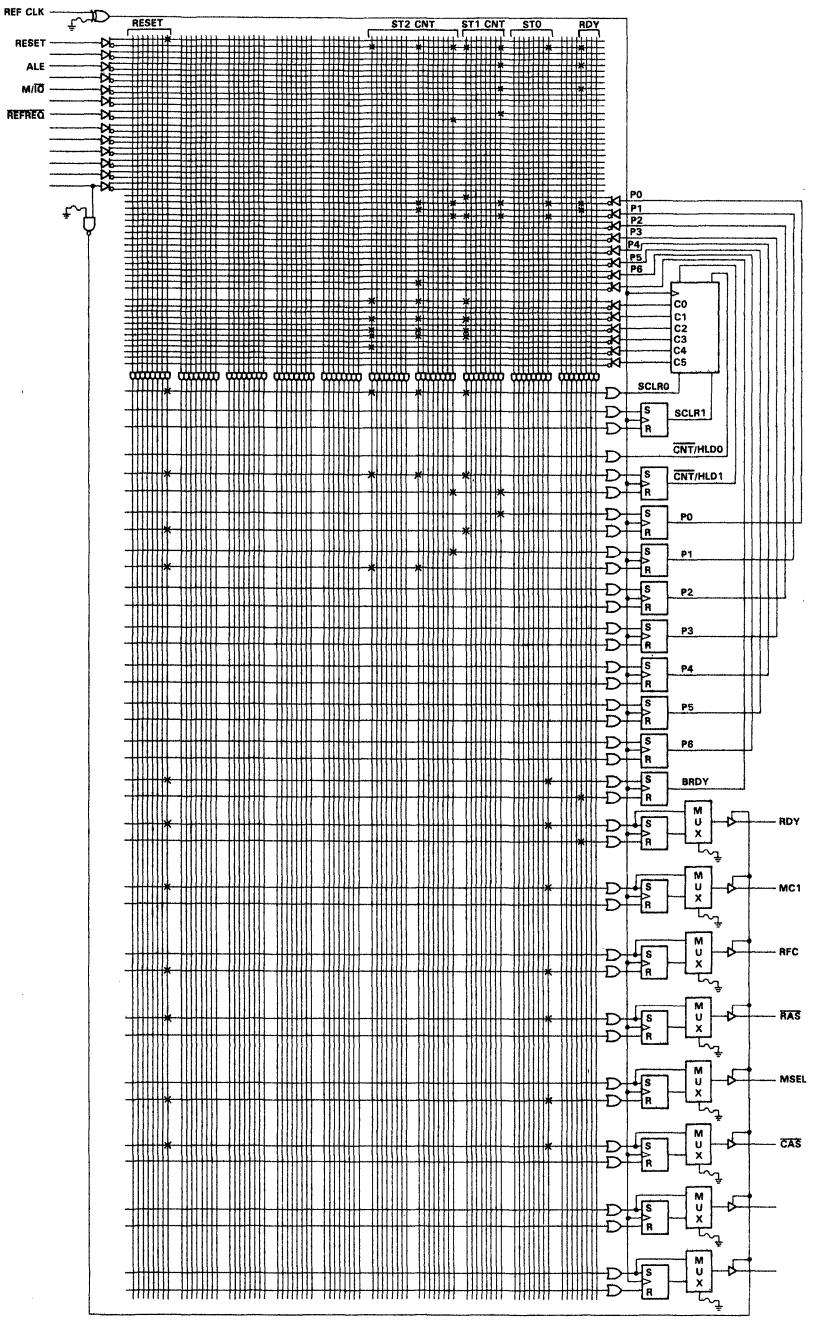


Figure 12. Counter Control Logic
(Example 3 — Dynamic Memory Timing Controller)

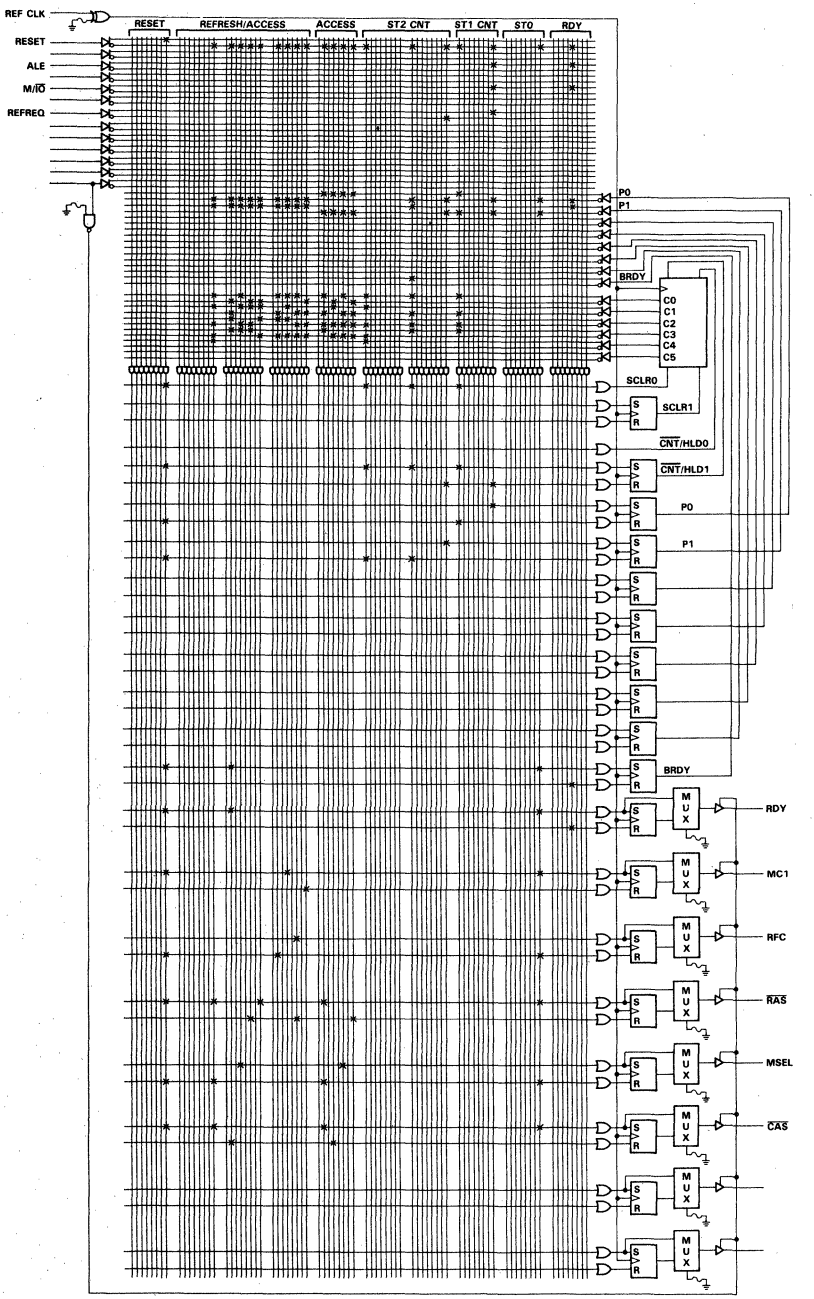


Figure 13. Memory Timing Controller (Example 3)

DESIGNER NOTES

Obtaining Maximum Counter Performance

As with any programmable logic device, there are usually several different methods for implementing any one application. In some cases, device performance is affected. On the PSG, maximum counter frequency is affected by how the designer controls the 6-bit counter.

For example, in the waveform generator example shown at the beginning of this application note, the counter was reset to zero after reaching count 11 by using the nonregistered SCLR0 function. By using the registered SCLR1 function, a higher operating frequency is obtainable.

This method requires an additional "AND" term as shown in Figure 14, but does provide maximum performance. Note that during the 10th clock cycle the set input on the SCLR1 register is high. On the next active clock edge, the counter advances to 11 and the SCLR1 register is set high. This causes the counter to be reset on the next active clock edge. At the same time, the SCLR1 register is reset low to allow the counter to advance past zero.

In effect, the setup time requirement for SCLR1 is performed in the previous clock cycle. When using the SCLR0 method, the setup time must be added to the f_{max} equation. This results in a lower f_{max}. The same tradeoffs apply with the $\overline{CNT}$/HLD function. The PSG507 data sheet specifies f_{max} for both methods.

Expanding the 6-Bit Counter

In Example 2, the six bit counter had to be expanded to 7 bits. This was accomplished by adding one of the state registers to the most significant bit of the counter. It should be noted that the synchronous clear and count hold functions must be controlled through the set and reset inputs of the added bits. The designer must be aware of certain limitations when trying to perform this function. Figure 15 shows three additional bits being added to the 6-bit counter. Note that every bit added requires two additional "AND" terms.

A problem can arise on certain counts when trying to generate a synchronous clear before reaching the full binary count (all outputs high). The designer must ensure that both S and R are not high simultaneously. For example, let's say we want the 9-bit counter to return to zero at count 383 (101111111_2). At count 383, the S/R register used for C7 is being told to set. Therefore, any reset command would result in both S and R being high simultaneously.

This problem, only seen on a few data words, can be solved by using another state register to control the counter reset. This method is similar to that used above to obtain maximum operating frequency. Figure 16 shows the 9-bit counter returning to zero after count 383. Notice that at count 382 the extra S/R register is being told to reset on the next active clock edge. At count 383 the six product lines controlling C6, C7, and C8 are disabled by the feedback from the extra register, in particular the S input on C7. At count 383, the 9-bit counter will return to zero and the extra register is set high.

An extra register may also be needed to achieve the count/hold function when using an expanded counter. During certain counts the added bits will change state, even though the 6-bit counter is programmed to hold. For example, let's say we want the 9-bit counter to hold at count 383. Even though the 6-bit counter can be held at 111111, C6 and C7 will advance on the next active clock edge. In order to hold C6 and C7 where they are, an extra register is used to disable the product lines responsible for the transition from count 383 to 384. Since the counter is on hold, the extra hold register can only be reset from an input pin or a state register(s) transition (not on the next count). In this example, an input pin is used to reset the extra register and the $\overline{CNT}$/HOLD register. When the CONTINUE input is taken low, the counter will continue to advance. The system must guarantee that the continue input will not be low during count 382 to avoid the indeterminant set = H, reset = H state. Figure 17 shows this 9-bit counter.

It is also important to note that when using extra registers a reset input may be necessary to set the extra registers high after powerup, since all S/R registers power-up clear. This requirement would not be necessary if the phase of the extra register was reversed. This is easily accomplished by using the inverted feedback from the extra register. However, it is good state machine design practice to include a reset input that forces all S/R registers to a known state.

Software Support

The PSG507 is supported by two software packages; CUPL, which was created by and is supported by Assisted Technologies, a division of Personal CAD Systems Incorporated, and ABEL, which was created by and is supported by FutureNet, a division of Data I/O Corporation. Each of these software packages can be used to reduce equations and to generate a fuse map necessary to program the PSG507. Appendices A and B show the ABEL and CUPL files for Examples 1, 2, and 3. In addition, a PSG507 template is shown for each software package. These templates provide software information that will make it easier for the designer to create the source files.

Test vectors are included with the ABEL and CUPL source files so software simulation can be performed on the computer. If the proper instruction is provided, the software will attach the test vectors to the end of the fuse map. This allows programming equipment to run a functional test on each device immediately after programming.

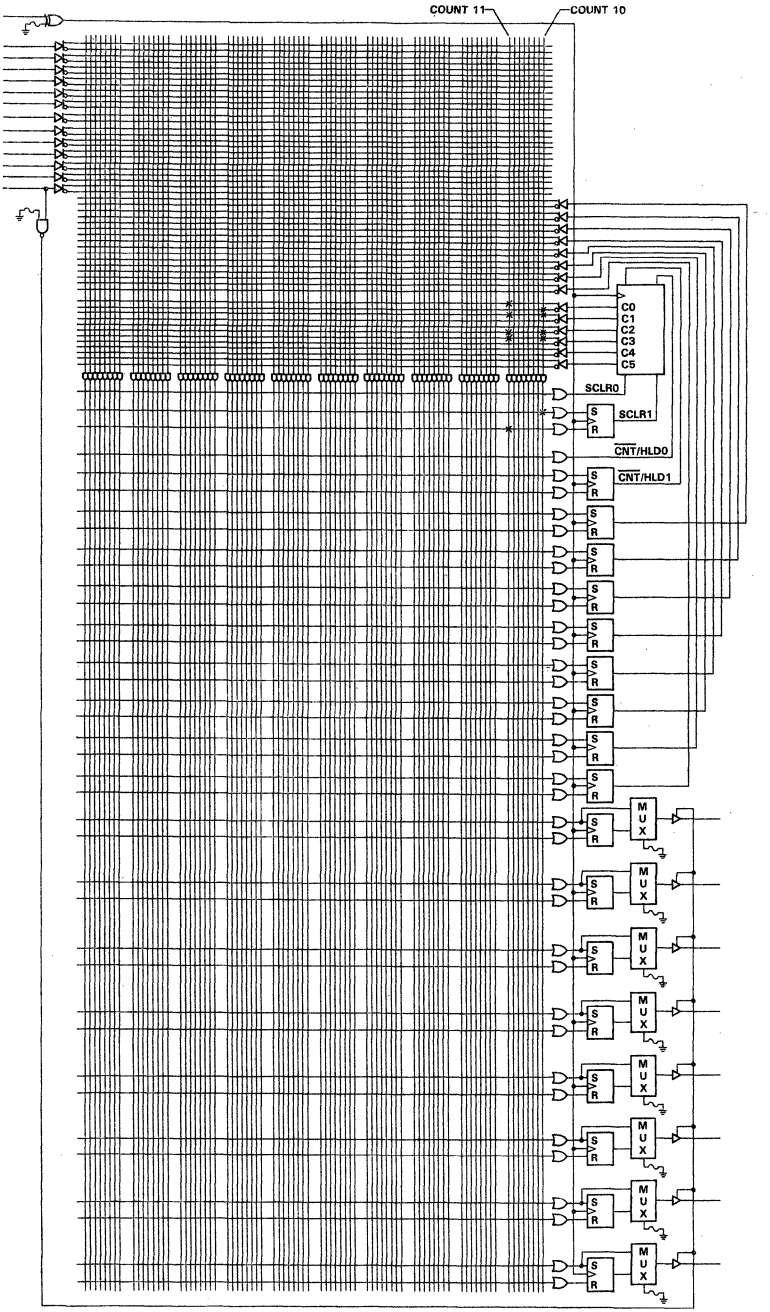


Figure 14. Registered $\overline{\text{SCLR}}$ Example (Designer Notes)

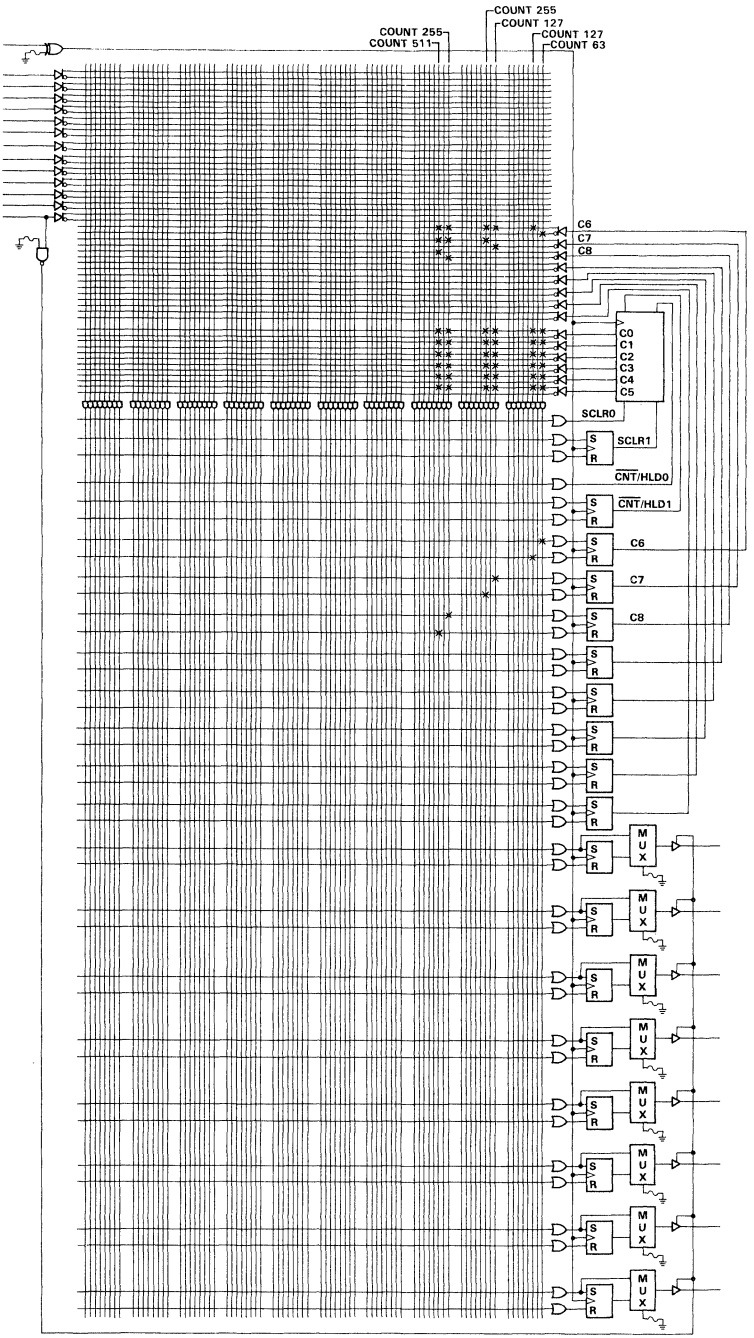


Figure 15. Expanding to 9-Bit Counter

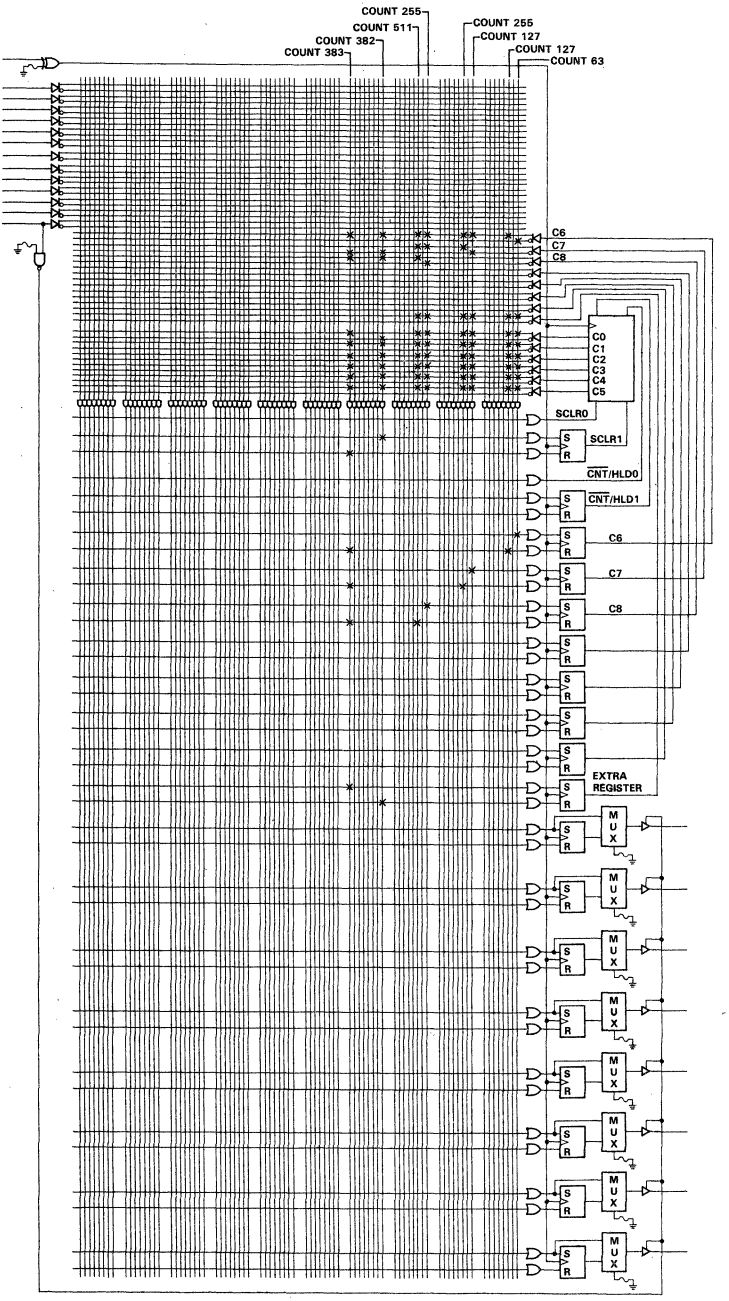


Figure 16. Resetting after Count 383 (Expanding the 6-Bit Counter)

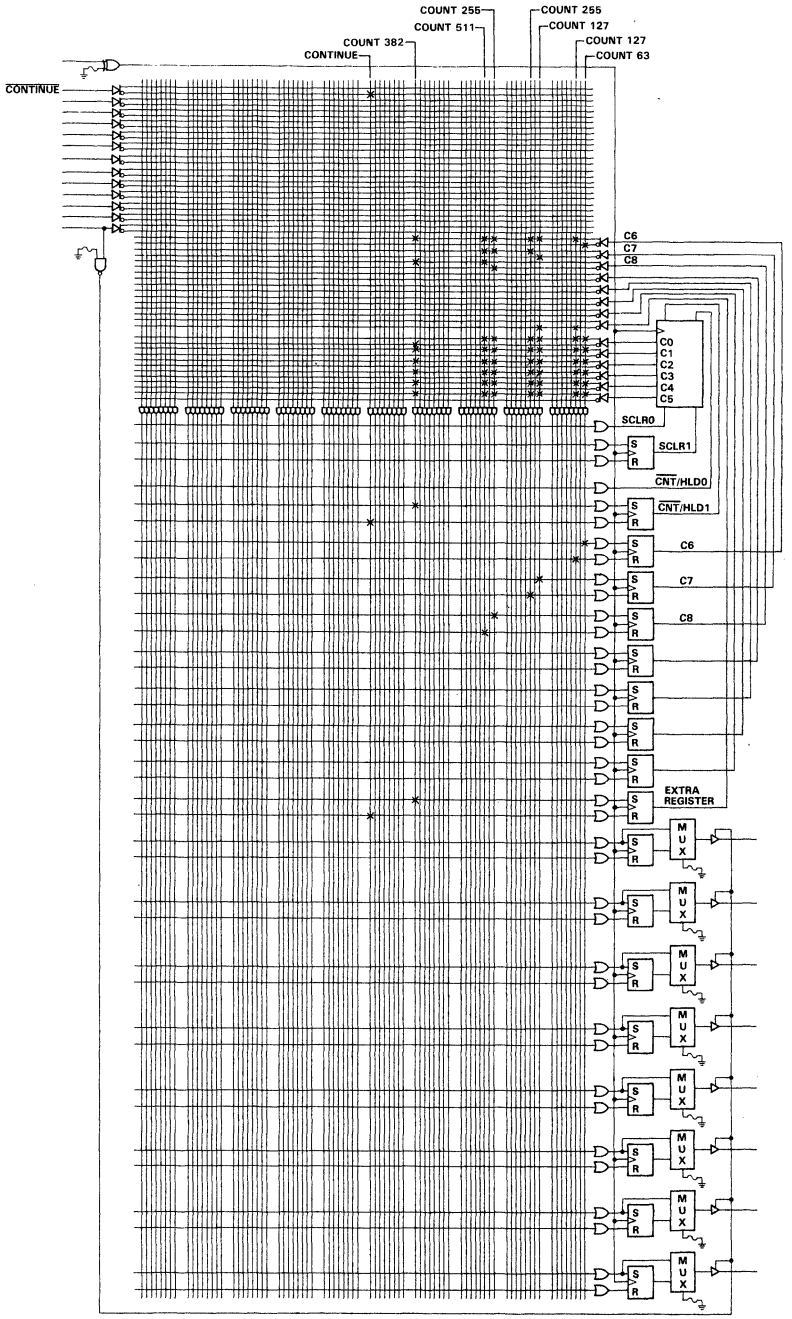


Figure 17. Holding the 9-Bit Counter at Count 383 (Expanding the 6-Bit Counter)

```
" ABEL (tm) TEMPLATE FOR THE TI PSG507                                    "
"                                                                         "
" This file provides the PSG507 designer quick access to the information  "
" needed to write an ABEL source file. To use this file as a template, make "
" a copy and delete this box from your new file.                          "
"                                                                         "
" NODES: The PSG counter bits, counter control bits and state register bits "
"        are accessed through the use of nodes.  Any valid identifier can "
"        be used for node names.  The node numbers are specific and must be "
"        used as shown below. Nodes that will not be used do not have to be "
"        declared.                                                        "
"                                                                         "
" OUTPUT STRUCTURE:  The default output stucture is registered.  The output "
"                    type is determined by usage, i.e. Q0 := (COUNT==7);  "
"                    will cause Q0 to remain registered and Q0 = (COUNT==7);"
"                    will cause Q0 to be combinatorial.  When an output is "
"                    used as nonregistered, ABEL will automatically program "
"                    the associated reset fuses as required in the PSG507 "
"                    data sheet.  Unused product terms can be left        "
"                    connected to either side of an output register.      "
"                                                                         "
" CLOCK POLARITY:  The default clock polarity is active on the rising edge. "
"                  The statement fuses [7360]=1; can be used to blow the  "
"                  clock polarity fuse so that the clock will be active on "
"                  the falling edge (fuses [7360]=0; is the default). 7360 "
"                  is the clock polarity fuse number.                     "
"                                                                         "
" OUTPUT ENABLE:  The output enable fuse is blown by using the equation   "
"                 enable output = !en; where output is a defined output pin "
"                 or set of outputs and en is assigned to pin 17.  The    "
"                 default  condition is permantly enabled with pin 17 an  "
"                 input.  If desired the default condition can be specified "
"                 with enable output = en;  This fuse can also be blown by "
"                 the statement: fuses [7361]=1;                          "
"                                                                         "
" SET NOTATION:  Set notation is often used to represent control, buried   "
"                state, and output registers. This is done to simplify    "
"                equations.  The sets shown below (Q0_ = [Q0, Q0_r];) are "
"                in the form; New register name = [set input, reset input]. "
"                Note that the ouput register pin name specifies the set  "
"                input.                                                   "
"                                                                         "
"                The sets 'high' and 'low' (high=[1,0]; and low=[0,1];) can "
"                be used to set or reset the S/R registers.   Example:    "
"                Q1_ := high & I0; will cause pin 9 to go high on the next "
"                clock edge if input pin 7 is high.                       "
"                                                                         "
" SIMULATION:    During simulation of a PSG507 design the ABEL 2.10a      "
"                simulator will advance the counter on each clock depending "
"                on the state of the counter hold and clear functions.    "
"                If counter bits are included on the output side of a test "
"                vector simulation errors will occur. Counter bits included "
"                on the input side of the test vectors are ignored.  The  "
"                powerup condition (counter bits and all registers low) is "
"                recognized by the simulator.                             "
"                                                                         "
"  ABEL is a trademark of Data I/O Corporation                            "
"                                                                         "
```

```
Module PSGFILE
title 'ABEL TEMPLATE FILE FOR THE TEXAS INSTRUMENTS PSG507'

       PSG device 'F507';

" Input pin assignments
CLK      pin   1;                          " comments
I0       pin   7;                          "
I1       pin   6;                          "
I2       pin   5;                          "
I3       pin   4;                          "
I4       pin   3;                          "
I5       pin   2;                          "
I6       pin  23;                          "
I7       pin  22;                          "
I8       pin  21;                          "
I9       pin  20;                          "
I10      pin  19;                          "
I11      pin  18;                          "
I12_OE   pin  17;                          "

" Output pin and node assignments
Q0       pin   8;  Q0_r    node 47;        " comments
Q1       pin   9;  Q1_r    node 48;        "
Q2       pin  10;  Q2_r    node 49;        "
Q3       pin  11;  Q3_r    node 50;        "
Q4       pin  13;  Q4_r    node 51;        "
Q5       pin  14;  Q5_r    node 52;        "
Q6       pin  15;  Q6_r    node 53;        "
Q7       pin  16;  Q7_r    node 54;        "

" Internal counter bits & control - node declarations
C0,C1,C2,C3,C4,C5  node 55,56,57,58,59,60;

SCLR0    node 25;                          " nonregistered counter clear con-
trol
SCLR1    node 26;  SCLR1_r    node 27;     " registered counter clear control
CNTHOLD0 node 28;                          " nonregistered count/hold control
CNTHOLD1 node 29;  CNTHOLD1_r node 30;     " registered count/hold control

" Buried state registers - node declarations
P0       node 31;  P0_r       node 39;     " buried state register
P1       node 32;  P1_r       node 40;     " buried state register
P2       node 33;  P2_r       node 41;     " buried state register
P3       node 34;  P3_r       node 42;     " buried state register
P4       node 35;  P4_r       node 43;     " buried state register
P5       node 36;  P5_r       node 44;     " buried state register
P6       node 37;  P6_r       node 45;     " buried state register
P7       node 38;  P7_r       node 46;     " buried state register

@page
```

```
Q0_ = [Q0, Q0_r];
Q1_ = [Q1, Q1_r];
Q2_ = [Q2, Q2_r];
Q3_ = [Q3, Q3_r];
Q4_ = [Q4, Q4_r];
Q5_ = [Q5, Q5_r];
Q6_ = [Q6, Q6_r];
Q7_ = [Q7, Q7_r];
SCLR1_     = [SCLR1, SCLR1_r];
CNTHOLD1_ = [CNTHOLD1, CNTHOLD1_r];

" Intermediate declarations for simplification
INPUTS     = [I12_OE,I11,I10,I9,I8,I7,I6,I5,I4,I3,I2,I1,I0];
OUTPUTS    = [Q7,Q6,Q5,Q4,Q3,Q2,Q1,Q0];
STATE_     = [P7,P6,P5,P4,P3,P2,P1,P0];
COUNT      = [C5,C4,C3,C2,C1,C0];
H,L,X,Z    = 1, 0, .X.,.Z.;
high       = [ 1,  0];
low        = [ 0,  1];
ck         = .C.;    " Use .K. for falling edge, .C. for rising edge clock.


" DEVICE FUNCTION can be specified using state diagrams, equations,
" and truth tables.


test_vectors ' optional header
([CLK, INPUTS ] -> [OUTPUTS, STATE_])
 [ ck,         ] -> [       ,       ];   "count xx
 [ ck,         ] -> [       ,       ];   "count xx
 [ ck,         ] -> [       ,       ];   "count xx
end PSGFILE
```

```
Module PSG_EX1
title 'ABEL EXAMPLE #1 (Waveform Generator) for the
PSG507 DESIGNERS GUIDE, Texas Instruments,  August 26, 1987'

        PSG1 device 'F507';

" Input pin assignments
PSG_CLK  pin   1;

" Output pin and node assignments
REF_CLK  pin   8;
SYS_CLK  pin   9;    SYS_CLK_r  node 48;
PCLK     pin  10;    PCLK_r     node 49;

REF_CLK IsType 'com';    " REF_CLK is combinational

" Internal counter bits & control - node declarations
C0      node 55;     C1     node 56;
C2      node 57;     C3     node 58;
SCLR0   node 25;

" Intermediate declarations for simplification
COUNT    = [C3,C2,C1,C0];
H,L,clk  = 1, 0, .C.;

equations
REF_CLK    = !C0;
SYS_CLK    := (COUNT==5) # (COUNT==11);   " High on cnt 5 and 11
SYS_CLK_r  := (COUNT==1) # (COUNT==7);    " Low on cnt 1 and 7
PCLK       := (COUNT==11);                " High on cnt 11
PCLK_r     := (COUNT==5);                 " Low on cnt 5
SCLR0       = (COUNT==11);                " Counter cleared after cnt 11


" The PSG507 has powerup clear of counter and registers.  Six clocks
" are required after powerup for this design to initialize.  This
" design could be initialized after one clock by setting SYS_CLK and
" PCLK high at COUNT0. i.e. SYS_CLK := COUNT0 # COUNT5 # COUNT11; and
" PCLK := COUNT0 # COUNT11;
```

```
test_vectors
([PSG_CLK , COUNT] -> [REF_CLK, SYS_CLK, PCLK])
 [ clk    ,    0  ] -> [   L   ,    L   ,  L  ];
 [ clk    ,    1  ] -> [   H   ,    L   ,  L  ];
 [ clk    ,    2  ] -> [   L   ,    L   ,  L  ];
 [ clk    ,    3  ] -> [   H   ,    L   ,  L  ];
 [ clk    ,    4  ] -> [   L   ,    L   ,  L  ];
 [ clk    ,    5  ] -> [   H   ,    H   ,  L  ];
 [ clk    ,    6  ] -> [   L   ,    H   ,  L  ];
 [ clk    ,    7  ] -> [   H   ,    L   ,  L  ];
 [ clk    ,    8  ] -> [   L   ,    L   ,  L  ];
 [ clk    ,    9  ] -> [   H   ,    L   ,  L  ];
 [ clk    ,   10  ] -> [   L   ,    L   ,  L  ];
 [ clk    ,   11  ] -> [   H   ,    H   ,  H  ];
 [ clk    ,    0  ] -> [   L   ,    H   ,  H  ];
 [ clk    ,    1  ] -> [   H   ,    L   ,  H  ];
 [ clk    ,    2  ] -> [   L   ,    L   ,  H  ];
 [ clk    ,    3  ] -> [   H   ,    L   ,  H  ];
 [ clk    ,    4  ] -> [   L   ,    L   ,  H  ];
 [ clk    ,    5  ] -> [   H   ,    H   ,  L  ];
 [ clk    ,    6  ] -> [   L   ,    H   ,  L  ];
 [ clk    ,    7  ] -> [   H   ,    L   ,  L  ];
 [ clk    ,    8  ] -> [   L   ,    L   ,  L  ];
 [ clk    ,    9  ] -> [   H   ,    L   ,  L  ];
 [ clk    ,   10  ] -> [   L   ,    L   ,  L  ];
 [ clk    ,   11  ] -> [   H   ,    H   ,  H  ];
 [ clk    ,    0  ] -> [   L   ,    H   ,  H  ];

end PSG_EX1
```

```
Module PSG_EX2
title 'ABEL EXAMPLE #2 (Refresh Timer) for the
PSG507 DESIGNERS GUIDE, Texas Instruments,  August 26, 1987'

        PSG2 device 'F507';

" Input pin assignments
PSG_CLK  pin   1;
RESET    pin   2;
RFC      pin   3;

" Output pin and node assignments
REFREQ   pin   8;  REFREQ_r node 47;

" Internal counter bits & control - node declarations
C0 node 55;  C1 node 56;  C2 node 57;
C3 node 58;  C4 node 59;  C5 node 60;
SCLR0  node 25;

" Buried register
C6 node 31; C6_r node 39; " 7th counter bit

" Intermediate declarations for simplification
COUNT       = [C6,C5,C4,C3,C2,C1,C0];
H,L,clk,X  = 1, 0, .C., .X.;

equations
REFREQ    := RFC # RESET;                    " set input
REFREQ_r  := (COUNT==76) & !RESET;           " reset input
C6        := (COUNT==63) & !RESET;           " set input
C6_r      := (COUNT==76) & !RESET # RESET;   " reset input
SCLR0      = (COUNT==76) & !RESET # RESET;   " synchronous nonregistered
clear


test_vectors              ([PSG_CLK,RESET,RFC] ->  REFREQ )
                           [  clk  ,  H  , X ] ->    H     ;   "CNT0
@REPEAT 76  {              [  clk  ,  L  , L ] ->    H     ; } "CNT1-76
                           [  clk  ,  L  , L ] ->    L     ;   "CNT0
@REPEAT 20  {              [  clk  ,  L  , L ] ->    L     ; } "CNT1-20
                           [  clk  ,  L  , H ] ->    H     ;   "CNT21
                           [  clk  ,  L  , L ] ->    H     ;   "CNT22
                           [  clk  ,  H  , X ] ->    H     ;   "CNT0


end PSG_EX2
```

```
Module PSG_EX3
title 'ABEL EXAMPLE #3 (Dynamic Memory Timing Controller)
for the PSG507 DESIGNERS GUIDE, Texas Instruments,  August 26, 1987'

        PSG3 device 'F507';

" Input pin assignments
OSC      pin   1;                          " OSCILLATOR
RESET    pin   2;                          " RESET - INITIALIZES WHEN HIGH
ALE      pin   3;                          " ADDRESS LATCH ENABLE
MIO      pin   4;                          " MEMORY I/O
REFREQ   pin   5;                          " REFRESH REQUEST

" Output pin and node assignments
RDY      pin   8;  RDY_r     node 47;      " READY
MC1      pin   9;  MC1_r     node 48;      " MODE CONTROL
RFC      pin  10;  RFC_r     node 49;      " REFRESH COMPLETE
RAS      pin  11;  RAS_r     node 50;      " ROW ADDRESS STROBE
MSEL     pin  13;  MSEL_r    node 51;      " MULTIPLEXER SELECT
CAS      pin  14;  CAS_r     node 52;      " COLUMN ADDRESS STROBE

" Internal counter bits & control, and state reg - node declarations
C0       node 55;  C1 node 56;  C2 node 57;
C3       node 58;  C4 node 59;
SCLR0    node 25;
CNTHOLD1 node 29;  CNTHOLD1_r node 30; " COUNT/HOLD CONTROL REGISTER
P0       node 31;  P0_r       node 39; " BURIED STATE REGISTER
P1       node 32;  P1_r       node 40; " BURIED STATE REGISTER
BRDY     node 33;  BRDY_r     node 41; " BURIED READY SIGNAL

" Set notation is used to represent control, buried state, and output
" registers. This is done to simplify the equations.  The following
" sets are in the form;  register name = [set input, reset input]. Note
" that the ouput register pin name specifies the set input.
RDY_     = [RDY, RDY_r];
MC1_     = [MC1, MC1_r];
RFC_     = [RFC, RFC_r];
RAS_     = [RAS, RAS_r];
MSEL_    = [MSEL, MSEL_r];
CAS_     = [CAS, CAS_r];
BRDY_    = [BRDY, BRDY_r];

" Intermediate declarations for simplification.
" The sets 'high' and 'low' are used to set or reset the S/R
" registers.  Example: MC1_ := high & RESET; will cause pin 9
" to go high on the next clock edge if input pin 2 is high.
high     = [ 1,  0];
low      = [ 0,  1];
COUNT    = [C4,C3,C2,C1,C0];
STATE_   = [P1,P0];          " STATE REGISTER SET DEFINED
H,L,clk,X = 1, 0, .C., .X.;
@page
```

```
equations
       enable MC1 = 1;  "outputs always enabled, pin 12 is only an input

" Initialization when RESET is high
       [ BRDY,RDY,MC1,RAS,CAS]    :=  RESET;
       [ P0_r,P1_r,MSEL_r,RFC_r]  :=  RESET;

" Counter controls defined
SCLR0 =          RESET
             # (STATE_==1) & (COUNT==9)
             # (STATE_==2) & (COUNT==9) & BRDY
             # (STATE_==2) & (COUNT==19);

CNTHOLD1   =   RESET
             # (STATE_==1) & (COUNT==9)
             # (STATE_==2) & (COUNT==9) & BRDY
             # (STATE_==2) & (COUNT==19);

CNTHOLD1_r =   (STATE_==0) & ALE & MIO & REFREQ & !RESET
             # (STATE_==0) & !REFREQ & !RESET;

" Execution of access and refresh sequènces
state_diagram STATE_                                  " NEXT
   State 0:          case                             " STATE
                       RESET==H                         : 0;
                       ALE & MIO & REFREQ & !RESET      : 1;
                      !REFREQ & !RESET                  : 2;
                       REFREQ & (!ALE # !MIO)           : 0;
                     endcase;
" ACCESS CYCLE
   State 1:          RAS_   := (COUNT==0) & low  & !RESET;
                     MSEL_  := (COUNT==1) & high & !RESET;
                     CAS_   := (COUNT==2) & low  & !RESET;
                     RAS_   := (COUNT==9) & high;
                     MSEL_  := (COUNT==9) & low;
                     CAS_   := (COUNT==9) & high;
                               if (COUNT==9) # RESET then 0 else 1;

" REFRESH CYCLE WITH ACCESS GRANT
   State 2:          RDY_   := low & ALE & MIO  & !RESET;
                     BRDY_  := low & ALE & MIO  & !RESET;
                     MC1_   := (COUNT==0) & low  & !RESET;
                     RFC_   := (COUNT==1) & high & !RESET;
                     RAS_   := (COUNT==1) & low  & !RESET;
                     MC1_   := (COUNT==3) & high;
                     RFC_   := (COUNT==5) & low;
                     RAS_   := (COUNT==6) & high;
                     RAS_   := (COUNT==10)& low  & !RESET;
                     RDY_   := (COUNT==11)& high;
                     BRDY_  := (COUNT==11)& high;
                     MSEL_  := (COUNT==11)& high & !RESET;
                     CAS_   := (COUNT==12)& low  & !RESET;
                     RAS_   := (COUNT==19)& high;
                     MSEL_  := (COUNT==19)& low;
                     CAS_   := (COUNT==19)& high;
                               if (COUNT==9) & BRDY then 0 else 2;
                               if (COUNT==19)# RESET then 0 else 2;
@page
```

```
test_vectors ' ACCESS SEQUENCE '
([OSC,RESET,ALE,MIO,REFREQ,COUNT] -> [RDY,MC1,RFC,RAS,MSEL,CAS,STATE_])
 [clk,  H  , X , X ,  X   ,  X  ] -> [ H , H , L , H , L  , H ,  0   ];
 [clk,  L  , L , H ,  H   ,  0  ] -> [ H , H , L , H , L  , H ,  0   ];
 [clk,  L  , H , H ,  H   ,  0  ] -> [ H , H , L , H , L  , H ,  1   ];
 [clk,  L  , X , X ,  X   ,  0  ] -> [ H , H , L , L , L  , H ,  1   ];
 [clk,  L  , X , X ,  X   ,  1  ] -> [ H , H , L , L , H  , H ,  1   ];
 [clk,  L  , X , X ,  X   ,  2  ] -> [ H , H , L , L , H  , L ,  1   ];
@CONST cnt = 3; @REPEAT 6  {
 [clk,  L  , X , X ,  X   , cnt ] -> [ H , H , L , L , H  , L ,  1   ];
@CONST cnt = cnt + 1;}
 [clk,  L  , X , X ,  X   ,  9  ] -> [ H , H , L , H , L  , H ,  0   ];
 [clk,  L  , L , L ,  H   ,  0  ] -> [ H , H , L , H , L  , H ,  0   ];

test_vectors ' REFRESH WITH ACCESS FOLLOWING'
([OSC,RESET,ALE,MIO,REFREQ,COUNT] -> [RDY,MC1,RFC,RAS,MSEL,CAS,STATE_])
 [clk,  H  , X , X ,  X   ,  X  ] -> [ H , H , L , H , L  , H ,  0   ];
 [clk,  L  , X , X ,  L   ,  0  ] -> [ H , H , L , H , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  0  ] -> [ H , L , L , H , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  1  ] -> [ H , L , H , L , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  2  ] -> [ H , L , H , L , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  3  ] -> [ H , H , H , L , L  , H ,  2   ];
 [clk,  L  , H , H ,  X   ,  4  ] -> [ L , H , H , L , L  , H ,  2   ];
 [clk,  L  , X , X ,  X   ,  5  ] -> [ L , H , L , L , L  , H ,  2   ];
 [clk,  L  , X , X ,  X   ,  6  ] -> [ L , H , L , H , L  , H ,  2   ];
 [clk,  L  , X , X ,  X   ,  7  ] -> [ L , H , L , H , L  , H ,  2   ];
 [clk,  L  , X , X ,  X   ,  8  ] -> [ L , H , L , H , L  , H ,  2   ];
 [clk,  L  , X , X ,  X   ,  9  ] -> [ L , H , L , H , L  , H ,  2   ];
 [clk,  L  , X , X ,  X   , 10  ] -> [ L , H , L , L , L  , H ,  2   ];
 [clk,  L  , X , X ,  X   , 11  ] -> [ H , H , L , L , H  , H ,  2   ];
 [clk,  L  , X , X ,  X   , 12  ] -> [ H , H , L , L , H  , L ,  2   ];
@CONST cnt =13; @REPEAT 6  {
 [clk,  L  , X , X ,  X   , cnt ] -> [ H , H , L , L , H  , L ,  2   ];
@CONST cnt = cnt + 1;}
 [clk,  L  , X , X ,  X   , 19  ] -> [ H , H , L , H , L  , H ,  0   ];

test_vectors ' REFRESH WITHOUT ACCESS FOLLOWING'
([OSC,RESET,ALE,MIO,REFREQ,COUNT] -> [RDY,MC1,RFC,RAS,MSEL,CAS,STATE_])
 [clk,  H  , X , X ,  X   ,  X  ] -> [ H , H , L , H , L  , H ,  0   ];
 [clk,  L  , X , X ,  L   ,  0  ] -> [ H , H , L , H , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  0  ] -> [ H , L , L , H , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  1  ] -> [ H , L , H , L , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  2  ] -> [ H , L , H , L , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  3  ] -> [ H , H , H , L , L  , H ,  2   ];
 [clk,  L  , L , H ,  X   ,  4  ] -> [ H , H , H , L , L  , H ,  2   ];
 [clk,  L  , H , L ,  X   ,  5  ] -> [ H , H , L , L , L  , H ,  2   ];
 [clk,  L  , H , L ,  X   ,  6  ] -> [ H , H , L , H , L  , H ,  2   ];
 [clk,  L  , H , L ,  X   ,  7  ] -> [ H , H , L , H , L  , H ,  2   ];
 [clk,  L  , H , L ,  X   ,  8  ] -> [ H , H , L , H , L  , H ,  2   ];
 [clk,  L  , H , L ,  X   ,  9  ] -> [ H , H , L , H , L  , H ,  0   ];
@page
```

```
test_vectors ' RESET DURING REFRESH '
([OSC,RESET,ALE,MIO,REFREQ,COUNT] -> [RDY,MC1,RFC,RAS,MSEL,CAS,STATE_])
 [clk,  H  , X , X ,  X   ,  X  ] -> [ H , H , L , H , L  , H ,  0   ];
 [clk,  L  , X , X ,  L   ,  0  ] -> [ H , H , L , H , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  0  ] -> [ H , L , L , H , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  1  ] -> [ H , L , H , L , L  , H ,  2   ];
 [clk,  L  , L , L ,  X   ,  2  ] -> [ H , L , H , L , L  , H ,  2   ];
 [clk,  H  , X , X ,  X   ,  3  ] -> [ H , H , L , H , L  , H ,  0   ];

end PSG_EX3
```

```
/*****************************************************************************/
/* CUPL (tm) TEMPLATE FOR THE TI PSG507                                      */
/*                                                                           */
/* This file provides the PSG507 designer quick access to the information   */
/* needed to write a CUPL source file.  By copying this file and deleting    */
/* this box from the  new file a fill-in-the-blanks template will be left    */
/* for use in creating a source file.                                        */
/*                                                                           */
/* 6-BIT COUNTER:  The 6-bit counter is accessed through use of the PINNODE */
/*                 statement.  The pinnode statement is used to assign       */
/*                 variables to the internal node numbers.  i.e. pinnode     */
/*                 [33..38] = [C0..C5].CNT.  These variables can then        */
/*                 be used in the same manner as input pins.Using the        */
/*                 field statement, i.e. field COUNTER = [C0..C5].CNT;       */
/*                 allows an equation like Q0 = COUNTER'd'3 # COUNTER'd'7;    */
/*                 This  equation causes the nonregistered output Q0 to be   */
/*                 high only during counts 3 and 7.                          */
/*                                                                           */
/* COUNTER CONTROLS:  Clear and hold functions SCLR0, SCLR1, CNTHOLD0,       */
/*                    and CNTHOLD1 are specified using the PINNODE           */
/*                    statement. Any valid variable can be used as a node    */
/*                    name, i.e. pinnode [39..42] = [CLR0,CLR1,HLD0,HLD1];   */
/*                    These variables can then be used in the same manner    */
/*                    as an output pin.                                      */
/*                                                                           */
/* STATE  REGISTERS:  Buried registers are assigned using the NODE state-    */
/*                    ment, i.e. node  [P0..P7];.  The actual registers      */
/*                    used are chosen by software in the order specified.    */
/*                                                                           */
/* OUTPUT STRUCTURE: Each output can be defined as either registered or      */
/*                   nonregistered. The structure assignment is automatic    */
/*                   and is determined by usage.  Q0.s = COUNTER'd'77;       */
/*                   causes the Q0 output to remain registered while         */
/*                   Q0 = COUNTER'd'77; causes the Q0 output to be non-      */
/*                   registered.  When using nonregistered outputs CUPL      */
/*                   will automatically program the associated reset fuse    */
/*                   for each product term used as required in the PSG507    */
/*                   data sheet.                                             */
/*                                                                           */
/*****************************************************************************/
```

```
/*****************************************************************************/
/*                                                                           */
/*                                                                           */
/* CLOCK POLARITY:  The default clock polarity is active on the rising       */
/*                  edge.  The equation  OUTPUT.ckmux = !CLK; will cause     */
/*                  the clock to be active on the falling edge.  The         */
/*                  default can be specified by OUTPUT.ckmux = CLK;          */
/*                                                                           */
/* OUTPUT ENABLE:  The default condition is outputs always enabled. The      */
/*                 output enable fuse at pin 17 can be blown using the       */
/*                 .oe extention. If pin 17 = EN; the fuse will be blown     */
/*                 by the equation  OUTPUTS.oe = EN; where OUTPUTS is a      */
/*                 defined set of outputs. A single output can also be       */
/*                 used to blow the fuse, Q0.oe = EN;                        */
/*                                                                           */
/* SIMULATION:     During simulation of a PSG design the CUPL 2.15a          */
/*                 simulator will advance the counter on each clock          */
/*                 depending on the state of the counter hold and clear      */
/*                 functions. The powerup condition (counter bits and        */
/*                 all registers low) is recognized by the simulator.        */
/*                                                                           */
/*   CUPL is a trade mark of Personal CAD Systems, Inc.                      */
/*****************************************************************************/
```

```
NAME      XXXXX ;
PARTNO    XXXXX ;
DATE      XX/XX/XX ;
REV       XX ;
DESIGNER  XXXXX ;
COMPANY   XXXXX ;
ASSEMBLY  XXXXX ;
LOCATION  XXXXX ;

/*************************************************************************/
/*                                                                       */
/*                                                                       */
/*                                                                       */
/*************************************************************************/
/*  Allowable Target Device Types :  TEXAS INTSRUMENTS  PSG507           */
/*************************************************************************/

/**  Inputs  **/
pin  1           = CLK       ;          /* PSG's clock input             */
pin  2           =           ;          /*                               */
pin  3           =           ;          /*                               */
pin  4           =           ;          /*                               */
pin  5           =           ;          /*                               */
pin  6           =           ;          /*                               */
pin  7           =           ;          /*                               */
pin 17           =           ;          /* input and/or output enable    */
pin 18           =           ;          /*                               */
pin 19           =           ;          /*                               */
pin 20           =           ;          /*                               */
pin 21           =           ;          /*                               */
pin 22           =           ;          /*                               */
pin 23           =           ;          /*                               */

/**  Outputs  **/
pin  8           =           ;          /*                               */
pin  9           =           ;          /*                               */
pin 10           =           ;          /*                               */
pin 11           =           ;          /*                               */
pin 13           =           ;          /*                               */
pin 14           =           ;          /*                               */
pin 15           =           ;          /*                               */
pin 16           =           ;          /*                               */

/** Node Declarations **/
pinnode [33..38] = [C0..5]   ;          /* BUILT-IN 6-BIT COUNTER        */
pinnode 39       = SCLR0     ;          /* COUNTER CLEAR - non registered */
pinnode 40       = SCLR1     ;          /* COUNTER CLEAR - registered    */
pinnode 41       = CNTHOLD0  ;          /* COUNTER HOLD  - non registered */
pinnode 42       = CNTHOLD1  ;          /* COUNTER HOLD  - registered    */
node               [P0..P7]  ;          /* BURIED STATE REGISTERS        */

/** Declarations and Intermediate Variable Definitions **/
field COUNTER    = [C5..0]   ;          /* 6-BIT COUNTER                 */

/** Logic Equations **/

/** End of File **/
```

```
Name      PSG_EX1;
Partno    TI0001;
Date      08/26/87;
Rev       02;
Designer  Schiele/Woolhiser;
Company   Texas Instruments/Personnal CAD Systems;
Assembly  None;
Location  None;

/*********************************************************************/
/* Waveform Generator                                                */
/*                                                                   */
/* This is the first example from "A Designer's Guide to the         */
/* PSG507", by R. Breuninger.  In this example a waveform generator */
/* which generates three clocks, running at 15, 5, and 2.5MHz, is    */
/* implemented for the PSG507 using CUPL.  In this implementation    */
/* the built-in counter feature of the PSG507 is utilized to divide */
/* a 30MHz master clock to generate the three output waveforms. The */
/* built-in counter is accessed by defining the variable list        */
/* [C0..5] as PINNODE's and then using the list where ever the       */
/* counter values are needed. The synchronous clear function, SCLR0 */
/* is also accessed through use of the pinnode statement.            */
/*********************************************************************/
/*  Allowable Target Device Types :   TI PSG507                      */
/*********************************************************************/

/**  Inputs  **/

pin 1             =  PSG_CLK;      /* 30MHz MASTER CLOCK              */

/**  Outputs  **/

pin 8             = REF_CLK;       /* 15MHz REFERENCE CLOCK           */
pin 9             = SYS_CLK;       /*  5MHz SYSTEM CLOCK              */
pin 10            = PCLK;          /* 2.5MHz PERIPHERAL CLOCK         */

pinnode [33..36] = [C0..3];        /* BUILT-IN COUNTER                */
pinnode 39        = SCLR0;         /* COUNTER SYNCHRONOUS CLEAR       */

/** Declarations and Intermediate Variable Definitions **/

field COUNTER     = [C3..0].CNT;

/**[SYS_CLK, PCLK, C0..3].CKMUX = !PSG_CLK;                          **/

/** Logic Equations **/

REF_CLK           = !C0.CNT;
SYS_CLK.r         = COUNTER:'d'1 # COUNTER:'d'7;
SYS_CLK.s         = COUNTER:'d'5 # COUNTER:'d'11;
PCLK.r            = COUNTER:'d'5;
PCLK.s            = COUNTER:'d'11;
SCLR0             = COUNTER:'d'11;

/* The PSG507 has powerup clear of counter and registers.  Six clocks  */
/* are required after powerup for this design to initialize.  This     */
/* design could be initialized after one clock by setting SYS_CLK and  */
/* PCLK high at COUNT 0. i.e. SYS_CLK.s = COUNTER:'d'0 # COUNTER:'d'5  */
/* # COUNTER:'d'11; and  PCLK.s = COUNTER:'d'0 # COUNTER:'d'11;        */

/** End of file **/
```

```
Name      PSG_EX1;
Partno    TI0001;
Date      08/26/87;
Rev       02;
Designer  Schiele/Woolhiser;
Company   Texas Instruments/Personnal CAD Systems;
Assembly  None;
Location  None;

/*********************************************************************/
/*                                                                   */
/* Waveform Generator                                                */
/*                                                                   */
/* CUPL simulation file for Example 1 from  "A Designer's Guide to  */
/* the PSG507".                                                      */
/*********************************************************************/
/*  Allowable Target Device Types :   TI PSG507                      */
/*********************************************************************/

ORDER: PSG_CLK, %7, REF_CLK, %9, SYS_CLK, %6, PCLK;

BASE: DECIMAL;

VECTORS:
$msg"  ";
$msg"  PSG_CLK  REF_CLK   SYS_CLK PCLK ";
$msg" ---------------------------------------- ";

          P        X        0     0
          0        H        H     H                    /* 0 */
          C        L        H     H                    /* 1 */
          C        H        L     H                    /* 2 */
          C        L        L     H                    /* 3 */
          C        H        L     H                    /* 4 */
          C        L        L     H                    /* 5 */
          C        H        H     L                    /* 6 */
          C        L        H     L                    /* 7 */
          C        H        L     L                    /* 8 */
          C        L        L     L                    /* 9 */
          C        H        L     L                    /* 10 */
          C        L        L     L                    /* 11 */
          C        H        H     H                    /* 0  */
```

```
Name      PSG_EX2;
Partno    TI0002;
Date      08/26/87;
Rev       02;
Designer  Schiele/Woolhiser;
Company   Texas Instruments/Personal CAD Systems;
Assembly  None;
Location  None;

/*************************************************************************/
/*                                                                       */
/* Refresh Timer                                                         */
/*                                                                       */
/* This is the second example from "A Designer's Guide to the PSG507", by */
/* R. Breuninger.  In this example a dynamic memory refresh timer, which  */
/* generates a refresh request every 15.4 uS, is implemented for the TI   */
/* PSG507 using CUPL.  In this implementation the built-in 6-bit counter  */
/* is extended by using one of the buried state registers as the 7th bit. */
/*                                                                       */
/*************************************************************************/
/*  Allowable Target Device Types :  TI PSG507                           */
/*************************************************************************/

/**  Inputs  **/
pin 1           = PSG_CLK;          /* 5MHz SYSTEM CLOCK                */
pin 2           = RESET;            /* SYNCHRONOUS RESET OR INITIALIZE  */
pin 4           = RFC;              /* REFRESH COMPLETE                 */

/**  Outputs  **/
pin 8           = REFREQ;           /* REFRESH REQUEST                  */

/** Node Declarations **/
pinnode [33..38] = [C0..5];         /* BUILT-IN 6-BIT COUNTER           */
pinnode 39      = SCLR0;            /* COUNTER CLEAR CONTROLS           */
node              C6;               /* EXTENSION TO 6-BIT COUNTER       */

/** Declarations and Intermediate Variable Definitions **/
field 6BIT      = [C0..5].CNT;      /* 6 BIT COUNTER                    */
field COUNTER   = [6BIT,C6];        /* FULL 7-BIT COUNTER               */

/** Logic Equations **/

REFREQ.s        = RFC # RESET;
REFREQ.r        = COUNTER:'d'76 & !RESET;

/* EXTEND BUILT-IN 6-BIT COUNTER BY ADDING A BURIED STATE REGISTER */

C6.s            =  COUNTER:'d'63 & !RESET;
C6.r            =  COUNTER:'d'76 #  RESET;

/* BUILT-IN COUNTER CONTROL */

SCLR0           = COUNTER:'d'76 # RESET;

/** End of file **/
```

```
Name      PSG_EX2;
Partno    TI0002;
Date      08/26/87;
Rev       02;
Designer  Schiele/Woolhiser;
Company   Texas Instruments/Personal CAD Systems;
Assembly  None;
Location  None;

/*************************************************************************/
/* Refresh Timer                                                         */
/*                                                                       */
/* CUPL simulation file for example 2 from "A Designer's Guide to the    */
/* PSG507".  This simulation file uses the $REPEAT directive to generate */
/* many of the test vectors in the counter sequence.                     */
/*************************************************************************/
/*  Allowable Target Device Types :  TI PSG507                           */
/*************************************************************************/

ORDER:  PSG_CLK,%6,RESET,%4,RFC,%4,C6,%5,REFREQ;

BASE: DECIMAL;

VECTORS:

$msg"  ";
$msg" NORMAL REFRESH CYCLE WITH REFRESH COMPLETE SIGNAL";
$msg"  ";
$msg"   -------INPUTS--------  -OUTPUT-";
$msg"   PSG_CLK RESET RFC  C6   REFREQ ";
$msg"   ------------------------------------"; /*COUNT*/
        C      1    X    L    H              /*  0  */
        C      0    X    L    H              /*  1  */
$repeat 74;
        C      0    X    *    *              /*2-75 */
$msg "end repeat";
        C      0    0    H    H              /* 76  */
        C      0    0    L    L              /*  0  */
        C      0    0    L    L              /*  1  */
        C      0    0    L    L              /*  2  */
        C      0    1    L    H              /*  3  */
        C      0    0    L    H              /*  4  */

$msg"  ";
$msg" CHECK RESET FUNCTION AFTER REFREQ=L ";
$msg"  ";
$msg"   -------INPUTS--------  -OUTPUT-";
$msg"   PSG_CLK RESET RFC  C6   REFREQ ";
$msg"   ------------------------------------"; /*COUNT*/
        C      1    X    L    H              /*  0  */
        C      0    X    L    H              /*  1  */
$repeat 74;
        C      0    X    *    *              /*2-75 */
$msg "end repeat";
        C      0    0    H    H              /* 76  */
        C      0    0    L    L              /*  0  */
$repeat 29;
        C      0    0    *    *              /*1-30 */
$msg "end repeat";
        C      0    0    L    L              /* 31  */
        C      1    0    L    H              /*  0  */
```

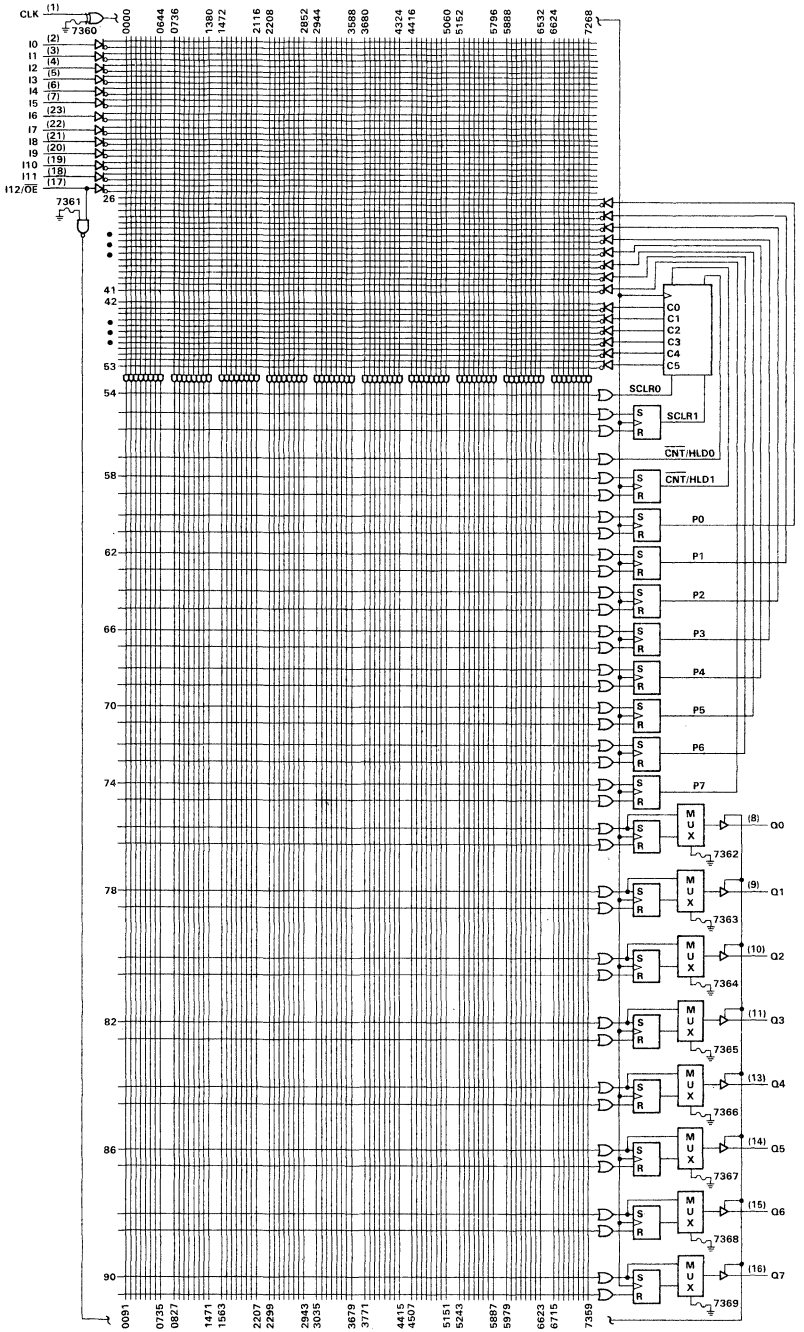
```
Name      PSG_EX3;
Partno    TI0003;
Date      08/26/87;
Rev       02;
Designer  Schiele/Woolhiser;
Company   Texas Instruments/Personnal CAD Systems;
Assembly  None;
Location  None;

/*************************************************************************/
/*                                                                       */
/* Dynamic Memory Timing Controller                                      */
/*                                                                       */
/* This is the third example from "A Designer's Guide to the PSG507", by */
/* R. Breuninger.  In this example a dynamic memory timing controller,   */
/* which generates the control signals (RDY, MC1, RFC, RAS, CAS, MSEL)   */
/* necessary for accessing and refreshing dynamic memory, is implemented */
/* for the TI PSG507 using CUPL.                                         */
/*************************************************************************/
/*  Allowable Target Device Types :  TI PSG507                           */
/*************************************************************************/

/**  Inputs  **/
PIN 1           =  REF_CLK;          /* OSCILLATOR                  */
PIN 2           =  RESET;            /* RESET - INITIALIZE          */
PIN 3           =  ALE;              /* ADDRESS LATCH ENABLE        */
PIN 4           =  MIO;              /* MEMORY I/O                  */
PIN 5           =  REFREQ;           /* REFRESH REQUEST             */

/**  Outputs  **/
PIN 8           = RDY;               /* READY                       */
PIN 9           = MC1;               /* MODE CONTROL                */
PIN 10          = RFC;               /* REFRESH COMPLETE            */
PIN 11          = RAS;               /* ROW ADDRESS STROBE          */
PIN 13          = MSEL;              /* MULTIPLEXER SELECT          */
PIN 14          = CAS;               /* COLUMN ADDRESS STROBE       */

/**  Node Declarations **/
pinnode [33..37] = [C0..4];          /* BUILT-IN COUNTER            */
pinnode 39       = SCLR0;            /* COUNTER HOLD non-registered */
pinnode 40       = SCLR1;            /* COUNTER HOLD registered     */
pinnode 41       = CNTHOLD0;         /* COUNTER HOLD non-refistered */
pinnode 42       = CNTHOLD1;         /* COUNTER HOLD registered     */
node               [P0..1];          /* BURIED STATE REGISTERS      */
node               BRDY;             /* BURIED READY SIGNAL         */

 /** Declarations and Intermediate Variable Definitions **/
field COUNTER    = [C0..4].CNT;
field STATE      = [P1..0];
$define ST0        'b'00
$define ST1        'b'01
$define ST2        'b'10
```

```
sequence STATE {
present ST0:
       /* INITIALIZE AND HOLD */
       if(RESET)                              next ST0;
       if(ALE & MIO & REFREQ & !RESET) next ST1;
       if(!REFREQ & !RESET)                   next ST2;
       default                                next ST0;

present ST1:
       /* ACCESS CYCLE */
       if(RESET)                              next ST0;
       if(COUNTER:'d'0)  & !RESET      next ST1 out !RAS;
       if(COUNTER:'d'1)  & !RESET      next ST1 out  MSEL;
       if(COUNTER:'d'2)  & !RESET      next ST1 out !CAS;
       if(COUNTER:'d'9)  & !RESET      next ST0 out [RAS,!MSEL,CAS];
       default                                next ST1;

present ST2:
       /* REFRESH/ACCESS GRANT CYCLE */
       if(RESET)                              next ST0;
       if(COUNTER:'d'0)  & !RESET      next ST2 out !MC1;
       if(COUNTER:'d'1)  & !RESET      next ST2 out [RFC,!RAS];
       if(COUNTER:'d'3)  & !RESET      next ST2 out  MC1;
       if(COUNTER:'d'5)  & !RESET      next ST2 out !RFC;
       if(COUNTER:'d'6)  & !RESET      next ST2 out  RAS;
       if(COUNTER:'d'9)  &  BRDY       next ST0;
       if(COUNTER:'d'10) & !RESET      next ST2 out !RAS;
       if(COUNTER:'d'11) & !RESET      next ST2 out [BRDY,MSEL];
       if(COUNTER:'d'12) & !RESET      next ST2 out [RDY,!CAS];
       if(COUNTER:'d'19)                      next ST0 out [RAS,!MSEL,CAS];
       default                                next ST2; }

append BRDY.r    = STATE:ST2 & ALE & MIO & !RESET;
append  RDY.r    = STATE:ST2 & ALE & MIO & !RESET;

/* BUILT-IN COUNTER CONTROL EQUATIONS, WRITTEN  */
/* OUTSIDE THE STATE MACHINE FOR CLARITY.       */
SCLR0            = RESET                        /* Clear counter on RESET */
                 # STATE:ST1 & COUNTER:'d'9     /* and transitions to ST0.*/
                 # STATE:ST2 & COUNTER:'d'9 & BRDY
                 # STATE:ST2 & COUNTER:'d'19;
CNTHOLD1.s       = RESET                        /* Set count hold while   */
                 # STATE:ST1 & COUNTER:'d'9     /* clearing the counter.  */
                 # STATE:ST2 & COUNTER:'d'9 & BRDY
                 # STATE:ST2 & COUNTER:'d'19;
CNTHOLD1.r       = STATE:ST0 & ALE & MIO
                   & REFREQ & !RESET  /* Reset count hold       */
                 # STATE:ST0 & !REFREQ & !RESET;/* on transition to ST1,2 */

APPEND BRDY.s  = RESET;  APPEND RAS.s  = RESET;  APPEND P1.r   = RESET;
APPEND RDY.s   = RESET;  APPEND CAS.s  = RESET;  APPEND MSEL.r = RESET;
APPEND MC1.s   = RESET;  APPEND P0.r   = RESET;  APPEND RFC.r  = RESET;

/** End of file **/
```

```
Name     PSG_EX3;
Partno   TI0003;
Date     08/26/87;
Rev      02;
Designer Schiele/Woolhiser;
Company  Texas Instruments/Personnal CAD Systems;
Assembly None;
Location None;

/*****************************************************************************/
/*                                                                           */
/* Dynamic Memory Timing Controller                                          */
/*                                                                           */
/* CUPL simulation file for Example 3 from "A Designer's Guide to the        */
/* PSG507".                                                                  */
/*****************************************************************************/
/*  Allowable Target Device Types :  TI PSG507                               */
/*****************************************************************************/

ORDER:  REF_CLK,%4,RESET,%4,ALE,%3,MIO,%4,REFREQ,%9,RDY,%3,
        MC1,%3,RFC,%3,RAS,%3,MSEL,%4,CAS,%3,STATE;

BASE: DECIMAL;

VECTORS:

$msg"     ";
$msg"     ";
$msg"ACCESS TIMING CYCLE ";
$msg"     ";
$msg"     ------------ INPUT -----     ------------ OUTPUT ----------- ";
$msg"     CLK RESET ALE MIO REFREQ     RDY MC1 RFC RAS MSEL CAS STATE  ";
$msg"     ------------------------------------------------------------- ";
/*RESET*/  C    1    X   X    X         H   H   L   H   L   H   "0"
           C    0    0   1    1         H   H   L   H   L   H   "0"
           C    0    1   1    1         H   H   L   H   L   H   "1"
           C    0    X   X    X         H   H   L   L   L   H   "1"
           C    0    X   X    X         H   H   L   L   H   H   "1"
           C    0    X   X    X         H   H   L   L   H   L   "1"
           C    0    X   X    X         H   H   L   L   H   L   "1"
           C    0    X   X    X         H   H   L   L   H   L   "1"
           C    0    X   X    X         H   H   L   L   H   L   "1"
           C    0    X   X    X         H   H   L   L   H   L   "1"
           C    0    X   X    X         H   H   L   L   H   L   "1"
           C    0    X   X    X         H   H   L   H   L   H   "0"
           C    0    0   0    1         H   H   L   H   L   H   "0"

$msg"     ";
$msg"     ";
$msg"REFRESH WITH ACCESS FOLLOWING ";
$msg"     ";
$msg"     ------------ INPUT -----     ------------ OUTPUT ----------- ";
$msg"     CLK RESET ALE MIO REFREQ     RDY MC1 RFC RAS MSEL CAS STATE  ";
$msg"     ------------------------------------------------------------- ";
/*RESET*/  C    1    X   X    X         H   H   L   H   L   H   "0"
           C    0    X   X    0         H   H   L   H   L   H   "2"
           C    0    0   0    X         H   L   L   H   L   H   "2"
           C    0    0   0    X         H   L   H   L   L   H   "2"
           C    0    0   0    X         H   L   H   L   L   H   "2"
           C    0    0   0    X         H   H   H   L   L   H   "2"
```

```
                C    0    1    1    X         L    H    H    L    L    H    "2"
                C    0    X    X    X         L    H    L    L    L    H    "2"
                C    0    X    X    X         L    H    L    H    L    H    "2"
                C    0    X    X    X         L    H    L    H    L    H    "2"
                C    0    X    X    X         L    H    L    H    L    H    "2"
                C    0    X    X    X         L    H    L    H    L    H    "2"
                C    0    X    X    X         L    H    L    L    L    H    "2"
                C    0    X    X    X         L    H    L    L    H    H    "2"
                C    0    0    X    X         H    H    L    L    H    L    "2"
                C    0    0    X    X         H    H    L    L    H    L    "2"
                C    0    0    X    X         H    H    L    L    H    L    "2"
                C    0    0    X    X         H    H    L    L    H    L    "2"
                C    0    0    X    X         H    H    L    L    H    L    "2"
                C    0    0    X    X         H    H    L    L    H    L    "2"
                C    0    0    X    X         H    H    L    L    H    L    "2"
                C    0    0    X    X         H    H    L    H    L    H    "0"

$msg"      ";
$msg"      ";
$msg" REFRESH WITHOUT ACCESS FOLLOWING ";
$msg"      ";
$msg"      ------------ INPUT -----      ------------ OUTPUT ----------- ";
$msg"      CLK RESET ALE MIO REFREQ      RDY MC1 RFC RAS MSEL CAS STATE  ";
$msg"      ------------------------------------------------------------- ";
/*RESET*/  C    1    X    X    X         H    H    L    H    L    H    "0"
           C    0    X    X    0         H    H    L    H    L    H    "2"
           C    0    0    0    X         H    L    L    H    L    H    "2"
           C    0    0    0    X         H    L    H    L    L    H    "2"
           C    0    0    0    X         H    L    H    L    L    H    "2"
           C    0    0    0    X         H    H    H    L    L    H    "2"
           C    0    0    1    X         H    H    H    L    L    H    "2"
           C    0    1    0    X         H    H    L    L    L    H    "2"
           C    0    1    0    X         H    H    L    H    L    H    "2"
           C    0    1    0    X         H    H    L    H    L    H    "2"
           C    0    1    0    X         H    H    L    H    L    H    "2"
           C    0    1    0    X         H    H    L    H    L    H    "0"

$msg"      ";
$msg"      ";
$msg" RESET DURING REFRESH";
$msg"      ";
$msg"      ------------ INPUT -----      ------------ OUTPUT ----------- ";
$msg"      CLK RESET ALE MIO REFREQ      RDY MC1 RFC RAS MSEL CAS STATE  ";
$msg"      ------------------------------------------------------------- ";
/*RESET*/  C    1    X    X    X         H    H    L    H    L    H    "0"
           C    0    X    X    0         H    H    L    H    L    H    "2"
           C    0    0    0    X         H    L    L    H    L    H    "2"
           C    0    0    0    X         H    L    H    L    L    H    "2"
           C    0    0    0    X         H    L    H    L    L    H    "2"
           C    1    X    X    X         H    H    L    H    L    H    "0"
```

Appendix C. PSG507 Fuse Numbers



System Solutions for Static Column Decode

Robert K. Breuninger, Loren Schiele,
and Joshua K. Peprah

TEXAS
INSTRUMENTS

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Contents

Title	Page
INTRODUCTION	3-85
STATIC COLUMN DECODE	3-85
TYPICAL MEMORY CONTROLLER	3-87
TIMING CONTROLLER DETAILS	3-87
NORMAL ACCESS SEQUENCE	3-89
HIGH-SPEED ACCESS SEQUENCE	3-89
EXTENDED ACCESS SEQUENCE	3-90
NORMAL/EXTENDED REFRESH SEQUENCES	3-90
SOFTWARE SUPPORT	3-94
SUMMARY	3-94

Appendixes

A	ABEL™ Files	3-95
B	CUPL™ Files	3-101

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List of Illustrations

Figure	*Title*	*Page*
1	Static Column Decode Mode Read Cycle Timing	3-85
2	68020/6301 Static Column Memory Controller	3-86
3	ALS6310 Static Column/Page Mode Access Detector	3-87
4	Timing Controller Flowchart	3-88
5	Normal Access Cycle	3-89
6	High-Speed Access Cycle	3-90
7	Extended Access Cycle	3-91
8	Normal Refresh/Access Grant Cycle	3-92
9	Extended Refresh Cycle	3-93

INTRODUCTION

The new 32-bit microprocessors are capable of addressing 4G bytes of physical memory and typically feature clock frequencies greater than 16 Mhz. However, clock speed alone does not guarantee increased system performance; if the processor must wait for data, then memory bandwidth will be the limiting factor.

This situation exists between today's microprocessors and the access times of affordable DRAMs. One solution to optimizing system performance is to mix and match memory, using lower cost dynamic RAM in conjunction with fast, more expensive static RAM caches. However, this approach is only attractive to high end systems where cost and board space is a less significant factor.

Another approach to improving system performance is to utilize the new accessing modes available on certain 1 meg DRAMs, such as static column decode. This method does not improve system performance as much as caches, but it does involve less hardware, resulting in lower system cost. This approach can also be used in systems already using caches, further improving system performance.

This application note describes the theory of using static column decode and also describes how it might be implemented in a typical system. In addition, it highlights three new products from Texas Instruments. The SN74ALS6300 "Selectable Refresh Timer", the SN74ALS6310 "Static Column Access Detector", and the TIBPSG507 "Programmable Sequence Generator".

STATIC COLUMN DECODE

The TMS4C1027 is a 1,048,576-bit × 1 dynamic RAM featuring static column decode. Static column decode allows high-speed read and write operations by reducing the number of required signal setup, hold, and transition timings. This is achieved by first strobing the row and column addresses in the normal manner by taking $\overline{RAS}$ and $\overline{CAS}$ low. If $\overline{RAS}$ and $\overline{CAS}$ are kept low, new data can be accessed by simply changing the column addresses, assuming the new address is in the same row. If the new address is not in the same row, then a normal access cycle must be performed.

Figure 1 is a timing diagram taken from the TMS4C1027 datasheet showing static column decode mode read cycle timing.

If the assumption is made that the majority of memory references tend to be sequential, which is a similar assumption made when using caches, then it is logical to assume that a large percentage of memory accesses will be within the same row. The trick is how to implement a timing controller which will take full advantage of the static column mode of operation.

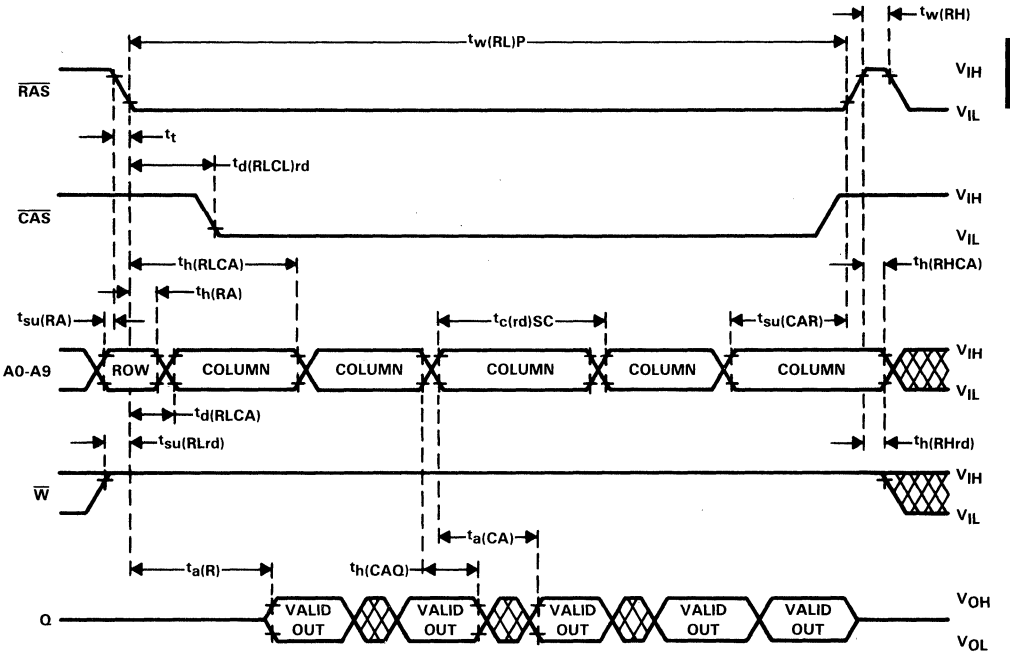


Figure 1. Static Column Decode Mode Read Cycle Timing

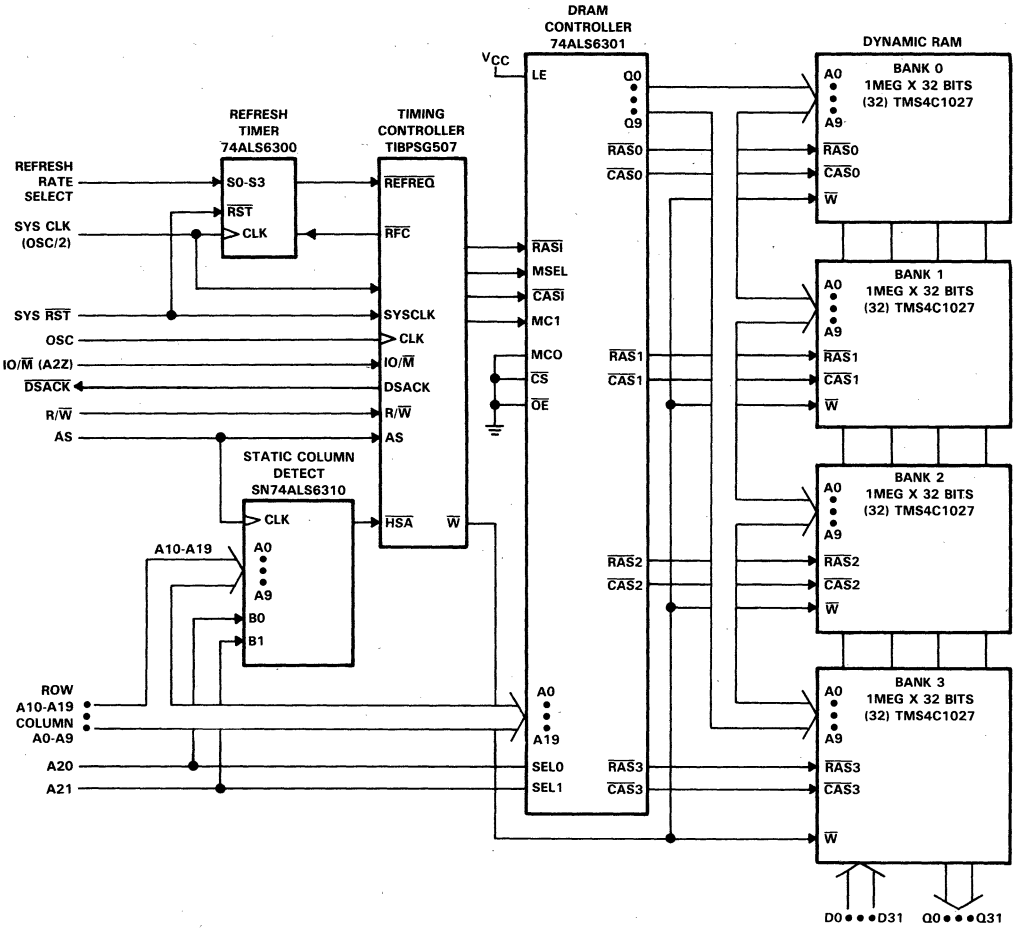


Figure 2. 68020 Static Column Memory Controller

TYPICAL MEMORY CONTROLLER

Figure 2 shows a block diagram of a memory system utilizing static column decode. The ALS6310 is a new circuit offered by Texas Instruments which detects if the present row being accessed is the same as last row accessed. This is the fundamental requirement for implementing static column decode. Note that the row addresses from the 68020 are used as the most significant bits (A10-A19) and the column addresses are used as the least significant bits (A0-A9). Figure 3 shows a block diagram of the ALS6310.

In circuit operation, when address strobe (AS) from the 68020 is taken low, the present row (A10-A19) and bank address (B0, B1) is clocked into the first register of the ALS6310. The previous bank and row address, stored in the first register, is clocked into the second register at the same time. The two addresses are then compared to see if they are equal. If they are equal, the high speed access output ($\overline{HSA}$) will be logically low. If not, $\overline{HSA}$ will be high.

The function of the PSG507 is to generate the required memory timing control signals ($\overline{RAS}$, $\overline{CAS}$, etc.) for the ALS6301 dynamic memory controller. The ALS6301 is responsible for multiplexing row and column addresses into DRAM. The ALS6301 is also capable of driving 4 banks of 1M-byte memory.

Supporting the PSG507 is the ALS6300 refresh timer. This device is responsible for generating a refresh request signal ($\overline{REFREQ}$) every 15.5 μs. The input select lines are hardwired to match the microprocessor clock frequency. The refresh complete input ($\overline{RFC}$), resets the $\overline{REFREQ}$ signal after the timing controller completes the refresh cycle.

TIMING CONTROLLER DETAILS

Figure 4 shows a typical flow chart for implementing static column decode. As stated before, the PSG507 is responsible for implementing the flow chart shown in Figure 4. A breakdown of this flow chart reveals 9 states (ST0-ST8), associated with 5 different sequences. States ST0, ST1, ST3, and ST4 are holding and transition states, leading into the various sequences. The five possible sequences are listed below.

ST2 Normal Access Sequence
ST5 Extended Access Sequence
ST6 High-Speed Access Sequence
ST7 Normal Refresh Sequence
ST8 Extended Refresh Sequence

Notice that the $\overline{HSA}$ signal from the ALS6310 decides if the timing controller will execute ST5, the Extended Access Sequence, or ST6, the High-Speed Access Sequence. A brief description of each sequence follows.

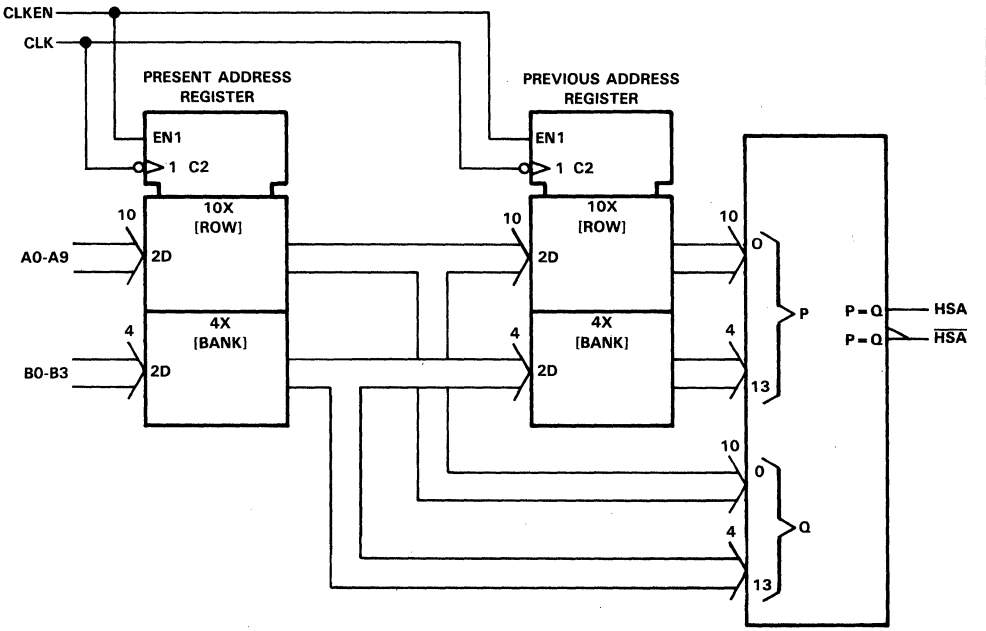


Figure 3. ALS6310 Static Column Page Mode Access Detector

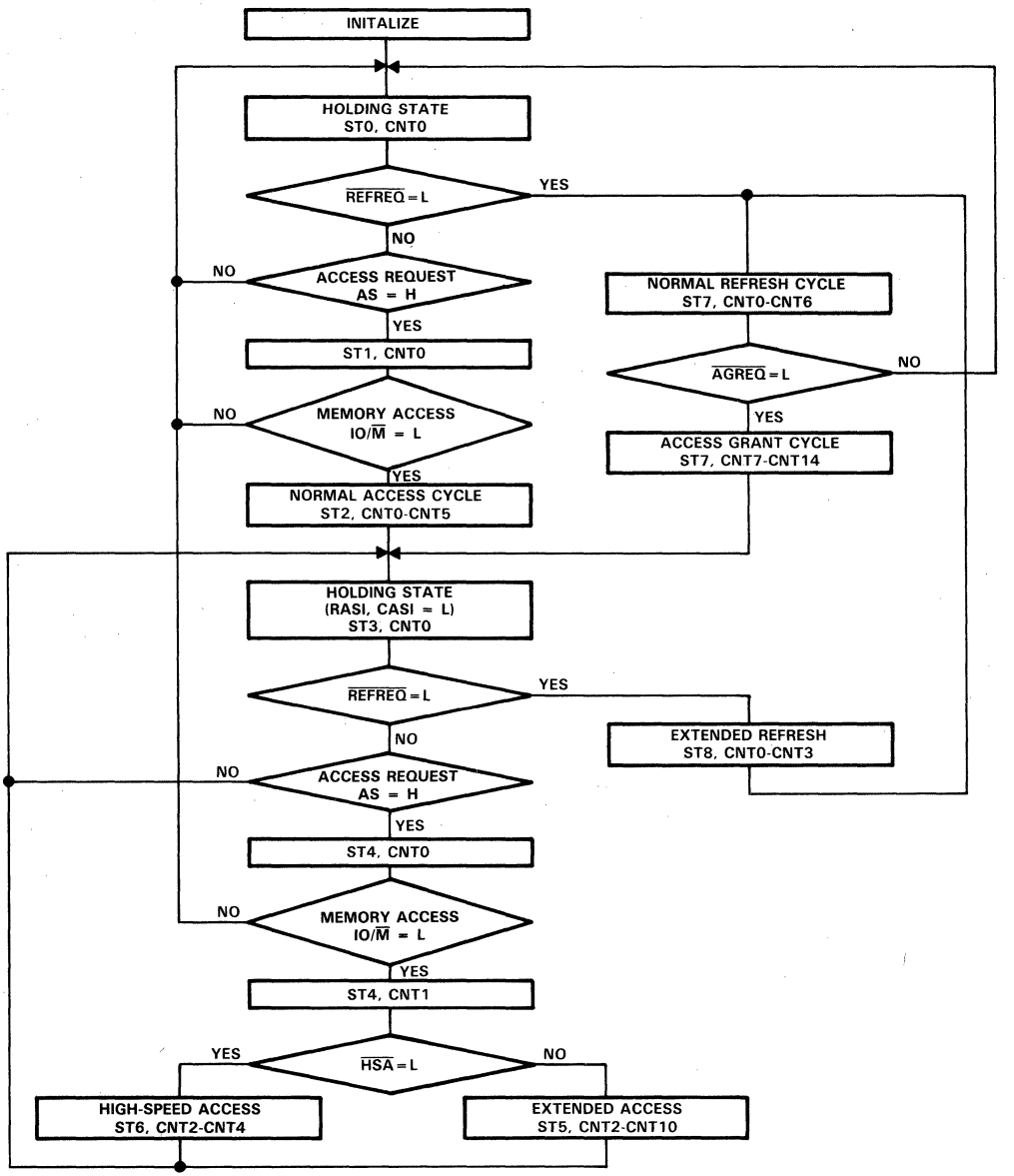


Figure 4. Timing Controller Flowchart

NORMAL ACCESS SEQUENCE

The normal access sequence is shown in Figure 5. This sequence begins by executing a normal $\overline{RAS}/\overline{CAS}$ cycle. Notice that a wait state of one clock cycle is needed to guarantee that data is valid for the 68020. This is the problem mentioned in the introduction; if all access cycles had to be performed in this manner, then the processor would face a wait state every access cycle. As will be shown later, this wait state can be eliminated if the next address is from the same row.

Notice also, at the end of this sequence, the $\overline{RAS}$ and $\overline{CAS}$ output signals are left active low. Here we are making the assumption that the next access cycle will be a high-speed access. We will not know if this assumption is true until the next address is presented by the 68020. At that time, the ALS6310 will signal the timing controller if it can execute a high-speed access.

HIGH-SPEED ACCESS SEQUENCE

For a high-speed access sequence to be executed, two conditions must be met. The $\overline{RAS}$ and $\overline{CAS}$ inputs must already be low, and secondly, the static column access detector must be indicating the present row is the same as the last row ($\overline{HSA}$ = L). The bank addresses must also be unchanged as detected by the ALS6310.

Figure 6 shows the timing diagram for the high-speed access sequence. Notice that no wait states are required. If the assumption is made that the majority of memory references are sequential, then this sequence will be the one typically used. In other words, this sequence is similar to accessing data from a static RAM, or just like taking data from cache.

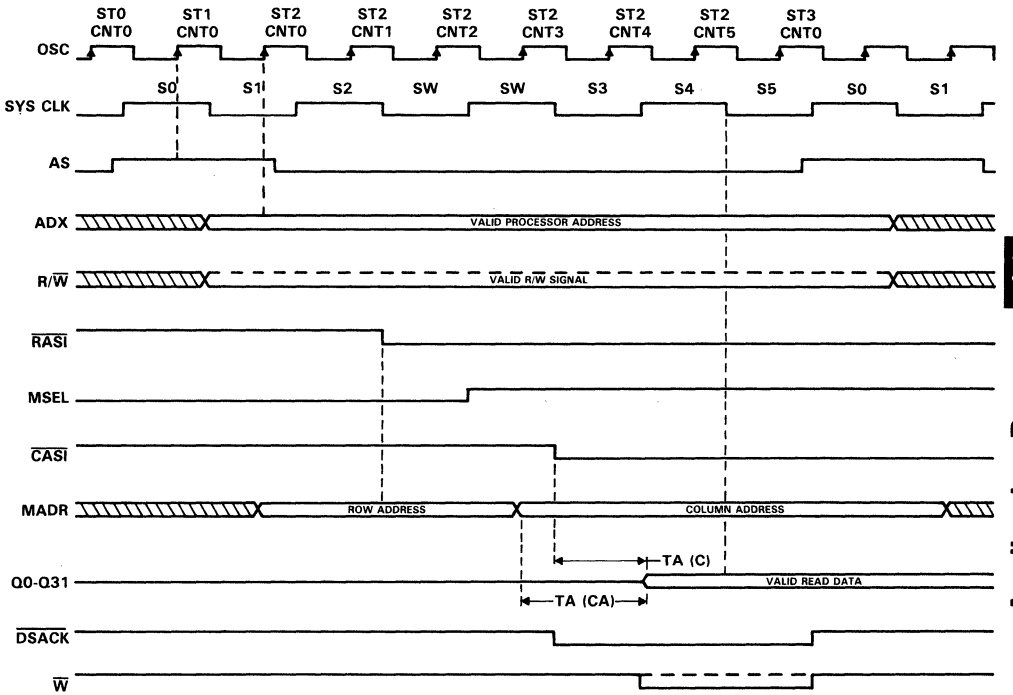


Figure 5. Normal Access Cycle

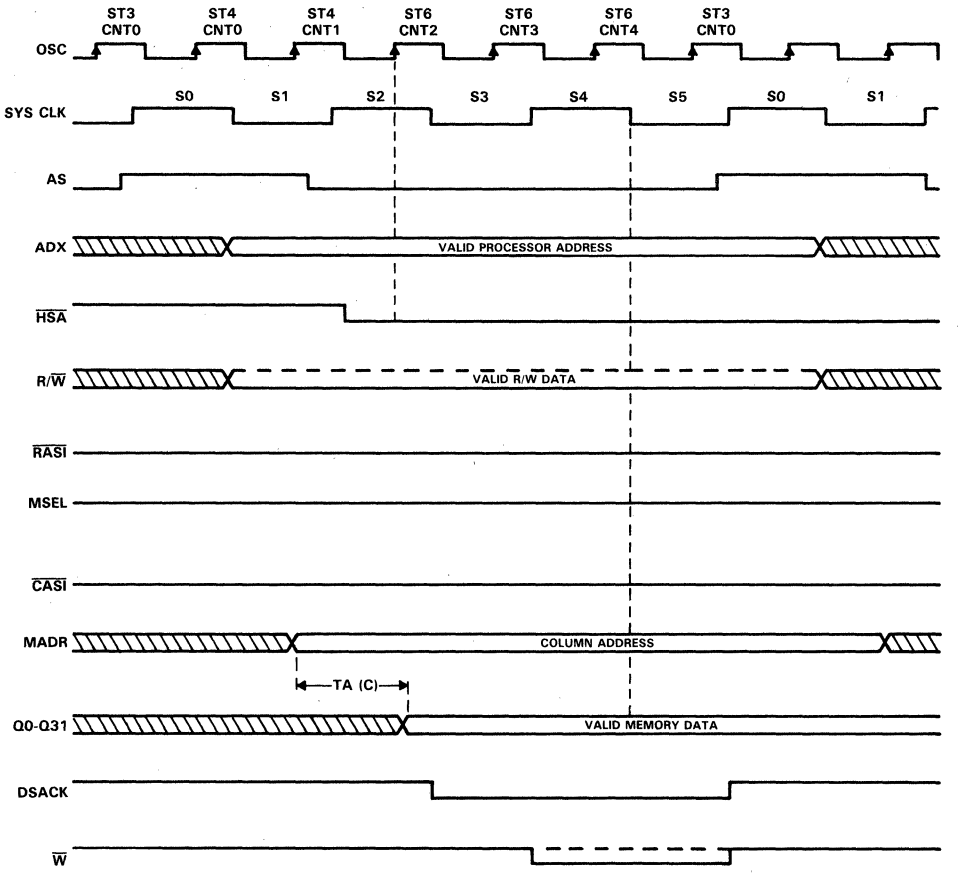


Figure 6. High-Speed Access Cycle

EXTENDED ACCESS SEQUENCE

The extended access sequence is executed if the ALS6310 detects a difference between the present, and last row addresses.. This cycle is called extended because $\overline{RAS}$ and $\overline{CAS}$ are presently low and both must be brought high to strobe in the new row and column addresses. The precharge time of the DRAM has to be met before taking $\overline{RAS}$ and $\overline{CAS}$ low. From the timing diagram in Figure 7, it can be seen that wait states of three clock cycles are generated when executing this timing sequence.

In systems where sequential data is not the general rule, it would be more efficient to execute only normal access sequences, since this generates fewer wait states. The system designer must understand what type of memory accesses will be used. For example, the designer may want only to enter the high-speed access portion of the flow chart when the system is performing DMA access cycles.

NORMAL/EXTENDED REFRESH SEQUENCES

Figures 8 and 9 show the timing diagrams for the normal and extended refresh sequences. The refresh sequence selected is a function of the present condition of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ and $\overline{CAS}$ are presently low, an extended refresh cycle is performed. If $\overline{RAS}$ and $\overline{CAS}$ are presently high, a normal refresh cycle is executed. At the end of each refresh sequence, the controller checks to see if an access request has been generated. If there has been an access request, the controller will perform an access grant sequence at the end of the refresh cycle before returning to normal process flow.

Referring back to Figure 1, there is a maximum time that $\overline{RAS}$ and $\overline{CAS}$ can be held low, $t_w(RL)P$. For the TMS4C1027, $t_w(RL)P$ must not exceed 100 μs. Since our refresh timer forces a refresh cycle every 15.5 μs, $t_w(RL)P$ cannot be violated. If the designer chooses to use a different refresh scheme, then $t_w(RL)P$ must be considered.

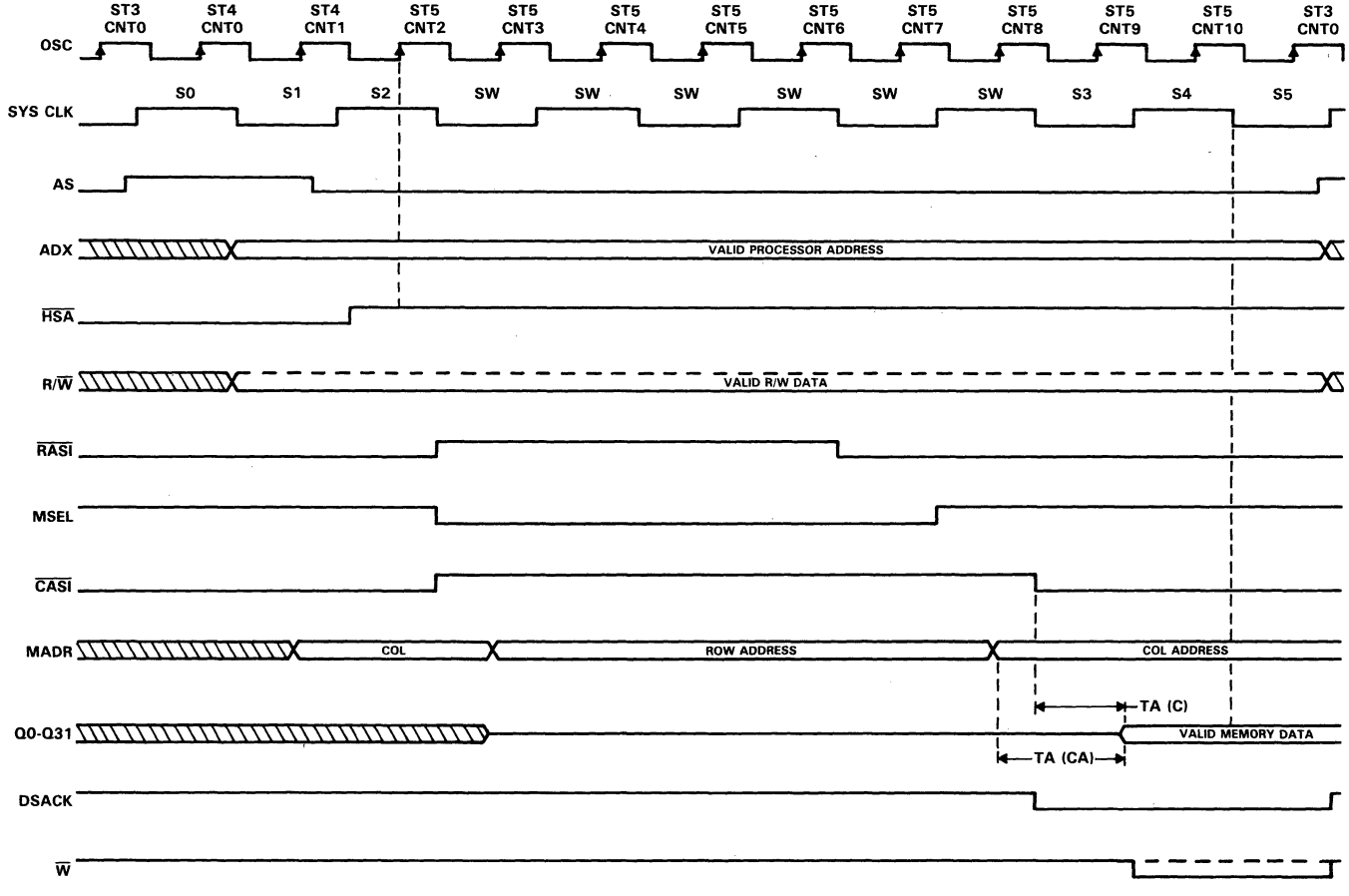


Figure 7. Extended Access Cycle

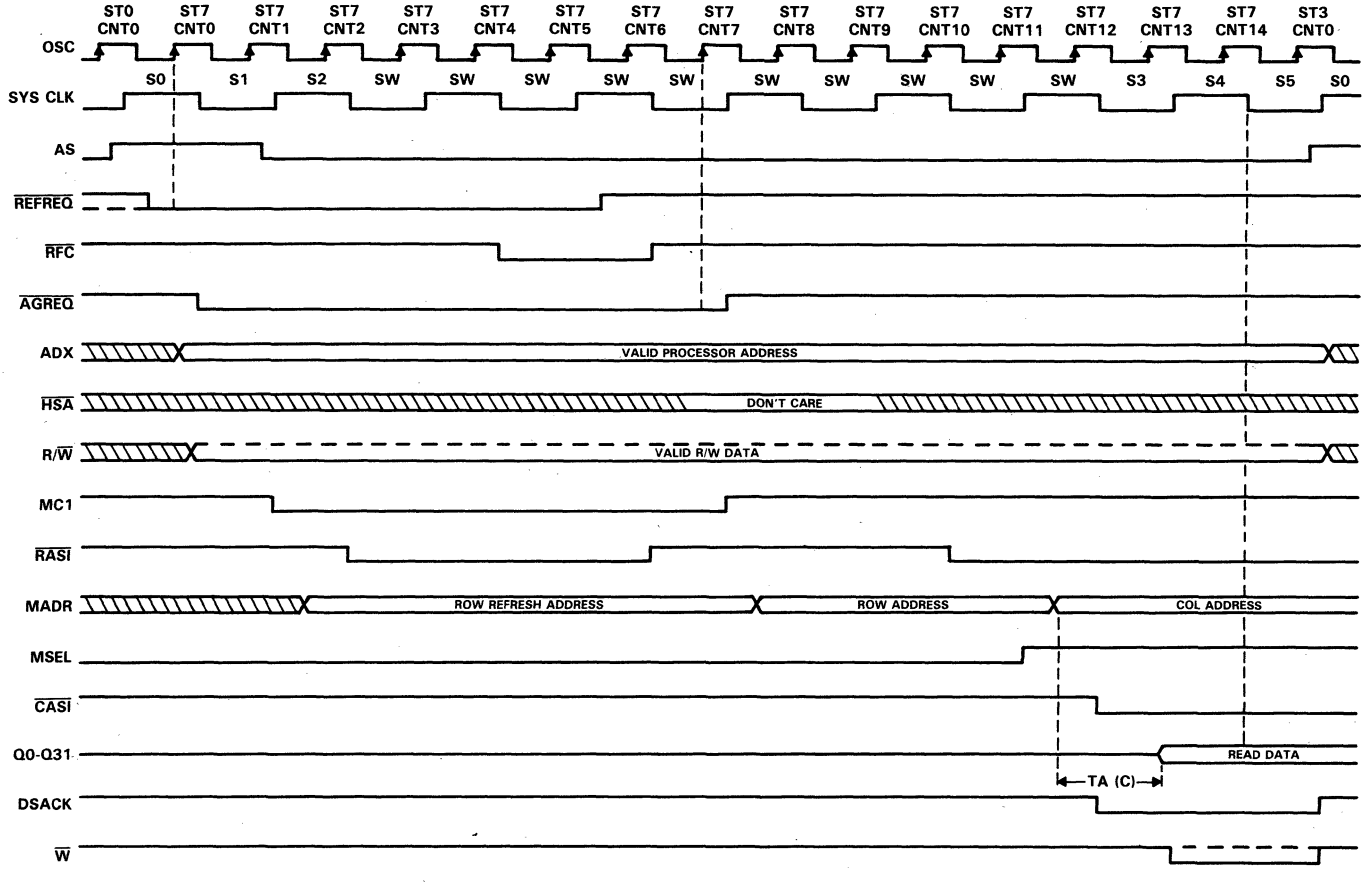


Figure 8. Normal Refresh/Access Grant Cycle

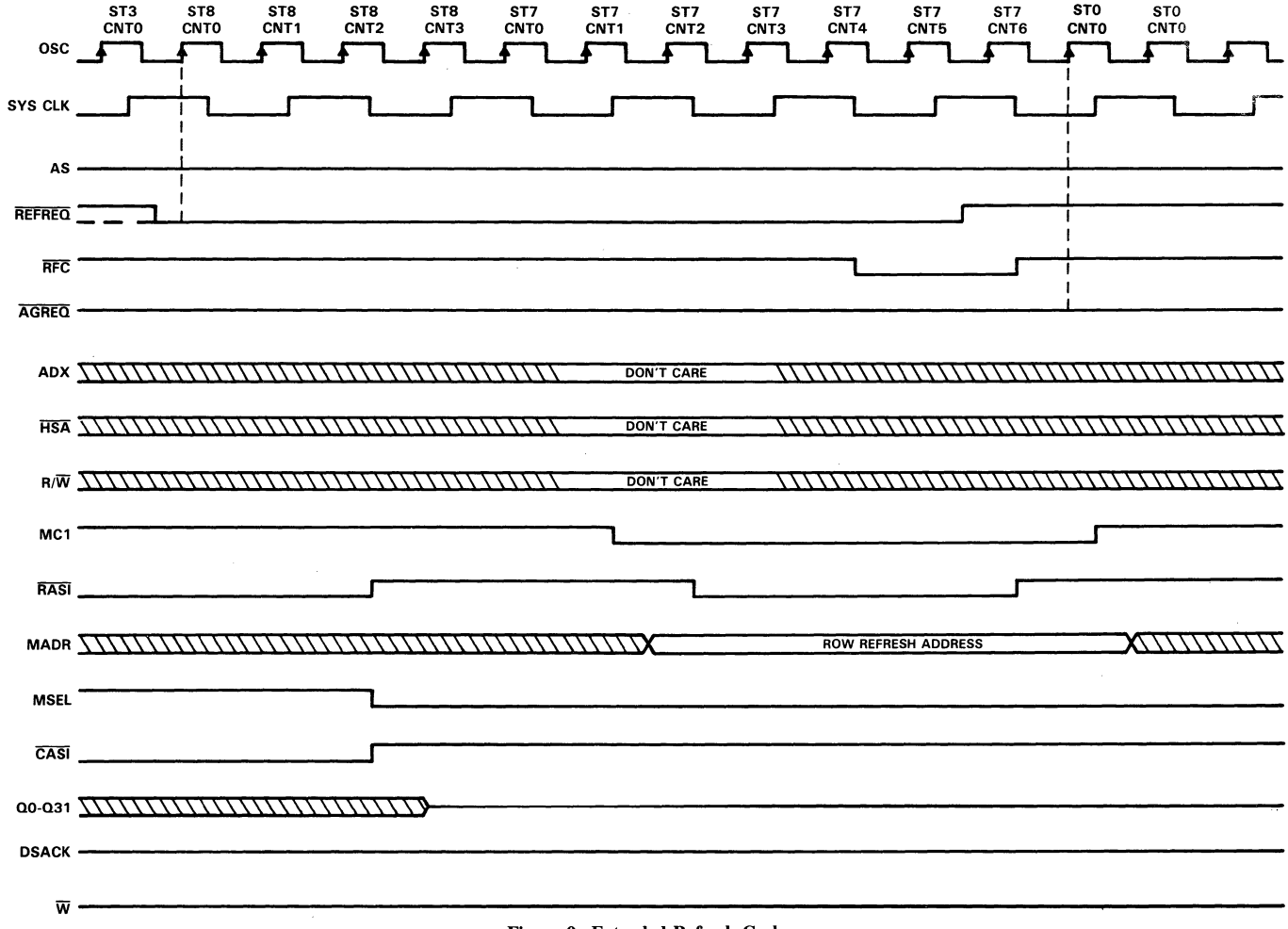


Figure 9. Extended Refresh Cycle

SOFTWARE SUPPORT

The PSG507 is supported by two software packages. CUPL which was created by and is supported by Assisted Technologies, a division of Personal CAD Systems Inc. and ABEL which was created by and is supported by FutureNet a division of Data I/O Corp. Both of these software packages have been used to reduce equations and to generate the fusemap necessary to program the PSG507. Appendices A and B show the ABEL™ and CUPL™ source files for the described static column memory timing controller are attached to assist the designer in programming the PSG507.

Since only 54% (43 out of 80) of the PG507's product terms were used in this design, it will be easy to modify or add to the sequences used to meet specific system requirements. For detailed information on designing with the PSG507 see "A Designer's Guide to the PSG507" application report.

SUMMARY

Static column decode offers the system designer a method for improving system performance in applications where the microprocessor can outperform conventional DRAM access times. By utilizing the ALS6310 "Static Column Access Detector", the ALS6300 "Refresh Timer", and the TIBPSG507 "Programmable Sequence Generator" a high performance memory timing controller can be easily developed to take full advantage of static column decode.

APPENDIX A

```
module SCDECODE
title  'ABEL EXAMPLE FOR THE STATIC COLUMN DECODER
                JOSH PEPRAH, TEXAS INSTRUMENTS, OCT 29, 1987'

      DECODE device 'F507';

" Input pin assignments
OSC           pin   1;                        " OSCILLATOR
RESET         pin   2;                        " SYSTEM RESET - WHEN LOW
A22           pin   3;                        " IO/MEMORY - MEMORY ACCESS
RW            pin   4;                        " READ / WRITE ENABLE
REFREQ        pin   5;                        " REFRESH REQUEST
AS            pin   6;                        " ADDR STROBE - ACCESS REQ
HSA           pin   7;                        " HIGH SPEED ACCESS
SYSCLK        pin  17;                        " SYSTEM CLOCK - (OSC/2)

" Output pin and node assignments
RFC           pin   8;  RFC_r    node 47;   " REFRESH COMPLETE
RASI          pin   9;  RASI_r   node 48;   " ROW ADDRESS STROBE
MSEL          pin  10;  MSEL_r   node 49;   " MULTIPLEXER SELECT
CASI          pin  11;  CASI_r   node 50;   " COLUMN ADDRESS STROBE
MC1           pin  13;  MC1_r    node 51;   " MODE CONTROL
W             pin  14;  W_r                  node 52;   " WRITE
DSACK         pin  15;  DSACK_r  node 53;   " DATA STROBE ACKNOWLEDGE


" Internal counter bits & control, and state reg - node declarations
C0,C1,C2,C3,C4,C5  node 55,56,57,58,59,60;
SCLR0         node 25;
CNTHOLD0 node 28;
CNTHOLD1 node 29;  CNTHOLD1_r node 30; " COUNT/HOLD CONTROL REGISTER

" Buried state registers - node declarations

P0     node 31;  P0_r       node 39;       " STATE REGISTER
P1     node 32;  P1_r       node 40;       " STATE REGISTER
P2     node 33;  P2_r       node 41;       " STATE REGISTER
P3     node 34;  P3_r       node 42;       " STATE REGISTER
AGREQ  node 35; AGREQ_r node 43;       " ACCESS GRANT REQUEST STATUS REGISTER

" Set notation is used to represent control, buried state, and output
" registers. This is done to simplify the equations.  The following
" sets are in the form;  register name_ = [set input, reset input]. Note
" that the ouput register pin name specifies the set input.

RFC_              = [RFC, RFC_r];
RASI_             = [RASI, RASI_r];
MSEL_             = [MSEL, MSEL_r];
CASI_             = [CASI, CASI_r];
MC1_              = [MC1, MC1_r];
W_                = [W, W_r];
DSACK_            = [DSACK, DSACK_r];
AGREQ_            = [AGREQ, AGREQ_r];
```

```
" Intermediate declarations for simplification.
" The sets 'high' and 'low' are used to set or reset the S/R
" registers.  Example: RASI_ := high & RESET; will cause pin 9
" to go high on the next clock edge if input pin 6 is high.

high            = [ 1,  0];
low             = [ 0,  1];
COUNT           = [C3,C2,C1,C0];
STATE_          = [P3,P2,P1,P0];              " STATE REGISTER SET DEFINED
H,L,clk,X   = 1, 0, .C., .X.;

equations

enable RFC  = 1;  "outputs always enabled, pin 17 is only an input

" Initialization when RESET is low
    [RASI,CASI,RFC,W,AGREQ,DSACK,MC1,SCLR0] := !RESET;
    [MSEL_r,P0_r,P1_r,P2_r,P3_r]             := !RESET;

" Counter controls defined

SCLR0           =  !RESET
                  # (STATE_==2) & (COUNT==5)
                  # (STATE_==4) & (COUNT==0) & A22
                  # (STATE_==5) & (COUNT==10)
                  # (STATE_==6) & (COUNT==4)
                  # (STATE_==7) & (COUNT==6) & (A22 # AGREQ)
                  # (STATE_==7) & (COUNT==14)
                  # (STATE_==8) & (COUNT==3);

CNTHOLD1   :=  !RESET
                  # (STATE_==2) & (COUNT==5)
                  # (STATE_==4) & (COUNT==0) & A22
                  # (STATE_==5) & (COUNT==10)
                  # (STATE_==6) & (COUNT==4)
                  # (STATE_==7) & (COUNT==6) & (A22 # AGREQ)
                  # (STATE_==7) & (COUNT==14)
                  # (STATE_==8) & (COUNT==3);

CNTHOLD1_r := (STATE_==0) & !REFREQ & RESET
                  # (STATE_==1) & !A22 & RESET
                  # (STATE_==3) & !REFREQ & RESET
                  # (STATE_==3) &  REFREQ &  AS & SYSCLK & RESET;

" Execution of access and refresh sequences
state_diagram STATE_
   State 0:                                                    " NEXT
                                                               " STATE
                                 case
                                  !RESET                                  : 0;
                                   REFREQ & (!AS  # !SYSCLK)          : 0;
                                   REFREQ &  AS & SYSCLK & RESET      : 1;
                                  !REFREQ &  RESET                        : 7;
                                 endcase;
```

```
" NORMAL ACCESS CYCLE

   State 1:                                                    " NEXT
                          case                                 " STATE
                            (COUNT==0) & !A22                 : 2;
                            (COUNT==0) &  A22                 : 0;
                          endcase;

   State 2:
                          RASI_ := (COUNT==0)  & low  & RESET;
                          MSEL_ := (COUNT==1)  & high;
                          CASI_ := (COUNT==2)  & low  & RESET;
                         DSACK_ := (COUNT==2)  & low  & RESET;
                            W_  := (COUNT==3)  & low  & RESET;
                            W_  := (COUNT==5)  & high;
                         DSACK_ := (COUNT==5)  & high;
                        if (COUNT==5) then 3 else 2;

"HOLDING STATE
   State 3:                                                    " NEXT
                          case                                 " STATE
                        (!AS # !SYSCLK) & REFREQ & RESET     : 3;
                          REFREQ &  AS & SYSCLK & RESET      : 4;
                         !REFREQ & RESET                                : 8;
                          endcase;

   State 4:
                         CASI_  := (COUNT==0)  &  high &  A22;
                         RASI_  := (COUNT==0)  &  high &  A22;
                         MSEL_  := (COUNT==0)  &  low  &  A22;
                         RASI_  := (COUNT==1)  &  high &  HSA;
                         DSACK_ := (COUNT==1)  &  low  & !HSA;
                         MSEL_  := (COUNT==1)  &  low  &  HSA;
                         CASI_  := (COUNT==1)  &  high &  HSA;

                                                                        " NEXT
                          case                                 " STATE
                            (COUNT==0) &  A22  & RESET        : 0;
                            (COUNT==0) & !A22  & RESET        : 4;
                            (COUNT==1) &  HSA  & RESET        : 5;
                            (COUNT==1) & !HSA  & RESET        : 6;
                          endcase;

"EXTENDED ACCESS CYCLE
   State 5:
                          RASI_ := (COUNT==5)  & low & RESET;
                          MSEL_ := (COUNT==6)  & high & RESET;
                          CASI_ := (COUNT==7)  & low & RESET;
                         DSACK_ := (COUNT==7)  & low & RESET;
                                   W_  := (COUNT==8)  & low & RESET;
                                   W_  := (COUNT==10) & high;
                         DSACK_ := (COUNT==10) & high;
                            if (COUNT==10) & RESET then 3 else 5;
```

```
"HIGH SPEED ACCESS
   State 6:
                                    W_ := (COUNT==2)  & low & RESET;
                                    W_ := (COUNT==4)  & high;
                                DSACK_ := (COUNT==4)  & high;
                                   if (COUNT==4) then 3 else 6;

"NORMAL REFRESH CYCLE
   State 7:
                                AGREQ_ := AS           & low  & RESET;
                                 MC1_ := (COUNT==0)  & low  & RESET;
                                RASI_ := (COUNT==1)  & low  & RESET;
                                 RFC_ := (COUNT==3)  & low  & RESET;
                                 RFC_ := (COUNT==5)  & high;
                                RASI_ := (COUNT==5)  & high;
                                 MC1_ := (COUNT==6)  & high;
                                RASI_ := (COUNT==9)  & low  & RESET;
                                MSEL_ := (COUNT==10) & high & RESET;
                                CASI_ := (COUNT==11) & low  & RESET;
                                DSACK_ := (COUNT==11) & low  & RESET;
                                        W_ := (COUNT==12) & low  & RESET;
                                        W_ := (COUNT==14) & high;
                                DSACK_ := (COUNT==14) & high;
                                if (COUNT==6) & (A22 # AGREQ) then 0 else 7;
                                if (COUNT==14) then 3 else 7;

"EXTENDED REFRESH CYCLE
   State 8:
                                 RASI_ := (COUNT==1)  & high;
                                 MSEL_ := (COUNT==1)  & low ;
                                 CASI_ := (COUNT==1)  & high;
                                 if (COUNT==3) then 7 else 8;


test_vectors  'NORMAL ACCESS CYCLE'

([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,       L , X , X,  X              , X, X ,   X  ,  X  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0       ];
 [clk,       H , X , X,  H              , L, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0       ];
 [clk,       H , X , X,  H              , H, X ,   H  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  1       ];
 [clk,       H , L , X,  X              , X, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  2       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  0  ] -> [ H ,  L ,  L ,  H , H ,H,  H  ,  2       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  1  ] -> [ H ,  L ,  H ,  H , H ,H,  H  ,  2       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  2  ] -> [ H ,  L ,  H ,  L , H ,H,  L  ,  2       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  3  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  2       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  4  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  2       ];
 [clk,       H , X , X,  X              , X, X ,   X  ,  5  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  3       ];

test_vectors  'HOLDING STATE 4 WITH EXTENDED ACCESS REQUEST'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,       H , H , X,  H              , H, X ,   H  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  4       ];
 [clk,       H , L , X,  X              , X, X ,   X  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  4       ];
 [clk,       H , X , X,  X              , X, H ,   X  ,  1  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  5       ];
```

```
test_vectors  'EXTENDED ACCESS'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,      H , X , X,  X            , X, X ,   X  ,  2  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  5      ];
 [clk,      H , X , X,  X            , X, X ,   X  ,  3  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  5      ];
 [clk,      H , X , X,  X            , X, X ,   X  ,  4  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  5      ];
 [clk,      H , X , X,  X            , X, X ,   X  ,  5  ] -> [ H ,  L ,  L ,  H , H ,H,  H  ,  5      ];
 [clk,      H , X , X,  X            , X, X ,   X  ,  6  ] -> [ H ,  L ,  H ,  H , H ,H,  H  ,  5      ];
 [clk,      H , X , X,  X            , X, X ,   X  ,  7  ] -> [ H ,  L ,  H ,  L , H ,H,  L  ,  5      ];
 [clk,      H , X , X,  X            , X, X ,   X  ,  8  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  5      ];
 [clk,      H , X , X,  X            , X, X ,   X  ,  9  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  5      ];
 [clk,      H , X , X,  X            , X, X ,   X  , 10  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  3      ];

test_vectors  'HOLDING STATE 4 WITH HIGH SPEED ACCESS REQUEST'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,      H , H , X,  H            , H, X ,   H  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  4      ];
 [clk,      H , L , X,  X            , X, X ,   X  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  4      ];
 [clk,      H , L , X,  X            , X, L ,   X  ,  1  ] -> [ H ,  L ,  H ,  L , H ,H,  L  ,  6      ];

test_vectors  'HIGH SPEED ACCESS'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,      H , X , X,  X            , X, X ,   X  ,  2  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  6      ];
 [clk,      H , X , X,  X            , X, X ,   X  ,  3  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  6      ];
 [clk,      H , X , X,  X            , X, X ,   X  ,  4  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  3      ];

test_vectors  'NON-MEMORY ACCESS FOLLOWED BY REFRESH REQUEST'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,      H , H , X,  H            , H, X ,   H  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  4      ];
 [clk,      H , H , X,  X            , X, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0      ];
 [clk,      H , X , X,  H            , L, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0      ];
 [clk,      H , X , X,  H            , X, X ,   L  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0      ];
 [clk,      H , X , X,  L            , X, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  7      ];

test_vectors  'NORMAL REFRESH CYCLE'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,      H , X , X,  X            , L, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , L ,H,  H  ,  7      ];
 [clk,      H , X , X,  X            , L, X ,   X  ,  1  ] -> [ H ,  L ,  L ,  H , L ,H,  H  ,  7      ];
 [clk,      H , X , X,  X            , L, X ,   X  ,  2  ] -> [ H ,  L ,  L ,  H , L ,H,  H  ,  7      ];
 [clk,      H , X , X,  X            , L, X ,   X  ,  3  ] -> [ L ,  L ,  L ,  H , L ,H,  H  ,  7      ];
 [clk,      H , X , X,  X            , L, X ,   X  ,  4  ] -> [ L ,  L ,  L ,  H , L ,H,  H  ,  7      ];
 [clk,      H , X , X,  H            , L, X ,   X  ,  5  ] -> [ H ,  H ,  L ,  H , L ,H,  H  ,  7      ];
 [clk,      H , X , X,  X            , L, X ,   X  ,  6  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0      ];
```

```
test_vectors  'NORMAL REFRESH CYCLE FOLLOWED BY ACCESS GRANT REQUEST'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
[clk,  H  , X , X,  L      , X, X ,   X  ,  0  ] -> [ H ,          H ,  L ,  H , H ,H,  H      ,  7   ];
[clk,  H  , X , X,  X      , L, X ,   X  ,  0  ] -> [ H ,          H ,  L ,  H , L ,H,  H      ,  7   ];
[clk,  H  , X , X,  X      , L, X ,   X  ,  1  ] -> [ H ,          L ,  L ,  H , L ,H,  H      ,  7   ];
[clk,  H  , X , X,  X      , H, X ,   X  ,  2  ] -> [ H ,          L ,  L ,  H , L ,H,  H      ,  7   ];
[clk,  H  , X , X,  X      , H, X ,   X  ,  3  ] -> [ L ,          L ,  L ,  H , L ,H,  H      ,  7   ];
[clk,  H  , X , X,  X      , L, X ,   X  ,  4  ] -> [ L ,          L ,  L ,  H , L ,H,  H      ,  7   ];
[clk,  H  , L , X,  H      , L, X ,   X  ,  5  ] -> [ H ,          H ,  L ,  H , L ,H,  H      ,  7   ];
[clk,  H  , L , X,  X      , L, X ,   X  ,  6  ] -> [ H ,          H ,  L ,  H , H ,H,  H      ,  7   ];
[clk,  H  , L , X,  X      , L, X ,   X  ,  7  ] -> [ H ,          H ,  L ,  H , H ,H,  H      ,  7   ];
[clk,  H  , L , X,  X      , L, X ,   X  ,  8  ] -> [ H ,          H ,  L ,  H , H ,H,  H      ,  7   ];
[clk,  H  , L , X,  X      , L, X ,   X  ,  9  ] -> [ H ,          L ,  L ,  H , H ,H,  H      ,  7   ];
[clk,  H  , L , X,  X      , L, X ,   X  , 10  ] -> [ H ,          L ,  H ,  H , H ,H,  H      ,  7   ];
[clk,  H  , L , X,  X      , L, X ,   X  , 11  ] -> [ H ,          L ,  H ,  L , H ,H,  L      ,  7   ];
[clk,  H  , L , X,  X      , L, X ,   X  , 12  ] -> [ H ,          L ,  H ,  L , H ,L,  L      ,  7   ];
[clk,  H  , L , X,  X      , L, X ,   X  , 13  ] -> [ H ,          L ,  H ,  L , H ,L,  L      ,  7   ];
[clk,  H  , L , X,  X      , L, X ,   X  , 14  ] -> [ H ,          L ,  H ,  L , H ,H,  H      ,  3   ];

test_vectors  'HOLDING STATE 3 WITH EXTENDED REFRESH REQUEST'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,       H  , X , X,  H            , X, X ,   L  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  3      ];
 [clk,       H  , X , X,  H            , L, X ,   X  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  3      ];
 [clk,       H  , X , X,  L            , X, X ,   X  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  8      ];

test_vectors  'EXTENDED REFRESH CYCLE'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE_])
 [clk,       H  , X , X,  X            , X, X ,   X  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  8      ];
 [clk,       H  , X , X,  X            , X, X ,   X  ,  1  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  8      ];
 [clk,       H  , X , X,  X            , X, X ,   X  ,  2  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  8      ];
 [clk,       H  , X , X,  X            , X, X ,   X  ,  3  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  7      ];


end SCDECODE
```

APPENDIX B

```
NAME      SCDECODE;
PARTNO    T10004;
DATE      05/07/87 ;
REV       01 ;
DESIGNER  Breuninger/Peprah;
COMPANY   Texas Instruments;
ASSEMBLY  None ;
LOCATION  Dallas;

/*************************************************************************************/
/*   Static Column Decode                                                            */
/*                                                                                   */
/*                                                                                   */
/*       This is an example of how the PSG507 can be used to generate the            */
/*   required memory timing control signals (RAS, CAS, MSEL etc) for static          */
/*   column decode implementation using the ALS6301, ALS6310 and the ALS630          */
/*   ALS6300, in a system environment.                                               */
/*                                                                                   */
/*                                                                                   */
/*************************************************************************************/
/*   Allowable Target Device Types :  TEXAS INTSRUMENTS  PSG507                      */
/*************************************************************************************/

/**  Inputs  **/

pin  1          =  OSC      ;          /* Oscillator                          */
pin  2          =  RESET    ;          /* System Reset - when low             */
pin  3          =  A22      ;          /* IO/!M - Memory access               */
pin  4          =  RW       ;          /* Read / Write  Enable                */
pin  5          =  REFREQ   ;          /* Refresh Request                     */
pin  6          =  AS       ;          /* Addr Strobe - access request        */
pin  7          =  HSA      ;          /* High Speed Access                   */
pin 18          =  SYSCLK   ;          /* System Clock - (OSC/2)              */

/**  Outputs  **/

pin  8          =  RFC      ;          /* Refresh Complete                    */
pin  9          =  RASI     ;          /* Row Address Strobe                  */
pin 10          =  MSEL     ;          /* Multiplexer Select                  */
pin 11          =  CASI     ;          /* Column Address Strobe               */
pin 13          =  MC1_     ;          /* Mode Control                        */
pin 14          =  W        ;          /* Write                               */
pin 15          =  DSACK    ;          /* Data Strobe Acknowledge             */

/** Node Declarations **/
pinnode [33..38] = [C0..5]  ;          /* Built-in 6-Bit counter              */
pinnode 39       = SCLR0    ;          /* Counter Cclear- non registered      */
pinnode 41       = CNTHOLD0 ;          /* Counter Hold - non registered       */
pinnode 42       = CNTHOLD1 ;          /* Counter Hold - registered           */
node               [P3..0]  ;          /* Buried State Registers              */
node               AGREQ    ;          /* Access Grant Request                */
```

```
/** Declarations and Intermediate Variable Definition **/
field COUNT      = [C5..0]   ;
field STATE      = [P3..0]   ;
$define ST0       'b'0000
$define ST1       'b'0001
$define ST2       'b'0010
$define ST3       'b'0011
$define ST4       'b'0100
$define ST5       'b'0101
$define ST6       'b'0110
$define ST7       'b'0111
$define ST8       'b'1000

/* BUILT-IN COUNTER CONTROL EQUATIONS */

SCLR0        = !RESET                          /* Clear counter when RESET is low        */
             # ST2 & COUNT:'d'5                /* and during transitions at the end      */
             # ST4 & COUNT:'d'0                /* the indicated states and counts.       */
             # ST5 & COUNT:'d'10               /*                                        */
             # ST6 & COUNT:'d'4                /*                                        */
             # ST7 & COUNT:'d'6 & (A22 & AGREQ)  /*                                      */
             # ST7 & COUNT:'d'14               /*                                        */
             # ST8 & COUNT:'d'3;               /*                                        */

CNTHOLD1.s   = !RESET                          /* Set count hold while clearing          */
             # ST2 & COUNT:'d'5                /* the counters accordingly.              */
             # ST4 & COUNT:'d'0                /*                                        */
             # ST5 & COUNT:'d'10               /*                                        */
             # ST6 & COUNT:'d'4                /*                                        */
             # ST7 & COUNT:'d'6 & (A22 & AGREQ)  /*                                      */
             # ST7 & COUNT:'d'14               /*                                        */
             # ST8 & COUNT:'d'3;               /*                                        */

 CNTHOLD1.r  = ST0 & !REFREQ & RESET           /* Reset count hold on transition to ST7  */
             # ST1 & !A22 & RESET              /* Reset count hold on transition to ST2  */
             # ST3 & !REFREQ & RESET           /* Reset count hold on transition to ST8  */
             # ST3 &  REFREQ &  AS             /* Reset count hold on transition to ST4  */
                  & SYSCLK & RESET;

/** State Machine Equations **/
sequence STATE {
present ST0:
       if(REFREQ & (!AS  # !SYSCLK))       next ST0;
       if(REFREQ &  AS & SYSCLK & RESET)   next ST1;
       if(!REFREQ &  RESET)                next ST7;
       default                             next ST0;

present ST1:
       if(COUNT:'d'0 & !A22)               next ST2;
       if(COUNT:'d'0 &  A22)               next ST0;
       default                             next ST1;

present ST2:
       /* NORMAL ACCESS CYCLE */
       if(COUNT:'d'0) &  RESET             next ST2 out !RAS1;
       if(COUNT:'d'1)                      next ST2 out  MSEL;
       if(COUNT:'d'2) & RESET              next ST2 out [!CAS1,!DSACK];
       if(COUNT:'d'3) & RESET              next ST2 out !W;
       if(COUNT:'d'5)                      next ST3 out [W,DSACK];
       default                             next ST2;
```

```
present ST3:
        /* HOLDING STATE    */
        if(!AS # !SYSCLK) & REFREQ & RESET    next ST3;
        if(REFREQ &  AS & SYSCLK & RESET)     next ST4;
        if(!REFREQ & RESET)                   next ST8;
        default                               next ST3;

present ST4:
        if(COUNT:'d'0) & A22 & RESET          next ST0 out [RASI,!MSEL,CASI];
        if(COUNT:'d'0) & !A22 & RESET         next ST4;
        if(COUNT:'d'1) & HSA & RESET          next ST5 out [RASI,!MSEL,CASI];
        if(COUNT:'d'1) & !HSA & RESET         next ST6 out !DSACK;
        default                               next ST4;

present ST5:
        /* EXTENDED ACCESS CYCLE */
        if(COUNT:'d'5) & RESET                next ST5 out !RASI;
        if(COUNT:'d'6) & RESET                next ST5 out  MSEL;
        if(COUNT:'d'7) & RESET                next ST5 out [!CASI,!DSACK];
        if(COUNT:'d'8) & RESET                next ST5 out !W;
        if(COUNT:'d'10) & RESET               next ST3 out [W,DSACK];
        default                               next ST5;

present ST6:
        /* HIGH SPEED ACCESS    */
        if(COUNT:'d'2) & RESET                next ST6 out !W;
        if(COUNT:'d'4)                        next ST3 out [W,DSACK];
        default                               next ST6;

present ST7:
        /* NORMAL REFRESH CYCLE */
        if AS                                 next ST7 out !AGREQ;
        if(COUNT:'d'0) & RESET                next ST7 out !MCI_;
        if(COUNT:'d'1) & RESET                next ST7 out !RASI;
        if(COUNT:'d'3) & RESET                next ST7 out !RFC;
        if(COUNT:'d'5)                        next ST7 out [RFC,RASI];
        if(COUNT:'d'6) & (A22 # AGREQ)        next ST0 out  MCI_;
        if(COUNT:'d'6) & !A22 & !AGREQ        next ST7 out  MCI_;
        if(COUNT:'d'9) & RESET                next ST7 out !RASI;
        if(COUNT:'d'10) & RESET               next ST7 out  MSEL;
        if(COUNT:'d'11) & RESET               next ST7 out [!CASI,!DSACK];
        if(COUNT:'d'12) & RESET               next ST7 out !W;
        if(COUNT:'d'14)                       next ST3 out [W,DSACK];
        default                               next ST7;

present ST8:
        /* EXTENDED REFRESH CYCLE   */
        if(COUNT:'d'1)                        next ST8 out [RASI,!MSEL,CASI];
        if(COUNT:'d'3)                        next ST7;
        default                               next ST8; }

APPEND RASI.s = !RESET; APPEND CASI.s  = !RESET; APPEND RFC.s   = !RESET;
APPEND W.s    = !RESET; APPEND AGREQ.s = !RESET; APPEND DSACK.s = !RESET;
APPEND MCI_.s = !RESET; APPEND SCLR0   = !RESET; APPEND MSEL.r  = !RESET;
APPEND P0_.r  = !RESET; APPEND P1_.r   = !RESET; APPEND P2_.r   = !RESET;
APPEND P3_.r  = !RESET;
```

```
NAME     SCDECODE;
PARTNO   T10004;
DATE     05/07/87 ;
REV      01 ;
DESIGNER Breuninger/Peprah;
COMPANY  Texas Instruments;
ASSEMBLY None ;
LOCATION Dallas;

/*************************************************************************************************/
/* Static Column Decode                                                                          */
/*                                                                                               */
/*      CUPL simulation file for the Static Column Decode Application                            */
/*                                                                                               */
/*************************************************************************************************/
/*  Allowable Target Device Types :  TEXAS INTSRUMENTS  PSG507                                   */
/*************************************************************************************************/

ORDER:  OSC,%4,RESET,%4,A22,%3,RW,%3,REFREQ,%5,AS,%2,HSA,%5,SYSCLK,%3,COUNT,
        %2,RFC,%4,RASI,%4,MSEL,%4,CASI,%3,MCI_,%2,W,%3,DSACK,%4,STATE;

BASE: DECIMAL;

VECTORS:

$msg"   ";
$msg"   ";
$msg"NORMAL ACCESS CYCLE";
$msg"   ";
$msg"     ----------------- INPUT -----------------  ------------- OUTPUT -------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------- ";
          C   0   X  X  X    X  X    X   'X'   H   H   L   H  H  H  H   "0"
          C   1   X  X  1    0  X    X   '0'   H   H   L   H  H  H  H   "0"
          C   1   X  X  1    1  X    1   '0'   H   H   L   H  H  H  H   "1"
          C   1   0  X  X    X  X    X   '0'   H   H   L   H  H  H  H   "2"
          C   1   X  X  X    X  X    X   '0'   H   L   L   H  H  H  H   "2"
          C   1   X  X  X    X  X    X   '1'   H   L   H   H  H  H  H   "2"
          C   1   X  X  X    X  X    X   '2'   H   L   H   L  H  H  L   "2"
          C   1   X  X  X    X  X    X   '3'   H   L   H   L  H  L  L   "2"
          C   1   X  X  X    X  X    X   '4'   H   L   H   L  H  L  L   "2"
          C   1   X  X  X    X  X    X   '5'   H   L   H   L  H  H  H   "3"

$msg"   ";
$msg"   ";
$msg"HOLDING STATE 4 WITH EXTENDED ACCESS REQUEST";
$msg"   ";
$msg"     ----------------- INPUT -------------------  ------------- OUTPUT ------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------- ";
          C   1   1  X  1    1  X    1   '0'   H   L   H   L  H  H  H   "4"
          C   1   0  X  X    X  X    X   '0'   H   L   H   L  H  H  H   "4"
          C   1   X  X  X    X  1    X   '1'   H   H   L   H  H  H  H   "5"
```

```
$msg"   ";
$msg"   ";
$msg"EXTENDED ACCESS";
$msg"   ";
$msg"     ------------------ INPUT ------------------  ------------- OUTPUT ---------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
          C   1   X   X   X    X  X    X    '2'   H   H   L   H   H  H   H    "5"
          C   1   X   X   X    X  X    X    '3'   H   H   L   H   H  H   H    "5"
          C   1   X   X   X    X  X    X    '4'   H   H   L   H   H  H   H    "5"
          C   1   X   X   X    X  X    X    '5'   H   L   L   H   H  H   H    "5"
          C   1   X   X   X    X  X    X    '6'   H   L   H   H   H  H   H    "5"
          C   1   X   X   X    X  X    X    '7'   H   L   H   L   H  H   L    "5"
          C   1   X   X   X    X  X    X    '8'   H   L   H   L   H  L   L    "5"
          C   1   X   X   X    X  X    X    '9'   H   L   H   L   H  L   L    "5"
          C   1   X   X   X    X  X    X   '10'   H   L   H   L   H  H   H    "3"

$msg"   ";
$msg"   ";
$msg"HOLDING STATE 4 WITH HIGH SPEED ACCESS REQUEST";
$msg"   ";
$msg"     ------------------ INPUT ------------------  ------------- OUTPUT ---------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
          C   1   1   X   1    1  X    1    '0'   H   L   H   L   H  H   H    "4"
          C   1   0   X   X    X  X    X    '0'   H   L   H   L   H  H   H    "4"
          C   1   0   X   X    X  0    X    '1'   H   L   H   L   H  H   L    "6"

$msg"   ";
$msg"   ";
$msg"HIGH SPEED ACCESS";
$msg"   ";
$msg"     ------------------ INPUT ------------------  ------------- OUTPUT ---------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
          C   1   X   X   X    X  X    X    '2'   H   L   H   L   H  L   L    "6"
          C   1   X   X   X    X  X    X    '3'   H   L   H   L   H  L   L    "6"
          C   1   X   X   X    X  X    X    '4'   H   L   H   L   H  H   H    "3"

$msg"   ";
$msg"   ";
$msg"NON-MEMORY ACCESS FOLLOWED BY REFRESH REQUEST";
$msg"   ";
$msg"     ------------------ INPUT ------------------  ------------- OUTPUT ---------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
          C   1   1   X   1    1  X    1    '0'   H   L   H   L   H  H   H    "4"
          C   1   1   X   X    X  X    X    '0'   H   H   L   H   H  H   H    "0"
          C   1   X   X   1    0  X    X    '0'   H   H   L   H   H  H   H    "0"
          C   1   X   X   1    X  X    0    '0'   H   H   L   H   H  H   H    "0"
          C   1   X   X   0    X  X    X    '0'   H   H   L   H   H  H   H    "7"
```

```
$msg"   ";
$msg"   ";
$msg"NORMAL REFRESH CYCLE";
$msg"   ";
$msg"     ------------------ INPUT ------------------  -------------- OUTPUT --------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
          C   1   X   X   X    0  X    X    '0'   H   H   L   H   L  H   H    "7"
          C   1   X   X   X    0  X    X    '1'   H   L   L   H   L  H   H    "7"
          C   1   X   X   X    0  X    X    '2'   H   L   L   H   L  H   H    "7"
          C   1   X   X   X    0  X    X    '3'   L   L   L   H   L  H   H    "7"
          C   1   X   X   X    0  X    X    '4'   L   L   L   H   L  H   H    "7"
          C   1   X   X   1    0  X    X    '5'   H   H   L   H   L  H   H    "7"
          C   1   X   X   X    0  X    X    '6'   H   H   L   H   H  H   H    "0"

$msg"   ";
$msg"   ";
$msg"NORMAL REFRESH CYCLE FOLLOWED BY ACCESS GRANT REQUEST";
$msg"   ";
$msg"     ------------------ INPUT ------------------  -------------- OUTPUT --------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
          C   1   X   X   0    X  X    X    '0'   H   H   L   H   H  H   H    "7"
          C   1   X   X   X    0  X    X    '0'   H   H   L   H   L  H   H    "7"
          C   1   X   X   X    0  X    X    '1'   H   L   L   H   L  H   H    "7"
          C   1   X   X   X    1  X    X    '2'   H   L   L   H   L  H   H    "7"
          C   1   X   X   X    1  X    X    '3'   L   L   L   H   L  H   H    "7"
          C   1   X   X   X    0  X    X    '4'   L   L   L   H   L  H   H    "7"
          C   1   0   X   X    0  X    X    '5'   H   H   L   H   L  H   H    "7"
          C   1   0   X   X    0  X    X    '6'   H   H   L   H   H  H   H    "7"
          C   1   0   X   X    0  X    X    '7'   H   H   L   H   H  H   H    "7"
          C   1   0   X   X    0  X    X    '8'   H   H   L   H   H  H   H    "7"
          C   1   0   X   X    0  X    X    '9'   H   L   L   H   H  H   H    "7"
          C   1   0   X   X    0  X    X   '10'   H   L   H   H   H  H   H    "7"
          C   1   0   X   X    0  X    X   '11'   H   L   H   L   H  H   L    "7"
          C   1   0   X   X    0  X    X   '12'   H   L   H   L   H  L   L    "7"
          C   1   0   X   X    0  X    X   '13'   H   L   H   L   H  L   L    "7"
          C   1   0   X   X    0  X    X   '14'   H   L   H   L   H  H   H    "3"

$msg"   ";
$msg"   ";
$msg"HOLDING STATE 3 WITH EXTENDED REFRESH REQUEST";
$msg"   ";
$msg"     ------------------ INPUT ------------------  -------------- OUTPUT --------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MC1,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
          C   1   X   X   1    X  X    0    '0'   H   L   H   L   H  H   H    "3"
          C   1   X   X   1    0  X    X    '0'   H   L   H   L   H  H   H    "3"
          C   1   X   X   0    X  X    X    '0'   H   L   H   L   H  H   H    "8"
```

```
$msg"   ";
$msg"   ";
$msg"EXTENDED REFRESH CYCLE";
$msg"   ";
$msg"     ------------------ INPUT ------------------  -------------- OUTPUT --------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
           C   1   X  X  X    X  X    X   '0'   H   L   H   L  H  H  H    "8"
           C   1   X  X  X    X  X    X   '1'   H   H   L   H  H  H  H    "8"
           C   1   X  X  X    X  X    X   '2'   H   H   L   H  H  H  H    "8"
           C   1   X  X  X    X  X    X   '3'   H   H   L   H  H  H  H    "7"
```

General Information 1

Data Sheets 2

Application Reports 3

Mechanical Data 4

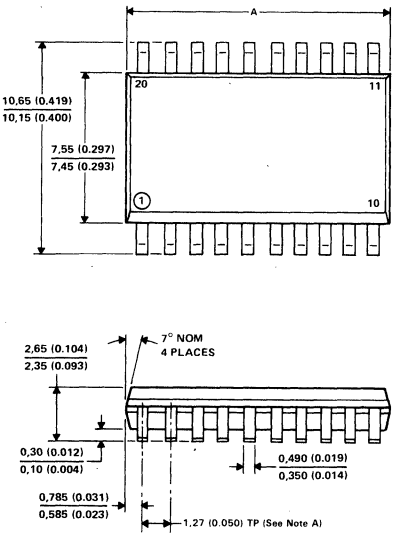
Contents

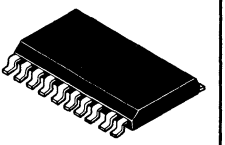
	Page
Packages	**4-3**
Sockets	**4-25**

DW plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DW PLASTIC PACKAGE
(20-pin package used for illustration)





DIM \ PINS	16	20	24	28†
A MIN	10,16	12,70	15,29	17,68
	(0.400)	(0.500)	(0.602)	(0.696)
A MAX	10,36	12,90	15,49	17,88
	(0.408)	(0.508)	(0.610)	(0.704)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

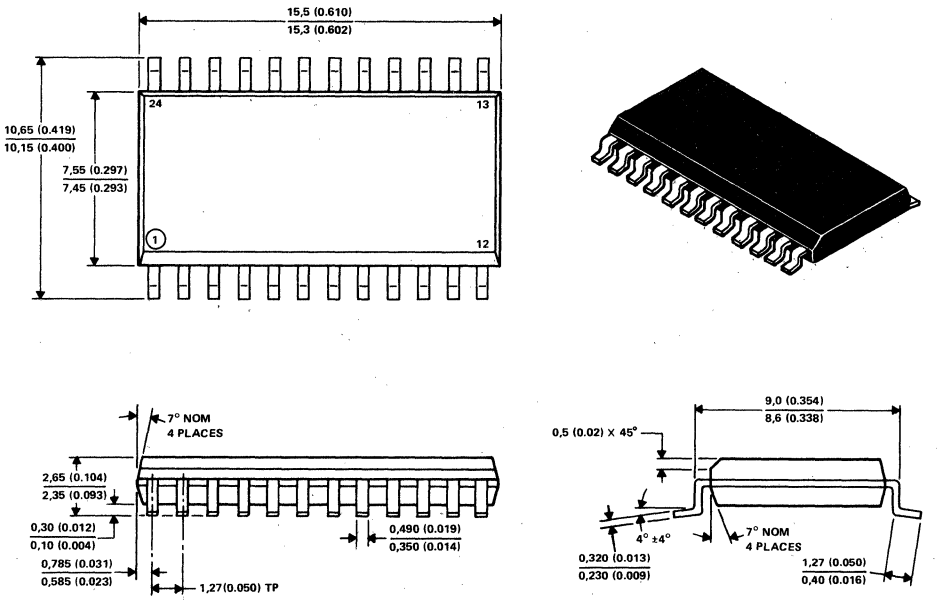
†The 28-pin package drawing is presently classified as Advance Information.

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

DW plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

24-PIN DW PACKAGE



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

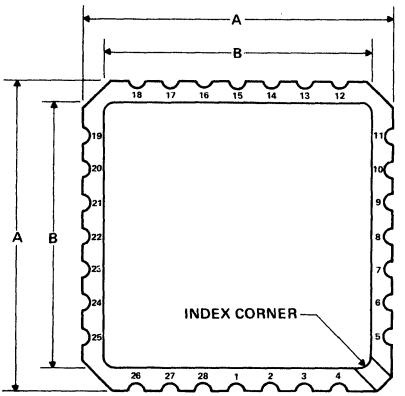
NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold flash or protrusion shall not exceed 0,15 (0.006).
C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

FK ceramic chip carrier packages

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.

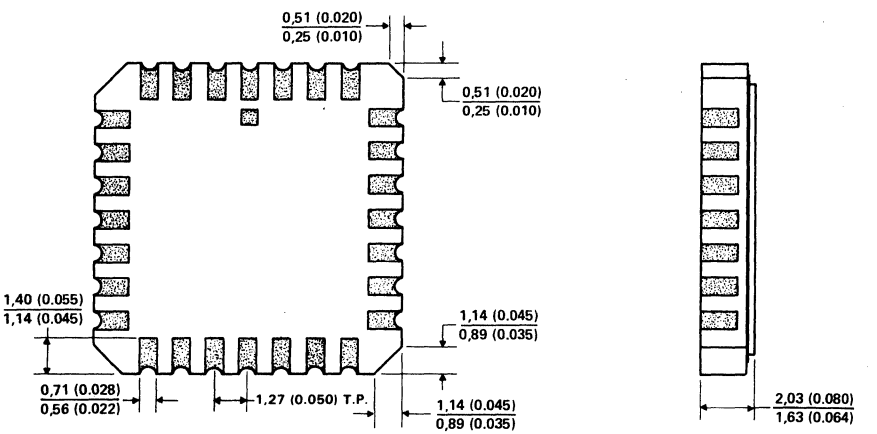
FK CERAMIC CHIP CARRIER PACKAGES
(28-terminal package shown)



CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS004CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)

*All dimensions and notes for the specified JEDEC outline apply.

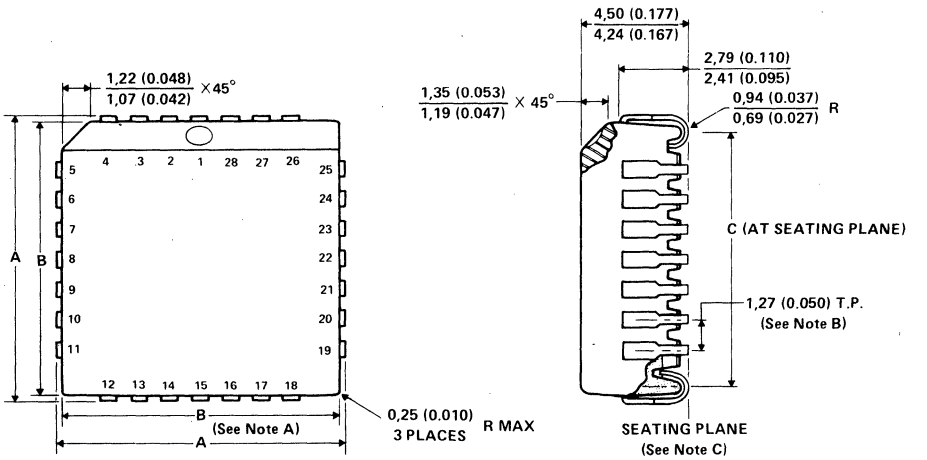


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

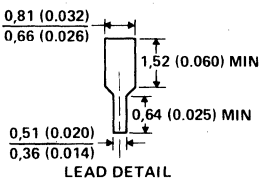
FN plastic chip carrier package

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN PLASTIC CHIP CARRIER
(28-terminal package used for illustration)



NO. OF TERMINALS	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
20	9,78 (0.385)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	7,87 (0.310)	8,38 (0.330)
28	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,41 (0.410)	10,92 (0.430)
44	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,49 (0.610)	16,00 (0.630)
68	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.956)	23,11 (0.910)	23,62 (0.930)
84	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.158)	27,69 (1.090)	28,70 (1.130)



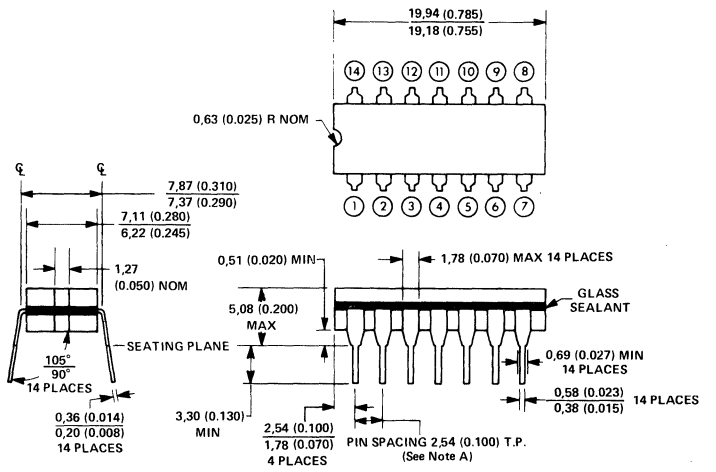
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

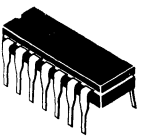
NOTES: A. Centerline of center pin each side is within 0,10 (0.004) of package centerline as determined by dimension B.
B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.
C. The lead contact points are planar within 0,10 (0.004).

J ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

14-PIN J CERAMIC





Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

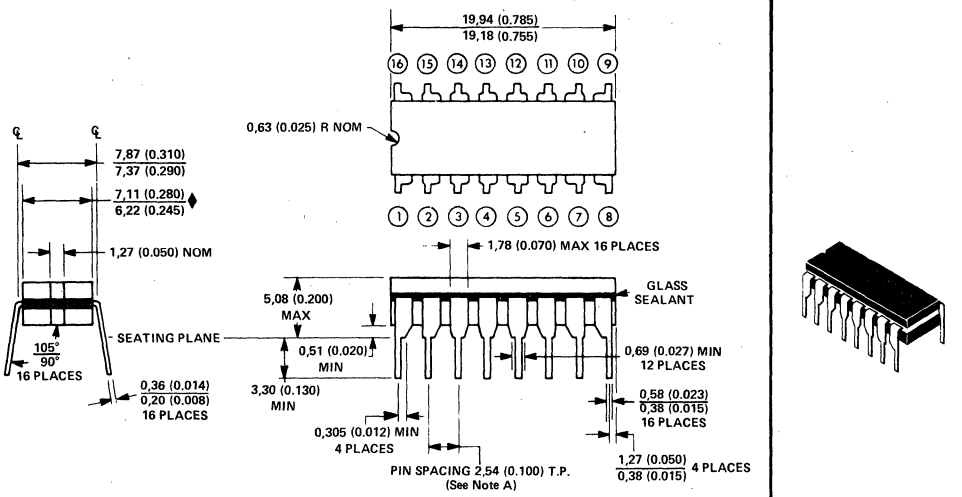
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

J ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

16-PIN J CERAMIC



♦ For memories of 64 bits and up, a few MSI/LSI products in Series 54/74 and Series 54S/74S that are derived from memory circuit bars, and complex HCMOS parts, this maximum is 7,62 (0.300). All other dimensions apply without modification.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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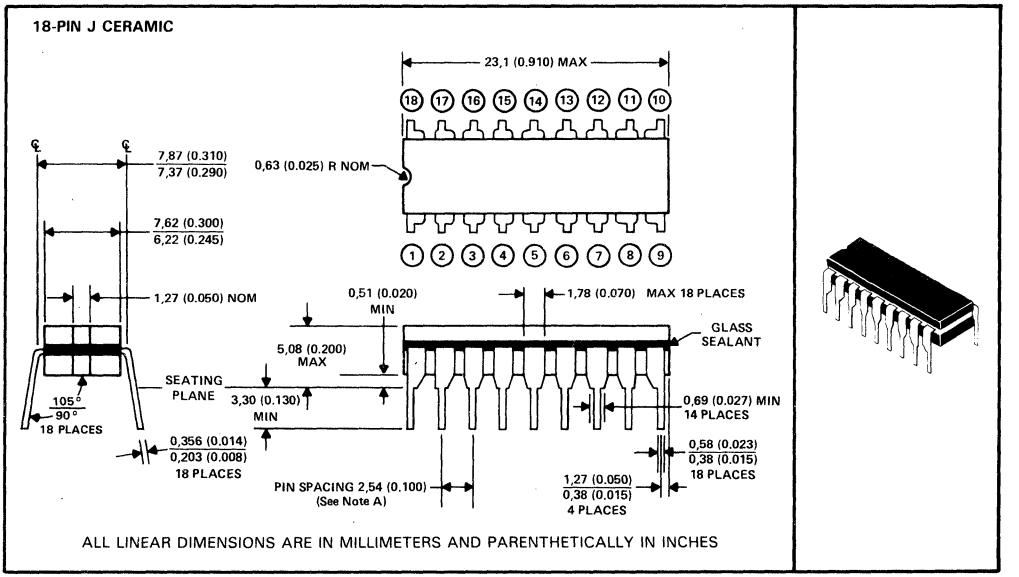
J ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

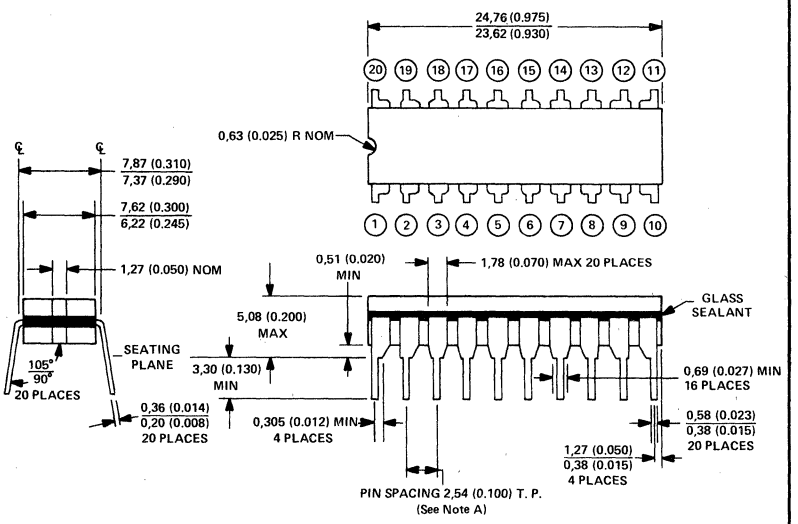


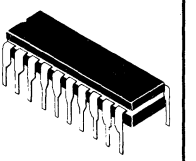
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

J ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

20-PIN J CERAMIC





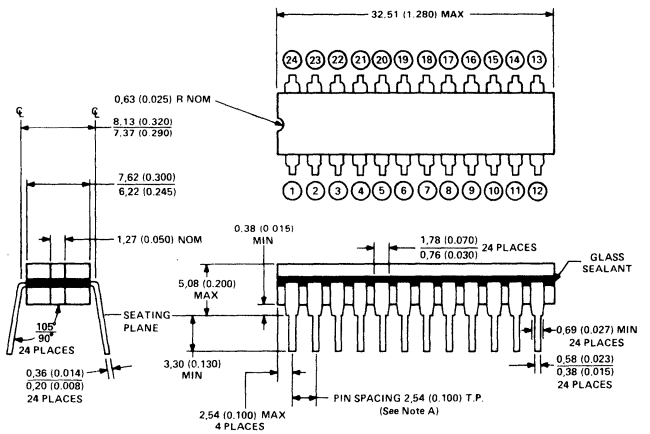
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

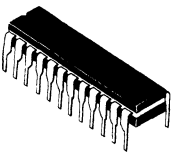
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

JT ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the pins are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-diped'') pins require no additional cleaning or processing when used in soldered assembly.

24-PIN JT CERAMIC





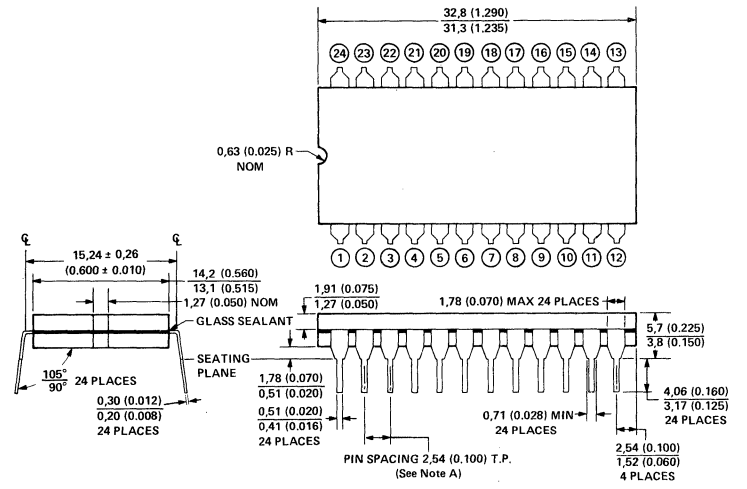
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

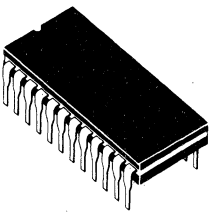
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

J ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the pins are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-diped") pins require no additional cleaning or processing when used in soldered assembly.

24-PIN JW CERAMIC





Falls within JEDEC MO-015AA dimensions

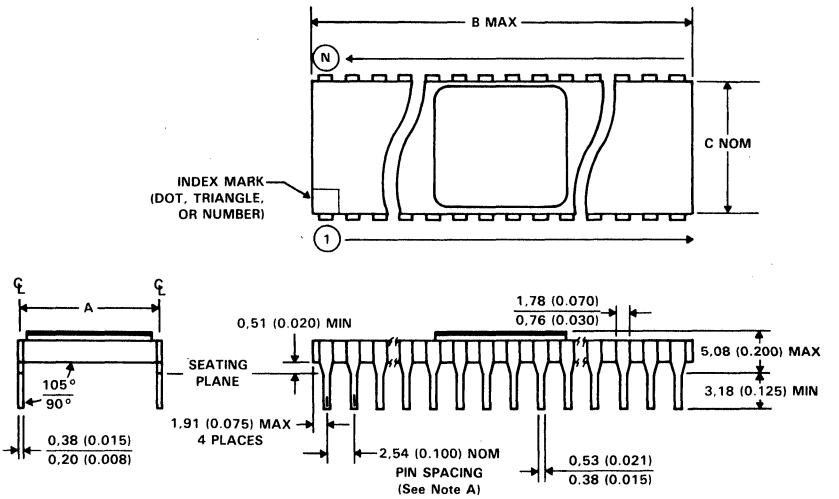
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

JD ceramic side-brade dual-in-line packages

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.

JD CERAMIC–SIDE-BRAZE



DIM \ PINS (N)	16	18	20	22	24
A +0,51 (+0.020) −0,25 (−0.010)	7,62 (0.300)	7,62 (0.300)	7,62 (0.300)	10,16 (0.400)	7,62 (0.300)
B (MAX)	20,57 (0.810)	23,11 (0.910)	25,65 (1.010)	27,94 (1.100)	30,86 (1.215)
C (NOM)	7,37 (0.290)	7,37 (0.290)	7,37 (0.290)	9,91 (0.390)	7,37 (0.290)

DIM \ PINS (N)	24	28	40	48	52	64
A +0,51 (+0.020) −0,25 (−0.010)	15,24 (0,600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	22,86 (0.900)
B (MAX)	31,8 (1.250)	36,8 (1,450)	52,1 (2.050)	62,2 (2.450)	67,3 (2.650)	82,6 (3.250)
C (NOM)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	22,6 (0.890)

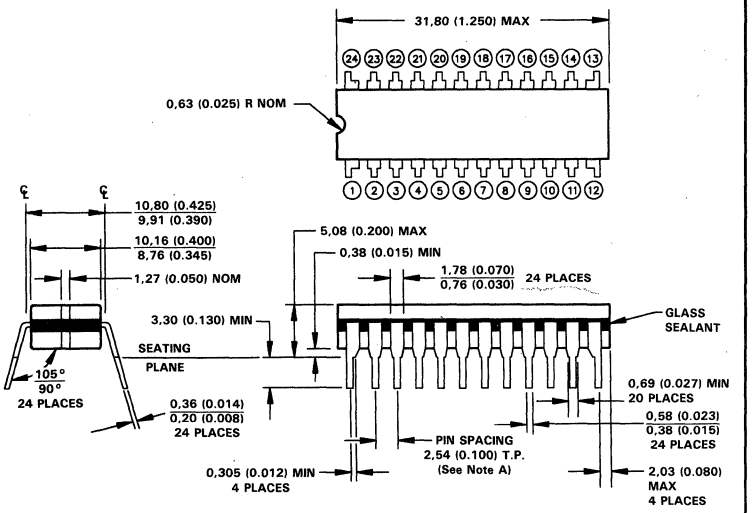
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

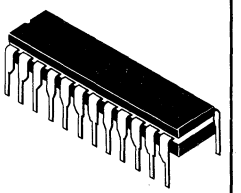
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

JK ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 10,16 (0.400) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

24-PIN JK CERAMIC





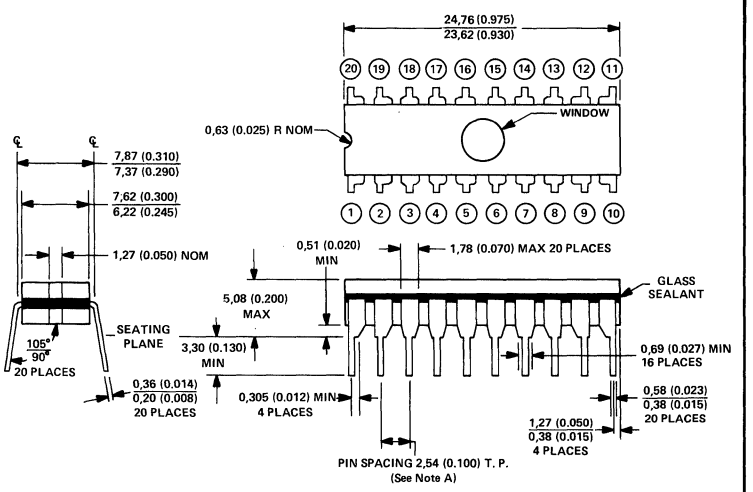
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

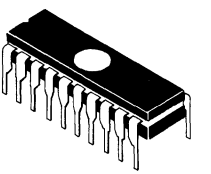
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

JL ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap with a window, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

20-PIN JL CERAMIC





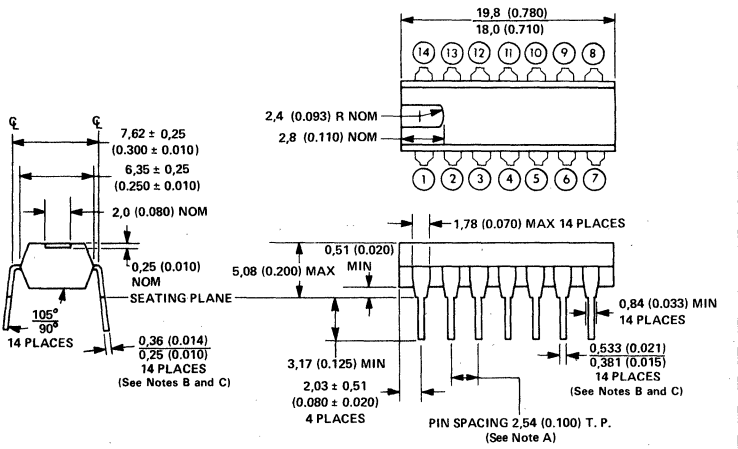
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

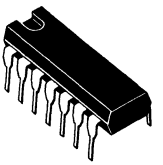
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

N plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

14-PIN N PLASTIC





Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

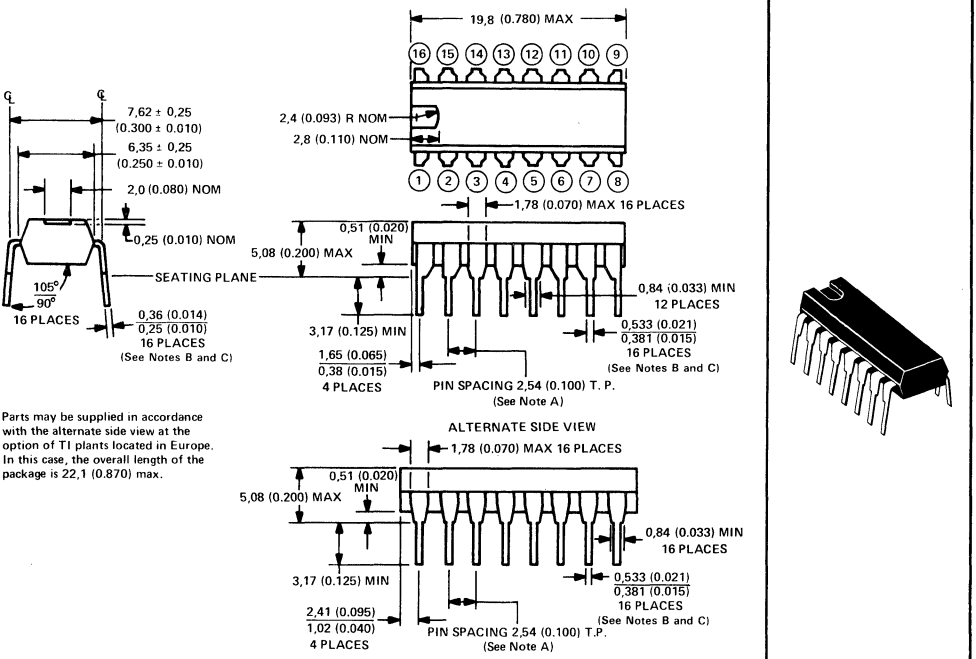
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

16-PIN N PLASTIC



Parts may be supplied in accordance with the alternate side view at the option of TI plants located in Europe. In this case, the overall length of the package is 22,1 (0.870) max.

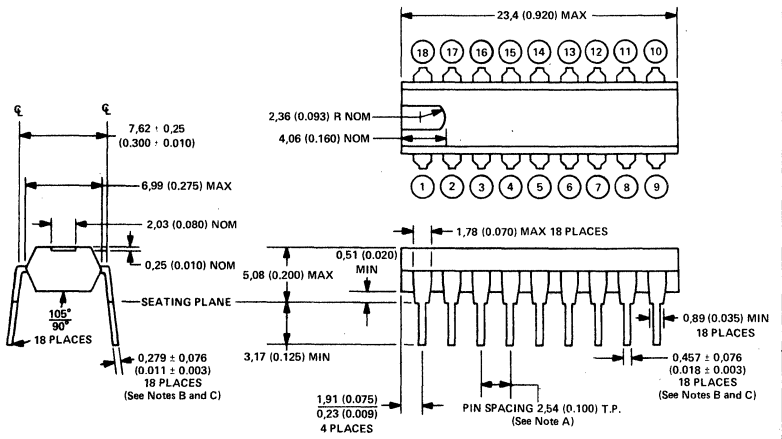
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

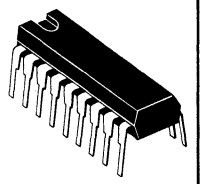
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

18-PIN N PLASTIC





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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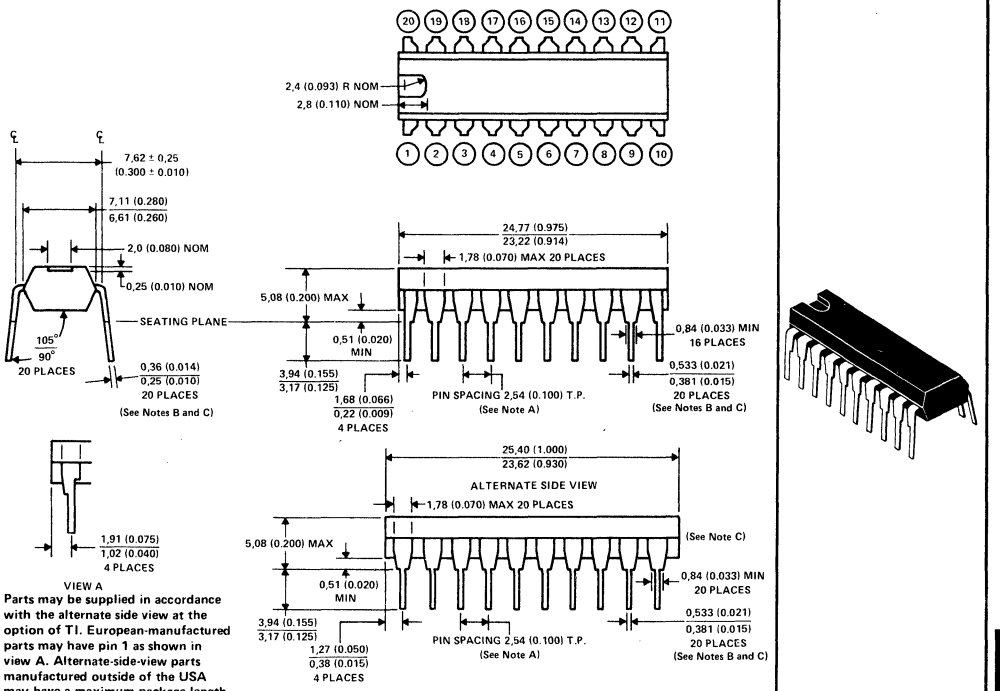
N plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

20-PIN N PLASTIC



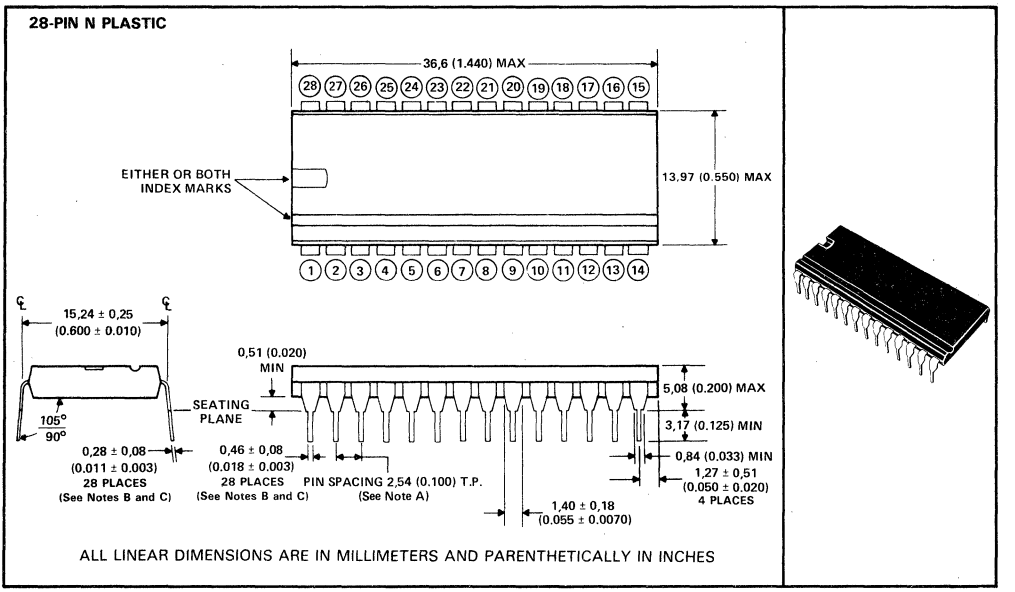
Parts may be supplied in accordance with the alternate side view at the option of TI. European-manufactured parts may have pin 1 as shown in view A. Alternate-side-view parts manufactured outside of the USA may have a maximum package length of 26,7 (1.050).

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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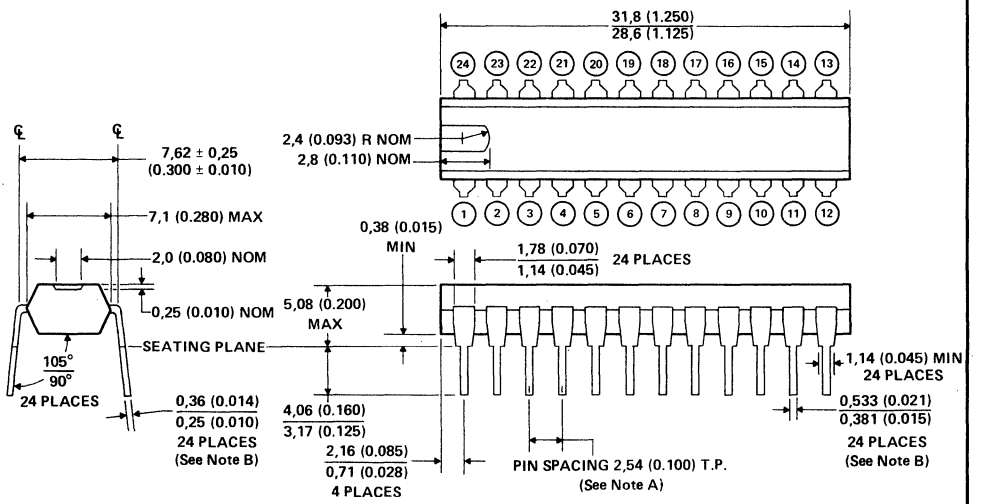
N plastic dual-in-line packages (continued)

24-PIN NT PLASTIC



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

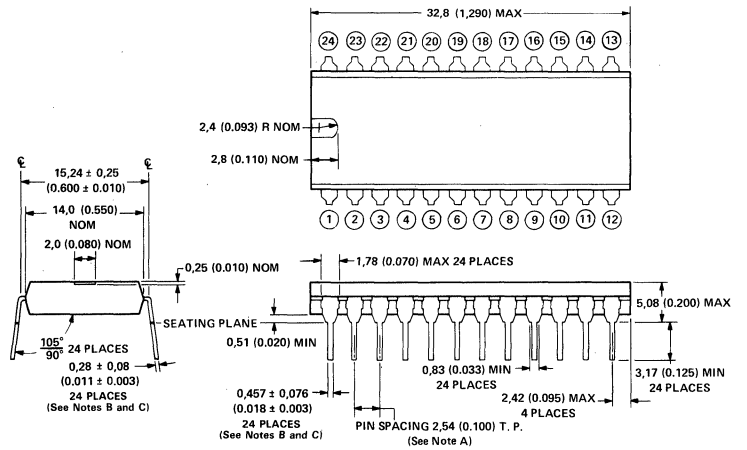
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.

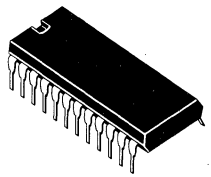
NW plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

24-PIN NW PLASTIC





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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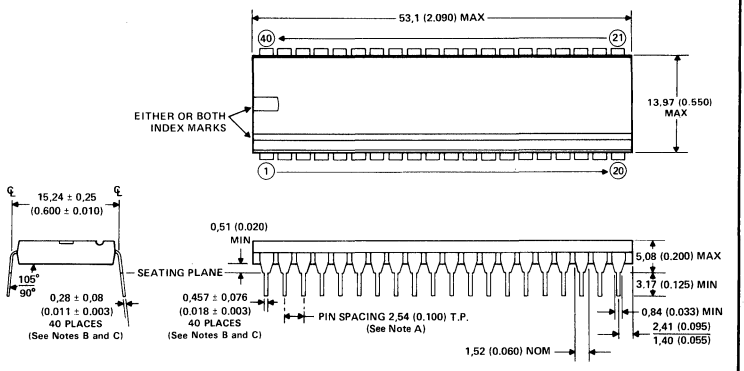
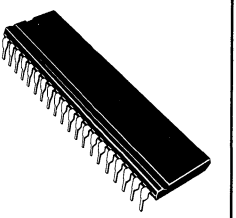
N plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

40-PIN N PLASTIC





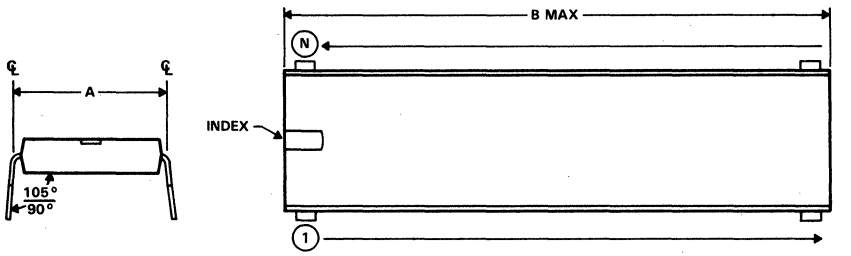
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic dual-in-line package

These dual-in-line packages consist of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

48-PIN, 52-PIN, AND 64-PIN N PLASTIC



PIN SPACING IS 2,54 (0.100) T.P.
(See Note A)

DIM \ PINS (N)	48	52	64
A ± 0,25 (0.010)	15,24 (0.600)	15,24 (0.600)	22,86 (0.900)
B MAX	62,2 (2.45)	67,3 (2.65)	81,3 (3.20)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

TEXAS INSTRUMENTS
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INTRODUCTION

Texas Instruments has developed solutions for today's high density packaging needs. The TI facility at Attleboro, Massachusetts (one of the world's largest suppliers of multimetal systems) provides leading-edge technology which, combined with reliable, high-volume, off-the-shelf interconnection products, allows TI to quickly meet volume commercial applications.

During the last decade, TI has produced one of the largest IC socket families. TI's sockets include every type and size socket in common use today and are available in a wide choice of contact materials and designs.

Our sockets are designed for:

- easy and efficient hand assembly
- compatibility with automatic assembly equipment
- maximum performance and board density

This section provides information on the following types of IC socket products.

PRODUCTION SOCKETS	TYPE
Plastic Leaded Chip Carrier	PLCC
Single-in-Line Packages	SIP
Pin-Grid Arrays	PGA
Dual In-Line	DIP
Dual In-Line 0.070-inch spacing	Shrink Pack
Quad In-Line	QUIP

BURN-IN/TEST SOCKETS	TYPE
Plastic Leaded Chip Carrier	PLCC
Pin Grid Array	PGA
Small Outlilne	J Lead
Dual In-Line	DIP
Dual In-Line 0.070-inch spacing	Shrink Pack
Small Outline	Flat Pack
Quad	Flat Pack

Specially formulated alloys give the TI contact springs:

- Low Contact Resistance
- High Contact Strength (to stand up to repetitive insertions and withdrawals)
- High normal forces assure gas-tight reliability

A full line of reliable, readily available, low-cost interconnection systems means premium performance at an economical price.

Additional information on these and other TI products, including pricing and delivery quotations, may be obtained from your nearest authorized TI Distributor, TI Sales Representative or:

Texas Instruments Incorporated
Connector Systems Department, MS 14-3
Attleboro, Massachusetts 02703
Telephone: (617) 699-5242/5375
TELEX: 92-7708

PERFORMANCE SPECIFICATIONS

Mechanical

Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Vibration: 15 G max
Shock: 100 G max
Insertion force: 0.59 lbs per position typ
Withdrawal force: 0.25 lbs per position typ
Normal force: 200 g min, 450 g typ
Wipe: 0.075 in min
Durability: 5 cycles min
Contact retention: 1.5 lbs min

Electrical

Current carrying capacity: 1 A per contact
Insulation resistance: 5000 MΩ min
Dielectric withstanding voltage: 1000 V ac rms min
Capacitance: 1 pF max

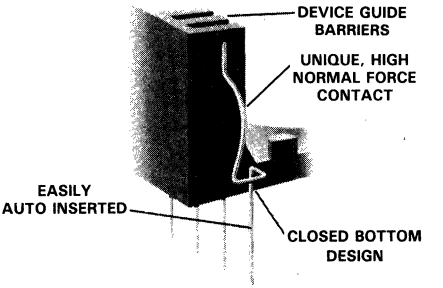
Environmental

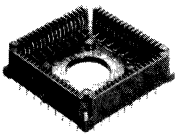
Operating temperature:
Operating: – 40°C to 85°C
Storage: –40°C to 95°C
Temperature cycling with humidity: will conform to final EIA specifications

MATERIALS

Body – Ryton R-4 (40% glass) UL 94 V-0 rating
Contacts – CDA 510 spring temper
Contact finish – 90/10 tin/lead (200 μin –400 μin) over 40 μin copper

Extraction tool available, consult factory
Contact factory for detailed information



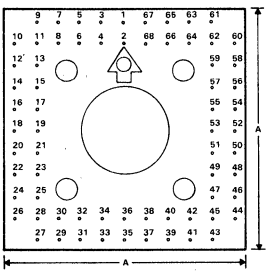


PART NUMBER SYSTEM

CPR PH XXX – X – X – O

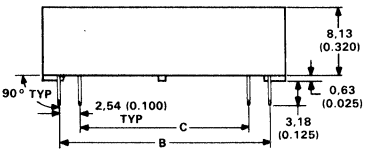
- O: Contact surface 1 – tin/lead plating
- X: Contact spacing 1 - 0.050 in
- XXX: Number of pos (044, 052, 068, 084)
- PH: Plated thru hole, solder tail
- CPR: TI socket Series, Plastic leaded chip carrier

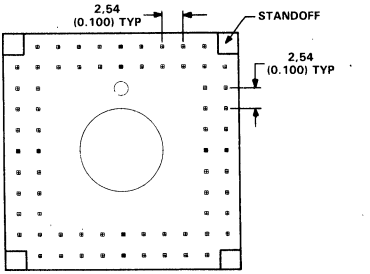
PLASTIC LEADED CHIP CARRIER CPR SERIES



68-Pin shown

NOTE: Socket electrical pin-out pattern represents component side of P.C.B. layout. (TYP. counter clockwise numbering pin-out system.)





Pos	A	B	C
44	21,43 (0.844)	17,78 (0.700)	12,70 (0.500)
52	23,98 (0.944)	20,32 (0.800)	15,24 (0.600)
68	29,06 (1.144)	25,40 (1.000)	20,32 (0.800)
84	34,14 (1.344)	30,48 (1.200)	25,40 (1.000)

Dimensions in parentheses are in inches

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS INSTRUMENTS
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PRODUCT FEATURES

Can be loaded by top actuated insertion or press-in insertion, either manually or automatically
High reliability due to high pressure contact point
Open body and high stand-off design provide high efficiency in heat dissipation
High durability up to 10,000 cycles
Compact design

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads per specific IC device
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Durability: 10,000 cycles 10 mΩ max contact resistance change
Insertion force: Zero g
Withdrawal force: Zero g†

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ per MIL-STD 202, Method 302, Condition B
Dielectric withstanding voltage: 500 V ac rms per MIL-STD 202, Method 301

Environmental

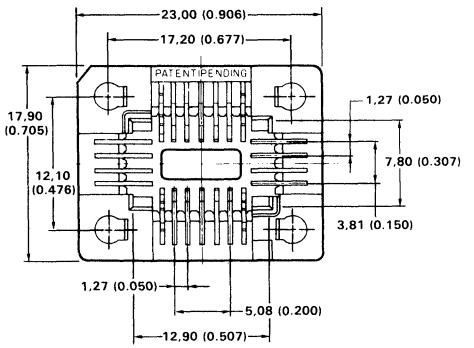
Thermal shock: 100 cycles, −25°C to +150°C
Temperature soak: 150°C for 48 hours
Operating temperature: −40°C to +150°C

MATERIALS

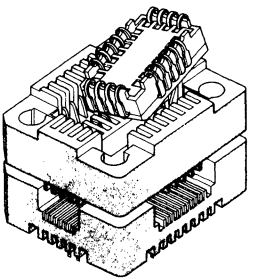
Body — ULTEM glass filled (UL 94 V-0)
Contact — copper alloy
Plating‡ — overall gold plate 4 μin over min 70 μin nickel plating

†After IC is unlocked from the socket
‡For additional plating options contact factory
For complete test report contact the factory

PLCC BURN-IN/TEST SOCKETS CPJ SERIES



Dimensions in parentheses are inches
Contact factory for detailed information

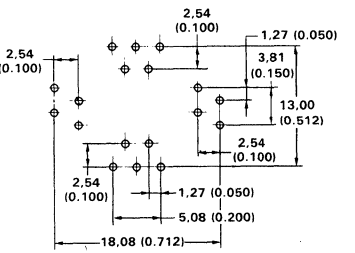


PART NUMBER SYSTEM

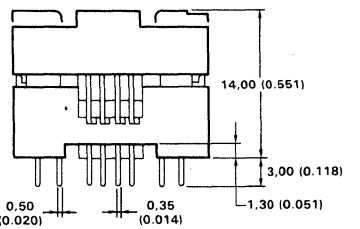
CPJ XX XX X – XXX – B

- CPJ: TI Burn-in PLCC series
- XX: Material — AA = copper alloy
- XX: Contact finish — 33 = overall gold plate
- X: Pitch — A = 0.050
- XXX: Number of contacts
- B

18 PIN FOOTPRINT SHOWN



SIZES: 18 PIN
22 PIN



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PERFORMANCE SPECIFICATIONS†

Mechanical
Vibration: MIL-STD-202
Durability: 30 cycles
Insertion force: Zero g
Withdrawal force: Zero g‡
Contact (normal) force: 200 g min
Contact retention force: 2 lbs per circuit min

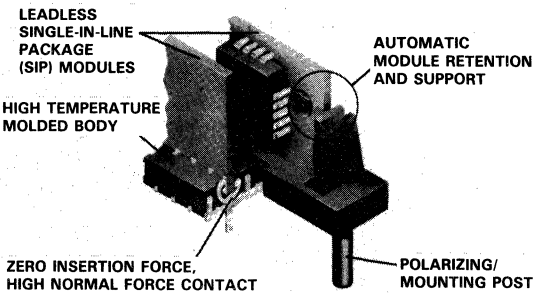
Electrical
Contact rating: 1 A
Contact resistance: 30 mΩ max initial
Insulation resistance: 1000 MΩ at 500 dc
Dielectric strength: 1500 V ac rms
Capacitance: 2 pF max

†Values may vary due to test sequence and SIP module configuration
‡After module is unlocked from the receptacle
For a complete test report, please contact factory

Environmental
(20 mΩ max contact resistance change after all tests)
Operating and storage temperature: −40°C to 100°C
Humidity: MIL-STD 202, Method 106D, 10 days
Temperature soak: 85°C for 160 hours
Thermal Shock: 5 cycles, −40°C to 85°C per MIL-STD 202, Method 107E

MATERIALS
Body — PES polyether sulfone, glass filled, UL 94 V-0
Contact — Beryllium copper C17000; phosphor bronze alloy CA510
Contact finishes — Post plate min 200 μin tin/lead over min 50μin nickel overall
Post plate min 30 μin hard gold over min 75 μin nickel overall

For additional plating options contact the factory.



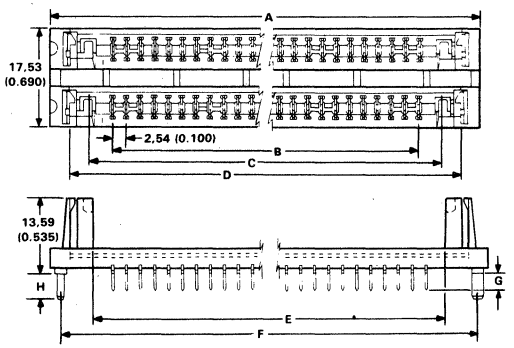
PART NUMBER SYSTEM

TS8X XX XX X −XX − XX

- Variations
  00 — standard product
- Size (number of contacts per row)
- Housing material
  A — PES
- Contact base material/plating
  01—C17000/30 μin gold
  02—CA510/30 μin gold
  03—C17000/200 μin tin/lead
  04—CA510/200 μin tin/lead
- Configuration/row-to-row spacing
  01—single row/N/A
  03—dual row/0.300 in
  04—dual row/0.400 in
  05—dual row/0.500 in
- Series number denotes
  0—0.100 in pitch, vertical mount
  1—0.100 in pitch, low-profile (25°) mount

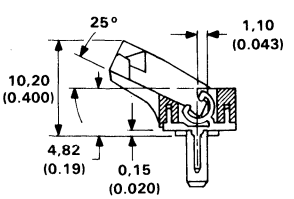
Consult factory for availability of configurations, materials, and sizes.

DUAL ROW VERTICAL



Contact factory for detailed information

SINGLE ROW LOW PROFILE



Ckt. Size	A	B	C	D	E	F	G	H
30	96,52 (3.800)	73,66 (2.900)	82,14 (3.234)	89,28 (3.515)	80,52 (3.170)	92,71 (3.650)	2,79 (0.110)	3,86 (0.152)

Dimensions in parentheses are in inches

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TEXAS INSTRUMENTS
34 Forest Street • Attleboro, Massachusetts 02703

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads 0.015 in to 0.021 in diameter
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Recommended hole grid pattern: 0.100 in ± 0.002 in each direction
Vibration: 15 G, 10-2000 Hz per MIL-STD 1344A, Method 2005.1 Test Condition III
Shock: 100 G, sawtooth waveform, 2 shocks each direction per MIL-STD 202, Method 213, Test Condition I
Durability: 5 cycles, 10 mΩ max contact resistance change per MIL-STD 1344, Method 2016
Insertion force: 3.6 oz (102 g) per pin typ using 0.018 in diameter test pin
Withdrawal force: 0.5 oz (14 g) per pin min using 0.018 in diameter test pin

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ at 500 V dc per MIL-STD 1344, Method 3003.1
Dielectric withstanding voltage: 1000 V ac rms per MIL-STD 1344, Method 3001.1
Capacitance: 1 pF max per MIL-STD 202, Method 305

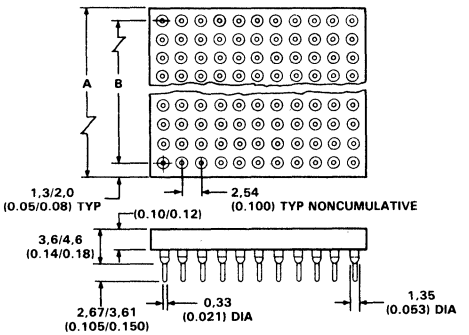
Environmental

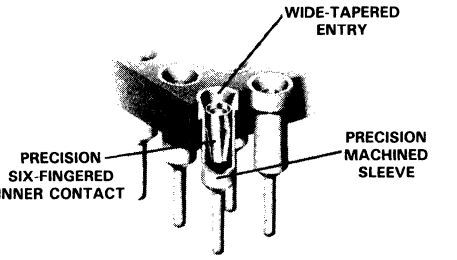
Operating temperature: −65°C to 125°C, gold; −40°C to 100°C, tin/lead
Corrosive atmosphere: 10 mΩ max contact resistance change when exposed to 22% ammonium sulfide for 4 hours
Gas tight: 10 mΩ max contact resistance change when exposed to nitric acid vapor for 1 hour
Temperature soak: 10 mΩ max contact resistance change when exposed to 105°C temperature for 48 hours

MATERIALS

Body — PBT polyester UL 94 V-0
On request, G10/FR4 or Mylar film
Outer sleeve — Machined Brass (QQ-B-626)
Inner contact — Beryllium copper (QQ-C-530) heat treated
Plating: (specified by part number)

PIN GRID ARRAY





Inner contact — 30 μin gold over 50 μin nickel or 100 μin tin/lead over 50 μin nickel
Outer sleeve — 10 μin gold over 50 μin nickel or 50 μin tin/lead over 50 μin nickel

PART NUMBER SYSTEM

C X G XX − XXX X X − X X

Pin Length

WIRE WRAP	SOLDER TAIL
3-0.510 long	9-0.105/0.150

Plating

P/N	Sleeve	Clip
0	Gold	Gold
5	Tin	Gold

Body Style and Orientation
Contact Loading Pattern
Number of Pins 024 to 324
Pin Grid Array
Overall Grid Size 5×5=05 to 18×18=18
BODY MATERIAL
G — Glass Filled Epoxy
P — PBT Polyester
TI Socket

Insulator Size	A ±0.010	B ±0.005†
9×9	(0.950) 24,13	(0.800) 20,32
10×10	(1.050) 26,67	(0.900) 22,86
11×11	(1.150) 29,21	(1.000) 25,40
12×12	(1.250) 31,75	(1.100) 27,94
13×13	(1.350) 34,29	(1.200) 30,48
14×14	(1.450) 36,83	(1.300) 33,02
15×15	(1.550) 39,37	(1.400) 35,56
16×16	(1.650) 41,91	(1.500) 38,10
17×17	(1.750) 44,45	(1.600) 40,64
18×18	(1.850) 46,99	(1.700) 43,18

†Noncumulative
Dimensions in parentheses are inches
Consult factory for detailed information

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PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads per specific IC device
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Durability: 10,000 cycles, 20 mΩ max contact resistance change
Insertion force: 1.3 oz per position max
Withdrawal force: 8.8 grams per position min

Electrical

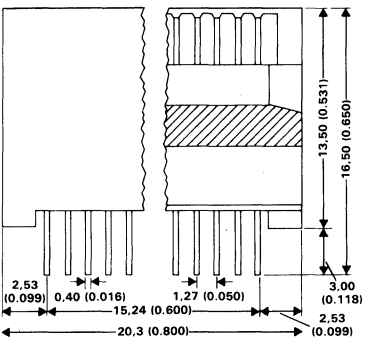
Contact rating: 1.0 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ per MIL-STD 202, Method 302, Condition B
Dielectric withstanding voltage: 700 V ac rms per MIL-STD 202, Method 301

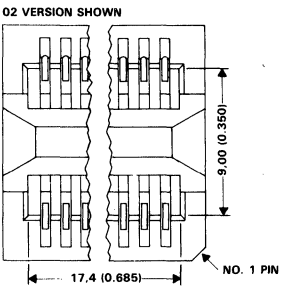
Environmental

Thermal shock: 100 cycles, −25°C to +180°C, 1 hour
Temperature soak: 180°C for 1000 hours, 80 mΩ max change
Operating temperature: −65°C to +180°C

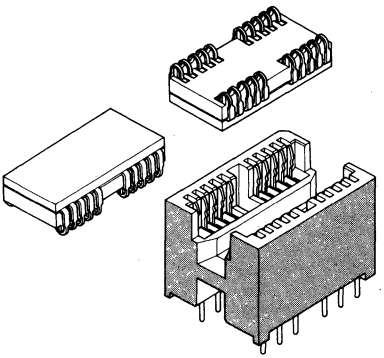
MATERIALS

Body — PES glass filled UL 94 V-0
Contact — copper alloy
Plating — overall gold plate min 4 μin over min 70 μin nickel plating





Dimensions in parentheses are inches
Contact factory for detailed information



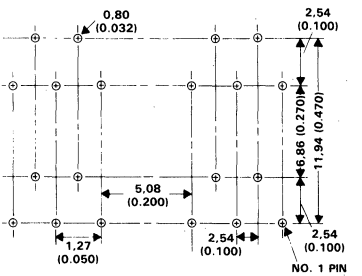
PART NUMBER SYSTEM

CSJT XXX – XX – XX X

- CSJT: TI SOJ series
- XXX: Number of Contacts
- XX (Contact Finish):
  - 37 = Overall gold plate 4 μin
  - 38 = Overall gold plate 30 μin
  - 57 = Selective gold plate 4 μin
  - 58 = Selective gold plate 30 μin
- XX (Body Variation):
  - 02 = Standard 1 forward/backward insertion
  - 03 = Special/orientation pin
  - 04 = Special/high standoff
  - 05 = Special/24-pin
  - 06 = Standard 2 forward insertion, BECU
- X (Body Material):
  - Blank = G.F. PES
  - A = PPS R4-03
  - B = G.F. PEI

SIZES: 20 pin
26 pin

20-PIN (02 VERSION) FOOTPRINT SHOWN



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TEXAS INSTRUMENTS
34 Forest Street • Attleboro, Massachusetts 02703

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads 0.011 ± 0.003 in by 0.018 ± 0.003
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Recommended hole grid pattern: 0.100 in ± 0.003 in each direction
Vibration: 15 G, 10-2000 Hz per MIL-STD 1344A, Method 2005.1 Test Condition III.
Shock: 100 G, sawtooth waveform, 2 shocks each direction per MIL-STD 202, Method 213, Test Condition I
Durability: 5 cycles, 10 mΩ max contact resistance change per MIL-STD 1344, Method 2016
Insertion force (C7X and C86): 16 oz (454 g) per pin max
Withdrawal force: (40 g) per pin min

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ at 500 V dc per MIL-STD 1344, Method 3003
Dielectric withstanding voltage: 1000 V ac rms per MIL-STD 1344, Method 3001.1
Capacitance: 1 pF max per MIL-STD 202, Method 305

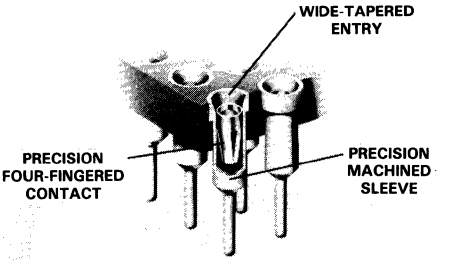
Environmental

Operating temperature: −55°C to 125°C, gold; −40°C to 100°C, tin
Corrosive atmosphere: 10 mΩ max contact resistance change when exposed to 22% ammonium sulfide for 4 hours
Gas tight: 10 mΩ max contact resistance change when exposed to nitric acid vapor for 1 hour
Temperature soak: 10 mΩ max contact resistance change when exposed to 105°C temperature for 48 hours

Materials (C7X and C86)

Body — PBT polyester UL 94 V-0
C7X Contacts — Outer sleeve: brass
Clip: BECU
Contact finish — clip 30 μin gold over 50 μin nickel or 50 μin tin/lead over 50 μin nickel
Specified by Part Number — sleeve 10 μin gold over 50 μin nickel or 50 μin tin/lead over 50 μin nickel
C86 Contacts — Phosphor bronze base metal
C86 Contact-finish — Tin plate 200 μin over copper flash

C7X SERIES — SCREW MACHINE

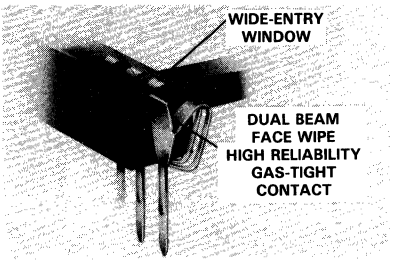


C7X SERIES — SCREW MACHINE PART NUMBER SYSTEM

C7X (X) XX − X X

- C7X: Screw Machine Socket
  - 1 — wire wrap
  - 2 — solder tail
- (X): S — Single-in-line package (where applicable)
- XX: Number of Positions
- X: Plating (Sleeve/Clip)
  - 0 — Gold/Gold
  - 5 — Tin/Gold
- X: Variations
  - Solder Tail : 9 Pin length 0.125 Typ
  - Wire Wrap : 3 Pin length 0.510

C86 SERIES — STAMPED AND FORMED



C86 SERIES PART NUMBER SYSTEM

C 86 XX − 01

- C: TI Socket Series
- 86: Tin Dual Beam Face Wipe
- XX: Number of positions
- 01: Variation
  - 01 — Standard product

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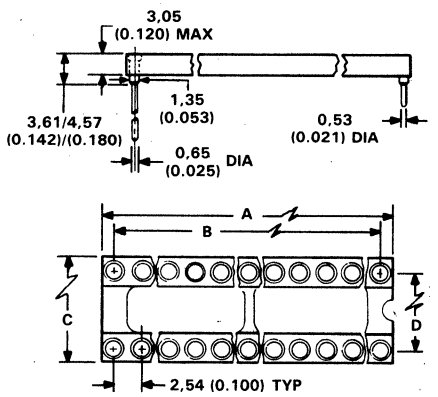
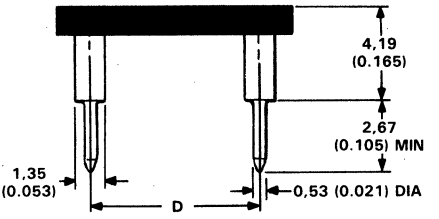
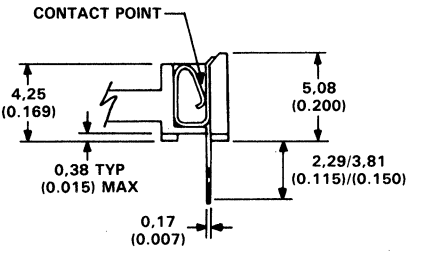
DUAL-IN-LINE
C7X AND C86 SERIES



C7X SERIES



C86 SERIES



DIPS

Positions	Dim A Max	Dim B ±0.005	Dim C Max	Dim D ±0.005	Positions	Dim A Max	Dim B ±0.005	Dim C Max	Dim D ±0.005
6	7,62 (0.300)	5,08 (0.200)	10,16 (0.400)	7,62 (0.300)	†24	30,48 (1.200)	27,94 (1.100)	12,76 (0.500)	10,16 (0.400)
8	10,16 (0.400)	7,62 (0.300)	10,16 (0.400)	7,62 (0.300)	28	35,56 (1.400)	33,02 (1.300)	17,78 (0.700)	15,24 (0.600)
14	17,78 (0.700)	15,24 (0.600)	10,16 (0.400)	7,62 (0.300)	32	40,64 (1.600)	38,10 (1.500)	17,78 (0.700)	15,24 (0.600)
16	20,32 (0.800)	17,78 (0.700)	10,16 (0.400)	7,62 (0.300)	34	45,72 (1.800)	43,18 (1.700)	17,78 (0.700)	15,24 (0.600)
18	22,86 (0.900)	20,32 (0.800)	10,16 (0.400)	7,62 (0.300)	40	50,80 (2.000)	48,26 (1.900)	17,78 (0.700)	15,24 (0.600)
20	25,40 (1.000)	22,86 (0.900)	10,16 (0.400)	7,62 (0.300)	48	60,96 (2.400)	58,42 (2.300)	17,78 (0.700)	15,24 (0.600)
22	27,94 (1.100)	25,40 (1.000)	12,76 (0.500)	10,16 (0.400)	50	63,50 (2.500)	60,96 (2.400)	25,40 (1.000)	7,62 (0.900)
24	30,48 (1.200)	27,94 (1.100)	17,78 (0.700)	15,24 (0.600)	64	81,28 (3.200)	78,74 (3.100)	25,40 (1.000)	22,86 (0.900)
†24	30,48 (1.200)	27,94 (1.100)	10,16 (0.400)	7,62 (0.300)					

†Nonstandard sizes
Not all sizes available in each series
Dimensions apply to all series

Dimensions in parentheses are inches
Contact factory for detailed information

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TEXAS INSTRUMENTS
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PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads 0.011 in by 0.018 in
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hold size range: 0.032 in to 0.042 in
Durability: 10K cycles – CM Series, 5K cycles – CP/CQ

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ at 500 V dc
Dielectric withstanding voltage: 1000 V ac rms
Capacitance: 1 pF max per MIL-STD 202, Method 305

Environmental

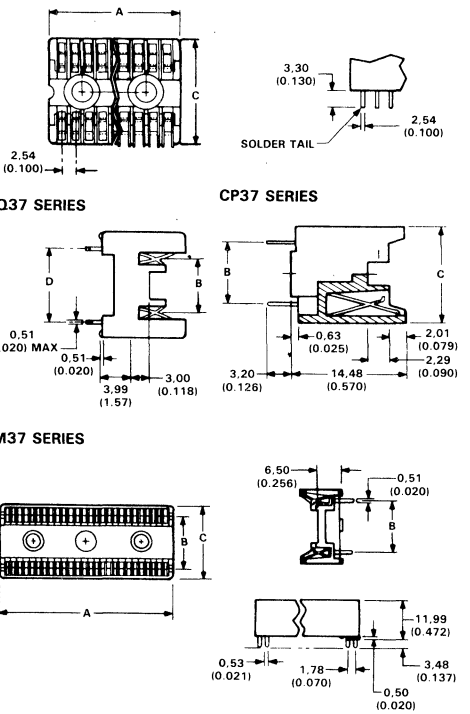
Operating temperature: –65°C to 170°C – CP/CM Series,
–65°C to 150°C – CQ Series
Humidity: 10 mΩ max contact resistance
Temperature Soak: 10 mΩ max contact resistance change

MATERIALS

Body – PPS (polyphenylen sulfide) UL 94 V-0
Contacts – Higher performance copper nickel alloy
Plating:† 4 μin of gold min over 100 μin of nickel min

†For additional plating options consult the factory

BURN-IN/TEST DIP SOCKETS



PART NUMBER SYSTEM

C X 37 XX – 22 S X

- X: Pin to pin — A=0.100 centers, B=0.070 centers
- S: PPS high temperature body material
- 22: Copper nickel alloy Soldertail
- XX: Number of positions
- 37: Overall gold plate
- X: Series Features — Q=Auto unloadable, P=High density mounting, M=Shrink 0.070 centers
- C: TI Socket Series

CQ37 SERIES

Number of Positions	A ±0.01 Length	D ±0.02	C ±0.01 Width	B ±0.01 Contact
14	20,32 (0.800)			
16	22,35 (0.880)	12,70	15,24	7,62
18	24,89 (0.980)	(0.500)	(0.600)	(0.300)
20	27,43 (1.080)			
24	32,51 (1,280)			
28	37,59 (1.480)	19,05	22,86	15,24
40	52,83 (2.080)	(0.750)	(0.900)	(0.600)
42	55,37 (2.180)			

CP37 SERIES

Number of Positions	A max Length	B ±0.02	C max Width
8	11,68 (0.460)		
14	17,78 (0.700)		
16	20,32 (0.800)	7,62	12,70
18	22,86 (0.900)	(0.300)	(0.500)
20	25,40 (1.000)		
24	30,48 (1.200)		
28	35,56 (1.400)	15,24	20,32
40	50,80 (2.000)	(0.600)	(0.800)

CM37 SERIES

Number of Positions	A ±0.016 Length	B ±0.02	C ±0.016 Width
28	27,18 (1.070)	10,67 (0.420)	17,20 (0.677)
40	37,85 (1.490)		
42	39,62 (1.560)	16,51 (0.650)	23,11 (0.910)
54	50,29 (1.980)		
64	59,18 (2.330)	20,32 (0.800)	26,92 (1.060)

Dimensions in parentheses are inches
Contact factory for detailed information

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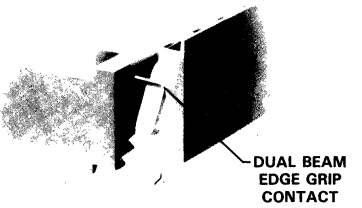
PERFORMANCE SPECIFICATIONS

Insertion force: 16 oz (454 g) per pin max
Withdrawal force: 1.5 oz (42 g) per pin min
Operating temperature: −40°C to 100°C, tin/lead
Accommodates IC leads 0.011 ± 0.0003 in by 0.018 ± 0.003 in
Contact rating: 1 A per contact

MATERIALS

Body — PBT polyester UL 94 V-0
C4S & CxW Contacts — Copper alloy
Contact finish — Reflow tin plating, 40 µin min



PART NUMBER SYSTEM FOR CxW SERIES

C X W XX − 11

- XX: Number of contacts (42, 52, 64)
- W: Staggered leads
- X: 5 — 64 contacts; 6 — 42, 52 contacts
- C: TI Socket Series

QUAD-IN-LINE (CxW SERIES)

Product Number	A Max Length	B Row to Row	C Max Row to Row
C5W64-11	41,90 (1.65)	22,90 (0.950)	19,05 (0.750)
C6W42-11	27,90 (1.10)	22,90 (0.900)	17,80 (0.700)
C6W52-11	34,30 (1.35)	22,90 (0.900)	17,80 (0.700)

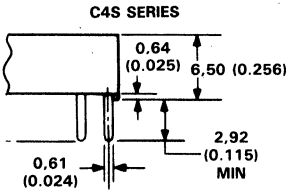
Dimensions in parentheses are inches
Contact factory for detailed information

PART NUMBER SYSTEM† FOR C4S SERIES

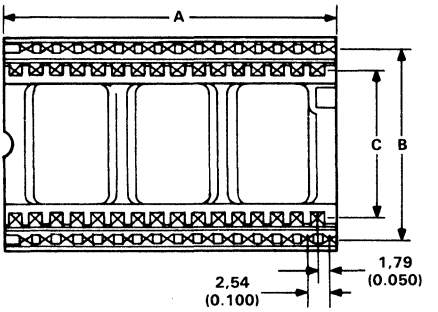
C 4 S XX − 02

- XX: Number of contacts 28, 40, 42, 52, 54, 64
- S: Shrink Pack (0.070 in pin-to-pin contact spacing)
- 4: Reflow tin plating
- C: TI Socket Series

†Also available in screw machine contacts



QUAD-IN-LINE (CxW SERIES)

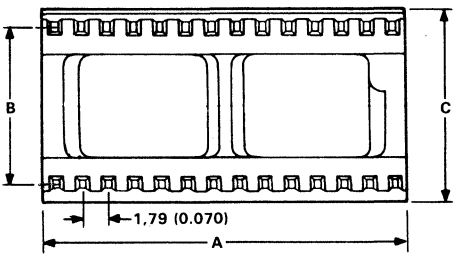


C4S SERIES

Positions	A Max Length	B Row to Row	C Max Width
28	25,02 (0.985)	10,16 (0.400)	13,00 (0.512)
40	35,69 (1.405)	15,24 (0.600)	17,98 (0.708)
64	57,07 (2.247)	19,05 (0.750)	21,62 (0.851)

Dimensions in parentheses are inches

SHRINK PACK DIP (C4S SERIES)



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TEXAS INSTRUMENTS
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PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads per specific IC device
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Durability: 5000 cycles, 10 mΩ max contact resistance change per MIL-STD 1344, Method 2016

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1 MΩ at 500 V dc per MIL-STD 1344, Method 3003.1
Dielectric withstanding voltage: 700 V ac rms per MIL-STD 1344, Method 3001.1
Capacitance: 1 pF max per MIL-STD 202, Method 305

Environmental

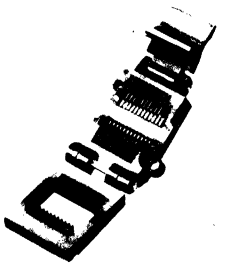
Operating temperature: −65°C to 170°C
Humidity: 10 mΩ max contact resistance change when tested per MIL-STD 202, Method 103B
Temperature soak: 10 mΩ max contact resistance change when exposed to 105°C temperature for 48 hours

MATERIALS

Body — CFP Series — PES (polyether sulfone) glass filled UL 94 V-0
Temperature: −65°C to 170°C
Contact — Beryllium copper
Plating:† Overall gold plate min 4 μin over min 70 μin nickel plating

†For additional plating option consult the factory.
Dimensional drawings available from factory.

SMALL OUTLINE FLAT PACK (CFPH/K SERIES)

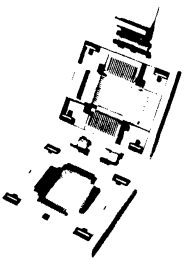


PART NUMBER SYSTEM

C XX X – XXX – XX – 01

- C: TI Series socket
- XX: Style FP — Flat pack
- X: Configuration
  - H — 14, 16, 18, 20 Positions
  - K — 24, 28 Positions
- XXX: Number of positions
- XX: Plating
  - 37 — overall gold plate
- 01: Variations

QUAD FLAT PACK (CFPM SERIES)

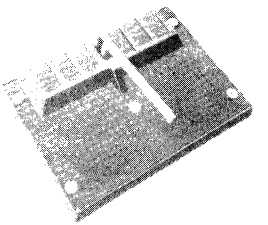


PART NUMBER SYSTEM

CXX X – XXX – XX – 01X

- CXX: TI socket
  - Style PF — Flat pack
- X: Configuration
  - M — Quad pack
- XXX: Number of positions
- XX: Plating
  - 37 — overall gold plate
- 01X: Variations
  - A — 1.0 mm ℄ contact spacing
  - B — 0.8 mm ℄ contact spacing

PIN GRID ARRAY (CZFW SERIES)



PART NUMBER SYSTEM

C XX X – XXX – XX – 01

- C: TI Series socket
- XX: Style ZF — Zero force
- X: Configuration
  - W — 11 × 11 × 2
- XXX: Number of positions
- XX: Plating
  - 37 — overall gold plate
- 01: Variations

AVAILABLE SIZES

CFPH Series 14, 16, 18, 20 CFPK Series 24, 28	Small Outline Flat Pack
CFPM Series 64, 80	Quad Flat Pack
CZFW Series 11 × 11 × 2	Pin Grid Array

Contact factory for detailed information

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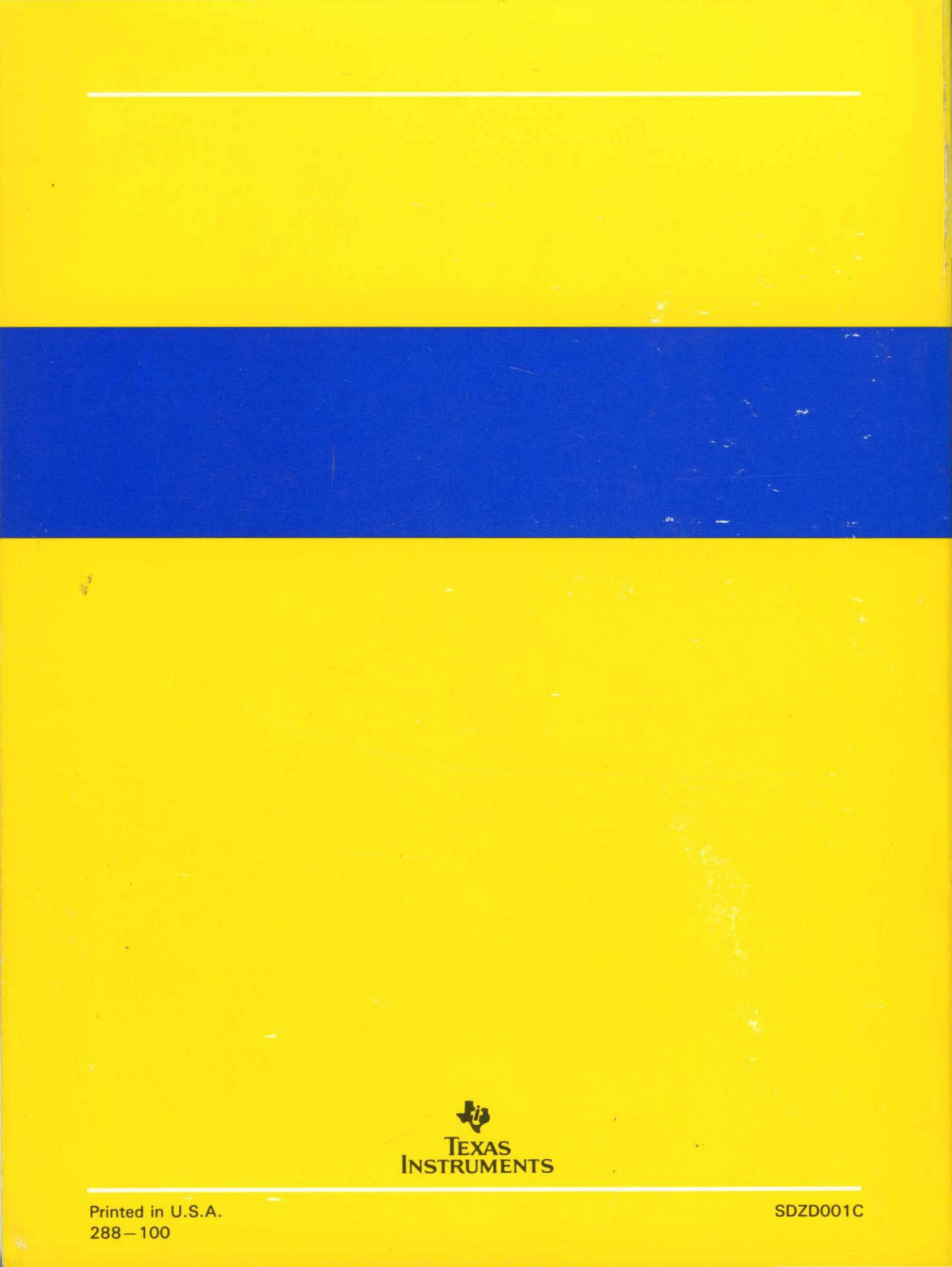

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