

TVP4020 PERMEDIA® 2 Architecture Overview

User's Guide

SLAU010
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Preface

Read This First

About This Manual

This manual provides an architectural overview of the TVP4020, a high-performance PERMEDIA 2 graphics processor. It is written for design engineers and project managers. Hardware and software engineers can also use this manual as an introduction to TVP4020 architecture before proceeding to more detailed information in other TVP4020 documents.

You should be familiar with basic graphics and video processing theory and general graphics and video applications.

How to Use This Manual

This document contains the following chapters:

Chapter 1

gives an overview of the TVP4020 graphics processor features and benefits.

Chapter 2

describes the key TVP4020 hardware capabilities that provide 3-D, 2-D, and video graphics benefits.

Chapter 3

discusses the TVP4020 architecture consisting of the setup processor and the main graphics processor, augmented by external interfaces.

Chapter 4

describes the 3DLabs™ software drivers incorporated by the TVP4020.

Chapter 5

defines the range of TVP4020-based add-in boards and motherboards that can be designed to meet the requirements of particular markets and their price/performance criteria.

Related Documentation From Texas Instruments

The following books describe the TVP4020 and related support tools. To obtain a copy of any of these TI documents, call the Texas Instruments Literature Response Center at (800) 477–8924. When ordering, please identify the book by its title and literature number.

TVP4020 Programmer Reference User's Guide, Literature No. SLAU011

Other Documentation

This manual references the following specifications:

Video Module Interface (VMI) Specification, Video Electronics Standard Association (VESA)

Peripheral Component Interconnect (PCI) Specification, Video Electronics Standards Association (VESA)

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Introduction

This chapter gives an overview of the TVP4020 graphics processor, and highlights its features and benefits.

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1.1 TVP4020 Feature Highlights

The TVP4020 is a high-performance peripheral-component interconnect/accelerated graphics port (PCI/AGP) graphics processor. It balances high quality, three-dimensional (3-D) polygon and textured graphics acceleration; windows acceleration; and state-of-the-art MPEG1/MPEG2 playback, with a fast integrated super-video graphic array (SVGA) core, integrated random-access memory digital-to-analog converter (RAMDAC), and video ports.

The TVP4020 features a full line of advanced graphics processing functions that include:

- Enhanced 3-D graphics features and performance at 83 MHz
 - 83M perspective-correct, bilinear filtered, texture mapped pixels/s
 - 42M perspective-correct, bilinear filtered, texture mapped, depth buffered pixels/s
 - 800K texture mapped polygons/s
 - True-color 3-D graphics
 - Polygon based with Z buffer
 - Texture decompression
 - Full scene antialiasing
 - Integrated geometry pipeline setup processor
 - 100 MFLOPS
 - Slope and setup information calculation
 - Floating- to fixed-point conversion
- Full support for the Intel™ AGP and PCI
 - 66-MHz operation
 - Direct memory access (DMA) and execute mode support
 - Sideband addressing
 - Enhanced graphical user interface (GUI) acceleration
 - Ultra-fast block transfer (BLT) engine and two-dimensional (2-D) rasterizer
 - Stretch BLTs, monochrome/color expansion, and logic operations
- Fast SVGA with 8, 16, 24, and 32-bit packed framebuffer storage

- MPEG2 compatible video playback acceleration
 - YUV 4:4:4, YUV 4:2:2, and YUV 4:2:0 (native MPEG2 format)
 - Unlimited multiple playback windows (occluded)
 - Independent x- and y-scaling and mirroring
- Integrated true-color 230-MHz RAMDAC
 - DPMS, DDC1, and DDC2AB+
 - Clock synthesizer and hardware cursor
 - 320×200 to 1600×1200 screen resolutions
- Multimode video streams
 - Simultaneous input and output video
 - Optional scaling and filtering
 - Optional color space conversion and gamma correction
- Flexible multifunction synchronous dynamic random-access memory (SDRAM) or synchronous graphic random-access memory (SGRAM)
- Comprehensive suite of optimized software drivers
- Reference board designs and manufacturing kits

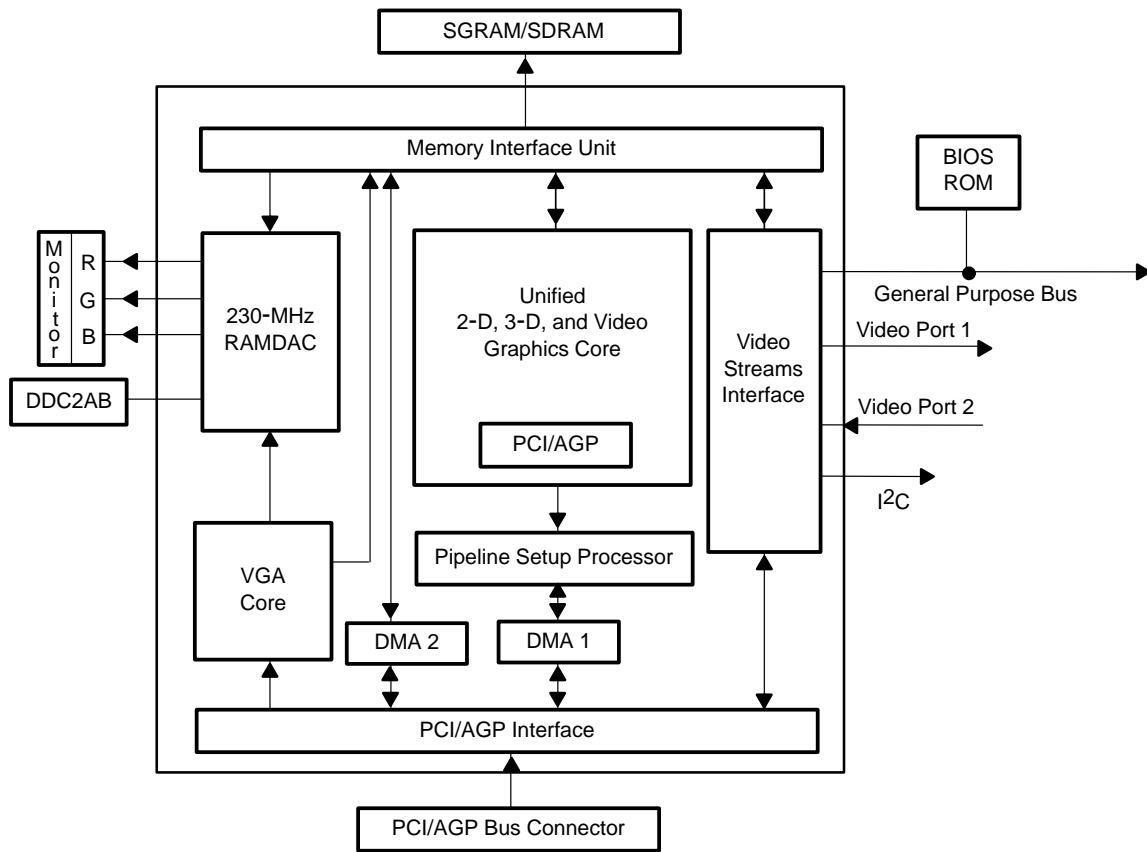
1.2 Setting New Standards

The TVP4020 sets a new standard for 3-D graphics and represents a fully integrated solution to meet the increasing requirement for low-cost 3-D, 2-D, and multimedia acceleration. Based on a proven low-cost and scalable architecture, the TVP4020 accelerates a broad range of applications, including: games, multimedia, animations, presentations, authoring tools, 3-D Internet browsers, personal computer-aided design/computer-aided manufacturing, and visualization.

1.3 Block Diagram

The TVP4020 is a single low-cost package that combines maximum levels of integration with the demand for flexible multimedia input/output (I/O) requirements. Figure 1-1 shows the TVP4020 configuration.

Figure 1-1. TVP4020 Block Diagram



TVP4020 Features

This chapter describes the key TVP4020 hardware capabilities that provide superior 3-D, 2-D, and video graphics benefits.

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2.1 3-D Graphics

The TVP4020 architecture provides a full array of 3-D graphics features.

- Full primitive support
- Efficient processing of small primitives
- High fill rate
- Fast buffer clearing
- Efficient texture storage
- High quality rendering
- High quality textures
- High quality lighting
- Extremely realistic special effects
- Translucent objects and sprites
- High-quality texture cutouts
- Antialiased sprites
- Fast hidden surface elimination
- Fast shadow and transparency effects
- Arbitrary cutout and multipass rendering
- High quality output at any color depth
- Fast sprite handling
- Seamless integration of video and 3-D
- Minimize update area, target selection
- Improved image quality at lower resolutions
- Use of rendered images as textures
- Full range of double-buffer techniques
- Overlays
- Texture cache support
- Points, lines, triangles, rectangles
- Integrated setup calculation, low latency
- Wide data paths, high performance memory
- SGRAM block filling for any buffer type
- Fully flexible formats, internal 256-entry look-up table (LUT)
- Subpixel and subtixel accuracy
- Accurate perspective correction and bilinear filtering
- Interpolated diffuse and specular components
- Interpolated fog and depth-cueing
- Blending/transparency on any primitive
- Color key with bilinear filter does not leave edge effects
- Edge antialiasing for zoomed sprites
- Depth (Z) buffering
- Area stippling with no performance cost
- Stencil buffer

- Dithering with no performance cost
- Color key, scale, stretch, rotate, mirror
- Color key with depth test and perspective correction
- Hardware extent-checking and picking
- Full screen antialiasing
- Multifunction memory
- Full screen flip, per window buffer selection, fast BLT
- Per-pixel main image/overlay selection
- Page tables for map indirection, AGP, DMA

2.2 2-D Graphics

The TVP4020 architecture also supports 2-D graphics functions.

- Full primitive support
- Efficient processing of small primitives
- Window clipping
- Ultra-fast solid filling
- Ultra-fast monochrome expansion
- High-speed color brushes
- High-speed monochrome brushes
- Raster operations
- Fast BLTs
- Fast uploading and downloading
- High-speed monochrome downloading
- Flexible font caching support
- Color translation
- High-speed stretch BLT
- Points, lines, spans, rectangles, polygons
- Integrated setup calculation, low latency
- Hardware rectangle clipping
- SGRAM block filling
- SGRAM block filling with pixel mask
- Internal pattern RAM
- Internal stipple table
- Logic operations unit
- Wide data path
- Packed into 32-bit words
- Bitmask test with SGRAM block filling
- Byte-aligned monochrome bitmaps in local memory
- Through internal LUT
- Texture operations

2.3 MPEG2 and Video

The TVP4020 additionally supports MPEG2 and video graphics functions.

- Support for software decoders
- Support for hardware decoders
- High-speed-color space conversion
- Flexible YUV data formats
- Fast arbitrary stretch with filter
- Fully featured video effects
- Direct memory access from system, or writes directly to local memory
- Input data through video port
- YUV to RGB with no performance cost
- 4:4:4, 4:2:2, 4:2:0
- Bilinear filter
- Scale, stretch, rotate, mirror

TVP4020 Architecture

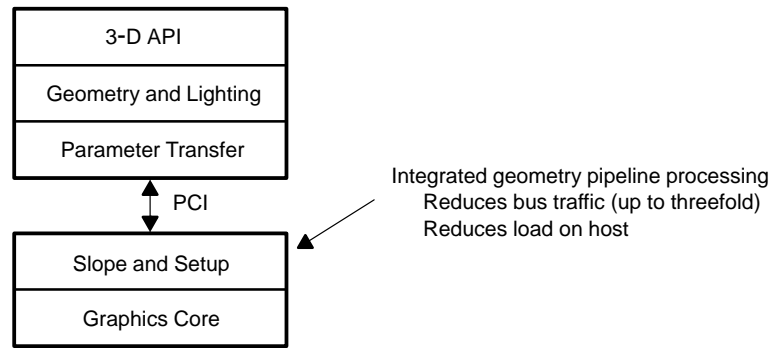
This chapter discusses the TVP4020 architecture consisting of the setup processor and the main graphics processor, augmented by external interfaces.

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3.1 Geometry Setup Processing

The geometry setup unit (see Figure 3–1) is a 100-MFLOPS OpenGL™- and Direct3D™-compliant setup processor, designed to break the 3-D bottleneck on personal computers that are unable to saturate the TVP4020 rendering capabilities. The unit calculates the slope and setup information, and performs high precision floating- to fixed-point conversion. The unit significantly reduces the load on the central processing unit and PCI bus, and is a general-purpose design that supports any 3-D API.

Figure 3–1. Geometry Setup Unit



The geometry setup unit accepts the coordinates of vertices plus color, depth, fog, and texture parameters. It accepts the input parameters in either fixed-point format or in Institute of Electrical and Electronic Engineers (IEEE) single-precision floating-point format; internal calculations are performed in floating-point format. Vertex sharing for meshes, fans, and polylines is supported, with the shared vertices being loaded only once.

3.2 Graphics Processor

The graphics processor unifies 3-D, 2-D, and video operations into the same processing pipeline. This provides flexibility in data handling, while ensuring no duplication of functions.

The graphics processor rasterizes each primitive to determine the pixels covered on the screen. It then processes each pixel through the following sequence of operations:

- 1) Clips to window
- 2) Applies stipple pattern
- 3) Performs depth and stencil tests
- 4) Calculates texture address, fetches and formats texture data
- 5) Key tests color
- 6) Updates depth and stencil buffers
- 7) Interpolates color
- 8) Applies texture
- 9) Applies fog
- 10) Applies transparency
- 11) Dithers to final color format
- 12) Applies logic operations
- 13) Updates framebuffer
- 14) Updates extent and picking statistics

Each stage is optional and may be omitted. If a pixel fails any of the tests, it does not take part in any further processing. For example, if a pixel fails the depth test the processor does not calculate an address for it, nor does it read and apply texture data from memory. This ensures that time is not wasted processing pixels that will not be written to memory.

The graphics processor supports a high degree of parallelism that allows several pixels to be processed at the same time. The design ensures a high throughput while maintaining a low latency between primitives. It is not necessary for one primitive to be finished before the next one starts.

3.3 Host Interfaces

The TVP4020 can be used with a number of host interfaces to achieve high performance processing.

3.3.1 AGP Interface

AGP is Intel's high-performance, component-level interconnector targeted at 3-D display applications that use a 66-MHz PCI specification as a baseline.

The characteristics for the TVP4020 AGP interface are as follows:

- 66-MHz operation
- DMA and execute mode support
- Sideband addressing

Implementing these features enables the TVP4020 to achieve over 250 Mbytes/second bandwidth from the host for instructions, textures, and video data (limited by the host system throughput).

The add-in slot, defined for AGP, uses a new connector body that is not compatible with the PCI connector; therefore, boards designed for use in an AGP slot are not mechanically interchangeable with PCI boards.

3.3.1.1 DMA Mode Texturing

To achieve optimal performance, the TVP4020 treats the local synchronous memory as working texture storage, and uses the performance of AGP to use system memory as high-speed, virtual storage for textures that are not currently held in memory. This demand-loaded texture mechanism is optimized to transfer data directly into local memory through a DMA controller.

3.3.1.2 Execute Mode Texturing

To achieve optimal performance in low-cost systems, the TVP4020 implements the AGP execute model and can directly access textures stored in system memory, without loading them into local memory.

3.3.2 PCI Interface

The host PCI interface on the TVP4020 is compliant with version 2.1 of the Video Electronics Standards Association (VESA) *Peripheral Component Interconnect (PCI) Specification* and contains first-in first-out (FIFO) and DMA controllers. Control registers for the host interface are memory mapped onto the PCI bus. The host can read back control and state information from the programmable registers.

Two methods of communication are available between the host and the TVP4020: either direct to the FIFO where the TVP4020 acts as a PCI slave; or alternatively, by programming the TVP4020 to function as a PCI master and use the internal DMA controller to fetch commands from the FIFO.

3.3.2.1 PCI Characteristics

The host PCI interface has the following characteristics:

- Glueless interface – simple and low cost design
- 32-bit master/slave – maximum speed
- Big-endian – avoids byte swapping on PowerMacs™
- Plug and play – VESA *PCI Specification* (version 2.1) compliant

3.3.2.2 DMA1 Controller - Graphics Core

The DMA1 controller (graphics core) has the following characteristics:

- Autonomous– setup/fetch parallelism
- No wait state – maximum transfer rate
- Programmable block size – large DMA buffers

3.3.2.3 DMA2 Controller - Direct to Memory

The DMA2 controller (direct to memory) has the following characteristics:

- Fast texture/image uploading and downloading
- Fast software MPEG2 downloading

3.3.2.4 Input FIFO

The input FIFO has the following characteristics:

- 256 entries – fetch/draw parallelism
- Burst mode – bursts for programmed I/O
- PCI disconnect on full – avoids polling FIFO

3.3.2.5 Interrupt Controller

The interrupt controller has the following characteristics:

- End-of-DMA – allows DMA chaining
- VSYNC – efficient double buffering
- Scanline – special effects
- Video streams – separates input and output frame interrupts
- I²C start condition – alerts host to start of I²C transfer
- Sync – indicates graphics core is idle
- Error – for example, writing to a full FIFO

3.3.2.6 Core Bypass to Memory

The core bypass offers fast access to memory for software rendering.

3.4 Memory Interface

The TVP4020 memory subsystem uses SGRAM or compatible SDRAM to supply the memory bandwidth for 3-D operations and display updates.

3.4.1 SGRAM/SDRAM Overview

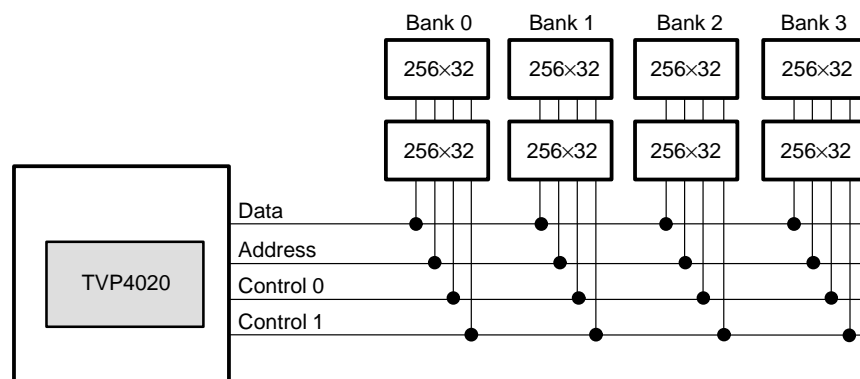
The SGRAM and SDRAM have the following characteristics:

- 64-bit synchronous memory interface
 - SGRAM for best performance (block filling and write masking)
 - SDRAM for reduced cost
- Two 256K×32 parts for every bank of memory (2 Mbytes)
- Four banks of memory maximum (2, 4, 6, or 8 Mbytes of total memory)
- 83-MHz and above SGRAM/SDRAM clock speeds
- High-speed block filling and masked writing
- Single-cycle burst readings

3.4.2 Memory Organization

Each bank of the TVP4020 memory subsystem is made up of two 32-bit wide devices. The data and address lines are common to all the memory devices. There are two sets of control lines that are provided to reduce loading: they are driven identically. Figure 3–2 shows one set of control lines driving bank 0 and bank 1, with the second set driving bank 2 and bank 3. Alternatively, the control lines can be split along the upper and lower devices in each bank.

Figure 3–2. Memory Organization

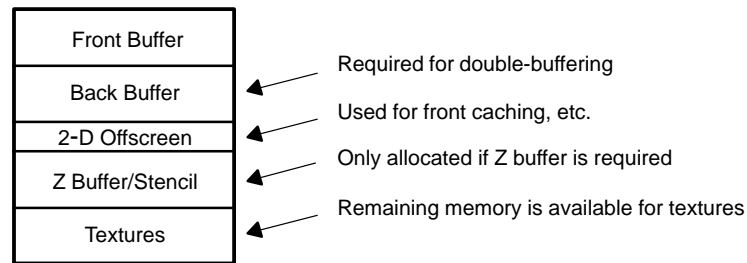


To minimize page breaks, the TVP4010 can store and access data in memory as 2-D patches. This is particularly useful for texture maps, where texture can be accessed in any direction through memory. By storing the data in a 2-D format, the chances of a page break are reduced. The TVP4020 drivers allow configurable texture compression on download, thereby saving memory and increasing performance.

3.4.3 Flexible Multifunctional Memory Layout

The TVP4010 stores a variety of data and color formats in memory at the same time, as shown in Figure 3–3. The organization of data in memory is unconstrained and allows mixing of buffers of any data type. The color data (ready for display) is referred to as the framebuffer, which, in double-buffering applications such as games and animations, is made up of a front buffer and a back buffer (one being drawn to, the other being displayed). After these buffers are allocated, the Z buffer (depth), stencil buffer and texture buffer are stored in the remaining memory.

Figure 3–3. Multifunctional Memory Layout



The multifunctional nature of the memory organization allows the TVP4020 to store the different buffers anywhere in the same physical memory, minimizing memory waste and offering a simplified programming model. It is not necessary to store all data of a particular type together; thus, a texture map may be followed by a depth buffer or a framebuffer or another texture map.

The video graphics array (VGA) is an independent unit that shares the memory controller and accesses the framebuffer when VGA mode is active.

3.4.4 Supported Memory Data Formats

The TVP4020 supports a variety of data formats for storing and retrieving information in the various memory buffers.

3.4.4.1 Framebuffer Storage Color Formats

THE TVP4020 supports the following color formats for framebuffer storage (front buffer and back buffer) and supports both RGBA and BGRA ordering of pixels.

- 8-bit RGBA – 2:3:2:1 or 3:3:2:–
- 16-bit RGBA – 5:5:5:1 or 5:6:5:– or 4:4:4:–
- 24-bit RGB – 8:8:8
- 32-bit RGBA – 8:8:8:8
- CI – 8:–:–:–

3.4.4.2 Texture Formats

Textures can be stored in memory in the formats that follow. These formats are a superset of the framebuffer storage formats due to the support for 4- and 8-bit palletized textures and the YUV formats. The use of palletized textures significantly reduces the texture memory requirements, and enhances performance.

If the texture format is different than the framebuffer format then the graphics core performs the conversion between color formats. If the texture map is 4- or 8-bit palletized, then the user defined on-chip LUT is used to convert the data into full RGBA.

3.4.4.3 Supported Texture Formats

The following texture formats are supported:

- 4-bit palletized
- 8-bit palletized
- 8-bit RGBA – 2:3:2:1 or 3:3:2:–
- 16-bit RGB – 5:5:5:1 or 5:6:5:– or 4:4:4:–
- 24-bit RGB – 8:8:8
- 32-bit RGBA – 8:8:8:8
- YUV: – 4:4:4 or 4:2:2 or 4:2:0

3.4.4.4 Depth and Stencil Formats

The use of depth and stencil buffers is optional. Not using depth or stencil buffers increases the memory available to support higher display resolutions and more local texture storage.

The following depth and stencil formats are supported:

- Depth: 0, 15, or 16 bits
- Stencil: 0 or 1 (if 1, then the depth must be set to 15)

3.5 Video Streams Interface

The TVP4020 supports independent input and output of digital video. The input stream complies with the *Video Electronics Standard Association (VESA) Video Module Interface (VMI) Specification*. Input data may be scaled and filtered before being written to local memory. The output stream is based on the VMI specifications work with common National Television Standards Committee/Phase Alternating Line (NTSC/PAL) encoders. Both streams are independent of the video output to the monitor.

The interface may be configured to meet different needs. Table 3–1 describes the modes supported.

Table 3–1. Digital Video I/O

Input Width	Output Width	Notes
8	8	Simultaneous input and output
16	0	Input only zoom video port
0	16	Output only zoom video port

Input data may be scaled and filtered to reduce memory requirements. The output stream may be gamma corrected and converted from RGB to YUV. The output video is a slave and supplies data on demand from the external encoder chip. Both streams support automatic hardware triple-buffering.

Separate control is provided for vertical blank interval (VBI) data such as closed caption, Teletext, or Intercast. VBI data may be inserted into the output stream or extracted from the input stream, as required.

3.5.1 Control Buses

The interface supports two buses for programming devices that are connected to the video streams. The I²C bus is a two-wire serial bus commonly used to control chips that supply or receive data on the video ports. The general-purpose bus is a parallel bus that supports a higher bandwidth and uses an 8-bit data path with a 4-bit address. If the parallel bus is used, only input video is available.

3.5.2 External ROM

The TVP4020 external read-only memory (ROM) stores the video basic input/output systems (BIOS) and the power-up configuration information, reducing the need for configuration resistors in board designs. Access to the

ROM is through the general-purpose bus when both video streams are disabled.

If the ROM is flash programmable, the contents may be modified under software control.

3.6 RAMDAC

The TVP4020 incorporates a high-performance 230-MHz RAMDAC that is the equivalent of the TVP3026B RAMDAC.

3.6.1 RAMDAC Characteristics

The TVP4020 RAMDAC has the following characteristics:

- 230 MHz, 64-bits wide
- Supports resolutions up to 1600×1200×16 at 85-Hz refresh rate
- Supports packed pixel formats
- Supports per-window double buffering
- Color depths of 8, 16, 24, and 32 bits/pixel
- Dot clock and memory clock phase-locked loops (PLLs)
- Triple 8-bit DACs
- 64×64×2 hardware cursor

3.6.2 Display Resolutions

The TVP4020 supports all the standard screen resolutions at ergonomical refresh rates. For each resolution and color depth described in Table 3–2, the number represents the maximum refresh rate supported.

Table 3–2. Standard Screen Resolutions

Resolution	Color Depth			
	8 bpp	16 bpp	24 bpp	32 bpp
320×200	220 Hz	220 Hz	220 Hz	220 Hz
640×480	220 Hz	220 Hz	220 Hz	220 Hz
800×600	220 Hz	220 Hz	204 Hz	153 Hz
1024×768	220 Hz	186 Hz	124 Hz	93 Hz
1152×860	153 Hz	153 Hz	107 Hz	85 Hz
1280×1024	118 Hz	118 Hz	85 Hz	60 Hz
1600×1200	85 Hz	85 Hz	–	–

3.6.3 Display Data Channels

Two control lines are dedicated on the TVP4020 to support display data channel (DDC) DDC1 and DDC2AB+ monitor configuration utilities. The DDC2 serial bus is independent of the serial bus in the VMI.

3.7 SVGA

The SVGA unit (see Table 3–3) is register-level compatible with standard VGA devices and requires no software emulation. It supports all standard VGA modes, and h100 and h101 SVGA modes. Using universal VESA BIOS extension (UniVBE) drivers, the resolution may be increased to 1600×1200. The SVGA unit is a high-performance 32-bit implementation.

Table 3–3. SVGA Unit

Mode (Hex)	Alpha Format	Char Size	Colors	Max Page	Type Format	Resolution
00 0	40×25	8×8	16/256K bw	8	Alpha	320×200
0*	40×25	8×14	16/256K bw	8	Alpha	320×350
0+	40×25	9×16	16/256K bw	8	Alpha	360×400
01 1	40×25	8×8	16/256K	8	Alpha	320×200
1*	40×25	8×14	16/256K	8	Alpha	320×350
1+	40×25	9×16	16/256K	8	Alpha	360×400
02 2	80×25	8×8	16/256K bw	8	Alpha	640×200
2*	80×25	8×14	16/256K bw	8	Alpha	640×350
2+	80×25	9×16	16/256K bw	8	Alpha	720×400
03 3	80×25	8×8	16/256K	8	Alpha	720×200
3*	80×25	8×14	16/256K	8	Alpha	640×350
3+	80×25	9×16	16/256K	8	Alpha	720×400
04 4	40×25	8×8	4/256K	1	Graph	320×200
05 5	40×25	8×8	4/256K bw	1	Graph	320×200
06 6	80×25	8×8	2/256K bw	1	Graph	640×200
07 7	80×25	9×14	bw	8	Alpha	720×350
7+	80×25	9×16	bw	8	Alpha	720×400
0D D	40×25	8×8	16/256K	8	Graph	320×200
0E E	80×25	8×8	16/256K	4	Graph	640×200
0F F	80×25	8×14	bw	2	Graph	640×350
10 10	80×25	8×14	16/256K	2	Graph	640×350
11 11	80×30	8×16	2/256K	1	Graph	640×480
12 12	80×30	8×16	16/256K	1	Graph	640×480
13 13	40×25	8×8	256/256K	1	Graph	320×200

Table 3–4 describes the supported VESA SVGA modes.

Table 3–4. VESA SVGA Modes

Mode (Hex)	Pixels	Colors
100	640×400	256
101	640×480	256

Software Drivers

This chapter describes the 3Dlabs software drivers that are incorporated by the TVP4020 to extract maximum processor and system performance.

Topic	Page
4.1 2-D Drivers	4-2
4.2 3-D Drivers	4-2
4.3 Other	4-2

4.1 2-D Drivers

The TVP4020 is a high performance 2-D engine and video engine with optimized drivers for:

- Windows™ 95 with DirectDraw™
- Windows NT™ with DirectDraw
- Microsoft™ DirectX™
- Other drivers are available on request.

4.2 3-D Drivers

The TVP4020 accelerates key consumer-focused 3-D APIs and drivers. The TVP40x0 family of PERMEDIA processors is the reference port for many 3-D drivers:

- Microsoft Direct3D™
- OpenGL
- Creative Labs CGL™
- Autodesk Heidi™ for 3D Studio MAX™ support

4.3 Other

The TVP4020 also supports VGA BIOS software.

OEM Focused Solutions

This chapter defines the range of TVP4020-based add-in boards and motherboards that can be designed to meet the requirements of particular markets and their price/performance criteria. 3DLabs produces reference designs for many of the more common configurations, all of which support a full suite of software drivers including Windows 95, Windows NT, OpenGL, and Direct3D.

Topic	Page
5.1 TVP4020 for Windows 95 and Windows NT	5-2
5.2 Early Access Program	5-2
5.3 Manufacturing Kits	5-2
5.4 OEM Solution Designs	5-3
5.5 Typical Resolutions and Memory Configurations	5-6
5.6 Feature Set Summary	5-10

5.1 TVP4020 for Windows 95 and Windows NT

For users seeking a 3-D accelerator for Windows 95 and Windows NT applications based on Direct3D, OpenGL, or 3D Studio MAX, there is no better acceleration solution than a 2- to 8-Mbyte graphics board based on the TVP4020 processor.

This solution delivers unrivaled 3-D and multimedia acceleration for both business and consumer 3-D applications such as Web browsers, authoring tools, games, and personal design packages.

5.2 Early Access Program

The TVP4020 Early Access Program (EAP) is for independent hardware vendors (IHVs) and original equipment manufacturers (OEMs) who wish to work closely with Texas Instruments to bring TVP4020-based designs to market quickly and efficiently. The program supports a close technical and marketing collaboration and is open to IHVs committed to developing TVP4020-based solutions. It offers:

- Close technical support, and joint marketing and press programs
- Early access to design engineers, design guides, and application notes
- Priority supply of sample parts and access to reference board schematics
- Participation in driver beta programs

5.3 Manufacturing Kits

To minimize development times, 3Dlabs provides the TVP4020 Manufacturing Kit. This kit contains the TVP4020-based reference boards along with extensive hardware design documentation, board schematics, PC-board files, design guides, application notes, as well as access to a full suite of 3-D and 2-D device drivers.

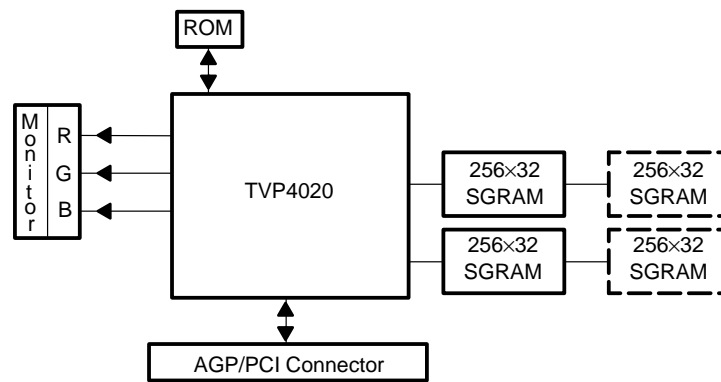
5.4 OEM Solution Designs

A number of OEM solutions are available using the TVP4020.

5.4.1 3-D Solution

The 3-D board, shown in Figure 5-1, sets the standard for low-cost, high volume 3-D, 2-D, and video acceleration.

Figure 5-1. 3-D Solution

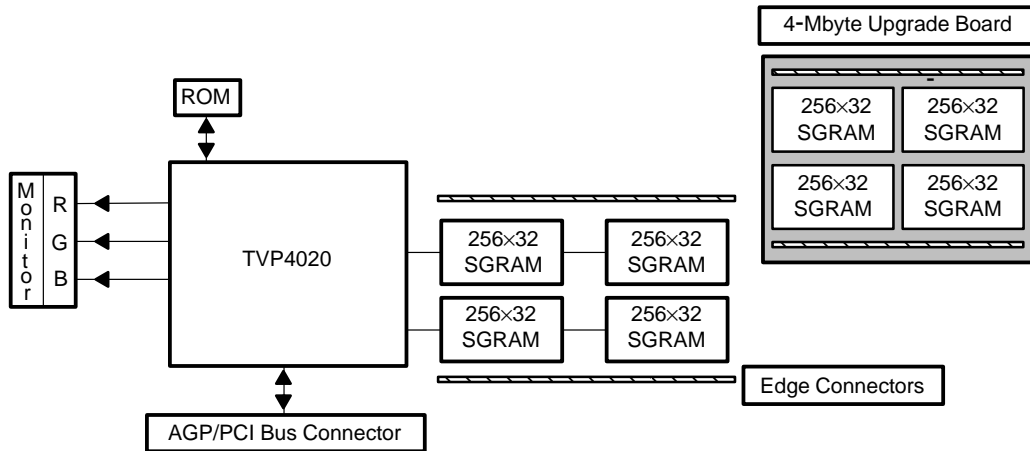


It is based on a TVP4020 with 2 Mbytes of memory and the option for an additional 2 Mbytes. It may be built as either a standard PCI board or as an AGP card. If built as an AGP card, it uses the AGP execute model to avoid storing textures locally; this frees memory for higher resolution screens.

5.4.2 Business 3-D Solution

The business 3-D board, shown in Figure 5-2, is designed for the business or home user and adds extra memory for higher screen resolutions and extended local texture storage.

Figure 5–2. Business Solution

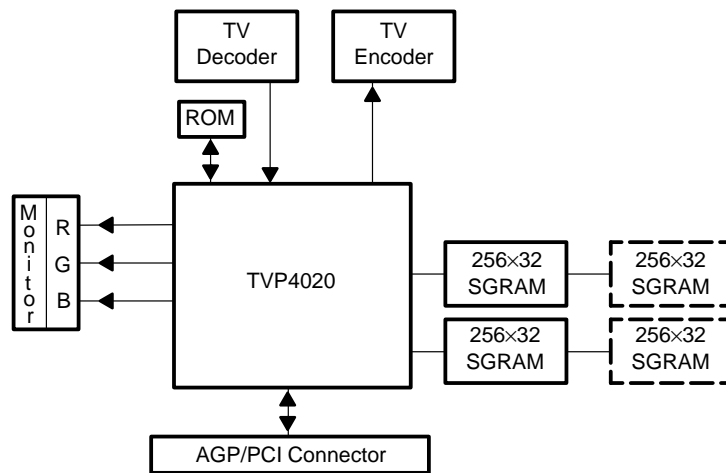


The memory can be either a standard PCI board or an AGP card. As an AGP card, it uses the DMA model to transfer textures into local memory where it caches them for higher performance.

5.4.3 Home PC Solution

The home PC board, shown in Figure 5–3, takes the 3-D board and adds extra hardware to enable TV input and output.

Figure 5–3. Home PC Solution



5.4.4 Other Solutions

Other TVP4020 solutions include:

- Hardware MPEG2
- Hardware decompression to the video streams port
- Video conferencing
- Hardware video conferencing support to video streams port

5.5 Typical Resolutions and Memory Configurations

Table 5–1 describes 3-D color and display resolutions and the texture storage supported for some typical memory configurations. All 3-D content is assumed to be double buffered.

The texture column indicates the amount of texture memory available after the framebuffer (including back buffer) and depth buffer are allocated.

Table 5–1. 3-D Color and Display Resolutions

Pixels		Color	Z	Texture Space		
Width	Height			2-Mb Card	4-Mb Card	8-Mb Card
512	384	8-bit	0-bit	1.6 Mb	3.6 Mb	7.6 Mb
512	384	8-bit	16-bit	1.2 Mb	3.2 Mb	7.2 Mb
512	384	16-bit	0-bit	1.2 Mb	3.2 Mb	7.2 Mb
512	384	16-bit	16-bit	0.8 Mb	2.8 Mb	6.8 Mb
512	384	24-bit	0-bit	0.9 Mb	2.9 Mb	6.9 Mb
512	384	24-bit	16-bit	0.5 Mb	2.5 Mb	6.5 Mb
512	384	32-bit	0-bit	0.5 Mb	2.5 Mb	6.5 Mb
512	384	32-bit	16-bit	0.1 Mb	2.1 Mb	6.1 Mb
640	400	8-bit	0-bit	1.5 Mb	3.5 Mb	6.48 Mb
640	400	8-bit	16-bit	1 Mb	3 Mb	7 Mb
640	400	16-bit	0-bit	1 Mb	3 Mb	7 Mb
640	400	16-bit	16-bit	0.5 Mb	2.5 Mb	6.5 Mb
640	400	24-bit	0-bit	0.5 Mb	2.5 Mb	6.5 Mb
640	400	24-bit	16-bit	0.05 Mb	2 Mb	6 Mb
640	400	32-bit	0-bit	0.05 Mb	2 Mb	6 Mb
640	400	32-bit	16-bit	–	1.6 Mb	5.6 Mb
640	480	8-bit	0-bit	1.5 Mb	3.5 Mb	6.5 Mb
640	480	8-bit	16-bit	0.8 Mb	2.8 Mb	6.8 Mb
640	480	16-bit	0-bit	0.8 Mb	2.8 Mb	6.8 Mb
640	480	16-bit	16-bit	0.25 Mb	2.25 Mb	6.25 Mb
640	480	24-bit	0-bit	0.25 Mb	2.25 Mb	6.25 Mb
640	480	24-bit	16-bit	–	1.7 Mb	5.7 Mb
640	480	32-bit	16-bit	–	1.1 Mb	5.1 Mb
800	600	8-bit	0-bit	1 Mb	3 Mb	7 Mb
800	600	8-bit	16-bit	–	2.1 Mb	6.1 Mb
800	600	16-bit	0-bit	–	2.1 Mb	6.1 Mb
800	600	16-bit	16-bit	–	1.3 Mb	5.3 Mb
800	600	24-bit	0-bit	–	1.3 Mb	5.3 Mb
800	600	24-bit	16-bit	–	0.35 Mb	4.35 Mb
800	600	32-bit	0-bit	–	0.35 Mb	4.35 Mb

Table 5–1. 3-D Color and Display Resolutions (Continued)

Pixels				Texture Space		
Width	Height	Color	Z	2-Mb Card	4-Mb Card	8-Mb Card
800	600	32-bit	16-bit	–	–	3.6 Mb
1024	768	8-bit	0-bit	0.5 Mb	2.5 Mb	6.5 Mb
1024	768	8-bit	16-bit	–	1 Mb	5 Mb
1024	768	16-bit	0-bit	–	1 Mb	5 Mb
1024	768	16-bit	16-bit	–	-	3.6 Mb
1024	768	24-bit	0-bit	–	-	3.6 Mb
1024	768	24-bit	16-bit	–	-	2 Mb
1024	768	32-bit	0-bit	–	-	2 Mb
1024	768	32-bit	16-bit	–	-	0.5 Mb
1280	1024	8-bit	0-bit	–	1.5 Mb	5.5 Mb
1280	1024	8-bit	16-bit	–	–	3.1 Mb
1280	1024	16-bit	0-bit	–	–	3.1 Mb
1280	1024	16-bit	16-bit	–	–	0.5 Mb
1280	1024	24-bit	0-bit	–	–	0.5 Mb
1280	1024	24-bit	16-bit	–	–	–
1280	1024	32-bit	0-bit	–	–	–
1280	1024	32-bit	16-bit	–	–	–

Table 5–2 describes the 2-D screen resolutions. supported by 2-Mb, 4-Mb, and/or 8-Mb memory, as specified by X.

Table 5–2. 2-D Screen Resolutions

Pixels		Color	Card Size		
Width	Height		2-Mb Card	4-Mb Card	8-Mb Card
512	384	8-bit	X	X	X
512	384	16-bit	X	X	X
512	384	24-bit	X	X	X
512	384	32-bit	X	X	X
640	400	8-bit	X	X	X
640	400	16-bit	X	X	X
640	400	24-bit	X	X	X
640	400	32-bit	X	X	X
640	480	8-bit	X	X	X
640	480	16-bit	X	X	X
640	480	24-bit	X	X	X
640	480	32-bit	X	X	X
800	600	8-bit	X	X	X
800	600	16-bit	X	X	X
800	600	24-bit	X	X	X
800	600	32-bit	X	X	X
1024	768	8-bit	X	X	X
1024	768	16-bit	X	X	X
1024	768	24-bit	–	X	X
1024	768	32-bit	–	X	X
1280	1024	8-bit	X	X	X
1280	1024	16-bit	–	X	X
1280	1024	24-bit	–	X	X
1280	1024	32-bit	–	–	X
1600	1200	8-bit	X	X	X
1600	1200	16-bit	–	X	X
1600	1200	24-bit	–	–	X
1600	1200	32-bit	–	–	X

5.6 Feature Set Summary

The TVP4020 features are summarized in the sections that follow.

5.6.1 Texture Mapping

The TVP4020 has the following texture mapping features:

- True perspective correcting
- Bilinear filtering
- Palletized and RGB texturing
- Transparency mapping
- Local texture buffering
- Specular highlighting
- Fast texture loading
- Color keying

5.6.2 3-D Rendering

The TVP4020 has the following 3-D rendering features:

- Points, lines, triangles, and bitmaps
- Gouraud and flat shading
- 8-, 16-, 24-, or 32-bit RGBA
- Depth (Z) buffering
- Alpha blending
- Full-screen antialiasing
- Fogging and depth cueing
- Dithering
- Area stippling
- Stencil testing and stencil buffering
- Scissor testing and logic operations

5.6.3 Display Features

The TVP4020 has the following display features:

- 8-, 16-, 24-, or 32-bit RGB
- 8-bit color index
- Double and triple buffering
- Hardware dithering
- Hardware panning
- Per-window double buffering
- Overlays

5.6.4 Fast Video Playback

The TVP4020 has the following video playback features:

- MPEG2 playback acceleration
- YUV color space conversion
- Scaling (bilinear filtered)
- Dithering
- Color keying (blue screen)

5.6.5 GUI Acceleration

The TVP4020 has the following GUI features:

- Bit-aligned block transfer raster operations
- Points, lines, polygons
- Filling and text primitives
- Fast linear framebuffer
- On-chip SVGA
- Windows

5.6.6 PCI/AGP Interface

The TVP4020 has the following PCI/AGP interface features:

- 32-bit glueless PCI V2.1
- 33-MHz PCI/66-MHz AGP
- Target and master support
- DMA mastering
- 32-entry command FIFO
- Big-endian apertures on bus
- Interrupts

5.6.7 Memory Architecture

The TVP4020 has the following memory architecture features:

- 64-bit SGRAM/SDRAM interface
- Single multifunction memory
- Optimal memory usage
- 2 to 8 Mbytes

5.6.8 Display Resolutions

The TVP4020 features the following display characteristics:

- 320×200 to 1600×1200
- Ergonomical refresh rates

5.6.9 Programming

The TVP4020 supports the following programs:

- Direct3D and OpenGL
- Windows 95 and Windows NT
- Creative Labs CGL
- Heidi for 3D Studio MAX

5.6.10 Industry Standard Package BGA

The TVP4020 features an industry standard ball-grid array (BGA) package at 3.3 V (5-V tolerant I/O).

5.6.11 Video Output

The TVP4020 supports a 230-MHz RAMDAC interface.

5.6.12 TV In, TV Out

The TVP4020 supports simultaneous digital video input and output.

5.6.13 Green PC, and Plug and Play

The TVP4020 features VESA display power-management support.

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