TEXAS INSTRUMENTS

9900

TMS9927 and TMS9937 Single-Chip Video Timers/Controllers

MICROPROCESSOR SERIES™

Data Manual

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1. INTRODUCTION

1.1 DESCRIPTION

The TMS9927/TMS9937 single-chip video timer/controllers (VTC) from Texas Instruments are produced with silicon-gate, N-channel, MOS technology. These 40-pin devices generate video display timing signals for standard and nonstandard CRT monitors incorporating both interlaced and noninterlaced formats. The TMS9927 provides noninterlaced operation with either an even or odd number of scan lines per data row; and interlaced operation with an even number of scan lines per data row. The TMS9937 provides the same operational features as the TMS9927, plus interlaced operation with an odd number of scan lines per data row. Character distortion-caused by uneven beam current-common to odd field/even field interlacing of alphanumeric displays, may be eliminated by programming the TMS9937 for an odd number of scan lines per data row. The TMS9927/TMS9937 are designed as memory-mapped I/O devices, but can be communicated with over a CRU interface via the TMS9901.

The TMS9927/TMS9937 provide nine, user-programmable control registers. Seven of the registers control horizontal and vertical formatting, and two registers control the cursor address. The inherent flexibility of the control registers make possible a wide variety of cost-effective applications.

1.2 KEY FEATURES

- Standard and nonstandard CRT monitors
- Interlaced or noninterlaced formats
- Scrolling capability
- Programmable display format:
  - Characters per row
  - Rows per frame
  - Raster scans per row
  - Raster scans per frame
- Programmable monitor timing:
  - Blanking
  - Horizontal sync
  - Vertical sync
  - Composite sync
- Programmable via microprocessors or PROMS
- Cursor output
- N-Channel, silicon gate MOS device
- Standard 40-pin plastic or ceramic package
- Equivalent to CRT 5027/CRT 5037 by SMC.

1.3 TYPICAL APPLICATION

The TMS9927/TMS9937 may be interfaced to a CPU through the communications register unit (CRU) via a TMS9901 as shown in Figure 1. Following is a tutorial discussion of this application. Subsequent sections of this manual detail the many aspects of the TMS9927/TMS9937 usage introduced here. The TMS9901 accepts serial data bits and serial select bits from the CRU and creates parallel data select lines for the TMS9927/TMS9937. One other bit, chip select, not shown on the diagram, through the TMS 9901 interface causes the VTC to monitor its data and select lines.

The character column lines (H0-H7) and row lines (DR0-DR5) are combined to address the refresh RAM. The refresh RAM outputs the seven-bit ASCII character for display. The TMS4710 character generator uses the raster scan counter (R0-R3) outputs to select the row of the dot matrix for output. A shift register then shifts the dot information to the video circuit at the video dot frequency.

The TMS9927/TMS9937 also feature self-load functions as shown in Figure 2. This function is effected by placing the SELF-LOAD command on the VTC select lines and strobing DATA STROBE ($\overline{DS}$). SELF-LOAD will cause the TMS9927/TMS9937 to transmit addresses on their row select lines to the control PROM (74S288). The outputs of the control PROM are loaded into the VTC control registers. There are two types of self-load: processor and nonprocessor. The NONPROCESSOR SELF-LOAD function will automatically start the timing chain after load is completed. The PROCESSOR SELF-LOAD function will simply cause a self-load and then wait for a START command from the processor. The command to the VTC, which causes self-load, should be applied for the entire duration of self-load.

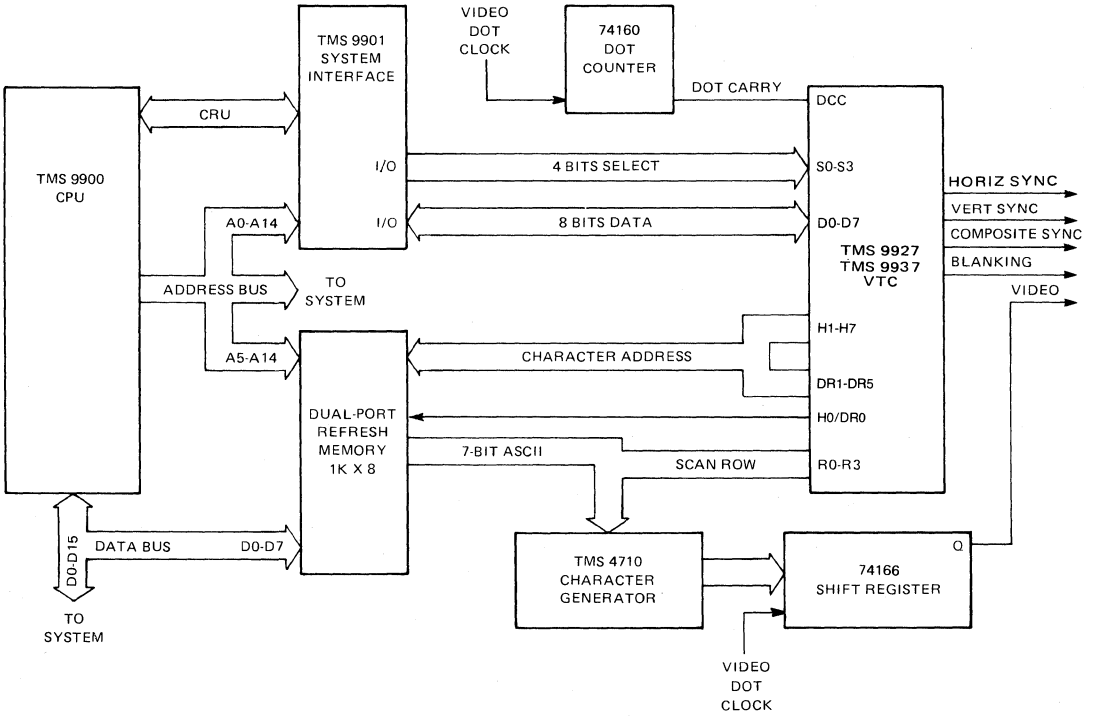


FIGURE 1 — TMS9901-BASED APPLICATION

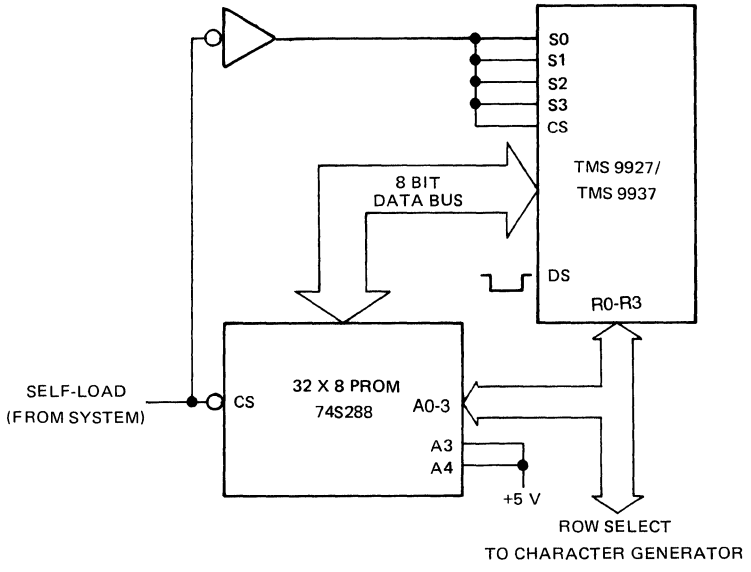


FIGURE 2 — TMS9927/TMS9937 SELF-LOAD FUNCTION

2. ARCHITECTURE

The architecture of the TMS9927/TMS9937 video timer/controller (VTC) diagrammed in Figure 3, permits maximum design flexibility. Simply by programming the control registers appropriately, most raster-scan CRTs may be controlled by the TMS9927/TMS9937.

The TMS9927/TMS9937 can be subdivided into five sections: CPU interface, cursor control, horizontal control, vertical control, and self-load. Each of these subsections will be discussed in the following paragraphs.

2.1 CPU INTERFACE

2.1.1 General

The select lines, S0-S3, select the control register for loading and reading via the data bus, D0-D7. The lines also select control functions for the device. Table 1 lists the 16 assignments for the four select lines. The bit assignments for the nine control registers are listed in Table 2. Note that both the cursor row address and character address can be read from and written to indicating that the VTC data bus is bidirectional.

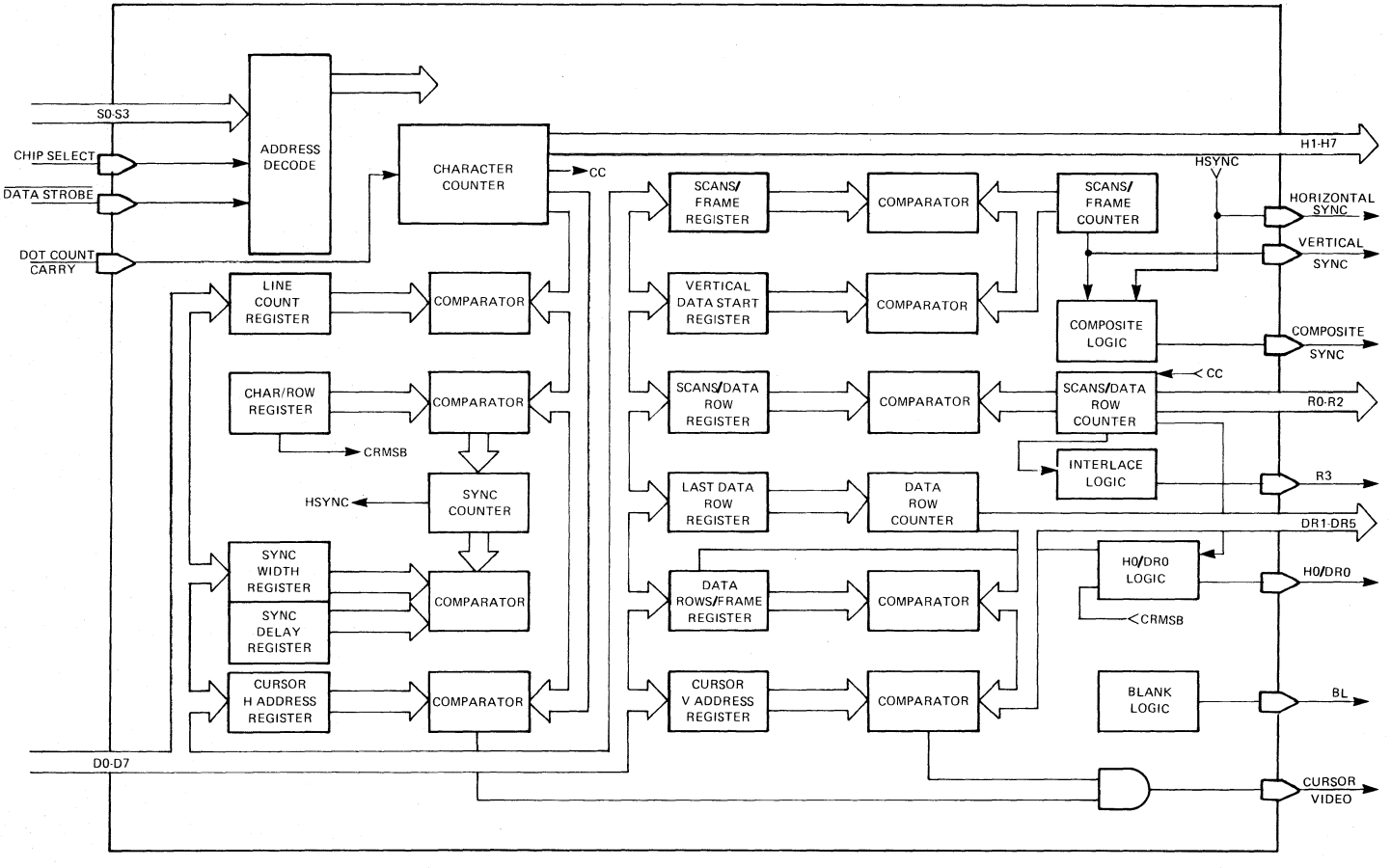


FIGURE 3 — TMS9927/TMS9937 ARCHITECTURE

TABLE 1 — SELECT LINE (S0-S3) COMMAND ASSIGNMENTS

S0	S1	S2	S3	COMMAND	REMARKS
0	0	0	0	LOAD CONTROL REGISTER 0	
0	0	0	1	LOAD CONTROL REGISTER 1	
0	0	1	0	LOAD CONTROL REGISTER 2	
0	0	1	1	LOAD CONTROL REGISTER 3	See Table 2
0	1	0	0	LOAD CONTROL REGISTER 4	
0	1	0	1	LOAD CONTROL REGISTER 5	
0	1	1	0	LOAD CONTROL REGISTER 6	
0	1	1	1	PROCESSOR SELF LOAD	Instructs TMS9927/TMS9937 to enter self-load mode.
1	0	0	0	READ CURSOR ROW ADDRESS	
1	0	0	1	READ CURSOR CHARACTER ADDRESS	
1	0	1	0	RESET	Resets timing chain to top left of page. Reset is latched on-chip by data strobe ($\overline{DS}$), and counters are held until released by START command.
1	0	1	1	UP SCROLL	Increments address of first displayed data row on page; i.e., prior to receipt of SCROLL command top line = 0, bottom line = 23; after receipt of SCROLL command top line = 1, bottom line = 0.
1	1	0	0	LOAD CURSOR CHARACTER ADDRESS	
1	1	0	1	LOAD CURSOR ROW ADDRESS	
1	1	1	0	START TIMING CHAIN	After a Reset or Processor SELF-LOAD command, this command releases the timing chain approximately one scan-line later. Synchronous operation of more than one TMS9927/TMS 9937 should have the dot counter held low during the $\overline{DS}$ for this command.
1	1	1	1	NON-PROCESSOR SELF-LOAD	TMS9927/TMS9937 will begin self-load via PROM when $\overline{DS}$ goes low. (The 1111 command should be maintained on S0-S3 long enough to guarantee self load, i.e., the scan counter should cycle at least once.) Self-Load is automatically terminated and timing chain initiated when the all ONEs condition is removed (independent of $\overline{DS}$). Synchronous operation of more than one TMS9927/TMS9937 should have the Dot Counter Carry held low when the command is removed.

TABLE 2 — CONTROL REGISTER BIT ASSIGNMENTS

REGISTER	FUNCTION	BITS							
Register 0	Horizontal character count	0	1	2	3	4	5	6	7
Register 1	Mode-interlaced/non interlaced	0							
	H sync width		1	2	3	4			
	H sync delay						5	6	7
Register 2	Scans/data row		1	2	3	4			
	characters/data row						5	6	7
Register 3	Skew bits	0	1						
	data rows/frame			2	3	4	5	6	7
Register 4	Scan lines/frame	0	1	2	3	4	5	6	7
Register 5	Vertical data start	0	1	2	3	4	5	6	7
Register 6	Last displayed data row			2	3	4	5	6	7
Register 7	Cursor character address	0	1	2	3	4	5	6	7
Register 8	Cursor row address			2	3	4	5	6	7

2.1.2 Device Initialization:

(a) Under microprocessor control—The device can be reset under system or program control by presenting a 1010 address on S0-S3. The device will remain reset at the top of the even field page until a START command is executed by presenting a 1110 address on S0-S3.

(b) Via "Self-Loading"—In a non-processor environment, the self-loading sequence is effected by presenting and holding the 1111 address on S0-S3, and is initiated by the receipt of the strobe pulse (DS). The 1111 address should be maintained long enough to ensure that all seven registers have been loaded (in most applications under one millisecond). The timing sequence will begin one line scan after the 1111 address is removed. In processor-based systems, self-loading is initiated by presenting the 0111 address to the device. Self-loading is terminated by the START command, which also initiates the timing chain.

2.1.3 Scrolling

In addition to the Register 6 storage of the last displayed data row, a SCROLL command (address 1011) increments the first displayed data row count to facilitate up-scrolling in certain applications.

2.2 CURSOR CONTROL

Two of the nine control registers on the TMS9927/TMS9937 are dedicated to cursor control. Register seven (R7) contains the eight-bit cursor character address (the address within a row that is the current cursor position). Register eight (R8) has the six-bit row address of the cursor. Under software control the position of the cursor is defined by writing to these registers. Hence, to move the cursor to the next horizontal position, the user simply increments the value of R7, the cursor character address register, assuming the cursor is not at the end of the line. Cursor position is tracked by the two registers, a feature that can be useful for light-pen applications. When the character counter (H lines) and data row counter (DR lines) outputs match the cursor character and cursor row address registers, respectively, a pulse is output on the CRV pin indicating the current cursor position. As the cursor position changes, the cursor address registers must be updated under software control.

2.3 HORIZONTAL CONTROL

The TMS9927/TMS9937 horizontal control section is contained in four registers, R0-R3, which control six functions, including:

- Total horizontal character count
- Horizontal sync width
- Horizontal sync delay
- Characters per data row
- Skew
- Data rows per frame

Bits in Register 1-3, which pertain to vertical formatting, are discussed in Section 2.4.

Horizontal control (Section 2.3) and vertical control (Section 2.4) are summarized in Tables 5 and 6.

2.3.1 Register 0

Register 0 (R0) contains the 8-bit horizontal character count. Because the count starts with zero, the horizontal character count is the total number of characters in a line minus one. For example, if a line contains 32 displayed characters plus eight characters for horizontal retrace, R0 will total 39.

2.3.2 Register 1

Four bits (1-4) of Register 1 (R1) are used to store the horizontal sync width in character times. From one to 15 character times are allowed. Horizontal sync delay is indicated with three bits (5-7). Sync delay can be given from one to seven character times. In each case, zero is not allowed. Bit seven is the least-significant bit.

2.3.3 Register 2

Register 2 (R2) contains the number of characters per data row. The MSB (bit 0) is not used. Three bits (5-7) indicate the number of active characters per data row: from 20 to 132 active characters may be present in a data row. The bit combinations indicating which of the eight predefined number of active characters per data row selected are listed in Table 3.

TABLE 3 — ACTIVE CHARACTERS PER LINE BIT COMBINATIONS, REGISTER 2

D5	D6	D7	ACTIVE CHARACTERS/DATA ROW
0	0	0	20
0	0	1	32
0	1	0	40
0	1	1	64
1	0	0	72
1	0	1	80
1	1	0	96
1	1	1	132

2.3.4 Register 3

Register 3 (R3) contains skew information. Two bits (0-1) can be programmed to skew or delay sync, blanking, and cursor a predefined number of character times. Table 4 lists the skew bit combinations and the resulting delay.

TABLE 4 — SKEW BIT COMBINATIONS AND RESULTING DELAYS

D0	D1	SYNC AND BLANK DELAY*	CURSOR DELAY*
0	0	0	0
0	1	2	1
1	0	1	0
1	1	2	2

*Character times

TABLE 5 — HORIZONTAL AND VERTICAL CONTROL

FUNCTIONS	DEFINITIONS
Horizontal Formatting:	
Characters/Data Row	A 3-bit code providing eight mask-programmable character lengths from 20 to 132. The standard device will be masked for the following character lengths; 20, 32, 40, 64, 72, 80, 96, and 132.
Horizontal Sync Delay	Three bits assigned providing up to 8 character times for generation of "front porch".
Horizontal Sync Width	Four bits assigned providing up to 15 character times for generaton of horizontal sync width.
Horizontal Line Count	Eight bits assigned providing up to 256 character times for total horizontal formatting
Skew Bits	A 2-bit code providing for a 0 to 2 character skew (delay) between the horizontal address counter and the blank and sync (horizontal, vertical, composite) signals allows retiming of video data prior to generation of composite video signal. The Cursor Video signal is also skewed as a function of this code.
Vertical Formatting:	
Interlaced/Non-interlaced	This bit provides for data presentation with odd/even field formatting for interlaced systems. It modifies the vertical timing counters as described below. A logic 1 establishes the interlace mode.
Scans/Frame	Eight bits assigned, defined according to the following equations: Let X = value of 8 assigned bits. 1) In interlaced mode — scans/frame = 2X + 513. Therefore for 525 scans, program X = 6. (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields. Range = 513 to 1023 scans/frame, odd counts only. 2) In non-interlaced mode — scans/frame = 2X + 256. Therefore for 262 scans, program X = 3. (00000011). Range = 256 to 766 scans/frame, even counts only. In either mode, vertical sync width is fixed at three horizontal scans (= 3H).
Vertical Data Start	Eight bits defining the number of raster scans from the leading edge of vertical sync until the start of display data. At this raster scan, the data row counter is set to the data row address at the top of the page.
Vertical Rows/Frame	Six bits assigned providing up to 64 data rows per frame.
Last Data Row	Six bits to allow up or down scrolling via a preload defining the count of the last displayed data row.
Scans/Data Row	Four bits assigned providing up to 16 scan lines per data row.

2.4 VERTICAL CONTROL

The vertical control section consists of three registers, R4-R6, and parts of R1-R3. The vertical control functions are:

- Raster scans per frame
- Vertical data start
- Last displayed data row
- Interlaced mode indicator
- Scans per data row
- Data rows per frame

Vertical control is summarized in Tables 5 and 6.

2.4.1 Registers 1-3

Three vertical control functions are performed in control registers R1-R3. They are interlaced mode indicator, scans per data row, and data rows per frame.

R1 bit 0 is used to indicate the interlace mode; a one in this bit indicates interlaced mode and a zero indicates noninterlaced operation.

For the TMS9927, both interlaced and non-interlaced modes, R2 bits 1-4 are used to store the number of raster scans per data row minus 1; e.g. if 12 scans are wanted per data row, this section of R2 would contain 11. In the interlaced mode, this section of R2, must contain an even number (minus one) since the LSB of the scan also serves as the odd or even field indicator.

For the TMS9937, interlaced mode only, R2 bits 1-4 are used to store the number of raster scans per data row minus 2; i.e., if 15 scans are wanted per data row, this section of R2 must contain 13. In this mode, unlike the TMS9927, this section of R2 can contain an even or odd number (minus 2). In non-interlaced mode, operation is the same as the TMS9927.

R3 bits 2-7 are used to indicate the total number of data rows per frame minus one.

TABLE 6 — CONTROL REGISTERS PROGRAMMING CHART

FUNCTIONS	DEFINITIONS
Character/Data Row:	Horizontal Line Count: Total characters/Line = N + 1, N = 0 to 225 = (D7 = LSB)
	D5 D6 D7 — Active Characters/Data Row 0 0 0 = 20 0 0 1 = 32 0 1 0 = 40 0 1 1 = 64 1 0 0 = 72 1 0 1 = 80 1 1 0 = 96 1 1 1 = 132
Horizontal Sync Delay:	= N, from 1 to 7 character times (D7 = LSB) (N = 0 disallowed)
Horizontal Sync Width:	= N, from 1 to 15 character times (D4 = LSB) (N = 0 disallowed)
Skew Bits:	D1 D0 — Sync/Blank Delay (Character Times) — Cursor Delay (Character Times) 0 0 — 0 — 0 1 0 — 1 — 0 0 1 — 2 — 1 1 1 — 2 — 2
Scans/Frame:	Eight bits assigned, defined according to the following equations: Let X = value of 8 assigned bits. (D7 = LSB) 1) In interlaced mode – scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields. Range = 513 to 1023 scans/frame, odd counts only. 2) In non-interlaced mode – scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011). Range = 256 to 766 scans/frame, even counts only. In either mode, vertical sync width is fixed a three horizontal scans (= 3H).
Vertical Data Start:	N = number of raster lines delay after leading edge of vertical sync of vertical start position. (D7 = LSB)
Data Rows/Frame:	Number of data rows = N + 1, N = 0 to 63 (D7 = LSB)
Last Data Row:	N = Address of last displayed data row, N = 0 to 63, i.e.; for 24 data rows, program N = 23. (D7 = LSB)
Mode:	Register, 1, D0 = 1 establishes Interlace.
Scans/Data Row:	Interlace Mode TMS9927: Scans per data row = N + 1 where N = programmed number of data rows. N = 0 to 15. Scans per data row must be even counts only TMS9937: Scans per data row = N + 2. N = 0 to 14, odd or even counts Non-Interlace Mode TMS9927/TMS9937: Scans per data row = N + 1, odd or even count. N = 0 to 15.

2.4.2 Register 4

All eight bits of Register 4 (R4) are used to indicate the total number of raster scans per frame. In interlaced model the total scans per frame is twice the contents of R4, plus 513. For example, if 525 scans are desired, R4 should contain 6→ (2 x 6 + 513 = 525), and vertical sync will occur exactly every 262.5 scans. In interlaced mode, only odd counts are permitted between 513 and 1023.

To program the total number of scans per frame using the non-interlaced mode, the contents of R4 are multiplied by 2 and added to 256. Therefore, if 262 scans per frame are required in the non-interlaced mode, R4 should be programmed as 3→ (2 x 3 + 256 = 262). Only even counts are permitted for non-interlaced modes between 256 and 766. In both modes, vertical sync width is equal to three horizontal scans.

2.4.3 Register 5

Control Register 5 (R5) contains the vertical-data-start indicator. This is the 8-bit number of raster scans delay, after the start of vertical sync to valid video data. The delay permits vertical retrace and signals the TMS9927/TMS9937 the number of raster scans after the start of vertical sync to display data.

2.4.4 Register 6

Register 6 (R6) uses six bits (2-7) to store the address of the last displayed data row minus one. The two most-significant bits are not used. If R3 is programmed for 32 data rows, and if it is desired to have line 13 as the bottom line, then R6 should be programmed with 13 - 1 = 12. In this example, line 14 would be the top line and line 1 and 32 would be contiguous near the middle of the screen.

NOTE

Character counter outputs (H lines) are active during blanking and vertical retrace.

2.4.5 Timing Example

Timing considerations must comprehend the particular monitor to be controlled. For the purposes of this discussion, the following timing constraints are assumed: 63.5 microseconds per horizontal scan and 60 frames per second, non-interlaced, 262 scans per frame.

A total of 63.5 microseconds per horizontal scan elapse from the beginning of one horizontal raster scan to the beginning of the next, including horizontal retrace. If a display of 32 characters per data row is desired, 40 total characters per data row must be used to calculate timing. At this character width eight character times are needed for horizontal sync and retrace. Assuming that each character block is eight dots wide, a character block shown in Figure 4, consists of the display matrix plus the spacing between characters. The dot frequency of the assumed system is:

5.04 MHz = 15,750 Hz x (32 + 8) char/line x 8 dots/char
(63.5 μsec/scan = 15750 Hz)

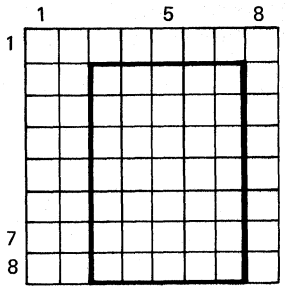


FIGURE 4 – TMS4710 CHARACTER GENERATOR 5 X 7 EMBEDDED DISPLAY BLOCK

Since approximate bandwidth equals dot frequency divided by two, the bandwidth needed by this system is 2.52 MHz. The designer must ensure the particular monitor can handle this bandwidth. Since a standard TV monitor has a bandwidth of 4.5 MHz, it could satisfactorily accept the 2.52-MHz worst-case video signal computed above. Therefore, a user could use a home TV to implement this application.

The video screen is completely refreshed 60 times per second in the noninterlaced format. A total of 262 scans per frame are made of which 240 scans display video data and 22 scans are used for high vertical sync and retrace. If the design dictates 20 data rows per frame, each data row is 12 scans high.

2.5 SELF-LOAD

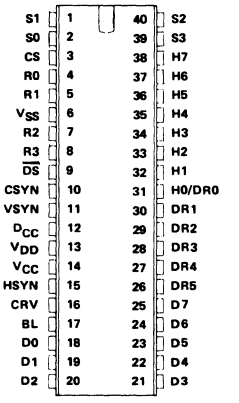
The TMS9927/TMS9937 features two self-load operations: processor and nonprocessor. The command on the select lines for processor self-load is 0111 and for nonprocessor self-load is 1111. The nonprocessor SELF-LOAD command must be applied on the select line long enough to ensure that self-load is completed. SELF-LOAD is initiated when DS is strobed.

Issuing a nonprocessor SELF-LOAD command causes a self-load and, upon removal of the all ONEs state from the select lines (independent of DS), the timing chain will begin. A processor SELF-LOAD command only causes the TMS9927/TMS9937 to load its registers. A START command then is needed to start the timing chain.

During self-load, VTC-produced control register commands load the appropriate registers (see Table 2). Therefore, if cursor row and character position registers require resetting via self-load, the PROM words for addresses 1100 and 1101 should be programmed as all ZEROs.

2.6 TMS9927/TMS9937 TERMINAL ASSIGNMENTS

SIGNATURE	PIN	I/O	DESCRIPTION
D0 (MSB)	18	I/O	D0 through D7 constitute the data bus. The data serves as input for control register contents to VTC and output for cursor address read data. See note below.
D1	19	I/O	
D2	20	I/O	
D3	21	I/O	
D4	22	I/O	
D5	23	I/O	
D6	24	I/O	
D7 (LSB)	25	I/O	
S0 (MSB)	2	I	S0 through S3 are the select lines, used to select the control register to be loaded or other control function. See note below.
S1	1	I	
S2	40	I	
S3 (LSB)	39	I	
			POWER SUPPLIES
V_{CC}	14		Supply voltage (5 V NOM)
V_{DD}	13		Supply voltage (12 V NOM)
V_{SS}	6		Ground reference
CS	3	I	Chip select alerts TMS9927/TMS9937 that it is being addressed.
$\overline{DS}$	9	I	Data strobe strobes data from D0-D7 into the register pointed to by S lines or out of cursor control registers (LOW active).
HSYN	15	O	Horizontal sync goes active (HIGH) to indicate horizontal retrace.
VSYN	11	O	Vertical sync goes active (HIGH) to indicate vertical retrace.
CSYN	10	O	Composite sync provides a RS-170, composite sync waveform, active only in noninterlaced mode and is of the same width as HSYN.
BL	17	O	Blanking, when active (HIGH), defines nonactive portion of horizontal and vertical scans.
DR1	30	O	Data row counter outputs to the refresh memory indicate which data row is being displayed. See note below.
DR2	29	O	
DR3	28	O	
DR4	27	O	
DR5 (LSB)	26	O	
H0/DR0	31	O	Output is MSB of character counter if MSB of character per data row is a ONE; otherwise, output is MSB of data row counter.
H1	32	O	Character counter outputs to the refresh memory indicate which character in the data row is being displayed.
H2	33	O	See note below.
H3	34	O	
H4	35	O	
H5	36	O	
H6	37	O	
H7 (LSB)	38	O	
R0 (MSB)	4	O	Scan counter outputs to character generator indicate which scan lines of character, are to be output. In interlaced mode, R3 defines which field is being displayed, odd or even. See note below.
R1	5	O	
R2	7	O	
R3	8	O	
DCC	12	I	Dot counter carry, carry from off-device character dot counter, establishes basic character clock rate.
CRV	16	O	Cursor video, when active (HIGH), defines cursor location.



NOTE: The terminal assignments for the TMS9927/TMS9937 follow Texas Instruments convention of bit 0 being the most significant bit.

3. APPLICATIONS

3.1 TMS9900-BASED SYSTEM

- 16 rows of 64 characters
- Noninterlaced format
- 5 x 7 display matrix embedded in an 8 x 12 field
- 63.5 microseconds per horizontal sweep
- Vertical refresh 60 times per second
- Monitor has 262 scans per frame.

Figure 5 is a block diagram of a TMS9900-based application for the VTC used as a memory-mapped device. The TMS9900 controls VTC functions but is not necessarily dedicated to that purpose. The dual-port memory can be any system, which allows both CPU and VTC access to it. The reset circuit shown in the block diagram provides both the necessary power-up reset and a pushbutton reset option. Three subsystems may be defined in the block diagram: TMS9900, memory, and video.

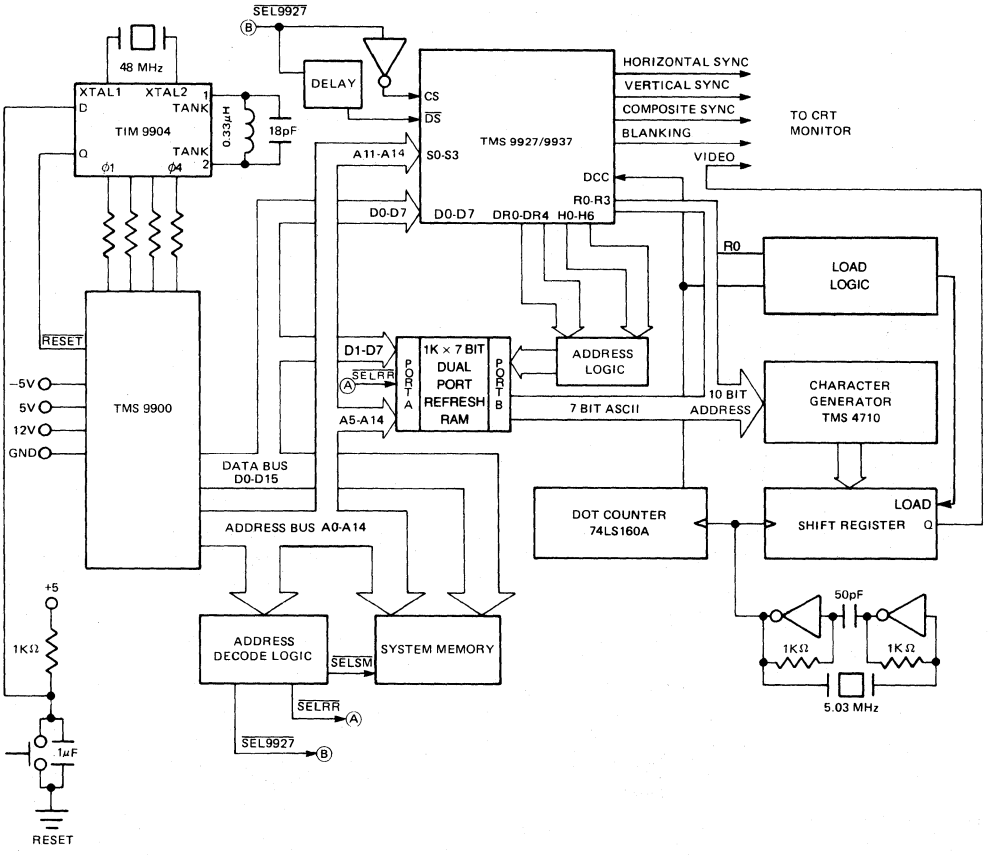


FIGURE 5 — TMS9900 BASED APPLICATION FOR TMS9927/TMS9937

The TMS9900 portion of the 9900-based performs any function requiring an interface to a CRT monitor. The components of the 9900 subsystem include a TMS9900, a TMS9904, system memory, and reset circuitry. The TMS9900 subsystem, shown in the block diagram, is the minimum system necessary to interface the TMS9927/TMS9937.

The memory subsystem consists of four elements: an address decoder and three memory elements system memory, dual-port refresh RAM, and TMS9927/TMS9937, each of which is selected by the address decoder. The system memory is that portion of memory that the TMS9900 uses to store its instructions and data. The refresh RAM stores the ASCII characters the system uses to drive the display. The TMS9927/TMS9937 is used as a memory-mapped I/O device.

The 7-bit ASCII code output from the refresh RAM is combined with the least significant three bits of the scan counter outputs to generate a 10-bit address to the TMS4710 character generator. The TMS9927/TMS9937 occupies 16 eight-bit words in the system memory space. Since the VTC has an 8-bit bus and the TMS9900 has a 16-bit bus, the eight most-significant bits of the TMS9900 data bus are connected to the TMS9927/TMS9937.

The video output subsystem comprises a dot clock, a dot counter (74LS160A), a shift register (74LS166), and a TMS4710 character generator. The dot clock, which oscillates at the video dot frequency, clocks the shift register, sending out video to the Z input of the CRT. The dot clock also increments the dot counter, which counts dots until the number of horizontal dots in a character have been output. Then the counter notifies the VTC, via the dot counter carry (DCC) line, that a character has been output. Upon receipt of a pulse on the DCC line, the TMS9927/TMS9937 updates the character counter outputs (H lines), scan counter outputs (R lines), and data row counter outputs (DR lines).

Since there are 13 lines of character select from the TMS9927/TMS9937, some address derivation logic may be needed to combine the 13 lines with the correct number of address lines for the particular refresh memory. The output of the refresh RAM is a 7-bit ASCII character. The ASCII code and the scan counter outputs (R lines) are combined to generate an address for the TMS4710 character generator. The TMS4710 generates an 8 x 8 character block with an embedded 5 x 7 display dot matrix. The eight bits from the TMS4710 are sent to the shift register to be shifted out at the video dot frequency by the dot clock.

3.1.1 Design Particulars

The typical application described below is a display with 16 rows of 64 characters each, and the CRT monitor is a standard monitor (noninterlaced mode). This standard monitor has 262 total scans per frame, of which 22 are used for vertical sync and retrace, leaving 240 scans to display information. Since there are 16 data rows per frame and each row consists of 12 scans, there will be 48 unused scans. Of these 12 scans per row, seven are used to display information, and five scans are used for vertical spacing.

In the horizontal direction 64 characters per row are specified at a fixed horizontal scan time of 63.5 microseconds per scan. The time needed to effect horizontal sync and retrace for a CRT monitor can be calculated by multiplying 63.5 microseconds by 0.18, (18 percent of horizontal sweep time is for retrace) obtaining 11.43 microseconds. Since 11.43 microseconds for retrace, plus the number of display characters, times the time per character should yield 63.5 microseconds, solve for the time per character as follows:

$$\text{time/char} = \frac{63.5\ \mu\text{sec} - 11.43\ \mu\text{sec}}{64\ \text{char}} = \frac{0.814\ \mu\text{sec}}{\text{char}}$$

Next calculate the number of characters times for horizontal sync and retrace. Divide 11.43 microseconds by 0.814 microseconds/char, and round to the next highest integer, obtaining 15 character times for back porch, horizontal sync and horizontal retrace. Thus, there are 79 total characters per data row. A 63.5 microseconds per row scan time equals a scan frequency of 15,750 hertz. Multiply the scan frequency by the total number of characters to find character frequency, and multiply character frequency by dots-per-character to obtain dot frequency:

dot frequency = 15,750 hertz x (64 + 15) char/row x 8 dots/char = 9.954 megahertz

To calculate the bandwidth the monitor must handle, divide the dot frequency by two. In this typical system the monitor must accept a bandwidth of 4.977 megahertz.

In the vertical direction 12 scans per character are needed; this includes seven scans for display information and five scans for spacing. There are 16 data rows, each consisting of 12 scans, giving a total of 192 scans. The standard monitor used in this example has 262 total scans per frame, of which 240 are used for displayable data and 22 for vertical sync and retrace. Only 192 scans of the 240 displayable scans are used, leaving 48 scans. The 48 scans are compensated by using control register 5, vertical data start. The vertical data start register is used to vertically center the data rows.

The screen display size is 16 rows of 64 characters each, which totals 1024 displayed characters. The minimum size of the refresh memory is 1024 words of seven bits each. Depending on the refresh memory architecture and component speeds, pipelining of memory may be necessary to achieve system speed.

The six least-significant bits of the character counter outputs (H lines) can be connected to the least the least-significant bits of the refresh memory address lines. Six bits can uniquely address all 64 characters of the data line. If there were 72 characters per data row, seven bits would be needed to represent this, but 56 of the 128 possible combinations would not be used, thus requiring some address compression logic. The four least significant bits of the data row counter outputs (DR lines) are then tied to the most-significant bit inputs of its refresh memory. Four bits can uniquely address the 16 data rows. This is possible without any address modification since 16 is an exact integral power of two.

The three least-significant bits of the scan counter outputs (R1-R3) are connected to the least significant address bit inputs of the TMS4710 character generator. The seven bits of ASCII code from the refresh memory are then connected to the most-significant bits of the address inputs of the TMS4710. Since three bits of the scan counter are used, only eight scan lines per character can be addressed, which is all the TMS4710 stores. In order to blank the last four of the 12 scan rows for vertical spacing, some circuitry is needed to ensure that the shift register is not loaded with data from the TMS4710 so that its output is blank for these scans.

The dot counter (74LS160A) is clocked at the video dot frequency. When it counts eight (the number of dots per character), it generates the carry that is used as the input to the TMS9927 dot counter carry (DCC).

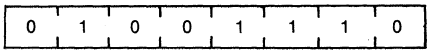
3.1.2 Power Up

Upon power-up the TMS9900 must initialize the video interface. The first logical step in this process is to ensure that the refresh RAM is clear. Next, the control registers should be loaded. A typical TMS9900 instruction sequence to accomplish this function is listed below (Table 7) and flowchart in Figure 6.

TABLE 7 — TYPICAL TMS9900 INSTRUCTION SEQUENCE

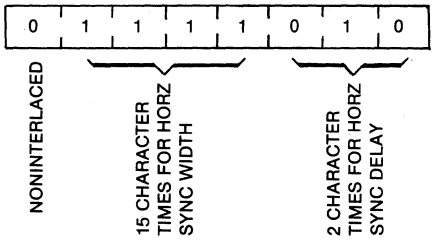
```
        LI      R7,    FD14     SET POINTER TO VTC RESET
        CLR     *R7             RESET VTC
        LI      R7,    FD00     SET POINTER TO START ADDRESS OF VTC IN MEMORY
        LI      R8, TABLE       SET POINTER TO VALUES FOR VTC CONTROL REGISTERS
LOOP    MOV     *R8 +, *R7 +    SEND EIGHT-BIT CONTROL WORD TO TMS9927
        CI      R7,    FD0E     HAVE 7 CONTROL WORDS BEEN SENT?
        JL      LOOP
        AL      R7, 10          SET ADDRESS TO PERFORM CURSOR LOAD
        CLR     *R7+            CURSOR CHARACTER ADDRESS SET TO ZERO
        CLR     *R7+            CURSOR ROW ADDRESS SET TO ZERO
        CLR     *R7             START TMS9927/TMS9937 TIMING CHAIN
          •       •
          •       •
          •       •
          •       •
TABLE   EQU     $
R0      DATA      4E00
R1      DATA      7A00
R2      DATA      5B00
R3      DATA      4F00
R4      DATA      0300
R5      DATA      4600
R6      DATA      0F00
```

3.1.2.1 Register 0

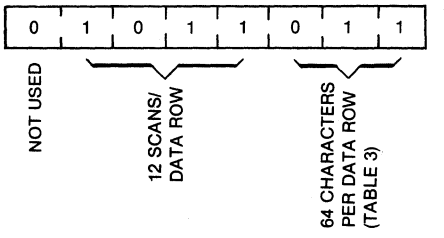


Horizontal Character Count = $4E_{16}$ = 78 + 1 = 79

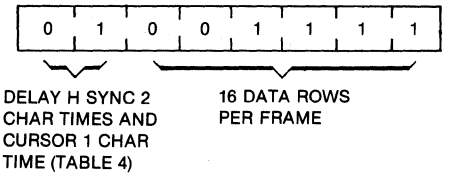
3.1.2.2 Register 1



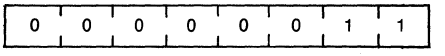
3.1.2.3 Register 2



3.1.2.4 Register 3

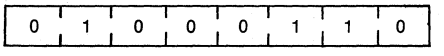


3.1.2.5 Register 4



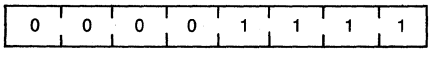
(2*3) + 256 = 262 scans per frame (noninterlaced)

3.1.2.6 Register 5



46_{16} = 70_{10} scans after VSYN and before valid for vertical data start

3.1.2.7 Register 6



16 is last displayed data row

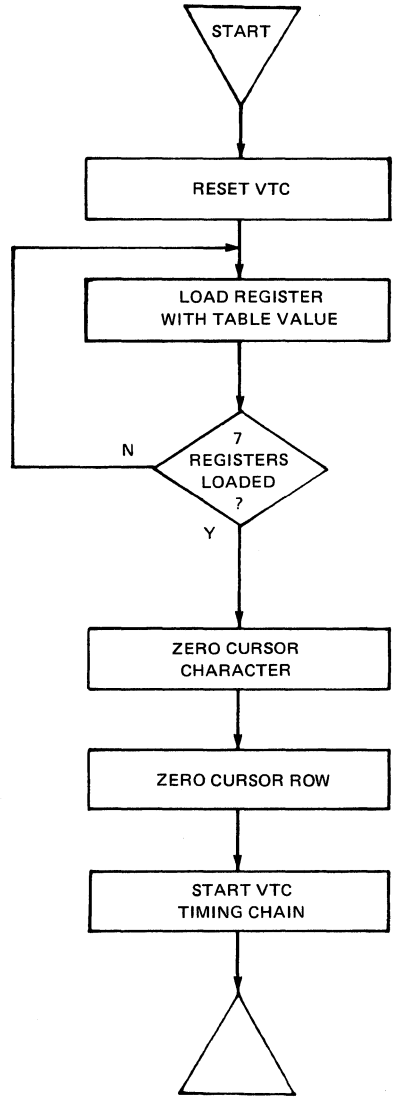


FIGURE 6 — POWER-UP FLOWCHART

The TMS9927/TMS9937-controlled display is now running and outputting a blank screen. The cursor is visible in the upper left-hand corner of the screen (external circuitry uses the cursor video (CRV) output of the TMS9927/TMS9937 to generate the cursor). Anything placed in the refresh RAM now will be displayed automatically. The TMS9900 may place a character in the refresh memory of this system simply as follows:

```
MOV CHAR, *R4+  MOVE DATA AT CHAR TO REFRESH RAM
```

Note that R4 must contain the pointer into refresh RAM to signify where the character is supposed to go. The five least-significant bits of R4 contain the character row address and the next six bits contain the row number. As described in a previous section, an address derivation scheme to the refresh RAM might be required. And, as each character is added to the refresh memory, it will be desirable to update the cursor position by issuing the cursor load commands.

3.1.3 Scrolling

Scrolling is easily implemented in this system. When the scroll command is issued, the top data row displayed is moved to the bottom data row, the remainder of the screen is moved up one line, thus producing a wrap-around scheme. Therefore, to implement a scroll up, a scroll command is issued and the new bottom line data should be cleared by software or overwritten by new data. Multiple scrolling is accomplished by reloading Register 6 or by multiple iterations of the scroll command.

3.2 TMS9940-BASED SYSTEM

3.2.1 GENERAL

A typical TMS9940 application using the TMS9927/TMS9937 to function as an intelligent terminal is diagrammed in Figure 7. This system comprises three subsystems: keyboard interface, TMS9927/TMS9937 interface, and a video generation section. In this application the TMS9940 is dedicated to controlling the CRT monitor.

The keyboard interface enables the user to communicate character and control information to the CPU. The interface consists of a keyboard, ASCII converter, and I/O lines to the TMS9940. Many special function keys on the keyboard may be defined in the TMS9940 software, and the ASCII converter also may be implemented in TMS9940 software.

The CPU communicates with and controls the VTC through the TMS9927/TMS9937 interface. This interface consists of the select lines, the self-load PROM, and the dual-port refresh RAM. The select lines control the TMS9927/TMS9937 by issuing SELF-LOAD and CURSOR ADDRESS UPDATE commands.

The two cursor address registers can be read by first issuing a READ CURSOR LINE ADDRESS command and sampling the eight I/O ports, which are used as the data bus. Next, the READ CURSOR CHARACTER ADDRESS is issued, and again the data bus is sampled. Before the data bus is read, the I/O line connected to DS must be set LOW. The cursor address register is programmed similarly except the DS I/O lines are not set LOW until valid data is output on the data bus I/O lines.

The 74S288 is a 32-word by 8-bit PROM, which contains the control words for the TMS9927/TMS9937 control register. When the SELF-LOAD command from the CPU is received, the VTC scan counter outputs (R lines) either send addresses to the PROM or send data for PROM control registers. If the CPU issues a NONPROCESSOR SELF-LOAD command, it must be accompanied by a START command; otherwise, no START command is needed with a SELF-LOAD.

The dual-port refresh RAM is identical to that described in Section 3.1.

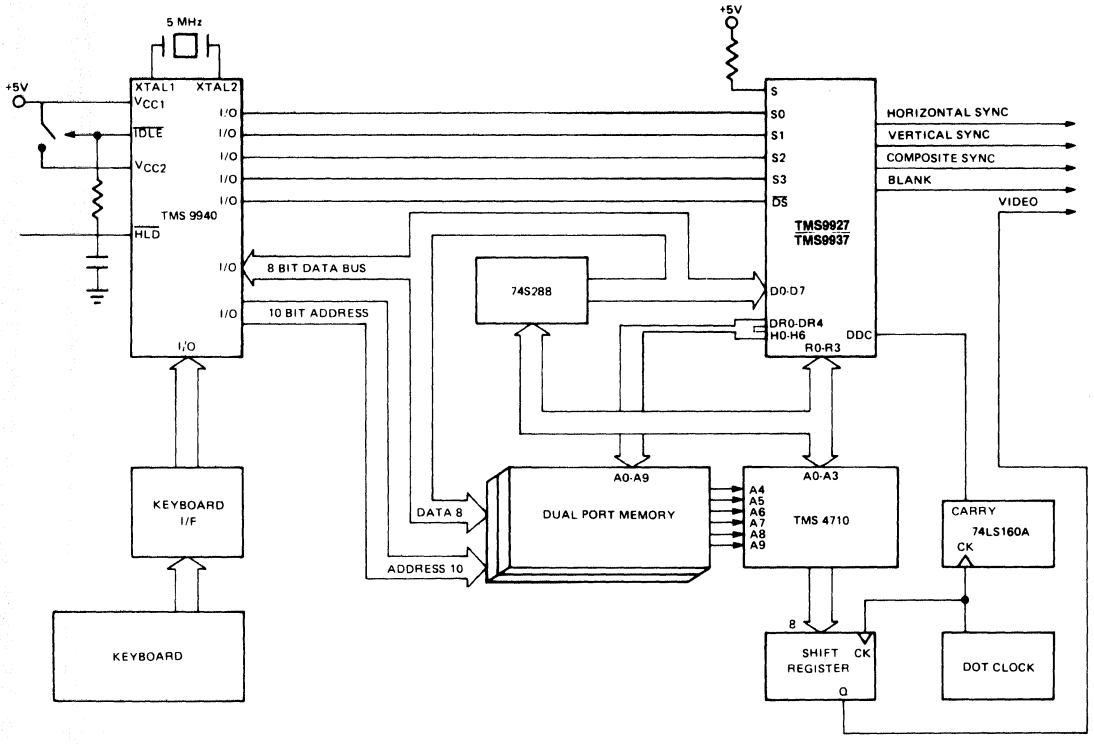


FIGURE 7—TMS9940 APPLICATION WITH TMS9927/TMS9937 USING SELF-LOAD FEATURE

3.3 START-UP, TMS9927

When employing microprocessor-controlled loading of the TMS9927 registers, the following sequence of instructions is necessary:

ADDRESS				COMMAND
1	1	1	0	Start Timing Chain
1	0	1	0	Reset
0	0	0	0	Load Register 0
	•			•
	•			•
	•			•
0	1	1	0	Load Register 6
1	1	1	0	Start Timing Chain

The sequence of START, RESET, LOAD, START ensures proper initialization of the registers; however, this sequence is not required if register loading is accomplished by either of the Self-Load modes. This sequence is optional with the TMS9937.

3.4 RESTRICTIONS

1. Only one pin is available for strobing data into the device via the data bus. The cursor X and Y coordinates are therefore loaded into the chip by presenting one set of addresses and outputted by presenting a different set of addresses. Therefore the standard WRITE and READ control signals from most microprocessors must be "NORed" externally to present a single strobe (DS) signal to the device.
2. In interlaced mode the total number of character slots assigned to the horizontal scan must be even to insure that vertical sync occurs precisely between horizontal sync pulses.

4. TMS9927/TMS9937 ELECTRICAL AND MECHANICAL SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATING OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.3 V to 10 V
Supply voltage, V_{DD} . . . . . −0.3 V to 18V
All inputs and outputs voltage . . . . . −0.3 V to 18 V
Continuous power dissipation . . . . . 1.25 W
Free-air operating temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE: Voltage values are with respect to V_{SS}.

4.2 RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Ground reference, V_{SS}		0		V
High-level input voltage, V_{IH}	$V_{CC}-1.5$		V_{CC}	V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

4.3 ELECTRICAL CHARACTERISTICS

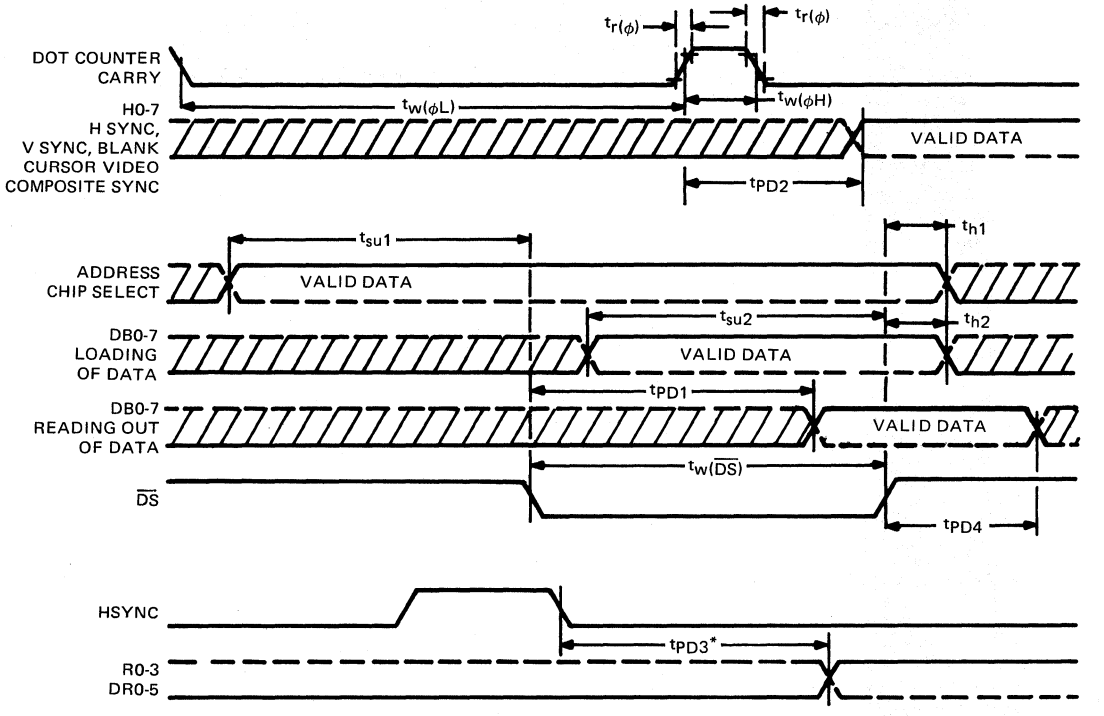
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	R0-R3, D0-D7 (I_{OH} = 80μA)	2.4			V
		All others (I_{OH} = 40 μA)	2.4			
V_{OL}	Low-level output voltage	R0-R3 (I_{OL} = 3.2 mA)			0.4	V
		All others (I_{OL} = 1.6 mA)			0.4	
I_I	Input current	S0-S3, CS V_{IN} = 0.4			250	μA
		All others $0 \leq V_{IN} \leq V_{CC}$			10	
$I_{CC(av)}$	Average supply current from V_{CC}			80	100	mA
$I_{DD(av)}$	Average supply current from V_{DD}			40	70	mA
I_{DB}	Data bus leakage in input mode				10	μA
C_i	Input capacitance	Data bus		10	15	pF
		Clock, DS		25	40	
		All others		10	15	

4.4 TIMING REQUIREMENTS – TMS9927: T_A = 25°C; TMS 9937: T_A = 0°C to 70°C

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(\phi)}$	Dot counter cycle time	250		2000	ns
$t_{r(\phi)}$	Rise time		10	50	ns
$t_{f(\phi)}$	Fall time		10	50	ns
$t_{w(\phi L)}$	Width of low clock	215			ns
$t_{w(\phi H)}$	Width of high clock	35			ns
$t_{w(\overline{DS})}$	Width of DS low level	150		10,000	ns
t_{su1}	Setup time – address bus, chip select	125			ns
t_{su2}	Setup time – data bus	125			ns
t_{h1}	Hold time – address bus, chip select	50			ns
t_{h2}	Hold time – data bus	75			ns

4.5 SWITCHING CHARACTERISTICS TMS9927: T_A = 25°C; TMS9937: T_A = 0°C to 70°C

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD1}	Propagation delay, DS to D0-D7 valid	C_L = 50 pF			125	ns
t_{PD2}	Propagation delay, Dot count carry to H0-H7, HS, VS, BL, CRV, COMP SYNC	C_L = 20 pF			125	ns
t_{PD3}	Propagation delay, HSYNC to R0-R3, DR0-DR5	C_L = 20 pF			500	ns
t_{PD4}	Propagation delay, DS to D0-D7 invalid	C_L = 50 pF	5		60	ns



R3-R0 and DR5-DR0 may change prior to the falling edge of HSYNC.

FIGURE 8 — TMS9927/TMS9937 VTC TIMING DIAGRAM *

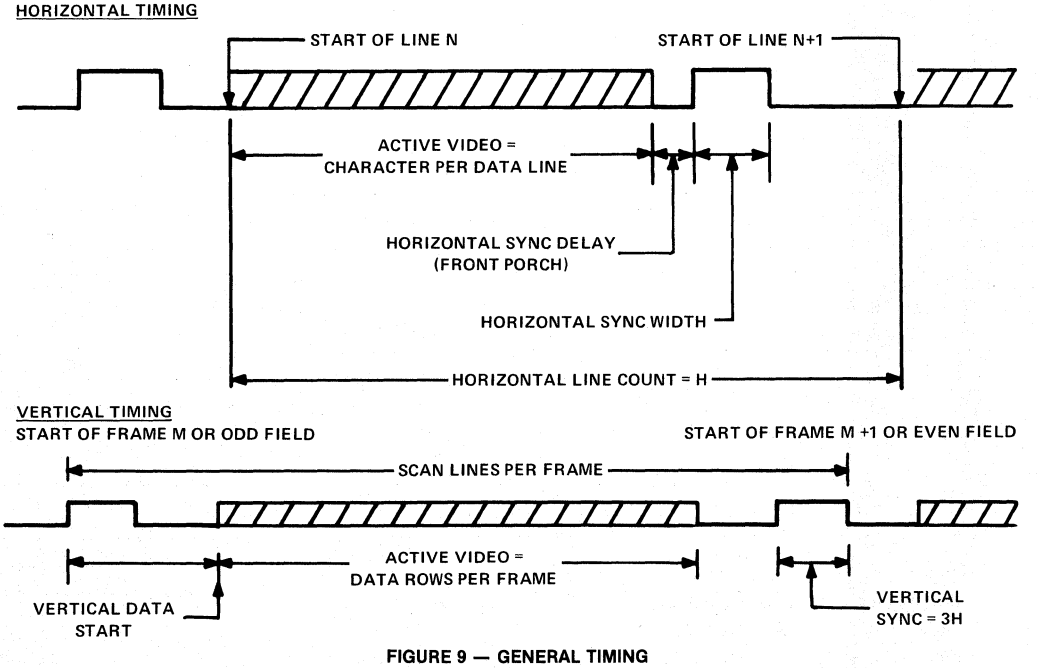


FIGURE 9 — GENERAL TIMING

* All switching times are assumed to be at 10% or 90% values.

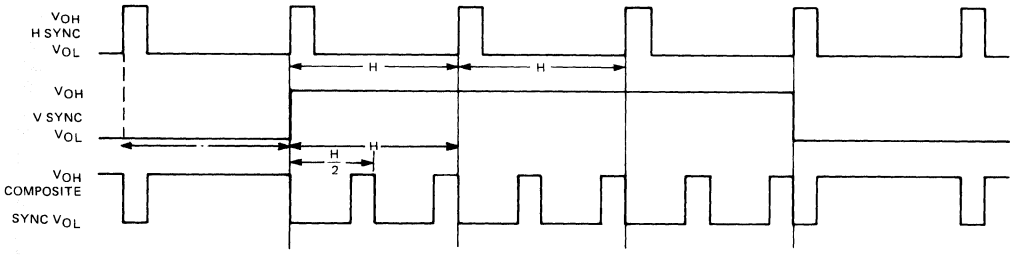
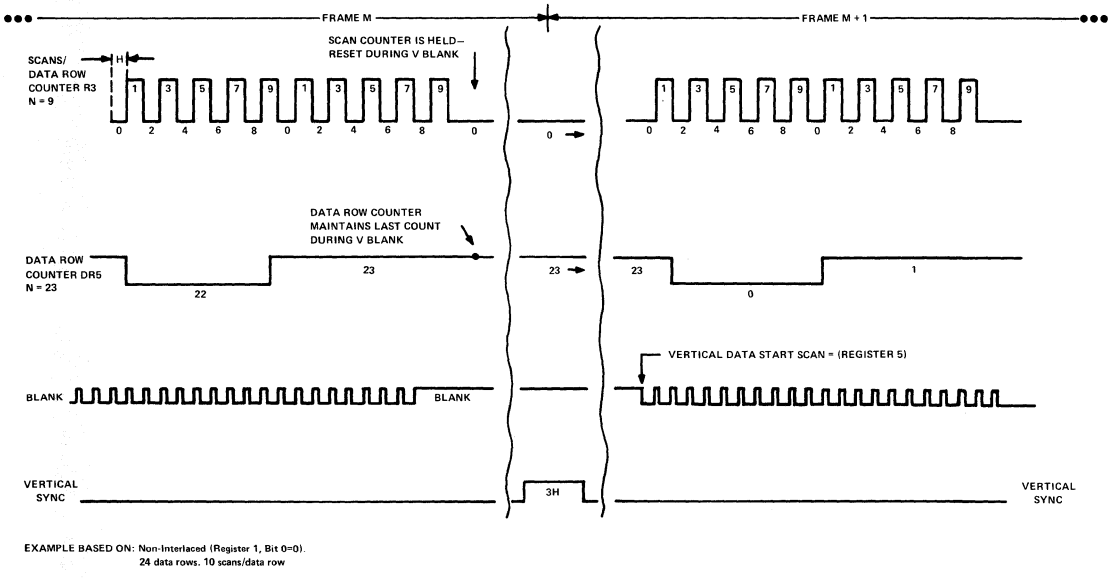


FIGURE 10 — COMPOSITE SYNC TIMING

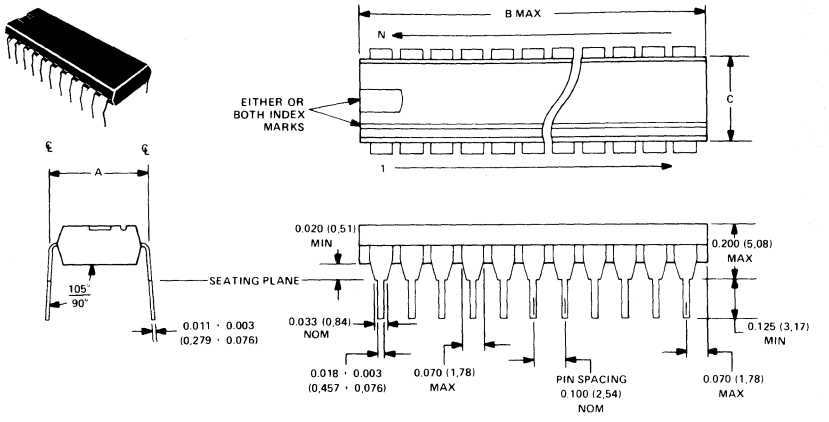


EXAMPLE BASED ON: Non-Interlaced (Register 1, Bit 0=0).
24 data rows, 10 scans/data row

FIGURE 11 — VERTICAL SYNC TIMING

5. MECHANICAL DATA

5.1 TMS9927/TMS9937 40-PIN PLASTIC PACKAGE

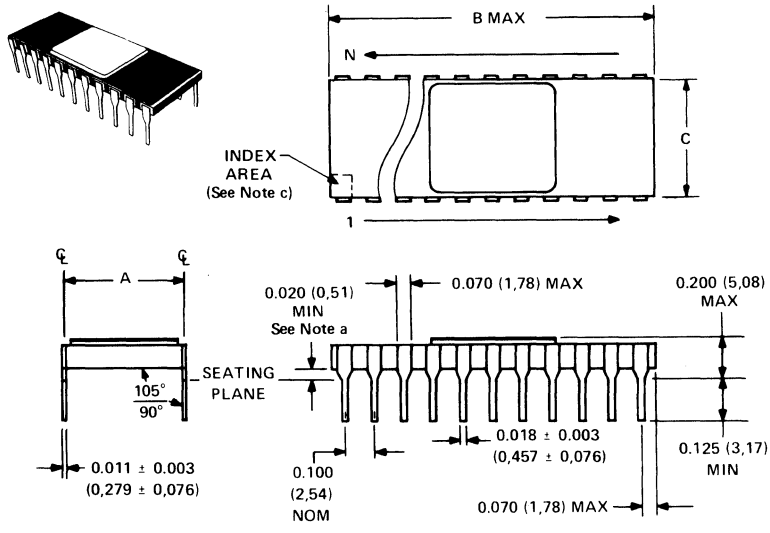


ALL LINEAR DIMENSIONS ARE IN INCHES AND PARENTHETICALLY IN MILLIMETERS. INCH DIMENSIONS GOVERN.

DIM \ PINS	8	16	18	20	22	24	28	40
A + 0.010 (0,26)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.400 (10,16)	0.600 (15,24)	0.600 (15,24)	0.600 (10,24)
B MAX	0.390 (9,9)	0.870 (22,1)	0.920 (23,4)	1.070 (27,2)	1.100 (28,0)	1.290 (32,8)	1.440 (36,6)	2.090 (53,1)
C NOM	0.250 (6,4)	0.250 (6,4)	0.250 (6,4)	0.265 (6,7)	0.350 (8,9)	0.550 (14,0)	0.550 (14,0)	0.550 (14,0)

5.2 TMS9927/TMS9937 40-PIN CERAMIC PACKAGE

Ceramic packages are provided with side-brazed leads and a metal, epoxy, or glass lid seal.



NOTES: a. This minimum spacing is valid for printed circuit board mounting with 0.033 (0,84) diameter holes for the leads.
b. All linear dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
c. The index is placed in this area to identify pin 1 and to provide other information as follows:

1 Pin 1 connected to chip-mounting pad.
△XX Pin XX connected to chip-mounting pad.
• No connection to chip-mounting pad.

Other symbols may indicate any combination of up to 4 pins connected to the chip-mounting pad.

DIM \ PINS	16	18	20	22	24	28	40
A ± 0.010 (0,26)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.400 (10,16)	0.600 (15,24)	0.600 (15,24)	0.600 (15,24)
B MAX	0.840 (21,4)	0.910 (23,1)	1.020 (25,9)	1.100 (28,0)	1.290 (32,8)	1.415 (36,0)	2.020 (51,3)
C NOM	0.290 (7,4)	0.290 (7,4)	0.290 (7,4)	0.390 (9,9)	0.590 (15,0)	0.590 (15,0)	0.590 (15,0)

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