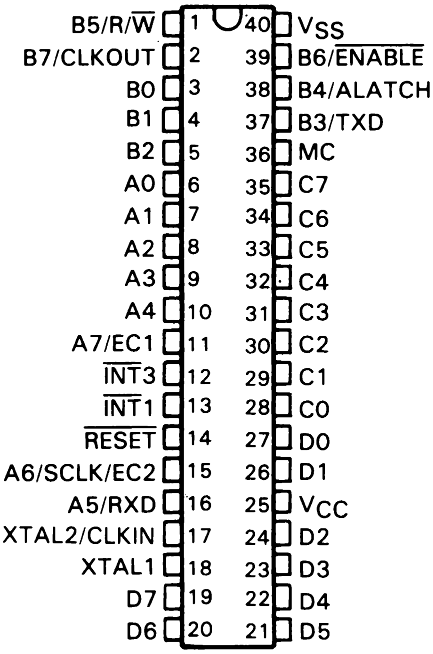
TMS7742JDL.EPP001 8-BIT EPROM MICROCOMPUTER

- TMS7000 Family Compatible
- 4K-Byte On-Chip EPROM
- EPROM Progamming Procedure Compatible with TMS2732A
- 256 Byte On-Chip RAM Register File
- 5 MHz Operating Frequency
- 32 TTL-Compatible I/O Pins:
  - —22 Bidirectional Pins
  - —8 Output Pins
  - —2 Input Pins
- Three 8-Bit Timers On-Chip:
  - —Two Timers with 5-Bit Prescale
  - —One Timer with a 2-Bit Prescale
  - —Internal Interrupt with Automatic Timer Reload
  - —Capture Latch
- On-Chip Serial Port:
  - —Asynchronous, Isosynchronous, and Serial Modes
  - —Two Multiprocessor Communication Formats
  - —Error Detection Flags
  - —Fully Software Programmable
  - —Internal or External Baud Rate Generator
  - —Separate Baud Rate Timer Usable as a Third Timer
- Memory-Mapped Ports for Easy Addressing
- Register-to-Register Architecture
- Eight Functional Addressing Formats Including:
  - —Register-to-Register Arithmetic
  - —Indirect Addressing
  - —Indexed and Indirect Branches and Calls

JD PACKAGE
(TOP VIEW)



- Flexible Interrupt Handling:
  - —Priority Servicing of Simultaneous Interrupts
  - —Software Calls through Interrupt Vectors
  - —Precise Timing of Interrupts through Capture Latch
  - —Software Monitoring of Interrupt Status
- Supports All TMS7000 Family Expansion Modes
- N-Channel Silicon Gate MOS
- 5-Volt Power Supply, ±5%

description

The TMS7742JDL.EPP001 is an EPROM version of the 8-bit TMS7042 microcomputer with a relaxed specification. It contains 4K bytes of on-chip EPROM and is completely software and pin compatible with the TMS7042. Other features include 256 bytes of on-chip RAM, a flexible serial port (UART), three timers, and the same advanced register-to-register architecture that allows direct register arithmetic and logical operations without requiring the use of an accumulator (e.g., ADD R24, R245).

Uses of this device include prototyping capabilities for the TMS7020, TMS7040, and TMS7042, a low volume alternative to masked ROM parts, and also for applications where program constraints are likely to change periodically.

serial port

The serial port of the TMS7742JDL.EPP001 supports three modes of operation which enable it to communicate with multiple devices using various communication protocol techniques. It is double buffered on both transmit and receive, contains extensive status flag logic that can be used to ensure data entegrity, and supports both the Intel and Motorola multiprocessor communications protocols. Also, Timer 3 can be used as an internal baud rate generator. A major enhancement to the serial port is the speed of operation. In the Isosynchronous or Serial I/O mode, the maximum baud rate is 625 kilobits, and in the Asynchronous mode the maximum baud rate is 78 kilobits.

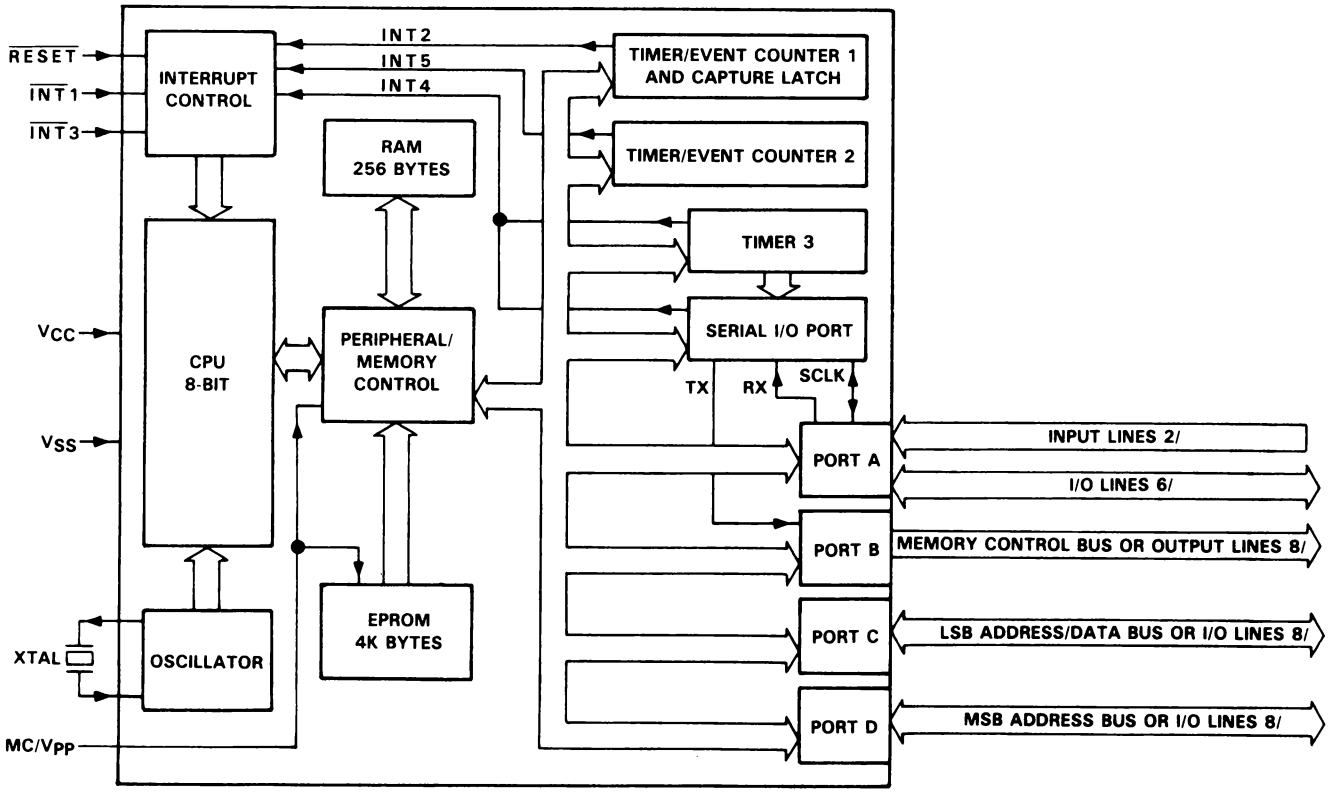
timers

The TMS7742JDL.EPP001 features three on-chip timers with individual start/stop control bits. Two of these are 8-bit timers with 5-bit programmable prescalers. These timers can be clocked by either the internal oscillator or an external source, and can be cascaded to form a 26-bit timer. Timer 3 is an 8-bit timer with a 2-bit programmable prescaler. This timer can function as a general purpose timer or a baud rate generator for the serial port. All timers are countdown timers with reload latches. They are automatically reloaded when they count past zero. There is also an 8-bit capture latch which automatically captures the value of Timer 1 when interrupt 3 occurs. This allows very accurate time measurements of external events.

interrupts

There are six prioritized interrupt levels on the TMS7742JDL.EPP001. Level 0 is the non-maskable reset, levels 1 and 3 are falling edge only external interrupts, level 2 is associated with Timer 1, level 4 is associated with the serial port (receive, transmit, and Timer 3), and level 5 is generated by Timer 2. All interrupts are routed through a user-defined vector to the appropriate service routine ; therefore, each service routine can be located anywhere in its address space. There is a global interrupt enable bit in the status register as well as individual interrupt enable bits for interrupts 1 through 5.

functional block diagram



TEXAS INSTRUMENTS

pin descriptions

OPERATION MODES				EPROM MODE			
PIN NAME	PIN NO.	I/O	DESCRIPTION	PIN NAME	PIN NO.	I/O	DESCRIPTION
A0	6	I/O	A0-A4 and A7 are general-purpose bidirectional pins.	A7	6	I	A3-A7 are address
A1	7	I/O	A5 and A6 are input-only data pins.	A6	7	I	lines.
A2	8	I/O		A5	8	I	
A3	9	I/O		A4	9	I	
A4	10	I/O		A3	10	I	
A5/RXD	16	I	Data input/Serial port receiver		16		
A6/SCLK/EC2	15	I/O	Data input/Serial port clock/Timer 2 event counter		15		
A7/EC1	11	I/O	Data I/O/Timer 1 event counter		11		
B0	3	O	B0-B3 are outputs. B4-B7 are outputs in Single-Chip		3		
B1	4	O	mode and memory interface pins in all other modes.		4		
B2	5	O			5		
B3/TXD	37	O	Data output/Serial port transmitter		37		
B4/ALATCH	38	O	Data output/Memory interface address latch strobe		38		
B5/R/$\overline{W}$	1	O	Data output/Memory interface Read-Write signal		1		
B6/$\overline{ENABLE}$	39	O	Data output/Memory interface enable strobe		39		
B7/CLKOUT	2	O	Data output/Internal clockout		2		
C0	28	I/O	Port C is a bidirectional data port. In Microprocessor	Q1	28	I/O	Q1-Q8 are
C1	29	I/O	mode, Port C is a multiplexed low address and data	Q2	29	I/O	bidirectional
C2	30	I/O	bus.	Q3	30	I/O	data lines.
C3	31	I/O		Q4	31	I/O	
C4	32	I/O		Q5	32	I/O	
C5	33	I/O		Q6	33	I/O	
C6	34	I/O		Q7	34	I/O	
C7	35	I/O		Q8	35	I/O	
D0	27	I/O	Port D is a bidirectional data port. In Microprocessor	A8	27	I	A0-A2 and A8-A10
D1	26	I/O	mode, it is the high address bus.	A9	26	I	are address lines.
D2	24	I/O		A11	24	I	
D3	23	I/O		A10	23	I	
D4	22	I/O		E	22	I	Chip Enable
D5	21	I/O		A0	21	I	
D6	20	I/O		A1	20	I	
D7	19	I/O		A2	19	I	
$\overline{INT1}$	13	I	Highest priority maskable interrupt		13		
$\overline{INT3}$	12	I	Lowest priority maskable interrupt		12		
$\overline{RESET}$	14	I	Reset	GND	14	I	V_{SS} for EPROM mode
MC	36	I	Mode control pin	$\overline{G}/V_{PP}$	36	I	Program enable (21 V to program, 0 V to verify)
XTAL2/CLKIN	17	I	Crystal input for control of internal oscillator	GND	17	I	V_{SS} for EPROM mode
XTAL1	18	O	Crystal output for control of internal oscillator		18		
V_{CC}	25		Supply voltage (5 V NMOS)	V_{CC}	25		Supply voltage (5 V)
V_{SS}	40		Ground reference	GND	40		Ground reference

mode control

All TMS7000 family members have four different operating modes allowing the optimization of the on-chip versus off-chip memory for each application. These modes are Single-Chip, Peripheral Expansion, Full Expansion, and Microprocessor modes. The tables below show the pin conditions that must be met for each mode, the number of I/O pins, and the amount of external address space available in each of the modes. To enter the EPROM mode, the $\overline{\text{RESET}}$ and XTAL2 pins must be held low.

MODE SELECT		OPERATION MODES				EPROM PROGRAMMING MODE	EPROM VERIFY MODE
		SINGLE CHIP	PERIPHERAL EXPANSION	FULL EXPANSION	MICRO-PROCESSOR		
I/O CONTROL REGISTER	BIT 7	0	0	1	X	X	X
	BIT 6	0	1	0	X	X	X
MODE CONTROL PIN		V_{SS}	V_{SS}	V_{SS}	V_{CC}	V_{PP}	V_{SS}
$\overline{\text{RESET}}$ PIN		V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{SS}	V_{SS}
XTAL2 PIN		N/A	N/A	N/A	N/A	V_{SS}	V_{SS}

X – Don't care
N/A – Not applicable

	SINGLE CHIP	PERIPHERAL EXPANSION	FULL EXPANSION	MICRO-PROCESSOR
I/O Pins:				
Bidirectional	22	14	6	6
Input only	2	2	2	2
Output only	8	4	4	4
Expansion Bus:				
Multiplexed Address/Data lines	0/0	8/8	16/8	16/8
Control lines	0	4	4	4
Memory Space (bytes):				
RAM	256	256	256	256
EPROM†	4096	4096	4096	0
Peripheral file	18	254	254	254
Memory expansion	0	0	60928	65024

†First six bytes of masked ROM devices are reserved for TI internal use.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 7 V
Supply voltage range, V_{PP} . . . . . −0.3 V to 22 V
Input voltage range . . . . . −0.3 V to 20 V
Output voltage range . . . . . −0.3 V to 7 V
Maximum buffer sink current . . . . . 10 mA
Continuous power dissipation . . . . . 2 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: All voltages are with respect to V_{SS}.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{PP}	Program supply voltage (see Note 3)		20.5	21	21.5	V
V_{IH}	High-level input voltage	CLKIN	2.6			V
		All others	2			
V_{IL}	Low-level input voltage	CLKIN			0.6	V
		All others			0.8	
T_A	Operating free-air temperature		0		70	°C

NOTES: 2. Ambient light may affect operational functionality and electrical characteristics. It is recommended to use an opaque label over the window when the EPROM is not being erased.
3. V_{PP} is applied to the MC pin in EPROM mode only.

electrical characteristics over full range of operating conditions (see Note 2)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current	A5, MC, $\overline{RESET}$, $\overline{INT1}$, $\overline{INT3}$, XTAL2	V_I = V_{SS} to V_{CC}		±2	±10	μA
		Ports C and D, A0-A4, A6, A7	V_I = 0.4 V to V_{CC}		±10	±100	
C_I	Input capacitance				2		pF
V_{OH}	High-level output voltage		I_O = −400 μA	2.4	2.8		V
V_{OL}	Low-level output voltage		I_O = 3.2 mA		0.2	0.4	V
$t_{r(O)}$	Output rise time‡		See Figure 1		9	50	ns
$t_{f(O)}$	Output fall time‡		See Figure 1		10	60	ns
I_{CC}	Supply current		All outputs open		180	250	mA
I_{PP}	Program supply current		$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{PP}			30	mA
$P_{D(av)}$	Average power dissipation		All outputs open		900	1313	mW

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Rise and fall times are measured between the maximum low level and the minimum high level using the 10% and 90% points (see Figure 2). Outputs have 100-pF loads to V_{SS}.

PARAMETER MEASUREMENT INFORMATION

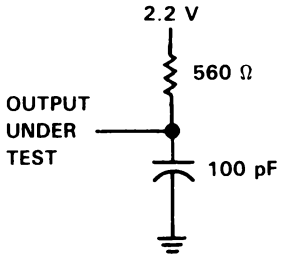


FIGURE 1. TYPICAL OUTPUT LOAD CIRCUIT

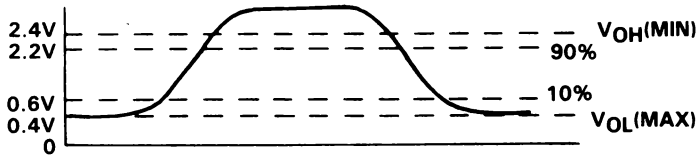


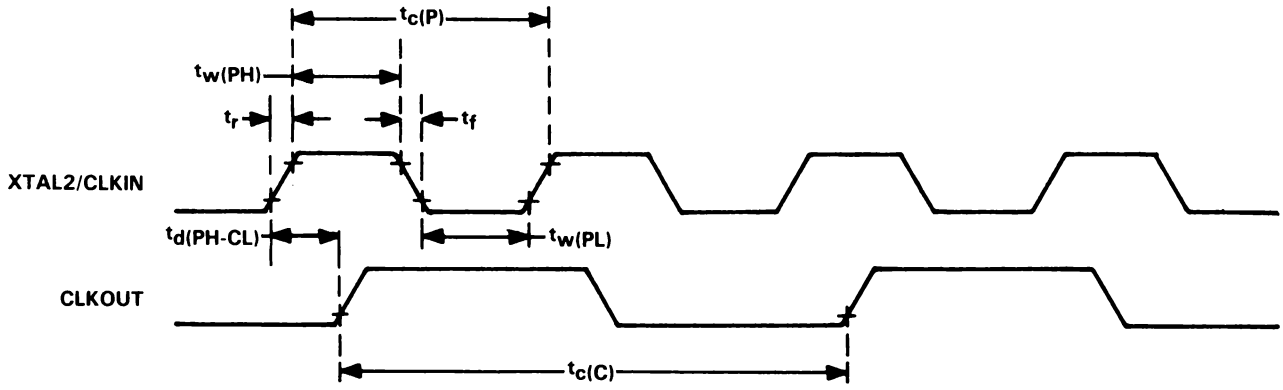
FIGURE 2. MEASUREMENTS POINTS FOR OUTPUT SWITCHING CHARACTERISTICS

recommended crystal operating conditions over full operating range

	PARAMETER	MIN	TYP	MAX	UNIT
f_{osc}	Crystal frequency	3		5	MHz
	CLKIN duty cycle		50		%
$t_{c(P)}$	Crystal cycle time	200		666	ns
$t_{c(C)}$	Internal state cycle time	400		1332	ns
$t_{w(PH)}$	CLKIN pulse duration high	90			ns
$t_{w(PL)}$	CLKIN pulse duration low	90			ns
t_r	CLKIN rise time (see Note 4)			30	ns
t_f	CLKIN fall time (see Note 4)			30	ns
$t_{d(PH-CL)}$	CLKIN rise to CLKOUT rise delay		120	200	ns

NOTE 4: Rise and fall times are measured between the maximum low level and the minimum high level.

clock timing



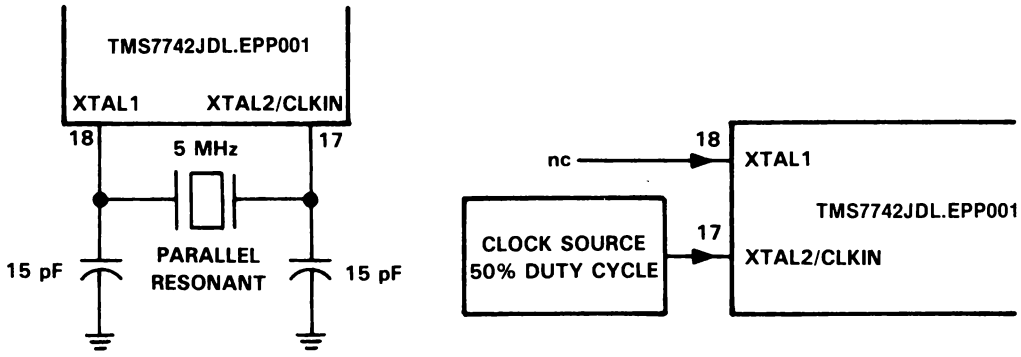


FIGURE 3. RECOMMENDED CLOCK CONNECTIONS

memory interface timings as a function of frequency

In the table below, $t_{c(C)} = 2/f_{osc}$. At 5 MHz $t_{c(C)}$ would be 400 ns. Minimum and maximum times may be calculated by using the formulas below with the appropriate clock period. Typical values for 5 MHz timing are shown on the next page.

	PARAMETER	MIN	MAX	UNIT
$t_{c(C)}$	CLKOUT cycle time (see Note 5)	400	1332	ns
$t_{w(CH)}$	CLKOUT high pulse duration	$0.5t_{c(C)} - 40$	$0.5t_{c(C)} + 10$	ns
$t_{w(CL)}$	CLKOUT low pulse duration	$0.5t_{c(C)} - 40$	$0.5t_{c(C)} + 15$	ns
$t_{d(CH-JL)}$	Delay time, CLKOUT rise to ALATCH fall	$0.5t_{c(C)} - 10$	$0.5t_{c(C)} + 30$	ns
$t_{w(JH)}$	ALATCH high pulse duration	$0.25t_{c(C)} - 15$	$0.25t_{c(C)} + 30$	ns
$t_{su(HA-JL)}$	Setup time, high address valid before ALATCH fall	$0.25t_{c(C)} - 40$	$0.25t_{c(C)} + 45$	ns
$t_{su(LA-JL)}$	Setup time, low address valid before ALATCH fall	$0.25t_{c(C)} - 45$	$0.25t_{c(C)} + 15$	ns
$t_{h(JL-LA)}$	Hold time, low address valid after ALATCH fall	$0.25t_{c(C)}$	$0.25t_{c(C)} + 45$	ns
$t_{su(RW-JL)}$	Setup time, R/$\overline{W}$ valid before ALATCH fall	$0.25t_{c(C)} - 35$	$0.25t_{c(C)} + 30$	ns
$t_{h(EH-RW)}$	Hold time, R/$\overline{W}$ valid after $\overline{ENABLE}$ rise	$0.5t_{c(C)} - 40$	$0.5t_{c(C)} + 15$	ns
$t_{h(EH-HA)}$	Hold time, high address valid after $\overline{ENABLE}$ rise	$0.5t_{c(C)} - 50$	$0.5t_{c(C)} + 35$	ns
$t_{su(Q-EH)}$	Setup time, data output valid before $\overline{ENABLE}$ rise	$0.5t_{c(C)} - 40$		ns
$t_{h(EH-Q)}$	Hold time, data output valid after $\overline{ENABLE}$ rise	$0.5t_{c(C)} - 45$		ns
$t_{d(LA-EL)}$	Delay time, low address high impedance to $\overline{ENABLE}$ fall	$0.25t_{c(C)} - 45$	$0.25t_{c(C)} + 15$	ns
$t_{d(EH-A)}$	Delay time, $\overline{ENABLE}$ rise to next address drive	$0.5t_{c(C)} - 25$	$0.5t_{c(C)} + 80$	ns
$t_{a(EL-D)}$	Access time, data input valid after $\overline{ENABLE}$ fall	$0.75t_{c(C)} - 135$		ns
$t_{a(A-D)}$	Access time, address valid to data input valid	$1.5t_{c(C)} - 160$		ns
$t_{d(A-EH)}$	Delay time, address valid to $\overline{ENABLE}$ rise	$1.5t_{c(C)} - 80$	$1.5t_{c(C)} + 30$	ns
$t_{h(EH-D)}$	Hold time, data input valid after $\overline{ENABLE}$ rise	0		ns
$t_{d(EH-JH)}$	Delay time, $\overline{ENABLE}$ rise to ALATCH rise	$0.5t_{c(C)} - 25$	$0.5t_{c(C)} + 25$	ns
$t_{d(CH-EL)}$	Delay time, CLKOUT rise to $\overline{ENABLE}$ fall	−10	35	ns

NOTE 5: $t_{c(C)}$ is defined to be $2/f_{osc}$ and may be referred to as a machine state or simply a state.

As an example, consider calculating the minimum data out hold time from $\overline{ENABLE}$ rising [$t_{h(EH-Q)}$].

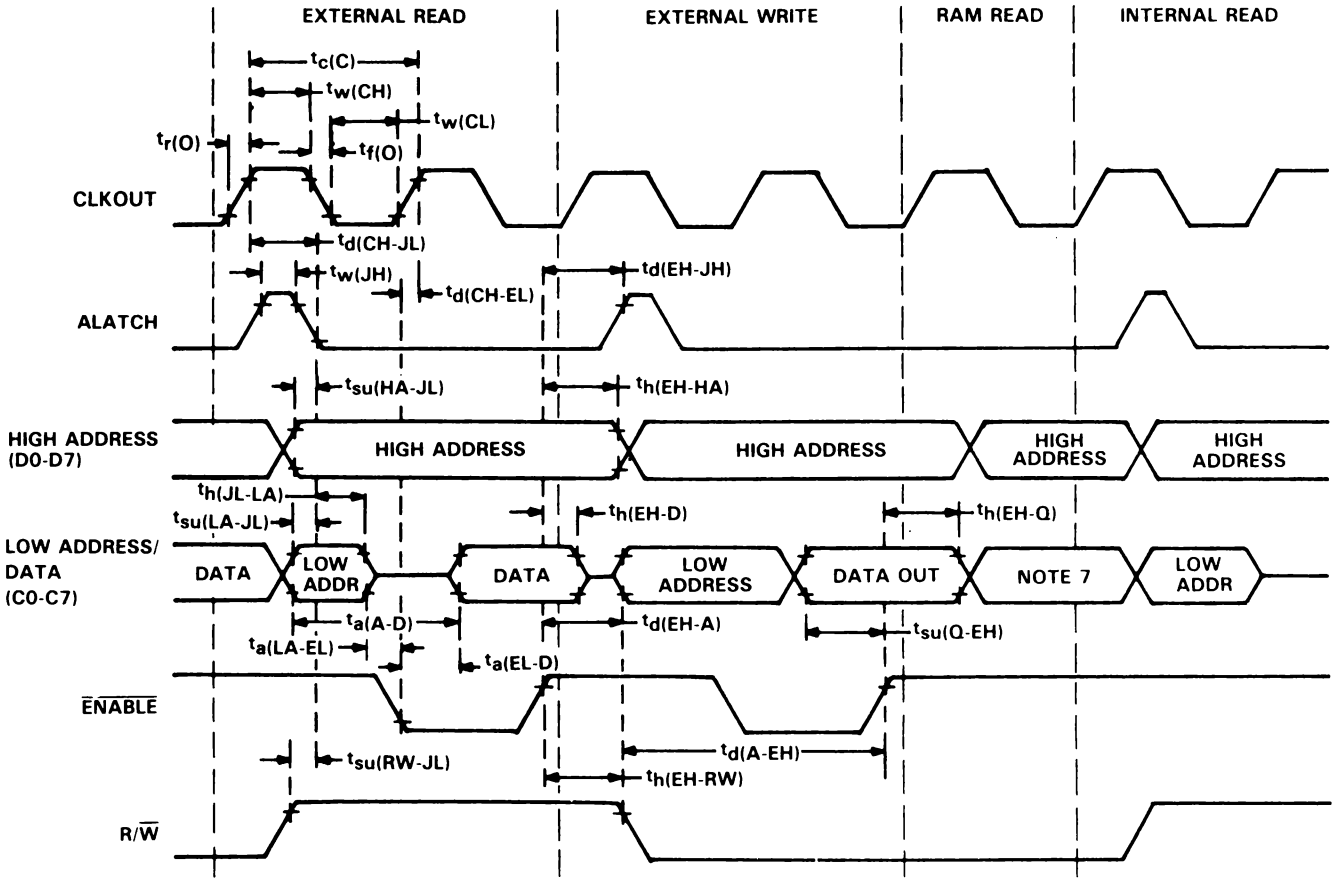
$$t_{h(EH-Q)} = 0.5t_{c(C)} - 45 \text{ ns}$$
$$= 0.5(400 \text{ ns}) - 45 \text{ ns}$$
$$= 200 \text{ ns} - 45 \text{ ns}$$
$$\therefore t_{h(EH-Q)} = 155 \text{ ns}$$

memory interface timing at 5 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{c(C)}$	CLKOUT cycle time (see Note 6)	f = 5 MHz, duty cycle = 50%		400		ns
$t_{w(CH)}$	CLKOUT high pulse duration		160	180	210	ns
$t_{w(CL)}$	CLKOUT low pulse duration		160	205	215	ns
$t_{d(CH-JL)}$	Delay time, CLKOUT rise to ALATCH fall		190	200	230	ns
$t_{w(JH)}$	ALATCH high pulse duration		85	110	130	ns
$t_{su(HA-JL)}$	Setup time, high address valid before ALATCH fall		60	85	145	ns
$t_{su(LA-JL)}$	Setup time, low address valid before ALATCH fall		55	80	115	ns
$t_{h(JL-LA)}$	Hold time, low address valid after ALATCH fall		100	120	145	ns
$t_{su(RW-JL)}$	Setup time, R/$\overline{W}$ valid before ALATCH fall		65	90	130	ns
$t_{h(EH-RW)}$	Hold time, R/$\overline{W}$ valid after $\overline{ENABLE}$ rise		160	200	215	ns
$t_{h(EH-HA)}$	Hold time, high address valid after $\overline{ENABLE}$ rise		150	205	235	ns
$t_{su(Q-EH)}$	Setup time, data output valid before $\overline{ENABLE}$ rise		160	320		ns
$t_{h(EH-Q)}$	Hold time, data output valid after $\overline{ENABLE}$ rise		155			ns
$t_{d(LA-EL)}$	Delay time, low address high impedance to $\overline{ENABLE}$ fall		55	85	115	ns
$t_{d(EH-A)}$	Delay time, $\overline{ENABLE}$ rise to next address drive		175	210	280	ns
$t_{a(EL-D)}$	Access time, data input valid after $\overline{ENABLE}$ fall		165	210		ns
$t_{a(A-D)}$	Access time, address valid to data input valid		440	495		ns
$t_{d(A-EH)}$	Delay time, address valid to $\overline{ENABLE}$ rise		520	590	630	ns
$t_{h(EH-D)}$	Hold time, data input valid after $\overline{ENABLE}$ rise		0	0		ns
$t_{d(EH-JH)}$	Delay time, $\overline{ENABLE}$ rise to ALATCH rise		175	210	225	ns
$t_{d(CH-EL)}$	Delay time, CLKOUT rise to $\overline{ENABLE}$ fall		−10	25	35	ns

NOTE 6: $t_{c(C)}$ is defined to be $2/f_{osc}$ and may be referred to as a machine state or simply a state.

read and write cycle timing



NOTE 7: During an internal RAM access, the CPORT outputs are stable but the data is a ''don't care''.

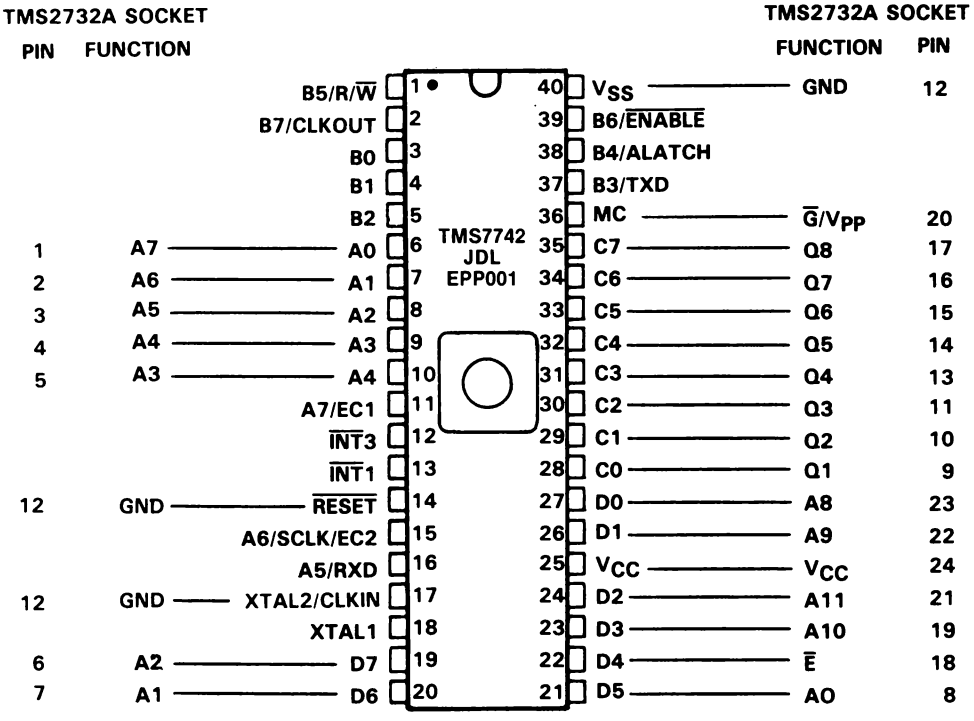
EPROM MODE

programming the TMS7742JDL.EPP001 using a PROM programmer

The TMS7742JDL.EPP001 can be programmed like any Texas Instruments TMS2732A on a wide variety of PROM programmers. Programming it requires a 40-to-24 pin adapter socket with the $\overline{\text{RESET}}$ and XTAL2 pins grounded. Contact your PROM programmer manufacturer or local TI field sales office for programming support. Please note that some PROM programmers have current limiting circuitry which is used to sense correct EPROM placements. The TMS7742JDL.EPP001 can draw up to 250 mA of current when being programmed, which may cause some PROM programmers to display insertion error messages. If this happens, use an external power supply for V_{CC}.

40-to-24 pin socket

The following diagram shows the connections needed to be made on the 40-to-24 pin socket.



erasure

The TMS7742JDL.EPP001 is erased by exposing the chip to shortwave ultraviolet light that has a wavelength of 253.7 nanometers (2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. The lamp should be located about 2.5 centimeters (1 inch) above the chip during erasure. After erasure, all bits are at a high level. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS7742JDL.EPP001 the window should be covered with an opaque label.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS†	MIN	MAX	UNIT
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, $t_r \leq$ 20 ns, $t_f \leq$ 20 ns		1	μs
$t_{en(G)}$	Output enable time from $\overline{G}$			350	ns
$t_{dis(G)}$‡	Output disable time from $\overline{G}$			350	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$ whichever occurs first		0		ns

†Timing measurement reference levels for inputs and outputs are 0.8 V and 2 V.
‡Value calculated from 0.5 V delta to measured output level.

recommended conditions for programming, T_A = 25°C

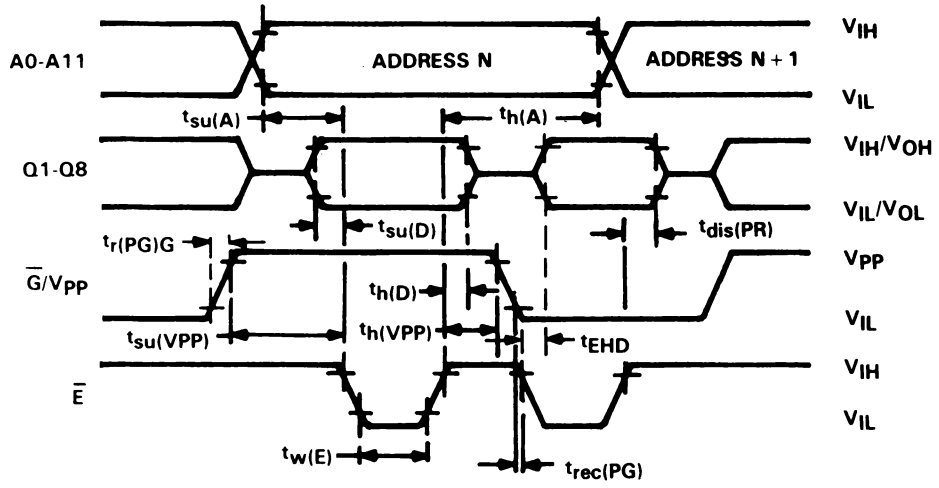
		MIN	NOM	MAX	UNIT
$t_{w(E)}$	$\overline{E}$ pulse duration	45	50	55	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{h(VPP)}$	V_{PP} hold time	2			μs
$t_{rec(PG)}$	V_{PP} recovery time	2			μs
$t_{r(PG)G}$	$\overline{G}$ rise time during programming	50			ns
t_{EHD}	Delay time, data valid after $\overline{E}$ low			1	μs

programming characteristics, T_A = 25°C

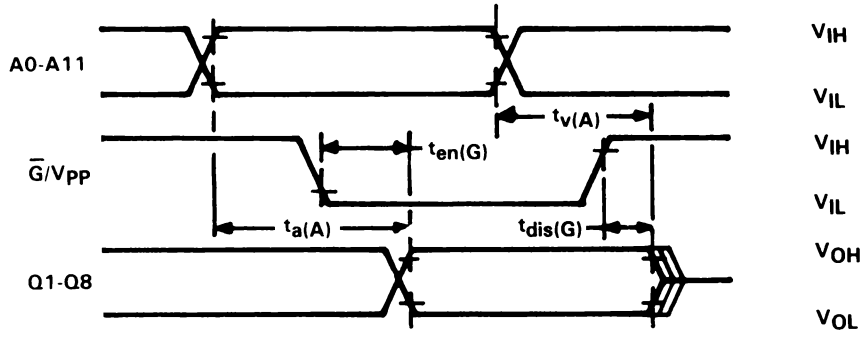
PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$t_{dis(PR)}$	Output disable time		0		100	ns

†Timing measurement reference levels for inputs and outputs are 0.8 V and 2 V.

program cycle timing



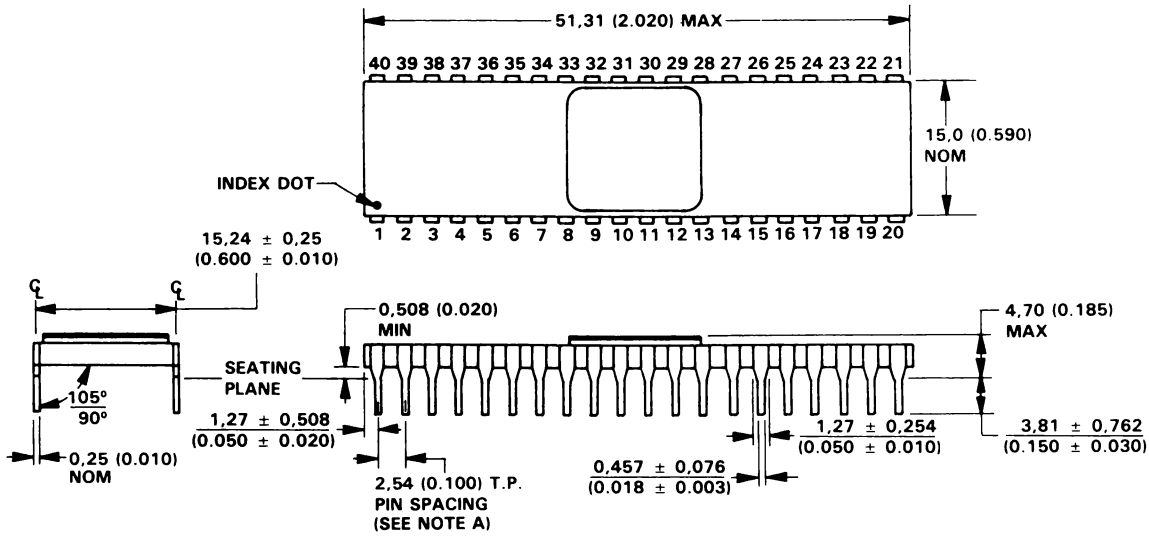
read cycle timing



NOTE 8: The timing measurement reference levels for inputs and outputs are 0.8 V and 2 V.

MECHANICAL DATA

40-pin JD ceramic sidebraze package

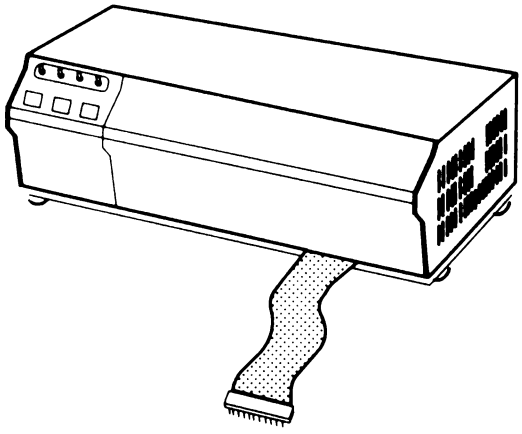


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE A: Each pin centerline is located within 0.254 (0.010) of its true longitudinal position.

TMS7742JDL.EPP001 DEVELOPMENT SUPPORT

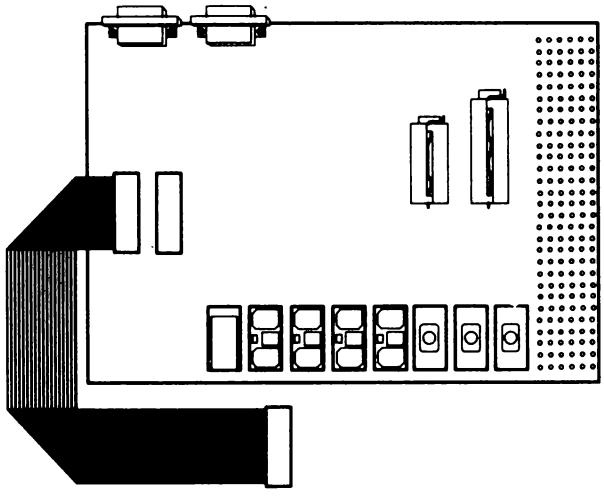
XDS* – extended development system



- Full TMS7000 Family Development System
- Host Independent/RS-232-C Interface
- Full Speed 8 MHz In-Circuit Emulation
- Extensive Breakpoint and Trace Functions
  - —Detailed Timing Analysis
  - —2K-Byte Trace Samples
  - —Breakpoint Sequencing Ability
- Command/Default Storage
- Removable Target Connector
- External Probe for Breakpoint/ Trace Qualifiers
- On-Board Assembler and Reverse Assembler
- Multiprocessing Capabilities

EVM – evaluation module

- TMS7000 Family Low Cost Development System
- Single-Chip Mode Emulation Only
- On-Board Assembler/Line Text Editor
- On-Board Hardware/Software Debugger
- Multiple Breakpoints
- Trace Display Function
- EPROM Programmer Utilities
- NMOS and CMOS versions



PROM programmers

Please contact your PROM programmer manufacturer or local TI field sales office for TMS7742JDL.EPP001 programming support. Please note that an adapter socket may be required by certain PROM programmers. These sockets may be obtained through the PROM programmer manufacturer or directly through your local Texas Instruments field sales office.

assembler/linker packages

Crossware* assembler/linker packages are available through Texas Instruments for the following operating systems: MVS,† CMS,† PC†-DOS, MS‡-DOS, VMS,§ and DX10.*

*XDS, Crossware, and DX10 are registered trademarks of Texas Instruments Incorporated.
†MVS, CMS, and PC-DOS are registered trademarks of International Business Machines Corporation.
‡MS-DOS is a registered trademark of Microsoft Corporation.
§VMS is a registered trademark of Digital Equipment Corporation.

TI Sales Offices

BELGIË/BELGIQUE
N.V. Texas Instruments Belgium S.A.
Mercure Centre
Raketstraat, 100, Rue de la Fusée
1130 Brussel/Bruxelles
Tel : (02) 720 80 00
Télex : 61161 TEXBEL

DANMARK
Texas Instruments A/S
Marielundvej 46E
2730 Herlev
Tel : (02) 917400
Telex : 35123 TEXIN

DEUTSCHLAND
Texas Instruments
Deutschland GmbH.
Haggertystr. 1
8050 Freising
Tel : 08161/80-4002
Telex : 526529

Kurfürstendamm 195-196
1000 Berlin 31
Tel : 030/8 82 73 65

Frankfurter Allee 6-8
6236 Eschborn
Tel : 06196/80 70

EIRE
Texas Instruments (Ireland)
Brewery Road
Stillorgan
Co. Dublin
Tel : (01) 831311

ESPAÑA
Texas Instruments España S.A.
C/José Lázaro Galdiano No. 6
28036 Madrid
Tel : (1) 4581458
Telex : 23634

FRANCE
Texas Instruments France
8-10 Avenue Morane Saulnier
78141 Vélizy-Villacoublay Cedex
Tel : (1) 39 46 97 12
Telex : 698707 F

HOLLAND
Texas Instruments Holland B.V.
Hogehilweg 19
Postbus 12995
1100 AZ Amsterdam-Zuidoost
Tel : (020) 5602911
Telex : 12196

ITALIA
Texas Instruments Italia S.p.A.
Divisione Semiconduttori
Nucleo Industriale
Viale Delle Scienze, 1
02015 Cittaducale (Rieti)
Tel : (0746) 6941
Telex : 611003 TISIT I

NORGE
Texas Instruments Norge A/S
PB 106
Refstad (Sinsenveien 53)
0585 Oslo 5
Tel : (02) 155090

ÖSTERREICH
Texas Instruments Ges.mbH.
Industriestr. B/16
A-2345 Brunn am Gebirge
Tel : (02236) 846210
Telex : 79304

PORTUGAL
Texas Instruments Equipamento
Electronico (Portugal) LDA.
R. Eng. Frederico Ulrich, 2650
Moreira Da Maia
4470 Maia
Tel : (2) 948 1003
Telex : 22485

SCHWEIZ/SUISSE
Texas Instruments Switzerland AG
Riedstraße 6
CH-8953 Dietikon
Tel : (01) 740 22 20
Telex : 56260 TEXIN

SUOMI FINLAND
Texas Instruments OY
Ahertajantie 3
P.O. Box 81,
0201 Espoo
Tel : (90) 0-461-422
Telex : 121457

SVERIGE
Texas Instruments
International Trade Corporation
(Sverigefilialen)
Nörra Hamnvagen 3
BOX 39103
100 54 Stockholm
Tel : (08) 235480
Telex : 10377

UNITED KINGDOM
Texas Instruments Ltd.
Manton Lane,
Bedford, MK41 7PA
Tel : (0234) 67466
Telex : 82178

Technical Enquiry Service
Tel : (0234) 223000

TI Regional Technology Centres

DEUTSCHLAND
Texas Instruments
Deutschland GmbH.
Haggertystraße 1
8050 Freising
Tel : 08161/80-4002

TEXAS INSTRUMENTS

Creating useful products
and services for you.

Kirchhorsterstraße 2
3000 Hannover 51
Tel : 0511/64 80 21

III. Hagen 43/Kibbelstraße 19
4300 Essen 1
Tel : 0201/24 25-0

Maybachstr. 11
7302 Ostfildern 2/Nellingen
Stuttgart
Tel : 0711/34 03-0

FRANCE
Centre de Technologie
Texas Instruments France
8-10 Avenue Morane Saulnier
78141 Vélizy-Villacoublay Cedex
Tel : (1) 39 46 97 12
Telex : 698707 F

Texas Instruments France
Boite Postale 5
06270 Villeneuve-Loubet
Tel : 93 20 01 01
Telex : 470127 F

HOLLAND
Texas Instruments Holland B.V.
Hogehilweg 19
Postbus 12995
1100 AZ Amsterdam-Zuidoost
Tel : (020) 5602911
Telex : 12196

ITALIA
Texas Instruments Italia S.p.A.
Divisione Semiconduttori
Nucleo Industriale
Viale Delle Scienze, 1
02015 Cittaducale (Rieti)
Tel : (0746) 6941
Telex : 611003 TISIT I

Texas Instruments Italia S.p.A.
Divisione Semiconduttori
Viale Europa 40,
20093 Cologno Monzese (Milano)
Tel : (02) 25300 1
Telex : 332633 MITEX I

SVERIGE
Texas Instruments
International Trade Corporation
(Sverigefilialen)
Nörra Hamnvagen 3
BOX 39103
100 54 Stockholm
Tel : (08) 235480
Hotline : (08) 615448

UNITED KINGDOM
Texas Instruments Ltd.
Regional Technology Centre
Manton Lane,
Bedford, MK41 7PA
Tel : (0234) 67466
Telex : 82178

Technical Enquiry Service
Tel : (0234) 223000

Printed in France.

GBNDs681S/C418ET-A