TEXAS INSTRUMENTS

TMS320C2x Reference Card

Phone Numbers

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Instruction Symbols

Symbol	Meaning
ARn	Auxiliary Register (AR0 and AR1) are predefined assembler symbols equal to 0 and 1, respectively
ARP	Auxiliary register pointer
B	Bit code
BR	Branch address
D	Data memory address or indirect addressing control bits
dma	Data memory address
I	Indirect/direct addressing mode; 1 = indirect, 0 = direct
ind	Indirect address: {*|*+|*–|*0+|*0–} for '20; {*|*+|*–|*0+|*0–|*BR0+|*BR0–} for 'C25
italics	User-defined terms
K	Immediate value
PA	Port address
pma	Program memory address
S	Shift count
[ ]	Options

Status Register ST0 Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ARP				OV	OVM	1	INTM	DP							

Status Register ST1 Bits

15	14	13	12†	11	10	9‡	8	7†	6‡	5‡	4	3	2	1	0
ARB			CNF	TC	SXM	C	1	1	HM	FSM	XF	FO	TXM	PM	

† On theTMS32026, bit 7 is CNF1 and bit 12 is CNF0.
‡ On theTMS32020, bits 5, 6, and 9 of ST1 are ones.

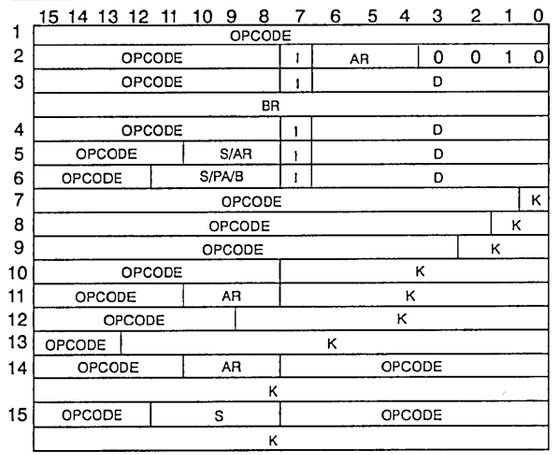
Instruction Set Summary

Instr	Description	C†/W
ABS	Absolute value of accumulator	1/1
ADD	Add to accumulator with shift	1/1
ADDC‡	Add to accumulator with carry	1/1
ADDH	Add to high accumulator	1/1
ADDK‡	Add to accumulator short immediate	1/1
ADDS	Add to low accumulator with sign-extension sup-	1/1
ADDT	Add to accumulator with shift specified by T register	1/1
ADLK	Add to accumulator long immediate with shift	2/2

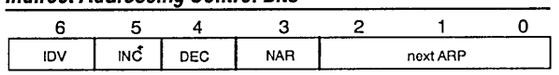
† Cycles using full-speed, on-chip, external program memory.
‡ These instructions are not available on the TMS32020.

ARP Auxiliary register pointer
OV Accumulator overflow flag bit
OVM Overflow mode bit
INTM Interrupt mask bit
DP Data memory page pointer
ARB Auxiliary register pointer buffer
CNF On-chip RAM configuration control bit
TC Test/control flag bit
SXM Sign-extension mode bit
FSM Frame synchronization mode bit
XF XF pin status bit
FO Format bit
TXM Transmit mode bit
PM Product shift mode bits

Instruction Format Description



Indirect Addressing Control Bits



IDV Increment/decrement value
INC Increment flag; 1 increments auxiliary register
DEC Decrement flag; 1 decrements auxiliary register
NAR New auxiliary register control bit; 1 loads new ARP
ARP Auxiliary register pointer

6	5	4	Operation	6	5	4	Operation
0	0	0	*	1	0	0	*BRO–
0	0	1	*–	1	0	1	*0–
0	1	0	*+	1	1	0	*0+
0	1	1	Not used	1	1	1	*BRO+

Operand Options	Opcode	Format
None	0CE1Bh	1
dma [, *shift*] *ind* [, *shift* [, *next ARP*]]	00000h	6
dma; ind [, *next ARP*]	04300h	4
dma; ind [, *next ARP*]	04800h	4
constant	0CC00h	10
dma;	04900h	4
dma; ind [, *next ARP*]	04A00h	4
constant [, *shift*]	0D002h	15

Instruction Set Summary (Continued)

Instr	Description	C†/W
ADRK‡	Add to auxiliary register short immediate	1/1
AND	AND with accumulator	1/1
ANDK	AND immediate with accumulator with shift	2/2
APAC	Add P register to accumulator	1/1
B	Branch unconditionally	3/2
BACC	Branch to address specified by accumulator	3/1
BANZ	Branch on auxiliary register not zero	3/2
BBNZ	Branch if TC bit ≠ 0	3/2
BBZ	Branch if TC bit = 0	3/2
BC‡	Branch on carry	3/2
BGEZ	Branch if accumulator ≥ 0	3/2
BGZ	Branch if accumulator > 0	3/2
BIOZ	Branch on I/O status = 0	3/2
BIT	Test bit	1/1
BITT	Test bit specified by T register	1/1
BLEZ	Branch if accumulator ≤ 0	3/2
BLKD	Block move from data memory to data memory	4/2
BLKP	Block move from program memory to data memory	4/2
BLZ	Branch if accumulator < 0	3/2
BNC‡	Branch on no carry	3/2
BNV	Branch if no overflow	3/2
BNZ	Branch if accumulator ≠ 0	3/2
BV	Branch on overflow	3/2
BZ	Branch if accumulator = 0	3/2
CALA	Call subroutine indirect	3/1
CALL	Call subroutine	3/2
CMPL	Complement accumulator	1/1
CMPR	Compare auxiliary register with AR0	1/1
CNFD	Configure block as data memory	1/1
CNFP	Configure block as program memory	1/1
CONF¶	Configure block as data/program memory	1/1
DINT	Disable interrupt	1/1
DMOV	Data move in data memory	1/1
EINT	Enable interrupt	1/1
FORT	Format serial port registers	1/1
IDLE	Idle until interrupt	3/1
IN	Input data from port	2/1
LAC	Load accumulator with shift	1/1
LACK	Load accumulator short immediate	1/1
LACT	Load accumulator with shift specified by T register	1/1
LALK	Load accumulator long immediate with shift	2/2
LAR	Load auxiliary register	1/1
LARK	Load auxiliary register short immediate	1/1
LARP	Load auxiliary register pointer	1/1
LDP	Load data memory page pointer	1/1

† Cycles using full-speed, on-chip, external program memory.
‡ These instructions are not available on the TMS32020.
¶ This instruction configures RAM blocks B0, B1, B3 on the TMS320C26 replacing instructions CNFD and CNFP.

Operand Options	Opcode	Format
constant	07E00h	10
dma; ind [, *next ARP*]	04E00h	4
constant [, *shift*]	0D004h	15
None	0CE15h	1
pma; [, *ind* [, *next ARP*]]	0FF80h	3
None	0CE25h	1
pma [, *ind* [, *next ARP*]]	0FB80h	3
pma [, *ind* [, *next ARP*]]	0F980h	3
pma [, *ind* [, *next ARP*]]	0F880h	3
pma [, *ind* [, *next ARP*]]	05E80h	3
pma [, *ind* [, *next ARP*]]	0F480h	3
pma [, *ind* [, *next ARP*]]	0F180h	3
pma [, *ind* [, *next ARP*]]	0FA80h	3
dma, bit code; ind, bit code [, *next ARP*]	09000h	6
dma; ind [, *next ARP*]	05700h	4
pma [, *ind* [, *next ARP*]]	0F280h	3
dma1, dma2; dma1, ind [, *next ARP*]	0FD00h	4
pma, dma; pma, ind [, *next ARP*]	0FC00h	4
pma, ind [, *next ARP*]	0F380h	3
pma, ind [, *next ARP*]	05F80h	3
pma, ind [, *next ARP*]	0F780h	3
pma, ind [, *next ARP*]	0F580h	3
pma, ind [, *next ARP*]	0F080h	3
pma, ind [, *next ARP*]	0F680h	3
None	0CE24h	1
pma, ind [, *next ARP*]	0FE80h	3
None	0CE27h	1
constant	0CE50h	8
None	0CE04h	1
None	0CE05h	1
constant	0CE3Ch	8
None	0CE01h	1
dma; ind [, *next ARP*]	05600h	4
None	0CE00h	1
constant	0CE0Eh	7
None	0CE1Fh	1
dma, PA; ind, PA [, *next ARP*]	08000h	6
dma [, *shift*]; *ind* [, *shift* [, *next ARP*]]	02000h	6
constant	0CA00h	10
dma; ind [, *next ARP*]	04200h	4
constant [, *shift*]	0D001h	15
AR, dma; AR, ind [, *next ARP*]	03000h	5
AR, constant	0C000h	11
constant	05588h	9
dma; ind [, *next ARP*]	05200h	4

Instruction Set Summary (Continued)

Instr	Description	C†/W
LDPK	Load data memory page pointer immediate	1/1
LPH	Load high P register	1/1
LRLK	Load auxiliary register long immediate	2/2
LST	Load status register ST0	1/1
LST1	Load status register ST1	1/1
LT	Load T register	1/1
LTA	Load T register and accumulate previous product	1/1
LTD	Load T register, accumulate previous product, move data	1/1
LTP	Load T register and store P register in accumulator	1/1
LTS	Load T register and subtract previous product	1/1
MAC	Multiply and accumulate	4/2
MACD	Multiply and accumulate with data move	4/2
MAR	Modify auxiliary register	1/1
MPY	Multiply (with T register, store product in P register)	1/1
MPYA‡	Multiply and accumulate previous product	1/1
MPYK	Multiply immediate	1/1
MPYS‡	Multiply and subtract previous product	1/1
MPYU‡	Multiply unsigned	1/1
NEG	Negate accumulator	1/1
NOP	No operation	1/1
NORM	Normalize contents of accumulator	1/1
OR	OR with accumulator	1/1
ORK	OR immediate with accumulator with shift	2/2
OUT	Output data to port	1/1
PAC	Load accumulator with P register	1/1
POP	Pop top of stack to low accumulator	1/1
POPD	Pop top of stack to data memory	1/1
PSHD	Push data memory value onto top of stack	1/1
PUSH	Push low accumulator onto stack	1/1
RC‡	Reset carry bit	1/1
RET	Return from subroutine	3/1
RFSM‡	Reset serial port frame synchronization mode	1/1
RHM‡	Reset hold mode	1/1
ROL‡	Rotate accumulator left	1/1
ROR‡	Rotate accumulator right	1/1
ROVM	Reset overflow mode	1/1
RPT	Repeat instruction as specified by data memory value	1/1
RPTK	Repeat instruction as specified by immediate value	1/1
RSXM	Reset sign-extension mode	1/1
RTC‡	Reset test/control flag	1/1
RTXM	Reset serial port transmit mode	1/1
RXF	Reset external flag	1/1
SACH	Store high accumulator with shift	1/1
SACL	Store low accumulator	1/1
SAR	Store auxiliary register	1/1
SBLK	Subtract from accumulator long immediate with shift	2/2

† Cycles using full-speed, on-chip, external program memory.
‡ These instructions are not available on the TMS32020.

Operand Options	Opcode	Format
constant	0C800h	12
dma; ind [, *next ARP*]	05300h	4
AR, constant	0D000h	14
dma; ind [, *next ARP*]	05000h	4
dma; ind [, *next ARP*]	05100h	4
dma; ind [, *next ARP*]	03C00h	4
dma; ind [, *next ARP*]	03D00h	4
dma; *ind* [, *next ARP*]	03F00h	4
dma; ind [, *next ARP*]	03E00h	4
dma; ind [, *next ARP*]	05B00h	4
pma, dma; pma, ind [, *next ARP*]	05D00h	4
pma, dma; pma, ind [, *next ARP*]	05C00h	4
dma; ind [, *next ARP*]	05500h	4
dma;ind [, *next ARP*]	03800h	4
dma; ind [, *next ARP*]	03A00h	4
constant	0A000h	13
dma; ind [, *next ARP*]	03B00h	4
dma; ind [, *next ARP*]	0CF00h	4
None	0CE23h	1
None	05500h	1
ind	0CE82h	2
dma; ind [, *next ARP*]	04D00h	4
constant [, *shift*]	0D005h	15
dma, PA; ind PA [, *next ARP*]	0E000h	6
None	0CE14h	1
None	0CE1Dh	1
dma; ind [, *next ARP*]	07A00h	4
dma; ind [, *next ARP*]	05400h	4
None	0CE1Ch	1
None	0CE30h	1
None	0CE26h	1
None	0CE36h	1
None	0CE38h	1
None	0CE34h	1
None	0CE35h	1
None	0CE02h	1
dma; ind [, *next ARP*]	04B00h	4
constant	0CB00h	10
None	0CE06h	1
None	0CE32h	1
None	0CE20h	1
None	0CE0Ch	1
dma [, *shift*]; *ind* [, *shift* [, *next ARP*]]	06800h	5
dma; ind [, *shift* [, *next ARP*]]	06000h	5
AR, dma; AR, ind [, *next ARP*]	07000h	5
constant [, *shift*]	0D003h	15

Instruction Set Summary (Continued)

Instr	Description	C†/W
SBRK‡	Subtract from auxiliary register short immediate	1/1
SC‡	Set carry bit	1/1
SFL	Shift accumulator left	1/1
SFR	Shift accumulator right	1/1
SFSM‡	Set serial port frame synchronization mode	1/1
SHM‡	Set hold mode	1/1
SOVM	Set overflow mode	1/1
SPAC	Subtract P register from accumulator	1/1
SPH‡	Store high P register	1/1
SPL‡	Store low P register	1/1
SPM	Set P register output shift mode	1/1
SQRA	Square and accumulate	1/1
SQRS	Square and subtract previous product	1/1
SST	Store status register ST0	1/1
SST1	Store status register ST1	1/1
SSXM	Set sign-extension mode	1/1
STC‡	Set test/control flag	1/1
STXM	Set serial port transmit mode	1/1
SUB	Subtract from accumulator with shift	1/1
SUBB‡	Subtract from accumulator with borrow	1/1
SUBC	Conditional subtract	1/1
SUBH	Subtract from high accumulator	1/1
SUBK‡	Subtract from accumulator short immediate	1/1
SUBS	Subtract from low accumulator with no sign extension	1/1
SUBT	Subtract from accumulator with shift specified by T register	1/1
SXF	Set external flag	1/1
TBLR	Table read	4/1
TBLW	Table write	3/1
TRAP	Software interrupt	3/1
XOR	Exclusive-OR with accumulator	1/1
XORK	Exclusive-OR immediate with accumulator with shift	2/2
ZAC	Zero accumulator	1/1
ZALH	Zero low accumulator and load high accumulator	1/1
ZALR‡	Zero low accumulator and load high accumulator with rounding	1/1
ZALS	Zero low accumulator, load low accumulator with no sign extension	1/1

† Cycles using full-speed, on-chip, external program memory.
‡ These instructions are not available on the TMS32020.

Operand Options	Opcode	Format
constant	07F00h	10
None	0CE31h	1
None	0CE18h	1
None	0CE19h	1
None	0CE37h	1
None	0CE39h	1
None	0CE03h	1
None	0CE16h	1
dma; ind [, *next ARP*]	07D00h	4
dma; ind [, *next ARP*]	07C00h	4
constant	0CE08h	8
dma; ind [, *next ARP*]	03900h	4
dma; ind [, *next ARP*]	05A00h	4
dma; ind [, *next ARP*]	07800h	4
dma; ind [, *next ARP*]	07900h	4
None	0CE07h	1
None	0CE33h	1
None	0CE21h	1
dma [, *shift*]; *ind* [, *shift* [, *next ARP*]]	01000h	6
dma; ind [, *next ARP*]	04F00h	4
dma; ind [, *next ARP*]	04700h	4
dma; ind [, *next ARP*]	04400h	4
constant	0CD00h	10
dma;ind [, *next ARP*]	04500h	4
dma; *ind* [, *next ARP*]	04600h	4
None	0CE0Dh	1
dma; ind [, *next ARP*]	05800h	4
dma; ind [, *next ARP*]	05900h	4
None	0CE1Eh	1
dma; ind [, *next ARP*]	04C00h	4
constant [, *shift*]	0D006h	15
None	0CA00h	1
dma; ind [, *next ARP*]	04000h	4
dma; *ind* [, *next ARP*]	07B00h	4
dma; *ind* [, *next ARP*]	04100h	4