Instruction Set Summary (Concluded)

Mnemonic	Description	# Words	Instruction Bit Code
			FEDCBA9876543210
STXM	Set serial port transmit mode	1	1100111000100001
SUB	Subtract from accumulator with shift	1	0001←S →I←— D—→
SUBB	Subtract from accumulator with borrow	1	01001111 I←— D—→
SUBC	Conditional subtract	1	01000111 I←— D—→
SUBH	Subtract from high accumulator	1	01000100 I←— D—→
SUBK	Subtract from accumulator short immediate	1	11001101←—K—→
SUBS	Subtract from low accumulator with sign-extension suppressed	1	01000101 I←— D—→
SUBT	Subtract from accumulator with shift specified by T register	1	01000110 I←— D—→
SXF	Set external flag	1	1100111000001101
TBLR	Table read	1	01011000 I←— D—→
TBLW	Table write	1	01011001 I←— D—→
TRAP	Software interrupt	1	1100111000011110
XOR	Exclusive-OR with accumulator	1	01001100 I←— D—→
XORK	Exclusive-OR immediate with accumulator with shift	2	1101←S →00000110
ZAC	Zero accumulator	1	1100101000000000
ZALH	Zero low accumulator and load high accumulator	1	01000000 I←— D—→
ZALR	Zero low accumulator and load high accumulator with rounding	1	01111011 I←— D—→
ZALS	Zero accumulator and load low accumulator with sign-extension suppressed	1	01000001 I←— D—→

Assembler Directives (Concluded)

LOAD (Force Load): Defines symbols for other programs.
[<label>] LOAD <symbol>[,<symbol>] [<comment>]

MLIB (Define MACRO Library): Specifies the library containing macro definitions.
[<label>] MLIB '<pathname>' [<comment>]

OPTION (Output Options): Selects several options for the assembler listing output.
[<label>] OPTION <option list> [<comment>]

PAGE (Eject Page): Continues source listing on new page.
[<label>] PAGE [<comment>]

PEND (Program Segment End): Terminates definition of a block of program-relocatable code.
[<label>] PEND [<comment>]

PSEG (Program Segment): Defines succeeding locations as program-relocatable.
[<label>] PSEG [<comment>]

REF (External Reference): Provides access to symbols defined in other programs.
[<label>] REF <symbol>[,<symbol>] [<comment>]

RORG (Relocatable Origin): Defines succeeding locations as program-relocatable and initializes location counter.
[<label>] RORG [[<exp>] /<comment>/]

SREF (Secondary External Reference): Provides secondary access to symbols defined in other programs.
[<label>] SREF <symbol>[,<symbol>] [<comment>]

TEXT (Initialize Text): Places a character string in successive program memory words.
[<label>] TEXT [-]'<string>' [<comment>]

TITL (Page Title): Supplies source listing page titles.
[<label>] TITL '<string>' [<comment>]

UNL (Stop Source Listing): Halts source listing output until the occurrence of a LIST directive.
[<label>] UNL [<comment>]

XEND (Independent Segment End): Terminates definition of an independently stored program segment, definedby EXEC.
[<label>] XEND [<comment>]

TMS320C25
DIGITAL SIGNAL PROCESSOR
Programmer's Reference Card

TI Customer Response Center (CRC) Hotline Number

For help with the TMS320C25, call 1-800-232-3200.

Symbols for Instruction Set Summary

SYMBOL	MEANING
B	4-bit field specifying a bit code
CM	2-bit field specifying compare mode
D	Data memory address field
FO	Format status bit
I	Addressing mode bit
K	Immediate operand field
PA	Port address (PA0 through PA15 are predefined assembler symbols equal to 0 through 15, respectively.)
PM	2-bit field specifying P register output shift code
R	3-bit operand field specifying auxiliary register
S	4-bit left-shift code
X	3-bit accumulator left-shift field

Assembler Directives

AORG (Absolute Origin): Defines succeeding locations as absolute and places a value in the location counter.
[<label>] AORG [<exp> /<comment>/]

BES (Block Ending with Symbol): Advances location counter and assigns a label the value of location following block.
[<label>] BES <exp> [<comment>]

BSS (Block Starting with Symbol): Advances location counter and assigns a label the value of location of first word in block.
[<label>] BSS <exp> [<comment>]

CEND (Common Segment End): Terminates definition of a block of common-relocatable code.
[<label>] CEND [<comment>]

COPY (Copy Source File): Causes source statements to be read from a different file.
[<label>] COPY <file-name> [<comment>]

CSEG (Common Segment): Defines succeeding locations as common-relocatable.
[<label>] CSEG ['<string>' /<comment>/]

DATA (Initialize Word): Places values in successive program memory words.
[<label>] DATA <exp>[,<exp>] [<comment>]

DEF (External Definition): Defines symbols for other programs.
[<label>] DEF <symbol>[,<symbol>] [<comment>]

DEND (Data Segment End): Terminates definition of a block of data-relocatable code.
[<label>] DEND [<comment>]

DORG (Dummy Origin): Defines succeeding locations as a dummy block.
[<label>] DORG <exp> [<comment>]

DSEG (Data Segment): Defines succeeding locations as data-relocatable.
[<label>] DSEG [<comment>]

END (Program End): Terminates the assembly.
[<label>] END [<symbol>/<comment/]

EQU (Define Assembly-Time Constant): Assigns symbol value.
[<label>] EQU <exp> [<comment>]

EXEC (Independent Program Segment): Defines independently stored program segment and loads location counter.
[<label>] EXEC <pma> [<comment>]

IDT (Program Identifier): Names the object module produced.
[<label>] IDT '<string>' [<comment>]

LIST (Restart Source Listing): Resumes source listing.
[<label>] LIST [<comment>]

TEXAS INSTRUMENTS

Instruction Set Summary

Mnemonic	Description	# Words	Instruction Bit Code
			FEDCBA9876543210
ABS	Absolute value of accumulator	1	1100111000001101
ADD	Add to accumulator with shift	1	0000←S→|← D→
ADDC	Add to accumulator with carry	1	01000011 |← D→
ADDH	Add to high accumulator	1	01001000 |← D→
ADDK	Add to accumulator short immediate	1	11001100←K→
ADDS	Add to low accumulator with sign-extension suppressed	1	01001001 |← D→
ADDT	Add to accumulator with shift specified by T register	1	01001010 |← D→
ADLK	Add to accumulator long immediate with shift	2	1101←S→00000010
ADRK	Add to auxiliary register short immediate	1	01111110←K→
AND	AND with accumulator	1	01001110 |← D→
ANDK	AND immediate with accumulator with shift	2	1101←S→00000100
APAC	Add P register to accumulator	1	1100111000010101
B	Branch unconditionally	2	11111111 1←D→
BACC	Branch to address specified by accumulator	1	1100111000100101
BANZ	Branch on auxiliary register not zero	2	11111011 1←D→
BBNZ	Branch if TC bit ≠ 0	2	11111001 1←D→
BBZ	Branch if TC bit = 0	2	11111000 1←D→
BC	Branch on carry	2	01011111 01←D→
BGEZ	Branch if accumulator ≥ 0	2	11110100 1←D→
BGZ	Branch if accumulator > 0	2	11110001 1←D→
BIT	Test bit	1	1001←B→|← D→
BITT	Test bit specified by T register	1	01010111 |← D→
BIOZ	Branch on I/O status = 0	2	11111010 1←D→
BLEZ	Branch if accumulator ≤ 0	2	11111001 0←D→
BLKD	Block move from data memory to data memory	2	11111101 |← D→
BLKP	Block move from program memory to data memory	2	11111100 |← D→
BLZ	Branch if accumulator < 0	2	11111001 1←D→
BNC	Branch on no carry	2	01011111 1←D→
BNV	Branch if no overflow	2	11111011 1←D→
BNZ	Branch if accumulator ≠ 0	2	11111010 1←D→
BV	Branch on overflow	2	11111000 0←D→
BZ	Branch if accumulator = 0	2	11111010 1←D→
CALA	Call subroutine indirect	1	1100111000100100
CALL	Call subroutine	2	11111110 1←D→
CMPL	Complement accumulator	1	1100111000100111
CMPR	Compare auxiliary register with auxiliary register AR0	1	11001110010100 CM
CNFD	Configure block as data memory	1	1100111000000100
CNFP	Configure block as program memory	1	1100111000000101
DINT	Disable interrupt	1	1100111000000001
DMOV	Data move in data memory	1	01010110 |← D→
EINT	Enable interrupt	1	1100111000000000
FORT	Format serial port registers	1	1100111000000111FO
IDLE	Idle until interrupt	1	1100111000001111
IN	Input data from port	1	1000←PA→|← D→
LAC	Load accumulator with	1	0010←S →|← D→
LACK	Load accumulator immediate short	1	11001010←K→
LACT	Load accumulator with shift specified by T register	1	01000010 |← D→
LALK	Load accumulator long immediate with shift	2	1101←S→00000001
LAR	Load auxiliary register	1	00110←R→|← D→
LARK	Load auxiliary register immediate short	1	11000←R→|←K→
LARP	Load auxiliary register pointer	1	0101010110001←R→
LDP	Load data memory page pointer	1	01010010 |← D→
LDPK	Load data memory page pointer immediate	1	1100100←K→
LPH	Load high P register	1	01010011 |← D→
LST	Load status register ST0	1	01010000 |← D→
LST1	Load status register ST1	1	01010001 |← D→
LRLK	Load auxiliary register long immediate	2	11010←R→00000000
LT	Load T register	1	00111100 |← D→

Instruction Set Summary (Continued)

Mnemonic	Description	# Words	Instruction Bit Code
			FEDCBA9876543210
LTA	Load T register and accumulate previous product	1	00111101 |← D→
LTD	Load T register, accumulate previous product, and move data	1	00111111 |← D→
LTP	Load T register and store P register in accumulator	1	00111110 |← D→
LTS	Load T register and subtract previous product	1	01011011 |← D→
MAC	Multiply and accumulate	2	01011101 |← D→
MACD	Multiply and accumulate with data move	2	01011100 |← D→
MAR	Modify auxiliary register	1	01010101 |← D→
MPY	Multiply (with T register, store product in P register)	1	00111000 |← D→
MPYA	Multiply and accumulate previous product	1	00111010 |← D→
MPYK	Multiply immediate	1	101←K→
MPYS	Multiply and subtract previous product	1	00111011 |← D→
MPYU	Multiply unsigned	1	11001111 |← D→
NEG	Negate accumulator	1	1100111000010001
NOP	No operation	1	0101010100000000
NORM	Normalize contents of accumulator	1	11001110 1←D→
OR	OR with accumulator	1	01001101 |← D→
ORK	OR immediate with accumulator with shift	2	1101←S→00000101
OUT	Output data to port	1	1110←PA→|← D→
PAC	Load accumulator with P register	1	1100111000010100
POP	Pop top of stack to low accumulator	1	1100111000011101
POPD	Pop top of stack to data memory	1	01111010 |← D→
PSHD	Push data memory value onto stack	1	01010100 |← D→
PUSH	Push low accumulator onto stack	1	1100111000011100
RC	Reset carry bit	1	1100111000110000
RET	Return from subroutine	1	1100111000100110
RFSM	Reset serial port frame synchronization mode	1	1100111000110110
RHM	Reset hold mode	1	1100111000111000
ROL	Rotate accumulator left	1	1100111000110100
ROR	Rotate accumulator right	1	1100111000110101
ROVM	Reset overflow mode	1	1100111000000010
RPT	Repeat instruction as specified by data memory value	1	01001011 |← D→
RPTK	Repeat instruction as specified by immediate value	1	11001011←K→
RSXM	Reset sign-extension mode	1	1100111000000110
RTC	Reset test/control flag	1	1100111000110010
RTXM	Reset serial port transmit mode	1	1100111000100000
RXF	Reset external flag	1	1100111000001100
SACH	Store high accumulator with shift	1	01101←X→|← D→
SACL	Store low accumulator with shift	1	01100←X→|← D→
SAR	Store auxiliary register	1	01110←R→|← D→
SBLK	Subtract from accumulator long immediate with shift	2	1101←S→00000011
SBRK	Subtract from auxiliary register short immediate	1	01111111←K→
SC	Set carry bit	1	1100111000110001
SFL	Shift accumulator left	1	1100111000001000
SFR	Shift accumulator right	1	1100111000011001
SFSM	Set serial port frame synchronization mode	1	1100111000110111
SHM	Set hold mode	1	1100111000111001
SOVM	Set overflow mode	1	1100111000000011
SPAC	Subtract P register from accumulator	1	1100111000010110
SPH	Store high P register	1	01111101 |← D→
SPL	Store low P register	1	01111100 |← D→
SPM	Set P register output shift mode	1	11001110000010 PM
SQRA	Square and accumulate	1	00111001 |← D→
SQRS	Square and subtract previous product	1	01011010 |← D→
SST	Store status register ST0	1	01111000 |← D→
SST1	Store status register ST1	1	01111001 |← D→
SSXM	Set sign-extension mode	1	1100111000000111
STC	Set test/control flag	1	1100111000110011