STANDARD MICROSYSTEMS CORPORATION

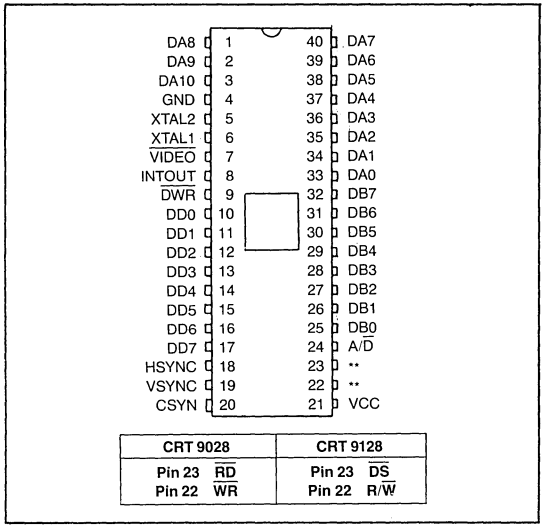
CRT 9028
CRT 9128
PRELIMINARY

VTLC
Video Terminal Logic Controller

FEATURES

- ☐ Built-in High Frequency (4-14 MHz) Oscillator
- ☐ Built-in Video Shift Register
- ☐ Built-in Character Generator
- ☐ Bi-Directional Smooth Scroll Capability
- ☐ Visual Attributes Include Reverse Video, Intensity Control, Underline and Character Blank
- ☐ Separate HSYNC, VSYNC and VIDEO Outputs
- ☐ Composite Sync (RS170 Compatible) Output
- ☐ Absolute (RAM address) Cursor Addressing
- ☐ MASK Programmable Video Parameters:
  - Dots Per Character Block (6-8)
  - Raster Scans Per Data Row (8-12)
  - Characters Per Data Row (32, 48, 64, 80)
  - Data Rows Per Page (8,10,12,16,20,24 or 25)
  - Horizontal Blanking (8-64 Characters)
  - Horizontal Sync Front Porch (0-7 Characters)
  - Horizontal Sync Duration (1-64 Characters)
  - Horizontal Sync Polarity
  - Two Values of Vertical Blanking
  - Two Values of Vertical Sync Front Porch (0-63 Scan Lines)
  - Two Values of Vertical Sync Duration (1-16 Scan Lines)
  - Vertical Sync Polarity
  - Internal 128 Character 5x8 Dot Font
  - Character/Cursor Underline Position
  - Scan Row and Column for Thin Graphics Entity Segments
  - Scan Rows and Columns for Wide Graphics Entity Elements
- ☐ Software Enabled Non-Scrolling 25th Data Row Available with 25 Data Row/Page Display
- ☐ Non-Interlace Display Format
- ☐ Separate Display Memory Bus Eliminates Contention Problems
- ☐ Fill (Erase) Screen Capability
- ☐ Standard 8-bit Data Bus Microprocessor Interface
- ☐ Wide Graphics with Six Independently Addressable Segments Per Character Space
- ☐ Thin Graphics with Four Independently Addressable Segments Per Character Space
- ☐ Single +5V Supply
- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ TTL Compatible

PIN CONFIGURATION



CRT 9028	CRT 9128
Pin 23 RD	Pin 23 DS
Pin 22 WR	Pin 22 R/W

GENERAL DESCRIPTION

The CRT 9028 VTLC and CRT 9128 VTLC are mask programmable 40 pin COPLAMOS® n-channel MOS/LSI Video Display Controller Chips that combine video timing, video attributes, alphanumeric and graphics generation, smooth scroll and screen buffer interface functions.

The VTLC incorporates many of the features (previously requiring a number of external components) required in building a low cost yet versatile display interface. An internal mask programmable 128 character font provides for a full ASCII character set. Wide graphics allow plotting and graphing capabilities while thin graphics and visual attributes can make the display of forms straight-forward.

Two pinout configurations enhance the versatility of the VTLC. The CRT 9028 controls data flow over the processor system data bus through separate read ($\overline{RD}$) and write ($\overline{WR}$) strobes for use with the 8085, 8051, Z80®, 8086, and similar microprocessors or microcomputers. The CRT 9128 regulates the data flow with a data strobe ($\overline{DS}$) and read/write (R/$\overline{W}$) enable signals for use with the 6500, Z8™, 68000 and similar microprocessors or microcomputers.

The VTLC provides two independent data buses; one bus that interfaces to the processor and one that interfaces to the display memory. Data is transferred to the display memory from the processor through the VTLC eliminating contention problems and the need for a separate row buffer.

The VTLC has an internal crystal oscillator requiring only an external crystal to operate. Masked constants for critical video timing simplify programming, operation and improve reliability. A separate non-scrolling status line (enabled or disabled by the processor) is available for displaying system status.

*Z80 is a registered trademark of Zilog Corporation.
Z8 is a trademark of Zilog Corporation.

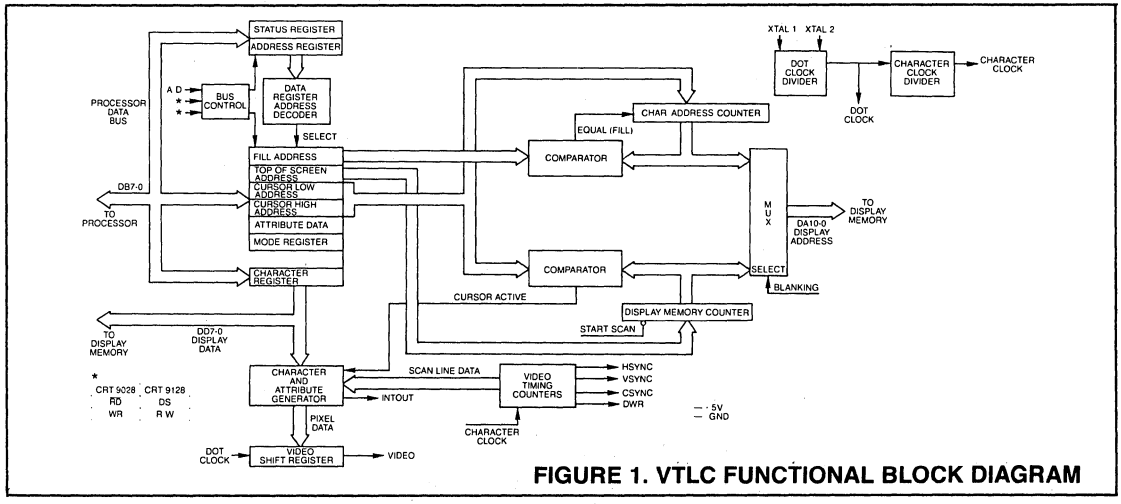


FIGURE 1. VTLC FUNCTIONAL BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	I/O	NAME	DESCRIPTION
3-1, 40-33	DA10-0	O	Display Address	11 bit address bus to display memory
4	GND		Ground	Ground Connection
5,6	XTAL2,1	I	Crystal 2,1	External Crystal An external TTL level clock may be used to drive XTAL1 (in which case XTAL2 is left floating).
7	$\overline{\text{VIDEO}}$	O	$\overline{\text{Video Output}}$	This output is a digital TTL waveform used to develop the VIDEO and composite VIDEO signals to the monitor. The polarity of this signal is: HIGH = BLACK LOW = WHITE
8	INTOUT	O	Intensity Output	This pin is the intensity level modification attribute bit (synchronized with the video data output).
9	$\overline{\text{DWR}}$	O	$\overline{\text{Display Write}}$	Write strobe to display memory
17-10	DD7-0	I/O	Display Data	8-bit bidirectional data bus to display memory
18	HSYNC	O	Horizontal Sync	Horizontal sync signal to monitor
19	VSYNC	O	Vertical Sync	Vertical sync signal to monitor
20	CSYNC	O	Composite Sync	This output is used to generate an RS170 compatible composite VIDEO signal for output to a composite VIDEO monitor.
21	V_{cc}		Power	5.0 V power connection
			CRT 9028	
22	$\overline{\text{WR}}$	I	$\overline{\text{Write Strobe}}$	Causes data on the microprocessor data bus to be strobed into the VTLC
23	$\overline{\text{RD}}$	I	$\overline{\text{Read Strobe}}$	Causes data from the VTLC to be strobed onto the microprocessor data bus
			CRT 9128	
22	R/$\overline{\text{W}}$	I	Read/$\overline{\text{Write}}$ Select	Determines whether the processor is reading data from or writing data into the VTLC (high for read, low for write)
23	$\overline{\text{DS}}$	I	$\overline{\text{Data Strobe}}$	Causes data to be strobed into or out of the VTLC from the microprocessor data bus depending on the state of the R/W signal
24	A/$\overline{\text{D}}$	I	Register Select	The state of this input pin will determine whether the data is being read from, or written to, the address or status register, or a data register.
32-25	DB7-0	I/O	Processor Data Bus	8-bit bi-directional processor data bus

DESCRIPTION OF OPERATION*

THE VTLC INTERNAL REGISTERS

CRT 9028

Addressing of the internal VTLC data registers of the CRT 9028 is accomplished through the use of the A/$\overline{D}$ select input qualified by the $\overline{RD}$ and $\overline{WR}$ strobes.

A/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	REGISTER OPERATION
0	1	0	WRITE TO DATA REGISTER
0	0	1	READ DATA REGISTER
1	1	0	WRITE TO ADDRESS REGISTER
1	0	1	READ STATUS REGISTER

CRT 9128

Addressing of the internal VTLC data registers of the CRT 9128 is accomplished through use of the A/$\overline{D}$ and R/$\overline{W}$ select inputs qualified by the $\overline{DS}$ strobe.

A/$\overline{D}$	$\overline{DS}$	R/$\overline{W}$	REGISTER OPERATION
0	0	0	WRITE TO DATA REGISTER
0	0	1	READ DATA REGISTER
1	0	0	WRITE TO ADDRESS REGISTER
1	0	1	READ STATUS REGISTER

The contents of the seven processor programmable registers located in the upper left hand side of the Functional Block Diagram of figure 1 indicate the memory locations from which screen data is to be fetched and displayed as well as the selected modes of display operation. These registers are addressed indirectly via the Address Register.

To access one of the seven eight-bit registers, the processor must first load the Address Register with the three-bit address of the selected data register. The next read or write to a data register will then cause the data register pointed to by the Address Register to be accessed. The Line A/$\overline{D}$ controls whether writing is occurring to the Address Register or to a data register. When a read operation is performed, A/$\overline{D}$ controls access to either the Status Register or to the data register selected by the Address Register.

REGISTER DESCRIPTION

ADDRESS REGISTER

Writing a byte to the ADDRESS register will select the specified register the next time the processor writes to or reads the VTLC data registers. The data register addresses are as follows:

STATUS REGISTER

When reading the STATUS register, the DONE bit (DB7 of STATUS Register) will represent the current status of the CHARACTER register. This bit is used to synchronize data transfers between the processor and the VTLC. The VTLC will set the DONE bit to a logic one after completing a byte transfer command or a FILL operation. The DONE bit is set to a logic zero by reading from, or writing to, the CHARACTER register. The processor must wait until the DONE bit is 1 before attempting to change the CURSOR ADDRESS, in order to write a character to, or read a character from, the CHARACTER register.

STATUS REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DONE	X	X	X	X	X	X	X

DONE = 1 signifies that external processor is allowed to access cursor ADDRESS and/or CHARACTER registers.

DONE = 0 signifies that external processor must wait until VTLC completes transfer of data between display memory and CHARACTER register.

DATA REGISTERS

FILADD (Fill Address) This register contains the RAM address of the character following the last address to be filled. Writing to this register will enable the VTLC "fill" circuitry. The FILL operation will then be triggered by the next processor write to the CHARACTER register. The FILL operation will write the character in the CHARACTER register to every location in display memory starting with the address specified in the CURLO and CURHI registers through the location preceeding the address specified in the FILADD register. The cursor position is not changed after a FILL operation. Note that the address bits DA3-DA0 are internally forced to 0 forcing the FILADD address to be 00, 16, 32, etc. to 1920. The CURLO and CURHI registers will not be changed by this operation. Writing to the CHARACTER register will cause the VTLC to reset DB7 of the STATUS register to "0". Bit 7 will be set to 1 after the VTLC has filled the last memory location specified.

FILADD REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	DA10	DA9	DA8	DA7	DA6	DA5	DA4

ADDRESS								TYPE	REGISTER
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
X	X	X	X	0	1	1	0	Write	CHIP RESET
X	X	X	X	1	0	0	0	Write	TOSADD
X	X	X	X	1	0	0	1	Write	CURLO
X	X	X	X	1	0	1	0	Write	CURHI
X	X	X	X	1	0	1	1	Write	FILADD
X	X	X	X	1	1	0	0	Write	ATTDAT
X	X	X	X	1	1	0	1	RD/WR	CHARACTER
X	X	X	X	1	1	1	0	Write	MODE REGISTER

(X = don't care)

*NOTE: Chip Reset is required before starting operation.

TOSADD (Top of Screen Address) This register contains the RAM address of the first character displayed at the top of the video monitor screen. In addition, this register controls selection of either of two mask programmable vertical scan rates.

TOSADD REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
TIM	DA10	DA9	DA8	DA7	DA6	DA5	DA4

Note that address bits DA3-DAO are internally forced to 0 forcing the first address at the beginning of each row to be 00, 16, 32, etc. to 1920.

The most significant bit of this register (TIM) is used to select between the two mask programmed sets of vertical retrace parameters (scan A and scan B). This allows software selection of, for example, 50/60 HZ.

TIM = 0 enable raster scan A (60 Hz)
TIM = 1 enable raster scan B (50 Hz)

CURLO (Cursor Low) This register contains the eight lower order address bits of the RAM cursor address. All FILL screen and character transfer operations begin at the memory location pointed to by this address.

CURLO REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

CURHI (Cursor High) This register contains the three higher address bits of the RAM cursor address (DA10, DA9, DA8). All FILL screen and character transfer operations begin at the memory location pointed to by this address. In addition, this register contains the Smooth Scroll Offset Values SS3-SS0 which determine the number of scan lines that the data is shifted on the screen. The MSB of this register (SLE-status line enable) is the enable for the non-scrolling status line (this feature is available only on a part programmed for 25 data rows).

CURHI REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
SLE	SS3	SS2	SS1	SS0	DA10	DA9	DA8

SLE = 1 enables non-scrolling 25th status line
SLE = 0 disables and blanks non-scrolling status line

SS3-SS0 Smooth Scroll Offset Value

ATTDAT (Attribute Data) This register specifies the visual attributes of the video data and the cursor presentation. The visual attributes specified in the ATTDAT register (DB3-DB0) are enabled or disabled by a TAG bit that is appended to the ASCII character written to the CHARACTER register. Every character on the screen with its TAG bit set is displayed with the same attribute. Changing the Attribute register will change the attribute of every "tagged" character on the screen. The functions of the remaining bits in the ATTDAT register are not affected by the display character's TAG bit.

There are two display modes, "alphanumerics" and "graphics". In the alphanumeric mode, visual attributes may be selected by the TAG bit. In the graphics mode, a tagged character will be a normal alphanumeric character. This allows a screen to display a mix of graphic and alphanumeric characters or visually attributed alphanumeric characters. The display variations of the alphanumerics and graphics modes are summarized by the following:

ATTDAT REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

DB7	MODE SELECT	DB7 = 1	enables graphics mode display (No attributes allowed)
		DB7 = 0	enables alpha mode display
DB6	CURSOR SUPPRESS	DB6 = 1	inhibits VIDEO display at cursor time by forcing the VIDEO output to background level during cursor display time
		DB6 = 0	enables VIDEO display at cursor time Note: a blinking cursor display can be achieved by toggling this bit under processor control.
DB5	CURSOR DISPLAY	DB5 = 1	enables underline cursor display
		DB5 = 0	enables block cursor display Note: An underline cursor in an underline character attribute field will be dashed.
DB4	SCREEN	DB4 = 1	for white screen and black characters
		DB4 = 0	for black screen and white characters Note: this is a screen attribute (versus character attribute) bit and sets the default Video background level.

ENABLED OR DISABLED BY TAG BIT

DB3	CHARACTER SUPPRESS	DB3 = 1	to enable Video suppress
		DB3 = 0	to inhibit Video suppress This bit allows character blinking and blanking under processor control
DB2	INTENSITY	DB2 = 1	allows the INTOUT output pin to go high for the character time
		DB2 = 0	inhibits the INTOUT output pin from going high
DB1	UNDERLINE	DB1 = 1	will cause the character to be underlined
		DB1 = 0	will inhibit the underline
DB0	REVERSE VIDEO	DB0 = 1	will cause the standard foreground and background Video levels (selected with DB4) to be reversed for the character time
		DB0 = 0	will inhibit reverse video

MODE — The AUTO INCREMENT bit in this register specifies whether or not the display memory character address is automatically incremented by the VTLC after every read/write of the CHARACTER register. Note: The visible cursor position is not affected.

MODE REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
AUTO INC	X	X	X	X	X	X	X

DB7 AUTO INCREMENT — DB7 = 1 to enable automatic character address
The RAM address is incremented after the VTLC completes a display memory access initiated by a processor to RAM or RAM to processor character transfer.

DB7 = 0 to disable automatic increment

CHARACTER — This register allows access to the display memory for both byte transfers and FILL operations. In BYTE Transfer Write Mode, the processor first writes a character to this register. The VTLC takes that character and stores it in the display memory in the location specified by the CURLO and CURHI registers. In Byte Transfer Read Mode, the processor reads this register causing the VTLC to fetch the character whose address is specified in the CURLO and CURHI registers from the display memory and place it in the CHARACTER register. The processor then reads the character and initiates another fetch from memory cycle. In FILL mode, writing a byte to this register will initiate a FILL operation. All VTLC/memory data transfers take place during horizontal and vertical video retrace blank time.

CHARACTER REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
TAG BIT + 7 BIT ASCII CHARACTER							

CHARACTER SET

Using the DB7-DB0 data bus I/O pins and the MOD SEL bit in the ATTDAT register, the user can address 128 characters, a six segment "wide graphics" and a four segment "thin graphics" entity. Included in the 128 mask programmable characters can be the 96 standard ASCII characters and 32 special characters.

A. (MODE SEL = 1) GRAPHICS MODE

This mode allows an intermix of alpha-numeric and graphics characters. No attributes are permitted in this mode. If TAG BIT = 1, the character will be an alpha-numeric. If TAG BIT = 0, the character will be a graphics character.

CHARACTER REGISTER

ALPHANUMERIC: TAG BIT = 1

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
TAG = 1	← ALPHA-NUMERIC CHARACTER →						

DB6-DB0 Specify character

CHARACTER REGISTER

GRAPHICS: TAG BIT = 0

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
TAG=0	W/T	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1

DB6 — W/T = 1 specifies a wide graphics character
W/T = 0 specifies a thin graphics character

WIDE GRAPHICS ONLY:
DB5-4 SEG6-5 = 1 to turn on graphics entity segment
SEG6-5 = 0 to turn off graphics entity segment

Note that DB5 and DB4 have no meaning in the thin graphics entity.

SECTION V

WIDE AND THIN GRAPHICS:

DB3-0 SEG4-1 if any bit = 1, corresponding graphics entity segment ON

It any bit = 0, corresponding graphics entity segment OFF

B. (MOD SEL = 0) ALPHA-NUMERICS MODE

This mode allows display of alpha-numeric characters with attributes. If DB7 is set to a logical one, the attribute(s) specified in the ATTDAT register will be enabled for that character. If TAG BIT is cleared, attributes will not be enabled for that character.

CHARACTER REGISTER

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
TAG	⊢ ALPHA-NUMERIC CHARACTER ⊣						

DB7 = 1 to enable attribute(s) for character.
DB7 = 0 to disable attribute(s) for character.

DB6-DB0 Specify character

SEGMENT 6	SEGMENT 3
SEGMENT 5	SEGMENT 2
SEGMENT 4	SEGMENT 1

WIDE GRAPHICS ENTITY

NOTE: scan line and column of segment locations are mask programmable.

	SEGMENT 3
SEGMENT 4	SEGMENT 2 SEGMENT 1

THIN GRAPHICS ENTITY

NOTE: scan line and column of segment locations are mask programmable.

DESCRIPTION OF SYSTEM OPERATION

The VTLC circuitry provides two control functions. One function interprets and controls data from the system processor interface through the data bus DB7-DB0 as shown in the Processor Timing of figure 3. The other function generates and refreshes the video image on the screen through the DD7-DD0 data bus as shown in the Display Memory Timing of figure 2. Because the system data bus is isolated from the display data bus, the VTLC maintains complete control over access to display memory. All data flow between display RAM and the processor or the VTLC takes place through the VTLC. Refer to the VTLC Display Memory Access Timing of figure 7.

DISPLAY MEMORY ACCESS

Processor/display memory access is accomplished through the CHARACTER register of the VTLC. All processor transfers to or from the CHARACTER register take place only when the DONE bit is high. The DONE bit is used to synchronize data transfers between the VTLC and the processor as shown in the Typical Processor To Display Memory Transfer of figure 6. When the processor needs to store a byte of data in the display memory, it will write the byte to the CHARACTER register of the VTLC. The VTLC will immediately reset the DONE bit indicating that the transfer hardware is busy. At the next blanked Video time, the VTLC will store the byte in the display memory, increment the character address, (if auto increment is enabled) and set the DONE bit. When the processor needs to read a byte of data from the display memory, it will read the CHARACTER register. The VTLC will fetch the desired byte from the display memory during the next blanked VIDEO time, increment the character address (if enabled), and set the DONE bit. When the processor detects that the DONE bit is set, it will read the CHARACTER register to get the data byte from the VTLC. This read will reset the DONE bit and cause the VTLC to fetch the next byte of data from the memory.

If auto increment is not enabled, the processor must set the cursor address in the CURLO and CURHI register to the address of the memory location being read from, or written into, before every access to the CHARACTER register.

It should be noted that Auto Increment does not affect the visible cursor location. If auto-increment is enabled, the current character location will equal the cursor position only for the first character transfered following an update of the CURLO and CURHI registers. Note that the DONE bit must be high before attempting to update the cursor registers because the loading of the cursor registers will reset the character position counters to the cursor position.

SMOOTH SCROLL

The VTLC may be programmed to do either "jump" or "smooth" scrolling. Jump scrolling moves the data up or down the monitor screen one data row at a time. Smooth scrolling moves the data up the monitor screen one scan line at a time. The number of scan lines and the rate they move up the screen is under processor control.

Smooth scroll is controlled through manipulation of the SS3-SS0 bits of the CURHI register. These bits represent the binary address of the first scan line of the first data row displayed on the monitor screen (the data row whose beginning address is in the TOSADD register). When the value represented by these bits is incremented, the video data on the monitor screen moves up by the same number of scan lines. After the address of the last scan line of the data row is loaded into the CURHI register and the VIDEO data has moved up the last scan line of the data row, the processor resets the SS3-SS0 address to point to scan line

0 and does a jump scroll. Jump scroll is accomplished by incrementing the RAM address in the TOSADD register by a data row length (so that it points to the address of the first character of the new top data row on the monitor).

When programmed for a data row of 80 characters/data row display (1920 data words), for example, the display RAM contains 25 actual rows of data (2000 RAM locations). If the smooth scroll offset equals zero, the VTLC will display the 1919 RAM locations following the top of screen address when displaying data. The first data row is partially scrolled off the screen and the 25th data row is scrolled onto the screen when the smooth scroll offset is incremented. The VTLC will now display the 1999 RAM locations following the top of screen address (wrapping to 0 after address 1999). After the VTLC does a jump scroll, the processor will program it to erase the line just scrolled off the screen (preparing it to be scrolled onto the screen). This line now becomes the non-displayed 25th data row.

NON-SCROLLING STATUS LINE

The non-scrolling status line is only functional on a VTLC that has been programmed for 25 data rows. This data row will remain stationary at the bottom of the screen and will not move up the screen when the remainder of the display data is scrolled. Otherwise, VIDEO data on the status line may be manipulated as though it were normal display data. The smooth scroll offset will not function properly when the status line is enabled. The memory address of the characters on the status line are always characters 1920–1999.
NOTE: If the part is programmed for 25 data rows an additional mask option must be specified which makes the 25th data row either fixed (always displayed) or a status row (enabled/disabled by the SLE bit).

CHIP RESET

The CRT 9028 and CRT 9128 Chip Reset requires two steps. The system processor first writes the reset address to the address register of the VTLC. The system processor then writes a dummy character to the VTLC Data register. Writing to the Data register resets the chip. The only state affected by the reset function is the setting of the DONE bit in the STATUS register.

ROM CHARACTER BLOCK FORMAT

COLUMN DOT ->	C7	C6	C5	C4	C3	C2	C1	C0
SCAN LINE 0 ->	0	0	0	0	0	0	0	0
SCAN LINE 1 ->	0						0	0
SCAN LINE 2 ->	0						0	0
SCAN LINE 3 ->	0			MASK PROGRAMMABLE			0	0
SCAN LINE 4 ->	0			CHARACTER BLOCK (FONT) 5 X 8			0	0
SCAN LINE 5 ->	0						0	0
SCAN LINE 6 ->	0						0	0
SCAN LINE 7 ->	0						0	0
SCAN LINE 8 ->	0						0	0
SCAN LINE 9 ->	0	0	0	0	0	0	0	0
SCAN LINE 10 ->	0	0	0	0	0	0	0	0
SCAN LINE 11 ->	0	0	0	0	0	0	0	0

Mask programmable options–The ROM character block format above shows the 5X8 mask programmable character font within the character cell as defined by dots C7 through C0 and scan lines 0 through 11.

Dots/Character: 6 dots/character cell = > C7 - C2 displayed
7 dots/character cell = > C7 - C1 displayed
8 dots/character cell = > C7 - C0 displayed

Column dots C0 and C1 will be the same as column dot C7 when more than 6 dots/character cell are specified when generating alpha-numerics.

NOTE: The maximum dot clock crystal frequency is dependent on the dots/character programmed:

DOTS/CHARACTER	MAX XTAL FREQ
6 dots	10.5 MHz max*
7 dots	12.25 MHz max*
8 dots	14.0 MHz max*

*These values are preliminary

Scan Lines per Character: 8 scan lines/character = > SL0 - SL7 displayed
9 scan lines/character = > SL0 - SL8 displayed
10 scan lines/character = > SL0 - SL9 displayed
11 scan lines/character = > SL0 - SL10 displayed
12 scan lines/character = > SL0 - SL11 displayed

Thin and Wide Graphics: Dots mask programmed for vertical column C2 will be the same as backfill Columns 0 and 1 when generating wide and thin graphics.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (TA = 0°C to 70°C, V_{cc} = +5V ±5%, unless otherwise noted.)

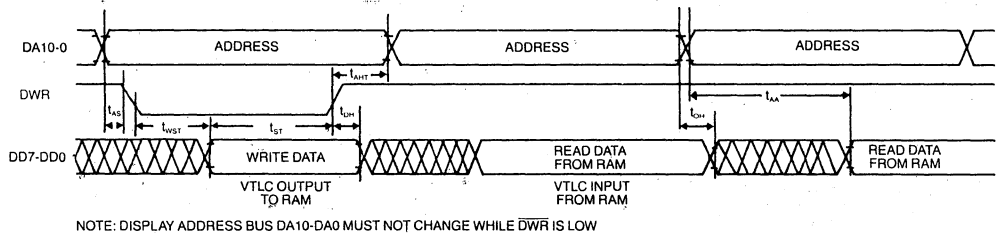
PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, Vil			0.8	V	
High-Level, Vih	2.2			V	
OUTPUT VOLTAGE LEVELS					
Low-level, Vol			0.4	V	All outputs except $\overline{VIDEO}$, CSYNC, INTOUT, HSYNC, VSYNC; Iol = 1.6 mA
Low-level, Vol			0.4	V	$\overline{VIDEO}$, CSYNC, INTOUT, HSYNC, VSYNC; Iol = 0.4 mA
High-level, Voh	2.4			V	All outputs except $\overline{VIDEO}$, CSYNC, INTOUT, HSYNC, VSYNC; Ioh = −40 µA
High-level, Voh	2.4			V	$\overline{VIDEO}$, CSYNC, INTOUT, HSYNC, VSYNC; Ioh = −20 µA
INPUT LEAKAGE CURRENT					
High-level, Ilh			10	µA	All inputs; Vin = Vcc
Low-level, Iil			−10	µA	All inputs except $\overline{WR}$, $\overline{RD}$, $\overline{DS}$, R/$\overline{W}$; Vin = .04V
Low-level, Iil			−200	µA	$\overline{WR}$, $\overline{RD}$, $\overline{DS}$, R/$\overline{W}$; Vin = 0.4V
INPUT CAPACITANCE					
All inputs, Cin			15	pF	
OUTPUT LOAD					
C_L			15	pF	Except DB7-0
C_L			100	pF	DB7-0
POWER SUPPLY CURRENT					
Icc		125		mA	
AC CHARACTERISTICS					
CLOCK FREQUENCY, fin	1.0		14.0	MHz	
DISPLAY MEMORY TIMING					
Address Set-up Time					
t_{AS}	20			ns	
Write Strobe Set-up Time					
t_{WST}	80			ns	
Data Set-up Time					
t_{ST}	80			ns	
Data Hold Time					
t_{DH}	10		25	ns	

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Address Hold Time t_{AHT}	25			ns	
Output Hold From Address Change t_{OH}	15			ns	
Address Access Time t_{AA}			250	ns	
PROCESSOR TIMING					
Address Read/Write Set-up t_{ARWS}	160			ns	
Write Pulse Width t_{WPW}	160			ns	
Write Hold Time t_{WHT}	15			ns	
Read Set-up Time t_{RST}			200	ns	
Read Data Valid T_{RDV}	0			ns	
Read Pulse Width t_{RPW}	250			ns	
Data Write Falling Set-up t_{DWFS}	120			ns	
Data Write Rising Set-up t_{DWRS}	160			ns	

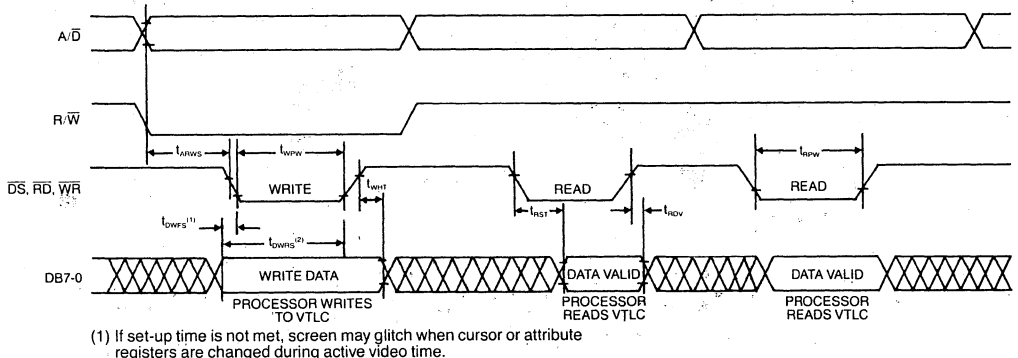
Crystal specification (Applies for 4-14 MHz):

Series Resonant
50 ohms max series resistance
1.5 pf typ parallel capacitance
Operation below 4 MHz requires external crystal oscillator



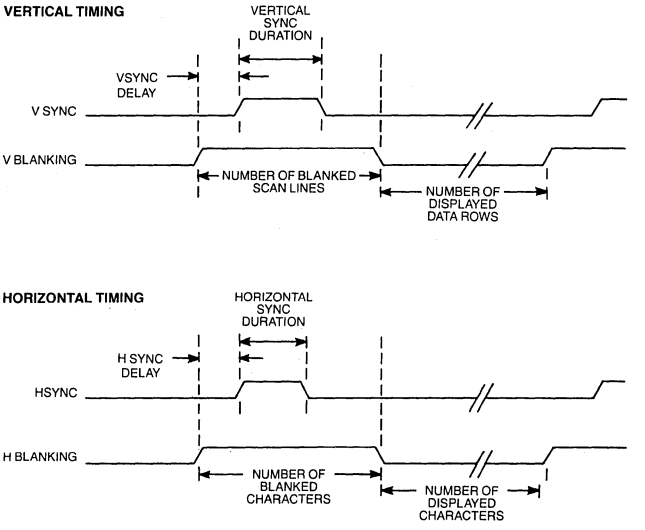
NOTE: DISPLAY ADDRESS BUS DA10-DA0 MUST NOT CHANGE WHILE $\overline{DWR}$ IS LOW

FIGURE 2. DISPLAY MEMORY TIMING



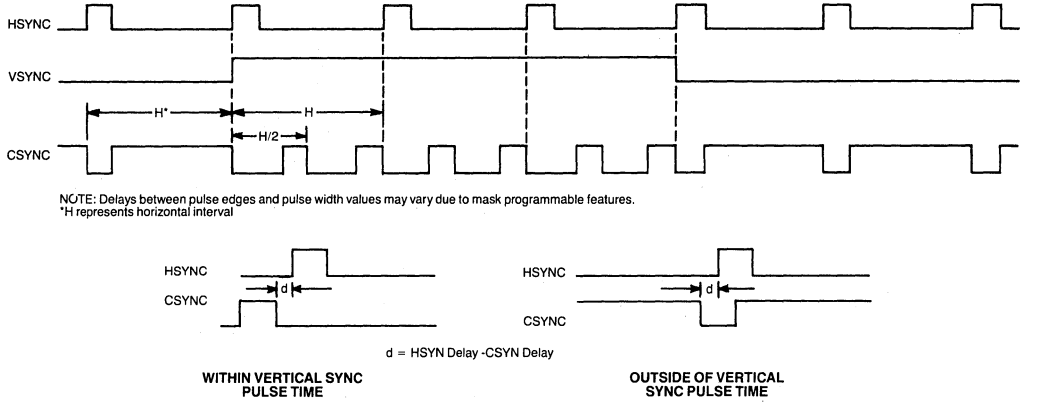
(1) If set-up time is not met, screen may glitch when cursor or attribute registers are changed during active video time.
(2) Minimum set-up time to ensure valid data into VTLC internal registers.

FIGURE 3. PROCESSOR TIMING



NOTE: Video parameters above are mask programmable

FIGURE 4. VERTICAL AND HORIZONTAL SYNC TIMING



NOTE: Delays between pulse edges and pulse width values may vary due to mask programmable features.
*H represents horizontal interval

FIGURE 5. VIDEO SIGNAL TIMING

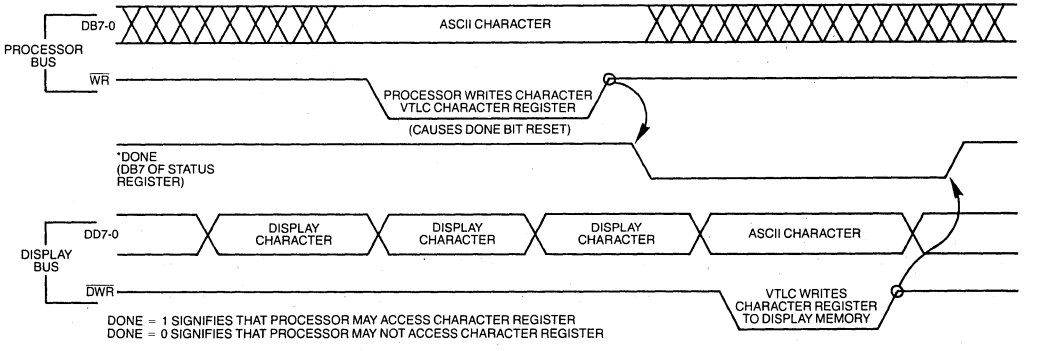


FIGURE 6. TYPICAL PROCESSOR TO DISPLAY MEMORY TRANSFER

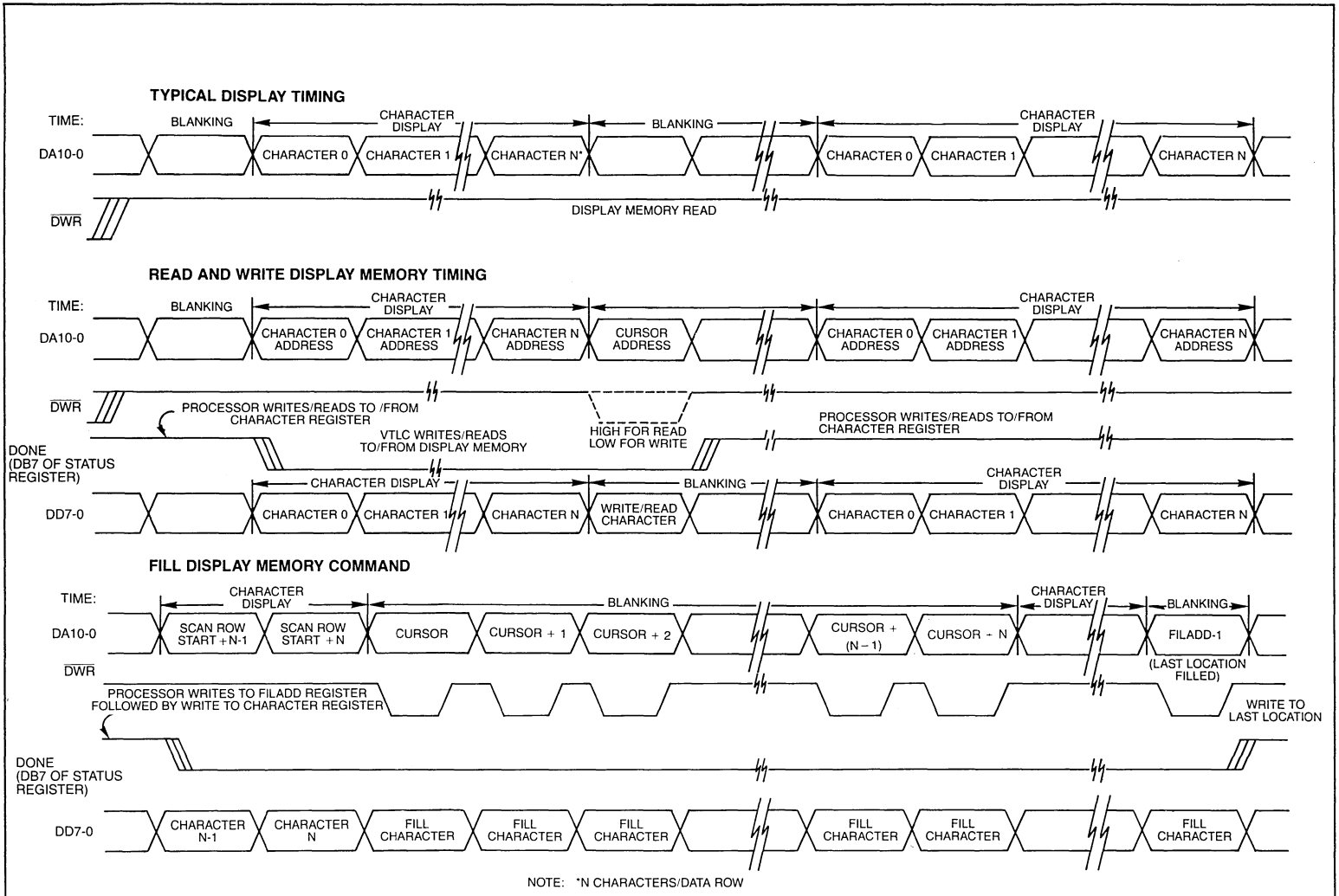


FIGURE 7. VTLC DISPLAY MEMORY ACCESS TIMING

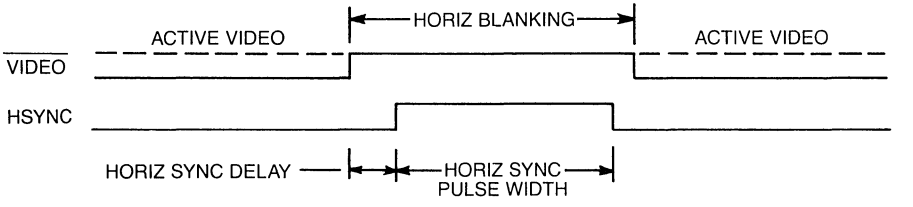
I. ROM CHARACTER BLOCK FORMAT:

COLUMN DOT	C7	C6	C5	C4	C3	C2	C1
SCAN LINE 0	0	0	0	0	0	0	0
SCAN LINE 1	0						0
SCAN LINE 2	0						0
SCAN LINE 3	0		CHARACTER BLOCK 5 X 8 CELL				0
SCAN LINE 4	0						0
SCAN LINE 5	0						0
SCAN LINE 6	0						0
SCAN LINE 7	0						0
SCAN LINE 8	0						0
SCAN LINE 9	0	0	0	0	0	0	0

DOTS PER CHARACTER: 7
DOT CLOCK XTAL FREQUENCY (MHz): 10.92

II. HORIZONTAL TIMING (IN CHARACTER TIMES):

CHARACTERS PER DATA ROW: 80
HORIZONTAL BLANKING: 20
HORIZONTAL SYNC DELAY: 4
HORIZONTAL SYNC PULSE WIDTH: 8
HORIZONTAL SYNC POLARITY: NEGATIVE ACTIVE

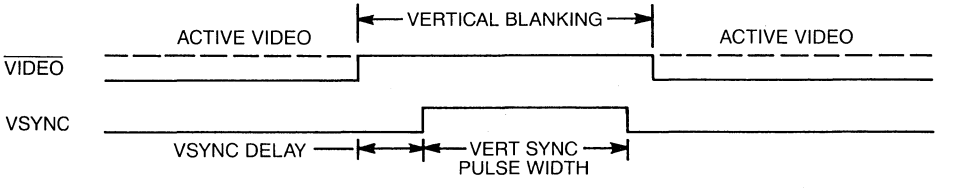


III. VERTICAL TIMING:

CHARACTER ROWS: 24
SCAN LINES PER CHARACTER: x 10
TOTAL VISIBLE SCAN LINES: 240
VERTICAL SYNC POLARITY: NEGATIVE ACTIVE

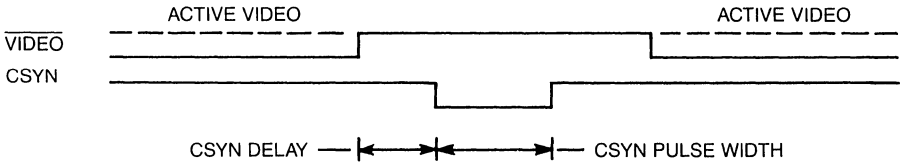
IV. VERTICAL SYNC TIMING (IN SCAN LINES):

60 Hz VERTICAL BLANKING: 20
60 Hz VERTICAL SYNC DELAY: 4
60 Hz VERTICAL SYNC PULSE WIDTH: 8
ALTERNATE (50 Hz) VERTICAL BLANKING: 72
ALTERNATE (50 Hz) VERTICAL SYNC DELAY: 30
ALTERNATE (50 Hz) VERTICAL SYNC PULSE WIDTH: 10



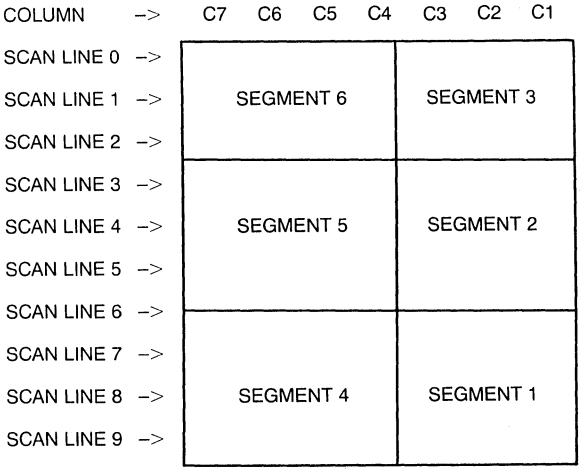
V. COMPOSITE SYNC OUTPUT (IN CHARACTER TIMES):

COMPOSITE SYNC DELAY: 2
COMPOSITE SYNC PULSE WIDTH: 8

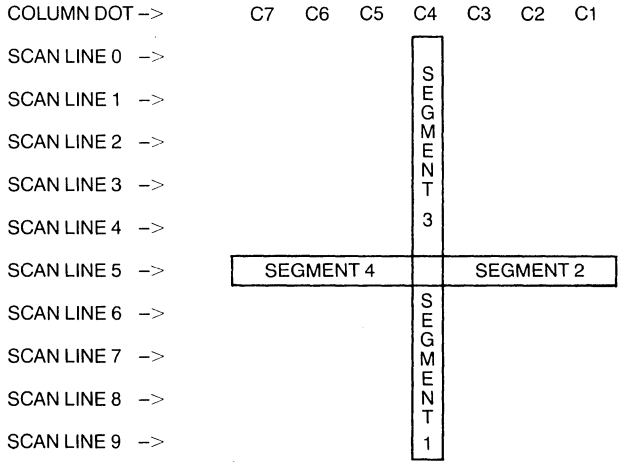


VI. UNDERLINE ATTRIBUTE AND CURSOR LINE: SCAN LINE 9

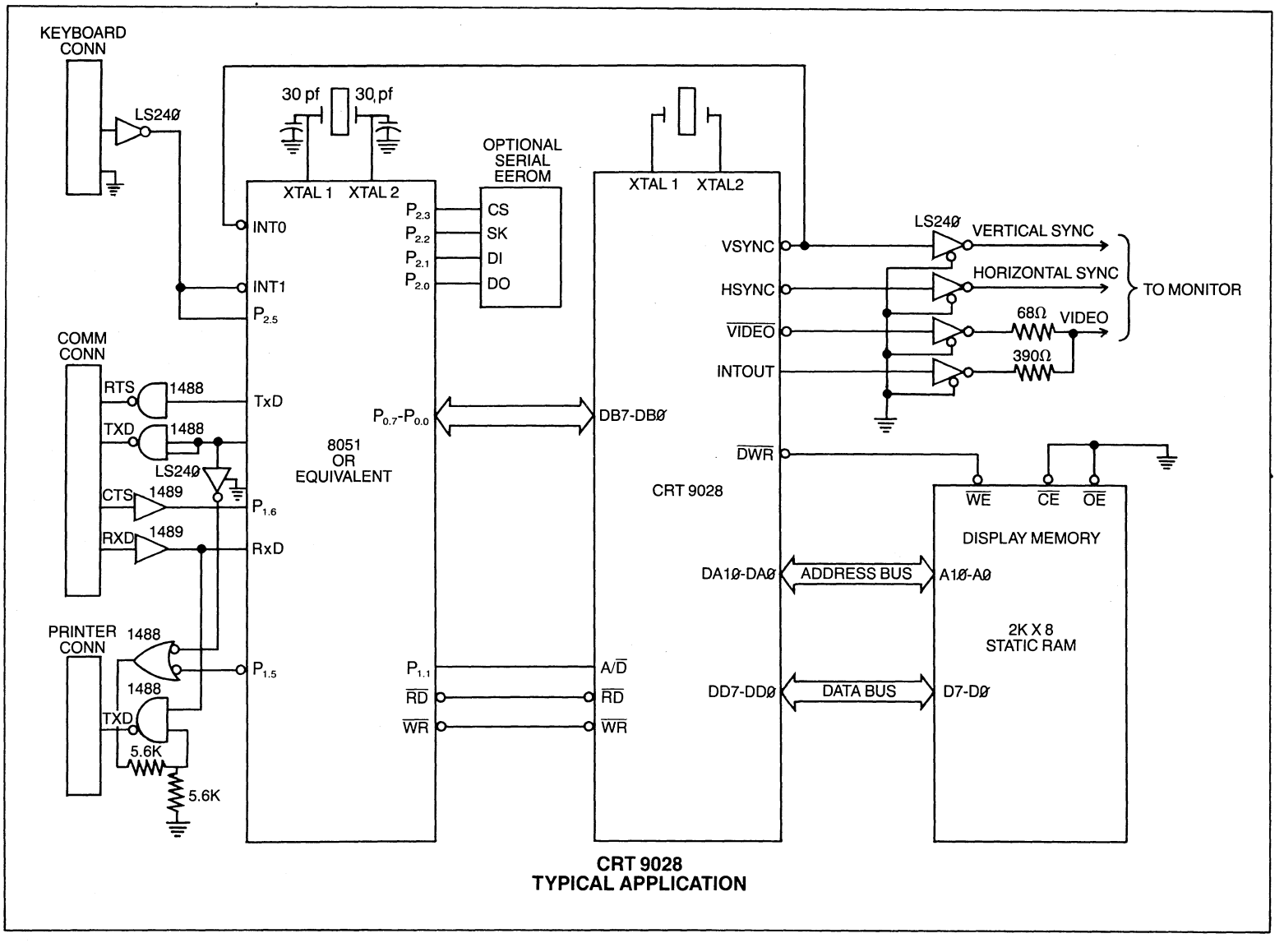
VII. WIDE GRAPHICS FIGURE DEFINITION:



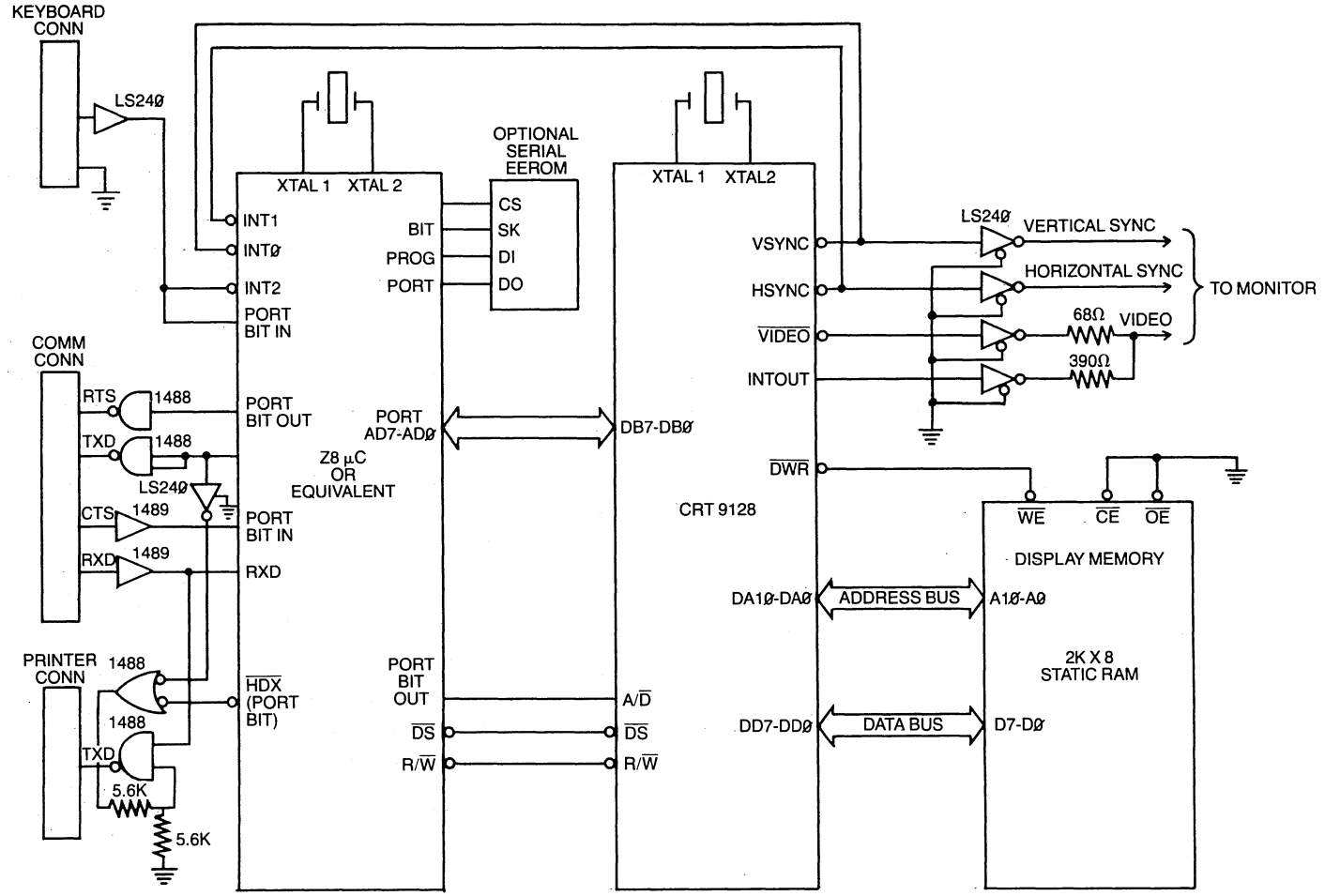
VIII. THIN GRAPHICS FIGURE DEFINITION:



SEGMENT 4 = SCAN LINE 5; C7, C6, C5, C4
SEGMENT 3 = C4; SCAN LINES 0, 1, 2, 3, 4, 5
SEGMENT 2 = SCAN LINE 5; C4, C3, C2, C1
SEGMENT 1 = C4; SCAN LINES 5, 6, 7, 8, 9



CRT 9028
TYPICAL APPLICATION



CRT 9128
TYPICAL APPLICATION

CRT 9028/9128-000

DD6...DD4 \ DD3...DD0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2	C6-2
000	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL
001	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL
010	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL
011	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL
100	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL
101	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL
110	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL
111	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL	SL

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