SGS-THOMSON MICROELECTRONICS

AN624 APPLICATION NOTE

SERIAL EEPROM MEMORY COMPATIBLE WITH THE PLUG&PLAY VESA DISPLAY DATA CHANNEL 1.0

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INTRODUCTION

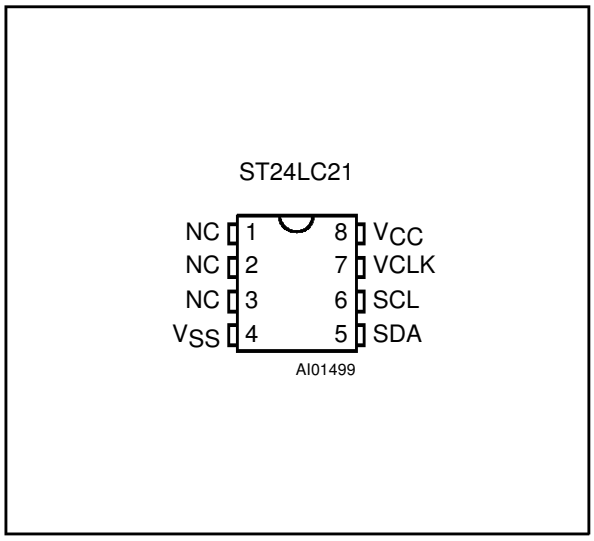
The SGS-THOMSON ST24LC21 serial EEPROM memory has been designed to meet the Vesa Data Display Channel specification Version 1.0 (V.D.D.C) for the Plug&Play PC monitors market. The ST24LC21 is a 1K bit Application Specific Memory (A.S.M) EEPROM organized by 128 x 8 bits. It is fully compatible with V.D.D.C modes DDC1 (1) and DDC2B (2). When installed in a PC monitor, the ST24LC21 can work in DDC1 mode using only a 2 wire bus or in both DDC1 and DDC2B modes using a 3 wire bus to be fully DDC-compliant.

The ST24LC21 allows a direct connection from the PC monitor to the PC Host computer, with a suitable graphics card, using the standard Video cable, which simplifies the design of the application.

The ST24LC21 has a standard I2C interface, including SCL and SDA lines, plus an additional clock input, VCLK, specific to the V.D.D.C. specification. This additional clock input allows the PC host-computer to receive, from the monitor, all information required to configure the video card and the monitor's software driver.

The serial communication of the ST24LC21 can run at 400kHz in both DDC1 and DDC2B modes with a supply voltage from 2.5V to 5.5V. The ST24LC21 is available in an 8 pin PDIP and SO packages.

Figure 1. ST24LC21 Pin Connections



ST24LC21 DESCRIPTION

The ST24LC21 device can operate in two modes which correspond to the two V.D.D.C. specification modes. The Transmit Only mode of the ST24LC21 corresponds to the V.D.D.C. DDC1 mode and the I2C bi-directional mode to the DDC2B mode.

When first powered, the ST24LC21 is in Transmit Only mode. In this mode, the EEPROM data is clocked out on the rising edge of the signal applied on VCLK.

The ST24LC21 will switch to the I2C bi-directional mode upon the falling edge of the signal applied on the SCL pin. The ST24LC21 cannot switch from the I2C bi-directional mode to the Transmit Only mode (except when the power supply is removed).

1. *DDC1: a uni-directional data channel from the display to the Host, continuously transmitting Extended Display Identification, EDID, information.*
2. *DDC2B: a bi-directional data channel based on the I2C protocol. The Host can request Extended Display Identification information, EDID, or Video Display Interface information, VDIF, over the DDC2 channel. In addition to this, the DDC2 channel can act as a transparent channel for ACCESS.bus communication.*

DDC1 TRANSMIT ONLY MODE

After a Power-up, the ST24LC21 is in the Transmit Only mode. In this mode, the ST24LC21 uses the VCLK input as a clock and the SDA line as DATA OUTPUT (see Figure 2). The SCL input must be held high.

A proper initialization sequence (see Figure 3) must supply nine clock pulses on the VCLK pin (in order to internally synchronize the device). During this initialization sequence, the SDA pin is in the high impedance state. On the rising edge of the tenth pulse applied on VCLK pin, the device will output the first bit of the byte located at address 00h (most significant bit first).

For the ST24LC21 in DDC1/transmit only mode, a data byte is clocked out (on the SDA pin) with nine clock pulses on VCLK: 8 clock pulses for the data byte and one extra clock pulse for a Don't Care bit (see Figure 3). Note that this last data bit should be read at 1 due to the pull-up resistor on the SDA line. If not, the memory will be de-synchronized and the data will not be valid. It is then necessary to re-syn-

Figure 2. ST24LC21 in DCC1 Mode

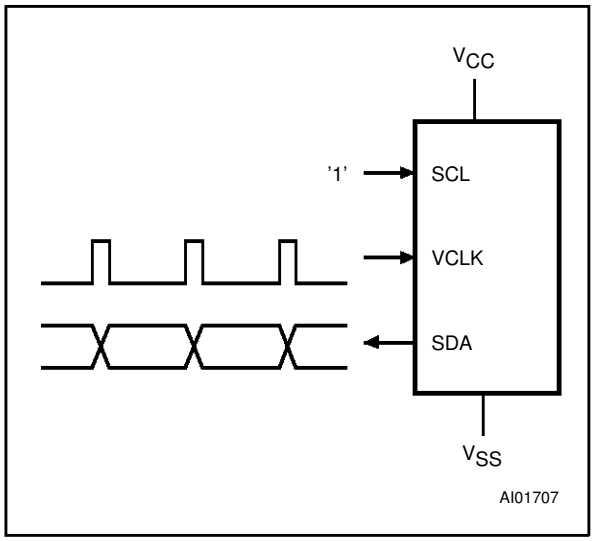
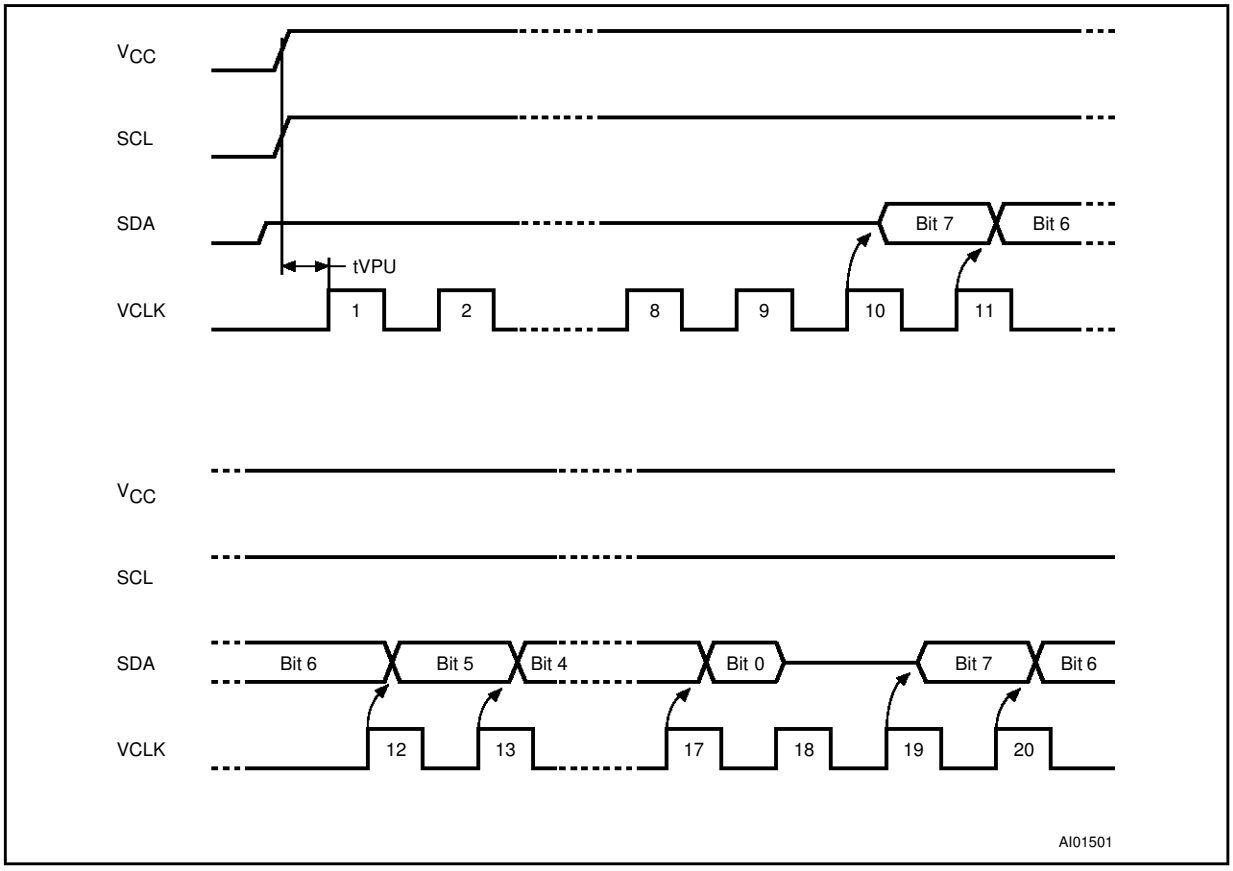


Figure 3. DDC1 Transmit Only Mode Waveforms



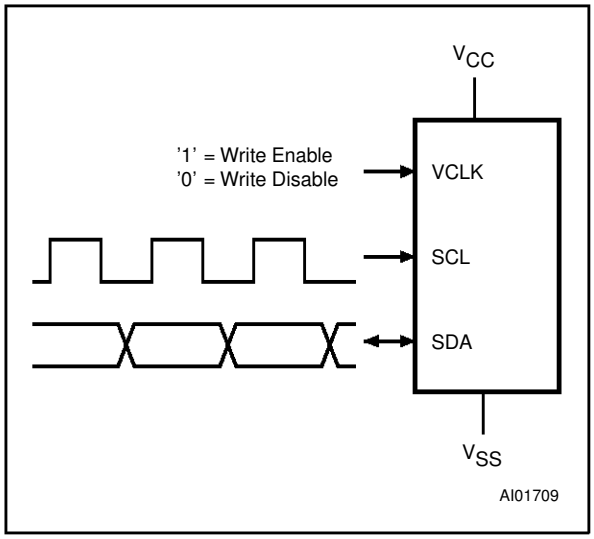
chronize the communication by powering OFF and ON the memory or by checking a synchronization block of data written in the ST24LC21. In DDC1 mode, there is no instruction or command needed on the bus and it is impossible to write any data using the VCLK clock. The ST24LC21 only allows you to read continuously its 128 data bytes.

As long as the SCL pin is held high, each byte of the memory array is transmitted serially on SDA pin with an automatic address increment. When the last data byte is transmitted, the address counter will roll back to location 00h.

DDC2 I²C BI-DIRECTIONAL MODE

The device can be switched from Transmit Only mode (DDC1) to I²C Bi-directional mode (DDC2B) by applying a valid high to low transition on the SCL pin (see Figure 5). When the device is in the I²C Bi-directional mode, the VCLK input enables (or inhibits) the execution of any write instruction: if VCLK=1, write instructions are executed; if VCLK=0 write instructions are not executed. The device is compatible with the I2C standard two wire serial interface which uses a bi-directional data line (SDA) and a serial clock (SCL). The device carries a built-in 4 bit unique device identification code (1010) corresponding to the I²C bus definition device code.

Figure 4. ST24LC21 in DCC2B Mode



The ST24LC21 behaves as a slave device in the I²C protocol with all memory operations synchronized by the serial clock SCL. Read and write operations are initiated by a START condition generated by the bus master (Table 2). The START condition is followed by a stream of 7 bits (Table 1), plus one read/write control bit and is terminated by an acknowledge bit.

When the bus master writes data to the memory, the ST24LC21 responds to the 8 received data bits by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it must acknowledge the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Figure 5. Transition from Transmit Only (DDC1) to Bi-directional (DDC2B) Mode Waveforms

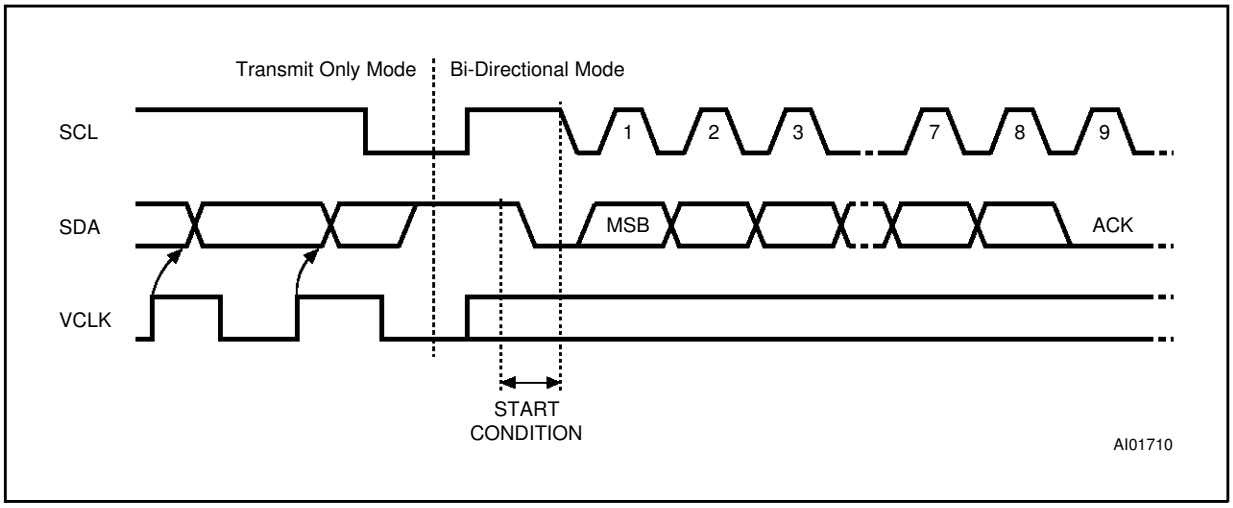


Table 1. Device Select Code in Bi-directional Mode

	Device Code				Chip Enable			R$\overline{W}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	X	X	X	R$\overline{W}$

Note: The MSB b7 is sent first.
X = 0 or 1.

Table 2. Operating Modes

Mode	R$\overline{W}$ bit	VCLK	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, R$\overline{W}$ = '1'
Random Address Read	'0'	X	1	START, Device Select, R$\overline{W}$ = '0', Address,
	'1'	X		reSTART, Device Select, R$\overline{W}$ = '1'
Sequential Read	'1'	X	1 to 128	Similar to Current or Random Mode
Byte Write	'0'	V_{IH}	1	START, Device Select, R$\overline{W}$ = '0'
Page Write	'0'	V_{IH}	8	START, Device Select, R$\overline{W}$ = '0'

Note: X = V_{IH} or V_{IL}

NOTE CONCERNING THE CONTROL OF THE WRITE MODES

An hardware Control of the Write modes is offered for the ST24LC21 on pin 7 when the device is in bi-directional mode. The functionality of pin 7 switches from the VCLK clock input in the transmit-only mode to a write control input in the Bi-directional mode.

This feature is useful to protect the contents of the memory from any erroneous erase/write cycles. The write control signal is used to enable (VCLK at V_{IH}) or disable (VCLK at V_{IL}) the execution of the write instruction.

For a valid WRITE instruction, the voltage level applied on the VCLK input must be higher than V_{IH} as shown in Figure 6. The level at VCLK must be high before reaching the START condition and stay in that state until after the STOP condition has been met.

Any write command with VCLK = 0 will not modify data but will be Acknowledged on data bytes, as shown in Figure 7.

This write control feature has been designed to check and to memorize any trouble on the VCLK input during a Byte Write or a Page Write sequence. This means that if there is a negative noise glitch on the VCLK input, the internal logic will automatically protect the memory area and the incoming Write instruction will not be executed. By this way, you can be sure that there will not be data corruption at a random address: It is preferable to have no write cycle rather than random address data modification.

Figure 6. Writes Modes Sequence

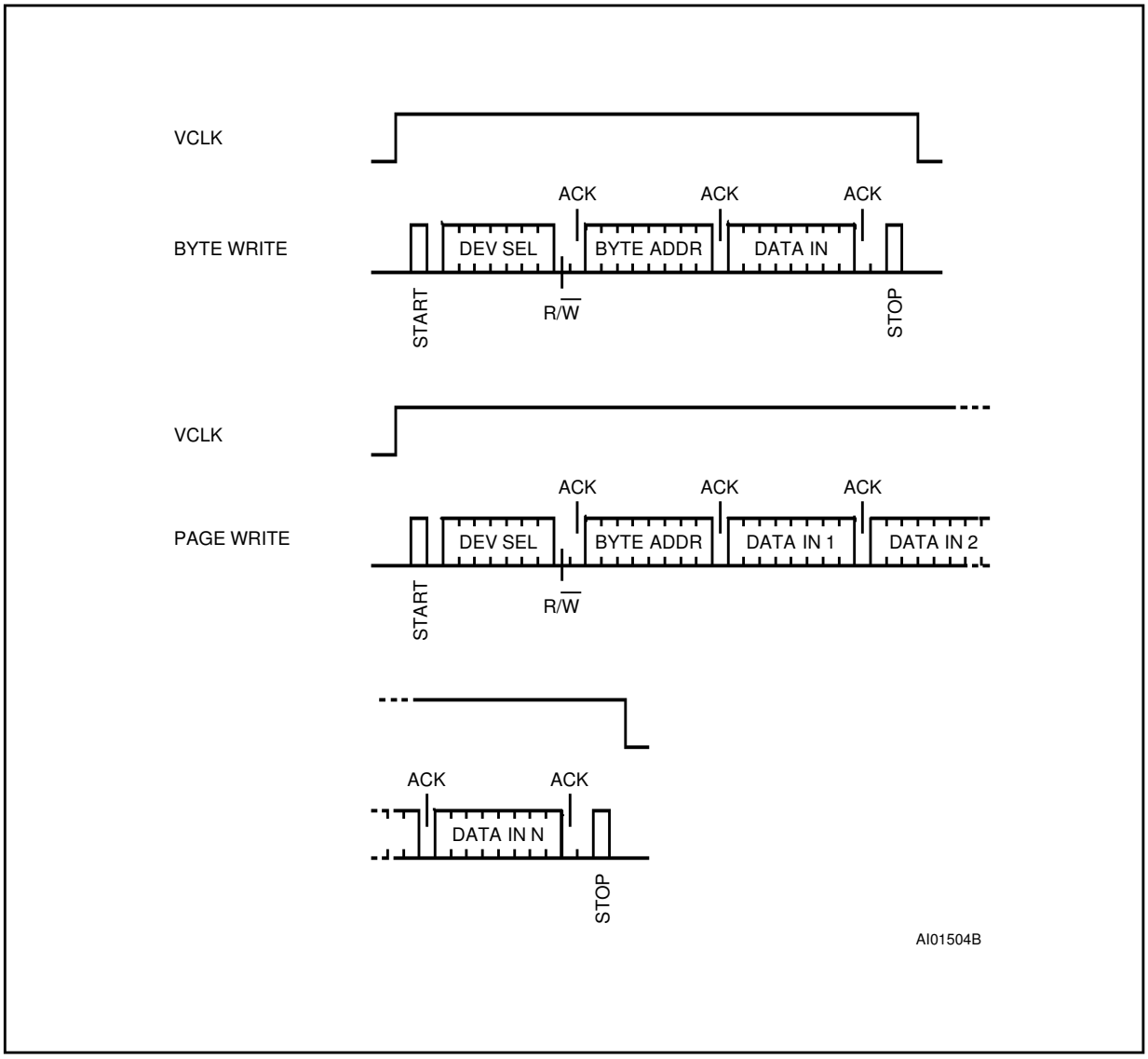
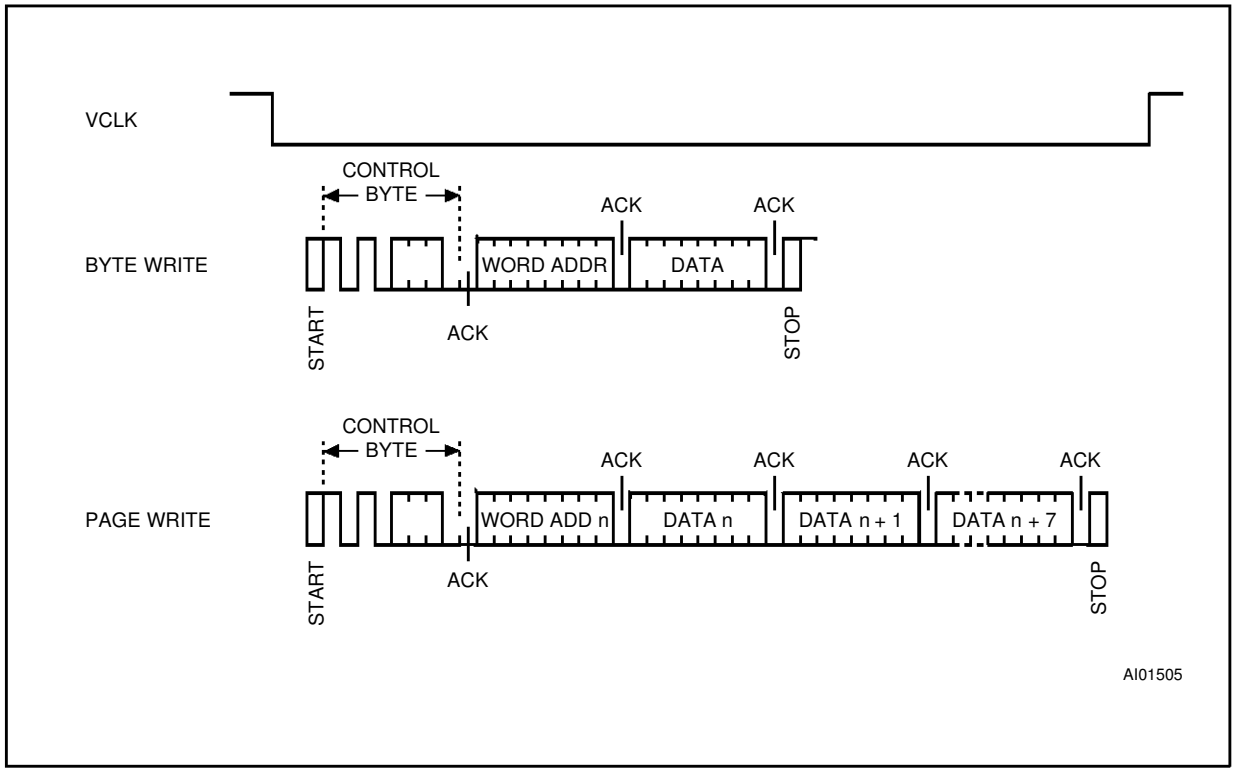


Figure 7. Inhibited Write when VCLK = 0



TYPICAL ST24LC21 APPLICATION SCHEMATIC

The ST24LC21 is used in a Plug&Play PC monitor to transmit all the display information needed by the host in DDC1 or DDC2B mode. The display capabilities are retrieved by the system software during boot-up and configuration. During this data retrieval, the display can provide the system unit information about its capabilities.

The mechanical connector specification for the Display to Host graphic controller is backward compatible to the standard 15 pin, VGA-type, connector. The VGA pin-out connector is described in Table 3. You will notice that the Host and the Display pin-out connections are different, depending on the V.D.D.C. mode available in the host graphic controller.

Referring to the VESA Data Display Channel specification, the Host graphic controller board needs to provide 15k ohm pull-up resistors on the Bi-directional data (SDA) and on the data clock (SCL) lines. With this configuration, the ST24LC21 in the PC monitor can be accessed in either DDC1 or DDC2B mode.

The display PCB board just needs to provide a 47k ohm pull-up resistor on the data clock line.

According to the VGA pin-out connection for a VGA display, a PC monitor application schematic which use a ST24LC21 could be as shown in Figure 8.

The VESA Plug&Play specification defines 4 pins of the VGA connector.

The Transmit-only clock signal VCLK is connected to pin 14 of the VGA connector, the Data clock line (SCL) used for the bi-directional mode is connected to pin 15 and the Data line (SDA) is connected to pin 12.

Table 3. 15 pin VGA Connector Pin-out Description

Pin	Standard VGA	DDC1 Host	DDC2 Host	DDC1/2 Display
1	Red Video	Red Video	Red Video	Red Video
2	Green Video	Green Video	Green Video	Green Video
3	Blue Video	Blue Video	Blue Video	Blue Video
4	Monitor ID bit 2	Monitor ID bit 2	Monitor ID bit 2	Optional
5	Test (ground)	Return	Return	Return
6	Red Video Return	Red Video Return	Red Video Return	Red Video Return
7	Green Video Return	Green Video Return	Green Video Return	Green Video Return
8	Blue Video Return	Blue Video Return	Blue Video Return	Blue Video Return
9	No Connection (mechanical key)	5V Supply (Optional)	5V Supply (Optional)	5V Supply (Optional)
10	Sync Return	Sync Return	Sync Return	Sync Return
11	Monitor ID bit 0	Monitor ID bit 0	Monitor ID bit 0	Optional
12	Monitor ID bit 1	Data from Display	Bi-directional Data (SDA)	Bi-directional Data (SDA)
13	Horizontal Sync	Horizontal Sync	Horizontal Sync	Horizontal Sync
14	Vertical Sync	Vertical Sync (VCLK Output)	Vertical Sync	Vertical Sync (VCLK Input)
15	Monitor ID bit 3	Monitor ID bit 3	Data Clock (SCL)	Data Clock (SCL)

An optional +5V supply voltage generated by the Host can be available on the pin 9 of the VGA connector (used for the ACCESS.bus™ protocol). This +5V supply voltage may be used to supply the Vcc voltage of the ST24LC21. This will allow a proper power-up sequence driven only by the Host. If the Host and the monitor are powered-on asynchronously, noise on the lines may trigger improper configuration of the whole system.

The SCL (Bi-directional clock) and SDA (Data) pins of the ST24LC21 can be directly connected to the VGA connector. An ESDA6V1 transil array may be used in order to improve the memory protection against ESD and latch-up.

The VCLK (Transmit-only clock) pin of the ST24LC21 can also be directly connected to the VGA connector with the same diode protection. However, it is recommended to use the internal VSync signal available in the monitor as it is important for a good use of the ST24LC21 to have good transitions on its VCLK input with a rise and fall time of 1µs Max. On a normal application, VSync could have slow rise and fall times or bounces on edges and the ST24LC21 will output more than one data bit.

Figure 8. PC Monitor Application Schematic