Panasonic

ideas for life

2010

Microcomputer Family

AM Series

8-bit AM1 Series

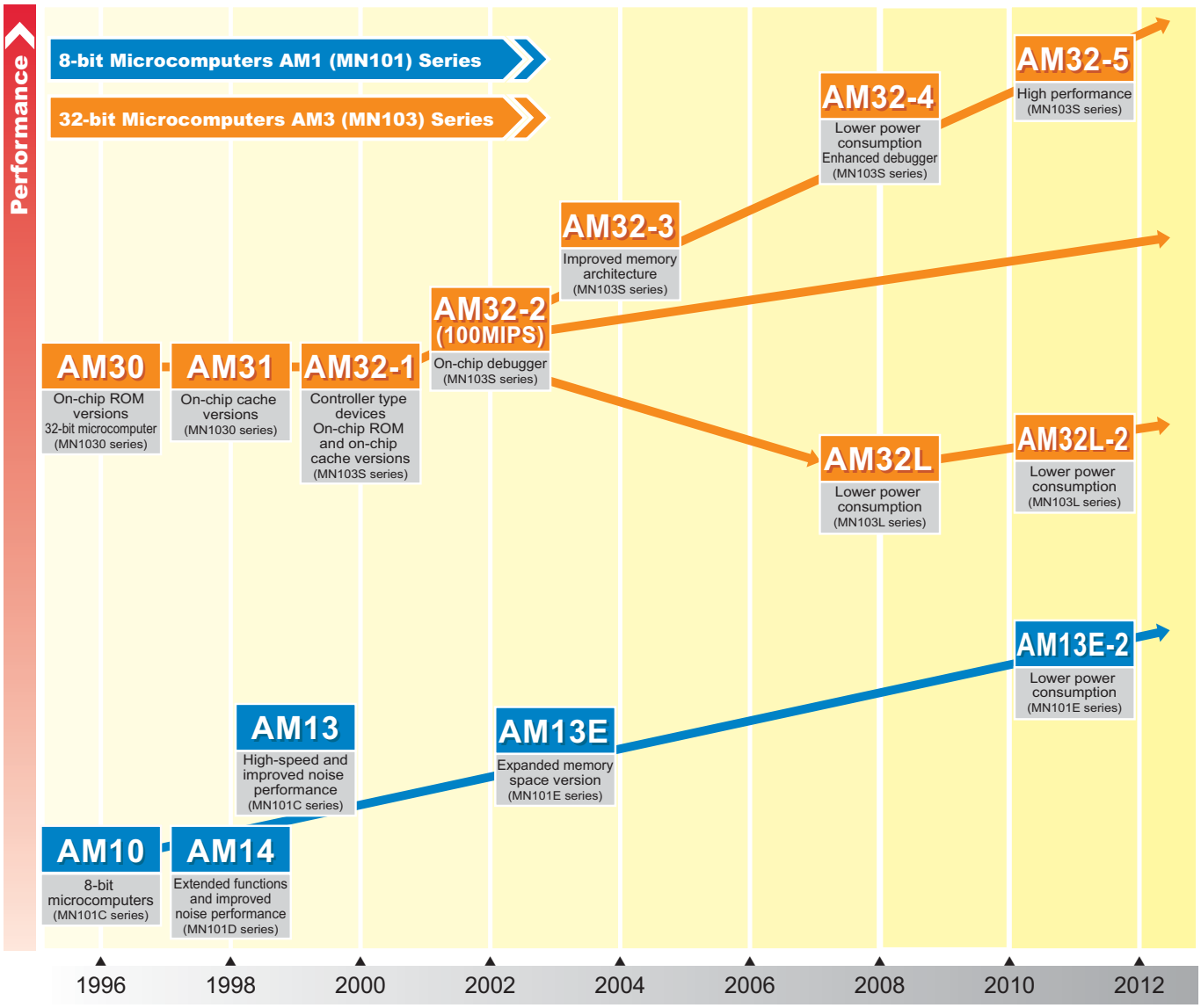
32-bit AM3 Series

Delivers Improved Performance and Cost Savings

Unified Microcomputer Architecture

Common architecture shared by 8- and 32-bit models

The products of a rigorous analysis of embedded device software and system needs, the Panasonic AM1 (MN101) and AM3 (MN103) Series signal a new concept in microcomputer design.
With 8- and 32-bit models that share a unified architecture, these microcomputers combine high performance with low power consumption in a package that supports C-language programming for a fast, efficient development cycle. They feature a single development environment and are suitable for a wide range of applications, including high-performance embedded controllers and key devices in multimedia hardware.



Small ROM Sizes
Simpler Structure for Faster Execution

CONTENTS

C Language Oriented Architecture

C

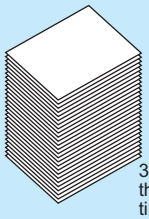
Develop systems efficiently in C

Program development is 3-10 times faster

Past — Assembler program

Syntax dependent on the microcomputer

```
        cmp (ram1),(ram2)
        bgt $label
        mov (ram5),r0
        sub (ram4),r0
        jmp $label2
label   mov (ram5),r0
        add (ram4),r0
label2  mov r0,(ram3)
```

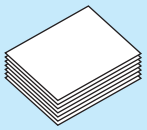


3-10 times the development time

Future — C language program

Easy to read

```
if(a>b)
  c=d+e;
else
  c=d-e;
```



The C programming language makes it easier and faster to program large systems, but generates more code than assembler. Larger code size in turn means higher ROM costs and slower execution speed. Panasonic eliminates this tradeoff with its C language-oriented microcomputers, which combine a true microcomputer architecture with a highly optimized C compiler to achieve unprecedented code efficiencies. This combination minimizes the size of the resulting code while retaining the threefold to tenfold development speed advantage afforded by the C programming language. The approach yields efficient system development in C over the entire range of 8- and 32-bit microcomputers.

C Language Oriented Microcomputer for [Higher Performa

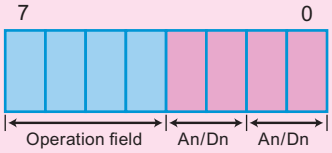
High Performance

High

Single-cycle execution for higher throughput

New instruction code assignments

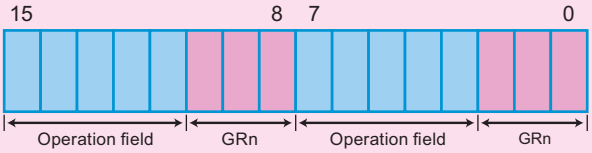
Basic instructions (register-to-register operations, load/store operations) fit within a single byte.



An : Address register field Dn : Data register field

Conventional code assignment for general register instruction

Because register field take up six bits, it is impossible to fit the instruction into a single byte.



GRn : General register field

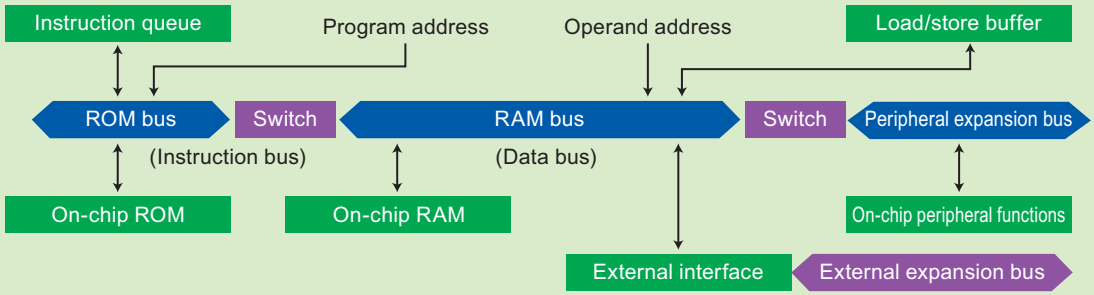
The register set represents a careful balancing of hardware needs against C compiler code generation efficiency. From the eight available registers, the instruction format requires four bits to specify registers. As a result, the architecture assigns the basic instructions most frequently used in C code to single bytes. The compiler uses register optimization techniques to maximize the efficiency of register usage. Finally, a high-performance pipeline executes these instructions at the rate of one every machine cycle.

Low Power Consumption

Low

Optimized internal bus design lowers power consumption

AM1 (MN101), AM3 (MN103L) bus conversion



The CPU features separate buses for instructions and data, and even provides a separate bus for expanding the latter for use with on-chip peripheral functions.

nce] + [Faster Development]

We Match Your Needs. You Don't Have to Match Ours.

Result : Greatly Reduced System Costs

Using an AM Series C language oriented microcomputers

Development advantage	Device advantage
Using the C programming language greatly reduces development time. The language also facilitates the accumulation and reuse of software resources.	The resulting systems are smaller, have higher performance, and consume less power.

Code takes less ROM.

The result is higher cost performance from both the device and the system.

These C language oriented microcomputers (the AM Series) offer twin advantages to system development. First, they permit program development in C, a language that cuts development time. Secondly, they help reduce system costs by fitting programs into smaller ROM spaces. The result is higher cost performance from systems that are smaller, have higher performance, and consume less power.

Microcomputer with Flash-memories

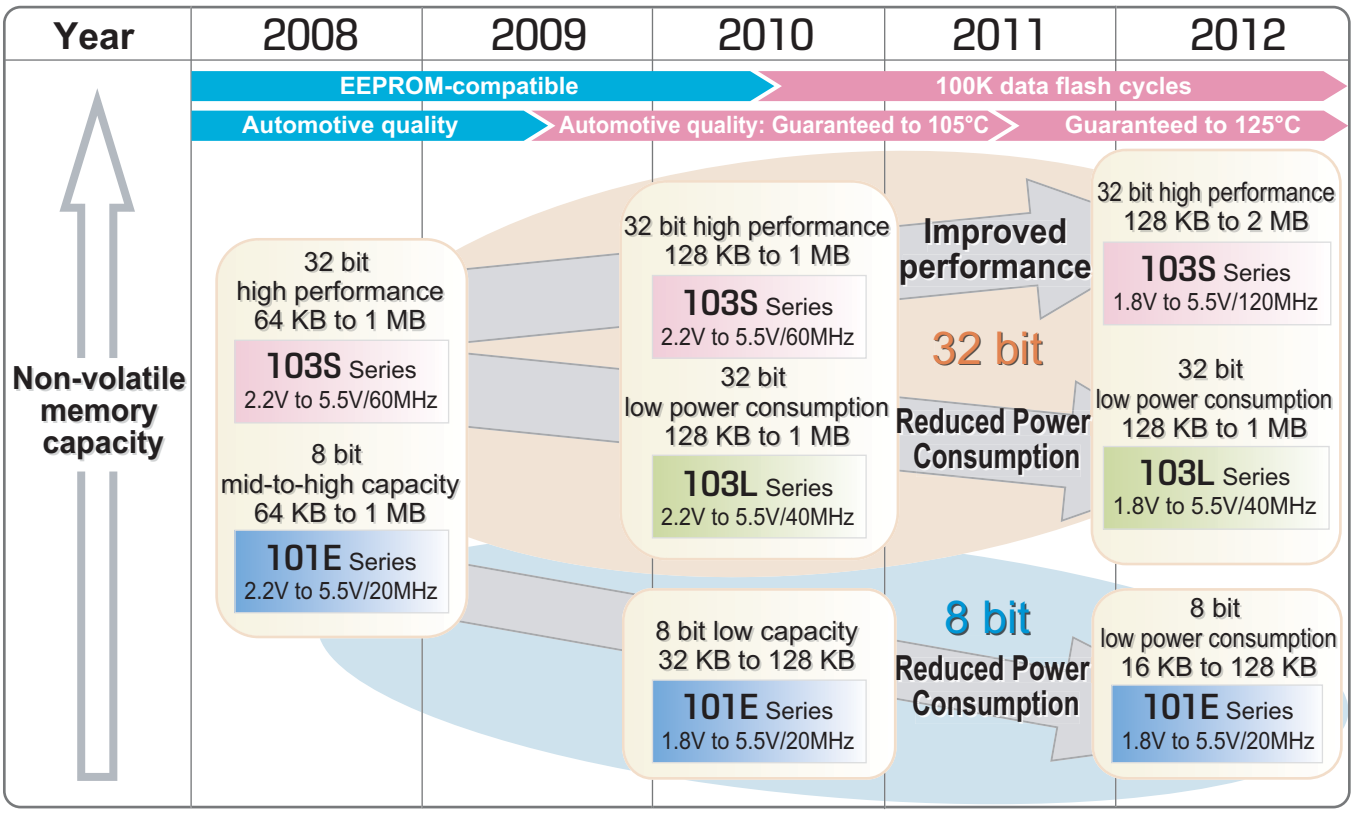
The World Microcomputers with Flash Memory Expands

Road Map of Microcomputers with Flash Memory

As the development period of equipment becomes shorter, it is increasingly necessary that system control microcomputers be equipped with flash memory that can be substituted for the mask ROM. This is because conventional microcomputers are unable to meet the customers' requirements, for example, to rewrite the program after the microcomputer is mounted on the equipment and to shorten the lead time after the ROMs have been ordered.

Microcomputers with flash memory allow the programs to be rewritten even after being mounted on the equipment. This helps reduce the equipment system development period.

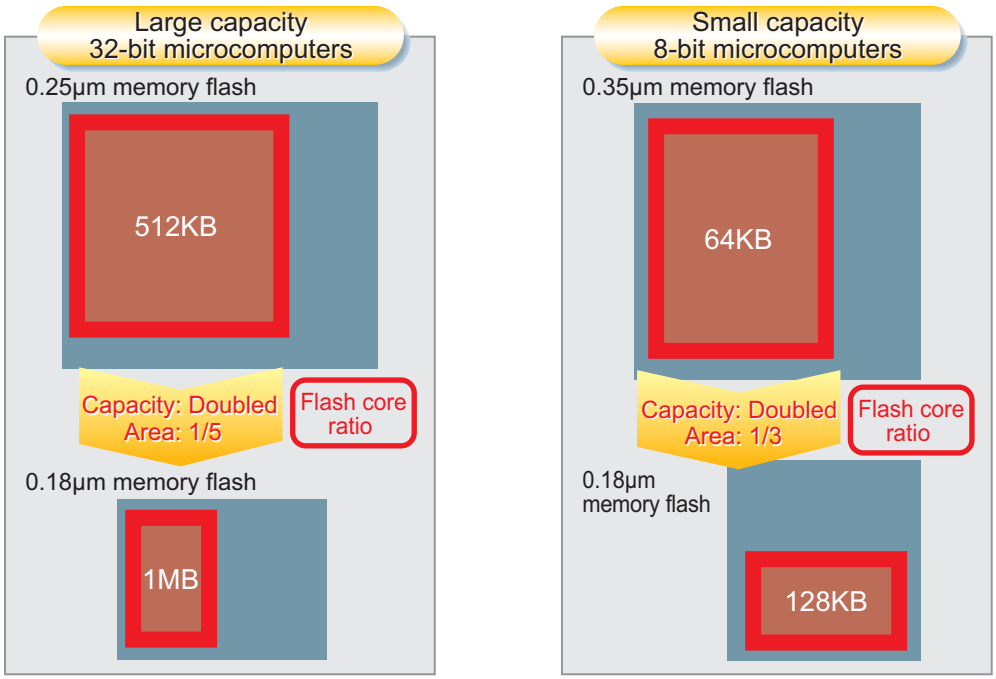
Features of our microcomputers with flash memory are not limited to this. They also help make audio equipment and household electrical appliances more sophisticated and compact, and consume less power.



Our 0.18µm Flash Core Opens The Way to Tomorrow

The world's smallest memory cell technology used in microcomputer onboard flash memory achieves a 10 to 1 surface ratio reduction (for flash area: 1MB).

When our microcomputers equipped with a 0.18µm flash memory are compared to those with a conventional 0.25µm flash memory, the ROM capacity is doubled while the area is reduced to one fifth, providing excellent cost-effectiveness.
This is achieved through our 0.18µm flash core being developed using the world's smallest class memory cell technology.



* As of Novemver 2005

High-Performance

Lower Power Consumption

Large capacity microcomputers

High-speed processing of internal 60 MHz with
low power consumption
• 180 mW (60 MHz/3.0 V) ..... 1 mA/MHz

Small capacity microcomputers

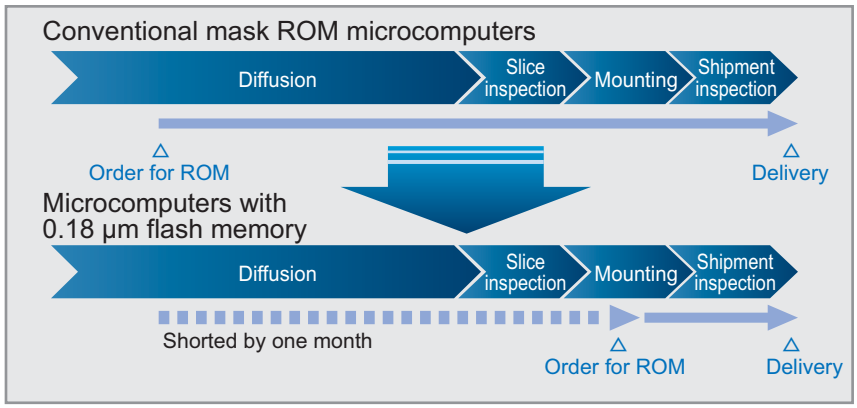
Performance at a high level in the 8-bit class with
low power consumption
• 18 mW (20 MHz/3.0 V) ..... 0.3 mA/MHz
• Minimum instruction execution time 50 ns(2.7 V to 3.6 V)

Shorter Lead Time Reduces Development Risks

Shipment with ROM Data Written in A Short Lead Time

Shortens the lead time from receipt of ROM data to shipment by one month

Microcomputers with flash memory reduce the lead time by approximately one month compared to the conventional mask ROM by installing ROM data immediately during mounting.
It is also possible to write the programs in our production lines or at our business partners.



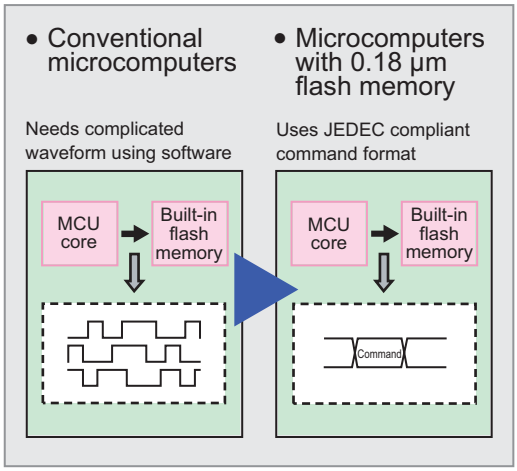
More Diversified and Convenient Program Environment

Simple Rewriting Program Development

Simplifies development for users' original rewriting program (e.g. writing to PC) using JEDEC compliant command format

- Supports rewriting using JEDEC compliant command format
- Provides samples of rewriting programs
- Rewriting from the serial port specified by users is possible without any special tools.
- Optimal for rewriting at shipment lines or service departments

For conventional microcomputers with flash memory, it was necessary to create a complicated waveform using the software to rewrite the built-in flash memories.
New microcomputers with a 0.18µm flash memory are able to rewrite programs using the JEDEC compliant command format, so the rewriting program can be created easily. We can also provides samples of rewriting programs.



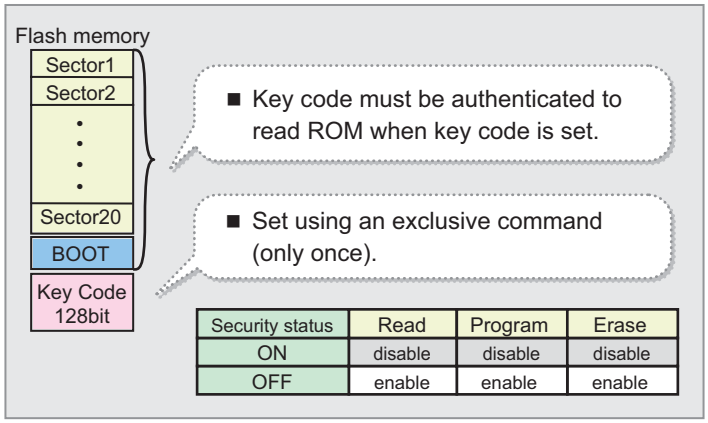
Secure Guard of Important Software

Reliable Security Function

Equipped with a protection function to prevent unauthorized access to ROM code

- A key code (128 bits) storage area is provided.
- Only one setting of key code is available.
- The key code must be authenticated using an exclusive command to read the ROM data.
- Shipment is possible with security information set.

The 0.18µm flash core has a 128 bit key code. Writing this key code prevents the ROM data from being read by third parties.
The key code can be written only once. The flash memory with a key code written to it cannot be accessed unless the key code is authenticated.
Accordingly, persons that do not have the key code cannot read the ROM data using programming various tools. Executing instructions from the CPU or reading ROM data via executed commands are, of course, possible without the key code.



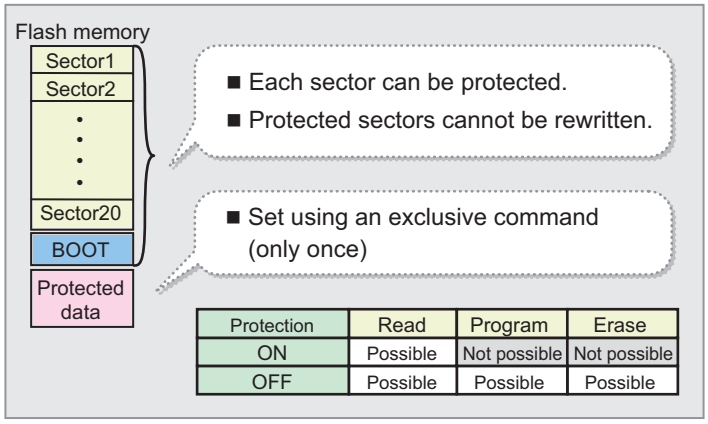
Security status	Read	Program	Erase
ON	disable	disable	disable
OFF	enable	enable	enable

Protection Function

The writable area is limited to protect data even when the microcomputer has runaway.

- A protected data storage area is provided.
- Each sector is protected using an exclusive command (only once).
- Shipment is possible with protect data set.
- The protected sector cannot be rewritten.

The 0.18µm flash core has a protection function. This function prevents the flash memory being rewritten accidentally even when the microcomputer has runaway.
Once the protection for the protection data area is set to [ON], each sector can be protected. The protection data area can be written only once.
The protected sector cannot be rewritten, so the memory data will not be damaged even when the program has runaway.



Protection	Read	Program	Erase
ON	Possible	Not possible	Not possible
OFF	Possible	Possible	Possible

Microcontrollers with Improved Resistance to Noise

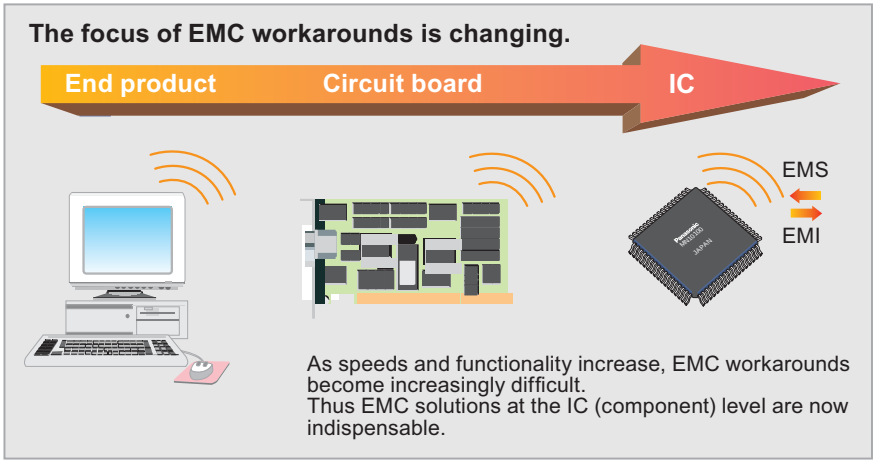
Why is Electromagnetic Compatibility (EMC) So Important Now?

The IC, as the center of control in modern electronic equipment, plays a crucial role supporting progress in this equipment. As the functionality provided by the latest electronic equipment continues to advance, even higher integration levels and even higher speeds are required in their ICs. At the same time, the popularity of portable electronic equipment has led to demands for further miniaturization and lower operating voltages. To respond to these needs and demands, IC fabrication processes have moved to ever finer feature sizes, progressing in tandem with other IC developments.

Due to these advances, IC malfunctions due to noise is becoming a significant issue, and inadequate electromagnetic compatibility (EMC: the ability to operate in the presence of noise) is now the focus of much concern.

Since EMC problems largely depend on the PCB design, until now, EMC problems have been seen as an issue for end product design, and workarounds have largely focused on the end product. However, due to the lower voltages and higher speeds of the latest equipment, it has become harder then ever to distinguish between noise and normal signals. At the same time, the increasing functionality of advanced ICs has made analyses related to EMC more difficult, and this in turn makes workarounds in the end product harder to achieve.

With today's shorter product cycles, the time and effort required to achieve the required EMC at the end product level has become a significant factor, and improved resistance to noise at the independent IC level is becoming increasingly important.



EMC Standards for ICs

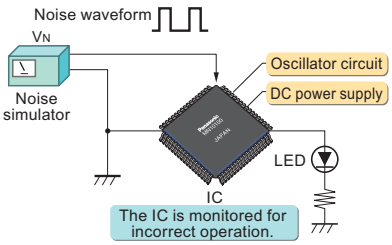
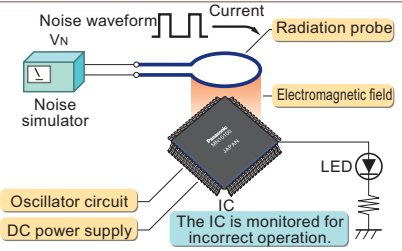
In Japan, EMC standards for electronic equipment as end products are regulated by a variety of laws covering electromagnetic radiation and consumer products. Radio Low, Electrical Appliance and Material Control Low, or similar laws are in force around the world, such as the IEC regulations on electronic equipment that have been in force in Europe since 1996.

In contrast, EMC standards for electronic device such as ICs are still at the stage where the IEC is working on the standardization of test procedures. Although evaluation procedures have been standardized for EMI, study has only just begun on electromagnetic susceptibility (EMS).

In addition to EMI measurement in conformance with the standards being developed, Panasonic is also developing evaluation methods for EMS such as those described below and preparing an environment that will allow independent evaluation of ICs.

Panasonic's Original Noise Immunity Evaluation Methods

Panasonic models the noise entering an IC as being of two types: conductive noise and radiation noise, and aims at standardization with common programs and noise evaluation boards that improve observability to eliminate dependence on the user's mounting boards and software.

Test	DC line noise test	Loop radiation noise test
Presumed noise	Direct noise from the power supply or IC pins	Indirect noise transmitted across space
Overview		

EMS Countermeasures (EMS: Electromagnetic Susceptibility)

Technologies for reduced EMS for improved noise immunity characteristics

Causes of IC Malfunctions

The ICs used in electronic equipment are subject to a wide range of noise sources. These include power supply noise, electrostatic noise (ESD), radio noise, and spark noise from high-voltage components in the vicinity.

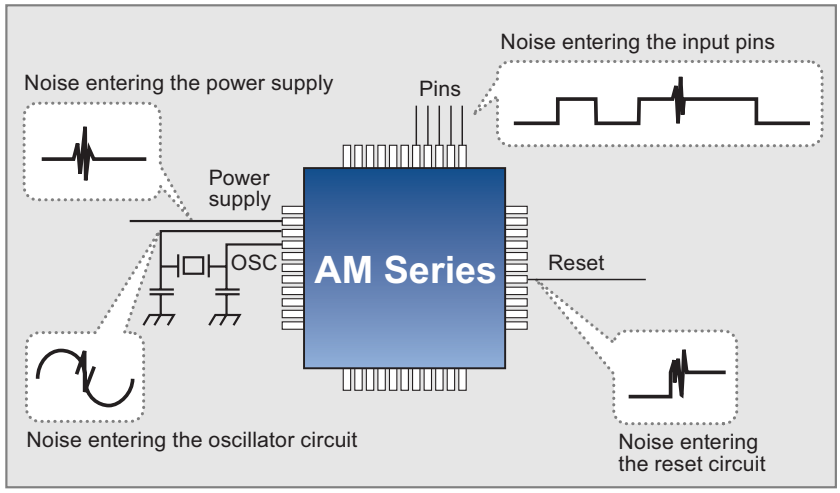
These noise signals enter the end product through power supply lines and the chassis, affect the PCBs the ICs are mounted on, and finally impinge on the ICs.

The following phenomena are thought to cause IC malfunctions in this type of environment.

(1) Noise is superimposed on the input signals, the IC is unable to distinguish between noise and the actual input signals, and as a result, the IC malfunctions.

(2) Power supply level fluctuations cause internal signal levels to fluctuate and the IC to malfunction.

■ What is the noise that enters ICs?



Enhancements to Noise Immunity Characteristics

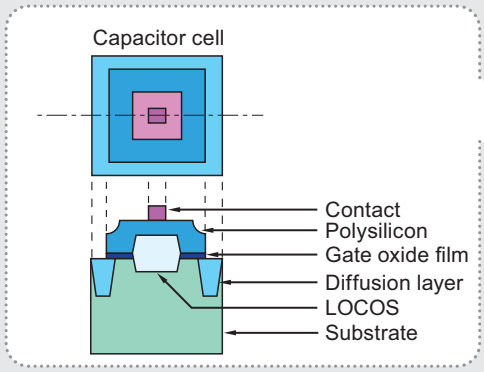
Panasonic has enhanced the noise immunity of the AM microcomputers based on the following points.

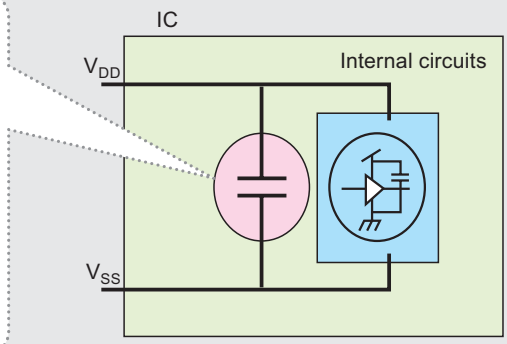
(1) Improved immunity to noise superimposed on input signals: Strengthening the ability to reject noise on the oscillator, reset, and interrupt signal pins.

(2) Improved immunity to power supply fluctuations: Fabricating capacitors internally on the chip itself to both improve power supply stability and to suppress fluctuations in the power supply levels.

(3) AM microcomputer operating mode stabilization: Additional failsafe measures have been implemented to handle rare and unexpected malfunctions.

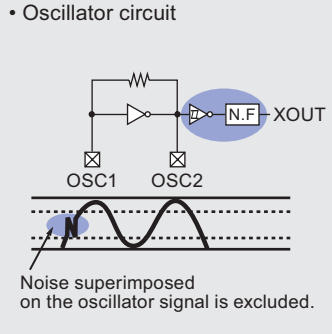
■ Improved resistance to power supply noise

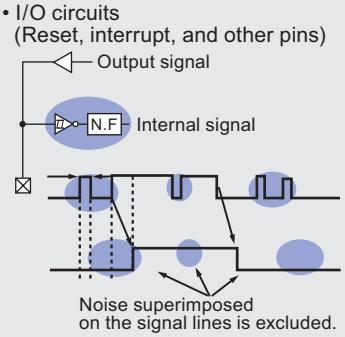




Capacitors are placed at critical points in the IC power supply and function blocks in the AM microcomputers. The placement of these capacitors in the IC stabilizes the power supply are and improves the IC's resistance to noise.

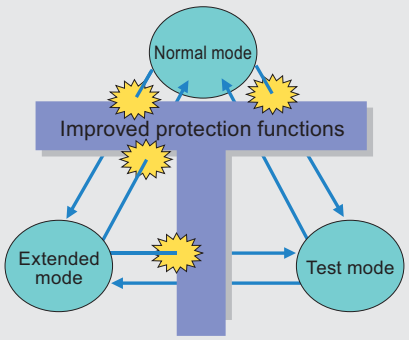
■ Improved resistance to input signal noise





Transmission of noise superimposed on input signals to internal circuits is prevented by inserting appropriate noise filters. Furthermore, measures such as adding Schmitt trigger circuits and optimizing input sensitivities have been applied to pins, such as oscillator, reset, and interrupt pins, for which software noise countermeasures are difficult.

■ Improved protection functions



These microcomputers feature protection functions for operating mode transitions to prevent operating mode transitions should a software runaway occur.

EMI Countermeasures (EMI: Electromagnetic Interference)

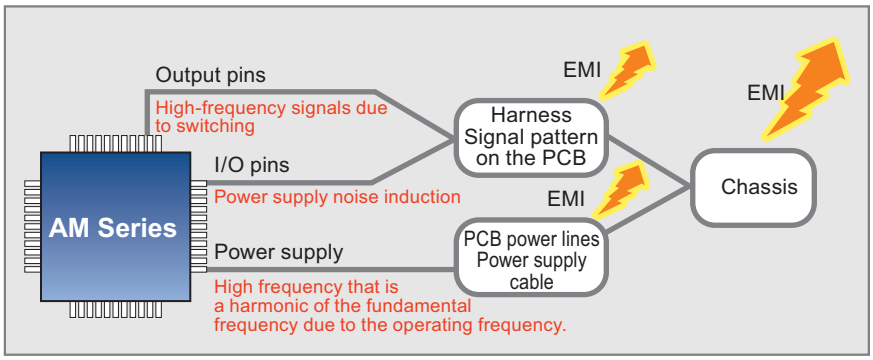
Reduction of extraneous radiation using EMI suppression technology

Causes of EMI Emission in Electronic Equipment

ICs used in electronic equipment handle digital signals and generate harmonic currents. It is thought that the PCBs, wiring harnesses, and chassis in application systems act as antennas and radiate these high-frequency signals to the surrounding environment.

Of these, the supply currents associated with internal logic operation show little attenuation, since these are upper harmonics of a fundamental that is the operating frequency, and as a result can easily cause problems.

■ **EMI generation mechanisms**



EMI Reduction Measures

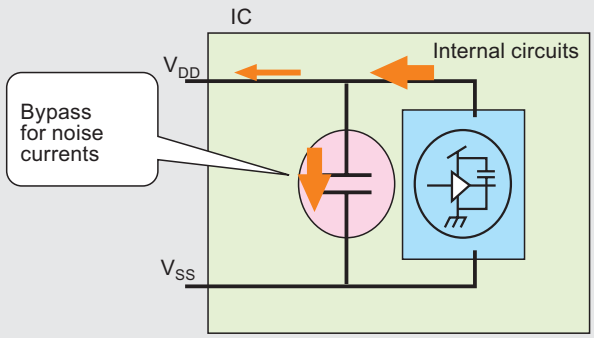
The following EMI reduction measures are implemented in the AM microcomputers.

(1) Improved decoupling capacitors: High-frequency noise leakage is suppressed by forming capacitors on the chip internal power supply lines.

(2) Current smoothing: IC internal peak currents were reduced by implementing gated clock circuits, optimizing the clock driver circuits, and other measures.

(3) Power supply isolation: Interference due to internal noise is prevented by isolating the CPU, I/O system, and analog system power supplies. Furthermore, the noise power itself is reduced by achieving both reduced power consumption and reduced EMS. In addition, it is now possible to create EMI countermeasures early in the IC design stage with EMI prediction technologies that use power supply current analysis technologies.

■ **Improved decoupling capacitors**



In the AM microcomputer series, bypasses are provided for noise currents by placing capacitors in the IC. This suppresses power supply noise leakage.

■ **Current smoothing**

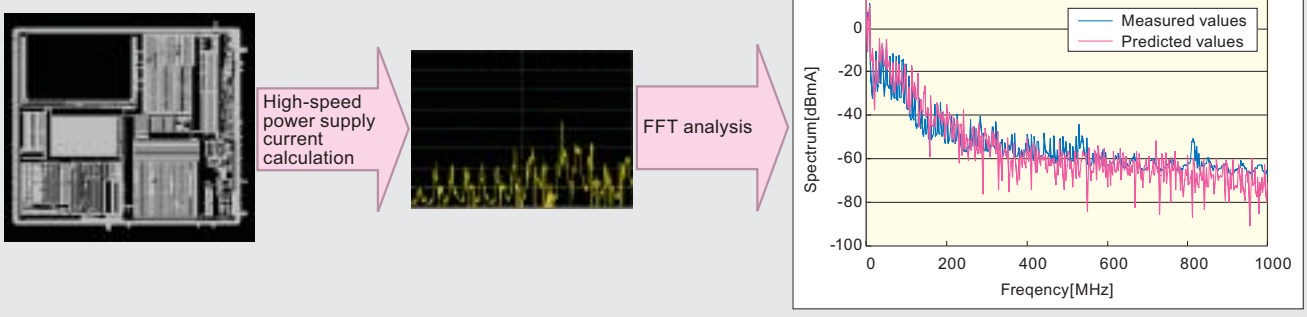
Noise source countermeasures
(Suppressing instantaneous currents)

- Optimization of clock drive transistor sizes
  Actual delay simulation is used to determine the optimum size.
- Pin current capacity optimization

Low-voltage operation that achieves both reduced power consumption and reduced EMS in the AM microcomputer series reduces the power of the noise itself.

■ **EMI prediction technology based on EDA**

Power supply currents are calculated using single-chip simulation, and the EMI of the final product is predicted based on waveform analysis.
This allows the desired EMI characteristics to be built into the product from the design stage.



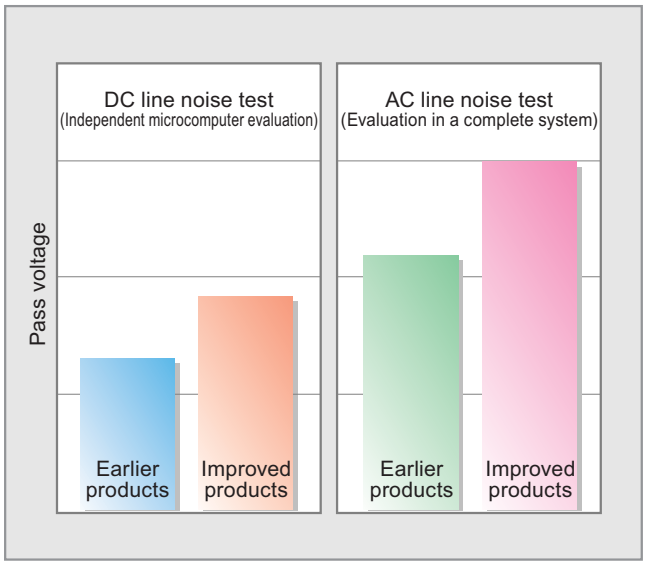
Examples of Improved EMC Performance

Achievement of both high noise immunity and low EMI

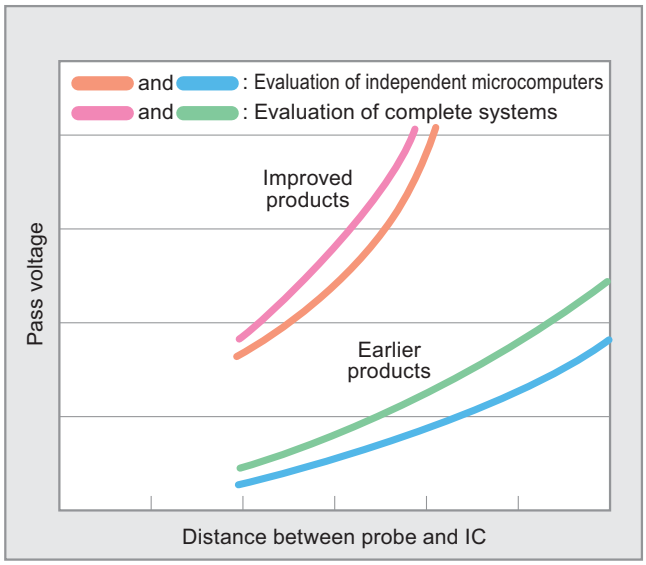
Examples of Improved Noise Immunity

Panasonic has achieved a significant improvement in noise immunity over earlier products. Despite progress in process feature sizes, Panasonic has achieved even further improvements in voltage handling capacity, and has assured better noise immunity than provided by earlier improved products, even in low-voltage process devices.

■ **Power line noise test**



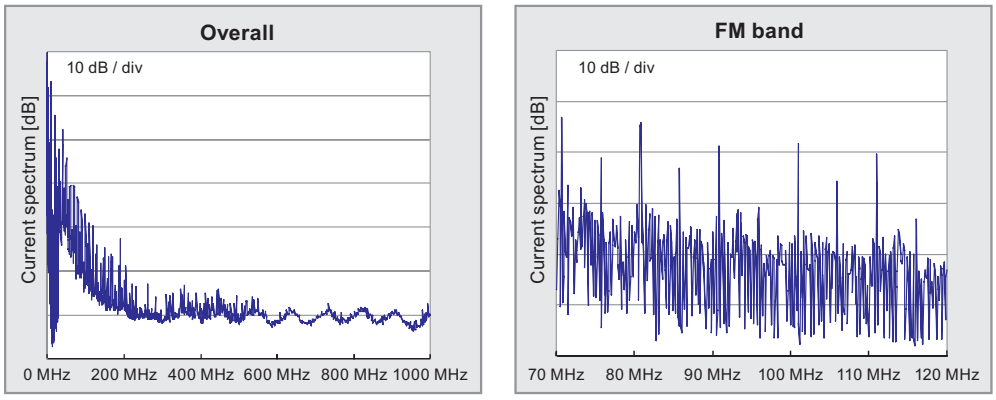
■ **Loop radiation noise test**



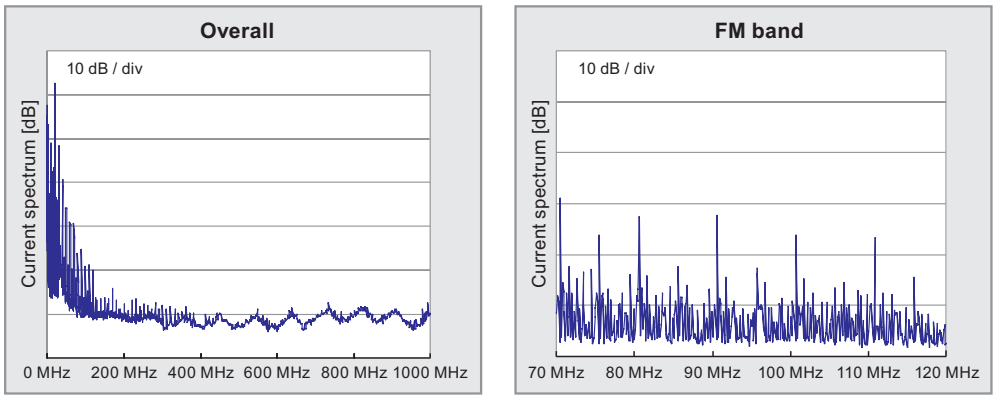
The DC line noise and loop radiation noise test methods were developed by Panasonic, and are based on two models, one for noise transmitted to the IC via conduction and one for noise transmitted to the IC via radiation.
To eliminate dependency of the test result on the application program, these tests are standardized with a common program that improves observability and a dedicated noise evaluation board.

Examples of Reduced EMI

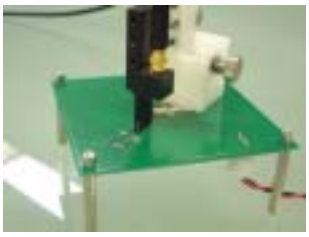
■ **Earlier products (Test results using the MP method)**



■ **Improved version (Test results using the MP method)**



* The MP method is one of the IC EMI evaluation methods currently being considered by the IEC. The IC power supply current is measured using a shielded loop antenna. (IEC61967-6)



EMI measurement test for the MP method

8-bit
AM1 (MN101) Series

C Language Development for 8-bit High-performance Microcomputers

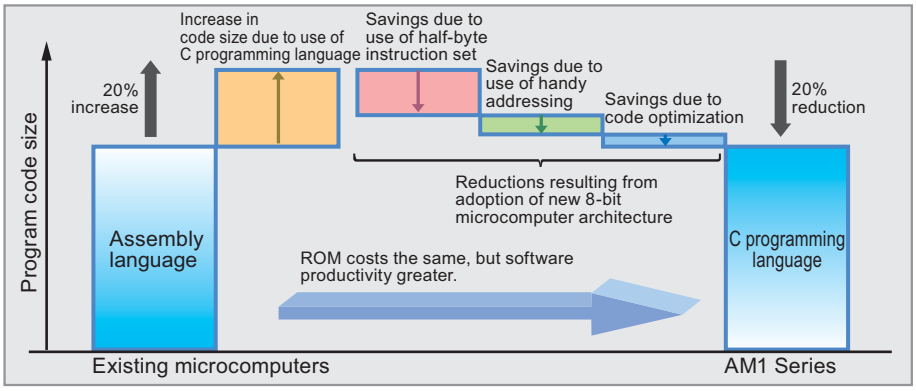
The AM1 Series of 8-bit microcomputers allows short-time program development in the C programming language. Its half-byte instruction set and other architectural features yield ROM code sizes that are small enough to rival those achieved with assembly language.
These devices are compact and have low power consumptions, yet offer high-speed operation with a minimum instruction execution time of 100 ns (at 5 V,3 V)*1 and 50 ns(at 5 V, 3 V).*2
These microcomputers are suitable for a wide range of applications demanding high cost performance.
The MN101 Series consists of the MN101C and MN101E Series.

*1:MN101C Series, *2:MN101E Series

C Language Oriented Architecture

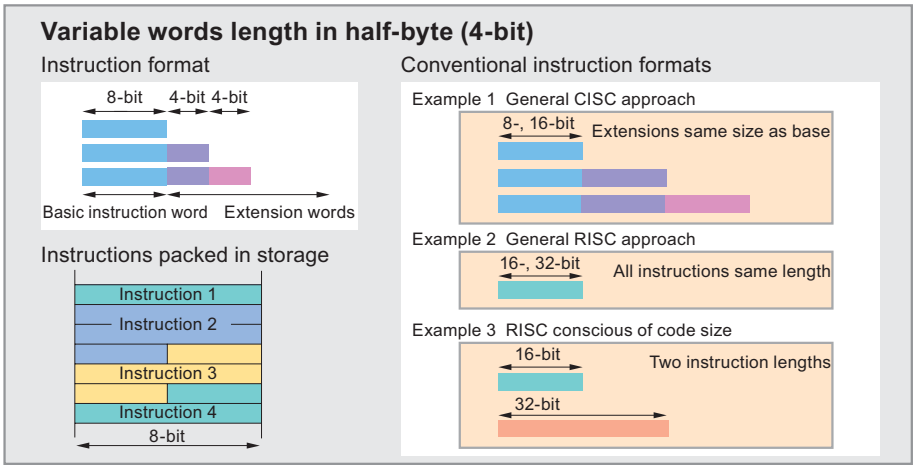
Programs in C the same size or smaller as those in assembler

Powerful architectural features such as a half-byte instruction set and handy addressing, plus aggressive code optimization mean that the C compiler can generate ROM code that is the same size or smaller as that produced using assembly language. (This conclusion is based on comparison with previous Panasonic microcomputers.)



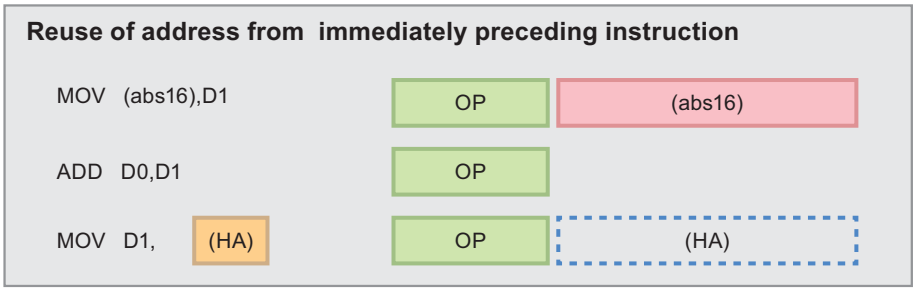
Half-byte Instruction Set

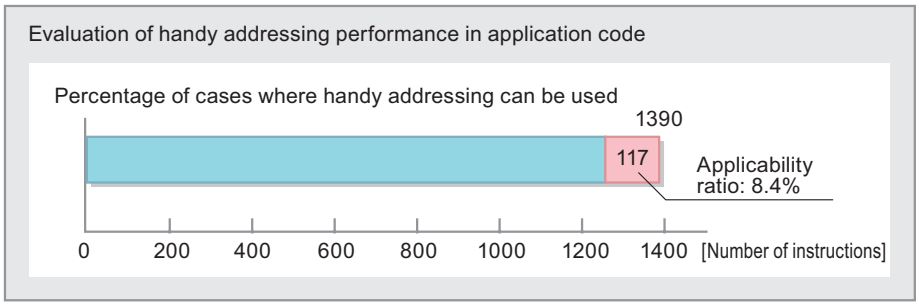
The Series adopts a variable-word length approach with basic instructions 1 byte long and extensions only 4 bits long. Since the resulting instruction set permits the specification of such operands as branch offsets and immediate values in units of four bits, instructions are shorter. Program sizes are therefore smaller.

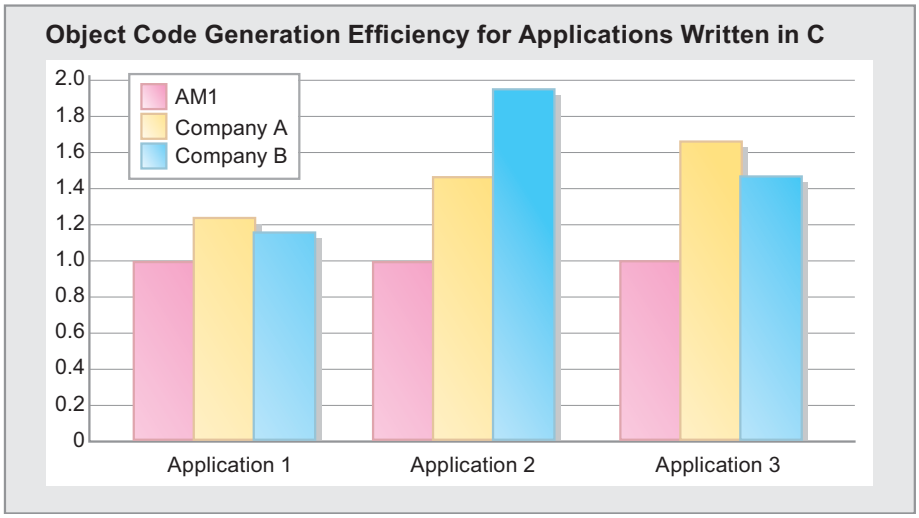


Handy Addressing

This technique focuses on the point that when variable data in memory is manipulated, load and store instructions will, in many cases, be to the same address. This technique allows the code size to be reduced by omitting the store instruction operand.







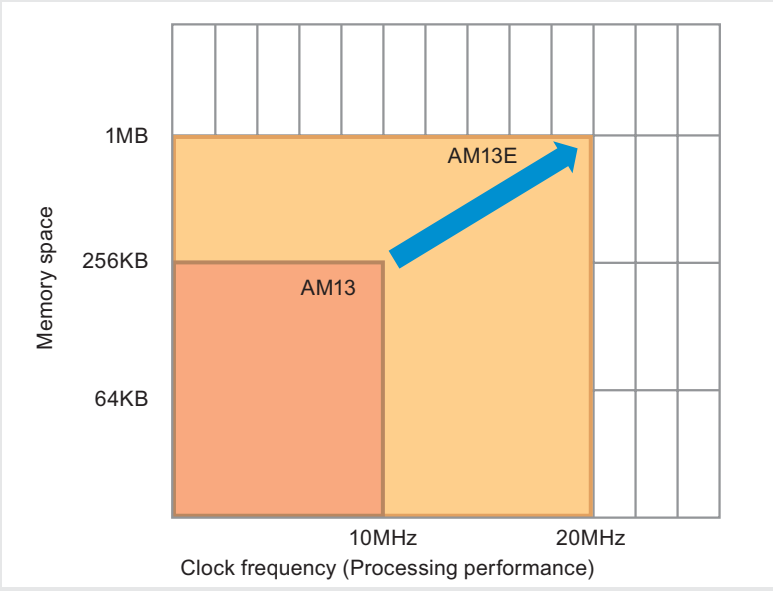
High-Speed Extended Memory Space Series (MN101E Series)

This series is upwardly compatible with the MN101C Series.

1 MB Linear Address Space

The 1 MB address space allows these microcontrollers to support more advanced and sophisticated systems.

	Memory space	Maximum on-chip ROM	Maximum on-chip RAM	Maximum internal clock frequency	Minimum instruction execution cycle
MN101C Series	256 KB	244 KB	11.75 KB	10 MHz	100 ns
MN101E Series	1 MB	944 KB	64 KB(Allocated in separate banks)	20 MHz	50 ns



32-bit
AM3 (MN103) Series

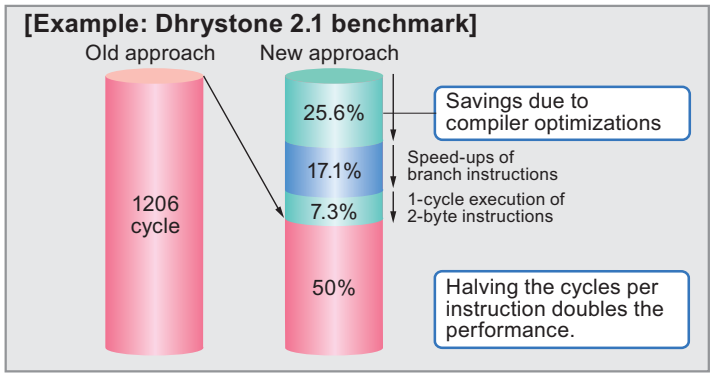
32-bit Lineup Accelerates Multimedia Performance

The AM3 (MN103) Series of 32-bit microcomputers covers a broad range of applications from equipment controllers through multimedia processing.
The combination of a C language oriented architecture and optimizing compiler delivers both high performance and lower power consumption.
To streamline the development of applications high in both performance and functionality, these devices incorporate the AM Series standard on-chip I/O bus (C-bus) and the extended calculation instruction function for adapting them for ASSP enhancement and ASIC microcomputer development.
The MN103 Series consists of the MN1030, MN103S, and MN103L Series.

C Language Oriented Architecture

Optimizing compiler generates highly efficient code

The optimizing compiler examines overall C program structure as it assigns variables to make most efficient use of the available registers. For frequently repeated loops, it preloads branch registers with the first instruction and the address of the next instruction. This small investment in additional hardware produces great advances in branch execution speed.

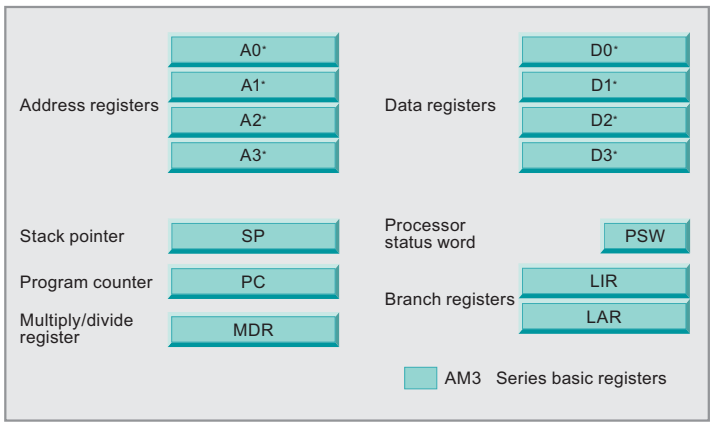


High Performance, Greater Efficiency

Variable word lengths of instructions, minimum of eight bits reduce program size

Cutting program size is always a major issue in embedded microcomputer applications. The AM3 (MN103) Series organizes registers by function and is thus able to adapt a variable instruction length approach with a minimum length of only 8 bits. Making the most frequently used instructions shorter and then maximizing register usage with an optimizing C compiler minimizes program size.

The AM3 (MN103) Series has eight basic registers available.
It also uses a Harvard architecture with separate instructions and data memory to boost throughput by eliminating conflicts between instruction fetches and data access.

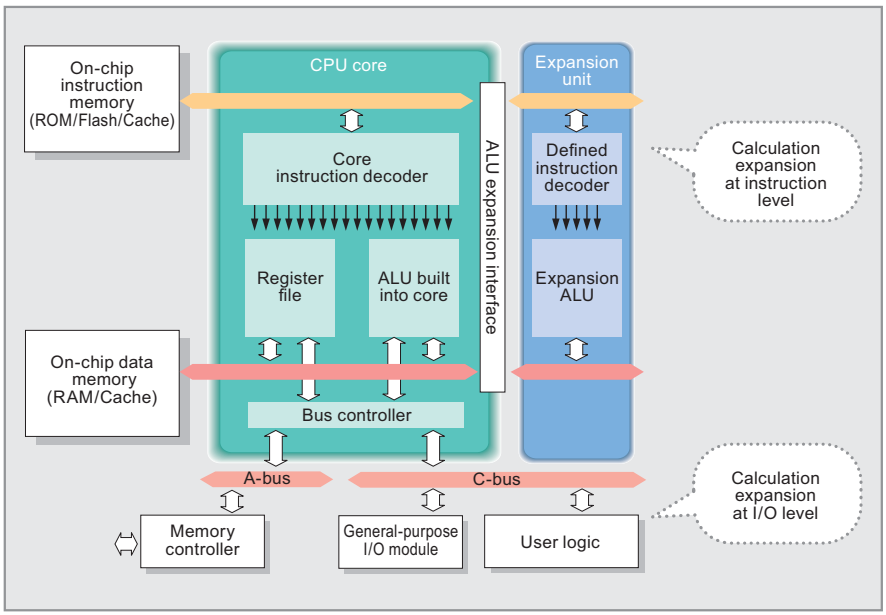


Multimedia Support

Mechanisms for increasing system-level performance

Function Expandability (MN103S Series)

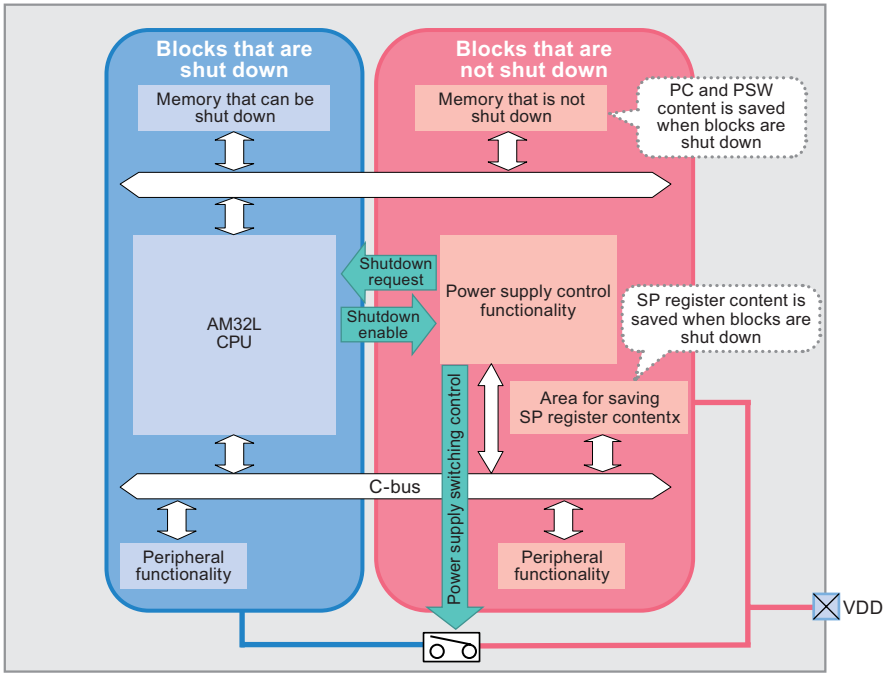
The expansion interface allows the development to assign multiply and accumulate and other new instructions to reserved opcodes to provide high-speed processing of digital sound and image data. This flexibility opens the door to semicustom microcomputer systems with the high cost performance demanded of multimedia applications.
In addition, the AM Series features an on-chip I/O bus, C-bus, for attaching I/O modules for the intended user application system. Standard across the entire Series, this bus greatly reduces development times for systems combining both performance and functionality.



Low Power Series (MN103L Series)

Low power series offering instruction set compatibility with the MN103S Series

The MN103L Series features a simple architecture with a 3-stage pipeline that preserves instruction set compatibility in order to deliver optimal performance in the medium to low speed segment. Furthermore, it is able to deliver both high performance and low power consumption by implementing 32 expanded instruction functions that are shared with the CPU's internal operations, including 32 × 32 high-speed multiplication and multiply-and-accumulate operations.
The product also boosts the effectiveness of standby mode with POFF mode, which maximizes power savings during standby operation by controlling the power supply to shut off power to certain blocks, including the core.
After returning from POFF mode, the blocks that had been shut down are reset (initialized) and the program can continue executing from an instruction just after a mode setting instruction.

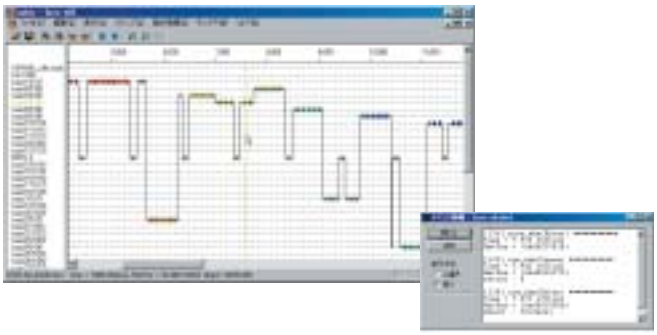


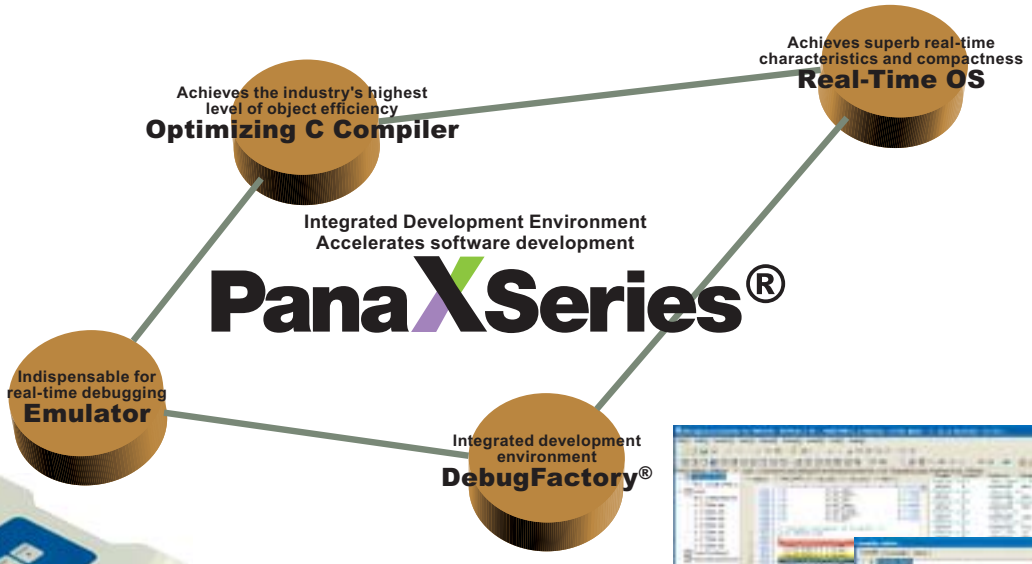
Development Environments

PanaXSeries®

PanaXSeries® Boosts up Your System Development with C Language

PanaXSeries® is Panasonic's cross (X) development support system.
This C program development tool presents a single development environment for developing 8 bit and 32 bit software.





Optimizing C Compilers

Compilers that achieve the industry's highest level of object efficiency

These compilers perform an extensive set of optimizations, including common subexpression elimination, induction variable elimination and replacement, optimal register allocation using a proprietary algorithm, and optimization of branch instruction and immediate address values at link time, and achieve the industry's highest level of generated code efficiency.

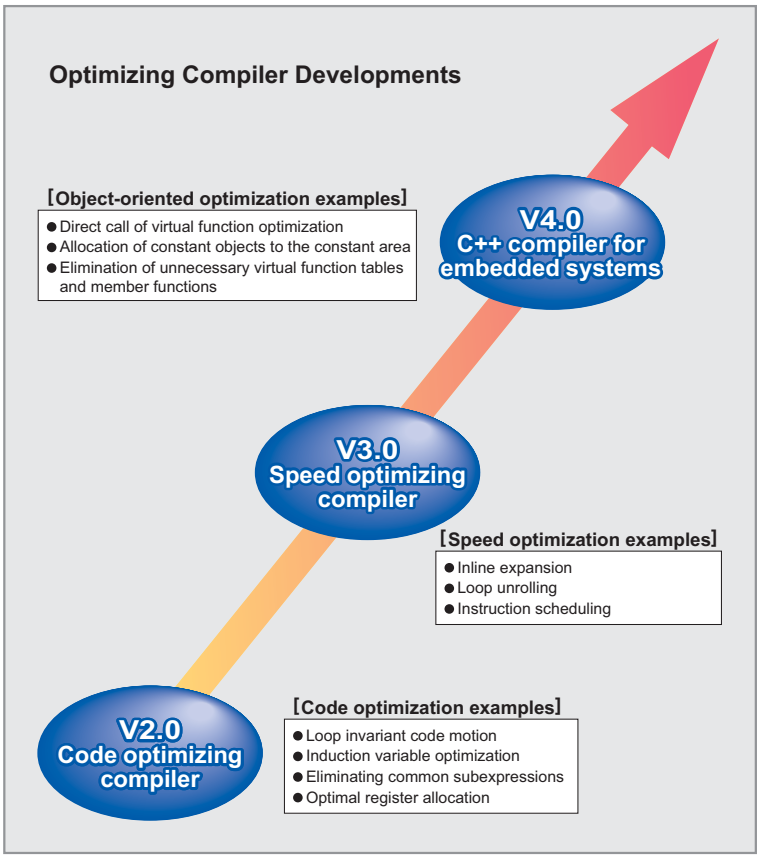
● AM1 (MN101) Series C Compiler

- The C compiler for the Panasonic 8-bit microcontrollers (AM1 series) improves code efficiency by extending and modifying parts of the ANSI C language specifications to take maximum advantage of the 8-bit microcontroller instruction set. This compiler also generates code that takes advantage of the AM1 series microcontrollers features such as half-byte instructions and handy addressing modes for efficient use of ROM space.
- This compiler supports functions, such as the char type bit field functions, that make effective use of 8-bit data.
- Furthermore, this compiler adds an inline assembler function that improves the interface between C code and assembler code. This makes it easy to integrate C and assembler code, and furthermore allows higher code efficiency C expressions to be used.

● AM3 (MN103) Series C Compiler and EC++ Compiler

- At the same time as providing speed optimizations such as inline function expansion (inlining), loop unrolling, and instruction scheduling, the compiler for the Panasonic 32-bit microcontrollers (AM3 series) also features improved size reduction optimizations such as tail merging to get the maximum performance from these 32-bit microcontrollers. In addition, this compiler also achieves faster processing of iterative programs and function calls by making effective use of the loop start instruction, special loop branch instructions, and highly functional subroutine call instruction provided by these 32-bit microcontrollers.
- Starting with version 4.0, this compiler also supports the EC++ language designed for embedded applications.

- EC++ is an object-oriented language for embedded processors that forgoes the features of C++ that may result in code bloat, and is a subset of C++.
- Additionally, Panasonic EC++ provides object-oriented language optimizations that reduce the size of the generated code making it possible for users to take advantage of object-oriented programming, even when developing software for embedded applications with severe memory resource limitations.

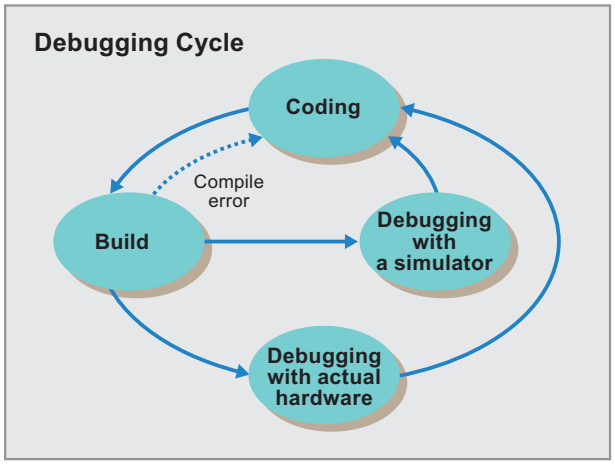


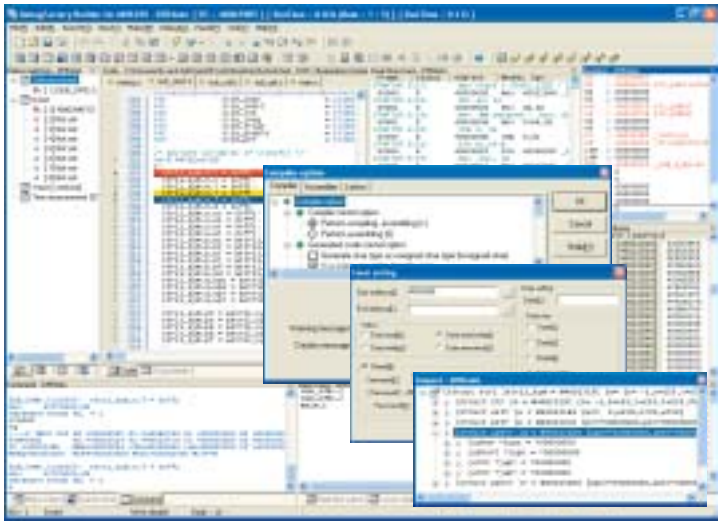
DebugFactory® Builder

Microcomputer software integrated development environment that supports debugging with a simulator

● User-Friendly Debugging Tools

The DebugFactory Builder provides efficient microcomputer software debugging by supporting, in a single application, the edit, build (make file generation and compilation), and debug sequence that is used repeatedly in debugging. For example, when you find a bug during debugging and want to change the source code, you can immediately change the source code in the debugging screen and then perform a build and reload operation with a single operation.





The DebugFactory Builder Screen

● Support Debugging with a Simulator

★There are certain microcomputer series for which simulation functions are not available.

Since the DebugFactory Builder includes a built-in instruction set simulator, microcomputer software can be debugged even if the hardware that is the debugging target is not available.

The DebugFactory Builder includes a visual tool that supports debugging with the instruction set simulator. This tool allows operations on the microcomputer, such as issuing interrupts or modifying memory, to be performed with icon operations, such as mouse clicks. This allows microcomputer software to be debugged on a personal computer as though one were using the actual hardware itself.

This tool can significantly speed up the product delivery period, since unit testing and integrated testing in advance of the availability of the hardware can be performed fully.

The DebugFactory Builder provides functions for performing automated unit tests and simplified system simulations without modifying the source code that will be embedded in the end product.

Example of a simulation debugging screen created with the panel tool included in the DebugFactory Builder.

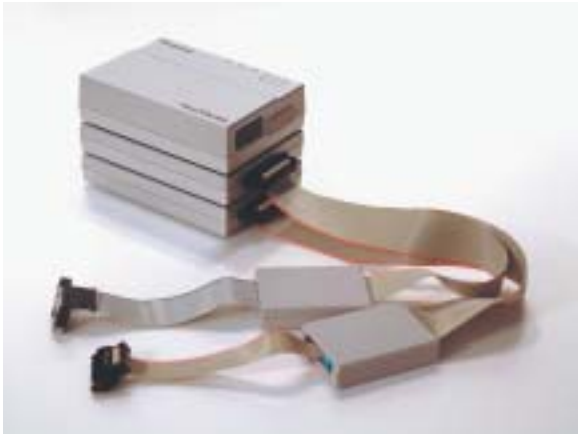
- ●Panel tool
- ●Function swapping
- ●Memory access event
- ●Timer event
- ●File access

Support Functions for Debugging with a Simulator

PanaX NEO On-Board Debugging Environment

Ideal for debugging high-speed processors and actual machines

- PanaX NEO is a new debugging environment designed to take the place of previous on-board debugging environments.
- In addition to basic functionality equivalent to that offered by in-circuit emulators, including execution controls, events and breakpoints, and program downloading, semi-non-intrusive functions (such as the watch function) enable efficient real-time debugging. The optional data gathering unit enables real-time trace functinality such as program execution log acquisition.
- Standard host computer connectivity is via USB 2.0 (High Speed) and Ethernet 10Base-T/100Base-TX.



● AM32 (MN103S) Series

- Either JTAG boundary scan test pins or a dedicated serial interface (DWire32A) is used as the debugging control interface.
- For products with trace pins, a data gathering unit can be connected to enable real-time trace functionality.

<Applicable products>

- MN103S Series microcomputers with a debugging control interface (JTAG/DWire32A) and system ICs that include an AM32 core

On-board debugging environment	PanaXSeries®
	AM32 (MN103S)
Maximum operating frequency	The internal operating frequency of the microcontroller
Debugging control interfaces	JTAG/DWire32A
Events (hardware breakpoints)	Total for ROM and RAM: 4 points*1, Area, AND, and Sequential breakpoints
Trace capacity	512K frames*2 *3
Trace operating modes	Branch and delayed trigger*2
Time measurements	Between arbitrary events, maximum, minimum
Trigger	Input, Output (Event, Signal Level)
Semi-non-intrusive functions*4	Changes to/display of memory and I/O registers, trace data display (dump), watch, RAM monitor, changes to various settings
Debugger	DebugFactory® Builder
Host OS	Windows® 2000/XP(SP2 or later)/Vista
Host interfaces	USB 2.0 (High Speed), Ethernet 10BASE-T/100BASE-TX
Other features	Using execution address instead of fetch address in ROM event setting and display of trace data.

*1: Differences exist depending on the model used.
*2: For products with trace pins
*3: Depends on debugger settings and target program.
*4: May stop target program execution briefly.

In-Circuit Emulator

Provides non-disrupted development aid for high-speed devices

● Real-time Emulation

Integrated emulator circuits and high-density mounting technology combine to deliver high-speed, real-time emulation.

● Powerful Event, Break and Trace Capabilities

- H/W breakpoints can be used as events that trigger various debugging actions.
- These events can be combined with other events to form a complex pre-condition (e.g. SEQUENTIAL or AND)
- Various and useful trace operation modes, e.g. delayed triggered conditioned by the event.

● Non-intrusive Debugging Functionality

Without any interference to program execution, you can see contents of memory, display trace data and alter event, break and trace settings.

● Low Voltage Devices are Supported

MN103L Series In-Circuit Emulators

NEW

Introducing the newly released PX-ICE103L In-Circuit Emulator for the MN103L Series

● Dramatically enhanced functionality compared to the PX-ICE103S, an in-circuit emulator for the MN103S

- Enhanced basic functionality such as event and time measurement
- Expanded RAM monitor capacity
- C0 (command coverage) support
- High-accuracy profile (The sampling rate is about 100 times in comparison with PX-ICE103S.) / High-speed RAM sampling

● USB 2.0 (High Speed) host interface

● Selection of target connection method to match target system

- Flexible cable for versatile connectivity options
- Direct adapter connectivity for faithful replication of characteristics

● Same operation as target device thanks to probe using actual chip (Microcomputer with Flash-memories)

● Simple model lineup

	PX-ICE103L	PX-ICE103S
Maximum operating frequency *1	40 MHz	100 MHz
Emulation memory size (Byte)	On-chip ROM: 2 MB, On-chip RAM: 64 KB, Expansion RAM: 1 MB (2 MB)*2	On-chip ROM: 1 MB Expansion RAM: 4 MB
Events (H/W breakpoints)	ROM: 4 points; RAM: 8 points, Area, AND, Concurrent AND, Sequential, External input, Timeout	ROM: 4 points; RAM: 4 points, Area, AND, Sequential
Trace memory depth	128 K frames (1 M frames)*2	128 K frames
Trace operation modes	Normal, Jump, Event, Data, Delayed trigger, Multi, Cumulative trace	Normal, Jump, Event, Data, Delayed trigger
RAM monitor (real-time guarantee with specialized hardware)	64 KB internal RAM + 1 KB other × 16 blocks (with read/write data detection function)	1 KB (no distinction between read/write data)
Time measurments	Between any two events (breakpoints) (max. approx. 116,853 years) Maximum, minimum, and average time measurement (max. 858 sec) Resolution: 25/50/100/200 ns	Between any two events (breakpoints) Maximum and minimum time measurement (max. 432 sec) Resolution: 25/50/100 ns
Trigger	Input (3-bit edge detection and 8-bit data detection) Output (Select either 2-bit event or 8-bit data)	Output (Event output, Data output)
Coverage	C0 coverage (execution address) 512 KB × 4 blocks	—
Non-intrusive functions *3	Display of trace raw data; Watch; RAM monitor; Alteration of event, break, and trace settings	
Semi-non-intrusive functions *4	Display and modification of memory and I/O registers, Display of trace data with disassemble list	
Sampling functionality	High-precision profile, high-speed RAM data sampling	Profile
Debugger software	DebugFactory® Builder	
Host OS	Windows® 2000/XP(SP2 or later)/Vista	
Host interfaces	USB2.0 (High Speed)	PC card and PCI interface board
Other comments	Using execution address instead of fetch address for events, trace data display, coverage, etc.	

Note: • The PX-ICE103S does not support the MN103L Series. The PX-ICE103L does not support the MN103S Series.
• Unless otherwise noted, instruction addresses are treated as execution rather than fetch addresses.

*1: Indicates internal operating frequency in microcomputer. Frequency may vary by model.
*2: Figures in parentheses represent options that can be specified at time of order.
*3: Does not interfere with target program execution.
*4: May stop target program execution briefly.

MN101C/E Series In-Circuit Emulators

● PX-ICE101C/E Standard-edition In-Circuit Emulator

The PX-ICE101C/E is the standard in-circuit emulator for the MN101C/E Series.

● PX-ICE101C/E-PLUS Expanded Trace Memory Type In-Circuit Emulator

This in-circuit emulator with expanded trace memory adds 1M frames to the trace memory offered on Panasonic's previous in-circuit emulator (PX-ICE101C/E).

● PX-ICE101C/E-Lite Economy Type In-Circuit Emulator

This in-circuit emulator is available at a lower cost than Panasonic's previous in-circuit emulator (PX-ICE101C/E).

- Lower cost due to partially reduced functionality and a design that integrates the in-circuit emulator and probe into a single unit
- USB 2.0 (High Speed) host interface
- Same model-specific probe board as Panasonic's previous in-circuit emulator (PX-ICE101C/E) (Contact Panasonic for more information on applicable products.)

PX-ICE101C/E-Lite

	Normal Type PX-ICE101C/E	Expanded Trace Memory Type PX-ICE101C/E-PLUS	Economy Type PX-ICE101C/E-Lite
Maximum operating frequency *1	20 MHz	24 MHz	
Emulation memory size (Byte)	944 KB for instruction / 64 KB for data		
Events (H/W breakpoints)	ROM: 16 points; RAM: 16 points Area, AND, and Sequential breakpoints		ROM: 2 points; RAM: 2 points Area, and Sequential breakpoints
Trace memory depth	32 K frames	1 M frames	2 K frames
Trace operation modes	Normal, Area, Delayed triggered, Multi		Normal, Delayed triggered
RAM monitor	Specialized hardware(real-time guarantee) Internal RAM space: 64 KB + 128 KB		Installing no specialized hardware
Time measurments	Between any two events (breakpoints) (max. 214 sec) and maximum time measurement Resolution: 50 ns		Maximum between arbitrary events (breakpoints) (max. 214 sec) Resolution: 50 ns
Trigger	Input: 8 bit, Output: 8 bit (Event, Signal Level)		Output: 2 bit (Event, Signal Level Low)
Coverage	C0 coverage (prefetch address) 1 MB (full space)		—
Non-intrusive functions *2	Display of trace raw data; Watch; RAM monitor; Alteration of event, break, and trace settings		Display of trace raw data, Alteration to event, break and trace settings
Semi-non-intrusive functions *3	Display and modification of memory and I/O registers, Display of trace data with disassemble list		Display and Modification of memory or I/O registers, Display of trace data with disassemble list, "Watch", "RAM monitor"
Sampling functionality	Profile		
Debugger software	DebugFactory® Builder		
Host OS	Windows® 2000/XP(SP2 or later)/Vista		
Host interfaces	PC card and PCI interface board		USB 2.0 (High Speed)
Other comments	Using execution address instead of fetch address in ROM event setting and display of trace data		

Note: Unless otherwise noted, instruction addresses are treated as execution rather than fetch addresses.

*1: Indicates internal operating frequency in microcomputer. Frequency may vary by model.
*2: Does not interfere with execution of target program.
*3: May stop target program execution briefly.

PX-ICE101C/E-Advance Advanced In-Circuit Emulator

NEW

Updates previous PX-ICE101C/E and PX-ICE101C/E-PLUS in-circuit emulators.

(This product remains under development, and specifications are subject to change without notice. Information about the product release schedule is available at Panasonic's website.)

● Major Features

- USB 2.0 (High Speed) host interface
- Expanded trace depth and functionality
- More advanced time measurement functionality
- Sampling functionality
  High-accuracy profile (The sampling rate is about 100 times in comparison with PX-ICE101C/E.)
  High-speed RAM data sampling
- Same model-specific board as the PX-ICE101C/E and other Panasonic in-circuit emulators

	PX-ICE101C/E-Advance
Maximum operating frequency *1	24 MHz
Emulation memory size (Byte)	Internal ROM use: 944 KB for instruction / internal RAM use: 64 KB for data
Events (H/W breakpoints)	ROM: 8 points; RAM: 8 points Area, AND, Concurrent AND, Sequential, External input, and Timeout breakpoints
Trace memory depth	128 K frames (1 M frames) *2
Trace operation modes	Normal, Jump, Event, Data, Delayed trigger, Multi, Cumulative trace
RAM monitor	Specialized hardware (real-time guarantee) 64 KB internal RAM + 1 KB other × 16 blocks (with read/write data detection function)
Time measurments	Between any two events (breakpoints) (max. approx. 116,853 years) Maximum, minimum, and average time measurement (max. 858 s) Resolution: 25/50/100/200 ns
Trigger	Input (3-bit edge detection and 8-bit data detection) Output (select either 2-bit event or 8-bit data)
Coverage	C0 coverage (execution address) 1 MB (full space)
Non-intrusive functions *3	Display of trace raw data; Watch; RAM monitor; Alteration of event, break, and trace settings
Semi-non-intrusive functions *4	Display and modification of memory and I/O registers, Display of trace data with disassemble list
Sampling functionality	High-precision profile, high-speed RAM data sampling
Debugger software	DebugFactory® Builder
Host OS	Windows® 2000/XP(SP2 or later)/Vista
Host interfaces	USB2.0 (High Speed)

Note: Unless otherwise noted, instruction addresses are treated as execution rather than fetch addresses.

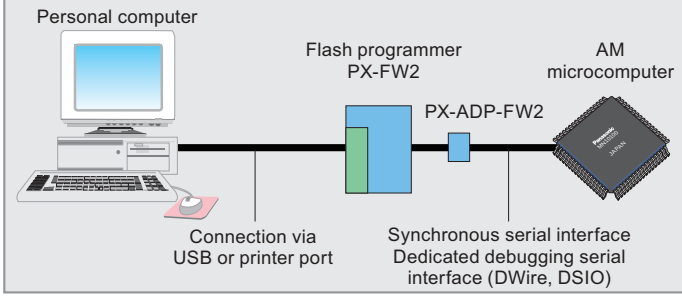
*1: Indicates internal operating frequency in microcomputer. Frequency may vary by model.
*2: Figures in parentheses represent options that can be specified at time of order.
*3: Does not interfere with target program execution.
*4: May stop target program execution briefly.

Flash Programmer (PX-FW2)

Single unit supports both adapter-based parallel and onboard serial programming

- This is a tool for reading out or programming the contents of the flash memory in an AM Series microcomputer. This single unit supports both adapter-based parallel operation using a Programming adapter and onboard serial operation using the microcomputer's serial communications functions.
- May be connect to a computer via USB or printer port. (Printer port connection cable sold separately.)
- Data to be written can be loaded into the flash programmer in advance to allow programming to flash memory without the flash programmer being connected to the personal computer.

Onboard serial programming connections



■Development Support Tools

Please see the following Web site about information on the development tool.

Information on tool whole
http://www.semicon.panasonic.co.jp/e-micom/support.html
Product support list
http://www.semicon.panasonic.co.jp/e-micom/hardtool/tool_list.html
Inquiry
http://www.semicon.panasonic.co.jp/e-micom/qa.html

●AM1 (MN101) Series of 8-bit Microcontroller

Tool Name	AM13 (MN101C) Series	AM13E (MN101E) Series
Compiler and Assembler	ANSI C compiler with extensions for 8-bit microcomputers (8-bit internal computation and bit fields within chars)	
Debugger	DebugFactory® Builder	
Emulator	In-circuit emulator supporting real-time debugging with 224 KB (944 KB) of ROM and 16 KB (64KB) of RAM, trace function,break functions, etc. ( ):MN101E Series	
On-board Debugger	On-board debugging environment offering real-time debugging using the actual device Effective solution for field debugging and final product evaluation, including analog characteristics	
	Manufactured by OBJECT Co., Ltd. Memory reference/modification, breakpoints, etc.	
Software Simulator	Tool for debugging without the actual machine (DebugFactory® Builder)	

●AM3 (MN103) Series of 32-bit Microcontroller

Tool Name	AM32 (MN103S) Series	AM32L (MN103L) Series
Compiler and Assembler	ANSI-compliant C compiler, EC++-compliant compiler	
Debugger	DebugFactory® Builder	
Emulator	In-circuit emulator capable of real-time debugging	
	Emulation function for 1 MB of on-chip ROM and up to 4 MB of expansion RAM, trace function, breakpoint functions, etc.	Emulation function for 2 MB of on-chip ROM, 64 KB of on-chip RAM, and 1 MB (max. 2 MB) of expansion RAM, trace function, breakpoint functions, coverage function, etc.
On-board Debugger	On-board debugging environment offering real-time debugging using the actual device Effective solution for field debugging and final product evaluation, including analog characteristics	
	Memory reference/modification, breakpoints, trace function, etc. (depends on device's on-chip functionality)	Manufactured by OBJECT Co., Ltd. Memory reference/modification, breakpoints, etc.
Software Simulator	Tool for debugging without the actual machine (DebugFactory® Builder)	

●Operating Environment

Tool Name		Windows® 2000/XP(SP2 or later)/Vista	Red Hat Enterprise Linux 4
Compiler and Assembler	AM1 Series	○*1	—
	AM3 Series	○*1	○
DebugFactory® Builder Emulator Flash Programmer (PX-FW2)		○	—

*1: In a command prompt.

●Package - Surface Mount Socket

Package code	Panasonic number	Remarks		Distributor
QFP044-P-1010	PRB-SKT44QF10			Panasonic Corporaion
QFP084-P-1818	PRB-SKT84QF18			
QFP100-P-1818	PRB-SKT100QF18	Plastic package exclusive use		
Package code	**Panasonic number**	**Socket manufacturer catalog number**		**Distributor**
TQFP032-P-0707	———	HQPACK032SA	NQPACK032SA	Tokyo Eletech Corporation It is possible to order by the Panasonic number.
SSOP032-P-0300	———	HSPACK32BK	NSPACK32BK	
QFP044-P-1010F	PRB-TET44QF10F*1	HQPACK044SA	NQPACK044SA	
QFH048-P-0707 TQFP048-P-0707B	PRB-TET48TH07	HQPACK048SD	NQPACK048SD	
	PRB-TET48TH07-SL	HQPACK048SD	NQPACK048SD-SL	
QFH064-P-1010	PRB-TET64TH10	HQPACK064SD	NQPACK064SD	
	PRB-TET64TH10-SL	HQPACK064SD	NQPACK064SD-SL	
LQFP064-P-1414	PRB-TET64LF14	HQPACK064SA160	NQPACK064SA160	
	PRB-TET64LF14-SL	HQPACK064SA160	NQPACK064SA160-SL	
QFH080-P-1212 TQFP080-P-1212	PRB-TET80TH12	HQPACK080SD	NQPACK080SD-ND	
	PRB-TET80TH12-SL	HQPACK080SD	NQPACK080SD-ND-SL	
LQFP080-P-1414	PRB-TET80LF14	HQPACK080SB160	NQPACK080SB	
	PRB-TET80LF14-SL	HQPACK080SB160	NQPACK080SB-SL	
LQFP100-P-1414	PRB-TET100LF14	HQPACK100SD	NQPACK100SD-ND	
	PRB-TET100LF14-SL	HQPACK100SD	NQPACK100SD-ND-SL	
QFP100-P-1818	PRB-TET100QF18	HQPACK100SB	NQPACK100SB	
	PRB-TET100QF18-SL	HQPACK100SB	NQPACK100SB-SL	
LQFP112-P-2020	PRB-TET112LF20	HQPACK112SB	NQPACK112SB	
	PRB-TET112LF20-SL	HQPACK112SB	NQPACK112SB-SL	
TQFP128-P-1414	PRB-TET128LF14	HQPACK128SE	NQPACK128SE	
	PRB-TET128LF14-SL	HQPACK128SE	NQPACK128SE-SL	
LQFP128-P-1818	PRB-TET128LF18	HQPACK128SD	NQPACK128SD	
	PRB-TET128LF18-SL	HQPACK128SD	NQPACK128SD-SL	
QFP160-P-2828	PRB-TET160QF28	HQPACK160SB	NQPACK160SB	
	PRB-TET160QF28-SL	HQPACK160SB	NQPACK160SB-SL	
QFP208-P-2828	PRB-TET208QF28H	HQPACK208SD306H	NQPACK208SD	

*1 : Lead-free package
-SL : Screw reinforcement from solder fixation + back of substrate

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