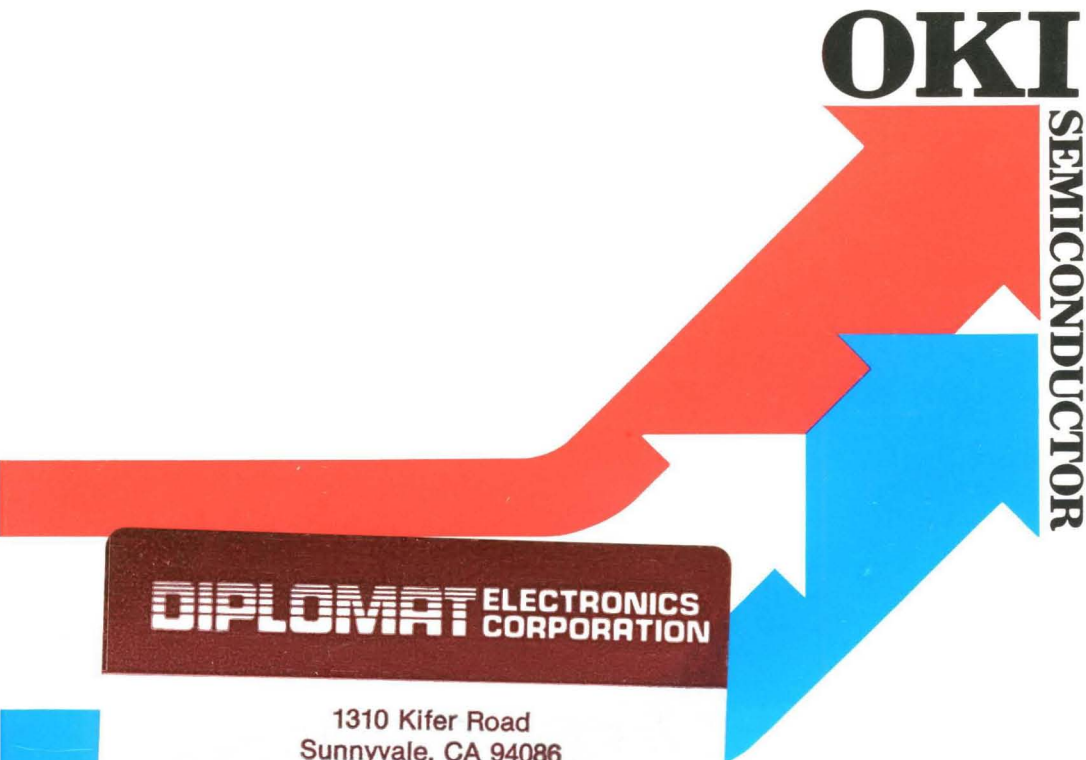
LCD DRIVER/CONTROLLER DATABOOK 1986



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CONTENTS

PRODUCT LINE-UP

1 PRODUCT LINE-UP

APPLICATION	TYPE NO	FUNCTION	OUTPUT		DUTY	PACKAGE	REMARKS
			COMMON	SEGMENT			
STATIC LCD DRIVER	MSM58292	static driver	5 digit (7 segment)		1/1	56 FLT.	
	MSM5219B	static driver	48 dot		1/1	60 FLT.	
	MSM5221	static driver	56 dot		1/1	80 FLT.	
	MSM5265	static driver	160 dot		1/1 or 1/2	100 FLT.	
DOT MATRIX LCD DRIVER	MSM5238	COMMON DRIVER	32	–	1/32 – 1/128	44 FLT.	
	MSM5839B	SEGMENT DRIVER	–	40	1/8 – 1/128	56 FLT.	
	MSM5259	SEGMENT DRIVER	–	40	1/1 – 1/16	56 FLT.	use with MSM6222B-01
	MSM5260	COMMON/ SEGMENT DRIVER	80	80	1/1 – 1/128	100 FLT.	COMMON/ SEGMENT selectable
	MSM5278	COMMON DRIVER	64	–	1/8 – 1/128	80 FLT.	
	MSM5279	SEGMENT DRIVER	–	80	1/8 – 1/128	100 FLT.	
DOT MATRIX LCD CONTROLLER	MSM6222B -01	DRIVER/ CON- TROLLER	16	40	1/8 – 1/16	80 FLT.	with character generator ROM
	MSM6240	CON- TROLLER	–	–	1/32 – 1/144	60 FLT.	
	MSM6255	CON- TROLLER	–	–	1/2 – 1/256	80 FLT.	512K dot
	MSM6265	CON- TROLLER	–	–	1/100 x 2	80 FLT.	512K dot software compatible with CRT Controller

Note: 1. MSM5259 and MSM5260 can be used as static display dot drives like MSM5219B and so forth.
2. The duty of LCD module is determined by the performance of drivers and the material of LCD panel. So, to select suitable LCD driver for superior display, it is necessary to study the material of the LCD panel.

PACKAGING

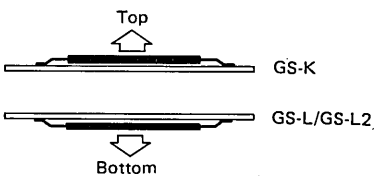
PACKAGING

2

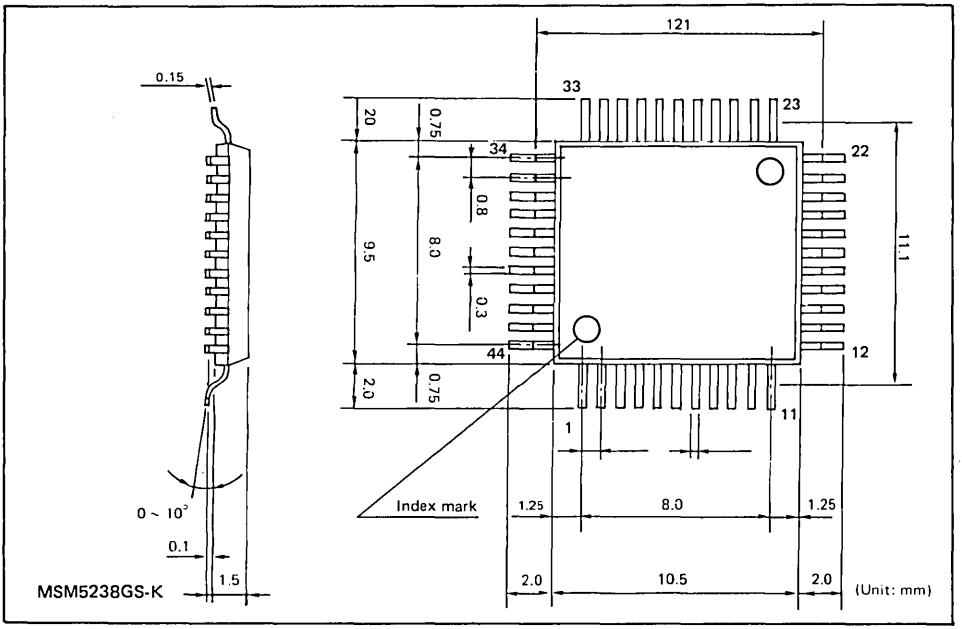
	PRODUCT	PLASTIC FLAT PACKAGE (No. of Pins)	GS-K	GS-L	GS-L2
STATIC LCD DRIVER	MSM58292	56 (small)	○		
	MSM5219B	60	○		
	MSM5221	80	○		
	MSM5265	100	○		
DOT MATRIX LCD DRIVER	MSM5238	44	○		○
	MSM5839B	56 (small)	○		○
	MSM5259	56 (small)	○		○
	MSM5260	100	○	○	
	MSM5278	80	○		
	MSM5279	100	○		
DOT MATRIX LCD CONTROLLER	MSM6222B-01	80		○	
	MSM6240	60	○		
	MSM6255	80	○		
	MSM6265	80	○		

Note: Model names suffixed by GS denote plastic mold flat package, while -K, -L or -L2 denote the direction of the lead bent.

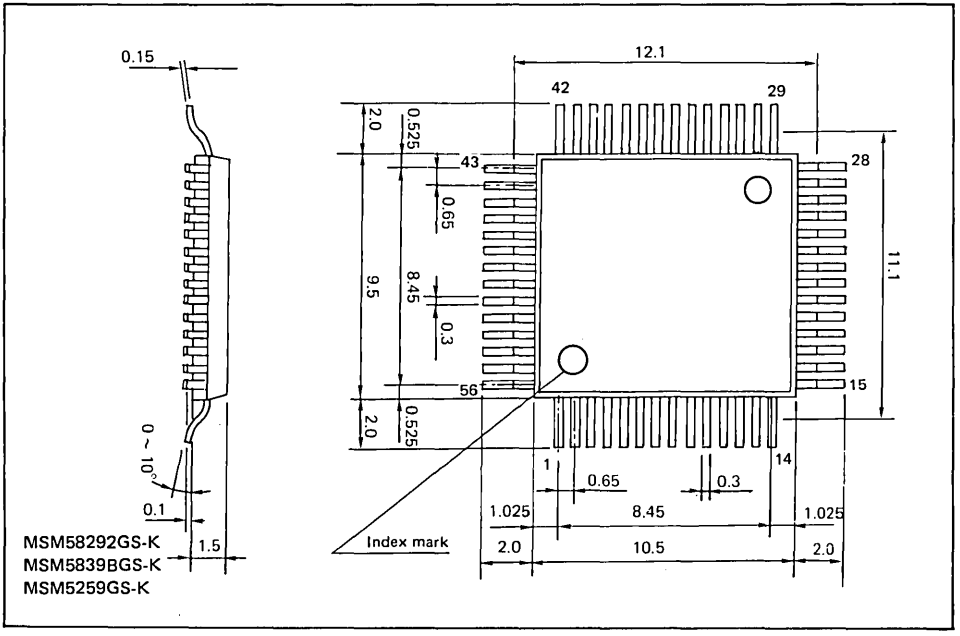
Plastic Flat Package Variations



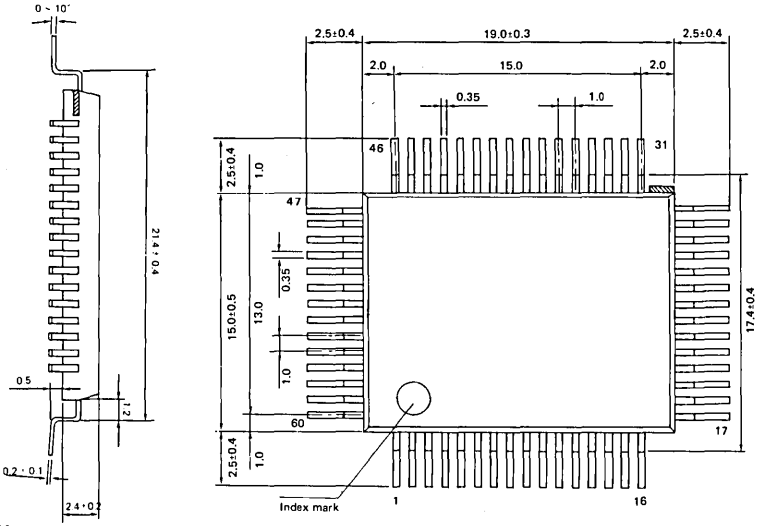
• 44 PIN PLASTIC FLAT PACKAGE



• 56 PIN PLASTIC FLAT PACKAGE

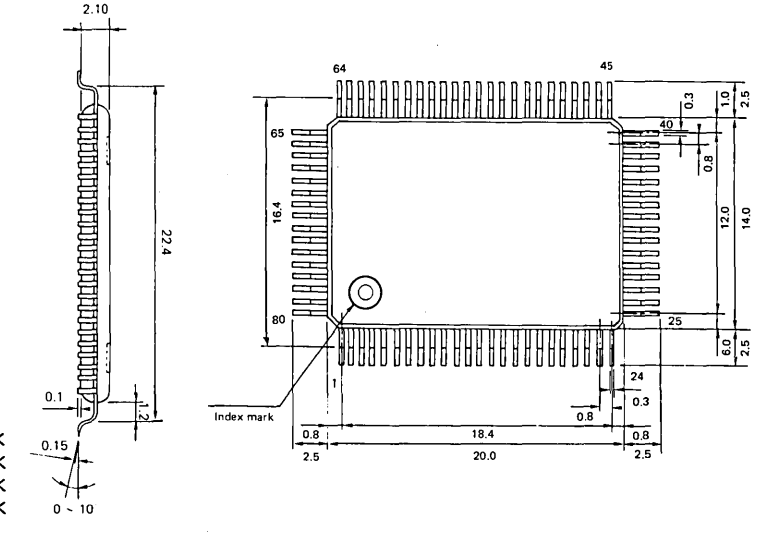


• 60 PIN PLASTIC FLAT PACKAGE



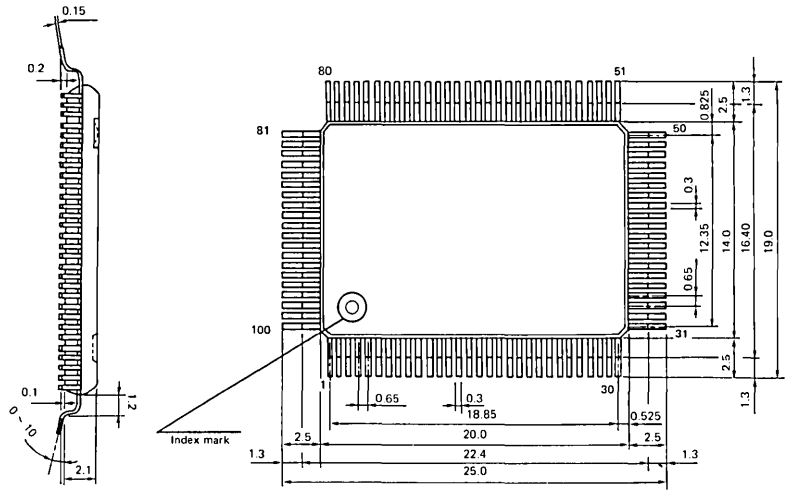
MSM5219BGS-K
MSM6240GS-K

• 80 PIN PLASTIC FLAT PACKAGE



MSM5221GS-K
MSM5278GS-K
MSM6255GS-K
MSM6265GS-K

• 100 PIN PLASTIC FLAT PACKAGE

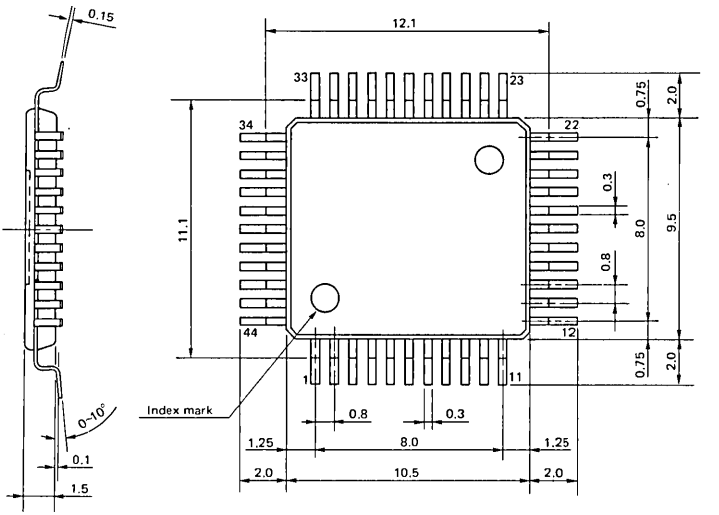


MSM5265GS-K
MSM5260GS-K
MSM5279GS-K

2

• 44 PIN PLASTIC FLAT PACKAGE (LEAD BENT OPPOSITE DIRECTION)

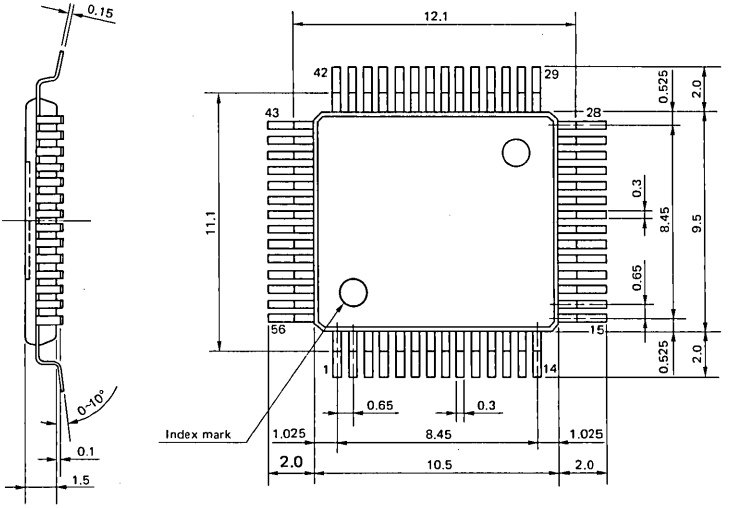
(Unit: mm)



MSM5238GS-L2

• 56 PIN PLASTIC FLAT PACKAGE (LEAD BENT OPPOSITE DIRECTION)

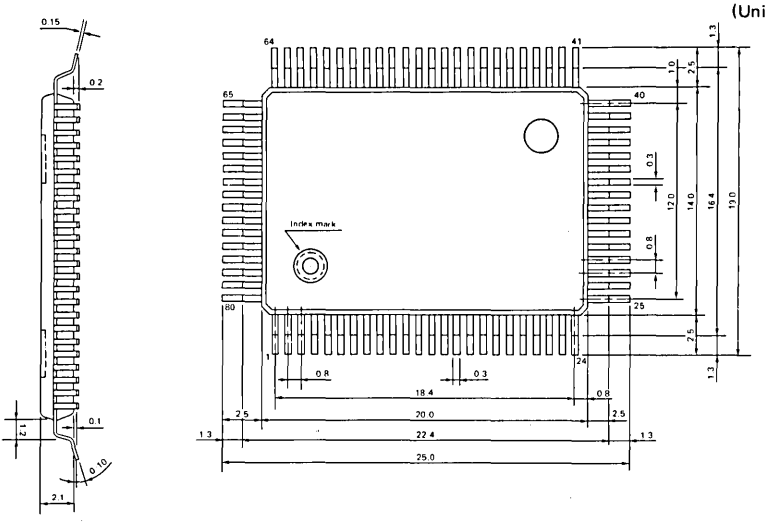
(Unit: mm)



MSM5839BGS-L2
MSM5259GS-L2

• 80 PIN PLASTIC FLAT PACKAGE (LEAD BENT OPPOSITE DIRECTION)

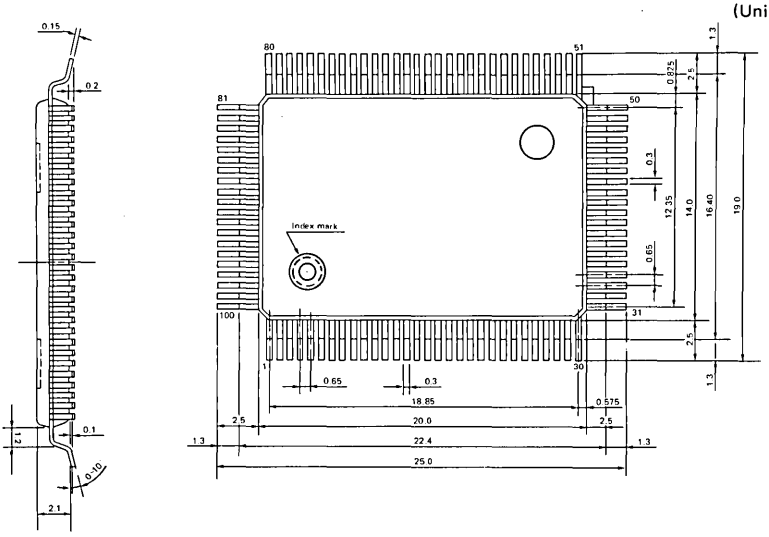
(Unit: mm)



MSM6222B-01GS-L

• 100 PIN PLASTIC FLAT PACKAGE (LEAD BENT OPPOSITE DIRECTION)

(Unit: mm)



MSM5260GS-L

DATA SHEET

3

STATIC LCD DRIVER

MSM58292GS

5-DIGIT STATIC LCD DRIVER

GENERAL DESCRIPTION

The OKI MSM58292GS is a 7-segment static LCD driver LSI which is fabricated by low power CMOS metal gate technology. This LSI consists of 32-bit shift register, 32-bit latch, 5 sets of 7-segment decoder and LCD drivers.

It receives the serial display data from the microcomputer etc, converts it to a parallel data, then output to the 7-segment LCD panel.

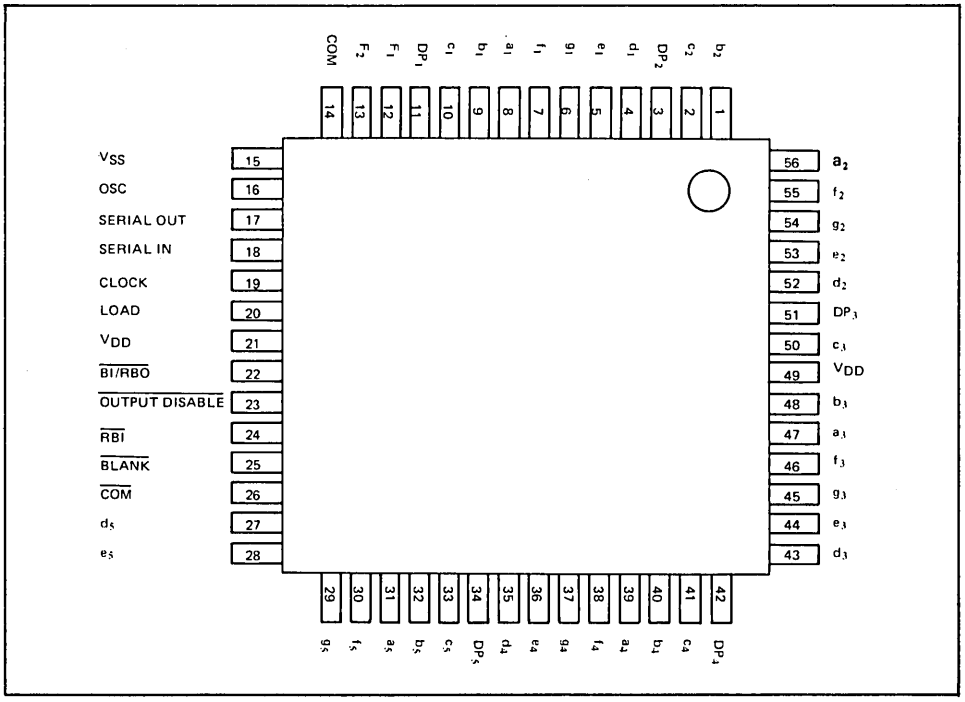
The input code for each digit is a 4-bot binary code. The input codes are decoded into digits 0 ~ 9 and alphabetic letters A ~ F, to display hexadecimal numbers. The expansion of display can be easily made by using another MSM58292GS in cascade connection.

The MSM58292GS can directly drive the LCD panel, as the AC driving circuit is integrated on the chip.

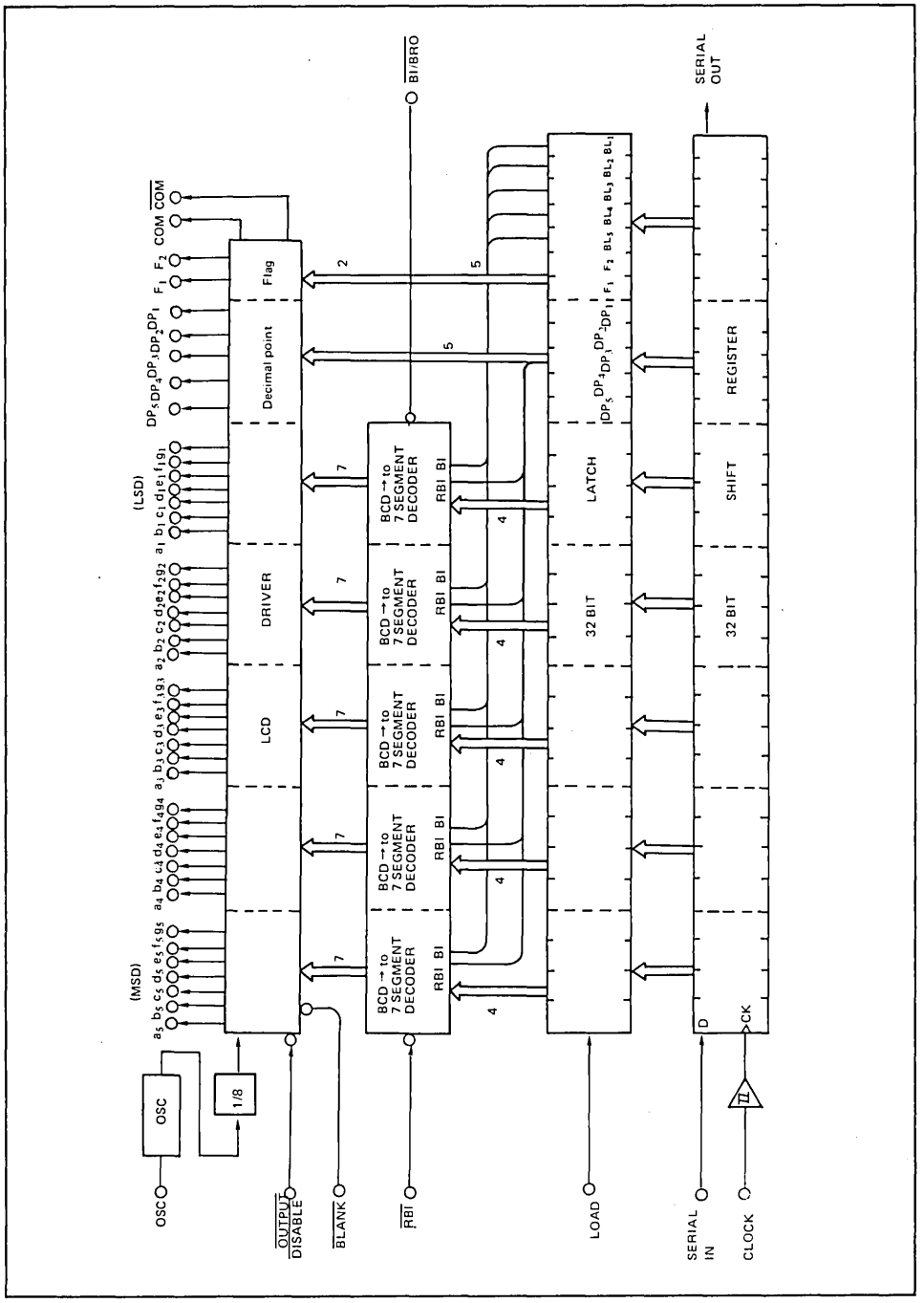
FEATURES

- 5 digit 7-segment LCD display
- Serial input from the microcomputer etc.
- Expansion of display by cascade connection
- Supply voltage: 3 ~ 7V
- 56 pin plastic flat package

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Limits	Unit
Supply voltage	V_{DD}	T_a = 25°C	−0.3 ~ 7	V
Input voltage	V_I		−0.3 ~ V_{DD}	V
Storage temperature	Tstg	—	−55 ~ +150	°C

3

OPERATING RANGE

Item		Symbol	Condition	Limits	Unit
Supply voltage		V_{DD}	–	3 ~ 7	V
Operating temperature		T_{OP}	–	−30 ~ +85	°C
Fan out	$\overline{BI/RBO}$	N	MOS load	1	–
	SERIAL OUT	N	MOS load	40	–
			TTL load	1	–

DC CHARACTERISTICS

(V_{DD} = 5V ± 5%, T_a = −30 ~ +85°C)

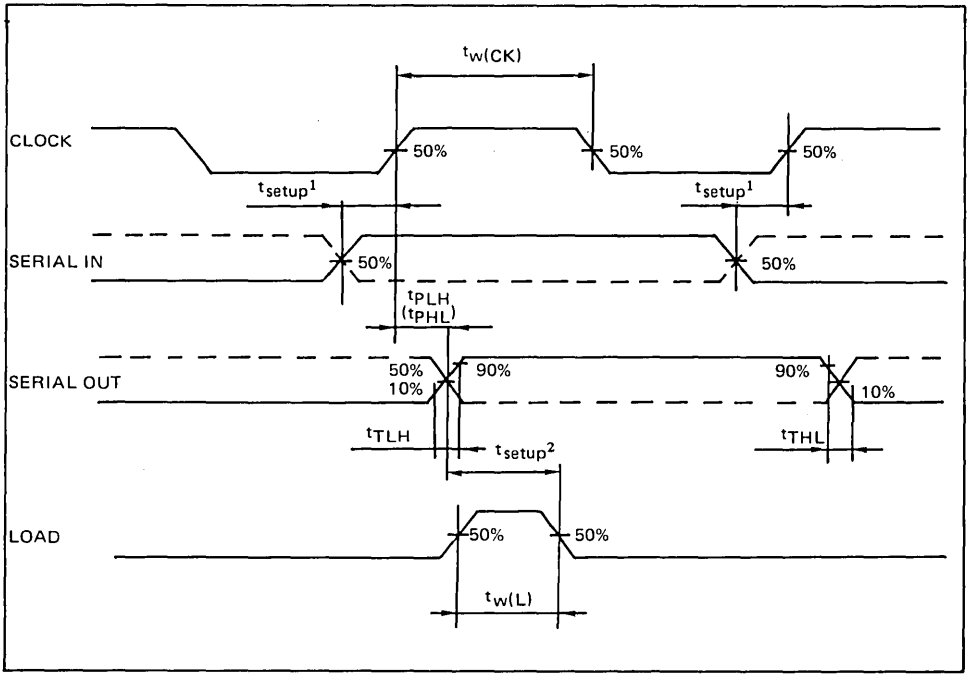
Item	Symbol	Condition	MIN	TYP	MAX	Unit
High Input voltage	V_{IH}	–	3.6	–	–	V
Low Input voltage	V_{IL}	–	–	–	0.8	V
High Output voltage[1]	V_{OH}	I_O = −5 μA	4.95	–	–	V
Low Output voltage[1]	V_{OL}	I_O = 5 μA	–	–	0.05	V
High Output voltage[2]	V_{OH}	I_O = −40 μA	4.2	–	–	V
Low Output voltage[2]	V_{OL}	I_O = 1.6mA	–	–	0.4	V
High Output voltage[3]	V_{OH}	I_O = −500 μA	4.5	–	–	V
Low Output voltage[3]	V_{OL}	I_O = 500 μA	–	–	0.5	V
High Output voltage[4]	V_{OH}	I_O = −250 μA	4.5	–	–	V
Low Output voltage[4]	V_{OL}	I_O = 250 μA	–	–	0.5	V
Input current[5]	I_{IH}/I_{IL}	$V_I = V_{DD}/V_I$ = 0V	–	–	1/−1	μA
Output current[1]	I_{OH}/I_{OL}	V_O = 0V /$V_O = V_{DD}$	−0.2/ 0.2	–	–	mA
Output current[2]	I_{OH}/I_{OL}	V_O = 2.5V/V_O = 0.4V	−0.2/ 1.6	–	–	mA
$\overline{BI/RBO}$ short-circuit current	I_{OH}/I_{OL}	V_O = 0V /$V_O = V_{DD}$	−10/ 10	–	−500/ 500	μA
Dynamic current consumption	I_{DD}	f(OSC) = 360Hz no load	–	–	500	μA

Note 1: Applied to the output pins excluding the SERIAL OUT, $\overline{BI/RBO}$, $\overline{COM}$ and COM Pins.
Note 2: Applied to the SERIAL OUT pin.
Note 3: Applied to the COM pin.
Note 4: Applied to the COM pin.
Note 5: Applied to the input pins excluding the OSC pin.

SWITCHING CHARACTERISTICS

(V_{DD} = 5V, T_a = 25°C, CL = 15pF)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Propagation delay time (for a shift in the shift register)	t_{PHL} t_{PLH}	–	–	–	1000	nS
SERIAL OUT rise/fall time	t_{THL} t_{TLH}	–	–	–	300	nS
Maximum clock frequency	$f_{(CK)\ max}$	–	1	–	–	MHz
Minimum clock pulse width	$t_{w(CK)}$	–	–	–	500	nS
Minimum load pulse width	$t_{w(L)}$	–	–	–	500	nS
Data setup time SERIAL IN → CLOCK	t_{setup}^{1}	–	–	–	250	nS
Data setup time SERIAL OUT → LOAD	t_{setup}^{2}	–	–	–	500	nS



FUNCTION TABLE

Hexadecimal digit	$\overline{RBI}$	$\overline{BI/RBO}$	SEGMENT OUT (Note 1)							Display
			a	b	c	d	e	f	g	
*	*	L	L	L	L	L	L	L	L	(Note 3)
0	*	(Note 2)	L	L	L	L	L	L	L	(Note 4)
0	*	H	H	H	H	H	H	H	L	0
1	*	H	L	H	H	L	L	L	L	1
2	*	H	H	H	L	H	H	L	H	2
3	*	H	H	H	H	H	L	L	H	3
4	*	H	L	H	H	L	L	H	H	4
5	*	H	H	L	H	H	L	H	H	5
6	*	H	H	L	H	H	H	H	H	6
7	*	H	H	H	H	L	L	L	L	7
8	*	H	H	H	H	H	H	H	H	8
9	*	H	H	H	H	H	L	H	H	9
A	*	H	H	H	H	L	H	H	H	A
B	*	H	L	L	H	H	H	H	H	b
C	*	H	H	L	L	H	H	H	L	C
D	*	H	L	H	H	H	H	L	H	d
E	*	H	H	L	L	H	H	H	H	E
F	*	H	H	L	L	L	H	H	H	F

Note 1: The H indicates that the segment is displayed, and the L indicates that the segment is not displayed. The H is an antiphase output of the COM output, and the L is an in-phase output of the COM output.

Note 2: The $\overline{RBI}$/$\overline{RBO}$ pin goes to low level only when the $\overline{RBI}$ pin is at a low level and all the digit are 0 (the display is blank).
If the $\overline{BI/RBO}$ pin is forcibly turned to high level, 0 at LSD is displayed.

Note 3: If the $\overline{BI/RBO}$ pin is forcibly turned to low level, the LSD is made blank.

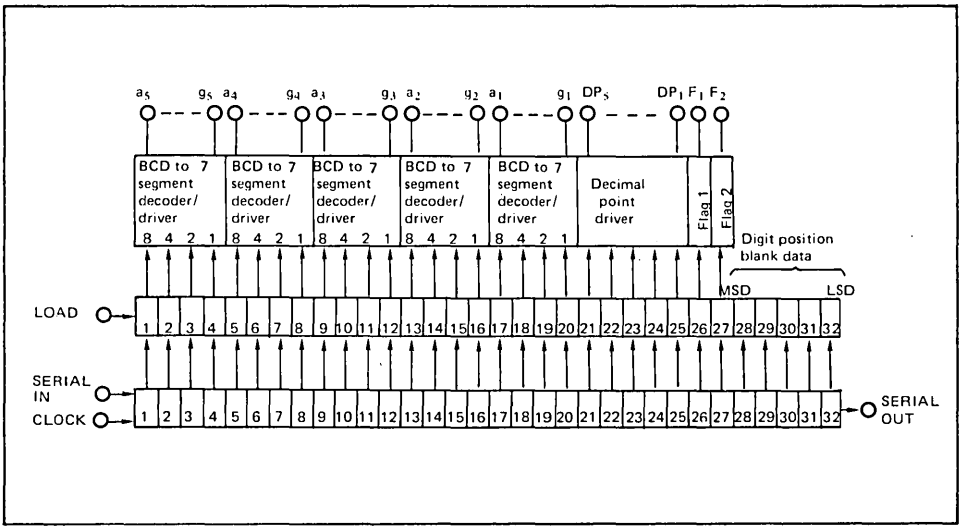
Note 4: If the $\overline{RBI}$ pin is turned to low level, the display is placed in the leading zero blanking status, in which the contiguous 0s preceding the MSD are made blank.

FUNCTIONAL DESCRIPTION

- **SERIAL IN**

  The SERIAL IN pin is a shift register data input pin. The display data are input to this pin synchronized with the clock pulses. The data are input in the order of blank data, flag data, decimal point data, then numeric data (beginning with the LSB) (positive logic).

< Data input procedure >



- **SERIAL OUT**

  The SERIAL OUT pin is a shift register serial output pin. The data input to the SERIAL IN pin is output from this pin synchronised with the clock pulses, with a delay of the total bit count of the shift register (32 bits). This pin is used for extension of digit display capacity.

- **CLOCK**

  The CLOCK pin is a synchronizing pulse input pin used for data input to the shift register or data output from the shift register. The data is shifted at the rising edge (low to high) of each clock pulse. A Schmitt trigger circuit is employed as the CLOCK input circuit (the hysteresis is approximately 0.5V).

- **LOAD**

  The LOAD pin is an input pin for latching the shift register contents. When this pin is at high level, the shift register contents are transferred to the decoders, and when this pin is at low level, the last data to be transferred from the shift register when this pin was at high level is held, so that the display contents are not changed with the change of the shift register contents.

- **$\overline{\text{RBI}}$**

  The $\overline{\text{RBI}}$ PIN is an input pin for suppressing the display of leading 0s. When this pin is at high level, the leading 0s, if any, are displayed; when this pin is at a low level, contiguous 0s preceding the MSD are not displayed. The $\overline{\text{RBI}}$ pin is connected to the decoder circuit for the MSD.

  Note: The DP_1 through DP_5 are not made blank.

- **$\overline{\text{BI}}/\overline{\text{RBO}}$**

  The $\overline{\text{BI}}/\overline{\text{RBO}}$ pin is used for both input and output. As an input pin, the input level can forcibly be set to low regardless of the output level, since the output resistance is treat.

  1 For use as an output pin $\overline{\text{RBO}}$

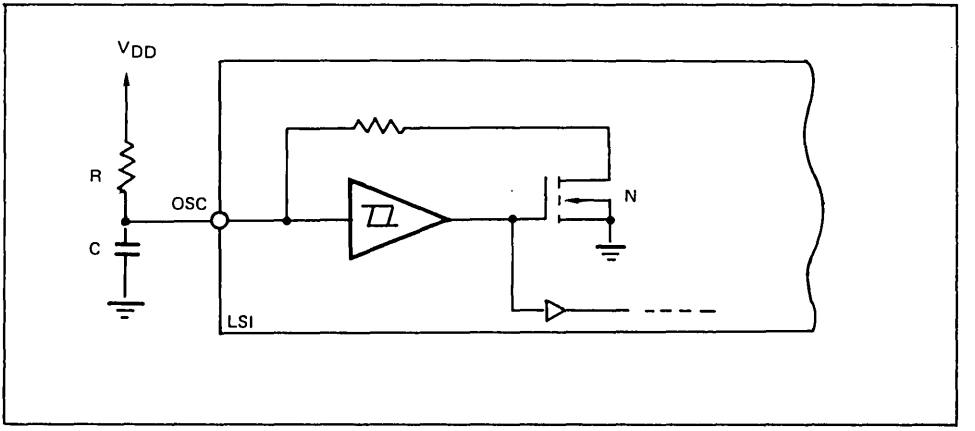
  When the $\overline{\text{RBI}}$ pin is turned to low level, if all the digits are 0s, the display is made blank and the $\overline{\text{RBO}}$ pin is turned to low level. If the $\overline{\text{RBI}}$ pin is at high level or a number including some significant digits is displayed, the $\overline{\text{RBO}}$ pin is turned to high level. If two MSM58292GS chips are connected for extension of the digit display capacity, the $\overline{\text{RBO}}$ pin of the first chip is connected to the $\overline{\text{RBI}}$ pin of the second chip, which connects to the MSD of the second chip, so that all the continguous 0s preceding the MSD are made blank.

2 For use as an input pin $\overline{BI}$
The $\overline{BI}$ pin is connected to the decoder circuit for the LSD. Therefore, if this pin is turned to low level, only the LSD digit is made blank. Since this pin is also used as an output pin $\overline{ROB}$, some current indicated in the rating flows when this pin is set to low level. level.
The $\overline{BI}$ pin may be open when not used.
Note: The DP_1 through DP_5 are not made blank.

- **SEGMENT OUT (a_1–g_5, DP_1–DP_5, F_1, F_2)**
The SEGMENT OUT pins are output pins for driving the seven segments of digits (a_1 – g_5), decimal points (DP_1–DP_5), and flags (F_1 and F_2) on the display device.
The seven segment outputs (a – g) for each digit are used to display a digit 0–9 or an alphabetic letter A – F.

- **OSC**
The OSC pin is an input pin for a signal generator circuit which outputs AC signals required for driving a LCD panel. The oscillator starts to generate AC signals only by connecting a resistor and a capacitor to the OSC pin as shown in the figure below.

$f_{(OSC)}$ = 360 Hz when the V_{DD} = 5V, C = 0.068μF, and R = 100 kΩ



- **COM, $\overline{COM}$**
The COM pin is an output pin for sending an anti-phase signal of the seven segment outputs required for AC-driving the LCD panel. The COM output drives the COMMON pin on the LCD panel.
The $\overline{COM}$ pin is an output pin for sending an in-phase signal of the seven segment outputs (antiphase of the COM pin). This pin is not necessary in general display.
Both the COM and $\overline{COM}$ pins output square waves whose frequency is one eighth of the oscillator output appearing at the OSC pin (with a duty factor of 50%).

- **$\overline{OUTPUT\ DISABLE}$**
The $\overline{OUTPUT\ DISABLE}$ pin is an input pin for control of the COM pin. Setting this pin to high level places the COM pin in the normal status (the COM pin is used as an ordinary output pin), and setting this pin to low level makes the COM pin impedance high, so that the COM pin can be used as an input pin.
When two MSM58292GS chips are interconnected in a cascade, the $\overline{OUTPUT\ DISABLE}$ pin of the second chip is set to low level and the COM pin is used as an input pin.

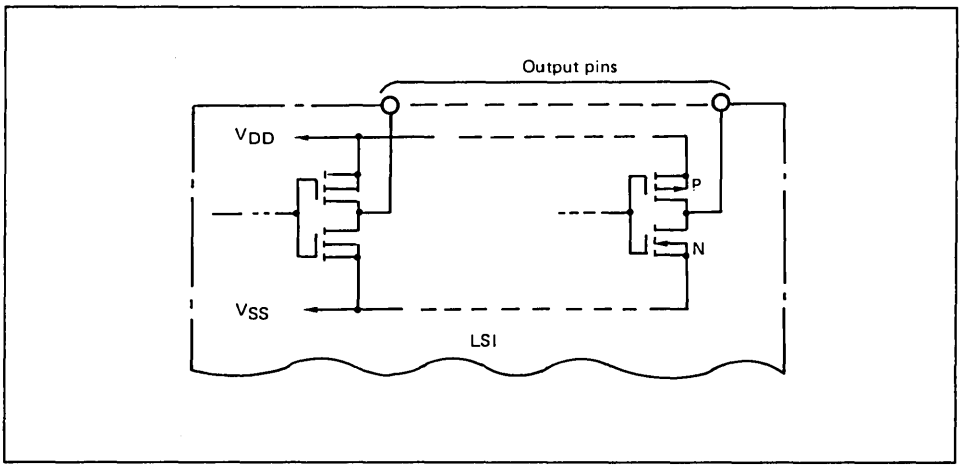
- **$\overline{\text{BLANK}}$**
  The $\overline{\text{BLANK}}$ pin is an input pin for making the display blank. Setting this pin to high level makes normal display, and setting this pin to low level makes the entire display blank.

- **Blanking a specific digit position**
  Any given digit position of the 5 digit display can be made blank by setting the MSM58292GS to ON. A specific digit position can be made blank by setting a bit of the shift register bits 28-32, as shown in the table below.

Shift register bit setting	Digit position which is made blank
Set bit 28 to 1	Digit position with segments $a_5 - g_5$ (MSD)
Set bit 29 to 1	Digit position with segments $a_4 - g_4$
Set bit 30 to 1	Digit position with segments $a_3 - g_3$
Set bit 31 to 1	Digit position with segments $a_2 - g_2$
Set bit 32 to 1	Digit position with segments $a_1 - g_1$ (LSD)

- **Decimal points**
  A digit position for which a decimal point has been specified is not subject to zero blanking even though that digit position contains the value 0. A decimal point can be used as a flag by setting the blank bit corresponding to that digit position to 1 to suppress the a – g segment display of that digit position (when the $\overline{\text{RBI}}$ pin is at low level).

- **Output circuit**
  Each output pin consists of a CMOS FET, and the $\overline{\text{BI}}/\overline{\text{RBO}}$ pin and SERIAL OUT pin output signals at high or low level.
  The output pins for display (for segments, decimal points, and flags) output pulse signals which are antiphase of the COM pin output when displaying, and output pulse signals which are in-phase of the COM pin output when not displaying. The output pins for display can directly drive the LCD panel.



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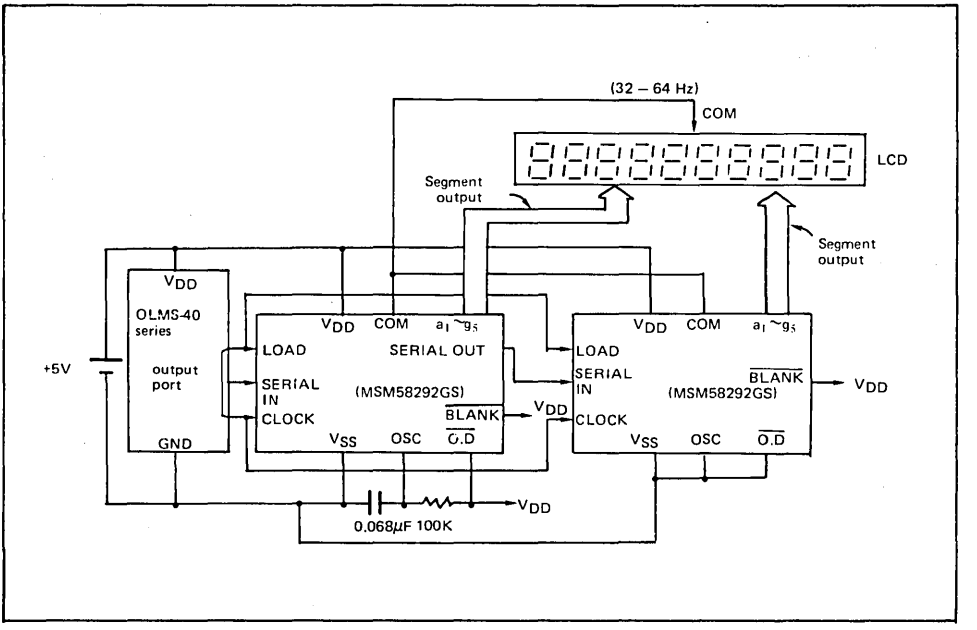
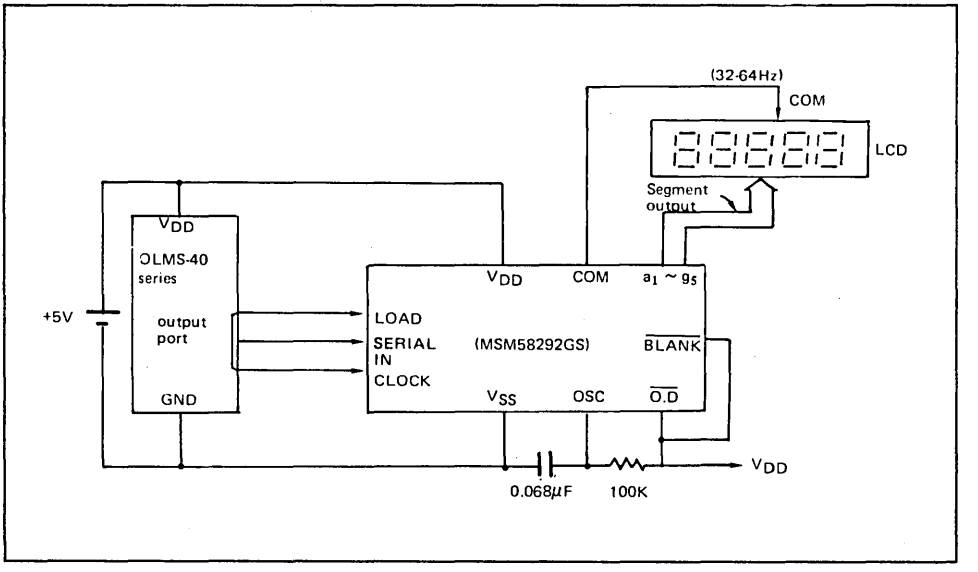
- **Application circuit**

I. 10 digit display (using two MSM58292GSs, cascade connection)



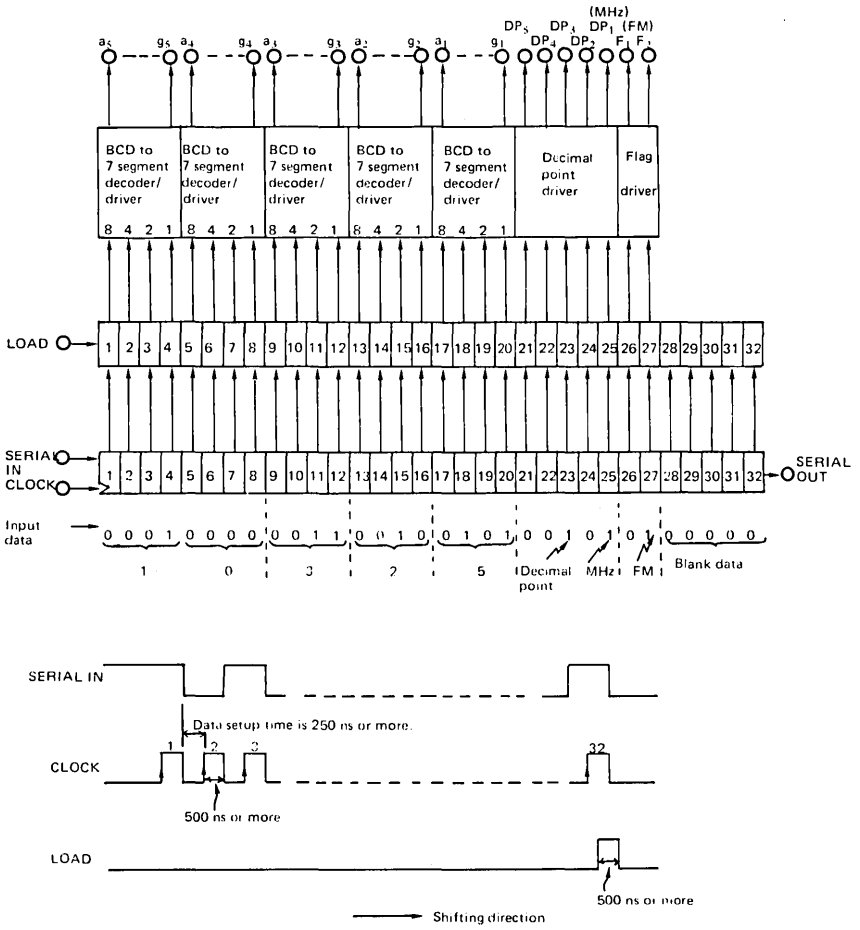
Note: $\overline{\text{O.D}}$ is the abbreviation of $\overline{\text{OUTPUT DISABLE}}$.

II. 5 digit display



Note: $\overline{\text{O.D}}$ the abbreviation of $\overline{\text{OUTPUT DISABLE}}$.

● **Data input example (FM 103.25 MHz)**



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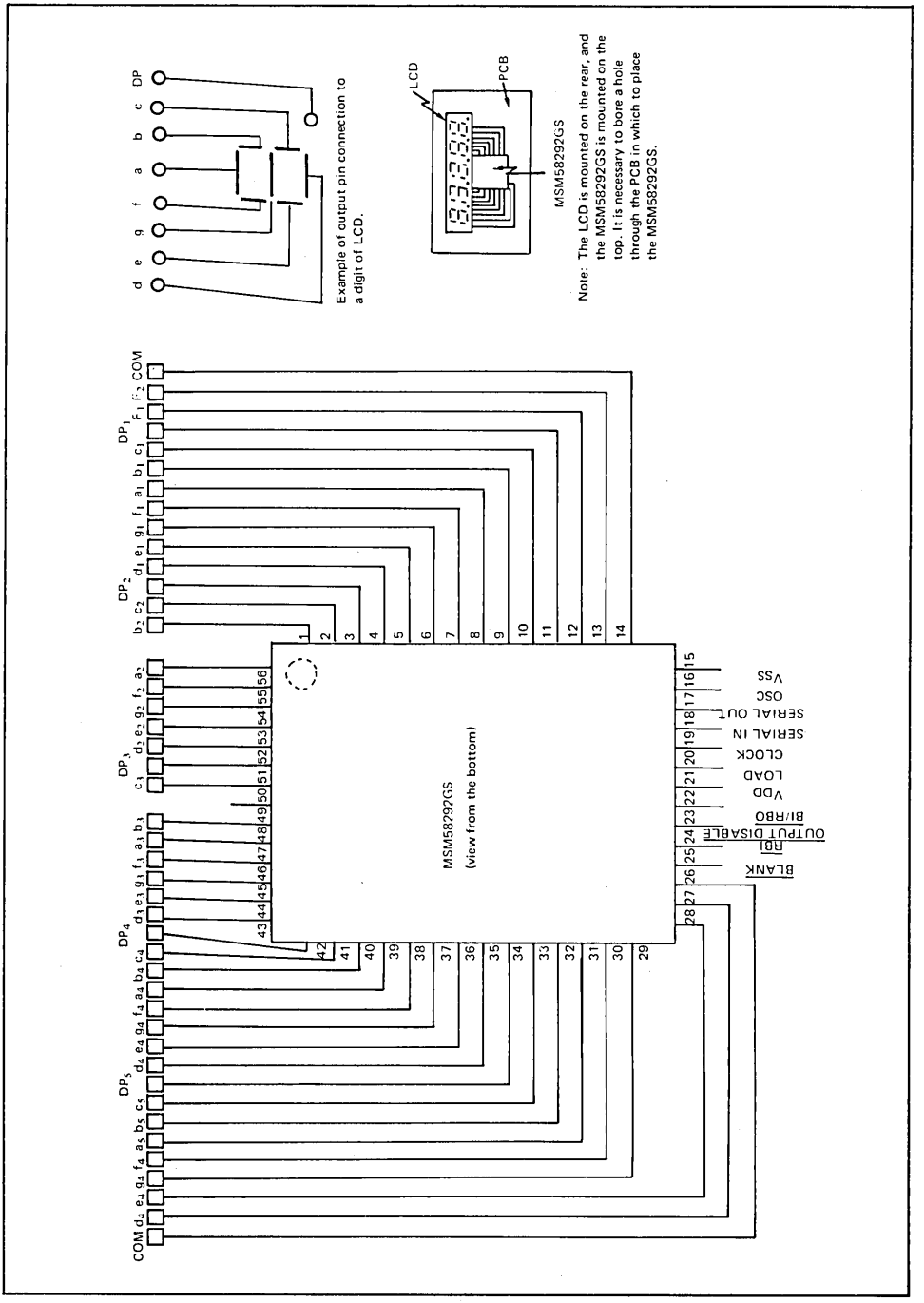
Example of interconnection with LCD



MSM5219BGS

48-DOT STATIC LCD DRIVER

GENERAL DESCRIPTION

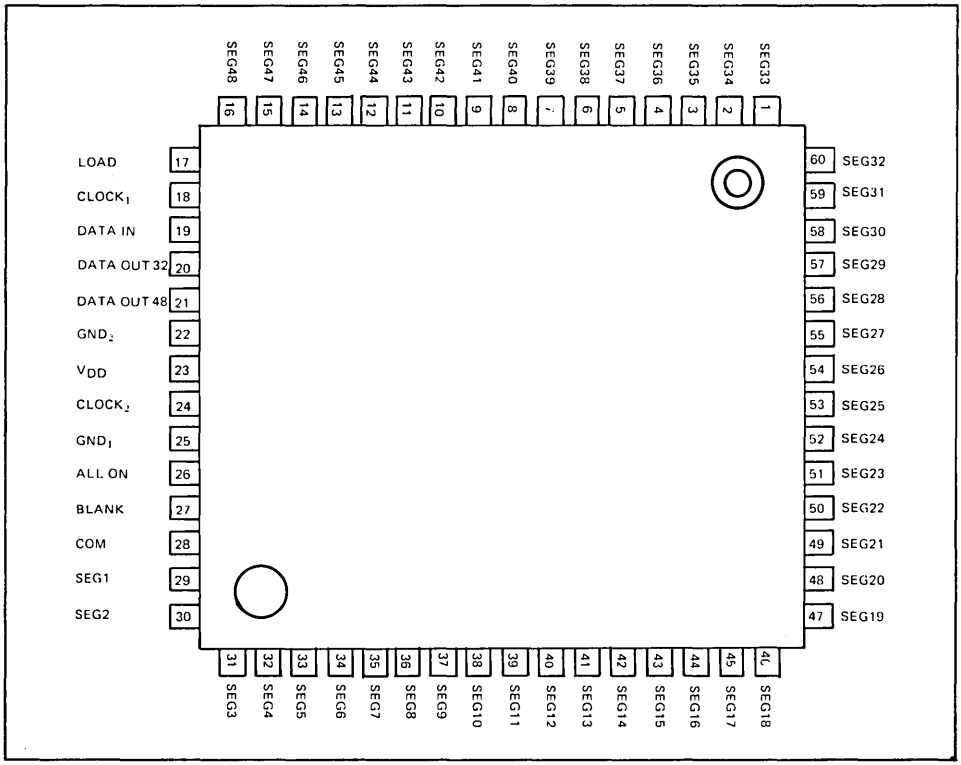
The OKI MSM5219BGS is a 48 dot static LCD driver which is fabricated by low power CMOS metal gate technology. This LSI consists of 48-bit shift register, 48-bit latch and 48-bit LCD driver. The display data, which was input to the 48-bit shift register, is shifted to the 48-bit latch by the LOAD signal. Then the data is output to the LCD panel through the 48-bit LCD driver.

FEATURES

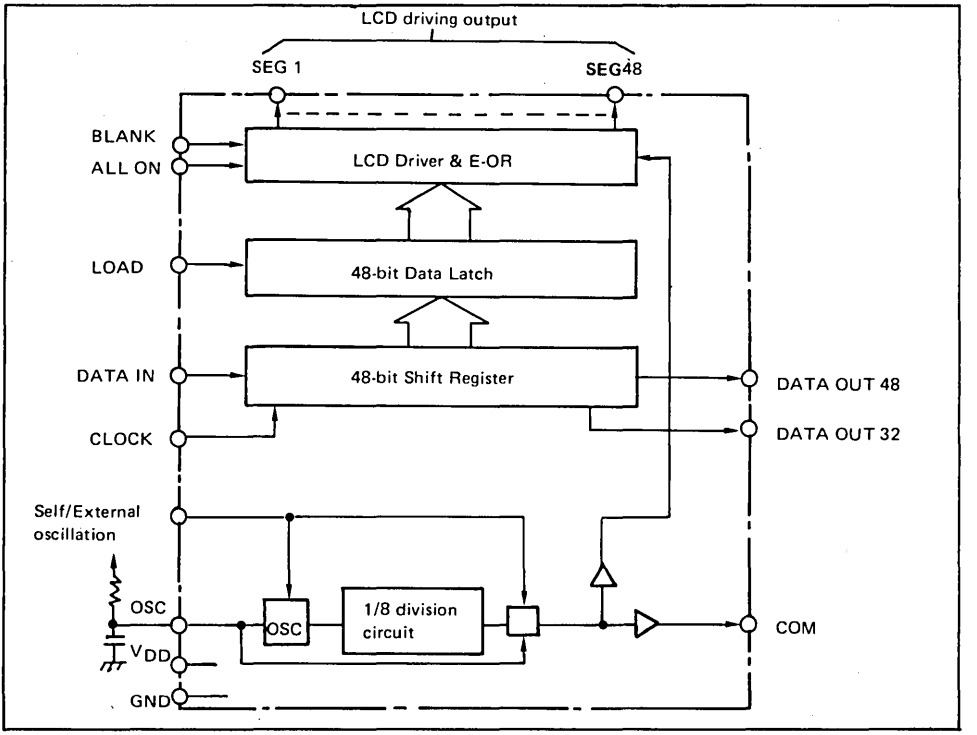
- 48 dots static LCD driving capability
- Simple interface with microcomputer chip (controlled by three input signals)
- Bit-to-bit correspondence between the input and the output
- Cascade connection capability
- LCD driving AC frequency is directly input externally
- Applicable as an output expander
- Supply voltage: 3 ~ 7V
- 60 pin plastic flat package (bent lead)

PIN CONFIGURATION

(Top View) 80 Lead Plastic Flat Package



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Limits	Unit
Supply voltage	$V_{DD} - V_{SS}$	T_a = 25°C	−0.3 ~ +7	V
Input voltage	V_I	T_a = 25°C	V_{SS} − 0.3 ~ V_{DD} + 0.3	V
Storage temperature	T_{stg}	—	−55 ~ +150	°C

OPERATING RANGE

Item	Symbol	Condition	Limits	Unit
Supply voltage	$V_{DD} - V_{SS}$	Self-Oscillation circuit	4 ~ 7	V
		External oscillation	3 ~ 7	V
Operating temperature	Top	—	−40 ~ +85	°C

DC CHARACTERISTICS

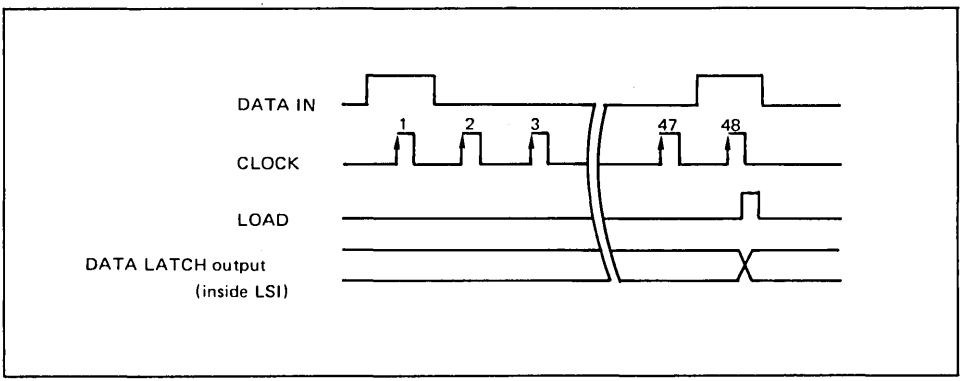
($V_{DD} - V_{SS}$ = 5V, T_a = −40 ~ +85°C)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
"H" Input voltage*1	V_{IH}	—	3.6	–	–	V
"L" Input voltage*1	V_{IL}	—	–	–	1.0	V
Input leakage current*1	I_{IH}/I_{IL}	V_I = 5V/V_I = 0V	–	–	1/−1	μA
SEG "H" Output voltage	V_{OHS}	I_O = −30μA	4.8	–	–	V
SEG "L" Output voltage	V_{OLS}	I_O = 30μA	–	–	0.2	V
COM "H" Output voltage	V_{OHC}	I_O = −150μA	4.8	–	–	V
COM "L" Output voltage	V_{OLC}	I_O = 150μA	–	–	0.2	V
SEG Output current 1	I_{OHS1}/I_{OLS1}	V_{OH} = 4.5V/V_{OL} = 0.5V	−100/100	–	–	μA
SEG Output current 2	I_{OHS2}/I_{OLS2}	V_{OH} = 1V/V_{OL} = 4V	−400/400	–	–	μA
COM Output current 1	I_{OHC1}/I_{OLC1}	V_{OH} = 4.5V/V_{OL} = 0.5V	−500/500	–	–	μA
COM Output current 2	I_{OHC2}/I_{OLC2}	V_{OH} = 1V/V_{OL} = 4V	−2/2	–	–	mA
"H" Output voltage*2	V_{OH}	I_O = −40μA	4.2	–	–	V
"L" Output voltage*2	V_{OL}	I_O = 1.6mA	–	–	0.4	V
Output current*2	I_{OH}/I_{OL}	V_O = 2.5V/V_O = 0.4V	−0.2/1.6	–	–	V
Clock pulse width	$t_{W\phi}$	*3	5	–	–	μS
		*4	0.5	–	–	
Max. clock pulse frequency	$f_{\phi MAX}$	*3	0.1	–	–	MHz
		*4	1	–	–	
Input signal rising/falling time	$t_{r\phi}$, $t_{f\phi}$	*5	–	–	5	μS
Static current consumption	I_{DD1}	—	–	–	100	μA
Active current consumption	I_{DD2}	No load when R_{OSC} = 150 kΩ, C_{OSC} = 0.015 μF	–	–	2	mA
COM Frequency (Self oscillation)	f_{COM}	No load when V_{DD} = 5V	25	–	300	Hz

*1: Applicable to all terminals except OSC. This condition is applied to OSC in the external oscillation mode.
*2: Applicable to DATA OUT 32, DATA OUT 48.
*3: Applicable to OSC.
*4: Applicable to CLOCK.
*5: Applicable to all terminals except OSC terminal.

FUNCTIONAL DESCRIPTION

- **Operational Description**
  The display data is input to the shift register by the DATA IN signal and CLOCK signal. It is transferred to the 48-bit latch by the LOAD signal and it is output to the LCD panel through 48-bit LCD driver.



- **$CLOCK_2$**
  The clock, which is used to generate the COM signal and the LCD driving signal, is input to this pin.

- **DATA IN $CLOCK_1$**
  DATA IN is a data input pin which enables the LCD to display when DATA IN pin is at high level. The 48-bit shift register is shifted at the rising edge of the CLOCK signal. Initially, the first bit of the shift register contains the current logic level of the DATA IN pin, and the bit N (N = 2 ~ 48) contains the data which was in bit N – 1 (N = 2 ~ 48) before the start of the operation. The data which was in bit 48 before the operation start is considered invalid.

- **LOAD**
  The data in the 48-bit shift register is shifted to the 48-bit latch when the LOAD pin set at high level, while the last data which was transferred to the latch when the LOAD pin was set at high level is constantly output when the LOAD pin is set at low level.

- **ALL SEG ON**
  When this pin is set at high level, all segments display turn on. This pin has the priority to the BLANK pin described as below.

- **BLANK**
  When this pin is set at high level, all segments display turn off. The ALL SEG ON pin has the priority over this pin.

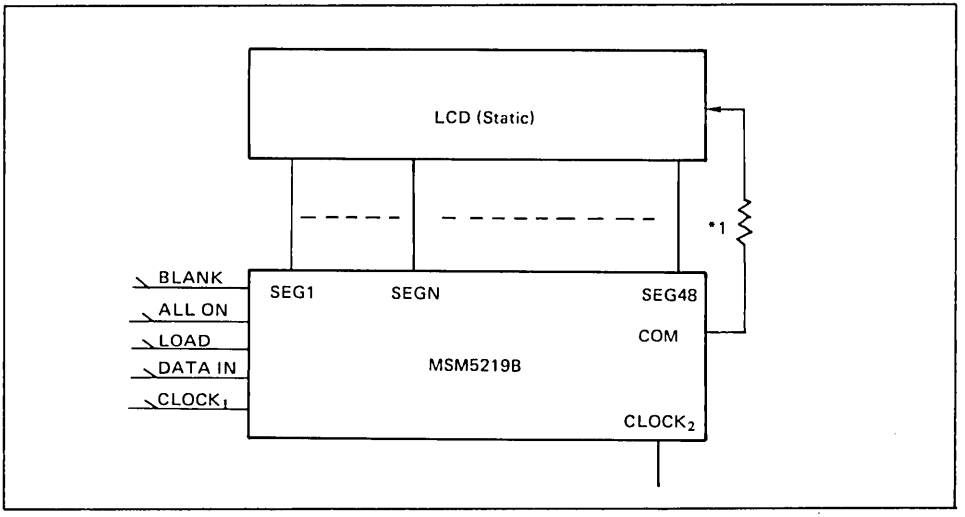
- **SEG1 ~ SEG48**
  LCD driving output pins. The reversed phase of the COM signal, which is used to display the data, is output from these pins when SEG1 ~ SEG48 are set at high level, while there is no display on the LCD when these pins are set at low level. The data which was input from the DATA IN pin is output from these pins to the LCD panel. The SEG N pin corresponds to the bit N of the shift register.

- **COM**
  Output terminal for the LCD. It is connected to the common side of the LCD.

- **DATA OUT 32, DATA OUT 48**
  Output pin of the shift register. It is used when the MSM5219BGS is connected in a series (cascade connection). It is connected to next MSM5219BGS's DATA IN terminal.

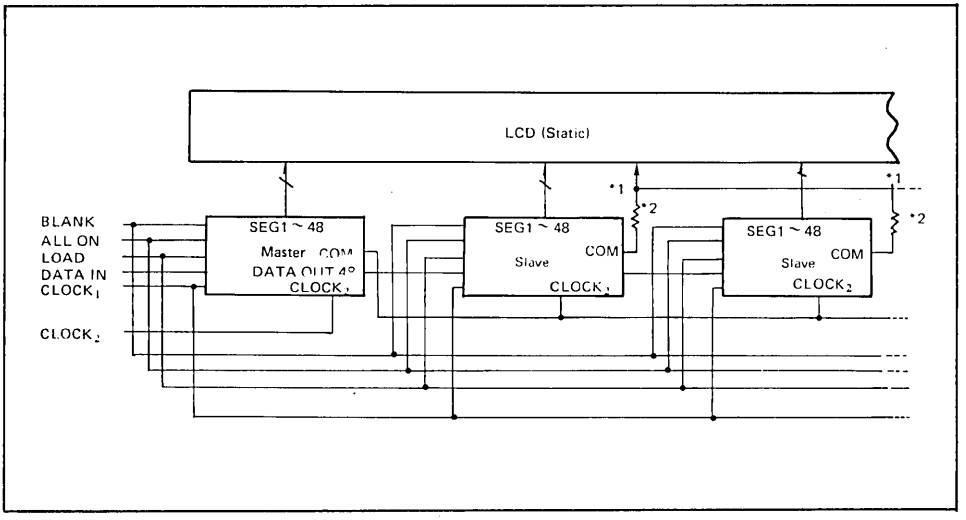
APPLICATION CIRCUIT

● **Single MSM5219BGS**



*1: When this IC is used under a strong external noise or large-capacity LCD load, this resistor prevents latch-up to be caused by a low output impedance of the COM pin.
The resistance is about 100Ω.

● **Cascade connection**

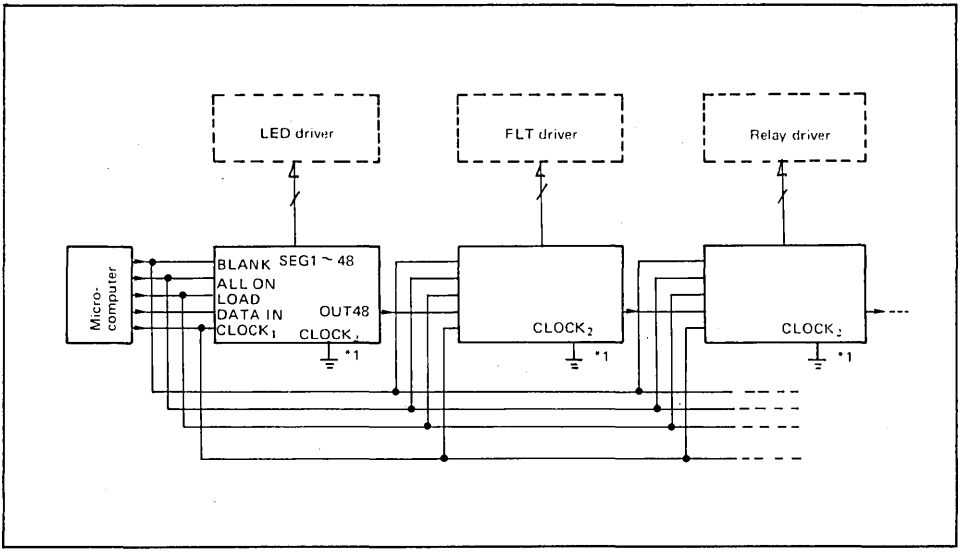


*1: The COM pin of the slave MSM5219BGS can be WIRED OR.

*2: When this IC is used under a strong external noise or large-capacity LCD load, this resistor prevents latch-up to be caused by a low output impedance of the COM pin.
The resistance is about 100Ω.

● **Output Expander**

As explained above, this IC can drive the static LCD with the COM pin. In addition, it can also be used as an output pin expander for a microcomputer with the following connections:



*1: In this example, "H" is output by the positive logic, that is, when "H" is written from DATA IN, "H" is output with a LOAD signal. If the OSC pin is connected to V_{DD}, the output has the negative logic, that is, the logic level input from the DATA IN pin is inverted and output.

MSM5221GS

56-DOT STATIC LCD DRIVER

GENERAL DESCRIPTION

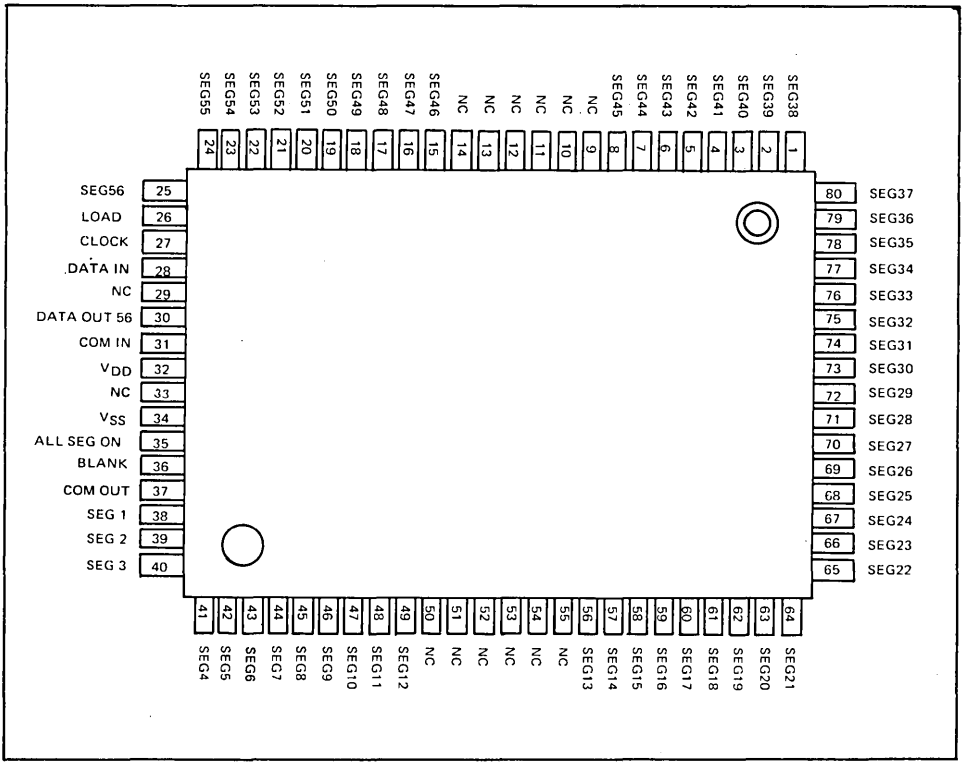
The OKI MSM5221GS is a 56 dot static LCD driver which is fabricated by low power CMOS metal gate technology. This LSI consists of 56-bit shift register, 56-bit latch and 56-bit LCD driver. The display data, which was input to the 56-bit shift register by the DATA IN signal and CLOCK signal, is transferred to the 56-bit latch by the LOAD signal and the data is output to the LCD through the 56-bit LCD driver.

FEATURES

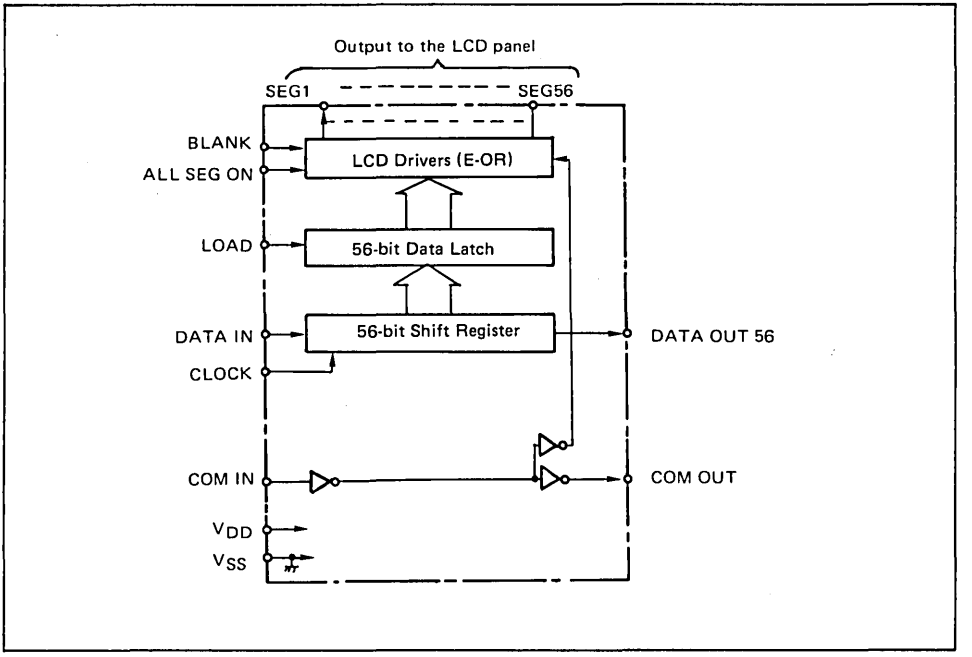
- 56 dots static LCD driving capability
- Simple interface with microcomputer chip (controlled by three input signals)
- Bit-to-bit correspondence between the input and output
- Cascade connection capability
- Fully controlled by the software
- LCD driving AC frequency is directly input externally
- Applicable as an output expander
- Supply voltage: 3 ~ 7V
- 80 pin plastic package (bent lead)

PIN CONFIGURATION

(Top View) 80 Lead Plastic Flat Package



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Limits	Unit
Supply voltage	$V_{DD} - V_{SS}$	T_a = 25°C	−0.3 ~ +7	V
Input voltage	V_I	T_a = 25°C	V_{SS} − 0.3 ~ V_{DD} + 0.3	V
Storage temperature	T_{stg}	—	−55 ~ +150	°C

OPERATING RANGE

Item	Symbol	Condition	Limits	Unit
Supply voltage	$V_{DD} - V_{SS}$	—	3 ~ 7	V
Operating temperature	T_{OP}	—	−40 ~ +85	°C

DC CHARACTERISTICS

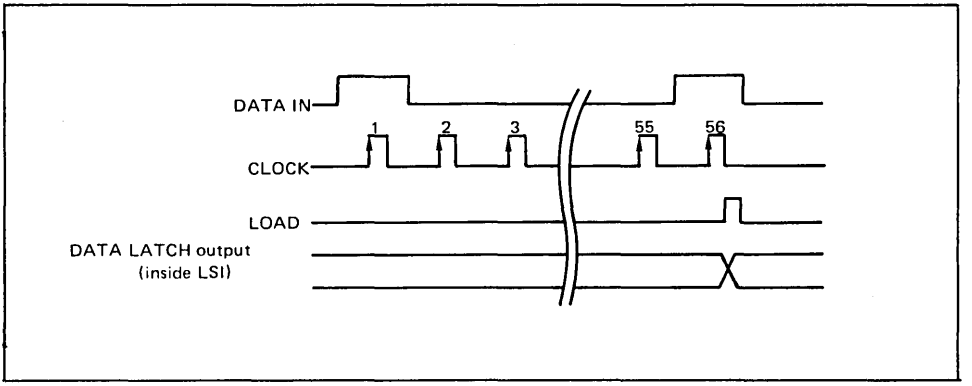
($V_{DD} - V_{SS}$ = 5V, T_a = −40 ~ +85°C)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
"H" Input voltage	V_{IH}	—	3.6	–	–	V
"L" Input voltage	V_{IL}	—	–	–	1.0	V
Input leakage current	I_{IH}/I_{IL}	V_I = 5V/V_I = OV	–	–	1/−1	μA
"H" SEG Output voltage	V_{OHS}	I_O = −30μA	4.8	–	–	V
"L" SEG Output voltage	V_{OLS}	I_O = 30μA	–	–	0.2	V
"H" COM Output voltage	V_{OHC}	I_O = −150μA	4.8	–	–	V
"L" COM output voltage	V_{OLC}	I_O = 150μA	–	–	0.2	V
SEG Output current 1	I_{OHS1}/I_{OLS1}	V_{OH} = 4.5V/V_{OL} = 0.5V	−100/100	–	–	μA
SEG Output current 2	I_{OHS2}/I_{OLS2}	V_{OH} = 1V/V_{OL} = 4V	−400/400	–	–	μA
COM Output current 1	I_{OHC1}/I_{OLC1}	V_{OH} = 4.5V/V_{OL} = 0.5V	−500/500	–	–	μA
COM Output current 2	I_{OHC2}/I_{OLC2}	V_{OH} = 1V/V_{OL} = 4V	−2/2	–	–	mA
"H" Output voltage*1	V_{OH}	I_O = −0.1mA	4.5	–	–	V
"L" Output voltage*1	V_{OL}	I_O = 0.1mA	–	–	0.5	V
Clock pulse width*2	$t_{W\phi}$	—	0.5	–	–	μS
Maximum clock pulse frequency*2	$f_{\phi MAX}$	—	1	–	–	MHz
Input signal rising/falling time	$t_{r\phi}$, $t_{f\phi}$	—	–	–	5	μS
Static current consumption	I_{DD}	V_{IN} = V_{DD}, V_{SS}	–	–	100	μA

*1: Applied to DATA OUT 56.
*2: Applied to the clock for shift register.

FUNCTIONAL DESCRIPTION

- **Operation Description**
  The display data is input to the shift register by the DATA IN signal and CLOCK signal. It is transferred to the 56-bit latch by the LOAD signal and it is output to the LCD panel through 56-bit LCD driver.



- **COM IN**
  Input pin to generate the COM OUT signal. The same phase signal as the COM IN pin is output from the COM OUT pin.

- **DATA IN, CLOCK**
  DATA IN is a data input in which enables the LCD to display when DATA IN signal is at high level. The 56-bit shift register is shifted at the rising edge of the CLOCK signal. Initially, the first bit of the shift register contains the current logic level of the DATA IN pin, and the bit N (N = 2 ~ 56) contains the data which was in bit N – 1 (N = 2 ~ 56) before the start of the operation. The data which was in bit 56 before the operation start is considered invalid.

- **LOAD**
  The data in the 56-bit shift register is shifted to the 56-bit latch when the LOAD pin is set at the high level, while the last data which was transferred to the latch when the LOAD pin was set at high level is constantly output when the LOAD is set at low level.

- **ALL SEG ON**
  When this pin is set at high level, all segments display turn on. This pin has the priority to the BLANK pin described as below.

- **BLANK**
  When this pin is set at high level, all segments display turn off. The ALL SEG ON pin has the priority over this pin.

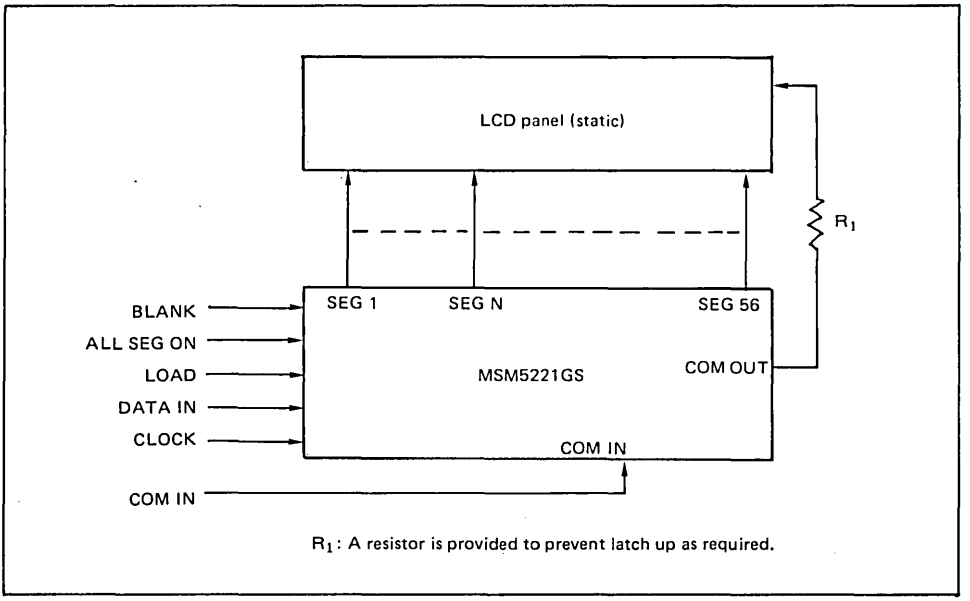
- **SEG1 ~ SEG56**
  LCD driving output pins. The reversed phase of the COM signal, which is used to display the data, is output from these pins when SEG1 ~ SEG56 are set at high level, while there is no display on the LCD when these pins are set at low level.
  The display data which was input from the DATA IN pin is output from these pins to the LCD panel. The SEG N pin corresponds to the bit N of the shift register.

- **COM OUT**
  Output terminal for the LCD. It is connected to the common side of the LCD panel.

- **DATA OUT 56**
  Output pin of the shift register. It is used when the MSM5221GS is connected in a series (cascade connection). MSM5221GS's DATA OUT 56 is connected to the next MSM5221GS's DATA IN terminal.

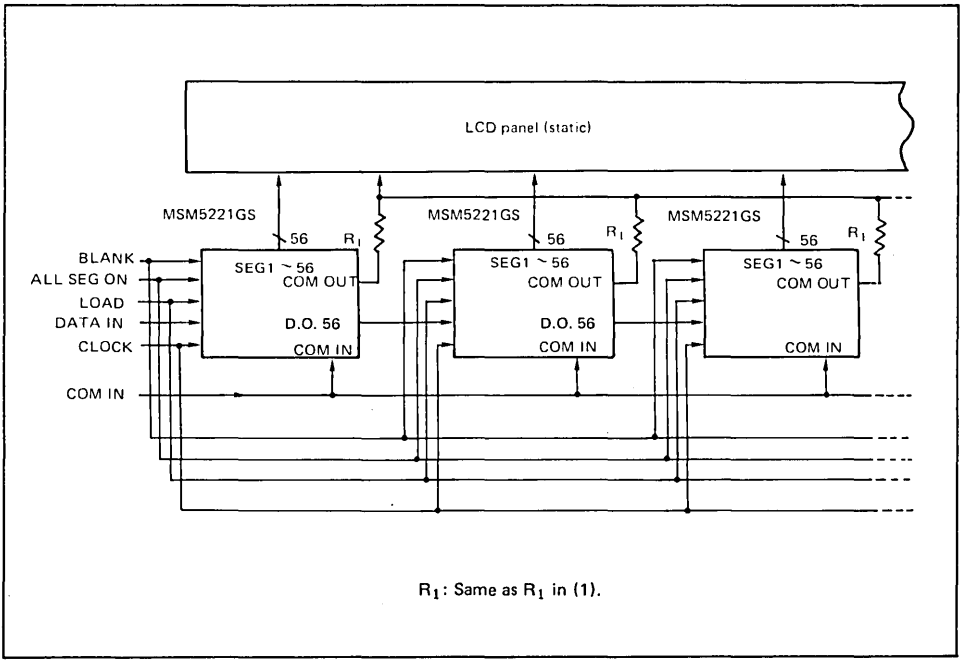
APPLICATION CIRCUIT

- **Single MSM5221GS to the LCD panel**



R_1 : A resistor is provided to prevent latch up as required.

- **Cascade connection**



R_1 : Same as R_1 in (1).

MSM5265GS

160-DOT LCD DRIVER

GENERAL DESCRIPTION

The OKI MSM5265GS is an LCD driver which can directly drive up to 80 segments in the static display mode, while it can directly drive up to 160 segments in the 1/2 duty dynamic display mode.

The MSM5265GS is fabricated by low power CMOS metal gate technology, consisting of 160-stage shift register, 160-bit latch, 80 sets of LCD driver and a common signal generator.

The display data is serially input from the DATA-IN terminal to the 160-stage shift register synchronized with the CLOCK pulse. The data is shifted to the 160-bit latch by the LOAD signal. Then the latched data is directly output to the LCD from the 80 sets of LCD driver as serial output.

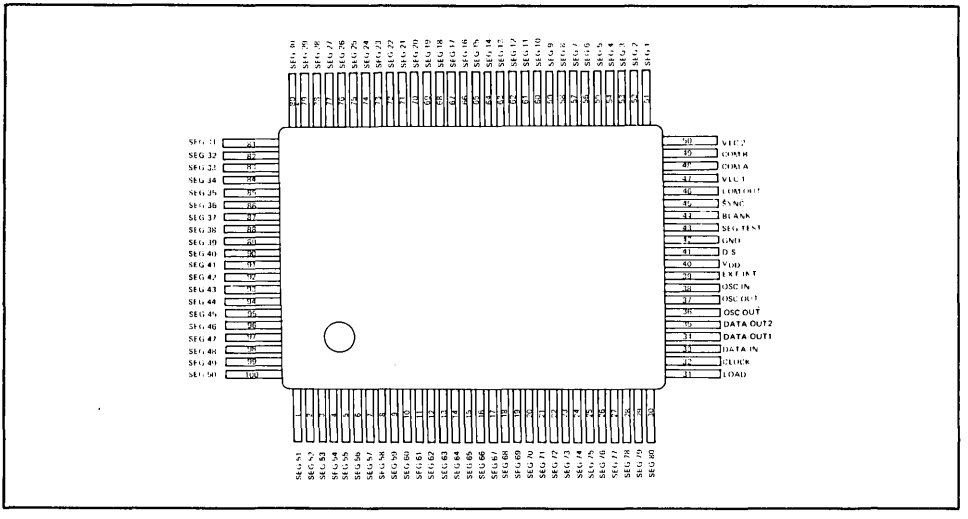
The common signal can be generated by the on-chip generator, or can be externally input. The common synchronization circuit which is used in the dynamic display mode is integrated on the chip.

FEATURES

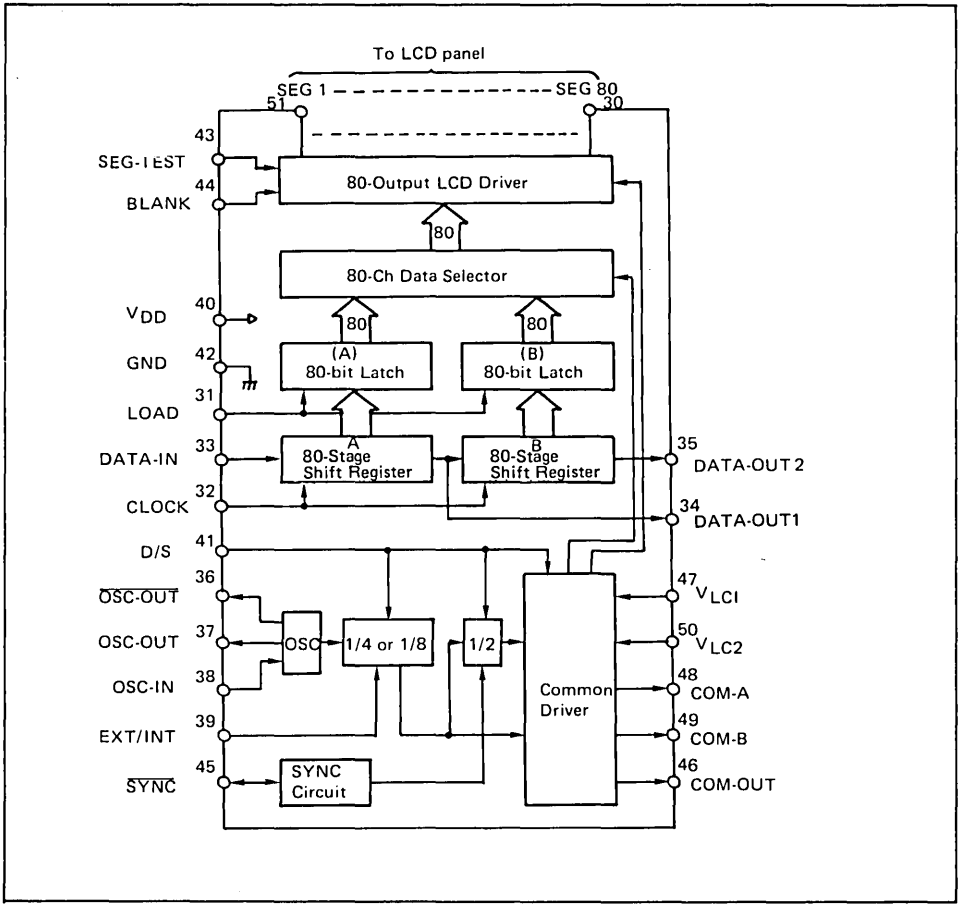
- 80 segments display drive (in the static display mode)
- 160 segments display drive (in the dynamic display mode)
- Simple interface with microcomputer
- Bit-to-bit correspondence between input data and output data
  H : Display L : No display
- Cascade connection capability
- On-chip common signal generator
- Can be synchronized with the external common signal
- Testing terminals for all-on (SEG-TEST) and all-off (BLANK)
- Applicable as an output expander
- LCD driving voltage can be adjusted by the combination of V_{LC1} and V_{LC2}
- Supply voltage: 3.0 ~ 6.0V
- 100 pin plastic flat package (bent lead)

PIN CONFIGURATION

(Top View)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Limits	Unit
Supply voltage	V_{DD}	T_a = 25°C	− 0.3 ~ + 6.5	V
Input voltage	V_I	T_a = 25°C	GND − 0.3 ~ V_{DD} + 0.3	V
Storage temperature	T_{stg}	—	− 55 ~ + 150	°C

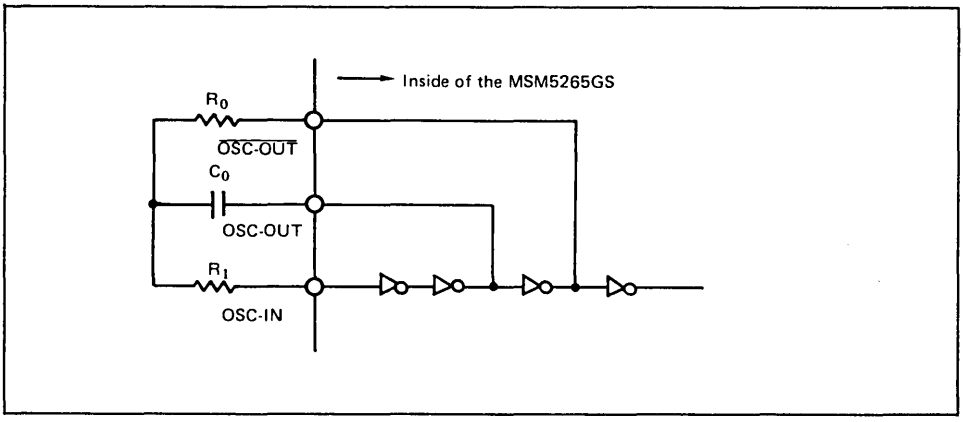
OPERATING RANGE

Item	Symbol	Condition	Limits	Unit
Supply voltage	V_{DD}	—	3 ~ 6	V
Operating temperature	T_{OP}	—	−40 ~ 85	°C
LCD driving voltage	$V_{DD} - V_{LC2}$	—	3 ~ V_{DD}	V

3

RECOMMENDING OSCILLATION CIRCUIT CONDITION

Item	Symbol	Corresponding pin	Condition	MIN	TYP	MAX	Unit
Oscillator resistance	R_0	36 $\overline{\text{OSC-OUT}}$	—	56	100	220	kΩ
Oscillator capacitance	C_0	37 OSC-OUT	Film capacitor	0.001	–	0.047	μF
Current limiter resistance	R_1	38 OSC-IN	$R_1 \geqq 10\ R_0$	0.56	1	2.2	MΩ
Common signal frequency	f_{COM}	48 COM-A 49 COM-B	—	25	–	150	Hz



D.C. CHARACTERISTICS

(V_{DD} = 5.0V T_a = −40 ~ +85°C)

Item	Symbol	Corresponding pin	Condition	MIN	TYP	MAX	Unit
"H" Input voltage	V_{IH}	43 SEG-TEST 44 BLANK 31 LOAD 33 DATA-IN 32 CLOCK 41 D/S 39 EXT/INT 38 OSC-IN	—	3.6	–	–	V
"L" Input voltage	V_{IL}		—	–	–	1.0	V
Input leakage current	I_{IL}		V_I = 5.0V/0V	–	–	±1	μA
"H" Output voltage	V_{OH}	34 DATA-OUT1 35 DATA-OUT2 46 COM-OUT	I_O = −100μA	4.5	–	–	V
		37 OSC-OUT 36 $\overline{\text{OSC-OUT}}$	I_O = −200μA	4.5	–	–	V
		50 ~ 100 1 ~ 30 output of all segments	V_{LC1} = 2.5V V_{LC2} = 0V I_O = −30μA	4.8	–	–	V
		48 COM-A 49 COM-B	V_{LC1} = 2.5V V_{LC2} = 0V I_O = 150μA	4.8	–	–	V
"M" Output voltage	V_{OM}	48 COM-A 49 COM-B	V_{LC1} = 2.5V V_{LC2} = 0V I_O = ±150μA	2.3	–	2.7	V
"L" Output voltage	V_{OL}	34 DATA-OUT1 35 DATA-OUT2 46 COM-OUT	I_O = 100μA	–	–	0.5	V
		37 OSC-OUT 36 $\overline{\text{OSC-OUT}}$	I_O = 200μA	–	–	0.5	V
		51 ~ 100 1 ~ 30 Output of all segments	V_{LC1} = 2.5V V_{LC2} = 0V I_O = 30μA	–	–	0.2	V
		48 COM-A 49 COM-B	V_{LC1} = 2.5V V_{LC2} = 0V I_O = 150μA	–	–	0.2	V
		45 $\overline{\text{SYNC}}$	I_O = 250μA	–	–	0.8	V
Output leakage current	I_{LO}	45 $\overline{\text{SYNC}}$	V_O = 5V when internal Tr is off	–	–	5	μA
Segment output impedance	R_{SEG}	51 ~ 100 1 ~ 30 Output of all segments	V_{LC1} = (5 + V_{LC2})/2 V_{LC2} = 0 ~ 2V	–	–	10	kΩ

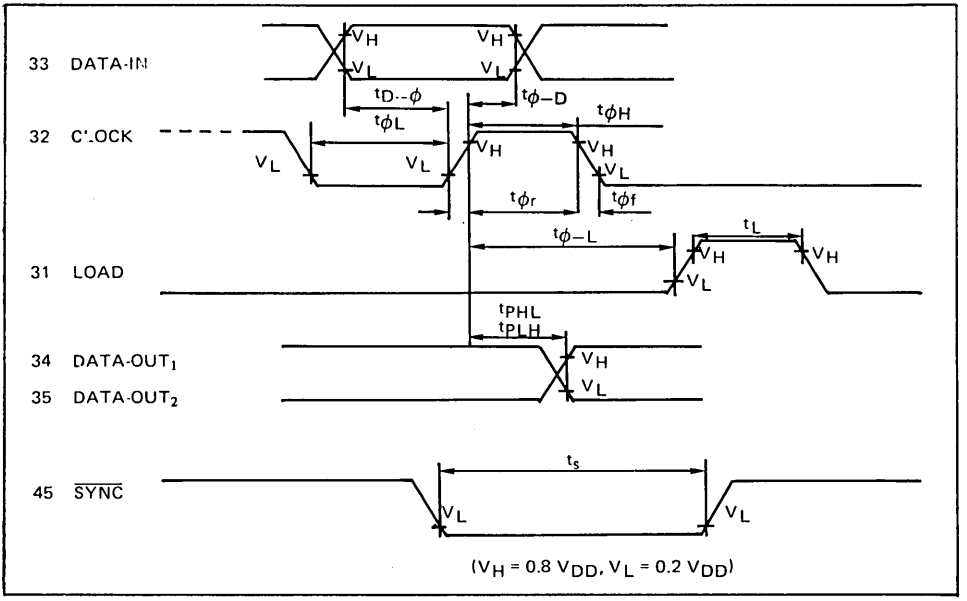
Item	Symbol	Corresponding pin	Condition	MIN	TYP	MAX	Unit
Common output impedance	R_{COM}	48 COM-A 49 COM-B	$V_{LC1} = (5 + V_{LC2})/2$ $V_{LC2} = 0 \sim 2V$	–	–	1.5	kΩ
Static mode consumption current	I_{DD1}	40 V_{DD}	Set all input level either "H" or "L"			100	μA
Dynamic mode consumption current	I_{DD2}		No load oscillation. $R_0 = 100$ kΩ, $C_0 = 0.01$ μF, $R_1 = 1$MΩ		0.12	0.5	mA

3

SWITCHING CHARACTERISTICS

($V_{DD} = 3.0 \sim 6.0V$ $T_a = -40 \sim +85°C$)

Item	Symbol	Corresponding pin	Condition	MIN	MAX	Unit
Maximum clock frequency	$f_{\phi MAX}$	32 CLOCK	—	1	–	MHz
Clock "H" time	$t_{\phi H}$		—	0.3	–	μs
Clock "L" time	$t_{\phi L}$		—	0.5	—	μs
Clock pulse rising/ falling time	$t_{\phi r}$ $t_{\phi f}$		—	–	0.1	μs
Data setup time	$t_{D-\phi}$	33 DATA-IN	—	0.1	–	μs
Data hold time	$t_{\phi-D}$	32 CLOCK	—	0.1	–	μs
"H", "L" propagation delay time	t_{PHL} t_{PLH}	34 DATA-OUT$_1$ 35 DATA-OUT$_2$ 32 CLOCK	When 15PF output capacitors are loaded 34 and 35.	–	0.8	μs
LOAD "H" time width	t_L	31 LOAD	—	0.2	–	μs
CLOCK → LOAD time	$t_{\phi-L}$	32 CLOCK 31 LOAD	—	0.1	–	μs
OSC-IN Maximum input frequency	f_{OSCMAX}	38 OSC-IN	—	5	–	kHz
$\overline{SYNC}$ "L" time width	t_s	45 $\overline{SYNC}$	—	0.2	–	μs

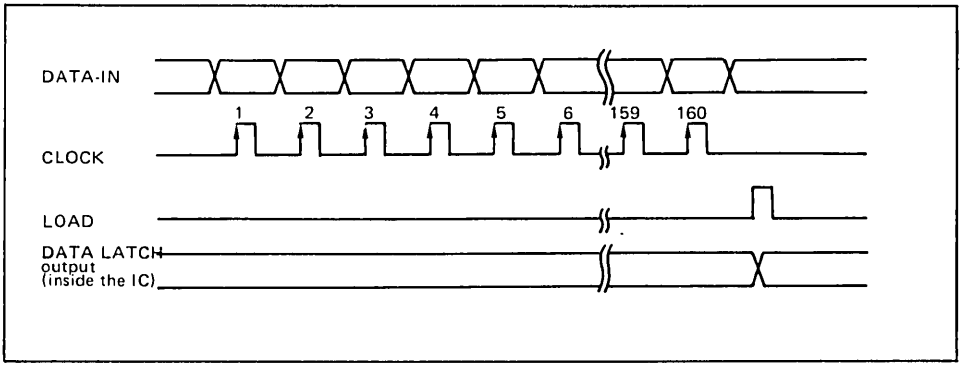


($V_H = 0.8\ V_{DD}$, $V_L = 0.2\ V_{DD}$)

FUNCTIONAL DESCRIPTION

- **Operational description**

The MSM5265GS consists of 160-stage shift register, 160-bit latch, and 80 sets of LCD driver. The display data is input from the DATA-IN terminal to the 160-stage shift register at the rising edge of the CLOCK pulse and it is shifted to the 160-bit latch when the LOAD signal is set at "H" level, then it is directly output to the LCD panel from the 80 sets of LCD driver.



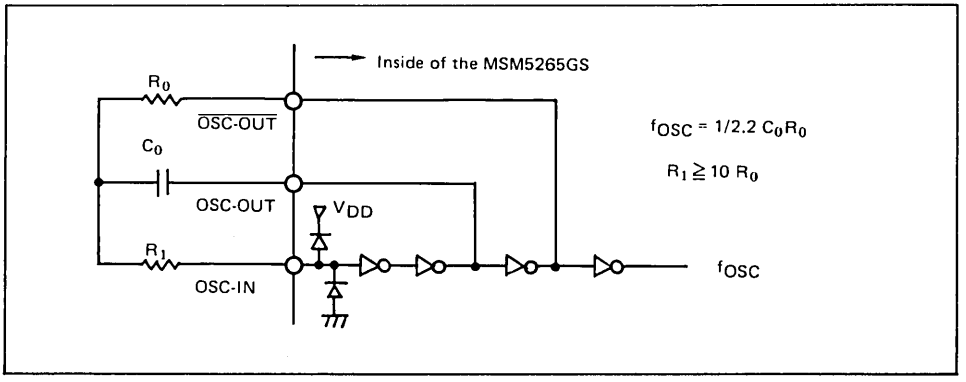
- **OSC-IN, OSC-OUT, $\overline{\text{OSC-OUT}}$**

By connecting the external registors R_0, R_1 and external capacitor C_1 with OSC-IN, OSC-OUT and $\overline{\text{OSC-OUT}}$ respectively as shown in the figure below, an oscillating circuit to generate the common signal is formed.

This frequency is divided into either 1/8 or 1/4 by the internal dividing circuit. The 1/8 divided frequency is used in the static display mode, while the 1/4 divided frequency is used as the common signal in the dynamic display mode which is output from the COM-OUT terminal. (EXT/INT should be set at low level.)

The resistor R_1 is to limit the current on the OSC-IN terminal's protecting diodes. The value of the R_1 should be 10 times more than that of R_0.

When the external common signal is used, the EXT/INT terminal should be set at high level and the external common signal should be input from the OSC-IN terminal.



- **D/S**
  When this pin is set at high level, the MSM5265GS operates in the dynamic display mode, while it operates in the static display mode when this pin is set at low level.

- **EXT/INT**
  When the external common signal is used, this pin should be set at high level and the external common signal is to be input from the OSC-IN terminal. The input common signal is used same as the internal common signal and is output from the COM-OUT pin through the buffer.
  When the on-chip common signal generator is used, this pin should be set at low level.
  When the MSM5265GS is used as an output expander, this pin should be set at high level and the OSC-IN pin should be set at low level.

- **COM-OUT**
  When more than two MSM5265GSs are connected in a series (cascade connection), this pin should be connected with all of the slave MSM5265GS's OSC-IN terminal.

- **$\overline{\text{SYNC}}$**
  This pin is an input/output pin which is used when more than two MSM5265GSs are used in a series (cascade connection) in the dynamic display mode. All of the involved MSM5265GS's $\overline{\text{SYNC}}$ pins should be connected in a same line so that they should be pulled up by the common resistor, which makes phase level of all involved MSM5265GS's COM-A terminals and COM-B terminals equal. When single MSM5265GS is used in the dynamic display mode, $\overline{\text{SYNC}}$ should be pulled up by the resistor.
  In the static display mode including single MSM5265GS's operation, cascade connection and output expander operation, this pin should be set at ground level.

- **DATA-IN, CLOCK**
  The display data is serially input from the DATA-IN terminal to the 160-stage shift register at the rising edge of the CLOCK pulse. The high level of the display data is used to turn the display on, while low level of the display data is used to turn off the display.

- **DATA-OUT$_1$**
  The 80th stage of the shift register contents is output from this pin.
  When more than two MSM5265GSs are connected in a series (cascade connection) in the static display mode, this pin should be connected to the next MSM5265GS's DATA-IN terminal.

- **DATA-OUT$_2$**
  The 160th stage of the shift register contents is output from this pin.
  When more than two MSM5265GSs are connected in a series (cascade connection) in the dynamic display mode, this pin should be connected to the next MSM5265GS's DATA-IN terminal.

- **LOAD**
  The signal for latching the shift register contents is input from this pin.
  When LOAD pin is set at high level, the shift register contents is shifted to the 80 sets of the LCD driver. When this pin is set at low level, the last display data, which was transferred to the 80 sets of LCD driver when LOAD pin was set at high level, is held.

- **V_{LC2}**
  Supply voltage pin for the 80 sets of LCD driver. The input level to this pin should be the low level output voltage of segment output (SEG1 ~SEG80) and common output (COM-A, COM-B).
  In this case, the high level of segment output and common output is V_{DD} level, while low level of segment output and common output is V_{LC2} level. V_{LC2} should be set at more than ground level.

- **V_{LC1}**
  Supply voltage pin for the middle level voltage of the common output. The input level of this pin is the middle level output voltage of the common output (COM-A, COM-B) in the dynamic display mode.
  The value of the V_{LC1} is calculated by the following formula.

$$V_{LC1} = (V_{DD} + V_{LC2})/2$$

  In the static display mode, this pin should be set at open level.

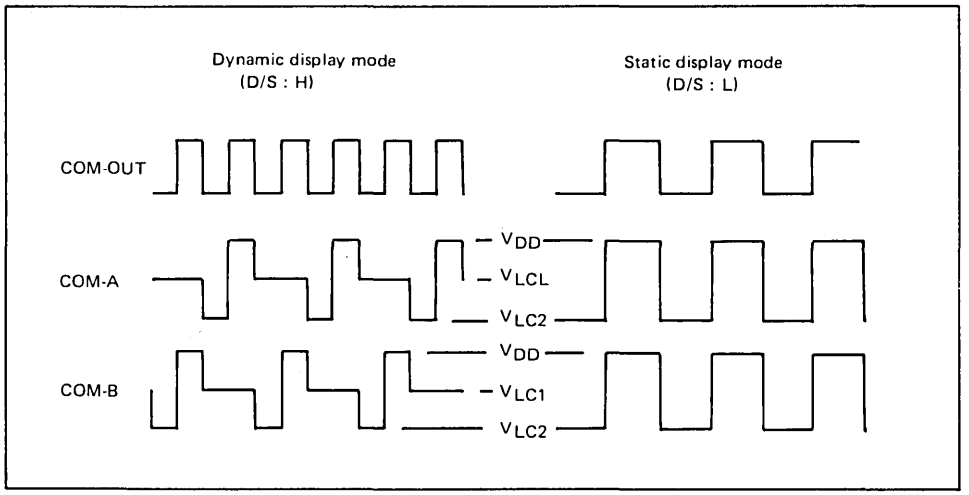
- **COM-A, COM-B**

  LCD driving common signal is output from these pins and these pins should be connected to the common side of the LCD panel.

  – In the static display mode
  Same phase pulse as COM-OUT terminal is output from both of COM-A and COM-B. In this case high level is V_{DD} level and low level is V_{LC2} level.

  – In the dynamic display mode
  The COM-A and COM-B output signal are alternately changed within each COM-OUT output cycle, resulting in alternately repetition of select and non-select modes.

  In the select mode the, same phase level as the COM-OUT signal is output.
  In this case, V_{DD} or V_{LC2} is output at high level or low level respectively. In the non-select mode, V_{LC1} is output at the middle level.
  In the select mode of COM-A (non-select mode of COM-B), the 1st ~80th latched data contents are output from the 80 sets of LCD driver to the LCD panel.
  In the select mode of COM-B (non-select mode of COM-A), the 81st ~ 160th latched data contents are output from the 80 sets of LCD driver to the LCD panel.



● **SEG1 ~ SEG80**

LCD segment driving signal is output from these pins and these pins should be connected to the segment side of the LCD panel.

"H" level : V_{DD} level, "L" level : V_{LC2} level

– In the static display mode

Since the Nth bit of the latched data contents corresponds to the SEG N, the data after 81st bit is invalid for the display in the static display mode.

The inversed phase signal as the COM-OUT signal is output to the LCD, when the display turns on, while the same phase signal is output when the display turns off.

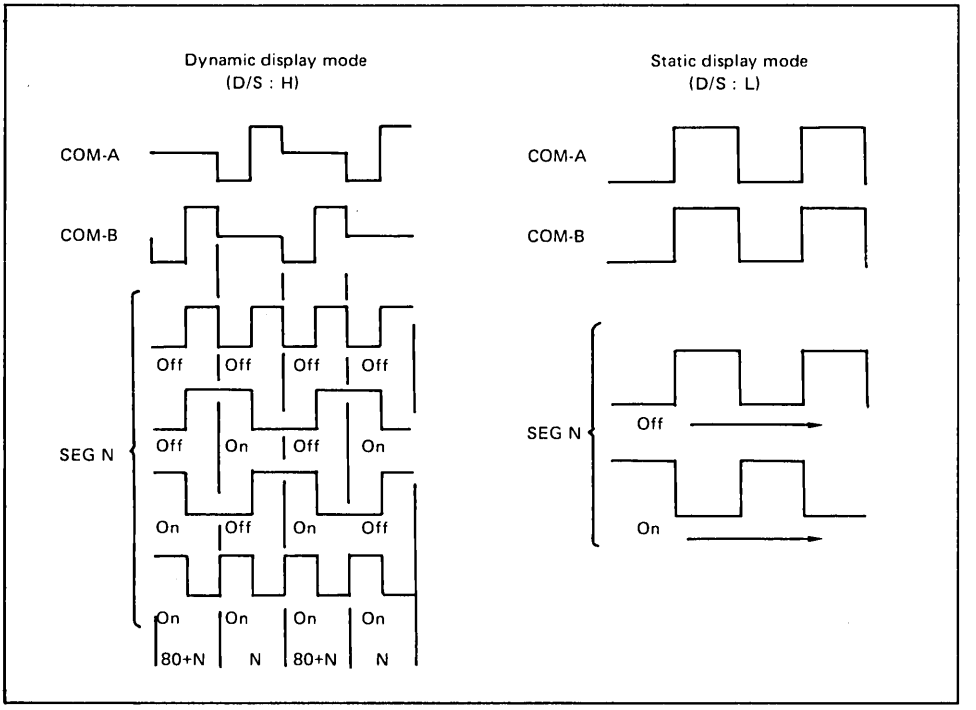
– In the dynamic display mode

Output of the SEG N corresponds as follows.

When COM-A is select mode:
Nth bit of the latched data contents

When COM-B is select mode:
(80 + N)th bit of the latched data contents

When the display turns on, the inversed phase signal as the common signal is output, while the same phase signal as the common signal is output when the display turns off.



● **SEG-TEST**

This pin is used to test the segment output (SEG1 ~ SEG80). All display turn on when this pin is set at high level, while the display becomes the same condition before this pin was set at high level, when this pin is set at low level. This pin has the priority over BLANK terminal.

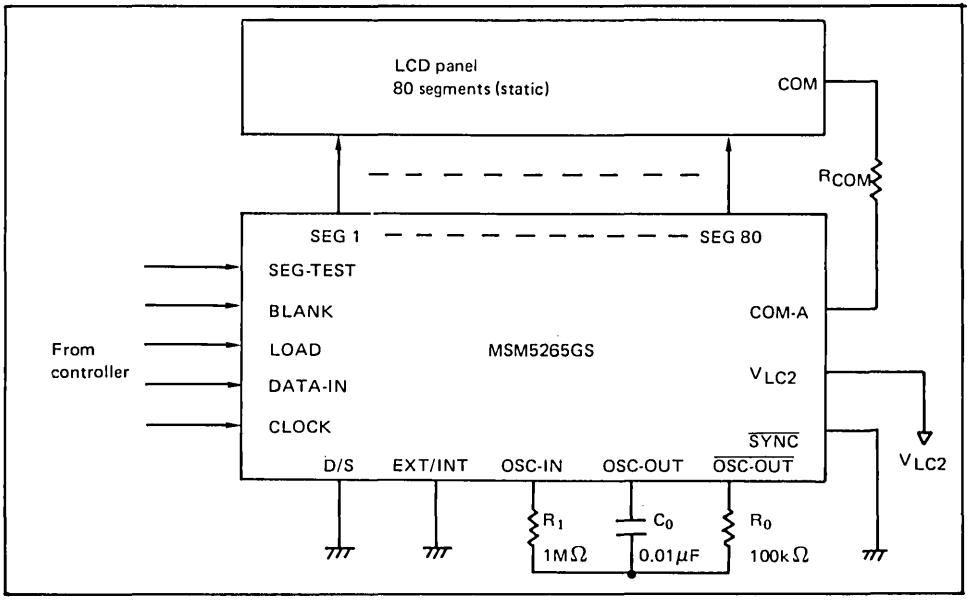
● **BLANK**

This pin is also used to test the segment output (SEG1 ~ SEG80). All display turn off when this pin is set at high level, while the display becomes the same condition before this pin was set at high level, when this pin is set at low level.

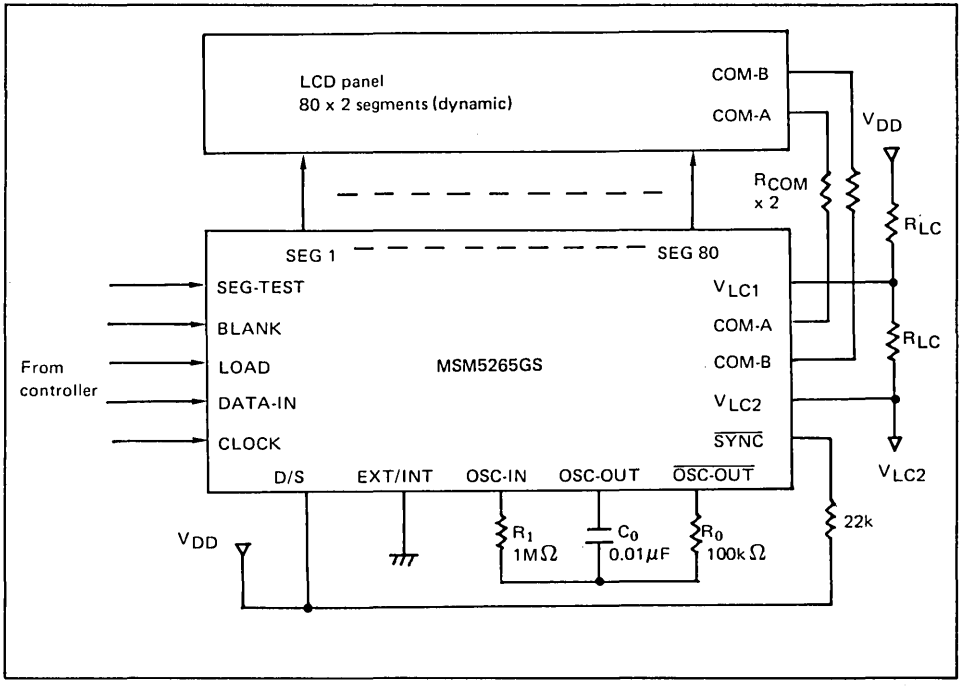
When SEG-TEST pin is set at high level, the input on this pin is invalid.

APPLICATION CIRCUIT

1) Single MSM5265GS operation in the static display mode.

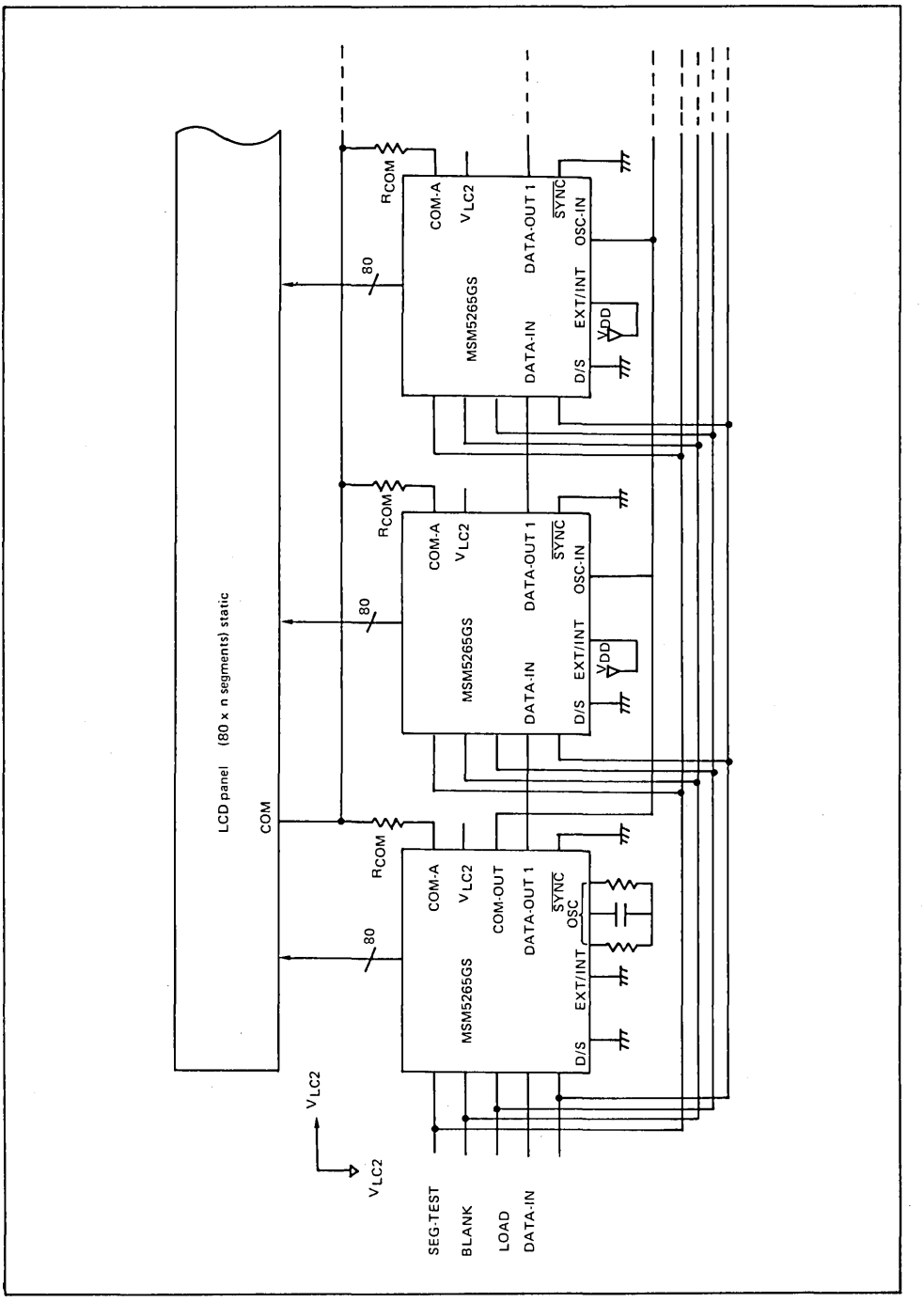


2) Single MSM5265GS operation in the dynamic display mode.

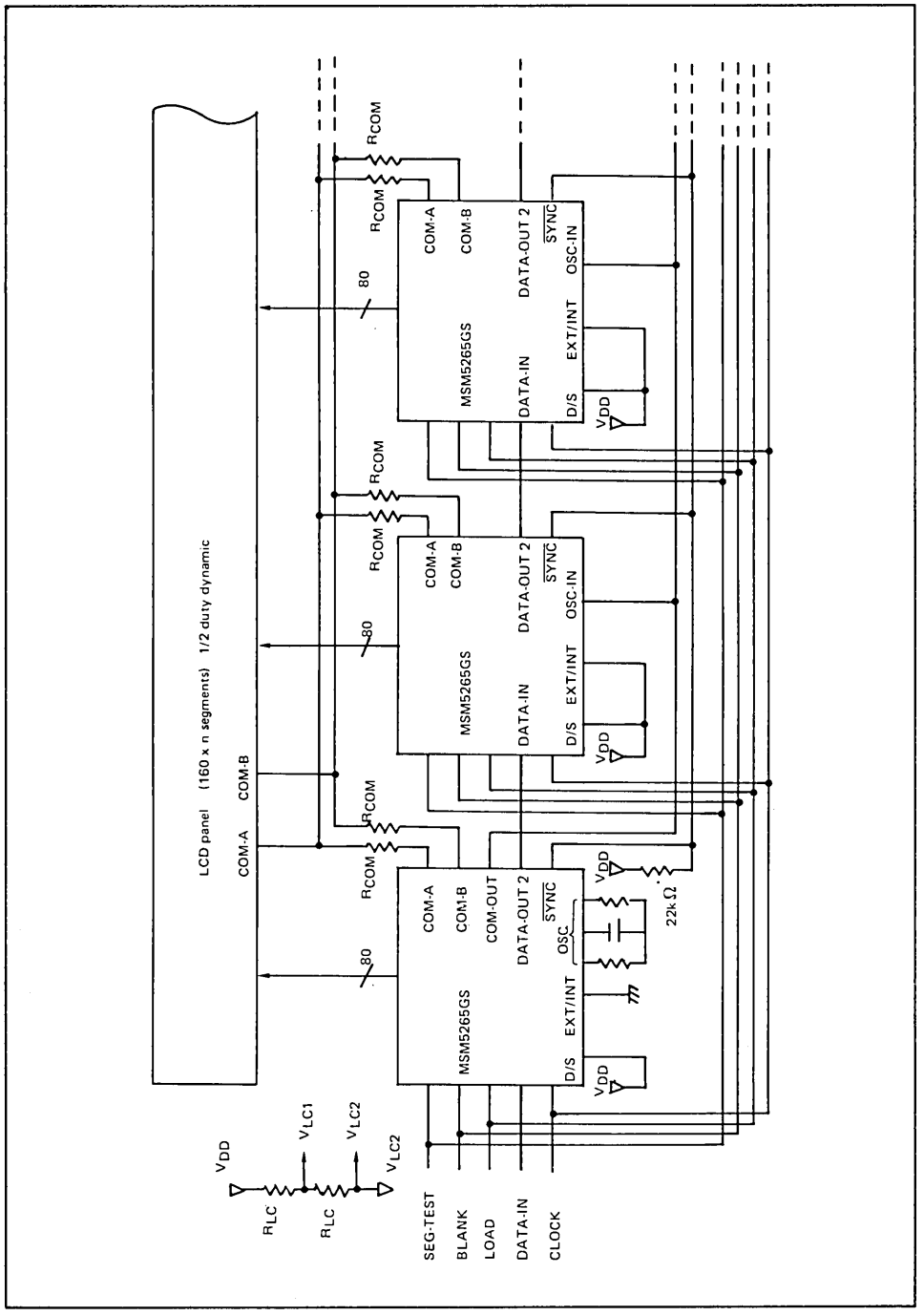


3

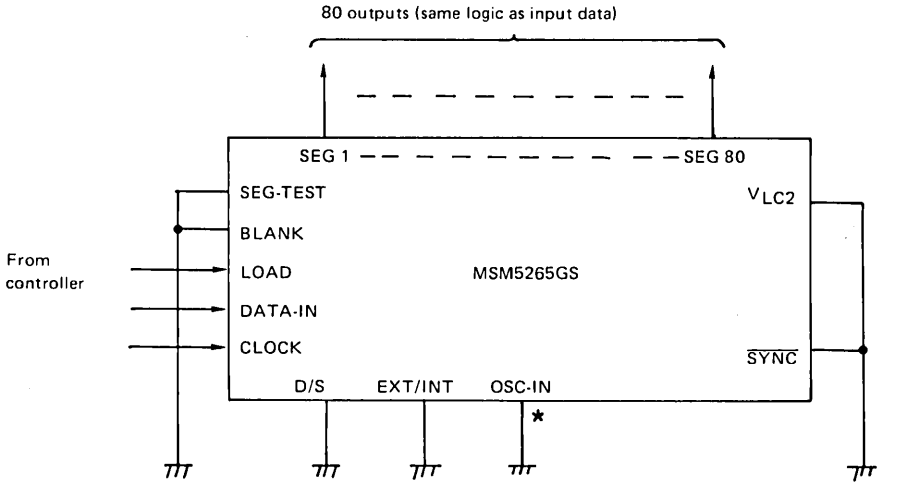
3) Cascade connection of MSM5265GSs in the static display mode.



4) Cascade connection of MSM5265GSs in the dynamic display mode.



5) Output-expander



*The output logic can be reversed in respect to the input data by setting OSC-IN to "H" level.

3

DOT MATRIX LCD DRIVER

MSM5238GS

DOT MATRIX LCD 32 DOT COMMON DRIVER

GENERAL DESCRIPTION

The OKI MSM5238GS is a dot matrix LCD's common driver LSI which is fabricated by low power CMOS metal gate technology. The scanning signal in one matrix display frame can be divided into up to 1/32 duty. This LSI consists of 32-bit shift register, 32-bit level shifter and 32-bit 4-level driver.

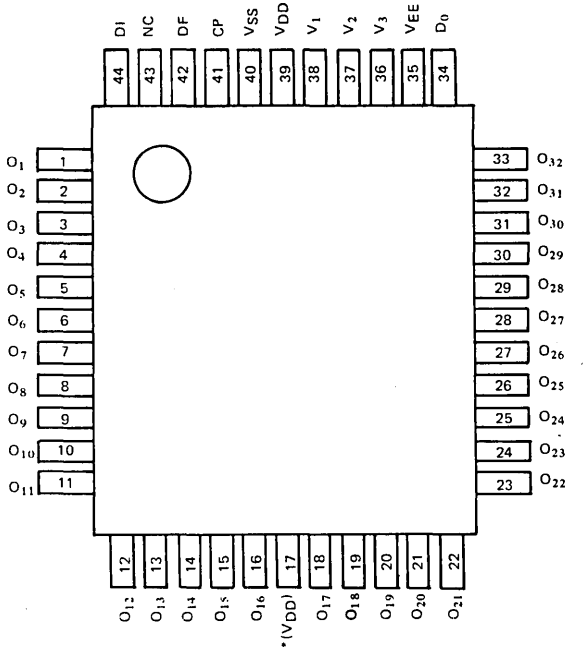
This LSI can drive a variety of LCD panel because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from external source.

FEATURES

- Supply voltage: 3 ~ 7V
- LCD driving voltage: 3 ~ 16V
- Applicable LCD duty: 1/32 ~ 1/64
  (Two chips of MSM5238GS are required to drive 1/64 duty LCD panel).
- Bias voltage can be supplied externally
- 44 pin PLASTIC FLAT Package

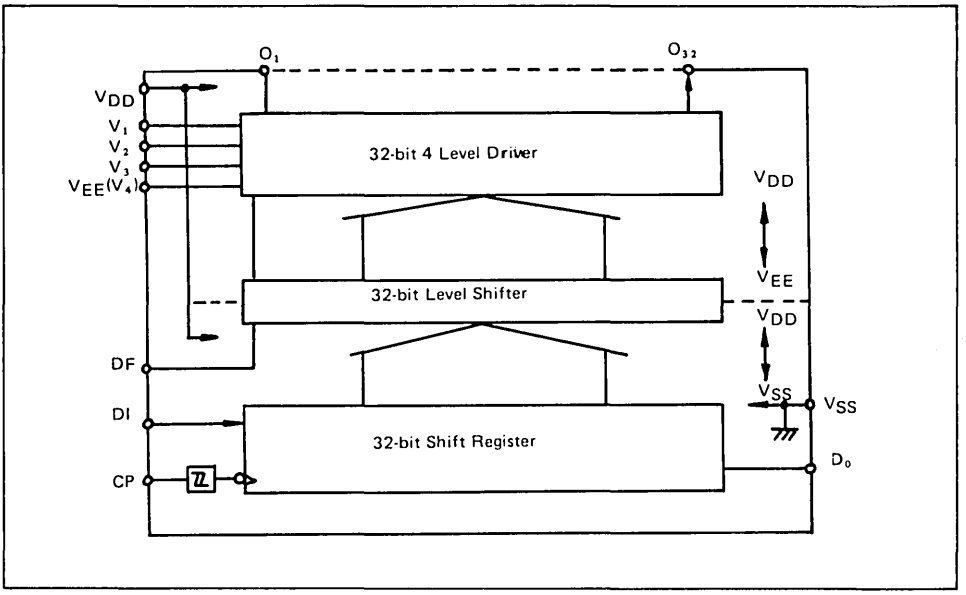
PIN CONFIGURATION

(Top View)



*Pin 17 is an auxiliary pin. It shall be connected to the power supply or disconnected to any other terminal.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Limits	Unit
Supply voltage	V_{DD}	Ta = 25°C	−0.3 ~ 7	V
Supply voltage	$V_{DD} - V_{EE}$		0 ~ 16	V
Input voltage	V_I		−0.3 ~ V_{DD}	V
Storage temperature	Tstg	–	−55 ~ + 150	°C

OPERATING RANGE

Item	Symbol	Condition	Value	Unit
Supply voltage	V_{DD}	–	3 ~ 7	V
Supply voltage	$V_{DD} - V_{EE}$	–	3 ~ 16	V
Operation temperature	Topr	–	−40 ~ + 85	°C
Fan-out	N	MOS load	5	–

$V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 (V_{EE})$

D.C. CHARACTERISTICS

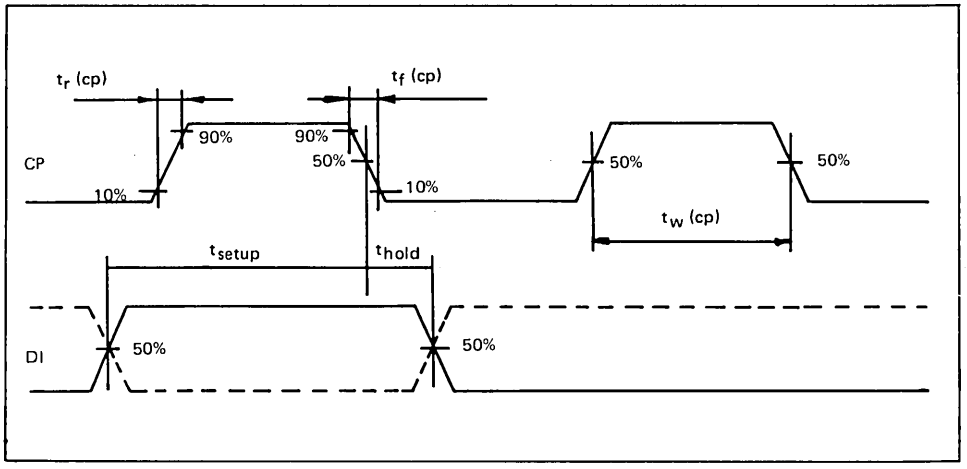
Item	Symbol	Condition				Limits			Unit
		V_{DD} (V)	V_{SS} (V)	V_{EE} (V)		MIN	TYP	MAX	
"H" input voltage	*1 V_{IH_1}/ V_{IH_2}	5	0	0 ~ −9	–	3.6/ 4.2	–	–	V
		7	0	0 ~ −7	–	5.2/ 6.0	–	–	
"L" input voltage	*1 V_{IL_1}/ V_{IL_2}	5	0	0 ~ −9	–	–	–	0.8/ 0.4	V
		7	0	0 ~ −7	–			1.1/ 0.5	
Input voltage	I_{IH}	7	0	−7	V_I = 7V	–	–	1	μA
	I_{IL}	7	0	−7	V_I = 0V	–	–	−1	
"H" output voltage	*2 V_{OH}	5	0	0 ~ −9	I_{OD} = −40μA	4.2	–	–	V
		7	0	0 ~ −7	I_{OD} = −56μA	5.8	–	–	
"L" output voltage	*2 V_{OL}	5	0	0 ~ −9	I_{OD} = 0.2mA	–	–	0.4	V
		7	0	0 ~ −7	I_{OD} = 0.3mA	–	–	0.4	
ON Resistance	R_{ON} (V_1, V_4)	5	0	0	V_0: DRV output $V_0 - V_1$ = 0.25V $V_1 = V_{EE} \sim (V_{DD} - 0.25V)$ $V_0 - V_4$ = 0.25V $V_4 (V_{EE})$: MAX 0V	–	500	2000	Ω
			0	−5		–	250	1000	
		7	0	0		–	350	1400	
			0	−7		–	200	800	
	R_{ON} (V_2, V_3)	5	0	0	$V_N = V_2$ or V_3 V = DRV output $V_0 - V_N$ = 0.25V $V_N = V_{EE} \sim (V_{DD} - 0.25V)$	–	800	3200	Ω
			0	−5		–	450	1800	
		7	0	0		–	550	2200	
			0	−7		–	350	1400	
OFF Lead current	I_{OFF}	5	0	−9	–	–	–	±5	μA
		7	0	−7	–	–	–	±5	
Power supply current	I_{DD}	5	0	−9	–	–	–	0.5	mA
		7	0	−7	–	–	–	1.0	
Input capacitance	C_I				–	–	5	–	pF

*1 V_{IH_1} and V_{IL_1} are input pins for DI and DF, while V_{IH_2} and V_{IL_2} are input pins for CP.

*2 V_{OH} and V_{OL} are output pins for D_0.

SWITCHING CHARACTERISTICS

Item	Symbol	V_{DD} (V)	Condition	MIN	TYP	MAX	Unit
Maximum clock frequency	t (cp)	5	–	400	–	–	KHz
		7	–	550	–	–	
Clock pulse width	t_W (cp)	5	–	400	–	–	ns
		7	–	300	–	–	
Data setup time (DATAIN → CP)	t_{setup}	5	–	100	–	–	ns
		7	–	50	–	–	
Data hold time (DATAIN → CP)	t_{hold}	5	–	800	–	–	ns
		7	–	500	–	–	
Clock pulse Rising/Falling time	tr (cp)	5	–	–	–	0.5	ms
	tr (cp)	7	–	–	–	0.1	



PIN DESCRIPTION

- **DI**
  The data from LCD controller LSI is input to 32-bit shift register from DI. (Positive logic)
  This LSI is applicable up to 1/32 duty LCD panel because this LSI consists of 32-bit shift register.

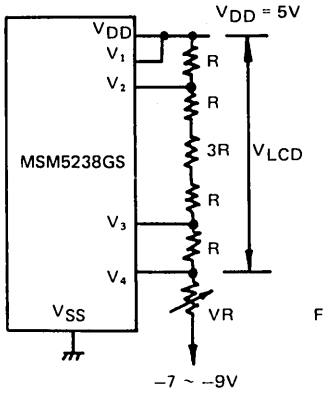
- **CP**
  Clock pulse input pin for 32-bit shift register. The data is shifted to 32-bit level shifter at the falling edge of the clock pulse. A data set up time (t_{setup}) and data hold time (t_{hold}) is required between DI and CP signal. (Refer to SWITCHING CHARACTERICS.) Schmit circuit is included in CP input circuit.

- **DF**
  Alternate signal input pin for LCD driving waveform.

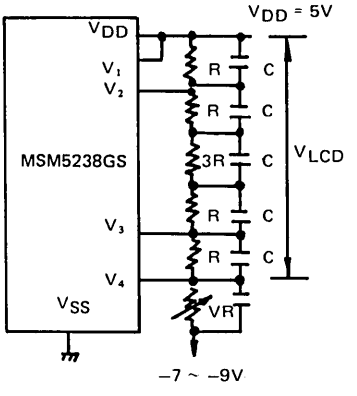
- **V_{DD}, V_{SS}**
  V_{DD} is a supply voltage pin. Usually it is used at V_{DD} = 3.0 ~ 7.0V V_{SS} is a ground pin. (V_{SS} = 0V)

- **$O_1 - O_{32}$**
  Display data output pins which correspond to each data bit in the latch. One of V_1, V_2, V_3 and V_4 is selected as a display driving voltage source according to the combination of latched data level and DF signal. Refer to the truth table and Time Chart. Output signal is a analog signal. $O_1 - O_{32}$ are connected to the common side of the LCD panel.

Latched data	DF	Display data output level
L	L	V_2
	H	V_3
H	L	V_4
	H	V_1



1/32 duty C = 0.1 μF or less
1/7 bias R = 0.5 KΩ~6



1/32 duty C = 0.1 μF or less
1/7 bias R = 0.5 kΩ~5kΩ
VR = 5kΩ~10kΩ

Fig. 1

*The value of R should be decided according to the power consumption and LCD panel size.

- **V_1, V_2, V_3, V_4**
  Bias supply voltage pin to drive the LCD. Bias voltage divided by the registance is usually used as supply voltage source.
  Fig. 1 shows the case when the bias voltage, which determines the LCD driving voltage, is supplied from the external source.

- **DO**
  Shift register contents output pin. The data which was input from DI is output from DO with 32 bits' delay, synchronized with the clock pulse. By connecting DO with next MSM5238GS's DI, this LSI is applicable to the LCD, the duty of which is 1/64. Refer to the Fig. 2 below.

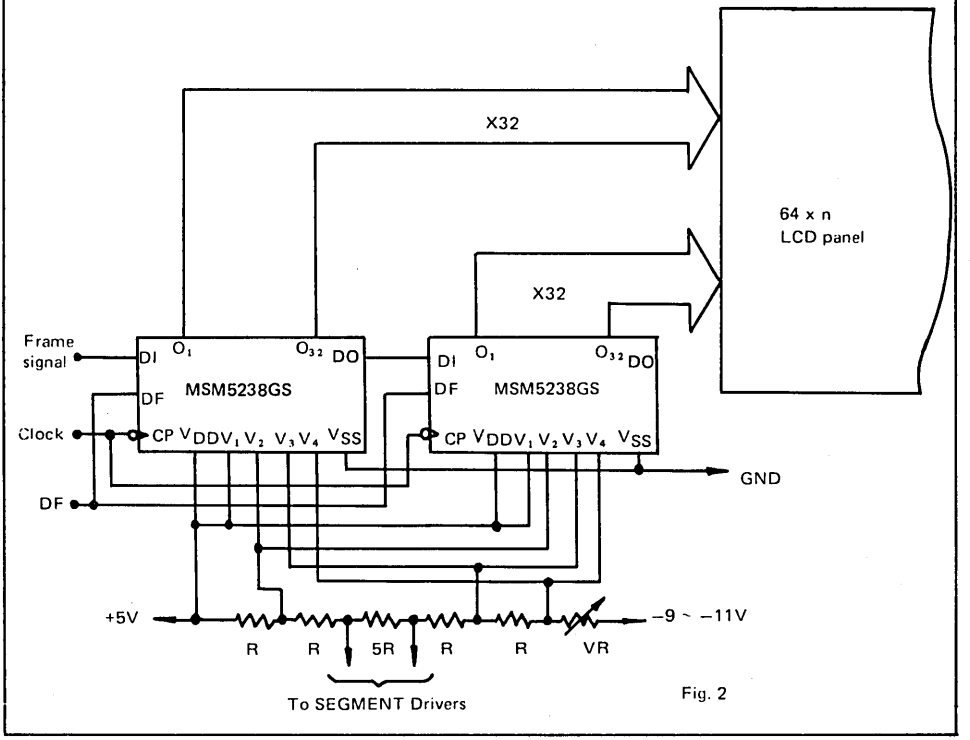
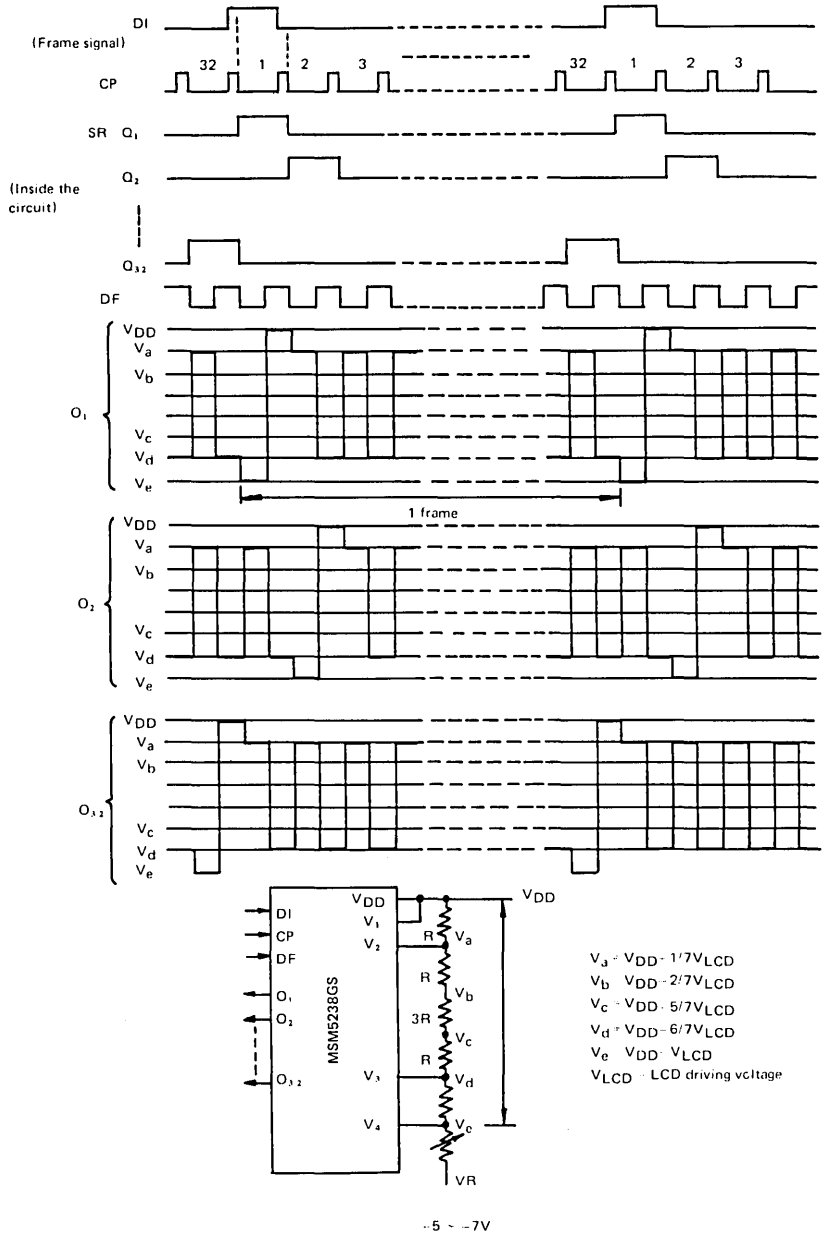


Fig. 2

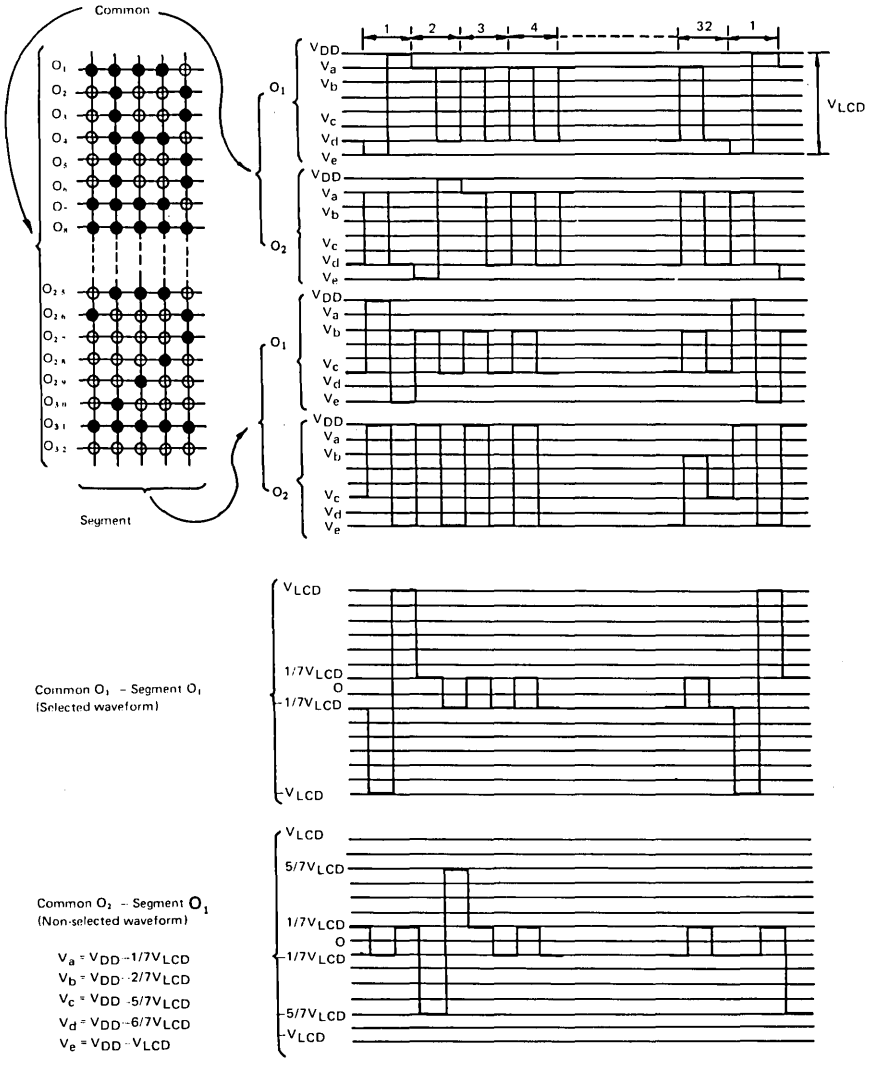
TIME CHART

1/32 duty, 1/7 bias



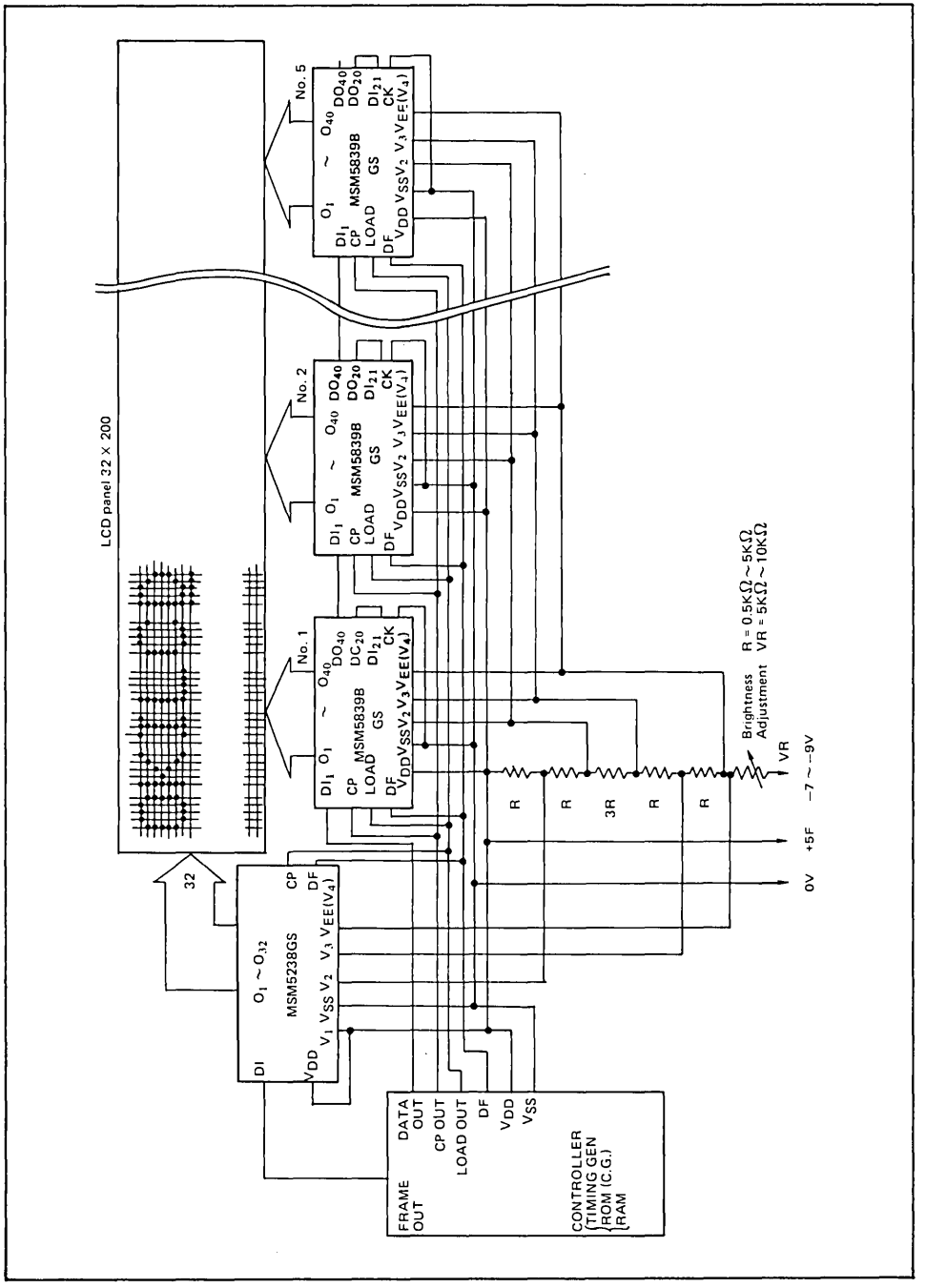
LCD DRIVING WAVEFORM

1/32 duty, 1/7 bias



$V_a = V_{DD} - 1/7V_{LCD}$
$V_b = V_{DD} - 2/7V_{LCD}$
$V_c = V_{DD} - 5/7V_{LCD}$
$V_d = V_{DD} - 6/7V_{LCD}$
$V_e = V_{DD} - V_{LCD}$

TYPICAL APPLICATION CIRCUIT



MSM5839BGS

DOT MATRIX LCD 40 DOT SEGMENT DRIVER

GENERAL DESCRIPTION

The OKI MSM5839BGS is a dot matrix LCD's segment driver LSI which is fabricated by low power CMOS metal gate technology. This LSI consists of 40-bit shift register (two 20-bit shift registers), 40-bit latch (two 20-bit latches), 40-bit level shifter and 40-bit 4-level driver.

It converts serial data, which is received from LCD controller LSI, to parallel data and outputs LCD driving waveform to the LCD panel.

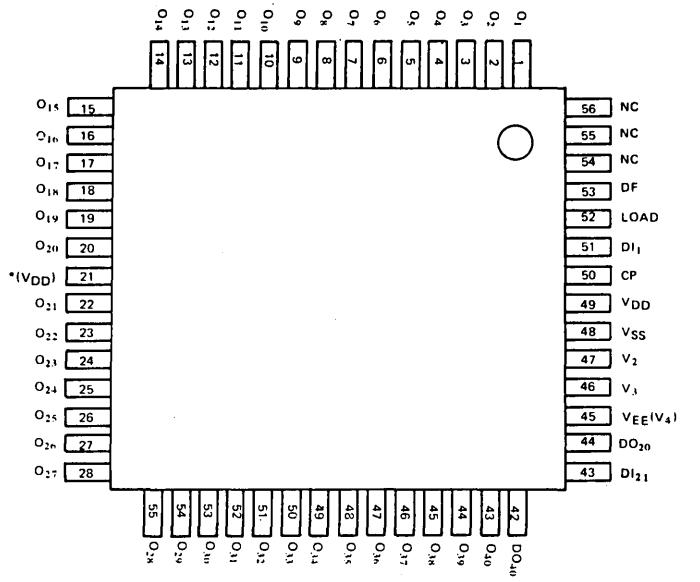
This LSI can drive a variety of LCD panel because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from the external source.

FEATURES

- Supply voltage: 4.5 ~ 5.5V
- LCD driving voltage: 8 ~ 18V
- Applicable LCD duty: 1/8 ~ 1/128
- Bias voltage can be supplied externally
- 56 pin plastic flat package

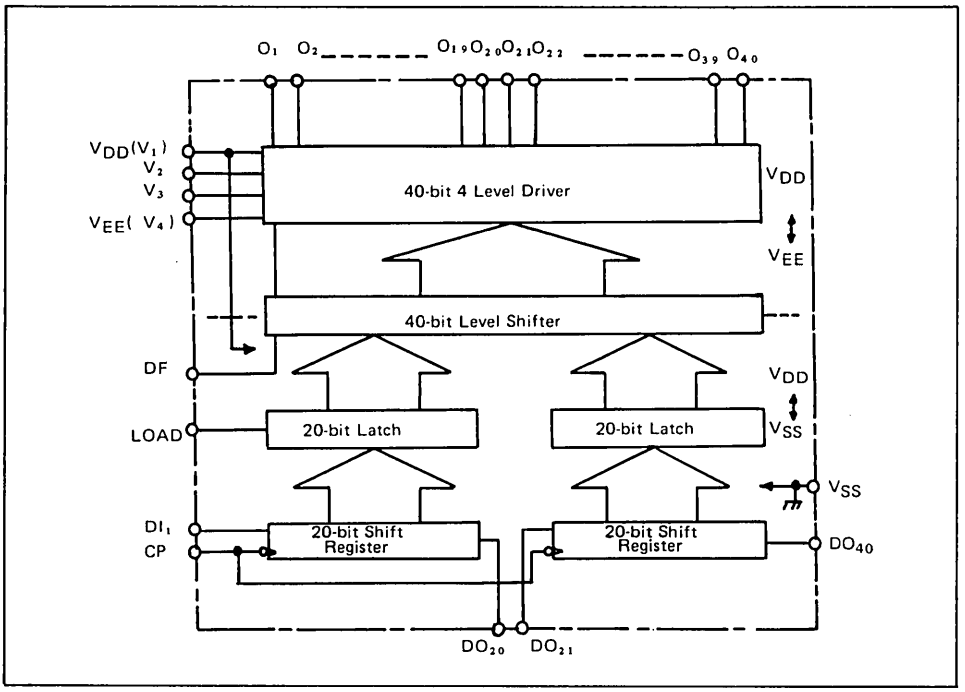
PIN CONFIGURATION

(Top View)



*This pin is internally connected with V_{DD}, so it must not be connected to other signals. It is also prohibited to use the 21 pin as a V_{DD} independently. This pin may be used as a line reinforcing V_{DD}.

BLOCK DIAGRAM

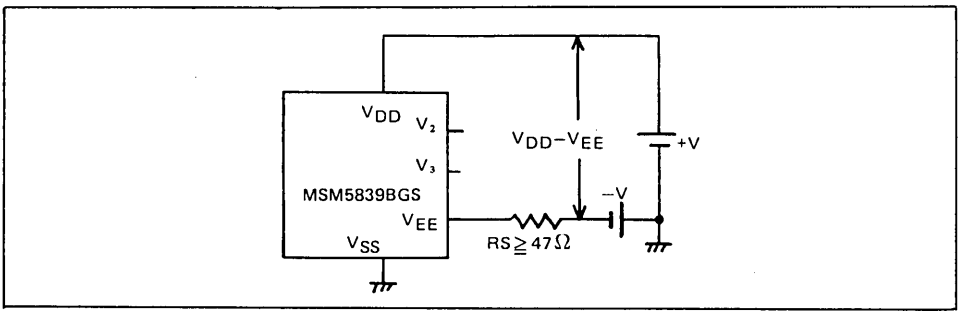


ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Value	Unit
Supply voltage (1)	V_{DD}	T_a = 25°C	−0.3 ~ 6	V
Supply voltage (2)	$V_{DD} - V_{EE}$*1	T_a = 25°C	0 ~ 18	V
	$V_{DD} - V_{EE}$*2	T_a = 25°C	0 ~ 18	V
Input voltage	V_I	T_a = 25°C	−0.3 ~ V_{DD} + 0.3	V
Storage temperature	T_{stg}	–	−55 ~ +150	°C

*1 : $V_{DD} > V_2 > V_3 > V_{EE}$

*2 : When a series resistance of more than 47Ω is connected as shown below.

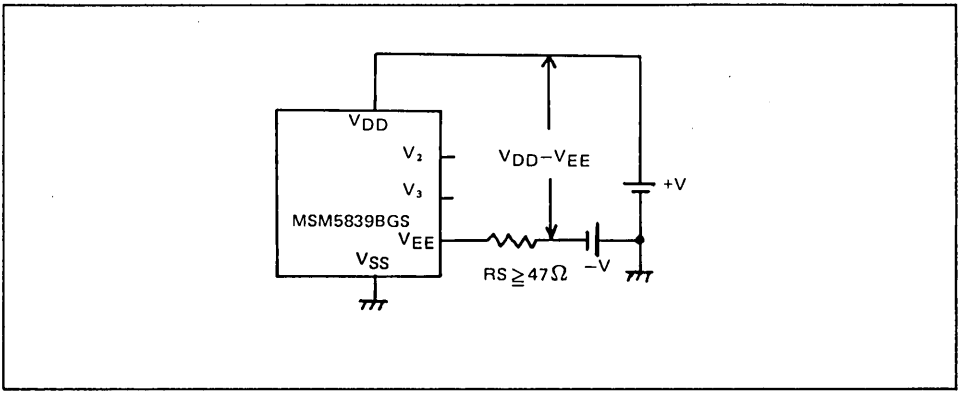


OPERATING RANGE

Item	Symbol	Condition	Limit	Unit
Supply voltage (1)	V_{DD}	–	4.5 ~ 5.5	V
Supply voltage (2)	$V_{DD} - V_{EE}$*1	–	8 ~ 16	V
	$V_{DD} - V_{EE}$*1*2	–	8 ~ 18	V
Operating temperature	T_{op}	–	−20 ~ +85	°C

*1 : $V_{DD} > V_2 > V_3 > V_{EE}$

*2 : When a series resistance of more than 47Ω is connected as shown below.



D.C. CHARACTERISTICS

(V_{DD} = 5V ± 10%, T_a = −20 ~ +85°C)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
"H" input voltage	V_{IH}*1	—	0.8V_{DD}	–	–	V
"L" input voltage	V_{IL}*1	—	–	–	0.2V_{DD}	V
"H" input current	I_{IH}*1	$V_{IH} = V_{DD}$	–	–	1	μA
"L" input current	I_{IL}*1	V_{IL} = 0V	–	–	−1	μA
"H" output voltage	V_{OH}*2	I_0 = −0.4mA	V_{DD} − 0.4	–	–	V
"L" output voltage	V_{OL}*2	I_0 = 0.4mA	–	–	0.4	V
ON registance	R_{ON}*4	$V_{DD} = V_{EE}$ = 10V $\lvert V_N - V_O \rvert$ = 0.25V*3	–	3.5	7	kΩ
Power consunption	I_{DD}	CP = DC $V_{DD} - V_{EE}$ = 18V No load	–	–	100	μA

*1 : LOAD, CP, DI_1, DI_{21}, DF

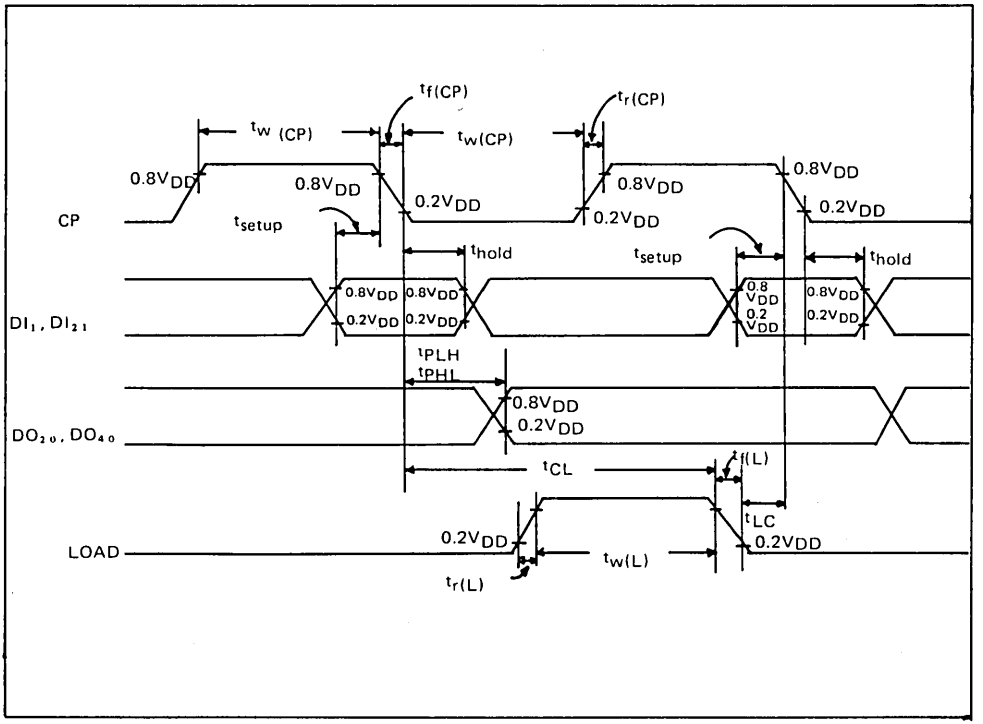
*2 : DO_{20}, DO_{40}

*3 : VN = V_{DD} ~ V_{EE}, $V_2 = \frac{8}{9}(V_{DD} - V_{EE})$, $V_3 = \frac{1}{9}(V_{DD} - V_{EE})$

*4 : Applicable to O_1 ~ O_{40}

SWITCHING CHARACTERISTICS

Item	Symbol	Condition	MIN	TYP	MAX	Unit
"H", "L" propagation delay time	t_{PLH} t_{PHL}	—	–	–	250	ns
Max. clock frequency	f_{CP}	DUTY = 50%	3.3	–	–	MHz
Clock pulse width	$t_{W(CP)}$	—	125	–	–	ns
LOAD pulse width	$t_{W(L)}$	—	125	–	–	ns
Data setup time DI → CP	t_{setup}	—	50	–	–	ns
CP → LOAD time	t_{CL}	—	250	–	–	ns
LOAD → CP time	t_{LC}	—	0	–	–	ns
DATA hold time DI → CP	t_{hold}	—	50	–	–	ns
CP Rising/Falling time	$t_{r(CP)}$ $t_{f(CP)}$	—	–	–	50	ns
LOAD Rising/Falling time	$t_{r(L)}$ $t_{f(L)}$	—	–	–	1	μs



PIN DESCRIPTION

- **DI_1**
  The 1st ~ 20th data from the LCD controller LSI is input to shift register from DI_1. (Positive logic)

- **CP**
  Clock pulse input pin for the two 20-bit shift register. The data is shifted to the two 20-bit latch at the falling edge of the clock pulse. A data setup time (t_{setup}) and data hold time (t_{hold}) are required each between DI_1, DI_{21} and CP.
  Schmit circuit is included in CP input circuit.

- **DO_{20}**
  The 20th bit of shift register contents is output from DO_{20} synchronized with the clock pulse. By connecting DO_{20} with DI_{21}, two 20-bit shift registers are connected and becomes 40-bit shift register.

- **DI_{21}**
  The 21st ~ 40th data from the LCD controller LSI is input to shift register from DI_{21}. By connecting DO_{20} with DI_{21}, two 20-bit shift registers are connected and becomes 40-bit shift register.

- **DO_{40}**
  The 40th bit of shift register contents is output from DO_{40} synchronized with the clock pulse. By connecting DO_{40} with next MSM5839BGS's DI_1, this LSI is applicable to a wide screen LCD. Refer to the sample application circuit.

- **DF**
  Alternate signal input pin for LCD driving waveform.

- **$V_{DD}(V_1)$, V_{SS}**
  Supply voltage pin. V_{DD} should be 4.5 ~ 5.5V.
  V_{SS} is a ground pin (V_{SS} = 0V).

- **V_1 (V_{DD}), V_2, V_3, V_{EE} (V_4)**
  Bias supply voltage pin to drive the LCD. Bias voltage divided by the resistance is usually used as supply voltage source.

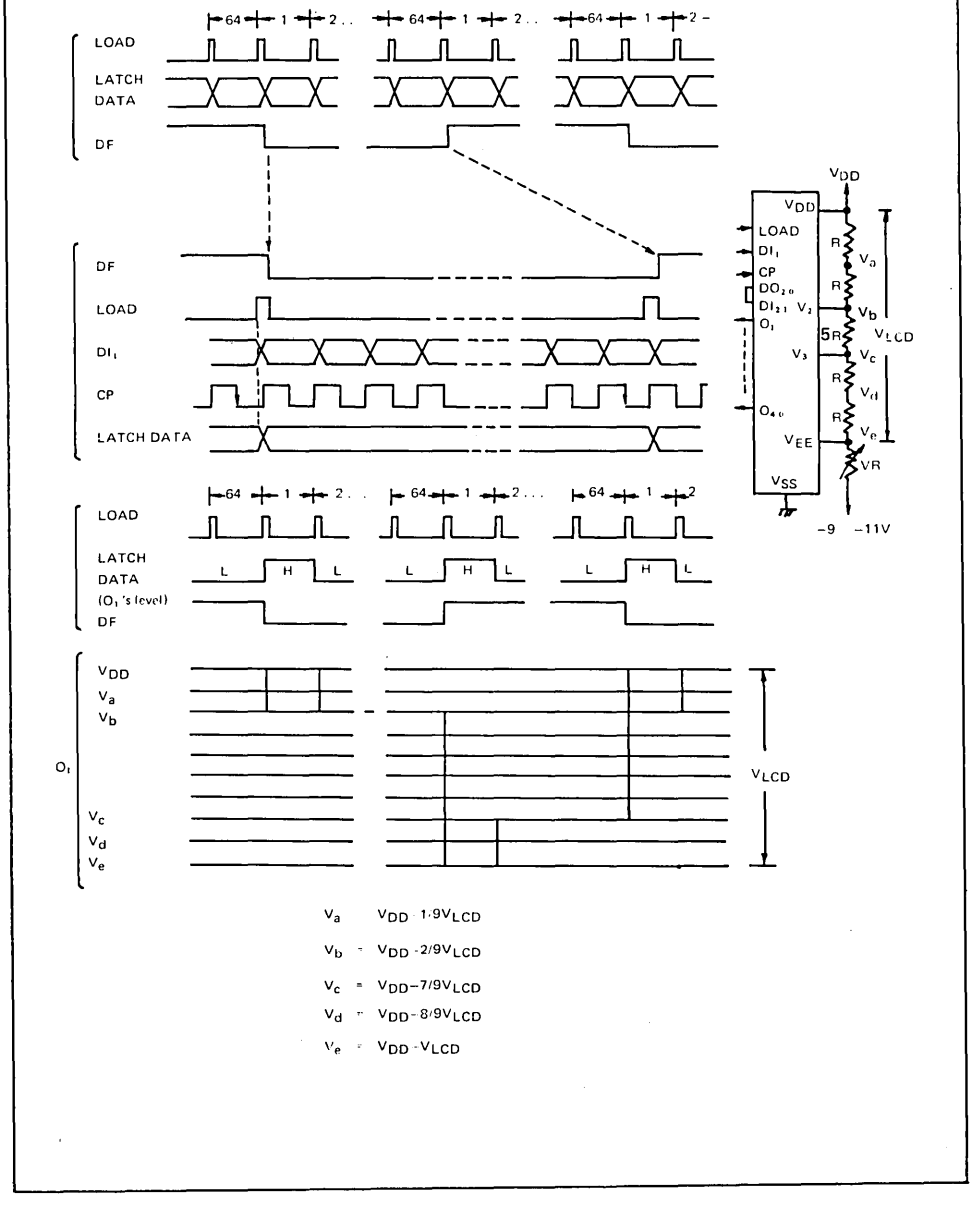
- **LOAD**
  The signal for latching the shift register contents is input from this pin.
  When LOAD pin is set at "H", the shift register contents are transferred to 40-bit 4-level driver. When LOAD pin is set at "L", the last display output data (O_1 ~ O_{40}), which was transferred when LOAD pin was at "H", is held.

- **O_1 ~ O_{40}**
  Display data output pins which correspond to each data bit in the latch.
  One of V_{DD}, V_2, V_3 or V_{EE} is selected as a display driving voltage source according to the combination of latched data level and DF signal.
  These pins should be connected to the SEGMENT side of the LCD panel. Refer to the truth table below.

Latched data	DF	Display data output level
H	H	V_{EE} (V_4)
	L	V_{DD}
L	H	V_3
	L	V_2

TIME CHART

1/64 duty, 1/9 bias



$V_a = V_{DD} - 1/9V_{LCD}$

$V_b = V_{DD} - 2/9V_{LCD}$

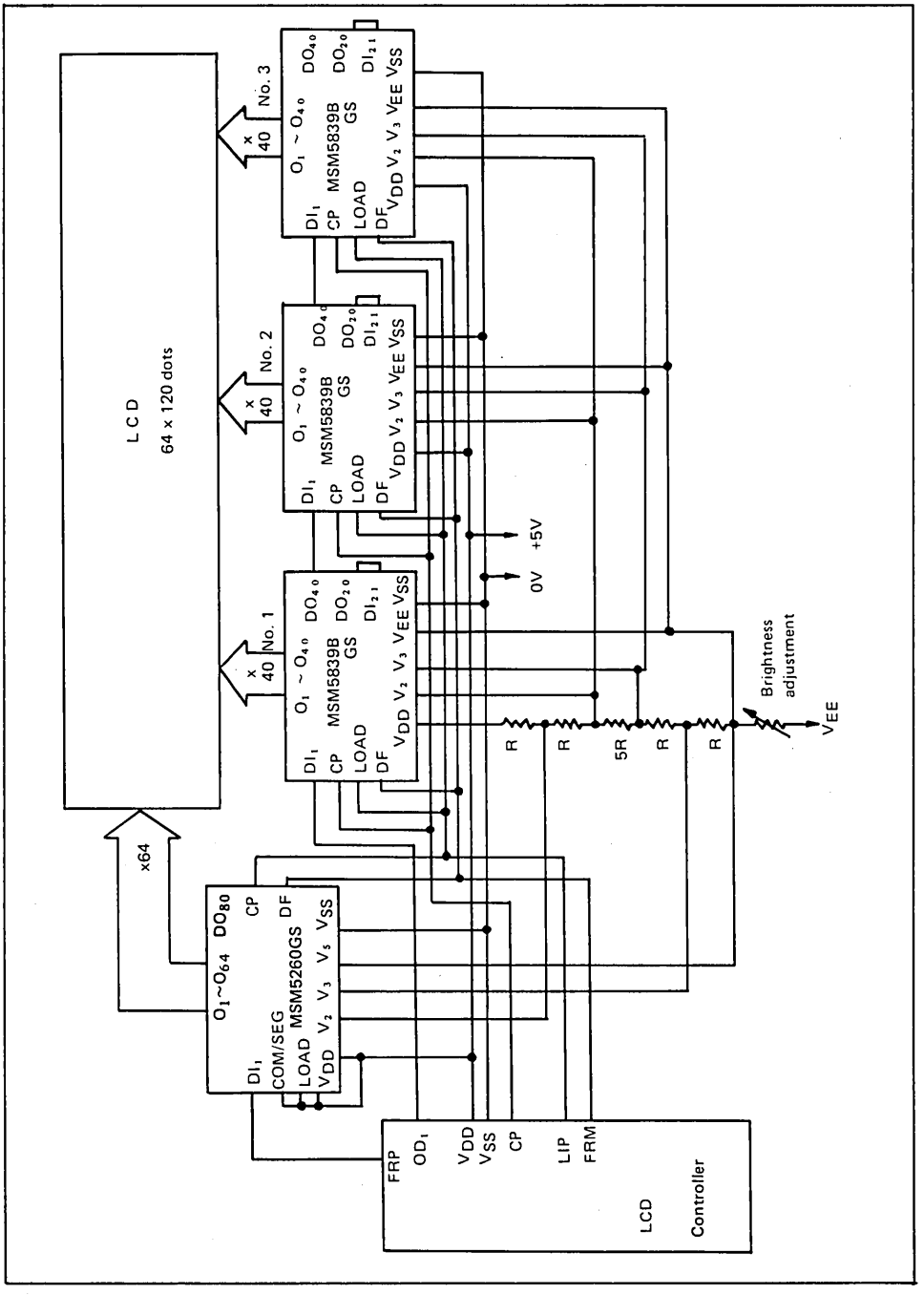
$V_c = V_{DD} - 7/9V_{LCD}$

$V_d = V_{DD} - 8/9V_{LCD}$

$V_e = V_{DD} - V_{LCD}$

TYPICAL APPLICATION CIRCUIT

1/64 duty, 1/9 bias



MSM5259GS

DOT MATRIX LCD 40 DOT SEGMENT DRIVER

GENERAL DISCRIPTION

The OKI MSM5259GS is a dot matrix LCD's segment driver which is fabricated by low power CMOS metal gate technology. This LSI consists of 40-bit shift register (two 20-bit shift registers), 40-bit latch and 40-bit 4-level driver.

It converts serial data, which is received from LCD controller LSI, to parallel data and output LCD driving waveform to LCD.

Expansion of display can be easily made according to the number and structure of characters. Its 40-bit shift register consists of two 20-bit shift registers and this make it possible to allot bits efficiently according to the numbers of characters.

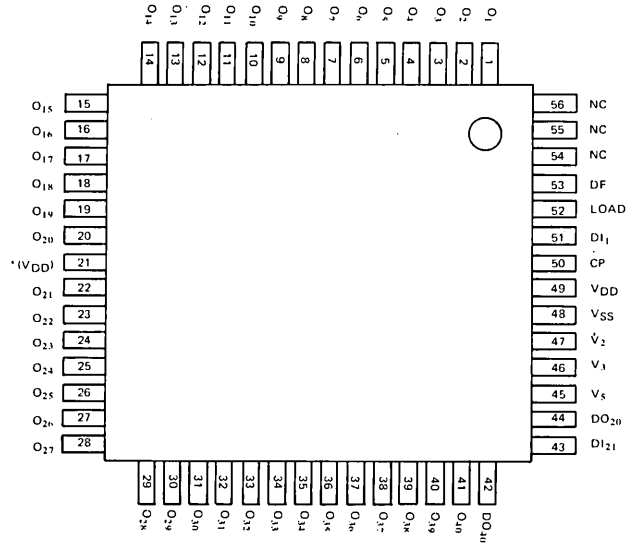
The MSM5259GS can drive a variety of LCD panel because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from the external source.

FEATURES

- Supply voltage: 3.5 ~ 6.0V
- LCD driving voltage: 3.0 ~ 6.0V
- Applicable LCD duty: 1/8 ~ 1/16
- Interface with MSM6222GS (LCD controller LSI with 16-bit common driver and 40-bit segment driver)
- 56 pin plastic flat package (bent lead)
- Bias voltage can be supplied externally

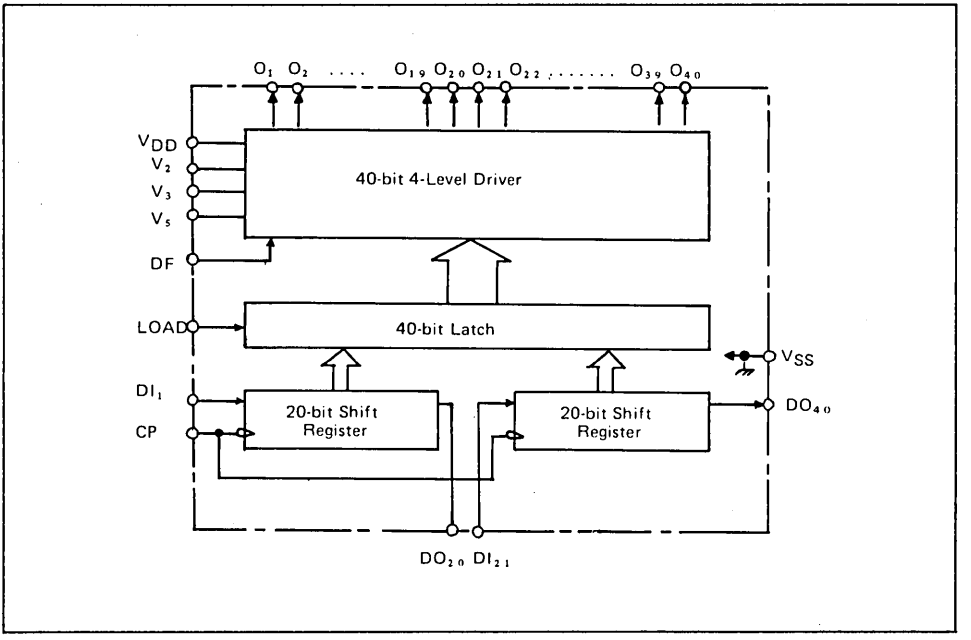
PIN CONFIGULATION

(Top View)



*21 pin is used as a V_{DD} supporting pin, however, 21 pin alone cannot be used as V_{DD} pin.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Limits	Unit
Supply voltage (1)	V_{DD}	Ta = 25°C	−0.3 ~ +6.5	V
Supply voltage (2)	$V_{DD} - V_5$ *1		0 ~ +6.5	V
Input voltage	V_I		−0.3 ~ V_{DD} + 0.3	V
Storage temperature	T_{stg}	—	−55 ~ +150	°C

OPERATING RANGE

Item	Symbol	Condition	Limits	Unit
Supply voltage (1)	V_{DD}	—	3.5 ~ 6.0	V
Supply voltage (2)	$V_{DD} - V_5$ *1	—	3.0 ~ 6.0*2	V
Operating temperature	T_{op}	—	−20 ~ +85	°C

*1. $V_{DD} > V_2 \geq V_3 > V_5 \geq V_{SS}$ (Dynamic display)
$V_{SS} = V_3 > V_2 = V_5 = V_{SS}$ (Static display)

*2. To decide the LCD driving voltage, change the value of V_5. (Minimum 0V)

D.C. CHARACTERISTICS

(V_{DD} = 5 ± 10%, Ta = −20 ~ 85°C)

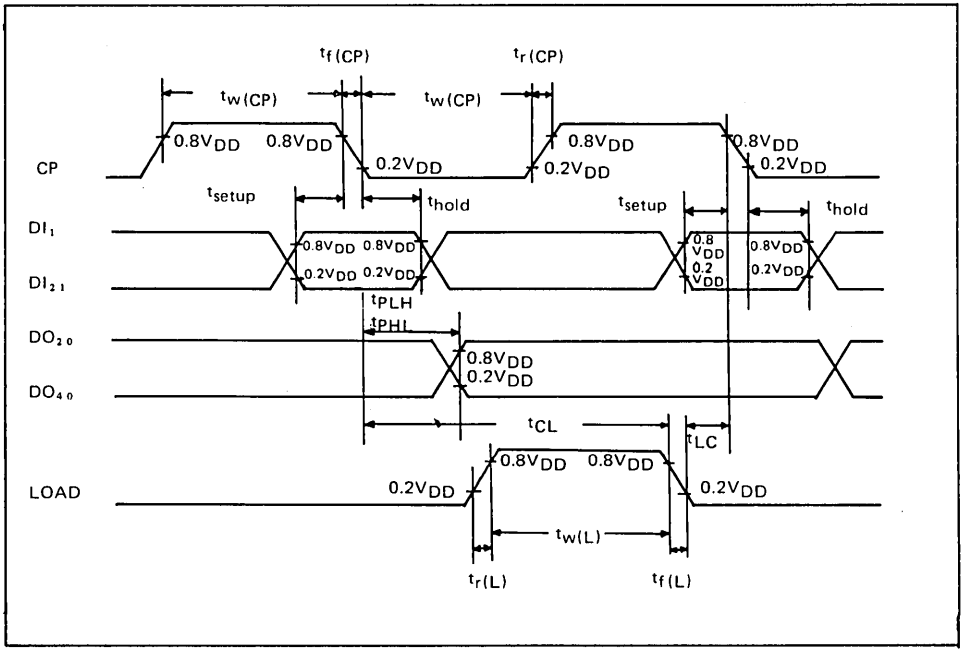
Item	Symbol	Condition	MIN	TYP	MAX	Unit
"H" input voltage	V_{IH}*1	—	0.8V_{DD}	–	–	V
"L" input voltage	V_{IL}*1	—	–	–	0.2V_{DD}	V
"H" input current	I_{IH}*1	$V_{IH} = V_{DD}$	–	–	1	μA
"L" input current	I_{IL}*1	V_{IL} = 0V	–	–	−1	μA
"H" output voltage	V_{OH}*2	I_O = −40μA	4.2	–	–	V
"L" output voltage	V_{OL}*2	I_O = 0.4mA	–	–	0.4	V
ON resistance	R_{ON}*3	$V_{DD} - V_5$ = 5V $\lvert V_N - V_O \rvert$ = 0.25V*4	–	–	5	kΩ
Current consumption	I_{DD}	CP = DC, No load	–	–	0.5	mA

*1. Applicable to DF, LOAD, DI_1 and DI_{21} terminals.
*2. Applicable to DO_{20} and DO_{40} terminals.
*3. Applicable to $O_1 \sim O_{40}$ terminals.
*4. $V_N = V_{DD} \sim V_5$, $V_2 = \frac{2}{3}(V_{DD} - V_5)$, $V_3 = \frac{1}{3}(V_{DD} - V_5)$

SWITCHING CHARACTERISTICS

(V_{DD} = 5 ± 10%, Ta = −20 ~ +85°C, C_L = 15pF)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
"H", "L" propagation delay time	t_{PLH} t_{PHL}	—	–	–	250	ns
Max. clock frequency	f_{CP}	Duty = 50%	3.3	–	–	MHz
Clock pulse width	$t_{W(CP)}$	—	125	–	–	ns
Load pulse width	$t_{W(L)}$	—	125	–	–	ns
Data set-up time, DI → CP	t_{setup}	—	50	–	–	ns
CP → LOAD time	t_{CL}	—	250	–	–	ns
LOAD → CP time	t_{LC}	—	0	–	–	ns
Data hold time DI → CP	t_{hold}	—	50	–	–	ns
Clock pulse Rising/Falling time	$t_{r(CP)}$ $t_{f(CP)}$	—	–	–	50	ns
Load pulse Rising/Falling time	$t_{r(L)}$ $t_{f(L)}$	—	–	–	1	μs



PIN DESCRIPTION

- **DI_1, DI_{21}**
  The date (1st ~ 20th bit) from the LCD controller LSI is input to 20-bit shift register from DI_1. The data (21st ~ 40th bit) is input to another 20-bit shift register from DI_{21}.
  (Positive logic)

- **CP**
  Clock pulse input pin for the two 20-bit shift register. The data is shifted to 40-bit latch at the falling edge of the clock pulse. A data set up time (t_{setup}) and data hold time (t_{hold}) are required between a DI_1 signal and a clock pulse.
  Clock pulse rising time (t_r) and clock pulse falling time (t_f) should be maximum 50ns respectively.

- **DO_{20}**
  20th bit of the shift register contents is output from DO_{20}. The data which was input from DI_1 is output from this pin with 20 bits' delay, synchronized with the clock pulse. By connecting DO_{20} to DI_{21}, two 20-bit shift registers can be used as a 40-bit shift register.

- **DO_{40}**
  40th bit of the shift register contents is output from DO_{40}. The data which was input from DI_{21} is output from this pin with 20 bits' delay, synchronized with the clock pulse. By connecting DO_{40} to the next MSM5259GS's DI_1, this LSI is applicable to a wide screen LCD.
  Refer to the application circuit.

- **DF**
  Alternate signal input pin for LCD driving.

- **LOAD**
  The signal for latching the shift register contents is input from this pin.
  When LOAD pin is set at "H" level, the shift register contents are transferred to the 40-bit 4-level driver. When LOAD pin is set at "L" level, the last display output data (O_1 ~ O_{40}), which was transferred when LOAD pin was at "H" level, is held.

- **V_{DD}, V_{SS}**
  Supply voltage pins. V_{DD} should be 3.0 ~ 6.0V.
  V_{SS} is a ground pin (V_{SS} = 0V)

- **V_{DD}, V_2, V_3, V_5**
  Bias supply voltage pins to drive the LCD. Bias voltage divided by the register is usually used as supply voltage source.
  Refer to the application circuit.

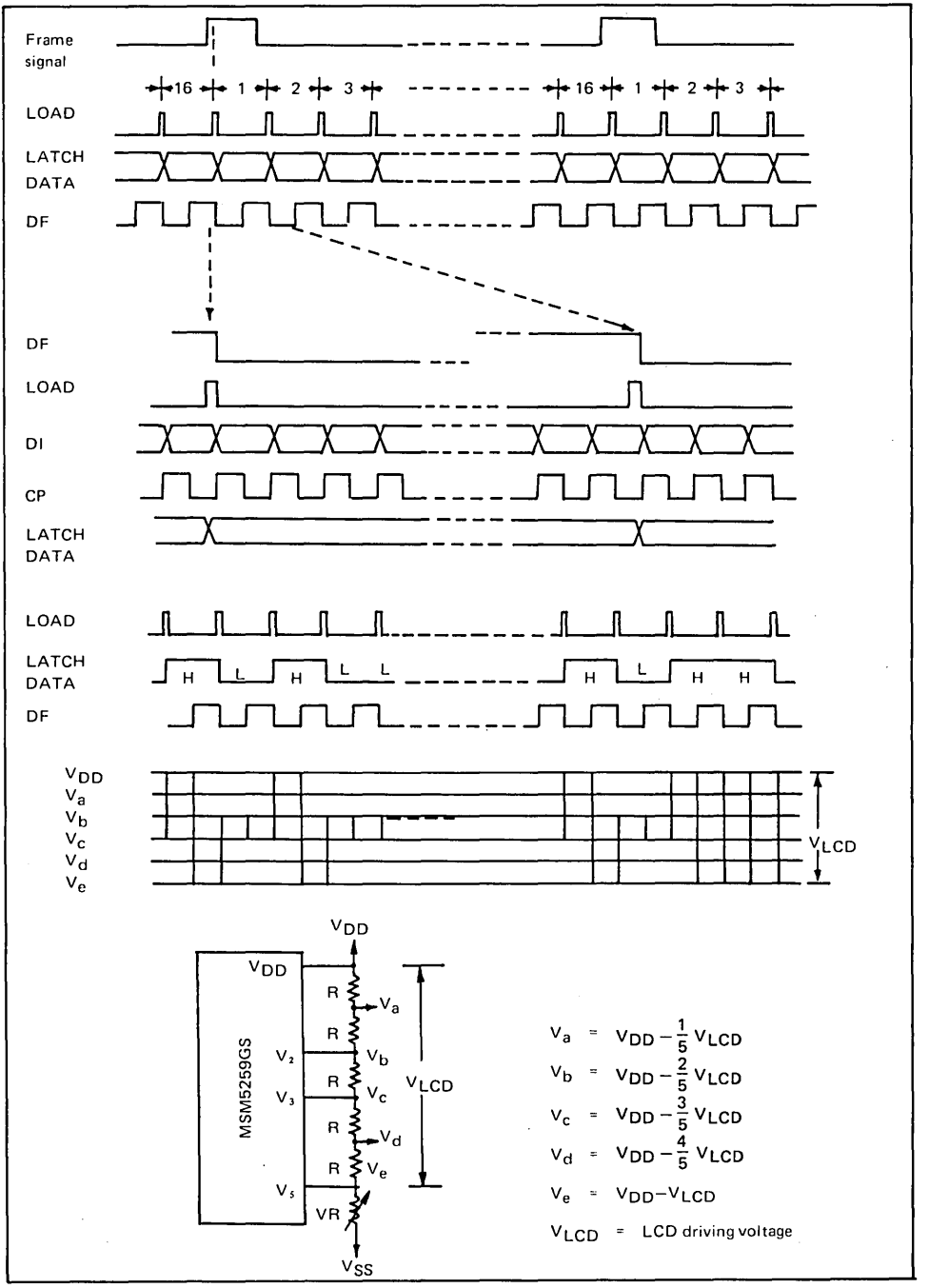
- **O_1 ~ O_{40}**
  Display data output pin which corresponds to each data bit in the latch.
  One of V_{DD}, V_2, V_3 and V_5 is selected as a display driving voltage source according to the combination of latched data level and DF signal.
  (Refer to the truth table below)

Latched data	DF	Display data output level
"H" (Selected)	H	V_5
	L	VDD
"L" (Non-selected)	H	V_3
	L	V_2

Truth Table

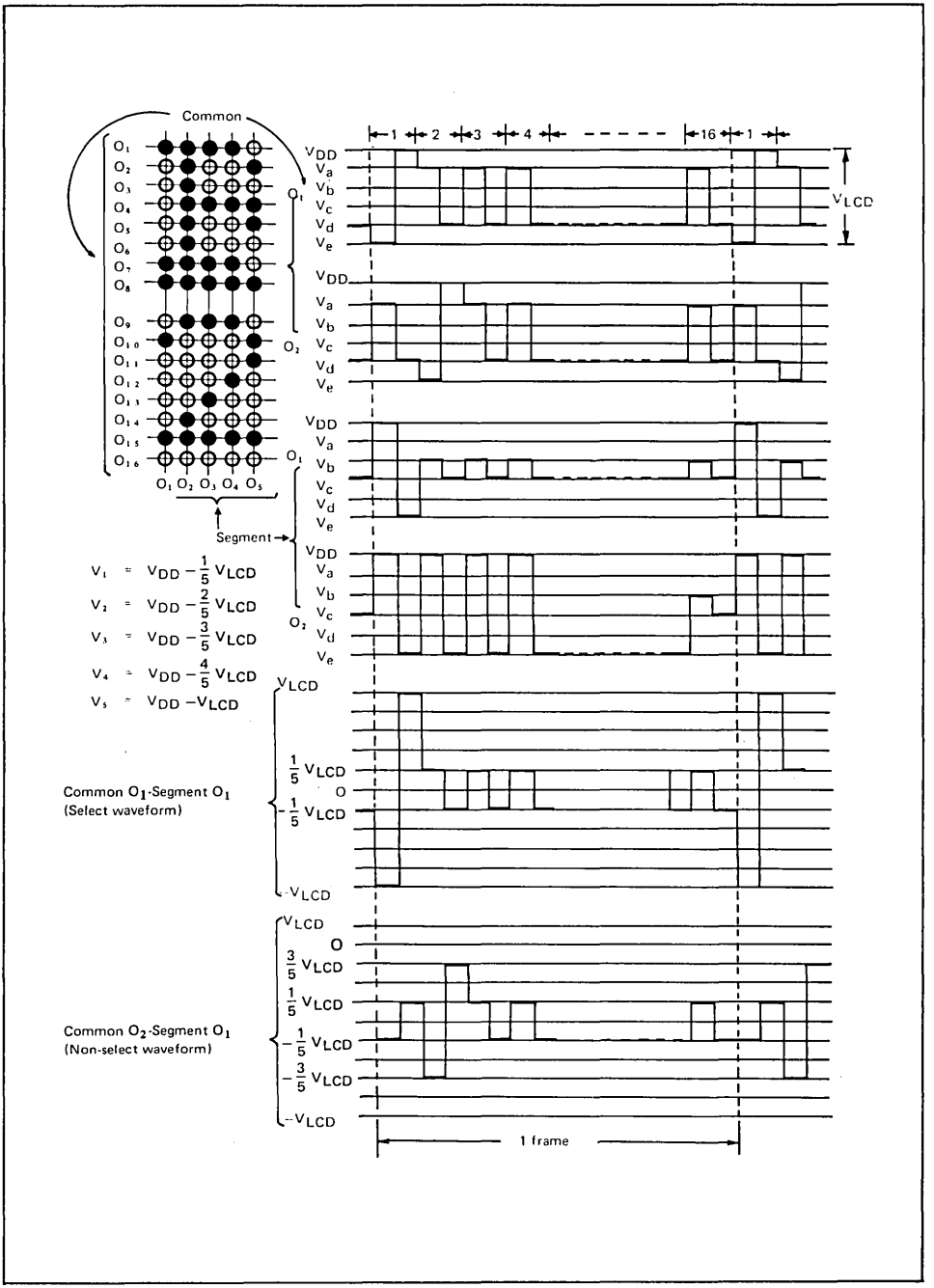
TIME CHART

1/5 bias, 1/16 duty



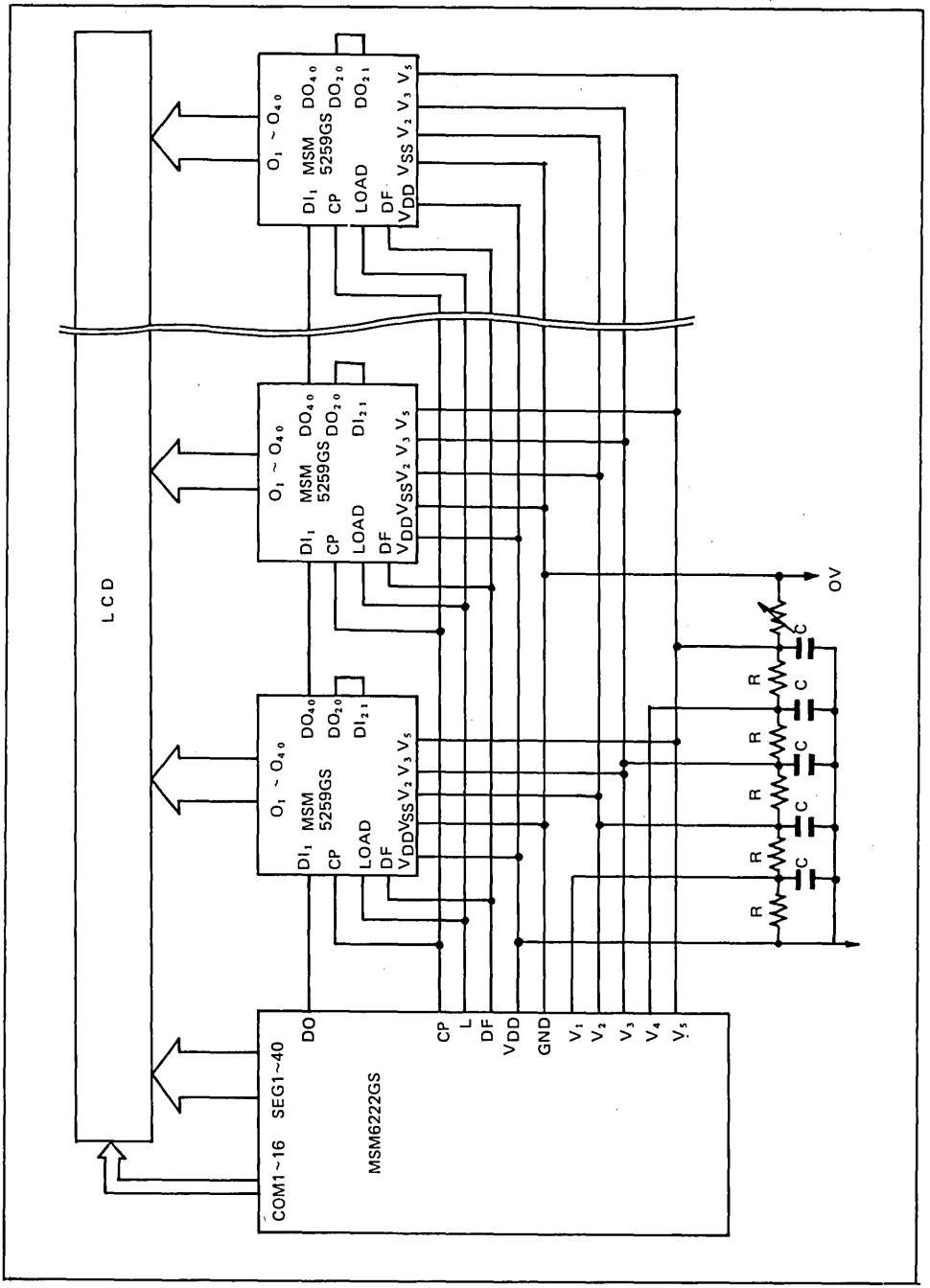
LCD DRIVING WAVEFORM

1/5 bias, 1/16 duty



TYPICAL APPLICATION CIRCUIT

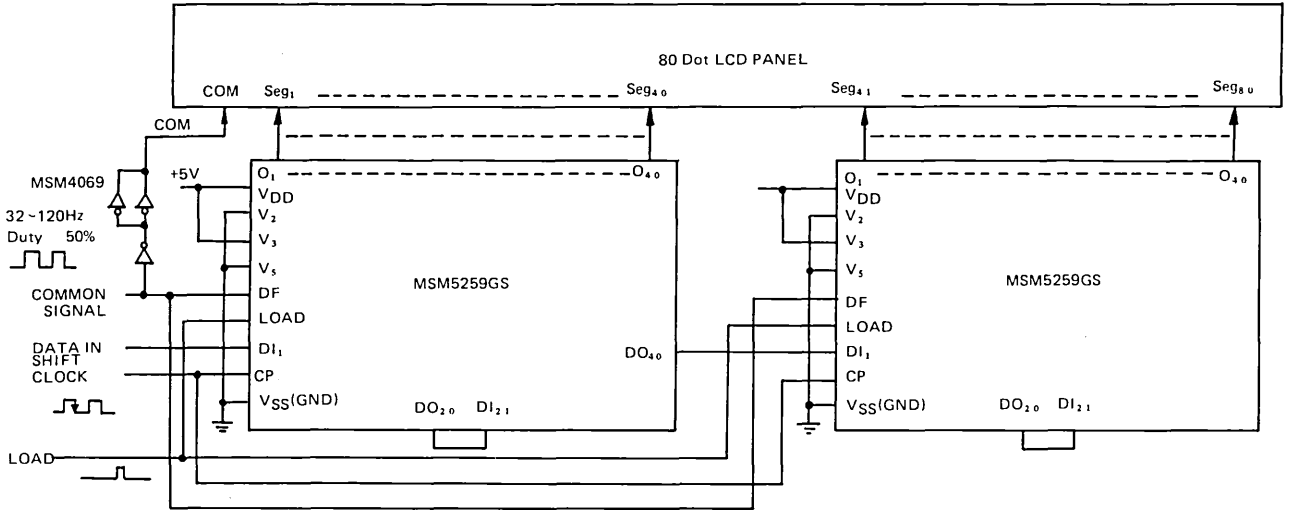
(Connected to MSM6222GS LCD Controller)



TYPICAL APPLICATION CIRCUIT FOR STATIC DISPLAY

The MSM5259GS is applicable to a static LCD by setting V_2 and V_5 at ground level, connecting V_3 to V_{DD} and inputting COMMON SIGNAL to DF pin.

This sample application circuit below is the case when the MSM5259GS is applied to a 80-bit LCD panel by connecting two MSM5259GS in series.



MSM5260GS

DOT MATRIX LCD 80 DOT COMMON/SEGMENT DRIVER

GENERAL DESCRIPTION

The OKI MSM5260 is a dot matrix common/segment LCD driver LSI which is fabricated by low power CMOS metal gate technology. This LSI consists of 80-bit shift register, 80-bit data latch, 80-bit level shifter and 80-bit 4-level driver.

It converts serial data, which is received from LCD controller LSI, to parallel data and outputs LCD driving waveform to LCD.

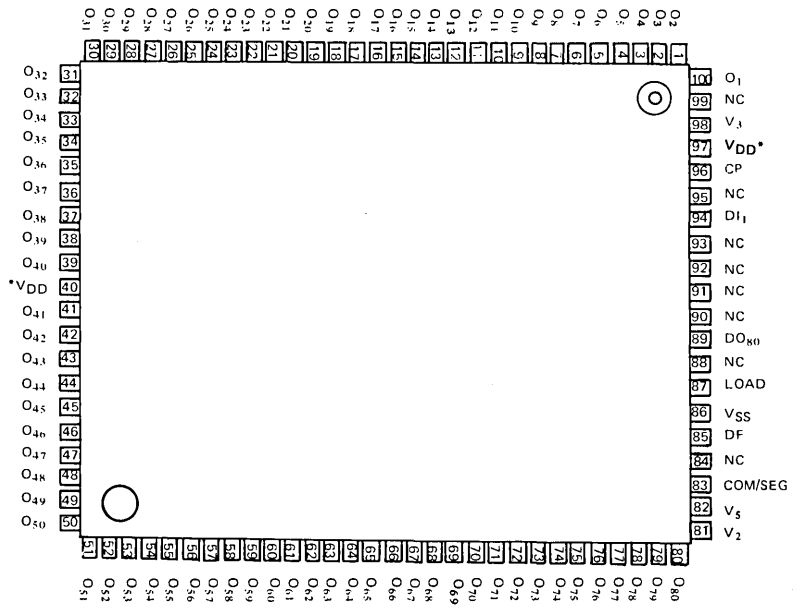
This LSI can drive a variety of LCD pannel because the bias voltage can be optionally provided from the external source.

FEATURES

- Supply voltage: 4.5 ~ 5.5V
- LCD driving voltage: 8 ~ 18V
- Duty 1/1 ~ 1/128
- Bias voltage can be supplied externally
- Can be used either as common driver or segment driver
- Interface with MSM6240GS LCD controller LSI
- 100 pin plastic flat package

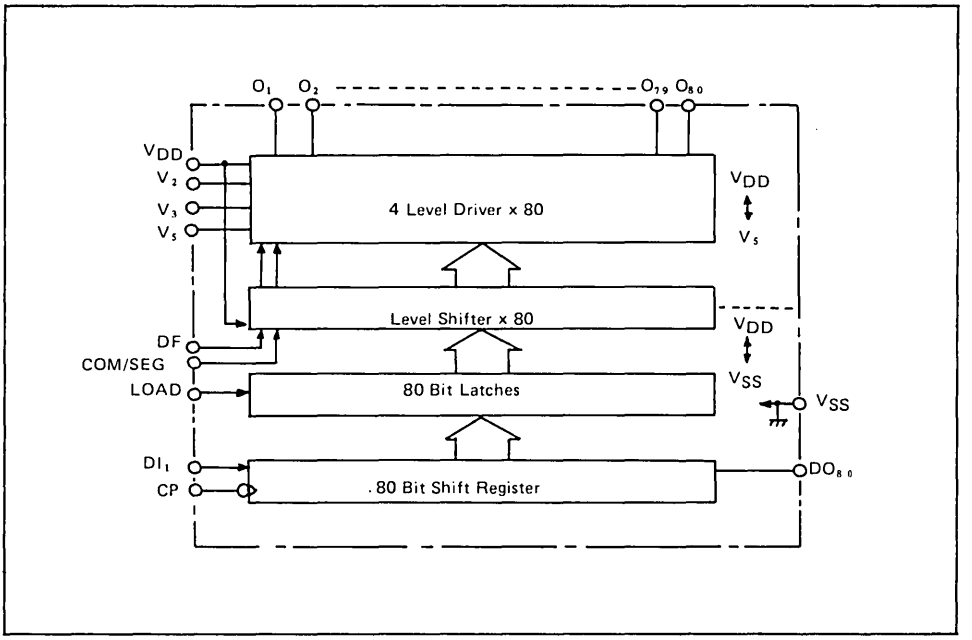
PIN CONFIGURATION

(Top View)



*V_{DD} must be supplied to both 40 pin and 97 pin.

BLOCK DIAGRAM

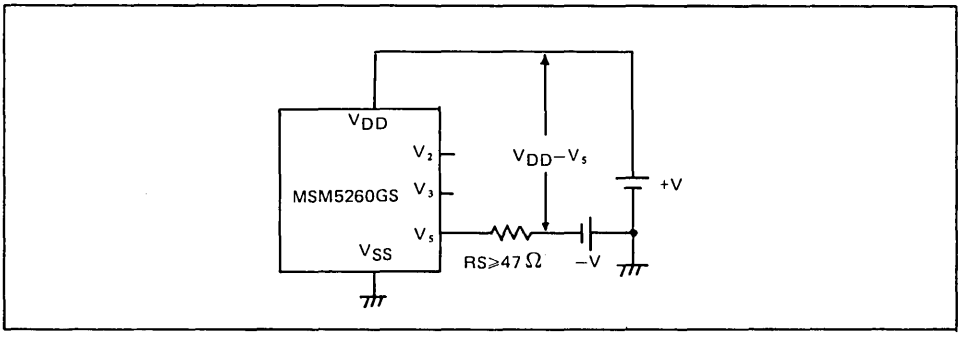


ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Limit	Unit
Supply Voltage (1)	V_{DD}	Ta = 25°C	−0.3 ~ 6	V
Supply Voltage (2)	$V_{DD} - V_5$ *1 $V_{DD} - V_5$ *2	Ta = 25°C Ta = 25°C	0 ~ 18 0 ~ 20	V V
Input Voltage	V_I	Ta = 25°C	−0.3 ~ V_{DD} + 0.3	V
Storage Temperature	V_{stg}	—	−55 ~ +150	°C

*1 : $V_{DD} > V_2 > V_3 > V_5$

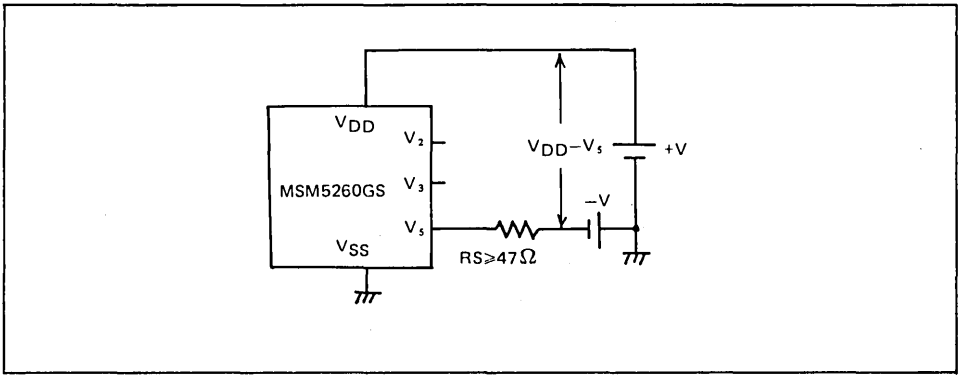
*2 : When a series resistance of more than 47Ω is connected as shown below:



OPERATING RANGE

Parameter	Symbol	Condition	Limit	Unit
Supply Voltage (1)*1	V_{DD}	—	4.5 ~ 5.5	V
Supply Voltage (2)*1 *2	$V_{DD} - V_5$*1	—	8 ~ 16	V
	$V_{DD} - V_5$*1 *2	—	8 ~ 18	V
Operating Temperature	Top	—	−20 ~ +85	°C

*1 : $V_{DD} > V_2 > V_3 > V_5$
*2 : When a series resistance of more than 47Ω is connected as shown below:



D.C. CHARACTERISTICS

(V_{DD} = 5V ± 10% T_a = −20 ~ +85°C)

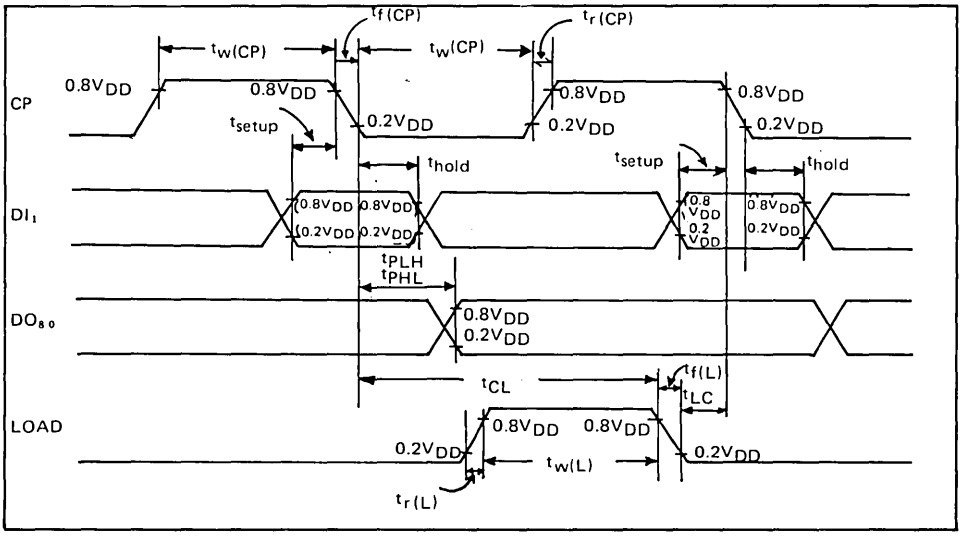
Parameter	Symbol	Condition	Value			Unit
			MIN	TYP	MAX	
"H" Input Voltage	V_{IH}*1		0.8V_{DD}	—	—	V
"L" Input Voltage	V_{IL}*1		—	—	0.2V_{DD}	V
"H" Input Current	I_{IH}*1	$V_{IH} = V_{DD}$	—	—	1	μA
"L" Input Current	I_{IL}*1	V_{IL} = 0V	—	—	−1	μA
"H" Output Voltage	V_{OH}*2	I_O = −0.4 mA	V_{DD} − 0.4	—	—	V
"L" Output Voltage	V_{OL}*2	I_O = 0.4 mA	—	—	0.4	V
ON Resistance	R_{ON}*4	$V_{DD} - V_5$ = 10V $\lvert V_N - V_O \rvert$ = 0.25*3	—	—	2	kΩ
Power Consumption	I_{DD}	CP = DC $V_{DD} - V_5$ = 18V No load	—	—	100	μA

*1 Applicable to LOAD, CP, DT_1, DF and COM/SEG pins.
*2 DO_{80}
*3 $V_N = V_{DD} \sim V_5$ V_2 = 8/9 ($V_{DD} - V_5$) V_3 = 1/9 ($V_{DD} - V_5$)
*4 Applicable to $O_1 \sim O_{80}$ display data output pin.

SWITCHING CHARACTERISTICS

(V_{DD} = 5V ± 10%, T_a = 20 ~ 85°C. CL = 15pF)

Parameter	Symbol	Condition	Value			Unit
			MIN	TYP	MAX	
"H", "L" Propagation Delay Time	t_{PLH} t_{PHL}	—	–	–	250	ns
Max. Clock Frequency	f_{CP}	Duty = 50%	3.3	–	–	MHz
Clock Pulse Width	$t_{W(CP)}$	—	125	–	–	ns
LOAD Pulse Width	$t_{W(L)}$	—	125	–	–	ns
Data Set-up Time $D_I \rightarrow$ CP	t_{setup}	—	50	–	–	ns
CP → LOAD Time	t_{CL}	—	250	–	–	ns
LOAD → CP Time	t_{LC}	—	0	–	–	ns
Data Hold Time DI → CP	t_{hold}	—	50	–	–	ns
CP Rising/Falling Time	$t_{r(CP)}$ $t_{f(CP)}$	—	–	–	50	ns
LOAD Rising/Falling Time	$t_{r(L)}$ $t_{f(L)}$	—	–	–	1	μs



PIN DESCRIPTION

- **DI_1**
  The date from the LCD controller LSI is input to 80-bit shift register from DI_1. (Positive logic)

- **CP**
  Clock pulse input pin for 80-bit shift register. The data is shifted to 80-bit latch at the falling edge of the clock pulse. A data set up time (t_{setup}) and a data hold time (t_{hold}) are required between a DI_1 signal and a clock pulse.
  Clock pulse rising time (t_r) and clock pulse falling time (t_f) should be maximum 50 ns respectively.

- **DO_{80}**
  80th bit of the shift register contents is output from DO_{80}. The data which was input from DI_1 is output from this pin with 80 bits' delay, synchronized with the clock pulse. By connecting DO_{80} with next MSM5260GS's DI_1, this LSI is applicable to a wide screen LCD. Refer to the application circuit.

- **LOAD**
  The signal for latching the shift register contents is input from this pin.
  When LOAD pin is set at "H" level, the shift register contents are transferred to 80-bit 4-level driver through 80-bit level shifter.
  When LOAD pin is set at low level, the last display output data ($O_1 \sim O_{80}$), which was transferred when LOAD pin was at high level, is held.

- **DF**
  Alternate signal input pin for LCD driving.

- **COM/SEG**
  Selection signal input pin. MSM5260GS is used either as common driver or segment driver according to input signal level at COM/SEG pin.
  When this pin is set at high level, MSM5260 is used as a common driver, while it is used as a row driver at low level.

  The display driving data $O_1 \sim O_{80}$, which are determined according to the combination of latched data and DF signal, are shown in the Table 1 below.

COM/SEG	Latched data level	DF	Display data output level ($O_1 \sim O_{80}$)	Note
H	High (Selected)	H	V_{DD}	Common driver
		L	V_5	
	Low (Non-selected)	H	V_3	
		L	V_2	
L	High (Selected)	H	V_5	Segment driver
		L	V_{DD}	
	Low (Non-selected)	H	V_3	
		L	V_2	

Table 1

When MSM5260GS is used as common driver, both LOAD pin and COM/SEG pin are to be connected to V_{DD}. In this case, a bias voltage of common side's non-selected level is to be supplied to V_2 and V_3 pins.

- **V_{DD}, V_{SS}**
  Supply voltage pins. V_{DD} should be 4.5 ~ 5.5V: V_{SS} is a ground pin (V_{SS} = 0V)

- **V_{DD}, V_2, V_3, V_5**
  Bias supply voltage pin to drive the LCD. Bias voltage divided by the register is usually used as supply voltage source.
  Figure 1 shows the case when bias voltage, which is used to drive the LCD, is obtained by the voltage disivion by external registers.

- **$O_1 \sim O_{80}$**
  Display data output pins which correspond to the 80-bit latch contents.
  One of V_{DD}, V_2, V_3 and V_5 is selected as a display driving voltage source according to the combination of latched data level and DF signal. (Refer to the time chart and Table 1.)

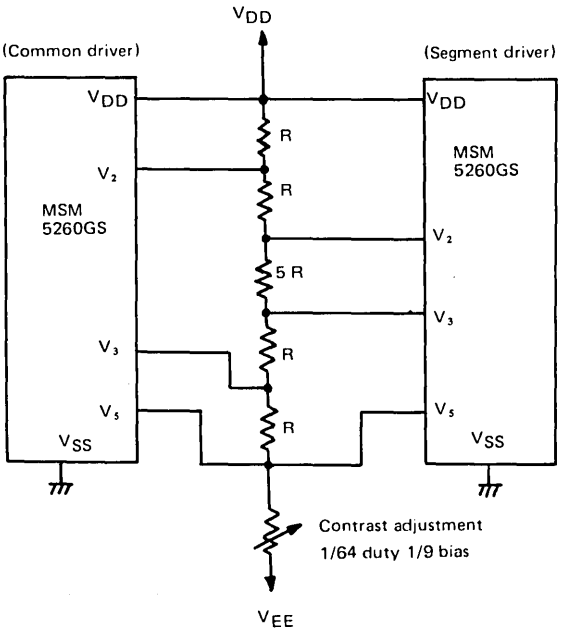
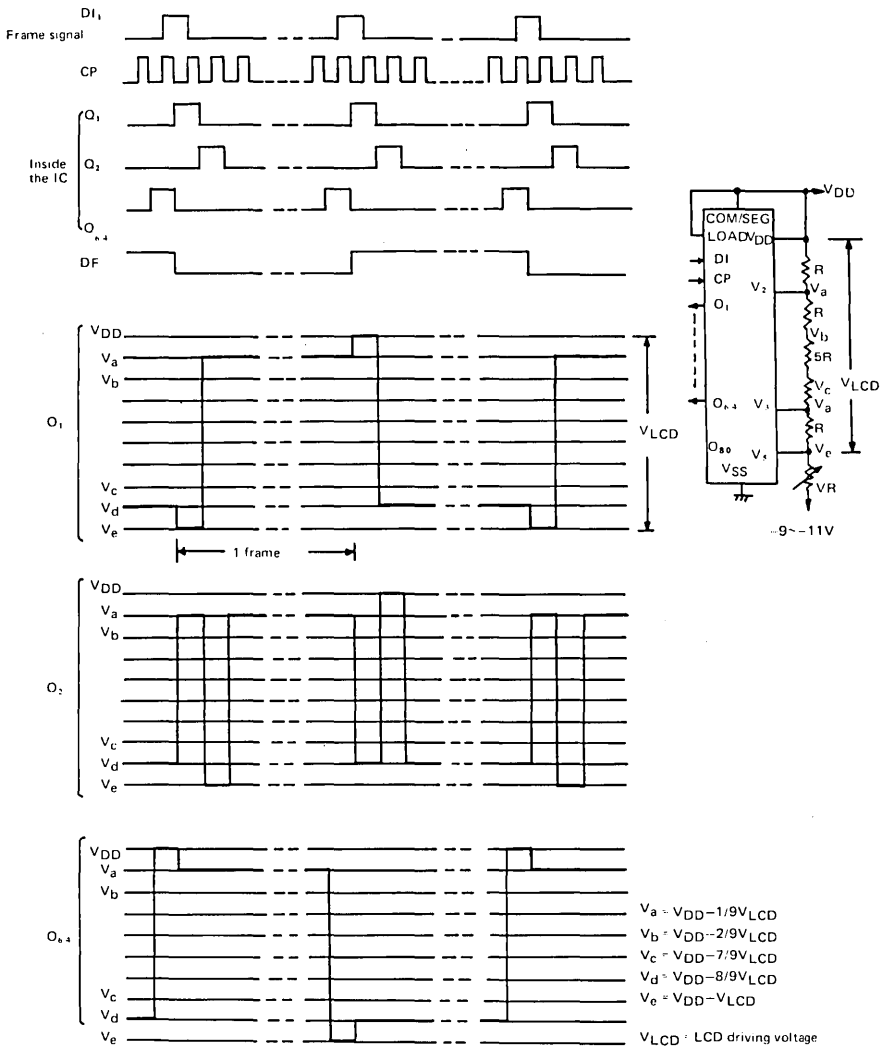


Figure 1

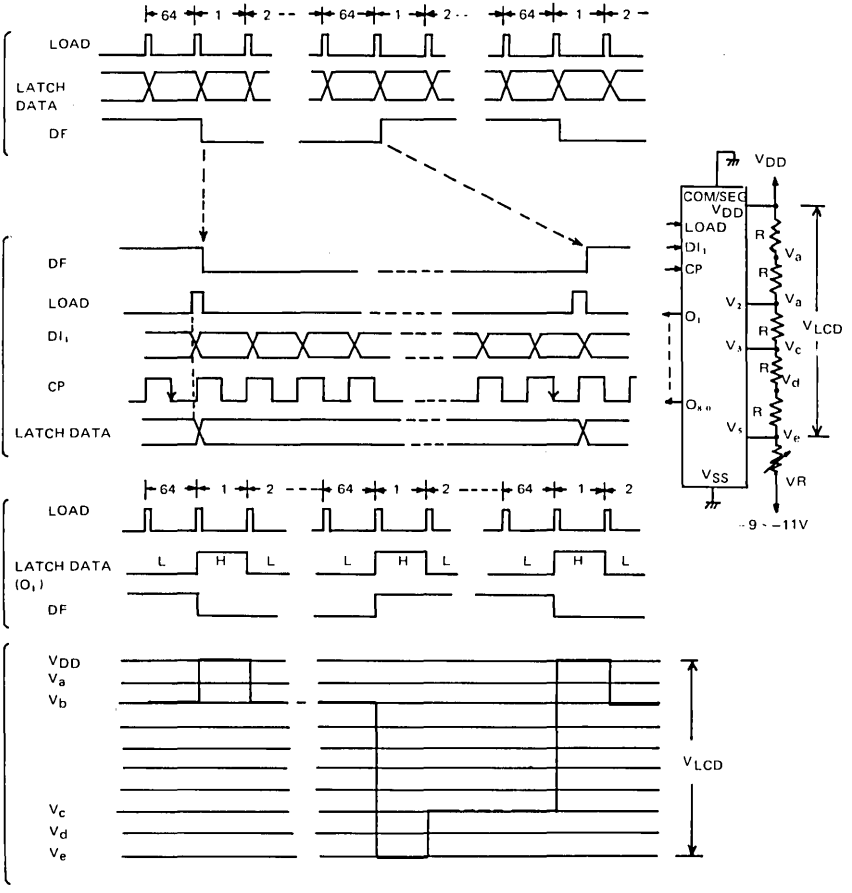
TIME CHART (COMMON DRIVER)

1/64 duty, 1/9 bias



TIME CHART (SEGMENT DRIVER)

1/64 duty, 1/9 bias



$V_a = V_{DD} - 1/9V_{LCD}$

$V_b = V_{DD} - 2/9V_{LCD}$

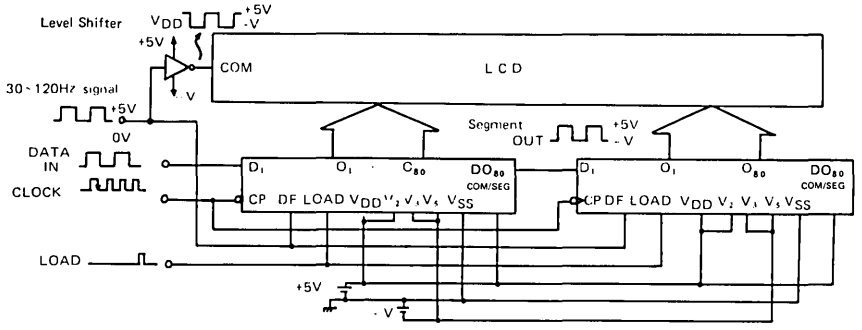
$V_c = V_{DD} - 7/9V_{LCD}$

$V_d = V_{DD} - 8/9V_{LCD}$

$V_e = V_{DD} - V_{LCD}$

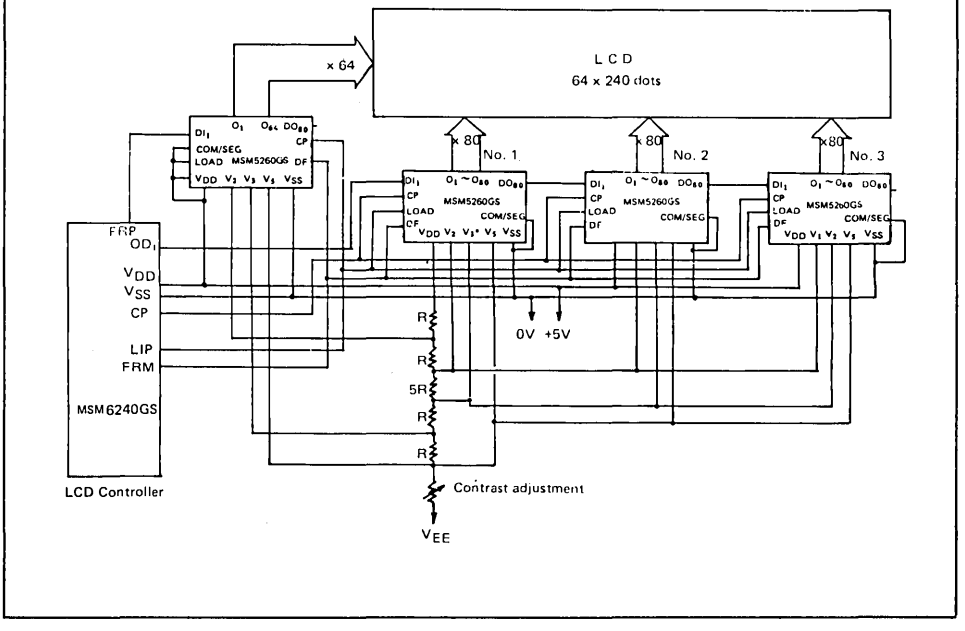
APPLICATION CIRCUIT

- STATIC display



The MSM5260GS can make a static drive of a LCD by controlling the supply voltage. So it can be used to drive a color LCD which requires high driving voltage. The value $V_{DD} \sim V_5$ must be $18V > V_{DD} \sim V_5 \geqq 5V$.

- 1/64 duty, 1/9 bias



MSM5278GS

DOT MATRIX LCD 64 DOT COMMON DRIVER

GENERAL

The OKI MSM5278GS is a dot matrix LCD's common driver LSI which is fabricated by low power CMOS metal gate technology. This LSI consists of 64-bit bidirectional shift register, 64-bit level shifter and 64-bit 4-level driver.

This LSI has 64 output pins to be connected to the LCD. By connecting more than two MSM5278GSs in series, this LSI is applicable to a wide LCD panel.

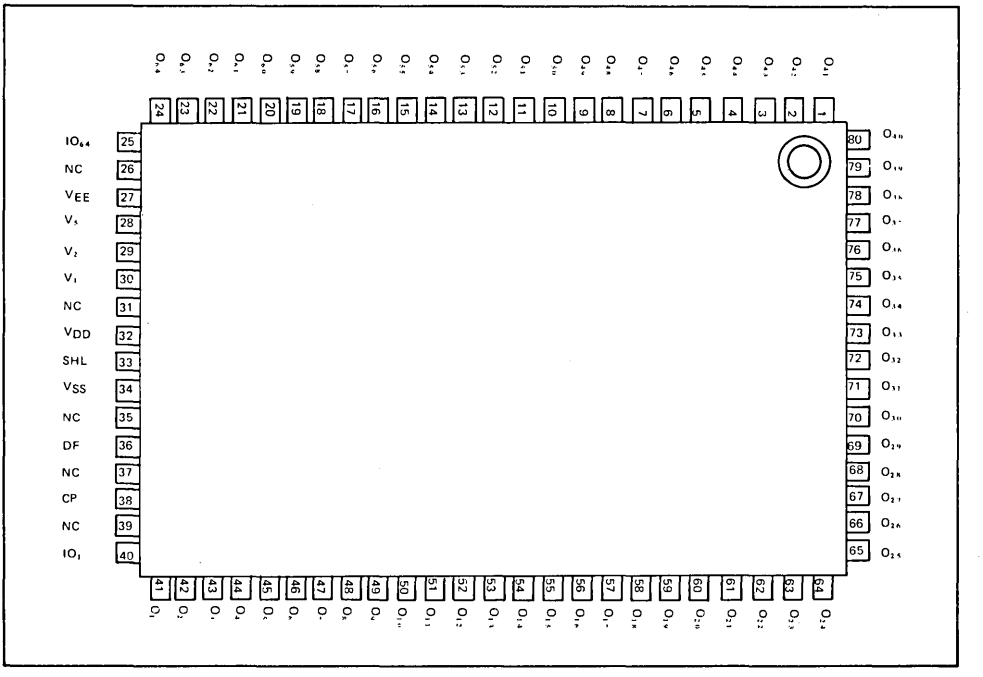
This LSI can drive a variety of LCD because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from the external source.

FEATURES

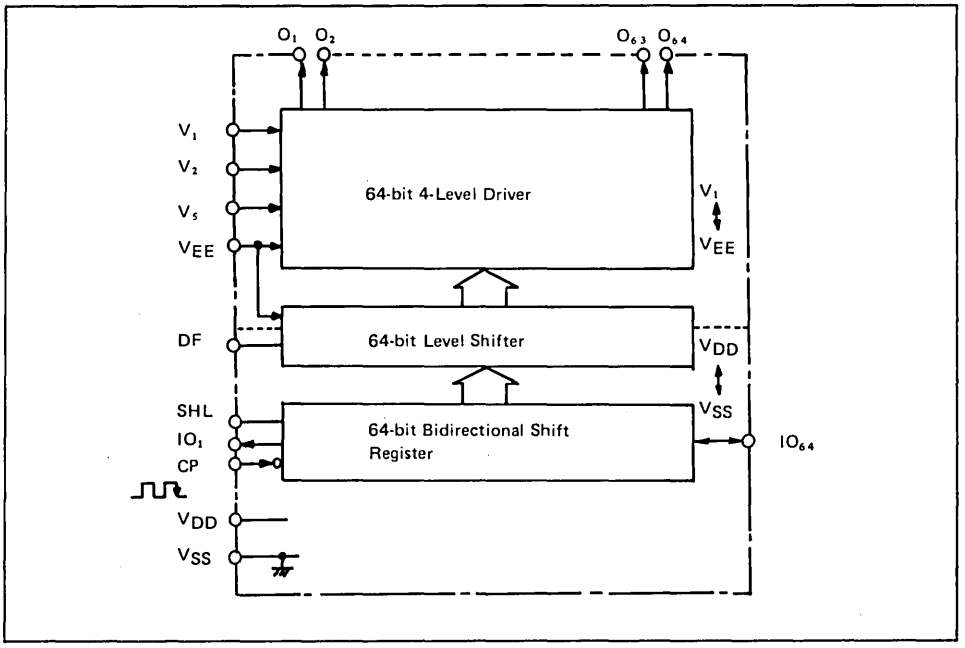
- Supply voltage: 4.5 ~ 5.5V
- LCD driving voltage: 8 ~ 20V
- Applicable LCD duty: 1/64 ~ 1/128
  Two chips of the MSM5278GS are required to drive 1/128 duty LCD.
- Bias voltage can be supplied externally
- 80 pin plastic flat package

PIN CONFIGURATION

(Top View) 80 Lead Plastic Flat Package



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Supply voltage (1)	V_{DD}	T_a = 25°C	−0.3 ~ 6	V
Supply voltage (2)	$V_{DD} - V_{EE}$*1	T_a = 25°C	0 ~ 22	V
Input voltage	V_I	T_a = 25°C	−0.3 ~ V_{DD} + 0.3	V
Storage temperature	T_{stg}	—	−55 ~ + 150	°C

*1 $V_1 > V_2 > V_5 > V_{EE}$, $V_1 \leqq V_{DD}$

OPERATING RANGE

Parameter	Symbol	Condition	Limits	Unit
Supply voltage (1)	V_{DD}	—	4.5 ~ 5.5	V
Supply voltage (2)	$V_{DD} - V_{EE}$*1	—	8 ~ 20	V
Operating temperature	T_{op}	—	−20 ~ + 85	°C

*1 $V_1 > V_2 > V_5 > V_{EE}$, $V_1 \leqq V_{DD}$

3

D.C. CHARACTERISTICS

(V_{DD} = 5V ± 10%, T_a = −20 ~ +85°C)

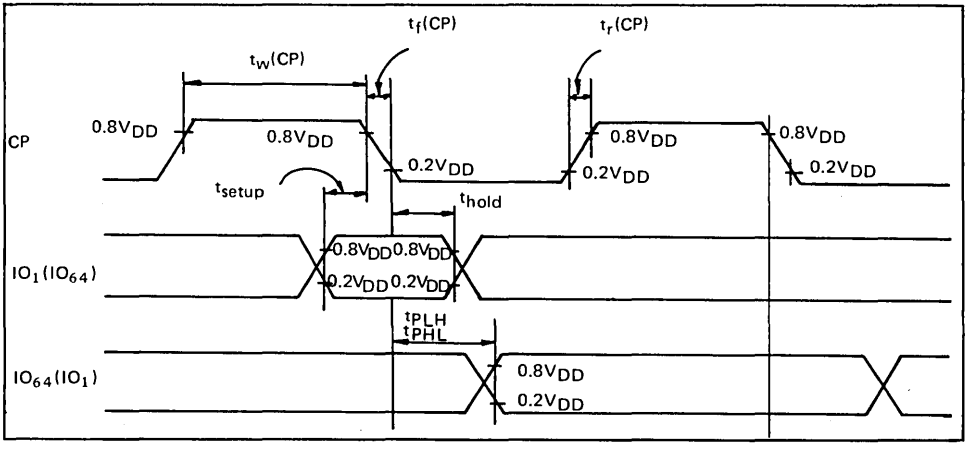
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H" Input voltage	V_{IH}*1	—	0.8V_{DD}	–	–	V
"L" Input voltage	V_{IL}*1	—	–	–	0.2V_{DD}	V
"H" Input current	I_{IH}*1	$V_{IH} = V_{DD}$	–	–	1	μA
"L" Input current	I_{IL}*1	V_{IL} = OV	–	–	−1	μA
"H" Output voltage	V_{OH}*2	I_O = −0.4mA	V_{DD}−0.4	–	–	V
"L" Output voltage	V_{OL}*2	I_O = 0.4mA	–	–	0.4	V
ON Resistance	R_{ON}*4	$V_{DD} - V_{EE}$ = 1.8V *3 $\lvert V_N - V_O \rvert$ = 0.25V	–	1	2	kΩ
Power consumption	I_{DD}	CP = DC $V_{DD}-V_{EE}$ = 18V No load	–	–	100	μA
Input capacitance	C_I	f = 1MHz	–	5	–	PF

*1 Application to CP, IO_1, IO_{64} SHL and DF terminals.
*2 Applicable to IO_1, and IO_{64} terminals.
*3 $V_N = V_{DD} \sim V_{EE}$, $V_2 = \frac{10}{11}(V_{DD} - V_{EE})$, $V_5 = \frac{1}{11}(V_{DD} - V_{EE})$, $V_{DD} = V_1$
*4 Applicable to $O_1 \sim O_{64}$ terminals.

SWITCHING CHARACTERISTICS

(V_{DD} = 5V ± 10%, T_a = −20 ~ +85°C CL = 15pF)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H" "L" propagation delay time	t_{PLH} t_{PHL}	—	–	–	250	ns
Max. clock frequency	f_{CP}	—	1	–	–	MHz
Clock pulse width	$t_{W(CP)}$	—	125	–	–	ns
Data set-up time $IO_1(IO_{64})$→CP	t_{setup}	—	100	–	–	ns
Data hold time $IO_1(IO_{64})$→CP	t_{hold}	—	100	–	–	ns
Clock pulse Rising/Falling time	$t_{r(CP)}$ $t_{f(CP)}$	—	–	–	50	ns



PIN DESCRIPTION

- **IO_1, IO_{64}, SHL**
  IO_1 and IO_{64} are 64-bit bidirectional shift register input/output pins. The shifting direction is selected by the H/L condition of SHL pin. Refer to the table below.

SEL	Shifting direction	IO_1/IO_{64}	Input/output	Pin description
L	$O_1 \rightarrow O_{64}$	IO_1	Input	The scanning data from the LCD controller LSI is input from IO_1 synchronized with the clock pulse. *1
		IO_{64}	Output	Shift register contents output pin. The data which was input from IO_1 is output from IO_{64} with 64 bits' delay, synchronized with the clock pulse. Refer to the application circuit.
H	$O_{64} \rightarrow O_1$	IO_{64}	Input	The scanning data from the LCD controller LSI is input from IO_{64} synchronized with the clock pulse. *1
		IO_1	Output	Shift register contents output pin. The data which was input from IO_{64} is output from IO_1 with 64 bits' delay, synchronized with the clock pulse. Refer to the application circuit.

*1 The combination of the scanning data, IO_1 or IO_{64}, and the LCD driving output, $O_1 \sim O_{64}$, is shown in the table below.

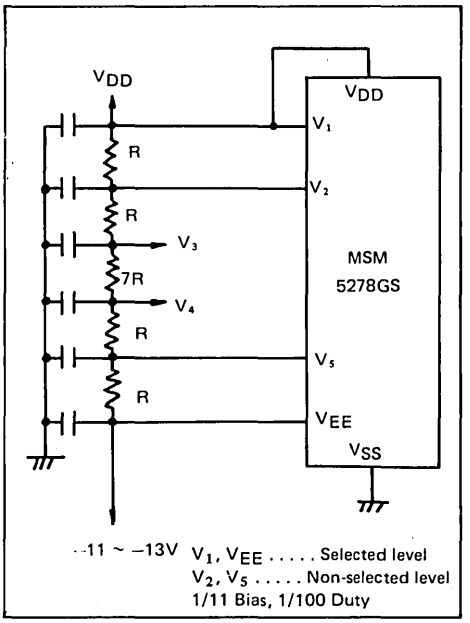
IO_1, IO_{64}	LCD driving output
H	Selected level (V_1, V_{EE})
L	Non-selected level (V_2, V_5)

- **CP**
  Clock pulse input pin for 64-bit bidirectional shift register. The data is shifted to 64-bit level shifter at the falling edge of the clock pulse.

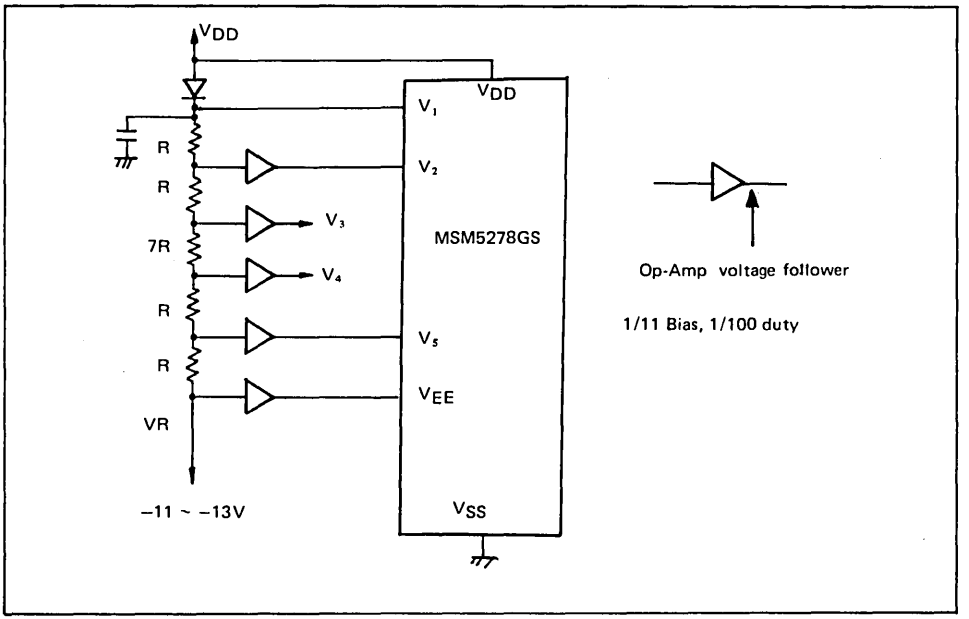
- **DF**
  Alternate signal input pin for LCD driving.
  Normal frame inversion signal is input.

- **V_{DD}, V_{SS}**
  Supply voltage pins. V_{DD} should be 4.5 ~ 5.5V. V_{SS} is a ground pin. (V_{SS} = 0V)

- **V_1, V_2, V_5, V_{EE}**
  Bias supply voltage pins to drive the LCD. Bias voltage divided by the resistance is usually used as supply voltage source.
  The below figure shows the case when bias voltage is divided by the resistance. V_1 is not necessarily connected to V_{DD}.



The figure below shows the case when bias voltage is supplied by the Op-Amps. By using Op-Amps, the bias voltage becomes low impedance and the power consumption of MSM5278 becomes low.



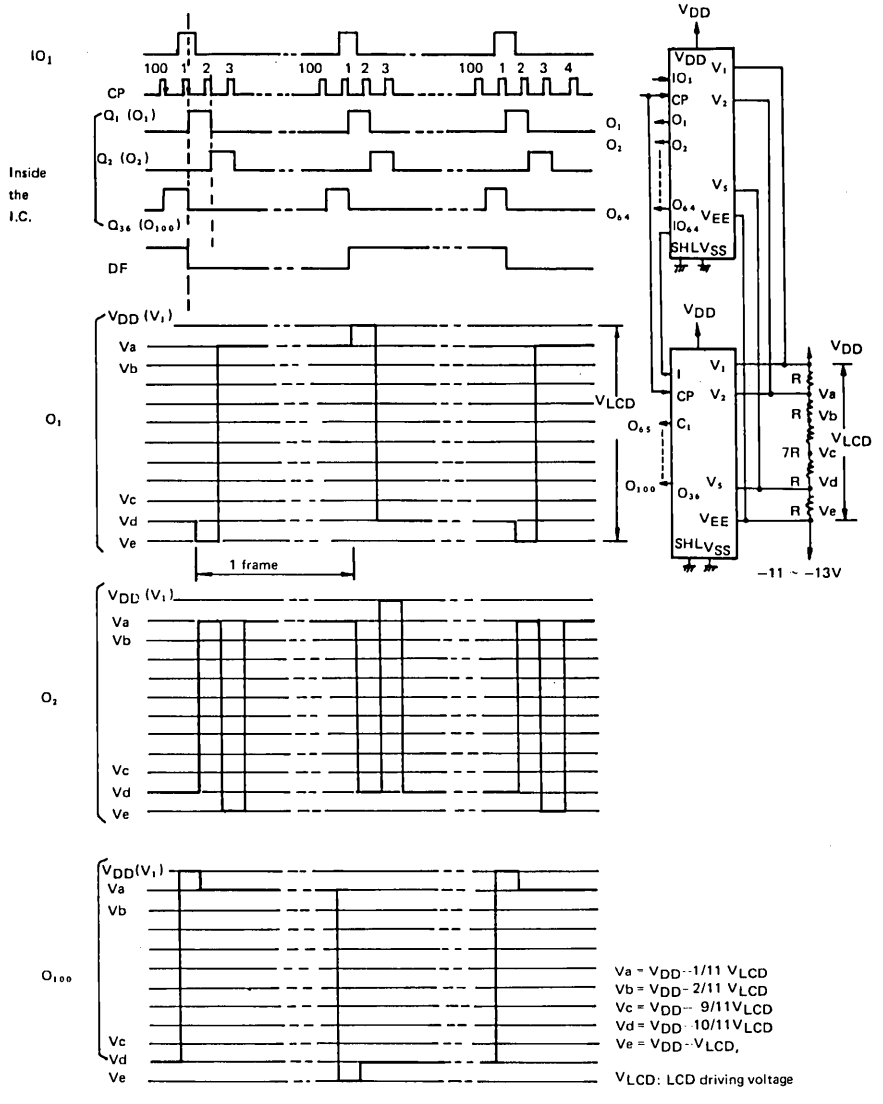
- **$O_1 \sim O_{64}$**
  Display data output pins which correspond to 64-bit shift register contents. One of V_1, V_2, V_5 and V_{EE} is selected as a display driving voltage source according to the combination of the latched data level and DF signal. (Refer to the truth table below.)

DF	Latched data level	Display data output level ($O_1 \sim O_{64}$)
L	L	V_2
L	H	V_{EE}
H	L	V_5
H	H	V_1

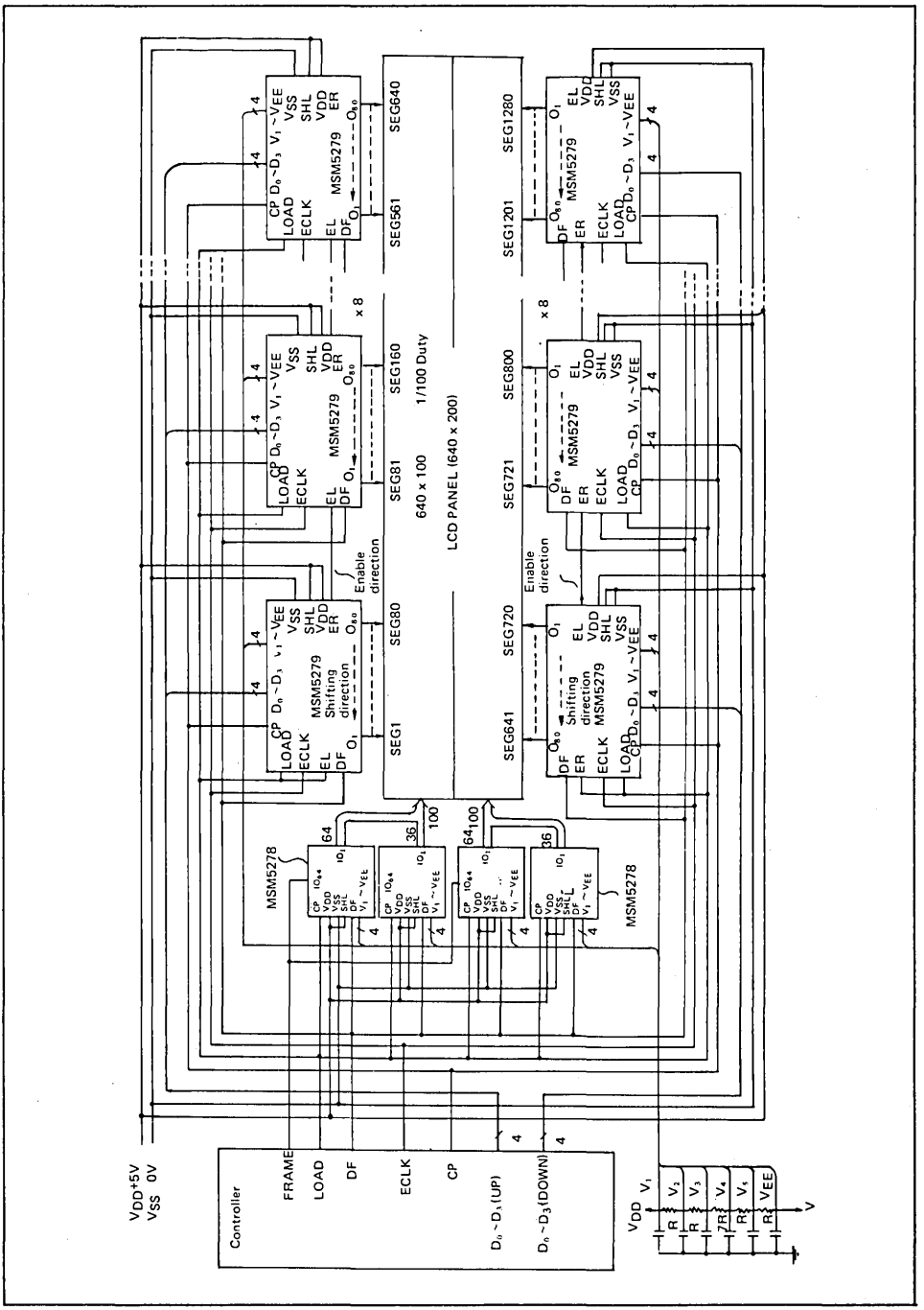
Truth table

TIMING CHART

1/100 duty, 1/11 bias



APPLICATION CIRCUIT



MSM5279GS

DOT MATRIX LCD 80 DOT SEGMENT DRIVER

GENERAL

The OKI MSM5279GS is a dot matrix LCD's segment driver LSI which is fabricated by CMOS low power metal gate technology. This LSI consists of 80-bit bidirectional shift register, 80-bit latch, 80-bit level shifter and 80-bit 4-level driver.

It receives the display driving data, which consists of 4-bit parallel, from the LCD controller LSI, then output the LCD driving waveform to the LCD'.

The MSM5279GS has the power down function which enables the MSM5279GS's power consumption low.

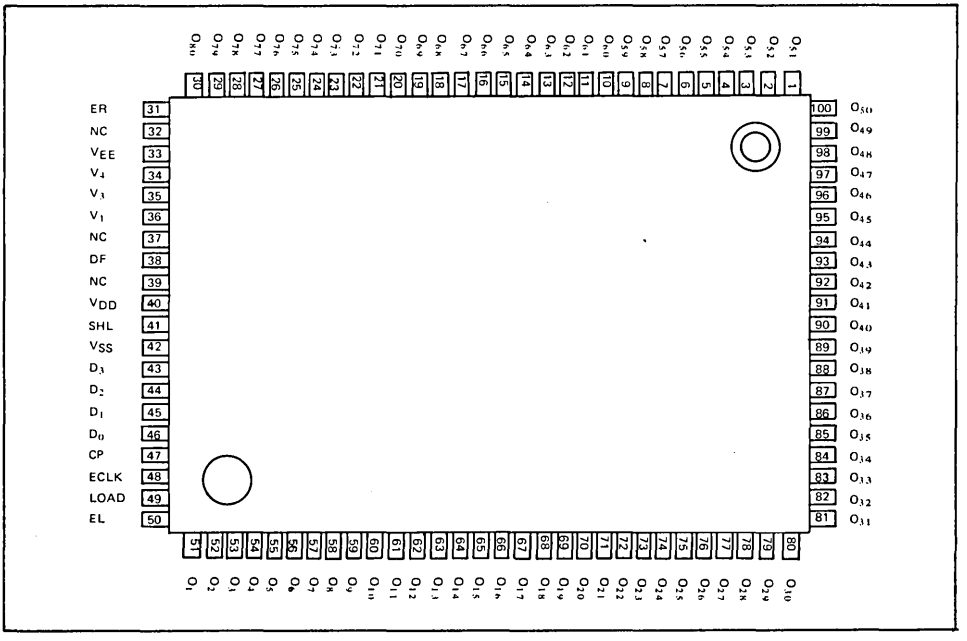
The MSM5279GS can drive a variety of LCD panel because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from the external source.

FEATURES

- Supply voltage: 4.5 ~ 5.5V
- LCD driving voltage: 8 ~ 20V
- Applicable LCD duty: 1/8 ~ 1/128
- Bias voltage can be supplied externally
- Power down function
- 4-bit parallel data processing
- Can be interfaced with the MSM6255GS, MSM6265GS, LCD controller LSI
- 100 pin plastic flat package

PIN CONFIGURATION

(Top View)



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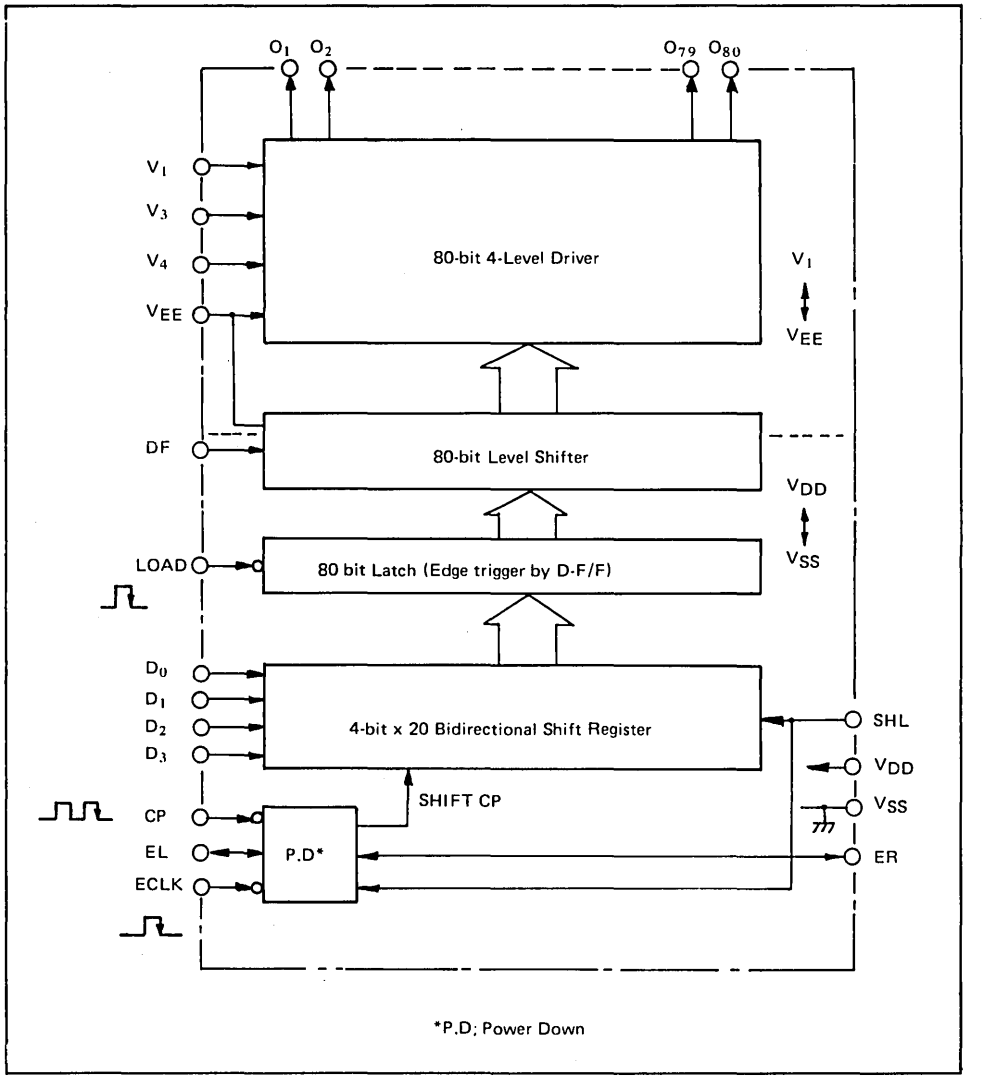
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Limits	Unit
Supply voltage (1)	V_{DD}	T_a = 25°C	−0.3 ~ 6	V
Supply voltage (2)	$V_{DD} - V_{EE}$*1	T_a = 25°C	0 ~ 22	V
Input voltage	V_I	T_a = 25°C	−0.3 ~ V_{DD} + 0.3	V
Storage temperature	T_{stg}	—	−55 ~ + 150	°C

*1 $V_1 > V_3 > V_4 > V_{EE}$, $V_1 \leqq V_{DD}$

OPERATING RANGE

Parameter	Symbol	Condition	Limits	Unit
Supply voltage (1)	V_{DD}	—	4.5 ~ 5.5	V
Supply voltage (2)	$V_{DD} - V_{EE}$*1	—	8 ~ 20	V
Operating temperature	Top	—	−20 ~ + 85	°C

*1 $V_1 > V_3 > V_4 > V_{EE}$, $V_1 \leqq V_{DD}$

3

DC CHARACTERISTICS

(V_{DD} = 5V ± 10%, Ta = −20 ~ +85°C)

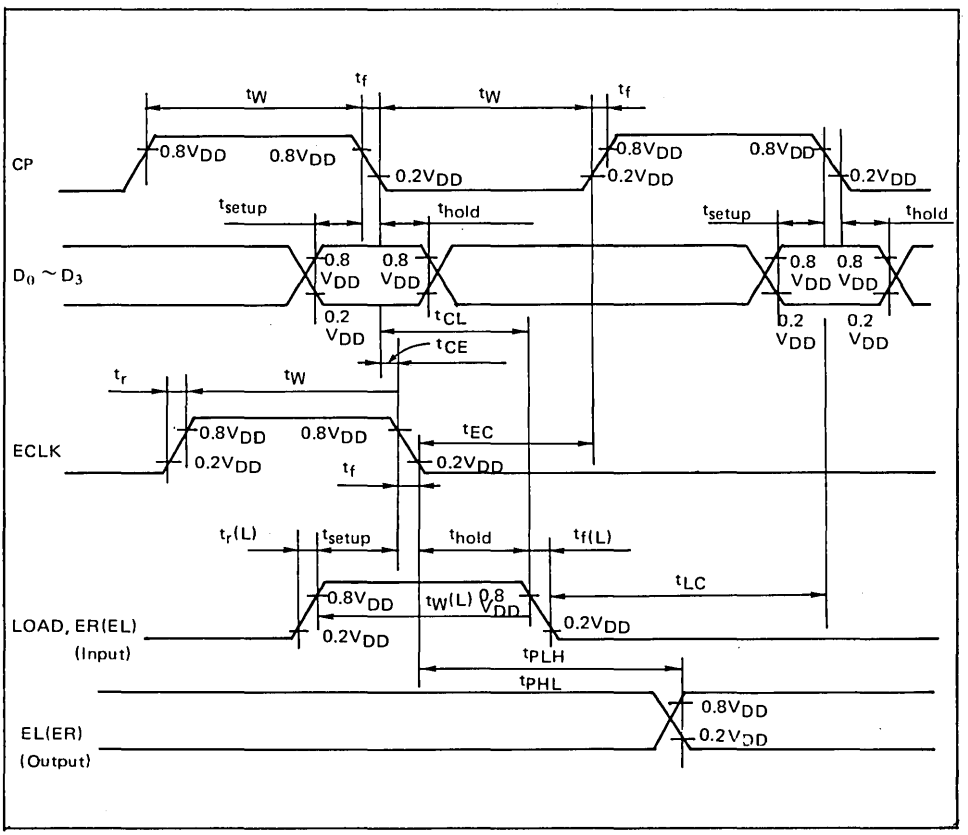
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H" Input voltage	V_{IH}*1	—	$0.8V_{DD}$	–	–	V
"L" Input voltage	V_{IL}*1	—	–	––	$0.2V_{DD}$	V
"H" Input current	I_{IH}*1	$V_{IH} = V_{DD}$	–	–	1	μA
"L" Input current	I_{IL}*1	V_{IL} = 0V	–	–	−1	μA
"H" Output voltage	V_{OH}*2	I_O = −0.2mA	V_{DD}− 0.4	–	–	V
"L" Output voltage	V_{OL}*2	I_O = 0.2mA	–	–	0.4	V
ON resistance	R_{ON}*4	$V_{DD} - V_{EE}$ = 18V $\lvert V_N - V_O \rvert$ = 0.25V	–	2	4	kΩ
Stand-by current consumption	$I_{DD}SBY$	CP = 1 MHz $V_{DD} - V_{EE}$ = 18V, No load*5	–	–	200	μA
Current consumption (1)	I_{DD1}	CP = 1 MHz $V_{DD} - V_{EE}$ = 18V, No load*6	–	–	4	mA
Current consumption (2)	I_V	CP = 1 MHz $V_{DD} - V_{EE}$ = 18V, No load*7	–	–	±100	μA
Input capacitance	C_I	f = 1 MHz	–	5	–	PF

*1 Applicable to LOAD, CP, $D_0 \sim D_3$, ECLK, EL, ER, SHL, DF terminals.
*2 Applicable to EL, ER terminals.
*3 VN = $V_{DD} \sim V_{EE}$ $V_3 = \frac{9}{11}(V_{DD} - V_{EE})$, $V_2 = \frac{9}{11}(V_{DD} - V_{EE})$, $V_{DD} = V_1$.
*4 Applicable to $O_1 \sim O_{80}$ terminals.
*5 Display data 1010 – DF = 40Hz, Current from V_{DD} to V_{SS} when the display data is not processing.
*6 Display data 1010 – DF = 40Hz, Current from V_{DD} to V_{SS} when the display data is processing.
*7 Display data 1010 – DF = 40Hz, Current on V_1, V_3, V_4 and V_{EE} terminals.

SWITCHING CHARACTERISTICS

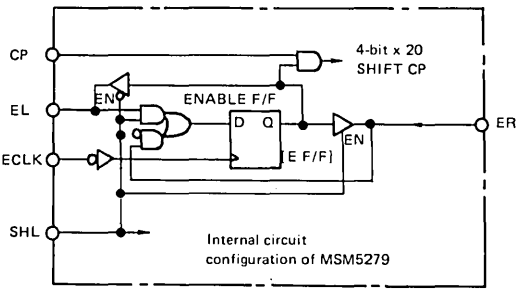
(V_{DD} = 5V ± 10%, T_a = −20 ~ +85°C CL = 15pF)

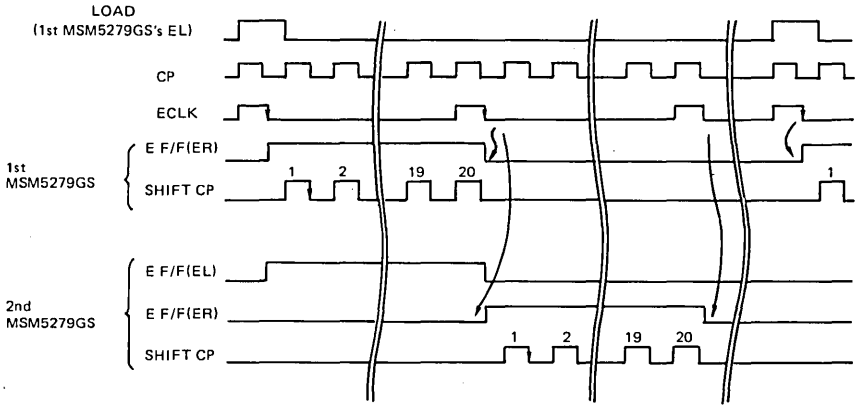
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
"H", "L" propagation delay time	t_{PLH}, t_{PHL}	—	–	–	250	ns
MAX. clock frequency	f_{CP}	DUTY = 50%	3	–	–	MHz
CP ELCK pulse width	t_W	—	125	–	–	ns
Load pulse width	$t_{W(L)}$	—	125	–	–	ns
Data set-up time	t_{setup}	—	100	–	–	ns
CP → LOAD time	t_{CL}	—	250	–	–	ns
LOAD → CP time	t_{LC}	—	0	–	–	ns
Data hold time CP → D_0 ~ D_3, ECLK → LOAD	t_{hold}	—	100	–	–	ns
Clock pulse Rising/Falling time	t_r t_f	—	–	–	50	ns
Load pulse Rising/Falling time	$t_{r(L)}$ $t_{f(L)}$	—	–	–	1	μs
CP → ECLK time	t_{CE}	—	0	–	–	ns
ECLK → CP time	t_{EC}	—	150	–	–	ns



POWER DOWN FUNCTION

When more than two MSM5279GSs are being connected in series, cascade connection, power down function of MSM5279GS can be utilized using the ENABLE F/F (flip flop circuit) in individual MSM5279GSs. (Regarding the internal circuit configuration of MSM5279GS, refer to the figure below.) The display data is processed only in the MSM5279GS, the ENABLE F/F of which is being activated by setting its ER and EL at high level, while the display data is not processed in the MSM5279GS, the ENABLE F/F of which is not being activated and the low power consumption condition (I_{DD} SBY) is being held. The activated condition of this ENABLE F/F is being shifted to next MSM5279GS one after another so that the ENABLE F/F of only one MSM5279GS out of the cascade connected MSM5279GSs should be being activated.





SHL = "H" (EL = Input ER = Output)
First MSM5279GS's ER should be
connected to second MSM5279GS's EL

Timing chart when MSM5279GS's are connected in series (cascade connection)

PIN DESCRIPTION

- **ER, EL**

Pin	Input/Output	SHL	Description
ER	Input	L	Input pin to ENABLE F/F of MSM5279GS.
EL	Output		Output pin of ENABLE F/F. EL is connected to next MSM5279GS's ER when MSM5279GSs are connected in series (cascade connection).
EL	Input	H	Input pin to ENABLE F/F of MSM5279GS.
ER	Output		Output pin of ENABLE F/F. ER is connected to next MSM5279GS's EL when MSM5279GSs are connected in series (cascade connection).

- **ELCK**
  Clock pulse input pin for ENABLE F/F. The active condition of ENABLE F/F is shifted to next MSM5279GS's ENABLE F/F at the falling edge of the clock pulse. ELCK is required every 20 CP. (Clock Pulse).

- **CP**
  Clock pulse input pin for the 4-bit parallel shift register. The data is shifted to 80-bit latch at the falling edge of the clock pulse. The clock pulse, which was input when the ENABLE F/F is not active condition, is invalid.

- **SHL**
  ER and EL can be used as either input pin or output pin according to the H/L condition of SHL. The shifting direction of each data, $D_0 \sim D_3$, the Input/Output condition of ER and EL and the H/L condition of SHL are described in the table below.

SHL	ER	EL	Shifting direction
L	Input	Output	$D_0 \rightarrow O_1 \rightarrow O_5 \longrightarrow O_{77}$ $D_1 \rightarrow O_2 \rightarrow O_6 \longrightarrow O_{78}$ $D_2 \rightarrow O_3 \rightarrow O_7 \longrightarrow O_{79}$ $D_3 \rightarrow O_4 \rightarrow O_8 \longrightarrow O_{80}$
H	Output	Input	$D_0 \rightarrow O_{80} \rightarrow O_{76} \longrightarrow O_4$ $D_1 \rightarrow O_{79} \rightarrow O_{75} \longrightarrow O_3$ $D_2 \rightarrow O_{78} \rightarrow O_{74} \longrightarrow O_2$ $D_3 \rightarrow O_{77} \rightarrow O_{73} \longrightarrow O_1$ ↑ end data ↑ start data

- **D_0, D_1, D_2, D_3**
  Data input pins for 4-bit parallel shift register and it is input synchronized with the clock pulse. The combination of $D_0 \sim D_3$ level, DF signal, display data output level and the display on the LCD panel is described on the table below.

$D_0 \sim D_3$	DF	Display data output level	Display on the LCD
L	L	V_3	OFF
H	L	V_1	ON
L	H	V_4	OFF
H	H	V_{EE}	ON

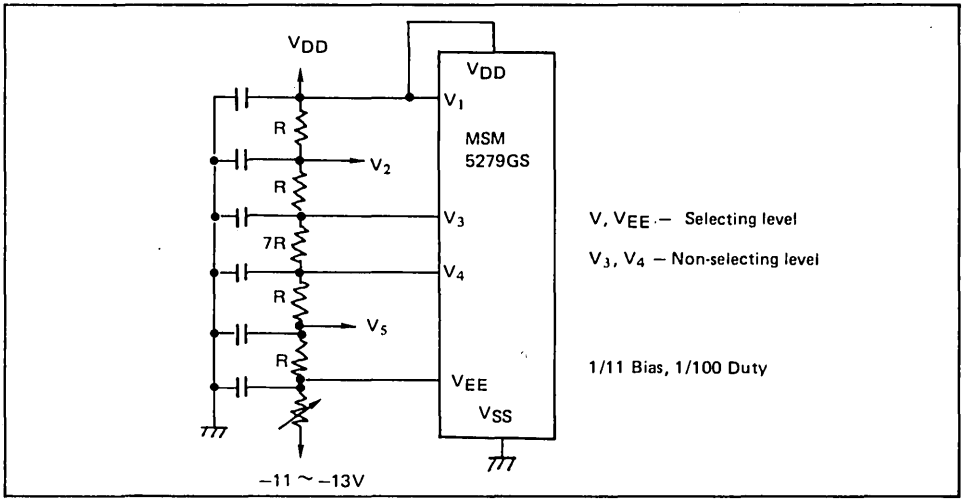
- **LOAD**
  The signal for latching the shift register contents is input from this pin. When LOAD pin is set at "H" level, the shift register contents are transferred to 80-bit latch at the falling edge of the LOAD pulse.

When more than two MSM5279GSs are connected in series, cascade connection, the first MSM5279GS's EL terminal (when SHL = "H") or ER terminal (when SHL = "L") should be connected with first MSM5279GS's LOAD terminal.

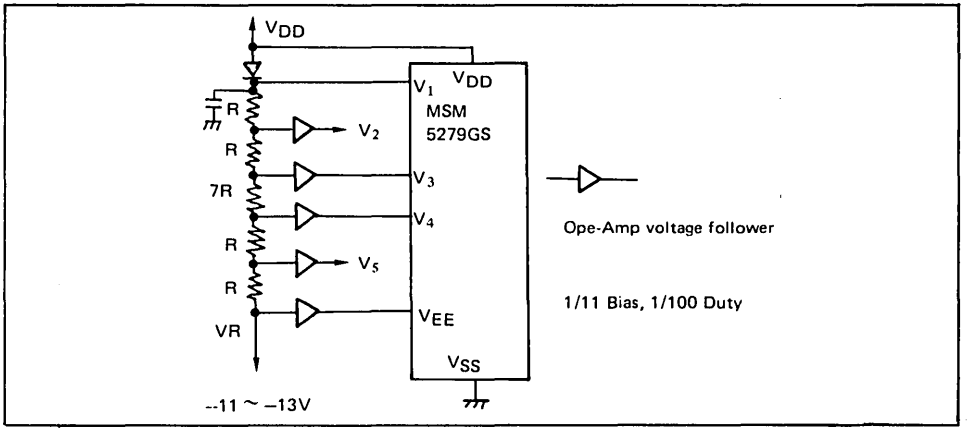
- **DF**
  Alternate signal input pin for LCD driving. Frame inversion signal is input to this terminal.

- **V_{DD}, V_{SS}**
  Supply voltage pins. V_{DD} should be 4.5 ~ 5.5V. V_{SS} is a ground pin (V_{SS} = OV)

- **V_1, V_3, V_4, V_{EE}**
  Bias supply voltage pin to drive the LCD. Bias voltage divided by the resistance is usually used as supply voltage source. The figure below shows the case when bias voltage, which determines the LCD driving voltage, is supplied from the external source. V_1 is not necessarily connected with V_{DD}.



The figure below shows the case when the bias voltage is supplied by using Ope-Amps, which enables the bias source low impedance and low power consumption.



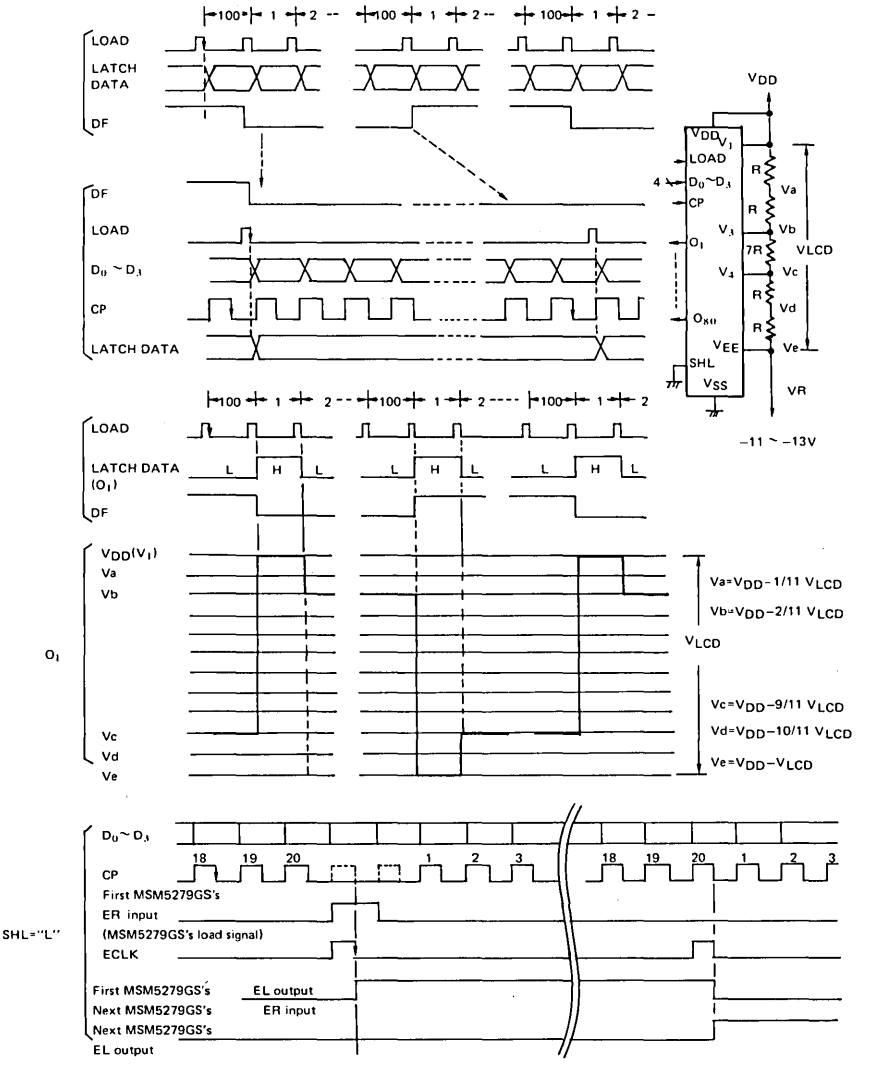
- **$O_1 \sim O_{80}$**
  Display data output pin which corresponds to the respective latch contents. One of V_1, V_3, V_4 and V_{EE} is selected as a display driving voltage source according to the combination of the latched data level and DF signal. (Refer to the truth table on the right).

DF	Latched data	Display data output level
L	L	V_3
L	H	V_1
H	L	V_4
H	H	V_{EE}

Truth table

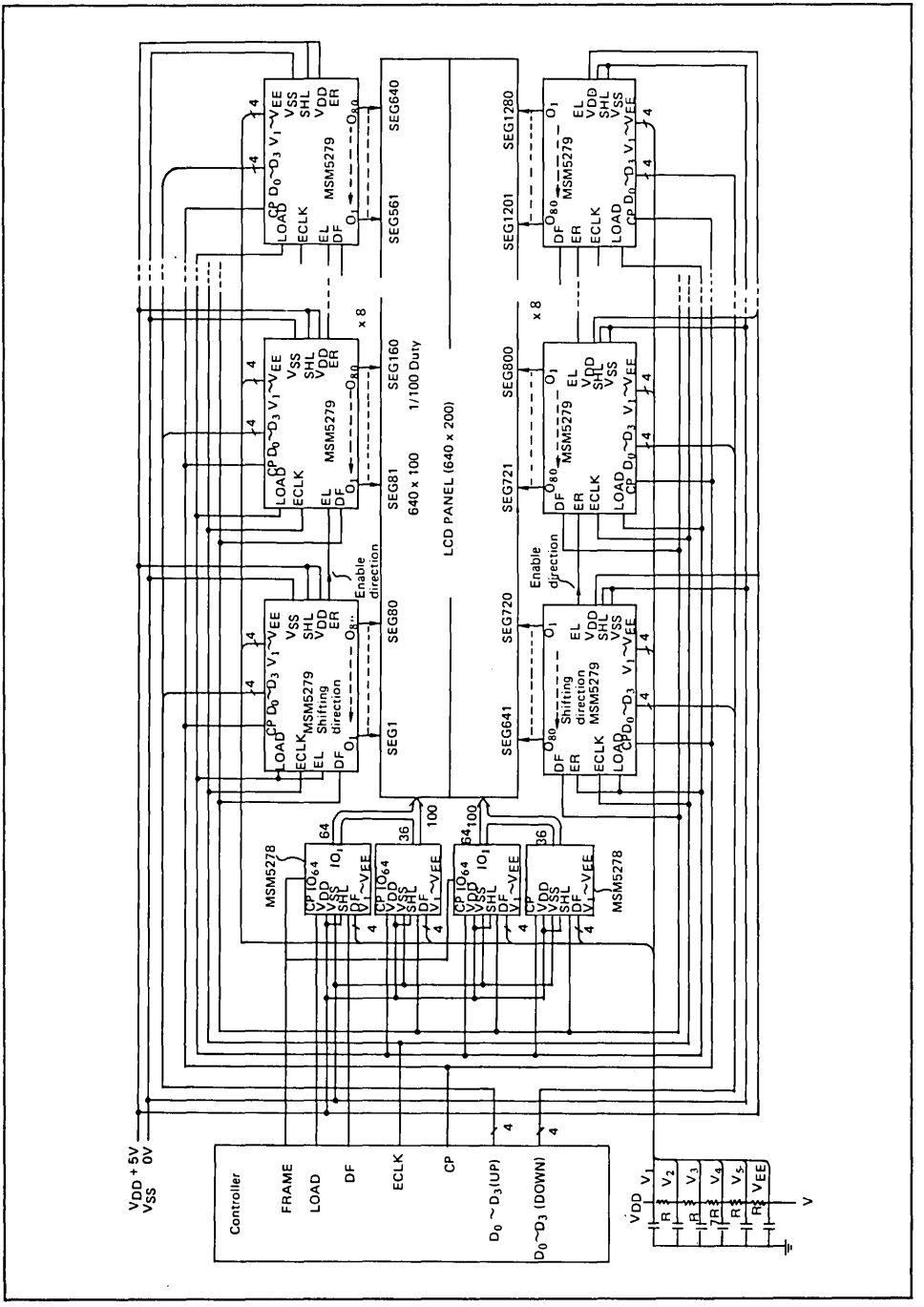
TIME CHART

1/100 duty, 1/11 Bias



Interface with MSM6255GS

APPLICATION CIRCUIT



3

DOT MATRIX LCD CONTROLLER

MSM6222B-01GS

DOT MATRIX LCD CONTROLLER WITH 16 DOT COMMON DRIVER AND 40 DOT SEGMENT DRIVER

GENERAL DESCRIPTION

The OKI MSM6222B-01GS is a dot matrix LCD controller which is fabricated by low power CMOS silicon gate technology. In combination with 4-bit/8-bit microcontroller, character display on the dot matrix character type LCD can be effected. This LSI consists of 16 dot COMMON driver, 40 dot SEGMENT driver, DISPLAY RAM, character generator RAM, character generator ROM and control circuit.
Max. 80 characters' display can be controlled by MSM6222B-01GS by using together with the MSM5259GS.

The OKI MSM6222B-01GS has the same performance as HD44780. There is, however, slight differences between these two devices as described in the table on page 101.

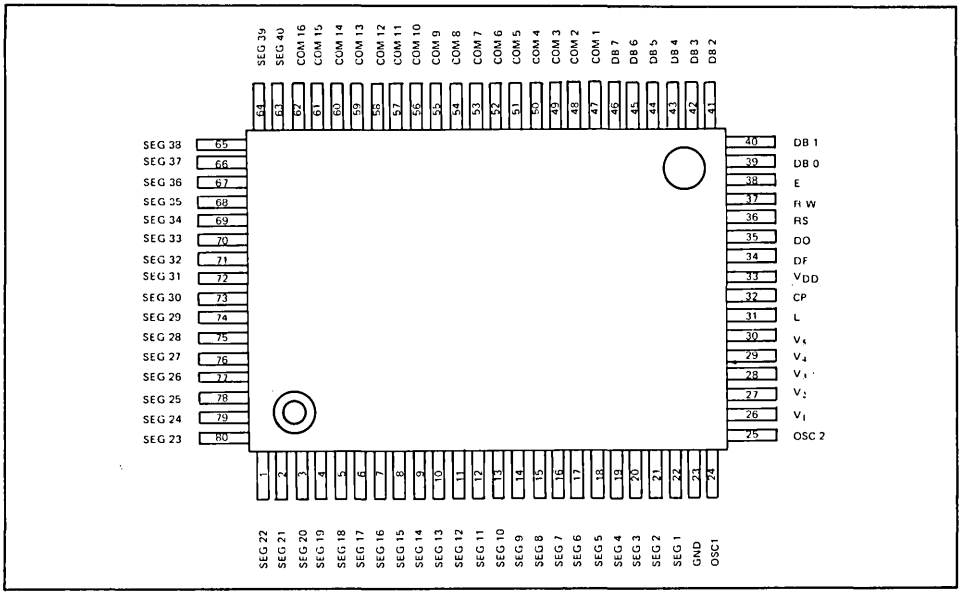
MSM6222B has ROM area for character code that can be programmed by custom mask. -01GS is the standard version with 160 characters, with small letter font 5 X 7, and 32 characters, with capital letter font 5 X 10, in this ROM area.

FEATURES

- Easy interface with an 8-bit or 4-bit microcontroller.
- Dot matrix LCD controller/driver for small letter font (6 X 7 dots) or capital letter font (5 X 10 dots).
- Automatic power ON reset.
- COMMON signal drivers (16) and SEGMENT signal drivers (40).
- Control up to 80 characters when used in combination with MSM5259GS.
- Character generator ROM for 160 characters with small letter font (5 X 7 dots) and 32 characters with capital letter font (5 X 10 dots).
- Character patterns can be programmable by CG RAM. (Small letter font: 8 kinds, 5 X 8 dots, Capital letter font: 4 kinds, 5 X 11 dots).
- Oscillation circuit for external register or ceramic resonator.
- 1/8 duty (1 line; 5 X 7 dots + cursor), 1/11 duty (1 line; 5 X 10 dots + cursor), or 1/16 duty (2 lines; 5 X 7 dots + cursor), selectable.
- Clear display even in case of 1/5 bias, 3.0V LCD driving voltage.

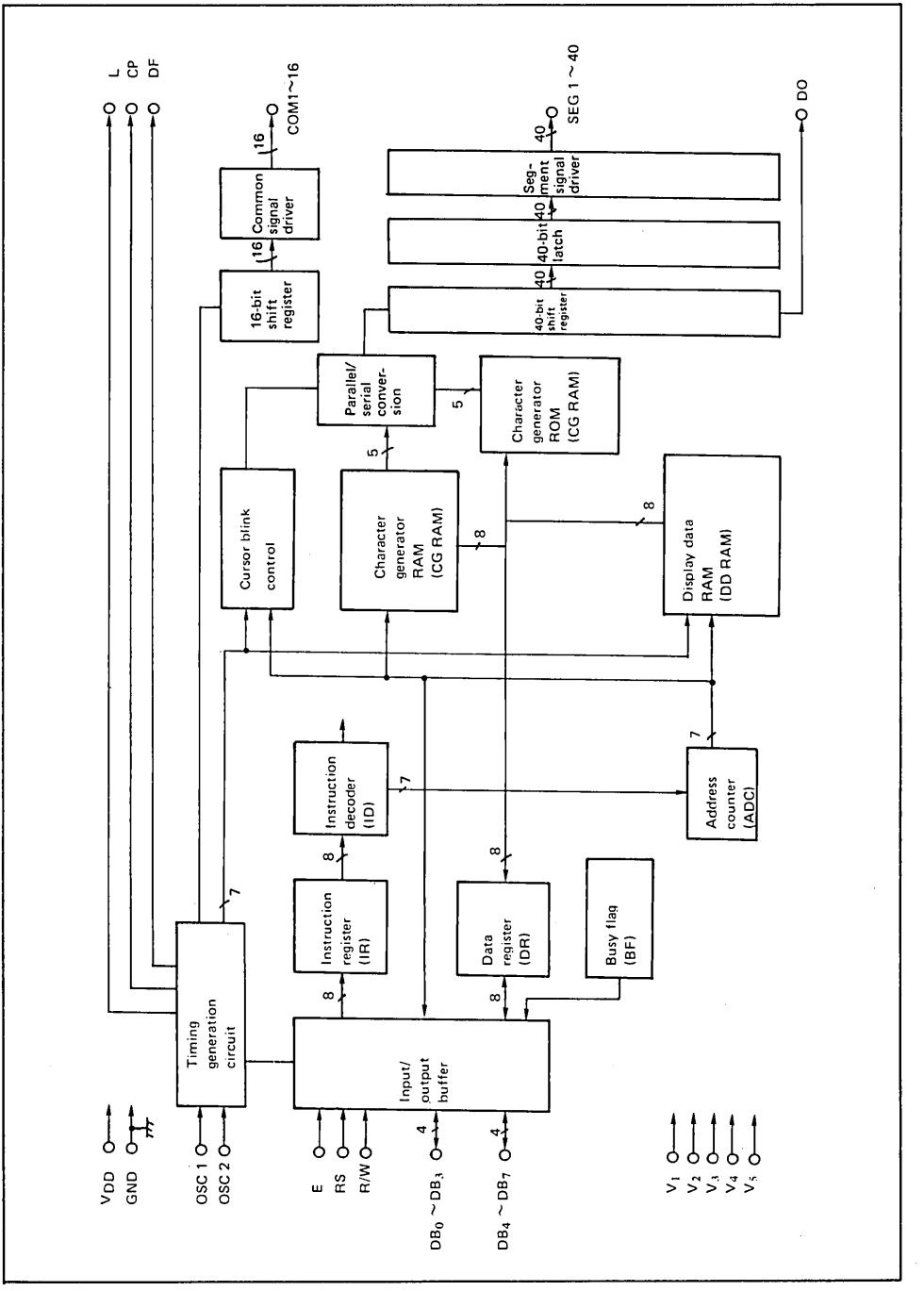
PIN CONFIGURATION

(Top View)



Item	HD44780	MSM6222B-01GS
LCD driving voltage 1/4 bias 1/5 bias	 3.0 ~ 11.0 (V) 4.6 ~ 11.0 (V)	 3.0 ~ 8.0 (V) 3.0 ~ 8.0 (V)
Bus interface speed with CPU	1 MHz (1000 ns)	1.5 MHz (667 ns) Signal rising/falling time is quite fast. So, the conduction between lines of the PCB and the cable assignment are very important.
The increment and decrement of the address counter in writing/reading the data to/from the CGRAM/DDRAM.	The address counter is incremented or decremented 6 μ sec (when f_{OSC} = 250 KHZ) after the busy condition is released. (Period of busy condition is 40 μs) So, the data cannot be written into/read out from the RAM for 6 μsec after the busy condition was over.	The address counter is incremented or decremented during the busy condition. So, data can be written into/read out from the RAM immediately after the busy condition was over.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Condition	Value	Unit	Applicable terminal
Supply voltage	V_{DD}	T_a = 25°C	−0.3 ~ + 7.0	V	V_{DD} − GND
Supply voltage for LCD displaying	V_1, V_2, V_3 V_4, V_5	T_a = 25°C	V_{DD} − 9.0 ~ V_{DD} + 0.3	V	V_1, V_2, V_3 V_4, V_5
Input voltage	V_{IN}	T_a = 25°C	−0.3 ~ V_{DD} + 0.3	V	R/W, RS, E, DB_0 ~ DB_7 OSC1
Permissible loss	P_D	—	500	mW	—
Storage temperature	T_{stg}	—	−55 ~ + 125	°C	—
Operating temperature	T_{opr}	—	−20 ~ +75	°C	—

OPERATING RANGE

Parameter	Symbol	Condition	Value	Unit	Applicable terminal
Supply voltage	V_{DD}	−	4.5 ~ 5.5	V	V_{DD}
LCD driving voltage	V_{DD}−V_5 (3) (V_{LCD})	1/4 bias (1)	3.0 ~ 8.0	V	V_{DD}, V_5
		1/5 bias (2)	3.0 ~ 8.0	V	
Operating temperature	T_{opr}	−	−20 ~ +75	°C	−

(1) This voltage should be applied to $V_{DD} - V_5$.
Voltage applicable to V_1, V_2, V_3 and V_4 are as follows.

(2) $V_1 = V_{DD} - 1/4\ (V_{DD} - V_5)$
$V_2 = V_3 = V_{DD} - 1/2\ (V_{DD} - V_5)$
$V_4 = V_{DD} - 3/4\ (V_{DD} - V_5)$

(3) $V_1 = V_{DD} - 1/5\ (V_{DD} - V_5)$
$V_2 = V_{DD} - 2/5\ (V_{DD} - V_5)$
$V_3 = V_{DD} - 3/5\ (V_{DD} - V_5)$
$V_4 = V_{DD} - 4/5\ (V_{DD} - V_5)$

DC CHARACTERISTICS

(V_{DD} = 4.5 ~ 5.5V, T_a = −20 ~ +75°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Applicable terminal
"H" input voltage	V_{IH1}	–	2.2	–	V_{DD}	V	R/W, RS, E, DB_0 ~ DB_7
"L" input voltage	V_{IL1}	–	−0.3	–	0.6	V	
"H" input voltage	V_{IH2}	–	V_{DD} − 1.0	–	V_{DD}	V	OSC1
"L" input voltage	V_{IL2}	–	−0.3	–	1.0	V	
"H" output voltage	V_{OH1}	I_O = −0.205mA	2.4	–		V	DB_0 ~ DB_7
"L" output voltage	V_{OL1}	I_O = 0.4mA	–	–	0.4	V	
"H" output voltage	V_{OH2}	I_O = −40μA	0.9V_{DD}	–		V	DO, CP, L, DC, OSC2
"L" output voltage	V_{OL2}	I_O = 40μA	–	–	0.1V_{DD}	V	
COM voltage drop	V_C	I_O = ± 50μA Note 1	–	–	2.9	V	COM_1 ~ COM_{16}
SEG voltage drop	V_S	I_O = ± 50μA Note 1	–	–	3.8	V	SEG_1 ~ SEG_{40}
Input leak current	I_{IL}	V_{IN} = 0V	–	–	−1	μA	E
		V_{IN} = V_{DD}	–	–	1	μA	
"L" input current	I_{IL}	V_{DD} = 5.0V V_{IN} = 0V	−50	−125	−250	μA	R/W, RS
			−30	−92.5	−185	μA	DB_0 ~ DB_7
"H" input current	I_{IH}	V_{IN} = V_{DD}	–	–	2	μA	

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Applicable terminal
Current consumption (1)	I_{DD_1}	V_{DD} = 5.0V E = L level registor oscillator = 270KHz R/W, RS, and DB_0 to DB_7 are open. Output terminals are all no load. See Note 2.	–	0.35	0.6	mA	V_{DD}
Current consumption (2)	I_{DD2}	V_{DD} = 5V, ceramic oscillator. f_{OSC} = 250 KHz. E is in "L" level. R/W, RS, and DB_0 to DB_7 are open. Output terminals are all no load. See Note 2.	–	0.55	0.8	mA	V_{DD}
R_f clock oscillation frequency	f_{OSC}	R_f = 91 KΩ ± 2% Note 3	200	300	380	KHz	OSC1 OSC2
Clock input frequency	f_{IN}	OSC 2 is open. Input from OSC1	150	250	380	KHz	OSC1
Input clock duty	f_{Duty}	Note 4	45	50	55	%	OSC1
Input clock rise time	t_{fr}	Note 5	–	–	0.2	μS	OSC1
Input clock fall time	t_{ff}	Note 5	–	–	0.2	μS	OSC1
Ceramic filter oscillation frequency	f_{OSC}	Rf = 1 MΩ, $C_1 = C_2$ = 680 PF, Rd = 3.3 KΩ, and ceramic filter CS8250A. See Note 6.	245	250	255	KHz	OSC1 OSC2
LCD driving bias input voltage	V_{LCD}	Refer to the interface between LCD and MSM5839GS.	4.0		8.0	V	$V_{DD} - V_5$ potential

(Note 1) Applied to the voltage drop (V_C) occuring from terminals V_{DD}, V_1, V_4, and V_5 to each COMMON terminal (COM1 to COM16) when 50 μA is flown in or out to and from all COM and SEG terminals, and also to voltage drop (V_S) occurring from terminals V_{DD}, V_2, V_3, and V_5 to each SEG terminal (SEG1 to SEG40).

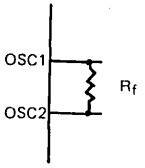
When output level is at V_{DD}, V_1, or V_2 level, 50 μA is flown out, while 50 μA is flown in when the output level is at V_3, V_4 or V_5 level.

This occurs when 5V or −5V is input to V_{DD}, V_1, and V_3 or to V_2, V_4, and V_5, respectively.

(Note 2) Applied to the current value flown in terminal V_{DD} when power is input as follows:

V_{DD} = 5V, GND = 0V, V_1 = 3.4V, V_2 = 1.8V, V_3 = 0.2V, V_4 = −1.4V, and V_2 = −3V.

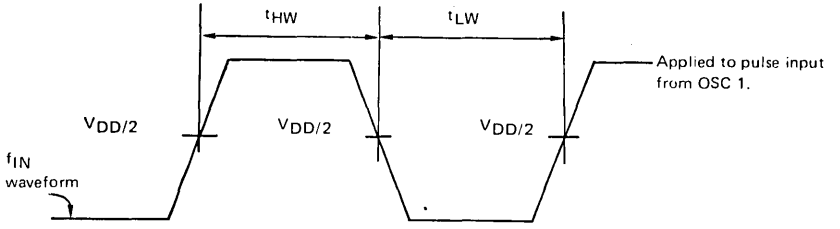
(Note 3)



R_f = 91 KΩ ± 2%

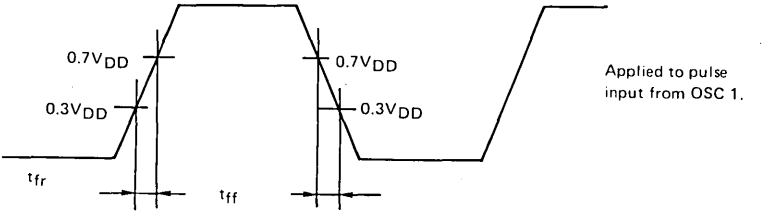
Minimum wiring is recommended between OSC 1 and R_f and between OSC 2 and R_f.

(Note 4)

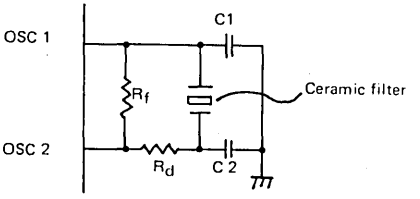


$f_{Duty} = t_{HW}/(t_{HW} + t_{LW}) \times 100$ (%)

(Note 5)



(Note 6)



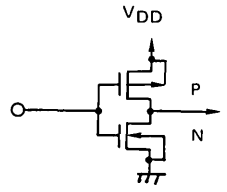
Ceramic filter : CSB250D (MURATA SEISAKUSHO Works)
Rf : 1MΩ ± 10%
C1 = C2 : 680pF ± 10%
Rd : 3.3KΩ ± 5%

(Note) Input the voltage listed in the table below to $V_1 - V_5$:

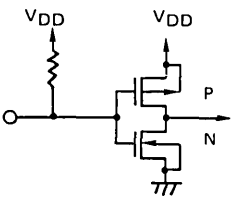
Terminal \ N (LCD line number)	1-line mode	2-line mode
V_1	$V_{DD} - \frac{VLCD}{4}$	$V_{DD} - \frac{VLCD}{5}$
V_2	$V_{DD} - \frac{VLCD}{2}$	$V_{DD} - \frac{2VLCD}{5}$
V_3	$V_{DD} - \frac{VLCD}{2}$	$V_{DD} - \frac{3VLCD}{5}$
V_4	$V_{DD} - \frac{3VLCD}{4}$	$V_{DD} - \frac{4VLCD}{5}$
V_5	$V_{DD} - V_{LCD}$	$V_{DD} - V_{LCD}$

V_{LCD} is the LCD driving voltage. (For "N (LCD line number), refer to the initial set of the instruction code.)

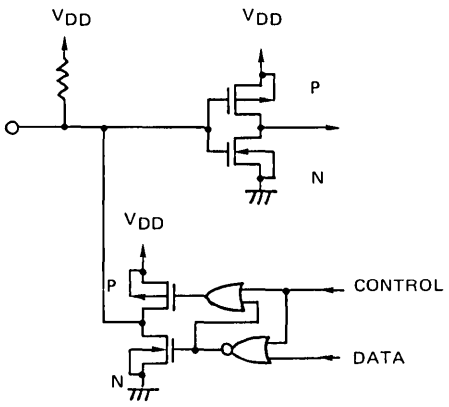
INPUT/OUTPUT CIRCUIT



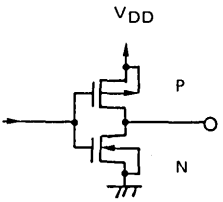
Applied to terminal E.



Applied to terminals R/W and RS.



Applied to $DB_0 - DB_7$.



Applied to DO, CP, L, and DF.

PIN DESCRIPTION

Terminal Name	Function
R/W	Read/write selection input terminal. "H": Read, and "L": Write
RS	Register selection input terminal. "H": Data register, and "L": Instruction register
E	Input terminal for data input/output between CPU and MSM6222B-01GS and for instruction register activation.
$DB_0 \sim DB_7$	Input/output terminal for data send/receive between CPU and MSM6222B-01GS
OSC1, OSC2	Clock oscillating terminal required for internal operation upon receipt of the LCD drive signal and CPU instruction.
$COM_1 \sim COM_{16}$	LCD COMMON signal output terminal.
$SEG1 \sim SEG_{40}$	LCD SEGMENT signal output terminal.
DO	Output terminal to be connected to MSM5259GS to expend the number of characters to be displayed.
CP	Clock output terminal used when DO terminal data output shifts the inside of MSM5259GS.
L	Clock output terminal for the serially transfered data to be latched to MSM5259GS.
DF	The alternating signal (DF, display frequency) output pin.
V_{DD}	Power supply pin.
GND	Ground pin.
$V_1 \sim V_5$	Bias voltage input pin to drive the LCD.

FUNCTIONAL DESCRIPTION

1. Instruction Register (IR) and Data Register (DR)

These two registers are selected by the register selector (RS) terminal.
The DR is selected when the "H" level is input and IR when the "L" level is input.
The IR is used to store the address code and instruction code of the display data RAM (DD RAM) or character generator RM (CG RAM).
The IR can be written into, but not be read out by the microcontroller (or CPU).
The DR is used to write into/read out the data to/from the DD RAM or CGRAM.
The data written to DR by the CPU is automatically written to the DD RAM or CG RAM as an internal operation.

When an address code is written to IR, the data (of the specified address) is automatically transferred from the DD RAM or CG RAM to the DR. By having the CPU subsequently read the DR (from the DR data), it is possible to verify DD RAM or CG RAM data.
After the writing of DR by the CPU, the DD RAM or CG RAM of the next address is selected to be ready for the next CPU writing.
Likewise, after the reading out of DR by the CPU, DD RAM or CG RAM data is read out by the DR to be ready for the next CPU reading.
Write/read to and from both registers is carried out by the READ/WRITE (R/W) terminal.

Table 1 Register and R/W terminals function table

R/W	RS	Function
L	L	IR write
H	L	Read of busy flag (BF) and address counter (ADC)
L	H	DR write
H	H	DR read

2. Busy Flag (BF)

When the busy flgag output is at "H", it indicates that the MSM6222B-01GS is engaged in internal operation.
When the busy flag is at "H" level, any new instruction is ignored.
When R/W = "H" and RS = "L", the busy flag is output from DB7.
New instruction should be input when BF is "L" level.
When the busy flag is set to "H", the output code of the address counter (ADC) cannot be fixed.

3. Address Counter (ADC)

The address counter (ADC) allocates the address for the DD RAM and CG RAM write/read and also for the cursor display.
When the instruction code for a DD RAM address or CG RAM address setting is input to IR, after deciding whether it is DD RAM or CG RAM, the address code is transferred from IR to ADC. After writing (reading) the display data to (from) the DD RAM or CG RAM, the ADC increments (decrements) by 1 as its internal operation.
The data of the ADC is output to DB0 – DB6 under the conditions that R/W = "H", RS = L, and BF = "L".

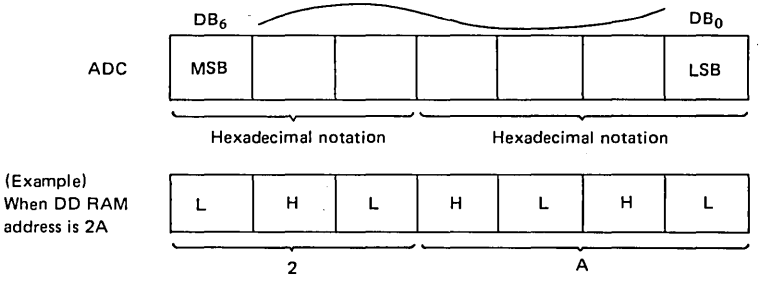
4. Timing Generator Circuit

This circuit is used to generate timing signals to activate internal operations upon receipt of CPU instruction and also from such internal circuits as the DD RAM, CG RAM, and CG ROM.
It is so designed that the internal operation caused by accessing from the CPU will not interfere with the internal operation caused by LCD display. Consequently, when data is written from the CPU to DD RAM no ill effect, e.g., flickering occurs in other than the display area where the data is written.
In addition, the circuit generates the transfer signal to MSM5259GS for display character expansion.

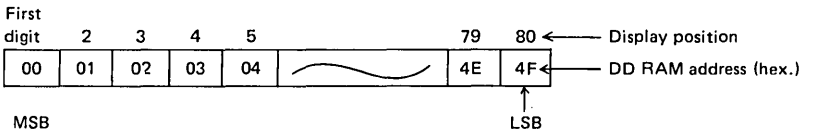
5. Display Data RAM (DD RAM)

This RAM is used to store display data of 8-bit character codes (see Table 2).
DD RAM address corresponds to the display position of the LCD. The coordination between the two is described in the following.

DD RAM address (set to ADC) is expressed in hexadecimal notation as shown below:



(1) Coordination between address and display position in the 1-line display mode



- When the MSM6222B-01GS is used alone, 8 characters max. can be displayed from the first digit to the eighth digit.

First digit	2	3	4	5	6	7	8
00	01	02	03	04	05	06	07

When the display is shifted by instruction, the coordination between the LCD display position and the DD RAM address changes as shown below:

(Display shifted to right)

First digit	2	3	4	5	6	7	8
4F	00	01	02	03	04	05	06

(Display shifted to left)

First digit	2	3	4	5	6	7	8
01	02	03	04	05	06	07	08

- When the MSM6222GS is used with one MSM5259GS, 16 characters max. can be displayed from the first digit to the sixteenth digit as shown below:

First digit	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F

MSM6222B-01GS display | MSM5259GS display

When the display is shifted by instruction, the coordination between the LCD display and DD RAM address changes as shown below:

	First digit	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
(Display shifted to right)	4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
(Display shifted to left)	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10

MSM6222B-01GS display | MSM5259GS display

- Since the MSM6222B-01GS has a DD RAM capacity for 80 characters, max. 9 pieces of MSM5259GS can be connected to MSM6222B-01GS so that 80 characters can be displayed.

First digit	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		73	74	75	76	77	78	79	80
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	~	42	49	4A	4B	4C	4D	4E	4F

MSM6222B-01GS display | MSM5259GS (1) display | MSM5259GS (2) – (8) display | MSM5259GS (9) display

(2) Coordination between address and display position in the 2-line display mode

	First digit	2	3	4	5		39	40 ← Display position
First line	00	01	02	03	04		26	27 ← DD RAM address (hex.)
Second line	40	41	42	43	44		66	67 ←

(Note) Note that the last address of the first line is not consecutive to the head address of the second line.

3

- When MSM6222B-01GS is ued alone, 16 characters (8 characters x 2 lines) max. can be displayed from the first digit to the eight digit.

	First digit	2	3	4	5	6	7	8
First line	00	01	02	03	04	05	06	07
Second line	40	41	42	43	44	45	46	47

When the display is shifted by instruction, the coordination between the LCD display position and the DD RAM address changes as shown below:

(Display shifted to right)

	First digit	2	3	4	5	6	7	8
First line	27	00	01	02	03	04	05	06
Second line	67	40	41	42	43	44	45	46

(Display shifted to left)

	First digit	2	3	4	5	6	7	8
First line	01	02	03	04	05	06	07	08
Second line	41	42	43	44	45	46	47	48

- When the MSM6222B-01GS is used with one MSM5259GS, 32 characters (16 characters x 2 lines) max. can be displayed from the first digit to the sixteenth digit.

	First digit	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
First line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
Second line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

MSM6222B-01GS display | MSM5259GS display

When the display is shifted by instruction, the coordination between the LCD display position and the DD RAM address changes as shown below:

(Display shifted to right)

	First digit 2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
First line	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
Second line	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

MSM6222B-01GS display — MSM5259GS display

(Display shifted to left)

	First digit 2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
First line	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
Second line	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50

MSM6222B-01GS display — MSM5259GS display

- Since the MSM6222B-01GS has a DD RAM capacity for 80 characters, max. 4 pieces of MSM5259GS can be connected to the MSM6222B-01GS in the 2-line display mode.

	First digit 2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		33	34	35	36	37	38	39	40
First line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11		20	21	22	23	24	25	26	27
Second line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51		60	61	62	63	64	65	66	67

MSM6222B-01GS display — MSM5259GS (1) display — MSM5259GS (2) ~ (3) display — MSM5259 (4) display

6. Character Generator ROM (CG ROM)

The CG ROM is used to generate 5 X 7 dot (160 kinds) character patterns or 5 X 10 dot (32 kinds) character patterns from an 8-bit DD RAM character code signal.

The coordination between 8-bit character codes and character patterns is shown in Table 2.

When the 8-bit character code of a CG ROM is written to the DD RAM, the character pattern of the CG ROM corresponding to the code is displayed on the LCD display position corresponding to the DD RAM address.

Table 2 Table of correspondence for character codes and characters (character pattern)

Upper 4 BIT / Lower 4 BIT	MSB 0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
0000 LSB	CG RAM (1)		0	@	P	\	p		—	ｿ	ﾐ	α	
0001	(2)	!	1	A	Q	a	q	。	ｱ	ﾁ	ﾑ	ä	
0010	(3)	"	2	B	R	b	r	「	ｲ	ﾂ	ﾒ	ß	
0011	(4)	#	3	C	S	c	s	」	ｳ	ﾃ	ﾓ	ε	
0100	(5)	$	4	D	T	d	t	、	ｴ	ﾄ	ﾔ	μ	
0101	(6)	%	5	E	U	e	u	・	ｵ	ﾅ	ﾕ	σ	
0110	(7)	&	6	F	V	f	v	ヲ	ｶ	ﾆ	ﾖ	ρ	
0111	(8)	'	7	G	W	g	w	ｧ	ｷ	ﾇ	ﾗ	g	
1000	(1)	(	8	H	X	h	x	ｨ	ｸ	ﾈ	ﾘ	√	
1001	(2)	)	9	I	Y	i	y	ｩ	ｹ	ﾉ	ﾙ	⁻¹	
1010	(3)	*	:	J	Z	j	z	ｪ	ｺ	ﾊ	ﾚ	j	
1011	(4)	+	;	K	[	k	{	ｫ	ｻ	ﾋ	ﾛ	x	
1100	(5)	,	<	L	¥	l	|	ｬ	ｼ	ﾌ	ﾜ	¢	
1101	(9)	—	=	M	]	m	}	ｭ	ｽ	ﾍ	ﾝ	£	
1110	(7)	.	>	N	^	n	→	ｮ	ｾ	ﾎ	ﾞ	ñ	
1111	(8)	/	?	O	_	o	←	ｯ	ｿ	ﾏ	ﾟ	ö	

7. Character Generator RAM (CG RAM)

The CG RAM is used to display user's original character patterns other than the CG ROM.

The CG RAM has the capacity (64 bytes = 512 bits) to write 8 kinds for 5 X 7 dots and 4 kinds for 5 X 10 dots.

When displaying character patterns stored in the CG RAM, write 8-bit character codes (00–07 or 02 to 0F; hex.) on the left side as shown in Table 2. It is then possible to output the character pattern to the LCD display position corresponding to the DD RAM address.

The following is a description on how to write and read character patterns to and from the CG RAM.

(1) When the character pattern is 5 X 7 dots (See Table 3-1).

- **A method to write character pattern into CG RAM by CPU:**

  Three bits of CG RAM address 0–2 correspond to the line position of the character pattern.

  First, set increment or decrement by the CPU, and then input the CG RAM address.

  After this, write character pattern codes into CG RAM through $DB_0 \sim DB_7$ line by line.

  DB_0 to DB_7 correspond to CG RAM data 0–7 in Table 3-1.

  It is displayed when "H" is set as input data and is not display when "L" is set as input data.

  Since the ADC is automatically incremented or decremented by 1 after the writing of data to the CG RAM, it is not necessary to set the CG RAM address again.

  The line, the CG RAM address 0–2 of which are all "H" ("7" in hexadecimal notation), is the cursor position. It is ORed with the cursor at the cursor position and displayed to LCD.

  For this reason, it is necessary to set all input data that become cursor positions to "L".

  Although CG RAM data 0–4 bit are output to the LCD as display data, CG RAM data bit 5–7 are not. The latter can be written and read to and from the RAM, it is therefore allowed to be used as data RAM.

  Accordingly, it is necessary to set all input data which become cursor positions to "H".

  0–4 bit of CG RAM data are output to the LCD as the display data, however, 5–7 bit of CG RAM data are not. But it can be used as RAM because data can be written/read into/from it.

- **A method to display the CG RAM character pattern to the LCD:**

  The CG RAM is selected when 4-upper order bits MSB of the character code are all "L".

  As character code bit 3 is invalid, the display of "0" in Table 3-1, is selected by character code "00" (hex.) or "08" (hex.).

  When the 8-bit character code of the CG RAM is written to the DD RAM, the character pattern of the CG RAM is displayed on the LCD display position corresponding to the DD RAM address. (DD RAM data, bit 0–2 correspond to CG RAM address, bit 3–5.)

(2) When character pattern is 5 x 10 dots (See Table 3-2)

- **A method to write character pattern into the CG RAM by the CPU**

  Four bits of CG RAM address, bit 0–3, correspond to the line position of the character pattern.

  First, set increment or decrement by the CPU, and then input the address of the CG RAM.

  After this, write the character pattern code into the CG RAM, line by line from DB_0–DB_7.

  DB_0 to DB_7 correspond to CG RAM data, bit 0–7, in Table 3-2.

  It is displayed when "H" is set as the input data, while it is not displayed when "L" is set as the input data.

  As the ADC is automatically incremented or decremented by 1 after the writing of data to the CG RAM, it is not necessary to set the CG RAM address again.

  The line in which the CG RAM address 0 to 3 is "A" (hex) is ORed with cursor at the cursor position and displayed on the LCD.

  When the CG RAM data, bit 0–4, CG RAM address, bit 0–3, is "0" ~ "A", it is displayed on the LCD as the display data. When the CG RAM data, bit of 5–7, and CG RAM, bit data is 0–4 and CG RAM address data is "B" ~ "F", it is not output to the LCD.

  But in this case, CG RAM can be used as RAM and it can be written into/read out. So, it can be used as the data RAM.

- **A method to display the CG RAM character pattern to the LCD:**

  The CG RAM is selected when 4-upper order bits MSB of the character code are all "L".

  As MSB and LSB of character code LSD are invalid, the display of "year" 年 in Kanji character is selected by character codes "00", "01", "08", and "09" (hex.) as in Table 3-2.

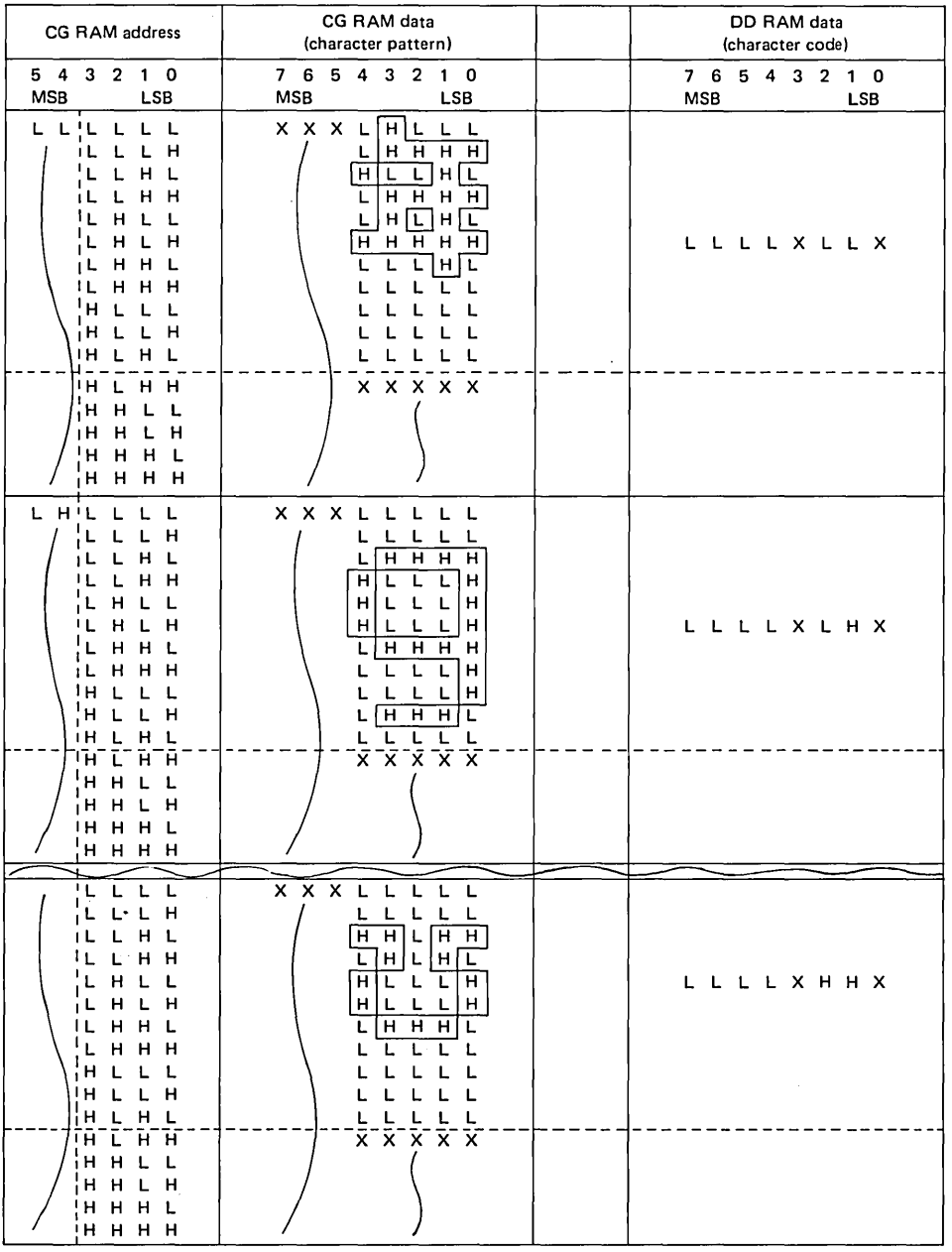
  When the CG RAM character code is written to the DD RAM, the CG RAM character pattern is displayed on the LCD display position corresponding to the DD RAM address.

  (DD RAM data bit 1, 2 correspond to CG RAM address bit 4, 5.)

CG RAM address	CG RAM data (character pattern)		DD RAM data (character code)
5 4 3 2 1 0 MSB LSB	7 6 5 4 3 2 1 0 MSB LSB		7 6 5 4 3 2 1 0 MSB LSB
L L L L L L L L H L H L L H H H L L H L H H H L H H H L L H L L L	X X X L H H H L H L L L H H L L L H H L L L H H L L L H L H H H L L L L L L X X X H L L L H		L L L L X L L L
L L H L H L L H H H L L H L H H H L H H H	H L L H L H L H L L H H L L L H L H L L H L L H L H L L L H L L L L L		L L L L X L L H
H H H L L L L L H L H L L H H H L L H L H H H L H H H	X X X L H H H L L L H L L L L H L L L L H L L L L H L L L L H L L L H H H L L L L L L		L L L L X H H H

X: Irrespective of H/L

Table 3-1 Relation between CG RAM data (character pattern) vs. CG RAM address and DD RAM data vs. character pattern when the caracter pattern is 5 X 7 dots. Above example indicate "OKI".

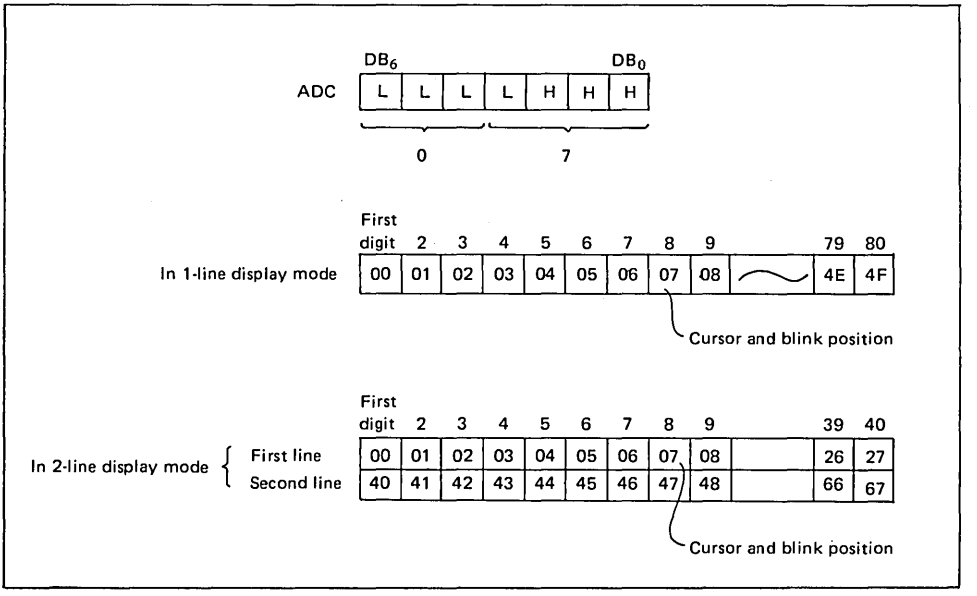


X: Irrespective of H/L

Table 3-2 Relation between CG RAM dada (character pattern) example vs. CG RAM address and DD RAM data vs. character pattern when the character pattern is 5 X 10 dots. Above examples indicate 年 , g, v respectively.

8. Cursor/Blink Control Circuit:

This is a circuit that generates the LCD cursor and blink.
This circuit is under the control of the CPU program. The display of the cursor and blink on the LCD is made at a position corresponding to the DD RAM address set to the ADC.
The figure below shows an example of the curson/ blink position when the value of ADC is set at "07" (hex.).



(Note) The cursor and blink are displayed even when the CG RAM address is set to ADC.
For this reason, it is necessary to inhibit the cursor and blink display while the CG RAM address is set to the ADC.

9. LCD Display Circuit (COM 1 to 16, SEG 1 to 40, L, CP, DO, and DF):

As the MSM6222B-01GS provides the COM signal outputs (16 pcs.) and the SEG signal outputs (40 pcs.), it can display 8 characters (1-line display) or 16 characters (2-line display) as a unit.
The SEG1 ~ SEG40 are used to display 8 digit display on the LCD. To expand the display, an MSM5259GS is used.
The MSM5259GS, 40 dot segement driver, is used for expansion of the SEG signal output.
Interface with the MSM5259GS is made through data output terminal (DO), clock output terminal (CP), latch output terminal (L), and display frequency terminal (DF). The character pattern data is serially transferred to MSM5259GS through DO and CP. When the data of 72 characters 360-bit (= 5-bit/ch. x 72 ch. = 1-line display) or 32 characters 160-bit (5-bit/ch. x 32 ch. = 2-line display) is output, the latch pulse is also output through terminal L. By this latch pulse, the data transferred serially to MSM5259GS is latched to be used as display data. The display frequency signal (DF) required when LCD is displayed is also synchronously output from DF terminal with this latch pulse.

10. Built-in Reset Circuit

The MSM6222B-01GS is automatically initialized when the power is turned on.
During initialization, the busy flag (BF) holds "H" and does not accept instructions (other than the busy flag read).
The busy flag goes to "H" for 15 ms after V_{DD} reaches 4.5V or more.
During initialization, the MSM6222B-01GS executes the following instructions:

- Display clear
- Data length of interface with CPU: 8 bits (8B/4B = H)
- LCD: 1-line display (N = L)
- Character font: 5 x 7 dots (F = L)
- ADC: Increment (I/D = H)
- No display shift (SH = L)
- Display: Off (DI = L)
- Cursor: Off (C = L)
- No blink (B = L)

When the built-in reset circuit is used, it is required to satisfy the following power supply conditions. As the built-in reset circuit does not operate normally unless these power supply conditions are met, initialize the MSM6222B-01GS by instruction through the CPU (refer to initialize instruction).
When a battery is used as supply voltage source, it is required to initialize the instruction.

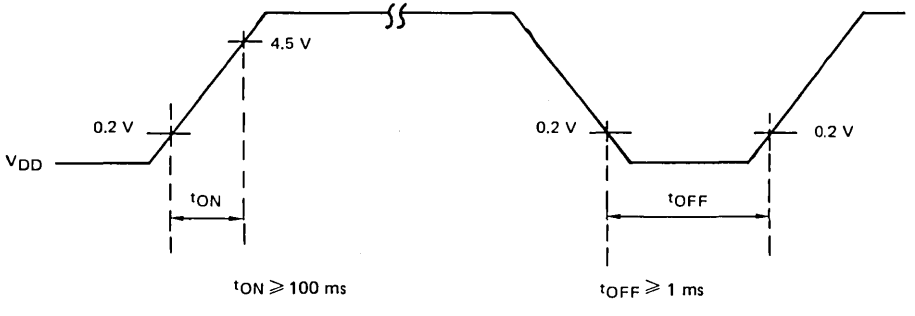


Fig 1 Power ON/OFF waveform

11. Data Bus with CPU

The data bus with CPU is available either once for 8 bits or twice for 4 bits allowing the MSM6222B-01GS to be interfaced with either an 8-bit or 4-bit CPU.

(1) When the interface data length is 8 bits

Data buses DB0 to DB7 (8 pcs.) are all used and data input/output is carried out simultaneously.

(2) When the interface data length is 4 bits

The 8-bit data input/output is carried out in two steps by using only 4-high order bits of data buses DB4 to DB7 (4 pcs.).

The first time data input/output is made for 4-high order bits (DB4 to DB7 when the interfaces data length is 8 bits) and the second time data input/output is made for 4-low order bits (DB0 to DB3 when the interface data length is 8 bits). Even when the data input/output can be completely made through 4-high order bits, be sure to make another input/output of 4-low order bits. (Example: Busy flag Read)
Since the data input/output is carried out in two steps but as one execution, no normal data transfer is executed from the next input/output if accessed only once.

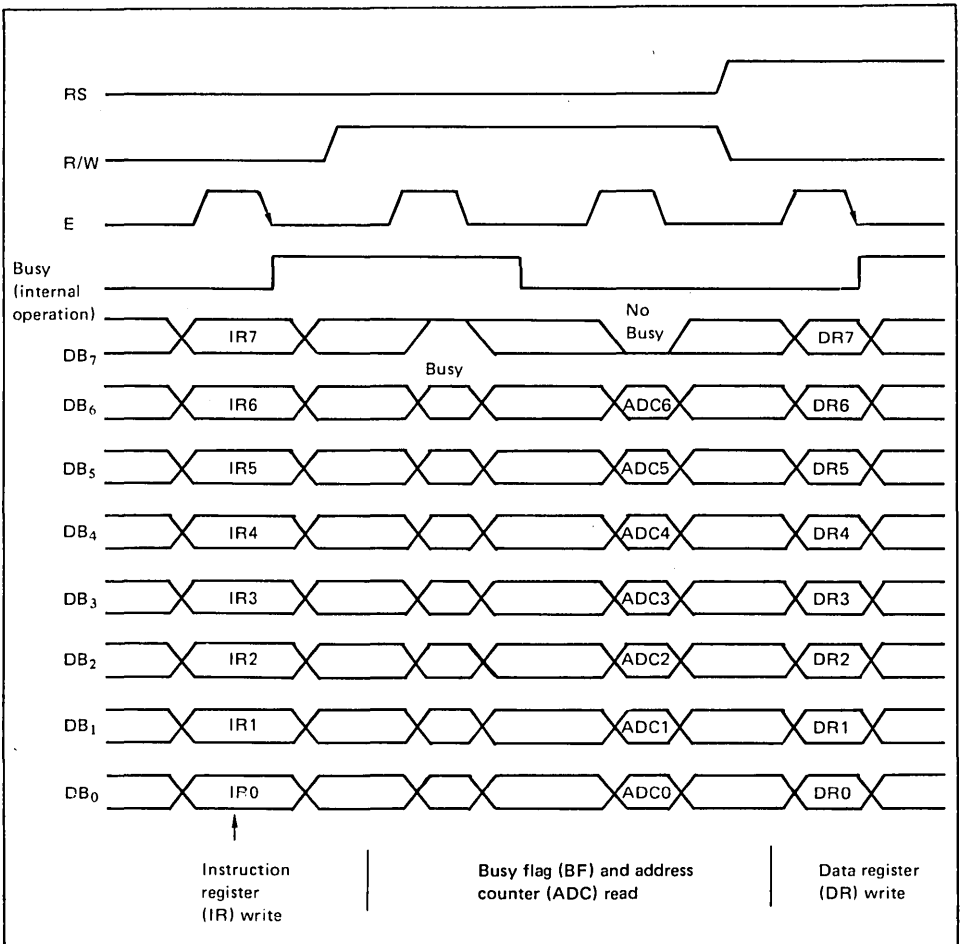


Fig. 2 Example of 8-bit data transfer

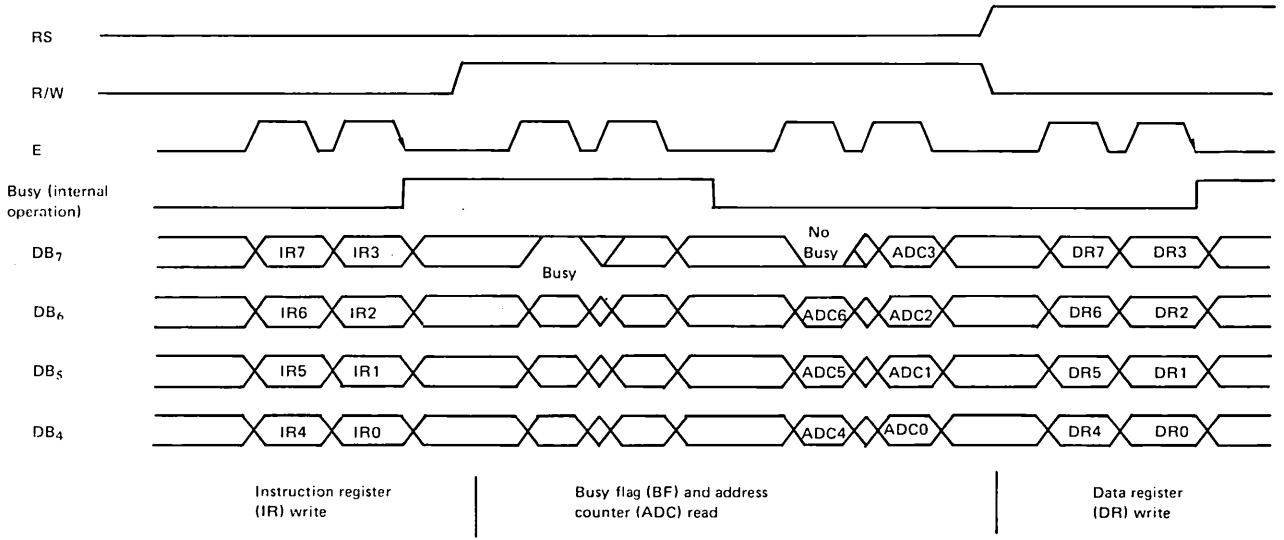


Fig. 3 Example of 4-bit data transfer

12. Instruction Code

The instruction code is defined as the signal through which the MSM6222B-01GS is accessed by the CPU. CPU.

The MSM6222B-01GS begins operation upon receipt of the instruction code input.

As the internal processing operation of MSM6222B-01GS is started with a timing that does not affect the LCD display, the busy status continues longer than the CPU cycle time.

Under the busy status (when the busy flag is set to "H"), the MSM6222B-01GS does not execute any instructions other than the busy flag read.

Therefore, the CPU has to verify that the busy flag is set to "L" prior to the input of the instruction code.

(1) Display clear:

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	L	L	L	L	H

When this instruction is executed, the LCD display is cleared.

When the cursor and blink are in display, the blinking position moves to the left end of the LCD (the left end of the first line in the 2-line display mode).

(Note) All DD RAM data goes to "20" (hex.), while the address counter (ADC) goes to "00" (hex.). The execution time, when the OSC oscillation frequency is 250 KHz is 1.64 ms (max.).

(2) Cursor home

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	L	L	L	H	X

X: Irrespective of H/L

When this instruction is executed, the blinking position moves to the left end of the LCD (to the left end of the first line in the 2-line display mode) when the cursor and blink are being displayed.

When the display is in shift, the display returns to its original position before shifting.

(Note) The address counter (ADC) goes to "00" (hex.). The execution time, when the OSC oscillation frequency is 250 KHz, is 1.64 ms (max.).

(3) Shift mode set

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	L	L	H	I/D	SH

① When the I/D is set, the 8-bit character code is written or read to and from the DD RAM, the cursor and blink shift to the right by 1 character position (I/D = H; increment) or to the left by 1 character position (I/D = L; decrement).

The address counter is incremented (I/D = H) or decremented (I/D = L) by 1 at this time. Even after the character pattern code is written or read to and from the CG RAM, the address counter (ADC) is incremented (I/D = H) or decremented (I/D = L) by 1.

② When SH = H is set, the character code is written to the DD RAM, and then the cursor and blink stop and the entire display shifts to the left (I/D = H) or to the right (I/D = L) by 1 character position.

When the character is read from the DD RAM when SH = H is set, or when the character pattern data is written or read to or from the CG RAM when SH = H is set, the entire display does not shift, but normal write/read is performed (the entire display does not shift, but the cursor and blink shift to the right (I/D = H) or to the left (I/D = L) by 1 character position.

When SH = L is set, the display does not shift, but normal write/read is performed.

The execution time when the OSC oscillation frequency is 250 KHz is 40 μs.

(4) Display mode set

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	L	H	DI	C	B

① The DI bit controls whether the character pattern is displayed or extinguished.
When DI is "H", this bit makes the LCD display the character pattern.
When DI is "L", this bit distinguishes the LCD character pattern. The cursor and blink are also cancelled at this time.
(Note) Different from the display clear, the character code is absolutely not rewritten.

② The cursor goes off when C = L and it is displayed when DI = H and C = H.

③ The blink is cancelled when B = L and it is executed when DI = H and B = H.
In the blink mode, all dots (including the cursor), displaying character pattern, and cursor are displayed alternately at 409.6 ms (in 5 X 7 dots character font) or 563.2 ms (in 5 X 10 dots character font) when the OSC oscillation frequency is 250 KHz. The execution time when the OSC oscillation frequency is 250 KHz is 40 μs.

(5) Cursor and display shift

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	L	D/C	R/L	X	X

X: Irrespective of H/L

When D/C = L and R/L = L, the cursor and blink position are shifted to the left by 1 character position (ADC is then decremented by 1).
When D/C = L and R/L = H, the cursor and blink position are shifted to the right by 1 character position (ADC is then incremented by 1).
When D/C = H and R/L = L, the entire display is shifted to the left by 1 character position. The cursor and blink positions are also shifted with the display (ADC remains unchanged).
When D/C = H and R/L = H, the entire display is shifted to right by 1 character position. The cursor and blink positions are also shifted with the display (ADC remains unchanged).
In the 2-line display mode, the cursor and blink positions are shifted from the first line to the second line when the cursor is shifted to the right next to the fortieth digit (27; hex.) in the first line. No such shifting is made in other cases.
When shifting the entire display, the display pattern, cursor, and blink positions are in no case shifted between lines (from the first line to the second line or vice versa).
The execution time when the OSC oscillation frequency is 250 KHz is 40 μs.

(6) Initial set

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	H	8B/4B	N	F	X	X

X: Irrespective of L/O

① When 8B/4B = H, the data input/output to and from the CPU is carried out simultaneously by means of 8 bits DB7 to DB0.
When 8B/4B = L, the data input/output to and from the CPU is carried out in two steps through of 4 bits DB7 to DB4.

② The 2-line display mode of the LCD is selected when N = H, while the 1-line display mode is selected when N = L.

③ The 5 X 7 dots character font is selected when F = L, while the 5 X 10 dots character font is selected when F = H and N = L.

This initial set has to be accessed prior to other instructions excepting the busy flag read after powering ON the MSM6222B-01GS.

N	F	Number of display lines	Character font	Duty ratio	Number of biases	Number of COMMON signals
L	L	1-line	5 X 7 dots	1/8	4	8
L	H	1-line	5 X 10 dots	1/11	4	11
H	L	2-line	5 X 7 dots	1/16	5	16
H	H	2-line	5 X 7 dots	1/16	5	16

Generate biases externally and input them to the MSM6222B-01GS (V_{DD}, V1, V2, V3, V4, and V5).
When the number of biases is 4, input the same potential to V2 and V3. The execution time, when the OSC oscillation frequency is 250 KHz, is 40 μs.

(7) CG RAM address set

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	H	C_5	C_4	C_3	C_2	C_1	C_0

When CG RAM addresses, bit C_5 to C_0 (binary), are set, the CG RAM is specified, until the DD RAM address is set.
Write/read of the character pattern to and from the CPU begins with addresses, bit C_5 to C_0, starting from CG RAM selection.
The execution time, when the OSC oscillation frequency is 250 KHz, is 40 μs.

(8) DD RAM address set

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	H	D_6	D_5	D_4	D_3	D_2	D_1	D_0

When the DD RAM addresses D6 to D0 (binary) are selected, the DD RAM is specified until the DD RAM address is set.
Write/read of the character code to and from the CPU begins with addresses D_6 to D_0 starting from DD RAM selection.
In the 1-line display mode (N = H), however, D_6 to D_0 (binary) must be set to one of the values among "00" to "4F" (hex.).

Likewise, in the 2-line mode, D_6 to D_0 (binary) must be set to one of the values among "00" ~ "27" (hex.) or "40" – "67" (hex.).
When any value other than the above is input, it is impossible to make a normal write/read of character codes to and from the DD RAM.
The execution time, when the OSC oscillation frequency is 250 KHz, is 40 μs.

(9) DD RAM and CG RAM data write

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	H	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0

When E7 to E0 (binary) codes are written to the DD RAM or CG RAM, the cursor and display move as described in "(5) Cursor and display shift". The execution time, when the OSC oscillation frequency is 250 KHz, is 40 μs.

(10) Busy flag and address counter read

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	H	L	BF	0_6	0_5	0_4	0_3	0_2	0_1	0_0

The busy flag (BF) is output by this instruction to indicate whether the MSM6222B-01GS is engaged in internal operations (BF = "H") or not (BF = "L").
When BF = "H", no new instruction is accepted. It is therefore necessary to verify BF = "L" before inputting a new instruction.
When BF = "L", a correct address counter value is output. The address counter value must match the DD RAM address or CG RAM address. The decision of whether it is a DD RAM address or CG RAM address is made by the address previously set.
Since the address counter value when BF = "H" is sometimes incremented or decremented by 1 during internal operations, it is not always a correct value.
Execution time is 1 μs.

(11) DD RAM and CG RAM data read

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	H	H	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

Character codes (bit P_7 to P_0) are read from the DD RAM, while character patterns (P7 to P0) from the CG RAM.
Selection of DD RAM or CG RAM is decided by the address previously set.
After reading those data, the address counter (ADC) is incremented or decremented by 1 as set by the shift mode mentioned in item "(3) shift mode set".
The execution time, when the OSC oscillation frequency is 250 KHz, is 40 μs.

(Note) Conditions for the reading of correct data:

1. When the DD RAM address set or CG RAM address set is input before inputting this instruction.
2. When the cursor/display shift is input before inputting this instruction in case the character code is read.
3. Data after the second reading from RAM when read more than 2 times. Correct data is not output in any other case.

13. Instruction Initialization

(1) When data input/ouput to and from the CPU is carried out by 8 bits (DB0 to DB7):

① ● Turn on the power
② ● Wait for 15 ms or more after V_{DD} has reached 4.5V or more.
③ ● Set 8B/4B at H by initial reset of instruction.
④ ● Wait for 4.1 ms or more.
⑤ ● Set 8B/4B at H by initial reset of instruction.
⑥ ● Wait for 100 μs or more.
⑦ ● Set 8B/4B at H by initial reset of instruction.
⑧ ● Check the busy flag as No Busy.
⑨ ● Set 8B/4B at H. Set LCD line number (N) and character font (F).
(After this, do not change the LCD line number and character font.)
⑩ ● Check No Busy.
⑪ ● Clear the display by setting the display mode.
⑫ ● Check No Busy.
⑬ ● Clear the display.
⑭ ● Check No Busy.
⑮ ● Set the shift mode.
⑯ ● Check No Busy.
⑰ ● Initialization completed.

Example of Instruction Code for Steps ③, ⑤, and ⑦.

R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
L	L	L	L	H	H	X	X	X	X

X: Irrespective of H/L

(2) When data input/output to and from the CPU is carried out by 4 bits (DB4 to DB7):

① ● Turn on the power.
② ● Wait for 15 ms or more after V_{DD} has reached 4.5V or more.
③ ● Set 8B/4B at H by initial reset of instruction.
④ ● Wait for 4.1 ms or more.
⑤ ● Set 8B/4B at H by initial reset of instruction.
⑥ ● Wait for 100 μs or more.
⑦ ● Set 8B/4B at H by initial reset of instruction.
⑧ ● Check the busy flag as No Busy.
⑨ ● Set 8B/4B at L. Set LCD line number (N) and character font (F).
⑩ ● Check No Busy.
⑪ ● Set 8B/4B at L. Set LCD line number (N) and character font (F).
⑫ ● Check No Busy.
⑬ ● Clear the display by setting the display mode.
⑭ ● Check No Busy.
⑮ ● Clear the display.
⑯ ● Check No Busy.
⑰ ● Set the shift mode.
⑱ ● Check No Busy.
⑲ ● Initialization completed.

Example of Instruction Code for Steps ③, ⑤, and ⑦.

R/W	RS	DB_7	DB_6	DB_5	DB_4
L	L	L	L	H	H

Example of Instruction Code for Step ⑨.

R/W	RS	DB_7	DB_6	DB_5	DB_4
L	L	L	L	H	L

LCD DRIVE WAVEFORM

Figures 4, 5 and 6 show the LCD driving waveform consists of COM signal, SEG signal DF signal and L (latch pulse waveform) signal, in the duty of 1/8, 1/11 and 1/16 respectively.

The relation between duty and frame frequency is described in the table below.

Duty	Frame frequency
1/8	78.1 Hz
1/11	56.8 Hz
1/16	78.1 Hz

(Note) The OSC oscillation frequency is assumed to be 250 KHz.

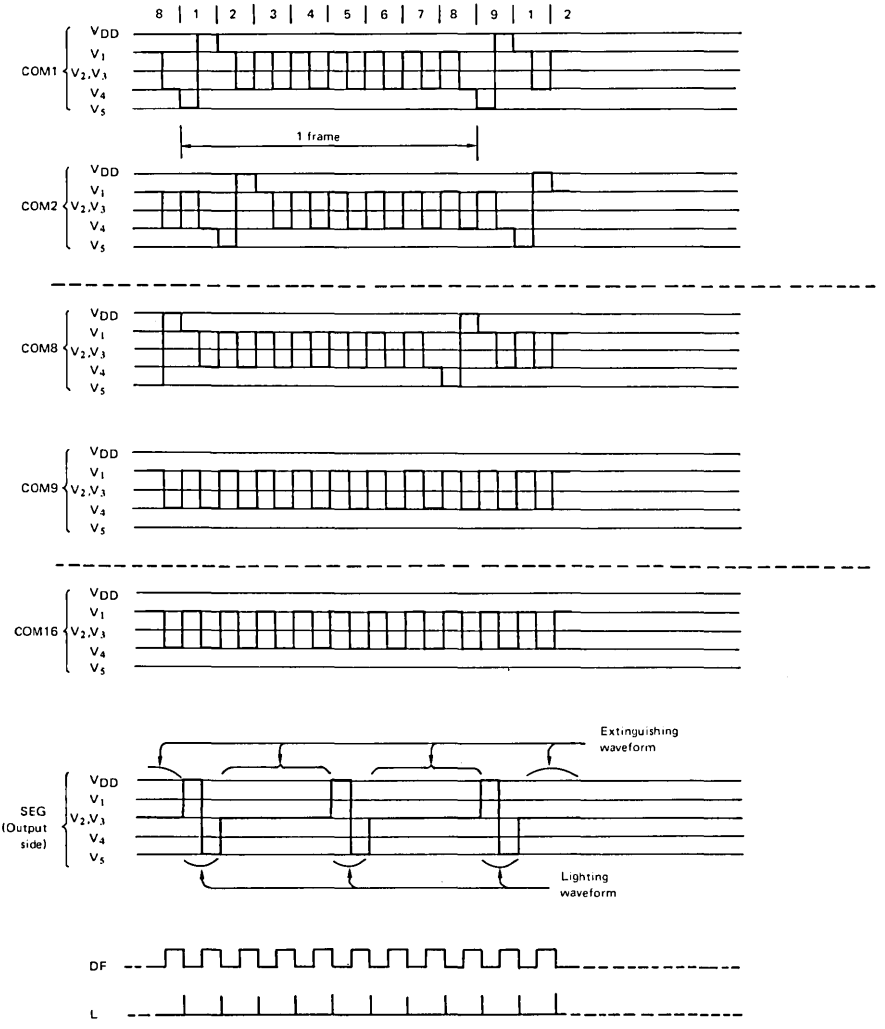


Figure 4 LCD driving waveform at 1/8 duty.

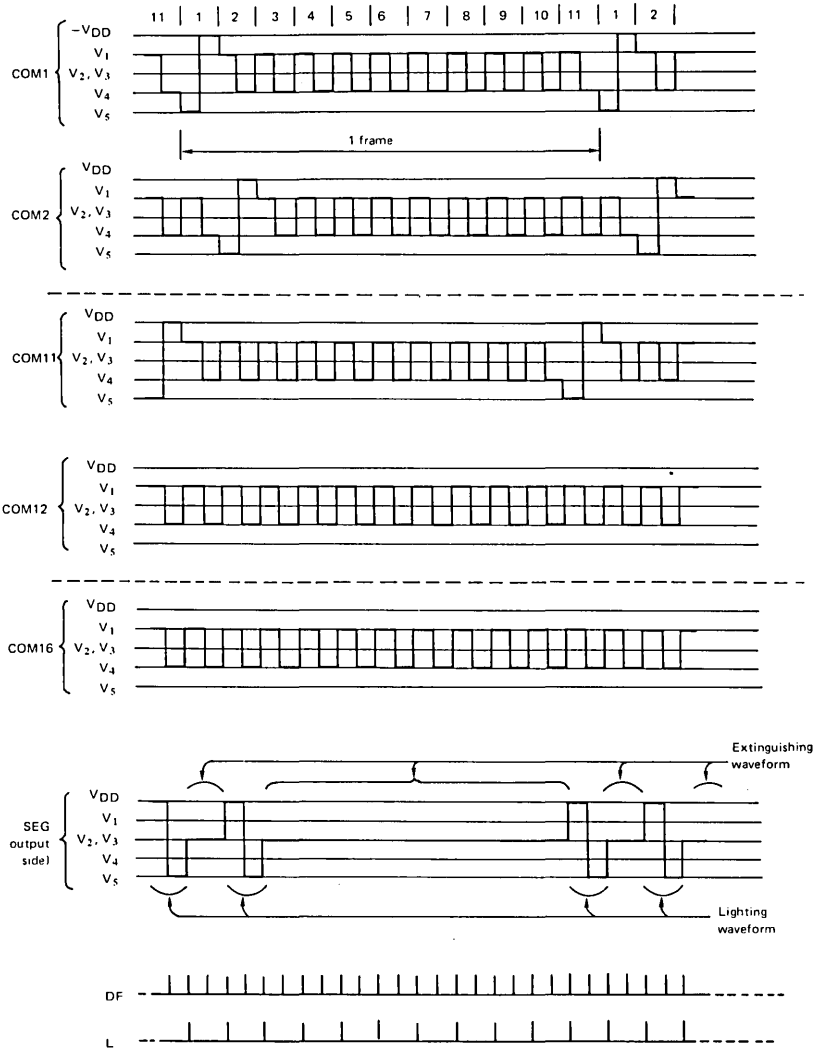


Figure 5 LCD driving waveform at 1/11 duty.

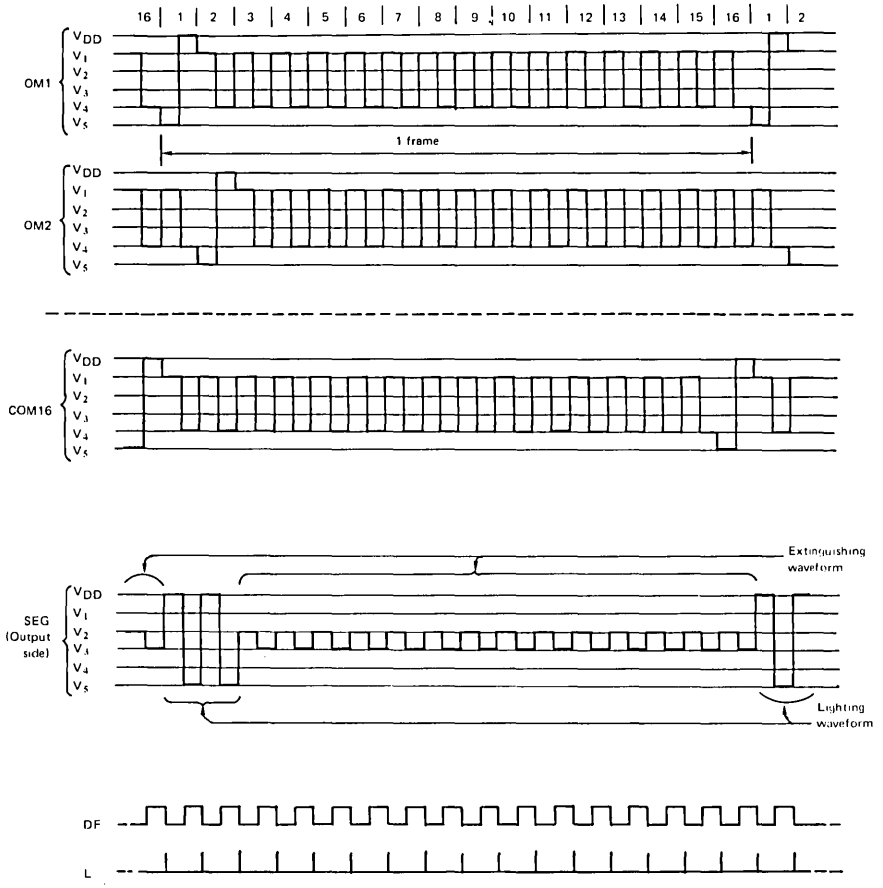


Figure 6 LCD driving waveform at 1/16 duty.

INPUT/OUTPUT TIMING TO AND FROM THE CPU AND OUTPUT TIMING TO MSM5259GS

Table 4, 5 and 6 show input characteristics from the CPU, output characteristics to the CPU and output characteristics to MSM5259GS respectively.

- **Input characteristics from the CPU**

(V_{DD} = 4.5 ~ 5.5V, T_a = −20 ~ +75°C)

Item	Symbol	Range			Unit
		MIN	TYP	MAX	
R/W and RS set-up time	t_B	140	–	–	nS
E and H pulse width	t_W	280	–	–	nS
R/W and RS holding time	t_A	10	–	–	nS
E rise time	t_r	–	–	25	nS
E fall time	t_f	–	–	25	nS
E and L pulse width	t_L	280	–	–	nS
E cycle time	t_C	667	–	–	nS
DB_0 to DB_7 input data set-up time	t_I	180	–	–	nS
DB_0 to DB_7 input data holding time	t_H	10	–	–	nS

Table 4: Input characteristics from the CPU

- **Output characteristics to the CPU**

(V_{DD} = 4.5 ~ 5.5V, T_a = −20 ~ +75°C)

Item	Symbol	Range			Unit
		MIN	TYP	MAX	
R/W and RS set-up time	t_B	140	–	–	nS
E and H pulse width	t_W	280	–	–	nS
R/W and RS holding time	t_A	10	–	–	nS
E rise time	t_r	–	–	25	nS
E fall time	t_f	–	–	25	nS
E and L pulse width	t_L	280	–	–	nS
E cycle time	t_C	667	–	–	nS
DB_0 to DB_7 data output delay time	t_D	–	–	220	nS
DB_0 to DB_7 data output holding time	t_O	20	–	–	nS

Table 5: Output characteristics to the CPU

- **Output characteristics to MSM5259GS**
  (V_{DD} = 4.5 ~ 5.5V, T_a = −20 ~ +75°C)

Item	Symbol	Range			Unit
		MIN	TYP	MAX	
CP and H pulse width	t_{HW1}	800	–	–	nS
CP and L pulse width	t_{LW}	800	–	–	nS
DO set-up time	t_S	300	–	–	nS
DO holding time	t_{DH}	300	–	–	nS
L clock set-up time	t_{SU}	500	–	–	nS
L clock holding time	t_{HO}	100	–	–	nS
L and H pulse width	t_{HW2}	800	–	–	nS
DF delay time	t_M	−1000	–	1000	nS

Table 6: Output characteristics to MSM5259GS

Figures 7, 8 and 9 show input timing from the CPU, output timing to the CPU and output timing to MSM5259GS respectively.

- **Input timing from the CPU**

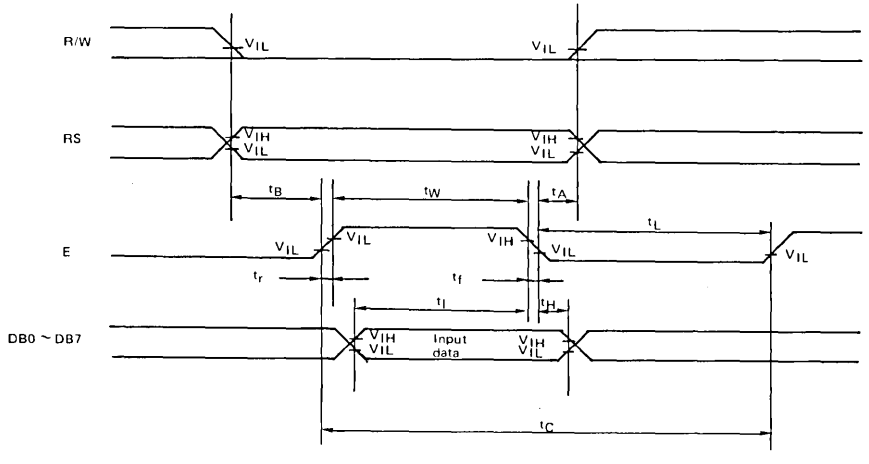


Figure 7

● **Output timing to the CPU**

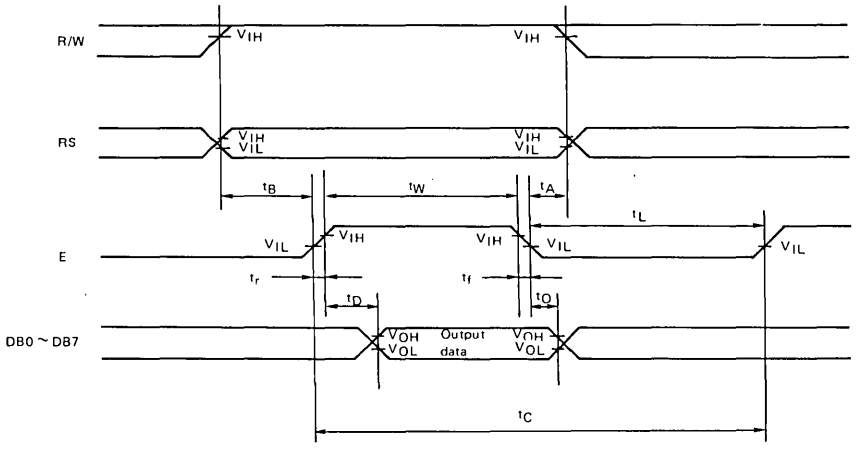


Figure 8

● **Output timing to MSM5259GS**

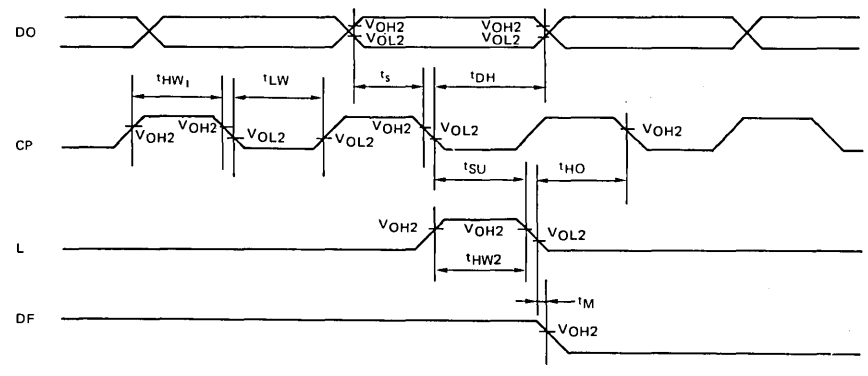


Figure 9

TYPICAL APPLICATION

Interface with LCD and MSM5259GS

Display examples when setting the 5 X 7 dots character font 1-line mode, 5 X 10 dots character font 1-line mode, and 5 X 7 dots character font 2-line mode through instructions are shown in Figures 10, 11, and 12, respectively.

When the 5 X 7 dots character font is set in the 1-line display mode, the COM signals COM9 to COM16 are output for extinguishing.

Likewise, when the 5 X 10 dots character font (1-line is set, the COM signals COM12 to COM16 are output for extinguishing.

The display example shows a combination of 16 characters (32 characters for the 2-line display mode) and the LCD. When the number of MSM5259GSs are increased according to the increase in the number of characters, it is possible to display a maximum of 80 characters.

Besides, it is necessary to generate bias voltage required for LCD operation by splitting resistors outside the IC to input it to MSM6222B-01GS and MSM5259GS.

Examples of these bias voltages are shown in Figures 13, 14, 15, and 16. Basically, this can be done by dividing the voltage of the resistors as shown in Figures 4 and 5. If the value of resistor R is made larger to reduce system power consumption, the LCD operating margin decreases and the LCD drive To prevent this, a by-pass condenser is serially connected to the resistor to lower voltage division impedance caused by the splitting of resistors as shown in Figures 15 and 16.

As the values of R, VR, and C vary according to the LCD size used and V_{LCD} (LCD drive voltage), these values have to be determined through actual experimentation in combination with the LCD. (Example set values:

$R = 3.3 - 10\ K\Omega$, $V_R = 10 - 30\ K\Omega$, and

$C = 0.0022\ \mu F$ to $0.047\ \mu F$)

Figure 17 shows an application circuit for the MSM6222B-01GS and MSM5259GS including a bias circuit.

The bias voltage has to maintain the following potential relation:

$$V_{DD} > V_1 > V_2 \geqq V_3 > V_4 > V_5$$

- In the case of 1-line 16 characters display (5 x 7 dot/font).

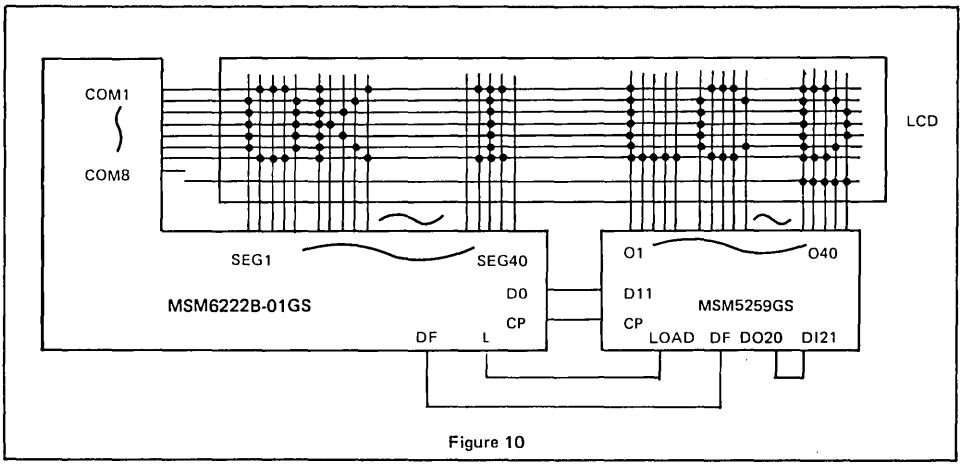


Figure 10

- In the case of 1-line 16 characters display (5 x 10 dot/font)

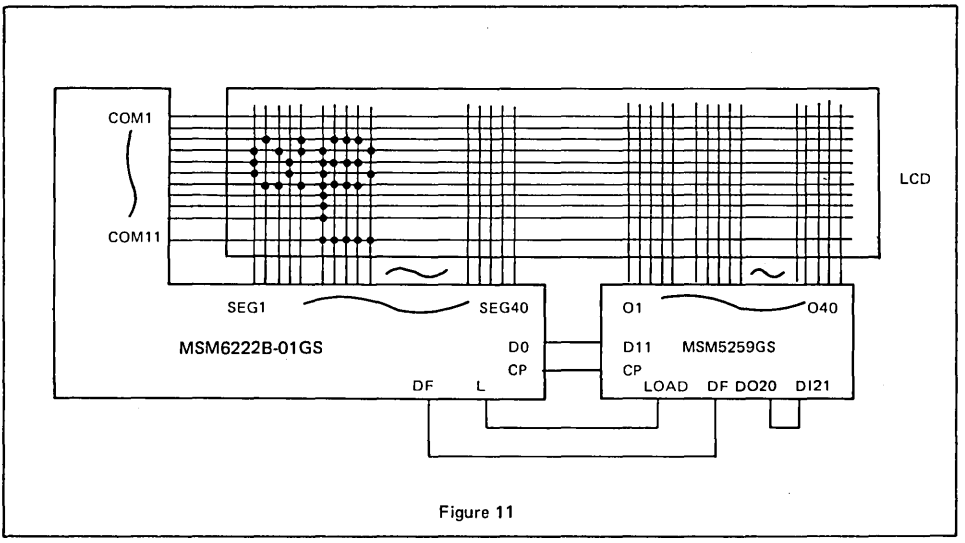


Figure 11

- In the case of 2-lines 16 characters display (5 x 7 dot/font)

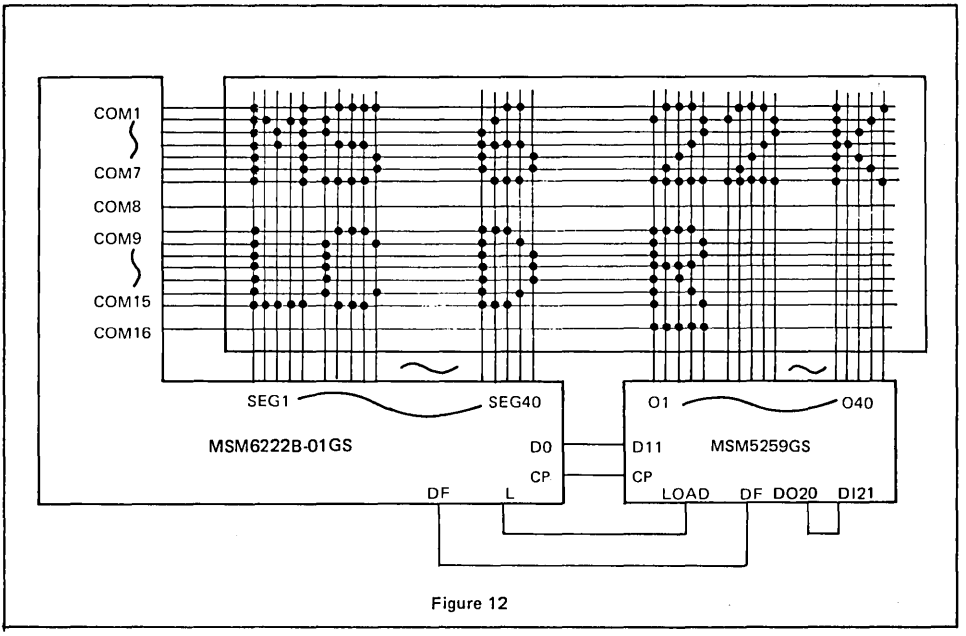


Figure 12

● Bias voltage circuit (1-line display mode)

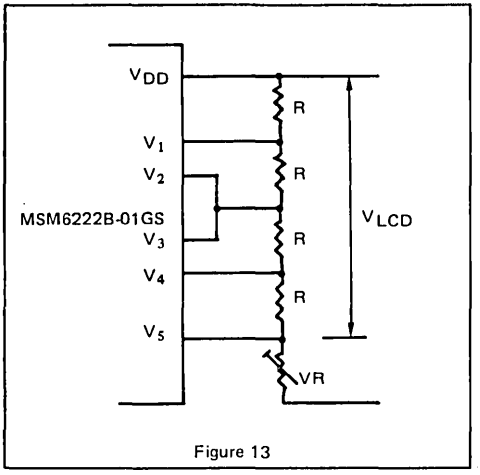


Figure 13

● Bias voltage circuit (2-line display mode)

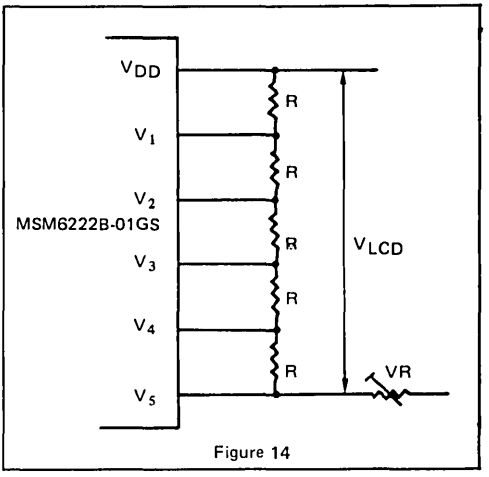


Figure 14

● Bias voltage circuit (1-line display mode)

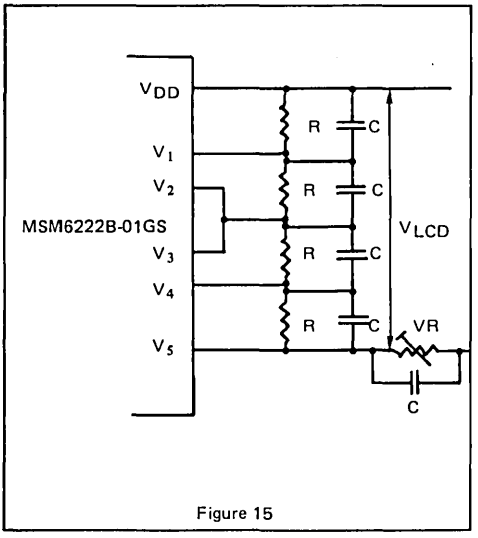


Figure 15

● Bias voltage circuit (2-line display mode)

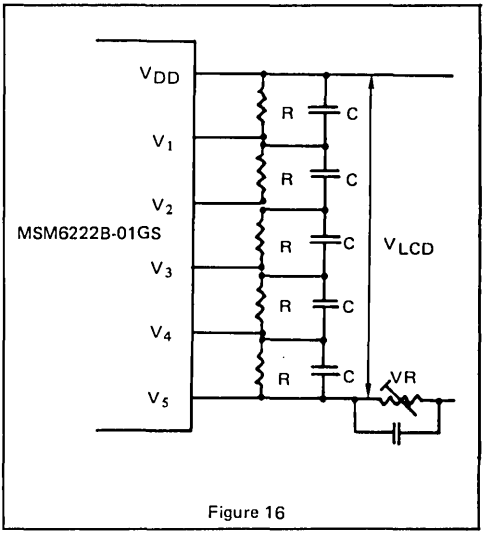


Figure 16

(V_{LCD}: LCD driving voltage)

● Application circuit.

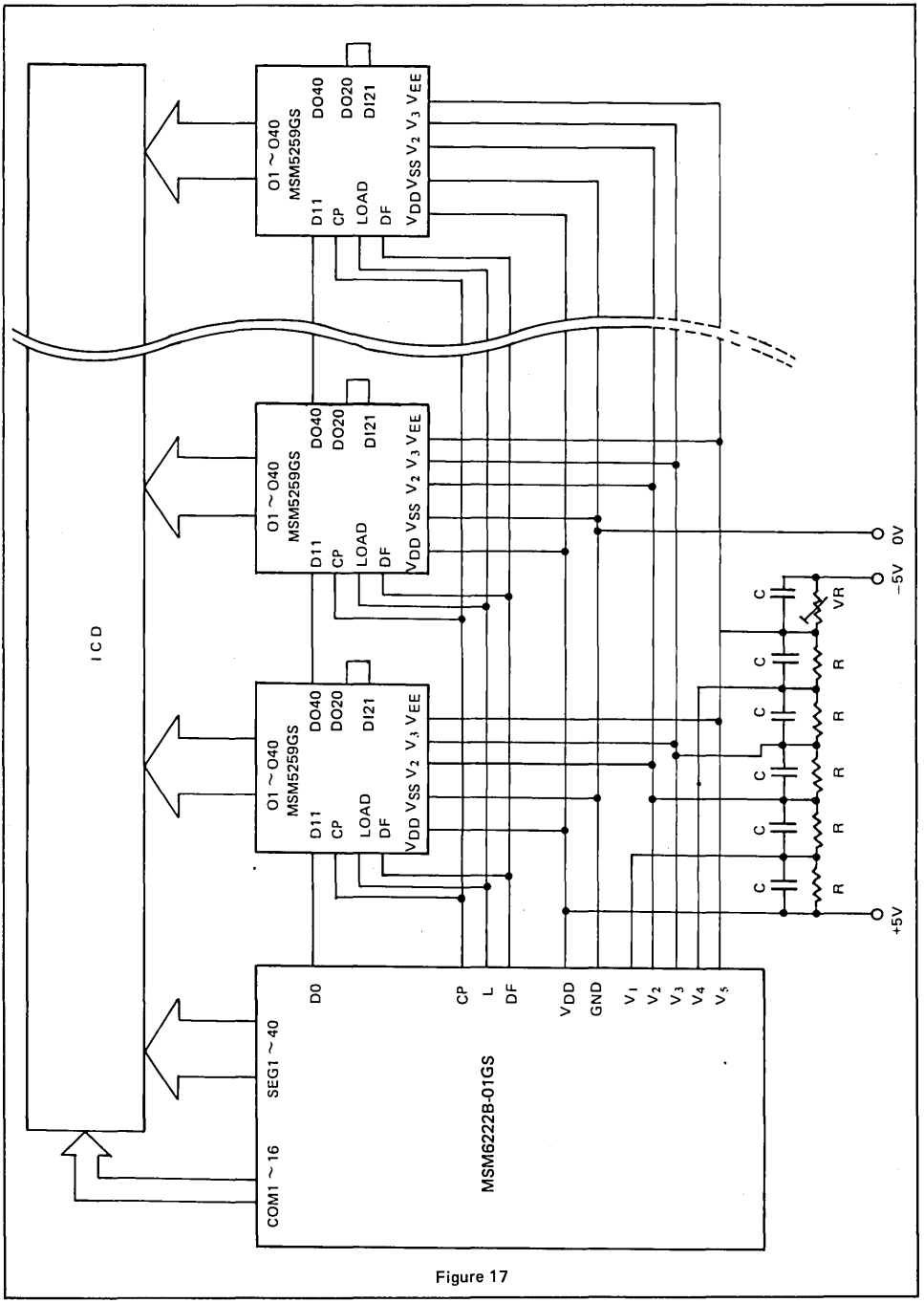


Figure 17

MSM6240GS

DOT MATRIX LCD CONTROLLER

GENERAL DESCRIPTION

The OKI MSM6240GS is a CMOS Si-gate LSI to control large size dot matrix LCD in characters and graphics.

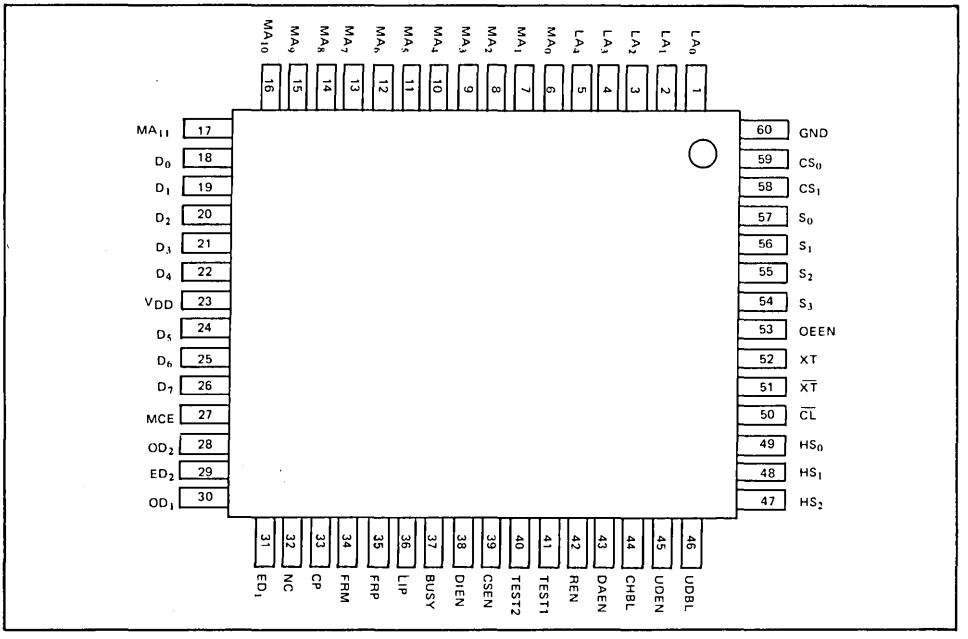
Three kinds of display modes are provided; Semi-graphic mode, Full-graphic mode and Character mode.

FEATURES

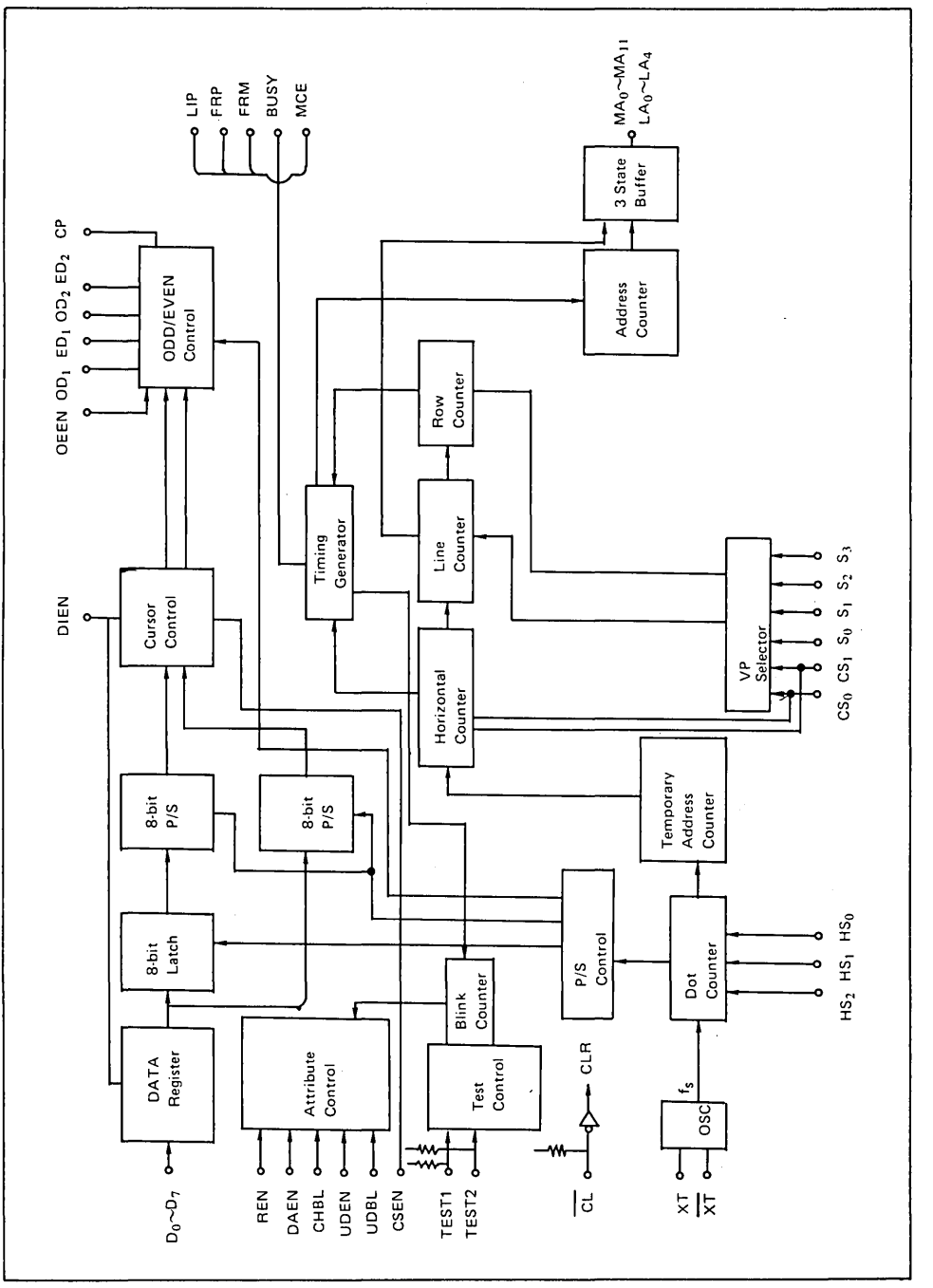
- Number of characters: 32, 40, 64 and 80/line
- Number of lines: 4 X 2, 6 X 2, 8 X 2 and 16 X 2
- Font composition (vertical): 8, 12, 18 and 20; hereinafter called VP (vertical pitch)
- Font composition (horizontal): 5, 6, 7, 8, 10, 12, 14 and 16; hereinafter called HP (horizontal pitch)
- Address: Straight binary
- Attribute
  1) Display inversion
  2) Display blank
  3) Cursor display
  4) Character blink
  5) Cursor blink
- Applicable LCD duty: 1/32, 1/48, 1/64, 1/72, 1/80, 1/96, 1/108, 1/128, 1/144
- Low power CMOS Silicon gate technology
- Single +5V power supply.
- 60 pin plastic flag package (bent lead)

PIN CONFIGURATION

(Top View) 60 Lead Flag Package



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	T_a = 25°C	−0.3 ~ 6.0	V
Input voltage	V_{IN}	T_a = 25°C	−0.3 ~ V_{DD}	V
Storage temperature	T_{stg}	—	−50 ~ 150	°C

3

OPERATING RANGE

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	—	4.5 ~ 5.5	V
Operating temperature	T_{op}	—	−20 ~ 85	°C

INPUT CHARACTERISTICS

(V_{DD} = 5V ± 10%, T_a = 25°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Applicable terminal
"H" Input voltage	V_{IH}	—	2.4	–	–	V	D_0 ~ D_7, REN
"L" Input voltage	V_{IL}	—	–	–	0.8	V	DAEN, CHBL, CSEN, UDEN, UDBL, DIEN
"H" Input voltage	V_{IH}	—	3.6	–	–	V	HS_0 ~ HS_2, CS_0, CS_1, S_0 ~ S_3, OEEN
"L" Input voltage	V_{IL}	—	–	–	1.0	V	
"H" Input current	I_{IH}	—	–	–	−1	μA	D_0 ~ D_7, REN, DAEN, CHBL, CSEN, UDEN, UDBL, FS, DIEN, HS_0 ~ HS_2, CS_0, CS_1, S_0 ~ S_3, OEEN
"L" Input current	I_{IL}	—	–	–	1	μA	
"H" Input current	I_{IH}	—	–	–	−1	μA	TEST1 ~ TEST3
"L" Input current	I_{IL}	—	–	500		μA	
"H" Input current	I_{IH}	—	–	–	−1	μA	$\overline{CL}$
"L" Input current	I_{IL}	—	–	50		μA	

OUTPUT CHARACTERISTICS

(V_{DD} = 5V ± 10%, Ta = 25°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Applicable terminal
"H" Output current	I_{OH}	V_{OH} = 2.8V	−500	–	–	μA	MA_0 ~ MA_{11}, LA_0 ~ LA_4, OD_1, ED_1, OD_2, ED_2, CP, BUSY, FRM, FRP, MCE, LIP
"L" Output current	I_{OL}	V_{OL} = 0.4V	2.1	–	–	mA	

POWER CONSUMPTION

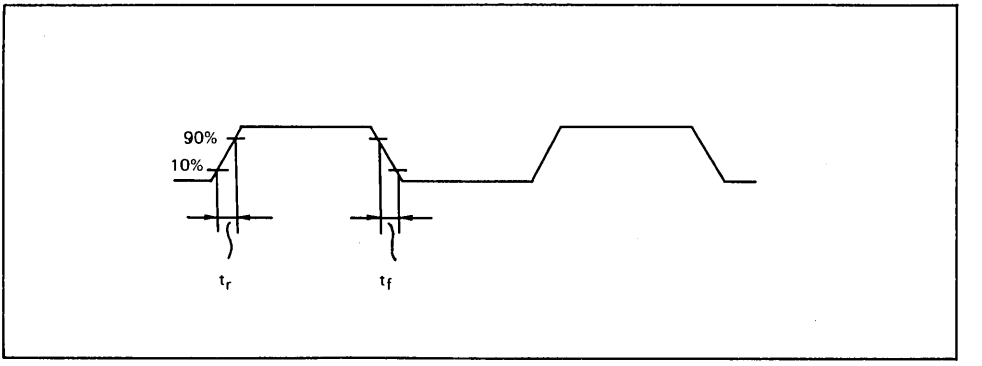
(Ta = 25°C)

Parameter	Symbol	V_{DD}	Condition	MIN	TYP	MAX	Unit	
Static current	I_{DDS}	5	f_{osc} = 0 Hz	–	–	50	μA	No load
Operating current	I_{DD}	5	f_{osc} = 10 MHz	–	–	10	mA	No load

3

SWITCHING CHARACTERISTICS

(V_{DD} = 5V ± 10%)



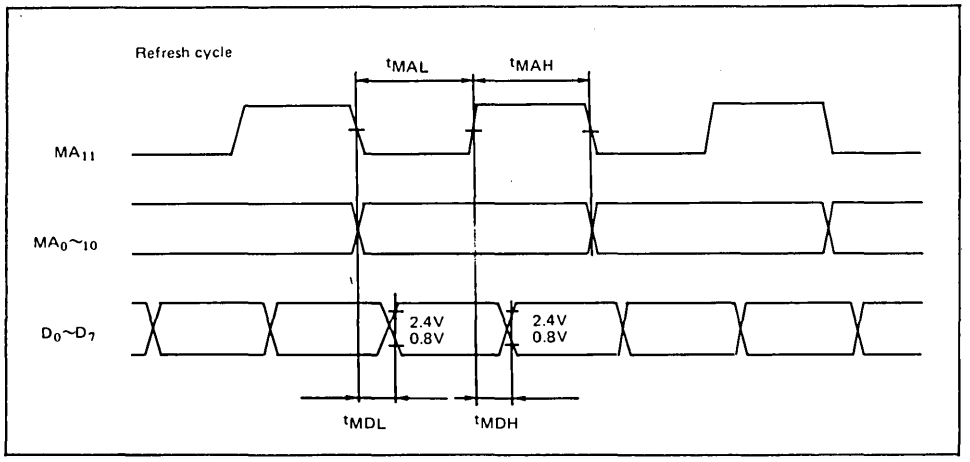
Parameter	Symbol	Load condition	MIN	TYP	MAX	Unit	Applicable terminal
Clock pulse	t_r	CL = 150PF	–	–	100	ns	All output terminals
Rise and fall time	t_f	CL = 150PF	–	–	100	ns	

MAXIMUM OPERATING FREQUENCY

(V_{DD} = 5V ± 10%)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Oscillation frequency	f_{osc}	—	10	–	–	MHz

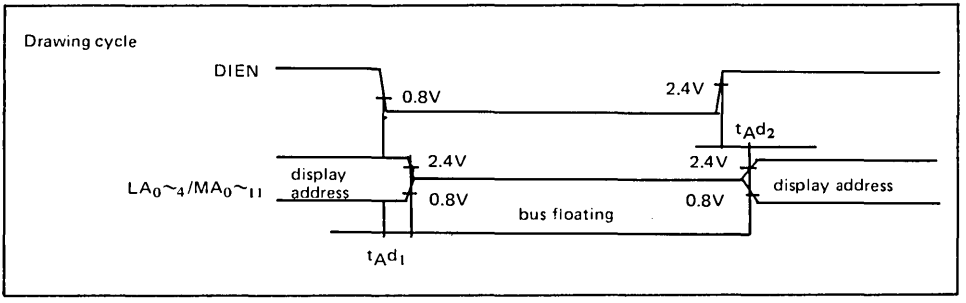
INTERFACE WITH EXTERNAL RAM, ROM



(C_L = 80pF)

Parameter	Symbol	MIN	TYP	MAX	Unit
Memory address time to the upper part	t_{MAL}	500	–	–	ns
Memory address time to the lower part	t_{MAH}	500	–	–	ns
Memory data delay time of the upper part	t_{MDL}	–	–	t_{MAL}-70	ns
Memory data delay time of the lower part	t_{MDH}	–	–	t_{MAH}-70	ns

Note: t_{MAL} and t_{MAH} is calculated by the following formula.
$t_{MAL} = t_{MAH} = 2/f_{osc} \times HP/2$
t_{MAL} and t_{MAH} become the minimum speed when HP is set at 5 and f_{osc} is 5MHz.

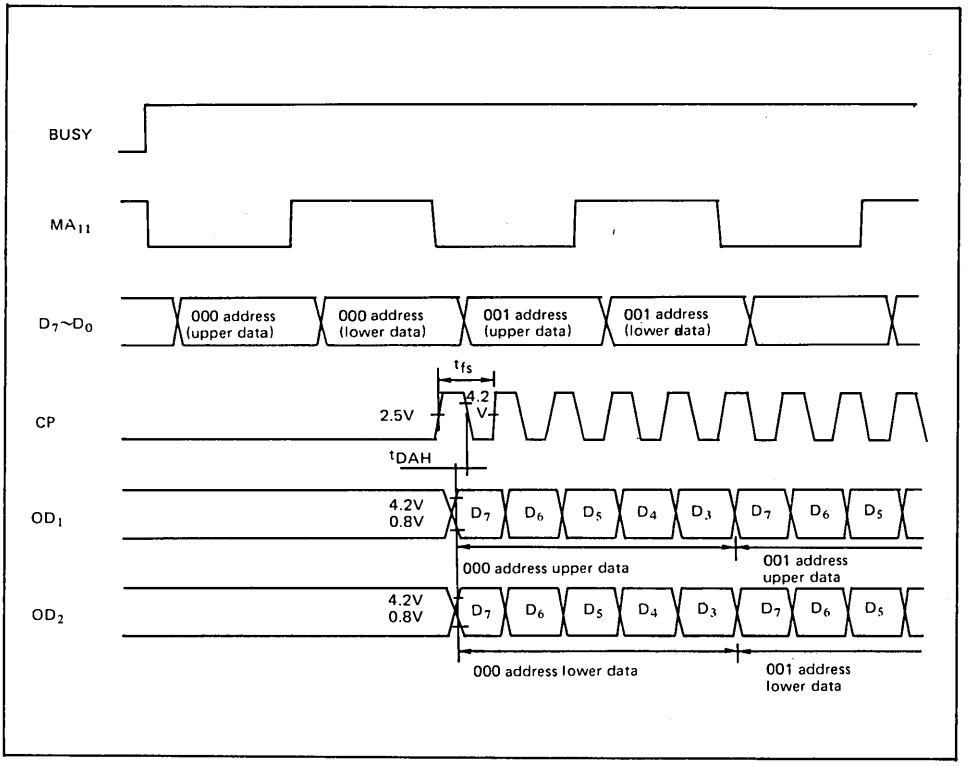


(CL = 150pF)

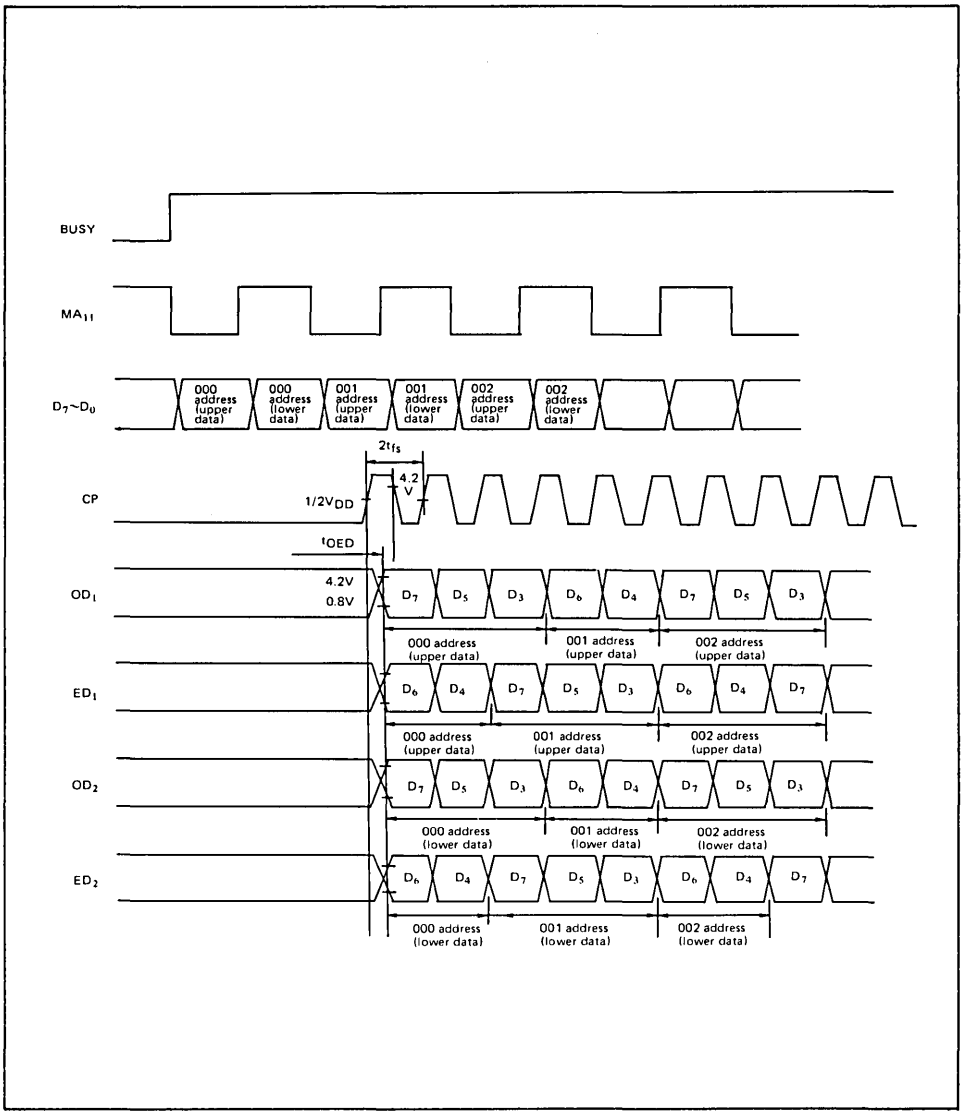
Parameter	Symbol	MIN	TYP	MAX	Unit
Drawing address delay time	t_{Ad1}			20	ns
Display address delay time	t_{Ad2}			120	ns

THE DISPLAY DATA TO LCD DRIVERS

1) Without ODD/EVEN data processing



2) Under ODD/EVEN data processing



(C_L = 80pF)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Shift clock pulse cycle time	t_{fs}	—	300	–	–	ns
Shift data delay time	t_{DAH}	—	–	–	50	ns
Shift clock pulse cycle time	$2t_{fs}$	—	400	–	–	ns
Shift clock data delay time	t_{OED}	—	–	–	80	ns

PIN DESCRIPTION

Terminal name	I/O/Z	Function
OD_1 ED_1	$\overline{O}$	(Odd data) Output of serial data for X driver (Even data) Upper screen's data
OD_2 ED_2	$\overline{O}$	(Odd data) Output of serial data for X driver (Even data) Lower screen's data
LIP	$\overline{O}$	(Latch pulse) Latch pulse for one line
FRP	$\overline{O}$	(Frame pulse) Signal input to Y driver
FRM	$\overline{O}$	(Frame) Frame inversion signal
CP	$\overline{O}$	(Shift clock pulse) Shift clock pulse for X driver
BUSY	$\overline{O}$	"READY" SIGNAL L druing suspension of serial transfer
DIEN	I	(Display enable) Display enable signal; active H
MCE	$\overline{O}$	(Chip Enable) Memory chip enable control signal
$\overline{CL}$	I	(Clear) Clear terminal
XT $\overline{XT}$	I $\overline{O}$	(X'tal OSC) Crystal oscillation
V_{DD}		+5V
GND		0V
OEEN	I	Odd-number even-number data enable; active H

Terminal name	I/O/Z	Function
MA_0 ∫ MA_{10}	$\overline{O}$/Z	(Memory address) Memory refresh address output, straight binary address $MA_0 \sim MA_{11}$ and $LA_0 \sim LA_4$ are at high impedance during DIEN = L
MA_{11}	$\overline{O}$/Z	Highest order bit of address signal, switching of upper and lower surfaces $MA_0 \sim MA_{11}$ and $LA_0 \sim LA_4$ are at high impedance during DIEN = L
LA_0 ∫ LA_4	$\overline{O}$/Z	(Line address) Line scan output for character generation $MA_0 \sim MA_{11}$ and $LA_0 \sim LA_4$ are at high impedance during DIEN = L
D_0 ∫ D_7	I	Display data input
S_0 ∫ S_3	I	Selection of number of VP and lines Refer to Sec. 10
CS_0 ∫ CS_1	I	Selection of number of characters to be displayed

CS_1	L	L	H	H
CS_0	L	H	L	H
No. of characters	32	40	64	80

HS_0 ∫ HS_2	I	(Horizontal select) HP programming
REN	I	(Reverse enable) Display inversion; active H
DAEN	I	Data input enable signal; active H
UDEN	I	Cursor display; active H
CHBL	I	Character blink; active H
UDBL	I	Cursor blink; active H
CSEN	I	Cursor display; active H
TEST1 ∫ TEST3	I	Test pins. On-chip pull-up resistors

FUNCTIONAL DESCRIPTION

1. Selection of HP

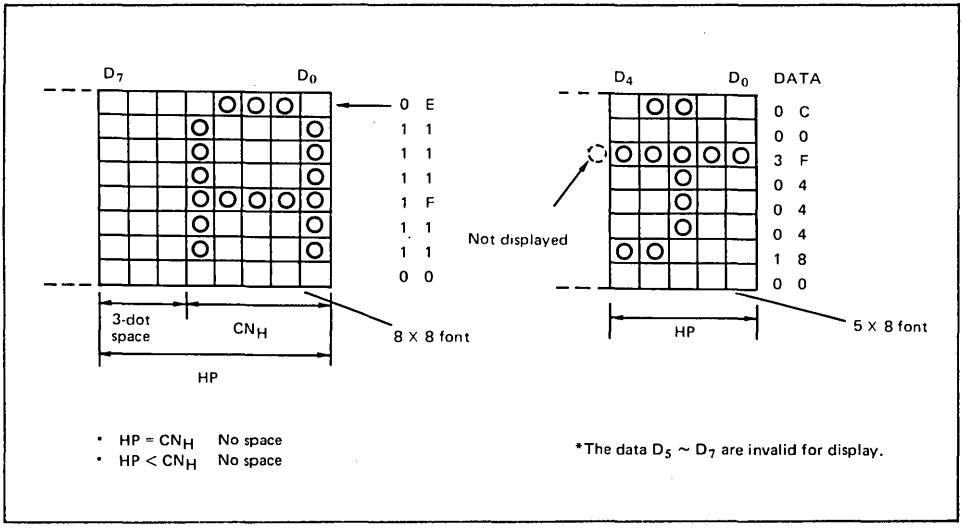
HP is determined by the logic levels of HS_2, HS_1 and HS_0.

HS_2	HS_1	HS_0	HP
L	L	L	5 dot
L	L	H	6
L	H	L	7
L	H	H	8
H	L	L	10
H	L	H	12
H	H	L	14
H	H	H	16

- **The horizontal space in a font**
  The horizontal space is determined by HP and number of horizontal dots/character (hereinafter called CN_H) in the character generator ROM.
  $HP > CN_H$ Space = $HP = CN_H$

(Example)
$HP = 8$ (HS_2 HS_1 HS_0:011)
$CN_H = 5$

(Example)
$HP = 5$ (HS_2 HS_1 HS_0:000)



- $HP = CN_H$ No space
- $HP < CN_H$ No space

*The data $D_5 \sim D_7$ are invalid for display.

- **The vertical space in a font**
  The vertical space is determined by VP and vertical dots/character (hereinafter called CN_V) in the character ROM.
  - $VP > CN_V$ Space = $VP - CN_V$
  - $VP = CN_V$ No space
  - $VP < CN_V$ No space

  The data whose number of bits are more than the number of HP are invalid for display.

2. Selection of Number of Characters

Number of characters controlled by MSM6240GS is determined by the logic levels of CS_0 and CS_1, as follows:

CS_1	L	L	H	H
CS_0	L	H	L	H
No. of characters	32	40	64	80

8(4 X 2) lines X 80 characters
This is the case when HP is 8 or less. When HP is 10 ~ 16, the display on the LCD panel becomes 8(4 X 2) lines X 40 characters.

(Note) When HP is set to 10, 12, 14 or 16, display of characters on the LCD panel is made by accessing twice to the character generator ROM.
The memory address signal, $MA_0 \sim MA_{10}$, to the LCD panel is addressed as shown in the table below.

000	001		04E	04F
050	051		09E	09F
0A0	0A1		0EE	0EF
0F0	0F1		13E	13F
000	001		04E	04F
050	051		09E	09F
0A0	0A1		0EE	0EF
0F0	0F1		13E	13F

MA_{11} = L

MA_{11} = H

0F0 means following data.

MA 10	9	8	7	6	5	4	3	2	1	0
L	L	L	H	H	H	H	L	L	L	L

3

3. Selection of Number of HP and Lines

S_3 S_2	S_1 S_0	VP	No. of lines	Number of characters/line								Duty
				HP is 10 ~ 16				HP is 8 or less				
L L	L L	8	4	80	64	40	32	80	64	40	32	1/32
L L	L H	8	6	80	64	40	32	80	64	40	32	1/48
L L	H L	8	8	80	64	40	32	80	64	40	32	1/64
L L	H H	8	12	80	64	40	32	80	64	40	32	1/96
H H	H H	8	16	(80)	64	40	32	80	64	40	32	1/128
L H	L L	12	4	80	64	40	32	80	64	40	32	1/48
L H	H L	12	8	80	64	40	32	80	64	40	32	1/96
H L	L L	18	4	80	64	40	32	80	64	40	32	1/72
H L	L H	18	6	80	64	40	32	80	64	40	32	1/108
H L	H L	18	8	80	64	40	32	80	64	40	32	1/144
H H	L L	20	4	80	64	40	32	80	64	40	32	1/80

*Number of lines on above table is half of the actual number of lines on the LCD panel.
When all of $S_3 \sim S_0$ are set at high level (which means HP is 16 and number of characters/line is 80), the display on the LCD panel becomes as shown below because the capacity of the display RAM overflows.

HP = 8
Number of lines = 12
VP = 16
Number of characters/line = 80

4. Attribute Function

This function is determined by the data of the external attribute RAM. The attribute function per font is available.

- **Character Display, Blink**

DAEN	CHBL	Display
L	L	Blink
L	H	Blink
H	L	Display
H	H	$\overline{\text{Blink}}$

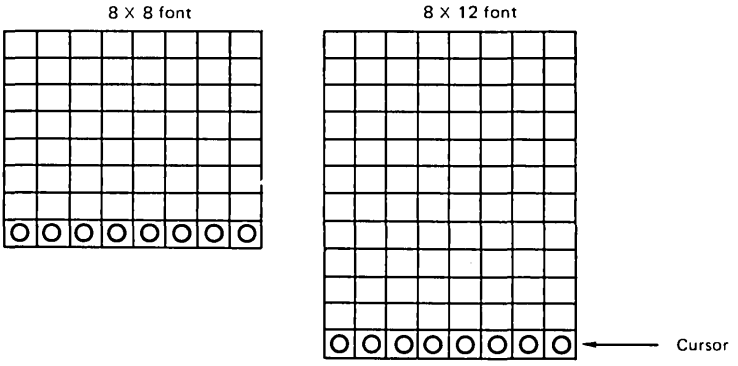
- **Cursor Display and Blink**

UDBL	CSEN	UDEN	Cursor Display
L	L	L	None
L	L	H	None
L	H	L	None
L	H	H	Cursor display
H	L	L	None
H	L	H	None
H	H	L	Cursor blink
H	H	H	$\overline{\text{Cursor blink}}$*

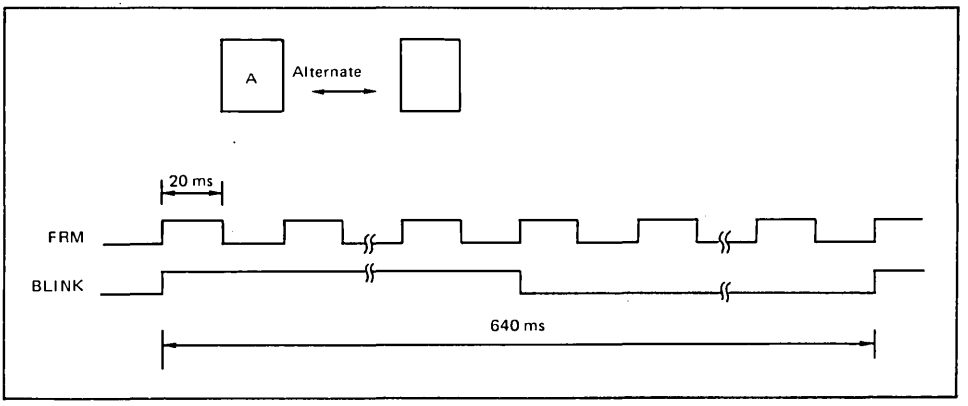
*The character and cursor blink alternately.

- **Cursor display position**
  Cursor is displayed in the bottom line of the font. The number of horizontal dots/font is same as that of HP.

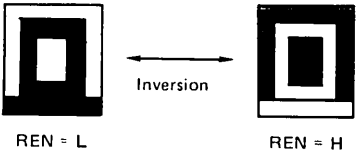
  (Example)



- **Blink**
  The blink cycle is 640 ms (FRP = 50 Hz) and is cynchronized to FRM signal.



- **Display inversion**

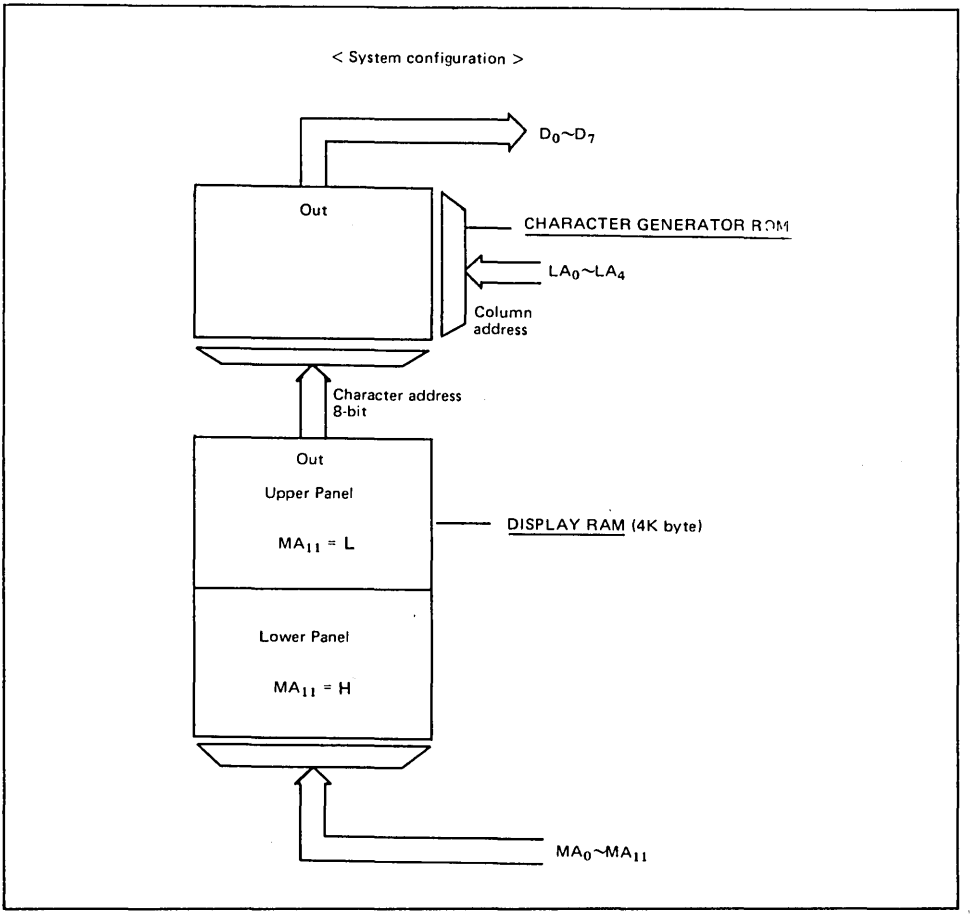


The display of character and cursor is inverted.

5. Display RAM (2K bytes)

The MSM6240GS is applicable to both character mode and graphic mode, which is only determined by system configuration, not by software.

- **When using Display RAM in the character mode**



The character code is programmed in the Display RAM in 8-bit configuration. The data of Display RAM is converted to the data necessary to display a character on the LCD, and is input to D_0 ~ D_7, display data input, of the MSM6240GS.

The MSM6240GS is capable of controlling 4,096 characters maximum, however, this capacity is affected, as is shown on the Sec. 13, by the LCD drivers speed.

- **Relationship between $LA_0 \sim LA_4$ and VP**
  $LA_0 \sim LA_4$ are valid for octal, duodecimal, octdicimal and vigesimal signals.

VP = 8

LA_2	LA_1	LA_0
L	L	L
L	L	H
L	H	L
L	H	H
H	L	L
H	L	H
H	H	L
H	H	H

VP = 12

LA_3	LA_2	LA_1	LA_0
L	L	L	L
L	L	L	H
L	L	H	L
L	L	H	H
L	H	L	L
L	H	L	H
L	H	H	L
L	H	H	H
H	L	L	L
H	L	L	H
H	L	H	L
H	L	H	H

VP = 18

LA_4	LA_3	LA_2	LA_1	LA_0
L	L	L	L	L
L	L	L	L	H
L	L	L	H	L
L	L	L	H	H
L	L	H	L	L
L	L	H	L	H
L	L	H	H	L
L	L	H	H	H
L	H	L	L	L
L	H	L	L	H
L	H	L	H	L
L	H	L	H	H
L	H	H	L	L
L	H	H	L	H
L	H	H	H	L
L	H	H	H	H
H	L	L	L	L

VP = 20

LA_4	LA_3	LA_2	LA_1	LA_0
L	L	L	L	L
L	L	L	L	H
L	L	L	H	L
L	L	L	H	H
L	L	H	L	L
L	L	H	L	H
L	L	H	H	L
L	L	H	H	H
L	H	L	L	L
L	H	L	L	H
L	H	L	H	L
L	H	L	H	H
L	H	H	L	L
L	H	H	L	H
L	H	H	H	L
L	H	H	H	H
H	L	L	L	L
H	L	L	L	H
H	L	L	H	L
H	L	L	H	H

- **Limitation of No. of characters and No. of lines**
  The No. of characters and the No. of lines are subject to limitation according to the RAM capacity.

When HP is set at 8 or less

No.	No. of characters/line	No. of lines	Display RAM area
1	80	16	000 ~ 4FF (H)
2	64	16	000 ~ 3FF (H)
3	40	16	000 ~ 27F (H)
4	32	16	000 ~ 1FF (H)

When HP is set at 10 ~ 16

No.	No. of characters/line	No. of lines	Display RAM area
5	80	12	000 ~ 77F (H)
6	64	16	000 ~ 7FF (H)
7	40	16	000 ~ 4FF (H)
8	32	16	000 ~ 3FF (H)

(Note) Number of lines on above table is half of the actual number of lines on the LCD panel.

(Example) RAM area 000 ~ 3BF

Memory address	MA_{11}	MA_{10}	MA_9	MA_8	MA_7	MA_6	MA_5	MA_4	MA_3	MA_2	MA_1	MA_0
Start address	L	L	L	L	L	L	L	L	L	L	L	L
End address	L	L	H	H	H	L	H	H	H	H	H	H
Start address	H	L	L	L	L	L	L	L	L	L	L	L
End address	H	L	H	H	H	L	H	H	H	H	H	H

Set HP at 8 or less

No. 1 In the case of 80 characters/line (Number of lines: 16 lines max.)

000	001	002	003		04E	04F
050	051	052	053		09E	09F
0A0	0A1	0A2	0A3		0EE	0EF
0F0	0F1	0F2	0F3		13E	13F
140	141	142	143		18E	18F
190	191	192	193		1DE	1DF
1E0	1E1	1E2	1E3		22E	22F
230	231	232	233		27E	27F
280	281	282	283		2CE	2CF
2D0	2D1	2D2	2D3		31E	31F
320	321	322	323		36E	36F
370	371	372	373		3BE	3BF
3C0	3C1	3C2	3C3		40E	40F
410	411	412	413		45E	45F
400	401	402	403		4AE	4AF
4B0	4B1	4B2	4B3		4FE	4FE

The table above shows the memory address to the LCD panel.
It only shows the address to the upper part of the LCD panel. Whether it be the upper or lower will be determined by the H/L condition of MA_{11}.

No. 2 In the case of 64 characters/line (Number of lines: 16 lines max.)

000	001	002	003		03E	03F
040	041	042	043		07E	07F
080	081	082	083		0BE	0BF
0C0	0C1	0C2	0C3		0FE	0FF
100	101	102	103		13E	13F
140	141	142	143		17E	17F
180	181	182	183		1BE	1BF
1C0	1C1	1C2	1C3		1FE	1FF
200	201	202	203		23E	23F
240	241	242	243		27E	27F
280	281	282	283		2BE	2BF
2C0	2C1	2C2	2C3		2FE	2FF
300	301	302	303		33E	33F
340	341	342	343		37E	37F
380	381	382	383		3BE	3BF
3C0	3C1	3C2	3C3		3FE	3FF

The table above shows the memory address to the LCD panel.
It only shows the address to the upper part of the LCD panel. Whether it be the upper or lower will be determined by the H/L condition of MA_{11}.

No. 3 In the case of 40 characters/line (Number of lines: 16 lines max.)

000	001	002	003		026	027
028	029	02A	02B		04E	04F
050	051	052	053		076	077
078	079	07A	07B		09E	09F
0A0	0A1	0A2	0A3		0C6	0C7
0C8	0C9	0CA	0CB		0EE	0EF
0F0	0F1	0F2	0F3		116	117
118	119	11A	11V		13E	13F
140	141	142	143		166	167
168	169	16A	16B		18E	18F
190	191	192	193		1B6	1B7
1B8	1B9	1BA	1BB		1DE	1DF
1E0	1E1	1E2	1E3		206	207
208	209	20A	20B		22E	22F
230	231	232	233		256	257
258	259	25A	25B		27E	27F

The table above shows the memory address to the LCD panel.
It only shows the address to the upper part of the LCD panel. Whether it be the upper or lower will be determined by the H/L condition of MA_{11}.

No. 4 In the case of 32 characters/line (Number of lines: 16 lines max.)

000	001	002	003		01E	01F
020	021	022	023		03E	03F
040	041	042	043		05E	05F
060	061	062	063		07E	07F
080	081	082	083		09E	09F
0A0	0A1	0A2	0A3		0BE	0BF
0C0	0C1	0C2	0C3		0DE	0DF
0E0	0E1	0E2	0E3		0FE	0FF
100	101	102	103		11E	11F
120	121	122	123		13E	13F
140	141	142	143		15E	15F
160	161	162	163		17E	17F
180	181	182	183		19E	19F
1A0	1A1	1A2	1A3		1BE	1BF
1C0	1C1	1C2	1C3		1DE	1DF
1E0	1E1	1E2	1E3		1FE	1FF

The table above shows the memory address to the LCD panel.
It only shows the address to the upper part of the LCD panel. Whether it be the upper or lower will be determined by the H/L condition of MA_{11}.

Set HP at 10 ~ 16

No. 5 In the case of 80 characters/line (Number of lines: 12 lines max.)

000	001	002	003		09E	09F
0A0	0A1	0A2	0A3		13E	13F
140	141	142	143		1DE	1DF
1E0	1E1	1E2	1E3		27E	27F
280	281	282	283		31E	31F
320	321	322	323		3BE	3BF
3C0	3C1	3C2	3C3		45E	45F
460	461	462	463		4FE	4FF
500	501	502	503		59E	59F
5A0	5A1	5A2	5A3		63E	63F
640	641	642	643		6DE	6DF
6E0	6E1	6E2	6E3		77E	77F

The table above shows the memory address to the LCD panel.
It only shows the address to the upper part of the LCD panel. Whether it be the upper or lower will be determined by the H/L condition of MA_{11}.

No. 6 In the case of 64 characters/line (Number of lines: 16 lines max.)

000	001	002	003		07E	07F
080	081	082	083		0FE	0FF
100	101	102	103		17E	17F
180	181	182	183		1FE	1FF
200	201	202	203		27E	27F
280	281	282	283		2FE	2FF
300	301	302	303		37E	37F
380	381	382	383		3FE	3FF
400	401	402	403		47E	47F
480	481	482	483		4FE	4FF
500	501	502	503		57E	57F
580	581	582	583		5FE	5FF
600	601	602	603		67E	67F
680	681	682	683		6FE	6FF
700	701	702	703		77E	77F
780	781	782	783		7FE	7FF

The table above shows the memory address to the LCD panel.
It only shows the address to the upper part of the LCD panel. Whether it be the upper or lower will be determined by the H/L condition of MA_{11}.

No. 7 In the case of 40 characters/line (Number of lines: 16 lines max.)

000	001	002	003		04E	04F
050	051	052	053		09E	09F
0A0	0A1	0A2	0A3		0EE	0EF
0F0	0F1	0F2	0F3		13E	13F
140	141	142	143		18E	18F
190	191	192	193		1DE	1DF
1E0	1E1	1E2	1E3		22E	22F
230	231	232	233		27E	27F
280	281	282	283		2CE	2CF
2D0	2D1	2D2	2D3		31E	31F
320	321	322	323		36E	36F
370	371	372	373		3BE	3BF
3C0	3C1	3C2	3C3		40E	40F
410	411	412	413		45E	45F
460	461	462	463		4AE	4AF
4B0	4B1	4B2	4B3		4FE	4FF

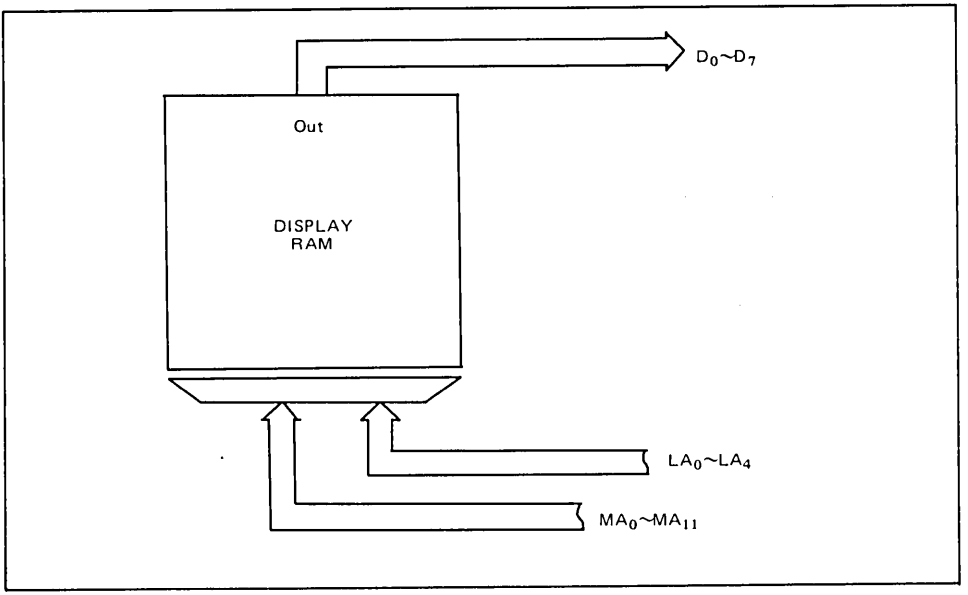
The table above shows the memoray address to the LCD panel.
It only shows the address to the upper part of the LCD panel. Whether it be the upper or lower will be determined by the H/L condition of MA_{11}.

No. 8 In the case of 32 characters/line (Number of lines: 16 lines max.)

000	001	002	003		03E	03F
040	041	042	043		07E	07F
080	081	082	083		0BE	0BF
0C0	0C1	0C2	0C3		0FE	0FF
100	101	102	103		13E	13F
140	141	142	143		17E	17F
180	181	182	183		1BE	1BF
1C0	1C1	1C2	1C3		1FE	1FF
200	201	202	203		23E	23F
240	241	242	243		27E	27F
280	281	282	283		2BE	2BF
2C0	2C1	2C2	2C3		2FE	2FF
300	301	302	303		33E	33F
340	341	342	343		37E	37F
380	381	382	383		3BE	3BF
3C0	3C1	3C2	3C3		3FE	3FF

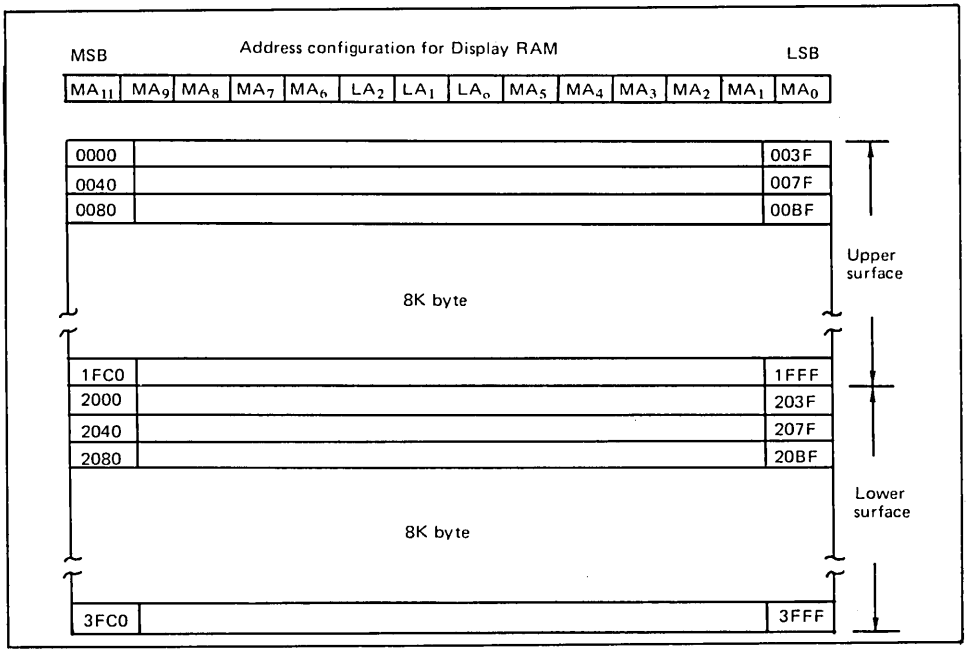
The table above shows the memory address to the LCD panel.
It only shows the address to the upper part of the LCD panel. Whether it be the upper or lower will be determined by the H/L condition of MA_{11}.

● When using Display RAM in the graph mode



(Note) The cursor display should not be used by setting CSEN at L.

(Example)HP = 8, VP = 8, 64 characters/line, 16 lines



6. Dien Signal

Before writing the data into DISPLAY RAM or ATTRIBUTE RAM, DIEN signal should be set at L.

7. Memory Chip Enable Signal (MCE)

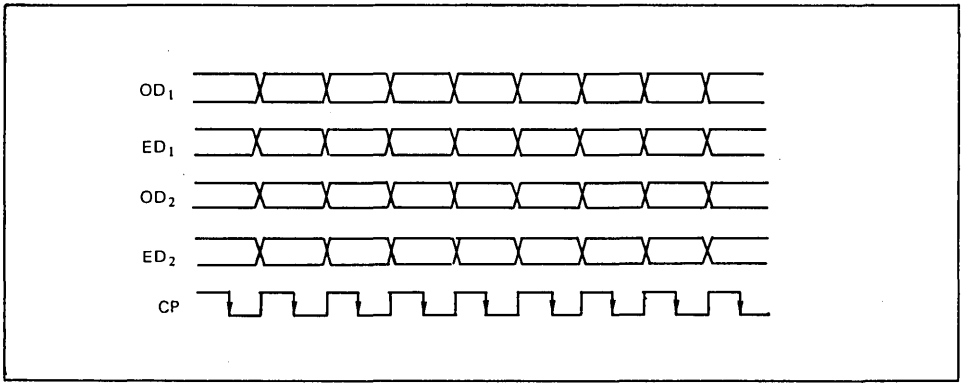
Normally this signal is set at L. This signal becomes H when BUSY signal or DIEN signal become L, which reduces the current consumption of the external RAM by half.

8. ODD/EVEN Number Data Processing

When OEEN is set at H, ODD/EVEN number data processing is proceeded.

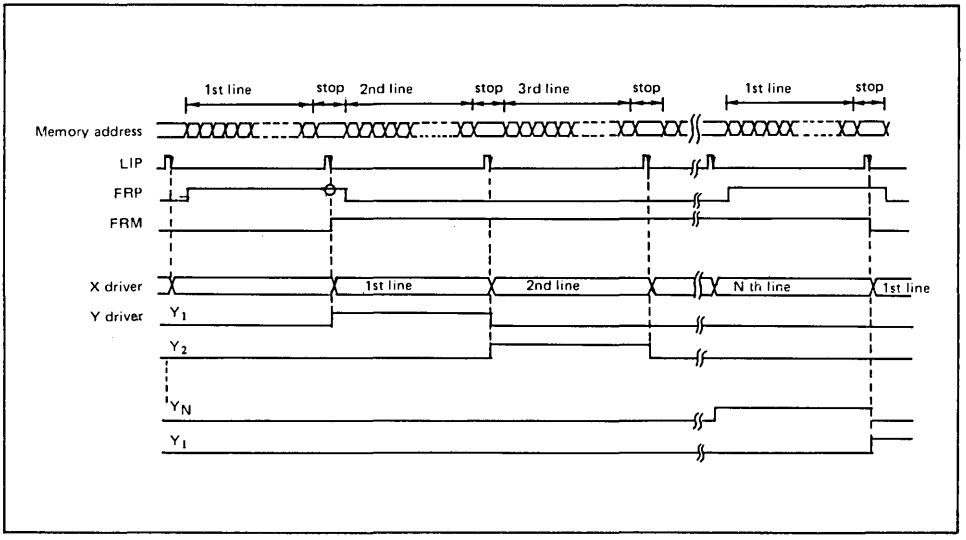
The purpose of ODD/EVEN number data processing is to reduce the shift pulse "CP" speed by half. When MSM6240 is applied to wide LCD's control, the speed of shift pulse becomes high and it exceeds the maximum clock frequency of the LCD drivers, so, to reduce the shift pulse speed is required. When OEEN is set at L, ODD/EVEN number data processing is not proceeded.

OEEN may set at L only when HP is set at 8 or less. In this case, the data is sent to OD_1 (upper part) and OD_2 (lower part).



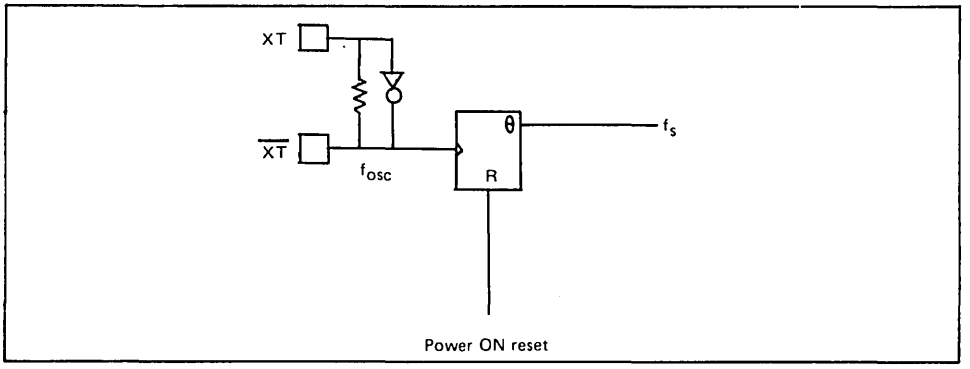
9. Frame Pulse, Frame, Latch

- **Time chart**



The proper FRP frequency is 50 to 70 Hz. f_{osc} must be calculated so that it might match with FRP frequency.

10. X'TAL Oscillation



The frequency of the crystal is calculated by following formula.

- HP is 8 or less
  f_{osc} = (Number of characters + 8) X HP X 1/duty X FRP X 2

HP is 10 ~ 16
f_{osc} = (Number of characters X 2 + 16) X 8 X 1/duty X FRP X 2

11. X'TAL Oscillation Frequency Table

HP = 8, FRP = 50 ~ 70 Hz

No. of characters / Duty	32	40	64	80
1/128	4.1 ~ 5.7	4.9 ~ 6.9	7.4 ~ 10.3	9.0 ~ 12.6
1/96	3.1 ~ 4.3	3.7 ~ 5.2	5.5 ~ 7.7	6.8 ~ 9.5
1/64	2.0 ~ 2.9	2.5 ~ 3.5	3.7 ~ 5.18	4.5 ~ 6.3
1/48	1.5 ~ 2.1	1.8 ~ 2.5	2.8 ~ 3.9	3.4 ~ 4.8

HP = 7, FRP = 50 ~ 70 Hz

No. of characters / Duty	32	40	64	80
1/128	3.6 ~ 5.0	4.3 ~ 6.0	6.5 ~ 9.1	7.9 ~ 11.1
1/96	2.7 ~ 3.8	3.2 ~ 4.5	4.8 ~ 6.7	5.9 ~ 8.3
1/64	1.7 ~ 2.5	2.2 ~ 3.1	3.2 ~ 4.5	3.9 ~ 5.5
1/48	1.3 ~ 1.8	1.6 ~ 2.2	2.5 ~ 3.5	3.0 ~ 4.2

HP = 6, FRP = 50 ~ 70 Hz

Duty \ No. of characters	32	40	64	80
1/128	3.1 ~ 4.3	3.7 ~ 5.2	5.6 ~ 7.8	6.8 ~ 9.5
1/96	2.3 ~ 3.2	2.8 ~ 3.9	4.1 ~ 5.7	5.1 ~ 7.1
1/64	1.5 ~ 2.1	1.9 ~ 2.7	2.8 ~ 3.9	3.4 ~ 4.8
1/48	1.1 ~ 1.5	1.4 ~ 2.0	2.1 ~ 2.9	2.6 ~ 3.6

HP = 5, FRP = 50 ~ 70 Hz

Duty \ No. of characters	32	40	64	80
1/128	2.6 ~ 3.6	3.1 ~ 4.3	4.6 ~ 6.4	5.6 ~ 7.8
1/96	1.9 ~ 2.7	2.3 ~ 3.2	3.4 ~ 4.8	4.3 ~ 6.0
1/64	1.3 ~ 1.8	1.6 ~ 2.2	2.3 ~ 3.2	2.8 ~ 3.9
1/48	0.9 ~ 1.3	1.1 ~ 1.5	1.8 ~ 2.5	2.1 ~ 2.9

HP = 10 ~ 16, FRP = 50 ~ 70 Hz

Duty \ No. of characters	32	40	64	80
1/128	8.2 ~ 11.5	9.8 ~ 13.7	14.7 ~ 20.6	18.0 ~ 25.2
1/96	6.1 ~ 8.5	7.4 ~ 10.4	11.1 ~ 15.5	13.5 ~ 18.9
1/64	4.1 ~ 5.7	4.9 ~ 6.9	7.4 ~ 10.3	9.0 ~ 12.6
1/48	3.1 ~ 4.3	3.7 ~ 5.2	5.5 ~ 7.7	6.8 ~ 9.5

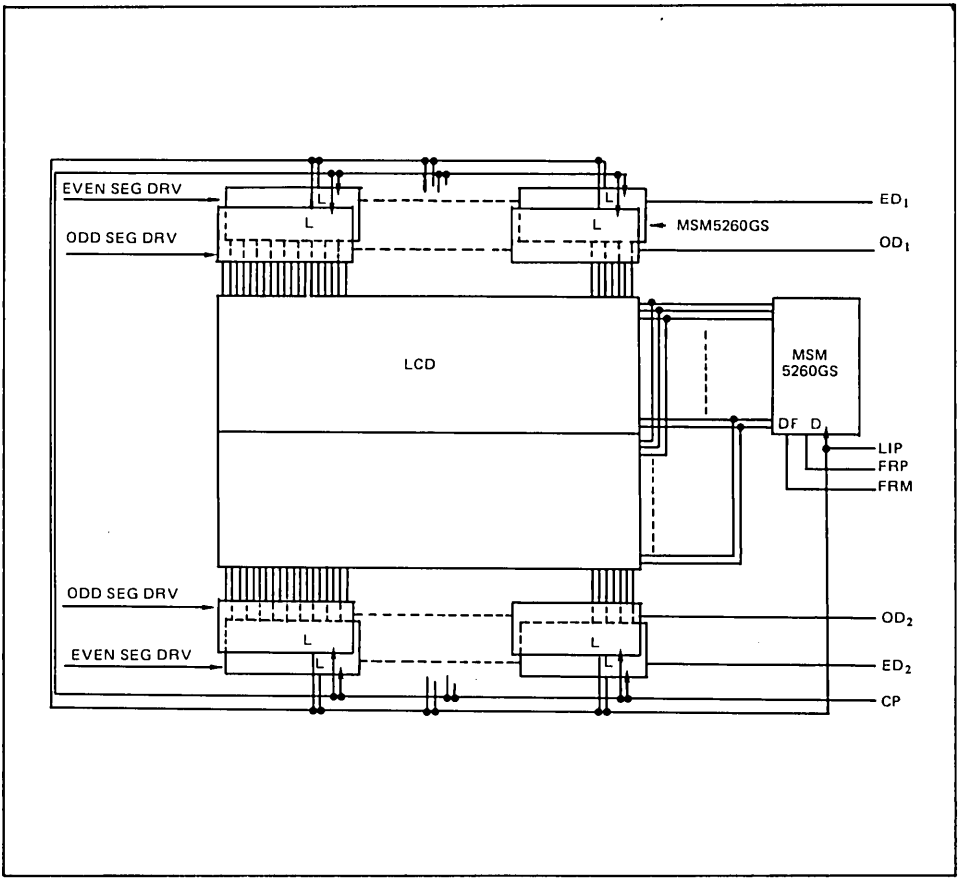
The value on above tables are affected by the maximum frequency of LCD driver's shift clock input and an maximum frequency of f_{osc}.
The relation between f_{osc} and shift clock is as follows.

- When ODD/EVEN data processing is proceeded
  $CP = f_{osc}/4$
- When ODD/EVEN data processing is not proceeded
  $CP = f_{osc}/2$

For example, the f_{osc} is limited as follows when MSM5260GS, whose maximum frequency of shift pulse is 3.3 MHz, is connected to MSM6240GS.

- When ODD/EVEN data processing is proceeded
  $f_{osc} \leq 10$ MHz
- When ODD/EVEN data processing is not proceeded
  $f_{osc} \leq 6.6$ MHz

TYPICAL SYSTEM CONFIGURATION



OKI semiconductor

MSM6255GS

DOT MATRIX LCD CONTROLLER

3

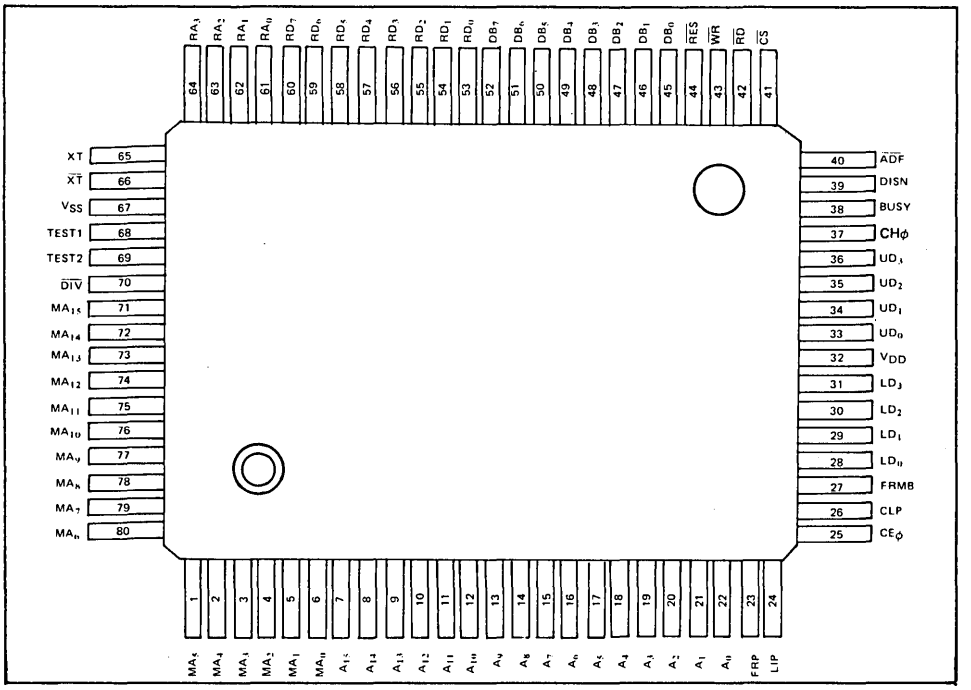
GENERAL DESCRIPTION

The OKI MSM6255GS is a CMOS Si-gate LSI designed for use in controlling large size of DOT MATRIX LCD panels in characters and graphics.

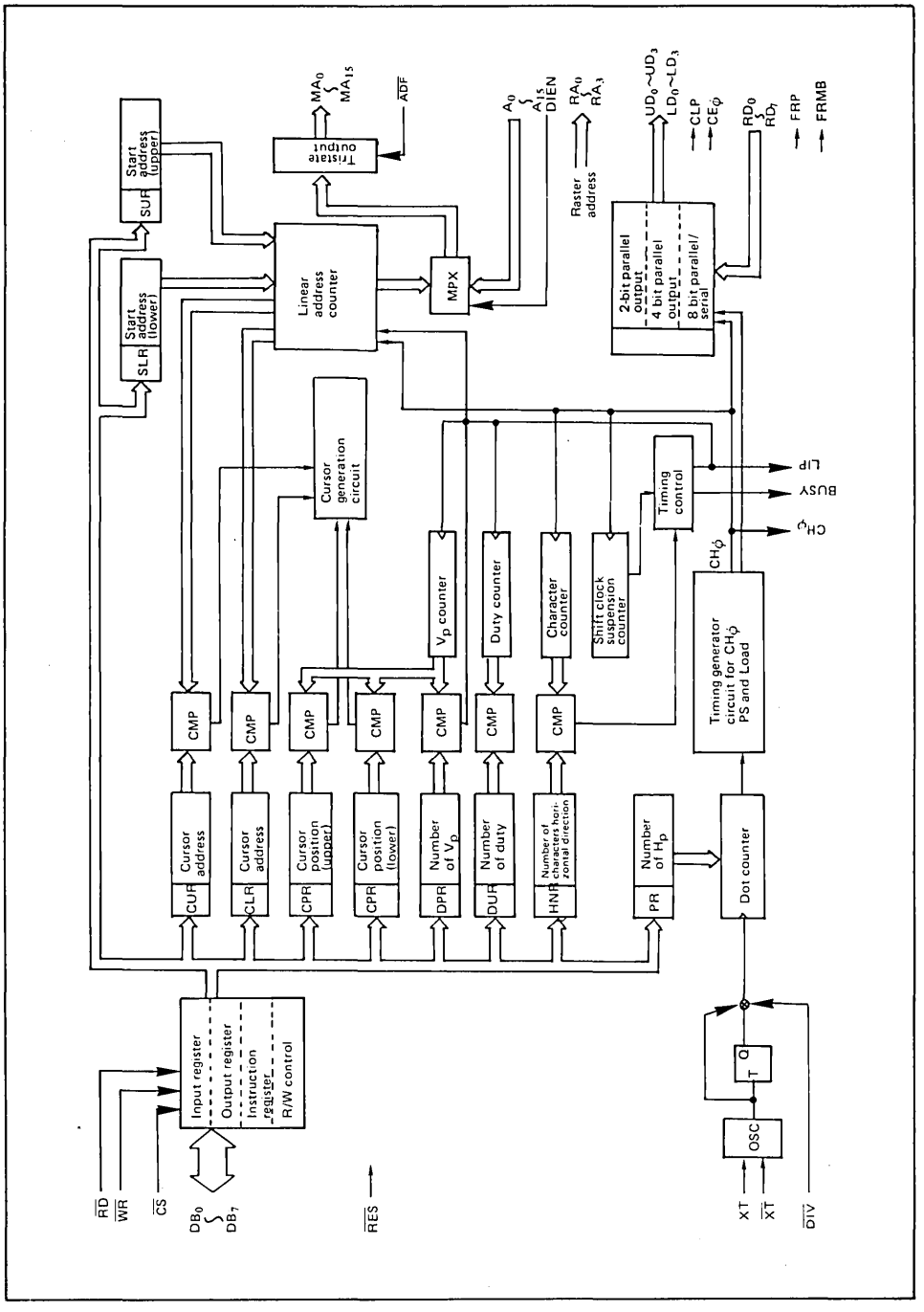
FEATURES

- Display control capacity
  - Graphic mode: 512,000 dots (2^{16} bytes)
    Memory address $MA_0 \sim MA_{15}$
  - Character mode: 65,536 characters (2^{16} bytes)
    Display address $MA_0 \sim MA_{15}$
- Direct interface with 8085 or Z80 CPU
- Duty: 1/2 to 1/256 selectable
- Attribute
  - Screen clear
  - Cursor ON/OFF/blink
- Scrolling and paging
- Display system: AC inversion at each frame
- Data output (upper and lower display outputs)
  4-bit parallel output, 2-bit parallel output
  1-bit serial output
- Crystal oscillation
- Low C-MOS Silicon gate process
- Single +5V power supply
- 80-pin flat package

PIN CONFIGURATION



BLOCK DIAGRAM



3

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating value	Unit
Supply voltage	V_{DD}	T_a = 25°C	−0.3 ~ 6	V
Input voltage	V_{IN}	T_a = 25°C	−0.3 ~ V_{DD}	V
Storage temperature	T_{stg}	—	−50 ~ 150	°C

OPERATING RANGE

Parameter	Symbol	Condition	Range	Unit
Supply voltage	V_{DD}	—	4.5 ~ 5.5	V
Operating temperature	T_{op}	—	−20 ~ 85	°C
Operating frequency	f_{osc}	V_{DD} = 5V ± 10%	0 ~ 11	MHz

INPUT CHARACTERISTICS

(V_{DD} = 5V ± 5%, T_a = −20 ~ 85°C)

Parameter	Symbol	MIN	TYP	MAX	Unit	Applicable terminal
"H" input voltage	V_{IH}	2.4	—	—	V	DB_0 ~ DB_7, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A_0 ~ A_{15}, DIEN, ADF, RD_0 ~ RD_7
"L" input voltage	V_{IL}	—	—	0.7	V	
"H" input voltage	V_{IH}	4.5	—	—	V	$\overline{RES}$, $\overline{DIV}$, XT
"L" input voltage	V_{IL}	—	—	1.0	V	
"H" input voltage	I_{IH}	—	—	1	μA	DB_0 ~ DB_7, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ A_0 ~ A_{15}, DIEN, $\overline{ADF}$ RD_0 ~ RD_7, $\overline{RES}$, $\overline{DIV}$
"L" input voltage	I_{IL}	—	—	−1	μA	
"H" input voltage	I_{IH}	—	—	250	μA	TEST1, TEST2
"L" input voltage	I_{IL}	—	—	−1	μA	

OUTPUT CHARACTERISTICS

(V_{DD} = 5V ± 5%, T_a = −20 ~ 85°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Applicable terminal
"H" output current	I_{OH}	V_{OH} = 2.8V	−500	—	—	μA	LD_0 ~ LD_3, UD_0 ~ UD_3, MA_0 ~ MA_{15}, RA_0 ~ RA_3, CH_ϕ, CE_ϕ, LIP, FRP, FRMB, BUSY, CLP, DB_0 ~ DB_7
"L" output current	I_{OL}	V_{OL} = 0.4V	2.4	—	—	mA	

CURRENT CONSUMPTION

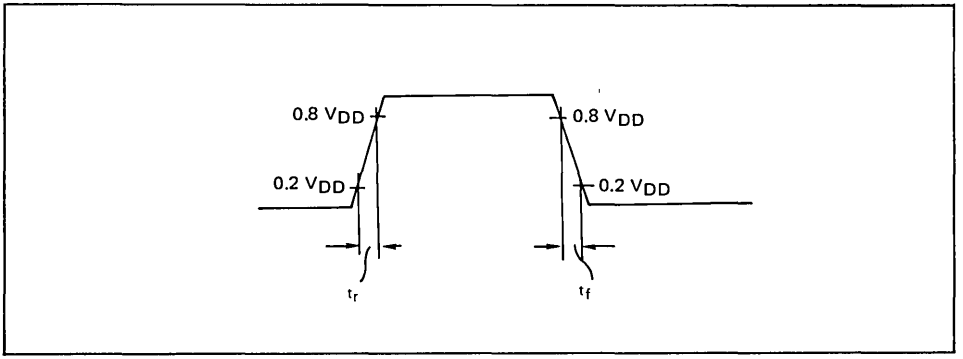
(V_{DD} = 5V ± 5%, T_a = –20 ~ 85°C)

Parameter	Symbol	V_{DD}	Condition	MIN	TYP	MAX	Unit
Static current	I_{DDS}	5	f_{osc} = 0 Hz, No load	–	–	50	μA
Dynamic current	I_{DD}	5	f_{osc} = 10 MHz, No load	–	–	15	mA

Note: TEST1 and TEST2 are open, and other inputs are either V_{DD} or GND.

3

SWITCHING CHARACTERISTICS



(V_{DD} = 5V ± 5%, T_a = –20 ~ 85°C)

Parameters	Symbol	Load condition	MIN	TYP	MAX	Unit	Applicable terminals
Rising time	t_r	60 pF	–	–	100	ns	All output terminals
Falling time	t_f	60 pF	–	–	100	ns	

MAXIMUM OPERATING FREQUENCY

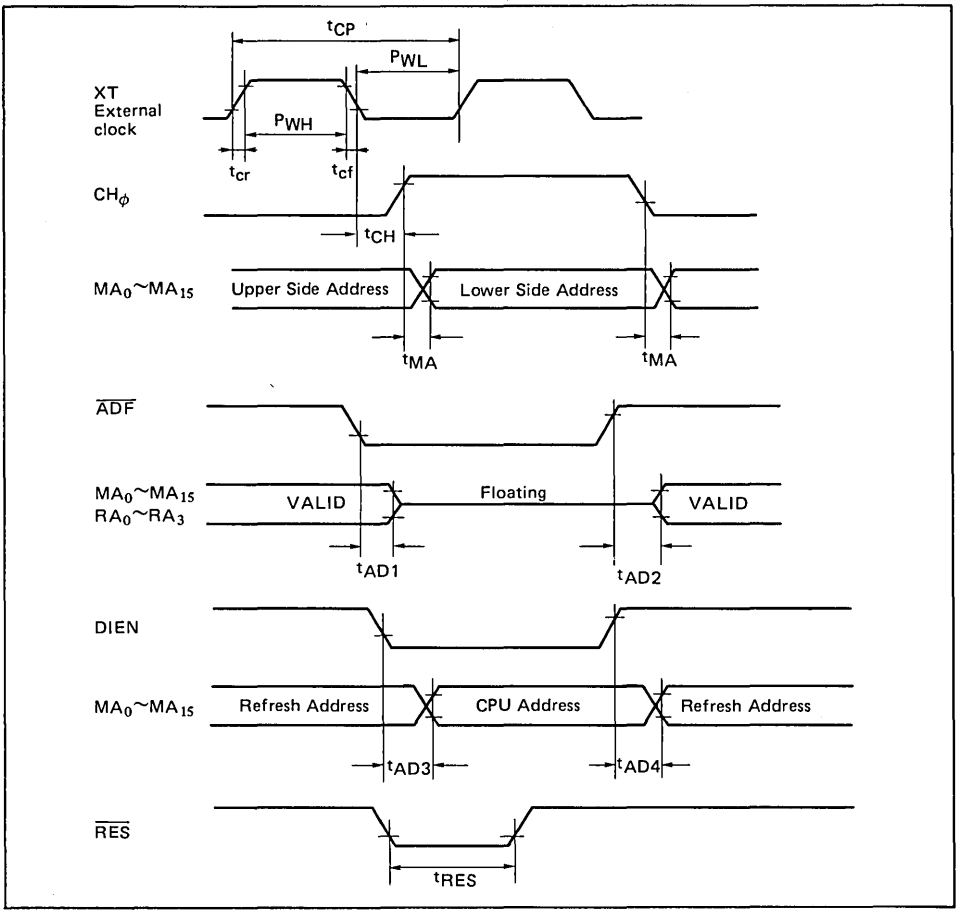
(V_{DD} = 5V ± 5%, T_a = –20 ~ 85°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Notes
Oscillating frequency	f_{osc}	$\overline{DIV}$ = "L"	11	–	–	MHz	Crystal oscillator
Basic clock frequency	f_s	$\overline{DIV}$ = "H"	5.5	–	–	MHz	External clock

LCDC CONTROL SIGNAL TIMING CHARACTERISTICS

(C_L = 30pF, V_{DD} = 5V ±5%, T_a = −20 ~ 85°C)

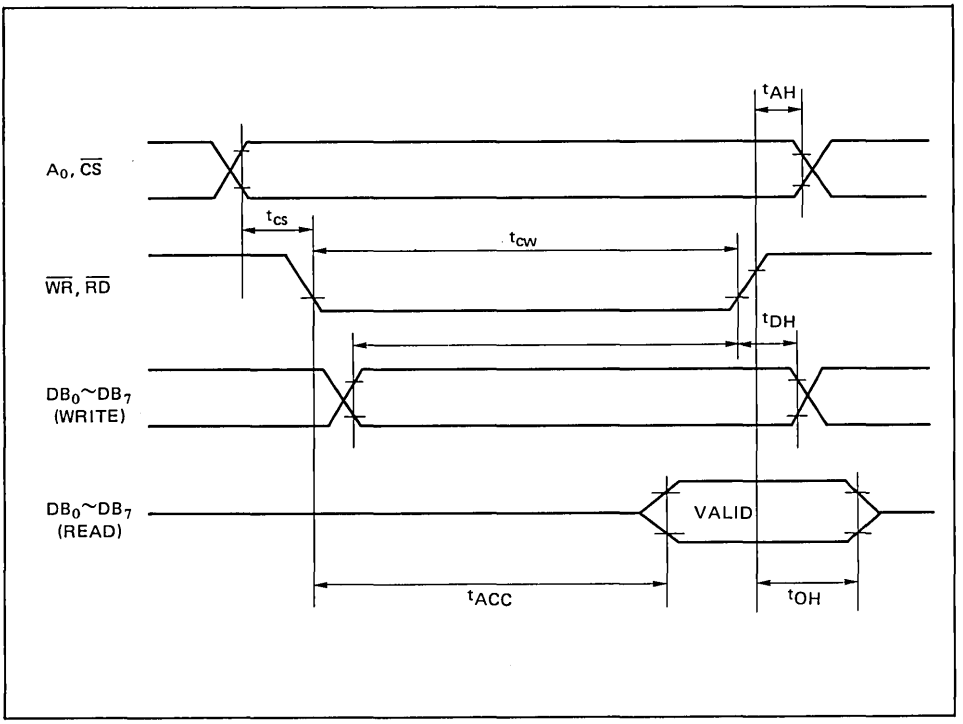
Parameter	Symbol	MIN	TYP	MAX	Unit
Clock cycle time	t_{CP}	180	–	–	ns
Clock "H" level pulse width	P_{WH}	80	–	–	ns
Clock "L" level pulse width	P_{WL}	80	–	–	ns
Clock rising/falling time	t_{cr}/t_{cf}	–	–	20	ns
Character clock delay time	t_{CH}	–	–	200	ns
Memory address clock delay time	t_{MA}	–	–	100	ns
Memory address disable delay time	t_{AD1}	–	–	40	ns
Memory address enable delay time	t_{AD2}	–	–	40	ns
CPU address delay time	t_{AD3}	–	–	100	ns
Refresh address delay time	t_{AD4}	–	–	100	ns
Reset "H" level pulse width	t_{RES}	1	–	–	μs



BUS TIMING CHARACTERISTICS

(C_L = 50pF, V_{DD} = 5V ± 5%, T_a = −20 ~ 85°C)

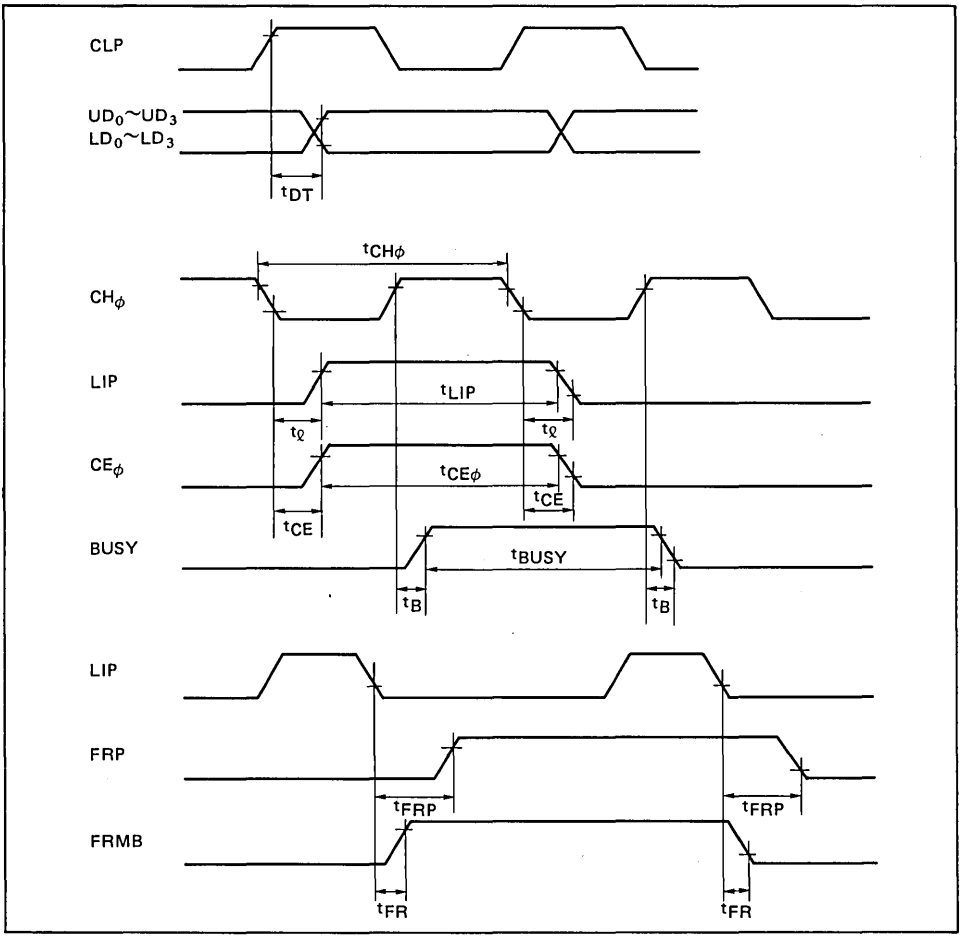
Parameter	Symbol	MIN	TYP	MAX	Unit
A_0, CS Set up time	t_{CS}	100	–	–	ns
$\overline{RD}$, $\overline{WR}$ Pulse width	t_{CW}	300	–	–	ns
Address hold time	t_{AH}	40	–	–	ns
Data set-up time	t_{DS}	200	–	–	ns
Data hold time	t_{DH}	40	–	–	ns
Output disable time	t_{OH}	0	–	40	ns
Access time	t_{ACC}	–	–	200	ns



LCD DRIVER INTERFACE TIMING CHARACTERISTICS

(C_L = 30pF, V_{DD} = 5V ± 5%, T_a = −20 ~ +85°C)

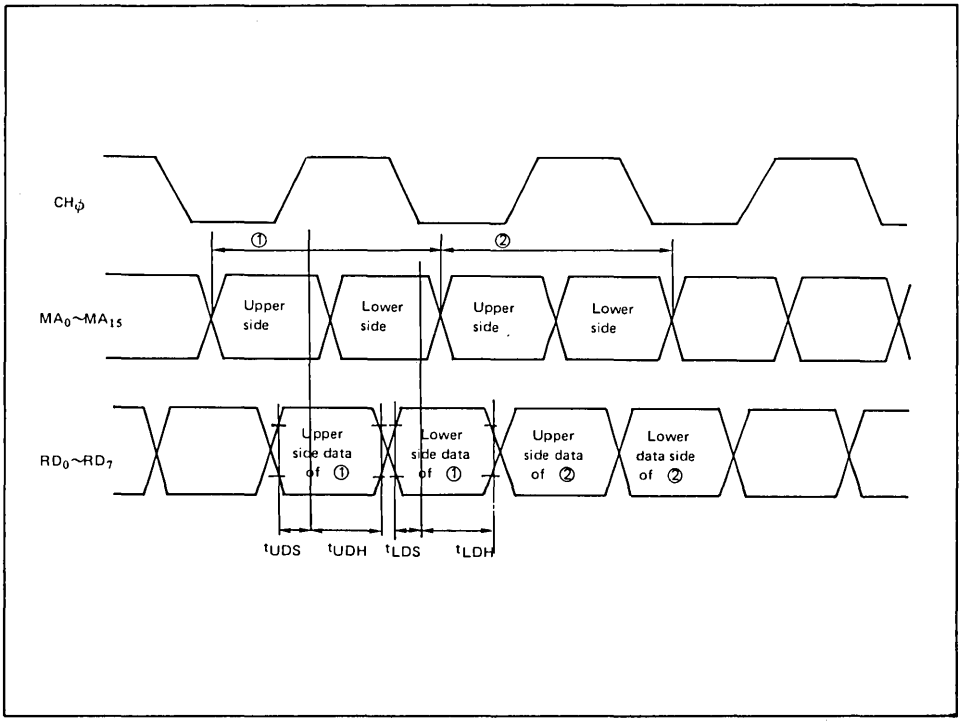
Parameter	Symbol	MIN	TYP	MAX	Unit
Data delay time	t_{DA}	–	–	100	ns
1 Character cycle time	$t_{CH\phi}$	730	–	–	ns
Latch signal delay time	t_{ℓ}	–	–	200	ns
Latch signal "H" time	t_{LIP}	1.46	–	–	ns
Chip enable clock delay time	t_{CE}	–	–	200	ns
Chip enable clock "H" time	$t_{CE\phi}$	730	–	–	ns
Ready signal delay time	t_B	–	–	200	ns
Ready signal "H" time	t_{BUSY}	5.11	–	–	μs
Frame signal delay time	t_{FRP}	$2t_{CH\phi}$	–	$2t_{CH\phi}$ +200	ns
Alternating frame signal delay time	t_{FR}	–	–	200	ns



TIMING FOR FETCHING PATTERN DATA

(V_{DD} = 5V ± 5%, T_a = −20 ~ 85°C)

Parameter	Symbol	MIN	TYP	MAX	Unit
Upper side data set-up time	t_{UDS}	120	–	–	ns
Upper side data hold time	t_{UDH}	40	–	–	ns
Lower side data set-up time	t_{LDS}	120	–	–	ns
Lower side data hold time	t_{LDH}	40	–	–	ns



PIN DESCRIPTION

Terminal No.	Terminal name	I/$\overline{O}$/Z	Function
1 ~ 6 71 ~ 80	MA_0 ∫ MA_{15}	$\overline{O}$/Z	Address output for displaying RAM.
7 ∫ 22	A_0 ∫ A_{15}	I	Memory address input terminals.
23	FRP	$\overline{O}$	Frame signal . . . . Synchronization of display
24	LIP	$\overline{O}$	Display data latch signal
25	$CE\phi$	$\overline{O}$	Chip enable clock for LCD segment driver.
26	CLP	$\overline{O}$	Display data shift clock
27	FRMB	$\overline{O}$	AC signal
28 ∫ 31	LD_0 ∫ LD_3	$\overline{O}$	Display data parallel output for lower side.
32	V_{DD}		Supply voltage
33 ∫ 36	UD_0 ∫ UD_3	$\overline{O}$	Display data parallel output, Upper display 4-bit output (OD1, ED1, OD2 and ED2 outputs)
37	$CH\phi$	$\overline{O}$	Character clock
38	Busy	$\overline{O}$	Ready state signal. This signal is used while serial transmission stops.
39	DIEN	I	Display enable signal. When this signal is H, display is enabled.
40	$\overline{ADF}$	I	Address floating input. When this signal is L, MA_0~MA_{15} RA_0~RA_3 are high impedance. Whereas, it is H, A_0~A_{15} or a refresh address is output to MA_0~MA_{15}.
41	$\overline{CS}$	I	Chip select.
42	$\overline{RD}$	I	Read . . . . . Reading data is valid when $\overline{RD}$ = L
43	$\overline{WR}$	I	Write . . . . . Data is written when $\overline{WR}$ = H
44	$\overline{RES}$	I	Reset . . . . . Resets each counter.
45 ∫ 52	DB_0 ∫ DB_7	I/$\overline{O}$/Z	8-bit data bus . . . Common terminal for three state I/O.
53 ∫ 60	RD_0 ∫ RD_7	I	ROM/RAM data input . . . Dot pattern data for the character generator
61 ∫ 64	RA_0 ∫ RA_3	$\overline{O}$/Z	Raster address output. *This output is not used in the graphic mode.
65 66	XT $\overline{XT}$	I $\overline{O}$	X'tal osc. . . .When an external clock is used by setting $\overline{DIV}$ to "L", feeds it to XT.
67	V_{SS}		Ground pin.
70	$\overline{DIV}$	I	"H": EXT clock. "L": Self-excided oscillation

FUNCTIONAL DESCRIPTION

1. LCDC Internal Registers

The internal registers include one instruction register (IR) and nine data registers. (See Table 1).

Table 1 MSM6255GS internal registers

$\overline{CS}$	A_0	Instruction register	Register	Register name	READ	WRITE	Data bit							
		3 2 1 0					7	6	5	4	3	2	1	0
H	X	X X X X		Invalid	–	–								
L	H	X X X X	IR	Instruction register	O	O	X	X	X	X				
L	L	L L L L	MOR	Mode control register	X	O	X							
L	L	L L L H	PR	Character pitch register	O	O					X			
L	L	L L H L	HNR	Horizontal character number register	O	O	X							
L	L	L L H H	DVR	Duty number register	X	O								
L	L	L H L L	CPR	Cursor form register	O	O								
L	L	L H L H	SLR	Start address (lower) register	O	O								
L	L	L H H L	SUR	Start address (upper) register	O	O								
L	L	L H H H	CLR	Cursor address (lower) register	O	O								
L	L	H L L L	CUR	Cursor address (upper) register	O	O								

Note: "L" is read if the data of the registers marked X is read.

– Instruction register

The instruction register is a register for specifying the address of the data register which is accessed. This register is cleared when $\overline{RES}$ input is "L".

3

– Mode control register

The mode control register is specified by writing "00_H" in the instruction register.

Register	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction register	H	L	L	L	L	L	L	L	L
Mode control register	L	L	MODE DATA						

D_6	D_5	D_4	D_3	D_2	D_1	D_0	Output system	
H/L	H/L	H/L	H/L	L	L	L	1-bit serial	Character display
				H	L		2-bit parallel	
				X	H		4-bit parallel	
				X	H			
				L	L	H	1-bit serial	Graphics
				H	L		2-bit parallel	
				X	H		4-bit parallel	
				X	H			
Blink time	Cursor ON/OFF	Cursor blink	Display ON/OFF	2-bit parallel	4-bit parallel/ 1-bit serial	MODE		

H: Display ON
L: Display OFF

D_5 D_4
L L Cursor OFF
L H Cursor OFF
H L Cursor ON
H H Cursor blink

H: 16 frames
L: 32 frames
} Half of blinking cycle

— Character pitch register

Register	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction register	H	L	L	L	L	L	L	L	H
Character pitch register	L	$(V_p - 1)$				L	$(H_p - 1)$		

H_p represents the number of bits to be displayed among one byte display data sent from RAM. The value of H_p is the following five types.

H_p	D_2	D_1	D_0
4	L	H	H
5	H	L	L
6	H	L	H
7	H	H	L
8	H	H	H

— Horizontal character number register

	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction register	H	L	L	L	L	L	L	H	L
Character number register	L	L	$(H_N - 1)$						

Assuming the total horizontal dot number of the display is η_H,

$\eta_H = H_p \times H_N$, where $H_N = 2 \sim 128$.

The maximum value of $\eta_H = 8 \times 128 = 128$ bytes = 1,024 dots.

— Duty number register

Register	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction register	H	L	L	L	L	L	L	H	H
Time division register	L	$(N_X - 1)$							

$N_X = 2 \sim 256$

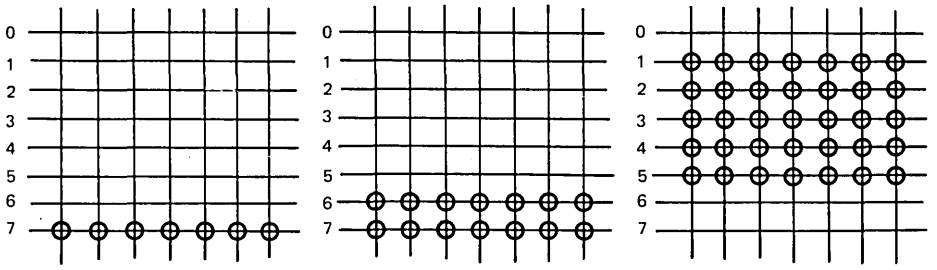
— Cursor form register

.Register	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction register	H	L	L	L	L	L	H	L	L
Cursor position register	L	$(C_{pu} - 1)$				$(C_{pd} - 1)$			

The cursor is displayed on the lines from C_{pu} to C_{pd} in the character display mode. The length of the cursor in the horizontal direction is equal to the character pitch in the horizontal direction, H_p.

The cursor is not displayed in graphic mode. The relation between the cursor and V_p is as follows.

Font configuration of $H_p = 7$ and $V_p = 8$



Note: (1) Setting of C_{pu}, $C_{pd} > V_p$ is not available.
(2) The cursor signal and pattern data are displayed subject to EX-OR.

– Start address (lower) register

Register	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction register	H	L	L	L	L	L	H	L	H
Display start address register (lower byte)	L	Start address (lower)							

– Start address (upper) register

Register	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction register	H	L	L	L	L	L	H	H	L
Display start address register (upper byte)	L	Start address (upper)							

The display start address shows an address of the RAM which stores data displayed at the left end and the most upper position.

The start address is composed of upper and lower 8 bits (16 bits in total).

– Cursor address (lower) register

Register	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction register	H	L	L	L	L	L	H	H	H
Cursor address register (lower byte)	L	Cursor address (lower)							

– Cursor address (upper) register

Register	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction register	H	L	L	L	L	H	L	L	L
Cursor address register (upper byte)	L	Cursor address (upper)							

By this instruction, the value of the cursor address is written in the cursor address register. The cursor is displayed at the position specified by the cursor address register.

2. LCD Display

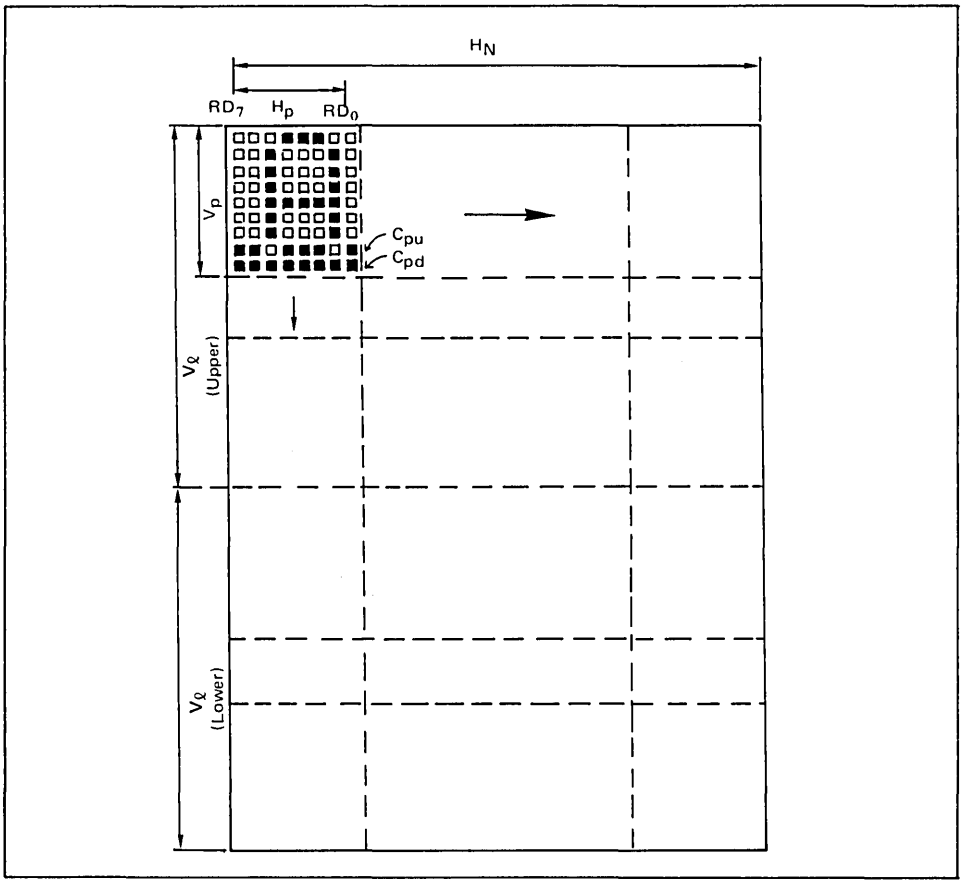


Table 2 Legend

Symbol	Name	Meaning	Value
H_p	Horizontal pitch	Pitch of characters in horizontal direction	4 ~ 8 dots
V_p	Vertical pitch	Pitch of characters in vertical direction	1 ~ 16 dots
H_N	Number of characters in one line	Number of characters per line or number of words per line	2 ~ 128 characters
V_L	Number of rows	Display duty	2 ~ 256
C_{pu}	Cursor start position	A position where the cursor starts display	Line 1 ~ 16
C_{pd}	Cursor end position	A position where the cursor stops display	Line 1 ~ 16

3. Built-In Bus Averter

The bus averter which switches the address buses $A_0 \sim A_{15}$ of the CPU with the memory address buses of the refresh. The refresh memory addresses are output to $MA_0 \sim MA_{15}$ when the input terminal of DIEN is set at high level and $A_0 \sim A_{15}$ are output to $MA_0 \sim MA_{15}$ when the input terminal of DIEN is set at low level.

4. External Clock Operation

An external clock enables the MSM6255GS to operate when the input terminal of $\overline{DIV}$ is set at high level. The external clock is input to XT.

5. Address Output Floating

$MA_0 \sim MA_{15}$ and $RA_0 \sim RA_3$ become high impedance when the input terminal of $\overline{ADF}$ is set at low level. This function is used when the address buses of memory are opened to others than $MA_0 \sim MA_{15}$.

$MA_0 \sim MA_{15}$ and $RA_0 \sim RA_3$ become normal impedance when the input terminal of $\overline{ADF}$ is set at high level.

6. Power Down Function

Power down function of the MSM5279GS (segment driver) can be used by connecting the output terminal of $CE\phi$ to the ECLK input of the MSM5279GS. This function is valid only in 4-bit parallel output mode.

7. Refresh Memory Address ($MA_0 \sim MA_{15}$) Operation

In the horizontal direction, MAxx is counted up at the trailing edge of $CH\phi$. Upper side is addressed while $CH\phi$ is set at low level and lower side is addressed while $CH\phi$ is set at high level.

MAxx is counted up even if it exceeds the number of horizontal display characters, but this does not affect the display since no data is being transferred at the time.

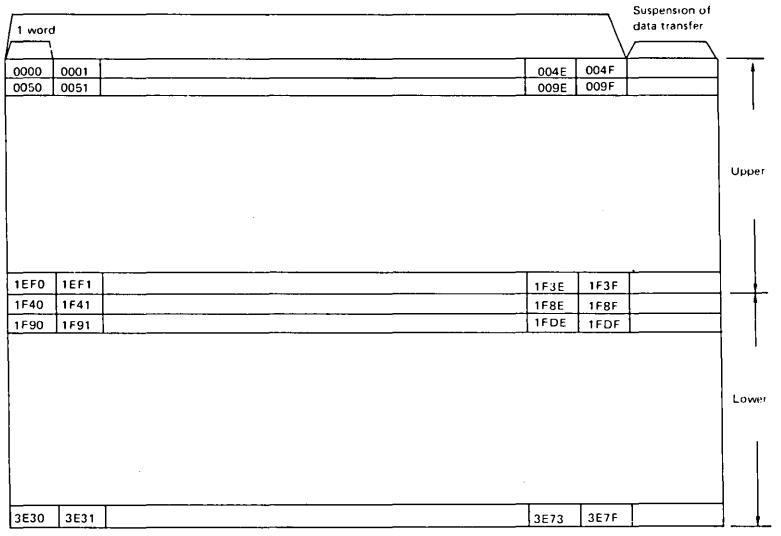
The period in which the data transfer is suspended corresponds to eight characters. When the period passes, one horizontal cycle is completed and the next cycle is commenced.

Memory address operation in the graphic mode is shown in Fig. 2 and that in the character mode is shown in Fig. 3.

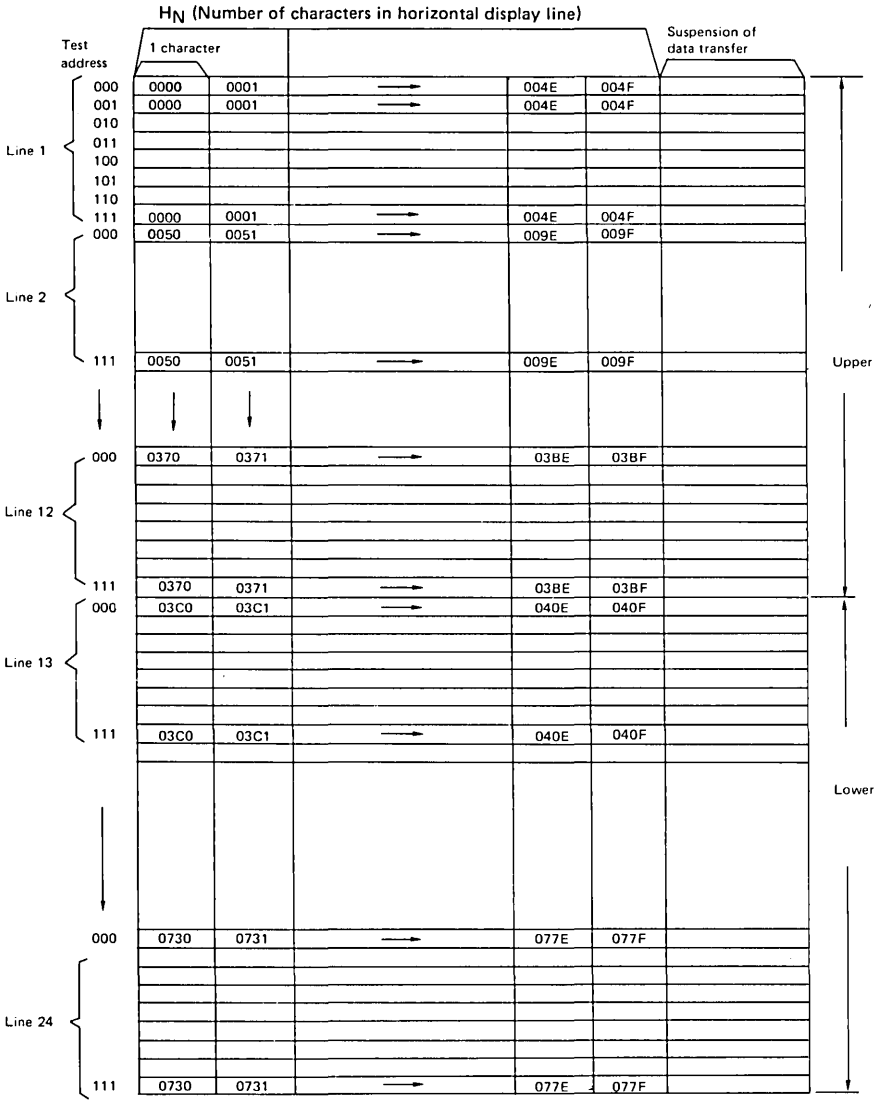
Address configuration of display RAM

HSB															LSB
MA_{15}	MA_{14}	MA_{13}	MA_{12}	MA_{11}	MA_{10}	MA_9	MA_8	MA_7	MA_6	MA_5	MA_4	MA_3	MA_2	MA_1	MA_0

Fig. 2 Memory address in the graphic mode (640 x 200)



Note: L is output for $RA_0 \sim RA_3$.



Note: Start address is 0000, 80 characters x 24 lines and V_p = 8.

Fig. 3 Memory address in the character mode (80 characters x 24 lines)

8. Output Mode

Three kinds of modes, 1 bit serial, 2-bit parallel and 4 bit parallel, are available as output modes. Data flow of each mode is shown below.

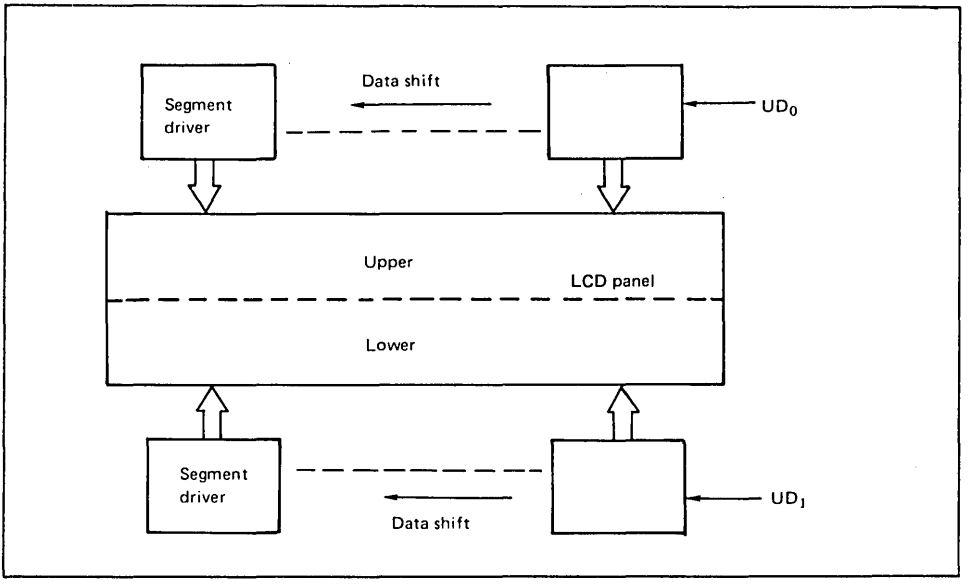


Fig. 4 1 bit seriel data transfer

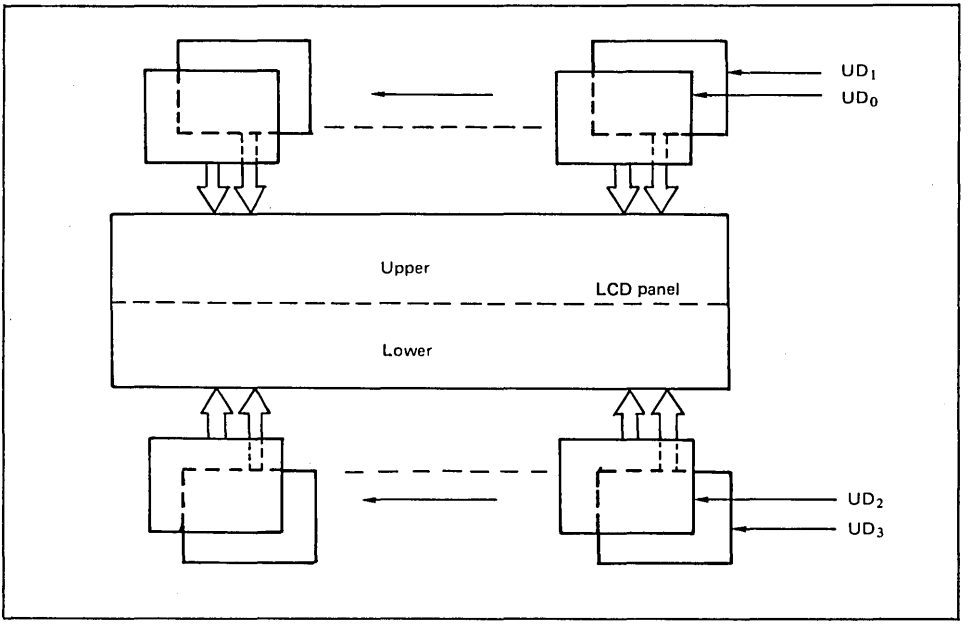


Figure 5 2-bit parallel data transfer

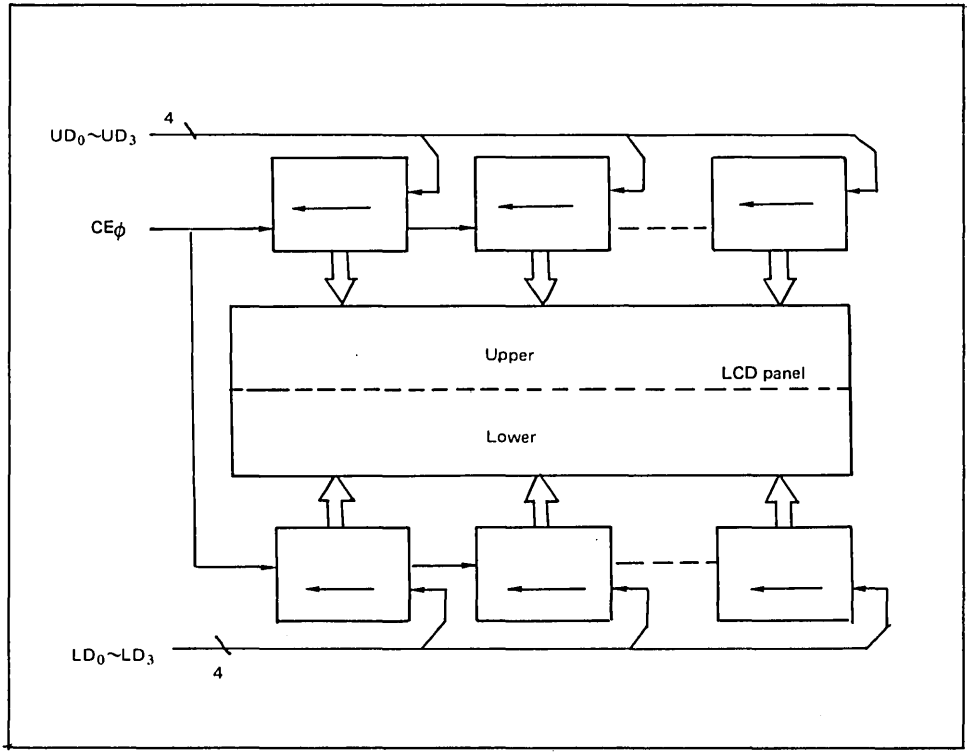
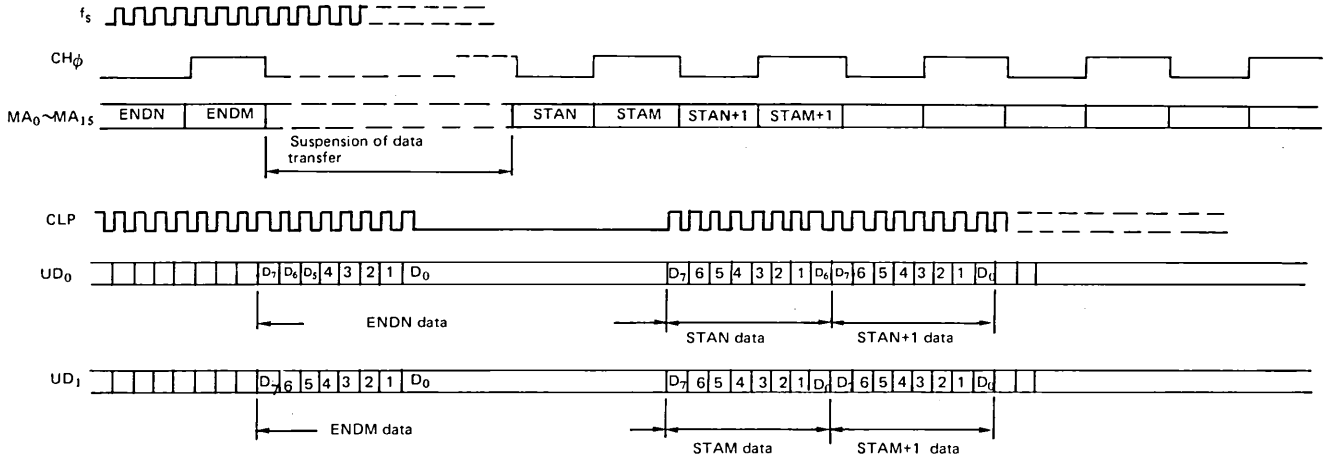


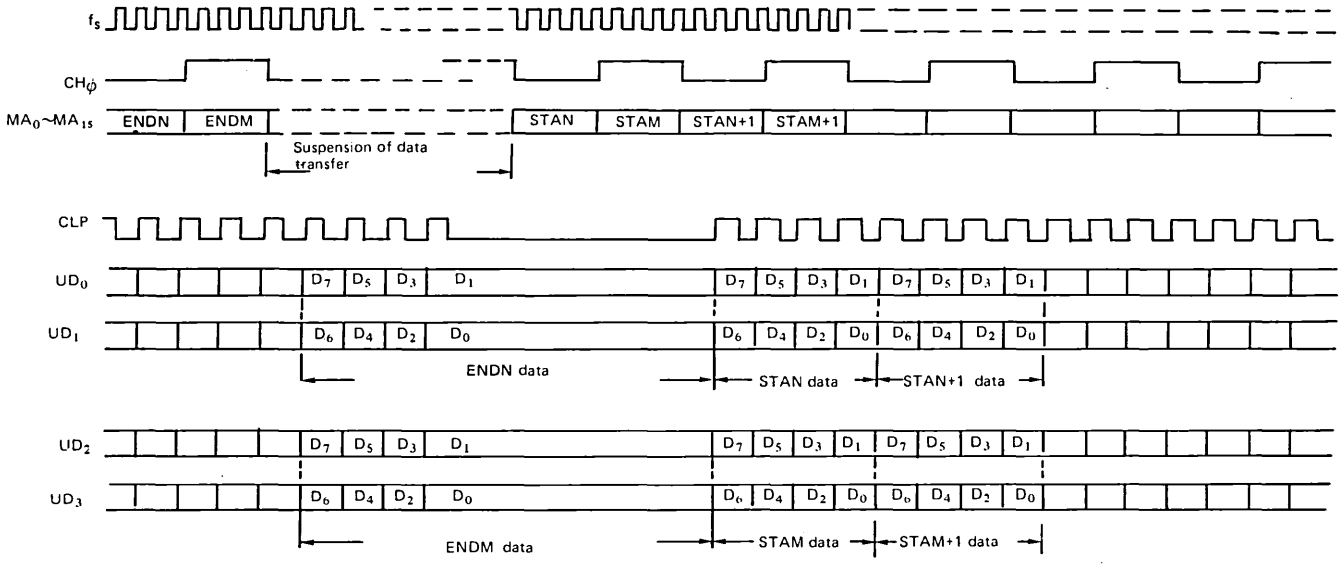
Fig. 6 4 bit parallel data transfer

Time charts corresponding to data transfers shown in Fig. 4 – Fig. 6 are shown in Fig. 7 – Fig. 9.



Note: STAN: First memory address of one horizontal line in the upper side
STAM: First memory address of one horizontal line in the lower side
ENDN: Last memory address of one horizontal line in the upper side
ENDM: Last memory address of one horizontal line in the lower side

Fig. 7 1 bit serial data transfer



Note: STAN: First memory address of one horizontal line in the upper side
STAM: First memory address of one horizontal line in the lower side
ENDN: Last memory address of one horizontal line in the upper side
ENDM: Last memory address of one horizontal line in the lower side

Fig. 8 2-bit parallel data transfer

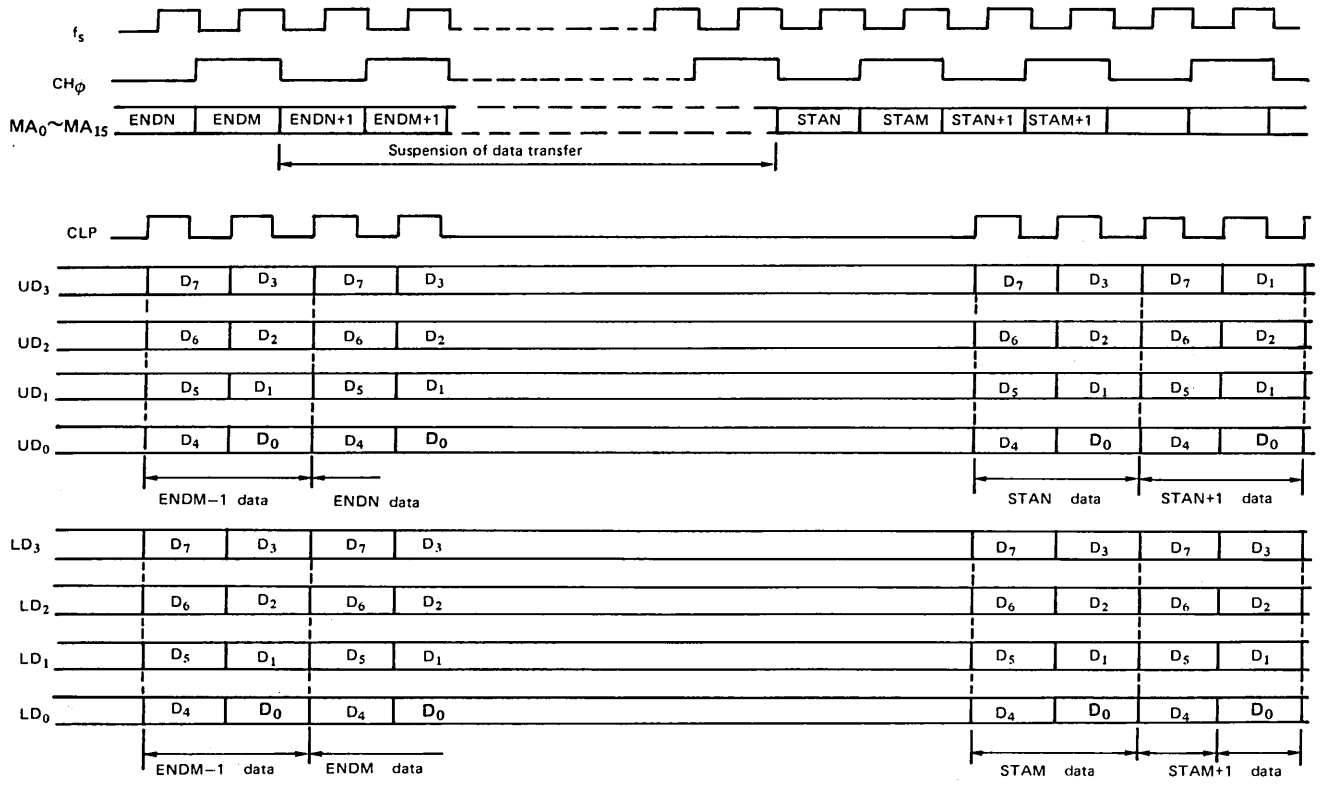


Fig. 9 4 bit parallel data transfer

9. LCD Driver

The most suitable LCD drivers for 4-bit parallel data transfer are MSM5278GS (common driver) and MSM5279GS (segment driver). MSM5260GS is the most suitable common/segment LCD driver in the case of 1-bit serial data transfer and 2-bit parallel data transfer.

Note: 4-bit parallel data transfer cannot be applied to MSM5260GS. Both 1-bit serial data transfer and 2-bit parallel data transfer cannot be applied to MSM5279GS.

10. Relation Between Duty and Number of Lines

Number of lines is determined by V_p, vertical character pitch, and V_ℓ, number of lines in vertical direction.

Number of lines = $V\ell/V_p \times 2$

Note: In the graphic mode, number of lines should not be odd number.

3

11. Calculation of Crystal Oscillation Frequency (f_{osc})

Table 3 Calculation formula of f_{osc}

$\overline{DIV}$	Output mode	Calculation formula of f_{osc}	Calculation example (MHz)
L	①	FRP × (H_N + 8) × H_p × V_ℓ × 2	9.856
	②	FRP × (H_N + 8) × $V\ell$ × 4	2.464
H	①	FRP × (H_N + 8) × V_p × V_ℓ	4.928
	②	FRP × (H_N + 8) × $V\ell$ × 2	1.232

Note: (1) Table 3 shows a calculation example assuming that FRP = 70 Hz, H_N = 80, H_p = 8 and $V\ell$ = 100, however, the example of H_p = 4 ~ 7 in 4-bit parallel is not included.

(2) Output mode ① : H_p = 4 ~ 7 in 1-bit serial, 2-bit parallel and 4-bit parallel
Output mode ② : H_p = 8 in 4-bit parallel

12. Calculation of Character Clock (CH_ϕ) Frequency

$$CH_\phi = FRP \times (H_N + 8) \times V_\ell$$

Example: Assuming FRP = 70 Hz, H_N = 80 and V_ℓ = 100,
CH_ϕ = 1.62 (μs)

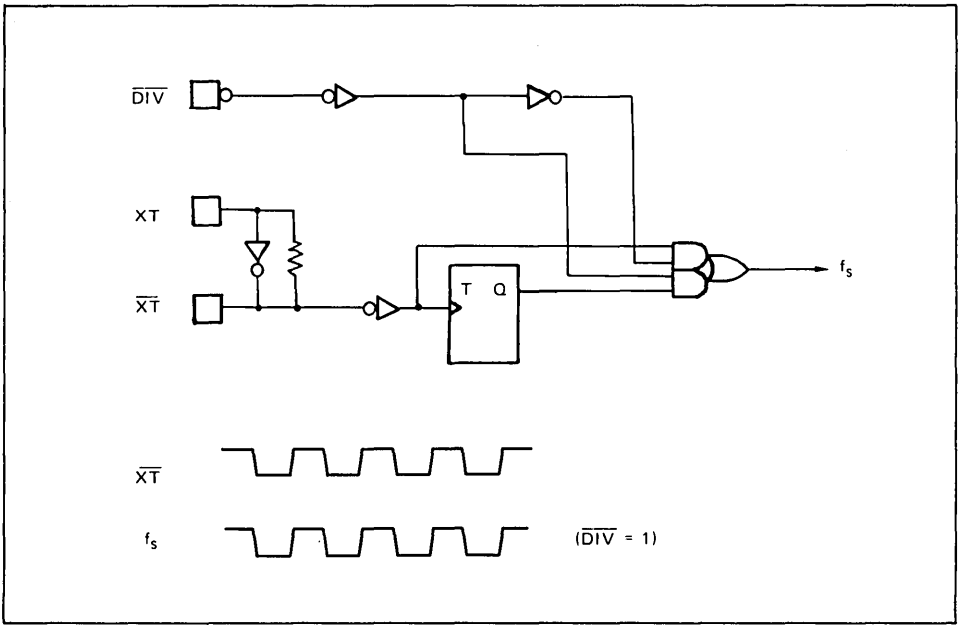
13. Calculation Shift Clock (CLP) Frequency

Table 4 Calculation formula of CLP

Output mode	Calculation formula of CLP	Calculation example (MHz)
1 bit serial	FRP × (H_N + 8) × H_p × V_ℓ	4.928
2-bit parallel	FRP × (H_N + 8) × H_p × V_ℓ × 1/2	2.464
4-bit parallel	FRP × (H_N + 8) × H_p × V_ℓ × 1/4	1.232

Note: Table 4 shows an calculation example assuming that FRP = 70 Hz, H_N = 80, H_p = 8 and V_ℓ = 100.

14. Relation Between Reference Clock (f_S) and External Clock



f_S functions as a dot clock in LCDC and the dot counter inside the IC is counted up at the tailing edge of f_S. The dot counter operates in N number system and its signals are output as CH_ϕ. (Refer to time charts Fig. 7–9 and Fig. 14.)

15. Access to the Display RAM

In writing/reading the data to/from the CPU, DIEN should be low level. By setting DIEN signal at low level, the address from the CPU are output from MA_0~MA_{15}, and this enables the access to the display RAM.
There are 3 method about accessing display RAM from the CPU.

(1) Direct access from CPU

Display RAM is accessed directly from the CPU, irrespective of MSM6255GS condition (refresh cycle or not).
In this method, the RAM address changes to the CPU address when the display is on the screen. So, frequent address to the RAM causes flickering on the screen.

(2) Access during BUSY signal is at high level

BUSY signal indicates the period when the data transfer is stopped and BUSY signal is set at high level during the data transfer is stopped. The period when BUSY signal is high corresponds to that of seven characters'. If display RAM is accessed during this period (when BUSY is high), the display on the screen does not flicker.

Note: This method is effective when the size of screen is small. In the case of big size screen, 640 x 200 dot, 1-character needs approx. 1.6μs. So, in this case, the period when BUSY is at high level is 11.2μs, which is impossible to write a lot of data.

(3) Synchronized access

Refresh scycle and CPU scycle are alternately performed. So, there is no flickering on the screen and there is no need to scence the BUSY signal.
In this method, however, some external circuits are necessary. The timing chart of this method is described in the Figure 10 below.

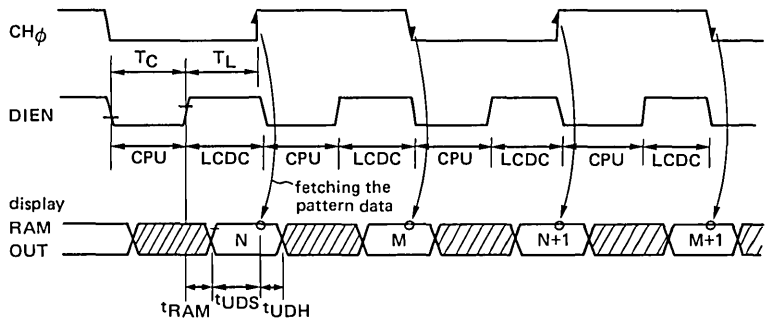


Figure 10 Basic timing of synchronized access to the display RAM.

legend

- T_C : Period wihen the address bus is occupied by CPU
- T_L : Period when the LCDC fetches the refreshed data
- t_{RAM} : Refresh address delay time + memory access time
- t_{UDS} : Upper side data set-up time
- t_{UDH} : Upper side data hold time

$MA_0 \sim MA_{15}$ output address to the upper side when DIEN is high and $CH\phi$ is low.
To perform synchronized access method, the timing between DIEN and $CH\phi$ should be as described in Figure 10.

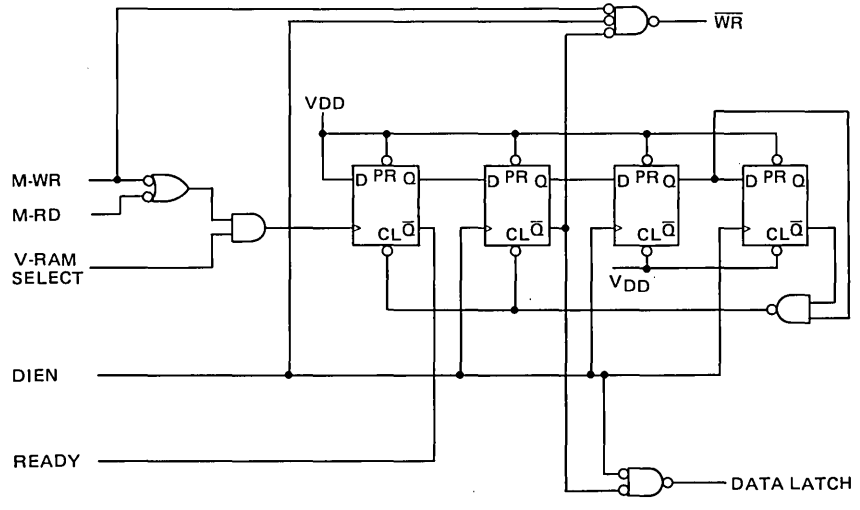


Figure 11 Wait function controlling circuit

Display RAM must meet following requirement.

$$T_L > t_{RAM} + t_{UDS}$$

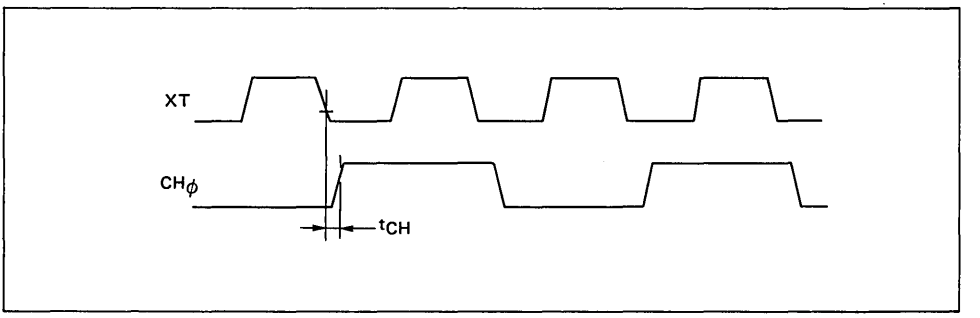
In writing data into the display RAM, LCDC should be synchronized so that the write pulse should occur during the period of T_C. In reading the pattern data from the CPU, the data of display RAM should be talched first.
Figure 11 shows the controlling circuit.

16. DIEN

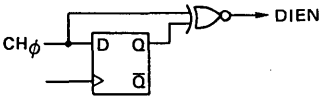
DIEN has to be generated when the display RAM is accessed by Synchronized access method described in 15-(3).

(1) Control the LCD module by separating upper side and lower side

Timing chart of XT and CHϕ is described as below. In this case, 4-bit data transfer is applied and H_p=8.



DIEN signal is generated by XT and CHϕ . DIEN signal generating circuit is described in the figure bellow.



When $H_p \neq 8$ in the 1-bit serial, 2-bit parallel and 4-bit parallel mode, the relation between XT and CHϕ should be refered to Figures 7 and 8.

17. Scroll·Paging

Scroll·paging is enabled by setting the display start address to the scroll address register.

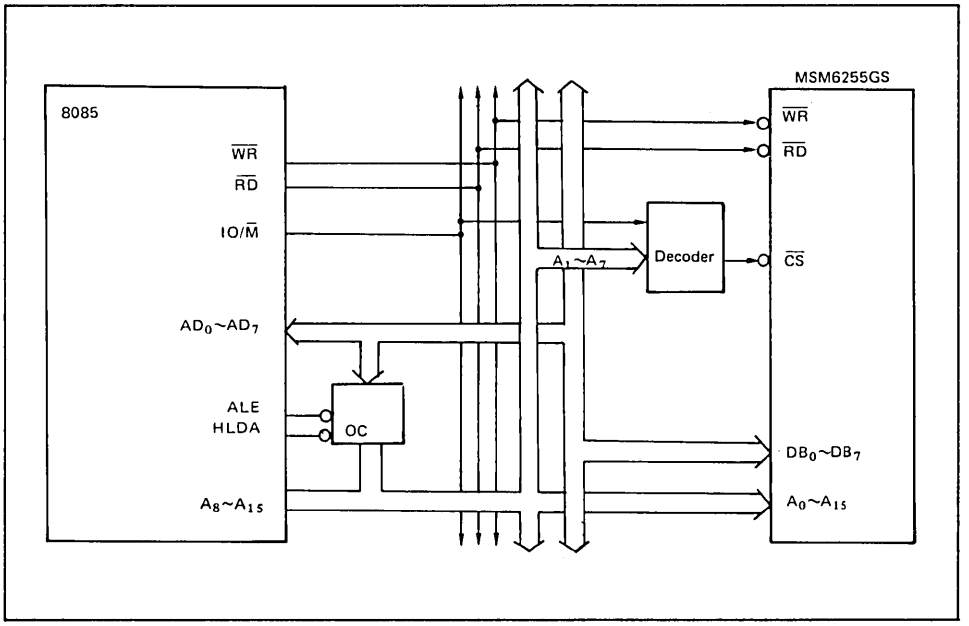
(1) Memory address of vertical scroll·paging

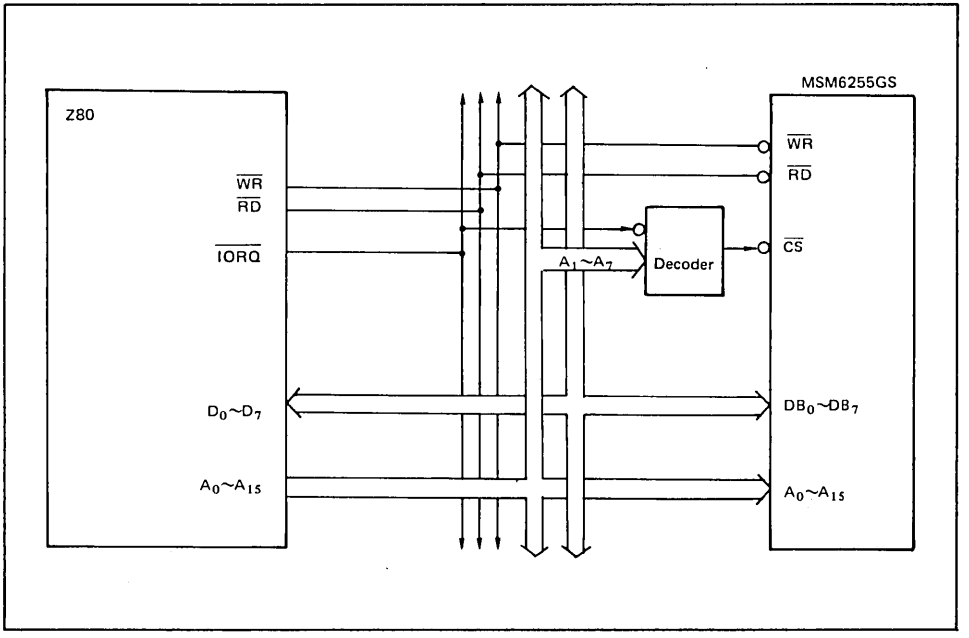
Figure 2 shows the memory address when the start address is 0000. When the start address is set at 0050, display will be vertically shifted by +1.
By setting the starting address one by one, screen will scroll vertically.
Paging will be performed by setting the start address as 3E80.

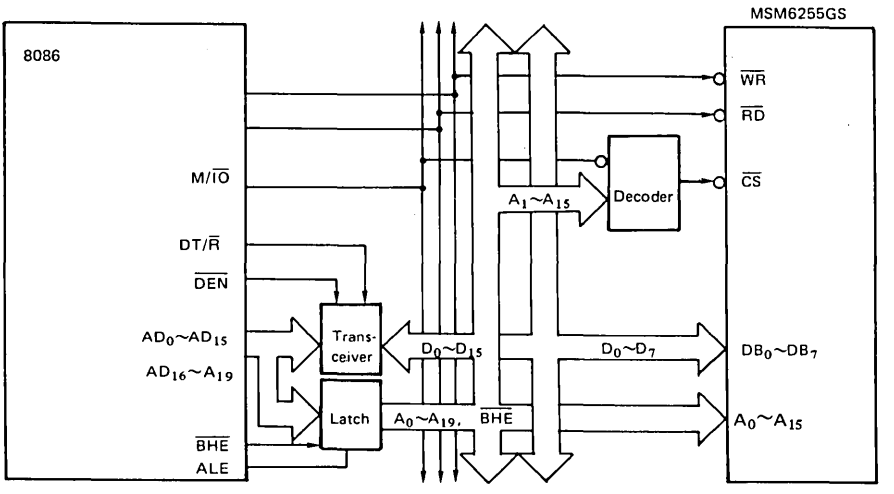
(2) Memory address of horizontal scroll

When the starting address is set at 0001 in Figure 2, the display on the screen will be shifted by +1 byte horizontally. The data shown as 004F in Figure 2 corresponds to the memory data in the 2nd line shown as 0050.

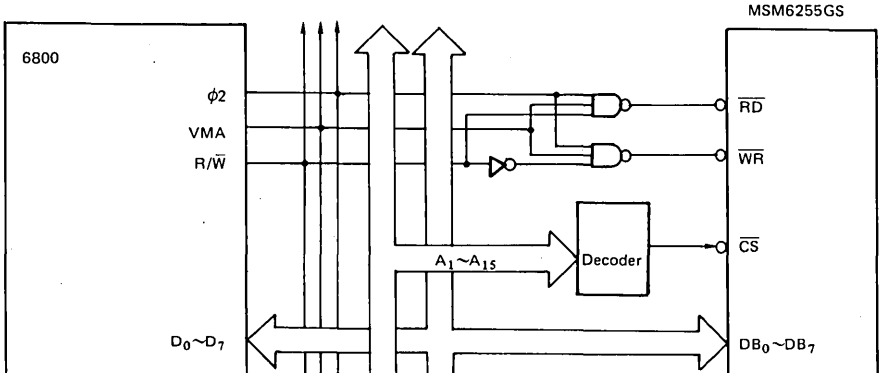
INTERFACE WITH CPU







*Minimum mode



SYSTEM CONFIGURATION

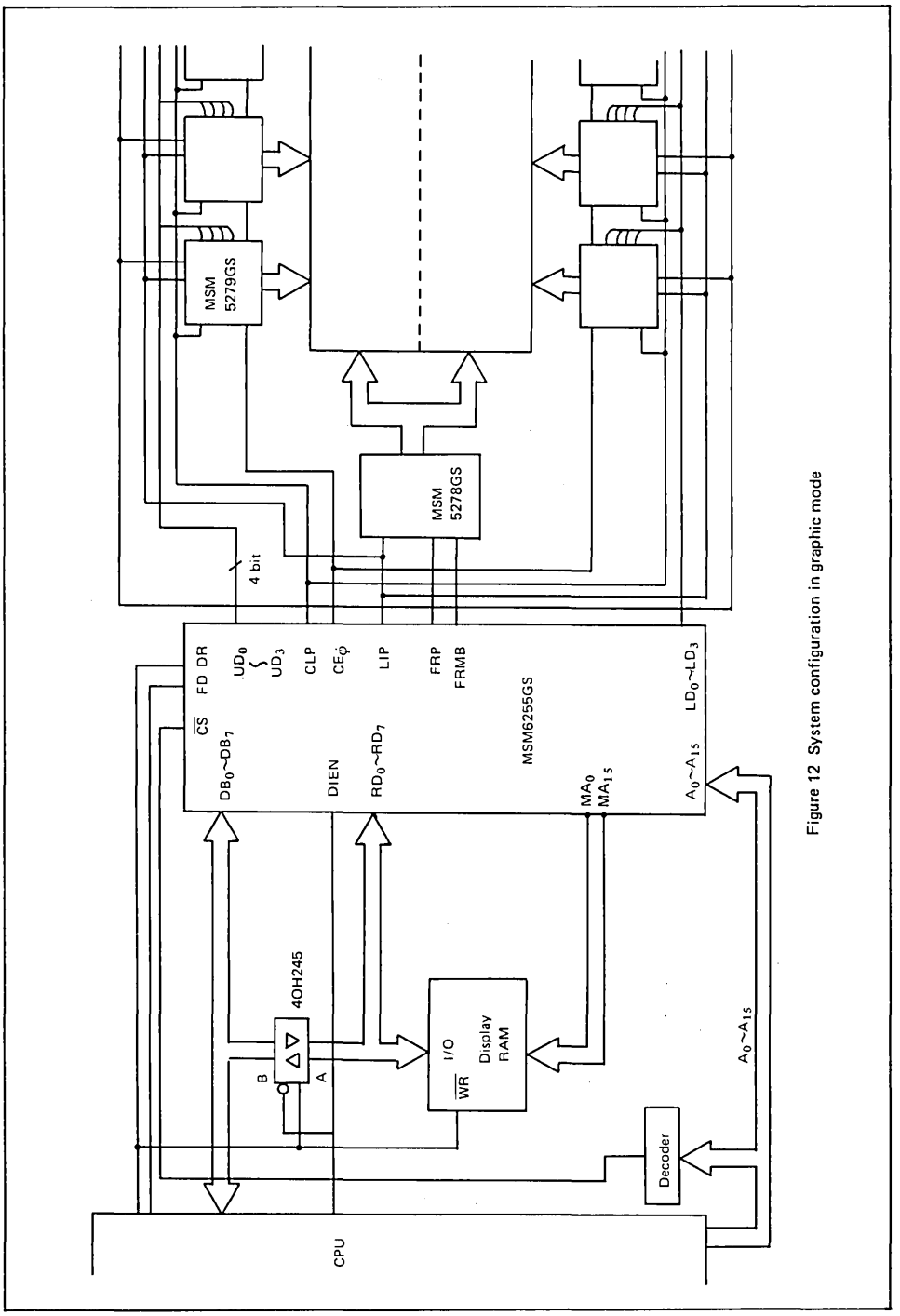


Figure 12 System configuration in graphic mode

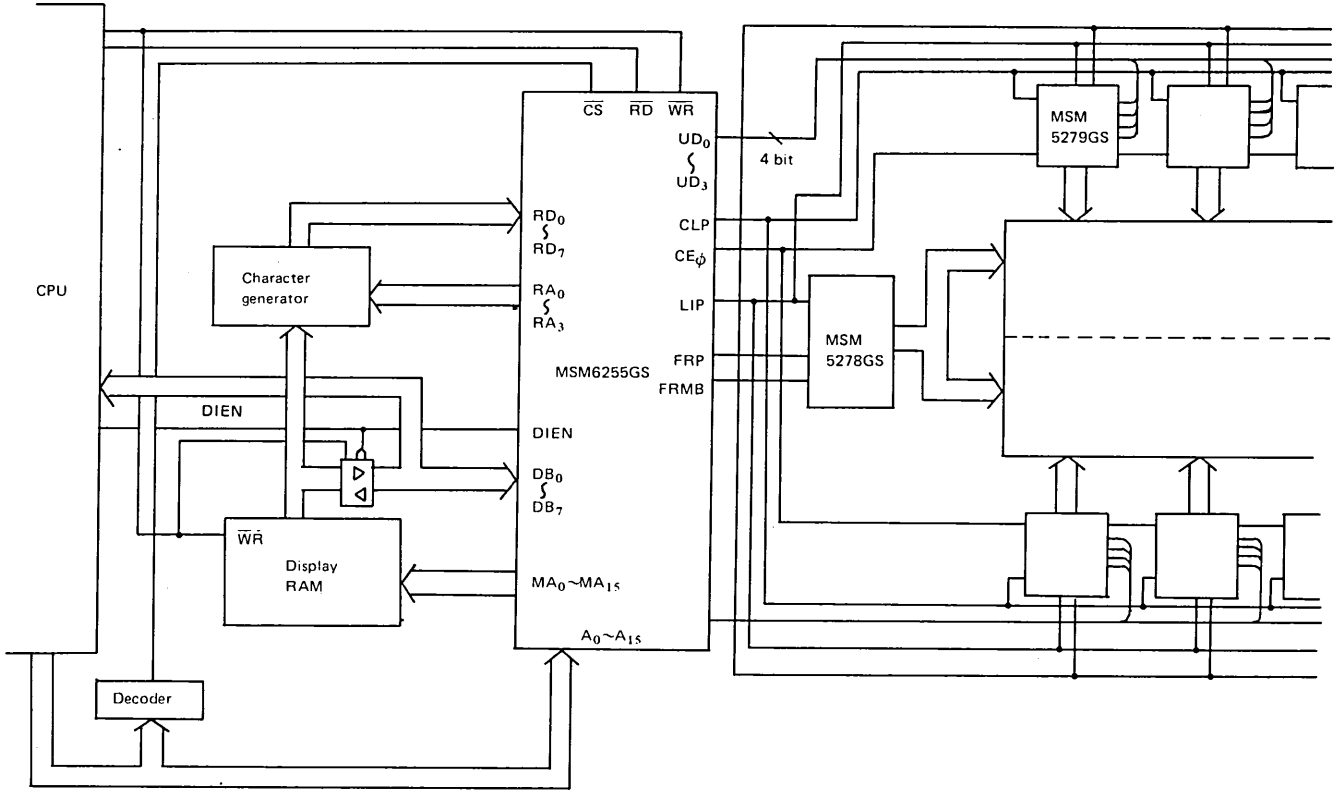


Figure 13 System configuration in character mode

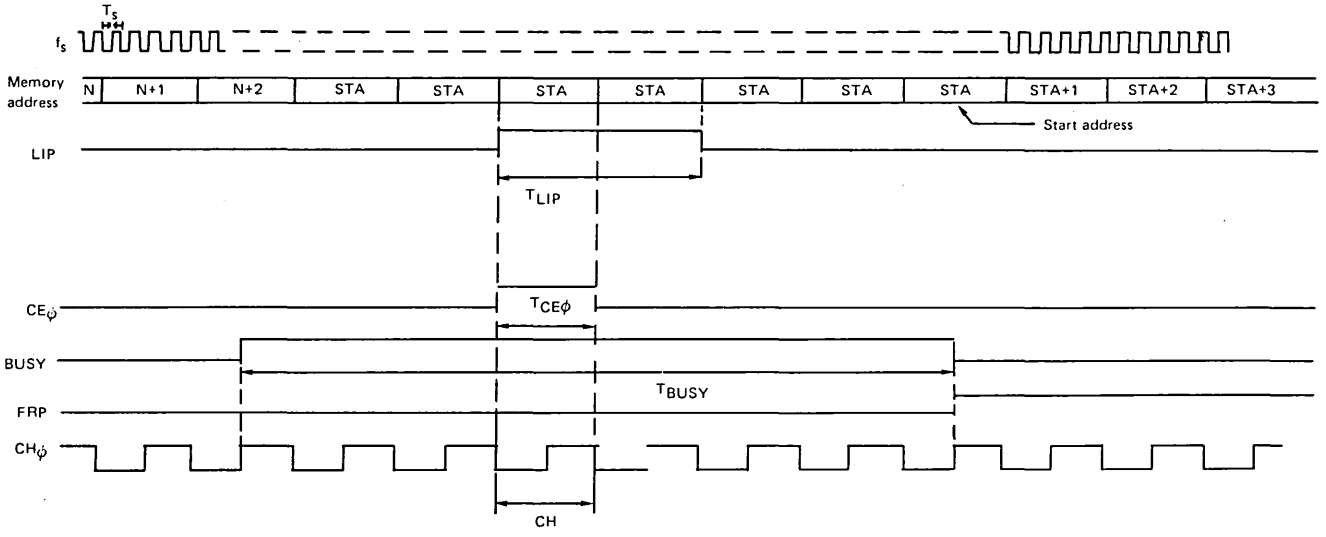


Figure 14 Time chart during suspension of shift clock

Condition: 4-bit parallel output mode
HP = 5

- $CH = T_s \times H_p$
- $T_{LIP} = 2CH$
- $T_{CE\phi} = CH$
- $T_{BUSY} = 7CH$

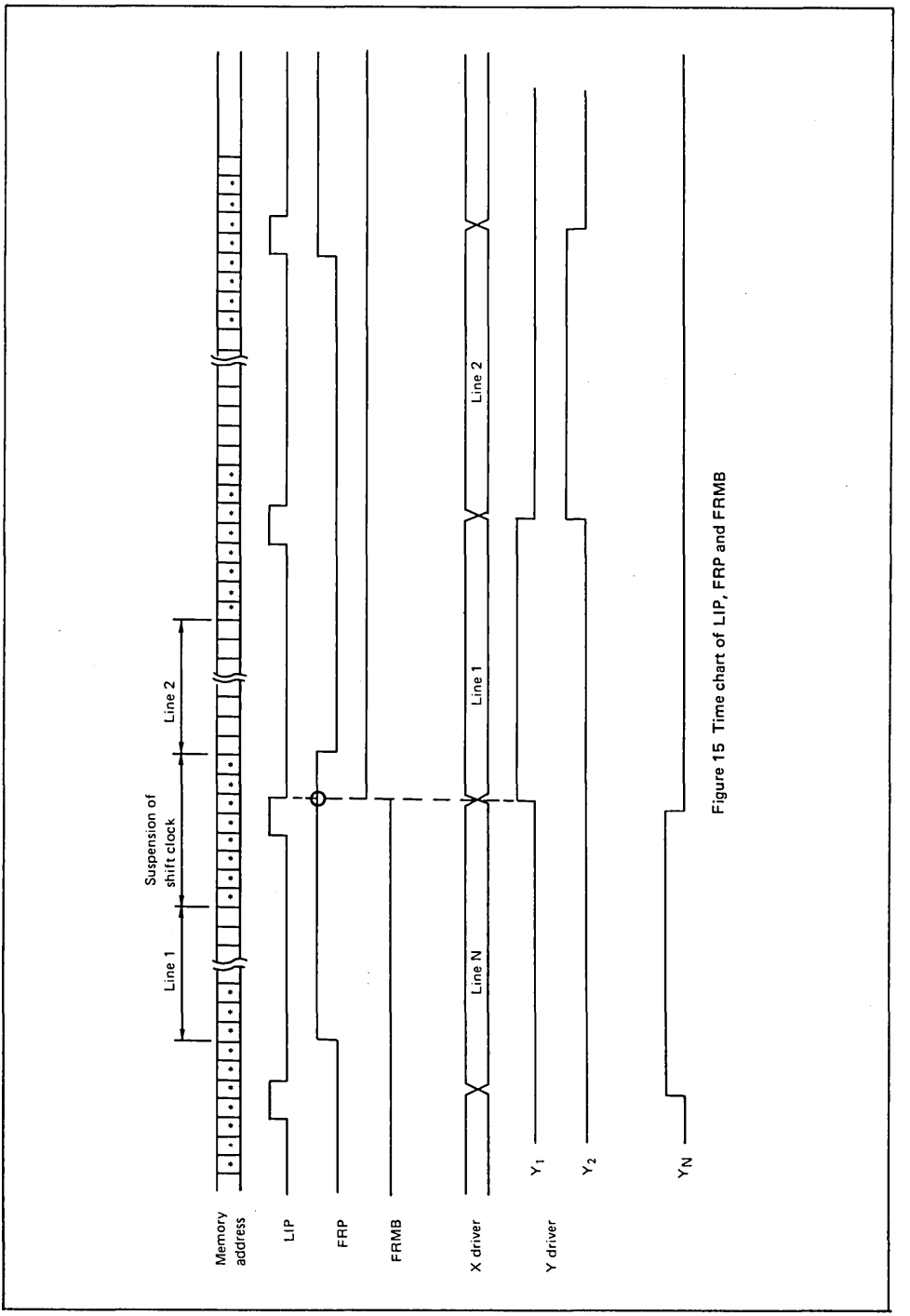


Figure 15 Time chart of LIP, FRP and FRMB

APPLICATION CIRCUIT

Figure 16 and Figure 17 show application circuits.
In these examples, the size of LCD module is 640 x 200 dot.
4-bit data transfer is applied and H_D = 8.
Synchronized access method is used as accessing method to the display VRAM.

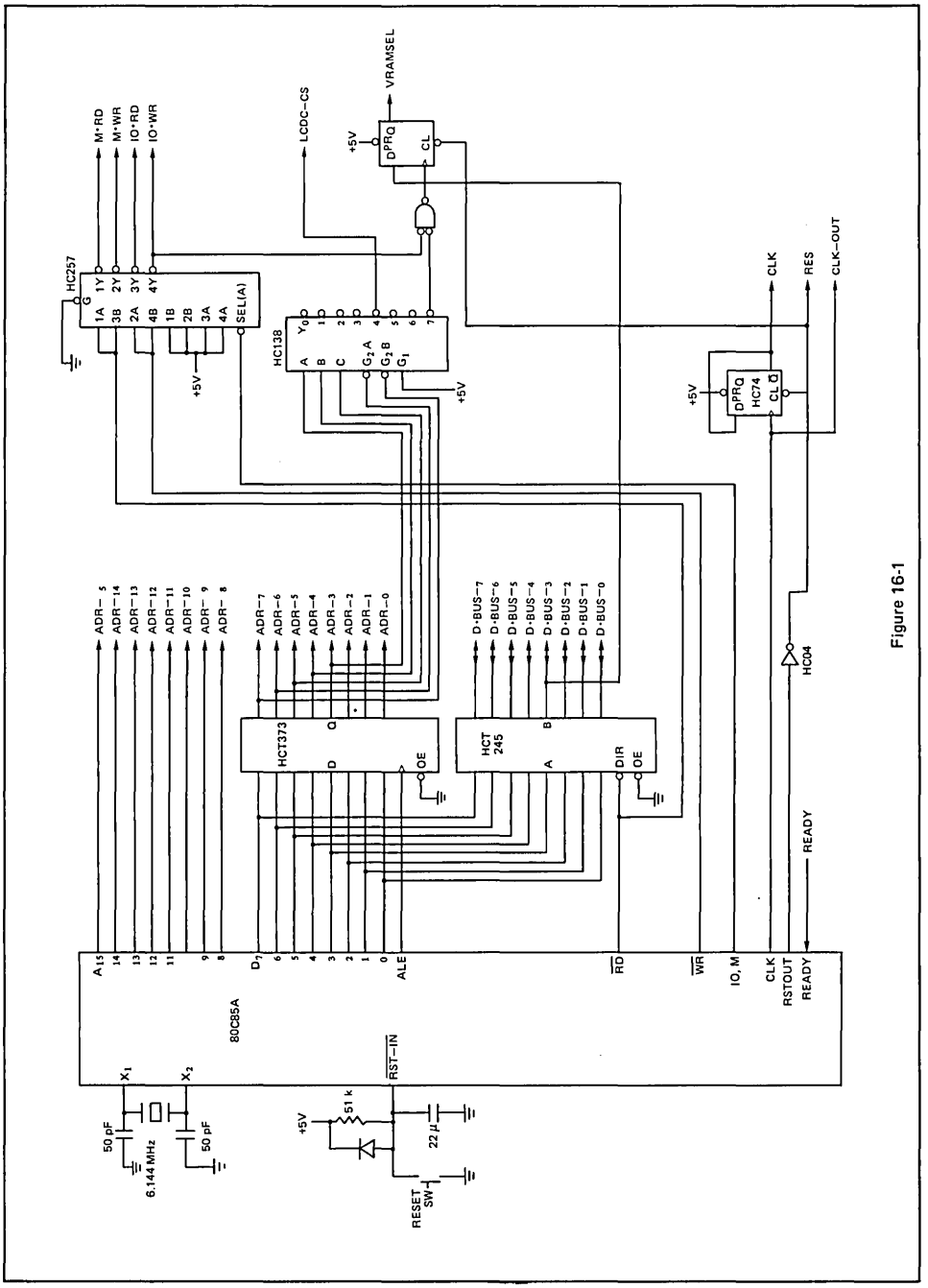


Figure 16-1

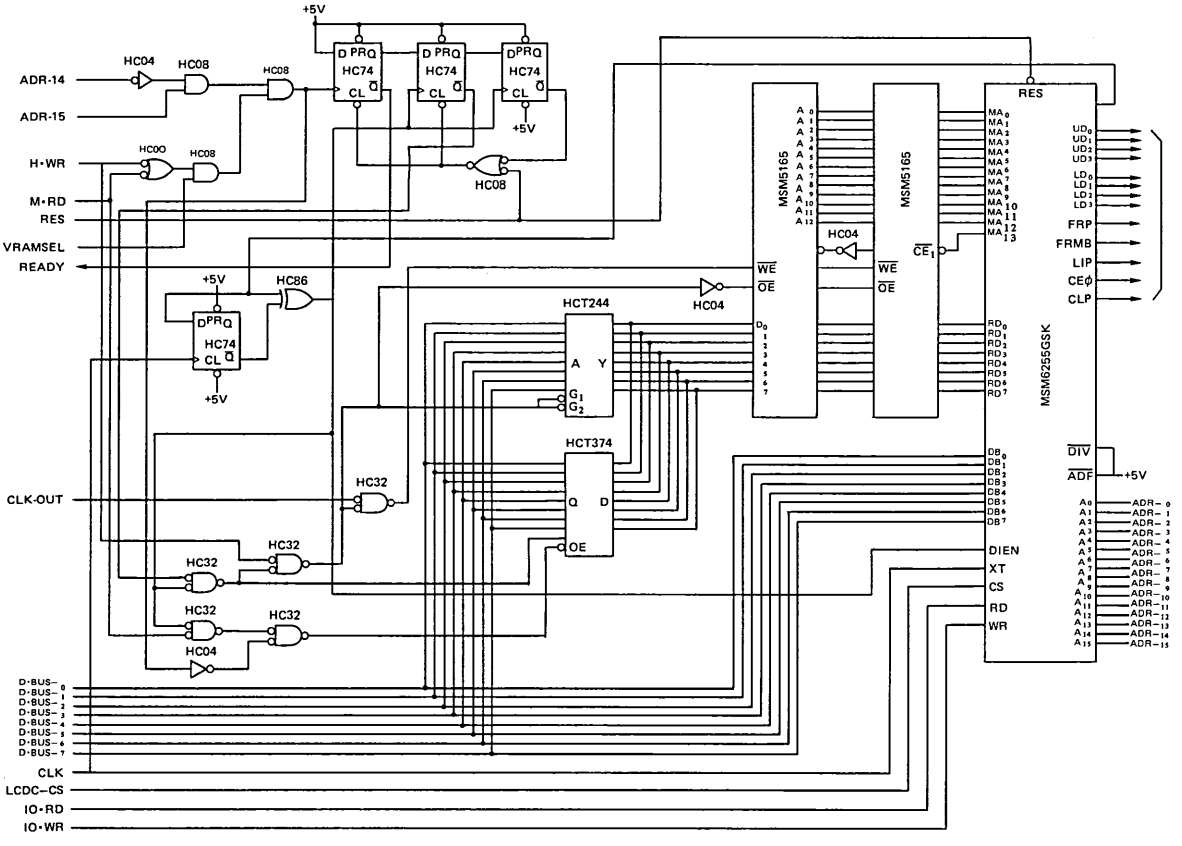

+5V
ADR-14
ADR-15
H•WR
M•RD
RES
VRAMSEL
READY
CLK-OUT
D•BUS-0
D•BUS-1
D•BUS-2
D•BUS-3
D•BUS-4
D•BUS-5
D•BUS-6
D•BUS-7
CLK
LCDC-CS
IO•RD
IO•WR
HC04
HC08
HC00
HC86
HC32
HC74
HCT244
HCT374
MSM5165
MSM6255GSK
WE
OE
CE1
DIV
ADF
DIEN
XT
CS
RD
WR
FRP
FRMB
LIP
CEϕ
CLP

Figure 16-2

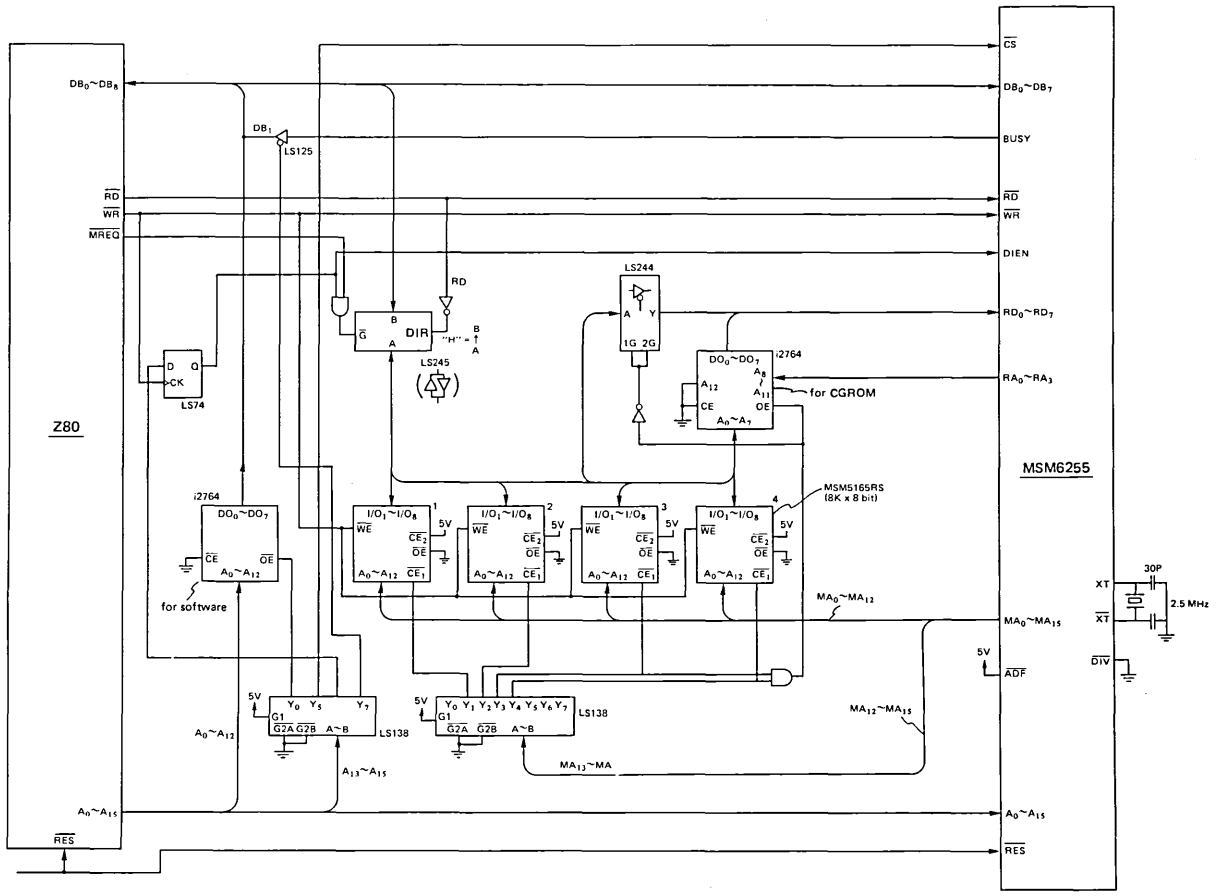

Z80
MSM6255
LS74
LS125
LS245
LS244
LS138
DIR
RD
for CGROM
for software
MSMS165RS
(8K x 8 bit)
2764
30P
2.5 MHz
XT
DIV
ADF
RES
BUSY
DIEN

Figure 17

MSM6265GS

DOT MATRIX LCD CONTROLLER

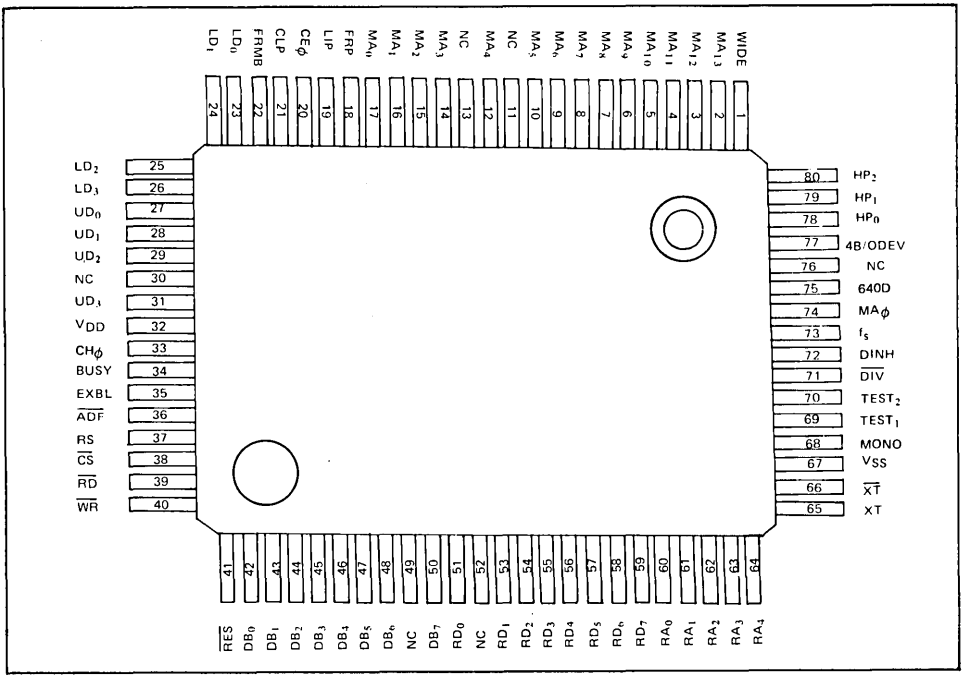
GENERAL DESCRIPTION

The OKI MSM6265GS is CMOS Si-gate LSI to control large size dot matrix LCD in characters and graphics.

FEATURES

- Software compatibility with HD6845 and HD46505 CRT controllers.
- Display control capacity
  Number of characters: 16,384 (2^{14}) characters
  Display addresses
  MA_0 to MA_{13}
  Raster addresses
  RA_0 to RA_4
- Duty: 1/100 X 2
- Number of characters per row: 2 to 128 (programmable)
- Font configuration: Vp: programmable
  Hp = 8 (4-bit parallel output),
  Hp = 4 to 8 (ODD/EVEN output)
- Attributes: Cursor ON/OFF/BLINK
- Scrolling, paging
- Data output: 4-bit parallel output, ODD/EVEN output
- Display system: AC inversion at each frame
- Crystal oscillator, external clock input
- Low power CMOS silicon gate process
- Single +5V power supply
- 80-pin flat package

PIN CONFIGURATION



BLOCK DIAGRAM

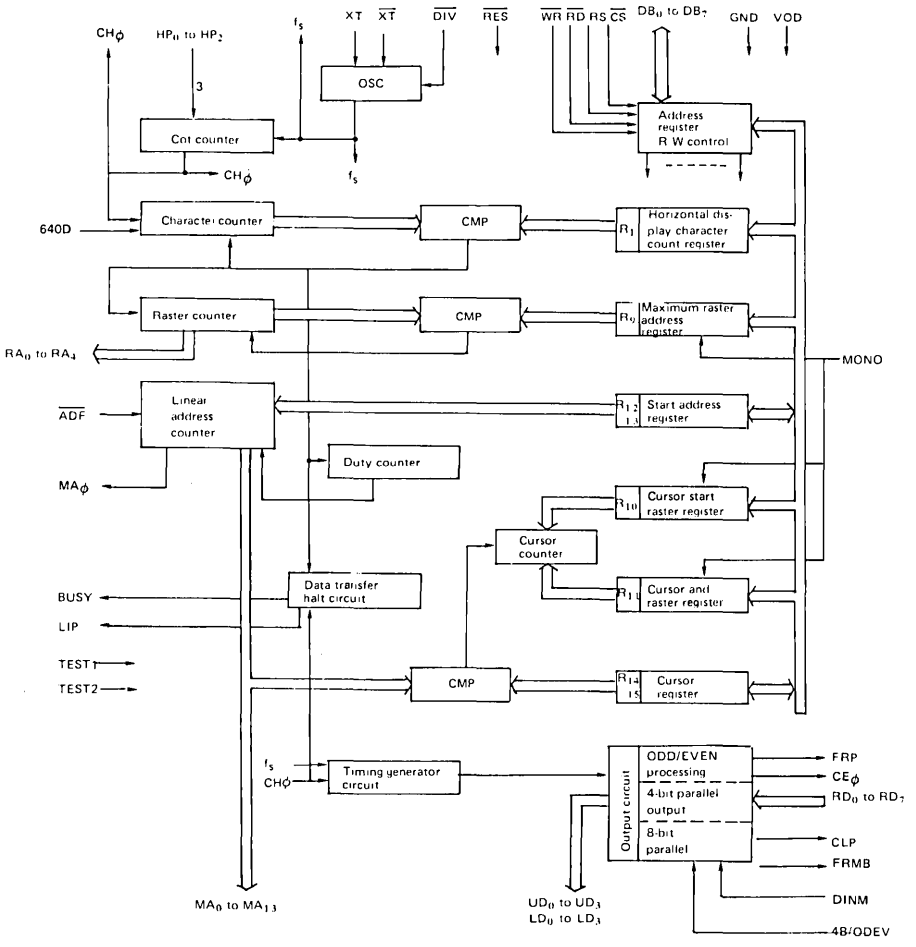


Figure 1 Block diagram

SYSTEM BLOCK DIAGRAM

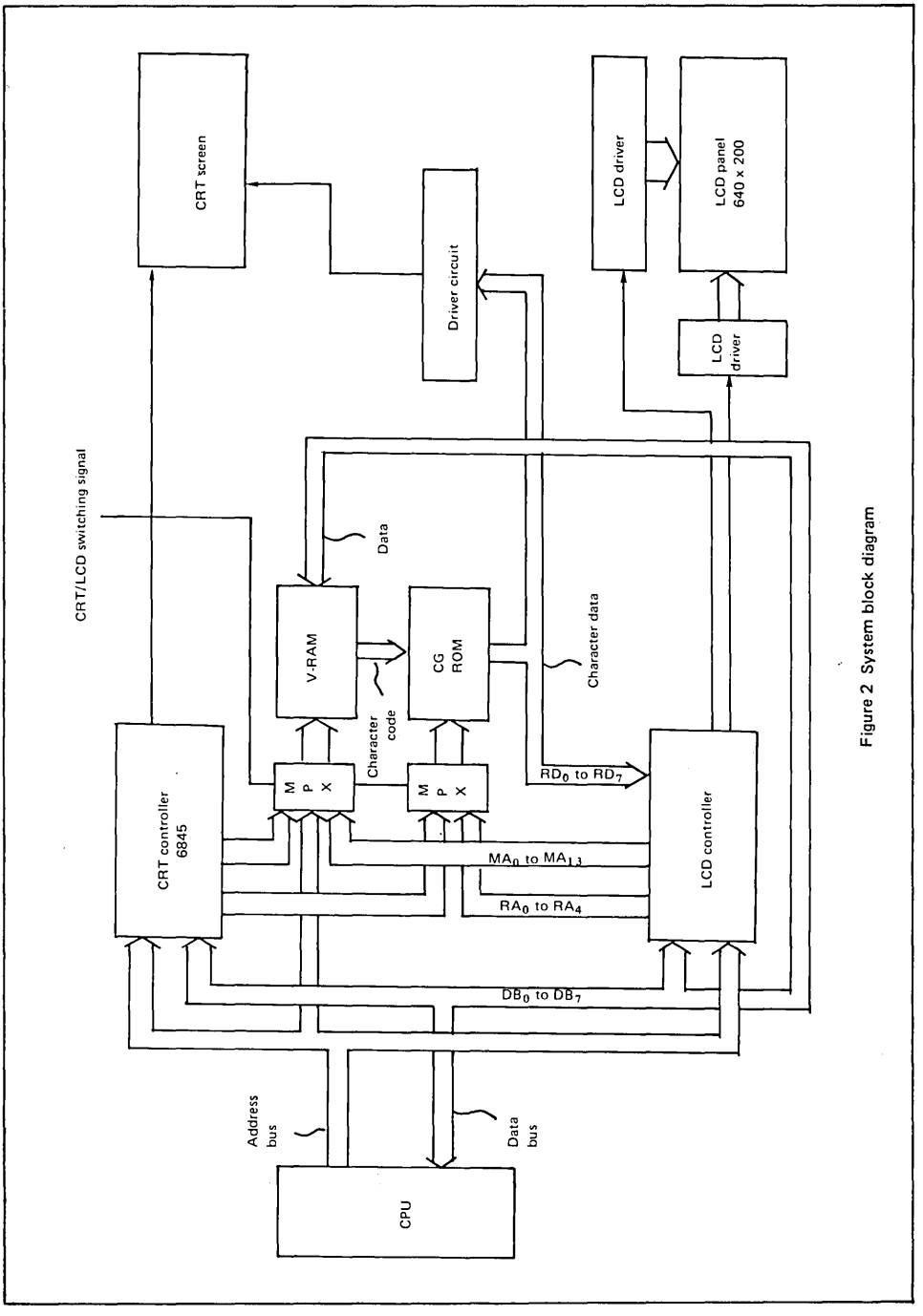


Figure 2 System block diagram

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	T_a = 25°C	−0.3 ~ 6.0	V
Input voltage	V_{IN}	T_a = 25°C	−0.5 ~ V_{DD} + 0.5	V
Storage temperature	T_{stg}	—	−55 ~ 150	°C

3

OPERATING RANGES

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	—	4.5 ~ 5.5	V
Operating temperature	T_{op}	—	−20 ~ 85	°C

INPUT CHARACTERISTICS

(V_{DD} = 5V ± 10%, T_a = −20 ~ 85°C)

Parameter	Symbol	MIN	TYP	MAX	Unit	Applicable terminal
"H" input voltage	V_{IH}	2.2	—	V_{DD}	V	DB_0 ~ DB_7, $\overline{RD}$, $\overline{WR}$, DINH, RD_0 ~ RD_7, $\overline{ADF}$, $\overline{CS}$, WIDE, RS, $\overline{RES}$, EXBL. MONO, 4B/ODEV.
"L" input voltage	V_{IL}	−0.3	—	0.8	V	
"H" input volage	V_{IH}	3.6	—	V_{DD}	V	XT, TEST1, TEST2, $\overline{DIV}$
"L" input voltage	V_{IL}	−0.3	—	1.0	V	
"H" input voltage	V_{IH}	2.4	—	V_{DD}	V	HP_0 ~ HP_2 640D
"L" input voltage	V_{IL}	−0.3	—	0.6	V	
"H" input current	I_{IH}	—	—	−1	μA	RS, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{ADF}$, $\overline{RES}$, $\overline{DIV}$, MONO, 640D, HP_0 ~ HP_2, DINH, DB_0 to DB_7, RD_0 to RD_7
"L" input current	I_{IL}	—	—	1	=A	
"H" input current	I_{IH}	—	—	−1	μA	TEST1, TEST2,
"L" input current	I_{IL}	—	—	100	μA	
Input capacitance	C_I	—	—	5	pF	All input terminals

OUTPUT CHARACTERISTICS

(V_{DD} = 5V ± 10%, T_a = −20 ~ 85°C)

Parameter	Symbol		MIN	TYP	MAX	Unit	Applicable terminal
"H" output current	I_{OH}	V_{OH} = 2.8V V_{OH} = 4.2V	−500 −100	—	—	μA μA	MA_0 ~ MA_{13}, DB_0 ~ DB_7, UD_0 ~ UD_3, LD_0 ~ LD_3, CLP, FRP, FRMB LIP, BUSY, $CH\phi$ $MA\phi$, fs
"L" output current	I_{OL}	V_{OL} = 0.4V	2.1	—	—	mA	

POWER CONSUMPTION

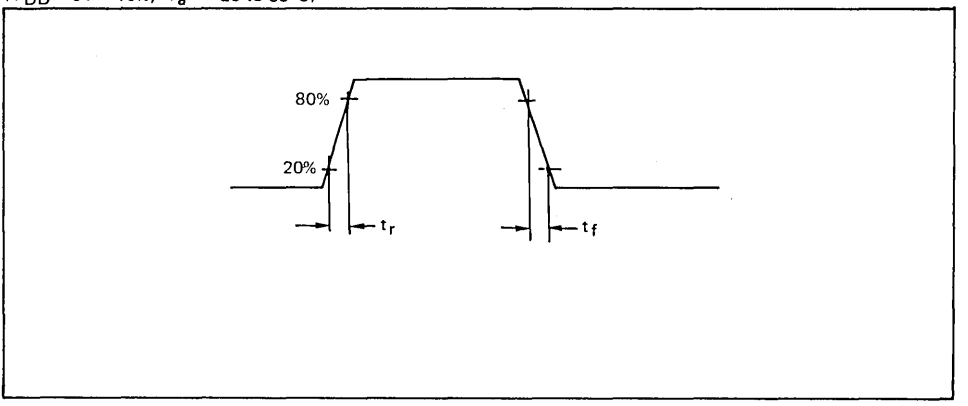
(T_a = 25°C)

Parameter	Symbol	V_{DD}	Condition	MIN	TYP	MAX	Unit
Static current	I_{DDS}	5v	f_{osc} = 0 Hz, No load	–	–	50	μA
Dynamic current	I_{DD}	5v	f_{osc} = 10 MHz, No load	–	–	15	mA

Note: TEST1 and TEST2 are open, and other inputs are either V_{DD} or GND level.

SWITCHING CHARACTERISTICS

(V_{DD} = 5V ± 10%, T_a = −20 to 85°C)



Parameters	Symbol	Load condition	MIN	TYP	MAX	Unit	Applicable terminal
Rising and falling times	t_r	60pF	–	–	40	ns	All output terminal
	t_f	60pF	–	–	40	ns	

MAXIMUM OPERATING FREQUENCY

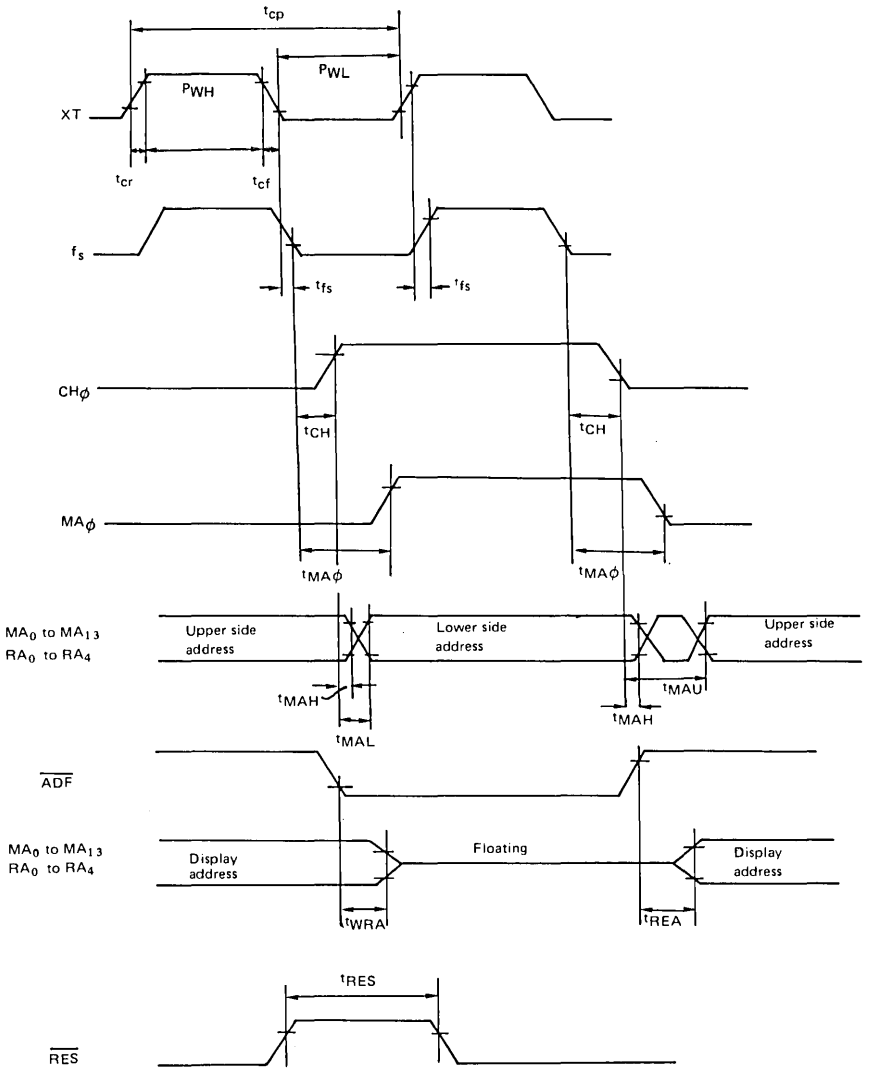
(V_{DD} = 5V ± 10%, T_a = −20 ~ 85°C)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	
Oscillating frequency	f_{osc}	$\overline{DIV}$ = "L"	11	–	–	MHz	Crystal oscillator
Basic clock frequency	f_s	$\overline{DIV}$ = "H"	5.5	–	–	MHz	External clock

PIN DESCRIPTION

Pin No.	Pin name	I/O/Z	Function
1	WIDE	I	Expansion mode when "H". Normal when "L".
2 ~ 17	MA_{13} ~ MA_0	O/Z	Address output to display RAM. High impedance when ADF = "L".
18	FRP	O	Frame signal
19	LIP	O	Display data latch signal
20	$\overline{CE\phi}$	O	Segment Drv chip enable clock
21	CLP	O	Display data shift clock
22	FRMB	O	Alternate signal
23 ~ 26	LD_0 ~ LD_3	O	Display data parallel outputs (lower side)
27 ~ 30	UD_0 ~ UD_3	O	Display data parallel outputs (upper side)
32	V_{DD}		+5V
33	$CH\phi$	O	Character clock
34	BUSY	O	Ready status signal. "H" during serial transfer halt period.
35	EXBL	I	Cursor control signal input
36	$\overline{ADF}$	I	Address floating input. Floating when "L".
37	RS	I	Register select input
38	$\overline{CS}$	I	Chip select . . . selection status when $\overline{CS}$ = "L"
39	$\overline{RD}$	I	Read . . . data reading possible while $\overline{RD}$ = "L"
40	$\overline{WR}$	I	Write . . . data writing executed by $\overline{WR}$ leading edge.
41	$\overline{RES}$	I	Reset signal input. Reset when "L".
42 ~ 50	DB_0 ~ DB_7	I/O/Z	8-bit data bus . . . three-state input/output common pins Pull-up registor on-chip Positive logic
51 ~ 59	RD_0 ~ RD_7	I	ROM data inputs . . . Dot pattern data of CGROM.
60 ~ 64	RA_0 ~ RA_4	O/Z	Raster address outputs. High impedance when $\overline{ADF}$ = "L".
65 66	XT $\overline{XT}$	I O	Crystal oscillator pins External clock is input to XT. ($\overline{XT}$ is open.)
67	GND		0V
68	MONO	I	Change R9, R10, and R11 contents when "H". Normal when "L". Direct V_{DD} and GND connections possible
69 70	$TEST_1$ $TEST_2$	I	Test input pins Left open for use.
71	$\overline{DIV}$	I	External clock when "H". Self-oscillation when "L". Direct V_{DD} and GND connections possible.
72	DINH	I	display OFF signal input. Display OFF when "L".
73	fs	O	Dot clock
74	$MA\phi$	O	Memory address counter clock output
75	640D	I	40-character memory address output and 80-character data reading when "H" Normal when "L"
77	4B/0DEV	I	4-bit parallel output when "H", ODD/EVEN output when "L". Direct V_{DD} and GND connections possible.
78 ~ 80	HP_0 ~ HP_2	I	1 font horizontal pitch program input. Direct V_{DD} and GND connections possible.

TIMING CHARACTERISTICS OF LCDC CONTROL SIGNAL

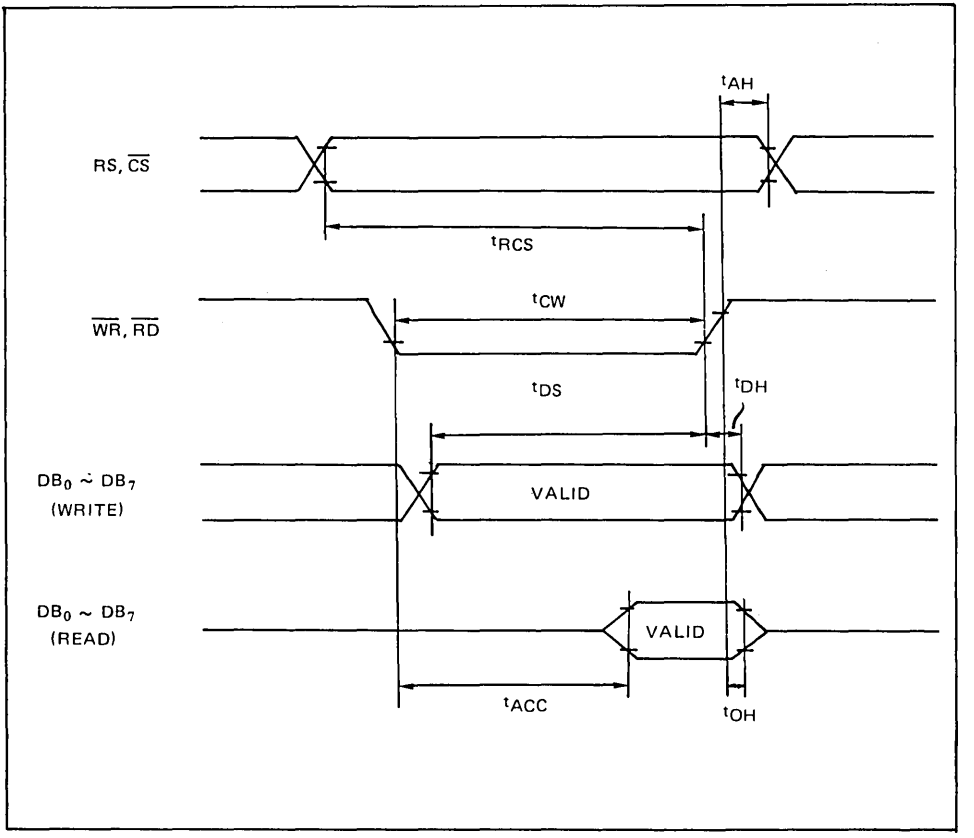


LCDC Control Signals

(C_L = 30pF, V_{DD} = 5V ± 10%, T_a = −20 to 85°C)

Parameter	Symbol	MIN	TYP	MAX	Unit
Clock cycle time	t_{cp}	180	–	–	ns
Clock "H" level pulse width	P_{WH}	80	–	–	ns
Clock "L" level pulse width	P_{WL}	80	–	–	ns
Clock rising and falling edge time	t_{cr}, t_{cf}	–	–	20	ns
Dot clock delay time	t_{fs}	–	–	110	ns
Character clock delay time	t_{CH}	–	–	100	ns
Memory address clock delay time	$t_{MA\phi}$	–	–	340	ns
Memory address hold time	t_{MAH}	5	–	–	ns
Upper side address delay time	t_{MAU}	–	–	290	ns
Lower side address delay time	t_{MAL}	–	–	120	ns
Drawing address delay time	t_{WRA}	–	–	40	ns
Display address delay time	t_{REA}	–	–	40	ns
Reset "H" level pulse width	t_{RES}	1	–	–	μs

BUS TIMING CHARACTERISTICS

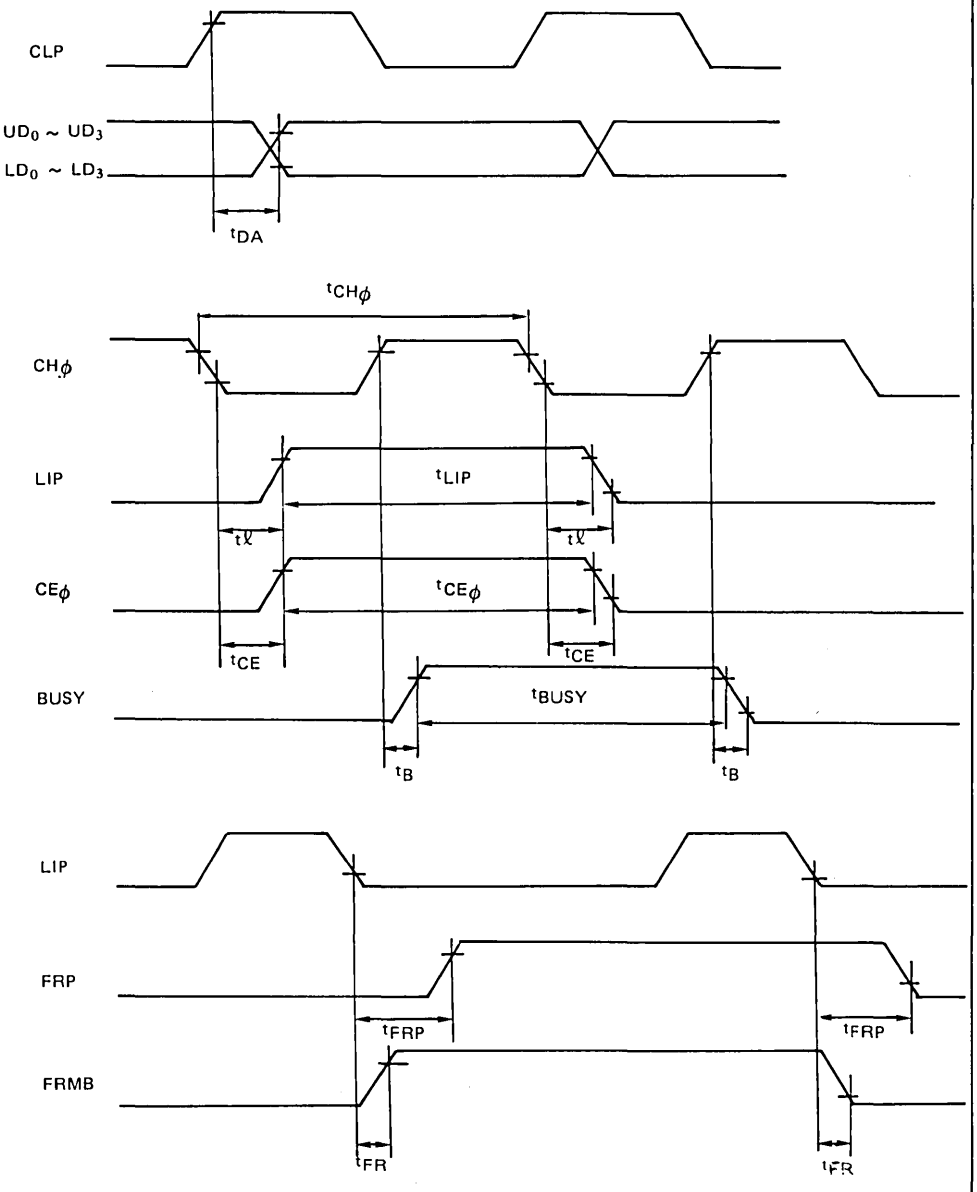


Bus Timing Characteristics

(C_L = 50pF, V_{DD} =5V ± 10%, T_a = −20 to 85°C)

Parameter	Symbol	MIN	TYP	MAX	Unit
Rs, $\overline{CS}$ set-up time	t_{RCS}	300	–	–	ns
$\overline{RD}$, $\overline{WR}$ pulse width	t_{CW}	300	–	–	ns
Address hold time	t_{AH}	40	–	–	ns
Data set-up time	t_{DS}	200	–	–	ns
Data hold time	t_{DH}	40	–	–	ns
Output disable time	t_{OM}	0	–	40	ns
Access time	t_{ACC}	–	–	200	ns

LCD DRIVER INTERFACE TIMING CHARACTERISTICS

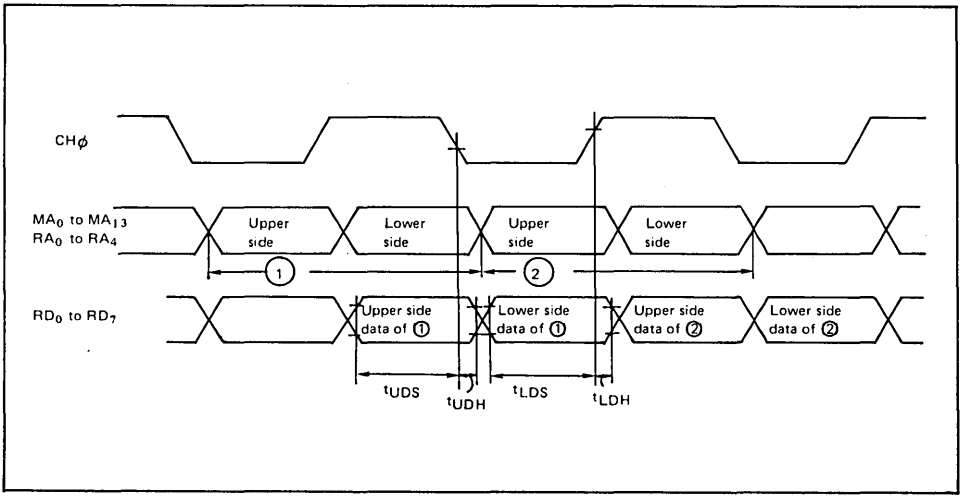


LCD Driver Interface Timing Characteristics

(C_L = 30pF, V_{DD} = 5V ± 10%, T_a = −20 ~ 85°C)

Parameter	Symbol	MIN	TYP	MAX	Unit
Data delay time	t_{DA}	–	–	100	ns
Cycle time for 1 character	$t_{CH\phi}$	730	–	–	ns
Latch signal delay time	t_{ℓ}	–	–	200	ns
Latch signal "H" time	t_{LIP}	1.46	–	–	μs
Chip enable clock delay time	t_{CE}	–	–	200	ns
Chip enable clock "H" time	$t_{CE\phi}$	730	–	–	ns
Ready signal delay time	t_B	–	–	200	ns
Ready signal "H" time	t_{BUSY}	5.11	–	–	μs
Frame signal delay time	t_{FRP}	$2t_{CH\phi}$	–	$2t_{CH\phi}$ + 200	ns
AC signal delay time	t_{FR}	–	–	200	ns

PATTERN DATA FETCHING TIMING



(C_L = 50 pF, V_{DD} = 5V ±10%, T_a = −20 ~ 85°C)

Parameter	Symbol	MIN	TYP	MAX	Unit
Upper side data set-up time	t_{UDS}	140	–	–	ns
Upper side data hold time	t_{UDH}	40	–	–	ns
Lower side data set-up time	t_{LDS}	140	–	–	ns
Lower side data hold time	t_{LDH}	40	–	–	ns

FUNCTIONAL DESCRIPTION

1. LCDC Internal Registers

The internal registers include one address register (AR), and eight data registers R1 and R9 ~ R15. (See Table 1).

1) Address register (AR)

When a data register is accessed, this register specifies the number of that register. Once this register has been written, the same value is held until the power is switched off without being influenced by $\overline{RES}$.

2) Horizontal display character number setting register (R_1)

Setting of the number of characters per line on the screen. Any value from 2 to 128 can be set.

Example: 80-character setting (50_H)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
L	H	L	H	L	L	L	L

3) Maximum raster address register (R9)

Setting of the value obtained by subtracting 1 from the raster counter corresponding to one line. The vertical pitch V_p for 1 font can be set to any value from 1 to 32.

Example: V_p = 8 setting

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
L	L	L	L	L	H	H	H

4) Cursor start raster register (R10)

This is one of the cursor control registers. The raster address of the top edge of the cursor is specified in the five lower order bits, and the cursor display mode is specified in the two higher order bits. The cursor display mode is set to either mode A or mode B by the EXBL input pin.

Cursor display mode A

	D_6	D_5	EXBL = "H"
	L	L	Cursor displayed in stationary position
	L	H	No cursor display
Note 1	H	L	Cursor blinked on and off every 32 frames
Note 2	H	H	Cursor blinked on and off every 64 frames

Cursor display mode B

D_6	D_5	EXBL = "L"
L	L	No cursor display
L	H	
H	L	
H	H	

Note 1 & 2:

Blinking cycles:

On | Off

32 or 64 frame interval

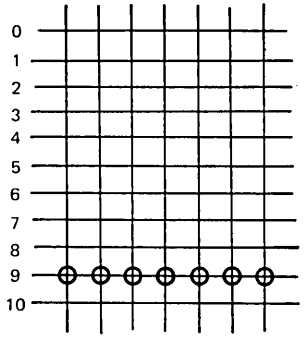
Note 3:

If the blinking cycle is applied to EXBL from an external source with D_6 = 0 and D_5 = 0, the cursor is blinked on and off by the EXBL frequency.

5) Cursor end raster address (R11)

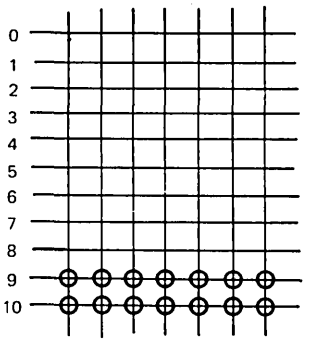
This is another cursor control register. This register specifies the raster address of the bottom edge of the cursor. The relation to R10 is outlined below.

• HP = 7, V_p = 11, cursor start address ≤ cursor end address ≤ maximum raster address

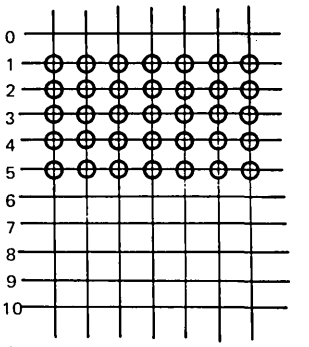


Cursor start address = 9

Cursor end address = 9

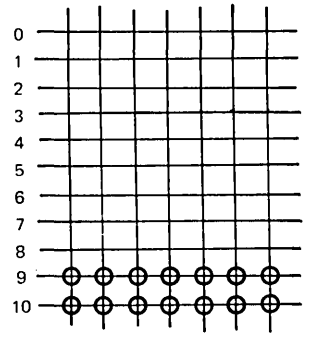


Cursor start address = 9
Cursor start address = 10



Cursor start address = 1
Cursor end address = 5

• HP = 7, V_p = 11, cursor start address > cursor end address



← Displayed up to the maximum raster address.

Cursor start address = 9
Cursor end address = 8

• Maximum raster address < cursor start address ≦ cursor end address.
Cursor display is switched off.

Note: When the cursor overlaps pattern data, the result of an EX-OR operation between the cursor signal and the pattern data is displayed.

6) Start address registers (R12 & R13)

Register for setting the memory address corresponding to the first character in the first line on the screen. The LCDC commences data display from this address. Both reading and writing are possible, and when reading, the two higher order bits become "00".

7) Cursor registers (R14 & R15)

The cursor display address is specified by two bytes. The LCDC controls the cursor when the memory address MAxx reaches this address while within the R10/R11 range.
Both reading and writing are possible, and when reading, the two higher order bits become "00".

Table 1 MSM6265GS internal registers

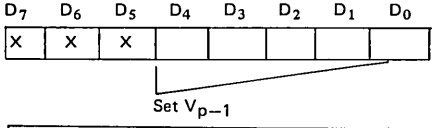
$\overline{CS}$	RS	Address register 3	2	1	0	Register	Register name	READ	WRITE	Data bit 7	6	5	4	3	2	1	0
H	X	X	X	X	X		Invalid	–	–								
L	L	X	X	X	X	AR	Address register	X	o	X	X	X	X				
L	H	L	L	L	H	R_1	Horizontal display character count	X	o	X							
L	H	H	L	L	H	R_9	Maximum raster address	X	o	X	X	X					
L	H	H	L	H	L	R_{10}	Cursor start raster	X	o	X	B	P					
L	H	H	L	H	H	R_{11}	Cursor end raster	X	o	X	X	X					
L	H	H	H	L	L	R_{12}	Start address (H)	o	o	X	X						
L	H	H	H	L	H	R_{13}	Start address (L)	o	o								
L	H	H	H	H	L	R_{14}	Cursor (H)	o	o	X	X						
L	H	H	H	H	H	R_{15}	Cursor (L)	o	o								

Note 1: B denotes cursor blinking, and P denotes the blinking cycle period.
Note 2: "00" is read if registers marked X are read.

2. R9, R10, & R11 Register Re-Reading Function

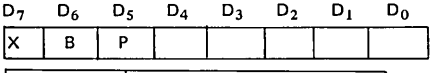
The maximum raster register (R9), cursor start raster (R10), and cursor and raster (R11) are re-read in the following way when the MONO input pin is switched to "H". Normal operation when "L".

- Maximum raster address (R9)



R9 setting	R9 re-reading
0 ~ 7	0 to 7 (according to setting)
8 ~ 1F(H)	Fixed at 7

- Cursor start raster (R10)



R10 setting	R10 re-reading
0 ~ 6	0 to 6 (according to setting)
7 ~ 1F(H)	Fixed at 6

- Cursor end raster (R11)

R11 setting	R11 re-reading
0 ~ 7	0 to 7 (according to setting)
8 ~ 1F	Fixed at 7

Note: Since MSM6265 has been fixed at 1/100 duty × 2, the 25-line structure will no longer be possible if V_p exceeds 8. If this function is used, 25-line displays can be achieved even if $V_p > 8$ is set by the CRTC application software.

3. 40-Character Mode

If the 640D input pin is set to "H", memory addresses for 40 characters per horizontal line are output to $MA_0 \sim MA_{13}$ regardless of the R1 contents. Pattern data equivalent to 80 characters per horizontal line is fetched.

Normal when "L". See time chart in Figures 9 and 11.

4. Display Off Function

Whenthe DINH input pin is set to "L", 0 is output by $UD_0 \sim UD_3$ and $LD_0 \sim LD_3$, resulting in the display being switched off. This function is useful in cases where the power supply is switched on, and where the display is to be left off for relatively long periods of time. Leave set to "H" when the function is not to be used.

5. External Clock Operation

Operation by external clock is enabled when the $\overline{DIV}$ input pin is set to "H". The external clock is applied to $\overline{XT}$ input.

The crystal oscillator is used when the pin is left at "L".

6. Address Output Floating

$MA_0 \sim MA_{13}$ and $RA_0 \sim RA_4$ are switched to high impedance when the ADF input pin is set to "L". This function can be used when the memory bus is opened to other than LCDC (for example to drawing cycle from refresh cycle).

7. Power Down Function

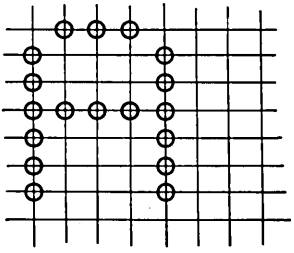
The LCDC generates the $CE\phi$ output signal for chip select of the segment driver. This $CE\phi$ signal is connected to the ECLK input of MSM5279GS. Note that this function can only be used when in 4-bit parallel output mode. See the time chart in Figure 13.

8. Expansion Mode

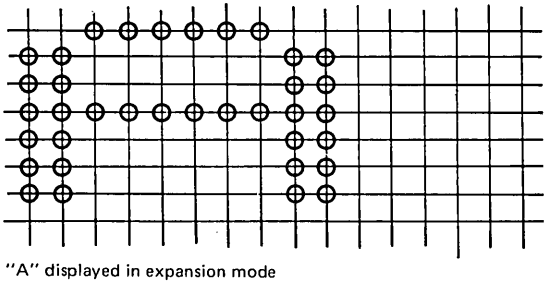
The shift clock count is doubled when "H" is applied to the WIDE input pin. Normal mode, when "L" is applied. In this mode, the clock frequency has to be changed.

Example: When 40-characters per line has been set
The number of display dots in the horizontal direction is changed to 640.

The difference between 80-characters per line in normal mode and 40-characters per line in expansion mode is outlined in the following diagram.



"A" displayed in normal mode



"A" displayed in expansion mode

The data transfer time charts are shown in Figures 3 and 4.

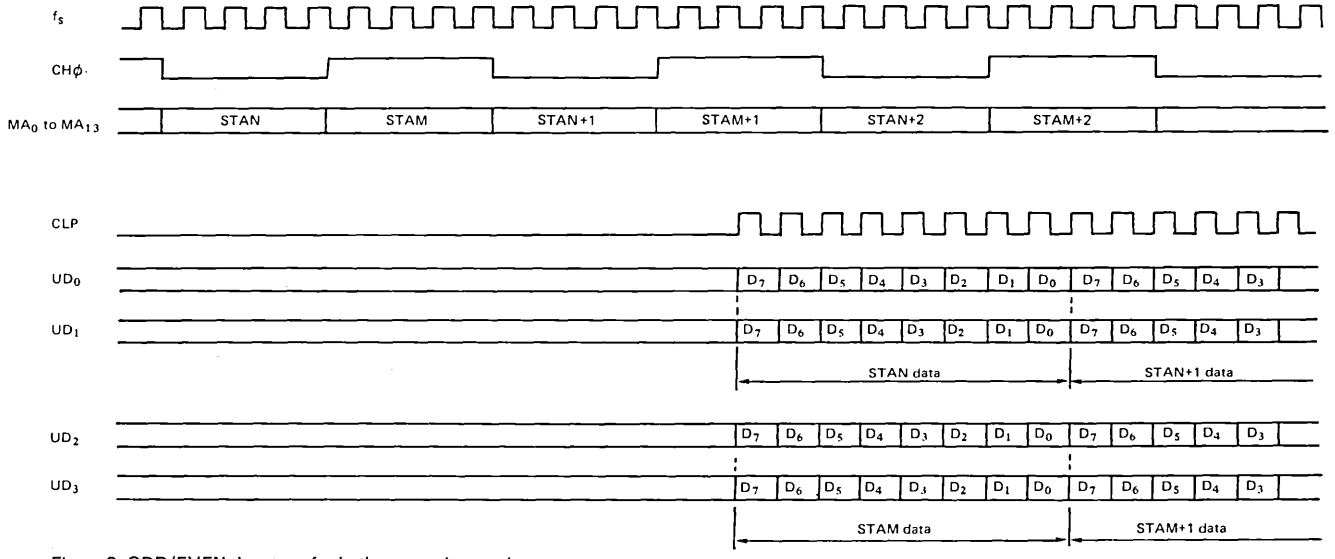


Figure 3 ODD/EVEN data transfer in the expansion mode

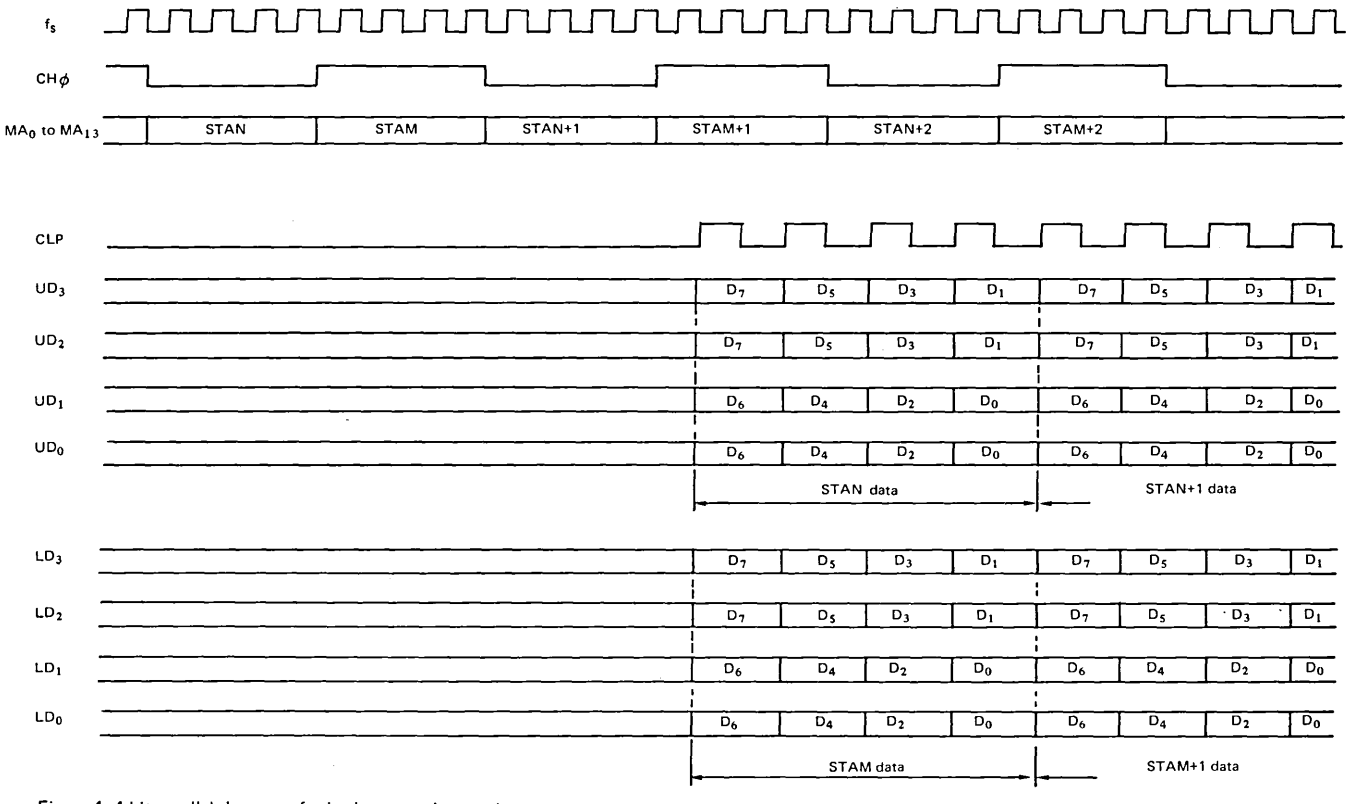


Figure 4 4-bit parallel data transfer in the expansion mode

9. Refresh Memory Address ($MA_0 \sim MA_{13}$) Operation

1) $MA_0 \sim MA_{13}$ Operation

In the horizontal direction, the MAxx output is synchronized with the $CH\phi$ trailing edge. And although MAxx is counted up even if the horizontal display character count is exceeded, this does not effect the display since no data is being transferred at the time. The interval in which data transfer is stopped corresponds to eight characters, and when that interval is exceeded, a single horizontal cycle is completed and the next cycle is commenced. Memory address operation is as indicated in Figure 5 below.

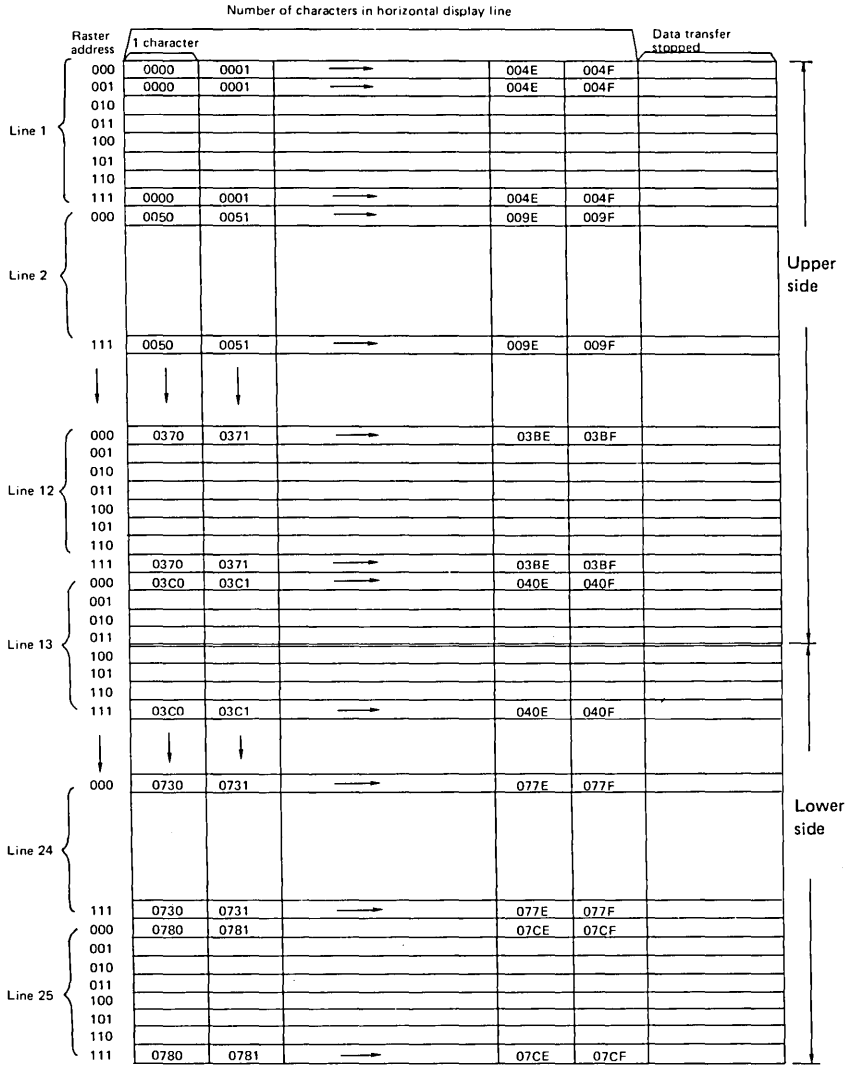


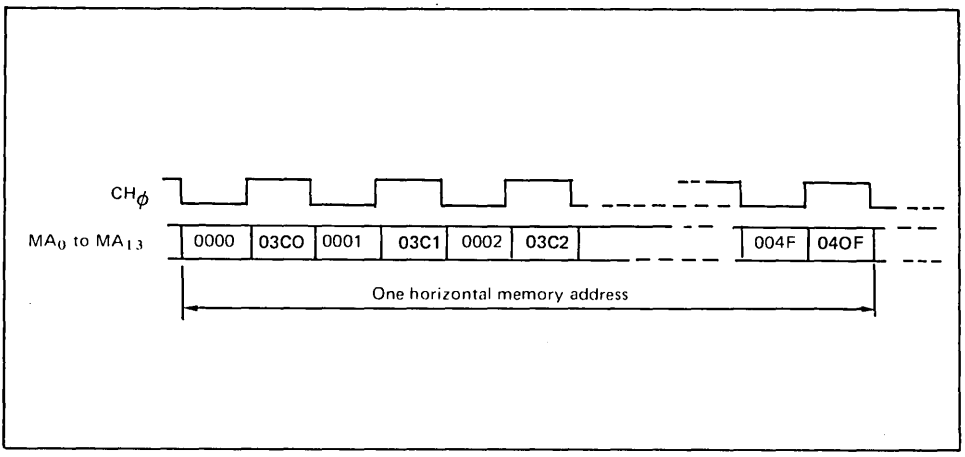
Figure 5 Refresh memory address ($MA_0 \sim MA_{13}$)

Note: When start address is 0000, 80 characters x 25 lines, Vp = 8.

2) Upper and Lower Screen Division

Since the screen is divided into upper and lower halves, MAxx for the upper side and MAxx for the lower side are sent by LCDC.

- **Simultaneous output of upper and lower screen halves**
  The upper and lower screen half addresses are sent upon being switched within a single character period. The upper side address is sent when the CHϕ is "L" while the lower side address is sent when CHϕ is "H".

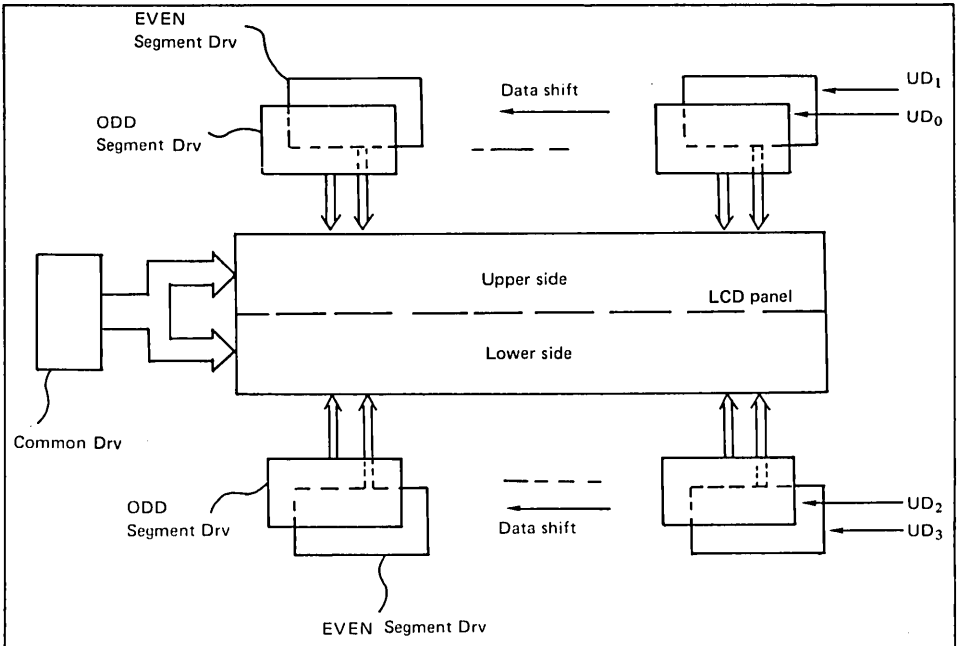


10. Output Mode Setting

Output mode is set by the 4B/ODEV input pin.

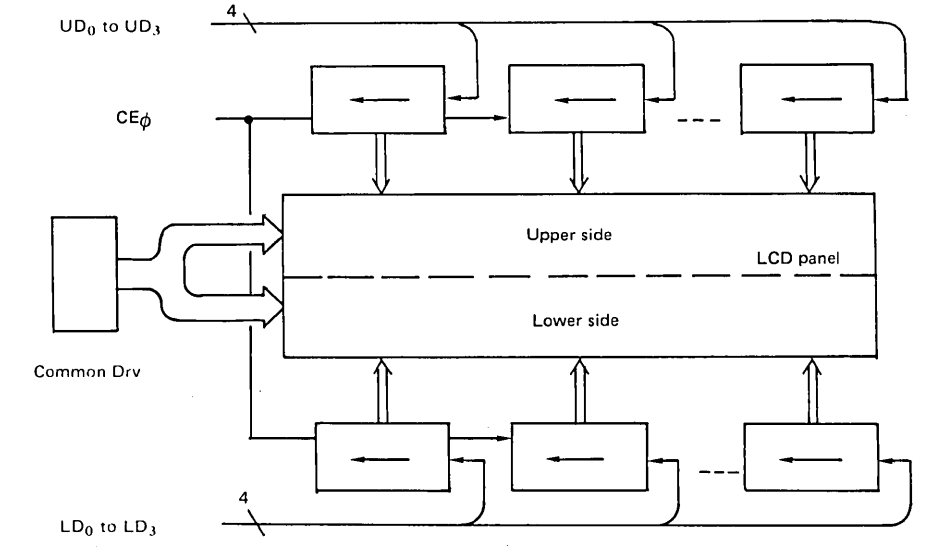
No.	4B/ODEV	Output mode
Mode 1	L	Simultaneous output of upper side and lower side data under 2-bit parallel data processing mode.
Mode 2	H	Simultaneous data output of upper side and lower side data under 4-bit parallel data processing mode.

The time charts for modes 1 and 2 are shown in Figure 10 ~ Figure 13.



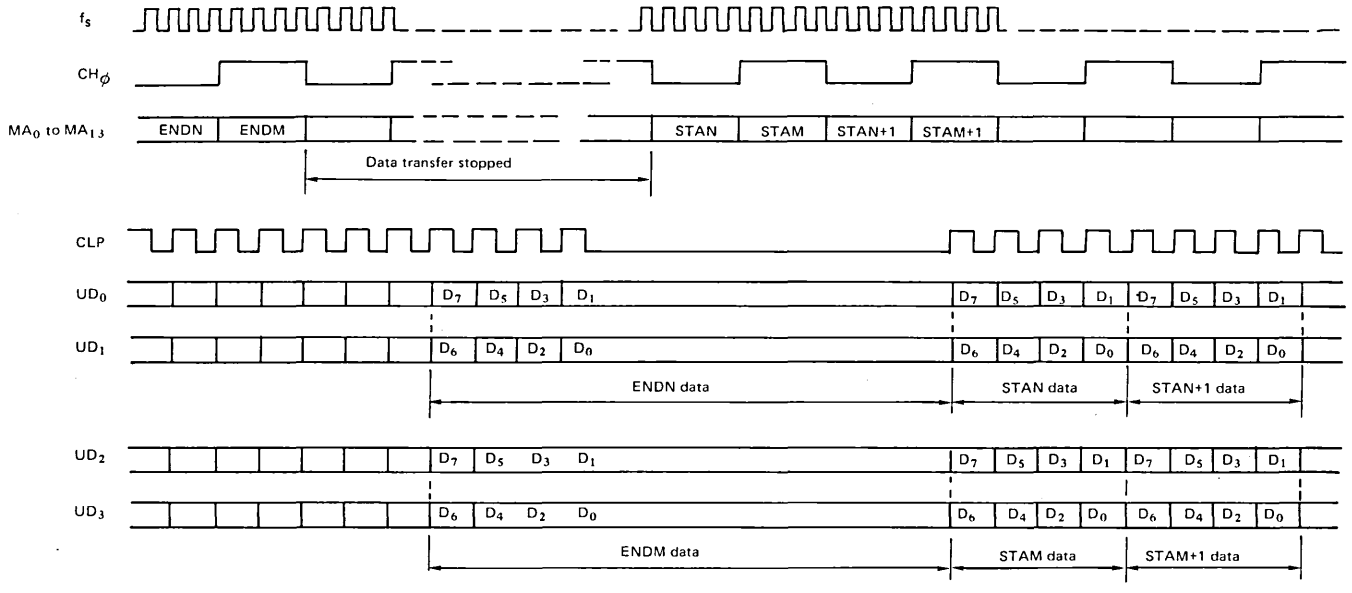
Note: MSM5260GS is used for the segment and common drivers. See Figure 8 and Figure 9 for the time chart.

Figure 6 Mode 1 data flow



Note: MSM5279GS is used for the segment driver, and MSM5278GS is used for the common driver. See Figure 10 and Figure 11 for the time chart.

Figure 7 Mode 2 data flow



Note: STAN: Start address of one horizontal line in upper side
ENDN: End address of one horizontal line in upper side
STAM: Start address of one horizontal line in lower side
ENDM: End address of one horizontal line in lower side

Figure 8 Mode 1 memory address and data transfer

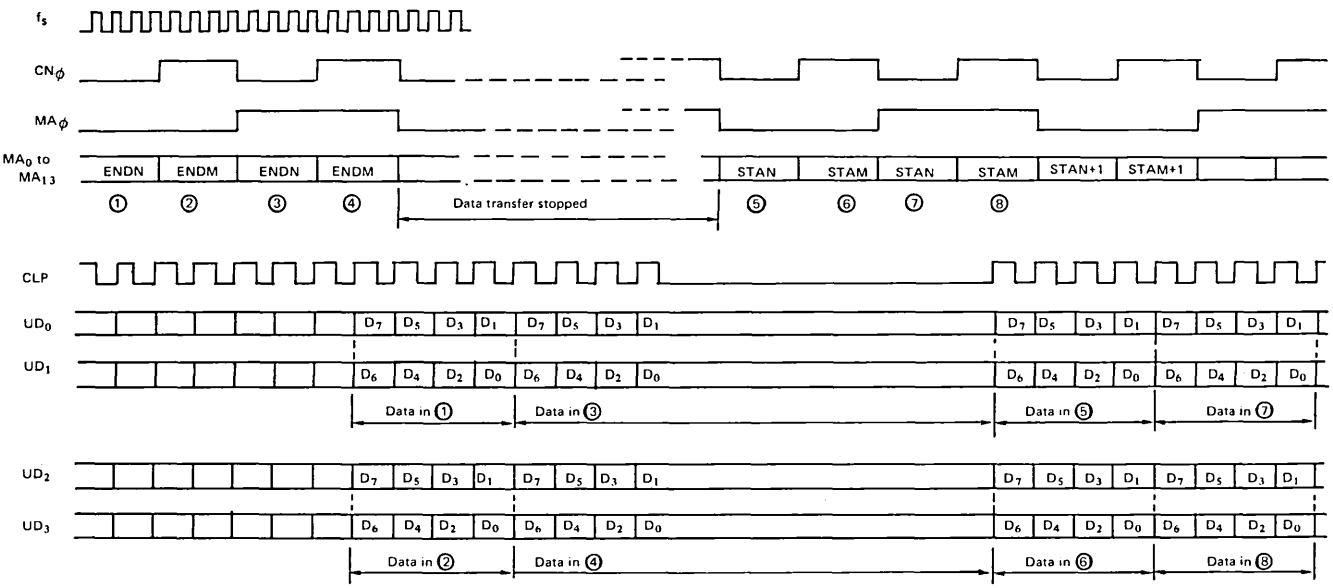


Figure 9 Mode 1 memeory address and data transfer in the expansion mode

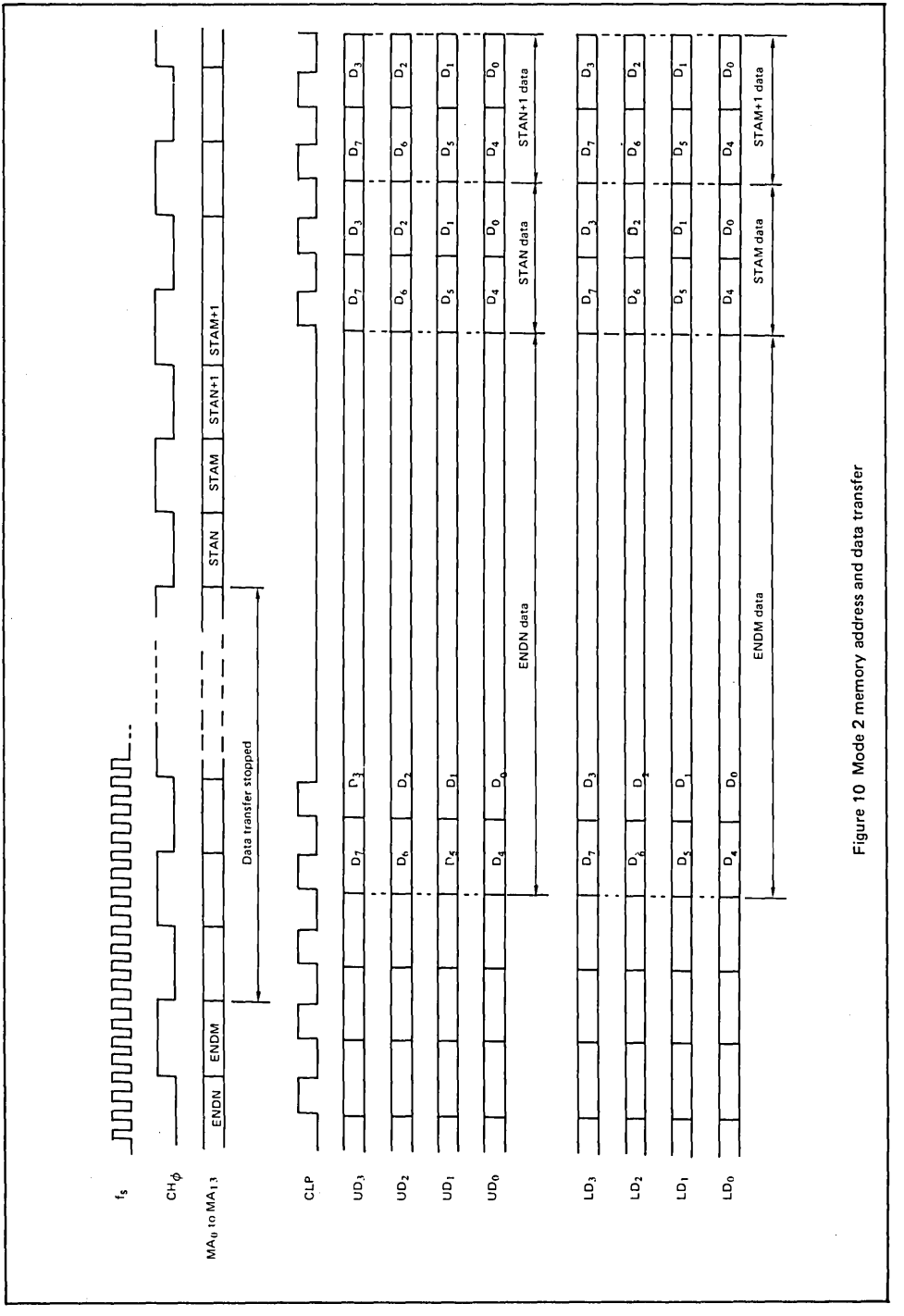


Figure 10 Mode 2 memory address and data transfer

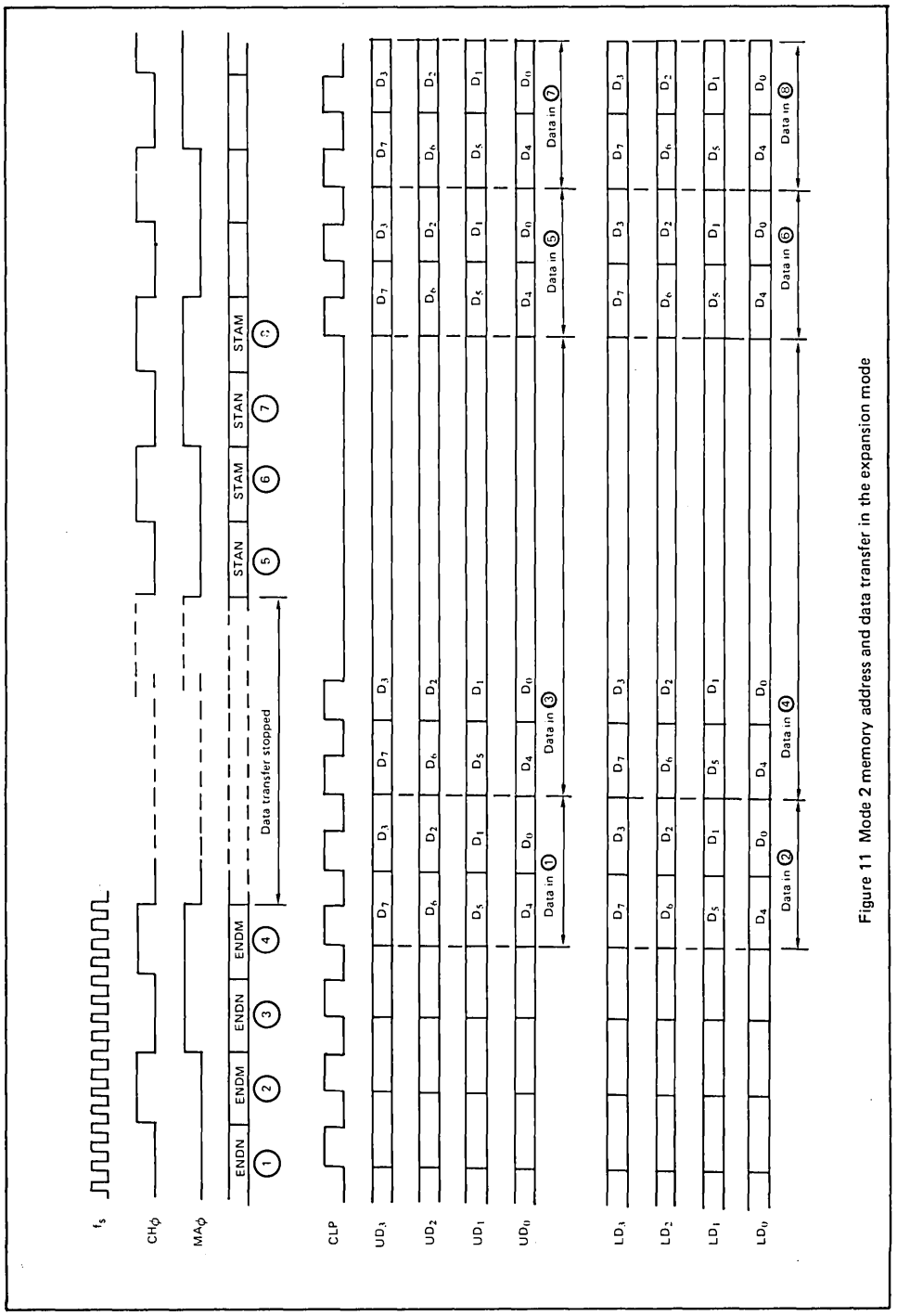


Figure 11 Mode 2 memory address and data transfer in the expansion mode

11. Relation between Duty and Number of Lines

Duty is fixed at 1/100 X 2. The screen is divided into upper and lower halves. The number of lines is determined according to the following equation.

Number of lines (number of characters in vertical display) = $200/V_p$

Note: V_p is the vertical pitch for 1 font (R9 contents)

Example 1. 25 lines when $V_p = 8$

Example 2. 20 lines when $V_p = 10$

Example 3. When $V_p = 14$ is set, only two rasters of contents are displayed in the line 8 font.

12. H_p Setting

The horizontal pitch H_p for 1 font is set by input pins $HP_0 \sim HP_2$.

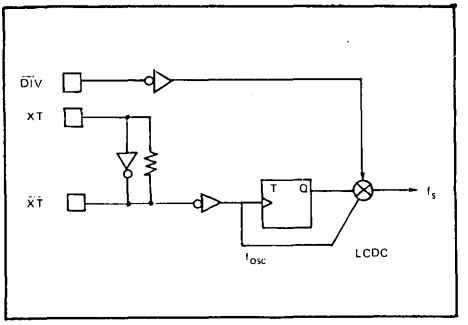
HP_2	HP_1	HP_0	HP
L	H	H	4
H	L	L	5
H	L	H	6
H	H	L	7
H	H	H	8

Note: $H_p = 8$ is fixed in 4-bit parallel output mode. $H_p = 4$ to 8 can only be set in ODD/EVEN output mode.
L denotes GND, and H denotes V_{DD}.

13. Crystal Oscillator Frequency Calculation

External clock or self-oscillation is selected by the $\overline{DIV}$ input pin.

$\overline{DIV}$	Oscillation source
L	Crystal oscillator
H	External clock connected to $\overline{XT}$ input pin.



f_{osc} calculation equation

$f_{osc} = FRP \times (HN + 8) \times H_p \times 1/Duty \times M$

where FRP is the frame frequency,
HN is the horizontal display character count.
HP is the horizontal pitch for 1 font.
8 denotes the data transfer stopped interval, 8 characters per horizontal line, and
M = 2 when $\overline{DIV}$ is L
M = 1 when $\overline{DIV}$ is H

Example of crystal oscillator Frequency Calculation

Calculation of output modes 1 and 2 with horizontal display character count of 80 characters, HP of 8, V_p of 8, and 1/duty = 100.
Substitute FRP = 70 Hz, HN = 80, Hp = 8, 1/duty = 100, and M = 2 into the equation.
f_{osc} = 9.856 (MHz)

14. Character Clock (CH_ϕ) Frequency Calculation

$CH_\phi = FRP \times (HN + 8) \times 1/Duty$

Example: FRP = 70 Hz, HN = 80, and 1/Duty = 100
CHO = 70 X 88 X 100 = 616 (KHz)
= 1.62 (μs) (approx.)

Note: The CH_ϕ cycle period is not related to output mode.

15. Shift Clock (CLP) Frequency Calculation

If the same conditions as in the f_{osc} calculated are used,
CLP = fs/2 = 2.464 (MHz) (Output mode 1)
CLP = fs/4 = 1.232 (MHz) (Output mode 2)

16. LCD Driver Interface

Signals related to the LCD driver include FRP, FRMB, CLP, CE_ϕ, and LIP. The time charts for these signals are shown in Figures 13 and 14.

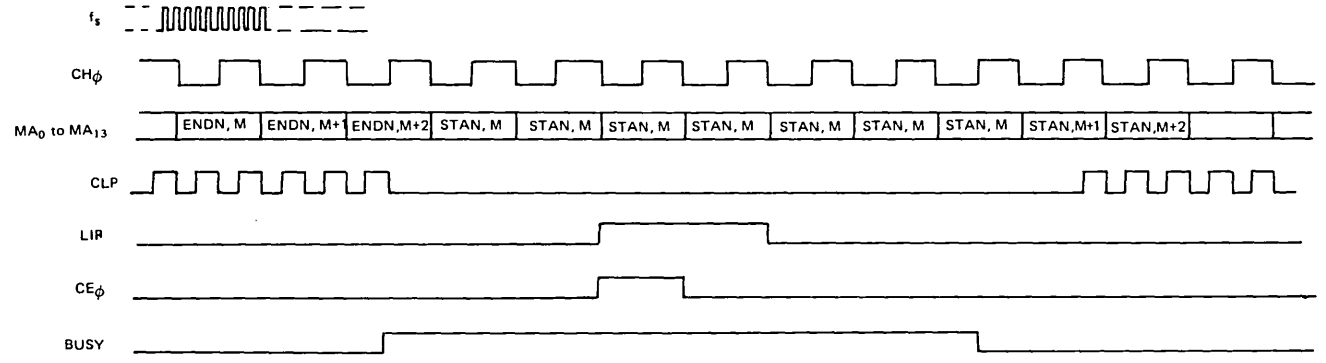


Figure 12 Mode 2 data transfer stop interval

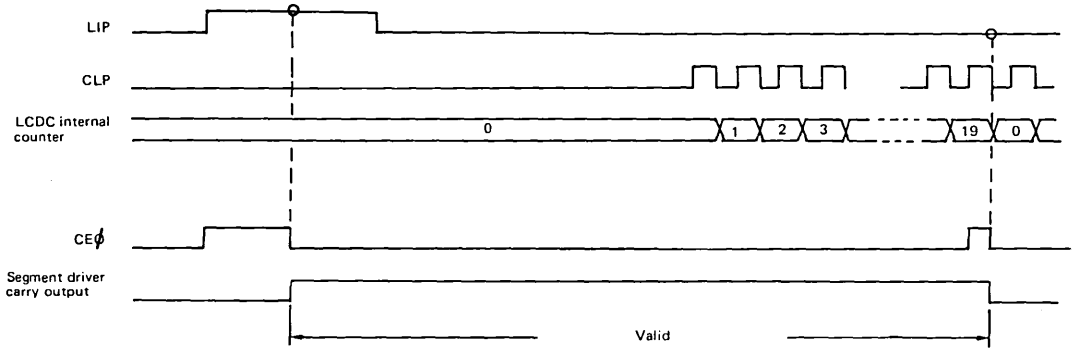


Figure 13 POWER DOWN time chart

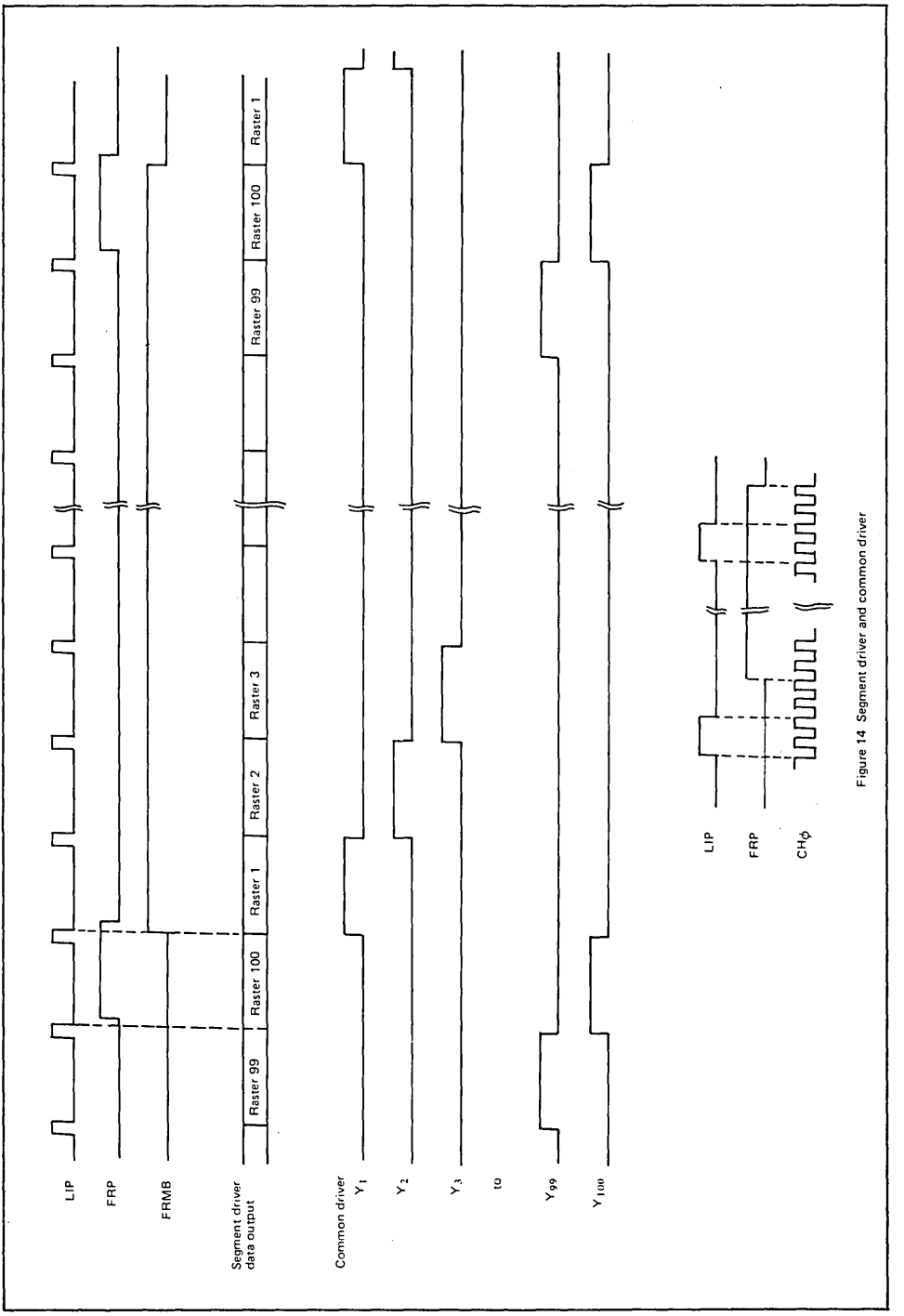


Figure 14 Segment driver and common driver

APPLICATION NOTE

1. Mono-Chro Mode

Only character mode is available in Mono-Chro mode. There is no graphic mode in this mode. Description of character mode is described as follows.

Character box : 8 x 8
Character font : According to the CGROM contents
Shape of cursor : 2 rasters
Display : 80 characters x 25 lines

- **Character box**

Horizontal pitch of the font is determined by $HP_2 \sim HP_0$. In the mono-chro mode, all of $HP_2 \sim HP_0$ should be set at "H" level and this determines the horizontal pitch at 8. Since the number of horizontal dot of the LCD is fixed at 640 dots, 80 characters/line can be displayed on the LCD panel.
Vertical pitch of the font is determined by R_9 contents. In the mono-chro mode, the vertical pitch of the font should be set at 8. Since the number of vertical dot of the LCD is fixed at 200 dots, 25 lines are displayed on the LCD. Even if the vertical pitch is set at 14*, it will be read as 8 when MONO input pin is set at "H" level.

* In the case of CRT display control by HD6845, vertical pitch is set at 14.

- **Character font**

The construction of character font can be changed according to the CG ROM contents. The pattern data has to be written into so that it can meet the character box.

- **Shape of cursor**

The shape of cursor is determined by R_{10} and R_{11} contents. Since the vertical pitch (14) is read as 8, the R_{10} and R_{11} contents have to be re-read.
Setting MONO input pin at "H" enables this re-reading as follows.

(example)

MSM6265			CRT Software
R_{10} : 6	←	R_{10}	: B
R_{11} : 7	←	R_{11}	: C

- **Attribute**

In this mode following attribute functions are available.

Character inversion, Display off, Under-line, Cursor On/Off/Blink

These attribute functions are determined by the external circuit, however, the contents of these attribute functions are stored in the attribute RAM.
In the Figure 15, writing data into the attribute RAM and character code RAM is effected by assigning the even number address to the character code and odd number address to the attribute function after selecting A_0 of the address bus from the CPU.
In reading out the data, 2-bytes are read out simultaneously.

Memory Address
B0000 Character code
B0001 Attribute
B0002 Character code
B0003 Attribute
. .
. .
. .

- **Cursor blink**

The cursor blink frequency should be supplid from the external source to EXBL.

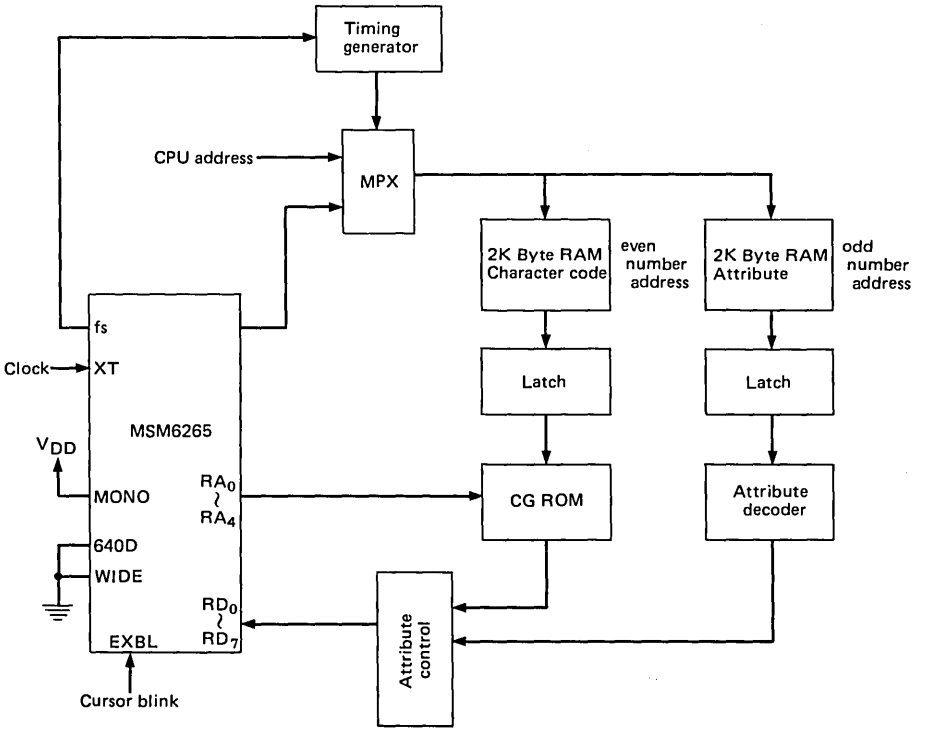


Figure 15 Mono-Chro mode (80 characters x 25 lines)

2. Color Mode

Both character mode and graphic mode are available in the color mode.

1) Character mode

Character box	: 8 x 8
Character font	: 5 x 7 or 7 x 7
Shape of cursor	: 2 rasters
Display	: 80 characters x 25 lines or 40 characters x 25 lines (display expasion mode)

The registers which determine the vertical pitch and the shape of cursor are determined as follows.

R_9 : 07, R_{10} : 06, R_{11} : 07

So, MONO input pin can be either "H" or "L".

- **40 characters x 25 lines display**

The shape of displayed characters have to be horizontally enlarged double to enable 40 characters/line display. To enable 40 characters/line display, WIDE input pin has to be set at "H" level. In this mode, however, the clock frequency has to be changed.

(example)

$f_{(OSC)}$ is calculated by following formula.

$f_{(OSC)}=F_{RP}x(H_N x8)xHPx1/DUTYxM$

$f_{(OSC)}$ is 4.928 MHz when F_{RP} = 70 Hz, H_N = 80, H_p = 8, DUTY = 1/100 and M = 1. So, if H_N is changed to 40, $f_{(OSC)}$ has to be changed to 2.464 MHz to maintain other conditions.

2) Graphic mode

640 dots x 200 dots graphic display is enabled if the vertical pitch is set at 2 and number of horizontal characters is set at 40. In this case, the constructure of the display buffer address are described in Figure 16.

If 8K byte is assigned to the even number address and odd number address respectively as CPU address, a signal is necessary for the RAM address signal. This signal (MA_ϕ) is provided when 640D input pin is set at "H" level. Figure 17 shows an example of system configuration in the color mode.

RA_0	MA_{11} MA_{10} MA_9 MA_8	MA_7 MA_6 MA_5 MA_4	MA_3 MA_2 MA_1 MA_0

Figure 16

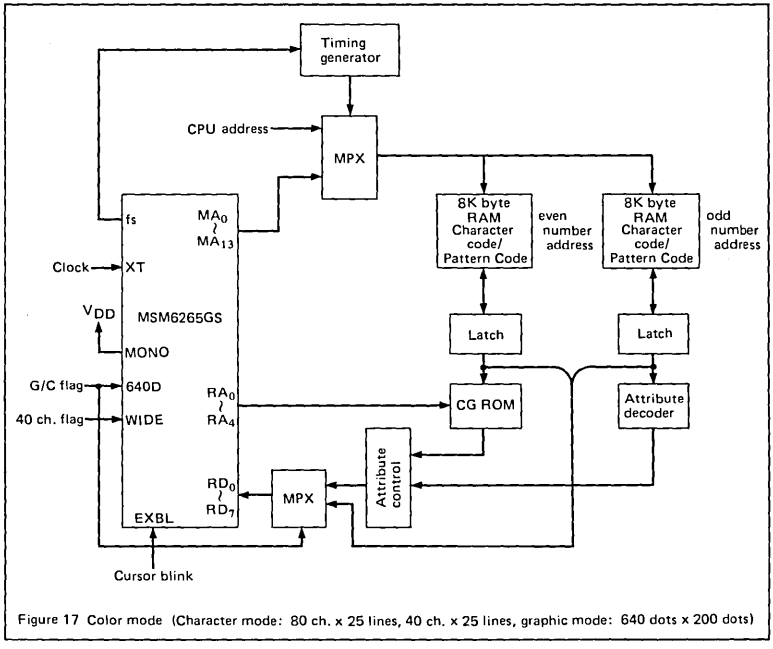


Figure 17 Color mode (Character mode: 80 ch. x 25 lines, 40 ch. x 25 lines, graphic mode: 640 dots x 200 dots)

3. DISPLAY METHOD

V-RAM is provided in the system configuration. So, inadequate access of CPU to the V-RAM results flickers on the display. Therefore, refresh cycle and CPU cycle should come alternatively, in other words, without omitting the refresh cycle, the V-RAM is accessed. This is commonly called the "Cycle Steal Method". Figure 18 shows the timing chart.

Writing data into V-RAM has to be done during the course of the CPU cycle. So, external circuit is necessary to generate timing for $\overline{WR}$ signal. In reading the data of the V-RAM, the data bus has to be latched as the address bus is changing alternatively. Figure 19 shows an example circuit.

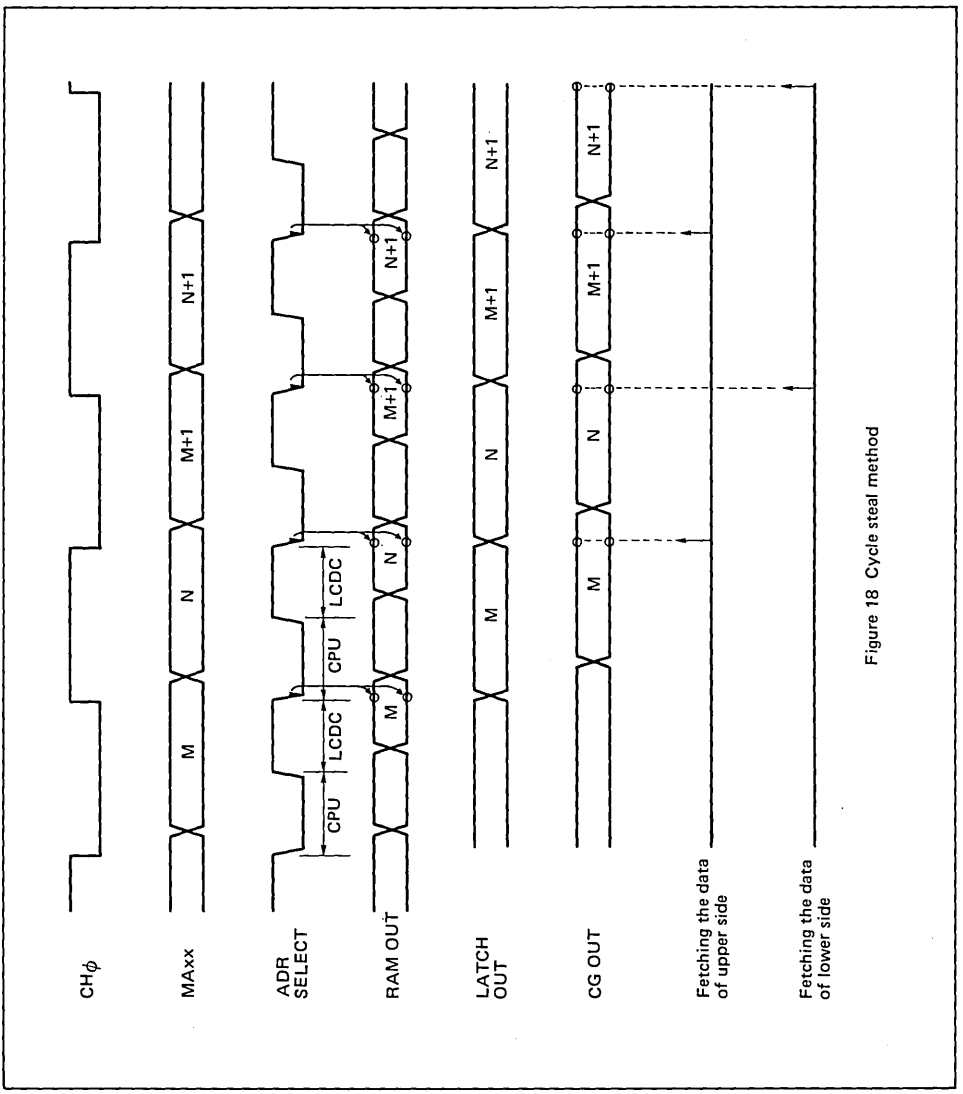


Figure 18 Cycle steal method

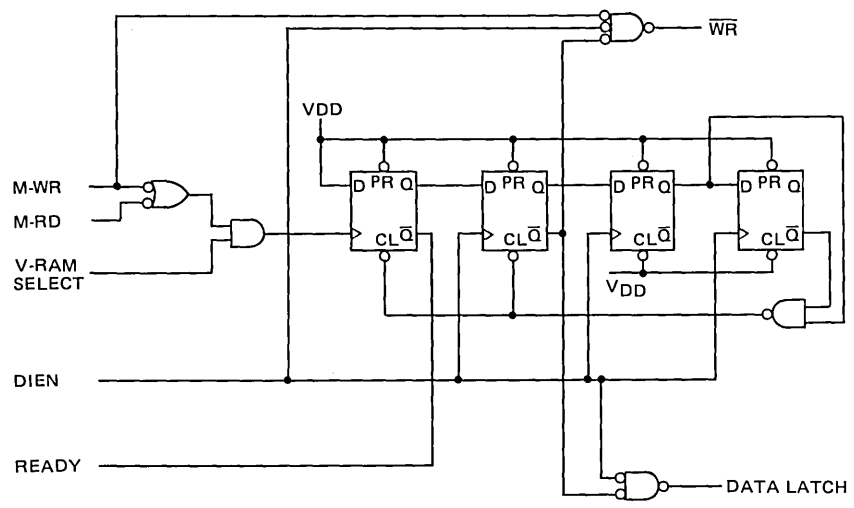


Figure 19 Wait control circuit

Legend

Symbol	Function
M-WR	Write signal to V-RAM from CPU
M-RD	Read signal to V-RAM from CPU
V-RAM SEL	Address bus of CPU is decoded and being output
ADR SEL	Address bus switching signal, 1/4 of fs signal is to be output
READY	Signal which let the CPU to wait
$\overline{WR}$	Write signal of V-RAM
DATA LATCH	Signal to latch the data output from V-RAM

All specifications and details published are subject to change without notice.

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