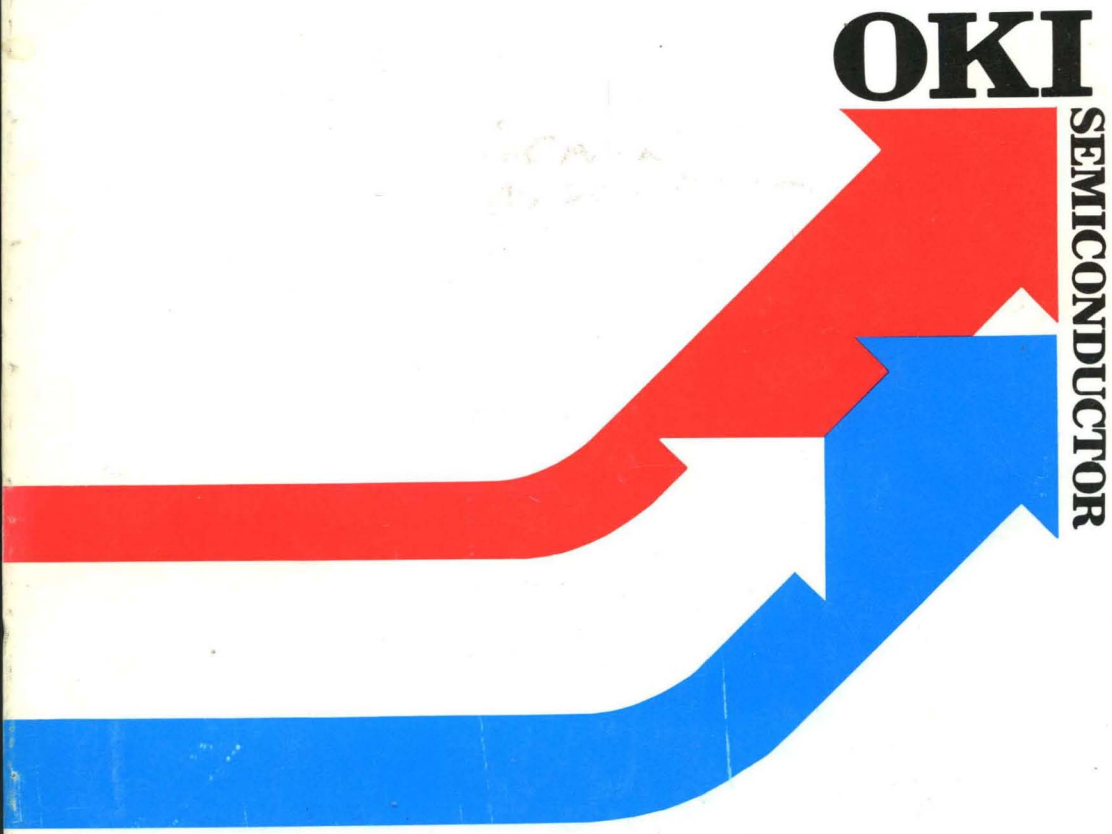
MEMORY DATABOOK 1986



First Edition: July 1986

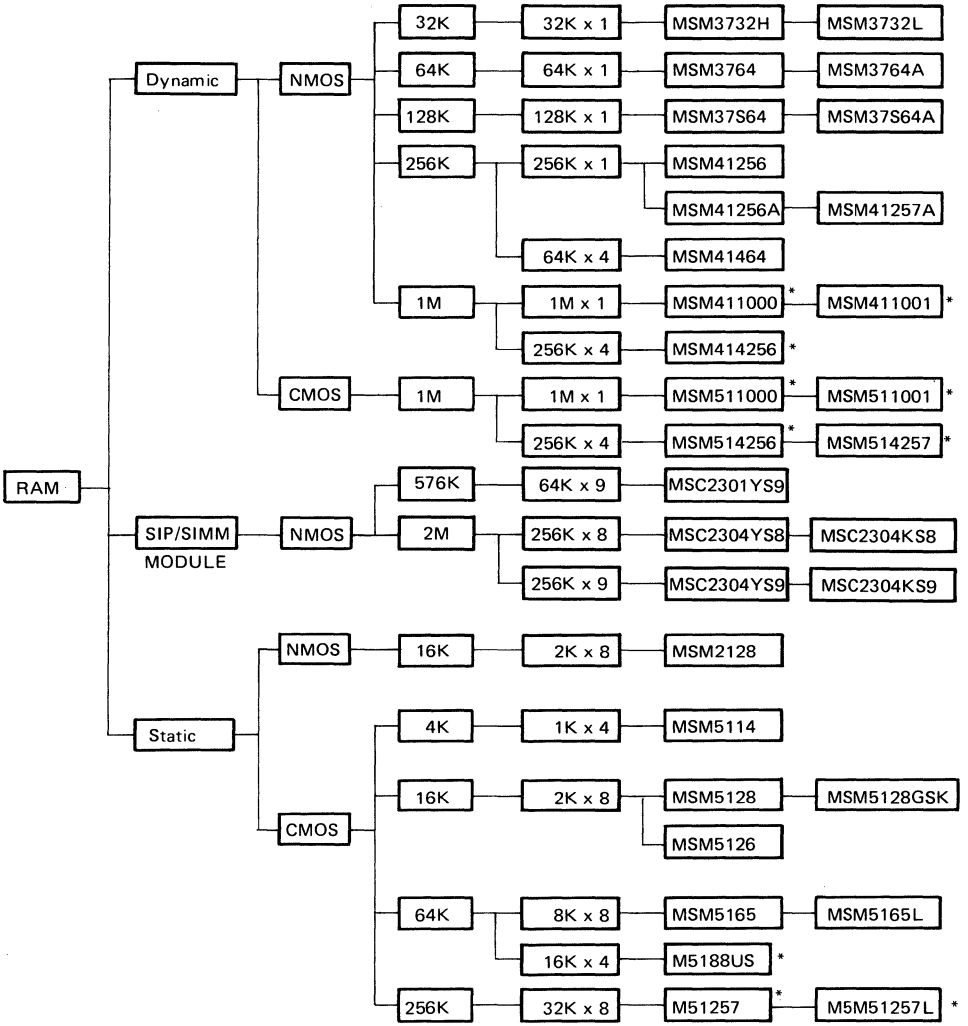
MEMORY DATABOOK 1986

CONTENTS

1 IC MEMORY LINE-UP AND TYPICAL CHARACTERISTICS

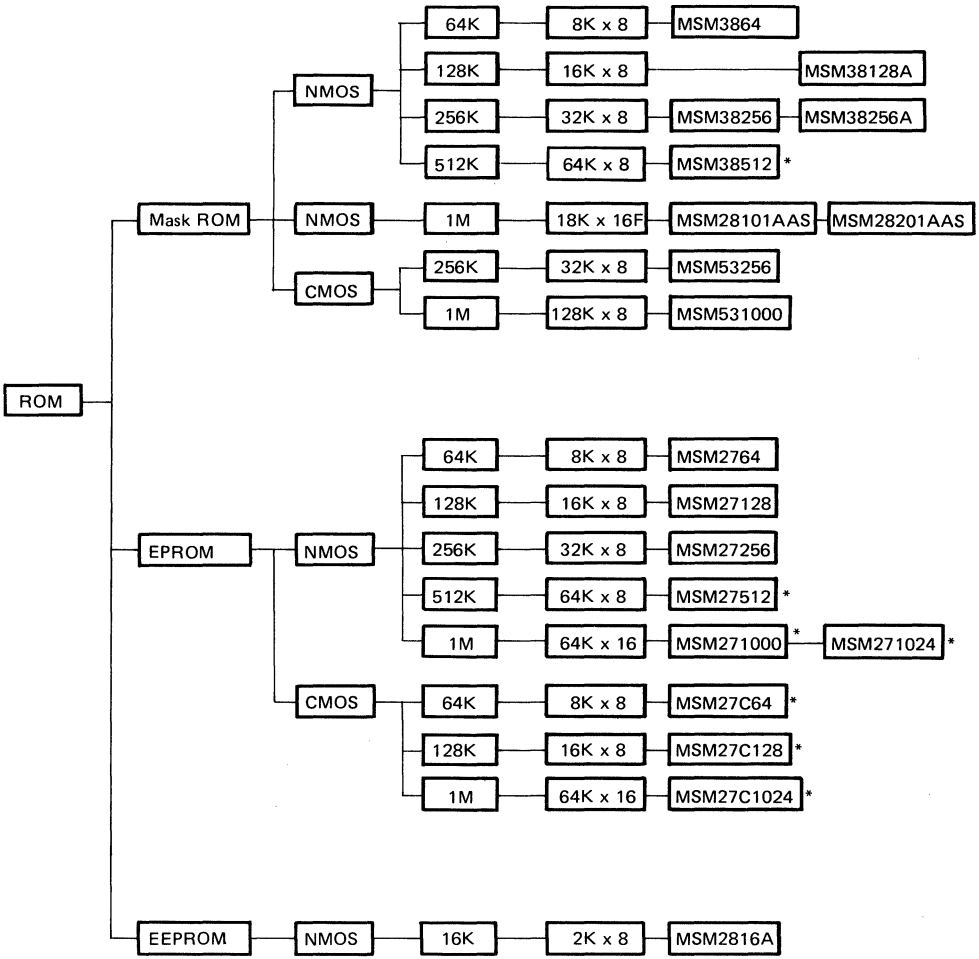
1

IC MEMORY LINE-UP AND TYPICAL CHARACTERISTICS



*Under development

■ IC MEMORY LINE-UP AND TYPICAL CHARACTERISTICS ■



*Under development

• DYNAMIC RAMS

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM3732H-15	32k	16 Pin Dynamic A7 (Column)=H	32,768x1	16	150	270	248/28	+5	
MSM3732H-20					200	330	248/28		
MSM3732L-15	32k	16 Pin Dynamic A7 (Column)=L	32,768x1	16	150	270	248/28	+5	
MSM3732L-20					200	330	248/28		
MSM3764-15	64k	16 Pin Dynamic	65,536x1	16	150	270	248/28	+5	TMS4164-15
MSM3764-20					200	330	248/28		TMS4164-20
MSM3764A-12	64k	16 Pin Dynamic	65,536x1	16	120	230	330/28	+5	
MSM3764A-15					150	260	330/28		
MSM3764A-20					200	330	330/28		
MSM41256-15	256k	16 Pin Dynamic	262,144x1	16	150	260	385/28	+5	
MSM41256-20					200	330	385/28		
MSM41256A-10	250k	16 Pin Dynamic	262,144x1	16	100	200	385/28	+5	
MSM41256A-12					120	220	385/28		
MSM41256A-15					150	260	385/28		
MSM41257A-10	256k	16 Pin Dynamic	262,144x1	16	100	200	385/28	+5	
MSM41257A-12					120	220	385/28		
MSM41257A-15					150	260	385/28		
MSM41464-10	256k	18 Pin Dynamic	65,536x4	18	100	200	385/28	+5	
MSM41464-12					120	230	385/28		
MSM41464-15					150	260	385/28		
MSM414256-10	256k	20 Pin Dynamic	262,144x4	20	100	200	413/28	+5	
MSM414256-12					120	230	385/28		
MSM411000-10	1M	18 Pin Dynamic	1,048,576x1	18	100	200	413/28	+5	
MSM411000-12					120	230	385/28		
MSM411001-10	1M	18 Pin Dynamic	1,048,576x1	18	100	200	413/28	+5	
MSM411001-12					120	230	385/28		
MSM511000-10	1M	18 Pin Dynamic	1,048,576x1	18	100	190	385/11	+5	
MSM511000-12					120	220	330/11		
MSM511001-10	1M	18 Pin Dynamic	1,048,576x1	18	100	190	385/11	+5	
MSM511001-12					120	220	330/11		
MSM514256-10	1M	20 Pin Dynamic	262,144x4	20	100	190	413/11	+5	
MSM514256-12					120	220	385/11		

■ IC MEMORY LINE-UP AND TYPICAL CHARACTERISTICS ■

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM514257-10	1M	20 Pin Dynamic	262.144x4	20	100	190	413/11	+5	
MSM514257-12					120	220	385/11		
MSM37S64-15	128k	16 Pin Dynamic	131,072x1	16	150	270	360/55	+5	
MSM37S64-20					200	330	360/55		

- SIP/SIMM MODULE

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (nw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSC2301-12YS9/KS9	576k	30 Pin Socket Insertable Module	65536x9	30	120	120	—	+5	
MSC2301-15YS9/KS9					150	150	—		
MSC2304-12YS8/KS8	2M	30 Pin Socket Insertable Module	262144x8	30	120	120	—	+5	
MSC2304-15YS8/KS8					150	150	—		
MSC2304-12YS9/KS9	2M	30 Pin Socket Insertable Module	262144x9	30	120	120	—	+5	
MSC2304-15YS9/KS9					150	150	—		

• NMOS STATIC RAMS

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM2128-12	16k	Static, Common I/O with Power Down Mode	2048x8	24	120	120	660/110	+5	TMM2016 M58725
MSM2185-15					150	150	550/110		
MSM2128-20					200	200	550/110		

• CMOS STATIC RAMS

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM5114-2	4k	Fully Static, Common I/O	1024x4	18	200	200	192/0.04	+5	TC5514 μPD444
MSM5114-3					300	300	192/0.04		
MSM5114					450	450	192/0.04		
MSM5128-12	16k	Fully Static, Common I/O	2048x8	24	120	120	330/0.275	+5	HM6116 μPD446 TC5517
MSM5128-15					150	150	300/0.275		
MSM5128-20					200	200	275/0.275		
MSM5126-20	16k	Fully Static Common I/O	2048x8	24	150	150	385/0.165	+5	
MSM5126-25					200	200	385/0.165		
MSM5165-12	64k	Fully Static Common I/O	8192x8	28	120	120	248/5.5	+5	
MSM5165-15					150	150	248/5.5		
MSM5165-20					200	200	248/5.5		
MSM5165L-12	64k	Fully Static Common I/O	8192x8	28	120	120	248/0.55	+5	
MSM5165L-15					150	150	248/0.55		
MSM5165L-20					200	200	248/0.55		
MSM5188-45	64k	Fully Static Common I/O	16384x4	22	45	45	605/11	+5	
MSM5188-55					55	55	605/11		
MSM5188-70					70	70	605/11		
MSM51257-85	256k	Fully Static Common I/O	32768x8	28	85	85	385/5.5	+5	
MSM51257-100					100	100	385/5.5		
MSM51257-120					120	120	385/5.5		
MSM51257L-85	256k	Fully Static Common I/O	32768x8	28	85	85	385/0.55	+5	
MSM51257L-100					100	100	385/0.55		
MSM51257L-120					120	120	385/0.55		

■ IC MEMORY LINE-UP AND TYPICAL CHARACTERISTICS ■

• MASK ROMS

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM3864	64k	Fully Static	8192x8	28	250	250	550/165	+5	
MSM38128A	128k	Fully Static	16384x8	28	250	250	550/165	+5	
MSM38256	256k	Fully Static	32768x8	28	250	250	660/165	+5	
MSM38256A	256k	Fully Static	32768x8	28	150	150	330/33	+5	
MSM38512	512k	Fully Static	65536x8	28	200	200	—	+5	
MSM28101	1M	40 Pin MASK RAM 18x16 Chinese-character font output	3760x16 x 18	40	10μs	22μs	893	+5	JIS-Chinese-character coding system 0~7, 16~47
MSM28201									JIS-Chinese-character coding system 48~87
MSM53256	256k	Fully Static	32768x8	28	150	150	83/0.6	+5	
MSM531000	1M	Fully Static	131072x8	28	250	250	83/0.6	+5	

• EPROMS

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM2764	64k	28 Pin EPROM	8192x8	28	200	200	790/185	+5	2764
MSM27128	128k	28 Pin EPROM	16,384x8	28	250	250	788/184	+5	27128
MSM27256	256k	28 Pin EPROM	32,768x8	28	150	150	525/184	+5	27256
MSM27512	512k	28 Pin EPROM	65,536x8	28	150	150	525/184	+5	27512
MSM271000	1M	32 Pin EPROM	131,072x8	32	120	120	525/184	+5	271000
MSM271024	1M	40 Pin EPROM	65,536x16	40	120	120	525/184	+5	271024
MSM27C64	64k	28 Pin EPROM	8,192x8	28	200	200	165/0.55	+5	27C64
MSM27C128	128k	28 Pin EPROM	16,384x8	28	200	200	165/0.55	+5	27C128
MSM27C1024	1M	40 Pin EPROM	65,536x16	40	100	100	175/0.55	+5	27C1024

• E^2P ROMS

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (nw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM2816A-25	16k	24 Pin E^2P ROM	2048x8	24	250	250	–	+5	
MSM2816A-30					300	300	–		
MSM2816A-35					350	350	–	+5	
MSM2816A-45					450	450	–		

PACKAGING

2

2

PACKAGING

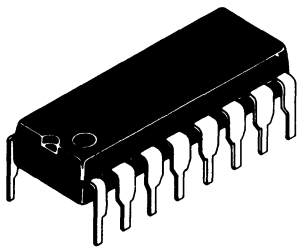
Name	No. of Pins	PACKAGES						
		RS	GS	JS	US	YS	KS	AS
		PLASTIC DIP	PLASTIC FLAT	PLASTIC LCC	PLASTIC SKINNY	MODULE	MODULE	SIDE-BRAZED
MSM3732	16	○						
3764	16	○						
3764A	16	○						
37S64	16	○						
37S64A	16	○						
41256	16	○						
	18			○				
41256A	16	○						
	18			○				
41257A	16	○						
41464	18	○						
	22			○				
411000	18	○						
	26			○				
411001	18	○						
	26			○				
414256	20	○						
	26			○				
511000	18	○						
	26			○				
511001	18	○						
	26			○				
514256	20	○						
	26			○				
514257	20	○						
	26			○				
2128	24	○						
5114	18	○						
5126	24	○						
5128	24	○	○					
5165	28	○						
	32			○				
5165L	28	○						
	32			○				
5188	22				○			
51257	28	○						
	32			○				
51257L	28	○						
	32			○				
3864	28	○						
38128A	28	○						
38256	28	○						
38256A	28	○						
28101A	40							○
28201A	40							○
38512	28	○						
531000	28	○						
53256	28	○						
2764	28							○

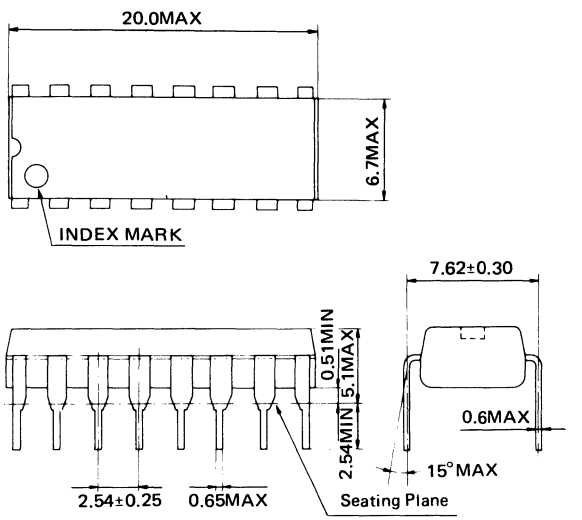
■ PACKAGING ■

2

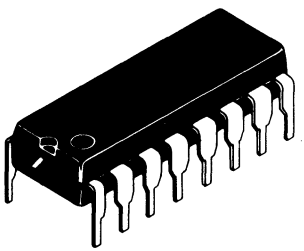
Name	No. of Pins	PACKAGES						
		RS	GS	JS	US	YS	KS	AS
		PLASTIC DIP	PLASTIC FLAT	PLASTIC LCC	PLASTIC SKINNY	MODULE	MODULE	SIDE-BRAZED
27128	28							○
27256	28							○
27512	28							○
271000	32							○
271024	40							○
27C64	28							○
27C128	28							○
27C1024	40							○
2816A	24	○						
2301	30					○	○	
2304	30					○	○	

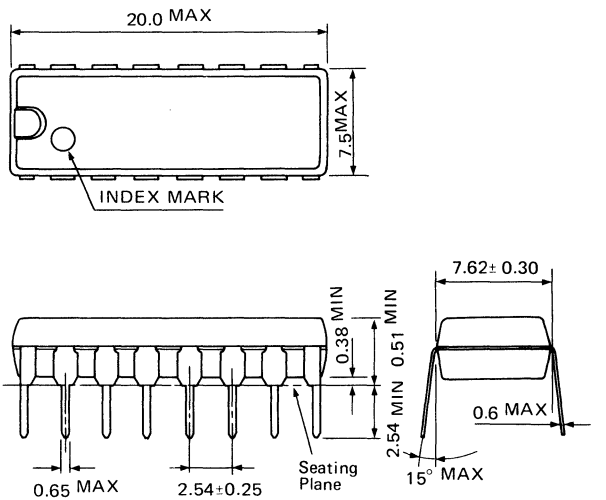
• 16 PIN PLASTIC





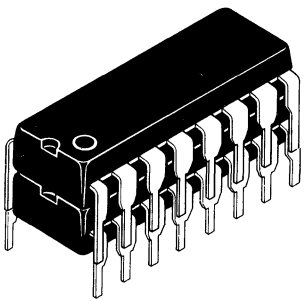
• 16 PIN PLASTIC

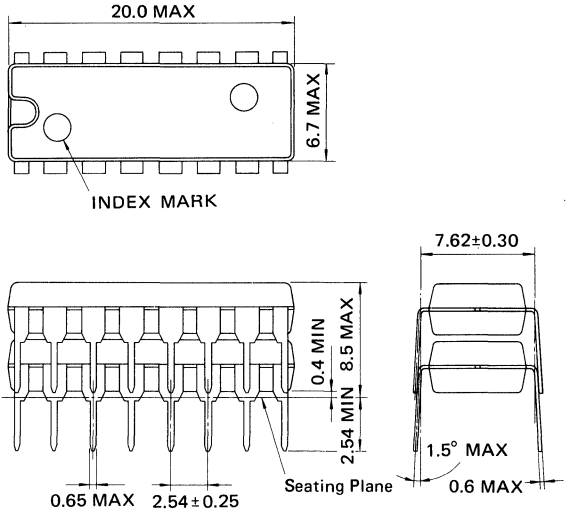




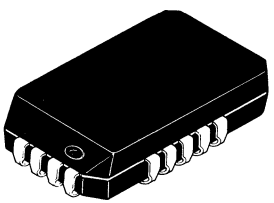
Note: All dimensions in millimeters.

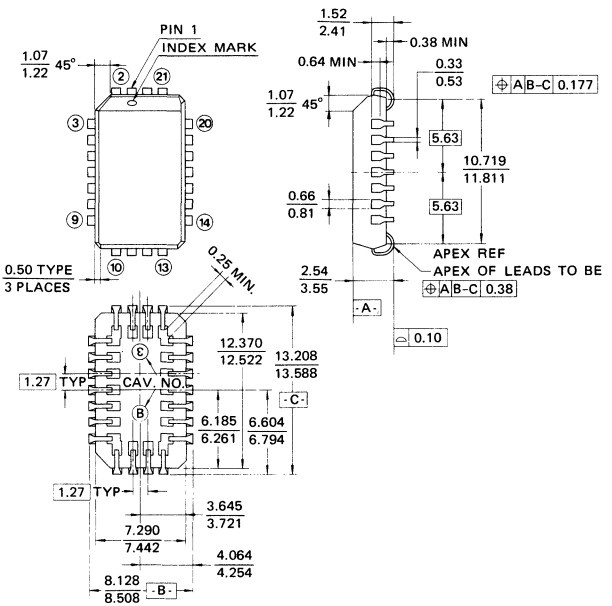
• 16 PIN STACK PLASTIC



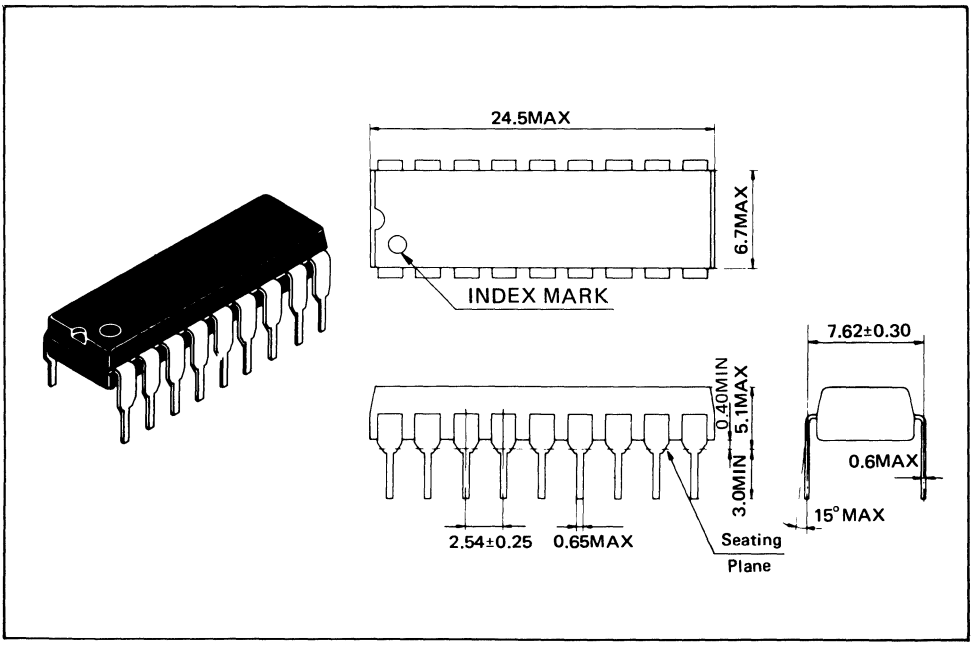


• 18 PIN PLCC

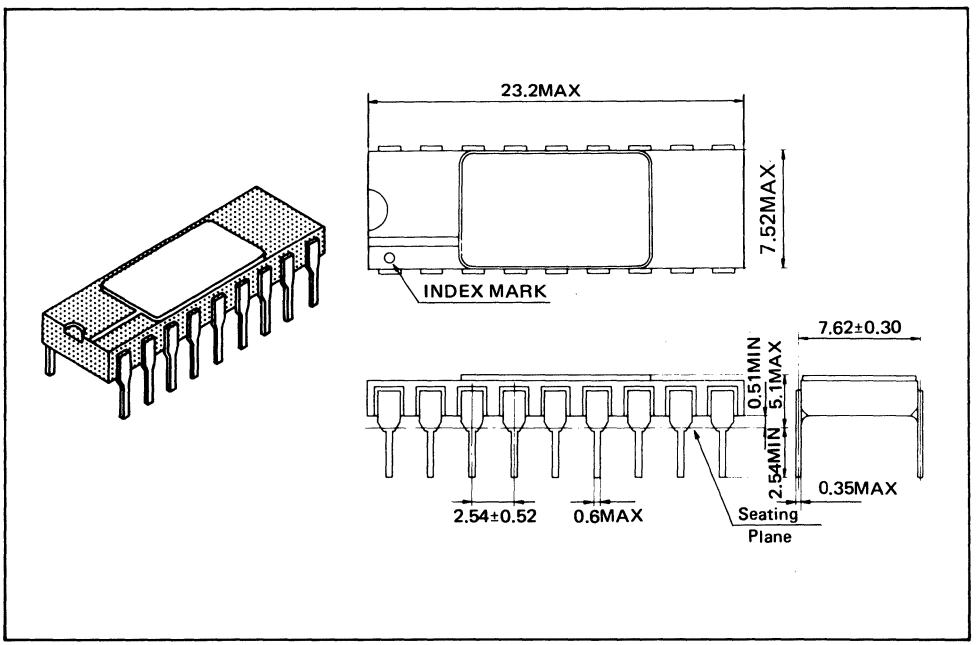




• 18 PIN PLASTIC



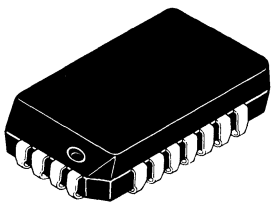
• 18 PIN SIDE-BRAZED

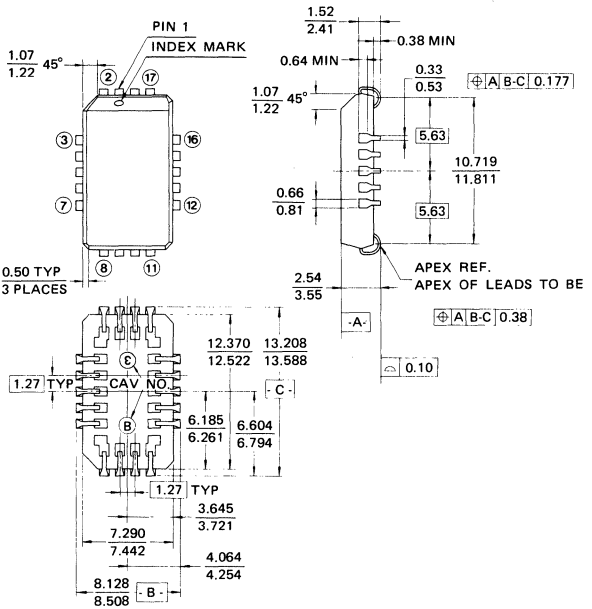


Note: All dimensions in millimeters.

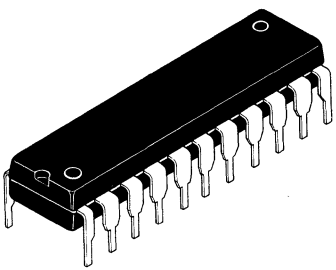
2

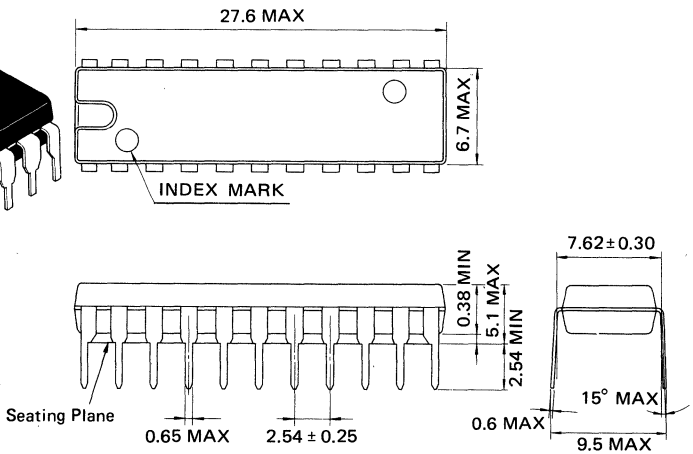
• 22 PIN PLCC



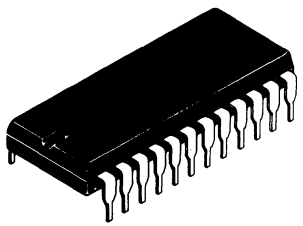


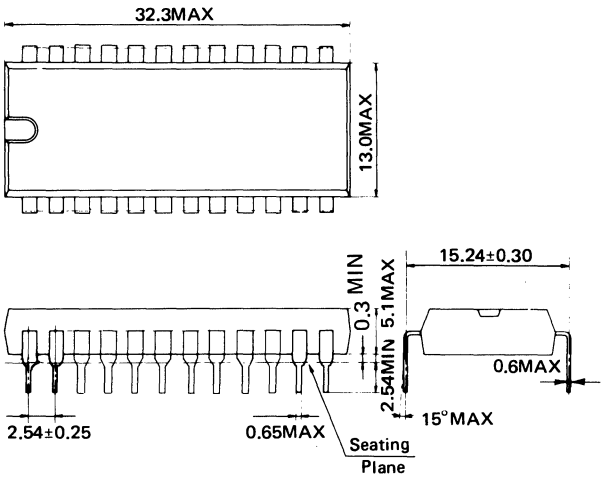
• 22 PIN PLASTIC



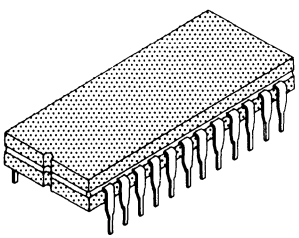


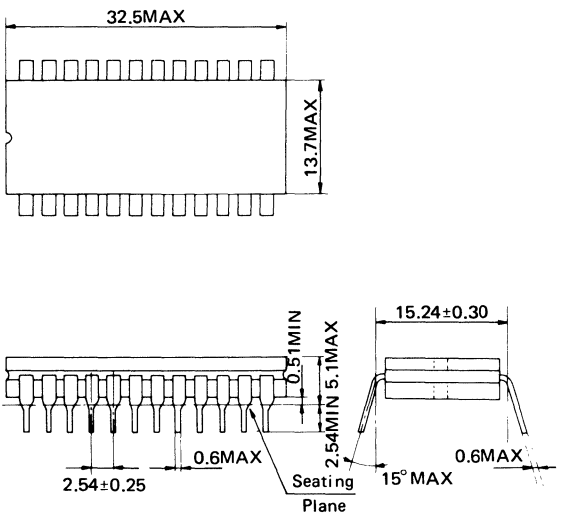
• 24 PIN PLASTIC





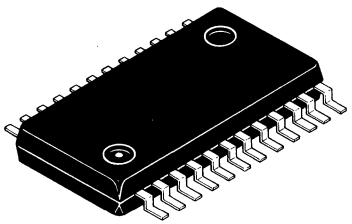
• 24 PIN CERDIP

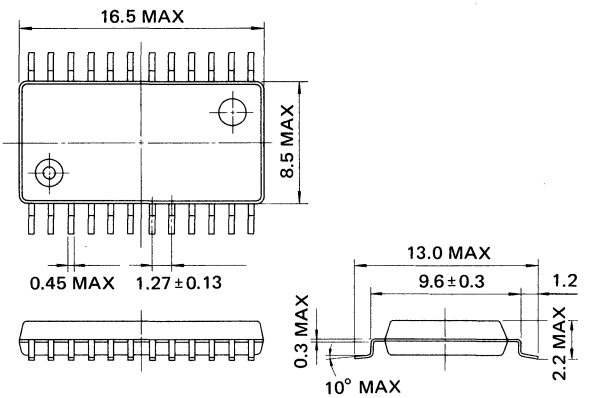




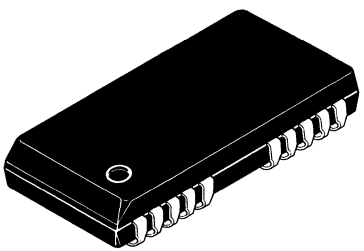
Note: All dimensions in millimeters.

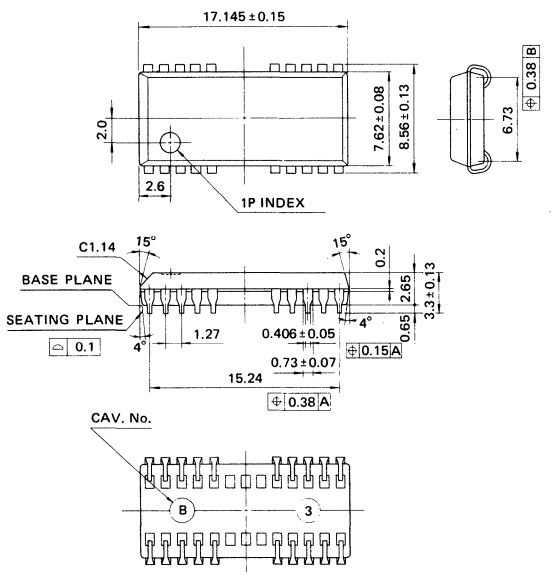
• 24 PIN PLASTIC FLAT



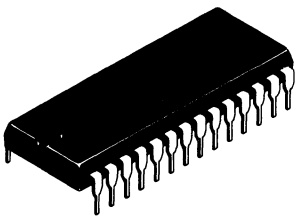


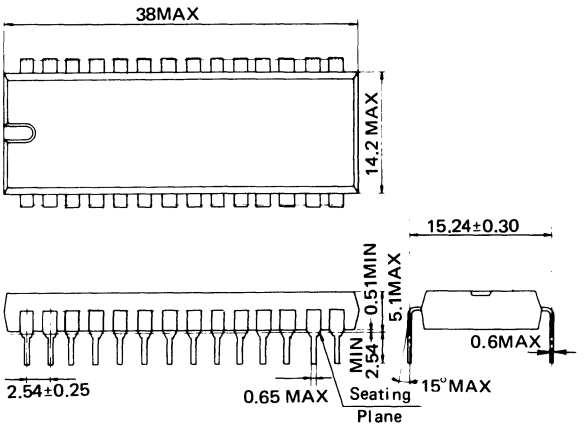
• 26 PIN SOJ





• 28 PIN PLASTIC





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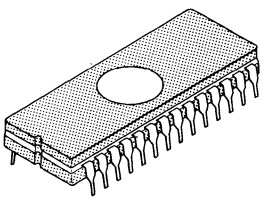

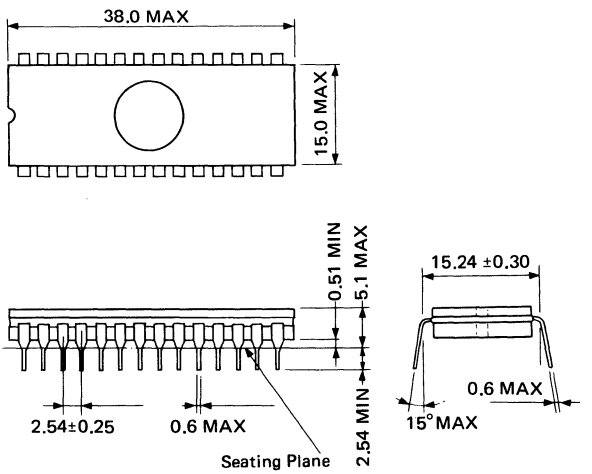

Note: All dimensions in millimeters.

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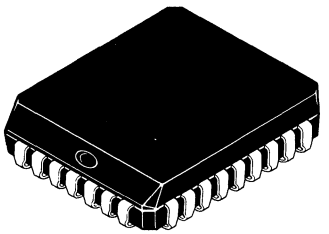
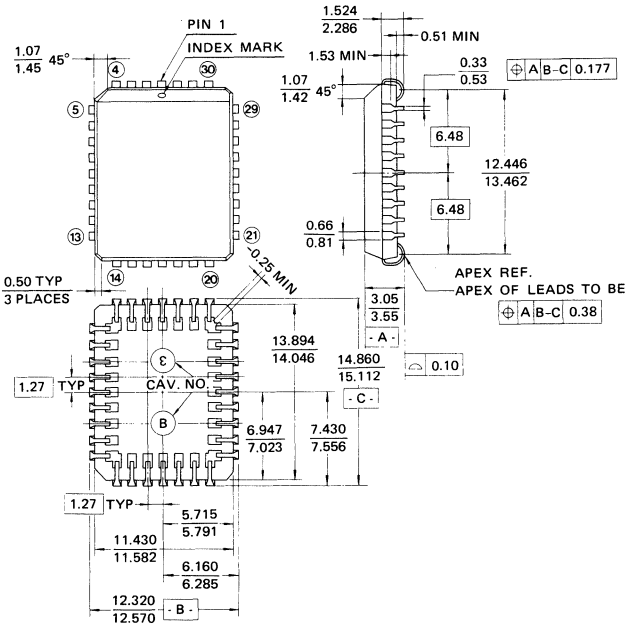
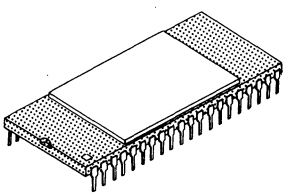
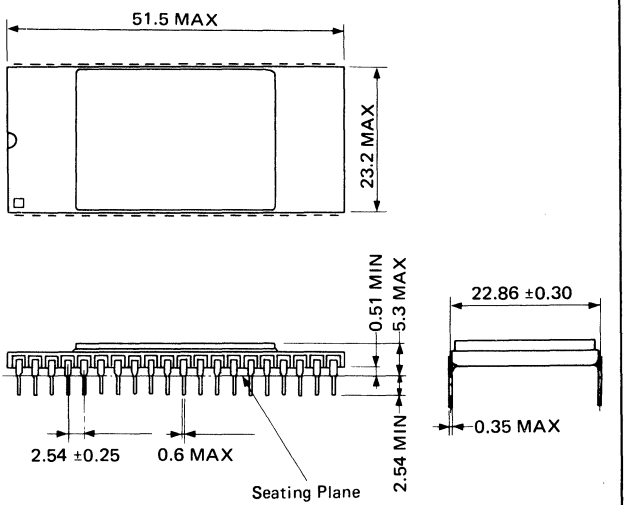
• 32 PIN PLCC





• 40 PIN SIDE-BRAZED





RELIABILITY INFORMATION

3

3

RELIABILITY INFORMATION

1. INTRODUCTION

Semiconductor memories play a leading role in the explosive progress of semiconductor technology. They use some of the most advanced design and manufacturing technology developed to date. With greater integration, diversity and reliability, their applications have expanded enormously. Their use in large scale computers, control equipment, calculators, electronic games and in many other fields has increased at a fast rate.

A failure in electronic banking or telephone switching equipment, for example, could have far reaching effects and can cause incalculable losses. So, the demand, for stable high quality memory devices is strong.

We, at Oki Electric is fully aware of this demand. So we have adopted a comprehensive quality assurance system based on the concept of consistency in development, manufacturing and sales.

With the increasing demand for improvement in function, capability and reliability, we will expand our efforts in the future. Our quality assurance system and the underlying concepts are outlined briefy below.

2. QUALITY ASSURANCE SYSTEM AND UNDERLYING CONCEPTS

The quality assurance system employed by Oki Electric can be divided into 4 major stages: device planning, developmental prototype, production prototype, and mass production. This system is outlined in the following block diagram (Fig. 1-1).

1) Device planning stage

To manufacture devices that meet the market demands and satisfy customer needs, we carefully consider functional and failure rate requirements, utilization form, environment and other conditions. Once we determine the proper type, material and structure, we check the design and manufacturing techniques and the line processing capacity. Then we prepare the development planning and time schedule.

2) Developmental prototype stage

We determine circuits, pattern design, process settings, assembly techniques and structural requirements during this stage. At the same time, we carry out actual prototype reliability testing.

Since device quality is largely determined during the designing stage, Oki Electric pays careful attention to quality confirmation during this stage.

This is how we do it:

(1) After completion of circuit design (or pattern design), personnel from the design, process technology, production technology, installation technology and reliability departments get together for a thorough review to ensure design quality and to anticipate problems that may occur during mass production. Past experience and know-how guide these discussions.

(2) Since many semiconductor memories involve new concepts and employ high level manufacturing technology, the TEG evaluation test is often used during this stage.

Note: TEG (Test Element Group) refers to the device group designed for stability evaluation of MOS transistors, diodes, resistors, capacitors and other circuit component element used in LSI memories.

(3) Prototypes are subjected to repeated reliability and other special evaluation tests. In addition, the stability and capacity of the manufacturing process are checked.

3) Production prototype stage

During this stage, various tests check the reliability and other special features of the production prototype at the mass production factory level. After confirming the quality of device, we prepare the various standards required for mass production, and then start production. Although reliability and other special tests performed on the production prototype are much the same as those performed on the developmental prototype, the personnel, facilities and production site differ for the two prototypes, necessitating repeated confirmation tests.

4) Mass production

During the mass production stage, careful management of purchased materials, parts and facilities used during the manufacturing process, measuring equipment, manufacturing conditions and environment is necessary to ensure device quality first stipulated during the designing stages. The manufacturing process (including inspection of the completed device) is followed by a lot guarantee inspection to check that the specified quality is maintained under conditions identical to those under which a customer would actually use the device. This lot guarantee inspection is performed in 3 different forms as shown below.

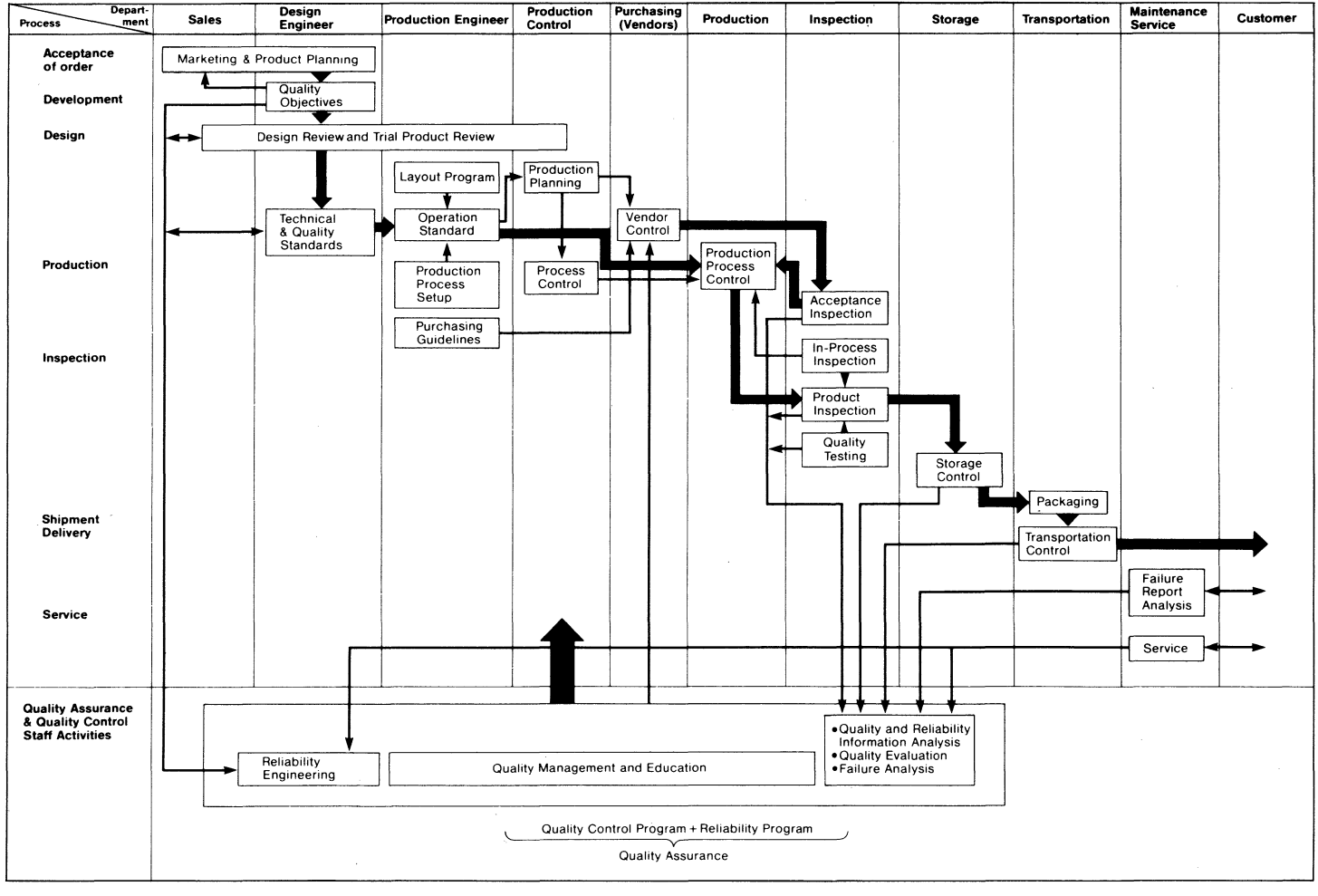
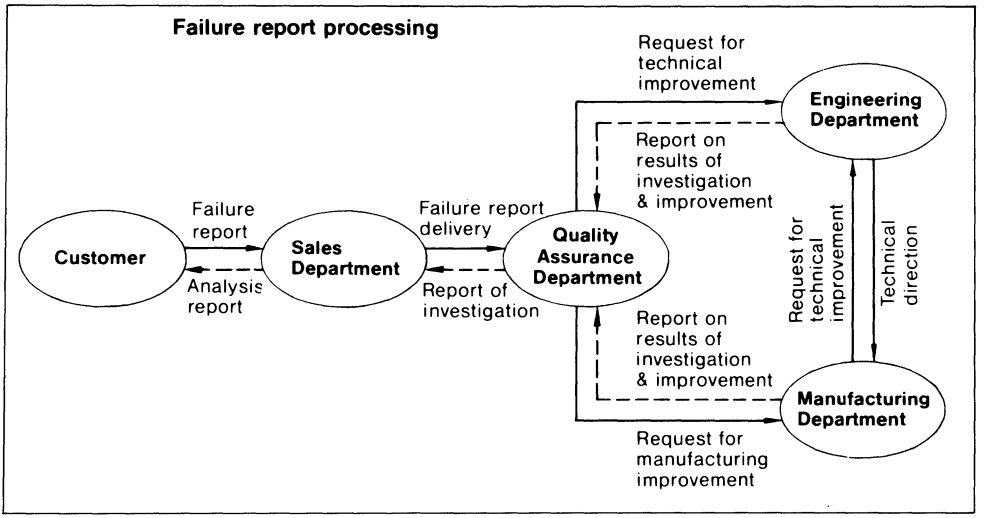


Fig. 1 Quality Assurance System

Fig. 2 Defect Processing Flowchart



(1) Group A tests: appearance, labels, dimensions and electrical characteristics inspection

(2) Group B tests: check of durability under thermal and mechanical environmental stresses, and operating life characteristics

(3) Group C tests: performed periodically to check operational life etc on long term basis.

Note: Like the reliability tests, the group B tests conform to the following standards.
MIL-STD-883B, JIS C 7022, EIAJ-IC-121

Devices which pass these lot guarantee inspections are stored in a warehouse awaiting shipment to customers. Standards are also set up for handling, storage and transportation during this period, thereby ensuring quality prior to delivery.

5) At Oki Electric, all devices are subjected to thorough quality checks. If, by chance, a failure does occur after delivery to the customer, defective devices are processed and the problem rectified immediately to minimize the inconvenience to the customer in accordance with the following flowchart.

3. EXAMPLE OF RELIABILITY TEST RESULTS

We have outlined the quality assurance system and the underlying concepts employed by Oki Electric. Now, we will give a few examples of the reliability tests performed during the developmental and production prototype stages. All reliability tests performed by Oki Electric conform with the following standards.

MIL-STD-883B, JIS C 7022, EIAJ-IC-121

Since these reliability tests must determine performance under actual working conditions in a short period of time, they are performed under severe test conditions. For example, the 125°C high temperature continuous operation test performed for 1000 hours is equivalent to testing device life from 2 to 300 years of use at Ta = 40°C.

By repeating these accelerated reliability tests, device quality is checked and defects analyzed. The resulting information is extremely useful in improving the manufacturing processes. Some of the more common defects in memory LSI elements and their analysis are described below.

3

OKI MEMORY LSI LIFE TEST RESULTS

Test item	Test condition	Device name	MSM41256-XXRS			MSM3764A-XXRS			MSM5165-XXRS		
		Function	262144 x 1 bit DYNAMIC RAM			65536 x 1 bit DYNAMIC RAM			8192 x 8 bit STATIC RAM		
		Structure	Si gate N-MOS 16P plastic package			Si gate N-MOS 16P plastic package			Si gate C-MOS 28P plastic package		
			Sample size	Test hours	Failures	Sample Size	Test hours	Failures	Sample size	Test hours	Failures
Operating life test	Ta = 125°C Vcc = 5.5V		300	2000	0	300	2000	0	88	2000	0
	Ta = 150°V Vcc = 5.5V		40	6000	0	50	2000	0	50	2000	0
Temperature humidity test	140°C 85% Vcc = 5.5V		100	100	0	100	100	0	22	100	0
	85°C 85% Vcc = 5.5V		100	2000	0	150	2000	0	100	2000	0
Pressure cooker test	121°C 100% No bias		100	500	0	100	500	0	50	300	0
Low temperature life test	Ta = -10°C Vcc = 7.0V		22	2000	0	22	2000	0	22	2000	0
Temperature cycling test	-55°C ~ 150°C		100	500 cycles	0	100	500 cycles	0	100	500 cycles	0

Test item	Test condition	Device name	MSM27256-AS			MSM38256-XXRS			MSM531000-XXRS		
		Function	32768 x 8 bit UV erasable EP ROM			32768 x 8 bit Mask ROM			MSM531000-XXRS Mask ROM		
		Structure	Si gate N-MOS 28P cerdip			Si gate N-MOS 28P plastic package			Si gate C-MOS 28P plastic package		
			Sample size	Test hours	Failures	Sample Size	Test hours	Failures	Sample size	Test hours	Failures
Operating life test	Ta = 125°C Vcc = 5.5V		88	2000	0	55	2000	0	88	2000	0
	Ta = 150°C Vcc = 5.5V		40	2000	0						
Temperature humidity test	140°C 85% Vcc = 5.5V								22	100	0
	85°C 85% Vcc = 5.5V		50	1000	0	50	2000	0	25	2000	0
Pressure cooker test	121°C 100% No bias		22	48	0	22	500	0	50	200	0
Low temperature life test	Ta = -10°C Vcc = 7.0V		22	2000	0				22	2000	0
Temperature cycling test	-55°C ~ 150°C		100	500 cycles	0	50	300 cycles	0	50	300	0

OKI MEMORY LSI ENVIRONMENTAL TEST RESULTS

Test item		Test condition	MSM41256-XXRS Sample size	MSM41256-XXRS Failures	MSM3764A-XXRS Sample size	MSM3764A-XXRS Failures	MSM5165-XXRS Sample size	MSM5165-XXRS Failures
Thermal environmental test	Soldering heat	260°C 10 sec	22	0	22	0	22	0
	Thermal shock	0°C~100°C 5 min 5 min 10 cycles						
	Temperature cycling	−55°C~RT~150°C 30 min 30 min 20 cycles						
Mechanical environmental test	Variable frequency vibration	100Hz~2000Hz 4 min per cycle 4 times in X, Y, Z	22	0	22	0	22	0
	Shock	1500G, 0.5 ms, 5 times in each X, Y, Z						
	Constant acceleration	10000G or 20000G 1 min in each X, Y, Z						
Electrical Environmental test	ESD	200pF, 0Ω, 5 times ±200V	10	0	10	0	10	0

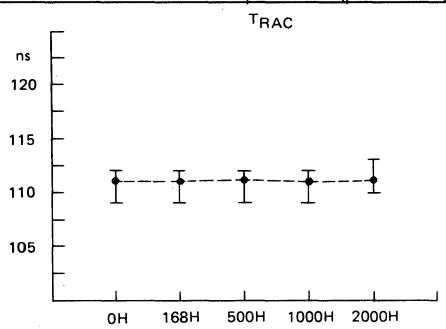
Test item		Test condition	MSM2725-AS Sample size	MSM2725-AS Failures	MSM38256-XXRS Sample size	MSM38256-XXRS Failures	MSM531000-XXRS Sample size	MSM531000-XXRS Failures
Thermal environmental test	Soldering heat	260°C 10 sec	22	0	22	0	22	0
	Thermal shock	0°C~100°C 5 min 5 min 10 cycles						
	Temperature cycling	−55°C~RT~150°C 30 min 30 min 20 cycles						
Mechanical environmental test	Variable frequency vibration	100Hz~2000Hz 4 min per cycle 4 times in X, Y, Z	22	0	22	0	22	0
	Shock	1500G, 0.5 ms, 5 times in each X, Y, Z						
	Constant acceleration	10000G or 20000G 1 min in each X, Y, Z						
Electrical environmental test	ESD	200pF, 0Ω, 5 times ±200V	10	0	10	0	10	0

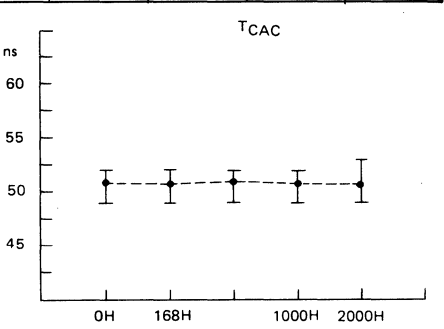
HIGH TEMPERATURE OPERATING LIFE TEST

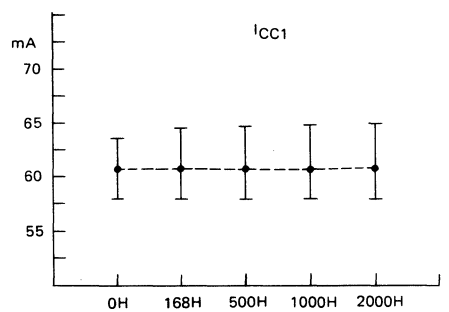
(Ta = 125°C, V_{CC} = 5.5V, t_{cycle} = 3 μs) SAMPLE SIZE = 300 pcs.

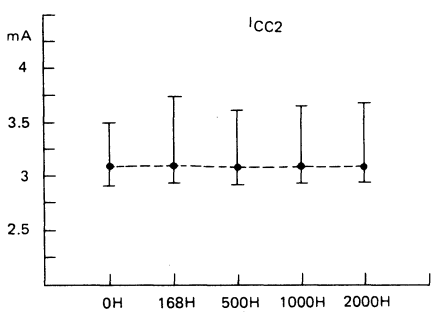
MSM41256-12RS

			0H	168H	500H	1000H	2000H	
I_{CC1}	mA	MAX.	63.54	64.58	64.70	64.86	64.98	
		MIN.	57.92	57.94	57.86	57.90	57.96	
		MEAN	60.700	60.710	60.620	60.700	60.740	
		S.D.	1.339	1.370	1.376	1.389	1.394	
		DEL.	0.00	1.04	1.16	1.32	1.44	
I_{CC2}	mA	MAX.	3.50	3.74	3.62	3.66	3.68	
		MIN.	2.92	2.94	2.92	2.94	2.94	
		MEAN	3.083	3.097	3.068	3.084	3.084	
		S.D.	.113	.144	.119	.119	.120	
		DEL.	0.00	0.68	0.20	0.24	0.26	
T_{RAC}	ns	MAX.	112	112	112	112	113	
		MIN.	109	109	109	109	110	
		MEAN	110.9	110.9	111.1	110.9	111.0	
		S.D.	.7	.7	.8	.7	.8	
		DEL.	0	−1	1	−1	−1	
T_{CAC}	ns	MAX.	52	52	52	52	53	
		MIN.	49	49	49	49	49	
		MEAN	50.8	50.6	51.0	50.6	50.6	
		S.D.	.7	.6	.7	.6	.7	
		DEL.	0	−1	1	−1	−1	





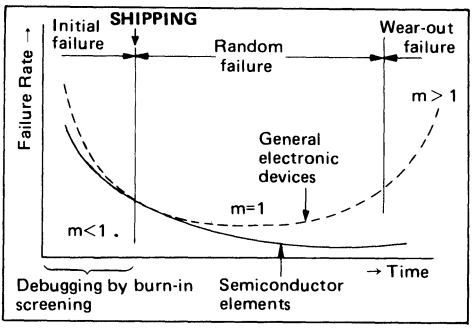




4. SEMICONDUCTOR MEMORY FAILURES

The life-span characteristics of semiconductor elements in general (not only semiconductor IC devices) is described by the curve shown in the diagram below. Although semiconductor memory failures are similar to those of ordinary integrated circuits, the degree of integration (miniaturization), manufacturing complexity and other circuit element factors influence their incidence.

< Semiconductor Element Failure Rate Curve >

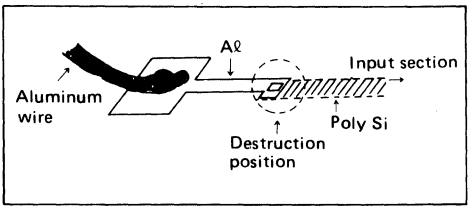


1) Surge Destruction

This is destruction of the input/output stage circuits by external surge currents or static electricity. The accompanying photograph shows a point of contact between aluminum and poly-silicon that has been dissolved by a surge current. A hole has formed in the substrate silicon, leading to a short circuit. This kind of failure is traceable in about 30% of defective devices returned to the manufacturer. Despite miniaturization of semiconductor memory component elements (which means the elements themselves are less resistant), these failures usually occur during assembly and other handling operations.

At Oki Electric, all devices are subjected to static electricity intensity tests (under simulated operational conditions) in the development stage to reduce this type of failure. In addition to checking endurance against surge currents, special protective circuits are incorporated in the input and output sections.

Example of surge destruction



2) Oxide Film Insulation Destruction (Pin Holes)

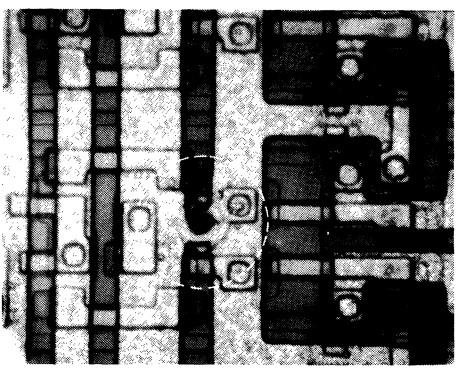
Unlike surge destruction, this kind of failure is caused by manufacturing defects. Local weakened sections are ruptured when subjected to external electrical stress. Although this problem is accentuated by the miniaturization of circuit elements, it can be resolved by maintaining an ultra-clean manufacturing environment and through 100% burn-in screening.

3) Surface Deterioration due to Ionic Impurities

Under some temperature and electric field conditions, charged ionic impurities moving within the oxide film previously resulted in occasional deterioration of silicon surfaces. This problem has been eliminated by new surface stabilization techniques.

4) Photolithographic Defects

Integrated circuits are formed by repeated photographic etching processes. Dust and scratches on the mask (which corresponds to a photographic negative) can cause catastrophic defects. At present, component elements have been reduced in size to the order of 10^{-4} cm through miniaturization. However, the size of dust and scratches stays the same. At Oki Electric, a high degree of automation, minimizing human intervention in the process, and unparalleled cleanliness solves this problem.



Photolithographic Defect

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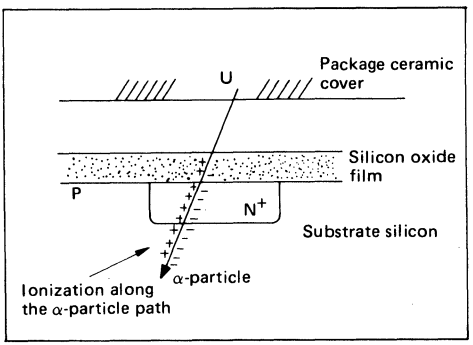
5) Aluminum Corrosion

Aluminum corrosion is due to electrolytic reactions caused by the presence of water and minute impurities. When aluminum dissolves, lines break. This problem is unique to the plastic capsules now used widely to reduce costs. Oki Electric has carefully studied the possible cause and effect relationship between structure and manufacturing conditions on the one hand, and the generation of aluminum corrosion on the other. Refinements incorporated in Oki LSIs permit superior endurance to even the most severe high humidity conditions.

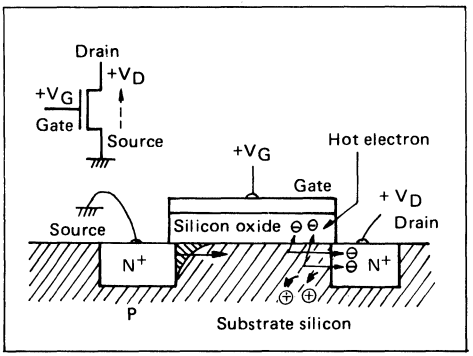
6) Alpha-Particle Soft Failure

This problem occurs when devices are highly miniaturized, such as in 64-kilobit RAMs. The inversion of memory cell data by alpha-particle generated by radioactive elements like uranium and thorium (present in minute quantities, measured in ppb) in the ceramic package material causes defects. Since failure is only temporary and normal operation restored quickly, this is referred to as a "soft" failure. At Oki Electric we have eliminated the problem by coating the chip surface of 64-kilobit RAMs with a resin which effectively screens out these alpha-particle.



7) Degradation in Performance Characteristics Due to Hot Electrons

With increased miniaturization of circuit elements, internal electric field strength in the channels increases since the applied voltage remains the same at 5 V. As a result, electrons flowing in the channels, as shown in the accompanying diagram, tend to enter into the oxide film near the drain, leading to degradation of performance. Although previous low-temperature operation tests have indicated an increase of this failure, we have confirmed by our low-temperature acceleration tests, including checks on test element groups, that no such problem exists in Oki LSIs.



Characteristic deterioration caused by hot electron

With further progress in the miniaturization of circuit components, failures related to pin hole oxide film destruction and photolithography have increased. To eliminate these defects during manufacturing, we at Oki Electric have been continually improving our production processes based on reliability tests and information gained from the field. And we subject all devices to high-temperature burn-in screening for 48 to 96 hours to ensure even greater reliability.

MOS MEMORY HANDLING PRECAUTIONS

MOS MEMORY HANDLING PRECAUTIONS

1. STATIC ELECTRICITY COUNTER-MEASURES

Since voltage is generally controlled by means of the transistor gate oxide film in MOS memories, the input impedance is high and the insulation tends to be destroyed more readily by static electricity.

Although Oki MOS memories incorporate built-in protector circuits to protect all input terminals from such destruction, it is not considered possible to give complete protection against heat destruction due to overcurrents and insulation film destruction due to irregular high voltages. It is, therefore, necessary to observe the following precautionary measures.

1) Under no circumstances must voltages or currents in excess of the specified ratings be applied to any input terminal.
2) Always use an electrically conductive mat or shipping tubes for storage and transporting purposes.
3) Avoid wearing apparel made of synthetic fiber during operations. The wearing of cottons which do not readily generate static electricity is desirable. Also avoid handling devices with bare hands. If handling with bare hands cannot be avoided, make sure that the body is grounded, and that a 1MΩ resistor is always connected between the body and ground in order to prevent the generation of static electricity.
4) Maintaining the relative humidity in the operation room at 50% helps to prevent static electricity. This should be remembered especially during dry seasons.
5) When using a soldering iron, the iron should be grounded from the tip. And as far as possible, use low power soldering irons (12 V or 24 V irons).

2. POWER SUPPLY AND INPUT SIGNAL NOISE

2.1 Power supply noise absorption

In dynamic memories, the flow of power supply current differs greatly between accessing and standby modes.

Although very little power is consumed by CMOS memories during standby mode, considerable current is drawn for charging and discharging (instantaneous current requirements) during access mode. In order to absorb the "spike noise" generated by these current requirements, the use of relatively large capacitance capacitors (about one 10μF capacitor for every 8 to 10 RAMs) is recommended along with good high frequency response capacitors of about 0.1μF for each memory element. Power line wiring with as little line impedance as possible is also desirable.

2.2 Input signal noise absorption

Overshooting and undershooting of the input signal should be kept to a bare minimum. Undershooting in particular can result in loss of cell data stability within the memory. For this reason,

(1) Avoid excessive undershooting when using an address common bus for memory board RAMs and ROMs.
(2) Since noise can be generated very easily when using direct drive for applying memory board RAM addresses from other driver boards, it is highly recommended that these addresses be first received by buffer.
(3) Methods available for eliminating undershooting generated in the address line include
   a) Clamping of the undershooting by including a diode.
   b) Connect 10~20Ω in series with driver outputs.
   c) Smooth the rising edge and falling edge waveforms.

3. CMOS MEMORY OPERATING PRECAUTIONS

3.1 Latch-Up

If the CMOS memory input signal level exceeds the Vcc power line voltage by +0.3 V, or drops below the ground potential by −0.3 V, the latch-up mechanism may be activated. And once this latch-up mode has been activated, the memory power has to be switched off before normal operating mode can be restored. Destruction of the memory element is also possible if the power is not switched off.

Although Oki CMOS memories have been designed to counter these tendencies, it is still recommended that input signal overshooting and undershooting by avoided.

3.2 Battery Back-Up

Take special note of the following 4 points when designing battery back-up systems.

(1) Do not permit the input signal H level to exceed Vcc +0.3 V when the memory Vcc power is dropped. To achieve this, it is recommended that a CMOS driver using a Vcc power common with the CMOS memory, or an open collector buffer or open drain buffer pulled-up by a Vcc power common with the CMOS memory be used for driving purposes.
(2) Set the chip select input signal CE to the same H level as the CMOS memory Vcc power line. And in order to minimize memory power consumption, set the write enable input $\overline{WE}$ level, the address input and the data input to either ground level or to the same H level as the CMOS memory Vcc power line.
(3) Make sure that the CMOS memory Vcc power line is increased without "ringing" or temporary breaks when restoring the battery back-up mode.
(4) When using synchronous type CMOS memories (MSM5115, MSM5104), make sure that accessing occurs after elapse of the chip enable off time (t_{CC}) prescribed in the catalog after the Vcc power line has reached the guaranteed operating voltage range.

For further details, refer to "CMOS Memory Battery Back-up" at the end of this manual.

EPROM WRITING AND ERASURE

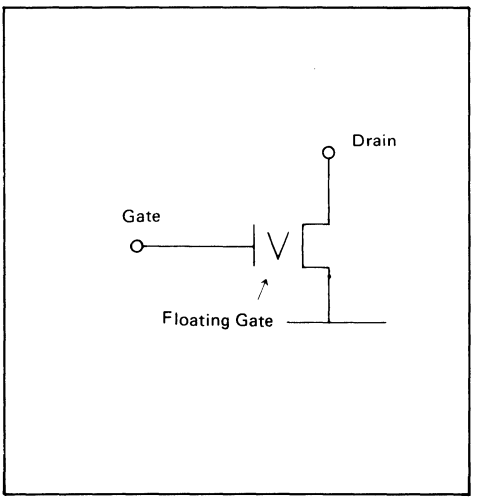
5

EPROM WRITING AND ERASURE

1. EPROM WRITING ERASURE

1.1 EPROM MSM2764 writing

Writing in the MSM2764RS involves setting the drain and gate voltages of the floating gate stage to a high voltage. When the drain voltage exceeds 15 V and the gate voltage 20 V, the channel charge (electrons) becomes highly energized and flow over the oxide film barrier into the floating gate. And since the high gate voltage is positive polarity, electrons will flow into the floating gate very easily. When electrons build up in the floating gate, the memory element "threshold voltage" is changed, and subsequently stored as memory data. Once the charge has been built up, the surrounding oxide film (high insulation) prevents escape of electrons. The data is thus stored as "non-volatile" data.



When the MSM2764RS is shipped from the factory, the floating gate is left in discharged status (all bits "1"), i.e. "blank" status. During writing processes, +25 V is applied to the Vpp terminal and V_{IH} to the $\overline{OE}$ input. The data to be programmed is applied in parallel to the outputs ($O_0 - 7$). After the address and data have been set up, application of V_{IH} level for 50 ms to the $\overline{CE}$ input will enable writing of data. Since the +25 V applied to Vpp is fairly close to the element's withstanding voltage, make sure that the voltage setting is maintained strictly within the 25 V ±1 V range. Application of voltages in excess of the rated voltage, and overshooting, to the Vpp terminal can result in permanent damage to the element.

Although MSM2764RS rewriting should be checked about 100 times by sample testing, in actual practice 5 to 10 times is usually the limit. This will not likely result in any problem.

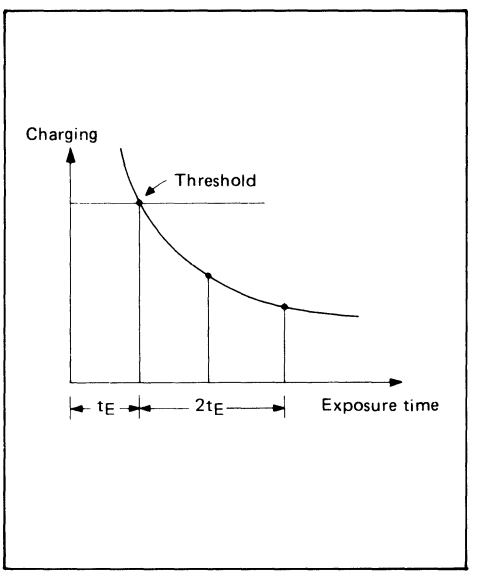
1.2 PROM programmer

Oki Electric employs a system whereby the various programmer available on the market are examined, and agreements reached with different programmer manufacturers. The purpose of this system is to check compatibility between programmer manufacturers and Oki Electric devices, and making modifications whenever required. Users are thus ensured trouble-free use.

In the event of EPROM trouble with Oki devices and approved programmer, problems will be handled by both Oki and driver manufacturer except where such problems have been caused purposely.

1.3 Erasure

Erasure of data written in the MSM2764RS can be effected by ultra-violet radiation of the memory element. In this case, the charge is discharged into the substrate or electrode by the ultra-violet energy, but note that the following erasure conditions must be met. If a memory which has not been properly erased is used, writing problems and operating failures are likely to arise. Also note that excessively long erasure times (of several hours duration) can also result in failure.



Lengthy exposure to direct sunlight can also result in loss of bits. Direct exposure of MSM2764 to the strong summer sun for a single day can result in bit changes. Although normal fluorescent lights have practically no effect, light rays beamed onto elements can cause special changes. It is therefore recommended that the glass face be covered with a screening label.

2. EPROM HANDLING

2.1 Defects caused by static electricity

The generation of static electricity on the EPROM glass face can result in changes in the memory contents. This, however, can be restored by brief exposure (several seconds) to ultra-violet radiation. But this exposure must be kept short. Exposure for 30 seconds or more can cause changes in the normal bits.

2.2 Handling precautions

(1) Avoid carpets and clothes etc where static electricity is generated.
(2) Make sure the programmer and mounting system are securely grounded.
(3) Also make sure that any soldering iron employed is properly grounded.
(4) Always carry in an electrically conductive plastic mat.
(5) Written ROMs are also to be kept in an electrically conductive plastic mat.
(6) Do not touch the glass seal by hand since this can result in deterioration of the ultra-violet permeability required for erasure, and subsequently lead to poor erasure.

2.3 System debugging precautions

During system debugging, check operations with a voltage of ±5% (oscillating).

MASK ROM CUSTOMER PROGRAM SPECIFICATIONS

MASK ROM CUSTOMER PROGRAM SPECIFICATIONS

The mask ROM custom program code programming method is outlined below.

1. USABLE MEDIA

(1) Magnetic tape
(2) EPROM

Magnetic tape and EPROM are used as standard.

2. MAGNETIC TAPE SPECIFICATIONS

2.1 Use the following types of magnetic tape in magnetic tape units compatible with IBM magnetic tape units.

(1) Length: 2400 feet, 1200 feet or 600 feet
(2) No label
(3) Width: 1/2 feet
(4) Channels: 9 channels
(5) Bit density: 800BPI standard, although 1600BPI can also be employed.
(6) Block size: Integer multiples of 256 bytes possible with 256 bytes as standard. 1 block, 1 record is standard.

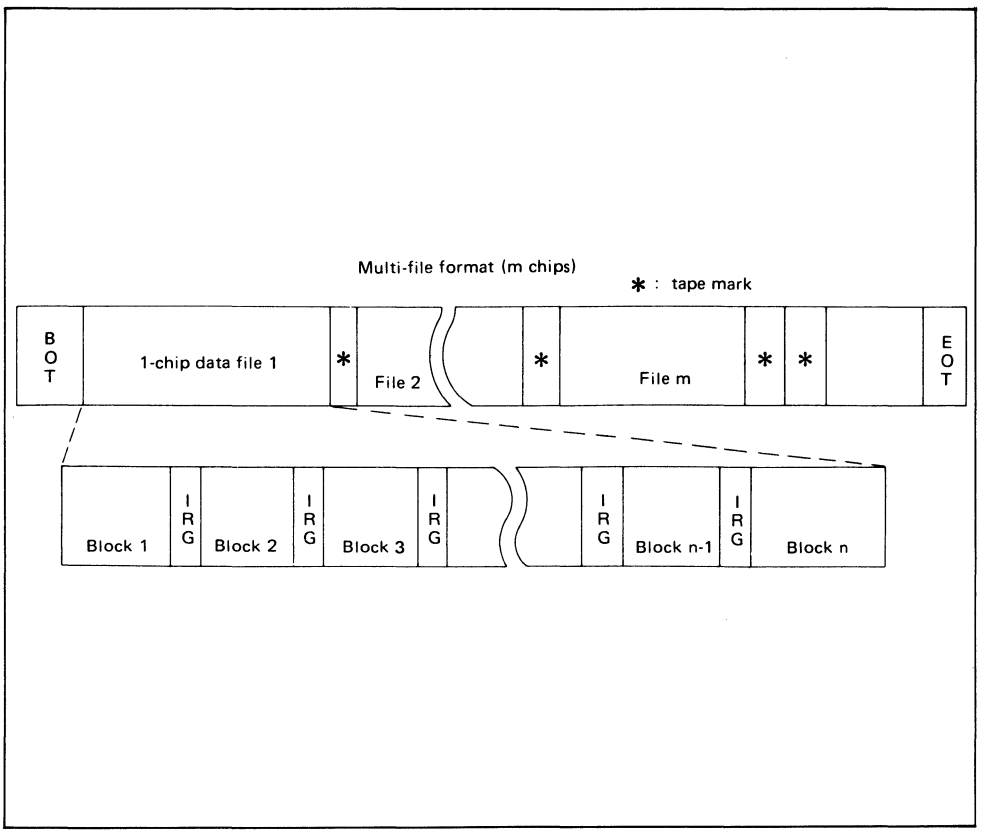
2.2 Magnetic tape format

(1) The data for a single chip should not extend into several tapes. Data for several chips are allowed to be included in a single magnetic tape, multiple file format being permitted. In this case, include the data of a single chip in one file.
(2) Use tape marks for file partitions when employing multiple file formats.
(3) Denote the completion of a magnetic tape file by two successive tape marks.

2.3 Magnetic tape data format

(1) The data contained in a single file on magnetic tape must be inserted from the head address $(0000)_{hex}$ of the device up to the final address in succession for a single chip.
(2) In this case, the LSB of the data should correspond to D_0, and the MSB to D_7.
(3) "1" bits in the data denote high device output, while "0" denotes low output.

2.4 Magnetic tape examples



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3. EPROM SPECIFICATIONS

(1) MSM2764, Intel 2764 or 27128 equivalent device may be used.

(2) Prepare 2 EPROMs containing identical data.

MASK ROM DEVELOPMENT FLOWCHART

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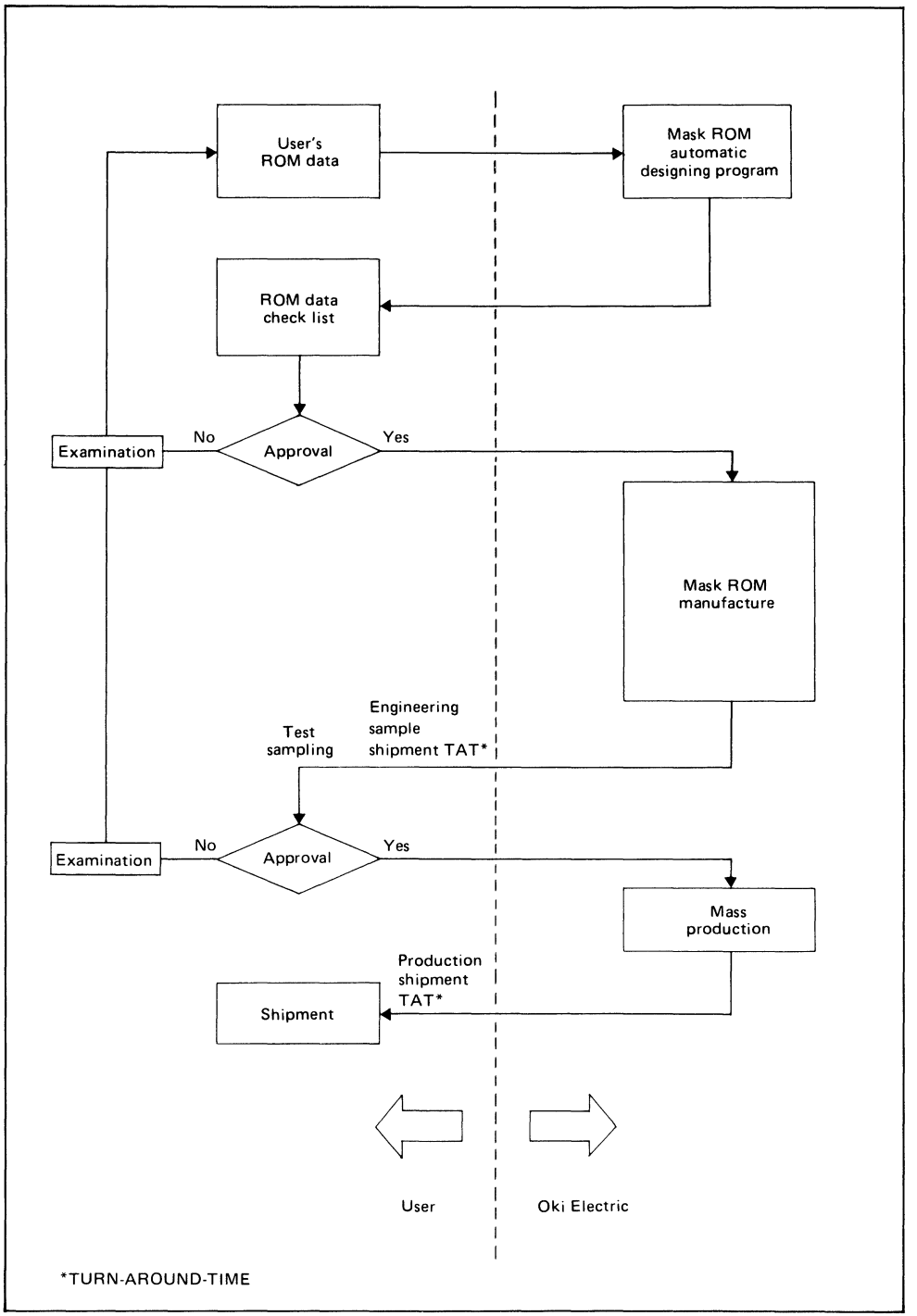
MASK ROM DEVELOPMENT FLOWCHART



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TERMINOLOGY AND SYMBOLS

TERMINOLOGY AND SYMBOLS

1. PIN TERMINOLOGY

Term	EPROM	ROM	Static RAM	Dynamic RAM
Power Supply Voltage Pin	V_{DD}, V_{CC} V_{GG}, V_{BB}	V_{CC}	V_{CC}	V_{DD}, V_{CC}
Address Input Pin	$A_0 \sim A_{12}$	$A_0 \sim A_{13}$	$A_0 \sim A_{11}$	$A_0 \sim A_7$
Data Input Pin			DI	D IN
Data Output Pin	$O_0 \sim O_7$	$D_0 \sim D_{15}$	DO	D OUT
Data Input/Output Pin			$I/O_1 \sim I/O_8$	
Chip Enable Pin	CE	CE	CE	
Output Enable Pin	OE	OE	OE	
Address Enable Pin		AE		
Chip Select Pin	CS		CS	
Write Enable Pin	WE		WE	$\overline{WE}$
Row Address Strobe Pin				$\overline{RAS}$
Column Address Strobe Pin				$\overline{CAS}$
Program Input Pin	Program, V_{PP}			
Data Valid Pin		DV		
Clock Input Pin		ϕT		
Ground Pin	V_{SS}	V_{SS}	V_{SS}	V_{SS}
Vacant Terminal	NC	NC		

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2. ABSOLUTE MAXIMUM RATINGS

Term	EPROM	ROM	Static RAM	Dynamic RAM
Power supply voltage	V_{DD}, V_{CC} V_{GG}, V_{BB} V_{SS}	V_{CC} V_{SS}	V_{CC} V_{SS}	V_{DD}, V_{CC} V_{SS}
Terminal voltage	V_T		V_T	V_T
Input voltage	V_I	V_I	V_I	V_I
Output voltage	V_O	V_O	V_O	V_O
Input current				
Output current			I_O	
Output short circuit current				I_{OS}
Load capacitance				
Power dissipation	P_D	P_D	P_D	P_D
Operating temperature	Topr	Topr	Topr	Topr
Storage temperature	Tstg	Tstg	Tstg	Tstg

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3. RECOMMENDED OPERATION CONDITIONS

Term	EPROM	ROM	Static RAM	Dynamic RAM
Power Supply Voltage	V_{DD}, V_{CC} V_{GG}, V_{BB} V_{SS}	V_{CC} V_{SS}	V_{CC} V_{SS}	V_{DD}, V_{CC} V_{BB} V_{SS}
"H" Clock Input Voltage				V_{IHC}
"H" Input Voltage	V_{IH}	V_{IH}	V_{IH}	V_{IH}
"L" Input Voltage	V_{IL}	V_{IL}	V_{IL}	V_{IL}
Data Pretention Voltage			V_{CCH}	
Load Capacitance		C_L	C_L	
Fan-out	N	N	N	
Operating Temperature	Topr	Topr	Topr	Topr

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4. DC CHARACTERISTICS

Term	EPROM	ROM	Static RAM	Dynamic RAM
"H" output voltage	V_{OH}	V_{OH}	V_{OH}	V_{OH}
"L" output voltage	V_{OL}	V_{OL}	V_{OL}	V_{OL}
"H" output current			I_{OH}	
"L" output current				
Input leakage current	I_{LI}	I_{LI}	I_{LI}	I_{LI}
Output leakage current	I_{LO}	I_{LO}	I_{LO}	I_{LO}
I/O leak current			I_{LO}	
Program terminal current	I_{PP1}, I_{PP2}			
Peak power on current		I_{PO}	I_{PO}, I_{SBP}	
Power supply current	I_{DD}, I_{CC} I_{BB}, I_{CC1} I_{CC2}	I_{CC}, I_{CCS} I_{CCA}	I_{CC}, I_{CCA} I_{CC1}, I_{CC2} I_{CCS}, I_{CCS1} I_{SB}	I_{DD1}, I_{CC1}, I_{BB1} I_{DD2}, I_{CC2}, I_{BB2} I_{DD3}, I_{CC3}, I_{BB3} I_{DD4}, I_{CC4}, I_{BB4}

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5. AC CHARACTERISTICS

(1) Read cycle

Term	EPROM	ROM	Static RAM	Dynamic RAM
Read cycle time		t_C, t_{RC}, t_{CYC}	t_{RC}	t_{RC}
Address access time	t_{ACC}	t_{AA}, t_{ACC}	t_A, t_{AC}, t_{ACC}, t_{AA}	
Chip select access time	t_{CO}	t_{CS}	t_{CO}, t_{ACS1}, t_{ACS2}	
Chip enable access time	t_{CE}	t_{ACE}	t_{AC}	
Output enable access time	t_{OE}	t_{CO}	t_{OE}	
Output setting time		t_{LZ}	t_{CX}, t_{LZ}	
Output valid time	t_{OH}	t_{OH}	t_{OH}, t_{OHA}	
Output disable time	t_{DF}	t_{HZ}	t_{OTD}, t_{HZ}, t_{OFF}	t_{OFF}
Address set-up time		t_{AS}	t_{AS}	
Address hold time		t_{AH}	t_{AH}	
Chip enable off time			t_{CC}	
Chip enable pulse width			t_{CE}	
Power-up time		t_{PU}	t_{PU}	
Power-down time		t_{PD}	t_{PD}	
Address enable pulse width		t_{AE}		
Data valid access time		t_{VA}		
Data valid delay time		t_{VD}		
Clock delay time		t_{VH}		
Clock pule width		t_H		
Clock delay time		t_L		
Output delay time		t_{DD}		
Output access time		t_{DA}		
Output hold time		t_{DH}		
Address enable set-up time		t_{AES}		

(2) Write Cycle

Term	EPROM	ROM	Static RAM	Dynamic RAM
Write cycle time			t_{WC}	t_{RC}
Address set-up time	t_{AS}		t_{AS}, t_{AW}	
Write pulse width	t_{PW}		t_{W}, t_{WP}	t_{WP}
Write recovery time			t_{WR}	
Data set-up time	t_{DS}		t_{DS}, t_{DW}	t_{DS}
Data hold time	t_{DH}		t_{DH}	t_{DH}
Output off-time	t_{DF}		t_{OTW}, t_{WZ}	t_{OFF}
Chip select set-up time	t_{CSS}		t_{CW}	
Address hold time	t_{AH}		t_{AH}, t_{WR}	
Chip enable off time			t_{CC}	
Chip enable pulse width			t_{CW}, t_{CE}	
Write enable set-up time			t_{WS}	
Write enable read time			t_{WCL}	
Write enable hold time			t_{WH}	
Address/write enable setting time			t_{AW}	
Write enable output activation			t_{OW}	
Output enable set-up time	t_{OES}			
Output enable hold time	t_{OEH}			
Program read delay time	t_{DPR}			
Output enable delay time	t_{OE}			
Chip enable data valid time	t_{DV}			
Program pulse rising edge time	t_{PRT}			
Program pulse falling edge time	t_{PFT}			
V_{PP} restoration time	t_{VR}			
Chip enable hold time	t_{CH}			

DATA SHEETS

9 DATA SHEET

MOS DYNAMIC RAMS

9

OKI semiconductor

MSM3732 AS/RS

32,768-BIT DYNAMIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION

The Oki MSM3732H/L is a fully decoded, dynamic NMOS random access memory organized as 32,768 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

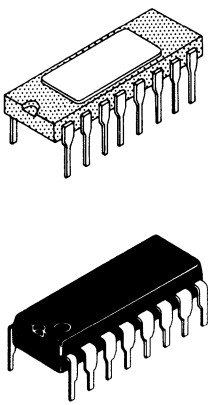
Multiplexed row and column address inputs permit the MSM3732 to be housed in a standard 16 pin DIP.

The MSM3732 is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

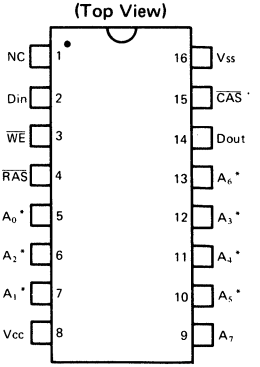
FEATURES

- 32,768 x 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  150 ns max (MSM3732H/L-15)
  200 ns max (MSM3732H/L-20)
- Cycle time,
  270 ns min (MSM3732H/L-15)
  330 ns min (MSM3732H/L-20)
- Low power: 248 mW active,
  28 mW max standby
- **Single +5V Supply, ±10% tolerance**
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 128 refresh cycles/2 ms
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance



PIN CONFIGURATION

(Top View)



Pin Names	Function
$A_0 \sim A_7$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
Din	Data Input
Dout	Data Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

* Refresh Address

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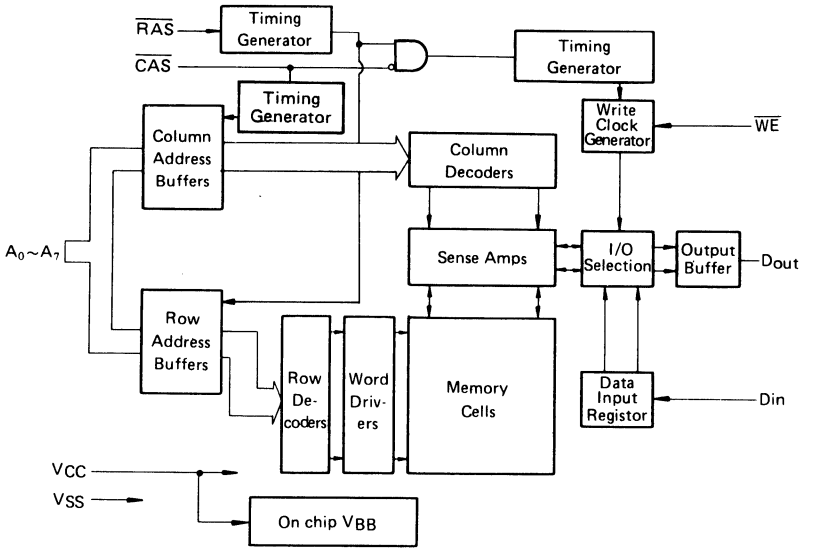
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		45	mA	
Standby Current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		5.0	mA	
Refresh Current* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}		35	mA	
Page Mode Current* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}		42	mA	
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−10	10	μA	
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	μA	
Output Levels Output high voltage (I_{OH} = −5 mA) Output low voltage (I_{OL} = 4.2 mA)	V_{OH} V_{OL}	2.4	 0.4	V V	

Note*: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A_0 ~ A_7, D_{IN})	C_{IN1}	4.5	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	7	10	pF
Output Capacitance (D_{OUT})	C_{OUT}	5	7	pF

Capacitance measured with Boonton Meter.

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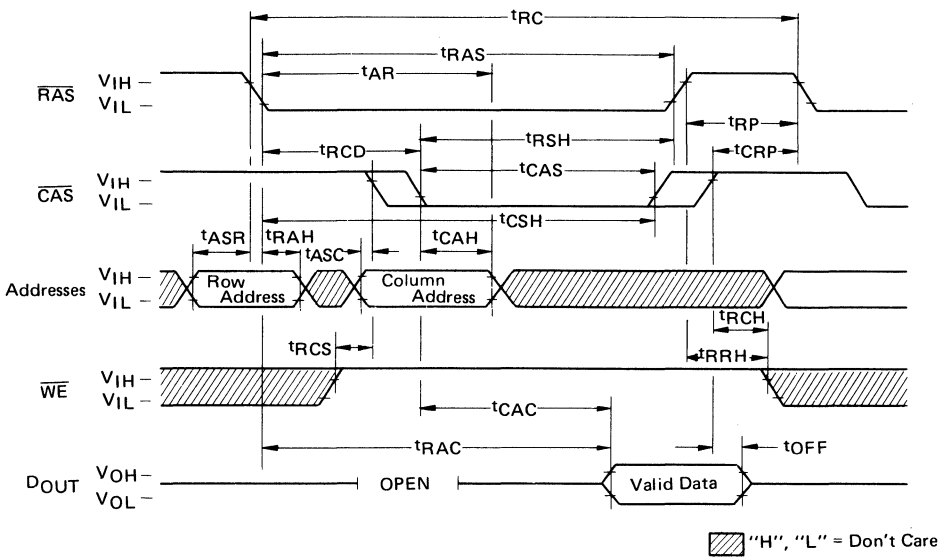
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1,2,3

Parameter	Symbol	Units	MSM3732-15		MSM3732-20		Note
			Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		2		2	
Random read or write cycle time	t_{RC}	ns	270		330		
Read-write cycle time	t_{RWC}	ns	270		330		
Page mode cycle time	t_{PC}	ns	170		225		
Access time from $\overline{RAS}$	t_{RAC}	ns		150		200	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		100		135	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	40	0	50	
Transition time	t_T	ns	3	35	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	100		120		
$\overline{RAS}$ pulse width	t_{RAS}	ns	150	10,000	200	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	100		135		
$\overline{CAS}$ precharge time	t_{CP}	ns	60		80		
$\overline{CAS}$ pulse width	t_{CAS}	ns	100	10,000	135	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	150		200		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	50	30	65	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		
Row Address set-up time	t_{ASR}	ns	0		0		
Row Address hold time	t_{RAH}	ns	15		20		
Column Address set-up time	t_{ASC}	ns	0		0		
Column Address hold time	t_{CAH}	ns	45		55		
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	ns	95		120		
Read command set-up time	t_{RCS}	ns	0		0		
Read command hold time	t_{RCH}	ns	0		0		
Write command set-up time	t_{WCS}	ns	−10		−10		8
Write command hold time	t_{WCH}	ns	45		55		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	95		120		
Write command pulse width	t_{WP}	ns	45		55		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	45		55		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	45		55		
Data-in set-up time	t_{DS}	ns	0		0		
Data-in hold time	t_{DH}	ns	45		55		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	95		120		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	60		80		8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	110		145		8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	20		25		

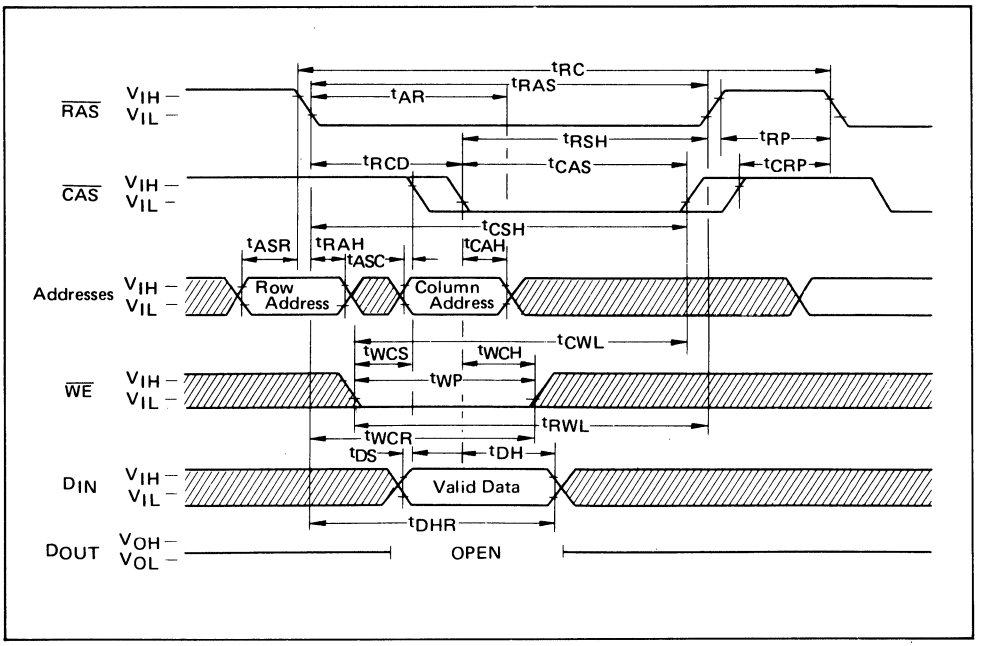
NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Examples; $\overline{RAS}$ only) before proper device operation is achieved.
2) AC measurements assume t_T = 5 ns.
3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4) Assumes that $t_{RCD} \leq t_{RCD}$ (max.).
If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5) Assumes that $t_{RCD} \leq t_{RCD}$ (max.)
6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} > t_{RWD}$ (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

READ CYCLE TIMING

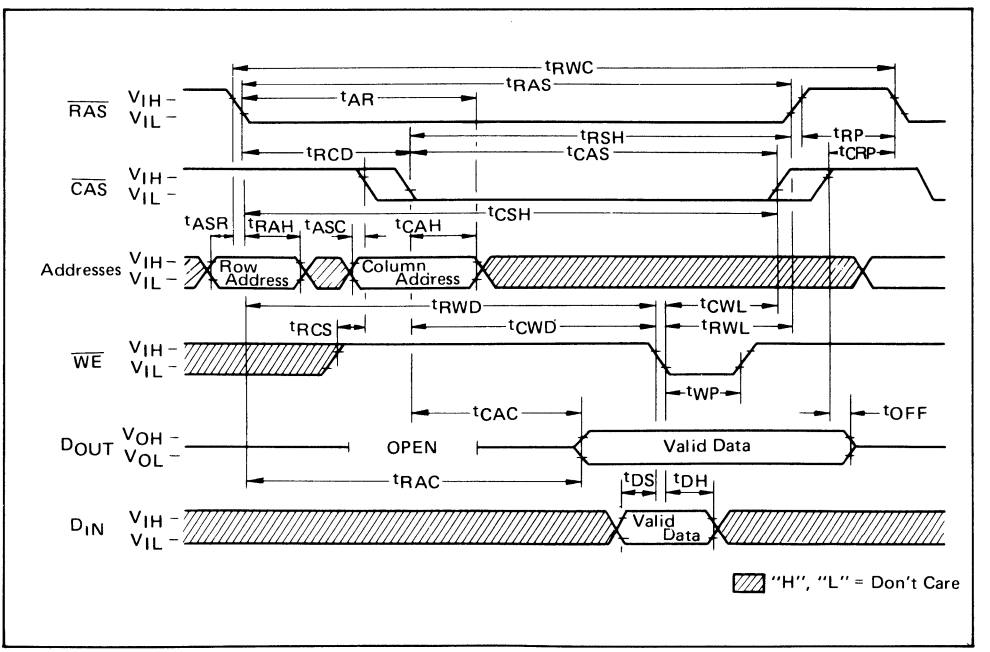


WRITE CYCLE TIMING

(EARLY WRITE)

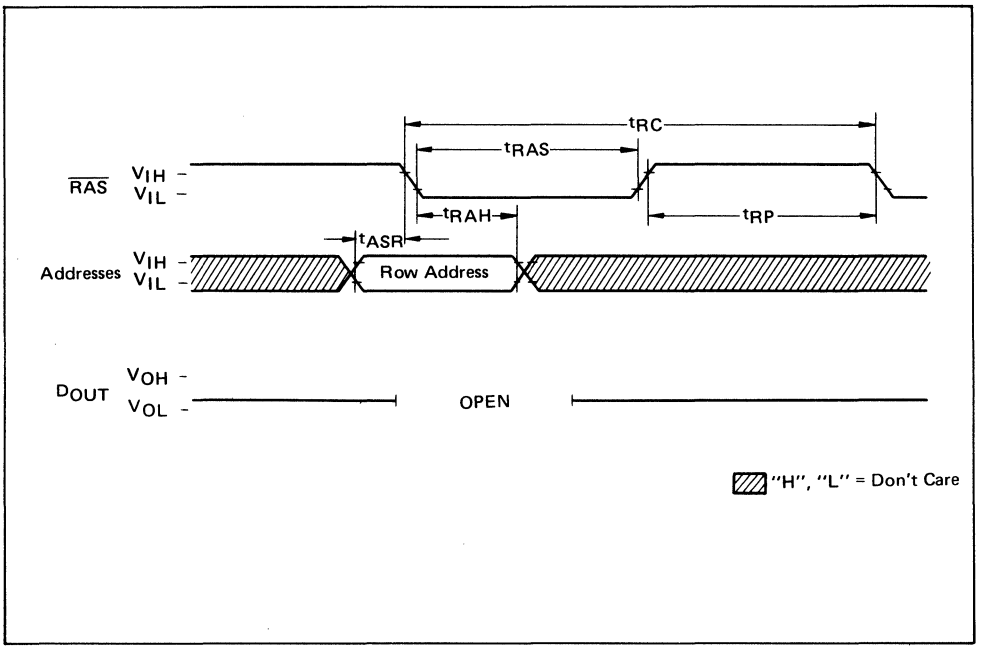


READ-WRITE/READ-MODIFY-WRITE CYCLE

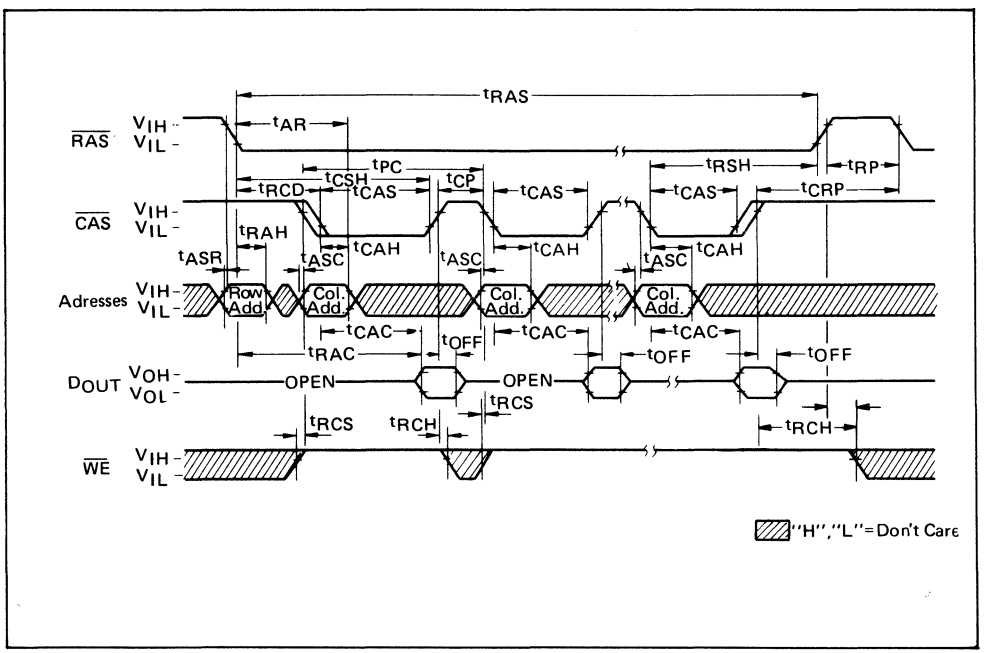


$\overline{RAS}$ ONLY REFRESH TIMING

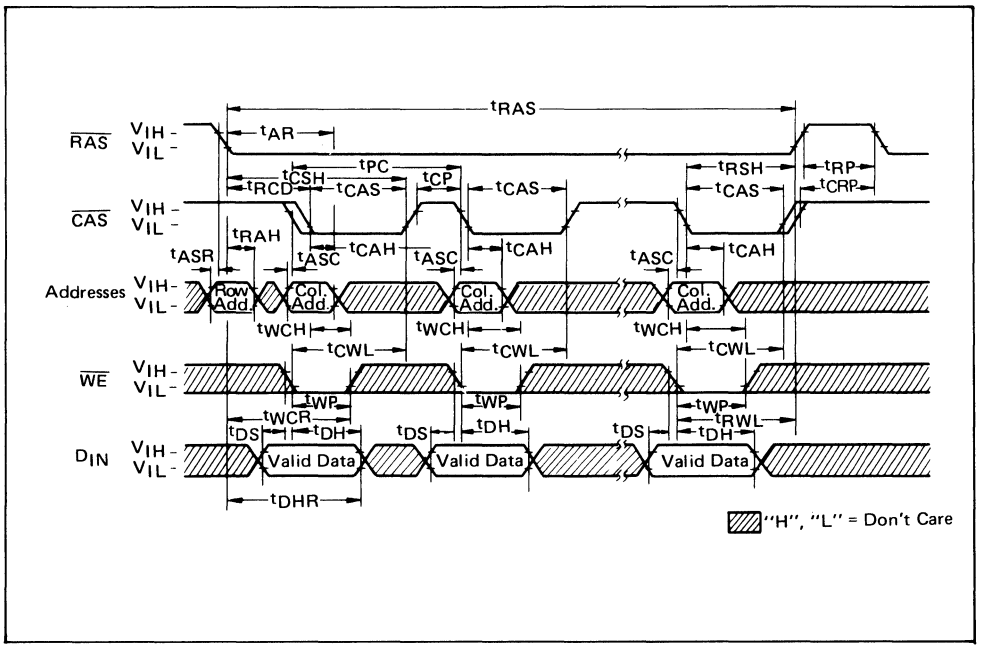
($\overline{CAS}$: V_{IH}, $\overline{WE}$ & D_{IN}: Don't care)



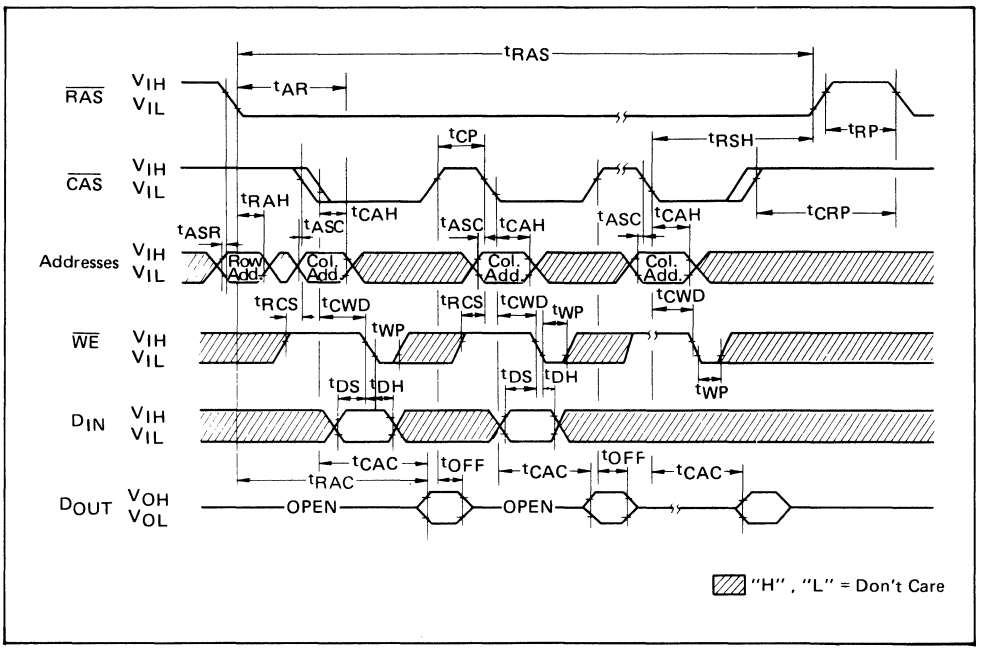
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE

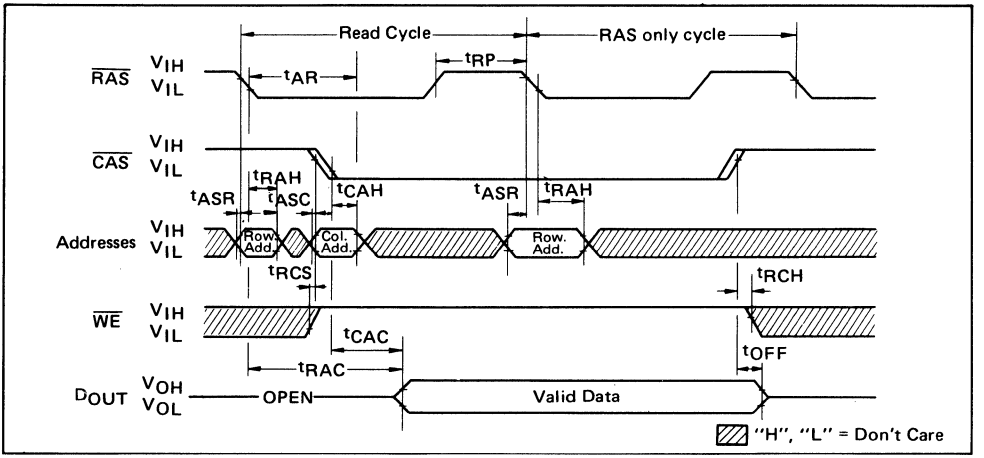


PAGE MODE, READ-MODIFY-WRITE CYCLE



9

HIDDEN REFRESH



DESCRIPTION

Address Inputs:

A total of fifteen binary input address bits are required to decode any 1 of 32,768 storage cell locations within the MSM3732. Eight row-address bits are established on the input pins (A_0~A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The seven column-address bits (A_0 through A_6) are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

One Column Address (A_7) has to be fixed at logic "0" (low level) for MSM3732L, and at logic "1" (high level) for MSM3732H.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM3732 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transistion. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSM3732 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses (A_0~A_6) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each rwo to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

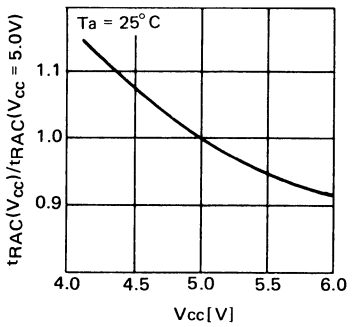
Hidden Refresh:

$\overline{RAS}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

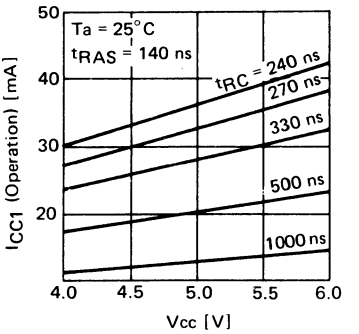
Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

TYPICAL CHARACTERISTICS

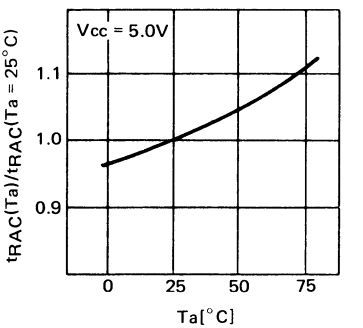
Access time from $\overline{RAS}$
(Relative value) v.s. Vcc



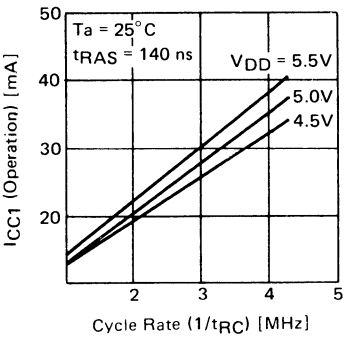
I_{CC1} (t_{RAS}: Constant)
v.s. Vcc



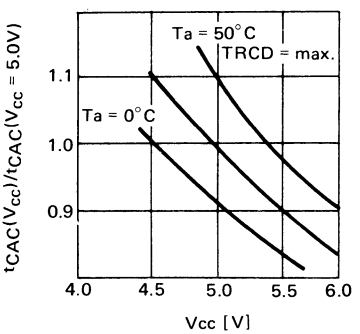
Access time from $\overline{RAS}$
(Relative value) v.s. Ta



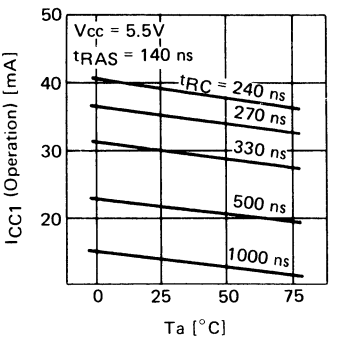
I_{CC1} (t_{RAS}: Constant)
v.s. Cycle rate



Access time from $\overline{CAS}$
(Relative value) v.s. Vcc

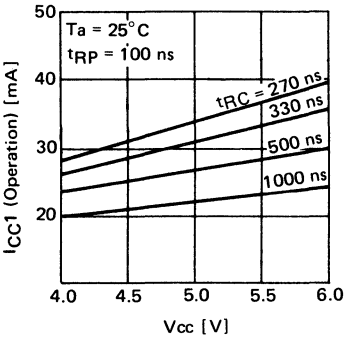


I_{CC1} (t_{RAS}: Constant)
v.s. Ta

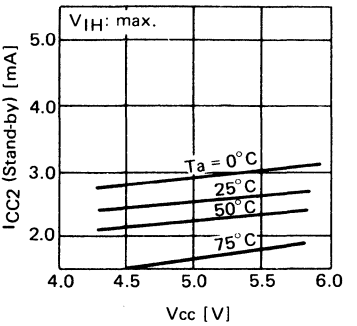


9

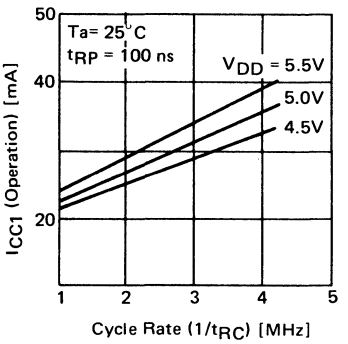
I_{CC1} (t_{RP}: Constant) v.s. Vcc



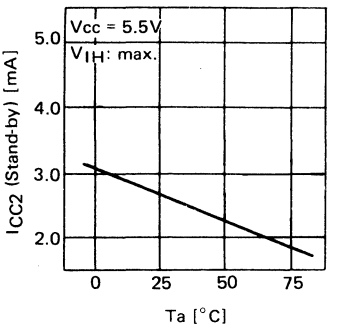
I_{CC2} v.s. Vcc



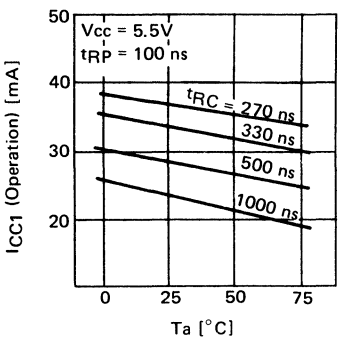
I_{CC1} (t_{RP}: Constant) v.s. Cycle rate



I_{CC2} v.s. Ta

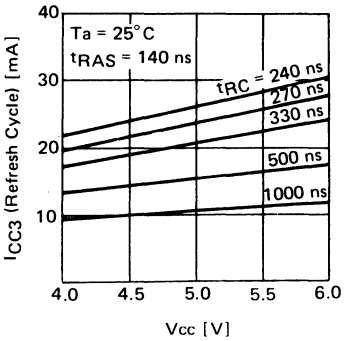


I_{CC1} (t_{RP}: Constant) v.s. Ta

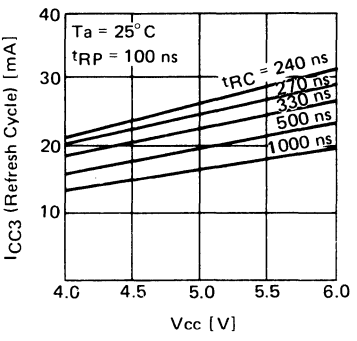


9

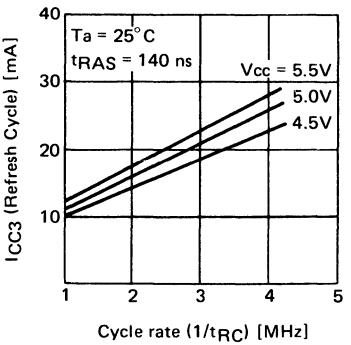
I_{CC3} (t_{RAS}: Constant)
v.s Vcc



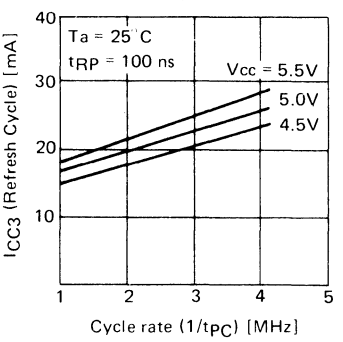
I_{CC3} (t_{RP}: Constant)
v.s. Vcc



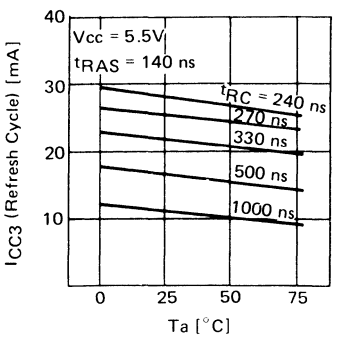
I_{CC3} (t_{RAS}: Constant)
v.s. Cycle rate



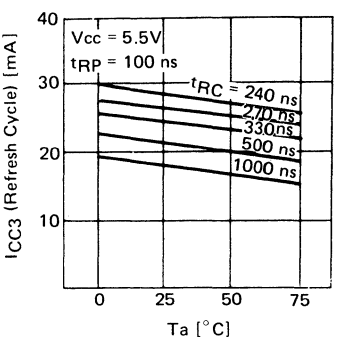
I_{CC3} (t_{RP}: Constant)
v.s. Cycle rate



I_{CC3} (t_{RAS}: Constant)
v.s. Ta

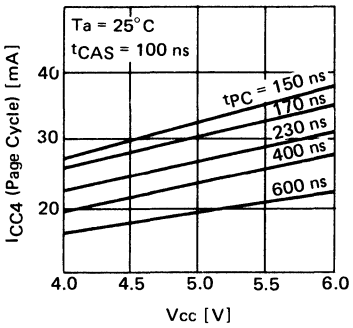


I_{CC3} (t_{RP}: Constant)
v.s. Ta

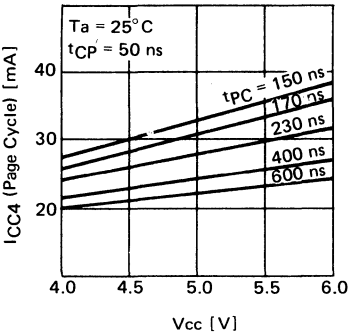


9

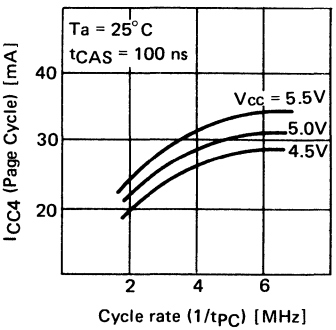
I_{CC4} (t_{CAS}: Constant)
v.s. Vcc



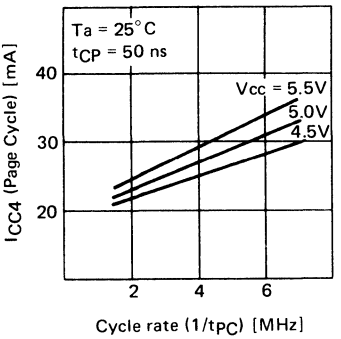
I_{CC4} (t_{CP}: Constant)
v.s. Vcc



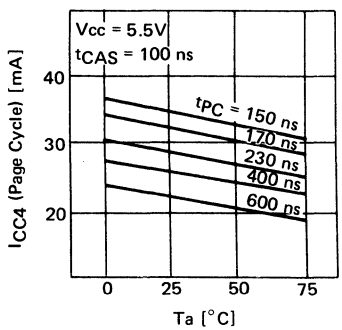
I_{CC4} (t_{CAS}: Constant)
v.s. Cycle rate



I_{CC4} (t_{CP}: Constant)
v.s. Cycle rate



I_{CC4} (t_{CAS}: Constant)
v.s. Ta



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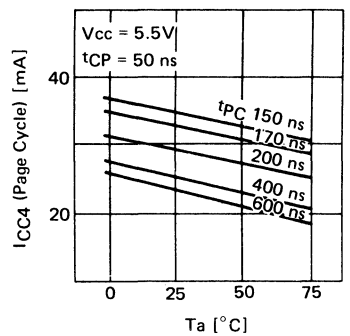
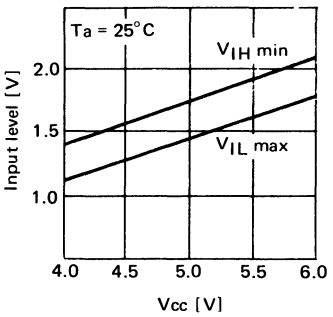
v.s. Ta

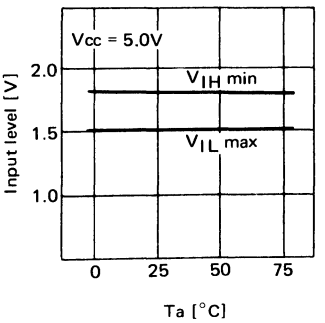


9

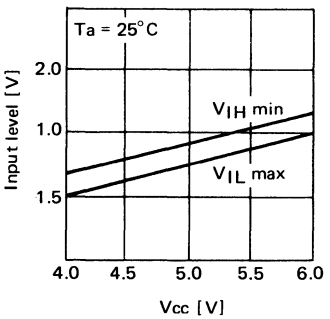
Address Input
v.s Vcc



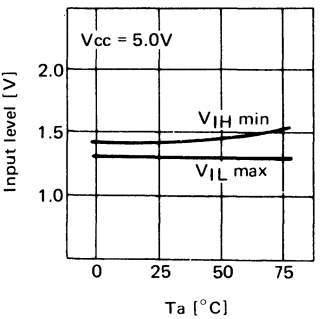
Address Input
v.s. Ta



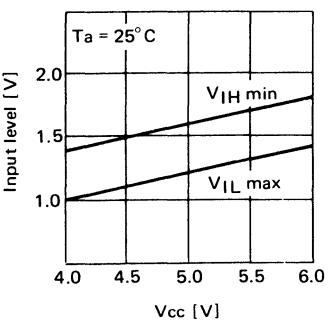
Data Input
v.s. Vcc



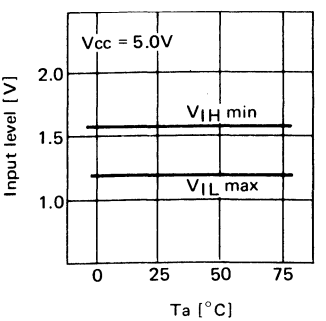
Data Input
v.s. Ta



Clock Input
v.s. Vcc



Clock Input
v.s. Ta



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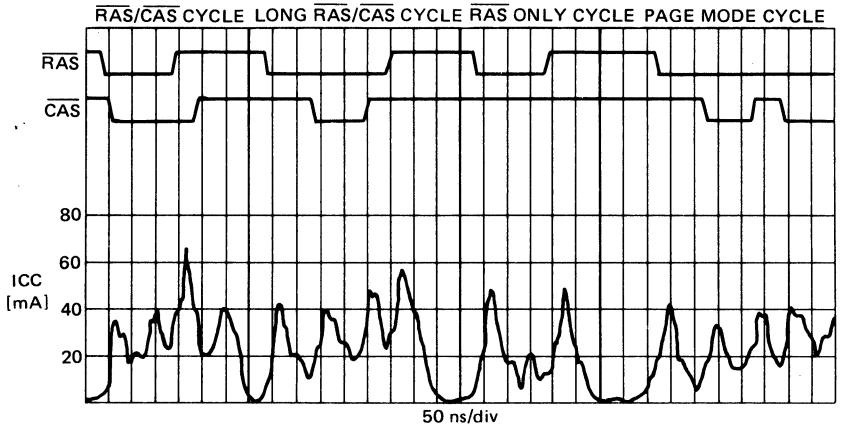
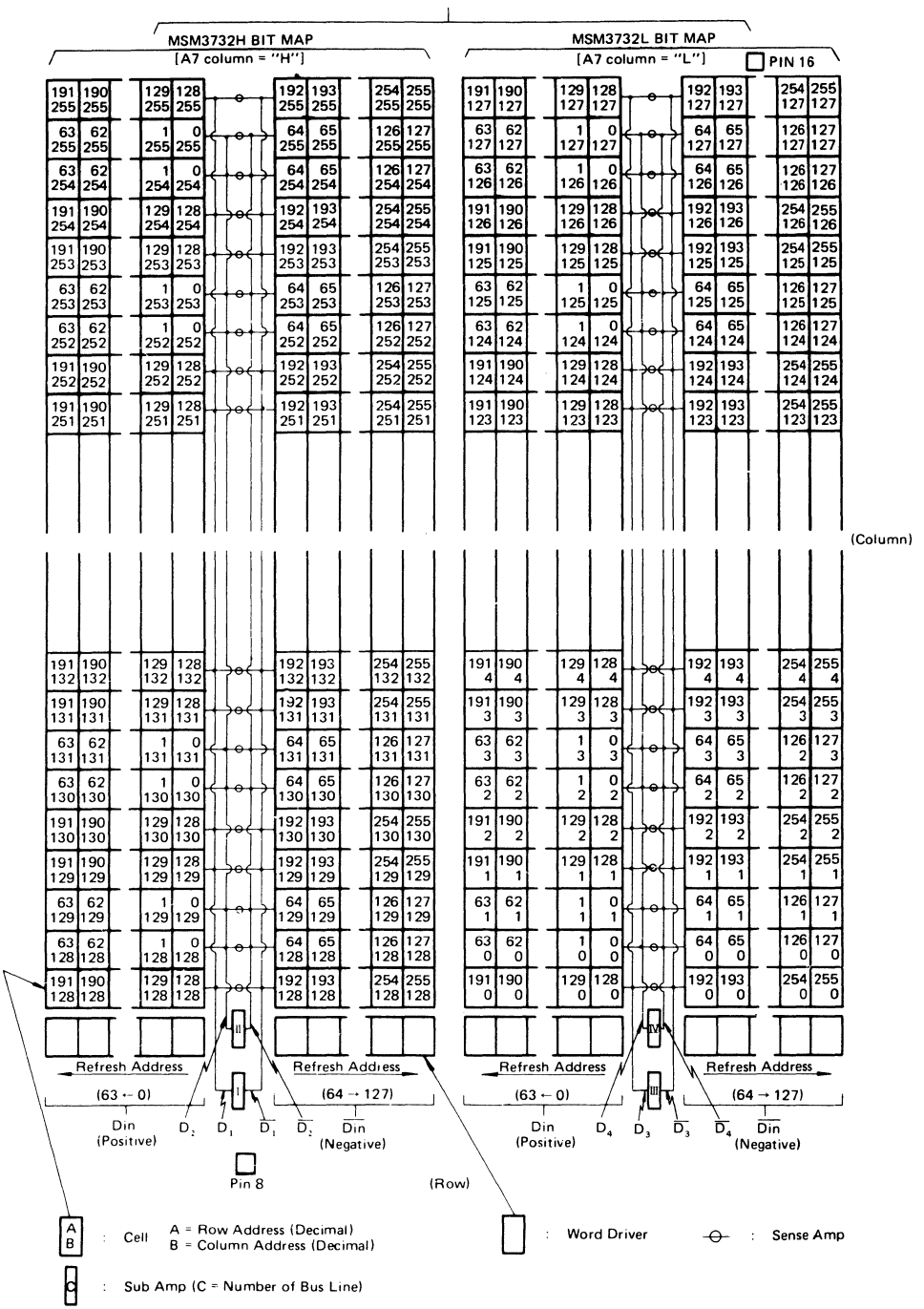

RAS/CAS CYCLE
LONG RAS/CAS CYCLE
RAS ONLY CYCLE
PAGE MODE CYCLE
RAS
CAS
80
60
ICC
[mA]
40
20
50 ns/div

9

MSM3732 Bit MAP (Physical-Decimal)



OKI semiconductor

MSM3764 AS/RS

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION

The Oki MSM3764 is a fully decoded, dynamic NMOS random access memory organized as 65536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

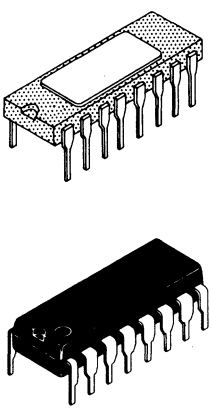
Multiplexed row and column address inputs permit the MSM3764 to be housed in a standard 16 pin DIP. Pin-outs conform to the JEDEC approved pin out.

The MSM3764 is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

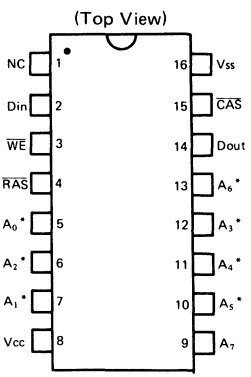
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

- 65,536 x 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  150 ns max (MSM3764-15)
  200 ns max (MSM3764-20)
- Cycle time,
  270 ns min (MSM3764-15)
  330 ns min (MSM3764-20)
- Low power: 248 mW active,
  28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 128 refresh cycles/2 ms
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance



PIN CONFIGURATION



Pin Names	Function
$A_0 \sim A_7$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
Din	Data Input
Dout	Data Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

* Refresh Address

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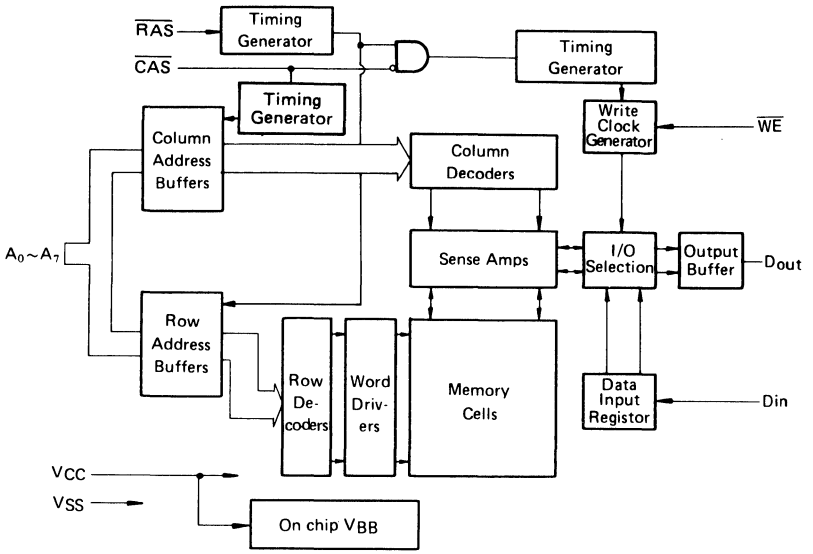
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		45	mA	
Standby Current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		5.0	mA	
Refresh Current* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}		35	mA	
Page Mode Current* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}		42	mA	
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−10	10	μA	
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	μA	
Output Levels Output high voltage (I_{OH} = −5 mA) Output low voltage (I_{OL} = 4.2 mA)	V_{OH} V_{OL}	2.4	 0.4	V V	

Note*: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A_0 ~ A_7, D_{IN})	C_{IN1}	4.5	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	7	10	pF
Output Capacitance (D_{OUT})	C_{OUT}	5	7	pF

Capacitance measured with Boonton Meter.

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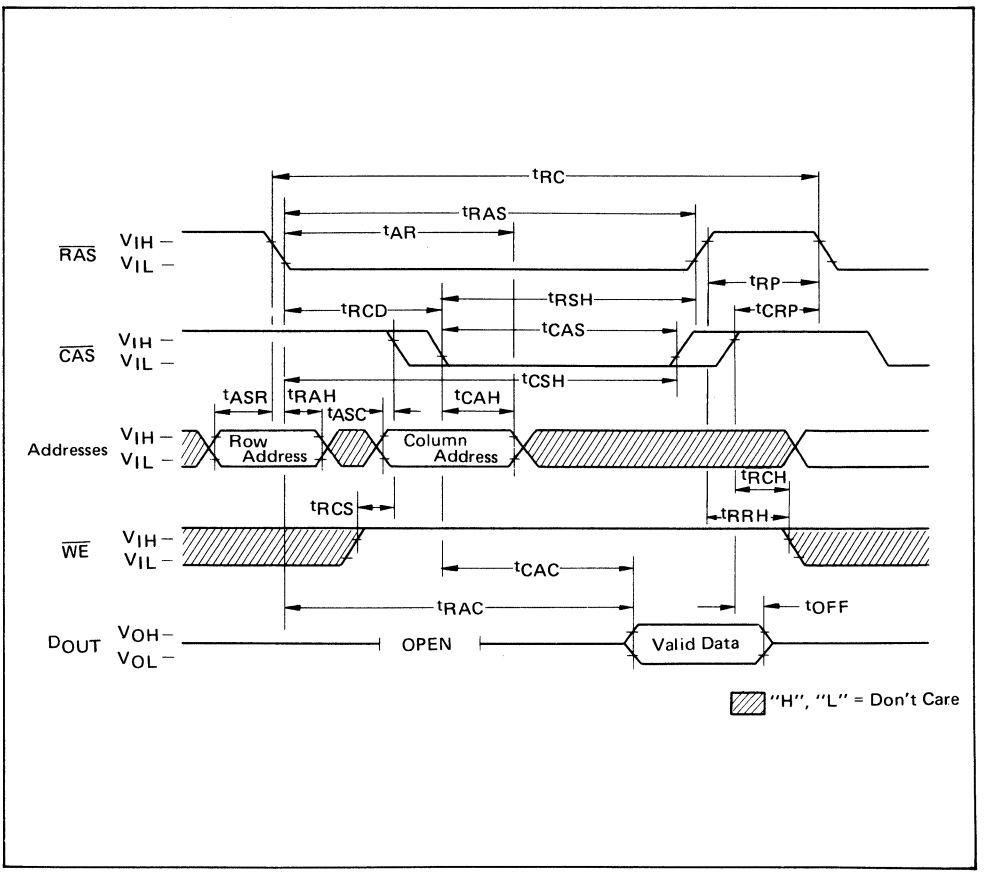
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1,2,3

Parameter	Symbol	Units	MSM3764-15		MSM3764-20		Note
			Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		2		2	
Random read or write cycle time	t_{RC}	ns	270		330		
Read-write cycle time	t_{RWC}	ns	270		330		
Page mode cycle time	t_{PC}	ns	170		225		
Access time from $\overline{RAS}$	t_{RAC}	ns		150		200	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		100		135	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	40	0	50	
Transition time	t_T	ns	3	35	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	100		120		
$\overline{RAS}$ pulse width	t_{RAS}	ns	150	10,000	200	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	100		135		
$\overline{CAS}$ precharge time	t_{CP}	ns	60		80		
$\overline{CAS}$ pulse width	t_{CAS}	ns	100	10,000	135	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	150		200		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	50	30	65	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		
Row Address set-up time	t_{ASR}	ns	0		0		
Row Address hold time	t_{RAH}	ns	15		20		
Column Address set-up time	t_{ASC}	ns	0		0		
Column Address hold time	t_{CAH}	ns	45		55		
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	ns	95		120		
Read command set-up time	t_{RCS}	ns	0		0		
Read command hold time	t_{RCH}	ns	0		0		
Write command set-up time	t_{WCS}	ns	−10		−10		8
Write command hold time	t_{WCH}	ns	45		55		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	95		120		
Write command pulse width	t_{WP}	ns	45		55		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	45		55		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	45		55		
Data-in set-up time	t_{DS}	ns	0		0		
Data-in hold time	t_{DH}	ns	45		55		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	95		120		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	60		80		8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	110		145		8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	20		25		

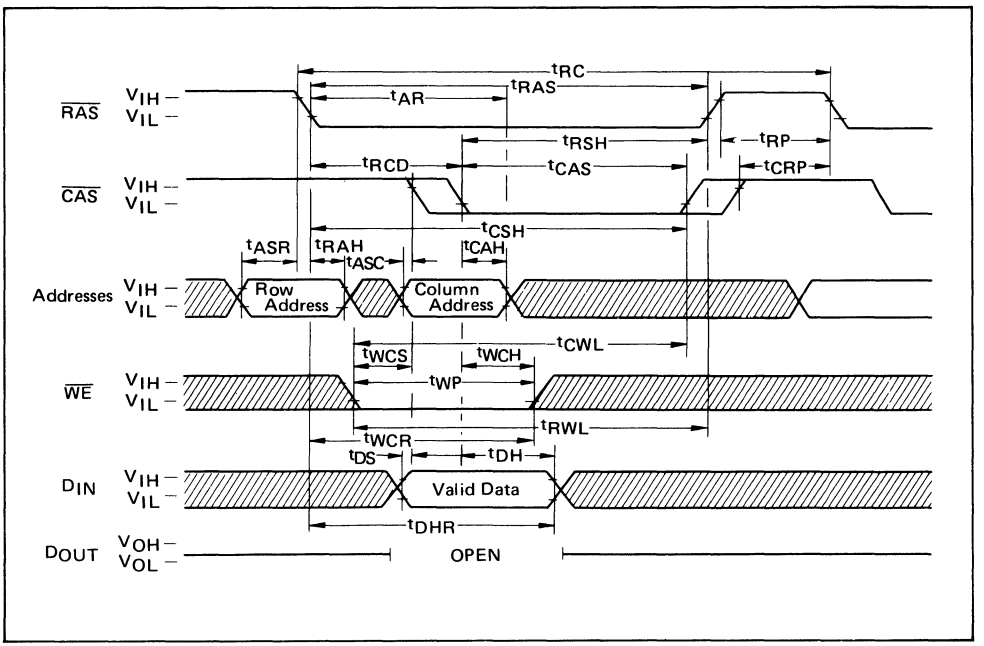
NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Examples; $\overline{RAS}$ only) before proper device operation is achieved.
2) AC measurements assume t_T = 5 ns.
3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4) Assumes that $t_{RCD} \leq t_{RCD}$ (max.).
If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5) Assumes that $t_{RCD} \leq t_{RCD}$ (max.)
6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} > t_{RWD}$ (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

READ CYCLE TIMING

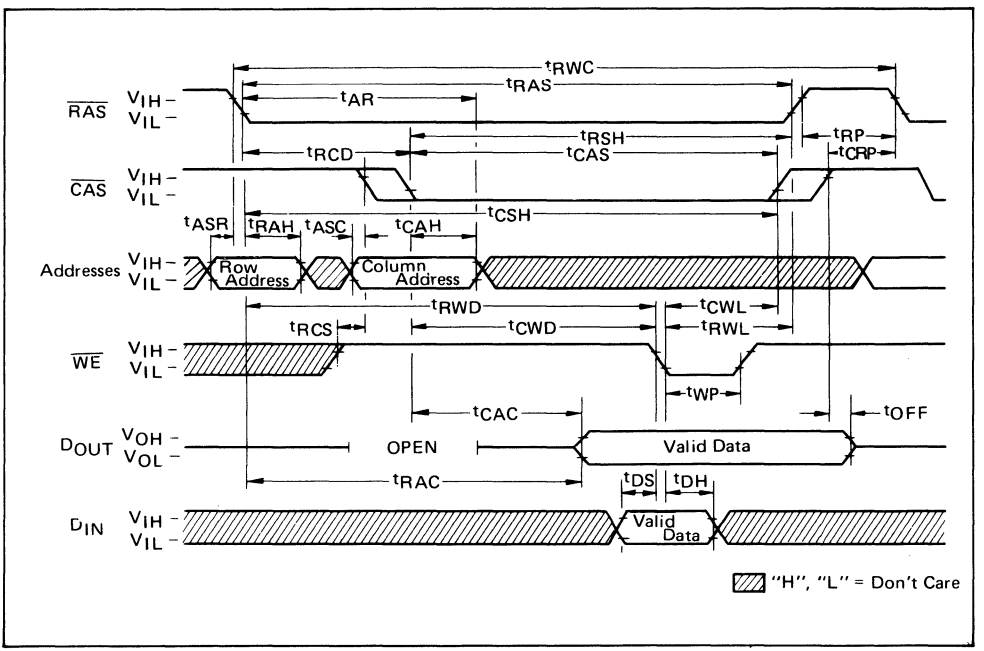


WRITE CYCLE TIMING

(EARLY WRITE)

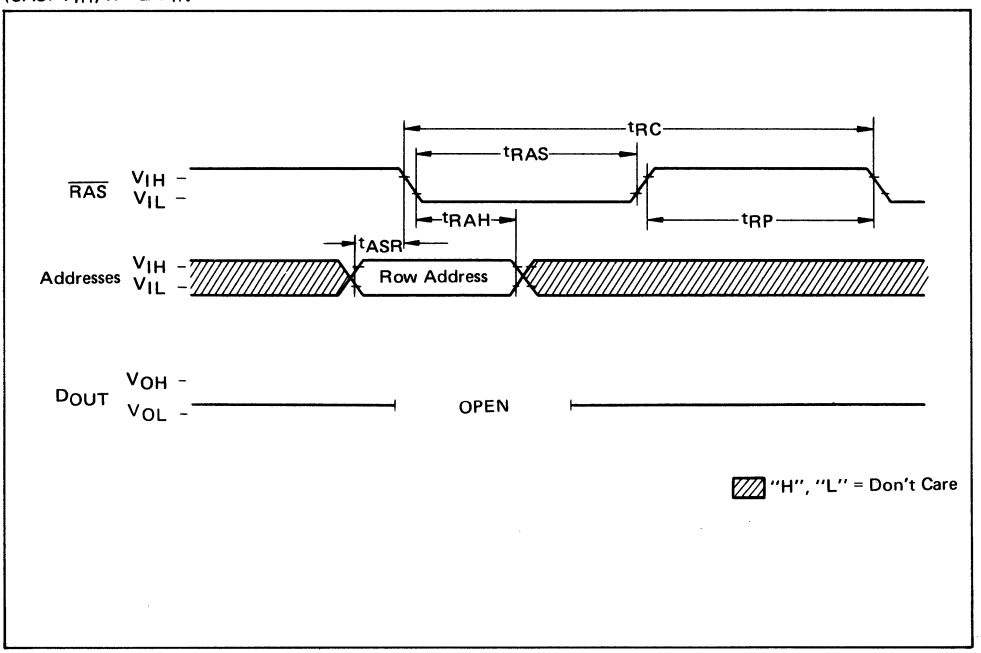


READ-WRITE/READ-MODIFY-WRITE CYCLE

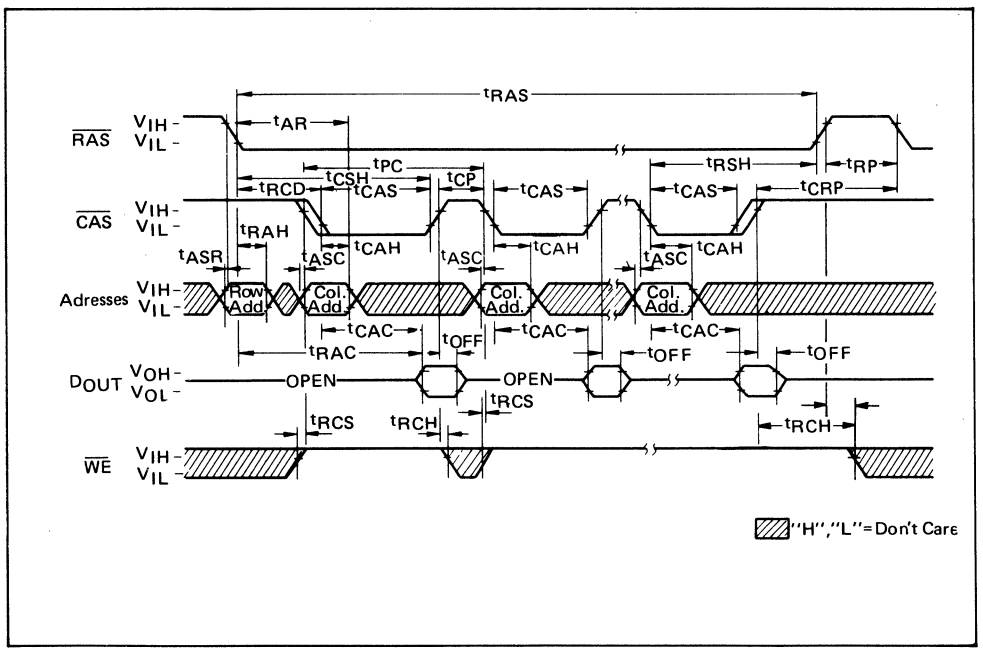


$\overline{RAS}$ ONLY REFRESH TIMING

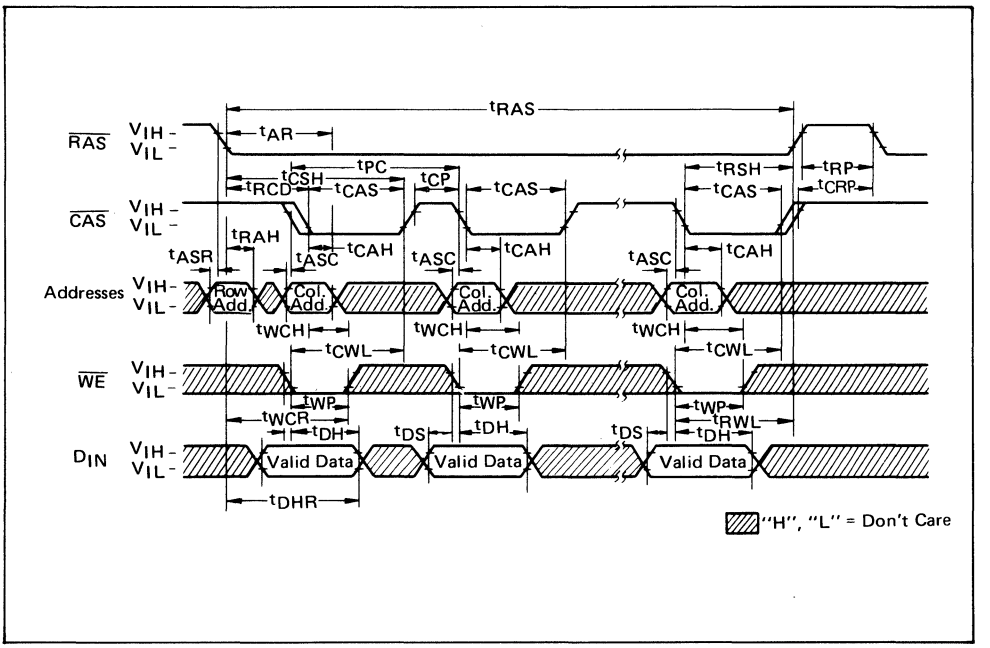
($\overline{CAS}$: V_{IH}, $\overline{WE}$ & D_{IN}: Don't care)



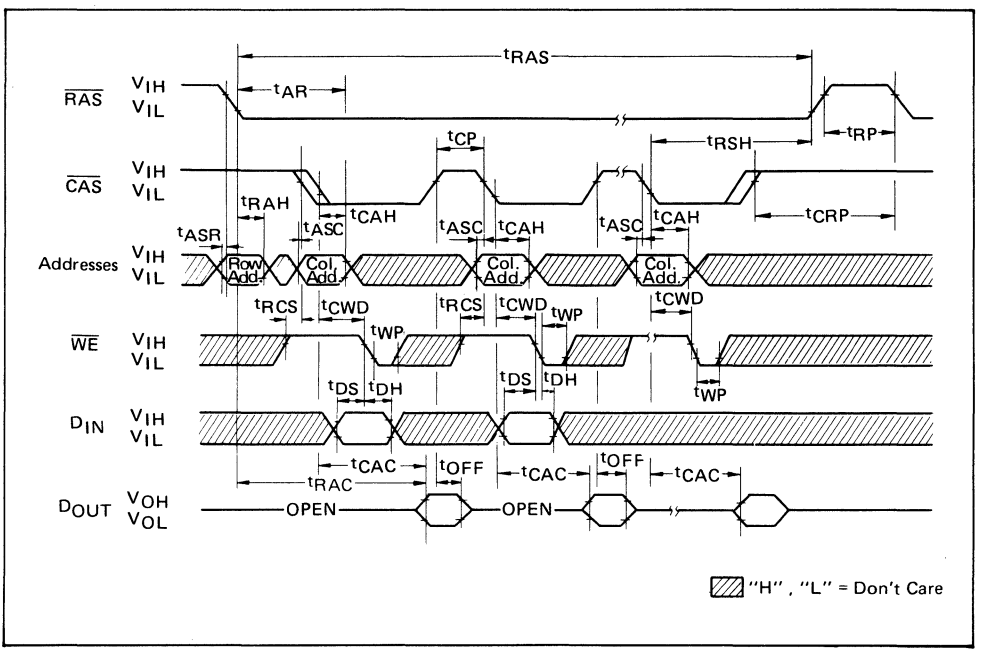
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



PAGE MODE, READ-MODIFY-WRITE CYCLE



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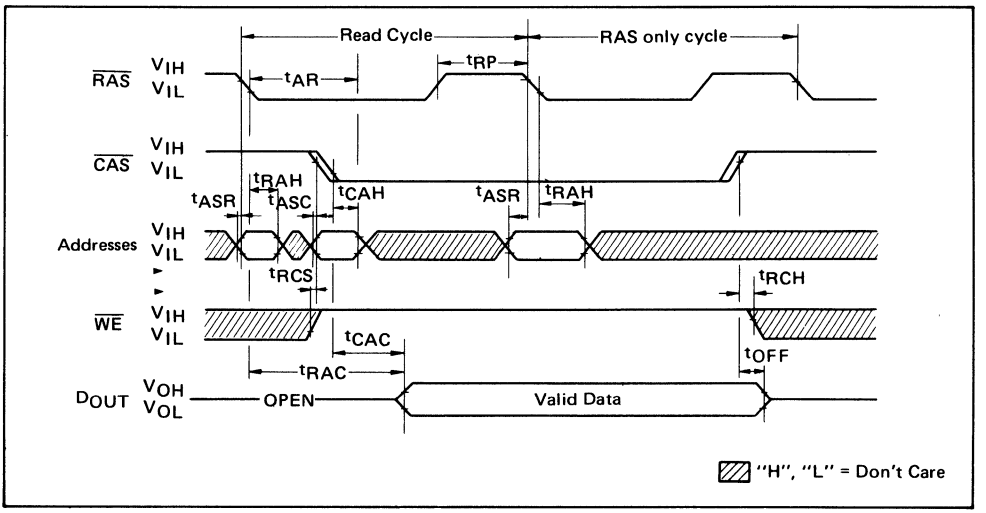
HIDDEN REFRESH



DESCRIPTION

Address Inputs:

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MSM3764. Eight row-address bits are established on the input pins (A_0~A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM3764 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transistion. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSM3764 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses (A_0~A_6) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each rwo to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

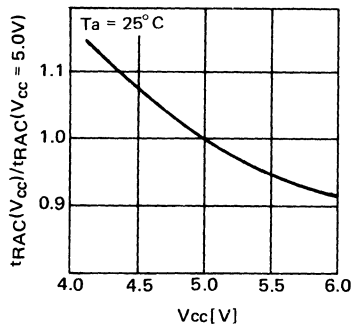
Hidden Refresh:

$\overline{RAS}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

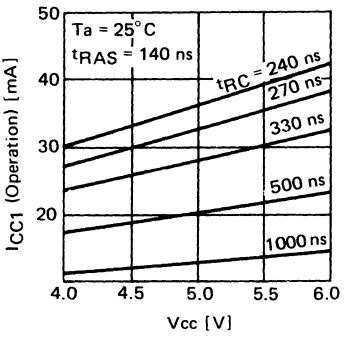
Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

TYPICAL CHARACTERISTICS

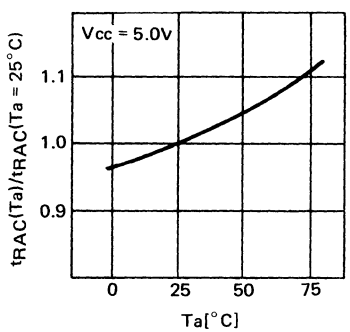
Access time from $\overline{RAS}$
(Relative value) v.s. Vcc



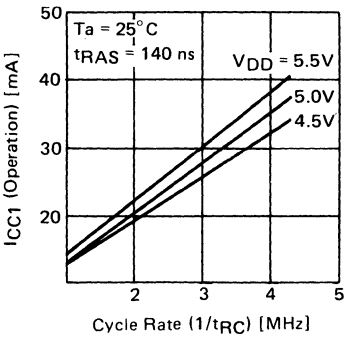
I_{CC1} (t_{RAS}: Constant)
v.s. Vcc



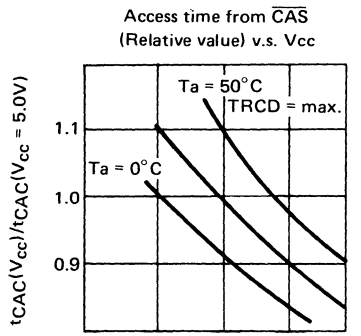
Access time from $\overline{RAS}$
(Relative value) v.s. Ta



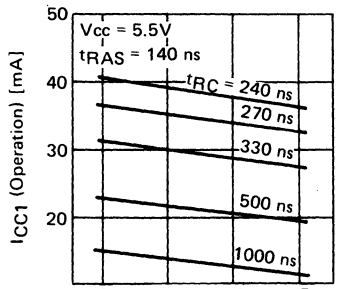
I_{CC1} (t_{RAS}: Constant)
v.s. Cycle rate



Access time from $\overline{CAS}$
(Relative value) v.s. Vcc



I_{CC1} (t_{RAS}: Constant)
v.s. Ta



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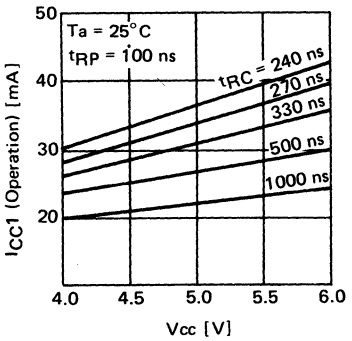
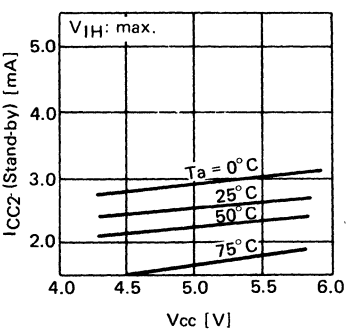
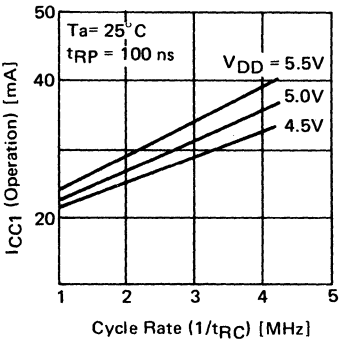
I_{CC1} (t_{RP}: Constant)
v.s. Vcc



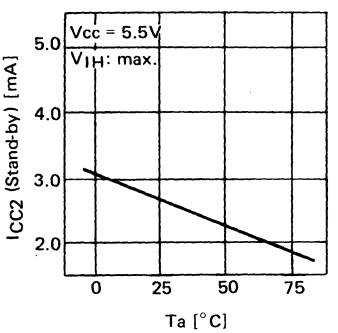
I_{CC2} v.s. Vcc



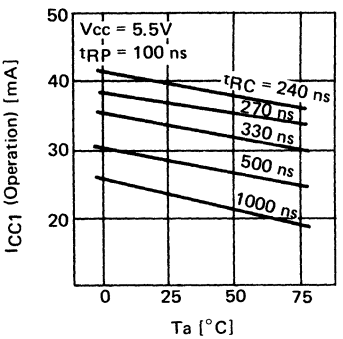
I_{CC1} (t_{RP}: Constant)
v.s. Cycle rate



I_{CC2} v.s. Ta



I_{CC1} (t_{RP}: Constant)
v.s. Ta



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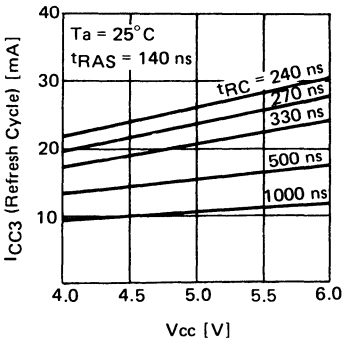
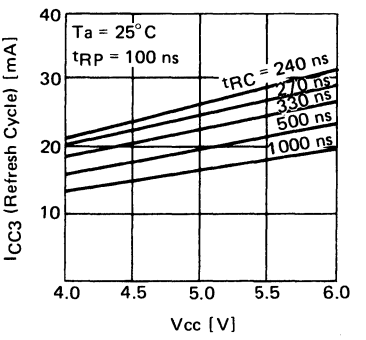
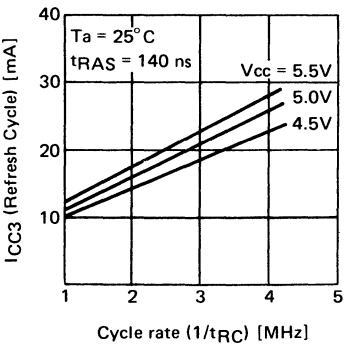
I_{CC3} (t_{RAS}: Constant)
v.s Vcc



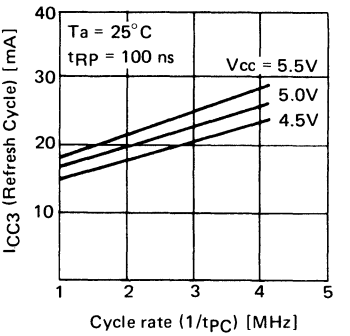
I_{CC3} (t_{RP}: Constant)
v.s. Vcc



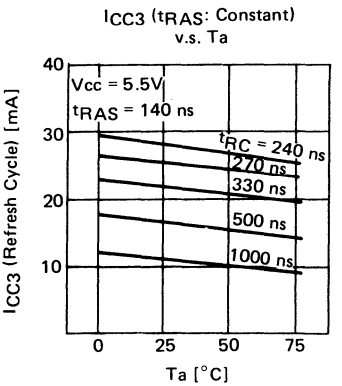
I_{CC3} (t_{RAS}: Constant)
v.s. Cycle rate



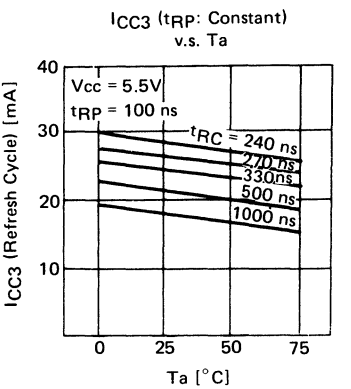
I_{CC3} (t_{RP}: Constant)
v.s. Cycle rate



I_{CC3} (t_{RAS}: Constant)
v.s. Ta



I_{CC3} (t_{RP}: Constant)
v.s. Ta



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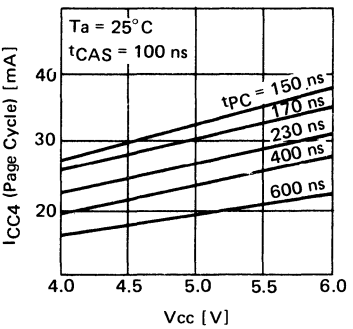
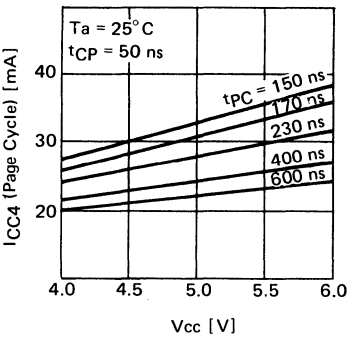
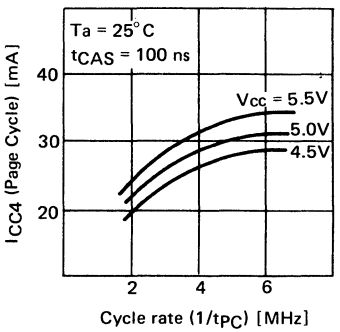
I_{CC4} (t_{CAS}: Constant)
v.s. Vcc



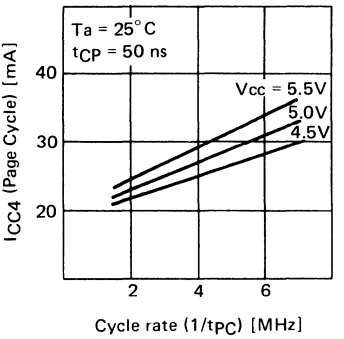
I_{CC4} (t_{CP}: Constant)
v.s. Vcc



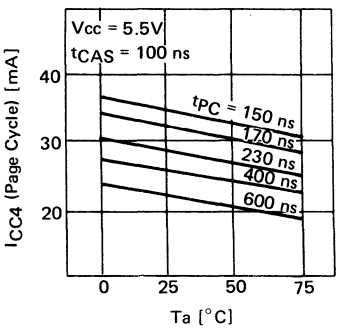
I_{CC4} (t_{CAS}: Constant)
v.s. Cycle rate



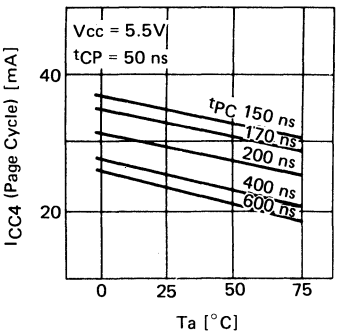
I_{CC4} (t_{CP}: Constant)
v.s. Cycle rate



I_{CC4} (t_{CAS}: Constant)
v.s. Ta



I_{CC4} (t_{CP}: Constant)
v.s. Ta



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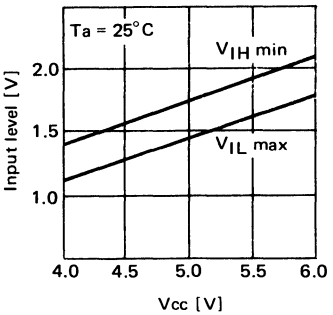
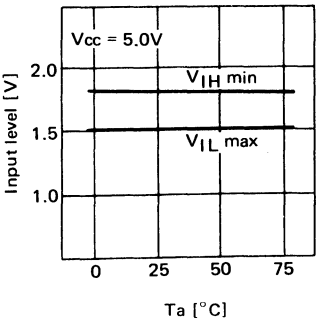
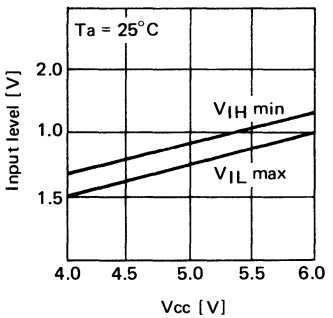
Address Input
v.s Vcc



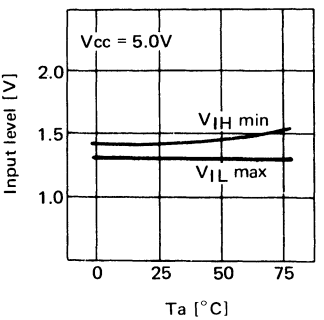
Address Input
v.s. Ta



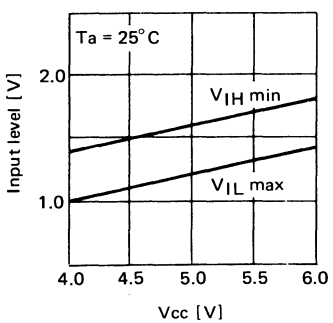
Data Input
v.s. Vcc



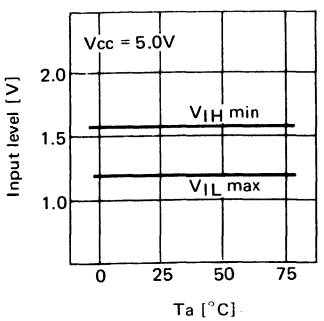
Data Input
v.s. Ta



Clock Input
v.s. Vcc



Clock Input
v.s. Ta



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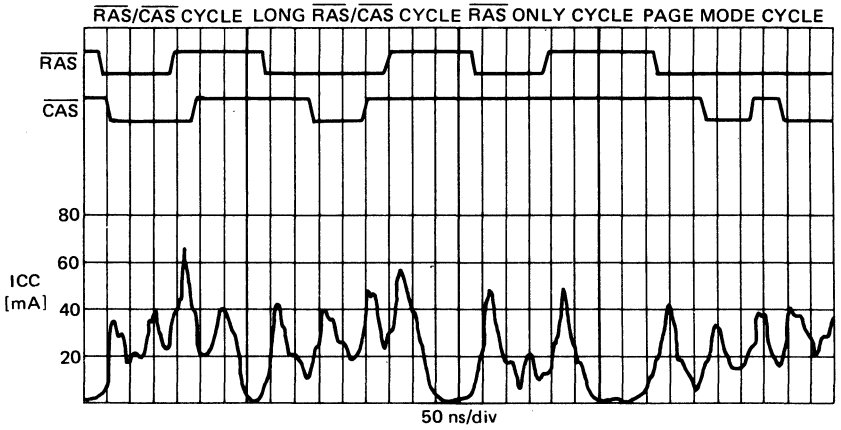
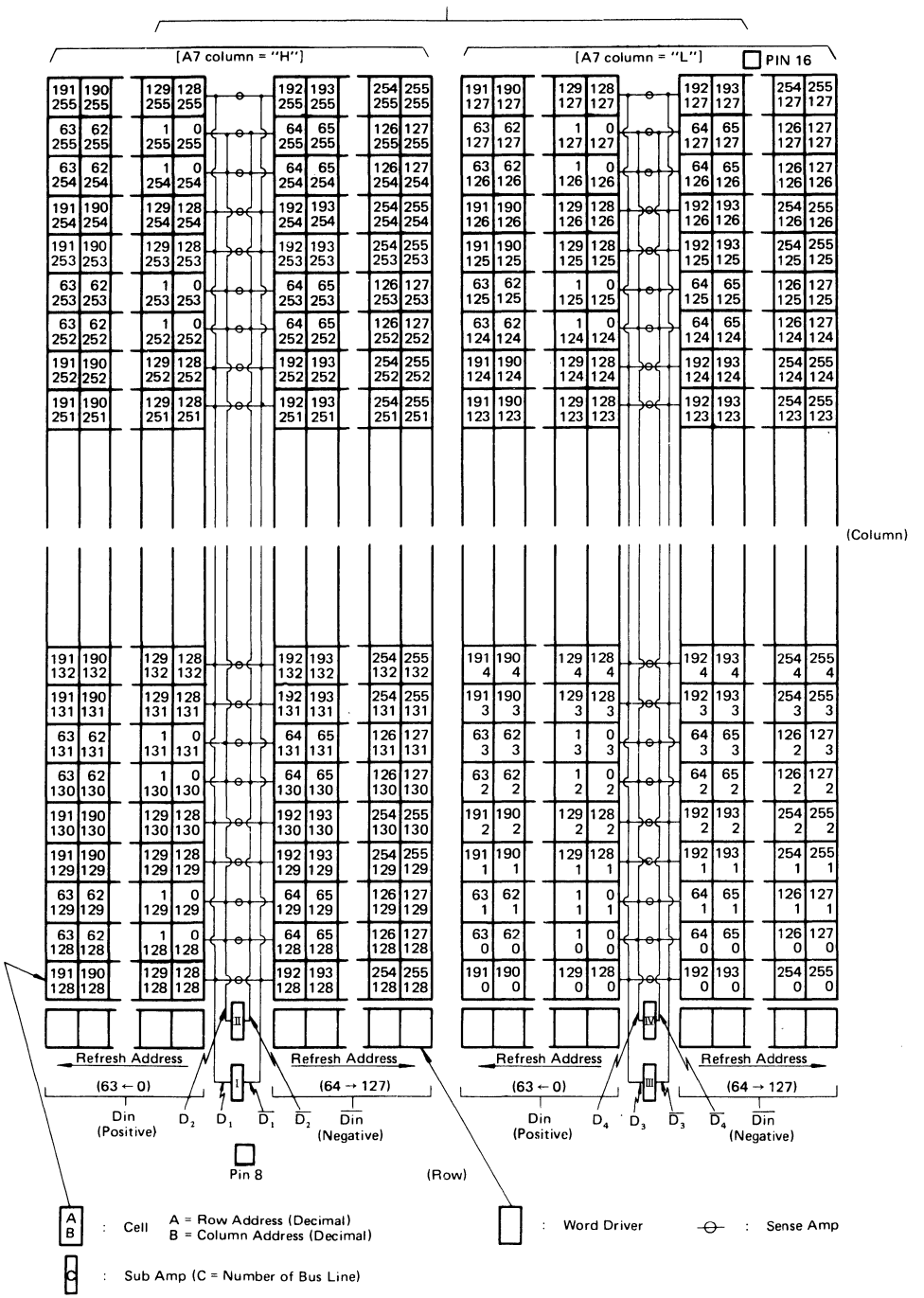

RAS/CAS CYCLE LONG RAS/CAS CYCLE RAS ONLY CYCLE PAGE MODE CYCLE
RAS
CAS
80
60
ICC
[mA]
40
20
50 ns/div

MSM3764 Bit MAP (Physical-Decimal)



OKI semiconductor

MSM3764 AAS/RS

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY (E3-S-004-32)

GENERAL DESCRIPTION

The Oki MSM3764A is a fully decoded, dynamic NMOS random access memory organized as 65536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

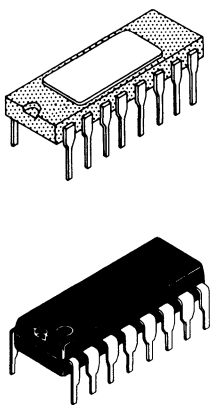
Multiplexed row and column address inputs permit the MSM3764A to be housed in a standard 16 pin DIP. Pin-outs conform to the JEDEC approved pin out.

The MSM3764A is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

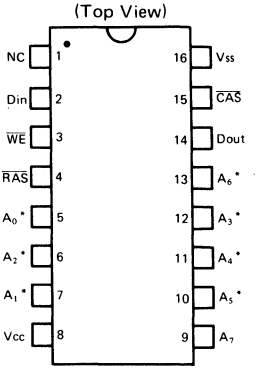
FEATURES

- 65,536 x 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  120 ns max (MSM3764A-12)
  150 ns max (MSM3764A-15)
  200 ns max (MSM3764A-20)
- Cycle time,
  230 ns min (MSM3764A-12)
  260 ns min (MSM3764A-15)
  330 ns min (MSM3764A-20)
- Low power: 330 mW active,
  28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 128 refresh cycles/2 ms
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance



PIN CONFIGURATION

(Top View)



Pin Names	Function
$A_0 \sim A_7$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
Din	Data Input
Dout	Data Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

* Refresh Address

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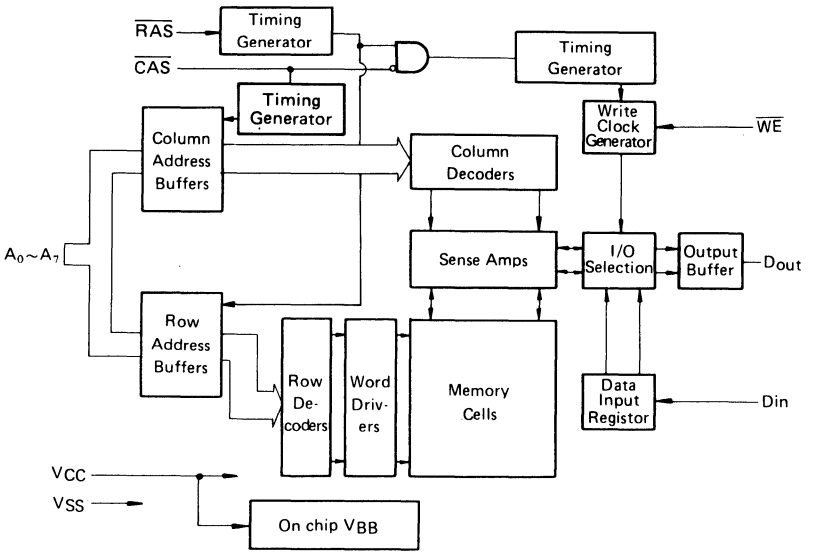
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		60	mA	
Standby Current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		5.0	mA	
Refresh Current* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}		40	mA	
Page Mode Current* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}		60	mA	
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−10	10	μA	
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	μA	
Output Levels Output high voltage (I_{OH} = −5 mA) Output low voltage (I_{OL} = 4.2 mA)	V_{OH} V_{OL}	2.4	 0.4	V V	

Note*: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A_0 ~ A_7, D_{IN})	C_{IN1}	–	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	–	8	pF
Output Capacitance (D_{OUT})	C_{OUT}	–	7	pF

Capacitance measured with Boonton Meter.

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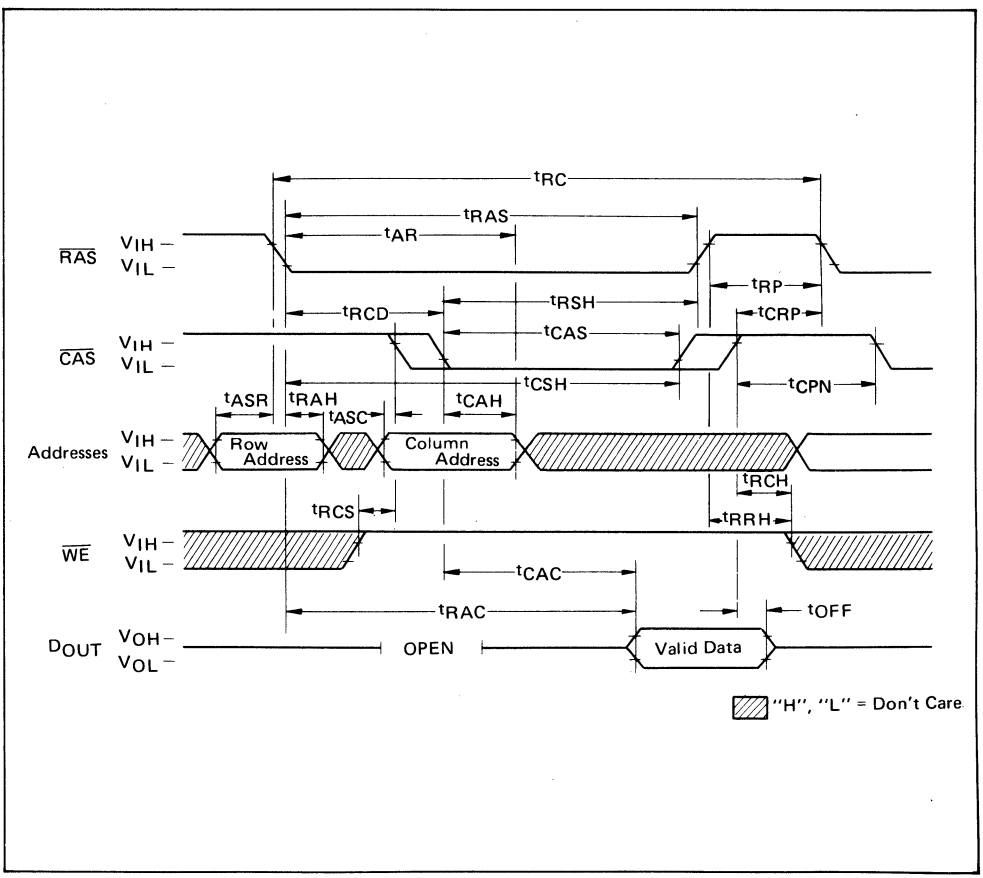
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1,2,3

Parameter	Symbol	Units	MSM3764A-12		MSM3764A-15		MSM3764A-20		Note
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		2		2		2	
Random read or write cycle time	t_{RC}	ns	220		260		330		
Read-write cycle time	t_{RWC}	ns	245		280		345		
Page mode cycle time	t_{PC}	ns	120		145		190		
Access time from $\overline{RAS}$	t_{RAC}	ns		120		150		200	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		60		75		100	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	35	0	40	0	50	
Transition time	t_T	ns	3	35	3	35	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		100		120		
$\overline{RAS}$ pulse width	t_{RAS}	ns	120	10,000	150	10,000	200	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	60		75		100		
$\overline{CAS}$ precharge time (Page cycle)	t_{CP}	ns	50		60		80		
$\overline{CAS}$ pulse width	t_{CAS}	ns	60	10,000	75	10,000	100	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	120		150		200		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	60	25	75	30	100	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		0		
Row Address set-up time	t_{ASR}	ns	0		0		0		
Row Address hold time	t_{RAH}	ns	15		15		20		
Column Address set-up time	t_{ASC}	ns	0		0		0		
Column Address hold time	t_{CAH}	ns	20		20		25		
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	ns	80		95		125		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time	t_{RCH}	ns	0		0		0		
Write command set-up time	t_{WCS}	ns	−10		−10		−10		8
Write command hold time	t_{WCH}	ns	40		45		55		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	100		120		155		
Write command pulse width	t_{WP}	ns	40		45		55		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	40		45		55		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	40		45		55		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	40		45		55		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	100		120		155		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	40		45		55		8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	100		120		155		8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	0		0		0		
$\overline{CAS}$ precharge time	t_{CPN}	ns	30		35		45		

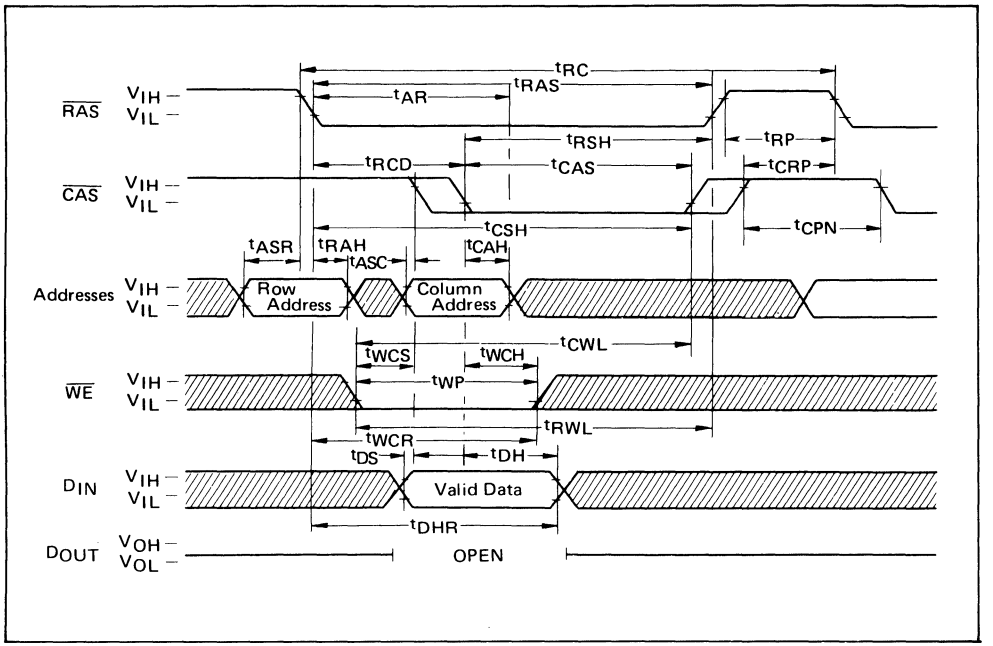
NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Examples; $\overline{RAS}$ only) before proper device operation is achieved.
2) AC measurements assume t_T = 5 ns.
3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4) Assumes that $t_{RCD} < t_{RCD}$ (max.).
If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5) Assumes that $t_{RCD} < t_{RCD}$ (max.)
6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} > t_{RWD}$ (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

READ CYCLE TIMING

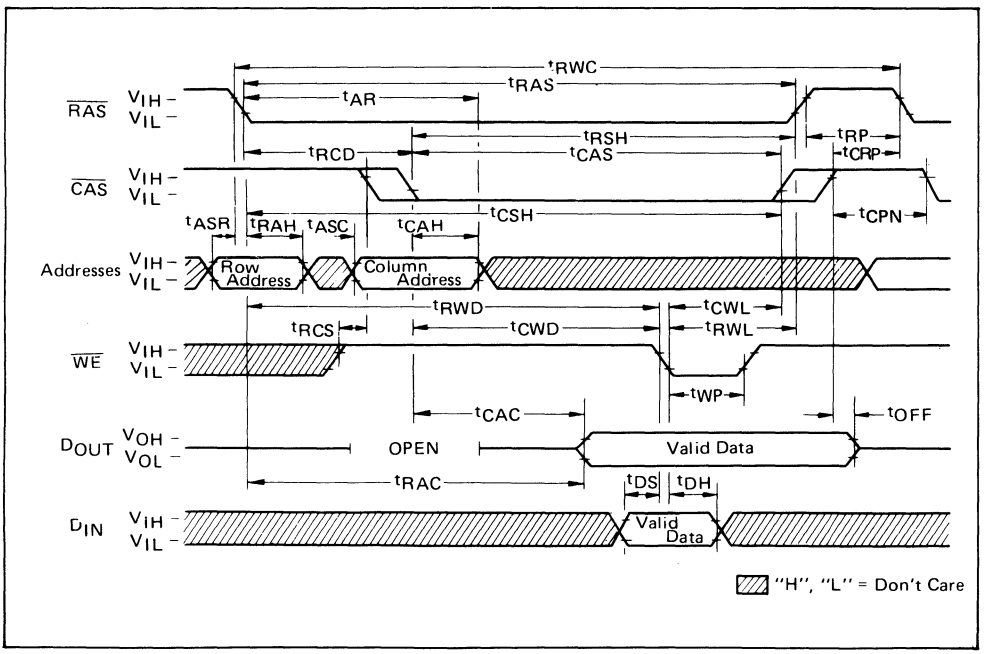


WRITE CYCLE TIMING

(EARLY WRITE)

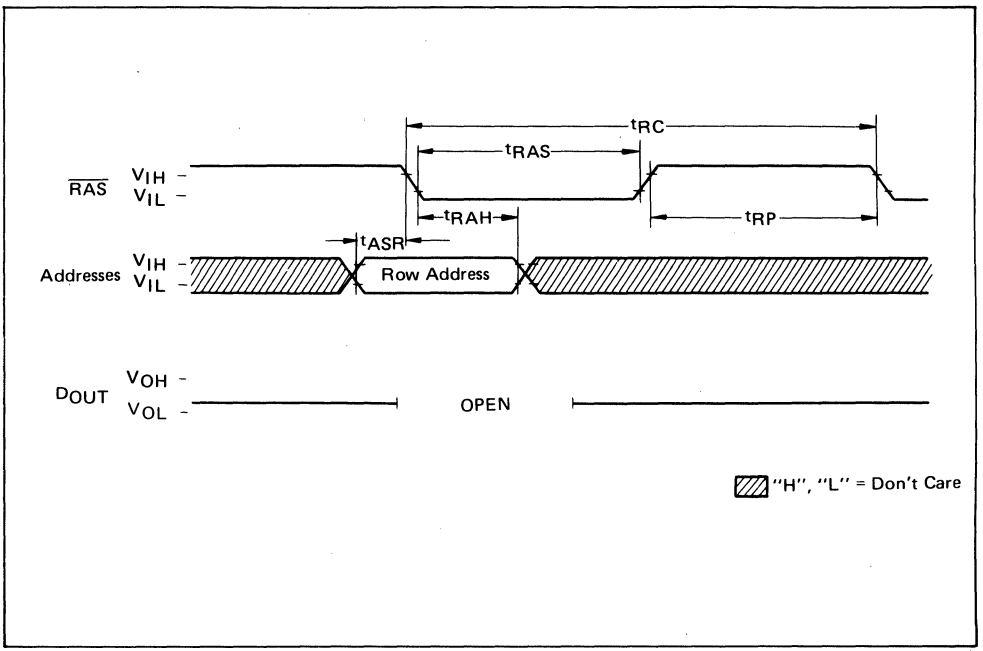


READ-WRITE/READ-MODIFY-WRITE CYCLE

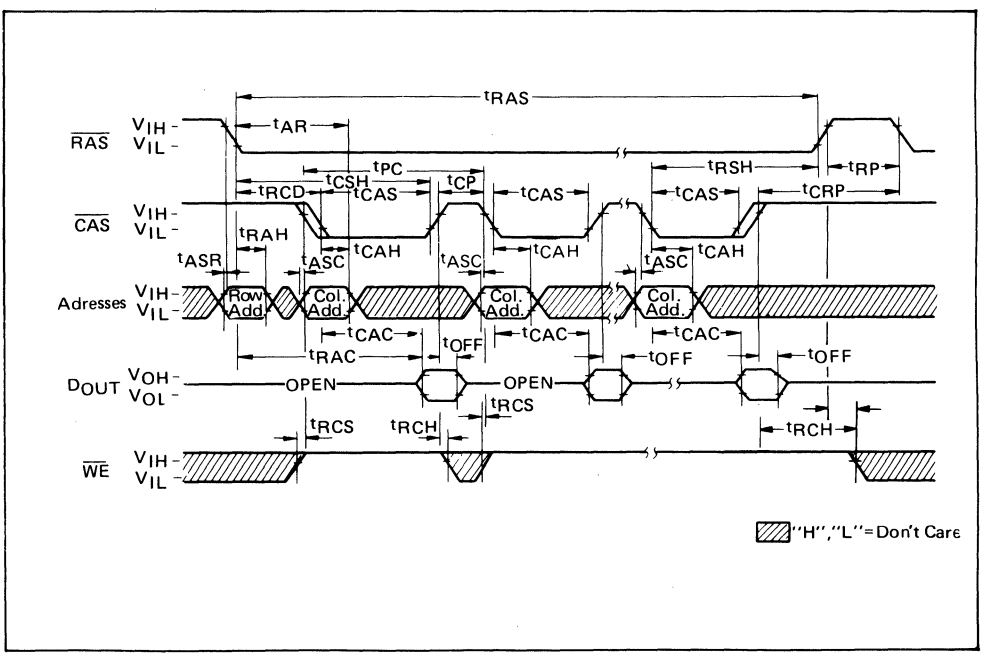


$\overline{RAS}$ ONLY REFRESH TIMING

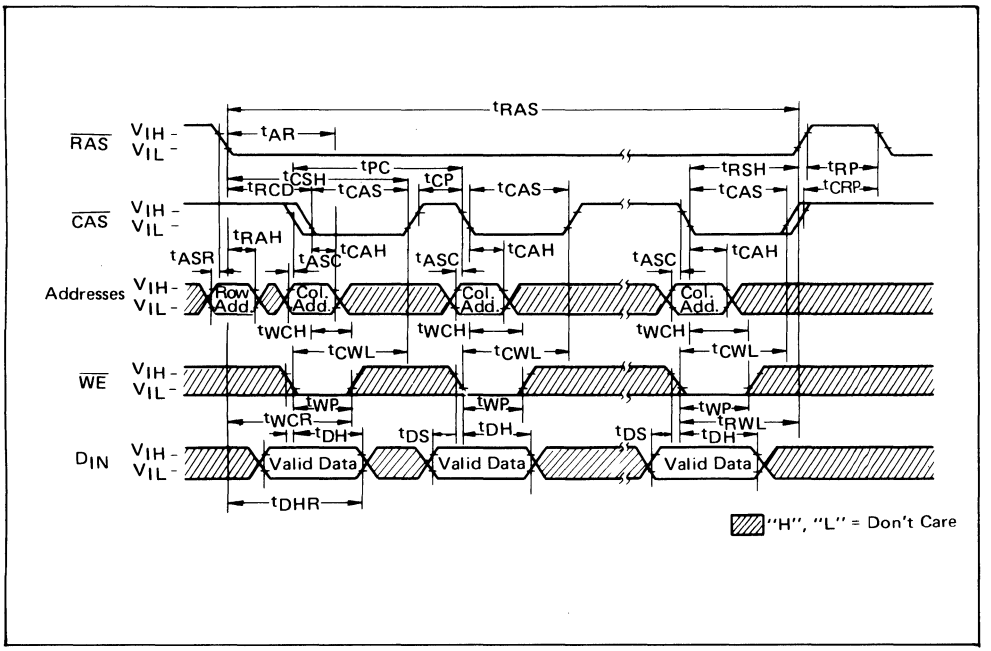
($\overline{CAS}$: V_{IH}, $\overline{WE}$ & D_{IN}: Don't care)



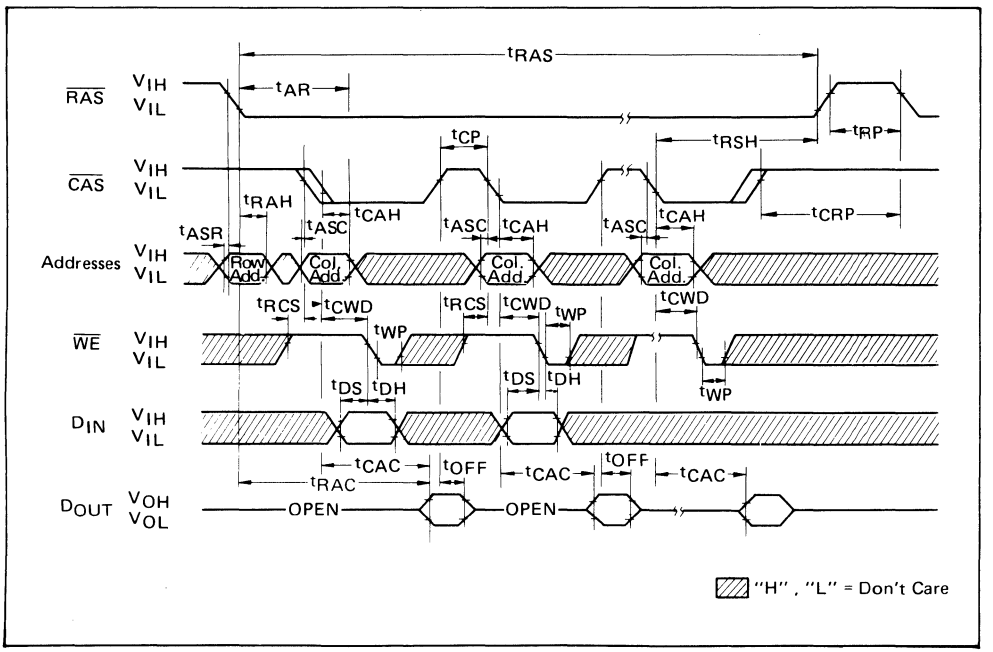
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



PAGE MODE, READ-MODIFY-WRITE CYCLE



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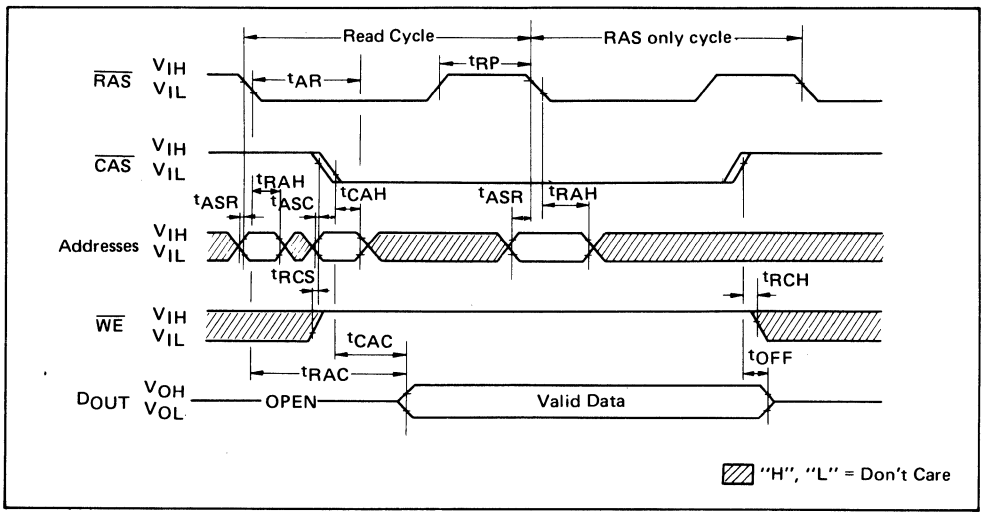
HIDDEN REFRESH



DESCRIPTION

Address Inputs:

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MSM3764A. Eight row-address bits are established on the input pins (A_0~A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM3764A during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transistion. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSM3764A while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

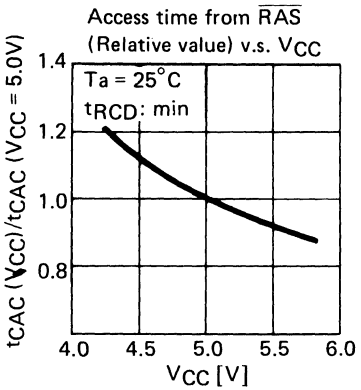
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses (A_0~A_6) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each rwo to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

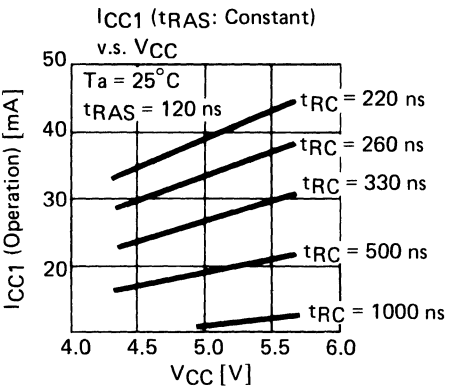
Hidden Refresh:

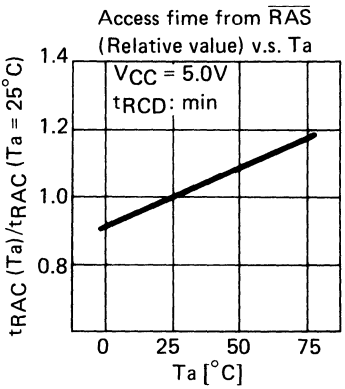
$\overline{RAS}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

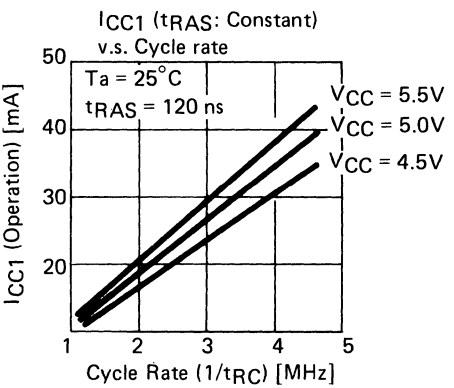
Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

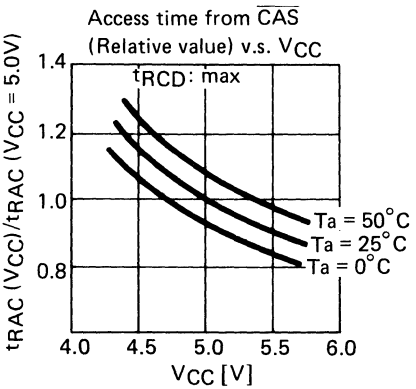
TYPICAL CHARACTERISTICS

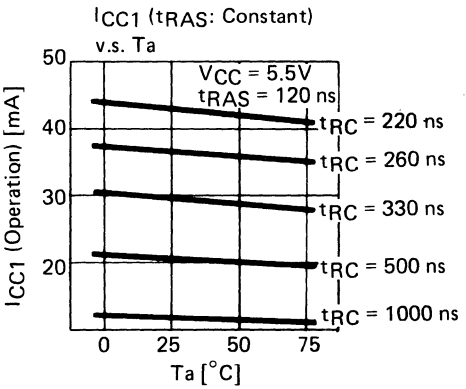












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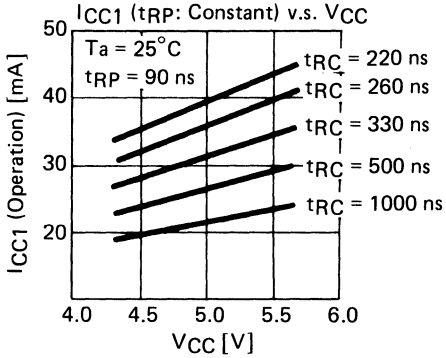
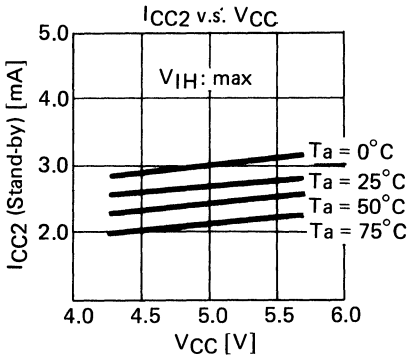
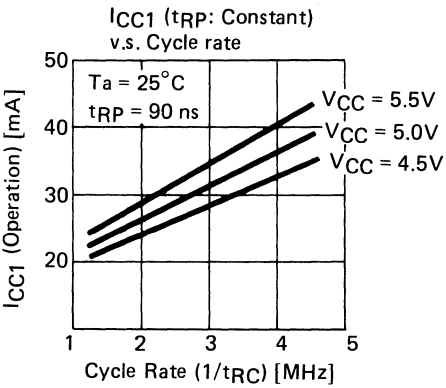
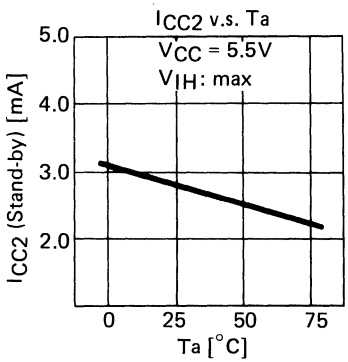
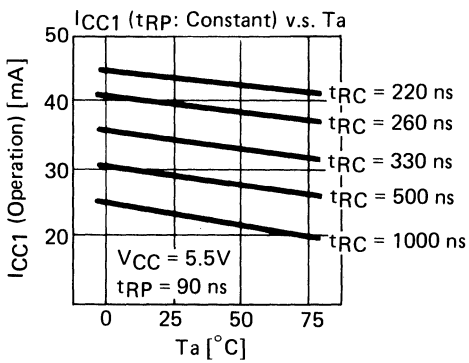

ICC1 (tRP: Constant) v.s. VCC
Ta = 25°C
tRP = 90 ns
tRC = 220 ns
tRC = 260 ns
tRC = 330 ns
tRC = 500 ns
tRC = 1000 ns
ICC1 (Operation) [mA]
50
40
30
20
4.0
4.5
5.0
5.5
6.0
VCC [V]


ICC2 v.s. VCC
VIH: max
Ta = 0°C
Ta = 25°C
Ta = 50°C
Ta = 75°C
ICC2 (Stand-by) [mA]
5.0
4.0
3.0
2.0
4.0
4.5
5.0
5.5
6.0
VCC [V]

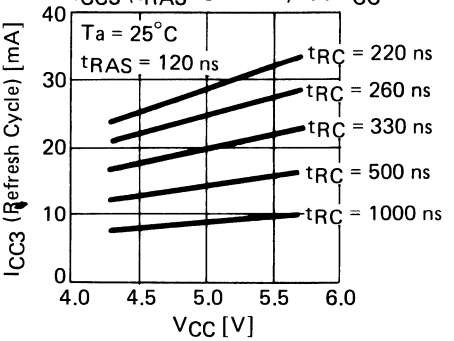

ICC1 (tRP: Constant)
v.s. Cycle rate
Ta = 25°C
tRP = 90 ns
VCC = 5.5V
VCC = 5.0V
VCC = 4.5V
ICC1 (Operation) [mA]
50
40
30
20
1
2
3
4
5
Cycle Rate (1/tRC) [MHz]


ICC2 v.s. Ta
VCC = 5.5V
VIH: max
ICC2 (Stand-by) [mA]
5.0
4.0
3.0
2.0
0
25
50
75
Ta [°C]

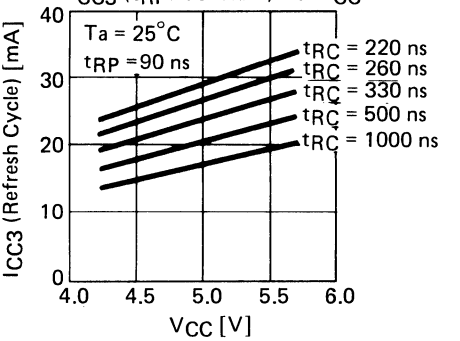

ICC1 (tRP: Constant) v.s. Ta
tRC = 220 ns
tRC = 260 ns
tRC = 330 ns
tRC = 500 ns
tRC = 1000 ns
VCC = 5.5V
tRP = 90 ns
ICC1 (Operation) [mA]
50
40
30
20
0
25
50
75
Ta [°C]

9

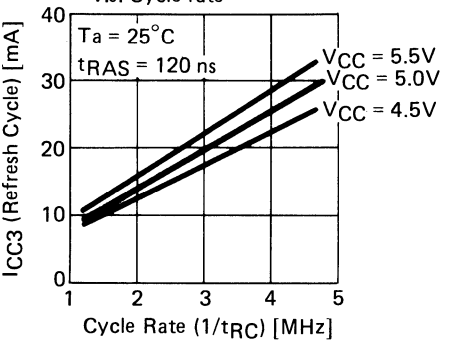
I_{CC3} (t_{RAS}: Constant) v.s. V_{CC}



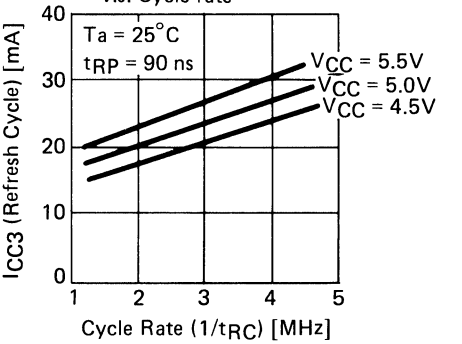
I_{CC3} (t_{RP}: Constant) v.s. V_{CC}



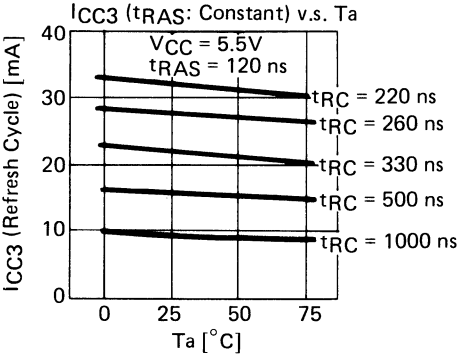
I_{CC3} (t_{RAS}: Constant)
v.s. Cycle rate



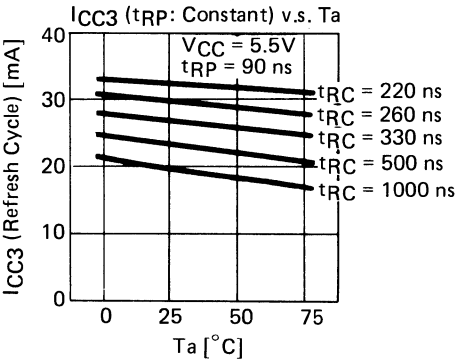
I_{CC3} (t_{RP}: Constant)
v.s. Cycle rate



I_{CC3} (t_{RAS}: Constant) v.s. Ta

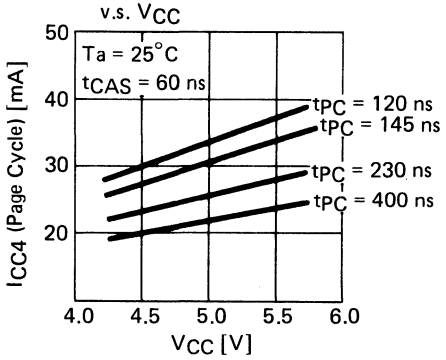


I_{CC3} (t_{RP}: Constant) v.s. Ta

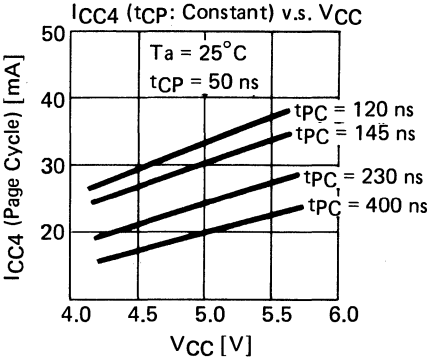


9

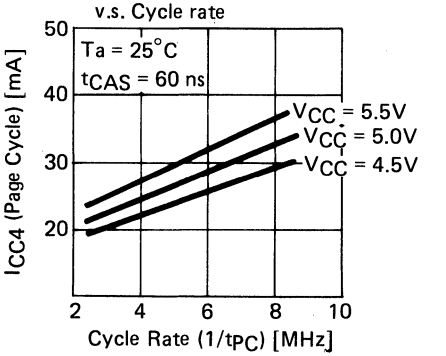
I_{CC4} (t_{CAS}: Constant) v.s. V_{CC}



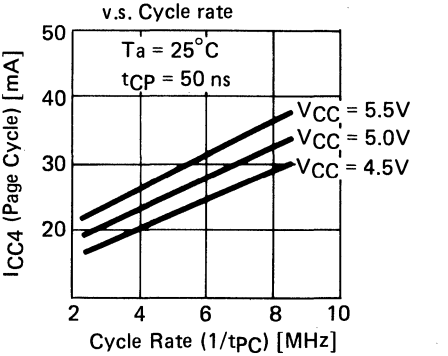
I_{CC4} (t_{CP}: Constant) v.s. V_{CC}



I_{CC4} (t_{CAS}: Constant) v.s. Cycle rate

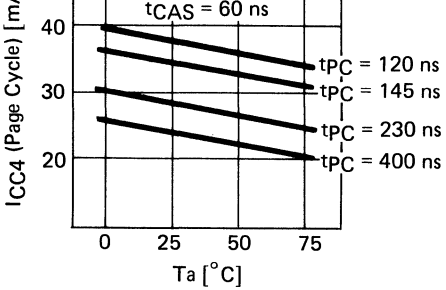


I_{CC4} (t_{CP}: Constant) v.s. Cycle rate

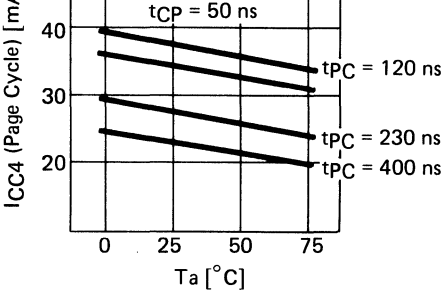


9

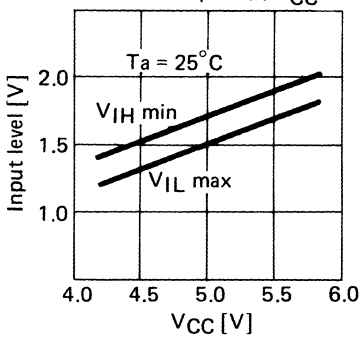
I_{CC4} (t_{CAS}: Constant) v.s. Ta



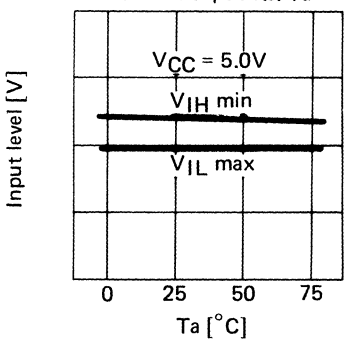
I_{CC4} (t_{CP}: Constant) v.s. Ta



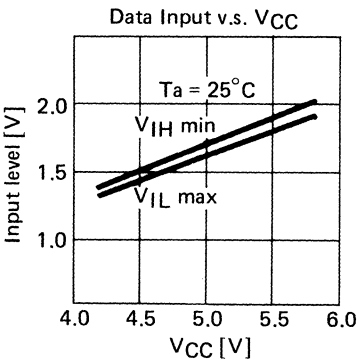
Address Input v.s. V_{CC}



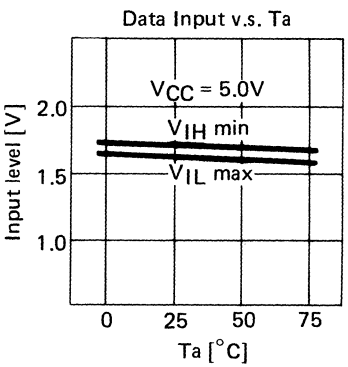
Address Input v.s. Ta



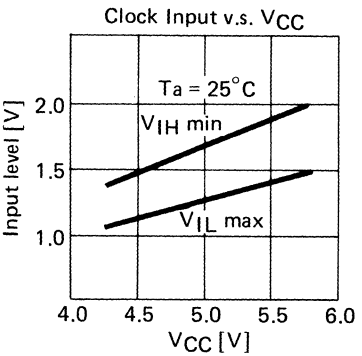
Data Input v.s. V_{CC}



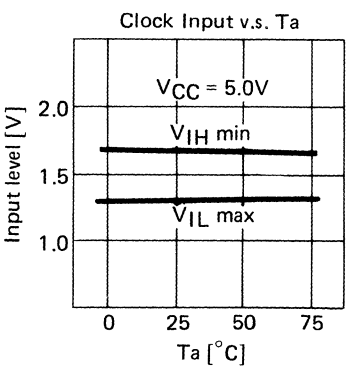
Data Input v.s. Ta



Clock Input v.s. V_{CC}

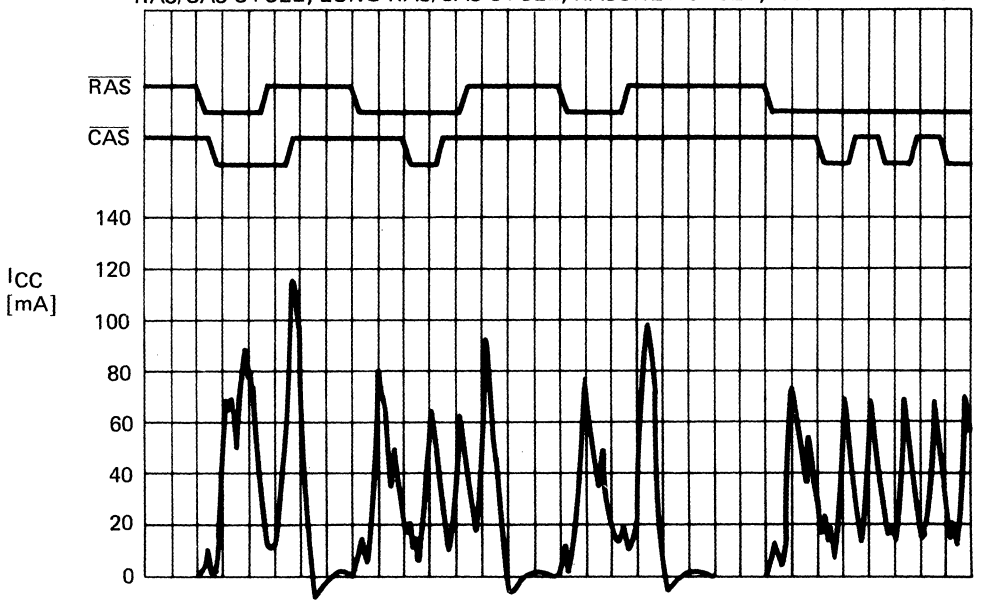


Clock Input v.s. Ta

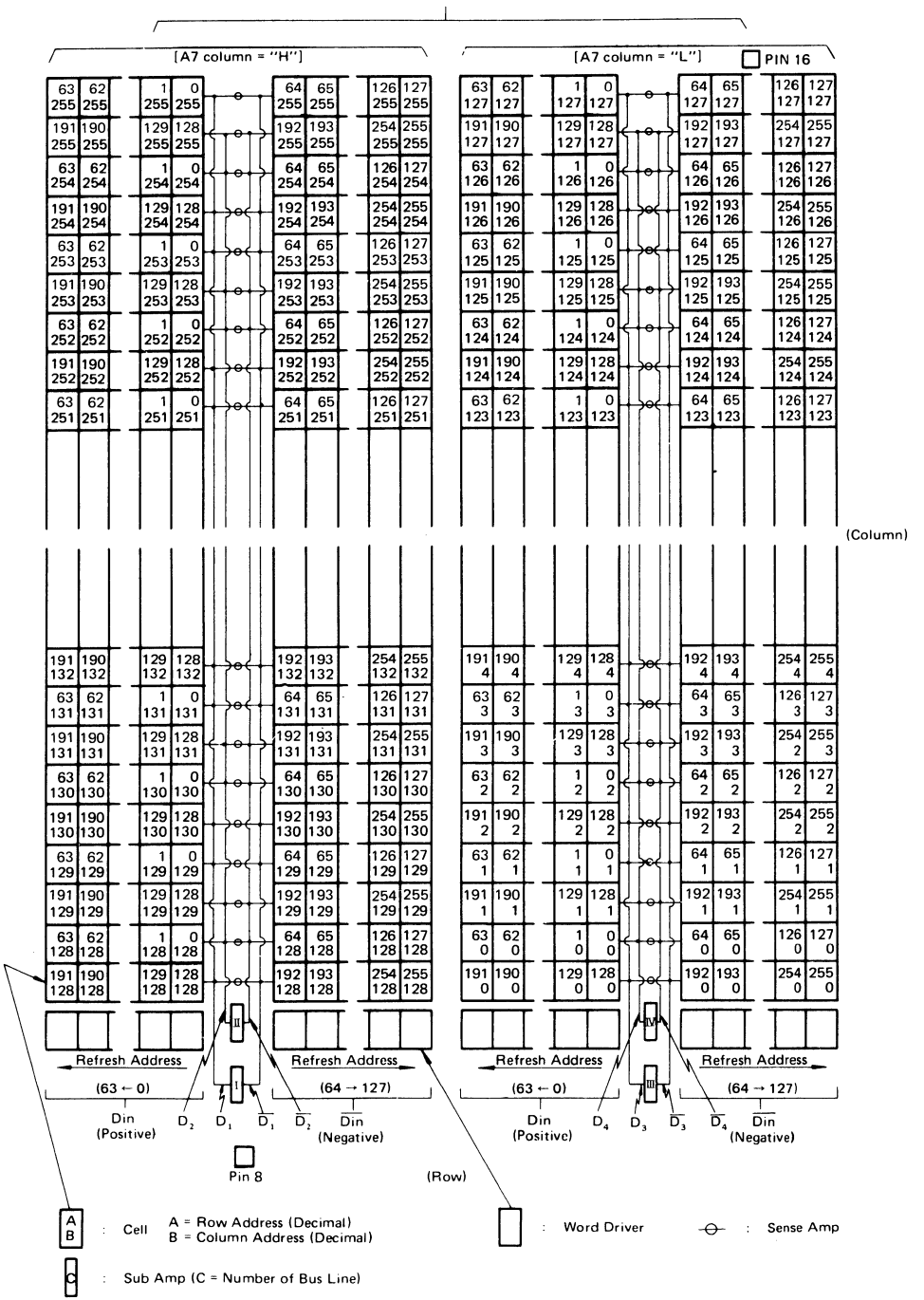


V_{CC} = 5.5V
Ta = 25°C
50 ns/div

RAS/CAS CYCLE, LONG RAS/CAS CYCLE, RASONLY CYCLE, PAGE MODE CYCLE



MSM3764A Bit MAP (Physical-Decimal)



MSM41256AS/RS

262144-BIT DYNAMIC RANDOM ACCESS MEMORY < Page Mode Type >

GENERAL DESCRIPTION

The Oki MSM41256 is a fully decoded, dynamic NMOS random access memory organized as 262144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

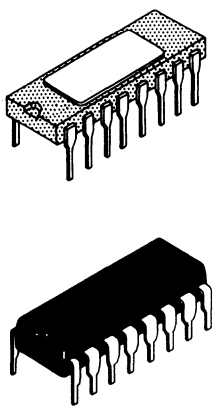
Multiplexed row and column address inputs permit the MSM41256 to be housed in a standard 16-pin DIP, Pin-outs conform to the JEDEC approved pin out.

The MSM41256 is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

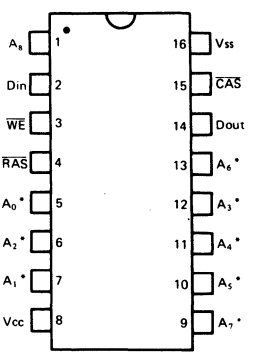
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

- 262144 x 1 RAM, 16-pin package.
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  - 120 ns max. **(MSM41256-12AS/RS)**
  - 150 ns max. **(MSM41256-15AS/RS)**
  - 200 ns max. **(MSM41256-20AS/RS)**
- Cycle time,
  - 230 ns min. **(MSM41256-12AS/RS)**
  - 260 ns min. **(MSM41256-15AS/RS)**
  - 330 ns min. **(MSM41256-20AS/RS)**
- Low power:
  - 385 mW active **(MSM41256-12AS/RS)**
  - 360 mW active **(MSM41256-15AS/RS)**
  - 305 mW active **(MSM41256-20AS/RS)**
  - 28 mW max. standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 4 ms/256 refresh cycles
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle and allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance



PIN CONFIGURATION

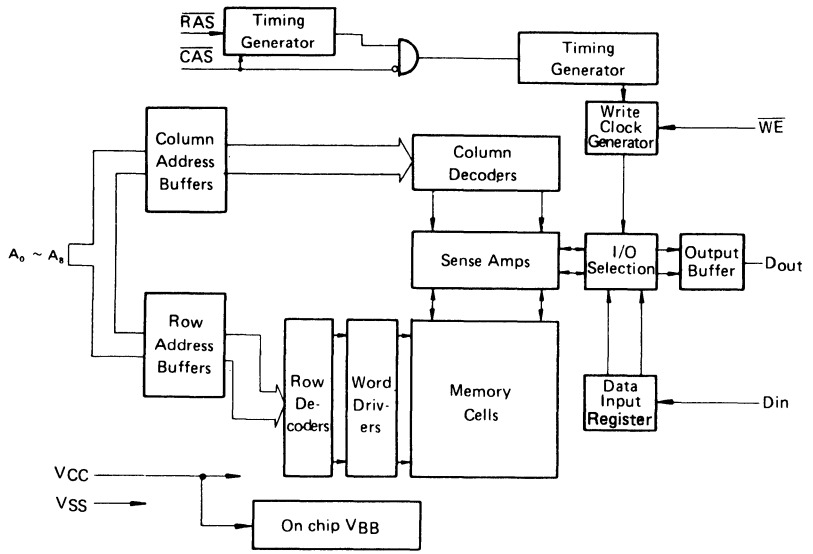


Pin Names	Function
$A_0 \sim A_8$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
Din	Data Input
Dout	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground (0V)

* Refresh Address

9

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Respect to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min.	Max.	Unit
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	MSM41256-12	I_{CC1}		70	mA
	MSM41256-15			65	
	MSM41256-20			60	
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		5.0	mA
REFRESH CURRENT Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	MSM41256-12	I_{CC3}		60	mA
	MSM41256-15			55	
	MSM41256-20			50	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	MSM41256-12	I_{CC4}		60	mA
	MSM41256-15			55	
	MSM41256-20			50	
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)		I_{LI}	-10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, (0V ≤ V_{OUT} ≤ 5.5V)		I_{LO}	-10	10	μA
OUTPUT LEVELS Output high voltage (I_{OH} = -5 mA)		V_{OH}	2.4		V
Output low voltage (I_{OL} = 4.2 mA)		V_{OL}		0.4	V

Note*: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance (A_0 ~ A_8, D_{IN})	C_{IN1}	6	pF
Input Capacitance (RAS, CAS, WE)	C_{IN2}	7	pF
Output Capacitance (D_{OUT})	C_{OUT}	7	pF

Note: Capacitance measured with Boonton Meter.

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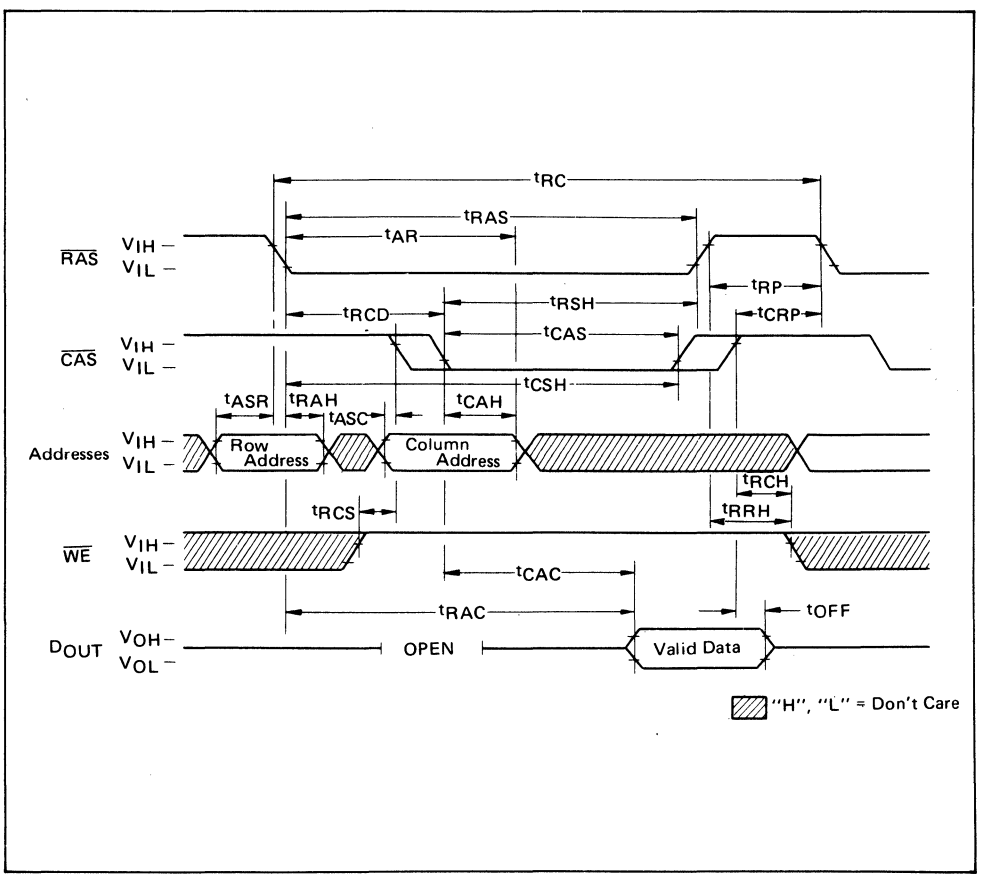
AC CHARACTERISTICS

Notes 1, 2, 3 Under Recommended Operating conditions

Parameter	Symbol	Units	MSM41256-12		MSM41256-15		MSM41256-20		Note
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4		4	
Random read or write cycle time	t_{RC}	ns	230		260		330		
Read-write cycle time	t_{RWC}	ns	255		325		410		
Page mode cycle time	t_{PC}	ns	130		145		190		
Access time from $\overline{RAS}$	t_{RAC}	ns		120		150		200	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		60		75		100	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	40	0	40	0	50	
Transition time	t_T	ns	3	50	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	100		100		120		
$\overline{RAS}$ pulse width	t_{RAS}	ns	120	10,000	150	10,000	200	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	60		75		100		
$\overline{CAS}$ precharge time	t_{CP}	ns	60		60		80		
$\overline{CAS}$ pulse width	t_{CAS}	ns	60	10,000	75	10,000	100	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	120		150		200		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	60	25	75	30	100	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		0		
Row Address set-up time	t_{ASR}	ns	0		0		0		
Row Address hold time	t_{RAH}	ns	20		20		25		
Column Address set-up time	t_{ASC}	ns	0		0		0		
Column Address hold time	t_{CAH}	ns	35		45		55		
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	ns	95		120		155		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time	t_{RCH}	ns	0		0		0		
Write command set-up time	t_{WCS}	ns	0		0		0		8
Write command hold time	t_{WCH}	ns	40		45		55		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	100		120		155		
Write command pulse width	t_{WP}	ns	40		45		55		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	40		60		80		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	40		60		80		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	40		45		55		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	100		120		155		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	40		75		100		8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	100		150		200		8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	20		20		25		

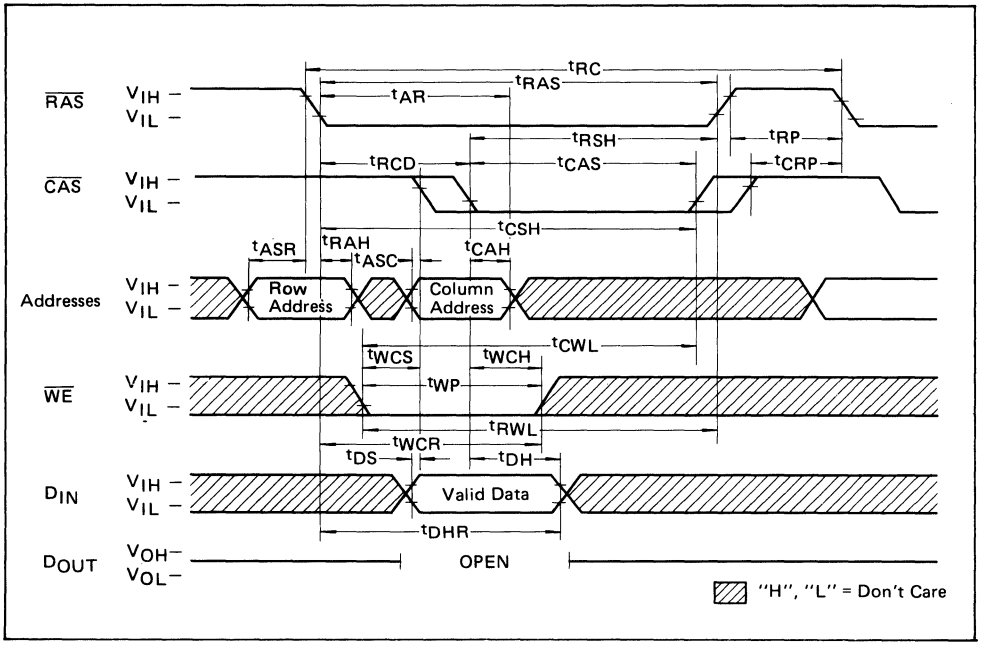
NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Examples; $\overline{RAS}$ only) before proper device operation is achieved.
2) AC measurements assume t_T = 5 ns.
3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4) Assumes that $t_{RCD} < t_{RCD}$ (max.).
If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
5) Assumes that $t_{RCD} < t_{RCD}$ (max.)
6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} > t_{RWD}$ (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

READ CYCLE TIMING

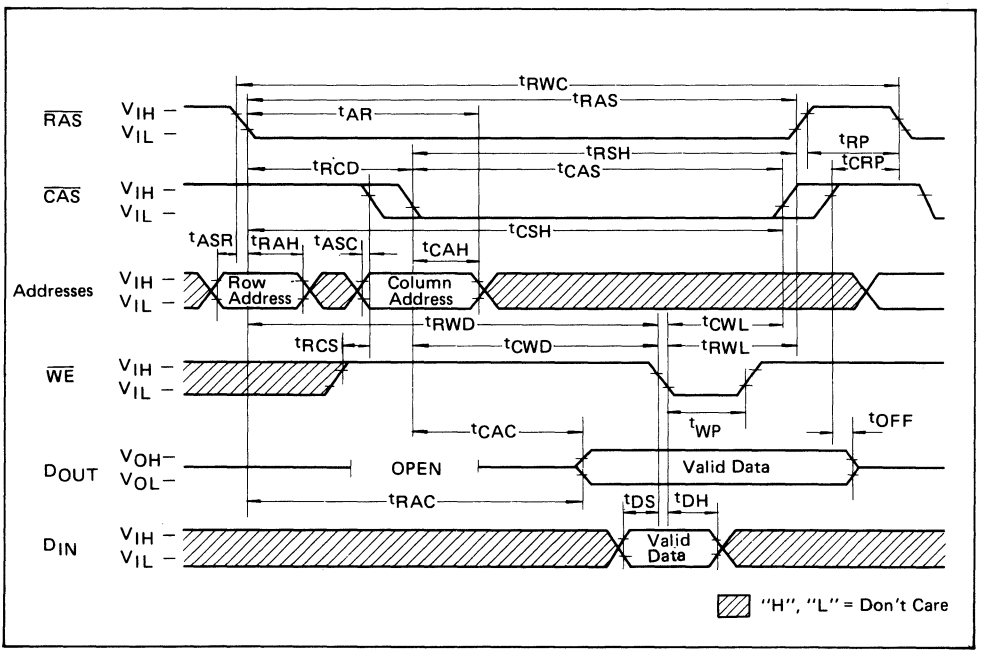


WRITE CYCLE TIMING

(EARLY WRITE)

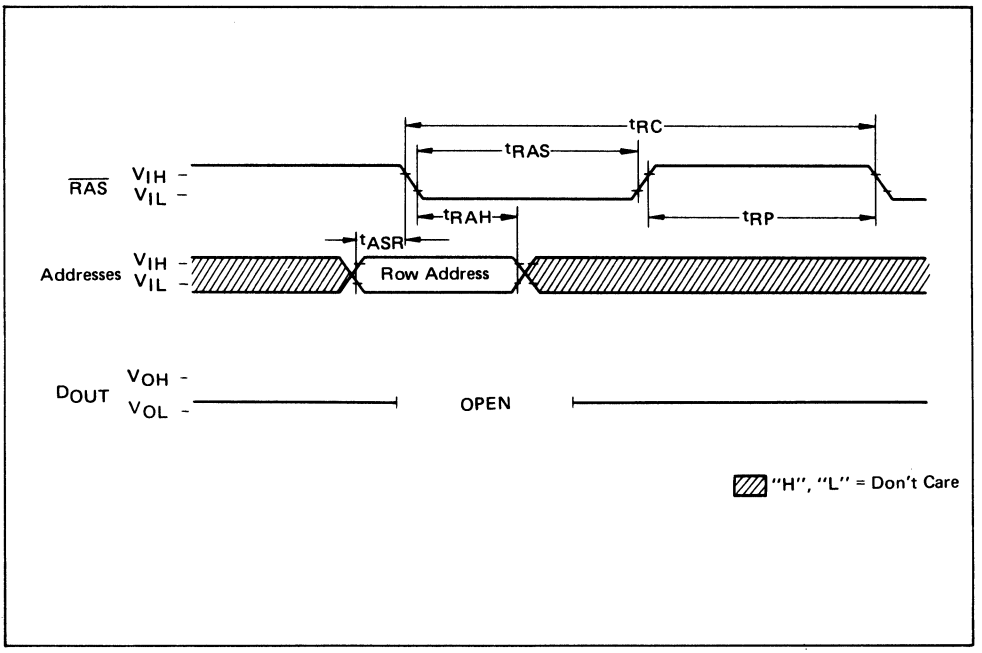


READ-WRITE/READ-MODIFY-WRITE CYCLE

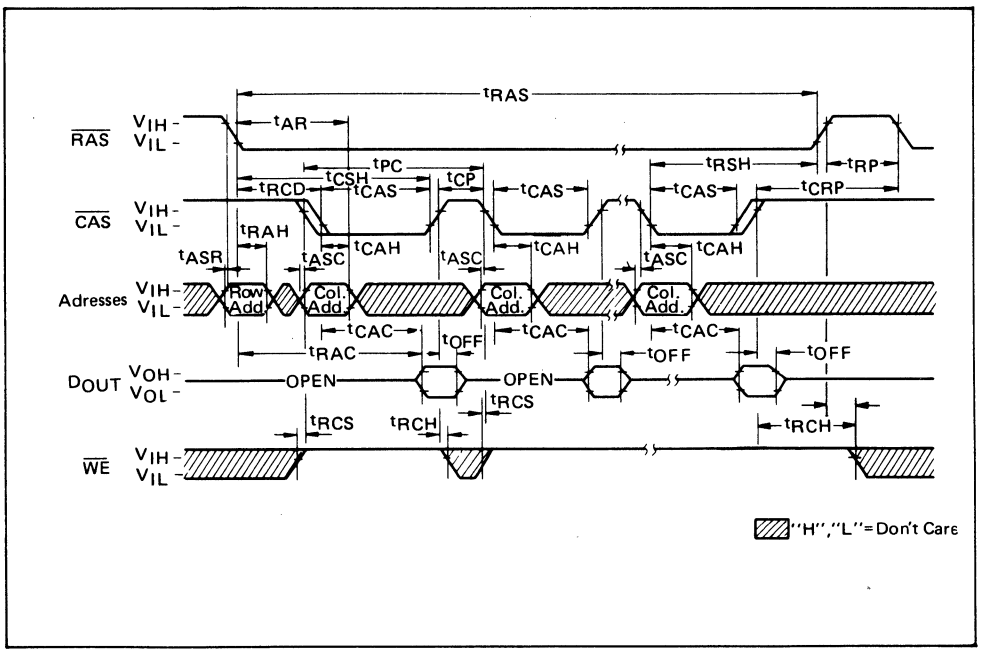


$\overline{RAS}$ ONLY REFRESH TIMING

($\overline{CAS}$: V_{IH}, $\overline{WE}$ & DIN: Don't care)



PAGE MODE READ CYCLE



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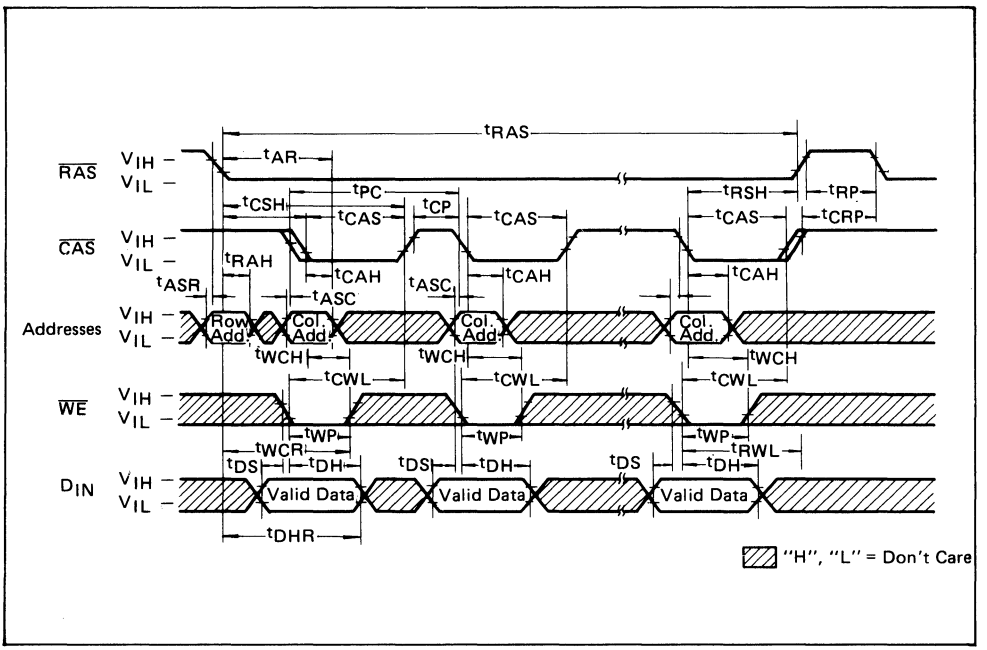
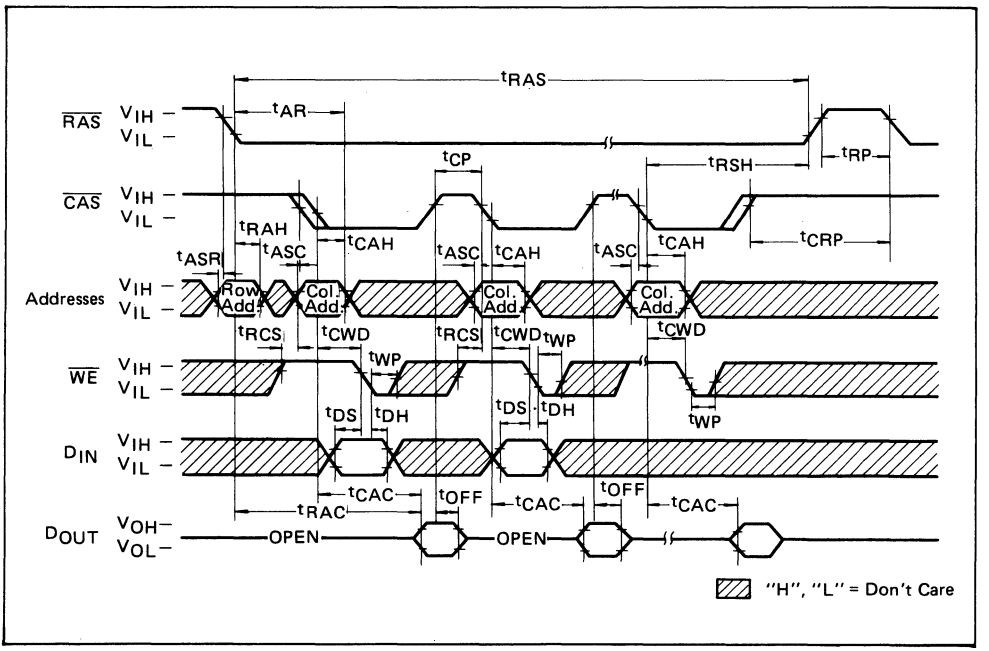
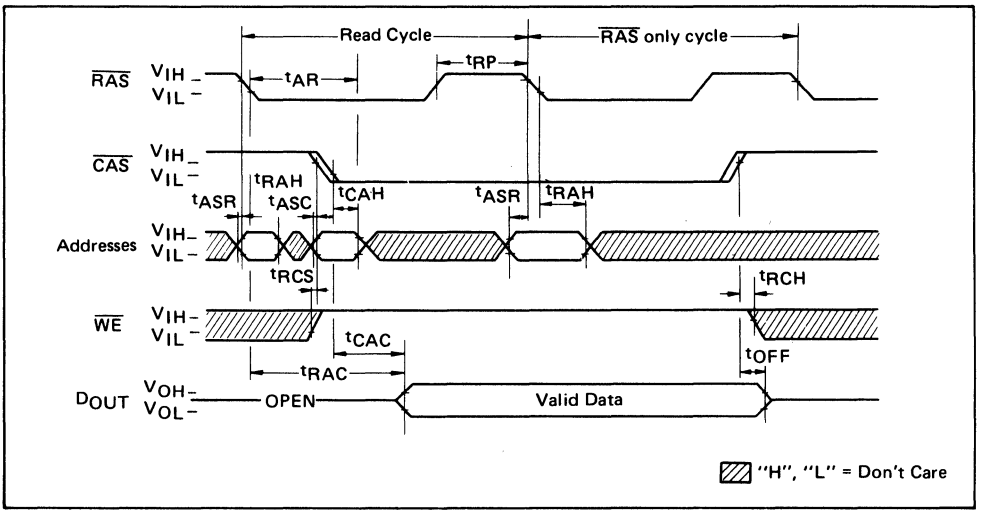
PAGE MODE WRITE CYCLE



PAGE MODE, READ-MODIFY-WRITE CYCLE



HIDDEN REFRESH



DESCRIPTION

Address Inputs:

A total of eighteen binary input address bits is required to decode any 1 of 262144 storage cell locations within the MSM41256 Nine row-address bits are established on the input pins ($A_0 \sim A_8$) and latched with the Row Address Strobe ($\overline{RAS}$). The Nine column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$, $\overline{CAS}$ is internally inhibited (or "gated") by RAS to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM41256 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until CAS has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSM41256 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

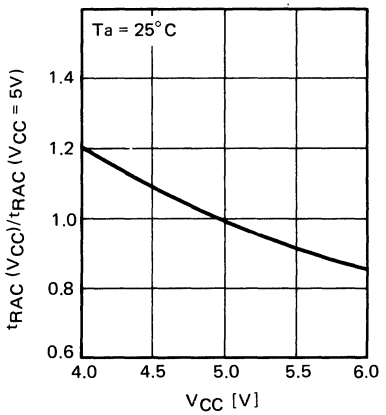
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses ($A_0 \sim A_7$) at least every four milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_8. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Hidden Refresh:

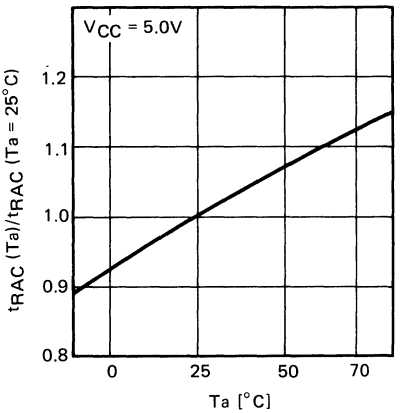
$\overline{RAS}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

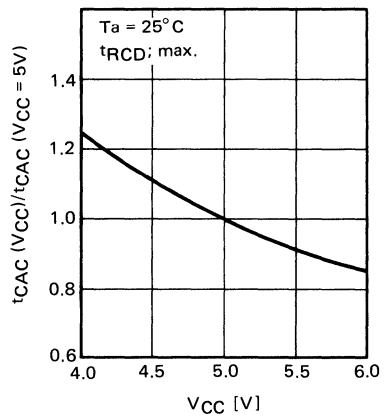
Access time from $\overline{RAS}$ (Relative value) vs. V_{CC}



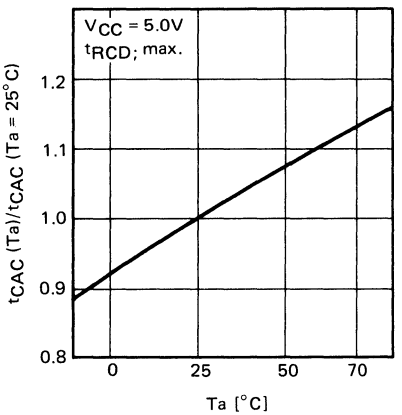
Access time from $\overline{RAS}$ (Relative value) vs. Ta



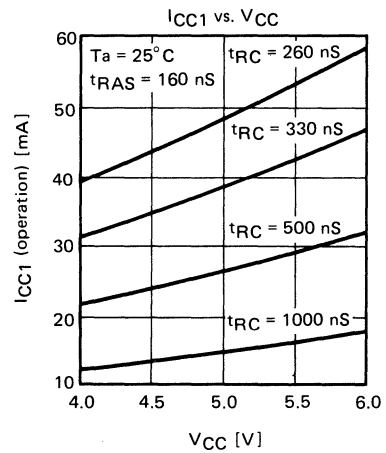
Access time from $\overline{CAS}$ (Relative value) vs. V_{CC}



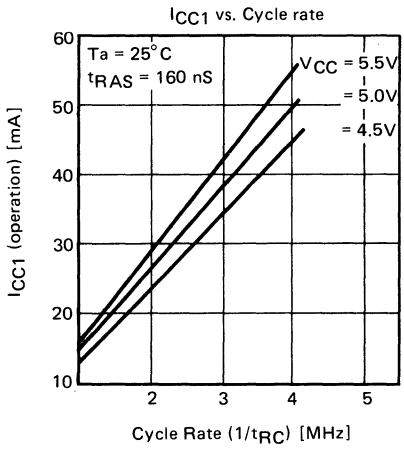
Access time from $\overline{CAS}$ (Relative value) vs. Ta



I_{CC1} vs. V_{CC}



I_{CC1} vs. Cycle rate



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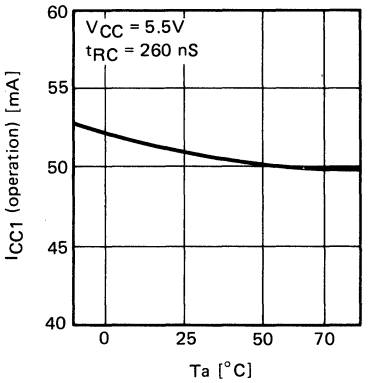
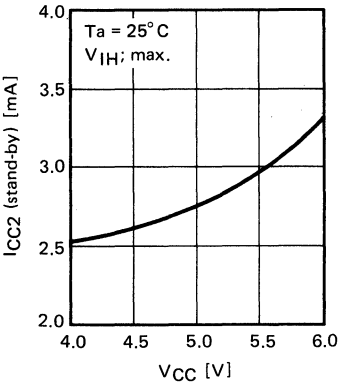
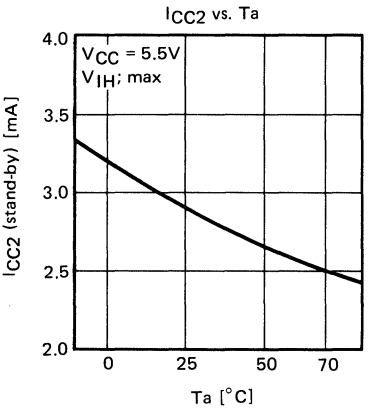
I_{CC1} vs. Ta



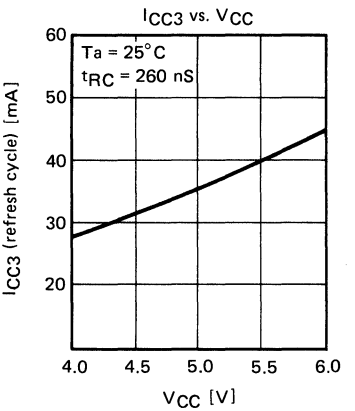
I_{CC2} vs. V_{CC}



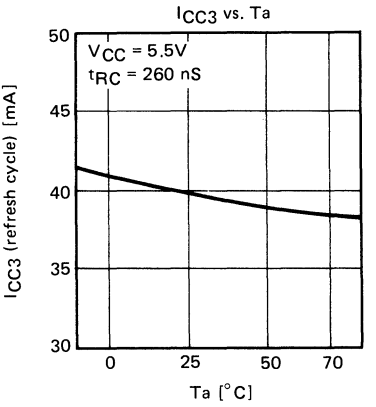
I_{CC2} vs. Ta



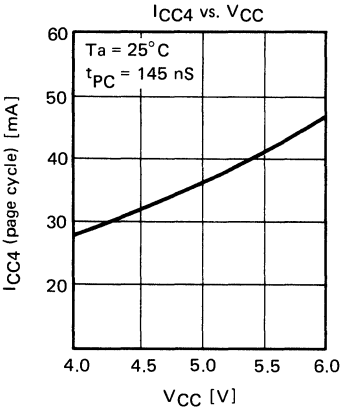
I_{CC3} vs. V_{CC}



I_{CC3} vs. Ta



I_{CC4} vs. V_{CC}



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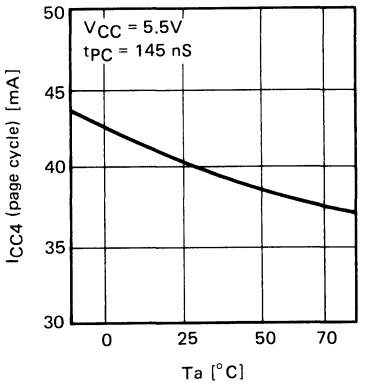
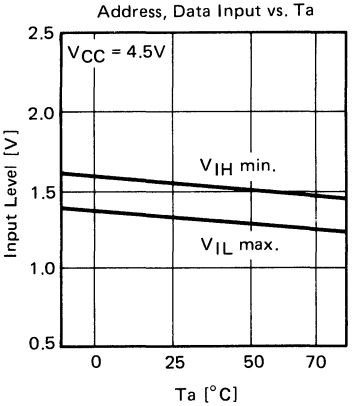
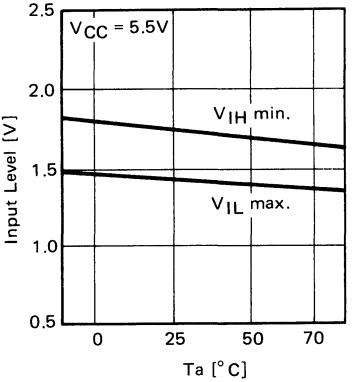
I_{CC4} vs. Ta



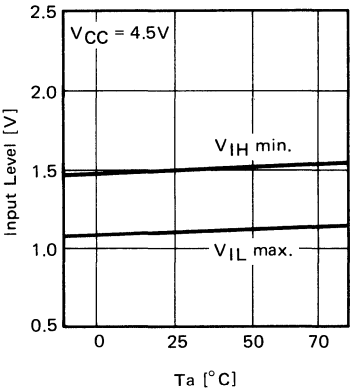
Address, Data Input vs. Ta



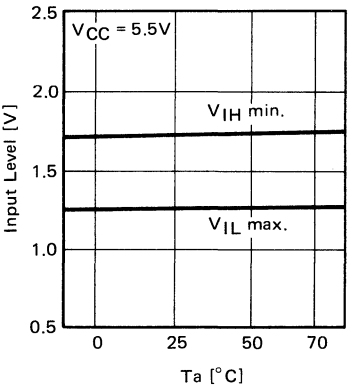
Address, Data Input vs. Ta



Clock Input vs. Ta



Clock Input vs. Ta



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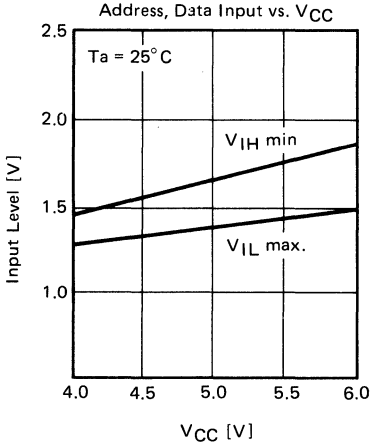
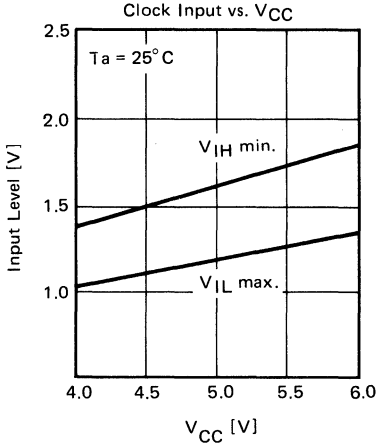
Address, Data Input vs. V_{CC}

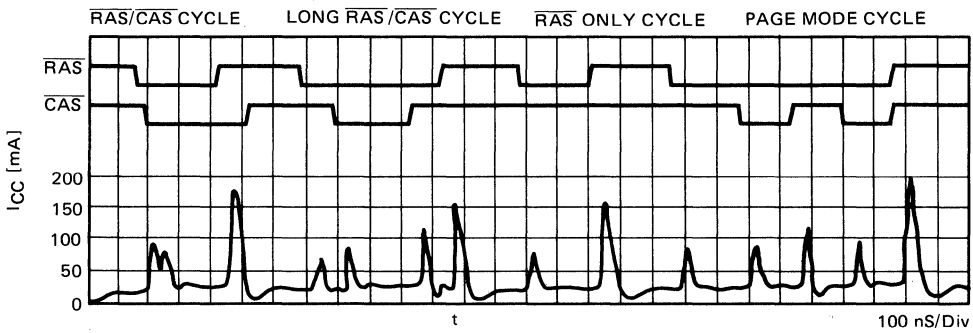


Clock Input vs. V_{CC}



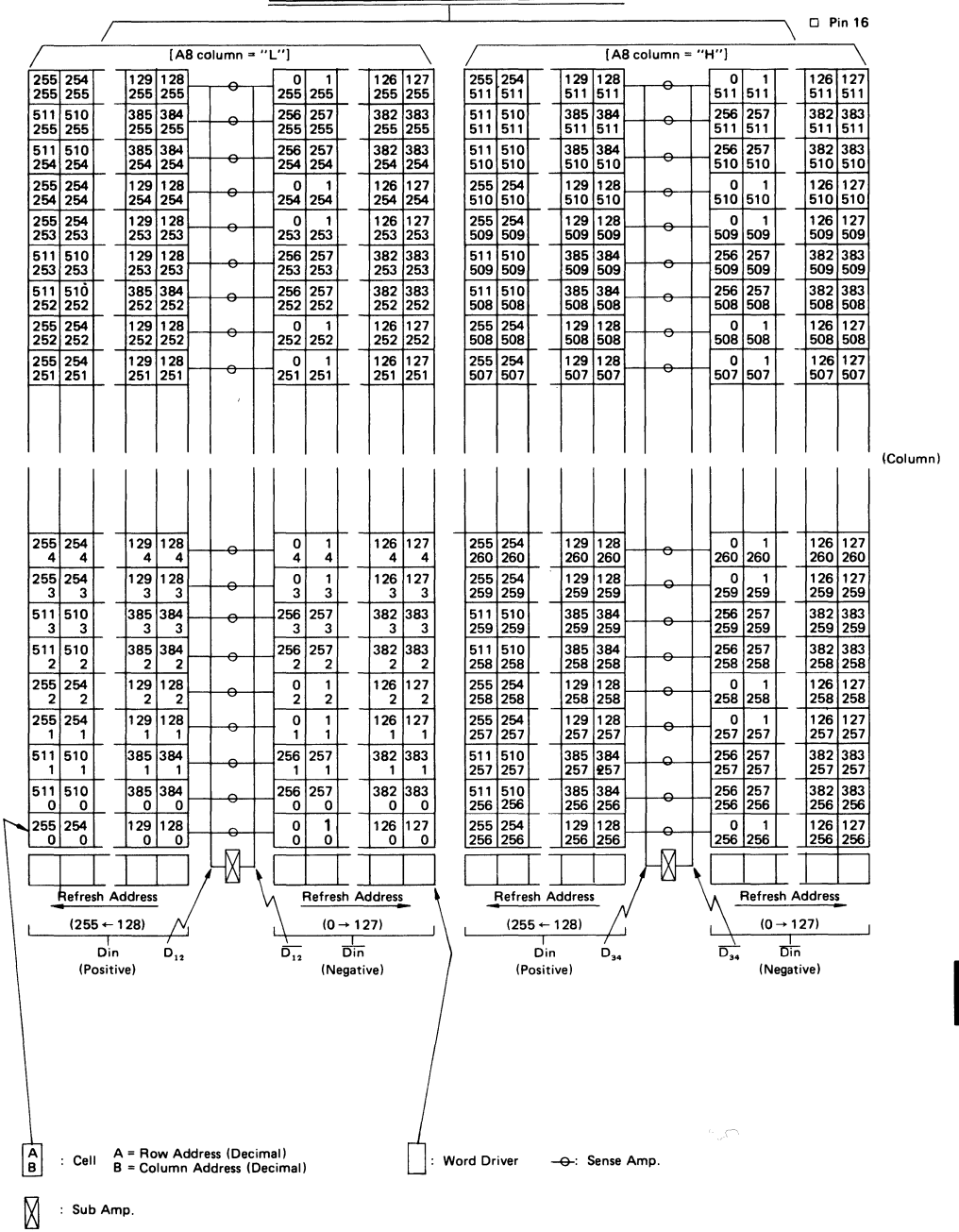
TYPICAL CURRENT WAVEFORMS

V_{CC} = 5.5V
Ta = 25°C



9

MSM41256 Bit Map (Physical-Decimal)



MSM41256JS

262144-BIT DYNAMIC RANDOM ACCESS MEMORY < Page Mode Type >

GENERAL DESCRIPTION

The Oki MSM41256 is a fully decoded, dynamic NMOS random access memory organized as 262144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

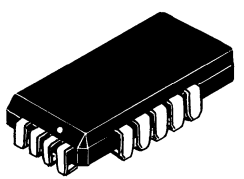
Multiplexed row and column address inputs permit the MSM41256 to be housed in a standard 18-pin PLCC, Pin-outs conform to the JEDEC approved pin out.

The MSM41256 is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

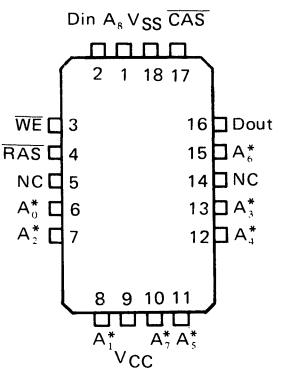
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

- 262144 x 1 RAM, 18-pin PLCC package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  120 ns max. (MSM41256-12JS)
  150 ns max. (MSM41256-15JS)
- Cycle time,
  230 ns min. (MSM41256-12JS)
  260 ns min. (MSM41256-15JS)
- Low power: 385 mW/360 mW active
  28 mW max. standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 4 ms/256 refresh cycles
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle and allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance



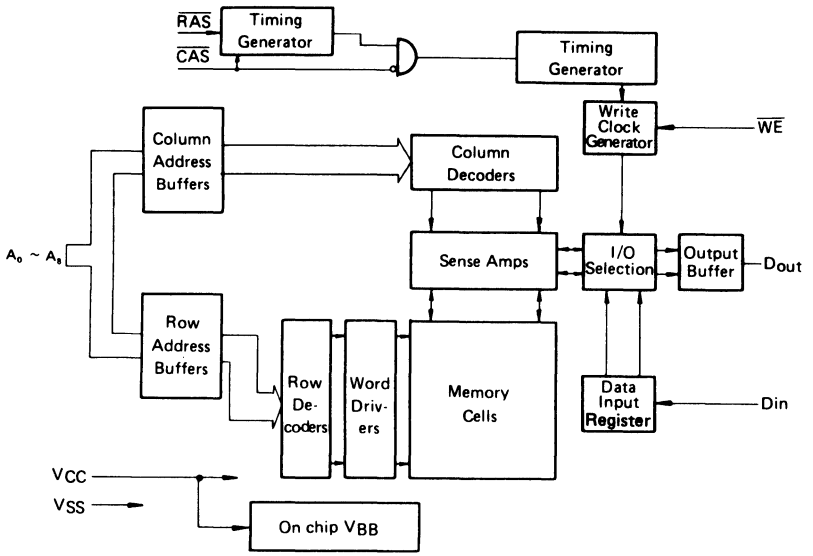
PIN CONFIGURATION



Pin Names	Function
$A_0 \sim A_8$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
Din	Data Input
Dout	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground (0V)
NC	No Connection

* Refresh Address

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Respect to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min.	Max.	Unit
OPERATING CURRENT* Average power supply current (RAS, CAS cycling; t_{RC} = min.)	MSM41256-12	I_{CC1}		70	mA
	MSM41256-15			65	
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		5.0	mA
REFRESH CURRENT Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	MSM41256-12	I_{CC3}		60	mA
	MSM41256-15			55	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	MSM41256-12	I_{CC4}		60	mA
	MSM41256-15			55	
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)		I_{LI}	-10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, (0V ≤ V_{OUT} ≤ 5.5V)		I_{LO}	-10	10	μA
OUTPUT LEVELS Output high voltage (I_{OH} = -5 mA)		V_{OH}	2.4		V
Output low voltage (I_{OL} = 4.2 mA)		V_{OL}		0.4	V

Note*: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance (A_0 ~ A_8, D_{IN})	C_{IN1}	6	pF
Input Capacitance (RAS, CAS, WE)	C_{IN2}	7	pF
Output Capacitance (D_{OUT})	C_{OUT}	7	pF

Note: Capacitance measured with Boonton Meter.

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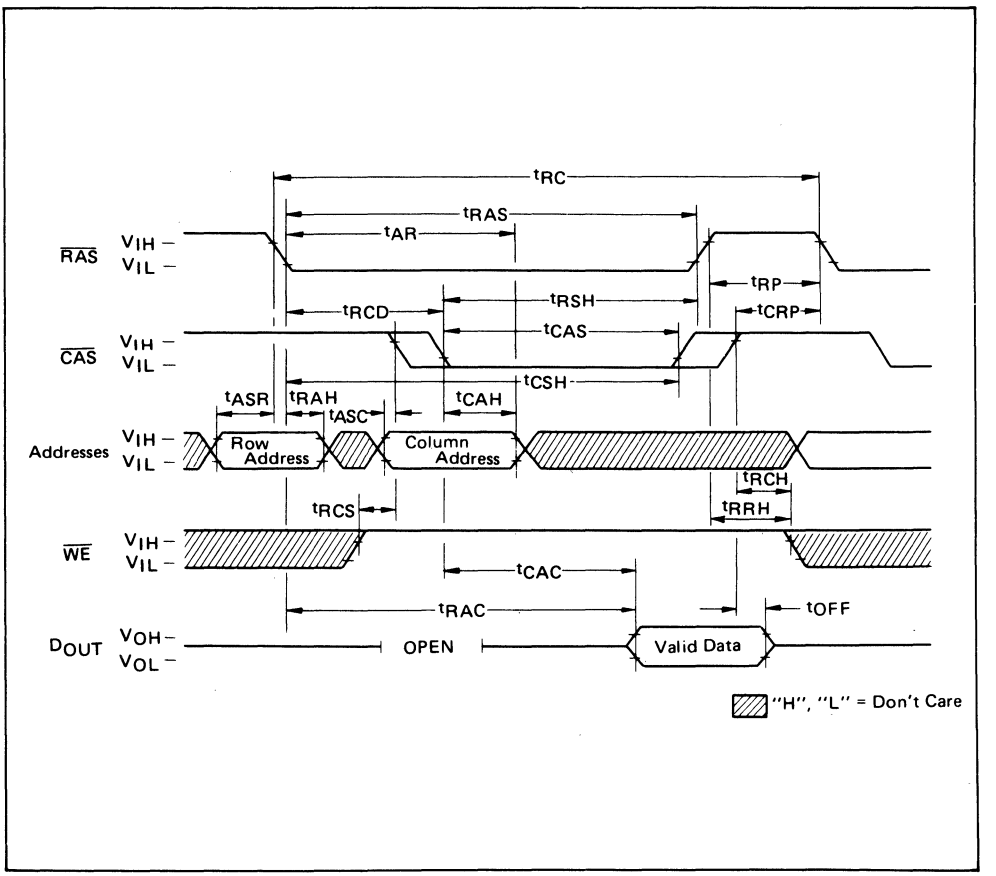
AC CHARACTERISTICS

Notes 1, 2, 3 Under Recommended Operating conditions

Parameter	Symbol	Units	MSM41256-12		MSM41256-15		Note
			Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4	
Random read or write cycle time	t_{RC}	ns	230		260		
Read-write cycle time	t_{RWC}	ns	255		325		
Page mode cycle time	t_{PC}	ns	130		145		
Access time from $\overline{RAS}$	t_{RAC}	ns		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	40	0	40	
Transition time	t_T	ns	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	100		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	120	10,000	150	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	60		75		
$\overline{CAS}$ precharge time	t_{CP}	ns	60		60		
$\overline{CAS}$ pulse width	t_{CAS}	ns	60	10,000	75	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	60	25	75	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		
Row Address set-up time	t_{ASR}	ns	0		0		
Row Address hold time	t_{RAH}	ns	20		20		
Column Address set-up time	t_{ASC}	ns	0		0		
Column Address hold time	t_{CAH}	ns	35		45		
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	ns	95		120		
Read command set-up time	t_{RCS}	ns	0		0		
Read command hold time	t_{RCH}	ns	0		0		
Write command set-up time	t_{WCS}	ns	0		0		8
Write command hold time	t_{WCH}	ns	40		45		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	100		120		
Write command pulse width	t_{WP}	ns	40		45		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	40		60		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	40		60		
Data-in set-up time	t_{DS}	ns	0		0		
Data-in hold time	t_{DH}	ns	40		45		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	100		120		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	40		75		8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	100		150		8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	20		20		

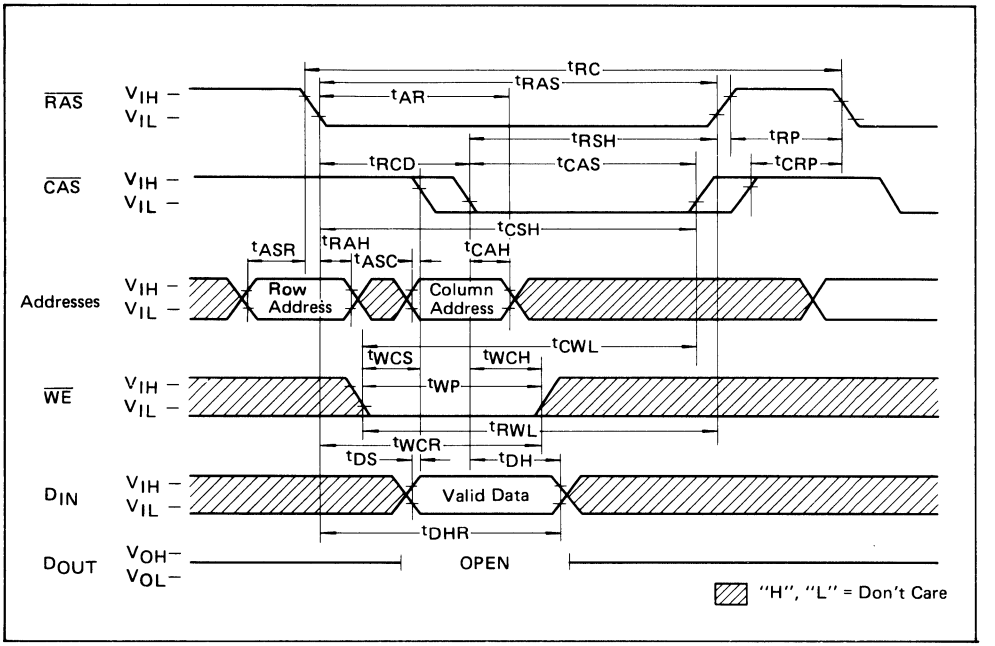
NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Examples; $\overline{RAS}$ only) before proper device operation is achieved.
2) AC measurements assume t_T = 5 ns.
3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4) Assumes that $t_{RCD} < t_{RCD}$ (max.).
If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
5) Assumes that $t_{RCD} < t_{RCD}$ (max.)
6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} > t_{RWD}$ (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

READ CYCLE TIMING

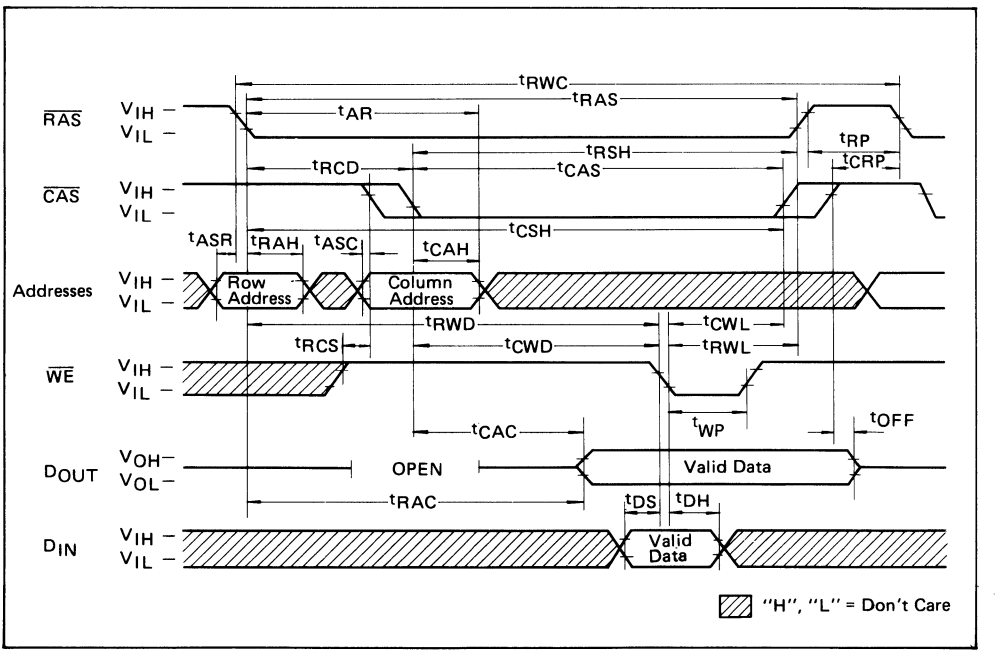


WRITE CYCLE TIMING

(EARLY WRITE)

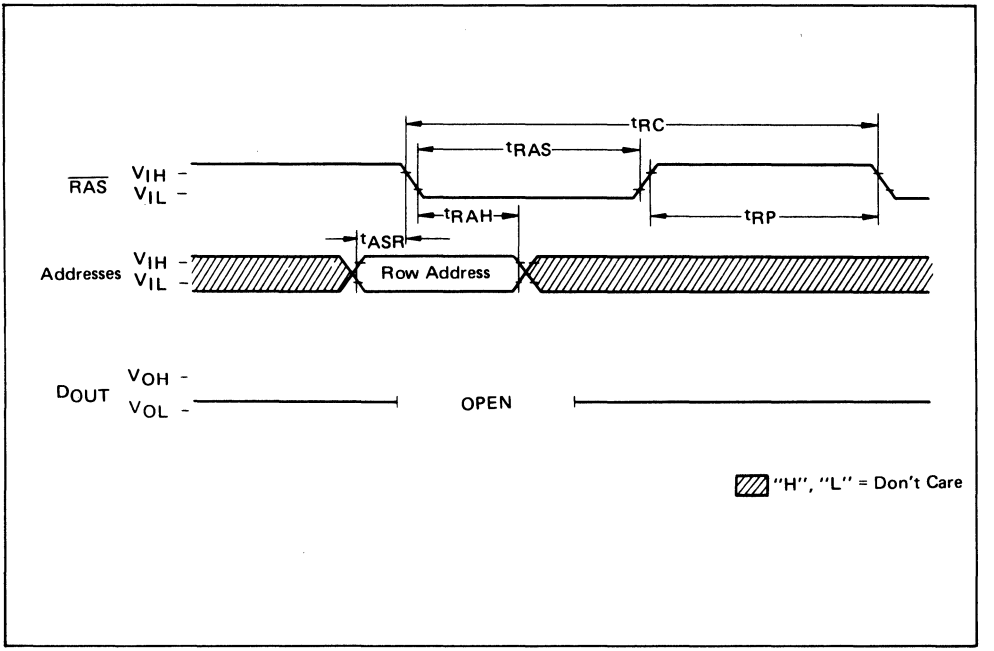


READ-WRITE/READ-MODIFY-WRITE CYCLE

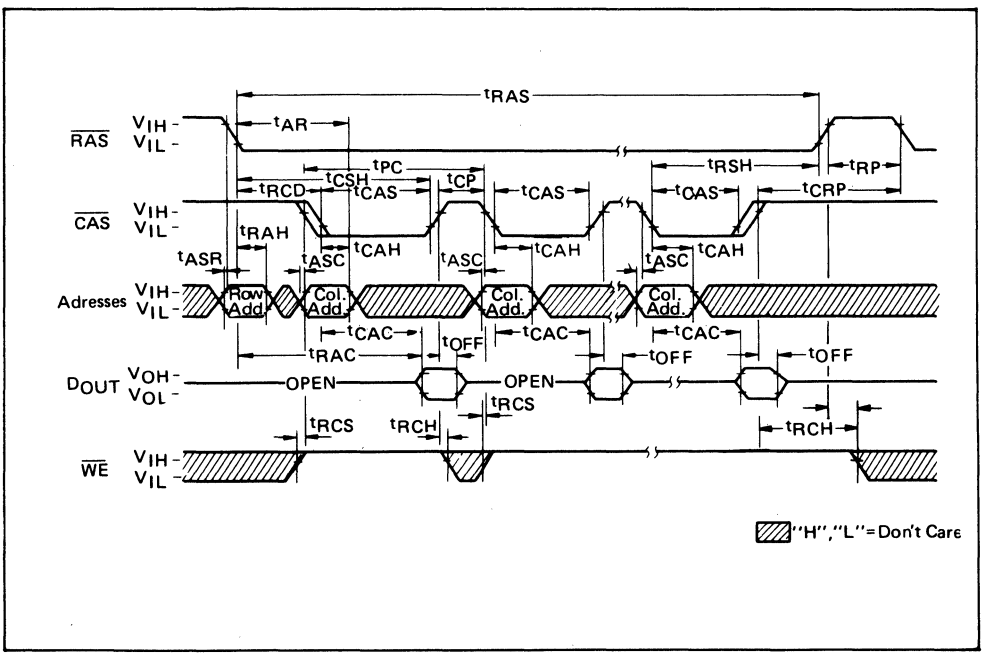


$\overline{RAS}$ ONLY REFRESH TIMING

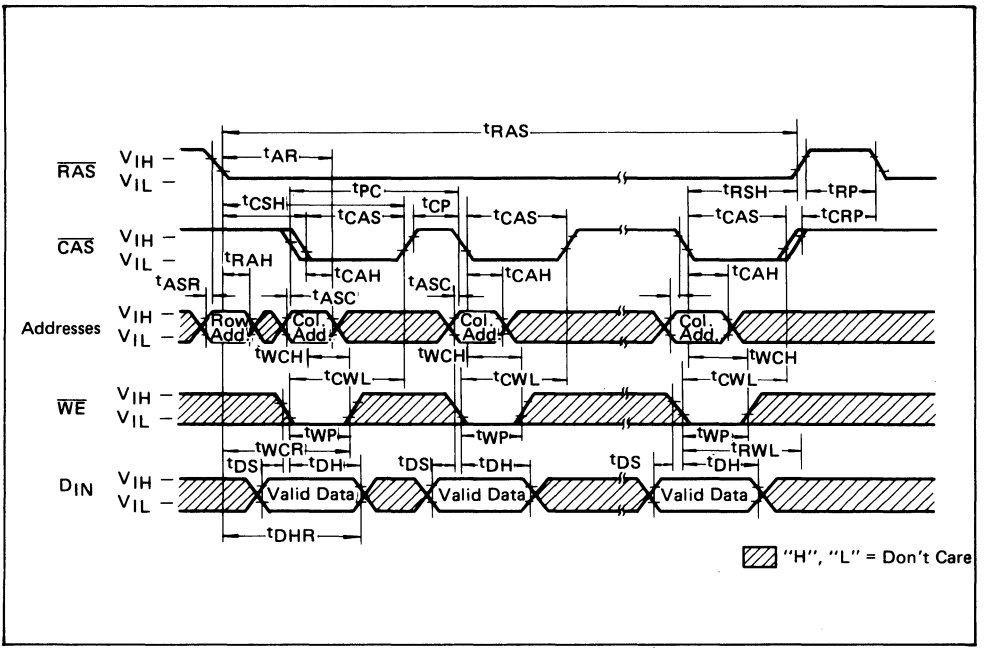
($\overline{CAS}$: V_{IH}, $\overline{WE}$ & D_{IN}: Don't care)



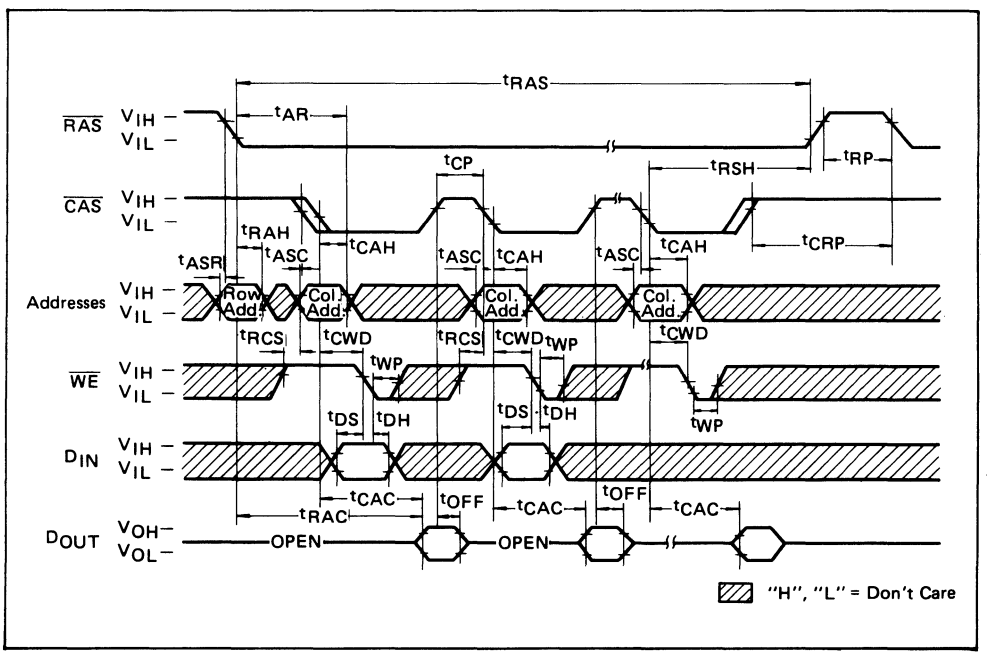
PAGE MODE READ CYCLE



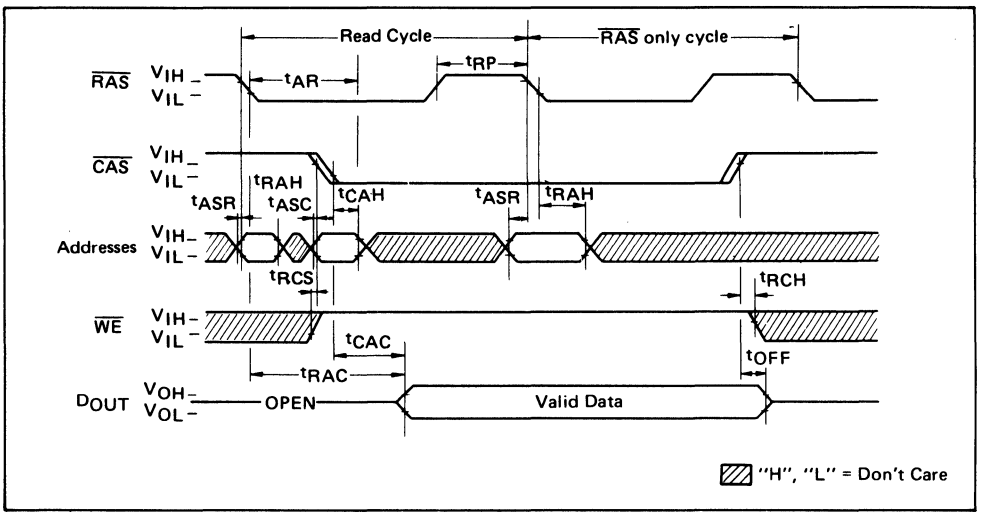
PAGE MODE WRITE CYCLE



PAGE MODE, READ-MODIFY-WRITE CYCLE



HIDDEN REFRESH



DESCRIPTION

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262144 storage cell locations within the MSM41256 Nine row-address bits are established on the input pins ($A_0 \sim A_8$) and latched with the Row Address Strobe ($\overline{RAS}$). The Nine column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$, $\overline{CAS}$ is internally inhibited (or "gated") by RAS to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM41256 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSM41256 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

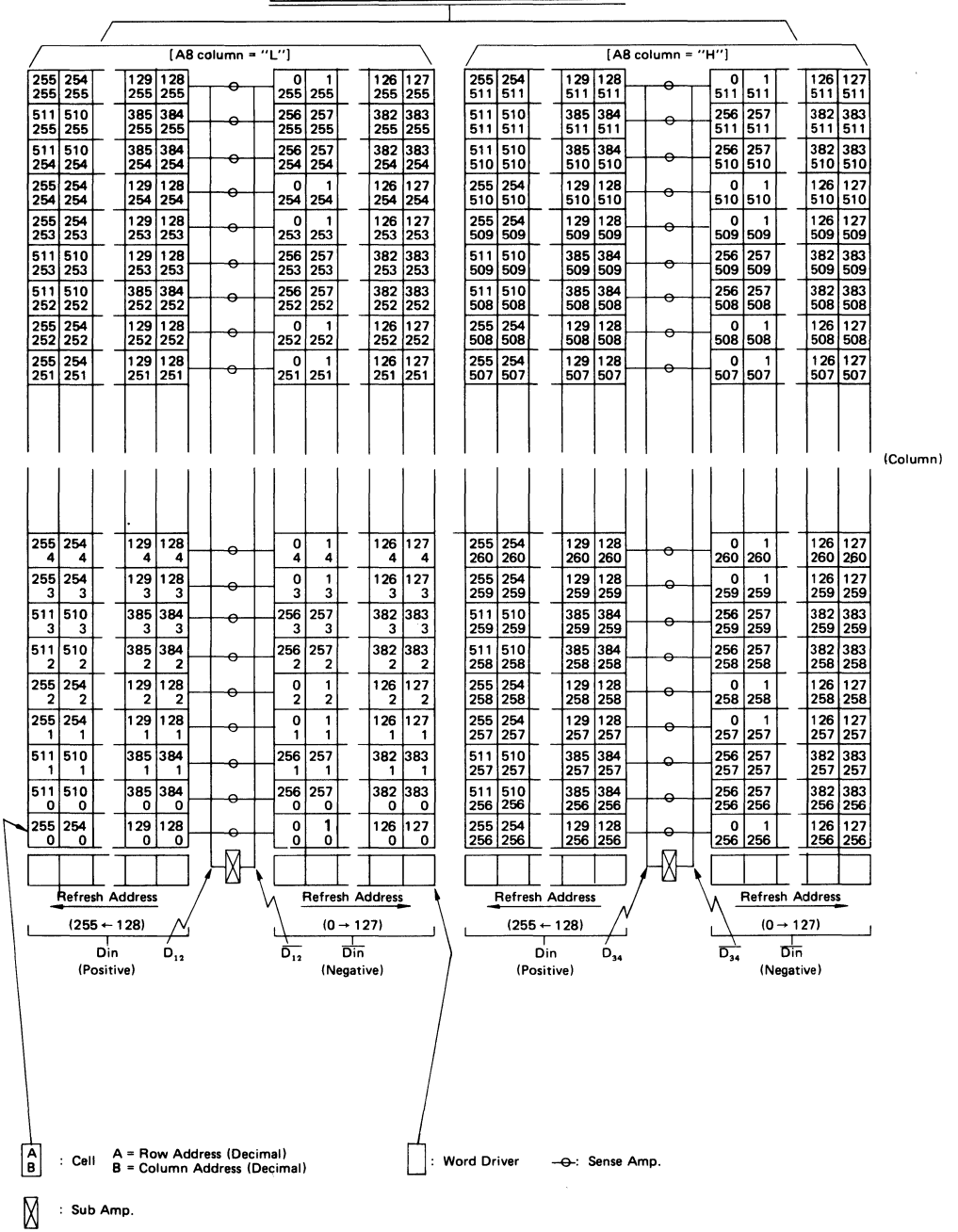
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses ($A_0 \sim A_7$) at least every four milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_8. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Hidden Refresh:

$\overline{RAS}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

MSM41256 Bit Map (Physical-Decimal)



MSM41256AAS/RS

262,144-BIT DYNAMIC RANDOM ACCESS MEMORY <Page Mode Type>

GENERAL DESCRIPTION

The Oki MSM41256A is a fully decoded, dynamic NMOS random access memory organized as 262144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MSM41256A to be housed in a standard 16 pin DIP. Pin-outs conform to the JEDEC approved pin out. Additionally, the MSM41256A offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability.

The MSM41256A is fabricated using silicon gate NMOS and Oki's advanced VLSI Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

- 262,144 × 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time:
  - 100 ns max (MSM41256A-10AS/RS)
  - 120 ns max (MSM41256A-12AS/RS)
  - 150 ns max (MSM41256A-15AS/RS)
- Cycle time:
  - 200 ns min (MSM41256A-10AS/RS)
  - 220 ns min (MSM41256A-12AS/RS)
  - 260 ns min (MSM41256A-15AS/RS)
- Low power:
  - 385 mW active, 28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 256 refresh cycles/4 ms
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- "Page Mode" capability

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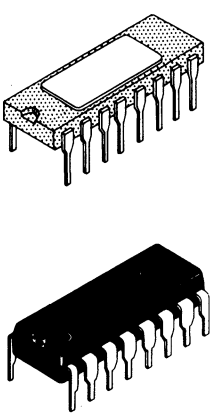
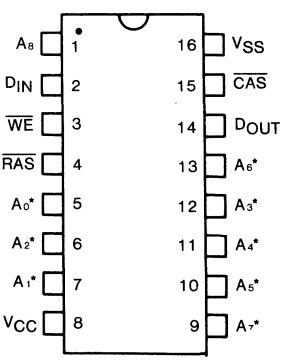


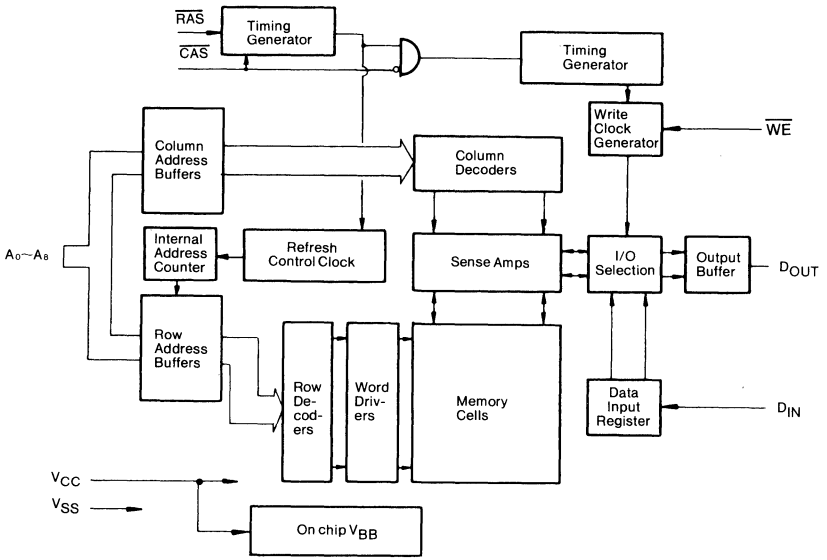
PIN CONFIGURATION (TOP VIEW)



Pin Names	Function
$A_0 \sim A_8$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

* Refresh Address

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	Topr	0 to 70	°C
Storage temperature	Tstg	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Parmanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		70	mA	
STANDBY CURRENT Power supply current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC2}		5.0	mA	
REFRESH CURRENT 1* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$; t_{RC} = min.)	I_{CC3}		60	mA	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}		40	mA	
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = min.)	I_{CC5}		65	mA	
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−10	10	μA	
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	μA	
OUTPUT LEVELS Output high voltage (I_{OH} = −5 mA) Output low voltage (I_{OL} = 4.2 mA)	V_{OH} V_{OL}	2.4	0.4	V V	

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE
(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input capacitance ($A_0 \sim A_8$, D_{IN})	C_{IN1}	–	7	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	–	10	pF
Output capacitance (D_{OUT})	C_{OUT}	–	7	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

Parameter	Symbol	Unit	MSM41256A-10		MSM41256A-12		MSM41256A-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4		4	
Random read or write cycle time	t_{RC}	ns	200		220		260		
Read-write cycle time	t_{RWC}	ns	200		220		260		
Access time from $\overline{RAS}$	t_{RAC}	ns		100		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		50		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	30	0	30	0	30	
Transition time	t_T	ns	3	50	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	85		90		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	105	10μs	120	10μs	150	10μs	
$\overline{RAS}$ hold time	t_{RSH}	ns	55		60		75		
$\overline{CAS}$ pulse width	t_{CAS}	ns	55	10μs	60	10μs	75	10μs	
$\overline{CAS}$ hold time	t_{CSH}	ns	105		120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	50	25	60	25	75	7
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	ns	20		20		20		
Row address set-up time	t_{ASR}	ns	0		0		0		
Row address hold time	t_{RAH}	ns	15		15		15		
Column address set-up time	t_{ASC}	ns	0		0		0		
Column address hold time	t_{CAH}	ns	20		20		25		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	ns	0		0		0		
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	20		20		20		
Write command set-up time	t_{WCS}	ns	0		0		0		8

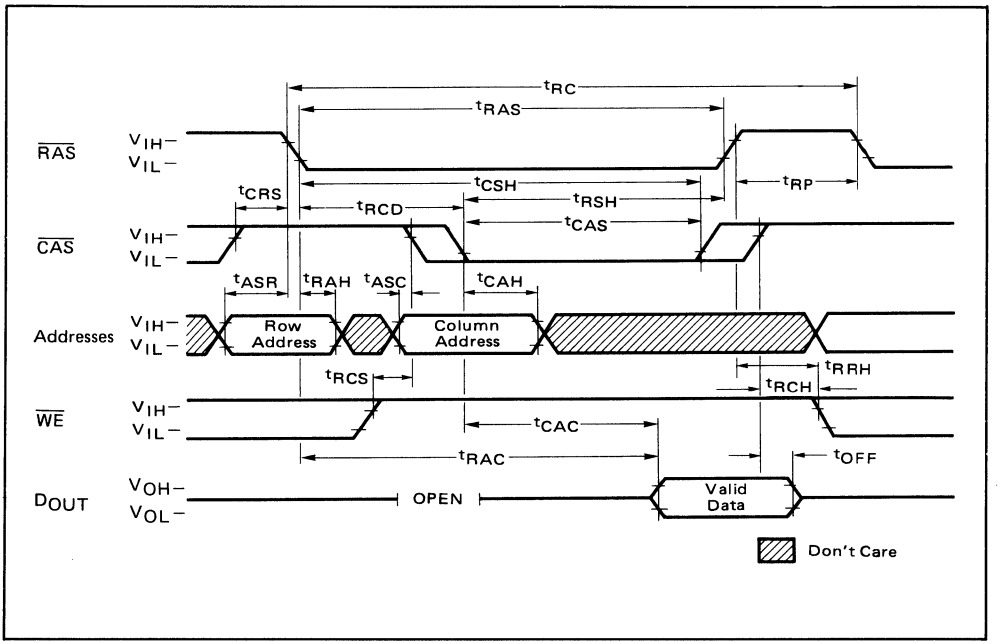
AC CHARACTERISTICS (Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Unit	MSM41256A-10		MSM41256A-12		MSM41256A-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Write command pulse width	t_{WP}	ns	15		20		25		
Write command hold time	t_{WCH}	ns	15		20		25		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	35		40		45		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	35		40		45		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	20		20		25		
$\overline{CAS}$ to WE delay time	t_{CWD}	ns	15		20		25		8
Refresh set-up time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCS}	ns	20		25		30		
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCH}	ns	20		25		30		
$\overline{CAS}$ precharge time (C before R cycle)	t_{CPR}	ns	20		25		30		
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	ns	20		20		20		
Page mode cycle time	t_{PC}	ns	100		120		150		9
Page mode read write cycle time	t_{PRWC}	ns	100		120		150		9
Page mode $\overline{CAS}$ precharge time	t_{CP}	ns	40		50		65		9
Refresh counter test cycle time	t_{RTC}	ns	340		375		430		10
Refresh counter test $\overline{RAS}$ pulse width	t_{TRAS}	ns	230	10μs	265	10μ	320	10μs	10
Refresh counter test $\overline{CAS}$ precharge time	t_{CPT}	ns	50		60		70		10

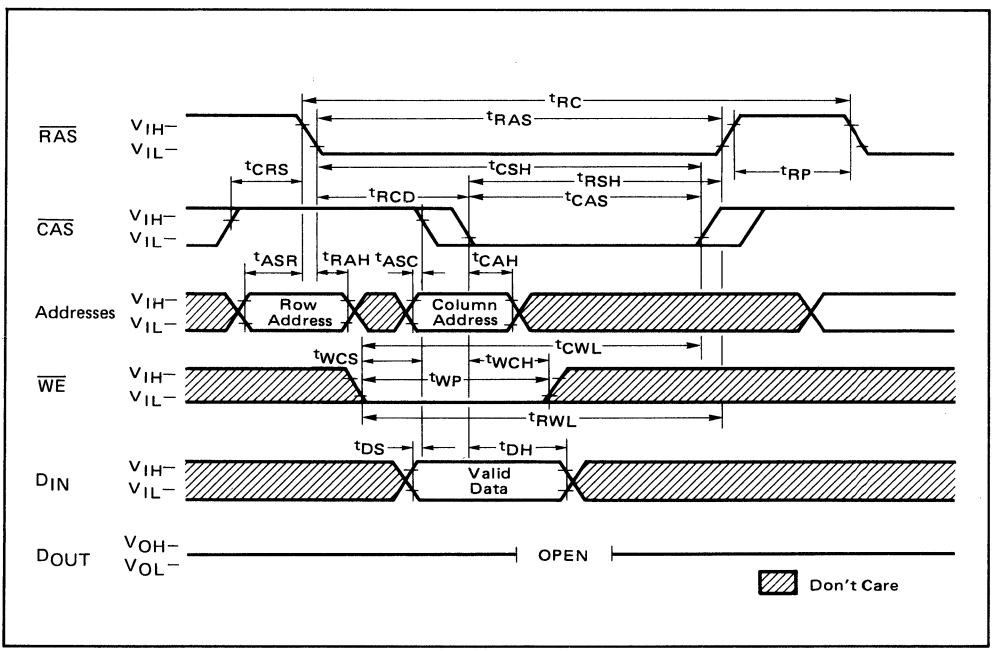
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 RAS cycles (Example: RAS only) before proper device operation is achieved.
2. The AC measurements assume $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical charcteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. Page mode cycle.
10. $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Cycle only.

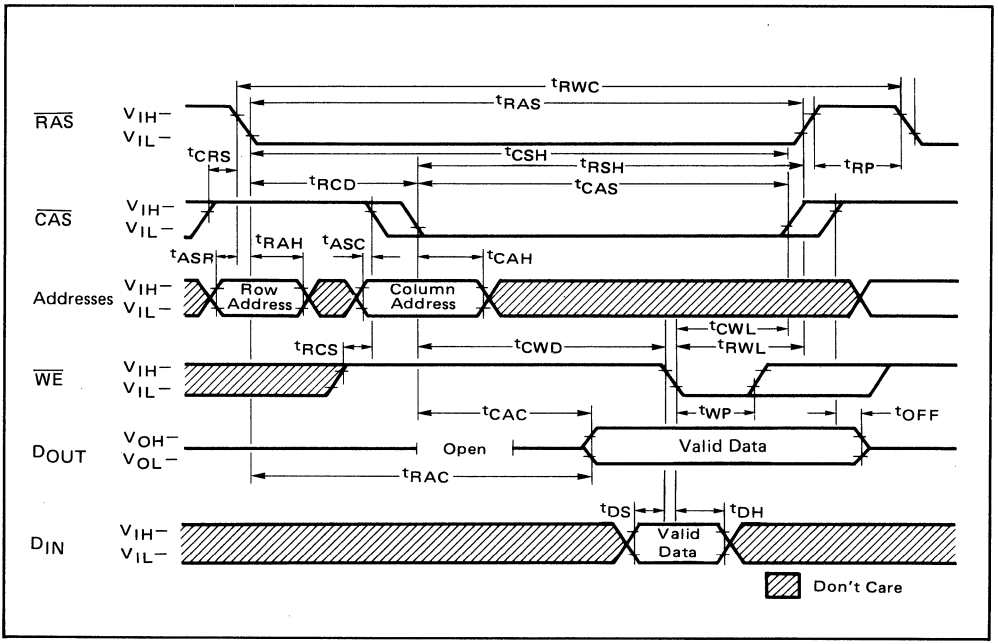
READ CYCLE



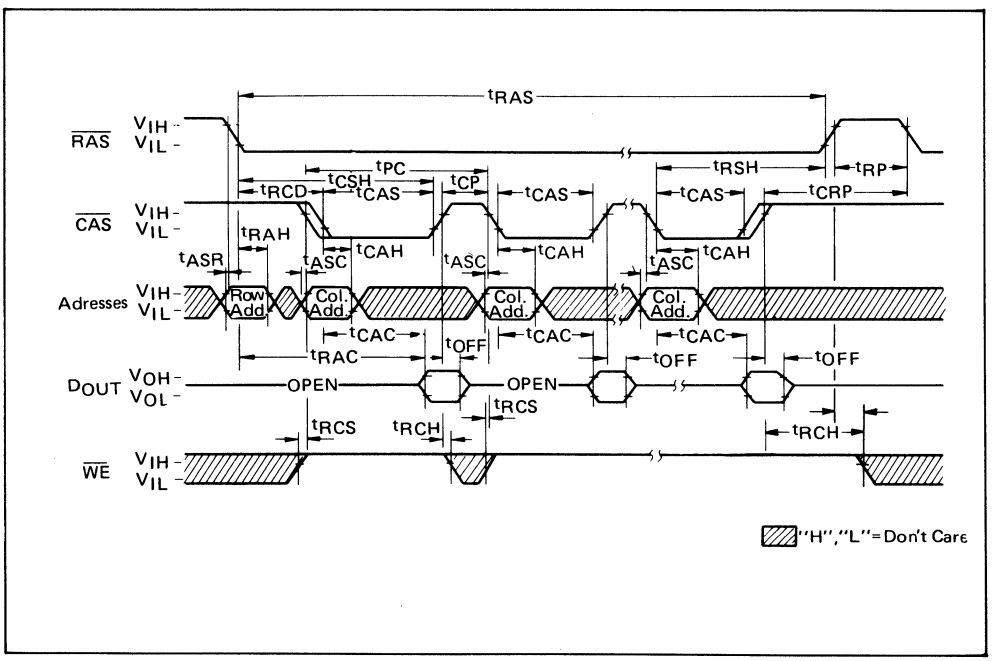
WRITE CYCLE (EARLY WRITE)



READ/WRITE/READ-MODIFY-WRITE CYCLE



PAGE MODE READ CYCLE



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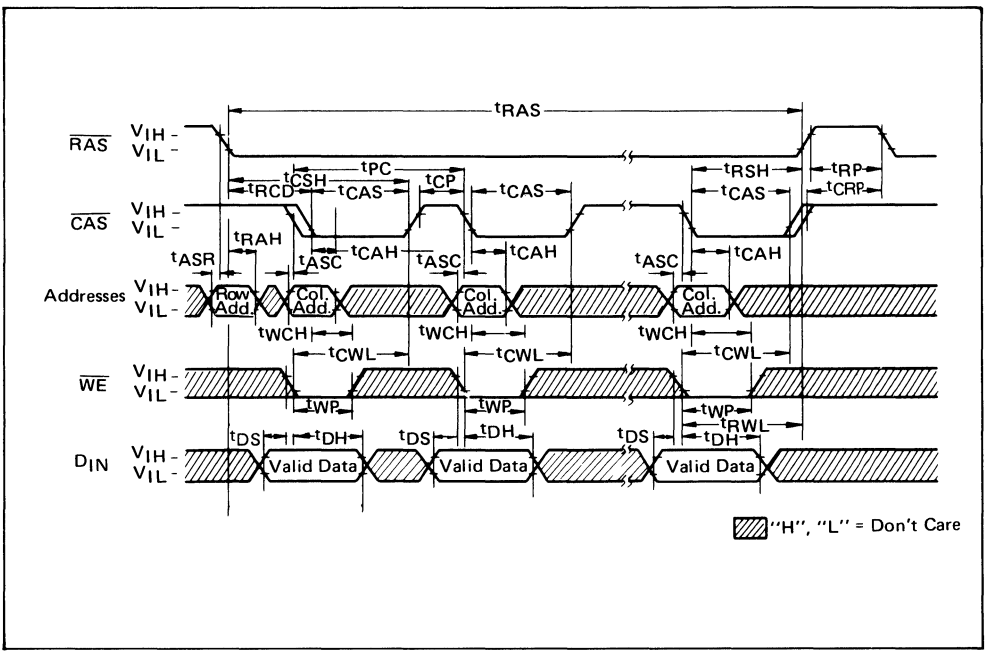
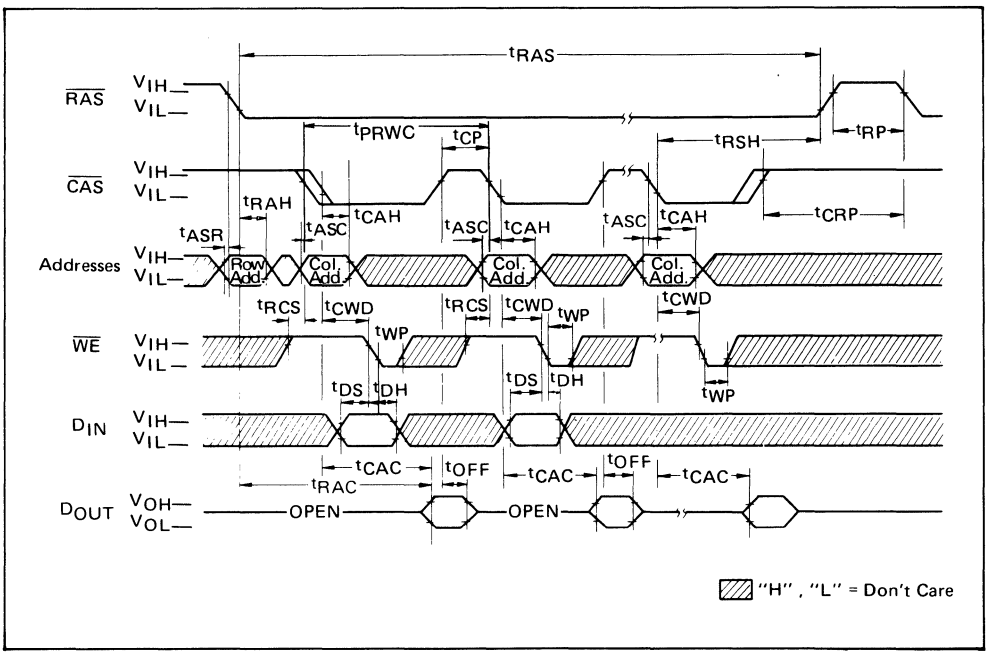
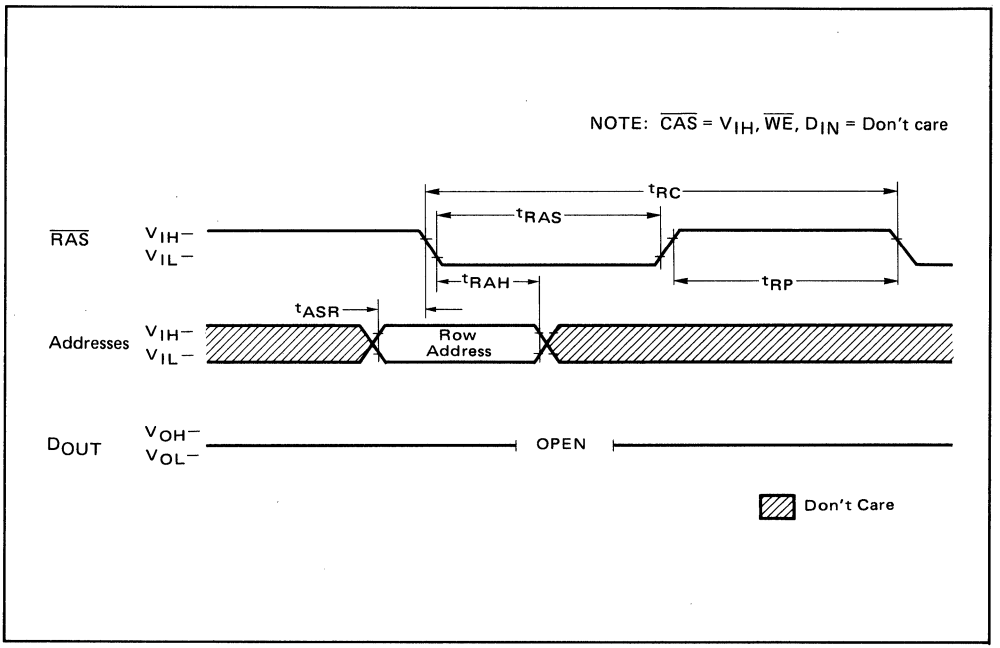
PAGE MODE WRITE CYCLE



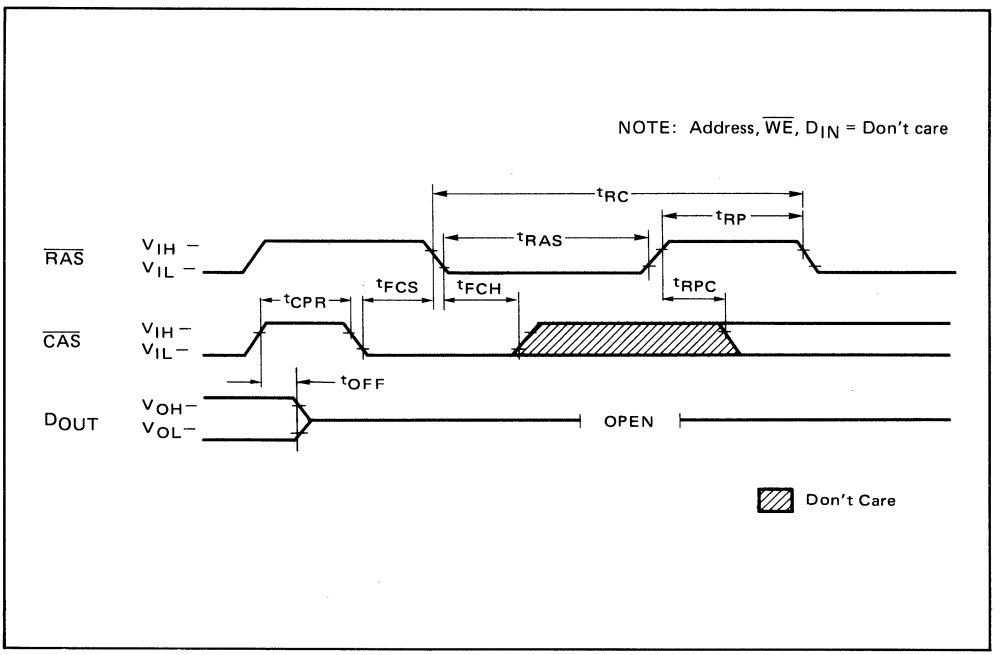
PAGE MODE, READ-MODIFY-WRITE CYCLE



$\overline{RAS}$ ONLY REFRESH CYCLE



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



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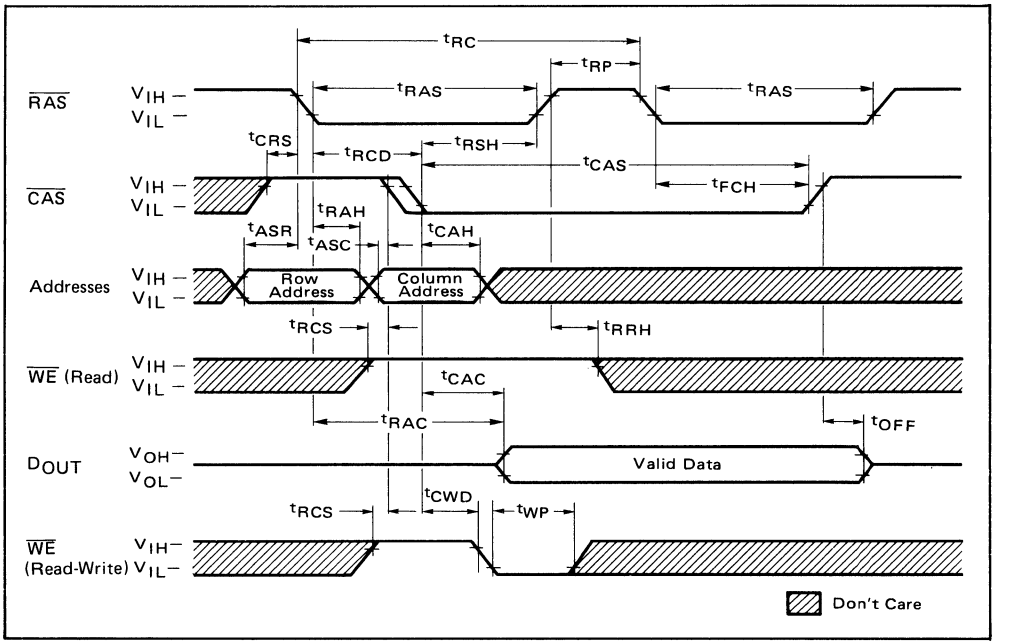
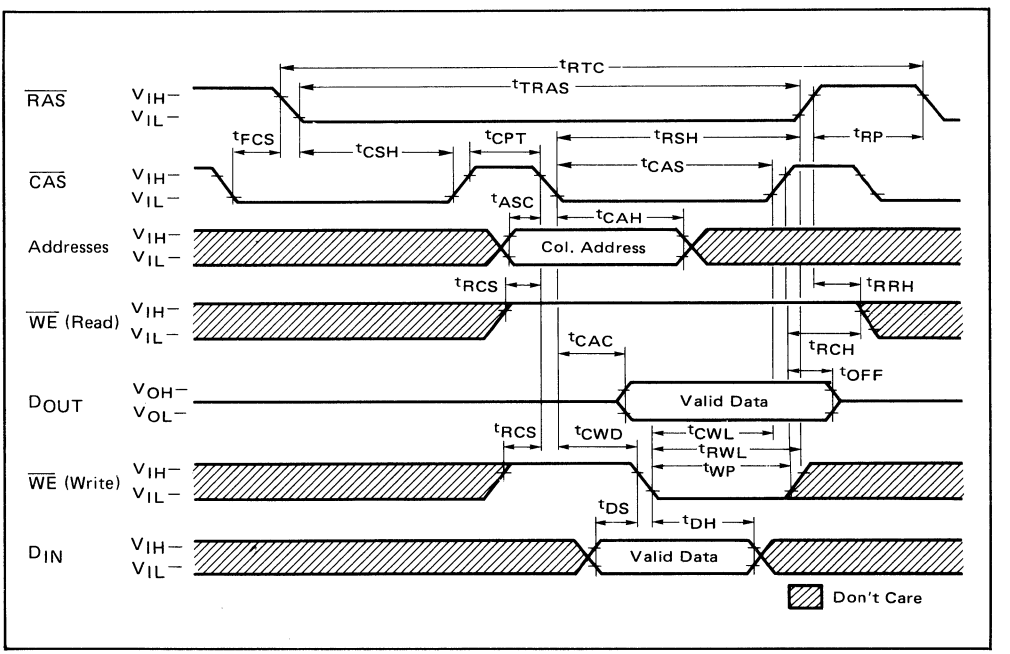
HIDDEN REFRESH CYCLE



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



FUNCTIONAL DESCRIPTION

Simple Timing Requirements:

The MSM41256A has the circuit considerations for easy operational timing requirements for high speed access time operations. The MSM41256A can operate under the condition of t_{RCD} (max) = t_{CAC} which provides an optimal time space for address multiplexing. In addition, the MSM41256A has the minimal hold time of Address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). And the MSM41256A can commit better memory system through-put during operations in an interleaved system. Furthermore, Oki has made timing requirements referenced to $\overline{RAS}$ non-restrictive and deleted from the data sheet, which includes t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. Therefore, the hold times of the Column Address D_{IN} and $\overline{WE}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{WE}$ Delay) are not restricted by t_{RCD}.

Fast Read- While-Write Cycle:

The MSM41256A has the fast read while write cycle which is achieved by excellent control of the three-state output buffer in addition to the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{WE}$ when $\overline{CAS}$ goes low. When $\overline{WE}$ is low during $\overline{CAS}$ transition to low, the MSM41256A goes to early write mode where the output becomes floating and common I/O bus can be used on the system level. Whereas, when $\overline{WE}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MSM41256A goes to delayed write mode where the output contains the data from the cell selected and the data from D_{IN} is written into the cell selected. Therefore, very fast read write cycle becomes available.

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262,144 storage cell location within the MSM41256A. Nine row-address bits are established on the input pins (A_0 through A_8) and latched with the Row Address Strobe ($\overline{RAS}$). Then nine column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode, logic "low" dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM41256A during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data in (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought "low" (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4 milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of the 256 row-addresses (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$ only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the MSM41256A offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle. In MSM41256A hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle:

A special timing sequence using $\overline{CAS}$ before $\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$ before $\overline{RAS}$ refresh activated circuitry. As shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be acceded can be defined as follows:

* A ROW ADDRESS
  - Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set "high" internally.
* A COLUMN ADDRESS
  - All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of CAS.

Suggested $\overline{CAS}$ before $\overline{RAS}$ Counter Test Procedure:

The timing, as shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, is used for all the operations described as follows:

(1) Initialize the internal refresh counter. For this operaton, 8 cycles are required.
(2) Write a test pattern of lows into memory cells at a single column address and 256 row addresses.
(3) By using read-modify-write cycle, read the low written at the last operation (Step (2)) and write a new high in the same cycle. This cycle is repeated 256 times, and highs are written into the 256 memory cells.
(4) Read the high written at the last operation (Step (3)).
(5) Complement the test pattern and repeat the steps (2), (3) and (4).

MSM41256A Bit Map (Physical-Decimal)

□ Pin 16

252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508	
0	0	0	0		0	0	0	0		0	0	0	0		0	0	0	0	
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508	
256	256	256	256		256	256	256	256		256	256	256	256		256	256	256	256	
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508	
1	1	1	1		1	1	1	1		1	1	1	1		1	1	1	1	
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508	
257	257	257	257		257	257	257	257		257	257	257	257		257	257	257	257	
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508	
126	126	126	126		126	126	126	126		126	126	126	126		126	126	126	126	
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508	
382	382	382	382		382	382	382	382		382	382	382	382		382	382	382	382	
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508	
127	127	127	127		127	127	127	127		127	127	127	127		127	127	127	127	
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508	
383	383	383	383		383	383	383	383		383	383	383	383		383	383	383	383	

COLUMN DECODER

ROW DECODER

ROW DECODER

252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508	
511	511	511	511		511	511	511	511		511	511	511	511		511	511	511	511	
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508	
255	255	255	255		255	255	255	255		255	255	255	255		255	255	255	255	
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508	
510	510	510	510		510	510	510	510		510	510	510	510		510	510	510	510	
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508	
254	254	254	254		254	254	254	254		254	254	254	254		254	254	254	254	
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508	
385	385	385	385		385	385	385	385		385	385	385	385		385	385	385	385	
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508	
129	129	129	129		129	129	129	129		129	129	129	129		129	129	129	129	
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508	
384	384	384	384		384	384	384	384		384	384	384	384		384	384	384	384	
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508	
128	128	128	128		128	128	128	128		128	128	128	128		128	128	128	128	

COLUMN DECODER

A8 ROW = "L"
REFRESH ADDRESS

(0 – 255)

A8 ROW = "H"
REFRESH ADDRESS

(0 – 255)

□
Pin 8

A
B

: CELL

A = ROW ADDRESS (DECIMAL)

B = COLUMN ADDRESS (DECIMAL)

MSM41257AAS/RS

262,144-BIT DYNAMIC RANDOM ACCESS MEMORY <Nibble Mode Type>

GENERAL DESCRIPTION

The Oki MSM41257A is a fully decoded, dynamic NMOS random access memory organized as 262144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

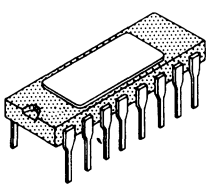
Multiplexed row and column address inputs permit the MSM41257A to be housed in a standard 16 pin DIP. Pin-outs conform to the JEDEC approved pin out. Additionally, the MSM41257A offers new functional enhancements that make it more versatile than previous dynamic RAMs. "CAS-before-$\overline{RAS}$" refresh provides an on-chip refresh capability, also features "nibble mode" which allows high speed serial access to up to 4 bits of data.

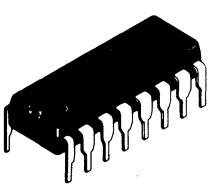
The MSM41257A is fabricated using silicon gate NMOS and Oki's advanced VLSI Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

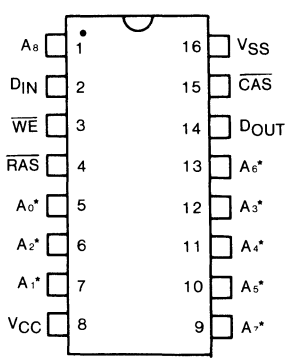
FEATURES

- 262,144 × 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time:
  - 100 ns max (MSM41257A-10AS/RS)
  - 120 ns max (MSM41257A-12AS/RS)
  - 150 ns max (MSM41257A-15AS/RS)
- Cycle time:
  - 200 ns min (MSM41257A-10AS/RS)
  - 220 ns min (MSM41257A-12AS/RS)
  - 260 ns min (MSM41257A-15AS/RS)
- Low power:
  - 385 mW active, 28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" CAS
- 256 refresh cycles/4 ms
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- "Nibble Mode" capability





PIN CONFIGURATION (TOP VIEW)

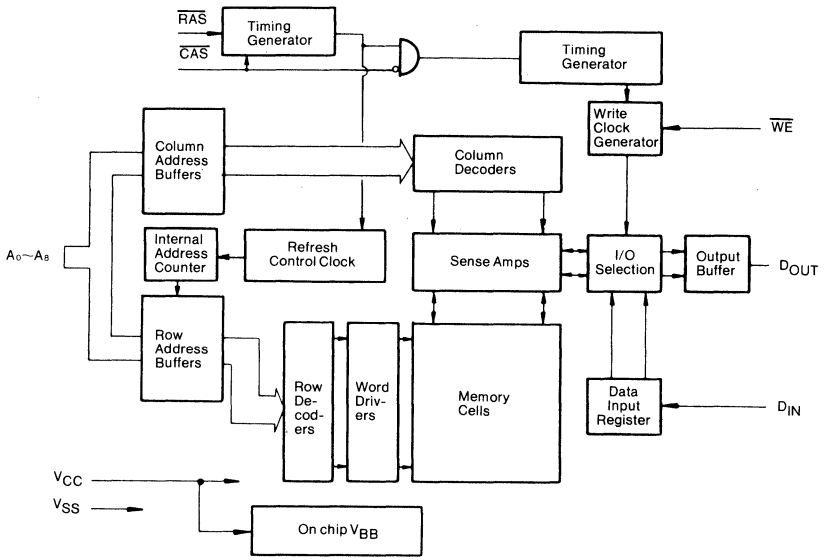


Pin Names	Function
$A_0 \sim A_8$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

* Refresh Address

9

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	Topr	0 to 70	°C
Storage temperature	Tstg	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Parmanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		70	mA	
STANDBY CURRENT Power supply current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC2}		5.0	mA	
REFRESH CURRENT 1 Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$; t_{RC} = min.)	I_{CC3}		60	mA	
NIBBLE MODE CURRENT* Average power supply current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{NC} = min.)	I_{CC4}		30	mA	
REFRESH CURRENT 2 Average power supply current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = min.)	I_{CC5}		65	mA	
INPUT LEAKAGE CURRENT Input leakage current, any input ($0V \leq V_{IN} \leq 5.5V$, all other pins not under test = 0V)	I_{LI}	−10	10	μA	
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	I_{LO}	−10	10	μA	
OUTPUT LEVELS Output high voltage ($I_{OH} = -5$ mA) Output low voltage ($I_{OL} = 4.2$ mA)	V_{OH} V_{OL}	2.4	0.4	V V	

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

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CAPACITANCE
(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input capacitance ($A_0 \sim A_8$, D_{IN})	C_{IN1}	–	7	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	–	10	pF
Output capacitance (D_{OUT})	C_{OUT}	–	7	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

Parameter	Symbol	Unit	MSM41257A-10		MSM41257A-12		MSM41257A-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4		4	
Random read or write cycle time	t_{RC}	ns	200		220		260		
Read-write cycle time	t_{RWC}	ns	200		220		260		
Access time from $\overline{RAS}$	t_{RAC}	ns		100		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		50		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	30	0	30	0	30	
Transition time	t_T	ns	3	50	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	85		90		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	105	10μs	120	10μs	150	10μs	
$\overline{RAS}$ hold time	t_{RSH}	ns	55		60		75		
$\overline{CAS}$ pulse width	t_{CAS}	ns	55	10μs	60	10μs	75	10μs	
$\overline{CAS}$ hold time	t_{CSH}	ns	105		120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	50	25	60	25	75	7
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	ns	20		20		20		
Row address set-up time	t_{ASR}	ns	0		0		0		
Row address hold time	t_{RAH}	ns	15		15		15		
Column address set-up time	t_{ASC}	ns	0		0		0		
Column address hold time	t_{CAH}	ns	20		20		25		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	ns	0		0		0		
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	20		20		20		
Write command set-up time	t_{WCS}	ns	0		0		0		8

AC CHARACTERISTICS (Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Unit	MSM41257A-10		MSM41257A-12		MSM41257A-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Write command pulse width	t_{WP}	ns	15		20		25		
Write command hold time	t_{WCH}	ns	15		20		25		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	35		40		45		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	35		40		45		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	20		20		25		
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	ns	15		20		25		8
Refresh set-up time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCS}	ns	20		25		30		
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCH}	ns	20		25		30		
$\overline{CAS}$ precharge time (C before R cycle)	t_{CPR}	ns	20		25		30		
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	ns	20		20		20		
Nibble mode read/write cycle time	t_{NC}	ns	55		60		70		9
Nibble mode read-write cycle time	t_{NRWC}	ns	55		60		70		9
Nibble mode access time	t_{NCAC}	ns		25		30		35	9
Nibble mode $\overline{CAS}$ pulse width	t_{NCAS}	ns	25		30		35		9
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	ns	20		25		30		9
Nibble mode read $\overline{RAS}$ hold time	t_{NRRSH}	ns	25		30		40		9
Nibble mode write $\overline{RAS}$ hold time	t_{NWRSH}	ns	45		50		60		9
Nibble mode $\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{RNH}	ns	20		20		20		9

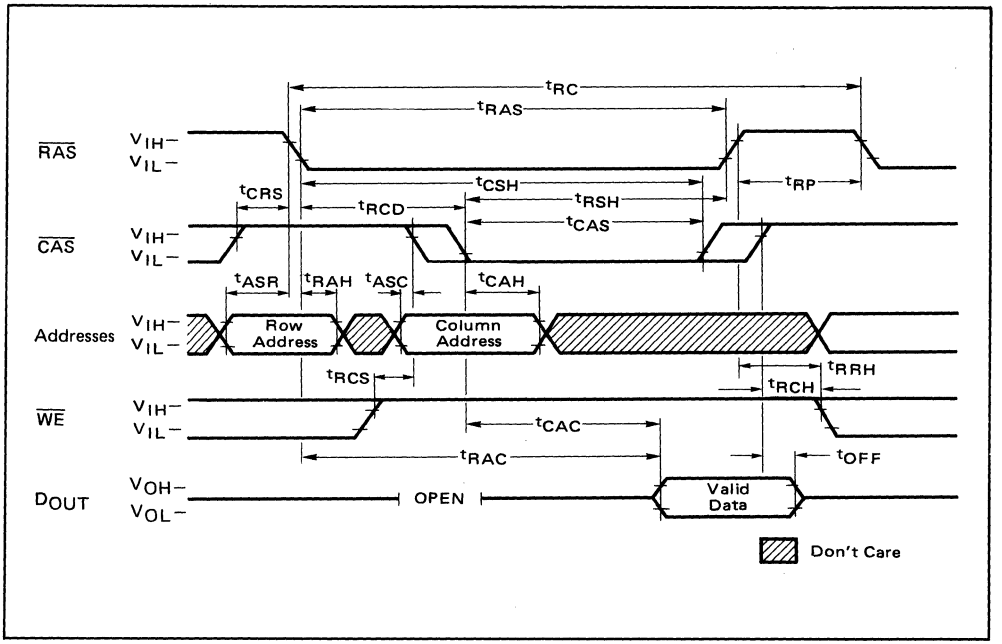
AC CHARACTERISTICS (Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Unit	MSM41257A-10		MSM41257A-12		MSM41257A-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh counter test cycle time	t_{RTC}	ns	340		375		430		10
Refresh counter test $\overline{RAS}$ pulse width	t_{TRAS}	ns	230	10μs	265	10μs	320	10μs	10
Refresh counter test $\overline{CAS}$ precharge time	t_{CPT}	ns	50		60		70		10

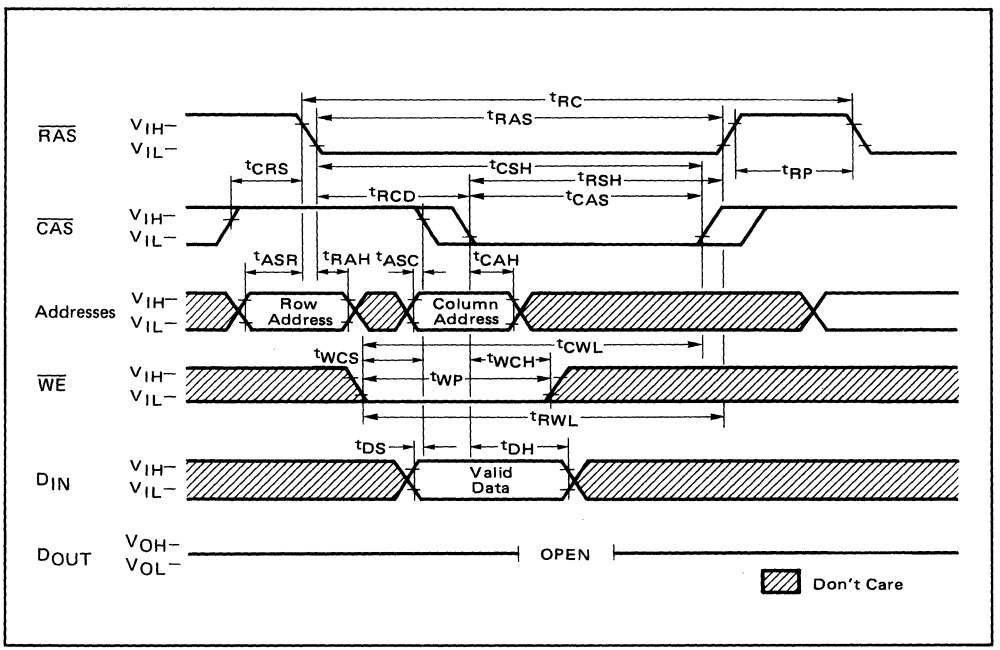
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical charcteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. Nibble mode cycle.
10. $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Cycle only.

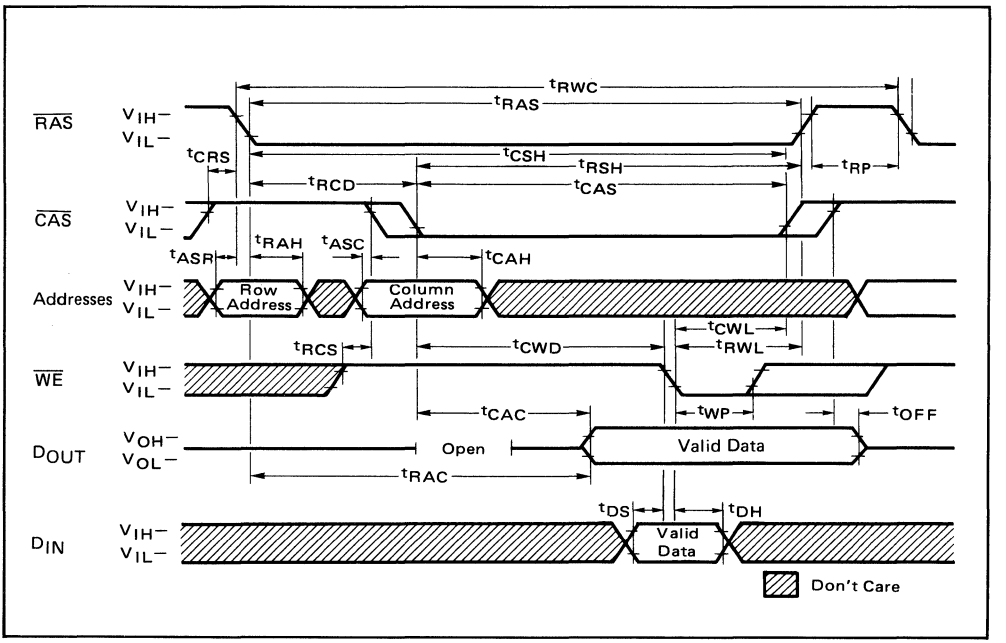
READ CYCLE



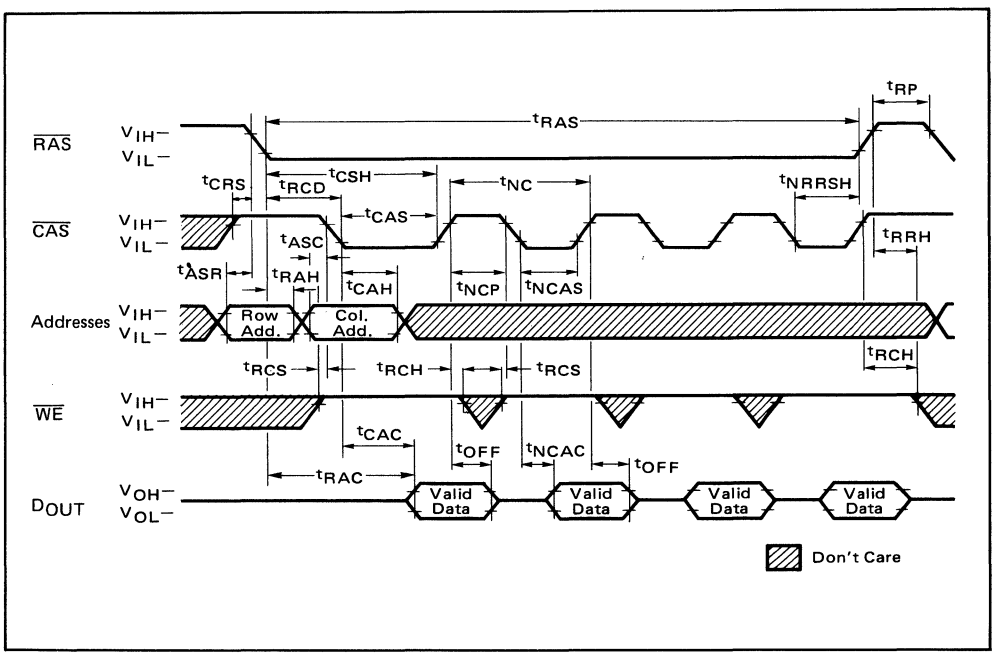
WRITE CYCLE (EARLY WRITE)



READ-WRITE/READ-MODIFY-WRITE CYCLE



NIBBLE MODE READ CYCLE



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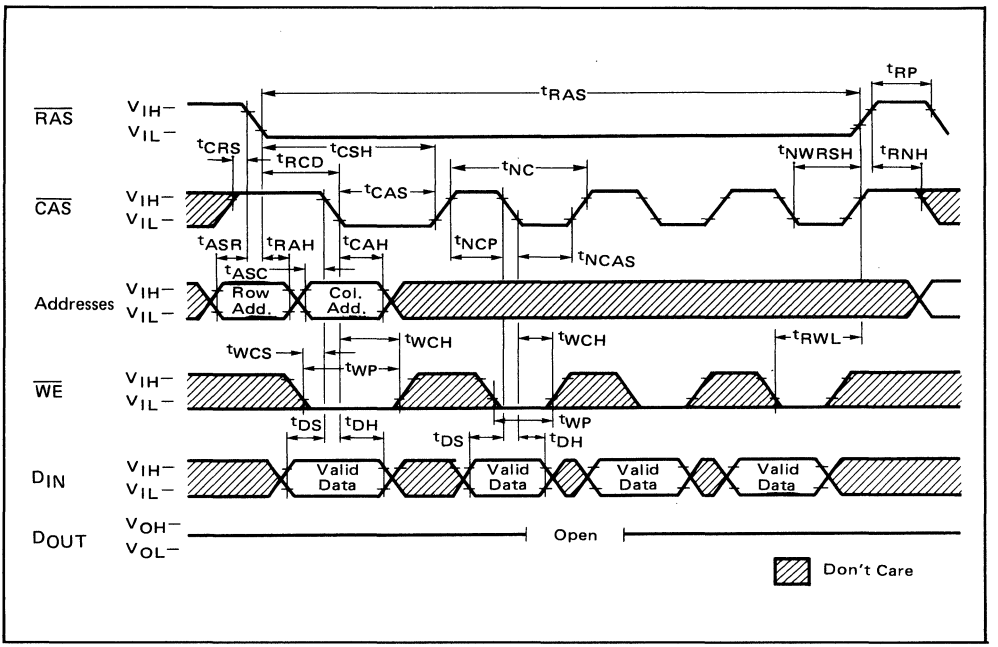
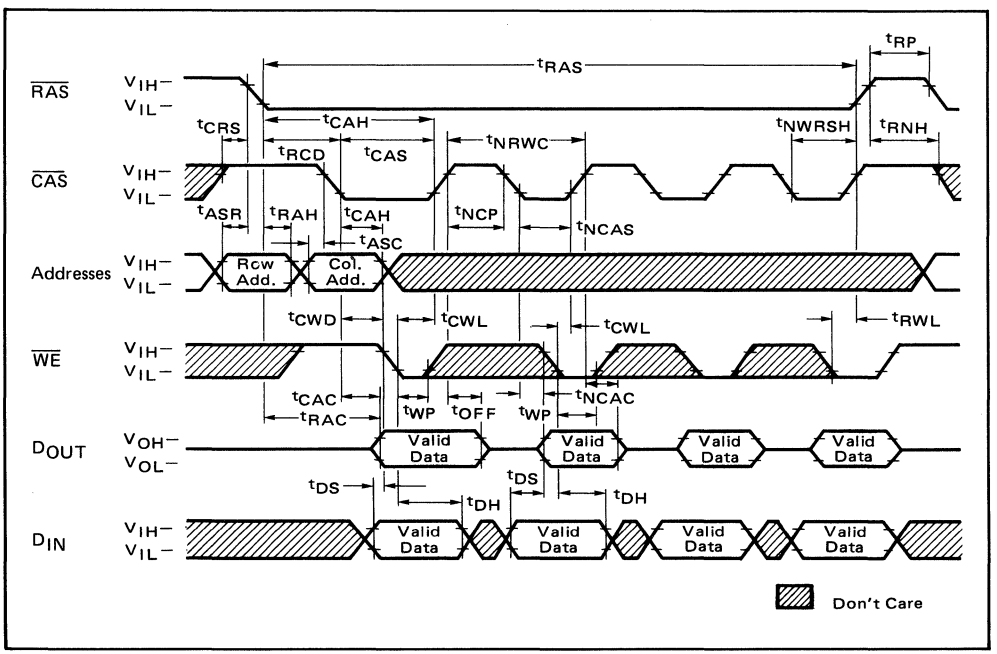
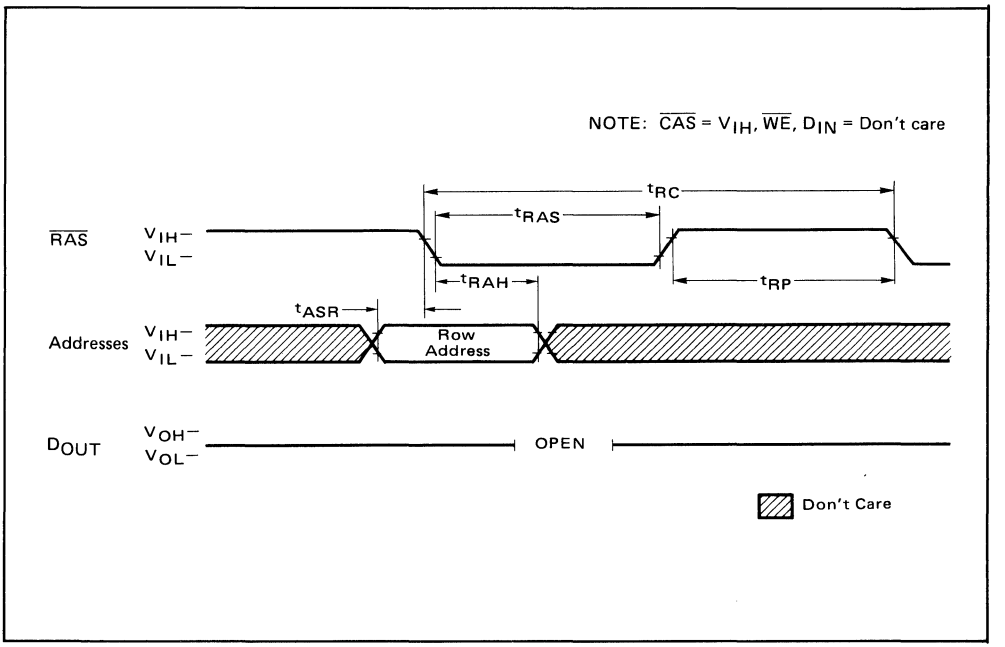
NIBBLE MODE WRITE CYCLE



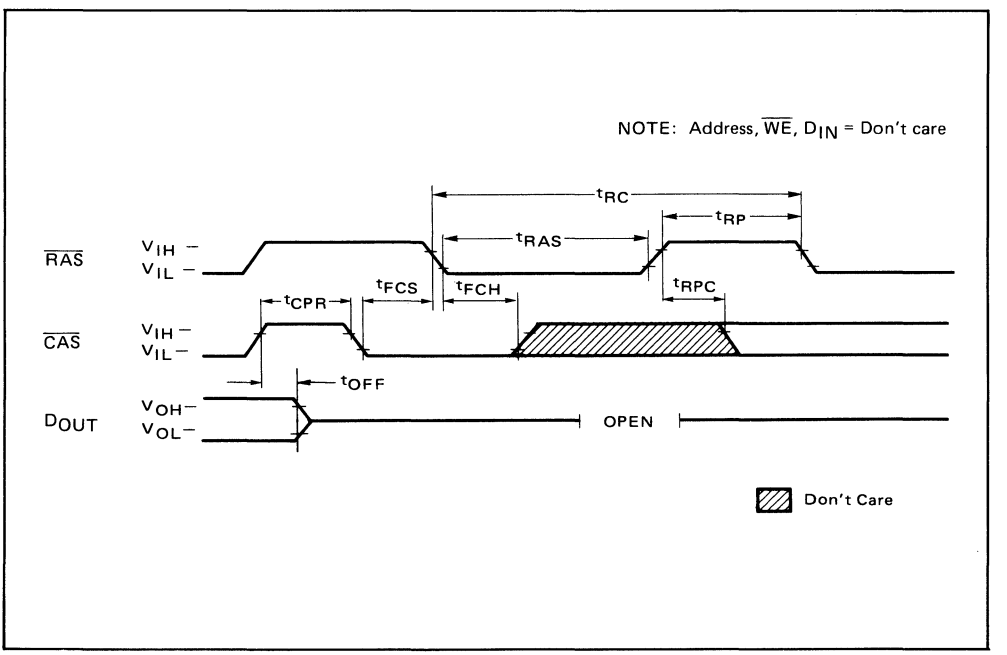
NIBBLE MODE READ-WRITE CYCLE



$\overline{RAS}$ ONLY REFRESH CYCLE



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



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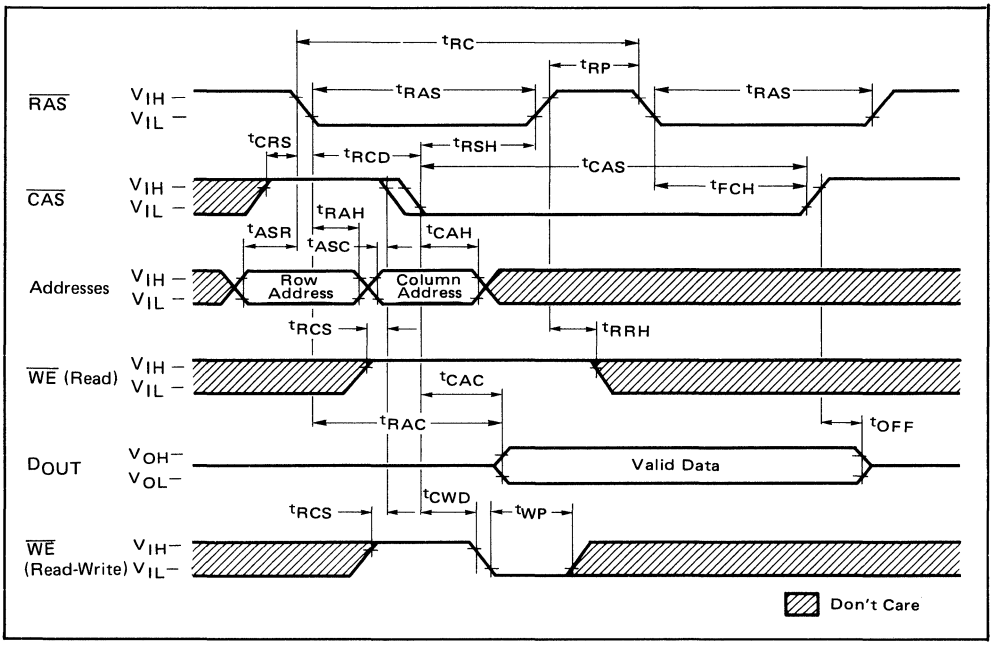
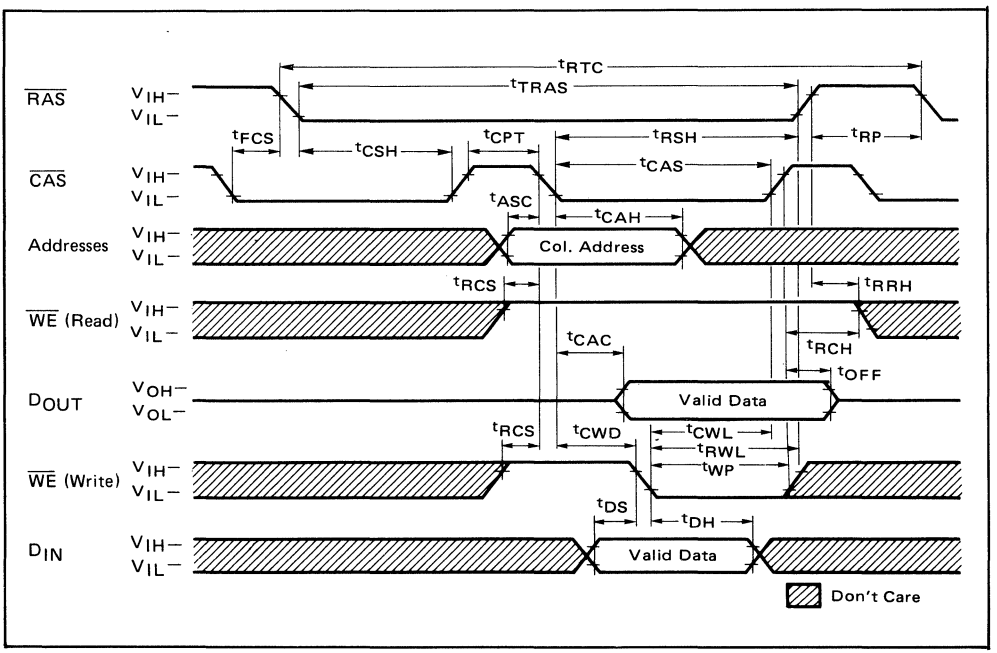
HIDDEN REFRESH CYCLE



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



9

FUNCTIONAL DESCRIPTION

Simple Timing Requirements:

The MSM41257A has the circuit considerations for easy operational timing requirements for high speed access time operations. The MSM41257A can operate under the condition of t_{RCD} (max) = t_{CAC} which provides an optimal time space for address multiplexing. In addition, the MSM41257A has the minimal hold time of Address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). And the MSM41257A can commit better memory system through-put during operations in an interleaved system. Furthermore, Oki has made timing requirements referenced to $\overline{RAS}$ non-restrictive and deleted from the data sheet, which includes t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. Therefore, the hold times of the Column Address D_{IN} and $\overline{WE}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{WE}$ Delay) are not restricted by t_{RCD}.

Fast Read- While-Write Cycle:

The MSM41257A has the fast read while write cycle which is achieved by excellent control of the three-state output buffer in addition to the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{WE}$ when $\overline{CAS}$ goes low. When $\overline{WE}$ is low during $\overline{CAS}$ transition to low, the MSM41257A goes to early write mode where the output becomes floating and common I/O bus can be used on the system level. Whereas, when $\overline{WE}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MSM41257A goes to delayed write mode where the output contains the data from the cell selected and the data from D_{IN} is written into the cell selected. Therefore, very fast read write cycle becomes available.

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262,144 storage cell location within the MSM41257A. Nine row-address bits are established on the input pins (A_0 through A_8) and latched with the Row Address Strobe ($\overline{RAS}$). Then nine column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode, logic "low" dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM41257A during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data in (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought "low" (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Nibble Mode:

Nibble mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and the 8 column addresses. The 2 bits of addresses (CA_8 RA_8) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by normal mode, the remaining nibble bits may be accessed by $\overline{CAS}$ "high" then "low" while $\overline{RAS}$ remains "low". Toggling $\overline{CAS}$ causes RA_8 and CA_8 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See Table 1)

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation may be executed again on subsequent access, the new data will be written into the selected cell location.

In nibble mode, the three-state control of D_{OUT} Pin is determined by the first normal access cycle.

The data output is controlled by only $\overline{WE}$ state referenced at $\overline{CAS}$ negative transition of the normal cycle (first Nibble bit). That is, when $t_{WCS} > t_{WCS}$ (min) is met, the data output will remain open circuit throughout the succeeding Nibble cycle regardless of $\overline{WE}$ state. Whereas, when $t_{CWD} > t_{CWD}$ (min) is met, the data output will contain data from the cell selected during the succeeding nibble cycle regardless of $\overline{WE}$ state. The write operation is done during the period where $\overline{WE}$ and $\overline{CAS}$ clocks are low. Therefore, write operation can be done bit by bit during each nibble operation at any timing conditions of $\overline{WE}$ (t_{WCS} and t_{CWD}) at the normal cycle (first Nibble bit).

Table 1 NIBBLE MODE ADDRESS SEQUENCE EXAMPLE

SEQUENCE	NIBBLE BIT	RA_8	ROW ADDRESS	CA_8	COLUMN ADDRESS	
$\overline{RAS}/\overline{CAS}$ (normal mode)	1	0	10101010	0	10101010	. . . input addresses
toggle $\overline{CAS}$ (nibble mode)	2	1	10101010	0	10101010	generated internally sequence repeats
toggle $\overline{CAS}$ (nibble mode)	3	0	10101010	1	10101010	
toggle $\overline{CAS}$ (nibble mode)	4	1	10101010	1	10101010	
toggle $\overline{CAS}$ (nibble mode)	1	0	10101010	0	10101010	

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4 milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of the 256 row-addresses (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$ only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the MSM41257A offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle. In MSM41257A hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle:

A special timing sequence using $\overline{CAS}$ before $\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$ before $\overline{RAS}$ refresh activated circuitry. As shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be acceded can be defined as follows:

* A ROW ADDRESS
  - Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set "high" internally.
* A COLUMN ADDRESS
  - All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of CAS.

Suggested $\overline{CAS}$ before $\overline{RAS}$ Counter Test Procedure:

The timing, as shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, is used for all the operations described as follows:

(1) Initialize the internal refresh counter. For this operaton, 8 cycles are required.
(2) Write a test pattern of lows into memory cells at a single column address and 256 row addresses.
(3) By using read-modify-write cycle, read the low written at the last operation (Step (2)) and write a new high in the same cycle. This cycle is repeated 256 times, and highs are written into the 256 memory cells.
(4) Read the high written at the last operation (Step (3)).
(5) Complement the test pattern and repeat the steps (2), (3) and (4).

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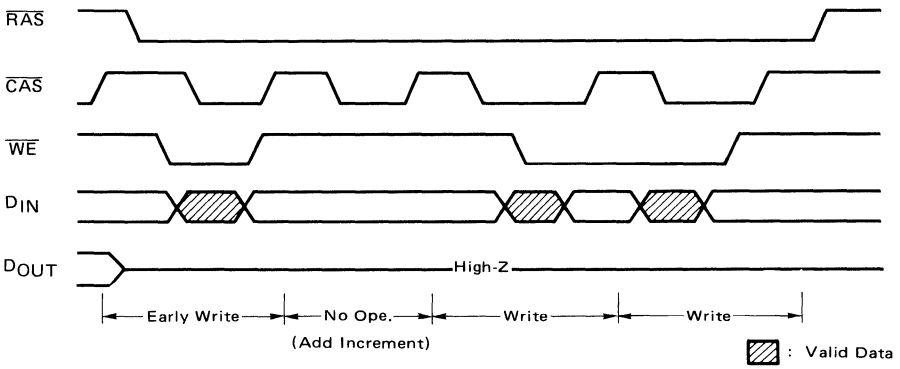
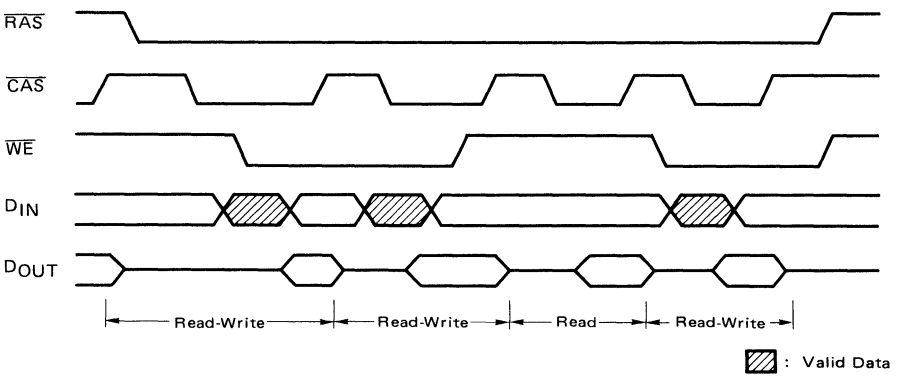
NIBBLE MODE

1) The case of first nibble cycle is Early write



2) The case of first nibble cycle is delyed write (Read-Write)



9

MSM41257A Bit Map (Physical-Decimal)

□ Pin 16

252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
0	0	0	0		0	0	0	0		0	0	0	0		0	0	0	0
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
256	256	256	256		256	256	256	256		256	256	256	256		256	256	256	256
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
1	1	1	1		1	1	1	1		1	1	1	1		1	1	1	1
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
257	257	257	257		257	257	257	257		257	257	257	257		257	257	257	257
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
126	126	126	126		126	126	126	126		126	126	126	126		126	126	126	126
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
382	382	382	382		382	382	382	382		382	382	382	382		382	382	382	382
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
127	127	127	127		127	127	127	127		127	127	127	127		127	127	127	127
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
383	383	383	383		383	383	383	383		383	383	383	383		383	383	383	383

COLUMN DECODER

ROW DECODER

ROW DECODER

252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
511	511	511	511		511	511	511	511		511	511	511	511		511	511	511	511
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
255	255	255	255		255	255	255	255		255	255	255	255		255	255	255	255
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
510	510	510	510		510	510	510	510		510	510	510	510		510	510	510	510
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
254	254	254	254		254	254	254	254		254	254	254	254		254	254	254	254
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
385	385	385	385		385	385	385	385		385	385	385	385		385	385	385	385
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
129	129	129	129		129	129	129	129		129	129	129	129		129	129	129	129
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
384	384	384	384		384	384	384	384		384	384	384	384		384	384	384	384
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
128	128	128	128		128	128	128	128		128	128	128	128		128	128	128	128

COLUMN DECODER

A8 ROW = "L"
REFRESH ADDRESS

(0 – 255)

A8 ROW = "H"
REFRESH ADDRESS

(0 – 255)

□
Pin 8

A
B

: CELL

A = ROW ADDRESS (DECIMAL)
B = COLUMN ADDRESS (DECIMAL)

9

MSM41464RS

65,536-WORD × 4-BITS DYNAMIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION

The Oki MSM41464 is a fully decoded, dynamic NMOS random access memory organized as 65,536 words by 4 bits. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

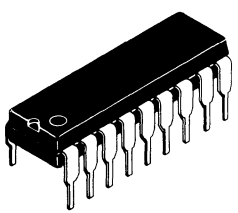
Multiplexed row and column address inputs permit the MSM41464 to be housed in a standard 18 pin DIP. Pin-outs conform to the JEDEC approved pin out. Additionally, the MSM41464 offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability.

The MSM41464 is fabricated using silicon gate NMOS and Oki's advanced VLSI Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

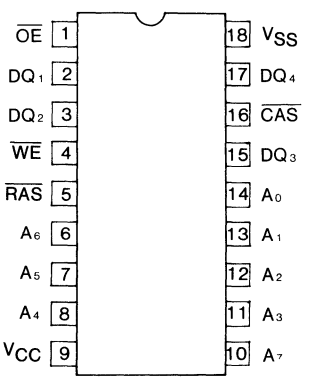
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

- 65,536 × 4 RAM, 18 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time:
  - 100 ns max (MSM41464-10RS)
  - 120 ns max (MSM41464-12RS)
  - 150 ns max (MSM41464-15RS)
- Cycle time:
  - 200 ns min (MSM41464-10RS)
  - 230 ns min (MSM41464-12RS)
  - 260 ns min (MSM41464-15RS)
- Low power:
  - 385 mW active, 28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 256 refresh cycles/4 ms
- Output impedance controllable through early write and $\overline{OE}$ operations
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- "Page Mode" capability



PIN CONFIGURATION (TOP VIEW)



Pin Names	Function
$A_0 \sim A_7$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$DQ_1 \sim DQ_4$	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

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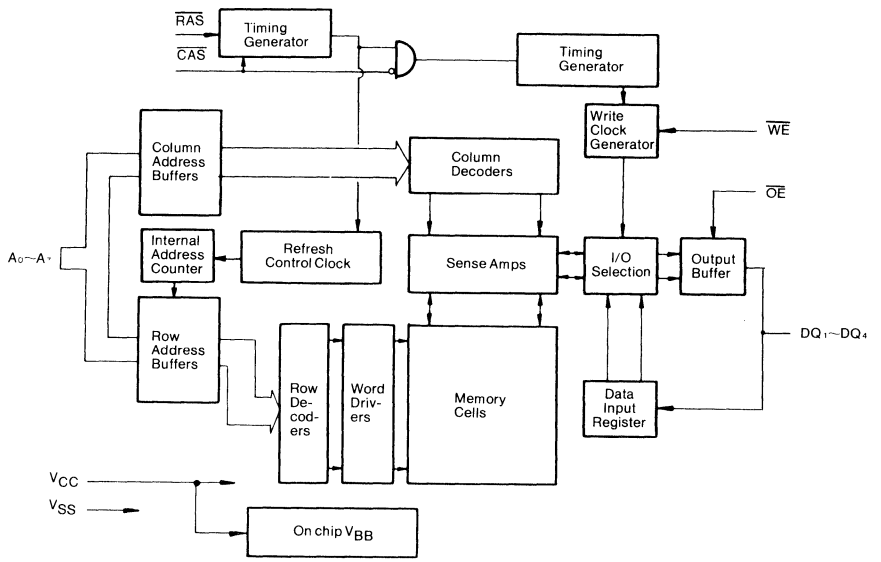
FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	Topr	0 to 70	°C
Storage temperature	Tstg	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Parmanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		70	mA	
STANDBY CURRENT* Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		5.0	mA	
REFRESH CURRENT 1* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}		55	mA	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}		60	mA	
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = min.)	I_{CC5}		60	mA	
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−10	10	μA	
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	μA	
OUTPUT LEVELS Output high voltage (I_{OH} = −5 mA) Output low voltage (I_{OL} = 4.2 mA)	V_{OH} V_{OL}	2.4	 0.4	V V	

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE
(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input capacitance ($A_0 \sim A_7$)	C_{IN1}	–	7	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	–	10	pF
Data I/O capacitance ($DQ_1 \sim DQ_4$)	C_D	–	7	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

Parameter	Symbol	Unit	MSM41464-10		MSM41464-12		MSM41464-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4		4	
Random read or write cycle time	t_{RC}	ns	200		230		260		
Read-write cycle time	t_{RWC}	ns	275		320		360		
Page mode cycle time	t_{PC}	ns	100		120		145		
Access time from $\overline{RAS}$	t_{RAC}	ns		100		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		50		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	30	0	35	0	40	
Transition time	t_T	ns	3	50	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		100		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	100	10μs	120	10μs	150	10μs	
$\overline{RAS}$ hold time	t_{RSH}	ns	50		60		75		
$\overline{CAS}$ precharge time (Page mode cycle only)	t_{CP}	ns	40		50		60		
$\overline{CAS}$ pulse width	t_{CAS}	ns	50	10μs	60	10μs	75	10μs	
$\overline{CAS}$ hold time	t_{CSH}	ns	100		120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	22	50	22	60	25	75	7, 8
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	ns	20		25		30		
Row address set-up time	t_{ASR}	ns	0		0		0		
Row address hold time	t_{RAH}	ns	12		12		15		
Column address set-up time	t_{ASC}	ns	0		0		0		
Column address hold time	t_{CAH}	ns	15		15		20		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time	t_{RCH}	ns	0		0		0		10
Write command set-up time	t_{WCS}	ns	−5		−5		−5		9

AC CHARACTERISTICS (Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Unit	MSM41464-10		MSM41454-12		MSM41464-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Write command pulse width	t_{WP}	ns	20		25		30		
Write command hold time	t_{WCH}	ns	20		25		30		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	35		45		50		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	35		45		50		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	20		25		30		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	85		100		120		9
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	135		160		195		9
Read command hold time reference to $\overline{RAS}$	t_{RRH}	ns	20		20		25		10
Access time from $\overline{OE}$	t_{OEA}	ns		25		30		40	
$\overline{OE}$ data delay time	t_{OED}	ns	30		35		40		
$\overline{OE}$ hold time	t_{OEH}	ns	0		0		0		
Turn-off delay time from $\overline{OE}$	t_{OEZ}	ns	0	30	0	35	0	40	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCS}	ns	20		25		30		
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCH}	ns	20		25		30		
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	ns	20		20		20		
$\overline{CAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CPR}	ns	20		25		30		
Read/write cycle (Refresh counter test)	t_{RTC}	ns	385		450		515		11
$\overline{RAS}$ pulse width (Refresh counter test)	t_{TRAS}	ns	285	10μs	340	10μs	405	10μs	11
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	ns	50		60		70		11
Read/write cycle time (Page mode)	t_{PRWC}	ns	175		210		245		

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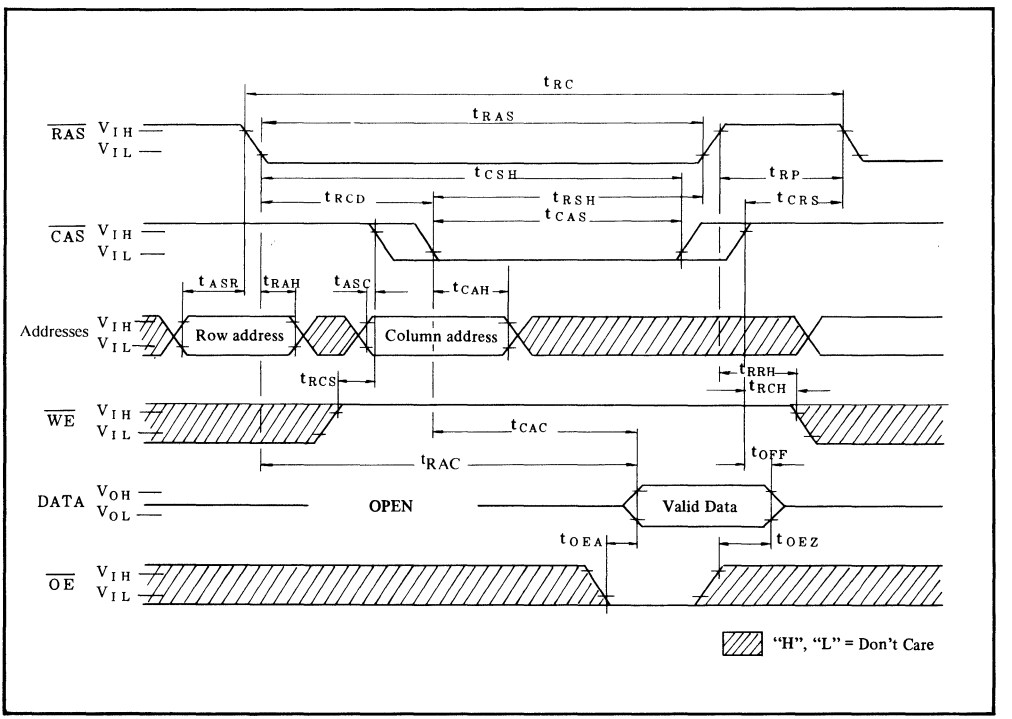
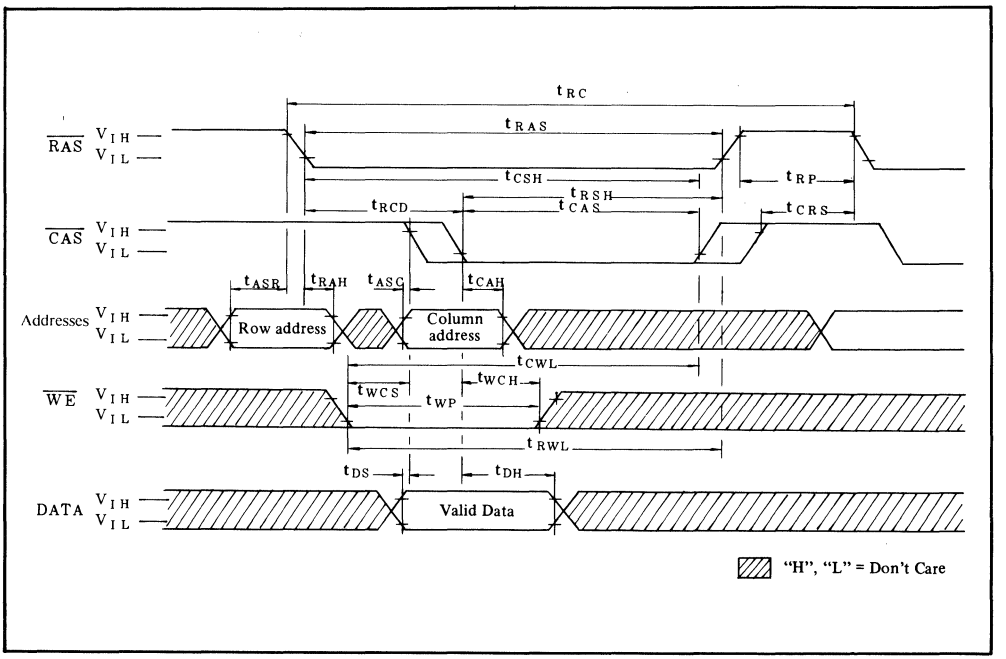
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.) If $t_{RCD} > t_{RCD}$ (Max.), t_{RAC} will increase by $\{t_{RCD} - t_{RCD}$ (Max.)$\}$.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. Assumes that t_{RCD} (Min.) $= t_{RAH}$ (Min.) $+ 2t_T + t_{ASC}$ (Min.)
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical charcteristics only; if $t_{WCS} > t_{WCS}$ (Min.), the cycle is an early write cycle and the data in/data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (Min.) and $t_{RWD} \geqq t_{RWD}$ (Min.) the cycle is read-write cycle and the data in/data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle only.

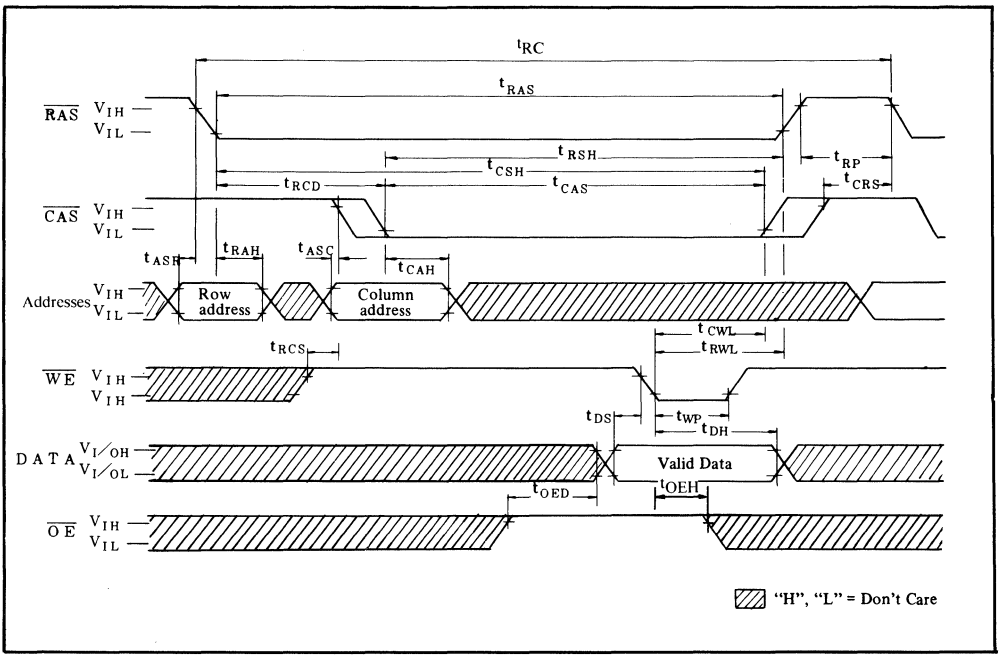
READ CYCLE



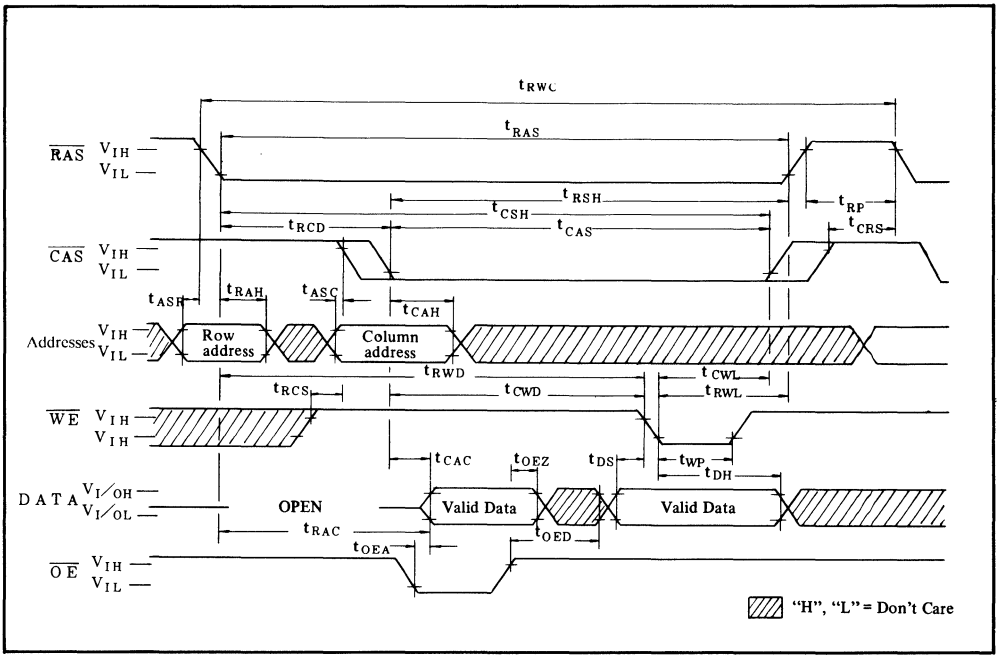
WRITE CYCLE (EARLY WRITE)



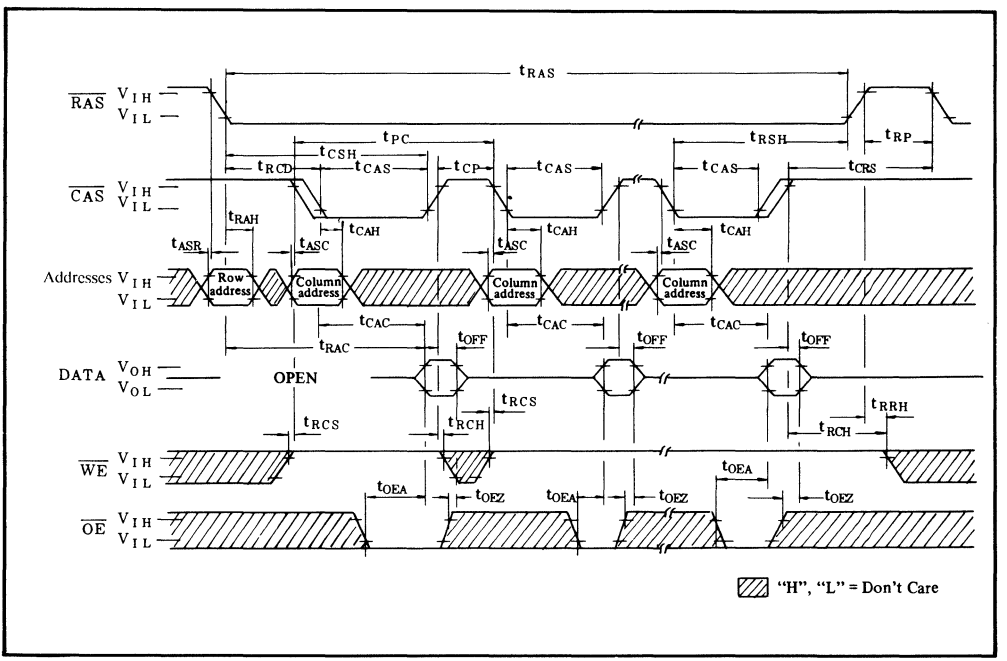
OE WRITE CYCLE



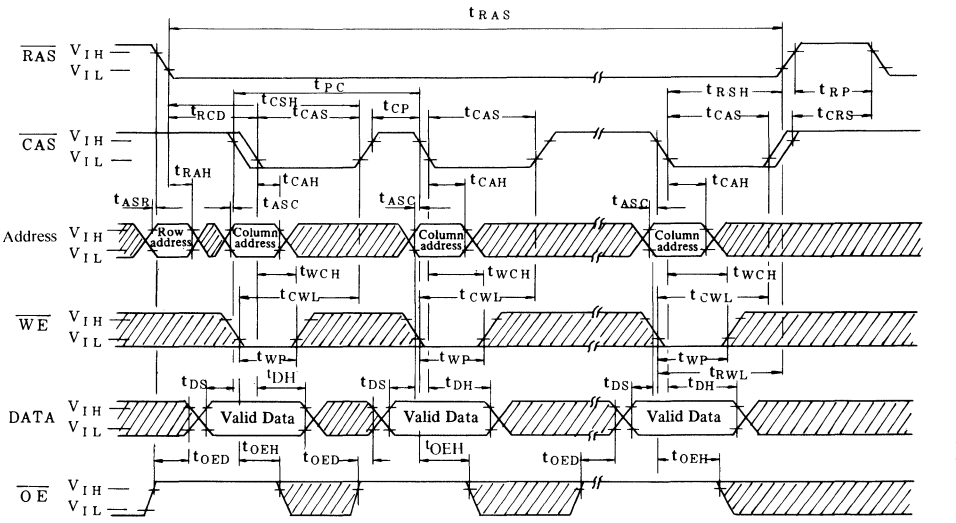
READ/WRITE AND READ MODIFY WRITE CYCLE



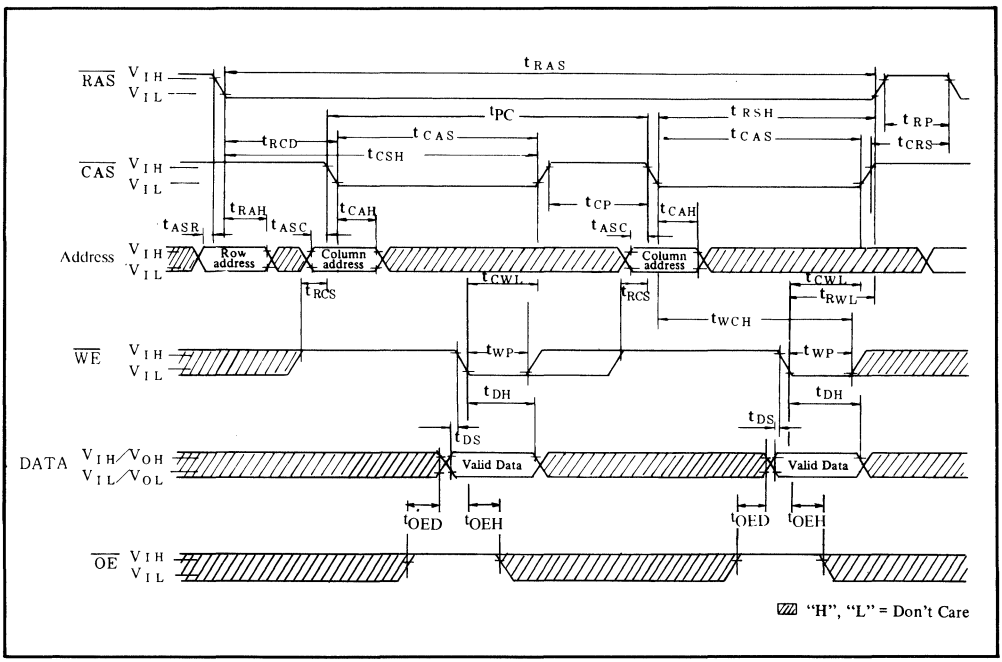
PAGE MODE READ CYCLE



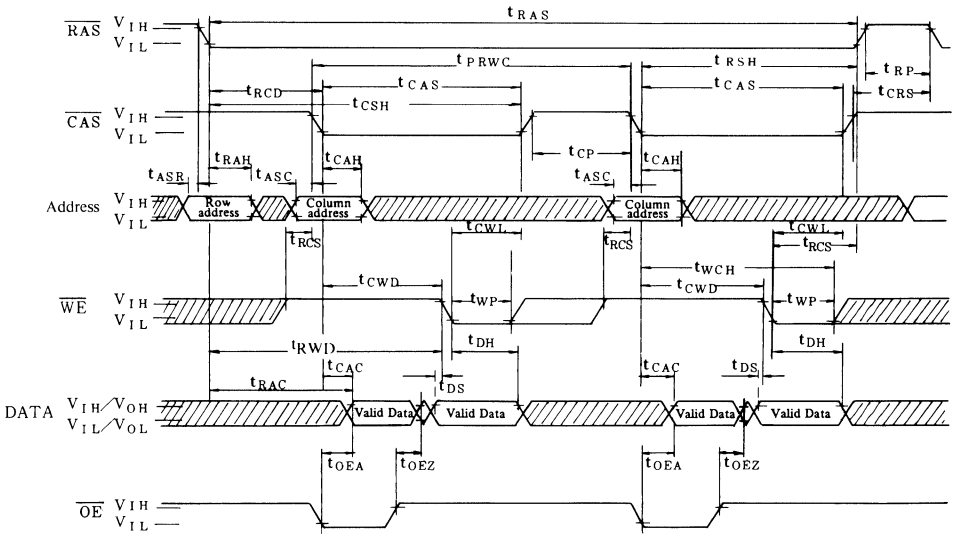
PAGE MODE WRITE CYCLE



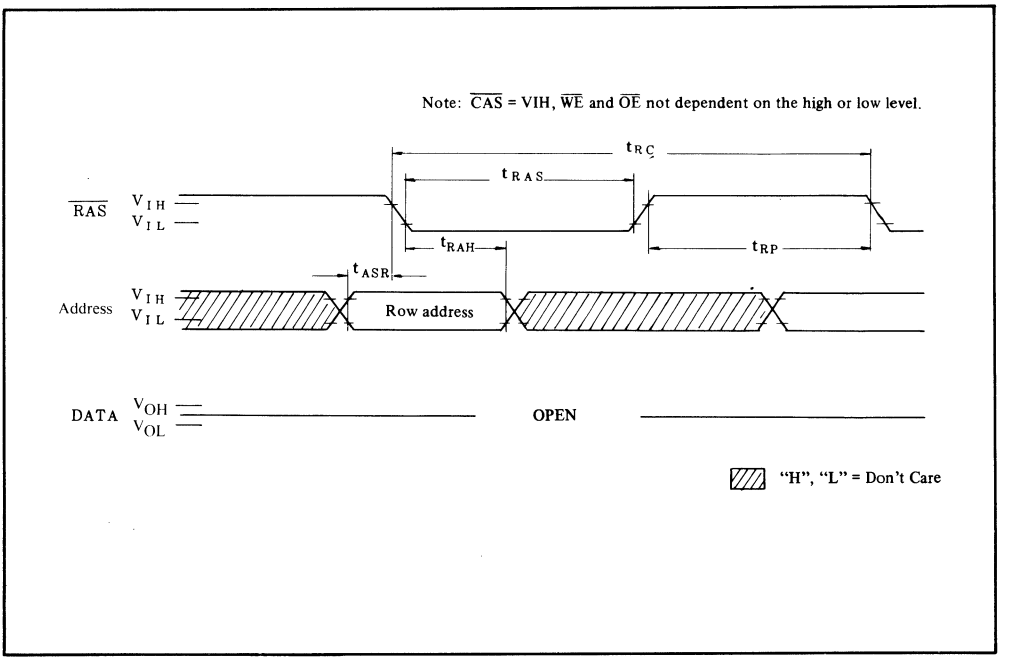
PAGE MODE $\overline{OE}$ WRITE CYCLE



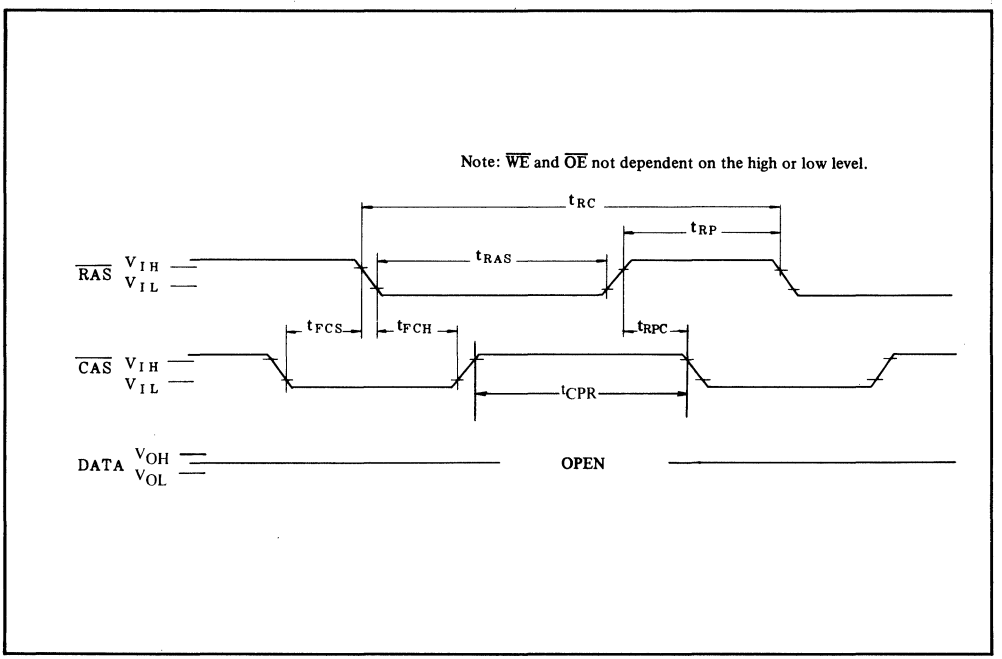
PAGE MODE READ/WRITE CYCLE



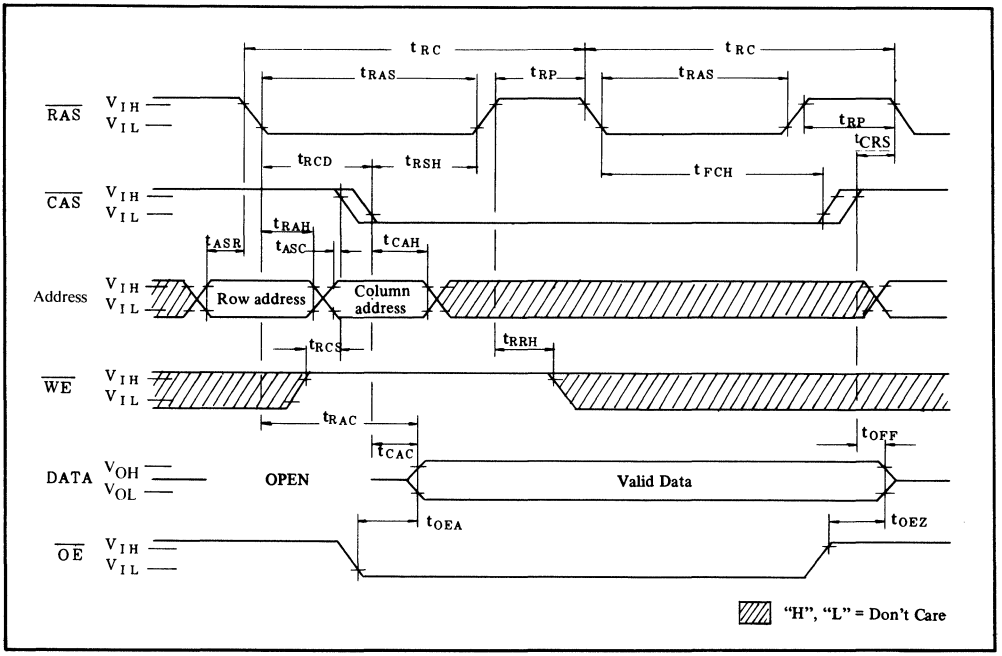
RAS ONLY REFRESH CYCLE



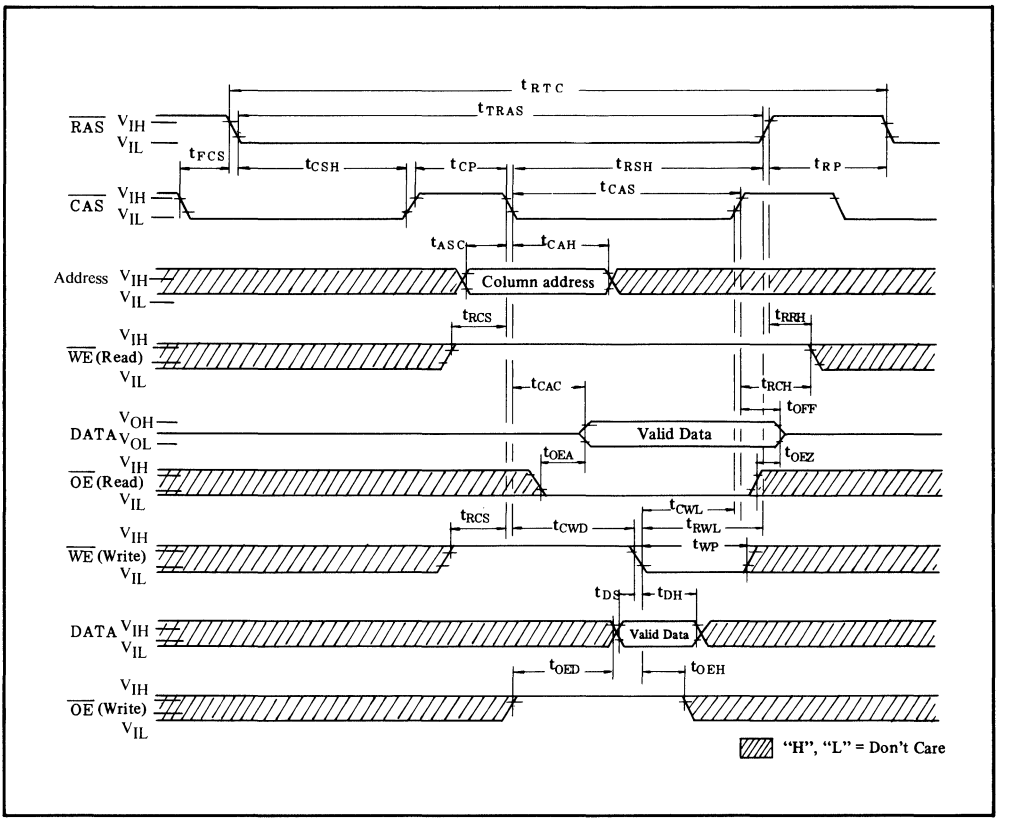
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



FUNCTIONAL DESCRIPTION

Address Inputs:

16 bits of binary address input are required to decode any one of the 65,536 words by 4 bit storage cell locations.

8 row-address bits are set up on address input pins A_0 through A_7 and latched onto the chip by the row address strobe (RAS). Then 8 column-address bits are set up on pins A_0 through A_7 and latched onto the chip by the column address strobe (CAS).

All addresses must be stable on or before the falling edges of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (gated) by the $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Therefore specifications permit column addresses to be input immediately after the row address hold time (t_{RAH}).

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. The logic high of the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The data input is disabled when the read mode is selected. Data-out will remain in the high-impedance state allowing a write cycle with $\overline{WE}$ grounded.

Data Input:

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latches. In an early-write cycle, $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{WE}$ with setup and hold times referenced to this signal. In delayed or read-modify-write, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

Data Output:

The three-state output buffer provides direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} and t_{OEA} are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ or $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the output is always in the high impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfy t_{OED}.

Output Enable:

The $\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low impedance state. Once in the low impedance state, they will remain in the low impedance state until $\overline{OE}$ or $\overline{CAS}$ is brought high.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every four milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 (A_0 to A_7) row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

$\overline{CAS}$ before $\overline{RAS}$ refreshing offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. Hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle:

A special timing sequence using $\overline{CAS}$ before $\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$ before $\overline{RAS}$ refresh activated circuitry. As shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. This is shown in the $\overline{CAS}$ before $\overline{RAS}$ counter test cycle. A memory cell address, consisting of a row address (8 bits) and a column address (8 bits), to be acceded can be defined as follows:

* A ROW ADDRESS
  - Bits A_0 through A_7 are defined by the refresh counter.
* A COLUMN ADDRESS
  - All the bits A_0 through A_7 are defined by latching levels on A_0 through A_7 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$ before $\overline{RAS}$ Counter Test Procedure:

The timing, as shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, is used for all the operations described as follows:

(1) Initialize the internal refresh counter. For this operaton, 8 cycles are required.
(2) Write a test pattern of lows into memory cells at a single column address and 256 row addresses.
(3) By using read-modify-write cycle, read the low written at the last operation (Step (2)) and write a new high in the same cycle. This cycle is repeated 256 times, and highs are written into the 256 memory cells.
(4) Read the high written at the last operation (Step (3)).
(5) Complement the test pattern and repeat the steps (2), (3) and (4).

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MSM41464 Bit Map (Physical-Decimal)

□ Pin 18

DQ1 DQ2 DQ3 DQ4

252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
1	1	1	1	1	1	1	1		1	1	1	1	1	1	1	1
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
1	1	1	1	1	1	1	1		1	1	1	1	1	1	1	1
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
2	2	2	2	2	2	2	2		2	2	2	2	2	2	2	2
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
2	2	2	2	2	2	2	2		2	2	2	2	2	2	2	2
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
125	125	125	125	125	125	125	125		125	125	125	125	125	125	125	125
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
125	125	125	125	125	125	125	125		125	125	125	125	125	125	125	125
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
126	126	126	126	126	126	126	126		126	126	126	126	126	126	126	126
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
126	126	126	126	126	126	126	126		126	126	126	126	126	126	126	126
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
127	127	127	127	127	127	127	127		127	127	127	127	127	127	127	127
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
127	127	127	127	127	127	127	127		127	127	127	127	127	127	127	127

COLUMN DECODER

ROW DECODER

ROW DECODER

252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
255	255	255	255	255	255	255	255		255	255	255	255	255	255	255	255
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
255	255	255	255	255	255	255	255		255	255	255	255	255	255	255	255
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
254	254	254	254	254	254	254	254		254	254	254	254	254	254	254	254
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
254	254	254	254	254	254	254	254		254	254	254	254	254	254	254	254
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
253	253	253	253	253	253	253	253		253	253	253	253	253	253	253	253
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
253	253	253	253	253	253	253	253		253	253	253	253	253	253	253	253
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
130	130	130	130	130	130	130	130		130	130	130	130	130	130	130	130
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
130	130	130	130	130	130	130	130		130	130	130	130	130	130	130	130
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
129	129	129	129	129	129	129	129		129	129	129	129	129	129	129	129
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
129	129	129	129	129	129	129	129		129	129	129	129	129	129	129	129
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
128	128	128	128	128	128	128	128		128	128	128	128	128	128	128	128
252	253	254	255	3	2	1	0		0	1	2	3	255	254	253	252
128	128	128	128	128	128	128	128		128	128	128	128	128	128	128	128

COLUMN DECODER

REFRESH ADDRESS (0 – 255)

REFRESH ADDRESS (0 – 255)

□ Pin 9

A
B

: CELL

A = ROW ADDRESS (DECIMAL)

B = COLUMN ADDRESS (DECIMAL)

9

Preliminary

MSM414256RS

262,144-WORD × 4-BITS DYNAMIC RAM

GENERAL DESCRIPTION

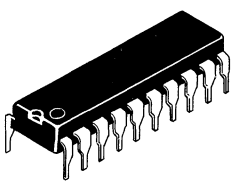
The MSM414256RS is a new generation dynamic RAM organized as 262,144 words by 4 bits. The technology used to fabricate the MSM414256RS is OKI's N channel silicon gate MOS process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

FEATURES

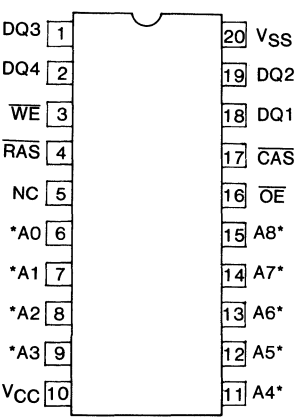
- Silicon gate, tripple polysilicon NMOS, 1-transistor memory cell
- 262,144 words by 4 bits
- Standard 20-pin plastic DIP
- Family organization

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Stand By (MAX)
MSM414256-10RS	100 ns	200 ns	413 mW	28 mW
MSM414256-12RS	120 ns	230 ns	385 mW	

- Single +5V supply, ±10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Output impedance controllable through early write and OE operations
- Page mode, read modify write capability
- CAS before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- "Gated" $\overline{CAS}$
- Built-in V_{BB} generator circuit



PIN CONFIGURATION (TOP VIEW)

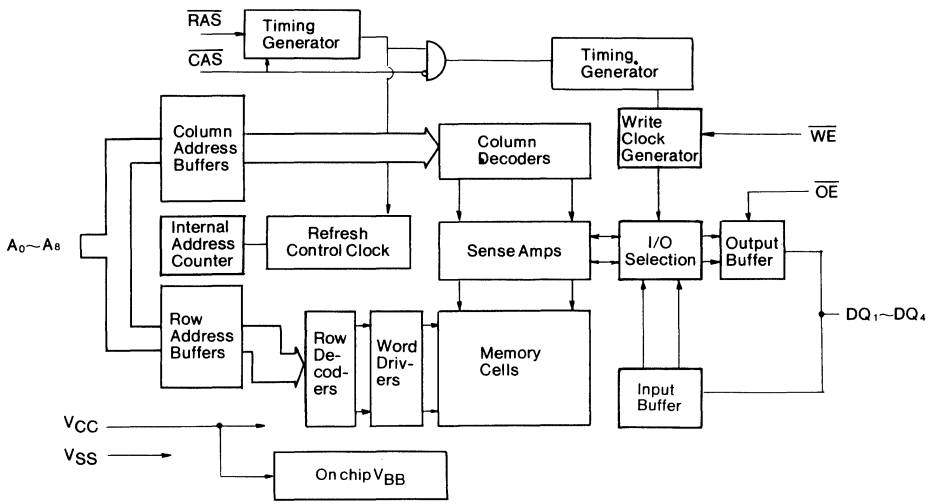


*Refresh Address

Pin Names	Function
A0 to A8	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
DQ1 to DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

9

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	VT	Ta = 25°C	−1.0 to +7.0	V
Short circuit output current	Ios	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	Topr	–	0 to +70	°C
Storage temperature	Tstg	–	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to +70°)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	–	4.5	5.0	5.5	V
	V_{SS}	–	0	0	0	V
Input high voltage	V_{IH}	–	2.4	–	6.5	V
Input low voltage	V_{IL}	–	−1.0	–	0.8	V

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions	MSM 414256-10		MSM 414256-12		Unit	Note
			MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = −5.0 mA	2.4	–	2.4	–	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA	–	−0.4	–	0.4	V	
Input leakage current	I_{LI}	0V ≦ VI ≦ 6.5V; all other pins not under test = 0V	−10	10	−10	10	μA	
Output leakage current	I_{LO}	D_{OUT} disable 0V ≦ VO ≦ 5.5V	−10	10	−10	10	μA	
Average power supply current* (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min	–	75	–	70	mA	
Power supply current* (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IH}	–	5	–	5	mA	
Average power supply current* ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} t_{RC} = min	–	65	–	60	mA	
Average power supply current* (Page mode)	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min	–	70	–	65	mA	
Average power supply current* ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC5}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$	–	70	–	65	mA	

***Note:** I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

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CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A8)	C_{IN1}	–	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	–	–	10	pF
I/O capacitance (DQ1 to DQ4)	C	–	–	7	pF

AC CHARACTERISTICS

Note 1, 2, 3 (V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	MSM414256-10		MSM414256-12		Unit	Note
		MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	–	8	–	8	ms	
Random read/write cycle time	t_{RC}	200	–	230	–	ns	
Read/write cycle time	t_{RWC}	275	–	305	–	ns	
Page mode cycle time	t_{PC}	100	–	120	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	100	–	120	ns	4, 6
Access time from $\overline{CAS}$	t_{CAC}	–	50	–	60	ns	5, 6
Output buffer turn-off delay	t_{OFF}	0	25	0	25	ns	
Transition time	t_T	3	50	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	90	–	100	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50	–	60	–	ns	
$\overline{CAS}$ precharge time (Page mode cycle only)	t_{CP}	40	–	50	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10000	60	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	–	120	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	50	25	60	ns	7, 8
$\overline{CAS}$ and $\overline{RAS}$ set-up time	t_{CRS}	15	–	20	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	20	–	20	–	ns	
Column address hold time from $\overline{RAS}$,	t_{AR}	70	–	80	–	ns	
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	10
Write command hold time from $\overline{RAS}$	t_{WCR}	80	–	95	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	9
Write command hold time	t_{WCH}	30	–	35	–	ns	

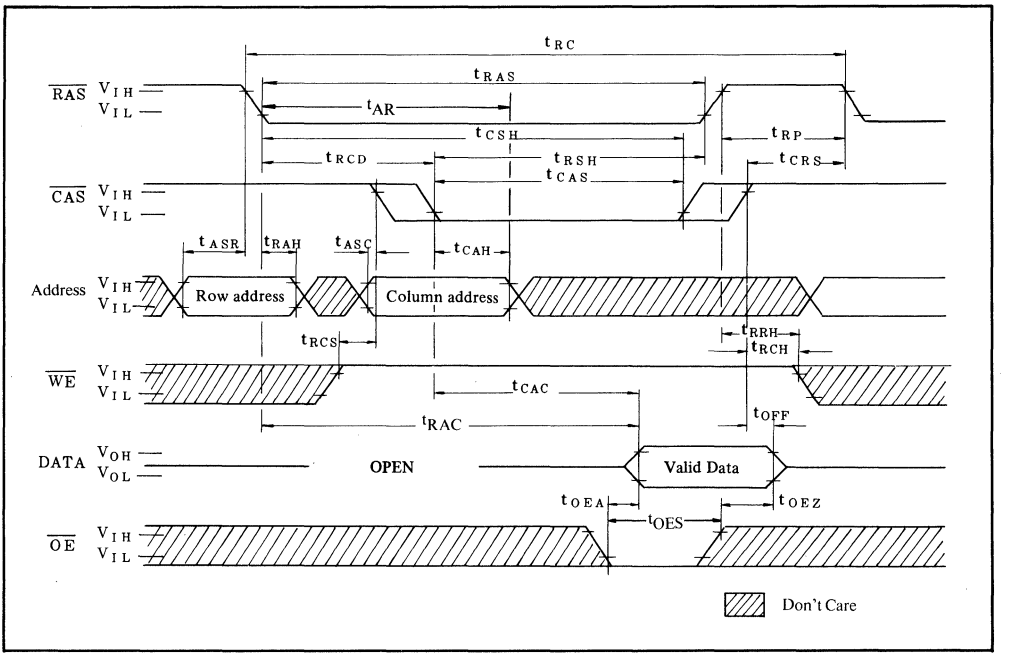
AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM414256-10		MSM414256-12		Unit	Note
		MIN	MAX	MIN	MAX		
Write command pulse width	t_{WP}	30	–	35	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40	–	40	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40	–	40	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	30	–	35	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	80	–	95	–	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	80	–	90	–	ns	9
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	130	–	150	–	ns	9
Read command hold time reference to $\overline{RAS}$	t_{RRH}	20	–	20	–	ns	10
Access time from $\overline{OE}$	t_{OEA}	–	30	–	30	ns	
$\overline{OE}$ data delay time	t_{OED}	25	–	25	–	ns	
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	ns	11
Turn-off delay time from $\overline{OE}$	t_{OEZ}	0	25	0	25	ns	
$\overline{OE}$ set-up time	t_{OES}	30	–	30	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCS}	20	–	25	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCH}	30	–	30	–	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	20	–	20	–	ns	
$\overline{CAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CPR}	20	–	25	–	ns	
Read/write cycle (Refresh counter test)	t_{RTC}	385	–	435	–	ns	11
$\overline{RAS}$ pulse width (Refresh counter test)	t_{TRAS}	285	10000	325	10000	ns	11
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	50	–	60	–	ns	11
Read/write cycle time (Page mode)	t_{PRWC}	175	–	195	–	ns	

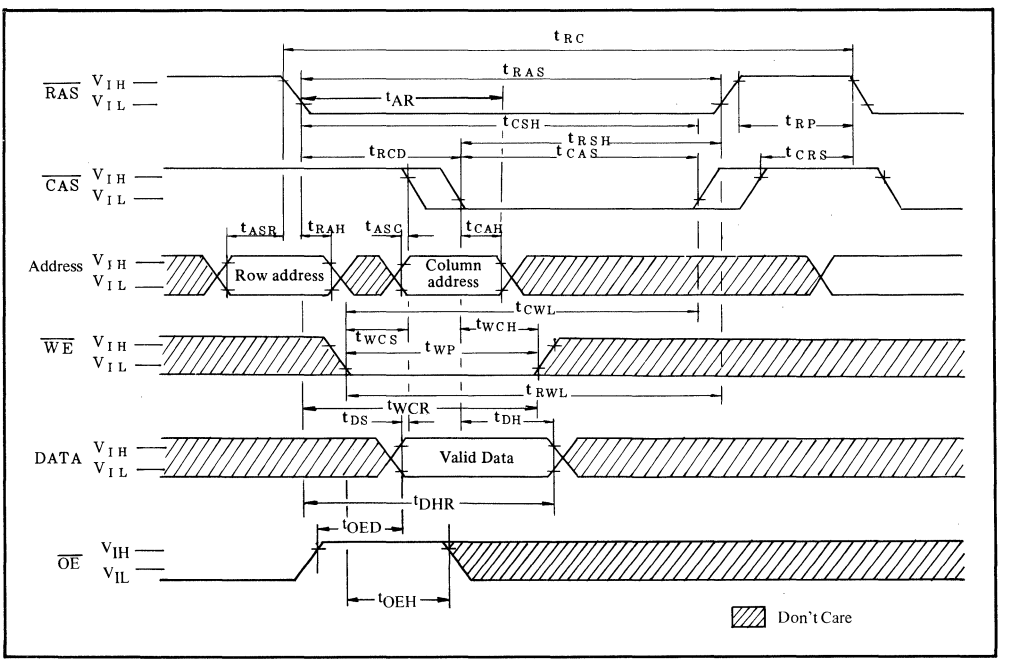
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If $t_{RCD} > t_{RCD}$ (Max.), t_{RAC} will increase by $\{t_{RCD} - t_{RCD}$ (Max.)$\}$.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL + 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. Assumes that t_{RCD} (Min.) = t_{RAH} (Min.) + $2t_T$ + t_{ASC} (Min.).
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical charcteristics only; if $t_{WCS} \geqq t_{WCS}$ (Min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (Min.) and $t_{RWD} \geqq t_{RWD}$ (Min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle only.

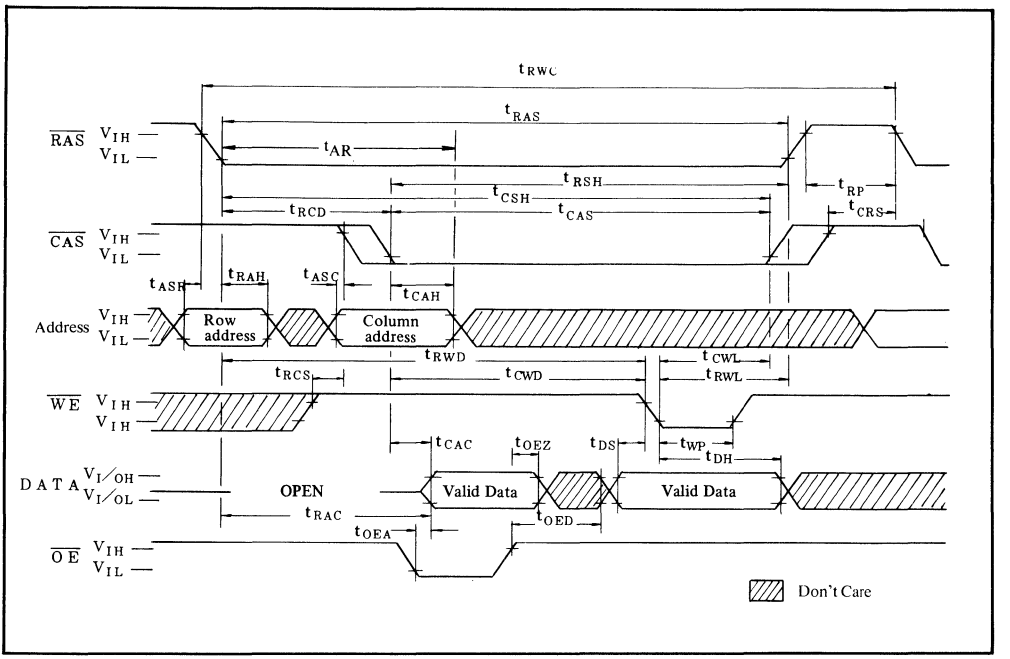
READ CYCLE



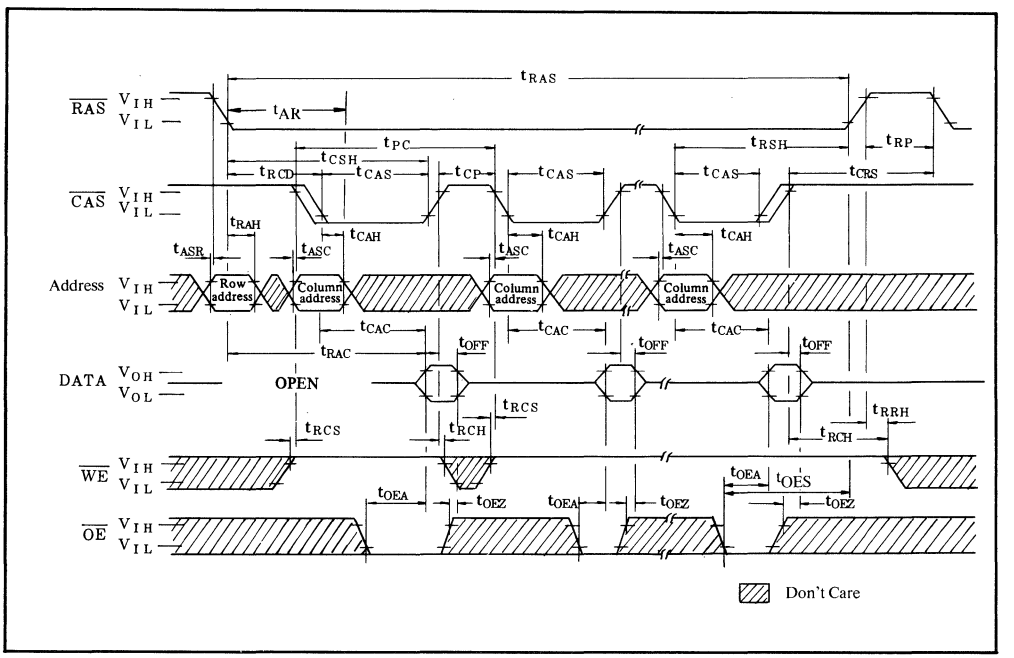
WRITE CYCLE (EARLY WRITE)



READ/WRITE AND READ MODIFY WRITE CYCLE



PAGE MODE READ CYCLE



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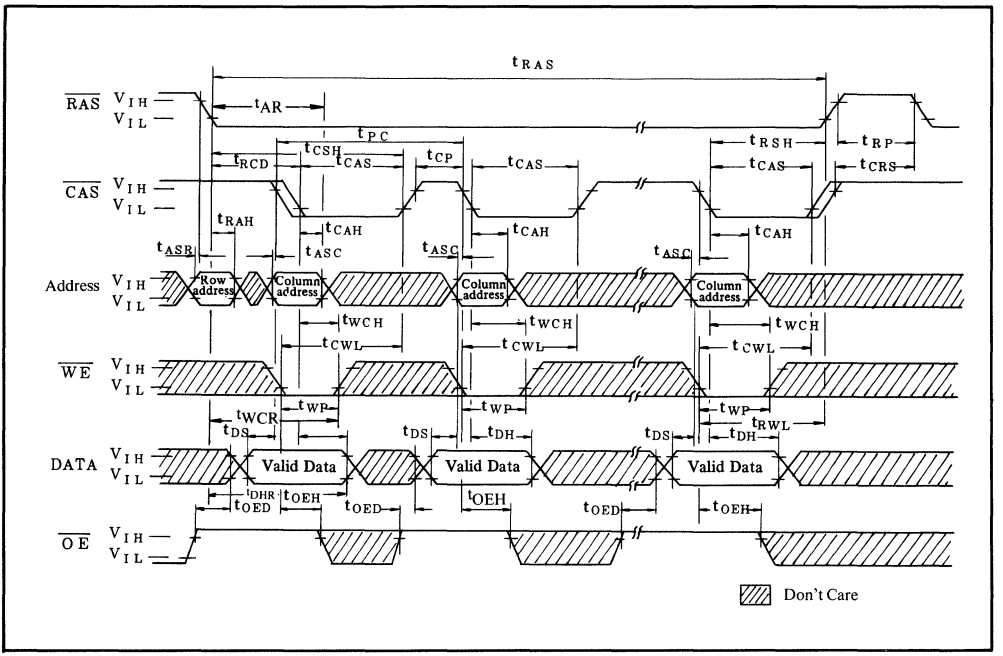
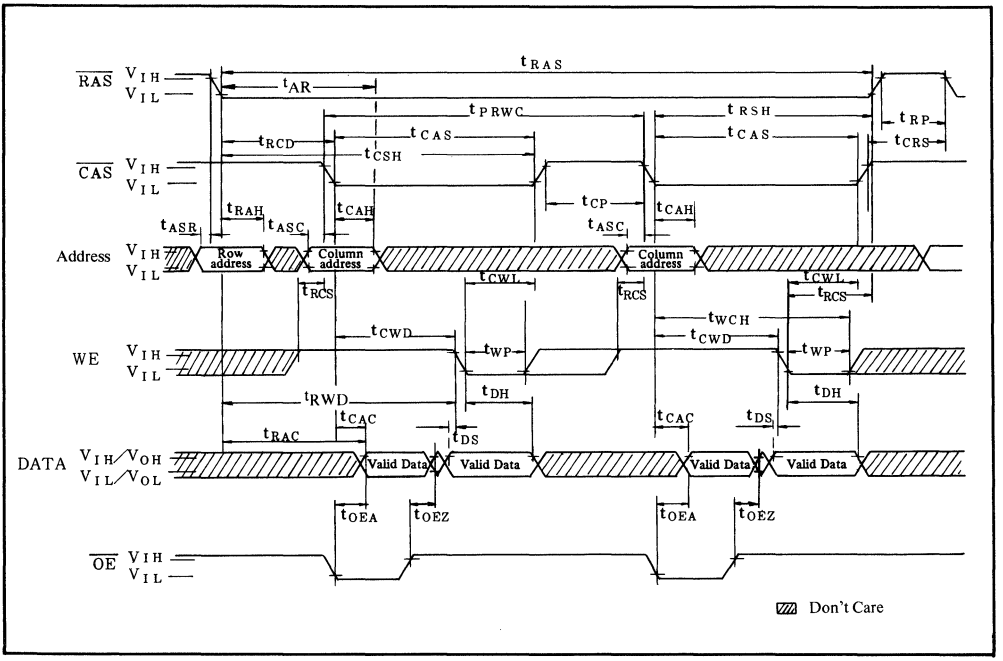
PAGE MODE WRITE CYCLE

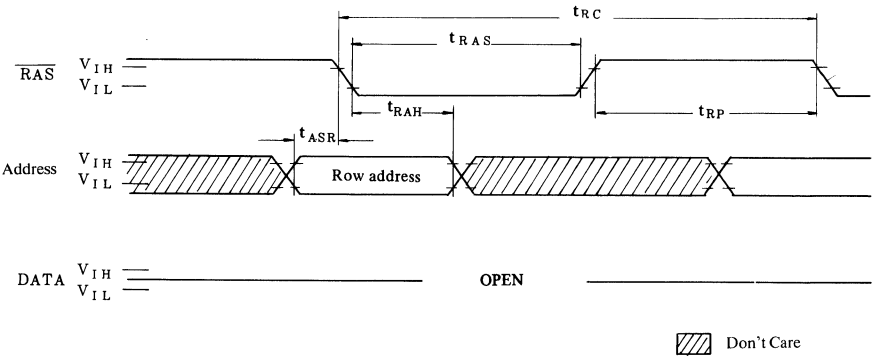


PAGE MODE READ/WRITE CYCLE



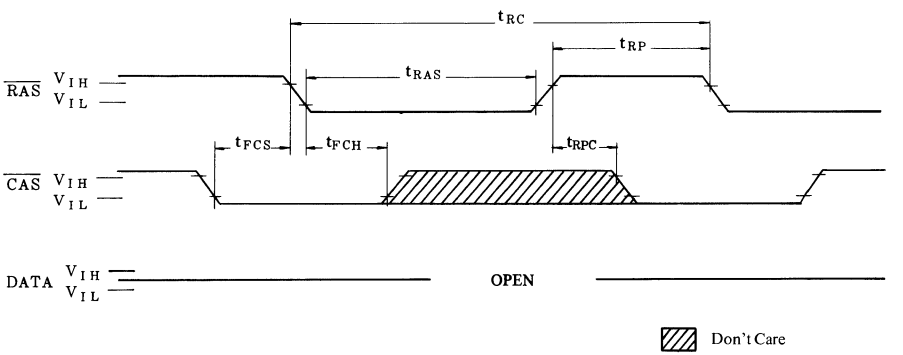
$\overline{RAS}$ ONLY REFRESH CYCLE

Note: CAS = VIH, $\overline{WE}$ and $\overline{OE}$ not dependent on the high or low level.



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

Note: $\overline{WE}$ and $\overline{OE}$ not dependent on the high or low level.



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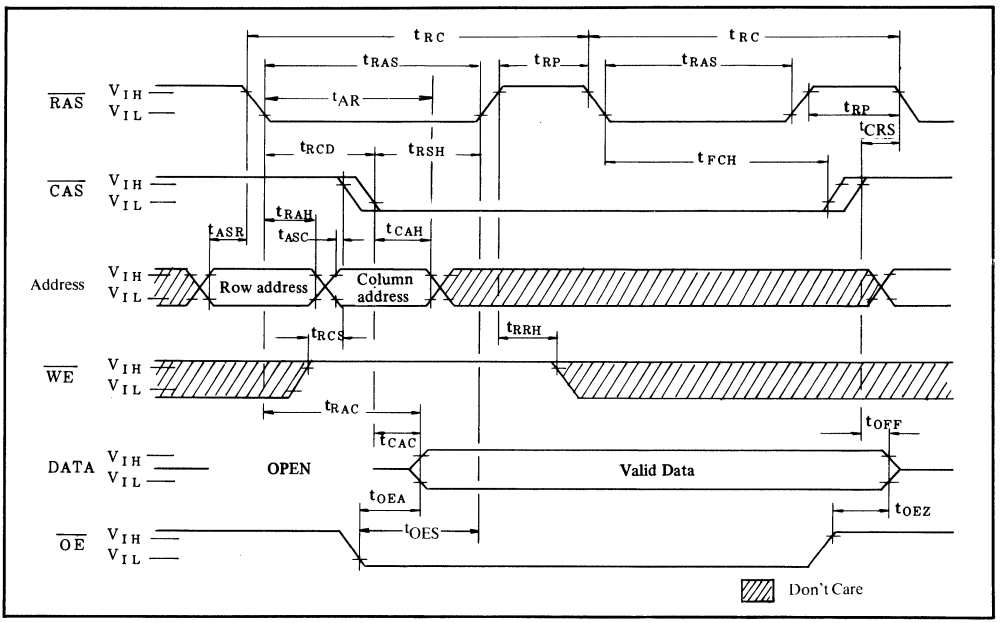
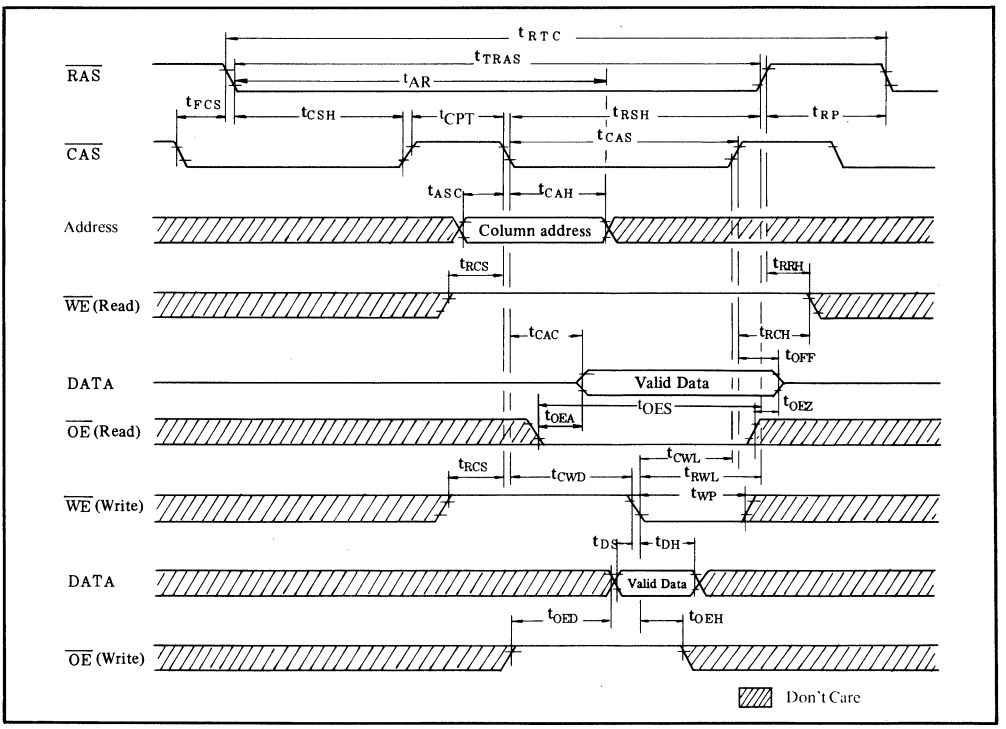
HIDDEN REFRESH CYCLE



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



FUNCTIONAL DESCRIPTION

Address Inputs:

18 bits of binary address input are required to decode any one of the 262,144 words by 4 bits storage cell locations.

9 row-address bits are set up on address input pins A0 through A8 and latched onto the chip by the row address strobe ($\overline{RAS}$). Then 9 column-address bits are set up on pins A0 through A8 and latched onto the chip by the column address strobe ($\overline{CAS}$).

All addresses must be stable on or before the falling edges of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (gated) by the $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Therefore specifications permit column addresses to be input immediately after the row address hold time (t_{RAH}).

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. The logic high of the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The data input is disabled when the read mode is selected. Data-out will remain in the high-impedance state allowing a write cycle with $\overline{WE}$ grounded.

Data Input:

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latches. In an early-write cycle, $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{WE}$ with setup and hold times referenced to this signal. In delayed or read-modify-write, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

Data Output:

The three-state output buffer provides direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} and t_{OEA} are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ is low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the output is always in the high impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfy t_{OED}.

Output Enable:

The $\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low impedance state. Once in the low impedance state, they will remain in the low impedance state until $\overline{CAS}$ or $\overline{OE}$ is brought high.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 512 row-addresses (A_0 to A_8) at least every eight milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 512 (A_0 to A_8) row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

$\overline{CAS}$ before $\overline{RAS}$ refreshing offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. Hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle:

A special timing sequence using $\overline{CAS}$ before $\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$ before $\overline{RAS}$ refresh activated circuitry. As shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. This is shown in the $\overline{CAS}$ before $\overline{RAS}$ counter test cycle. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be acceded can be defined as follows:

* A ROW ADDRESS
  - Bits A_0 through A_8 are defined by the refresh counter.
* A COLUMN ADDRESS
  - All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$ before $\overline{RAS}$ Counter Test Procedure:

The timing, as shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, is used for all the operations described as follows:

(1) Initialize the internal refresh counter. For this operaton, 8 cycles are required.
(2) Write a test pattern of lows into memory cells at a single column address and 512 row addresses.
(3) By using read-modify-write cycle, read the low written at the last operation (Step (2)) and write a new high in the same cycle. This cycle is repeated 512 times, and highs are written into the 512 memory cells.
(4) Read the high written at the last operation (Step (3)).
(5) Complement the test pattern and repeat the steps (2), (3) and (4).

Preliminary

MSM411000RS

1,048,576-WORD × 1-BITS DYNAMIC RAM

GENERAL DESCRIPTION

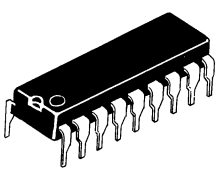
The MSM411000RS is a new generation dynamic RAM organized as 1,048,576 words by 1 bit. The technology used to fabricate the MSM411000RS is OKI's N channel silicon gate MOS process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

FEATURES

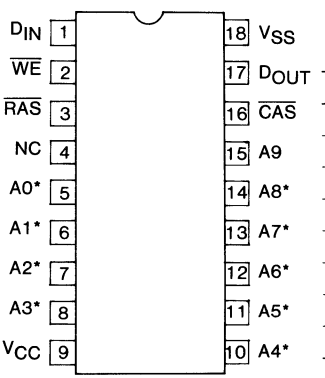
- Silicon gate, tripple polysilicon NMOS, 1-transistor memory cell
- 1,048,576 words by 1 bit
- Standard 18-pin plastic DIP
- Family organization

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Stand By (MAX)
MSM411000-10RS	100 ns	200 ns	413 mW	28 mW
MSM411000-12RS	120 ns	230 ns	385 mW	

- Single +5V supply, ±10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Common I/O capability using "Early Write" operation
- Page mode, read modify write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- "Gated" $\overline{CAS}$
- Built-in V_{BB} generator circuit



PIN CONFIGURATION (TOP VIEW)



* Refresh Address

Pin Names	Function
A0 to A9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

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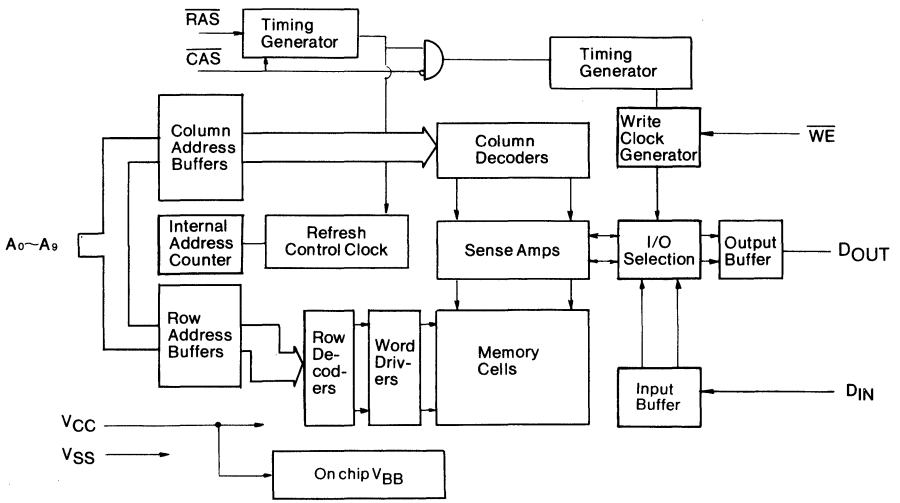
FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	VT	Ta = 25°C	−1.0 to +7.0	V
Short circuit output current	Ios	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	Topr	–	0 to +70	°C
Storage temperature	Tstg	–	−55 to +150	°C

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RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to +70°)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	–	4.5	5.0	5.5	V
	V_{SS}	–	0	0	0	V
Input high voltage	V_{IH}	–	2.4	–	6.5	V
Input low voltage	V_{IL}	–	−1.0	–	0.8	V

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions	MSM 411000-10		MSM 411000-12		Unit	Note
			MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = −5.0 mA	2.4	–	2.4	–	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA	–	0.4	–	0.4	V	
Input leakage current	I_{LI}	0V ≦ VI ≦ 6.5V; all other pins not under test = 0V	−10	10	−10	10	μA	
Output leakage current	I_{LO}	D_{OUT} disable 0V ≦ VO ≦ 5.5V	−10	10	−10	10	μA	
Average power supply current* (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min	–	75	–	70	mA	
Power supply current* (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IH}	–	5	–	5	mA	
Average power supply current* ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} t_{RC} = min	–	65	–	60	mA	
Average power supply current* (Page mode)	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min	–	70	–	65	mA	
Average power supply current* ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC5}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$	–	70	–	65	mA	

***Note:** I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A9, D_{IN})	C_{IN1}	–	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	–	–	10	pF
Output capacitance (D_{OUT})	C_{OUT}	–	–	7	pF

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AC CHARACTERISTICS

Note 1, 2, 3 (V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	MSM411000-10		MSM411000-12		Unit	Note
		MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	–	8	–	8	ms	
Random read/write cycle time	t_{RC}	200	–	230	–	ns	
Read/write cycle time	t_{RWC}	235	–	255	–	ns	
Page mode cycle time	t_{PC}	100	–	120	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	100	–	120	ns	4, 6
Access time from $\overline{CAS}$	t_{CAC}	–	50	–	60	ns	5, 6
Output buffer turn-off delay	t_{OFF}	0	25	0	25	ns	
Transition time	t_T	3	50	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	90	–	100	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50	–	60	–	ns	
$\overline{CAS}$ precharge time (Page mode cycle only)	t_{CP}	40	–	50	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10000	60	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	–	120	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	50	25	60	ns	7, 8
$\overline{CAS}$ and $\overline{RAS}$ set-up time	t_{CRS}	15	–	20	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	20	–	20	–	ns	
Column address hold time from $\overline{RAS}$,	t_{AR}	70	–	80	–	ns	
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	10
Write command hold time from $\overline{RAS}$	t_{WCR}	80	–	95	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	9
Write command hold time	t_{WCH}	30	–	35	–	ns	

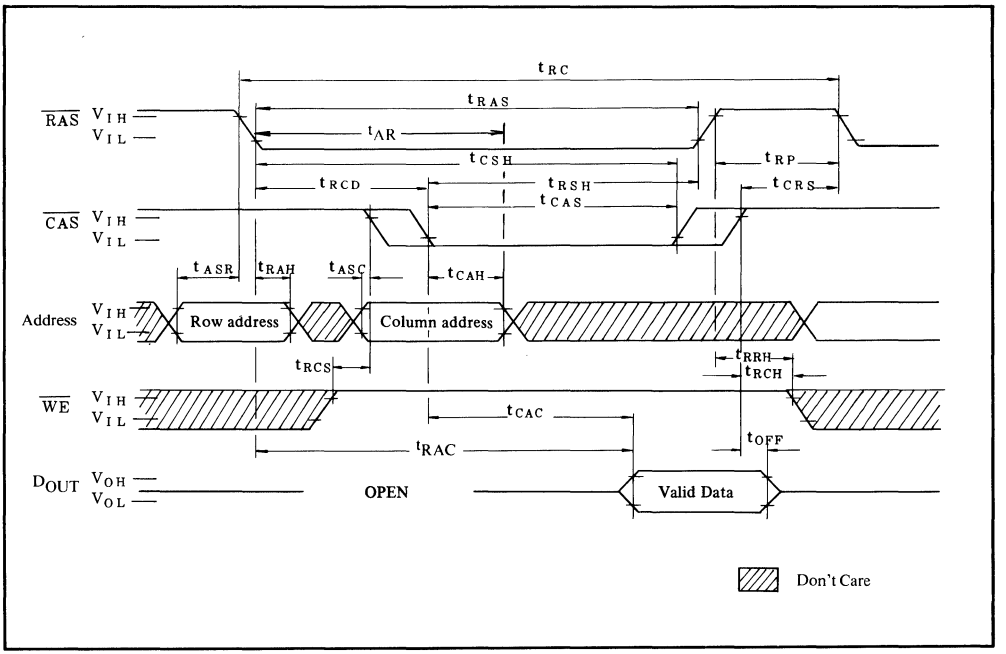
AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM411000-10		MSM411000-12		Unit	Note
		MIN	MAX	MIN	MAX		
Write command pulse width	t_{WP}	30	–	35	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40	–	40	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40	–	40	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	30	–	35	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	80	–	95	–	ns	
CAS to $\overline{WE}$ delay	t_{CWD}	40	–	40	–	ns	9
RAS to $\overline{WE}$ delay	t_{RWD}	90	–	100	–	ns	9
Read command hold time reference to $\overline{RAS}$	t_{RRH}	20	–	20	–	ns	10
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCS}	20	–	25	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCH}	30	–	30	–	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	20	–	20	–	ns	
$\overline{CAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CPR}	20	–	25	–	ns	
Read/write cycle (Refresh counter test)	t_{RTC}	355	–	385	–	ns	11
$\overline{RAS}$ pulse width (Refresh counter test)	t_{TRAS}	255	10000	275	10000	ns	11
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	50	–	60	–	ns	11
Read/write cycle time (Page mode)	t_{PRWC}	135	–	145	–	ns	

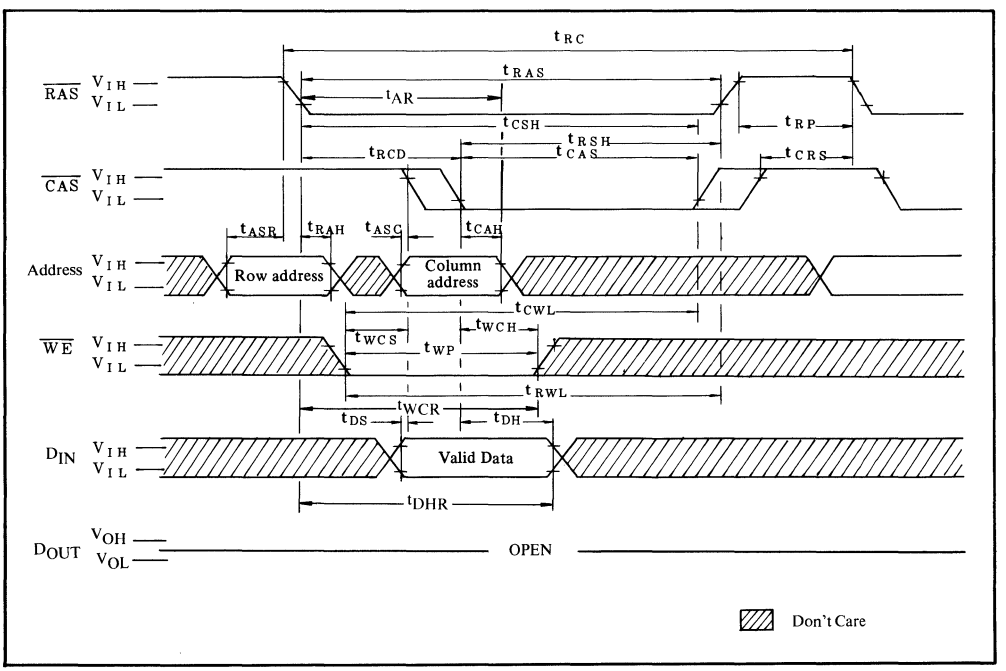
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If $t_{RCD} > t_{RCD}$ (Max.), t_{RAC} will increase by $\{t_{RCD} - t_{RCD}$ (Max.)$\}$.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL + 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. Assumes that t_{RCD} (Min.) = t_{RAH} (Min.) + $2t_T$ + t_{ASC} (Min.).
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical charcteristics only; if $t_{WCS} \geqq t_{WCS}$ (Min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (Min.) and $t_{RWD} \geqq t_{RWD}$ (Min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle only.

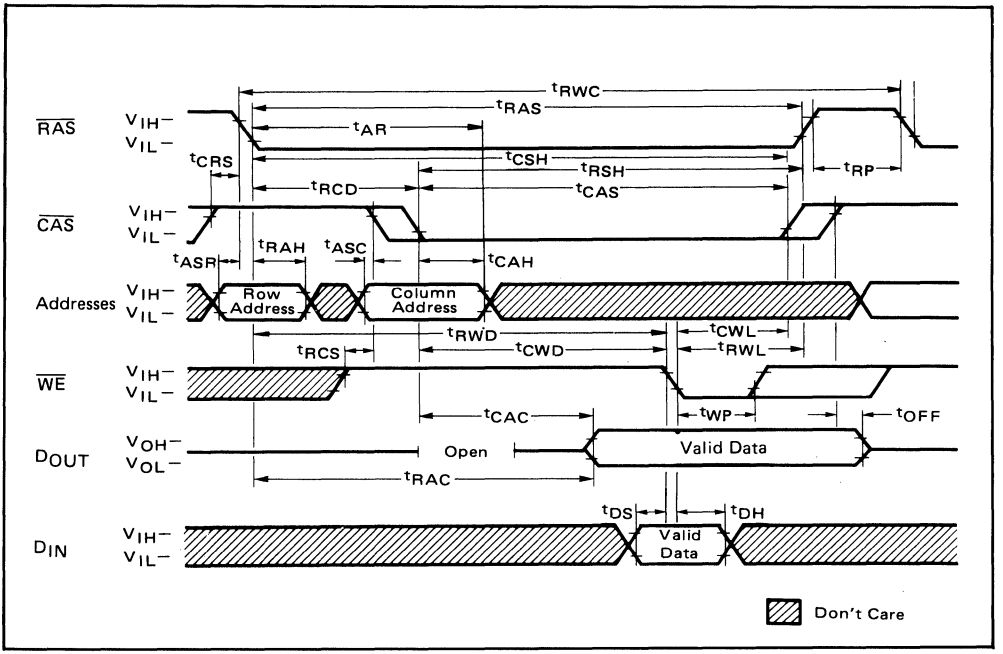
READ CYCLE



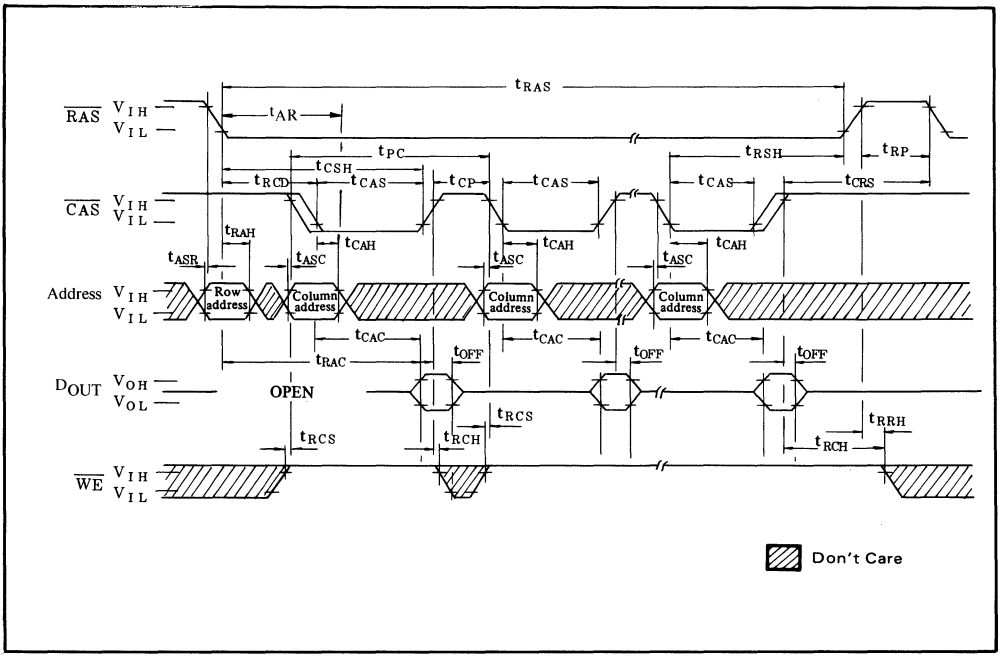
WRITE CYCLE (EARLY WRITE)



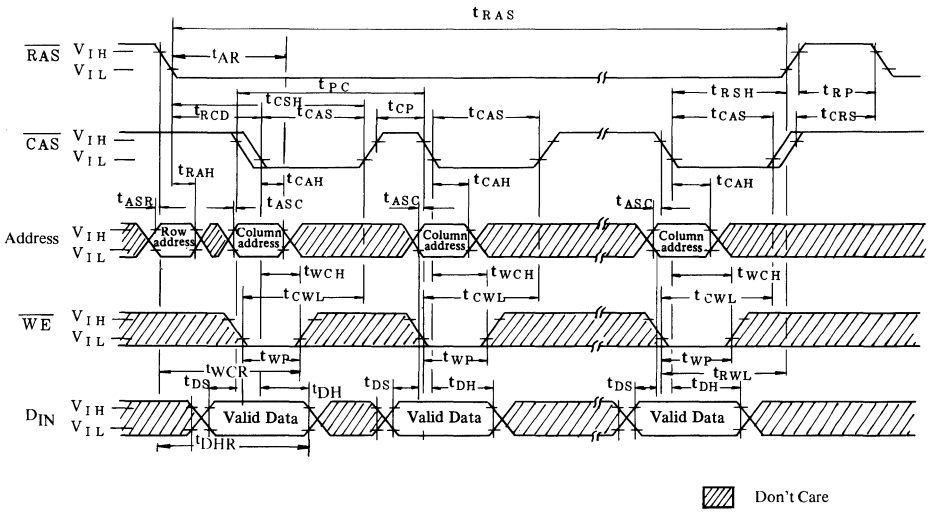
READ/WRITE AND READ MODIFY WRITE CYCLE



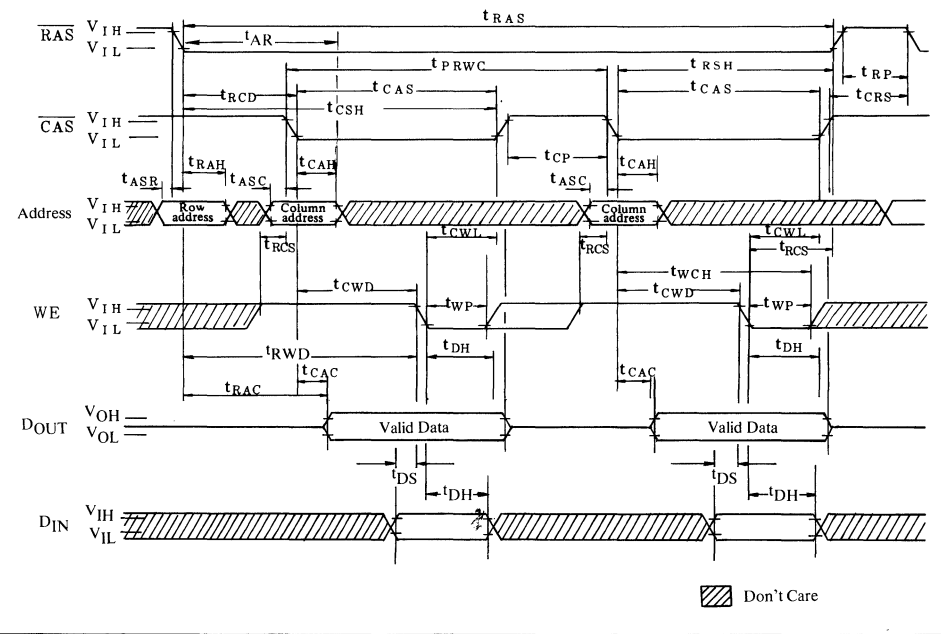
PAGE MODE READ CYCLE



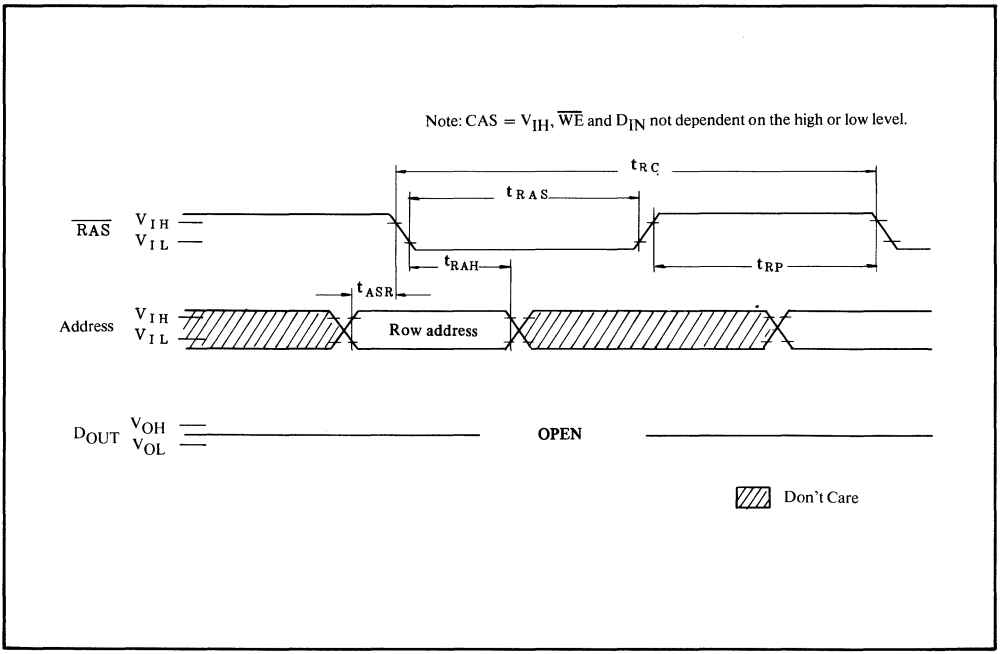
PAGE MODE WRITE CYCLE



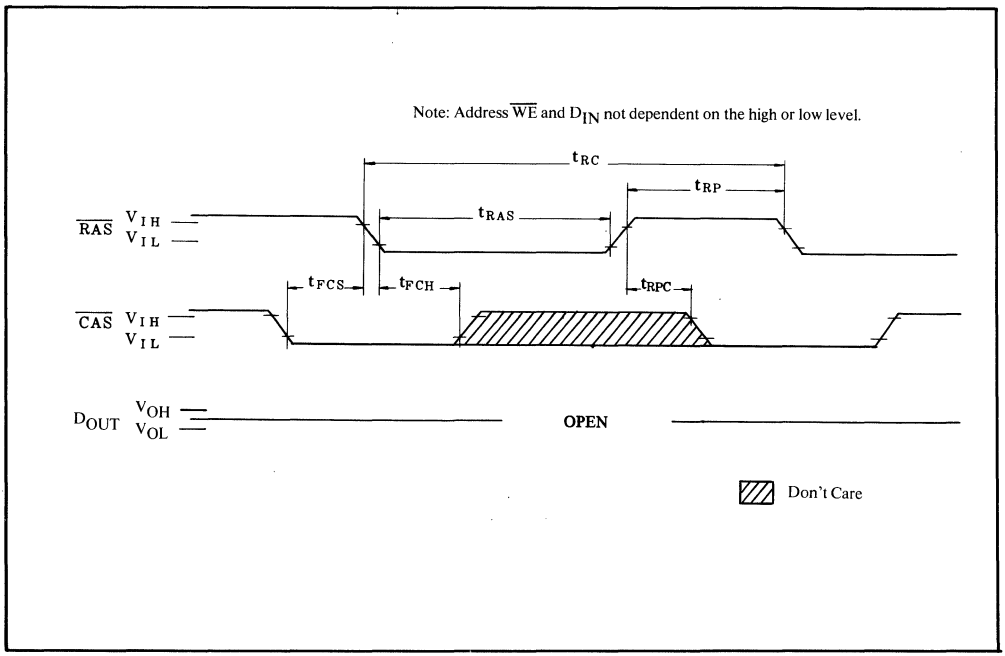
PAGE MODE READ/WRITE CYCLE



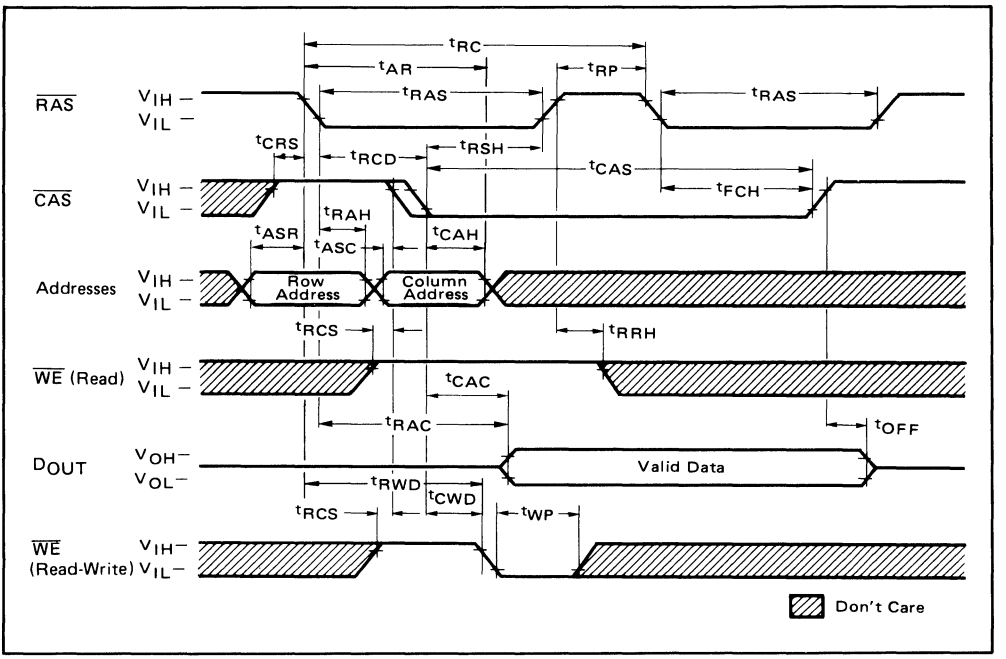
$\overline{RAS}$ ONLY REFRESH CYCLE



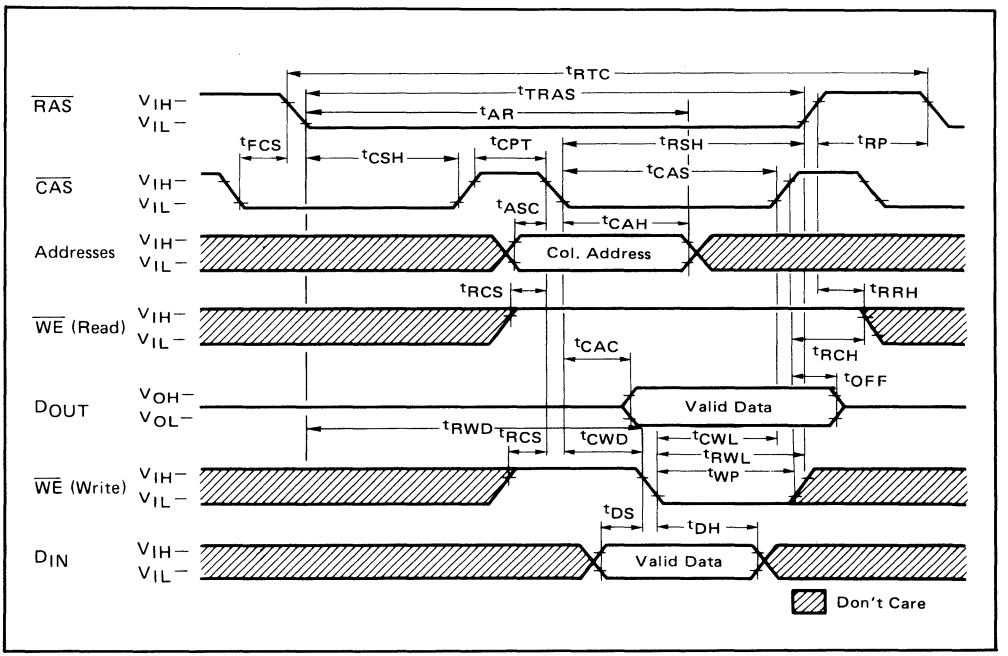
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



FUNCTIONAL DESCRIPTION

Address Inputs:

20 bits of binary address input are required to decode any one of the 1,048,576 words by 1 bit storage cell locations.

10 row-address bits are set up on address input pins A0 through A9 and latched onto the chip by the row address strobe ($\overline{RAS}$). Then 10 column-address bits are set up on pins A0 through A9 and latched onto the chip by the column address strobe ($\overline{CAS}$).

All addresses must be stable on or before the falling edges of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (gated) by the $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Therefore specifications permit column addresses to be input immediately after the row address hold time (t_{RAH}).

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. The logic high of the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The data input is disabled when the read mode is selected.

Data Input:

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latches. In an early-write cycle, $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{WE}$ with setup and hold times referenced to this signal.

Data Output:

The three-state output buffer provides direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low. $\overline{CAS}$ going high returns it to a high impedance state. In an early-write cycle, the output is always in the high impedance state.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 512 row-addresses (A_0 to A_8) at least every 8 milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 512 (A_0 to A_8) row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

$\overline{CAS}$ before $\overline{RAS}$ refreshing offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. Hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle:

A special timing sequence using $\overline{CAS}$ before $\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$ before $\overline{RAS}$ refresh activated circuitry. As shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. This is shown in the $\overline{CAS}$ before $\overline{RAS}$ counter test cycle. A memory cell address, consisting of a row address (9 bits) and a column address (10 bits), to be acceded can be defined as follows:

* A ROW ADDRESS
  - Bits A_0 through A_8 are defined by the refresh counter.
* A COLUMN ADDRESS
  - All the bits A_0 through A_9 are defined by latching levels on A_0 through A_9 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$ before $\overline{RAS}$ Counter Test Procedure:

The timing, as shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, is used for all the operations described as follows:

(1) Initialize the internal refresh counter. For this operaton, 8 cycles are required.

(2) Write a test pattern of lows into memory cells at a single column address and 512 row addresses.

(3) By using read-modify-write cycle, read the low written at the last operation (Step (2)) and write a new high in the same cycle. This cycle is repeated 512 times, and highs are written into the 512 memory cells.

(4) Read the high written at the last operation (Step (3)).

(5) Complement the test pattern and repeat the steps (2), (3) and (4).

Preliminary

MSM411001RS

1048576-BIT DYNAMIC RANDOM ACCESS MEMORY < Nibble Mode Type >

GENERAL DESCRIPTION

The Oki MSM411001 is a fully decoded, dynamic NMOS random access memory organized as 1048576 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MSM411001 to be housed in a standard 18 pin DIP. Pin-outs conform to the JEDEC approved pin out. Additionally, the MSM411001 offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability, also features "nibble mode" which allows high speed serial access to up to 4 bits of data.

The MSM411001 is fabricated using silicon gate NMOS and Oki's advanced VLSI Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

- 1048576 x 1 RAM, 18 pin package
- Silicon-gate, Tripple Poly NMOS, single transistor cell
- Row access time
  100 ns max (MSM411001-10RS)
  120 ns max (MSM411001-12RS)
- Cycle time
  200 ns min (MSM411001-10RS)
  230 ns min (MSM411001-12RS)
- Low power: 411001-12RS
  413 mW/28 mW (MSM411001-10RS)
  385 mW/28 mW (MSM411001-12RS)
- Single+5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- Gated $\overline{CAS}$
- 8ms/512 refresh cycles
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- "Nibble Mode" capability

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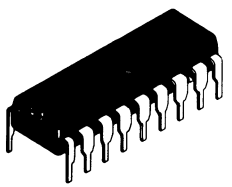
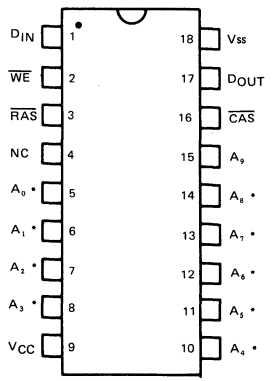


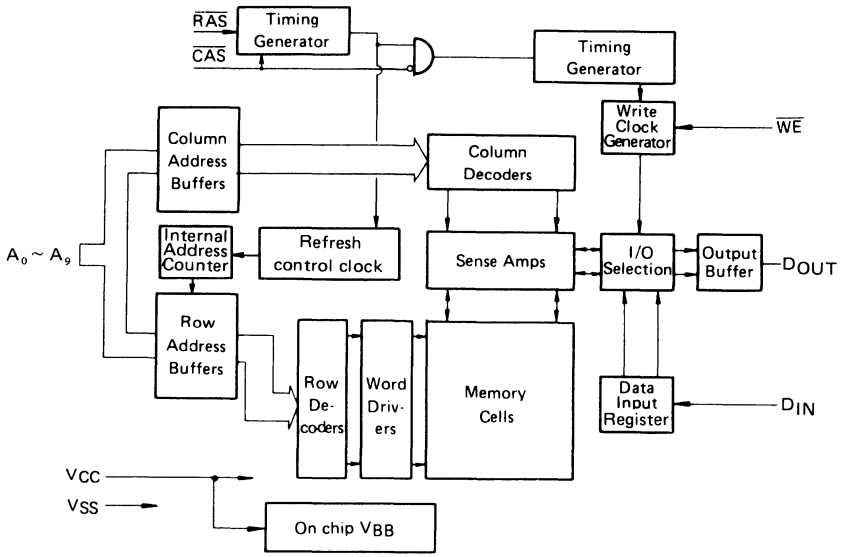
PIN CONFIGURATION



Pin Names	Function
$A_0 \sim A_9$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground (0V)

* Refresh Address

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MSM411001-10		MSM411001-12		Unit	Notes
		Min	Max	Min	Max		
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}	–	75	–	70	mA	
STANDBY CURRENT* Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	5	–	5	mA	
REFRESH CURRENT 1* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}	–	65	–	60	mA	
Nibble MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{NC} = min.)	I_{CC4}	–	70	–	65	mA	
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = min.)	I_{CC5}	–	70	–	65	mA	
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	-10	10	-10	10	μA	
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	-10	10	-10	10	μA	
OUTPUT LEVELS Output high voltage (I_{OH} = -5 mA)	V_{OH}	2.4	–	2.4	–	V	
Output low voltage (I_{OL} = 4.2 mA)	V_{OL}	–	0.4	–	0.4	V	

Note*: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A_0 ~ A_9, D_{IN})	C_{IN1}	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	—	10	pF
Output Capacitance (D_{OUT})	C_{OUT}	—	7	pF

Capacitance measured with Boonton Meter.

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AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noded.)

Parameter	Symbol	Unit	MSM411001 10		MSM411001 12		Notes
			Min	Max	Min	Max	
Refresh period	t_{REF}	ms		8		8	
Random read or write cycle time	t_{RC}	ns	200		230		
Read-write cycle time	t_{RWC}	ns	235		255		
Access time from $\overline{RAS}$	t_{RAC}	ns		100		120	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		50		60	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	25	0	25	
Transition time	t_T	ns	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	100	10 μs	120	10 μs	
$\overline{RAS}$ hold time	t_{RSH}	ns	50		60		
$\overline{CAS}$ pulse width	t_{CAS}	ns	50	10 μs	60	10 μs	
$\overline{CAS}$ hold time	t_{CSH}	ns	100		120		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	50	25	60	7
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	ns	15		20		
Row address set-up time	t_{ASR}	ns	0		0		
Row address hold time	t_{RAH}	ns	15		15		
Column address set-up time	t_{ASC}	ns	0		0		
Column address hold time	t_{CAH}	ns	20		20		
Column address hold time from $\overline{RAS}$	t_{AR}	ns	70		80		
Read command set-up time	t_{RCS}	ns	0		0		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	ns	0		0		
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	20		20		
Write command hold time from $\overline{RAS}$	t_{WCR}	ns	80		95[1]		
Write command set-up time	t_{WCS}	ns	0		0		8
Write command pulse width	t_{WP}	ns	30		35		
Write command hold time	t_{WCH}	ns	30		35		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	40		40		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	40		40		
Data-in set-up time	t_{DS}	ns	0		0		
Data-in hold time	t_{DH}	ns	30		35		
Data-in hold time from $\overline{RAS}$	t_{DHR}	ns	80		95		
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	ns	40		40		8
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	ns	90		100		
Refresh set-up time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCS}	ns	20		25		
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCH}	ns	30		30		
$\overline{CAS}$ precharge time (C before R cycle)	t_{CPR}	ns	20		25		
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	ns	20		20		
Nibble mode read/write cycle time	t_{NC}	ns	65		70		9
Nibble mode read-write cycle time	t_{NRWC}	ns	65		70		9
Nibble mode access time	t_{NCAC}	ns		30		35	9
Nibble mode $\overline{CAS}$ pulse width	t_{NCAS}	ns	30		35		9

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Unit	MSM411001 10		MSM411001 12		Notes
			Min	Max	Min	Max	
Nibble mode CAS precharge time	t_{NCP}	ns	25		25		9
Nibble mode read RAS hold time	t_{NRRSH}	ns	40		40		9
Nibble mode write RAS hold time	t_{NWRSH}	ns	40		40		9
Nibble mode $\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{RNH}	ns	20		20		9
Refresh counter test cycle time	t_{RTC}	ns	355		385		10
Refresh counter test RAS pulse width	t_{TRAS}	ns	255	10,000	275	10,000	10
Refresh counter test CAS precharge time	t_{CPT}	ns	50		60		10

NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Examples; $\overline{RAS}$ only) before proper device operation is achieved.

2) AC measurements assume t_T = 5 ns.

3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

4) Assumes that $t_{RCD} \leqq t_{RCD}$ (max.).
If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.

5) Assumes that $t_{RCD} \geqq t_{RCD}$ (max.)

6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.

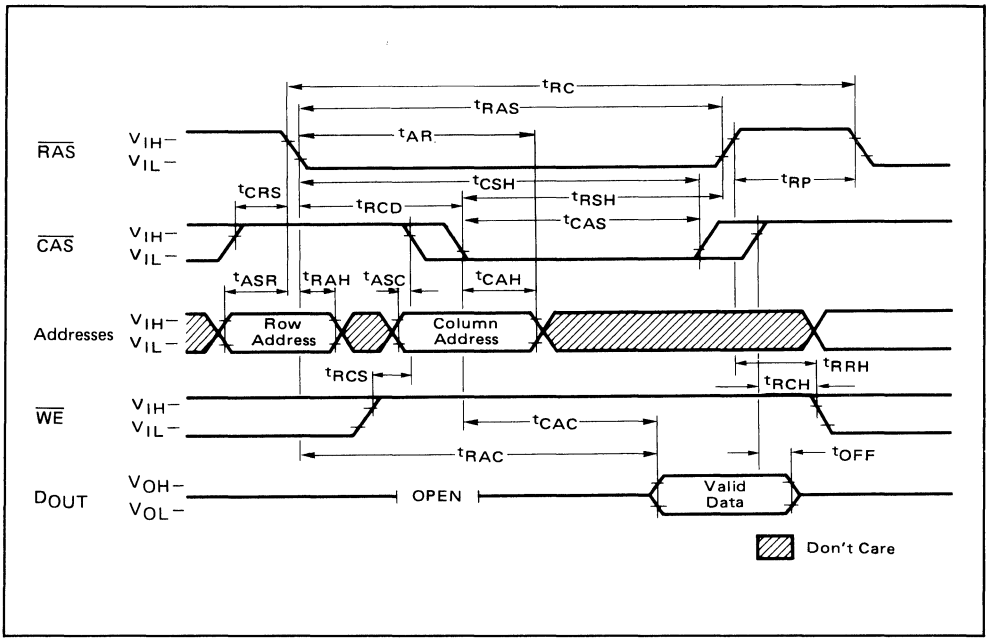
7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data dheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$(min.), and $t_{RWD} \geq t_{RWD}$ (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at acccess time) is indeterminate.

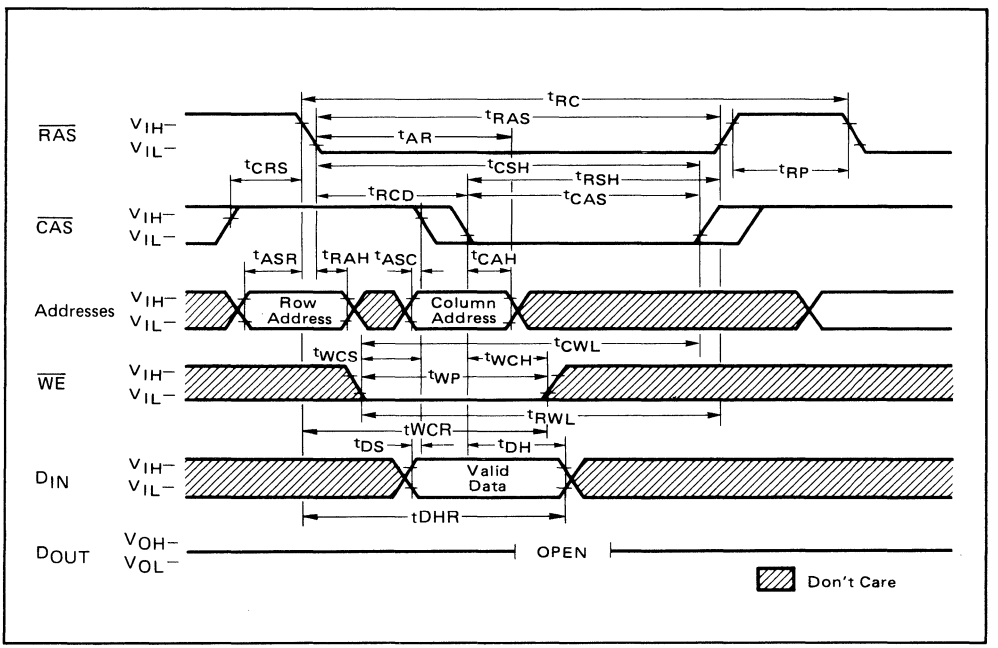
9) Nibble mode cycle.

10) $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Cycle only.

READ CYCLE



WRITE CYCLE (EARLY WRITE)



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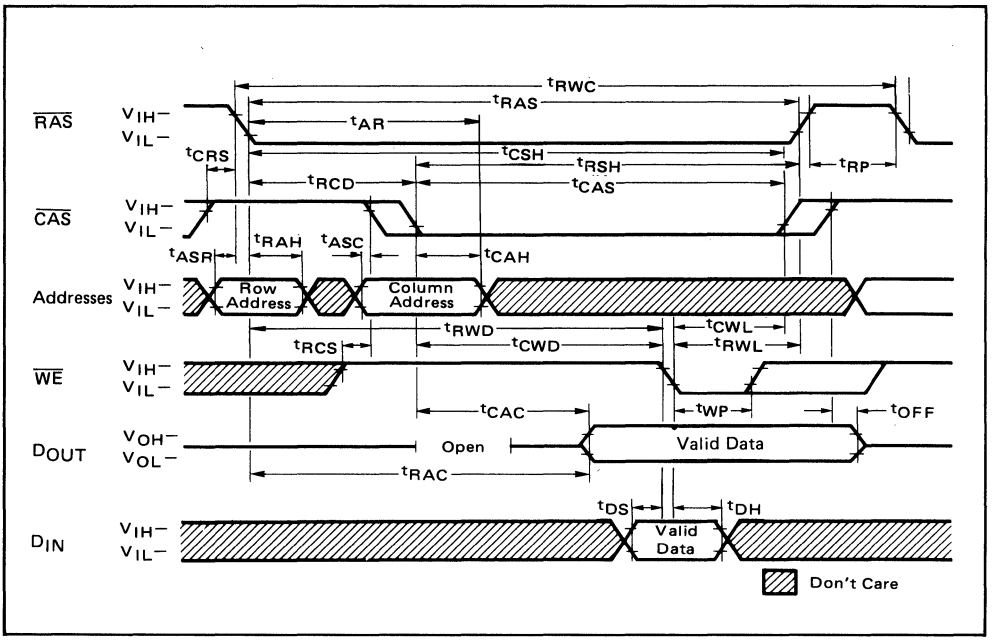
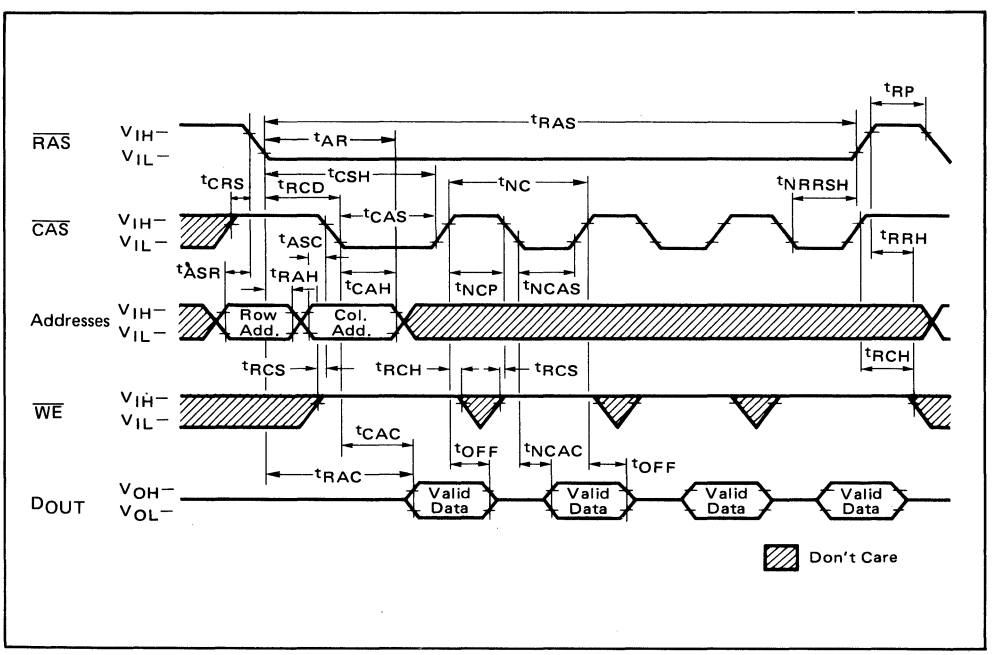
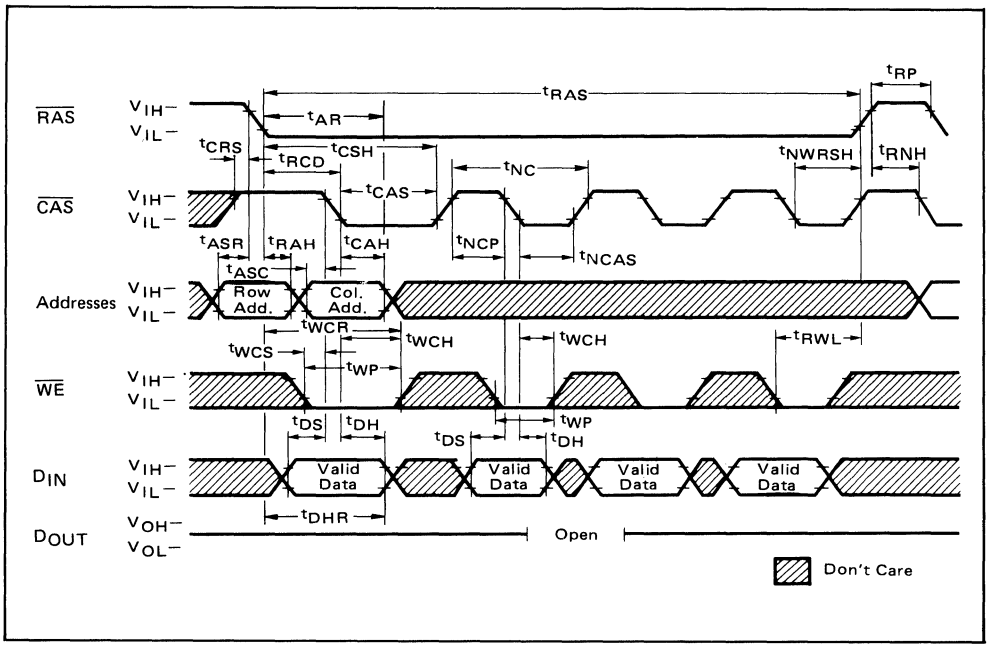
READ-WRITE/READ-MODIFY-WRITE CYCLE



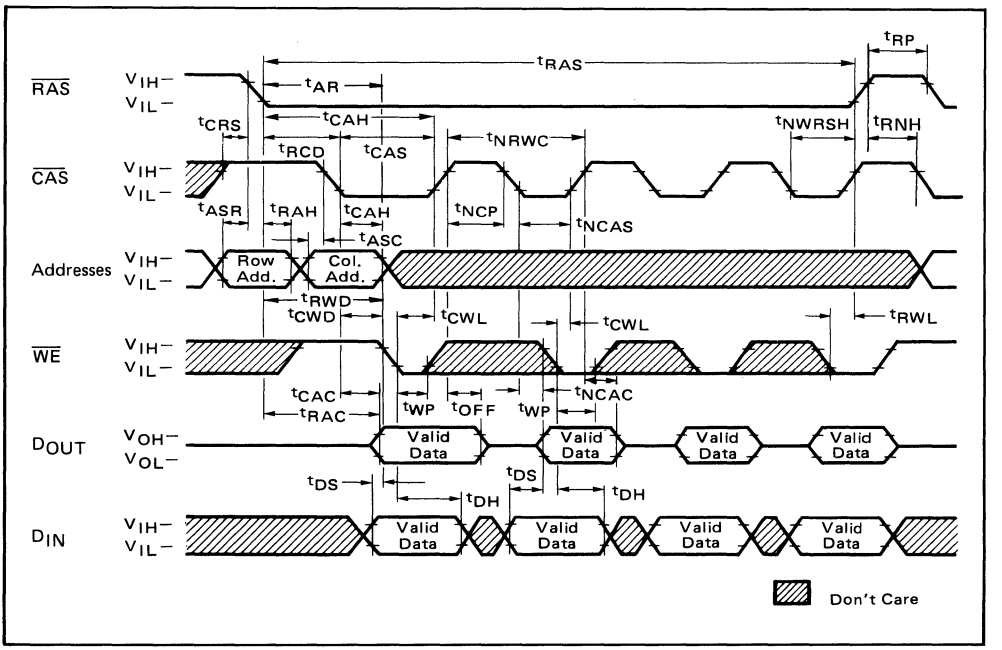
NIBBLE MODE READ CYCLE



NIBBLE MODE WRITE CYCLE



NIBBLE MODE READ-WRITE CYCLE



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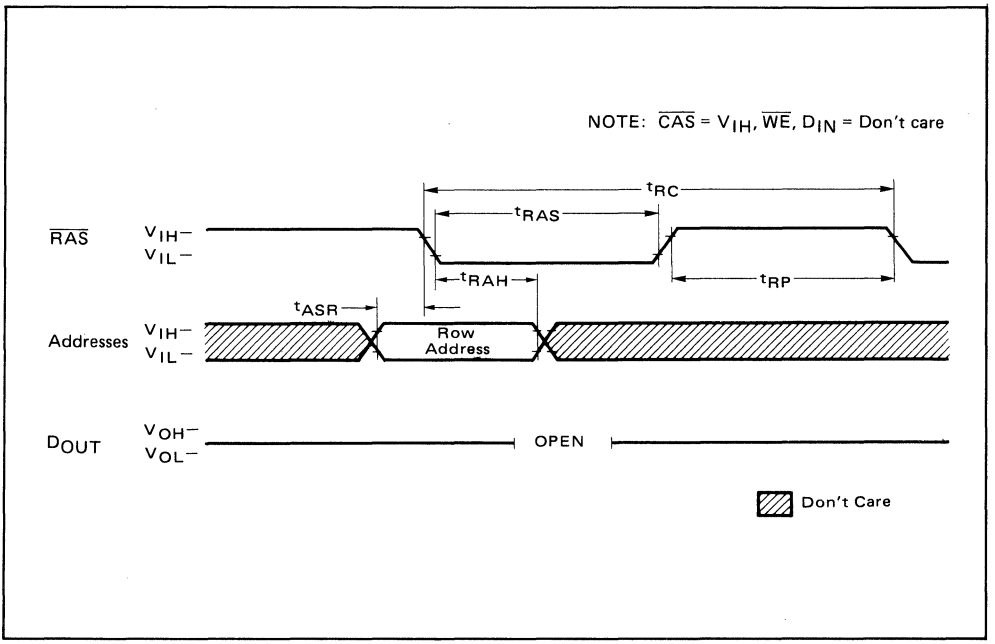
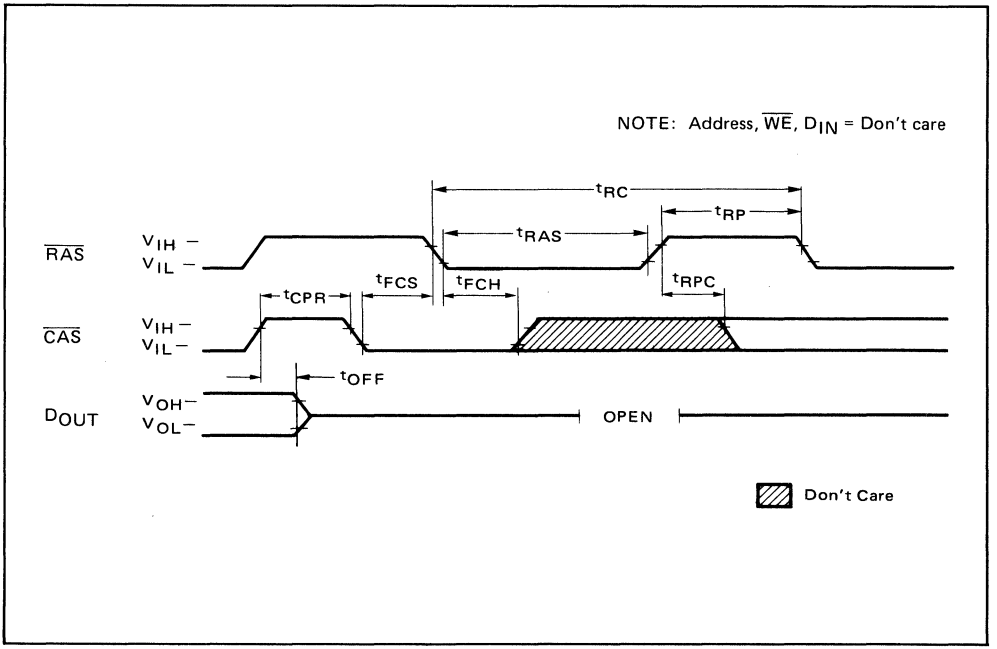
$\overline{RAS}$ ONLY REFRESH CYCLE



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



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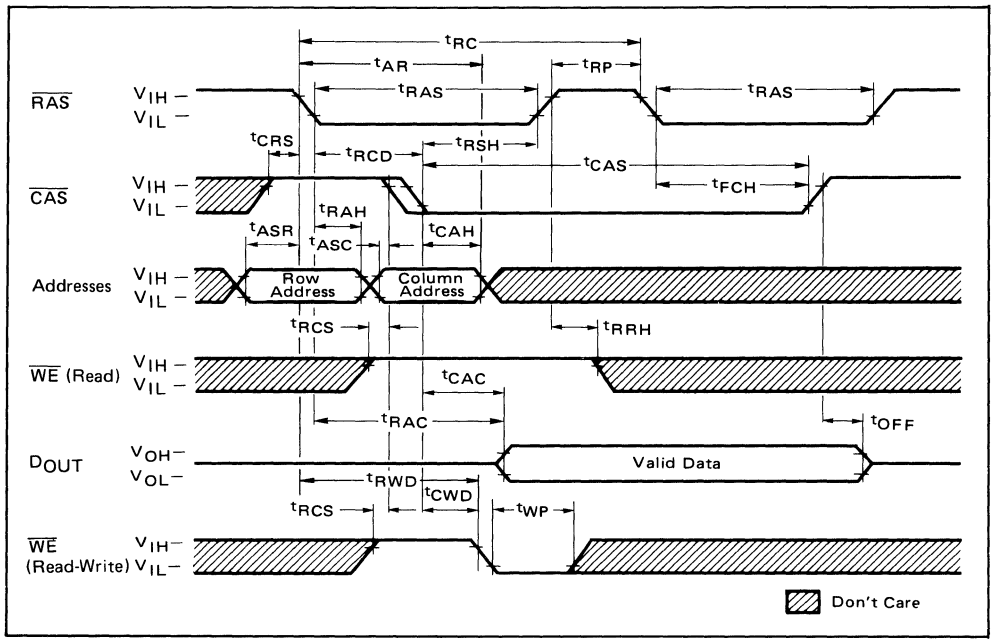
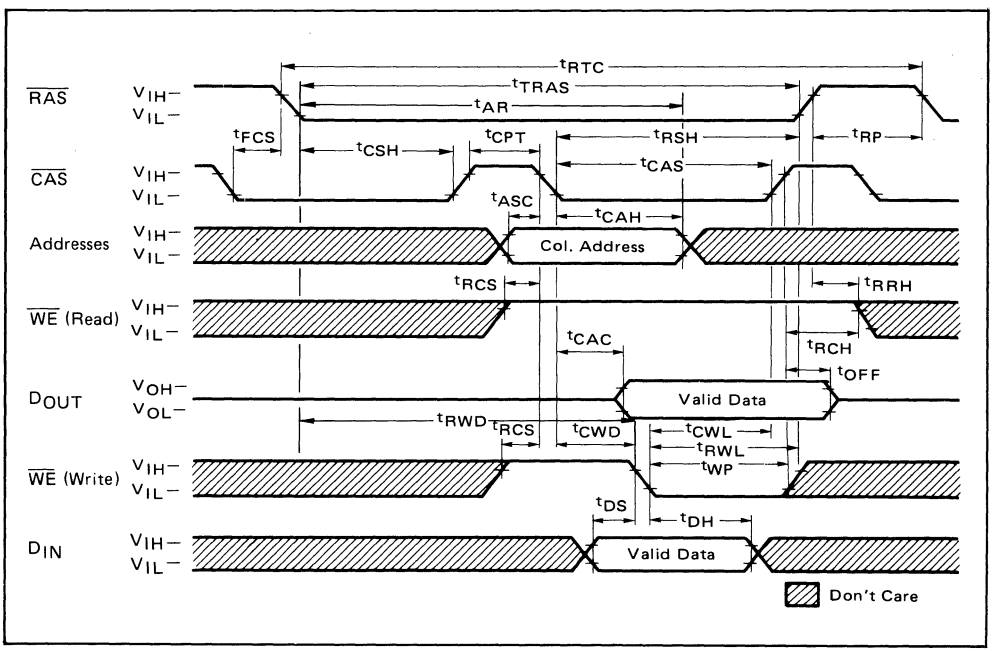
HIDDEN REFRESH CYCLE



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DESCRIPTION

Simple Timing Requirement

The MSM411001 has the circuit considerations for easy operational timing requirements for high speed access time operations. The MSM411001 can operate under the condition of t_{RCD} (max) = t_{CAC} which provides an optimal time space for address multiplexing. In addition, the MSM411001 has the minimal hold times of Address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). And the MSM411001 can commit better memory system through-put during operations in an inter-leaved system.

Fast Read- While-Write cycle

The MSM411001 has the fast read while write cycle which is achieved by excellent control of the three-state output buffer in addition to the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{WE}$ when $\overline{CAS}$ goes low. When $\overline{WE}$ is low during $\overline{CAS}$ transition to low, the MSM411001 goes to early write mode where the output becomes floating and common I/O bus can be used on the system level. Whereas, when $\overline{WE}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MSM411001 goes to delayed write mode where the output contains the data from the cell selected and the data from D_{IN} is written into the cell selected. Therefore, very fast read write cycle becomes available.

Address Inputs

A total of twenty binary input address bits are required to decode any 1 of 1048576 storage cell locations within the MSM411001. Nine row-address bits are established on the input pins (A_0 through A_9) and latched with the Row Address Strobe ($\overline{RAS}$). Then ten column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of RAS. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode, logic "low" dictates write mode. Data input is disabled when read mode is selected.

Data Input

Data is written into the MSM411001 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data in (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought "low" (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transistion of $\overline{RAS}$ when t_{RCD}(max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Nibble Mode

Nibble mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 9 row addresses and the 9 column addresses. The 2 bits of addresses (CA_9 RA_9) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by normal mode, the remaining nibble bits may be accessed by $\overline{CAS}$ "high" then "low" while $\overline{RAS}$ remains "low". Toggling $\overline{CAS}$ causes RA_9 and CA_9 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See Table 1)

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation may be executed again on subsequent access, the new data will be written into the selected cell location.

In nibble mode, the three-state control of D_{OUT} Pin is determined by the first normal access cycle.

The data output is controlled by only $\overline{WE}$ state referenced at $\overline{CAS}$ negative transition of the normal cycle (first Nibble bit). That is, when $t_{WCS} > t_{WCS}$ (min) is met, the data output will remain open circuit throughout the succeeding Nibble cycle regardless of $\overline{WE}$ state. Whereas, when $t_{CWD} > t_{CWD}$ (min) is met, the data output will contain data from the cell selected during the succeeding nibble cycle regardless of $\overline{WE}$ state. The write operation is done during the period where $\overline{WE}$ and $\overline{CAS}$ clocks are low. Therefore, write operation can be done bit by bit during each nibble operation at any timing conditions of $\overline{WE}$ (t_{WCS} and t_{CWD}) at the normal cycle (first Nibble bit).

Table 1 NIBBLE MODE ADDRESS SEQUENCE EXAMPLE

SEQUENCE	NIBBLE BIT	RA_9	ROW ADDRESS	CA_9	COLUMN ADDRESS	
$\overline{RAS}/\overline{CAS}$ (normal mode)	1	0	101010101	0	101010101	----- input addresses
toggle $\overline{CAS}$ (nibble mode)	2	1	101010101	0	101010101	generated internally
toggle $\overline{CAS}$ (nibble mode)	3	0	101010101	1	101010101	
toggle $\overline{CAS}$ (nibble mode)	4	1	101010101	1	101010101	
toggle $\overline{CAS}$ (nibble mode)	1	0	101010101	0	101010101	sequence repeats

$\overline{RAS}$ only Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 512 row-addresses (A_0 through A_8) at least every 8 millisecond. $\overline{RAS}$ only refresh avoids any output during refresh because the buffer is in the high impedance state unless $\overline{CAS}$ is brought "low". Strobing each of the 512 row-addresses (A_0 through A_8) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$ only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the MSM411001 offers an alternate refresh method. If $\overline{CAS}$ is held on "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes to "low", on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh

Hidden refresh cycle may takes place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle. In MSM411001 hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always "low" when $\overline{RAS}$ goes to "low" in hidden refresh.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using $\overline{CAS}$ before $\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$ before $\overline{RAS}$ refresh activted circuitry.

As shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, if $\overline{CAS}$ goes to "high" and goes to "low" again while $\overline{RAS}$ is held "low", the read and write operations are enabled. A memory cell address (consisting of a row address (10 bits) and a column address (10 bits)) to be accessed can be defined as follows:

* A ROW ADDRESS – Bits A_0 through A_8 are defined by the refresh counter.
  The other bit A_9 is set "high" internally.
* A COLUMN ADDRESS – All the bits A_0 through A_9 are defined by latching levels on A_0 throgh A_9 at the second falling edge of CAS.

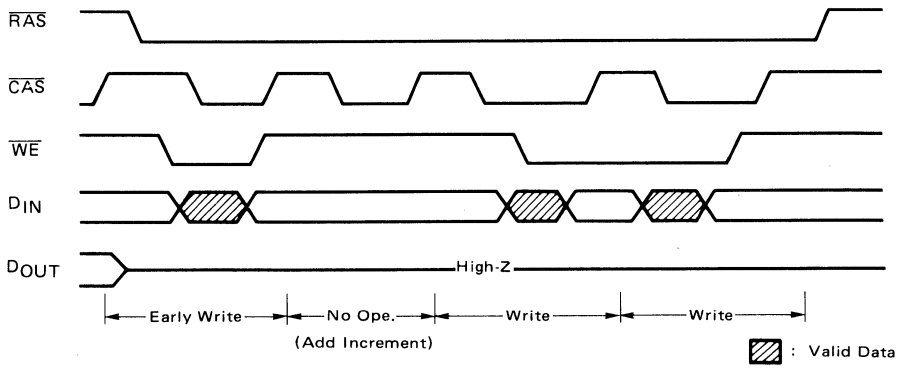
Suggested $\overline{CAS}$ before $\overline{RAS}$ Counter Test Procedure

The timing as shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle is used for all the operations described as follows:

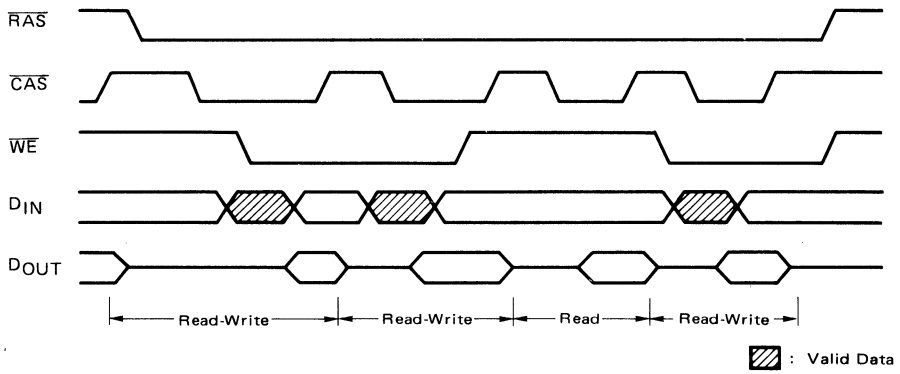
(1) Initialize the internal refresh counter. For this operation, 8 cycles are required.
(2) Write a test pattern of data "low" into memory cells at a single column address and 512 row addresses.
(3) By using read-modify-write cycle, read the "low" written at the last operation (Step (2)) and write a new data "high" in the same cycle. This cycle is repeated 512 times, and data "high" are written into the 512 memory cells.
(4) Read the data "high" written at the last operation (Step (3)).
(5) Complement the test pattern and repeat the steps (2), (3) and (4).

NIBBLE MODE

1) The case of first nibble cycle is Early write



2) The case of first nibble cycle is delyed write (Read-Write)



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FUNCTIONAL TRUTH TABLE

$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Read	Write	Refresh	Note
H	H	Don't Care	Don't Care	High-Z	No	No	No	Standby
L	L	H	Don't Care	Valid Data	Yes	No	Yes	Read
L	L	L	Valid Data	High-Z	No	Yes	Yes	Early Write $t_{WCS} \geqq t_{WCS}$ (min)
L	L	L	Valid Data	Valid Data	Yes	Yes	Yes	Delayed Write or Read-Write $t_{CWD} \geqq t_{CWD}$ (min)
L	H	Don't Care	Don't Care	High-Z	No	No	Yes	$\overline{RAS}$ Only Refresh
L	L	Don't Care	Don't Care	Valid Data	No	No	Yes	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Valid data selected at previous Read or Read-Write cycle is held.
H	L	Don't Care	Don't Care	High-Z	No	No	No	$\overline{CAS}$ disturb.

Preliminary

MSM511000RS

1,048,576-WORD × 1-BIT DYNAMIC RAM <Fast Page>

GENERAL DESCRIPTION

The MSM511000RS is a new generation dynamic RAM organized as 1,048,576 words by 1 bit. The technology used to fabricate the MSM511000RS is OKI's silicon gate CMOS process technology. The device operates from a single +5V power supply. Its I/O pins are TTL compatible.

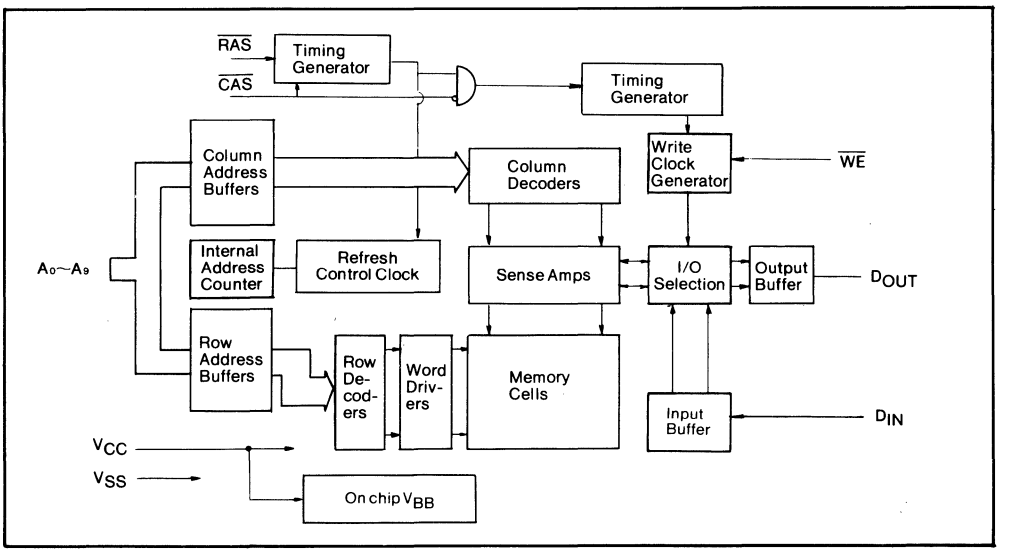
FEATURES

- Silicon gate, N-well CMOS, 1-transistor memory cell
- 1,048,576 words by 1 bit
- Standard 18-pin plastic DIP
- Family organization

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Standby (MAX)
MSM511000-10RS	100 ns	190 ns	385 mW	11 mW
MSM511000-12RS	120 ns	220 ns	330 mW	

- Single +5V supply, ±10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Common I/O capability using "Early Write" operation
- Fast page mode, read modify write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- "Gated" $\overline{CAS}$
- Built-in V_{BB} generator circuit

FUNCTIONAL BLOCK DIAGRAM



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Preliminary

OKI semiconductor

MSM511001RS

1,048,576-WORD × 1-BIT DYNAMIC RAM <Static Column>

GENERAL DESCRIPTION

The MSM511001RS is a new generation dynamic RAM organized as 1,048,576 words by 1 bit. The technology used to fabricate the MSM511001RS is OKI's silicon gate CMOS process technology. The device operates from a single +5V power supply. Its I/O pins are TTL compatible.

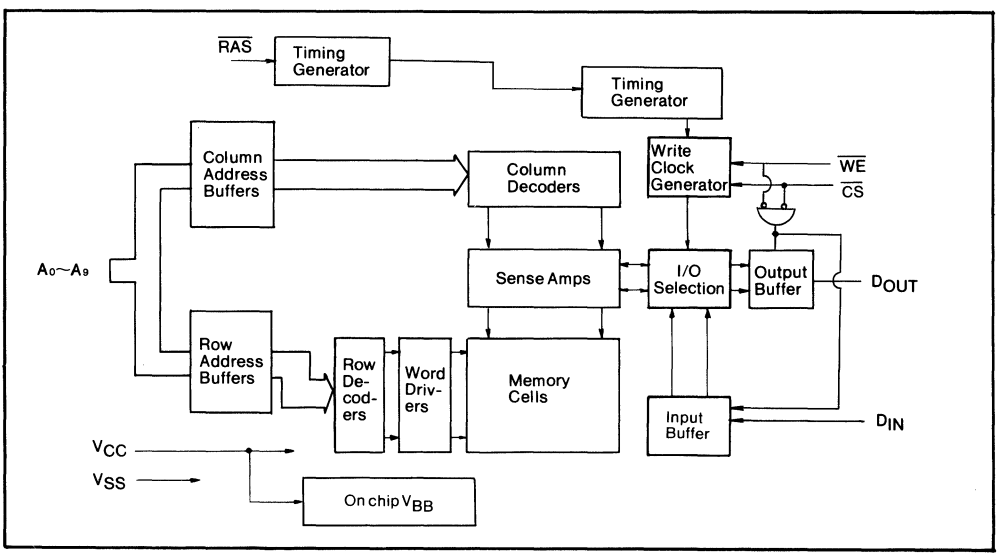
FEATURES

- Silicon gate, N-well CMOS, 1-transistor memory cell
- 1,048,576 words by 1 bit
- Standard 18-pin plastic DIP
- Family organization

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Standby (MAX)
MSM511001-10RS	100 ns	190 ns	385 mW	11 mW
MSM511001-12RS	120 ns	220 ns	330 mW	

- Single +5V supply, ±10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Common I/O capability using "Early Write" operation
- Static column mode, read modify write capability
- $\overline{RAS}$ only refresh capability
- Built-in V_{BB} generator circuit

FUNCTIONAL BLOCK DIAGRAM



Preliminary

MSM514256RS

262,144-WORD × 4-BIT DYNAMIC RAM <Fast Page>

GENERAL DESCRIPTION

The MSM514256RS is a new generation dynamic RAM organized as 262,144 words by 4 bits. The technology used to fabricate the MSM514256RS is OKI's silicon gate CMOS process technology. The device operates from a single +5V power supply. Its I/O pins are TTL compatible.

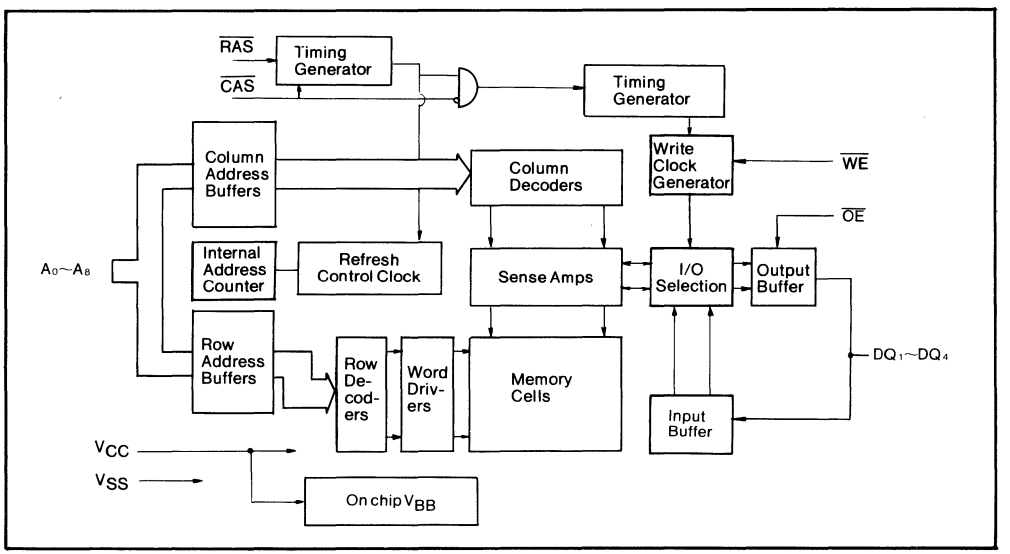
FEATURES

- Silicon gate, N-well CMOS, 1-transistor memory cell
- 262,144 words by 4 bits
- Standard 20-pin plastic DIP
- Family organization

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Standby (MAX)
MSM514256-10RS	100 ns	190 ns	413 mW	11 mW
MSM514256-12RS	120 ns	220 ns	385 mW	

- Single +5V supply, ±10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Output impedance controllable through early write and $\overline{OE}$ operations
- Fast page mode, read modify write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- "Gated" $\overline{CAS}$
- Built-in V_{BB} generator circuit

FUNCTIONAL BLOCK DIAGRAM



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Preliminary

MSM514257RS

262,144-WORD × 4-BIT DYNAMIC RAM <Static Column>

GENERAL DESCRIPTION

The MSM514257RS is a new generation dynamic RAM organized as 262,144 words by 4 bits. The technology used to fabricate the MSM514257RS is OKI's silicon gate CMOS process technology. The device operates from a single +5V power supply. Its I/O pins are TTL compatible.

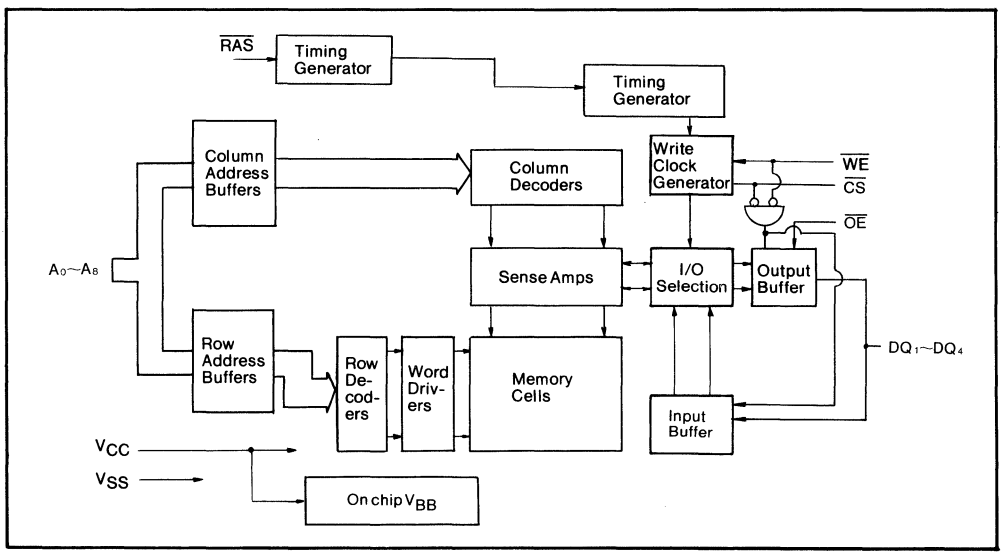
FEATURES

- Silicon gate, N-well CMOS, 1-transistor memory cell
- 262,144 words by 4 bits
- Standard 20-pin plastic DIP
- Family organization

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Standby (MAX)
MSM514257-10RS	100 ns	190 ns	413 mW	11 mW
MSM514257-12RS	120 ns	220 ns	385 mW	

- Single +5V supply, ±10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Output impedance controllable through early write and OE operations
- Static column mode, read modify write capability
- $\overline{RAS}$ only refresh capability
- Built-in V_{BB} generator circuit

FUNCTIONAL BLOCK DIAGRAM



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MSM37S64ARS/37S64RS

131,072-BIT DYNAMIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION

The Oki MSM37S64 is a fully decoded dynamic NMOS random access memory organized as 131,072 one-bit words using 65,536 bit stacked. The design is optimized for high-speed, high performance applications such as main-frame memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

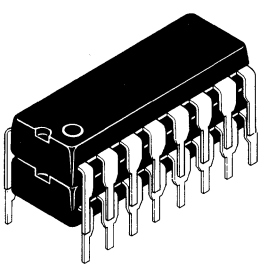
Multiplexed row and column address inputs permit the MSM37S64 to be housed in a standard 16 pin DIP.

The MSM37S64 is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

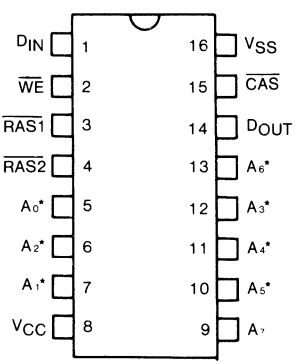
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

- 131,072 × 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time:
  150 ns max (MSM37S64-15)
  200 ns max (MSM37S64-20)
- Cycle time:
  270 ns min (MSM37S64-15)
  330 ns min (MSM37S64-20)
- Low power:
  360 mW active, 55 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" CAS
- 128 refresh cycles/2 ms
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, RAS-only refresh, and Page-Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance



PIN CONFIGURATION (TOP VIEW)



Pin Names	Function
A_0–A_7	Address Inputs
$\overline{RAS1}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

* Refresh Address
1. Designates Bottom Module
2. Designates Top Module

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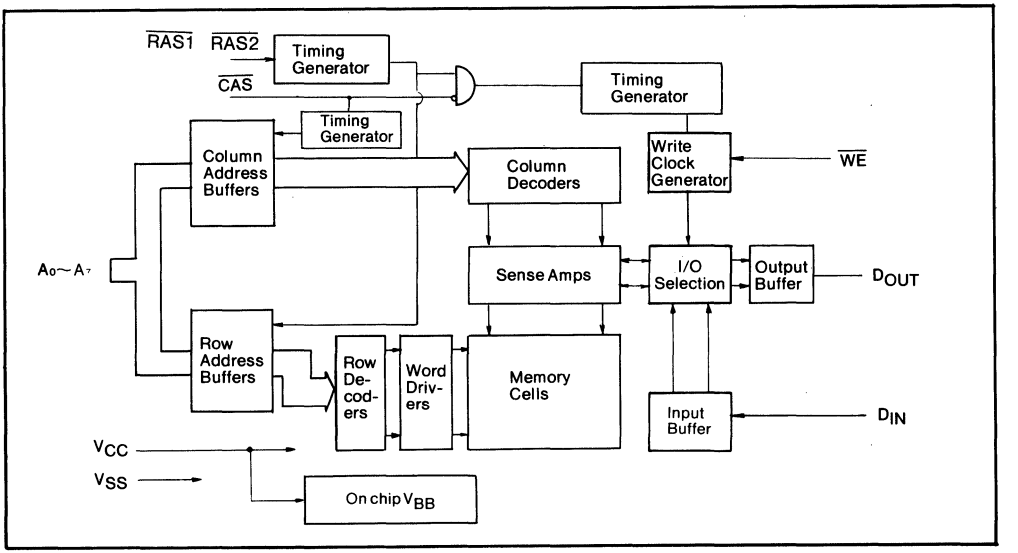
FUNCTIONAL BLOCK DIAGRAM (ONE MODULE)



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (See Note)

(TA = 25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	2	W
Short circuit output current	I_{os}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Note
Operating Current* – One Module Selected Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		65	mA	1
Standby Current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		10	mA	
Refresh Current* – One Module Selected Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} =min.)	I_{CC3}		45	mA	
Page Mode Current* – One Module Selected Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} =min.)	I_{CC4}		65	mA	1
Refresh Current* – Two Module Selected Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC5}		80	mA	
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{L1}	−10	10	μA	
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	μA	
Output Levels Output high voltage (I_{OH} = −5mA) Output low voltage (I_{OL} = 4.2mA)	V_{OH} V_{OL}	2.4	 0.4	V V	

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance ($A_0 \sim A_7$, D_{IN})	C_{IN1}	10	pF
Input Capacitance ($\overline{RAS1}$, $\overline{RAS2}$)	C_{IN2}	10	pF
Input Capacitance ($\overline{CAS}$)	C_{IN3}	15	pF
Input Capacitance ($\overline{WE}$)	C_{IN4}	12	pF
Output Capacitance (D_{OUT})	C_{OUT}	14	pF

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

Parameter	Symbol	Units	MSM37S64-15		MSM37S64-20		Note
			Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		2		2	
Random read or write cycle time	t_{RC}	ns	270		330		
Read-write cycle time	t_{RWC}	ns	270		330		
Page mode cycle time	t_{PC}	ns	170		225		
Access time from $\overline{RAS}$	t_{RAC}	ns		150		200	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		100		135	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	40	0	50	
Transition time	t_T	ns	3	35	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	100		120		
$\overline{RAS}$ pulse width	t_{RAS}	ns	150	10,000	200	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	100		135		
$\overline{CAS}$ precharge time	t_{CP}	ns	60		80		
$\overline{CAS}$ pulse width	t_{CAS}	ns	100	10,000	135	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	150		200		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	50	30	65	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		
Row Address set-up time	t_{ASR}	ns	0		0		

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Units	MSM37S64-15		MSM37S64-20		Note
			Min.	Max.	Min.	Max.	
Row Address hold time	t_{RAH}	ns	15		20		
Column Address set-up time	t_{ASC}	ns	0		0		
Column Address hold time	t_{CAH}	ns	45		55		
Column Address hold time reference to $\overline{RAS}$	t_{AR}	ns	95		120		
Read command set-up time	t_{RCS}	ns	0		0		
Read command hold time	t_{RCH}	ns	0		0		
Write command set-up time	t_{WCS}	ns	−10		−10		8
Write command hold time	t_{WCH}	ns	45		55		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	95		120		
Write command pulse width	t_{WP}	ns	45		55		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	45		55		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	45		55		
Data-in set-up time	t_{DS}	ns	0		0		
Data-in hold time	t_{DH}	ns	45		55		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	95		120		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	60		80		8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	110		145		8
Read command hold time reference to $\overline{RAS}$	t_{RRH}	ns	20		25		

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

Parameter	Symbol	Units	MSM37S64A-15		MSM37S64A-20		Note
			Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		2		2	
Random read or write cycle time	t_{RC}	ns	260		330		
Read-write cycle time	t_{RWC}	ns	280		345		
Page mode cycle time	t_{PC}	ns	145		190		
Access time from $\overline{RAS}$	t_{RAC}	ns		150		200	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		75		100	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	40	0	50	
Transition time	t_T	ns	3	35	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	100		120		
$\overline{RAS}$ pulse width	t_{RAS}	ns	150	10,000	200	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	75		100		
$\overline{CAS}$ precharge time (page mode only)	t_{CP}	ns	60		80		
$\overline{CAS}$ precharge time	t_{CPN}	ns	35		45		
$\overline{CAS}$ pulse width	t_{CAS}	ns	75	10,000	100	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	150		200		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	75	30	100	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		
Row Address set-up time	t_{ASR}	ns	0		0		
Row Address hold time	t_{RAH}	ns	15		20		
Column Address set-up time	t_{ASC}	ns	0		0		
Column Address hold time	t_{CAH}	ns	20		25		
Column Address hold time reference to $\overline{RAS}$	t_{AR}	ns	95		125		
Read command set-up time	t_{RCS}	ns	0		0		

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AC CHARACTERISTICS (Continued)

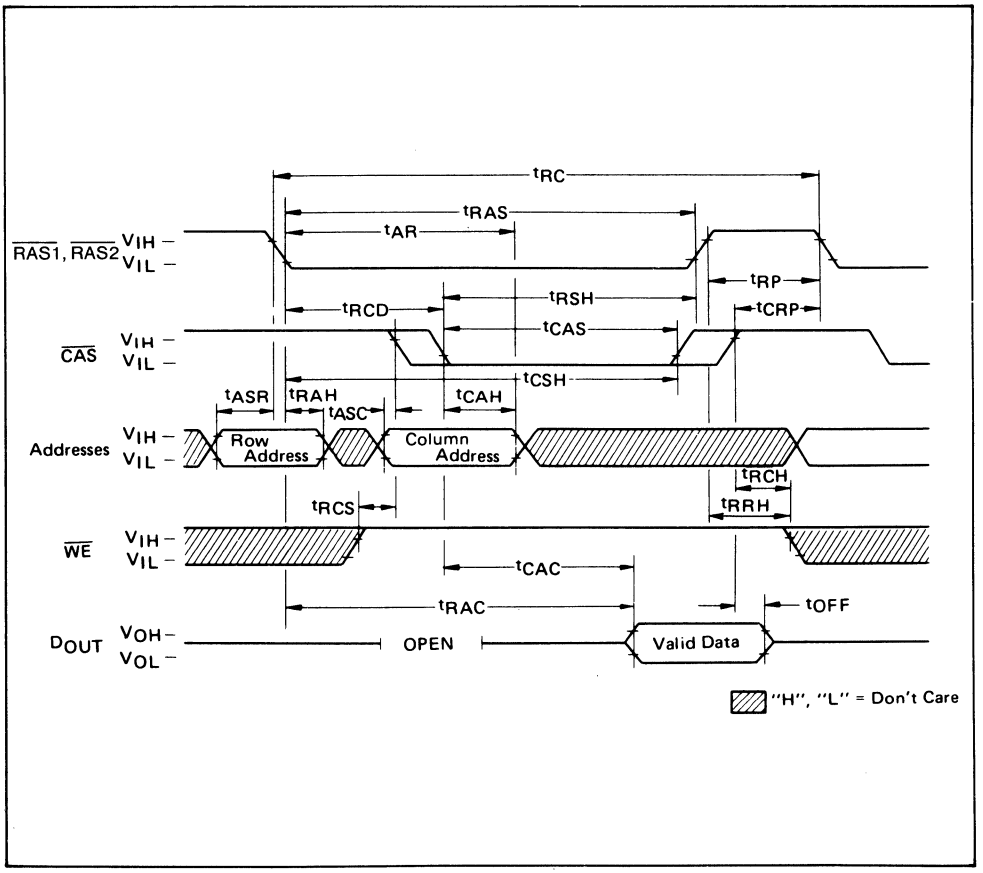
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Units	MSM37S64A-15		MSM37S64A-20		Note
			Min.	Max.	Min.	Max.	
Read command hold time	t_{RCH}	ns	0		0		
Write command set-up time	t_{WCS}	ns	−10		−10		8
Write command hold time	t_{WCH}	ns	45		55		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	120		155		
Write command pulse width	t_{WP}	ns	45		55		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	45		55		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	45		55		
Data-in set-up time	t_{DS}	ns	0		0		
Data-in hold time	t_{DH}	ns	45		55		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	120		155		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	45		55		8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	120		155		8
Read command hold time reference to $\overline{RAS}$	t_{RRH}	ns	0		0		

Notes:

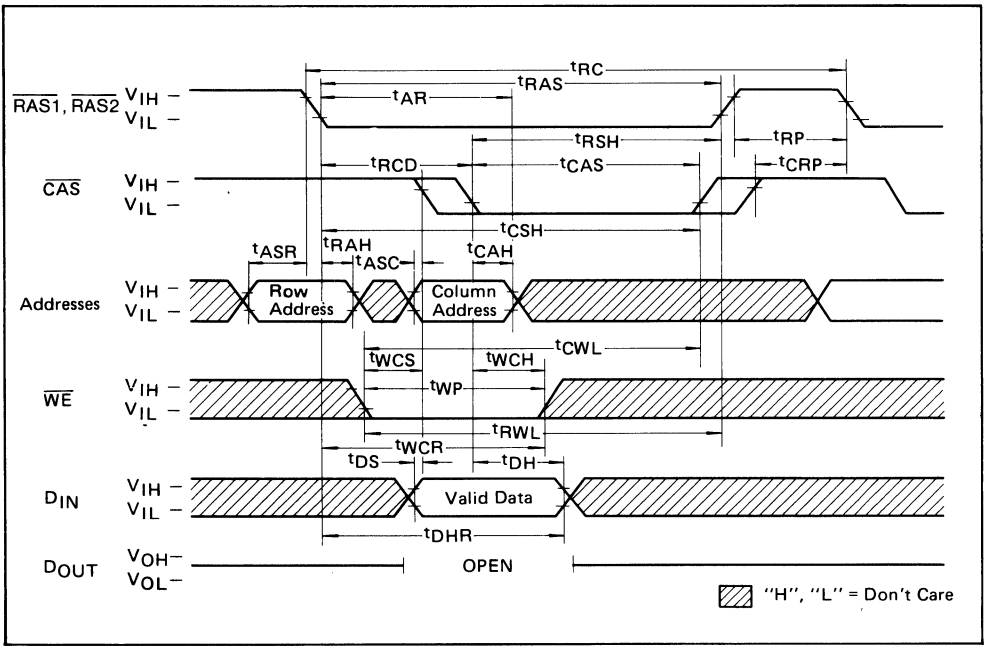
1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. AC measurements assume at $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} < t_{RCD}$ (Max.)
   If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} < t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} > t_{RWD}$ (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

READ CYCLE TIMING

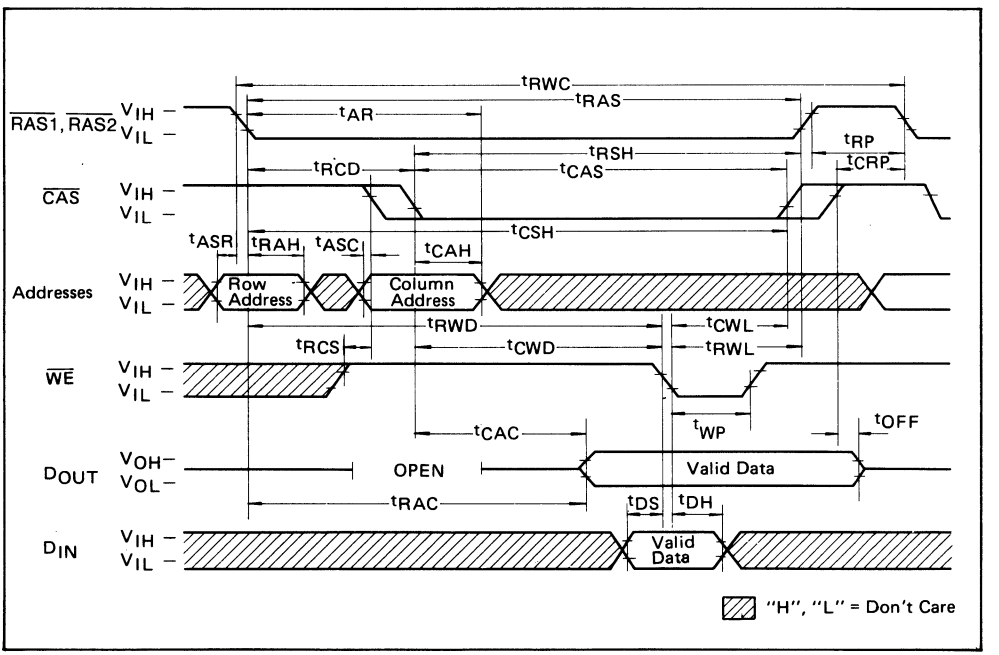


WRITE CYCLE TIMING

(EARLY WRITE)

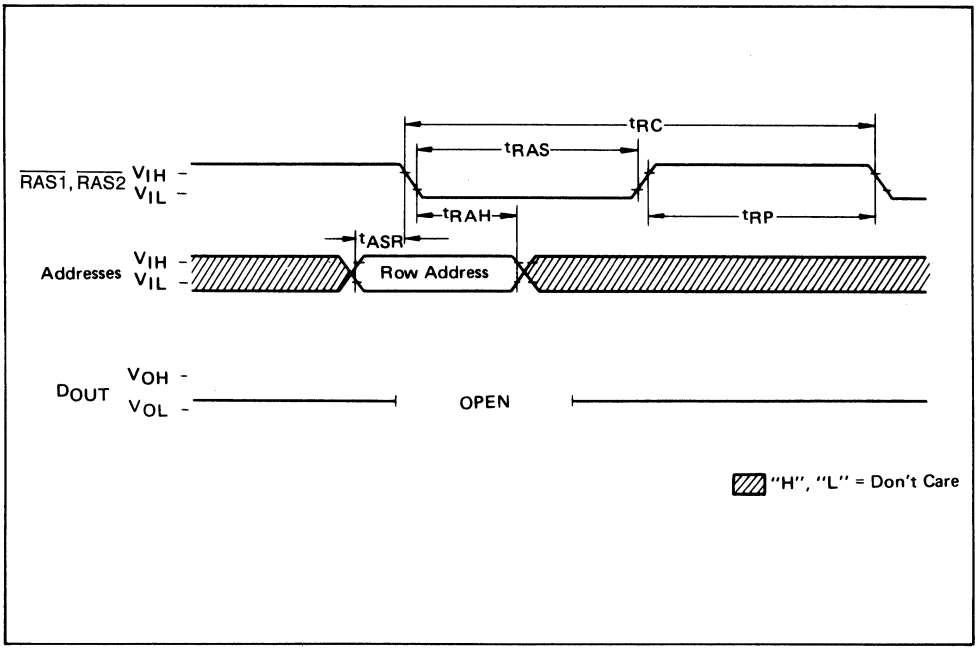


READ-WRITE/READ-MODIFY-WRITE CYCLE

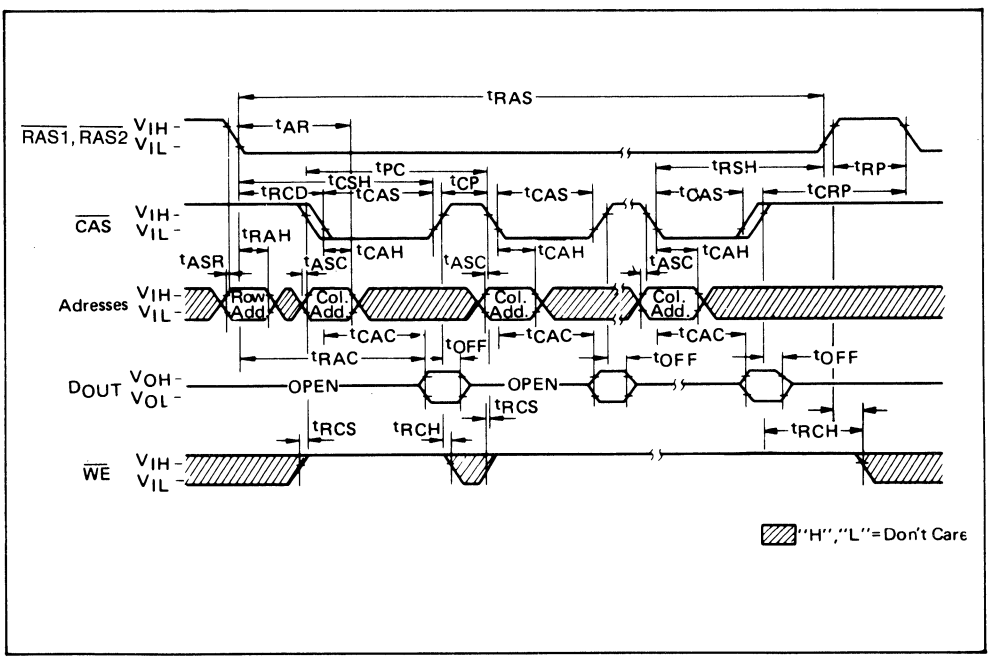


$\overline{RAS}$ ONLY REFRESH TIMING

($\overline{CAS}$: V_{IH}, $\overline{WE}$ & D_{IN}: Don't care)



PAGE MODE READ CYCLE



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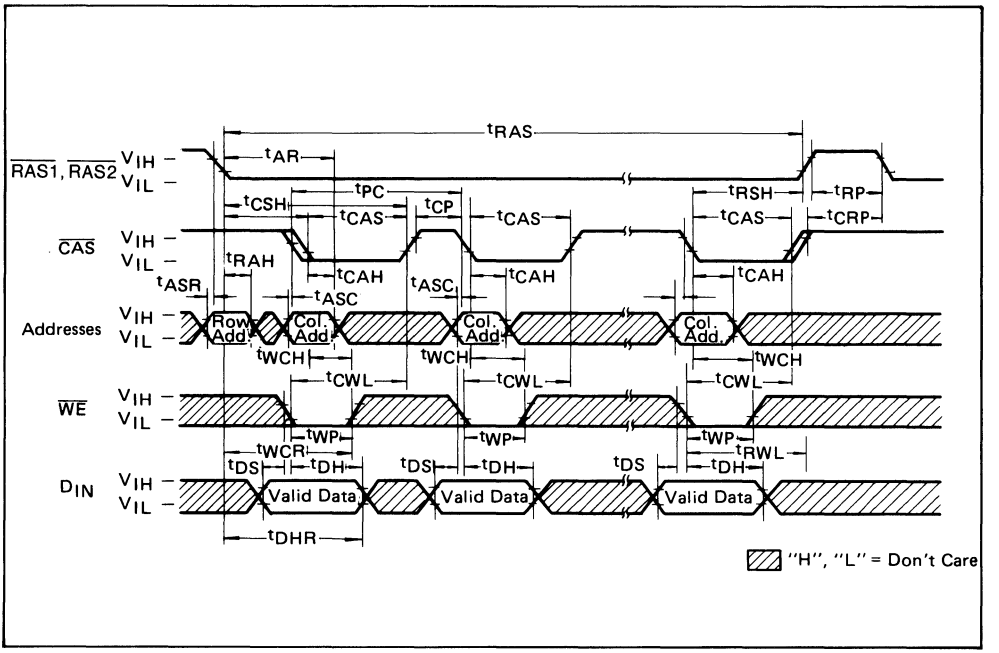
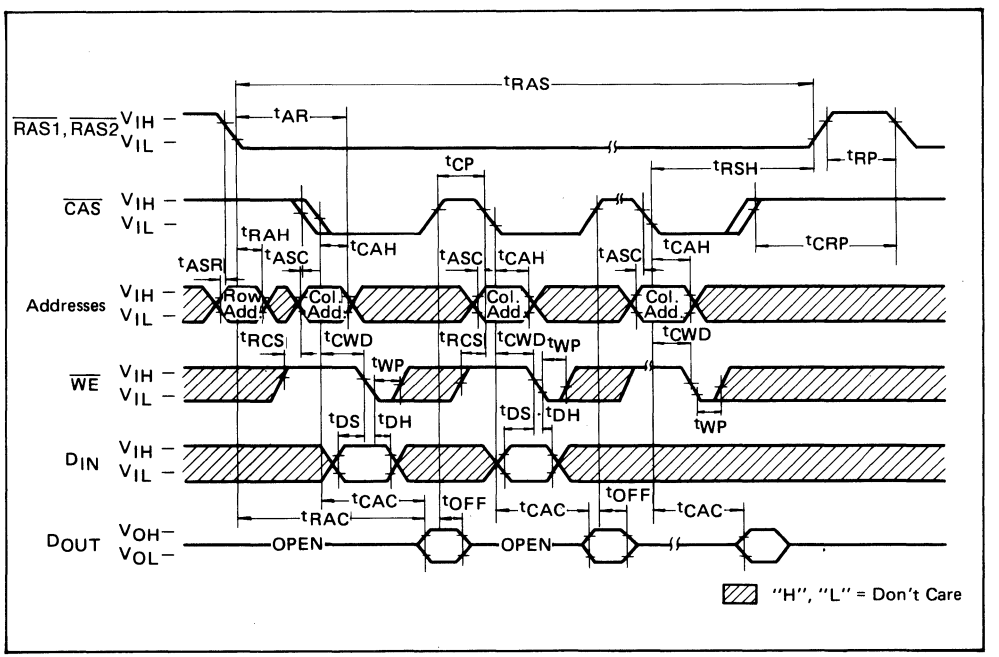
PAGE MODE WRITE CYCLE



PAGE MODE, READ-MODIFY-WRITE CYCLE



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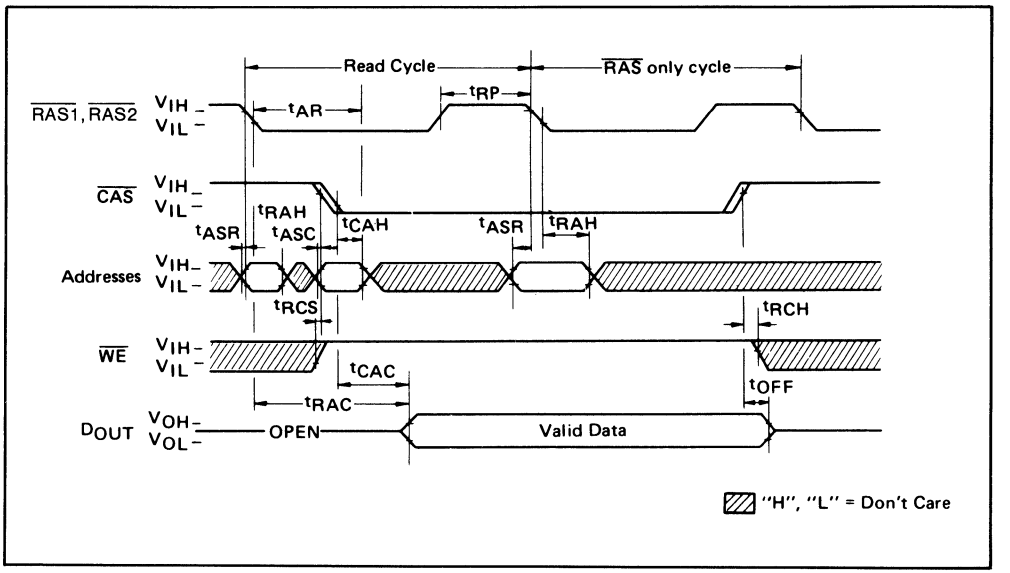
HIDDEN REFRESH



FUNCTIONAL DESCRIPTION

Address Inputs:

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the one module. Eight row-address bits are established on the input pins ($A_0 \sim A_7$) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$, $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses. The top module or bottom module is selected with $\overline{RAS1}$ input and $\overline{RAS2}$ input.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM37S64 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (Max.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (Max.). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSM37S64 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at

each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Hidden Refresh:

$\overline{RAS}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

Preliminary

MSC2301YS9/KS9

65,536 BY 9 BIT DYNAMIC RAM MODULE

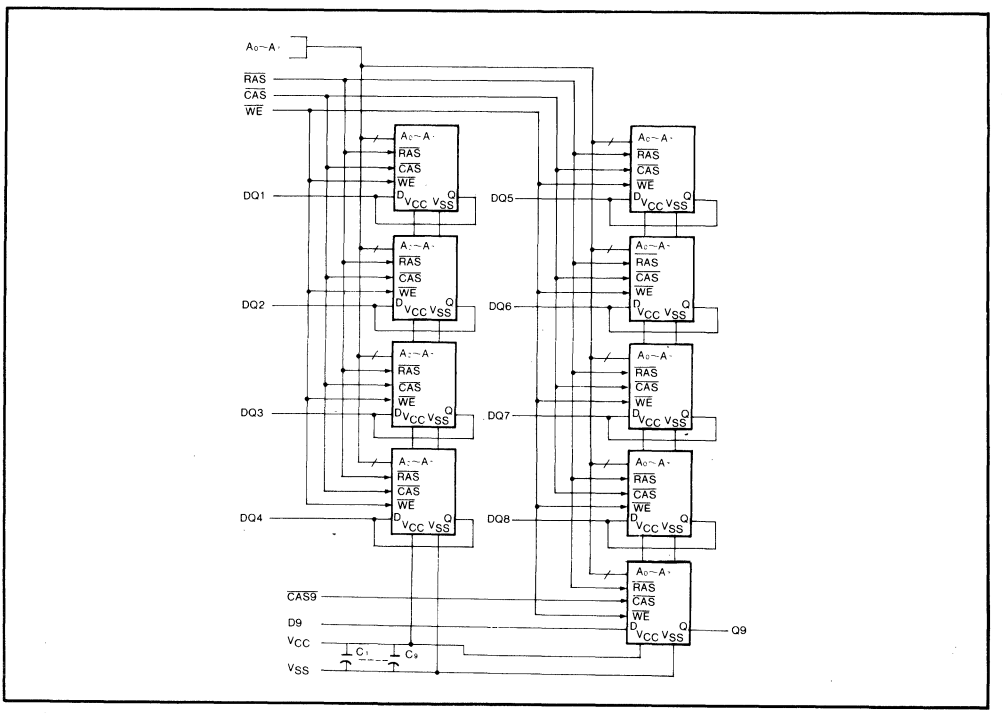
GENERAL DESCRIPTION

The Oki MSC2301YS9/KS9 is a fully decoded, 65,536 words × 9 bit NMOS dynamic random access memory composed of nine 64K DRAMs in plastic leaded chip carrier. The mounting of nine PLCCs together with nine 0.2μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2301YS9/KS9 are quite same as the original MSM3764A; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

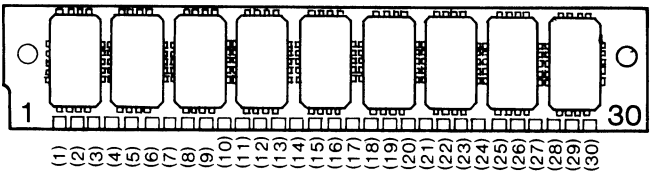
- 65,536 word × 9 bit Organization
- Single +5V Supply (10% Tolerance)
- 30-Pin Socket Insertable Module
- Refresh Period ... 2ms (128 cycles)
- All Inputs, Outputs, Clocks Fully TTL compatible
- 3-States Outputs
- Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines
- Separate $\overline{CAS}$ Control for One Separate Pair of Data-In and Data-Out Lines
- Row Access Time;
  120ns max. (MSC2301-12YS9/KS9)
  150ns max. (MSC2301-15YS9/KS9)
- Low Power Dissipation;
  2970mW max. (MSC2301-12YS9/KS9)
  2725mW max. (MSC2301-15YS9/KS9)
- Operating Temperature ... 0°C to 70°C

FUNCTIONAL BLOCK DIAGRAM

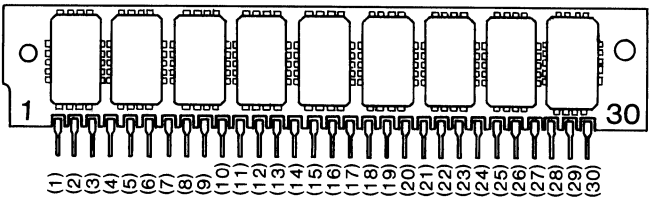


PIN ASSIGNMENT

MSC2301YS9



MSC2301KS9



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	V_{CC}	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ1	13	DQ4	23	DQ7
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ8
6	DQ2	16	DQ5	26	Q9
7	A2	17	NC	27	$\overline{RAS}$
8	A3	18	NC	28	$\overline{CAS9}$
9	VSS	19	NC	29	D9
10	DQ3	20	DQ6	30	V_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−40 to +125	°C
Power dissipation	P_D	9	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	120ns MODULE		150ns MODULE		Unit
		Min.	Max.	Min.	Max.	
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		540		495	mA
Standby Current* Power supply current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC2}		45		45	mA
Refresh Current* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$; t_{RC} =min.)	I_{CC3}		360		360	mA
Page Mode Current* Average power supply current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{PC} =min.)	I_{CC4}		450		405	mA
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{L1}	−90	90	−90	90	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	−10	10	μA
Output Levels Output high voltage (I_{OH} = −5mA)	V_{OH}	2.4		2.4		V
Output low voltage (I_{OL} = 4.2mA)	V_{OL}		0.4		0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance ($A_0 \sim A_7$)	C_{IN1}	40	70	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	40	75	pF
Data Input/Output Capacitance (DQ)	C_{DQ}	7	20	pF
Input Capacitance ($\overline{CAS9}$)	C_{IN3}	5	10	pF
Input Capacitance (D9)	C_{IN4}	4	10	pF
Output Capacitance (Q9)	C_{OUT}	4	15	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

Parameter	Symbol	Units	MSC2301-12YS/KS		MSC2301-15YS/KS		Note
			Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		2		2	
Random read or write cycle time	t_{RC}	ns	220		260		
Page mode cycle time	t_{PC}	ns	120		145		
Access time from $\overline{RAS}$	t_{RAC}	ns		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	35	0	40	
Transition time	t_T	ns	3	35	3	35	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	120	10,000	150	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	60		75		
$\overline{CAS}$ precharge time	t_{CP}	ns	50		60		
$\overline{CAS}$ pulse width	t_{CAS}	ns	60	10,000	75	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	120		150		

AC CHARACTERISTICS (Continued)

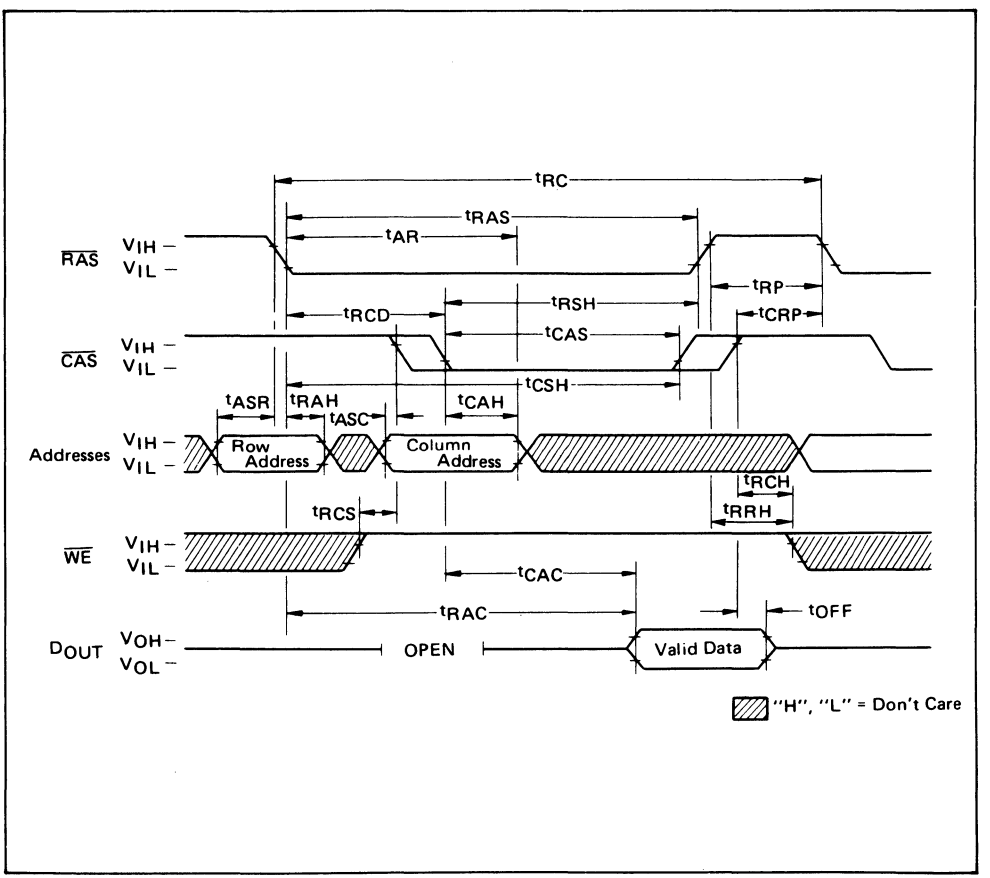
(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

Parameter	Symbol	Units	MSC2301-12YS/KS		MSC2301-15YS/KS		Note
			Min.	Max.	Min.	Max.	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	60	25	75	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		
Row Address set-up time	t_{ASR}	ns	0		0		
Row Address hold time	t_{RAH}	ns	15		15		
Column Address set-up time	t_{ASC}	ns	0		0		
Column Address hold time	t_{CAH}	ns	20		20		
Column Address hold time reference to $\overline{RAS}$	t_{AR}	ns	80		95		
Read command set-up time	t_{RCS}	ns	0		0		
Read command hold time	t_{RCH}	ns	0		0		
Write command set-up time	t_{WCS}	ns	−10		−10		
Write command hold time	t_{WCH}	ns	40		45		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	100		120		
Write command pulse width	t_{WP}	ns	40		45		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	40		45		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	40		45		
Data-in set-up time	t_{DS}	ns	0		0		
Data-in hold time	t_{DH}	ns	40		45		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	100		120		

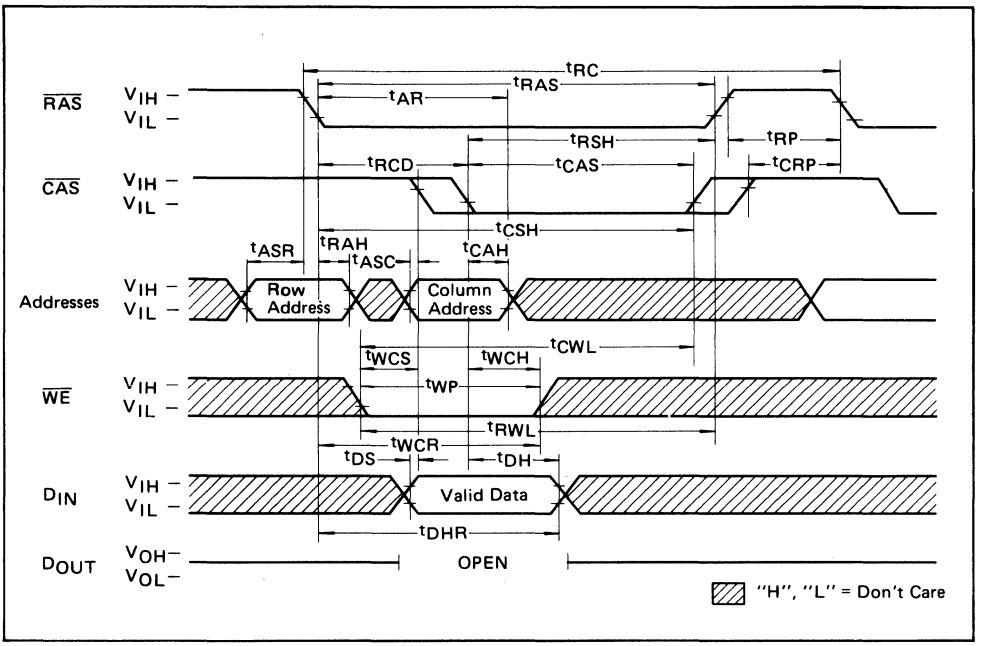
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. AC measurements assume at $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} < t_{RCD}$ (Max.)
   If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
5. Assumes that $t_{RCD} < t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.

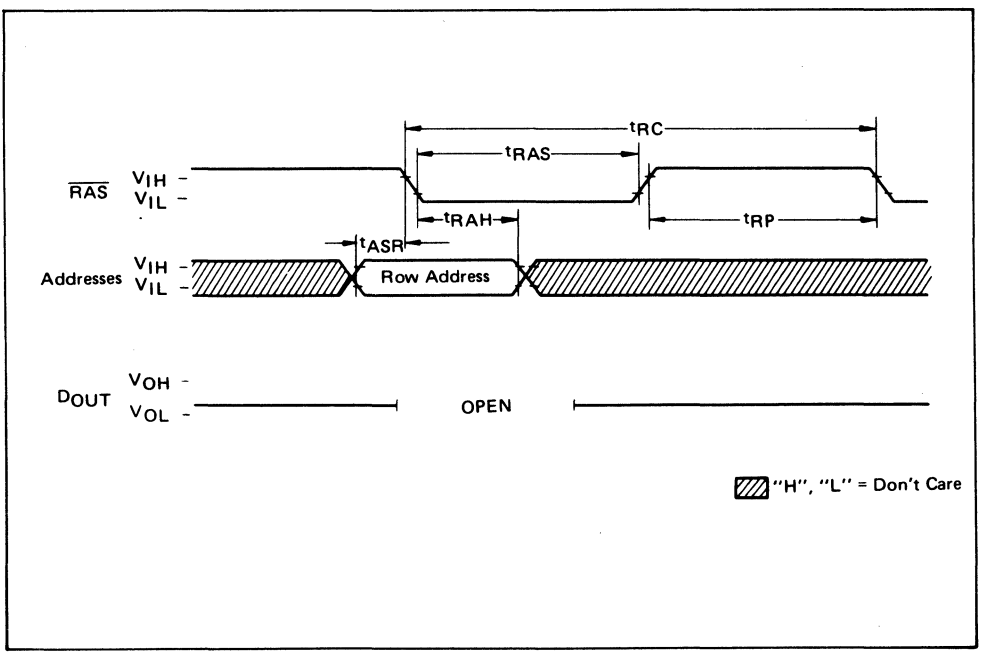
READ CYCLE TIMING



WRITE CYCLE TIMING
(EARLY WRITE)



RAS ONLY REFRESH TIMING
(CAS: VIH, WE & DIN: Don't care)



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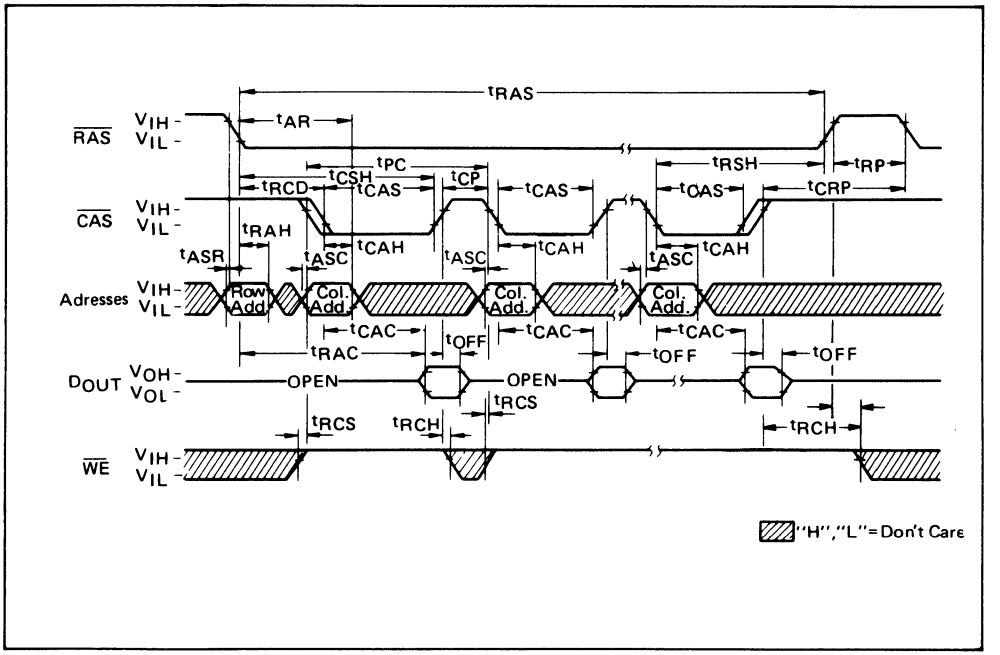
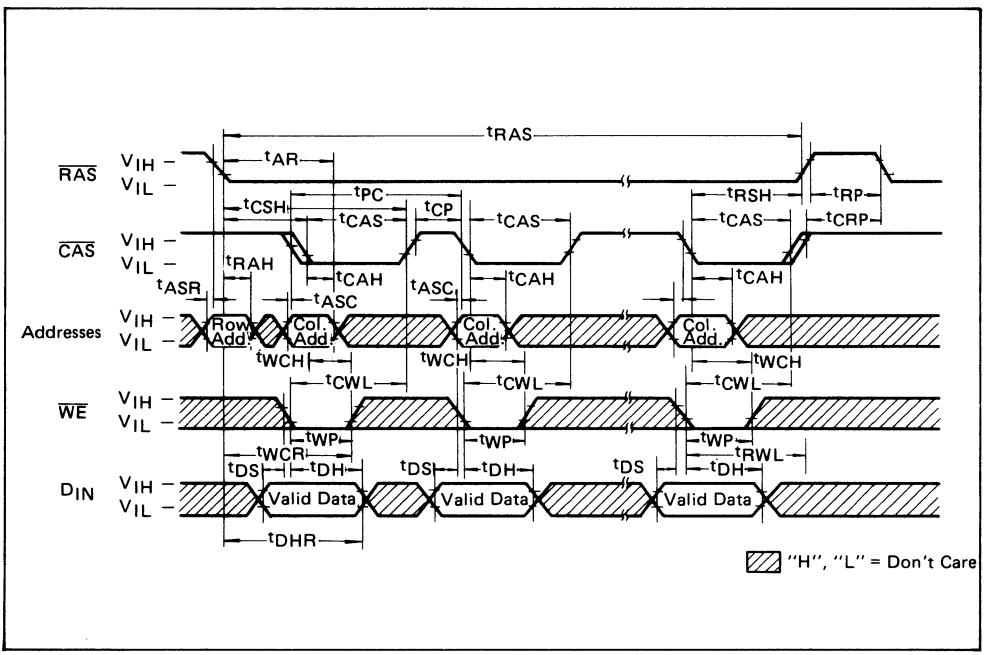
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



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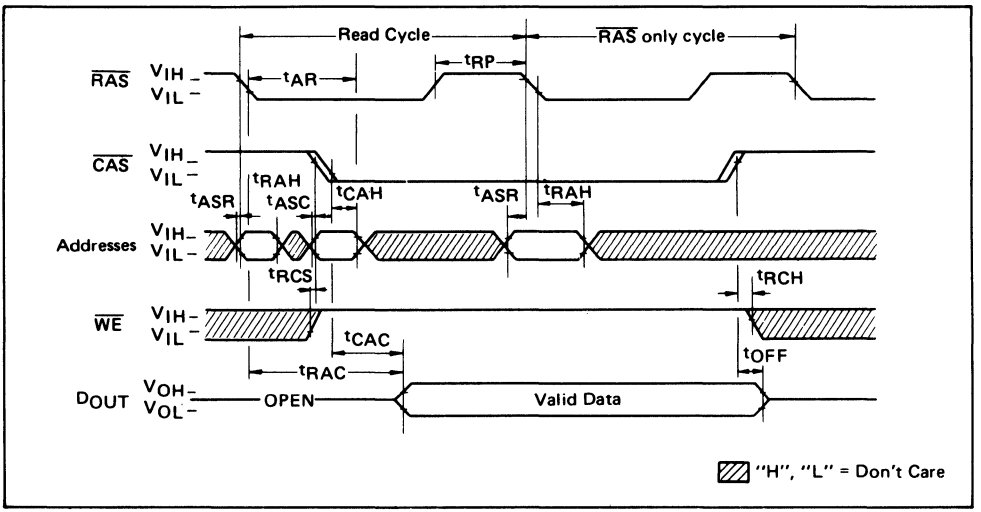
HIDDEN REFRESH



FUNCTIONAL DESCRIPTION

Address Inputs:

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MSC2301. Eight row-address bits are established on the input pins ($A_0 \sim A_7$) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$, $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSC2301 during a write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (Max.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (Max.). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSC2301 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in

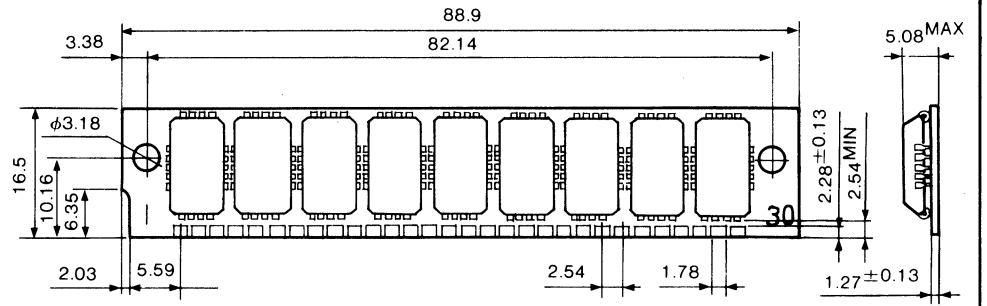
each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

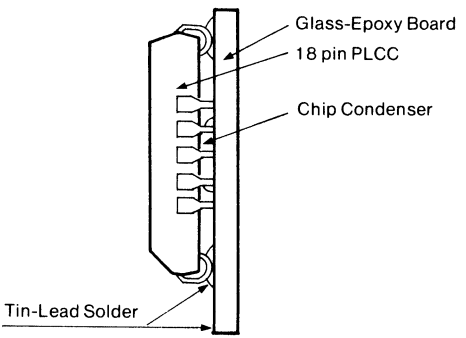
Hidden Refresh:

$\overline{RAS}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

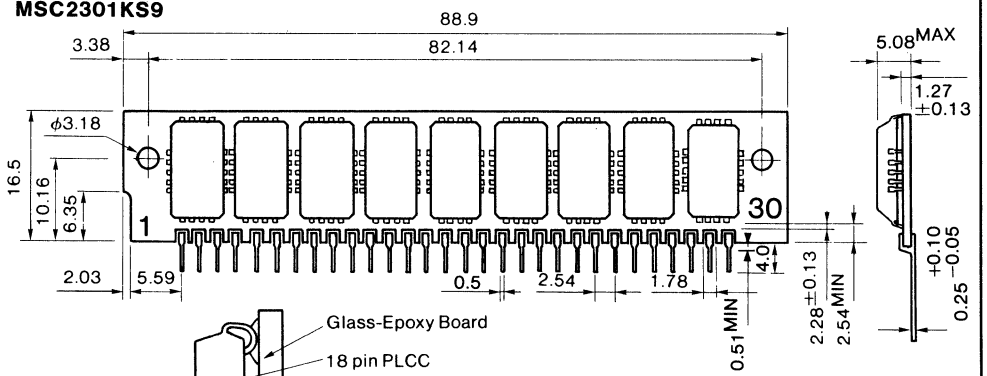
MSC2301YS9

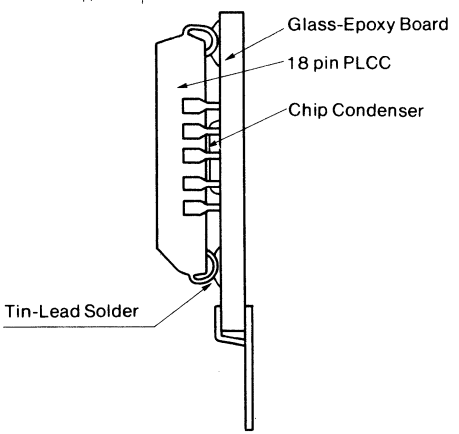




1. Substrate: GLASS-EPOXY
2. Through Hole: Copper Plating Followed by Sn/Pb Plating
3. Contact Pads: Copper Plating Followed by Sn/Pb Plating on Copper Film (18μm^t)
4. Surface Coating: Photo Film Resist

MSC2301KS9





1. Substrate: GLASS-EPOXY
2. Through Hole: Copper Plating Followed by Sn/Pb Plating
3. Contact Pads: Copper Plating Followed by Sn/Pb Plating on Copper Film (18μm^t)
4. Surface Coating: Photo Film Resist

9

MSC2304YS8/KS8

262,144 BY 8 BIT DYNAMIC RAM MODULE

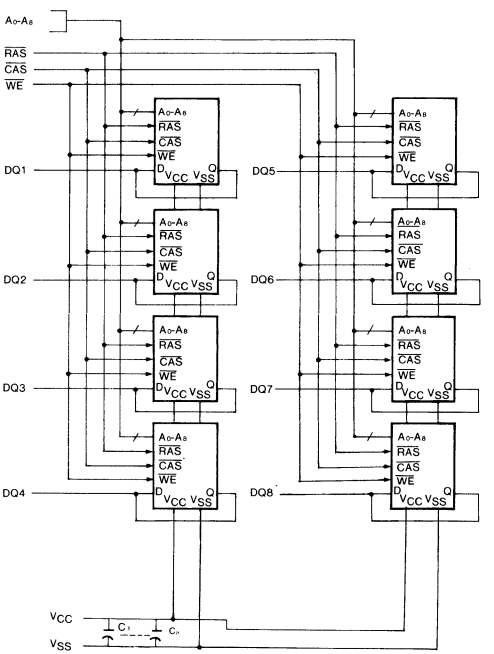
GENERAL DESCRIPTION

The Oki MSC2304YS8/KS8 is a fully decoded, 262,144 words × 8 bit NMOS dynamic random access memory composed of eight 256K DRAMs in plastic leaded chip carrier (MSM41256JS). The mounting of eight PLCCs together with eight 0.2μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2304YS8/KS8 are quite same as the original MSM41256JS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

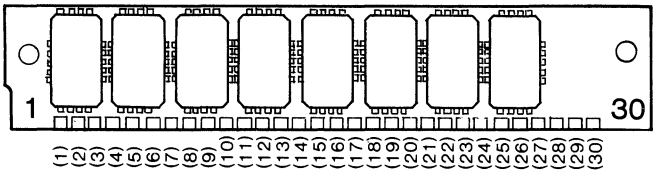
- 262,144 word × 8 bit Organization
- Single +5V Supply (10% Tolerance)
- 30-Pin Socket Insertable Module
- Refresh Period ... 4ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL compatible
- 3-States Outputs
- Common CAS Control for Eight Common Data-In and Data-Out Lines
- Row Access Time;
  120ns max. (MSC2304-12YS8/KS8)
  150ns max. (MSC2304-15YS8/KS8)
- Low Power Dissipation;
  3080mW max. (MSC2304-12YS8/KS8)
  2860mW max. (MSC2304-15YS8/KS8)
- Operating Temperature ... 0°C to 70°C

FUNCTIONAL BLOCK DIAGRAM

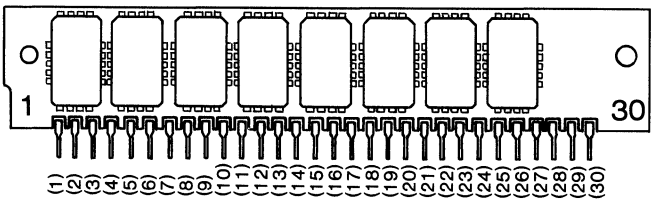


PIN ASSIGNMENT

MSC2304YS8



MSC2304KS8



PIN No.	PIN NAME	PIN No.	PIN NAME
1	V_{CC}	16	DQ5
2	$\overline{CAS}$	17	A8
3	DQ1	18	NC
4	A0	19	NC
5	A1	20	$\underline{DQ6}$
6	DQ2	21	$\overline{WE}$
7	A2	22	VSS
8	A3	23	DQ7
9	VSS	24	NC
10	DQ3	25	DQ8
11	A4	26	$\underline{NC}$
12	A5	27	$\overline{RAS}$
13	DQ4	28	NC
14	A6	29	NC
15	A7	30	V_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−40 to +125	°C
Power dissipation	P_D	8	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	120ns MODULE		150ns MODULE		Unit
		Min.	Max.	Min.	Max.	
Operating Current* Average power supply current (RAS, CAS cycling; t_{RC} = min.)	I_{CC1}		560		520	mA
Standby Current Power supply current (RAS = CAS = V_{IH})	I_{CC2}		40		40	mA
Refresh Current Average power supply current (RAS cycling, CAS = V_{IH}; t_{RC} =min.)	I_{CC3}		440		400	mA
Page Mode Current* Average power supply current (RAS = V_{IL}, CAS cycling; t_{PC} =min.)	I_{CC4}		440		400	mA
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{L1}	−80	80	−80	80	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	−10	10	μA
Output Levels Output high voltage (I_{OH} = −5mA)	V_{OH}	2.4		2.4		V
Output low voltage (I_{OL} = 4.2mA)	V_{OL}		0.4		0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance ($A_0 \sim A_8$)	C_{IN1}	37	60	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	35	65	pF
Data Input/Output Capacitance (DQ)	C_{DQ}	7	20	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

Parameter	Symbol	Units	MSC2304-12YS/KS		MSC2304-15YS/KS		Note
			Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4	
Random read or write cycle time	t_{RC}	ns	230		260		
Page mode cycle time	t_{PC}	ns	125		145		
Access time from $\overline{RAS}$	t_{RAC}	ns		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	40	0	40	
Transition time	t_T	ns	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	100		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	120	10,000	150	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	60		75		
$\overline{CAS}$ precharge time	t_{CP}	ns	55		60		
$\overline{CAS}$ pulse width	t_{CAS}	ns	60	10,000	75	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	60	25	75	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		

AC CHARACTERISTICS (CONT.)

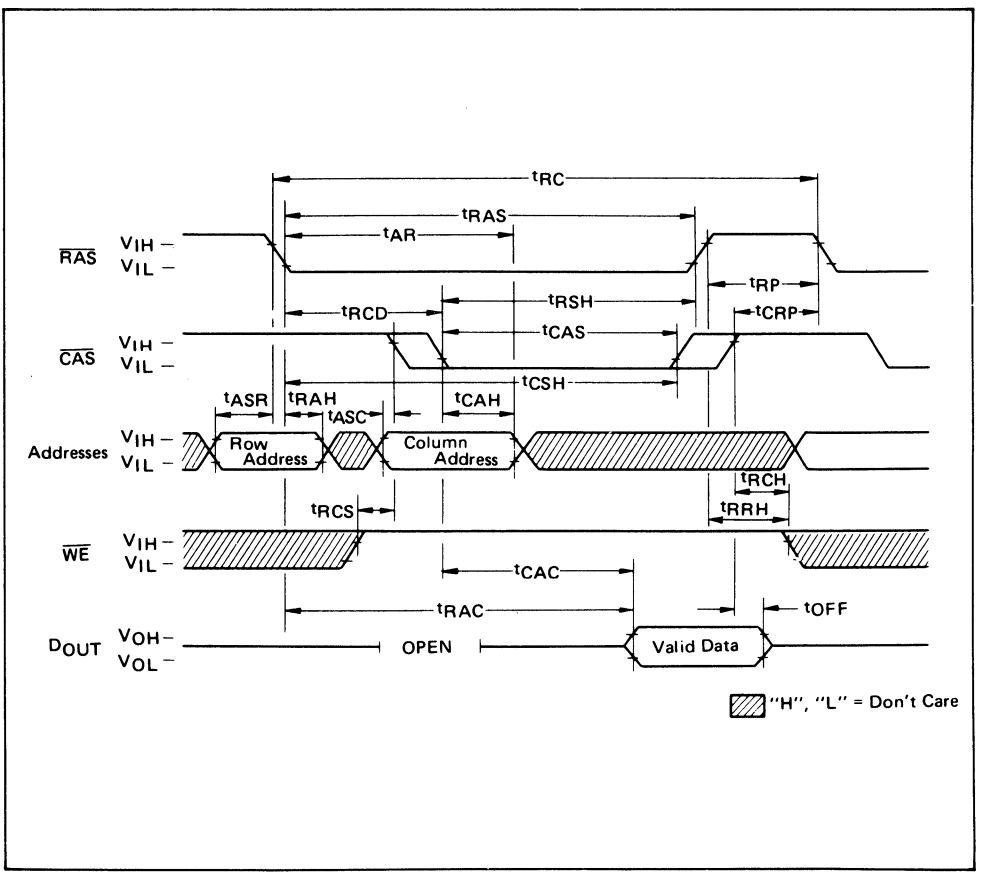
Parameter	Symbol	Units	MSC2304-12YS/KS		MSC2304-15YS/KS		Note
			Min.	Max.	Min.	Max.	
Row Address set-up time	t_{ASR}	ns	0		0		
Row Address hold time	t_{RAH}	ns	15		20		
Column Address set-up time	t_{ASC}	ns	0		0		
Column Address hold time	t_{CAH}	ns	30		35		
Column Address hold time reference to $\overline{RAS}$	t_{AR}	ns	90		110		
Read command set-up time	t_{RCS}	ns	0		0		
Read command hold time	t_{RCH}	ns	0		0		
Write command set-up time	t_{WCS}	ns	0		0		
Write command hold time	t_{WCH}	ns	40		45		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	100		120		
Write command pulse width	t_{WP}	ns	40		45		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	40		45		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	40		45		
Data-in set-up time	t_{DS}	ns	0		0		
Data-in hold time	t_{DH}	ns	40		45		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	100		120		

Note 1, 2, 3: Under recommended operating conditions

Notes:

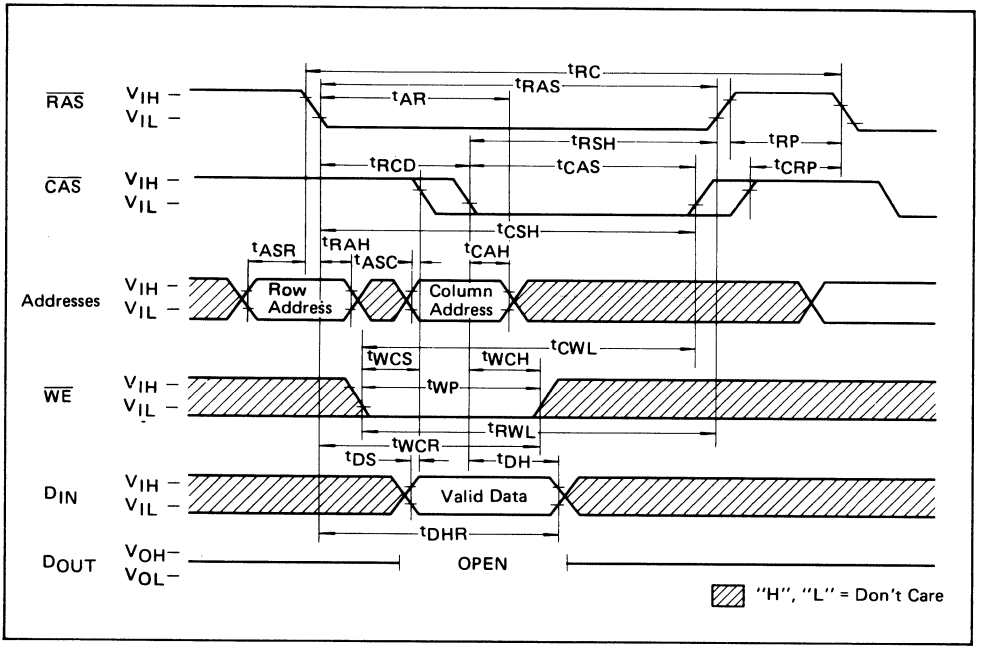
1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. AC measurements assume at $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} < t_{RCD}$ (Max.)
   If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
5. Assumes that $t_{RCD} < t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.

READ CYCLE TIMING



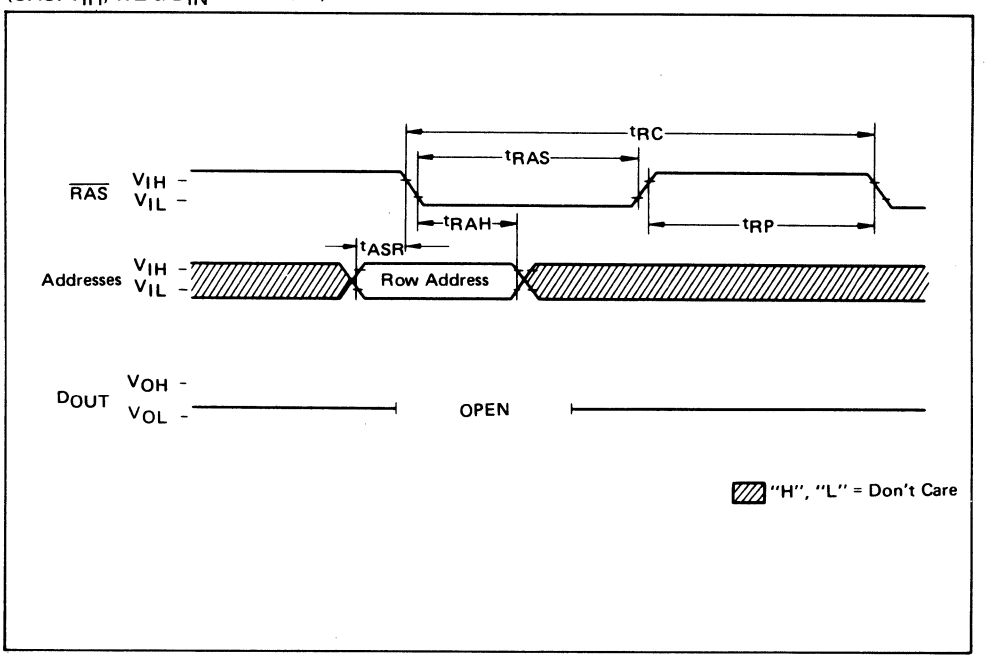
WRITE CYCLE TIMING

(EARLY WRITE)



RAS ONLY REFRESH TIMING

(CAS: V_{IH}, WE & D_{IN}: Don't care)



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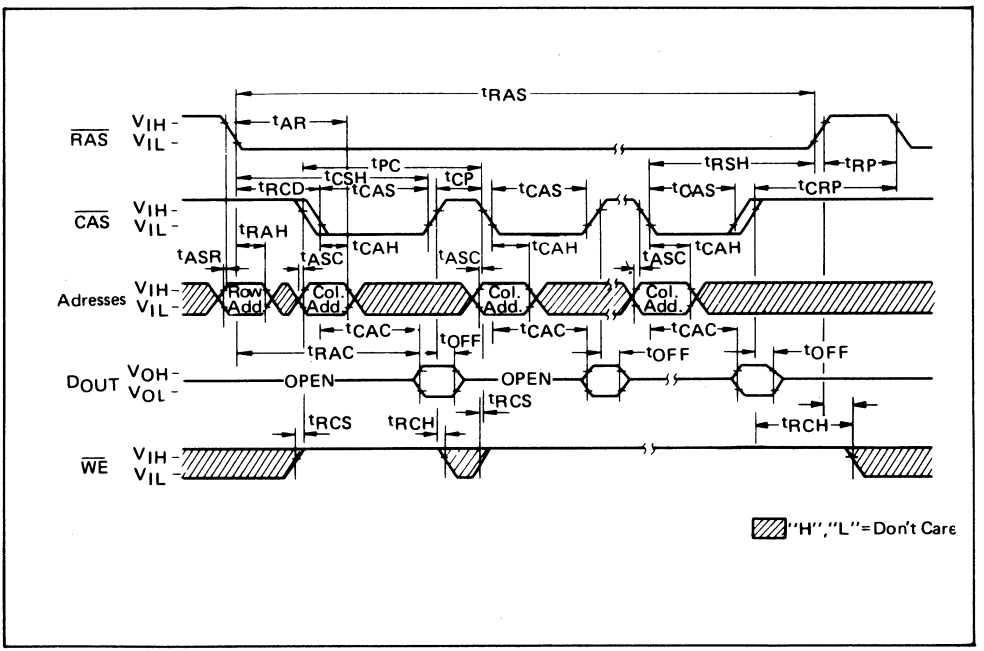
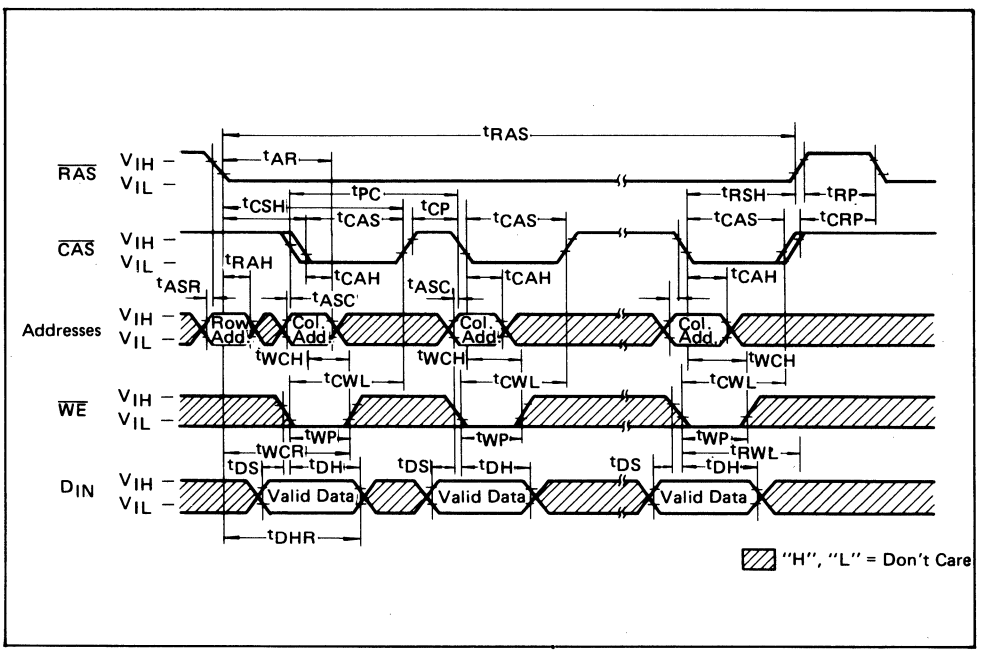
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



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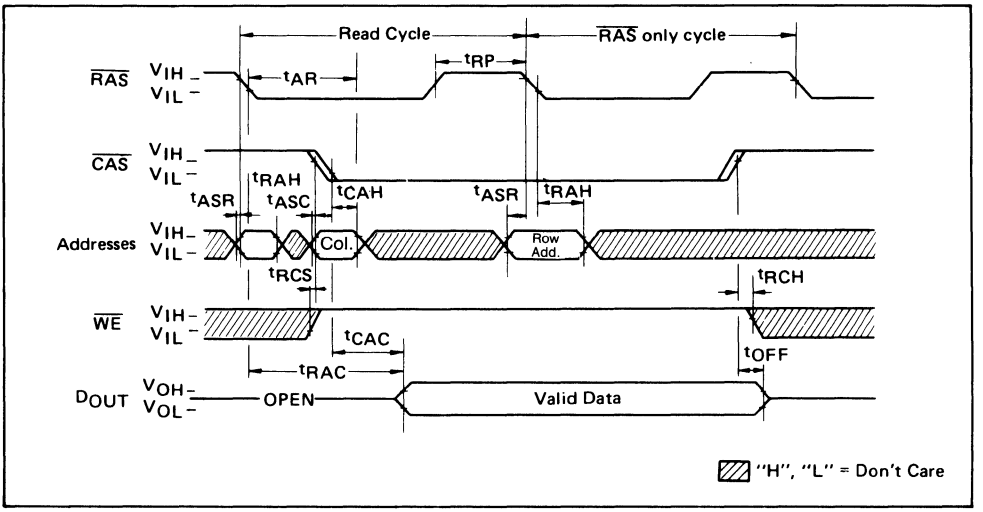
HIDDEN REFRESH



FUNCTIONAL DESCRIPTION

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262144 storage cell locations within the MSC2304. Nine row-address bits are established on the input pins ($A_0 \sim A_8$) and latched with the Row Address Strobe ($\overline{RAS}$). The Nine column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$, $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSC2304 during a write. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (Max.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (Max.). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSC2304 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

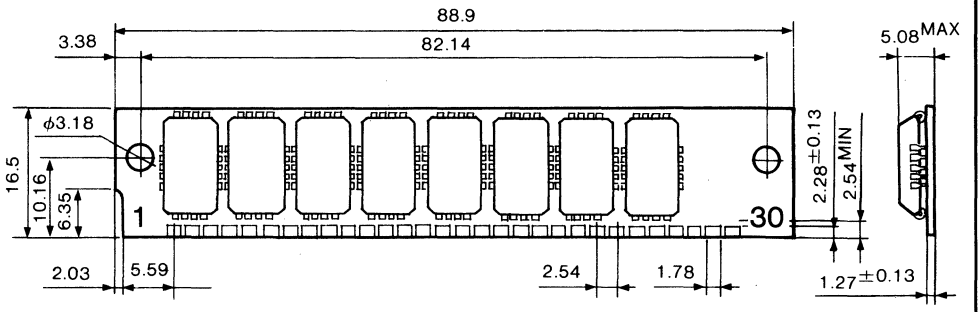
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses ($A_0 \sim A_7$) at least every four milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_8. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

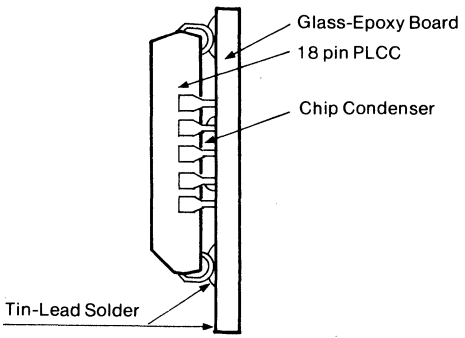
Hidden Refresh:

$\overline{RAS}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

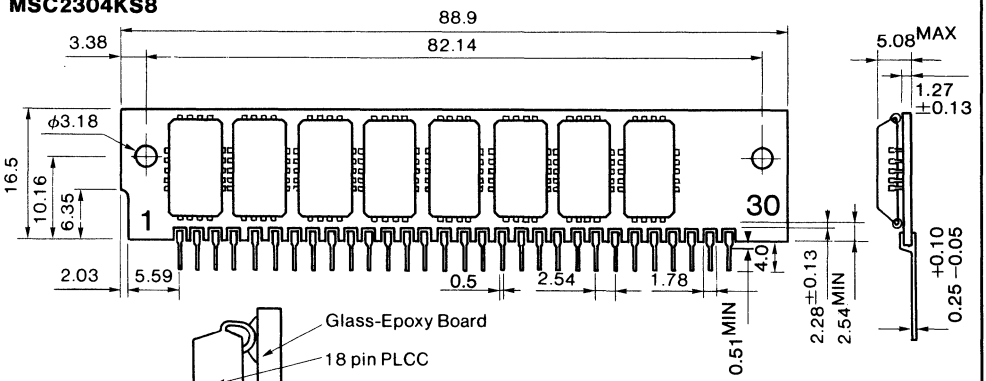
MSC2304YS8

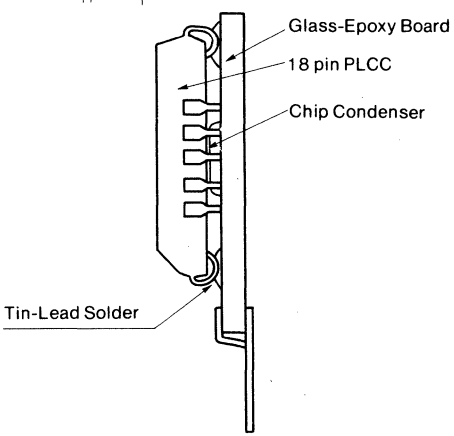




1. Substrate: GLASS-EPOXY
2. Through Hole: Copper Plating Followed by Sn/Pb Plating
3. Contact Pads: Copper Plating Followed by Sn/Pb Plating on Copper Film (18μm^t)
4. Surface Coating: Photo Film Resist

MSC2304KS8





1. Substrate: GLASS-EPOXY
2. Through Hole: Copper Plating Followed by Sn/Pb Plating
3. Contact Pads: Copper Plating Followed by Sn/Pb Plating on Copper Film (18μm^t)
4. Surface Coating: Photo Film Resist

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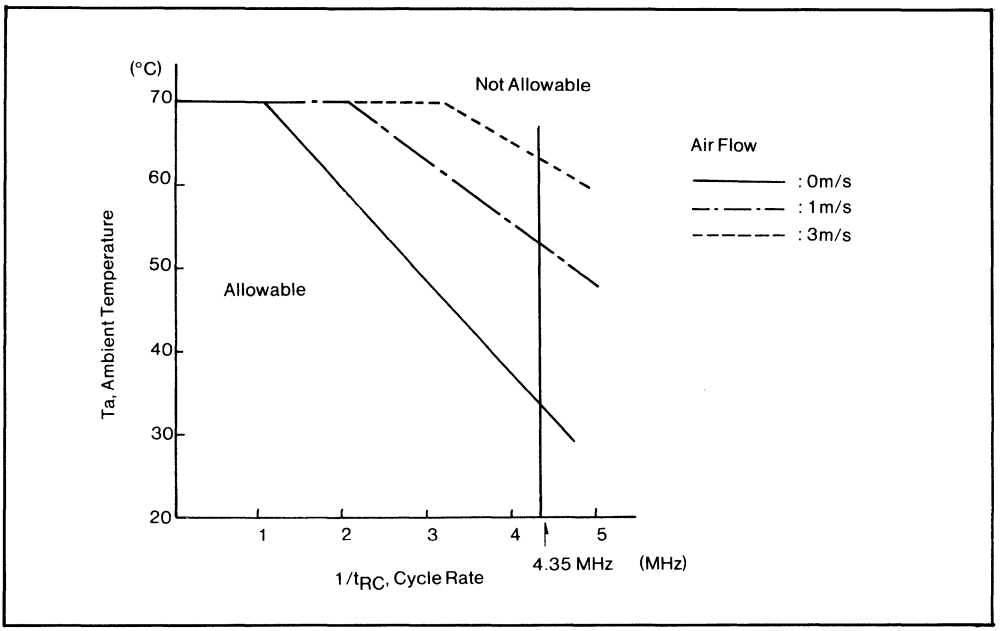
MSC2304YS8/KS8 (SIP/SIM) DERATING CURVE



MSC2304YS9/KS9

262,144 BY 9 BIT DYNAMIC RAM MODULE

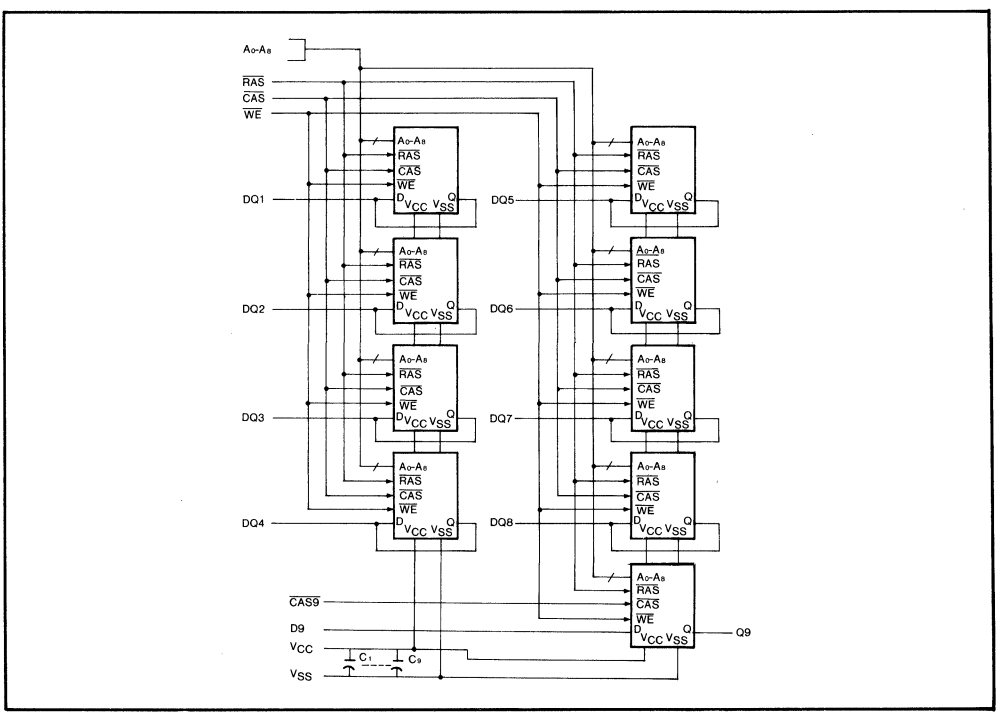
GENERAL DESCRIPTION

The Oki MSC2304YS9/KS9 is a fully decoded, 262,144 words × 9 bit NMOS dynamic random access memory composed of nine 256K DRAMs in plastic leaded chip carrier (MSM41256JS). The mounting of nine PLCCs together with nine 0.2μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2304YS9/KS9 are quite same as the original MSM41256JS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

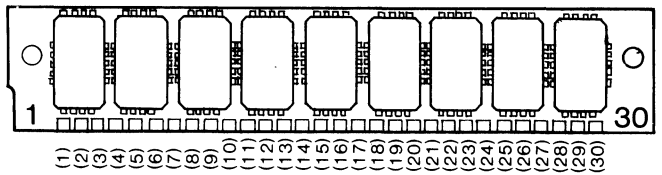
- 262,144 word × 9 bit Organization
- Single +5V Supply (10% Tolerance)
- 30-Pin Socket Insertable Module
- Refresh Period ... 4ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL compatible
- 3-States Outputs
- Common CAS Control for Eight Common Data-In and Data-Out Lines
- Separate CAS Control for One Separate Pair of Data-In and Data-Out Lines
- Row Access Time;
  120ns max. (MSC2304-12YS9/KS9)
  150ns max. (MSC2304-15YS9/KS9)
- Low Power Dissipation;
  3465mW max. (MSC2304-12YS9/KS9)
  3218mW max. (MSC2304-15YS9/KS9)
- Operating Temperature ... 0°C to 70°C

FUNCTIONAL BLOCK DIAGRAM

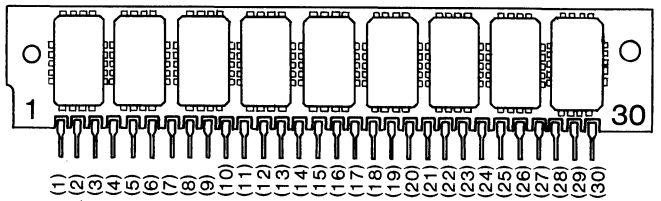


PIN ASSIGNMENT

MSC2304YS9



MSC2304KS9



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	V_{CC}	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ1	13	DQ4	23	DQ7
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ8
6	DQ2	16	DQ5	26	$\overline{Q9}$
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	NC	28	$\overline{CAS9}$
9	VSS	19	NC	29	D9
10	DQ3	20	DQ6	30	V_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−40 to +125	°C
Power dissipation	P_D	9	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	120ns MODULE		150ns MODULE		Unit
		Min.	Max.	Min.	Max.	
Operating Current* Average power supply current (RAS, CAS cycling; t_{RC} = min.)	I_{CC1}		630		585	mA
Standby Current Power supply current (RAS = CAS = V_{IH})	I_{CC2}		45		45	mA
Refresh Current Average power supply current (RAS cycling, CAS = V_{IH}; t_{RC} =min.)	I_{CC3}		495		450	mA
Page Mode Current* Average power supply current (RAS = V_{IL}, CAS cycling; t_{PC} =min.)	I_{CC4}		495		450	mA
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{L1}	−90	90	−90	90	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	−10	10	μA
Output Levels Output high voltage (I_{OH} = −5mA)	V_{OH}	2.4		2.4		V
Output low voltage (I_{OL} = 4.2mA)	V_{OL}		0.4		0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance ($A_0 \sim A_8$)	C_{IN1}	40	70	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	40	75	pF
Data Input/Output Capacitance (DQ)	C_{DQ}	7	20	pF
Input Capacitance ($\overline{CAS9}$)	C_{IN3}	5	10	pF
Input Capacitance (D9)	C_{IN4}	4	10	pF
Output Capacitance (Q9)	C_{OUT}	4	15	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

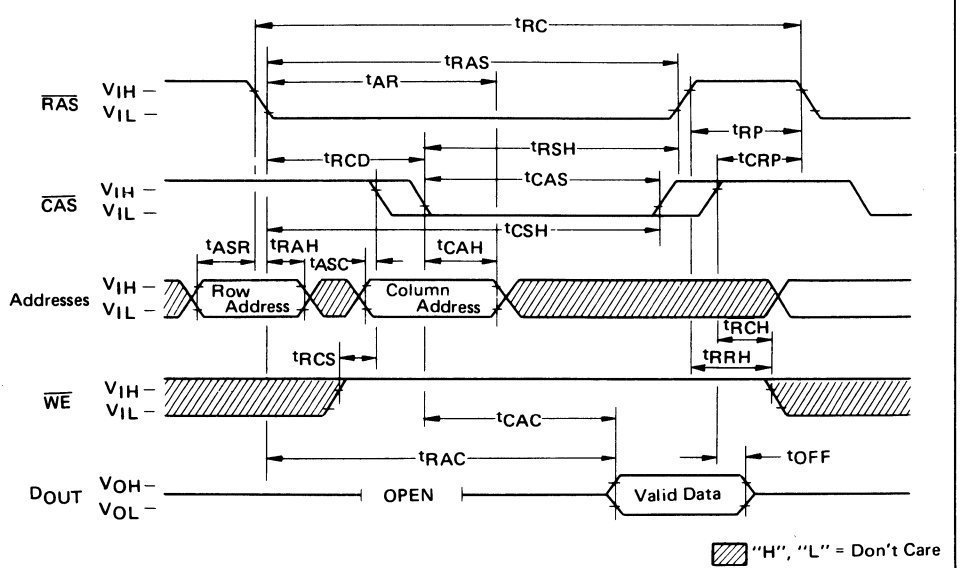
Parameter	Symbol	Units	MSC2304-12YS/KS		MSC2304-15YS/KS		Note
			Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4	
Random read or write cycle time	t_{RC}	ns	230		260		
Page mode cycle time	t_{PC}	ns	125		145		
Access time from $\overline{RAS}$	t_{RAC}	ns		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	40	0	40	
Transition time	t_T	ns	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	100		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	120	10,000	150	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	60		75		
$\overline{CAS}$ precharge time	t_{CP}	ns	55		60		
$\overline{CAS}$ pulse width	t_{CAS}	ns	60	10,000	75	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	120		150		

AC CHARACTERISTICS (CONT.)

Parameter	Symbol	Units	MSC2304-12YS/KS		MSC2304-15YS/KS		Note
			Min.	Max.	Min.	Max.	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	60	25	75	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		
Row Address set-up time	t_{ASR}	ns	0		0		
Row Address hold time	t_{RAH}	ns	15		20		
Column Address set-up time	t_{ASC}	ns	0		0		
Column Address hold time	t_{CAH}	ns	30		35		
Column Address hold time reference to $\overline{RAS}$	t_{AR}	ns	90		110		
Read command set-up time	t_{RCS}	ns	0		0		
Read command hold time	t_{RCH}	ns	0		0		
Write command set-up time	t_{WCS}	ns	0		0		
Write command hold time	t_{WCH}	ns	40		45		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	100		120		
Write command pulse width	t_{WP}	ns	40		45		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	40		45		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	40		45		
Data-in set-up time	t_{DS}	ns	0		0		
Data-in hold time	t_{DH}	ns	40		45		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	100		120		

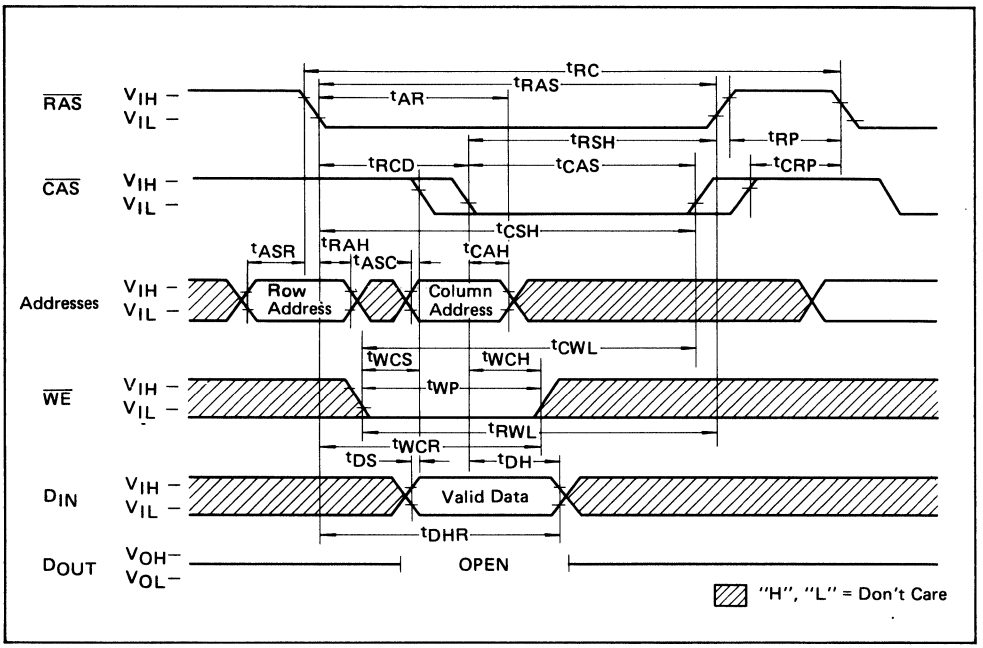
NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Examples; $\overline{RAS}$ only) before proper device operation is achieved.
2) AC measurements assume t_T = 5 ns.
3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4) Assumes that $t_{RCD} < t_{RCD}$ (max.).
If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
5) Assumes that $t_{RCD} < t_{RCD}$ (max.)
6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

READ CYCLE TIMING



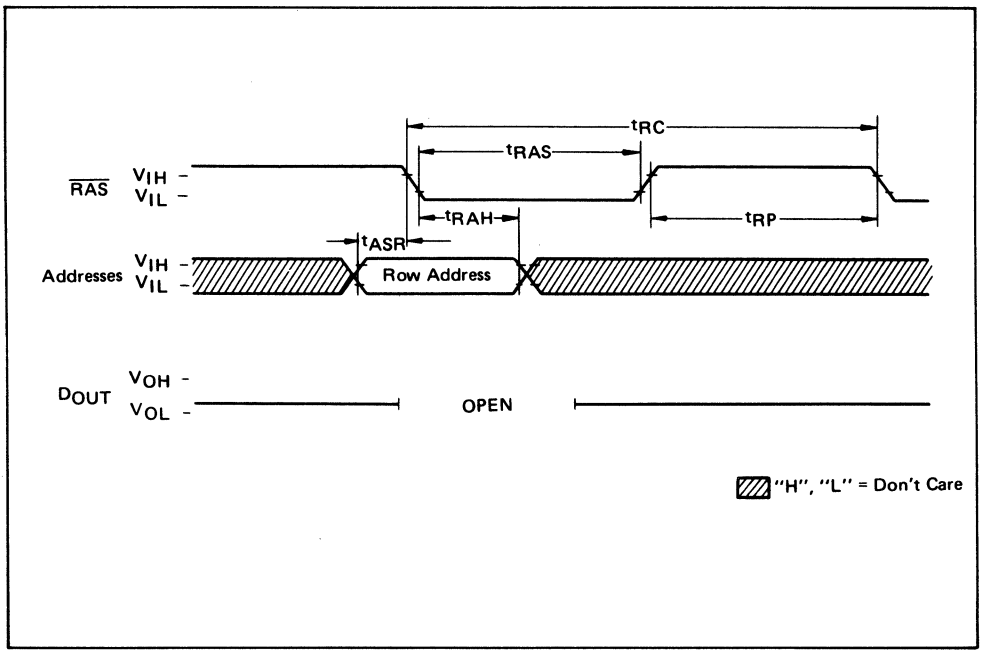
WRITE CYCLE TIMING

(EARLY WRITE)



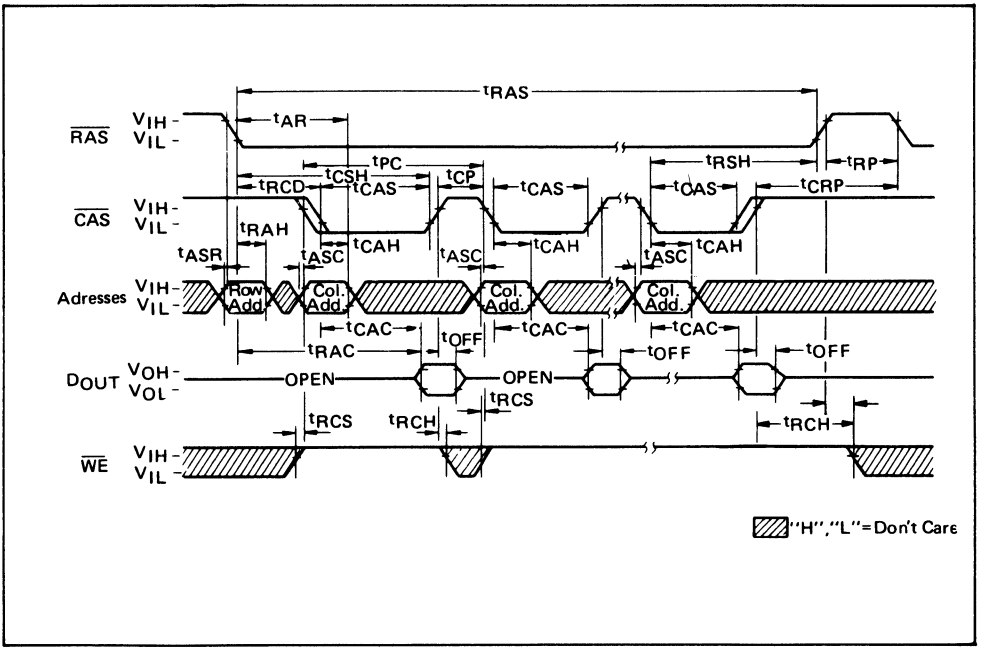
RAS ONLY REFRESH TIMING

(CAS: VIH, WE & DIN: Don't care)

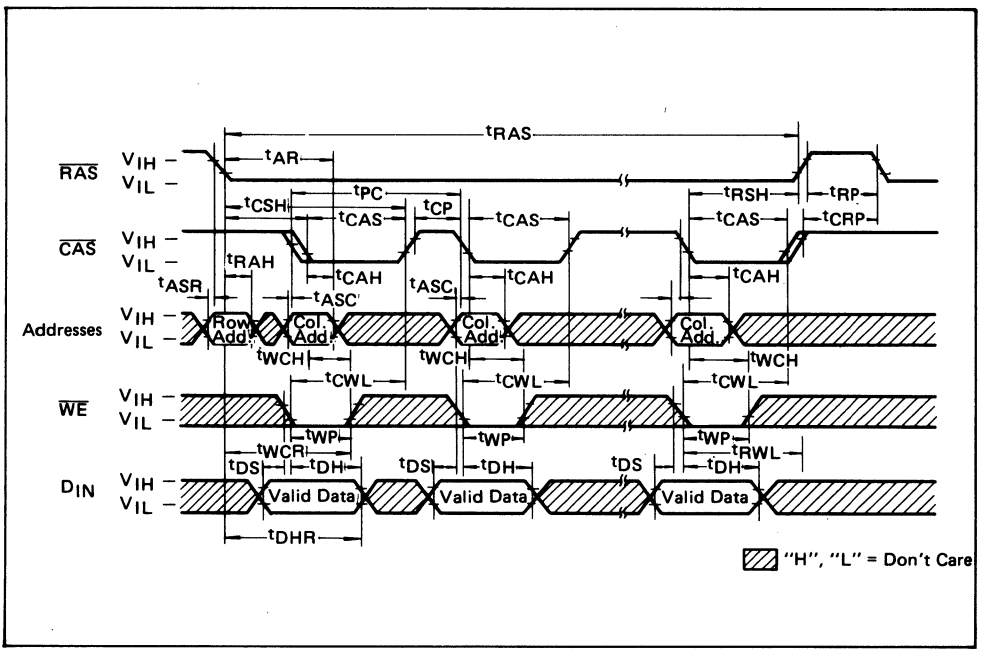


9

PAGE MODE READ CYCLE

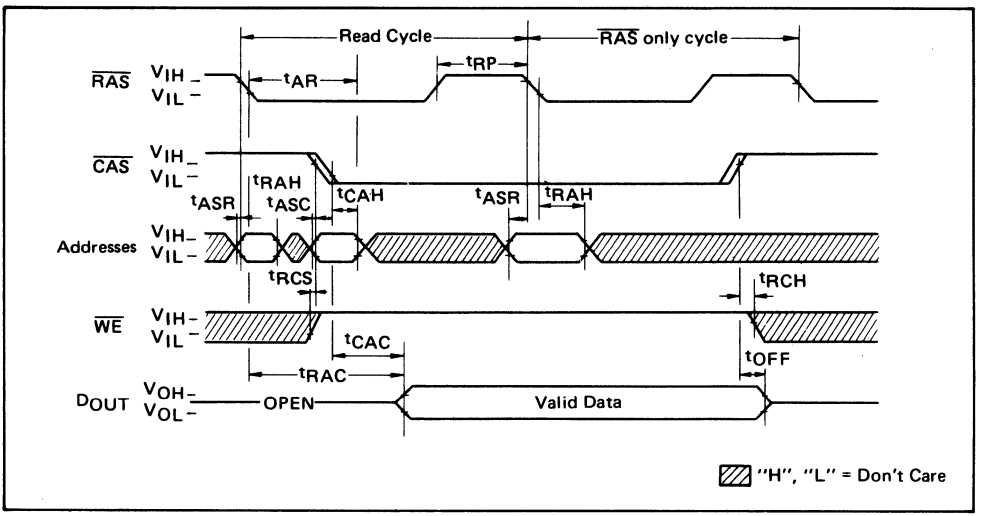


PAGE MODE WRITE CYCLE



9

HIDDEN REFRESH



FUNCTIONAL DESCRIPTION

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262144 storage cell locations within the MSC2304. Nine row-address bits are established on the input pins ($A_0 \sim A_8$) and latched with the Row Address Strobe ($\overline{RAS}$). The Nine column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$, $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the WE input. A logic high (1) on WE dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSC2304 during a write. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (Max.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (Max.). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSC2304 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

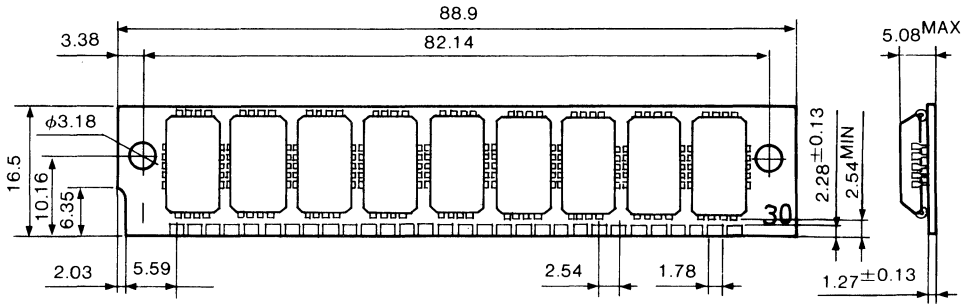
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses ($A_0 \sim A_7$) at least every four milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_8. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

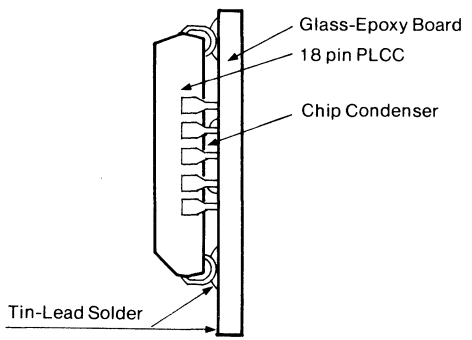
Hidden Refresh:

$\overline{RAS}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

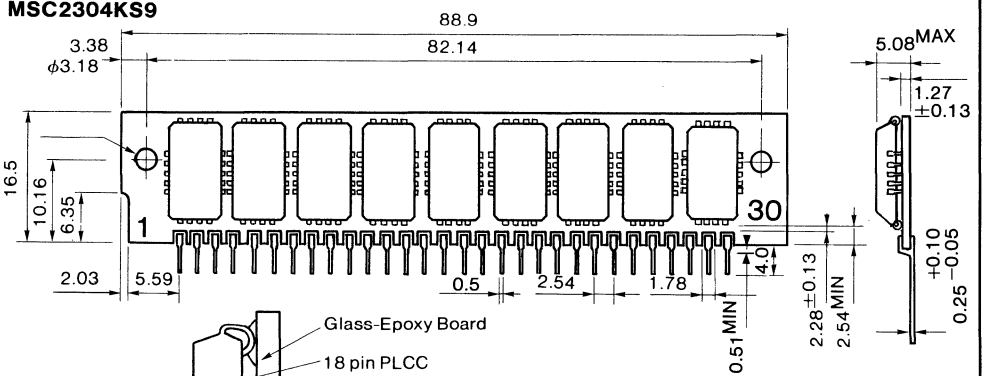
MSC2304YS9

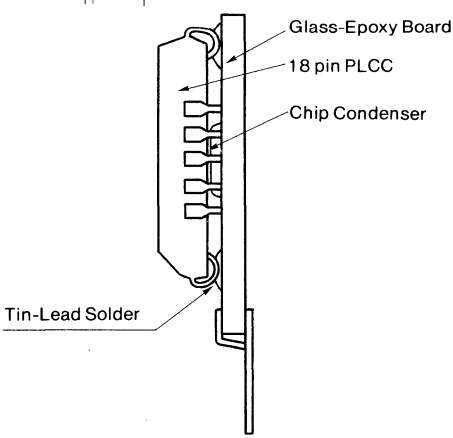




1. Substrate: GLASS-EPOXY
2. Through Hole: Copper Plating Followed by Sn/Pb Plating
3. Contact Pads: Copper Plating Followed by Sn/Pb Plating on Copper Film (18μm^t)
4. Surface Coating: Photo Film Resist

MSC2304KS9

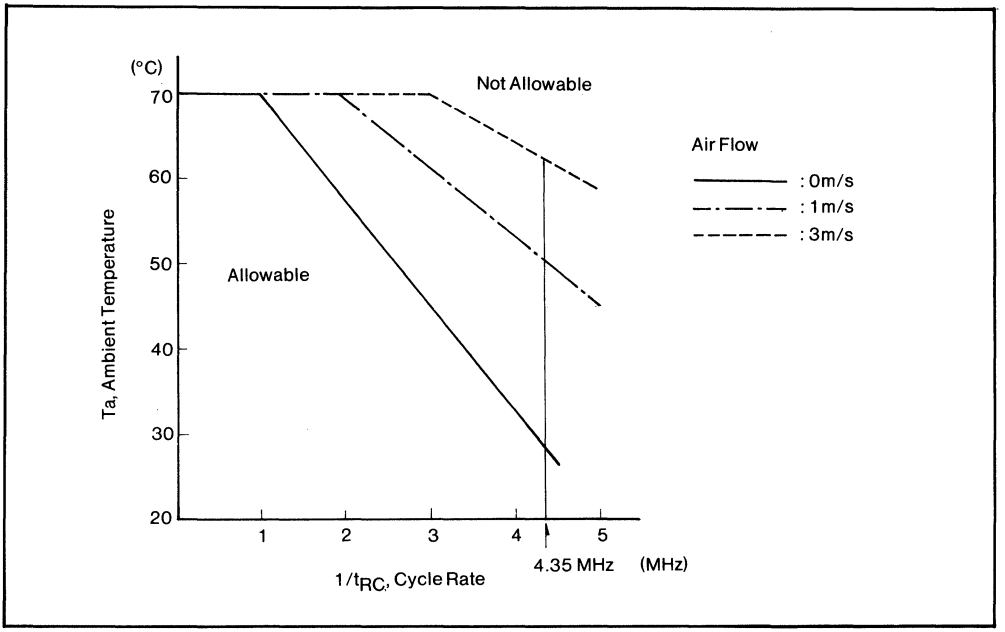




1. Substrate: GLASS-EPOXY
2. Through Hole: Copper Plating Followed by Sn/Pb Plating
3. Contact Pads: Copper Plating Followed by Sn/Pb Plating on Copper Film (18μm^t)
4. Surface Coating: Photo Film Resist

9

MSC2304YS9/KS9 (SIP/SIM) DERATING CURVE



MOS STATIC RAMS

9

OKI semiconductor

MSM5114RS

4096-BIT (1024 x 4) CMOS STATIC RAM

GENERAL DESCRIPTION

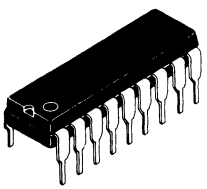
The Oki MSM5114 is a 4096-bit static Random Access Memory organized as 1024 words by 4 bits using Oki's reliable Silicon Gate CMOS technology. It uses fully static circuitry and therefore requires no clocks or refreshing to operate. Microwatt power dissipation typical of all CMOS is exhibited in all static states. Directly TTL compatible inputs, outputs and operation from a single +5V supply simplify system designs. Common data input/output pins using three-state outputs are provided.

The MSM5114 series is offered in an 18-pin plastic (RS suffix) package. The series is guaranteed for operation from 0°C to 70°C and over a 4V to 6V power supply range.

FEATURES

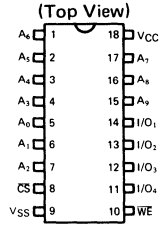
- Fully Static Operation
- Low Power Dissipation
  40μW Max. Standby Power
  192 mW/MHz Max. Operating Power
- Data Retention to V_{CC}=2V
- Single 4 ~ 6V Power Supply
- High Density 300-mil 18-Pin Package
- Common I/O Capability using Three-State Outputs
- Directly TTL/CMOS Compatible
- Silicon Gate CMOS Technology
- Interchangeable with Intel 2114L Devices

	5114-2	5114-3	5114
Max. Access Time (NS)	200	300	450
Max. Operating Power (MW/MHz)	192	192	192
Max. Standby Power (μW)	40	40	40



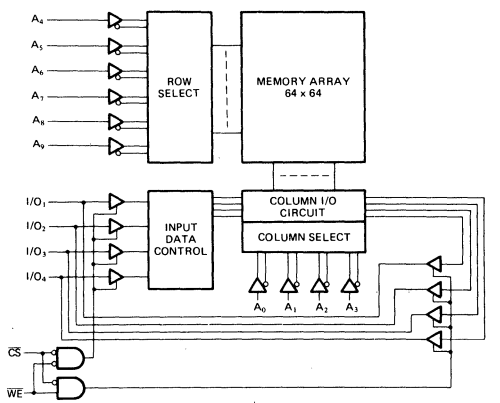
PIN CONFIGURATION

(Top View)



A_0 To A_9: Address Inputs
$\overline{WE}$: Write Enable
$\overline{CS}$: Chip Select
$I/O_1 \sim I/O_4$: Data Input/Output
V_{CC}: +5V Supply
VSS : Ground

FUNCTIONAL BLOCK DIAGRAM



$\overline{CS}$	$\overline{WE}$	I/O	Mode
H	X	Hi-Z	Not Selected
L	L	H	Write 1
L	L	L	Write 0
L	H	D-out	Read

9

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to VSS
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Data I/O Voltage	V_D	−0.3 to V_{CC} + 0.3	V	
Storage Temperature	T_{stg}	−55 to 150	°C	

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operations of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4	5	6	V	
Input Signal Level	V_{IH}	2.4	5	V_{CC}	V	5V ±10%
	V_{IL}	−0.3	0	0.8	V	
Operating Temperature	T_{opr}	0		70	°C	

DC CHARACTERISTICS

(V_{CC} = 5V ± 10%; Ta = 0°C to +70°C, unless otherwise noted.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Load Current	I_{LI}	−1		1	μA	V_{IN} = 0 to V_{CC}
Data I/O Leakage Current	I_{LO}	−1		1	μA	$V_{I/O}$ = 0 to V_{CC}
Output High Voltage	V_{OH}	2.4			V	I_{OUT} = −1.0 mA
Output Low Voltage	V_{OL}			0.4	V	I_{OUT} = 1.6 mA
Standby Supply Current	I_{CCS}		0.2	50	μA	V_{IN} = 0 or V_{CC}, $V_{\overline{CS}}$ = V_{CC}
Operating Supply Current	I_{CC}		19	35	mA	V_{IN} = 0 or V_{CC}, t_{RC} = 1 μs

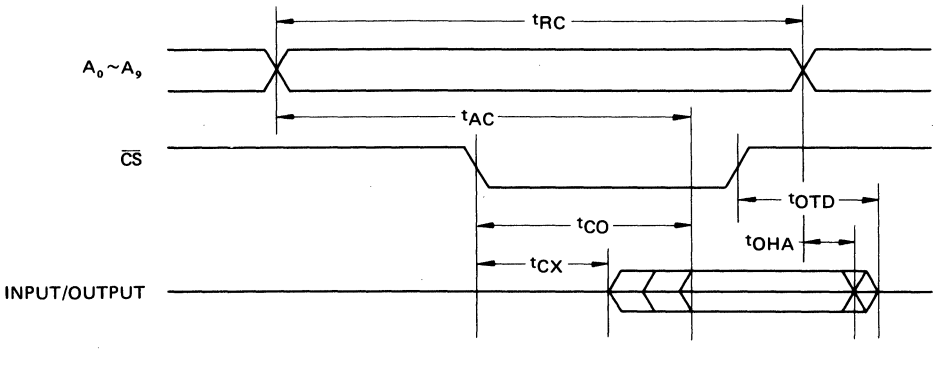
AC CHARACTERISTICS

READ CYCLE

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

Parameter	Symbol	5114-2		5114-3		5114		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	200		300		450		ns
Access Time	t_{AC}		200		300		450	ns
Chip Selection to Output Valid	t_{CO}		200		300		450	ns
Chip Selection to Output Active	t_{CX}	20		20		20		ns
Output 3-state from Deselection	t_{OTD}		60		80		100	ns
Output Hold from Address Change	t_{OHA}	10		10		10		ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CS}$ and high $\overline{WE}$.
2. Input Pulse levels: 0.8V to +2.4V
3. Input Rise and Fail Time: 10 ns
4. Timing Measurement Reference Levels: 1.5V
5. Output Load: 1 TTL Gate and C_L = 50 pF

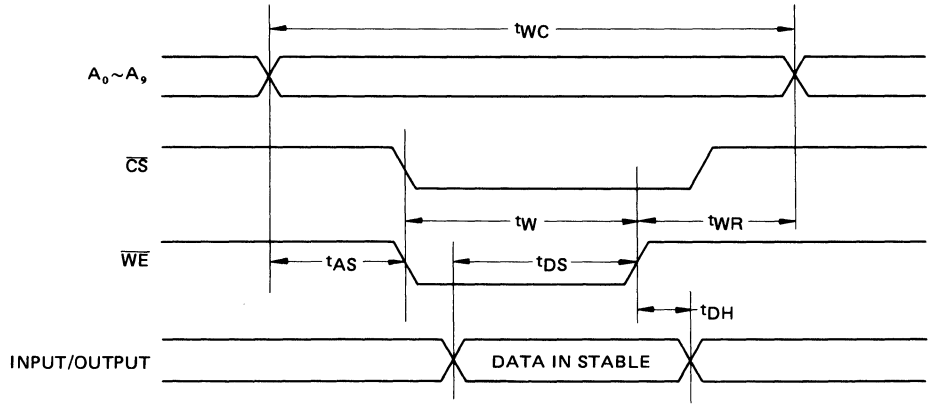
9

WRITE CYCLE

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

Parameter	Symbol	5114-2		5114-3		5114		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	200		300		450		ns
Write Time	t_W	150		190		250		ns
Write Release Time	t_{WR}	20		30		50		ns
Address Setup Time	t_{AS}	20		20		20		ns
Data Setup Time	t_{DS}	120		150		200		ns
Data Hold From Write Time	t_{DH}	10		10		10		ns

WRITE CYCLE



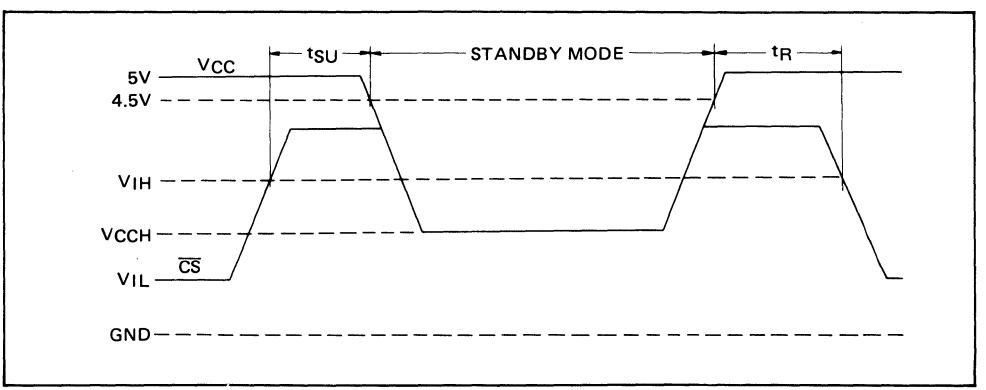
Notes:
1. A Write occurs during the overlap of a low $\overline{CS}$ and low $\overline{WE}$.
2. Input Pulse Levels: 0.8V to +2.4V
3. Input Rise and Fall Time: 10 ns
4. Timing Measurement Reference Levels: 1.5V
5. t_W: Overlap time of a low $\overline{CS}$ and low $\overline{WE}$.
6. t_{AS}: Low $\overline{WE}$ from address or low $\overline{CS}$ from address
7. t_{WR}, t_{DS} and t_{DH} are defined from High CS or High $\overline{WE}$, whichever occurs first.

LOW V_{CC} DATA RETENTION CHARACTERISTICS

(T_a = 0°C to +70°C, unless otherwise noted.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2			V	V_{IN} = 0 or V_{CC}, $V_{\overline{CS}} = V_{CC}$
Data Retention Current	I_{CCH}		0.1	20	μA	V_{CC} = 2V $V_{CS} = V_{CC}$ V_{IN} = 0V or V_{CC}
$\overline{CS}$ to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	t_{RC}			ns	

LOW V_{CC} DATA RETENTION WAVEFORM



9

CAPACITANCE

($T_a = 25°C$, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			10	pF
Input Capacitance	C_{IN}			8	pF

Note: This parameter is periodically sampled and not 100% tested.

OKI semiconductor

MSM2128RS

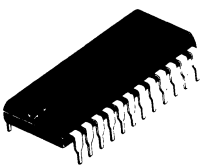
2 KW x 8 BIT STATIC RAM

GENERAL DESCRIPTION

The OKI MSM2128 is a 16384 bits static Random Access Memory organized as 2048 words by 8 bits using Advanced N-channel Silicon Gate MOS technology. It uses fully static circuitry throughout and no clocks or refresh are required. The reduced standby power dissipation is automatically performed by CS control. Single +5 V Power supply. All inputs and outputs are directly TTL compatible. Common data I/O using three-state outputs. The 24 pin package is pin compatible with standard 16 K UV Erasable Programmable ROM.

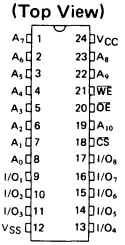
FEATURES

- Single power supply
- External clock and refresh operation not required
- Access time
  - MSM2128-12RS . . . 120ns (max)
  - MSM2128-15RS . . . 150ns (max)
  - MSM2128-20RS . . . 200ns (max)
- Low power dissipation
  - during operation . . . MSM2128-15RS/20RS . . . 550 mW (max)
  - . . . MSM2128-12RS . . . 660 mW (max)
  - during standby . . . 110 mW (max)
- TTL compatible I/O
- Three-state I/O
- Common data I/O capability
- Power down mode using chip select signal
- Convertibility of pins used in 16KEPROM MSM2716



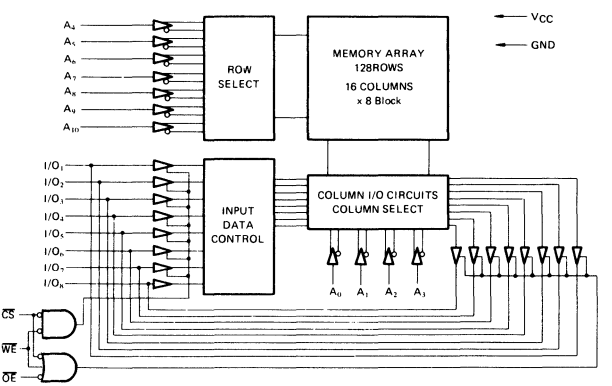
PIN CONFIGURATION

(Top View)



$A_0 \sim A_{10}$: Address Inputs
$I/O_1 \sim I/O_8$: Data Input/Output
V_{CC}: Power (5V)
V_{SS}: Ground
$\overline{WE}$: Write Enable
$\overline{CS}$: Chip Select
$\overline{OE}$: Output Enable

FUNCTIONAL BLOCK DIAGRAM



9

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_{IN}	−0.5 to 7	V	
Operating Temperature	Topr	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	

DC AND OPERATING CHARACTERISTICS

(T_a = 0°C to + 70°C, V_{CC} = 5V ±10%, unless otherwise notes.)

Parameter	Symbol	2128-12RS			2128-15/20RS			Unit	Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Input Load Current	I_{LI}	−10		10	−10		10	μA	V_{CC} = Max. V_{IN} = GND to V_{CC}
Output Leakage Current	I_{LO}	−10		10	−10		10	μA	$\overline{CS}$ = $\overline{OE}$ = V_{IH}, V_{CC} = Max. V_{out} = GND to V_{CC}
Operating Current	I_{CC}			120			100	mA	V_{CC} = Max. $\overline{CS}$ = V_{IL} I I/O = 0 mA t_{cyc} = Min.
Standby Current	I_{SB}			15			15	mA	V_{CC} = Min. to Max. $\overline{CS}$ = V_{IH}
Peak Power-on Current	I_{SBP}			20			20	mA	V_{CC} = GND to V_{CC} = Min. $\overline{CS}$ = Lower of V_{CC} or V_{IH}
Input Voltage	V_{IH}	2	5	6	2	5	6	V	Respect to V_{SS}
	V_{IL}	−0.5	0	0.8	−0.5	0	0.8	V	
Output Voltage	V_{OH}	2.4		V_{CC}	2.4		V_{CC}	V	I_{OH} = −1.0 mA
	V_{OL}			0.4			0.4	V	I_{OL} = 2.1 mA

Notes 1. Typical limits are at V_{CC} = 5V, T_a = 25°C, and specified loading.

9

AC CHARACTERISTICS

(T_a = 0°C to + 70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

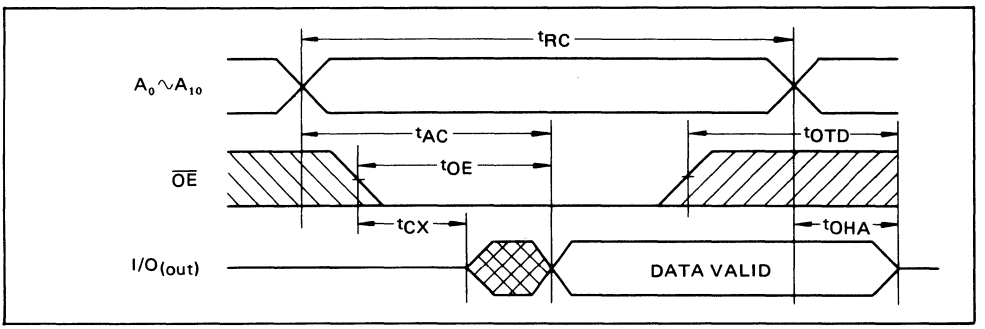
AC TEST CONDITIONS

Parameter	Conditions
Input High Level	2.0V
Input Low Level	0.8V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	C_L = 100 pF, 1TTL Gate

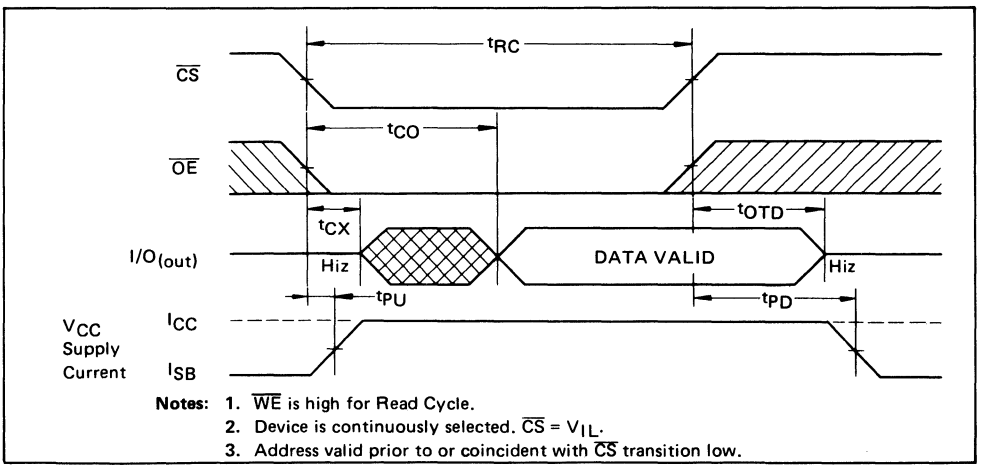
READ CYCLE [1]

Parameter	Symbol	2128-12RS		2128-15RS		2128-20RS		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	120		150		200		ns	
Address Access Time	t_{AC}		120		150		200	ns	
Output Enable to Output Delay	t_{OE}		50		60		70	ns	
Chip Select Access Time	t_{CO}		120		150		200	ns	
Chip Selection to Output in Low Z	t_{CX}[2]	10		10		10		ns	
Chip Selection to Output in High Z	t_{OTD}[3]	0	40	0	50	0	60	ns	
Output Hold from Address Time	t_{OHA}	10		10		10		ns	
Chip Select to Power Up Time	t_{PU}	0		0		0		ns	
Chip Select to Power Down Time	t_{PD}		50		60		80	ns	

READ CYCLE NO. 1 [8] [9]



READ CYCLE NO. 2 [8] [10]



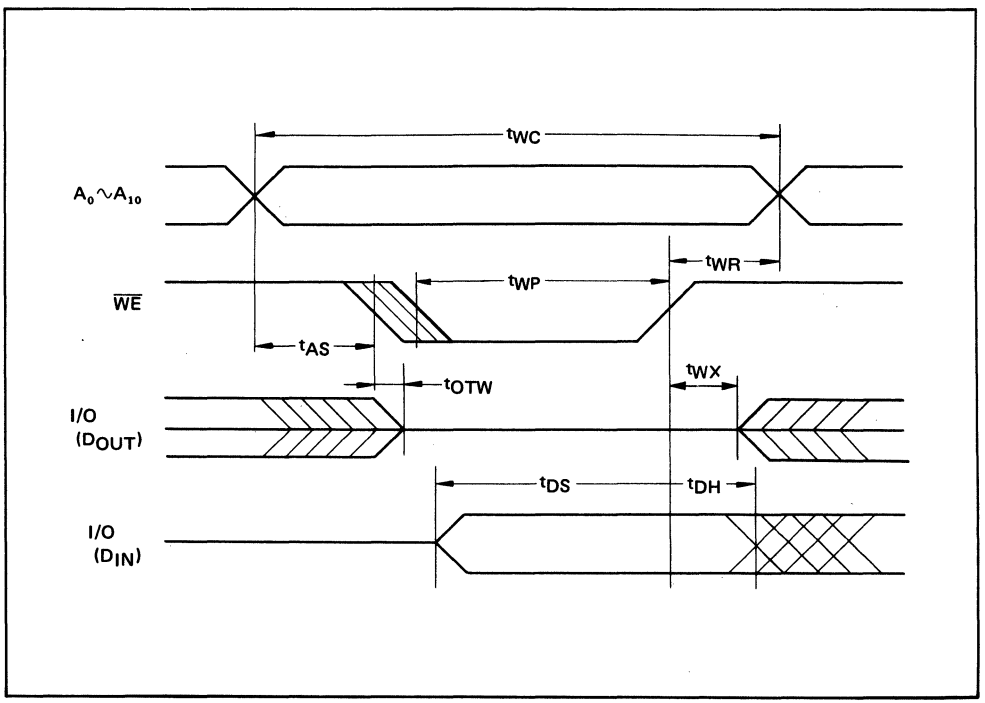
Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

WRITE CYCLE (4)(5)

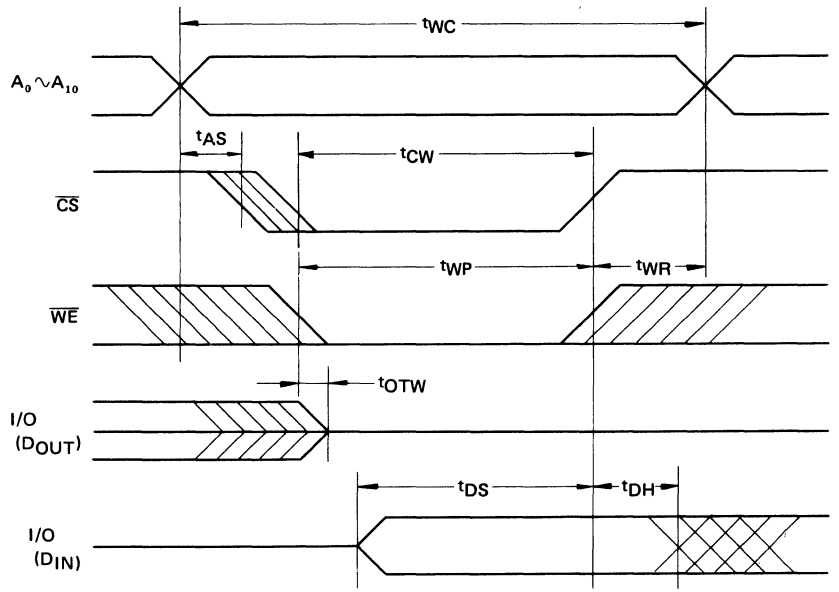
Parameter	Symbol	2128-12RS		2128-15RS		2128-20RS		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	120		150		200		ns	
Chip Selection to End of Write	t_{CW}	90		120		150		ns	
Address Setup Time	t_{AS}	20		20		20		ns	
Write Pulse Width	t_{WP}	60		80		100		ns	
Write Recovery Time	t_{WR}(6)	10		10		10		ns	
Data Valid to End of Write	t_{DS}(6)	50		70		90		ns	
Data Hold Time	t_{DH}(6)	10		15		15		ns	
Write Enabled to Output in High Z	t_{OTW}(7)	0	40	0	50	0	60	ns	
Output Active from End of White	t_{WX}	5		5		5		ns	

Notes
1. A read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CX} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs last.
3. t_{OTD} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs first.
4. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
5. $\overline{OE}$ may be allowed in a Write Cycle both high and low.
6. t_{WR}, t_{DS}, and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
7. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.

WRITE CYCLE NO. 1(11)(13)



WRITE CYCLE NO. 2[12][13]



Notes 1. $\overline{WE}$ control mode
2. $\overline{CS}$ control mode
3. When I/O pins are Data output mode, don't force inverse signal to these pins.

FUNCTION TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	Output	Power
H	X	X	Not Selected	High Z	Standby
L	L	X	Write	High Z	Active
L	H	L	Read	D_{OUT}	Active
L	H	H	Not Selected	High Z	Active

CAPACITANCE

(T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Max.	Unit	Conditions
Input/Output Capacitance	$C_{I/O}$		8	pF	$V_{I/O}$ = 0V
Input Capacitance	C_{IN}		6	pF	V_{IN} = 0V

Note: This parameter is periodically sampled and not 100% tested.

OKI semiconductor

MSM5128RS

2048-WORD x 8-BIT C-MOS STATIC RAM

GENERAL DESCRIPTION

The MSM5128RS is a 2048-word by 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM5128RS is also a CMOS silicon gate device which requires very little power during standby (maximum standby current of 50μA) when there is no chip selection. Stored data is retained if the power voltage drops to 2V, thereby enabling battery back-up.

A byte system is adopted, and since there is pin compatibility with standard ultra-violet EPROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, $\overline{CS}$ and $\overline{OE}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

FEATURES

- Single 5V Supply
- Battery Back-up at 2V
- Operating temperature range Ta = −40°C to +85°C
- Low Power Dissipation

  Standby;

5128-20	5128-12/15
1.0 μA MAX Ta = 25°C	0.3 μA MAX Ta = 25°C
10 μA MAX Ta = 60°C	1.0 μA MAX Ta = 60°C
50 μA MAX Ta = 85°C	

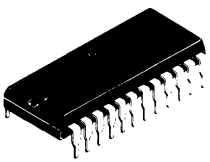
  Operation;

  200 mW TYP
- High Speed (Equal Access and Cycle Time)

  MSM5128-12/15/20; 120 ns/150 ns/200 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- Pin Compatible with

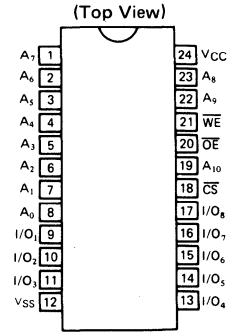
  16K EPROM (MSM2716)

  16K NMOS SRAM (MSM2128)



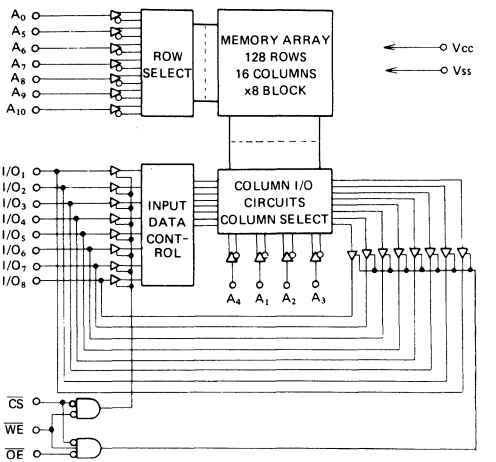
PIN CONFIGURATION

(Top View)



$A_0 \sim A_{10}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data Input/Output
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS}: Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



9

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	High Z
Read	L	H	H	High Z
	L	H	L	D_{OUT}
Write	L	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Operating Temperature	T_{opr}	−40 to 85	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	Ta = 25°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Data Retention Voltage	V_{CCH}	2	5	5.5	V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	5V ± 10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

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DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_a = −40°C to +85°C)

Parameter	Symbol		MSM5128-12			MSM5128-15			MSM5128-20			Unit	Test Condition	
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Input Leakage Current	I_{LI}		−1		1	−1		1	−1		1	μA	V_{IN} = 0 to V_{CC}	
Output Leakage Current	I_{LO}		−1		1	−1		1	−1		1	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}	
Output Voltage	V_{OH}		2.4			2.4			2.4			V	I_{OH} = −1 mA	
	V_{OL}				0.4			0.4			0.4	V	I_{OL} = 4 mA (5128-12) I_{OL} = 2.1 mA (5128-15/20)	
Standby Supply Current	I_{CCS}	Ta										μA	$\overline{CS} \geqq V_{CC}$ − 0.2V V_{IN} = 0 to V_{CC}	
		25°C			0.2			0.2		0.1	1.0			
		60°C			1.0			1.0			10			
		85°C									50			
	I_{CCS1}			0.3	1		0.3	1		0.3	1	mA	$\overline{CS}$ = V_{IH} t_{cyc} = Min. cycle	
Operating Supply Current	I_{CCA}			40	60		37	55		35	50	mA	Min. cycle	Ta = 0~85°C
				40	72		37	66		35	60	mA		Ta=−40~85°C

AC CHARACTERISTICS

Test Condition

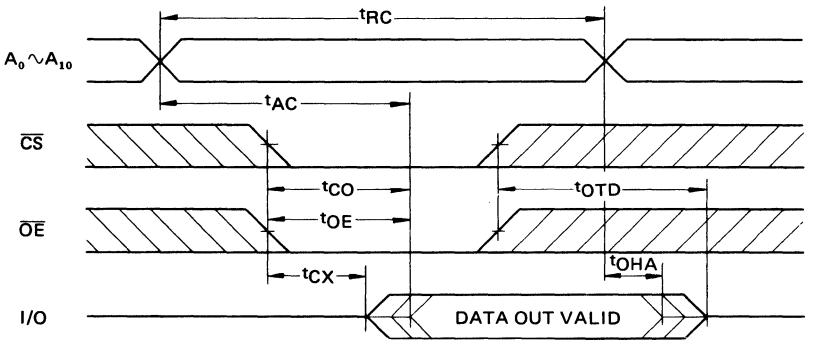
Parameter	Conditions
Input Pulse Level	V_{IH}=2.2V, V_{IL}=0.8V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L=100 pF, 1 TTL Gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_a = −40°C to +85°C)

Parameter	Symbol	MSM5128-12		MSM5128-15		MSM5128-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	120		150		200		ns
Address Access Time	t_{AC}		120		150		200	ns
Chip Select Access Time	t_{CO}		120		150		200	ns
Output Enable to Output Valid	t_{OE}		80		100		120	ns
Chip Selection to Output Active	t_{CX}	10		15		20		ns
Output Hold Time From Address Change	t_{OHA}	10		15		20		ns
Output 3-state from Deselection	t_{OTD}	0	50	0	50	0	60	ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CX} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs last.
3. t_{OTD} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs first.
4. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.

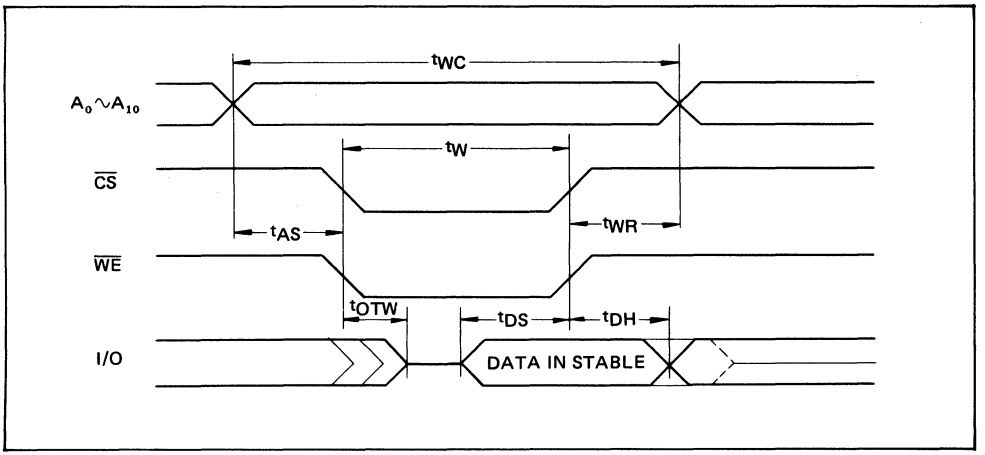
WRITE CYCLE

(V_{CC} = 5V ± 10%, T_a = −40°C to +85°C)

Parameter	Symbol	MSM5128-12		MSM5128-15		MSM5128-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	120		150		200		ns
Address to Write Setup Time	t_{AS}	15		20		20		ns
Write Time	t_W	70		90		120		ns
Write Recovery Time	t_{WR}	15		20		20		ns
Data Setup Time	t_{DS}	50		60		80		ns
Data Hold from Write Time	t_{DH}	5		10		10		ns
Output 3-State from Write	t_{OTW}		50		50		60	ns

Notes: 1. A Write Cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CS}$ and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

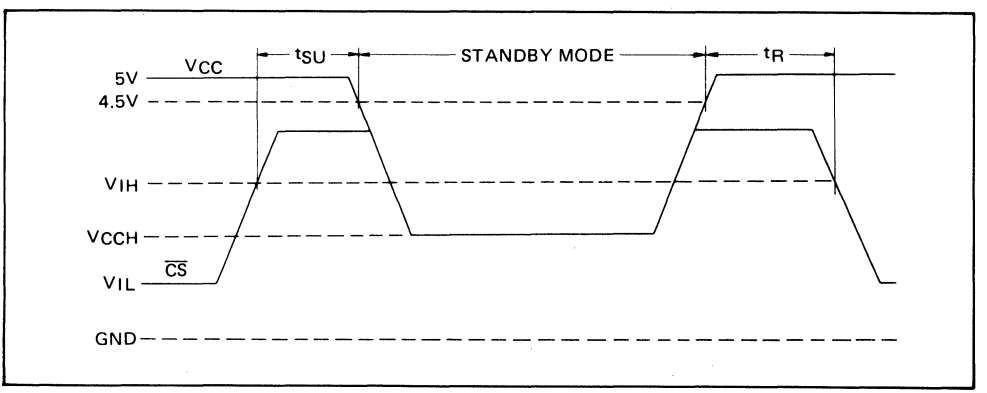
WRITE CYCLE



LOW V_{CC} DATA RETENTION CHARACTERISTICS

(T_a = −40°C to +85°C, unless otherwise noted)

Parameter	Symbol		5128-12/15 MIN	5128-12/15 MAX	5128-20 MIN	5128-20 MAX	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}		2		2		V	V_{IN} = 0V to V_{CC}, CS = V_{CC}
Data Retention Current	I_{CCH}	25°C		0.2		0.5	μA	V_{CC} = 2V CS = V_{CC} V_{IN} = 0V to V_{CC}
		60°C		1.0				
		85°C				20		
CS to Data Retention Time	t_{SU}		0		0		ns	
Operation Recovery Time	t_R		t_{RC}		t_{RC}		ns	



CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			8	pF
Input Capacitance	C_{IN}			6	pF

Note: This parameter is periodically sampled and not 100% tested.

OKI semiconductor

MSM5128-20GSK

2048-WORD x 8-BIT C-MOS STATIC RAM (E3-S-013-32)

GENERAL DESCRIPTION

The MSM5128GS is a 2048-word by 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM5128GS is also a CMOS silicon gate device which requires very little power during standby (maximum standby current of 50μA) when there is no chip selection. Stored data is retained if the power voltage drops to 2V, thereby enabling battery back-up.

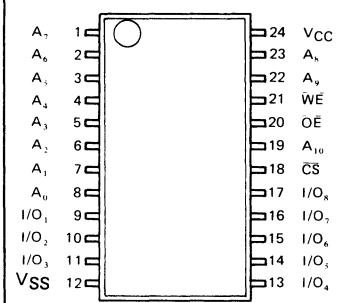
A byte system is adopted, and since there is pin compatibility with standard ultra-violet EPROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, $\overline{CS}$ and $\overline{OE}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

FEATURES

- Single 5V Supply
- Battery Back-up at 2V
- Operating temperature range Ta = −40°C to +85°C
- Low Power Dissipation
  - Standby; 1.0 μA MAX Ta = 25°C
    10 μA MAX Ta = 60°C
    50 μA MAX Ta = 85°C
  - Operation; 200 mW TYP
- High Speed (Equal Access and Cycle Time)
  MSM5128-20; 200 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- 24 Pin Flat PKG

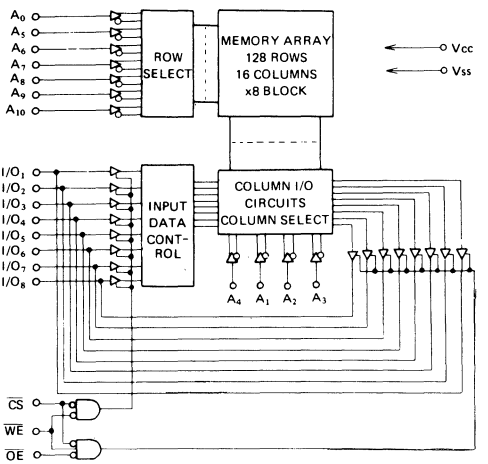
PIN CONFIGURATION

(Top View)



$A_0 \sim A_{10}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data Input/Output
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS}: Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



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TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	High Z
Read	L	H	H	High Z
	L	H	L	D_{OUT}
Write	L	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Operating Temperature	T_{opr}	−40 to 85	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	Ta = 25°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Data Retention Voltage	V_{CCH}	2	5	5.5	V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	5V ± 10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

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DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_a = −40°C to +85°C)

Parameter	Symbol		MSM5128-20 Min.	MSM5128-20 Typ.	MSM5128-20 Max.	Unit	Test Condition	
Input Leakage Current	I_{LI}		−1		1	μA	V_{IN} = 0 to V_{CC}	
Output Leakage Current	I_{LO}		−1		1	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}	
	V_{OH}		2.4			V	I_{OH} = −1 mA	
Output Voltage	V_{OL}				0.4	V	I_{OL} = 2.1 mA	
Standby Supply Current	I_{CCS}	Ta 25°C		0.1	1.0	μA	$\overline{CS} \geqq V_{CC}$ − 0.2V V_{IN} = 0 to V_{CC}	
		60°C			10			
		85°C			50			
	I_{CCS1}			0.3	1	mA	$\overline{CS}$ = V_{IH} t_{cyc} = Min. cycle	
Operating Supply Current	I_{CCA}			35	50	mA	Min. cycle	Ta = 0 ~ 85°C
				35	60	mA		Ta = −40 ~ 85°C

AC CHARACTERISTICS

Test Condition

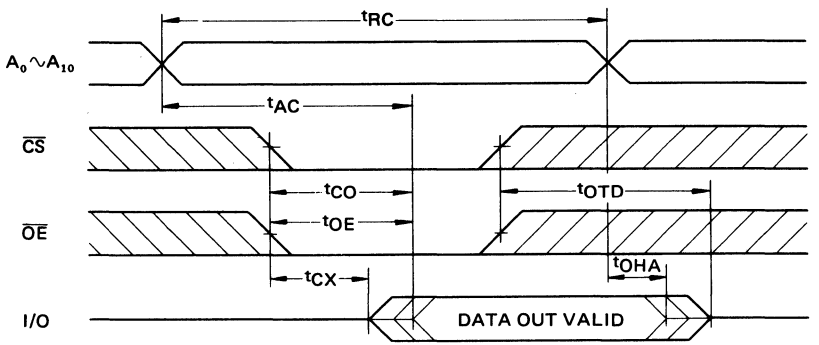
Parameter	Conditions
Input Pulse Level	V_{IH}=2.2V, V_{IL}=0.8V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L=100 pF, 1 TTL Gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_a = −40°C to +85°C)

Parameter	Symbol	MSM5128-20 Min.	MSM5128-20 Max.	Unit
Read Cycle Time	t_{RC}	200		ns
Address Access Time	t_{AC}		200	ns
Chip Select Access Time	t_{CO}		200	ns
Output Enable to Output Valid	t_{OE}		120	ns
Chip Selection to Output Active	t_{CX}	20		ns
Output Hold Time from Address Change	t_{OHA}	20		ns
Output 3-state from Deselection	t_{OTD}	0	60	ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CX} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs last.
3. t_{OTD} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs first.
4. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.

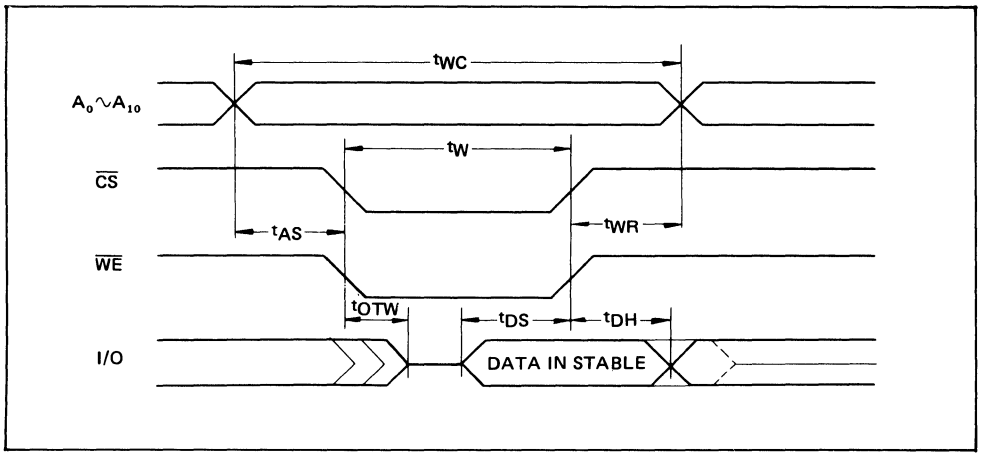
WRITE CYCLE

(V_{CC} = 5V ± 10%, T_a = −40°C to +85°C)

Parameter	Symbol	MSM5128-20		Unit
		Min.	Max.	
Write Cycle Time	t_{WC}	200		ns
Address to Write Setup Time	t_{AS}	20		ns
Write Time	t_W	120		ns
Write Recovery Time	t_{WR}	20		ns
Data Setup Time	t_{DS}	80		ns
Data Hold from Write Time	t_{DH}	10		ns
Output 3-State from Write	t_{OTW}		60	ns

Notes: 1. A Write Cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CS}$ and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

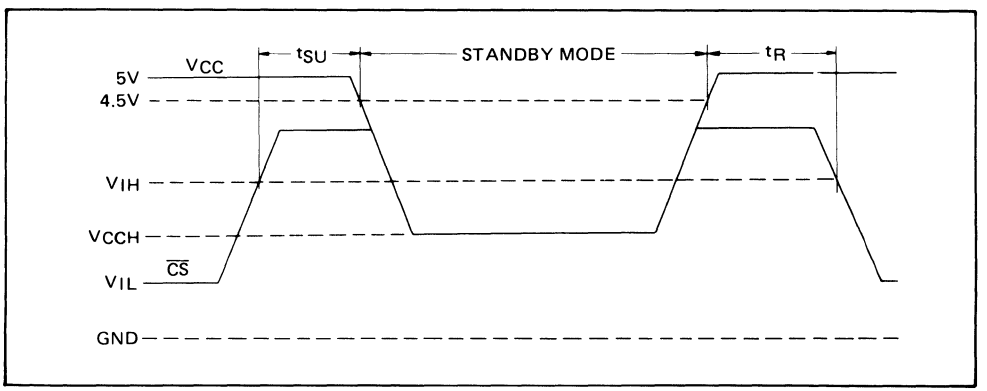
WRITE CYCLE



LOW V_{CC} DATA RETENTION CHARACTERISTICS

(T_a = -40°C to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2			V	V_{IN} = 0V to V_{CC}, $\overline{CS}$ = V_{CC}
Data Retention Current	I_{CCH}		0.05	20	μA	V_{CC} = 2V $\overline{CS}$ = V_{CC} V_{IN} = 0V to V_{CC}
$\overline{CS}$ to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	t_{RC}			ns	



CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			8	pF
Input Capacitance	C_{IN}			6	pF

Note: This parameter is periodically sampled and not 100% tested.

OKI semiconductor

MSM5126RS

2048-WORD x 8-BIT C-MOS STATIC RAM (E3-S-014-32)

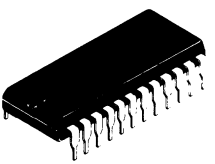
GENERAL DESCRIPTION

The MSM5126RS is a 2048-word by 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM5126RS is also a CMOS silicon gate device which requires very little power during standby (maximum standby current of 30μA) when there is no chip selection. Stored data is retained if the power voltage drops to 2V, thereby enabling battery back-up.

A byte system is adopted, and since there is pin compatibility with standard ultra-violet EPROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, $\overline{CS}$ and $\overline{OE}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

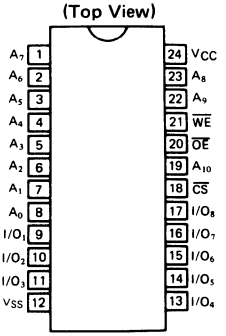
FEATURES

- Single 5V Supply
- Battery Back-up at 2V
- Operating temperature range Ta = −30°C to +85°C
- Low Power Dissipation
  - Standby; 1.0 μA MAX T_a = 25°C
    5.0 μA MAX T_a = 60°C
    30 μA MAX T_a = 85°C
  - Operation; 200 mW TYP
- High Speed (Equal Access and Cycle Time)
  MSM5126-20/25; 200 ns/250 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- Pin Compatible with
  16K EPROM (MSM2716)
  16K NMOS SRAM (MSM2128)



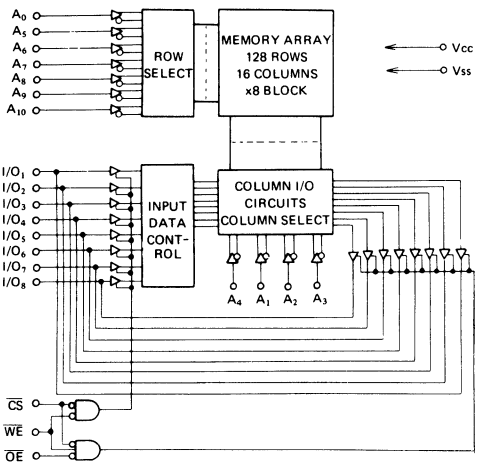
PIN CONFIGURATION

(Top View)



$A_0 \sim A_{10}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data Input/Output
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS}: Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



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TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	High Z
Read	L	H	H	High Z
	L	H	L	D_{OUT}
Write	L	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Operating Temperature	T_{opr}	−30 to 85	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	Ta = 25°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Data Retention Voltage	V_{CCH}	2	5	5.5	V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	5V ±10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

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DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_a = −30°C to +85°C)

Parameter	Symbol	Test Condition		MSM5126-20/25 Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}		−1		1	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}		−5		5	μA
Output Voltage	V_{OH}	I_{OH} = −1 mA		2.4			V
	V_{OL}	I_{OL} = 2.0 mA				0.4	V
Standby Supply Current	I_{CCS}	CS ≧ V_{CC} − 0.5V V_{CC} = 2V to 5.5V V_I = 0 to V_{CC}	Ta = 25°C		0.05	1.0	μA
			Ta = 60°C			5.0	
			Ta = 85°C			30	
	I_{CCS_1}	$\overline{CS}$ = V_{IH} t_{CYC} = Min. cycle			1	3	mA
Operating Supply Current	I_{CCA}	$\overline{CS}$ = 0V, V_{IN} = V_{IH}/V_{IL} I_{OUT} = 0 mA			40	70	mA
		$\overline{CS}$ = 0V, V_{IN} = V_{CC}/G_{ND}, I_{OUT} = 0 mA			30	55	mA

AC CHARACTERISTICS

Test Condition

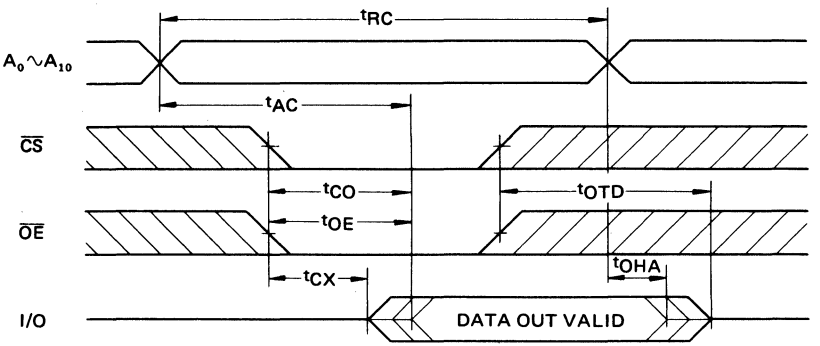
Parameter	Conditions
Input Pulse Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Level	2.2V 0.8V
Output Load	C_L=100 pF, 1 TTL Gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_a = −30°C to +85°C)

Parameter	Symbol	MSM5126-20 Min.	MSM5126-20 Max.	MSM5126-25 Min.	MSM5126-25 Max.	Unit
Read Cycle Time	t_{RC}	200		250		ns
Address Access Time	t_{AC}		200		250	ns
Chip Select Access Time	t_{CO}		200		250	ns
Output Enable to Output Valid	t_{OE}		100		100	ns
Chip Selection to Output Active	t_{CX}	10		10		ns
Output Hold Time From Address Change	t_{OHA}	10		10		ns
Output 3-state from Deselection	t_{OTD}	0	80	0	80	ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CX} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs last.
3. t_{OTD} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs first.
4. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.

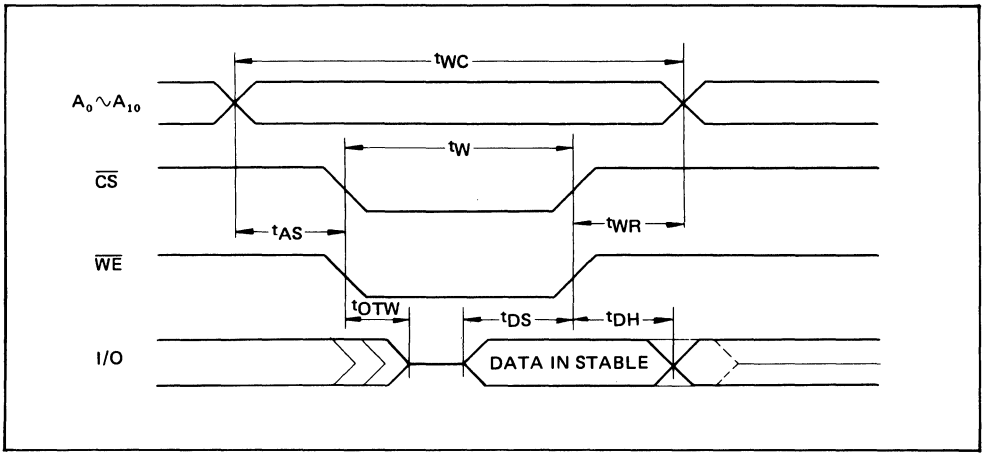
WRITE CYCLE

(V_{CC} = 5V ± 10%, T_a = −30°C to +85°C)

Parameter	Symbol	MSM5126-20		MSM5126-25		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	200		250		ns
Address to Write Setup Time	t_{AS}	0		0		ns
Write Time	t_W	160		200		ns
Write Recovery Time	t_{WR}	10		10		ns
Data Setup Time	t_{DS}	80		120		ns
Data Hold from Write Time	t_{DH}	0		0		ns
Output 3-State from Write	t_{OTW}		80		80	ns

Notes: 1. A Write Cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CS}$ and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

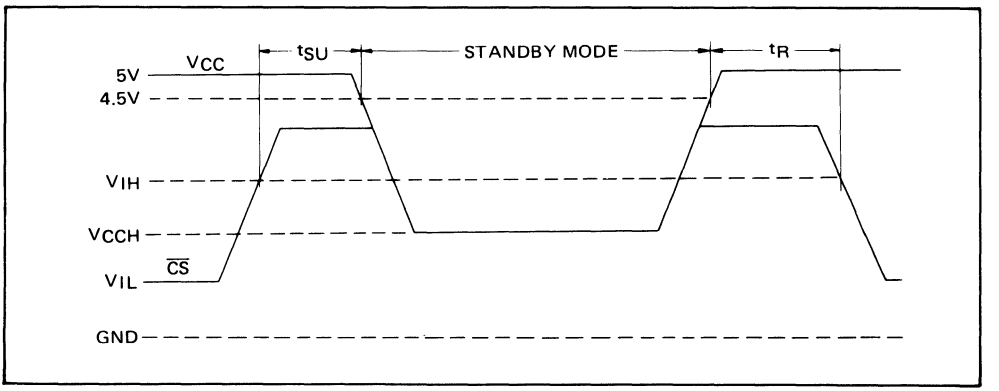
WRITE CYCLE



LOW V_{CC} DATA RETENTION CHARACTERISTICS

(T_a = −30°C to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2			V	V_{IN} = 0V to V_{CC}, CS = V_{CC}
Data Retention Current	I_{CCH}		0.05	30	μA	V_{CC} = 2V to 5.5V, V_I = 0V to V_{CC} CS ≧ = V_{CC} − 0.5V
CS to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	t_{RC}			ns	



CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$		5	10	pF
Input Capacitance	C_{IN}		5	10	pF

Note: This parameter is periodically sampled and not 100% tested.

OKI semiconductor

MSM5165RS/JS

8,192-WORD x 8-BIT CMOS STATIC RAM (E3-S-017-32)

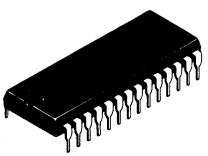
GENERAL DESCRIPTION

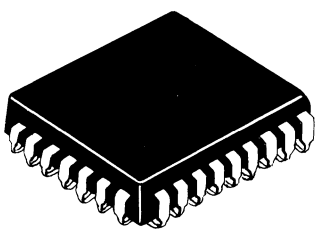
The MSM5165RS/JS is a 8192-word by 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM5165RS/JS is also a CMOS silicon gate device which requires very low power during standby (standby current of 1mA) when there is no chip selection.

A byte system is adopted, and since there is pin compatibility with standard ultra-violet EPROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, $\overline{CE}_1$ CE_2 and $\overline{OE}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

FEATURES

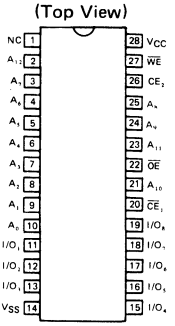
- Single 5V Supply
- 0°C ~ 70°C
- Low Power Dissipation
  - Standby; 5.5 mW MAX
  - Operation; 248 mW MAX
- High Speed (Equal Access and Cycle Time)
  - 120 — 200 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- Pin Compatible with
  - 64K EPROM (MSM2764)
- 28-pin DIP PKG
- 32-pin PLCC





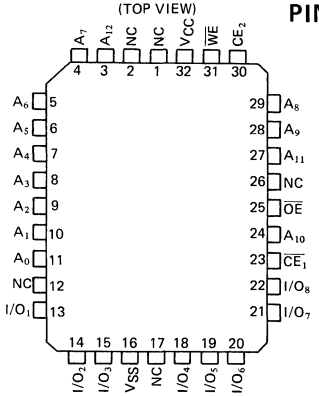
PIN CONFIGURATION

(Top View)



$A_0 \sim A_{12}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data Input/Output
$\overline{CE}_1$, CE_2 : Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS} : Supply Voltage

(TOP VIEW)



PIN CONFIGURATION

$A_0 \sim A_{12}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data INPUT/OUTPUT
$\overline{CE}_1$, CE_2 : Chip Select
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V_{CC}, V_{SS} : Supply Voltage

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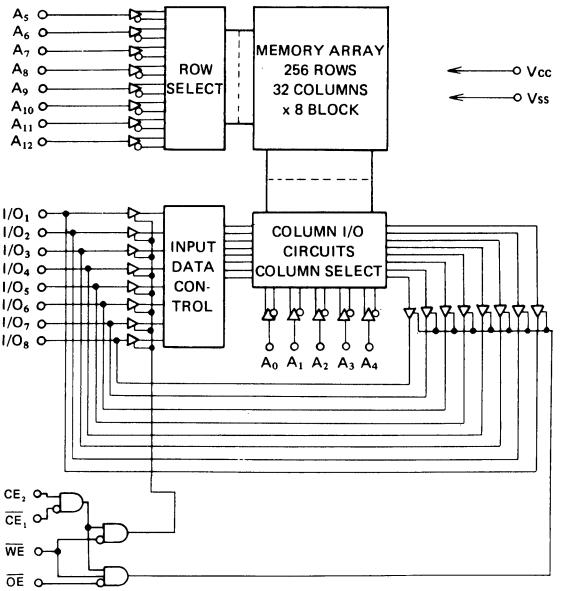
FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Mode	$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	X	High Z
	X	L	X	X	
Read	L	H	H	H	High Z
	L	H	H	L	D_{OUT}
Wreite	L	H	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	Ta = 25°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	5V ± 10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

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DC CHARACTERISTICS

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

Paramter	Symbol	MSM5165			Unit	Test Condition
		Min.	Typ.	Max.		
Input Leakage Current	I_{LI}	−1		1	μA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	−1		1	μA	$\overline{CE}_1$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}
Output Voltage	V_{OH}	2.4			V	I_{OH} = −1 mA
	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Standby Supply Current	I_{CCS}		0.02	1	mA	$\overline{CE}_1 \geqq V_{CC} - 0.2V$, $CE_2 \geqq V_{CC} - 0.2V$ V_{IN} = 0 to V_{CC}
						$CE_2 \leqq 0.2V$ V_{IN} = 0 to V_{CC}
	I_{CCS1}			3	mA	$\overline{CE}_1$ = V_{IH}, CE_2 = V_{IL} t_{cyc} = Min. cycle
Operating Supply Current	I_{CCA}			①	mA	T_{CYC} = Min. cycle
				15		T_{CYC} = 1 μs

5165-12 55 mA 5165-15 50 mA 5165-20 45 mA

AC CHARACTERISTICS

Test Condition

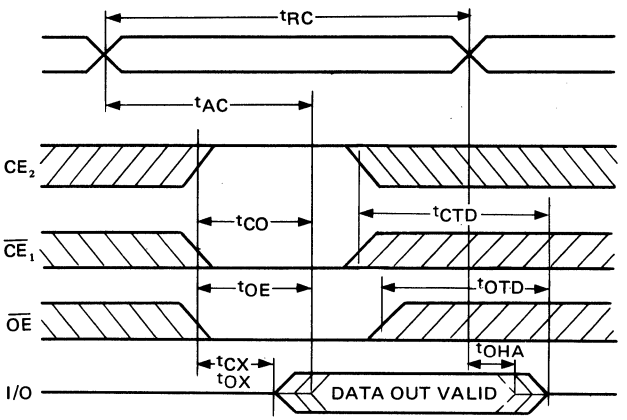
Parameter	Conditions
Input Pulse Level	V_{IH}=2.4V, V_{IL}=0.6V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L=100 pF, 1 TTL Gate

READ CYCLE

(V_{cc} = 5V ± 10%, T_a = 0°C to 70°C)

Parameter	Symbol	MSM5165-12		MSM5165-15		MSM5165-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	120		150		200		ns
Address Access Time	t_{AC}		120		150		200	ns
Chip Enable Access Time	t_{CO}		120		150		200	ns
Output Enable to Output Valid	t_{OE}		60		70		90	ns
Chip Selection to Output Active	t_{CX}	10		10		10		ns
Output Hold Time From Address Change	t_{OHA}	10		15		20		ns
Output Enable to Output Active	t_{OX}	5		5		5		ns
Output 3-state from Output Disable	t_{OTD}	0	40	0	50	0	60	ns
Output 3-state from Chip Deselection	t_{CTD}	0	60	0	70	0	80	ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CE_1}$, a high CE_2, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CX} is specified from $\overline{CE_1}$, CE_2 or $\overline{OE}$, whichever occurs last.
3. t_{OTD} is specified from $\overline{CE_1}$, CE_2 or $\overline{OE}$, whichever occurs first.
4. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.

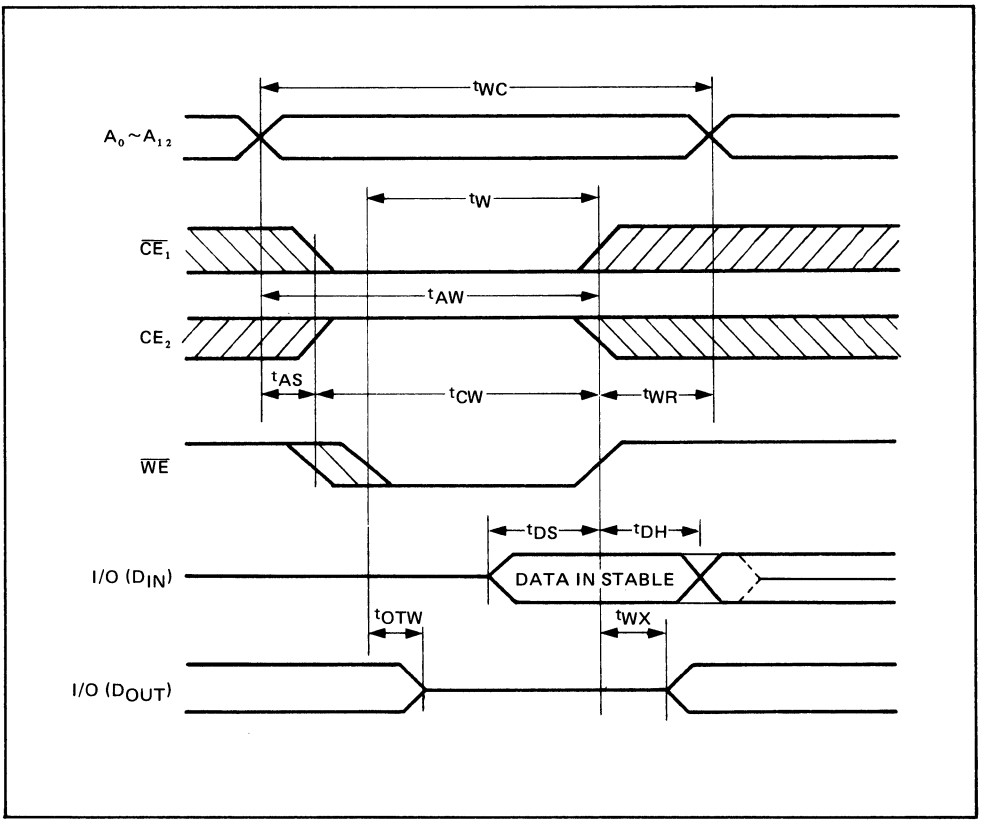
WRITE CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to +70°C)

Item	Symbol	MSM5165-12		MSM5165-15		MSM5165-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	120		150		200		ns
Address to Write Setup Time	t_{AS}	0		0		0		ns
Write Time	t_W	70		90		120		ns
Write Recovery Time	t_{WR}	15		15		15		ns
Data Setup Time	t_{DS}	50		60		80		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
Output 3-State from Write	t_{OTW}	0	40	0	50	0	60	ns
Chip Selection to End of Write	t_{CW}	100		120		150		ns
Address Valid to End of Write	t_{AW}	100		120		150		ns
Output Active from End of Write	t_{WX}	5		5		5		ns

Notes: 1. A Write Cycle occurs during the overlap of a low $\overline{CE_1}$, a high CE_2 and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CE_1}$, CE_2 or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CE_1}$, a high CE_2 and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CE_1}$, CE_2 or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

WRITE CYCLE



CAPACITANCE

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			8	pF
Input Capacitance	C_{IN}			6	pF

Note: This parameter is periodically sampled and not 100% tested.

OKI semiconductor

MSM5165LRS/JS

8,192-WORD x 8-BIT CMOS STATIC RAM (E3-S-017-32)

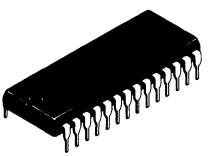
GENERAL DESCRIPTION

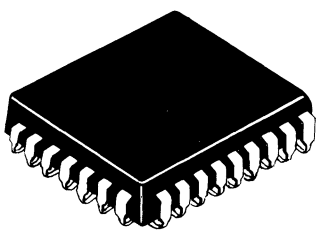
The MSM5165LRS/JS is a 8192-word by 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM5165LRS/JS is also a CMOS silicon gate device which requires very low power during standby (standby current of 100μA) when there is no chip selection.

A byte system is adopted, and since there is pin compatibility with standard ultra-violet EPROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, CE_1 CE_2 and OE signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

FEATURES

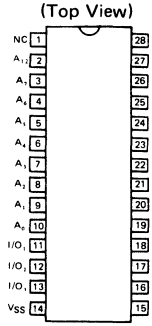
- Single 5V Supply
- 0°C ~ 70°C
- Low Power Dissipation
  - Standby; 0.55 mW MAX
  - Operation; 248 mW MAX
- High Speed (Equal Access and Cycle Time)
  - 120 – 200 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- Pin Compatible with
  - 64K EPROM (MSM2764)
- 28-pin DIP PKG
- 32-pin PLCC





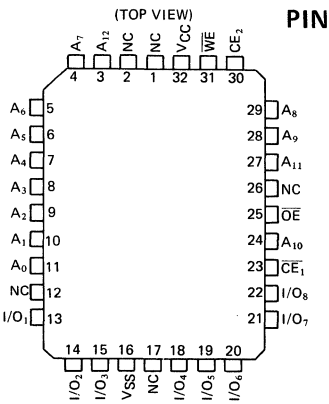
PIN CONFIGURATION

(Top View)



$A_0 \sim A_{12}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data Input/Output
$\overline{CE}_1$, CE_2 : Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS} : Supply Voltage

PIN CONFIGURATION



$A_0 \sim A_{12}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data INPUT/OUTPUT
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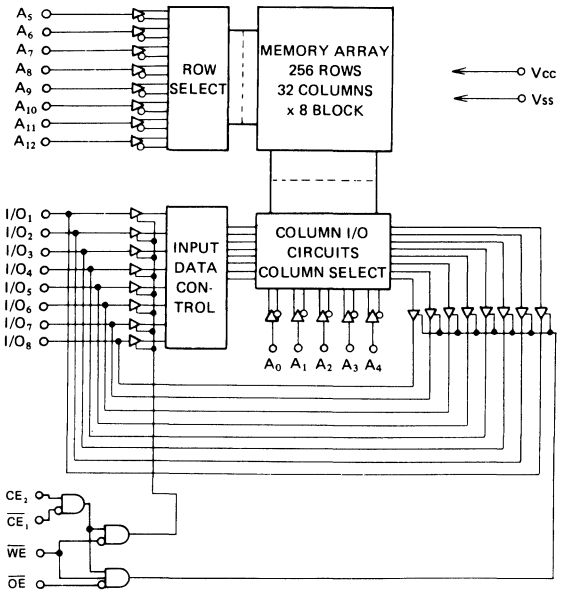
$\overline{WE}$: Write Enable
$\overline{OE}$: OUTPUT Enable
V_{CC}, V_{SS} : Supply Voltage

9

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Mode	$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	X	High Z
	X	L	X	X	
Read	L	H	H	H	High Z
	L	H	H	L	D_{OUT}
Wreite	L	H	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	Ta = 25°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Data Retention Voltage	V_{CCH}	2	5	5.5	V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	5V ± 10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

9

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

Paramter	Symbol	MSM5165L			Unit	Test Condition
		Min.	Typ.	Max.		
Input Leakage Current	I_{LI}	-1		1	μA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-1		1	μA	$\overline{CE}_1$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}
Output Voltage	V_{OH}	2.4			V	I_{OH} = -1 mA
	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Standby Supply Current	I_{CCS}		2	100	μA	$\overline{CE}_1 \geqq V_{CC}$ - 0.2V, $CE_2 \geqq V_{CC}$ - 0.2V or V_{IN} = 0 to V_{CC}
						$CE_2 \leqq 0.2V$ V_{IN} = 0 to V_{CC}
	I_{CCS1}			3	mA	$\overline{CE}_1$ = V_{IH}, CE_2 = V_{IL} t_{cyc} = Min, cycle
Operating Supply Current	I_{CCA}			①	mA	T_{CYC} = Min, cycle
				15		T_{CYC} = 1 μs

AC CHARACTERISTICS

Test Condition

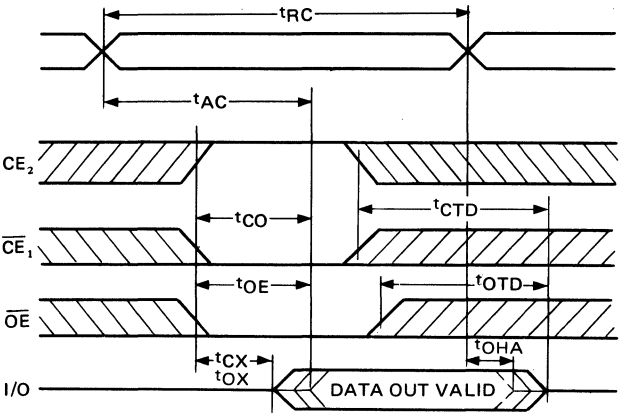
Parameter	Conditions
Input Pulse Level	V_{IH}=2.4V, V_{IL}=0.6V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L=100 pF, 1 TTL Gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to 70°C)

Parameter	Symbol	MSM5165-12		MSM5165-15		MSM5165-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	120		150		200		ns
Address Access Time	t_{AC}		120		150		200	ns
Chip Enable Access Time	t_{CO}		120		150		200	ns
Output Enable to Output Valid	t_{OE}		60		70		90	ns
Chip Selection to Output Active	t_{CX}	10		10		10		ns
Output Hold Time From Address Change	t_{OHA}	10		15		20		ns
Output Enable to Output Active	t_{OX}	5		5		5		ns
Output 3-state from Output Disable	t_{OTD}	0	40	0	50	0	60	ns
Output 3-state from Chip Deselection	t_{CTD}	0	60	0	70	0	80	ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CE_1}$, a high CE_2, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CX} is specified from $\overline{CE_1}$, CE_2 or $\overline{OE}$, whichever occurs last.
3. t_{OTD} is specified from $\overline{CE_1}$, CE_2 or $\overline{OE}$, whichever occurs first.
4. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.

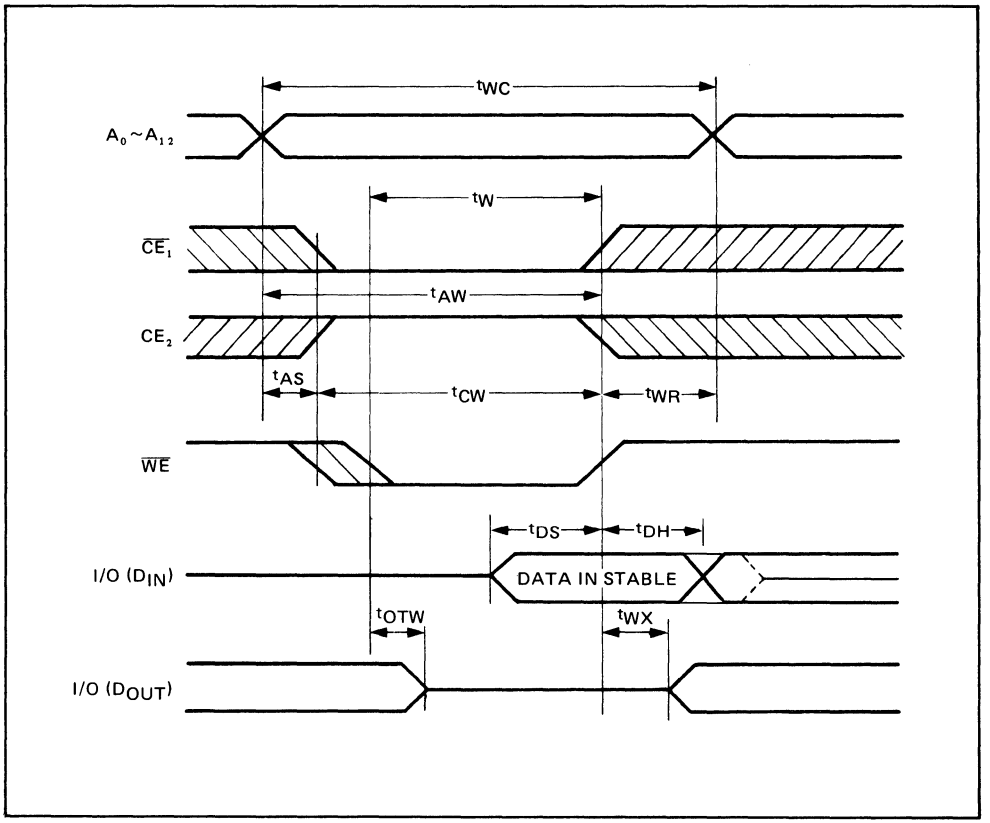
WRITE CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to +70°C)

Item	Symbol	MSM5165L-12		MSM5165L-15		MSM5165L-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	120		150		200		ns
Address to Write Setup Time	t_{AS}	0		0		0		ns
Write Time	t_W	70		90		120		ns
Write Recovery Time	t_{WR}	15		15		15		ns
Data Setup Time	t_{DS}	50		60		80		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
Output 3-State from Write	t_{OTW}	0	40	0	50	0	60	ns
Chip Selection to End of Write	t_{CW}	100		120		150		ns
Address Valid to End of Write	t_{AW}	100		120		150		ns
Output Active from End of Write	t_{WX}	5		5		5		ns

Notes: 1. A Write Cycle occurs during the overlap of a low $\overline{CE_1}$, a high CE_2 and a low $\overline{WE}$.
2. OE may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CE_1}$, CE_2 or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CE_1}$, a high CE_2 and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CE_1}$, CE_2 or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

WRITE CYCLE

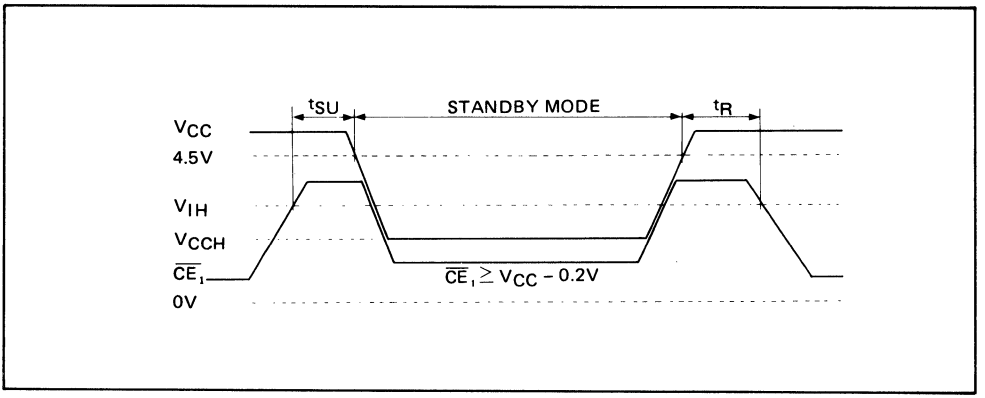


LOW V_{CC} DATA RETENTION CHARACTERISTICS

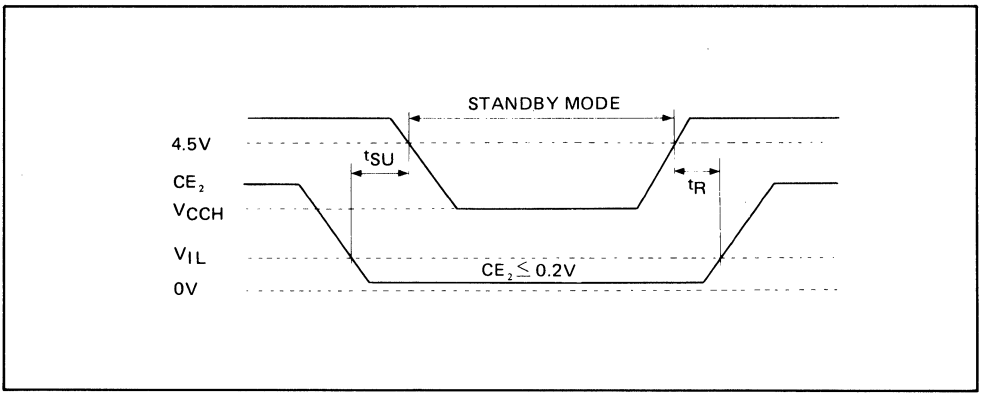
(T_a = 0°C to +70°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2			V	$\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \geq V_{CC} - 0.2V$
						$CE_2 \leq 0.2V$
Data Retention Current	I_{CCH}		1	50	μA	V_{CC} = 3V, $\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \geq V_{CC} - 0.2V$
						V_{CC} = 3V, $CE_2 \leq 0.2V$
CS to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	t_{RC}			ns	

$\overline{CE}_1$ CONTROL



CE_2 CONTROL



CAPACITANCE

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			8	pF
Input Capacitance	C_{IN}			6	pF

Note: This parameter is periodically sampled and not 100% tested.

Preliminary

MSM5188US

16,384-WORD × 4-BIT HIGH SPEED STATIC CMOS RAM

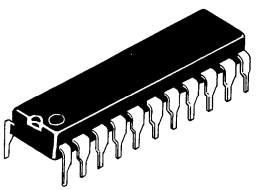
GENERAL DESCRIPTION

The MSM5188 is a static CMOS RAM organized as 16384 words by 4 bits. It features 5V single power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary which makes this device very easy to use.

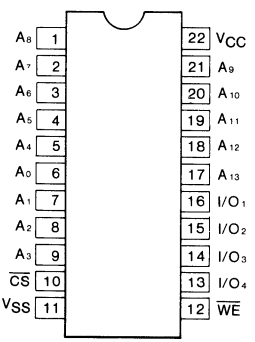
The MSM5188 is offered in a 22-pin slim package.

FEATURES

- Single 5V supply (±10%)
- Completely static operation
- Operating temperature range Ta = 0 to 70°C
- Low power dissipation
  - Standby ..... 11 mW MAX
  - Operation ..... 605 mW MAX
- Access time
  - 45/55/70 ns MAX
- Direct TTL compatible (Input and output)
- 3-State output
- 22 pin DIP PKG (300 mil width)

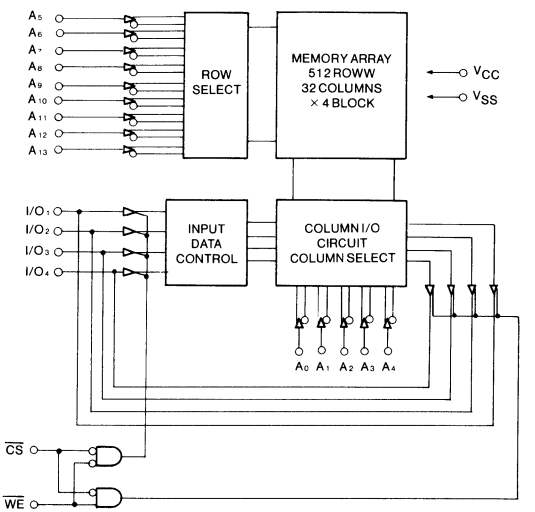


PIN CONFIGURATION



Pin Names	Function
A_0 to A_{13}	Address input
I/O_1 to I/O_4	Data input/output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}, V_{SS}	Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



9

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Condition	Value	Unit
Supply Voltage	V_{CC}	Ta = 25°C Respect to V_{SS}	−0.3 to 7.0	V
Input Voltage	V_{IN}		−0.3 to 7.0	V
Power Dissipation	PD	Ta = 25°C	1.0	W
Operating Temperature	Topr	–	0 to +70	°C
Storage Temperature	Tstg	–	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	–	4.5	5.0	5.5	V
"H" Input Voltage	V_{IH}	V_{CC} = 5V ± 10%	2.2	–	V_{CC} +0.3	V
"L" Input Voltage	V_{IL}		−0.3	–	0.8	V
Output Load	CL	–	–	–	30	pF
	N	TTL Load	–	–	1	

* When pulse width is equal to or smaller than 20 ns, V_{IH} max = V_{CC} + 1.0V, V_{IL} min = −1.0V.

DC CHARACTERISTICS

(V_{CC} = 5V±10%, Ta = 0°C to 70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	VI = 0 to V_{CC}	−1		1	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} VI/O = 0 to V_{CC}	−1		1	μA
"H" Output Voltage	V_{OH}	I_{OH} = −4 mA	2.4			V
"L" Output Voltage	V_{OL}	I_{OL} = 8 mA			0.4	V
Standby Supply Current	I_{CCS}	$\overline{CS} \geqq V_{CC} - 0.2V$ VIN ≦ 0.2V OR VIN ≧ V_{CC} − 0.2V			2	mA
	I_{CCS1}	$\overline{CS}$ = V_{IH} T_{CYC} = min cycle			18	mA
Operating Supply Current	I_{CCA}	Min cycle			110	mA

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Max.	Unit
Input Capacitance	C_I	$V_I = 0V$		6	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O} = 0V$		8	pF

AC CHARACTERISTICS TEST CONDITIONS

Parameter	Conditions
Input Pulse Level	$V_{IH} = 3.0V$, $V_{IL} = 0V$
Input Rise and Fall Times	5 ns
Input/Output Timing Reference Level	1.5V
Output Load	CL = 30 pF, 1 TTL GATE

READ CYCLE

(V_{CC} = 5V±10%, Ta = 0°C to 70°C)

Parameter	Symbol	5188-45		5188-55		5188-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	T_{RC}		45		55		70	ns
Address Access Time	T_{AC}		45		55		70	ns
Chip Select Access Time	T_{CO}		45		55		70	ns
Chip Selection to Output Active	T_{CX}	5		5		5		ns
Output Hold Time from Address Change	T_{OHA}	5		5		5		ns
Output 3-state from Deselection	T_{OTD}	0	25	0	30	0	30	ns
Chip Selection to Power up Time	T_{PU}	0		0		0		ns
Chip Deselection to Power Down Time	T_{PD}	0	45	0	55	0	70	ns

Notes: 1. Read Condition: During the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. T_{CX} and T_{OTD} are measured ±200 mV from steady state voltage with specified loading in Figure 2.

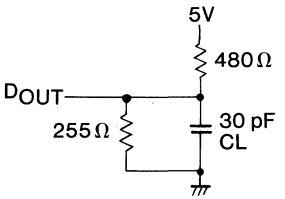


Figure 1 Output Load

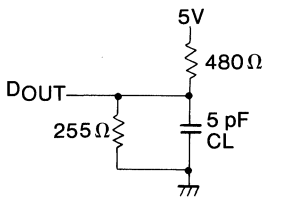


Figure 2 Output Load

Note: CL includes scope and jig.

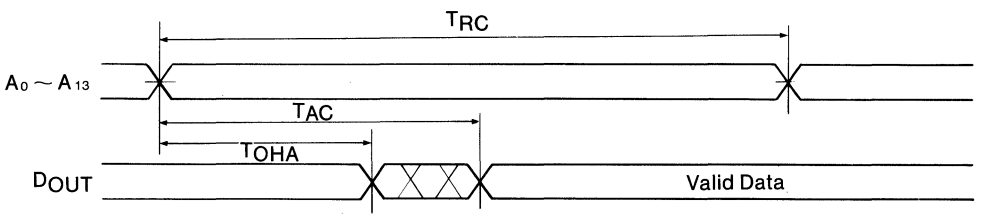
WRITE CYCLE

(V_{CC} = 5V±10%, Ta = 0°C to 70°C)

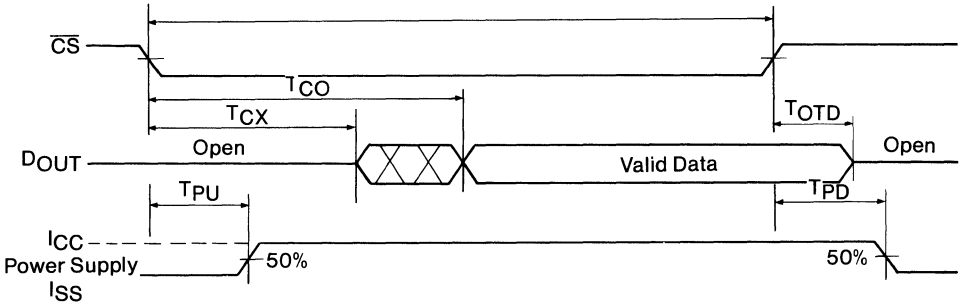
Parameter	Symbol	5188-45		5188-55		5188-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	T_{WC}	45		55		70		ns
Chip Selection to End of Write	T_{CW}	40		45		55		ns
Address Valid to End of Write	T_{AW}	40		45		55		ns
Address to Write Setup Time	T_{AS}	0		0		0		ns
Write Time	T_W	30		35		40		ns
Write Recovery Time	T_{WR}	5		10		10		ns
Data Setup Time	T_{DS}	25		25		30		ns
Data Hold from Write Time	T_{DH}	0		0		0		ns
Output 3-state from Write	T_{OTW}	0	25	0	25	0	30	ns
Output Active from End of Write	T_{OW}	0		0		0		ns

Notes:
1. Write condition: During the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. T_{AS} is specified from a low $\overline{CS}$ or a low $\overline{WE}$, whichever occurs last after the address is set.
3. T_W is an overlap time of a low $\overline{CS}$ and a low $\overline{WE}$.
4. T_{WR}, T_{DS} and T_{DH} are specified from a high $\overline{CS}$ or a high $\overline{WE}$, whichever occurs first.
5. T_{OTW} and T_{OW} are measured ±200 mV from steady state voltage with specified loading in Figure 2.
6. When I/O pins are Data output mode, don't force inverse input signals to those pins.

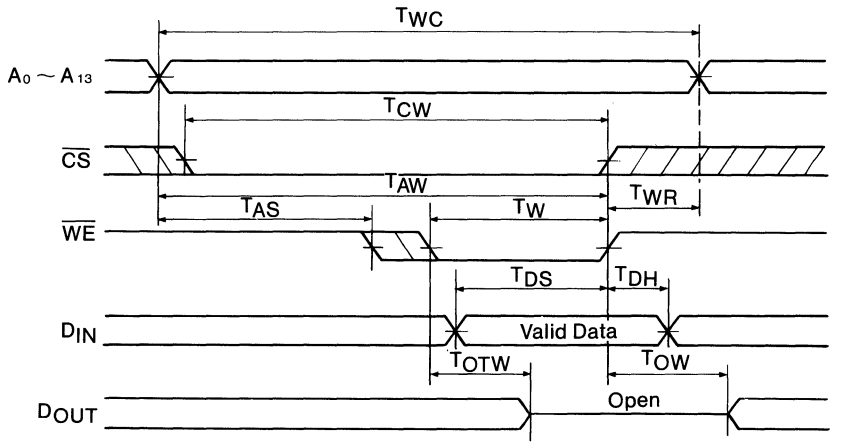
READ CYCLE TIMING 1



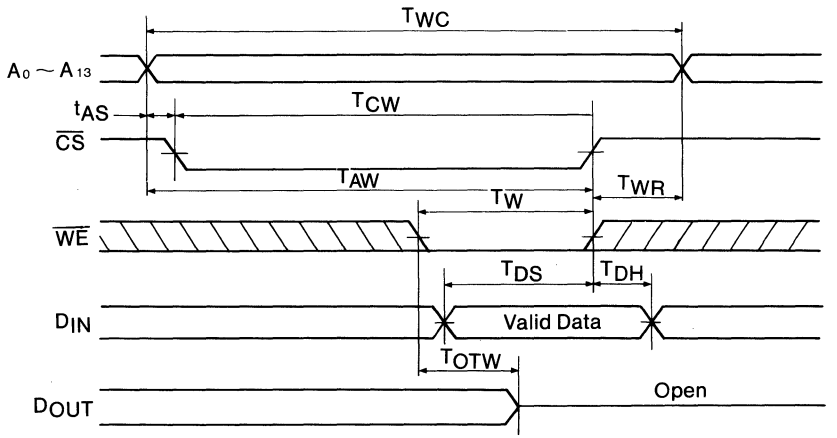
READ CYCLE TIMING 2



WRITE CYCLE TIMING 1
(WE Control)



WRITE CYCLE TIMING 2
(CS Control)



9

OKI semiconductor

MSM51257RS/JS

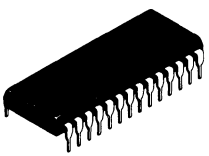
32,768-WORD x 8-BIT CMOS STATIC RAM

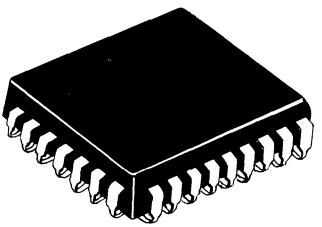
GENERAL DESCRIPTION

The MSM51257RS/JS is a 32768-word by 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM51257RS/JS is also a CMOS silicon gate device which requires very low power during standby (standby current of 1mA) when there is no chip selection.
$\overline{CS}$ and $\overline{OE}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

FEATURES

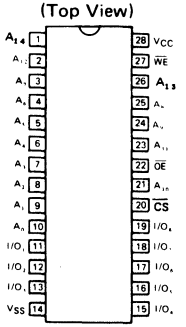
- Single 5V Supply
- 0°C ~ 70°C
- Low Power Dissipation
  Standby; 5.5 mW MAX
  Operation; 385mW MAX
- High Speed (Equal Access and Cycle Time)
  85-120 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- 28-pin DIP PKG
- 32-pin PLCC





PIN CONFIGURATION

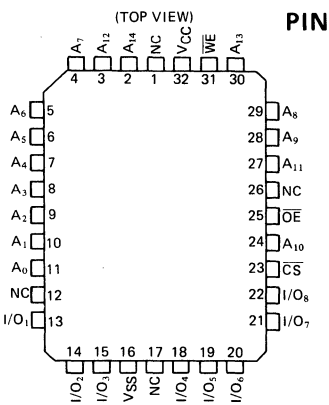
(Top View)



$A_0 \sim A_{14}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data Input/Output
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS} : Supply Voltage

PIN CONFIGURATION

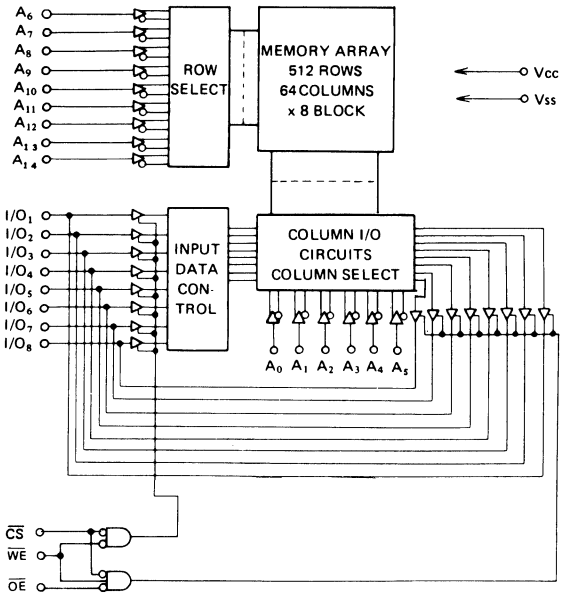
(TOP VIEW)



$A_0 \sim A_{14}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data INPUT/OUTPUT
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: OUTPUT Enable
V_{CC}, V_{SS} : Supply Voltage

9

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	High Z
Read	L	H	H	High Z
	L	H	L	D_{OUT}
Wreite	L	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	Ta = 25°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	5V ± 10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

9

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

Paramter	Symbol	MSM51257			Unit	Test Condition
		Min.	Typ.	Max.		
Input Leakage Current	I_{LI}	−1		1	μA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	−1		1	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}
Output Voltage	V_{OH}	2.4			V	I_{OH} = −1 mA
	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Standby Supply Current	I_{CCS}		0.02	1	mA	$\overline{CS}$ ≧ V_{CC} − 0.2V V_{IN} = 0 to V_{CC}
	I_{CCS1}			3	mA	$\overline{CS}$ = V_{IH} t_{cyc} = Min. cycle
Operating Supply Current	I_{CCA}			70	mA	MIN CYCLE

AC CHARACTERISTICS

Test Condition

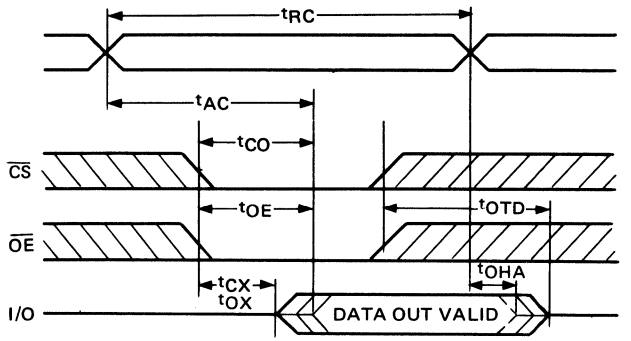
Parameter	Conditions
Input Pulse Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L=100 pF, 1 TTL Gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to 70°C)

Parameter	Symbol	MSM51257-85		MSM51257-10		MSM51257-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	85		100		120		ns
Address Access Time	t_{AC}		85		100		120	ns
Chip Enable Access Time	t_{CO}		85		100		120	ns
Output Enable to Output Valid	t_{OE}		45		50		60	ns
Chip Selection to Output Active	t_{CX}	10		10		10		ns
Output Hold Time From Address Change	t_{OHA}	5		10		10		ns
Output 3-state from Deselection	t_{OTD}	0	30	0	35	0	40	ns
Output Enable to Output Active	t_{OX}	5		5		5		ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and ahigh $\overline{WE}$.
2. t_{CX} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs last.
3. t_{OTD} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs first.
4. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.

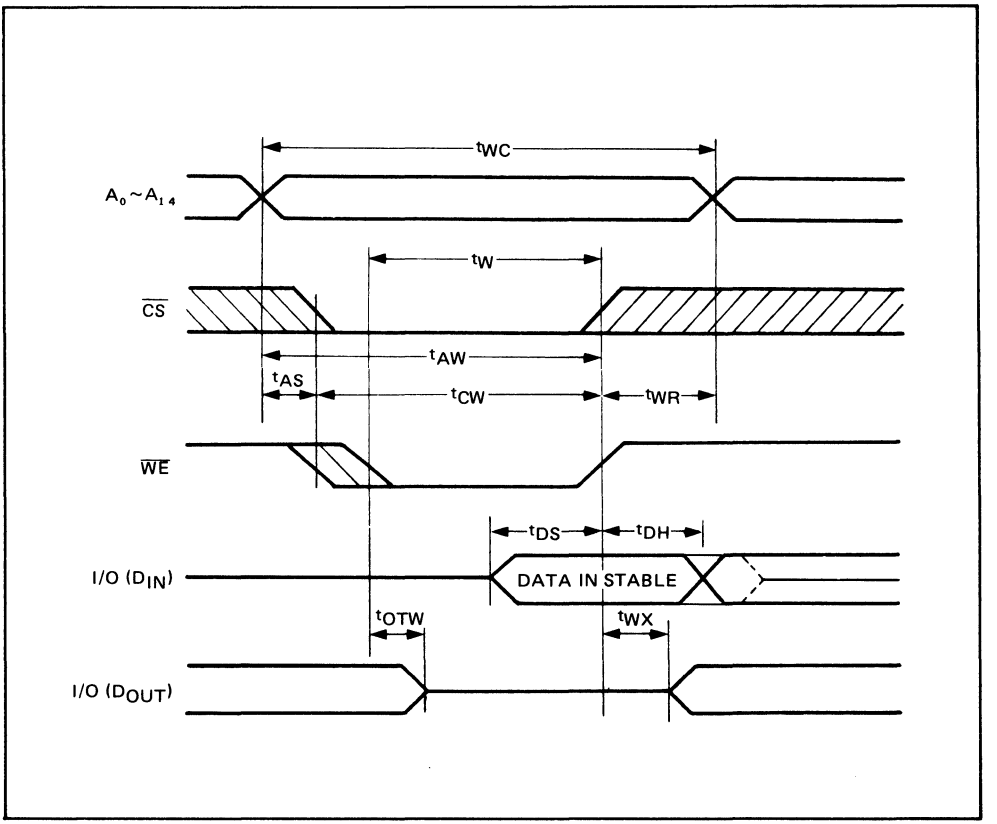
WRITE CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to +70°C)

Item	Symbol	MSM51257-85		MSM51257-10		MSM51257-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	85		100		120		ns
Address to Write Setup Time	t_{AS}	0		0		0		ns
Write Time	t_W	65		75		90		ns
Write Recovery Time	t_{WR}	5		10		10		ns
Data Setup Time	t_{DS}	35		40		50		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
Output 3-State from Write	t_{OTW}	0	30	0	35	0	40	ns
Chip Selection to End of Write	t_{CW}	75		90		100		ns
Address Valid to End of Write	t_{AW}	75		90		100		ns
Output Active from End of Write	t_{WX}	5		5		5		ns

Notes: 1. A Write Cycle occurs during the overlap of a low $\overline{CS}$, and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CS}$, and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

WRITE CYCLE



CAPACITANCE

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			8	pF
Input Capacitance	C_{IN}			6	pF

Note: This parameter is periodically sampled and not 100% tested.

9

OKI semiconductor

MSM51257LRS/JS

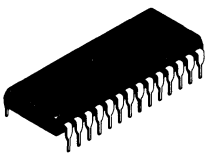
32,768-WORD x 8-BIT CMOS STATIC RAM

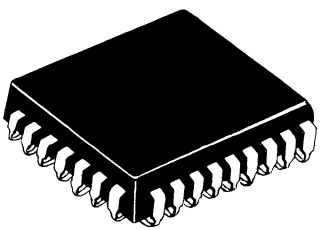
GENERAL DESCRIPTION

The MSM51257LRS/JS is a 32768-word by 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM51257LRS/JS is also a CMOS silicon gate device which requires very low power during standby (standby current of 100μA) when there is no chip selection.
$\overline{CS}$ and $\overline{OE}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

FEATURES

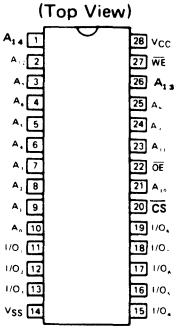
- Single 5V Supply
- 0°C ~ 70°C
- Low Power Dissipation
  Standby; 0.55 mW MAX
  Operation; 385 mW MAX
- High Speed (Equal Access and Cycle Time)
  85-120 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- 28-pin DIP PKG
- 32-pin PLCC





PIN CONFIGURATION

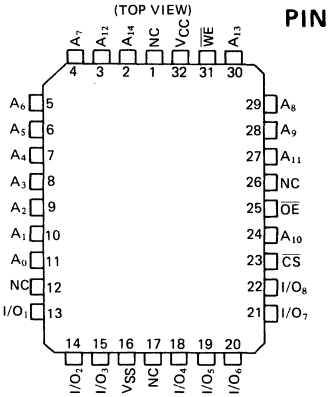
(Top View)



$A_0 \sim A_{14}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data Input/Output
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS} : Supply Voltage

PIN CONFIGURATION

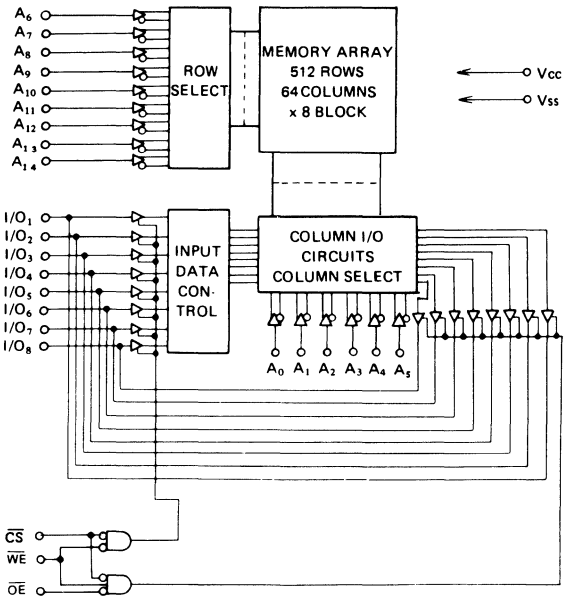
(TOP VIEW)



$A_0 \sim A_{14}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data INPUT/OUTPUT
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: OUTPUT Enable
V_{CC}, V_{SS} : Supply Voltage

9

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	High Z
Read	L	H	H	High Z
	L	H	L	D_{OUT}
Wreite	L	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	Ta = 25°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Data Retention Voltage	V_{CCH}	2	5	5.5	V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	5V ± 10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

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DC CHARACTERISTICS

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

Paramter	Symbol	MSM51257			Unit	Test Condition
		Min.	Typ.	Max.		
Input Leakage Current	I_{LI}	−1		1	μA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	−1		1	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}
Output Voltage	V_{OH}	2.4			V	I_{OH} = −1 mA
	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Standby Supply Current	I_{CCS}		2	100	μA	$\overline{CS}$ ≧ V_{CC} − 0.2V V_{IN} = 0 to V_{CC}
	I_{CCS1}			3	mA	$\overline{CS}$ = V_{IH},
Operating Supply Current	I_{CCA}			70	mA	MIN CYCLE

AC CHARACTERISTICS

Test Condition

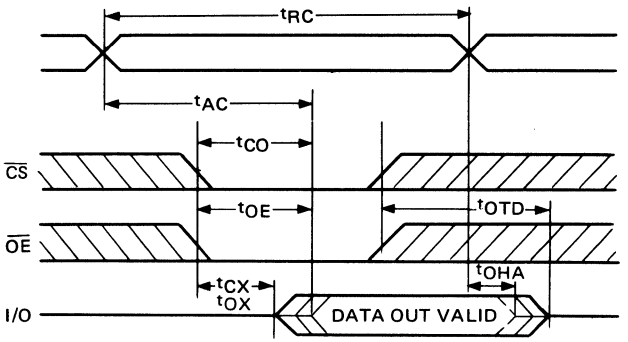
Parameter	Conditions
Input Pulse Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L=100 pF, 1 TTL Gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to 70°C)

Parameter	Symbol	MSM51257L-85		MSM51257L-10		MSM51257L-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	85		100		120		ns
Address Access Time	t_{AC}		85		100		120	ns
Chip Enable Access Time	t_{CO}		85		100		120	ns
Output Enable to Output Valid	t_{OE}		45		50		60	ns
Chip Selection to Output Active	t_{CX}	10		10		10		ns
Output Hold Time From Address Change	t_{OHA}	5		10		10		ns
Output 3-state from Deselection	t_{OTD}	0	30	0	35	0	40	ns
Output Enable to Output Active	t_{OX}	5		5		5		ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and ahigh $\overline{WE}$.
2. t_{CX} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs last.
3. t_{OTD} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs first.
4. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.

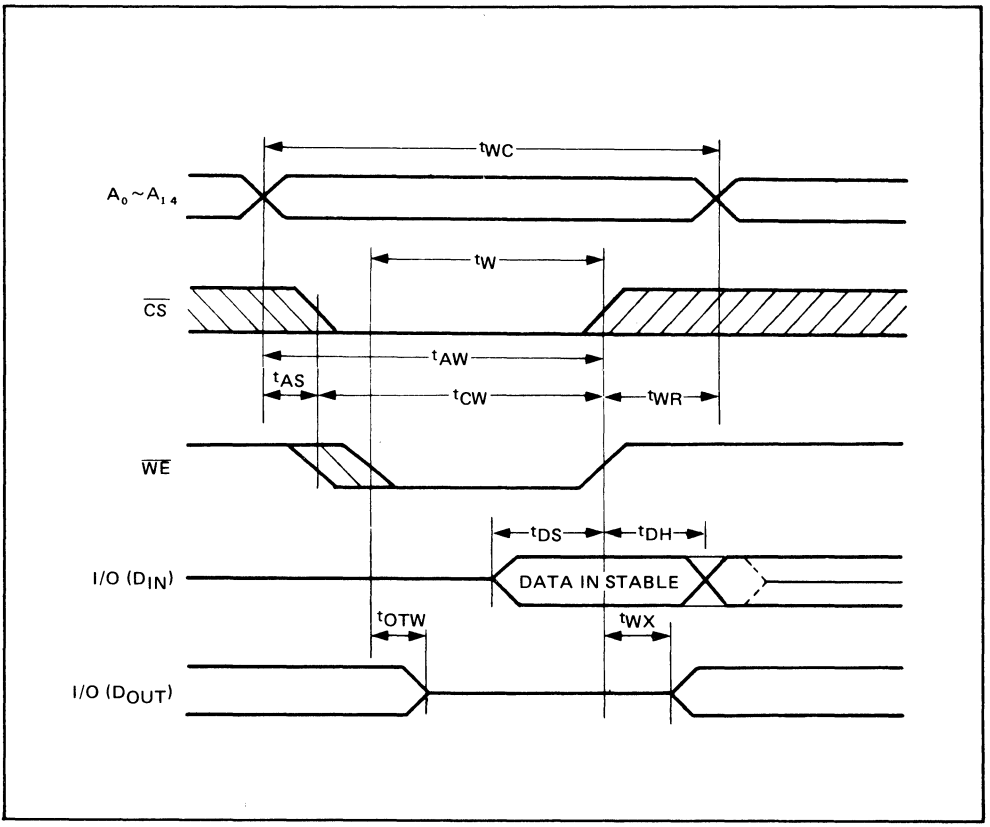
WRITE CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to +70°C)

Item	Symbol	MSM51257L-85		MSM51257L-10		MSM51257L-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	85		100		120		ns
Address to Write Setup Time	t_{AS}	0		0		0		ns
Write Time	t_W	65		75		90		ns
Write Recovery Time	t_{WR}	5		10		10		ns
Data Setup Time	t_{DS}	35		40		50		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
Output 3-State from Write	t_{OTW}	0	30	0	35	0	40	ns
Chip Selection to End of Write	t_{CW}	75		90		100		ns
Address Valid to End of Write	t_{AW}	75		90		100		ns
Output Active from End of Write	t_{WX}	5		5		5		ns

Notes: 1. A Write Cycle occurs during the overlap of a low $\overline{CS}$, and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CS}$, and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

WRITE CYCLE

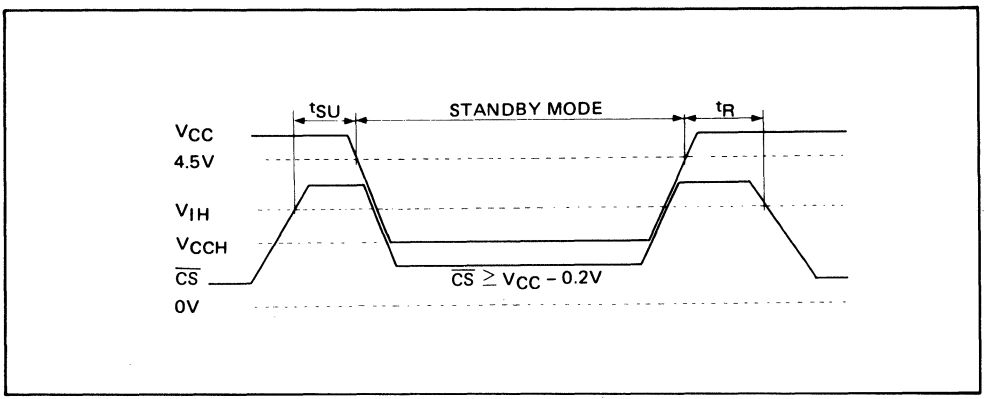


LOW V_{CC} DATA RETENTION CHARACTERISTICS

(T_a = 0°C to +70°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2			V	$\overline{CS} \geq V_{CC} - 0.2V$
Data Retention Current	I_{CCH}		1	50	μA	V_{CC} = 3V, $\overline{CS} \geq V_{CC} - 0.2V$
CS to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	t_{RC}			ns	

$\overline{CS}$ CONTROL



CAPACITANCE

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			8	pF
Input Capacitance	C_{IN}			6	pF

Note: This parameter is periodically sampled and not 100% tested.

MOS MASK ROMS

OKI semiconductor

MSM3864RS

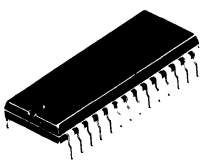
8,192 WORD x 8 BIT MASK ROM

GENERAL DESCRIPTION

The MSM3864RS is an N-channel silicon gate MOS device MASK ROM with a 8,192 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 30mA (max) when the chip is not selected. The application of a byte system and the pin compatibility with standard UV EPROMs make the device most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.
As it provides CE, OE, and CS as the control signal, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expansion of memory and bus line control.

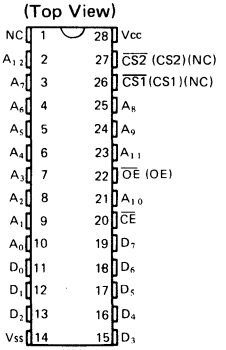
FEATURES

- 5V single power supply
- 8,192 words x 8 bits
- Access time: 250 ns MAX
- Input/output TTL compatible
- 3-state output
- Power down mode
- 28-pin DIP



PIN CONFIGURATION

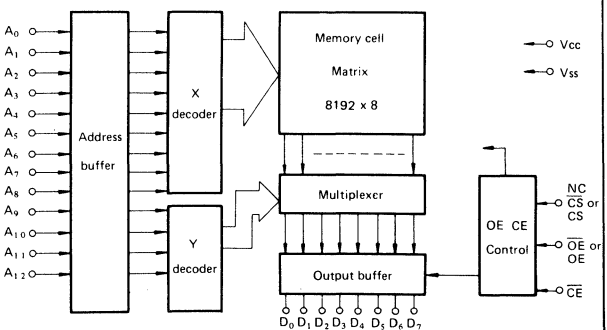
(Top View)



$\overline{OE}$	:	Output enable
Vcc, Vss	:	Power supply
$A_0 \sim A_{12}$	:	Address input
$D_0 \sim D_7$	:	Data output
$\overline{CE}$	:	Chip enable
$\overline{CS1}$, $\overline{CS2}$	:	Chip select

Note: Please specify the OE active level and CS active level or open in ordering this IC.

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	V_{CC}	−0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.5 to 7	V	Respect to V_{SS}
Output Voltage	V_O	−0.5 to 7	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	–	4.5	5	5.5	V
	V_{SS}	–	0	0	0	V
Input Signal Level	V_{IH}	–	2	5	6	V
	V_{IL}	–	−0.5	0	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4	–	Vcc	V
	V_{OL}	I_{OL} = 2.1 mA		–	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	−10	–	10	μA
Output Leakage Current	I_{LO}	V_O = 0V or Vcc Chip not selected	−10	–	10	μA
Power Supply Current	Icc	Vcc = Max. I_O = 0 mA	–	–	100	mA
	Iccs	Vcc = Max. CE = V_{IH}, I_O = 0 mA	–	–	30	mA
Peak Power ON Current	Ipo	Vcc = GND ~ Vcc Min. $\overline{CE}$ = V_{CC} or V_{IH}	–	–	60	mA
Operating Temperature	T_{opr}	–	0	–	70	°C

AC CHARACTERISTICS

TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V_{IH}=2.4V V_{IL}=0.6V
Input Rising, Falling Time	tr=tf=15 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8V & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

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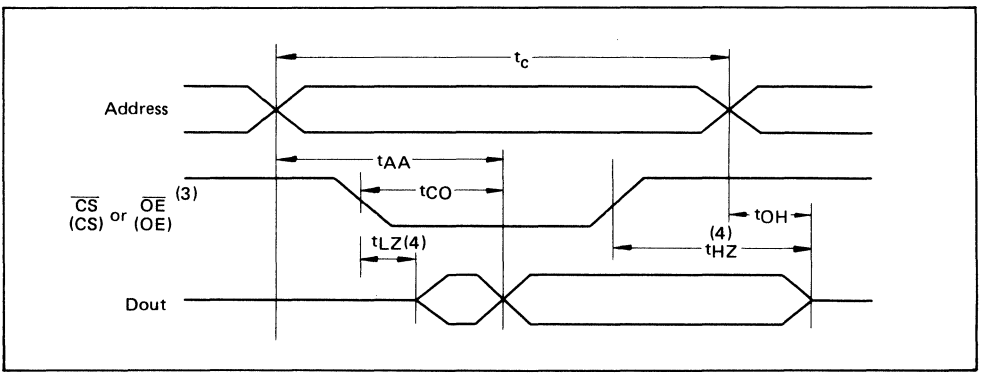
READ CYCLE

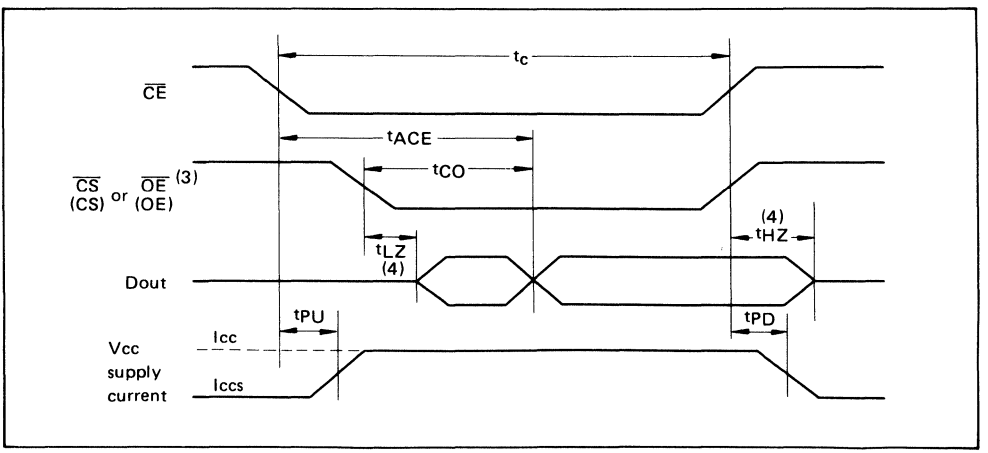
(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_c	250	–		ns	
Address Access Time	t_{AA}	–	–	250	ns	
Chip Enable Access Time	t_{ACE}	–	–	250	ns	
Output Delay Time	t_{CO}	–	–	100	ns	
Output Setting Time	t_{LZ}	10	–	–	ns	
Output Disable Time	t_{HZ}	10	–	100	ns	
Output Retaining Time	t_{OH}	10	–	–	ns	
Power Up Time	t_{PU}	0	–		ns	
Power Down Time	t_{PD}	–	–	100	ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



Notes: (1) $\overline{CE}$ is "L" level.
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) The $\overline{OE}$ and $\overline{CS}$ are shown in the negative logic here, however the active level is freely selected.
(4) t_{LZ} is determined by the later level, $\overline{CE}$ "L"/$\overline{CS}$ "L" or $\overline{OE}$ "L".
t_{HZ} is determined by the earlier $\overline{CE}$ "H"/$\overline{CS}$ "H" or $\overline{OE}$ "H".
While, t_{HZ} shows the time until floating and it is therefore not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I		8	pF	V_I=0V
Output Capacitance	C_O		10	pF	V_O=0V

MSM38128ARS

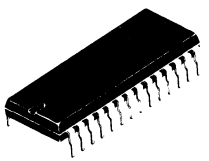
16,384 WORD x 8 BIT MASK ROM (E3-S-028-32)

GENERAL DESCRIPTION

The MSM38128ARS is an N-channel silicon gate MOS device MASK ROM with a 16,384 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 30mA (max) when the chip is not selected. The application of a byte system and the pin compatibility with standard UV EPROMs make the device most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.
As it provides CE, OE, and CS as the control signal, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

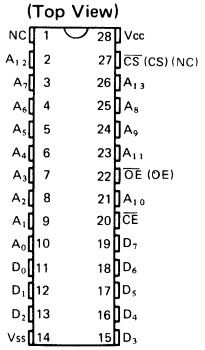
FEATURES

- 5V single power supply
- 16384 words x 8 bits
- Access time: 250 ns MAX
- Input/output TTL compatible
- 3-state output
- Power down mode
- 28-pin DIP



PIN CONFIGURATION

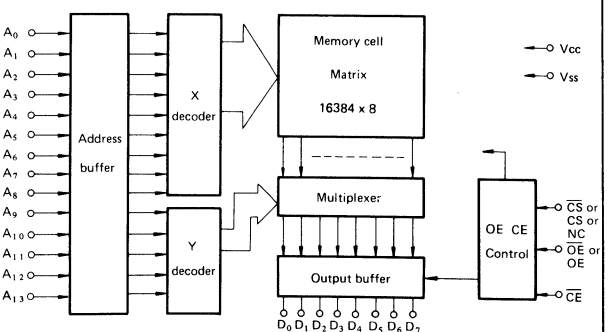
(Top View)



$\overline{OE}$	:	Output enable
Vcc, Vss	:	Power supply
$A_0 \sim A_{12}$	:	Address input
$D_0 \sim D_7$	:	Data output
$\overline{CE}$	:	Chip enable
$\overline{CS}$	:	Chip select

Note: Please specify the $\overline{OE}$ active level and $\overline{CS}$ active level or open in ordering this IC.

FUNCTIONAL BLOCK DIAGRAM



9

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	V_{CC}	−0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.5 to 7	V	Respect to V_{SS}
Output Voltage	V_O	−0.5 to 7	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	–	4.5	5	5.5	V
	V_{SS}	–	0	0	0	V
Input Signal Level	V_{IH}	–	2	5	6	V
	V_{IL}	–	−0.5	0	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4	–	Vcc	V
	V_{OL}	I_{OL} = 2.1 mA		–	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	−10	–	10	μA
Output Leakage Current	I_{LO}	V_O = 0V or Vcc Chip not selected	−10	–	10	μA
Power Supply Current	Icc	Vcc = Max. I_O = 0 mA	–	–	100	mA
	Iccs	Vcc = Max.	–	–	30	mA
Peak Power ON Current	Ipo	Vcc = GND ~ Vcc Min. $\overline{CE}$ = V_{CC} or V_{IH}	–	–	60	mA
Operating Temperature	T_{opr}	–	0	–	70	°C

AC CHARACTERISTICS

TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V_{IH}=2.4V V_{IL}=0.6V
Input Rising, Falling Time	tr=tf=15 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8V & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

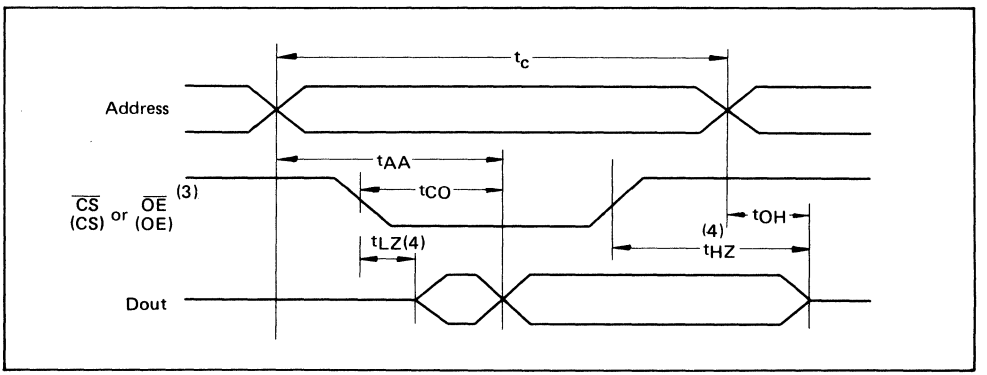
9

READ CYCLE

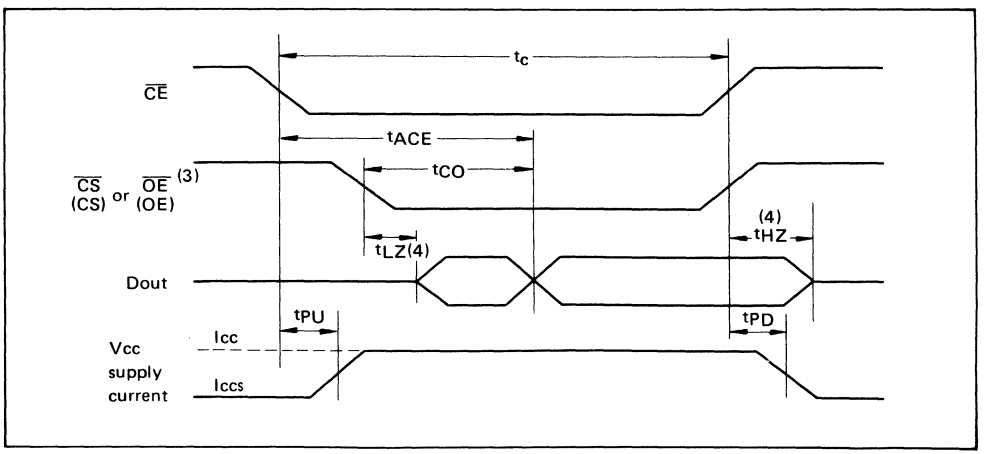
(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_c	250	–		ns	
Address Access Time	t_{AA}	–	–	250	ns	
Chip Enable Access Time	t_{ACE}	–	–	250	ns	
Output Delay Time	t_{CO}	–	–	100	ns	
Output Setting Time	t_{LZ}	10	–	–	ns	
Output Disable Time	t_{HZ}	10	–	100	ns	
Output Retaining Time	t_{OH}	10	–	–	ns	
Power Up Time	t_{PU}	0	–		ns	
Power Down Time	t_{PD}	–	–	100	ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



Notes: (1) $\overline{CE}$ is "L" level.
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) The $\overline{OE}$ and $\overline{CS}$ are shown in the negative logic here, however the active level is freely selected.
(4) t_{Lz} is determined by the later level, $\overline{CE}$ "L"/$\overline{CS}$ "L" or $\overline{OE}$ "L".
t_{Hz} is determined by the earlier $\overline{CE}$ "H"/$\overline{CS}$ "H" or $\overline{OE}$ "H".
While, t_{Hz} shows the time until floating and it is therefore not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I		8	pF	V_I=0V
Output Capacitance	C_O		10	pF	V_O=0V

MSM38256RS

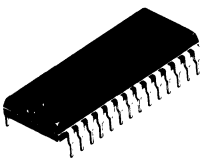
32768 WORD x 8 BIT MASK ROM (E3-S-029-32)

GENERAL DESCRIPTION

The MSM38256RS is an N-channel silicon gate MOS device ROM with a 32,768 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 30mA (max) when the chip is not selected. The application of a byte system and the pin compatibility with standard UV EPROMs make the device most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.
Since it provides CE, CS and OE signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

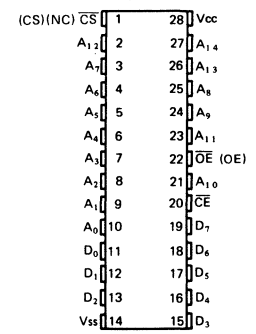
FEATURES

- 32768 words x 8 bits
- 5V single power supply
- Access time: 250 ns MAX
- Input/output TTL compatible
- 3-state output
- Power down mode
- 28-pin DIP



PIN CONFIGURATION

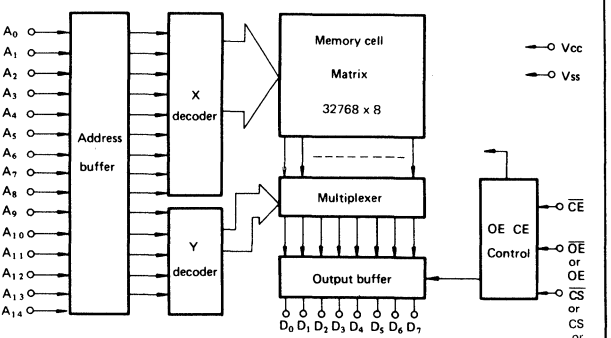
(Top View)



$\overline{CS}$: Chip Select
$\overline{OE}$: Output enable
Vcc, Vss : Power supply voltage
$A_0 \sim A_{13}$: Address input
$D_0 \sim D_7$: Data output
$\overline{CE}$: Chip enable

Note: The $\overline{OE}$ active level and $\overline{CS}$ active level are specified by customer.

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	V_{CC}	−0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.5 to 7	V	
Output Voltage	V_O	−0.5 to 7	V	
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}		4.5	5	5.5	V
	V_{SS}		0	0	0	V
Input Signal Level	V_{IH}		2	5	6	V
	V_{IL}		−0.5	0	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4		Vcc	V
	V_{OL}	I_{OL} = 2.1 mA			0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	−10		10	μA
Output Leakage Current	I_{LO}	V_O = 0V or Vcc Chip not selected	−10		10	μA
Power Supply Current	Icc	Vcc = Max. I_O = 0 mA			120	mA
	Iccs	Vcc = Max.			30	mA
Peak Power ON Current	Ipo	Vcc = GND ~ Vcc Min. $\overline{CE}$ = V_{CC} or V_{IH}			60	mA
Operating Temperature	T_{opr}		0		70	°C

AC CHARACTERISTICS

TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V_{IH}=2.4V V_{IL}=0.6V
Input Rising, Falling Time	tr=tf=15 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8 & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

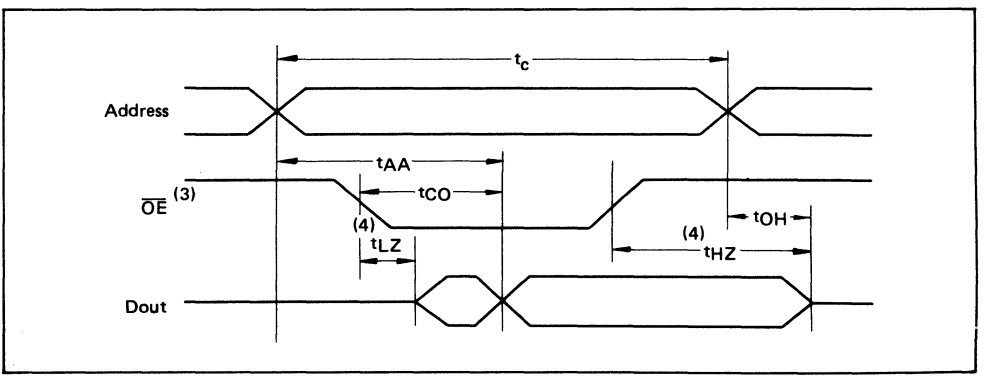
9

READ CYCLE

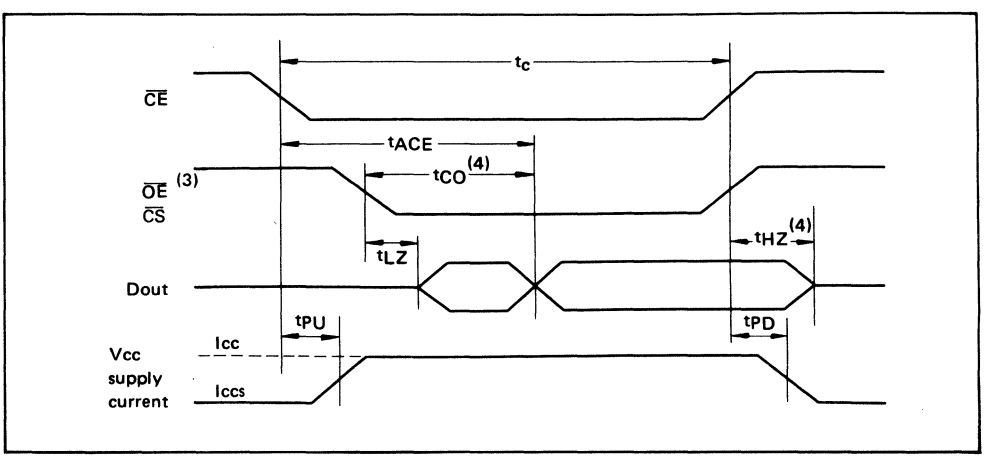
(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_C	250			ns	
Address Access Time	t_{AA}			250	ns	
Chip Enable Access Time	t_{ACE}			250	ns	
Output Delay Time	t_{CO}			100	ns	
Output Setting Time	t_{LZ}	10			ns	
Output Disable Time	t_{HZ}	10		100	ns	
Output Retaining Time	t_{OH}	10			ns	
Power Up Time	t_{PU}	0			ns	
Power Down Time	t_{PD}			100	ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



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Notes: (1) $\overline{CE}$ is "L" level.
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) $\overline{OE}$ and $\overline{CS}$ are shown in the negative logic here, however the active level is freely selected.
(4) t_{CO} and t_{LZ} are determined by the later $\overline{CE}$ "L", $\overline{OE}$ "L" or $\overline{CS}$ "L".
t_{HZ} is determined by the earlier $\overline{CE}$ "H", $\overline{OE}$ "H" or $\overline{CS}$ "H".
t_{HZ} shows time until floating therefore it is not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I		8	pF	V_I=0V
Output Capacitance	C_O		10	pF	V_O=0V

9

OKI semiconductor

MSM38256ARS

32768 WORD x 8 BIT MASK ROM (E3-S-030-32)

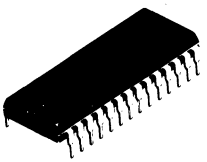
GENERAL DESCRIPTION

The MSM38256ARS is an N-channel silicon gate E/DMOS device ROM with a 32,768 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 6mA (max) when the chip is not selected. The application of a byte system and the pin compatibility with standard UV EPROMs make the device most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.

Since it provides CE, OE, CS signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

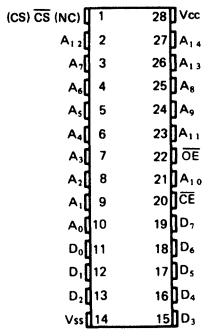
FEATURES

- 32768 words x 8 bits
- 5V single power supply
- Access time: 150 ns MAX
- Input/output TTL compatible
- 3-state output
- Power down mode
- 28-pin DIP



PIN CONFIGURATION

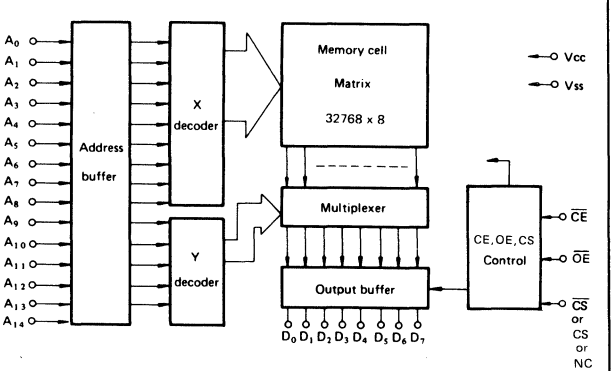
(Top View)



$\overline{CE}$	:	Chip enable
$\overline{OE}$	:	Output enable
(CS) $\overline{CS}$	:	Chip select
Vcc, Vss	:	Power supply voltage
$A_0 \sim A_{13}$	:	Address input
$D_0 \sim D_7$	:	Data output
(NC)	:	No Connection

Note: $\overline{CS}$ active level is specified by customers.

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	V_{CC}	−0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.5 to 7	V	
Output Voltage	V_O	−0.5 to 7	V	
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	PD	1.0	W	Per package

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Conditions	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}		4.5	5	5.5	V
	V_{SS}		0	0	0	V
"H" Input Signal Level	V_{IH}		2.2	5	6	V
"L" Input Signal Level	V_{IL}		−0.5	0	0.8	V
"H" Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4		V_{CC}	V
"L" Output Signal Level	V_{OL}	I_{OL} = 2.1 mA			0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	−10		10	μA
Output Leakage Current	I_{LO}	V_O = 0V or V_{CC} Chip not selected	−10		10	μA
Power Supply Current	I_{CC}	V_{CC} = Max. I_O = 0 mA			60	mA
	I_{CCS}	V_{CC} = Max.			6	mA
Peak Power On Current	I_{PO}	V_{CC} = GND ~ V_{CC} Min. CE = V_{CC} or V_{IH}			60	mA
Operating Temperature	Topr		0		70	°C
Load Capacitance	C_L				100	pF
Fan Out	N	TTL Load			1	Piece

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AC CHARACTERISTICS

TIMING CONDITIONS

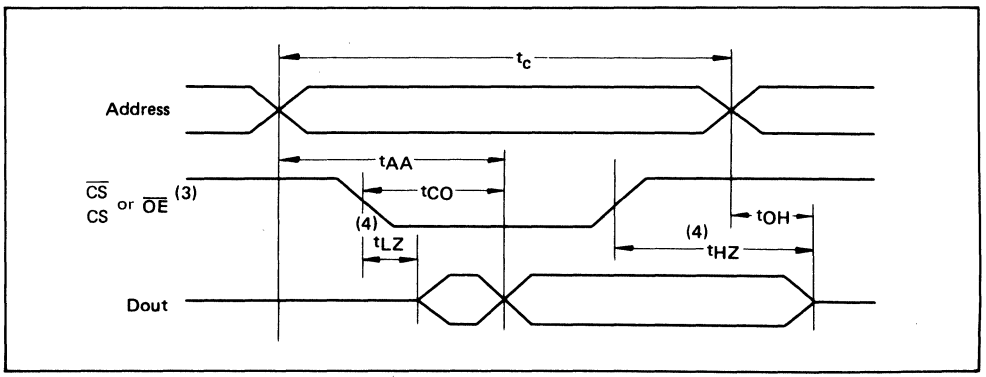
Parameter	Conditions
Input Signal Level	V_{IH}=2.4V V_{IL}=0.6V
Input Rising, Falling Time	tr=tf=15 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8 & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

READ CYCLE

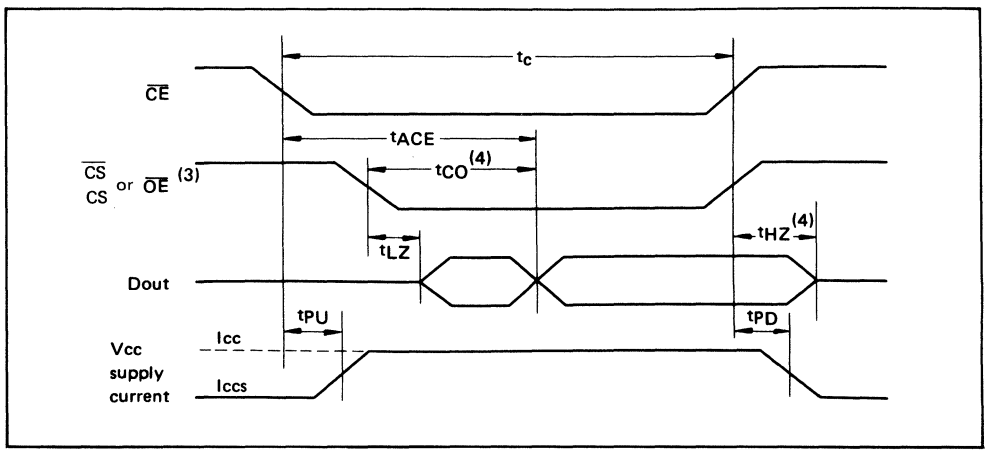
(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_c	150			ns	
Address Access Time	t_{AA}			150	ns	
Chip Enable Access Time	t_{ACE}			150	ns	
Output Delay Time	t_{CO}			50	ns	
Output Setting Time	t_{LZ}	10			ns	
Output Disable Time	t_{HZ}	10		50	ns	
Output Retaining Time	t_{OH}	10			ns	
Power Up Time	t_{PU}	0			ns	
Power Down Time	t_{PD}			100	ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



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Notes: (1) $\overline{CE}$ is "L" level.
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) $\overline{CS}$ are shown in the negative logic here, however the active level is freely selected.
(4) t_{CO} and t_{LZ} are determined by the later $\overline{CE}$ "L", $\overline{OE}$ "L" or $\overline{CS}$ "L".
t_{HZ} is determined by the earlier $\overline{CE}$ "H", $\overline{OE}$ "H" or $\overline{CS}$ "H".
t_{HZ} shows time until floating therefore it is not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I		8	pF	V_I=0V
Output Capacitance	C_O		6	pF	V_O=0V

9

OKI semiconductor

Preliminary

MSM38512RS

65536 WORD x 8 BIT MASK ROM

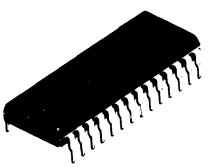
GENERAL DESCRIPTION

The MSM38512RS is an N-channel silicon gate E/DMOS device ROM with a 65,536 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 10mA(max) when the chip is not selected. The application of a byte system and the pin compatibility with standard UV EPROMs make the device most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.

Since it provides $\overline{CE}$, $\overline{OE}$, signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

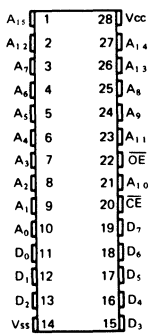
FEATURES

- 512k bits: 65,536 words x 8 bit
- high speed: access time 200 ns max
- low power: active current 60 mA max
  standby current 10 mA max
- wide tolerance operating: Vcc = 5 V ± 10 %
- fully static operating: using no clock
- fully TTL compatible
- pin compatible to 512k EPROM
- packaged to 28 pins plastic
- fabricated with 2um NMOS silicon gate technology



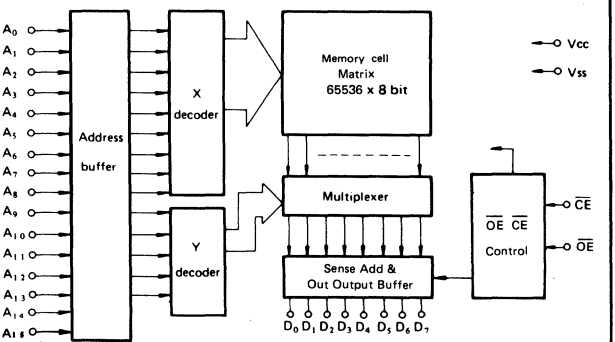
PIN CONFIGURATION

(Top View)



$\overline{OE}$	: Output enable
Vcc, Vss	: Power supply voltage
A_0—A_{15}	: Address input
$\overline{CE}$	: Chip enable
D_0— D_7	: Data output

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	Vcc	−0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.5 to 7	V	Respect to V_{SS}
Output Voltage	V_O	−0.5 to 7	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Par package
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	Vcc	−	4.5	5	5.5	V
	Vss	−	0	0	0	V
Input Signal Level	V_{IH}	−	2.2	−	6	V
	V_{IL}	−	−0.3	−	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4	−	−	V
	V_{OL}	I_{OL} = 2.1 mA	−	−	0.4	V
Input Leak Current	I_{LI}	V_I = 0V or V_{CC}	−10	−	10	μA
Output Leak Current	I_{LO}	V_O = 0V or V_{CC} Chip not selected	−10	−	10	μA
Power Supply Current	Icc		−	−	60	mA
	Iccs		−	−	10	mA

AC CHARACTERISTICS

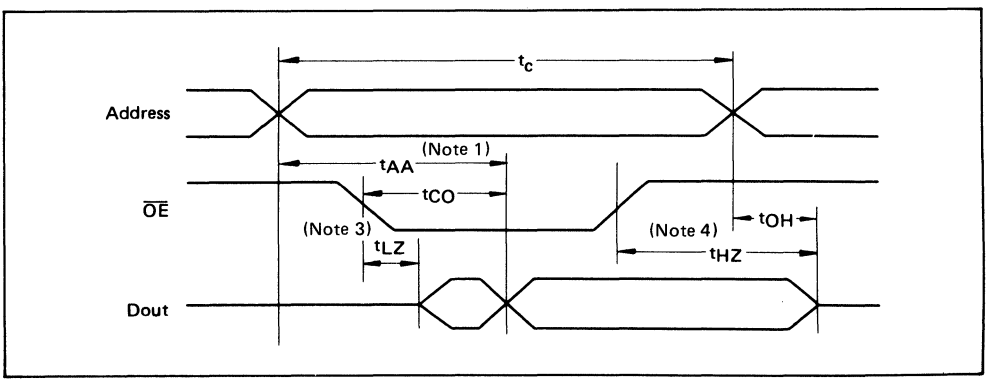
TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V_{IH} 2.4V, V_{IL} 0.6 V
Input Rising, Falling Time	tr = tf = 15 ns
Timing Measuring Point Voltage	Input Voltage = 1.5V
	Output Voltage = 0.8V & 2.0V
Loading Condition	C_L = 100 pF + 1 TTL

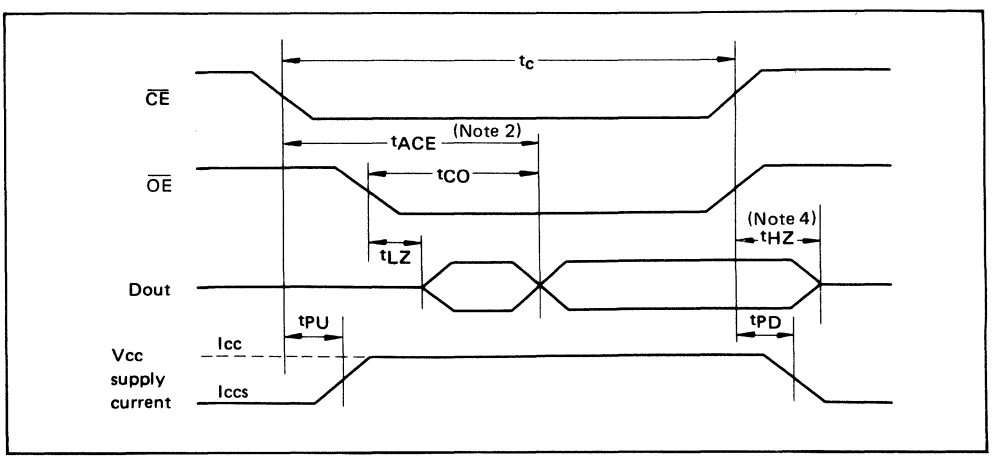
READ CYCLE

Parameter	Symbol	xxxxxx Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_C	200	–	–	ns	
Address Access Time	t_{AA}	–	–	200	ns	
Chip Enable Access Time	t_{ACE}	–	–	200	ns	
Output Delay Time	t_{CO}	–	–	50	ns	
Output Setting Time	t_{LZ}	10	–	–	ns	
Output Disable Time	t_{HZ}	10	–	50	ns	
Output Retaining Time	t_{OH}	10	–	–	ns	
Power Up Time	t_{PU}	0	–	–	ns	
Power Down Time	t_{PD}	–	–	100	ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



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Notes: (1) $\overline{CE}$ is "L" level
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) t_{LZ} is determined by the later level, $\overline{CE}$ "L" or $\overline{OE}$ "L".
(4) t_{HZ} is determined by the earlier $\overline{CE}$ "H" or $\overline{OE}$ "H".
While, t_{HZ} shows the time until floating and it is therefore not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I		8	pF	V_I = 0V
Output Capacitance	C_O		10	pF	V_O = 0V

OKI semiconductor

MSM28101AAS

JAPANESE-CHARACTER GENERATING 1M BIT MASK ROM (E3-S-032-32)

GENERAL DESCRIPTION

The MSM 28101AAS is a 1M Bit Mask ROM using the N-channel silicon gate MOS process which stores 3,760 characters of numeric characters, Japanese cursive and square syllabarys, JIS 1st standard Japanese-characters, etc., in one chip.

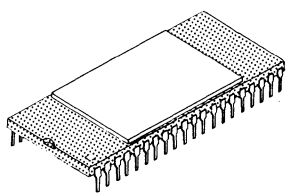
Because of its large capacity, Japanese-character pattern of 3,760 characters can be generated with only one chip. Furthermore, since the dot matrix character form of 18 lines x 16 strings is available from the data out pin by only inputting the JIS Japanese-character code into the address pin, the MSM28101AAS is efficient and optimum for constituting the Japanese-character terminal.

The power supply voltage is of 5 V single power supply, the input level is of TTL compatible, the data output is of 3-state output, the data valid is the output of the open collector and is packaged on the 40-pin DIP.

FEATURES

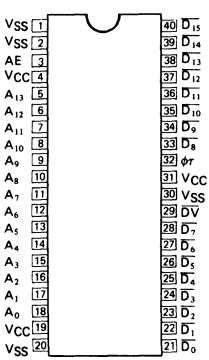
• Function	18 x 16 chinese-character font output
• Configuration	Duplex configuration of cell-array using the defect permissible technique
• Storage capacity	1082880 Bits
• Number of generating characters	3,418 characters
• Storage character range	Partition 0 ~ 7 and partition 16 ~ 47 of Japanese-character code system for JIS information processing
• Address input	14 Bits ($A_0 \sim A_{13}$)
• Data output	16 Bits ($\overline{D_0} \sim \overline{D_{15}}$, 3-state)
• Output mode	16 Bits x 18 times transfer
• Address enable	1 each (AE)
• Data valid	1 each ($\overline{DV}$, open collector output)
• Clock	1 each (ϕT) DC ~ 1.5MHz
• Used temperature	Ta = 0 ~ 70°C
• Access time	10 μs MAX
• Data transfer rate	22 μs/character
• Interface	TTL level
• Power supply voltage	5V single power supply (±5%)
• Power consumption	700 mW TYP
• Package	Side-brazed 40-pin DIP
• Memory cell	Multi-gate ROM

This specification is subject to change without notice



PIN CONFIGURATION

(Top View)



$A_0 \sim A_{13}$: Address input
$\overline{D_0} \sim \overline{D_{15}}$: Data output
AE: Address enable
$\overline{DV}$: Data valid output
ϕT: Clock input
V_{CC}: Power supply voltage (5V)
V_{SS}: GND (OV)

(Note) Connect all V_{CC} and V_{SS} terminals.

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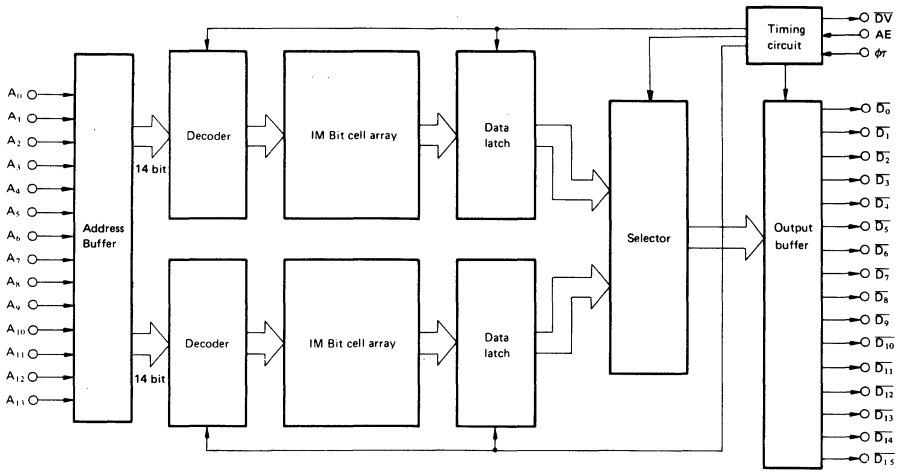
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Conditions	Value	Unit
Power Supply Voltage	Vcc	Respect to Vss	−0.5 ~7	V
Input Terminal Voltage	V_{IN}	Respect to Vss	−0.5 ~7	V
Output Terminal Voltage	V_{OUT}	Respect to Vss	−0.5 ~7	V
Power Dissipation	P_D		2	W
Operating Temperature	T_{opr}		0 ~70	°C
Storage Temperature	T_{stg}		−35 ~ 125	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Specification value			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	Vcc	5V ± 5%	4.75	5	5.25	V
Power Supply Voltage	Vss		0	0	0	V
Input Signal Level	V_{IH}	Respect to Vss	2.0	5	6	V
	V_{IL}	Respect to Vss	−0.5	0	0.8	V
Operating Temperature	Topr		0		70	°C

DC CHARACTERISTICS

(Vcc = 5V ±5%, Ta = 0°C to +70°C)

Parameter	Symbol	Conditions	Specification value			Unit
			Min.	Typ.	Max.	
Output Signal Level	V_{OH}	I_{OH}=–0.2 mA	2.4		Vcc	V
	V_{OL}	I_{OL} =1.6 mA			0.4	V
Input Leakage Current	I_{LI}	V_{IN}=0 ~Vcc	–10		10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 ~Vcc V_{AE}=0.8V	–10		10	μA
Average Power Supply Current	I_{CCA}	t_{RC}=22μs t_C=650 ms t_{AR}=300 ns			170	mA
Steady State Power Supply Current	I_{CCS}	V_{AE}=0.8V			170	mA

AC CHARACTERISTICS

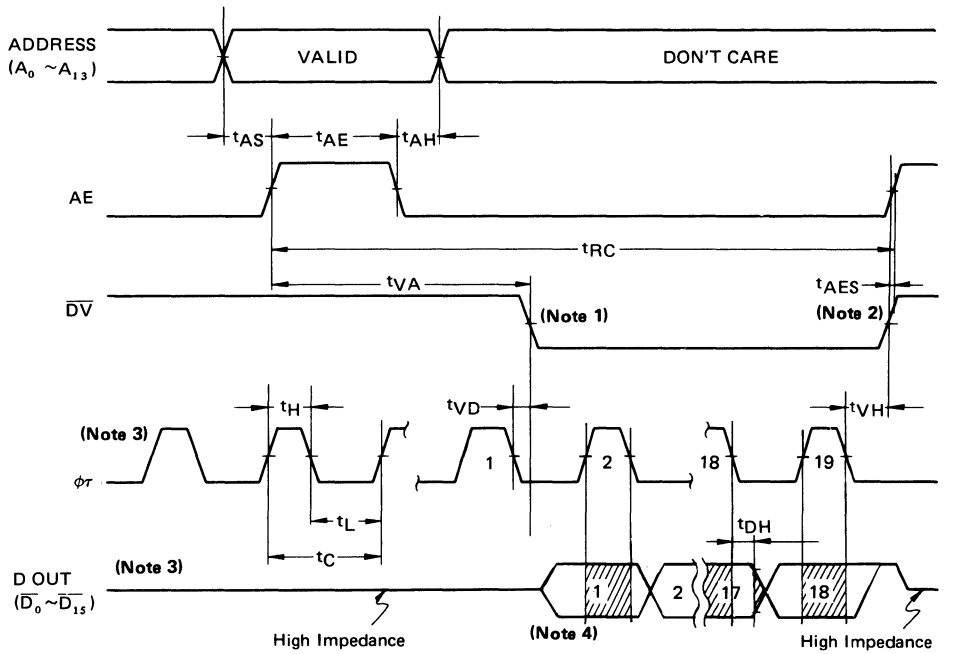
TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V_{IH} = 2.0V, V_{IL} = 0.8V
Input Rising, Falling Time	t_r = t_f = 15 ns
Input Timing Level	1.5V
Loading Condition	C_L = 50 pF, 1TTL Gate

READ CYCLE

(Vcc = 5V ±5%, T_a = 0°C to +70°C)

Parameter	Symbol	Conditions	Specification Value			Unit
			Min.	Typ.	Max.	
Read Cycle Time	t_{RC}		22			μS
Address Setting Time	t_{AS}		0			ns
AE Pulse Width	t_{AE}		300			ns
Address Retaining Time	t_{AH}		100			ns
$\overline{DV}$ Access Time	t_{VA}				10	μS
$\overline{DV}$ Delay Time	t_{VD}				150	ns
$\overline{DV}$ Retaining Time	t_{VH}				100	ns
ϕ_T Pulse Width	t_H		200			ns
ϕ_T Delay Time	t_L		450			ns
Output Retaining Time	t_{DH}		50			ns
AE Setting Time	t_{AES}		0			ns



(Note 1) $\overline{DV}$ is determined by the falling of ϕT.
(Note 2) $\overline{DV}$ changes with the falling of ϕT.
(Note 3) ϕT and Dn DATA are repeated 18 times during $\overline{DV}$ is Low.
(Note 4) The $\overline{Dn}$ timing levels are 2.0 V and 0.8 V.
(Note 5) Sometimes it will not normally operate unless input is made at least once with AE as the dummy after input of power supply.
(Note 6) $\overline{DV}$ is an open collector output and $\overline{Dn}$ is a 3-stage output.

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INPUT/OUTPUT CAPACITANCE

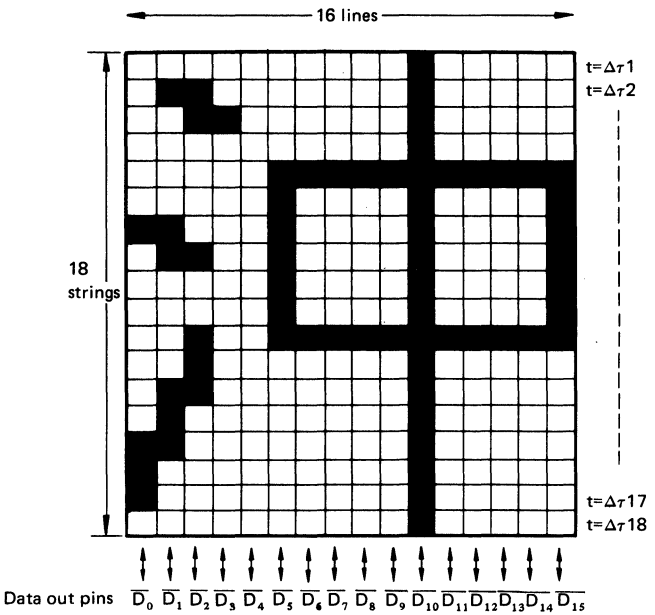
(Ta = 25°C, f = 1 MHz)

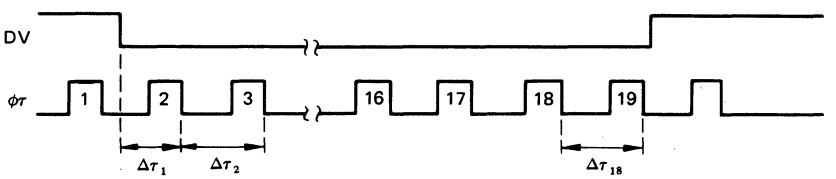
Parameter	Symbol	Conditions	Specification value			Unit
			Min.	Typ.	Max.	
Input Capacitance (excluding AE)	C_{IN}	V_{IN} = OV			8	pF
Input Capacitance (AE terminal)	C_{IN}	V_{IN} = OV			15	pF
Output Capacitance	C_{OUT}	V_{OUT} = OV			8	pF

FUNCTIONAL CHARACTERISTICS

Parameter	Specification	Unit	Remarks
Font Type	18 lines x 16 strings dot matrix		
Output Mode	16 bits x 18 times transfer		**(Note 1)**
Number of Generating characters	3418	Word	
Storage Character Range	0 ~ 7 (Non chinese-character area) 16 ~ 47 (JIS 1st standard)	Partition	**(Note 2)**

(Note 1) The correspondence of the 18 lines x 16 strings matrix and the data out pins are as shown in the diagram below.
Output for the character portion will be Low (V_{OL}) and the output for the background portion will be High (V_{OH}).





(Note 2) The correspondence of the 1st and 2nd bytes of JIS C 6226 and the address pins are as shown below.

JIS C 6226	Second byte							First byte						
	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_7	b_6	b_5	b_4	b_3	b_2	b_1
Address Pin	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

OKI semiconductor

MSM28201AAS

1M BIT MASK ROM FOR JAPANESE-CHARACTER PATTERN (E3-S-033-32)

GENERAL DESCRIPTION

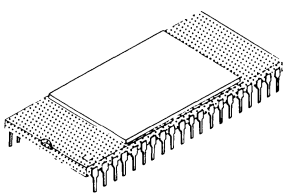
The MSM28201AAS is a 1M-bit mask ROM employing an N-channel silicon gate MOS process, and with 3760 Japanese-characters (kanji conforming with JIS No. 2 standards) incorporated in single chip.

With this large capacity, 3760 Japanese-character patterns can be generated in a single chip. And by only a single input of JIS Japanese-character code via the address pin, 18-row x 16-column dot matrix character forms can be obtained from the data output pin, making this device ideal for construction of functionally versatile Japanese-character terminals.

The power supply voltage is 5V single, the input level TTL compatible, outputs are tri-state data out, and data valid is denoted by open collector. The device is mounted in a 40-pin DIP.

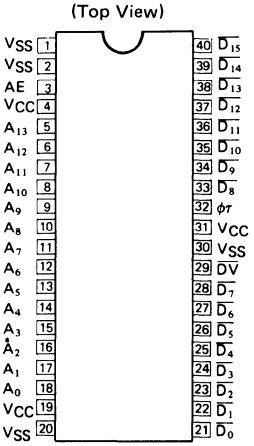
FEATURES

- Function . . . . . 18 x 16 chinese-character font output
- Configuration . . . . Duplex configuration employing defect permissible technique
- Storage capacity . . . 1082880 bits
- Number of generated characters . . . . . 3384 characters
- Accommodation . . . Japanese-character encoded character region partitions 48 to 87 for JIS data processing.
- Address input . . . . 14 bits (A_0 to A_{13})
- Data output . . . . . 16 bits ($\overline{D_0}$ to $\overline{D_{15}}$, tristate)
- Output mode . . . . 16 bit x 18 transfers
- Address enable . . . 1 (AE)
- Data valid . . . . . 1 ($\overline{DV}$, open collector output)
- Clock . . . . . 1 (ϕT) DC to 1.5MHz
- Operating temperature . . . . . Ta=0°C to 70°C
- Access time . . . . . 10 μs MAX.
- Data transfer rate . . 22 μs/character
- Interface . . . . . TTL level
- Power supply voltage 5V single (±5%)
- Power consumption . 700 mW TYP
- Package . . . . . Side-brazed 40-pin DIP
- Memory cell . . . . . Multi-gate ROM



PIN CONFIGURATION

(Top View)



$A_0 \sim A_{13}$: Address inputs
$\overline{D_0} \sim \overline{D_{15}}$: Data outputs
AE : Address enable
$\overline{DV}$: Data valid output
ϕT : Clock input
Vcc : Power supply voltage (5 V)
Vss : GND (0 V)

Note: All Vss pins are to be connected

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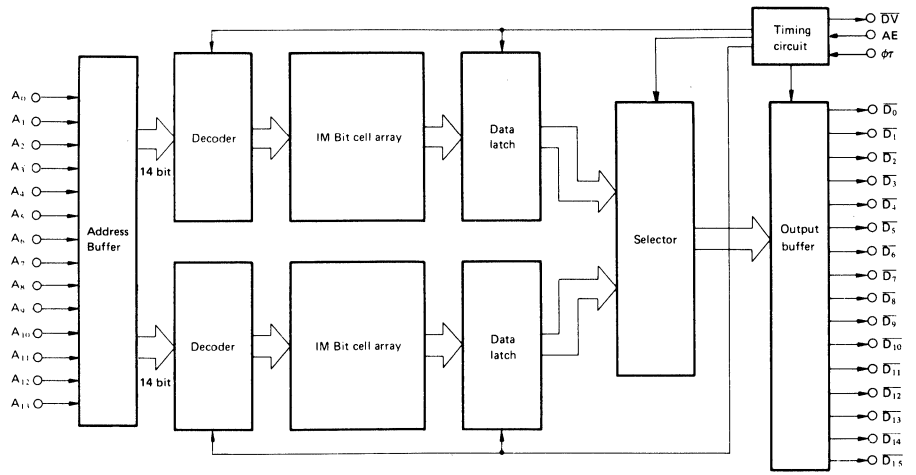
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Conditions	Value	Unit
Power Supply Voltage	Vcc	Respect to Vss	−0.5~7	V
Input Voltage	V_I	Respect to Vss	−0.5~7	V
Output Voltage	V_O	Respect to Vss	−0.5~7	V
Power Dissipation	P_D		2	W
Operating Temperature	Topr		0 ~ 70	°C
Storage Temperature	Tstg		−35~125	°C

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Range Value			Unit
			Min	Typ	Max	
Power Supply Voltage	Vcc	5 V ± 5%	4.75	5	5.25	V
Power Supply Voltage	Vss		0	0	0	V
"H" Input Voltage	V_{IH}	Respect to Vss	2.0	5	6	V
"L" Input Voltage	V_{IL}	Respect to Vss	−0.5	0	0.8	V
Operating Temperature	Topr		0		70	°C

DC CHARACTERISTICS

(V_{CC} = 5V ±5%, Ta = 0°C to +70°C)

Parameter	Symbol	Conditions	Range Value			Unit
			Min.	Typ.	Max.	
"H" Output Voltage	V_{OH}	I_{OH} = −0.2 mA	2.4		V_{CC}	V
"L" Output Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input Leakage Current	I_{LI}	V_I = 0 ~ V_{CC}	−10		10	μA
Output Leakage Current	I_{LO}	V_O = 0 ~ V_{CC} V_{AE} = 0.8V	−10		10	μA
Average Power Supply Current	I_{CCA}	t_{RC} = 22μS, t_C = 650 ns t_{AE} = 300ns			170	mA
Rated Power Supply Current	I_{CCS}	V_{AE} = 0.8V			170	mA

AC CHARACTERISTICS

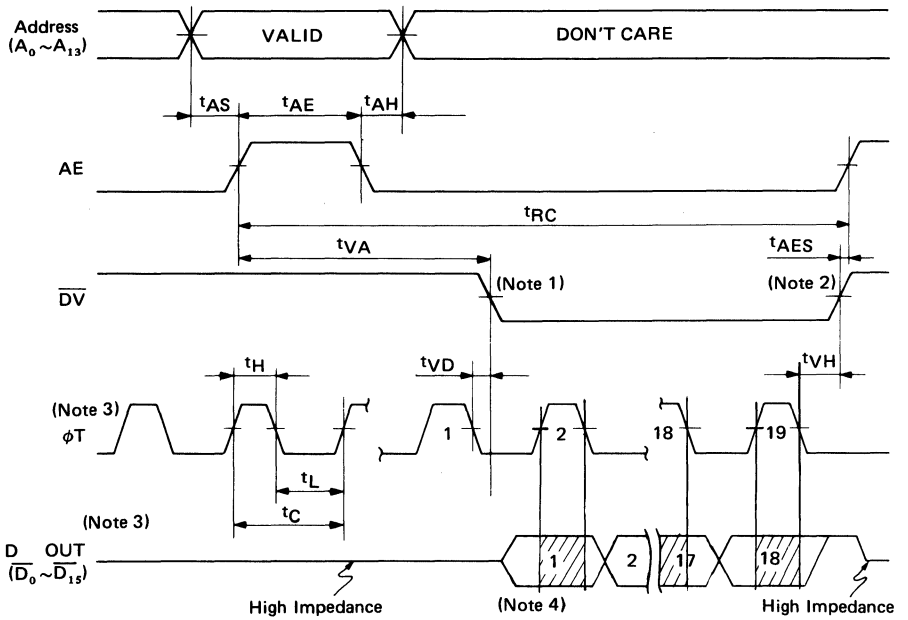
TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V_{IH}=2.0 V, V_{IL}=0.8 V
Input Rise/Fall Time	tr=tf=15ns
Input Timing Level	1.5V
Output Load	C_L=50pF, 1TTL Gate

READ CYCLE

(V_{CC} = 5V ±5%, Ta = 0°C to +70°C)

Parameter	Symbol	Conditions	Specification Value			Unit
			Min.	Typ.	Max.	
Read Cycle Time	t_{RC}		22			μS
Address Setting Time	t_{AS}		0			ns
AE Pulse Width	t_{AE}		300			ns
Address Retaining Time	t_{AH}		100			ns
$\overline{DV}$ Access Time	t_{VA}				10	μS
$\overline{DV}$ Delay Time	t_{VD}				150	ns
$\overline{DV}$ Retaining Time	t_{VH}				100	ns
ϕ_T Pulse Width	t_H		200			ns
ϕ_T Delay Time	t_L		450			ns
Output Retaining Time	t_{DH}		50			ns
AE Setting Time	t_{AES}		0			ns



Notes:
1. $\overline{DV}$ is determined by the φT falling edge.
2. $\overline{DV}$ is changed by the φT falling edge.
3. φT and DnDATA are repeated 18 times when $\overline{DV}$ is low.
4. $\overline{Dn}$ timing levels of 2.0V and 0.8V.
5. Normal operation may not be possible unless there is at least one AE dummy input after the power is switched on.
6. $\overline{DV}$ denotes open collector output, and $\overline{Dn}$ the tristate output.

INPUT/OUTPUT CAPACITANCE

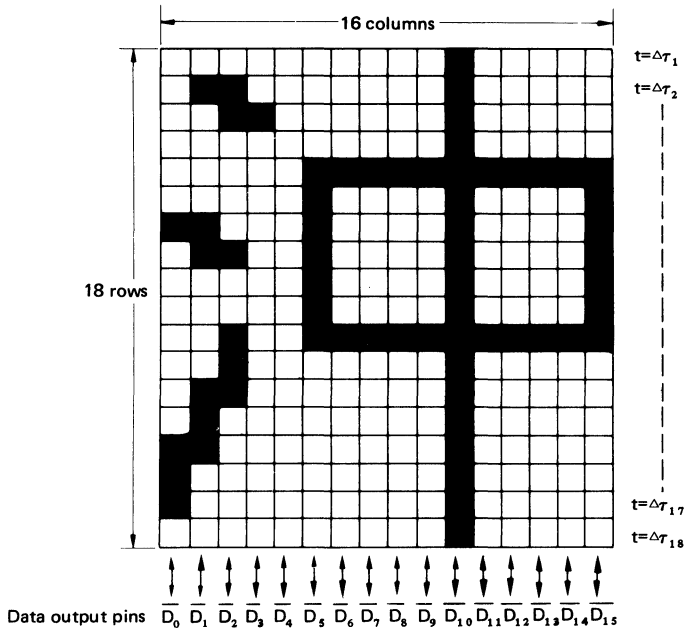
(Ta=25°C, f=1 MHz)

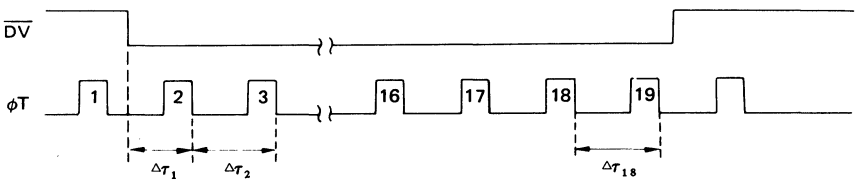
Parameter	Symbol	Conditions	Range Value			Unit
			Min.	Typ.	Max.	
Input Capacitance (excluding AE)	C_I	V_I=0 V			15	pF
Input Capacitance (AE pin)	C_I	V_I=0 V			35	pF
Output Capacitance	C_O	V_O=0 V			10	pF

FUNCTIONAL CHARACTERISTICS

Parameter	Range	Unit	Remarks
Font Format	18-row x 16-column dot matrix		
Output Mode	16 bit x 18 transfers		(Note 1)
Number of Characters Generated	3384	Word	
Character Accommodation Region	48~87 (JIS No.2 standard)	Partition	(Note 2)

Note 1. The relation between the 18-row x 16-column matrix and the data output pins is outlined below. The output is low (V_{OL}) for the character portion, and high (V_{OH}) for the background area.





Note 2. The address pins are related to the JIS C6226 no.1 and no.2 bytes in the following way.

JIS C 6226	No.2 byte							No.1 byte						
	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_7	b_6	b_5	b_4	b_3	b_2	b_1
Address Pin	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

OKI semiconductor

MSM53256RS

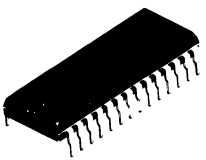
32,768 WORD x 8 BIT MASK ROM

GENERAL DESCRIPTION

The MSM53256RS is a silicon gate CMOS device ROM with 32,768 words x 8 bit capacity. It operates on a 5V single power supply and all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation when the chip is not selected. The application of a byte system is most suitable for use as a large capacity fixed memory for microcomputers and data terminals.
Since it provides signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

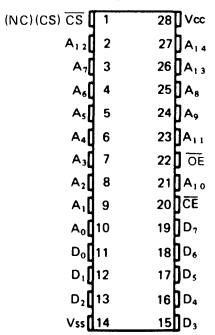
FEATURES

- 256k bits: 32,768 words x 8 bits
- High speed: access time 150 ns max
- Low power: active current 15 mA max
  standby current 0.1 mA max
- Wide tolerance operating: Vcc = 5V ± 10%
- Fully static operating: using no clock
- Fully TTL compatible
- Pin compatible to 256k EPROM
- Packaged to 28 pins plastic
- Fabricated with CMOS silicon gate technology



PIN CONFIGURATION

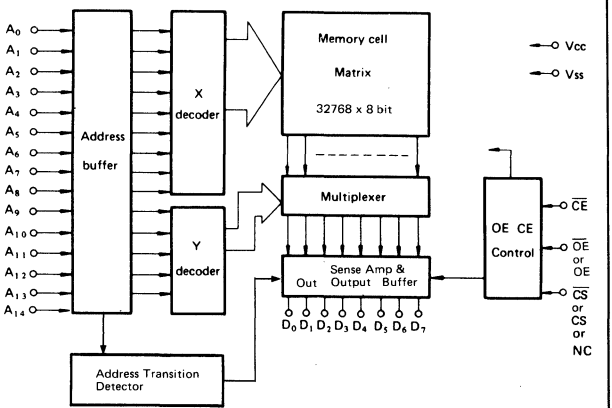
(Top View)



$\overline{CS}$	: Chip select
$\overline{OE}$	: Output enable
Vcc, Vss	: Power supply voltage
$A_0 \sim A_{13}$	: Address input
$D_0 \sim D_7$	: Data output
$\overline{CE}$	: CHip enable

Note: $\overline{CS}$ active level is specified by customer.

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	Vcc	−0.3 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.3 to Vcc + 0.3	V	Respect to V_{SS}
Output Voltage	V_O	−0.3 to Vcc + 0.3	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	T_{opr}	0 to 70	°C	—
Storage Temperature	T_{stg}	−55 to 150	°C	—

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	—	4.5	5	5.5	V
	V_{SS}	—	0	0	0	V
Input Signal Level	V_{IH}	—	2.2	5	Vcc +0.3	V
	V_{IL}	—	−0.3	0	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4	—	—	V
	V_{OL}	I_{OL} = 2.1 mA	—	—	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	−10	—	10	μA
Output Leakage Current	I_{LO}	V_O = 0V or Vcc Chip not selected	−10	—	10	μA
Power Supply Current	I_{CCA}	Vcc = Max. I_O = 0 mA, t_C = 150 ns	—	—	15	mA
	I_{CCS}	Vcc = Max. $\overline{CE}$ = Vcc − 0.2V	—	—	0.1	mA
	I_{CCS1}	Vcc = Max. $\overline{CE}$ = V_{IH} min.	—	—	0.5	mA
Operating Temperature	T_{opr}	—	0	—	70	°C

AC CHARACTERISTICS

TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rising, Falling Time	tr=tf=15 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8V & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

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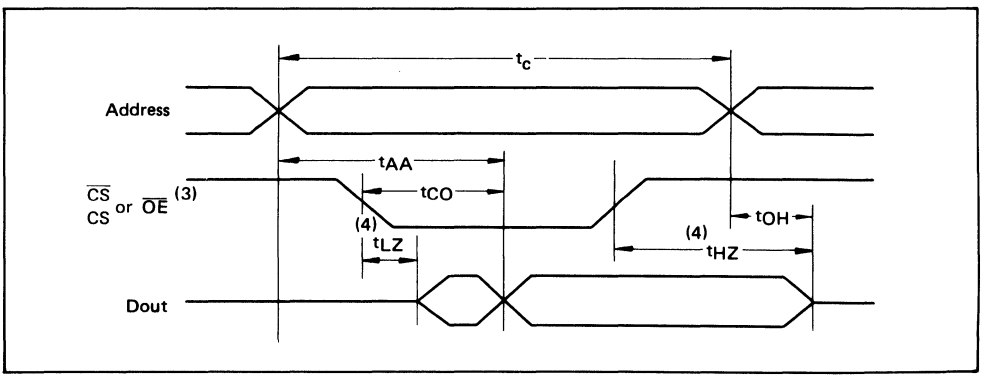
READ CYCLE

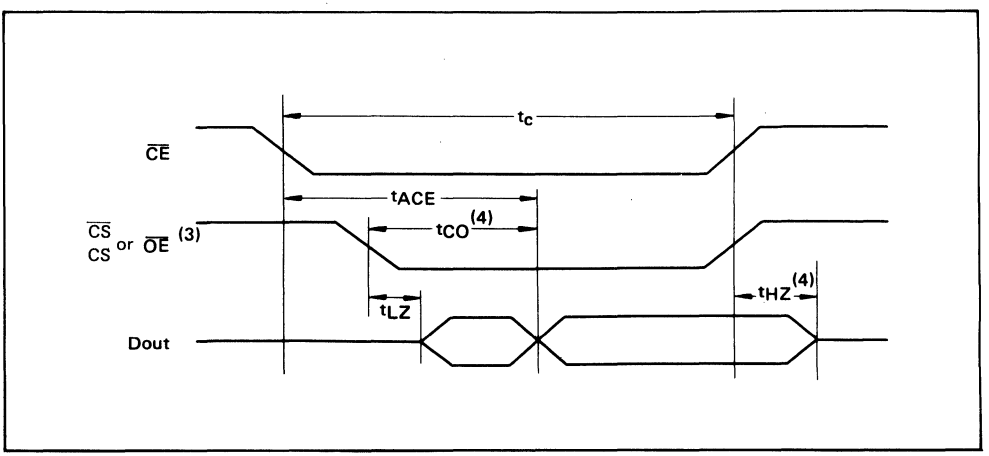
(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_C	150			ns	
Address Access Time	t_{AA}			150	ns	
Chip Enable Access Time	t_{ACE}			150	ns	
Output Delay Time	t_{CO}			50	ns	
Output Setting Time	t_{LZ}	10			ns	
Output Disable Time	t_{HZ}	10		50	ns	
Output Retaining Time	t_{OH}	10			ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



Notes: (1) $\overline{CE}$ is "L" level.
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) $\overline{CS}$ are shown in the negative logic here, however the active level is freely selected.
(4) t_{CO} and t_{LZ} are determined by the later $\overline{CE}$ "L", $\overline{OE}$ "L" or $\overline{CS}$ "L".
t_{HZ} is determined by the earlier $\overline{CE}$ "H", $\overline{OE}$ "H" or $\overline{CS}$ "H".
t_{HZ} shows time until floating therefore it is not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I		8	pF	V_I=0V
Output Capacitance	C_O		6	pF	V_O=0V

OKI semiconductor

MSM531000RS

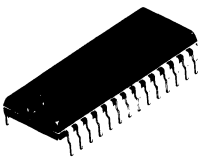
131,072 WORD x 8 BIT MASK ROM (E3-S-031-32)

GENERAL DESCRIPTION

The MSM531000RS is a silicon gate CMOS device ROM with 131,072 words x 8 bit capacity. It operates on a 5V single power supply and all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation when the chip is not selected. The application of a byte system is most suitable for use as a large capacity fixed memory for microcomputers and data terminals.
Since it provides signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

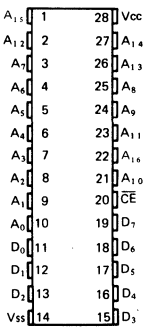
FEATURES

- 131,072 words x 8 bits
- 5V single power supply
- Access time: 250 ns MAX
- Input/output TTL compatible
- 3-state output
- 28-pin DIP



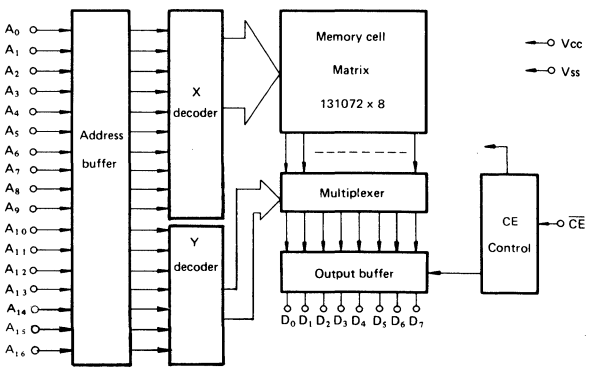
PIN CONFIGURATION

(Top View)



Vcc, Vss : Power supply voltage
$A_0 \sim A_{13}$: Address input
$D_0 \sim D_7$: Data output
$\overline{CE}$: Chip enable

FUNCTIONAL BLOCK DIAGRAM



9

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	Vcc	−0.3 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.3 to Vcc + 0.3	V	Respect to V_{SS}
Output Voltage	V_O	−0.3 to Vcc + 0.3	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	T_{opr}	0 to 70	°C	—
Storage Temperature	T_{stg}	−55 to 150	°C	—

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	—	4.5	5	5.5	V
	V_{SS}	—	0	0	0	V
Input Signal Level	V_{IH}	—	2.2	5	Vcc +0.3	V
	V_{IL}	—	−0.3	0	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4	—	—	V
	V_{OL}	I_{OL} = 2.1 mA	—	—	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	−10	—	10	μA
Output Leakage Current	I_{LO}	V_O = 0V or Vcc Chip not selected	−10	—	10	μA
Power Supply Current	I_{CCA}	Vcc = Max. I_O = 0 mA, t_C = 250 ns	—	—	15	mA
	I_{CCS}	Vcc = Max. $\overline{CE}$ = Vcc − 0.2V	—	—	0.1	mA
	I_{CCS1}	Vcc = Max. $\overline{CE}$ = V_{IH} min.	—	—	0.5	mA
Operating Temperature	T_{opr}	—	0	—	70	°C

AC CHARACTERISTICS

TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rising, Falling Time	tr=tf=15 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8V & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

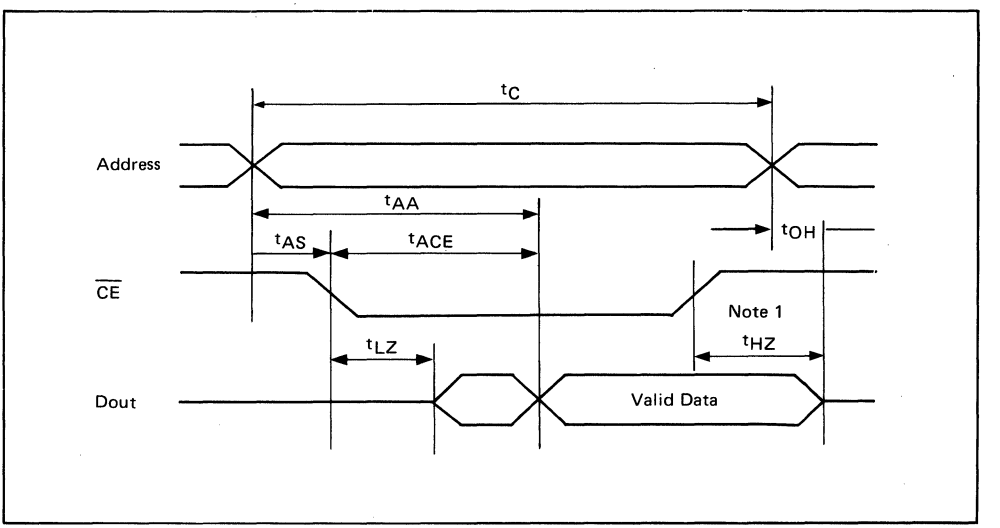
9

READ CYCLE

(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_C	250	–	–	ns	
Address Access Time	t_{AA}	–	–	250	ns	
Chip Enable Access Time	t_{ACE}	–	–	250	ns	
Address Setting Time	t_{AS}	0	–	–	ns	
Output Setting Time	t_{LZ}	10	–	–	ns	
Output Disable Time	t_{HZ}	10	–	80	ns	
Output Retaining Time	t_{OH}	10	–	–	ns	

READ CYCLE



Note: t_{HZ} shows the time until floating and it is therefore not determined by the output level.

9

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I	–	8	pF	V_I=0V
Output Capacitance	C_O	–	6	pF	V_O=0V

MOS EPROMS

MSM2764AS

8192 × 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

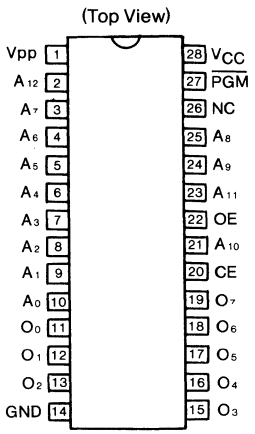
GENERAL DESCRIPTION

The MSM2764 is a 8192 words × 8 bit ultraviolet erasable and electrically programmable read-only memory. Users can freely prepare the memory content, which can be easily changed, so the MSM2764 is ideal for microprocessor programs, etc. The MSM2764 is manufactured by the N channel double silicon gate MOS technology and is contained in the 28 pin package.

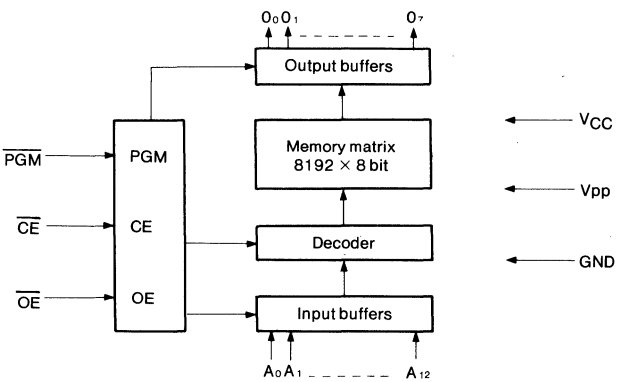
FEATURES

- +5V single power supply
- 8192 words × 8 bit configuration
- Access time:
  MAX200 ns (MSM2764-20)
  MAX250 ns (MSM2764-25)
  MAX300 ns (MSM2764-30)
- Power consumption:
  MAX525 mW (during operation)
  MAX184 mW (during stand-by)
- Perfect static operation
- INPUT/OUTPUT TTL level
  (three state output)

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	Vpp (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	–	+5V	+5V	High impedance
Program	V_{IL}	–	V_{IL}	+21V	+6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+21V	+6V	Dout
Program Inhibit	V_{IH}	–	–	+21V	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	–10°C ~ 80°C
Storage Temperature	Tstg	–55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	–0.6V ~ 13.5V
V_{CC} Supply Voltage	V_{CC}	–0.3V ~ 7V
Program Voltage	Vpp	–0.6V ~ 23V
Power Assembly Voltage	P_D	1.5W

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±0.25V Vpp=V_{CC}±0.6V	V
Vpp Voltage	Vpp	4.15	5.0	5.85			V
"H" Level Input Voltage	V_{IH}	2.00	–	6.25			V
"L" Level Input Voltage	V_{IL}	–0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}±0.6V, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC_1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC_2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Program Power Current	I_{PP_1}	Vpp = V_{CC}±0.6V	–	–	5	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

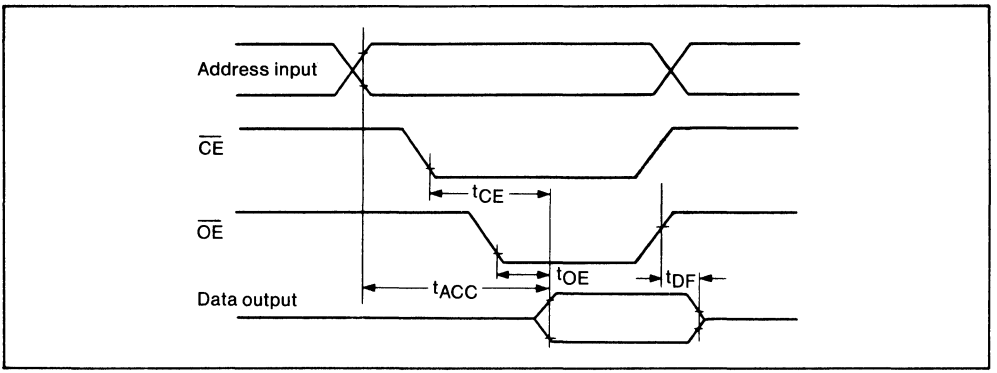
(V_{CC} = 5V±5%, Vpp = V_{CC}±0.6V, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	2764-20		2764-25		2764-30		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	200	–	250	–	300	ns
CE Access Time	t_{CE}	$\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	200	–	250	–	300	ns
OE Access Time	t_{OE}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	70	–	100	–	120	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	60	0	85	0	105	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

TIME CHART


Address input
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{OE}
t_{DF}
t_{ACC}
Data output

<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 6V±0.25V, Vpp = 21V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	Ipp	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	30	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

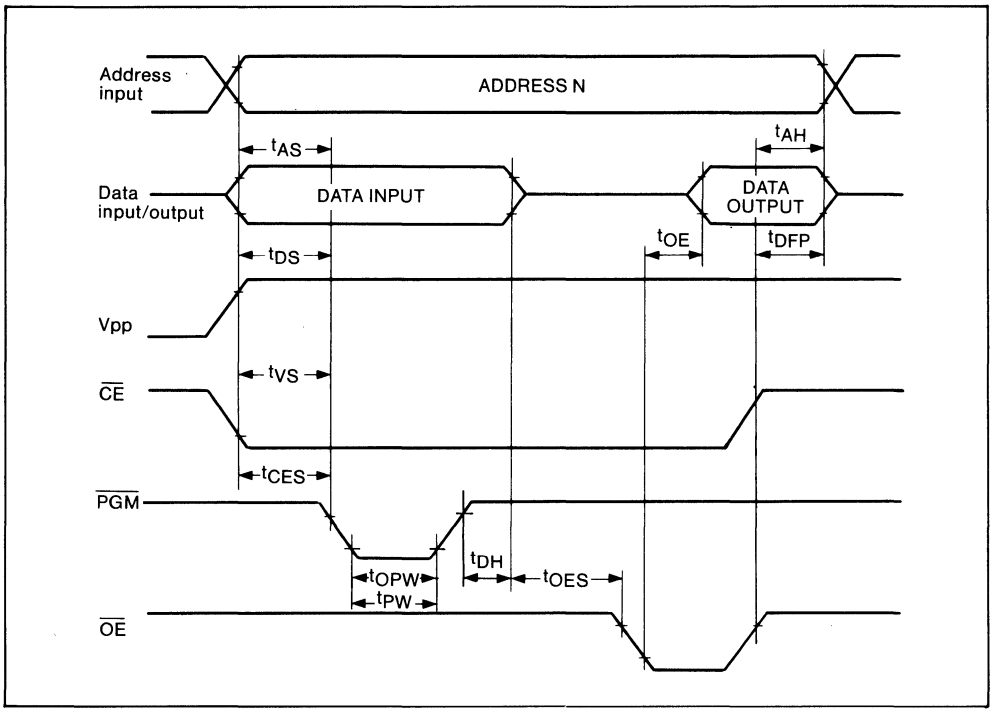
AC CHARACTERISTICS

(V_{CC} = 6V±0.25V, Vpp = 21V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Initial Program Pulse Width	t_{PW}	–	0.95	1.0	1.05	ms
$\overline{PGM}$ Overprogram Pulse Width	t_{OPW}	–	3.8	–	63	ms
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

9

TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF

MSM27128AS

16384 × 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

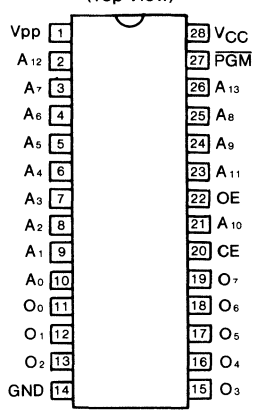
The MSM27128 is a 16834 words × 8 bit ultraviolet erasable and electrically programmable read-only memory. Users can freely prepare the memory content, which can be easily changed, so the MSM27128 is ideal for microprocessor programs, etc. The MSM27128 is manufactured by the N channel double silicon gate MOS technology and is contained in the 28 pin package.

FEATURES

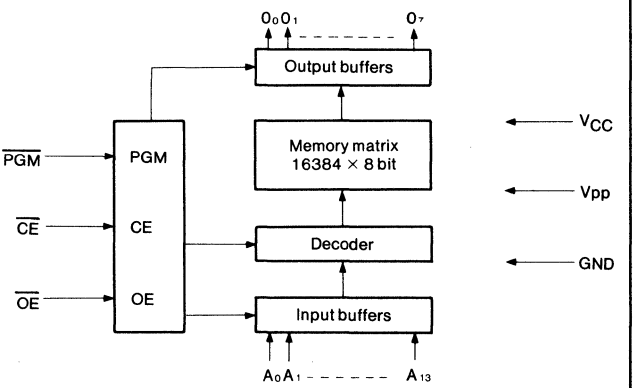
- +5V single power supply
- 13834 words × 8 bit configuration
- Access time:
  MAX200 ns (MSM27128-20)
  MAX250 ns (MSM27128-25)
  MAX300 ns (MSM27128-30)
- Power consumption:
  MAX525 mW (during operation)
  MAX184 mW (during stand-by)
- Perfect static operation
- INPUT/OUTPUT TTL level
  (three state output)

PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	Vpp (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	–	+5V	+5V	High impedance
Program	V_{IL}	–	V_{IL}	+21V	+6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+21V	+6V	Dout
Program Inhibit	V_{IH}	–	–	+21V	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	−10°C ~ 80°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	−0.6V ~ 13.5V
V_{CC} Supply Voltage	V_{CC}	−0.3V ~ 7V
Program Voltage	Vpp	−0.6V ~ 23V
Power Assembly Voltage	P_D	1.5W

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±5% Vpp=V_{CC}±0.6V	V
Vpp Voltage	Vpp	4.75	5.0	5.25			V
"H" Level Input Voltage	V_{IH}	2.00	–	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}±0.6V, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC_1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC_2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Program Power Current	I_{PP_1}	Vpp = V_{CC}±0.6V	–	–	5	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

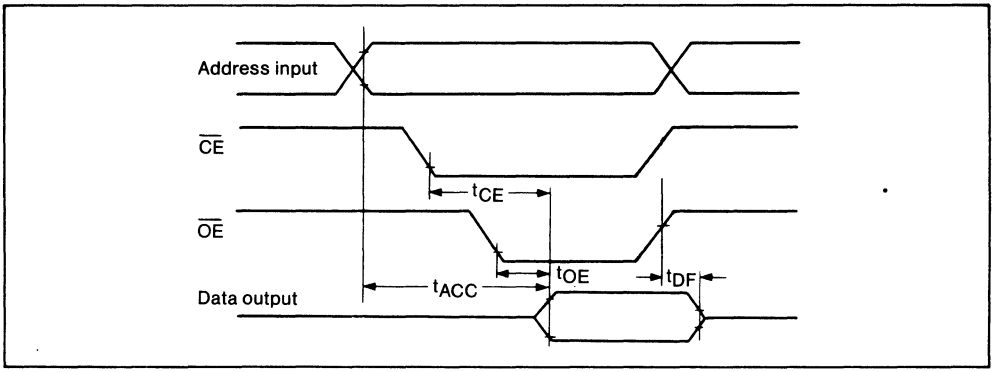
(V_{CC} = 5V±5%, Vpp = V_{CC}±0.6V, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	27128-20		27128-25		27128-30		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, PGM = V_{IH}	–	200	–	250	–	300	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	200	–	250	–	300	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	75	–	100	–	120	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	60	0	60	0	105	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

TIME CHART


Address input
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{OE}
t_{DF}
t_{ACC}
Data output

DC CHARACTERISTICS

(V_{CC} = 6V±0.25V, Vpp = 21V±0.5V, Ta = 25°C±5°C)

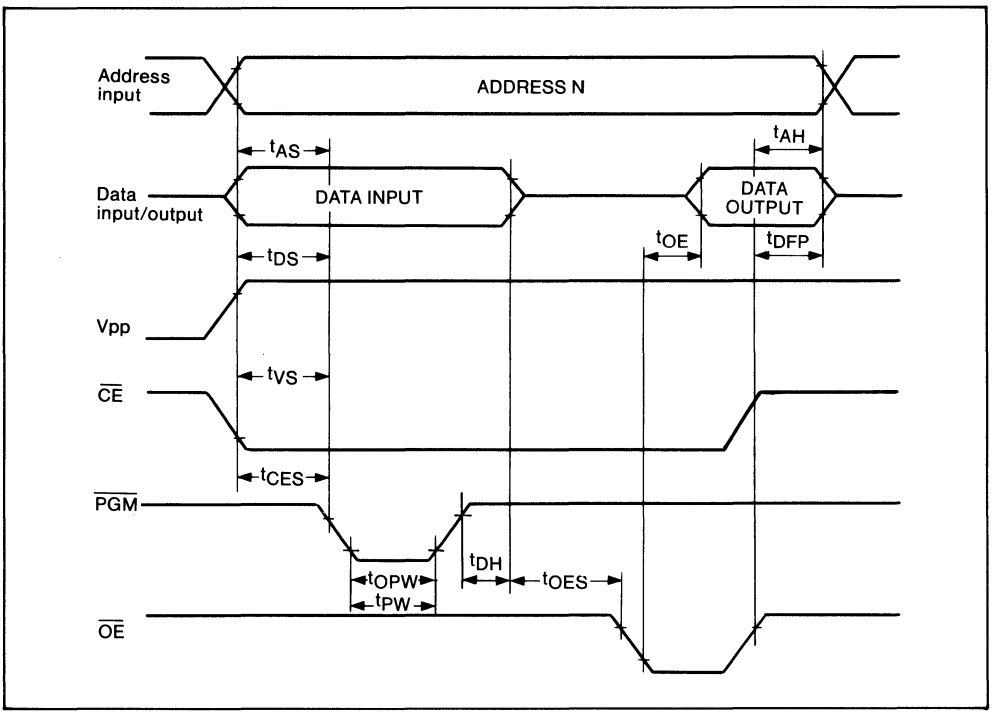
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	Ipp	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	30	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 6V±0.25V, Vpp = 21V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
OE Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Initial Program Pulse Width	t_{PW}	–	0.95	1.0	1.05	ms
$\overline{PGM}$ Overprogram Pulse Width	t_{OPW}	–	3.8	–	63	ms
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF

MSM27256AS

32768 × 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

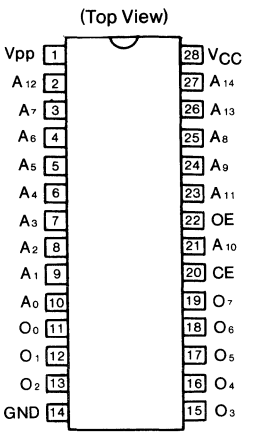
GENERAL DESCRIPTION

The MSM27256 is a 32768 words × 8 bit ultraviolet erasable and electrically programmable read-only memory. Users can freely prepare the memory content, which can be easily changed, so the MSM27256 is ideal for microprocessor programs, etc. The MSM27256 is manufactured by the N channel double silicon gate MOS technology and is contained in the 28 pin package.

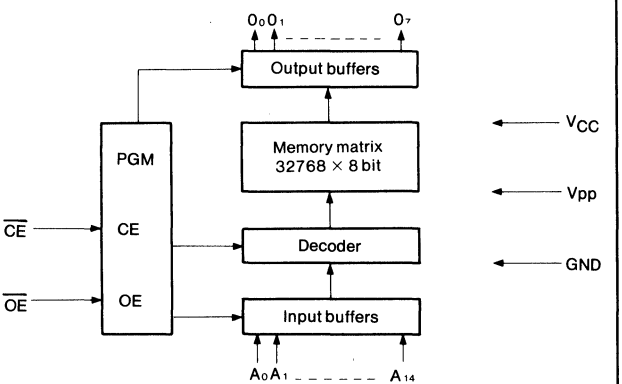
FEATURES

- +5V single power supply
- 32768 words × 8 bit configuration
- Access time:
  MAX150 ns (MSM27256-15)
  MAX200 ns (MSM27256-20)
  MAX250 ns (MSM27256-25)
- Power consumption:
  MAX525 mW (during operation)
  MAX184 mW (during stand-by)
- Perfect static operation
- INPUT/OUTPUT TTL level
  (three state output)

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	Vpp (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	+12.5V	+6V	D_{IN}
Program Verify	V_{IH}	V_{IL}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	V_{IH}	+12.5V	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	−10°C ~ 80°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	−0.6V ~ 13.5V
V_{CC} Supply Voltage	V_{CC}	−0.3V ~ 7V
Program Voltage	Vpp	−0.6V ~ 13.5V
Power Assembly Voltage	P_D	1.5W

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±5% Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.75	5.0	5.25			V
"H" Level Input Voltage	V_{IH}	2.00	–	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Program Power Current	I_{PP1}	Vpp = V_{CC}	–	–	5	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	27256-15		27256-20		27256-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	150	–	200	–	250	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}	–	150	–	200	–	250	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}	–	70	–	75	–	100	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}	0	50	0	55	0	60	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

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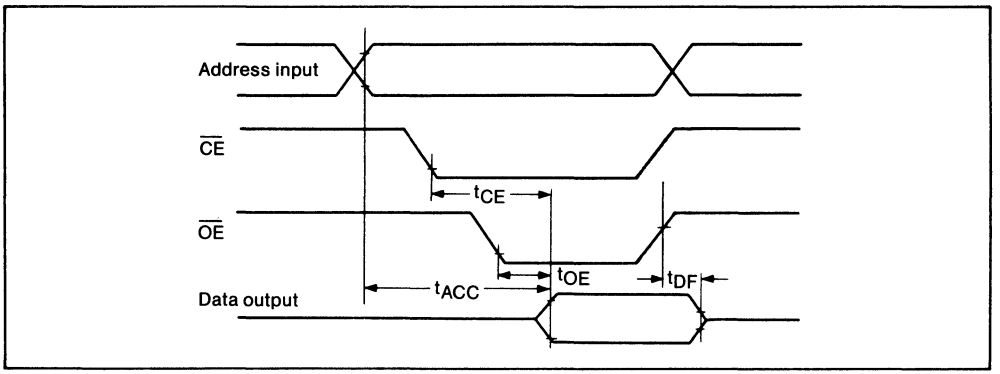
TIME CHART


Address input
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{OE}
t_{DF}
t_{ACC}
Data output

DC CHARACTERISTICS

(V_{CC} = 6V±0.25V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

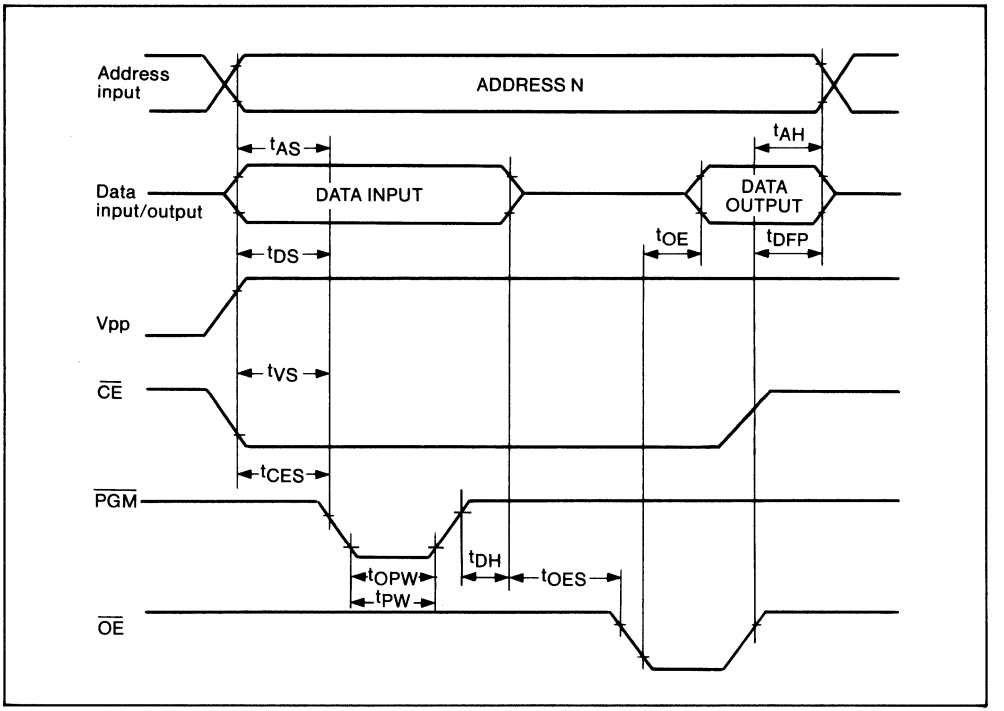
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	Ipp	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 6V±0.25V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{CE}$ Initial Program Pulse Width	t_{PW}	–	0.95	1.0	1.05	ms
$\overline{CE}$ Overprogram Pulse Width	t_{OPW}	–	2.85	–	78.75	ms
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF

9

Preliminary

MSM27512AS

65536 × 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

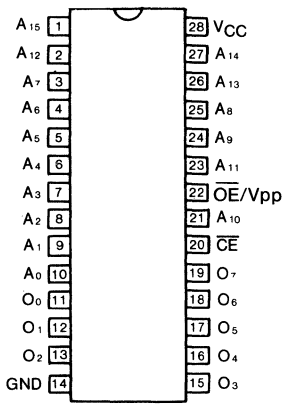
The MSM27512 is a 65536 words × 8 bit ultraviolet erasable and electrically programmable read-only memory. Users can freely prepare the memory content, which can be easily changed, so the MSM27512 is ideal for microprocessor programs, etc. The MSM27512 is manufactured by the N channel double silicon gate MOS technology and is contained in the 28 pin package.

FEATURES

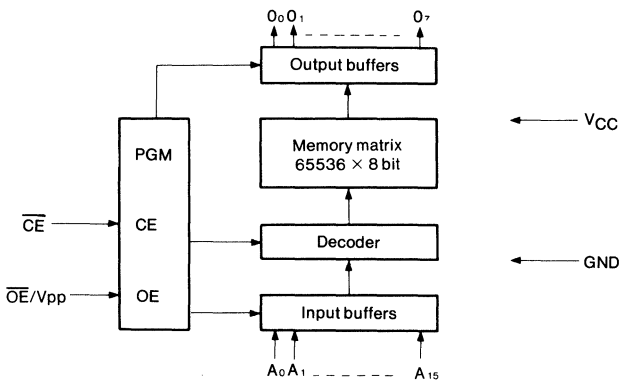
- +5V single power supply
- 65536 words × 8 bit configuration
- Access time:
  - MAX150 ns (MSM27512-15)
  - MAX200 ns (MSM27512-20)
  - MAX250 ns (MSM27512-25)
- Power consumption:
  - MAX525 mW (during operation)
  - MAX184 mW (during stand-by)
- Perfect static operation
- INPUT/OUTPUT TTL level (three state output)

PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

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FUNCTION TABLE

Pins / Mode	$\overline{CE}$ (20)	$\overline{OE}$/Vpp (22)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	+5V	Dout
Output Disable	V_{IL}	V_{IH}	+5V	High impedance
Stand-by	V_{IH}	–	+5V	High impedance
Program	V_{IL}	Vpp	+6V	D_{IN}
Program Inhibit	V_{IH}	Vpp	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	–10°C ~ 80°C
Storage Temperature	Tstg	–55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	–0.6V ~ 13.5V
V_{CC} Supply Voltage	V_{CC}	–0.3V ~ 7V
Program Voltage	Vpp	–0.6V ~ 13.5V
Power Assembly Voltage	P_D	1.5W

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±5%	V
"H" Level Input Voltage	V_{IH}	2.00	–	6.25			V
"L" Level Input Voltage	V_{IL}	–0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	–0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = –400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

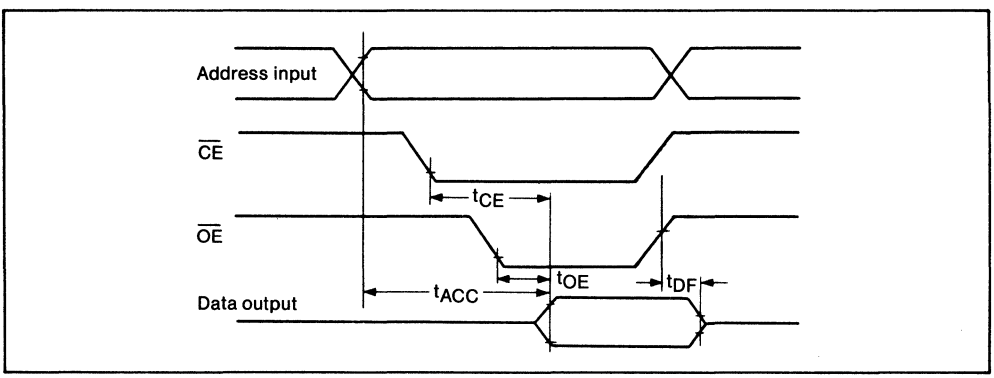
Parameter	Symbol	Conditions	27512-15		27512-20		27512-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$/Vpp = V_{IL}	–	150	–	200	–	250	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$/Vpp = V_{IL}	–	150	–	200	–	250	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}	–	70	–	75	–	100	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}	0	50	0	55	0	60	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

9

TIME CHART



DC CHARACTERISTICS

(V_{CC} = 6V±5%, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

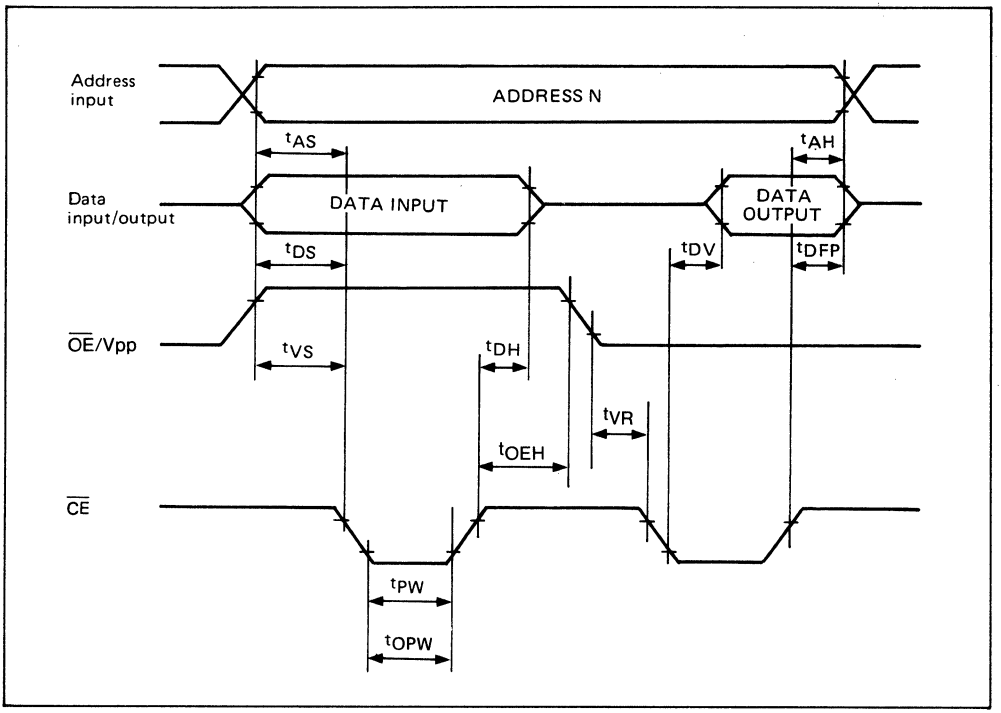
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	Ipp	$\overline{CE}$ = V_{IL}	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 6V±0.25V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
$\overline{CE}$ Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{CE}$ Initial Program Pulse Width	t_{PW}	–	0.95	1.0	1.05	ms
$\overline{CE}$ Overprogram Pulse Width	t_{OPW}	–	2.85	–	78.75	ms
$\overline{OE}$/Vpp Hold Time	t_{OEH}	–	2	–	–	μs
Data Valid from $\overline{CE}$	t_{DV}	–	–	–	1	μs
$\overline{OE}$/Vpp Recovery Time	t_{VR}	–	2	–	–	μs

TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF

9

Preliminary

MSM271000AS

131072 × 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

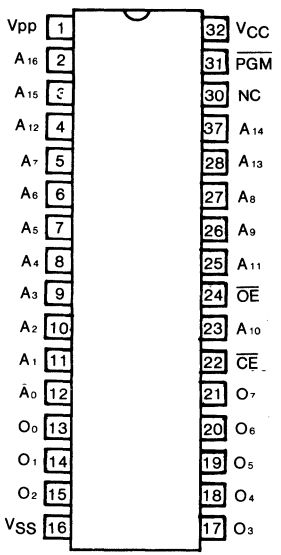
GENERAL DESCRIPTION

The MSM271000 is a 131072 words × 8 bit ultraviolet erasable and electrically programmable read-only memory. Users can freely prepare the memory content, which can be easily changed, so the MSM271000 is ideal for microprocessor programs, etc. The MSM271000 is manufactured by the N channel double silicon gate MOS technology and is contained in the 32 pin package.

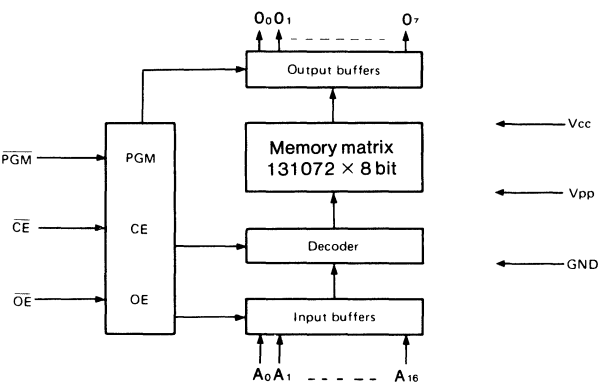
FEATURES

- +5V single power supply
- 131072 words × 8 bit configuration
- Access time:
  MAX120 ns (MSM271000-12)
  MAX150 ns (MSM271000-15)
  MAX200 ns (MSM271000-20)
- Power consumption:
  MAX525 mW (during operation)
  MAX184 mW (during stand-by)
- Perfect static operation
- INPUT/OUTPUT TTL level (three state output)

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

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FUNCTION TABLE

Pins / Mode	CE (22)	OE (24)	PGM (31)	Vpp (1)	V_{CC} (32)	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	–	+5V	+5V	High impedance
Program	V_{IL}	–	V_{IL}	+12.5V	+6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	–	–	+12.5V	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	–10°C ~ 80°C
Storage Temperature	Tstg	–55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	–0.6V ~ 13V
V_{CC} Supply Voltage	V_{CC}	–0.3V ~ 7V
Program Voltage	Vpp	–0.6V ~ 13.5V
Power Assembly Voltage	P_D	1.5W

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±0.25V Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.75	5.0	5.25			V
"H" Level Input Voltage	V_{IH}	2.00	–	6.25			V
"L" Level Input Voltage	V_{IL}	–0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC_1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC_2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Program Power Current	I_{PP_1}	Vpp = V_{CC}	–	–	5	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

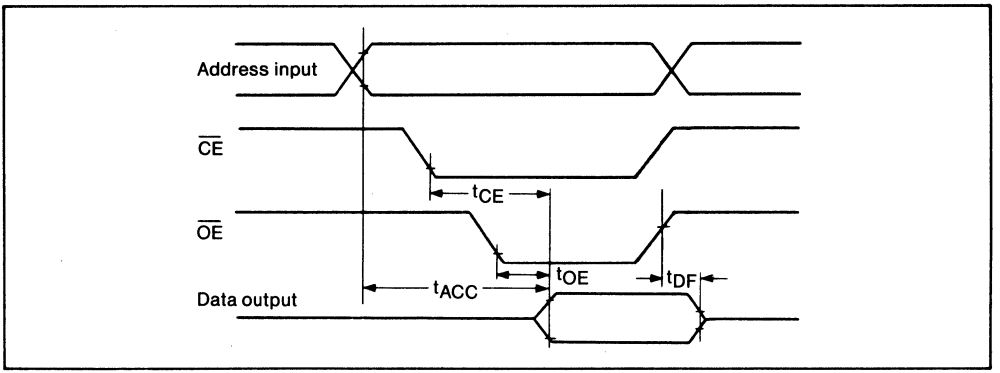
(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	271000-12		271000-15		271000-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	120	–	150	–	200	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	120	–	150	–	200	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	50	–	60	–	75	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	40	0	50	0	55	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

TIME CHART


Address input
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{OE}
t_{DF}
t_{ACC}
Data output

<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 6V±0.25V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

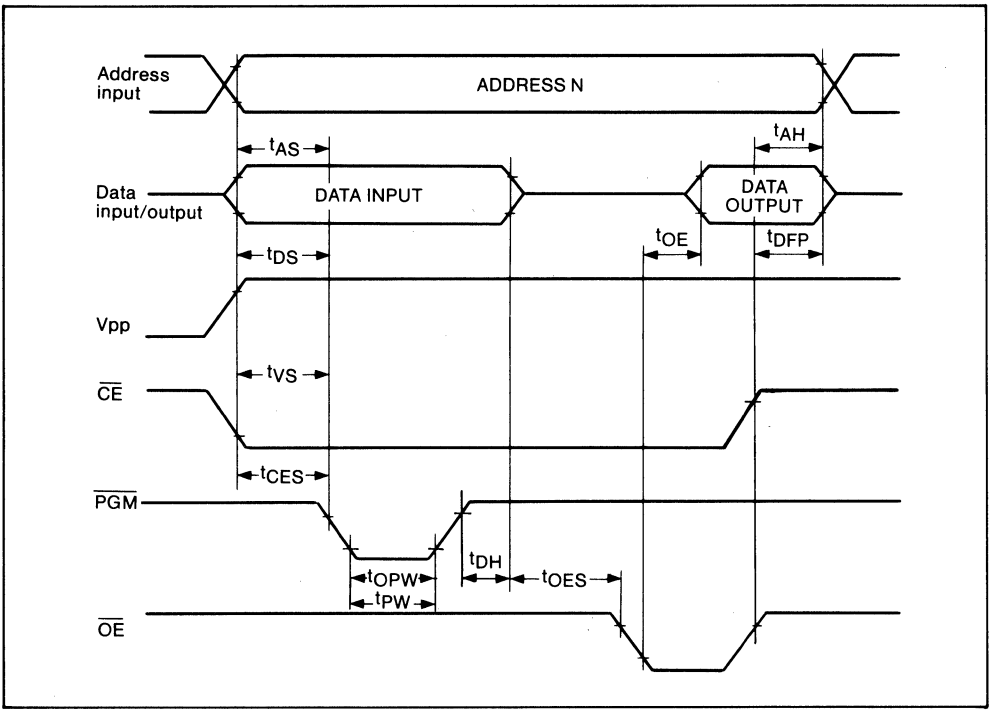
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	Ipp	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 6V±0.25V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Initial Program Pulse Width	t_{PW}	–	0.95	1.0	1.05	ms
$\overline{PGM}$ Overprogram Pulse Width	t_{OPW}	–	2.85	–	78.75	ms
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF

9

MSM271024AS

65536 × 16 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

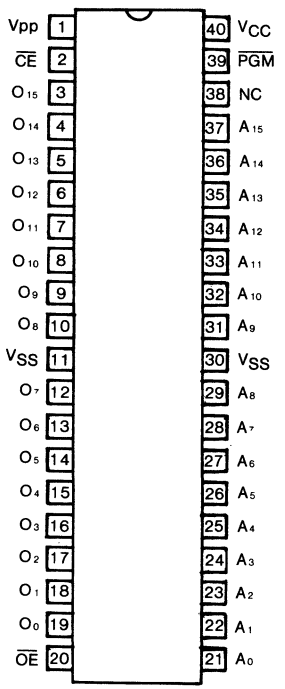
GENERAL DESCRIPTION

The MSM271024 is a 65536 words × 16 bit ultraviolet erasable and electrically programmable read-only memory. Users can freely prepare the memory content, which can be easily changed, so the MSM271024 is ideal for microprocessor programs, etc. The MSM271024 is manufactured by the N channel double silicon gate MOS technology and is contained in the 40 pin package.

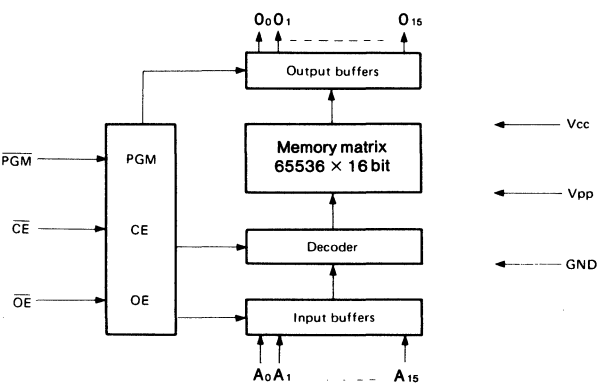
FEATURES

- +5V single power supply
- 65536 words × 16 bit configuration
- Access time:
  MAX120 ns (MSM271024-12)
  MAX150 ns (MSM271024-15)
  MAX200 ns (MSM271024-20)
- Power consumption:
  MAX525 mW (during operation)
  MAX184 mW (during stand-by)
- Perfect static operation
- INPUT/OUTPUT TTL level (three state output)

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (2)	$\overline{OE}$ (20)	$\overline{PGM}$ (39)	Vpp (1)	V_{CC} (40)	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	–	+5V	+5V	High impedance
Program	V_{IL}	–	V_{IL}	+12.5V	+6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	–	–	+12.5V	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	–10°C ~ 80°C
Storage Temperature	Tstg	–55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	–0.6V ~ 13V
V_{CC} Supply Voltage	V_{CC}	–0.3V ~ 7V
Program Voltage	Vpp	–0.6V ~ 13.5V
Power Assembly Voltage	P_D	1.5W

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±0.25V Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.75	5.0	5.25			V
"H" Level Input Voltage	V_{IH}	2.00	–	6.25			V
"L" Level Input Voltage	V_{IL}	–0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE} = V_{IH}$	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE} = V_{IL}$	–	–	100	mA
Program Power Current	I_{PP1}	Vpp = V_{CC}	–	–	5	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

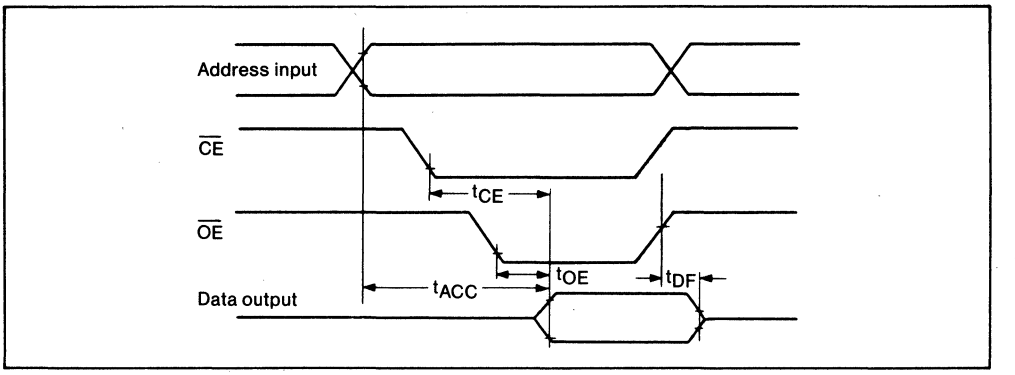
Parameter	Symbol	Conditions	271024-12		271024-15		271024-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	–	120	–	150	–	200	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	–	120	–	150	–	200	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	–	50	–	60	–	75	ns
Output Disable Time	t_{DF}	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	40	0	50	0	55	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

9

TIME CHART


Address input
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{OE}
t_{DF}
t_{ACC}
Data output

<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 6V±0.25V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

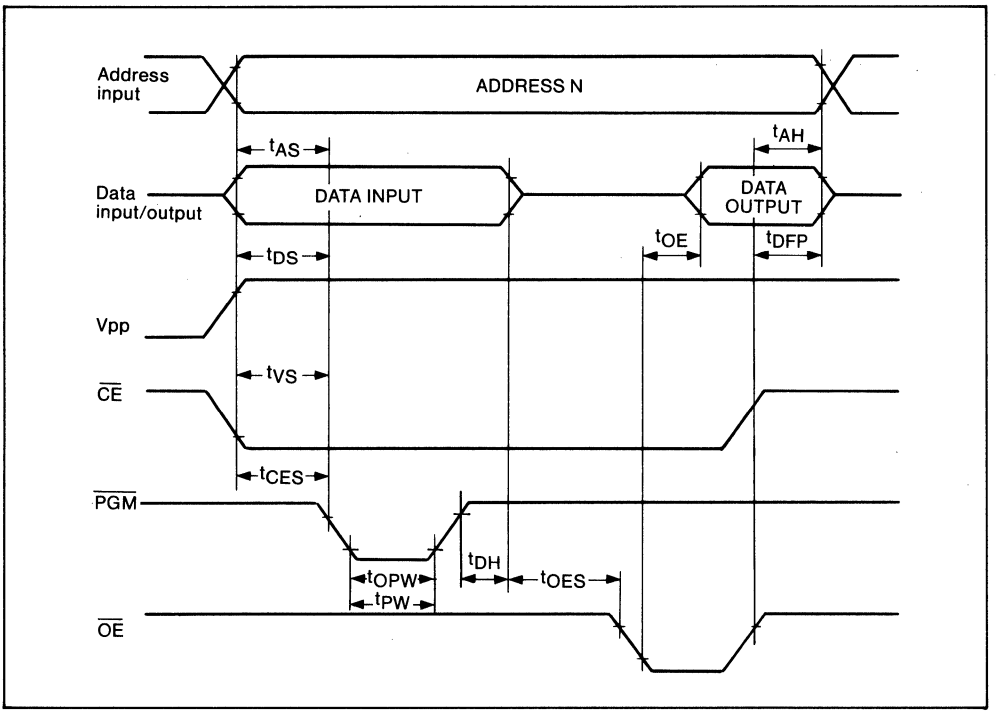
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	Ipp	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 6V±0.25V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Initial Program Pulse Width	t_{PW}	–	0.95	1.0	1.05	ms
$\overline{PGM}$ Overprogram Pulse Width	t_{OPW}	–	2.85	–	78.75	ms
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from OE	t_{OE}	–	–	–	150	ns

TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF

9

Preliminary

MSM27C64AS

8192 × 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

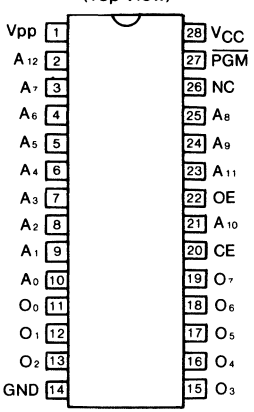
The MSM27C64 is a 8192 words × 8 bit ultraviolet erasable and electrically programmable read-only memory. Users can freely prepare the memory content, which can be easily changed, so the MSM27C64 is ideal for microprocessor programs, etc. The MSM27C64 is manufactured by the CMOS double silicon gate technology and is contained in the 28 pin package.

FEATURES

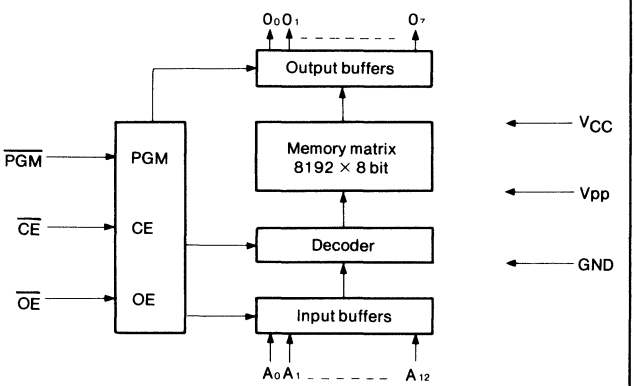
- +5V single power supply
- 8192 words × 8 bit configuration
- Access time:
  MAX200 ns (MSM27C64-20)
  MAX250 ns (MSM27C64-25)
  MAX300 ns (MSM27C64-30)
- Power consumption:
  MAX165 mW (during operation)
  MAX0.55 mW (during stand-by)
- Perfect static operation
- INPUT/OUTPUT TTL level
  (three state output)

PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

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FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	Vpp (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	–	+5V	+5V	High impedance
Program	V_{IL}	–	V_{IL}	+21V	+6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+21V	+6V	Dout
Program Inhibit	V_{IH}	–	–	+21V	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	–10°C ~ 80°C
Storage Temperature	Tstg	–55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	V_{IN} = –0.6V ~ 13.5V, V_{OUT} = –0.3V ~ V_{CC} + 1V
V_{CC} Supply Voltage	V_{CC}	–0.3V ~ 7V
Program Voltage	Vpp	–0.6V ~ 23V
Power Assembly Voltage	P_D	1.5W

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.5	5.0	5.5	0°C ~ 70°C	V_{CC}=5V±10% Vpp=V_{CC}±0.7V	V
Vpp Voltage	Vpp	3.8	5.0	6.2			V
"H" Level Input Voltage	V_{IH}	2.00	–	6.5			V
"L" Level Input Voltage	V_{IL}	–0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±10%, Vpp = V_{CC}±0.7V, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.5V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.5V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC_1}	$\overline{CE}$ = V_{IH} = V_{CC}	–	–	100	μA
V_{CC} Power Current (Operation)	I_{CC_2}	$\overline{CE}$ = V_{IL}	–	–	30	mA
Vpp Power Current	I_{PP_1}	Vpp = V_{CC}±0.7V	–	–	100	μA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	4.0	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5V±10%, Vpp = V_{CC}±0.7V, Ta = 0°C ~ 70°C)

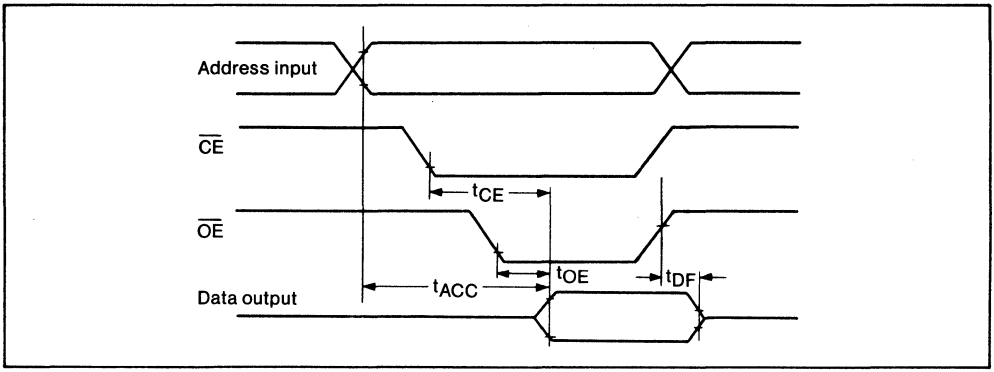
Parameter	Symbol	Conditions	27C64-20		27C64-25		27C64-30		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	200	–	250	–	300	ns
CE Access Time	t_{CE}	$\overline{OE}$ = V_{IL}, PGM = V_{IH}	–	200	–	250	–	300	ns
OE Access Time	t_{OE}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	75	–	100	–	120	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	60	0	85	0	105	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

9

TIME CHART


Address input
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{OE}
t_{DF}
t_{ACC}
Data output

DC CHARACTERISTICS

(V_{CC} = 6V±0.25V, Vpp = 21V±0.5V, Ta = 25°C±5°C)

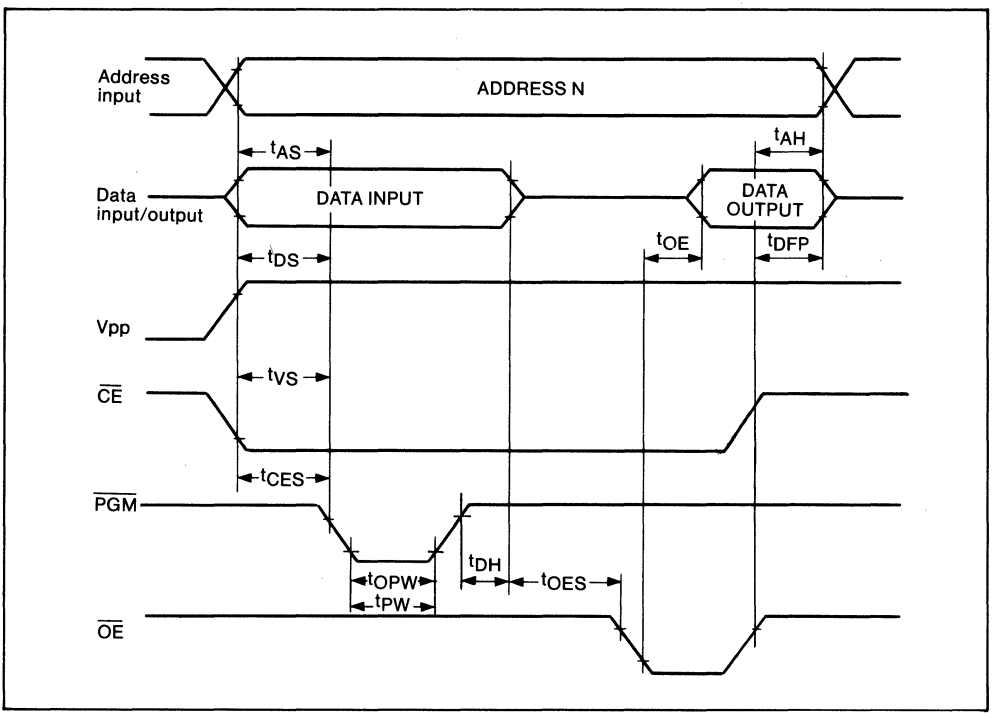
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.5V	–	–	10	μA
Vpp Power Current	Ipp	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	30	mA
V_{CC} Power Current	I_{CC}	–	–	–	30	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 6V±0.25V, Vpp = 21V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Initial Program Pulse Width	t_{PW}	–	0.95	1.0	1.05	ms
$\overline{PGM}$ Overprogram Pulse Width	t_{OPW}	–	3.8	–	63	ms
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from OE	t_{OE}	–	–	–	150	ns

TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF

9

Preliminary

MSM27C128AS

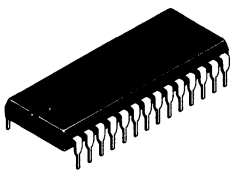
16384 × 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

The MSM27C128 is a 16384 words × 8 bit ultraviolet erasable and electrically programmable read-only memory. Users can freely prepare the memory content, which can be easily changed, so the MSM27C128 is ideal for microprocessor programs, etc. The MSM27C128 is manufactured by the CMOS double silicon gate technology and is contained in the 28 pin package.

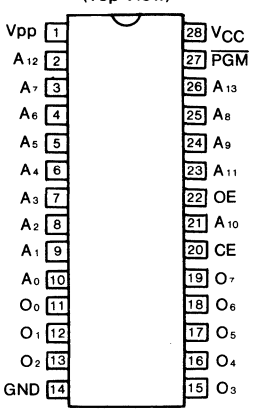
FEATURES

- +5V single power supply
- 16384 words × 8 bit configuration
- Access time:
  MAX200 ns (MSM27C128-20)
  MAX250 ns (MSM27C128-25)
  MAX300 ns (MSM27C128-30)
- Power consumption:
  MAX165 mW (during operation)
  MAX0.55 mW (during stand-by)
- Perfect static operation
- INPUT/OUTPUT TTL level
  (three state output)

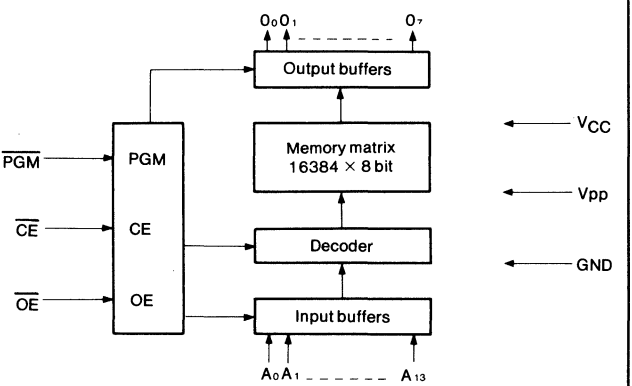


PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

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FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	Vpp (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	–	+5V	+5V	High impedance
Program	V_{IL}	–	V_{IL}	+21V	+6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+21V	+6V	Dout
Program Inhibit	V_{IH}	–	–	+21V	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	−10°C ~ 80°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	V_{IN} = −0.6V ~ 13.5V, V_{OUT} = −0.3V ~ V_{CC} + 1V
V_{CC} Supply Voltage	V_{CC}	−0.3V ~ 7V
Program Voltage	Vpp	−0.6V ~ 23V
Power Assembly Voltage	P_D	1.5W

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.5	5.0	5.5	0°C ~ 70°C	V_{CC}=5V±10% Vpp=V_{CC}±0.7V	V
Vpp Voltage	Vpp	3.8	5.0	6.2			V
"H" Level Input Voltage	V_{IH}	2.00	–	6.5			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±10%, Vpp = V_{CC}±0.7V, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.5V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.5V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC_1}	$\overline{CE}$ = V_{IH} = V_{CC}	–	–	100	μA
V_{CC} Power Current (Operation)	I_{CC_2}	$\overline{CE}$ = V_{IL}	–	–	30	mA
Vpp Power Current	I_{PP_1}	Vpp = V_{CC}±0.7V	–	–	100	μA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	4.0	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5V±10%, Vpp = V_{CC}±0.7V, Ta = 0°C ~ 70°C)

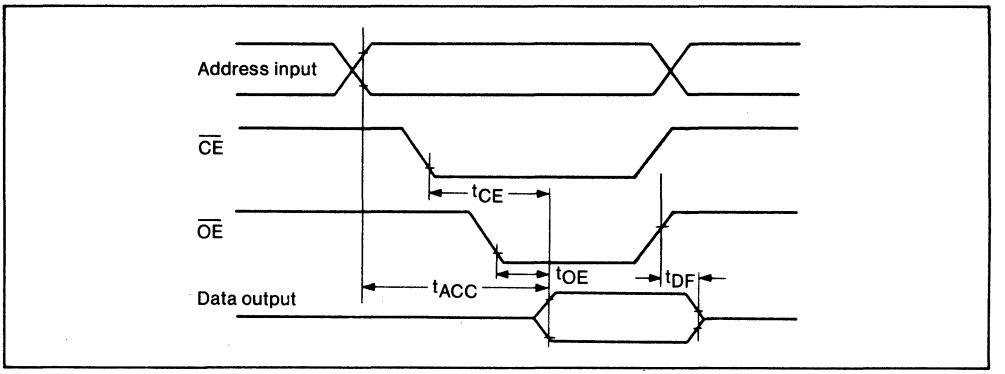
Parameter	Symbol	Conditions	27C128-20		27C128-25		27C128-30		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	200	–	250	–	300	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	200	–	250	–	300	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	75	–	100	–	120	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	60	0	85	0	105	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

9

TIME CHART


Address input
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{OE}
t_{DF}
t_{ACC}
Data output

DC CHARACTERISTICS

(V_{CC} = 6V±0.25V, Vpp = 21V±0.5V, Ta = 25°C±5°C)

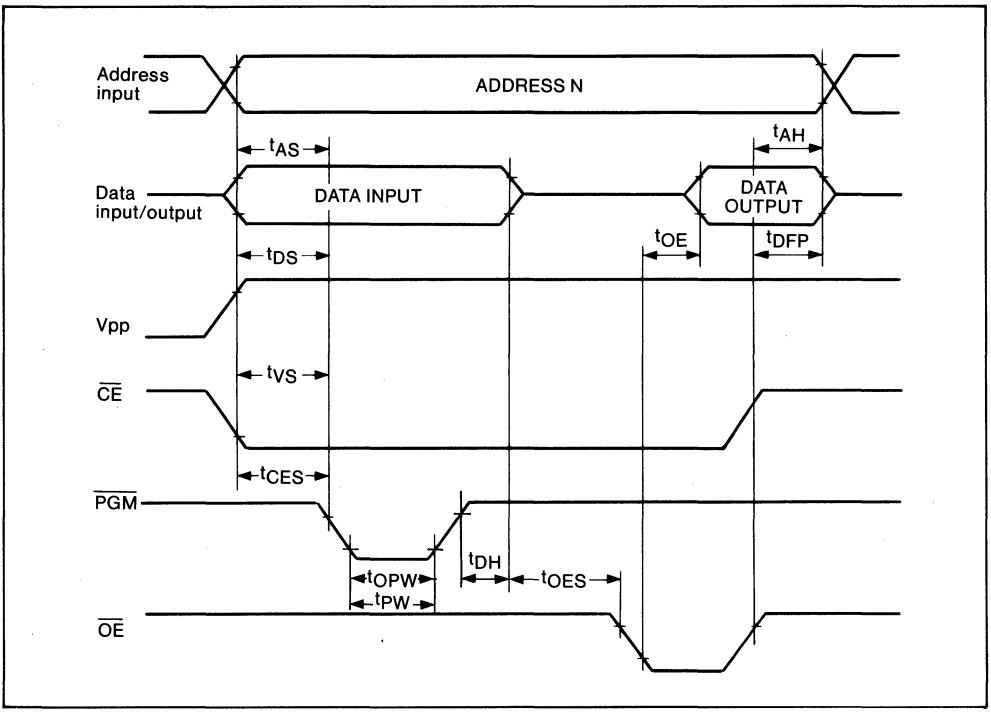
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.5V	–	–	10	μA
Vpp Power Current	Ipp	CE = PGM = V_{IL}	–	–	30	mA
V_{CC} Power Current	I_{CC}	–	–	–	30	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 6V±0.25V, Vpp = 21V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Initial Program Pulse Width	t_{PW}	–	0.95	1.0	1.05	ms
$\overline{PGM}$ Overprogram Pulse Width	t_{OPW}	–	3.8	–	63	ms
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF

9

Preliminary

MSM27C1024AS

65536 × 16 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

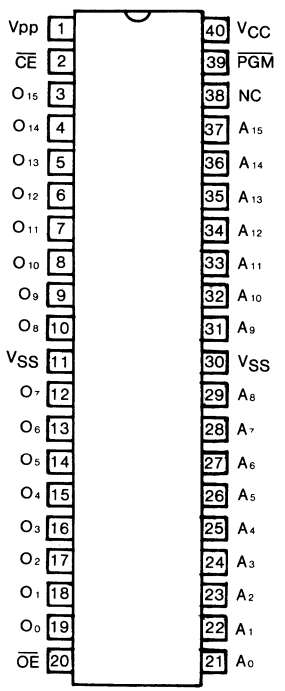
GENERAL DESCRIPTION

The MSM27C1024 is a 65536 words × 16 bit ultraviolet erasable and electrically programmable read-only memory. Users can freely prepare the memory content, which can be easily changed, so the MSM27C1024 is ideal for microprocessor programs, etc. The MSM27C1024 is manufactured by the CMOS double silicon gate technology and is contained in the 40 pin package.

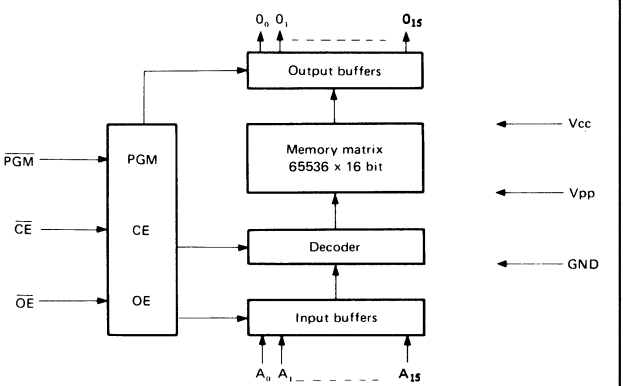
FEATURES

- +5V single power supply
- 65536 words × 16 bit configuration
- Access time:
  - MAX100 ns (MSM27C1024-10)
  - MAX150 ns (MSM27C1024-15)
  - MAX200 ns (MSM27C1024-20)
- Power consumption:
  - MAX175 mW (during operation)
  - MAX0.55 mW (during stand-by)
- Perfect static operation
- INPUT/OUTPUT TTL level (three state output)

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

9

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (2)	$\overline{OE}$ (20)	$\overline{PGM}$ (39)	Vpp (1)	V_{CC} (40)	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	–	+5V	+5V	High impedance
Program	V_{IL}	–	V_{IL}	+12.5V	+6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	–	–	+12.5V	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	−10°C ~ 80°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	V_{IN} = −0.6V ~ 13V, V_{OUT} = −0.3V ~ V_{CC} + 1V
V_{CC} Supply Voltage	V_{CC}	−0.3V ~ 7V
Program Voltage	Vpp	−0.6V ~ 13.5V
Power Assembly Voltage	P_D	1.5W

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.5	5.0	5.5	0°C ~ 70°C	V_{CC}=5V±0.5V Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.5	5.0	5.5			V
"H" Level Input Voltage	V_{IH}	2.00	–	6.5			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±10%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE}$ = V_{IH} = V_{CC}	–	–	50	μ
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	–	30	mA
Program Power Current	I_{PP1}	Vpp = V_{CC}	–	–	50	μ
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5V±10%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

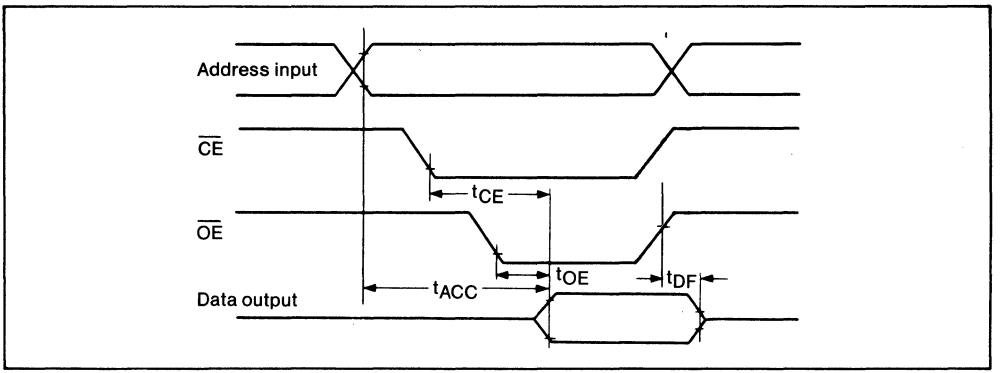
Parameter	Symbol	Conditions	27C1000-10		27C1000-15		27C1000-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	100	–	150	–	200	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	100	–	150	–	200	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	45	–	60	–	75	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	35	0	50	0	55	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

9

TIME CHART


Address input
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{OE}
t_{DF}
t_{ACC}
Data output

DC CHARACTERISTICS

(V_{CC} = 6V±0.25V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

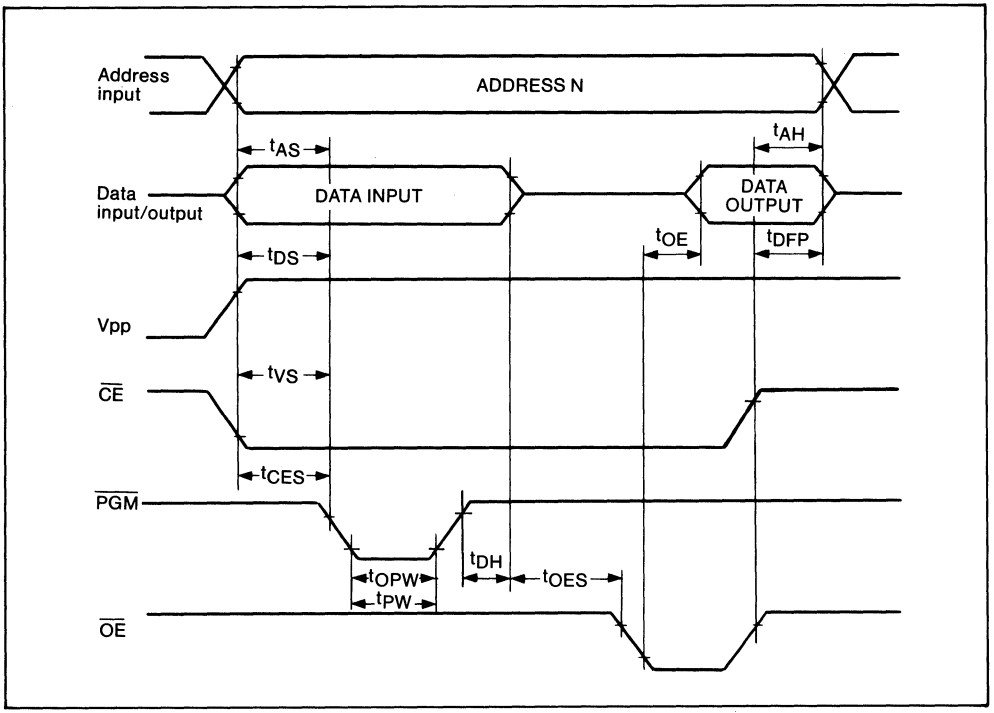
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	Ipp	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	30	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 6V±0.25V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Initial Program Pulse Width	t_{PW}	–	0.95	1.0	1.05	ms
$\overline{PGM}$ Overprogram Pulse Width	t_{OPW}	–	2.85	–	78.75	ms
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from OE	t_{OE}	–	–	–	150	ns

TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF

9

MOS E^2 ROMS

9

MSM2816ARS

2K x 8 BIT ELECTRICALLY ERASABLE PROM

GENERAL DESCRIPTION

The MSM2816A is a 2,048 word x 8 bit electrically erasable programmable read-only memory (E^2 PROM). The MSM2816A operates from a single 5V power supply, has a static standby mode, and features easiest programming. Though the MSM2816A requires no high voltage during reading or writing, it is still operable in the high-voltage mode as well.

The process of updating byte data in the 5V programming mode is initiated by setting the write signal at the TTL low (L) level for 200 ns. Address and data bus information is latched within the IC, and the system is made available to other tasks during the write cycle.

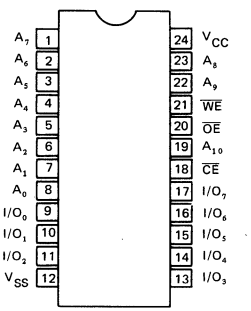
The MSM2816A erases a selected byte automatically before writing new information to it. The erase/write cycle completes within a maximum period of 10 ms. In addition to the byte erase/write function, the MSM2816A supports a mode permitting the entire chip to be cleared at 10 ms or less.

The MSM2816A is ideally suited for applications involving the use of a nonvolatile memory to make modifications to a system. Typical applications include self-controllable equipments, memorizing ratio of tariffs at terminals on the sales counter, storing keywords for encoding data, programmable character generators, and storing map information in air navigation systems.

FEATURES

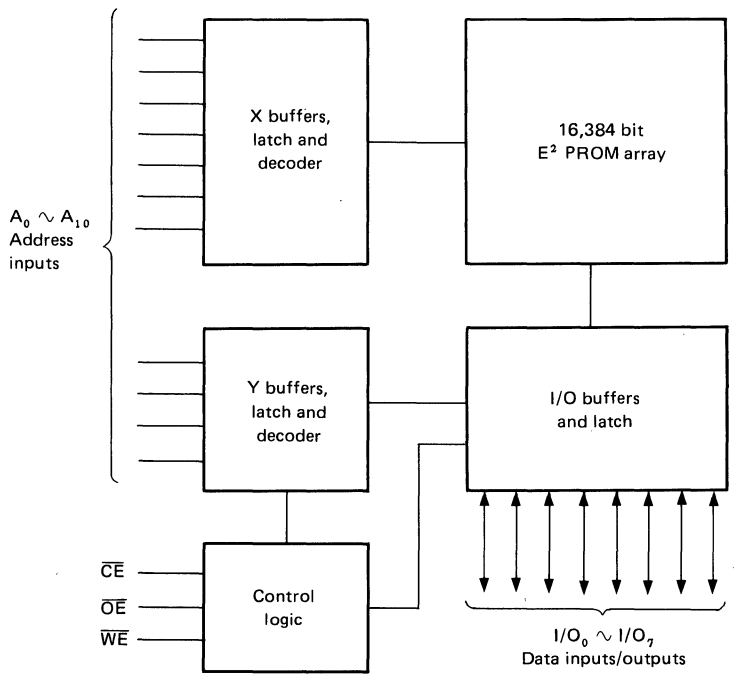
- Single 5V power supply
- High-speed access time . . . . . 250 ns MAX.
  300 ns MAX.
  350 ns MAX.
  450 ns MAX.
- TTL level byte write . . . . . 10 ms MAX.
- Internally latched address data during write
- Automatic erase before write
- Automatic completion of write
- Inadvertent write protection
- Input and output TTL compatible
- JEDEC-compliance pin configuration
- Pin compatible to Xicor 2816A, Intel 2816/2816A

PIN CONFIGURATION (Top View)



Pin names	Function
$A_0 \sim A_{10}$	Address inputs
$I/O_0 \sim I/O_7$	Data inputs/outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	+5V
V_{SS}	Ground

FUNCTIONAL BLOCK DIAGRAM



MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power	
V_{IH}	X	X	Standby	High Z	Standby	
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active	
V_{IL}	V_{IH}	⊓	5V byte write	D_{IN}	Active	
V_{IL}	V_{IH}	V_{IH}	Program (READ AND WRITE) inhibit	High Z	Active	
V_{IL}	V_{IH}	V_{PP}	Byte erase	$D_{IN}=V_{IH}$	Active	High-voltage programming mode
V_{IL}	V_{IH}	V_{PP}	Byte write	D_{IN}	Active	
V_{IL}	V_{OE}	V_{PP}	Chip erase	$D_{IN}=V_{IH}$	Active	

Note: X; Don't care (V_{IH} or V_{IL})

DEVICE OPERATION

Read Mode

Data in the MSM2816A can be read by applying a TTL high signal to $\overline{WE}$, and a low signal to $\overline{CE}$ and $\overline{OE}$. The data for t_{AA} time from address inputs, for t_{CE} time from a low on $\overline{OE}$, and for t_{OE} from a low on $\overline{OE}$, whichever occurs last, is valid. Once a TTL high signal is applied to $\overline{OE}$ or $\overline{CE}$, the I/O pins are in a high impedance state to prevent data bus contention within the system.

Write Mode

The MSM2816A has two write modes:

- 5V programming mode (standard)

  In this mode, a write cycle is initiated by applying a TTL low signal to $\overline{WE}$ and $\overline{CE}$ and a high signal to $\overline{OE}$. Address inputs are latched on the trailing edge of $\overline{WE}$ or $\overline{CE}$ whichever is the slower. Data on the I/O pins is latched on the leading edge of $\overline{WE}$ or $\overline{CE}$. The address and data are latched for 200 ns by using TTL level write signal. Once the data is latched, the MSM2816A erases the byte that is selected within 10 ms automatically and writes new data to it.

  In the meantime, the system is available to other tasks, but the I/O pins are in a high impedance state while writing is in progress. The system recognizes the completion of a write operation by comparing the data last written against previous data. When this method of verification is to be used, the output may be pulled up to V_{CC} with a resistor so that all read data prior to the completion of the write operation should be '1'.

- High-voltage programming mode

  While the MSM2816A merely requires a single 5V power supply to write, it is also operable in the high-voltage mode to remain compatible with existing E^2 PROMs. In this mode, all selected bytes must be erased before new data can be written to them. The byte erase operation can be initiated the same way as a high-voltage write operation, except that a TTL high level is applied to every I/O pin. To be able to write new data to a byte in the high-voltage mode, it is necessary to apply a TTL high level to $\overline{OE}$ and a TTL low level to $\overline{CE}$ before $\overline{WE}$ is raised to a voltage (V_{PP}) between 12V and 22V. The MSM2816A has no constrain on V_{PP} rising or falling edges, and data present on the I/O pins is written to memory within a maximum period of 9 ms from address inputs.

High-voltage Chip Erase

The data in all memory cells is erased within 9 ms when $\overline{OE}$ is initially raised to 12-22V, then $\overline{WE}$ is raised to 12-22V while applying a TTL high signal to every I/O pin. After the erasure, all data bits in the device are set to TTL high level (logic '1').

Standby Mode

The 2816A has a standby mode which reduces the active power dissipation by about 55% when a TTL high level is applied to $\overline{CE}$.

- Number of repetitive write cycles

  The MSM2816A is designed to support applications requiring up to 10,000 write cycles per byte.

- Inadvertent write protection

  The MSM2816A has following four functions to prevent inadvert write during power up, power down, and during line noise occurrence.

  (1) V_{CC} level detection

  Writing to the device is automatically inhibited when V_{CC} has fallen to 3.0V or below.

  (2) Time delay

  Any write operation is automatically inhibited while V_{CC} is 5-20 ms in the Vwl state when the MSM2816A is being powered up.

  This features allows sufficient time for the system to apply a TTL high signal to $\overline{WE}$ or $\overline{CE}$ before write occurs.

  (3) $\overline{OE}$ gating

  The MSM2816A inhibits all write operations while $\overline{OE}$ is low.

  (4) $\overline{WE}$ noise protection

  No write cycle may be initiated by write pulses for 20 ns or shorter.

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ELECTRICAL CHARACTERISTICS

- Absolute Maximum Ratings (Note 1)

Ambient temperature under bias	−10°C ∿ +85°C
Storage temperature	−65°C ∿ +125°C
Voltage on any pin with respect to ground (Note 2)	−0.5V ∿ +6V
DC output current	5 mA
$\overline{OE}$ and $\overline{WE}$ voltage in high-voltage mode	22.5V

Notes: 1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. The device incorporates a special circuit to safeguard it against electrostatic damage. For added assurance, avoid operating the device above the maximum ratings indicated.

DC OPERATING CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = 0°C ∿ 70°C)

Parameter	Symbol	Condition	Limits MIN	Limits MAX	Unit
Input low voltage	V_{IL}		–	0.8	V
Input high voltage	V_{IH}		2.0	–	V
Output low voltage	V_{OL}	I_{OL} = 2.1 mA	–	0.4	V
Output high voltage	V_{OH}	I_{OH} = –400 μA	2.4	–	V
Write inhibit V_{CC} voltage	V_{WI}		3.0	3.5	V
$\overline{WE}$ voltage (erase/write) (Note 1)	V_{PP}		12	22	V
$\overline{OE}$ voltage (chip erase) (Note 1)	V_{OE}		12	22	V
V_{PP} current (byte erase/write) (Note 1)	$I_{PP(W)}$	$\overline{CE}$ = V_{IL}	–	10	μA
V_{PP} current (inhibit) (Note 1)	$I_{PP(I)}$	V_{PP} = 22V, CE = V_{IH}	–	10	μA
V_{PP} current (chip erase) (Note 1)	$I_{PP(C)}$		–	10	μA
V_{OE} current (chip erase) (Note 1)	I_{OE}	V_{OE} = V_{PP} = 22V	–	10	μA
Input leakage current	I_{LI}	V_{IN} = 0 ∿ 5.25V	–	10	μA
Output leakage current	I_{LO}	V_{OUT} = 0 ∿ 5.25V	–	±10	μA
Operating supply current	I_{CC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} All I/O S = OPEN Other pins = 5.25V	–	110	mA
Standby supply current	I_{SB}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O S = OPEN Other pins = 5.25V	–	40	mA

Note 1: These parameters apply only in the high-voltage programming mode.

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V)

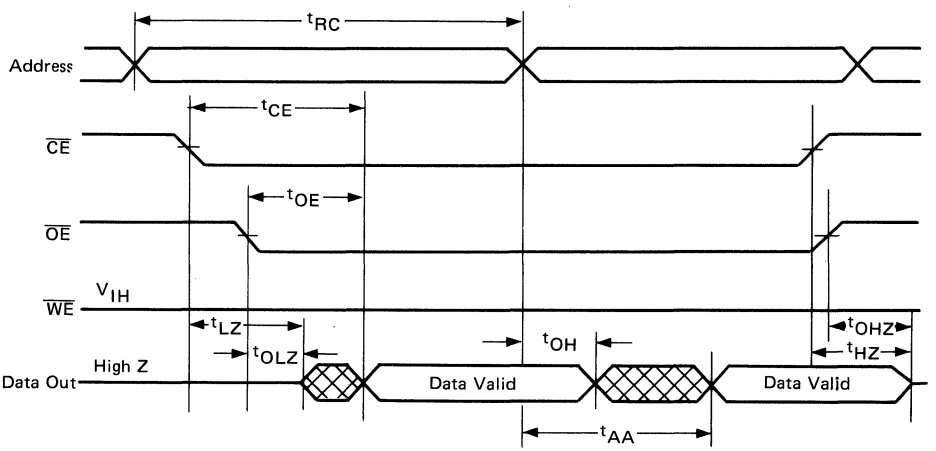
Parameter	Symbol	Conditions	MAX	Unit
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	10	pF
Input capacitance	C_{IN}	V_{IN} = 0V	6	pF

AC CHARACTERISTICS (Note 1)

(1) Read cycle

(V_{CC} = 5V ±5%, Ta = 0°C ∿ 70°C)

Parameter	Symbol	MSM2816A -250		MSM2816A -300		MSM2816A -350		MSM2816A -450		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Read cycle time	t_{RC}	250	–	300	–	350	–	450	–	ns
Chip enable access time	t_{CE}	–	250	–	300	–	350	–	450	ns
Address access time	t_{AA}	–	250	–	300	–	350	–	450	ns
Output enable access time	t_{OE}	–	100	–	120	–	135	–	150	ns
Output set time ($\overline{CE}$)	t_{LZ}	10	–	10	–	10	–	10	–	ns
Output disable time ($\overline{CE}$)	t_{HZ}	10	100	10	100	10	100	10	100	ns
Output set time ($\overline{OE}$)	t_{OLZ}	10	–	10	–	10	–	10	–	ns
Output disable time ($\overline{OE}$)	t_{OHZ}	10	70	10	80	10	100	10	100	ns
Output hold time	t_{OH}	20	–	20	–	20	–	20	–	ns



Note 1: **AC test conditions**

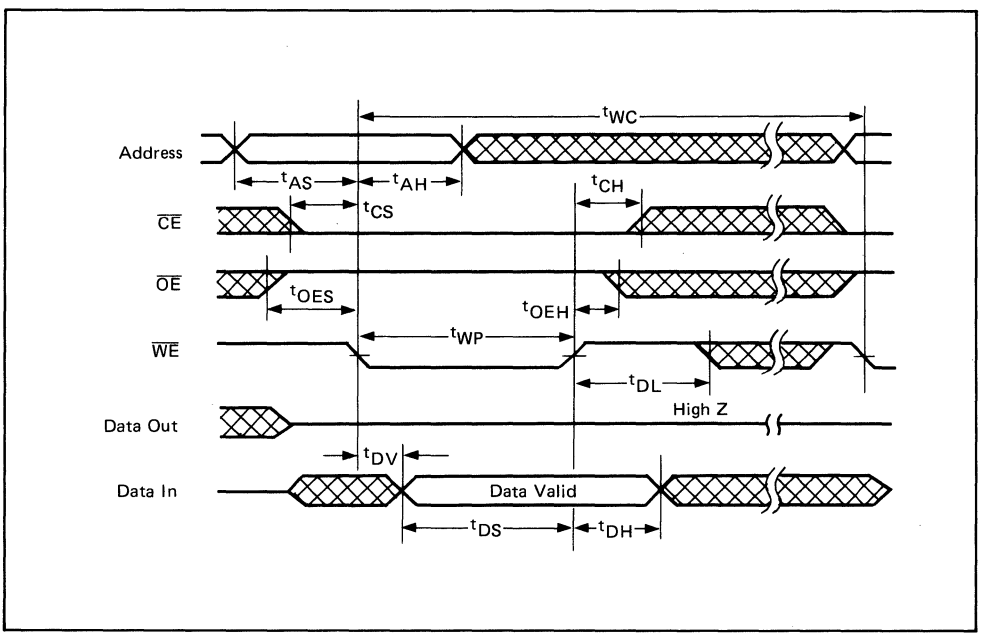
Input pulse voltage level	:	0 ∿ 3V
Pulse rise/fall time	:	10 ns
Input/output timing level	:	1.5V
Load conditions	:	1 TTL, CL = 100 pF.

(2) Write cycle (5V programming mode)

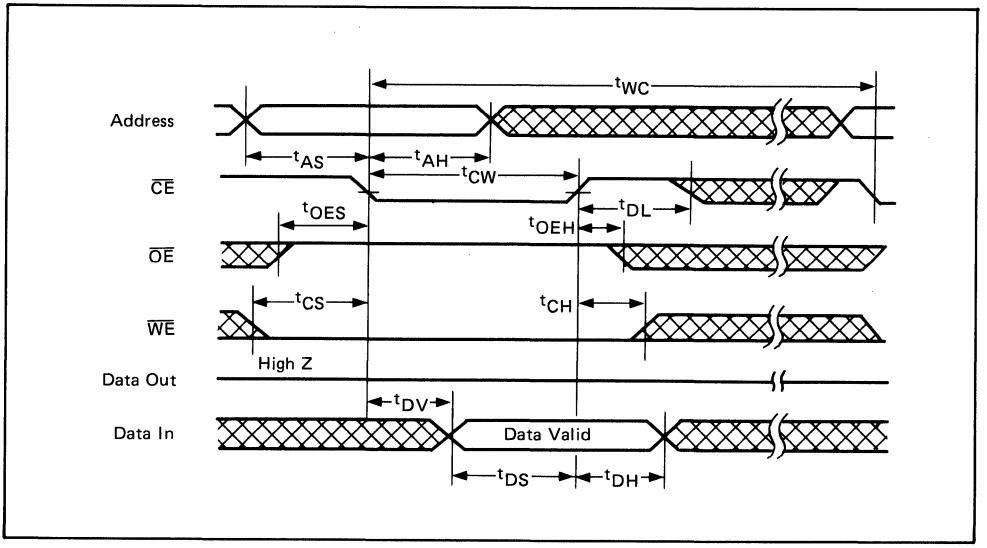
(V_{CC} = 5V ±5%, Ta = 0°C ∿ 70°C)

Parameter	Symbol	Limits		Unit
		MIN	MAX	
Write cycle time	t_{WC}	10	–	ms
Address setup time	t_{AS}	10	–	ns
Address hold time	t_{AH}	70	–	ns
Write setup time	t_{CS}	0	–	ns
Write hold time	t_{CH}	0	–	ns
Write pulse width ($\overline{CE}$)	t_{CW}	150	–	ns
Output enable setup time	t_{OES}	10	–	ns
Output enable hold time	t_{OEH}	10	–	ns
Write pulse width ($\overline{WE}$) (Note 1)	t_{WP}	150	–	ns
Data latch time	t_{DL}	50	–	ns
Data valid time (Note 2)	t_{DV}	–	1	μs
Data setup time	t_{DS}	50	–	ns
Data hold time	t_{DH}	10	–	ns
Write inhibit time during power-up	t_{INIT}	5	20	ms

• $\overline{WE}$ control write cycle



• $\overline{CE}$ control write cycle



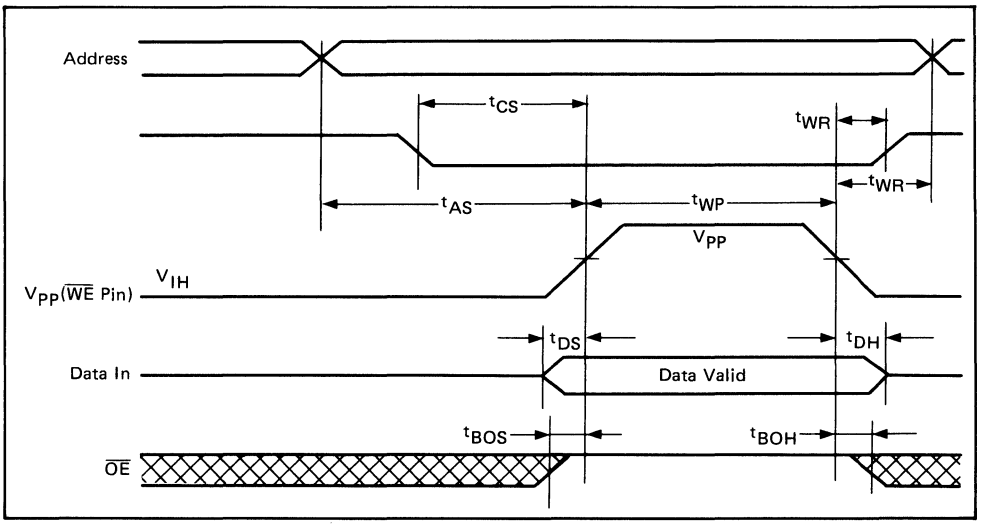
Notes: 1. $\overline{WE}$ is noise protected. No write cycle may be initiated by write pulses for 20 ns or shorter.
2. Data must be set valid within 1 μs after the start of a write cycle.

(3) Write/erase cycle **(High-voltage programming mode)**

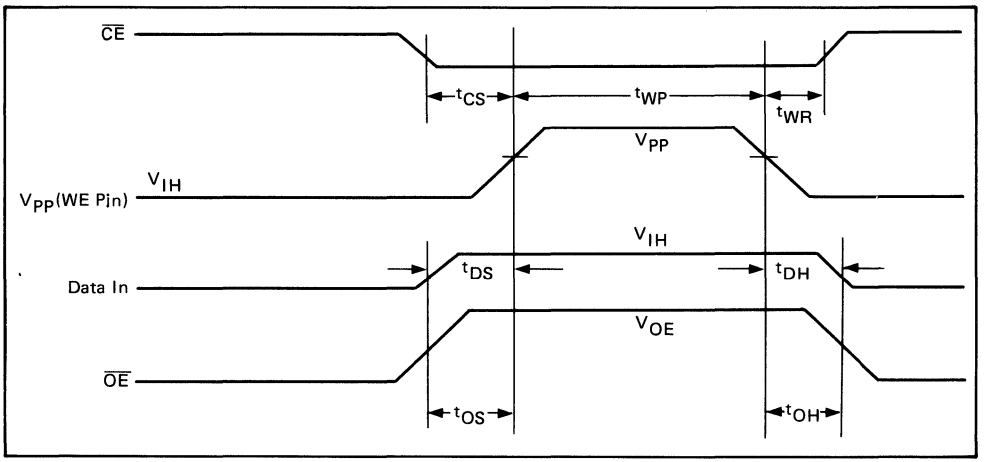
(V_{CC} = 5V ±5%, Ta = 0°C ∿ 70°C)

Parameter	Symbol	Conditions	Limits		Unit
			MIN	MAX	
Vpp address setup time	t_{AS}		10	—	ns
Vpp $\overline{CE}$ setup time	t_{CS}		10	—	ns
Vpp data setup time	t_{DS}		0	—	ns
Data hold time	t_{CH}	V_{PP} = 6V	50	—	ns
Write pulse width	t_{WP}	V_{PP} = 12V	9	70	ms
Write recovery time	t_{WR}	V_{PP} = 6V	50	—	ns
Chip erase setup time	t_{OS}	V_{PP} = 6V, V_{OE} = 12V	10	—	ns
Chip erase hold time	t_{OH}	V_{PP} = 6V, V_{OE} = 12V	10	—	ns
Vpp $\overline{OE}$ setup time	t_{BOS}	V_{PP} = 6V	10	—	ns
Vpp $\overline{OE}$ hold time	t_{BOH}	V_{PP} = 6V	10	—	ns
Write inhibit time during power-up	t_{INIT}	$V_{CC} > V_{WI}$	5	20	ms

• Byte erase/write cycle



• Chip erase cycle



PRODUCT INFORMATION

Model name	Access time	Operating temperature	Package
MSM2816A AS-250	250	0 ∿ 70°C	Cerdip
MSM2816A AS-300	300		
MSM2816A AS-350	350		
MSM2816A AS-450	450		
MSM2816A RS-250	250	0 ∿ 70°C	Plastic
MSM2816A RS-300	300		
MSM2816A RS-350	350		
MSM2816A RS-450	450		

CROSS REFERENCE LIST

10 CROSS REFERENCE LIST

(Note)

MSM3764	← Type No.
120 P.G	← Package Material
↑ Access Time (ns) max.	

P: PLASTIC J: PLCC
G: CERDIP YS: SIMM
C: SIDE-BRAZED KS: SIP

1. DYNAMIC RAM

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	64k	65536 x 1	16	MSM3764-15	HM4864-2	2164-15	TMS4164-15	MK4164-15	MCM6665-15	μPD4164-3	TMM4164C-3	M5K4164-15	MB8264-15
				150 P.C	150 C	150 C	150 C	150 C	150 C	150 C	150 P.C	150 C	150 C
				MSM3764-20	HM4864-3			MK4164-20	MCM6665-20	μPD4164-2	TMM4164C-4	M5K4164-20	MB8264-20
				200 P.C	200 C			200 C	200 C	200 C	150 P.C	200 C	200 C
												M5K4164A-10	MB8264A 10
												100 P.C	100 P.G
				MSM3764A-12	HM4864A-1		TMS4164A-12		MCM6665A-12	μPD4164A-4	TMM4164A-2	M5K4164A-12	MB8264A-12
				120 P.C	120 P.G		120 P.C		120 C	120 P.G.C	120 P	120 P.C	120 P G
				MSM3764A-15	HM4864A-2		TMS4164A-15	MK4564	MCM6665A-15	μPD4164A-3	TMM4164A-3	M5K4164A-15	MB8264A-15
				150 P.C	150 P.G		150 P.C	150 P	150 C	150 P.G.C	150 P	150 P.C	150 P.G
				MSM3764A-20	HM4864A-3		TMS4164A-20		MCM6665A-20	μPD4164A-2		M5K4164A-20	MB8264A-20
				200 P.C	200 P.G		200 P.C		200 C	200 P.G.C		200 P.C	200 P.G
NMOS	128k	131072 x 1	16	MSM37S64-15									
				150 P									
				MSM37S64-20									
				200 P									
				MSM37S64A-15									
				150 P									
				MSM37S64A-20									
				200 P									

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	256k	262144 x 1	16						MCM6256-10				MB81256-10
									100 P.C				100 P
				MSM41256-12	HM50256-12		TMS4256-12	MK4556-12	MCM6256-12	μPD41256-12	TMM41256C-12	M5M4256S-12	MB81256-12
				120 P.C.J	120 P.G		120 P	120 P	120 P.C	120 P.G.C	120 P.G	120 P.C	120 P
				MSM41256-15	HM50256-15		TMS4256-15	MK4556-15	MCM6256-15	μPD41256-15	TMM41256C-15	MSM4256S-15	MB81256-15
				150 P.C.J	150 P.G		150 P	150 P	150 P.C	150 P.G.C	150 P.G	150 P.C	150 P
				MSM41256-20	HM50256-20		TMS4256-20	MK4556-20		μPD41256-20		M5M4256S-20	
				200 P.C	200 P.G		200 P	200 P		200 P.G.C		200 P.C	
				MSM41256A-10					MCM6256-10				MB81256-10
				100 P.C					100 P.C				100 P
				MSM41256A-12	HM50256-12		TMS4256-12		MCM6256-12	μPD41256-12	TMM41256C-12	M5M4256S-12	MB81256-12
				120 P.C	120 P.G		120 P		120 P.C	120 P.G.C	120 P.G	120 P.C	120 P
				MSM41256-15	HM50256-15		TMS4256-15		MCM6256-15	μPD41256-15	TMM41256C-15	MSM4256S-15	MB81256-15
				150 P.C	150 P.G		150 P		150 P.C	150 P.G.C	150 P.G	150 P.C	150 P
				MSM41257A-10						μPD41257-10			MB81257-10
				100 P.C						100 P.C			100 P.C
				MSM41257A-12	HM50257-12		TMS4257-12		MCM6257-12	μPD41257-12	TMM41257-12	M5M41257-12	MB81257-12
				120 P.C	120 P.C		120 P		120 P.C	120 P.C	120 P.C	120 P.C	120 P.C
				MSM41257A-15	HM50257-15		TMS4257-15		MCM6257-15	μPD41257-15	TMM41257-15	M5M41257-15	MB81257-15
				150 P.C	150 P.C		150 P		150 P.C	150 P.C	150 P.C	150 P.C	150 P.C

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	256k	65536 x 4	18	MSM41464-10	HM50464P-10					μPD41464C-10			MB81464-10
				100 P	100 P					100 P			100 P
				MSM41464-12	HM50464P-12					μPD41464C-12	TMM41464P-12		MB81464-12
				120 P	120 P					120 P	120 P		120 P
				MSM41464-15	HM50464P-15					μPD41464C-15	TMM41464P-15		MB81464-15
				150 P	150 P					150 P	150 P		150 P
	512k	65536 x 8	30	MSC2301-12								MH25609-12	
				120 YS.KS								120 YS	
				MSC2301-15									
				150 YS.KS									
	576k	65536 x 9	30	MSC2301-12			TM4164-12						
				120 YS.KS			120 KS						
				MSC2301-15			TM4164-15						
				150 YS.KS			150 KS						
	2048k	262,144 x 8	30	MSC2304-12									
				120 YS.KS									
				MSC2304-15									
				150 YS.KS									
	2304k	262,144 x 9	30	MSC2304-12	HM561003-12							MH25609-12	
				120 YS.KS	120 YS.KS							120 YS	
				MSC2304-15	HM561003-15							MH25609-15	
				150 YS.KS	150 YS.KS							150 YS	

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	1M	1048576 x 1	18	MSM411000 100 P						μPD411000 100 P			
				MSM411000 120 P						μPD411000 120 P			MB81100 120 P
				MSM411001 100 P									
				MSM411001 120 P									MB811001 120 P
		262144 x 4	20	MSM414256-10 100 P									
				MSM414256-12 120 P									
CMOS	1M	1048576 x 1	18	MSM511000-10 100 P							TC511000-10 100 P		
				MSM511000-12 120 P	HM511000-12 120 P						TC511000-12 120 P		
					HM511000-15 150 P								
				MSM511001-10 100 P							TC511001-10 100 P		
				MSM511001-12 120 P	HM511001-12 120 P						TC511001-12 120 P		
					HM511001-15 150 P								

Structure	Total Bit	Organization	Number of Pin	Oki		Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
CMOS	1M	262144 x 4	20	MSM514256-10										
				100	P									
				MSM514256-12										
				120	P									
				MSM514257-10										
				100	P									
				MSM514257-12										
				120	P									

2. STATIC RAM

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	16k	2048 x 8	24								TMM2016P-1 100 P		MB8178 100 P
				MSM2128-12 120 P									
				MSM2128-15 150 P						μPD4016C-3 150 P	TMM2016P 150 P	58725-15 150 P.C	MB8178 150 P
				MSM2128-20 200 P						μPD4016C-2 200 P	TMM2016P-2 200 P	58725 200 P.C	
CMOS	4k	1024 x 4	18	MSM5114-2 200 P						μPD444-3 200 P			
										μPD444-2 250 P			
				MSM5114-3 300 P	HM4334-3 300 P					μPD444-1 300 P			
				MSM5114 450 P	HM4334-4 450 P					μPD444 450 P	TC5514 450 P	M58981-45 450 G	
											TC5514-1 650 P		
											TC5514-2 800 P		

Structure	Total Bit	Organization	Number of Pin	Oki		Hitachi		Intel	Texas	Mostek	Motorola	NEC		Toshiba		Mitsubishi		Fujitsu	
CMOS	16k	2048 x 8	24	MSM5128-12		HM6116L-2										M5M5117-12			
				120	P	120	P									120	P		
				MSM5128 15		HM6116L-3						μPD446-3				M5M5117-15		MB8416-15	
				150	P	150	P					150	P			150	P	150	P
				MSM5128-20		HM6116L-4						μPD446-2		TC5517-2				MB8416-20	
				200	P	200	P					200	P	200	P			200	P
												μPD446-1		TC5517		M5M5117			
												250	P	250	P	250	P		
				MSM5126-20		HM6116L-4						μPD446-7		TC5517-2					
				200	P	200	P					200	P	200	P				
				MSM5126-25								μPD446-1		TC5517					
				250	P							250	P	250	P				
												μPD445							
												450	P						
CMOS	64k	8192 x 8	28	MSM5165-12		HM6264-12										M5M5165-12			
				120	P	120	P									120	P		
				MSM5165-15		HM6264-15						μPD4364-15		TC5565-1				MB8464-15	
				150	P	150	P					150	P	150	P			150	P
				MSM5165-20								μPD4364-20							
				200	P							200	P						
		16384 x 4	22	MSM5188-45								μPD4362-45							
				45	P							45	P						
				MSM5188-55								μPD4362-55							
				55	P							55	P						
				MSM5188-70								μPD4362-70							
				70	P							70	P						

3. MASK ROM

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	64k	8192 x 8	24	MSM2965 300 P				MK36000-5 300 P.G	MCM68A-364 250 P.C				
					HN48364 350 P				MCM68A-364 350 P.C			M58334 650 P	
			28	MSM3864 250 P		2364A 450 P.G				μPD2364 450 P.G	TMM2364 250 P		
	128k	16384 x 8	28	MSM38128A 250 P							TMM23128 200 P		
NMOS	256k	32768 x 8	28	MSM38256 250 P				MK38000 250 P.G				M5M23256 250 P	
				MSM38256A 150 P									
	512k	65536 x 8	28	MSM38512 200 P									
CMOS	256k	32768 x 8	28	MSM53256 150 P									
	1M	131072 x 8	28	MSM531000 250 P									

4. EPROM

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	64k	8192 x 8	28	MSM2764-20	HN482764G-20	D2764-2				μPD2764D 2	TMM2764D-2		MBM2764-20
				200 G	200 G	200 G				200 G	200 G		200 G
				MSM2764-25	HN482764G	D2764				μPD2764D	TMM2764D		MBM2764 25
				250 G	250 G	250 G				250 G	250 G		250 G
				MSM2764 30	HN482764G 30	D2764-3				μPD2764D-3			MEM2764-30
				300 G	300 G	300 G				300 G			300 G
						D2764A						TMM2764AP	
						G						G	
						P2764A						TMM2764AP	
						250 P						200 P	
	128k	16384 x 8	28	MSM27128-20						μPD27128D-2	TMM27128D-20	M5L27128K-2	
				200 G						200 G	200 G	200 G	
				MSM27128-25	HN4827128G-25	D27128				μPD27128D	TMM27128D-25	M5L27128K (-1)	MBM27128-25
				250 G	250 G	250 G				250 G	250 G	250 G	250 G
				MSM27128-30	HN4827128G-30	D27128-3				μPD27128D-3		M5L27128K-3	MBM27128-30
				300 G	300 G	300 G				300 G		300 G	300 G
						D27128A					TMM27128AD		MBM27128A
						G					G		200 G
						P27128A					TMM24128AP		
						250 P					200 P		

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	256k	32768 x 8	28	MSM27256-15 150 G							TMM27256D-15 150 G		
				MSM27256-20 200 G							TMM27256AD-20 200 G	M5L27256K-2 200 G	MBM27256-20 200 G
						P27256 250 P					TMM24256AP 200 P		
				MSM27256-25 250 G	HN27256G-25 250 G	27256 250 G						M5L27256K 250 G	MBM27256-25 250 G
										μPD27256D 200 G	TMM27256D 150 G		
	512k	65536 x 8	28	MSM27512-15 150 G									
				MSM27512-20 200 G								M5L27512K-2 200 G	
				MSM27512-25 250 G	HN27512G-25 250 G	27512 250 G						M5L27512K 200 G	MBM27512-25 250 G
				MSM271000-12 120 G									
	1M	131072 x 8	32	MSM271000-15 150 G									
				MSM271000-20 200 G		27010-200V05 200 G							

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	1M	65536 x 16	40	MSM271024-12 120 G									
				MSM271024-15 150 G		27210-150/05 150 G							
						27210-170/05 170 G							
				MSM271024-20 200 G		27210-200/05 200 G							

5. E^2P ROM

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	16k	2048 x 8	24	MSM2816A-25 250 P		2816A 250 P							
				MSM2816A 30 300 P									
				MSM2816A-35 350 P		2816A-3 350 P							
				MSM2816A-45 450 P									

APPLICATIONS

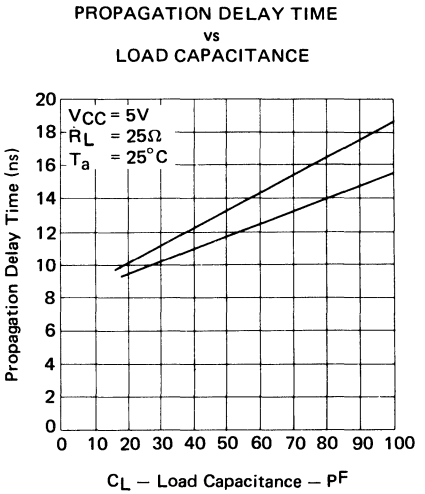
11 APPLICATIONS

64K BIT DYNAMIC RAM APPLICATION NOTES

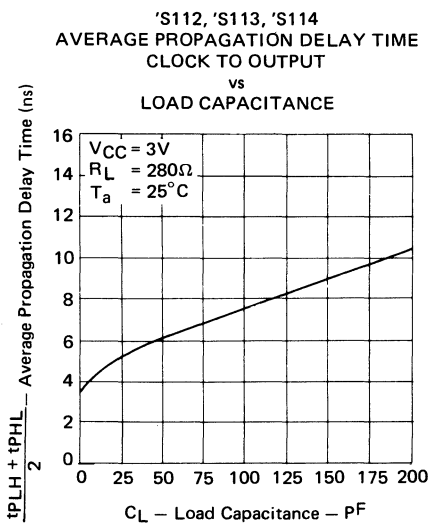
1. MEMORY DRIVER

There are problems in driving MOS ICs by a TTL driver: increase of driver delay time due to capacitive load and ringing waveform at the falling edge.
An example of the increase of delay time due to capacitive load is shown in the following figure.
The number of load memory elements must be taken into consideration when designing the timing.

In case of LS type



In case of L type



- If the number of load memory elements is 20 ~ 40 (150 ~ 300pF) on a two layer board, an undershoot of −2 to −3V (peak voltage) occurs. Therefore, measures against ringing must be taken as described in the following.

- Measures against ringing
  (1) No consideration is required for the rising edge since there is a margin.
  (2) Since ringing may be considered as a reflection due to mismatching between the driver output impedance and signal line impedance, it can be prevented by line matching (termination).
  For memory arrays, however, termination with pull up or bleeder resistance is not effective. Instead, series resistance (damping resistance) is suitable for memory arrays.
  (3) The optimal value of series resistance differs depending upon the speed, pattern status, and driver. Experience will help in determining the optimal series resistance.
  As a general rule, a resistance of 10 ~ 100Ω is suitable.
  However the speed will be lowered if the resistance is too large. An example is shown in attached drawing 3.
  (4) Make the signal lines as short as possible. Multilayer board design is effective in reducing the undershoot (as the signal line impedance is lowered).

2. DECOUPLING CAPACITORS

The dynamic MOS RAM is featured by the great power current at the active time in comparison to that at the standby time.
For example, the rated value (Icc1) of the mean power current of the MSM3764 is 45mA, while the standby current (Icc2) of the MSM3764-15 (150ns version) is 5mA. The former is approximately 10 times greater than the latter. The peak current of the MSM3764 approaches 90mA in the worst case. It is approximately 20 times as great as the standby current Icc2.
Therefore, the power circuit must be designed so as to prevent the above current variation from causing an erroneous operation of the memory. A by-pass capacitor must be inserted for this purpose. There are two types of by-pass capacitors: high frequency capacitor and low frequency capacitor.

2.1 High Frequency Capacitor

In the Icc current waveform, the peak current rises at a high speed such as 10ns, and a high frequency noise represented by the following expression is caused to occur by the L component of the current applied to the capacitor:

$$\triangle V = L\frac{\triangle i}{\triangle t}$$

To reduce the fluctuation $\triangle V$, the value of L must be reduced.
For this purpose, the capacitor must be placed as close as possible to the power pin of the IC. Further, sufficient capacity for supplying the peak current is required. The standard capacity for a double sided circuit board (two layer circuit board) is $0.05 \sim 0.1\mu F$ or more. The capacity may be less than this value for a multi layer circuit board since the L component is less than the former.
When designing a board, mount one capacitor with excellent high frequency characteristics for every two or three MOS IC memory chips, near the power pins of these IC chips.

2.2 Low Frequency Capacitor

A low frequency capacitor is required for suppressing the power fluctuation due to a sudden current variation (for example, current variation caused by a status change from the standby status to the continuous access status or concurrent refreshment of the entire board) in a board unit. The power fluctuation in this case is a slow variation of several handred ns.
For this reason, the low frequency capacitor must have a capacity larger than the high frequency capacitor.
Though the capacity requirement depends upon the number of memories which operate simultaneously (bit width), $50\mu F$ is enough for a 16 ~ 32 bit system in a practical use.
As an example of capacitor which satisfies the requirements in both 2.1 and 2.2 above, a small-sized tantalum capacitor with excellent high frequency characteristics is shown in the following table. It is desirable to mount a low frequency capacitor near the power input pin in order to suppress the fluctuation of power supplied from outside, even if this capacitor is mounted.

Manufacturer	Model	Capacity (μF)
Oki Ceramic Co.	Model CA tantalum capacitor Model CB	$0.1 \sim 20\mu F$

The frequency characteristics of the above capacitor and the power bus bar are illustrated in attached figure 1.

3. PRINTED CIRCUIT BOARD

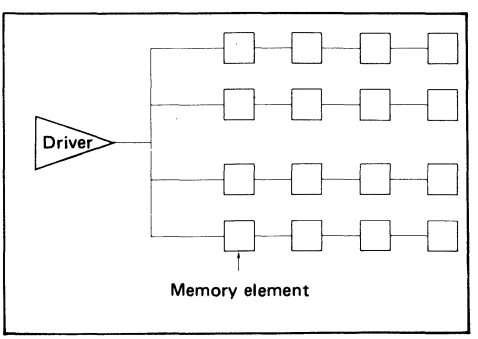
3.1 Number of Layers

Considering the measures against power noise which was described in 2. above and the routing to be described in 3.2, two layers are enough in principle.

3.2 Routing

An example of routing on a two-layer circuit board is shown in attached drawing 2. In designing the routing, note the following four points:

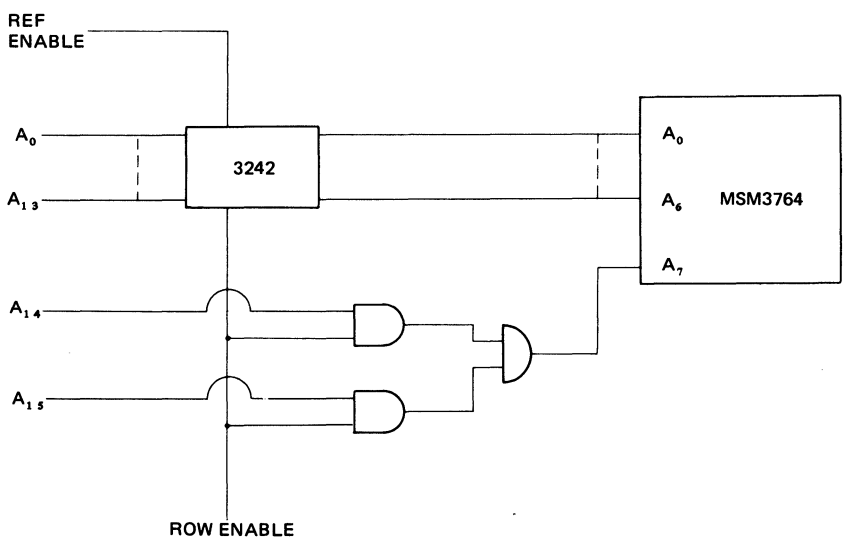
(I) The MOS drive line based on the TTL must be as short as possible to prevent ringing (reflection) and reduce crosstalk.
(II) Considerations are required to lower the impedance of the power line (including the ground). (For example, make a solid or grid-formed power line pattern. It is desirable that the power line pattern has width of at least 1.27mm.)
(III) If a signal line is to be branched for multi drive, the line must be branched at the driving end. (See the following figure.) And, the memory matrix must be designed in an integrated form, and peripheral drivers must be placed near the memory matrix.



4. PERIPHERAL CONTROL CIRCUIT

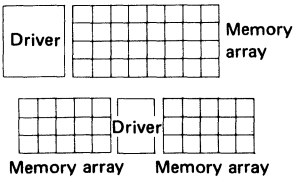
The three types of dynamic RAM control ICs shown in the following table are available at present.

Manufacturer	Model	Functions
Intel	i-3242	○ Seven-bit address multiplexer (for 16K bit dynamic RAM) ○ Seven-bit refresh address count function ○ Direct dirving capability of memory elements (for approx. 20 elements. 250 pF/25 ns 15 pF/9 ns) ○ Application to a 64K bit dynamic RAM, example (see the following figure)
Motorola	MC-3242	
Texas Instruments (T. I)	74LS601 603	○ Refresh timer using an RC multivibrator ○ Timing generation ○ Refresh address (7-bit address)
Advanced Micro Device (AMD)	Am2964A	○ Address latch/multiplex function (16-bit address) ○ Refresh address counter ○ $\overline{RAS}$ decoder (2 ~ 4)
Intel	i-8203	○ 8-bit address multiplexer (for 16K/64K DRAM) ○ Direct dring capability of memory element ○ Including timing control



5. NOTES ON MOUNTING 1 MB MEMORY ON A BOARD

The advent of a 64K bit dynamic RAM such as the MSM3764 has made it extremely easy to mount 1 MB memory on a board from the viewpoint of mounting space. In this case, however, note the following points since the number of memory elements mounted is so large as 128 ~ 176 (when redundant bits are provided).

<table>
<tr><th>Point to be noted</th><th>Consideration</th><th>Practical example</th></tr>
<tr><td>Mounting of memory elements</td><td>Memory elements may be integrated or divided.
(Design the memory array(s) to make the drive lines shortest.)</td><td> 
</td></tr>
<tr><td>Memory element driving method</td><td>Take care about the delay time and undershoot noise of the drive element.
(If the condition V_{ILmin} = −1V recommended for the MOS dynamic RAM operation is satisfied, the memory elements will display the full reliability.)</td><td>Drive element
<table>
<tr><th>Parameter / Element</th><th>Delay time</th><th>(mA) IOL</th><th>Noise</th></tr>
<tr><td>7404</td><td>Medium speed</td><td>16</td><td>○</td></tr>
<tr><td>74S04</td><td>High speed</td><td>20</td><td>×</td></tr>
</table></td></tr>
<tr><td rowspan="3">Measures against noise</td><td>○ Two layers are enough for a board.
(Pay attention to the power line pattern.)</td><td></td></tr>
<tr><td>○ High frequency noise</td><td>Mount a 0.1 ~ 1 μF capacitor for every two memory elements.</td></tr>
<tr><td>○ Low frequency noise</td><td>Mount a tantalum capacitor etc. of 50 μF or more near the power input pin of the memory package.</td></tr>
<tr><td rowspan="2">Timing design</td><td>○ Prevent skew between each timing in order to enhance the system access speed.</td><td>Use ICs of the same tipe for racing timing (for example, $\overline{RAS}$ or $\overline{CAS}$).</td></tr>
<tr><td>○ Make a sufficient margin in timing design.</td><td>Skew and mounting delay</td></tr>
<tr><td>Thermal design</td><td>Thermal design under the worst condition is required.</td><td>Operation at a case temperature of 70°C must be guaranteed.</td></tr>
</table>

6. MEMORY SYSTEM RELIABILITY

6.1 Reliability Determination Factors

The memory system reliability depends upon the four factors shown in the left column of the following table. These factors are determined as shown in the right column of this table.

Memory system reliability factor	Factor determination
System-required reliability	Determined by the user-required specifications (MTBF).
Unit capacity	α [MB] = [word depth] x [bit count]
Parts reliability	Logic element ——— Hard error Memory element ——— Soft error
Cost	

6.2 Hard Error and Soft Error

(I) Hard error

A hard error is a permanent error which occurs each time a certain address is accessed.

(II) Soft error

A soft error is a transient error that does not repeat. The following are the three causes for soft errors:

(1) Insufficient power margin
(2) Insufficient system noise margin
(3) Particle failure
(4) Insufficient power margin
(5) Insufficient system noise margin
(6) particle failure

Items (1) through (5) are largely influenced by the system design. For item (6), it is required to consider whether a remedy such as ECC should be taken or not to satisfy the system-required reliability based on the parts reliability (pertaining to hard errors and soft errors). See 1.3 and 1.4 for details.

6.3 Measures for Reliability Enhancement

The following are the two typical means for the enhancement of system reliability.

(1) Parity..... Error detection only (makes no contribution to the MTBF enhancement)
(2) ECC..... The SEC-DED* is used in general

*Single Error Correct — Double Error Detect
(one bit error correction and two bit error detection)

6.4 Reliability Calculation Method

MTBF for a hard error and a soft error

(1) Memory element reliability

Hard error $r_H = e^{-\lambda_H \cdot t}$ (λ_H: Hard error rate)
Soft error $r_S = e^{-\lambda_S \cdot t}$ (λ_S: Soft error rate)

Reliability

$$R = \underbrace{(r_H)^n}_{①} + \underbrace{nC_1 \cdot (r_H \cdot r_S)^{n-1} \cdot (1 - r_H)}_{②}$$

① Probability of no hard error
② Probability of one bit hard error followed by no hard or soft error

Find a value for t when the value of R is e^{-1}.
The following calculations are based on the assumption that there is a low probability of two bit soft error occurrence.

(2) Memory unit reliability

Assume a memory unit whose size is n bits in bit width and k blocks in address capacity. The memory element reliability is expressed as follows:

$$r = e^{-\lambda t} \quad (\lambda: \text{ error rate})$$

① One bit correction

Find a value for t which satisfies the following expression:

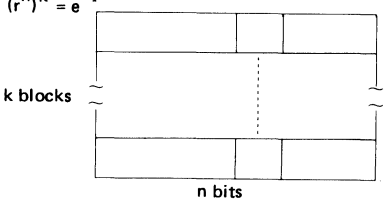
$$R = \left\{ \underbrace{(r)^n}_{①} + \underbrace{nC_1 \cdot r^{n-1}(1 - r)}_{②} \right\}^k = e^{-1}$$

① Probability of all bits being correct
② Probability of error occurrence for only one bit

② Only parity error detection without bit correction

Find a value for t which satisfies the following expression:

$$R = (r^n)^k = e^{-1}$$



6.5 Reliability Calculation Result Example

(1) Comparison of 64k byte, 128k byte, and 256k byte configurations (without ECC)

① 64kbyte

Element	λH (Fit)	λS (Fit)	MTBF (years)
64k	100	1000	11.5
16k	100	200	10.6
		100	15.9
		50	21.1
	50	200	12.7
		100	21.1
		50	31.7

② 128kbyte

Element	λH (Fit)	λS (Fit)	MTBF (years)
64k	100	1000	5.8
16k	100	200	5.3
		100	7.9
		50	10.6
	50	200	6.3
		100	10.6
		50	15.9

③ 256kbyte

Element	λH (Fit)	λS (Fit)	MTBF (years)
64k	100	1000	2.9
16k	100	200	2.6
		100	4.0
		50	5.3
	50	200	3.2
		100	5.3
		50	7.9

Notes: 1. The bit width is 9 bits for each case.
2. 1 bit is used for parity error detection.

(2) Comparison of 1M byte configurations (with ECC)

Element	λH (Fit)	λS (Fit)	Reliability (years)	
			Bit width: 22 bits	Bit width: 39 bits
64k	100 (100%)	1000	8.2 (0.76)	7.9 (0.79)
	100 (50% 50%)	1000	13.9 (0.76)	14.5 (0.79)
16k	100 (100%)	100	8.3 (1.05)	6.8 (1.08)
	100 (50% 50%)	100	13.0 (1.05)	10.7 (1.08)

Notes: 1. When the bit width is 22 bits, six bits are used for the ECC.
2. When the bit width is 39 bits, seven bits are used for the ECC.
3. Values in parentheses are the reliabilities in the case of parity error detection without ECC.
4. The (50%, 50%) in the λH column means that 50% of the hard error rate λH is handled as the total bit hard error rate and the remaining 50% is handled as the one bit hard error rate (which reflects the hard error mode analysis result confirmed so far).

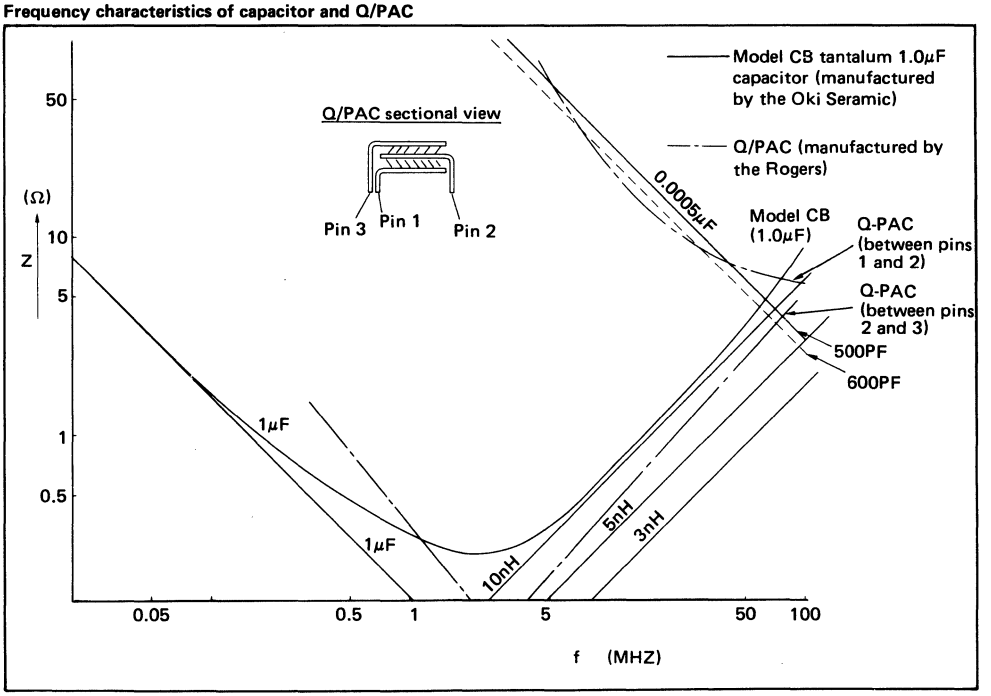
7. MEMORY COMPARISON STANDARD

In general, power, speed, and usability are required for memory elements. At present, 64K bit dynamic RAMs can be supplied by a lot of manufacturers, and these elements have almost unified specifications.

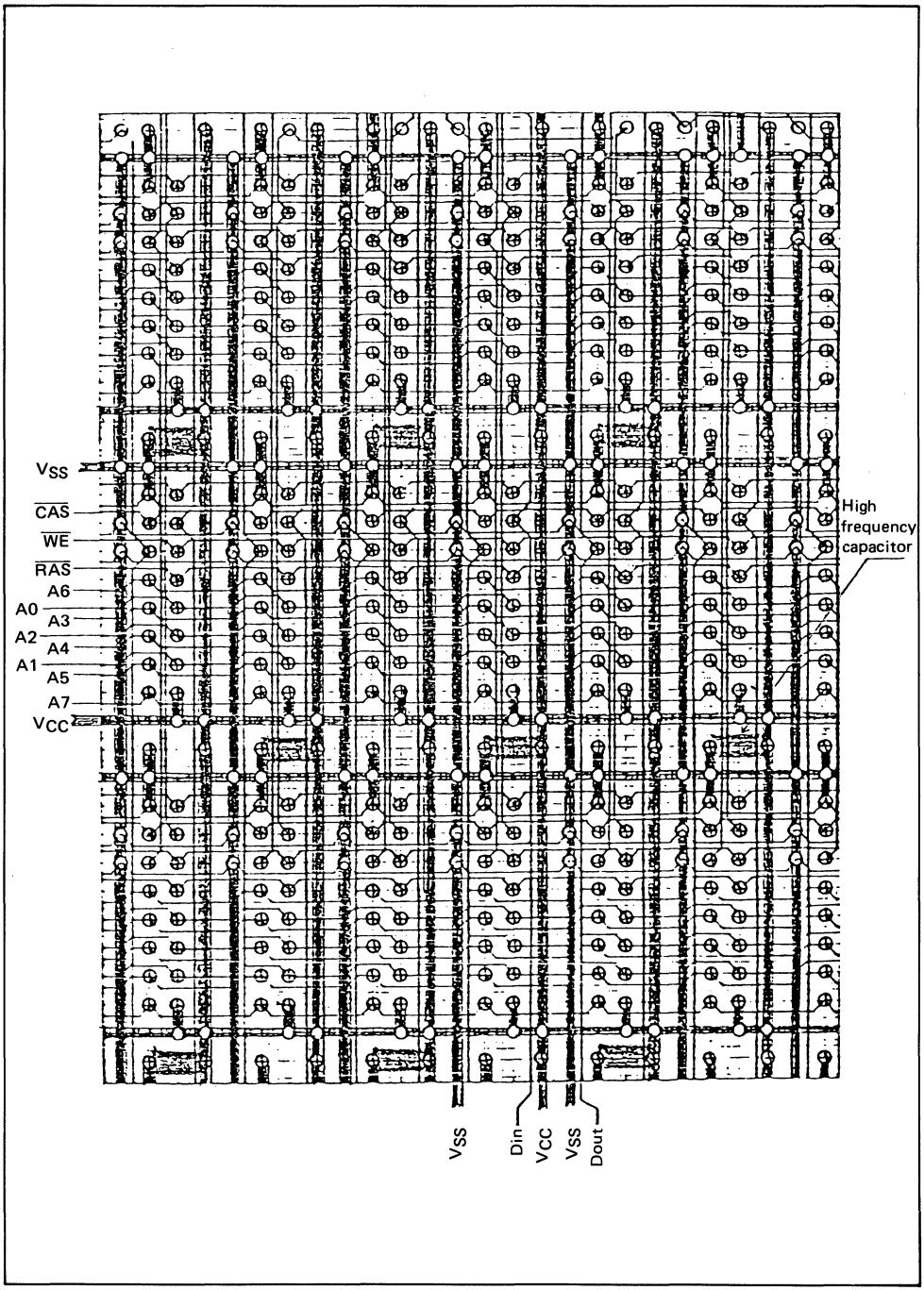
In designing a circuit board to achieve stable system operation, however, considerations must be given to the specification values and margins against the specification values, pertaining to the points shown in the following table. Factors that will affect the stable system operation are power, temperature, aging, clock skew, uneven operation of peripheral ICs, and so forth.

Point to be noted	Actual item to be considered	Reason
Power	○ Currents (Icc1, Icc3, and Icc4) at the operating time and current (Icc2) at the standby time	The power system must be noted. (example: with battery backup)
	○ Current waveform (especially the peak current value)	The noise margin must be strict for memories with large peak current.
Timing margin	○ Address setup (t_{ASR}, t_{ASC}) and hold (t_{RAH}, t_{CAH}) timing	In system designing, these timing pulses are directly related to the access time.
	○ Data setup (t_{DS}) timing and write pulse width (t_{WP})	These timing pulses are related to the cycle time in writing.
	Voltage, temperature, and dependability of each timing (especially the t_{REF} and t_{RAC})	The temperature inclination must be little for the timing pulses t_{REF} and t_{RAC}.
Voltage margin	It is impossible to achieve the ideal voltage status when used within a system.	A sufficient voltage margin must be provided under consideration of various factors which will affect the system operation stability.

Attached drawing 1
Frequency characteristics of capacitor and Q/PAC

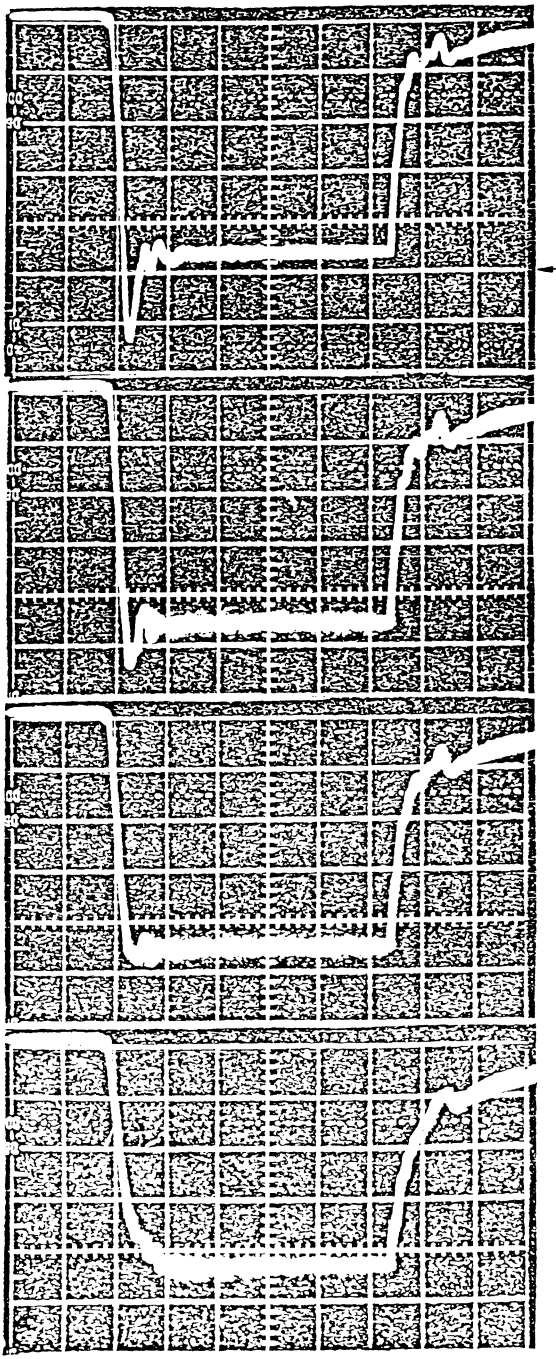


Attached drawing 2
Two layer board circuit pattern example



Attached drawing 3
Input waveform example

Horizontal: 50 ns/div
Vertical: 1 volt/div



CMOS RAM BATTERY BACK-UP

A practical example of formation of non-volatile data by CMOS static RAM battery back-up is outlined below.

1. System power and battery switching circuit

The simplest RAM power supply (CMOS Vcc) is outlined in Fig. 1. In this case, the CMOS Vcc for normal operation is kept at a voltage 0.7V below the system voltage by the voltage drop across a diode (forward direction).

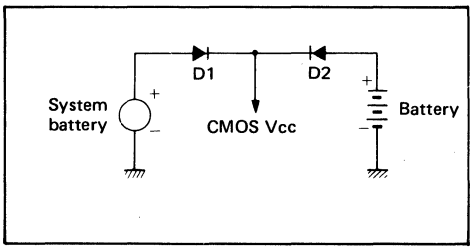


Fig. 1

Fig. 2 is an example of use of a chargeable Ni-Ca battery as the back-up battery. While the system power is being employed, the Ni-Ca battery is gradually charged up via Rc. As in Fig. 1, the diode voltage drop also poses a problem in this circuit.

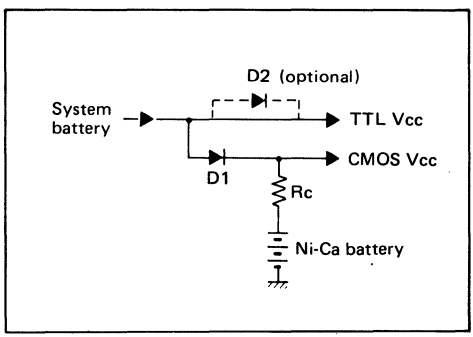


Fig. 2

The conditions for formation of non-volatile data (data retention) by battery back-up are listed below.

(1) The input signal H level must not exceed Vcc + 0.3V when the CMOS RAM Vcc power voltage is dropped.

(2) $\overline{CE}$ (or $\overline{CS}$) must maintain CMOS Vcc "H" level.

(3) In order to minimize power consumption, $\overline{WE}$, AD, DIN (or I/O) must be set to GND level or to the same "H" level as CMOS Vcc. (This is not necessary, however, for CMOS RAMs with chip select floating capability).

Note: $\overline{CS}$ floating capability
Power down possible irrespective of other input levels when memory has not been selected (i.e. when $\overline{CS}$ = H).

Consequently, if the TTL Vcc level is greater than the CMOS RAM supply voltage, and the RAM driver is at the TTL Vcc level, the CMOS RAM input voltage will exceed CMOS Vcc + 0.3V (a situation which must be avoided). Therefore, in order to reduce the voltage difference between CMOS Vcc and TTL Vcc with the battery voltage set to at least 4.5V or 4.75V (due to the RAM operating supply voltage range), the D2 diode may be added to abtain a system voltage level at least 0.7V above 4.5 ~ 4.75V (which will keep CMOS Vcc and TTL Vcc within the respective CMOS and TTL operating supply voltage ranges).
To cope with (1) and (3), a CMOS driver which will also operate at a low voltage Vcc during data hold may be employed, or else, the open collector and open drain buffer may be pulled up to CMOS Vcc in order to drive the RAM.
A control circuit for coping with (2) when an abnormal system power supply is detected is also required.

2. Switching Circuit Modifications

Modification of the diode switching circuit can employ PNP transistors. Voltage drops by PNP transistor V_{CE} are smaller by about 0.2V, and this can lead to the generation of a system "power fail" signal.

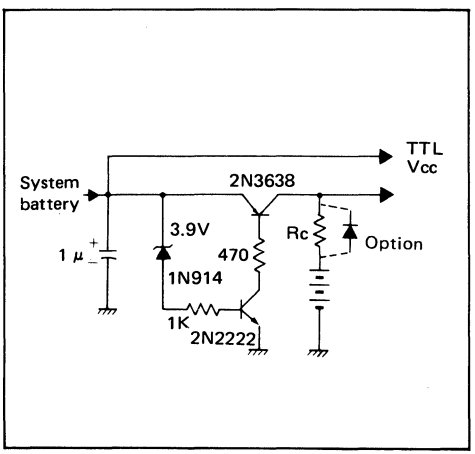


Fig. 3

Fig. 3 outlines a switching circuit employing a PNP transistor. The Rc used when a chargeable battery is employed is replaced by a diode when a non-chargeable battery is used. In this case, switching occurs at the zener diode voltage, so "power fail" must be detected by another circuit, and $\overline{CE}$ set to CMOS Vcc "high" level.

Figs. 4 and 5 are examples of circuits capable of generating a POWER FAIL output signal. In these circuits, the C2 capacitance must be rather large, the important point being the need for a smooth gradual change in CMOS Vcc when the system power is cut. See next page for further details.

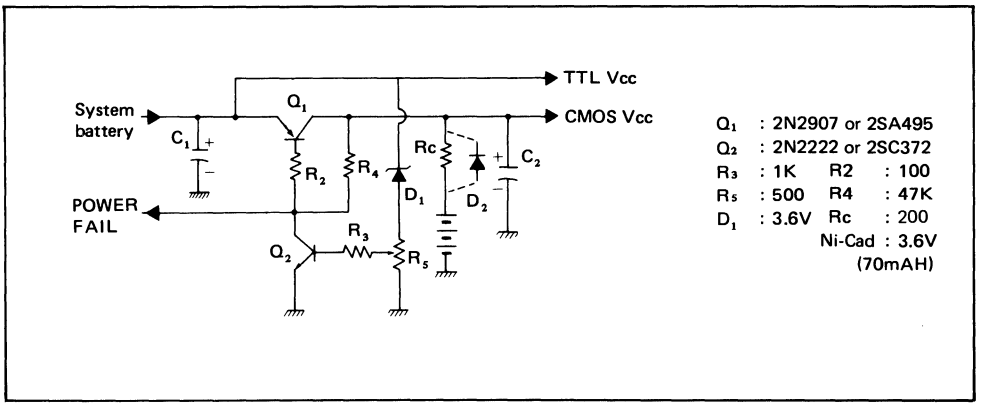


Fig. 4

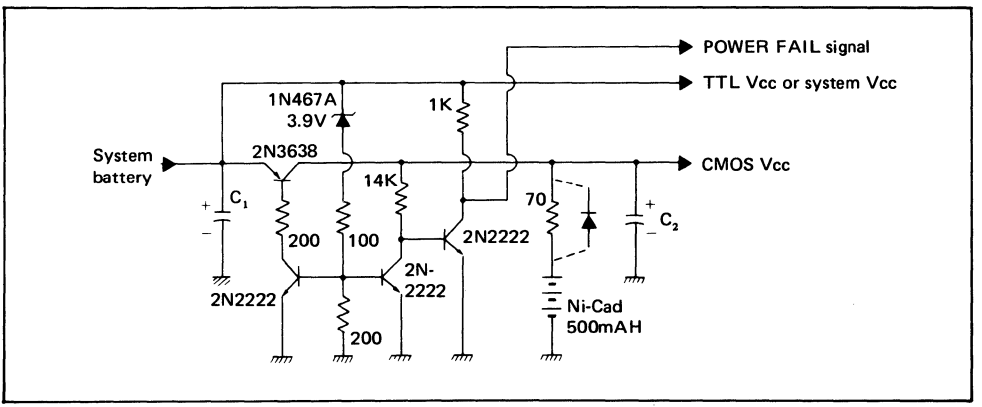


Fig. 5

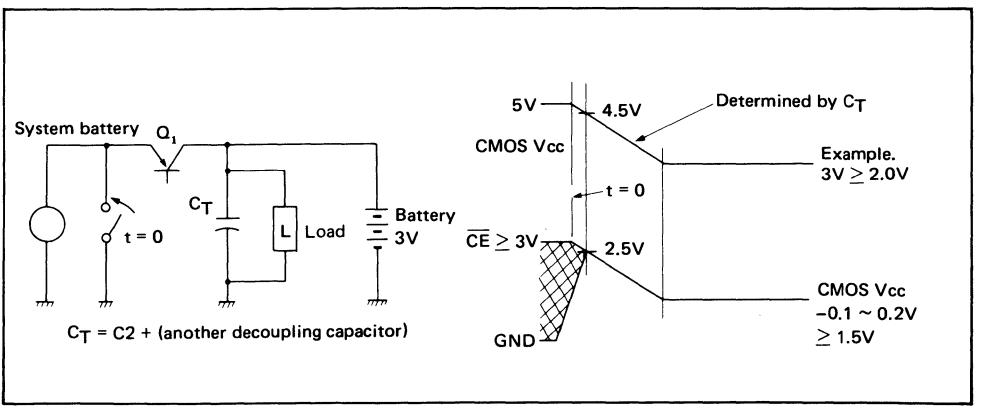


Fig. 6

3. Data Retention Mode

The RAM driver (peripheral circuit) is determined according to conditions (1) and (3) required for data retention. In Oki Electric CMOS RAMs, the power voltage during data retention is kept at a minimum of 2.0V. The $\overline{CE}$ (or $\overline{CS}$) voltage at this time has to be kept at about Vcc -0.2V. And as was mentioned earlier, the CMOS Vcc must drop smoothly when the system power is cut until it reaches the power voltage for data retention (practically equivalent to the battery voltage, or else reduced by the diode voltage drop). And although $\overline{CE}$ traces the slope of CMOS Vcc reduction at this time, a smooth change in $\overline{CE}$ is also a necessary condition for actual circuits.

(4) When switching to retention mode, or from retention mode to operation mode, $\overline{CE}$ must exhibit a smooth change. If noise is generated in $\overline{CE}$ in this case, the data will be subject to rewriting.

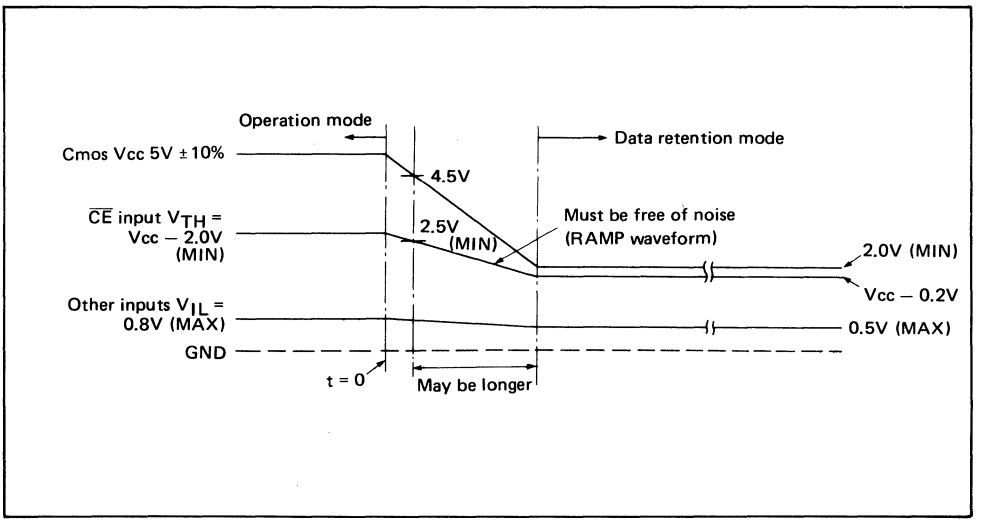


Fig. 7

(5) When switching to operation mode, commence operation after elapse of t_{RC} (read cycle time) following Vcc reaching the operating power voltage range.

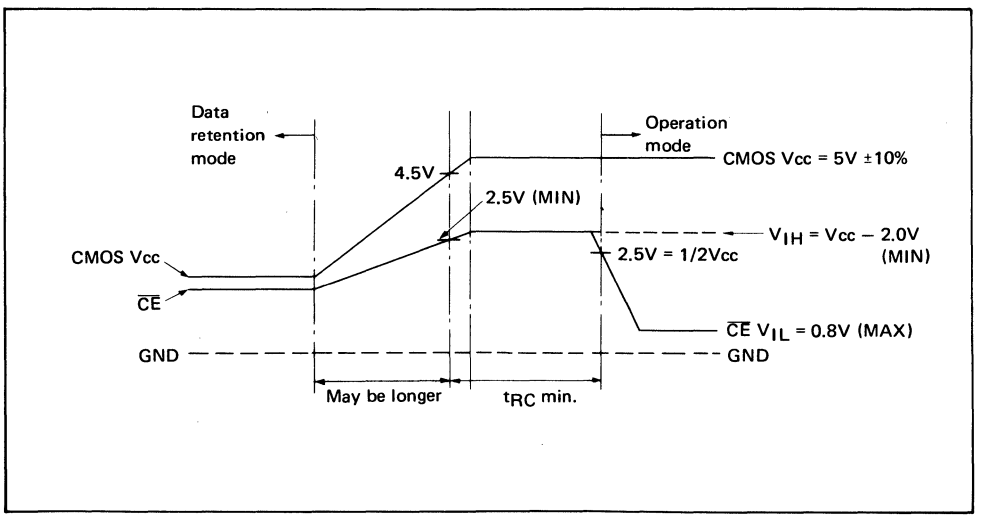


Fig. 8

4. Interfacing

A) TTL Interface

In the case of CMOS RAM drive by TTL, use an open-collector type TTL according to conditions (1) and (3).

When the system power line (i.e. TTL Vcc) is cut, the open-collector TTL Q2 in Fig. 9 is turned off, followed by Q1 also being turned off, resulting in the CMOS RAM input being pulled-up to CMOS Vcc.

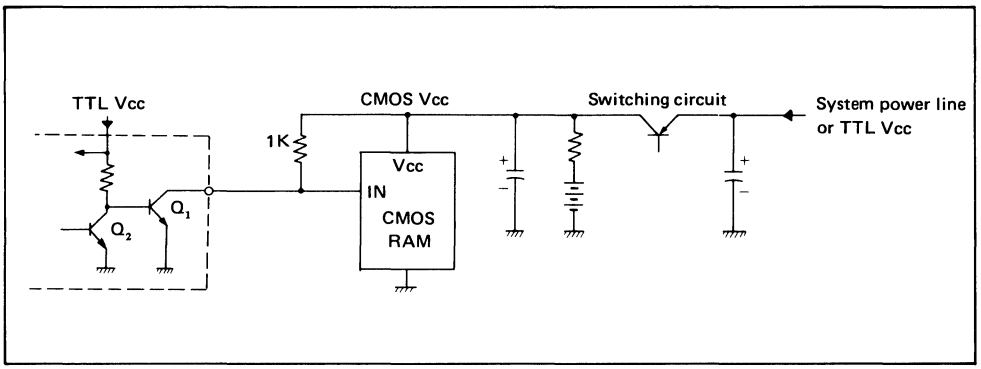


Fig. 9

When the power line voltage in LS type TTL is dropped to ground, the output is also dropped to ground, thereby making the pull-up resistors for address line buffers etc no longer necessary. In this case, however, it will not be possible to employ this as a control line buffer which must be switched to "high" during $\overline{CE}$ (or $\overline{CS}$) data retention.

(6) In order to minimize the consumption current during data retention, all inputs except $\overline{CE}$ (or $\overline{CS}$, this being designated as either "high" or "low") must be maintained at either GND or CMOS Vcc. (This does not apply, however, for CMOS RAMs equipped with $\overline{CS}$ floating function).

B) CMOS Interface

In systems where the CMOS RAM is driven by CMOS buffer, operation must be at the data retention power voltage, and the corresponding output voltage must satisfy the requirements indicated in Figs. 7 and 8.

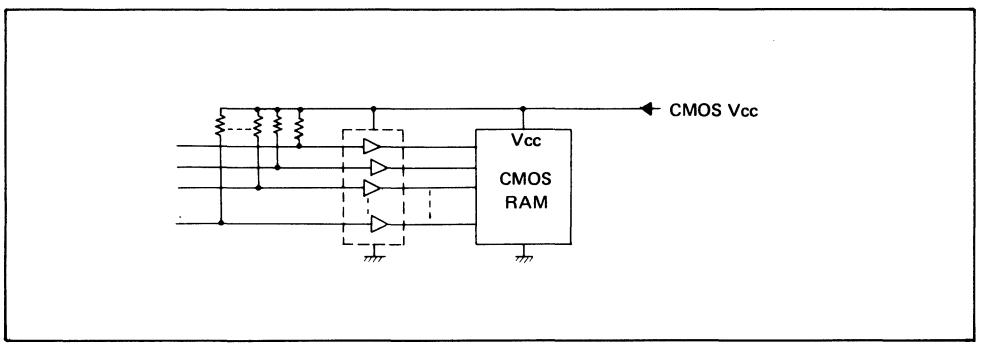


Fig. 10

5. Miscellaneous

In order to further reduce power consumption during data retention by even a small margin, the use of a MOS FET as the transistor generating the POWER FAIL output signal is recommended. This is in order to prevent flow of current from the 14kΩ resistor.

MASK ROM KANJI GENERATION MEMORY DESCRIPTION

1. KANJI GENERATION MEMORIES

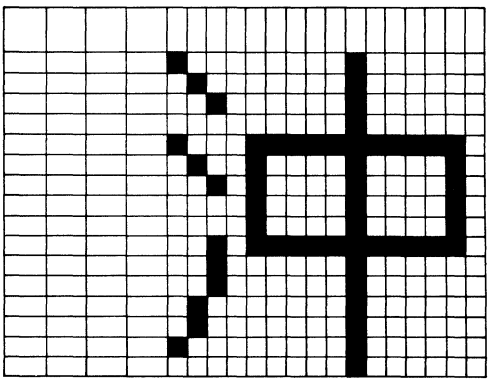
	IC models	Number of codes	Character storing capacity	Configuration	Character style	Bit capacity	Access time
High speed memories	MSM38256-19 MSM38256-22	4	JIS standard No. 1 3418 characters	15 x 16	Gothic style	25yK bits	250ns max
	MSM38256-32 MSM38256-35	4	JIS standard No. 2 3418 characters	15 x 16	Gothic style	256K bits	250ns max
	MSM38256-10 MSM38256-18	9	JIS standard No. 1 3418 characters	24 x 24	Ming style	256K bits	250ns max
	MSM38256-38 MSM38256-46	9	JIS standard No. 2 3418 characters	24 x 24	Ming style	256K bits	250ns max
Middle speed memories	MSM38128-00 MSM38128-17	18	JIS standard No. 1 3418 characters	24 x 24	Ming style	128K bits	450ns max
	MSM38128-18 MSM38128-27	10	JIS standard No. 1 3418 characters	16 x 18	Gothic style	128K bits	450ns max
Low speed memories	MSM28101A	1	JIS standard No. 1 3418 characters	16 x 18	Gothic style	1M bits	10μs max (16 x 18 transfer)
	MSM28201A	1	JIS standard No. 2 3384 characters	16 x 18	Gothic style	1M bits	10μs max (16 x 18 transfer)

2. MSM38256 SERIES

2-1 15 x 16 Font

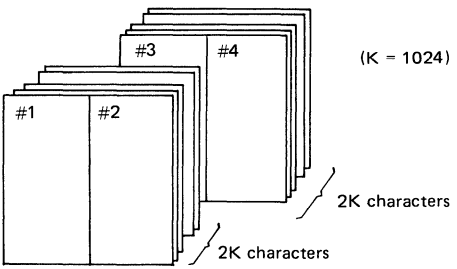
(1) Model names
MSM38256-19~22 (four codes); JIS standard No. 1 (2,965 characters) + Non-kanji (524 characters)
MSM38256-32~35 (four codes); JIS standard No. 2 (3,384 characters)
These models are similar in electrical characteristics to the MSM38256 mask ROM. The CS and OE signals are active low.

(2) Split character patterns, and their storage
• Split character patterns



- The character patterns are standard OKI character patterns.
- Each character consists of two chips.
- Character data is generated at high level, and background data is generated at low level.
- Character data is stored in a 16 x 16 dot pattern area, left-justified.

• Storage



- Each group of four chips forms one set to store about 4K characters.

	#1	#2	#3	#4
JIS standard No. 1	MSM38256-19	MSM38256-20	MSM38256-21	MSM38256-22
JIS standard No. 2	MSM38256-32	MSM38256-33	MSM38256-35	

(3) Address code conversions

The following address code conversions are required to access character patterns with the JIS C6226 kanji code:

(i) Converting JIS standards Nos. 1 and 2 (byte 1 = 50H ~ 6FH area)

	Byte 1								Byte 2							
C6226	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

	Byte 1								Byte 2							
ROM address				A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		A_{10}	A_9	A_8	A_7	A_6	A_5	A_4
Conversion address				X_5	X_4	X_3	X_2	X_1		Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

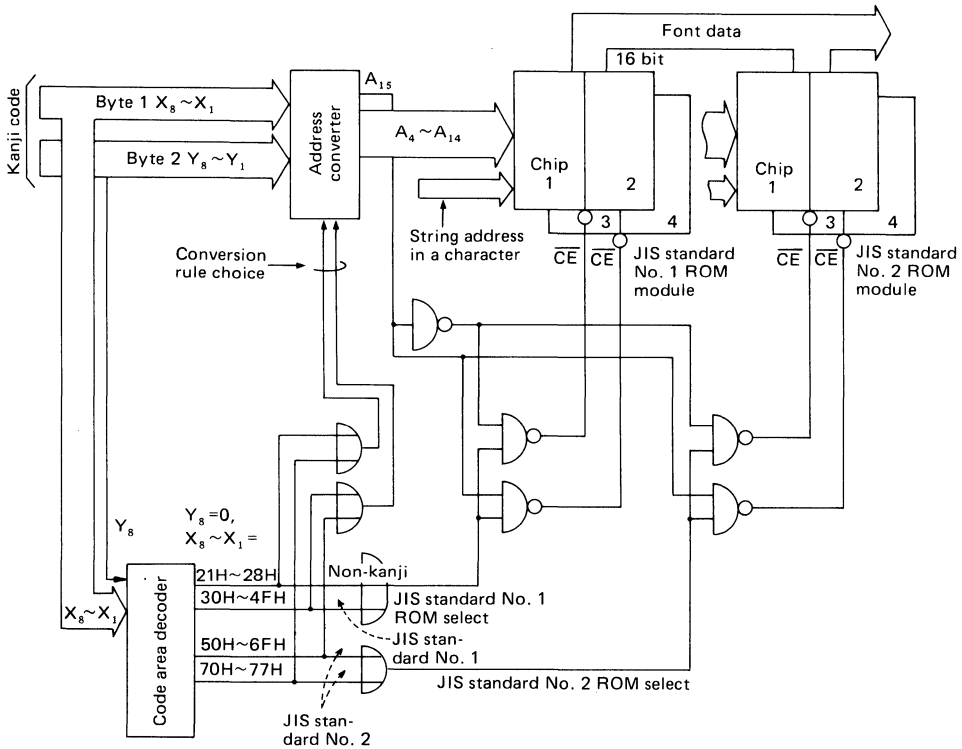
(ii) Converting non-kanji and JIS standard No. 2 (byte 1 = 70H ~ 74H)

	Byte 1								Byte 2							
C6226	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

	Byte 1								Byte 2							
ROM address				A_{15}	A_{14}	A_{13}	A_{12}	A_{11}		A_{10}	A_9	A_8	A_7	A_6	A_5	A_4
Conversion address				Y_7	Y_6	X_3	X_2	X_1		0	0	Y_5	Y_4	Y_3	Y_2	Y_1

* Use A_{15} as a CE control signal because it is not supported as a ROM address. (For further details, see the circuit example.)

15 x 16 font circuit configuration example



2-1 24 x 24 Font

(1) Model names

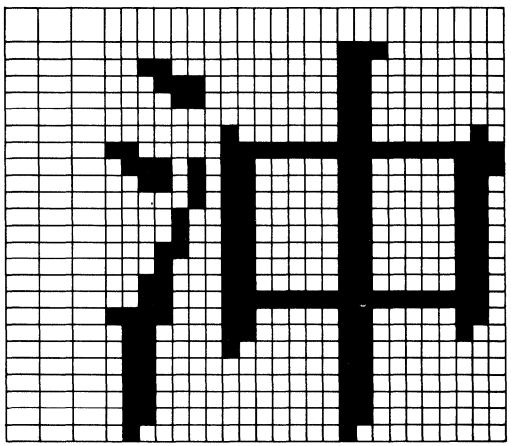
MSM38256-10~18 (nine codes); JIS standard No. 1 (2,965 characters) + Non-kanji (524 characters) + Half-size characters (159).

MSM38256-38~46; JIS standard No. 2 (3,384 characters)

These models are similar in electrical characteristics to the MSM38256 mask ROM. The CS and OE signals are active low.

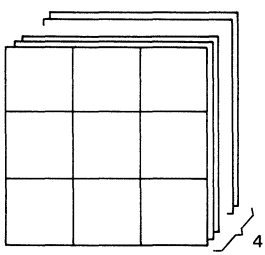
(2) Split character patterns, and their storage

• Split character patterns



- The character patterns are standard JIS character patterns.
- Each character consists of nine chips.
- Character data is generated at high level, and background data is generated at low level.

• Storage



	JIS standard No. 1	JIS standard No. 2
#1	MSM38256-10	MSM38256-38
#2	MSM38256-11	MSM38256-39
#3	MSM38256-12	MSM38256-40
#4	MSM38256-13	MSM38256-41
#5	MSM38256-14	MSM38256-42
#6	MSM38256-15	MSM38256-43
#7	MSM38256-16	MSM38256-44
#8	MSM38256-17	MSM38256-45
#9	MSM38256-18	MSM38256-46

(3) Address code conversions

The following address code conversions are required to access character patterns with the JIS C6226 and C6229 kanji code:

(i) Converting JIS standards Nos. 1 and 2 (byte 1 = 50H~6FH area)

	Byte 1								Byte 2							
C6226	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

	Byte 1								Byte 2							
ROM address				A_{14}	A_{13}	A_{12}	A_{11}	A_{10}		A_9	A_8	A_7	A_6	A_5	A_4	A_3
Conversion address				X_5	X_4	X_3	X_2	X_1		Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

(ii) Converting non-kanji and JIS standard No. 2 (byte 1 = 70H~74H area)

	Byte 1								Byte 2							
C6226	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

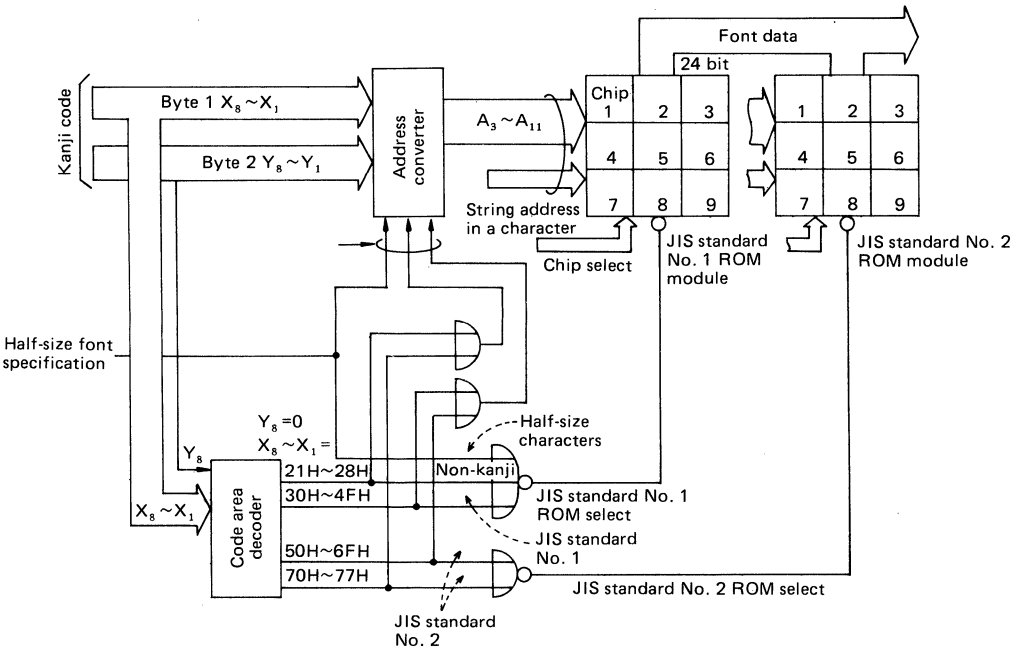
	Byte 1								Byte 2							
ROM address				A_{14}	A_{13}	A_{12}	A_{11}	A_{10}		A_9	A_8	A_7	A_6	A_5	A_4	A_3
Conversion address				Y_7	Y_6	X_3	X_2	X_1		0	0	Y_5	Y_4	Y_3	Y_2	Y_1

(iii) Converting half-size characters (C6220 code)

C6220	Z_8	Z_7	Z_6	Z_5	Z_4	Z_3	Z_2	Z_1

	Byte 1								Byte 2							
ROM address				A_{14}	A_{13}	A_{12}	A_{11}	A_{10}		A_9	A_8	A_7	A_6	A_5	A_4	A_3
Conversion address				0	0	Z_8	Z_7	Z_6		0	0	Z_5	Z_4	Z_3	Z_2	Z_1

(4) 24 x 24 font circuit configuration example



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