NEC

User's Manual

VRC4172™

Companion Chip for VR4121™

μPD31172

Document No. U14386EJ3V0UM00 (3rd edition)
Date Published September 2000 N CP(K)

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Availability of related technical literature
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- Network requirements

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Major Revisions in This Edition

Page	Description
Throughout	μPD31172 Change of development status (under development → development completed)
p. 48	Modification of description in **3.2.2 (4) Revision ID register (offset address: 0x08)**
p. 124	Modification of description in **11.2.2 Command register (offset address: 0x04)**
p. 154	Modification of description in **11.3.20 HcRhDescriptorA (offset address: 0x48)**
p. 176	Addition of **16.4 Preserving SDRAM Data**

The mark ★ shows major revised points.

INTRODUCTION

Target Readers

This manual is intended for users who wish to understand the functions of the VRC4172 and develop application systems using this chip.

Purpose

This manual is intended to give users an understanding of the architecture of the VRC4172, using the following organization.

Organization

This manual covers the following main contents.

- Overview
- Pin functions
- Address map
- Internal peripheral functions

How to Use This Manual

It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

To learn about the functions of the VRC4172:
→ Read the manual in the order listed in Contents.

To learn about the electrical specifications of the VRC4172:
→ Refer to the Data Sheet (published separately).

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	XXX# (# after pin or signal name)
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numerical representation:	Binary or decimal… XXXX
	Hexadecimal... 0xXXXX

Prefixes indicating powers of 2 (address space, memory capacity):

K (Kilo)	... $2^{10} = 1024$
M (Mega)	... $2^{20} = 1024^2$
G (Giga)	... $2^{30} = 1024^3$
T (Tera)	... $2^{40} = 1024^4$
P (Peta)	... $2^{50} = 1024^5$
E (Exa)	... $2^{60} = 1024^6$

Related Documents Please read the following related documents in combination with this manual.

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

- Device-related documents

Document Name	Document No.
V_{RC}4172 User's Manual	This manual
μPD31172 (V_{RC}4172) Data Sheet	U14388E
V_R4121 User's Manual	U13569E
μPD30121 (V_R4121) Data Sheet	U14691E

- USB-related documents (These documents are not handled by NEC.)
  - OPEN HCI Specification Release 1.0
  - PCI Local bus Specification Revision 2.1

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CHAPTER 1 OVERVIEW

This chapter gives an overview of the VRC4172 (μPD31172).

1.1 Features

The VRC4172 is a companion chip for NEC's VR4121 microprocessor.

The VRC4172 features on chip a USB host controller, IEEE1284 parallel controller, 16550 serial controller, PS/2 controller, general-purpose ports (GPIO), programmable chip select function (PCS), and PWM controller (duty modulation pulse generation function for LCD backlights).

The VRC4172 can directly be connected to the VR4121, reducing the number of man-hours required for the development of Windows™ CE systems.

The features of the VRC4172 are as follows.

- Can directly be connected to the VR4121
- On-chip USB host controller
  - 2 USB ports
  - Complies with OPEN HCI Specification Release 1.0
  - Communication with USB devices asynchronous with host CPU
  - Supports full speed (12 Mbps) and low speed (1.5 Mbps)
  - System clock: 48 MHz
- On-chip PS/2 controller
- On-chip IEEE1284 parallel controller
  - ECP, EPP, SPP and P1284 host functions
- On-chip 16550 serial controller
- Programmable chip select (PCS):6
- General-purpose ports (GPIO): 24
- On-chip PWM controller
  - Duty modulation pulse generation function for LCD backlights
- Supply voltage: V_{DD} = 3.3 ±0.3 V

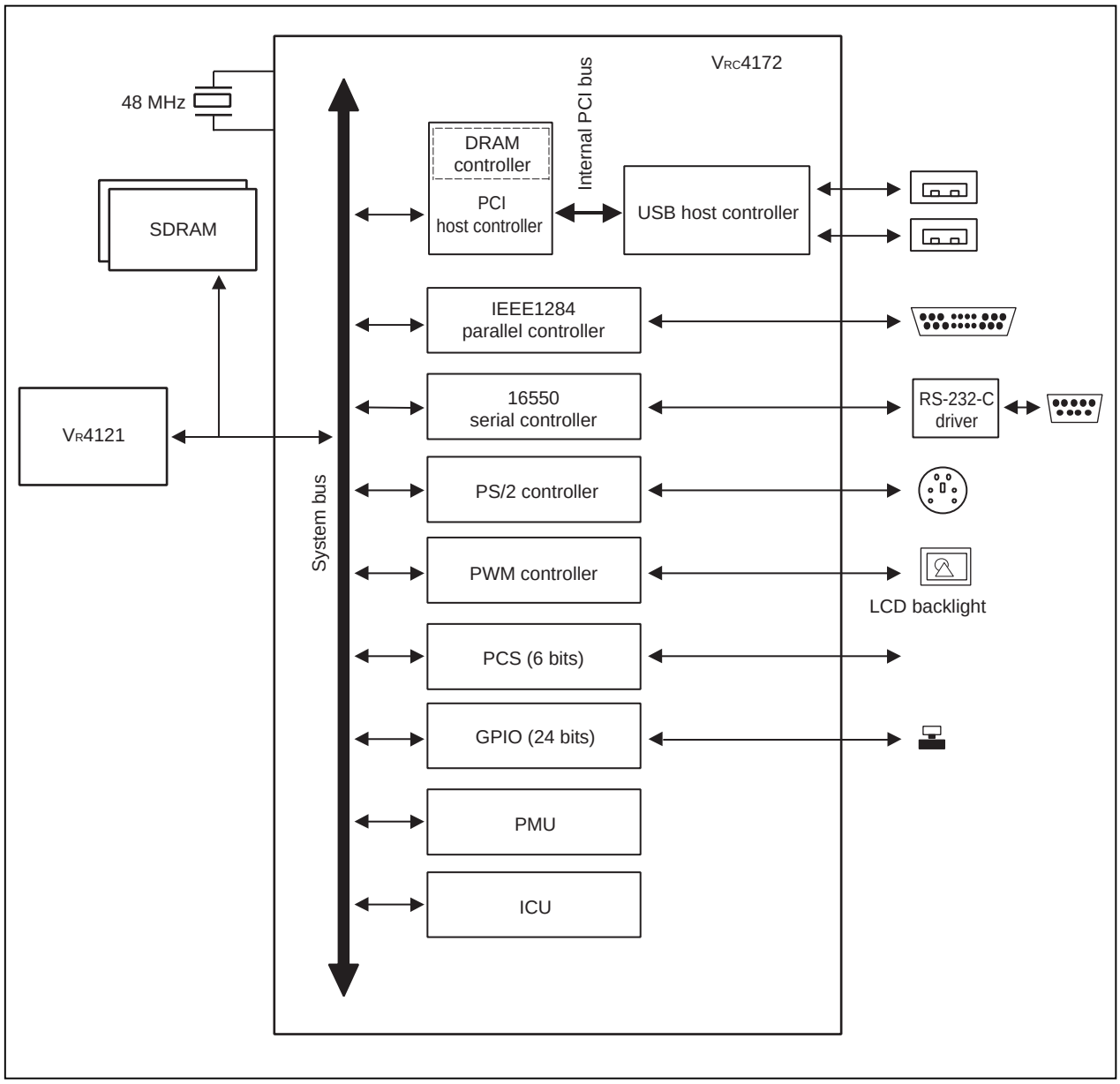
1.2 Ordering Information

Part Number	Package	Internal Maximum Operating Frequency
μPD31172F1-48-FN	208-pin plastic FBGA (15 × 15)	48 MHz

1.3 VRC4172 Processor

Figure 1-1 shows the internal block diagram of the VRC4172 and an example of connection with external components.

Figure 1-1. Internal Block Diagram and External Block Connection Example



1.3.1 Internal block configuration

(1) PCI host controller

The PCI host controller controls access from the system bus to the USB host controller.

Access to the USB host controller is done using the PCI bus. For this reason, the PCI host controller contains PCI configuration registers (PCI host control register). Access to the USB host controller is made possible by setting these registers.

(2) USB host controller

This controller is a USB host controller that complies with OPEN HCI Specification Release 1.0. It provides two downstream ports.

(3) IEEE1284 parallel controller

This controller is a parallel interface (host controller) that complies with the IEEE 1284 standard.

(4) 16550 serial controller

The 16550 serial controller is a serial interface for communication that is compatible with RS-232-C. It provides 1 channel each for transmitting and receiving data. This controller is functionally compatible with the NS16550D.

(5) PS/2 controller

The PS/2 controller performs control of bi-directional data transfer using the PS2CLK and PS2DATA signals.

(6) PWM controller

The PWM controller controls the frequency and duty of the modulation pulse for LCD backlights.

(7) PCS (Programmable Chip Select)

PCS compares the addresses set in a register with the addresses on the system bus and generates the EXCS# signal. The EXCS# signal is low level when the addresses match.

(8) GPIO (General-Purpose I/O ports)

GPIO control the GPIO pins. The GPIO pins are 24 general-purpose ports that support both input and output. Interrupt request signal input functions can be allocated to these ports, and 5 triggers can be selected: input signal changes (rising edge, falling edge, both edges), low level, and high level.

(9) PMU (Power Management Unit)

The PMU controls the clock supply and reset for the IEEE1284 parallel controller, 16550 serial controller, PS/2 controller, PWM controller, and USB host controller. It also performs enable/disable settings for the internal oscillator (48 MHz).

(10) ICU (Interrupt Control Unit)

The ICU controls the interrupts for the IEEE1284 parallel controller and the 16550 serial controller.

1.3.2 Registers of each unit

The registers of the various units are listed below.

Table 1-1. PCI Configuration Cycle Registers

Name	Register Address
PCI configuration address register	0x0AFF 0CF8
PCI configuration data register	0x0AFF 0CFC

Table 1-2. PCI Host Control Registers

Name	Offset Address
Vendor ID register	0x00
Command register	0x04
Status register	0x06
Revision ID register	0x08
Memory base address register	0x10 to 12
Control register	0x50

Table 1-3. GPIO Registers

Symbol	Function	Register Address
EXGPDATA0	GPIO (15:0) I/O data register	0x1500 1080
EXGPDIR0	GPIO (15:0) I/O setting register	0x1500 1082
EXGPINTEN0	GPIO (15:0) interrupt enable register	0x1500 1084
EXGPINTST0	GPIO (15:0) interrupt register	0x1500 1086
EXGPINTTYP0	GPIO (15:0) interrupt trigger register	0x1500 1088
EXGPINTLV0L	GPIO (15:0) interrupt level setting lower register	0x1500 108A
EXGPINTLV0H	GPIO (15:0) interrupt level setting higher register	0x1500 108C
EXGPDATA1	GPIO (23:16) I/O data register	0x1500 10C0
EXGPDIR1	GPIO (23:16) I/O setting register	0x1500 10C2
EXGPINTEN1	GPIO (23:16) interrupt enable register	0x1500 10C4
EXGPINTST1	GPIO (23:16) interrupt register	0x1500 10C6
EXGPINTTYP1	GPIO (23:16) interrupt trigger register	0x1500 10C8
EXGPINTLV1L	GPIO (23:16) interrupt level setting lower register	0x1500 10CA

Table 1-4. PCS Registers

Symbol	Function	Register Address
EXCS0SELL	EXCS0# compare address lower register	0x1500 1090
EXCS0SELH	EXCS0# compare address higher register	0x1500 1092
EXCS0MSKL	EXCS0# compare address mask lower & enable register	0x1500 1094
EXCS0MSKH	EXCS0# compare address mask higher register	0x1500 1096
EXCS1SELL	EXCS1# compare address lower register	0x1500 1098
EXCS1SELH	EXCS1# compare address higher register	0x1500 109A
EXCS1MSKL	EXCS1# compare address mask lower & enable register	0x1500 109C
EXCS1MSKH	EXCS1# compare address mask higher register	0x1500 109E
EXCS2SELL	EXCS2# compare address lower register	0x1500 10A0
EXCS2SELH	EXCS2# compare address higher register	0x1500 10A2
EXCS2MSKL	EXCS2# compare address mask lower & enable register	0x1500 10A4
EXCS2MSKH	EXCS2# compare address mask higher register	0x1500 10A6
EXCS3SELL	EXCS3# compare address lower register	0x1500 10A8
EXCS3SELH	EXCS3# compare address higher register	0x1500 10AA
EXCS3MSKL	EXCS3# compare address mask lower & enable register	0x1500 10AC
EXCS3MSKH	EXCS3# compare address mask higher register	0x1500 10AE
EXCS4SELL	EXCS4# compare address lower register	0x1500 10B0
EXCS4SELH	EXCS4# compare address higher register	0x1500 10B2
EXCS4MSKL	EXCS4# compare address mask lower & enable register	0x1500 10B4
EXCS4MSKH	EXCS4# compare address mask higher register	0x1500 10B6
EXCS5SELL	EXCS5# compare address lower register	0x1500 10B8
EXCS5SELH	EXCS5# compare address higher register	0x1500 10BA
EXCS5MSKL	EXCS5# compare address mask lower & enable register	0x1500 10BC
EXCS5MSKH	EXCS5# compare address mask higher register	0x1500 10BE

Table 1-5. PWM Registers

Symbol	Function	Register Address
LCDDUTYEN	LCDBAK enable register	0x1500 3880
LCDFREQ	LCDBAK frequency register	0x1500 3882
LCDDUTY	LCDBAK duty register	0x1500 3884

Table 1-6. PMU Registers

Symbol	Function	Register Address
SYSCLKCTRL	SYSCLK enable register	0x1500 3800
1284CTRL	1284 parallel clock/reset control register	0x1500 3802
16550CTRL	16550 serial clock/reset control register	0x1500 3804
USBCTRL	USB clock control register	0x1500 380C
PS2PWMCTRL	PS/2, PWM clock/reset control register	0x1500 380E

Table 1-7. ICU Registers

Symbol	Function	Register Address
1284INTRQ	IEEE1284 parallel controller interrupt control register	0x1500 3808
16550INTRQ	16550 serial controller interrupt control register	0x1500 380A

Table 1-8. Parallel Control Registers

Symbol	Function	Register Address
DATA	Parallel port data register	0x1500 3820
AFIFO	ECP address FIFO	
DSR	Device status register	0x1500 3822
DCR	Device control register	0x1500 3824
MCR	Mode control register	0x1500 3826
EPPA	EPP address register	
EPPD	EPP data register	0x1500 3828
CFIFO	Parallel port data FIFO	0x1500 3830
DFIFO	ECP data FIFO	
TFIFO	Test FIFO	
CNFGA	Configuration register A	
CNFGB	Configuration register B	0x1500 3832
ECR	Expansion control register	0x1500 3834

Table 1-9. Serial Control Registers

Symbol	Function	Register Address
RBR	Receive buffer register	0x1500 3810
THR	Transmit hold register	
DLL	Divide ratio lower register	
IER	Interrupt enable register	0x1500 3812
DLM	Divide ratio higher register	
IIR	Interrupt display register	0x1500 3814
FCR	FIFO control register	
LCR	Line control register	0x1500 3816
MCR	Modem control register	0x1500 3818
LSR	Line status register	0x1500 381A
MSR	Modem status register	0x1500 381C
SCR	Scratch register	0x1500 381E

Table 1-10. USB Host Control Configuration Registers

Name	Offset Address
Vendor ID register	0x00
Device ID register	0x02
Command register	0x04
Status register	0x06
Revision ID register	0x08
Class code base address register	0x09
Class code subclass register	
Class code programming interface register	
Cache line size register	0x0C
Latency timer register	0x0D
Header type register	0x0E
BIST register	0x0F
Built-in self test register	0x10
Subsystem vendor ID register	0x2C
Subsystem ID register	0x2E
Interrupt line register	0x3C
Interrupt mode register	0x3D
Min_Gnt register (burst cycle minimum request time register)	0x3E
Max_lat register (bus mastership request frequency register)	0x3F
Power management control/status register	0xE0

Table 1-11. Host Control Operational Registers

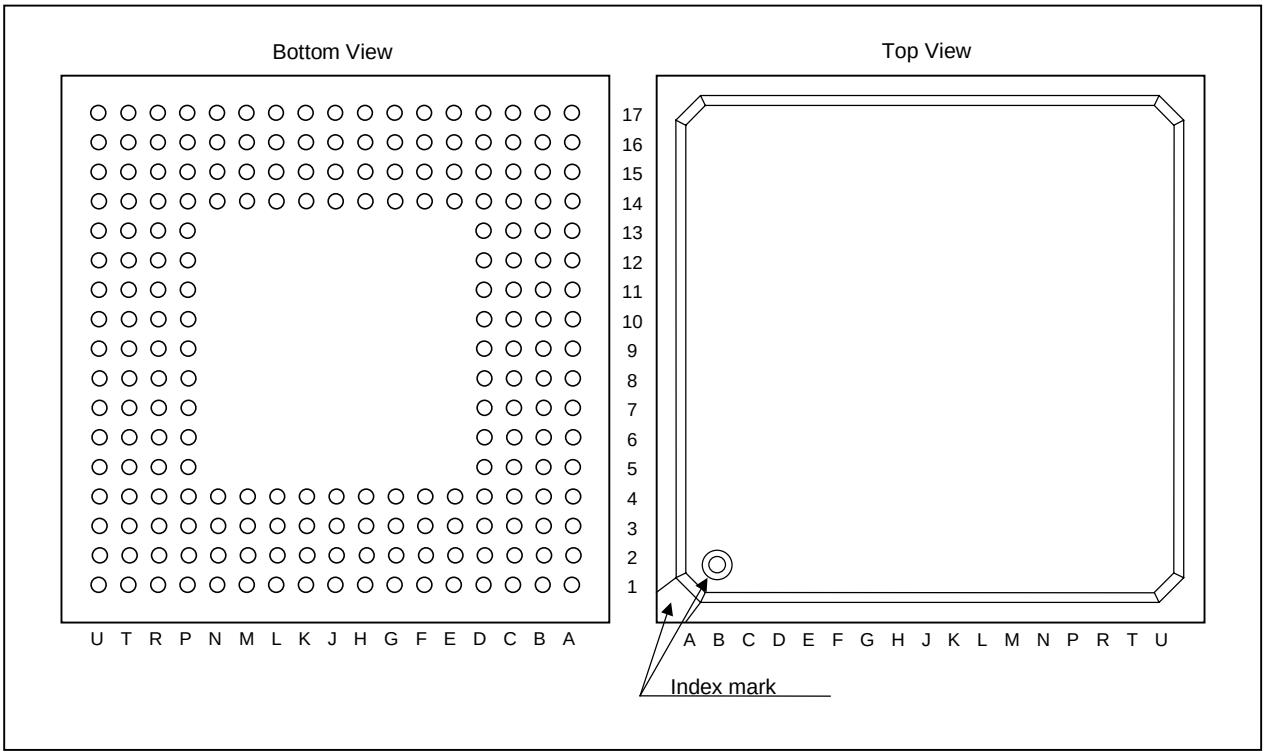
Symbol	Function	Offset Address
HcRevision	HC revision register	0x00
HcControl	HC control register	0x04
HcCommandStatus	HC command status register	0x08
HcInterruptStatus	HC interrupt status register	0x0C
HcInterruptEnable	HC interrupt enable register	0x10
HcInterruptDisable	HC interrupt disable register	0x14
HcHCCA	HC communication area register	0x18
HcPeriodCurrentED	HC period current ED register	0x1C
HcControlHeadED	HC control head ED register	0x20
HcControlCurrentED	HC control current ED register	0x24
HcBulkHeadED	HC bulk head ED register	0x28
HcBulkCurrentED	HC bulk current ED register	0x2C
HcDoneHead	HC done head register	0x30
HcFmInterval	HC frame interval register	0x34
HcFmRemaining	HC frame remaining register	0x38
HcFmNumber	HC frame number register	0x3C
HcPeriodicStart	HC periodic start register	0x40
HcLSThreshold	HC LS threshold register	0x44
HcRhDescriptorA	HC RH descriptor A register	0x48
HcRhDescriptorB	HC RH descriptor B register	0x4C
HcRhStatus	HC RH status register	0x50
HcRhPortStatus1	HC RH port status 1 register	0x54
HcRhPortStatus2	HC RH port status 2 register	0x58

Table 1-12. PS/2 Registers

Symbol	Function	Register Address
PS2DATA	PS/2 transmit/receive data register	0x1500 3870
PS2CTRL	PS/2 control register	0x1500 3872

2.1 Pin Configuration

- 208-pin plastic FBGA (15 × 15)



No.	Name	No.	Name	No.	Name	No.	Name
A1	GND	C3	STROBE#	E14	GND	K1	GPIO14
A2	AUTOFEED#	C4	ACK#	E15	PPON1	K2	GPIO10
A3	PE	C5	ERROR#	E16	OCI2	K3	GPIO7
A4	INIT#	C6	AD6	E17	USBRST#	K4	GPIO3
A5	IOCHRDY	C7	AD7	F1	GPIO22	K14	EXCS3#
A6	AD19	C8	AD8	F2	GPIO18	K15	EXCS0#
A7	AD20	C9	V_{DD}	F3	CD2	K16	SCAS#
A8	AD21	C10	AD9	F4	CD6	K17	SRAS#
A9	AD22	C11	AD10	F14	SCLK	L1	GPIO13
A10	AD23	C12	AD11	F15	PPON2	L2	GPIO9
A11	AD24	C13	LCDBAK	F16	LCAS#	L3	GPIO6
A12	Reserved[Note 1]	C14	SMI#	F17	MRAS0#	L4	GPIO2
A13	Reserved[Note 1]	C15	USBINT#	G1	GPIO21	L14	EXCS4#
A14	DP1	C16	GND	G2	GPIO17	L15	EXCS1#
A15	DN2	C17	RD#	G3	CD1	L16	Reserved (0)[Note 2]
A16	DP2	D1	GND	G4	CD5	L17	GND
A17	LCDRDY	D2	SELECTIN#	G14	Reserved[Note 1]	M1	GPIO12
B1	PS2CLK	D3	DIR1284	G15	Reserved[Note 1]	M2	GPIO8
B2	V_{DD}	D4	PS2INT	G16	UCAS#	M3	GPIO5
B3	V_{DD}	D5	SELECT	G17	MRAS1#	M4	GPIO1
B4	BUSY	D6	AD0	H1	GPIO20	M14	EXCS5#
B5	GND	D7	AD1	H2	GPIO16	M15	EXCS2#
B6	AD12	D8	AD2	H3	CD0	M16	Reserved (0)[Note 2]
B7	AD13	D9	GND	H4	CD4	M17	CKE
B8	AD14	D10	AD3	H14	Reserved[Note 1]	N1	RESET
B9	AD15	D11	AD4	H15	ARBCLKSEL	N2	BUSRQ0#
B10	AD16	D12	AD5	H16	ULCAS#	N3	GPIO4
B11	AD17	D13	V_{DD}	H17	ROMCS2#	N4	GPIO0
B12	AD18	D14	IEN	J1	GPIO15	N14	GND
B13	GND	D15	WAKE	J2	GPIO11	N15	DSR#
B14	DN1	D16	OCI1	J3	V_{DD}	N16	RXD
B15	V_{DD}	D17	LCDCS#	J4	GND	N17	RI#
B16	GND	E1	GPIO23	J14	V_{DD}	P1	HOLDRQ#
B17	WR#	E2	GPIO19	J15	GND	P2	BUSAK0#
C1	PS2DATA	E3	CD3	J16	UUCAS#	P3	BUSRQ1#
C2	GND	E4	CD7	J17	ROMCS3#	P4	GND

Notes 1. Leave the A12, A13, G14, G15, and H14 pins open, or input 0.

2. Be sure to input 0 to the L16 and M16 pins.

Remark # indicates active low.

No.	Name	No.	Name	No.	Name	No.	Name
P5	DATA31	R4	DATA23	T3	V_{DD}	U2	IRQ
P6	DATA30	R5	DATA22	T4	V_{DD}	U3	IOR#
P7	DATA29	R6	V_{DD}	T5	DATA15	U4	IOW#
P8	DATA28	R7	DATA21	T6	DATA14	U5	GND
P9	V_{DD}	R8	DATA20	T7	GND	U6	DATA7
P10	DATA27	R9	GND	T8	DATA13	U7	DATA6
P11	DATA26	R10	DATA19	T9	DATA12	U8	DATA5
P12	DATA25	R11	DATA18	T10	DATA11	U9	DATA4
P13	DATA24	R12	V_{DD}	T11	DATA10	U10	DATA3
P14	CLKOUT48M	R13	DATA17	T12	GND	U11	DATA2
P15	DCD#	R14	DATA16	T13	DATA9	U12	DATA1
P16	TXD	R15	CTS#	T14	DATA8	U13	DATA0
P17	INTRP	R16	GND	T15	V_{DD}	U14	GND
R1	HOLDAK#	R17	XOUT48M	T16	V_{DD}	U15	DTR#
R2	GND	T1	BUSCLK	T17	XIN48M	U16	RTS#
R3	BUSAK1#	T2	GND	U1	IOCS16#	U17	GND

Remark # indicates active low.

Pin Names

ACK#:	Acknowledge	MRAS (0:1)#:	DRAM Row Address Strobe
AD (0:24):	Address Bus	OCI (1:2):	Over Current Interrupt
ARBCLKSEL:	Arbitration Clock Select	PE:	Paper End
AUTOFEED#:	Autofeed	PPON (1:2):	Port Power ON
BUSAK (0:1)#:	Bus Acknowledge	PS2CLK:	PS2 Clock
BUSCLK:	System Bus Clock	PS2DATA:	PS2 Data
BUSRQ (0:1)#:	Bus Request	PS2INT:	PS2 Interrupt
BUSY:	Busy	RD#:	Read
CD (0:7):	Centronics Data	RESET:	Reset
CKE:	Clock Enable	RI#:	Ring Indicator
CLKOUT48M:	Clock Out of 48 MHz	ROMCS (2:3)#:	ROM Chip Select
CTS#:	Clear to Send	RTS#:	Request to Send
DATA (0:31):	Data Bus	RXD:	Receive Data
DCD#:	Data Carrier Detect	SCAS#:	Column Address Strobe for
DIR1284:	Direction of 1284		SDRAM
DN (1:2):	USB D-	SCLK:	SDRAM Clock
DP (1:2):	USB D+	SELECT:	Select
DSR#:	Data Set Ready	SELECTIN#:	Select in
DTR#:	Data Terminal Ready	SMI#:	USB System Interrupt
ERROR#:	Error	SRAS#:	Row Address Strobe for
EXCS (0:5)#:	External CS		SDRAM
GND:	Ground	STROBE#:	Strobe
GPIO (0:23):	General Purpose I/O	TXD:	Transmit Data
HOLDAK#:	Hold Acknowledge	UCAS#:	Upper Column Address
HOLDRQ#:	Hold Request		Strobe
IEN:	USB Input Enable	ULCAS#:	Lower Byte of Upper
INIT#:	Initialize		Column Address Strobe
INTRP:	Interrupt	USBINT#:	USB Interrupt
IOCHRDY:	I/O Channel Ready	USBRST#:	USB Reset
IOCS16#:	I/O Chip Select 16	UUCAS#:	Upper Byte of Upper
IOR#:	I/O Read		Column Address Strobe
IOW#:	I/O Write	V_{DD}:	Power Supply Voltage
IRQ:	I/O Request	WAKE:	Wake Up Interrupt
LCAS#:	Lower Column Address Strobe	WR#:	Write
LCDBAK:	LCD Back Light	XIN48M:	Clock In of 48 MHz
LCDCS#:	LCD Chip Select	XOUT48M:	Clock Out of 48 MHz
LCDRDY:	LCD Ready		

Remark # indicates active low.

2.2 List of Pin Functions

2.2.1 System bus interface signals

These signals are used when the VR4121 and SDRAM are connected.

Table 2-1. System Bus Interface Signals (1/2)

Signal Name	I/O	Function
SCLK	I/O	SDRAM operation clock
AD (0:24)	I/O	25-bit address bus
DATA (0:31)	I/O	32-bit data bus
LCDCS#	I	LCD chip select signal. This signal is active when the VR4121 uses the AD bus and DATA bus to perform LCD access.
RD#	I/O	• Output: Active when the VRC4172 accesses SDRAM. • Input: Active when the VR4121 reads data from the PCI host bridge of the VRC4172.
WR#	I/O	• Output: Active when the VRC4172 performs data write to SDRAM. • Input: Active when the VR4121 performs data write to the PCI host bridge of the VRC4172.
LCDRDY	O	LCD ready signal. Active when the VRC4172 is ready to accept access by the VR4121 to the LCD area.
ROMCS (2:3)#	I/O	SDRAM chip select signal
CKE	I/O	SDRAM clock enable signal
UUCAS#	I/O	DQM signal of SDRAM. I/O buffer control signal for DATA (24:31).
ULCAS#	I/O	DQM signal of SDRAM. I/O buffer control signal for DATA (16:23).
MRAS (0:1)#	I/O	SDRAM chip select signal
UCAS#	I/O	DQM signal of SDRAM. I/O buffer control signal for DATA (8:15).
LCAS#	I/O	DQM signal of SDRAM. I/O buffer control signal for DATA (0:7).
IOR#	I	System bus I/O read signal. Active during access of resources other than USB in the VRC4172.
IOW#	I	System bus I/O write signal. Active during access of resources other than USB in the VRC4172.
RESET	I	System bus reset signal
IOCS16#	O	Dynamic bus sizing request signal
IOCHRDY	O	System bus ready signal
HOLDRQ#	O	System bus mastership request signal
HOLDAK#	I	System bus use enable signal
SRAS#	I/O	RAS signal of SDRAM
SCAS#	I/O	CAS signal of SDRAM
BUSRQ (0 :1)#	I	System bus mastership request signal from external bus master
BUSAK (0:1)#	O	System bus use enable signal to external bus master

Table 2-1. System Bus Interface Signals (2/2)

Signal Name	I/O	Function
INTRP	O	Interrupt request signal from 16550 serial controller or IEEE1284 parallel controller
IRQ	O	Interrupt request signal from general-purpose port (GPIO (0:23)) or IEEE1284 parallel controller
USBINT#	O	Interrupt request signal from USB host controller
PS2INT	O	Interrupt request signal from PS/2 controller
BUSCLK	I	System bus clock
ARBCLKSEL	I	Signal that selects the clock for system bus arbitration (HOLDRQ# signal control) (1: Use internal clock, 0: Use BUSCLK)

2.2.2 USB interface signals

Table 2-2. USB Interface Signals

Signal Name	I/O	Function
DP (1:2)	I/O	Positive data signal
DN (1:2)	I/O	Negative data signal
PPON (1:2)	O	USB root hub port power supply control signal
OCI (1:2)	I	USB root hub port overcurrent status signal. Make this signal active when the current that flows through the Vbus line of the USB bus exceeds the reference value.
IEN	I	USB buffer input enable signal. Make this signal active to enable an input signal to the USB port.
WAKE	O	Wakeup interrupt request signal
SMI#	O	System interrupt request signal
USBRST#	I	Reset signal to USB block

2.2.3 IEEE1284 interface signals

Table 2-3. IEEE1284 Interface Signals

Signal Name	I/O	Function
CD (0:7)	I/O	Data signal
STROBE#	I/O	Data strobe signal
ACK#	I/O	Acknowledge signal
BUSY	I/O	Busy signal
PE	I/O	Paper end signal
SELECT	I/O	Select signal
AUTOFEED#	I/O	Autofeed signal
SELECTIN#	I/O	Select input signal
ERROR#	I/O	Fault signal
INIT#	I/O	Initialize signal
DIR1284	O	Transfer direction status output signal

2.2.4 RS-232-C interface signals

These signals are used during data transmit/receive with the VRC4172 and RS-232-C controller.

Table 2-4. RS-232-C Interface Signals

Signal Name	I/O	Function
RXD	I	Receive data signal
CTS#	I	Transmit enable signal
DSR#	I	Data set ready signal
TXD	O	Transmit data signal
RTS#	O	Transmit request signal
DTR#	O	Terminal device ready signal
DCD#	I	Carrier detection signal
RI#	I	Call-in display signal

2.2.5 PS/2 interface signals

Table 2-5. PS/2 Interface Signals

Signal Name	I/O	Function
PS2CLK	I/O	PS/2 clock signal
PS2DATA	I/O	PS/2 data signal

2.2.6 General-purpose port signal

Table 2-6. General-Purpose Port Signal

Signal Name	I/O	Function
GPIO (0:23)	I/O	General-purpose I/O signal

2.2.7 General-purpose chip select signal

Table 2-7. General-Purpose Chip Select Signal

Signal Name	I/O	Function
EXCS (0:5)#	O	General-purpose chip select signal

2.2.8 LCD interface signal

Table 2-8. LCD Interface Signal

Signal Name	I/O	Function
LCDBAK	O	LCD backlight control signal

2.2.9 Clock signals

These signals are used to supply clocks.

Table 2-9. Clock Signals

Signal Name	I/O	Function
XIN48M	I	48 MHz oscillator input pin. One side of a crystal resonator is connected.
XOUT48M	O	48 MHz oscillator output pin. One side of a crystal resonator is connected.
CLKOUT48M	O	48 MHz clock output for FIR of the VR4121

2.3 Pin Statuses

2.3.1 Status of pins under specific conditions

Table 2-10 lists the statuses of pins after the VRC4172 is reset and when HOLDAK# = 1.

Table 2-10. Statuses of Pins Under Specific Conditions (1/2)

Signal Name	After Reset	When HOLDAK# = 1
SCLK	Hi-Z	Hi-Z
AD (0:24)	Hi-Z	Hi-Z
DATA (0:31)	Hi-Z	Hi-Z
LCDCS#	—	—
RD#	Hi-Z	Hi-Z
WR#	Hi-Z	Hi-Z
LCDRDY	Hi-Z	Hi-Z
ROMCS (2:3)#	Hi-Z	Hi-Z
CKE	Hi-Z	Hi-Z
UUCAS#	Hi-Z	Hi-Z
ULCAS#	Hi-Z	Hi-Z
MRAS (0:1)#	Hi-Z	Hi-Z
UCAS#	Hi-Z	Hi-Z
LCAS#	Hi-Z	Hi-Z
IOR#	—	—
IOW#	—	—
RESET	—	—
IOCS16#	Hi-Z	Hi-Z
IOCHRDY	Hi-Z	Hi-Z
HOLDRQ#	1	1
HOLDAK#	—	—
SRAS#	Hi-Z	Hi-Z
SCAS#	Hi-Z	Hi-Z
BUSRQ (0:1)#	—	—
BUSAK (0:1)#	1	Normal operation
INTRP	0	Normal operation
IRQ	0	Normal operation
USBINT#	1	Normal operation
PS2INT	0	Normal operation
BUSCLK	—	—
ARBCLKSEL	—	—
DP (1:2)	1	Normal operation

Remark 0: Low level, 1: High level, Hi-Z: High impedance

Table 2-10. Statuses of Pins Under Specific Conditions (2/2)

Signal Name	After Reset	When HOLDAK# = 1
DN (1:2)	0	Normal operation
PPON (1:2)	0	Normal operation
OCI (1:2)	—	—
IEN	—	—
WAKE	0	Normal operation
SMI#	1	Normal operation
USBRST#	—	—
CD (0:7)	Hi-Z	Normal operation
STROBE#	Hi-Z	Normal operation
ACK#	Hi-Z	Normal operation
BUSY	Hi-Z	Normal operation
PE	Hi-Z	Normal operation
SELECT	Hi-Z	Normal operation
AUTOFEED#	Hi-Z	Normal operation
SELECTIN#	Hi-Z	Normal operation
ERROR#	Hi-Z	Normal operation
INIT#	Hi-Z	Normal operation
DIR1284	0	Normal operation
RXD	—	—
CTS#	—	—
DSR#	—	—
TXD	1	Normal operation
RTS#	1	Normal operation
DTR#	1	Normal operation
DCD#	—	—
RI#	—	—
PS2CLK	0	Normal operation
PS2DATA	Hi-Z	Normal operation
GPIO (0:23)	Hi-Z	Normal operation
EXCS (0:5)#	1	Normal operation
LCDBAK	0	Normal operation
CLKOUT48M	1	Normal operation

Remark 0: Low level, 1: High level, Hi-Z: High impedance

2.3.2 External processing of pins and drive performance

Table 2-11 lists the external processing of pins and their drive performance.

Table 2-11. External Processing of Pins and Drive Performance (1/2)

Signal Name	External Processing	Drive Performance	Withstand Voltage
SCLK	—	80 pF	3 V
AD (0:24)	—	80 pF	3 V
DATA (0:31)	—	80 pF	3 V
LCDCS#	Pull up	—	3 V
RD#	Pull up[Note]	80 pF	3 V
WR#	Pull up[Note]	80 pF	3 V
LCDRDY	Pull up	40 pF	3 V
ROMCS (2:3)#	Pull up	80 pF	3 V
CKE	Pull down	80 pF	3 V
UUCAS#	Pull up[Note]	80 pF	3 V
ULCAS#	Pull up[Note]	80 pF	3 V
MRAS (0:1)#	Pull up[Note]	80 pF	3 V
UCAS#	Pull up[Note]	80 pF	3 V
LCAS#	Pull up[Note]	80 pF	3 V
IOR#	Pull up[Note]	—	3 V
IOW#	Pull up[Note]	—	3 V
RESET	—	—	3 V
IOCS16#	Pull up	40 pF	3 V
IOCHRDY	Pull up	40 pF	3 V
HOLDRQ#	—	40 pF	3 V
HOLDAK#	Pull up	—	3 V
SRAS#	Pull up[Note]	80 pF	3 V
SCAS#	Pull up[Note]	80 pF	3 V
BUSRQ (0:1)#	—	—	3 V
BUSAK (0:1)#	—	40 pF	3 V
INTRP	—	40 pF	3 V
IRQ	—	40 pF	3 V
USBINT#	—	40 pF	3 V
PS2INT	—	40 pF	3 V
BUSCLK	—	—	3 V

Note The same specification as for the VR4121 is used for these pins. If external processing is performed for the VR4121, it does not have to be processed for the VRC4172.

Remark In the case of items for which nothing is specified in the External Processing column (—), external processing does not have to be performed.

Table 2-11. External Processing of Pins and Drive Performance (2/2)

Signal Name	External Processing	Drive Performance	Withstand Voltage
ARBCLKSEL	—	—	3 V
DP (1:2)	—	**Note**	5 V
DN (1:2)	—	**Note**	5 V
PPON (1:2)	—	40 pF	3 V
OCI (1:2)	—	—	3 V
IEN	—	—	3 V
WAKE	—	40 pF	3 V
SMI#	—	40 pF	3 V
USBRST#	—	—	3 V
CD (0:7)	—	40 pF	3 V
STROBE#	Pull up	40 pF	3 V
ACK#	Pull up	40 pF	3 V
BUSY	Pull down	40 pF	3 V
PE	Pull down	40 pF	3 V
SELECT	Pull down	40 pF	3 V
AUTOFEED#	Pull up	40 pF	3 V
SELECTIN#	Pull up	40 pF	3 V
ERROR#	Pull up	40 pF	3 V
INIT#	Pull up	40 pF	3 V
DIR1284	—	40 pF	3 V
RXD	—	—	3 V
CTS#	—	—	3 V
DSR#	—	—	3 V
TXD	—	40 pF	3 V
RTS#	—	40 pF	3 V
DTR#	—	40 pF	3 V
DCD#	—	—	3 V
RI#	—	—	3 V
PS2CLK	Pull up	40 pF	5 V
PS2DATA	Pull up	40 pF	5 V
GPIO (0:23)	Pull up/Pull down	40 pF	3 V
EXCS (0:5)#	—	40 pF	3 V
LCDBAK	—	40 pF	3 V
CLKOUT48M	—	40 pF	3 V

Note Full-speed mode: 50 pF, low-speed mode: 350 pF

Remark In the case of items for which nothing is specified in the External Processing column (—), external processing does not have to be performed.

2.3.3 Recommended connection of unused pins

Table 2-12 shows the recommended connection of unused pins.

Table 2-12. Recommended Connection of Unused Pins

Signal Name	Recommended Connection	Signal Name	Recommended Connection
SCLK	Pull up	PPON (1:2)	Leave open
AD (0:24)	—	OCI (1:2)	Pull down
DATA (0:31)	—	IEN	Pull down
LCDCS#	Pull up	WAKE	Leave open
RD#	Pull up	SMI#	Leave open
WR#	Pull up	USBRST#	Pull down
LCDRDY	Leave open	CD (0:7)	Pull down
ROMCS (2:3)#	Pull up	STROBE#	Pull up
CKE	Pull down	ACK#	Pull up
UUCAS#	Pull up	BUSY	Pull down
ULCAS#	Pull up	PE	Pull down
MRAS (0:1)#	Pull up	SELECT	Pull down
UCAS#	Pull up	AUTOFEED#	Pull up
LCAS#	Pull up	SELECTIN#	Pull up
IOR#	—	ERROR#	Pull up
IOW#	—	INIT#	Pull up
RESET	—	DIR1284	Leave open
IOCS16#	—	RXD	Pull down
IOCHRDY	—	CTS#	Pull up
HOLDRQ#	Leave open	DSR#	Pull up
HOLDAK#	Pull up	TXD	Leave open
SRAS#	Pull up	RTS#	Leave open
SCAS#	Pull up	DTR#	Leave open
BUSRQ (0:1)#	Pull up	DCD#	Pull up
BUSAK (0:1)#	Leave open	RI#	Pull up
INTRP	Leave open	PS2CLK	Pull up
IRQ	Leave open	PS2DATA	Pull up
USBINT#	Leave open	GPIO (0:23)	Pull down
PS2INT	Leave open	EXCS (0:5)#	Leave open
BUSCLK	Pull up	LCDBAK	Leave open
ARBCLKSEL	Pull down	XIN48M	Pull up
DP (1:2)	Pull down	XOUT48M	Leave open
DN (1:2)	Pull down	CLKOUT48M	Leave open

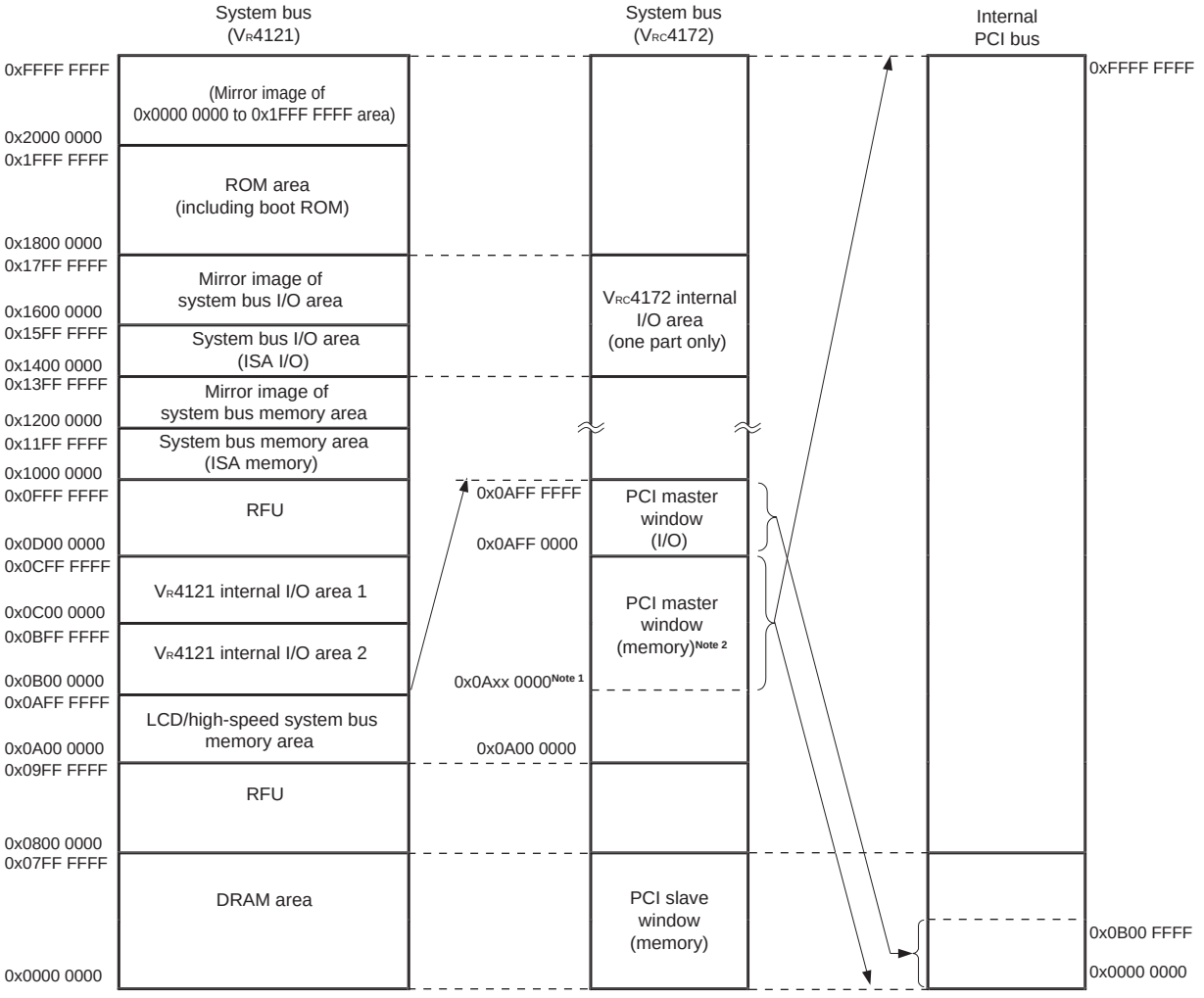
Remark Pins for which nothing is specified (—) are always used.

[MEMO]

CHAPTER 3 ADDRESS MAP

The VR4121 has a 4 GB physical address space. Access to the resources in the VRC4172 is done via the LCD area and the ISA I/O area. The USB host controller in the VRC4172 accesses the DRAM area via the internal PCI bus and the DRAM controller.

Figure 3-1. Physical Address Space



Notes 1. Set the start address with the memory base address register.

2. Perform mapping of the PCI space with the memory base address register.

3.1 Internal I/O Spaces

These spaces are used to access internal I/O resources of the VRC4172 such as the IEEE1284 parallel controller, 16550 serial controller, PS/2 controller, PWM controller, GPIO (general-purpose I/O port), and PCS (programmable chip select). Table 3-1 shows the internal I/O register address spaces.

All these spaces support only 16-bit access.

Table 3-1. Internal I/O Spaces

Physical Address	Internal I/O
0x1500 1080 to 0x1500 108F	GPIO (0:15)
0x1500 1090 to 0x1500 10BF	PCS
0x1500 10C0 to 0x1500 10CF	GPIO (16:23)
0x1500 3800 to 0x1500 380F	PMU, ICU
0x1500 3810 to 0x1500 381F	16550 serial controller
0x1500 3820 to 0x1500 383F	IEEE1284 parallel host controller
0x1500 3840 to 0x1500 385F	RFU
0x1500 3860 to 0x1500 386F	RFU
0x1500 3870 to 0x1500 387F	PS/2 controller
0x1500 3880 to 0x1500 388F	PWM controller

Remark RFU: Reserved for Future Use

3.2 PCI Master Window (Memory)

This space is used to issue memory access and the PCI configuration cycle to the internal PCI bus in the VRC4172.

The address range can be changed, and the start address bits (23:16) are specified with the memory base address register bits (23:16) of the PCI configuration space. The end address is 0x0AFE FFFF.

When this space is accessed, an address whose lower 24 bits are expressed by the lower 24 bits of the system bus address, and whose higher 8 bits are expressed by the memory base address register bits (31:24) is generated, and memory access is issued to the internal PCI bus (except during generation of the PCI configuration cycle).

3.2.1 PCI configuration cycle

The PCI configuration cycle uses the PCI configuration address register (0x0AFF 0CF8) and the PCI configuration data register (0x0AFF 0CFC). The access method is based on PCI configuration cycle mechanism 1.

Table 3-2. PCI Configuration Cycle Registers

Register Address	R/W	Name
0x0AFF 0CF8	R/W	PCI configuration address register
0x0AFF 0CFC	R/W	PCI configuration data register

The details of these registers are shown next.

(1) PCI configuration address register (0x0AFF 0CF8)

(1/2)

Bit Position	31	30	29	28	27	26	25	24
Bit name	Config EN	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R/W	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	23	22	21	20	19	18	17	16
Bit name	Bus Number7	Bus Number6	Bus Number5	Bus Number4	Bus Number3	Bus Number2	Bus Number1	Bus Number0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	15	14	13	12	11	10	9	8
Bit name	Device Number4	Device Number3	Device Number2	Device Number1	Device Number0	Function Number2	Function Number1	Function Number0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	Register Number5	Register Number4	Register Number3	Register Number2	Register Number1	Register Number0	RFU	RFU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
31	Config EN	Configuration cycle enable/disable 1: Enable 0: Disable
30:24	RFU	Reserved. Write 0. 0 returned when read.
23:16	Bus Number (7:0)	Reserved. Write 0. 0 returned when read.
15:11	Device Number (4:0)	Device number 00000: PCI host control register and USB host control configuration register Others: Not used
10:8	Function Number (2:0)	Specification of function number 001: USB host control configuration register 000: PCI host control register Others: Not used

(2/2)

Bit Position	Bit Name	Function
7:2	Register Number (5:0)	Specification of register to be accessed Input the higher 6 bits excluding the lower 2 bits of the register address. For the register addresses, refer to **Table 3-3 PCI Host Control Registers** and **Table 11-1 USB Host Control Configuration Registers**.
1:0	RFU	Reserved. Write 0. 0 returned when read.

This register specifies the PCI configuration cycle enable/disable, device number, function number, and register number of configuration cycle.

(2) PCI configuration data register (0x0AFF 0CFC)

Bit Position	31	30	29	28	27	26	25	24
Bit name	Data31	Data30	Data29	Data28	Data27	Data26	Data25	Data24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	23	22	21	20	19	18	17	16
Bit name	Data23	Data22	Data21	Data20	Data19	Data18	Data17	Data16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	15	14	13	12	11	10	9	8
Bit name	Data15	Data14	Data13	Data12	Data11	Data10	Data9	Data8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	7	6	5	4	3	2	1	0
Bit name	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	Bit Name	Function
31:0	Data (31:0)	Read data from selected register, write data to selected register

3.2.2 PCI host controller

The PCI host controller controls access from the system bus to the USB host controller.

The internal PCI bus is used for access to the USB host controller. For this reason, this controller contains PCI configuration registers (PCI host control registers). Access to the USB host controller is enabled by setting these registers. The PCI configuration cycle registers are used to perform read and write of these registers.

Table 3-3 lists the PCI host control registers.

Table 3-3. PCI Host Control Registers

Offset Address	R/W	Name
0x00	R	Vendor ID register
0x04	R/W	Command register
0x06	R/W	Status register
0x08	R	Revision ID register
0x10 to 12	R/W	Memory base address register
0x50	R/W	Control register

The details of these registers are shown next.

(1) Vendor ID register (offset address: 0x00)

Bit Position	15	14	13	12	11	10	9	8
Bit name	Vender ID15	Vender ID14	Vender ID13	Vender ID12	Vender ID11	Vender ID10	Vender ID9	Vender ID8
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	1	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	Vender ID7	Vender ID6	Vender ID5	Vender ID4	Vender ID3	Vender ID2	Vender ID1	Vender ID0
R/W	R	R	R	R	R	R	R	R
After reset	0	0	1	1	0	0	1	1

Bit Position	Bit Name	Function
15:0	Vender ID (15:0)	Vendor ID 0x1033: NEC

(2) Command register (offset address: 0x04)

Bit Position	15	14	13	12	11	10	9	8
Bit name	PCIRSTGO	PCLKSTOP	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R/W	R/W	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	Memory CycleEN	I/OCycle EN
R/W	R	R	R	R	R	R	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15	PCIRSTGO	A PCI reset pulse is issued at the rising edge of this bit.
14	PCLKSTOP	PCI clock 1: Disable 0: Enable
13:2	RFU	Reserved. Write 0. 0 returned when read.
1	MemoryCycleEN	Memory cycle 1: Enable 0: Disable
0	I/OCycleEN	I/O cycle 1: Enable 0: Disable

(3) Status register (offset address: 0x06)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	Received Master Abort	Received Target Abort	RFU	RFU	RFU	RFU
R/W	R	R	R/W	R/W	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:14	RFU	Reserved. Write 0. 0 returned when read.
13	ReceivedMaster Abort	When this bit is 1, this indicates that the PCI host controller has acknowledged that the master is in the abort status. This bit is cleared by writing 0 to it by software.
12	ReceivedTarget Abort	When this bit is 1, this indicates that the PCI host controller has acknowledged that the target is in the abort status. This bit is cleared by writing 0 to it by software.
11:0	RFU	Reserved. Write 0. 0 returned when read.

(4) Revision ID register (offset address: 0x08)

Bit Position	7	6	5	4	3	2	1	0
Bit name	Revision ID7	Revision ID6	Revision ID5	Revision ID4	Revision ID3	Revision ID2	Revision ID1	Revision ID0
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
★ 7:0	Revision ID (7:0)	Revision ID 0x03: Revision 3 0x00: Revision 1 and 2

(5) Memory base address register (offset address: 0x10 to 12)

Bit Position	31	30	29	28	27	26	25	24
Bit name	MBAR31	MBAR30	MBAR29	MBAR28	MBAR27	MBAR26	MBAR25	MBAR24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	23	22	21	20	19	18	17	16
Bit name	MBAR23	MBAR22	MBAR21	MBAR20	MBAR19	MBAR18	MBAR17	MBAR16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
31:24	MBAR (31:24)	Indicates the higher 8 bits of the PCI memory cycle.
23:16	MBAR (23:16)	Indicates the start address (23:16) of the memory space.
15:0	RFU	Reserved. Write 0. 0 returned when read.

This register sets the start address and the PCI address of the PCI master window (memory). MBAR (31:24) correspond to bits 31 to 24 of the PCI address.

PCI memory address (31:2) = MBAR (31:24) + CPU address (23:2)

MBAR (23:16) sets from where the PCI master window (memory) starts in the LCD space.

(6) Control register (offset address: 0x50)

(1/2)

Bit Position	31	30	29	28	27	26	25	24
Bit name	RFU	SIZE32	SIZE31	SIZE30	RFU	SIZE22	SIZE21	SIZE20
R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	23	22	21	20	19	18	17	16
Bit name	RFU	SIZE12	SIZE11	SIZE10	RFU	SIZE02	SIZE01	SIZE00
R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	PCICLK DIV1	PCICLK DIV0
R/W	R	R	R	R	R	R	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	EXTM64	M64SEL
R/W	R	R	R	R	R	R	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
31	RFU	Reserved. Write 0. 0 returned when read.
30:28	SIZE3 (2:0)	DRAM size of Bank3. Same value as SIZE3 (2:0) of RAMSIZEREG register of VR4121.
27	RFU	Reserved. Write 0. 0 returned when read.
26:24	SIZE2 (2:0)	DRAM size of Bank2. Same value as SIZE2 (2:0) of RAMSIZEREG register of VR4121.
23	RFU	Reserved. Write 0. 0 returned when read.
22:20	SIZE1 (2:0)	DRAM size of Bank1. Same value as SIZE1 (2:0) of RAMSIZEREG register of VR4121.
19	RFU	Reserved. Write 0. 0 returned when read.
18:16	SIZE0 (2:0)	DRAM size of Bank0. Same value as SIZE0 (2:0) of RAMSIZEREG register of VR4121.
15:10	RFU	Reserved. Write 0. 0 returned when read.

(2/2)

Bit Position	Bit Name	Function
9:8	PCICLKDIV (1:0)	PCI clock divide ratio 11: RFU 10: 48 MHz/1.5 01: 48 MHz/2 00: 48 MHz/3
7:2	RFU	Reserved. Write 0. 0 returned when read.
1	EXTM64	Same value as EXT_DRAM64 bit of BCUCNTREG3 register of VR4121.
0	M64SEL	Same value as DRAM64 bit of BCUCNTREG1 register of VR4121.

3.3 PCI Master Window (I/O)

This space is used to issue I/O access to the internal PCI bus in the VRC4172.

The address range is fixed to the 64 KB area from 0x0AFF0000 to 0x0AFF FFFF.

When this space is accessed, an address consisting of the lower 16 bits of the system bus address padded with 0s to form a 32-bit address is generated and I/O access is issued to the internal PCI bus.

3.4 PCI Slave Window (Memory)

When the PCI memory cycle address issued by the USB host controller is in this space, the VRC4172 performs access to SDRAM. The addresses on the internal PCI bus are used as is as the addresses for SDRAM.

CHAPTER 4 GPIO (GENERAL-PURPOSE I/O PORT)

GPIO controls the GPIO pins. The GPIO pins are 24 general-purpose ports that support both input and output. Interrupt request signal input functions can be allocated to these ports, and 5 triggers can be selected: input signal changes (rising edge, falling edge, both edges), low level, and high level. Notification is done via the IRQ pin.

When these pins are not used as interrupt requests, a low-level or high-level signal can be output by writing to the register corresponding to each pin. Moreover, the status of the signal input to each pin can be known by reading the contents of the corresponding register.

4.1 Register Set

Table 4-1 lists the GPIO registers.

Table 4-1. GPIO Registers

Address	R/W	Symbol	Function
0x1500 1080	R/W	EXGPDATA0	GPIO (15:0) I/O data register
0x1500 1082	R/W	EXGPDIR0	GPIO (15:0) I/O setting register
0x1500 1084	R/W	EXGPINTEN0	GPIO (15:0) interrupt enable register
0x1500 1086	R/W	EXGPINTST0	GPIO (15:0) interrupt register
0x1500 1088	R/W	EXGPINTTYP0	GPIO (15:0) interrupt trigger register
0x1500 108A	R/W	EXGPINTLV0L	GPIO (15:0) interrupt level setting lower register
0x1500 108C	R/W	EXGPINTLV0H	GPIO (15:0) interrupt level setting higher register
0x1500 10C0	R/W	EXGPDATA1	GPIO (23:16) I/O data register
0x1500 10C2	R/W	EXGPDIR1	GPIO (23:16) I/O setting register
0x1500 10C4	R/W	EXGPINTEN1	GPIO (23:16) interrupt enable register
0x1500 10C6	R/W	EXGPINTST1	GPIO (23:16) interrupt register
0x1500 10C8	R/W	EXGPINTTYP1	GPIO (23:16) interrupt trigger register
0x1500 10CA	R/W	EXGPINTLV1L	GPIO (23:16) interrupt level setting lower register

The details of these registers are shown next.

4.1.1 EXGPDATA0 (0x1500 1080)

Bit Position	15	14	13	12	11	10	9	8
Bit name	EXPD15	EXPD14	EXPD13	EXPD12	EXPD11	EXPD10	EXPD9	EXPD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	EXPD7	EXPD6	EXPD5	EXPD4	EXPD3	EXPD2	EXPD1	EXPD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:0	EXPD (15:0)	Specification of GPIO (15:0) pin output data 1: High level 0: Low level

This register reads/writes the data of the GPIO (15:0) pins. One bit corresponds to one pin.

When the EXPDR bit corresponding to the EXGPDIR0 register is set to 1, the data written to the EXPD bit is output to the corresponding GPIO pin. When the EXPDR bit is set to 0, writing a value to the EXPD bit has no influence on the GPIO pin (the write data is ignored).

Moreover, when the EXPD bit is read when the EXPDR bit is 0, the status of the corresponding GPIO pin is read.

4.1.2 EXGPDIR0 (0x1500 1082)

Bit Position	15	14	13	12	11	10	9	8
Bit name	EXPDR15	EXPDR14	EXPDR13	EXPDR12	EXPDR11	EXPDR10	EXPDR9	EXPDR8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	EXPDR7	EXPDR6	EXPDR5	EXPDR4	EXPDR3	EXPDR2	EXPDR1	EXPDR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:0	EXPDR (15:0)	Selection of GPIO (15:0) pin input/output 1: Output 0: Input

This register sets input/output for the GPIO (15:0) pins. One bit corresponds to one pin.

When an EXPDR bit is set to 1, the corresponding GPIO pin is set to output, and the value written to the EXPD bit corresponding to the EXGPDATA0 register is output. When an EXPDR bit is set to 0, the status of the corresponding GPIO pin is set to input.

4.1.3 EXGPINTEN0 (0x1500 1084)

Bit Position	15	14	13	12	11	10	9	8
Bit name	EXPIE15	EXPIE14	EXPIE13	EXPIE12	EXPIE11	EXPIE10	EXPIE9	EXPIE8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	EXPIE7	EXPIE6	EXPIE5	EXPIE4	EXPIE3	EXPIE2	EXPIE1	EXPIE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:0	EXPIE (15:0)	Enable detection of interrupts to GPIO (15:0) pins 1: Enable 0: Disable

This register enables/disables the detection of interrupts to GPIO (15:0) pins. One bit corresponds to one pin. When an EXPIE bit is set to 1, the detection of interrupts to the corresponding GPIO pin is enabled.

4.1.4 EXGPINTST0 (0x1500 1086)

Bit Position	15	14	13	12	11	10	9	8
Bit name	EXPIS15	EXPIS14	EXPIS13	EXPIS12	EXPIS11	EXPIS10	EXPIS9	EXPIS8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	EXPIS7	EXPIS6	EXPIS5	EXPIS4	EXPIS3	EXPIS2	EXPIS1	EXPIS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:0	EXPIS (15:0)	Interrupt request to GPIO (15:0) pins During read / During write 1: Interrupt occurred / Interrupt clear 0: No interrupt occurred / Clear cancellation

This register indicates the occurrence of an interrupt request to the GPIO (15:0) pins. One bit corresponds to one pin.

When a signal input to a GPIO pin satisfies the conditions set by the EXGPINTTYP0 register, EXGPINTLV0L register, and EXGPINTLV0H register, the corresponding EXPIS bit is set to 1. However, if the bit corresponding to the EXGPINTEN0 register is set to 0 (interrupt disabled), no interrupt is generated (the EXPIS bit is not set to 1).

Remark After 1 is written to clear the interrupt, write 0 for clear cancellation.
Interrupt clear is valid only during edge detection. During level detection, the register is cleared when the interrupt source signal becomes inactive.

4.1.5 EXGPINTTYP0 (0x1500 1088)

Bit Position	15	14	13	12	11	10	9	8
Bit name	EXPIT15	EXPIT14	EXPIT13	EXPIT12	EXPIT11	EXPIT10	EXPIT9	EXPIT8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	EXPIT7	EXPIT6	EXPIT5	EXPIT4	EXPIT3	EXPIT2	EXPIT1	EXPIT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:0	EXPIT (15:0)	Interrupt request detection trigger for GPIO (15:0) pins 1: Edge 0: Level

This register sets the trigger for detecting interrupt requests to the GPIO (15:0) pins. One bit corresponds to one pin.

When an EXPIT bit is set to 1, the change of the interrupt request signal for the corresponding GPIO pin from high level to low level, or from low level to high level, is detected as an interrupt request.

When an EXPIT bit is set to 0, an interrupt request is detected when the level set to the corresponding EXPIL bit of the EXGPINTLV0L register or EXGPINTLV0H register is reached.

4.1.6 EXGPINTLV0L (0x1500 108A)

Bit Position	15	14	13	12	11	10	9	8
Bit name	EXPIB7	EXPIB6	EXPIB5	EXPIB4	EXPIB3	EXPIB2	EXPIB1	EXPIB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	EXPIL7	EXPIL6	EXPIL5	EXPIL4	EXPIL3	EXPIL2	EXPIL1	EXPIL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:8	EXPIB (7:0)	Interrupt request detection level 1 for GPIO (7:0) pins 1: Enable detection of both edges 0: Disable detection of both edges
7:0	EXPIL (7:0)	Interrupt request detection level 2 for GPIO (7:0) pins During level detection / During edge detection 1: High level / Rising edge 0: Low level / Falling edge

This register sets the level for detecting interrupt requests to the GPIO (7:0) pins.

The EXPIB bit is enabled only when the edge trigger is selected with the EXGPINTTYP0 register. When the level trigger is selected, the EXPIB bit has no meaning.

When the EXPIB bit is 1, the EXPIL bit has no meaning.

4.1.7 EXGPINTLV0H (0x1500 108C)

Bit Position	15	14	13	12	11	10	9	8
Bit name	EXPIB15	EXPIB14	EXPIB13	EXPIB12	EXPIB11	EXPIB10	EXPIB9	EXPIB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	EXPIL15	EXPIL14	EXPIL13	EXPIL12	EXPIL11	EXPIL10	EXPIL9	EXPIL8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:8	EXPIB (15:8)	Interrupt request detection level 1 for GPIO (15:8) pins 1: Enable detection of both edges 0: Disable detection of both edges
7:0	EXPIL (15:8)	Interrupt request detection level 2 for GPIO (15:8) pins During level detection / During edge detection 1: High level / Rising edge 0: Low level / Falling edge

This register sets the level for detecting interrupt requests to the GPIO (15:8) pins.

The EXPIB bit is enabled only when the edge trigger is selected with the EXGPINTTYP0 register. When the level trigger is selected, the EXPIB bit has no meaning.

When the EXPIB bit is 1, the EXPIL bit has no meaning.

4.1.8 EXGPDATA1 (0x1500 10C0)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	EXPD23	EXPD22	EXPD21	EXPD20	EXPD19	EXPD18	EXPD17	EXPD16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7:0	EXPD (23:16)	Specification of GPIO (23:16) pin output data 1: High level 0: Low level

This register reads/writes the data of the GPIO (23:16) pins. One bit corresponds to one pin.

When the EXPDR bit corresponding to the EXGPDIR1 register is set to 1, the data written to the EXPD bit is output to the corresponding GPIO pin. When the EXPDR bit is set to 0, writing a value to the EXPD bit has no influence on the GPIO pins (the write data is ignored).

Moreover, when the EXPD bit is read when the EXPDR bit is 0, the status of the corresponding GPIO pin is read.

4.1.9 EXGPDIR1 (0x1500 10C2)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	EXPDR7	EXPDR6	EXPDR5	EXPDR4	EXPDR3	EXPDR2	EXPDR1	EXPDR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7:0	EXPDR (7:0)	Selection of GPIO (23:16) pin input/output 1: Output 0: Input

This register sets input/output for the GPIO (23:16) pins. One bit corresponds to one pin.

When an EXPDR bit is set to 1, the corresponding GPIO pin is set to output, and the value written to the EXPD bit corresponding to the EXGPDATA1 register is output. When an EXPDR bit is set to 0, the status of the corresponding GPIO pin is set to input.

4.1.10 EXGPINTEN1 (0x1500 10C4)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	EXPIE23	EXPIE22	EXPIE21	EXPIE20	EXPIE19	EXPIE18	EXPIE17	EXPIE16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7:0	EXPIE (23:16)	Enable detection of interrupts to GPIO (23:16) pins 1: Enable 0: Disable

This register enables/disables the detection of interrupts to GPIO (23:16) pins. One bit corresponds to one pin. When an EXPIE bit is set to 1, the detection of interrupts to the corresponding GPIO pin is enabled.

4.1.11 EXGPINTST1 (0x1500 10C6)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	EXPIS23	EXPIS22	EXPIS21	EXPIS20	EXPIS19	EXPIS18	EXPIS17	EXPIS16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7:0	EXPIS (23:16)	Interrupt request to GPIO (23:16) pins During read / During write 1: Interrupt occurred / Interrupt clear 0: No interrupt occurred / Clear cancellation

This register indicates the occurrence of an interrupt request to the GPIO (23:16) pins. One bit corresponds to one pin.

When a signal input to a GPIO pin satisfies the conditions set by the EXGPINTTYP1 register and the EXGPINTLV1L register, the corresponding EXPIS bit is set to 1. However, if the bit corresponding to the EXGPINTEN1 register is set to 0 (interrupt disabled), no interrupt is generated (the EXPIS bit is not set to 1).

Remark After 1 is written to clear the interrupt, write 0 for clear cancellation.
Interrupt clear is valid only during edge detection. During level detection, the register is cleared when the interrupt source signal becomes inactive.

4.1.12 EXGPINTTYP1 (0x1500 10C8)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	EXPIT23	EXPIT22	EXPIT21	EXPIT20	EXPIT19	EXPIT18	EXPIT17	EXPIT16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7:0	EXPIT (23:16)	Interrupt request detection trigger for GPIO (23:16) pins 1: Edge 0: Level

This register sets the trigger for detecting interrupt requests to the GPIO (23:16) pins. One bit corresponds to one pin.

When an EXPIT bit is set to 1, the change of the interrupt request signal for the corresponding GPIO pin from high level to low level, or from low level to high level, is detected as an interrupt request.

When an EXPIT bit is set to 0, an interrupt request is detected when the level set to the corresponding EXPIL bit of the EXGPINTLV1L register is reached.

4.1.13 EXGPINTLV1L (0x1500 10CA)

Bit Position	15	14	13	12	11	10	9	8
Bit name	EXPIB23	EXPIB22	EXPIB21	EXPIB20	EXPIB19	EXPIB18	EXPIB17	EXPIB16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	EXPIL23	EXPIL22	EXPIL21	EXPIL20	EXPIL19	EXPIL18	EXPIL17	EXPIL16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:8	EXPIB (23:16)	Interrupt request detection level 1 for GPIO (23:16) pins 1: Enable detection of both edges 0: Disable detection of both edges
7:0	EXPIL (23:16)	Interrupt request detection level 2 for GPIO (23:16) pins During level detection / During edge detection 1: High level / Rising edge 0: Low level / Falling edge

This register sets the level for detecting interrupt requests to the GPIO (23:16) pins.

The EXPIB bit is enabled only when the edge trigger is selected with the EXGPINTTYP1 register. When the level trigger is selected, the EXPIB bit has no meaning.

When the EXPIB bit is 1, the EXPIL bit has no meaning.

CHAPTER 5 PCS (PROGRAMMABLE CHIP SELECT)

PCS compares the addresses set to the register with the addresses on the system bus and generates the EXCS (5:0)# signals. The EXCS (5:0)# signals are low level when the addresses match. There are 6 EXCS (5:0)# signals, and the addresses to be compared can freely be set for each.

5.1 Register Set

Table 5-1 lists the PCS registers.

Table 5-1. PCS Registers

Address	R/W	Symbol	Function
0x1500 1090	R/W	EXCS0SELL	EXCS0# compare address lower register
0x1500 1092	R/W	EXCS0SELH	EXCS0# compare address higher register
0x1500 1094	R/W	EXCS0MSKL	EXCS0# compare address mask lower & enable register
0x1500 1096	R/W	EXCS0MSKH	EXCS0# compare address mask higher register
0x1500 1098	R/W	EXCS1SELL	EXCS1# compare address lower register
0x1500 109A	R/W	EXCS1SELH	EXCS1# compare address higher register
0x1500 109C	R/W	EXCS1MSKL	EXCS1# compare address mask lower & enable register
0x1500 109E	R/W	EXCS1MSKH	EXCS1# compare address mask higher register
0x1500 10A0	R/W	EXCS2SELL	EXCS2# compare address lower register
0x1500 10A2	R/W	EXCS2SELH	EXCS2# compare address higher register
0x1500 10A4	R/W	EXCS2MSKL	EXCS2# compare address mask lower & enable register
0x1500 10A6	R/W	EXCS2MSKH	EXCS2# compare address mask higher register
0x1500 10A8	R/W	EXCS3SELL	EXCS3# compare address lower register
0x1500 10AA	R/W	EXCS3SELH	EXCS3# compare address higher register
0x1500 10AC	R/W	EXCS3MSKL	EXCS3# compare address mask lower & enable register
0x1500 10AE	R/W	EXCS3MSKH	EXCS3# compare address mask higher register
0x1500 10B0	R/W	EXCS4SELL	EXCS4# compare address lower register
0x1500 10B2	R/W	EXCS4SELH	EXCS4# compare address higher register
0x1500 10B4	R/W	EXCS4MSKL	EXCS4# compare address mask lower & enable register
0x1500 10B6	R/W	EXCS4MSKH	EXCS4# compare address mask higher register
0x1500 10B8	R/W	EXCS5SELL	EXCS5# compare address lower register
0x1500 10BA	R/W	EXCS5SELH	EXCS5# compare address higher register
0x1500 10BC	R/W	EXCS5MSKL	EXCS5# compare address mask lower & enable register
0x1500 10BE	R/W	EXCS5MSKH	EXCS5# compare address mask higher register

The details of these registers are shown next.

5.1.1 EXCS compare address registers

(1) EXCSnSELL (0x1500 1090, 1098, 10A0, 10A8, 10B0, 10B8)

Bit Position	15	14	13	12	11	10	9	8
Bit name	CSnA15	CSnA14	CSnA13	CSnA12	CSnA11	CSnA10	CSnA9	CSnA8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	CSnA7	CSnA6	CSnA5	CSnA4	CSnA3	CSnA2	CSnA1	RFU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:1	CSnA (15:1)	Lower bits of decode address for EXCS (5:0)# pins
0	RFU	Reserved. Write 0. 0 returned when read.

(2) EXCSnSELH (0x1500 1092, 109A, 10A2, 10AA, 10B2, 10BA)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	CSnA24
R/W	R	R	R	R	R	R	R	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	CSnA23	CSnA22	CSnA21	CSnA20	CSnA19	CSnA18	CSnA17	CSnA16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:9	RFU	Reserved. Write 0. 0 returned when read.
8:0	CSnA (24:16)	Higher bits of decode address for EXCS (5:0)# pins

These registers set the decode addresses for the EXCS (5:0)# pins.

The EXCS (5:0)# pins output active-low signals by decoding ISA bus addresses based on the register set value.

Remarks 1. n = 0 to 5

2. The correspondence between the EXCS (5:0)# pins and their registers is shown in the following table.

Pin Name	EXCSnSELL	EXCSnSELH
EXCS0#	EXCS0SELL (0x1500 1090)	EXCS0SELH (0x1500 1092)
EXCS1#	EXCS1SELL (0x1500 1098)	EXCS1SELH (0x1500 109A)
EXCS2#	EXCS2SELL (0x1500 10A0)	EXCS2SELH (0x1500 10A2)
EXCS3#	EXCS3SELL (0x1500 10A8)	EXCS3SELH (0x1500 10AA)
EXCS4#	EXCS4SELL (0x1500 10B0)	EXCS4SELH (0x1500 10B2)
EXCS5#	EXCS5SELL (0x1500 10B8)	EXCS5SELH (0x1500 10BA)

5.1.2 EXCS address mask registers

(1) EXCSnMSKL (0x1500 1094, 109C, 10A4, 10AC, 10B4, 10BC)

Bit Position	15	14	13	12	11	10	9	8
Bit name	CSnM15	CSnM14	CSnM13	CSnM12	CSnM11	CSnM10	CSnM9	CSnM8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	CSnM7	CSnM6	CSnM5	CSnM4	CSnM3	CSnM2	CSnM1	CSnEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:1	CSnM (15:1)	Mask lower bits of decode address for EXCS (5:0)# pins
0	CSnEN	Control of output to EXCS (5:0)# pins 1: Output compare result 0: Output high level regardless of compare result

(2) EXCSnMSKH (0x1500 1096, 109E, 10A6, 10AE, 10B6, 10BE)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	CSnM24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	CSnM23	CSnM22	CSnM21	CSnM20	CSnM19	CSnM18	CSnM17	CSnM16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:9	RFU	Reserved. Write 0. 0 returned when read.
8:0	CSnM (24:16)	Mask higher bits of decode address for EXCS (5:0)# pins

These registers set the decode address range for the EXCS (5:0)# pins.

When the values set with the EXCSnSELH register and the EXCSnSELL register are compared, the bits set to 1 with these registers are excluded from the decode conditions.

Output enable/disable can be set for the EXCSn# pin with the CSnEN bit of the EXCSnMSKL register.

Remarks 1. n = 0 to 5

2. The correspondence between the EXCS (5:0)# pins and their registers is shown in the following table.

Pin Name	EXCSnMSKL	EXCSnMSKH
EXCS0#	EXCS0MSKL (0x1500 1094)	EXCS0MSKH (0x1500 1096)
EXCS1#	EXCS1MSKL (0x1500 109C)	EXCS1MSKH (0x1500 109E)
EXCS2#	EXCS2MSKL (0x1500 10A4)	EXCS2MSKH (0x1500 10A6)
EXCS3#	EXCS3MSKL (0x1500 10AC)	EXCS3MSKH (0x1500 10AE)
EXCS4#	EXCS4MSKL (0x1500 10B4)	EXCS4MSKH (0x1500 10B6)
EXCS5#	EXCS5MSKL (0x1500 10BC)	EXCS5MSKH (0x1500 10BE)

[MEMO]

CHAPTER 6 PWM CONTROLLER

The PWM controller controls the frequency and duty of the LCD backlight modulation pulse.

6.1 Register Set

Table 6-1 lists the PWM registers.

Table 6-1. PWM Registers

Address	R/W	Symbol	Function
0x1500 3880	R/W	LCDDUTYEN	LCDBAK enable register
0x1500 3882	R/W	LCDFREQ	LCDBAK frequency register
0x1500 3884	R/W	LCDDUTY	LCDBAK duty register

The details of these registers are shown next.

6.1.1 LCDDUTYEN (0x1500 3880)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	LCDEN
R/W	R	R	R	R	R	R	R	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:1	RFU	Reserved. Write 0. 0 returned when read.
0	LCDEN	LCDBAK signal control enable 1: Enable 0: Disable

This register enables/disables duty control.

When the LCDEN bit is set to 0, the LCDBAK signal outputs a low level.

6.1.2 LCDFREQ (0x1500 3882)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	1	1	1	1	1	1	1	1

Bit Position	7	6	5	4	3	2	1	0
Bit name	FREQD7	FREQD6	FREQD5	FREQD4	FREQD3	FREQD2	FREQD1	FREQD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	1	1	1	1	1	1	1	1

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 1. 1 returned when read.
7:0	FREQD (7:0)	LCDBAK signal frequency setting

This register sets the frequency of the LCDBAK signal.

The frequency can be set between 30.5 Hz and 7812.5 Hz.

The frequency of the LCDBAK signal is expressed with the following equation.

$$T_1 = \frac{2^4}{8 \times 10^6\ [\mathrm{Hz}]} \times 64 \times (\mathrm{FREQD}\ (7:0) + 1)\ [\mathrm{s}]$$

$$f = \frac{1}{T_1}\ [\mathrm{Hz}]$$

Remarks f: LCDBAK signal frequency

T_1: Cycle of generated waveform

6.1.3 LCDDUTY (0x1500 3884)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RFU	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:6	RFU	Reserved. Write 0. 0 returned when read.
5:0	DUTY (5:0)	LCDBAK signal duty setting (high-level width)

This register sets the LCDBAK signal duty (high-level width).

If a duty of 0% is selected, set the LDCEN bit of the LCDDUTYEN register to 0.

The high-level width (T_2) is expressed with the following equation.

$$T_2 = \frac{T_1}{64} \times (\text{DUTY (5:0)} + 1)\ [s]$$

Remarks T_2: High-level width of LCDBAK signal

T_1: Cycle of generated waveform

CHAPTER 7 PMU (POWER MANAGEMENT UNIT)

The PMU controls the clock supply and reset for the IEEE1284 parallel controller, 16550 serial controller, PS/2 controller, PWM controller, and USB host controller. It also performs enable/disable settings for the internal oscillator (48 MHz).

7.1 Register Set

Table 7-1 lists the PMU registers.

Table 7-1. PMU Registers

Address	R/W	Symbol	Function
0x1500 3800	R/W	SYSCLKCTRL	SYSCLK enable register
0x1500 3802	R/W	1284CTRL	1284 parallel clock/reset control register
0x1500 3804	R/W	16550CTRL	16550 serial clock/reset control register
0x1500 380C	R/W	USBCTRL	USB clock control register
0x1500 380E	R/W	PS2PWMCTRL	PS/2, PWM clock/reset control register

The details of these registers are shown next.

7.1.1 SYSCLKCTRL (0x1500 3800)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RFU	IRST	OSCEN	RFU	RFU	RFU	CKO48
R/W	R	R	R/W	R/W	R	R	R	R/W
After reset	0	0	1	0	0	0	0	1

Bit Position	Bit Name	Function
15:6	RFU	Reserved. Write 0. 0 returned when read.
5	IRST	Internal reset control 1: Reset start 0: Reset cancel
4	OSCEN	Setting of enable/disable of 48 MHz internal oscillator 1: Disable (clock stopped) 0: Enable
3:1	RFU	Reserved. Write 0. 0 returned when read.
0	CKO48	Output control of CLKOUT48M signal 1. Do not output 48 MHz clock 0: Output 48 MHz clock

This register enables/disables the 48 MHz internal oscillator which supplies the system clock of the VRC4172 and controls the 48 MHz clock output for FIR.

When the IRST bit is 1, registers, except this register and the PCI host controller, PCI configuration address register, and PCI configuration data register, are reset. Reset is cancelled by writing 0 to the IRST bit.

When the OSCEN bit is 0, the oscillator outputs a clock. When the OSCEN bit is 1, low level is output. When changing the OSCEN bit, first set the IRST bit to 1.

When the CKO48 bit is 0, a 48 MHz clock is output to the CLKOUT48M signal. When the CKO48 bit is 1, a high-level signal is always output.

This register is reset only when the RESET signal is 1.

7.1.2 1284CTRL (0x1500 3802)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RFU	RFU	RFU	RFU	1284USE	1284RST	1284CLK
R/W	R	R	R	R	R	R/W	R/W	R/W
After reset	0	0	0	0	0	0	1	1

Bit Position	Bit Name	Function
15:3	RFU	Reserved. Write 0. 0 returned when read.
2	1284USE	Use of IEEE1284 parallel controller 1: Use 0: Do not use
1	1284RST	Reset of IEEE1284 parallel controller 1: Reset start 0: Reset cancel
0	1284CLK	Control of clock to IEEE1284 parallel controller 1. Do not supply clock 0: Supply clock

This register enables use of the IEEE1284 parallel controller and controls reset and clock supply.
To use the IEEE1284 parallel controller, set the 128USE bit to 1 and always keep it fixed to 1 during use.

Remark Reset the IEEE1284 parallel controller using the following procedure.

1. Set the 1284CTRL register to 0x0006.
2. Wait 1 μs.
3. Set the 1284CTRL register to 0x0004.

7.1.3 16550CTRL (0x1500 3804)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	SIORST	SIOCLK
R/W	R	R	R	R	R	R	R/W	R/W
After reset	0	0	0	0	0	0	1	1

Bit Position	Bit Name	Function
15:2	RFU	Reserved. Write 0. 0 returned when read.
1	SIORST	Reset of 16550 serial controller 1: Reset start 0: Reset cancel
0	SIOCLK	Control of clock to 16550 serial controller 1. Do not supply clock 0: Supply clock

This register controls reset and clock supply to the 16550 serial controller.

Remark Reset the 16550 serial controller using the following procedure.

1. Set the 16550CTRL register to 0x0002.
2. Wait 200 ms.
3. Set the 16650CTRL register to 0x0000.

7.1.4 USBCTRL (0x1500 380C)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	USBCLK
R/W	R	R	R	R	R	R	R	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:1	RFU	Reserved. Write 0. 0 returned when read.
0	USBCLK	Control of clock to USB host controller 1. Do not supply clock 0: Supply clock

This register controls the clock supply to the USB host controller.

The USBCLK bit is valid when the OSCEN bit of the SYSCLKCTRL register is 0. When the OSCEN bit of the SYSCLKCTRL register is 1, the clock is not supplied regardless of the value of the USBCLK bit.

It is recommended to set the USBRST# pin to 0 when changing the value of the USBCLK bit.

After changing the value of the USBCLK bit from 1 to 0, be sure to input 0 to the USBRST# pin.

7.1.5 PS2PWMCTRL (0x1500 380E)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RFU	RFU	PWMCLK	RFU	RFU	PS2RST	PS2CLK
R/W	R	R	R	R/W	R	R	R/W	R/W
After reset	0	0	0	1	0	0	1	1

Bit Position	Bit Name	Function
15:5	RFU	Reserved. Write 0. 0 returned when read.
4	PWMCLK	PWM clock control 1. Do not supply clock 0: Supply clock
3:2	RFU	Reserved. Write 0. 0 returned when read.
1	PS2RST	Reset of PS/2 controller 1. Reset start 0: Reset cancel
0	PS2CLK	PS/2 controller clock control 1. Do not supply clock 0: Supply clock

This register controls PS/2 controller reset, and clock supply to the PS/2 controller and PWM controller.
For the PS/2 controller, perform clock supply and then reset cancel in this order (wait is not required).

7.2 Clock Supply

Next, the clock supply procedure is described.

(1) At power-on

1. Input 0 to the RESET pin while the RESET signal is high level and the USBRST# signal is low level (reset cancel).
2. Set the OSCEN bit of the SYSCLKCTRL register to 0 (clock supply start).
3. Set the IRST bit of the SYSCLKCTRL register to 0.
4. Input the USBRST# pin to 1 (USBRST# signal cancel).

(2) Stop 48 MHz clock supply → Resume supply

(a) During normal time

<1> Stop supply

1. Set the IRST bit of the SYSCLKCTRL register to 1 and input 0 to the USBRST# pin.
2. Set the OSCEN bit of the SYSCLKCTRL register to 1 (clock supply stop).

<2> Resume supply

1. Set the OSCEN bit of the SYSCLKCTRL register to 0 (clock supply stop).
2. Set the IRST bit of the SYSCLKCTRL register to 0 (internal reset cancel) and input 1 to the USBRST# pin (USBRST# signal cancel).

(b) While GPIO, PCS register information is held

<1> Stop supply

1. Set the 1284RST bit and the 1284CLK bit of the 1284CTRL register to 1.
   Set the SIORST bit and the SIOCLK bit of the 16550CTRL register to 1.
   Set the PWMCLK bit, the PS2RST bit, and the PS2CLK bit of the PS2PWMCTRL register to 1.
   Input 0 to the USBRST# pin (USBRST# signal start).
2. Set the USBCLK bit of the USBCTRL register to 1.
3. Set the OSCEN bit of the SYSCLKCTRL register to 1 (clock supply stop).

<2> Resume supply

1. Set the OSCEN bit of the SYSCLKCTRL register to 0 (clock supply start).
2. Set the USBCLK bit of the USBCTRL register to 0.
3. Input 1 to the USBRST# pin (USBRST# signal cancel).
   If needed, set again the 1284CTRL register, 16550CTRL register, and PS2PWMCTRL register, supply the clock to each unit, and perform reset cancel (for the setting method, refer to the sections describing each register).

If 1 is input to the ARBCLKSEL pin and the internal clock (48 MHz clock divided by 6) is used for system bus arbitration, the arbitration function is also stopped when the 48 MHz clock is stopped. When 0 is input to the BUSRQ (0:1)# pins immediately before the 48 MHz clock is stopped, the VRC4172 sets the HOLDRQ# signal to 0 and requests the bus to the VR4121. The VR4121 receives the HOLDRQ# signal, sets the HOLDAK# signal to 0, and passes the bus to the VRC4172, but since the arbitration function of the VRC4172 is stopped at this time, the operation stops at this point. To prevent this, fix the BUSRQ (0:1)# pins to 1 before stopping the 48 MHz clock, or input 0 to the ARBCLKSEL pin to select arbitration that uses an external clock.

CHAPTER 8 ICU (INTERRUPT CONTROL UNIT)

The ICU controls interrupts to the IEEE1284 parallel controller and the 16550 serial controller.

For details on the GPIO interrupts, refer to **CHAPTER 4 GPIO (GENERAL-PURPOSE I/O PORT**), and for details on the USB interrupts, refer to **CHAPTER 11 USB HOST CONTROLLER**.

8.1 Register Set

Table 8-1 lists the ICU registers.

Table 8-1. ICU Registers

Address	R/W	Symbol	Function
0x1500 3808	R/W	1284INTRQ	IEEE1284 parallel controller interrupt control register
0x1500 380A	R/W	16550INTRQ	16550 serial controller interrupt control register

The details of these registers are shown next.

8.1.1 1284INTRQ (0x1500 3808)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RFU	RFU	RFU	MASK3	MASK2	THRU	LATCH
R/W	R	R	R	R	R/W	R/W	R	R/W
After reset	0	0	0	0	0	0	Undefined	0

Bit Position	Bit Name	Function
15:4	RFU	Reserved. Write 0. 0 returned when read.
3	MASK3	Interrupt mask (IRQ pin) 1: Output interrupt to IRQ pin. 0: Do not output interrupt to IRQ pin.
2	MASK2	Interrupt mask (INTRP pin) 1: Output interrupt to INTRP pin. 0: Do not output interrupt to INTRP pin.
1	THRU	Interrupt status (through, read only) 1: Interrupt occurrence 0: No interrupt
0	LATCH	Interrupt status (latch) During read / During write 1: Interrupt occurrence / Interrupt clear 0: No interrupt / No change

This register controls interrupt output to the IEEE1284 parallel controller.

The THRU bit can read the interrupt output status for the IEEE1284 parallel controller as is.

The LATCH bit is held until the interrupt output for the IEEE1284 parallel controller is cleared by software. This bit is cleared to 0 by writing 1 to it.

8.1.2 16550INTRQ (0x1500 380A)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	THRU	LATCH
R/W	R	R	R	R	R	R	R	R/W
After reset	0	0	0	0	0	0	Undefined	0

Bit Position	Bit Name	Function
15:2	RFU	Reserved. Write 0. 0 returned when read.
1	THRU	Serial controller interrupt status (through, read only) 1: Interrupt occurrence 0: No interrupt
0	LATCH	Serial controller interrupt status (latch) During read / During write 1: Interrupt occurrence / Interrupt status clear 0: No interrupt / No change

This register indicates whether there is an interrupt output for the 16550 serial controller.

The THRU bit can read the interrupt output status for the 16550 serial controller as is.

The LATCH bit is held until the interrupt output for the 16550 serial controller is cleared by software. This bit is cleared to 0 by writing 1 to it.

[MEMO]

CHAPTER 9 IEEE1284 PARALLEL CONTROLLER

This controller is a parallel interface (host controller) that complies with IEEE1284. This controller uses the NBH1284L core macro.

9.1 Macro Functions

The NBH1284L macro provides 7 types of macro modes, which are selected by writing to the MODE (2:0) bits of the ECR register (refer to **9.2.14 ECR (0x1500 3834)**). Table 9-1 shows the macro mode functions.

Table 9-1. Macro Mode Functions (1/2)

Macro Mode	ECR Register MODE (2:0) Bits	Function
STD	000	Standard parallel port mode Only normal direction transfer using the DATA register is possible. • Reset FIFO • Even if the DIR bit of the DCR register is set, the output data bus to peripheral does not go into high impedance.
PS/2	001	PS/2 parallel port mode Normal direction and reverse direction transfers using the DATA register are possible. • Reset FIFO • The transfer direction can be set with the DIR bit of the DCR register.
FIFO	010	Parallel port FIFO mode Normal direction transfer using the CFIFO register is possible. • The data written to the CFIFO register is automatically transferred to peripheral using the compatible mode protocol. • Even if the DIR bit of the DCR register is set, the output data bus to peripheral does not go into high impedance.
ECP	011	ECP parallel port mode Normal direction and reverse direction transfers using the DFIFO register are possible, as well as normal direction transfer using the AFIFO register. • The data written to the DFIFO register and the commands written to the AFIFO register are automatically transferred to peripheral using the ECP protocol. • Data from peripheral is automatically stored to FIFO using the ECP protocol. • The transfer direction can be set with the DIR bit of the DCR register.

Table 9-1. Macro Mode Functions (2/2)

Macro Mode	ECR Register MODE (2:0) Bits	Function
EPP	100	EPP mode Normal direction and reverse direction transfers using the EPPA register and the EPPD register are possible. Normal direction transfer using the DATA register like in the STD mode is also possible (FIFO is not reset). Before entering this mode, select the EPP1.7 mode or the EPP1.9 mode with bit 7 of the MCR register. If the eppM bit of the MCR register is 0, the EPP1.7 mode is selected, and the eppM bit is 1, the EPP1.9 mode is selected. • The data written to the EPPA register and the EPPD register is automatically transferred to peripheral using the EPP1.7/EPP1.9 protocol. • The data of each register is automatically received using the EPP1.7/EPP1.9 protocol by reading the EPPA register and the EPPD register. • The DIR bit of the DCR register has no influence on the transfer direction (This bit becomes automatically 1 during read).
–	101	RFU
TEST	110	Test mode The software can know the FIFO configuration. • Write and read of FIFO on the VR4121 side only are possible. • No data output
CNFG	111	Configuration mode Transfer to/from peripheral is not possible. Software can know the device configuration. • Access to CNFGA and CNFGB registers is possible.

Furthermore, whether compatible, nibble, byte, ECP, and EPP transfer mode, which are set in IEEE1284, can be used is determined by the macro mode. Table 9-2 shows the relationships between the macro modes and the IEEE1284 transfer mode.

Table 9-2. Macro Mode Correspondence Table

Macro Mode		MCR Register eppM Bit	Transfer Type	DMA Enable/ Disable	IEEE1284 Transfer Mode Possible/Not Possible					
					Compatible	Nibble	Byte	ECP	EPP	
									1.7	1.9
STD		–	Register	×	O	O	×	O Note 2	O Note 2	O Note 2
PS/2		–		×	O	O	O	O	O	O
FIFO		–	FIFO	× Note 1	◎	×	×	×	×	×
ECP		–		× Note 1	×	×	×	◎	×	×
EPP	1.7	0	Register	×	O	O	×	O Note 2	◎	×
	1.9	1		×	O	O	×	O Note 2	×	◎
TEST		–	FIFO	× Note 1	×	×	×	×	×	×
CNFG		–	–	×	×	×	×	×	×	×

Notes 1. The NBH1284L core macro supports DMA, but since the VRC4172 does not incorporate a DMAC for the parallel controller, DMA transfer is not possible.

2. Only transmission is possible. Reception is not possible.

Remark ◎: Automatic handshake possible, O: Possible, ×: Not possible

9.2 Register Set

Table 9-3 lists the parallel control registers.

Table 9-3. Parallel Control Registers

Address	MODE (2:0)	R/W	Symbol	Function
0x1500 3820	001, 100	R	DATA	Parallel port data register
	000, 001, 100	W	DATA	Parallel port data register
	011		AFIFO	ECP address FIFO
0x1500 3822	-	R	DSR	Device status register
0x1500 3824	-	R/W	DCR	Device control register
0x1500 3826	000, 001	R/W	MCR	Mode control register
	100	R/W	EPPA	EPP address register
0x1500 3828	100	R/W	EPPD	EPP data register
0x1500 3830	010	W	CFIFO	Parallel port data FIFO
	011	R/W	DFIFO	ECP data FIFO
	110	R/W	TFIFO	Test FIFO
	111	R/W	CNFGA	Configuration register A
0x1500 3832	111	R/W	CNFGB	Configuration register B
0x1500 3834	-	R/W	ECR	Expansion control register

Remarks MODE(2:0)are bits 7 to 5 of the ECR register.

The details of these registers are shown next.

9.2.1 DATA (0x1500 3820: MODE (2:0) = 001, 100, DIR = 1, during read)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7:0	DATA (7:0)	Parallel receive data

This register stores parallel communication receive data.

Set the DIR bit of the DCR register to 1 when accessing this register.

9.2.2 DATA (0x1500 3820: MODE (2:0) = 000, 001, 100, DIR = 0, during write)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
R/W	W	W	W	W	W	W	W	W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7:0	DATA (7:0)	Parallel transmit data

This register stores parallel communication transmit data.

Set the DIR bit of the DCR register to 0 when accessing this register.

9.2.3 AFIFO (0x1500 3820: MODE (2:0) = 011, DIR = 0, during write)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	DTYPE	AFIFO6	AFIFO5	AFIFO4	AFIFO3	AFIFO2	AFIFO1	AFIFO0
R/W	W	W	W	W	W	W	W	W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7	DTYPE	AFIFO (6:0) data type 1: ECP address 0: Run Length
6:0	AFIFO (6:0)	ECP address or Run Length

This register sets the ECP address and the Run Length.

Transfer started automatically when this register is written.

Set the DIR bit of the DCR register to 1 when accessing this register.

9.2.4 DSR (0x1500 3822)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	nBusy	nAck	PError	Select	nFault	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	1	1	1

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7	nBusy	BUSY pin status 1: Low level 0: High level
6	nAck	ACK# pin status 1: High level 0: Low level
5	PError	PE pin status 1: High level 0: Low level
4	Select	SELECT pin status 1: High level 0: Low level
3	nFault	ERROR# pin status 1: High level 0: Low level
2:0	RFU	Reserved. Write 1. 1 returned when read.

This register shows the status of the parallel port interface pins.

9.2.5 DCR (0x1500 3824)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RFU	DIR	acklntEN	Selectln	nlnit	autofd	strobe
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
After reset	1	1	0	0	0	1	0	0

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7:6	RFU	Reserved. Write 1. 1 returned when read.
5	DIR	Transfer direction 1: External device → V_{RC}4172 (only PS/2 and ECP mode valid) 0: V_{RC}4172 → External device
4	acklntEN	Control of interrupt enable using rising edge of ACK# signal 1: Enable 0: Disable
3	Selectln	Output value to SELECTIN# pin 1: Low level 0: High level
2	nlnit	Output value to INIT# pin 1: High level 0: Low level
1	autofd	Output value to AUTOFEED# pin 1: Low level 0: High level
0	strobe	Output value to STROBE# pin 1: Low level 0: High level

This register controls the parallel port interface direction and sets the output value for the output pins.

9.2.6 MCR (0x1500 3826: MODE (2:0) = 000, 001)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	eppM	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R/W	R	R	R	R	R	R	R
After reset	1	0	0	0	0	0	0	1

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7	eppM	EPP mode setting 1: EPP1.9 mode 0: EPP1.7 mode
6:1	RFU	Reserved. Write 0. 0 returned when read.
0	RFU	Reserved. Write 1. 1 returned when read.

This register sets the EPP mode.

9.2.7 EPPA (0x1500 3826: MODE (2:0) = 100)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	eppA7	eppA6	eppA5	eppA4	eppA3	eppA2	eppA1	eppA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	1	0	0	0	0	0	0	1

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7:0	eppA (7:0)	Transmit/receive data in EPP mode (address)

This register stores transfer data in the EPP mode.

The data stored to this register through write is automatically transferred to peripheral using the EPP protocol. When this register is read, data is automatically received using the EPP protocol (The value is not stored in the register).

9.2.8 EPPD (0x1500 3828: MODE (2:0) = 100)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	eppD7	eppD6	eppD5	eppD4	eppD3	eppD2	eppD1	eppD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	1	0	0	0	0	0	0	1

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7:0	eppD (7:0)	Transmit/receive data in EPP mode (data)

This register stores transmit/receive data in the EPP mode.

The data stored to this register through write is automatically transferred to peripheral using the EPP protocol. When this register is read, data is automatically received using the EPP protocol (The value is not stored in the register).

9.2.9 CFIFO (0x1500 3830: MODE (2:0) = 010)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	CFIFO7	CFIFO6	CFIFO5	CFIFO4	CFIFO3	CFIFO2	CFIFO1	CFIFO0
R/W	W	W	W	W	W	W	W	W
After reset	0	0	0	0	0	0	0	1

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7:0	CFIFO (7:0)	Transmit data in FIFO mode

This register sets transmit data in the FIFO mode.

The data written to this register is transferred to FIFO, and is automatically transferred to peripheral using the compatible mode protocol.

9.2.10 DFIFO (0x1500 3830: MODE (2:0) = 011)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	DFIFO7	DFIFO6	DFIFO5	DFIFO4	DFIFO3	DFIFO2	DFIFO1	DFIFO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	1

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7:0	DFIFO (7:0)	Transmit/receive data in ECP mode

This register stores transmit/receive data in the ECP mode.

When the DIR bit of the DCR register is 0, the data stored to this register through write is automatically transferred to peripheral using the ECP protocol. When the DIR bit of the DCR register is 1, data is automatically received using the ECP protocol by reading this register.

9.2.11 TFIFO (0x1500 3830: MODE (2:0) = 110)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	TFIFO7	TFIFO6	TFIFO5	TFIFO4	TFIFO3	TFIFO2	TFIFO1	TFIFO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	1

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7:0	TFIFO (7:0)	Data stored to FIFO in TEST mode

This register is used to view the FIFO configuration.

The data written to this register is stored to FIFO. Data is read from the start of FIFO when this register is read. For example, when 0x22, 0x11, and 0x00 are written, 0x22, 0x11, 0x00 are read out, in this order.

Data transmission/reception with peripheral is not performed.

9.2.12 CNFGA (0x1500 3830: MODE (2:0) = 111)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	ISALVL	impID2	impID1	impID0	RFU	RFU	RFU	RFU
R/W	R/W	R	R	R	R	R	R	R
After reset	0	0	0	1	0	1	0	0

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7	ISALVL	Interrupt level setting 1: Level 0: Pulse
6:4	impID (2:0)	ID number and CFIFO, DFIFO, TFIFO size 001: 1 byte (fixed)
3	RFU	Reserved. Write 0. 0 returned when read.
2	RFU	Reserved. Write 1. 1 returned when read.
1:0	RFU	Reserved. Write 0. 0 returned when read.

This register sets the interrupt level.

9.2.13 CNFGB (0x1500 3832: MODE (2:0) = 111)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	compress	intrValue	intrLine2	intrLine1	intrLine0	RFU	RFU	RFU
R/W	R/W	R	R	R	R	R	R	R
After reset	0	Undefined	0	0	1	0	0	0

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7	compress	Support of compressed data from peripheral in ECP mode 1: Support 0: Do not support
6	intrValue	Interrupt notification pin (macro pin) status 1: High level 0: Low level
5:3	intrLine (2:0)	Interrupt line channel number (8 channels)
2:0	RFU	Reserved. Write 0. 0 returned when read.

This register sets interrupt-related definitions and option functions.

9.2.14 ECR (0x1500 3834)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	MODE2	MODE1	MODE0	nErIntEn	dmaEn	serviceInt	full	empty
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R
After reset	0	0	0	1	0	1	0	1

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7:5	MODE (2:0)	Operation mode setting 111: CNFIG (Config) mode 110: TEST mode 101: RFU 100: EPP mode 011: ECP mode 010: FIFO mode 001: PS/2 mode 000: STD (Standard) mode
4	nErIntEn	Enable interrupt occurrence at falling edge of ERROR# signal (valid only in ECP mode) 1: Disable 0: Enable
3	dmaEn	DMA operation enable 1: RFU 0: Disable
2	serviceInt	ECP service interrupt 1: Disable DMA and all service interrupts 0: Enable the following 3 interrupts. This bit is set to 1 upon occurrence of an interrupt. dmaEn = 1: When terminal count is reached during DMA dmaEn = 1, DIR = 0: When there are 8 or more free bytes in FIFO dmaEn = 1, DIR = 1: When there are 8 or more bytes of valid data in FIFO
1	full	FIFO status (full) 1: FIFO full status 0: FIFO has at least 1 byte of free space
0	empty	FIFO status (empty) 1: FIFO is empty 0: FIFO has at least 1 byte of data

This register sets the parallel controller operation mode.

CHAPTER 10 16550 SERIAL CONTROLLER

The 16550 serial controller is a serial interface that supports RS-232-C compliant communication. It provides 1 channel each for transmit and receive. This serial controller is functionally compatible with the NS16550D.

10.1 Register Set

Table 10-1 lists the serial control registers.

Table 10-1. Serial Control Registers

Address	LCR Register LCR7 Bit	R/W	Symbol	Function
0x1500 3810	0	R	RBR	Receive buffer register
		W	THR	Transmit hold register
	1	R/W	DLL	Divide ratio lower register
0x1500 3812	0	R/W	IER	Interrupt enable register
	1	R/W	DLM	Divide ratio higher register
0x1500 3814	–	R	IIR	Interrupt display register
		W	FCR	FIFO control register
0x1500 3816	–	R/W	LCR	Line control register
0x1500 3818	–	R/W	MCR	Modem control register
0x1500 381A	–	R/W	LSR	Line status register
0x1500 381C	–	R/W	MSR	Modem status register
0x1500 381E	–	R/W	SCR	Scratch register

The details of these registers are shown next.

10.1.1 RBR (0x1500 3810: LCR7 = 0, during read)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	RXD7	RXD6	RXD5	RXD4	RXD3	RXD2	RXD1	RXD0
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7:0	RXD (7:0)	Serial receive data

This register stores serial communication receive data.

Set the LCR7 bit of the LCR register to 0 when accessing this register.

10.1.2 THR (0x1500 3810: LCR7 = 0, during write)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	TXD7	TXD6	TXD5	TXD4	TXD3	TXD2	TXD1	TXD0
R/W	W	W	W	W	W	W	W	W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7:0	TXD (7:0)	Serial transmit data

This register stores serial communication transmit data.

Set the LCR7 bit of the LCR register to 0 when accessing this register.

10.1.3 DLL (0x1500 3810: LCR7 = 1)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	DLL7	DLL6	DLL5	DLL4	DLL3	DLL2	DLL1	DLL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7:0	DLL (7:0)	Baud rate divisor (lower byte)

This register sets the baud rate generator divisor (divide ratio).

This register and the DLM register (higher byte register) are handled combined as 16-bit data.

Set the LCR7 bit of the LCR register to 1 when accessing this register.

10.1.4 IER (0x1500 3812: LCR7 = 0)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RFU	RFU	RFU	IE3	IE2	IE1	IE0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:4	RFU	Reserved. Write 0. 0 returned when read.
3	IE3	Modem status interrupt 1: Enable 0: Disable
2	IE2	Receive status interrupt 1: Enable 0: Disable
1	IE1	Transmit hold register empty interrupt 1: Enable 0: Disable
0	IE0	Receive data existing interrupt or FIFO mode timeout interrupt 1: Enable 0: Disable

This register enables/disables the 5 types of interrupts that can be used for the serial controller. Setting a bit to 1 enables the corresponding interrupt. Setting all the bits of this register to 0 can stop use of all the interrupt functions.

When an interrupt has been disabled, it is not indicated as a pending interrupt by the IIR0 bit of the IIR register even if the conditions for that interrupt are satisfied.

Set the LCR7 bit of the LCR register to 0 when accessing this register.

10.1.5 DLM (0x1500 3812: LCR7 = 1)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	DLM7	DLM6	DLM5	DLM4	DLM3	DLM2	DLM1	DLM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7:0	DLM (7:0)	Baud rate divisor (higher byte)

This register sets the baud rate generator divisor (divide ratio).

This register and the DLL register (lower byte register) are handled combined as 16-bit data.

Set the LCR7 bit of the LCR register to 1 when accessing this register.

The relationship between the baud rate and the settings of the DLL and DLM registers is shown below.

Table 10-2. Relationship Between Baud Rate and Divisor

Baud Rate	Divisor	Error Percentage[Note]
50	2304	0.1
75	1536	0.2
110	1047	0.2
134.5	857	0.4
150	768	0.2
300	384	0.2
600	192	0.2
1200	96	0.2
1800	64	0.2
2000	58	0.5
2400	48	0.2
3600	32	0.2
4800	24	0.2
7200	16	0.2
9600	12	0.2
19200	6	0.2
38400	3	0.2
57600	2	0.2
115200	1	0.2

Note Error percentage for baud rate

10.1.6 IIR (0x1500 3814: during read)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	IIR7	IIR6	RFU	RFU	IIR3	IIR2	IIR1	IIR0
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	1

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7:6	IIR (7:6)	11 when the FCR0 bit of the FCR register is 1 (always set to 0 in 16450 mode)
5:4	RFU	Reserved. Write 0. 0 returned when read.
3	IIR3	Existence of pending character timeout interrupt request (in FIFO (16550) mode) 1: Yes 0: No
2:1	IIR (2:1)	Interrupt priority order setting Refer to **Table 10-3**
0	IIR0	Existence of pending interrupt request 1: Yes 0: No

This register displays whether pending interrupt requests exist and the priority order of the interrupts. The priority order, from high to low, is receive line status, receive data existence, character timeout, transmit hold register empty, and modem status.

The contents of the IIR3 bit are valid only in the FIFO (16550) mode. This bit is always 0 in the 16450 mode. Moreover, the IIR2 bit is also set to 1 when 1 is set to the IIR3 bit.

Table 10-3. Interrupt Set/Reset

IIR Register			Interrupt Set/Reset Function			
Bit 3 **Note**	Bit 2	Bit 1	Priority Order	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	1	1	Top priority	Receive line status	Overrun error, parity error, framing error, or break	Line status register read
0	1	0	2	Receive data existence	Receive data exists, or trigger level was reached	Receive buffer register read, or FIFO is lower than trigger level
1	1	0	2	Character timeout	Within the interval of the 4 latest characters, not a single character was removed from or added to the receive FIFO, and one or more characters existed in the receive FIFO during this period.	Receive buffer register read
0	0	1	3	Transmit hold register empty	Transmit register is empty	IIR read (in case of an interrupt source), or transmit hold register write
0	0	0	4	Modem status	CTS#, DSR#, or DCD#	Modem status register read

Note In the FIFO mode

10.1.7 FCR (0x1500 3814: during write)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	FCR7	FCR6	RFU	RFU	FCR3	FCR2	FCR1	FCR0
R/W	W	W	W	W	W	W	W	W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7:6	FCR (7:6)	Receive FIFO trigger 11: 14 bytes 10: 8 bytes 01: 4 bytes 00: 0 bytes
5:4	RFU	Reserved. Write 0. 0 returned when read.
3	FCR3	FIFO (16550) mode setting 1: Mode 1 0: Mode 0
2	FCR2	Transmit FIFO or counter clear. This bit is cleared to 0 when 1 is written. 1: FIFO or counter clear 0: Normal
1	FCR1	Transmit FIFO or counter clear. This bit is cleared to 0 when 1 is written. 1: FIFO or counter clear 0: Normal
0	FCR0	Transmit/receive FIFO enable 1: Enable 0: Disable (16450 mode)

This register controls the FIFO.

10.1.8 LCR (0x1500 3816)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	LCR7	LCR6	LCR5	LCR4	LCR3	LCR2	LCR1	LCR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7	LCR7	Register switch when divisor latch address 1: Divisor latch register 0: Receive buffer, transmit hold register, interrupt enable register
6	LCR6	Break control 1: Set break 0: Cancel break
5	LCR5	Parity fix 1: Fix parity 0: Do not fix parity
4	LCR4	Parity setting 1: Even parity 0: Odd parity
3	LCR3	Parity enable During transmit / During receive 1: Generate parity / Check 0: No parity / No check
2	LCR2	Stop bit setting 1: 1.5 bits (character length = 5 bits), 2 bits (character length = 6, 7, 8 bits) 0: 1 bit
1:0	LCR (1:0)	Length of 1 character 11: 8 bits 10: 7 bits 01: 6 bits 00: 5 bits

This register is used for specifying the asynchronous data communication/exchange format and setting the divisor latch access.

The LCR6 bit is used to transmit the break status to the UART of receive side. When the LCR6 bit becomes 1, the serial output (TXD) is forcibly changed to the spacing (0) status.

The LCR5 bit setting is made valid by the LCR4 and LCR3 bit settings.

10.1.9 MCR (0x1500 3818)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RFU	RFU	MCR4	MCR3	MCR2	MCR1	MCR0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:5	RFU	Reserved. Write 0. 0 returned when read.
4	MCR4	Diagnosis test (local loopback) use 1: RFU 0: Disable
3	MCR3	OUT2 signal (internal) setting 1: Low level 0: High level
2	MCR2	OUT1 signal (internal) setting 1: Low level 0: High level
1	MCR1	RTS# signal setting 1: Low level 0: High level
0	MCR0	DTR# signal setting 1: Low level 0: High level

This register is used to control the interface with the modem.

Since local loopback is not supported, do not set the MCR4 bit to 1.

10.1.10 LSR (0x1500 381A)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	LSR7	LSR6	LSR5	LSR4	LSR3	LSR2	LSR1	LSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	1	1	0	0	0	0	0

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7	LSR7	Detection of various types of errors (in FIFO (16550) mode) 1: Parity error, framing error, break detection 0: Normal
6	LSR6	Transmit block empty In 16450 mode / In FIFO (16550) mode 1: No data in transmit hold register and transmit shift register / No data in transmit FIFO 0: Data in either transmit hold register or transmit shift register / Data in transmit FIFO
5	LSR5	Transmit hold register empty In 16450 mode / In FIFO (16550) mode 1: Characters transferred to transmit shift register / Transmit FIFO is empty 0: Characters stored in transmit hold register / Transmit data in transmit FIFO
4	LSR4	Break interrupt 1: Detected 0: Normal
3	LSR3	Framing error 1: Detected 0: Normal
2	LSR2	Parity error 1: Detected 0: Normal
1	LSR1	Overrun error 1: Detected 0: Normal
0	LSR0	Receive data ready 1: Receive data in FIFO 0: No receive data in FIFO

This register is used for CPU to obtain information regarding data transfer.

When the LSR7 and LSR (4:1) bits are set to 1, they are cleared to 0 when this register is read.

The LSR7 bit is valid only in the FIFO (16550) mode. It is always 0 in the 16450 mode.

The LSR4 bit becomes 1 when the receive data input is in spacing status (0) for longer than the transmit time of 1 word (start bit + data bit + parity bit + stop bit) (break). In the FIFO (16550) mode, detection of a break in 1 character in the FIFO is considered as an error character, and a break is notified when that character reaches the top of the FIFO. Upon occurrence of a break, 1 zero character is transferred to the FIFO. The RXD pin changes to marking status, and upon reception of the next valid start bit, transfer of the next character becomes possible.

The LSR3 bit becomes 1 upon detection of a 0 (spacing level) stop bit after the last data bit or parity bit (framing error). In the FIFO (16550) mode, detection of a framing error in 1 character in the FIFO is considered as an error character, and a framing error is notified when that character reaches the top of the FIFO. Upon occurrence of a framing error, the serial controller attempts to gain synchronization again. At this time, the error source is considered to have been in the start bit, and data is loaded after sampling the next start bit two times.

The LSR2 bit becomes 1 when the received characters fail to satisfy the even or odd parity specified with the LCR4 bit (parity error). In the FIFO (16550) mode, detection of a parity error in 1 character in the FIFO is considered as an error character, and a parity error is notified when that character reaches the top of the FIFO.

The LSR1 bit becomes 1 when the next character is transferred to the receive buffer register before the CPU has read the receive buffer, and the preceding character disappears (overrun). If, in the FIFO (16550) mode, the data exceeds the trigger level and continues to be transferred to the FIFO, so that the FIFO becomes full, no overrun error occurs until the next characters have been completely stored to the shift register. An overrun error is notified immediately after it occurs. The characters in the shift register are overwritten, but they are not transferred to the FIFO.

10.1.11 MSR (0x1500 381C)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	MSR7	MSR6	MSR5	MSR4	MSR3	MSR2	MSR1	MSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	Undefined	Undefined	Undefined	Undefined	0	0	0	0

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7	MSR7	DCD# signal status 1: Low level 0: High level
6	MSR6	RI# signal status 1: Low level 0: High level
5	MSR5	DSR# signal status 1: Low level 0: High level
4	MSR4	CTS# signal status 1: Low level 0: High level
3	MSR3	DCD# signal change 1: Yes 0: No
2	MSR2	RI# signal change 1: Yes 0: No
1	MSR1	DSR# signal change 1: Yes 0: No
0	MSR0	CTS# signal change 1: Yes 0: No

This register indicates the current status of control signals input from the modem and whether line statuses have changed.

10.1.12 SCR (0x1500 381E)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	SCR7	SCR6	SCR5	SCR4	SCR3	SCR2	SCR1	SCR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. 0 returned when read.
7:0	SCR (7:0)	General-purpose data

This register is a read- and write-enabled 8-bit register that can be used freely by the user.

[MEMO]

CHAPTER 11 USB HOST CONTROLLER

The USB host controller conforms with OPEN HCI Specification Release 1.0. This controller supports power management such as the clock stop function on the PCI/USB side. It also provides two downstream ports. However, it does not support legacy functions.

11.1 Features

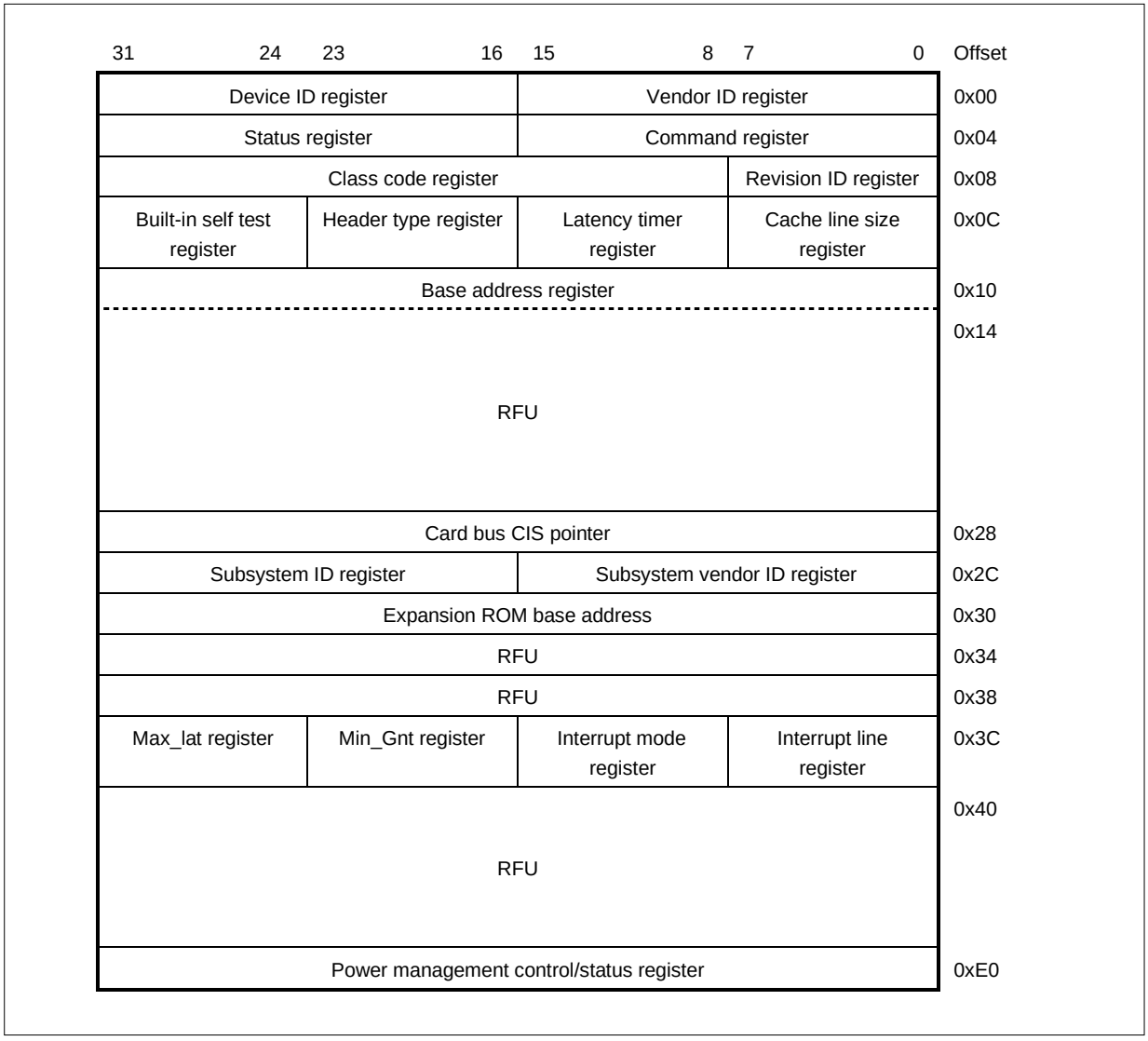
The features of the USB host controller are shown below.

- Functions
  - Conforms with OPEN HCI Specification Release 1.0
  - Communication with USB devices asynchronously to host CPU
  - Supports two types of USB devices, full speed (12 Mbps) and low speed (1.5 Mbps)
  - System clock: 48 MHz
- Interface
  - USB interface transceiver
    Conforms with Universal Serial Bus Specification 1.0
    Automatic switching between full speed (12 Mbps) and low speed (1.5 Mbps)
- Communication with host CPU
  - USB host: Via operational register in controller
  - System: Via host controller communication area in memory space
- Memory and I/O space
  - 4 GB system: Mapping to 4 KB space of memory space
  - System: 256-byte space host controller communication area allocated in memory space
- Internal FIFOs
  - PCI side: 16-byte (4×4 double-words)
  - USB side: 64-byte (64×1 bytes)
- Root hub
  - 2 downstream ports
- Low power consumption
  - PCI clock stop function and USB clock stop function

11.2 USB Host Control Configuration Registers

In the case of the PCI local bus (internal PCI bus in the VRC4172), the USB host control configuration registers are accessed to set the hardware resources used by devices and the characteristics and operation of devices. Each register is accessed with the PCI configuration cycle. For more detailed information, see **the PCI Local bus Specification Revision 2.1**.

Figure 11-1. USB Host Control Configuration Space



11.2.1 Register set

Table 11-1 lists the USB host control configuration registers.

Table 11-1. USB Host Control Configuration Registers

Offset Address	Name	Bit	R/W	Reset Value	Contents
0x00	Vendor ID register	15:0	R	0x1033	NEC vendor ID
0x02	Device ID register	31:16	R	0x0000	Device ID of this macro
0x04	Command register	15:0	R/W	0x0000	Refer to **11.2.2**
0x06	Status register	31:16	R/W	0x0000	Refer to **11.2.3**
0x08	Revision ID register	7:0	R	0x01	Indicates compliance with PCI Local bus Specification Revision 2.1
0x09	Class code base address register	31:24	R	0x0C	Indicates that it is a serial bus controller device
	Class code subclass register	23:16	R	0x03	Indicates that it is a USB device
	Class code programming interface register	15:8	R	0x10	Indicates that it is an OpenHCI host controller
0x0C	Cache line size register	7:0	R	0x00	Caches cannot be used
0x0D	Latency timer register	15:11	R/W	00000	Time during which bus cycle executed can be continued
		10:8	R	000	
0x0E	Header type register	23:16	R	0x80	Not a PCI-to-PCI bridge
0x0F	Built-in self test register	31:24	R	0x00	BIST not supported
0x10	Base address register	31:0	R/W	0x0000 0000	Refer to **11.2.4**
0x2C	Subsystem vendor ID register	15:0	R (/W)	0x0000	(Write is enabled by setting the ID Write Mask bit of the power management control/status register)
0x2E	Subsystem ID register	31:16	R (/W)	0x0000	(Write is enabled by setting the ID Write Mask bit of the power management control/status register)
0x3C	Interrupt line register	7:0	R (/W)	0x00	Displays the interrupt line route. Write is enabled only when using the power management control/status register
0x3D	Interrupt mode register	15:8	R	0x01	Indicates the INTA# signal (internal PCI bus signal)
0x3E	Min_Gnt register (burst cycle minimum request time register)	23:16	R	0x01	Burst cycle minimum request time
0x3F	Max_lat register (bus mastership request frequency register)	31:24	R	0x2A	Bus mastership request frequency
0xE0	Power management control/status register	31:0	R/W	0x0000 0000	Refer to **11.2.5**

11.2.2 Command register (offset address: 0x04)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	Fast back-to-back enable	SERR# enable
R/W	R	R	R	R	R	R	R	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	Wait cycle control	Parity Error response	VGA palette snoop	Memory write and Invalidate enable	Special Cycles	Bus Master	Memory space	I/O space
R/W	R	R	R	R	R	R/W	R/W	R
After reset	0	0	0	0	0	0	0	0

	Bit Position	Bit Name	Function
	15:10	RFU	Reserved. Write 0. 0 returned when read.
	9	Fast back-to-back enable	Fast back-to-back access is not supported.
★	8	SERR# enable	Response control for system errors 1: Drives the SERR# signal (internal PCI bus signal) 0: Does not drives the SERR# signal
	7	Wait cycle control	Address/data stepping is not supported.
	6	Parity Error response	Parity errors are not checked.
	5	VGA palette snoop	VGA palette snoop is invalid.
	4	Memory write and Invalidate enable	Memory write and invalidate are invalid.
	3	Special Cycles	Special cycles are ignored.
★	2	Bus Master	Bus master operation control 1: Can be operated as bus master 0: Cannot execute cycles as bus master
★	1	Memory space	Response control for memory access 1: Responds to memory access 0: Does not respond to memory access
	0	I/O space	Does not respond to I/O access

11.2.3 Status register (offset address: 0x06)

(1/2)

Bit Position	15	14	13	12	11	10	9	8
Bit name	Detected parity error	Signaled system error	Received master abort	Received target abort	Signal target abort	DEVSEL timing	DEVSEL timing	Data Parity Error detected
R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W
After reset	0	0	0	0	0	0	1	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	Fast back-to-back capable	UDF support	66 MHz capable	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
15	Detected parity error	Detection of data parity or address parity 1: Detected 0: Not detected
14	Signaled system error	SERR# signal (internal PCI bus signal) active 1: Active 0: Inactive
13	Received master abort	The master sets this bit to 1 when the bus cycle the USB host controller was executing is ended with master abort. This bit is cleared by writing 0 to it.
12	Received target abort	The master sets this bit to 1 when the bus cycle the USB host controller was executing is ended with target abort. This bit is cleared by writing 0 to it.
11	Signal target abort	The target sets this bit to 1 when the bus cycle in which the USB host controller was accessed is ended by target abort. This bit is cleared by writing 0 to it.
10:9	DEVSEL timing	Active timing of the DEVSEL# signal (internal PCI bus signal) 01: Medium speed
8	Data Parity Error detected	Set to 1 when the following 3 conditions are met. • When the USB host controller has made the PERR# signal (internal PCI bus signal) active, or the fact that the PERR# signal has been made active by the target has been detected • When the USB host controller was the bus master in the bus cycle in which a data parity error occurred • When the Parity Error response bit of the command register has been set to 1 In the case of the V_{RC}4172, the Parity Error response bit is fixed to 0, so that this bit is never set to 1.

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Bit Position	Bit Name	Function
7	Fast back-to-back capable	Response to fast back-to-back access Fixed to 0 (disabled).
6	UDF support	UDF is not supported.
5	66 MHz capable	33 MHz operation
4:0	RFU	Reserved. Write 0. 0 returned when read.

11.2.4 Base address register (offset address: 0x10)

Bit Position	31	30	29	28	27	26	25	24
Bit name	Base address (MSB)	Base address (MSB)	Base address (MSB)	Base address (MSB)	Base address (MSB)	Base address (MSB)	Base address (MSB)	Base address (MSB)
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	23	22	21	20	19	18	17	16
Bit name	Base address (MSB)	Base address (MSB)	Base address (MSB)	Base address (MSB)	Base address (MSB)	Base address (MSB)	Base address (MSB)	Base address (MSB)
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	15	14	13	12	11	10	9	8
Bit name	Base address (MSB)	Base address (MSB)	Base address (MSB)	Base address (MSB)	Base address (LSB)	Base address (LSB)	Base address (LSB)	Base address (LSB)
R/W	R/W	R/W	R/W	R/W	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	Base address (LSB)	Base address (LSB)	Base address (LSB)	Base address (LSB)	Prefetchable	Type	Type	Memory space Indicator
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
31:12	Base address (MSB)	Indicates the higher 20 bits of the base address of the operational register.
11:4	Base address (LSB)	Indicates that the operational register has a 4 KB address space.
3	Prefetchable	Prefetching is not possible.
2:1	Type	Indicates that the operational register can be placed anywhere in the 4 GB main memory space.
0	Memory space Indicator	Indicates that the operational register is mapped to the main memory space.

11.2.5 Power management control/status register (offset address: 0xE0)

(1/2)

Bit Position	31	30	29	28	27	26	25	24
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	23	22	21	20	19	18	17	16
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	Wakeup_ Enable
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	Wakeup_ Status
R/W	R	R	R	R	R	R	R	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	ID Write Mask	PC_mode	REQ_ Enable	RFU	RFU	Status Change Standby	Power Status	Power Status
R/W	R/W	R/W	R/W	R	R	R	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
31:17	RFU	Reserved. Write 0. 0 returned when read.
16	Wakeup_Enable	WAKE signal output control 1: WAKE signal enabled 0: WAKE signal disabled
15:9	RFU	Reserved. Write 0. 0 returned when read.
8	Wakeup_Status	Existence of Wakeup request 1: Yes 0: No This bit is cleared by writing 1 to it. Its value does not change even if 0 is written to it.
7	ID Write Mask	Write protect of subsystem ID and subsystem vendor ID 1: Write enable 0: Write mask
6	PC_mode	PC/AT™ compatible, PC-9800 series switch control 1: PC/AT compatible mode 0: PC-9800 series mode

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Bit Position	Bit Name	Function
5	REQ_Enable	REQ signal (internal PCI bus signal) output timing control 1: PCICLK (internal clock) asynchronous output 0: PCICLK synchronous output
4:3	RFU	Reserved. Write 0. 0 returned when read.
2	Status Change Standby	Device status regarding power status change control 1: Supported 0: Not supported
1:0	Power Status	Power status control bit 11: D3 (PCICLK stop, device power OFF) 10: D2 (PCICLK stop, device power ON) 01: RFU 00: D0 (PCICLK full mode)

Remarks 1. The REQ_Enable bit must always be used with its default value. If it is used asynchronously, the PCI specs will be deviated from.

2. When PC_mode bit = 0, the Power Status area is disabled. The Power Status area can be read and written from the system, while the USB host controller (HC) can perform read only.

3. When PC_mode bit = 0, the Wakeup_Status bit is disabled. This bit is set to 1 when Resume is detected from the USB while PC_mode bit = 1 and Power Status area = 10. At this time, make the WAKE signal active if Wakeup_Enable = 1. This bit is cleared by writing 1 to it, and the WAKE signal is made inactive at the same time. The above-described operation is performed only when the RHSC bit of the HcInterruptEnable register is set.

4. When the PC_mode bit = 0, the Wakeup_Enable bit is disabled.

5. When the Power Status area is set to 10 or 11, the Status Change Standby bit outputs 0s until status change becomes possible, and it outputs 1 when status change has become possible. When the Power Status area is set to 10 or 11, the value of the Status Change Standby bit is never returned to 0 once it has become 1.

11.3 Operational Registers

The USB host controller (HC) contains operational registers, which serve as the windows for communicating with the host CPU. These registers are mapped to a 4 KB space in the 4 GB main memory space of the system, and they are used by the host controller driver (HCD). All these registers are read/written in word units. The CPU accesses these registers via the internal PCI bus using the PC memory cycle. The base address is indicated by the base address register of the USB host control configuration space.

For more details, refer to **OPEN HCI Specification Release 1.0**.

11.3.1 Register set

Table 11-2 lists the host control operational registers.

Table 11-2. Host Control Operational Registers

Offset Address	R/W (HCD)	R/W (HC)	Symbol	Function
0x00	R	R	HcRevision	HC revision register
0x04	R/W	R/W	HcControl	HC control register
0x08	R/W	R/W	HcCommandStatus	HC command status register
0x0C	R/W	R/W	HcInterruptStatus	HC interrupt status register
0x10	R/W	R	HcInterruptEnable	HC interrupt enable register
0x14	R/W	R	HcInterruptDisable	HC interrupt disable register
0x18	R/W	R	HcHCCA	HC communication area register
0x1C	R	R/W	HcPeriodCurrentED	HC period current ED register
0x20	R/W	R	HcControlHeadED	HC control head ED register
0x24	R/W	R/W	HcControlCurrentED	HC control current ED register
0x28	R/W	R	HcBulkHeadED	HC bulk head ED register
0x2C	R/W	R/W	HcBulkCurrentED	HC bulk current ED register
0x30	R	R/W	HcDoneHead	HC done head register
0x34	R/W	R	HcFmInterval	HC frame interval register
0x38	R/W	R/W	HcFmRemaining	HC frame remaining register
0x3C	R/W	R/W	HcFmNumber	HC frame number register
0x40	R/W	R	HcPeriodicStart	HC periodic start register
0x44	R/W	R	HcLSThreshold	HC LS threshold register
0x48	R/W	R	HcRhDescriptorA	HC RH descriptor A register
0x4C	R/W	R	HcRhDescriptorB	HC RH descriptor B register
0x50	R/W	R/W	HcRhStatus	HC RH status register
0x54	R/W	R/W	HcRhPortStatus1	HC RH port status 1 register
0x58	R/W	R/W	HcRhPortStatus2	HC RH port status 2 register

The details of these registers are shown next.

11.3.2 HcRevision (offset address: 0x00)

Bit Position	31	30	29	28	27	26	25	24
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R	R	R	R	R	R	R	R
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	23	22	21	20	19	18	17	16
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R	R	R	R	R	R	R	R
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R	R	R	R	R	R	R	R
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	7	6	5	4	3	2	1	0
Bit name	Revision	Revision	Revision	Revision	Revision	Revision	Revision	Revision
R/W (HCD)	R	R	R	R	R	R	R	R
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0	0	0	1	0	0	0	0

Bit Position	Bit Name	Function
31:8	RFU	Reserved. Write 0. Since the values of these bits become undefined after reset, initialize them by software.
7:0	Revision	Indicates compliance with the OPEN HCI Specification Release 1.0.

11.3.3 HcControl (offset address: 0x04)

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Bit Position	31	30	29	28	27	26	25	24
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	23	22	21	20	19	18	17	16
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RWE	RWC	IR
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	0	0 Note 1	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	HCFS	HCFS	BLE	CLE	IE	PLE	CBCR	CBCR
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R/W	R/W	R	R	R	R	R	R
After reset	**Note 2**	**Note 2**	0	0	0	0	0	0

Bit Position	Bit Name	Function
31:11	RFU	Reserved. Write 0. Since the value of these bits become undefined after reset, initialize them by software.
10	RWE	Remote Wakeup Enable Enable/disable of remote wakeup upon detection of upstream resume signal 1: Enable 0: Disable
9	RWC	Remote Wakeup Connected Remote wakeup signal support 1: Support 0: Do not support

Notes 1. Only hardware reset is possible.

2. After hardware reset: 0
After software reset: 1

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Bit Position	Bit Name	Function
8	IR	Interrupt Routing Routing of interrupt request generated by event registered in the HcInterruptStatus register 1: SMI# signal output 0: USBINT# signal output
7:6	HCFS	Host Controller Functional Status for USB USB operation mode 11: UsbSuspend 10: UsbOperational 01: UsbResume 00: UsbReset
5	BLE	Bulk List Enable Enable/disable of bulk list processing for next frame 1: Enable 0: Disable
4	CLE	Control List Enable Enable/disable control list processing for next frame 1: Enable 0: Disable
3	IE	Isochronous Enable Enable/disable isochronous ED (Endpoint Descriptor) processing for next frame 1: Enable 0: Disable
2	PLE	Periodic List Enable Enable/disable cycle list processing for next frame 1: Enable 0: Disable
1:0	CBCR	Control Bulk Service Ratio Service ratio between control and bulk ED 11: 4:1 10: 3:1 01: 2:1 00: 1:1

11.3.4 HcCommandStatus (offset address: 0x08)

(1/2)

Bit Position	31	30	29	28	27	26	25	24
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	23	22	21	20	19	18	17	16
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	SOC	SOC
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R	R
R/W (HC)	R	R	R	R	R	R	R/W	R/W
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	0	0

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RFU	RFU	RFU	OCR	BLF	CLF	HCR
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R/W	R/W	R/W	R/W
After reset	Undefined	Undefined	Undefined	Undefined	0	0	0	0

Bit Position	Bit Name	Function
31:18	RFU	Reserved. Write 0. Since the value of these bits become undefined after reset, initialize them by software.
17:16	SOC	Scheduling Overrun Count Counting of scheduling overrun errors. Incremented upon occurrence of an error as follows: 00 (initialization) → 01 → 10 → 11 → 00
15:4	RFU	Reserved. Write 0. Since the value of these bits become undefined after reset, initialize them by software.
3	OCR	Ownership Change Request This bit is set by HCD to request HC control change. 1: Yes 0: No
2	BLF	Bulk List Filled Existence of TD (Transfer Descriptor) in bulk list 1: Yes 0: No

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Bit Position	Bit Name	Function
1	CLF	Control List Filled Existence of TD in control list 1: Yes 0: No
0	HCR	Host Controller Reset HC software reset Set to 1 by HCD, cleared to 0 by HC

11.3.5 HcInterruptStatus (offset address: 0x0C)

(1/2)

Bit Position	31	30	29	28	27	26	25	24
Bit name	RFU	OC	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R/W	R	R	R	R	R	R
After reset	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	23	22	21	20	19	18	17	16
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RHSC	FNO	UE	RD	SF	WDH	SO
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	Undefined	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
31	RFU	Reserved. Write 0. 0 returned when read.
30	OC	Ownership Change When the HCD sets the OCR bit of the HcCommandStatus register, this bit is set to 1 by HC. If it is not masked, a system monitoring interrupt (SMI) is immediately issued for this event. It is cleared by writing 0 to it.
29:7	RFU	Reserved. Write 0. Since the values of these bits become undefined after reset, initialize them by software.
6	RHSC	Root Hub Status Change This bit is set to 1 when the contents of the HcRhStatus register or HcRhPortStatusN (N = 1, 2) registers change. It is cleared by writing 0 to it.
5	FNO	Frame Number Overflow Change in value of bit 15 of HcFmNumber register 1: Yes 0: No

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Bit Position	Bit Name	Function
4	UE	Unrecoverable Error Detection of system error not related to USB 1: Detected 0: Normal
3	RD	Resume Detected Detection of Resume signal 1: Detected 0: Normal
2	SF	Start of Frame This bit is set at the start of a frame. It is cleared by writing 0 to it.
1	WDH	Writeback Done Head This bit is set when the contents of the HcDoneHead register are written to the HccaDoneHead area[Note]. This bit is cleared by HCD after the contents of HccaDoneHead are saved.
0	SO	Scheduling Overrun Occurrence of overrun in USB schedule of current frame 1: Occurred 0: Normal

Note The HccaDoneHead area is located on the HCCA (Host Controller Communication Area). The HCCA is a 256-byte system memory that is used when the HCD and HC communicate. For details, refer to **OPEN HCI Specification Release 1.0**.

11.3.6 HcInterruptEnable (offset address: 0x10)

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Bit Position	31	30	29	28	27	26	25	24
Bit name	MIE	OC	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	23	22	21	20	19	18	17	16
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RHSC	FNO	UE	RD	SF	WDH	SO
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
31	MIE	Master Interrupt Enable Enable/disable interrupts caused by events indicated by other bits of this register 1: Enable 0: Disable
30	OC	Ownership Change Interrupt request with Ownership Change 1: Enable 0: Disable
29:7	RFU	Reserved. Write 0. Since the values of these bits become undefined after reset, initialize them by software.
6	RHSC	Root Hub Status Change Interrupt request with Root Hub Status Change 1: Enable 0: Disable

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Bit Position	Bit Name	Function
5	FNO	Frame Number Overflow Interrupt request with Frame Number Overflow 1: Enable 0: Disable
4	UE	Unrecoverable Error Interrupt request with Unrecoverable Error 1: Enable 0: Disable
3	RD	Resume Detected Interrupt request with Resume Detect 1: Enable 0: Disable
2	SF	Start of Frame Interrupt request with Start of Frame 1: Enable 0: Disable
1	WDH	Writeback Done Head Interrupt request with HcDoneHead Writeback 1: Enable 0: Disable
0	SO	Scheduling Overrun Interrupt request with Scheduling Overrun 1: Enable 0: Disable

This register controls the sources of hardware interrupts.

Writing 1 sets the bits of this register, but writing 0 is ignored. To clear the values of the bits of this register, write 1 to the corresponding bit of the HcInterruptDisable register.

The bits of this register correspond to the bits of the HcInterruptStatus register.

When all the following conditions are satisfied, a hardware interrupt is generated.

- An interrupt source occurs and a given bit of the HcInterruptStatus register is set.
- A bit corresponding to the HcInterruptEnable register is set.
- The MIE bit of the HcInterruptEnable register is set.

11.3.7 HcInterruptDisable (offset address: 0x14)

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Bit Position	31	30	29	28	27	26	25	24
Bit name	MIE	OC	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	23	22	21	20	19	18	17	16
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RHSC	FNO	UE	RD	SF	WDH	SO
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
31	MIE	Master Interrupt Enable Enable/disable interrupts caused by events indicated by other bits of this register 1: Disable
30	OC	Ownership Change Interrupt request with Ownership Change 1: Disable
29:7	RFU	Reserved. Write 0. Since the values of these bits become undefined after reset, initialize them by software.
6	RHSC	Root Hub Status Change Interrupt request with Root Hub Status Change 1: Disable
5	FNO	Frame Number Overflow Interrupt request with Frame Number Overflow 1: Disable

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Bit Position	Bit Name	Function
4	UE	Unrecoverable Error Interrupt request with Unrecoverable Error 1: Disable
3	RD	Resume Detected Interrupt request with Resume Detect 1: Disable
2	SF	Start of Frame Interrupt request with Start of Frame 1: Disable
1	WDH	Writeback Done Head Interrupt request with HcDoneHead Writeback 1: Disable
0	SO	Scheduling Overrun Interrupt request with Scheduling Overrun 1: Disable

This register is used to clear the bits corresponding to the HcInterruptEnable register to 0.
When 1 is written, the corresponding bit of the HcInterruptEnable register is cleared to 0. Writing 0 is ignored.
The values of the HcInterruptEnable register are returned when this register is read.

11.3.8 HcHCCA (offset address: 0x18)

Bit Position	31	30	29	28	27	26	25	24
Bit name	HCCA	HCCA	HCCA	HCCA	HCCA	HCCA	HCCA	HCCA
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	23	22	21	20	19	18	17	16
Bit name	HCCA	HCCA	HCCA	HCCA	HCCA	HCCA	HCCA	HCCA
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	15	14	13	12	11	10	9	8
Bit name	HCCA	HCCA	HCCA	HCCA	HCCA	HCCA	HCCA	HCCA
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	HCCA	HCCA	HCCA	HCCA	HCCA	HCCA	HCCA	HCCA
R/W (HCD)	R	R	R	R	R	R	R	R
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
31:0	HCCA	Host Controller Communication Area Base address for host controller communication area. Since it is allocated in units of 256 bytes, bits 7 to 0 are fixed to 0.

11.3.9 HcPeriodCurrentED (offset address: 0x1C)

Bit Position	31	30	29	28	27	26	25	24
Bit name	PCED	PCED	PCED	PCED	PCED	PCED	PCED	PCED
R/W (HCD)	R	R	R	R	R	R	R	R
R/W (HC)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	23	22	21	20	19	18	17	16
Bit name	PCED	PCED	PCED	PCED	PCED	PCED	PCED	PCED
R/W (HCD)	R	R	R	R	R	R	R	R
R/W (HC)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	15	14	13	12	11	10	9	8
Bit name	PCED	PCED	PCED	PCED	PCED	PCED	PCED	PCED
R/W (HCD)	R	R	R	R	R	R	R	R
R/W (HC)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	PCED	PCED	PCED	PCED	PCED	PCED	PCED	PCED
R/W (HCD)	R	R	R	R	R	R	R	R
R/W (HC)	R/W	R/W	R/W	R/W	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
31:0	PCED	Period Current ED Physical addresses of Isochronous/InterruptED of cycle list processed in current frame. Since ED (Endpointer Descriptor) is allocated in units of 16 bytes, bits 3 to 0 are fixed to 0.

11.3.10 HcControlHeadED (offset address: 0x20)

Bit Position	31	30	29	28	27	26	25	24
Bit name	CHED	CHED	CHED	CHED	CHED	CHED	CHED	CHED
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	23	22	21	20	19	18	17	16
Bit name	CHED	CHED	CHED	CHED	CHED	CHED	CHED	CHED
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	15	14	13	12	11	10	9	8
Bit name	CHED	CHED	CHED	CHED	CHED	CHED	CHED	CHED
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	CHED	CHED	CHED	CHED	CHED	CHED	CHED	CHED
R/W (HCD)	R/W	R/W	R/W	R/W	R	R	R	R
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
31:0	CHED	Control Head ED Physical address of 1st ED of control list

11.3.11 HcControlCurrentED (offset address: 0x24)

Bit Position	31	30	29	28	27	26	25	24
Bit name	CCED	CCED	CCED	CCED	CCED	CCED	CCED	CCED
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	23	22	21	20	19	18	17	16
Bit name	CCED	CCED	CCED	CCED	CCED	CCED	CCED	CCED
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	15	14	13	12	11	10	9	8
Bit name	CCED	CCED	CCED	CCED	CCED	CCED	CCED	CCED
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	CCED	CCED	CCED	CCED	CCED	CCED	CCED	CCED
R/W (HCD)	R/W	R/W	R/W	R/W	R	R	R	R
R/W (HC)	R/W	R/W	R/W	R/W	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
31:0	CCED	Control Current ED Physical address of current ED of control list

11.3.12 HcBulkHeadED (offset address: 0x28)

Bit Position	31	30	29	28	27	26	25	24
Bit name	BHED	BHED	BHED	BHED	BHED	BHED	BHED	BHED
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	23	22	21	20	19	18	17	16
Bit name	BHED	BHED	BHED	BHED	BHED	BHED	BHED	BHED
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	15	14	13	12	11	10	9	8
Bit name	BHED	BHED	BHED	BHED	BHED	BHED	BHED	BHED
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	BHED	BHED	BHED	BHED	BHED	BHED	BHED	BHED
R/W (HCD)	R/W	R/W	R/W	R/W	R	R	R	R
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
31:0	BHED	Bulk Head ED Physical address of 1st ED of bulk list

11.3.13 HcBulkCurrentED (offset address: 0x2C)

Bit Position	31	30	29	28	27	26	25	24
Bit name	BCED	BCED	BCED	BCED	BCED	BCED	BCED	BCED
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	23	22	21	20	19	18	17	16
Bit name	BCED	BCED	BCED	BCED	BCED	BCED	BCED	BCED
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	15	14	13	12	11	10	9	8
Bit name	BCED	BCED	BCED	BCED	BCED	BCED	BCED	BCED
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	BCED	BCED	BCED	BCED	BCED	BCED	BCED	BCED
R/W (HCD)	R/W	R/W	R/W	R/W	R	R	R	R
R/W (HC)	R/W	R/W	R/W	R/W	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
31:0	BCED	Bulk Current ED Physical address of current ED of bulk list

11.3.14 HcDoneHead (offset address: 0x30)

Bit Position	31	30	29	28	27	26	25	24
Bit name	DH	DH	DH	DH	DH	DH	DH	DH
R/W (HCD)	R	R	R	R	R	R	R	R
R/W (HC)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	23	22	21	20	19	18	17	16
Bit name	DH	DH	DH	DH	DH	DH	DH	DH
R/W (HCD)	R	R	R	R	R	R	R	R
R/W (HC)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	15	14	13	12	11	10	9	8
Bit name	DH	DH	DH	DH	DH	DH	DH	DH
R/W (HCD)	R	R	R	R	R	R	R	R
R/W (HC)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	DH	DH	DH	DH	DH	DH	DH	DH
R/W (HCD)	R	R	R	R	R	R	R	R
R/W (HC)	R/W	R/W	R/W	R/W	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
31:0	DH	Done Head Physical address of TD added last to the Done queue (transfer completed queue)

11.3.15 HcFmInterval (offset address: 0x34)

Bit Position	31	30	29	28	27	26	25	24
Bit name	FIT	FSMPS	FSMPS	FSMPS	FSMPS	FSMPS	FSMPS	FSMPS
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	23	22	21	20	19	18	17	16
Bit name	FSMPS	FSMPS	FSMPS	FSMPS	FSMPS	FSMPS	FSMPS	FSMPS
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	FI	FI	FI	FI	FI	FI
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	1	0	1	1	1	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	FI	FI	FI	FI	FI	FI	FI	FI
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	1	0	1	1	1	1	1	1

Bit Position	Bit Name	Function
31	FIT	Frame Interval Toggle Inverted when loading a value to the FI area is performed.
30:16	FSMPS	FS Large Data Packet Maximum number of data bits that can be transmitted/received in single processing
15:14	RFU	Reserved. Write 0. Since the values of these bits become undefined after reset, initialize them by software.
13:0	FI	Frame Interval Bit time of 1 frame time width

11.3.16 HcFmRemaining (offset address: 0x38)

Bit Position	31	30	29	28	27	26	25	24
Bit name	FRT	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R/W	R	R	R	R	R	R	R
After reset	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	23	22	21	20	19	18	17	16
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	FR	FR	FR	FR	FR	FR
R/W (HCD)	R/W	R/W	R	R	R	R	R	R
R/W (HC)	R	R	R/W	R/W	R/W	R/W	R/W	R/W
After reset	Undefined	Undefined	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	FR	FR	FR	FR	FR	FR	FR	FR
R/W (HCD)	R	R	R	R	R	R	R	R
R/W (HC)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
31	FRT	Frame Remaining Toggle When the FR area becomes 0, the value of the FIT area of the HcFmInterval register is loaded.
30:14	RFU	Reserved. Write 0. Since the values of these bits become undefined after reset, initialize them by software.
13:0	FR	Frame Remaining Down counter indicating the remaining bit time of the current frame

11.3.17 HcFmNumber (offset address: 0x3C)

Bit Position	31	30	29	28	27	26	25	24
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	23	22	21	20	19	18	17	16
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	15	14	13	12	11	10	9	8
Bit name	FN	FN	FN	FN	FN	FN	FN	FN
R/W (HCD)	R	R	R	R	R	R	R	R
R/W (HC)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	FN	FN	FN	FN	FN	FN	FN	FN
R/W (HCD)	R	R	R	R	R	R	R	R
R/W (HC)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
31:16	RFU	Reserved. Write 0. Since the values of these bits become undefined after reset, initialize them by software.
15:0	FN	Frame Number Counter that is incremented when the HcFmRemaining register is reloaded.

11.3.18 HcPeriodicStart (offset address: 0x40)

Bit Position	31	30	29	28	27	26	25	24
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	23	22	21	20	19	18	17	16
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	PS	PS	PS	PS	PS	PS
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	PS	PS	PS	PS	PS	PS	PS	PS
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	Bit Name	Function
31:14	RFU	Reserved. Write 0. Since the values of these bits become undefined after reset, initialize them by software.
13:0	PS	Periodic Start Indicates the start of cycle list processing. The standard value is 0x3E67 counts (1 count = 0.1 ms).

11.3.19 HcLSThreshold (offset address: 0x44)

Bit Position	31	30	29	28	27	26	25	24
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	23	22	21	20	19	18	17	16
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	LST	LST	LST	LST
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	0	1	1	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	LST	LST	LST	LST	LST	LST	LST	LST
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0	0	1	0	1	0	0	0

Bit Position	Bit Name	Function
31:12	RFU	Reserved. Write 0. Since the values of these bits become undefined after reset, initialize them by software.
11:0	LST	LS Threshold This value and the FR area of the HcFmRemaining register are compared and whether low-speed transfer is possible before the EOF (End of Frame) is judged.

11.3.20 HcRhDescriptorA (offset address: 0x48)

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Bit Position	31	30	29	28	27	26	25	24
Bit name	POTPGT	POTPGT	POTPGT	POTPGT	POTPGT	POTPGT	POTPGT	POTPGT
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	1Note	1Note	1Note	1Note	1Note	1Note	1Note	1Note

Bit Position	23	22	21	20	19	18	17	16
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	NOCP	OCPM	DT	NPS	PSM
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	0Note	1Note	0Note	0Note	1Note

Bit Position	7	6	5	4	3	2	1	0
Bit name	NDP	NDP	NDP	NDP	NDP	NDP	NDP	NDP
R/W (HCD)	R	R	R	R	R	R	R	R
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0Note	0Note	0Note	0Note	0Note	0Note	1Note	1Note

Bit Position	Bit Name	Function
31:24	POTPGT	Poweron To Power Good Time Indicates the time during which HCD must wait prior to access to root hub ports to which current is applied.
23:13	RFU	Reserved. Write 0. Since the values of these bits become undefined after reset, initialize them by software.
12	NOCP	No Over Current Protection Whether overcurrent status is reported or not 1: Do not support overcurrent protection 0: Report overcurrent status
11	OCPM	Over Current Protection Mode Mode for overcurrent status report 1: Report in every report 0: Batch report for all downstream ports

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Note Only hardware reset is possible for bits 31 to 24 and bits 12 to 0.

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Bit Position	Bit Name	Function
10	DT	Device Type Indicates that the root hub is not a composite device.
9	NPS	No Power Switching Power application switching 1: Always apply power to ports when HC is ON. 0: Port power can be turned ON/OFF.
8	PSM	Power Switching Mode Mode for power application 1: Apply power to each port separately 0: Apply power to all ports at the same time
7:0	NDP	Number Downstream Ports Number of downstream ports supported by root hub

11.3.21 HcRhDescriptorB (offset address: 0x4C)

(1/2)

Bit Position	31	30	29	28	27	26	25	24
Bit name	PPCM	PPCM	PPCM	PPCM	PPCM	PPCM	PPCM	PPCM
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	1Note	1Note	1Note	1Note	1Note	1Note	1Note	1Note

Bit Position	23	22	21	20	19	18	17	16
Bit name	PPCM	PPCM	PPCM	PPCM	PPCM	PPCM	PPCM	PPCM
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	1Note	1Note	1Note	1Note	1Note	1Note	1Note	0Note

Bit Position	15	14	13	12	11	10	9	8
Bit name	DR	DR	DR	DR	DR	DR	DR	DR
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0Note	0Note	0Note	0Note	0Note	0Note	0Note	0Note

Bit Position	7	6	5	4	3	2	1	0
Bit name	DR	DR	DR	DR	DR	DR	DR	DR
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0Note	0Note	0Note	0Note	0Note	0Note	0Note	0Note

Bit Position	Bit Name	Function
31:16	PPCM	Reserved. Write 1. 1 returned when read.
18		Port Power Control Mask Masks a pair of power supply for port 2. 1: Mask 0: Do not mask
17		Port Power Control Mask Masks a pair of power supply for port 1. 1: Mask 0: Do not mask
16		Reserved. Write 0. 0 returned when read.

Note Only hardware reset is possible.

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Bit Position	Bit Name	Function
15:0	DR	Reserved. Write 0. 0 returned when read.
2		Device Removable Connection of device to port 2 1: Connected 0: Not connected
1		Device Removable Connection of device to port 1 1: Connected 0: Not connected
0		Reserved. Write 0. 0 returned when read.

11.3.22 HcRhStatus (offset address: 0x50)

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Bit Position	31	30	29	28	27	26	25	24
Bit name	CRWE	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	1 Note 1	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	23	22	21	20	19	18	17	16
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	OCIC	**Note 2**
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R/W	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	1 Note 1	0 Note 1

Bit Position	15	14	13	12	11	10	9	8
Bit name	**Note 2**	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0 Note 1	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	OCI	**Note 2**
R/W (HCD)	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
R/W (HC)	R	R	R	R	R	R	R/W	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	0 Note 1	0 Note 1

Notes 1. Only hardware reset is possible for bit 31, bits 17 to 15, and bits 1 and 0.

2. The name of these bits is different during HCD read and write.

The names of these bits are as follows.

Bit Position	Bit Name	
	During HCD Read	During HCD Write
16	LPSC	SGP
15	DRWE	SRWE
0	LPS	CGP

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Bit Position	Bit Name	Function
31	CRWE	Clean Remote Wakeup Enable 1: Clear the RWE bit of the HcControl register to 0 0: No change
30:18	RFU	Reserved. Write 0. Since the values of these bits become undefined after reset, initialize them by software.
17	OCIC	Over Current Indicator Change When a change occurs in the OCI bit, HC sets this bit to 1. This bit is cleared to 0 when HCD writes 1 to it. This bit remains unchanged when HCD writes 0 to it.
16	SGP[Note]	(During HCD write) Set Global Power 1: When the PSM bit of the HcRhDescriptorA register is 1, only the PPS bit of the HcRhPortStatus register of the ports that are not set by the PPCM area of the HcRhDescriptorB register is set to 1. When the PSM bit of the HcRhDescriptorA register is 0, the power to all ports is switched ON. 0: No change
	LPSC	(During HCD read, HC read) Local Power Status Change The root hub does not support the local power supply status.
15	SRWE[Note]	(During HCD write) Set Remote Wakeup Enable 1: Set RWE bit of the HcControl register 0: No change
	DRWE	(During HCD read, HC read) Device Remote Wakeup Enable 1: When the CSC bit of the HcRhPortStatus register becomes 1, this indicates a remote wakeup event. 0: When the CSC bit of the HcRhPortStatus register becomes 1, this indicates other than a remote wakeup event.
14:2	RFU	Reserved. Write 0. Since the values of these bits become undefined after reset, initialize them by software.
1	OCI	Over Current Indicator Wthether overcurrent status exists or not (when the overcurrent status is reported in batch for all downstream ports) 1: Overcurrent status exists 0: Current operation normal To report the overcurrent status individually for each port, clear this bit to 0.

Note These bits can be written only by HCD. The HC cannot read/write them.

(3/3)

Bit Position	Bit Name	Function
0	CGP[Note]	(During HCD write) Clear Global Power 1: When the PSM bit of the HcRhDescriptorA register is 1, only the PPS bit of the HcRhPortStatus register of the ports that are not set by the PPCM area of the HcRhDescriptorB register is cleared to 0. When the PSM bit of the HcRhDescriptorA register is 0, the power to all ports is switched OFF. 0: No change
	LPS	(During HCD read, HC read) Local Power Status The root hub does not support the local power supply status.

Note This bit can be written only by HCD. The HC cannot read/write it.

11.3.23 HcRhPortStatus 1 and 2 (offset address: 0x54, 0x58)

(1/4)

Bit Position	31	30	29	28	27	26	25	24
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W (HCD)	R	R	R	R	R	R	R	R
R/W (HC)	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	23	22	21	20	19	18	17	16
Bit name	RFU	RFU	RFU	PRSC	POCIC	PSSC	PESC	CSC
R/W (HCD)	R	R	R	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0Note 1	0Note 1	0Note 1	0Note 1	0Note 1

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	**Note 2**	**Note 2**
R/W (HCD)	R	R	R	R	R	R	R/W	R/W
R/W (HC)	R	R	R	R	R	R	R/W	R/W
After reset	0	0	0	0	0	0	UndefinedNote 1	0Note 1

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RFU	RFU	**Note 2**	**Note 2**	**Note 2**	**Note 2**	**Note 2**
R/W (HCD)	R	R	R	R/W	R/W	R/W	R/W	R/W
R/W (HC)	R	R	R	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0Note 1	0Note 1	0Note 1	0Note 1	0Note 1

Notes 1. Only hardware reset is possible for bits 20 to 16, bits 9 and 8, and bits 4 to 0.

2. The name of these bits is different during HCD and HC read and write.
The names of these bits are as follows.

Bit Position	Bit Name	
	During Read	During Write
9	LSDA	CPP
8	PPS	SPP
4	PRS	SPR
3	POCI	CSS
2	PSS	SPS
1	PES	SPE
0	CCS	CPE

(2/4)

Bit Position	Bit Name	Function
31:21	RFU	Reserved. Write 0. 0 returned when read.
20	PRSC	Port Reset Status Change This bit is set to 1 upon the end of the reset. It is cleared to 0 when the HCD writes 1 to it.
19	POCIC	Port Over Current Indicator Change This bit is set to 1 when the POCI bit changes. It is cleared to 0 when the HCD writes 1 to it.
18	PSSC	Port Suspend Status Change This bit is set to 1 upon the end of the Resume. It is cleared to 0 when the HCD writes 1 to it or when the PRSC bit is set to 1.
17	PESC	Port Enable Status Change This bit is set to 1 upon occurrence of overcurrent, port power-off by device disconnection, or operational errors such as bubble detection. It is cleared to 0 when the HCD writes 1 to it.
16	CSC	Connect Status Change This bit is set to 1 by writing 1 to the SPR bit, SPE bit, or SPS bit when the CCS bit is 0 or the bits corresponding to the DR area of the HcRhDescriptorB register are set and the CCS bit changes. It is cleared to 0 when the HCD writes 1 to it.
15:10	RFU	Reserved. Write 0. 0 returned when read.
9	CPP	(During write) Clear Port Power This bit is set to 1 by connecting a low-speed device. It is cleared to 0 when a full-speed device is connected.
	LSDA	(During read) Low-Speed Device Attached Speed of connected device 1: Low speed 0: Full speed

(3/4)

Bit Position	Bit Name	Function
8	SPP	(During write) Set Port Power This bit is set to 1 at the following times. • When the PSM bit of the HcRhDescriptorA register is 0 and the SGP bit of the HcRhStatus register becomes 1 • When the NPS bit and PSM bit of the HcRhDescriptorA register are 0 and 1, respectively, the bit corresponding to the PPCM area of the HcRhDescriptorB register is 0, so that the SGP bit of the HcRhStatus register becomes 1 • When the NPS bit is 0 and the PSM bit is 1, and the bit corresponding to the PPCM area is set to 1 This bit is cleared to 0 at the following times. • When the NPS and PSM bits are 0, and the CGP bit of the HcRhStatus register is set to 1 • When the NPS bit is 0 and the PSM bit is 1, and the bit corresponding to the PPCM area is 0 and the CGP bit is set to 1 • When the NPS bit is 0 and the PSM bit is 1, and the bit corresponding to the PPCM area is 1 and the CPP bit is set to 1 • When overcurrent occurs
	PPS	(During read) Port Power Status Status of the port power 1: ON 0: OFF
7:5	RFU	Reserved. Write 0. 0 returned when read.
4	SPR	(During write) Set Port Reset This bit is set to 1 when the HCD writes 1 while the CCS bit is 1. This bit is cleared to 0 when the PRSC bit is set to 1 and the HCFS area of the HCControl register is 01, or when the power to a port is switched OFF.
	PRS	(During read) Port Reset Status Status of port reset signal 1: Active 0: Inactive
3	CSS	(During write) Clear Suspend Status This bit is set to 1 when an overcurrent occurs while the NOCP bit and OCPM bit of the HcRhDescriptorA register is 0 and 1, respectively. It is cleared to 0 by canceling the set condition.
	POCI	(During read) Port Over Current Indicator Occurrence of overcurrent 1: Occurred 0: Normal

(4/4)

Bit Position	Bit Name	Function
2	SPS	(During write) Set Port Suspend This bit is set to 1 when the HCD writes 1 while the CCS bit is 1. This bit is cleared to 0 when the port power is switched OFF while the PSSC bit is set to 1, or the PRSC bit is set to 1, and the HCFS area of the HcControl register is 01.
	PSS	(During read) Port Suspend Status Suspension of port 1: Suspended 0: Not suspended
1	SPE	(During write) Set Port Enable This bit is set to 1 when the HCD writes 1 while CCS bit is 1, or when the PRSC bit is set, or when the PSSC bit is set to 1. This bit is cleared to 0 when the CPE bit is set to 1 or upon occurrence of overcurrent, port power-off by device disconnection, or operational errors such as bubble detection.
	PES	(During read) Port Enable Status Port status 1: Enable 0: Disable
0	CPE	(During write) Clear Port Enable This bit is set to 1 when a device is connected. This bit is cleared to 0 when a device is disconnected or when the power to a port is switched OFF.
	CCS	(During read) Current Connect Status Current status of downstream port 1: Device is connected 0: Device is not connected

CHAPTER 12 PS/2 CONTROLLER

The PS/2 controller controls bi-directional data transfer using the PS2CLK and PS2DATA signals.

12.1 Register Set

Table 12-1 lists the PS/2 registers.

Table 12-1. PS/2 Registers

Address	R/W	Symbol	Function
0x1500 3870	R/W	PS2DATA	PS/2 transmit/receive data register
0x1500 3872	R/W	PS2CTRL	PS/2 control register

The details of these registers are shown next.

12.1.1 PS2DATA (0x1500 3870)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit Position	7	6	5	4	3	2	1	0
Bit name	PSDATA7	PSDATA6	PSDATA5	PSDATA4	PSDATA3	PSDATA2	PSDATA1	PSDATA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

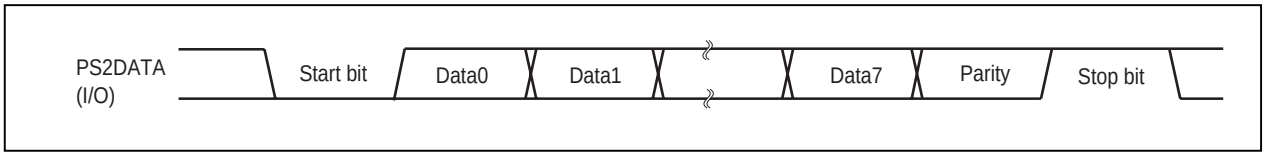
Bit Position	Bit Name	Function
15:8	RFU	Reserved. Write 0. Since the values of these bits become undefined after reset, initialize them by software.
7:0	PSDATA (7:0)	PS2 transmit/receive data During write: Transmit data During read: Receive data

This register is used to store the transmit data output from the PS2DATA pin and read the receive data input to the PS2DATA pin.

Receive data can be obtained by reading this register.

Using the PS/2 controller, the data can be transmitted or received in the following pattern.

Figure 12-1. Data Pattern



12.1.2 PS2CTRL (0x1500 3872)

Bit Position	15	14	13	12	11	10	9	8
Bit name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
R/W	R	R	R	R	R	R	R	R
After reset	0	0	0	0	0	0	0	0

Bit Position	7	6	5	4	3	2	1	0
Bit name	RFU	RFU	PERR	RVEN	INTEN	PS2EN	TEMT	REMT
R/W	R	R	R	R/W	R/W	R/W	R	R
After reset	0	0	Undefined	0	0	0	0	0

Bit Position	Bit Name	Function
15:6	RFU	Reserved. Write 0. 0 returned when read.
5	PERR	Receive data parity error detection (Enabled only when the REMT bit is 1, odd parity) 1: Error 0: No error
4	RVEN	Receive FIFO used/not used 1: Used 0: Not used
3	INTEN	Interrupt detection enable 1: Enable 0: Disable
2	PS2EN	PS2 interface enable 1: Disable 0: Enable
1	TEMT	Transmit data ready 1: Transmit data exists 0: No transmit data
0	REMT	Receive data ready 1: Receive data exists 0: No receive data

This register indicates the control settings for the PS/2 interface and the status information.

When the PS2EN bit is set to 0, data transmit/receive to/from the PS/2 interface becomes possible. When the RVEN bit is 1, receive FIFO (8 bits × 8 rows) is used. When data is received from external, the REMT bit becomes 1, which indicates that receive data exists in the PS2DATA register. This bit is cleared to 0 by reading the receive data. When the receive FIFO is used, this bit is cleared to 0 when all the receive data has been read and the FIFO has become empty.

The INTEN bit controls receive end interrupt request detection enable/disable. When the INTEN bit is 1, upon completion of a pair of data receive operations from the PS2DATA pin, an interrupt request is notified to the VR4121 at the same time as the REMT bit is set to 1. When the VR4121 reads receive data from the PS2DATA register, the interrupt request signal is made inactive.

The PERR bit is set to 1 when a parity error occurs in the receive data. Be sure to check the PERR bit prior to reading the receive data.

12.2 Transmit Procedure

The transmit procedure is described below.

1. Set the PS2EN bit to 1 to disable reception.
2. Check that the PS2EN bit is set to 1.
3. If receive data exists, read all the receive data.
4. Set the transmit data to the PS2DATA register.
5. Set the PS2EN bit to 0 to start transmission.
6. Poll the TEMT bit to check that the transmission has ended.

CHAPTER 13 CONNECTION WITH VR4121

This chapter describes how to connect the VRC4172 and the VR4121.

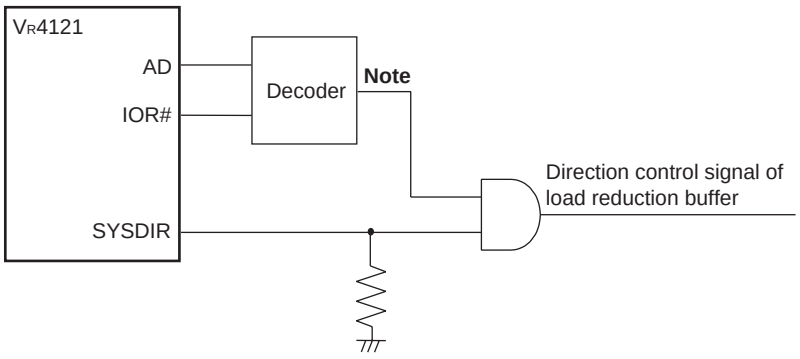
When connecting the VRC4172 and the VR4121, connect the pins corresponding to the following signals using wired OR connection.

SCLK	AD (0:24)
DATA (0:31)	RD#
WR#	ROMCS (2:3)#
CKE	UUCAS#
ULCAS#	MRAS (0:1)#
UCAS#	LCAS#

If a load reduction buffer is used, connect to the inner side of the load reduction buffer (VR4121). Moreover, set the bits 1 and 0 of the BCUCNTREG3 register of the VR4121 to 1 according to the address of the PCI master window of the VRC4172. Note that, in this case, the SYSDIR signal of the VR4121 cannot be used as is as the direction control signal of the load reduction buffer.

Figure 13-1 shows an example of a SYSDIR signal circuit when a load reduction buffer is used.

Figure 13-1. Example of SYSDIR Signal (VR4121) Circuit When Using Load Reduction Buffer



Note Low level during read access to internal registers of the VRC4172.

13.1 Load Reduction Buffer Control

(1) HLDACK# pin (VR4121)

Controls the buffer direction used for the address bus.

1: VR4121 → External I/O device (including VRC4172)

0: External I/O device → VR4121 (when CKE signal = 0)

VRC4172 → VR4121 (when CKE signal = 1)

(2) SYSDIR pin (VR4121)

Controls the buffer direction used for the data bus.

1: External I/O device (not including VRC4172) → VR4121

0: VR4121 → External I/O device (not including VRC4172)

Note When HLDAK# = 0, pull down the SYSDIR pin so that SYSDIR = 0.

(3) CKE pin (VR4121)

Buffer operation enable

1: Disable

0: Enable

13.2 Cautions When Connecting Load Reduction Buffer

Observe the following points when connecting a load reduction buffer.

- The CKE signal can be used to control operation enable only when the SCLK bit of the SDRAMMODEREG register of the VR4121 is 0.
- When the operation is disabled, the load reduction buffer goes into the high-impedance status. Therefore, implement protective measures such as adding pull-up or pull-down resistors to the external I/O device.

CHAPTER 14 INTERRUPT SIGNALS

The VRC4172 has 6 interrupt notification signals, IRQ, INTRP, PS2INT, USBINT#, WAKE, and SMI#. The interrupt source detection block of each interrupt signal is shown in Table 14-1. For the generation source, refer to the chapter of each detection block.

Table 14-1. Interrupt Signals

Signal Name	Interrupt Detection Block
IRQ	GPIO or IEEE1284 parallel controller[Note]
INTRP	16550 serial controller or IEEE1284 parallel controller[Note]
PS2INT	PS/2 controller
USBINT#	USB host controller (INTA# signal (internal PCI bus signal))
WAKE	USB host controller
SMI#	USB host controller

Note Specify either one of them to be allocated with bits 3 and 2 of the 1284INTRQ register (0x1500 3808).

[MEMO]

CHAPTER 15 RESET

There are two types of reset, hardware reset and software reset, by external pins (RESET, USBRST# pins).

The USBRST# signal is the reset signal for the USB host controller and the internal PCI bus controller (including the SDRAM controller), and the RESET signal is the reset signal for the other blocks.

Reset to the various blocks of the 16550 serial controller, IEEE1284 parallel controller, and PS/2 controller starts when the RESET signal becomes active, but these blocks are reset even if the RESET signal becomes inactive. To cancel reset, set bit 1 of the 1284CTRL register, 16550CTRL register, and PS2PWMCTRL register of the PMU to 0.

Software reset consists of reset to the internal PCI bus and reset to the IEEE1284 parallel controller, 16550 serial controller, and PS/2 controller blocks.

Software reset to the internal PCI bus is started by setting the PCIRSTGO bit of the command register of the PCI host controller to 1. This reset is automatically cancelled after the lapse of a given time. The register values of the PCI bus controller is held.

At power-on, always make the RESET and USBRST# signals active to initialize the entire VRC4172.

The registers that are initialized when RESET = 1 are listed below.

- GPIO registers
- PCS registers
- PMU registers
- 16550 serial controller registers
- IEEE1284 parallel controller registers
- PS/2 controller registers
- PWM controller registers

The registers that are initialized when the IRST bit of the SYSCLKCTRL register of the PMU is 1 are listed below.

- GPIO registers
- PCS registers
- PMU registers other than SYSCLKCTRL register
- 16550 serial controller registers
- IEEE1284 parallel controller registers
- PS/2 controller registers
- PWM controller registers

The registers that are initialized when USBRST# = 0 are listed below.

- PCI configuration address register
- PCI configuration data register
- PCI host control register
- USB host controller registers

[MEMO]

CHAPTER 16 USAGE CAUTIONS

The following usage cautions apply to the use of the VRC4172.

16.1 Power Supply Control

(1) Linkage with SDRAM power supply

If the 3.3 V power supply of the VR4121 and the power supply system of the SDRAM are separated and the system is designed so that the power supply to the SDRAM is switched ON after using the SPOWER pin of the VR4121, link the power supply of the VRC4172 with that of the SDRAM.

(2) Pull-up of SDRAM-related pins

In the case of the VRC4172, the SDRAM-related pins (WR#, ROMCS (2:3)#, UUCAS#, ULCAS#, MRAS (0:1)#, UCAS#, LCAS#, SRAS#, SCAS#) must be pulled up (refer to **2.3.2 External processing of pins and drive performance**). Connect pull-up resistors to the power supplies of the SDRAM and VRC4172. This is a measure to prevent that, when the bus mastership is passed from the VR4121 to the VRC4172 (or vice-versa), the SDRAM-related pins go into high impedance, causing erroneous SDRAM operation, and to prevent that those pins that are I/O pins of the VRC4172 are open while in high impedance.

If these countermeasures are not implemented, the voltage is applied due to the operation of the pull-up resistors provided for the VRC4172's SDRAM control pins when the SDRAM power supply is switched OFF. Note that if the pull-up resistors are extremely small, the SDRAM may get damaged.

16.2 Reset Pins

Design the system so that the VRC4172's USBRST# and RESET pins become active at the same time immediately following power application, or else the VRC4172 bus and the VR4121 bus may conflict immediately after power application.

16.3 Cautions on VR4121 Suspend Mode

If the BUSCLK pin of the VR4121 is connected to the BUSCLK pin of the VRC4172, the BUSCLK signal stops being supplied when the VR4121 goes into the Suspend mode. This causes the internal bus arbiter of the VRC4172 controlled by the BUSCLK signal to not function, and makes it impossible to make the HLDRQ# signal from the VRC4172 to the VR4121 active when USB data is transmitted/received. Therefore, when the VR4121 goes into the Suspend mode, connect the ARBCLKSEL pin of the VRC4172 to VDD (Since the ARBCLKSEL pin is pulled down internally, in order to use this function, the ARBCLKSEL pin must be connected directly to VDD instead of being pulled up).

If the ARBCLKSEL pin is connected to VDD, the VRC4172 internal bus arbiter operates on an 8 MHz clock obtained by dividing the internal 48 MHz clock, so that the VRC4172 internal bus arbiter operation is enabled.

★ 16.4 Preserving SDRAM Data

As SDRAM data may be corrupted in the following cases, be sure to take the appropriate countermeasures.

(1) When SDRAM is accessed using the USB function in VR4121 Suspend mode

When the VR4121 enters Suspend mode, a self-refresh command is issued to SDRAM, and while the VR4121 is in Suspend mode, the bus can be released via a bus hold request. When the USB function of the VRC4172 is used, therefore, SDRAM can be accessed even while the VR4121 is in Suspend mode. If, however, the VRC4172 issues a bus hold request to the VR4121 while it is in Suspend mode (SDRAM self-refresh mode) triggering the start of SDRAM access, the CKE signal will become high level, causing the self-refresh command for SDRAM to be inadvertently canceled. This command cancellation cannot be recognized by the VR4121, so if this state continues for a long period of time, SDRAM data may be corrupted due to insufficient refreshing.

To avoid this situation, when using the USB function of the VRC4172 while the VR4121 is in Suspend mode, input an external interrupt request to the VR4121 at the same time as the HLDRQ# signal becomes active to shift the VR4121 from Suspend mode to FullSpeed mode.

(2) When accessing SDRAM while the RSTSW# signal (VR4121) is active

If the VRC4172 accesses SDRAM and a bus hold occurs in the period between when RSTSW# (VR4121) becomes active and when the VR4121 is actually reset (about 90 μs), the refresh command for SDRAM will be canceled. In this case, because the refresh command will not be issued while the RSTSW# signal is active, if RSTSW# remains active for a long period of time, SDRAM data may be corrupted due to insufficient refreshing.

To avoid this situation, reshape the RSTSW# waveform into a one-shot pulse to ensure that the RSTSW# signal is active in the VR4121 for only a short pulse width, even if the RSTSW# switch is pressed for a long period of time. Three RTC clocks (about 100 μs) is necessary for the pulse width of the RSTSW#.

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