MEMORY PRODUCTS

DATA BOOK

Spring 1996

Dynamic

RAM

Modules

NEC

NEC Electronics Inc.

NEC

Dynamic RAM Module

Spring 1996 Data Book

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Index

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

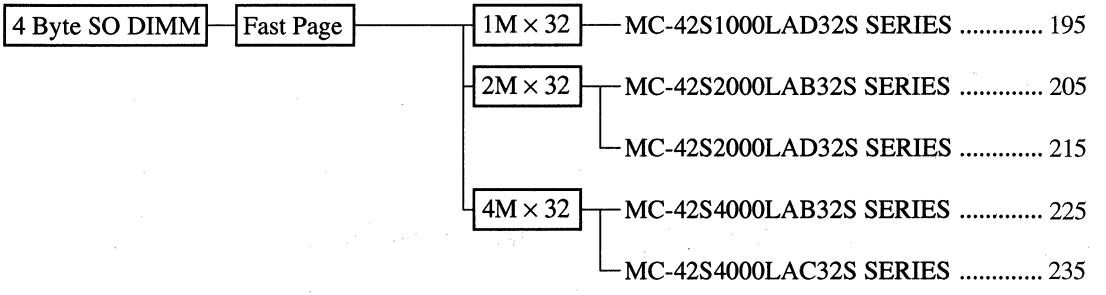
② HANDLING OF UNUSED INPUT PINS FOR CMOS

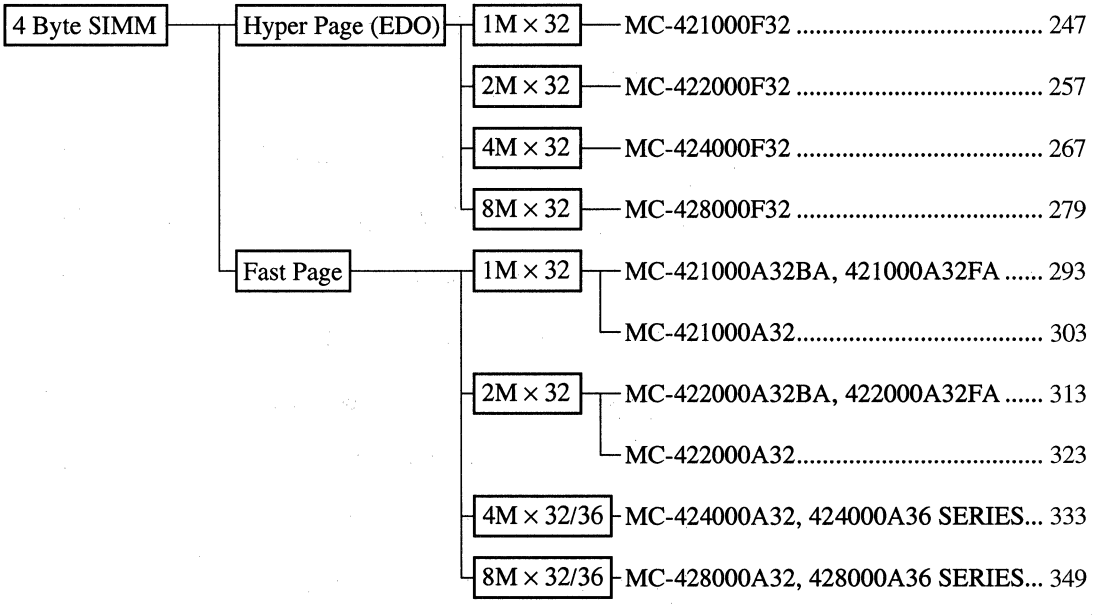
Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Contents

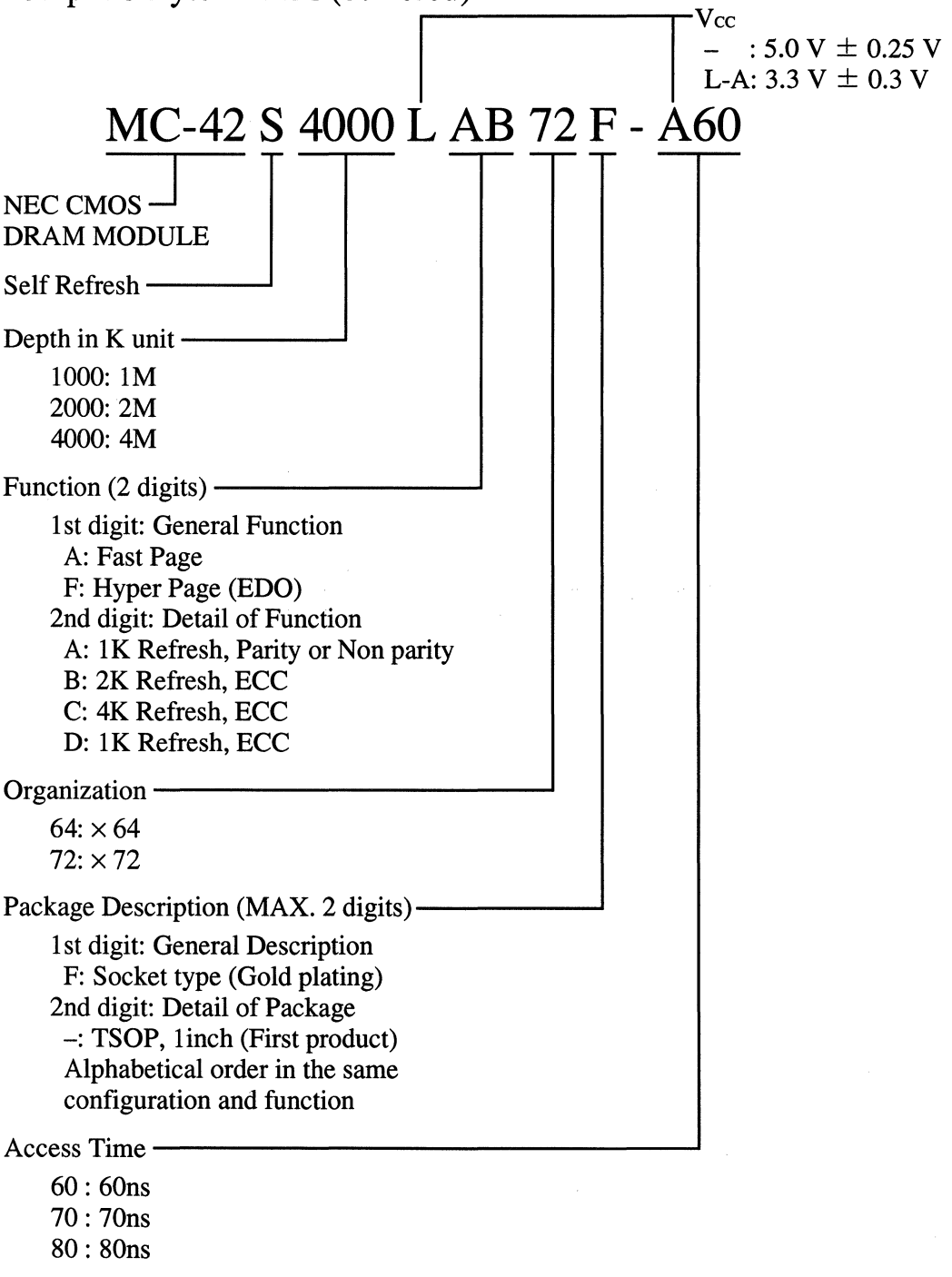




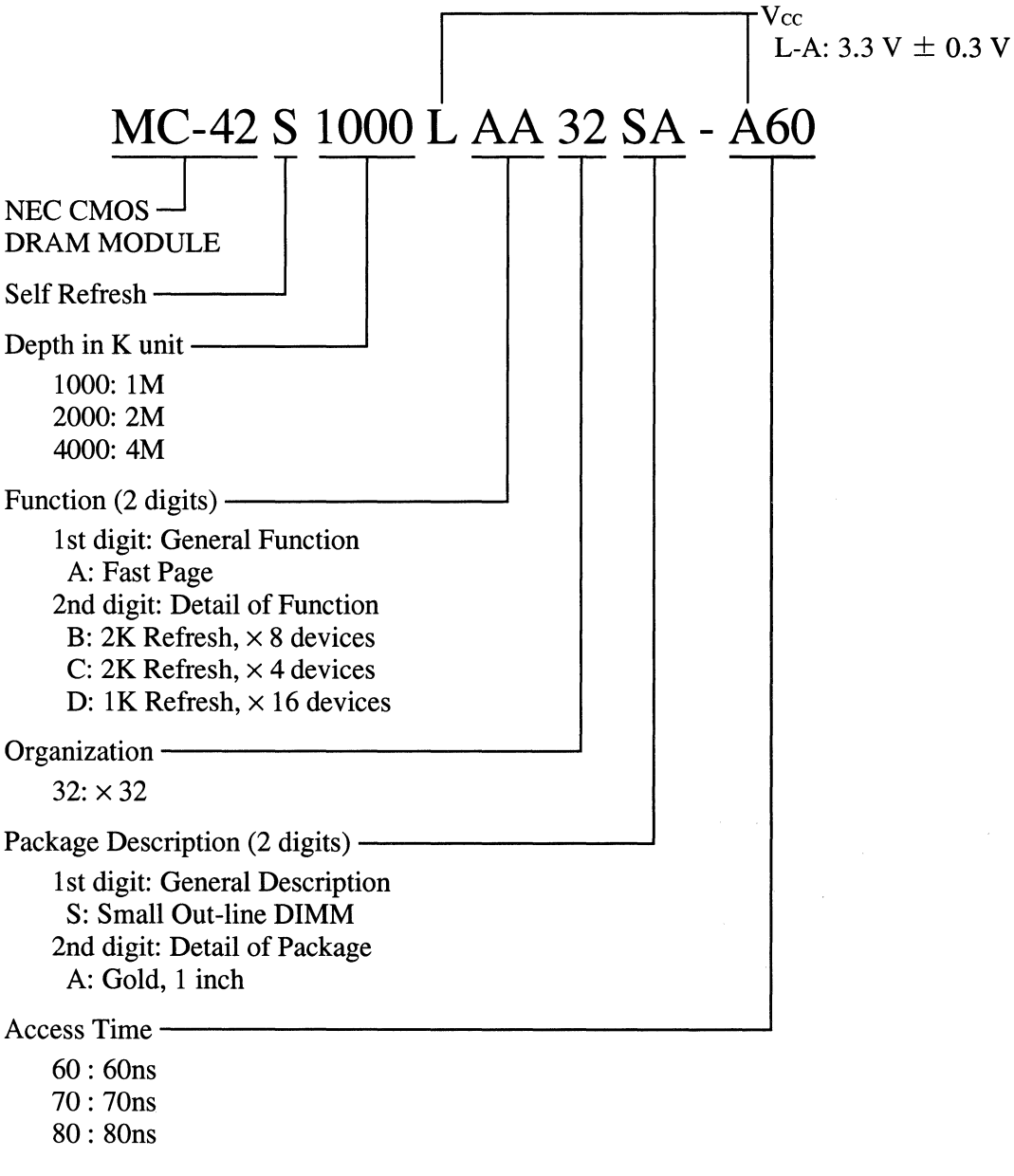
Selection Guide

Part Number

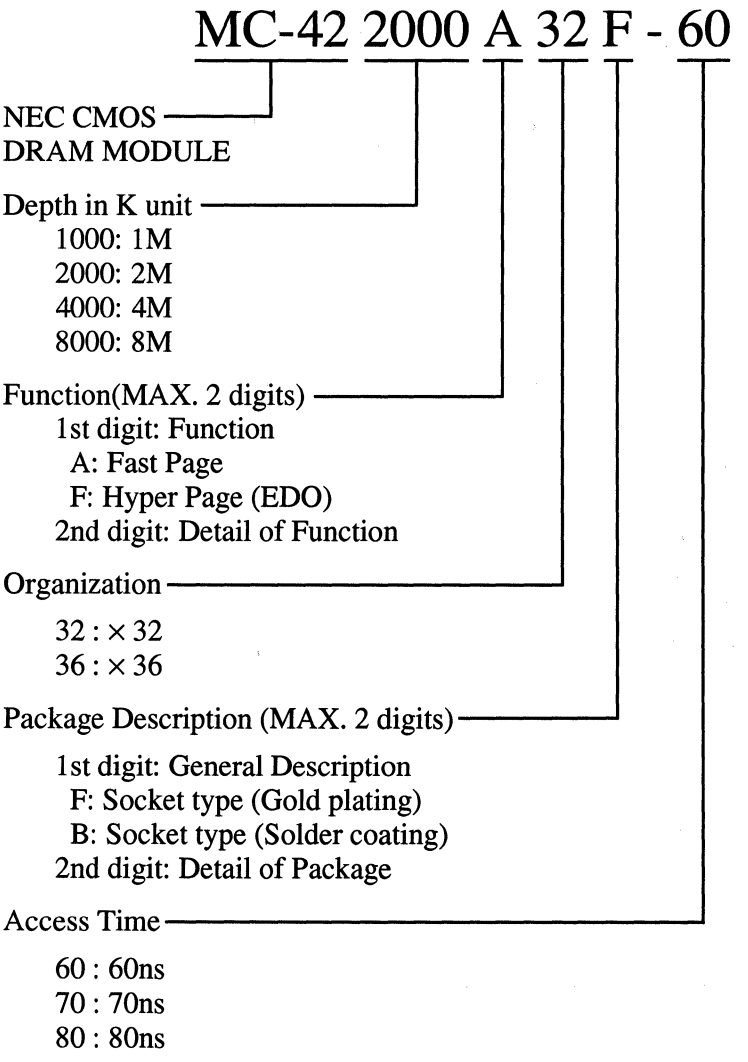
168-pin 8 Byte DIMM (buffered)

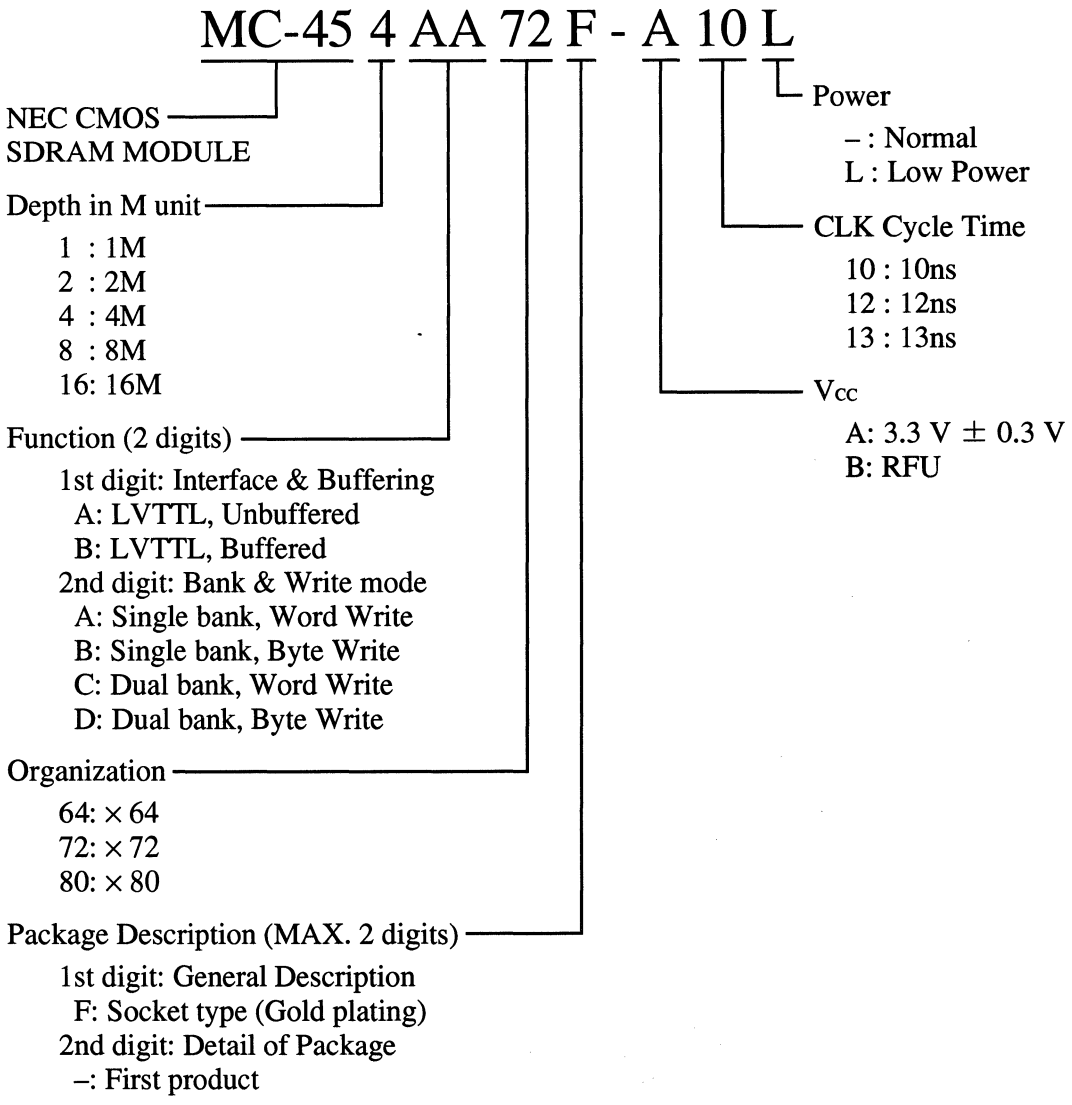


72-pin 4 Byte SO DIMM



72-pin 4 Byte SIMM




MC-45 4 AA 72 F - A 10 L
NEC CMOS SDRAM MODULE
Depth in M unit
1 : 1M
2 : 2M
4 : 4M
8 : 8M
16: 16M
Function (2 digits)
1st digit: Interface & Buffering
A: LVTTL, Unbuffered
B: LVTTL, Buffered
2nd digit: Bank & Write mode
A: Single bank, Word Write
B: Single bank, Byte Write
C: Dual bank, Word Write
D: Dual bank, Byte Write
Organization
64: × 64
72: × 72
80: × 80
Package Description (MAX. 2 digits)
1st digit: General Description
F: Socket type (Gold plating)
2nd digit: Detail of Package
–: First product
Vcc
A: 3.3 V ± 0.3 V
B: RFU
CLK Cycle Time
10 : 10ns
12 : 12ns
13 : 13ns
Power
– : Normal
L : Low Power

168-pin 8 Byte DIMM Hyper Page (EDO) Line-up

Organization	Part Number	Access Time (ns)	Refresh Cycle	Supply Voltage	Package			Monolithic Device			Page
					Mounted side	Edge connector	Height	Org.	Pkg.	Amt.	
1M × 64	MC-421000FA64FB	60, 70	1 K/16 ms	5.0 ± 0.5 V	Single side	Gold plated	1 inch	1M × 16	400 mil SOJ	2	17
2M × 64	MC-422000FA64FB	60, 70			Double side			1M × 16	400 mil SOJ	4	29
2M × 72	MC-422000FB72F	60, 70	2 K/32 ms		Double side			2M × 8	400 mil TSOP	9	41
	MC-422000LFB72F			3.3 ± 0.3 V							53
4M × 72	MC-424000FC72F	60, 70	4 K/64 ms	5.0 ± 0.5 V	Double side			4M × 4	300 mil TSOP	18	65
	MC-424000LFC72F			3.3 ± 0.3 V							77
8M × 72	MC-428LFC72F	60, 70	4 K/64 ms	3.3 ± 0.3 V	Single side		1.5 inch	8M × 8	400 mil TSOP	9	†
	MC-428LFF72F		8 K/64 ms								

† See NEC salesman for device availability.

168-pin 8 Byte DIMM Fast Page Line-up

Organization	Part Number	Access Time (ns)	Refresh Cycle	Supply Voltage	Package		Monolithic Device			Page
					Edge connector	Height	Org.	Pkg.	Amt.	
1M × 64	MC-421000AA64FA	60, 70, 80	1 K/16 ms	5.0 ± 0.25 V	Gold plated	1 inch	1M × 4	300 mil SOJ	16	91
	MC-421000AA64FB	60, 70, 80					1M × 16	400 mil SOJ	4	103
2M × 64	MC-422000AA64FB	60, 70, 80					1M × 16	400 mil SOJ	8	123
1M × 72 ECC	MC-421000AD72F	60, 70, 80					1M × 16 1M × 4	400 mil TSOP 300 mil TSOP	4 2	113
2M × 72 ECC	MC-422000AB72F	60, 70, 80	2 K/32 ms				2M × 8	400 mil TSOP	9	133
	MC-422000LAB72F	60, 70, 80		3.3 ± 0.3 V			2M × 8	400 mil TSOP	9	143
4M × 72 ECC	MC-424000AB72F	60, 70, 80		5.0 ± 0.25 V			4M × 4	300 mil TSOP	18	153
	MC-424000LAB72F	60, 70, 80		3.3 ± 0.3 V			4M × 4	300 mil TSOP	18	173
	MC-424000AC72F	60, 70, 80	4 K/64 ms	5.0 ± 0.25 V			4M × 4	300 mil TSOP	18	163
8M x 72 ECC	MC-428000LAF72	50, 60, 70	8 K/64 ms 4 K/64 ms	3.3 ± 0.3 V	Gold plated	1.25 inch	8M x 8	400 mil SOJ	9	183

144-pin 8 Byte Small Outline DIMM Hyper Page (EDO) Line-up

Organization	Part Number	Access Time (ns)	Refresh Cycle	Bank org.	Supply Voltage	Package	Mounted Device			Page
							Org.	Pkg.	Amt.	
1M × 64	MC-421LFA64SA	60, 70	1 K/16 ms	1	3.3 ± 0.3 V	144-pin SOD Gold plated	1M × 16	400 mil TSOP	4	See NEC salesman for device availability.
	MC-42S1LFA64SA		1 K/128 ms	1				400 mil TSOP	4	
2M × 32	MC-422LFB64SA	60, 70	2 K/16 ms	1			2M × 8	400 mil TSOP	8	
	MC-42S2LFB64SA		2 K/128 ms	1				400 mil TSOP	8	
4M × 32	MC-424LFC64SA	60, 70	4 K/64 ms	1			4M × 16	400 mil TSOP	16	

72-pin 4 Byte Small Outline DIMM Fast Page Line-up

Organization	Part Number	Access Time (ns)	Refresh Cycle	Bank org.	Supply Voltage	Package	Monolithic Device			Page
							Org.	Pkg.	Amt.	
1M × 32	MC-42S1000LAD32SA	60, 70, 80	1 K/128 ms	1	3.3 ± 0.3 V	72-pin SOD Gold plated	1M × 16	400 mil TSOP	2	195
2M × 32	MC-42S2000LAB32SA	60, 70, 80	2 K/128 ms	1			2M × 8	400 mil TSOP	4	205
	MC-42S2000LAD32SA		1 K/128 ms	2			1M × 16	400 mil TSOP	4	215
4M × 32	MC-42S4000LAB32SA	60, 70, 80	2 K/128 ms	2			2M × 8	400 mil TSOP	8	225
	MC-42S4000LAC32SA			1			4M × 4	300 mil TSOP	8	235

72-pin 4 Byte SIMM Hyper Page (EDO) Line-up

Organization	Part Number	Access Time (ns)	Refresh Cycle	Supply Voltage	Package			Monolithic Device			Page
					Mounted side	Edge connector	Height	Org.	Pkg.	Amt.	
1M × 32	MC-421000F32BA	60, 70	1 K/16 ms	5.0 ± 0.5 V	Single side	S/C	1 inch	1M × 16	400 mil SOJ	2	247
	MC-421000F32FA					G/P					
2M × 32	MC-422000F32BA	60, 70			Double side	S/C		1M × 16	400 mil SOJ	4	257
	MC-422000F32FA					G/P					
4M × 32	MC-424000F32B	60, 70	2 K/32 ms		Single side	S/C		4M × 4	300 mil SOJ	8	267
	MC-424000F32F					G/P					
8M × 32	MC-428000F32B	60, 70			Double side	S/C		4M × 4	300 mil SOJ	16	279
	MC-428000F32F					G/P					

S/C: Solder Coated, G/P: Gold Plated

72-pin 4 Byte SIMM Fast Page Line-up (× 32)

Organization	Part Number	Access Time (ns)	Refresh Cycle	Supply Voltage	Package			Monolithic Device			Page
					Mounted side	Edge connector	Height	Org.	Pkg.	Amt.	
1M × 32	MC-421000A32B	60, 70, 80	1 K/16 ms	5.0 ± 0.5 V	Single side	S/C	1 inch	1M × 4	300 mil SOJ	8	303
	MC-421000A32F					G/P					
	MC-421000A32BA	60, 70, 80			Single side	S/C		1M × 16	400 mil SOJ	2	293
	MC-421000A32FA					G/P					
2M × 32	MC-422000A32B	60, 70, 80			Double side	S/C		1M × 4	300 mil SOJ	16	323
	MC-422000A32F					G/P					
	MC-422000A32BA	60, 70, 80			Double side	S/C		1M × 16	400 mil SOJ	4	313
	MC-422000A32FA					G/P					
4M × 32	MC-424000A32B	60, 70, 80	2 K/32 ms		Single side	S/C		4M × 4	300 mil SOJ	8	333
	MC-424000A32F					G/P					
8M × 32	MC-428000A32B	60, 70, 80			Double side	S/C		4M × 4	300 mil SOJ	16	349
	MC-428000A32F					G/P					

S/C: Solder Coated, G/P: Gold Plated

72-pin 4 Byte SIMM Fast Page Line-up (× 36)

Organization	Part Number	Access Time (ns)	Refresh Cycle	Supply Voltage	Package			Monolithic Device			Page
					Mounted side	Edge connector	Height (inch)	Org.	Pkg.	Amt.	
4M × 36	MC-424000A36BJ	60, 70, 80	2K/32 ms	5.0 ± 0.5 V	Single side	S/C	1.25	4M × 4 4M × 1	300 mil SOJ 300 mil SOJ	8 4	333
	MC-424000A36FJ					G/P					
	MC-424000A36BE				Double side	S/C	1.0	4M × 4 4M × 1	300mil SOJ 300mil SOJ	8 4	333
	MC-424000A36FE					G/P					
8M × 36	MC-428000A36BJ	60, 70, 80			Double side	S/C	1.25	4M × 4 4M × 1	300 mil SOJ 300 mil SOJ	16 8	349
	MC-428000A36FJ					G/P					

S/C: Solder Coated, G/P: Gold Plated

200-pin SDRAM DIMM (buffered) Line-up

	Organization	Part Number	Bank Org.	Min.Cycle time (ns)	Supply Voltage	Package		Monolithic Device		Page
						Edge connector	Height	Org.	Amt.	
Unbuffered	2M × 72	MC-452AA72F	1	10 (100 MHz) 12 (83 MHz) 13 (77 MHz)	3.3 ± 0.3 V	Gold plated	29.2 mm	2M × 8	9	See NEC salesman for device availability.
Buffered	2M × 72	MC-452BA72F	1				38.1 mm	2M × 8	9	
	2M × 80	MC-452BA80F	1					2M × 8	10	
	4M × 72	MC-454BA72F	1					4M × 4	18	
		MC-454BC72F	2					2M × 8	18	
	4M × 80	MC-454BA80F	1					4M × 4	20	

168-pin SDRAM DIMM (unbuffered) Line-up

Organization	Part Number	Clock (MHz)	Access Time (ns)	Refresh Cycle	Bank org.	Supply Voltage	Package	Monolithic Device			Page
								Org.	Pkg.	Amt.	
1M × 64	MC-451AB64F	83 MHz	10 ns	2 K/32 ms	1	3.3 ± 0.3 V	Gold plated	1M × 16	400 mil TSOP	4	See NEC salesman for device availability.
2M × 64	MC-452AB64F	75 MHz			1			2M × 8		8	
2M × 72	MC-452AA72F	67 MHz			1			2M × 8		9	
4M × 64	MC-454AB64F	60 MHz			1			4M × 4		16	
4M × 72	MC-454AA72F				1			4M × 4		18	

8 Byte DIMM
[Hyper Page (EDO)]

NEC

MOS INTEGRATED CIRCUIT

MC-421000FA64

1 M-WORD BY 64-BIT DYNAMIC RAM MODULE HYPER PAGE MODE (EDO)

Description

The MC-421000FA64 is a 1,048,576 words by 64 bits dynamic RAM module on which 4 pieces of 16 M DRAM: μPD4218165 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 1,048,576 words by 64 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC-421000FA64-60	60 ns	104 ns	25 ns	3.68 W	336 mW (CMOS level input)
MC-421000FA64-70	70 ns	124 ns	30 ns	3.47 W	

- 1,024 refresh cycles/16 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

Ordering Information

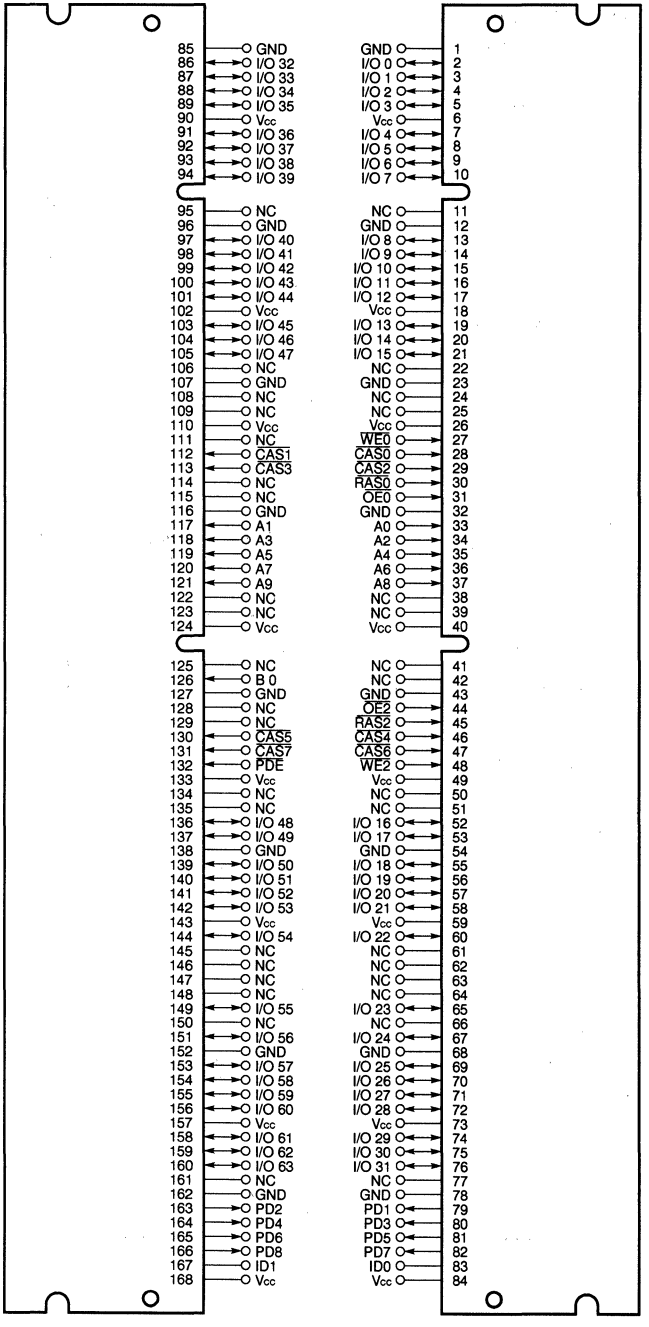
Part number	Access time (MAX.)	Package	Mounted devices
MC-421000FA64-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	4 pieces of μPD4218165LE (400 mil SOJ) [Single side]
MC-421000FA64-70	70 ns		

The information in this document is subject to change without notice.

Document No. M10519EJ2V0DSU1

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



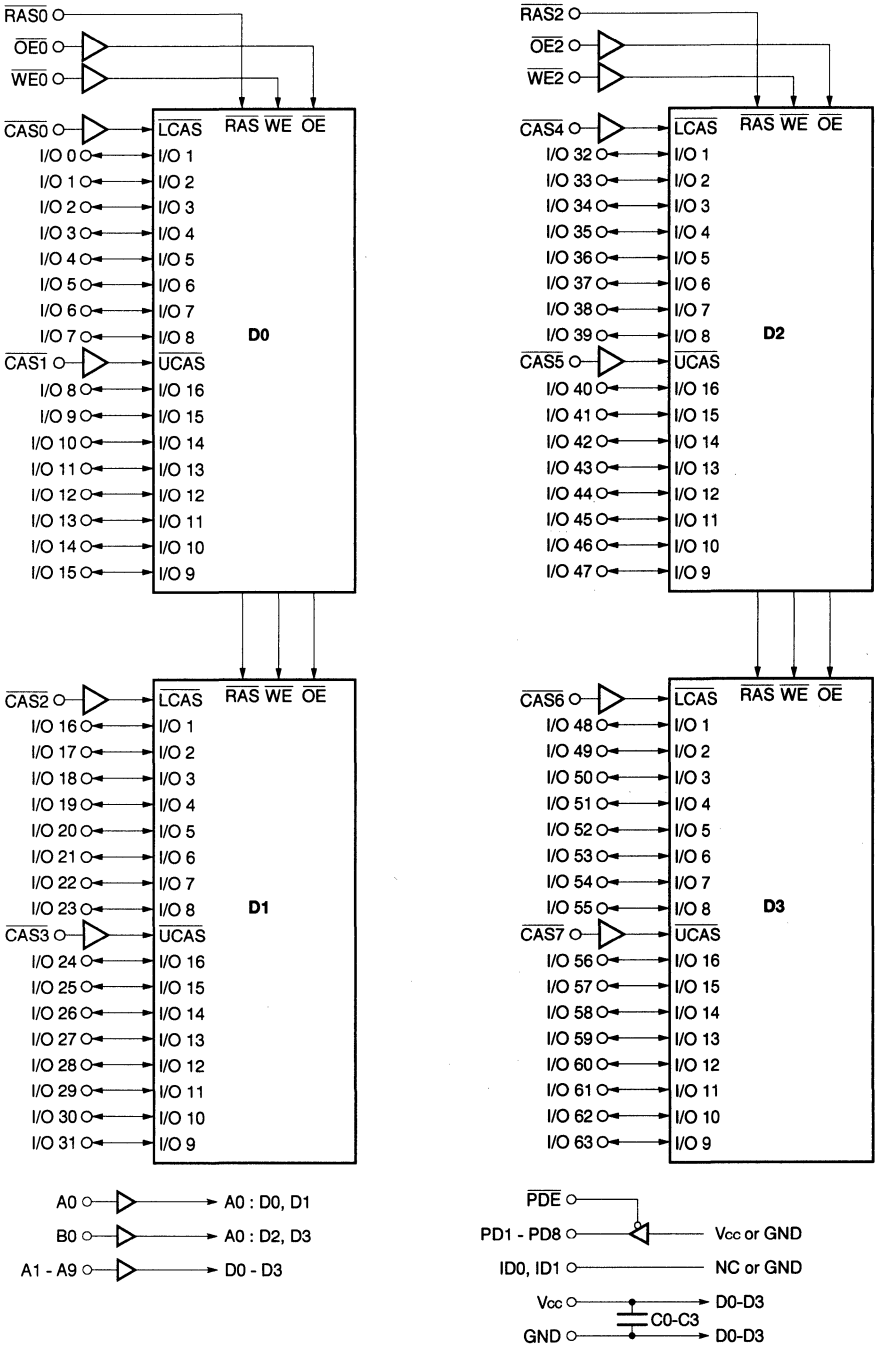
PD and ID Table

Pin Name	Pin No.	Access Time	
		60 ns	70 ns
PD1	79	L	L
PD2	163	L	L
PD3	80	H	H
PD4	164	L	L
PD5	81	H	H
PD6	165	H	L
PD7	82	H	H
PD8	166	H	H
ID0	83	GND	GND
ID1	167	GND	GND

Remark H: V_{OH}, L: V_{OL}

A0 - A9, B0 : Address Inputs
I/O 0 - I/O 63 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D3: μPD4218165

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		6	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Ao - A9, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			45	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS7}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data input/output capacitance	$C_{I/O}$	I/O0 - I/O63			20	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		700	mA	1, 2, 3
			t_{RAC} = 70 ns		660		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			68	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA			64		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		700	mA	1, 2, 3 ,4
			t_{RAC} = 70 ns		660		
Operating current (Hyper page mode (EDO))	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{HPC} = t_{HPC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		500	mA	1, 2, 5
			t_{RAC} = 70 ns		460		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		700	mA	1, 2
			t_{RAC} = 70 ns		660		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.25 V All other pins not under test = 0 V	$\overline{RAS}$	–10	+10	μA	
			others	–5	+1		
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.25 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –2.5 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.1 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.

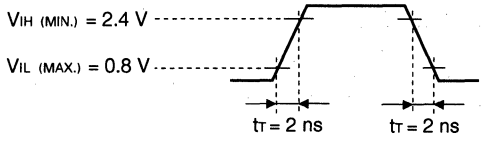
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO)cycle.

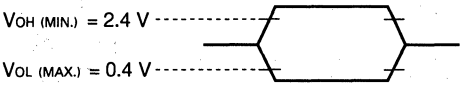
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

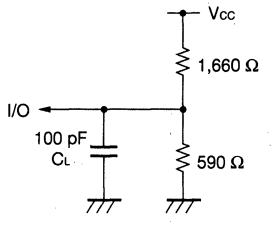
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	tRC	104	–	124	–	ns	
$\overline{RAS}$ Precharge Time	tRP	40	–	50	–	ns	
$\overline{CAS}$ Precharge Time	tCPN	10	–	10	–	ns	
$\overline{RAS}$ Pulse Width	tRAS	60	10,000	70	10,000	ns	
$\overline{CAS}$ Pulse Width	tCAS	10	10,000	12	10,000	ns	
$\overline{RAS}$ Hold Time	tRSH	15	–	17	–	ns	
$\overline{CAS}$ Hold Time	tCSH	40	–	50	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	14	45	14	52	ns	1
$\overline{RAS}$ to Column Address Delay Time	tRAD	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	10	–	10	–	ns	2
Row Address Setup Time	tASR	5	–	5	–	ns	
Row Address Hold Time	tRAH	10	–	10	–	ns	
Column Address Setup Time	tASC	0	–	0	–	ns	
Column Address Hold Time	tCAH	10	–	12	–	ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	tOES	0	–	0	–	ns	
$\overline{CAS}$ to Data Setup Time	tCLZ	0	–	0	–	ns	
$\overline{OE}$ to Data Setup Time	tOLZ	0	–	0	–	ns	
$\overline{OE}$ to Data Delay Time	tOED	13	–	15	–	ns	
Transition Time (Rise and Fall)	tT	1	50	1	50	ns	
Refresh Time	tREF	–	16	–	16	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	–	20	–	23	ns	1
Access Time from Column Address	t_{AA}	–	35	–	40	ns	1
Access Time from $\overline{OE}$	t_{OEA}	–	20	–	23	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
$\overline{CAS}$ Hold Time to $\overline{OE}$	t_{CHO}	5	–	5	–	ns	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ Pulse Width	t_{WP}	10	–	10	–	ns	1
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	15	–	17	–	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	10	–	12	–	ns	
$\overline{WE}$ Setup Time	t_{WCS}	0	–	0	–	ns	2
$\overline{OE}$ Hold Time	t_{OEH}	0	–	0	–	ns	
Data-in Setup Time	t_{DS}	0	–	0	–	ns	3
Data-in Hold Time	t_{DH}	10	–	10	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	t_{RWC}	148	–	172	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	87	–	99	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	32	–	37	–	ns	1
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	52	–	59	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{HPC}	25	–	30	–	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	10	10,000	12	10,000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	10	–	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	–	40	–	45	ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	52	–	59	–	ns	2
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	–	45	–	ns	
Read Modify Write Cycle Time	t_{HPRWC}	66	–	75	–	ns	
Data Output Hold Time	t_{DHC}	5	–	5	–	ns	
$\overline{OE}$ to $\overline{CAS}$ Hold Time	t_{OCH}	5	–	5	–	ns	4
$\overline{OE}$ Precharge Time	t_{OEP}	5	–	5	–	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	3,4
$\overline{WE}$ Pulse Width	t_{WPZ}	10	–	10	–	ns	4
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	3,4
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	3,4

Notes 1. $t_{HPC\ (MIN.)}$ is applied to $\overline{CAS}$ access.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $t_{OFC\ (MAX.)}$, $t_{OFR\ (MAX.)}$ and $t_{WEZ\ (MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.

(3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
$\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

(4) $\overline{WE}$: inactive (in read cycle)
$\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
$\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

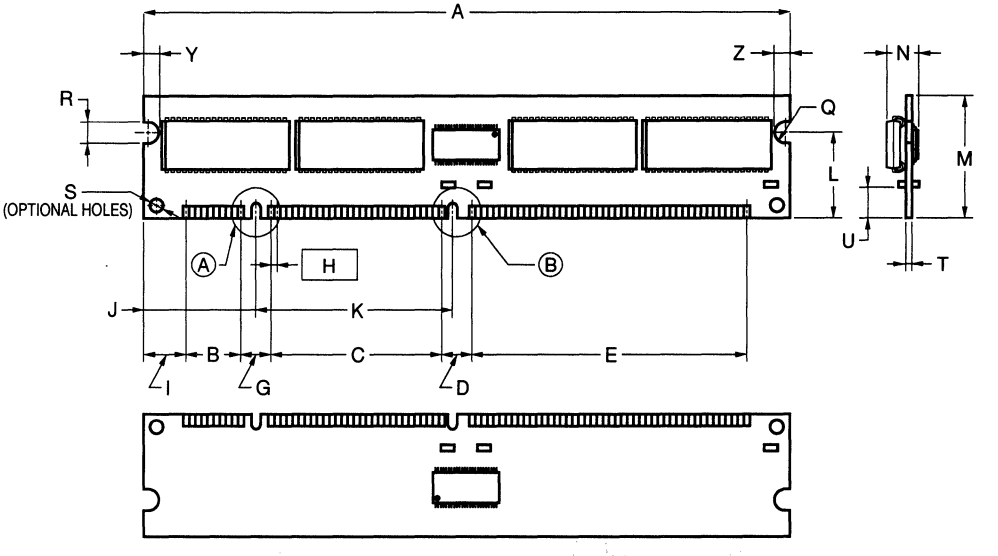
Refresh Cycle

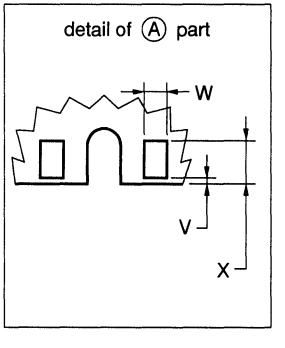
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	–	5	–	ns	
$\overline{WE}$ Hold Time (Hidden Refresh Cycle)	t_{WHR}	15	–	15	–	ns	

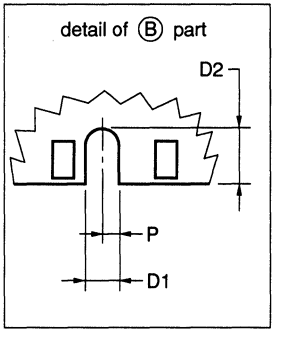
Timing Chart
Please refer to Timing Chart 1, page 365.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)







ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.1230
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.05 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.7000
M	25.4±0.13	1.000±0.006
N	9.0 MAX.	0.355 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A5

NEC

MOS INTEGRATED CIRCUIT
MC-422000FA64FB

2 M-WORD BY 64-BIT DYNAMIC RAM MODULE
HYPER PAGE MODE

Description

The MC-422000FA64FB is a 1,048,576 words by 64 bits dynamic RAM module on which 8 pieces of 16 M DRAM: μPD4218165 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 2,096,152 words by 64 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle Time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC-422000FA64-60	60 ns	104 ns	25 ns	3.73 W	357 mW (CMOS level input)
MC-422000FA64-70	70 ns	124 ns	30 ns	3.52 W	

- 1,024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

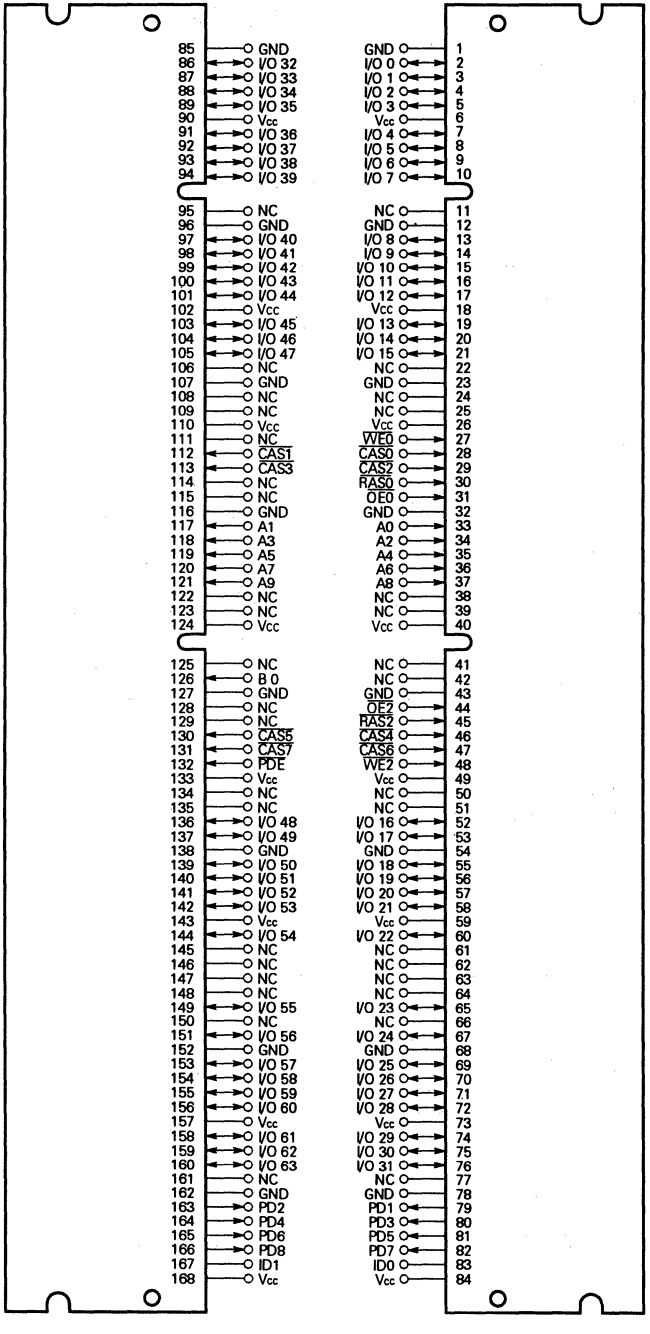
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000FA64FB-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	8 pieces of μPD4218165LE (400 mil SOJ) [Single side]
MC-422000FA64FB-70	70 ns		

Document No. M10559EJ1V0DSU1

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



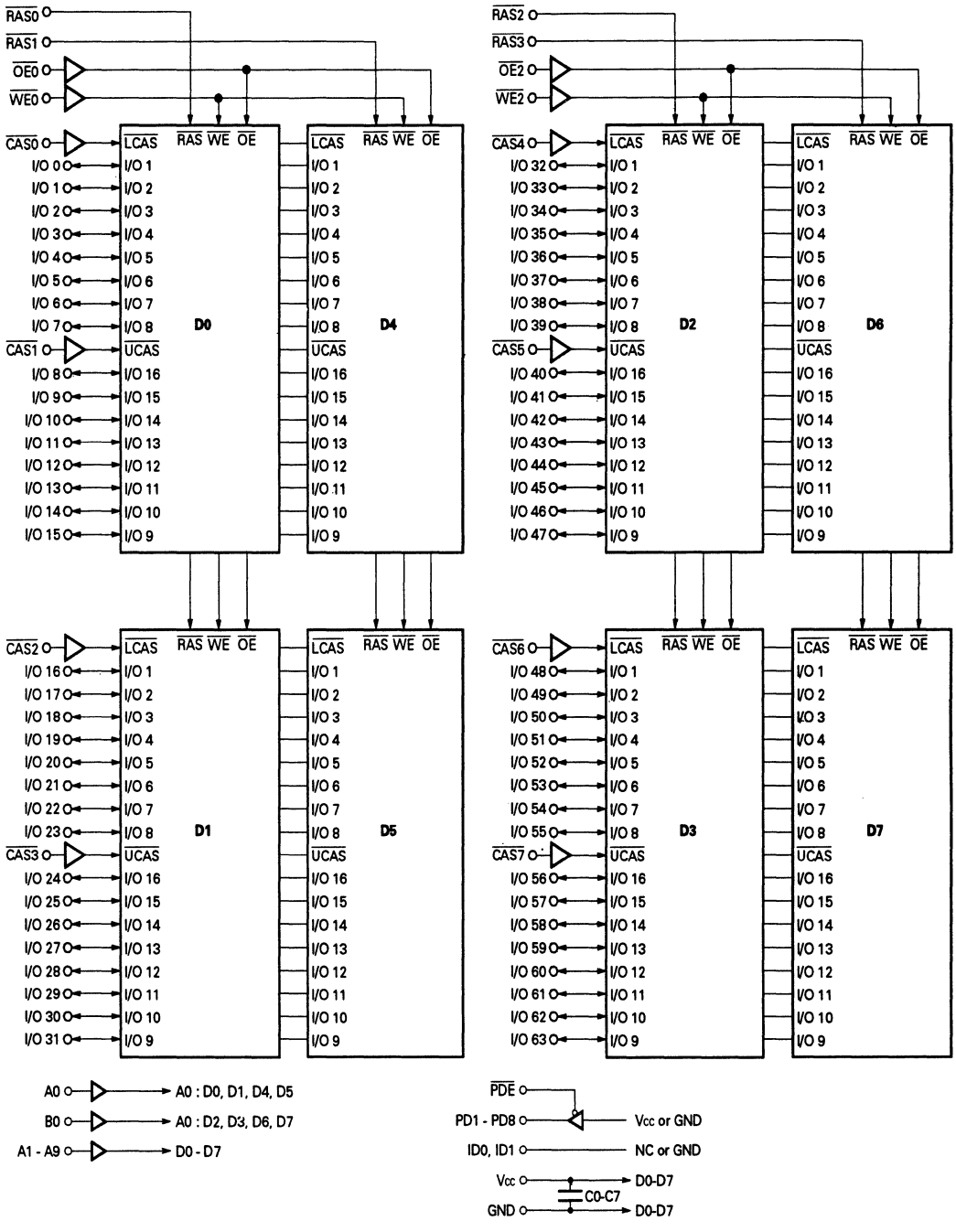
PD and ID Table

Pin Name	Pin No.	Access Time	
		60 ns	70 ns
PD1	79	H	H
PD2	163	L	L
PD3	80	H	H
PD4	164	L	L
PD5	81	H	H
PD6	165	H	L
PD7	82	H	H
PD8	166	H	H
ID0	83	GND	GND
ID1	167	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A9, B0 : Address Inputs
I/O 0 - I/O 63 : Data Inputs/Outputs
$\overline{RAS0}$ - $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
V_{CC} : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D7 : μPD4218165

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		6	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS2}$			45	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS7}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	C_{VO}	I/O0 - I/O63			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

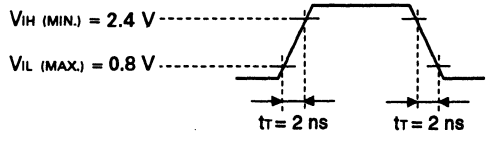
Parameter	Symbol	Test condition			MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns			710	mA	1,2,3
			t_{RAC} = 70 ns			670		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geqq V_{IH(MIN.)}$, I_O = 0 mA				76	mA	
		$\overline{RAS}$, $\overline{CAS} \geqq V_{CC}$ – 0.2 V, I_O = 0 mA				68		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geqq V_{IH(MIN.)}$ $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns			710	mA	1,2,3,4
			t_{RAC} = 70 ns			670		
Operating current (Hyper page mode)	I_{CC4}	$\overline{RAS} \leqq V_{IL(MAX.)}$ $\overline{CAS}$ Cycling $t_{HPC} = t_{HPC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns			510	mA	1,2,5
			t_{RAC} = 70 ns			470		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns			710	mA	1,2
			t_{RAC} = 70 ns			670		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V all other pins not under test = 0 V		$\overline{RAS}$	–10	+10	μA	
				others	–5	+1		
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)			–10	+10	μA	
High level output voltage	V_{OH}	I_O = –2.5 mA			2.4		V	
Low level output voltage	V_{OL}	I_O = +2.1 mA				0.4	V	

Notes
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).
2. Specified values are obtained with outputs unloaded.
3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leqq V_{IL(MAX.)}$ and $\overline{CAS} \geqq V_{IH(MIN.)}$.
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

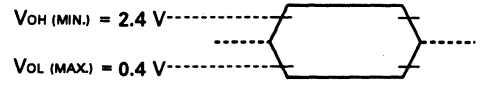
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write Cycle

Parameter	Symbol	tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	tRC	104	—	124	—	ns	
$\overline{RAS}$ Precharge Time	tRP	40	—	50	—	ns	
$\overline{CAS}$ Precharge Time	tCPN	10	—	10	—	ns	
$\overline{RAS}$ Pulse Width	tRAS	60	10 000	70	10 000	ns	
$\overline{CAS}$ Pulse Width	tCAS	10	10 000	12	10 000	ns	
$\overline{RAS}$ Hold Time	tRSH	10	—	12	—	ns	
$\overline{CAS}$ Hold Time	tCSH	40	—	50	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	14	45	14	52	ns	1
$\overline{RAS}$ to Column Address Delay Time	tRAD	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	5	—	5	—	ns	2
Row Address Setup Time	tASR	5	—	5	—	ns	
Row Address Hold Time	tRAH	10	—	10	—	ns	
Column Address Setup Time	tASC	0	—	0	—	ns	
Column Address Hold Time	tCAH	10	—	12	—	ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	tOES	0	—	0	—	ns	
$\overline{CAS}$ to Data Setup Time	tCLZ	0	—	0	—	ns	
$\overline{OE}$ to Data Setup Time	tOLZ	0	—	0	—	ns	
$\overline{OE}$ to Data Delay Time	tOED	13	—	15	—	ns	
Masked Byte Write Hold Time Referenced to $\overline{RAS}$	tMRH	0	—	0	—	ns	
Transition Time (Rise and Fall)	tT	1	50	1	50	ns	
Refresh Time	tREF	—	16	—	16	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	23	ns	1
Access Time from Column Address	t_{AA}	—	35	—	40	ns	1
Access Time from $\overline{OE}$	t_{OEA}	—	20	—	23	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	—	35	—	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	2
Output buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
$\overline{CAS}$ Hold Time to $\overline{OE}$	t_{CHO}	5	—	5	—	ns	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.

3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not refernced V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10	—	10	—	ns	1
$\overline{WE}$ Pulse Width	t_{WP}	10	—	10	—	ns	1
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	15	—	17	—	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	10	—	12	—	ns	
$\overline{WE}$ Setup Time	t_{WCS}	0	—	0	—	ns	2
$\overline{OE}$ Hold Time	t_{OEH}	0	—	0	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	ns	3
Data-in Hold Time	t_{DH}	10	—	10	—	ns	3

Notes 1. $t_{WP(MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH(MIN.)}$ should be met.

2. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	t_{RWC}	133	—	157	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	87	—	99	—	ns	1
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	32	—	37	—	ns	1
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	52	—	59	—	ns	1

Note 1. If $t_{WCS} \geqq t_{WCS(MIN.)}$ the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geqq t_{RWD(MIN.)}$, $t_{CWD} \geqq t_{CWD(MIN.)}$, $t_{AWD} \geqq t_{AWD(MIN.)}$, and $t_{CPWD} \geqq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{HPC}	25	—	30	—	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	60	125 000	70	125 000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	10	10 000	12	10 000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	52	—	59	—	ns	2
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	ns	
Read Modify Write Cycle Time	t_{HPRWC}	66	—	75	—	ns	
Data Output Hold Time	t_{DHC}	5	—	5	—	ns	
$\overline{OE}$ to CAS Hold Time	t_{OCH}	5	—	5	—	ns	
$\overline{OE}$ Precharge Time	t_{OEP}	5	—	5	—	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	3,4
$\overline{WE}$ Pulse Width	t_{WPZ}	10	—	10	—	ns	4
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	3.4
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	3.4

Notes 1. $t_{HPC(MIN.)}$ is applied to access time from $\overline{CAS}$

2. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $t_{RWD} \geqq t_{RWD(MIN.)}$, $t_{CWD} \geqq t_{CWD(MIN.)}$, $t_{AWD} \geqq t_{AWD(MIN.)}$, and $t_{CPWD} \geqq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
3. $t_{OFC(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.
4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.
   (1) $\overline{RAS}$, $\overline{CAS}$: Inactive (at the end of read cycle) .
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: inactive ··· t_{OEZ} is effective.
   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive
   (at the end of read cycle)
   $\overline{WE}$,$\overline{OE}$:active and either t_{RRH} or t_{RCH} must be met··· t_{WEZ}, t_{WPZ} are effective.

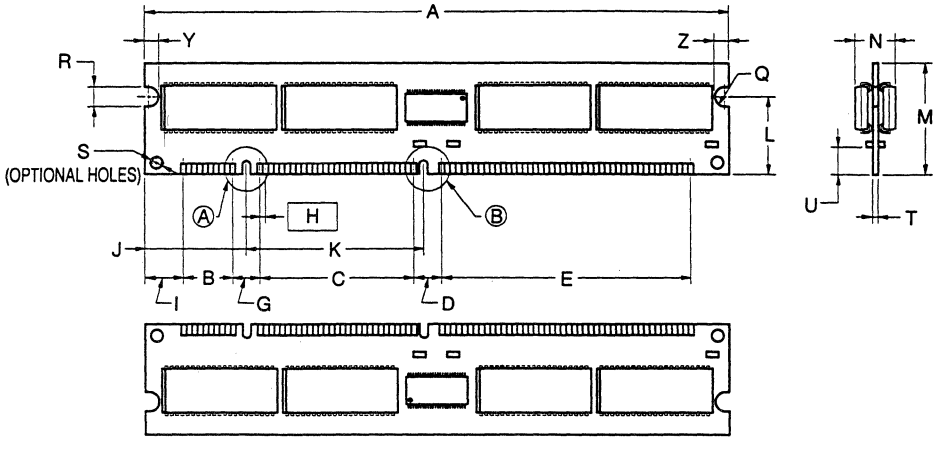
Refresh Cycle

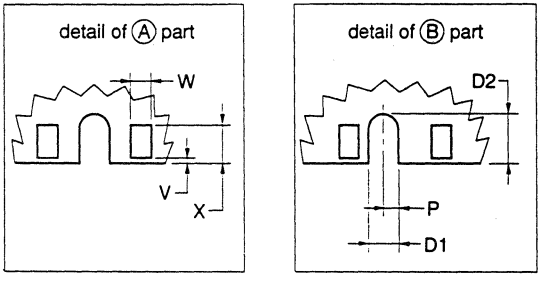
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	—	5	—	ns	
$\overline{WE}$ Hold Time (Hidden Refresh Cycle)	t_{WHR}	15	—	15	—	ns	

Timing Chart
Please refer to Timing Chart 1, page 365.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.1230
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.05 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.7000
M	25.4±0.13	1.000±0.006
N	9.0 MAX.	0.355 MAX.
P	1.0	0.039
Q	R 2.0	R 0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A7

NEC

MOS INTEGRATED CIRCUIT
MC-422000FB72

2 M-WORD BY 72-BIT DYNAMIC RAM MODULE
HYPER PAGE MODE (EDO)

Description

The MC-422000FB72 is a 2,097,152 words by 72 bits dynamic RAM module on which 9 pieces of 16 M DRAM: μPD4217805 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 2,097,152 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC-422000FB72-60	60 ns	104 ns	25 ns	5.51 W	363 mW (CMOS level input)
MC-422000FB72-70	70 ns	124 ns	30 ns	5.04 W	

- 2,048 refresh cycles/32 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

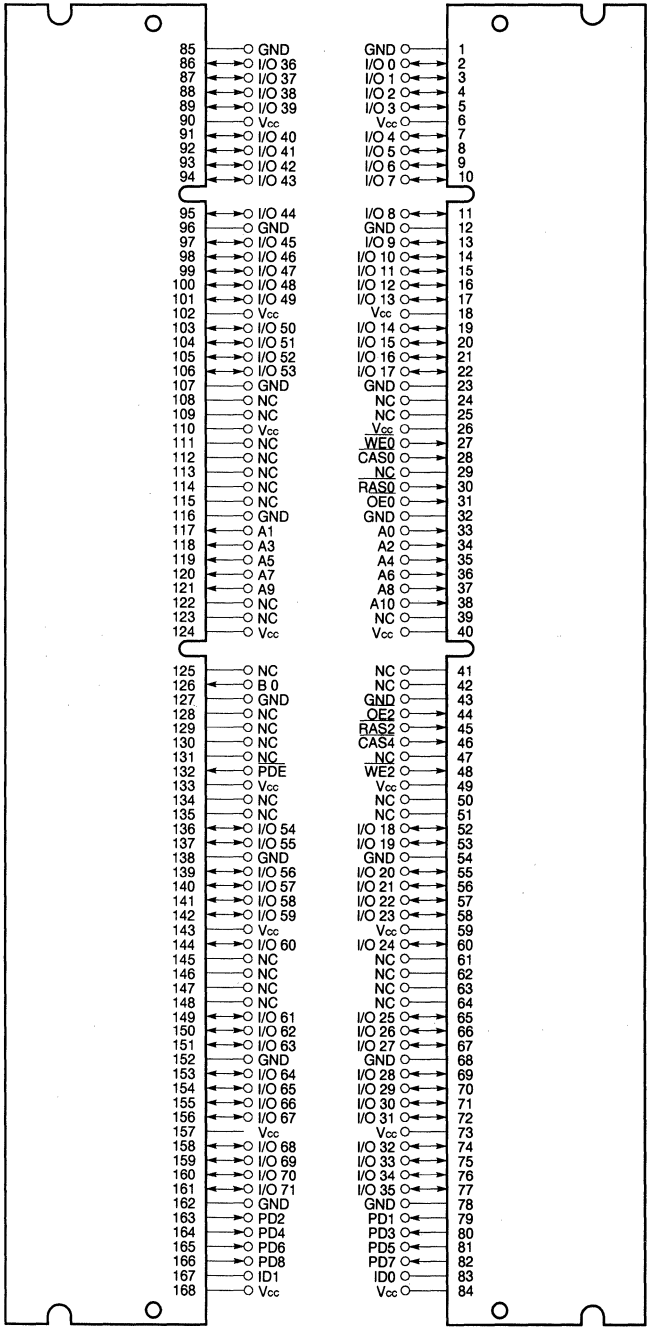
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000FB72F-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	9 pieces of μPD4217805G5 (400 mil TSOP(II)) [Double side]
MC-422000FB72F-70	70 ns		

The information in this document is subject to change without notice.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



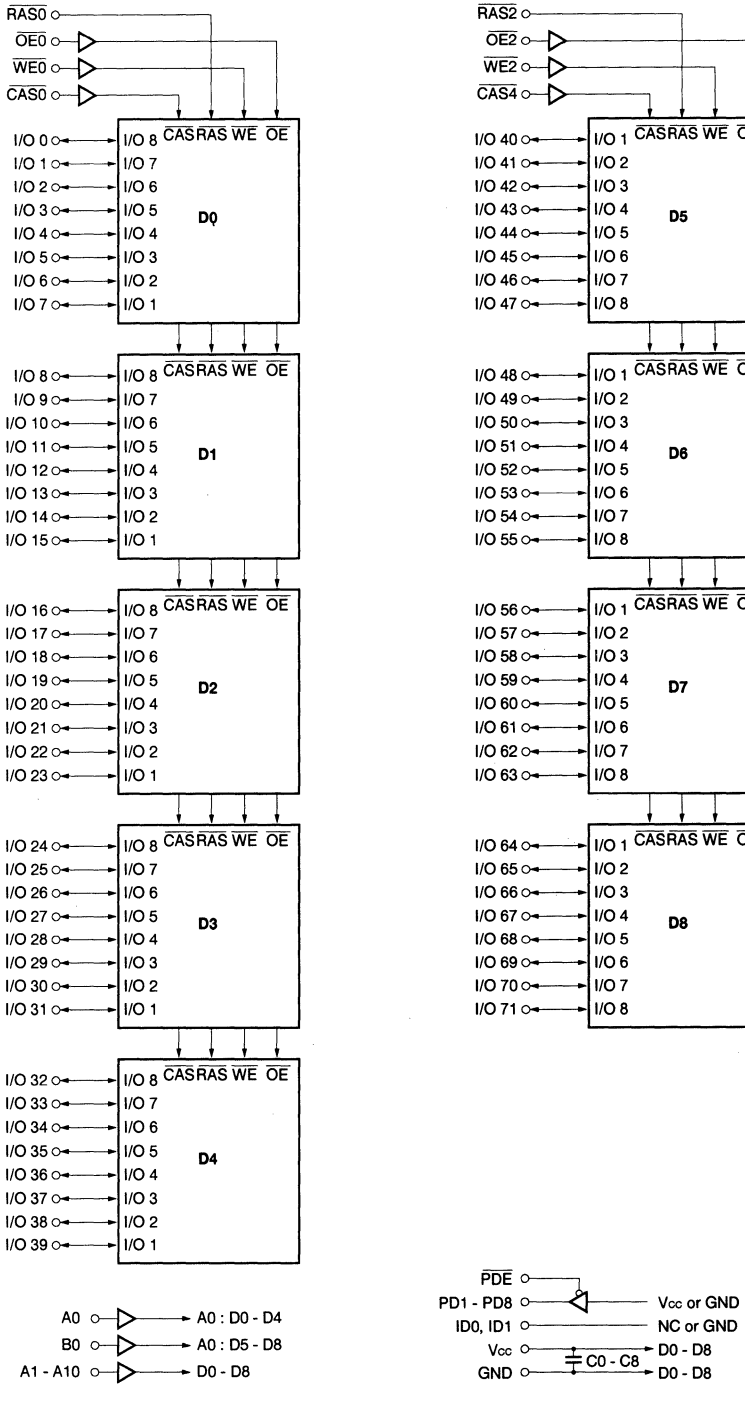
PD and ID Table

Pin Name	Pin No.	Access Time	
		60 ns	70 ns
PD1	79	H	H
PD2	163	L	L
PD3	80	L	L
PD4	164	H	H
PD5	81	H	H
PD6	165	H	L
PD7	82	H	H
PD8	166	L	L
ID0	83	GND	GND
ID1	167	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A10, B0 : Address Inputs
I/O 0 - I/O 71 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
V_{CC} : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D8 : μPD4217805

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		11	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			50	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS4}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data input/output capacitance	$C_{I/O}$	I/O0 - I/O71			20	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test condition			MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns			1,050	mA	1, 2, 3
			t_{RAC} = 70 ns			960		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA				78	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA				69		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns			1,050	mA	1, 2, 3 ,4
			t_{RAC} = 70 ns			960		
Operating current (Hyper page mode (EDO))	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling $t_{HPC} = t_{HPC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns			870	mA	1, 2, 5
			t_{RAC} = 70 ns			780		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns			1,050	mA	1, 2
			t_{RAC} = 70 ns			960		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.25 V All other pins not under test = 0 V		$\overline{RAS}$	–10	+10	μA	
				Others	–5	+1		
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.25 V Output is disabled (Hi-Z)			–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA			2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA				0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.

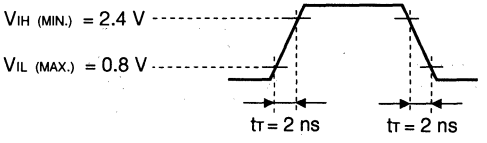
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

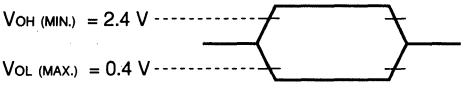
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

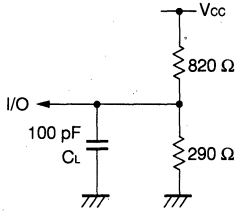
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read/Write cycle time	t_{RC}	104	–	124	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	–	10	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10,000	12	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15	–	17	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	40	–	50	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	14	45	14	52	ns	1
$\overline{RAS}$ to column address delay time	t_{RAD}	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	ns	2
Row address setup time	t_{ASR}	5	–	5	–	ns	
Row address hold time	t_{RAH}	10	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	10	–	12	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$	t_{OES}	0	–	0	–	ns	
$\overline{CAS}$ to data setup time	t_{CLZ}	0	–	0	–	ns	
$\overline{OE}$ to data setup time	t_{OLZ}	0	–	0	–	ns	
$\overline{OE}$ to data delay time	t_{OED}	13	–	15	–	ns	
Transition time (rise and fall)	t_T	1	50	1	50	ns	
Refresh time	t_{REF}	–	32	–	32	ms	

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	20	–	23	ns	1
Access time from column address	t_{AA}	–	35	–	40	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	20	–	23	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5	–	5	–	ns	

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	10	–	10	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	15	–	17	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	10	–	12	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	10	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	148	–	172	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	87	–	99	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	32	–	37	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	52	–	59	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read/Write cycle time	t_{HPC}	25	–	30	–	ns	1
$\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ pulse width	t_{HCAS}	10	10,000	12	10,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	40	–	45	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	52	–	59	–	ns	2
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40	–	45	–	ns	
Read modify write cycle time	t_{HPRWC}	66	–	75	–	ns	
Data output hold time	t_{DHC}	5	–	5	–	ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5	–	5	–	ns	4
$\overline{OE}$ precharge time	t_{OEP}	5	–	5	–	ns	
Output buffer turn-off delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	3,4
$\overline{WE}$ pulse width	t_{WPZ}	10	–	10	–	ns	4
Output buffer turn-off delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	3,4
Output buffer turn-off delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	3,4

Notes 1. $t_{HPC\ (MIN.)}$ is applied to $\overline{CAS}$ access.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $t_{OFC\ (MAX.)}$, $t_{OFR\ (MAX.)}$ and $t_{WEZ\ (MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.

(3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
$\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

(4) $\overline{WE}$: inactive (in read cycle)
$\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
$\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

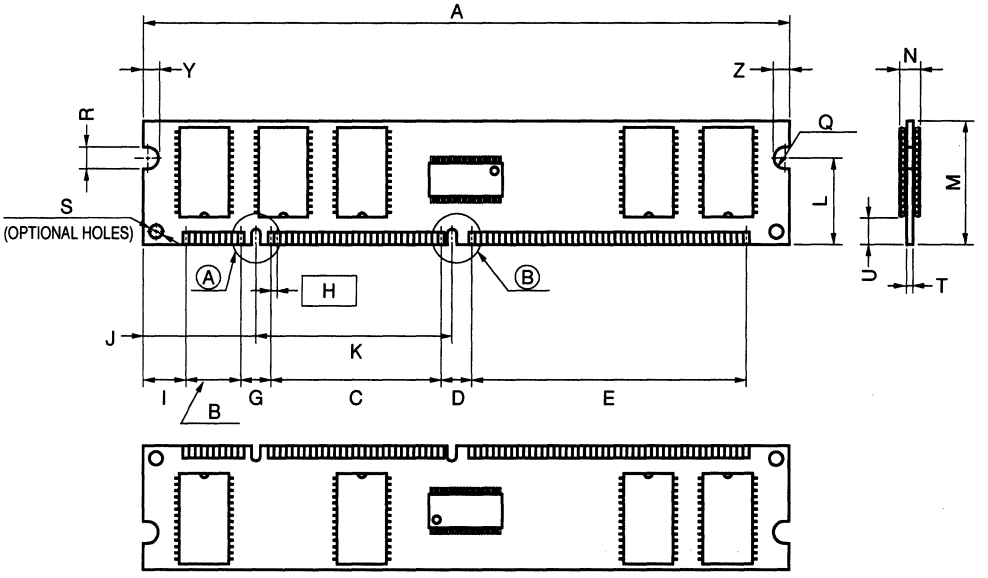
Refresh Cycle

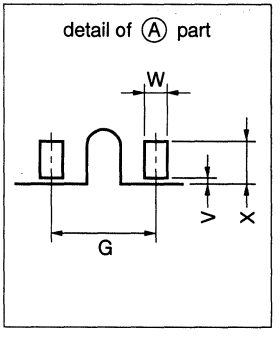
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	10	–	10	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	ns	
$\overline{WE}$ setup time	t_{WSR}	15	–	15	–	ns	
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	ns	

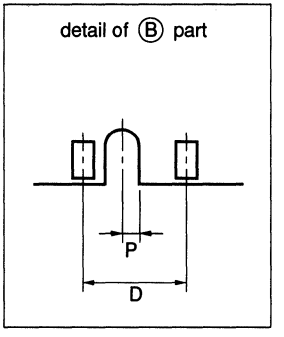
Timing Chart
Please refer to Timing Chart 2, page 381.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)







ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54	0.100
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A6

NEC

MOS INTEGRATED CIRCUIT

MC-422000LFB72F

3.3 V OPERATION 2 M-WORD BY 72-BIT DYNAMIC RAM MODULE HYPER PAGE MODE (EDO)

Description

The MC-422000LFB72F is a 2,097,152 words by 72 bits dynamic RAM module on which 9 pieces of 16 M DRAM: μPD4217805L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 2,097,152 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC-422000LFB72-A60	60 ns	104 ns	25 ns	3.28 W	147.6 mW (CMOS level input)
MC-422000LFB72-A70	70 ns	124 ns	30 ns	2.95 W	

- 2,048 refresh cycles/32 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

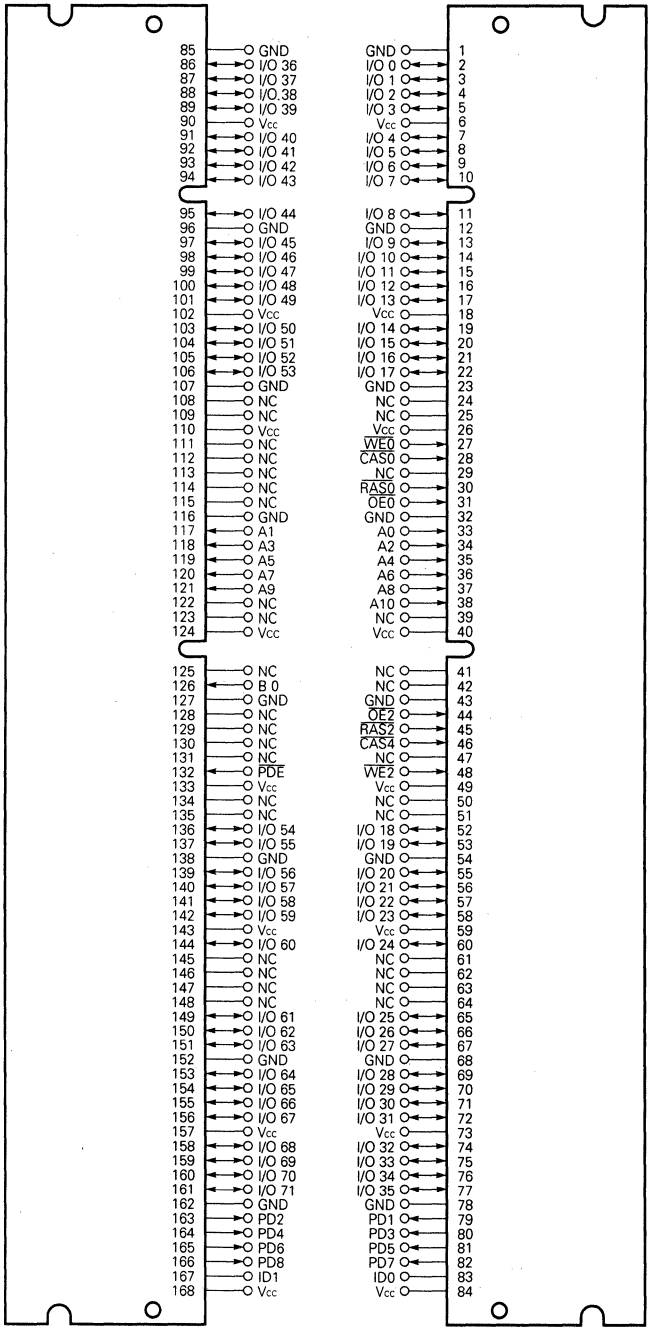
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000LFB72F-A60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	9 pieces of μPD4217805LG5 (400 mil TSOP(II)) [Double side]
MC-422000LFB72F-A70	70 ns		

Document No. M10042EJ5V0DSU1

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



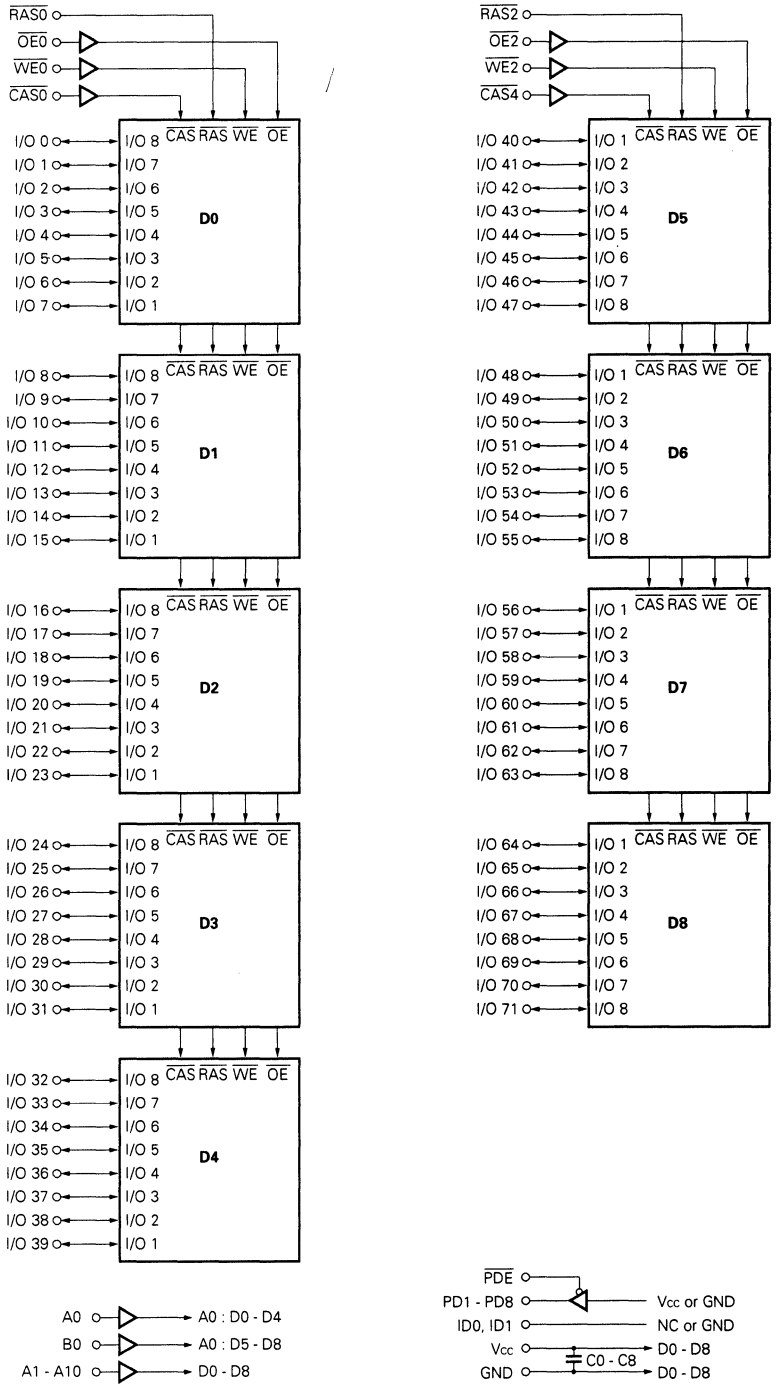
PD and ID Table

Pin Name	Pin No.	Access Time	
		60 ns	70 ns
PD1	79	H	H
PD2	163	L	L
PD3	80	L	L
PD4	164	H	H
PD5	81	H	H
PD6	165	H	L
PD7	82	H	H
PD8	166	L	L
ID0	83	GND	GND
ID1	167	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A10, B0 : Address Inputs
I/O 0 - I/O 71 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D8 : μPD4217805L

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		11	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0-A10, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			50	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS4}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data input/output capacitance	$C_{I/O}$	I/O0-I/O71			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition			MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns			910	mA	1, 2, 3
			t_{RAC} = 70 ns			820		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA			82	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA			41		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns			910	mA	1, 2, 3, 4
			t_{RAC} = 70 ns			820		
Operating current (Hyper page mode (EDO))	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{HPC} = t_{HPC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns			820	mA	1, 2, 5
			t_{RAC} = 70 ns			730		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns			910	mA	1, 2
			t_{RAC} = 70 ns			820		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		$\overline{RAS}$	–5	+5	μA	
				Others	–5	+1		
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)			–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA			2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA				0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.

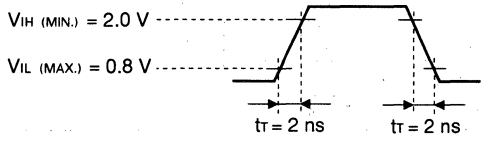
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

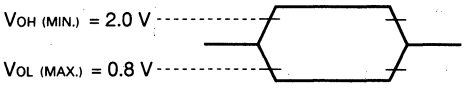
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

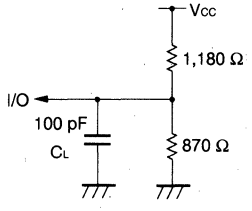
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{RC}	104	–	124	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	–	50	–	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	10	–	10	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	10	10,000	12	10,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15	–	17	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	40	–	50	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	14	45	14	52	ns	1
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	ns	2
Row Address Setup Time	t_{ASR}	5	–	5	–	ns	
Row Address Hold Time	t_{RAH}	10	–	10	–	ns	
Column Address Setup Time	t_{ASC}	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	10	–	12	–	ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OES}	0	–	0	–	ns	
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0	–	0	–	ns	
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0	–	0	–	ns	
$\overline{OE}$ to Data Delay Time	t_{OED}	13	–	15	–	ns	
Transition Time (Rise and Fall)	t_T	1	50	1	50	ns	
Refresh Time	t_{REF}	–	32	–	32	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	–	20	–	23	ns	1
Access Time from Column Address	t_{AA}	–	35	–	40	ns	1
Access Time from $\overline{OE}$	t_{OEA}	–	20	–	23	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
$\overline{CAS}$ Hold Time to $\overline{OE}$	t_{CHO}	5	–	5	–	ns	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ Pulse Width	t_{WP}	10	–	10	–	ns	1
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	15	–	17	–	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	10	–	12	–	ns	
$\overline{WE}$ Setup Time	t_{WCS}	0	–	0	–	ns	2
$\overline{OE}$ Hold Time	t_{OEH}	0	–	0	–	ns	
Data-in Setup Time	t_{DS}	0	–	0	–	ns	3
Data-in Hold Time	t_{DH}	10	–	10	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	t_{RWC}	148	–	172	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	87	–	99	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	32	–	37	–	ns	1
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	52	–	59	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{HPC}	25	–	30	–	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	10	10,000	12	10,000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	10	–	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	–	40	–	45	ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	52	–	59	–	ns	2
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	–	45	–	ns	
Read Modify Write Cycle Time	t_{HPRWC}	66	–	75	–	ns	
Data Output Hold Time	t_{DHC}	5	–	5	–	ns	
$\overline{OE}$ to $\overline{CAS}$ Hold Time	t_{OCH}	5	–	5	–	ns	4
$\overline{OE}$ Precharge Time	t_{OEP}	5	–	5	–	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	3,4
$\overline{WE}$ Pulse Width	t_{WPZ}	10	–	10	–	ns	4
Output Buffer Turn-off delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	3,4
Output Buffer Turn-off delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	3,4

Notes 1. $t_{HPC\ (MIN.)}$ is applied to $\overline{CAS}$ access.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $t_{OFC\ (MAX.)}$, $t_{OFR\ (MAX.)}$ and $t_{WEZ\ (MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.

(3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
$\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

(4) $\overline{WE}$: inactive (in read cycle)
$\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
$\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

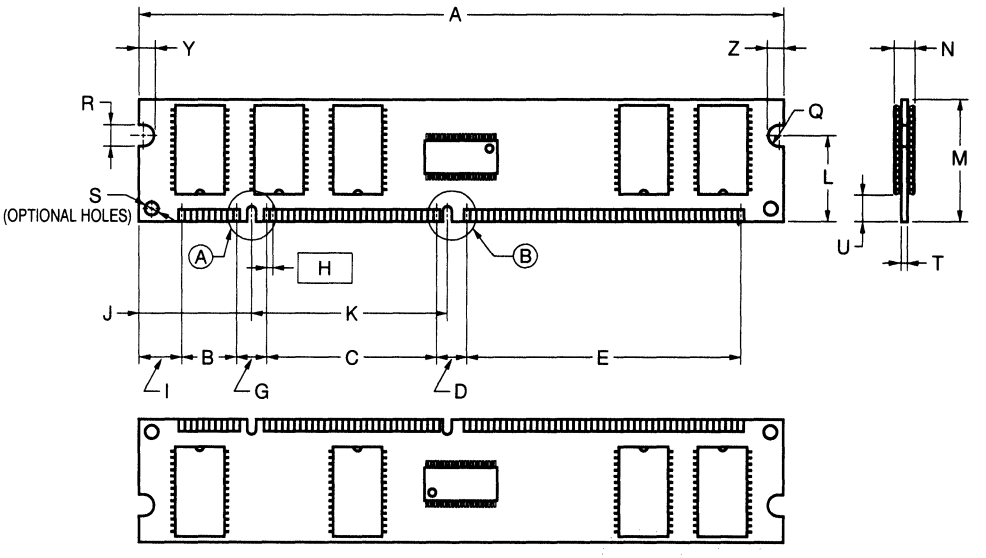
Refresh Cycle

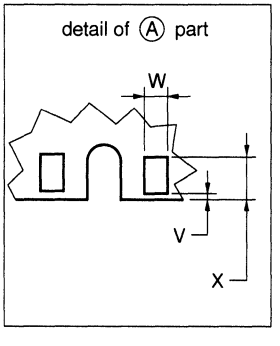
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	–	5	–	ns	
$\overline{WE}$ Setup Time	t_{WSR}	15	–	15	–	ns	
$\overline{WE}$ Hold Time	t_{WHR}	15	–	15	–	ns	

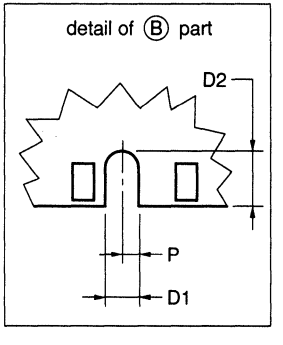
Timing Chart
Please refer to Timing Chart 2, page 381.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOKET TYPE)







ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.123
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.50	0.925
K	43.18	1.70
L	17.78	0.700
M	25.4±0.13	1.000±0.006
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A8

NEC

MOS INTEGRATED CIRCUIT

MC-424000FC72

4 M-WORD BY 72-BIT DYNAMIC RAM MODULE HYPER PAGE MODE (EDO)

Description

The MC-424000FC72 is a 4,194,304 words by 72 bits dynamic RAM module on which 18 pieces of 16 M DRAM: μPD4216405 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 4,194,304 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC-424000FC72-60	60 ns	104 ns	25 ns	8.82 W	410 mW
MC-424000FC72-70	70 ns	124 ns	30 ns	7.88 W	(CMOS level input)

- 4,096 refresh cycles/64 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

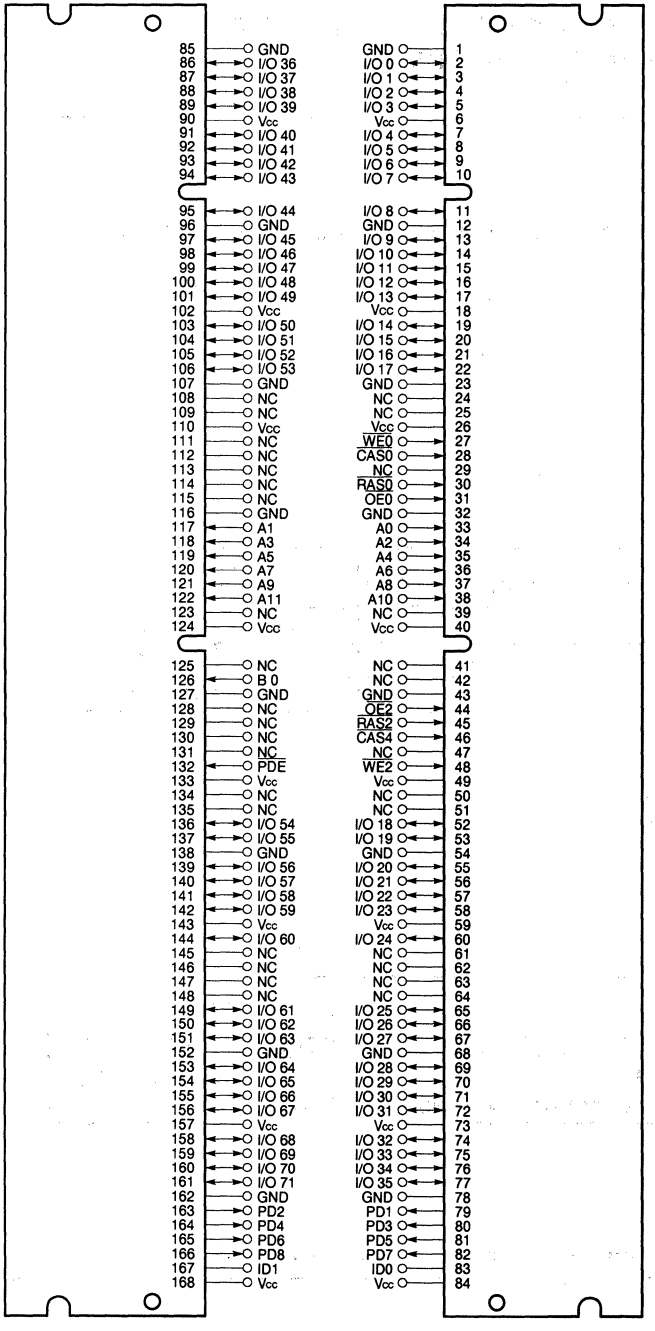
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-424000FC72F-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	18 pieces of μPD4216405G3 (300 mil TSOP(II)) [Double side]
MC-424000FC72F-70	70 ns		

Document No. M10548EJ2V0DSU1

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



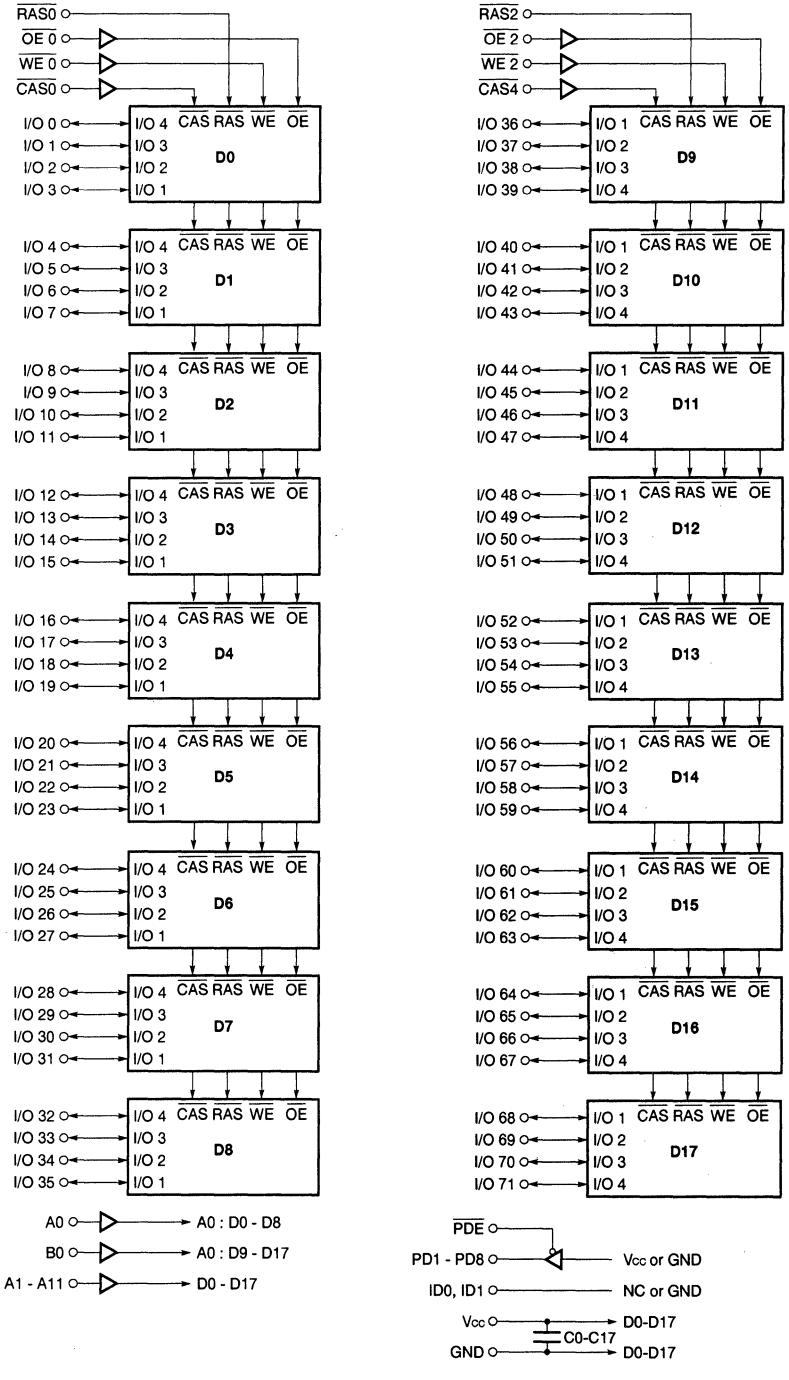
PD and ID Table

Pin Name	Pin No.	Access Time	
		60 ns	70 ns
PD1	79	H	H
PD2	163	H	H
PD3	80	L	L
PD4	164	H	H
PD5	81	H	H
PD6	165	H	L
PD7	82	H	H
PD8	166	L	L
ID0	83	GND	GND
ID1	167	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A11, B0 : Address Inputs
I/O 0 - I/O 71 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
V_{CC} : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D17 : μPD4216405

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC\ (MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		20	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0-A11, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			78	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS4}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data input/output capacitance	$C_{I/O}$	I/O0-I/O71			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition			MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling	t_{RAC} = 60 ns			1,680	mA	1, 2, 3
		$t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns			1,500		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA			96	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA			78		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$	t_{RAC} = 60 ns			1,680	mA	1, 2, 3, 4
		$t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns			1,500		
Operating current (Hyper page mode (EDO))	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling	t_{RAC} = 60 ns			1,680	mA	1, 2, 5
		$t_{HPC} = t_{HPC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns			1,500		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ cycling	t_{RAC} = 60 ns			1,680	mA	1, 2
		$t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns			1,500		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.25 V		$\overline{RAS}$	–10	+10	μA	
		All other pins not under test = 0 V		Others	–5	+1		
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.25 V Output is disabled (Hi-Z)			–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA			2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA				0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.

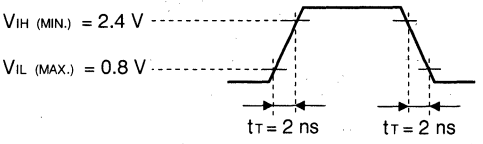
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

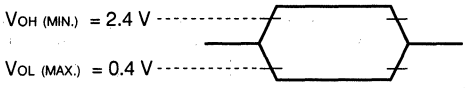
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

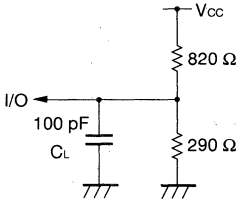
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t_{RC}	104	–	124	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	–	10	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10,000	12	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15	–	17	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	40	–	50	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	14	45	14	52	ns	1
$\overline{RAS}$ to column address delay time	t_{RAD}	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	ns	2
Row address setup time	t_{ASR}	5	–	5	–	ns	
Row address hold time	t_{RAH}	10	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	10	–	12	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$	t_{OES}	0	–	0	–	ns	
$\overline{CAS}$ to data setup time	t_{CLZ}	0	–	0	–	ns	
$\overline{OE}$ to data setup time	t_{OLZ}	0	–	0	–	ns	
$\overline{OE}$ to data delay time	t_{OED}	13	–	15	–	ns	
Transition time (rise and fall)	t_T	1	50	1	50	ns	
Refresh time	t_{REF}	–	64	–	64	ms	

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	20	–	23	ns	1
Access time from column address	t_{AA}	–	35	–	40	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	20	–	23	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5	–	5	–	ns	

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	10	–	10	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	15	–	17	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	10	–	12	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	10	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	148	–	172	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	87	–	99	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	32	–	37	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	52	–	59	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t_{HPC}	25	–	30	–	ns	1
$\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ pulse width	t_{HCAS}	10	10,000	12	10,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	40	–	45	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	52	–	59	–	ns	2
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40	–	45	–	ns	
Read modify write cycle time	t_{HPRWC}	66	–	75	–	ns	
Data output hold time	t_{DHC}	5	–	5	–	ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5	–	5	–	ns	4
$\overline{OE}$ precharge time	t_{OEP}	5	–	5	–	ns	
Output buffer turn-off delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	3,4
$\overline{WE}$ pulse width	t_{WPZ}	10	–	10	–	ns	4
Output buffer turn-off delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	3,4
Output buffer turn-off delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	3,4

Notes 1. $t_{HPC\ (MIN.)}$ is applied to $\overline{CAS}$ access.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $t_{OFC\ (MAX.)}$, $t_{OFR\ (MAX.)}$ and $t_{WEZ\ (MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.

(3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
$\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

(4) $\overline{WE}$: inactive (in read cycle)
$\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
$\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

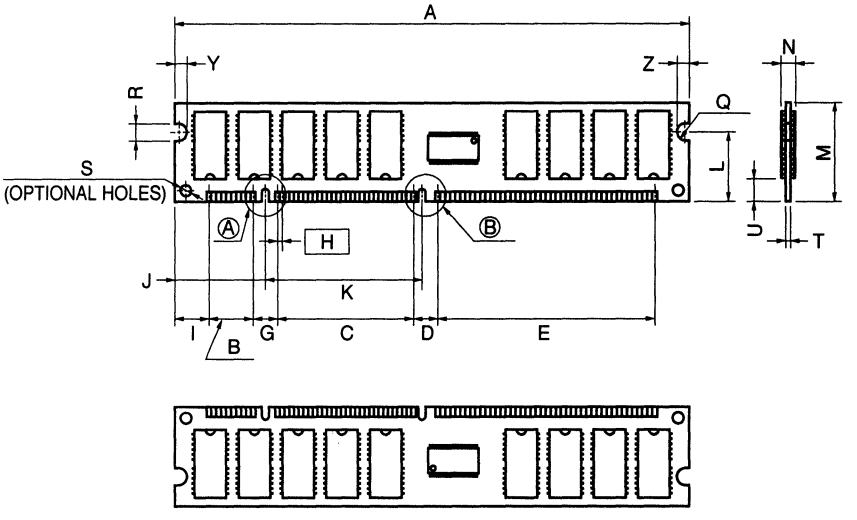
Refresh Cycle

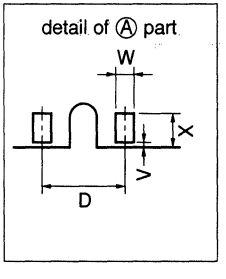
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	10	–	10	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	ns	
$\overline{WE}$ setup time	t_{WSR}	15	–	15	–	ns	
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	ns	

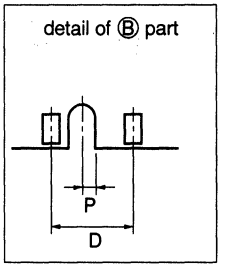
Timing Chart
Please refer to Timing Chart 2, page 381.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)







ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A2

NEC

MOS INTEGRATED CIRCUIT

MC-424000LFC72F

3.3 V OPERATION 4 M-WORD BY 72-BIT DYNAMIC RAM MODULE HYPER PAGE MODE (EDO)

Description

The MC-424000LFC72F is a 4,194,304 words by 72 bits dynamic RAM module on which 18 pieces of 16 M DRAM: μPD4216405L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 4,194,304 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC-424000LFC72-A60	60 ns	104 ns	25 ns	5.87 W	180 mW (CMOS level input)
MC-424000LFC72-A70	70 ns	124 ns	30 ns	5.22 W	

- 4,096 refresh cycles/64 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

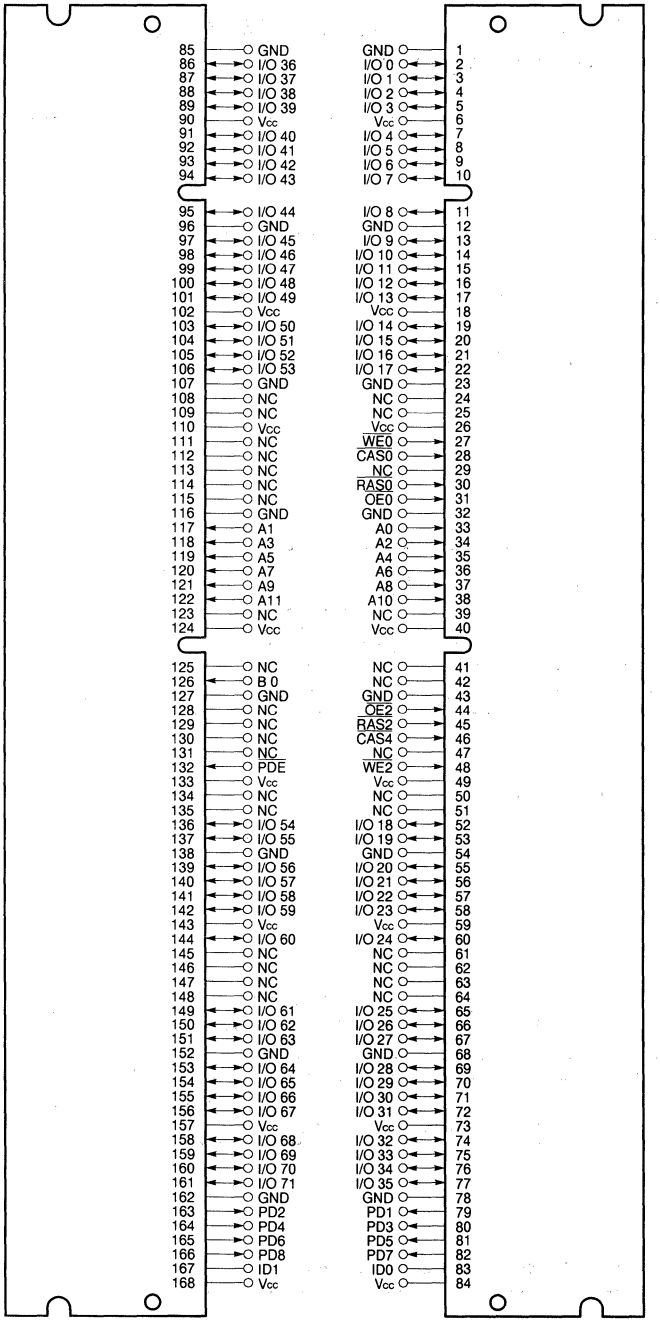
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-424000LFC72F-A60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	18 pieces of μPD4216405LG3 (300 mil TSOP(II)) [Double side]
MC-424000LFC72F-A70	70 ns		

The information in this document is subject to change without notice.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



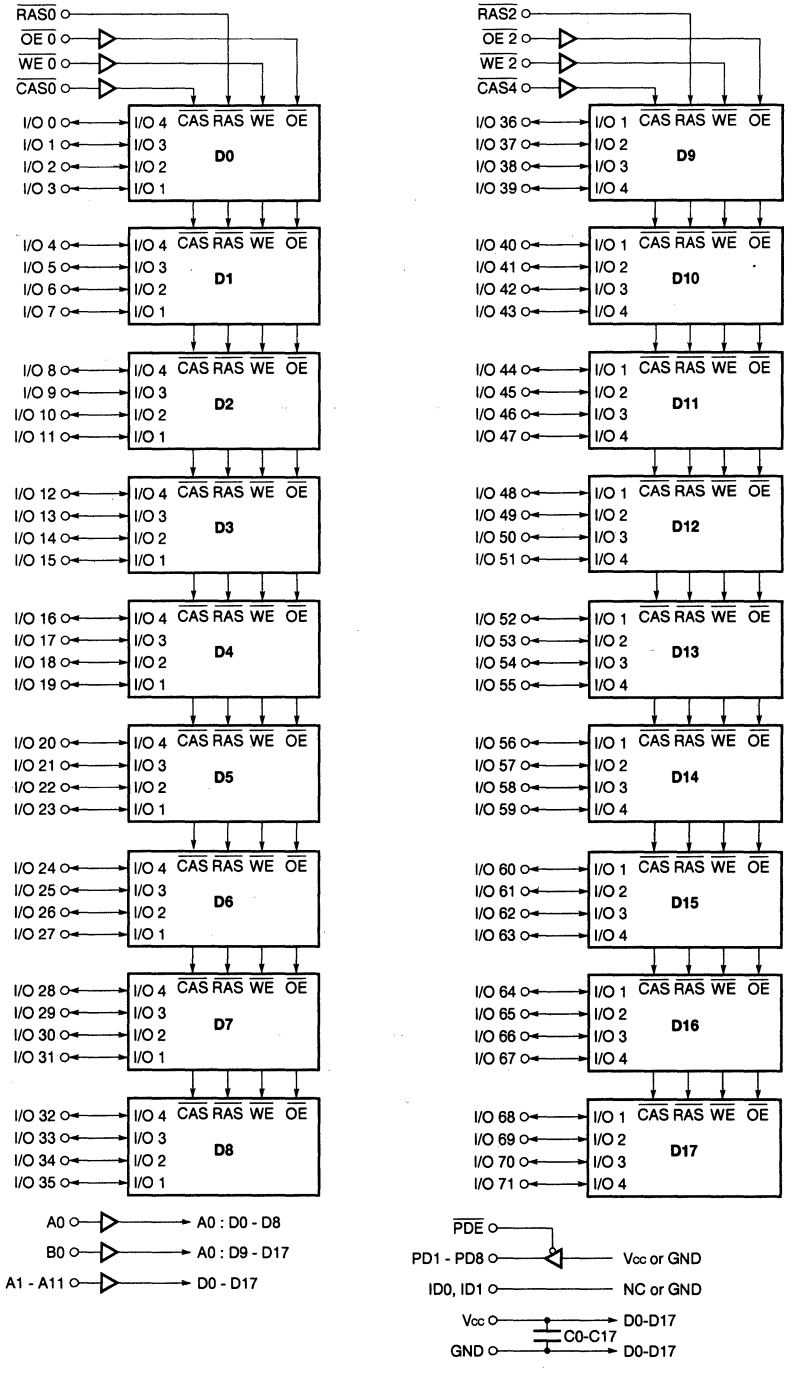
PD and ID Table

Pin Name	Pin No.	Access Time	
		60 ns	70 ns
PD1	79	H	H
PD2	163	H	H
PD3	80	L	L
PD4	164	H	H
PD5	81	H	H
PD6	165	H	L
PD7	82	H	H
PD8	166	L	L
ID0	83	GND	GND
ID1	167	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A11, B0 : Address Inputs
I/O 0 - I/O 71 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
V_{CC} : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D17 : μPD4216405L

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC\ (MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		20	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0-A11, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			78	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS4}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data input/output capacitance	$C_{I/O}$	I/O0-I/O71			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		1,450	mA	1, 2, 3
			t_{RAC} = 70 ns		1,270		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		100	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		50		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		1,450	mA	1, 2, 3, 4
			t_{RAC} = 70 ns		1,270		
Operating current (Hyper page mode (EDO))	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{HPC} = t_{HPC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		1,630	mA	1, 2, 5
			t_{RAC} = 70 ns		1,450		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		1,450	mA	1, 2
			t_{RAC} = 70 ns		1,270		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V	$\overline{RAS}$	–5	+5	μA	
			Others	–5	+1		
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.

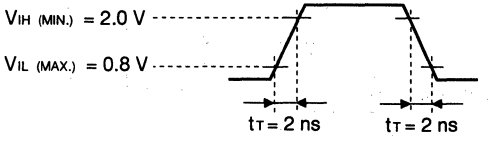
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

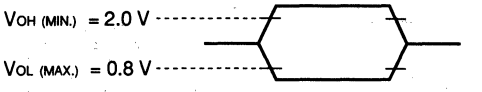
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

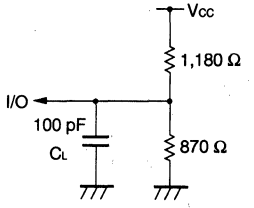
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{RC}	104	–	124	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	–	50	–	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	10	–	10	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	10	10,000	12	10,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15	–	17	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	40	–	50	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	14	45	14	52	ns	1
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	ns	2
Row Address Setup Time	t_{ASR}	5	–	5	–	ns	
Row Address Hold Time	t_{RAH}	10	–	10	–	ns	
Column Address Setup Time	t_{ASC}	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	10	–	12	–	ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OES}	0	–	0	–	ns	
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0	–	0	–	ns	
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0	–	0	–	ns	
$\overline{OE}$ to Data Delay Time	t_{OED}	13	–	15	–	ns	
Transition Time (Rise and Fall)	t_T	1	50	1	50	ns	
Refresh Time	t_{REF}	–	64	–	64	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	–	20	–	23	ns	1
Access Time from Column Address	t_{AA}	–	35	–	40	ns	1
Access Time from $\overline{OE}$	t_{OEA}	–	20	–	23	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
$\overline{CAS}$ Hold Time to $\overline{OE}$	t_{CHO}	5	–	5	–	ns	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ Pulse Width	t_{WP}	10	–	10	–	ns	1
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	15	–	17	–	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	10	–	12	–	ns	
$\overline{WE}$ Setup Time	t_{WCS}	0	–	0	–	ns	2
$\overline{OE}$ Hold Time	t_{OEH}	0	–	0	–	ns	
Data-in Setup Time	t_{DS}	0	–	0	–	ns	3
Data-in Hold Time	t_{DH}	10	–	10	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	t_{RWC}	148	–	172	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	87	–	99	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	32	–	37	–	ns	1
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	52	–	59	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{HPC}	25	–	30	–	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	10	10,000	12	10,000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	10	–	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	–	40	–	45	ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	52	–	59	–	ns	2
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	–	45	–	ns	
Read Modify Write Cycle Time	t_{HPRWC}	66	–	75	–	ns	
Data Output Hold Time	t_{DHC}	5	–	5	–	ns	
$\overline{OE}$ to $\overline{CAS}$ Hold Time	t_{OCH}	5	–	5	–	ns	4
$\overline{OE}$ Precharge Time	t_{OEP}	5	–	5	–	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	3,4
$\overline{WE}$ Pulse Width	t_{WPZ}	10	–	10	–	ns	4
Output Buffer Turn-off delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	3,4
Output Buffer Turn-off delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	3,4

Notes 1. $t_{HPC\ (MIN.)}$ is applied to $\overline{CAS}$ access.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $t_{OFC\ (MAX.)}$, $t_{OFR\ (MAX.)}$ and $t_{WEZ\ (MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.

(3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
$\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

(4) $\overline{WE}$: inactive (in read cycle)
$\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
$\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

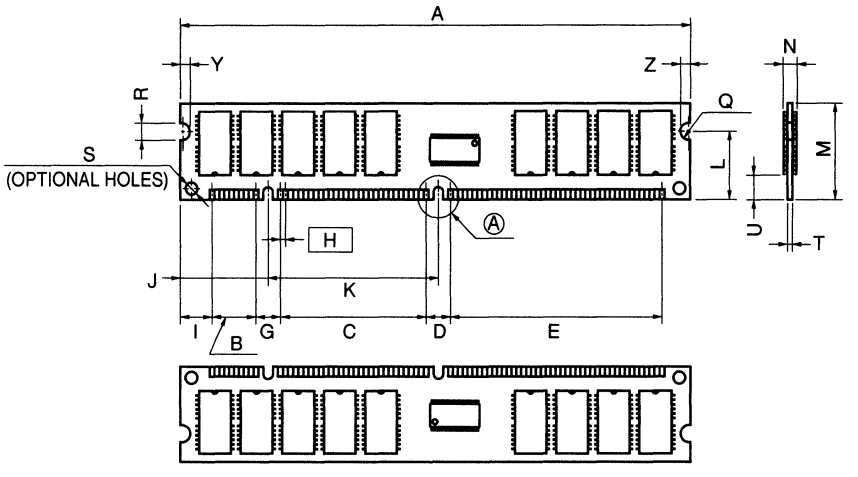
Refresh Cycle

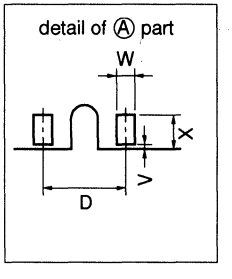
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	–	5	–	ns	
$\overline{WE}$ Setup Time	t_{WSR}	15	–	15	–	ns	
$\overline{WE}$ Hold Time	t_{WHR}	15	–	15	–	ns	

Timing Chart
Please refer to Timing Chart 2, page 381.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	43.18	1.700
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A3

8 Byte DIMM
[Fast Page]

NEC

MOS INTEGRATED CIRCUIT

MC-421000AA64FA

1 M-WORD BY 64-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-421000AA64FA is a 1,048,576 words by 64 bits dynamic RAM module on which 16 pieces of 4 M DRAM: μPD424400 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1,048,576 words by 64 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-421000AA64-60	60 ns	110 ns	10.42 W	420 mW (CMOS level input)
MC-421000AA64-70	70 ns	130 ns	8.74 W	
MC-421000AA64-80	80 ns	150 ns	7.90 W	

- 1,024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

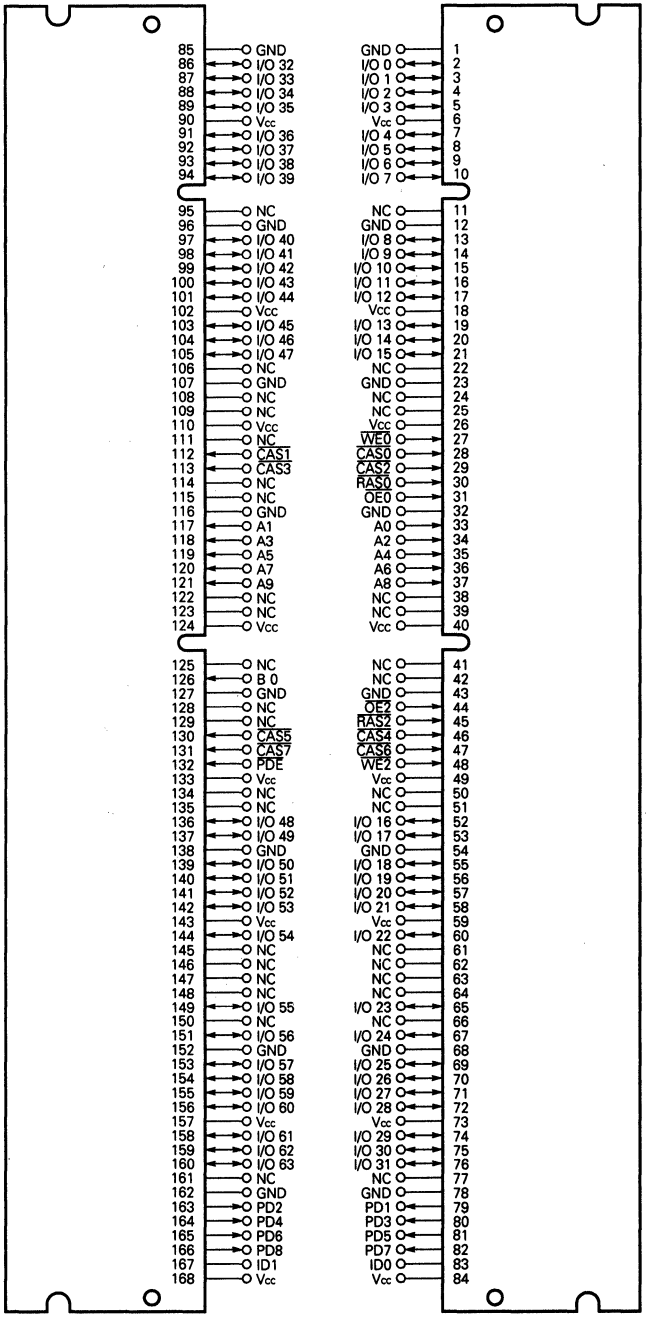
Document No. IC-3557A (Japan)

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000AA64FA-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	16 pieces of μPD424400LA (300 mil SOJ) [Double side]
MC-421000AA64FA-70	70 ns		
MC-421000AA64FA-80	80 ns		

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



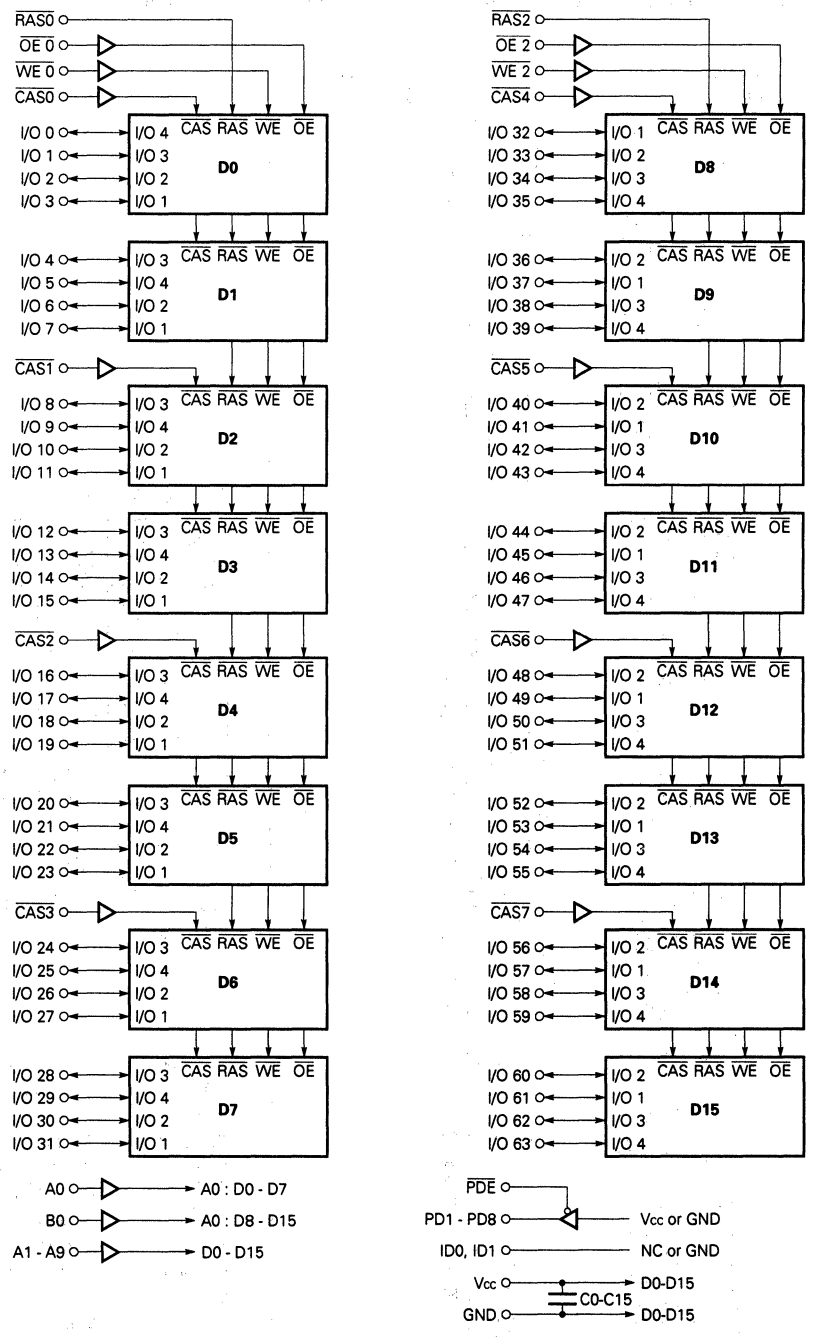
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	L	L	L
PD2	163	L	L	L
PD3	80	H	H	H
PD4	164	L	L	L
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	H	H	H
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A9, B0 : Address Inputs
I/O 0 - I/O 63 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D15 : μPD424400

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		18	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			78	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS7}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O63			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,984	mA	3, 4, 7
			t_{RAC} = 70 ns		1,664		
			t_{RAC} = 80 ns		1,504		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		96	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA		80		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,984	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		1,664		
			t_{RAC} = 80 ns		1,504		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,504	mA	3, 4, 6
			t_{RAC} = 70 ns		1,344		
			t_{RAC} = 80 ns		1,184		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,984	mA	3, 4
			t_{RAC} = 70 ns		1,664		
			t_{RAC} = 80 ns		1,504		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V	$\overline{RAS}$	−10	+10	μA	
			Others	−5	+1		
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage	V_{OH}	I_O = −5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

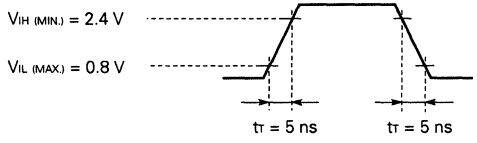
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		160		ns	
Read Modify Write Cycle Time	t_{RWC}	165		190		225		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	80		90		100		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	10, 11
Access Time Column Address	t_{AA}		35		40		45	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		40		45		50	ns	11
Access Time from $\overline{OE}$	t_{OEA}		20		25		25	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	12
$\overline{OE}$ to Data Delay Time	t_{OED}	15		15		20		ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns	12
$\overline{OE}$ Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		70		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		10		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	10		10		10		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40		45		50		ns	
Row Address Setup Time	t_{ASR}	5		5		5		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		10		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	15		15		15		ns	15
$\overline{WE}$ Pulse Width	t_{WP}	10		10		15		ns	15

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	15		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	35		40		45		ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	90		100		115		ns	17
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	55		60		70		ns	17
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	55		60		70		ns	17
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	20		25		25		ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15		15		15		ns	
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		15		ns	
$\overline{WE}$ Setup Time	t_{WSR}	0		0		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	10		10		15		ns	
Refresh Time	t_{REF}		16		16		16	ms	

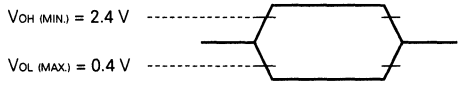
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{RAC} (MAX.)	t_{RAC} (MAX.)
$t_{RAD} > t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{AA} (MAX.)	$t_{RAD} + t_{AA}$ (MAX.)
$t_{RCD} > t_{RCD}$ (MAX.)	t_{CAC} (MAX.)	$t_{RCD} + t_{CAC}$ (MAX.)

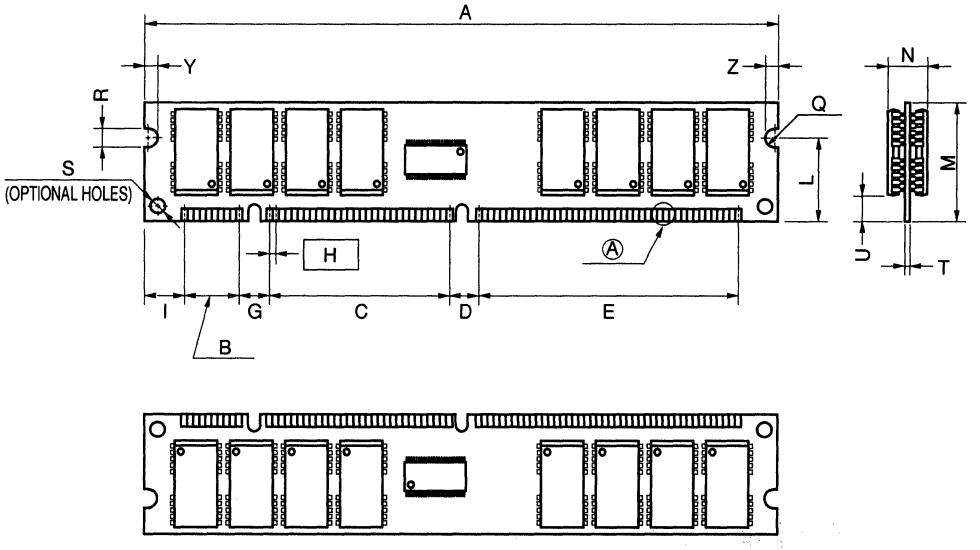
    t_{RAD} (MAX.) and t_{RCD} (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}$ (MAX.) and $t_{RCD} \geq t_{RCD}$ (MAX.) will not cause any operation problems.
11. Loading conditions are 2 TTLs and 100 pF.
12. t_{OFF} (MAX.) and t_{OEZ} (MAX.) define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. t_{CRP} (MIN.) requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either t_{RCH} (MIN.) or t_{RRH} (MIN.) should be met in read cycles.
15. t_{WP} (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, t_{WCH} (MIN.) should be met.

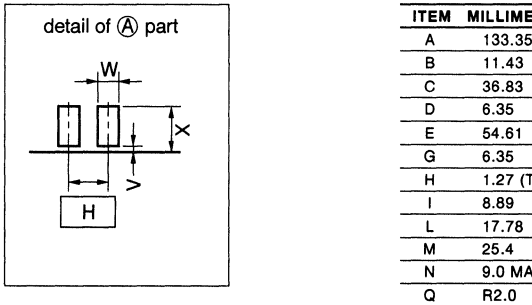
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Timing Chart
Please refer to Timing Chart 3, page 397.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
L	17.78	0.700
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54 MIN.	0.100 MIN.
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A1

NEC

MOS INTEGRATED CIRCUIT
MC-421000AA64FB

1 M-WORD BY 64-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-421000AA64FB is a 1,048,576 words by 64 bits dynamic RAM module on which 4 pieces of 16 M DRAM: μPD4218160 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1,048,576 words by 64 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-421000AA64-60	60 ns	110 ns	3.68 W	336 mW (CMOS level input)
MC-421000AA64-70	70 ns	130 ns	3.47 W	
MC-421000AA64-80	80 ns	150 ns	3.26 W	

- 1,024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

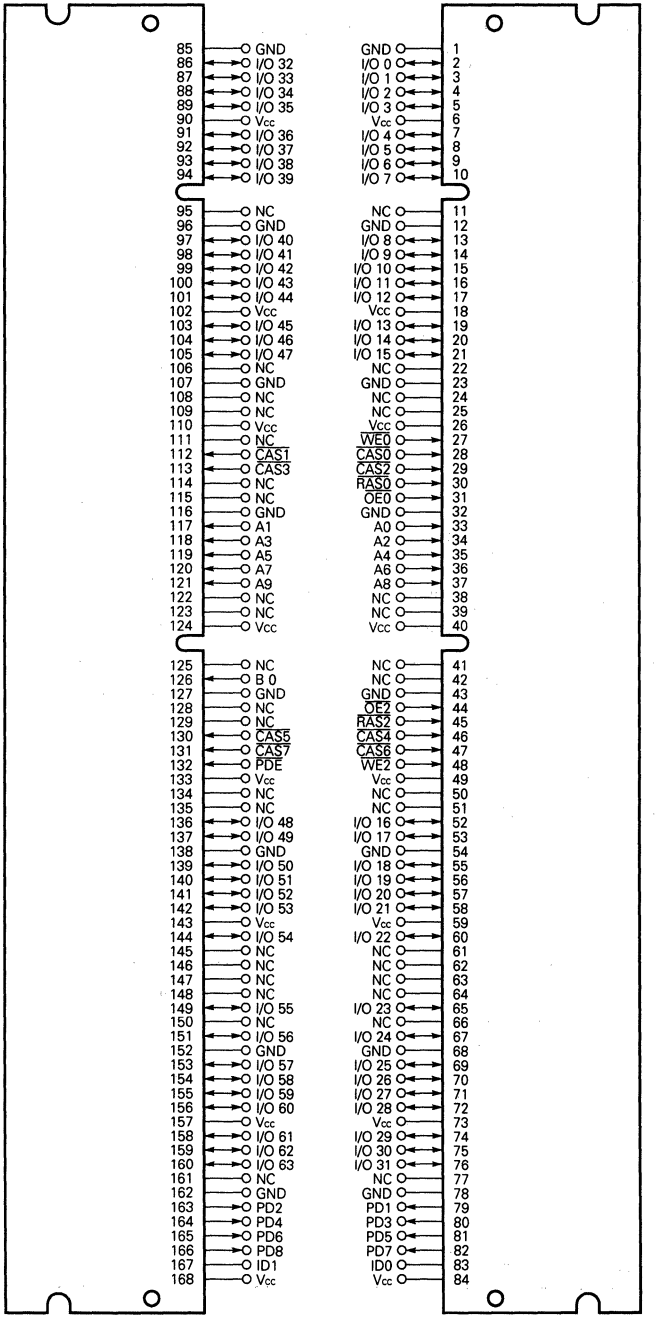
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000AA64FB-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	4 pieces of μPD4218160LE (400 mil SOJ) [Single side]
MC-421000AA64FB-70	70 ns		
MC-421000AA64FB-80	80 ns		

The information in this document is subject to change without notice.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



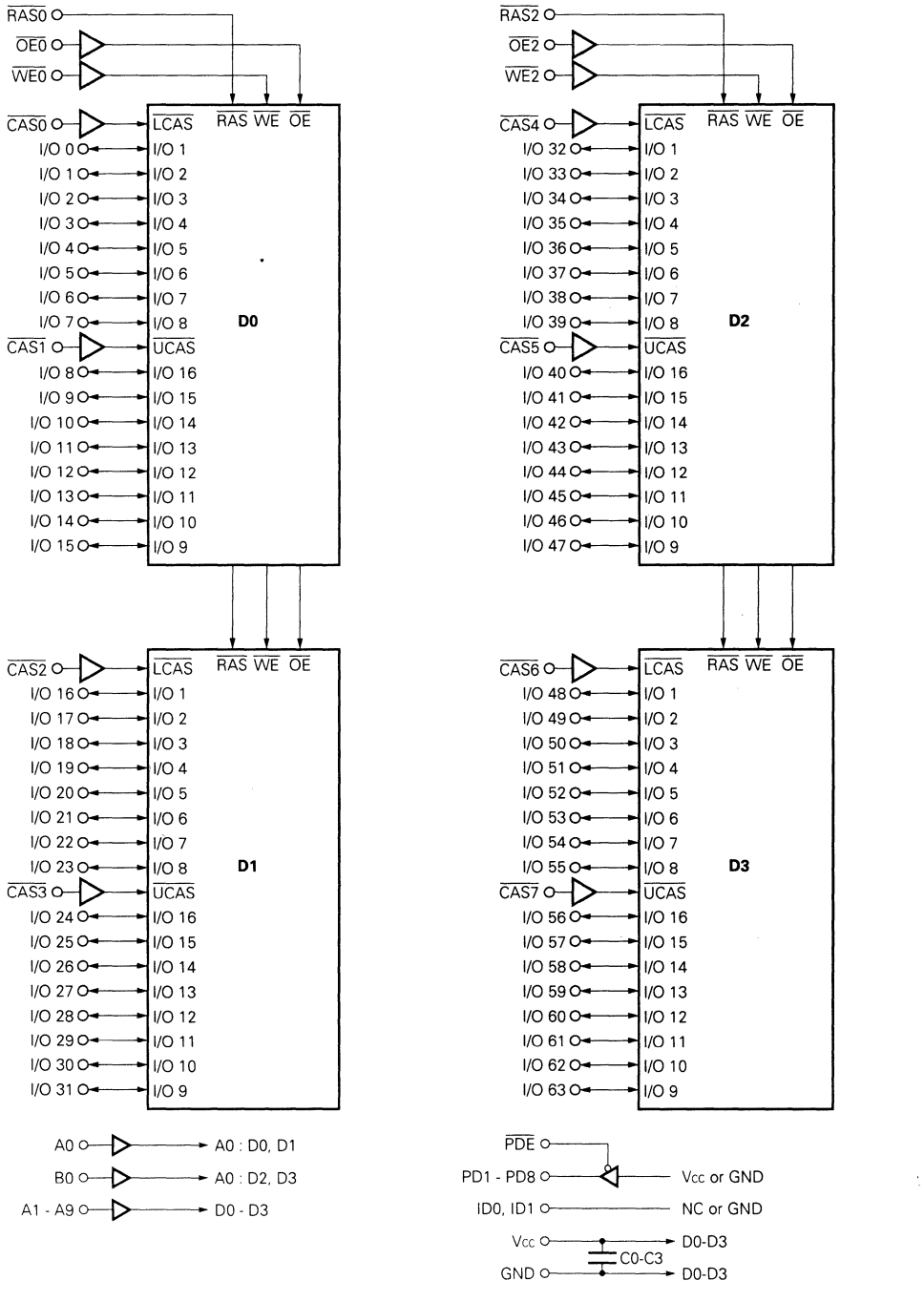
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	L	L	L
PD2	163	L	L	L
PD3	80	H	H	H
PD4	164	L	L	L
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	H	H	H
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A9, B0 : Address Inputs
I/O 0 - I/O 63 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
V_{CC} : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D3 : μPD4218160

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		6	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			45	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS7}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O63			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		700	mA	3, 4, 7
			t_{RAC} = 70 ns		660		
			t_{RAC} = 80 ns		620		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		68	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA		64		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		700	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		660		
			t_{RAC} = 80 ns		620		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		420	mA	3, 4, 6
			t_{RAC} = 70 ns		380		
			t_{RAC} = 80 ns		340		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		700	mA	3, 4
			t_{RAC} = 70 ns		660		
			t_{RAC} = 80 ns		620		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V	$\overline{RAS}$	−10	+10	μA	
			Others	−5	+1		
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage	V_{OH}	I_O = −2.5 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.1 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

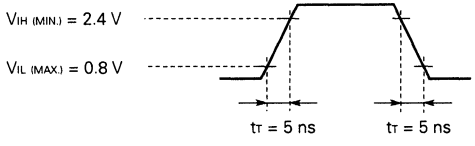
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Read Modify Write Cycle Time	t_{RWC}	173		195		215		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	85		90		105		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	10, 11
Access Time Column Address	t_{AA}		35		40		45	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		40		45		50	ns	11
Access Time from $\overline{OE}$	t_{OEA}		20		25		25	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	13	0	15	0	15	ns	12
$\overline{OE}$ to Data Delay Time	t_{OED}	13		15		15		ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	15	ns	12
$\overline{OE}$ Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40		45		50		ns	
Row Address Setup Time	t_{ASR}	5		5		5		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
$\overline{WE}$ Pulse Width	t_{WP}	10		10		15		ns	15

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	38		40		45		ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	93		105		115		ns	17
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	60		65		70		ns	17
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	58		65		70		ns	17
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	25		25		25		ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15		15		15		ns	
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		15		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		16		16		16	ms	

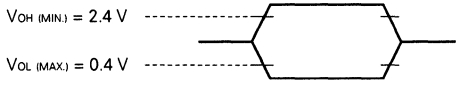
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

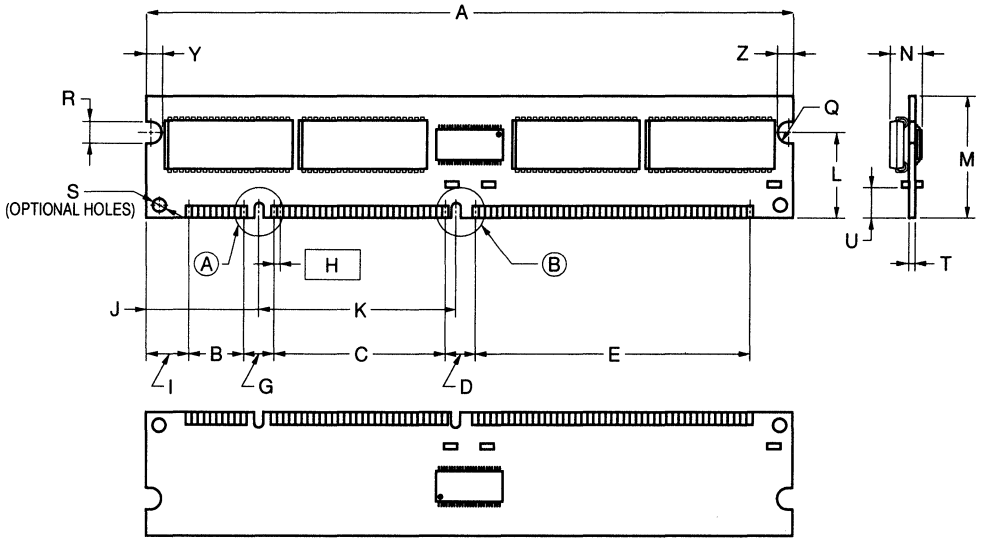
$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

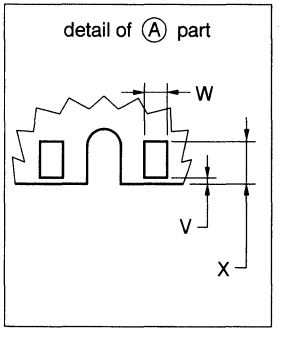
11. Loading conditions are 1 TTL and 100 pF.
12. $t_{OFF\ (MAX.)}$ and $t_{OEZ\ (MAX.)}$ define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP\ (MIN.)}$ requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
15. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

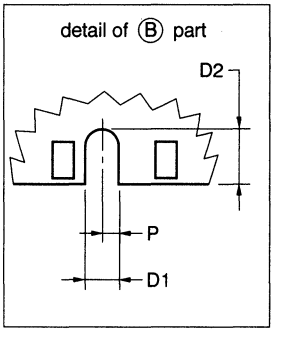
Timing Chart
Please refer to Timing Chart 4, page 411.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)







ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.1230
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.05 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.7000
M	25.4±0.13	1.000±0.006
N	9.0 MAX.	0.355 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A5

NEC

MOS INTEGRATED CIRCUIT
MC-421000AD72F

1 M-WORD BY 72-BIT DYNAMIC RAM MODULE FAST PAGE MODE (ECC)

Description

The MC-421000AD72F is a 1,048,576 words by 72 bits dynamic RAM module on which 4 pieces of 16 M DRAM: μPD4218160 and 2 pieces of 4 M DRAM: μPD424400 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1,048,576 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-421000AD72-60	60 ns	110 ns	4.94 W	347 mW (CMOS level input)
MC-421000AD72-70	70 ns	130 ns	4.52 W	
MC-421000AD72-80	80 ns	150 ns	4.20 W	

- 1,024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

Ordering Information

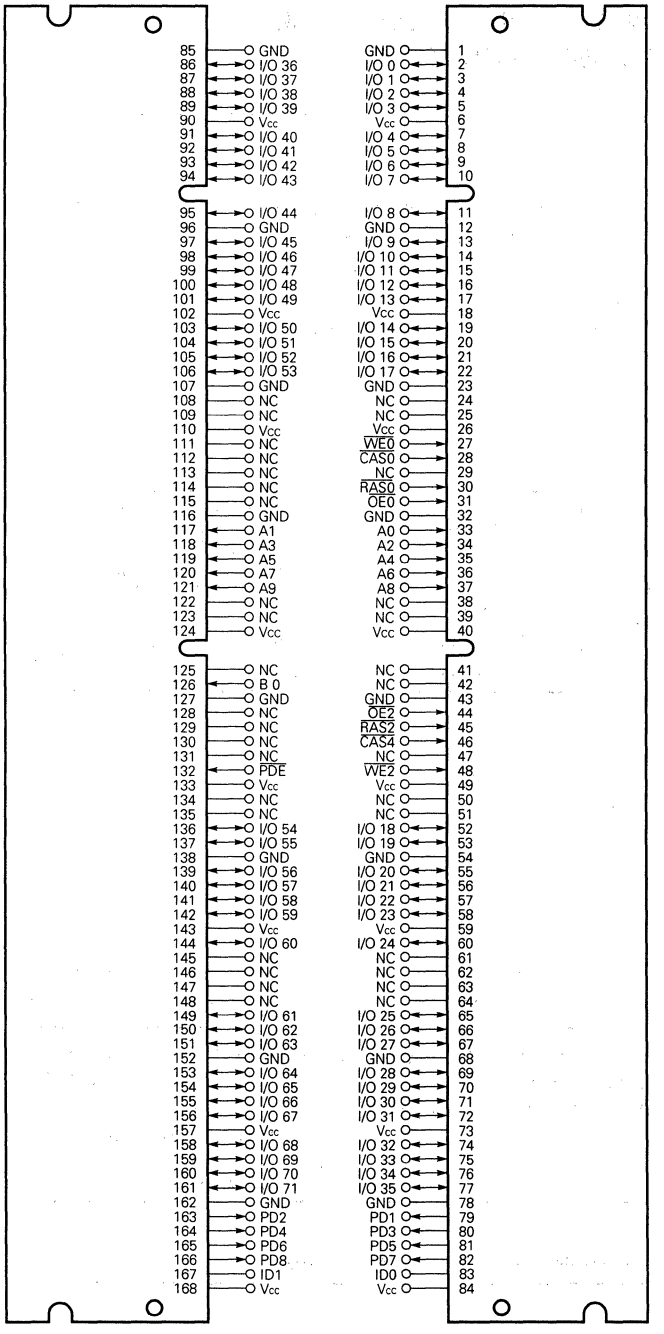
Part number	Access time (MAX.)	Package	Mounted devices
MC-421000AD72F-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	4 pieces of μPD4218160G5 (400 mil TSOP(II)) and 2 pieces of μPD424400G3 (300 mil TSOP(II)) [Double side]
MC-421000AD72F-70	70 ns		
MC-421000AD72F-80	80 ns		

The information in this document is subject to change without notice.

Document No. IC-3602 (Japan)

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



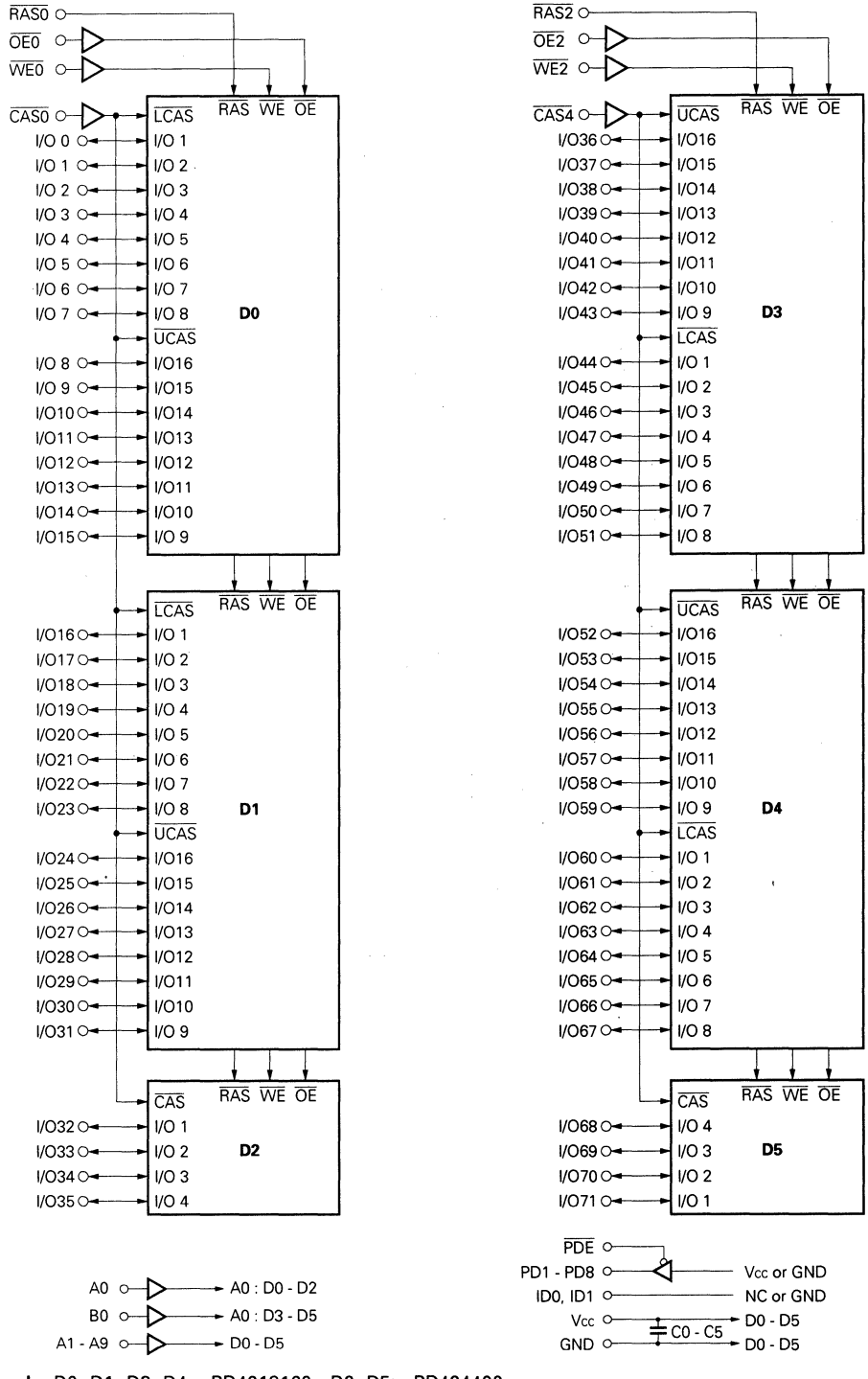
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	L	L	L
PD2	163	L	L	L
PD3	80	H	H	H
PD4	164	L	L	L
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	L	L	L
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A9, B0 : Address Inputs
I/O 0 - I/O 71 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0, D1, D3, D4: μPD4218160 D2, D5: μPD424400

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		8	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			36	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS4}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O71			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		940	mA	3, 4, 7
			t_{RAC} = 70 ns		860		
			t_{RAC} = 80 ns		800		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		72	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		66		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		940	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		860		
			t_{RAC} = 80 ns		800		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		600	mA	3, 4, 6
			t_{RAC} = 70 ns		540		
			t_{RAC} = 80 ns		480		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		940	mA	3, 4
			t_{RAC} = 70 ns		860		
			t_{RAC} = 80 ns		800		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V	$\overline{RAS}$	–10	+10	μA	
			Others	–5	+1		
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –2.5 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.1 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

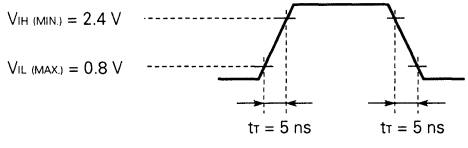
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		160		ns	
Read Modify Write Cycle Time	t_{RWC}	173		195		225		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	85		90		105		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	10, 11
Access Time Column Address	t_{AA}		35		40		45	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		40		45		50	ns	11
Access Time from $\overline{OE}$	t_{OEA}		20		25		25	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	12
$\overline{OE}$ to Data Delay Time	t_{OED}	15		15		20		ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns	12
$\overline{OE}$ Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		70		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		10		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	10		10		10		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40		45		50		ns	
Row Address Setup Time	t_{ASR}	5		5		5		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		10		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	15		15		15		ns	15
$\overline{WE}$ Pulse Width	t_{WP}	10		10		15		ns	15

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	38		40		45		ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	93		105		115		ns	17
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	60		65		70		ns	17
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	58		65		70		ns	17
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	25		25		25		ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15		15		15		ns	
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		16		16		16	ms	

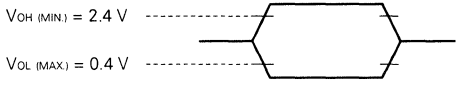
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

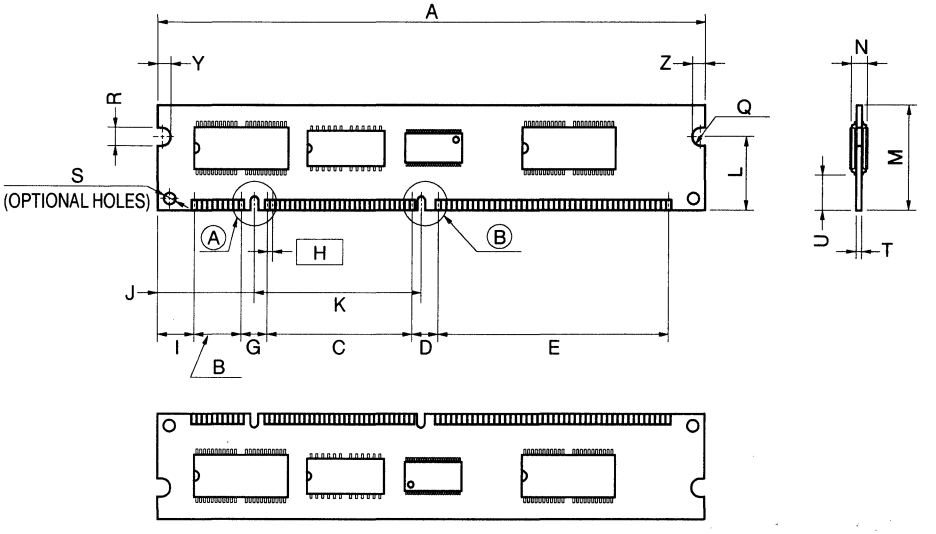
$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

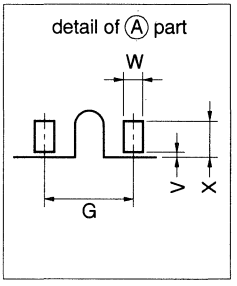
11. Loading conditions are 1 TTL and 100 pF.
12. $t_{OFF\ (MAX.)}$ and $t_{OEZ\ (MAX.)}$ define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP\ (MIN.)}$ requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
15. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

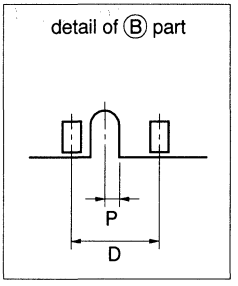
Timing Chart
Please refer to Timing Chart 3, page 397.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)







ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R 2.0	R 0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	φ3.0	φ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
X	2.54	0.100
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A4

NEC

MOS INTEGRATED CIRCUIT
MC-422000AA64

2 M-WORD BY 64-BIT DYNAMIC RAM MODULE
FAST PAGE MODE

Description

The MC-422000AA64 is a 2,097,152 words by 64 bits dynamic RAM module on which 8 pieces of 16 M DRAM: μPD4218160 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 2,097,152 words by 64 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-422000AA64-60	60 ns	110 ns	3.72 W	357 mW (CMOS level input)
MC-422000AA64-70	70 ns	130 ns	3.51 W	
MC-422000AA64-80	80 ns	150 ns	3.30 W	

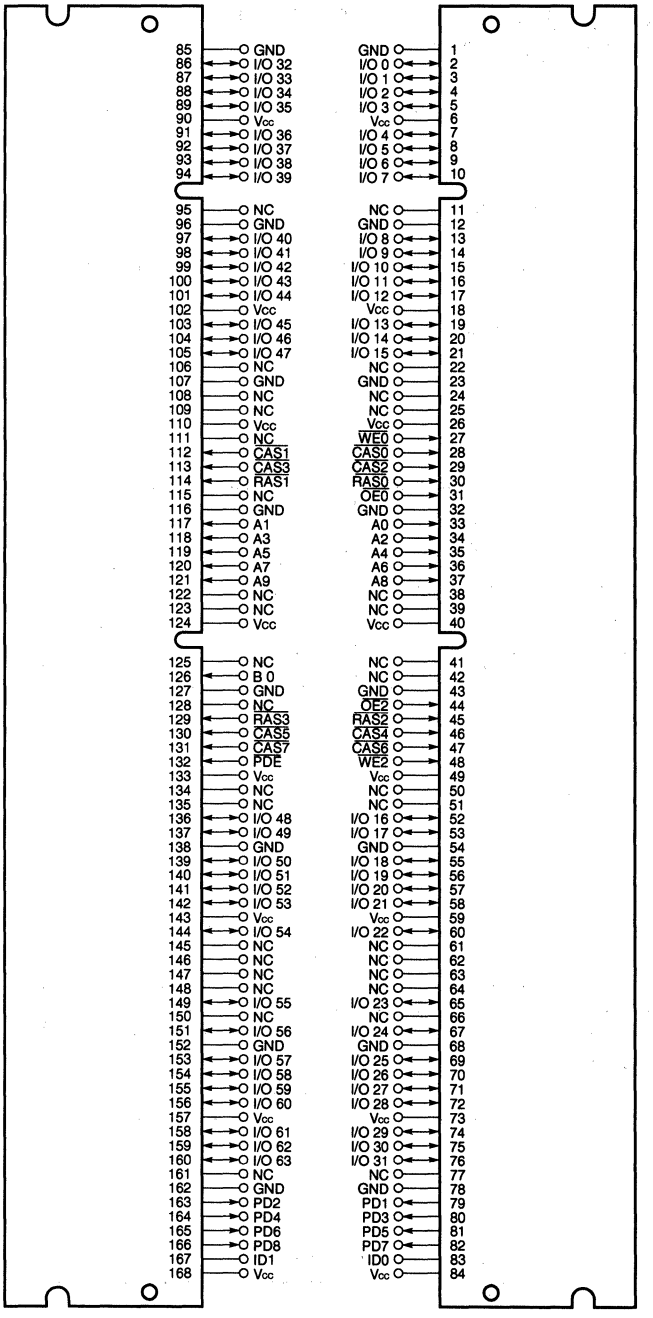
- 1,024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000AA64FB-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	8 pieces of μPD4218160LE (400 mil SOJ) [Double side]
MC-422000AA64FB-70	70 ns		
MC-422000AA64FB-80	80 ns		

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



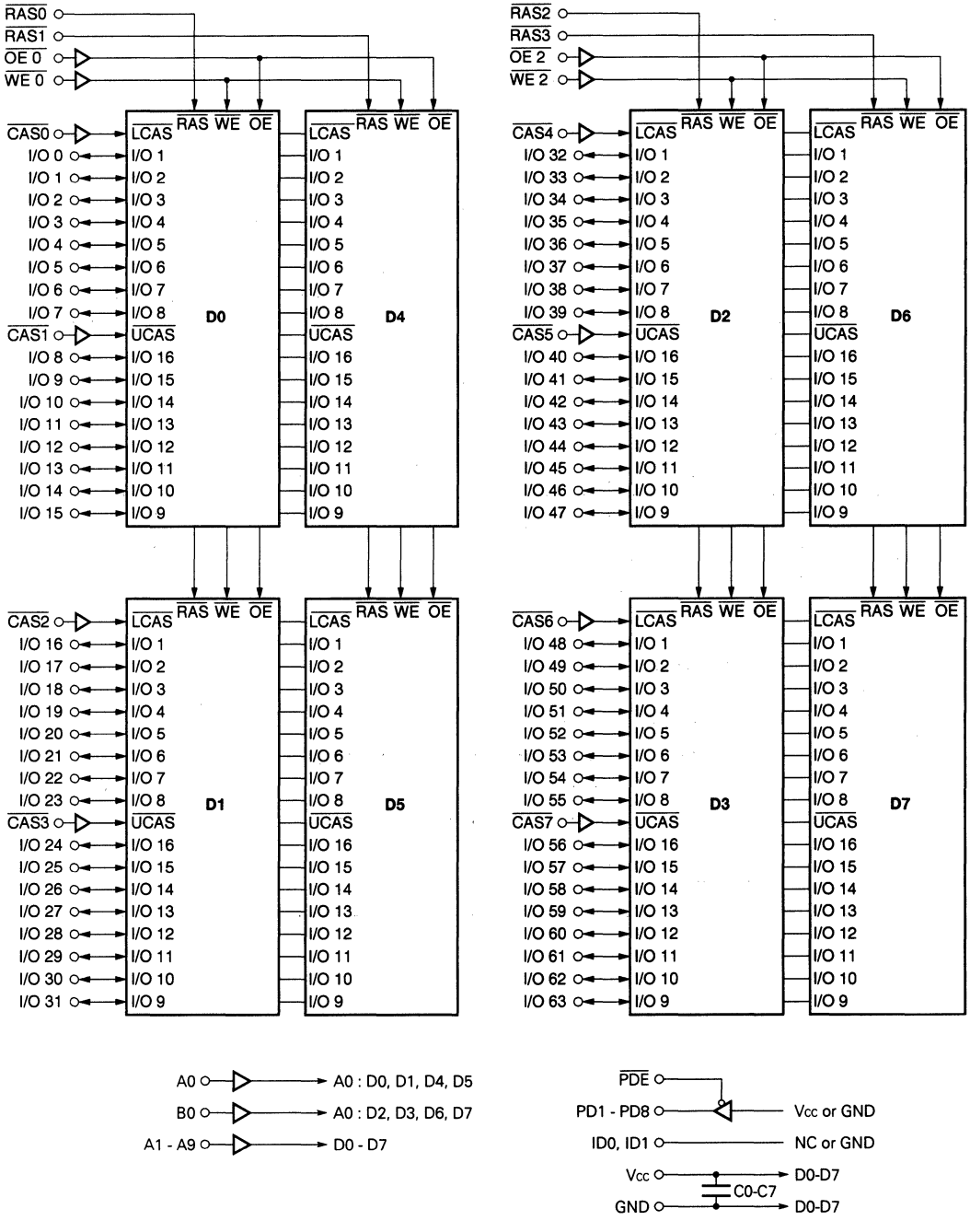
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	H	H	H
PD2	163	L	L	L
PD3	80	H	H	H
PD4	164	L	L	L
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	H	H	H
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A9, B0 : Address Inputs
I/O 0 - I/O 63 : Data Inputs/Outputs
$\overline{RAS0}$ - $\overline{RAS3}$: Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D7 : μPD4218160

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		10	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS3}$			45	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS7}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O63			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition			MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns			708	mA	3, 4, 7
			t_{RAC} = 70 ns			668		
			t_{RAC} = 80 ns			628		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA			76	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA			68		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns			708	mA	3, 4, 5, 7
			t_{RAC} = 70 ns			668		
			t_{RAC} = 80 ns			628		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns			428	mA	3, 4, 6
			t_{RAC} = 70 ns			388		
			t_{RAC} = 80 ns			348		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns			708	mA	3, 4
			t_{RAC} = 70 ns			668		
			t_{RAC} = 80 ns			628		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.25 V All other pins not under test = 0 V		$\overline{RAS}$	−10	+10	μA	
				Others	−5	+1		
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.25 V Output is disabled (Hi-Z)			−10	+10	μA	
High level output voltage	V_{OH}	I_O = −2.5 mA			2.4		V	
Low level output voltage	V_{OL}	I_O = +2.1 mA				0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

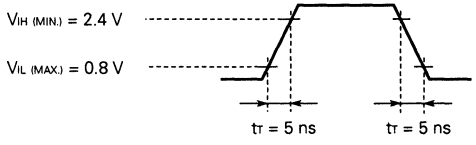
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Read Modify Write Cycle Time	t_{RWC}	173		195		215		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	83		90		95		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	10, 11
Access Time Column Address	t_{AA}		35		40		45	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		40		45		50	ns	11
Access Time from $\overline{OE}$	t_{OEA}		20		25		25	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	13	0	15	0	15	ns	12
$\overline{OE}$ to Data Delay Time	t_{OED}	13		15		15		ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	15	ns	12
$\overline{OE}$ Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	20		23		25		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		10		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40		45		50		ns	
Row Address Setup Time	t_{ASR}	5		5		5		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
$\overline{WE}$ Pulse Width	t_{WP}	10		10		15		ns	15

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	38		40		45		ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	93		105		115		ns	17
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	58		65		70		ns	17
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	58		65		70		ns	17
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	25		25		25		ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15		15		15		ns	
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		16		16		16	ms	

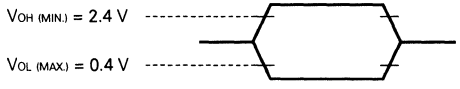
Notes

1. All voltages are referenced to GND.
2. After power up ($V_{CC} \geq V_{CC\ (MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification

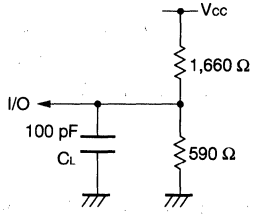


10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

11. Output load condition



12. $t_{OFF\ (MAX.)}$ and $t_{OEZ\ (MAX.)}$ define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.

13. $t_{CRP\ (MIN.)}$ requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.

14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

15. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

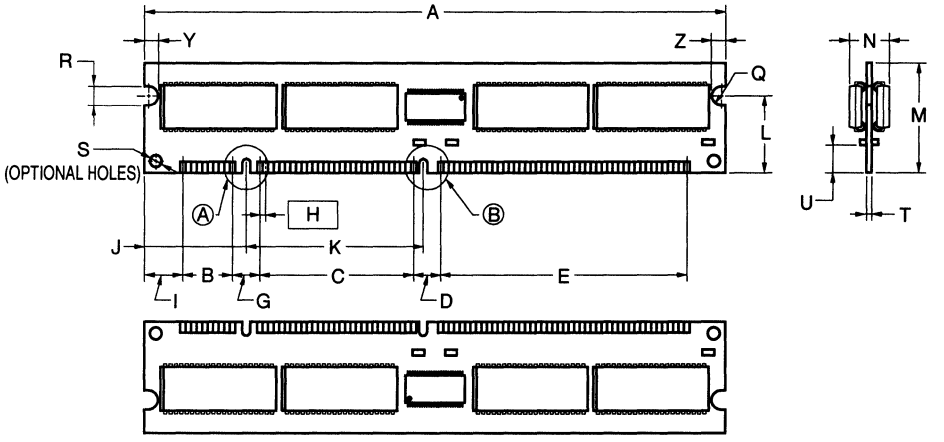
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.

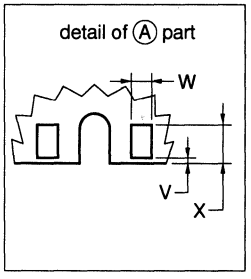
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

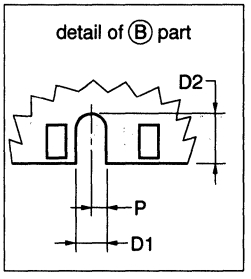
Timing Chart
Please refer to Timing Chart 4, page 411.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)







ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.1230
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.05 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.7000
M	25.4±0.13	1.000±0.006
N	9.0 MAX.	0.355 MAX.
P	1.0	0.039
Q	R 2.0	R 0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A7

NEC

MOS INTEGRATED CIRCUIT
MC-422000AB72F

2 M-WORD BY 72-BIT DYNAMIC RAM MODULE
FAST PAGE MODE (ECC)

Description

The MC-422000AB72F is a 2,097,152 words by 72 bits dynamic RAM module on which 9 pieces of 16 M DRAM: μPD4217800 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 2,097,152 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-422000AB72-60	60 ns	110 ns	5.53 W	383 mW (CMOS level input)
MC-422000AB72-70	70 ns	130 ns	5.06 W	
MC-422000AB72-80	80 ns	150 ns	4.59 W	

- 2,048 refresh cycles/32 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

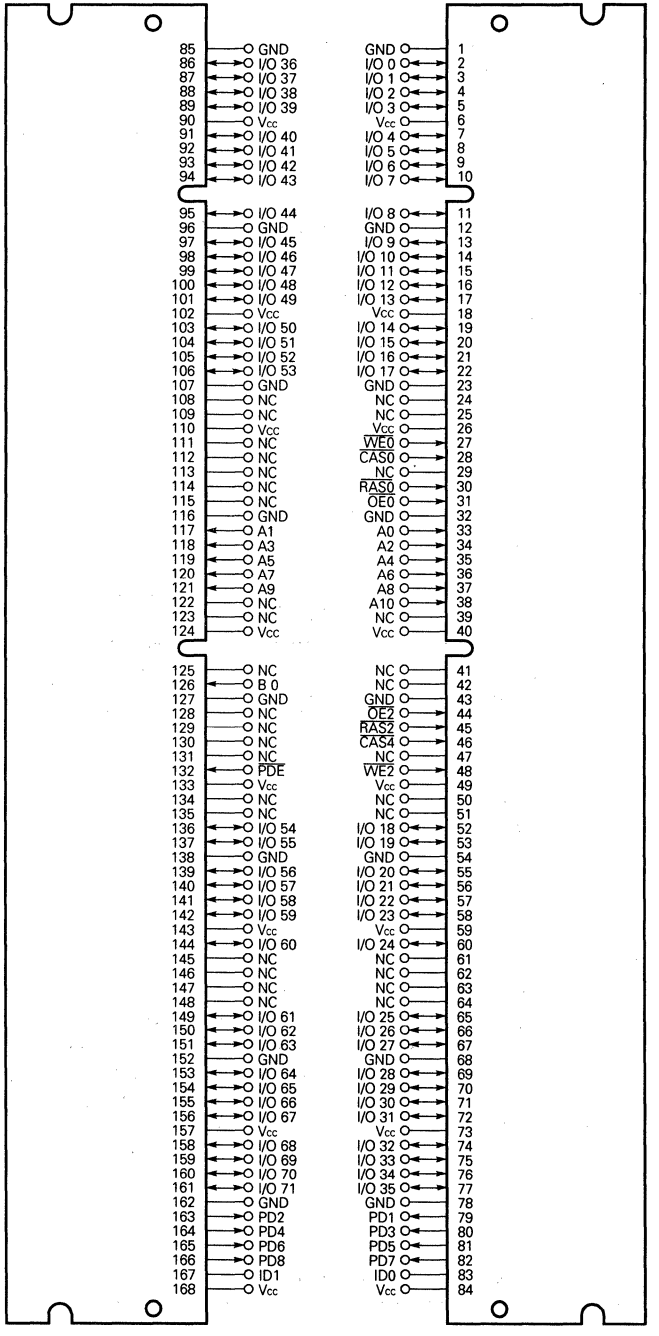
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000AB72F-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	9 pieces of μPD4217800G5 (400 mil TSOP(II)) [Double side]
MC-422000AB72F-70	70 ns		
MC-422000AB72F-80	80 ns		

Document No. IC-3542 (Japan)

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



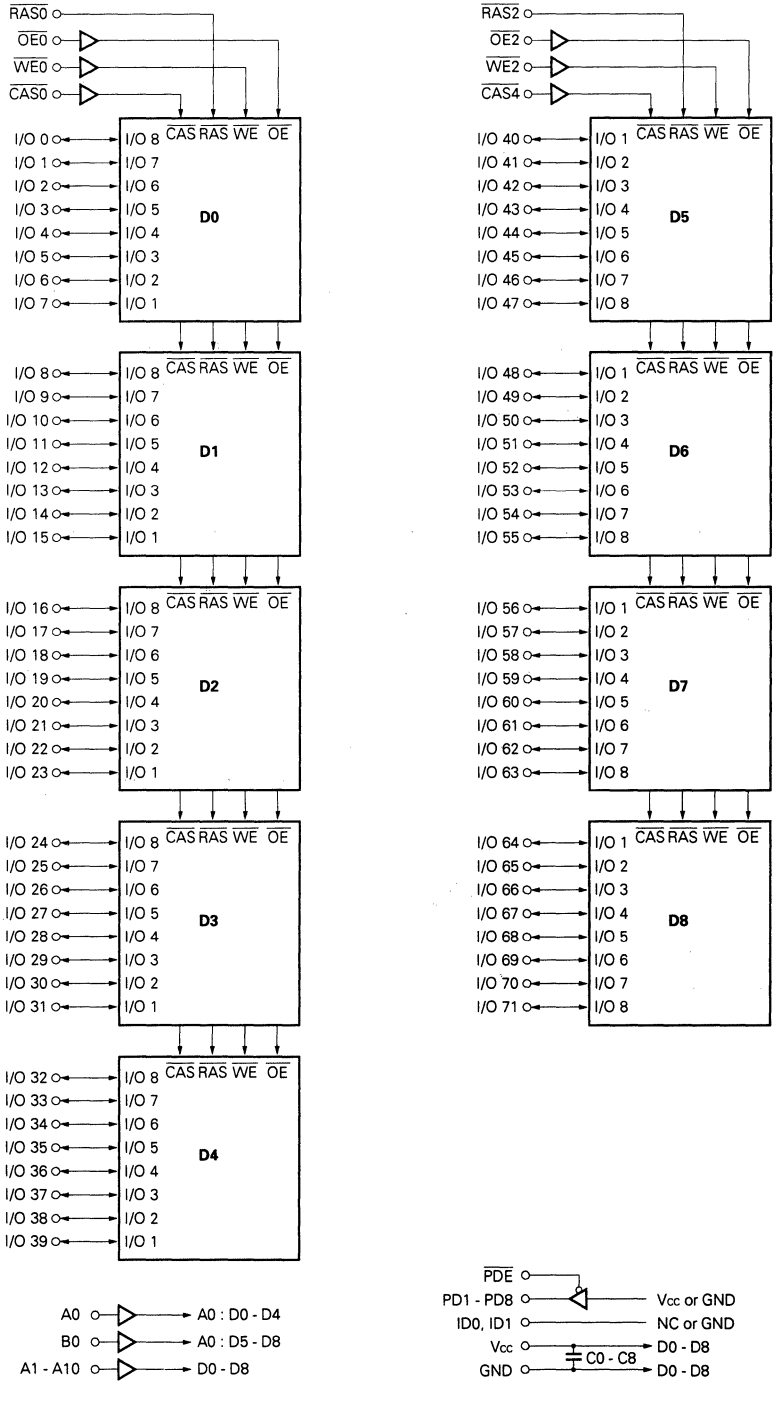
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	H	H	H
PD2	163	L	L	L
PD3	80	L	L	L
PD4	164	H	H	H
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	L	L	L
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A10, B0 : Address Inputs
I/O 0 - I/O 71 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D8 : μPD4217800

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		11	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			50	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS4}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O71			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,054	mA	3, 4, 7
			t_{RAC} = 70 ns		964		
			t_{RAC} = 80 ns		874		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		82	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA		73		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,054	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		964		
			t_{RAC} = 80 ns		874		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		694	mA	3, 4, 6
			t_{RAC} = 70 ns		604		
			t_{RAC} = 80 ns		514		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,054	mA	3, 4
			t_{RAC} = 70 ns		964		
			t_{RAC} = 80 ns		874		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V	$\overline{RAS}$	−10	+10	μA	
			Others	−5	+1		
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage	V_{OH}	I_O = −5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

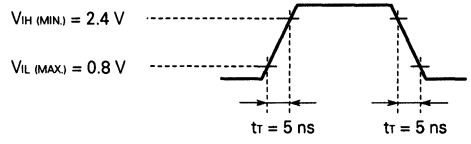
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Read Modify Write Cycle Time	t_{RWC}	173		195		215		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	85		90		100		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		20		23		25	ns	10, 11
Access Time Column Address	t_{AA}		35		40		45	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		40		45		50	ns	11
Access Time from $\overline{OE}$	t_{OEA}		20		23		25	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	13	0	15	0	15	ns	12
$\overline{OE}$ to Data Delay Time	t_{OED}	13		15		15		ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	15	ns	12
$\overline{OE}$ Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40		45		50		ns	
Row Address Setup Time	t_{ASR}	5		5		5		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
$\overline{WE}$ Pulse Width	t_{WP}	10		10		15		ns	15

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	38		43		45		ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	93		105		115		ns	17
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	58		65		70		ns	17
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	58		65		70		ns	17
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	25		25		25		ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15		15		15		ns	
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		32		32		32	ms	

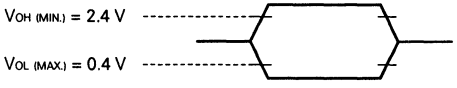
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

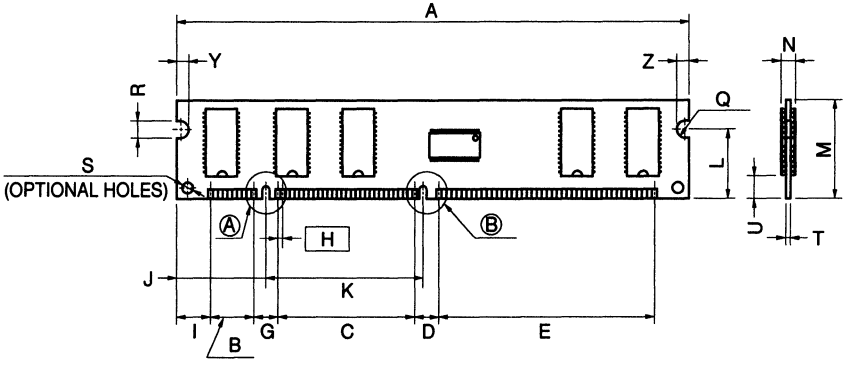
$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

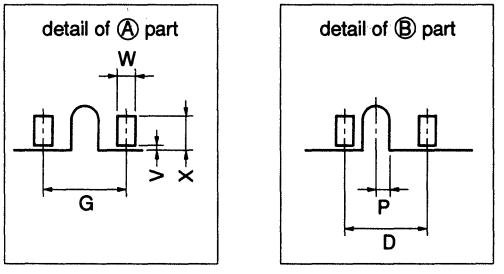
11. Loading conditions are 2 TTLs and 100 pF.
12. $t_{OFF\ (MAX.)}$ and $t_{OEZ\ (MAX.)}$ define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP\ (MIN.)}$ requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
15. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Timing Chart
Please refer to Timing Chart 3, page 397.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54	0.100
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A6

NEC

MOS INTEGRATED CIRCUIT

MC-422000LAB72F

3.3 V OPERATION 2 M-WORD BY 72-BIT DYNAMIC RAM MODULE FAST PAGE MODE (ECC)

Description

The MC-422000LAB72F is a 2,097,152 words by 72 bits dynamic RAM module on which 9 pieces of 16 M DRAM: μPD4217800L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 2,097,152 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-422000LAB72-A60	60 ns	110 ns	3.28 W	147.6 mW (CMOS level input)
MC-422000LAB72-A70	70 ns	130 ns	2.95 W	
MC-422000LAB72-A80	80 ns	150 ns	2.63 W	

- 2,048 refresh cycles/32 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

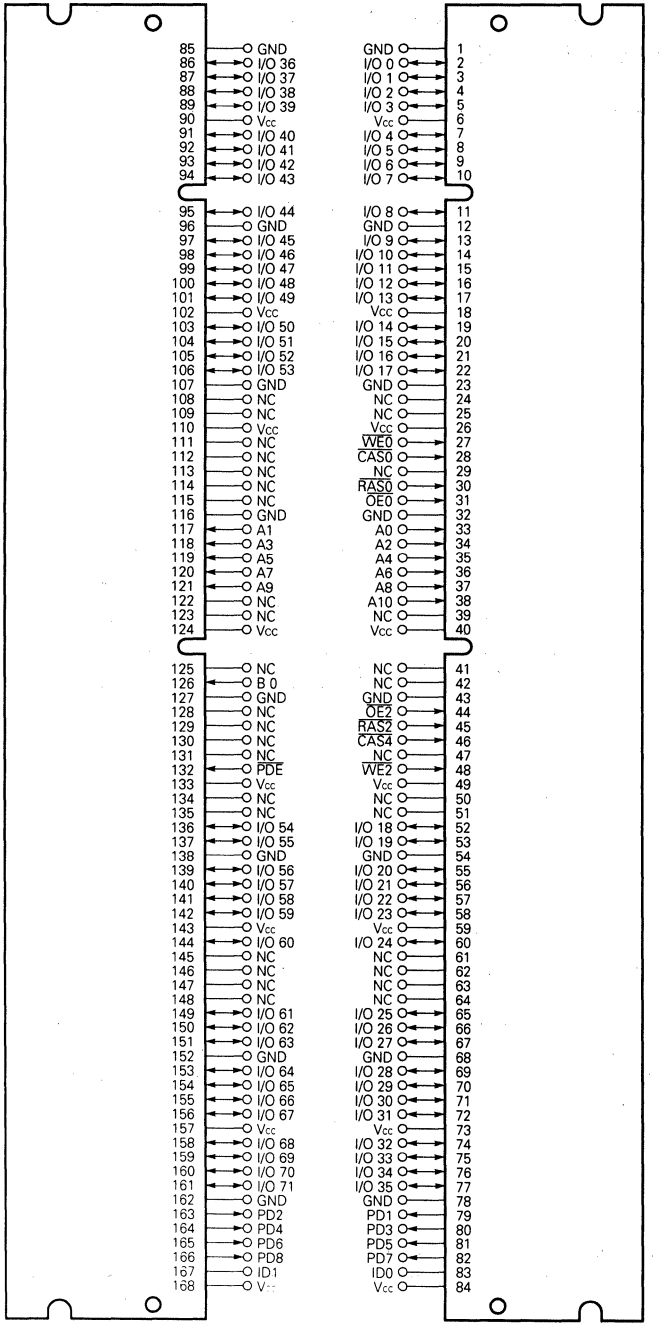
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000LAB72F-A60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	9 pieces of μPD4217800LG5 (400 mil TSOP(II)) [Double side]
MC-422000LAB72F-A70	70 ns		
MC-422000LAB72F-A80	80 ns		

The information in this document is subject to change without notice.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



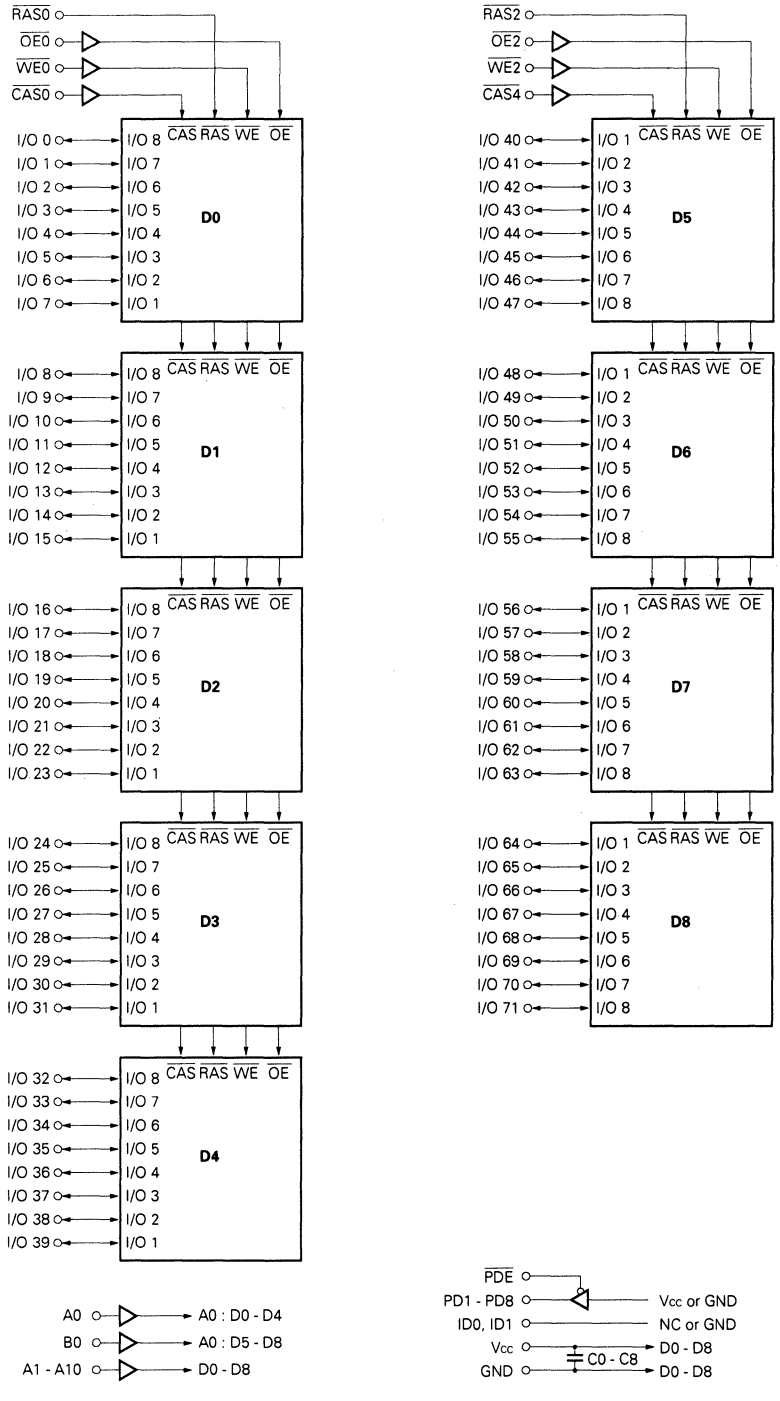
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	H	H	H
PD2	163	L	L	L
PD3	80	L	L	L
PD4	164	H	H	H
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	L	L	L
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A10, B0 : Address Inputs
I/O 0 - I/O 71 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D8 : μPD4217800L

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		11	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			50	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS4}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O71			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		910	mA	3, 4, 7
			t_{RAC} = 70 ns		820		
			t_{RAC} = 80 ns		730		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		82	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA		41		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		910	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		820		
			t_{RAC} = 80 ns		730		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		640	mA	3, 4, 6
			t_{RAC} = 70 ns		550		
			t_{RAC} = 80 ns		460		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		910	mA	3, 4
			t_{RAC} = 70 ns		820		
			t_{RAC} = 80 ns		730		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V	$\overline{RAS}$	−5	+5	μA	
			Others	−5	+1		
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		−5	+5	μA	
High level output voltage	V_{OH}	I_O = −2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

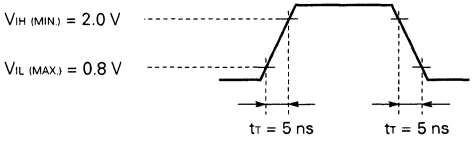
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Read Modify Write Cycle Time	t_{RWC}	173		195		215		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	85		90		100		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		20		23		25	ns	10, 11
Access Time Column Address	t_{AA}		35		40		45	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		40		45		50	ns	11
Access Time from $\overline{OE}$	t_{OEA}		20		23		25	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	13	0	15	0	15	ns	12
$\overline{OE}$ to Data Delay Time	t_{OED}	13		15		15		ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	15	ns	12
$\overline{OE}$ Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40		45		50		ns	
Row Address Setup Time	t_{ASR}	5		5		5		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
$\overline{WE}$ Pulse Width	t_{WP}	10		10		15		ns	15

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	38		43		45		ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	93		105		115		ns	17
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	58		65		70		ns	17
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	58		65		70		ns	17
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	25		25		25		ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15		15		15		ns	
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		32		32		32	ms	

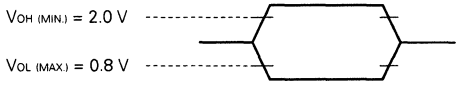
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

11. Loading conditions are 1 TTL and 100 pF.

12. $t_{OFF\ (MAX.)}$ and $t_{OEZ\ (MAX.)}$ define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.

13. $t_{CRP\ (MIN.)}$ requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.

14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

15. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

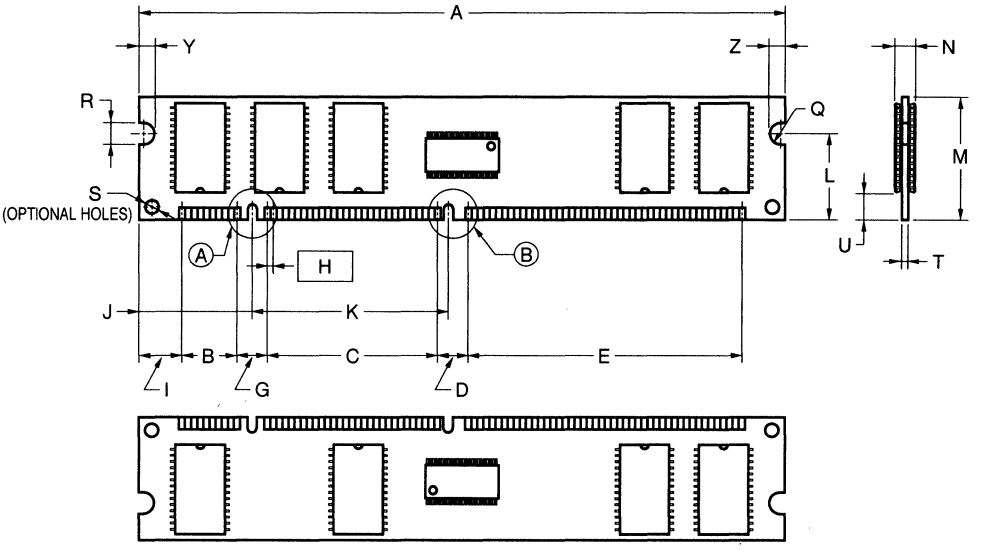
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.

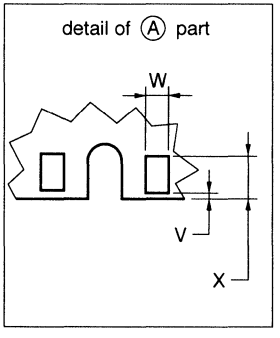
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

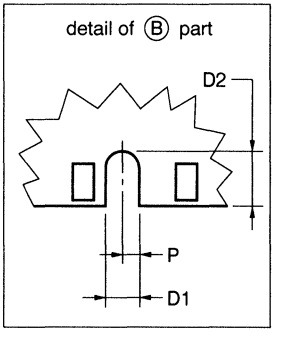
Timing Chart
Please refer to Timing Chart 3, page 397.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)







ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.123
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.50	0.925
K	43.18	1.70
L	17.78	0.700
M	25.4±0.13	1.000±0.006
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A8

NEC

MOS INTEGRATED CIRCUIT
MC-424000AB72F

4 M-WORD BY 72-BIT DYNAMIC RAM MODULE
FAST PAGE MODE (ECC)

Description

The MC-424000AB72F is a 4,194,304 words by 72 bits dynamic RAM module on which 18 pieces of 16 M DRAM: μPD4217400 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 4,194,304 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-424000AB72-60	60 ns	110 ns	10.73 W	430 mW (CMOS level input)
MC-424000AB72-70	70 ns	130 ns	9.79 W	
MC-424000AB72-80	80 ns	150 ns	8.84 W	

- 2,048 refresh cycles/32 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

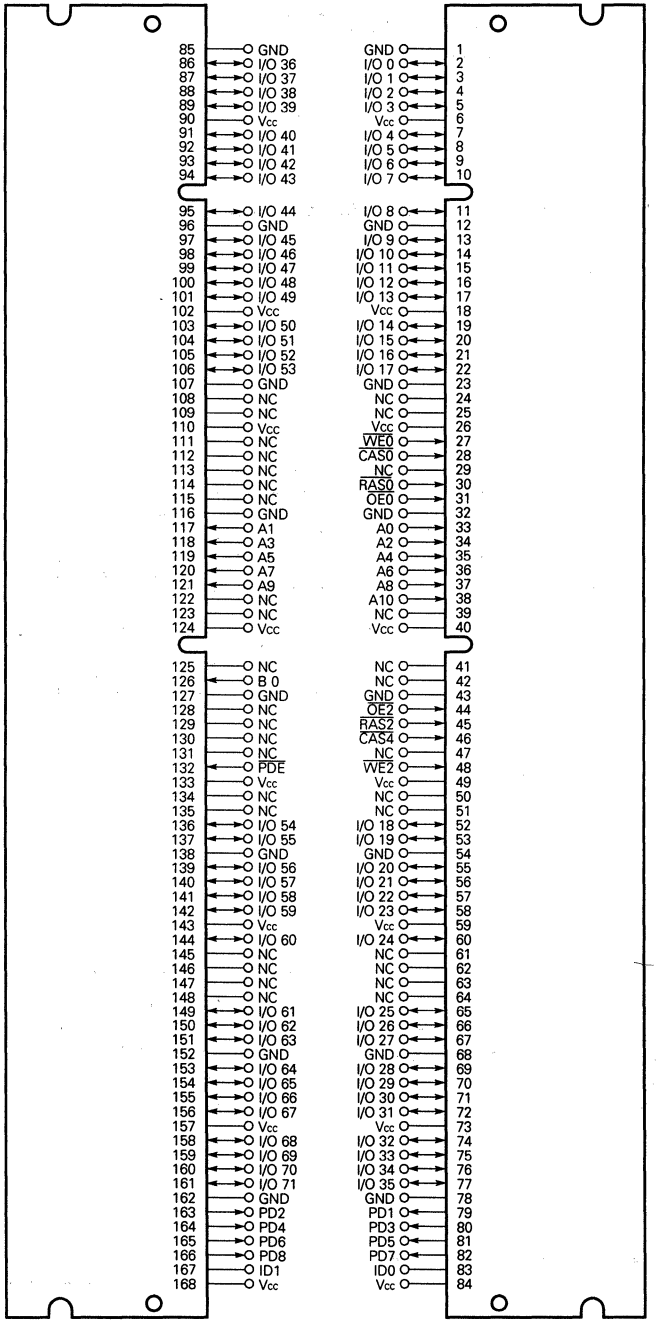
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-424000AB72F-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	18 pieces of μPD4217400G3 (300 mil TSOP(II)) [Double side]
MC-424000AB72F-70	70 ns		
MC-424000AB72F-80	80 ns		

Document No. IC-3598 (Japan)

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



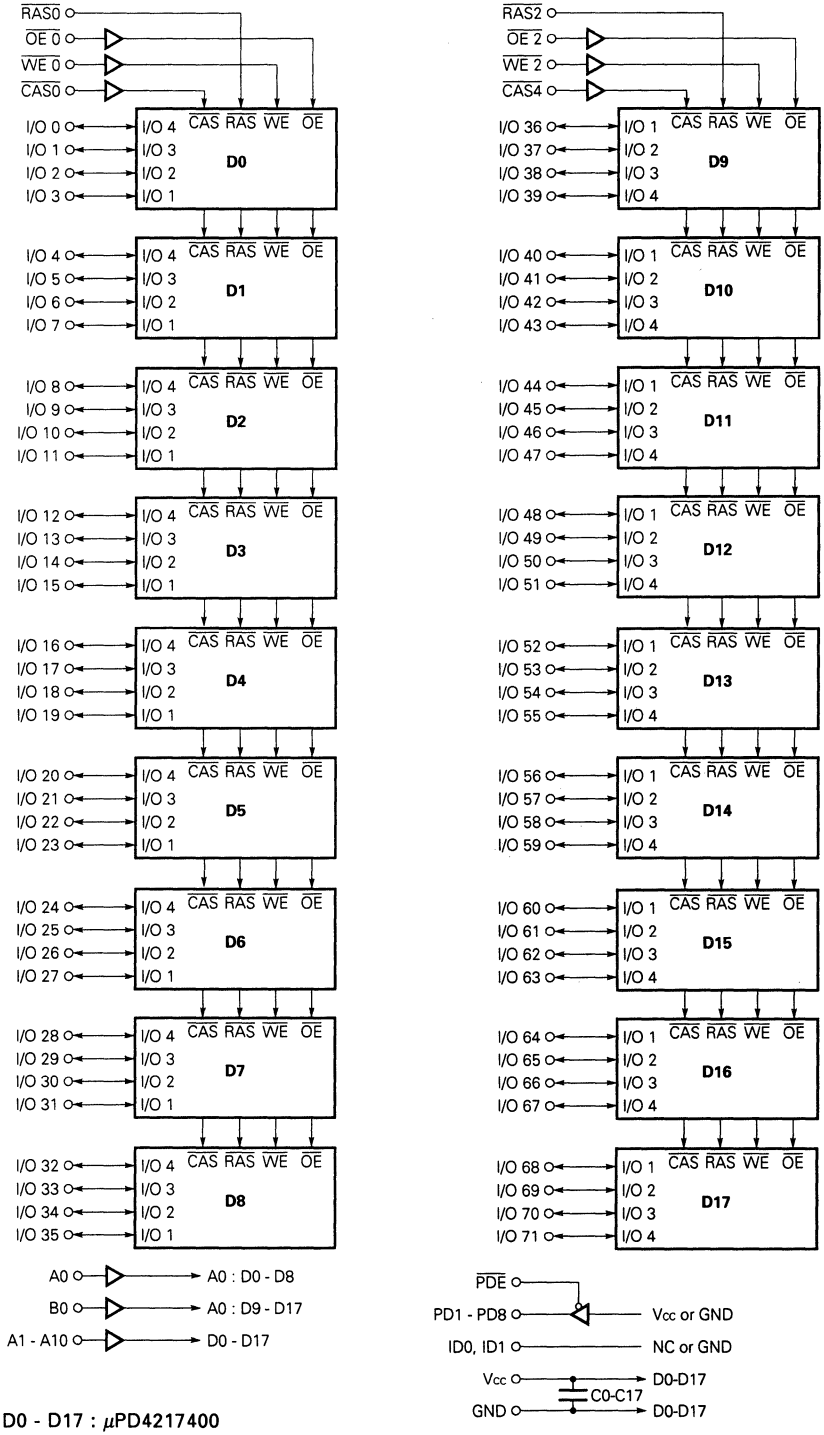
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	H	H	H
PD2	163	H	H	H
PD3	80	L	L	L
PD4	164	H	H	H
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	L	L	L
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A10, B0 : Address Inputs
I/O 0 - I/O 71 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D17 : μPD4217400

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		20	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			78	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS4}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O71			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC}$ (MIN.) I_O = 0 mA	t_{RAC} = 60 ns		2,044	mA	3, 4, 7
			t_{RAC} = 70 ns		1,864		
			t_{RAC} = 80 ns		1,684		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH}$ (MIN.)	I_O = 0 mA		100	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA		82		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH}$ (MIN.) $t_{RC} = t_{RC}$ (MIN.) I_O = 0 mA	t_{RAC} = 60 ns		2,044	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		1,864		
			t_{RAC} = 80 ns		1,684		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL}$ (MAX.), $\overline{CAS}$ Cycling $t_{PC} = t_{PC}$ (MIN.) I_O = 0 mA	t_{RAC} = 60 ns		1,324	mA	3, 4, 6
			t_{RAC} = 70 ns		1,144		
			t_{RAC} = 80 ns		964		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC}$ (MIN.) I_O = 0 mA	t_{RAC} = 60 ns		2,044	mA	3, 4
			t_{RAC} = 70 ns		1,864		
			t_{RAC} = 80 ns		1,684		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V	$\overline{RAS}$	−10	+10	μA	
			Others	−5	+1		
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage	V_{OH}	I_O = −5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

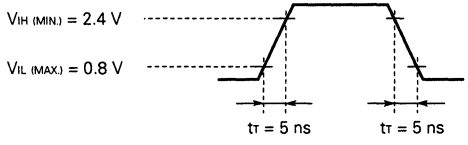
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Read Modify Write Cycle Time	t_{RWC}	175		195		220		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	85		90		105		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		20		23		25	ns	10, 11
Access Time Column Address	t_{AA}		35		40		45	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		40		45		50	ns	11
Access Time from $\overline{OE}$	t_{OEA}		20		23		25	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	12
$\overline{OE}$ to Data Delay Time	t_{OED}	15		15		20		ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns	12
$\overline{OE}$ Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40		45		50		ns	
Row Address Setup Time	t_{ASR}	5		5		5		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
$\overline{WE}$ Pulse Width	t_{WP}	10		10		15		ns	15

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	40		43		50		ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	95		105		120		ns	17
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	58		65		70		ns	17
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	60		65		75		ns	17
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	25		25		25		ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15		15		15		ns	
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		32		32		32	ms	

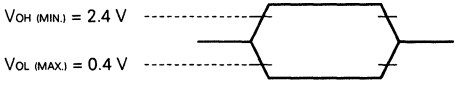
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

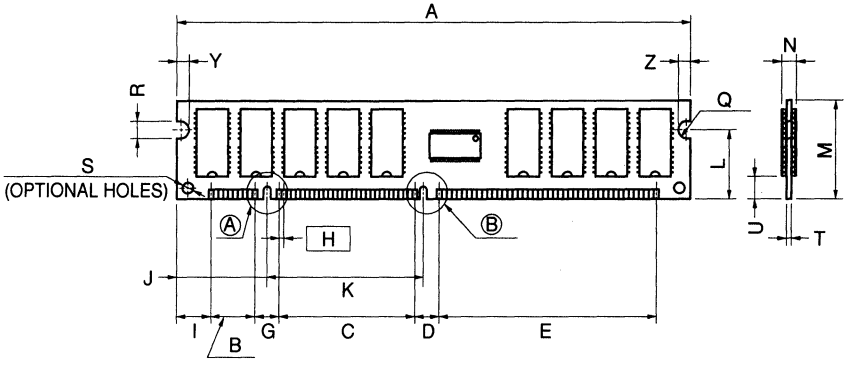
$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

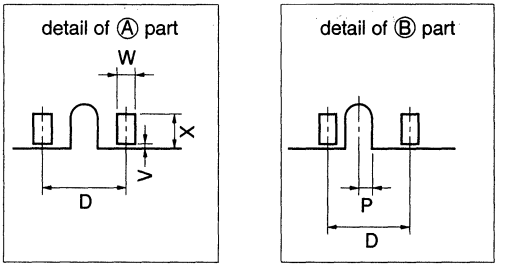
11. Loading conditions are 2 TTLs and 100 pF.
12. $t_{OFF\ (MAX.)}$ and $t_{OEZ\ (MAX.)}$ define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP\ (MIN.)}$ requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
15. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Timing Chart
Please refer to Timing Chart 3, page 397.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A2

NEC

MOS INTEGRATED CIRCUIT
MC-424000AC72F

4 M-WORD BY 72-BIT DYNAMIC RAM MODULE
FAST PAGE MODE (ECC)

Description

The MC-424000AC72F is a 4,194,304 words by 72 bits dynamic RAM module on which 18 pieces of 16 M DRAM: μPD4216400 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 4,194,304 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-424000AC72-60	60 ns	110 ns	8.84 W	430 mW (CMOS level input)
MC-424000AC72-70	70 ns	130 ns	7.90 W	
MC-424000AC72-80	80 ns	150 ns	6.95 W	

- 4,096 refresh cycles/64 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.25 V power supply

Ordering Information

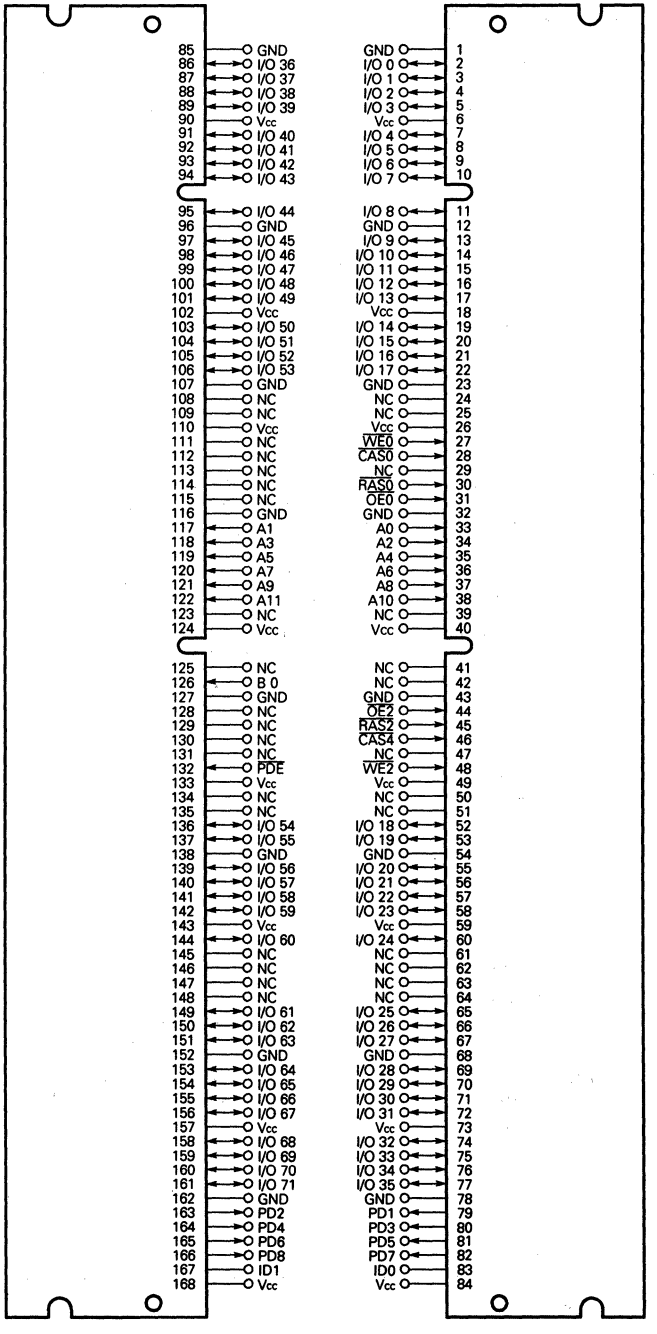
Part number	Access time (MAX.)	Package	Mounted devices
MC-424000AC72F-60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	18 pieces of μPD4216400G3 (300 mil TSOP(II)) [Double side]
MC-424000AC72F-70	70 ns		
MC-424000AC72F-80	80 ns		

The information in this document is subject to change without notice.

Document No. IC-3549 (Japan)

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



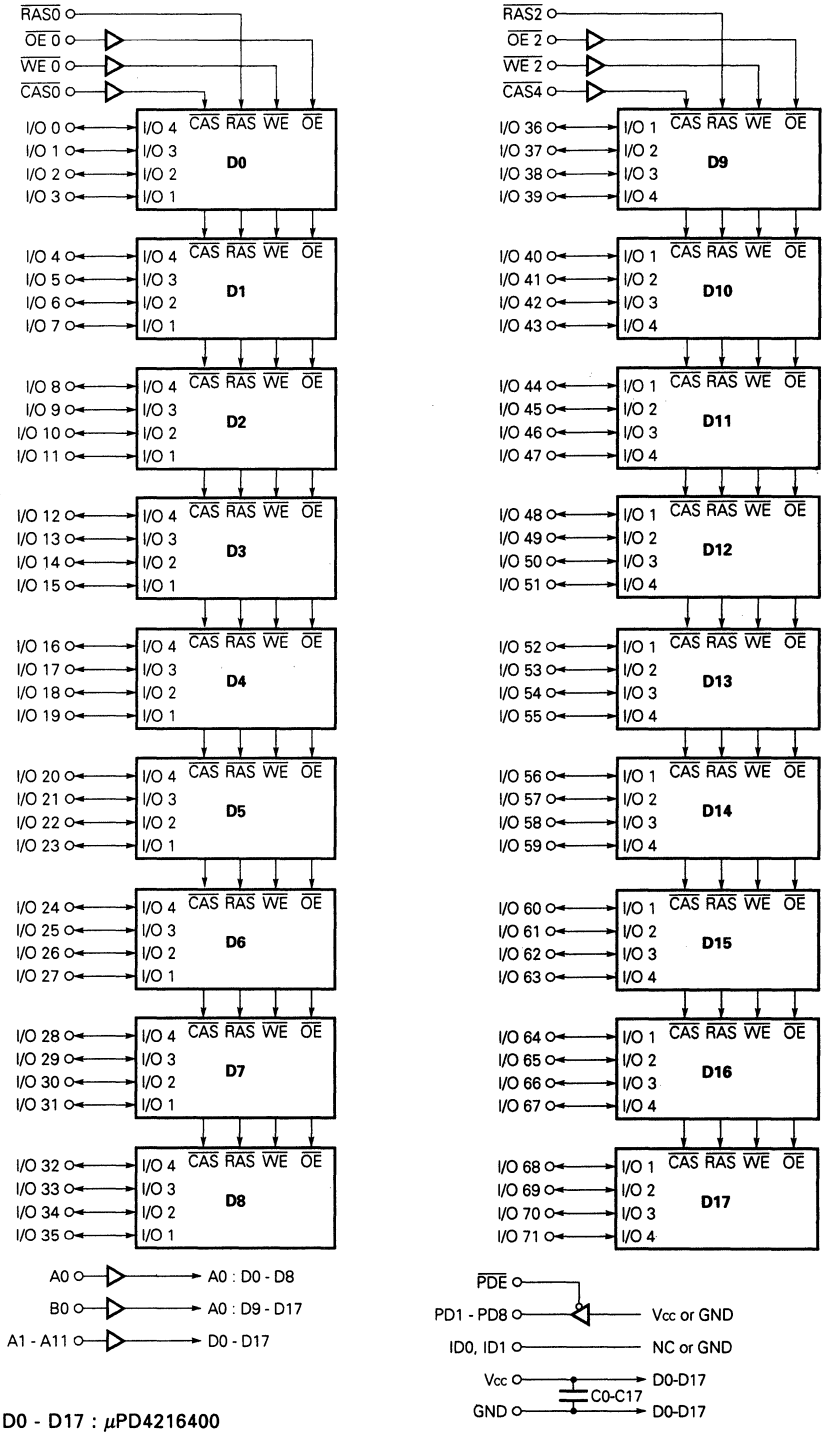
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	H	H	H
PD2	163	H	H	H
PD3	80	L	L	L
PD4	164	H	H	H
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	L	L	L
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A11, B0 : Address Inputs
I/O 0 - I/O 71 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D17 : μPD4216400

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		20	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A11, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			78	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS4}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O71			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,684	mA	3, 4, 7
			t_{RAC} = 70 ns		1,504		
			t_{RAC} = 80 ns		1,324		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		100	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA		82		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,684	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		1,504		
			t_{RAC} = 80 ns		1,324		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,324	mA	3, 4, 6
			t_{RAC} = 70 ns		1,144		
			t_{RAC} = 80 ns		964		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,684	mA	3, 4
			t_{RAC} = 70 ns		1,504		
			t_{RAC} = 80 ns		1,324		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V	$\overline{RAS}$	−10	+10	μA	
			Others	−5	+1		
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage	V_{OH}	I_O = −5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

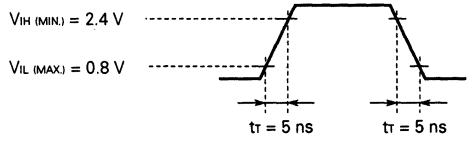
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Read Modify Write Cycle Time	t_{RWC}	175		195		220		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	85		90		105		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		20		23		25	ns	10, 11
Access Time Column Address	t_{AA}		35		40		45	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		40		45		50	ns	11
Access Time from $\overline{OE}$	t_{OEA}		20		23		25	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	12
$\overline{OE}$ to Data Delay Time	t_{OED}	15		15		20		ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns	12
$\overline{OE}$ Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40		45		50		ns	
Row Address Setup Time	t_{ASR}	5		5		5		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
$\overline{WE}$ Pulse Width	t_{WP}	10		10		15		ns	15

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	40		43		50		ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	95		105		120		ns	17
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	58		65		70		ns	17
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	60		65		75		ns	17
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	25		25		25		ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15		15		15		ns	
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		64		64		64	ms	

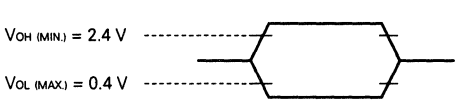
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

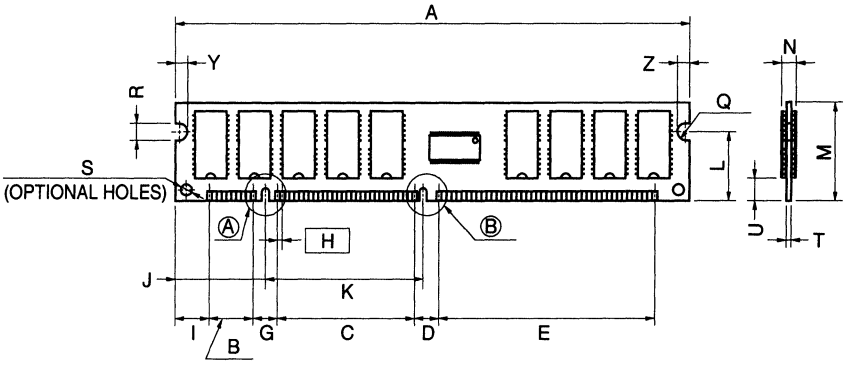
$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

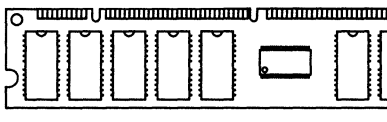
11. Loading conditions are 2 TTLs and 100 pF.
12. $t_{OFF\ (MAX.)}$ and $t_{OEZ\ (MAX.)}$ define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP\ (MIN.)}$ requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
15. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

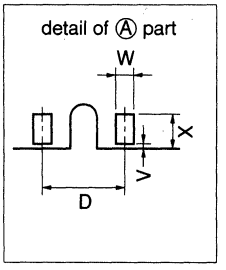
Timing Chart
Please refer to Timing Chart 3, page 397.

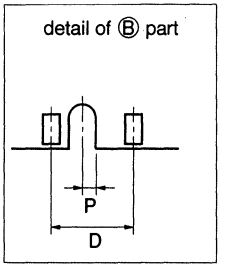
Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)









ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	42.18	1.661
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A2

NEC

MOS INTEGRATED CIRCUIT
MC-424000LAB72F

3.3 V OPERATION 4 M-WORD BY 72-BIT DYNAMIC RAM MODULE FAST PAGE MODE (ECC)

Description

The MC-424000LAB72F is a 4,194,304 words by 72 bits dynamic RAM module on which 18 pieces of 16 M DRAM: μPD4217400L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 4,194,304 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-424000LAB72-A60	60 ns	110 ns	6.52 W	180 mW (CMOS level input)
MC-424000LAB72-A70	70 ns	130 ns	5.87 W	
MC-424000LAB72-A80	80 ns	150 ns	5.22 W	

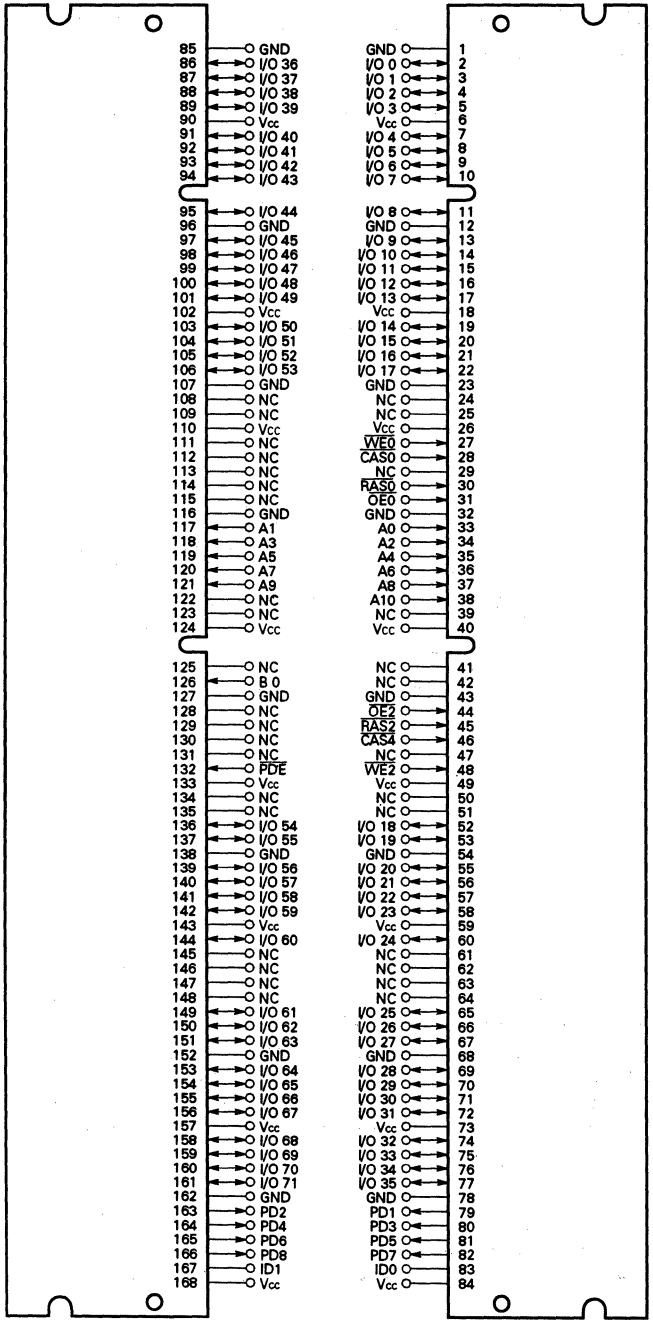
- 2,048 refresh cycles/32 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-424000LAB72F-A60	60 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	18 pieces of μPD4217400LG3 (300 mil TSOP(II)) [Double side]
MC-424000LAB72F-A70	70 ns		
MC-424000LAB72F-A80	80 ns		

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



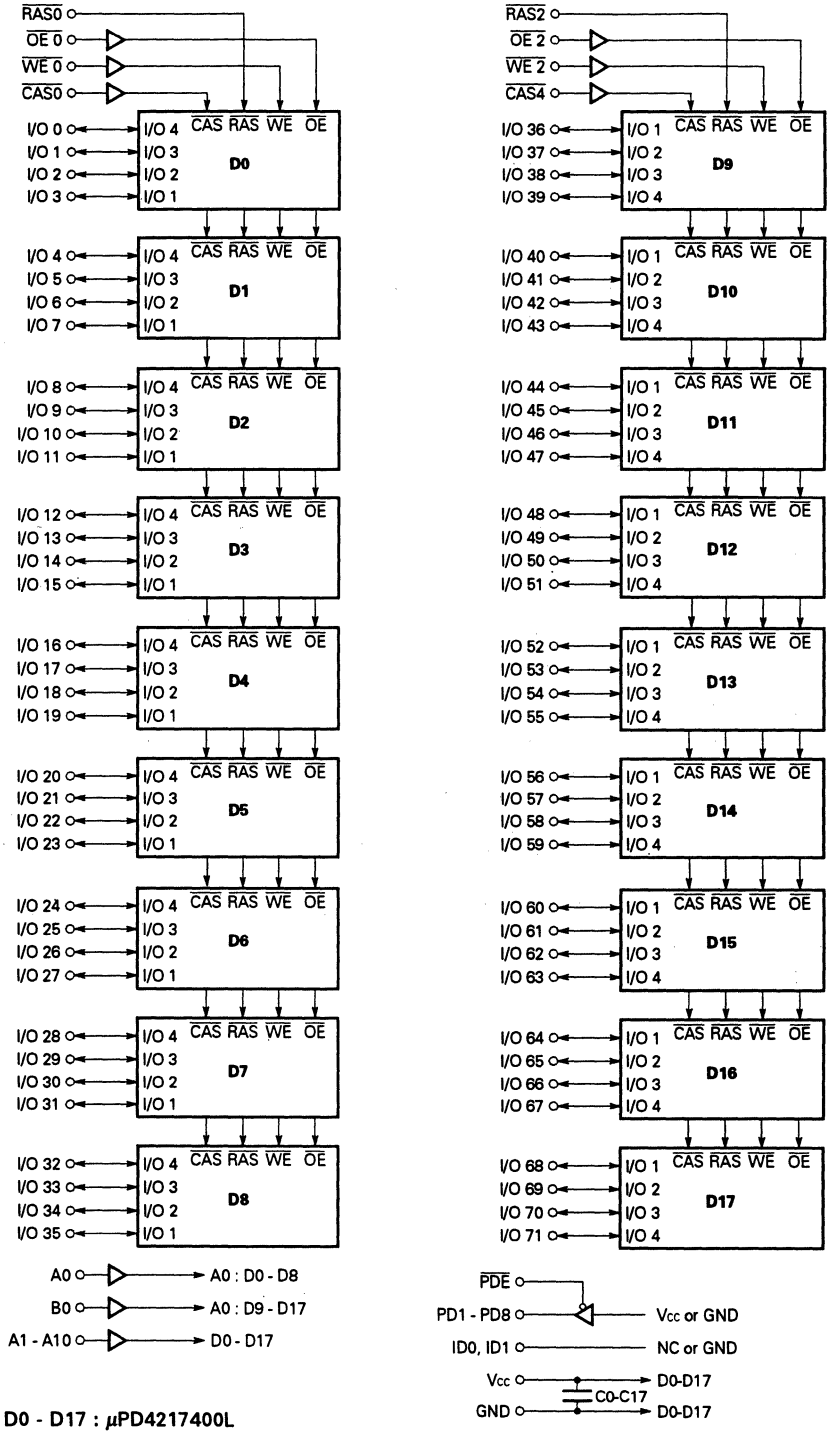
PD and ID Table

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	79	H	H	H
PD2	163	H	H	H
PD3	80	L	L	L
PD4	164	H	H	H
PD5	81	L	L	L
PD6	165	H	L	H
PD7	82	H	H	L
PD8	166	L	L	L
ID0	83	GND	GND	GND
ID1	167	GND	GND	GND

Remark H : V_{OH}, L : V_{OL}

A0 - A10, B0 : Address Inputs
I/O 0 - I/O 71 : Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$: Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$: Write Enable
$\overline{OE0}$, $\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1 - PD8 : Presence Detect Pins
ID0, ID1 : Identity Pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Remark D0 - D17 : μPD4217400L

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		–0.5 to +4.6	V
Supply voltage	V_{CC}		–0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		20	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		–0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			78	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS4}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O71			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition			MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns			1,810	mA	3, 4, 7
			t_{RAC} = 70 ns			1,630		
			t_{RAC} = 80 ns			1,450		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA			100	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA			50		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns			1,810	mA	3, 4, 5, 7
			t_{RAC} = 70 ns			1,630		
			t_{RAC} = 80 ns			1,450		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns			1,270	mA	3, 4, 6
			t_{RAC} = 70 ns			1,090		
			t_{RAC} = 80 ns			910		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns			1,810	mA	3, 4
			t_{RAC} = 70 ns			1,630		
			t_{RAC} = 80 ns			1,450		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		$\overline{RAS}$	–5	+5	μA	
				Others	–5	+1		
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)			–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA			2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA				0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

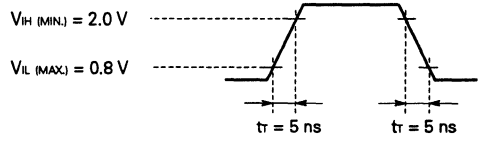
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Read Modify Write Cycle Time	t_{RWC}	175		195		220		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	85		90		105		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		20		23		25	ns	10, 11
Access Time Column Address	t_{AA}		35		40		45	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		40		45		50	ns	11
Access Time from $\overline{OE}$	t_{OEA}		15		18		20	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	12
$\overline{OE}$ to Data Delay Time	t_{OED}	15		15		20		ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns	12
$\overline{OE}$ Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40		45		50		ns	
Row Address Setup Time	t_{ASR}	5		5		5		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
$\overline{WE}$ Pulse Width	t_{WP}	10		10		15		ns	15

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	40		43		50		ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	95		105		120		ns	17
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	58		65		70		ns	17
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	60		65		75		ns	17
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	25		25		25		ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15		15		15		ns	
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		32		32		32	ms	

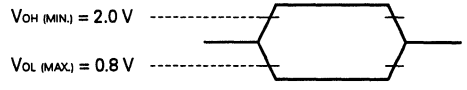
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

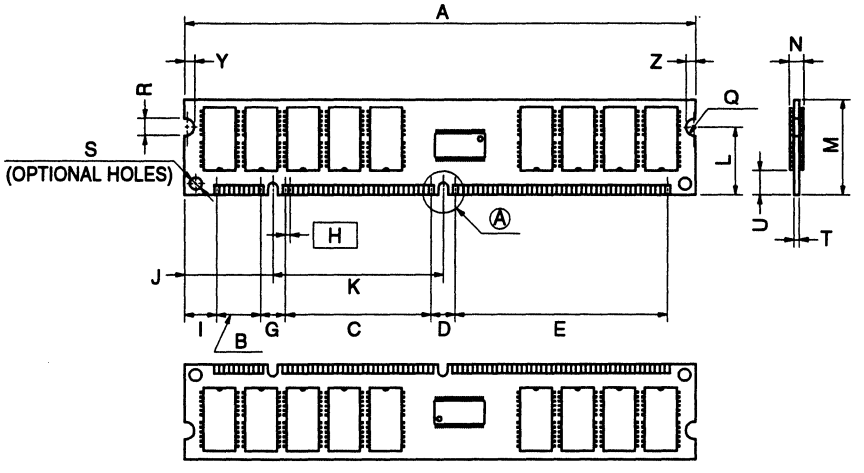
$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

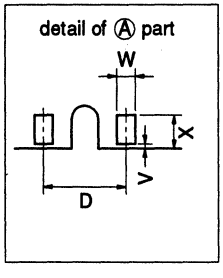
11. Loading conditions are 1 TTL and 100 pF.
12. $t_{OFF\ (MAX.)}$ and $t_{OEZ\ (MAX.)}$ define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP\ (MIN.)}$ requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
15. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Timing Chart
Please refer to Timing Chart 3, page 397.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.25±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	43.18	1.700
L	17.78	0.700
M	25.4	1.000
N	4.0 MAX.	0.158 MAX.
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	φ3.0	φ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A3

MC-428000LAF72

3.3 V OPERATION 8M -WORD BY 72-BIT DYNAMIC RAM MODULE FAST PAGE MODE (ECC)

Description

The MC-428000LAF72 is a 8 388 608 words by 72 bits dynamic RAM module on which 9 pieces of 64M DRAM (μPD 4264800) are assembled.

This module provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 8 388 608 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC- 428000LAF72-A50	50ns	90ns	3.55 w	295.2mw (CMOS level)
MC- 428000LAF72-A60	60ns	110ns	3.11 w	
MC- 428000LAF72-A70	70ns	130ns	2.14 w	

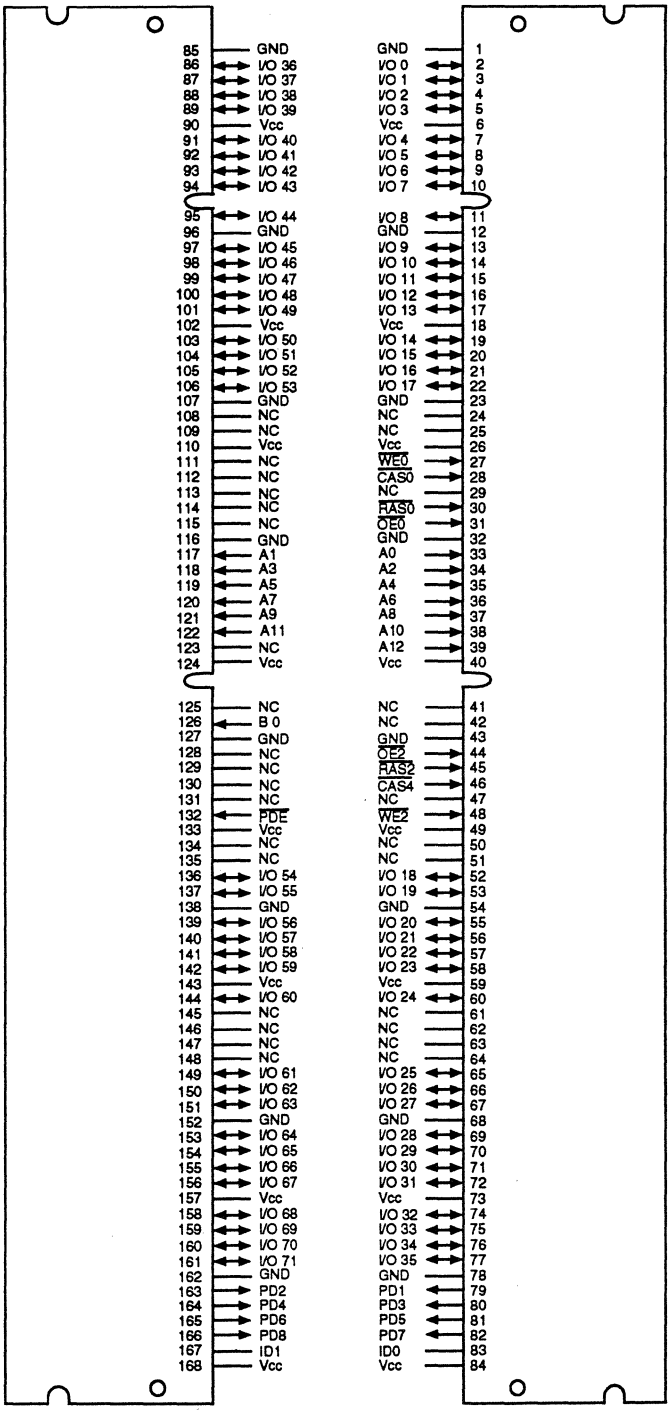
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh , $\overline{\text{RAS}}$ only refresh , Hidden refresh.
- 8 192 refresh cycles/64 ms ($\overline{\text{RAS}}$ only refresh)
  4 096 refresh cycles/64 ms ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, Hidden refresh)
- 168-pin dual in-line memory module (pin pitch = 1.27 mm)
- Single +3.3 V$\pm$0.3V power supply

Ordering information

Part Number	Access time (MAX.)	Package	Mounted devices
MC- 428000LAF72FA-A50	50ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	9 pieces of uPD 4264800LE (400mil SOJ) [Double side]
MC- 428000LAF72FA-A60	60ns		
MC- 428000LAF72FA-A70	70ns		

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge Connector : Gold plating)



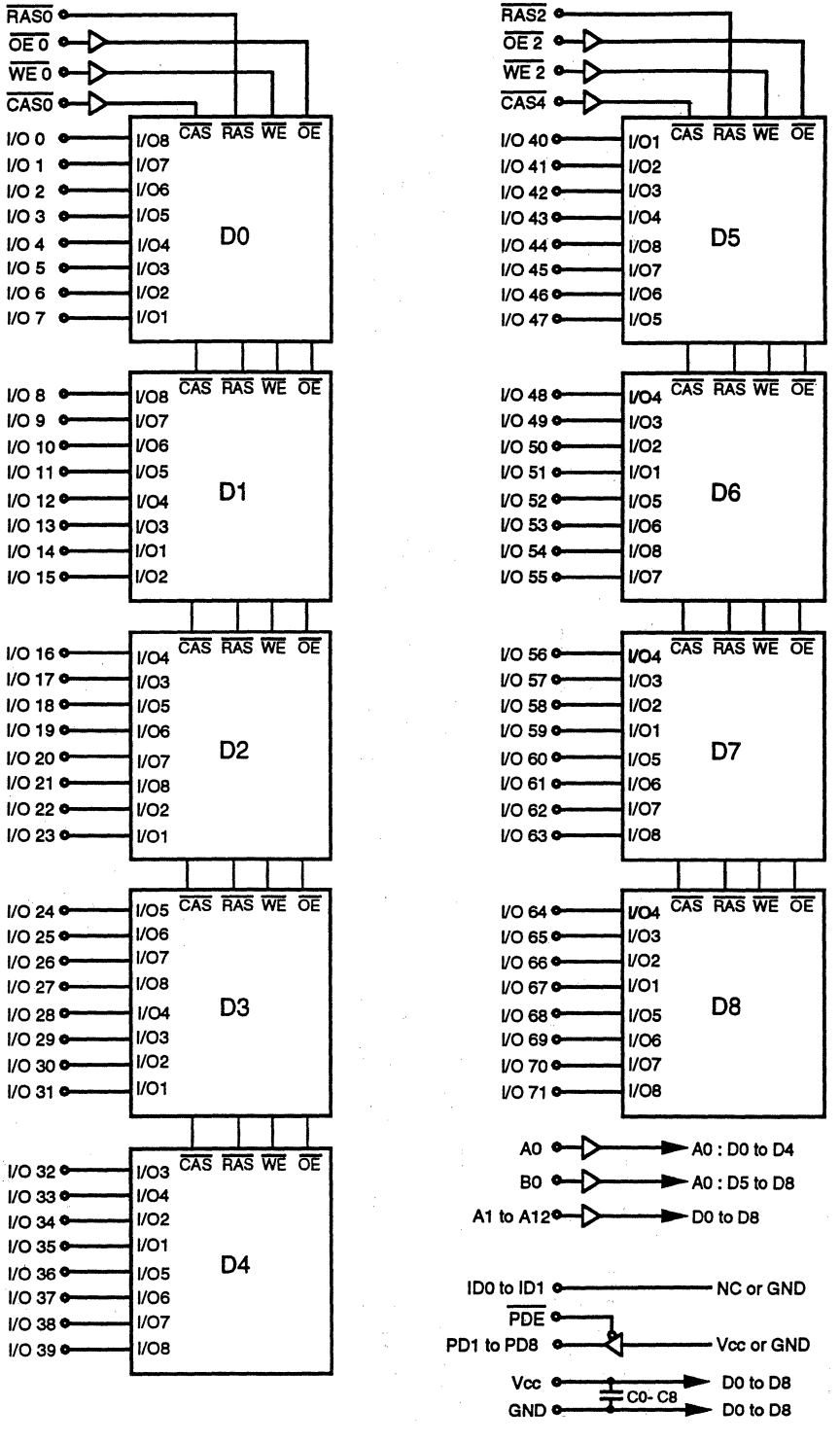
PD and ID Table

Pin Name	Pin No.	Accsess Time		
		50ns	60ns	70ns
PD1	79	H	H	H
PD2	163	L	L	L
PD3	80	H	H	H
PD4	164	H	H	H
PD5	81	L	L	L
PD6	165	L	H	L
PD7	82	L	H	H
PD8	166	L	L	L
I D0	83	GND	GND	GND
I D1	167	GND	GND	GND

Note) H : VOH, L : VOL

A0 - A12,B0 : Address Inputs
I/O 0-I/O 71 : Data Inputs / Outputs
$\overline{RAS0}$,$\overline{RAS2}$: Row Address Strobe
$\overline{CAS0}$,$\overline{CAS4}$: Column Address Strobe
$\overline{WE0}$,$\overline{WE2}$: Write Enable
$\overline{OE0}$,$\overline{OE2}$: Output Enable
$\overline{PDE}$: Presence Detect Enable
PD1- PD8 : Presence Detect Pins
ID0,ID1 : Identity pins
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	VT		-0.5 to +4.6	V
Supply voltage	VCC		-0.5 to +4.6	V
Output current	IO		20	mA
Power dissipation	PD		11	W
Operating temperature	Topt		0 to +70	℃
Storage temperature	Tstg		-55 to +125	℃

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device in not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (NOTES : 1, 2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	VCC		3.0	3.3	3.6	V
High level input voltage	VIH		2.0		Vcc + 0.3	V
Low level input voltage	VIL		-0.3		+0.8	V
Ambient temperature	Ta		0		70	℃

CAPACITANCE (Ta=25℃, f=1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	CI1	A0 - A12, B0			20	pF
	CI2	$\overline{WE0}$, $\overline{WE2}$			20	pF
	CI3	$\overline{RAS0}$, $\overline{RAS2}$			78	pF
	CI4	$\overline{CAS0}$, $\overline{CAS4}$			20	pF
	CI5	$\overline{OE0}$, $\overline{OE2}$			20	pF
Data Input/ Output capacitance	CI/O	I/O 0 - I/O 71			20	pF

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT	NOTES
Operating Current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC}=t_{RC(MIN.)}$, IO=0mA	t_{RAC}=50ns		985	mA	3,4,7
			t_{RAC}=60ns		865		
			t_{RAC}=70ns		775		
Standby Current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≧ $V_{IH(MIN.)}$			82	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≧ Vcc-0.2V			41		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS}$ ≧ V_{IH} $t_{RC}=t_{RC(MIN.)}$, IO=0mA	t_{RAC}=50ns		985	mA	3,4,5,7
			t_{RAC}=60ns		865		
			t_{RAC}=70ns		775		
Operating Current (Fast Page Mode)	I_{CC4}	$\overline{RAS}$ ≦ VIL, $\overline{CAS}$ Cycling tPC=tPC MIN., IO=0mA	t_{RAC}=50ns		775	mA	3,4,6
			t_{RAC}=60ns		685		
			t_{RAC}=70ns		550		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$t_{RC}=t_{RC(MIN.)}$ IO=0mA	t_{RAC}=50ns		985	mA	3,4
			t_{RAC}=60ns		865		
			t_{RAC}=70ns		775		
Input Leakage Current	$I_{I(L)}$	VI=0 to 3.6V all other pins not under test = 0V	$\overline{RAS}$	-5	+5	µA	
			others	-5	+1		
Output Leakage Current	$I_{O(L)}$	Outputs are disabled (Hi - Z) VO=0 to 3.6V		-5	+5	µA	
High level output voltage	V_{OH}	IO=-2.0mA		2.4		V	
Low level output voltage	V_{OL}	IO=+2.0mA			0.4	V	

AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Notes 8,9

(1/2)

PARAMETER	SYMBOL	t_{RAC} = 50ns		t_{RAC} = 60ns		t_{RAC} = 70ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	tRC	90	-	110	-	130	-	ns	
Read Modify Write Cycle Time	tRWC	138	-	163	-	185	-	ns	
Fast Page Mode Cycle Time (Read or Write)	tPC	35	-	40	-	45	-	ns	
Read Modify Write Cycle Time (Fast Page Mode)	tPRWC	73	-	83	-	90	-	ns	
Access Time from $\overline{RAS}$	tRAC	-	50	-	60	-	70	ns	10,11
Access Time from $\overline{CAS}$	tCAC	-	18	-	20	-	23	ns	10,11
Access Time from Column Address	tAA	-	30	-	35	-	40	ns	10,11
Access Time from $\overline{CAS}$ Precharge	tACP	-	35	-	40	-	45	ns	11
Access Time from $\overline{OE}$	tOEA	-	18	-	20	-	23	ns	11
$\overline{RAS}$ to Column Address Delay Time	tRAD	13	25	15	30	15	35	ns	10
$\overline{CAS}$ to Data Setup Time	tCLZ	0	-	0	-	0	-	ns	11
$\overline{OE}$ to Data Setup Time	tOLZ	0	-	0	-	0	-	ns	11
Output Buffer Turn-off Delay Time($\overline{CAS}$)	tOFF	0	10	0	13	0	15	ns	12
$\overline{OE}$ to Data Delay Time	tOED	15	-	13	-	15	-	ns	
Output Buffer Turn-off Delay Time($\overline{OE}$)	tOEZ	0	10	0	13	0	15	ns	12
$\overline{OE}$ Command Hold Time	tOEH	0	-	0	-	0	-	ns	
$\overline{OE}$ to $\overline{RAS}$ inactive Setup Time	tOES	0	-	0	-	0	-	ns	
Transition Time (Rise and Fall)	tT	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	tRP	30	-	40	-	50	-	ns	
$\overline{RAS}$ Pulse Width(Random Read, Write Cycle)	tRAS	50	10 000	60	10 000	70	10 000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	tRASP	50	125 000	60	125 000	70	125 000	ns	
$\overline{RAS}$ Hold Time	tRSH	13	-	15	-	18	-	ns	
$\overline{CAS}$ Pulse Width	tCAS	13	10 000	15	10 000	18	10 000	ns	
$\overline{CAS}$ Hold Time	tCSH	50	-	60	-	70	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	18	32	20	45	20	50	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	5	-	5	-	5	-	ns	13
$\overline{CAS}$ Precharge Time	tCPN	8	-	10	-	10	-	ns	
$\overline{CAS}$ Precharge Time(Fast Page Mode)	tCP	8	-	10	-	10	-	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	tRPC	5	-	5	-	5	-	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	tRHCP	35	-	40	-	45	-	ns	
Row Address Set Up Time	tASR	5	-	5	-	5	-	ns	
Row Address Hold Time	tRAH	8	-	10	-	10	-	ns	
Column Address Set Up Time	tASC	0	-	0	-	0	-	ns	
Column Address Hold Time	tCAH	13	-	15	-	15	-	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	tRAL	25	-	30	-	35	-	ns	
Lead Command Setup Time	tRCS	0	-	0	-	0	-	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	tRRH	0	-	0	-	0	-	ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	tRCH	0	-	0	-	0	-	ns	14
Write Command Hold Time Referenced to $\overline{CAS}$	tWCH	8	-	10	-	10	-	ns	15

(2/2)

PARAMETER	SYMBOL	tRAC = 50ns		tRAC = 60ns		tRAC = 70ns		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write Comand Set-Up Time	tWP	8	-	10	-	10	-	ms	15
Data-in Seup Time	tDS	0	-	0	-	0	-	ns	16
Data-in Hold Time	tDH	10	-	10	-	15	-	ns	16
Write Comand Setup Time	tWCS	0	-	0	-	0	-	ns	17
$\overline{CAS}$ to $\overline{WE}$ Delay Time	tCWD	33	-	38	-	43	-	ns	17
$\overline{RAS}$ to $\overline{WE}$ Delay Time	tRWD	80	-	93	-	105	-	ns	17
$\overline{CAS}$ Precharge Delay Time Referenced to $\overline{WE}$ (Fast Page Mode)	tCPWD	50	-	58	-	65	-	ns	17
Column Address Delay Time Referenced to $\overline{WE}$	tAWD	50	-	58	-	65	-	ns	17
Write Command Lead Time Referenced to $\overline{RAS}$	tRWL	18	-	20	-	20	-	ns	
Write Command Lead Time Referenced to $\overline{CAS}$	tCWL	18	-	20	-	20	-	ns	
$\overline{CAS}$ Setup Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	tCSR	5	-	5	-	5	-	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	tCHR	10	-	10	-	10	-	ns	
$\overline{WE}$ Setup Time	tWSR	10	-	10	-	10	-	ns	
$\overline{WE}$ Hold Time	tWHR	15	-	15	-	15	-	ns	
Refresh Time	tREF	-	64	-	64	-	64	ms	

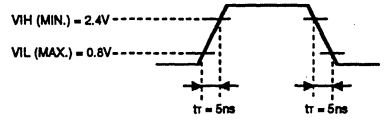
Timing Chart

Please refer to Timing Chart 3, page 397.

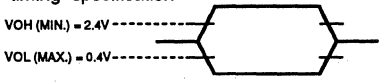
Notes:

1. All voltages are referenced to GND.
2. After power up, wait more than 100 µs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leqq V_{IL(MAX.)}$ and $\overline{CAS} \geqq V_{IH(MIN.)}$.
8. AC measurements assume t_T =5ns.
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification



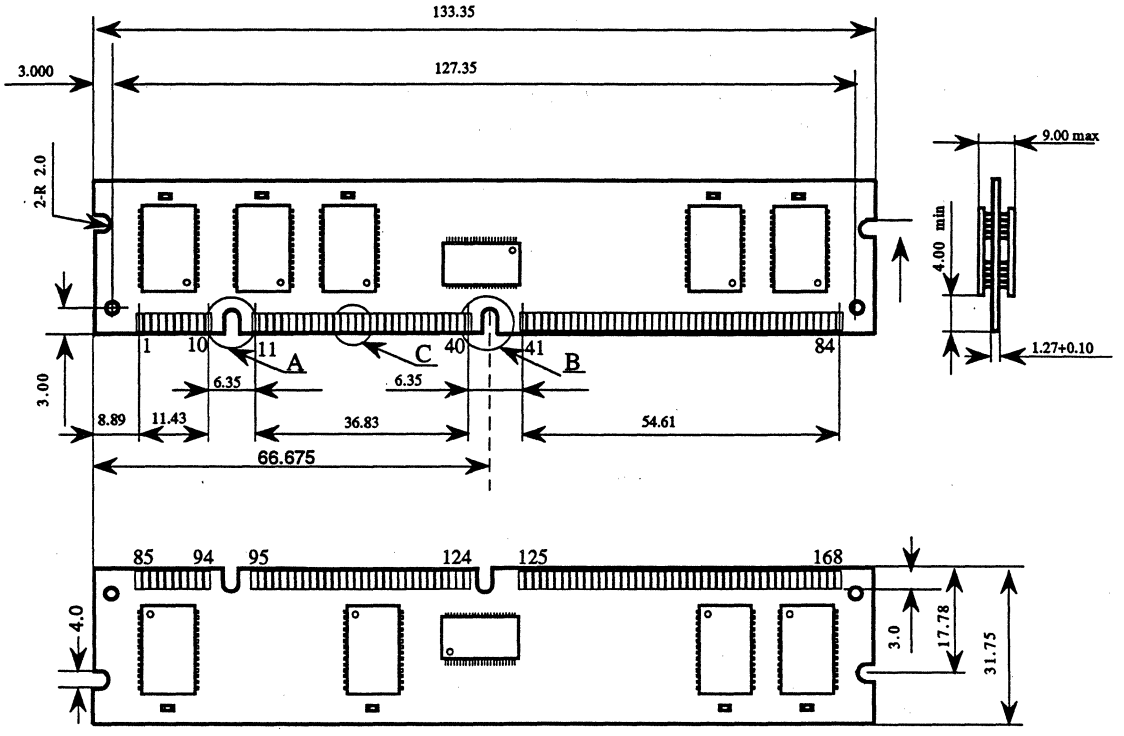
10. For read cycles, access time is defined as follows:

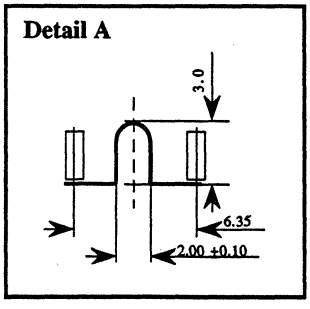
Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

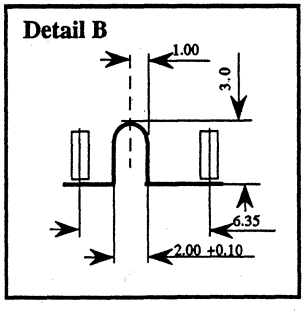
    $t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.
11. Loading conditions are 1 TTLs and 100 pF.
12. $t_{OFF(MAX.)}$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP(MIN.)}$ requirement should be applied to $\overline{RAS}$ / $\overline{CAS}$ cycles.
14. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.
15. $t_{WP(MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH(MIN.)}$ should be met.
16. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify cycles, they are referenced to the $\overline{WE}$ falling edge.
17. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geqq t_{RWD(MIN.)}$, $t_{CWD} \geqq t_{CWD(MIN.)}$, $t_{AWD} \geqq t_{AWD(MIN.)}$ and $t_{CPWD} \geqq t_{CPWD(MIN.)}$, the cycle is read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

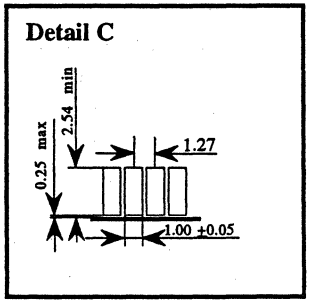
Package Drawing

UNIT: mm









4 Byte Small Outline DIMM

NEC

MOS INTEGRATED CIRCUIT

MC-42S1000LAD32S SERIES

1 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM) FAST PAGE MODE

Description

The MC-42S1000LAD32S series is a 1,048,576 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 2 pieces of 16 M DRAM: μPD42S18160L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- $\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 1,048,576 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-42S1000LAD32S-A60	60 ns	110 ns	1,080 mW	1.08 mW (CMOS level input)
MC-42S1000LAD32S-A70	70 ns	130 ns	1,008 mW	
MC-42S1000LAD32S-A80	80 ns	150 ns	936 mW	

- 1,024 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

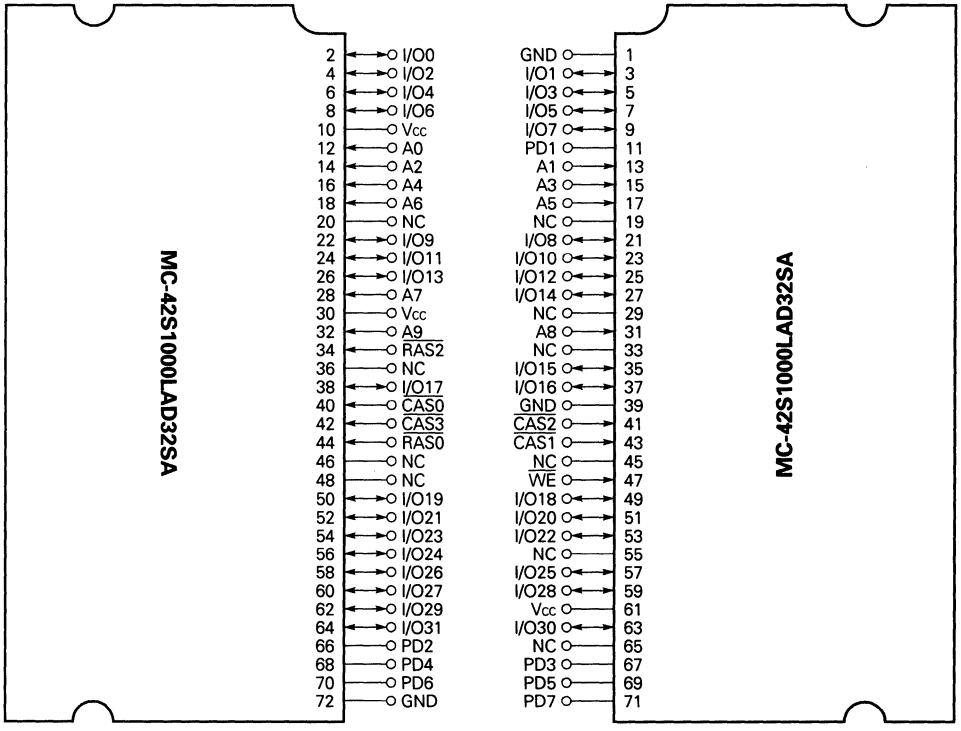
Document No. IC-3449 (Japan)

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-42S1000LAD32SA-A60	60 ns	72-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	2 pieces of μPD42S18160LG5 (400 mil TSOP (II)) [Single side]
MC-42S1000LAD32SA-A70	70 ns		
MC-42S1000LAD32SA-A80	80 ns		

Pin Configuration

72-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



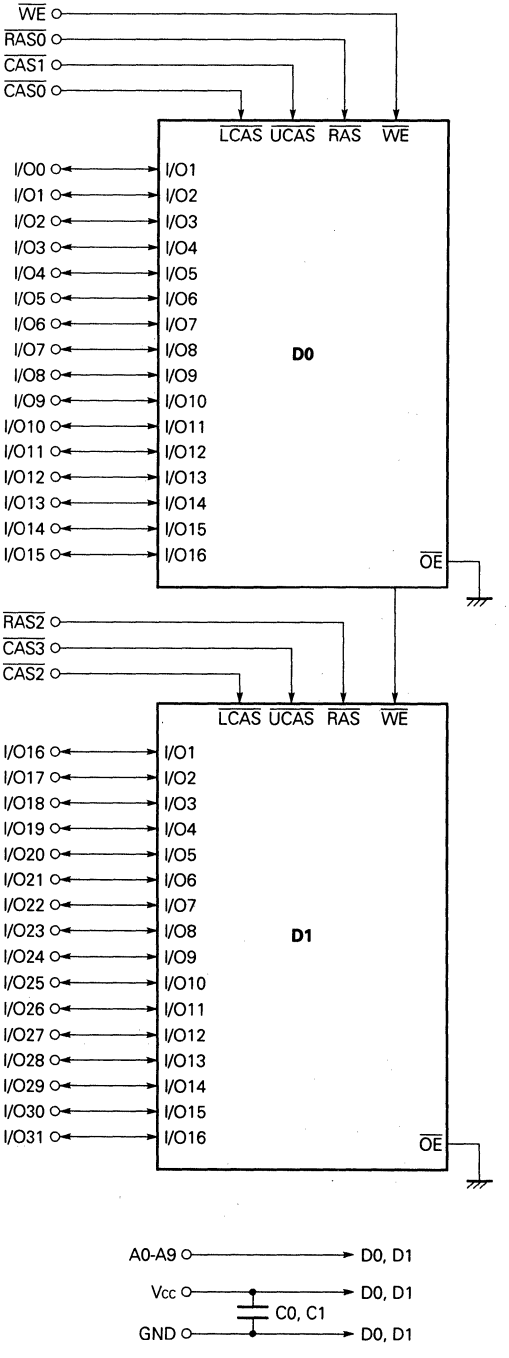
A0 - A9	:	Address Inputs
I/O0 - I/O31	:	Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$	:	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	:	Column Address Strobe
$\overline{WE}$	:	Write Enable
PD1 - PD7	:	Presence Detect Pins
Vcc	:	Power Supply
GND	:	Ground
NC	:	No connection

The internal connection of PD pins (PD1 to PD7).

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	11	NC	NC	NC
PD2	66	GND	GND	GND
PD3	67	GND	GND	GND
PD4	68	NC	NC	NC
PD5	69	NC	GND	NC
PD6	70	NC	NC	GND
PD7	71	GND	GND	GND

Block Diagram

Remark D0, D1 : μPD42S18160L (TSOP (II))



Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		–0.5 to +4.6	V
Supply voltage	V_{CC}		–0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		2	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		–0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			29	pF
	C_{I2}	$\overline{WE}$			29	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			23	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			17	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			12	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		300	mA	3, 4, 7
			t_{RAC} = 70 ns		280		
			t_{RAC} = 80 ns		260		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		1.0	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		0.3		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		300	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		280		
			t_{RAC} = 80 ns		260		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		180	mA	3, 4, 6
			t_{RAC} = 70 ns		160		
			t_{RAC} = 80 ns		140		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		300	mA	3, 4
			t_{RAC} = 70 ns		280		
			t_{RAC} = 80 ns		260		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current	I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: t_{RC} = 125.0 μs $\overline{RAS}$, $\overline{CAS}$: V_{CC} –0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V Standby: $\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ –0.2 V Address : V_{IH} or V_{IL} $\overline{WE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leq 1$ μs		360	μA	3, 4
$\overline{CAS}$ before $\overline{RAS}$ self refresh current	I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms V_{CC} –0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V I_O = 0 mA			300	μA	4
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

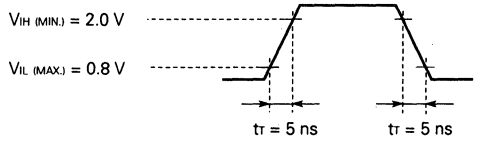
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RASS}	100		100		100		μs	
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RPS}	110		130		150		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{CHS}	−50		−50		−50		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		128		128		128	ms	

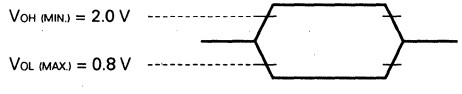
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification



10. For read cycles, access time is defined as follows:

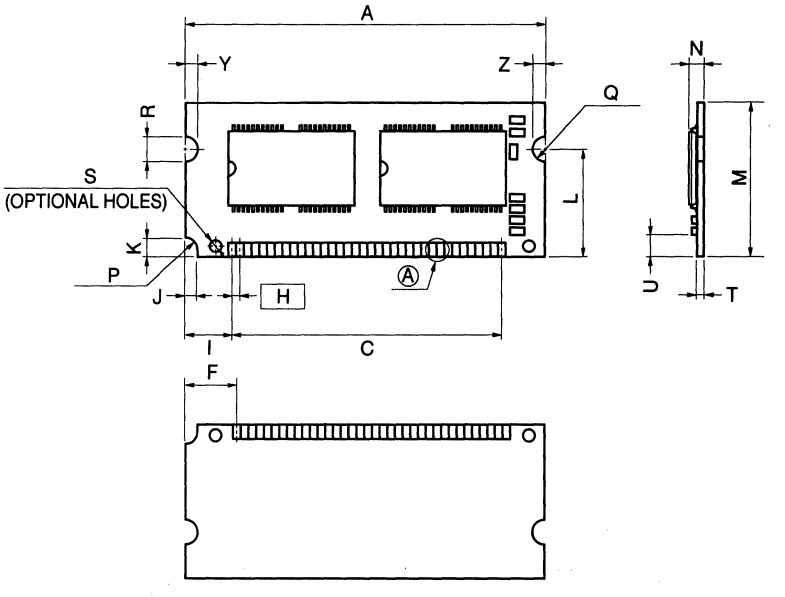
Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{RAC} (MAX.)	t_{RAC} (MAX.)
$t_{RAD} > t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{AA} (MAX.)	$t_{RAD} + t_{AA}$ (MAX.)
$t_{RCD} > t_{RCD}$ (MAX.)	t_{CAC} (MAX.)	$t_{RCD} + t_{CAC}$ (MAX.)

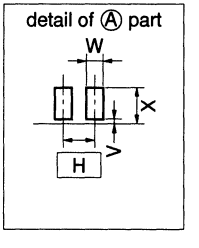
    t_{RAD} (MAX.) and t_{RCD} (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}$ (MAX.) and $t_{RCD} \geq t_{RCD}$ (MAX.) will not cause any operation problems.
11. Loading conditions are 1 TTL and 100 pF.
12. t_{OFF} (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. t_{CRP} (MIN.) requirements should be applied to $\overline{RAS}$/$\overline{CAS}$ cycles.
14. Either t_{RCH} (MIN.) or t_{RRH} (MIN.) should be met in read cycles.
15. In early write cycles, t_{WCH} (MIN.) should be met.
16. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

Timing Chart
Please refer to Timing Chart 5, page 425.

Package Drawing

72 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	59.69±0.13	2.35±0.006
C	44.45	1.750
F	8.255	0.325
H	1.27 (T.P.)	0.050 (T.P.)
I	7.62	0.300
J	2.0	0.079
K	3.18	0.125
L	17.78	0.700
M	25.4	1.000
N	2.45 MAX.	0.097 MAX.
P	R2.0	R0.079
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ1.8	ϕ0.071
T	1.0±0.1	$0.039^{+0.005}_{-0.004}$
U	3.18 MIN.	0.125 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54 MIN.	0.100 MIN.
Y	2.0 MIN.	0.078 MIN.
Z	2.0 MIN.	0.078 MIN.

M72S-50A4

NEC

MOS INTEGRATED CIRCUIT

MC-42S2000LAB32S SERIES

2 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM) FAST PAGE MODE

Description

The MC-42S2000LAB32S series is a 2,097,152 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 4 pieces of 16 M DRAM: μPD42S17800L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- $\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 2,097,152 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-42S2000LAB32S-A60	60 ns	110 ns	1,440 mW	2.16 mW (CMOS level input)
MC-42S2000LAB32S-A70	70 ns	130 ns	1,296 mW	
MC-42S2000LAB32S-A80	80 ns	150 ns	1,152 mW	

- 2,048 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

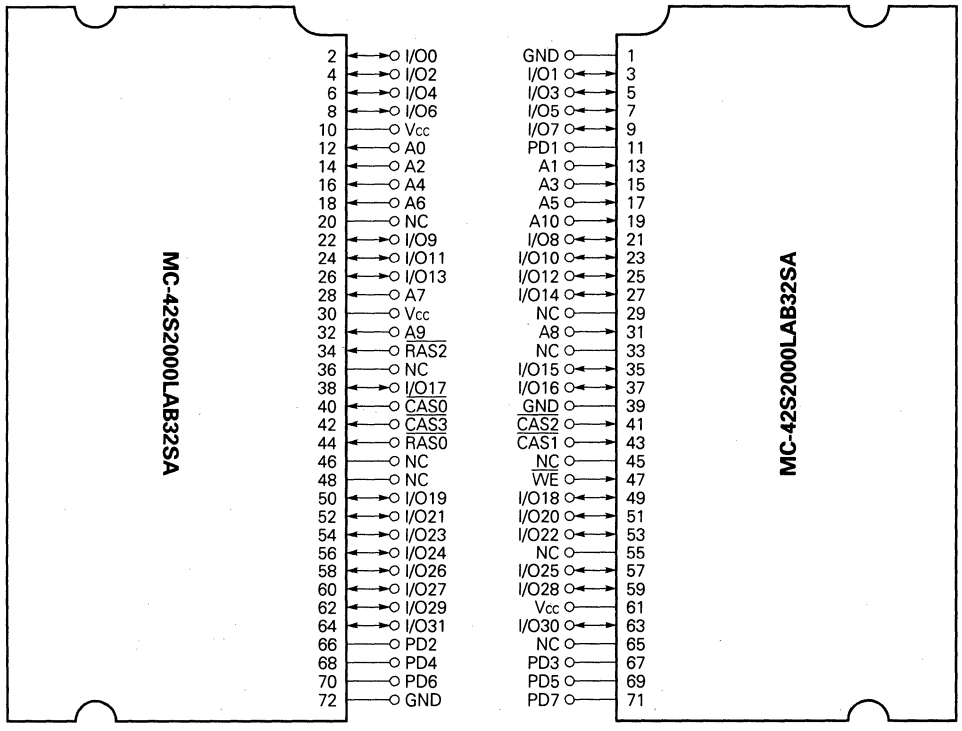
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-42S2000LAB32SA-A60	60 ns	72-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	4 pieces of μPD42S17800LG5 (400 mil TSOP (II)) [Single side]
MC-42S2000LAB32SA-A70	70 ns		
MC-42S2000LAB32SA-A80	80 ns		

Document No. M10054EJ3V0DSU1

Pin Configuration

72-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)

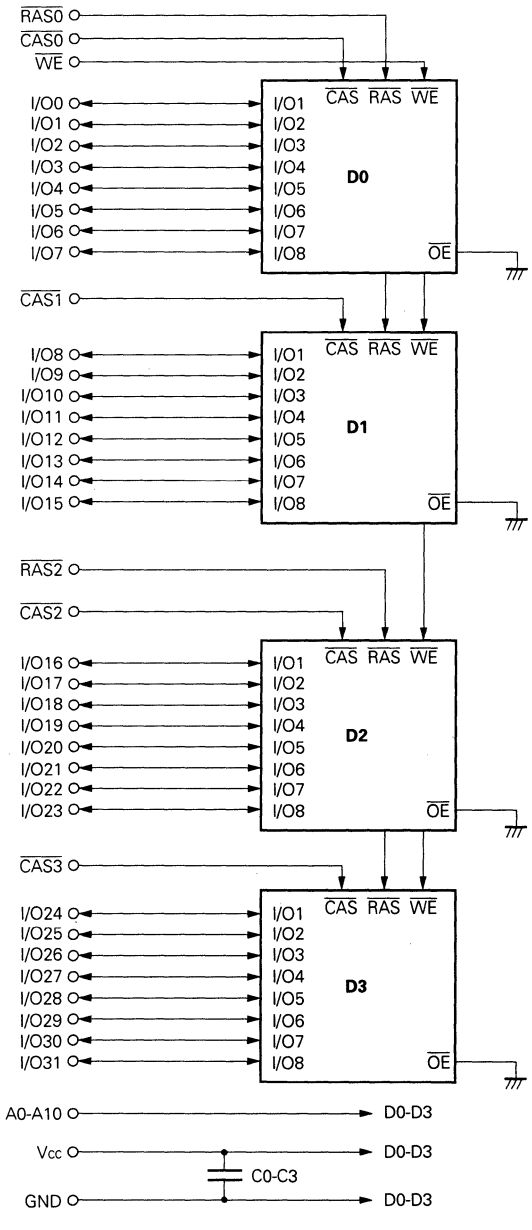


A0 - A10	:	Address Inputs
I/O0 - I/O31	:	Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$	:	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	:	Column Address Strobe
$\overline{WE}$	:	Write Enable
PD1 - PD7	:	Presence Detect Pins
Vcc	:	Power Supply
GND	:	Ground
NC	:	No connection

The internal connection of PD pins (PD1 to PD7).

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	11	GND	GND	GND
PD2	66	NC	NC	NC
PD3	67	GND	GND	GND
PD4	68	NC	NC	NC
PD5	69	NC	GND	NC
PD6	70	NC	NC	GND
PD7	71	GND	GND	GND

Block Diagram



Remark D0-D3 : μPD42S17800LG5 (TSOP (II))

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		4	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			35	pF
	C_{I2}	$\overline{WE}$			43	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			30	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			17	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			12	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		400	mA	3, 4, 7
			t_{RAC} = 70 ns		360		
			t_{RAC} = 80 ns		320		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		2.0	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA		0.6		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		400	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		360		
			t_{RAC} = 80 ns		320		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		280	mA	3, 4, 6
			t_{RAC} = 70 ns		240		
			t_{RAC} = 80 ns		200		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		400	mA	3, 4
			t_{RAC} = 70 ns		360		
			t_{RAC} = 80 ns		320		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current	I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: t_{RC} = 62.5 μs $\overline{RAS}$, $\overline{CAS}$: V_{CC} −0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V Standby: $\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ −0.2 V Address : V_{IH} or V_{IL} $\overline{WE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leq 1$ μs		800	μA	3, 4
$\overline{CAS}$ before $\overline{RAS}$ self refresh current	I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms V_{CC} −0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V I_O = 0 mA			600	μA	4
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		−5	+5	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		−5	+5	μA	
High level output voltage	V_{OH}	I_O = −2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

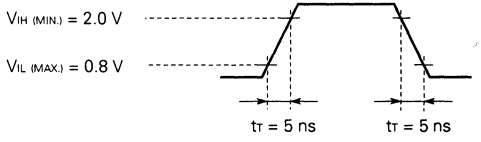
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		18		20	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RASS}	100		100		100		μs	
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RPS}	110		130		150		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{CHS}	−50		−50		−50		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		128		128		128	ms	

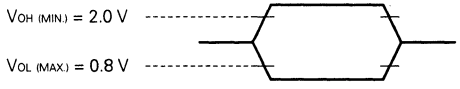
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification



10. For read cycles, access time is defined as follows:

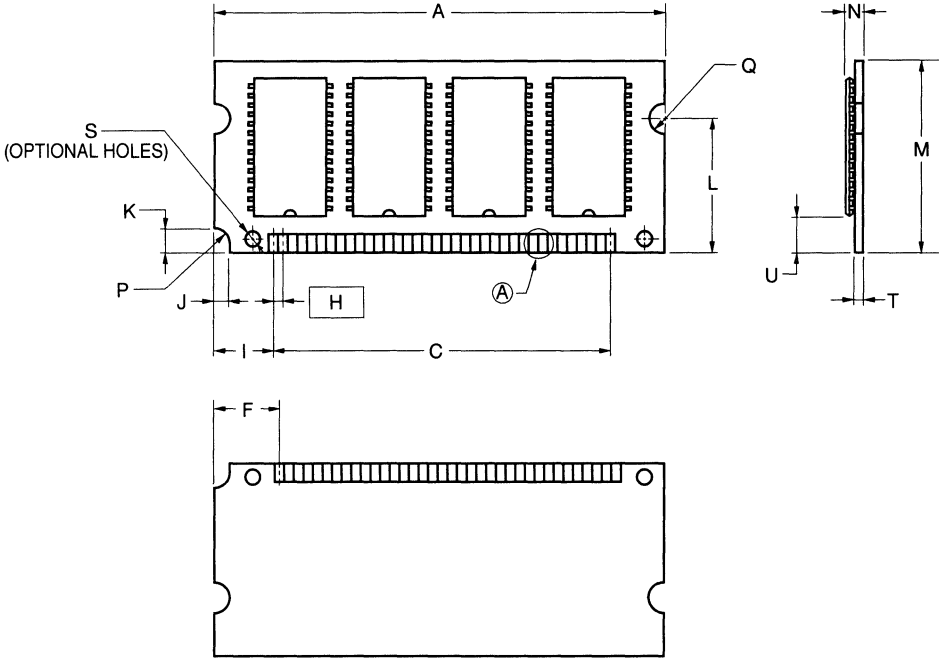
Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{RAC} (MAX.)	t_{RAC} (MAX.)
$t_{RAD} > t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{AA} (MAX.)	$t_{RAD} + t_{AA}$ (MAX.)
$t_{RCD} > t_{RCD}$ (MAX.)	t_{CAC} (MAX.)	$t_{RCD} + t_{CAC}$ (MAX.)

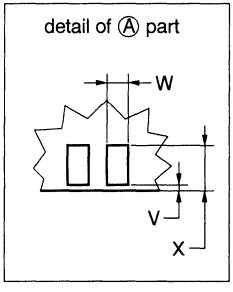
    t_{RAD} (MAX.) and t_{RCD} (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}$ (MAX.) and $t_{RCD} \geq t_{RCD}$ (MAX.) will not cause any operation problems.
11. Loading conditions are 1 TTL and 100 pF.
12. t_{OFF} (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. t_{CRP} (MIN.) requirements should be applied to $\overline{RAS}$/$\overline{CAS}$ cycles.
14. Either t_{RCH} (MIN.) or t_{RRH} (MIN.) should be met in read cycles.
15. In early write cycles, t_{WCH} (MIN.) should be met.
16. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

Timing Chart
Please refer to Timing Chart 6, page 435.

Package Drawing

72PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	59.69±0.13	2.35±0.006
C	44.45	1.750
F	8.255	0.325
H	1.27 (T.P.)	0.050 (T.P.)
I	7.62	0.300
J	2.03±0.13	$0.080^{+0.005}_{-0.006}$
K	3.175±0.13	0.125±0.006
L	17.78	0.700
M	25.4±0.13	1.000±0.006
N	2.463 MAX.	0.097 MAX.
P	R2.0	R0.079
Q	R2.0	R0.079
S	ϕ1.8	ϕ0.071
T	1.0±0.1	$0.039^{+0.005}_{-0.004}$
U	3.175 MIN.	0.125 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72S-50A1-2

NEC

MOS INTEGRATED CIRCUIT

MC-42S2000LAD32S SERIES

2 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM) FAST PAGE MODE

Description

The MC-42S2000LAD32S series is a 2,097,152 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 4 pieces of 16 M DRAM: μPD42S18160L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 2,097,152 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-42S2000LAD32S-A60	60 ns	110 ns	1,083.6 mW	2.16 mW (CMOS level input)
MC-42S2000LAD32S-A70	70 ns	130 ns	1,011.6 mW	
MC-42S2000LAD32S-A80	80 ns	150 ns	939.6 mW	

- 1,024 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

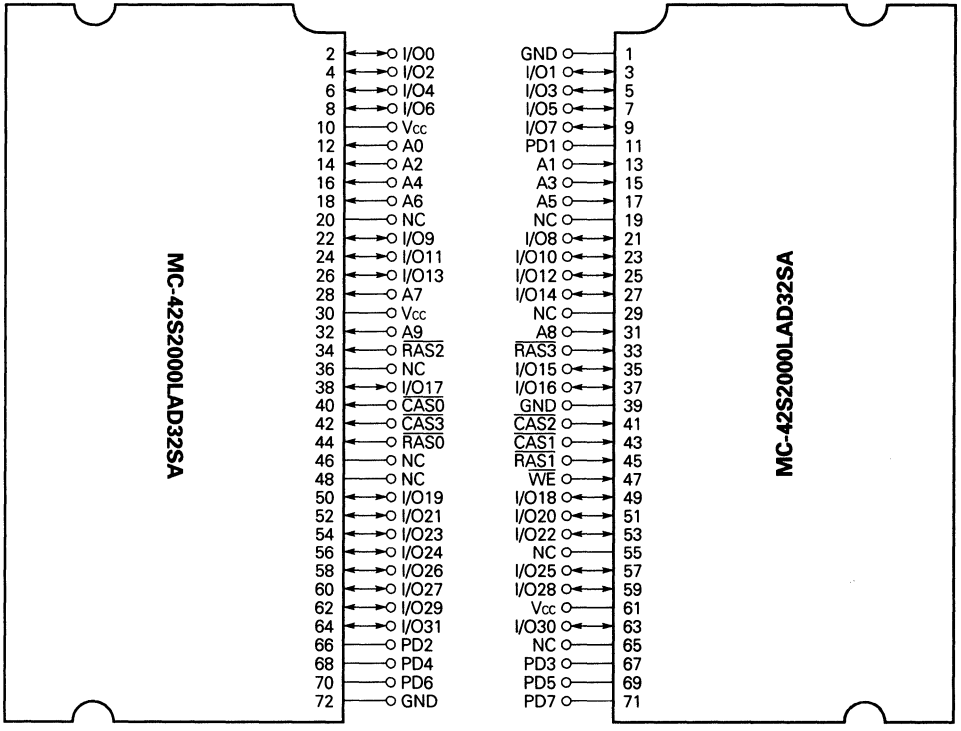
Document No. IC-3461 (Japan)

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-42S2000LAD32SA-A60	60 ns	72-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	4 pieces of μPD42S18160LG5 (400 mil TSOP (II)) [Double side]
MC-42S2000LAD32SA-A70	70 ns		
MC-42S2000LAD32SA-A80	80 ns		

Pin Configuration

72-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)

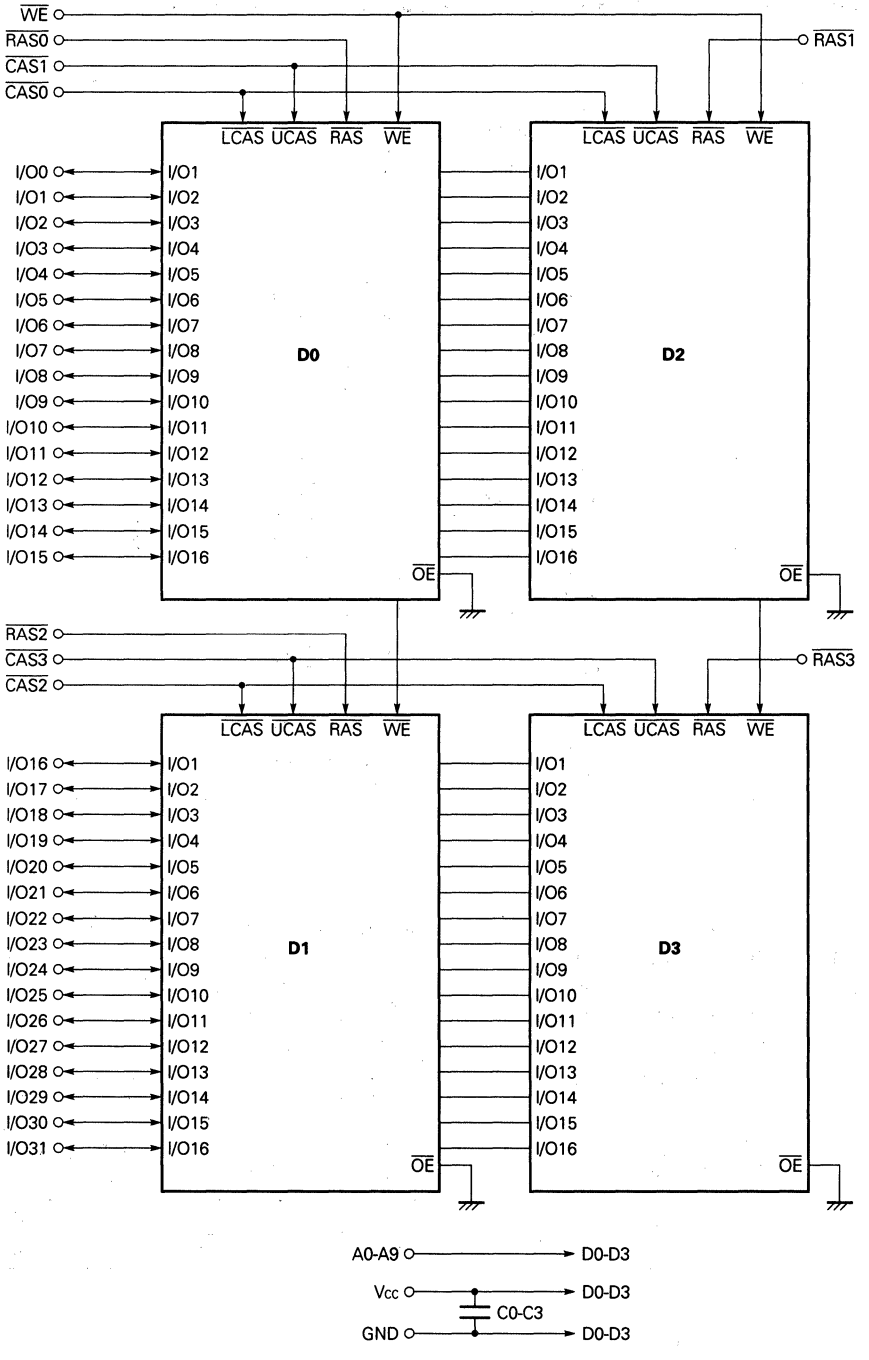


A0 - A9	: Address Inputs
I/O0 - I/O31	: Data Inputs/Outputs
$\overline{RAS0}$ - $\overline{RAS3}$	: Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	: Column Address Strobe
$\overline{WE}$	: Write Enable
PD1 - PD7	: Presence Detect Pins
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD1 – PD7).

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	11	NC	NC	NC
PD2	66	GND	GND	GND
PD3	67	GND	GND	GND
PD4	68	GND	GND	GND
PD5	69	NC	GND	NC
PD6	70	NC	NC	GND
PD7	71	GND	GND	GND

Block Diagram



Remark D0-D3 : μPD42S18160LG5 (TSOP (II))

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		8	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 – A9			35	pF
	C_{I2}	$\overline{WE}$			43	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS3}$			23	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			24	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			19	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC}$ (MIN.) I_O = 0 mA	t_{RAC} = 60 ns		301	mA	3, 4, 7
			t_{RAC} = 70 ns		281		
			t_{RAC} = 80 ns		261		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH}$ (MIN.)	I_O = 0 mA		2.0	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		0.6		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH}$ (MIN.) $t_{RC} = t_{RC}$ (MIN.) I_O = 0 mA	t_{RAC} = 60 ns		301	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		281		
			t_{RAC} = 80 ns		261		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL}$ (MAX.), $\overline{CAS}$ Cycling $t_{PC} = t_{PC}$ (MIN.) I_O = 0 mA	t_{RAC} = 60 ns		181	mA	3, 4, 6
			t_{RAC} = 70 ns		161		
			t_{RAC} = 80 ns		141		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC}$ (MIN.) I_O = 0 mA	t_{RAC} = 60 ns		301	mA	3, 4
			t_{RAC} = 70 ns		281		
			t_{RAC} = 80 ns		261		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current	I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: t_{RC} = 125.0 μs $\overline{RAS}$, $\overline{CAS}$: V_{CC} –0.2 V ≤ V_{IH} ≤ V_{IH} (MAX.) 0 V ≤ V_{IL} ≤ 0.2 V Standby: $\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ –0.2 V Address : V_{IH} or V_{IL} $\overline{WE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leq 1$ μs		720	μA	3, 4
$\overline{CAS}$ before $\overline{RAS}$ self refresh current	I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms V_{CC} –0.2 V ≤ V_{IH} ≤ V_{IH} (MAX.) 0 V ≤ V_{IL} ≤ 0.2 V I_O = 0 mA			600	μA	4
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

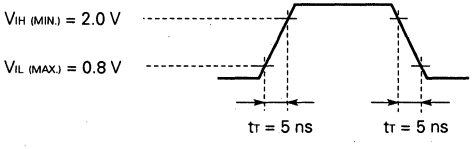
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RASS}	100		100		100		μs	
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RPS}	110		130		150		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{CHS}	–50		–50		–50		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		128		128		128	ms	

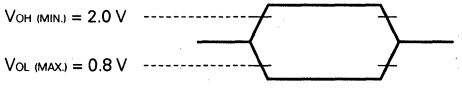
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification



10. For read cycles, access time is defined as follows:

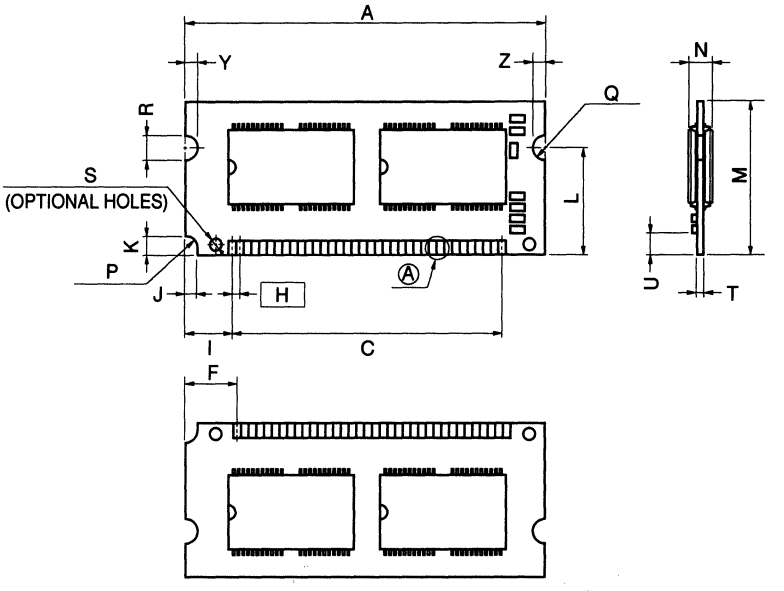
Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{RAC} (MAX.)	t_{RAC} (MAX.)
$t_{RAD} > t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{AA} (MAX.)	$t_{RAD} + t_{AA}$ (MAX.)
$t_{RCD} > t_{RCD}$ (MAX.)	t_{CAC} (MAX.)	$t_{RCD} + t_{CAC}$ (MAX.)

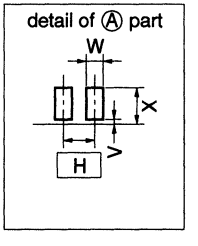
    t_{RAD} (MAX.) and t_{RCD} (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}$ (MAX.) and $t_{RCD} \geq t_{RCD}$ (MAX.) will not cause any operation problems.
11. Loading conditions are 1 TTL and 100 pF.
12. t_{OFF} (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. t_{CRP} (MIN.) requirements should be applied to $\overline{RAS}$/$\overline{CAS}$ cycles.
14. Either t_{RCH} (MIN.) or t_{RRH} (MIN.) should be met in read cycles.
15. In early write cycles, t_{WCH} (MIN.) should be met.
16. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

Timing Chart
Please refer to Timing Chart 5, page 425.

Package Drawing

72 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	59.69±0.13	2.35±0.006
C	44.45	1.750
F	8.255	0.325
H	1.27 (T.P.)	0.050 (T.P.)
I	7.62	0.300
J	2.0	0.079
K	3.18	0.125
L	17.78	0.700
M	25.4	1.000
N	3.8 MAX.	0.150 MAX.
P	R2.0	R0.079
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ1.8	ϕ0.071
T	1.0±0.1	$0.039^{+0.005}_{-0.004}$
U	3.18 MIN.	0.125 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54 MIN.	0.100 MIN.
Y	2.0 MIN.	0.078 MIN.
Z	2.0 MIN.	0.078 MIN.

M72S-50A3

NEC

MOS INTEGRATED CIRCUIT

MC-42S4000LAB32S SERIES

4 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM) FAST PAGE MODE

Description

The MC-42S4000LAB32S series is a 4,194,304 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 8 pieces of 16 M DRAM: μPD42S17800L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- $\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 4,194,304 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-42S4000LAB32S-A60	60 ns	110 ns	1,458 mW	4.32 mW (CMOS level input)
MC-42S4000LAB32S-A70	70 ns	130 ns	1,314 mW	
MC-42S4000LAB32S-A80	80 ns	150 ns	1,170 mW	

- 2,048 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

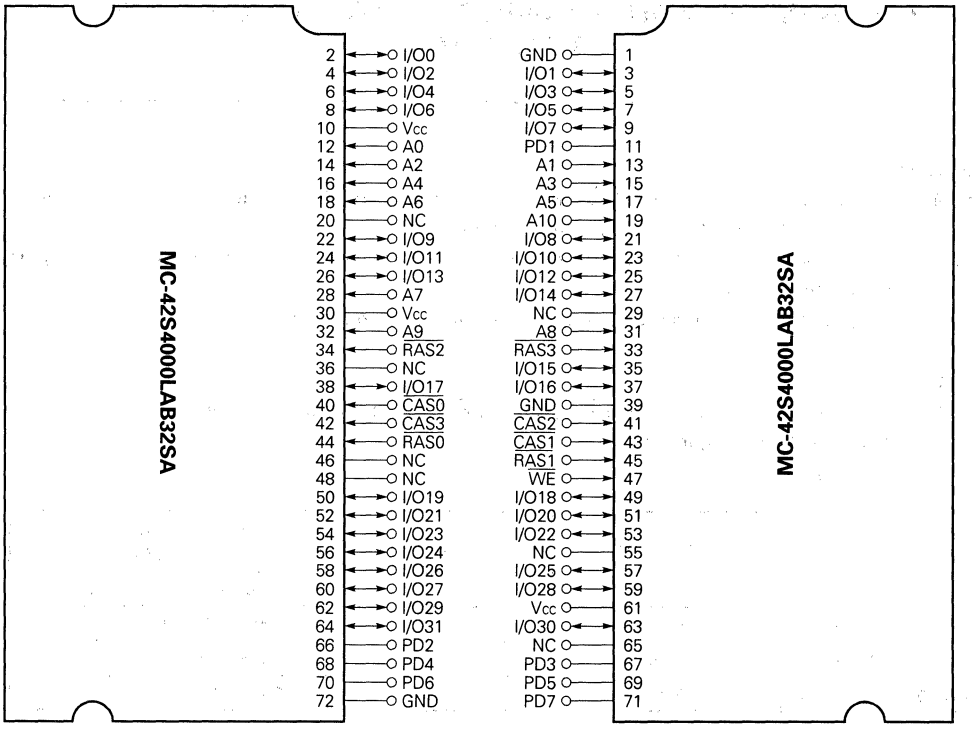
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-42S4000LAB32SA-A60	60 ns	72-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	8 pieces of μPD42S17800LG5 (400 mil TSOP (II)) [Double side]
MC-42S4000LAB32SA-A70	70 ns		
MC-42S4000LAB32SA-A80	80 ns		

Document No. M10055EJ3V0DSU1

Pin Configuration

72-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)

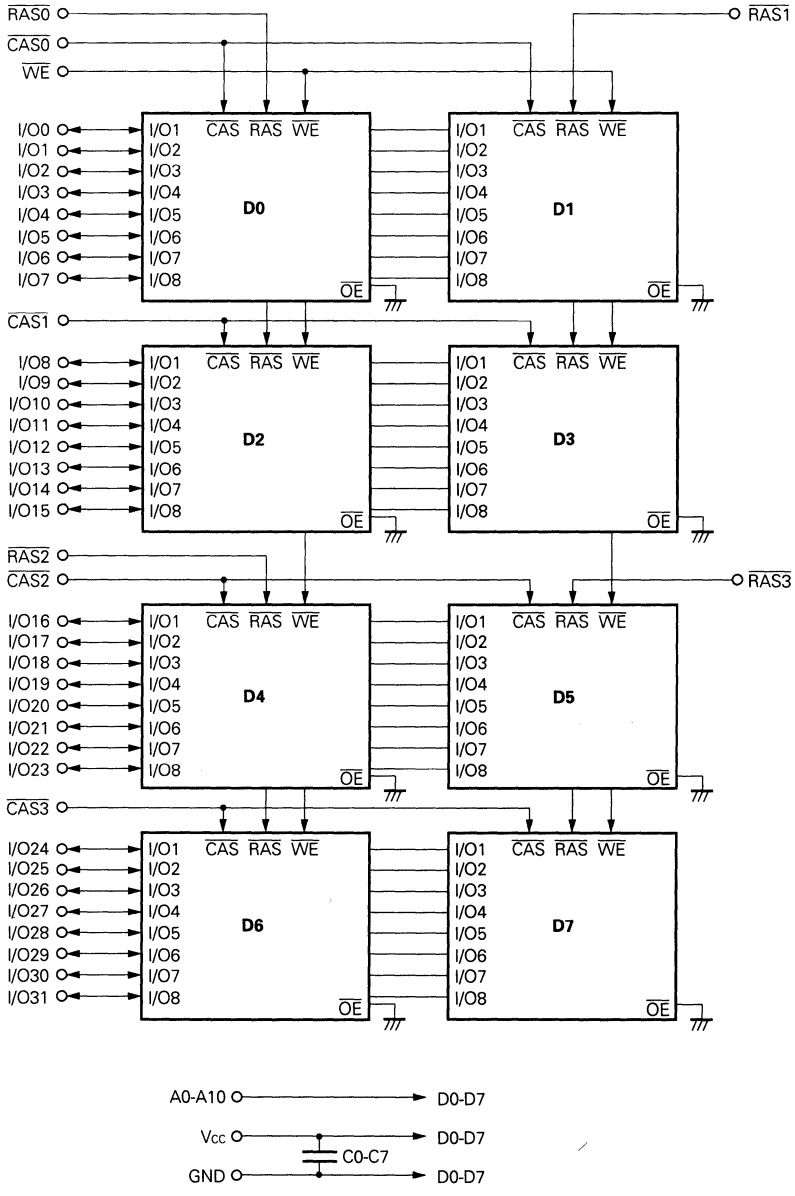


A0 - A10	: Address Inputs
I/O0 - I/O31	: Data Inputs/Outputs
$\overline{RAS0}$ - $\overline{RAS3}$	: Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	: Column Address Strobe
$\overline{WE}$	: Write Enable
PD1 - PD7	: Presence Detect Pins
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD1 to PD7).

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	11	GND	GND	GND
PD2	66	NC	NC	NC
PD3	67	GND	GND	GND
PD4	68	GND	GND	GND
PD5	69	NC	GND	NC
PD6	70	NC	NC	GND
PD7	71	GND	GND	GND

Block Diagram



Remark D0-D7 : μPD42S17800LG5 (TSOP (II))

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		8	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			55	pF
	C_{I2}	$\overline{WE}$			71	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS3}$			30	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			24	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			19	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		405	mA	3, 4, 7
			t_{RAC} = 70 ns		365		
			t_{RAC} = 80 ns		325		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		4.0	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA		1.2		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		405	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		365		
			t_{RAC} = 80 ns		325		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		285	mA	3, 4, 6
			t_{RAC} = 70 ns		245		
			t_{RAC} = 80 ns		205		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		405	mA	3, 4
			t_{RAC} = 70 ns		365		
			t_{RAC} = 80 ns		325		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current	I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: t_{RC} = 62.5 μs $\overline{RAS}$, $\overline{CAS}$: V_{CC} −0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V Standby: $\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ −0.2 V Address : V_{IH} or V_{IL} $\overline{WE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leq 1$ μs		1.6	mA	3, 4
$\overline{CAS}$ before $\overline{RAS}$ self refresh current	I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms V_{CC} −0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V I_O = 0 mA			1.2	mA	4
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		−5	+5	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		−5	+5	μA	
High level output voltage	V_{OH}	I_O = −2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

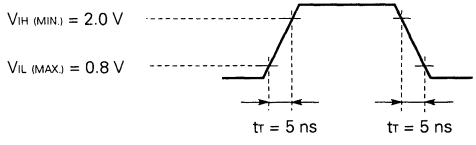
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		18		20	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RASS}	100		100		100		μs	
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RPS}	110		130		150		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{CHS}	−50		−50		−50		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		128		128		128	ms	

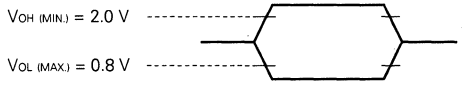
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification



10. For read cycles, access time is defined as follows:

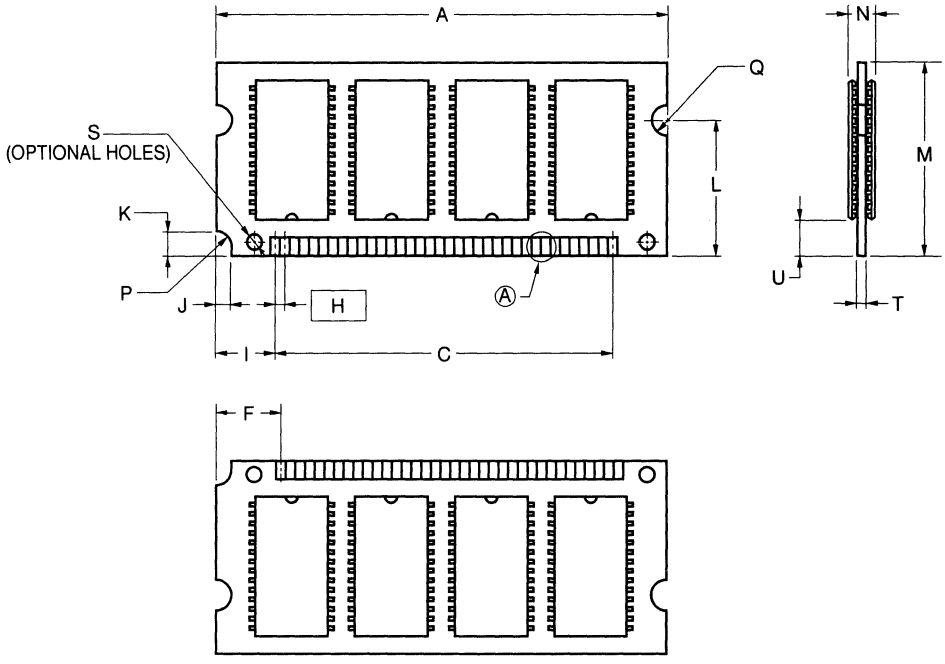
Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{RAC} (MAX.)	t_{RAC} (MAX.)
$t_{RAD} > t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{AA} (MAX.)	$t_{RAD} + t_{AA}$ (MAX.)
$t_{RCD} > t_{RCD}$ (MAX.)	t_{CAC} (MAX.)	$t_{RCD} + t_{CAC}$ (MAX.)

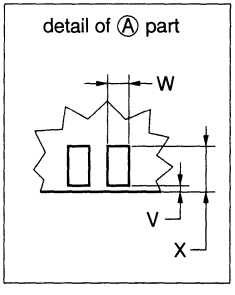
    t_{RAD} (MAX.) and t_{RCD} (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}$ (MAX.) and $t_{RCD} \geq t_{RCD}$ (MAX.) will not cause any operation problems.
11. Loading conditions are 1 TTL and 100 pF.
12. t_{OFF} (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. t_{CRP} (MIN.) requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either t_{RCH} (MIN.) or t_{RRH} (MIN.) should be met in read cycles.
15. In early write cycles, t_{WCH} (MIN.) should be met.
16. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

Timing Chart
Please refer to Timing Chart 6, page 435.

Package Drawing

72PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	59.69±0.13	2.35±0.006
C	44.45	1.750
F	8.255	0.325
H	1.27 (T.P.)	0.050 (T.P.)
I	7.62	0.300
J	2.03±0.13	$0.080^{+0.005}_{-0.006}$
K	3.175±0.13	0.125±0.006
L	17.78	0.700
M	25.4±0.13	1.000±0.006
N	3.81 MAX.	0.150 MAX.
P	R2.0	R0.079
Q	R2.0	R0.079
S	ϕ1.8	ϕ0.071
T	1.0±0.1	$0.039^{+0.005}_{-0.004}$
U	3.175 MIN.	0.125 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72S-50A2-2

NEC

MOS INTEGRATED CIRCUIT

MC-42S4000LAC32S SERIES

4 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM) FAST PAGE MODE

Description

The MC-42S4000LAC32S series is a 4,194,304 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 8 pieces of 16 M DRAM: μPD42S17400LG3 (TSOP (II)) are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 4,194,304 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-42S4000LAC32S-A60	60 ns	110 ns	2,880 mW	4.32 mW (CMOS level input)
MC-42S4000LAC32S-A70	70 ns	130 ns	2,592 mW	
MC-42S4000LAC32S-A80	80 ns	150 ns	2,304 mW	

- 2,048 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

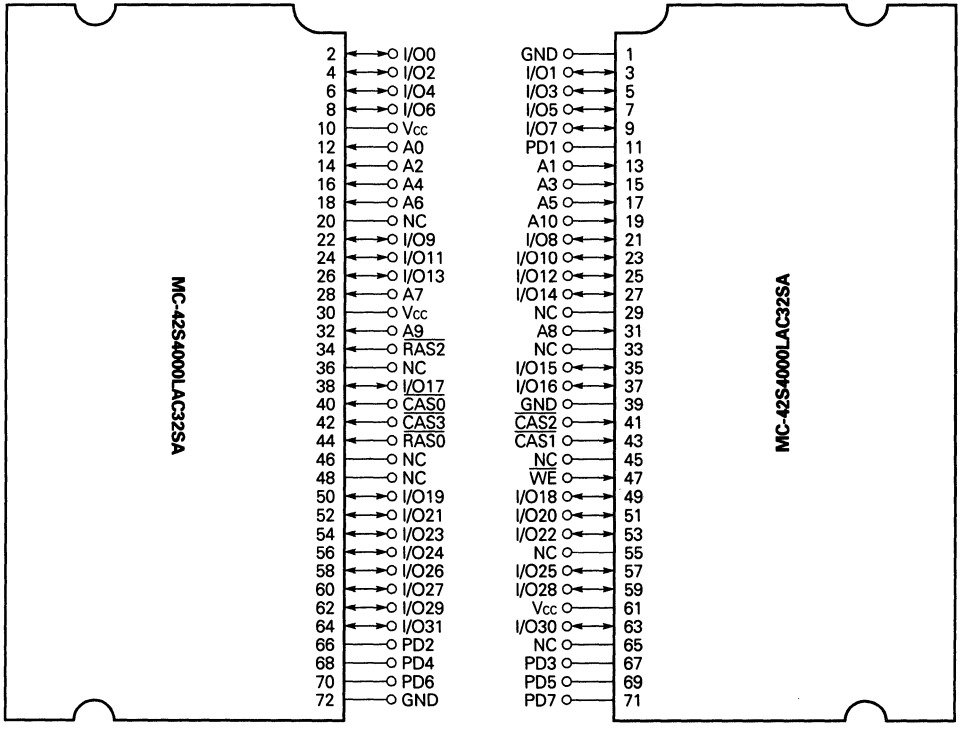
Document No. IC-3460 (Japan)

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-42S4000LAC32SA-A60	60 ns	72-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plating	8 pieces of μPD42S17400LG3 (300 mil TSOP (II)) [Double side]
MC-42S4000LAC32SA-A70	70 ns		
MC-42S4000LAC32SA-A80	80 ns		

Pin Configuration

72-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



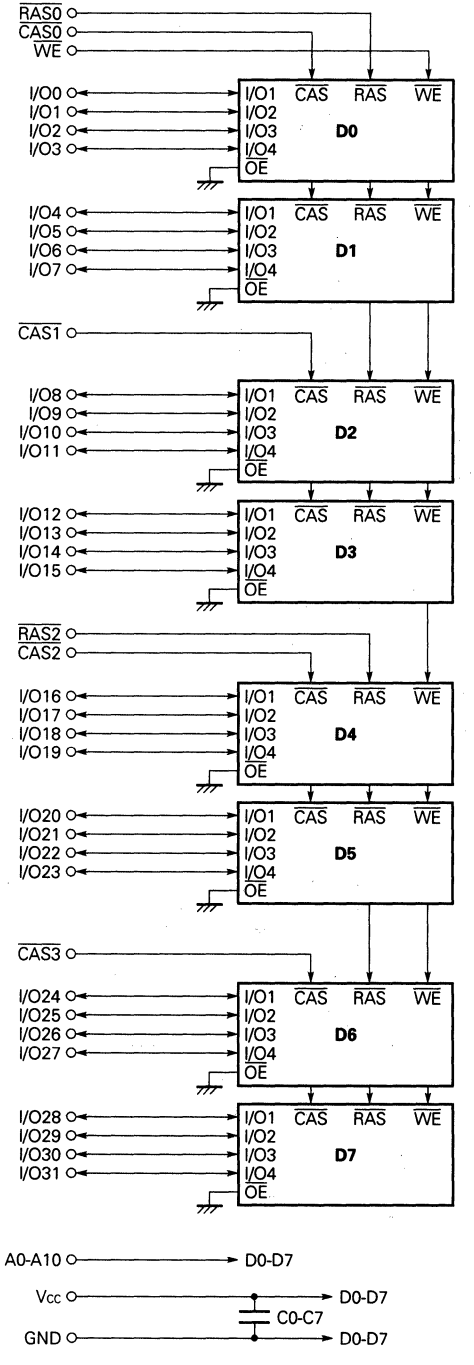
A0 - A10	:	Address Inputs
I/O0 - I/O31	:	Data Inputs/Outputs
$\overline{RAS0}$, $\overline{RAS2}$	:	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	:	Column Address Strobe
$\overline{WE}$	:	Write Enable
PD1 - PD7	:	Presence Detect Pins
Vcc	:	Power Supply
GND	:	Ground
NC	:	No connection

The internal connection of PD pins (PD1 to PD7).

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD1	11	NC	NC	NC
PD2	66	NC	NC	NC
PD3	67	GND	GND	GND
PD4	68	NC	NC	NC
PD5	69	NC	GND	NC
PD6	70	NC	NC	GND
PD7	71	GND	GND	GND

Block Diagram

Remark D0-07 : μPD42S17400LG3 (TSOP (II))



Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		–0.5 to +4.6	V
Supply voltage	V_{CC}		–0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		8	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		–0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			55	pF
	C_{I2}	$\overline{WE}$			71	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			36	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			19	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			10	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		800	mA	3, 4, 7
			t_{RAC} = 70 ns		720		
			t_{RAC} = 80 ns		640		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		4	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA		1.2		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		800	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		720		
			t_{RAC} = 80 ns		640		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		560	mA	3, 4, 6
			t_{RAC} = 70 ns		480		
			t_{RAC} = 80 ns		400		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		800	mA	3, 4
			t_{RAC} = 70 ns		720		
			t_{RAC} = 80 ns		640		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current	I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: t_{RC} = 62.5 μs $\overline{RAS}$, $\overline{CAS}$: $V_{CC} - 0.2\ V \leq V_{IH} \leq V_{IH\ (MAX.)}$ $0\ V \leq V_{IL} \leq 0.2\ V$ Standby: $\overline{RAS} \geq V_{CC} - 0.2$ V Address : V_{IH} or V_{IL} $\overline{WE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leq 1$ μs		1.6	mA	3, 4
$\overline{CAS}$ before $\overline{RAS}$ self refresh current	I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms $V_{CC} - 0.2\ V \leq V_{IH} \leq V_{IH\ (MAX.)}$ $0\ V \leq V_{IL} \leq 0.2\ V$ I_O = 0 mA			1.2	mA	4
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		−5	+5	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		−5	+5	μA	
High level output voltage	V_{OH}	I_O = −2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

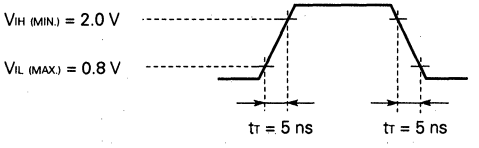
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		18		20	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RASS}	100		100		100		μs	
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RPS}	110		130		150		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{CHS}	–50		–50		–50		ns	
Refresh Time	t_{REF}		128		128		128	ms	

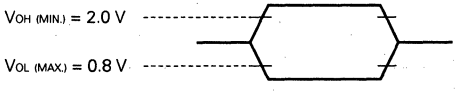
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification



10. For read cycles, access time is defined as follows:

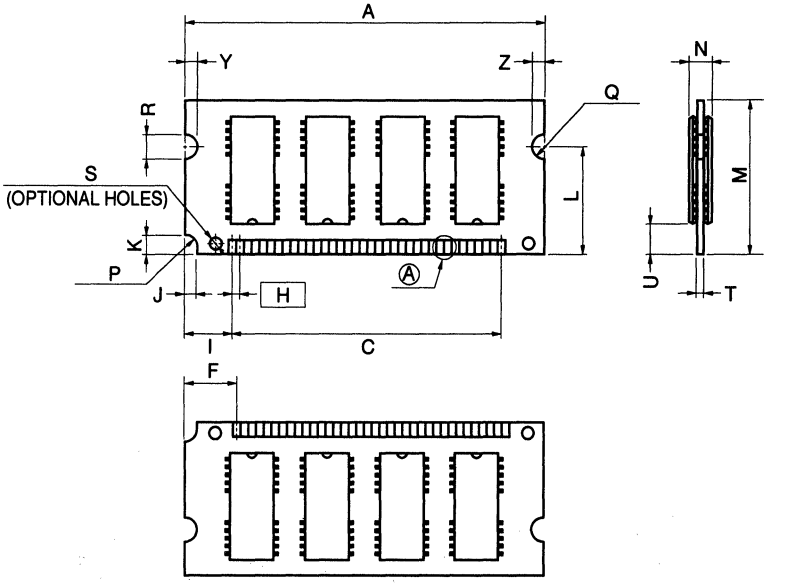
Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{RAC} (MAX.)	t_{RAC} (MAX.)
$t_{RAD} > t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{AA} (MAX.)	$t_{RAD} + t_{AA}$ (MAX.)
$t_{RCD} > t_{RCD}$ (MAX.)	t_{CAC} (MAX.)	$t_{RCD} + t_{CAC}$ (MAX.)

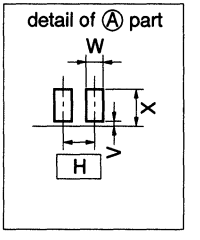
    t_{RAD} (MAX.) and t_{RCD} (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}$ (MAX.) and $t_{RCD} \geq t_{RCD}$ (MAX.) will not cause any operation problems.
11. Loading conditions are 1 TTL and 100 pF.
12. t_{OFF} (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. t_{CRP} (MIN.) requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either t_{RCH} (MIN.) or t_{RRH} (MIN.) should be met in read cycles.
15. In early write cycles, t_{WCH} (MIN.) should be met.
16. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

Timing Chart
Please refer to Timing Chart 6, page 435.

Package Drawing

72 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	59.69±0.13	2.35±0.006
C	44.45	1.750
F	8.255	0.325
H	1.27 (T.P.)	0.050 (T.P.)
I	7.62	0.300
J	2.0	0.079
K	3.18	0.125
L	17.78	0.700
M	25.4	1.000
N	3.8 MAX.	0.150 MAX.
P	R2.0	R0.079
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ1.8	ϕ0.071
T	1.0±0.1	$0.039^{+0.005}_{-0.004}$
U	3.18 MIN.	0.125 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54 MIN.	0.100 MIN.
Y	2.0 MIN.	0.078 MIN.
Z	2.0 MIN.	0.078 MIN.

M72S-50A5

4 Byte SIMM
[Hyper Page (EDO)]

NEC

MOS INTEGRATED CIRCUIT

MC-421000F32

1 M-WORD BY 32-BIT DYNAMIC RAM MODULE HYPER PAGE MODE (EDO)

Description

The MC-421000F32 is a 1,048,576 words by 32 bits dynamic RAM module on which 2 pieces of 16 M DRAM: μPD4218165 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 1,048,576 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC-421000F32-60	60 ns	104 ns	25 ns	1,760 mW	11 mW (CMOS level input)
MC-421000F32-70	70 ns	124 ns	30 ns	1,650 mW	

- 1,024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

Ordering Information

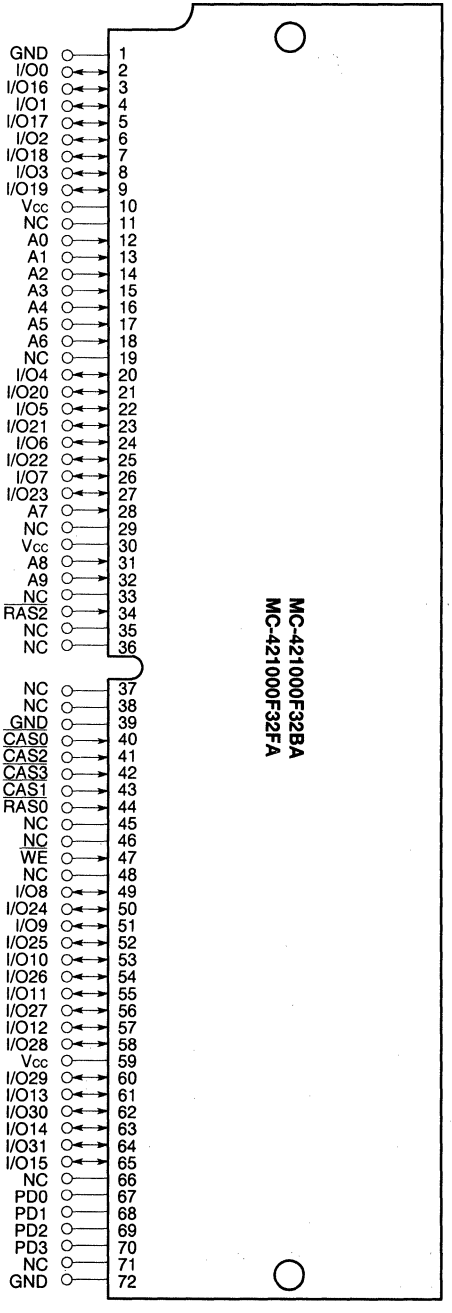
Part number	Access time (MAX.)	Package	Mounted devices
MC-421000F32BA-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	2 pieces of μPD4218165LE (400 mil SOJ) [Single side]
MC-421000F32BA-70	70 ns		
MC-421000F32FA-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-421000F32FA-70	70 ns		

The information in this document is subject to change without notice.

Document No. M10438EJ2V0DSU1

Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)

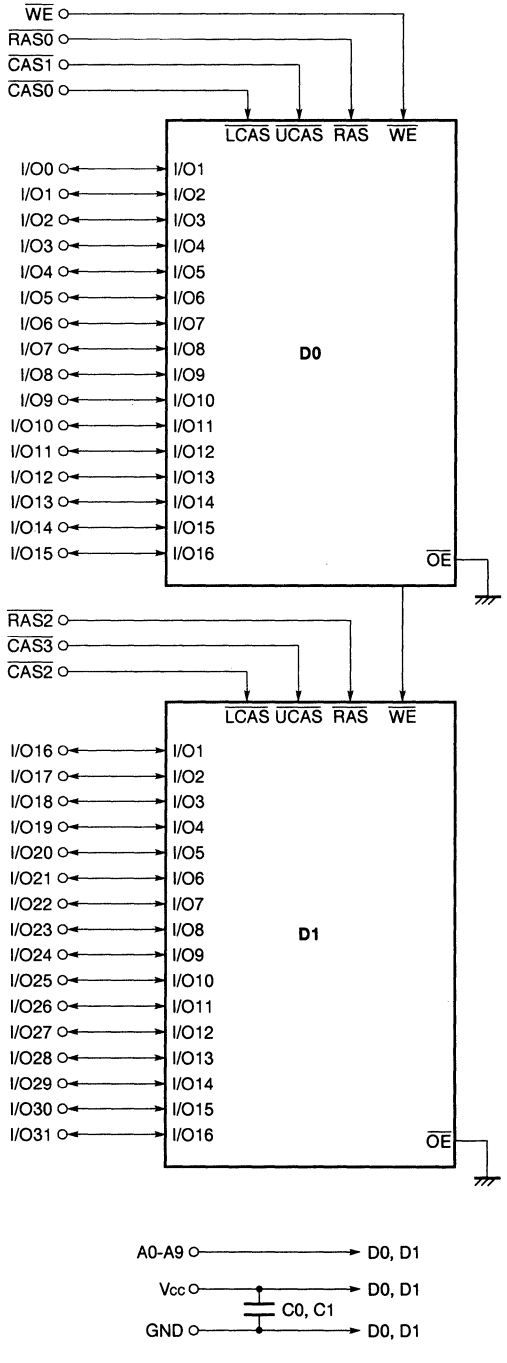


A0 - A9 : Address Inputs
I/O0 - I/O31 : Data Inputs/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$: Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{WE}$: Write Enable
Vcc : Power Supply
GND : Ground
NC : No Connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time	
		60 ns	70 ns
PD0	67	GND	GND
PD1	68	GND	GND
PD2	69	NC	GND
PD3	70	NC	NC

Block Diagram



Remark D0, D1: μPD4218165

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		2	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			30	pF
	C_{I2}	$\overline{WE}$			34	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			22	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			22	
Data input/output capacitance	$C_{I/O}$	I/O0 - I/O31			20	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		320	mA	1, 2, 3
			t_{RAC} = 70 ns		300		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH(MIN.)}$, I_O = 0 mA			4.0	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA			2.0		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS} \geq V_{IH(MIN.)}$ $t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		320	mA	1, 2, 3 ,4
			t_{RAC} = 70 ns		300		
Operating current (Hyper page mode (EDO))	I_{CC4}	$\overline{RAS} \leq V_{IL(MAX.)}$, $\overline{CAS}$ Cycling $t_{HPC} = t_{HPC(MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		220	mA	1, 2, 5
			t_{RAC} = 70 ns		200		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		320	mA	1, 2
			t_{RAC} = 70 ns		300		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –2.5 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.1 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL(MAX.)}$ and $\overline{CAS} \geq V_{IH(MIN.)}$.

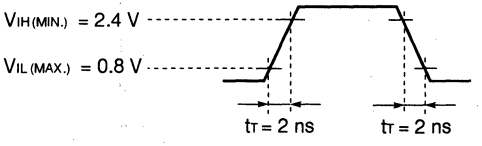
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

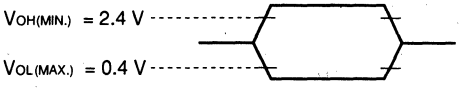
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

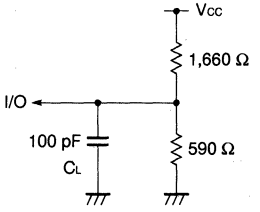
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	104	–	124	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	–	50	–	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	10	–	10	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	10	10,000	12	10,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	10	–	12	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	40	–	50	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	14	45	14	52	ns	1
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	–	5	–	ns	2
Row Address Setup Time	t_{ASR}	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	10	–	10	–	ns	
Column Address Setup Time	t_{ASC}	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	10	–	12	–	ns	
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0	–	0	–	ns	
Transition Time (Rise and Fall)	t_T	1	50	1	50	ns	
Refresh Time	t_{REF}	–	16	–	16	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	–	15	–	18	ns	1
Access Time from Column Address	t_{AA}	–	30	–	35	ns	1
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ Setup Time	t_{WCS}	0	–	0	–	ns	2
Data-in Setup Time	t_{DS}	0	–	0	–	ns	3
Data-in Hold Time	t_{DH}	10	–	10	–	ns	3

Notes 1. In early write cycles, $t_{WCH(MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
3. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles.

Hyper Page Mode (EDO)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{HPC}	25	–	30	–	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	10	10,000	12	10,000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	10	–	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	–	35	–	40	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	–	40	–	ns	
Data Output Hold Time	t_{DHC}	5	–	5	–	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	2, 3
$\overline{WE}$ Pulse Width	t_{WPZ}	10	–	10	–	ns	3
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	2, 3
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	2, 3

Notes 1. $t_{HPC(MIN.)}$ is applied to $\overline{CAS}$ access.

2. $t_{OFC(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

3. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
$\overline{WE}$: inactive
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
$\overline{WE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

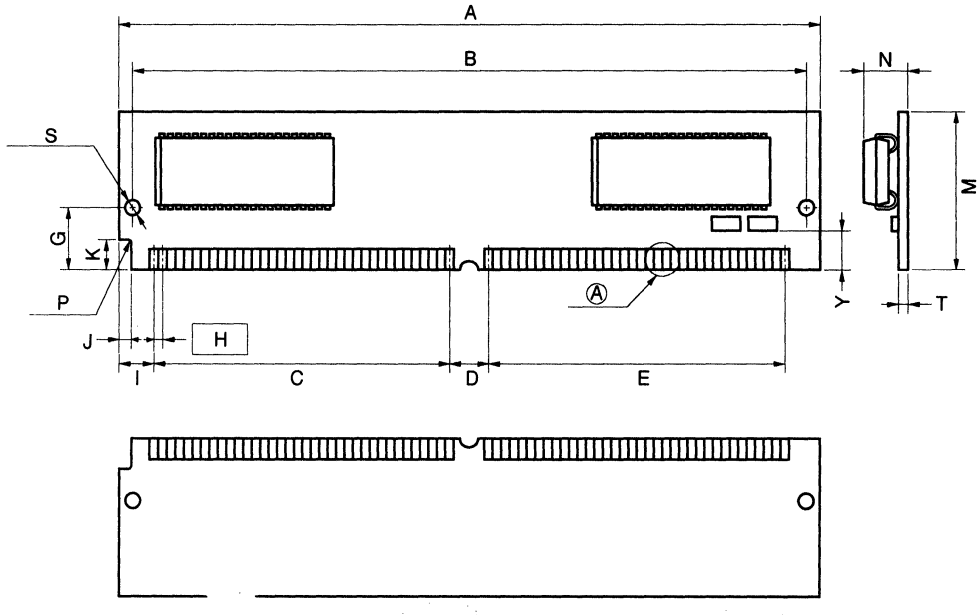
Refresh Cycle

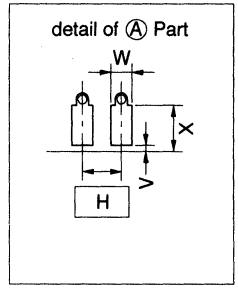
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	5	–	5	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	–	5	–	ns	
$\overline{WE}$ Hold Time	t_{WHR}	15	–	15	–	ns	

Timing Chart
Please refer to Timing Chart 7, page 445.

Package Drawing

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
P	R1.57	R0.062
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.
Y	3.17 MIN.	0.124 MIN.

M72B-50A46

NEC

MOS INTEGRATED CIRCUIT
MC-422000F32

2 M-WORD BY 32-BIT DYNAMIC RAM MODULE
HYPER PAGE MODE (EDO)

Description

The MC-422000F32 is a 2,097,152 words by 32 bits dynamic RAM module on which 4 pieces of 16 M DRAM: μPD4218165 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 2,097,152 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) Cycle Time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC-422000F32-60	60 ns	104 ns	25 ns	1,782 mW	22 mW (CMOS level input)
MC-422000F32-70	70 ns	124 ns	30 ns	1,672 mW	

- 1,024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

Ordering Information

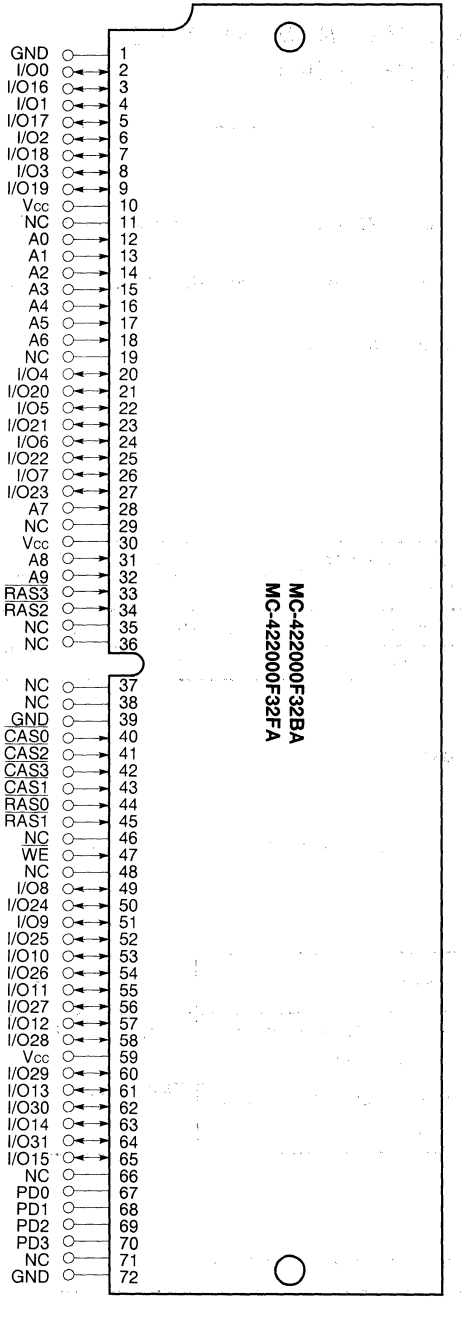
Part number	Access time (MAX.)	Package	Mounted devices
MC-422000F32BA-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	4 pieces of μPD4218165LE (400 mil SOJ) [Double side]
MC-422000F32BA-70	70 ns		
MC-422000F32FA-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-422000F32FA-70	70 ns		

The information in this document is subject to change without notice.

Document No. M10439EJ2V0DSU1

Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)

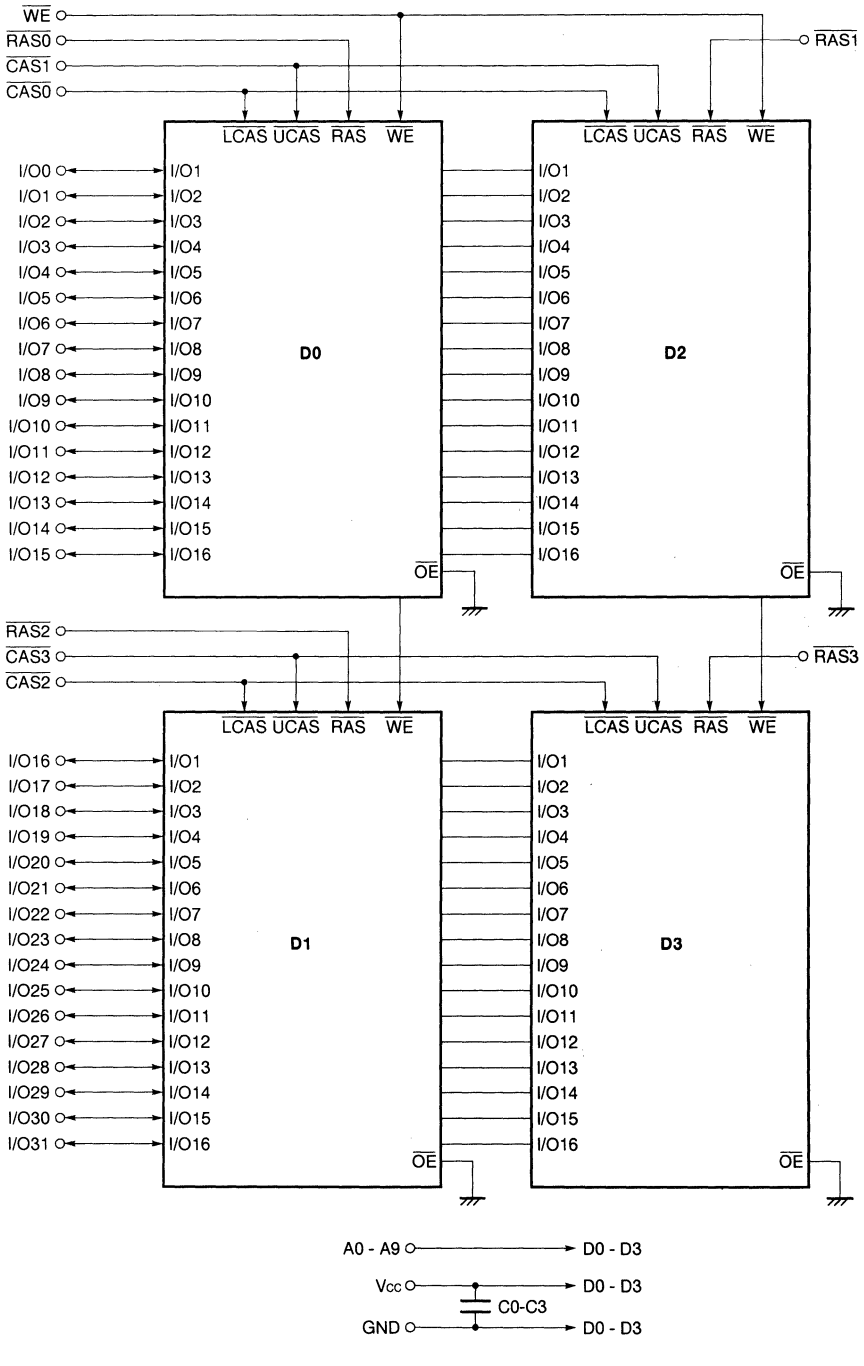


A0 - A9 : Address Inputs
I/O0 - I/O31 : Data Inputs/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$: Column Address Strobe
$\overline{RAS0}$ - $\overline{RAS3}$: Row Address Strobe
$\overline{WE}$: Write Enable
Vcc : Power Supply
GND : Ground
NC : No Connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time	
		60 ns	70 ns
PD0	67	NC	NC
PD1	68	NC	NC
PD2	69	NC	GND
PD3	70	NC	NC

Block Diagram



Remark D0 - D3: μPD4218165

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		4	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			40	pF
	C_{I2}	$\overline{WE}$			48	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS3}$			22	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			29	
Data input/output capacitance	$C_{I/O}$	I/O0 - I/O31			26	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		324	mA	1, 2, 3
			t_{RAC} = 70 ns		304		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH(MIN.)}$, I_O = 0 mA			8.0	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA			4.0		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS} \geq V_{IH(MIN.)}$ $t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		324	mA	1, 2, 3 ,4
			t_{RAC} = 70 ns		304		
Operating current (Hyper page mode (EDO))	I_{CC4}	$\overline{RAS} \leq V_{IL(MAX.)}$, $\overline{CAS}$ Cycling $t_{HPC} = t_{HPC(MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		224	mA	1, 2, 5
			t_{RAC} = 70 ns		204		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		324	mA	1, 2
			t_{RAC} = 70 ns		304		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –2.5 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.1 mA			0.4	V	

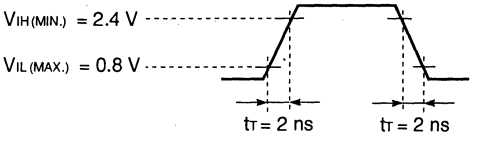
Notes 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.
3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL(MAX.)}$ and $\overline{CAS} \geq V_{IH(MIN.)}$.
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

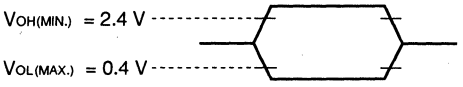
AC Characteristics (Recommended operating conditions unless otherwise noted)

AC Characteristics Test Conditions

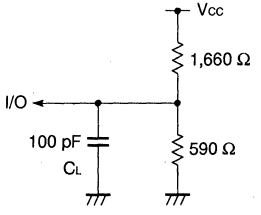
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	104	–	124	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	–	50	–	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	10	–	10	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	10	10,000	12	10,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	10	–	12	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	40	–	50	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	14	45	14	52	ns	1
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	–	5	–	ns	2
Row Address Setup Time	t_{ASR}	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	10	–	10	–	ns	
Column Address Setup Time	t_{ASC}	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	10	–	12	–	ns	
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0	–	0	–	ns	
Transition Time (Rise and Fall)	t_T	1	50	1	50	ns	
Refresh Time	t_{REF}	–	16	–	16	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	–	15	–	18	ns	1
Access Time from Column Address	t_{AA}	–	30	–	35	ns	1
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ Setup Time	t_{WCS}	0	–	0	–	ns	2
Data-in Setup Time	t_{DS}	0	–	0	–	ns	3
Data-in Hold Time	t_{DH}	10	–	10	–	ns	3

Notes 1. In early write cycles, $t_{WCH(MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles.

Hyper Page Mode (EDO)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{HPC}	25	–	30	–	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	10	10,000	12	10,000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	10	–	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	–	35	–	40	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	–	40	–	ns	
Data Output Hold Time	t_{DHC}	5	–	5	–	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	2, 3
$\overline{WE}$ Pulse Width	t_{WPZ}	10	–	10	–	ns	3
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	2, 3
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	2, 3

Notes 1. $t_{HPC(MIN.)}$ is applied to $\overline{CAS}$ access.

2. $t_{OFC(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

3. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
$\overline{WE}$: inactive
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
$\overline{WE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

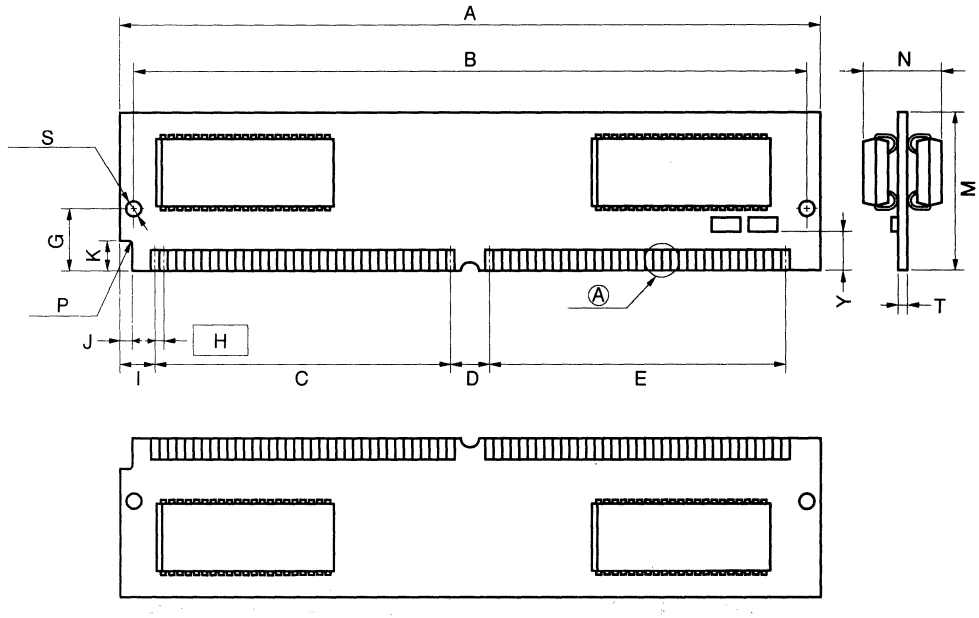
Refresh Cycle

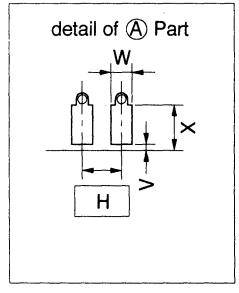
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	5	–	5	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	–	5	–	ns	
$\overline{WE}$ Hold Time	t_{WHR}	15	–	15	–	ns	

Timing Chart
Please refer to Timing Chart 7, page 445.

Package Drawing

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.
Y	3.17 MIN.	0.124 MIN.

M72B-50A45

NEC

MOS INTEGRATED CIRCUIT

MC-424000F32

4 M-WORD BY 32-BIT DYNAMIC RAM MODULE HYPER PAGE MODE (EDO)

Description

The MC-424000F32 is a 4,194,304 words by 32 bits dynamic RAM module on which 8 pieces of 16 M DRAM: μPD4217405 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 4,194,304 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC-424000F32-60	60 ns	104 ns	25 ns	4,840 mW	44 mW (CMOS level input)
MC-424000F32-70	70 ns	124 ns	30 ns	4,400 mW	

- 2,048 refresh cycles/32 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

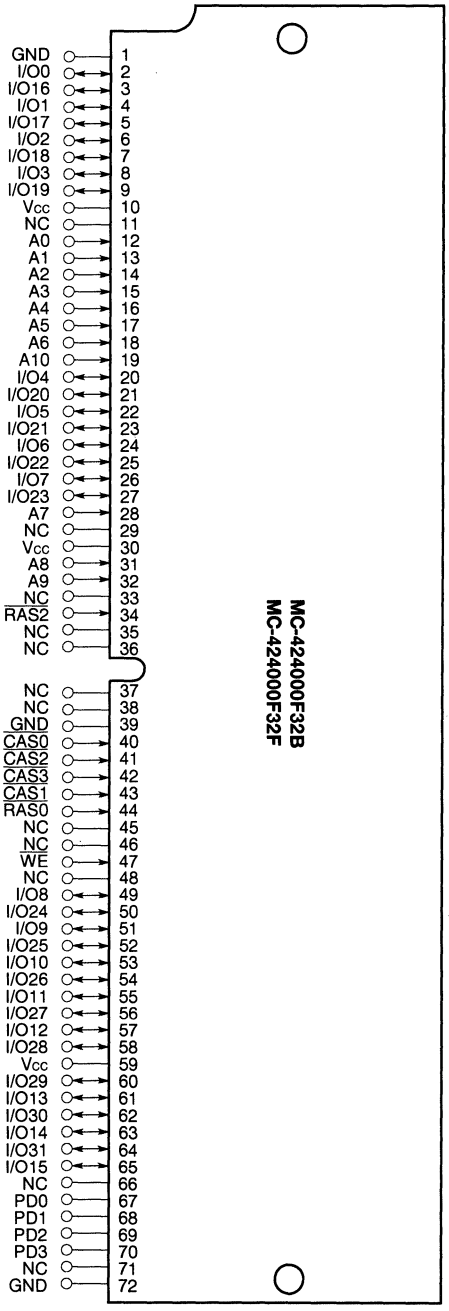
Document No. M10533EJ2V0DSU1

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-424000F32B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	8 pieces of μPD4217405LA (300 mil SOJ) [Single side]
MC-424000F32B-70	70 ns		
MC-424000F32F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-424000F32F-70	70 ns		

Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)

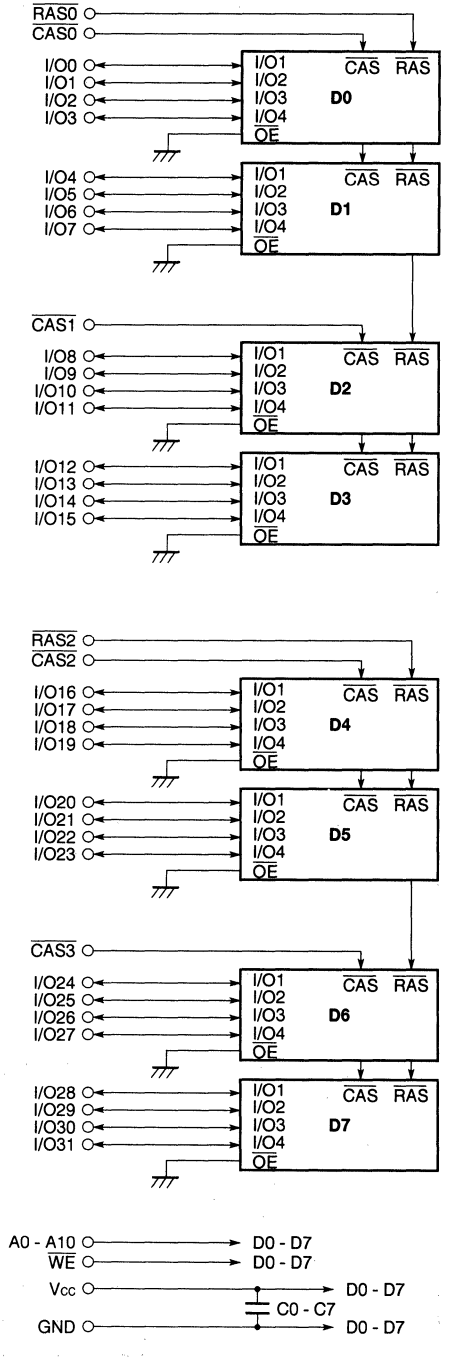


A0 - A10 : Address Inputs
I/O0 - I/O31 : Data Inputs/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$: Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$: Row Address Strobe
$\overline{WE}$: Write Enable
Vcc : Power Supply
GND : Ground
NC : No Connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time	
		60 ns	70 ns
PD0	67	GND	GND
PD1	68	NC	NC
PD2	69	NC	GND
PD3	70	NC	NC

Block Diagram



Remark D0 - D7: μPD4217405

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		8	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			68	pF
	C_{I2}	$\overline{WE}$			76	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			43	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			29	
Data input/output capacitance	$C_{I/O}$	I/O0 - I/O31			17	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		880	mA	1, 2, 3
			t_{RAC} = 70 ns		800		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH(MIN.)}$, I_O = 0 mA			16	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA			8		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS} \geq V_{IH(MIN.)}$ $t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		880	mA	1, 2, 3 ,4
			t_{RAC} = 70 ns		800		
Operating current (Hyper page mode (EDO))	I_{CC4}	$\overline{RAS} \leq V_{IL(MAX.)}$, $\overline{CAS}$ Cycling $t_{HPC} = t_{HPC(MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		720	mA	1, 2, 5
			t_{RAC} = 70 ns		640		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		880	mA	1, 2
			t_{RAC} = 70 ns		800		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL(MAX.)}$ and $\overline{CAS} \geq V_{IH(MIN.)}$.

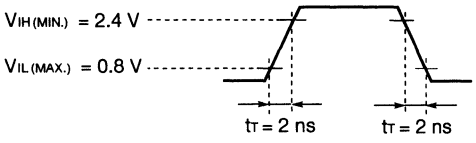
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

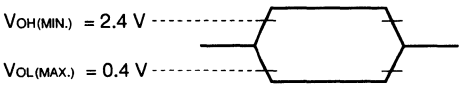
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

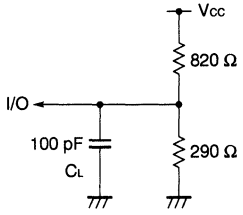
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	104	–	124	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	–	50	–	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	10	–	10	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	10	10,000	12	10,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	10	–	12	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	40	–	50	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	14	45	14	52	ns	1
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	–	5	–	ns	2
Row Address Setup Time	t_{ASR}	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	10	–	10	–	ns	
Column Address Setup Time	t_{ASC}	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	10	–	12	–	ns	
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0	–	0	–	ns	
Transition Time (Rise and Fall)	t_T	1	50	1	50	ns	
Refresh Time	t_{REF}	–	32	–	32	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	–	15	–	18	ns	1
Access Time from Column Address	t_{AA}	–	30	–	35	ns	1
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ Setup Time	t_{WCS}	0	–	0	–	ns	2
Data-in Setup Time	t_{DS}	0	–	0	–	ns	3
Data-in Hold Time	t_{DH}	10	–	10	–	ns	3

Notes 1. In early write cycles, $t_{WCH(MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles.

Hyper Page Mode (EDO)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{HPC}	25	–	30	–	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	10	10,000	12	10,000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	10	–	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	–	35	–	40	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	–	40	–	ns	
Data Output Hold Time	t_{DHC}	5	–	5	–	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	2, 3
$\overline{WE}$ Pulse Width	t_{WPZ}	10	–	10	–	ns	3
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	2, 3
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	2, 3

Notes 1. $t_{HPC(MIN.)}$ is applied to $\overline{CAS}$ access.

2. $t_{OFC(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

3. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)

$\overline{WE}$: inactive

t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.

t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)

$\overline{WE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

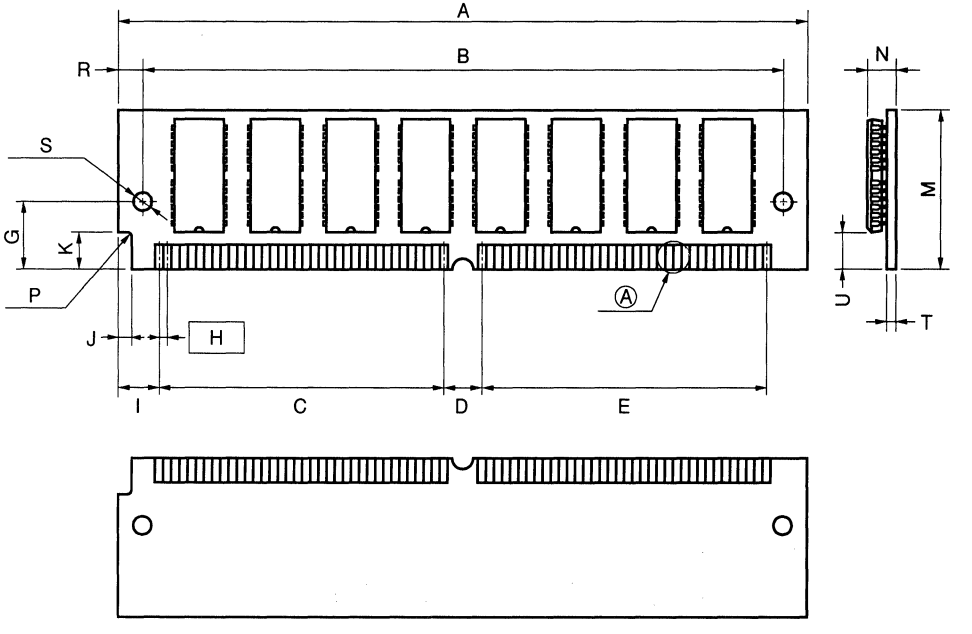
Refresh Cycle

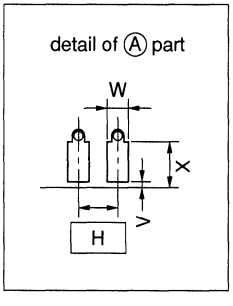
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	5	–	5	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	–	5	–	ns	
$\overline{WE}$ Setup Time	t_{WSR}	10	–	10	–	ns	
$\overline{WE}$ Hold Time	t_{WHR}	15	–	15	–	ns	

Timing Chart
Please refer to Timing Chart 8, page 457.

Package Drawing

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19±0.13	$3.984^{+0.005}_{-0.006}$
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
P	R1.57	R0.062
R	3.38±0.13	$0.133^{+0.006}_{-0.005}$
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	5.5 MIN.	0.216 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72B-50A54

NEC

MOS INTEGRATED CIRCUIT

MC-428000F32

8 M-WORD BY 32-BIT DYNAMIC RAM MODULE HYPER PAGE MODE (EDO)

Description

The MC-428000F32 is a 8,388,608 words by 32 bits dynamic RAM module on which 16 pieces of 16 M DRAM: μPD4217405 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 8,388,608 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC-428000F32-60	60 ns	104 ns	25 ns	5,170 mW	88 mW (CMOS level input)
MC-428000F32-70	70 ns	124 ns	30 ns	4,730 mW	

- 2,048 refresh cycles/32 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

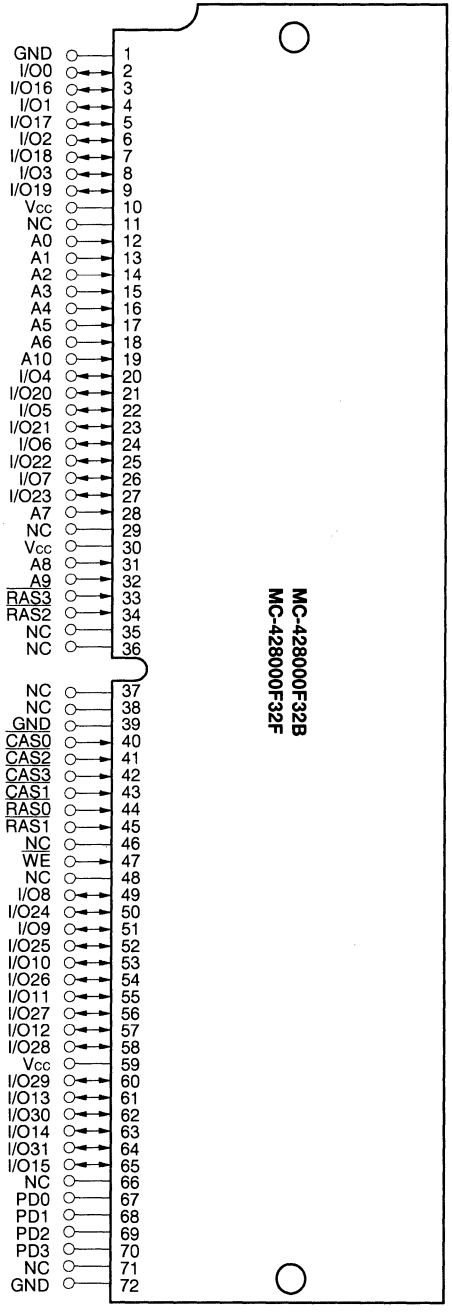
Document No. M10534EJ2V0DSU1

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-428000F32B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	16 pieces of μPD4217405LA (300 mil SOJ) [Double side]
MC-428000F32B-70	70 ns		
MC-428000F32F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-428000F32F-70	70 ns		

Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)

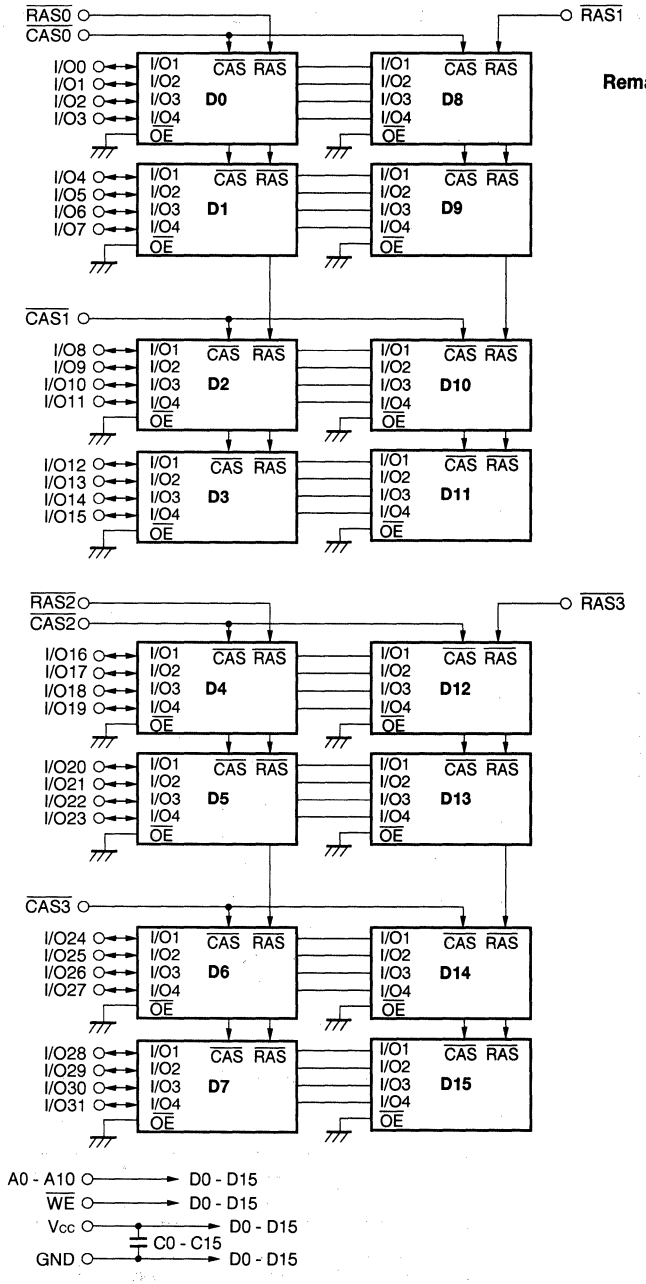


A0 - A10 : Address Inputs
I/O0 - I/O31 : Data Inputs/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$: Column Address Strobe
$\overline{RAS0}$ - $\overline{RAS3}$: Row Address Strobe
$\overline{WE}$: Write Enable
Vcc : Power Supply
GND : Ground
NC : No Connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time	
		60 ns	70 ns
PD0	67	NC	NC
PD1	68	GND	GND
PD2	69	NC	GND
PD3	70	NC	NC

Block Diagram



Remark D0 - D15: μPD4217405

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		16	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			121	pF
	C_{I2}	$\overline{WE}$			137	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS3}$			48	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			48	
Data input/output capacitance	$C_{I/O}$	I/O0 - I/O31			29	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling	t_{RAC} = 60 ns		940	mA	1, 2, 3
		$t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		860		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH(MIN.)}$, I_O = 0 mA			32	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA			16		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS} \geq V_{IH(MIN.)}$	t_{RAC} = 60 ns		940	mA	1, 2, 3 ,4
		$t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		860		
Operating current (Hyper page mode (EDO))	I_{CC4}	$\overline{RAS} \leq V_{IL(MAX.)}$, $\overline{CAS}$ Cycling	t_{RAC} = 60 ns		780	mA	1, 2, 5
		$t_{HPC} = t_{HPC(MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		700		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling	t_{RAC} = 60 ns		940	mA	1, 2
		$t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		860		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

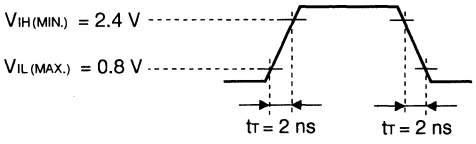
Notes 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.
3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL(MAX.)}$ and $\overline{CAS} \geq V_{IH(MIN.)}$.
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

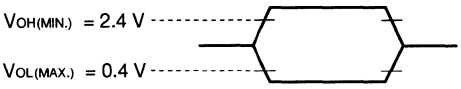
AC Characteristics (Recommended operating conditions unless otherwise noted)

AC Characteristics Test Conditions

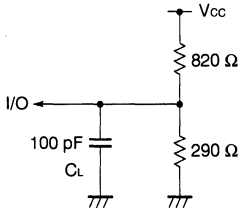
(1) Input timing specification



(2) Output timing specification



(3) Output load conditions



Common to Read, Write Cycle

Parameter	Symbol	tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	tRC	104	–	124	–	ns	
$\overline{RAS}$ Precharge Time	tRP	40	–	50	–	ns	
$\overline{CAS}$ Precharge Time	tCPN	10	–	10	–	ns	
$\overline{RAS}$ Pulse Width	tRAS	60	10,000	70	10,000	ns	
$\overline{CAS}$ Pulse Width	tCAS	10	10,000	12	10,000	ns	
$\overline{RAS}$ Hold Time	tRSH	10	–	12	–	ns	
$\overline{CAS}$ Hold Time	tCSH	40	–	50	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	14	45	14	52	ns	1
$\overline{RAS}$ to Column Address Delay Time	tRAD	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	5	–	5	–	ns	2
Row Address Setup Time	tASR	0	–	0	–	ns	
Row Address Hold Time	tRAH	10	–	10	–	ns	
Column Address Setup Time	tASC	0	–	0	–	ns	
Column Address Hold Time	tCAH	10	–	12	–	ns	
$\overline{CAS}$ to Data Setup Time	tCLZ	0	–	0	–	ns	
Transition Time (Rise and Fall)	tT	1	50	1	50	ns	
Refresh Time	tREF	–	32	–	32	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	–	15	–	18	ns	1
Access Time from Column Address	t_{AA}	–	30	–	35	ns	1
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ Setup Time	t_{WCS}	0	–	0	–	ns	2
Data-in Setup Time	t_{DS}	0	–	0	–	ns	3
Data-in Hold Time	t_{DH}	10	–	10	–	ns	3

Notes 1. In early write cycles, $t_{WCH(MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles.

Hyper Page Mode (EDO)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{HPC}	25	–	30	–	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	10	10,000	12	10,000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	10	–	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	–	35	–	40	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	–	40	–	ns	
Data Output Hold Time	t_{DHC}	5	–	5	–	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	2, 3
$\overline{WE}$ Pulse Width	t_{WPZ}	10	–	10	–	ns	3
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	2, 3
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	2, 3

Notes 1. $t_{HPC(MIN.)}$ is applied to $\overline{CAS}$ access.

2. $t_{OFC(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

3. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
$\overline{WE}$: inactive
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
$\overline{WE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

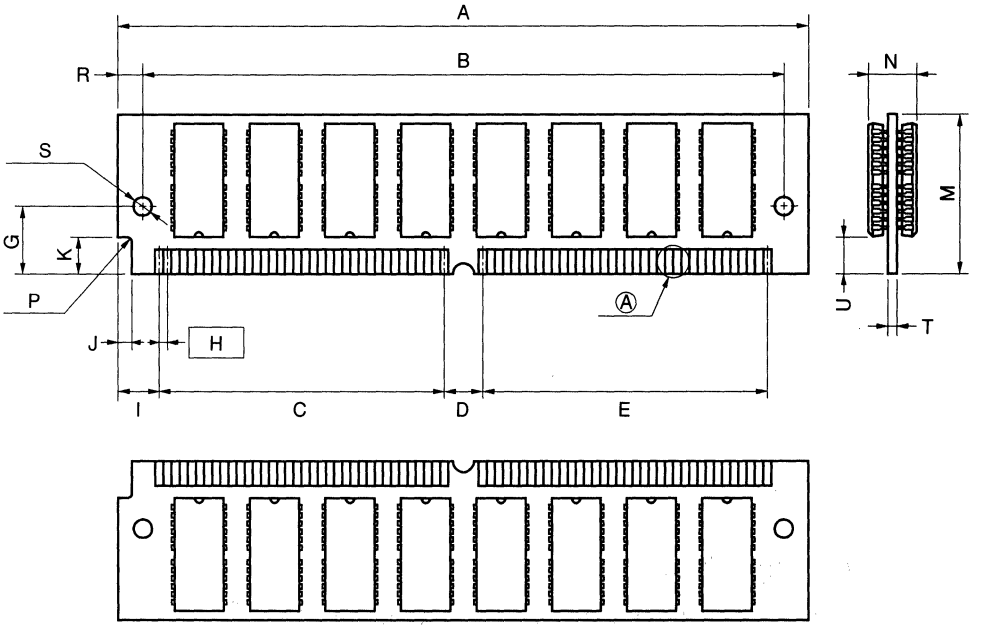
Refresh Cycle

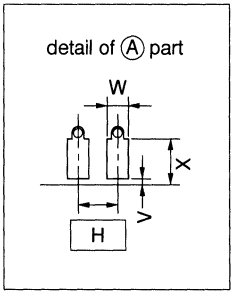
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	5	–	5	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	–	5	–	ns	
$\overline{WE}$ Setup Time	t_{WSR}	10	–	10	–	ns	
$\overline{WE}$ Hold Time	t_{WHR}	15	–	15	–	ns	

Timing Chart
Please refer to Timing Chart 8, page 457.

Package Drawing

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19±0.13	$3.984^{+0.005}_{-0.006}$
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
R	3.38±0.13	$0.133^{+0.006}_{-0.005}$
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	5.5 MIN.	0.216 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72B-50A55

4 Byte SIMM
[Fast Page]

NEC

MOS INTEGRATED CIRCUIT

MC-421000A32BA, 421000A32FA

1 M-WORD BY 32-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-421000A32BA, 421000A32FA are 1,048,576 words by 32 bits dynamic RAM module on which 2 pieces of 16 M DRAM: μPD4218160 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1,048,576 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-421000A32-60	60 ns	110 ns	1,760 mW	11 mW (CMOS level input)
MC-421000A32-70	70 ns	130 ns	1,650 mW	
MC-421000A32-80	80 ns	150 ns	1,540 mW	

- 1,024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

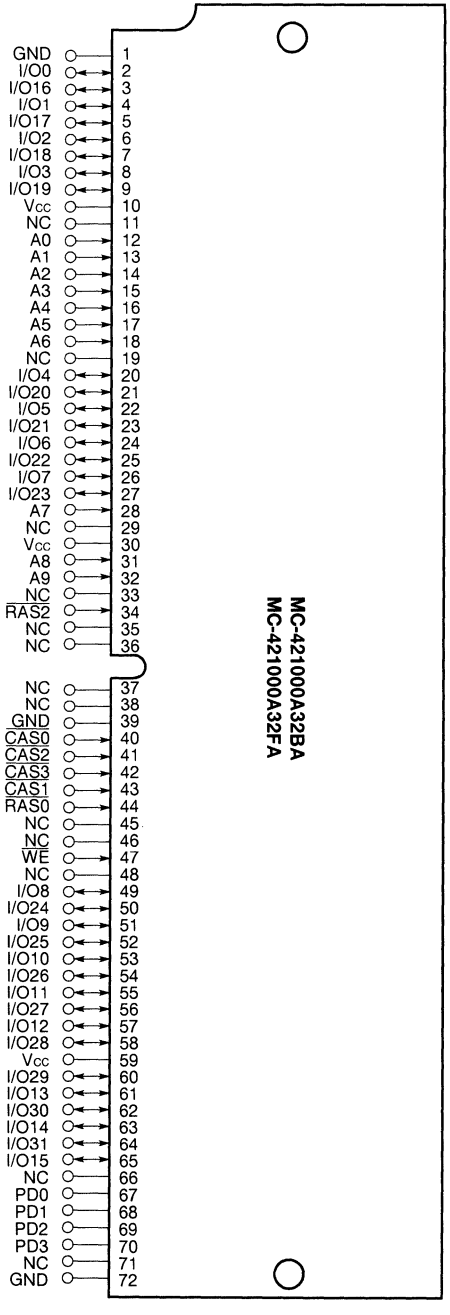
Document No. M10502EJ2V0DSU1

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000A32BA-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	2 pieces of μPD4218160LE (400 mil SOJ) [Single side]
MC-421000A32BA-70	70 ns		
MC-421000A32BA-80	80 ns		
MC-421000A32FA-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-421000A32FA-70	70 ns		
MC-421000A32FA-80	80 ns		

Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)

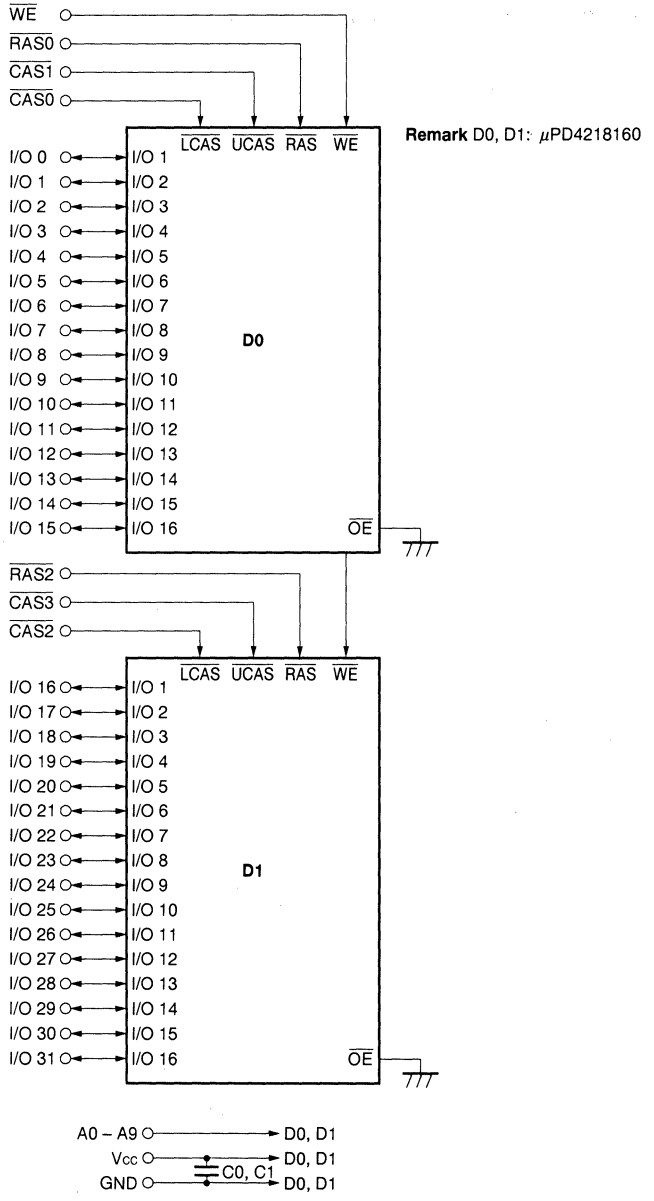


A0 - A9	:	Address Inputs
I/O0 - I/O31	:	Data Inputs/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$	:	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	:	Row Address Strobe
$\overline{WE}$	:	Write Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD0	67	GND	GND	GND
PD1	68	GND	GND	GND
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

Block Diagram



Remark D0, D1: μPD4218160

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		2	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			30	pF
	C_{I2}	$\overline{WE}$			34	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			22	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			22	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		320	mA	3, 4, 7
			t_{RAC} = 70 ns		300		
			t_{RAC} = 80 ns		280		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		4	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA		2		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		320	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		300		
			t_{RAC} = 80 ns		280		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		180	mA	3, 4, 6
			t_{RAC} = 70 ns		160		
			t_{RAC} = 80 ns		140		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		320	mA	3, 4
			t_{RAC} = 70 ns		300		
			t_{RAC} = 80 ns		280		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		−10	+10	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage	V_{OH}	I_O = −2.5 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.1 mA			0.4	V	

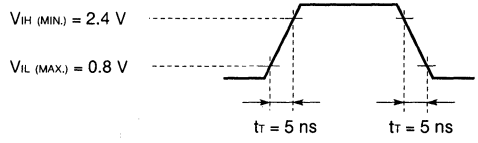
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		16		16		16	ms	

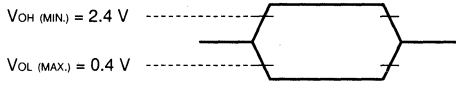
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification



10. For read cycles, access time is defined as follows:

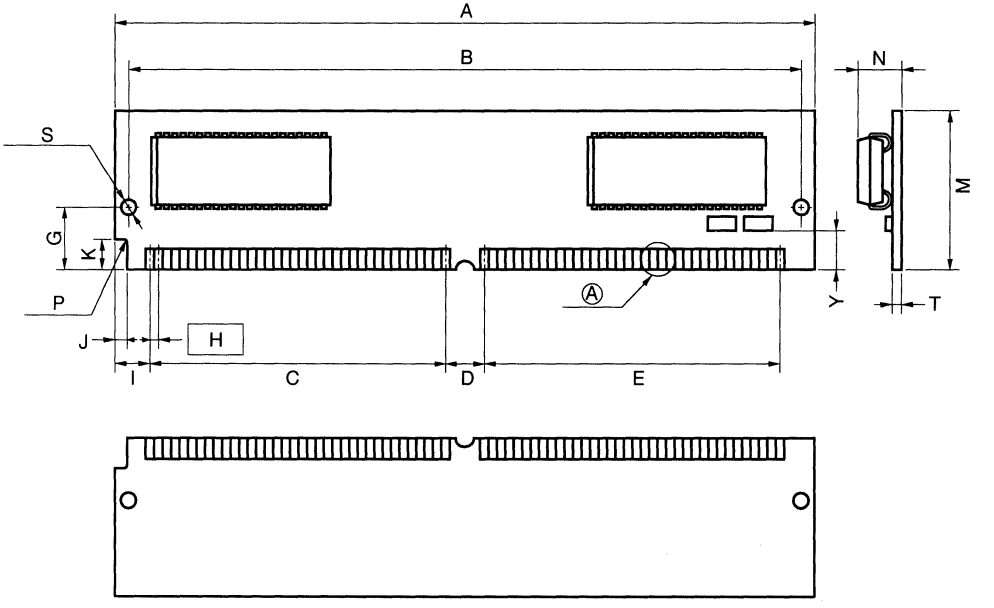
Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

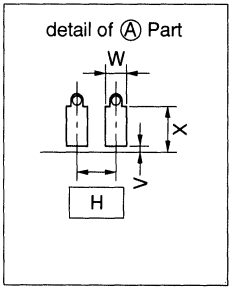
   $t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.
11. Loading conditions are 1 TTL and 100 pF.
12. $t_{OFF\ (MAX.)}$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP\ (MIN.)}$ requirements should be applied to $\overline{RAS}$/$\overline{CAS}$ cycles.
14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
15. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

Timing Chart
Please refer to Timing Chart 9, page 469.

Package Drawing

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
P	R1.57	R0.062
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.
Y	3.17 MIN.	0.124 MIN.

M72B-50A46

NEC

MOS INTEGRATED CIRCUIT

MC-421000A32

1 M-WORD BY 32-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-421000A32 is a 1,048,576 words by 32 bits dynamic RAM module on which 8 pieces of 4 M DRAM: μPD424400 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1,048,576 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-421000A32-60	60 ns	110 ns	3,960 mW	44 mW (CMOS level input)
MC-421000A32-70	70 ns	130 ns	3,520 mW	
MC-421000A32-80	80 ns	160 ns	3,520 mW	
MC-421000A32-10	100 ns	190 ns	3,520 mW	

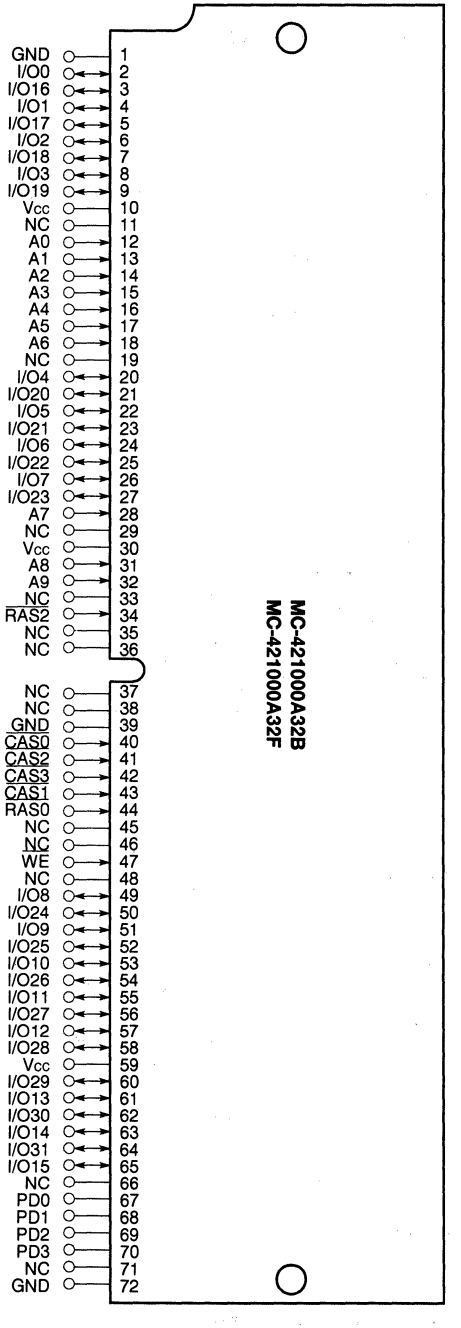
- 1,024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000A32B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	8 pieces of μPD424400LA (300 mil SOJ) [Single side]
MC-421000A32B-70	70 ns		
MC-421000A32B-80	80 ns		
MC-421000A32B-10	100 ns		
MC-421000A32F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-421000A32F-70	70 ns		
MC-421000A32F-80	80 ns		
MC-421000A32F-10	100 ns		

Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)

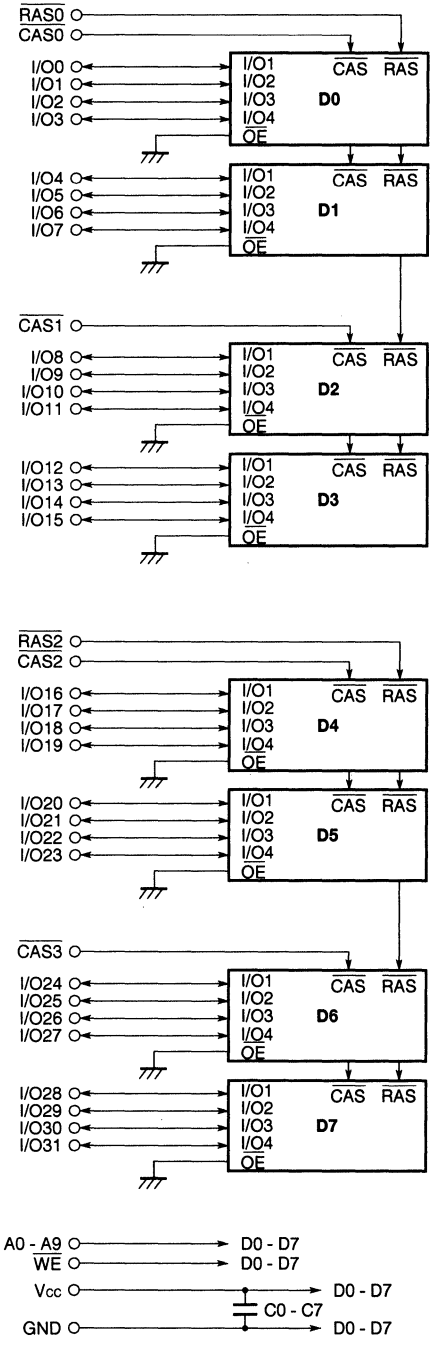


A0 - A9	: Address Inputs
I/O0 - I/O31	: Data Inputs/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$	: Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	: Row Address Strobe
$\overline{WE}$	: Write Enable
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time			
		60 ns	70 ns	80 ns	100 ns
PD0	67	GND	GND	GND	GND
PD1	68	GND	GND	GND	GND
PD2	69	NC	GND	NC	GND
PD3	70	NC	NC	GND	GND

Block Diagram



Remark D0 - D7 : μ PD424400

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		8	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			68	pF
	C_{I2}	$\overline{WE}$			76	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			43	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			29	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			17	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		720	mA	3, 4, 7
			t_{RAC} = 70 ns		640		
			t_{RAC} = 80 ns		640		
			t_{RAC} = 100 ns		640		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		16	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA		8		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		720	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		640		
			t_{RAC} = 80 ns		640		
			t_{RAC} = 100 ns		640		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		560	mA	3, 4, 6
			t_{RAC} = 70 ns		480		
			t_{RAC} = 80 ns		480		
			t_{RAC} = 100 ns		480		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		720	mA	3, 4
			t_{RAC} = 70 ns		640		
			t_{RAC} = 80 ns		640		
			t_{RAC} = 100 ns		640		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		−10	+10	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage	V_{OH}	I_O = −5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

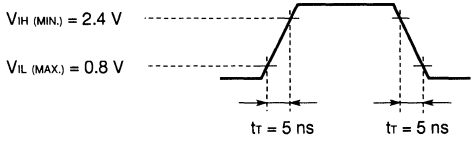
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		t_{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		160		190		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		60		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		20		20		25	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40		50	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45		55	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	17	50	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	0	25	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		70		80		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	100	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		20		20		25		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		100		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	25	75	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		10		10		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	10		10		10		10		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		55		ns	
Row Address Setup Time	t_{ASR}	0		0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		20		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		50		ns	
Read Command Setup Time	t_{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		10		10		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	15		15		15		20		ns	15
Data-in Setup Time	t_{DS}	0		0		0		0		ns	16
Data-in Hold Time	t_{DH}	15		15		15		20		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		15		20		ns	
$\overline{WE}$ Setup Time	t_{WSR}	0		0		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	10		10		15		20		ns	
Refresh Time	t_{REF}		16		16		16		16	ms	

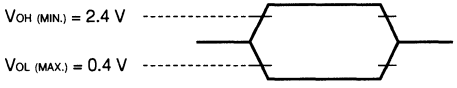
Notes

1. All voltages are referenced to GND.
2. After power up ($V_{CC} \geq V_{CC\ (MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles tc initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification

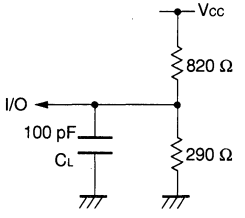


10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

11. Output load condition



12. $t_{OFF\ (MAX.)}$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.

13. $t_{CRP\ (MIN.)}$ requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.

14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

15. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles.

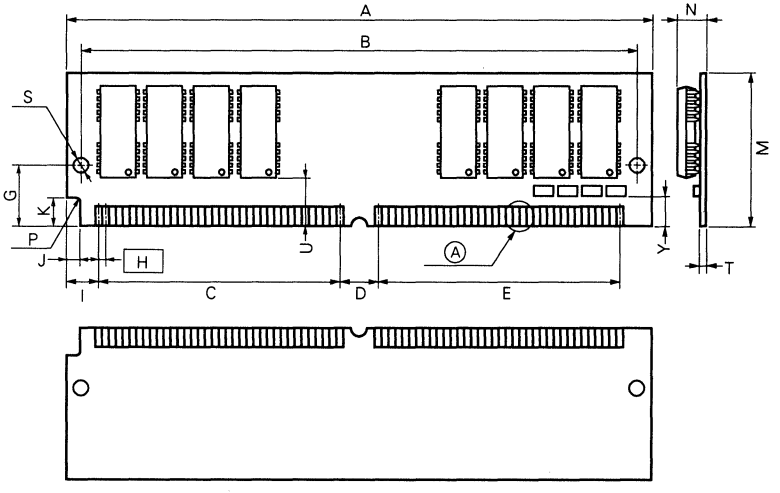
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

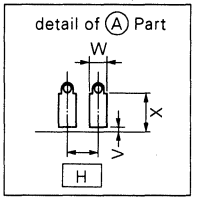
Timing Chart
Please refer to Timing Chart 10, page 479.

Package Drawing

[MC-421000A32B, 421000A32F]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





M72B-50A21-1

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
P	R 2.0	R 0.079
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	6.5 MIN.	0.255 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.75 MIN.	0.147 MIN.

NEC

MOS INTEGRATED CIRCUIT

MC-422000A32BA, 422000A32FA

2 M-WORD BY 32-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-422000A32BA, 422000A32FA are 2,097,152 words by 32 bits dynamic RAM module on which 4 pieces of 16 M DRAM: μPD4218160 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 2,097,152 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-422000A32-60	60 ns	110 ns	1,782 mW	22 mW (CMOS level input)
MC-422000A32-70	70 ns	130 ns	1,672 mW	
MC-422000A32-80	80 ns	150 ns	1,562 mW	

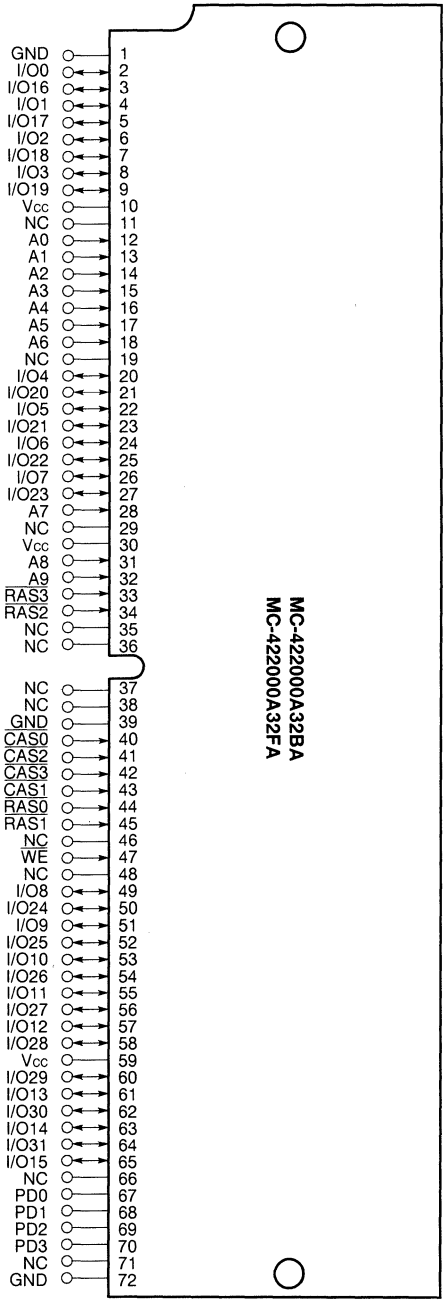
- 1,024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000A32BA-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	4 pieces of μPD4218160LE (400 mil SOJ) [Double side]
MC-422000A32BA-70	70 ns		
MC-422000A32BA-80	80 ns		
MC-422000A32FA-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-422000A32FA-70	70 ns		
MC-422000A32FA-80	80 ns		

Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)

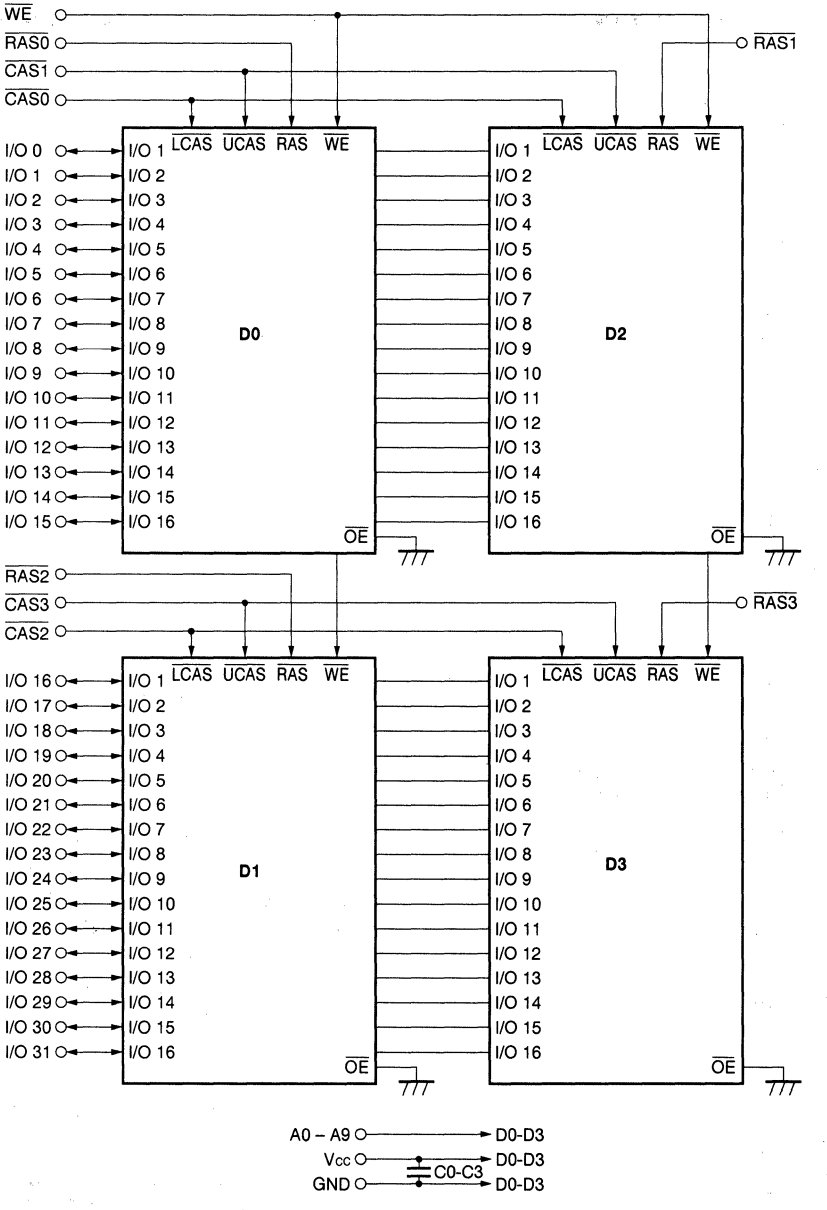


A0 - A9	:	Address Inputs
I/O0 - I/O31	:	Data Inputs/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$	:	Column Address Strobe
$\overline{RAS0}$ - $\overline{RAS3}$	:	Row Address Strobe
$\overline{WE}$	:	Write Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD0	67	NC	NC	NC
PD1	68	NC	NC	NC
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

Block Diagram



Remark D0 - D3: μPD4218160

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		4	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			40	pF
	C_{I2}	$\overline{WE}$			48	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS3}$			22	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			29	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			26	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		324	mA	3, 4, 7
			t_{RAC} = 70 ns		304		
			t_{RAC} = 80 ns		284		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		8	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		4		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		324	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		304		
			t_{RAC} = 80 ns		284		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		184	mA	3, 4, 6
			t_{RAC} = 70 ns		164		
			t_{RAC} = 80 ns		144		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		324	mA	3, 4
			t_{RAC} = 70 ns		304		
			t_{RAC} = 80 ns		284		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –2.5 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.1 mA			0.4	V	

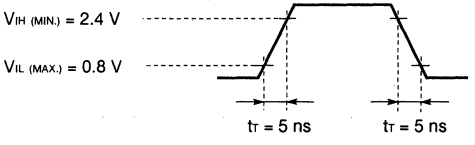
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	13	0	15	0	15	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		16		16		16	ms	

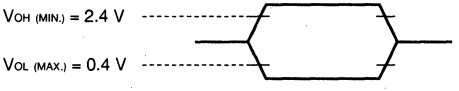
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification



10. For read cycles, access time is defined as follows:

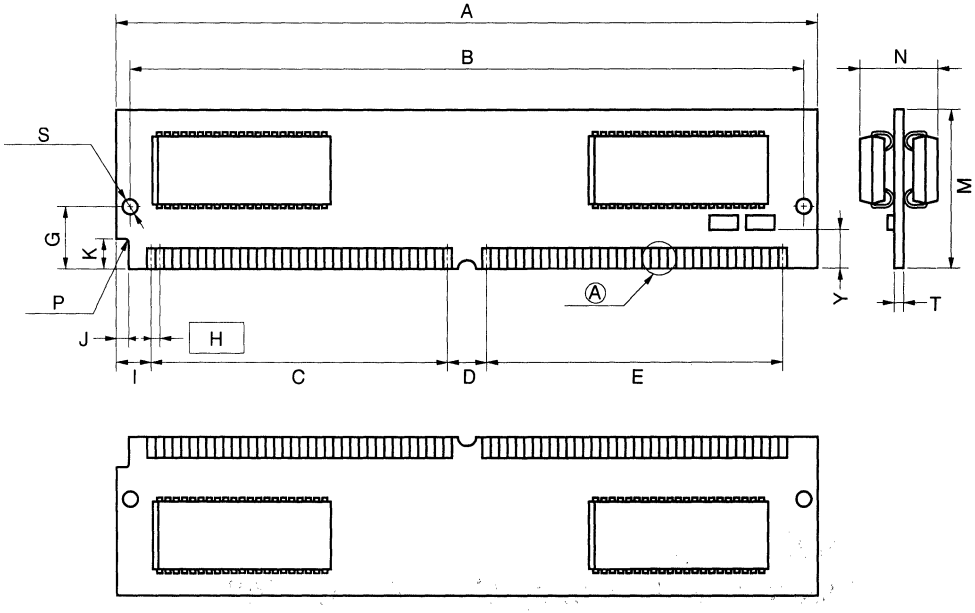
Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

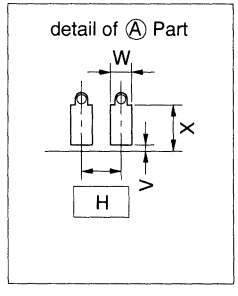
    $t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.
11. Loading conditions are 1 TTL and 100 pF.
12. $t_{OFF\ (MAX.)}$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP\ (MIN.)}$ requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
15. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.
16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

Timing Chart
Please refer to Timing Chart 9, page 469.

Package Drawing

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.
Y	3.17 MIN.	0.124 MIN.

M72B-50A45

NEC

MOS INTEGRATED CIRCUIT

MC-422000A32

2 M-WORD BY 32-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-422000A32 is a 2,097,152 words by 32 bits dynamic RAM module on which 16 pieces of 4 M DRAM: μPD424400 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 2,097,152 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-422000A32-60	60 ns	110 ns	4,290 mW	88 mW (CMOS level input)
MC-422000A32-70	70 ns	130 ns	3,850 mW	
MC-422000A32-80	80 ns	160 ns	3,850 mW	
MC-422000A32-10	100 ns	190 ns	3,850 mW	

- 1,024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

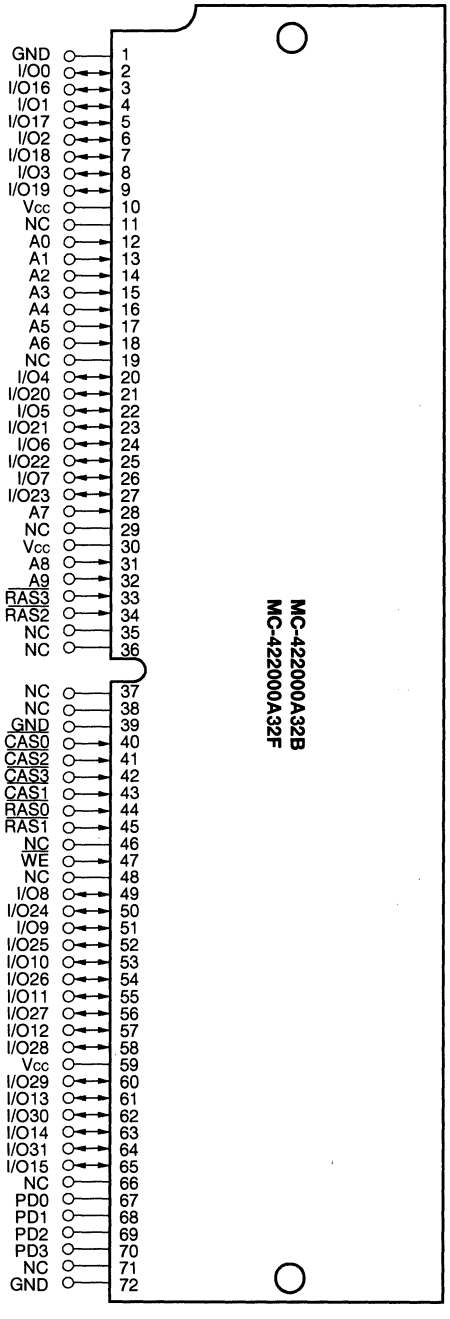
Document No. M10646EJ4V0DSU1

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000A32B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	16 pieces of μPD424400LA (300 mil SOJ) [Double side]
MC-422000A32B-70	70 ns		
MC-422000A32B-80	80 ns		
MC-422000A32B-10	100 ns		
MC-422000A32F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-422000A32F-70	70 ns		
MC-422000A32F-80	80 ns		
MC-422000A32F-10	100 ns		

Pin Configuration

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)

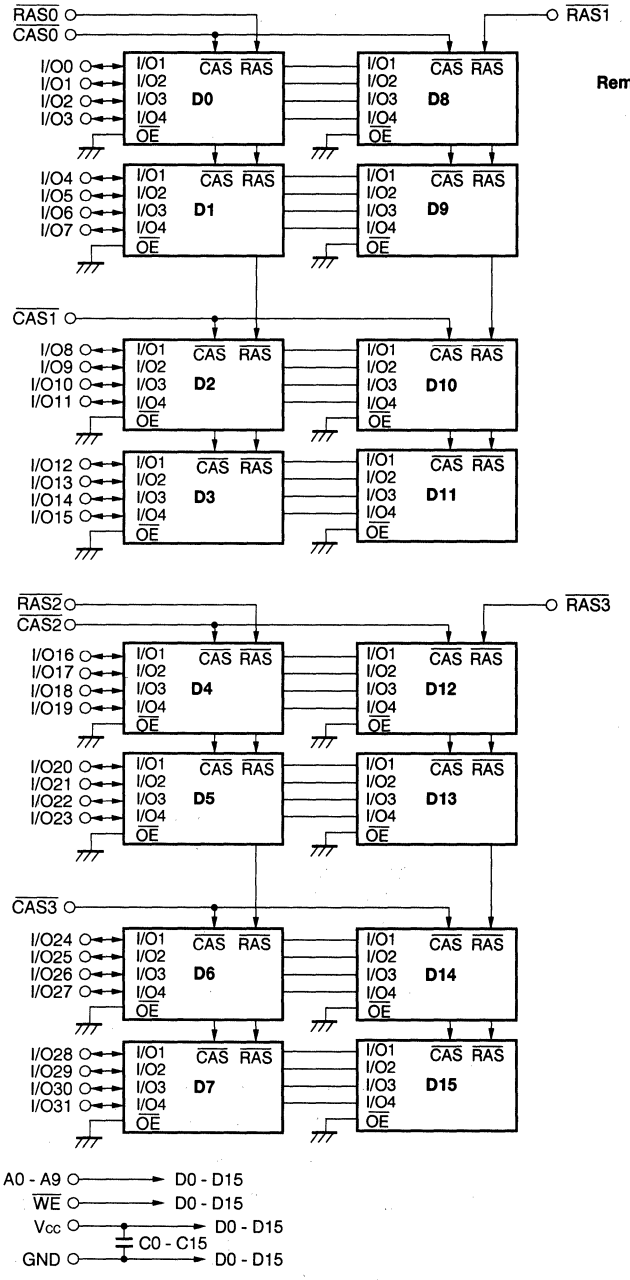


A0 - A9	:	Address Inputs
I/O0 - I/O31	:	Data Inputs/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$	:	Column Address Strobe
$\overline{RAS0}$ - $\overline{RAS3}$	:	Row Address Strobe
$\overline{WE}$	:	Write Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time			
		60 ns	70 ns	80 ns	100 ns
PD0	67	NC	NC	NC	NC
PD1	68	NC	NC	NC	NC
PD2	69	NC	GND	NC	GND
PD3	70	NC	NC	GND	GND

Block Diagram



Remark D0 - D15: μPD424400

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		16	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			121	pF
	C_{I2}	$\overline{WE}$			137	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS3}$			48	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			48	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			29	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		780	mA	3, 4, 7
			t_{RAC} = 70 ns		700		
			t_{RAC} = 80 ns		700		
			t_{RAC} = 100 ns		700		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		32	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA		16		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		780	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		700		
			t_{RAC} = 80 ns		700		
			t_{RAC} = 100 ns		700		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		620	mA	3, 4, 6
			t_{RAC} = 70 ns		540		
			t_{RAC} = 80 ns		540		
			t_{RAC} = 100 ns		540		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		780	mA	3, 4
			t_{RAC} = 70 ns		700		
			t_{RAC} = 80 ns		700		
			t_{RAC} = 100 ns		700		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		−10	+10	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage	V_{OH}	I_O = −5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

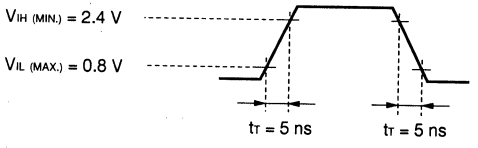
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		t_{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		160		190		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		60		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		20		20		25	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40		50	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45		55	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	17	50	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	0	25	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		70		80		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	100	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		20		20		25		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		100		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	25	75	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		10		10		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	10		10		10		10		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		55		ns	
Row Address Setup Time	t_{ASR}	0		0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		20		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		50		ns	
Read Command Setup Time	t_{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		10		10		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	15		15		15		20		ns	15
Data-in Setup Time	t_{DS}	0		0		0		0		ns	16
Data-in Hold Time	t_{DH}	15		15		15		20		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		15		20		ns	
$\overline{WE}$ Setup Time	t_{WSR}	0		0		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	10		10		15		20		ns	
Refresh Time	t_{REF}		16		16		16		16	ms	

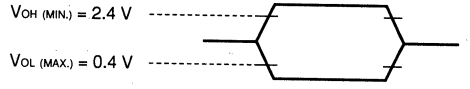
Notes

1. All voltages are referenced to GND.
2. After power up ($V_{CC} \geq V_{CC\ (MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification

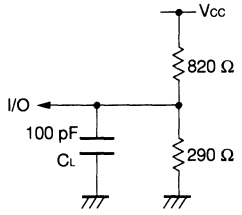


10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

11. Output load condition



12. $t_{OFF\ (MAX.)}$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.

13. $t_{CRP\ (MIN.)}$ requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.

14. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

15. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

16. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles.

17. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

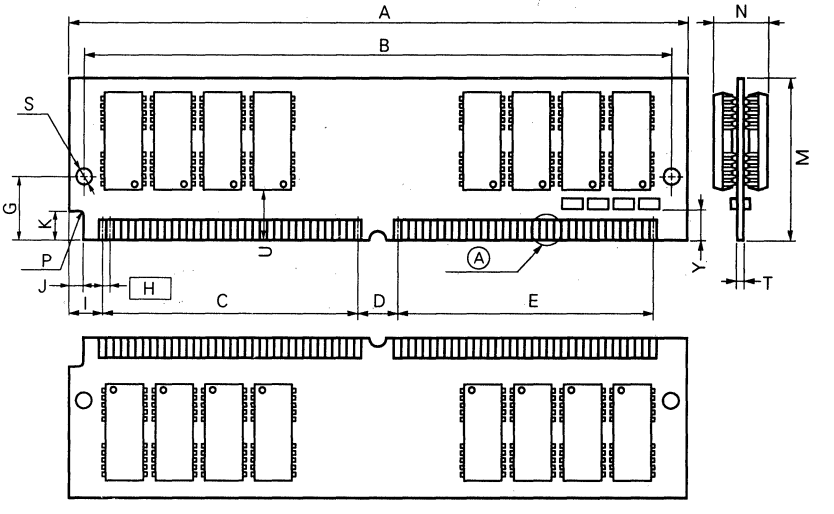
Timing Chart

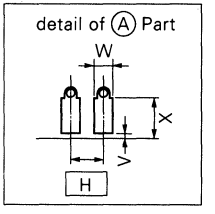
Please refer to Timing Chart 10, page 479.

Package Drawing

[MC-422000A32B, 422000A32F]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





M72B-50A22-1

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R 2.0	R 0.079
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	6.5 MIN.	0.255 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.75 MIN.	0.147 MIN.

NEC

MOS INTEGRATED CIRCUIT

MC-424000A32, 424000A36 SERIES

4 M-WORD BY 32-BIT, 4 M-WORD BY 36-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-424000A32 series is a 4,194,304 words by 32 bits dynamic RAM module on which 8 pieces of 16 M DRAM: μPD4217400 are assembled.

The MC-424000A36 series is a 4,194,304 words by 36 bits dynamic RAM module on which 8 pieces of 16 M DRAM: μPD4217400 and 4 pieces of 4 M DRAM: μPD424100 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 4,194,304 words by 32 bits organization (MC-424000A32 series)
- 4,194,304 words by 36 bits organization (MC-424000A36 series)
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-424000A32-60	60 ns	110 ns	4,840 mW	44 mW (CMOS level input)
MC-424000A32-70	70 ns	130 ns	4,400 mW	
MC-424000A32-80	80 ns	150 ns	3,960 mW	
MC-424000A36-60	60 ns	110 ns	7,480 mW	66 mW (CMOS level input)
MC-424000A36-70	70 ns	130 ns	6,600 mW	
MC-424000A36-80	80 ns	150 ns	5,940 mW	

- 2,048 refresh cycles/32 ms
- 2,048 refresh cycles/16 ms (MC-424000A36 burst refesh)
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

Document No. IC-3459 (Japan)

Ordering Information

[MC-424000A32 series]

Part number	Access time (MAX.)	Package	Mounted devices
MC-424000A32B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	8 pieces of μPD4217400LA (300 mil SOJ) [Single side]
MC-424000A32B-70	70 ns		
MC-424000A32B-80	80 ns		
MC-424000A32F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-424000A32F-70	70 ns		
MC-424000A32F-80	80 ns		

[MC-424000A36 series]

Part number	Access time (MAX.)	Package	Mounted devices
MC-424000A36BE-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	8 pieces of μPD4217400LA (300 mil SOJ) 4 pieces of μPD424100LA (300 mil SOJ) [Double side]
MC-424000A36BE-70	70 ns		
MC-424000A36BE-80	80 ns		
MC-424000A36FE-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-424000A36FE-70	70 ns		
MC-424000A36FE-80	80 ns		
MC-424000A36BJ-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	8 pieces of μPD4217400LA (300 mil SOJ) 4 pieces of μPD424100LA (300 mil SOJ) [Single side]
MC-424000A36BJ-70	70 ns		
MC-424000A36BJ-80	80 ns		
MC-424000A36FJ-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-424000A36FJ-70	70 ns		
MC-424000A36FJ-80	80 ns		

Quality Grade

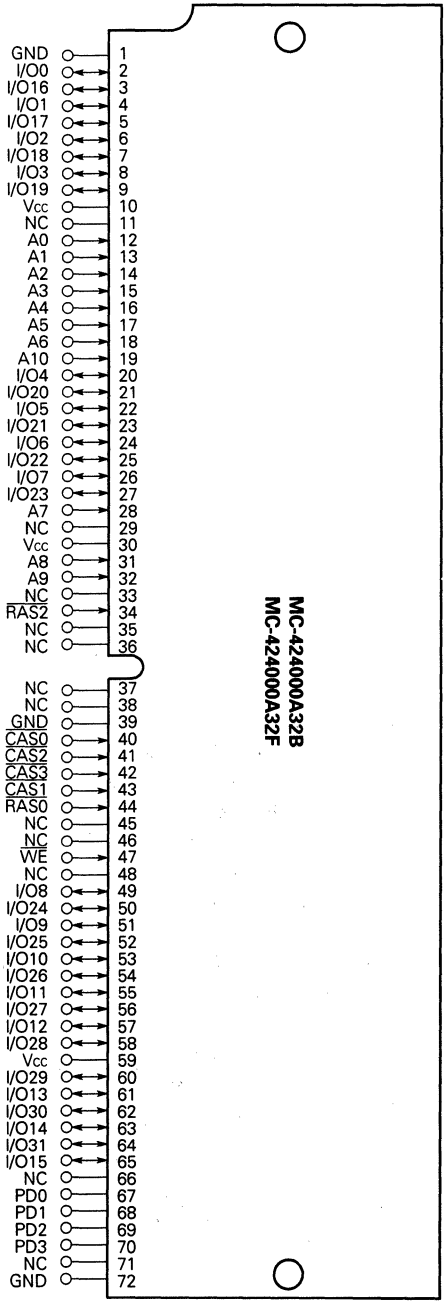
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configuration

[MC-424000A32 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



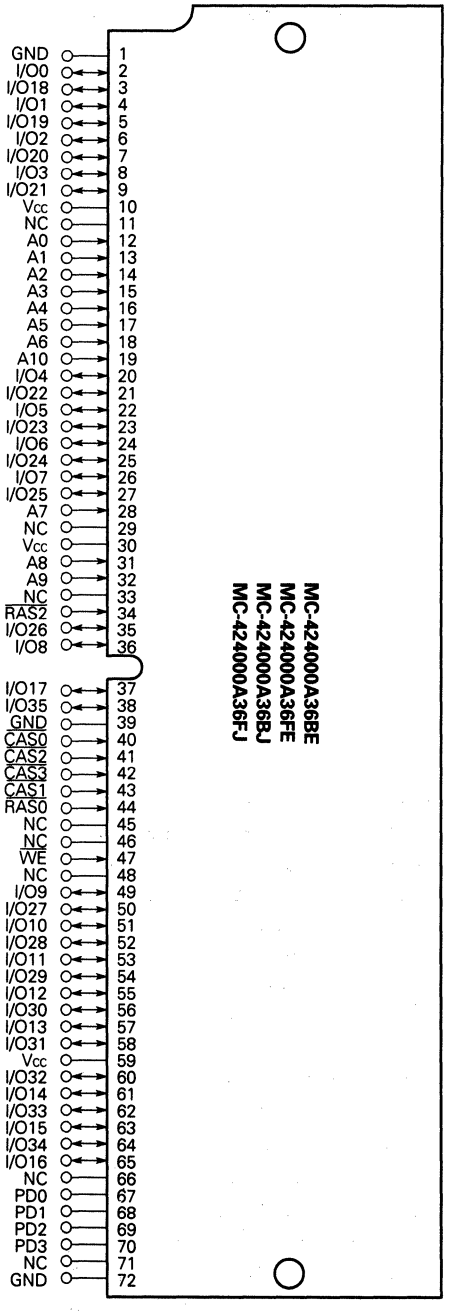
A0 - A10	: Address Inputs
I/O0 - I/O31	: Data Inputs/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$	: Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	: Row Address Strobe
$\overline{WE}$	: Write Enable
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD0	67	GND	GND	GND
PD1	68	NC	NC	NC
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

[MC-424000A36 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



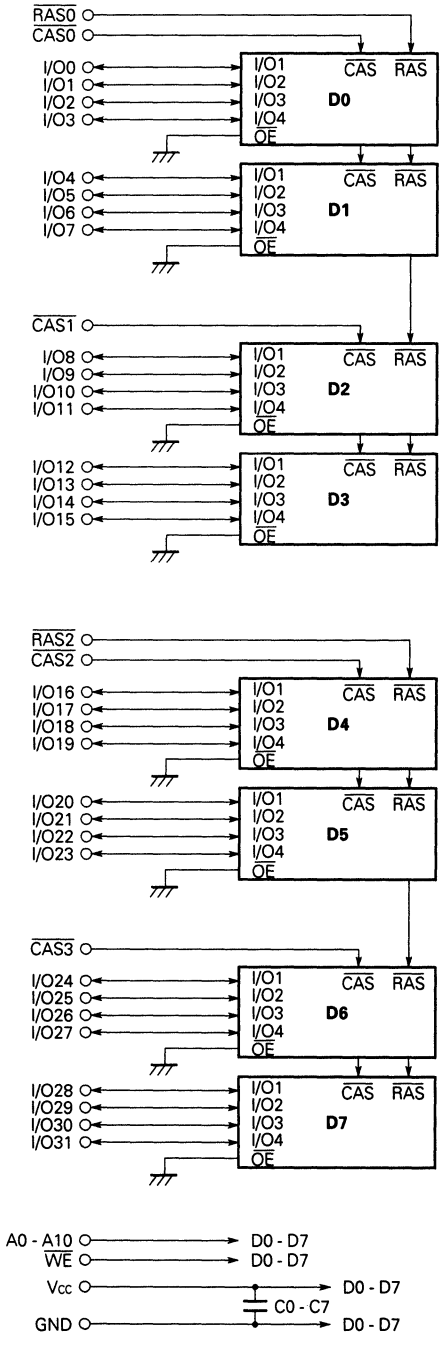
A0 - A10	: Address Inputs
I/O0 - I/O35	: Data Inputs/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$	: Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	: Row Address Strobe
$\overline{WE}$	: Write Enable
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD0	67	GND	GND	GND
PD1	68	NC	NC	NC
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

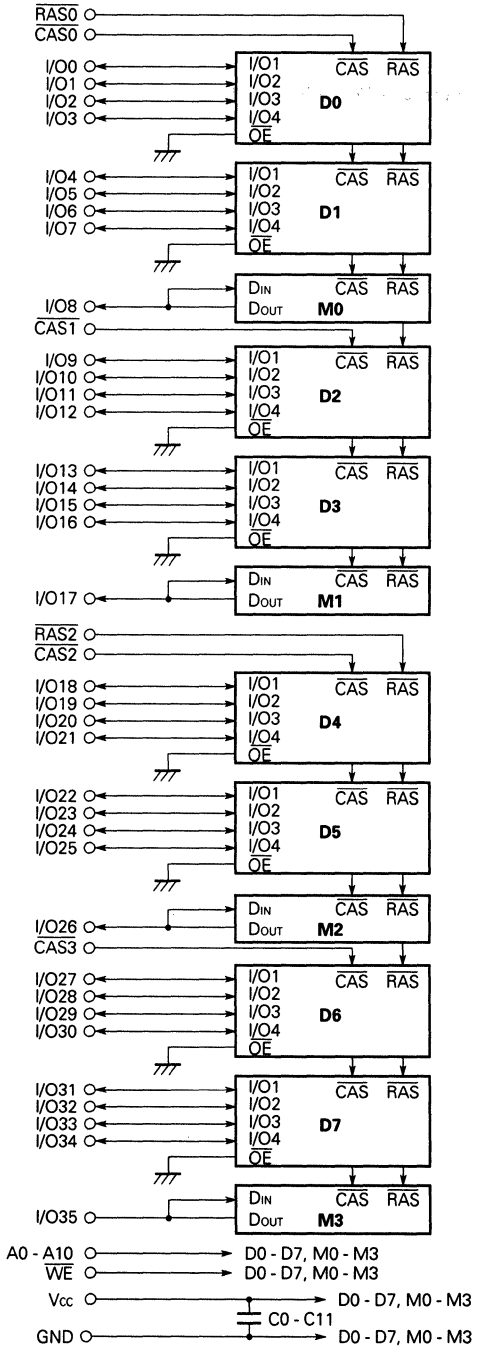
Block Diagram

[MC-424000A32 series]



Remark D0 - D7 : μPD4217400

[MC-424000A36 series]



Remark D0 - D7 : μPD4217400
M0 - M3 : μPD424100

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D	MC-424000A32	8	W
		MC-424000A36	12	
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Ambient temperature	T_a		0		70	°C

Capacitance (T_a = +25 °C, f = 1 MHz)

[MC-424000A32 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			68	pF
	C_{I2}	$\overline{WE}$			76	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			43	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			29	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			17	pF

[MC-424000A36 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			88	pF
	C_{I2}	$\overline{WE}$			104	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			57	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			36	
Data Input/Output capacitance	$C_{I/O1}$	I/O0 - I/O7, I/O9 - I/O16, I/O18 - I/O25, I/O27 - I/O34			17	pF
	$C_{I/O2}$	I/O8, I/O17, I/O26, I/O35			22	

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[MC-424000A32 series]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		880	mA	3, 4, 7
			t_{RAC} = 70 ns		800		
			t_{RAC} = 80 ns		720		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		16	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		8		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		880	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		800		
			t_{RAC} = 80 ns		720		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		560	mA	3, 4, 6
			t_{RAC} = 70 ns		480		
			t_{RAC} = 80 ns		400		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		880	mA	3, 4
			t_{RAC} = 70 ns		800		
			t_{RAC} = 80 ns		720		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

[MC-424000A36 series]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,360	mA	3, 4, 7
			t_{RAC} = 70 ns		1,200		
			t_{RAC} = 80 ns		1,080		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		24	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA		12		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,360	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		1,200		
			t_{RAC} = 80 ns		1,080		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		920	mA	3, 4, 6
			t_{RAC} = 70 ns		800		
			t_{RAC} = 80 ns		680		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,360	mA	3, 4
			t_{RAC} = 70 ns		1,200		
			t_{RAC} = 80 ns		1,080		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		−10	+10	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage	V_{OH}	I_O = −5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

[MC-424000A32 series]

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		18		20	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		32		32		32	ms	

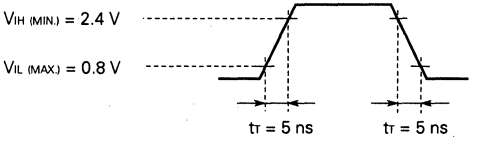
[MC-424000A36 series]

Parameter		Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time		t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time		t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$		t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$		t_{CAC}		15		20		20	ns	10, 11
Access Time Column Address		t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge		t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time		t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time		t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$		t_{OFF}	0	15	0	15	0	20	ns	12
Transition Time (Rise and Fall)		t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time		t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width		t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)		t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time		t_{RSH}	20		20		20		ns	
$\overline{CAS}$ Pulse Width		t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time		t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time		t_{RCD}	20	40	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	10		10		10		ns	13
$\overline{CAS}$ Precharge Time		t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)		t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time		t_{RPC}	10		10		10		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		t_{RHCP}	35		40		45		ns	
Row Address Setup Time		t_{ASR}	0		0		0		ns	
Row Address Hold Time		t_{RAH}	10		10		12		ns	
Column Address Setup Time		t_{ASC}	0		0		0		ns	
Column Address Hold Time		t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$		t_{RAL}	30		35		40		ns	
Read Command Setup Time		t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$		t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$		t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$		t_{WCH}	15		15		15		ns	15
Data-in Setup Time		t_{DS}	0		0		0		ns	16
Data-in Hold Time		t_{DH}	15		15		15		ns	16
Write Command Setup Time		t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		t_{CSR}	10		10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time		t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time		t_{WHR}	15		15		15		ns	
Refresh Time	Distributed refresh	t_{REF}		32		32		32	ms	
	Burst refresh			16		16		16	ms	

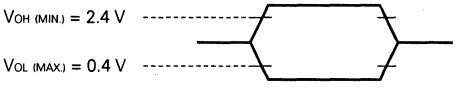
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{RAC} (MAX.)	t_{RAC} (MAX.)
$t_{RAD} > t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{AA} (MAX.)	$t_{RAD} + t_{AA}$ (MAX.)
$t_{RCD} > t_{RCD}$ (MAX.)	t_{CAC} (MAX.)	$t_{RCD} + t_{CAC}$ (MAX.)

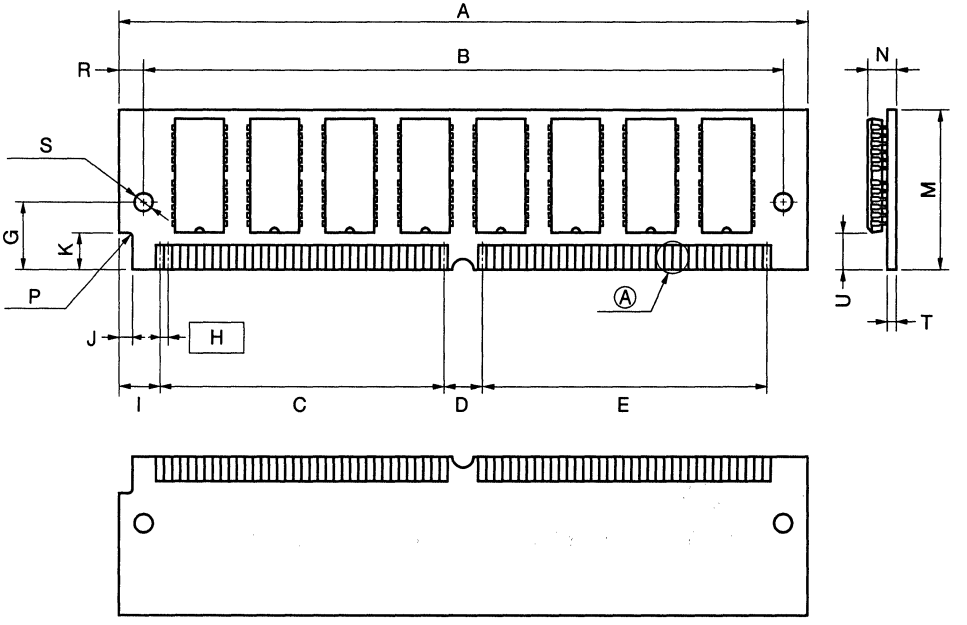
    t_{RAD} (MAX.) and t_{RCD} (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}$ (MAX.) and $t_{RCD} \geq t_{RCD}$ (MAX.) will not cause any operation problems.
11. Loading conditions are 2 TTLs and 100 pF.
12. t_{OFF} (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. t_{CRP} (MIN.) requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either t_{RCH} (MIN.) or t_{RRH} (MIN.) should be met in read cycles.
15. In early write cycles, t_{WCH} (MIN.) should be met.
16. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

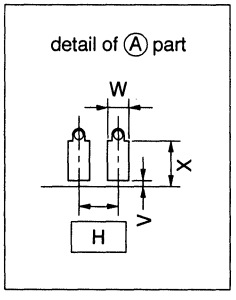
Timing Chart
Please refer to Timing Chart 10, page 479.

Package Drawings

[MC-424000A32B, 424000A32F]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



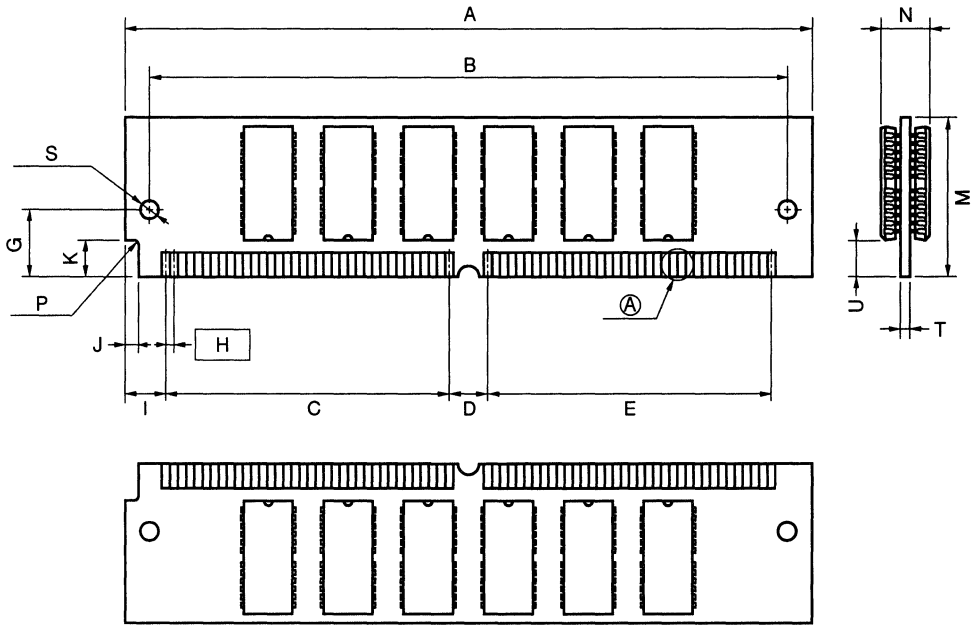


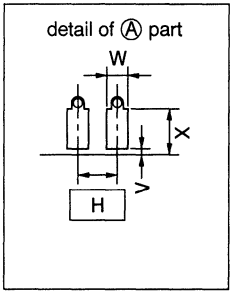
ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19±0.13	$3.984^{+0.005}_{-0.006}$
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
P	R1.57	R0.062
R	3.38±0.13	$0.133^{+0.006}_{-0.005}$
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	5.5 MIN.	0.216 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72B-50A54

[MC-424000A36BE, 424000A36FE]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



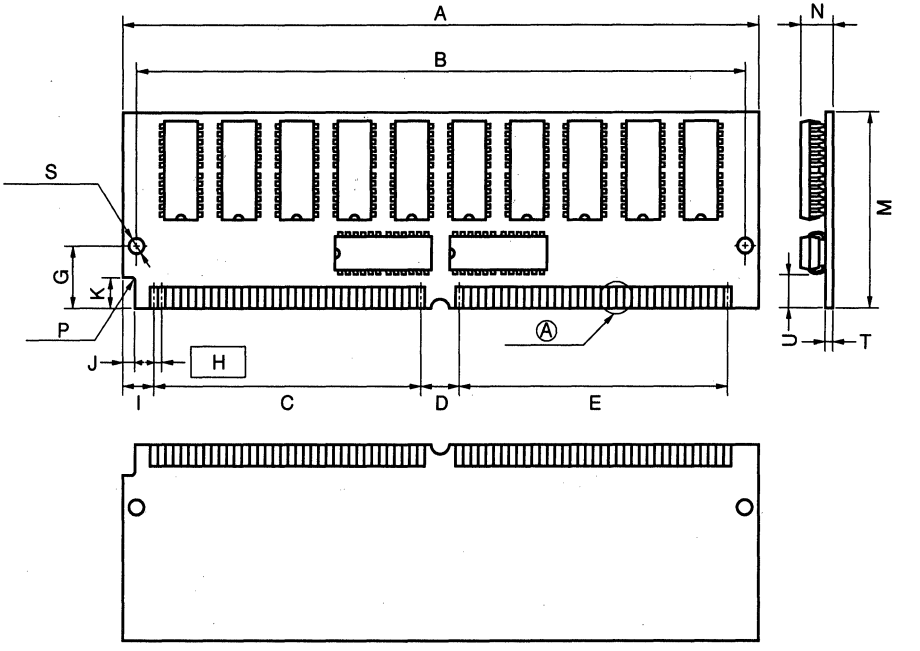


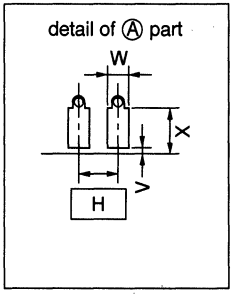
ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	5.08 MIN.	0.200 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.

M72B-50A47

[MC-424000A36BJ, 424000A36FJ]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	31.75	1.250
N	5.08 MAX.	0.200 MAX.
P	R1.57	R0.062
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	3.17 MIN.	0.124 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.

M72B-50A51-1

NEC

MOS INTEGRATED CIRCUIT

MC-428000A32, 428000A36 SERIES

8 M-WORD BY 32-BIT, 8 M-WORD BY 36-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-428000A32 series is a 8,388,608 words by 32 bits dynamic RAM module on which 16 pieces of 16 M DRAM: μPD4217400 are assembled.

The MC-428000A36 series is a 8,388,608 words by 36 bits dynamic RAM module on which 16 pieces of 16 M DRAM: μPD4217400 and 8 pieces of 4 M DRAM: μPD424100 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 8,388,608 words by 32 bits organization (MC-428000A32 series)
- 8,388,608 words by 36 bits organization (MC-428000A36 series)
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-428000A32-60	60 ns	110 ns	5,170 mW	88 mW (CMOS level input)
MC-428000A32-70	70 ns	130 ns	4,730 mW	
MC-428000A32-80	80 ns	150 ns	4,290 mW	
MC-428000A36-60	60 ns	110 ns	7,810 mW	132 mW (CMOS level input)
MC-428000A36-70	70 ns	130 ns	6,930 mW	
MC-428000A36-80	80 ns	150 ns	6,270 mW	

- 2,048 refresh cycles/32 ms
- 2,048 refresh cycles/16 ms (MC-428000A36 burst refesh)
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ±0.5 V power supply
- Access time can be distinguished with characteristics of PD-pins (PD0 to PD3)

Document No. IC-3455 (Japan)

Ordering Information

[MC-428000A32 series]

Part number	Access time (MAX.)	Package	Mounted devices
MC-428000A32B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	16 pieces of μPD4217400LA (300 mil SOJ) [Double side]
MC-428000A32B-70	70 ns		
MC-428000A32B-80	80 ns		
MC-428000A32F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-428000A32F-70	70 ns		
MC-428000A32F-80	80 ns		

[MC-428000A36 series]

Part number	Access time (MAX.)	Package	Mounted devices
MC-428000A36BJ-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Solder coating (HAL)	16 pieces of μPD4217400LA (300 mil SOJ) 8 pieces of μPD424100LA (300 mil SOJ) [Double side]
MC-428000A36BJ-70	70 ns		
MC-428000A36BJ-80	80 ns		
MC-428000A36FJ-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector: Gold plating	
MC-428000A36FJ-70	70 ns		
MC-428000A36FJ-80	80 ns		

Quality Grade

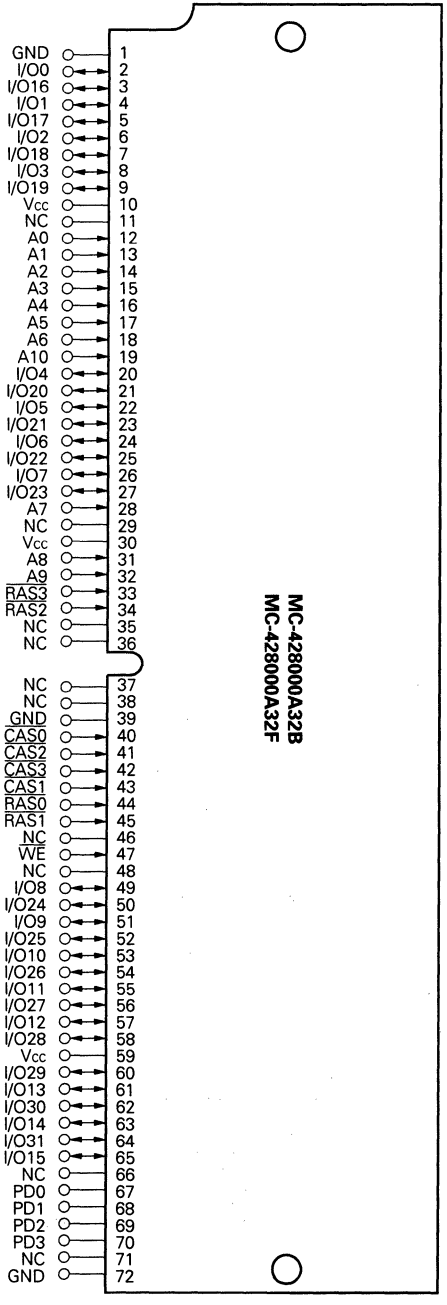
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configurations

[MC-428000A32 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



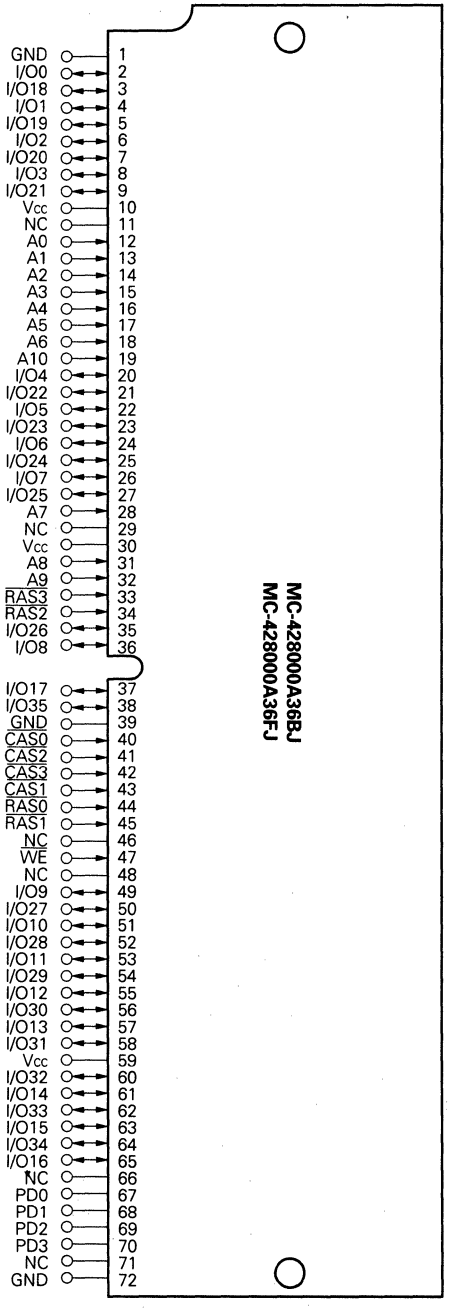
A0 - A10	: Address Inputs
I/O0 - I/O31	: Data Inputs/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$	: Column Address Strobe
$\overline{RAS0}$ - $\overline{RAS3}$	: Row Address Strobe
$\overline{WE}$	: Write Enable
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD0	67	NC	NC	NC
PD1	68	GND	GND	GND
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

[MC-428000A36 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder coating, Gold plating)



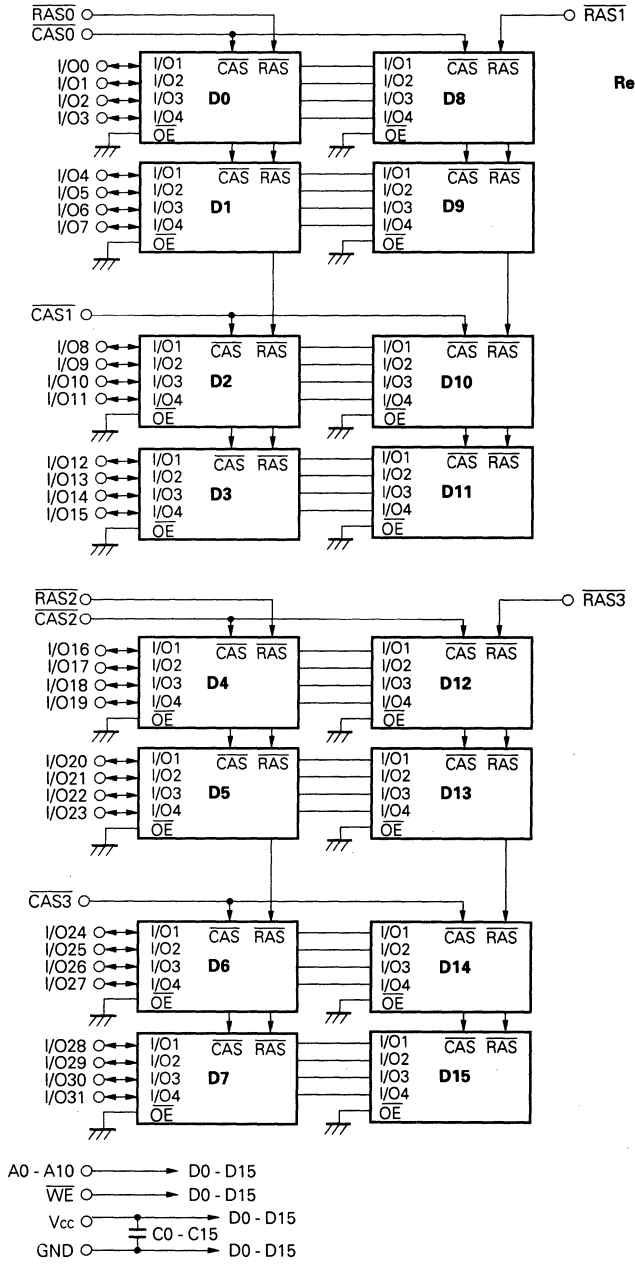
A0 - A10	: Address Inputs
I/O0 - I/O35	: Data Inputs/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$	: Column Address Strobe
$\overline{RAS0}$ - $\overline{RAS3}$	: Row Address Strobe
$\overline{WE}$	: Write Enable
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD0 to PD3) depends on access time.

Pin Name	Pin No.	Access Time		
		60 ns	70 ns	80 ns
PD0	67	NC	NC	NC
PD1	68	GND	GND	GND
PD2	69	NC	GND	NC
PD3	70	NC	NC	GND

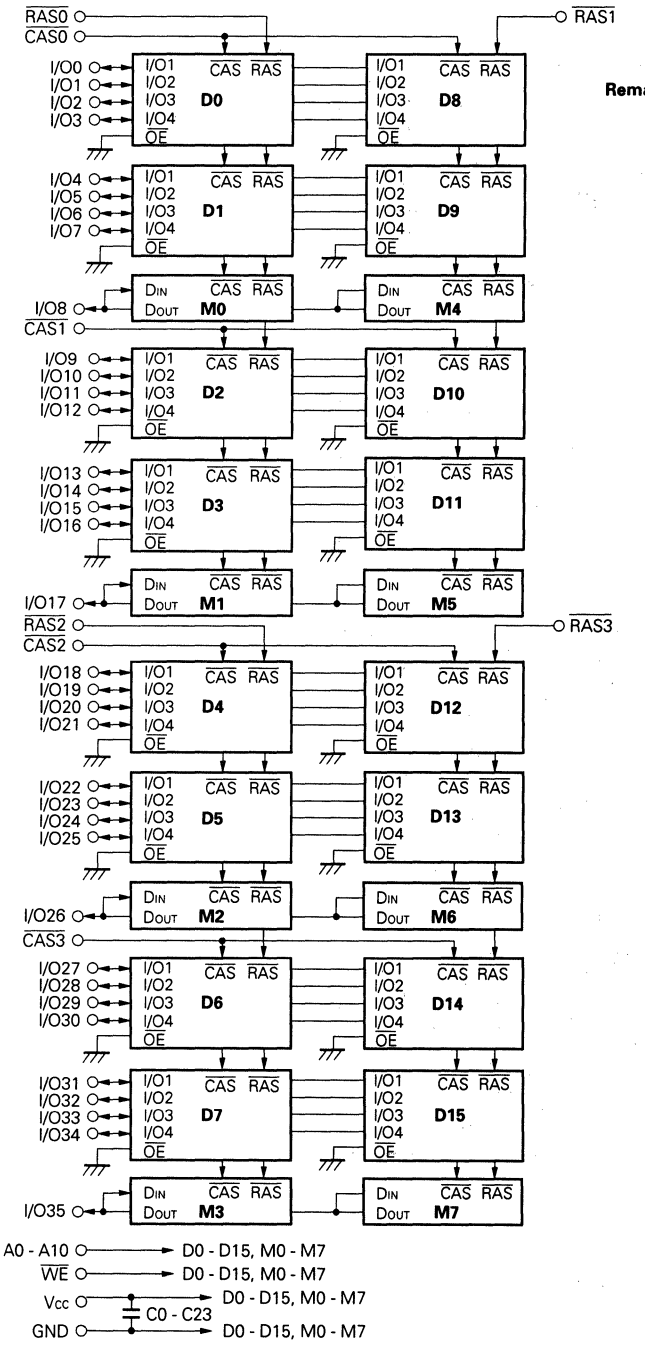
Block Diagrams

[MC-428000A32 series]



Remark D0 - D15: μPD4217400

[MC-428000A36 series]



Remark D0 - D15: μPD4217400
M0 - M7: μPD424100

Electrical Specifications [Notes 1, 2]

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D	MC-428000A32	16	W
		MC-428000A36	24	
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

[MC-428000A32 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			121	pF
	C_{I2}	$\overline{WE}$			137	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS3}$			48	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			48	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			29	pF

[MC-428000A36 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A10			161	pF
	C_{I2}	$\overline{WE}$			193	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS3}$			62	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			62	
Data Input/Output capacitance	$C_{I/O1}$	I/O0 - I/O7, I/O9 - I/O16, I/O18 - I/O25, I/O27 - I/O34			29	pF
	$C_{I/O2}$	I/O8, I/O17, I/O26, I/O35			39	

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[MC-428000A32 series]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		940	mA	3, 4, 7
			t_{RAC} = 70 ns		860		
			t_{RAC} = 80 ns		780		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		32	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		16		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		940	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		860		
			t_{RAC} = 80 ns		780		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		620	mA	3, 4, 6
			t_{RAC} = 70 ns		540		
			t_{RAC} = 80 ns		460		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		940	mA	3, 4
			t_{RAC} = 70 ns		860		
			t_{RAC} = 80 ns		780		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

[MC-428000A36 series]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,420	mA	3, 4, 7
			t_{RAC} = 70 ns		1,260		
			t_{RAC} = 80 ns		1,140		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		48	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V	I_O = 0 mA		24		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,420	mA	3, 4, 5, 7
			t_{RAC} = 70 ns		1,260		
			t_{RAC} = 80 ns		1,140		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		980	mA	3, 4, 6
			t_{RAC} = 70 ns		860		
			t_{RAC} = 80 ns		740		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1,420	mA	3, 4
			t_{RAC} = 70 ns		1,260		
			t_{RAC} = 80 ns		1,140		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

[MC-428000A32 series]

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time	t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$	t_{CAC}		15		18		20	ns	10, 11
Access Time Column Address	t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	12
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		10		15		ns	15
Data-in Setup Time	t_{DS}	0		0		0		ns	16
Data-in Hold Time	t_{DH}	10		15		15		ns	16
Write Command Setup Time	t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		ns	
Refresh Time	t_{REF}		32		32		32	ms	

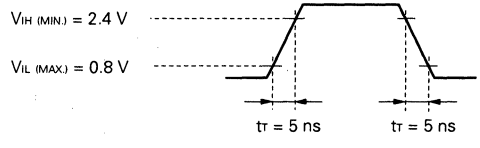
[MC-428000A36 series]

Parameter		Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time		t_{RC}	110		130		150		ns	
Fast Page Mode Cycle Time		t_{PC}	40		45		50		ns	
Access Time from $\overline{RAS}$		t_{RAC}		60		70		80	ns	10, 11
Access Time from $\overline{CAS}$		t_{CAC}		15		20		20	ns	10, 11
Access Time Column Address		t_{AA}		30		35		40	ns	10, 11
Access Time from $\overline{CAS}$ Precharge		t_{ACP}		35		40		45	ns	11
$\overline{RAS}$ to Column Address Delay Time		t_{RAD}	15	30	15	35	17	40	ns	10
$\overline{CAS}$ to Data Setup Time		t_{CLZ}	0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$		t_{OFF}	0	15	0	15	0	20	ns	12
Transition Time (Rise and Fall)		t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time		t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width		t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)		t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{RAS}$ Hold Time		t_{RSH}	20		20		20		ns	
$\overline{CAS}$ Pulse Width		t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time		t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time		t_{RCD}	20	40	20	50	25	60	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	10		10		10		ns	13
$\overline{CAS}$ Precharge Time		t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)		t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time		t_{RPC}	10		10		10		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		t_{RHCP}	35		40		45		ns	
Row Address Setup Time		t_{ASR}	0		0		0		ns	
Row Address Hold Time		t_{RAH}	10		10		12		ns	
Column Address Setup Time		t_{ASC}	0		0		0		ns	
Column Address Hold Time		t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$		t_{RAL}	30		35		40		ns	
Read Command Setup Time		t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$		t_{RRH}	0		0		0		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$		t_{RCH}	0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$		t_{WCH}	15		15		15		ns	15
Data-in Setup Time		t_{DS}	0		0		0		ns	16
Data-in Hold Time		t_{DH}	15		15		15		ns	16
Write Command Setup Time		t_{WCS}	0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		t_{CSR}	10		10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		t_{CHR}	10		10		10		ns	
$\overline{WE}$ Setup Time		t_{WSR}	10		10		10		ns	
$\overline{WE}$ Hold Time		t_{WHR}	15		15		15		ns	
Refresh Time	Distributed refresh	t_{REF}		32		32		32	ms	
	Burst refresh			16		16		16	ms	

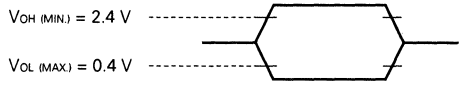
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL}$ (MAX.) and $\overline{CAS} \geq V_{IH}$ (MIN.).
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

   (1) Input timing specification



   (2) Output timing specification



10. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{RAC} (MAX.)	t_{RAC} (MAX.)
$t_{RAD} > t_{RAD}$ (MAX.) and $t_{RCD} \leq t_{RCD}$ (MAX.)	t_{AA} (MAX.)	$t_{RAD} + t_{AA}$ (MAX.)
$t_{RCD} > t_{RCD}$ (MAX.)	t_{CAC} (MAX.)	$t_{RCD} + t_{CAC}$ (MAX.)

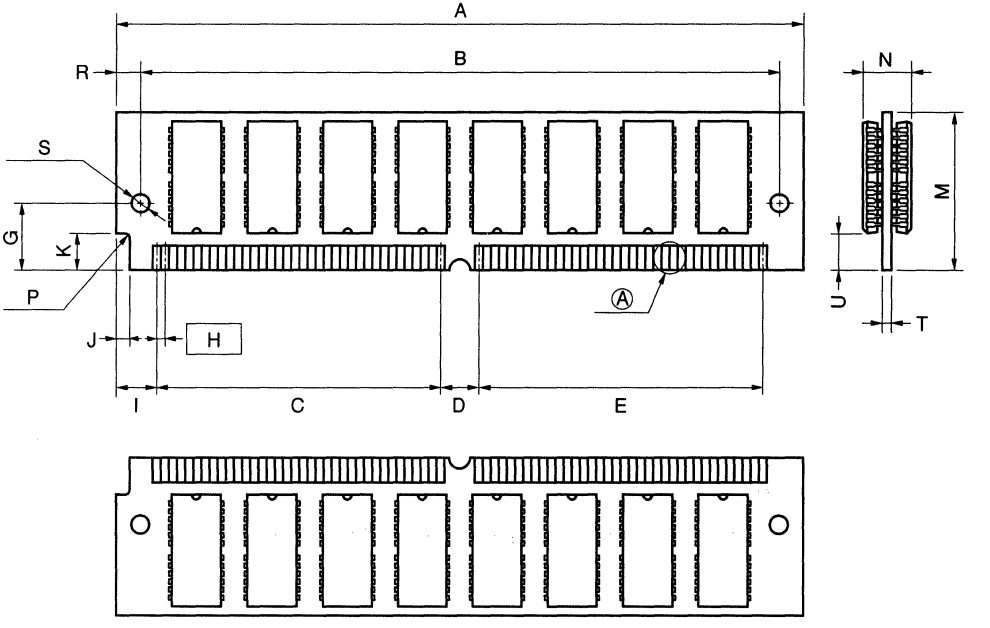
    t_{RAD} (MAX.) and t_{RCD} (MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD}$ (MAX.) and $t_{RCD} \geq t_{RCD}$ (MAX.) will not cause any operation problems.
11. Loading conditions are 2 TTLs and 100 pF.
12. t_{OFF} (MAX.) defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. t_{CRP} (MIN.) requirements should be applied to $\overline{RAS}/\overline{CAS}$ cycles.
14. Either t_{RCH} (MIN.) or t_{RRH} (MIN.) should be met in read cycles.
15. In early write cycles, t_{WCH} (MIN.) should be met.
16. t_{DS} (MIN.) and t_{DH} (MIN.) are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

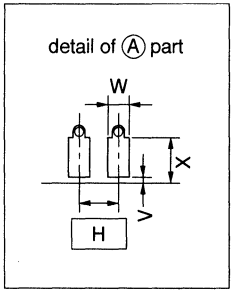
Timing Chart
Please refer to Timing Chart 10, page 479.

Package Drawings

[MC-428000A32B, 428000A32F]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



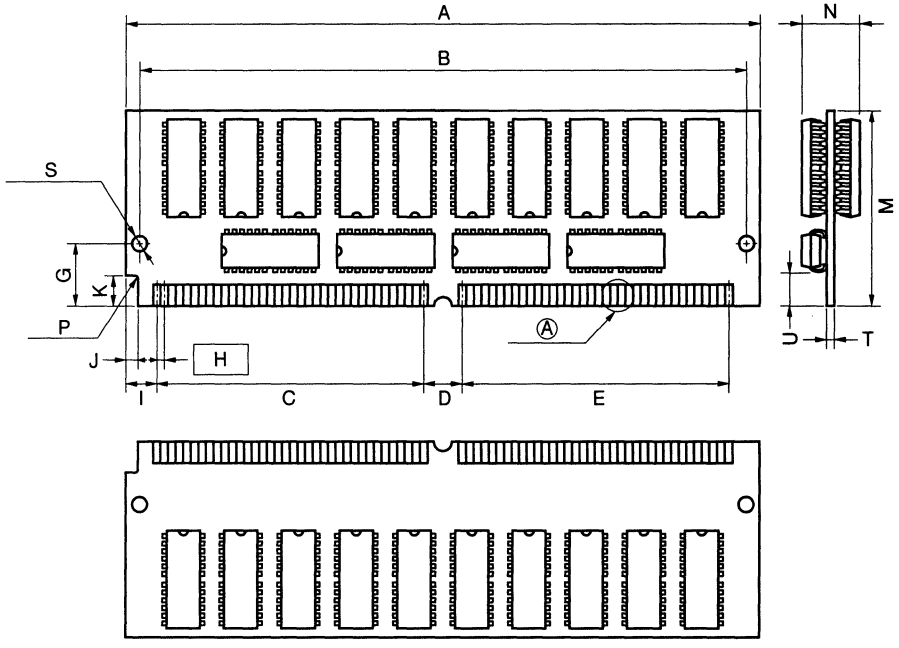


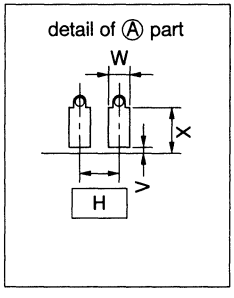
ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19±0.13	$3.984^{+0.005}_{-0.006}$
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
R	3.38±0.13	$0.133^{+0.006}_{-0.005}$
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	5.5 MIN.	0.216 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72B-50A55

[MC-428000A36BJ, 428000A36FJ]

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



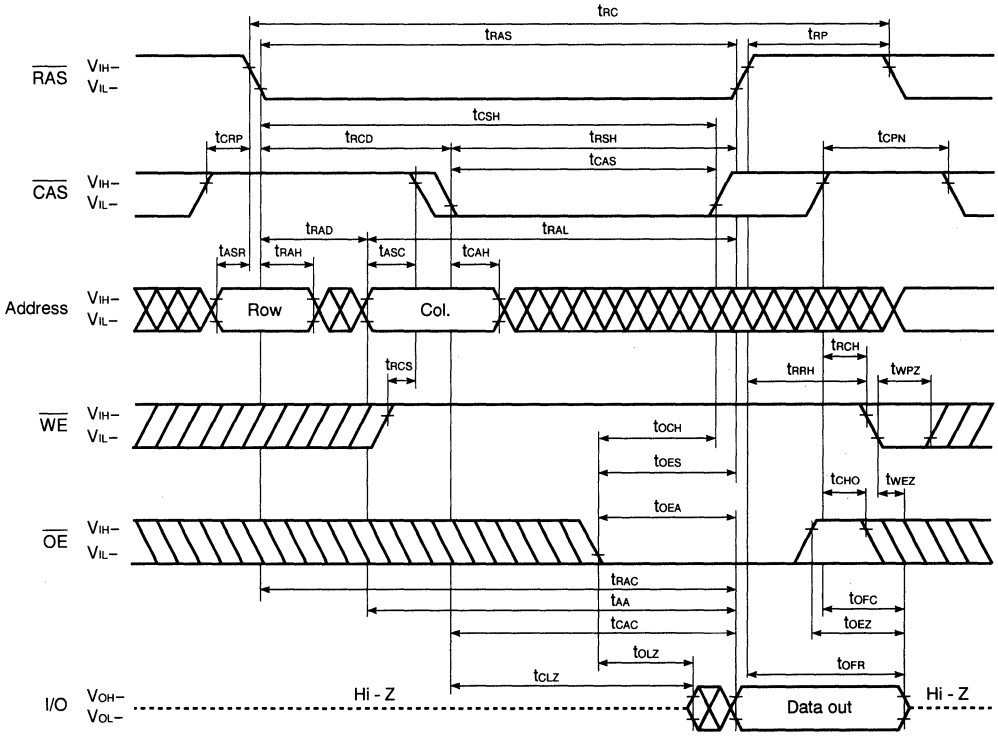


ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	31.75	1.250
N	9.0 MAX.	0.355 MAX.
P	R1.57	R0.062
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	3.17 MIN.	0.124 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	3.15 MIN.	0.124 MIN.

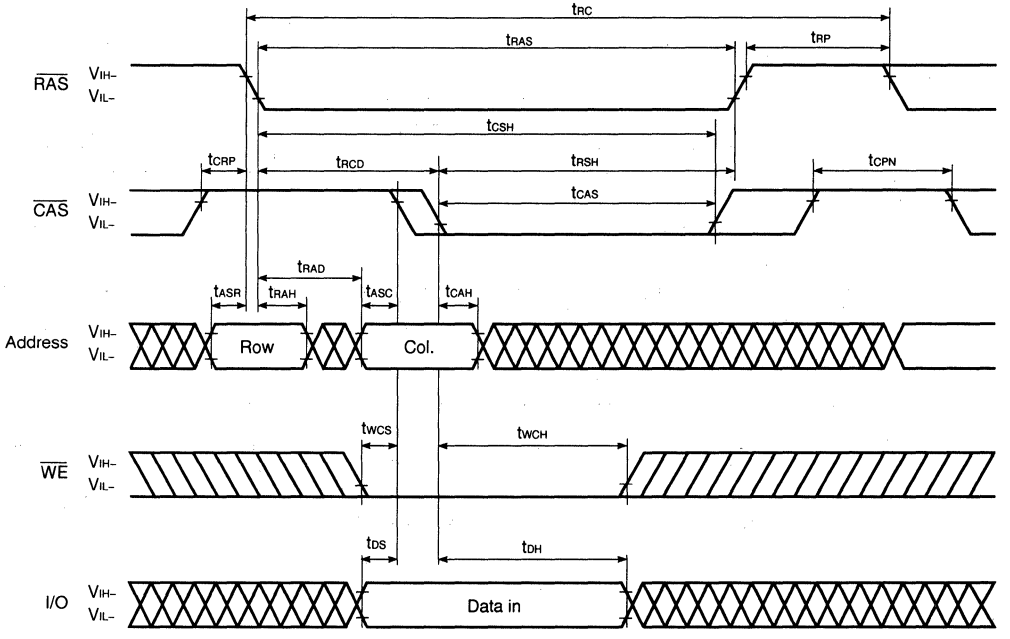
M72B-50A50

Timing Chart 1

Read Cycle

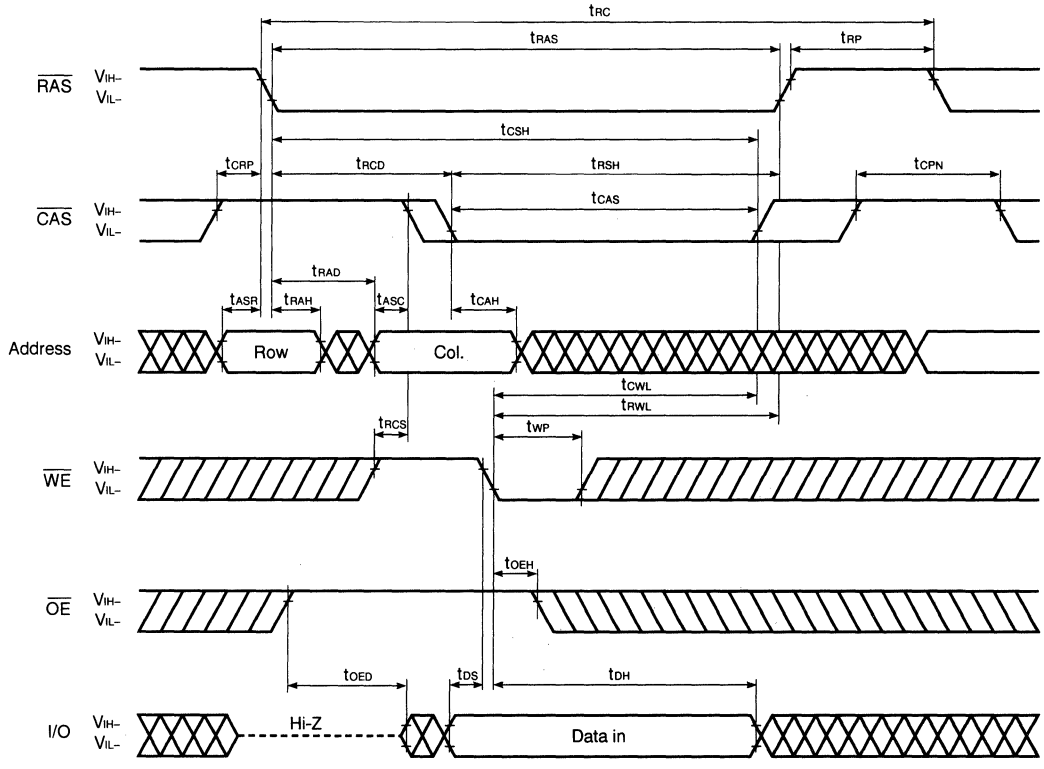

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCAS
tCPN
CAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
tWPZ
WE
tOCH
tOES
tCHO
tWEZ
tOEA
OE
tRAC
tAA
tOFC
tCAC
tOEZ
tOLZ
tOFR
tCLZ
I/O
VOH–
VOL–
Hi - Z
Data out
Hi - Z

Early Write Cycle

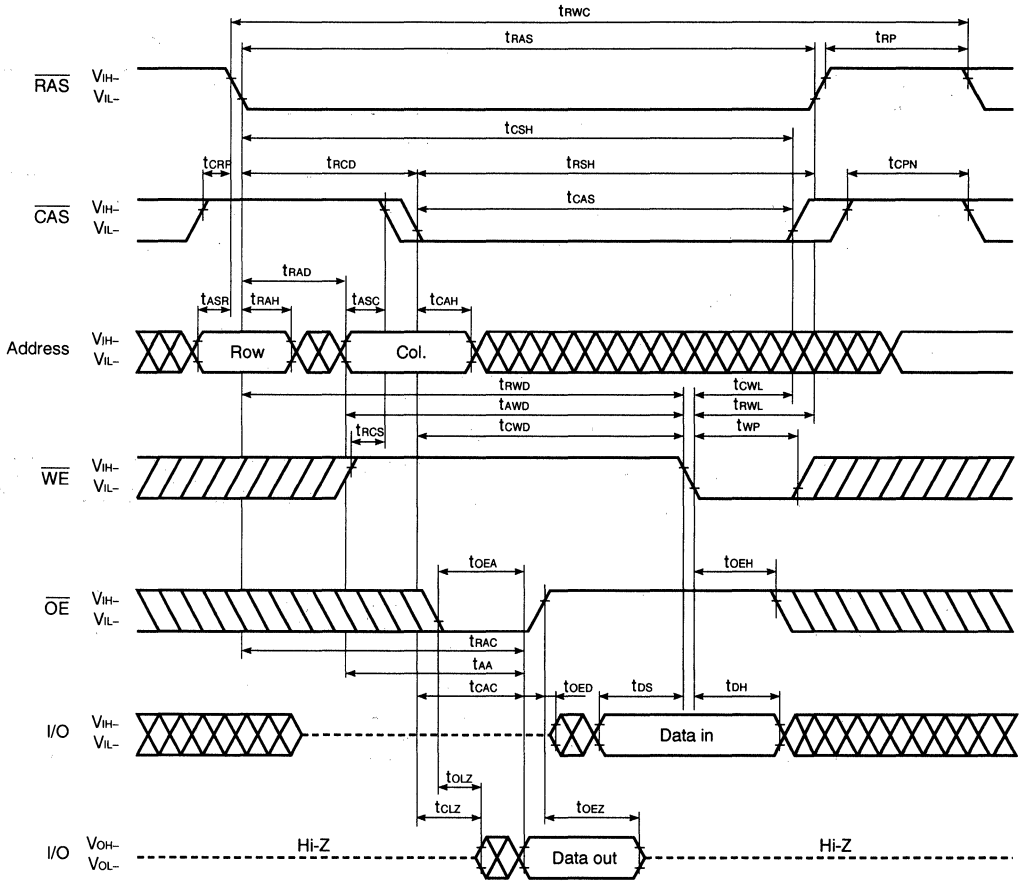


Remark $\overline{OE}$: Don't care

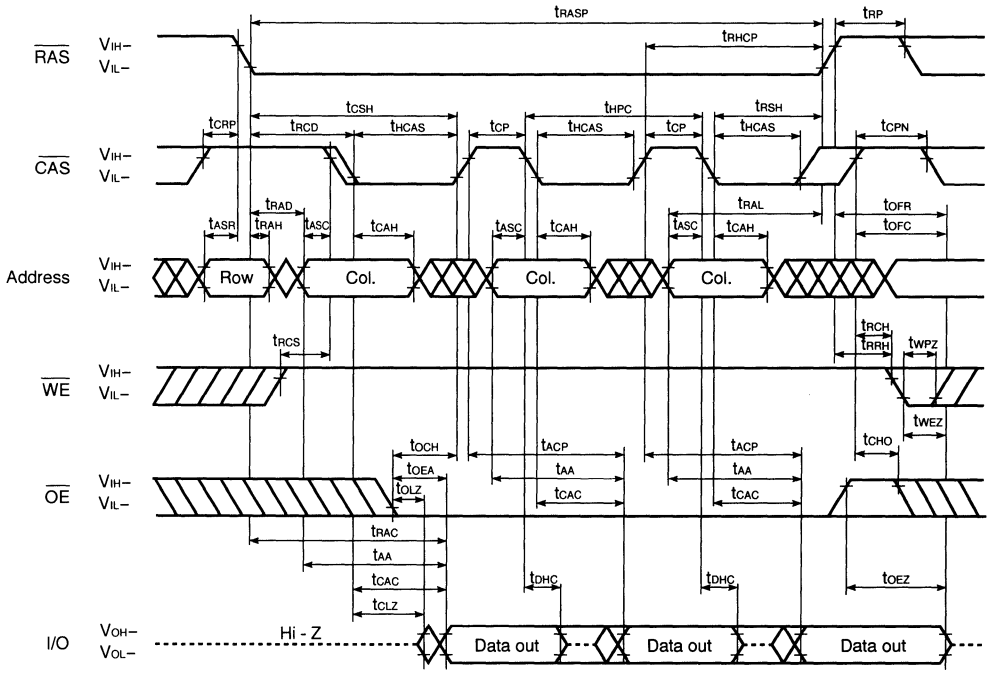
Late Write Cycle



Read Modify Write Cycle

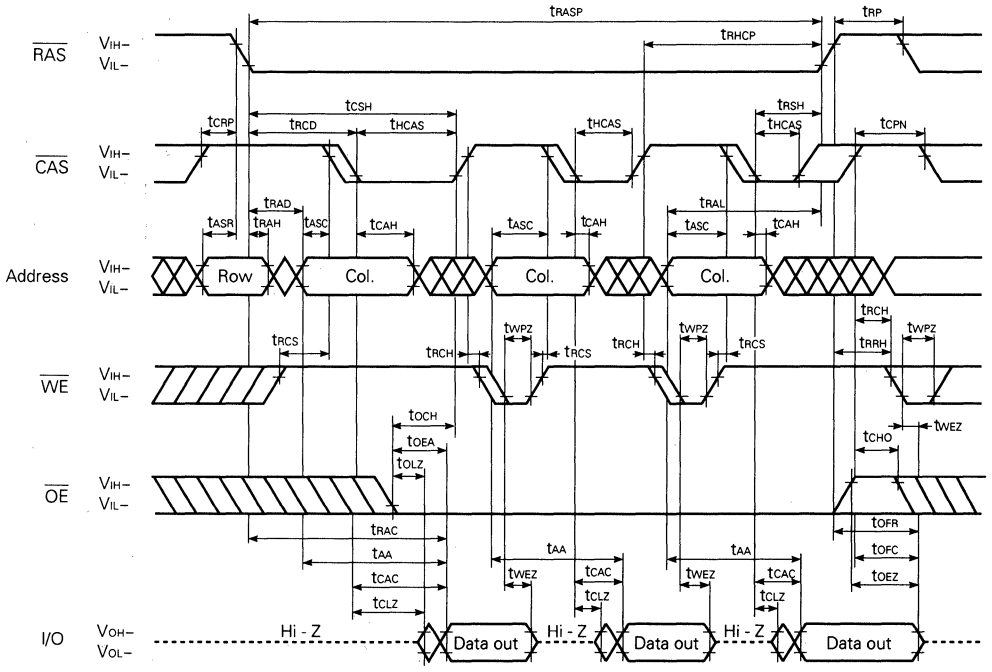


Hyper Page Mode (EDO) Read Cycle



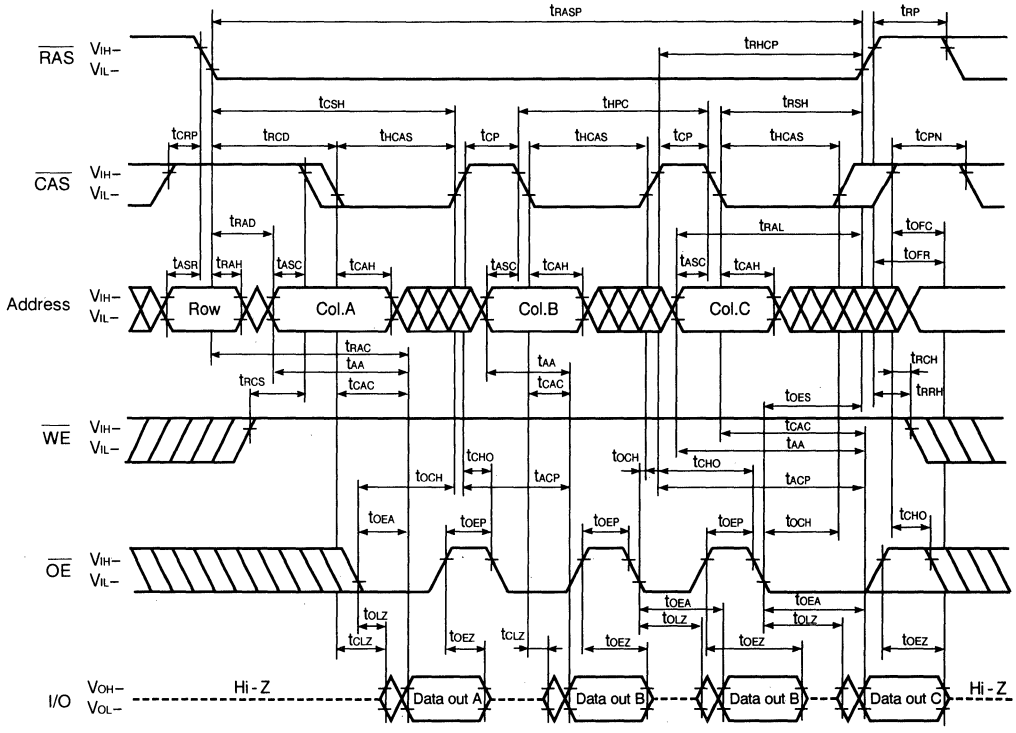
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{WE}$ Control)



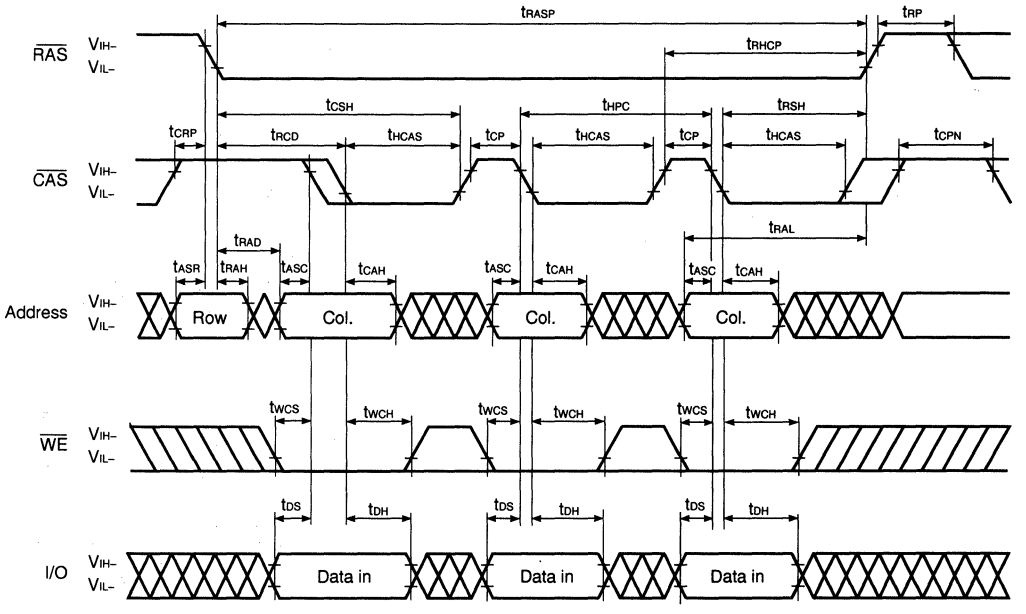
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{OE}$ Control)



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

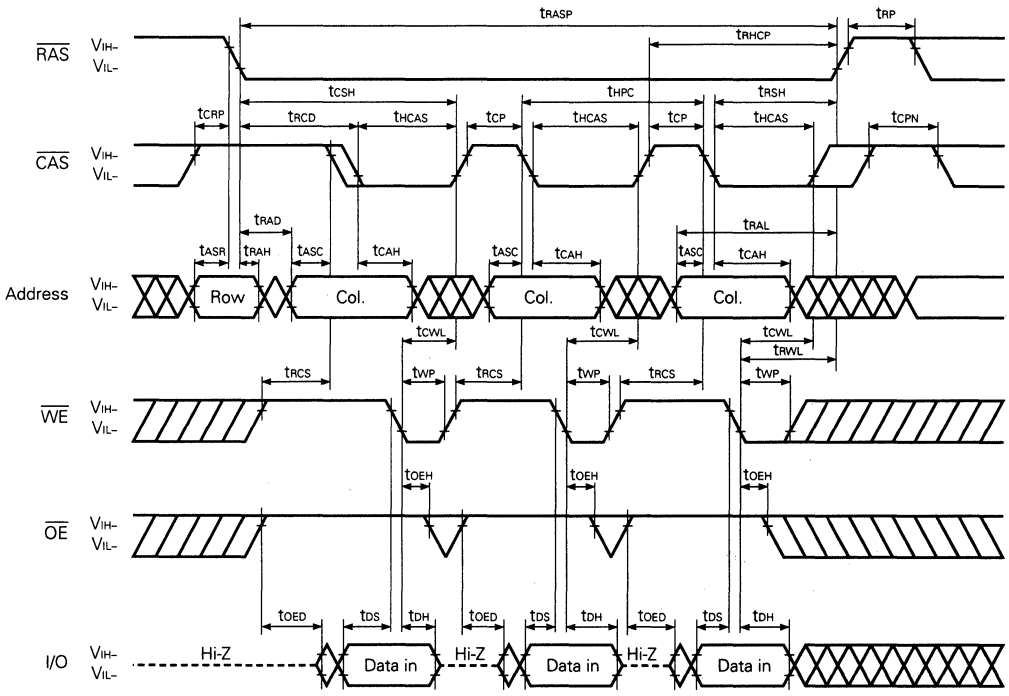
Hyper Page Mode (EDO) Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

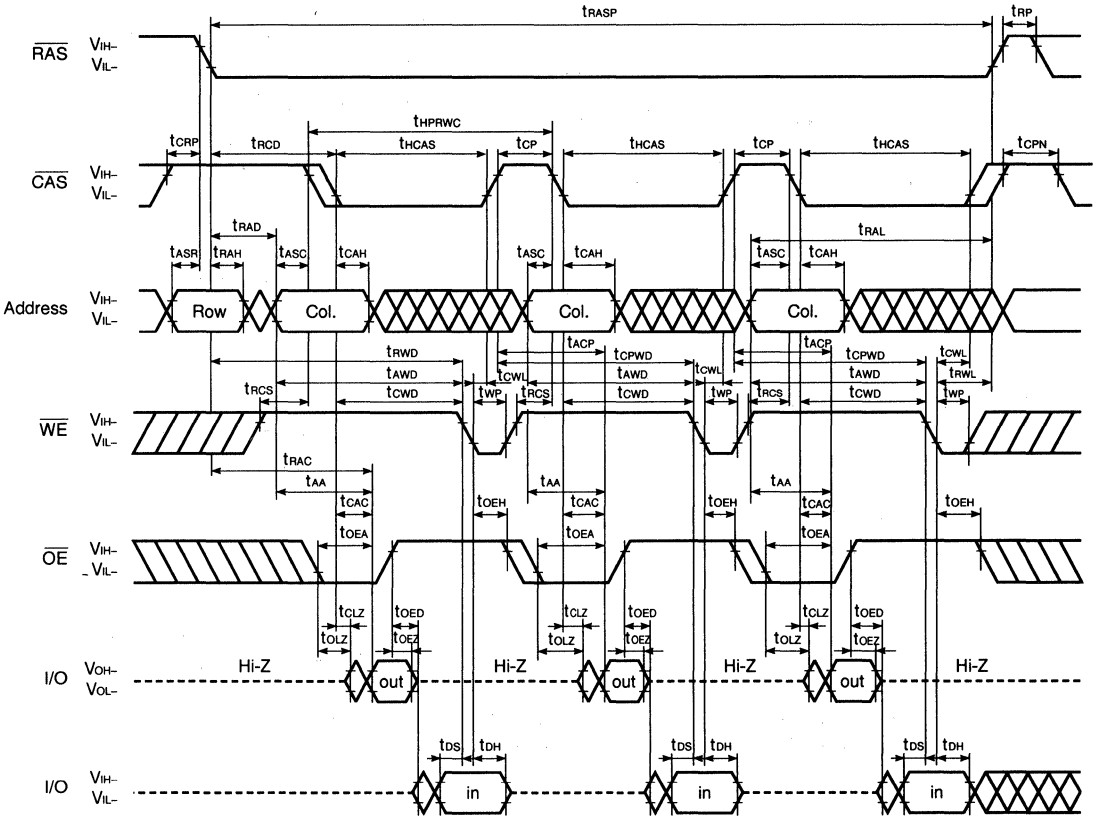
2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Late Write Cycle



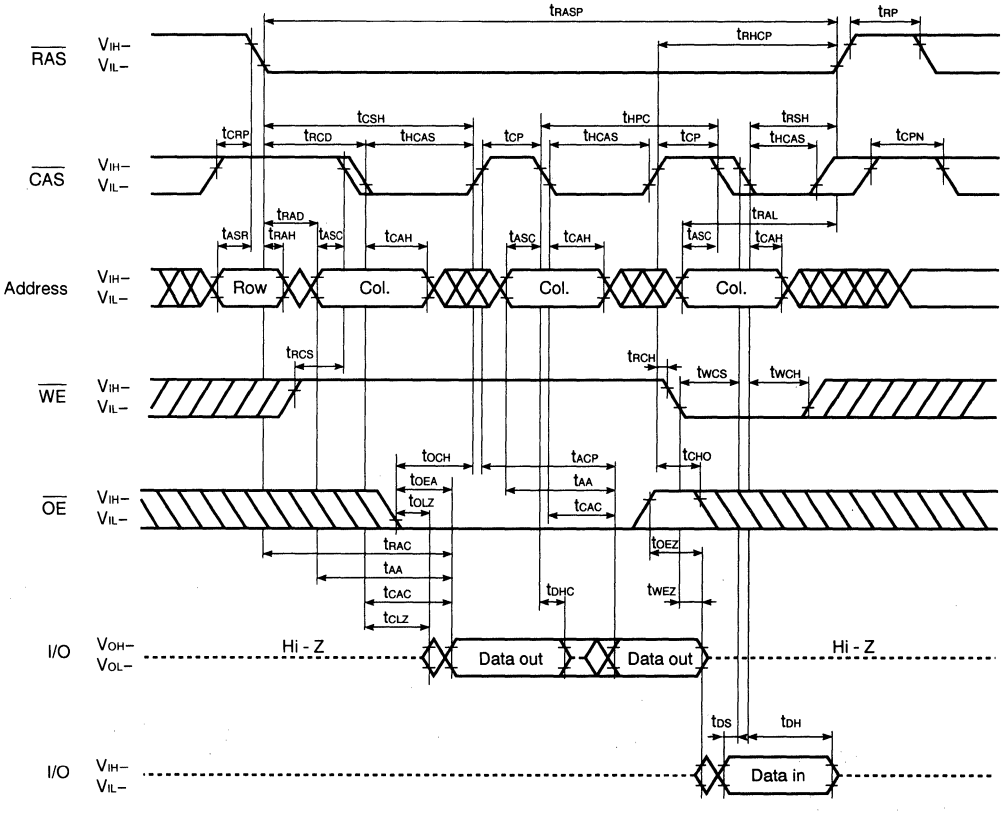
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Modify Write Cycle



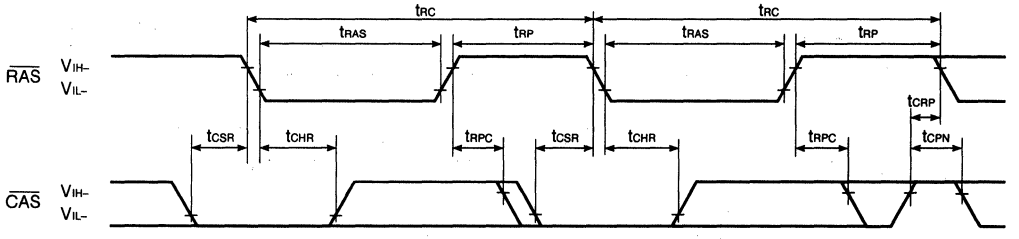
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read and Write Cycle



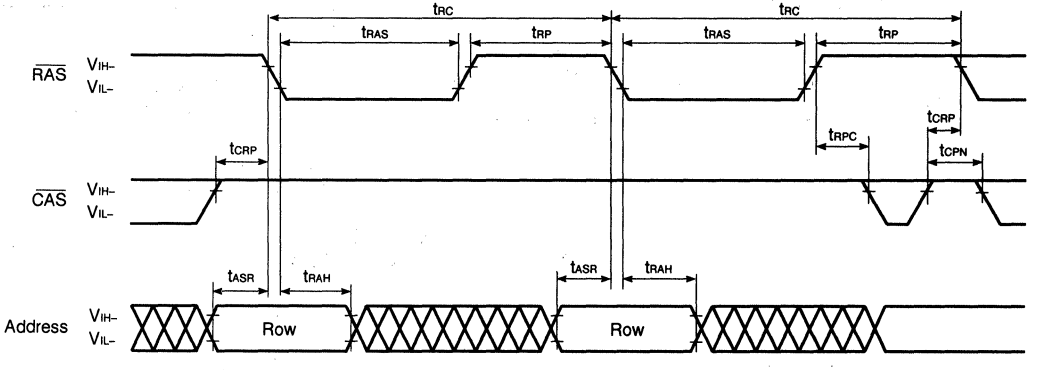
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



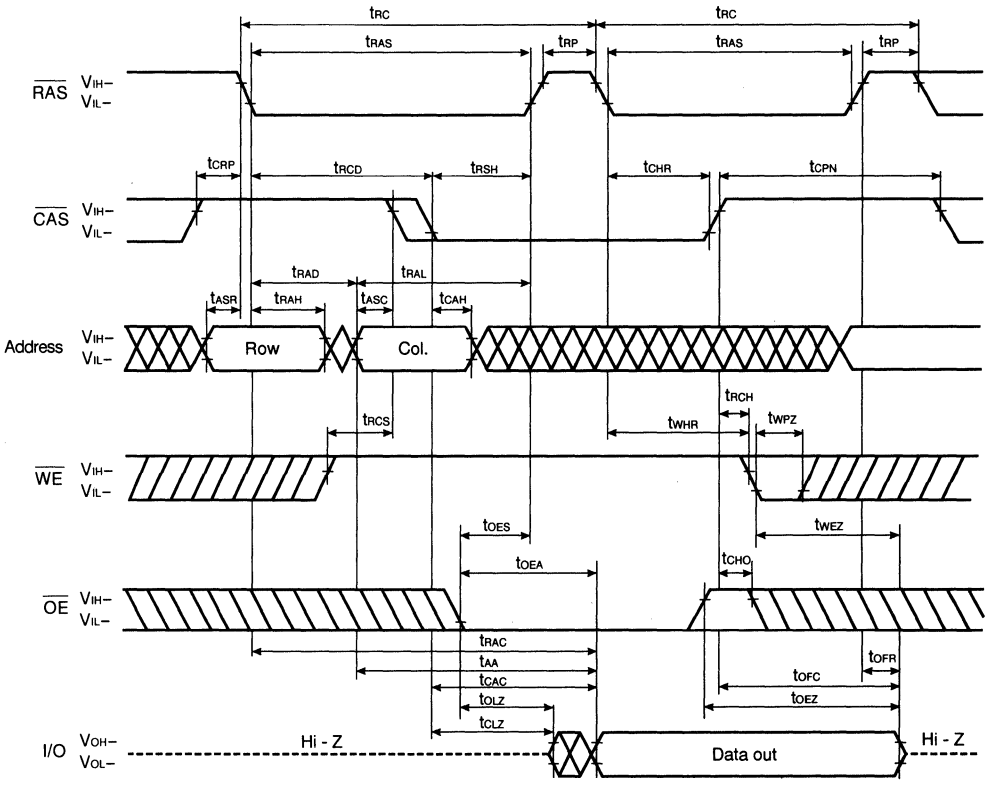
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

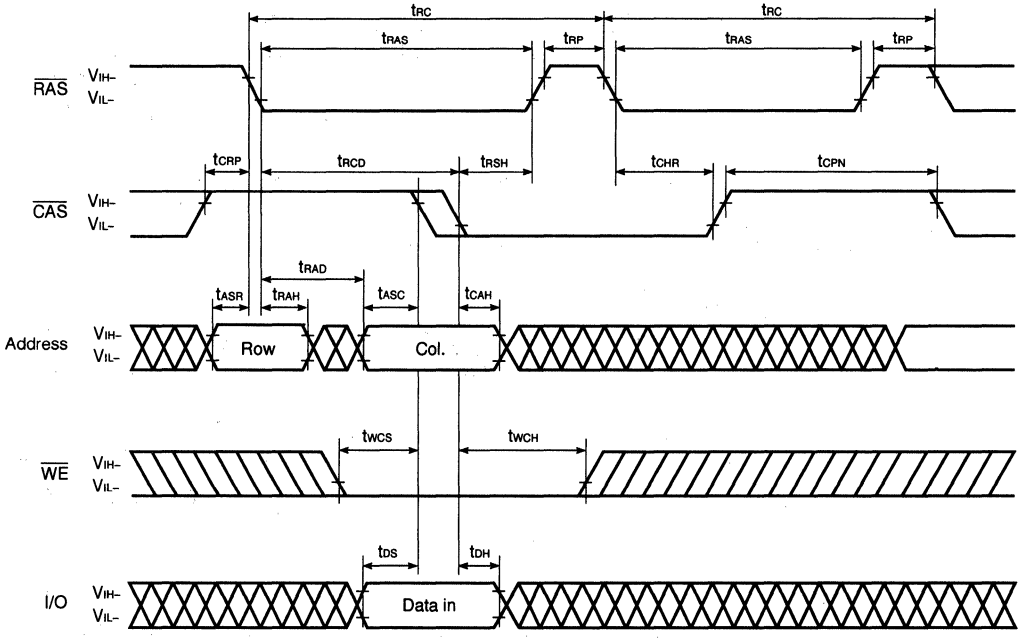


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



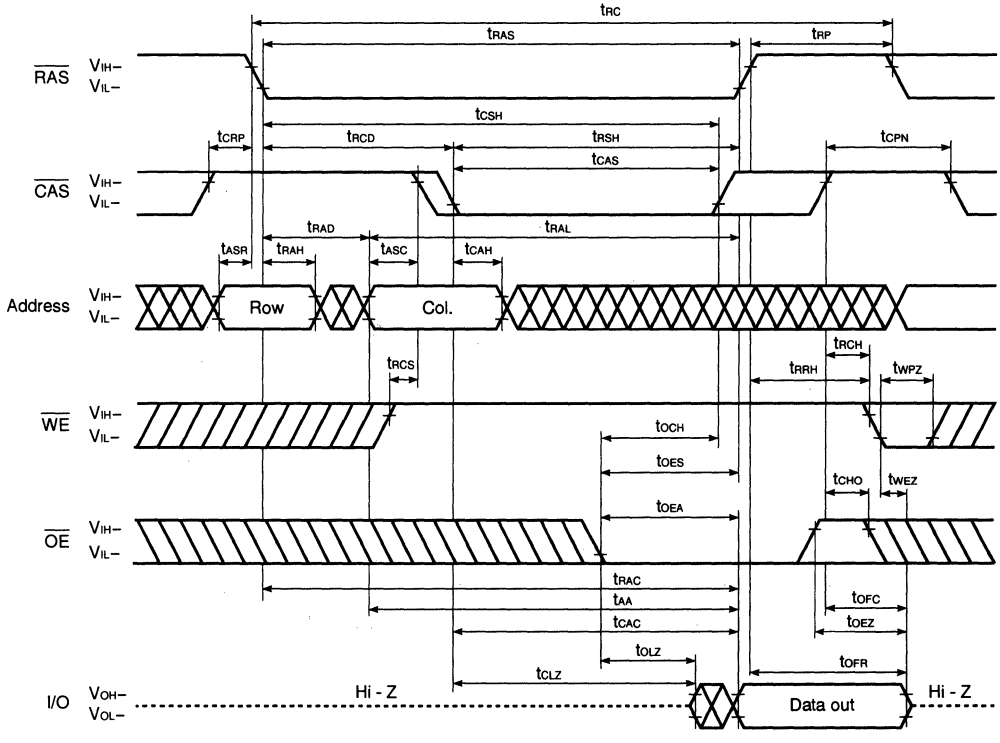
Hidden Refresh Cycle (Write)



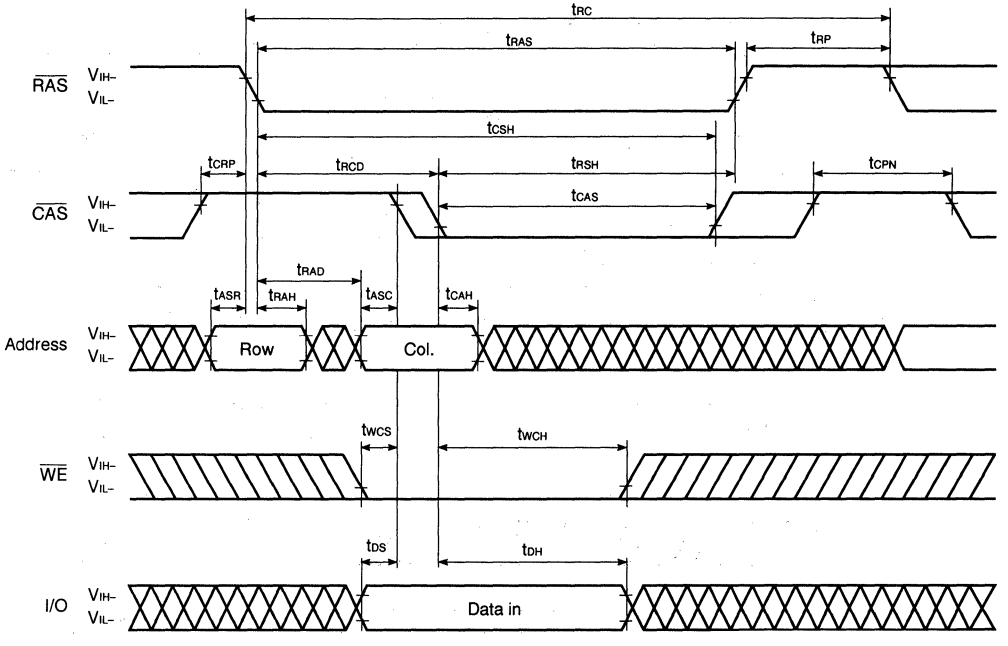
Remark $\overline{OE}$: Don't care

Timing Chart 2

Read Cycle

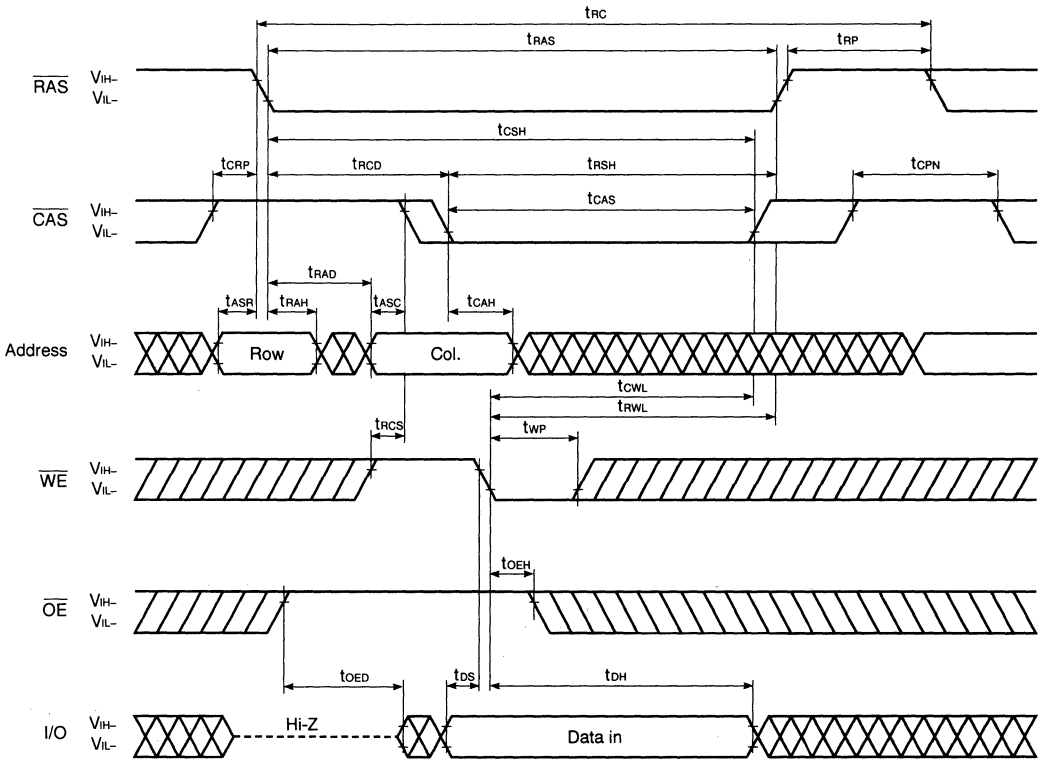

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCAS
tCPN
CAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
tWPZ
WE
tOCH
tOES
tCHO
tWEZ
tOEA
OE
tRAC
tAA
tOFC
tCAC
tOEZ
tOLZ
tOFR
tCLZ
I/O
VOH–
VOL–
Hi - Z
Data out
Hi - Z

Early Write Cycle

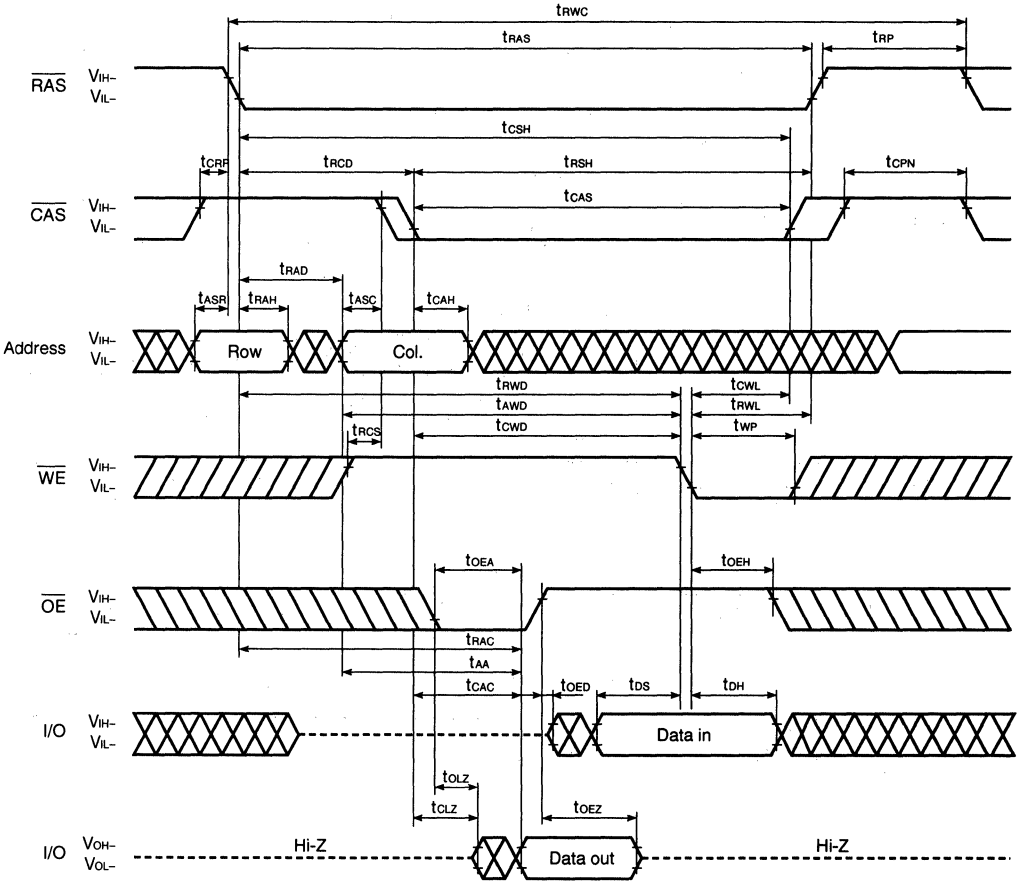


Remark $\overline{OE}$: Don't care

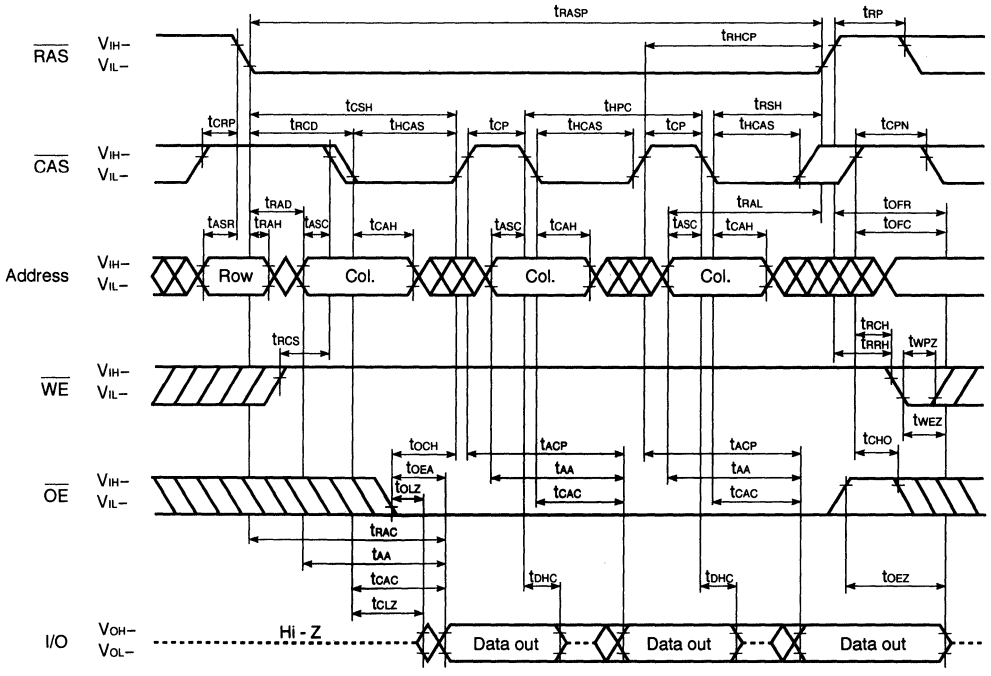
Late Write Cycle



Read Modify Write Cycle

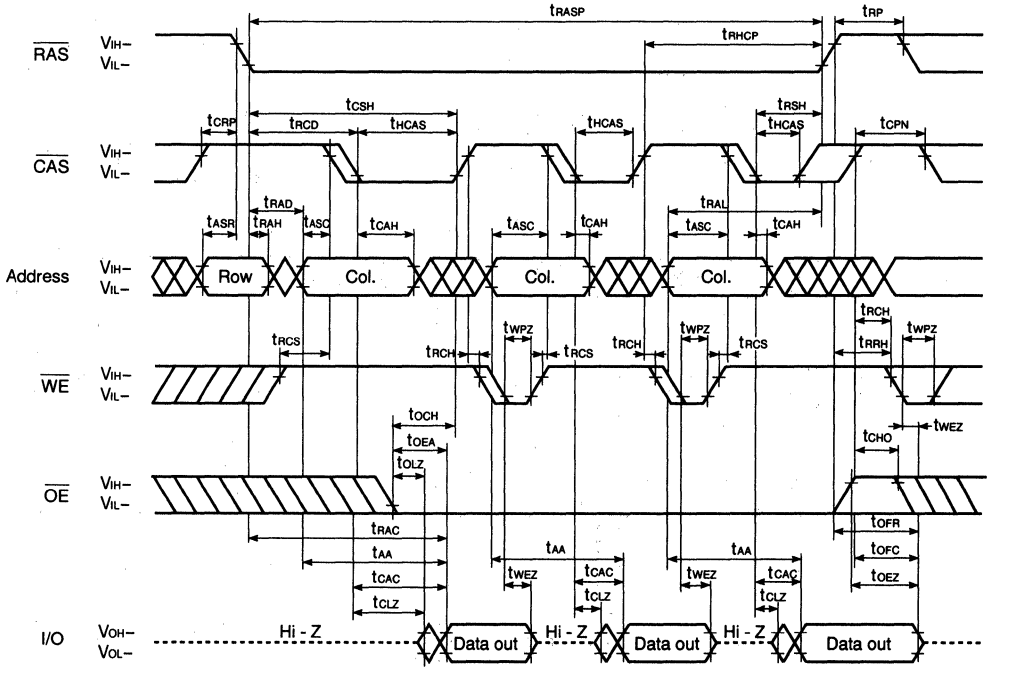


Hyper Page Mode (EDO) Read Cycle



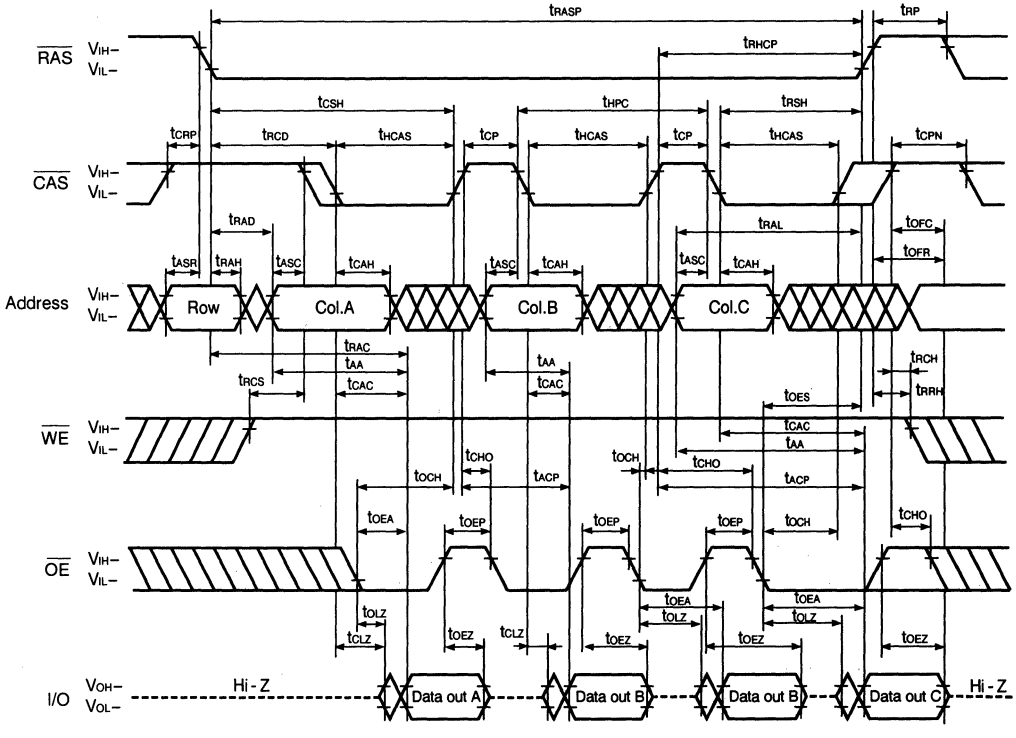
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{WE}$ Control)



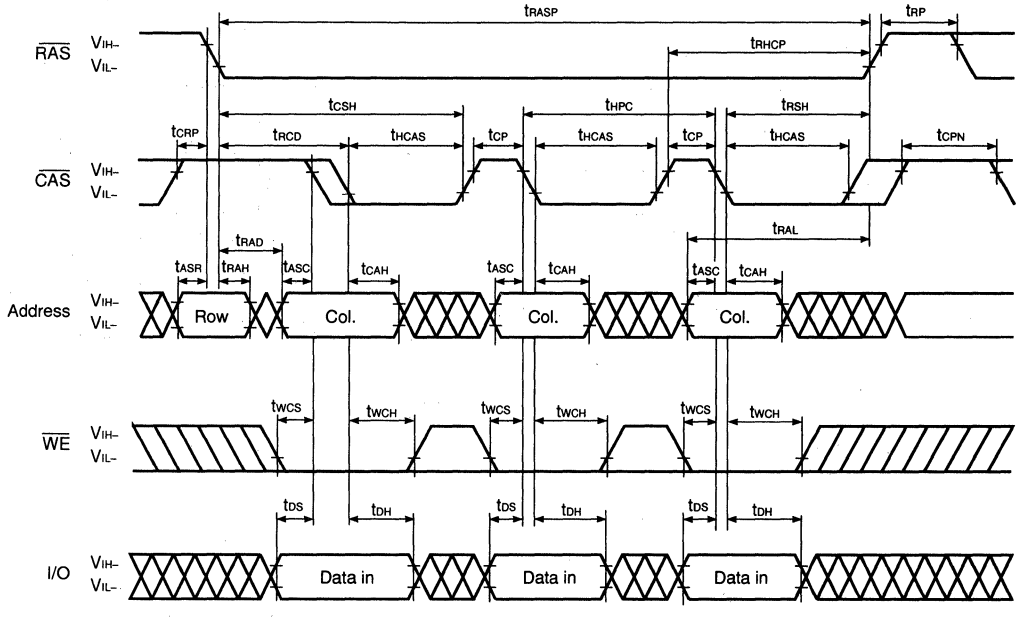
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{OE}$ Control)



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

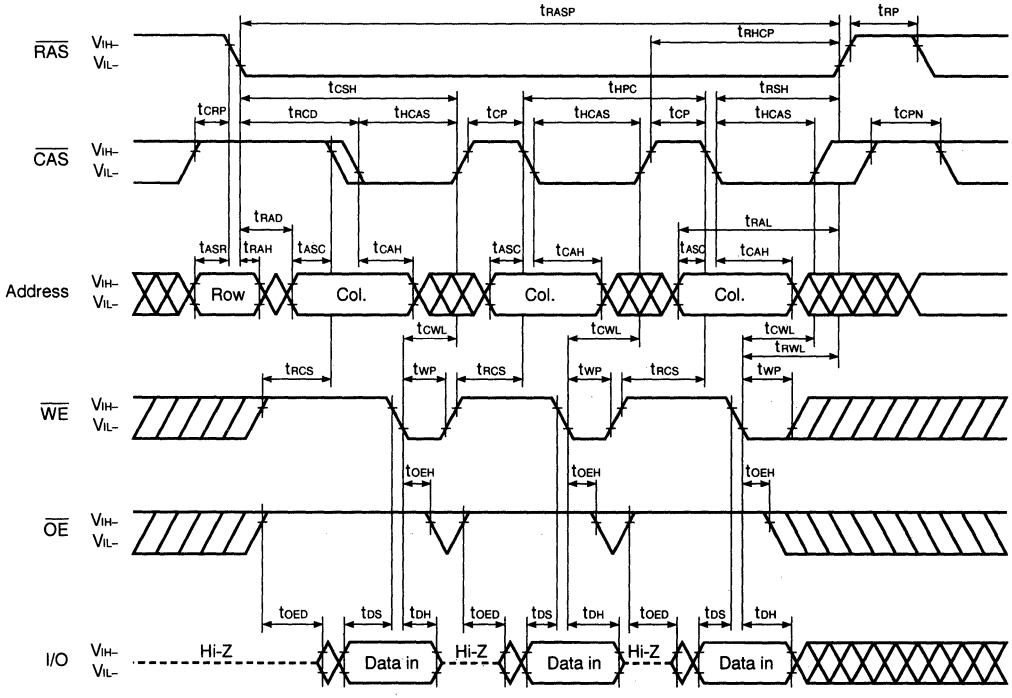
Hyper Page Mode (EDO) Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

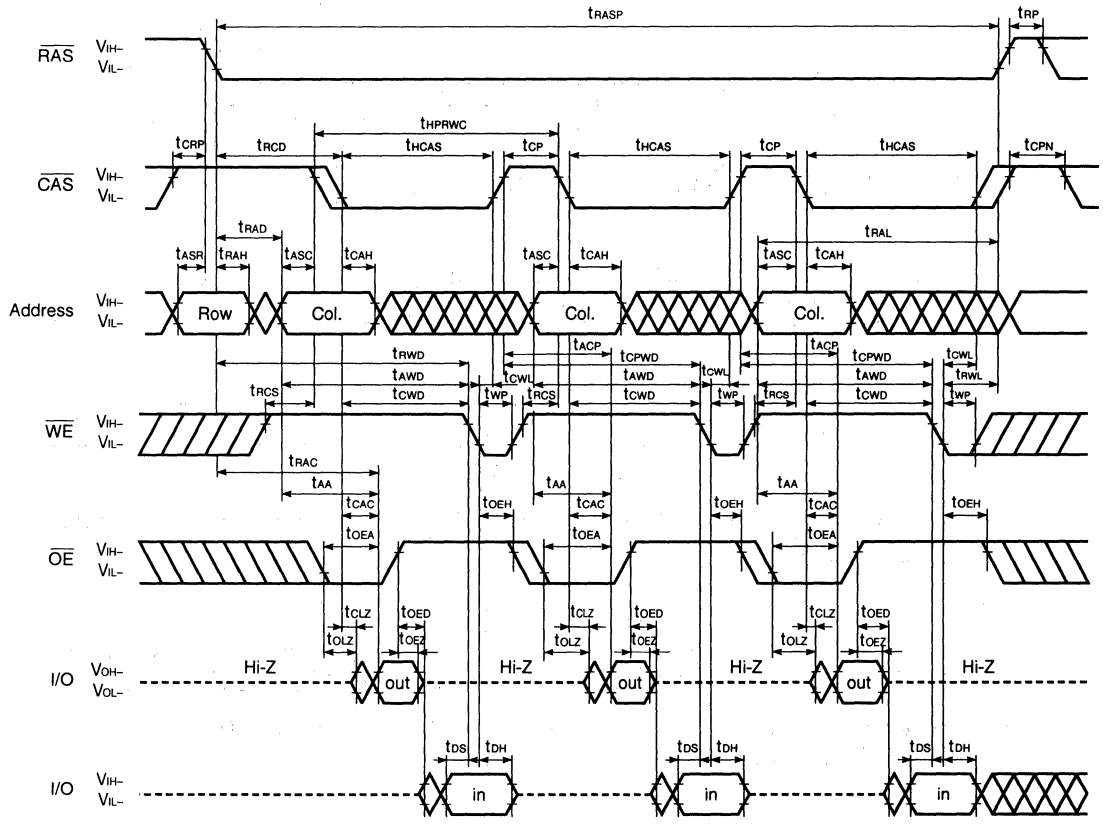
2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Late Write Cycle



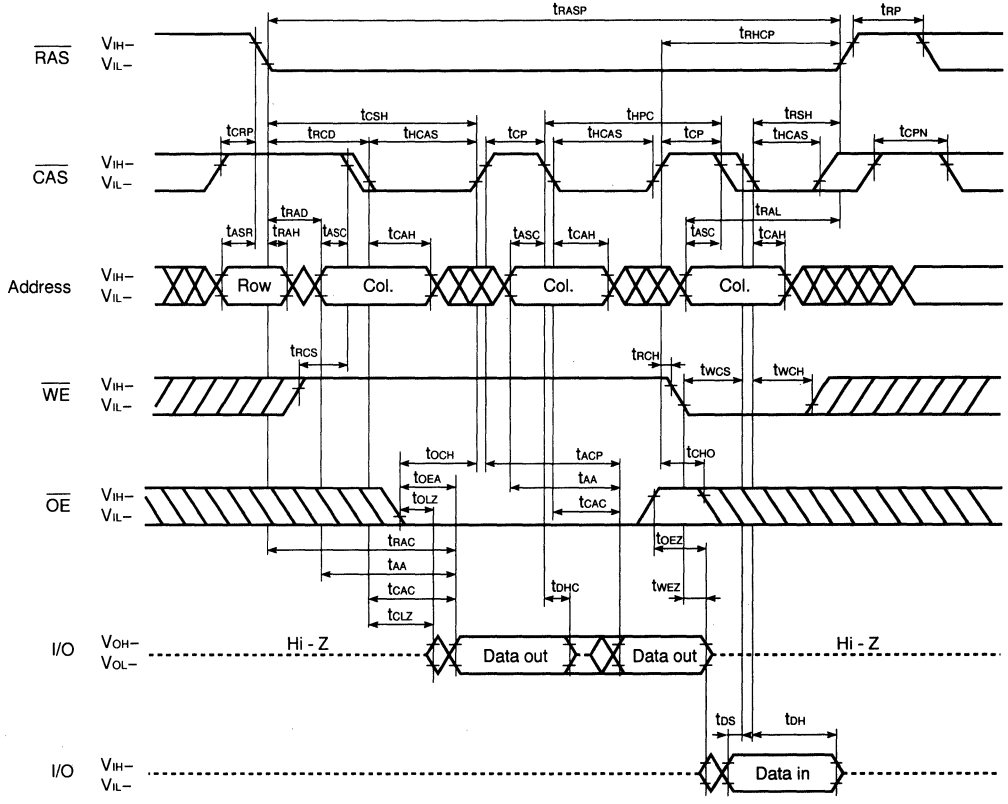
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Modify Write Cycle



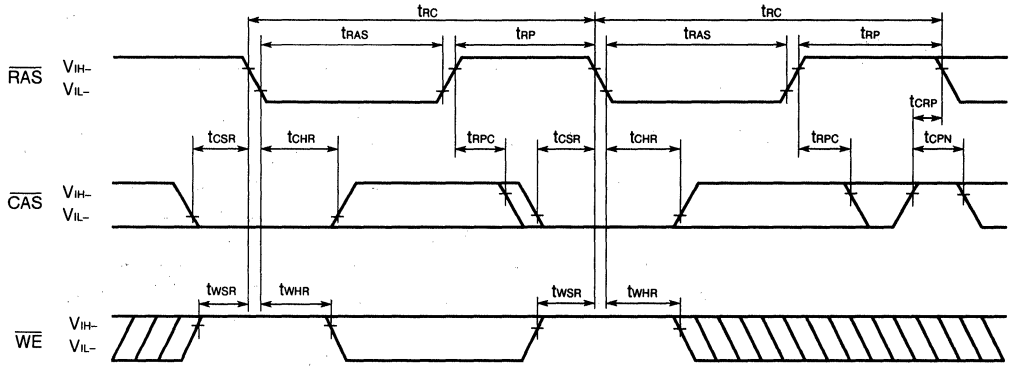
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read and Write Cycle



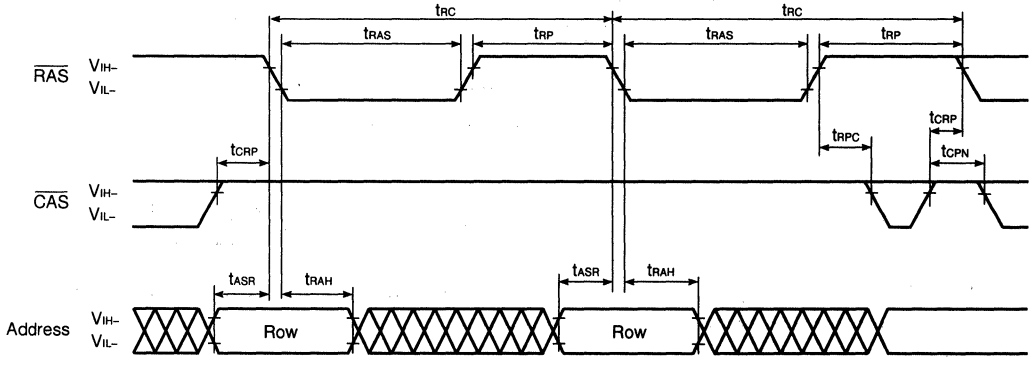
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



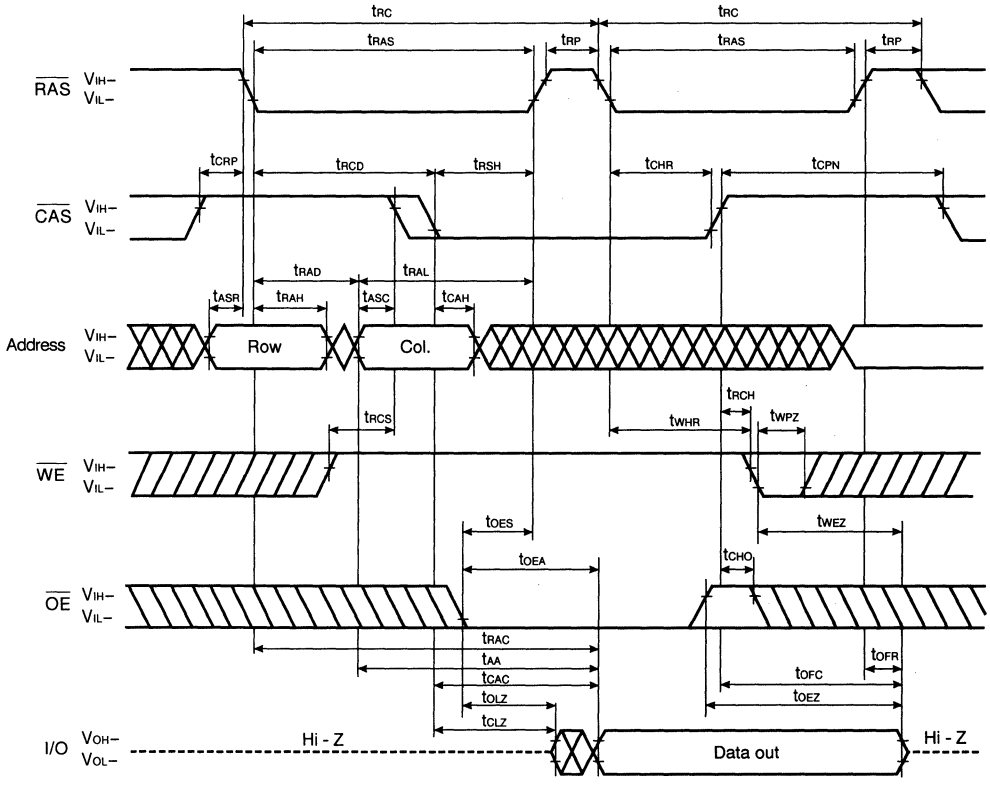
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

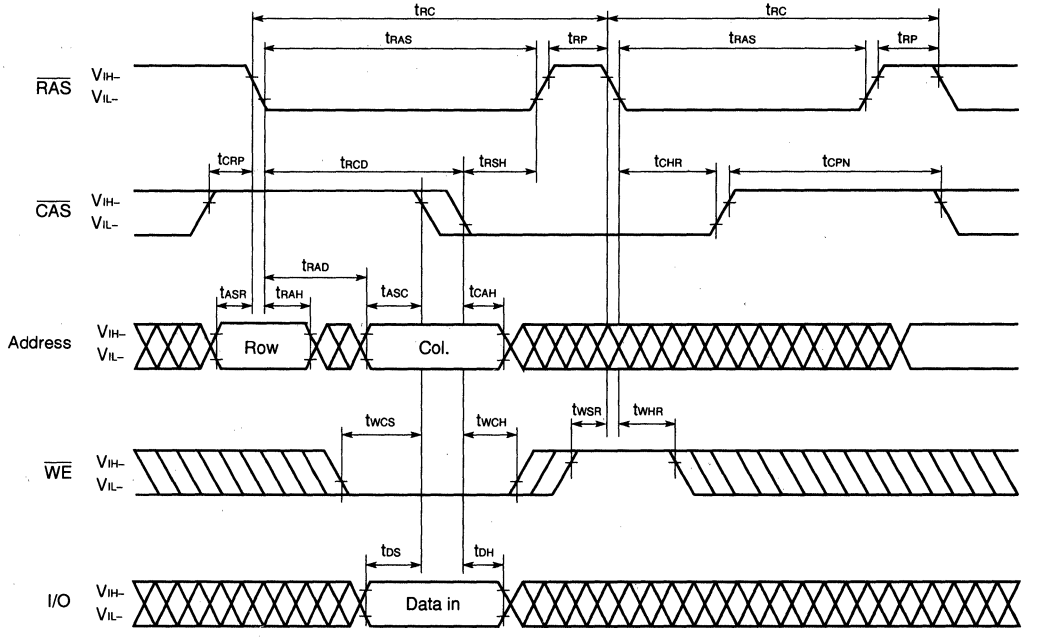


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



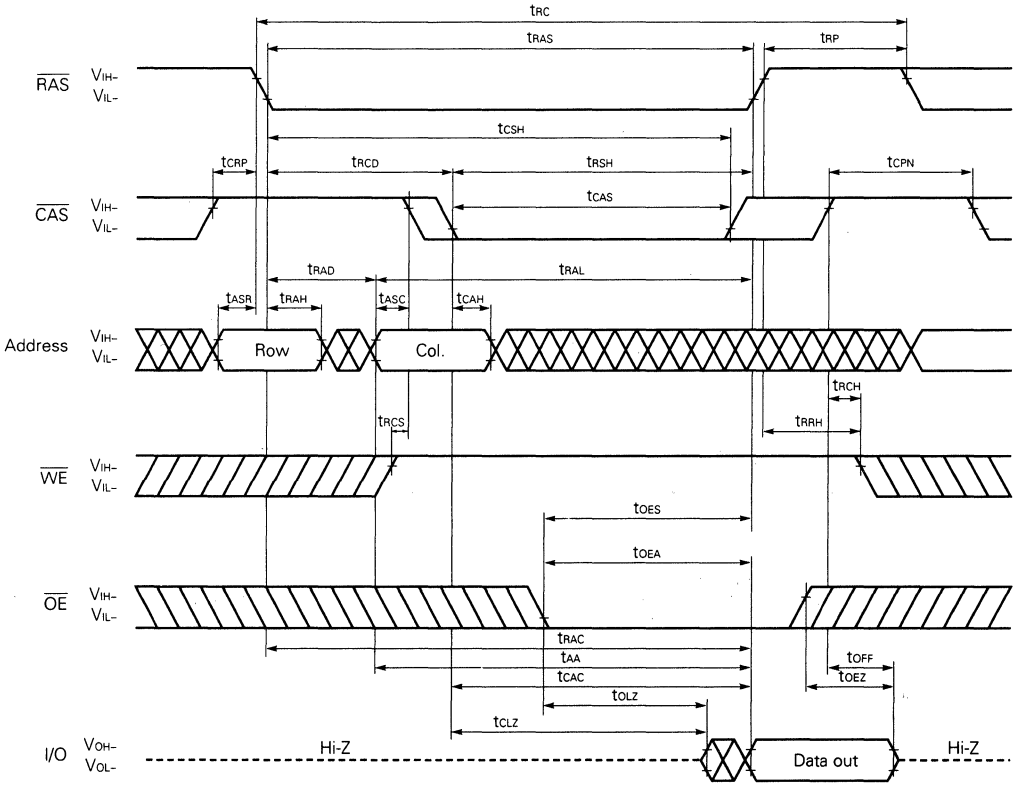
Hidden Refresh Cycle (Write)



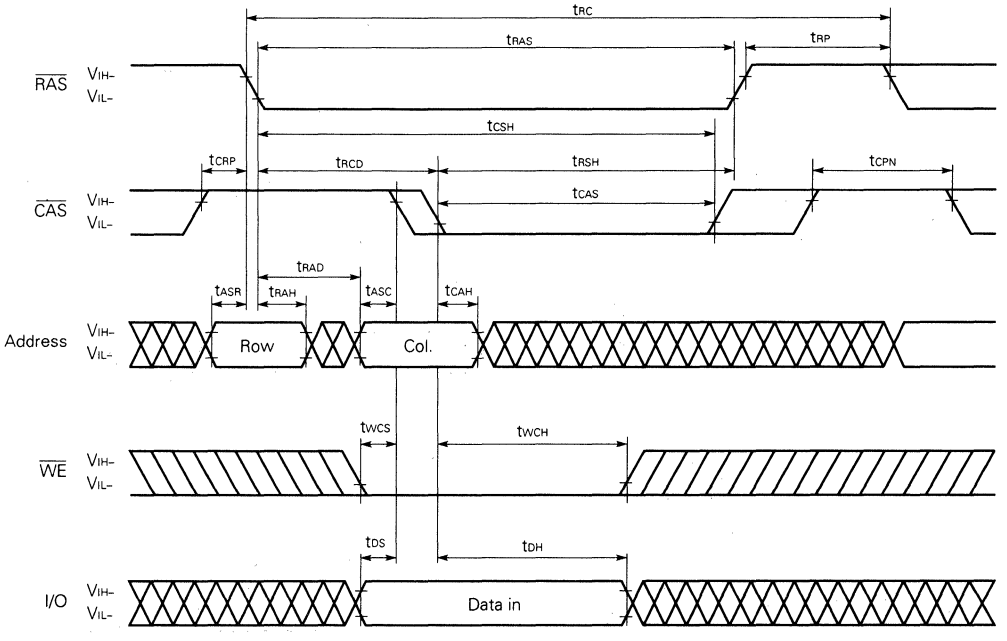
Remark $\overline{OE}$: Don't care

Timing Chart 3

Read Cycle

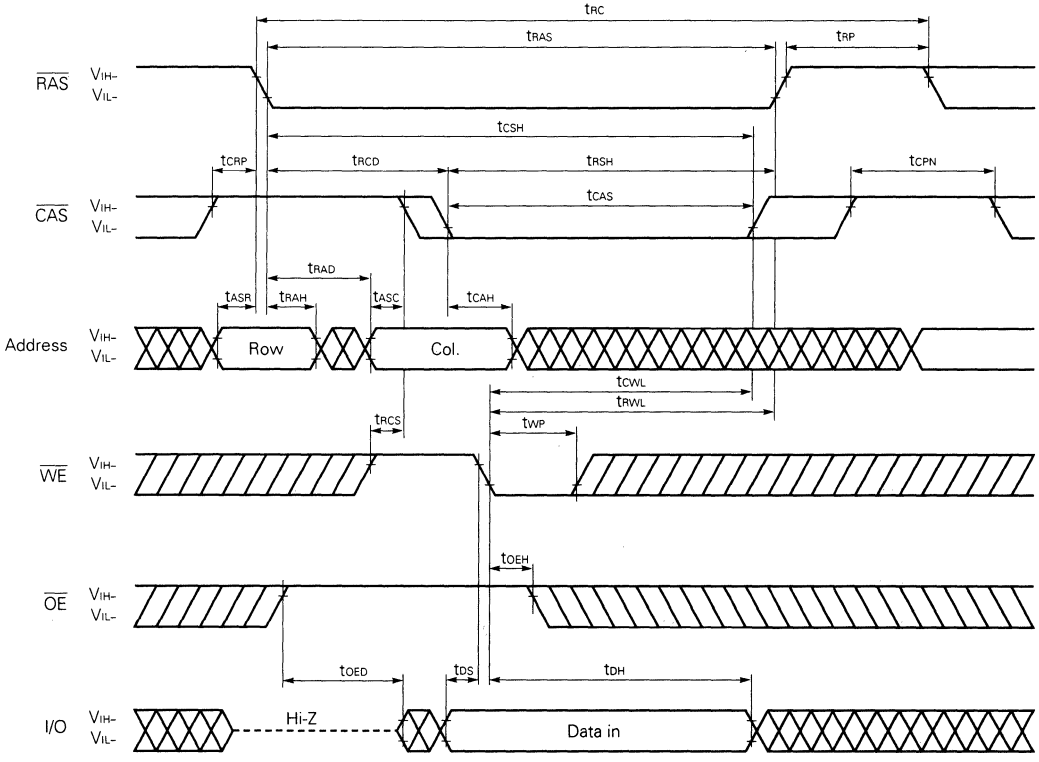

tRC
tRAS
tRP
RAS
VIH-
VIL-
tCSH
tCRP
tRCD
tRSH
tCPN
CAS
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
WE
tOES
tOEA
OE
tRAC
tAA
tOFF
tCAC
tOEZ
tOLZ
tCLZ
I/O
VOH-
VOL-
Hi-Z
Data out
Hi-Z

Early Write Cycle

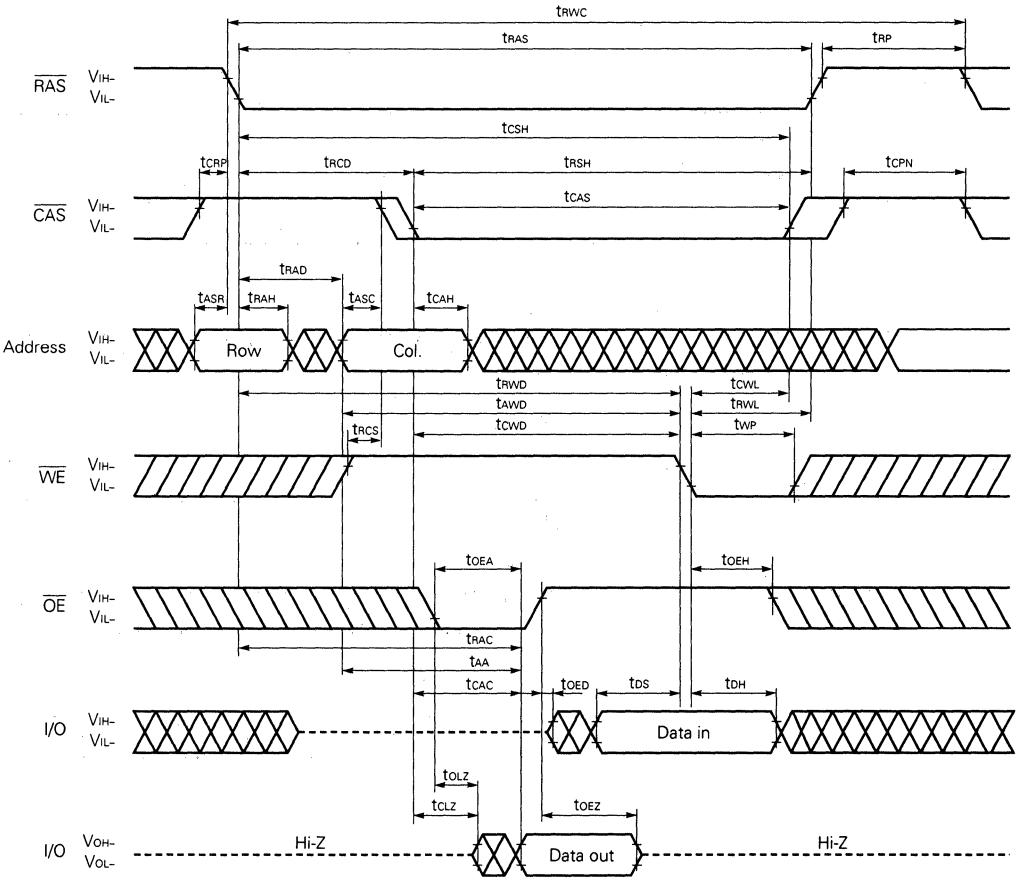


Remark $\overline{OE}$: Don't care

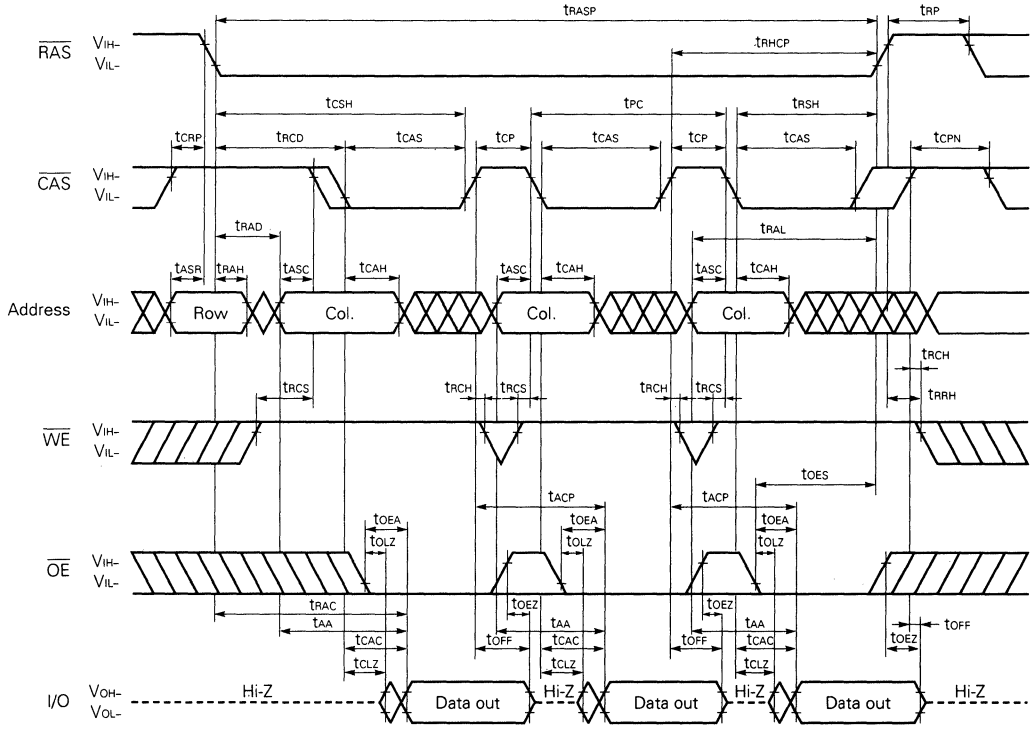
Late Write Cycle



Read Modify Write Cycle

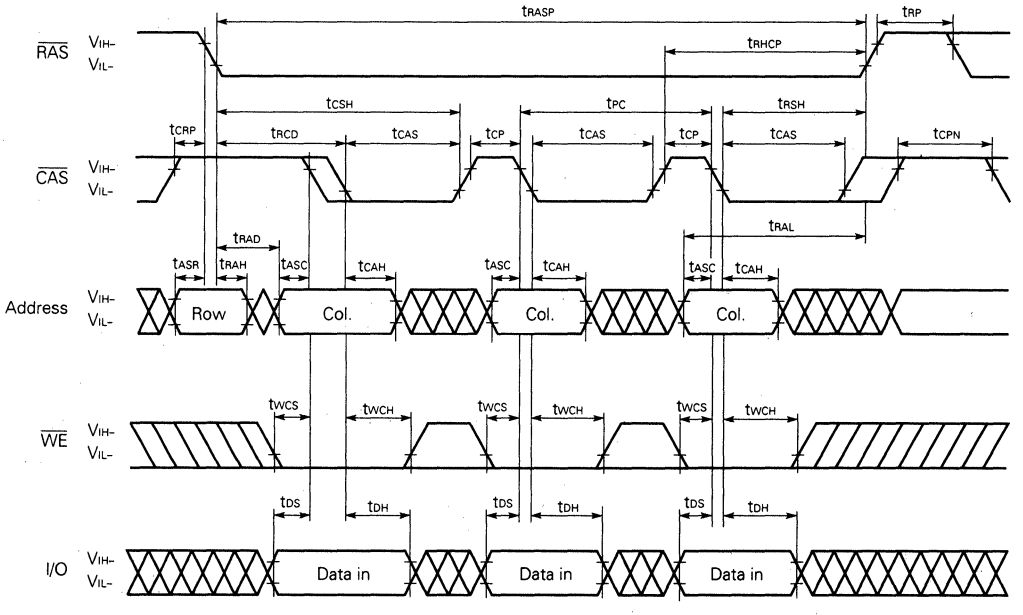


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

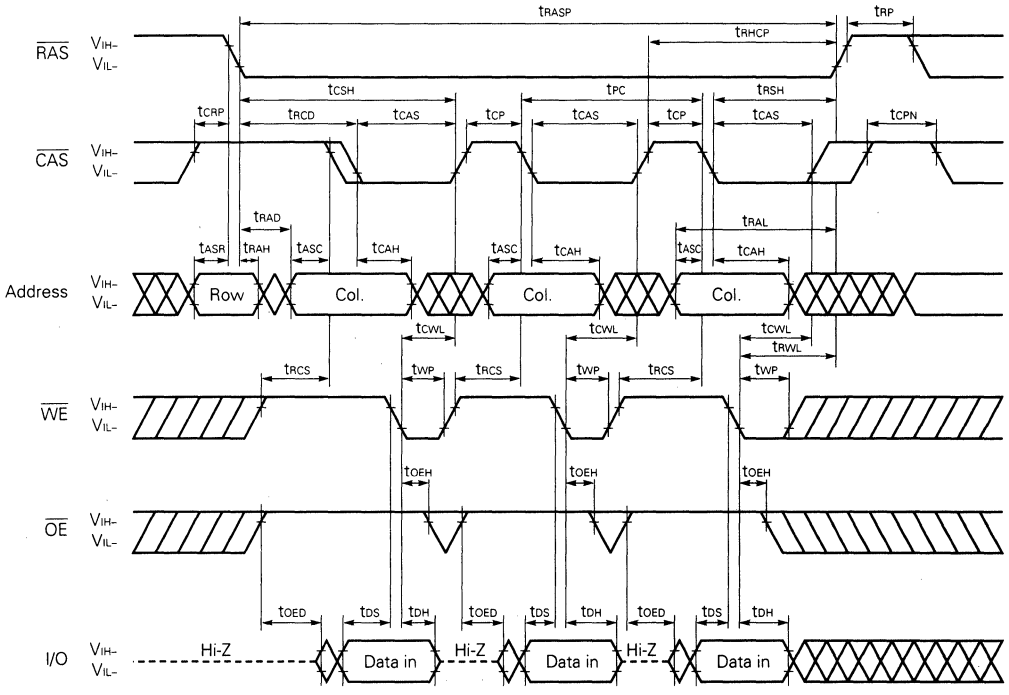
Fast Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

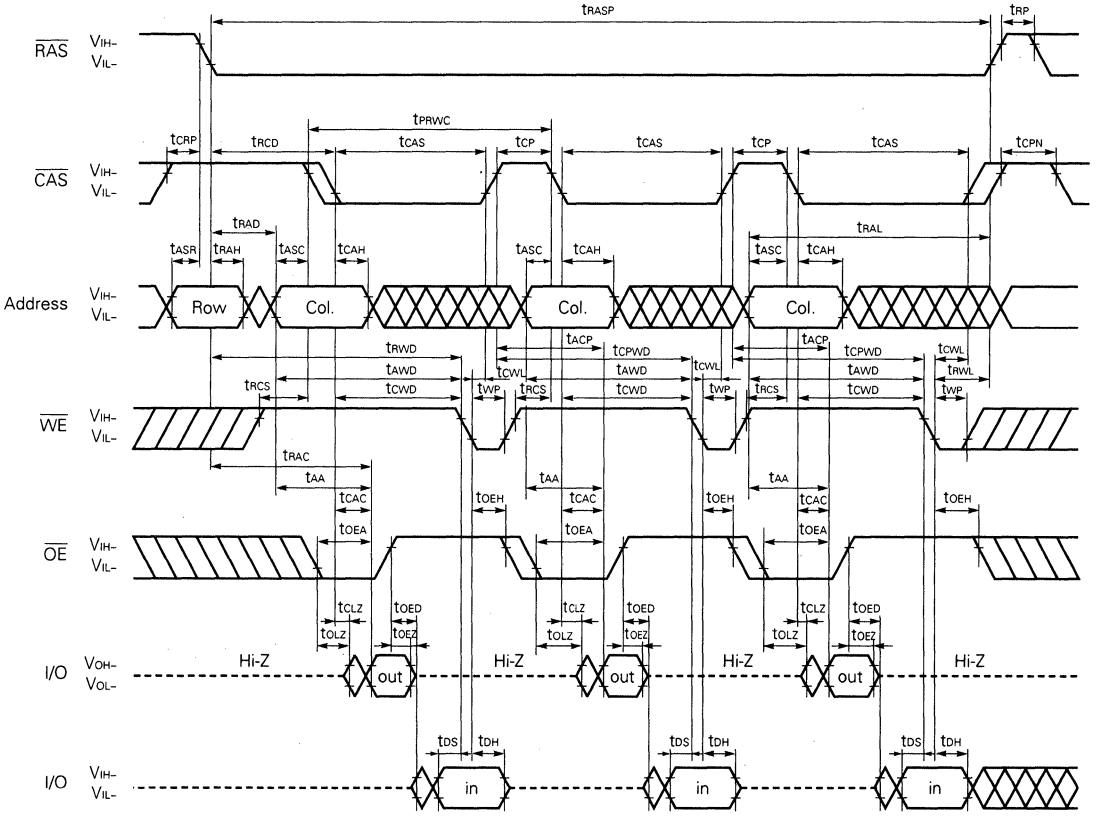
2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Late Write Cycle



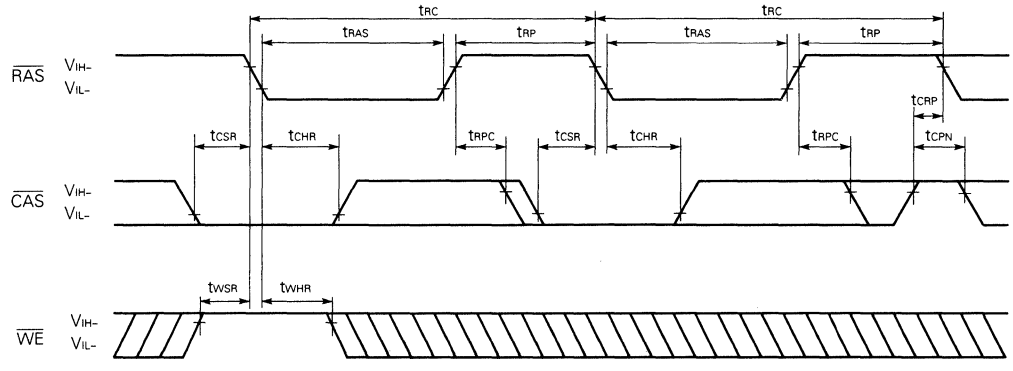
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Read Modify Write Cycle



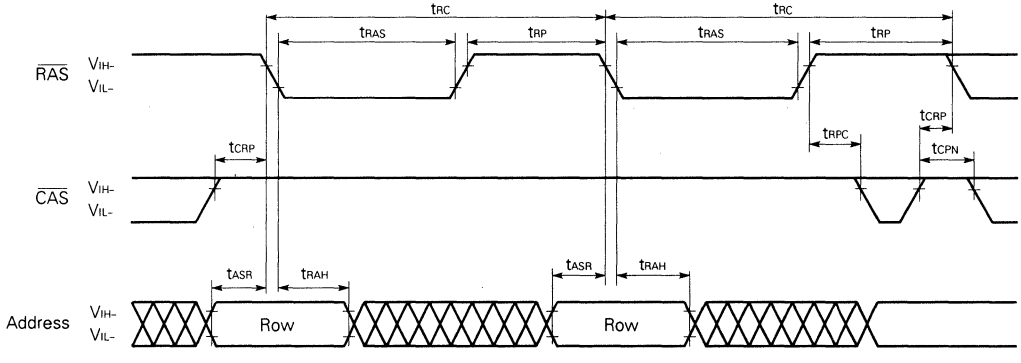
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



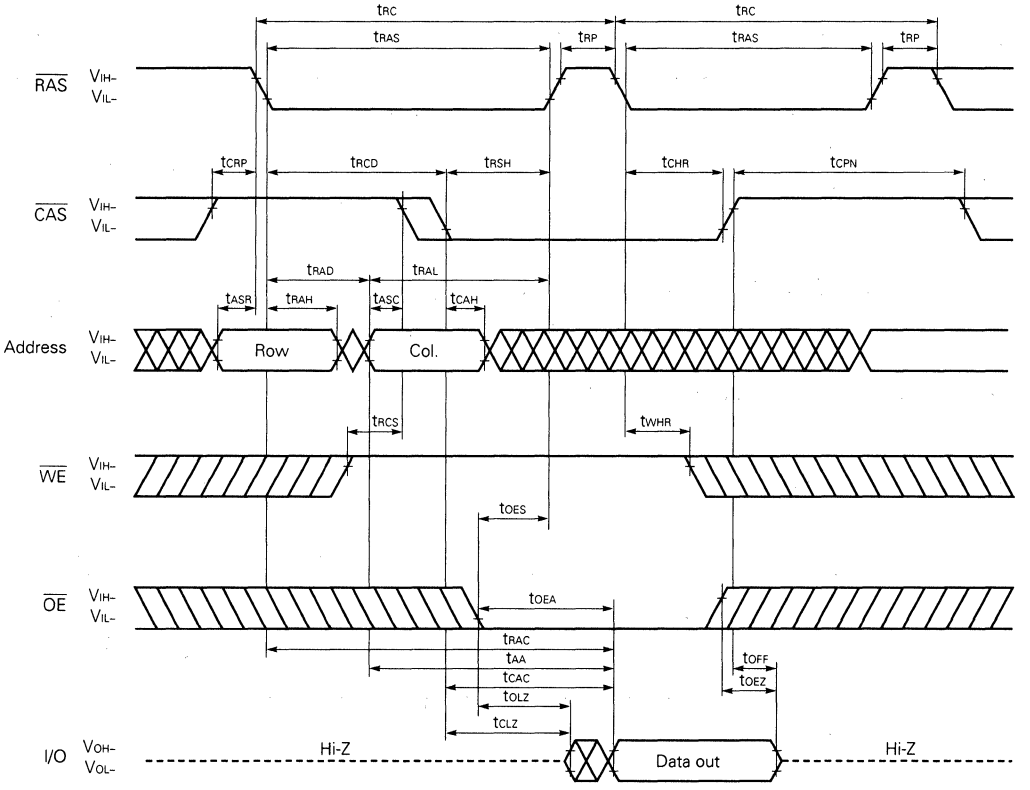
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

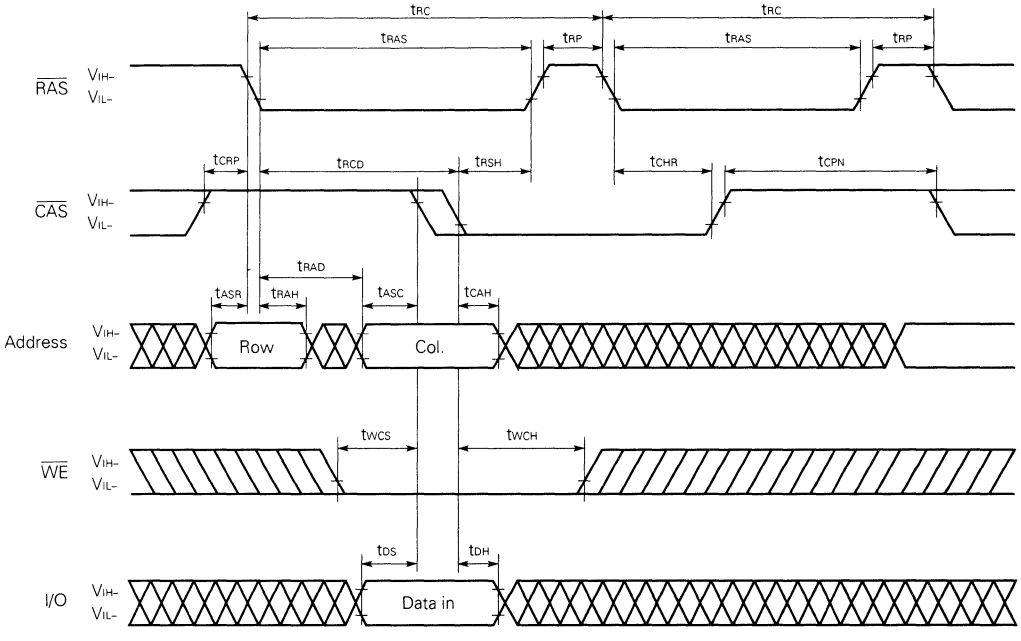


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



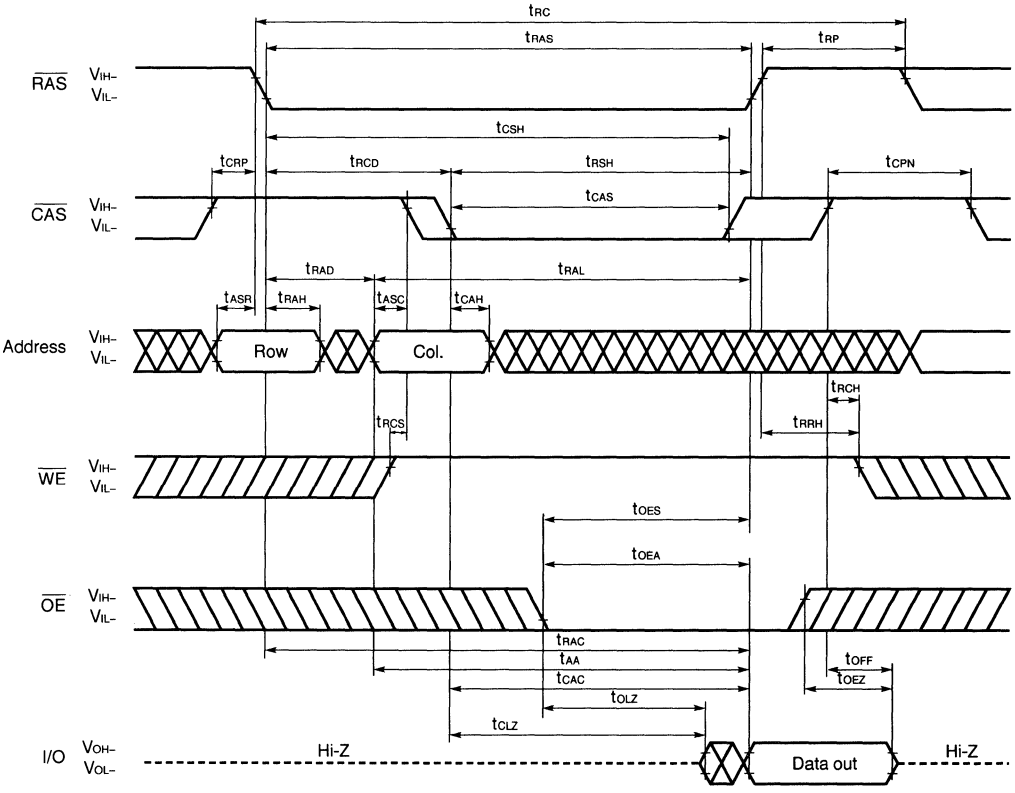
Hidden Refresh Cycle (Write)



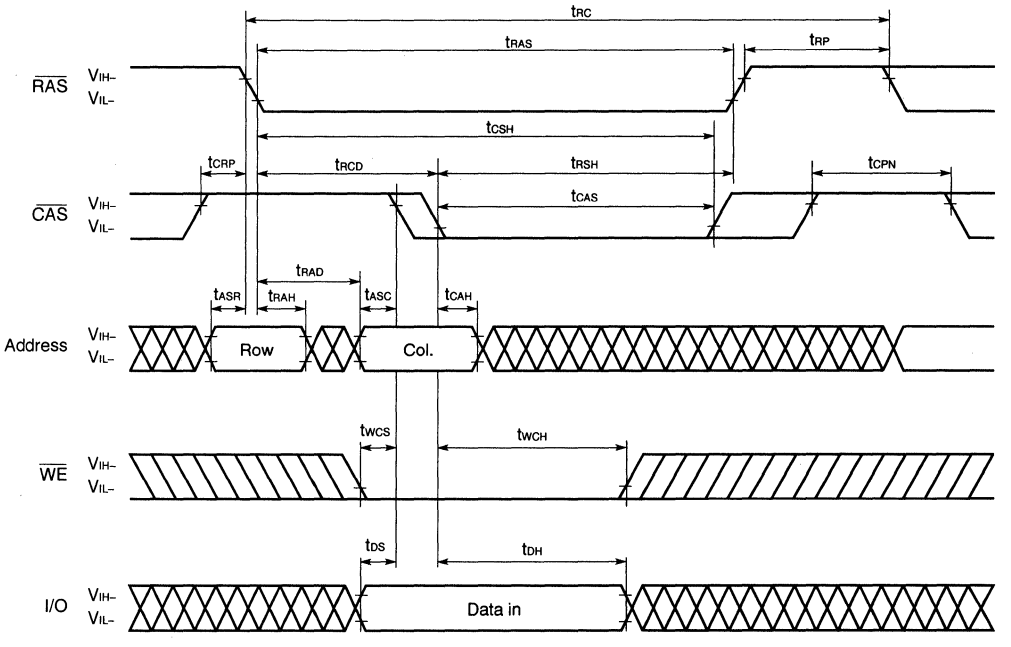
Remark $\overline{OE}$: Don't care

Timing Chart 4

Read Cycle

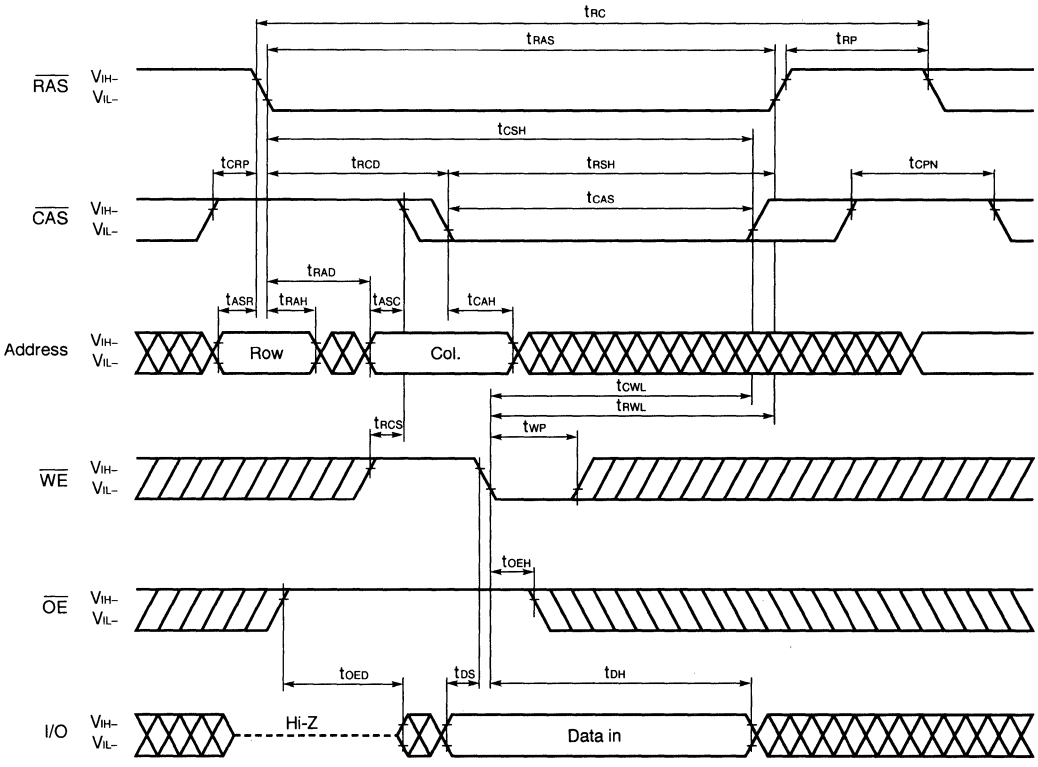

tRC
tRAS
tRP
RAS
VIH-
VIL-
tCSH
tCRP
tRCD
tRSH
tCPN
CAS
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
WE
tOES
tOEA
OE
tRAC
tAA
tOFF
tCAC
tOEZ
tOLZ
tCLZ
I/O
VOH-
VOL-
Hi-Z
Data out
Hi-Z

Early Write Cycle

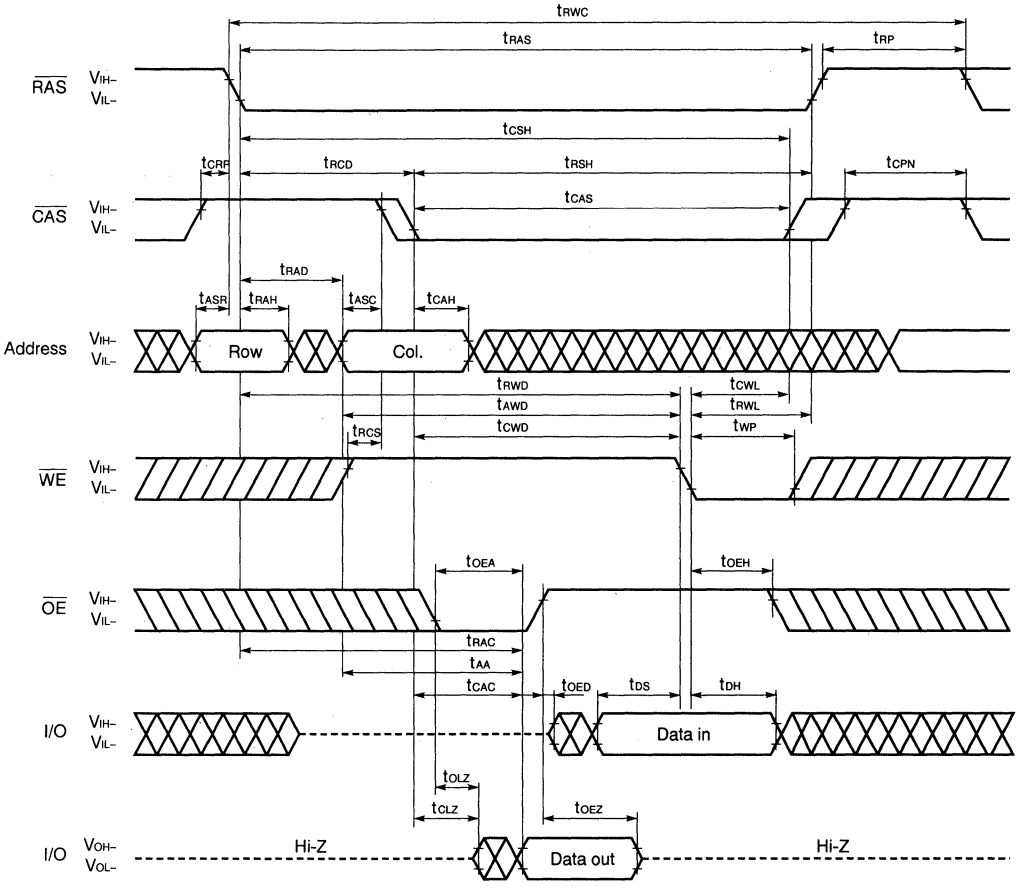


Remark $\overline{OE}$: Don't care

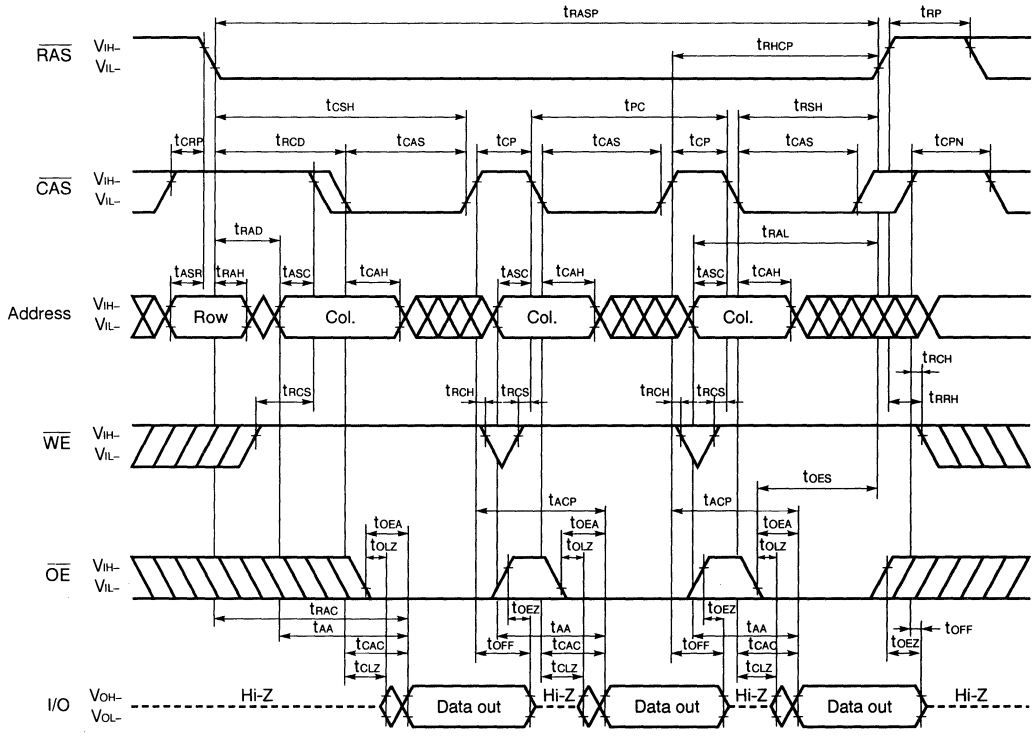
Late Write Cycle



Read Modify Write Cycle

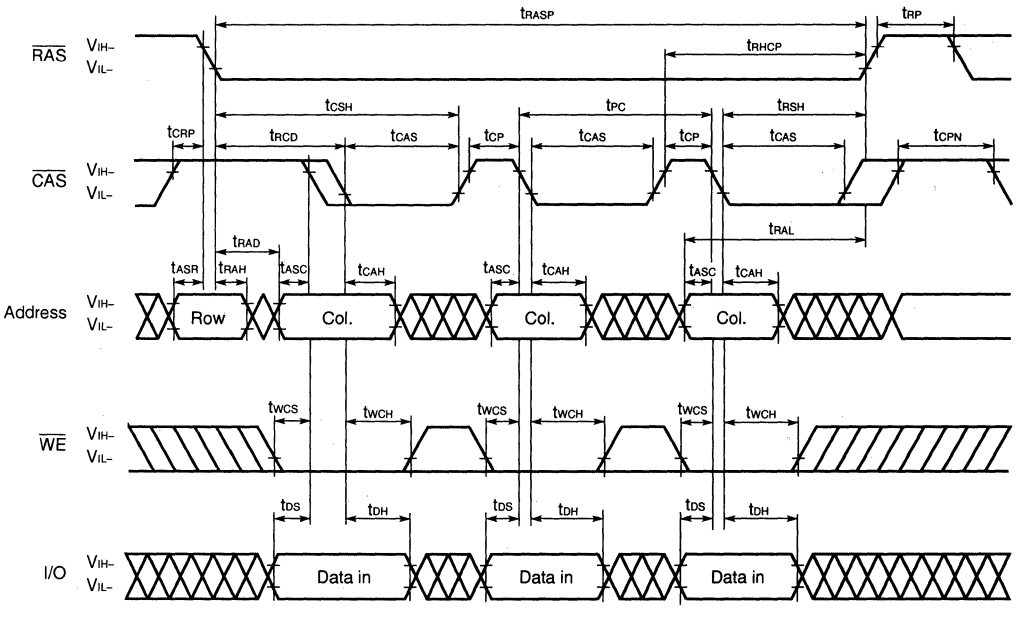


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

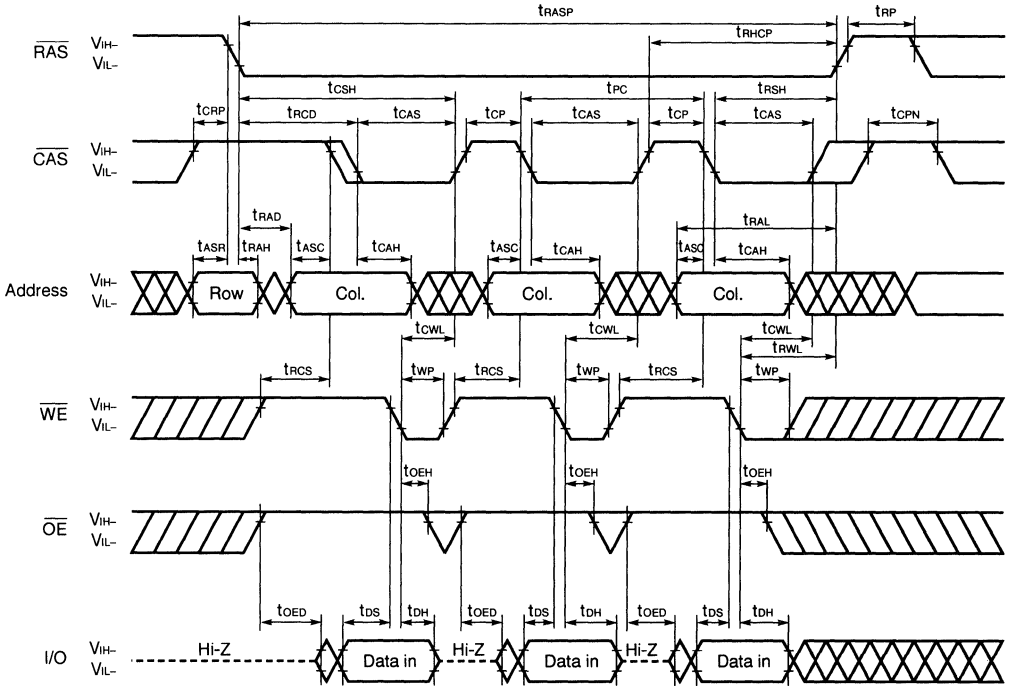
Fast Page Mode Early Write Cycle



Remark $\overline{OE}$: Don't care

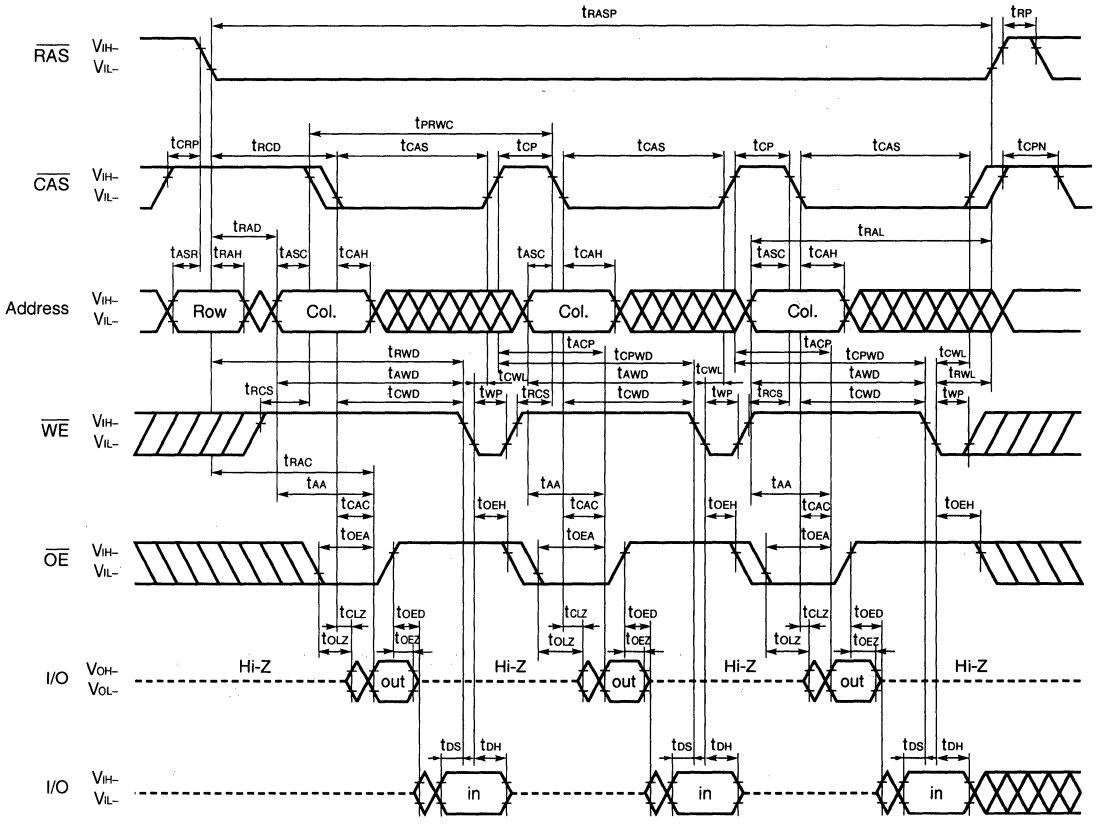
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Late Write Cycle



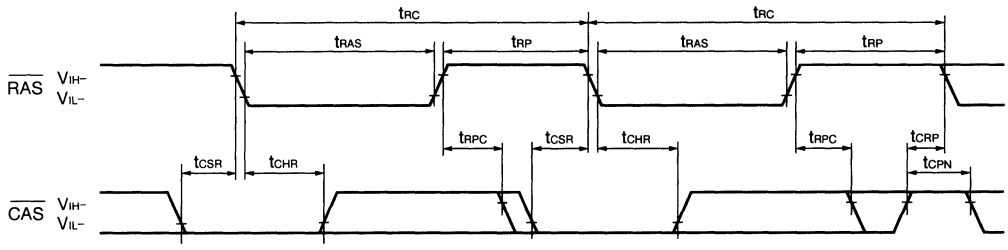
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Read Modify Write Cycle



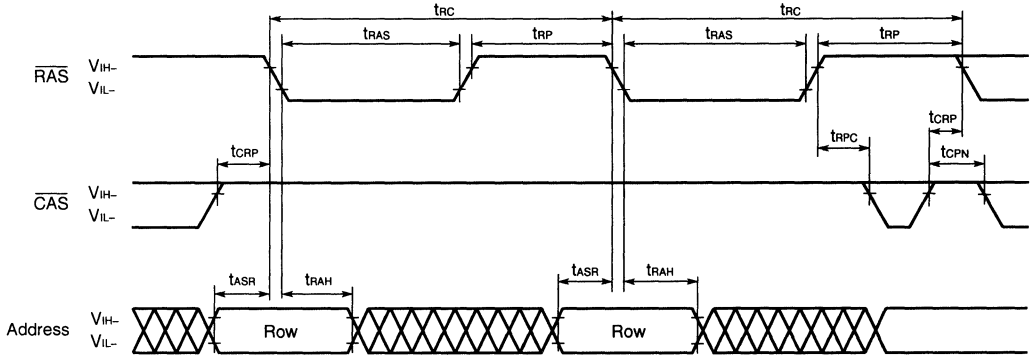
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



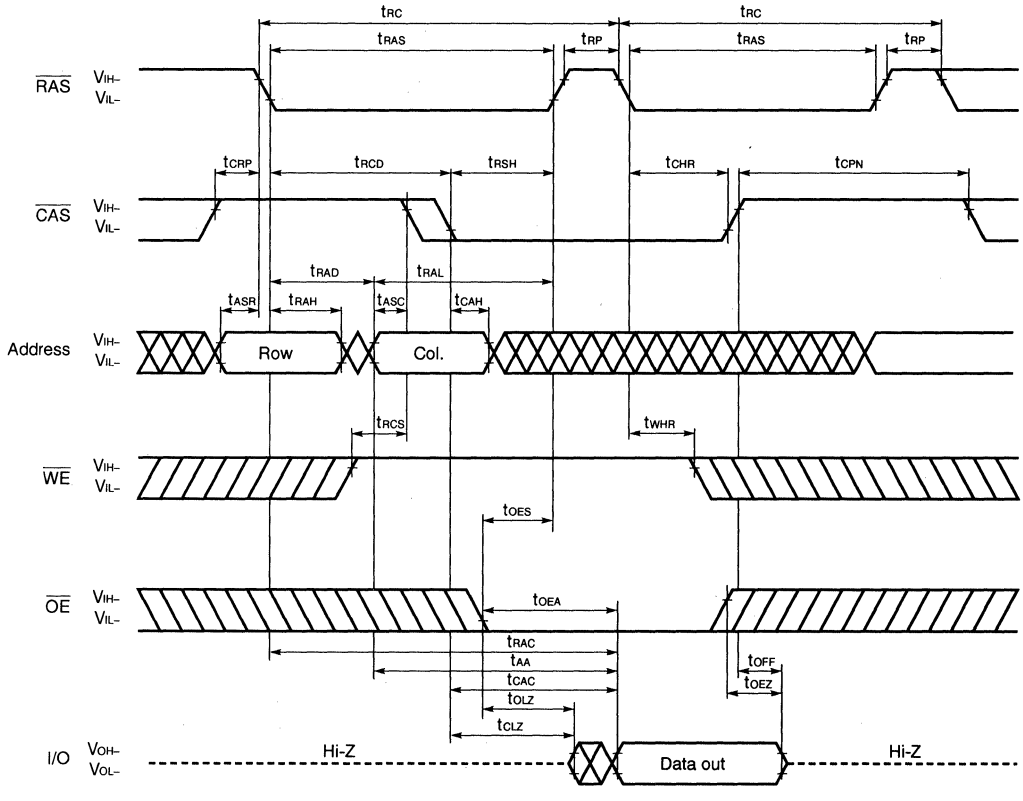
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

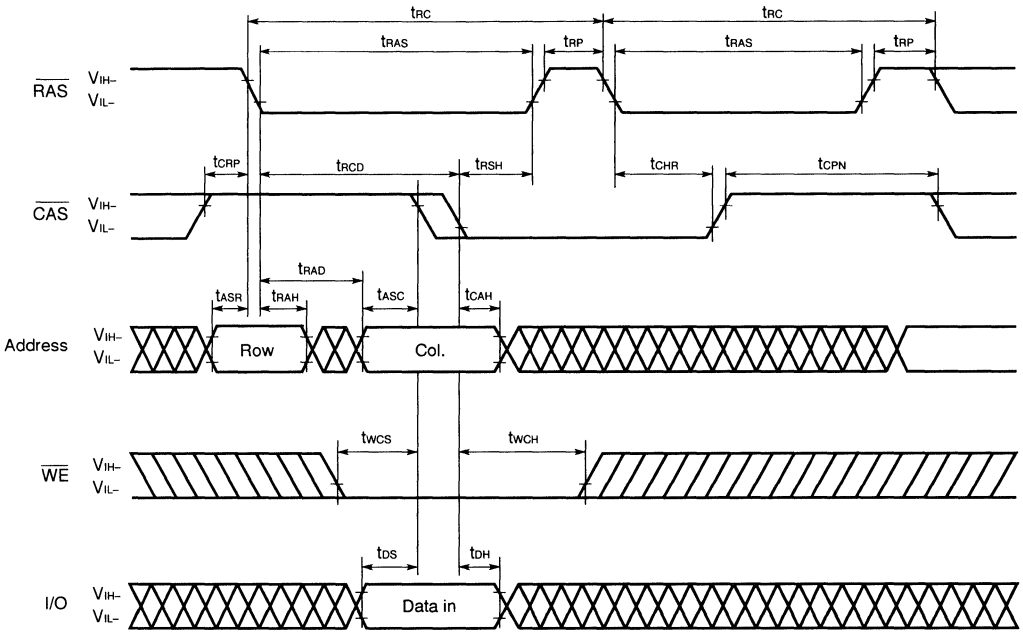


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



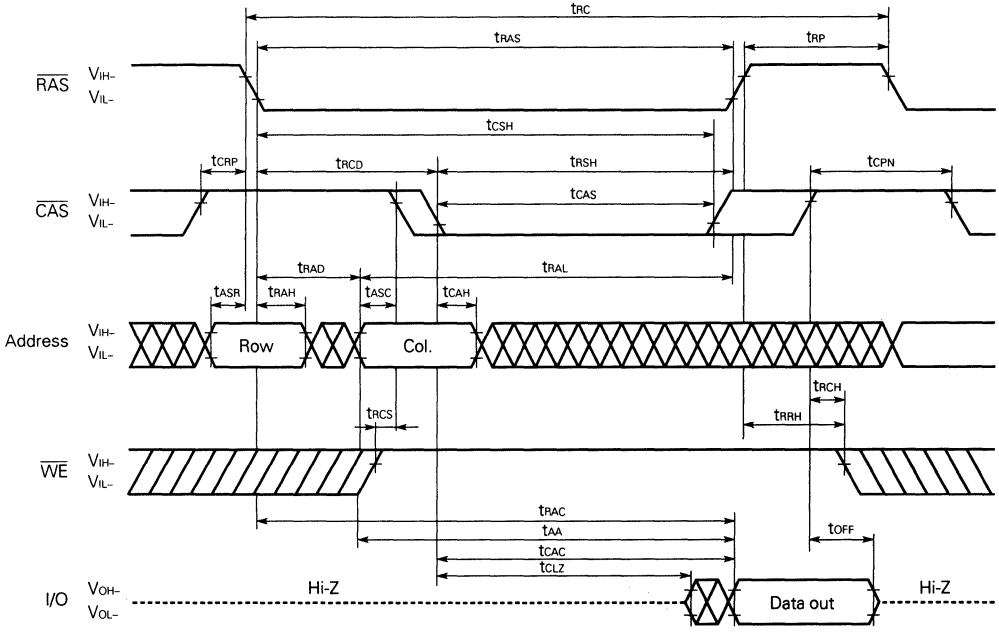
Hidden Refresh Cycle (Write)



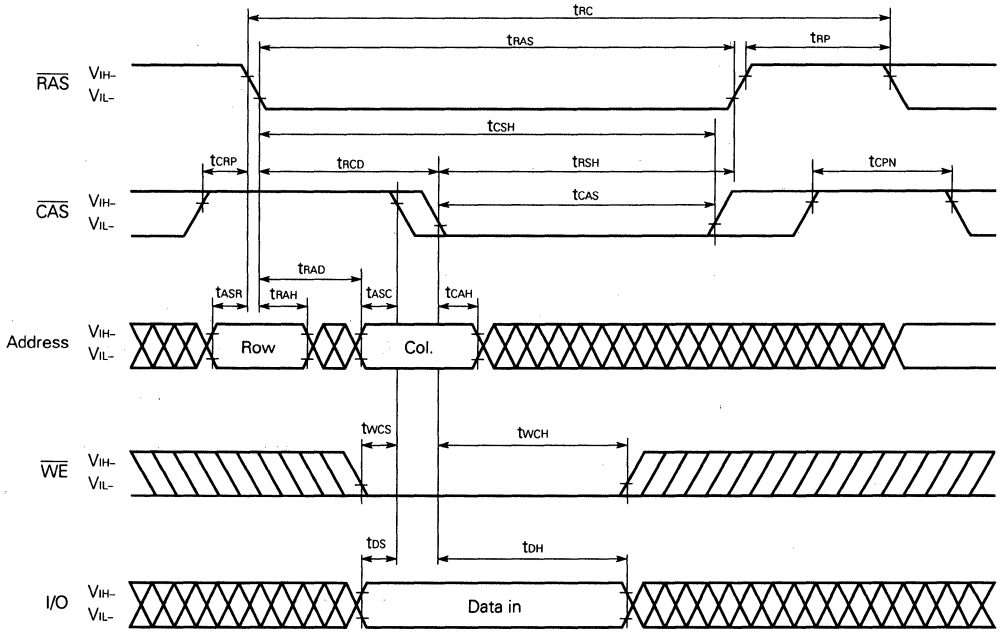
Remark $\overline{OE}$: Don't care

Timing Chart 5

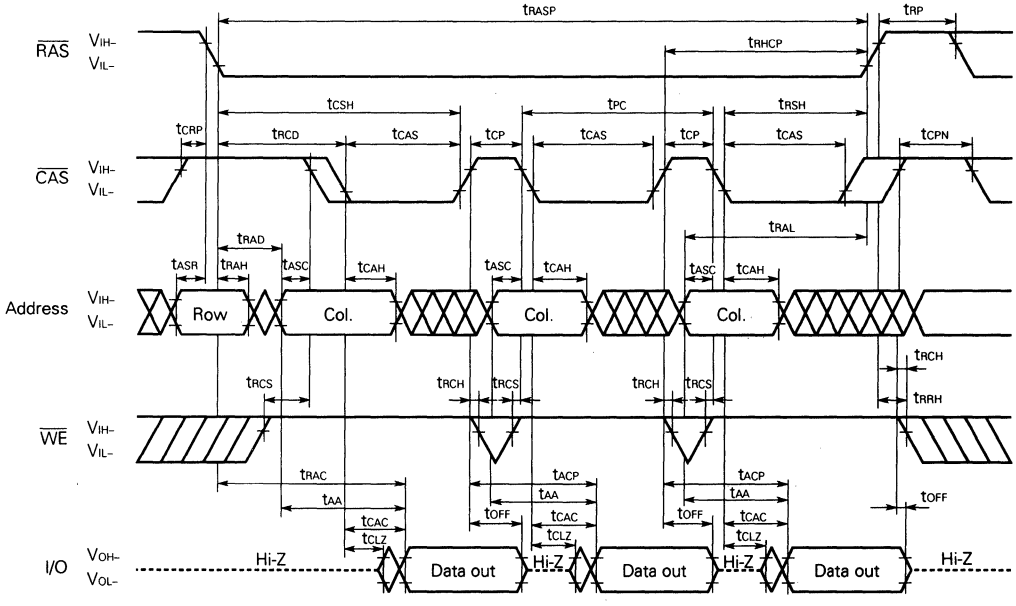
Read Cycle


tRC
tRAS
tRP
RAS
VIH-
VIL-
tCSH
tCRP
tRCD
tRSH
tCPN
CAS
VIH-
VIL-
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
VIH-
VIL-
Row
Col.
tRCH
tRCS
tRRH
WE
VIH-
VIL-
tRAC
tAA
tOFF
tCAC
tCLZ
I/O
VOH-
VOL-
Hi-Z
Data out
Hi-Z

Early Write Cycle

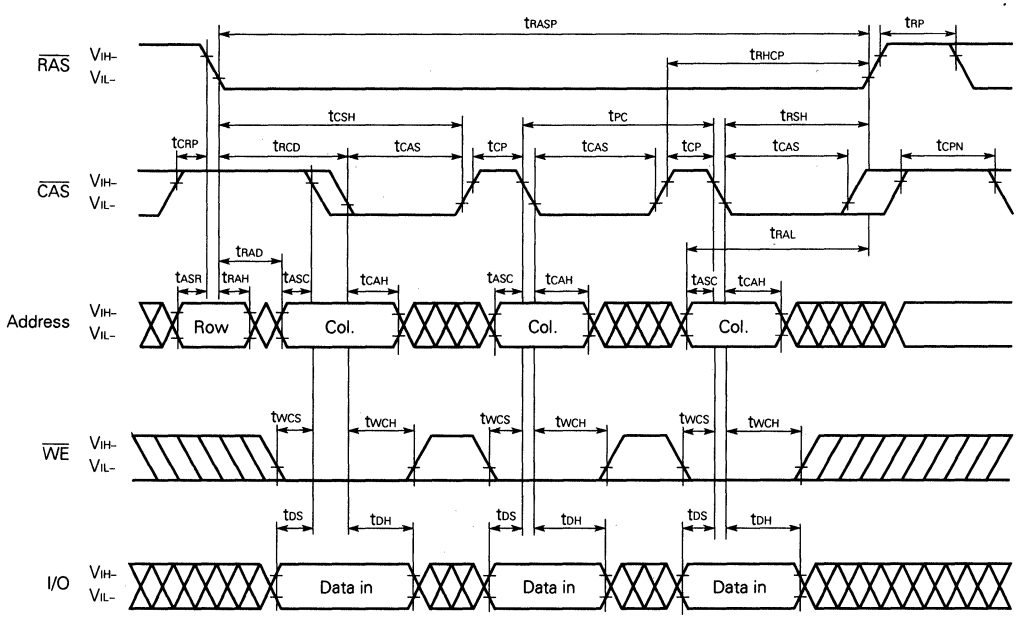


Fast Page Mode Read Cycle



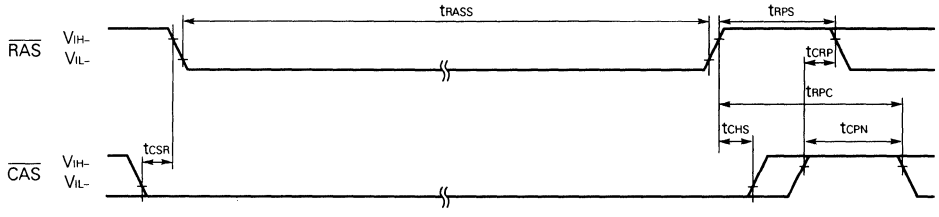
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Early Write Cycle



Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle



Remark Address, $\overline{WE}$: Don't care I/O : Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with burst long $\overline{RAS}$ only refresh, the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh

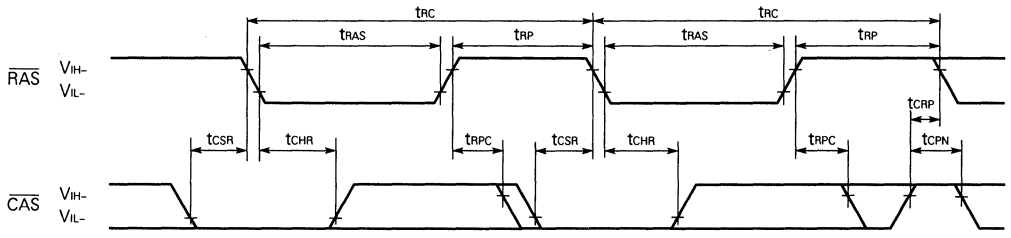
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 1,024 times within a 16 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst Long $\overline{RAS}$ Only Refresh

When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 1,024 times within a 16 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

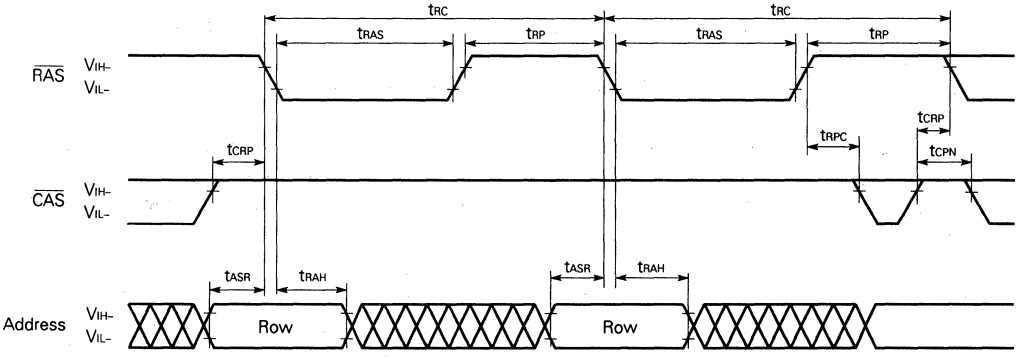
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



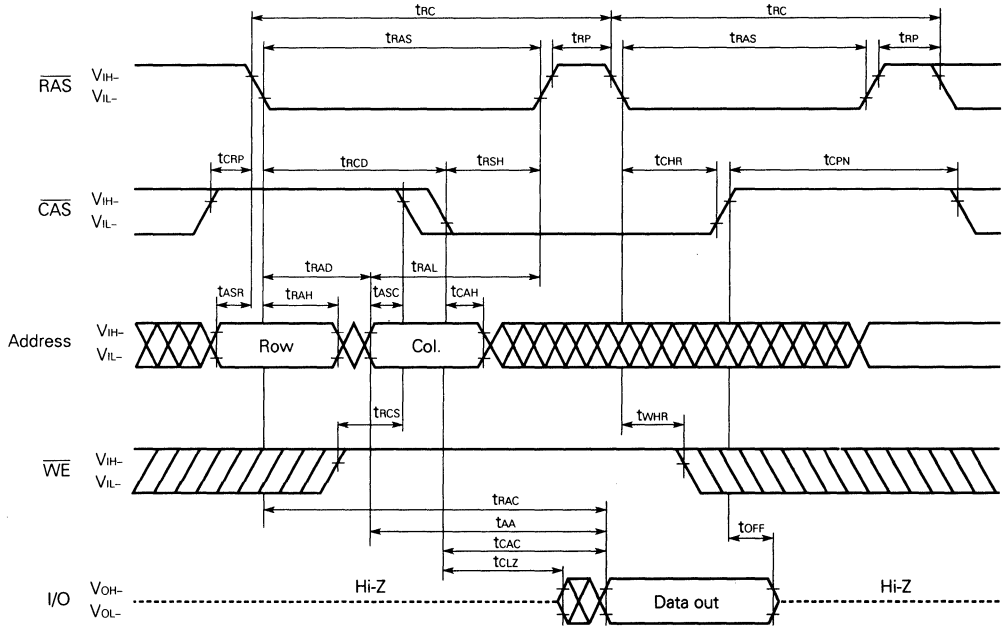
Remark Address, $\overline{WE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

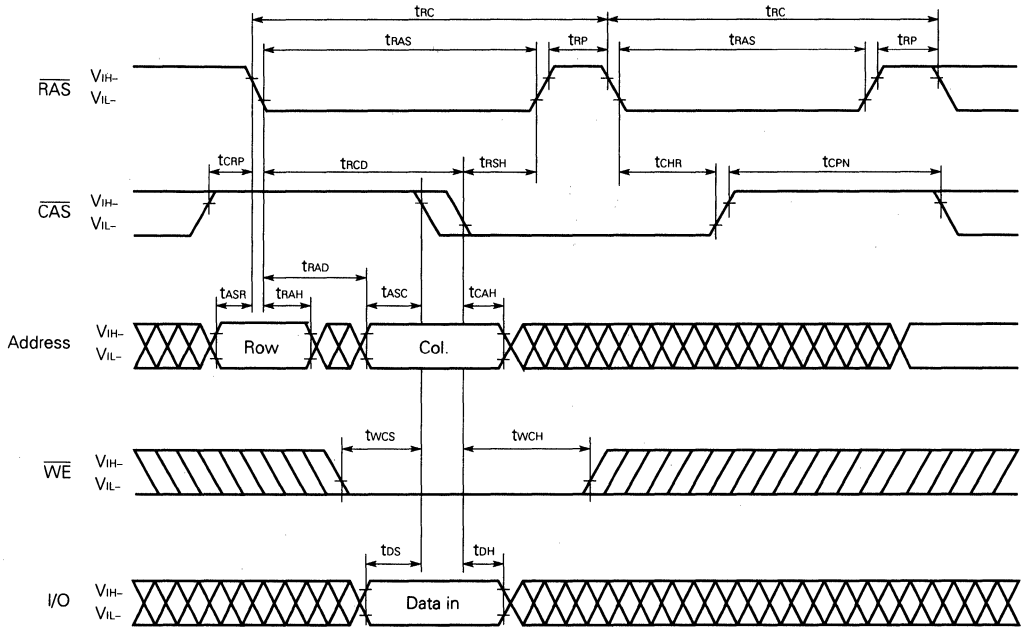


Remark $\overline{WE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

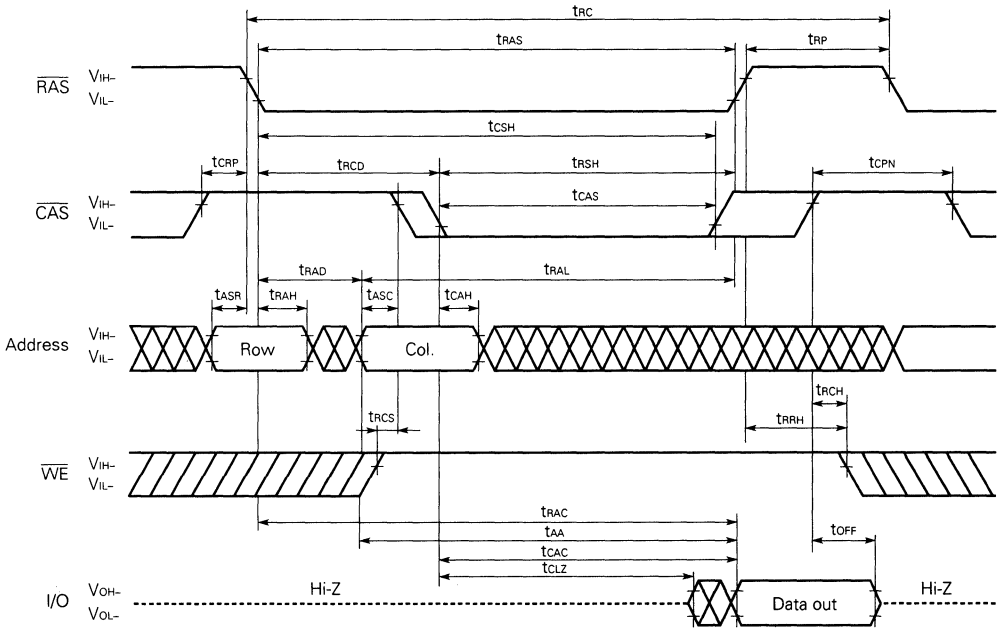


Hidden Refresh Cycle (Write)

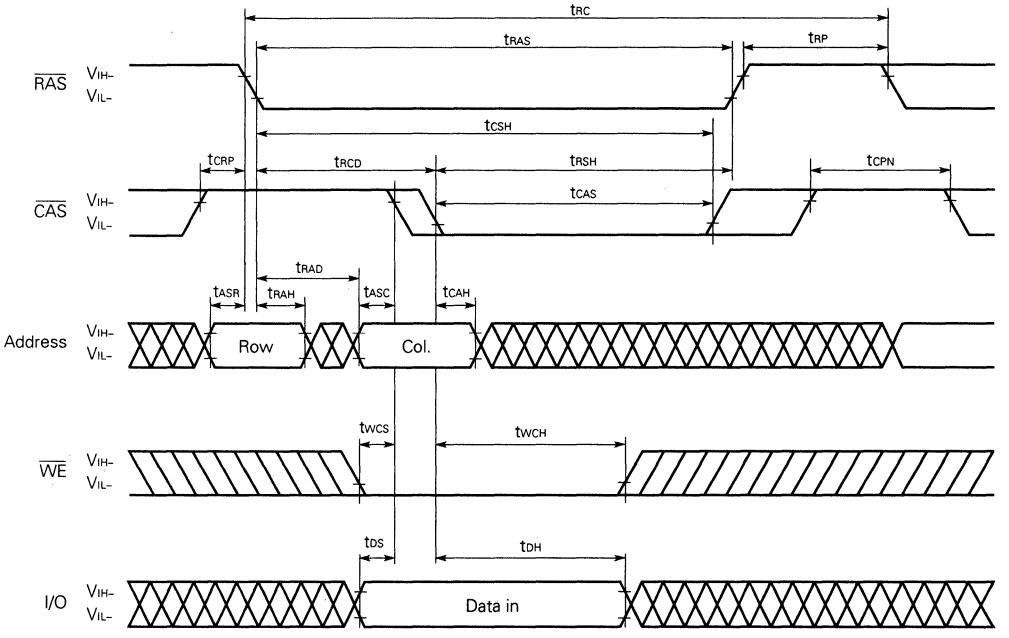


Timing Chart 6

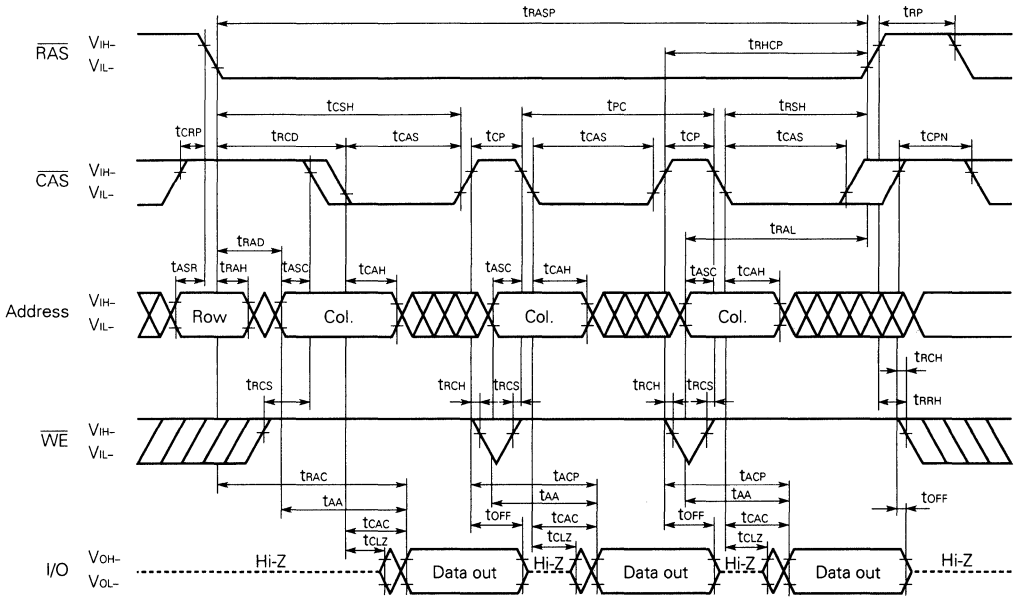
Read Cycle


tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
CAS
VIH–
VIL–
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
VIH–
VIL–
Row
Col.
tRCH
tRCS
tRRH
WE
VIH–
VIL–
tRAC
tAA
tOFF
tCAC
tCLZ
I/O
VOH–
VOL–
Hi-Z
Data out
Hi-Z

Early Write Cycle

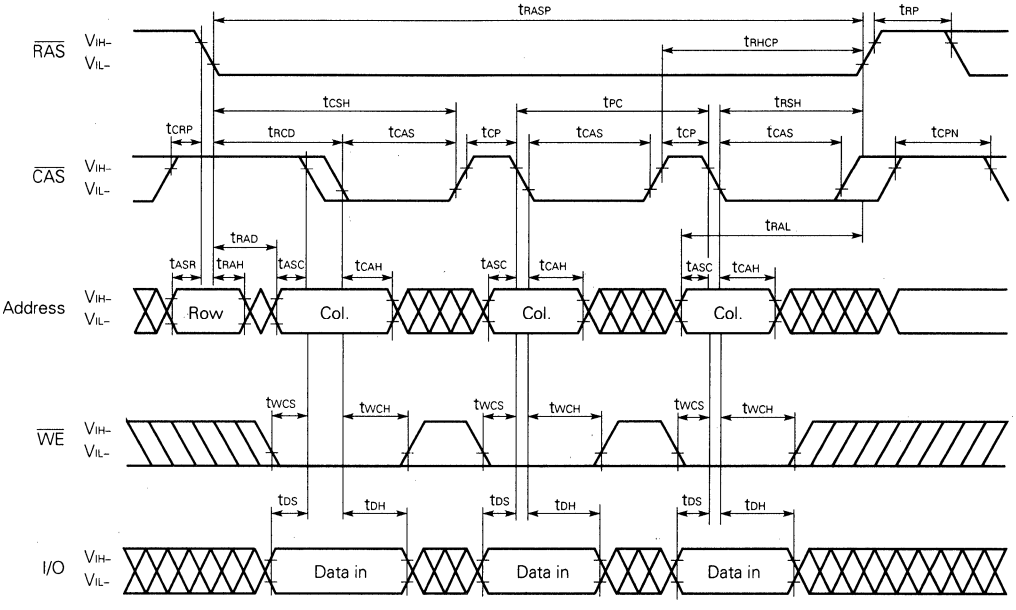


Fast Page Mode Read Cycle



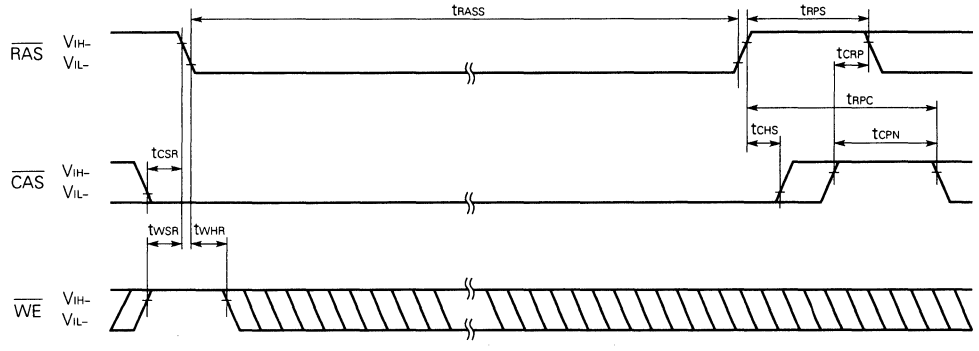
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Early Write Cycle



Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle



Remark Address : Don't care I/O : Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh

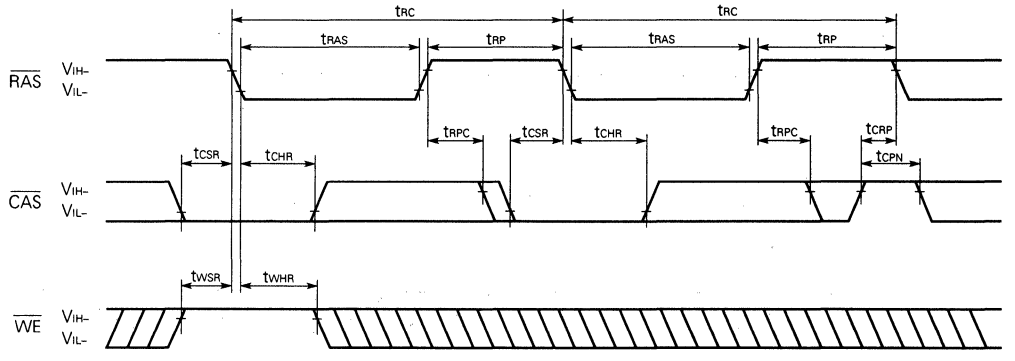
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 2,048 times within a 32 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh

When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 2,048 times within a 32 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

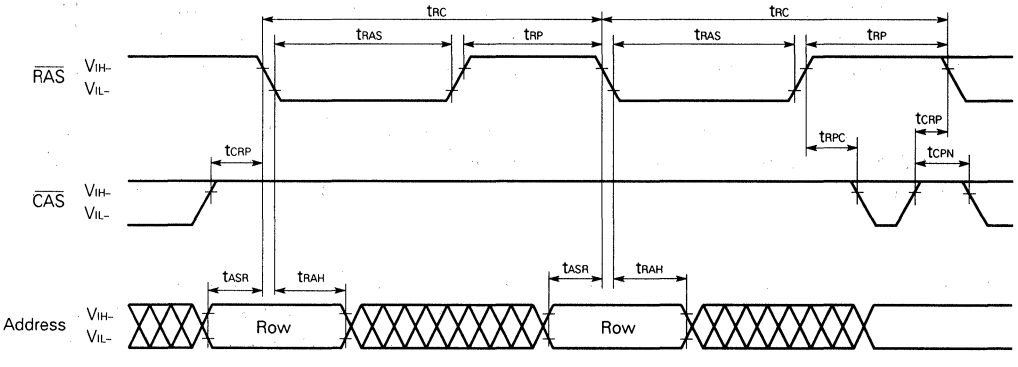
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



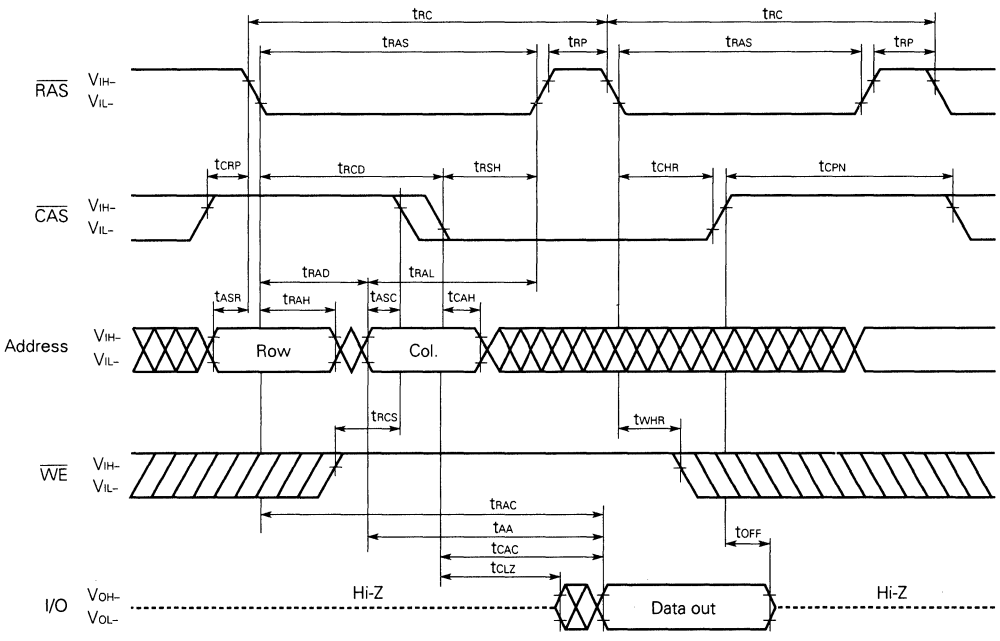
Remark Address : Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

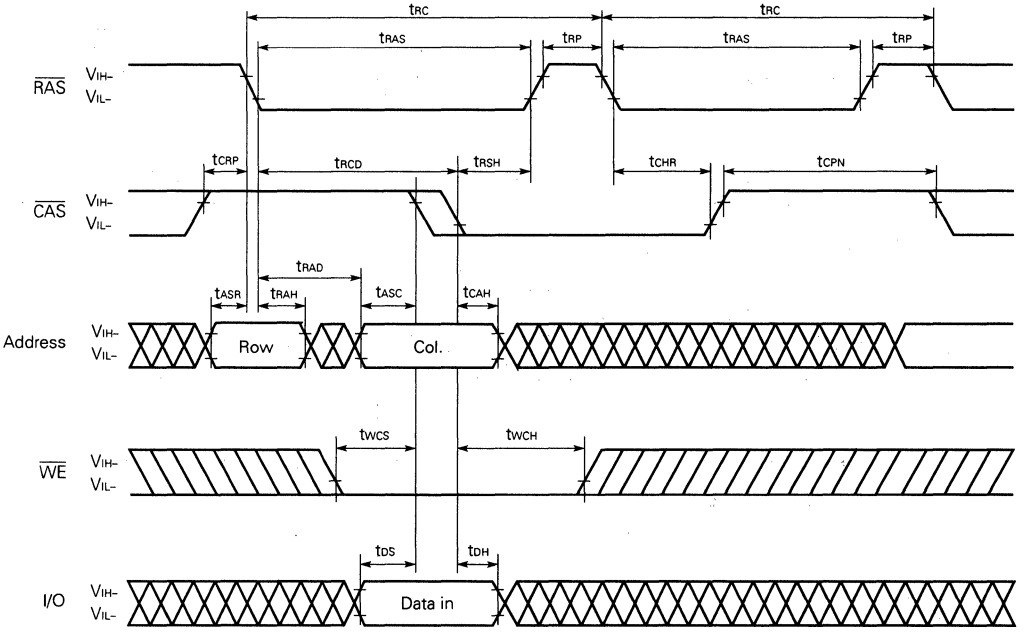


Remark $\overline{WE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

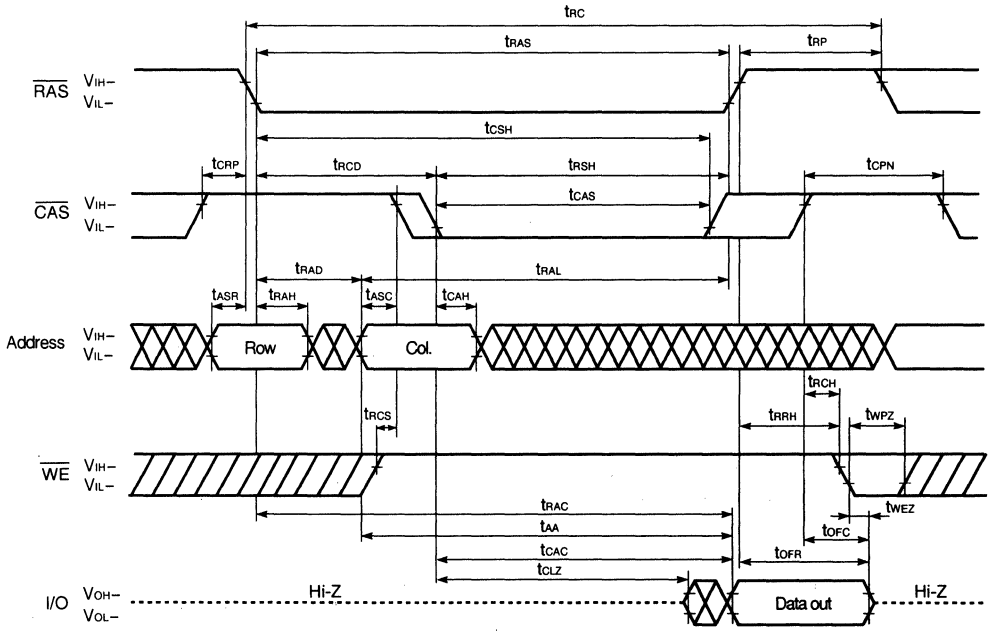


Hidden Refresh Cycle (Write)

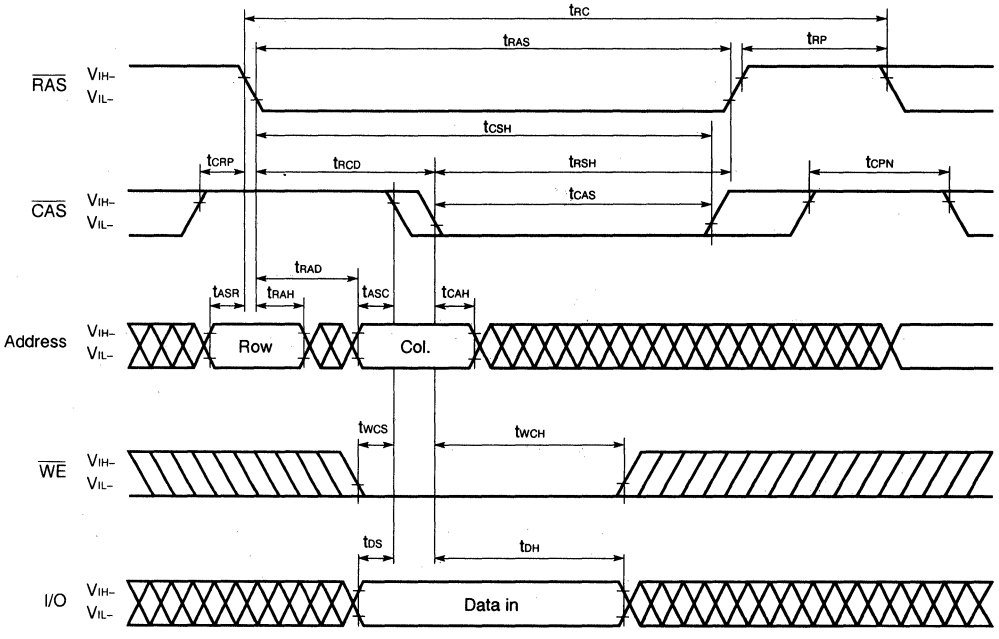


Timing Chart 7

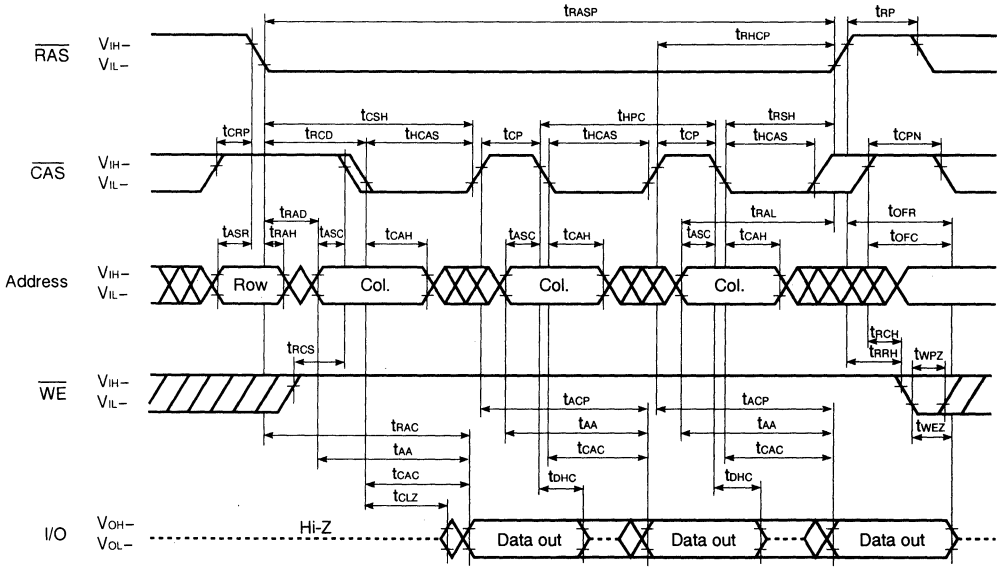
Read Cycle


tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
CAS
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
tWPZ
WE
tRAC
tAA
tWEZ
tOFC
tCAC
tOFR
tCLZ
I/O
VOH–
VOL–
Hi-Z
Data out
Hi-Z

Early Write Cycle

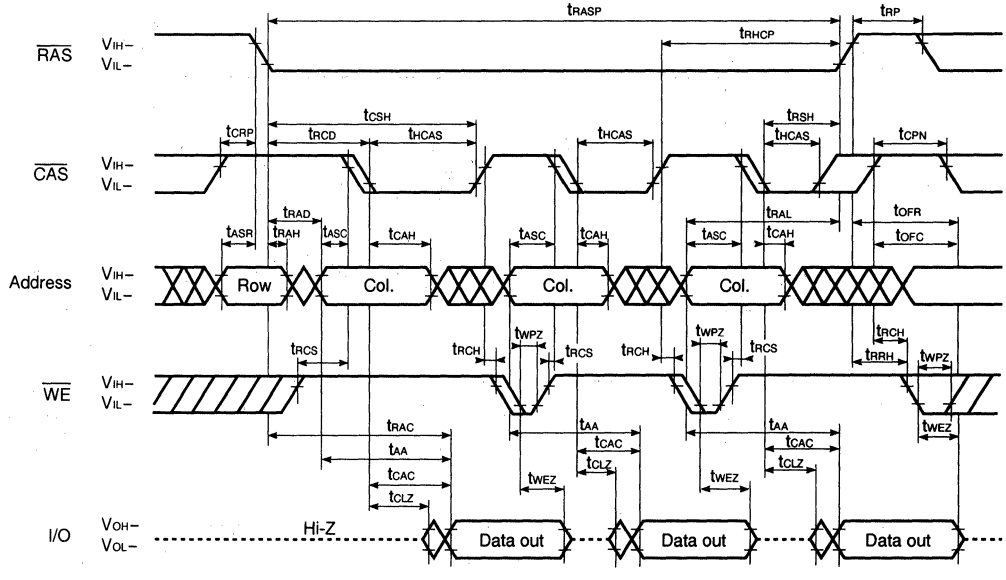


Hyper Page Mode (EDO) Read Cycle



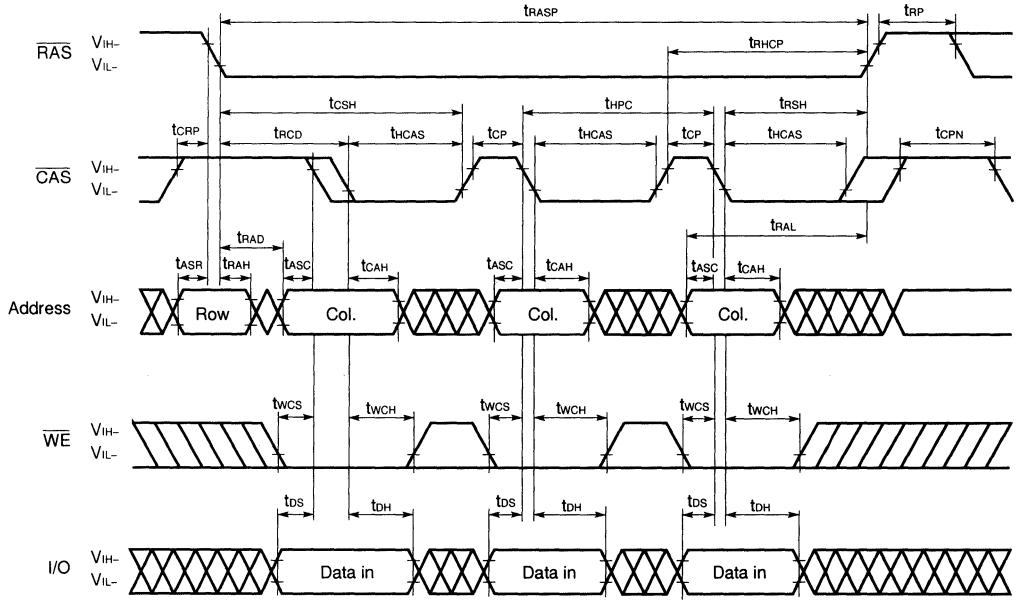
Remark In the hyper page mode (EDO), read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{WE}$ Control)



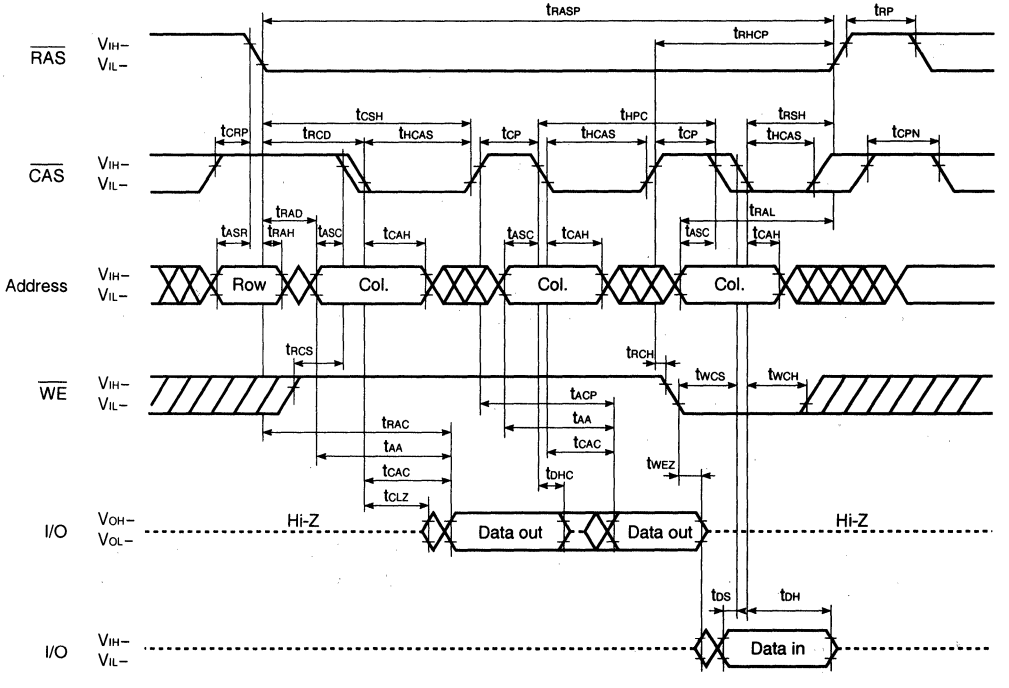
Remark In the hyper page mode (EDO), read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Early Write Cycle



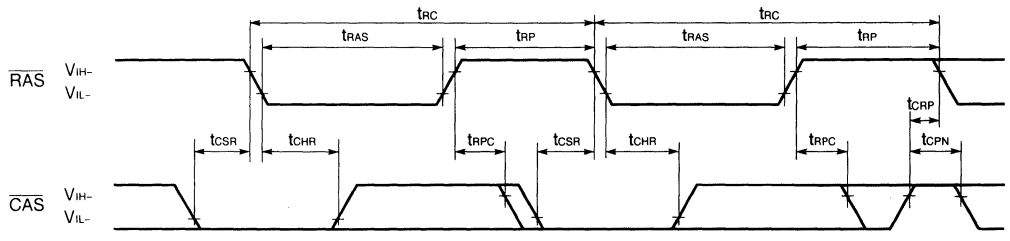
Remark In the hyper page mode (EDO), read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read and Write Cycle



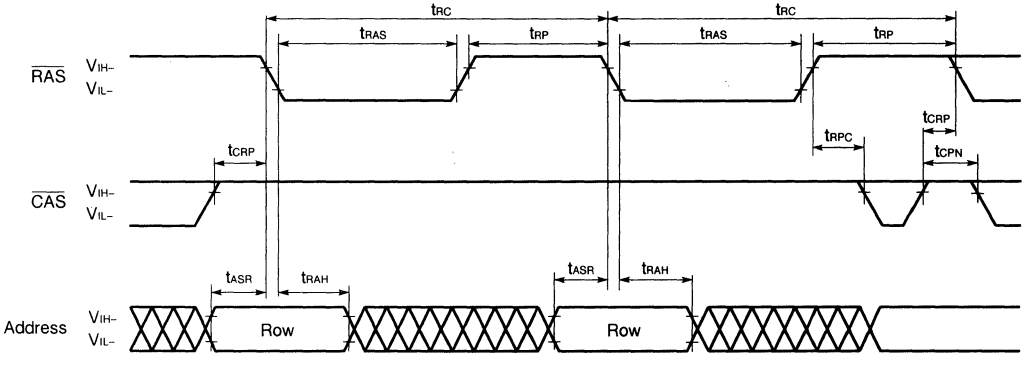
Remark In the hyper page mode (EDO), read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



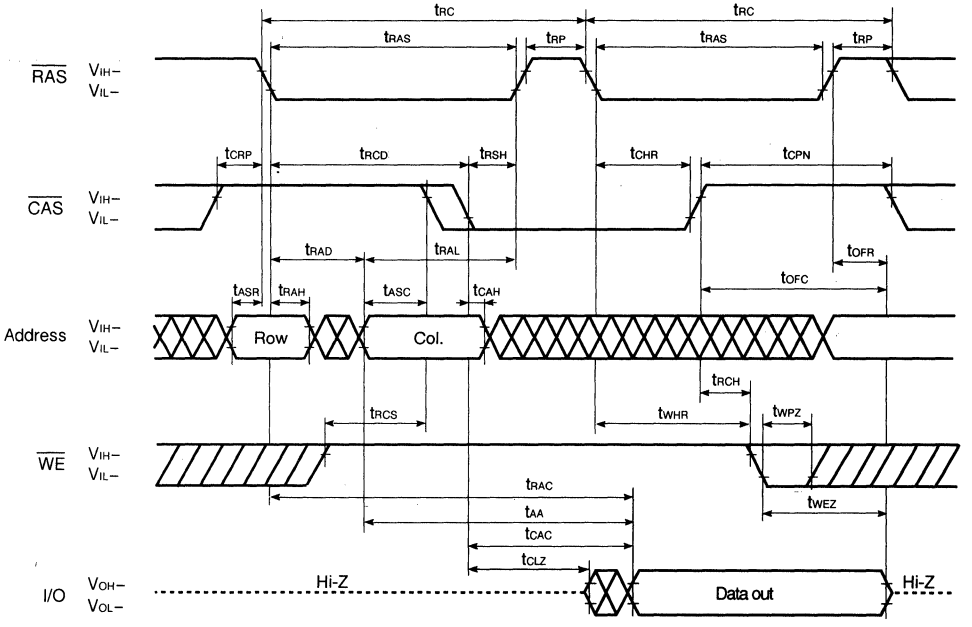
Remark Address, $\overline{WE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

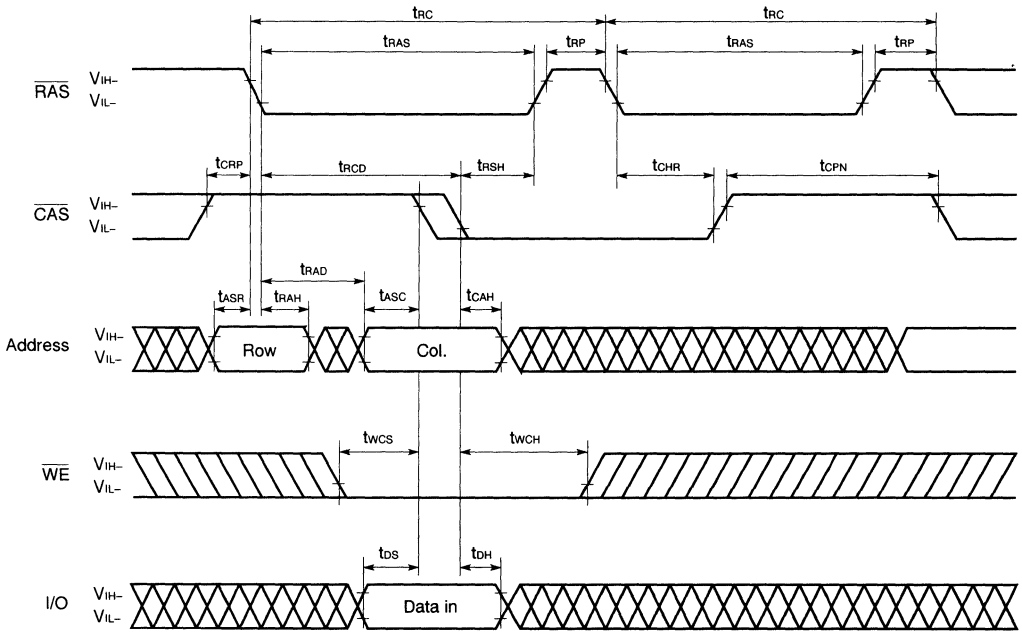


Remark $\overline{WE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

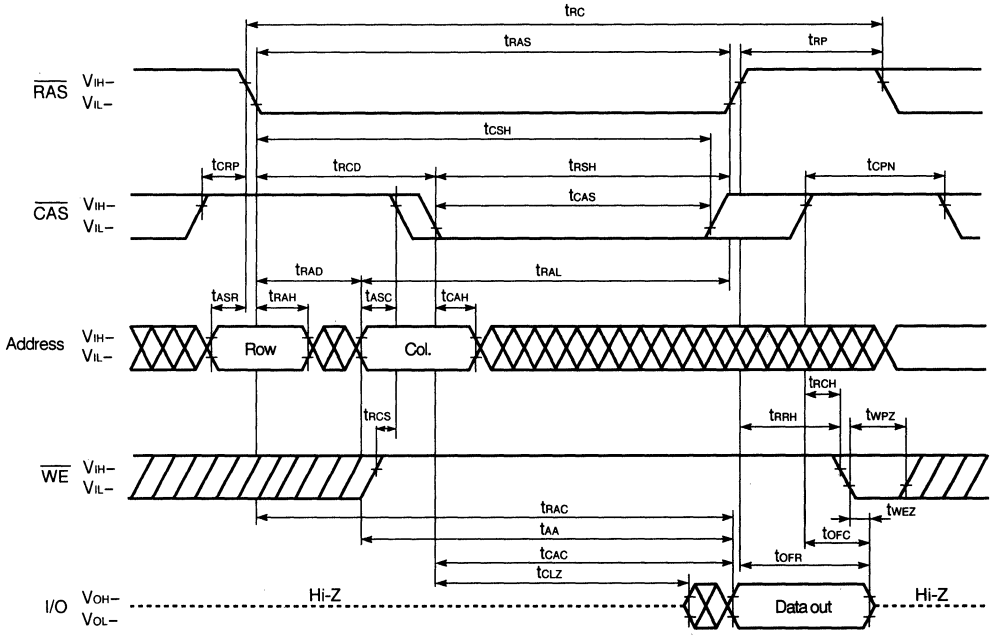


Hidden Refresh Cycle (Write)

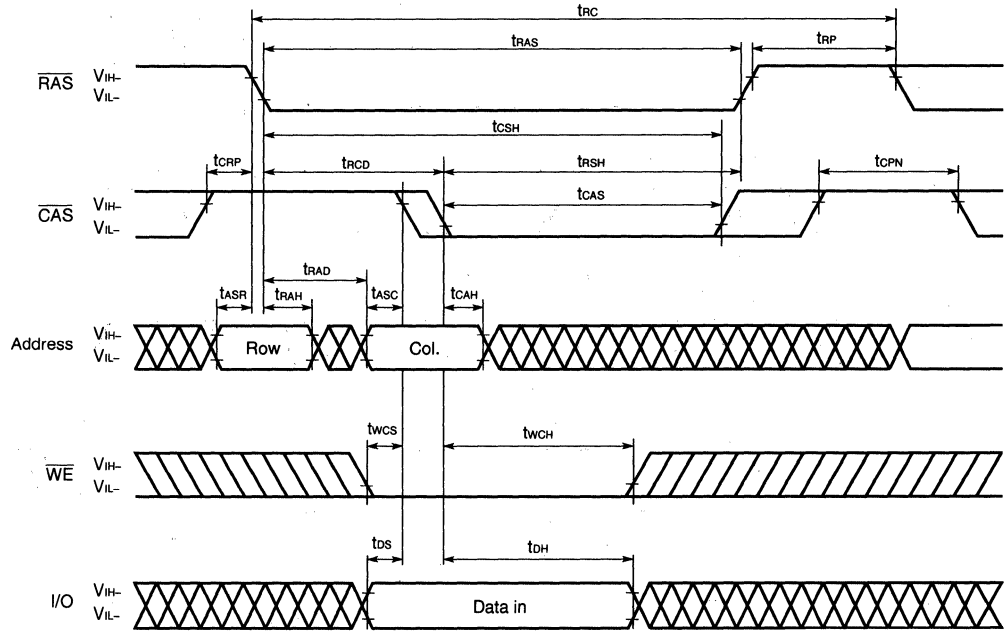


Timing Chart 8

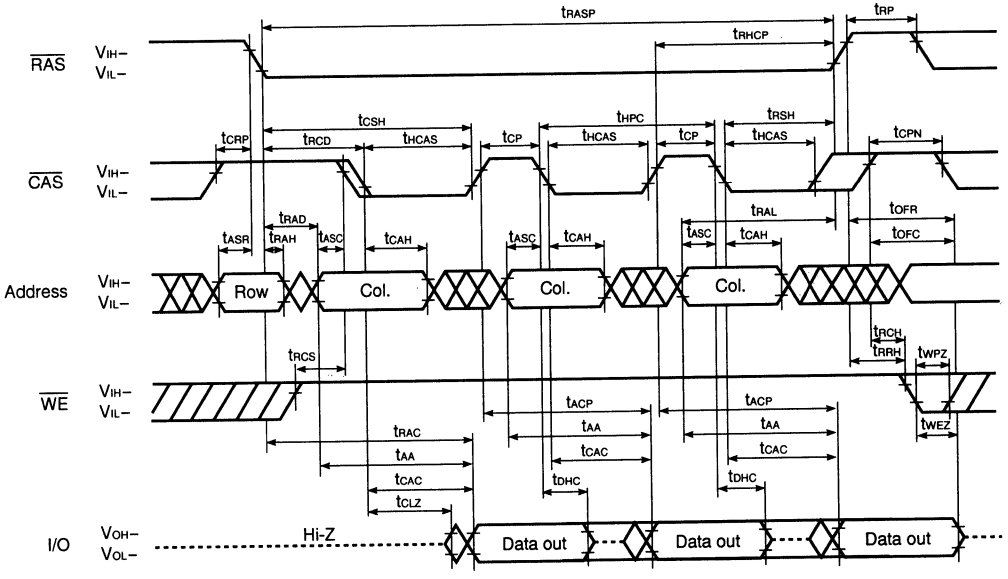
Read Cycle


tRC
tRAS
tRP
RAS VIH– VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
CAS VIH– VIL–
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address VIH– VIL–
Row
Col.
tRCH
tRCS
tRRH
tWPZ
WE VIH– VIL–
tRAC
tAA
tWEZ
tOFC
tCAC
tOFR
tCLZ
I/O VOH– VOL–
Hi-Z
Data out
Hi-Z

Early Write Cycle

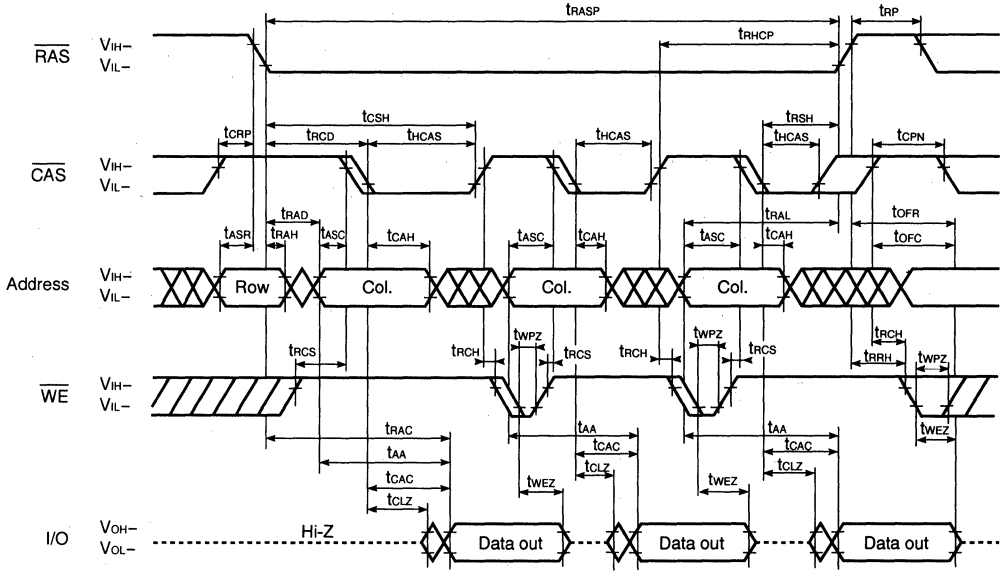


Hyper Page Mode (EDO) Read Cycle



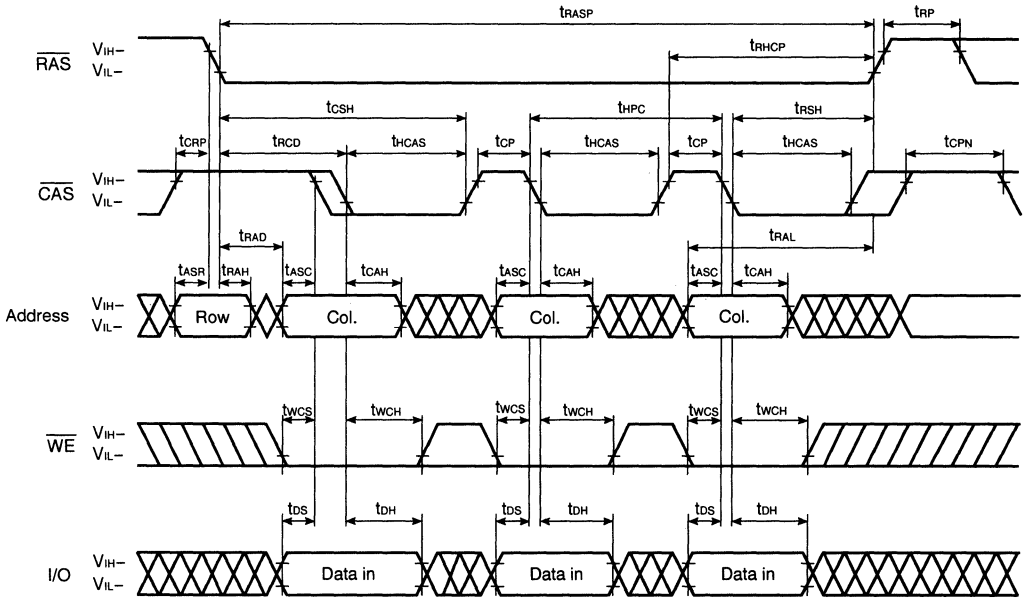
Remark In the hyper page mode (EDO), read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{WE}$ Control)



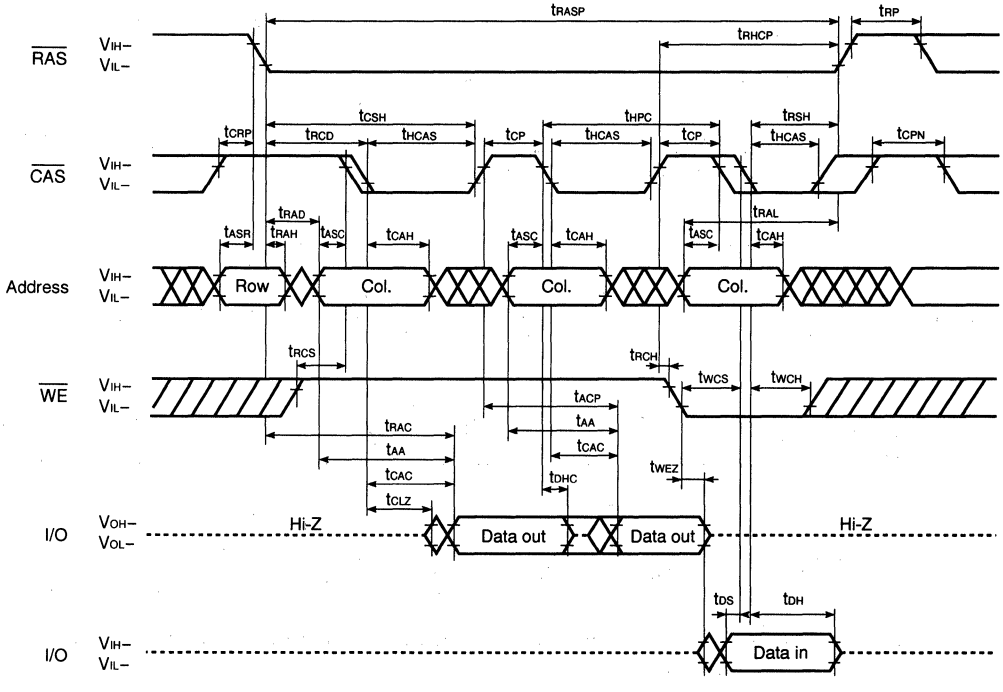
Remark In the hyper page mode (EDO), read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Early Write Cycle



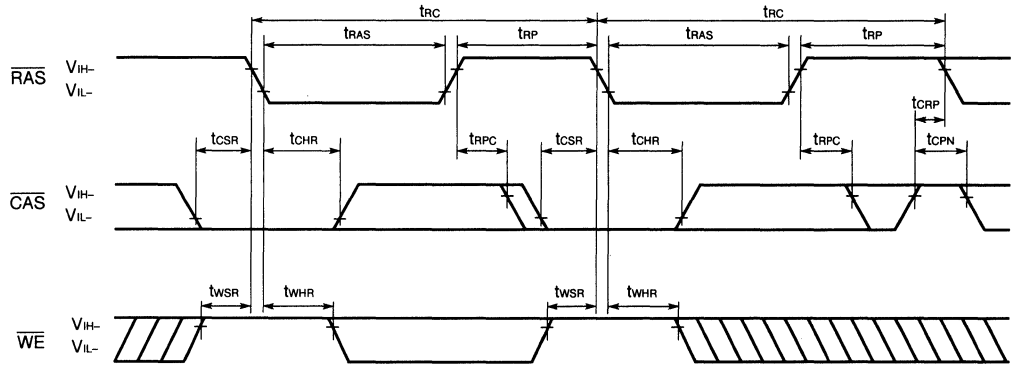
Remark In the hyper page mode (EDO), read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read and Write Cycle



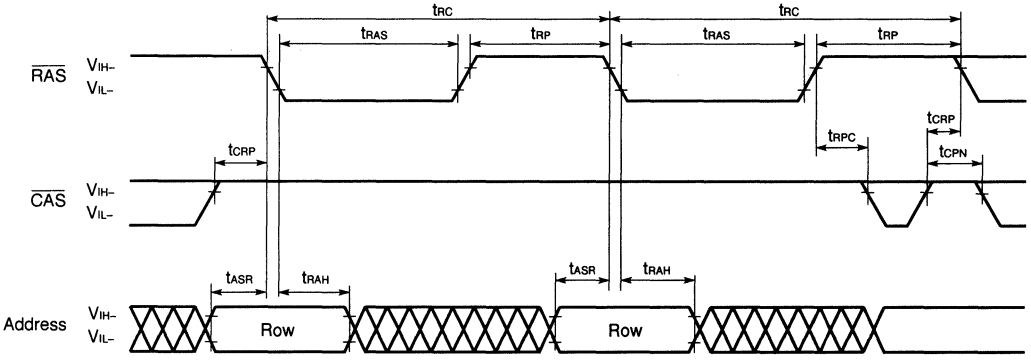
Remark In the hyper page mode (EDO), read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



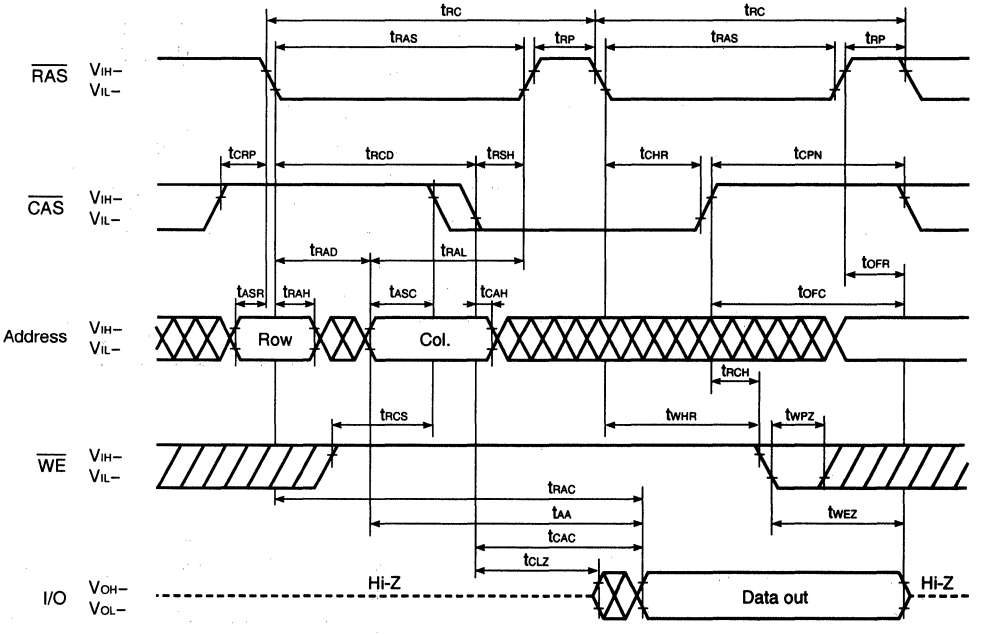
Remark Address: Don't care I/O: Hi-Z

RAS Only Refresh Cycle

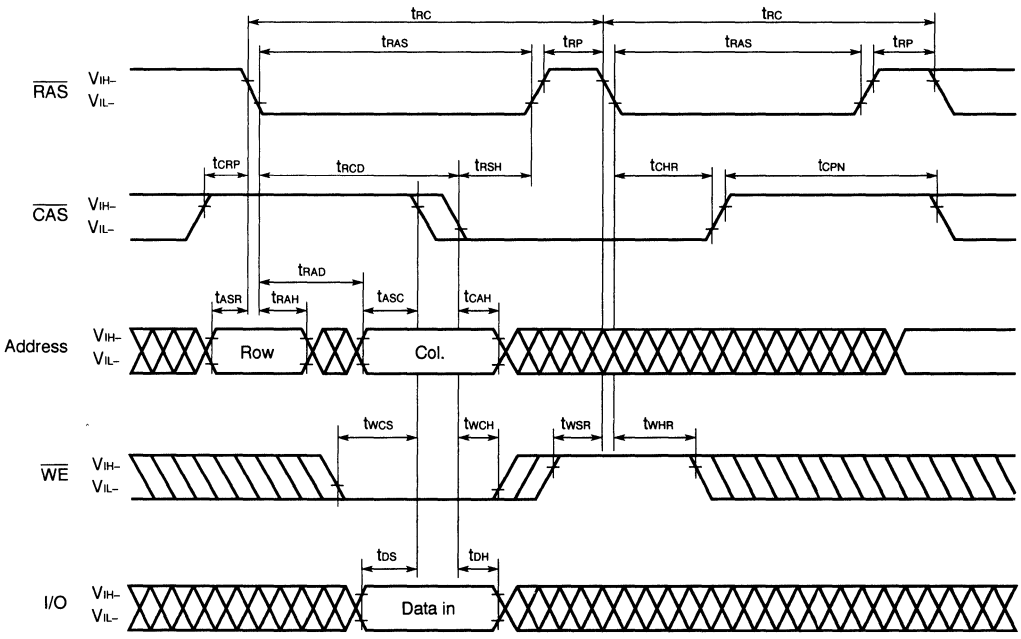


Remark $\overline{\text{WE}}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

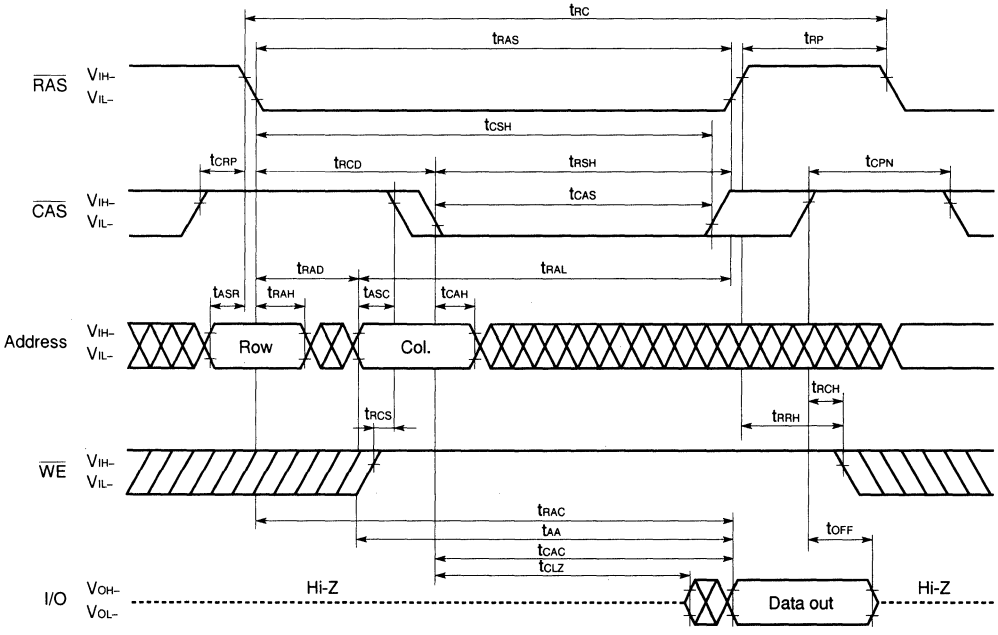


Hidden Refresh Cycle (Write)

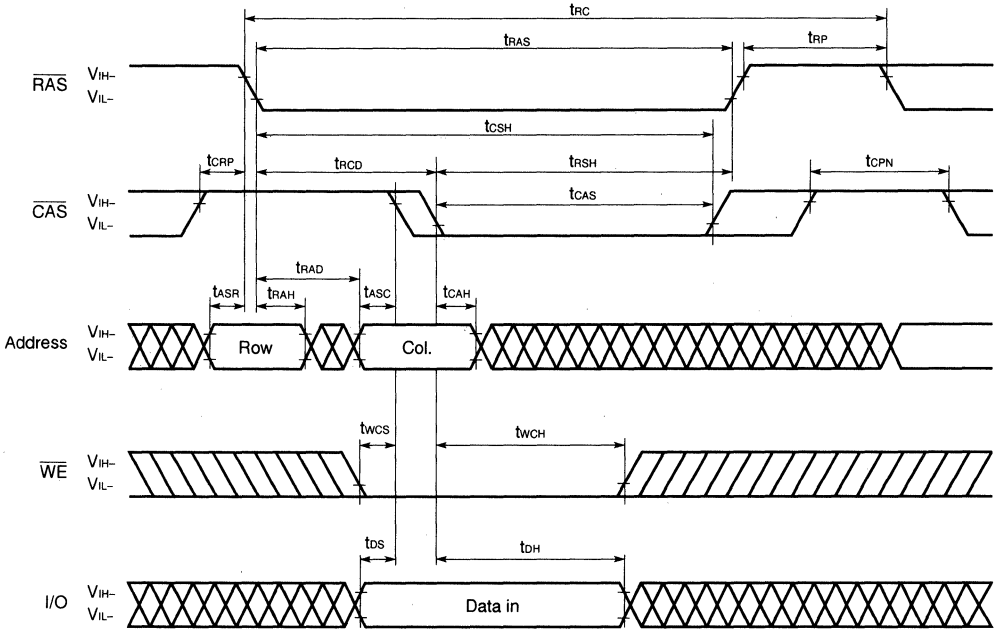


Timing Chart 9

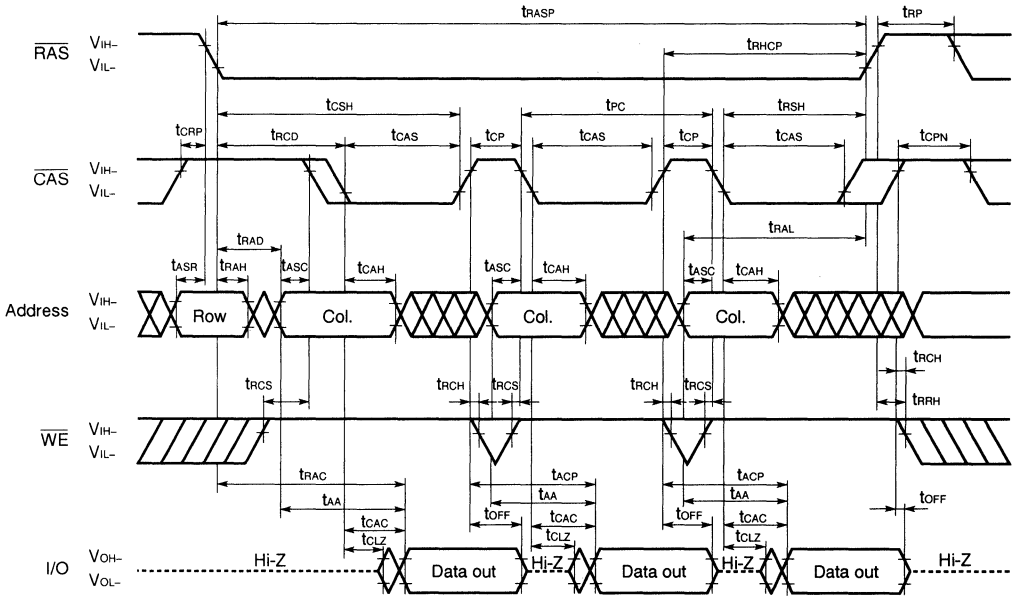
Read Cycle


tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
CAS
VIH–
VIL–
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
VIH–
VIL–
Row
Col.
tRCH
tRCS
tRRH
WE
VIH–
VIL–
tRAC
tAA
tOFF
tCAC
tCLZ
I/O
VOH–
VOL–
Hi-Z
Data out
Hi-Z

Early Write Cycle

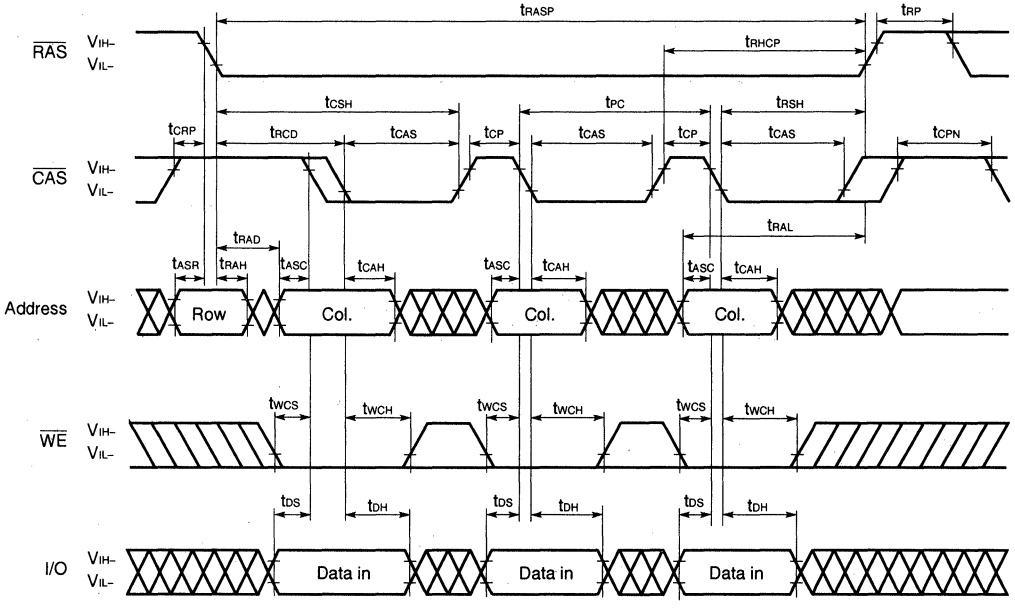


Fast Page Mode Read Cycle



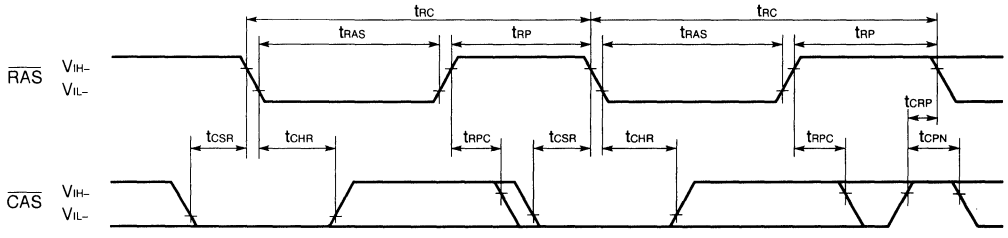
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Early Write Cycle



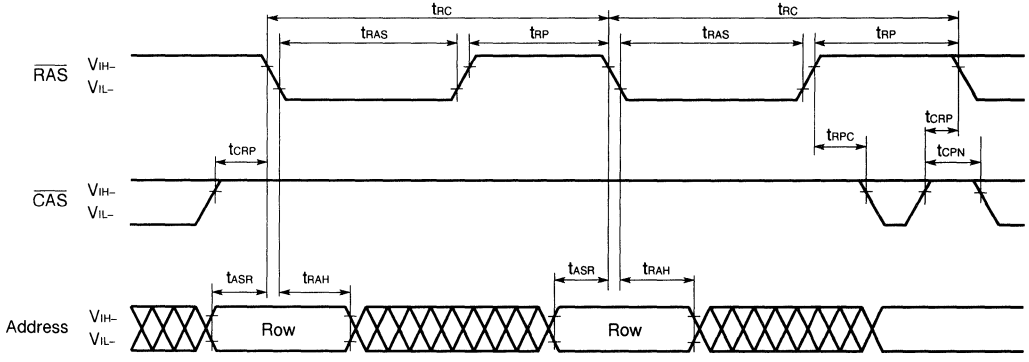
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



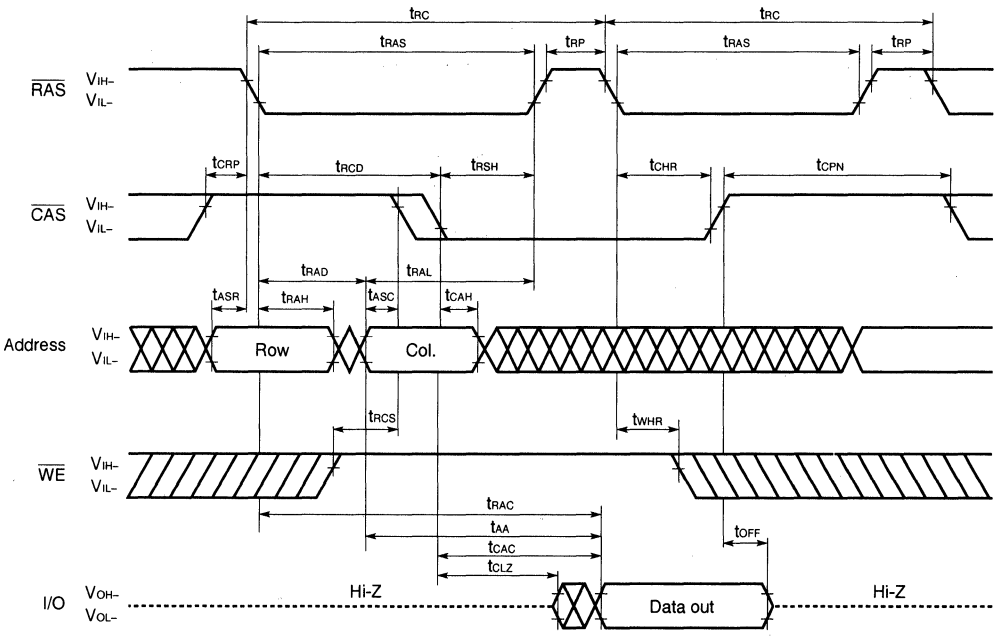
Remark Address, $\overline{WE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

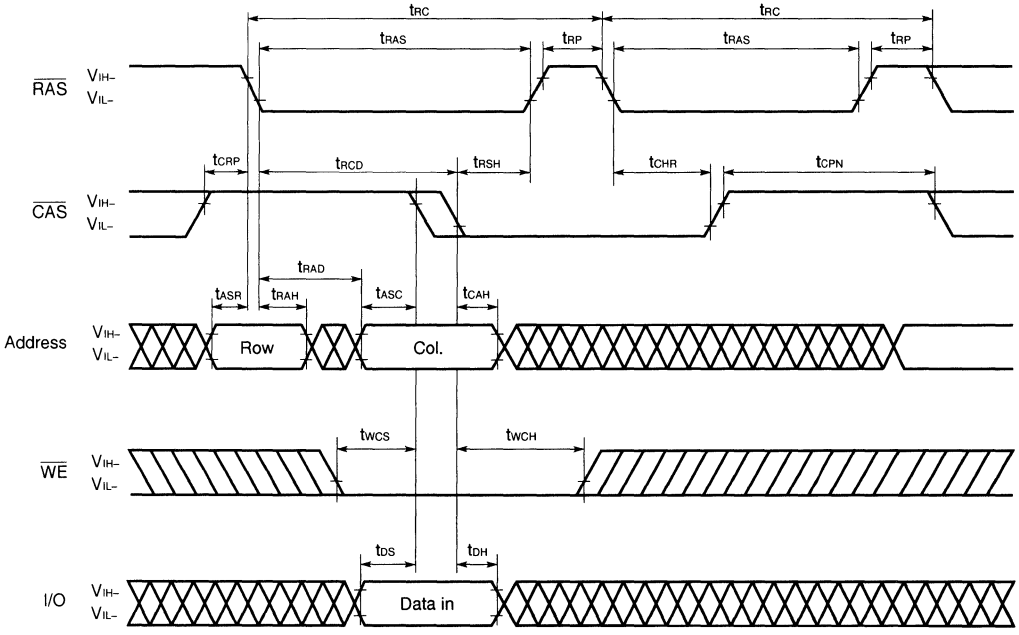


Remark $\overline{WE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

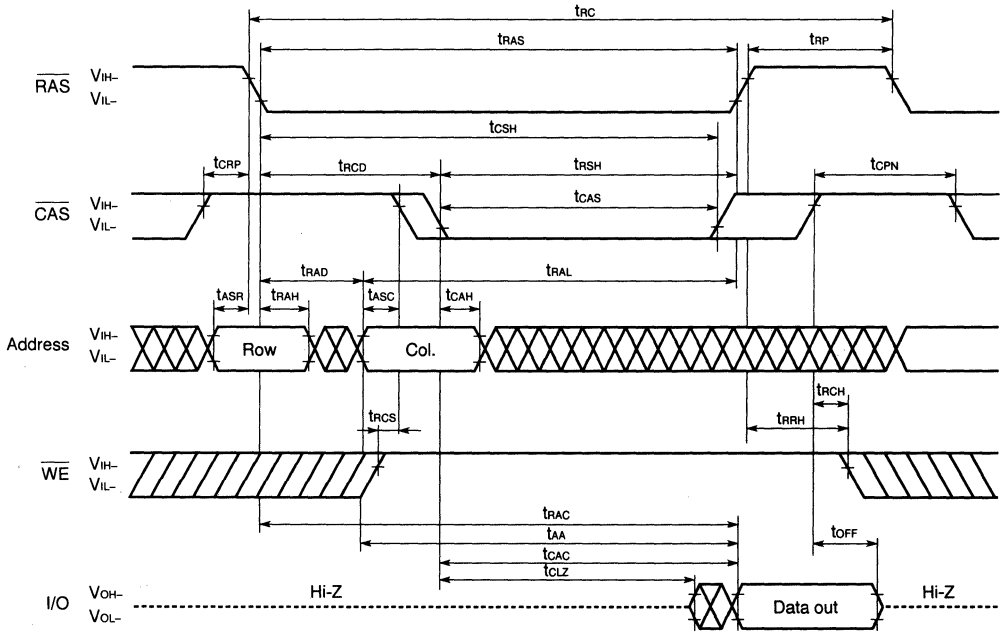


Hidden Refresh Cycle (Write)

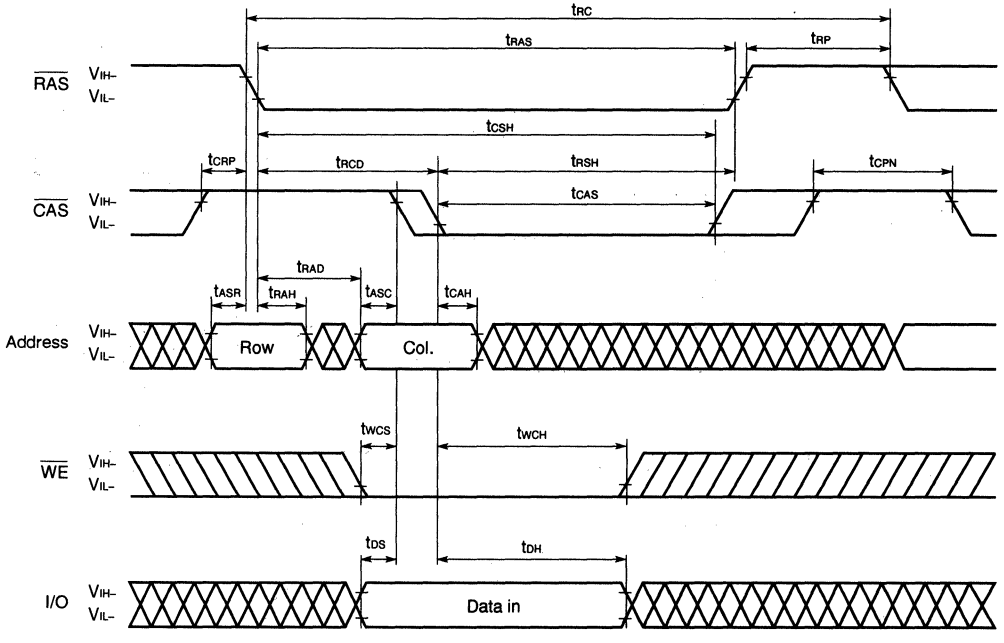


Timing Chart 10

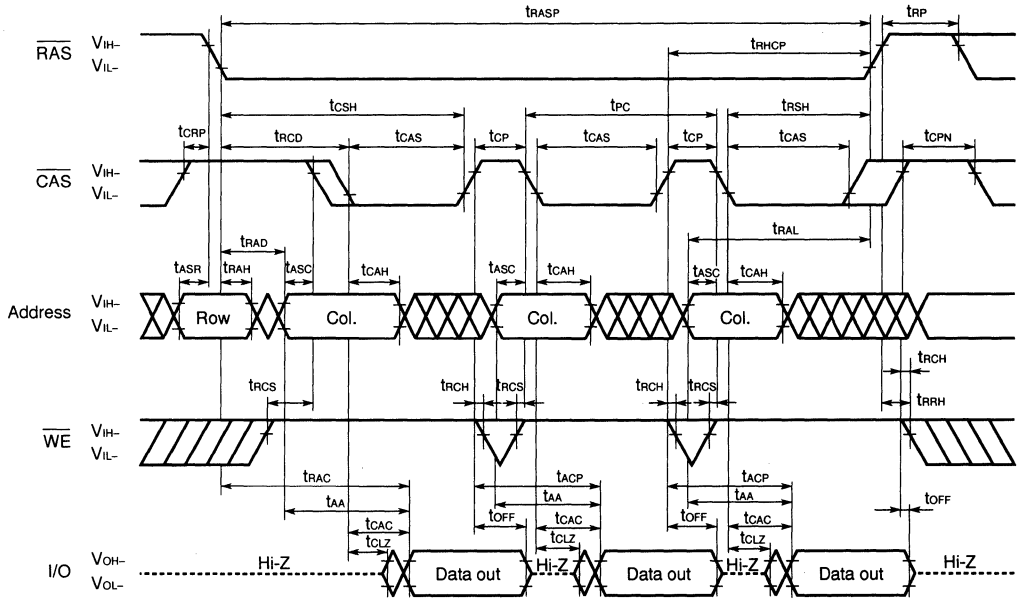
Read Cycle


tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
CAS
VIH–
VIL–
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
VIH–
VIL–
Row
Col.
tRCH
tRCS
tRRH
WE
VIH–
VIL–
tRAC
tAA
tOFF
tCAC
tCLZ
I/O
VOH–
VOL–
Hi-Z
Data out
Hi-Z

Early Write Cycle

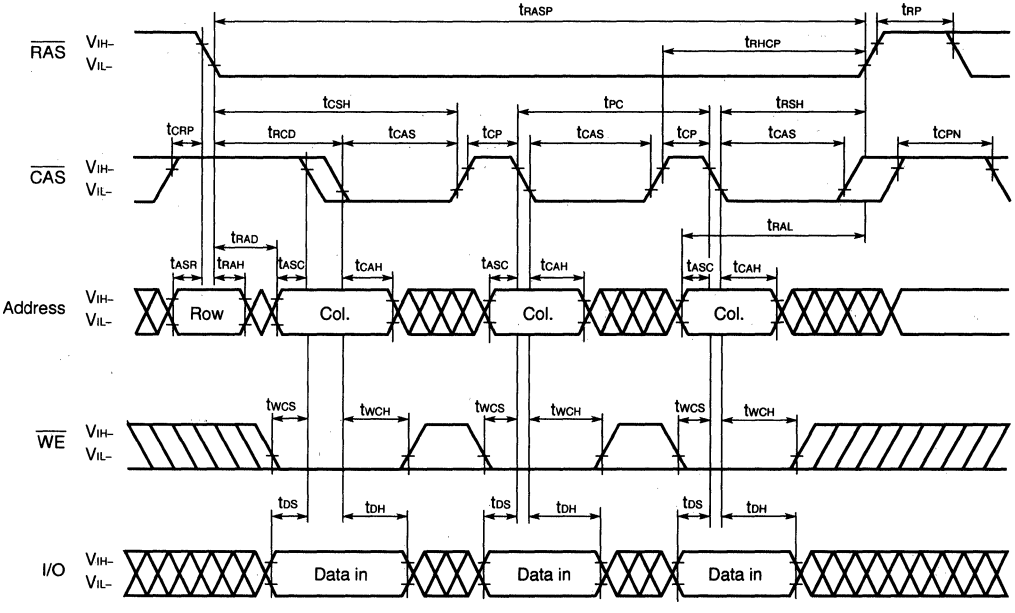


Fast Page Mode Read Cycle



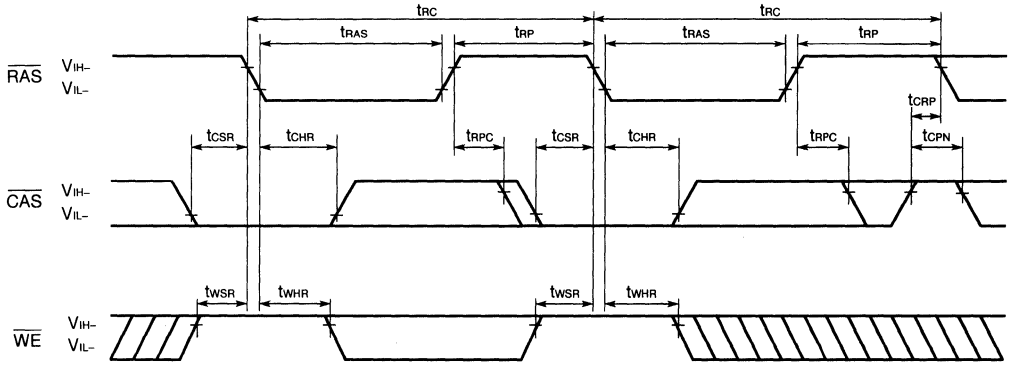
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Early Write Cycle



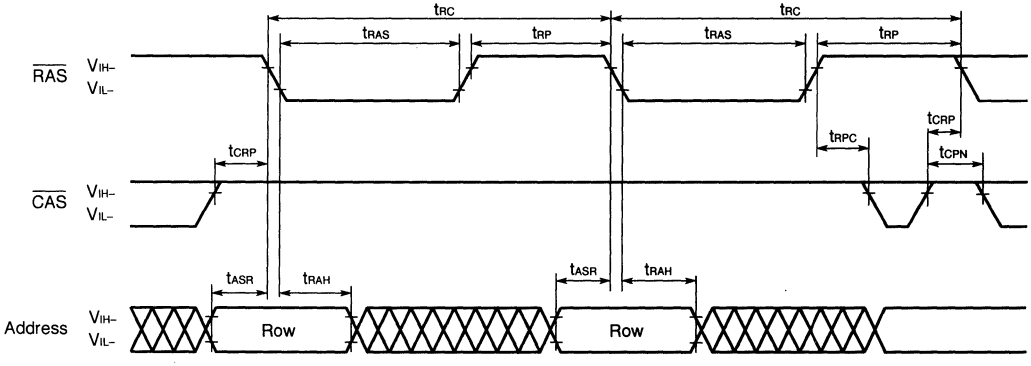
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



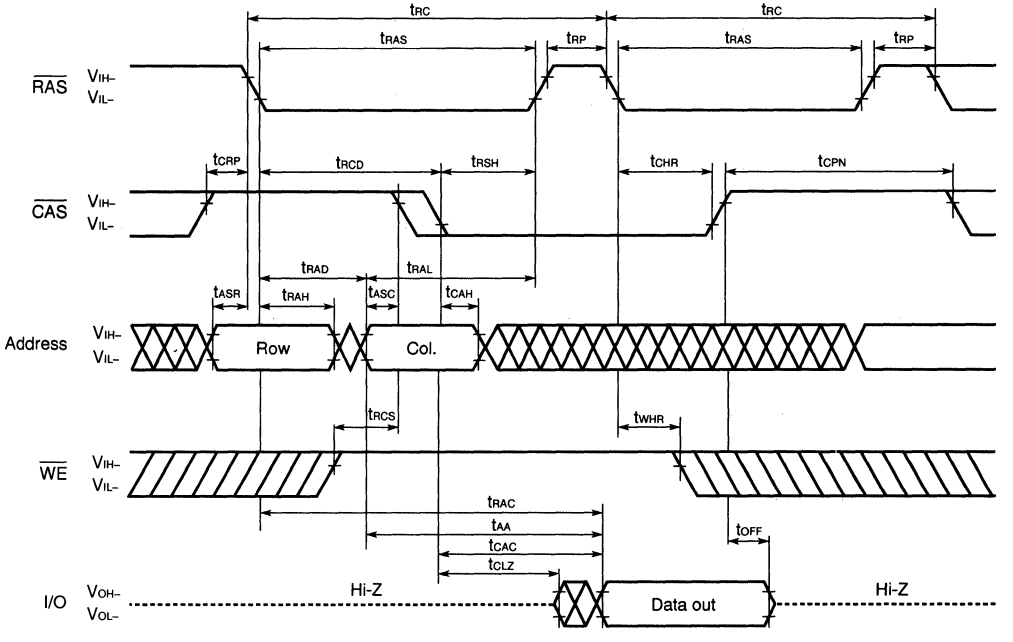
Remark Address: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

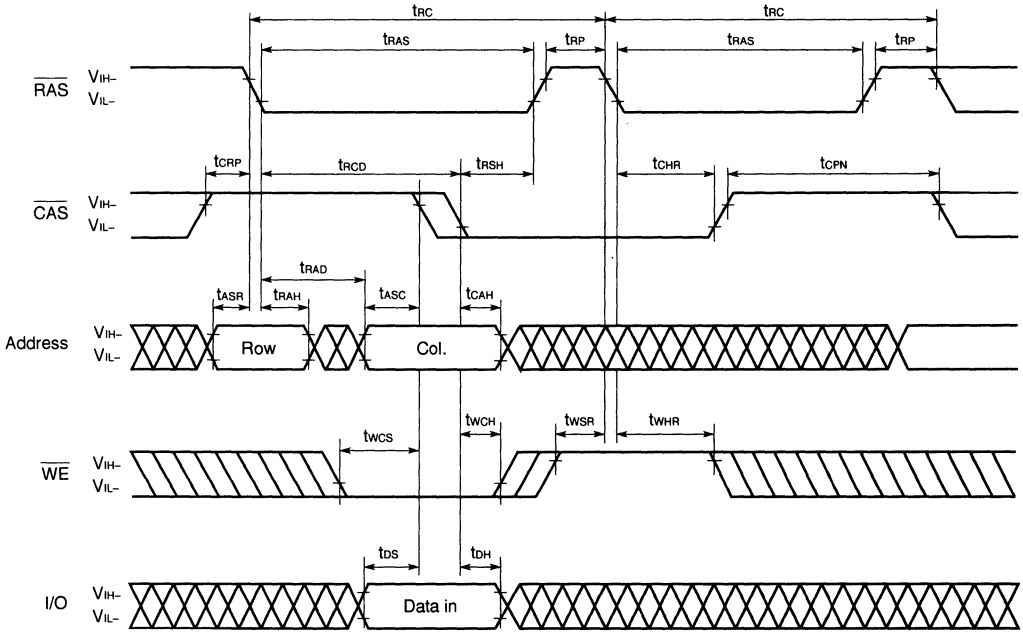


Remark $\overline{WE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)



How to Use DRAM

USER'S MANUAL

NEC

HOW TO USE DRAM

Document No. M10339EJ2V0UMU1

[MEMO]

INTRODUCTION

Purpose

This manual is intended for users who understand DRAM functions and design application systems using DRAMs.

Readers

This manual explains the basic properties of DRAM and their use.

How to read this manual

It is assumed that readers of this manual have general knowledge in the fields of electricity, logic circuits, and memory. For further details on the functions of each device, please refer to their data sheets.

DRAM devices can be divided into 5.0-V and low-voltage operation devices. This manual concentrates on 5.0-V operation devices (For information on low-voltage operation devices, see **CHAPTER 10 LOW VOLTAGE OPERATION**).

This manual uses the following abbreviations for refresh functions:

$\overline{CAS}$ before $\overline{RAS}$ refresh	→ CRB refresh
$\overline{CAS}$ before $\overline{RAS}$ long refresh	→ CBR long refresh
$\overline{CAS}$ before $\overline{RAS}$ self refresh	→ CBR self refresh
$\overline{RAS}$ only refresh	→ ROR
Long $\overline{RAS}$ only refresh	→ Long ROR

Legend

Active low	: $\overline{XXX}$ (top bar over pin or signal name)
Note	: Footnote
Caution	: Points to be noted
Remark	: Supplementary explanations for main text
Numeric representations	: decimal ... xxxx

Related documents

Document related to the μPD4216100

- μPD4216100, 4217100 Data Sheet (IC-2923)

Document related to the μPD4216400

- μPD42S16400, 4216400, 42S17400, 4217400 Data Sheet (IC-2922)

Document related to the μPD42S16160, 4216160, 42S18160

- μPD42S16160, 4216160, 42S18160, 4218160 Data Sheet (IC-3217)

Document related to the μPD42S16160L

- μPD42S16160L, 4216160L, 42S18160L, 4218160L Data Sheet (IC-3218)

Document related to the Hyper Page Mode (HPM)

- μPD4216165 Data Sheet (IC-3378)

[MEMO]

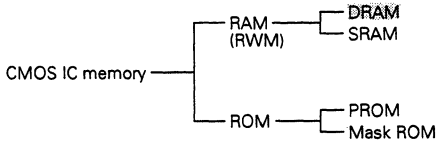
CHAPTER 1 DEFINITION OF DRAM

1.1 Classification of IC Memory

The CMOS IC memory can be divided into two main categories, namely RAM (RWM) and ROM (Read Only Memory).

Figure 1-1 shows the classification of the CMOS IC memory.

Figure 1-1. CMOS IC Memory Classification



(1) RAM (Random Access Memory)...RWM (Read Write Memory)

The RAM can be broadly divided into DRAM and SRAM (See **1.2 DRAM Features**). The RAM memory freely enables high-speed reading and writing.

The ROM also enables reading freely but the RAM generally enables both reading and writing freely. All data in the RAM are lost by turning off the power.

The DRAM can be further divided into conventional DRAM and high-speed DRAM. High-speed DRAM refers to synchronous DRAM and Rambus™ DRAM operating in synchronization with a clock and page access time enabling as compared with conventional DRAMs. This user's manual describes conventional DRAMs. See each user's manual for the details on the synchronous DRAM and Rambus DRAM.

(2) ROM (Read Only Memory)

The ROM can be broadly divided into PROM and mask ROM. It is a memory exclusively used for reading only. Data contained in ROM are retained even if the power is turned off.

As its name indicates, the ROM (Read Only Memory), once written, can be read only and hence cannot be generally rewritten. However, some PROM (Programmable ROM) can be rewritten.

1.2 DRAM Features

The DRAM has the following features:

(1) Memory cell structure = 1 transistor + 1 capacitor → Large density easily provided
(2) Refreshing required
(3) Address multiplex method

The following explains the features (1) to (3) of DRAM in comparison with the SRAM.

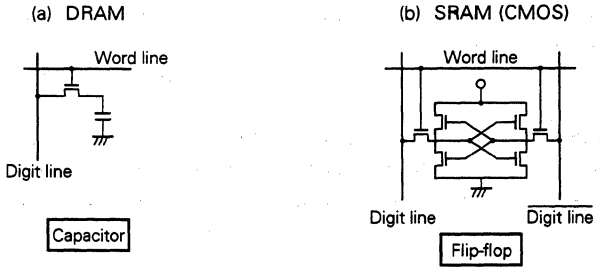
(1) Memory cell structure

The memory cell stores one-bit data. One 16M DRAM has 16,777,216 (2^{24}) memory cells. Figure 1-2 shows the memory cell structure of DRAM and SRAM.

The DRAM memory cell consists of one transistor and one capacitor and hence is highly integrated as compared with the SRAM in 6-transistor configuration.

The SRAM memory cell consists of flip-flops (in 6-transistor configuration) and does not use any capacitors.

Figure 1-2. Memory Cell



(2) Refresh operation

The DRAM uses capacitors in memory cells and hence must be refreshed.

The electric charge accumulated in DRAM capacitors tends to discharge little by little (leak) when left as it is. Therefore, data cannot be saved simply by providing power supply voltage.

Let us call the condition of a cell filled with electric charge as a "high level". If such a cell is left as is, the electric charge contained in the cell will be lost through leakage and the cell will change to the low level. The high level must always be maintained to retain data. Refreshing is the operation for constantly amplifying electric charge to retain data.

The SRAM does not use capacitors and hence does not require refreshing.

Caution **For some cells, the condition of a cell filled with electric charge is called "low level" and refreshing is also required for those cells to maintain the low level for the same reason explained above.**

(3) Address multiplex method

Figure 1-3 shows a diagram of the address multiplex method.

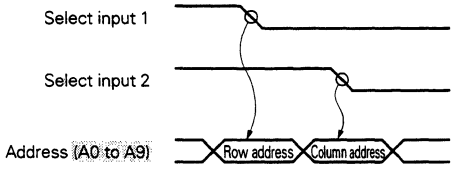
The address multiplex method uses two select inputs. For example, if an address line requires 20 bits, these 20 bits are read in two packets of 10 bits each. By thus reducing in half the number of address pins, high integration and package miniaturization can be achieved.

The DRAM uses this address multiplex method. For this reason, it can be packaged more compactly than SRAM for an equal memory density.

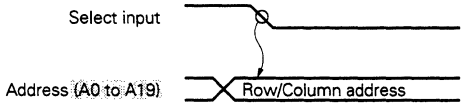
Although the SRAM does not use the address multiplex method, it enables easier timing design than DRAM as data can be transferred using one select input only.

Figure 1-3. Address Multiplex Method (for address line requiring 20 bits)

(a) DRAM type (address multiplex method)



(b) SRAM type (address non-multiplex method)



A comparison of DRAM features and other types of memories is shown in the table below.

Table 1-1. IC Memory Features

Feature \ Type	DRAM	SRAM	Mask ROM	EPROM	Flash Memory
Large density	◎	△	◎	○	◎
Compact package	◎	△	△	△	△
Data-retention capability	△	○	◎	◎	◎
Bit unit cost	◎	△	◎	△	○
Access time	○	◎	○	○	○

◎: excellent ○: very good △: lacking

[MEMO]

CHAPTER 2 WORD AND BIT ORGANIZATIONS

This chapter describes word and bit organizations using an example of 16M DRAM.

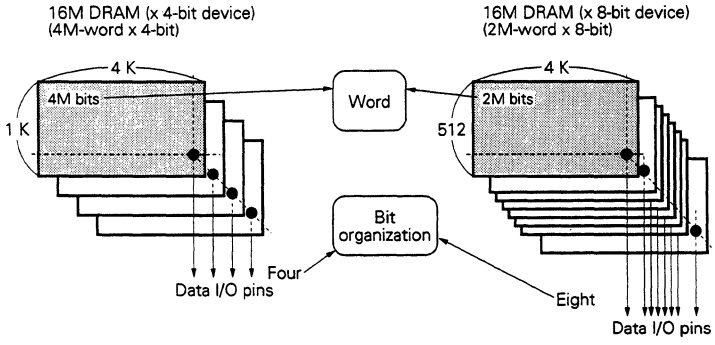
The word means a memory density controlled by one data I/O pin.

The bit organization means the number of data whose I/O can be controlled at one time. The x 4-bit device has four data I/O pins and can control I/O of four bits at one time. The x 8-bit device has eight data I/O pins and can control I/O of 8-bit data at one time. Therefore, word x bit organization forms an entire memory density.

For example, the memory density of 4M words x 1 bit is 4M bits and that of 4M words x 4 bits is 16M bits. The word x bit organization may be different for the same memory density.

The word and bit organization may be called depth and width, respectively, when Figure 2-1 is viewed from the side.

Figure 2-1. Simplified Block Diagram



When a certain address is defined, 4-bit and 8-bit data are selected for x 4-bit and x-8 bit organizations, respectively. Therefore, if there are address pins available for defining all words (x 4-bit device: 4M bits, x 8-bit device: 2M bits), the data of all addresses of memory can be selected.

Table 2-1. Number of Memory Cells and Number of Address Pins

Items / DRAM type	X axis		Y axis	
	Number of memory cells	Number of address pins	Number of memory cells	Number of address pins
16M DRAM (x 4-bit device)	4 K	12	1 K	10
16M DRAM (x 8-bit device)	4 K	12	512	9

Because the DRAM uses the address multiplex method, the number of address pins is 12 for both DRAMs in x 4-bit and x 8-bit organizations.

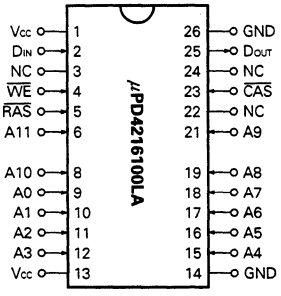
[MEMO]

CHAPTER 3 PIN FUNCTIONS

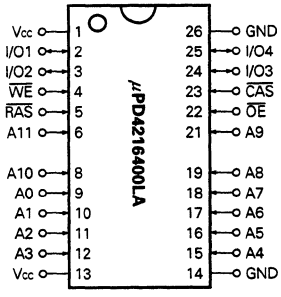
This chapter describes DRAM pin functions based on the μPD4216100 (16M-word x 1-bit device) and μPD4216400 (4M-word x 4-bit device).

3.1 Pin Configurations

(a) μPD4216100LA
(26-pin Plastic SOJ (300 mil))



(b) μPD4216400LA
(26-pin Plastic SOJ (300 mil))



3.2 Pin Functions (common to μPD4216100 and μPD4216400)

Pin name	I/O	Pin functions	Remark
$\overline{RAS}$: Row Address Strobe	In	Signal that activates chip and fetches row address	
$\overline{CAS}$: Column Address Strobe	In	Signal that fetches column address	
$\overline{WE}$: Write Enable	In	Signal enabling write	
VCC : Power Supply	–	Power supply voltage pin	
GND : Ground	–	Ground pin	
A0-A11 : Address	In	Address input pin	
DIN : Data Input	In	Data input pin	μPD4216100 only
DOUT : Data Output	Out	Data output pin	
$\overline{OE}$: Output Enable	In	Signal enabling output	μPD4216400 only
I/O1-I/O4 : Data Inputs/Outputs	I/O	Data I/O pin	
NC : No Connection	–	Not connected to internal memory	

3.3 Pin Function Explanation

The pin functions of $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and $\overline{OE}$ are explained below.

3.3.1 $\overline{RAS}$: Row address strobe

This is a signal that activates chips. When the $\overline{RAS}$ is activated, DRAM operation begins. When the $\overline{RAS}$ is activated, a row address is latched, the corresponding word line is selected, and the sense amplifier circuit is activated.

The sense amplifier circuit is used to amplify signals in the capacitor.

The $\overline{RAS}$ is activated when it is low. The "$\overline{\ }$" (bar) indicates that this signal is activated when it is low.

3.3.2 $\overline{CAS}$: Column address strobe

This signal fetches a column address, selects the digit line connected to the sense amplifier, and activates the data I/O circuit.

3.3.3 $\overline{WE}$: Write enable

When $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ are activated, write operation is enabled. Write operation is divided into two major groups.

- Early write : $\overline{WE}$ is activated before or at the same time $\overline{CAS}$ is activated.
- Late write : $\overline{WE}$ is activated after $\overline{CAS}$ is activated.

3.3.4 $\overline{OE}$: Output enable

This signal is used to switch between data input and output (for devices with multiple-bit organization only). The DRAM is divided as shown in Table 3-1 depending on the word and bit organization.

Table 3-1. DRAM Word x Bit Organization

	4M DRAM	16M DRAM
x1-bit device	4 M x 1	16 M x 1
Multiple-bit device	1 M x 4, 512 K x 8, 256 K x 16 etc.	4 M x 4, 2 M x 8, 1 M x 16 etc.

In multiple-bit devices, the I/O pin serve both as the input and output pins and therefore I/O switching signal (=$\overline{OE}$ signal) is required. In x 1-bit devices, $\overline{OE}$ is not required because the data input pins and data output pins are separate. The data I/O pins used for multiple-bit devices and x 1-bit devices are shown in Table 3-2.

Table 3-2. Data I/O Pins

	x 1-bit device	Multiple-bit device
Input pin	DIN	I/O1-I/On **Note**
Output pin	DOUT	

Note n = 4 : x 4-bit device
= 8 : x 8-bit device
= 16 : x 16-bit device

In multiple-bit devices, read operation is enabled when $\overline{OE}$ and then $\overline{RAS}$ and $\overline{CAS}$ are activated. At this time, when $\overline{WE}$ is activated, $\overline{OE}$ changes to 'don't care' in the memory and read operation is disabled. Therefore, read/write operation is enabled only through the control of $\overline{WE}$, with $\overline{OE}$ held active.

Remark In the read modify write cycle, data are output and input once each in one cycle. For details, see **4.3 Read Modify Write Cycle**.

3.4 Block Diagram

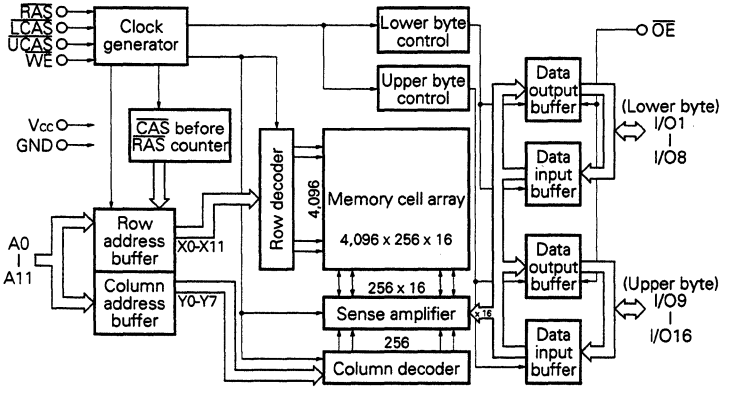
The following two types of DRAM block diagrams are shown.

μPD42S16160 (1M-word x 16-bit, 4,096 refresh)

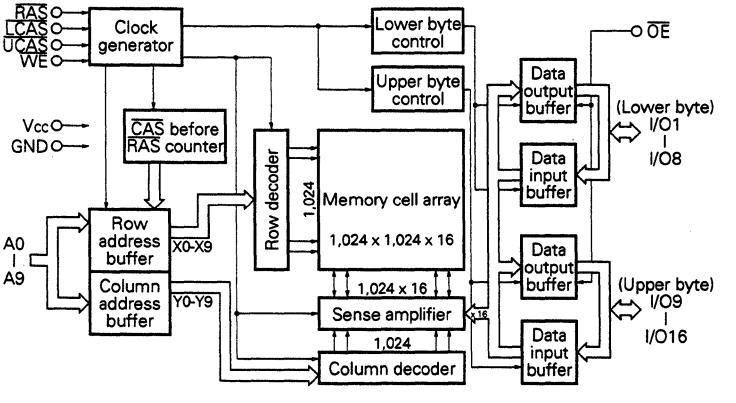
μPD42S18160 (1M-word x 16-bit, 1,024 refresh)

Figure 3-1. Block Diagram

(a) μPD42S16160 (1M-word x 16-bit, 4,096 refresh)



(b) μPD42S18160 (1M-word x 16-bit, 1,024 refresh)



3.4.1 Block diagram explanation

The block diagram is explained below.

(1) When $\overline{RAS}$ is activated:

When $\overline{RAS}$ is activated, the signal travels to the row decoder, latches a row address, selects the corresponding word line, and activates the sense amplifier. The $\overline{RAS}$ also enables activation of $\overline{CAS}$ (Signal priority is: $\overline{RAS}$>$\overline{CAS}$>$\overline{WE}$>$\overline{OE}$).

(2) When $\overline{CAS}$ is activated:

When $\overline{CAS}$ is activated, the signal travels to the column decoder, latches a column address, selects the corresponding digit line, and enables data I/O. The $\overline{CAS}$ also enables activation of $\overline{WE}$ and $\overline{OE}$.
The $\overline{UCAS}$ and $\overline{LCAS}$ control the upper and lower bytes, respectively, thus achieving control in units of bytes (See **CHAPTER 8 BYTE CONTROL**).
Also, when the $\overline{CAS}$ is activated before $\overline{RAS}$, the $\overline{CAS}$ before $\overline{RAS}$ counter is activated, thus automatically generating a row address.

(3) When $\overline{WE}$ is activated:

When $\overline{WE}$ is activated, data are input.

(4) When $\overline{OE}$ is activated:

When $\overline{OE}$ is activated and $\overline{WE}$ is inactivated, data are output.

[MEMO]

CHAPTER 4 OPERATION MODES

Operation modes can be generally divided into read and write. Read consists in extracting effective data from memory and write consists in inputting effective data into memory.

In this manual, a series of operations required for read operations is called read cycle and a series of operations for write operations is called write cycle. Before each operation mode is explained, legends used in timing charts are provided in Table 4-1.

Signal names listed higher in timing charts have precedence over ones listed lower ($\overline{RAS}$ > $\overline{CAS}$ > $\overline{WE}$ > $\overline{OE}$). If $\overline{WE}$ is low, $\overline{OE}$ is "don't care" in memory.

Table 4-1. Legend

Notation	Meaning
	Low or high level can be input and level can be changed from high to low or vice versa at any time. Input of undefined levels (neither high nor low) is prohibited.
	High level can be input and level can be changed from high to low at any time. However, low-to-high transition is prohibited.
	Low level can be input and level can be changed from low to high at any time. However, high-to-low transition is prohibited.
Don't care	Signals of all levels can be input. (Low, high, and undefined levels)
Hi-Z (High Impedance)	The output state is neither high nor low level.

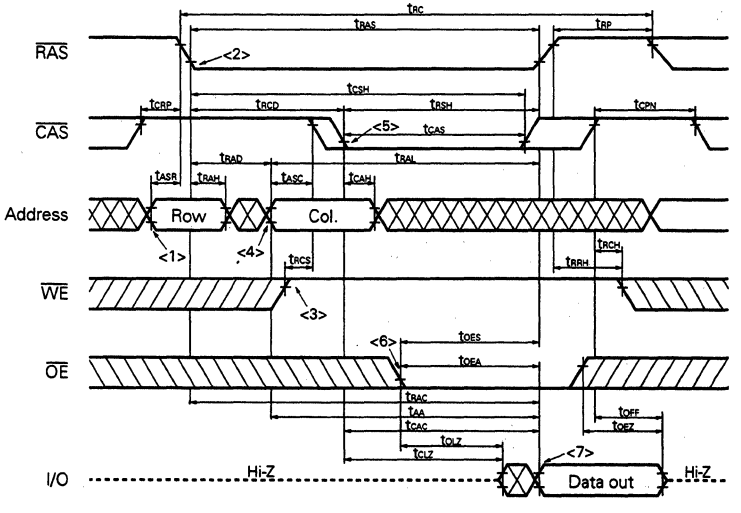
4.1 Read Operation

4.1.1 Read cycle

Read cycle is executed by activating $\overline{RAS}$ and then $\overline{CAS}$ while $\overline{WE}$ is not activated and $\overline{OE}$ is activated. The $\overline{RAS}$ latches row addresses and $\overline{CAS}$ latches column addresses.

Figure 4-1 shows the timing chart for the read cycle.

Figure 4-1. Read Cycle



<1> Defines row address.
<2> Activates $\overline{RAS}$ to latch row address.
<3> Inactivates $\overline{WE}$ to select read mode.
<4> Defines column address.
<5> Activates $\overline{CAS}$ to latch column address.
<6> Activates $\overline{OE}$ to enable output buffer.
<7> Start of data output.

$\overline{RAS}$	Active
$\overline{CAS}$	Active
$\overline{WE}$	Inactive
$\overline{OE}$	Active
I/O	Output

4.1.2 Access time

The effective access time in the read cycle varies depending on the conditions as shown in Table 4-2.

Table 4-2. Access Time in Read Cycle

	Input Conditions	Access Time	Access Time from $\overline{RAS}$
(1)	$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
(2)	$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
(3)	$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

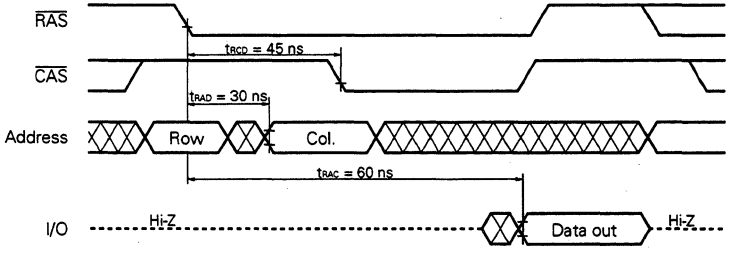
The $t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA}, or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

Assuming that the specification is as shown in Table 4-3, an example for Table 4-2 is shown below.

Table 4-3. Specification of a Certain Device (for read cycle)

	MIN.	MAX.	Unit
t_{RAD}	12	30	ns
t_{RCD}	14	45	
t_{RAC}	–	60	
t_{AA}	–	30	
t_{CAC}	–	15	

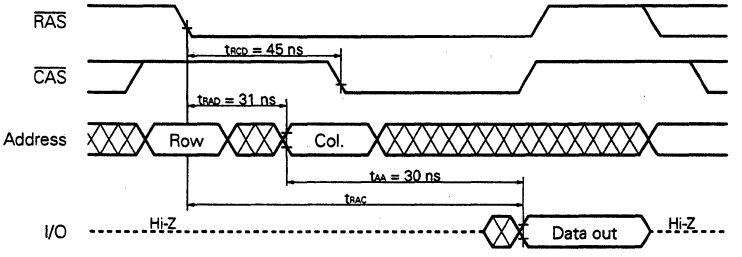
(1) When t_{RAC} becomes valid ($\overline{RAS}$ access):



Remark $\overline{WE}$: inactive, $\overline{OE}$: active

When t_{RAD} is equal to 30 ns and t_{RCD} is equal to 45 ns, t_{RAC} becomes valid. Data are output in 60 ns after the $\overline{RAS}$ is activated.

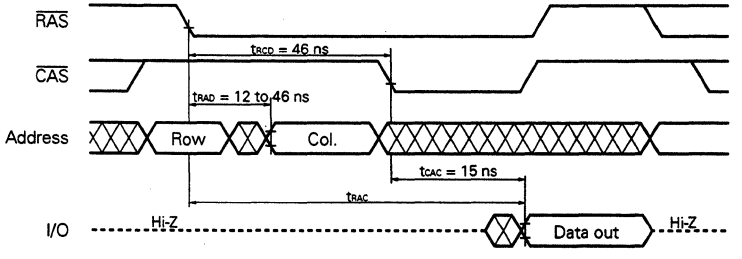
(2) When t_{AA} becomes valid (address access):



Remark $\overline{WE}$: inactive, $\overline{OE}$: active

When t_{RAD} is equal to 31 ns ($t_{RAD} > t_{RAD\ (MAX.)}$) and t_{RCD} is equal to 45 ns, t_{AA} becomes valid.
Therefore, data are output in 61 ns after $\overline{RAS}$ is activated.
The access time from $\overline{RAS}$ becomes ($t_{RAD} + t_{AA}$) and is delayed from $\overline{RAS}$ access.

(3) When t_{CAC} becomes valid ($\overline{CAS}$ access):



Remark $\overline{WE}$: inactive, $\overline{OE}$: active

The t_{CAC} becomes valid regardless of the value of t_{RAD} when t_{RCD} is equal to 46 ns ($t_{RCD} > t_{RCD\ (MAX.)}$) (the value of $t_{RAD\ (MIN.)}$ and address setup time need to be observed).
Therefore, data are output in 61 ns after $\overline{RAS}$ is activated.
The access time from $\overline{RAS}$ becomes ($t_{RCD} + t_{CAC}$) and is delayed from $\overline{RAS}$ access.

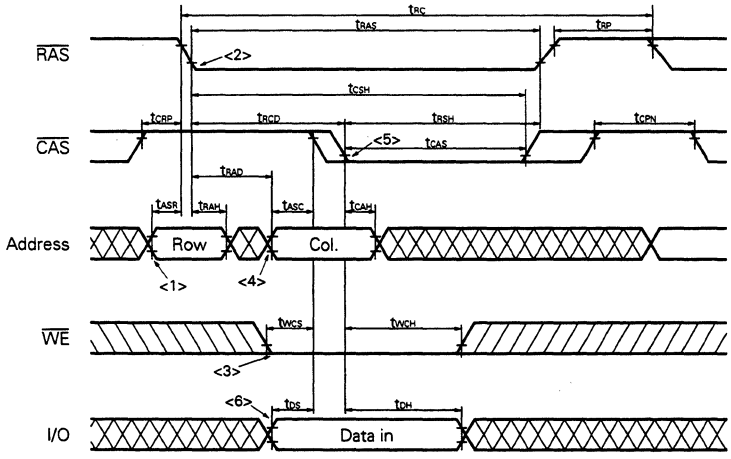
4.2 Write Operation

Write operation is enabled by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$.

4.2.1 Early write cycle

The early write cycle is executed by activating $\overline{WE}$ before or at the same time when $\overline{CAS}$ is activated.

Figure 4-2. Early Write Cycle



Remark $\overline{OE}$: don't care

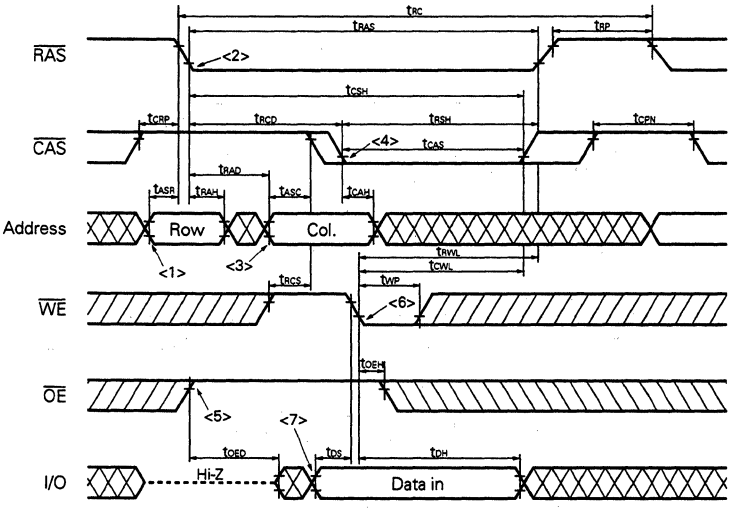
<1> Defines row address.
<2> Activates $\overline{RAS}$ to latch row address.
<3> Activates $\overline{WE}$ to enable input buffer.
<4> Defines column address.
<5> Activates $\overline{CAS}$ to latch column address.
<6> Sets input data.

$\overline{RAS}$	Active
$\overline{CAS}$	Active
$\overline{WE}$	Active
$\overline{OE}$	Don't care
I/O	Input

4.2.2 Late write cycle

The late write cycle is executed by activating $\overline{WE}$ after activating $\overline{CAS}$.

Figure 4-3. Late Write Cycle



<1> Defines row address.
<2> Activates $\overline{RAS}$ to latch row address.
<3> Defines column address.
<4> Activates $\overline{CAS}$ to latch column address.
<5> Inactivates $\overline{OE}$ to select write mode.
<6> Activates $\overline{WE}$ to enable input buffer.
<7> Sets input data.

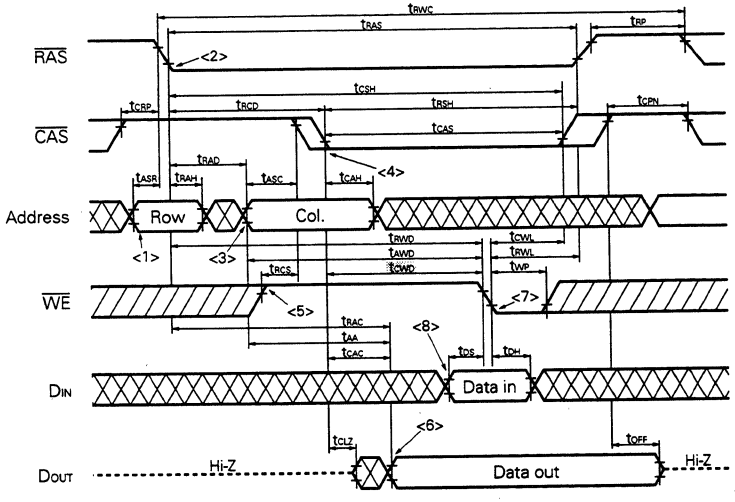
$\overline{RAS}$	Active
$\overline{CAS}$	Active
$\overline{WE}$	Active
$\overline{OE}$	Don't care
I/O	Input

4.3 Read Modify Write Cycle

Read modify write cycle is a cycle that outputs and inputs data from/to the same address during one cycle ($\overline{RAS}$/$\overline{CAS}$ cycle). Write is enabled by activating $\overline{WE}$ while $\overline{RAS}$ and $\overline{CAS}$ are active. Read is enabled by activating $\overline{OE}$ while $\overline{RAS}$ and $\overline{CAS}$ are active. Because x 1-bit devices do not have $\overline{OE}$, write and read operations are controlled by activating or inactivating $\overline{WE}$.

The timing charts of the read modify write cycles of x 1-bit and multiple-bit devices are shown in Figure 4-4 and Figure 4-5, respectively. In either case, if $\overline{WE}$ is activated after a delay from $\overline{CAS}$ that exceeds $\overline{CAS}$-$\overline{WE}$ delay time ($t_{CWD\ (MIN.)}$), the read modify write operation is enabled.

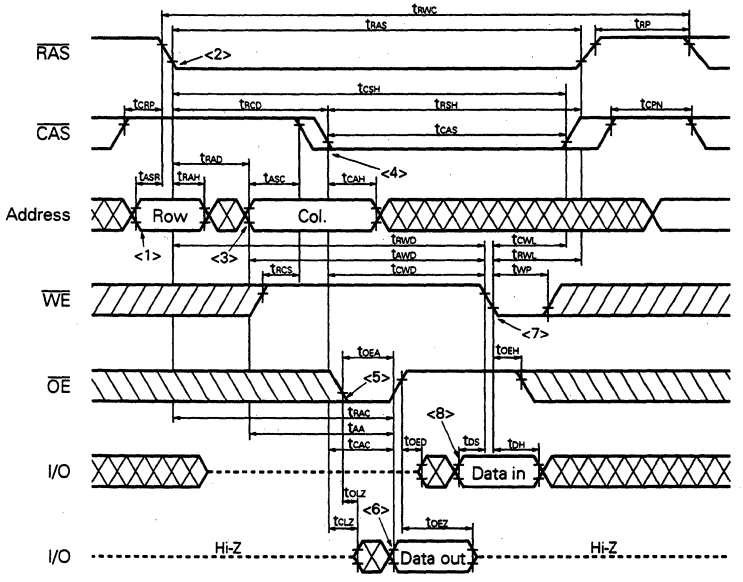
Figure 4-4. Read Modify Write Cycle of x1-Bit Device



<1> Defines row address.
<2> Activates $\overline{RAS}$ to latch row address.
<3> Defines column address.
<4> Activates $\overline{CAS}$ to latch column address.
<5> Inactivates $\overline{WE}$ to enable output buffer.
<6> Start of data output.
<7> Activates $\overline{WE}$ to enable input buffer.
<8> Sets input data.

$\overline{RAS}$	Active	
$\overline{CAS}$	Active	
$\overline{WE}$	Inactive	Active
DATA	Output	Input

Figure 4-5. Read Modify Write Cycle of Multiple-Bit Device



<1> Defines row address.
<2> Activates $\overline{RAS}$ to latch row address.
<3> Defines column address.
<4> Activates $\overline{CAS}$ to latch column address.
<5> Activates $\overline{OE}$ to enable output buffer.
<6> Start of data output.
<7> Activates $\overline{WE}$ to enable input buffer.
<8> Sets input data.

$\overline{RAS}$	Active	
$\overline{CAS}$	Active	
$\overline{WE}$	Inactive	Active
OE	Active	Don't care
I/O	Output	Input

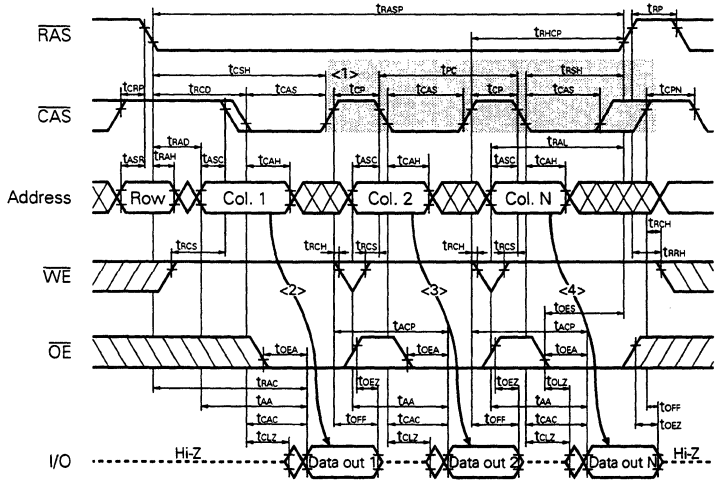
4.4 Page Mode

4.4.1 Fast page mode (FPM)

In the fast page mode (FPM), column addresses are latched by repeatedly activating and inactivating $\overline{CAS}$ after $\overline{RAS}$ has been activated and the row address has been latched. This mode is available for read/write or read modify write operations and allows the simultaneous use of read and write operations.

Taking the read operation as an example, during normal read operations, data can be output only once during each $\overline{RAS}$ cycle, while in the fast page mode, data can be output repeatedly. For this reason, during read operation in the fast page mode, the access time of the data output first (data output 1) is the same as the access time of normal read cycles, but the access time of the second and later data output (data output 2, data output N) becomes successively faster.

Figure 4-6. Fast Page Mode Read Cycle



<1> ▒▒▒▒ : $\overline{CAS}$ toggle operation (operation to repeat activating and inactivating)
<2> Data output 1 corresponding to column address 1
<3> Data output 2 corresponding to column address 2
<4> Data output N corresponding to column address N

4.4.2 Access time in fast page mode

The access time in the fast page mode varies depending on the conditions shown in Table 4-4.

Table 4-4. Access Time in Fast Page Mode Read Cycle

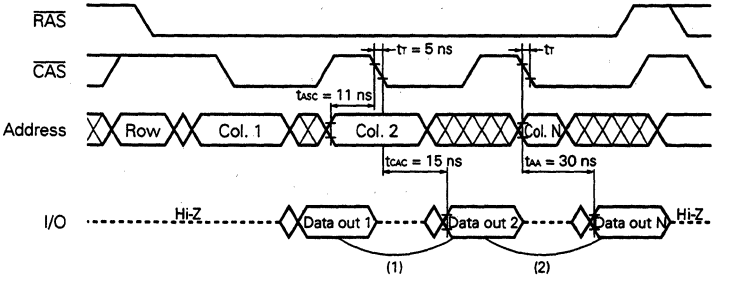
	Conditions	Valid access time
(1)	$t_{ASC} \geq (t_{AA\ (MAX.)} - t_T - t_{CAC\ (MAX.)})$	$t_{CAC\ (MAX.)}$
(2)	$t_{ASC\ (MIN.)} \leq t_{ASC} < (t_{AA\ (MAX.)} - t_T - t_{CAC\ (MAX.)})$	$t_{AA\ (MAX.)}$

Assuming that the specification in Table 4-5, an example in Table 4-4 is shown below (t_T = 5 ns).

Table 4-5. Specification of a Certain Memory (for fast page mode)

	MIN.	MAX.	Unit
t_{AA}	–	30	ns
t_{CAC}	–	15	
t_{ASC}	0	–	

Figure 4-7. $\overline{CAS}$ Access and Address Access



Remark $\overline{WE}$: inactive, $\overline{OE}$: active

(1) When t_{CAC} becomes valid ($\overline{CAS}$ access):

Data are output in 31 ns ($t_{ASC} + t_T + t_{CAC}$) after the column address is defined and in 15 ns after $\overline{CAS}$ is activated.

(2) When t_{AA} becomes valid (address access):

Data are output in 30 ns after column address is defined and in 25 ns ($t_{AA} - t_T$) after $\overline{CAS}$ is activated (in the case of t_{ASC} = 0 ns).

4.4.3 Hyper page mode (HPM)

Hyper page mode (HPM) is one type of page modes and is equivalent to EDO. The following describes main features of hyper page mode in relation to how it differs from the fast page mode (FPM).

(1) Data output time is extended

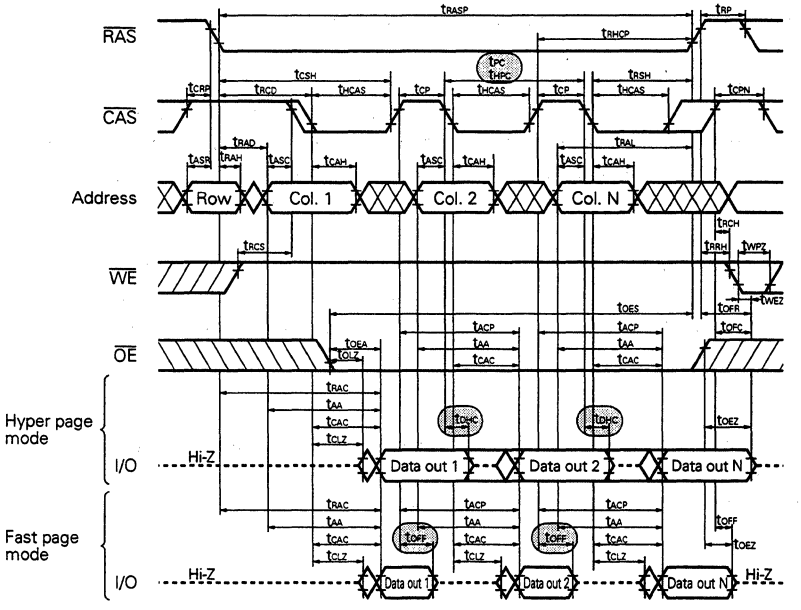
In hyper page mode, output data are held until the falling of the next $\overline{CAS}$ cycle rather than the rising of $\overline{CAS}$ to extend data output time (extended data out function). In normal fast page mode, data output time is reduced when $\overline{CAS}$ cycle time is shortened. However, in hyper page mode, the extended data out function increases the timing margin at the reading side even if the $\overline{CAS}$ cycle time becomes shorter.

(2) Further shortening in $\overline{CAS}$ cycle time (t_{HPC}) as compared with fast page mode

According to (1) above, the $\overline{CAS}$ cycle time can be further shortened in the hyper page mode as compared with the fast page mode if the timing margin at the reading side is the same. For example, the $\overline{CAS}$ cycle time in the hyper page mode is 25 ns while that in the fast page mode is 40 ns for a device with t_{RAC} = 60 ns.

In hyper page mode, read operation (data output) and write operation (data input) can be repeatedly executed during one $\overline{RAS}$ cycle as in fast page mode. The read and write operations can exist at the same time with the performance being equivalent to that of the fast page mode.

Figure 4-8. Hyper Page Mode Read Cycle

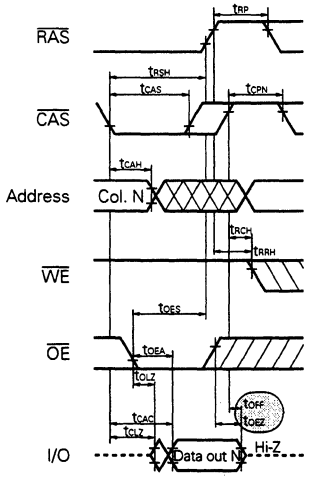


4.4.4 I/O Hi-Z state

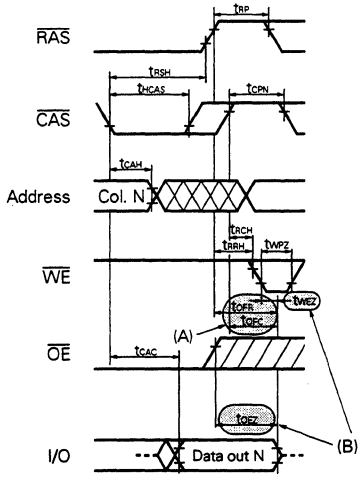
In page mode, when I/O is set to Hi-Z state in read cycle, valid signal specifications differ as shown below.

Figure 4-9. I/O Hi-Z State

(a) Fast page mode



(b) Hyper page mode



(1) Fast page mode:

The tOFF and tOEZ are applied to set I/O to Hi-Z state and the faster becomes effective.

(2) Hyper page mode:

The $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and $\overline{OE}$ need to be controlled as follows to set I/O to Hi-Z state. Valid signal specifications differ depending on the state of each signal.

- Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
  $\overline{WE}$: inactive, $\overline{OE}$: active
  tOFC is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
  tOFR is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
- Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
  $\overline{WE}$, $\overline{OE}$: inactive ····· tOEZ is effective.
- Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
  $\overline{WE}$, $\overline{OE}$: active and either tRRH or tRCH must be met ····· tWEZ and tWPZ are effective.
- $\overline{WE}$: inactive (in read cycle)
  $\overline{CAS}$: inactive, $\overline{OE}$: active ····· tCHO is effective.
  $\overline{CAS}$, $\overline{OE}$: active ····· tOCH is effective.

In short,

(A) The slower of tOFR and tOFC becomes effective.

(B) The faster of tWEZ and tOEZ becomes effective.

Please note that I/O will not become Hi-Z state even if $\overline{CAS}$ changes from active to inactive in case of hyper page mode with $\overline{RAS}$: active, $\overline{WE}$: inactive and $\overline{OE}$: active.

4.4.5 Access time in hyper page mode

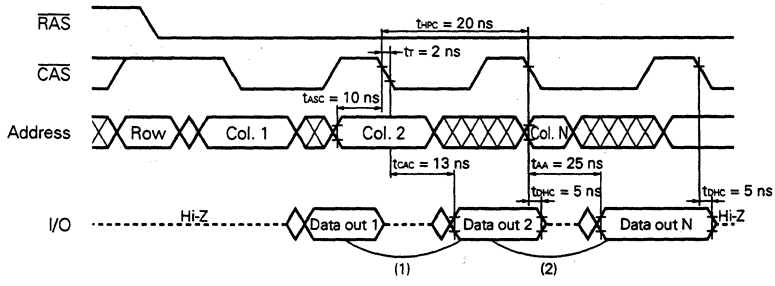
When t_{AA} is applied in the hyper page mode, t_{HPC} cannot be operated at the minimum value (See **4.4.2 Access time in fast page mode** for $\overline{CAS}$ access and address access).

Assuming that the specification in Table 4-6, an example in Figure 4-10 is shown below (t_T = 2 ns).

Table 4-6. Specification of a Certain Memory (for hyper page mode)

	MIN.	MAX.	Unit
t_{HPC}	20	–	ns
t_{AA}	–	25	
t_{CAC}	–	13	
t_{ASC}	0	–	
t_{DHC}	5	–	

Figure 4-10. $\overline{CAS}$ Access and Address Access (for hyper page mode)



Remark $\overline{WE}$: inactive, $\overline{OE}$: active

(1) When t_{CAC} becomes valid ($\overline{CAS}$ access):

Data output time is equal to 10 ns when t_{HPC} is set to the minimum value.

Data output time: $(t_{HPC} - t_T - t_{CAC}) + t_{DHC} = (20 - 2 - 13) + 5 = 10$ ns

(2) When t_{AA} becomes valid (address access):

Data output time is equal to 0 ns when t_{HPC} is set to the minimum value and hence 10 ns cannot be secured.

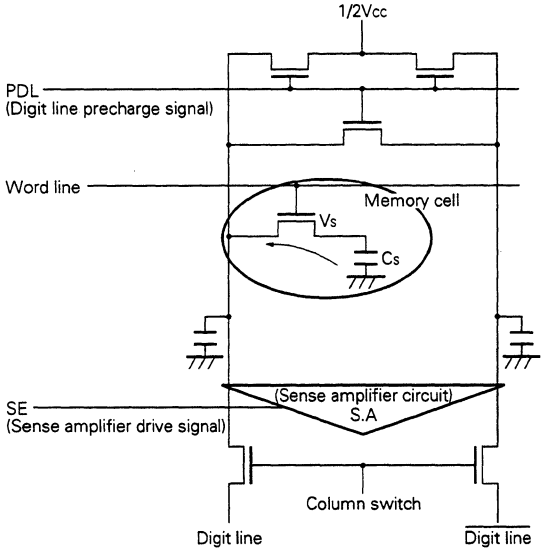
Data output time: $(t_{HPC} - t_{AA}) + t_{DHC} = (20 - 25) + 5 = 0$ ns

Therefore, t_{HPC} needs to be set to 30 ns (address access) or t_{ASC} needs to be set to 10 ns ($\overline{CAS}$ access) to secure 10 ns data output time.

CHAPTER 5 INTERNAL MEMORY OPERATION

This chapter describes the internal operation of memory devices, taking read cycles as an example.

Figure 5-1. Simplified Diagram of Internal Memory



Let us assume that the high level (= 5.0 V) is held by the capacitor in the memory cell and is to be output to the outside of the memory (read operation). When $\overline{RAS}$ is not activated, PDL (digit line precharge) is activated and the digit lines and $\overline{\text{digit lines}}$ are at half of Vcc potential.

Assuming that the word line is selected with the row address, activating $\overline{RAS}$ makes PDL and the word line inactive and active, respectively, followed by SE (sense amplifier drive) being activated with some delay time. When PDL is inactivated, the digit lines and $\overline{\text{digit lines}}$ are separated.

When the word line is activated, the transistor (Vs) is turned on, transferring electric charges in the capacitor (Cs) to the digit line. Then, the potential of the digit line becomes 1/2 Vcc + α, resulting in some voltage difference (=α) between the digit lines and $\overline{\text{digit lines}}$. The difference is amplified by the sense amplifier to 5.0 V and 0 V. When the capacitor (Cs) holds the low level (= 0 V), the reverse operation is performed (i.e., Digit line = 1/2 Vcc − α and $\overline{\text{Digit lines}}$ = 1/2 Vcc. The potential difference is amplified). The column switch is controlled with $\overline{\text{CAS}}$.

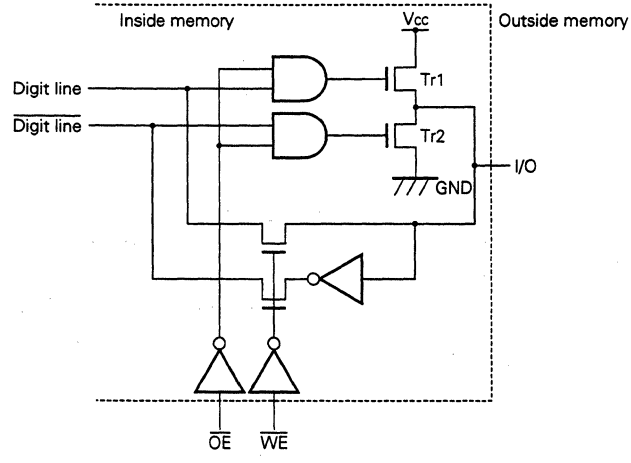
When $\overline{\text{CAS}}$ is inactivated, the column switch is inactivated. When $\overline{\text{RAS}}$ is inactivated, the transistor (Vs) is turned off, SE is inactivated, and PDL is activated. The digit lines and $\overline{\text{digit lines}}$ amplified by the sense amplifier to 5.0 V and 0 V gradually reach 1/2 Vcc.

The time it takes for the digit lines and $\overline{\text{digit lines}}$ to change from 5.0 V and 0 V to 1/2 Vcc at this time is the $\overline{\text{RAS}}$ precharge time (t_{RP}). When the $\overline{\text{RAS}}$ precharge time runs short, the sense amplifier may malfunction because the next operation (the transistor (Vs) is turned on) is made without causing the digit lines and $\overline{\text{digit lines}}$ to reach 1/2 Vcc.

Digit lines are connected to the transistors at the output stage. The transistors are controlled with $\overline{\text{OE}}$ ($\overline{\text{WE}}$ in write operation).

- When Tr1 = ON and Tr2 = OFF, the high level is output.
- When Tr1 = OFF and Tr2 = ON, the low level is output.

Figure 5-2. Simplified Diagram of Memory Output Stage



CHAPTER 6 REFRESH

This chapter describes the refresh operation, taking the μPD42S16160 (1M words x 16 bits) as an example.

6.1 Refresh Cycles and Distributed/Burst Refresh

The refresh cycle of the μPD42S16160 is 4,096/128 ms.

This expression means that 4,096 refresh cycles are required during each 128 ms interval. The requirement should be strictly observed, otherwise data stored in memory may be destroyed.

Refresh can be executed in two ways.

(1) Distributed refresh:

Refresh cycles are executed at intervals. In the case of the μPD42S16160, refresh cycles are executed every 31.3 μs (128 ms/4,096).

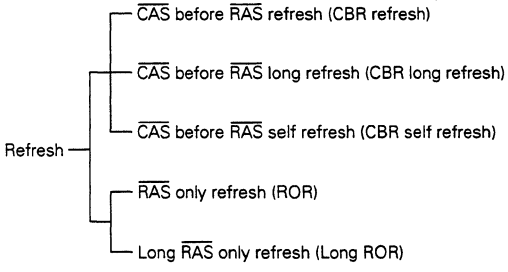
(2) Burst refresh:

Refresh cycles are executed in succession. In the case of the μPD42S16160, 4,096 refresh cycles are executed in succession.

6.2 Refresh Types

Refresh can be categorized into two main types and further into five sub-types as shown below.

Figure 6-1. Refresh Types



In normal (read/write) mode, CBR refresh, CBR long refresh, ROR, or long ROR are generally used; in data retain (with battery backup) mode, CBR self refresh is generally used.

6.3 Refresh Operation

This section describes refreshes used for DRAM. The control method for these refreshes and refresh cycle ratings are shown in Tables 6-1 and 6-2.

(1) CBR refresh:

Refresh is executed with (memory) external clock and (memory) internal address signals. In this case, the refresh cycle rating is 4,096/64 ms.

Addresses are generated by an internal counter which counts automatically. Therefore, 4,096 different addresses are generated automatically.

(2) CBR long refresh:

Refresh is executed with external clock and internal address signals. In this case, the refresh cycle rating is 4,096/128 ms. Compared with the CBR refresh (64 ms), the refresh period is longer (128 ms). Therefore, the number of refresh times per time interval is smaller than in the case of the CBR refresh, resulting in lower power consumption (lower average current consumption per time interval).

(3) ROR and long ROR:

Refresh is executed with external clock and external address signals. In this case, the refresh cycle rating is 4,096/64 ms (4,096/128 ms for long ROR). 4,096 different addresses must be created outside the memory.

(4) CBR self refresh:

Refresh is executed with internal clock and internal address signals. Memory executes refresh automatically under control of the internal clock (no refresh cycle). Therefore, CBR self refresh cannot be used when read and write operations are executed together and cannot be controlled externally.

Memories that can assure CBR self refresh can also assure CBR refresh, CBR long refresh, ROR, and long ROR.

Table 6-1. Refresh Control Methods

	Clock	Address
CBR refresh	External Clock	Internal Address
CBR long refresh		
ROR	External Clock	External Address
Long ROR		
CBR self refresh	Internal Clock	Internal Address

Table 6-2. Refresh Cycle Ratings

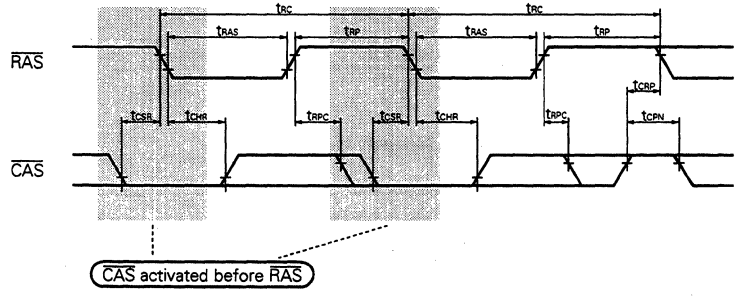
	DRAM with self refresh	DRAM without self refresh
Refresh cycle	4,096/128 ms	4,096/64 ms
CBR refresh	○	○
CBR long refresh	○	×
ROR	○	○
Long ROR	○	×
CBR self refresh	○	×

Remark ○: Assured, ×: Not assured

6.4 CBR Refresh, CBR Long Refresh Cycle

By activating $\overline{RAS}$ after $\overline{CAS}$ has been activated, the internal counter is activated and a row address is generated automatically. One row address is refreshed through this operation (in Figure 6-2, refresh is executed twice). Refresh is executed with the external clock and internal address signals.

Figure 6-2. CBR Refresh Cycle



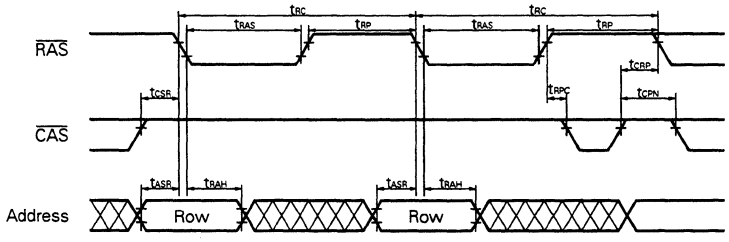
Remark Address, $\overline{WE}$, $\overline{OE}$: don't care I/O: Hi-Z

Although the refresh period for the CBR long refresh cycle is longer than that of the CBR refresh cycle, its operation is exactly the same.

6.5 ROR and Long ROR Cycles

After $\overline{RAS}$ has been activated, the row address is latched and refresh is executed. Through this operation, refresh is completed for one row address.

Figure 6-3. ROR Cycle



Remark $\overline{WE}$, $\overline{OE}$: don't care I/O: Hi-Z

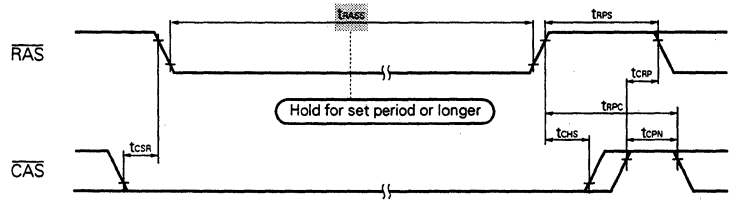
Although the refresh period for the long ROR refresh cycle is longer than that of the ROR refresh cycle, its operation is exactly the same.

6.6 CBR Self Refresh Cycle

6.6.1 Executing CBR self refresh

In the same way as for the CBR refresh cycle, after activating $\overline{CAS}$, activate $\overline{RAS}$. By keeping $\overline{RAS}$ activated for a set period ($t_{RASS\ (MIN.)}$ = 100 μs) or longer, the internal clock and the internal counter are activated and the memory repeatedly refreshes itself.

Figure 6-4. CBR Self Refresh Cycle



Remark Address, $\overline{WE}$, $\overline{OE}$: don't care I/O: Hi-Z

6.6.2 Cautions on use of CBR self refresh

CBR self refresh can be used independently when used in combination with distributed CBR long refresh; However, used in combination with burst CBR long refresh or with long ROR (both distributed and burst), the following cautions must be observed (For information on distributed and burst refresh, see **6.1 Refresh Cycles and Distributed/Burst Refresh**). The μPD42S16160 is used in the following example.

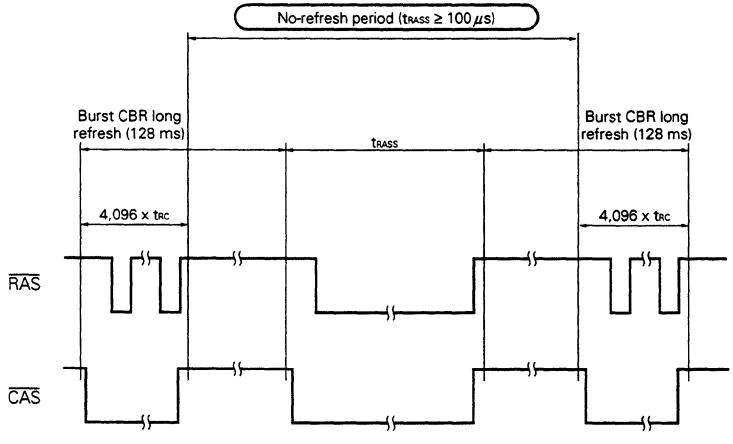
(1) Normal Combined Use of CBR Self Refresh and Burst CBR Long Refresh

Let us assume that CBR long refresh is used as shown in Figure 6-5. The $\overline{RAS}$ must be kept activated (= t_{RASS}) for 100 μs or longer to execute CBR self refresh (See **6.6.1 Executing CBR self refresh**).

In the CBR self refresh, it is not known how many seconds are required to refresh all memory cells. Therefore, if the CBR self refresh is stopped without refreshing all memory cells, an inactive period of up to approximately 2 t_{REF} occurs, the t_{REF} (= refresh time) requirement cannot be satisfied and data may be destroyed.

To prevent this from occurring, normally, when CBR self refresh and burst CBR long refresh are used in combination, execute CBR refresh for 4,096 times within 64 ms just before and after setting CBR self refresh. Through this CBR refresh, the period when any refresh is not executed will be within the t_{REF} requirement.

Figure 6-5. Example of Burst CBR Refresh Use

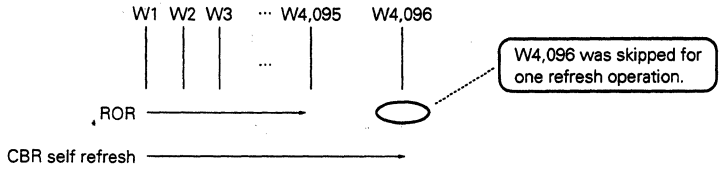


(2) Normal Combined Use of CBR Self Refresh and Burst Long ROR

The address control method for ROR and CBR refresh differ (ROR: Control from outside memory; CBR refresh: Control from inside memory).

Let us suppose that refresh is executed in the subsequence word line 1 (W1) to word line 2 (W2) with ROR. When refresh has been executed up to word line 4,095 (W4,095), CBR self refresh begins. At this time, if the internal counter (it cannot be controlled from the outside) happens to be set at word line 1 (W1), the refresh operation is executed in the subsequence word line 1 (W1) to word line 2 (W2). Under these conditions, an inactive period of up to approximately 2 t_{REF} occurs for the word line 4,096 (W4,096) (See **CHAPTER 5 INTERNAL MEMORY OPERATION** and **6.8 Internal Memory Operation During Refresh**). Execute ROR 4,096 times within an interval of 64 ms or less just before entering or exiting CBR self refresh to satisfy the t_{REF} requirement.

Figure 6-6. Example of ROR Use



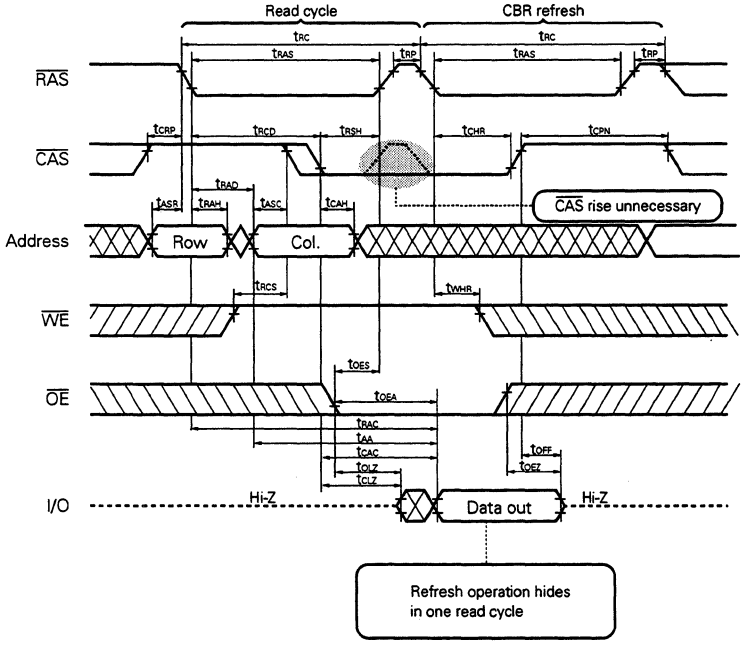
Remark W: Word line

6.7 Hidden Refresh Cycle

If CBR refresh cycle is started after a read/write cycle or read modify write cycle operation, it is possible to enter CBR refresh cycle with $\overline{CAS}$ activated.

Hidden refresh read cycle is shown in Figure 6-7 as an example.

Figure 6-7. Hidden Refresh Read Cycle



6.8 Internal Memory Operation During Refresh

This section explains how the memory operates during refresh using Figure 6-8 as an example.

As explained in **CHAPTER 5 INTERNAL MEMORY OPERATION**, when $\overline{RAS}$ is activated, a word line is selected and activated. The charge in the memory cell connected with this word line is transmitted to the digit line. The signal voltage difference generated at this time is amplified by the sense amplifier. Refresh consists of the above sequence of actions.

Figure 6-8. Simplified Circuit Diagram of 16-bit DRAM

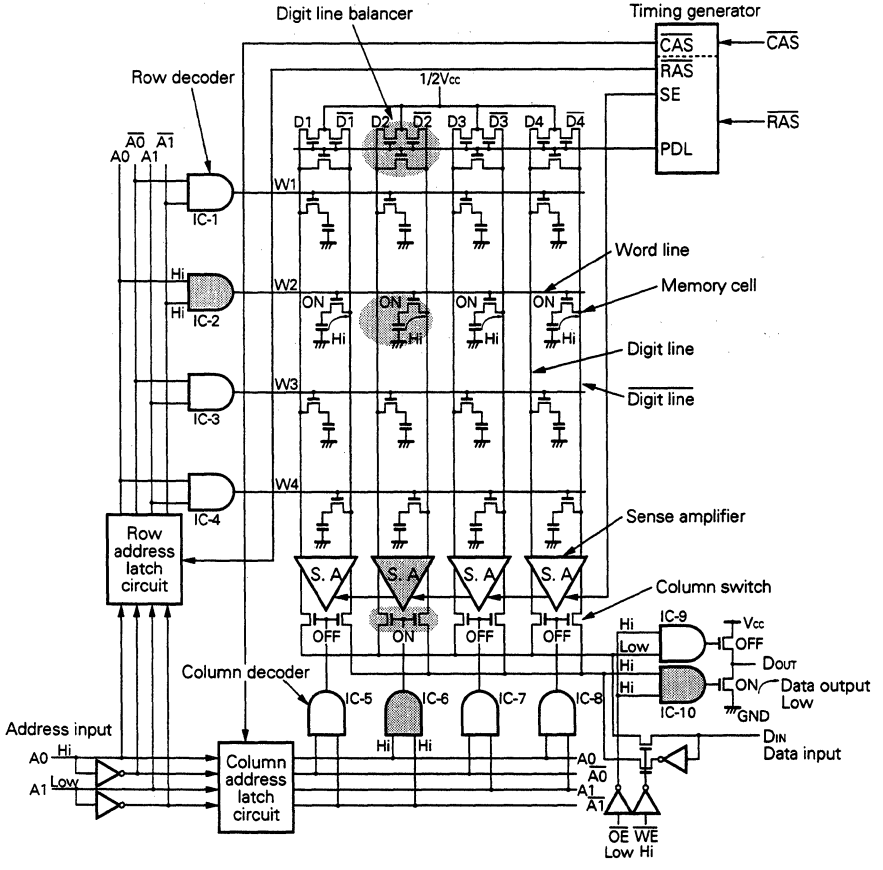


Figure 6-8 shows 16-bit DRAM (DRAM with 16 memory cells).

Let us suppose that the high level and the low level are input to the addresses A0 and A1, respectively, to select the word line (W2) while the high level is retained for all memory cells. Then, the IC-2 becomes the high level, the word line 2 (W2) is selected and activated, and all memory cells connected to it are refreshed (Because the output of the IC-6 is also at the high level, the column switch connected to the digit line 2 (D2, $\overline{D2}$) is activated. However, because the column address latch circuit is inactivated by refresh, all column switches are off.). Therefore, all memory cells are refreshed by selecting all word lines.

In a memory device with 4,096/128 ms refresh cycle, execution of read/write cycle at 4,096 different kinds of addresses is equivalent to refresh.

6.8.1 Not cell and true cell

Even if data within a memory cell are read after refresh fails and all data are destroyed, they are not always at the low level. The following provides an any explanation.

There are two types of memory cells, namely Not cell and True cell.

(1) Not Cell

The Not cell causes the data retention state of a memory cell to be reversed from the data input from the outside of memory or output to the outside of memory.

In Figure 6-8, when the output of the IC-2 and IC-6 reaches the high level, the column switches connected to the word line 2 (W2) and digit lines 2 (D2, $\overline{D2}$) becomes active, and digit line and $\overline{\text{digit line}}$ become the low level and high level, respectively. For read operation, the output of IC-10 becomes the high level, the transistor at the ground side is turned on, and hence a low-level signal is output from DOUT although the memory cell retains the high level because $\overline{WE}$ is inactive and $\overline{OE}$ is active.

Therefore, the output becomes the low level when the Not cell retains the high level at the memory cell and the high level when it retains the low level. The same applies to write operation. When a low level signal is input, the memory cell retains the high level. On the other hand, when the high level is input, it retains the low level.

(2) True Cell

The True cell causes the data retention state of a memory cell to be equal to the data input from the outside of memory or output to the outside of memory. The True cell causes the output to be the high level when the high level is retained at the memory cell and to be the low level when the low level is retained. The same applies to write operation.

In Figure 6-8, the memory cell connected to the word lines 2 and 4 (W2, W4) is Not cell and that connected to the word lines 1 and 3 (W1, W3) is True cell. The following table summarizes the I/O data state and data retention state of memory cell of Not and True cells.

Table 6-3. I/O Data State and Memory Cell Data Retention State

	I/O Data State	Data Retention State of Memory Cell
Not Cell	High level	Low level
	Low level	High level
True Cell	High level	High level
	Low level	Low level

According to the above, even if data are destroyed without observing refresh cycle (tREF) and electric charge is lost from the memory cell, the data output from the inside of the memory is not always at the low level. Also, the high level cannot always be retained even if a high level signal is input from the outside of memory to all memory cells.

The above is designed to minimize the interference between adjacent memory cells. In an actual device, the True and Not cells are aligned carefully, namely the True and Not cells are not always aligned alternately. See **CHAPTER 5 INTERNAL MEMORY OPERATION** for basic internal memory operation.

6.9 DRAM Refresh Cycles

Various DRAM refresh cycles are shown in the table below.

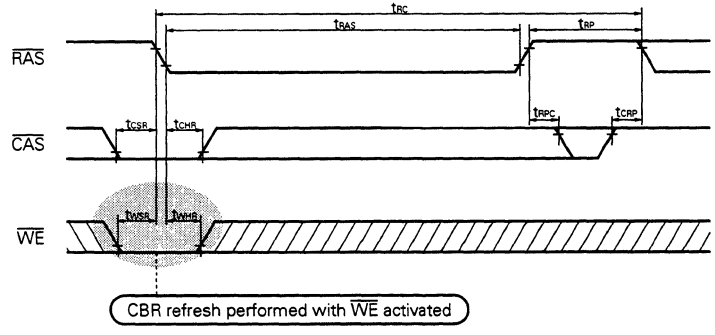
Table 6-4. Various DRAM Refresh Cycles

Density	Bit Organization	DRAM with Self Refresh Function	DRAM without Self Refresh Function
1 M	x 1	———	512/8 ms
	x 4		
4 M	x 1	1,024/128 ms	1,024/16 ms
	x 4		
	x 8		
	x 16	512/128 ms	512/8 ms
16 M	x 1	4,096/128 ms	4,096/64 ms
	x 4	2,048/128 ms	2,048/32 ms
	x 8		
	x 16	4,096/128 ms	4,096/64 ms
		1,024/128 ms	1,024/32 ms

CHAPTER 7 TEST MODE

By using the test mode, the test time can be reduced. The reason for this is that, in the case of 16M DRAM for example, the memory emulates the x 16-bit organization during test mode (In the case of 4M DRAM, the memory emulates the x 8-bit organization).

Figure 7-1. Test Mode Set Cycle ($\overline{WE}$, CBR Refresh Cycle)



Remark Address, $\overline{OE}$: don't care I/O: Hi-Z

(1) Setting the mode

Executing the test mode cycle ($\overline{WE}$, CBR refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, in the case of 16M DRAM, the data are written to 16 bits of memory cell and in the case of 4M DRAM, the data is written to 8 bits of memory cell (independent data can be written to any input pin). The case of 16M DRAM is illustrated in the example below.

Write Operation during Test Mode for 16M DRAM

- x 1-bit devices: "0" or "1" input from D_{IN} is written sequentially to all 16 bits of memory cells.
- x 4-bit devices: "0" or "1" input from I/O1-I/O4 is written sequentially to all 16 bits of memory cells in four-bit units.

Next, when the data are read from the output pin at the same address, the memory cell can be checked.

Output = "1": Normal write (all memory cells)

Output = "0": Abnormal write

(3) Refresh

Refresh in the test mode must be performed with read/write cycle (See **6.8 Internal Memory Operation During Refresh**) or with the $\overline{WE}$, CBR refresh cycle. The $\overline{WE}$, CBR refresh cycle use the same counter as the CBR refresh's internal counter (See **6.3 Refresh Operation**).

(4) Mode Cancellation

The test mode is canceled by executing one cycle of ROR cycle or CBR refresh cycle.

[MEMO]

CHAPTER 8 BYTE CONTROL

Concerning DRAMs with x 16 bits or more, controlling I/O data in byte (8 bits) units is called byte control. The byte control mode can be used for read, write, or read modify write operation.

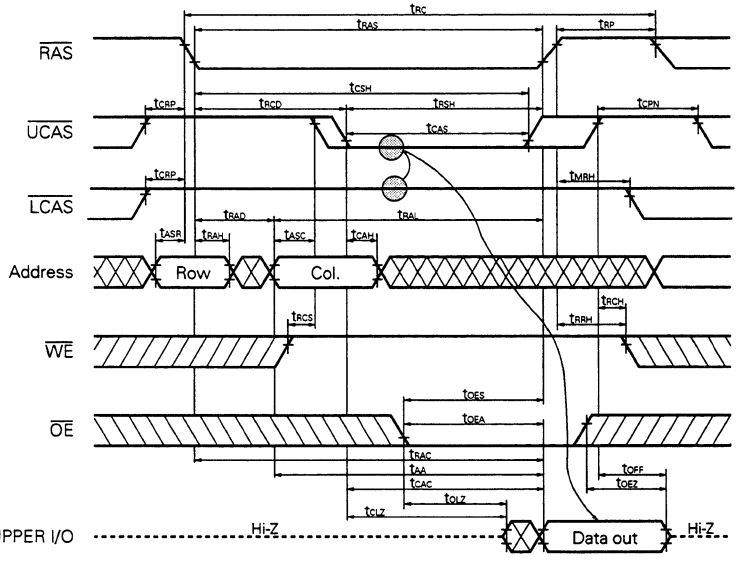
8.1 Byte Read/Write Mode

It is possible to read and write in byte units. Byte control is executed by the following two $\overline{\text{CAS}}$s.

- $\overline{\text{LCAS}}$ ($\overline{\text{LOWER CAS}}$) : Controls read/write operations for I/O1 to I/O8 (Lower I/O).
- $\overline{\text{UCAS}}$ ($\overline{\text{UPPER CAS}}$) : Controls read/write operations for I/O9 to I/O16 (Upper I/O).

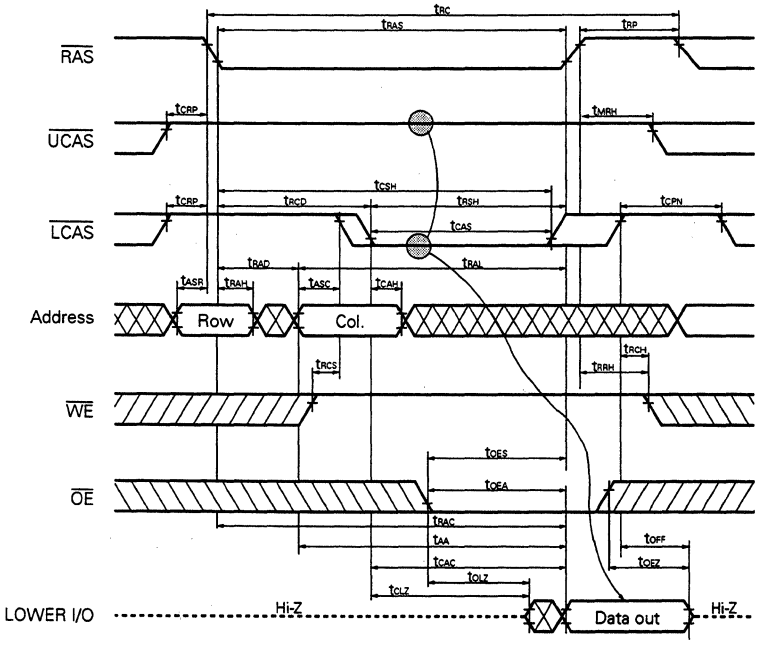
Figures 8-1 and 8-2 show examples controlled by $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$, respectively.

Figure 8-1. Upper Byte Read Cycle



Remark LOWER I/O: Hi-Z

Figure 8-2. Lower Byte Read Cycle



Remark UPPER I/O: Hi-Z

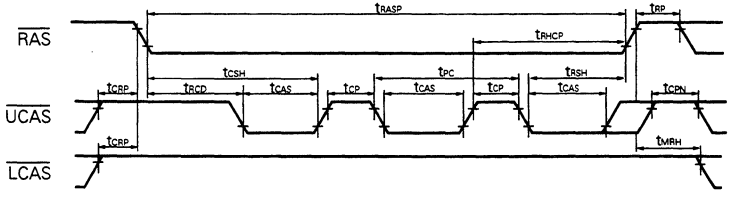
8.2 Page Mode of Byte Read/Write Mode

In the page mode, there are the following four types of control methods of I/O data according to the toggle operation (repeated operation of activation/inactivation) of $\overline{CAS}$ signal.

Table 8-1. Method for Controlling Byte Read/Write Mode

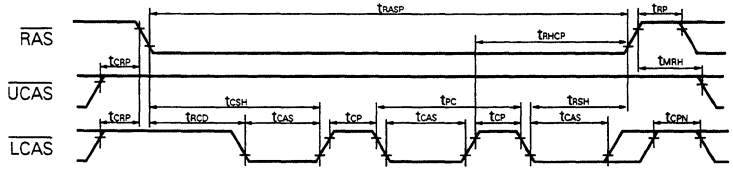
	$\overline{UCAS}$	$\overline{LCAS}$	I/O Data Control
(1)	Toggle operation	Inactive	8 bits
(2)	Inactive	Toggle operation	8 bits
(3)	Toggle operation	Toggle operation	16 bits
(4)	Toggle operation	Toggle operation	8 bits

(1) UPPER I/O Control



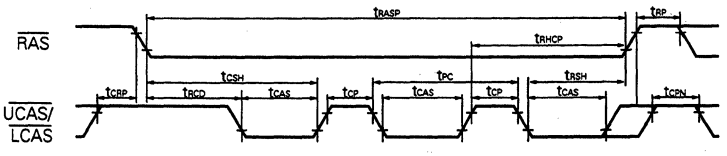
The $\overline{UCAS}$ is toggled while $\overline{LCAS}$ is inactive to control the UPPER I/O 8-bit data.

(2) LOWER I/O Control



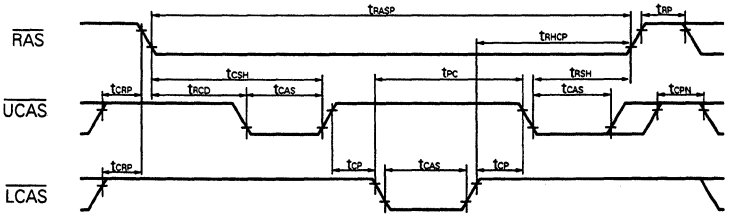
The $\overline{LCAS}$ is toggled while $\overline{UCAS}$ is inactive to control the LOWER I/O 8-bit data.

(3) All I/O Control



The $\overline{UCAS}$ and $\overline{LCAS}$ are toggled simultaneously to control UPPER I/O and LOWER I/O (all I/Os) 16-bit data.

(4) Mixed Control of UPPER I/O and LOWER I/O



The $\overline{UCAS}$ and $\overline{LCAS}$ are toggled in a mix to control each 8-bit data of UPPER I/O and LOWER I/O (No alternate control is required).

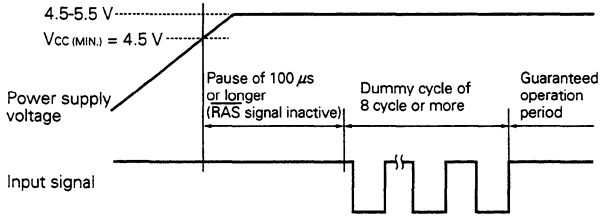
Remark In the page mode, read, write, and read modify write can be used in a mix by continuing $\overline{CAS}$ signal during the same $\overline{RAS}$ cycle.

CHAPTER 9 INITIALIZING

After turning on, the state of internal DRAM circuits is not known. It is therefore necessary to initialize them to ensure normal operation.

When turning on power, allow a 100-μs or longer pause ($\overline{RAS}$ signal inactive) and then be sure to execute eight or more ROR or CBR refresh cycles as dummy cycles to initialize the internal circuits.

Figure 9-1. Initializing



Remark This dummy cycle of 8 cycles or more is just a dummy cycle and does not guarantee refresh operation.

Unless initializing is executed accurately, the memory may not operate properly even during guaranteed operation period.

[MEMO]

CHAPTER 10 LOW VOLTAGE OPERATION

DRAM are divided into 5.0-V operation devices and low-voltage operation devices. The main differences between 5.0-V and low-voltage operation devices are shown in Table 10-1 using 16M DRAM (X 16-bit device) as an example.

Table 10-1. Main Differences between 5.0-V and Low-Voltage Operation Devices

	5.0-V Operation Devices	Low-voltage Operation Devices
Part number	μPD42S16160-60	μPD42S16160L-A60
Power supply voltage	5.0 V ± 10 % (4.5 V to 5.5 V)	3.3 V ± 0.3 V (3.0 V to 3.6 V)
Input voltage	V_{IH} = 2.4 V to V_{CC} + 1.0 V V_{IL} = −1.0 V to +0.8 V	V_{IH} = 2.0 V to V_{CC} + 0.3 V V_{IL} = −0.3 V to +0.8 V
Output voltage	V_{OH} = 2.4 V/V_{OL} = 0.4 V	V_{OH} = 2.4 V/V_{OL} = 0.4 V
Operating current	100 mA	90 mA
CBR self refresh current (data-retention current)	250 μA	150 μA
Pin configuration	Same	

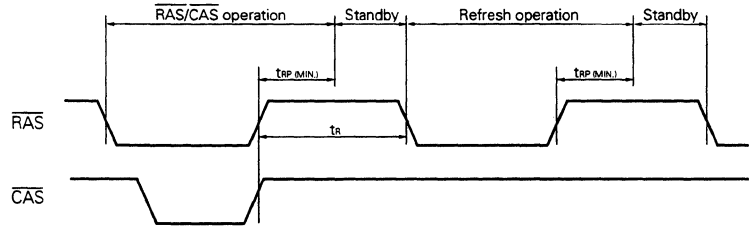
The 5.0-V operation devices of 16M DRAM all adopt an internal voltage-drop circuit. The internal voltage-drop circuit causes the power supply voltage (5.0 V) supplied to the memory externally to be dropped inside the memory and 5.0-V operation devices also operate on 3.3 V inside the memory. Therefore, there is almost no difference between the current consumption of the 5.0-V operation device and that of the low-voltage operation device. The low-voltage operation device of 16M DRAM does not adopt any internal voltage-drop circuit.

[MEMO]

CHAPTER 11 CURRENT CONSUMPTION CALCULATION

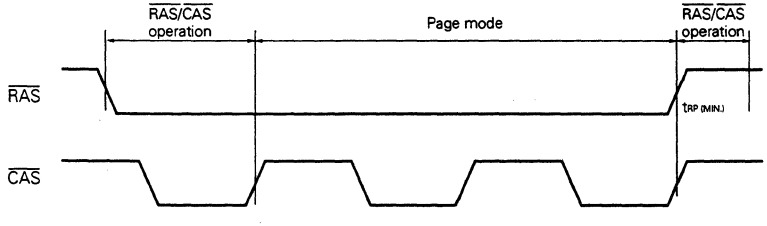
The following examples explains an approximate current consumption calculation according to timing.

(1) Example 1



In the example 1, after RAS/CAS operation (read, write, or read modify write cycle) is executed first, refresh (ROR) is executed. When the RAS precharge time ($t_{RP\,(MIN.)}$) exceeds the specification ($t_R > T_{RP\,(MIN.)}$), standby current is applied.

(2) Example 2



The example 2 executes the page mode. In the first CAS cycle, RAS/CAS operation is applied and the page mode is applied from the second CAS cycle or thereafter. The RAS precharge time ($t_{RP\,(MIN.)}$) when the page mode ends becomes the precharge of RAS/CAS operation. Therefore, the RAS/CAS operation is obtained by merging the first RAS active period and the RAS precharge period when the page mode ends.

When the timing shown in the example satisfies the conditions shown in Table 11-1 (extracted from data sheet), each current consumption (per unit time) is added.

Table 11-1. μPD4216160 DC Characteristics

Parameter	Symbol	Test Condition		MIN.	TYP.	MAX.	Unit
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling	t_{RAC} = 50 ns			110	mA
		t_{RC} = t_{RC} (MIN.)	t_{RAC} = 60 ns			100	
		I_O = 0 mA	t_{RAC} = 70 ns			90	
			t_{RAC} = 80 ns			80	
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≥ V_{IH} (MIN.), I_O = 0 mA				2	mA
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA				1	
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH} (MIN.)	t_{RAC} = 50 ns			110	mA
		t_{RC} = t_{RC} (MIN.), I_O = 0 mA	t_{RAC} = 60 ns			100	
			t_{RAC} = 70 ns			90	
			t_{RAC} = 80 ns			80	
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS}$ ≤ V_{IL} (MAX.), $\overline{CAS}$ Cycling	t_{RAC} = 50 ns			100	mA
		t_{PC} = t_{PC} (MIN.), I_O = 0 mA	t_{RAC} = 60 ns			90	
			t_{RAC} = 70 ns			80	
			t_{RAC} = 80 ns			70	
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns			110	mA
		t_{RC} = t_{RC} (MIN.)	t_{RAC} = 60 ns			100	
		I_O = 0 mA	t_{RAC} = 70 ns			90	
			t_{RAC} = 80 ns			80	
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10		+10	μA
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10		+10	μA
High level output voltage	V_{OH}	I_O = –2.5 mA		2.4			V
Low level output voltage	V_{OL}	I_O = +2.1 mA				0.4	V

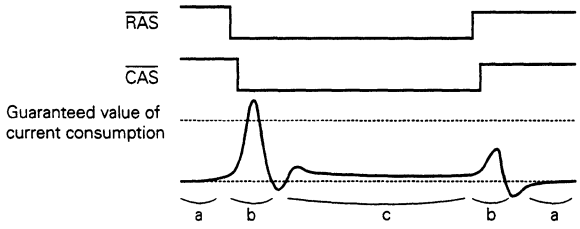
Current consumption varies depending on operating conditions (See **CHAPTER 12 MAIN DRAM CHARACTERISTICS** for the details). Appendix A shows the ratio and compensation which is required for each operating condition.

CHAPTER 12 MAIN DRAM CHARACTERISTICS

12.1 Current Consumption Waveform Diagram

In DRAM, as its name implies, consumption current flows more dynamically as compared with other memories. There is actually a peak current as shown in Figure 12-1.

Figure 12-1. Current Consumption Waveform Simplified Diagram of $\overline{RAS}/\overline{CAS}$ Cycle



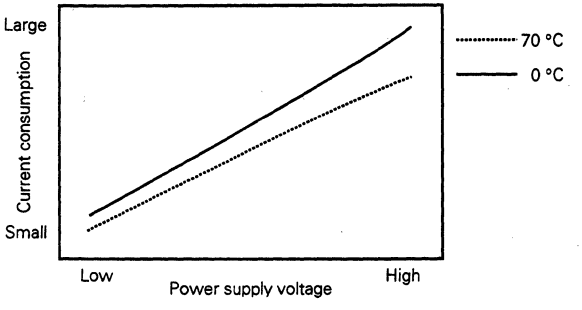
Period	Signal State	Current Consumption
a	$\overline{RAS}/\overline{CAS}$ = inactive	Almost 0
b	$\overline{RAS}/\overline{CAS}$ = from inactive to active or vice versa	Peak current
c	$\overline{RAS}/\overline{CAS}$ = inactive	Slight

When $\overline{RAS}$ changes from inactive to active state, the sense amplifier becomes active and hence current consumption is maximized at that instant (peak current). The guaranteed value indicates an average current consumption and hence the peak current may exceeds the guaranteed value.

As $\overline{RAS}/\overline{CAS}$ cycle becomes longer, the average current consumption becomes smaller.

12.2 Current Consumption Dependence on Power Supply Voltage

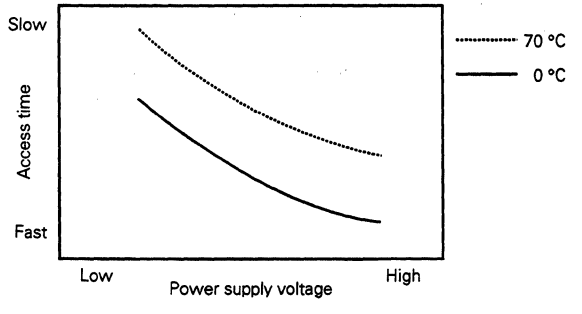
Figure 12-2. Current Consumption - Power Supply Voltage Characteristics



Current consumption decreases when the power supply voltage is reduced, and increases when the ambient temperature decreases. As ambient temperature decreases, resistance decreases and internal memory operation speeds up, resulting in increase in current consumption. The current consumption should be roughly estimated when the power supply voltage is higher (the worst case).

12.3 Access Time Dependence on Power Supply Voltage

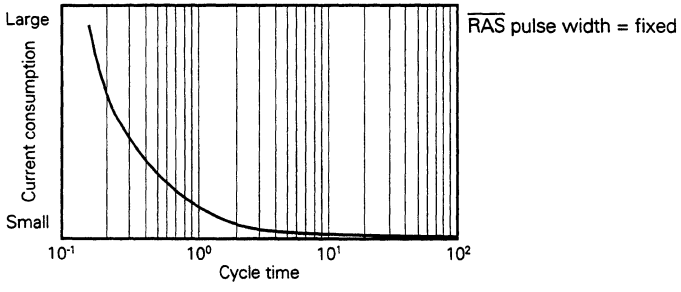
Figure 12-3. Access Time - Power Supply Voltage Characteristics



The access time is slower when the power supply voltage decreases, and is faster when the ambient temperature decreases. The access time should be roughly estimated when the power supply voltage is lower.

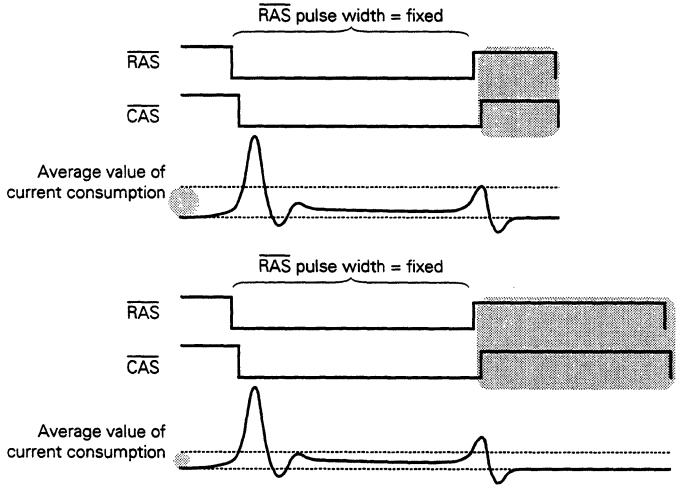
12.4 Current Consumption Dependence on $\overline{RAS}$ Cycle

Figure 12-4. Current Consumption - Cycle Time Characteristics



The current consumption per unit time is reduced as the cycle time becomes slower.

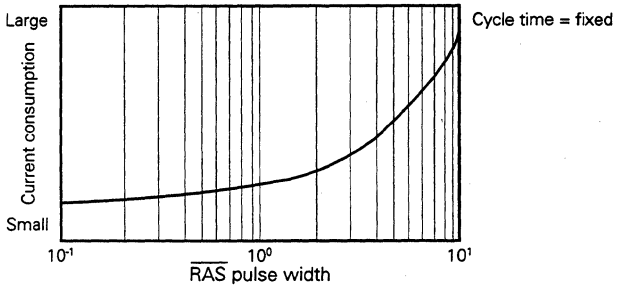
Figure 12-5. Average Current Consumption on Fixed $\overline{RAS}$ Pulse Width



Fixing the $\overline{RAS}$ pulse width and increasing the cycle time result in increasing the $\overline{RAS}$ precharge time. As the $\overline{RAS}$ precharge time becomes longer, the inactive time of $\overline{RAS}$ is extended and hence the average current consumption is reduced.

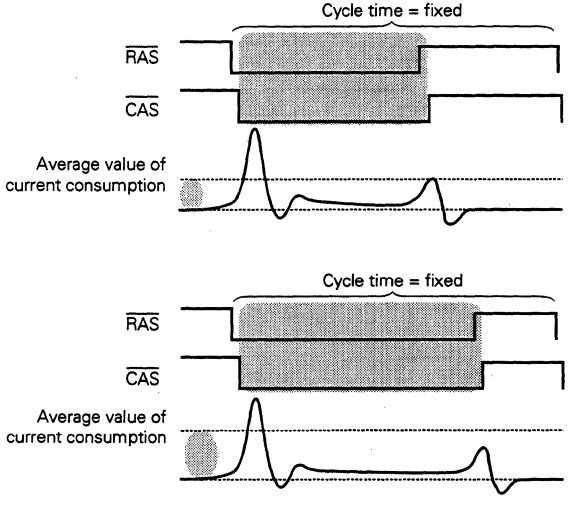
12.5 Current Consumption Dependence on $\overline{RAS}$ Pulse Width

Figure 12-6. Current Consumption - $\overline{RAS}$ Pulse Width Characteristics



As the $\overline{RAS}$ pulse width becomes longer, current consumption per unit time increases.

Figure 12-7. Average Current Consumption in Fixed Cycle Time

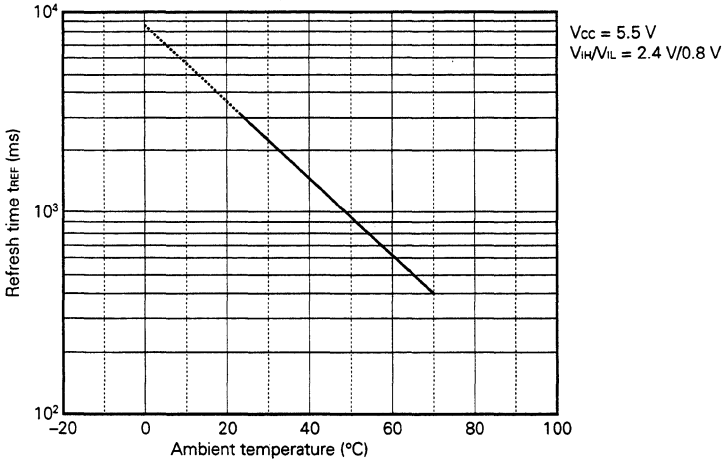


Fixing the cycle time and increasing the $\overline{RAS}$ pulse width result in reduction in the $\overline{RAS}$ precharge time. As the $\overline{RAS}$ pulse width is increased, the inactive time of $\overline{RAS}$ decreases and hence the average current consumption becomes larger.

12.6 Refresh Time Dependence on Ambient Temperature

Figure 12-8 shows the duration for which a high level can be read, supposing that the high level has been written and no refresh operation is performed.

Figure 12-8. Refresh Time - Ambient Temperature Characteristics



Remark The data were obtained by measurement using a sample extracted from a specific lot and do not indicate entire characteristics (they are not the assured values). Use them only for designing reference.

As ambient temperature rises, the leak in the capacitor tends to increase. In Figure 12-8, all memory cells (16,777,216 cells for 16M DRAM) are targeted rather than only one memory cell.

Therefore, the above figure indicates a point out of all memory cells where one or more data are destroyed.

12.7 Soft Error Rate (SER)

A memory can fail in the following two ways:

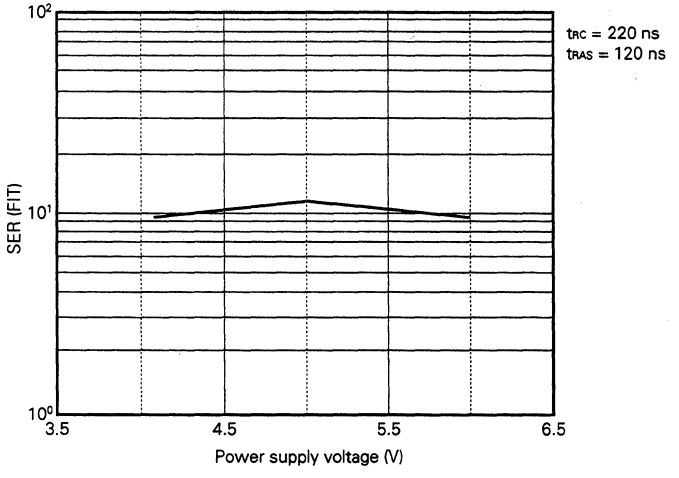
(1) The memory itself (hard) breaks due to application of some kind of stress.
(2) Data (soft) retained in the memory cell breaks.

Generally, a memory failure is due to (2) above.
Such a failure is called a soft error. Data are broken by alpha rays in the physical world. Data breakdown due to specification violation (any one of specifications listed in the data sheet is violated) is not included in category 2.

The soft error rate (SER) indicates the extent that data are broken under the above conditions and is normally expressed by FIT (Failure In Time). The FIT indicates the probability for failure per unit time, and 1 FIT is equal to 1×10^{-9} failures/time.

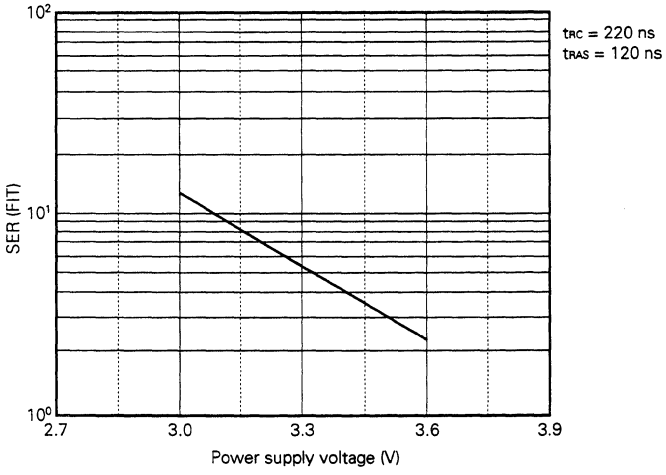
The FIT is a predicted value and varies depending on the memory usage conditions such as power supply voltage and access time and used environment such as ambient temperature.

Figure 12-9. Power Supply - SER Characteristics (5.0-V device)



Remark The data were obtained by measurement using a sample extracted from a specific lot and do not indicate entire characteristics (they are not the assured values). Use them only for designing reference.

Figure 12-10. Power Supply - SER Characteristics (3.3-V device)



Remark The data were obtained by measurement using a sample extracted from a specific lot and do not indicate entire characteristics (they are not the assured values). Use them only for designing reference.

Figure 12-11. $\overline{RAS}$ Cycle Time - SER Characteristics (5.0-V device)

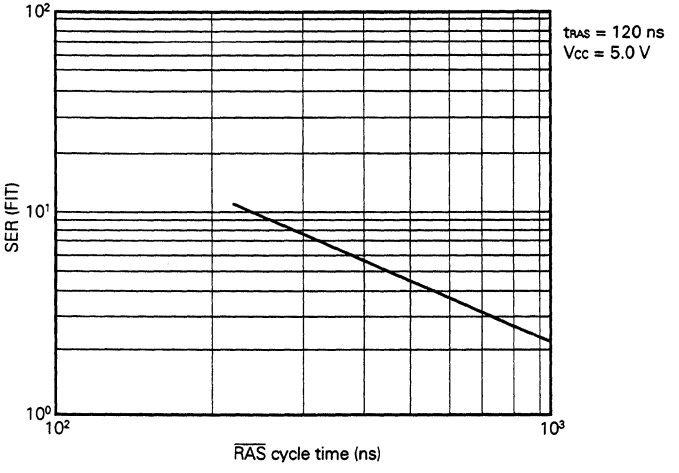
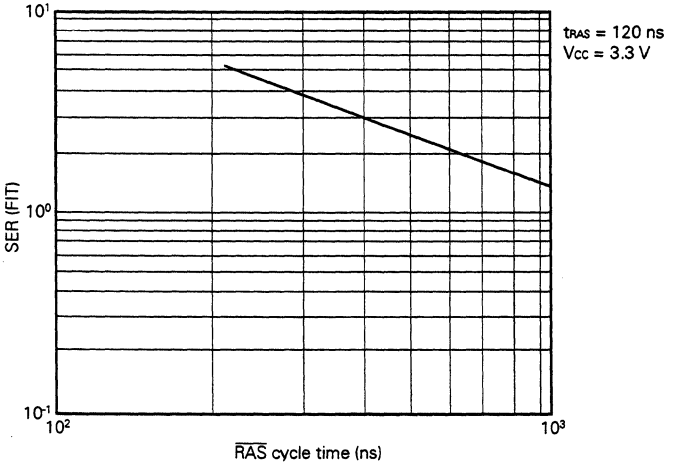


Figure 12-12. $\overline{RAS}$ Cycle Time - SER Characteristics (3.3-V device)



Remark The data were obtained by measurement using a sample extracted from a specific lot and do not indicate entire characteristics (they are not the assured values). Use them only for designing reference.

APPENDIX A DRAM DATA COLLECTION

The following shows the main characteristics of DRAM using 16M DRAM as an example.

The data were obtained by measurement using a sample extracted from a specific lot and do not indicate entire characteristics (they are not the assured values). Use them only for designing reference.

Normalization indicates the ratio of a value with a certain another value as 1.0.

A.1 Current Consumption Dependence on Power Supply Voltage

Figure A-1. I_{CC1}-Vcc Characteristics (3.3-V device)

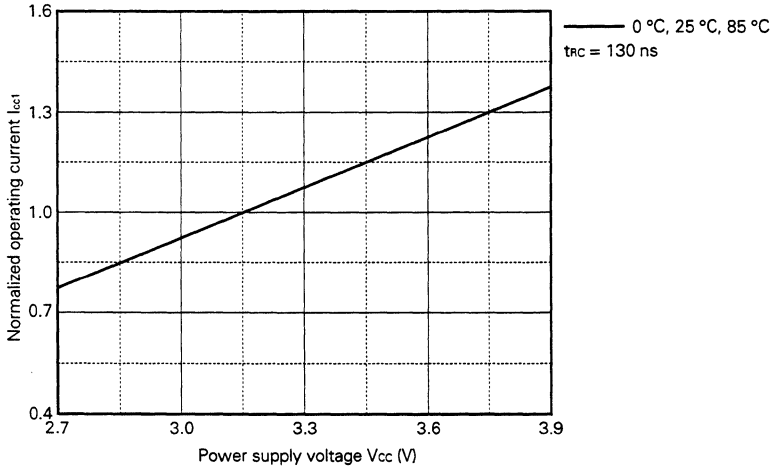
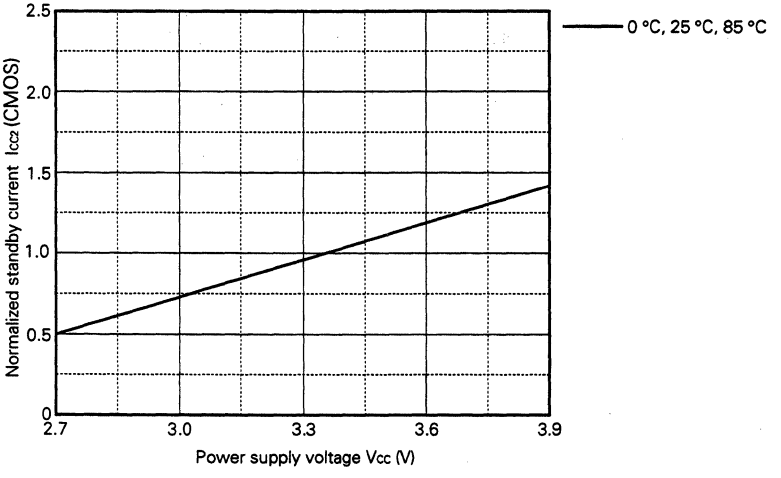


Figure A-2. I_{CC2}-V_{CC} Characteristics (3.3-V device)



Remark Standby refers to the memory condition where no operation is possible ($\overline{RAS}/\overline{CAS}$ inactive). Because, in the case of DRAM, refresh is required for retaining data, data cannot be retained in the standby mode.

Figure A-3. I_{CC3}-V_{CC} Characteristics (3.3-V device)

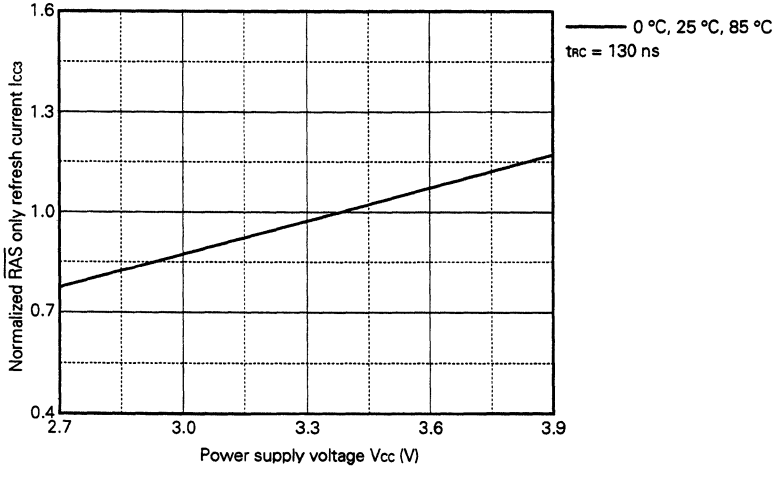


Figure A-4. I_{CC4}-V_{CC} Characteristics (3.3-V device)

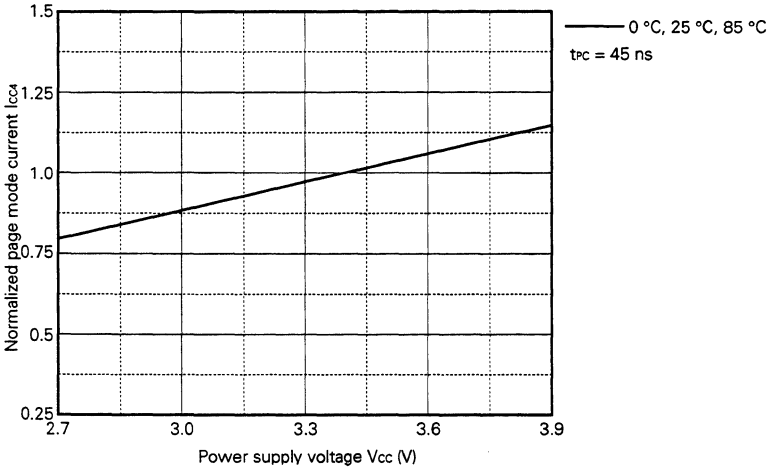


Figure A-5. I_{CC5}-V_{CC} Characteristics (3.3-V device)

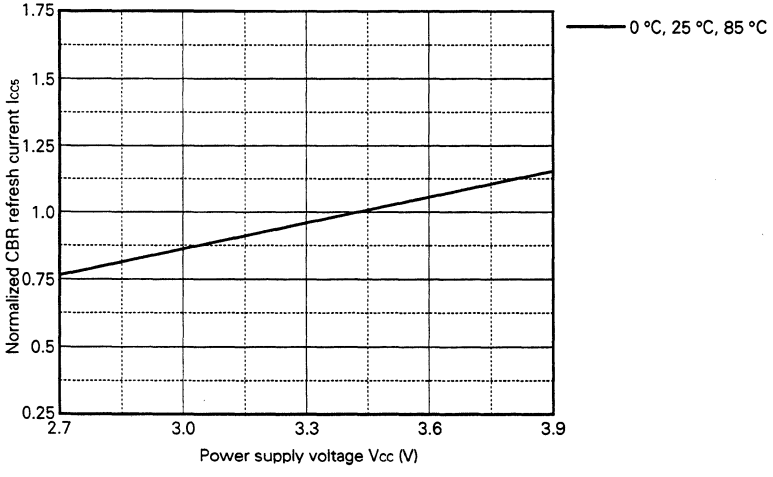


Figure A-6. I_{CC6}-V_{CC} Characteristics (3.3-V device)

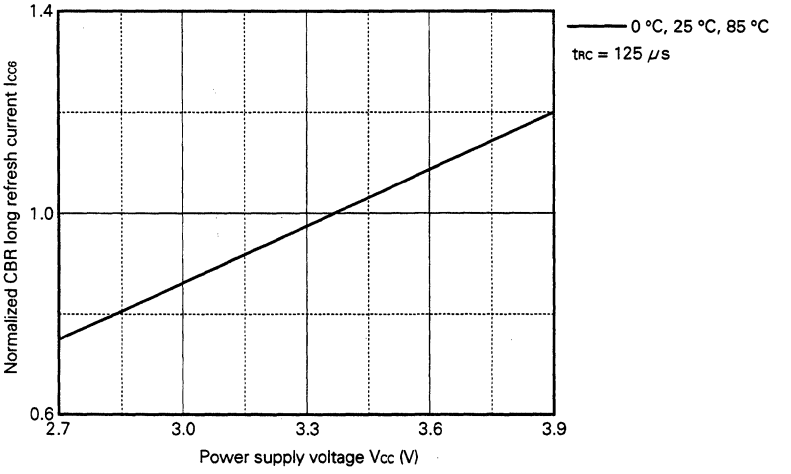


Figure A-7. I_{CC7}-V_{CC} Characteristics (3.3-V device)

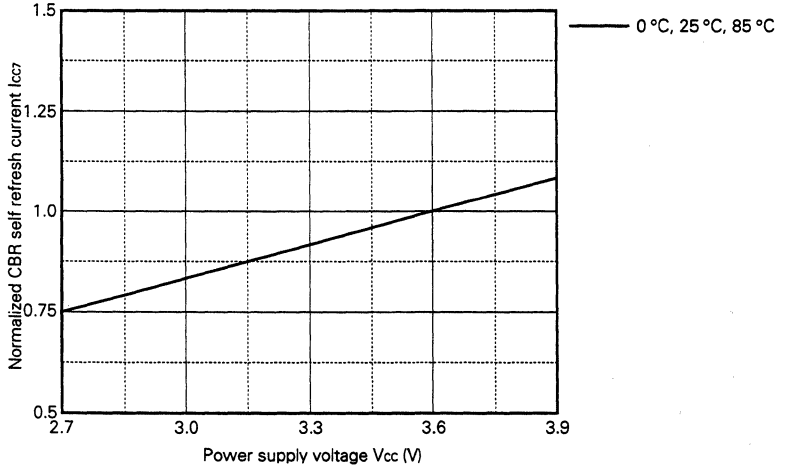


Figure A-8. I_{CC1}-V_{CC} Characteristics (5.0-V device)

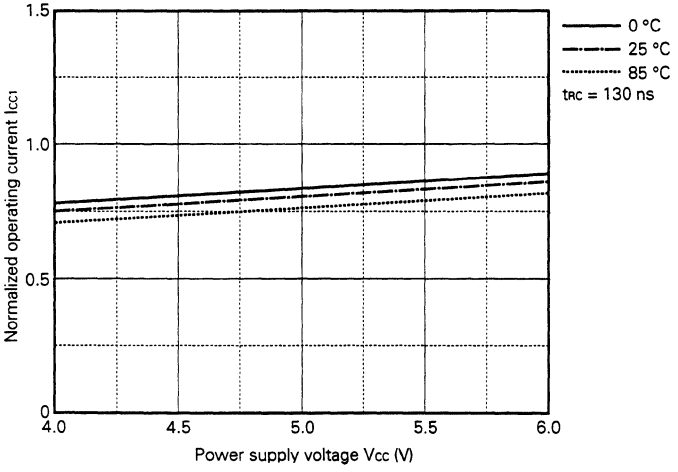
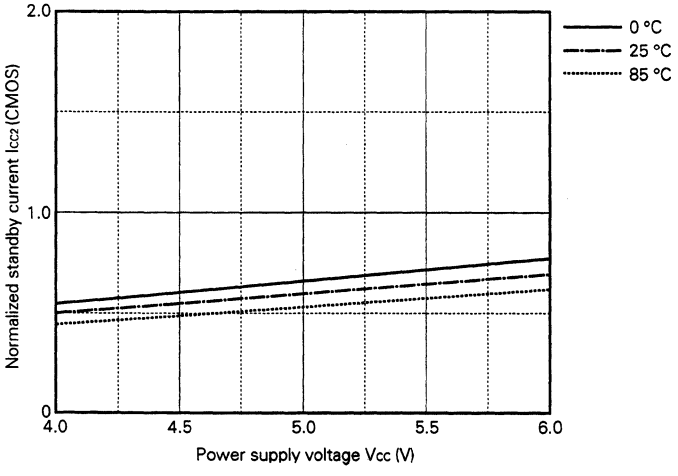


Figure A-9. I_{CC2}-V_{CC} Characteristics (5.0-V device)



Remark Standby refers to the memory condition where no operation is possible ($\overline{RAS}$/$\overline{CAS}$ inactive). Because, in the case of DRAM, refresh is required for retaining data, data cannot be retained in the standby mode.

Figure A-10. I_{CC3}-Vcc Characteristics (5.0-V device)

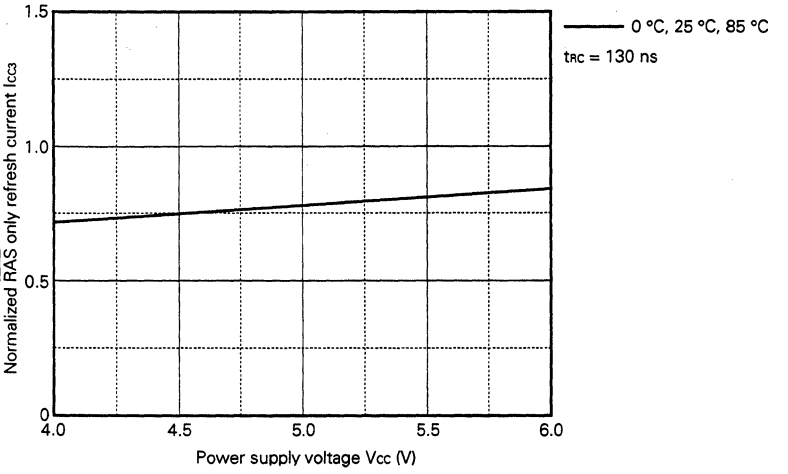


Figure A-11. I_{CC4}-Vcc Characteristics (5.0-V device, fast page mode)

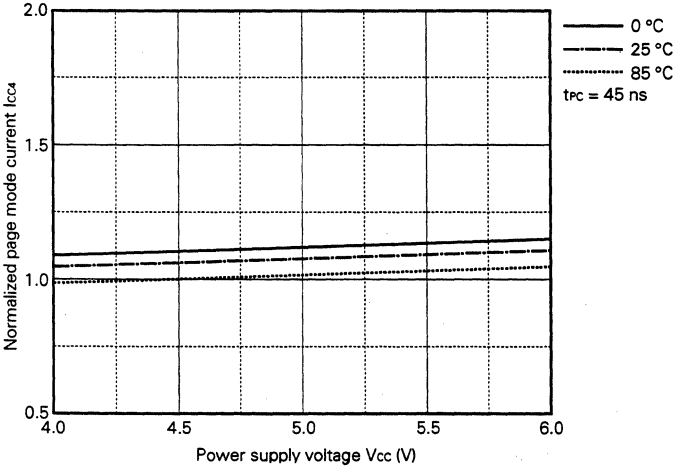


Figure A-12. I_{CC4}-V_{CC} Characteristics (5.0-V device, hyper page mode)

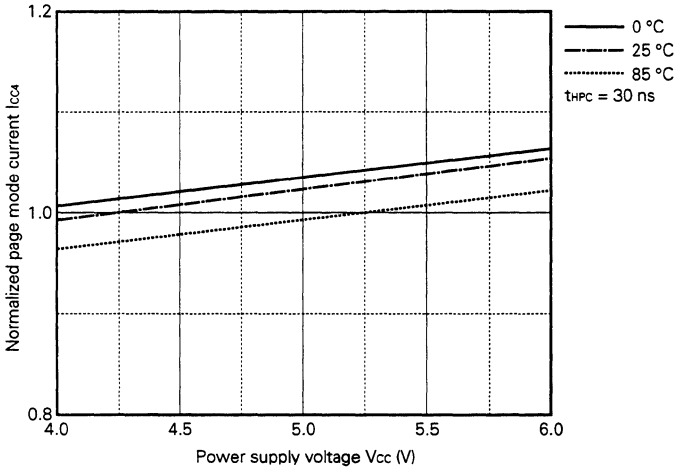


Figure A-13. I_{CC5}-V_{CC} Characteristics (5.0-V device)

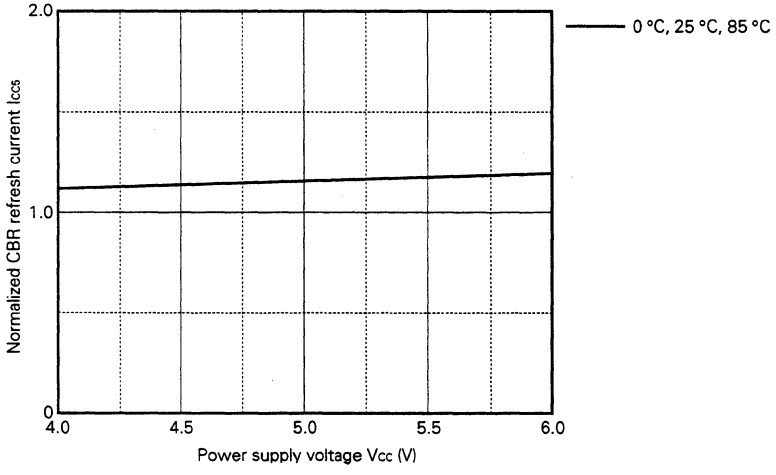


Figure A-14. I_{CC6}-V_{CC} Characteristics (5.0-V device)

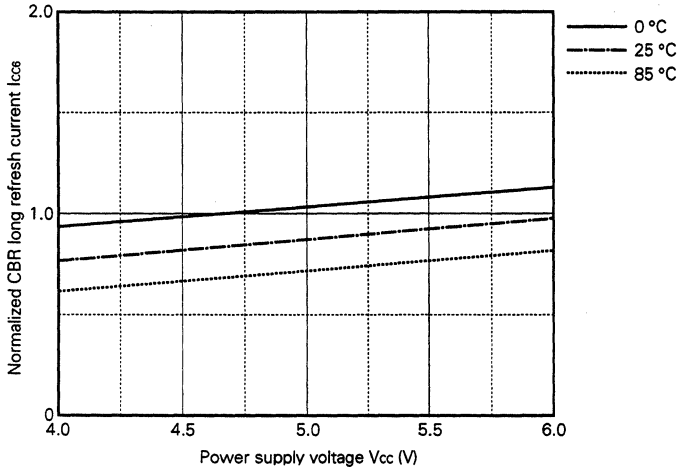
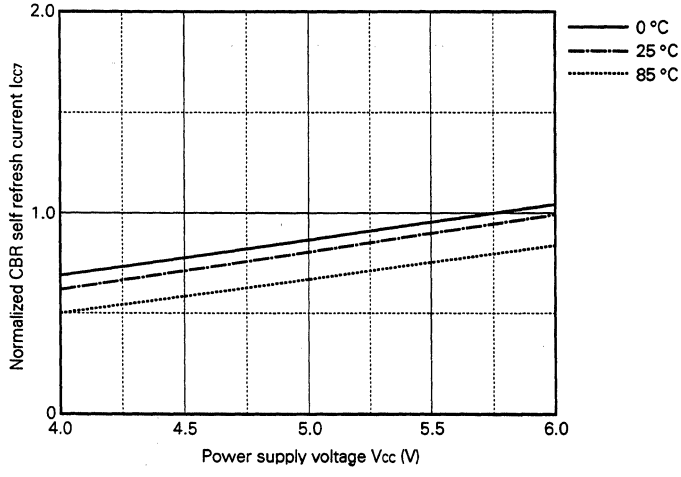


Figure A-15. I_{CC7}-V_{CC} Characteristics (5.0-V device)



A.2 Access Time Dependence on Power Supply Voltage

Figure A-16. V_{CC}-t_{RAC} Characteristics (3.3-V device)

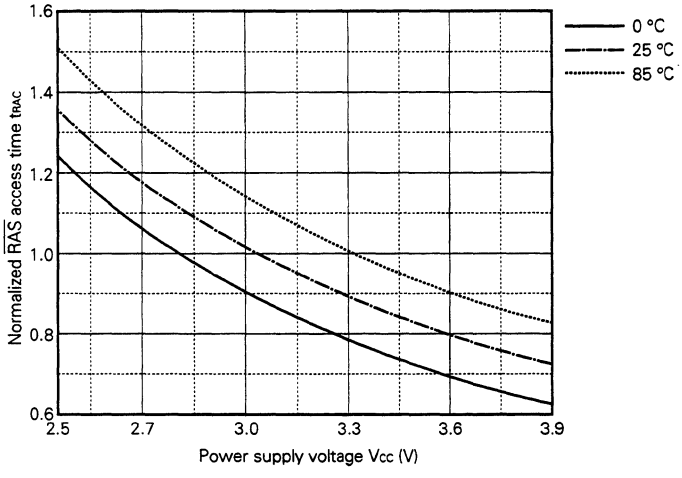


Figure A-17. V_{CC}-t_{CAC} Characteristics (3.3-V device)

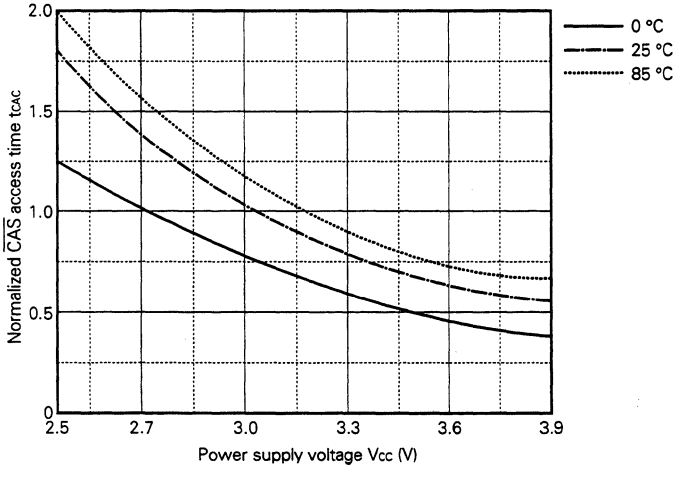


Figure A-18. V_{CC}-t_{AA} Characteristics (3.3-V device)

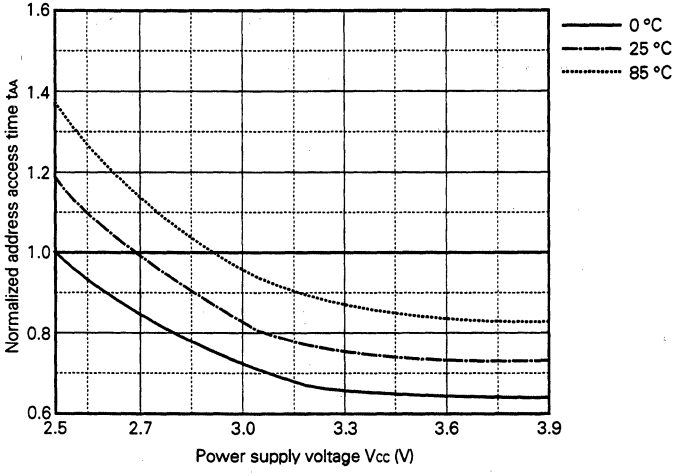


Figure A-19. V_{CC}-t_{ACP} Characteristics (3.3-V device)

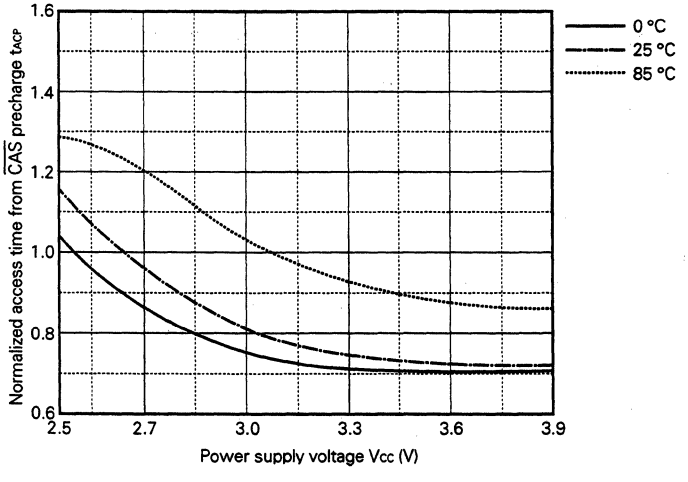


Figure A-20. V_{CC}-t_{OEA} Characteristics (3.3-V device)

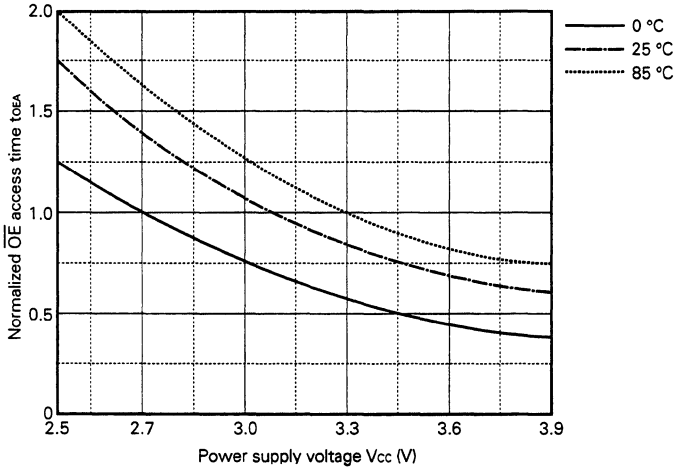
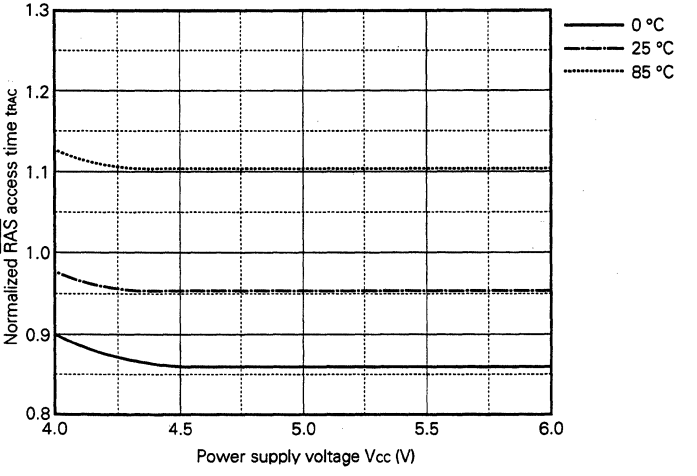


Figure A-21. V_{CC}-t_{RAC} Characteristics (5.0-V device)



The 5.0-V operation devices of 16M DRAM all adopt an internal voltage-drop circuit.

The internal voltage-drop circuit causes the power supply voltage (5.0 V) supplied to the memory externally to be dropped inside the memory and 5.0-V operation devices also operate on 3.3 V inside the memory. Therefore, there is almost no difference between the current consumption of a 5.0-V operation device and that of a low-voltage operation device. The low-voltage operation device of 16M DRAM does not adopt any internal voltage-drop circuit.

Figure A-22. V_{CC}-t_{CAC} Characteristics (5.0-V device)

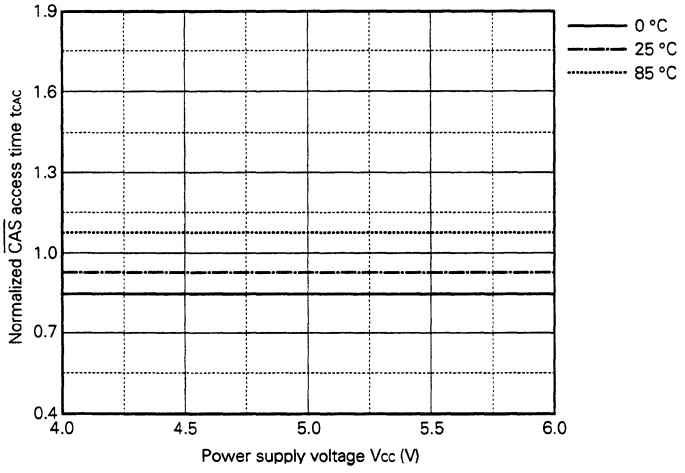


Figure A-23. V_{CC}-t_{AA} Characteristics (5.0-V device)

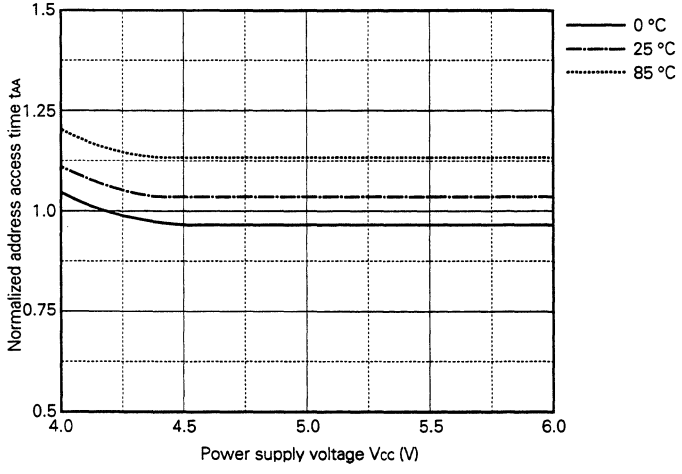


Figure A-24. V_{CC}-t_{ACP} Characteristics (5.0-V device)

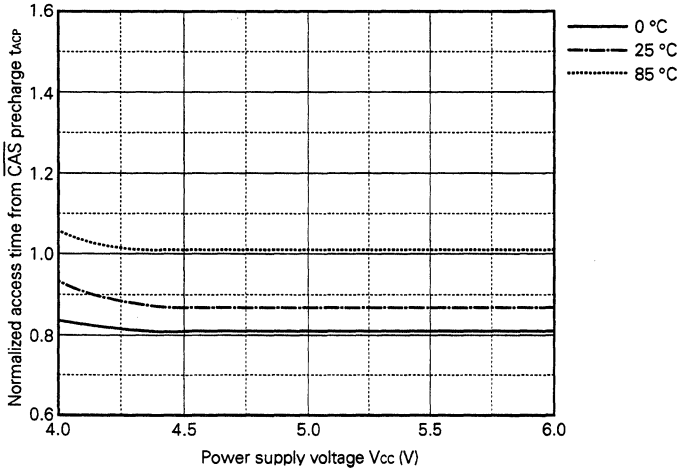
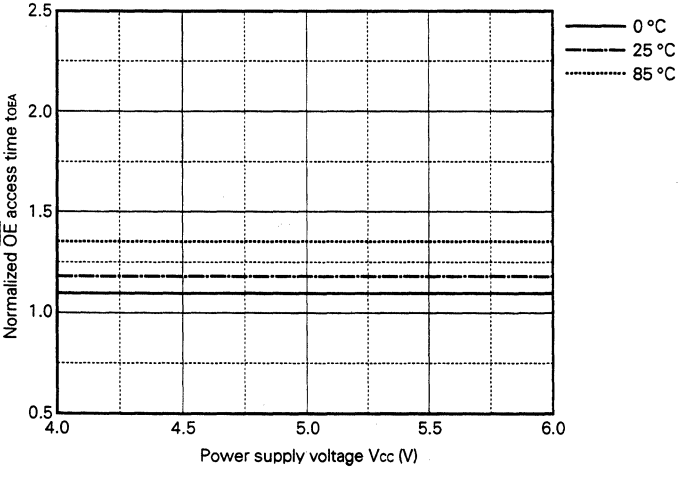


Figure A-25. V_{CC}-t_{OEA} Characteristics (5.0-V device)



A.3 Current Consumption Dependence on Cycle Time

Figure A-26. I_{CC1}-t_{RC} Characteristics (5.0-V device)

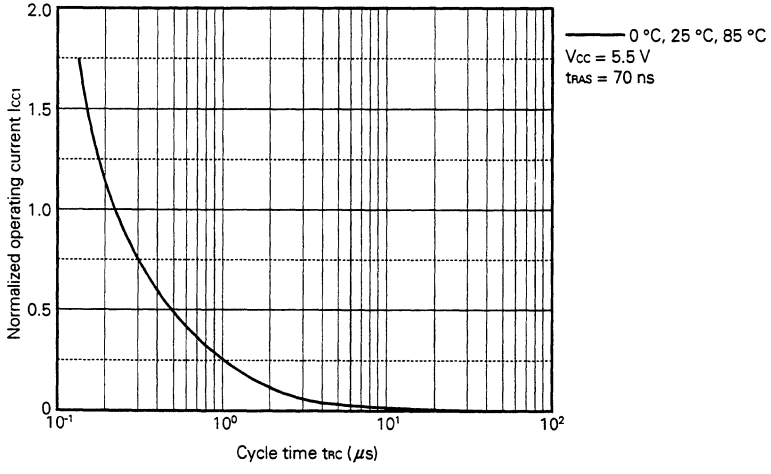


Figure A-27. I_{CC3}-t_{RC} Characteristics (5.0-V device)

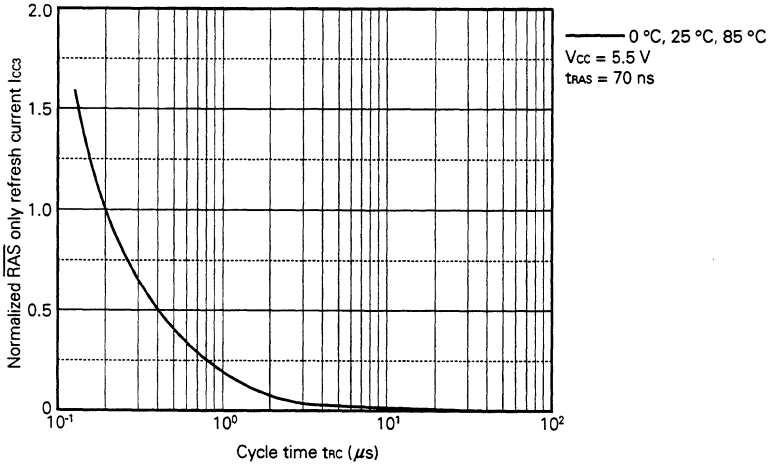


Figure A-28. I_{CC4}-t_{PC} Characteristics (5.0-V device)

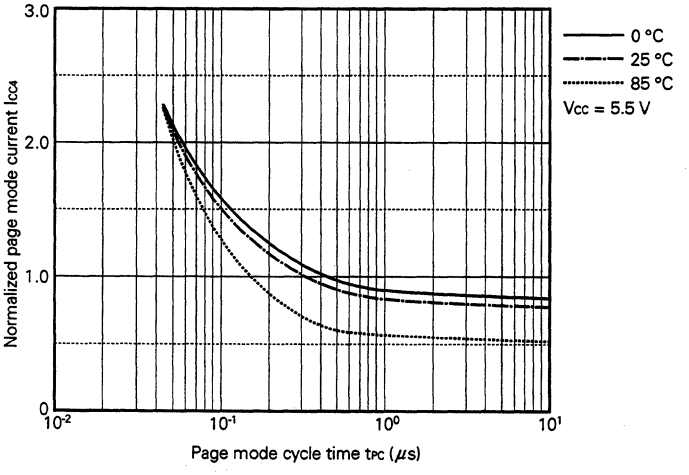


Figure A-29. I_{CC4}-t_{HPC} Characteristics (5.0-V device)

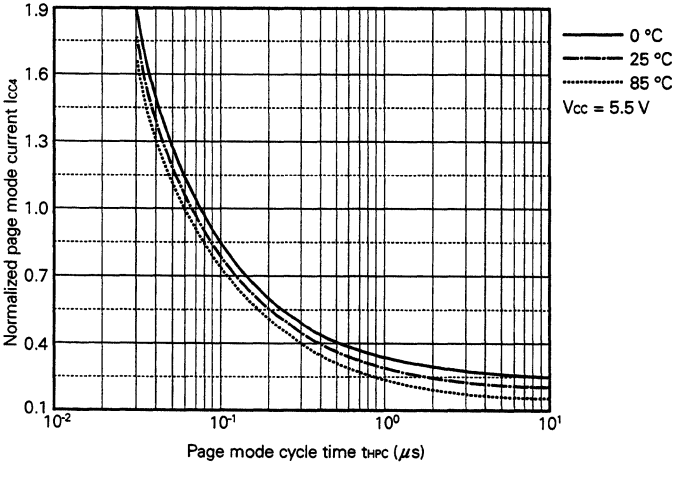


Figure A-30. I_{CC6}-t_{RC} Characteristics (5.0-V device)

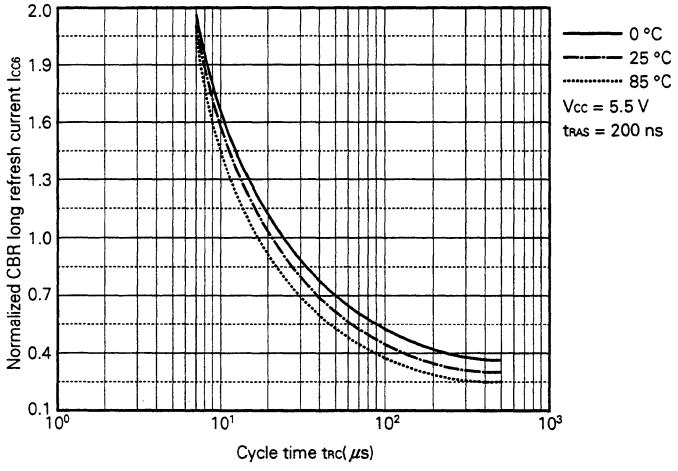


Figure A-31. I_{CC1}-t_{RAS} Characteristics (5.0-V device)

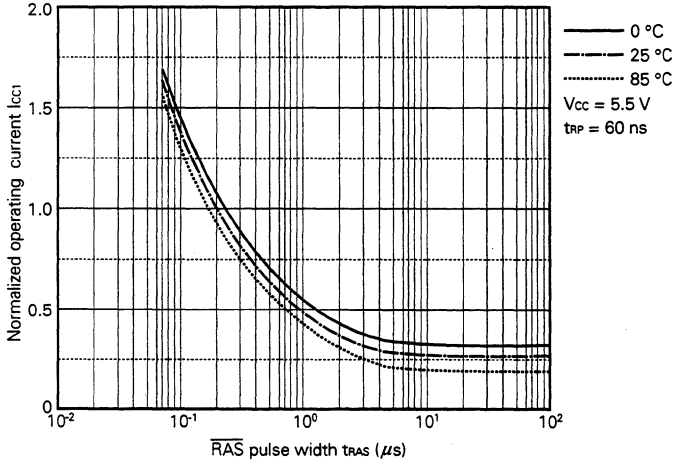


Figure A-32. I_{CC3}-t_{RAS} Characteristics (3.3-V device)

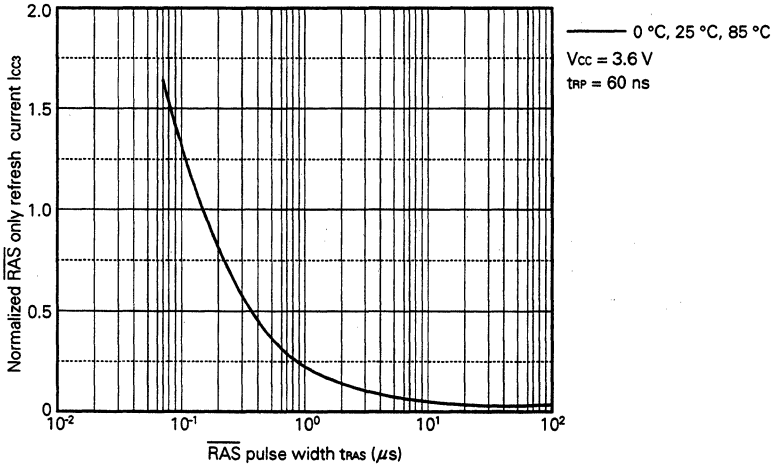


Figure A-33. I_{CC3}-t_{RAS} Characteristics (5.0-V device)

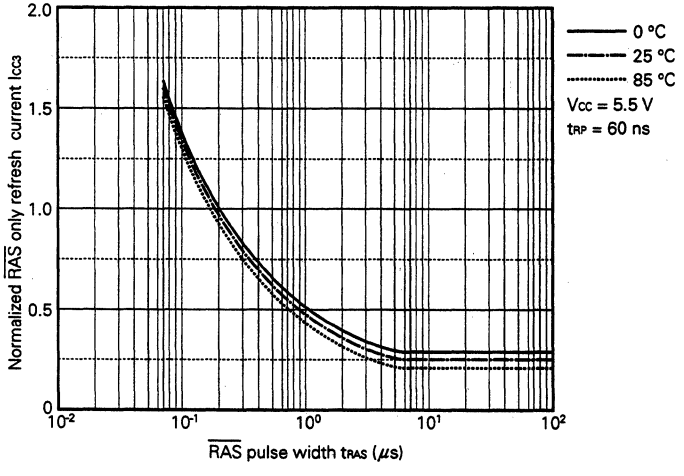
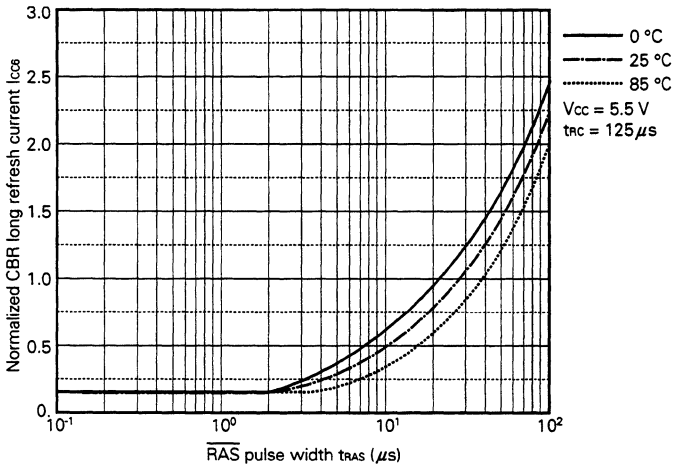


Figure A-34. I_{CC6}-t_{RAS} Characteristics (5.0-V device)

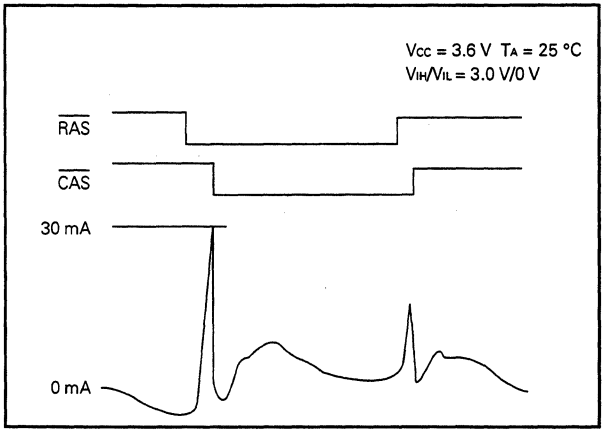


A.4 Current Consumption Waveform

When $\overline{RAS}$ is activated, the sense amplifier is also activated and hence current consumption is maximized at that instant (peak current).

The data in Figures A-1 through A-34 indicate the average current consumption. In reality, however, there is a current consumption peak, as shown in Figure A-35.

Figure A-35. $\overline{RAS}$/$\overline{CAS}$ Cycle Current Consumption Waveform



NEC Semiconductor Device Reliability/Quality Control System

INFORMATION

NEC

NEC SEMICONDUCTOR DEVICE RELIABILITY/QUALITY CONTROL SYSTEM

MICROCOMPUTER LSI

MEMORY IC

GATE ARRAY

LOGIC LSI

The information in this document is subject to change without notice.

Document No. C10983EJ3V0IFU1

1. BASIC PRINCIPLES OF RELIABILITY/QUALITY CONTROL SYSTEM

NEC's reliability/quality control of semiconductors is based on the thorough integration of the reliable management in market analysis, development and design of the products meeting users' needs, and manufacturing process design, on one hand, and, quality control in materials and parts supply, each and every manufacturing process, direct and reliable assurance of thorough examination and reliability test of the products, and shipment and after-sale service management, on the other. It is our pleasure and pride to serve our customers best through a product-specific efficient management system to realize reliable quality and reasonable prices to the satisfaction of the users.

As the semiconductor application fields expand and develop, the amount used in those areas is increasing tremendously. The needs of our customers for higher and higher product quality are inevitable results of the development of the electronic industry.

To meet such users' needs, the NEC concentrates on the following three key points:

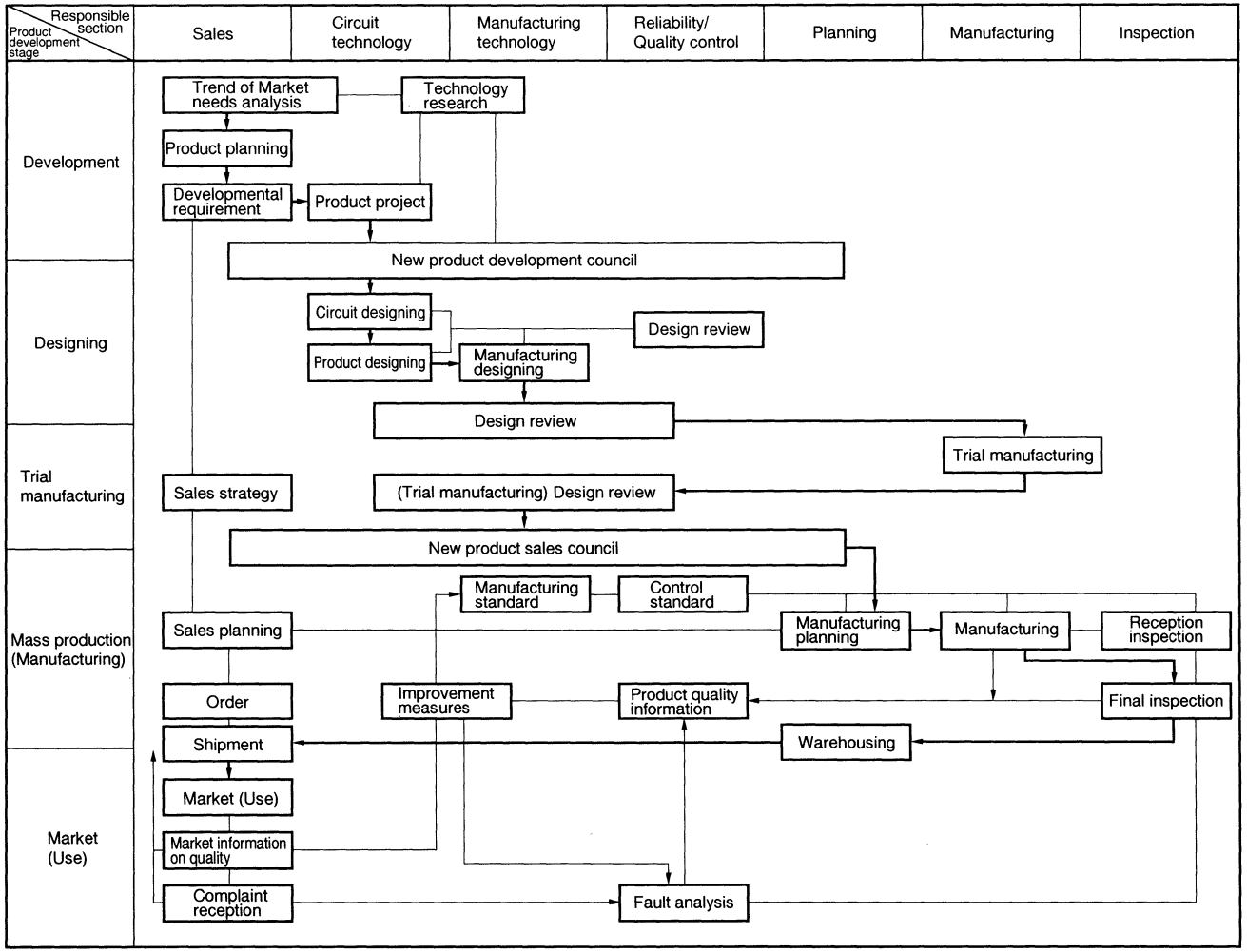
(1) Master design of key aspects of the product characteristics
(2) Quality control system built in the manufacturing process
(3) Removal of fault products through inspection of the products

The followings are our routine practices assure high quality products:

(a) Standardized designing practices to built reliability in to the developed products.
(b) Thorough examination of potential factors that may cause fault products at the design examination stage.
(c) Exhaustive and thoroughgoing evaluation of the characteristics and reliability test of the test products.
(d) Automated manufacturing equipment to reduce variability in the product quality.
(e) Quality control at each and every manufacturing process meeting the process-specific requirements.
(f) Built-in learning process to increase workers' awareness of the importance of the product quality through small group activities such as the ZD (Zero-defect) groups or QC circles.
(g) Product-specific screening, inspection, and reliability tests.
(h) Analysis of quality information, including the field data, and feed back/forward of the analysis results.

Through these effective measures, we believe that NEC can satisfy users' needs for its high quality products. It is not, however, the end of our efforts: we still try our best to improve the quality of our products. Figure 1 diagrammatically describes, our quality (Q) and reliability (R) control.

Fig. 1 Q and R System Diagram



2. MANUFACTURING PROCESS QUALITY CONTROL

NEC manufactures and sells its semiconductor products under the management policy of "Reliability Quality Control" based on an accurate understanding of customers' needs and operating conditions realized in the product designs.

To secure the intended reliability and quality in the product design, possible causes of off-grade products in the manufacturing processes must be eliminated in each step of the production line through qualified manufacturing management.

For the purpose, we carefully control the quality of the parts, materials and related goods, manufacturing equipment and environment. In addition, inspection processes are inserted in the manufacturing process to check the semifinal-final products by referring to key control items at proper sampling frequency.

The above-described quality control system is explained in detail referring to the flow chart Fig. 2 - Fig. 6.

The following is a brief explanation of the material/parts control system.

First, parts, materials, chemicals, highly pure gases, and other related goods are purchased from specific manufacturers authorized by NEC.

The results of the inspection are monitored and, when necessary, corrective measures are requested to the identified suppliers or the plants are audited by the purchase division to maintain quality of the purchased items.

Fig. 2 Manufacturing Process Control Flow Chart:
Example of Plastic Molded DIP, SOP, SOJ and QFJ (PLCC)

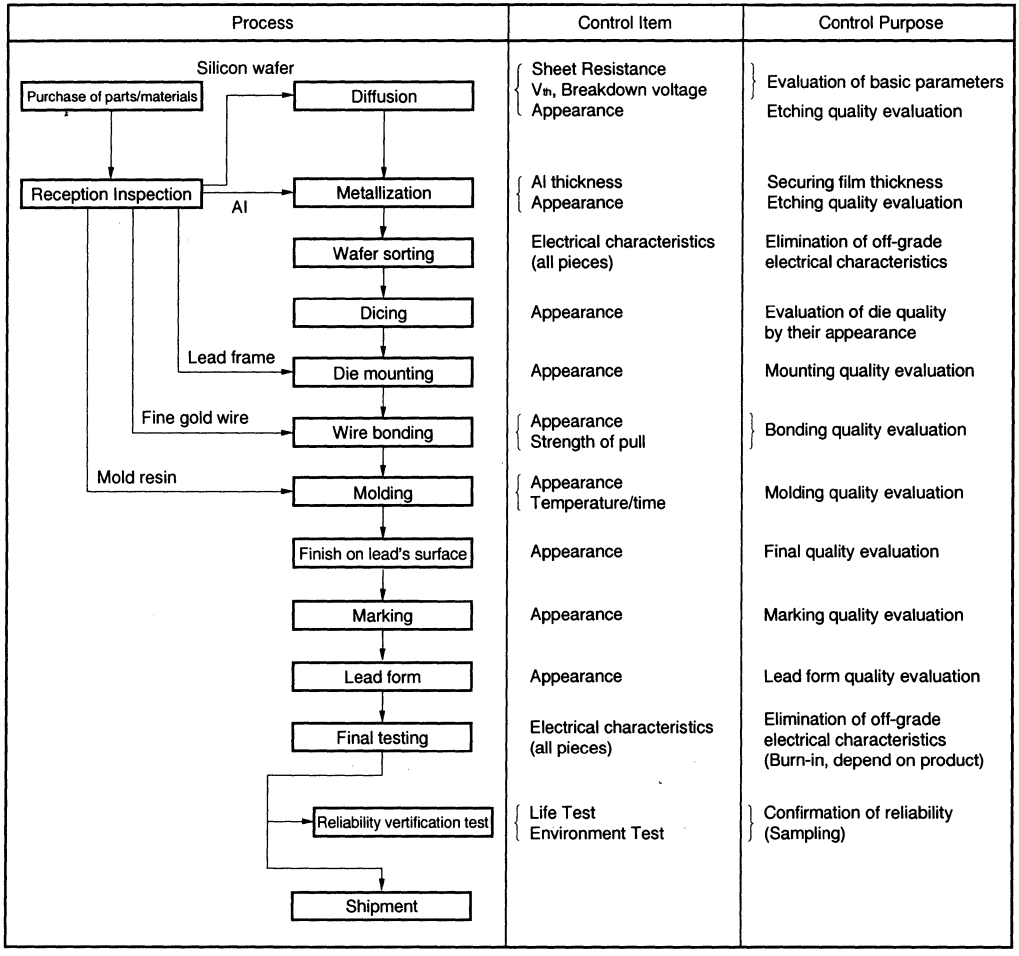


Fig. 3 Manufacturing Process Control Flow Chart: Example of Plastic Molded QFP and TSOP

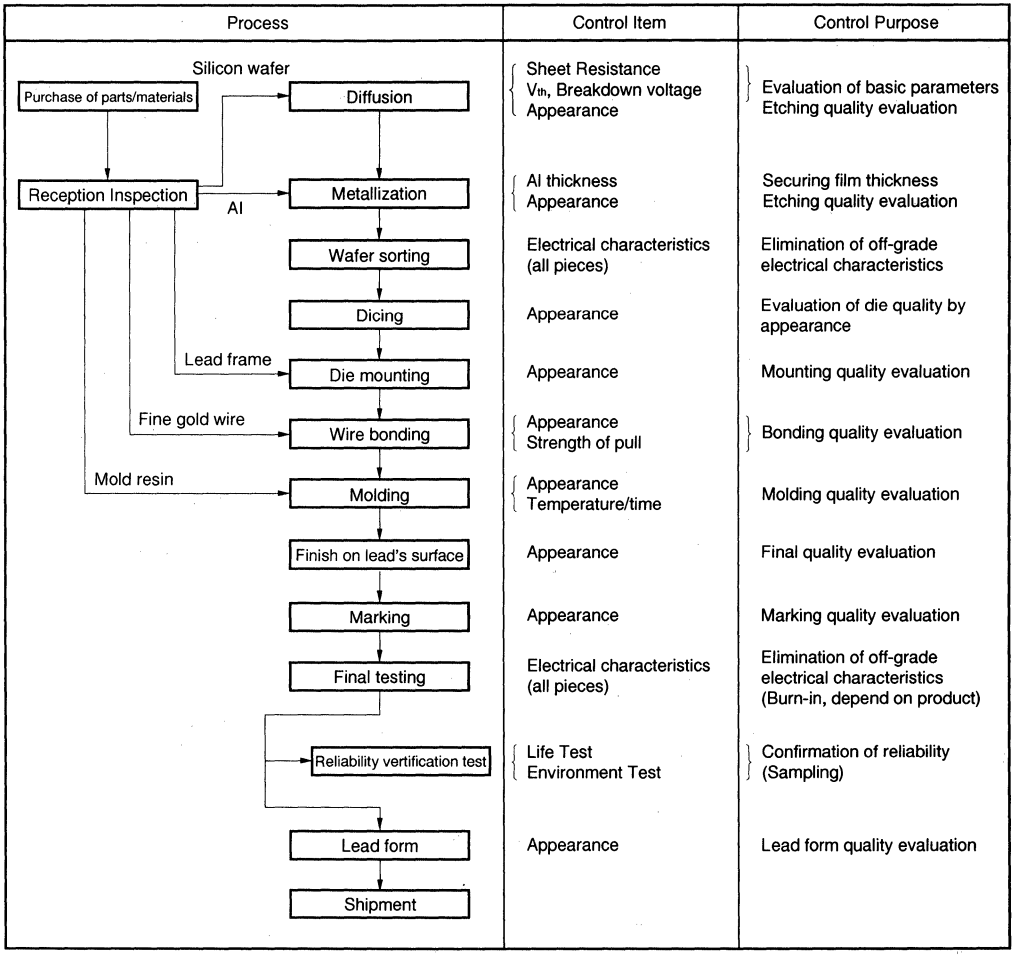


Fig. 4 Manufacturing Process Control Flow Chart: Example of PPGA

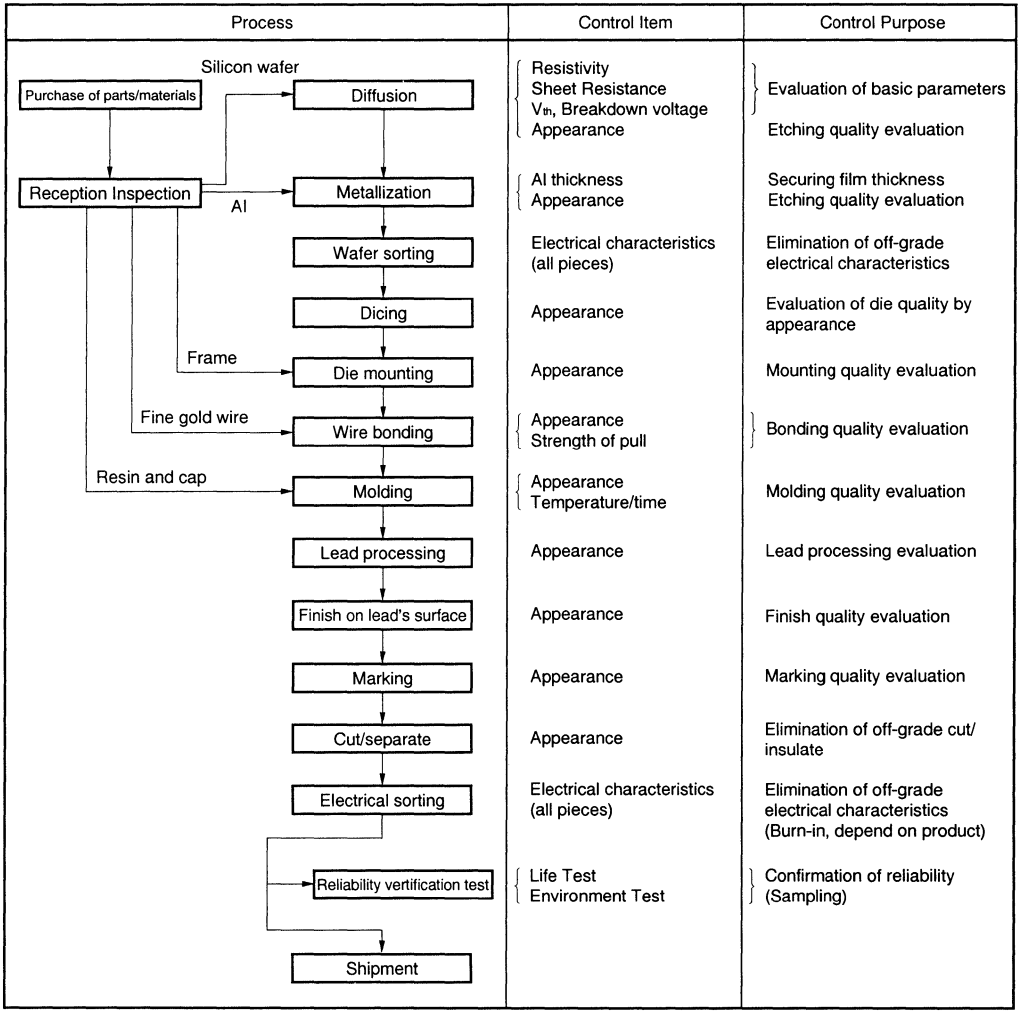


Fig. 5 Manufacturing Process Control Flow Chart: Example of Ceramic DIP (CERDIP)

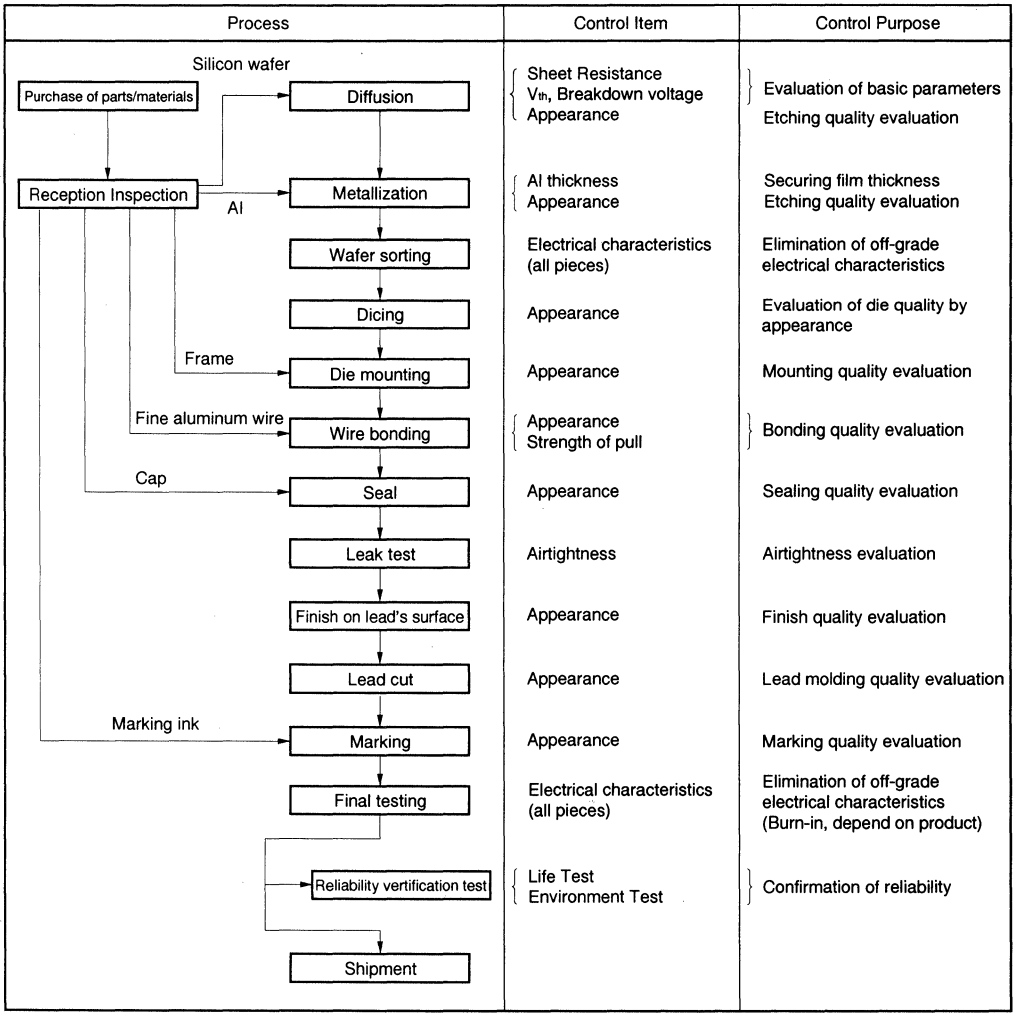
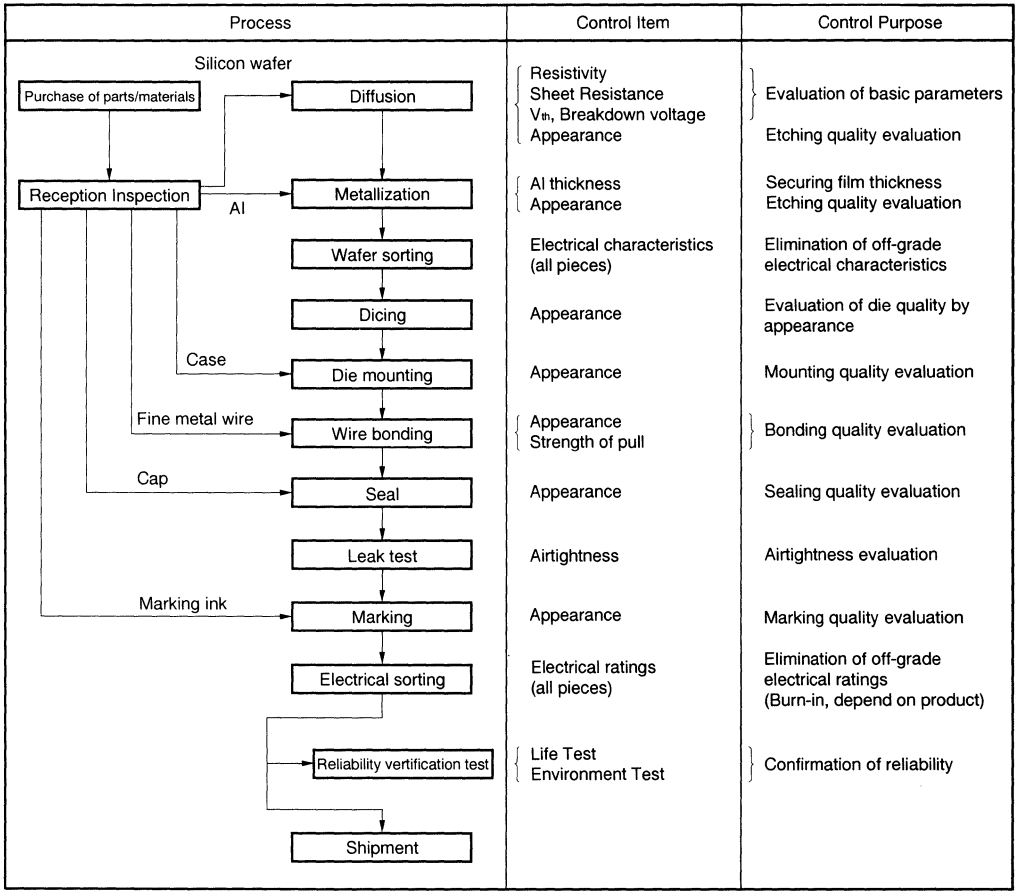


Fig. 6 Manufacturing Process Control Flow Chart:
Example of Ceramic DIP (SEAM WELD), Ceramic QFN (LCC), and Ceramic PGA



3. RELIABILITY TEST

NEC's reliability test is conducted periodically, considering various standards such as JIS C 7022, MIL-STD-883, and other standards.

The following, section 3.1 describes an example of the reliability test, and section 3.2, fault evaluation criteria in the reliability test.

3.1 DESCRIPTION OF THE RELIABILITY TEST

Reliability Test: Example of Plastic Packages

Test Item		Test Condition	Sample Size	Equipment Test Method	
				JIS C 7022	MIL-STD-883
Resistance to Soldering Heat*1		Soak the product in melted solder at 260 ±5 °C with no flux from 10 seconds. 1.6 ±0.8 mm deep from the product or its tab-stud.	18	A-1 Condition A	—
Temperature Cycle		Soak the product in a low temperature (T_{stg} min.) bath for 30 minutes then another 30 minutes in a high-temperature (T_{stg} max.) bath. Repeat this cycle 10 times.		A-4	1010 Condition C
Thermal Shock		Soak the product in a prescribed liquid at 100 °C for at least 5 minutes. Then, within 10 seconds, soak it in a prescribed liquid at 0 °C for at least 5 minutes. Repeat this cycle 15 times.		A-3 Condition A Method II	1011 Condition A
Solderability		Soak the device in noncorrosive flux up to 1.27 mm deep from the product for 5 to 10 seconds then in flux of melt solder at 230 ±5 °C with a soaking speed of 25.4 ±6.3 mm/s, again up to 1.27 mm deep from the device for 5 seconds. Wash away the flux in alcohol and examine the soldered area of the device.	5	A-2	2003
Terminal Strength	Bending*1	Apply a weight*2 to the lead of the product in a vertical direction of the axis of the lead without causing twist in it until the lead bends by 90 degrees, then release it. Repeat this operation three times. Apply this operation separately to 3 randomly chosen terminals.	5	—	2004 Condition B2
High-Temperature Storage		Conduct the left test in an environment atmosphere at 150 °C for 1000 hours.	18	B-3	1008
High-Temperature Bias		In an environmental atmosphere at 125 °C, apply the upper limit supply voltage of the recommended operating conditions for 1000 hours to conduct the bias life test.	24	B-1	1005 Condition A,B, and C
High-Temperature/ Humidity Storage		Conduct the life test in an atmosphere with relative humidity of 85 % at temperature of 85 °C for 1000 hours.	26	B-5 Condition B	—
PCT		Expose the device to vapor having a pressure of 2.3×10^5 Pa (2.3 barometric pressure) in an atmosphere at 125 °C for 96 hours.	18	—	—

***1)** PLCC is not subjected to this test.

***2)** The DIP and PPGA weight 250 grams; the SOP, QFP and QUIP weight 125 grams each.

Reliability Test: Example of Ceramic Packages

Test Item	Test Condition	Sample Size	Equipment Test Method	
			JIS C 7022	MIL-STD-883
Resistance to Soldering Heat*3	Soak the product in melted solder at 260 ±5 °C with no flux from 10 seconds. 1.6 ±0.8 mm deep from the product or its tab-stud.	18	A-1 Condition A	—
Temperature Cycle	Soak the product in a low temperature (T_{stg} min.) bath for 30 minutes, then another 30 minutes in a high-temperature (T_{stg} max.) bath. Repeat this cycle 10 times.		A-4	1010 Condition C
Thermal Shock	Soak the product in a prescribed liquid at 100 °C for at least 5 minutes. Then, within 10 seconds, soak it in a prescribed liquid at 0 °C for at least 5 minutes. Repeat this cycle 15 times.		A-3 Condition A Method II	1011 Condition A
Variable Frequency Oscillation	Fix the product on a vibrator and apply sine wave oscillation in the X, Y, and Z directions that logarithmically changes in the range between 10 to 2000, then 2000 to 10 Hz in 4 minutes, with a peak acceleration of 20 G.	18	A-10	2007 Condition A
Mechanical Shock	Mount the product on a shock tester and subject it to a shock of 1500 G (500 G*1) in acceleration and 0.5 ms in the pulse width, in the X, Y, and Z directions 3 times each.		A-7 Condition F, D	2002 Condition B, A
Constant Acceleration	Fix the product on the tester and subject it to a centrifugal acceleration of 20000 G (5000 G*2) is applied in the X, Y, and Z directions for 1 minute in each.		A-9 Condition C, A	2001 Condition A
Solderability	Soak the device in noncorrosive flux up to 1.27 mm deep from the product for 5 to 10 seconds, then in flux of melted solder at 230 ±5 °C at a soaking speed of 25.4 ±6.3 mm/s, again up to 1.27 mm deep from the device for 5 seconds. Wash away the flux in alcohol and examine the soldered area of the device.	5	A-2	2003
Terminal Strength — Bending*3	Apply a prescribed weight to the lead of the product in a vertical direction of the axis of the lead without causing twist in it until the lead bends by 90 ±5 degrees, then release it. Repeat this three times. Apply this separately to 3 randomly chosen terminals.	5	—	2004 Condition B2
High-Temperature Storage	Conduct the life test in an environmental atmosphere at 150 °C for 1000 hours.	18	B-3	1008
High-Temperature Bias	In an environmental atmosphere at 125 °C, apply the upper limit supply voltage of the recommended operating conditions for 1000 hours to conduct the bias life test.	24	B-1	1005 Condition A,B, and C

***1)** Glass-windowed products. ***2)** Glass-windowed products and products with heat sink.

***3)** The LCC is not subjected to this test.

3.2 FAULT EVALUATION CRITERIA IN RELIABILITY TEST

Example of Plastic Package Product

Testing Item	Fault Evaluation Criterion	
Resistance to Soldering Heat* Temperature Cycle Thermal Shock* High-Temperature Storage High-Temperature Bias High-Temperature/Humidity/Storage PCT	Within tolerance of the electrical characteristics	
Terminal Strength (Bending)*	Lead appearance	No breaking/Loosening
Solderability	Lead appearance	Above 95 % Solder Coverage of Tested Surface

*The PLCC is not subjected to this test.

Example of Ceramic Package Product

Testing Item	Fault Evaluation Criterion	
Resistance to Soldering Heat* Temperature Cycle Thermal Shock Variable Frequency Oscillation Mechanical Shock Constant Acceleration High-Temperature Storage High-Temperature Bias	Within tolerance of the electrical characteristics	
Terminal Strength (Bending)*	Lead appearance	No breaking/Loosening
Solderability	Lead appearance	Above 95 % Solder Coverage of Tested Surface

*The LCC is not subjected to this test.

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