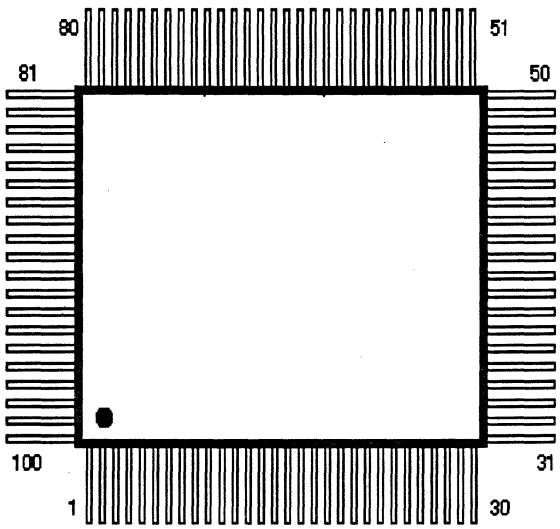
NCL2020 - FLOPPY DISK CONTROLLER

GENERAL DESCRIPTION

The NCL2020 is a single chip, floppy disk controller for the PC/AT compatible systems. It combines the industry standard FDC, analog data seperator, write precompensation, clock generation, data rate selection and all Host/Drive interface drivers/receivers. The NCL2020 provides all control and communications between the host and floppy drive(s).

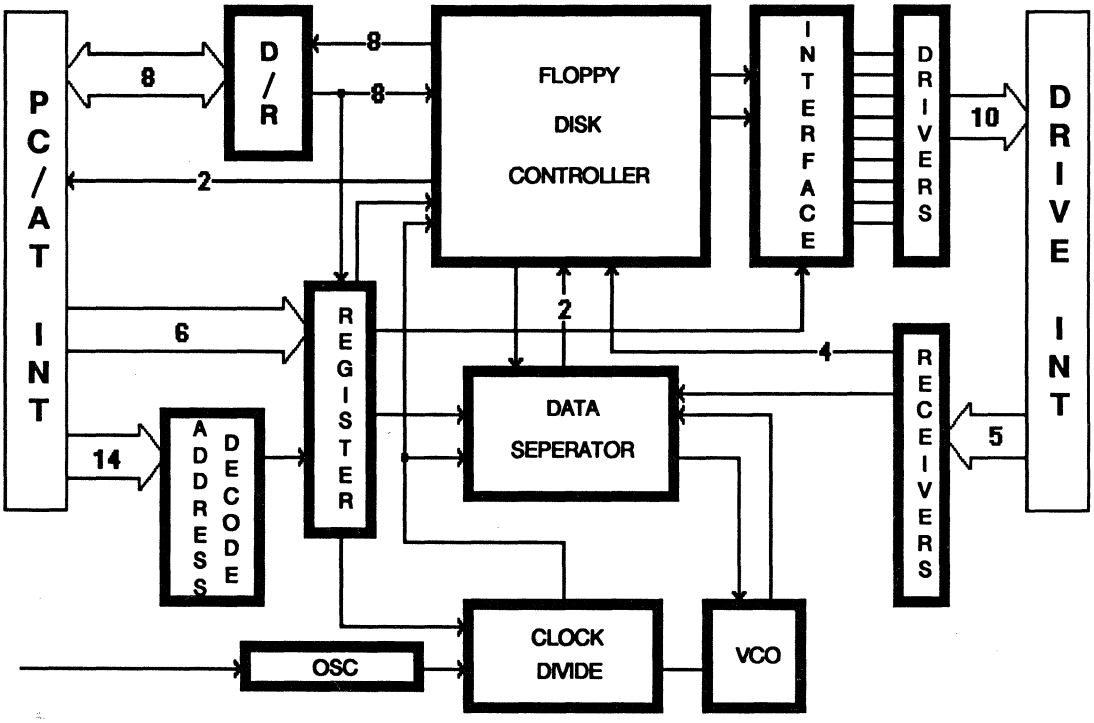
FEATURES

- o IBM PC/AT compatible format and bus interface
- o IBM PC/AT compatible commands and register
- o DMA/PIO data transfer
- o Embedded address decoder for chip and register select
- o No adjustment, no external components analog VCO
- o Programable data transfer rates (250,300,500Kb)
- o Embedded drivers/receivers for both host and drive
- o Recalibrate up to 77 tracks
- o Data scan function
- o Supports overlap seek
- o Supports up to 2 drives
- o Full CMOS LSI
- o Single +5 volt supply
- o Single 24Mhz crystal input
- o Available in 100 pin flat pack
- o Controls 5.25" and 3.5" drives



100 pin flat pack

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

FDC - Industry standard floppy disk controller. Recalibrate up to 77 cylinders.

Data Seperator - Generates the window for data seperation from raw read data (MFM). Includes phase comparator to generate VCO control signal.

VCO - Voltage controlled oscillator. Center frequency is 4Mhz with 1.25mhz/v sensitivity.

OSC/Divider - Generates all clocks for each function block from external 24Mhz crystal. Divider is programable for the different data rates.

Address Decoder - Address decode for chip select and task register select. Decodes both primary and secondary addresses.

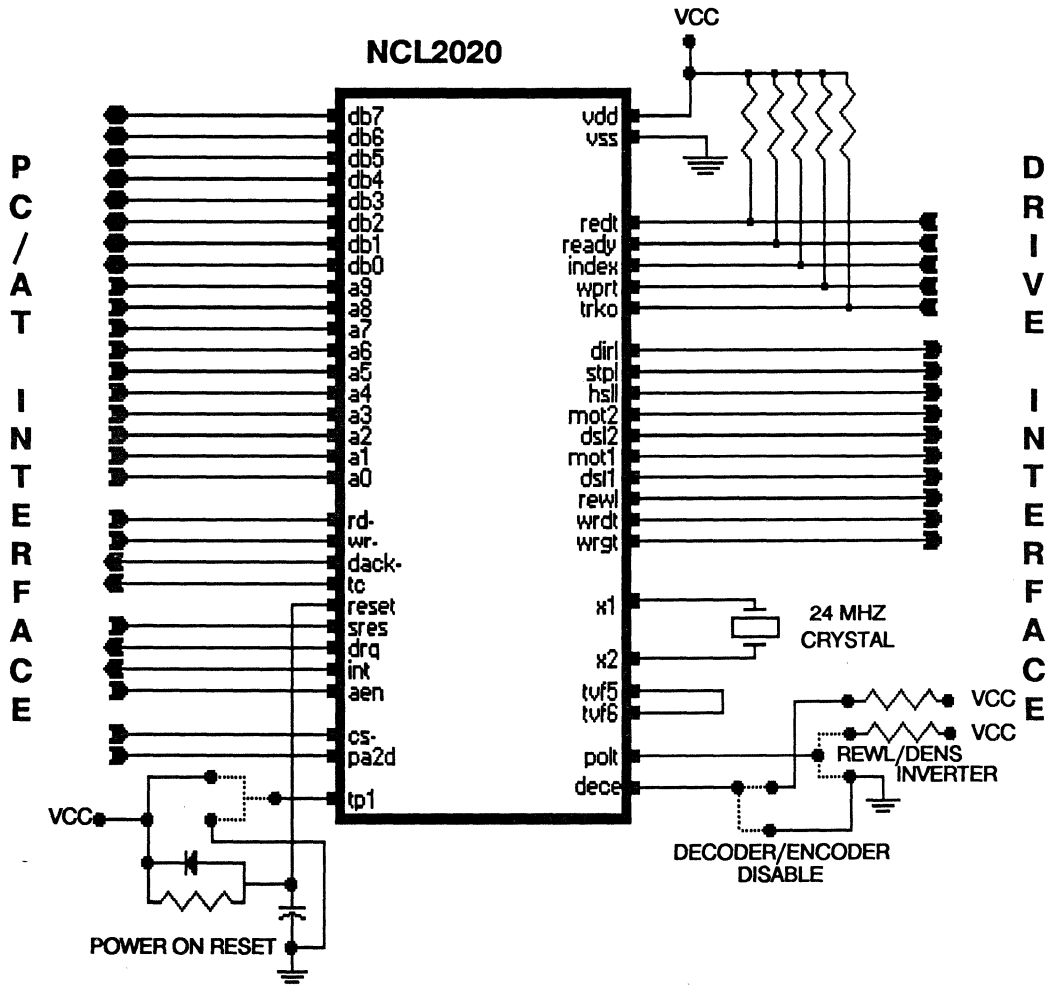
Host Interface Driver/Receiver - Bi-directional Bus driver/receiver. Bus drive capability is 12mA TTL.

Drive Interface Driver/Receiver - FDD drive interface drivers/receivers. Drive capability is 38mA. Schmitt Trigger line receivers.

Register - Consists of diskette control register and digital input/output register

Drive Interface Control - Logic to control floppy disk(s) and generate proper write pre-compensation.

TYPICAL APPLICATION
(PC/AT)



PIN ASSIGNMENTS

PIN#	NAME	PIN#	NAME	PIN#	NAME	PIN#	NAME
1	TVF8	26	INDEX	51	DIRL	76	A6
2	TVF5	27	READY	52	VSS3K	77	NC
3	TVF6	28	TRK0	53	NC	78	A7
4	POLT	29	VSS6	54	DB0	79	A8
5	TF	30	VDD6	55	DB1	80	A9
6	TV	31	VDD3	56	DB2	81	AEN
7	TVF7	32	VSS3A	57	VDD4A	82	DACK
8	VDD1	33	WRGT	58	VSS4A	83	TC
9	VSS1	34	VSS3B	59	DB3	84	DECE
10	TVF4	35	WRDT	60	DB4	85	PA2D
11	TVF3	36	VSS3C	61	DB5	86	CS
12	TVF2	37	REWL	62	DB6	87	RD
13	TVF1	38	VSS3D	63	VDD4B	88	WR
14	TPS1	39	DSL2	64	VSS4B	89	RESET
15	VDD5A	40	VSS3E	65	DB7	90	SRES
16	VSS5A	41	DSL1	66	INT	91	VDD5B
17	TPS0	42	VSS3F	67	DRQ	92	VSS5B
18	TVF0	43	MOT2	68	VDD4C	93	VDD2
19	T02	44	VSS3G	69	VSS4C	94	VSS2
20	TWIND	45	MOT1	70	A0	95	X1
21	TDT	46	VSS3H	71	A1	96	X2
22	TSYN	47	HSLL	72	A2	97	VDD2A
23	TP1	48	VSS3I	73	A3	98	T0
24	WPRT	49	STPL	74	A4	99	VDD5C
25	REDT	50	VSS3J	75	A5	100	VSS5C

I/O PIN DESCRIPTION

Host interface

A0 to A9
PC/AT buss address lines (input)
DB0 to DB7
Bi-directional, Tri-stated data buss (input/output)
RD/
Low true, signal to read data or status of LSI (input)
WR/
Low true, signal to write data or command to LSI (input)
AEN
Address enable from host. Held true during DMA transfer (input)
DRQ
Data request for DMA mode (output)
INT
Set true when the command execution is completed (output)

DACK/
Low true, acknowledged data request, DRQ (output)
TC
Request for data transfer termination (output)
SRES
System reset (input)
RESET
Internal reset signal, used for power on reset (input)
DECE
Set true, enables internal address decoder (input)
CS/
Low true, chip select. Signal valid only when DECE set low (input)
PA2D
Selects primary or secondary address for internal address decoder (input)
Low = 3FXh
High = 37Xh

Drive Interface

DIRL
Sets direction of head movement (output)
Low = toward spindle/ID
High = away from spindle/OD

STPL
Low active, pulse for track to track actuator movement (output)

HSLL
Head select (output)
Low = head 1
High = head 0

MOT1
Motor on for drive 0 (output)

MOT2
Motor on for drive 1 (output)

DSL1
Low active, selects drive 0 (output)

DSL2
Low active, selects drive 1 (output)

REWL/DENS
Density select (output)
High = high density
Low = standard density

POLT
Tied high, inverts REWL/DENS signal

WRDT
Write data, serial clock and data bits to selected drive (output)

WRGT
Low active, enables write operation to selected drive (output)

TRK0
Low active, drive at track 0 (input)

READY
Low active, drive is ready for seek, read or write (input)

INDEX
Low active, drive heads are at beginning of track (input)

REDT
Read data, raw data from selected drive (input)

WRPT
Low active, drive media is write protected (input)

NOTE:

TVF5/TVF6
Manufacturing test pins, **must be connected together for normal operation**

Power Pins

VDD5A, VDD5B, VDD5C, VDD6
Digital, +5 volt supply

VSS5A, VSS5B, VSS5C, VSS6
Digital, GND

VDD4A, VDD4B, VDD4C
Tri-state, +5 volt supply

VSS4A, VSS4B, VSS4C
Tri-state, GND

VDD1
VFO/analog, +5 volt supply

VSS1
VFO/analog, GND

VDD2, VDD2A
Oscillator, +5 volt supply

VSS2
Oscillator, GND

VDD3
38mA drive, +5 volt supply

VSS3A to VSS3K
38mA drive, GND

NCL2020 Write Precomp Values

125ns @ 500KB
208ns @ 300KB
250ns @ 250KB

INTERNAL REGISTERS

NCL2020 controller, PC/AT compatible register addresses.

Register Address

PRI	SEC	READ	WRITE
3F2	372	-------	digital output
3F4	374	main status	main status
3F5	375	diskette data	diskette data
3F6	376	-------	fixed disk
3F7	377	digital input	diskette control

Digital Output Register
The digital output register is an output only register used to control drive motor(s), drive selection and feature enable.

Bit 7	reserved
Bit 6	reserved
Bit 5	motor enable, drive 1
Bit 4	motor enable, drive 0
Bit 3	enable interrupts and DMA
Bit 2	reset
Bit 1	reserved
Bit 0	drive select (0=0)

Digital Input Register
The digital input register is a read only register. Only bit 7 is utilized in the floppy control.

Bit 7	diskette change
Bit 6	fixed disk
Bit 5	
Bit 4	
Bit 3	
Bit 2	
Bit 1	
Bit 0	fixed disk

Diskette Control Register
The diskette control register is used to select the desired data rates which controls the internal clock generation. Only bits 1 and 0 are used.

Bit 1	Bit 0	
0	0	= 500Kbit
0	1	= 300Kbit
1	0	= 250Kbit

Main Status Register
The main status register containes the status information of the selected floppy drive and may be accessed at any time.

Bit 7	request for master
Bit 6	data input/output (0=data from host)
Bit 5	non DMA mode
Bit 4	FDC busy
Bit 3	reserved
Bit 2	reserved
Bit 1	drive 1 busy
Bit 0	drive 0 busy

Status Register 0

Bit 7,6	interupt code
	00 = normal termination
	01 = abrupt termination
	10 = invalid command
	11 = abnormal termination
Bit 5	seek end (1 = seek complete)
Bit 4	equipment check (1 = fault/no trk 0)
Bit 3	not ready
Bit 2	head address
Bit 1	unit select 1
Bit 0	unit select 0

Status Register 1

Bit 7	end of cylinder
Bit 6	not used
Bit 5	data error (CRC)
Bit 4	overrun
Bit 3	not used
Bit 2	no data/sector
Bit 1	not writeable
Bit 0	missing address mark

Status Register 2

Bit 7	not used
Bit 6	control mark
Bit 5	data error (data field)
Bit 4	wrong cylinder
Bit 3	scan equal hit
Bit 2	scan not satisfied
Bit 1	bad cylinder
Bit 0	missing address mark (data field)

Status Register 3

Bit 7	fault
Bit 6	write protected
Bit 5	ready
Bit 4	track 0
Bit 3	two sided
Bit 2	head address
Bit 1	unit select 0
Bit 0	unit select 1

NCL2020 COMMAND SET

Compatible to industry standard 765 FDC, the NCL2020 is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the host and the result of the command may also be a multibyte transfer back to the host. With multibyte transfers, each command has three phases; command, execution and result phase.

Command Phase - FDC receives all information required to perform a particular operation.
Execution Phase - FDC performs the operation it was told to do.
Result Phase - After the operation is complete, status and other information are made available to the host.

COMMANDS

Read Data
Read Deleted Data
Write Data
Write Deleted Data
Read ID
Format A Track
Read A Track
Scan Equal
Scan Low or Equal
Scan High or Equal
Seek
Recalibrate
Sense Interrupt Status
Sense Device Status
Specify

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings
Power supply VDD
-0.5 to 7.0 volts
Input voltage VI
-0.5 to VDD +/-0.5volts
Output voltage VO
-0.5 to VDD +/-0.5volts
Operating current
70 mA
Operating temperature
0 C to 65 C
Storage temperature
-65 C to 150 C
Lead temperature
260 C for max. of 10 sec.

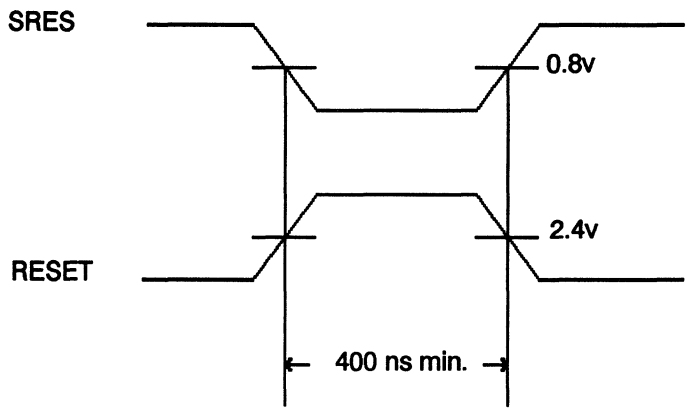
DC Characteristics VDD = 5v +/-5%, 0 to 65 C
VDC supply VDD
4.75 to 5.25 vdc
High level input voltage VIH
2.0 to VDD +/-0.3v
Low level input voltage VIL
-0.3 to 0.8v
High level output voltage VOH
2.4 to VDDv
Low level output voltage VOL
0.0 to 0.4v
Low level output current VOLD
38mA @ 0.4v
Supply current ICC
TBA

Tristate
High level output voltage VOHT
-3mA @ 4.0v
Low level output voltage VOLT
12mA @ 0.4v

Schmitt Trigger
Input voltage
VT+ = 1.6 to 2.0v
VT- = 0.9 to 1.3v

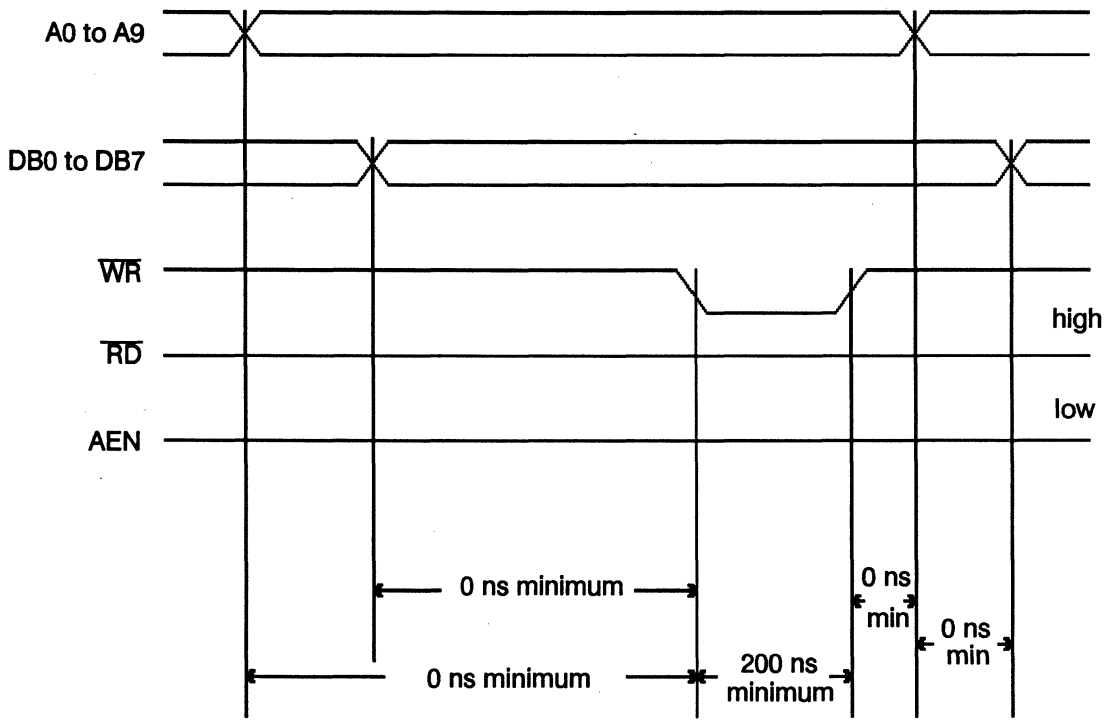
NCL2020 TIMING DIAGRAMS

RESET, SRES TIMING

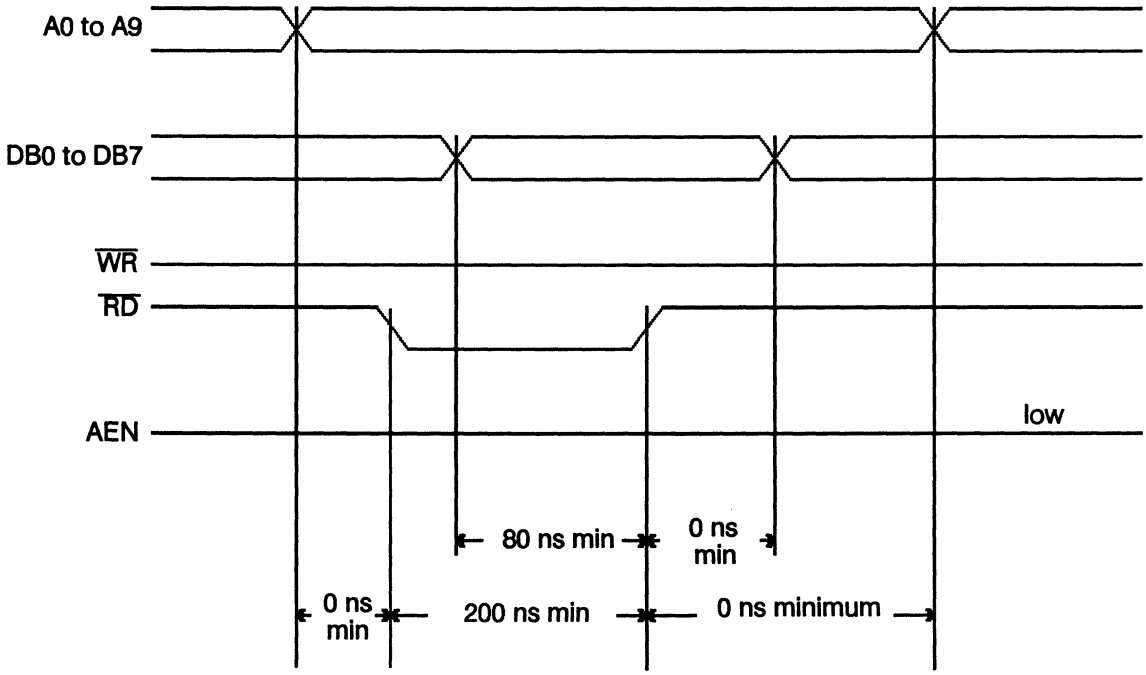


NOTE:
Requires a minimum of 2 us wait before a read/write to internal registers

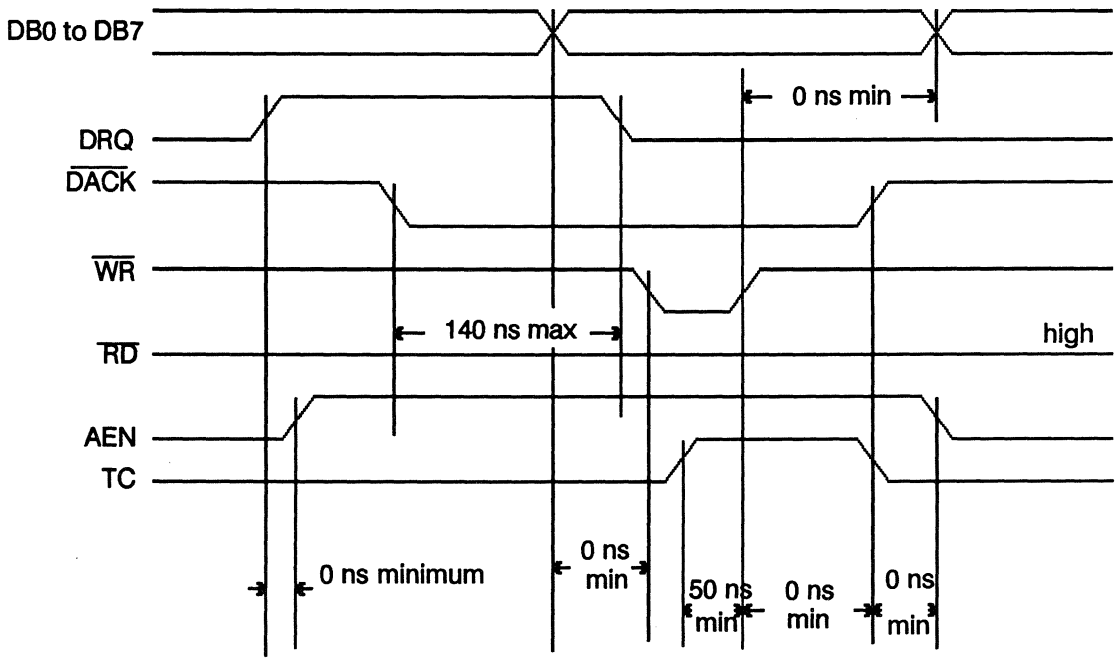
COMMAND SET/DATA SET TIMING



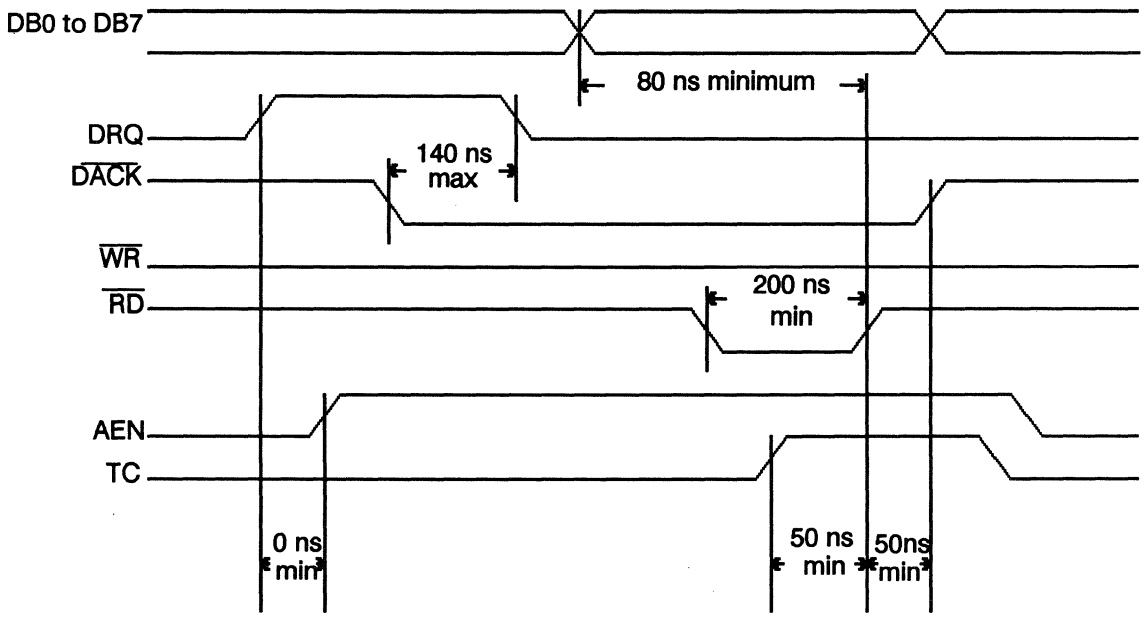
STATUS READ/DATA READ TIMING



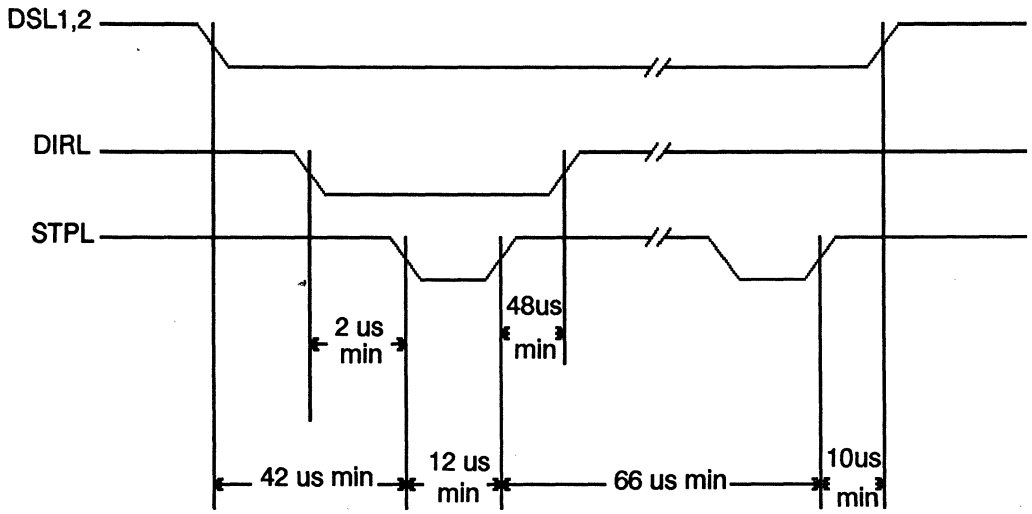
DMA, WRITE TIMING



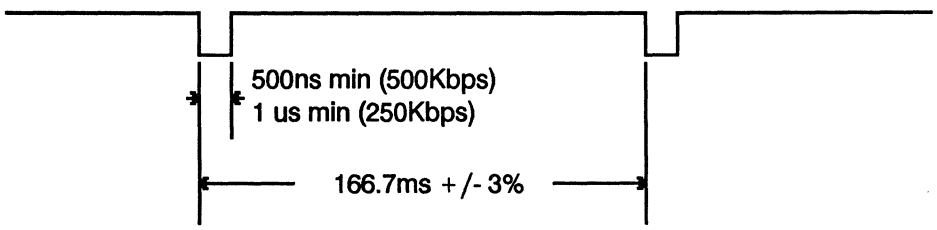
DMA READ TIMING



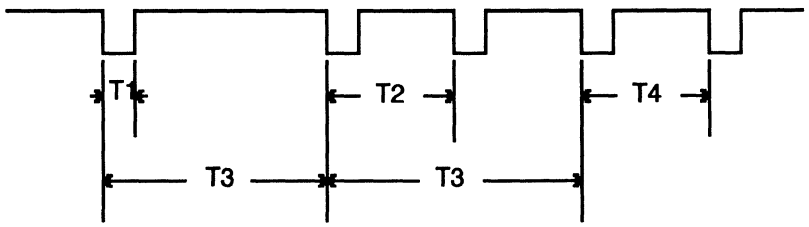
SEEK OPERATION TIMING



INDEX TIMING

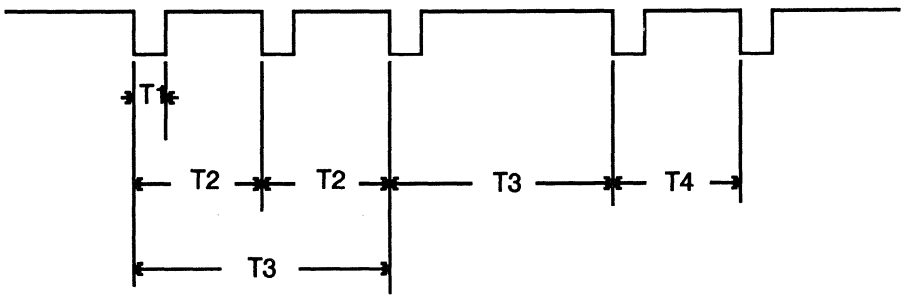


WRITE OPERATION TIMING



DENSITY	T1	T2	T3	T4
High Density (500Kbits)	150 - 1100ns	2us +/-10ns	4us +/-20ns	3us +/-15ns
Normal Density (250Kbits)	150 - 2100ns	4us +/-20ns	8us +/-40ns	6us +/-30ns
Normal Density (300Kbits)	150 - 1800ns	3.33us +/-17ns	6.67us +/-33ns	5us +/-25ns
Format	FM	FM	FM	MFM

READ OPERATION TIMING



DENSITY	T1	T2	T3	T4
High Density (500Kbits)	200ns +/-50ns	2us +/-400ns	4us +/-800ns	3us +/-600ns
Normal Density (250Kbits)	200ns +/-50ns	4us +/-800ns	8us +/-1600ns	6us +/-1200ns
Normal Density (300Kbits)	200ns +/-50ns	3.33us +/-667ns	6.67us +/-1333ns	5us +/-1000ns
Format	FM	FM	FM	MFM

AC CHARACTERISTICS

Power Supply Ripple
VFO supply, 50 mV maximum
Other, 100 mV maximum

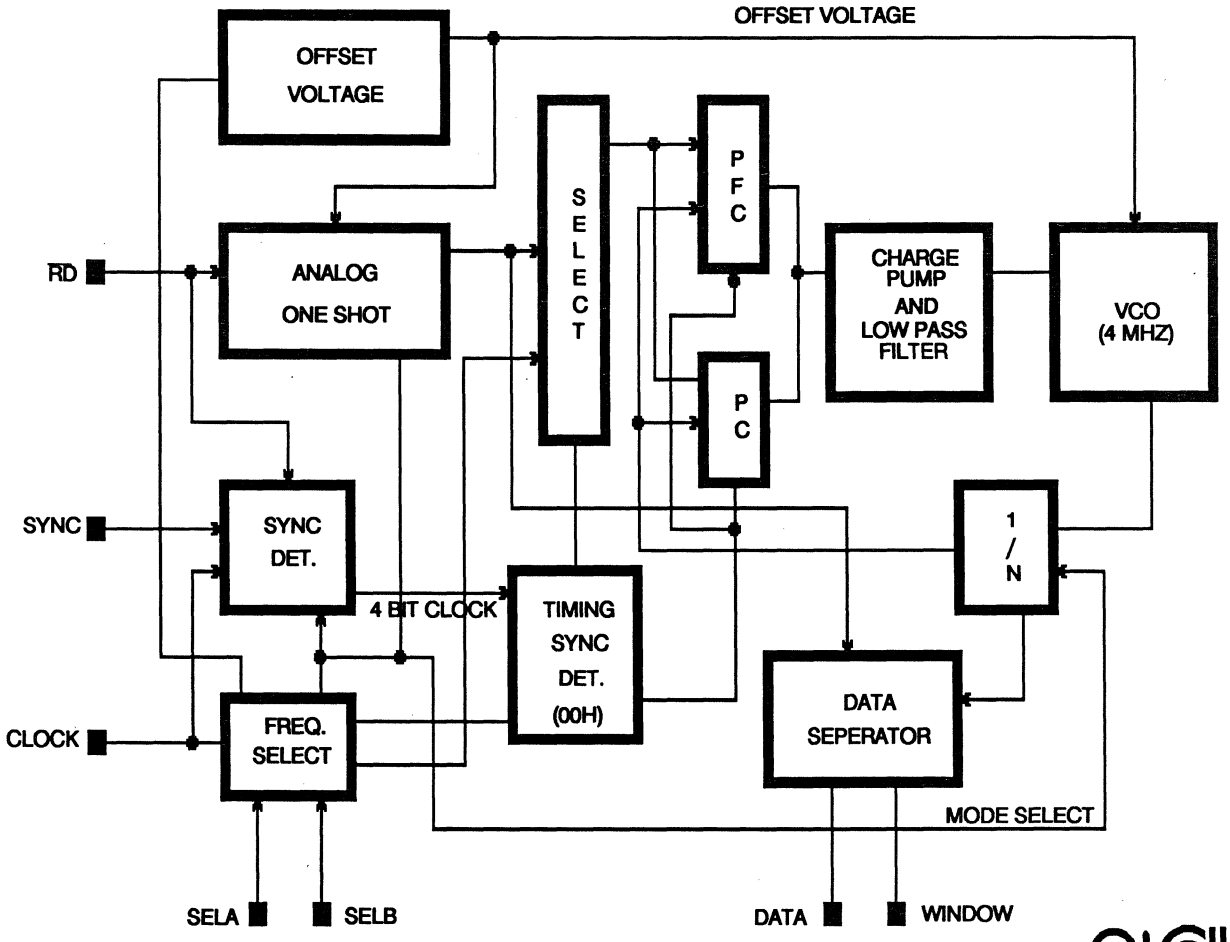
Data Seperator
Analog "one shot" pulse
-5 to 5% @ VDD = 5v +/-5%
0 to 70 C
VCO center frequency
-10 to 10% @ VDD = 5v +/-5%
0 to 70 C
control voltage = 2v

VCO control voltage variation
1.0 min, 1.25 typ, 1.5Mhz/V max
@ VDD = 5v, 25 C
control voltage = 2 to 3v
Read data detection frequency (00H)
500Kbit/s = 1.42 min, 2.00 typ, 2.58us max
300Kbit/s = 2.35 min, 3.33 typ, 4.30us max
250Kbit/s = 2.68 min, 4.00 typ, 5.16us max

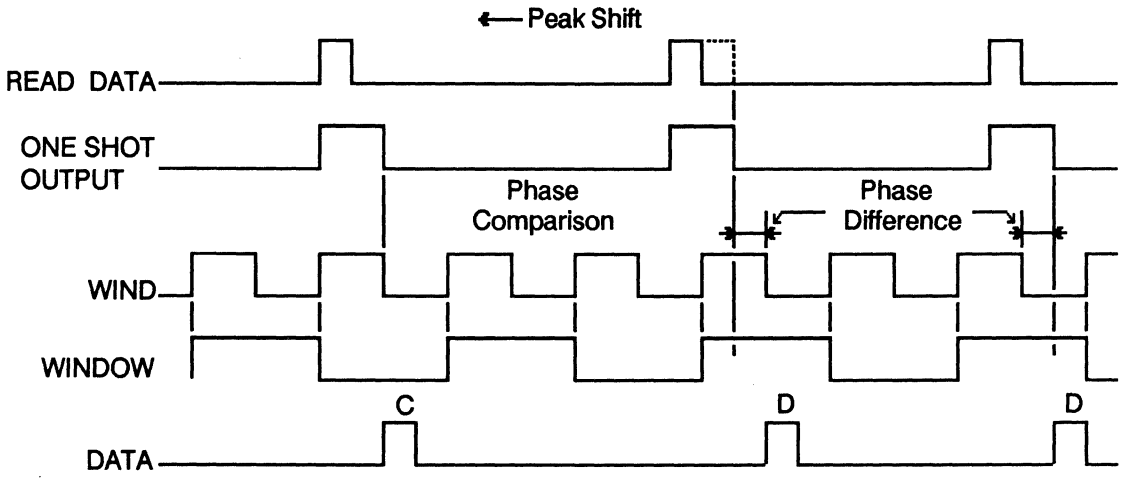
Maximum OSC Frequency
24Mhz @ VDD = 5v +/-5%
0 to 70 C

DATA SEPERATOR

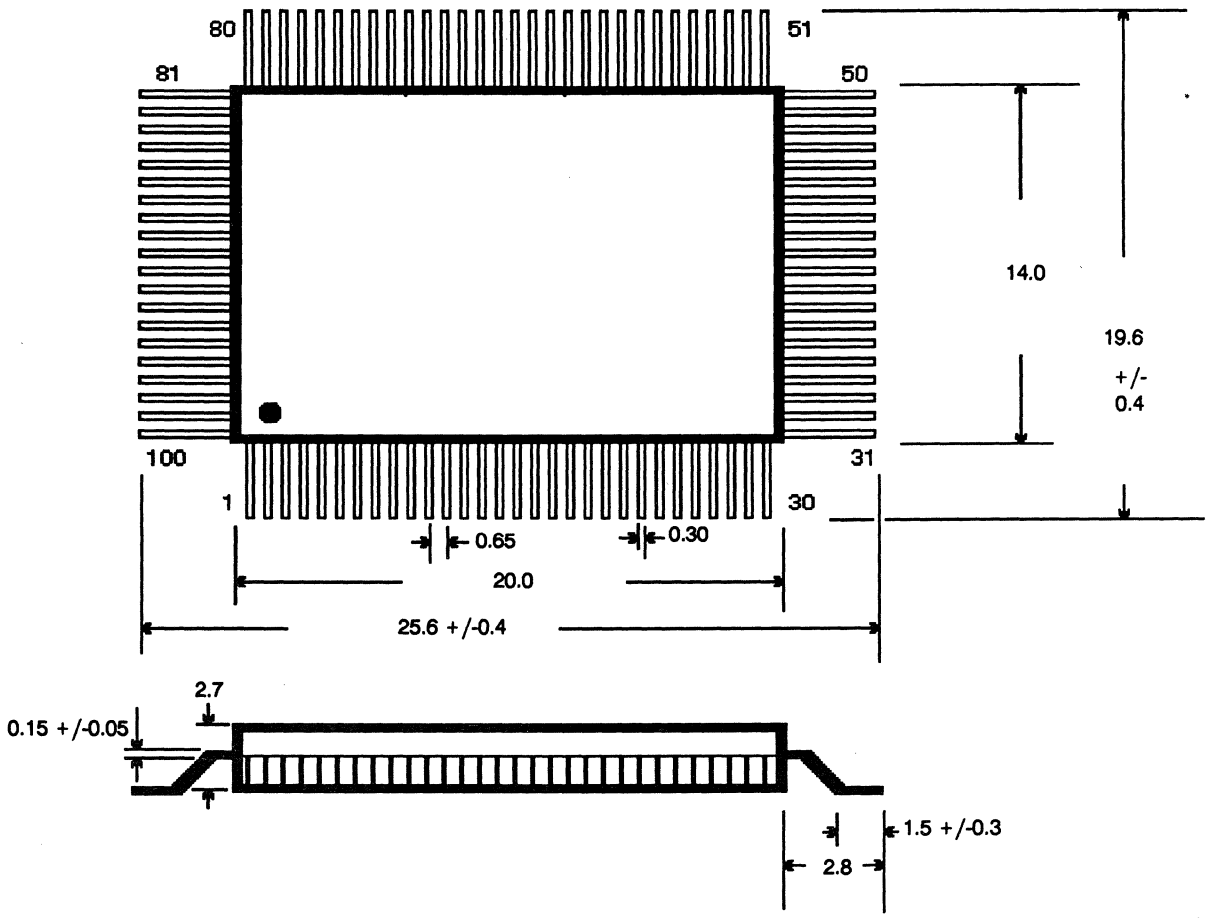
VFO BLOCK DIAGRAM



DATA WINDOW TIMING



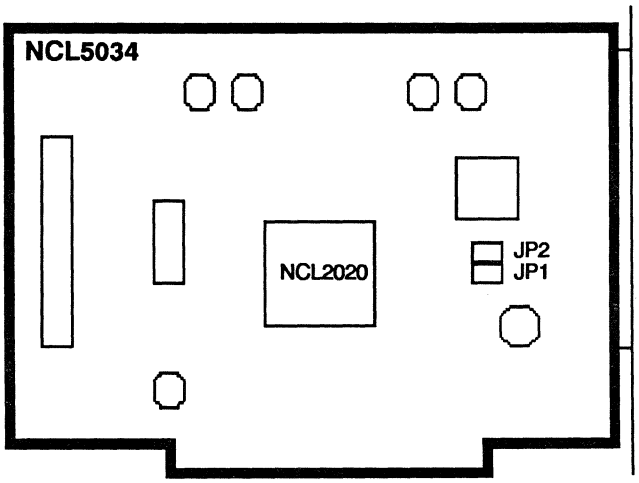
PHYSICAL DIMENSIONS (mm/tol. +/- 0.1)



JUMPER DESCRIPTION (NCL5034 eval. board)

JP1 - Jumpered, selects PS/2 mode (inverts REWL/DENS signal for 1.44 MB floppy)

JP2 - Jumpered, selects 3FX secondary address, open selects 37X primary address



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NCL2020 EVALUATION

Samples of the NCL2020 floppy disk controller are available in both chip and board forms.

The NCL5034 board is PC/AT compatible and allows easy evaluation of the NCL2020. No other equipment is required.

Contact NCLA for further information.

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