APPLICATION		REVISIONS			
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APPD

APPD

TITLE

SERIES 32000

User's Information

National Semiconductor Corporation

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SIZE A | DWG NO 422009735-001 | REV B

SHEET 1 OF 11

USER INFORMATION

NS32016-6 CPU, Revision N
NS32016-8 CPU, Revision N
NS32016-10 CPU, Revision N

August 8, 1985

1. During the instructions MULi, MEIi, DEIi and LPRi, if an Abort trap occurs on the second operand, this may cause the wrong Interrupt Table entry to be referenced, and thereby cause the Abort to transfer control to the wrong interrupt/trap service routine. The service routine actually invoked will depend on the value of the first operand (MUL, MEI, DEI), or on the state in which a previous instruction leaves the CPU (LPR) and is therefore unpredictable in general. However, it appears that the specific cases "LPR PSR" and "LPR INTBASE" will consistently transfer control to the Trap(ILL) service routine when this failure occurs. This problem is often associated with either HOLD/HLDA DMA or WAIT states.

2. The Floating-Point instructions:

   FLOORLB, FLOORLW
   ROUNDLB, ROUNDLW
   TRUNCLB, TRUNCLW

   will fail if the source operand is an immediate value, by bringing the CPU and FPU to a mutual deadlock. The CPU causes this deadlock by not issuing the whole immediate operand to the FPU.

3. The instructions CMPF and CMPL, if they generate a Trap(FPU), may cause the CPU to read the trap's interrupt descriptor from an address other than INTBASE + h'0C, or they may bring the CPU to an internal deadlock, requiring a reset. The bad address will be in the range INTBASE + h'2000 through INTBASE + h'327FC, depending on the exact encoding of the most significant 16 bits of the Basic Instruction field of the instruction. Note that the only condition under which these instructions will generate Trap(FPU) is when they are given a Reserved operand value. See the Instruction Set Manual, Section 3.3.

   MMU instructions can also trigger the above symptoms if a Rev. K1 or earlier MMU is used and DMA requests are occurring using the HOLD pin. However, this is only one side effect of an MMU malfunction that is often fatal in other ways.

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4. If an interrupt is set pending near the end of an instruction that branches, and the target of the branch is in an invalid page, an abort can occur after the interrupt has begun internal service within the CPU. Two results of this have been reported:

   1) When the Abort trap is taken the I, P and S bits of the PSR image on the stack may be cleared. In most systems this damage can be repaired by the Abort trap service routine, using the rule that if the U bit of the PSR image is set, then the S and I bits should also be set.

   2) When the Abort trap is taken, the PSR, MOD and PC images may be stored to the wrong addresses near the top of the Interrupt Stack. This is fatal if it is allowed to occur.

   Both manifestations of this bug may be bypassed by synchronizing the INT and NMI inputs so that they become active during the PFS pulse from the CPU. The NMI pulse from the MMU must bypass this synchronization in order to perform Interrupt-Mode breakpointing correctly. MMU Execution breakpoints must never be used in Interrupt Mode, as they can trigger this bug.

5. The following instruction forms should not appear after an instruction with an operand of access class "rmw":

```
ADDR    Rj[Rx:i],anydest
CHECKi  anyreg,Rj[Rx:i],anysource
CVTP    anyreg,Rj[Rx:i],anydest
```

   Doing so can cause the effective address of the first general operand to be computed incorrectly. Use instead the form 0(Rj)[Rx:i], which is identical in effect to Rj[Rx:i] but is not susceptible to this bug.

6. Shift instructions of the form:

```
LSHW    any-source,TOS
LSHD    any-source,TOS
ASHW    any-source,TOS
ASHD    any-source,TOS
```

   may misinterpret the sign and magnitude of the first operand, causing an incorrect shift direction and count. Use 0(SP) instead of TOS to bypass this problem.

7. In executing the RETT instruction, the CPU will sometimes read the MOD register value from the wrong address, and also with incorrect byte order and/or missing bytes. The related instruction RETI does not fail in this manner in an NS32016. The incorrect address will be offset by a small amount (+/- 1 byte) from the correct address. The instruction continues by attempting to read the SB value from the incorrect address in the MOD register. This problem is associated with a specific set of timing sequences on the bus, involving HOLD/HLDA DMA and/or WAIT states. It can be bypassed (in an NS32016 only) by aligning the RETT instruction so that it occupies one word (16 bits) on an even address, and is therefore fetched in one memory cycle. Doing this prevents the sequences that lead to this failure.

8. DMA requests made to the CPU on the HOLD pin may cause the CPU to lock up if they are made during the T1, T3 or Ti CPU states. HOLD requests must be qualified so that they are applied only during T2 or T4 while the PHI2 clock is active and must also be inhibited during slave operation. This problem is very unlikely to occur.

9. At higher ambient temperatures (above 40 degrees C), the CPU may perform interrupt service more than once in response to a pulse on the NMI pin.

DATA SHEET CLARIFICATION

1. As of Revision N of the CPU, it is no longer true that the CPU floats its ADS pin when the FLT signal is received from the MMU. The ADS pin no longer needs to be connected to a pull-up resistor unless a DMA controller is being used in the system.

2. A 10K pull-up resistor is required on the SPC/AT line.

3. Normally, when the CPU receives a DMA request on the HOLD pin it will float the HBE pin when it grants the bus. However, with an MMU attached, if the HOLD request occurs during an MMU page table lookup the CPU does not (and must not) do this, as it does not have sufficient information to synchronize the release of HBE to the MMU's bus cycles. An external tri-state buffer must be used on HBE in systems with an MMU and a DMA controller.

4. In systems containing an MMU, the HBE signal should not be latched externally on the rising edge of the PAV pulse as addresses are. When the MMU performs a Page Table access, and then removes the FLT signal to the CPU, there is a delay from the point that FLT is inactive to the point that HBE is valid which causes such latching to be unreliable at higher clock rates. See Figure 4-9 in the NS32016 data sheets, timing parameter tHBEr.

5. For reliability purposes it is strongly recommended that HOLD, INT and NMI be synchronized with the PHI clock. This can be accomplished by using external flip-flops clocked by the rising edge of the CTTL signal from the NS32201.

6. The minimum clock frequency for the 32000 family processors, CPU, MMU, and FPU, is 4 Mhz instead of 200 Khz as stated in the data sheets.

USER INFORMATION

NS32082-6 MMU, Rev. L
NS32082-8 MMU, Rev. L
NS32082-10 MMU, Rev. L

August 8, 1985

1. Breakpoints can not be used reliably with this revision of MMU.

2. Since the MMU alters the state of the M bit position in the Level-1 Page Table Entry (PTE), due to a bug in this revision of MMU, Level-1 PTE's should be initialized with the M bit position set to avoid any inefficiency. To workaround another bug in the current revision, the M bit in the Level-2 PTE should always be kept set.

3. The HLDAO signal will glitch if a DMA request (on the HOLD pin) is set pending during the last page table lookup cycle before the MMU aborts the CPU. The glitch is approximately simultaneous with the falling edge of the ABT pulse, and can last up to about 40 ns.

4. Upon powering up the MMU and placing it in 16-bit mode (A24 pin held high on the rising edge of RST, see Data Sheet Clarification item "b" below), the MMU may be placed in a mode in which it actively asserts an address (contents undefined) on the A16-A24 pins through T1 of the first memory cycle performed by the CPU. This address conflicts with the address asserted by the CPU during T1 (which should be zero), causing the first word of the first instruction to be fetched from an incorrect address. In 32-bit mode, the incorrect initialization has no side effects, and the MMU recovers without symptoms. 32-bit mode can be used in 32016-based systems if address bits A16-A24 are latched in the same manner as AD0-AD15.

5. HLDAO is released during the same clock cycle that generates PAV.

Data Sheet Clarifications

The following are clarifications or corrections to the March 1982 NS32082 Data Sheet:

a. The Program Flow features and Non-Sequential Trace Trap are being deleted as features of the MMU. The registers PF0, PF1 and SC are no longer supported. The MSR bits FT, UT and NT should always be kept zero for future compatibility.

b. There is a new 32-bit bus mode strap option not documented in the current data sheet. Pin A24 is sampled at reset. If A24 is high, 16-bit bus mode is selected, and the MMU operates as documented. If A24 is low, 32-bit bus mode is selected for use with the NS32032 microprocessor. In 32-bit bus mode, the MMU drives addresses on lines AD0-AD23 only during TMMU and during Page Table lookups, freeing these bus pins for data transfer from T2-T4. All address bits, including A16-A23, must be latched on PAV in this mode.

c. The BST, EST, BD, ED, TET and ERC fields are cleared if and only if the MSR is loaded with a value in which bit 1 is set (e.g.: hex 00010002 enables User Mode translation and clears the above status fields).

d. As of MMU Revision G, it is no longer true that the BPR0 register cannot count write cycles. Bits BW and CE may both be set (DBG16 options /W and /C both selected).

As of MMU Revision H, however, there remains a limitation that the BR, BW and CE bits must not all be set (DBG16 options /R,/W and /C).

e. The MMU alters the state of bit 4 of Level-1 Page Table Entries. Any information stored in that bit by software will be destroyed.

USER INFORMATION

NS32081-6 FPU, Revision D
NS32081-8 FPU, Revision D
NS32081-10 FPU, Revision D

August 8, 1985

1. The MOVLF instruction, with Operand 1 value of zero, will return the correct value of zero, but will set the Underflow Flag bit in the FSR. If the UEN (Underflow Trap Enable) bit is set, a TRAP(FPU) will occur. This will be corrected in the Rev. E NS32081.

2. While transferring operands into the Rev. D FPU, do not allow any delays between SPC pulses longer than 10 milliseconds. Doing so will cause this revision of the FPU to lose its internal state until the next FPU instruction is initiated. One observed side-effect of this has been a string of SPC pulses coming from the FPU, which may falsely activate other slave processors. In NS32000-based systems, do not allow DMA bursts longer than 10 milliseconds during FPU instructions, and if an abort occurs during an FPU instruction make certain that the abort trap handler promptly executes an FPU instruction in order to cancel the protocol that was in progress. This problem will be corrected in the Rev. E NS32081.

3. Performing a conversion from floating-point to integer (instructions: ROUND, TRUNC or FLOOR) on certain odd integral values (examples: 1.0, 3.0) and all negative integral values generates an erroneous inexact result flag. This will be corrected in the Rev. E NS32081.

4. If the FPU is used in a system that includes the MMU and the MMU aborts the fetch of the last word of the final operand, when the instruction is retried following the abort service routine the FPU will not latch the new operand data. This will cause the result of the retried instruction to be incorrect. To workaround this bug, the SFSR instruction should be used in the abort routine before doing any other floating point instruction. This will be corrected in the Rev. F NS32081.

DOCUMENTATION CLARIFICATION

The following are clarifications or corrections to the current NS32081 FPU documentation:

1. When the FPU signals that it is finished processing an instruction (by pulsing the SPC pin low), it is necessary to wait for at least two cycles of the clock (CLK) before reading the Status Word. Series 32000 CPU's satisfy this requirement.

2. After reading the Status Word from the FPU, it is necessary to wait for three cycles of the CLK clock before reading a result. Series 32000 CPU's satisfy this requirement.

3. Whenever an FPU error condition occurs, the FSR TT field is loaded with the error code, regardless of whether that condition is enabled to cause a trap. An FPU instruction can therefore complete normally and still display a code of 001 (Underflow) or 110 (Inexact Result). This code remains in the TT field only until the next floating-point instruction (other than SFSR) completes. Early documentation has strongly implied that the TT field will appear non-zero only if a trap actually occurs. This has been fixed in the Series 32000 Instruction Set Reference Manual, Doc. No. 420010099-001B, and in the Series 32000 Databook.

4. The FSR TT field is loaded with a new error status value (zero if no error) at the end of every floating-point instruction except LFSR or SFSR. (The LFSR instruction loads the TT field, but with the value supplied by the programmer instead of with error status). Most documentation to date, however, has stated that the FSR TT field is altered only if an error occurs or if the LFSR instruction is executed. The necessary changes appear in the Series 32000 Instruction Set Manual, Doc. No. 420010099-001B, and in the Series 32000 Databook.

5. Asynchronous timing of SPC pulses with respect to CLK does not work reliably. Transfers to the FPU must follow NS32000-series CPU timing exactly: i.e., the SPC pulse must start shortly after a CLK rising edge and terminate shortly after the next rising edge. If the FPU is used as a Slave Processor with a Series 32000 CPU, it should be clocked with the TCU CTTL signal. The necessary changes have been made in the Series 32000 Databook.

6. When transferring the ID Byte and the Operation Word to the FPU, there must be a gap of at least one clock cycle between T4 of the ID Byte transfer and T1 of the Operation Word transfer. Failure to do this can make register-to-register forms of FPU instructions execute unreliably. This requirement is met by 32000-series CPU's. Data sheets and Application Note AN383 do not yet mention it.

7. The value given for the DC characteristic II (Input Leakage Current) is incorrect. It should be -20 uA (min) to +20 uA (max).

8. The parameter tDf is 50 ns maximum for all speed versions. The parameter tSPCFnf is 0 minimum for all versions.

9. The minimum clock frequency (CLK pin) is 4 Mhz instead of 200 Khz as stated in the data sheet.

10. When the FPU is used in a system that includes the MMU, the FPU RST pin must be tied to the system reset, not the RST/ABT pin of the MMU.

USER INFORMATION

NS32202-6 ICU, Revision F
NS32202-8 ICU, Revision F
NS32202-10 ICU, Revision F

July 24, 1985

DATA SHEET CHANGES/CLARIFICATIONS

1. If edge-triggered interrupts are to be handled, the TPL register should be programmed before the ELTG register, contrary to what the initialization flowchart in the ICU data sheet implies. This prevents spurious interrupt requests from being generated during the ICU initialization from edge-triggered interrupt positions.

2. If any cascaded ICU is used, the CSRC register should be cleared during initialization (if the initialization does not follow a hardware reset) by writing zeroes into it. This should be done before setting the bits corresponding to the cascaded interrupt positions. This operation ensures that the 4-bit in-service counters (associated with each interrupt position to keep track of cascaded interrupts) always gets cleared when the ICU is re-initialized.

3. If the ICU initialization does not follow a hardware reset, the ISRV register should be cleared during initialization by writing zeroes into it.

4. If an external interrupt must be masked off, the CPU can do so by setting the corresponding bit in the IMSK register. However, if an interrupt is set pending during the CPU instruction that masks off that interrupt, the CPU may still perform an interrupt acknowledge cycle following that instruction since it may have sampled the INT line before it is removed by the ICU. This causes the ICU to output a vector value of 'XF' Hex. To avoid this problem the above operation should be performed with the CPU INTERRUPTS DISABLED.

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