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MOS BRIEF 7

TTL/MOS/DTL INTERFACES

Some of our low-voltage MOS integrated circuits couple directly to TTL or DTL logic circuits, some take a resistor or two. Voltage translators and special buffers are not needed because the data-input stages are designed to accept relatively small changes in signal voltages as well as large MOS-style swings.

Interfaces like Figures 1a and 1b do nicely in most applications. Devices with active pullup and pulldown output stages don't even need a current-sinking resistor (Figure 1b). An input pullup resistor can be used on the shift registers (MM506, MM510 and their cousins) in high-performance applications. We've clocked them at twice the normal MOS rate with the Figure 1c interface.

A pullup resistor is required by some of our larger-scale devices, particularly those containing a lot of logic and memory on the same chip. The MM521 read-only memory in Figure 1d is one of these. But considering that the MM521 stores 256 4-bit words and can replace an entire TTL assembly, we think that a few resistors is a small price to pay.

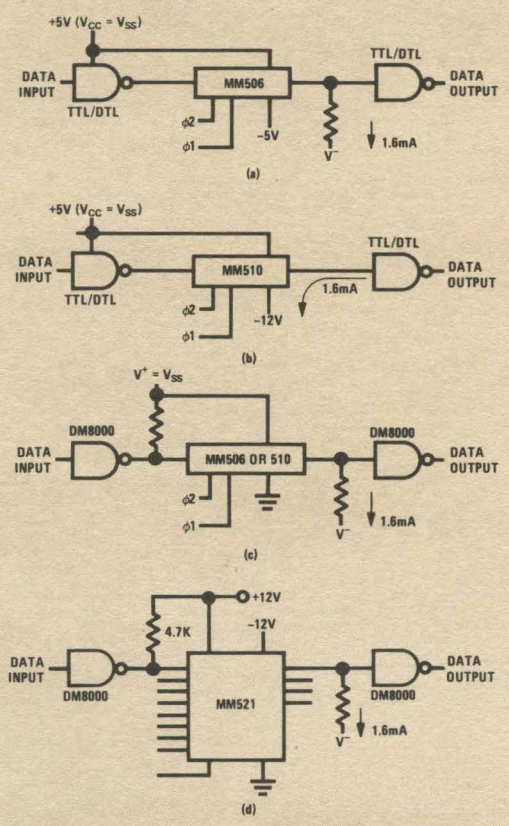

FIGURE 1. Typical TTL/MOS or DTL/MOS Interfaces.

What makes our MOS circuits so compatible? Design improvements based on better MOS processes, of course. The National Semiconductor process lowers the voltage threshold to about 2V, allowing small transitions in the data signals to be handled reliably. TTL and DTL transitions are usually 4V or less, while conventional MOS circuits demand a change of at least 7V. Some look for transitions as great as 18V.

Note, however, that the biases on the shift registers in Figure 1 are positive and negative, a la regular MOS. Although low-voltage elements are used in the input stages, they are designed with ample overdrive to establish proper MOS logic levels for the following stages' storage and switching elements. In fact, any number of our low-voltage MOS circuits can be placed in cascade between two TTL or DTL gates as long as MOS/MOS coupling specifications are met within the string.

You can usually disregard what has been the normal limits on our MOS inputs. Data levels can be as low as V_{SS}–2.5V for an MOS "0" bit and V_{SS} –4.2V for a "1". If V_{SS}, the MOS substrate voltage, is picked off the +5V supply used for TTL V_{CC}, logic levels of 2.5 and 0.4V are acceptable to low-voltage MOS inputs. They'll work even during worst-case V_{CC} ±5% and gate-loading conditions with an input resistor to V_{CC}.

At the output interface, different conditions must be satisfied (they can be calculated with the equations in Table 1). To drive a TTL gate, the MOS output stage must sink 1.6 mA of current and allow the signals to go more positive than +2.4V and more negative than +0.4V. Some designs require an external resistor to provide the negative current path, but devices with output stages like the MM510 do not. The latter design has proven itself in numerous applications, so we are using it in all appropriate new products. Either one meets the voltage spec.

Fanout is normally one, but this can often be improved by trade-offs between V_{SS} and V^-. The voltage transitions for the clock signals (ϕ_1 and ϕ_2) will have the same amplitude as specified for our MOS assemblies, but the levels should be shifted to correspond to V_{SS}. During the logic "0" clock intervals, the clock should be within 1.5V of V_{SS}.

When V_{SS} is the same as V_{CC}, it doesn't make much difference what types of TTL or DTL gates are used as signal sources and receivers. But be sure the gate can withstand its output being pulled up if V_{SS} is higher. That's why we recommend our DM8000 gates in Figures 1c and 1d. Even though its specifications read like a conventional TTL gate's, the DM8000 can be pulled as high as +14V without breakdown (a similar quad 2-input gate circuit, the DM8810, is specified for high breakdown voltages). The DM8000 is protected by a reverse-biased diode in the emitter-follower active-pullup string and a base-to-emitter resistor biases off the output-sinking transistor (see Figure 2). Also, the DM8000 has no trouble sinking the current required for an MOS input at the +0.4V level. It can handle 16 mA.

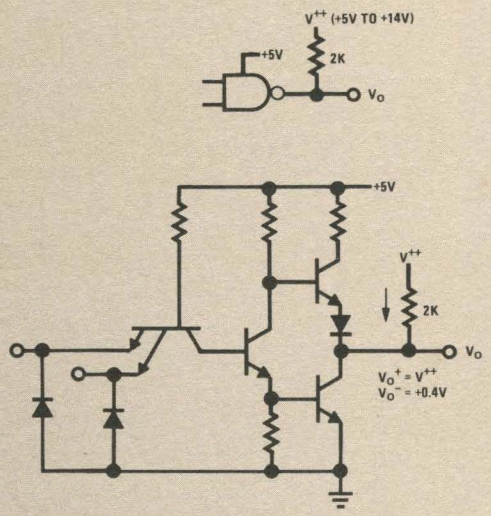

FIGURE 2. DM8000 Output Pullup Technique.

Another handy feature of these DTL or TTL/MOS/TTL interfaces is that there are no logic inversions through the interfaces. Of course, the MOS stages in an application like Figure 3 see each

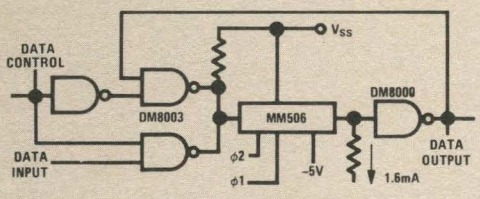

FIGURE 3. Recirculating MOS Delay Line with TTL or DTL Control.

TTL "1" bit as an "0" and vice-versa. But that's of no concern to the rest of the system. Nor need it bother the logician. Furthermore, when there are several MOS circuits between interfaces, TTL data can be taken off the MOS signal connections providing the loads do not severely degrade the MOS logic levels. Don't try this with conventional MOS, though.

Both the 5V and 12V techniques shown reduce interfacing costs to a minimum. Inserting MOS devices into an otherwise TTL or DTL system can lower the cost per bit significantly when the application calls for shift registers, small memories and similar functions. Both methods are equally convenient, since neither requires an additional power-supply connection. Most systems contain 5V and 12V supplies for other purposes. So the choice depends on the voltages that are most compatible with the rest of the system and performance factors such as the operating frequency desired.

Detailed information on low-voltage MOS devices and instructions on clocking and other auxiliary circuits can be found in National Semiconductor literature.

Table 1. Output Conditions

In MOS logic "0" state:

$$\frac{V_{SS} - 2.4V}{Z_o} \geq \frac{2.4V - V^-}{R_o}$$

In MOS logic "1" state:

$$I_1 \leq \frac{0.4V - V^-}{R_o}$$

Definitions:

I_1 = Current through R_o at V_o = +0.4V (1.6 mA)
R_o = Output resistor (internal or external)
Z_o = MOS output impedance
V^- = Supply sinking negative current
V_{SS} = Most positive voltage
V_{DD} = MOS drain voltage

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